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Effect of coarsened microstructure on electromigration behavior of eutectic Pb-Sn solder joints

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Effect of coarsened microstructure on electromigration behavior of eutectic Pb-Sn solder joints

By

Yi-Chih Lee

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ABSTRACT

Effect of Coarsened Microstructure on Electromigration behavior of Eutectic Pb-Sn Solder Joints

By

Yi-Chih Lee

Electromigration (EM) induced atom/ion movements in two-phase alloys should depend on the size, shape, and distribution of both phases present. In order to evaluate the roles of such morphological features on hillock/valley formation, and details of microstructure evolution resulting from EM, joints made with eutectic Sn-Pb solder were isothermally aged to coarsen the microstructure prior to current stressing. Effects of coarsened microstructure on the events resulting from EM, when compared to those noted in as-reflowed solder joints, indicate the roles of initial morphological features of the phases present on the electromigration in a two-phase alloy.

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1. Introduction

1.1 Electromigration is a significant reliability concern

Electromigration is the movement of the conducting materials due to interactions between conducting electrons and diffusing metallic atoms/ions. It was not a significant issue before 1970s since the current density in these earlier electrical and electronic systems were well below the electromigration limit [1]. Due to the continuous miniaturization of electronic devices, the current density reaches a level that is large enough to make electromigration a significant issue. In an example of a VLSI process, where integrated circuits are created on a single chip, thousands of transistor circuits are connected with Cu thin-film line in dimension that are about 0.5 μm wide and 0.2 μm thick. In such a circuit, a current as small as 1m Amps can result in current density of about 10^6 A/cm^2.

In direct current (DC) stressing, the atomic movement due to electromigration will cause void formation at the cathode and extrusion at the anode. These defects result in failure of these thin film integrated circuits [2]. The continuous miniaturization of electronic device results in smaller interconnects and a high current density imposed on these interconnects can cause the electromigration, such an event affects the electrical and mechanical reliability of solder joint interconnects.

The approach in quantifying effect of electromigration in electronic devise is the mean time to failure [3]. However, for the material science points-of-views, the mean time to failure due to electromigration depends on factors such as alloy composition, current density, service temperature and grain structure [4]. In this study, to isolate the

relationship between coarsened microstructures and electromigration behavior, eutectic Pb-Sn solder joints were isothermally aged to different extents, leading to different microstructure prior to the application of current stressing.

In the following section, the mechanism and phenomena of electromigration will be described briefly. Issues in accelerated electromigration of solder joint are presented below in order to reveal the links to various factors influencing electromigration. Then problems existing in the currently popular joint configuration will be discussed in order to give a clear picture that justifies development of a new solder joint design. The complexity of microstructure after electromigration needs a systematic analysis method to quantify and compare the results. Finally, the motivation and aim of this study will be presented.

1.2 Electromigration behavior

i. Phenomenon

Under high current density, electromigration-induced damages will occur. The corresponding microstructural changes include certain phenomena, such as valley/hillock formation in the solder region [5], significant phase segregation of Pb-rich and Sn-rich domains [6], asymmetric growth of Cu-Sn intermetallic layers at the interfaces [7], and excessive depletion of Cu at the cathode side [8].

a. Hillock and Valley formation due to electromigration

Electromigration is a serious concern in electronics under high current density and results in manifestation of visible surface features such as hillock and valley formation. This phenomenon occurs when electrons move to cathode while metallic ions

move to the anode during the passage of electric current. Then, such movements result in extrusions at the anode and voids at the cathode, which one call hillock and valley formation at the cathode and at the anode, respectively. In other words, electromigration behavior will change a flat solder surface into a buckled surface, which indicates the cathode side has sunk in and the anode side has bumped out.

According to Lee et al. [10], by using confocal laser scanning microscopy (CLSM), the height of the hillock and the depth of the valley can be measured. It is worth noting that the valley appears to be deeper than the height of hillock. It is because the valley at the cathode results from the migration of atoms away from the cathode. These atoms movement will tend to push the materials toward the free surface available at the anode, then the hillock forms. In other words, the hillock formation is a result from the blockage of atomic movements.

b. Significant phase segregation of Pb-rich and Sn-rich domains

According to Ho et al. [5], after current stressing with high current density, there will be a dense layer of a Pb-rich domain at the anode end of the solder. Adjacent to the Pb-rich layer, towards the solder will be a Sn-rich layer and a random mixture of Sn-rich, Pb-rich, and Cu_6Sn_5 phase, in sequence. Such segregation implies that the lowest energy to make this two-equilibrium phases stable can be reached only when the Pb-rich and Sn-rich domain exist as two separate domains with a single continuous interface boundary. So, under high current density, the significant two-layer segregation of Pb-rich and Sn-rich domain will be observed not only because the diffusivity of Pb and Sn under

high current density is different, but also the lowest energy can be reached only when this two-layer segregation of Pb-rich and Sn-rich phase result.

c. Asymmetric growth of Cu-Sn intermetallic layers at the interfaces

The essential process in solder joining is the chemical reaction between Cu and Sn to form intermetallic compounds:

$$6Cu+5Sn \rightarrow Cu_6Sn_5$$

$$9Cu+Cu_6Sn_5 \rightarrow 5Cu_3Sn$$

After reflow, the scallop-type Cu_6Sn_5 compounds form at solder/Cu interface. And, a very thin layer of Cu_3Sn may also form between the Cu_6Sn_5 scallop/Cu interfaces in the initial state. However, after current stressing both of Cu_6Sn_5 and Cu_3Sn transformed into layer-typed.

It is worth noting that if the joint was subjected to current stressing, massive transportation of electrons move from cathode to anode resulting in the enhancement of IMC growth at the anode, and inhibition of the IMC growth at the cathode. Therefore, at the anode, the total IMC layer always will be much thicker than that at the cathode. This is called the polarity effect of electromigration on IMC growth [7].

d. Excessive depletion of Cu at the cathode side

In addition, the transformation of 1 molecule of Cu_6Sn_5 into 2 molecules of Cu_3Sn will leave behind 3 molecules of Sn $\{Cu_6Sn_5 \rightarrow 2(Cu_3Sn)+3Sn\}$, which will attract 9 atoms of Cu to form 3 more molecules of Cu_3Sn. Therefore, the vacancy flux needed to transport the Cu atoms will accumulate at the Cu/Cu_3Sn to form Kirkendall voids. In

other words, the Cu at the cathode side will be consumed excessively. Voids are undesirable in device application; therefore it is of reliability interest to limit the growth of Cu_3Sn and reduce the depletion of Cu at the cathode.

In order to understand the fundamental failure mechanism resulting from electromigration, in-situ electromigration tests were performed by Lee et al. [10]. At the cathode side of the solder bump, the interfacial crack formed at the entry of the chip side between IMC layer and the solder. As mentioned in the previous paragraph, due to excessive depletion of Cu at the cathode, Cu was quickly consumed, followed by void formation at the contact area. The void reduces the contact area and displaces the electrical path, causing the current crowding and Joule heating inside the solder bump. A large joule heating inside the solder bumps can cause melting of the solder bump and the failure occurs quickly. Then, the interfacial crack propagates along the whole IMC layer/solder interface with increasing time resulting in a void formation along IMC layer/solder interface. Once a void is nucleated, electron flow will be interrupted.

ii. Quantitative evaluation for mean time to failure

Electromigration is associated with atomic migration resulting from electron wind. It is a serious reliability problem in electronics encountering high current densities. Such migration quite often results in manifestations of visible surface features and microstructural evolution in the interior region. At certain length of time, such migration will cause failure of the electronic device, which is called the mean time to failure (MTTF). Since the late 1960s, Black's equation [11] provided to predict current density and temperature for the mean time to failure of aluminum conductors due to electromigration.

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$$MTTF = A \bullet J^{-n} \bullet \exp(E_A/KT)$$

where,

A is the proportionality constant, J is the current density, n is the exponent on current density, E_A is the activation energy of the electromigration failure mechanism, T is temperature and K is Boltzmann constant.

It is noteworthy that the MTTF of solder bump decreases exponentially as the stressing temperature increase. Wu et al. [12] conducted electromigration tests on eutectic PbSn solder bumps, and found that the MTTF decreased from 711 hours to 84 hours when the testing temperature increase from 125°C to 150°C with an applied current density of 5.0×10^3 Amp/cm^2.

Additionally, according to Nah et al.[13], the MTTF of solder bump decreased as the current density increased. The composite solder joint used in their study did not fail after one month of current stressing at 4.07×10^4 Amp/cm^2, but they failed after 10 hrs of current stressing at 4.58×10^4 Amp/cm^2. At a slightly higher current stressing of 5×10^4 Amp/cm^2, these joints failed after only 0.6 hrs by the melting of the composite solder bumps.

These findings indicate that electromigration must be strongly dependent on the temperature and current density.

1.3 Issues in accelerated electromigration of solder bump

i. Effect of current density on electromigration

The current density is required to be larger than a critical current density to initiate and advance the atom/ion migration within a reasonable time. Besides, higher current density leads to faster electromigration. As discussed in the previous section, atomic

migration may not only occur by bulk diffusion, but also through dislocations, grain boundaries, and external surface. Although these "short circuit" diffusions are faster than bulk diffusion, they are insignificant in most situations because the cross-sectional areas of these paths are extremely small. However, as the continuous miniaturization of solder joint and the associated increases in current density, the effect of short circuit diffusion cannot be neglected. It is because the path for electromigration in these miniaturized devices is not only through lattice diffusion, but also along grain boundary and/or surface diffusion.

Chan et. al [15] classify the current density into three ranges: low, moderate, and high current density. Low current density refers to 10^0-10^1 Amp/cm^2. In the moderate range, 10^2-10^3 Amp/cm^2 is the experimental condition. High current density refers to 10^4-10^5 Amp/cm^2. Most of the electromigration studies are conducted in an accelerated manner where a high current density (10^4 to 10^5 Amp/cm^2) and a high temperature more than 100°C. On the other hand, with a moderate current density at 125°C, no significant electromigration was noted.

Thus, it was confirmed that no obvious electromigration occurred with the moderate current density. However, above a critical current density of 10^4 Amp/cm^2, significant electromigration behavior occurs.

ii. Effect of temperature on electromigration

Temperature plays an important role in electromigration. It is because electromigration occurs by an atomic diffusion mechanism. Atomic migration may not only occur by bulk diffusion, but also through dislocations, grain boundaries, and

external surface. These are sometimes called "short circuit" diffusion paths inasmuch with rates much faster than for bulk diffusion. Based on the mode of diffusion, Huntington [15] classifies the electromigration phenomenon into three types, A-C, depending on the homologous temperature ($T_H \equiv T/T_M$ where T_M is the melting temperature of alloy) as shown Table 1. If the conducting line is kept at a very low temperature (e.g., liquid nitrogen temperature), electromigration cannot occur because there is no atomic mobility of diffusion, even though there is a driving force. However, if the temperature increases at homogenous temperature below 0.5 for example, only grain boundary is the principal electromigration path. Moreover, if temperature increases to 423K (150°C), solder (T_M=456°K) typically operates well above T_H=0.5 in Type A diffusion where lattice and grain boundary diffusion domains. In other words, the diffusion rate increases causing significant electromigration.

Thus, higher temperature accelerates the electromigration behavior. On the other hand, it is difficult to investigate electromigration behavior at lower temperatures.

Table 1. Hungtington's diffusion regimes [15].

Type	Homologous temperature (T_H)	Diffusion mode
A	T_H>0.5	Lattice and grain boundary
B	0.3≤T_H≤0.5	Grain boundary with some trans-boundary diffusion
C	0.3<T_H	Grain boundary only

iii. Effect of microstructure on electromigration

Numerous studies have been carried out to investigate the effect of microstructure on electromigration in Al interconnects and Cu interconnects. However, only few studies focus electromigration in solder joint, such as those using eutectic Pb-Sn solder. The eutectic PbSn solder is a two-phase alloy. The microstructure of the alloy present in the solder joint region depends on the alloy composition and the fabrication of process used to make the solder joints.

a. Alloy composition

According to Liu et. al, [16] at ambient temperature imposition of a current density of 10^5 Amp/cm^2, eutectic Pb-Sn solder can result in very fast failure rate due to electromigration in this alloy composition. It is because this eutectic alloy has the lowest melting point and a highest density of lamella structure. Changing the composition of the alloy by increasing percentage of Sn to produce hyper or hypo condition reduce the failure rate due to electromigration. In other words, the highest density of lamella structure with the highest density of interfacial boundaries results in the highest rate of electromigration behavior. Thus, it is believed that grain boundary diffusion is the main kinetic path of atomic transport in electromigration at ambient temperature. Moreover, as the alloy composition changes, the electromigration rate changes. Starting from pure Sn, the electromigration rate decreases when Pb is added to it; however, it increases as the alloy approaches the eutectic composition. At the eutectic point, solder joint has the highest electromigration rate. Then it decreases again when alloy composition moves towards Pb. Therefore, electromigration rate is strongly dependent on the microstructure of solder joint.

b. Microstructure coarsening during annealing

As the solder joint is isothermally aged, the microstructure of solder joint will be coarsened. According to Jung et al. [17], the eutectic coarsening kinetics for eutectic PbSn solder joints annealed at 50°C to 150°C was determined to be of the form:

$$\bar{D}^n - \overline{D_0}^n = K_o \bullet t \bullet \exp(-Q/RT)$$

where,

$\bar{D}$ is the mean linear intercept phase size, $\overline{D_0}$ is the as-reflowed phase size, $n=4.1\pm0.15$, $Q=39.8\pm0.8$kJ/mole, $K_0=1*10^{-23}$-$4.5*10^{-23}$,t is time, T is temperature, and R is Boltzmann constant.

From the above equation, the phase size is strongly dependent on the time and temperature. In other words, by controlling the temperature and time, the phase size can also be controlled. Microstructural coarsening not only decreases the grain boundary of solder alloy joints, but also reduces the diffusion path available in the solder joint, and slows down the hillock and valley formation.

According to Yang et al. [18], it was found that pre-aging at 170°C was able to increase the electromigration lifetime of flip-chip Sn-Ag solder joints. It was believed that solid-state aging may form thicker intermetallic compound (IMC) layers and this may be able to increase the electromigration resistance.

However, in order to gain a better understanding of electromigration behavior as well as diffusion paths during electromigration, this study was focused on the effect of coarsened microstructure by using our newly designed solder joint to reduce unnecessary

issues, such as thermomigration and evaluate the electromigration behavior without additional complications.

1.4 Solder joint to reduce current crowding and thermomigration issue

In order to study electromigration behavior, there is a need to develop a new design for solder joint. It is because using the currently popular joint configuration it is hard to carry out studies that isolate critical events that occur mainly due to the electromigration. This joint configuration minimized the roles of other issues, such as "current crowding" and thermomigration.

i. Current crowding issue

Current crowding is serious issue in the failure mode of electromigration in flip chip solder joints. As the electron flows in the thin film and approaches the edge of a solder bump, electric current will take lowest resistance path and jam at the entrance into the solder bump, resulting in current crowding. In other words, the electric field, E rotates to accomplish this resulting in current crowding. Especially in the line to bump geometry of a flip-chip solder joint, as the current changes direction from line to bump, there is a very large current density change at the contact. It is because the cross-section of the line on the chip side is two orders of magnitude smaller than that in solder bump. Thus, as the same current passing through them, the current density on the chip will be at least two orders of magnitude lager than that of solder bump [19]. Since the rate of electromigration damage is roughly proportional to the square of the current density, void nucleation will occur at the via edge [1].

According to Tu et al. [20], there are two significant effects due to the current crowding. First, there is an abrupt change in current density before and beyond the point where current turns into the bump. Second, the current density in the solder bump near the entrance point will be about one order magnitude higher than the average current density in the middle of the bump. It will be 10^5 Amp/cm^2 near the entrance when the average current density in the middle of the bump is 10^4 Amp/cm^2.

Thus, it is current crowding or the high current density at the entrance point of electric current that will lead to electromigration, not the average current density in the bulk of the joint. So, it is our intent to investigate if the role of current density in the entire solder joint where the average current density influences the electromigration behavior.

ii. Thermomigration issue

Due to Joule heating, electromigration may cause a non-uniform temperature distribution in a flip chip solder joint. So, there may be a component of thermomigration in any electromigration experiment. In other words, electromigration in a flip chip solder joint is accompanied by thermomigration when a large current density is applied or when the current distribution is non-uniform because of current crowding.

Thermomigration is a mass transport caused by a large temperature gradient. If an initially homogeneous two-component alloy is placed within a temperature gradient, above a critical level, mass diffusion can cause disintegration of the components. Then, the components will move from the hot side to the cold side, and as a result the hot region becomes depleted in that component. This effect is known as the Soret effect in fluids. This resulting diffusion process is known as thermomigration or thermal diffusion [21].

According to Basaran et al.[22], there is a large temperature gradient across nano-electronics and power electronics solder joint, especially Si based devices that operate at high temperature. It is because high current density in power electronic devices leads to thermal gradient due to local Joule heating. These increased current density and temperature gradients are now major reliability concerns, especially for the solder joints of an electronic package.

Ye et al. [23] have shown that when the thermal gradient is large enough the thermomigration can be the dominant migration process, even larger than electromigration. According to Chen et al. [24], a hot spot was found in the vicinity of the entrance point of the Al interconnect, which is detrimental to the electromigration life time of the solder joints. According to Nah et al. [25], this hot spot was the most vulnerable part in the solder joint, since it may experience much larger electron wind force due to the higher current density and the higher diffusivity owing to the higher temperature. Hence, instead of being influenced by electromigration, the formation of voids and the cause of failure in solder joints may result from thermomigration.

iii. New design of solder joint to reduce current crowding issue and thermomigration issue

To understand fundamentals of these complex interaction, and to investigate failure mechanisms during electromigration, there is a need to developed a new design of solder joint to focus on the atomic movement purely due to electromigration. Fortunately, a new design has been developed by our group which will efficiently reduce current crowding and thermomigration during electromigration study. The followings are the advantages of this new design of solder joint. First, the geometry of solder joint is

symmetrical. Thus, the effect of current crowding will be efficiently reduced. Second, although there are still some current crowding region in the solder joint, the extent of current crowding regions can be controlled by appropriate minor modification in dimensions. Third, there is no serious joule heating due to Cu pillars and substrate has an excellent thermal conductivity. As a result, there was no thermal gradient from the cathode to anode of the joint. In other words, this joint configuration will avoid the influence of thermal migration. Last but not least, it is easy to adjust the size and change the alloy composition of the solder joint [26].

By using this joint configuration, several factors will influence the electromigration has already been identified, such as effect of current stressing time, effect of thickness, and effect of direct current (DC) and alternating current (AC).

a. Effect of current stressing time

According to Lee et al.[27], after three days of continuous current stressing with a current density of 10^4 Amp/cm^2 at 150 °C, significant hillock/valley formation while Pb-rich and Sn-rich start to segregate into two-layer morphology in the 25-μm joint. Additionally, prolonging the current stressing for four more days causes this two-layer morphology formation completely.

b. Effect of thickness of solder joint [27]

The time required to achieve the two-layer morphology in the thicker (75-μm) joint is longer than in the thinner (25-μm) joint.

c. Effect of DC and AC

According to Ho et al.[28], if the joint was stressed by DC, electromigration induced damage occurred, such as valley/hillock formation, two-layer segregation of Pb-rich and

Sn-rich domains, and asymmetric growth of Cu-Sn intermetallic layers. On the other hand, no significant electromigration was observed after the AC treatments, especially for the treatment with AC frequency higher than 1 $hour^{-1}$. The dependence of the damage on AC frequency suggests that electromigration in solder joints can be inhibited to a large extent when a proper reverse current is delivered.

1.5 Analysis method

There are numerous analysis methods used to investigate electromigration behavior. For example, Scanning Electron Microscopy (SEM), Optical Microscopy (OM), Transmission Electron Microscopy (TEM) [30], Energy Dispersive X-ray spectroscopy (EDX) [31] have already been widely used to evaluate the microstructure evolution of solder joint, and to analyze the composition at various locations in the solder joints.

However, few studies were focused on quantitatively analyzing the result. One of the currently popular ways to further discuss the electromigration behavior is to calculate the effective charge number Z*. According to Huntington et al.,[20] the drift velocity is taken as

$$V_d \equiv D/KT \bullet Z^* \bullet q \bullet j \bullet \rho \quad ,$$

where

V_d is drift velocity, D is diffusivity, Z* is effective charge number, T is temperature, q is the charge of an electron, j is current density, and ρ is resistivity

This indicates that if considers the self-electromigration of the noble metal and measure the drift velocity, knowing the diffusivity, D, the effective charge number can be calculated.

However, for a two-phase alloy, one must first have a detailed study of the microstructure before studying its electromigration. Without knowing the diffusion species and paths in the microstructure, the calculation of effective charge number is not necessarily accurate. [30]

Thus, instead of calculating the effective charge number, a systematic method should be developed to characterize the result. In this study, due to the large contrast for the Pb-rich and Sn-rich regions for the eutectic Pb-Sn solder joints under optical microscope (OM), it is easy to distinguish these two regions. In this way, by investigating the microstructure change of Pb-rich and Sn-rich regions after electromigration, the diffusion paths and diffusion species can be inferred.

1.6 Motivation

i. Grain coarsening

Grain coarsening effects plays an important role in electromigration related phenomenon. Isothermally aged sample joint will result in the change in the grain size of solder joint. So, by isothermally aging the solder joints to different extents of time, one can control the size of the grain as well as control the electromigration rate.

Besides, grain size is an important factor for mass diffusion rate. The smaller the grain size is, the faster the diffusion is. It is because the net contribution of lattice and grain boundary diffusion is the active electromigration paths for eutectic solder joint. As the grain size changes, the effect of grain boundary diffusion on electromigration can be evaluated.

ii. Diffusion mode and diffusion of atomic species at 100°C and 150°C

Diffusion mode and diffusion species under electromigration at 100°C and 150°C are still unclear. It is generally believed that the mode of diffusion path at 100°C is lattice diffusion and at 150°C is through grain boundary. If this saying is true, as we change the size of grain boundary, the electromigration phenomenon should remain the same at 100°C and change at 150°C. So, we can operate at two different temperatures and compare the result of changing the different coarsened structure to see the effect of coarsened microstructure on electromigration behavior.

Besides, the temperature of 100°C and 150°C are both very critical temperatures for electronic industry. It is because the working temperature of Si devices is around 100°C and an aging at 150°C for 1000 hour is a required test in reliability specification [15]. So, if one operates experiment at these two temperatures, the behavior of the solder joint at these two temperatures can be further discussed.

iii. Aging study

In order to compare different extent of the coarsened microstructure, how many isothermally aging days is also very important to decide the size of grain area. At lower temperature (100°C), the coarsening time should be longer than at higher temperature (150°C) to reach the same size of grain area. So, it is also interesting to investigate the growth of grain size for the different coarsening time at different temperature.

1.7 Aim of this study

Following were the objective of this study:

a. To develop a consistent method to fabricate new design of solder joint, that has less current crowding and thermomigration issues.
b. To gain a better understanding of material movement on electromigration behavior by isothermally aging the eutectic Pb-Sn solder joint to achieve different extents of coarsened microstructure prior to current stressing.
c. To evaluate the diffusion mode and species at 100°C and 150°C by comparing the results of different coarsened microstructure subjected to current stressing for the same length of time.
d. To understand the effect of coarsened microstructure on electromigration behavior of eutectic Pb-Sn solder joint.
e. To conduct systematic analysis to characterize the average grain area of Pb-rich phase and the concentration of Pb-rich domains to evaluate the accumulation Pb-rich layer, and to analyze the area distribution of Pb-rich domains.

2. EXPERIMENTAL PROCEDURE

2.1 General

In order to study electromigration behavior, there is a need to develop a new design of solder joint. It is because using the currently popular joint configuration is difficult to clearly characterize the electromigration behavior without interference from other influences. The currently used joint configuration is always involved with other issues, such as "current crowding" and the thermomigration. Due to the thin-thick divergence, this configuration exists a region where local density can vary by two or more orders of magnitude over a very short distance [32, 33, 34]. Additionally, this "current crowding" region will cause a significant local Joule heating and result in the local temperature differences [35, 36]. This temperature difference between the chip side and the board side will cause visible thermomigration from chip side to the board side. As the result, the influence of thermomigration cannot be ignored.

Therefore, in order to minimize the current crowding, as well as the local Joule heating, the current path in this joint needs to be straight. Moreover, in order to eliminate the thermomigration issue, the heat generated in the solder joint should be dissipated as soon as possible. Based on these two concepts, a new design of solder joint has been developed and is shown in Figure 1. Instead of using the thin-thick divergence configuration, the geometry of the joint in this new design is symmetrical and straight to reduce "current crowding." Also, the joint should be made by lots of copper to facilitate good heat conductivity. Thus, the heat generated will be dissipated easily.

According to the results by Ho et al. [37], more than 80 volume percent of solder in this new design of joint has current densities in-between a range of 15% of targeted

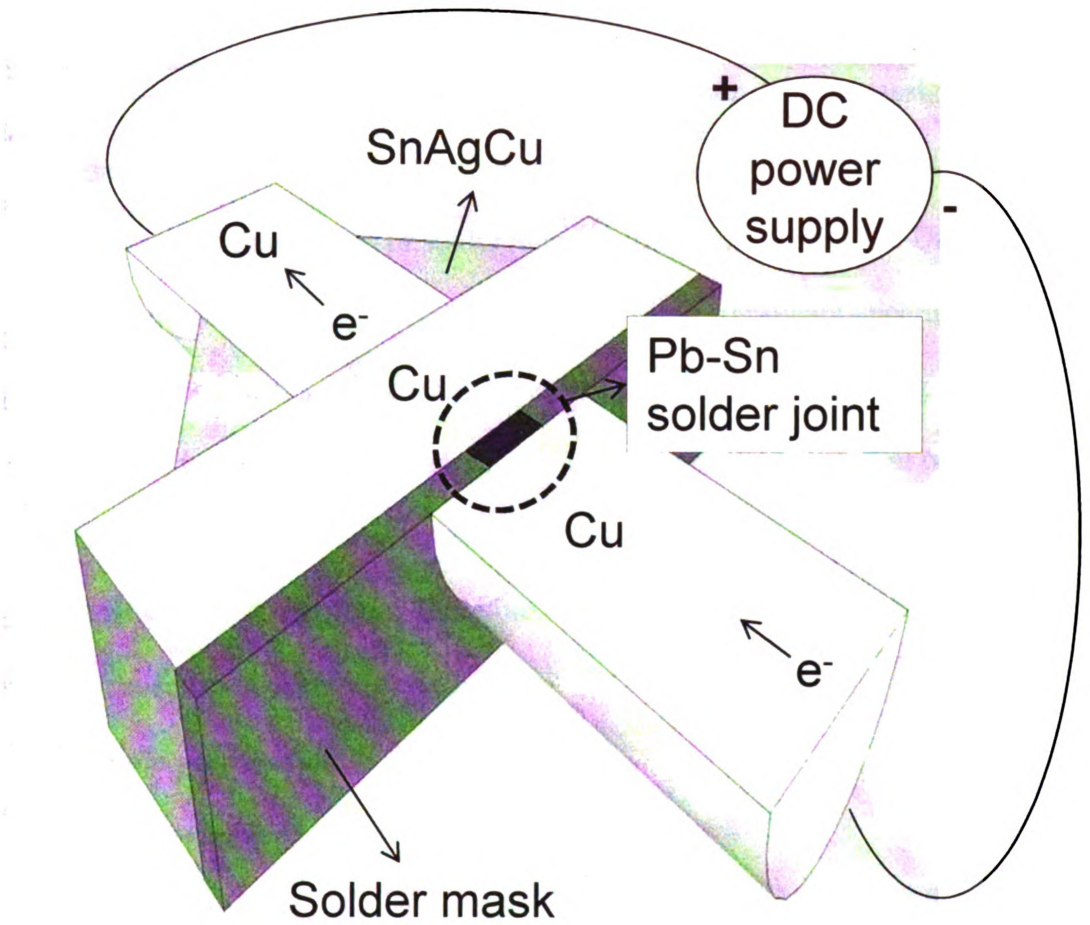


Figure 1. Schematics drawing showing the solder joint configuration used in this study

Note: e^- indicates direction of current stressing

value. During the 5.9 Amps current stressing, the temperature in the solder joint is only raised to about 2.5 (±2)°C above ambient environment temperature over a range of 30-150°C.Unlike in circuit of solder bump flip-chip joints, no serious heat generation occurs in the solder present in this new design of joint configuration. This suggests that there was no significant thermal gradient during current stressing.

However, this new design of solder joint was not easily fabricated. During the process of fabrication, any slight movement will result in significant uncertainty in the solder joint, such as cracks or uneven thickness of the solder joint. As long as there are cracks in the solder joint, these will significantly influence the events that occur during current stressing. Moreover, uneven thickness of solder joint will result in different current density in the solder joint. Therefore, the method of fabricating this new design of solder joint needs to be carefully controlled.

2.2 Sample preparation

i. Material used in this study

a) Solder ball

The solder ball used in this study was eutectic 63Sn37Pb prepared by Kinsus.

b) Solder mask

The solder mask used for mounting in this study was prepared by mixing the heat hardening solder mask and the hardener with a weight percentage of 9:1 respectively.

c) Cu pillar

The Cu pillar is 1.2 mm diameter and the tips of Cu pillars were metallographically polished before soldering.

d) Cu substrate package

The Cu substrate package included a 1200 μm diameter Cu pillar, a 500 μm thickness Cu pad, and a 70 μm thickness solder mask. As shown in Figure 2a, a solder mask with an opening of 460 μm was attached on the topside of Cu pad, and a Cu pillar was soldered on the backside to Cu pad by using eutectic SnAgCu paste in order to conduct the electric current. The use of eutectic SnAgCu assured that backside of this package will not fall off in the soldering process due to its higher melting point of 217°C.

e) Solder paste

A surface that is oily or oxidized will prevent the solder from spreading during soldering. This soldering paste with brand named Taiyo Soldering Accessory was used to remove such oil or oxides and to improve wettability while soldering.

ii. Equipment used in this study

a. Equipment for alignment

In order to recreate the new design proposed by Ho et al. [37], the equipment set-up for alignment shown in Figure 3 was used. The Jack was used for controlling the z-axis movement impositions between the inserting Cu pillar and the Cu substrate package. X-Y axis controller was used for aligning the inserting Cu pillar with the solder ball on the Cu substrate package. In addition, an aluminum stage with a 1.28 mm-diameter hole was connected on the X-Y axis controller to ensure vertical alignment. In order to heat up this aluminum stage as well as Cu pillar while soldering, a heat belt was surrounded on the aluminum stage.

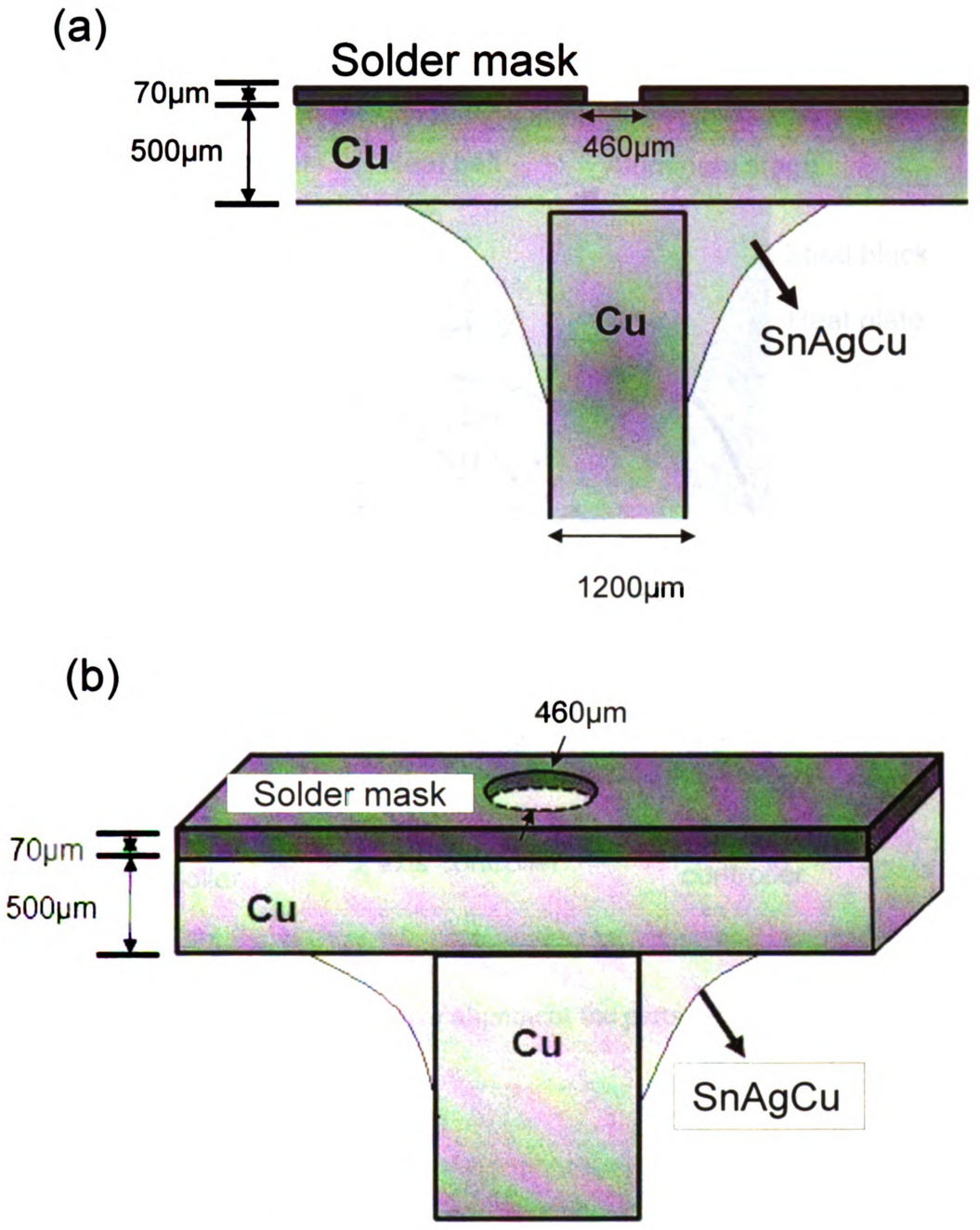


Figure 2. Schematics drawing showing the Cu substrate package (a) side view and (b) top view.

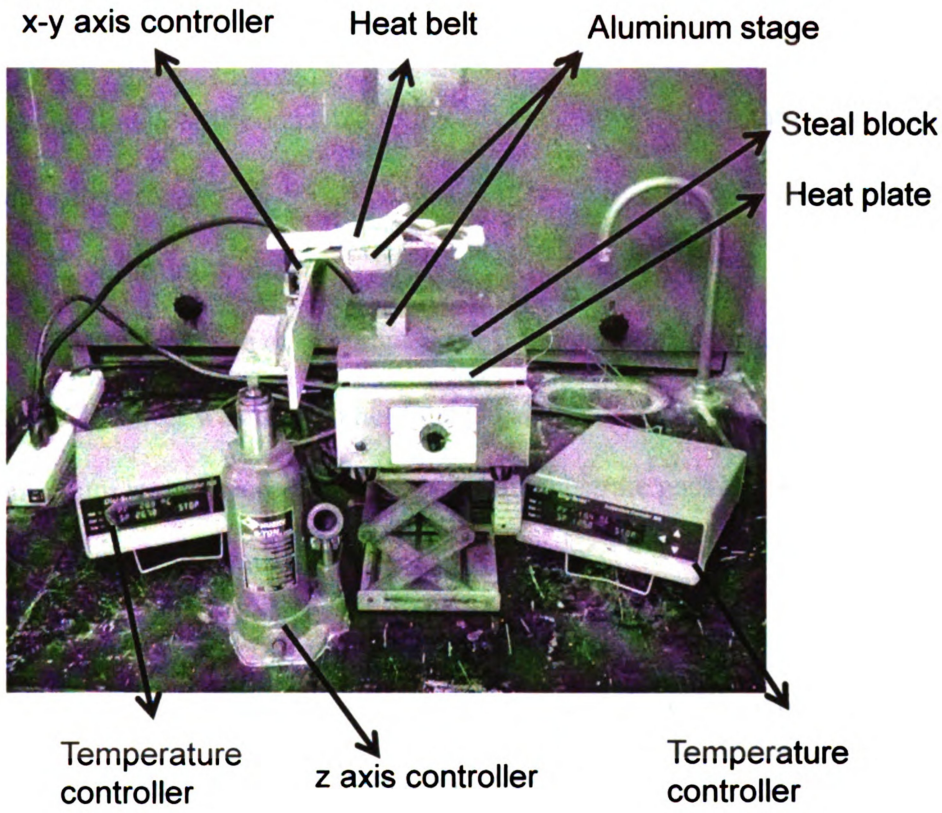


Figure 3. Equipment used for alignment the parts for the soldering operation.

b. Heat plate

A steal block was placed on the heat plate to ensure constant temperature during sample fabrication.

c. Temperature controller

Two parts were needed to maintain the temperature that was controlling by a temperature controller. One is connected to the aluminum stage on the equipment for alignment and the other is connected to the hot plate. The temperature was maintained at 220°C while soldering.

d. Aluminum stage

For the purpose of placing Cu substrate package, an aluminum stage with a hole of 1 cm-diameter was used to hold the Cu substrate package while soldering. The use of aluminum stage assured that the entire Cu substrate package was heated to 190°C while the hot plate temperature was controlled at 220°C

e. Power supplier

For current stressing, a well regulated constant voltage/ constant current supply with brand named Model 1796 high current regulated D.C. power supply was used. It delivered 0-16 V at 0-50 Amps and could be adjusted continuously throughout the output range.

iii. Joining Protocol

Schematics are provided in Figure 4 to illustrate the details corresponding to the steps described in the following methods.

Prior to the soldering, Cu pillars were cleaned by nitric acid solution (30%) and water, and then fluxed. First, the cleaned and fluxed Cu pillar was placed into the

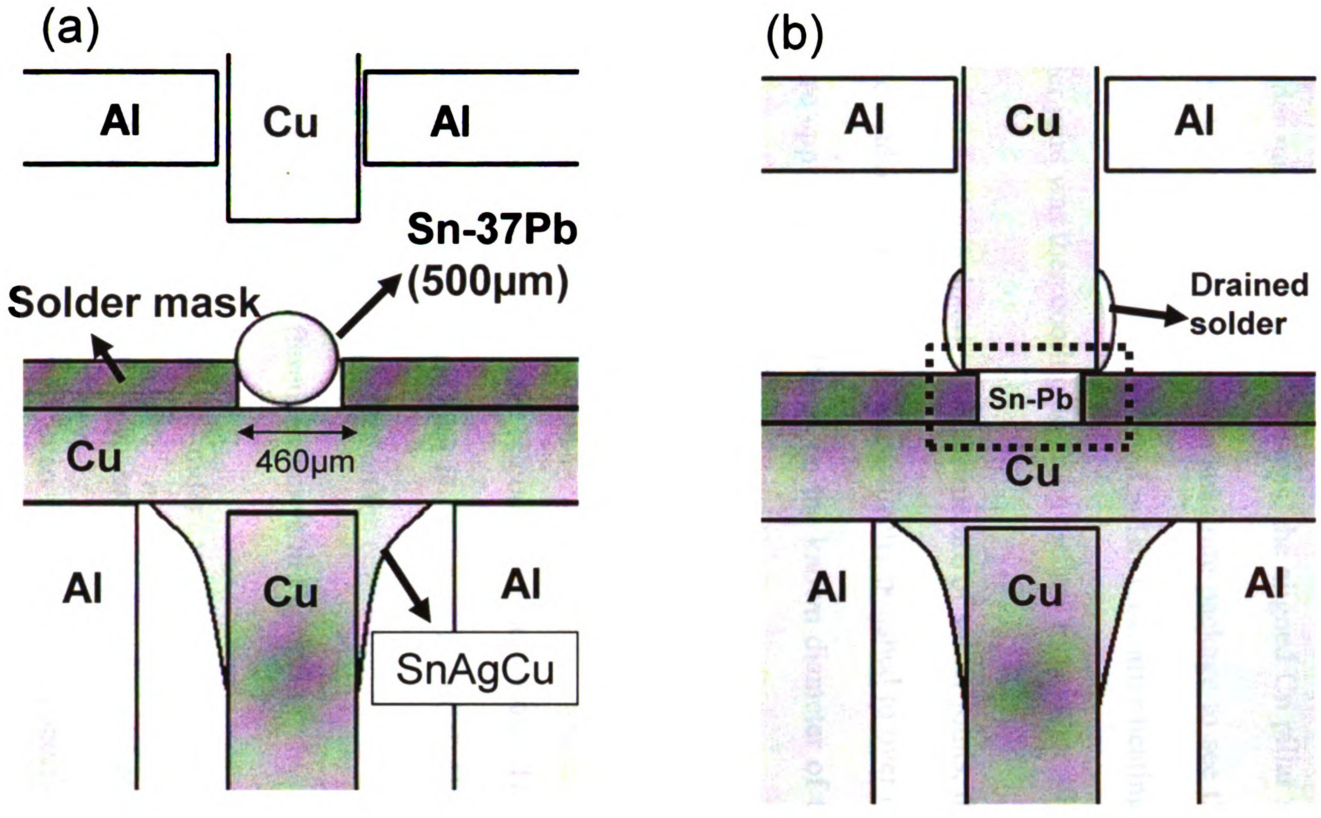


Figure 4. Schematics drawing showing the fabrication of the solder joint. Before soldering (a), and after soldering (b).

equipment for alignment heated up to 220 (±5)°C, and then aligned with the opening of solder mask. Second, Cu substrate package was then placed on the aluminum stage heated to 220 (±5)°C. At this temperature, a fluxed solder ball was then placed in the opening of solder mask. After these two steps, the aligned Cu pillar shown in Figure 4a was then inserted and squeezed to the Cu substrate package to see the excessive solder drained from the pad and wetted the inserted pillar. Last, after heating for 40 sec, the as-reflowed solder joint was then cooling down by airflow for another 40 sec.

In order to investigate interior microstructure of solder joints, the joints were heat-mounted in the solder mask and metallographically polished to over one-half of the joint diameter before applying current. Based on the known diameter of the solder joint, the current stressing area was calculated. In other words, current density was able to calculate by dividing the current passing through the joints by the contact area of current stressing. Figure 5 shows the overview of the polished solder joint used in this study. The dot line in the middle region indicated the region of observation. The image of initial microstructure of as-reflowed solder joint is shown in Figure 6. However, if the solder joint was cooling down by spraying water on the connection of Cu pillar and Cu substrate package, the microstructure is different as shown in Figure 7

Prior to current stressing, in order to observe the effect of coarsened microstructure during current stressing, solder joints were isothermally aged in a temperature-controlled, convection air oven for a required condition to cause different extents of coarsened microstructure.

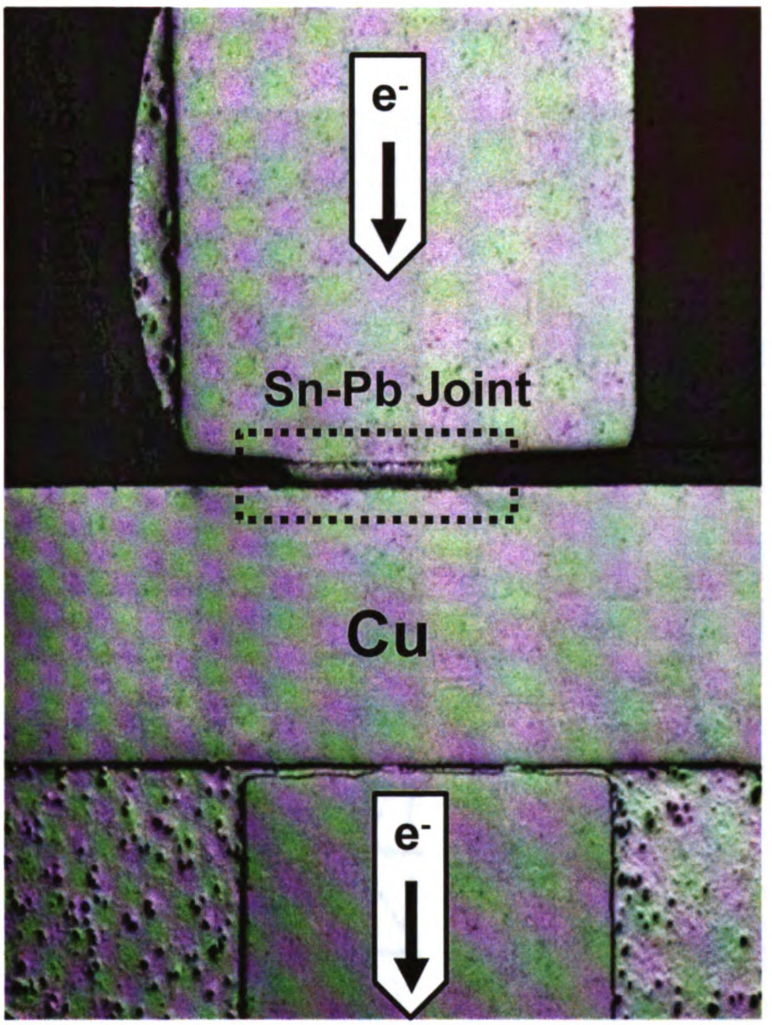


Figure 5. The overview of the joint used in this study.

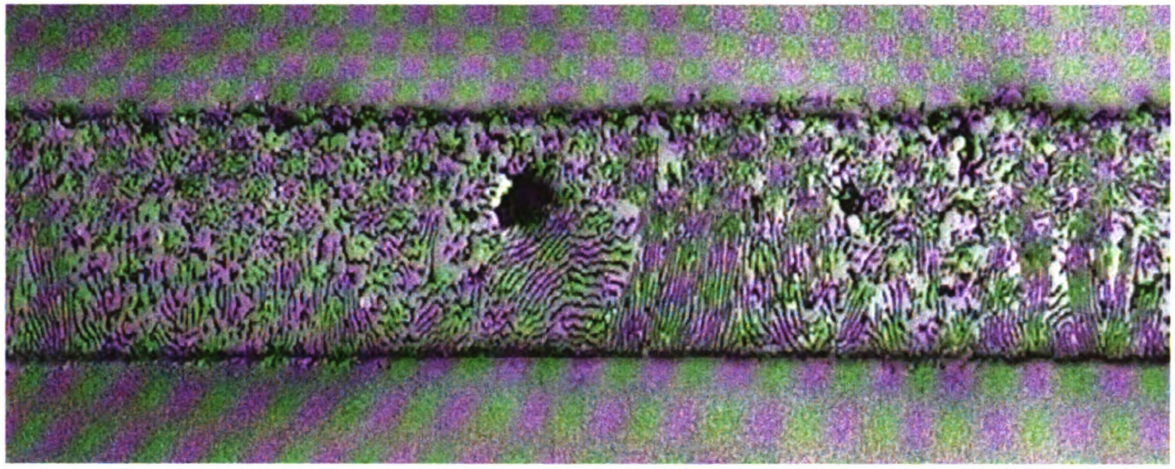


Figure 6. The microstructure of as-reflowed solder joint cooled by airflow.

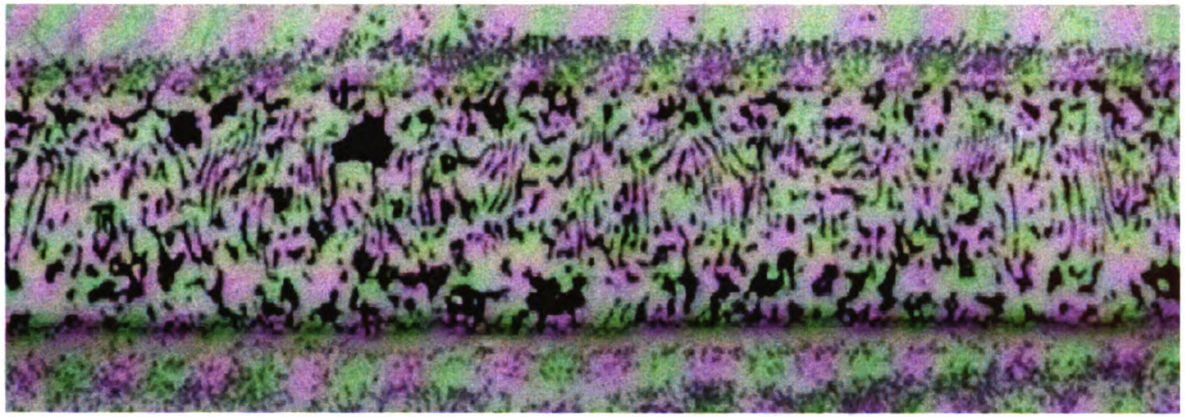


Figure 7. The microstructure of as-reflowed solder joint cooled by water.

These isothermally aged solder joints were then subjected to current stressing for a required time by placing them into a temperature-controlled, convection air oven set at a required temperature. The details of all required experimental conditions will be described in the next section. For current stressing, a constant electrical current of 4.9 Amps was passed through the solder joints, which generated a global average current density of 10^4 Amps/cm^2 within the solder joint.

After current stressing for a known period of time, surface features of solder joints were observed by using optical microscopy (OM) and a JEOL 6400 scanning electron microscopy (SEM) operated at 20 keV. In order to characterize the image, image analysis software *ImageJ* was used to automatically identify the phase region boundary, and measure phase area and average diameter. By setting the threshold in *ImageJ*, the Pb-rich region boundary could be detected, and the average area could be measured. The Pb-rich phase region is outlined by the software as shown in Figure 8.

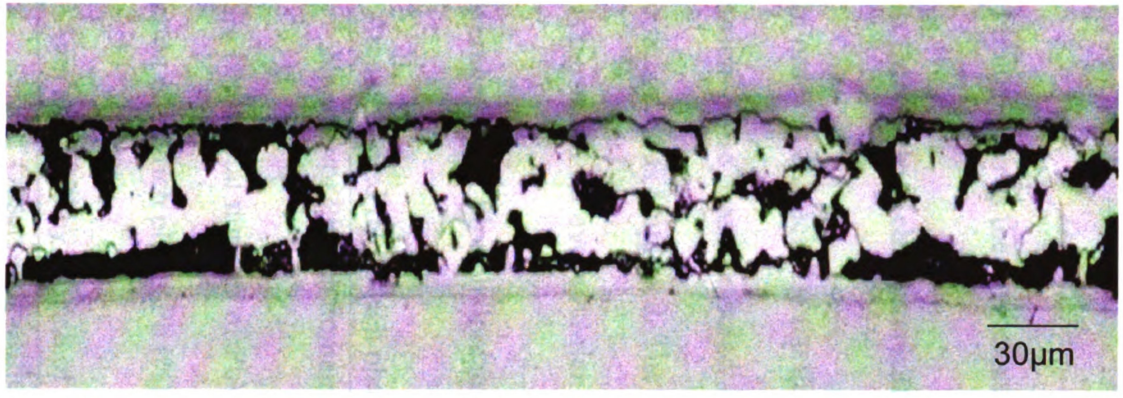
2.3 Date collection and data analysis

i. Experimental protocol

Basically, this experiment was performed at two temperatures, 100°C and 150°C.

At 100°C, the solder joints were isothermally aged for 12 days and 15 days. Then, these isothermally aged solder joints were subjected to current stressing for 20 days at 100°C; and compared to those noted in as-reflowed solder joints subjected to current stressing at 100°C.

(a)



(b)

Figure 8. Pb-rich phases in (a) is outlined by *ImageJ* shown in (b).

At 150°C, the solder joints were isothermally aged for 3 days and 6 days. Then, these isothermally aged solder joints were subjected to current stressing for 6 days at 150°C; and compared to those noted in as-reflowed solder joints subjected to current stressing at 150°C.

Figure 9 shows the flow chart of experimental protocol.

ii. Methods of characterization

In order to characterize the distribution of this two-phase structure, grain area for each Pb-rich phase was measured in this experiment since digital image processing software *ImageJ* was employed. The area of individual Pb-rich domain, A_i, on the solder surface is measured for every Pb-rich phase region.

The average size of Pb-rich domain, $\langle A_{Pb} \rangle$, was determined by:

$$\langle A_{Pb} \rangle = \frac{\text{Area occupied by Pb-rich phases}}{\text{Number of Pb-rich domain}} = \frac{\sum_{i=1}^{N} A_i}{N_{Pb}}$$

where N_{Pb} is the total number of Pb-rich domain within the chosen area of interest. The area fraction of Pb-rich phase, Pb (%), is determined by:

$$\text{Pb}(\%) = \frac{\text{Area occupied by Pb-rich of the specific layer}}{\text{Observed specific layer}} \text{X } 100(\%)$$

For the purpose of comparing the size distribution of Pb-rich phase, the segregation of Pb-rich phase and Sn-rich phase, and the accumulation of Pb-rich layer, three types of analyzed were developed to characterize these solder joints.

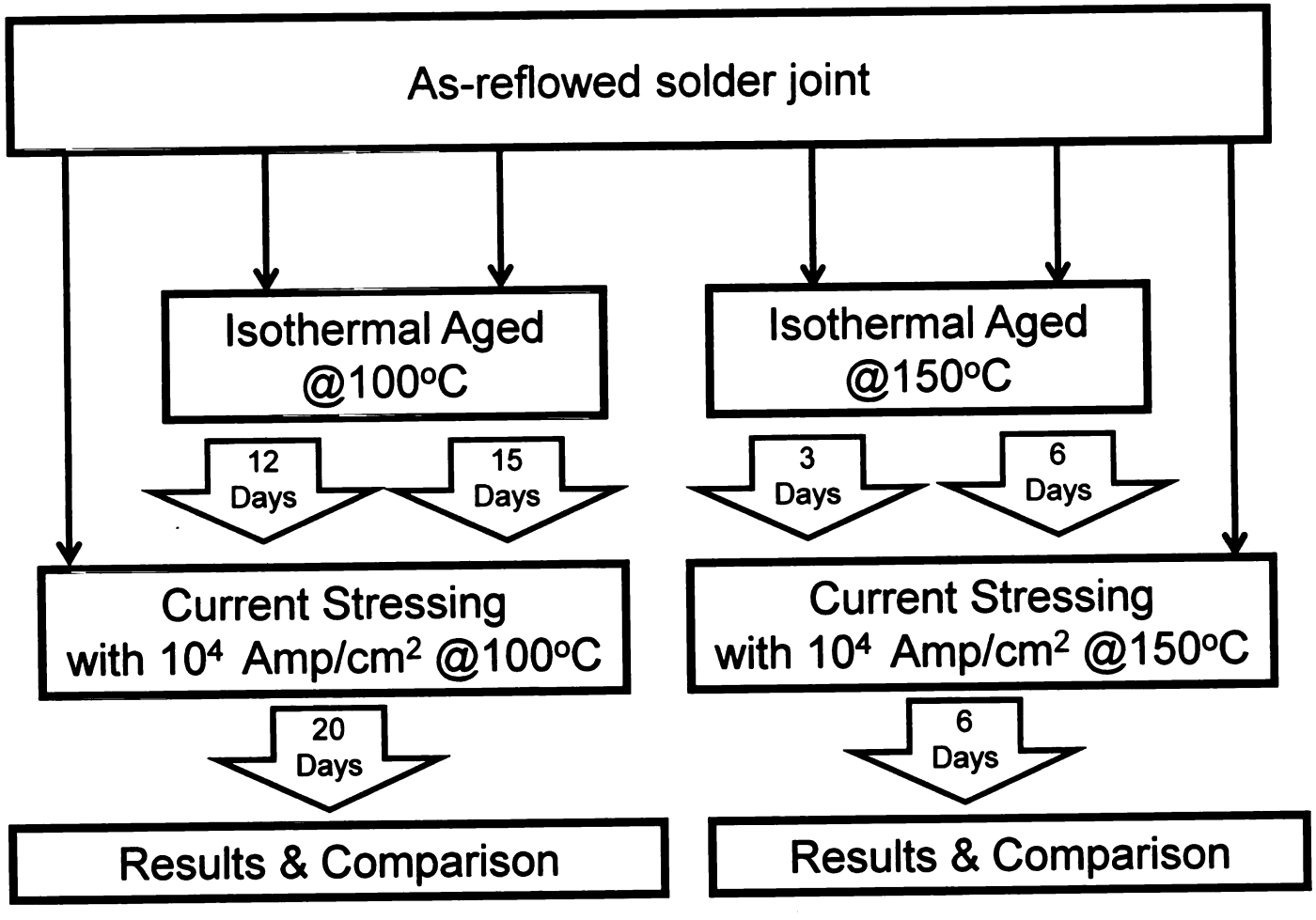


Figure 9. Flow-chart of experimental protocol.

a. Size distribution of Pb-rich phase within solder joint

As shown in Figure10, an area of constant width (350 μm) and length (30μm) within solder joint are chosen on the solder image. By plotting the size distribution of Pb-rich phase, not only mean size of Pb-rich phases but also standard deviation for the size distribution could be evaluated. In this way, the average size of Pb-rich phases resulting from different experimental condition could be compared. In addition to compare the mean size of Pb-rich phase, uniformity of the area distribution of Pb-rich phase could be evaluated by comparing the standard deviation of size distribution of Pb-rich phase within solder joint.

b. Area fraction of Pb-rich phase

a) Between two Cu substrate

In order to evaluate the distribution of Pb-rich area toward anode and cathode, a constant width of 220 μm in the center of solder joint was chosen. As shown in Figure 11, we increase the length from 1 to 35 μm towards anode and cathode. In this way, a layer by layer analysis of area fraction of Pb-rich domain from the cathode to anode can be plotted.

b) Anode accumulation

Since the accumulation of Pb-rich layer was not flat, the value of the thickness of Pb-rich accumulation layer was difficult to measure. As shown in Figure 12, in order to focus on the accumulation of Pb-rich phase as well as the thickness of Pb-rich accumulation, an enlarged image was used as shown in Fig. 8b. Besides, in order to see the change in the fraction of Pb-rich phase while increasing the distance away from anode, we fix a constant baseline with width of 120 μm and change the length of chosen area

from 1 to 30 μm. Comparing the fraction of Pb-rich phase from each chosen region and drawing the chart of Pb-rich phase fraction vs. the distance away from the cathode, the area fraction of Pb-rich phase near anode will be discussed.

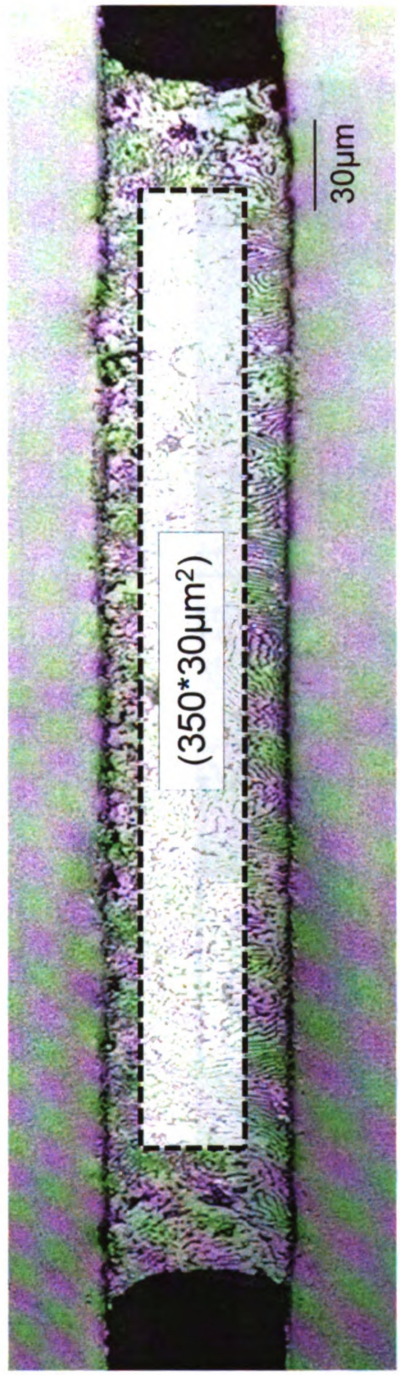


Figure 10. Observed area of the solder joint for size distribution of Pb-rich phase.

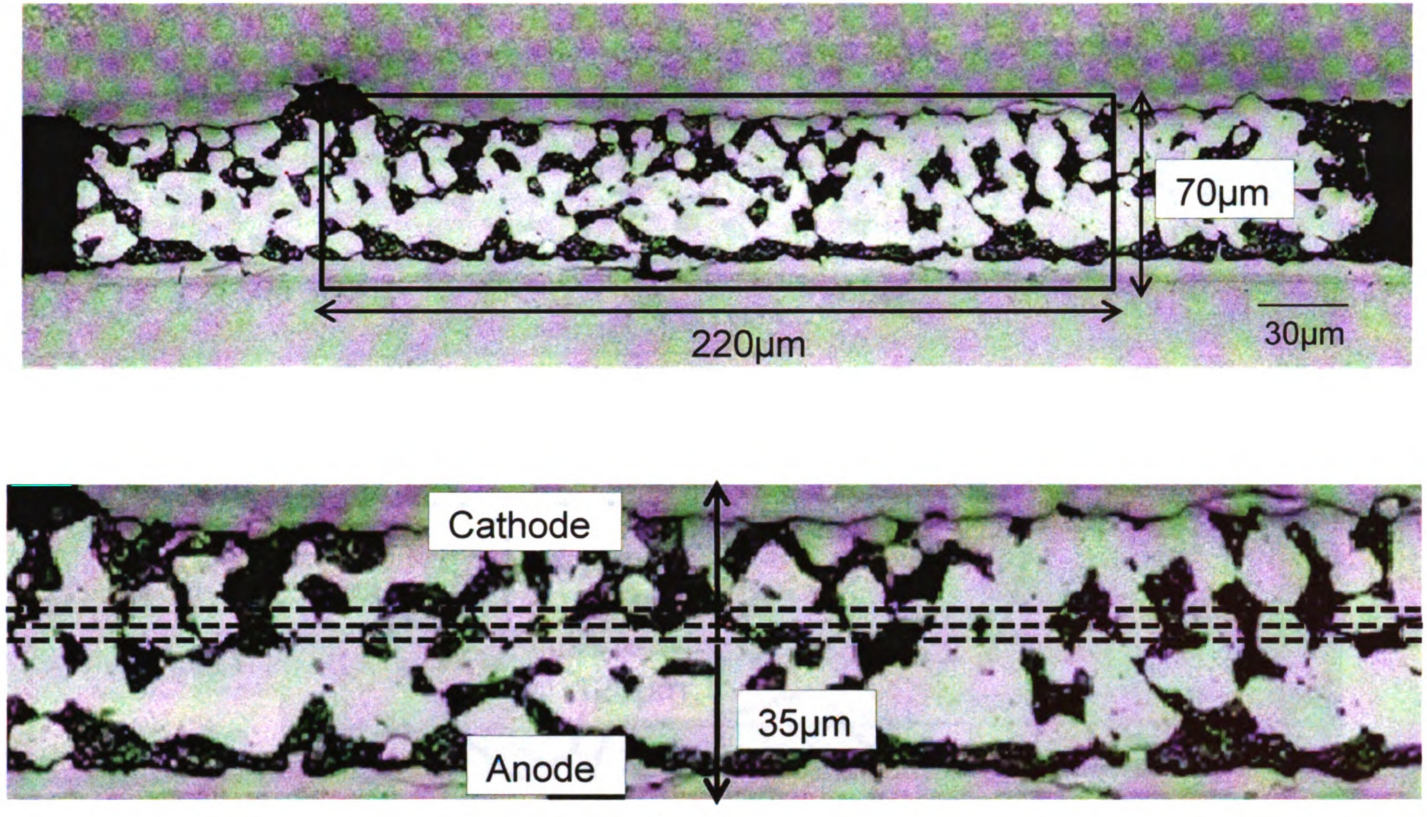


Figure 11. Area fraction of Pb-rich phase analysis. Joint coarsened for 3 days and subjected to current stressing for 6 days at 150°C (a) Observed area. (b) Enlarged picture of observed area. Fix the center line with width of 220 μm and increase the length of chosen area from 1 to 35 μm towards anode and cathode. Comparing the fraction of Pb-rich phase from each chosen region layer by layer, a chart for the fraction of Pb-rich phase vs. distance away from the cathode could be drown .

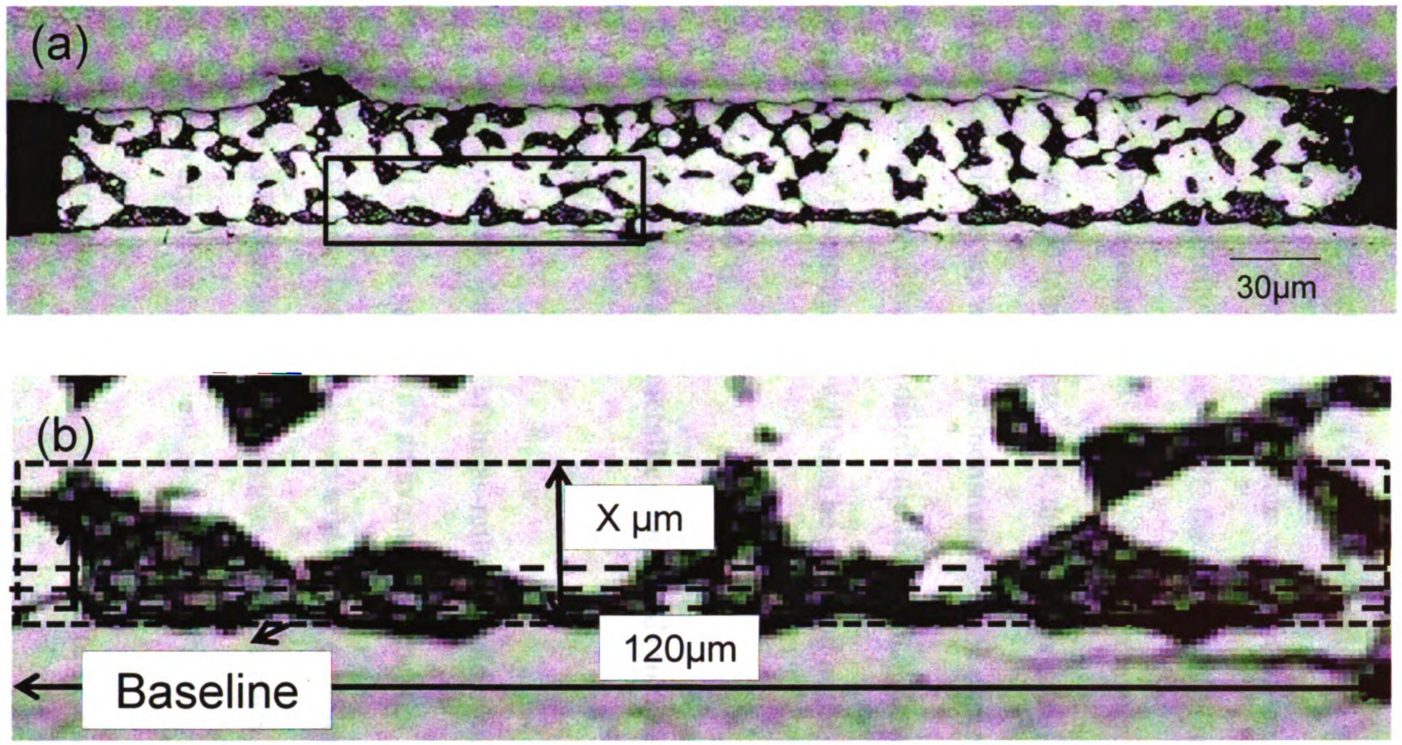


Figure 12 . Area fraction of Pb-rich phase analysis near anode. Joint coarsened for 3 days and subjected to current stressing for 6 days at 150°C (a) Image collected by objected lenses 20 X of observed area. (b) Image collected by objected lenses 50X of observed area. Fix the baseline with width of 120 μm and increase the length of chosen area from 1 to 30 μm, marked by X. Comparing the fraction of Pb-rich phase from each chosen region, we a chart for the fraction of Pb-rich phase vs. distance away from cathode could be drown.

3. RESULTS AND DISCUSSIONS

3.1. Aging studying

In this section, the results for 4 different as-reflowed solder joints that experienced different experimental conditions will be reported. Among these 4 solder joints, two were isothermally aged at 100°C for 12 and 15 days, respectively; the other two were isothermally aged at 150°C for 3 and 6 days, respectively. The structure of the chapter will be organized into 3 parts: first, the clear images of optical micrograph and the thickness of IMC layers will be demonstrate for each experimental conditions; followed by an analysis of the size distribution of Pb-rich phase within solder region; and alternate analysis of Pb-rich phase will also be provided in the last part of the chapter.

i. Aging at 100°C

a. Thickness of intermetallic compounds for solder/Cu substrate interface

Microstructural features of the as-reflowed solder joint are shown in Figure 1. A scallop-shaped of Cu_6Sn_5 layer with an average thickness of about 1 μm at both sides is presented in this figure. The as-reflowed solder joint exhibits the classic interlamellar eutectic structure of Pb-rich and Sn-rich phases that are clearly visible as dark and white domains, respectively, in this optical micrograph.

Optical micrographs of the joints coarsened for 12 and 15 days at 100°C are shown in Figure 2 and Figure 3, respectively. Morphologies of Pb-rich and Sn-rich regions in these micrographs indicate that both phases coarsen from isothermal aging.

Despite the extent of aging, the observation provided in Figure 2 and 3 show that the Cu-Sn interface IMC layers at both sides in both joints (coarsened for 12 and 15 days) are about 2 μm.

b. Size distribution of Pb-rich phase within the solder joint

For the purpose of comparing results of joints that experienced for different isothermal aging conditions, the best way is to compare the size distribution of Pb-rich phase. The size distribution of Pb-rich phases show not only the area distribution of Pb-rich phases, but also the mean size of Pb-rich phase and standard deviation of these Pb-rich phases. The size distribution of Pb-rich domain in intermediate region of solder joint calculated by image analysis software *ImageJ* is shown in Figure 4. The results showed that when the solder joint is isothermally aged for longer periods of time, the average size of Pb-rich domain increased. In addition, for Pb-rich phases smaller than 2 μm^2, their normalized count of Pb-rich phase was obviously decreased after solder joints was isothermal aged, indicating that some individual Pb-rich phase region was coarsened, not the exchange of smaller ones.

c. Area fraction of Pb-rich phases between the two Cu substrate

In order to observe the area fraction of Pb-rich phases during isothermal aging, a layer-by layer analysis from one end of the interface to the other end was carried out. Observation of Pb-rich phase occupied in each selected region (220*2 μm^2) layer by layer away from the interface is shown in Figure 5a and 5b. As the plot indicates, the area fraction of Pb-rich phase for joints isothermally aged 12 and 15 days are similar. The

percentage of each Pb-rich area was held constant around 30% except at the end regions of joints. In other words, isothermally aging samples in general does not change the area fraction of Pb-rich phase in a given region of the joint.

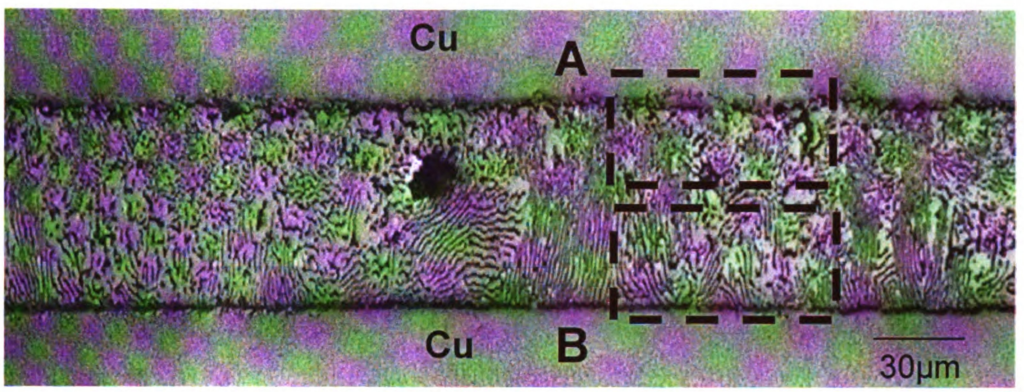


Figure 13a. The image of as-reflowed solder joint microstructure. The enlarged picture of regions A and region B are shown in Figure 1b.

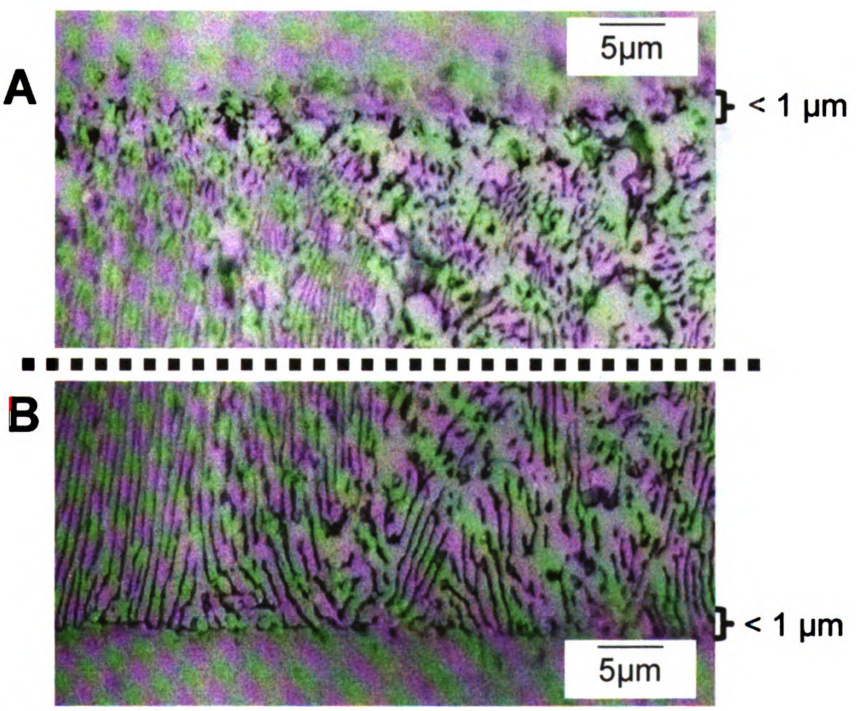


Figure 13b. In regions A and B, IMC layer are both less than 1μm thick.

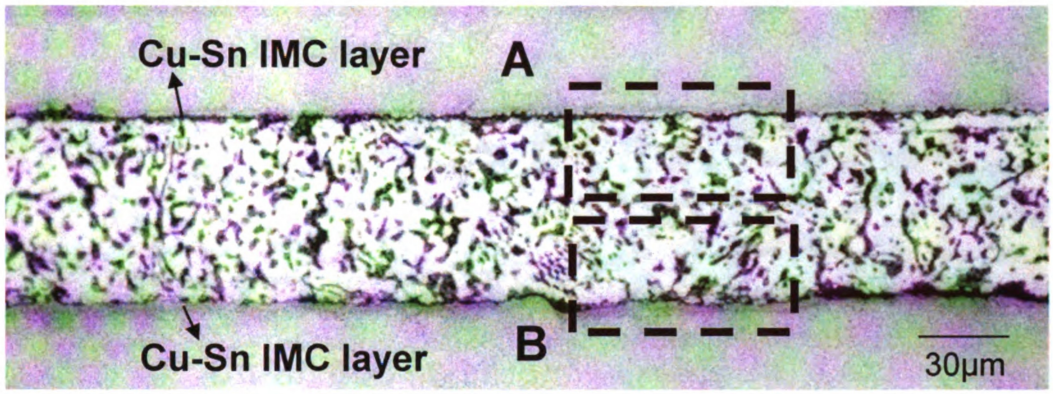


Figure 14a. The image of solder joint isothermally aged at 100 °C for 12 days. The enlarged picture of regions A and region B are shown in Figure 2b.

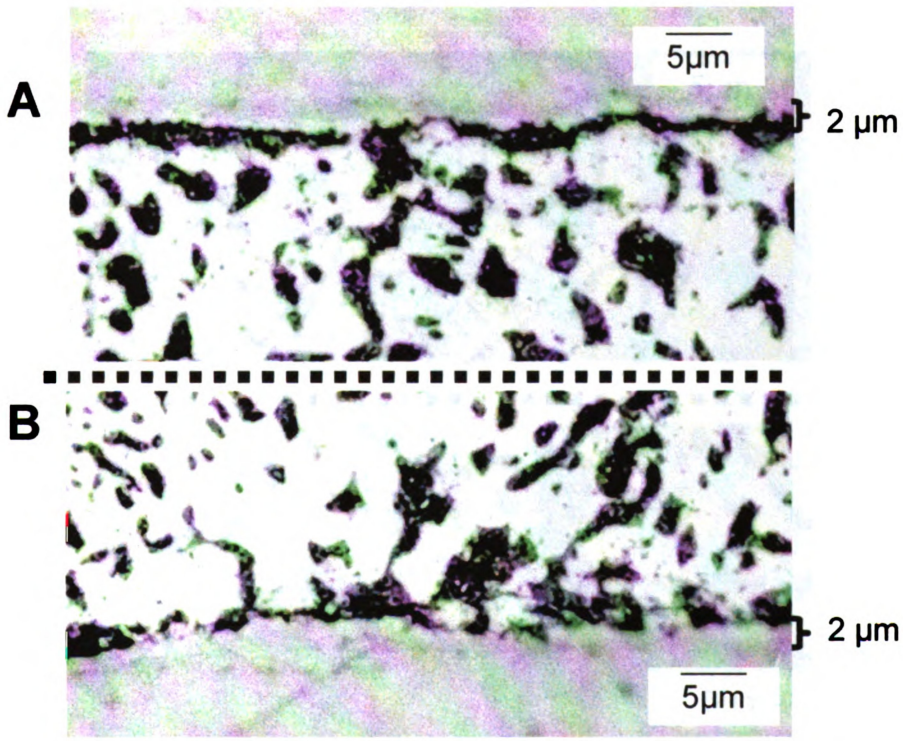


Figure 14b. In region A and B, IMC layer in both ends about 2 μm thick.

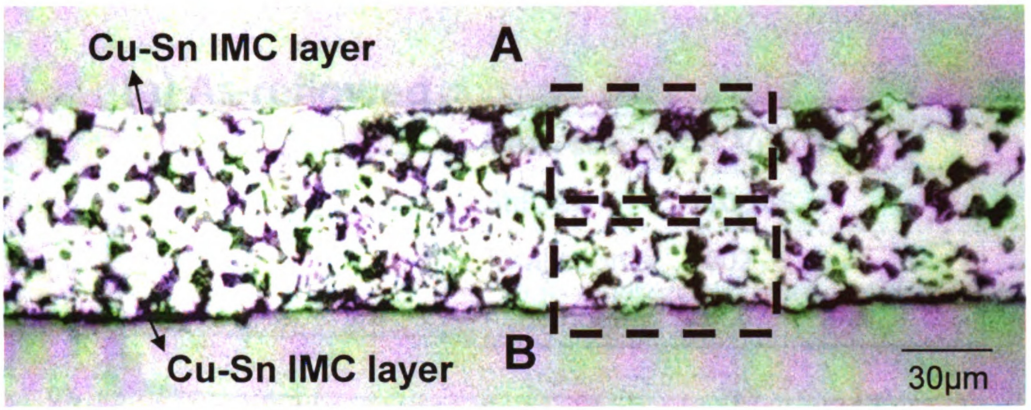


Figure 15a. The image of solder joint isothermally aged at 100 °C for 15 days. The enlarged picture of region A and B are shown in Figure 3b.

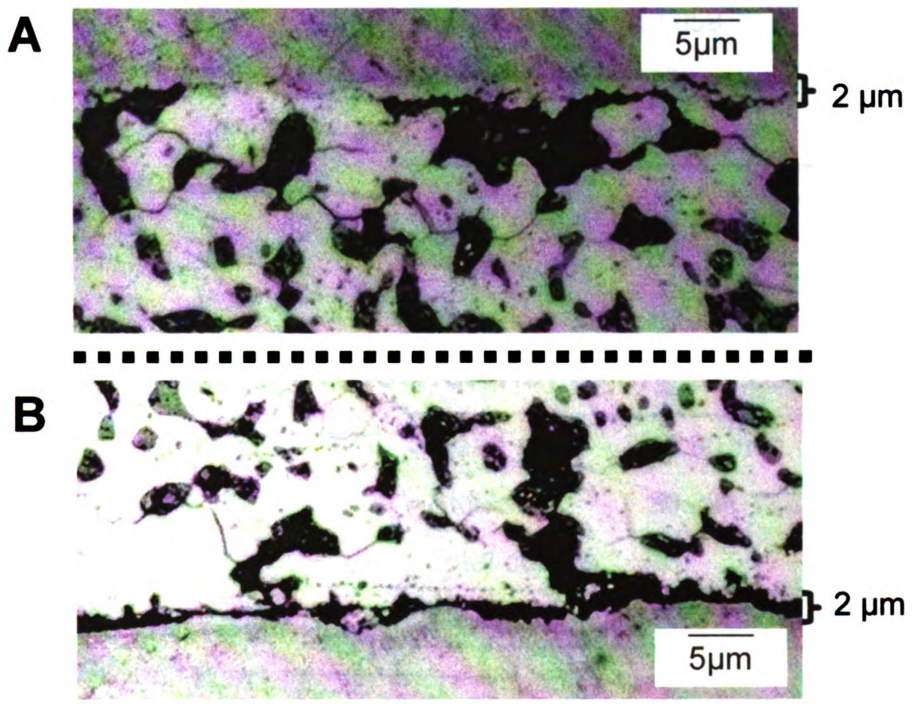


Figure 15b. In regions A and B, IMC layer in both ends about 2 μm thick.

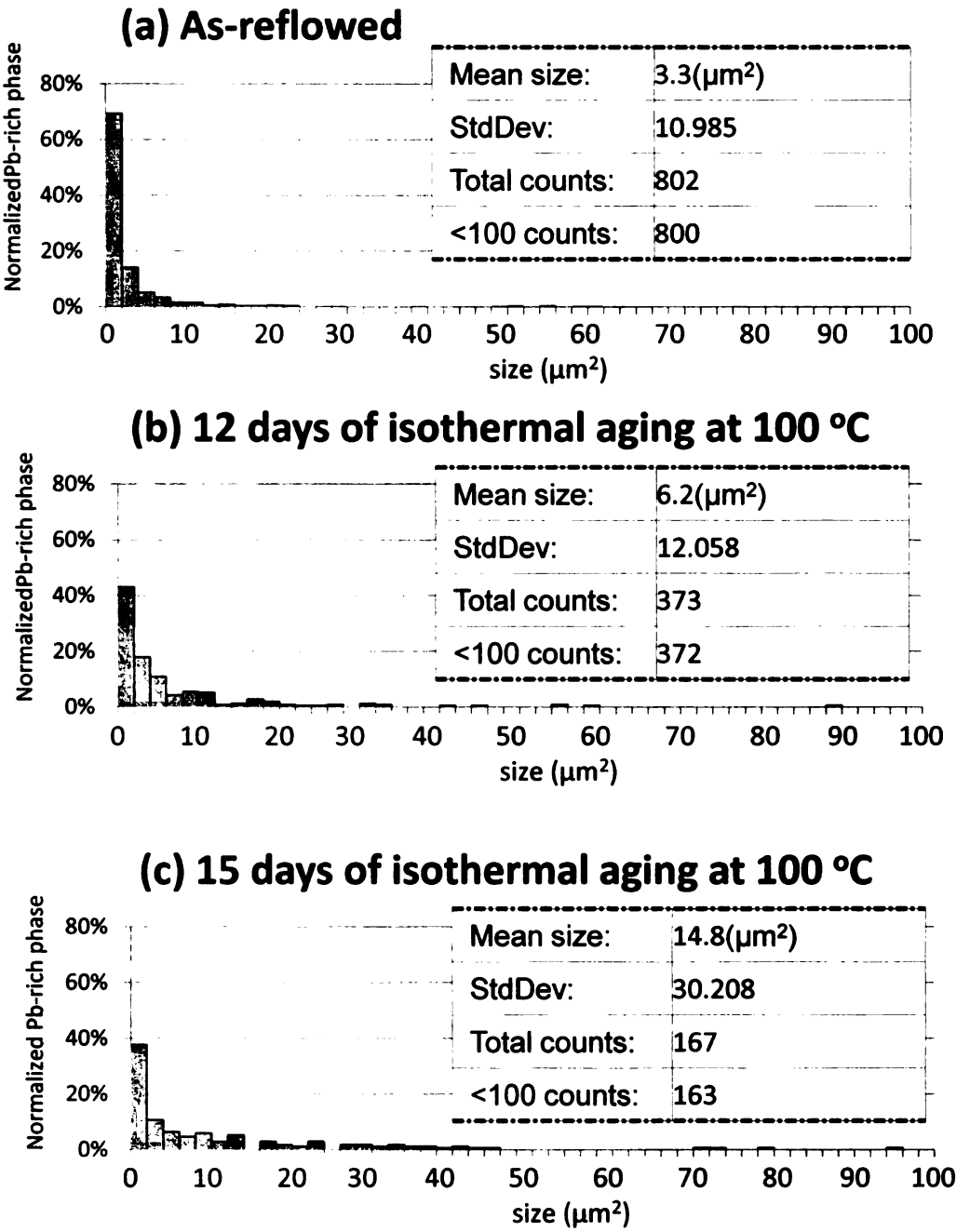


Figure 16. Size distribution of Pb-rich phase within solder joints (a) as-reflowed (b) 12 days of isothermal aging at 100 °C (c) 15 days of isothermal aging at 100 °C.

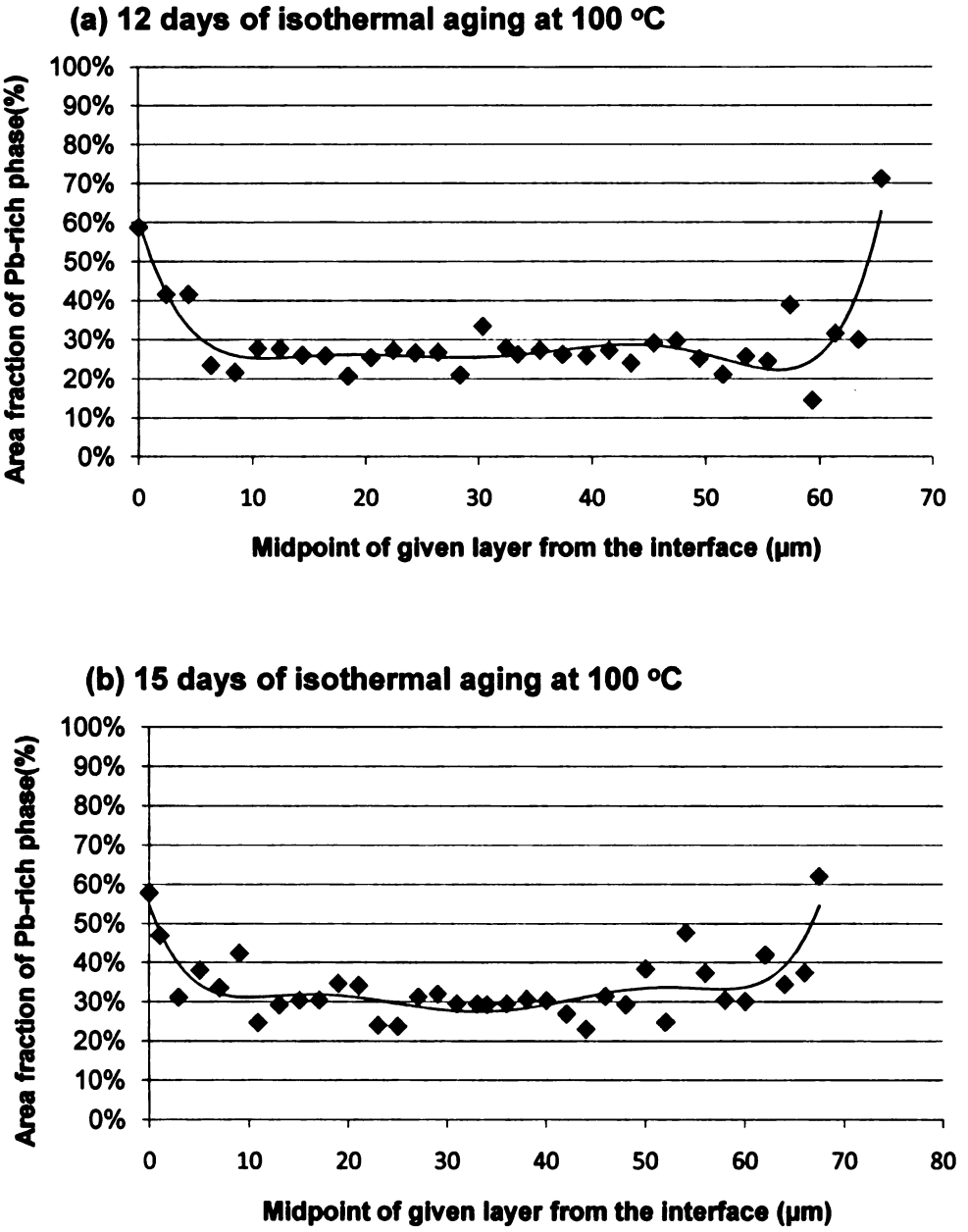


Figure 17. Area fraction of Pb-rich phase (a) Joint isothermally aged for 12 days at 100°C(b) Joint isothermally aged for 15 days at 100°C.

ii. Aging at 150°C

a. Thickness of intermetallic compounds layer at solder/Cu substrate interface

Optical micrographs of the joint coarsened for 3 and 6 days at 150°C are shown in Figure 6 and Figure 7, respectively. Morphologies of Pb-rich and Sn-rich regions in these micrographs indicate that both phases coarsen significantly from isothermal aging. However, the thicknesses of Cu-Sn interfacial IMC layers at both sides are significantly thicker than in joints coarsening at 100°C. Additionally, the total Cu-Sn interfacial IMC layer can be divided into two regions (Cu_6Sn_5+Cu_3Sn). The thicknesses of Cu-Sn interfacial IMC layers at both sides of the joints coarsened for 3 days and 6 days at 150°C are about 5μm and 6 μm thick, respectively. Besides, the thickness of Cu_6Sn_5 layer is greater than the thickness of Cu_3Sn layer.

b. Size distribution of Pb-rich phase within the solder joint

The size distribution of Pb-rich domains in interior region of solder joint isothermal aged at 150°C is shown in Figure8. The results indicate that the aging temperature will have positive influence on the mean size of Pb-rich domain. Compared to joints isothermal aged at 100°C, coarsening of the phases is more significant at higher temperature. In addition, while comparing the size distribution of Pb-rich phase for as-reflowed, 3-days isothermal aged, and 6-days isothermal aged, one can note that isothermally aging of solder joints caused the normalized counts of Pb-rich phases smaller than 10 μm^2 decreased, while larger ones coarsened.

c. Area fraction of Pb-rich phases in the interior region of the joint

The observation of Pb-rich phase occupied in each selected region (220*2 μm^2) layer by layer away from the interface is shown in Figure 9. The concentration of Pb-rich phase is about 30% in the middle region of solder joints and increases at both ends of solder joints. It indicates that there is an accumulation of Pb-rich layer at both ends of solder joints. However, this accumulation layer is not a continuous layer.

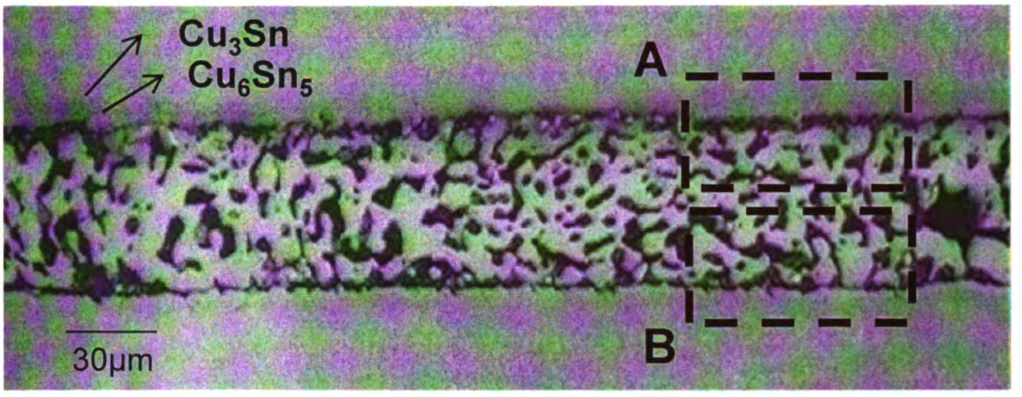


Figure 18a. The image of solder joint isothermally aged at 150 °C for 3 days. The enlarged picture of regions A and B are shown in Figure 6b.

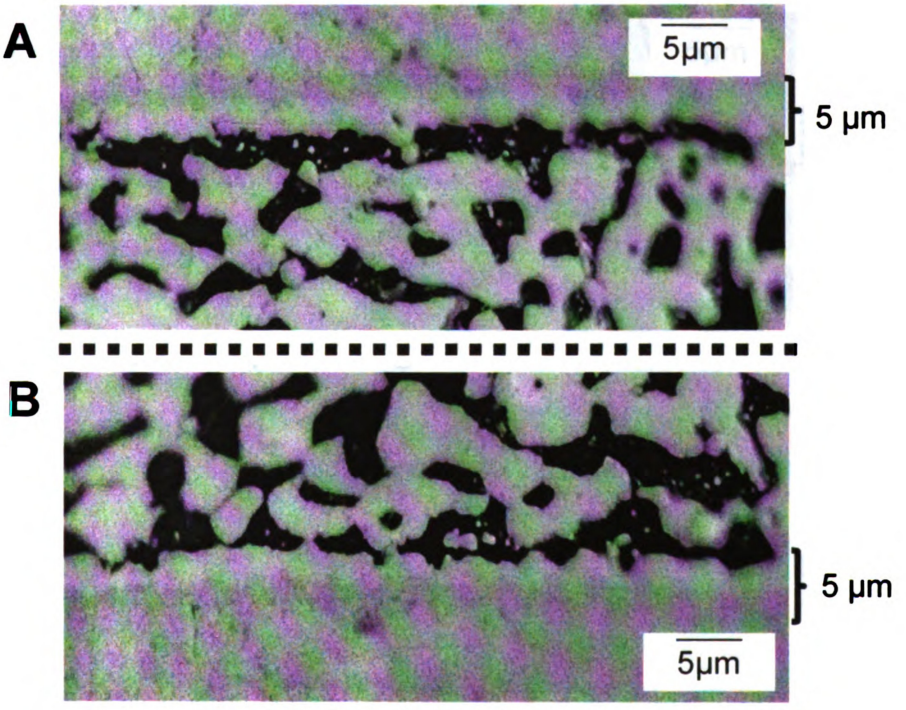


Figure 18b. In regions A and B, IMC layers are both about 5 μm thick.

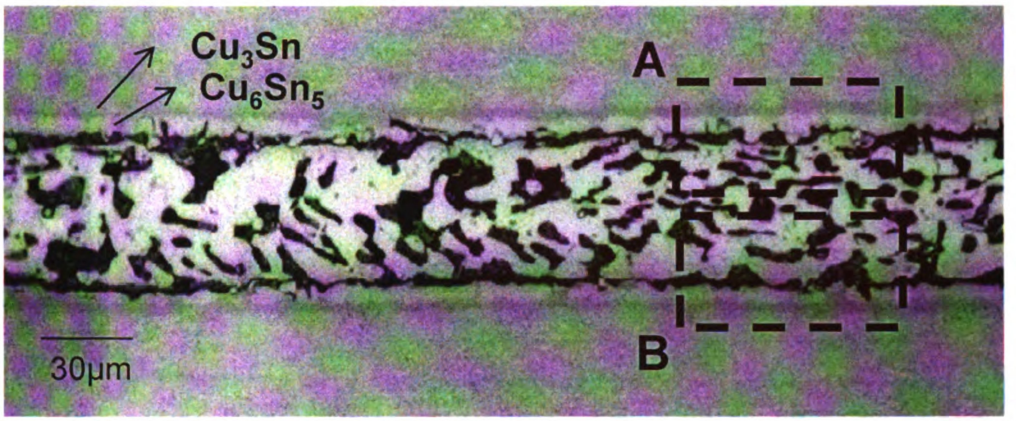


Figure 19a. The image of solder joint isothermally aged at 150 °C for 6 days. The enlarged picture of region s A and B are shown in Figure 7b.

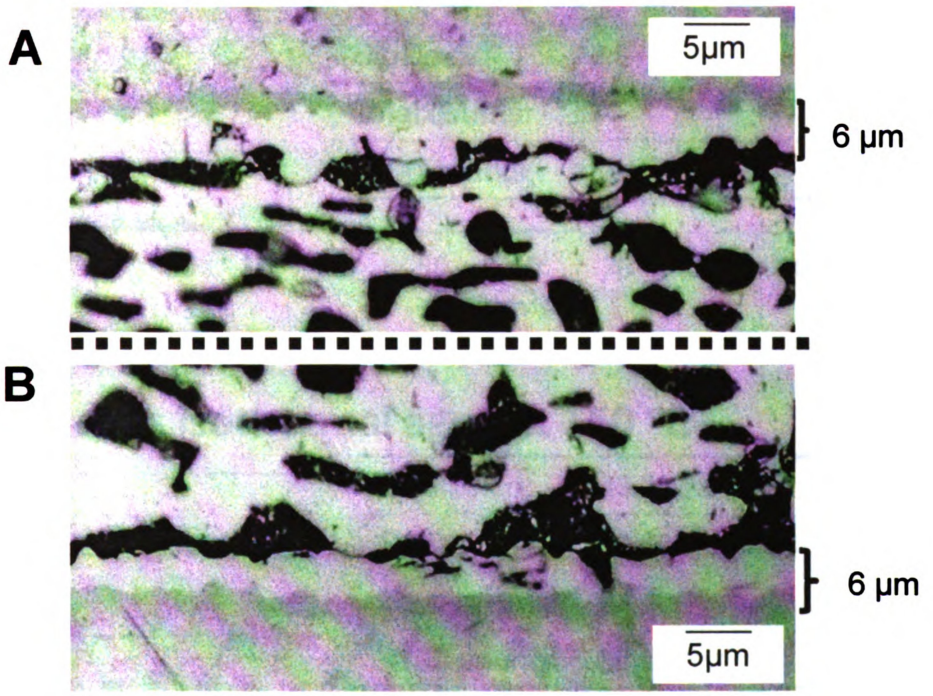


Figure 19b. In regions A and B, IMC layers are both about 6 μm thick.

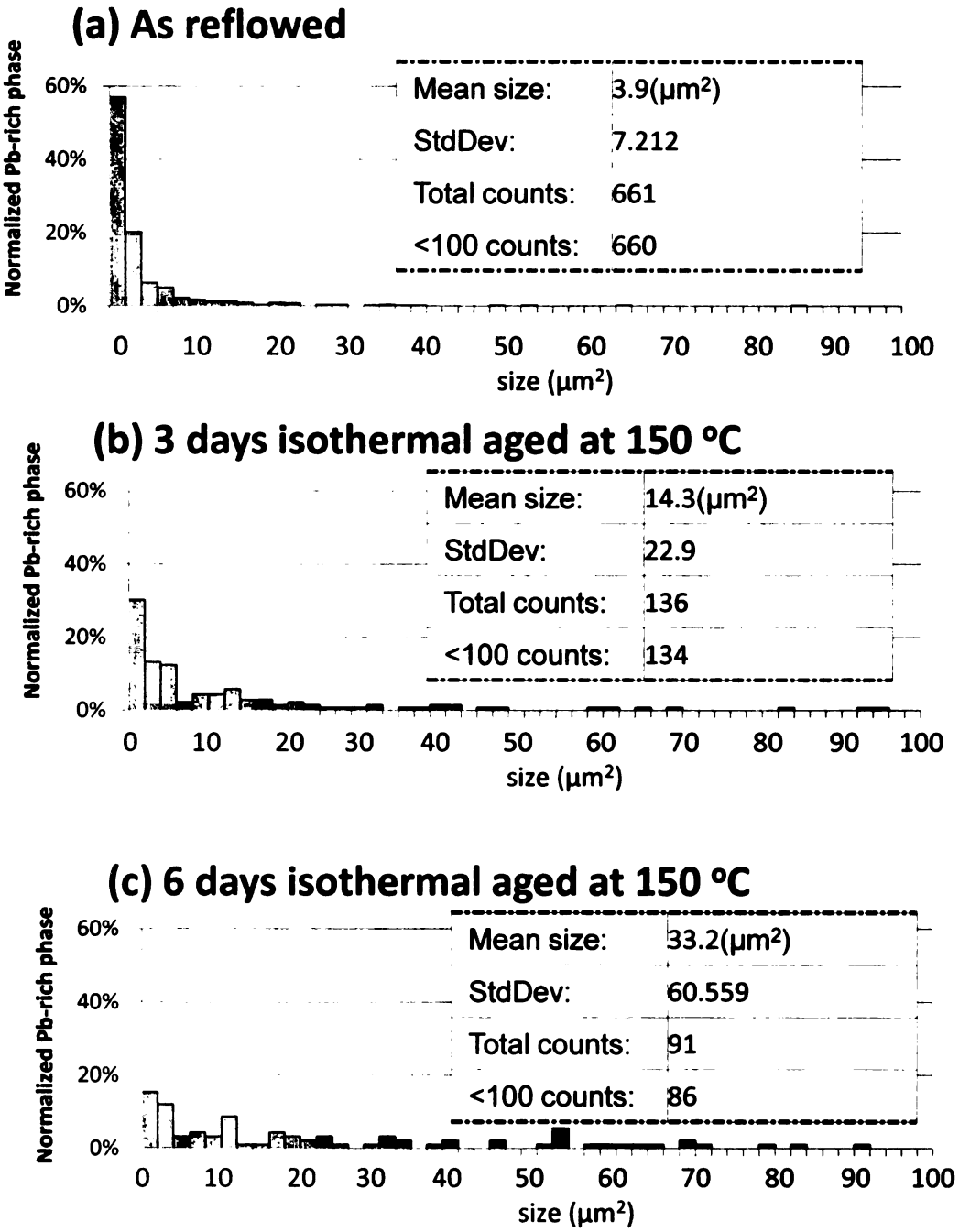


Figure 20. Size distribution of Pb-rich phase within solder joints (a) as-reflowed (b) 3 days of isothermal aged at 150 °C (c) 6 days of isothermal aged at 150 °C.

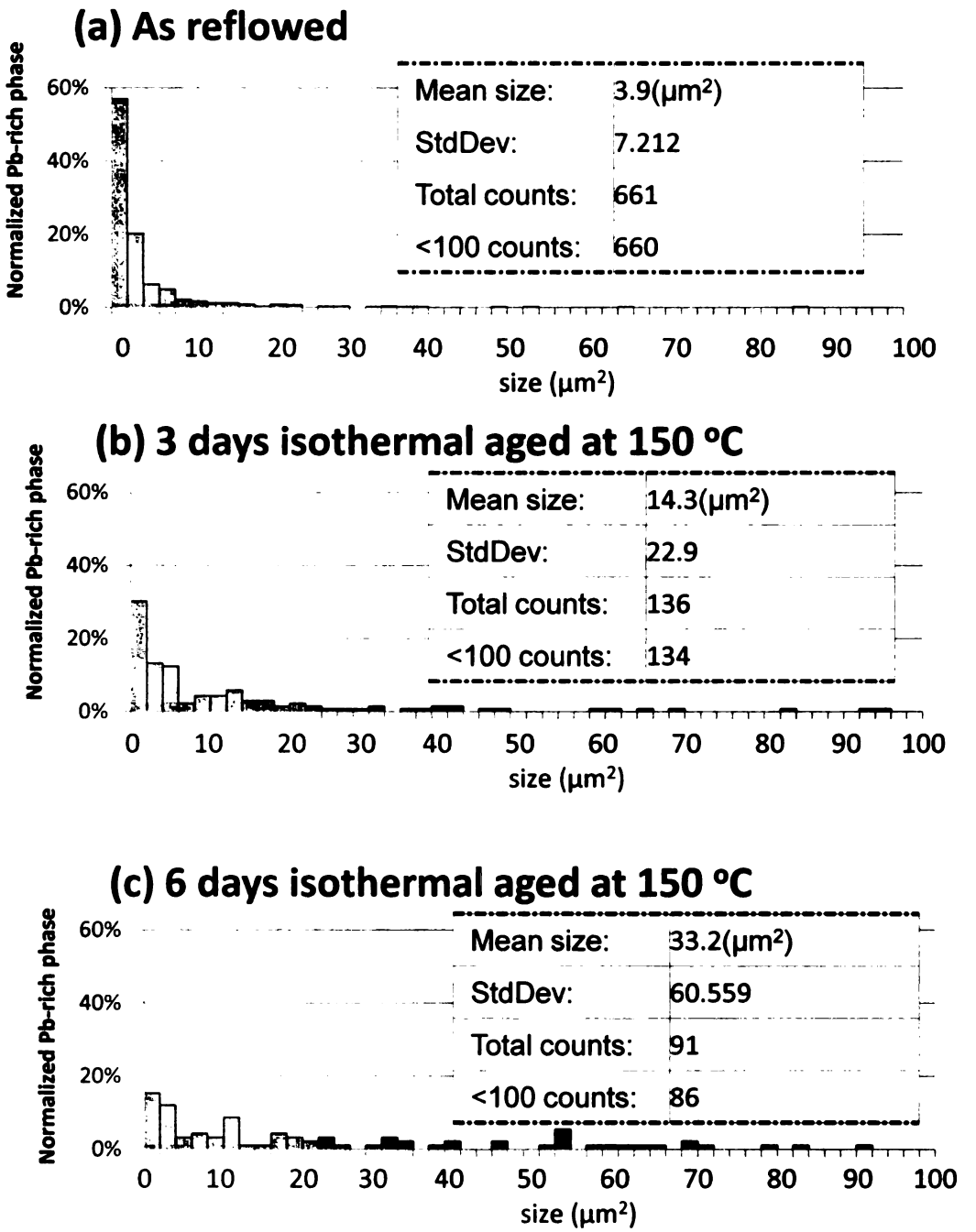
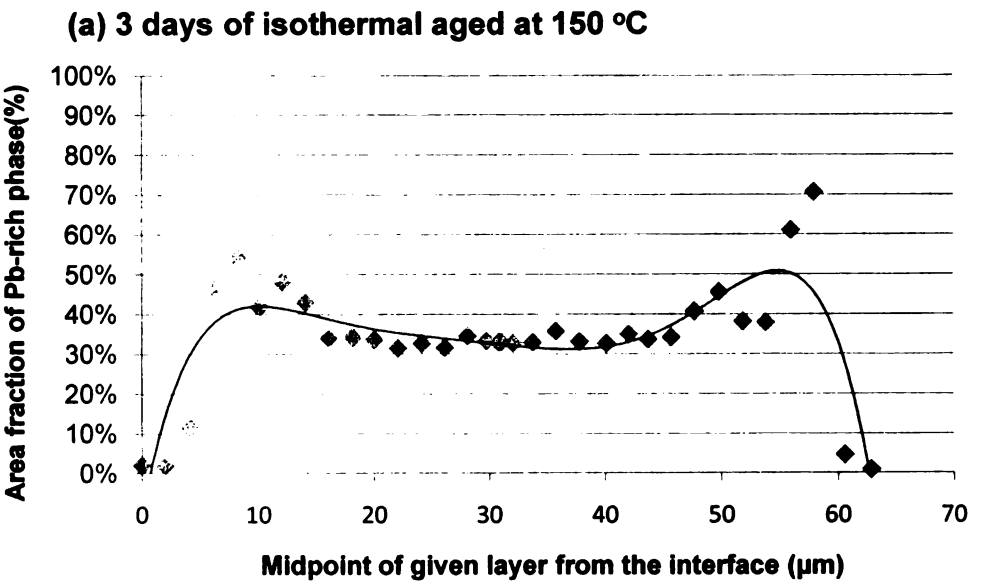


Figure 20. Size distribution of Pb-rich phase within solder joints (a) as-reflowed (b) 3 days of isothermal aged at 150 °C (c) 6 days of isothermal aged at 150 °C.



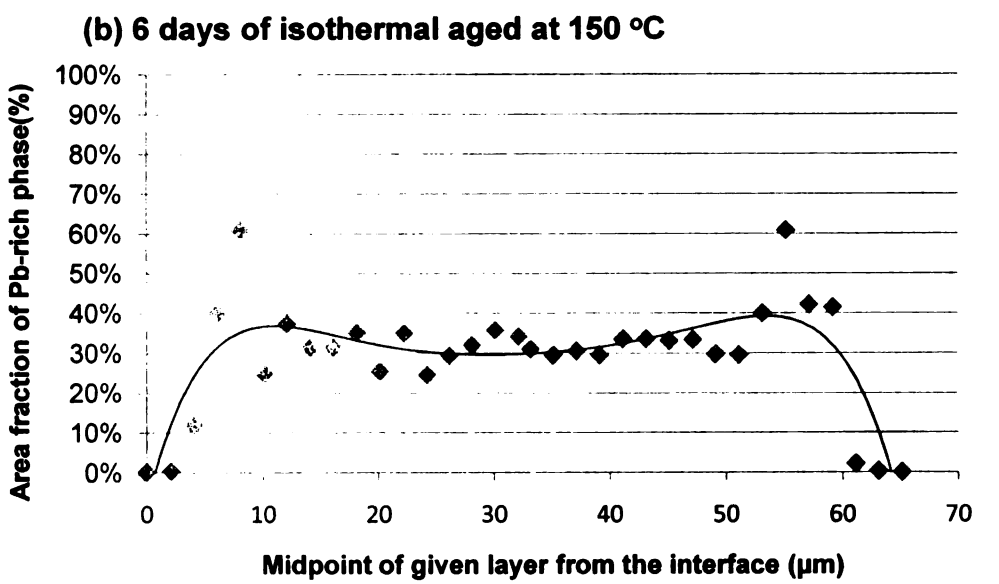


Figure 21. Area fraction of Pb-rich phases in the interior region of solder(a) Joint isothermal aged for 3 days at 150°C(b) Joint isothermal aged for 6 days at 150°C

d. Summary and discussion

Experimental research on the Pb phase coarsening in eutectic Pb-Sn solder joint under isothermal aging is reported. Phase growth is observed under different temperatures and times. Three interesting points should be discussed. First, longer aging time results in larger grain size. Second, isothermal aging does not change the area fraction of Pb. In other words, the distribution of Pb-rich phase and Sn-rich phase is uniform. Third, higher temperature leads to faster grain coarsening and thicker solder/substrate interface IMC layers.

a) More aging days results in larger grain size

Comparing the results of isothermally aging of solder joints with increasing days, it is obvious to find out the grain size is strongly dependent on the time. The experimental results can be explained by the equation $\overline{D}^n - \overline{D_0}^n = Kt = K_o \exp(-Q/RT)t$, provided by Jung et. al [16] where, $\overline{D}$ is the mean linear intercept phase size, $\overline{D_0}$ is the as-reflowed phase size, $n=4.1\pm0.15$, $Q=39.8\pm0.8$kJ/mole, $K_0=1*10^{-23}$-$4.5*10^{-23}$,t is time, T is temperature, and R is Boltzmann constant.

As the initial phase size D_o is fixed, the mean linear intercept of the grain size depends on time. In other words, more aging days results in larger grain size.

b) Isothermal aging does not change the area fraction of Pb-rich phase

While comparing the results of solder joints aged for six days and eletromigrated for six days, one can easily find out that isothermal aging does not change the area fraction of Pb-rich phase. Isothermal aging only causes the enhancement of grain size. Unlike

current stressing, there is no driving force during isothermally aging. Thus, each individual of Pb-rich phase coarsens due to by the self diffusion within solid.

c) Higher temperature leads to faster grain coarsening and thicker IMC layers

Comparing the results of isothermally aging of solder joints at lower temperature (100°C) and at higher temperature (150°C), higher temperature leads to faster grain coarsening and thicker IMC layers. According to Jung et al., $\overline{D}^n - \overline{D_0}^n = K_o \exp(-Q/RT)t$, where n=4.1, Q=39.8kJ/mole, $K_0=1*10^{-23}$-$4.5*10^{-23}$ m^4/s R=8.31 J/K•mole, we can insert T=100°C (373K) and 150 (423K). For constant time and constant initial phase size (D_0), the linear intercept phase size D at higher temperature is always higher than lower temperature. Moreover, in solid-state aging, it grows a thicker layer of Cu_3Sn and Cu_6Sn_5 at solder/substrate interface at higher temperature. It is because higher temperature has higher diffusion rate resulting in higher rate of Cu-Sn reactions. In addition, under such condition the thickness of Cu_6Sn_5 is greater than the thickness of Cu_3Sn.

3.2. Electromigration study

In this chapter, as-reflowed joints without subjected to current stressing with a current density of 10^4 Amp/cm^2 for 20 days at 100°C and for 6 days at 150°C, respectively will be provided. The structure of this chapter will be organized into 3 parts: first, SEM observations will be given to show the surface features, such as valley/hillock formation. Second, for the purpose of revealing detailed microstructures at regions below the valley/hillock formation, the specimens were metallographically polished to remove the surface manifestations. Thus, a clear image of optical micrograph and the characteristic of IMC layers will be demonstrated; followed by an analysis of the size distribution of Pb-rich phase within solder region; and then another analysis of the area fraction of Pb-rich phase will also be provided in the last part of this chapter.

i. Current stressing at 100°C for 20 days

Solder joints without isothermal aging exposed to current stressing with current density of 10^4 Amp/cm^2 for 20 days exhibited electromigration behavior result in the surface features shown in Figure 10a and 10b. SEM observations illustrate that the valley formed near the cathode and extruded a gentle hillock at the anode. Figure 10b, which is a manifestation of the same feature by tilting the specimen by 45°, shows the contrast of valley/hillock more clearly. The microstructure noted in interior regions below the hillock and valley are presented in Figure 11. These orientation show that the morphologies of both Pb-rich and Sn-rich regions were coarsened from current stressing. As the result indicates, there was a dense layer of Pb-rich phase accumulated at the anode end of the solder. The accumulation of Pb-rich layer was about 5 μm thick.

a. Characteristics of solder/substrate intermetallic compound layer

Optical micrographs of as-reflowed solder joints subjected to current stressing for 20 days at 100°C are shown in Figure 11a and b. The thicknesses of Cu-Sn interfacial IMC layers at both sides are thicker than initial microstructure. The thicknesses of Cu-Sn interfacial IMC layers at both sides are about 2 μm. Besides, the thickness of Cu_6Sn_5 is greater than the thickness of Cu_3Sn. In the interior regions of the solder, far away from the solder/substrate interface, Cu_6Sn_5 particles were found near anode.

b. Size distribution of Pb-rich phase within the solder joint

At 100°C, the size distribution of Pb-rich domain in the interior region for the joint that was not aged and subjected to current stressing for 20 days is shown in Figure 12. While comparing the size distribution of Pb-rich phase of as-reflowed solder joint (Figure 4a) with joint subjected to current stressing for 20 days (Figure 12), one can be observe that the mean size of Pb-rich area were coarsened after current stressing for 20 days. In addition, the standard deviation is significantly increased, indicating the sizes of individual Pb-rich phase regions are significantly different from each other.

c. Area fraction of Pb-rich phase between two Cu substrates

Area fraction of Pb-rich phase in the interior region between two Cu substrates for as-reflowed solder joint subjected to current stressing at 100°C is shown in Figure 13. The trendline remains at about 30% until a distance of 55 μm away from cathode is reached, where it increased significantly. Hence, two-layer segregation of Pb-

rich and Sn-rich becomes obvious. Besides, there is a continuous Pb-rich layer at distance of 63 μm away from cathode.

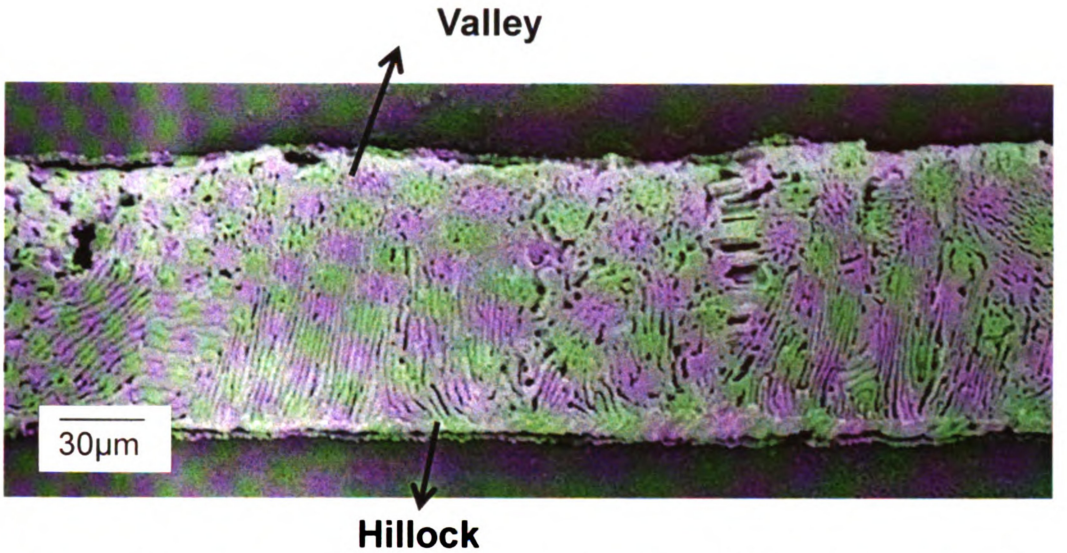


Figure 22a. The overview SEM image of as-reflowed solder joint subjected to current stressing for 20 days at 100 °C.

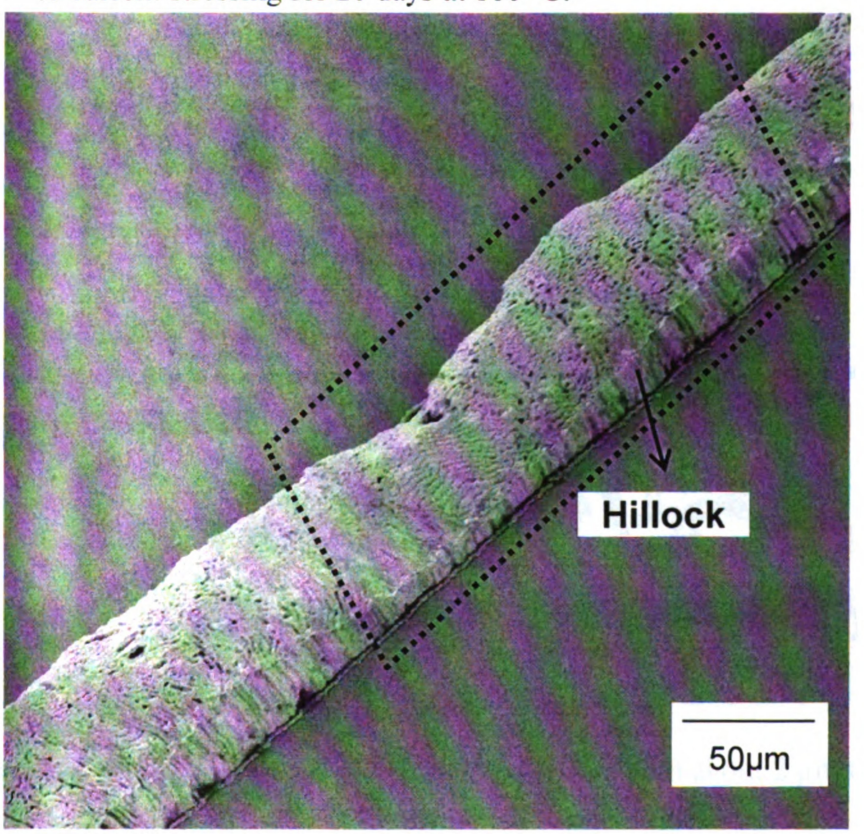


Figure 22b. As-reflowed solder joint subjected to current stressing for 20 days at 100 °C. Inside the dotted area is the tilted image of Figure 10a.

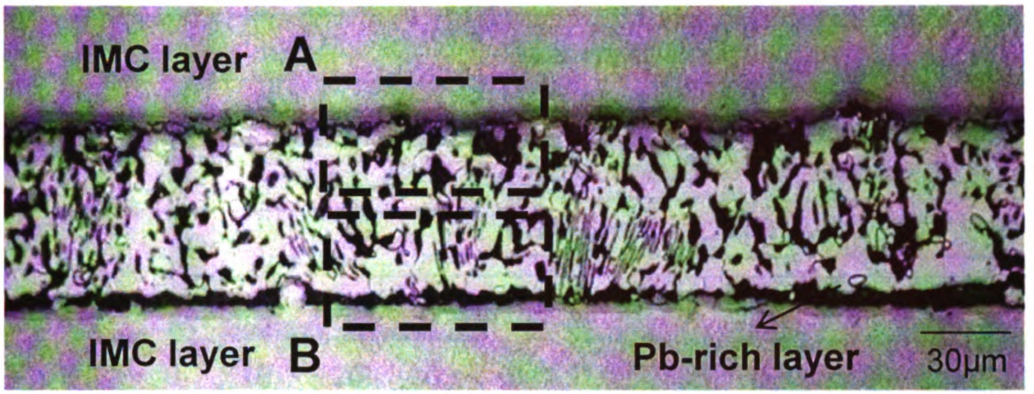


Figure 23a. The image of as-reflowed solder joint subjected to current stressing for 20 days at 100 °C. The Pb-rich accumulation layer is about 5 μm thick. The enlarged picture of regions A and B are shown in Figure 11b.

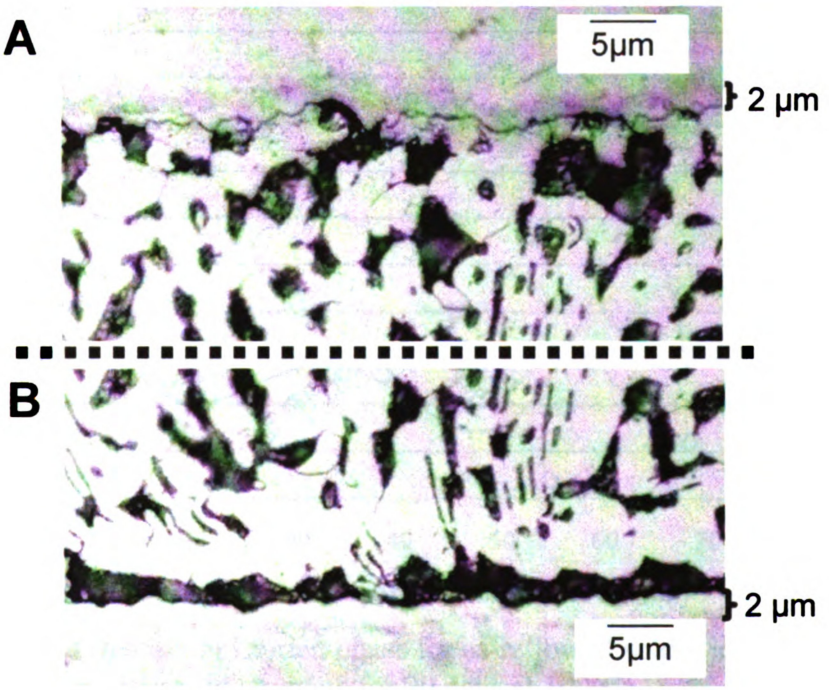


Figure 23b. In region s A and B, IMC layers are both about 2 μm thick.

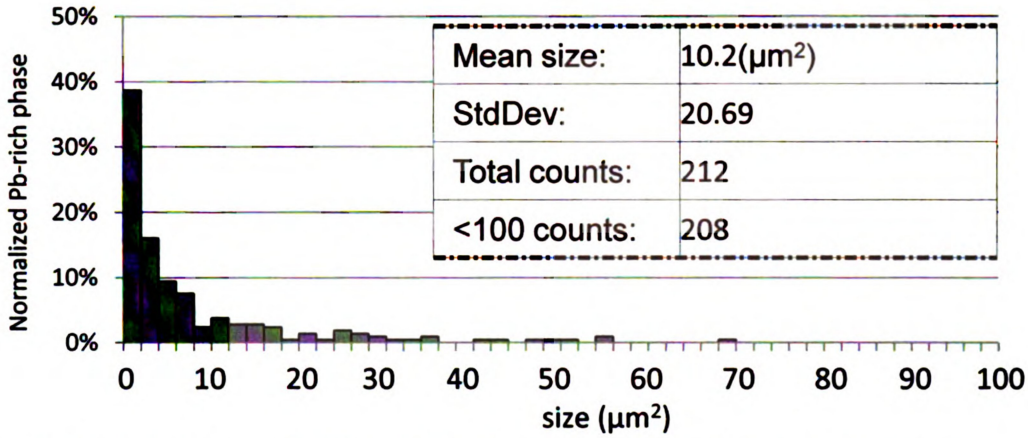


Figure 24. Size distribution of Pb-rich phase in as-reflowed solder joint subjected to current stressing for 20 days at 100 °C.

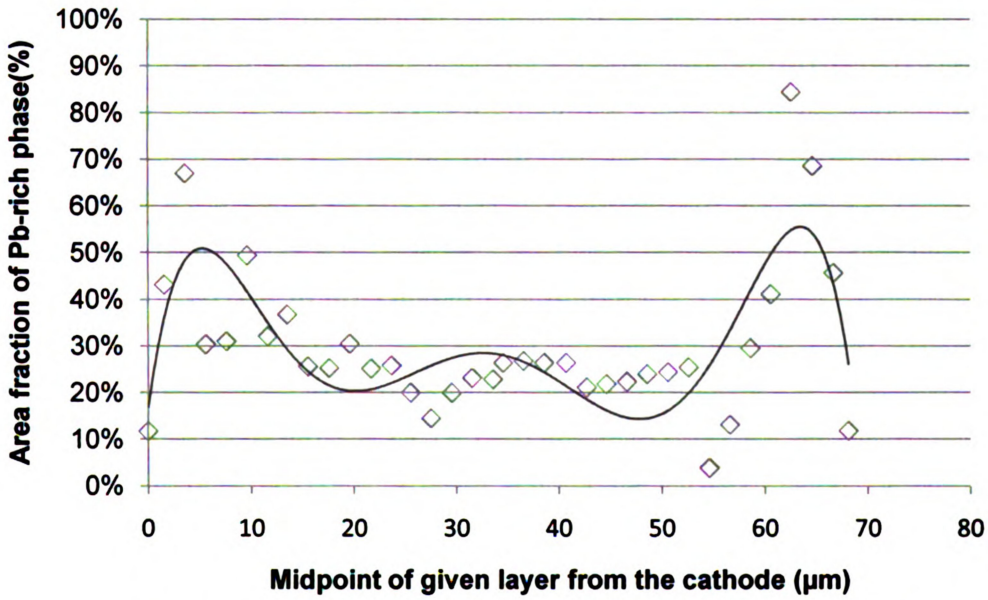


Figure 25. Area fraction of Pb-rich phase for as-reflowed solder joint subjected to current stressing for 20 days at 100°C.

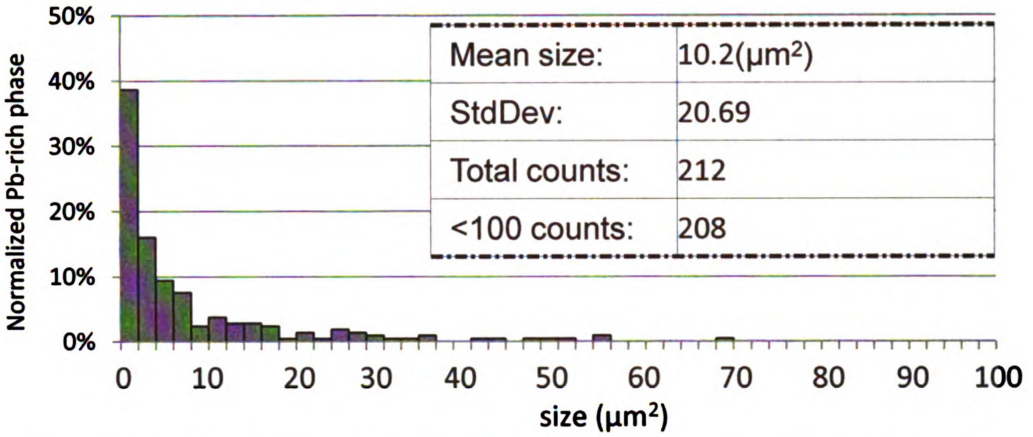


Figure 24. Size distribution of Pb-rich phase in as-reflowed solder joint subjected to current stressing for 20 days at 100 °C.

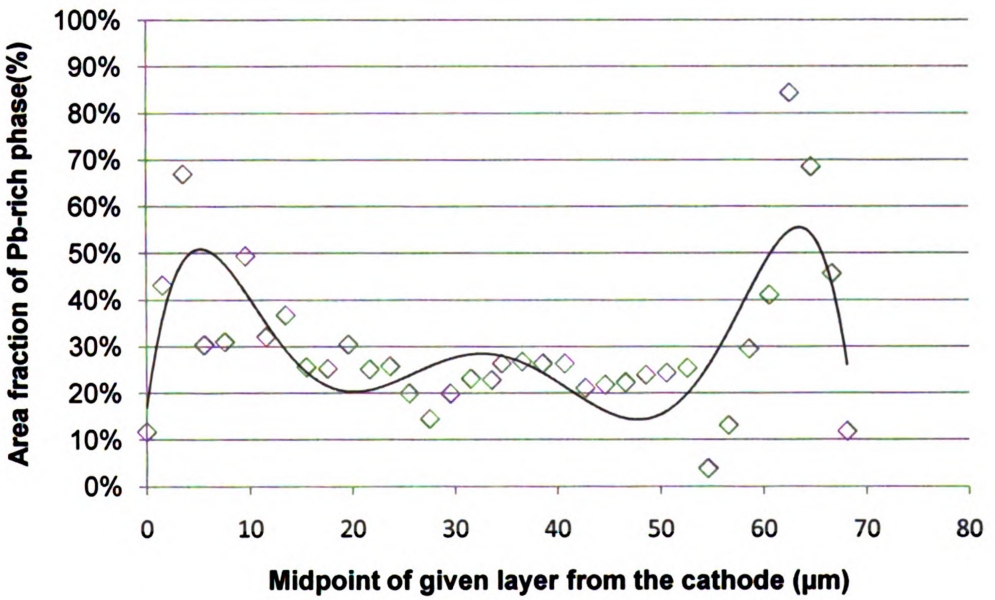


Figure 25. Area fraction of Pb-rich phase for as-reflowed solder joint subjected to current stressing for 20 days at 100°C.

ii. Current stressing at 150 °C for 6 days

Solder joints without isothermal aging exposed to current stressing with a current density of 10^4 Amp/cm^2 for 6 days at 150°C exhibited the surface feature shown in Figures 14a and 14b. These SEM observations illustrate the valley formed near the cathode with a gentle hillock formed near the anode. Figure 14b is view tilted by 45° for illustrate the contrast of valley/hillock more clearly. Compared to those stressed at 100°C for 20 days, the valley/hillock formation is more significant when current stressing at 150°C is carried out. The microstructure in interior regions of this specimen from current stressing is presented in Figure 15. It illustrates the coarsening of Pb-rich and Sn-rich regions from current stressing. As can be seen, there is a dense layer of Pb-rich phase accumulated at the anode end of the solder joint. The accumulation of Pb-rich layer was about 10 μm thick. In the interior regions of the solder, far away from the solder/substrate interface, Cu_6Sn_5 particles were also found.

a. Characteristic of intermetallic compound

Optical micrographs of as-reflowed solder joints subjected to current stressing for 6 days at 150°C are given in Figure 15b and 15c. The thicknesses of Cu-Sn interfacial IMC layers at both sides are thicker than initial microstructure and are asymmetric. The thickness of IMC layer at anode is 2 μm greater than at cathode. Besides, the total Cu-Sn interfacial IMC layer can be divided into two regions (Cu_6Sn_5+Cu_3Sn). At anode, the thickness of Cu_6Sn_5 is greater than the thickness of Cu_3Sn. However, at cathode, the thickness of Cu_3Sn is greater than the thickness of Cu_6Sn_5.

b. Size distribution of Pb-rich phase within the solder joint

Size distribution of Pb-rich phase for as-reflowed solder joint subjected to current stressing for 6 days at 150°C is shown in Figure 16. The mean size of Pb-rich phase was increased from 3.6 μm^2 to 55.7 μm^2, which indicates the Pb-rich phase has significantly coarsened from current stressing. Besides, the standard deviation of Pb-rich phase was increased from 10 to 100, which indicates the size of each individual Pb-rich phase is different from each other. In other words, with the driving force resulting from current stressing, each individual Pb-rich phase was not only coarsened but also combined together.

c. Area fraction of Pb-rich phase between two Cu substrate

Area fraction of Pb-rich phase between two Cu substrates is shown in Figure 17. There are two interesting points that should be mentioned. First, the accumulation of Pb-rich layer near anode is significant. A continuous layer of Pb-rich phase is observed at a distance of 55 μm to 60 μm away from the cathode. Second, the trendline of area fraction of Pb-rich phase increases significantly, which indicates the segregation of Pb-rich and Sn-rich is significant. However, the situation would become distinctly different near the cathode. No continuous layer of Pb-rich phase or segregation of Pb-rich phase and Sn-rich phase were found near the cathode.

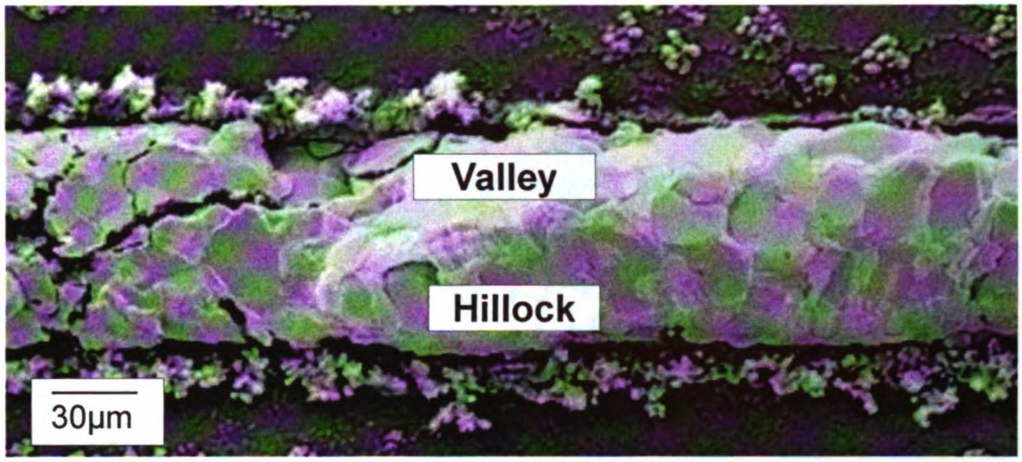


Figure 26a. The overview SEM image of as-reflowed solder joint subjected to current stressing for 6 days at 150 °C.

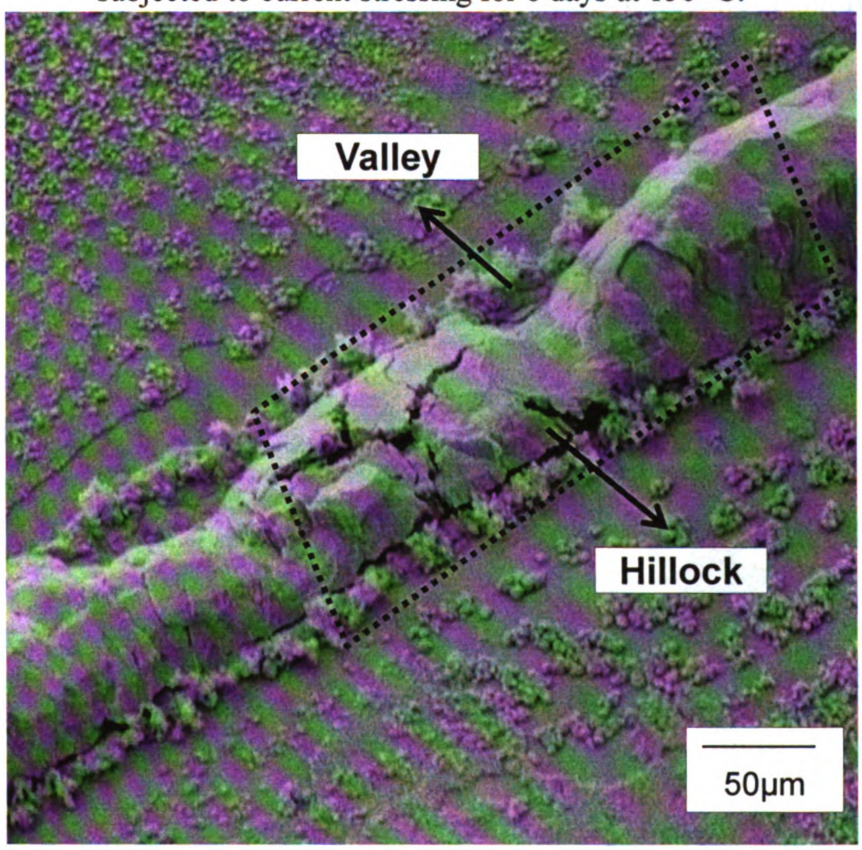


Figure 26b. As-reflowed solder joint subjected to current stressing for 6 days at 150 °C. Inside the dotted area is the tilted image of Figure 10a.

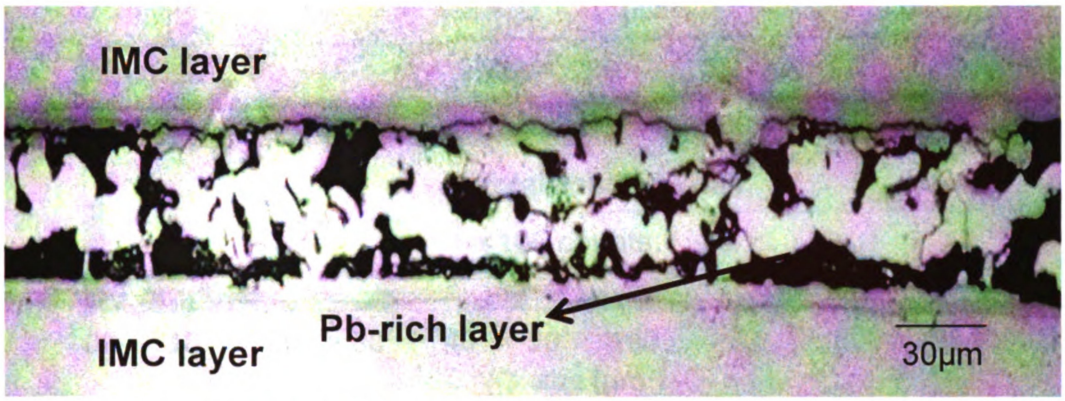


Figure 27a. The image of as-reflowed solder joint subjected to current stressing for 6 days at 150 °C. The Pb-rich accumulation layer is about 10 μm thick. The enlarged picture of regions A and B are shown in Figure 15b.

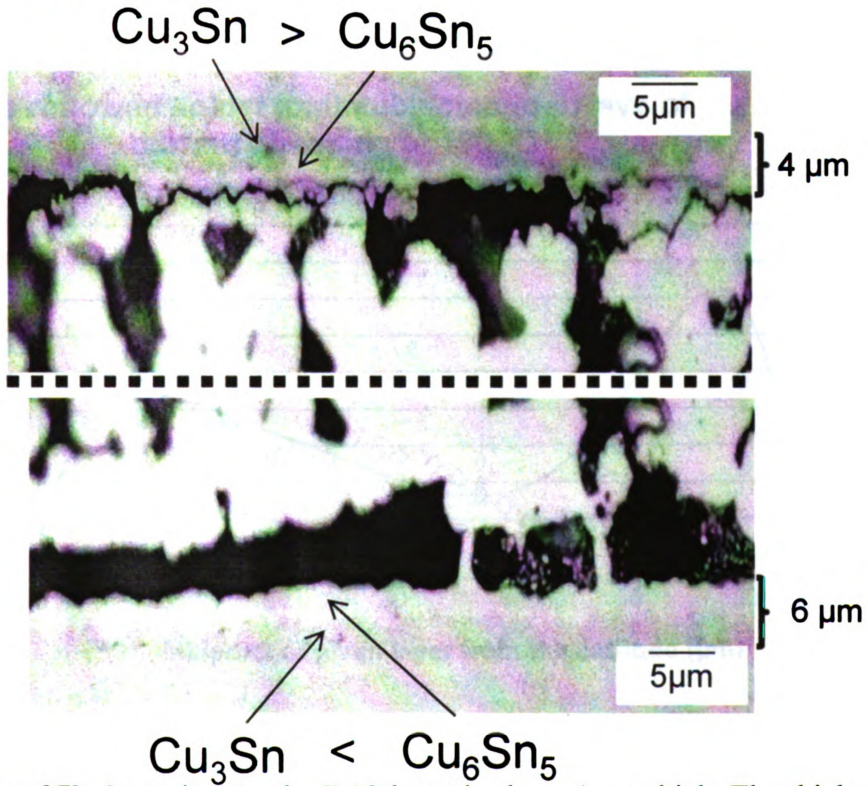


Figure 27b. In region A , the IMC layer is about 4 μm thick. The thickness of Cu_3Sn layer is thicker than Cu_6Sn_5 layer. In region B, the IMC layer is about 6 μm thick. The thickness of Cu_3Sn layer is thinner than Cu_6Sn_5 layer.

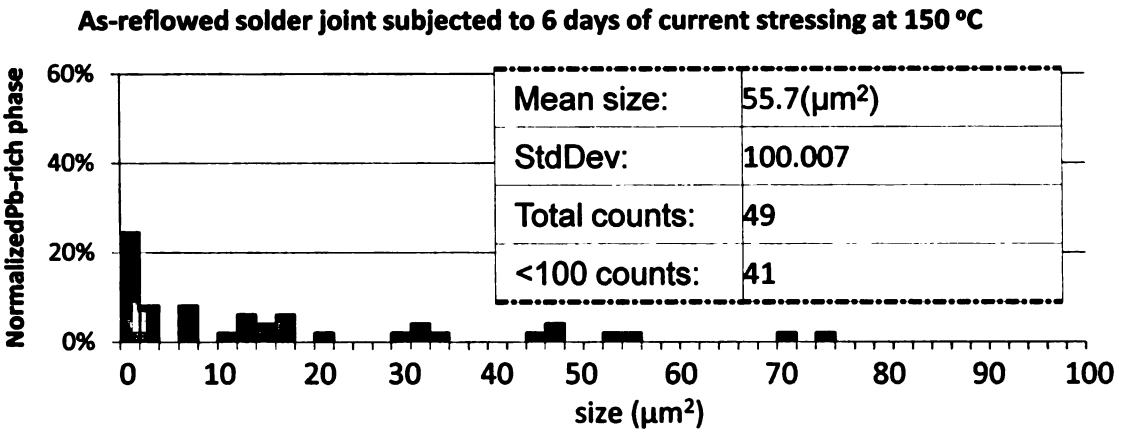


Figure 28. Size distribution of Pb-rich phase for joint without coarsening subjected to current stressing for 6 days at 150 °C.

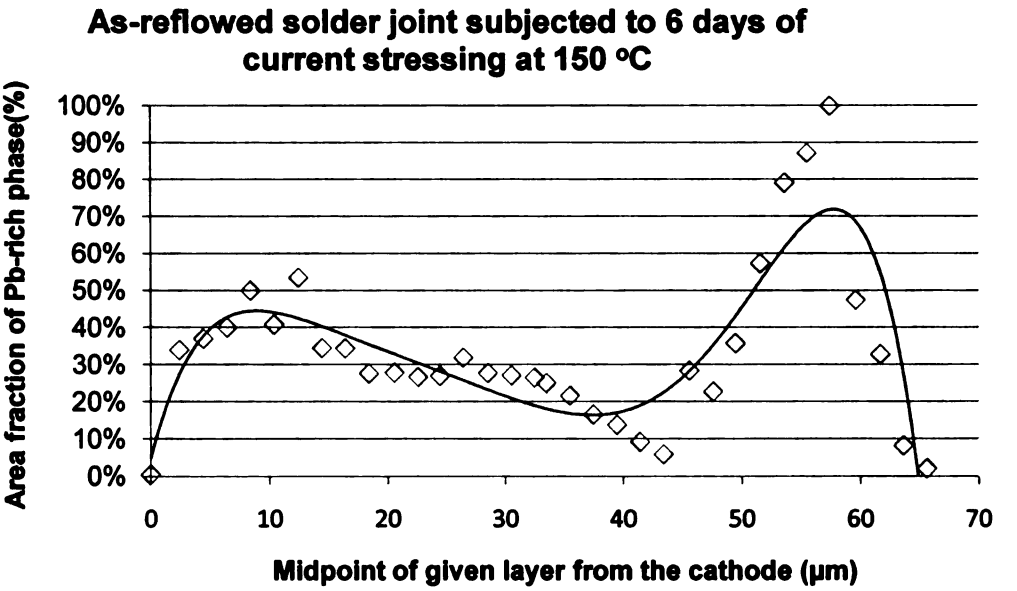


Figure 29. Area fraction of Pb-rich phase for as-reflowed joint subjected to current stressing for 6 days at 150°C

d. Summary and discussion

Electromigration study on as-reflowed solder joints under two different temperature of 100°C and 150°C was reported in this section. Regardless of temperature, three interesting points were noted to occur due to electromigration. First, current stressing results in large accumulation of Pb-rich layer near the anode. Second, the area fraction of Pb-rich phase near the anode is more than near the cathode. Third, solder/substrate interface IMC layer is thicker at the anode than at the cathode. While comparing two different current stressing temperatures (100°C and 150°C), the segregation of Pb-rich phase and Sn-rich phase under higher temperature is more significant.

a) Current stressing results in large accumulation of Pb-rich phase at the anode

After electromigration with current density of 10^4 Amp/cm^2, the interwoven lamellar eutectic structure nearly translated into a two layer structure of Pb-rich phase and Sn-rich phase near anode. Because Pb does not react with Cu, this segregation implies that with a driving force of current stressing, Pb is driven in the same direction of the electron flow towards anode resulting in accumulation at the anode.

b) The percentage of Pb-rich domain at the anode is higher than the cathode

After electromigration with a current density of 10^4 Amp/cm^2, Pb is driven in the same direction of electron flow from the cathode to the anode. So, unlike in the aging study, the area fraction of Pb-rich phase near the anode after electromigration is always

more than that near the cathode. In other words, atomic movement resulted from electromigration causes the uneven distribution of Pb-rich phases.

c) IMC layer is thicker at the anode than at the cathode

After electromigration with a current density of 10^4 Amp/cm^2, asymmetry in the growth of Cu-Sn interface IMC layer is observed. The Cu-Sn IMC layer is thicker at the anode than at the cathode. It is because Sn is driven in the same direction of electron flow and reacts with Cu. So, the growth of both Cu_3Sn and Cu_6Sn_5 at the anode would be enhanced. Other excessive Sn atoms are squeezed out from the anode by compressive stresses as a consequence of electromigration [8]. Besides, the thickness of Cu_3Sn is greater than Cu_6Sn_5 near cathode. It is because Sn is driven away from the cathode. Thus, lack of Sn to react with Cu. In other words, present of more Cu than Sn results in the thicker Cu_3Sn layer than the Cu_6Sn_5 layer.

d) Higher temperature leads to more significant electromigration behavior

Electromigration is a diffusion-control mechanism. So, it follows the rule of $D=D_0 \exp(-Q/RT)$. As the temperature increases, the diffusivity increases. Thus, the atomic movement during electromigration is faster at higher temperature. However, diffusion mode and diffusion species under electromigration at 100°C and 150°C are still unclear. It is generally believed that the mode of diffusion path at 100°C is lattice diffusion and at 150°C is through grain boundary. If this saying is true, as we change the size of grain boundary, the electromigration phenomenon should remain the same at 100°C and change at 150°C. So, in the next chapter, the results of coarser microstructure after current stressing will be provided to see the effect of coarsened microstructure.

3.3. Effect of coarsened microstructure on electromigration

In this section, joints isothermally aged to different extents of microstructure coarsening were subjected to current stressing with current density of 10^4 Amp/cm^2 for 20 days at 100°C and for 6 days at 150°C. The structure of the chapter will be organized into 3 parts: first, SEM observations will be given to show surface features, such as the valley/hillock formation resulting from electromigration. Second, optical micrographs and the characteristic of IMC layers resulting from electromigration will be presented; followed by an analysis of the size distribution of Pb-rich phase within solder region. Another analysis of area fraction of Pb-rich phase will also be provided to compare with those noted in as-reflowed solder joints in the last section of this chapter.

i. Current stressing on coarsened microstructure for 20 days at 100°C

Through SEM observations, the passage of high current density is given in Figure 18. It can be noted that no significant valley/hillock formation in the solder joint isothermally aged for 15 days in Figure 18b. Figure 18b is tilted 45° view for showing the contrast of the image. The dotted area is the same region as shown in Fig 18a. However, a comparison with the surface geometry observation on as-reflowed specimen, the undulation of the surface was not significant in the joint coarsened for 15 days.

a) Joint coarsened for 12 days at 100°C subjected to current stressing for 20 days

Feature in a solder joint coarsened for 12 days at 100°C followed by current stressing for 20 days at 100°C is shown in Figure 19. There are several microstructural features that are different from the observation on as-jointed specimen subjected to current

stressing. First, the size distribution of Pb-rich phases was more random. Second, the accumulation of Pb-rich layer is about 3 μm in thickness, which is thinner than that observed in as-reflowed solder joint. Third, the grain area size of Pb-rich domains were more coarsened than as-reflowed joints subjected to current stressing due to the fact that they had been coarsened for 12 days prior to current stressing. Last, fewer Cu_6Sn_5 were found in the interior of the solder as compared to that in as-reflowed solder joint subjected to current stressing, and the thickness of interfacial Cu-Sn layer at both interface is about 2 μm thick.

b) Joint coarsened for 15 days at 100°C subjected to current stressing for 20 days

The interior microstructures evolution of the solder joint coarsened for 15 days subjected to current stressing for 20 days at 100°C is shown in Figure 20. The results indicate that the two-layer segregation of Pb-rich and Sn-rich region was hardly observed because the Pb-rich and Sn-rich phases were randomly distributed and the accumulation of Pb-rich layer near anode was not as much as joints without coarsening subjected to current stressing (Figure 11). The thickness of Pb-rich layer was about 2 μm. In addition, there were less Cu_6Sn_5 phase observed inside the solder matrix and a fewer amount of IMCs nucleated at both interfaces.

a. Characteristic of intermetallic compound

Thickness of IMC layer for different experimental conditions at 100°C was shown in Table 1. Two interesting points should be mentioned. First, the thickness of IMC layer is symmetric for the joint current stressed at 100°C. Whether the joints were

coarsened or not, the thickness of IMC layer at both sides are the same. Second, for as-reflowed solder joints subjected to current stressing, the thickness of Cu_6Sn_5 layer near cathode is smaller than the thickness of Cu_3Sn layer. However, for solder joints aging prior subjected to current stressing, the thickness of Cu_6Sn_5 layer near cathode is greater than the thickness of Cu_3Sn layer.

b. Size distribution of Pb-rich phase within the solder joint

Size distribution of Pb-rich phase within the solder joint for coarser microstructure subjected to current stressing for 20 days at 100°C is shown in Figure 21. Compared with the as-reflowed solder joint subjected to current stressing (Figure 11), the average area of Pb-rich domain is more coarsened since the solder joint had experienced a thermal annealing treatment for more days before current stressing.

c. Area fraction of Pb-rich phase in the interior region between two Cu substrates

The observation of Pb-rich phase occupied in each selected region (220*2 μm^2) layer by layer away from the interface is shown in Figure 22a and 22b. While comparing with samples that reacted isothermal aging only (Figure 5a-b), one can find that current stressing does influence the area fraction of Pb-rich phase. There are few interesting things to note. First, from the center towards cathode, the distribution of Pb-rich phase remains constant at 30%. However, from the center towards anode, the distribution of Pb-rich phase depends on whether the microstructure is coarsened or not. Isothermally aging for longer period of time condition, more uniform distribution of Pb-rich phase is. For

example, in Figure 13 (joint without coarsening), there was a drop in Pb-rich phase around 55 μm away from the interface, and a pile-up at 62 μm away from the interface. In other words, there is a significant segregation of Pb-rich phase and Sn-rich phase near the anode. On the other hand, in Figure 22c (joint coarsened for 15 days), it is relatively constant in the distribution of Pb-rich phase. There is no such segregation of Pb-rich phase and Sn-rich phase since the joint was coarsened.

Additionally, in order to quantify the accumulation of Pb-rich phase near anode, method described in experimental procedure 3.2 p.25 was used. By changing the thickness of a selective region and comparing the area fraction of Pb-rich phase with each selected region (120*2 μm^2), one can draw a chart of the percentage of Pb-rich phases vs. distance away from the cathode as shown in Figure 23. From this chart, the thickness of Pb-rich layers and the segregation of Pb-rich phase and Sn-rich phase near anode can be examined.

The percentage of Pb-rich phase for the joint without coarsening subjected to current stressing remains at 30% to a distance of 55 μm away from anode and this exhibits an increasing trend. Because the trendline increased significantly, we know the two-layer segregation of Pb-rich and Sn-rich phase is significant. On the other hand, as the result indicates, the accumulation of Pb-rich layer for the joint coarsened for 15 days subjected to current stressing, the trendline remains at 30% and gradually increased without dropping at distance away from cathode about 60 μm. So, the two-layer segregation is not significant in joint aged for 15 days because the slope of the trendline is relatively small compared to the joint without coarsening. In addition, as the result indicates, for fine microstructure, the area faction of Pb-rich phase almost reaches to

100%, which implies that there is a continuous layer of Pb-rich layer near anode. On the other hand, for coarser microstructure, the maximum area fraction of Pb-rich phase is around 80%. Thus, there is no continuous layer of Pb-rich layer near anode.

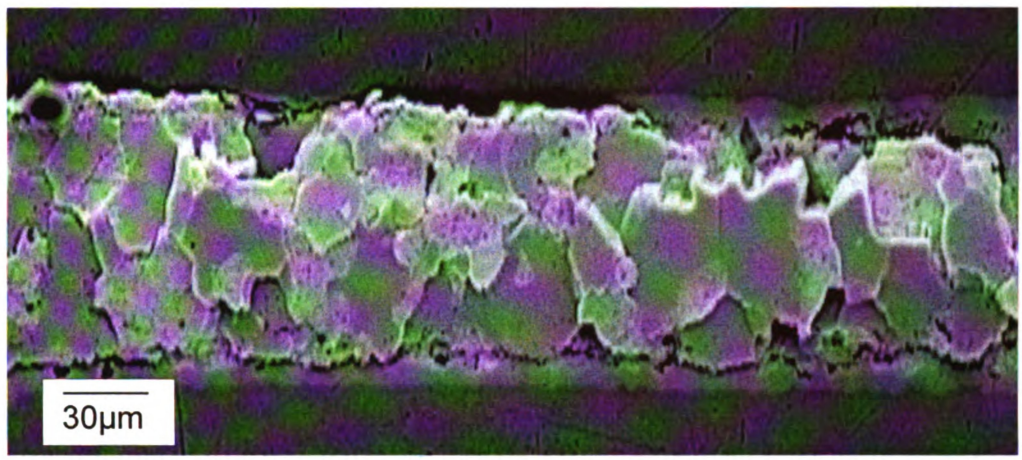


Figure 30a. The overview SEM image for Joint coarsened for 15 days at 100°C and subjected to current stressing for 20 days at 100°C.

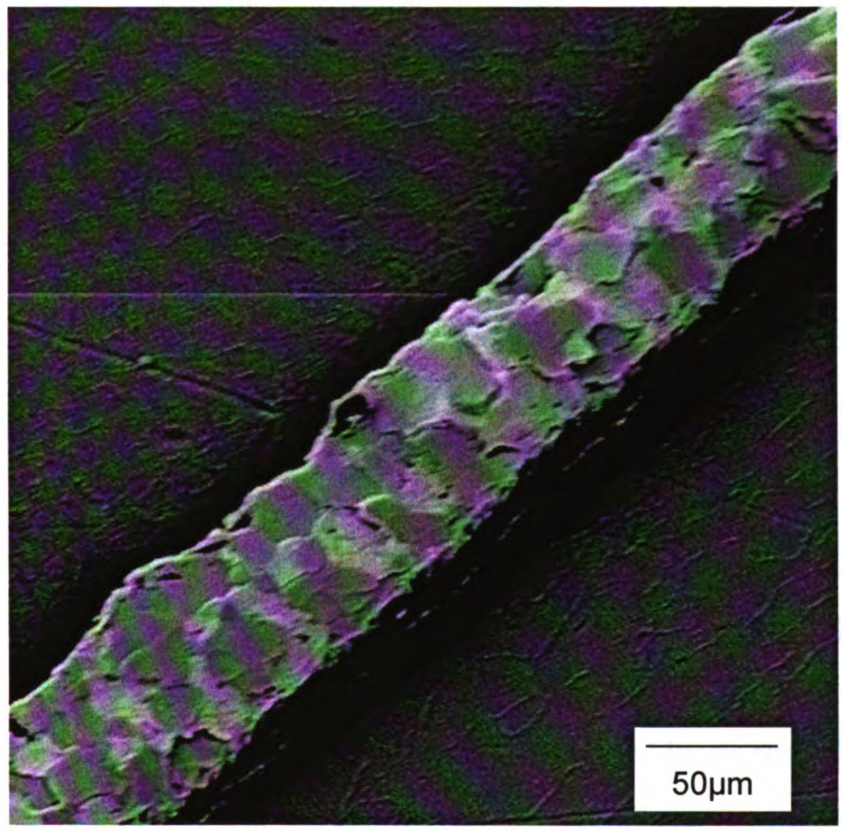


Figure 30b. Joint coarsened for 15 days at 100°C subjected to current stressing for 20 days at 100°C. Joint was tilted by 45°. The dot area is the same region as Figure 18a. No hillock/valley formation was noted.

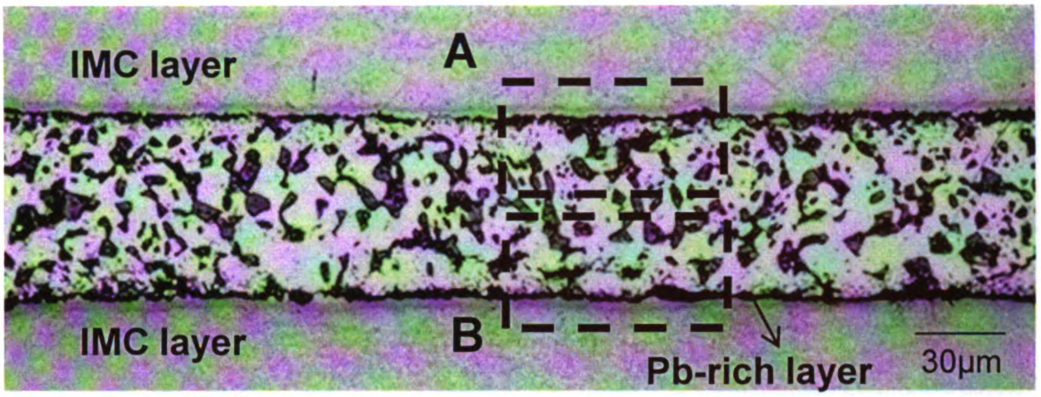


Figure 31a. The image of solder joint isothermally aged at 100 °C for 12 days and subjected to current stressing for 20 days at 100 °C. The enlarged picture of regions A and B are shown in Figure 19b.

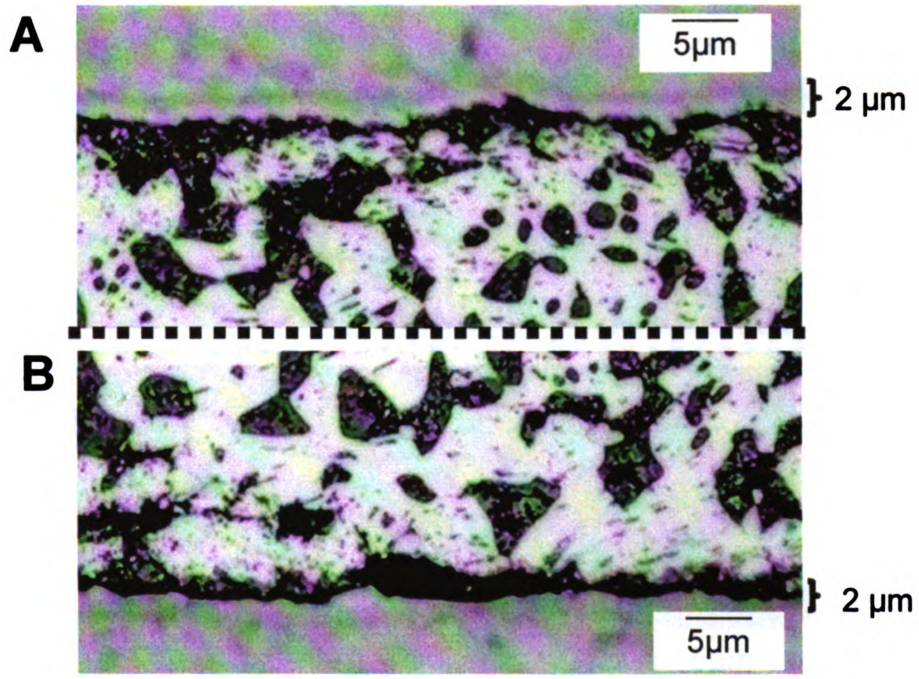


Figure 31b. In region s A and B, solder/substrate IMC layers are both about 2 μm thick.

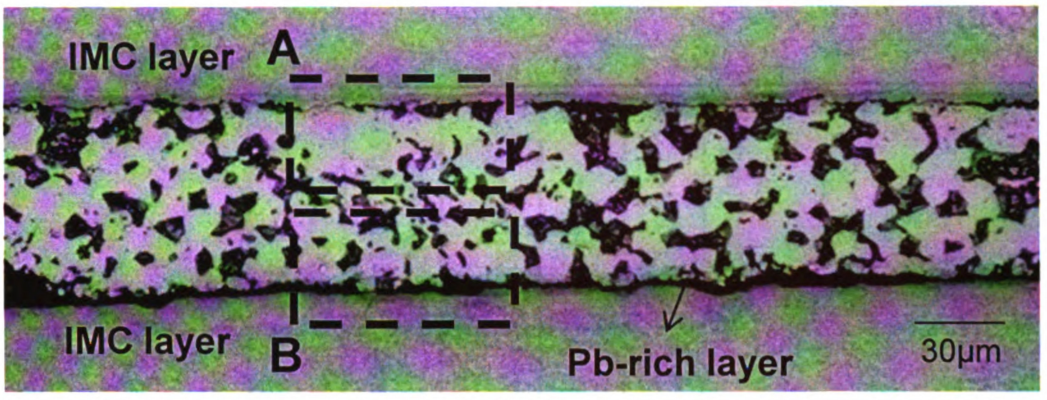


Figure 32a. The image of solder joint isothermally aged at 100 °C for 15 days and subjected to current stressing for 20 days at 100 °C. The enlarged picture of regions A and B are given in Figure 20b.

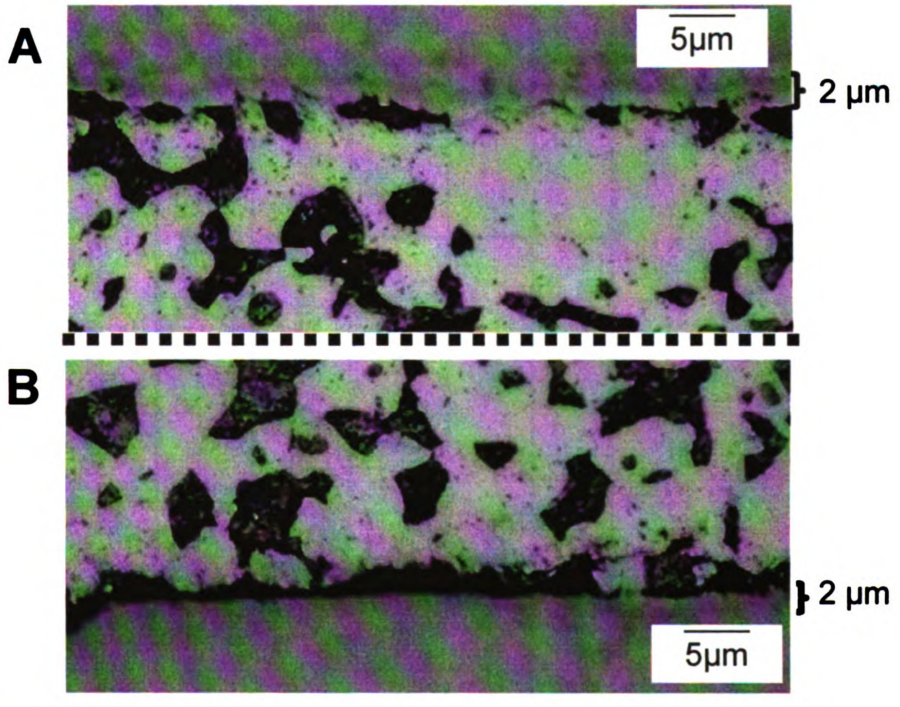


Figure 32b. In region s A and B, solder/substrate IMC layers are both about 2 μm thick.

Table 2. Thickness of IMC layer in specimen aged at 100 °C.

	Before EM (20 days @ 100 °C)		After EM (20 days @ 100 °C)	
	Region A (μm)	Region B (μm)	Region A(μm) Cathode	Region B(μm) Anode
As-reflowed	<1*	<1*	1 (Cu_6Sn_5<Cu_3Sn)	1*
12-days coarsening	1~2*	1~2*	2~3*	2~3*
15-days coarsening	1~2*	1~2*	2~3*	2~3*

*Cu_6Sn_5>Cu_3Sn

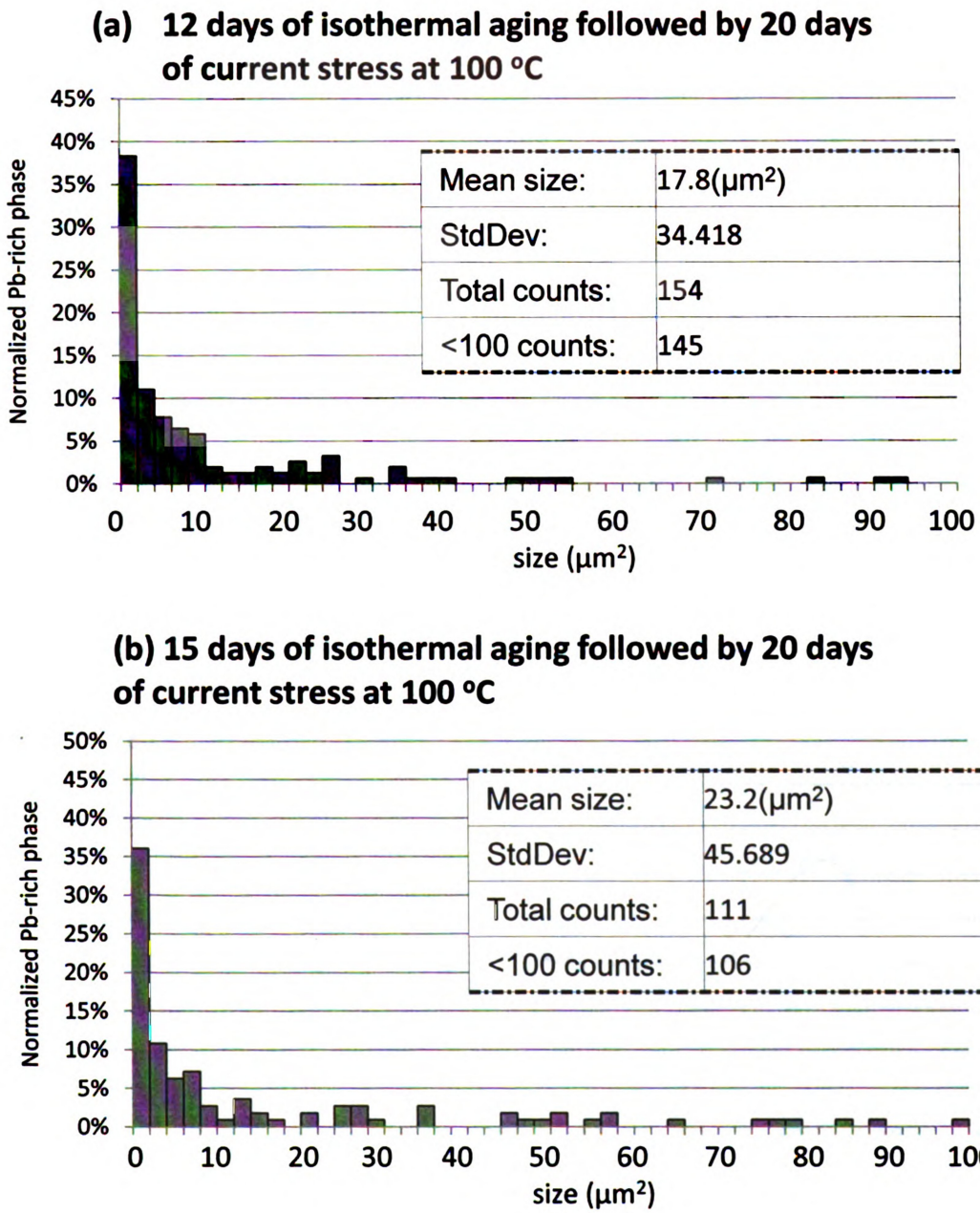


Figure 33. Size distribution of Pb-rich phase for (a) joint isothermally aged for 12 days at 100 °C and subjected to current stressing for 20 days at 100 °C (b) joint isothermally aged for 15 days at 100 °C and subjected to current stressing for 20 days at 100 °C.

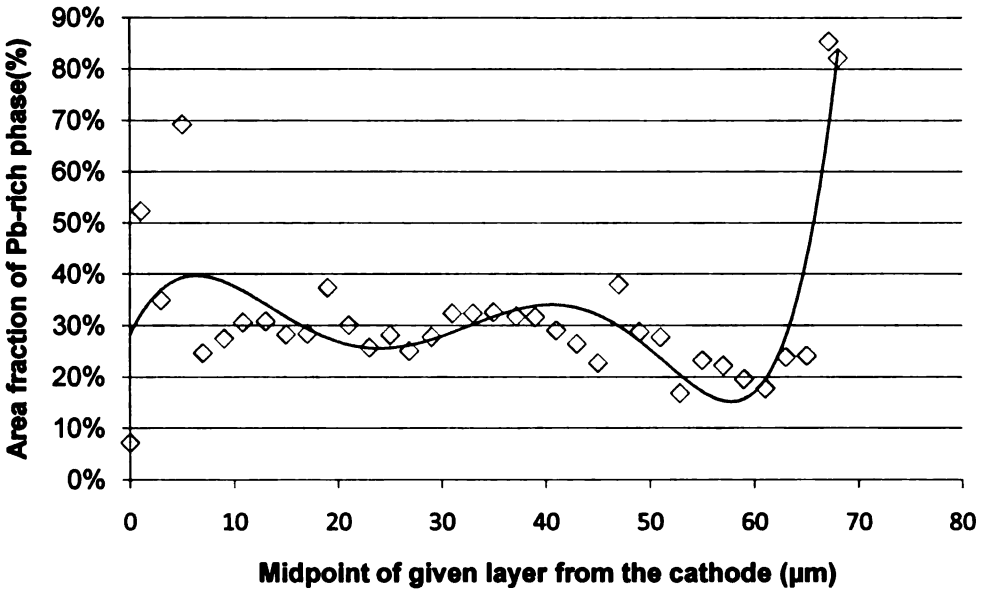


Figure 34a. Area fraction of Pb-rich phase for joint isothermally aged for 12 days at 100 °C and subjected to current stressing for 20 days at 100 °C.

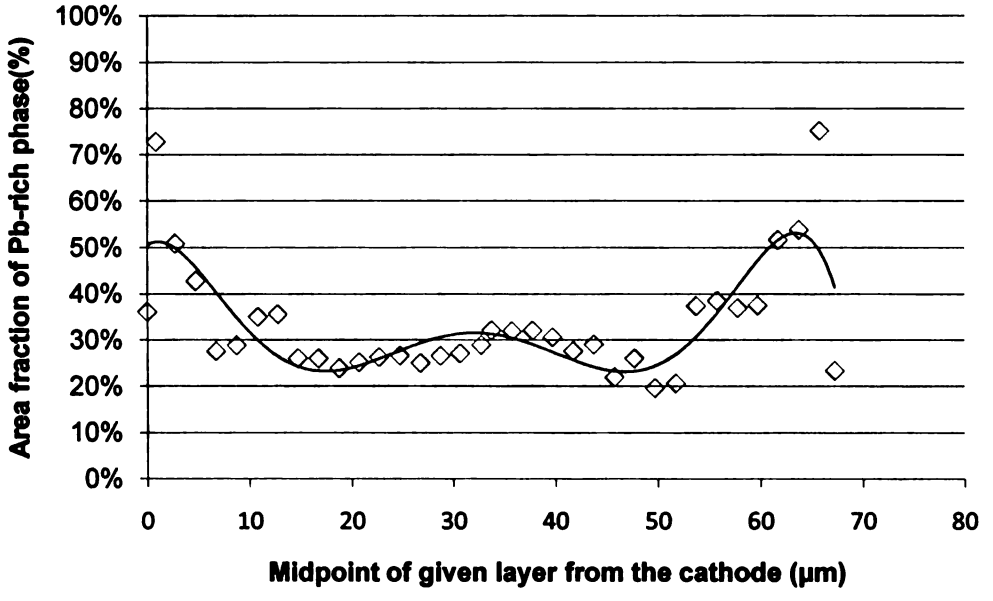


Figure 34b. Area fraction of Pb-rich phase for joint isothermally aged for 15 days at 100 °C and subjected to current stressing for 20 days at 100 °C.

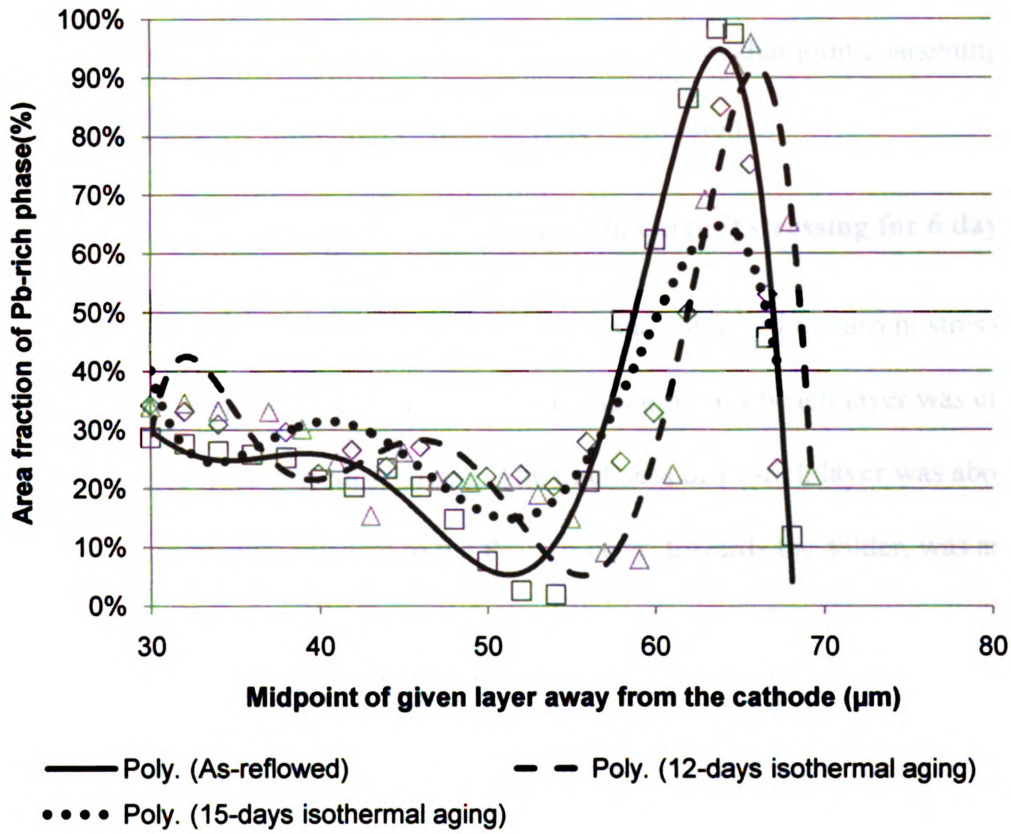


Figure 35. Accumulation of Pb-rich phase near anode using image taken by 50X objective lenses . Comparison of specimens with extents of coarsened microstructures subjected to current stressing for 20 days at 100 °C.

ii. Current stressing on specimen aged for 6 days at 150°C

SEM observations, the joint coarsened for 6 days subjected to current stressing for 6 days at 150°C is shown in Figure 24. As compared with the joint without isothermal aging subjected to similar current stressing conditions (Figure 14), no serious valley/hillock formation was found in Figure 24. This suggests that joint coarsening for 6 days at 150°C inhibits the formation of hillock/valley formation.

a) Joint coarsened for 3 days at 150°C subjected to current stressing for 6 days

The results of joint coarsened for 3 days at 150°C and subjected to current stressing for 6 days at 150°C is shown in Figure 25. An accumulation of Pb-rich layer was clearly observed near anode from current stressing. The thickness of Pb-rich layer was about 6 μm. As the result indicates, adjacent to the Pb-rich layer, towards the solder, was an Sn-rich layer followed by a random mixture of Sn-rich and Pb-rich. The two-layer segregation of Pb-rich and Sn-rich phases is not as obvious as Figure 16 (joint without coarsening). This suggests that area distribution of Pb-rich and Sn-rich phases is more random if the joint is coarsened for 3 days at 150°C prior to current stressing. Additionally, fewer Cu_6Sn_5 regions were found in the coarsened joint than in the joint without coarsening. Last but not least, the interfacial Cu-Sn IMC layer at both interfaces had a thickness of about 6 μm.

b) Joint coarsened for 6 days at 150°C subjected to current stressing for 6 days

The interior microstructures evolution of the solder joint coarsened for 6 days subjected to current stressing for 6 days is shown in Figure 26. Comparing to the as-

reflowed solder joint subjected to current stressing (as shown in Figure 16),one can note that the Pb-rich phases was more randomly distributed on the surface of solder. The accumulation of Pb-rich layer in thickness is reduced to 5 μm in joint coarsened for 6 days at 150°C. As the result indicates, no significant two-layer segregation of Pb-rich and Sn-rich layers was observed. Additionally, fewer Cu_6Sn_5 particles were observed within the solder matrix and the interfacial Cu-Sn IMC layer at both interfaces had a thickness of about 6 μm.

a. Characteristic of intermetallic compound

The thickness of solder/substrate interface IMC layers for different experimental conditions at 150°C is shown in Table 2. Three interesting points should be mentioned. First, the thickness of IMC layer is asymmetric for joint without isothermal aging subjected to current stressing at 150°C. However, it is symmetric for pre-aged solder joints. Second, for as-reflowed solder joints subjected to current stressing, the thickness of Cu_6Sn_5 near cathode is smaller than the thickness of Cu_3Sn near the cathode. However, in the specimen with coarser microstructure subjected to current stressing, the thickness of Cu_6Sn_5 layer near cathode is larger than the thickness of Cu_3Sn layer near the cathode. Last but not least, one can note that the overall thickness of solder/substrate interface IMC layer result in 150°C is greater than in 100°C.

b. Size distribution of Pb-rich phase within the solder joint

Size distribution of Pb-rich phase within the solder joint for coarser microstructure subjected to current stressing for 6 days at 150°C is shown in Figure 27. Two interesting points should be noted here. First, the mean size of Pb-rich phases within

solder joint is coarsened due to current stressing and the extent of coarsening is reduced if the joint was pre-aged. For example, in the as-reflowed solder joint the size of this phase increased from 3.9 μm^2 to 55.7 μm^2 and in sample that had 6-days isothermal aging solder joint the increase is from 33.2 μm^2 to 40.7 μm^2. In other words, the effect of isothermal aging prior to current stressing hinders the growth of mean size of Pb-rich phase while current stressing. Second, the difference in sized of each individual Pb-rich phase after 6-days of current stressing is reduced with increased extents of coarsening.

c. Area fraction of Pb-rich phase between two Cu substrate

The results of area fraction of Pb-rich phase occupied in each selected region (220*2 μm^2) layer by layer for joints exposed to current stressing at 150°C is shown Figure17 and Figure 28a-b. The results indicate that after electromigration for 6 days at 150°C, whether the microstructure was coarsened or not, the concentration of Pb-rich phase near anode is higher than near the cathode, which indicates Pb-rich phase was accumulated at the anode. In other words, electromigration results in Pb-rich accumulation near the anode. However, the segregation of Pb-rich phase and Sn-rich phase is more significant for as-reflowed solder joint than isothermally aged. In Figure 17, there is a drop at the position of 43 μm away from the cathode, which indicates Pb-rich phase is hardly found in this layer. In other words, this layer is Sn-rich layer. On the other hand, one cannot find any drop in coarsened microstructure as shown in Figure 28b. This observation indicates the distribution of Pb-rich phase and Sn-rich phase is more random after current stressing starting with coarser microstructure.

Additionally, for the purpose of focusing on quantification of Pb-rich phase accumulation near anode, methods described in experimental procedure 3.2 p.25 was used. The area fraction of Pb-rich phase vs. distance away from the cathode is shown in Figure 29. Few interesting points should be noted. First, isothermal aging of solder joints after current stressing shows less segregation of Pb-rich and Sn-rich than in as-reflowed solder joints. As the result indicates, the area fraction of Pb-rich phase for specimens with fine microstructure after current stressing is around 10 % in the intermediate region of solder joints and 30% for coarser microstructure. This shows the area fraction of Pb-rich phase is relatively uniform for coarser microstructure subjected to current stressing. Second, the thickness of Pb-rich accumulation layer for as-reflowed solder joints is thicker than pre-aged solder joints. As the result indicates, at 50 μm away from the cathode, the percentage of Pb-rich phases for the joint without coarsening remains at 95 % for about 10 μm, which indicates that the thickness of Pb-rich accumulation is about 10 μm. On the other hand, for the joints coarsened for 6 days and subjected to current stressing for 6 days, area fraction of Pb-rich phase is more than 95%. Besides, the distance of high area fraction of Pb-rich is relatively shorter than as-reflowed solder joints, indicating the Pb-rich accumulation layer is thinner. In addition, the area fraction of Pb-rich phase reach 100% for as reflowed solder joints subjected to current stressing, indicating that there is a continuous layer of Pb-rich phase near anode. However, no such continuous layer was found for pre-aging solder joints.

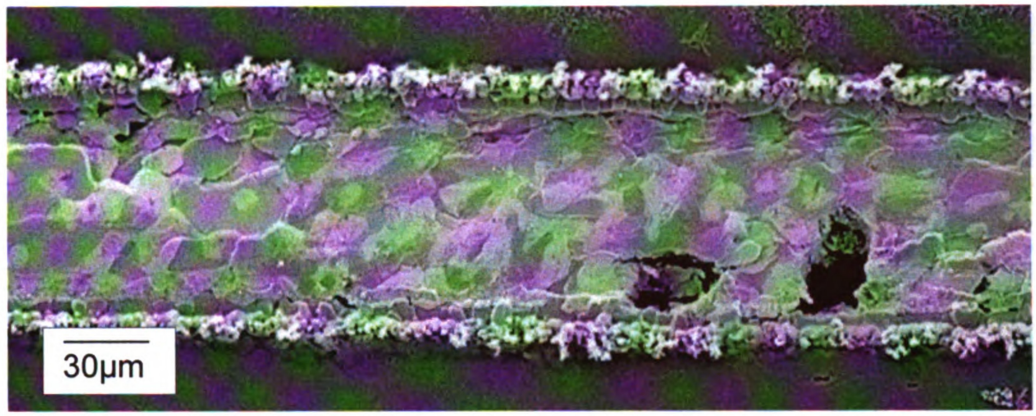


Figure 36a. The overview SEM image of joint coarsened for 6 days at 150°C and subjected to current stressing for 6 days at 150°C.

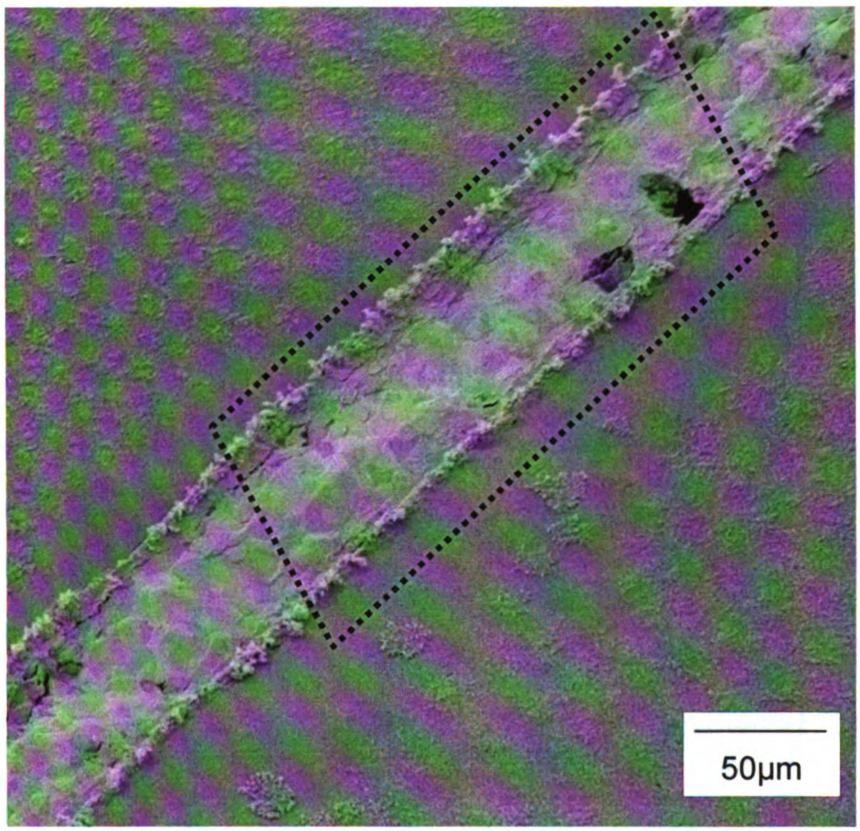


Figure 36b. Joint coarsened for 6 days at 150°C and subjected to current stressing for 6 days at 150°C. Joint was tilted by 45°. The dotted area is the same region as in Figure 24a. No hillock/valley formation noted.

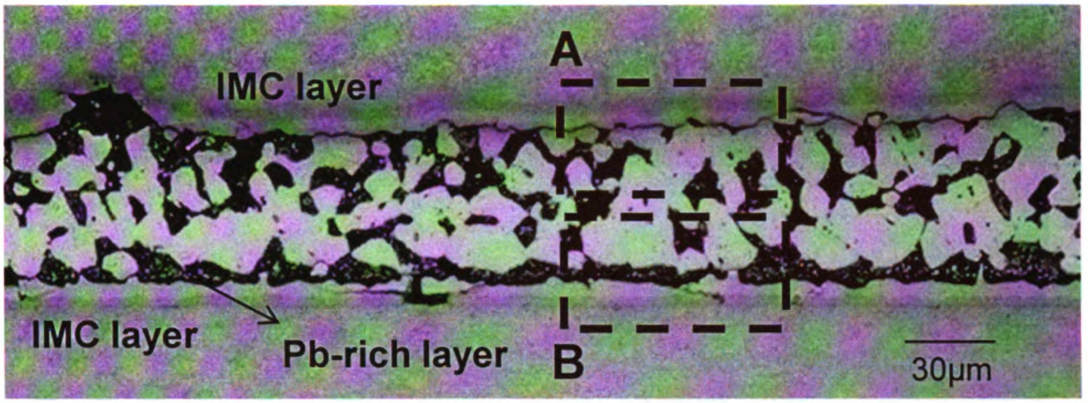


Figure 37a. The image of solder joint isothermally aged at 150 °C for 3 days subjected to current stressing for 6 days at 150 °C. The enlarged picture of regions A and B are shown in Figure 25b.

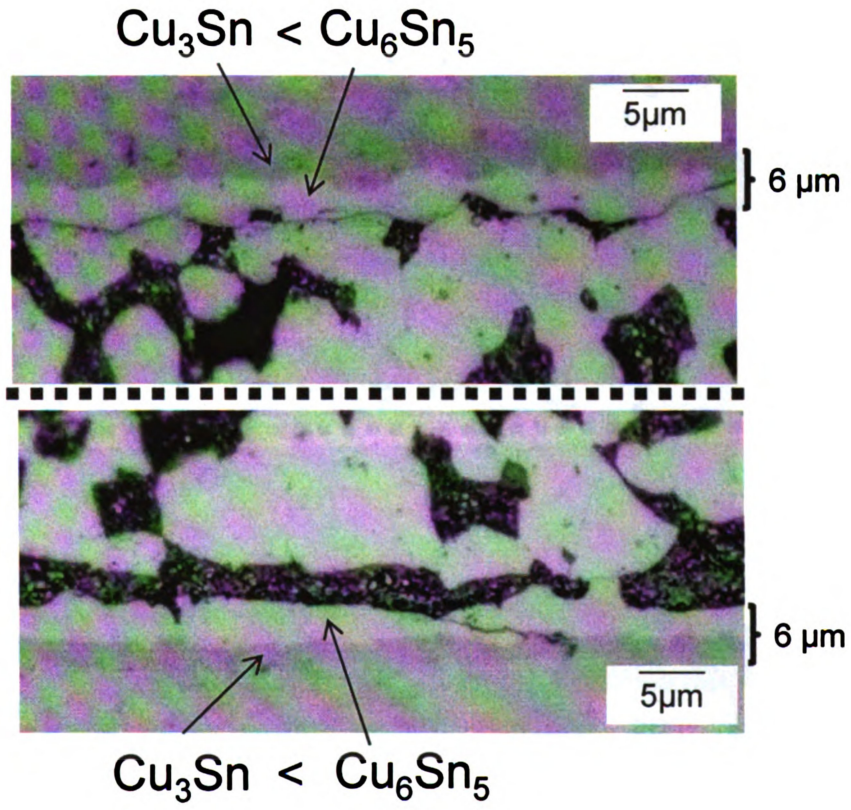


Figure 37b. In regions A and B, IMC layers are both about 6 μm thick. The thickness of Cu_3Sn layer is thinner than Cu_6Sn_5 layer in both regions.

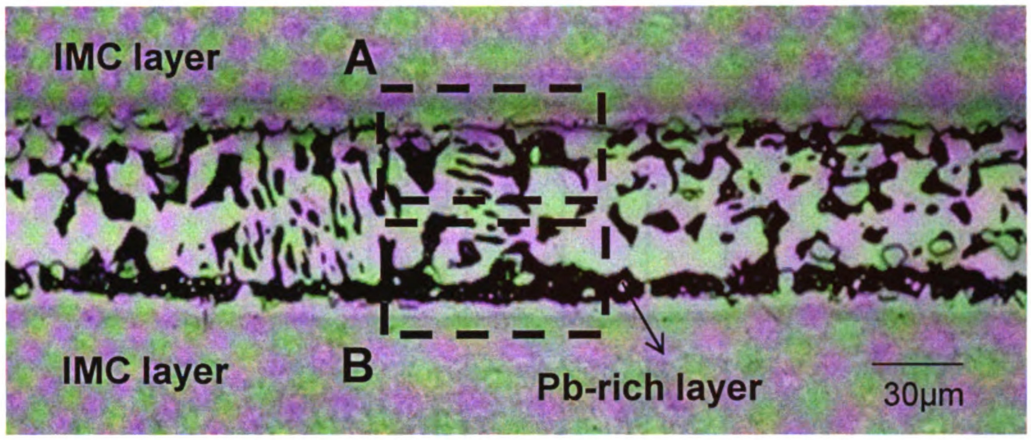


Figure 38a. The image of solder joint isothermally aged at 150 °C for 6 days and subjected to current stressing for 6 days at 150 °C. The enlarged picture of regions A and B are shown in Figure 26b.

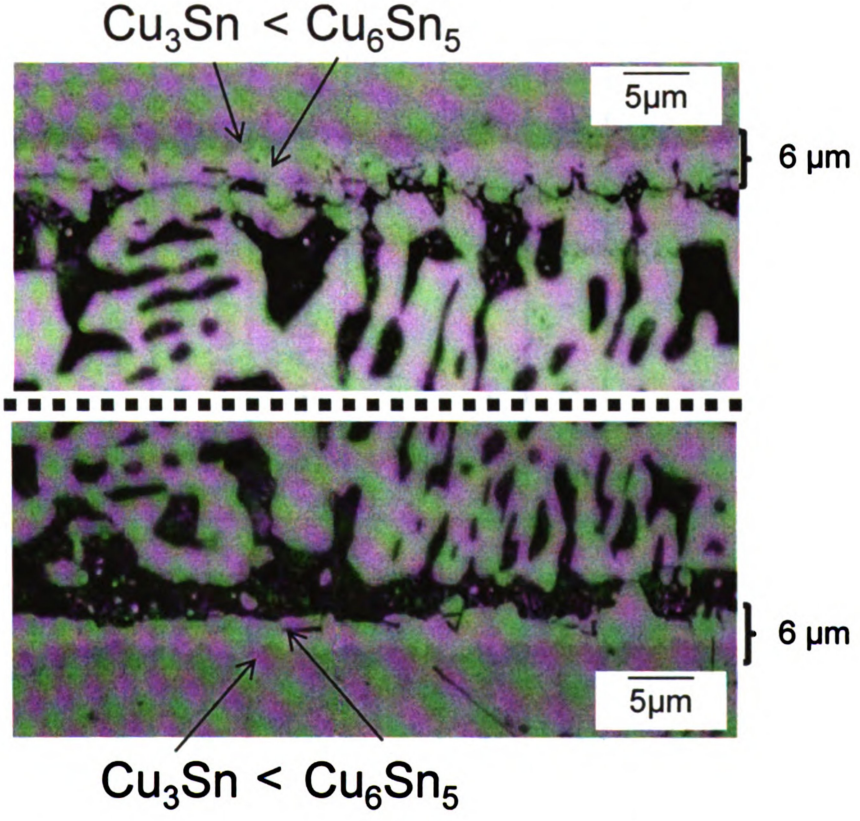


Figure 38b. In region s A and B, IMC layer are about 6 μm thick. The thickness of Cu_3Sn layer is thinner than Cu_6Sn_5 layer in both regions.

Table 3. Thickness of IMC layer in specimen aged at 150 °C.

	Before EM (6 days @ 150 °C)		After EM (6 days @ 150 °C)	
	Region A (μm)	Region B (μm)	Region A(μm) Cathode	Region B(μm) Anode
As-reflowed	<1*	<1*	4 (Cu_6Sn_5<Cu_3Sn)	6*
3-days coarsening	4*	4*	6*	6*
6-days coarsening	5*	5*	6*	6*

*Cu_6Sn_5>Cu_3Sn

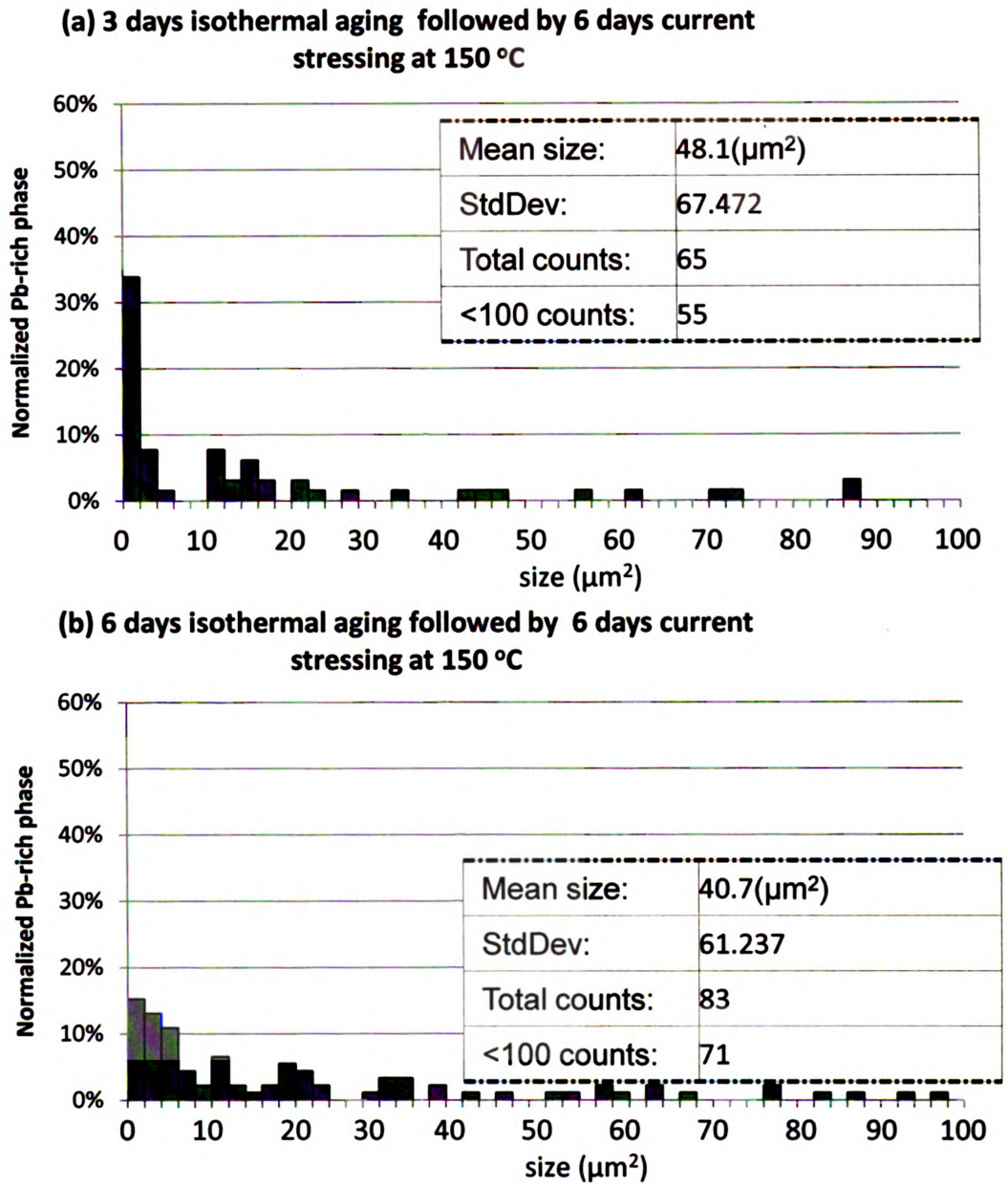


Figure 39. Size distribution of Pb-rich phase for (a) joint isothermally aged for 3 days at 150 °C and subjected to current stressing for 6 days at 150 °C (b) joint isothermally aged for 6 days at 150 °C and subjected to current stressing for 6 days at 150 °C.

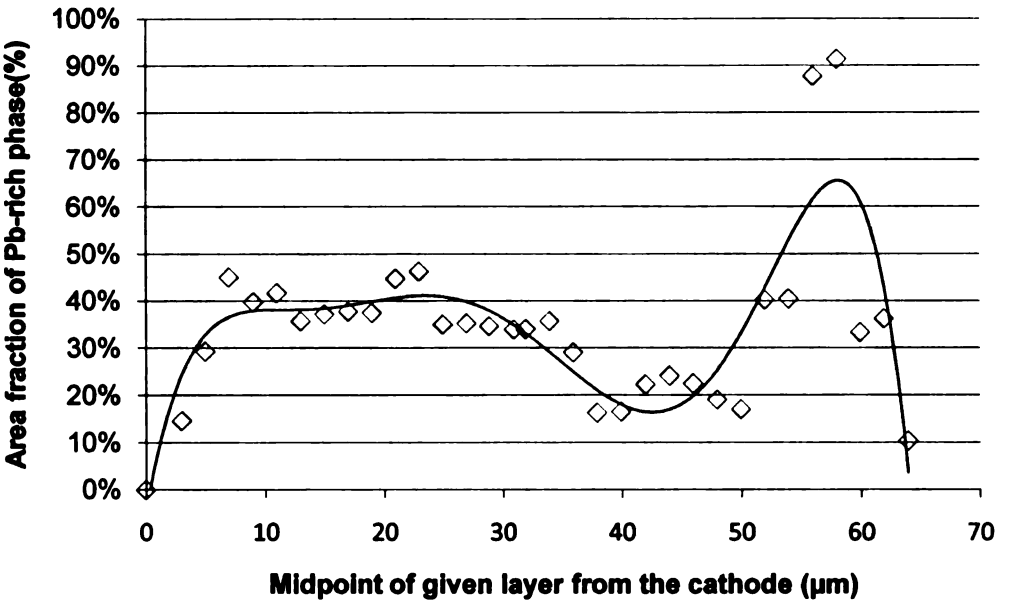


Figure 40a. Area fraction of Pb-rich phase for joint isothermally aged for 3 days at 150 °C and subjected to current stressing for 6 days at 150 °C.

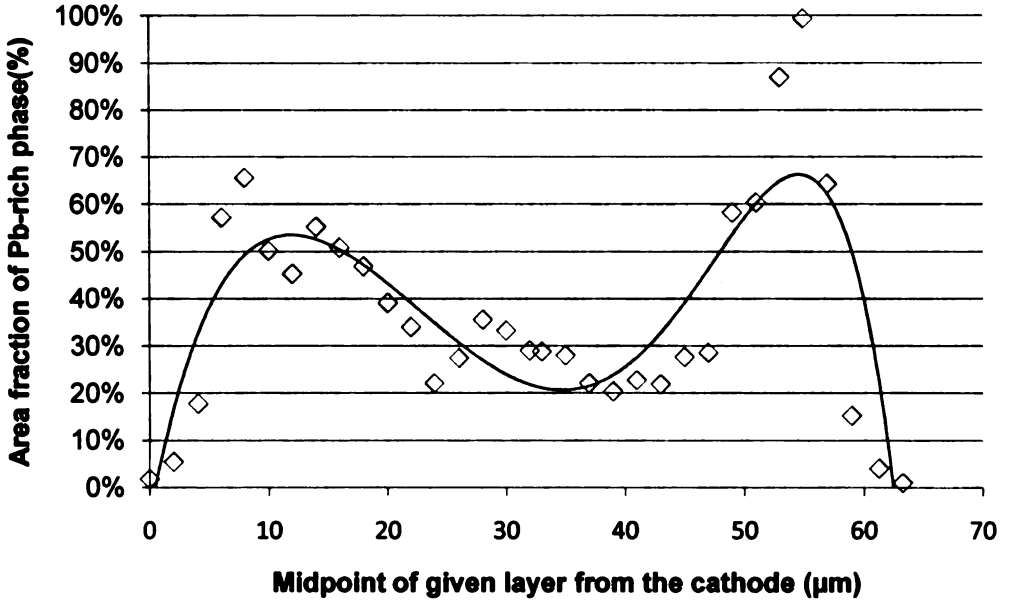


Figure 40b. Area fraction of Pb-rich phase for joint isothermally aged for 6 days at 150°C and subjected to current stressing for 6 days at 150°C.

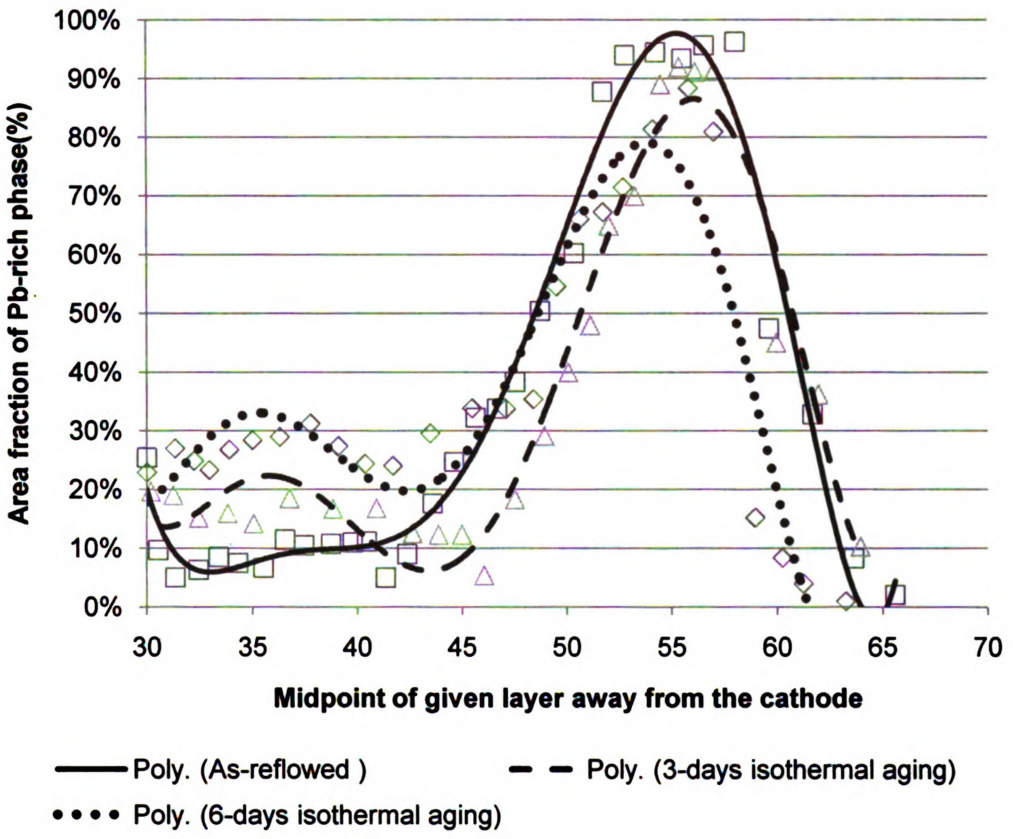


Figure 41. Pb-rich phase accumulation at anode region using image taken by 50X objective lenses . Comparison of specimen with different extents of coarsening subjected to current stressing for 6 days at 150°C.

d. Summary and discussion

Most important of all, the effect of coarsened microstructure on electromigration is investigated in this study. By controlling the annealing conditions, solder joints with various extent of coarsened microstructures can be fabricated. As compared with as-reflowed solder joint subjected to current stressing, several interesting points are discussed. First, coarsened microstructure results in less Pb-rich accumulation at the anode. Second, coarsened microstructure results in more uniform distribution of Pb-rich phases between the cathode and the anode. Last but not least, coarsened microstructure leads to more symmetric growth of Cu-Sn IMC layers at the interfaces.

a) Coarsened microstructure results in less Pb-rich accumulation at the anode

After electromigration with current density of 10^4 Amp/cm^2 on the coarsened microstructure, Pb is driven in the direction of electron flow from the cathode to the anode. However, unlike the as-reflowed solder joints, coarsened Pb-rich phase has less grain boundary between phases. So, it results in less Pb-rich accumulation at the anode.

b) Coarsened microstructure results in more uniform distribution of Pb-rich phases between the cathode and the anode

The domains of Pb-rich and Sn-rich phase were still distributed randomly, except for the fact that they had coarsened to different extents with time. The microstructural evolution in the solder region looks as if the solder joints experience an isothermal aging treatment without current stressing.

c) Coarsened microstructure leads to more symmetric growth of Cu-Sn IMC layers at the interfaces

After electromigration with a current density of 10^4 Amp/cm^2 on the specimen with coarsened microstructure, not only Pb, but also Sn is driven in the same direction of electron flow from the cathode to the anode. However, coarsened microstructure has less grain boundary. So, less Sn is pushed to the anode as compared to the as-reflowed solder joint. As a result, the growth of interface IMC layers at the anode is almost the same as the growth of IMC layers at the cathode. The microstructural evolution at the interface looks the same when the joints are subjected to isothermal aging treatment only. In other words, the atomic movements during electromigration in specimens with coarser microstructure in the solder region are not as fast as that in specimen with fine microstructure.

4. SUMMARY

In summary, isothermal aging solder joints results in coarsened microstructure. Coarsened microstructure has less interfacial area between phases. Regardless of temperature, electromigration on specimen with more coarsened microstructure shows less accumulation of Pb-rich phase at the anode. This suggests that the atomic movement during current stressing at 100 °C and 150 °C is not only through lattice diffusion but also through grain boundary diffusion. Moreover, this finding also suggests that the electromigration of Cu/eutectic Pb-Sn/Cu solder joints can be inhibited significantly by appropriate pre-aging treatment of solder joints.

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