HIGH PERFORMANCE CONTROL OF INVERTER INTERFACED DISTRIBUTED GENERATION

by

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ABSTRACT

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As a new means of power generation, distributed generation (DG) based on renewable energy source is experiencing a rapid development. All the power generated by each DG in the micro-grid must use an electric inverter to interface with the power system. Basically, the microgrid inverter has two operation modes: grid-connected mode and standalone mode. For standalone operation mode, a multi-loop controller is proposed. The voltage differential feedback inner loop is embedded in the outer voltage loop. Also an output voltage decoupling and current decoupling are implemented by only using the output voltage feedback. The proposed control scheme possesses very fast dynamic response at load step change and can also achieve good steady state performance at both linear and nonlinear loads. For grid-connected operation mode, it is demonstrated that the possible grid-impedance variations have a significant influence on the system stability when conventional proportional-integrator (PI) controller is used. To deal with this stability problem, an H∞ controller with the explicit robustness in terms of grid-impedance variations is proposed.. For the transition from grid-connected mode to standalone mode, this thesis proposes the voltage based and current control based algorithms which can force the current to decrease to zero at a short time thus provide seamless transfers between two modes, avoiding the temporarily uncontrolled output voltage. Finally, the thesis analyzes the transient characteristics of the voltage and proposes an intelligent load shedding scheme which can detect the grid outage fast and do the load shedding accurately to avoid the distortion in the transition. All the proposed controllers and control algorithms in this work are extensively tested and verified through experiments.

Dedicated to:
My parents, Chuping Lei and Airong Wang
And my husband Junjun Xin

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CHAPTER 1 . INTRODUCTION

1.1 The microgrid concept

In the last few years, the traditional power system witnessed an evolutional change in the conventional centralized operation due to the emergency of smaller generating systems, such as microturbines, connected to the medium voltage and low voltage distribution levels. This change has opened new opportunities for on-site power generation by electricity users. More recently, due to the economical, technological and environmental reasons, the concept of microgrid has gained popularity, which is a cluster of loads and micro-sources operating under a unified controller within a certain local area. This part will introduce the concept of microgrid, background technologies and its applications.

1.1.1. Microgrid concept

The concept of microgrid is proposed in [1], where is defined as a cluster of loads and micro-sources operating under a unified controller within a certain local area. the microgrid can thereby be understood as a cluster of loads and paralleled DG systems operating together. Being a systematic organization of DG systems, a microgrid has larger power capacity and more control flexibilities to fulfill system reliability and power quality requirement, in addition to all the inherited advantages of a single DG system. It also offers many opportunities for optimizing DG systems, such as CHP, premium power and peaking sharing to name a few.

1.1.1. Background technologies

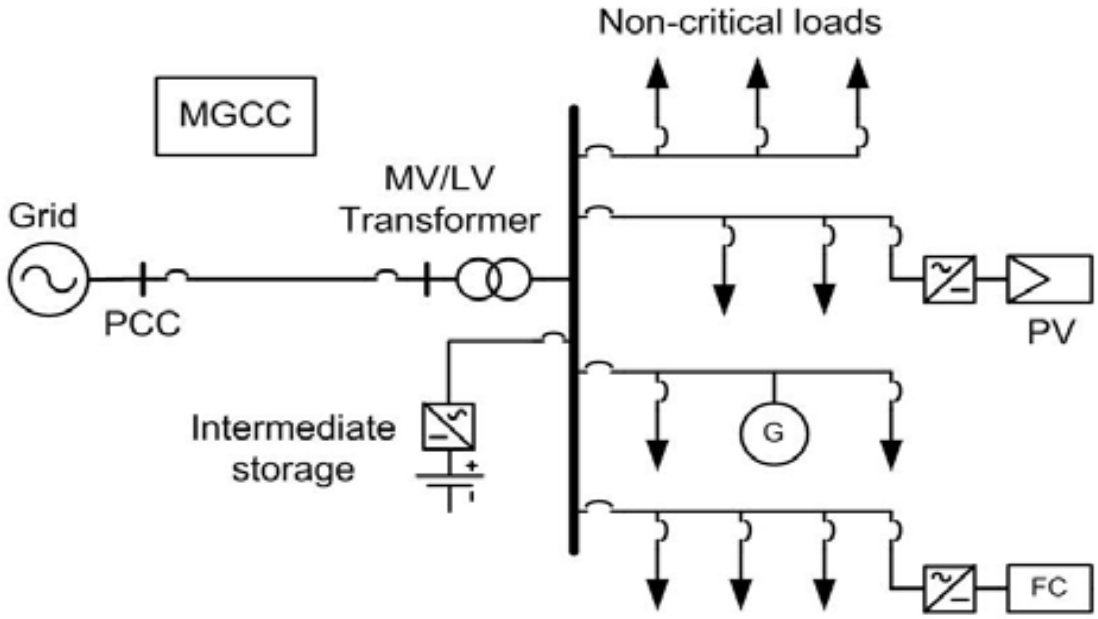


Fig. 1.1 Basic microgrid architecture

The background technologies for proper operation of a microgrid include generating technologies, storage technologies and control technology. A typical DG system based on micro-source depicted in illustrate that the micro-source generation involves all the generation, storage, interfacing and control technologies. A most distinguishing feature of the microgird is its power electronics interfaces as shown in Fig.1.1. All the power, DC or non-power frequency AC, generated by each DG in the microgrid must use an electric inverter to interface with the electrical power system. This power electronic interface provides significant flexibilities and permits the microgrid to function as a semi-automous power system. Control of the microgrid mainly refers to the control of the interfacing power electronic inverters, which is also the topic of this thesis.

1.2 The requirement and standard of the power electronics interface

There are two basic operation modes for grid-connected inverter as a distributed generation: (1) Grid-connected mode: it could provide the required power to the grid continuously, and also could store the energy and then compensate the grid in the peak time. (2) Standalone mode: it could support the local load independently when the grid has some fault. Therefore,

the grid-connected inverter should satisfy different requirements and standards in different operation modes.

1.2.1. Grid-connected operation mode

As the development of microgrid, more and more distributed generations are connected to the grid. IEEE std 1547-2003 (IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems) is the first standard of grid connected inverter with fuel cell, photovoltaic, energy storage as the front stage. This standard includes response to the grid fault, power quality, islanding, protection, testing and so on. Several important standards will be explained as follows:

1. The response to the grid voltage abnormity

When the inverter operates in grid-connected mode, the normal range of grid voltage is within 88% and 110% of the standard voltage. When the grid voltage exceeds this limit, the inverter system should detect this fault and disconnects with the grid in a required short time.

Table 1-1.The response time to the abnormal voltage

Voltage range	Response time (utility cycle)
Vrms<50%	6
50%<Vrms<88%	120
88%<Vrms<110%	Normal operation
110%<Vrms<120%	120
Vrms>120%	6

2. Response to the grid frequency abnormity

In IEEE Std 1547-2003, the normal range of frequency is within 59.3~60.5 Hz. This range also changes with the power rating. The details of response time to different

Table 1-2.The response time to grid frequency abnormity

Capacity of the Distributed Generation (KW)	Frequency range (Hz)	Response time (s)
<=30	<59.3	0.16
	>60.5	0.16
>30	<57.0	0.16
	<(57.0~59.8)	0.16~300
	>60.5	0.16

3. The requirement for the current harmonic that injected to the grid

The standard requires that the percentage of DC component over the AC component of the injected current should not exceed 0.5%. The requirement for other harmonics are shown in Table 1-3.

Table 1-3.The standard for the harmonics of injected current

Harmonic order	h<11	11<=h<=17	17<=h<=23	23<=h<=35	35<=h	THD
%	4.0	2.0	1.5	0.6	0.3	5.0

1.2.2. Standalone operation mode

The grid-connected inverter not only can provide power to the grid, can also provide the power to the local load. When the grid abnormity happens, the grid-connected inverter will disconnect with the grid and switch to standalone operation mode to provide local load. The corresponding standard for standalone operation is IEEE Standard 446-1995 (IEEE Recommended Practice for Emergency and Standby Power Systems for Industrial and Commercial Applications). The main points are:

(1) Security. This is the basic requirement for the grid-connected inverter as a back-up supply

to the load. The ground connection is an important factor, which is described in IEEE Std 142-1991 (ANSI) IEEE Recommended Practice for Grounding of Industrial and Commercial Power Systems.

(2) Power quality. This includes the voltage amplitude, waveform quality, frequency and dynamic response, system EMC and so on.

1.3 The basic topologies of the interface between distributed generation and grid

Grid-connected inverter plays the role of the interface between the renewable energy source or other distributed generation source and the grid, in order to best utilize the power and converter the voltage to the requirement voltage. Many topologies are proposed for this application. According to the structure, there are single stage, double stage and multi-stage. According to the isolation, it can be divided into isolated and non-isolated. According to the source, it can be classified into voltage source inverter and current source inverter, single-phase or three-phase. Paper [2-5] summarizes the present circuit topologies. The main topologies will be described here also.

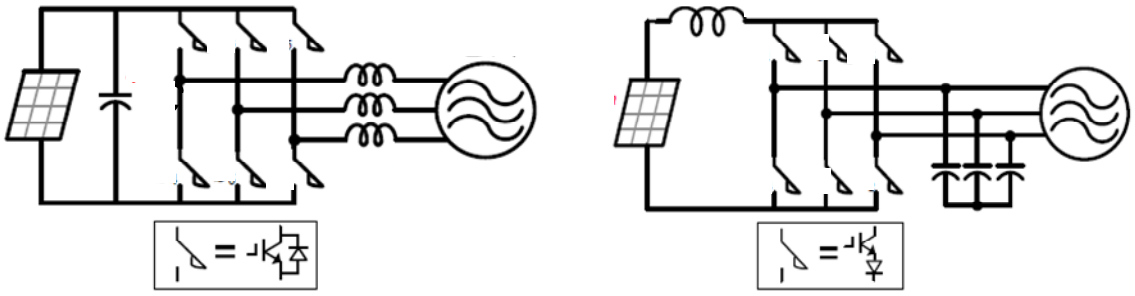


Fig.1.2 (a) Conventional voltage source inverter (b) Conventional current source inverter

Fig.1.2 shows the conventional three phase voltage source inverter (VSI), which is a buck converter. There are also other topologies like single phase or half bridge. This topology has simple structure, high efficiency and reliable gate drive system and control strategy. It can also be used for harmonic compensation and reactive power compensation. However, it also

also be used for harmonic compensation and reactive power compensation. However, it also has some drawbacks as follows: (1) the input dc voltage is relatively high, thus it is hard to use it with low voltage power source such as fuel cell, TEG and PV systems. (2) In PV or fuel cell system, the input voltage has a relatively wide range. This single stage has no voltage boost front-stage. So it needs a big power rating to satisfy a wide range of operation points. [8]

Different from VSI, conventional current source inverter (CSI) is a boost converter and its output voltage line to line peak value is bigger than the input dc voltage. Its basic circuit topology is shown in Fig.1.2 (b). It can implement voltage boost and inverter function at the same time. Thus it is suitable for the PV and fuel cell application. But the switch in the CSI has to have voltage reverse blocking capability. The conventional methods use a IGBT in series with a diode to implement this function. It has high conduction loss and high leakage inductance between these two discrete components. However, the recently developed Reverse-Blocking IGBT (R-B IGBT) overcomes this problem and promotes the development of current source inverter. The main drawbacks of CSI is: (1) it can only have uni-direction power flow (2) it only has voltage boost function thus also increase its total power rating when the input voltage changes in a large range.

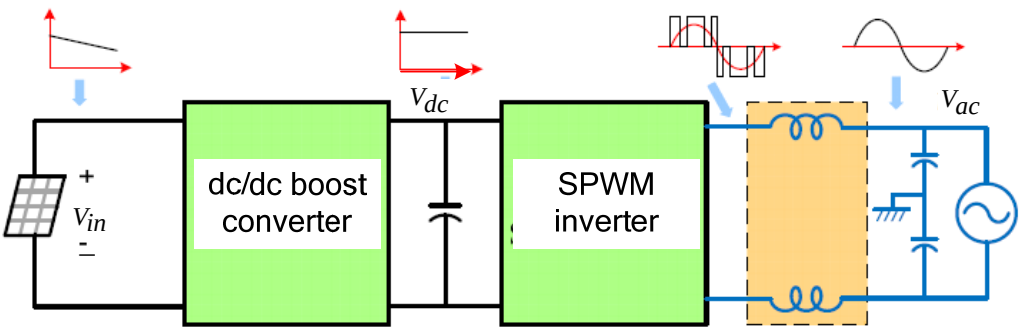


Fig.1.3. Two stage power conditioner (dc-dc boost and dc-ac inverter)

(interpretation of the references to color in this and all other figures, the reader is referred to the electronic version of this thesis.)

Fig.1.3 shows another widely used two stage power conditioner (dc-dc boost and SPWM dc-ac inverter). The front stage dc-dc boost can boost the voltage to the required a constant high voltage for the grid-connected inverter DC link when the input voltage varies in a large range, therefore it reduces the power rating for the inverter.

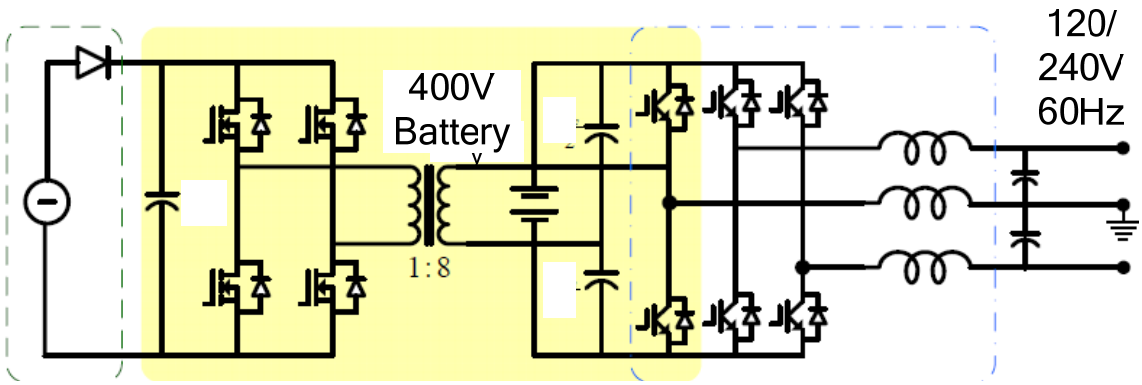


Fig.1.4. Two stage power conditioner (dc-dc full bridge converter and dc-ac PWM inverter)

For the two stage configuration, the front stage can also be replaced by half bridge, full bridge, or other dc-dc converter. Paper [6] applied a full bridge with an isolated high frequency transformer as a front stage for fuel cell application as shown in Fig.1.4. It uses a high frequency transformer to boost the voltage to a higher level and also used a voltage doubler in the inverter side to additionally boost the voltage. The rectifier side uses active switch to replace the diode, thus make the system more flexible and also guarantees the bidirectional power flow function. The details can also be found in [7-8].

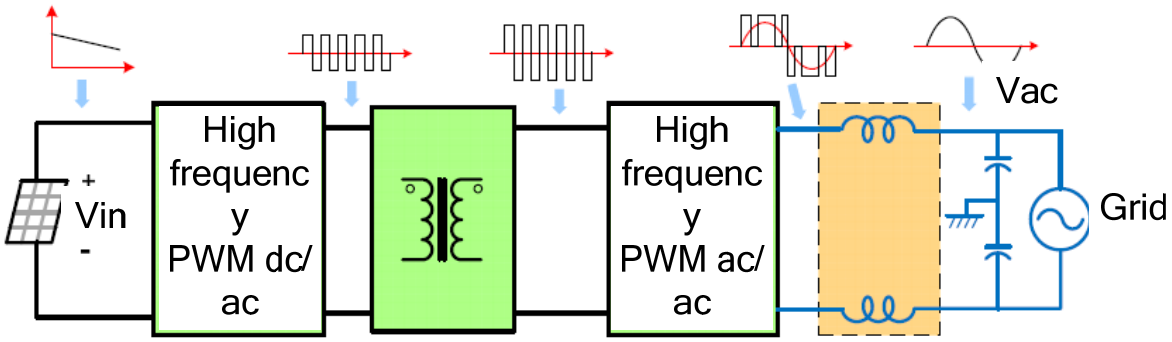


Fig.1.5. Two stage power conditioner (high frequency dc-ac inverter and high frequency ac-ac

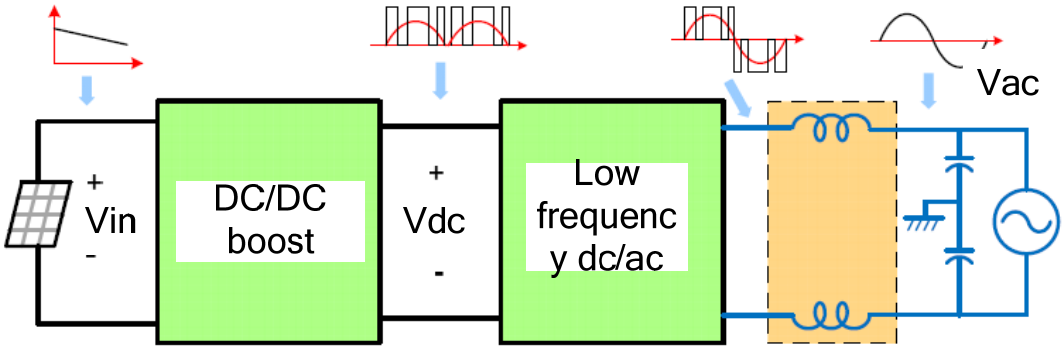


Fig.1.6.Two stage power conditioner (dc-dc boost converter and low frequency dc-ac inverter)

Another choice for the second stage of Fig.1.3 is to use ac-ac converter to replace the rectifier and inverter stage, as shown in Fig.1.5. The dc voltage is transformed into high frequency ac voltage by the inverter at the front stage, then the transformer is used to boost the ac voltage, finally the ac/ac converter is used to transform the high frequency ac voltage into utility frequency [9].

Another method for two stage topology is to use the dc-dc voltage to transform the dc voltage into high frequency PWM dc voltage and use the low frequency dc/ac inverter as the second stage to just transform the half-wave dc voltage into the full wave, as shown in Fig.1.6. This method can reduce the switching loss thus increase system efficiency. Also it deletes the big DC-link capacitor from the system thus reduce the cost.

1.4 Control strategies of the micro-grid inverter [10]

unity power factor).

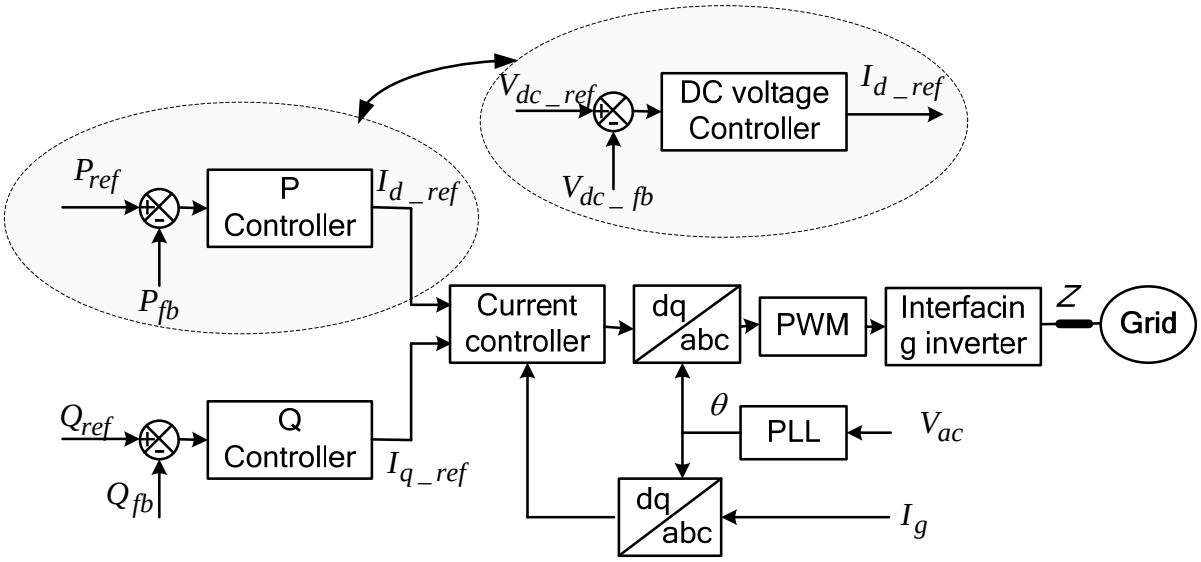


Fig.1.8. Grid-connected real and reactive power control scheme through output **current** regulation.

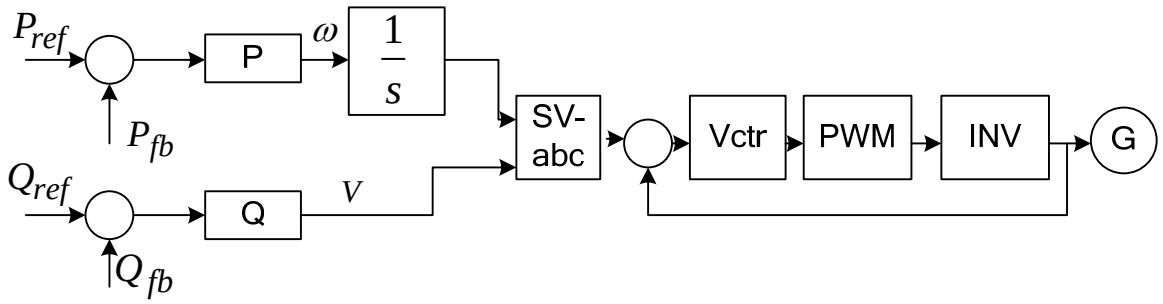


Fig. 1.9. Real and reactive power control through voltage regulation in grid-connected mode

In grid connected mode, the main target for the inverter control is to control the power injected into the grid. The power command can be generated by the micro-grid management system or the maximum power tracking system. When the reactive power command is zero, the output current and voltage are in phase with each other, the unity power factor is obtained. Generally, there are two ways to control the power: through output voltage regulation; through output current regulation.

1.4.1 Power control through current regulation

Fig.1.7 shows the real power control through current regulation. If both real and reactive power flow control is desired, the real power control loop can be used to produce the

In grid connected mode, the main target for the inverter control is to control the power injected into the grid. The power command can be generated by the micro-grid management system or the maximum power tracking system. When the reactive power command is zero, the output current and voltage are in phase with each other, the unity power factor is obtained. Generally, there are two ways to control the power: through output voltage regulation; through output current regulation.

1.4.1 Power control through current regulation

Fig.1.7 shows the real power control through current regulation. If both real and reactive power flow control is desired, the real power control loop can be used to produce the synchronous frame d-axis reference current (same as the current magnitude generation in) and the reactive power control loop can be employed to produce the q-axis current [11], as shown in Fig.1.8. The synchronous d-q frame current can then be controlled in a closed loop manner as shown in Fig.1.8. Note that similar current control performance can also be obtained in stationary frame by transforming the d-q reference current into stationary frame and using P+Resonant current controller [12-14].

1.4.2 Power control through voltage regulation

Fig. 1.9 shows the real and reactive power control strategy through regulating the output voltage. When the line impedance between the inverter output and the PCC is $Z_L = R + jX$, the real and reactive power flow are:

$$P = \frac{V_1}{R^2 + X^2}[R(V_1 - V_g \cos\delta) + XV_g \sin\delta] \tag{1.1}$$

$$Q = \frac{V_1}{R^2 + X^2}[-RV_g \sin\delta + X(V_1 - V_g \cos\delta)] \tag{1.2}$$

V_1, V_g are voltage difference and δ is the angle difference. When the impedance is almost inductive, the δ is very small. It can be seen that the real power controller produces the reference output voltage phase angle while the reactive power controller generates the

reference voltage magnitude. The phase angle and magnitude are then transformed to the three-phase reference voltage. In Fig.1.9, a proportional controller are used for the real and reactive power controllers to realize the real power versus system frequency (P-ω) droop and the reactive power versus voltage magnitude (Q-V) droop characteristics [15-16]. However, to improve the reactive power control accuracy in grid-connected operation mode, integral control can be included into the reactive power controller [17-19]. The advantage of voltage regulated power control method is that it can be used in both standalone and grid-connected mode. However, it also has some drawbacks: Compared to the power control through current regulation, the voltage regulation method is more sensitive to the line impedance between the DG and the PCC. The small line impedance in the denominators of (1.1) and (1.2) will cause significant power flow even with a slight variation of the DG output voltage. Furthermore, the low X/R line impedance ratio at a low voltage microgrid can also cause real and reactive power control couplings if the DG unit is directly coupled to the microgrid without grid side inductor or transformer. This can be noticed from (1.1-1.2), where if the line impedance is not mainly inductive, the voltage magnitude and phase angle will have non-negligible effects on the real and reactive power flows respectively.

1.4.3 Islanding detection and load shedding [10]

The intentional islanding mode is very important for microgrids to continue to provide power to critical loads during power outage of the main grid. During the grid-connected operation, each DG system in a microgrid is usually operated with the power flow control in the presence of a stiff grid voltage as has been discussed. When the microgrid is disconnected from the mains grid, each DG unit has to detect this islanding situation and switch its control scheme from power control mode to voltage control mode and provide a constant voltage to local loads.

Besides the control mode difference, there are several other issues to be considered for

islanding operation, such as synchronization among the DG units, the power flow constraint due to the DG capacity, voltage/frequency variations and thermal constraints of the distribution feeders. The islanding operation is further complicated when considering the large variation of electrical distance between DG units even within a small geographical area.

There are various islanding detection methods proposed for DG systems [20]. Since the DGs are in power control mode when connected to the grid, any power imbalance between DG generation and load demand will result in voltage magnitude (and frequency) changes when islanding occurs, regardless of whether the power control is through current or voltage regulation. Although there will be a non detection zone (NDZ) with this voltage magnitude or frequency detection method if the power difference is too small, this NDZ can be eliminated by employing some additional detection algorithms (e.g grid impedance detection). While serving as good indications for islanding detection, the quick voltage and frequency variations lead to a serious concern: the microgrid would operate out of the allowable voltage or frequency range quickly after islanding occurs. To avoid this, intelligent load shedding algorithms need to be implemented in a microgrid system to make sure that the demand is within available generation by disconnecting some least important loads. This thesis proposes the intelligent islanding detection and load shedding algorithms in chapter 5.

1.5 Scope of the thesis

Based on the previous work on microgrid inverter, this thesis focuses on the following subjects:

Chapter 2 proposes a multi-loop controller with voltage differential feedback, and with output voltage decoupling and output current decoupling by only using the output voltage feedback. The proposed control scheme possesses very fast dynamic response at load step change and can also achieve good steady state performance at both linear and nonlinear loads. In addition, it only uses the output voltage as the feedback variable, which reduces the system complexity.

Chapter 3 first proposes a proportional-integrator (PI) current controller for the inverter grid-connected mode. Then it analyzes the stability problem of the grid-connected voltage source inverter (VSI) with LC filters, thus an H∞ controller with the explicit robustness in terms of grid-impedance variations is proposed to incorporate the desired tracking performance and the stability margin.

Chapter 4 proposes the voltage control based voltage amplitude regulation, instantaneous voltage regulation algorithms and current control based zero current regulation algorithms to implement the seamless transition from grid-connected mode to standalone mode.

Chapter 5 proposes an intelligent islanding detection method and a load shedding scheme based on the voltage characteristics in the transient, in order to fast detect the grid outage and switch the inverter from grid-connected mode to standalone mode.

Chapter 6 discusses the future work that needs to be done.

CHAPTER 2 . MULTI-LOOP CONTROL SCHEME FOR MICRO-GRID INVERTER STANDALONE OPERATION

2.1. Introduction

Voltage source inverters (VSIs) are now widely used in many grid applications to interface distributed generation (DG) systems (for instance photovoltaics, wind, fuel cells and microturbines) to the utility system. When the inverter operates in standalone mode, the micro-grid inverter performs like a voltage source to provide required voltage to the local load. A traditional average voltage feedback control could maintain a desirable steady-state rms output voltage, but their response to load step change is noticeably slow, and nonlinear loads could greatly distort the output waveform. Instantaneous voltage feedback control can have faster transient response, lower total harmonic distortion and better disturbance rejection capability because of the lower output impedance. There are many instantaneous controllers been presented recently. State feedback controllers show good performance but the duty cycle has to be calculated on a pulse-by-pulse basis [21-23]. The hysteresis-type controllers have variable and relatively high switching frequencies and the control variable error is twice of the hysteresis band [24-26]. Dead-beat control proposed in [27-28] can make the capacitor voltage exactly tracks the reference voltage with the accurate knowledge of the filter parameters. A discrete-time sliding mode control technique has also been used in inverter control due to its robustness and overshoot-free fast tracking capability, [29-31]. A predictive controller [32-33] can enhance the system stability limits but its performance [33] is also subject to the accuracy of the plant model and the accuracy of the reference current prediction [33]. A H∞ control strategy [34] can improve the robust stability under model uncertainty and load disturbance. However, the control performance under nonlinear load is not satisfactory. The rotating synchronous frame PI controller for current control is used widely to obtain a

zero steady state error [35-36]. However, significant computation arises from the need of multiple reference frames for harmonic current attenuations.

To prevent the pollution of the utility by high-frequency current ripple, an LC filter is used at the output of the inverter. The capacitor is used to provide a low-impedance path for the high frequency components. But the LC filter is virtually un-damped (especially at no load) and thus its resonance can severally affect the quality of V_o and the overall stability of the controller. A resistor in series or parallel with the capacitor can be used to damp the resonance in the filter. However, it is more advantageous to use only a LC filter and design the control algorithm to "actively" damp the resonance. Current-loop regulated PWM inverters with output voltage compensation have been proposed in [37-38]. Controllers with the inductor current feedback as inner loop can be used to actively damp the resonance [39-41], while capacitor current feedback can also be utilized since it has better disturbance rejection capability than that of inductor current feedback [42-46]. Unlike both of the capacitor current feedback and inductor current feedback, paper [47] uses the current flowing between the split two capacitors of the LCL-filter as a feedback variable. By properly designing the controller, it degrades the control object from third-order to first order, so the loop gain and bandwidth can be increased thus the steady-state errors at both fundamental and harmonic frequencies can be decreased. But the zero-pole cancellation used here needs accurate parameters of inductance, capacitance and their internal resistance.

The current loop gain has to be high enough to suppress the disturbance caused by "back EMF" voltage and load current variation. However, the high gain control schemes face the noise corruption and limit cycle ringing problems. [48]. In Nonlinear loads with periodic distortions, the periodical tracking error or disturbance whose frequency is less than half of the sampling frequency can be eliminated by the use of a repetitive controller [49-60]. But repetitive control has slow dynamic response for non-periodic disturbances. To improve the

dynamic response, repetitive controllers are generally combined with other fast-response controllers [50]. However, the fast-response control scheme combined with a repetitive controller also requires the sensing of inductor or capacitor current, resulting in an overall scheme with a high degree of complexity.

This chapter proposes a multi-loop controller with voltage differential feedback, and with output voltage decoupling and output current decoupling by only using the output voltage feedback. The output voltage differential feedback loop actively damps the output LC filter resonance thus increases the system stability margin. The decoupling of output voltage and current makes the inner loop equivalent to a first order system thus improve the system dynamic response to load disturbance. The pole placement technique has been used here to design the inner loop and outer loop gain, with considering the effect of system control delay. The proposed control scheme possesses very fast dynamic response at load step change and can also achieve good steady state performance at both linear and nonlinear loads. In addition, it only uses the output voltage as the feedback variable, which reduces the system complexity. The theoretical conclusion has been verified by simulation and experiment results. This method is proved to be an effective solution for voltage control in standalone mode of three phase micro-grid inverters.

2.2. System configuration and prototype picture

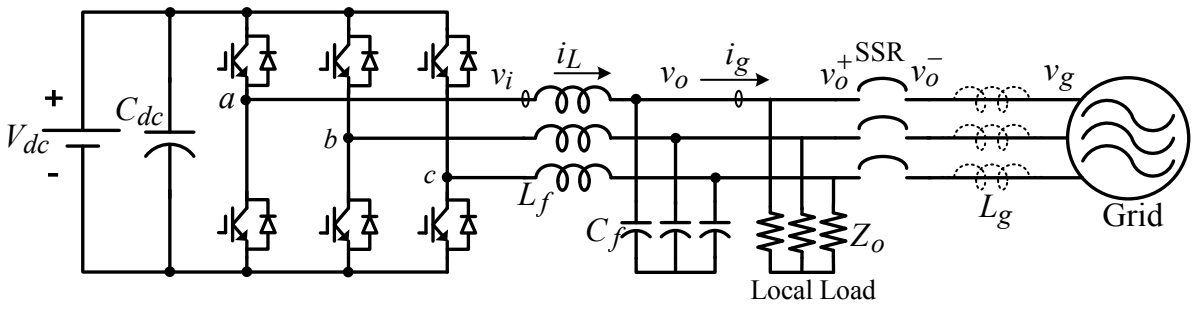


Fig. 2.1.Configuration of three-phase grid-connected VSI with LC filters and local load

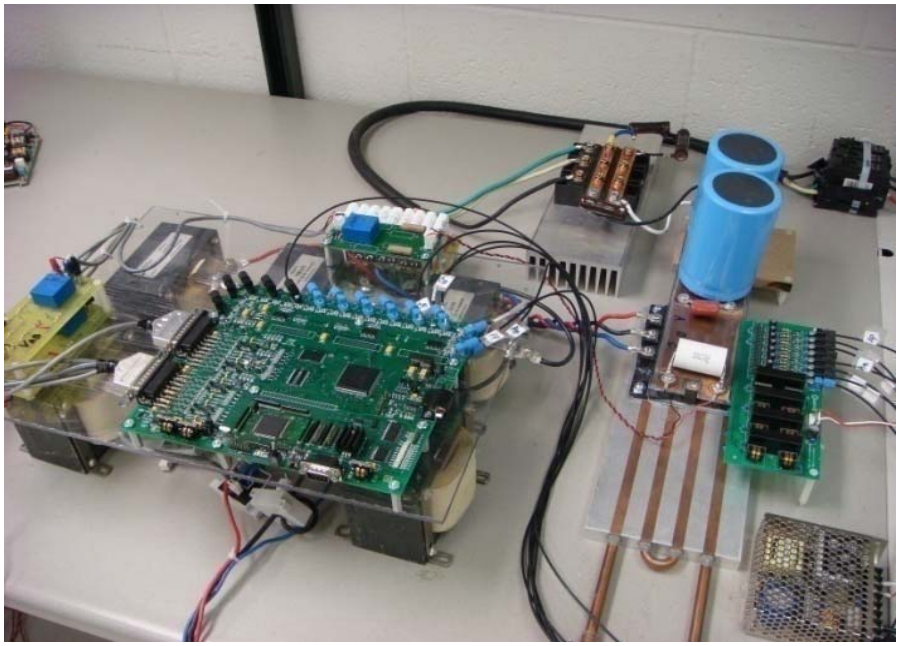


Fig.2.2. Photograph of the three-phase inverter prototype.

Fig. 2.1 shows the configuration of three-phase grid-connected VSI with LC filters and local load. It will operate in grid-connected or standalone mode by controlling the switch SSR. This paper concentrates on the control strategy for standalone mode. The system parameters used in this paper is: switching frequency: 10kHz; output frequency: 60Hz; IGBT dead time: 1.5us; DC-link voltage: 200V; output phase voltage(rms): 60V; output capacity: 10KVA. Fig.2.2 shows the prototype in the experiment.

To select the proper inverter-side inductor, several factors needs to be considered: inverter output current ripple, system cost, size and efficiency. Larger L_f can reduce the output current ripple which enables that the controller to have a high gain to achieve smaller steady state error and faster dynamic response. The maximum current ripple is calculated as: $\Delta I_{\max} = V_{dc} T_s / 4L$. So 1mH inductor is selected here to make the maximum ripple current within 30% of the rated current. For the capacitor design, the goal is to keep the resonant frequency of LC filter be smaller than 1/10 of the switching frequency to get enough attenuation at high frequency. A bigger capacitor can reduce the inductor value, but would also increase the reactive power it produces hence increase the current stress on the switches

also increase the reactive power it produces hence increase the current stress on the switches and inductors. So the capacitor is selected at 50uF to provide 2% reactive power of the rating power.

2.3. Multi-loop controller with capacitor voltage differential feedback [46]

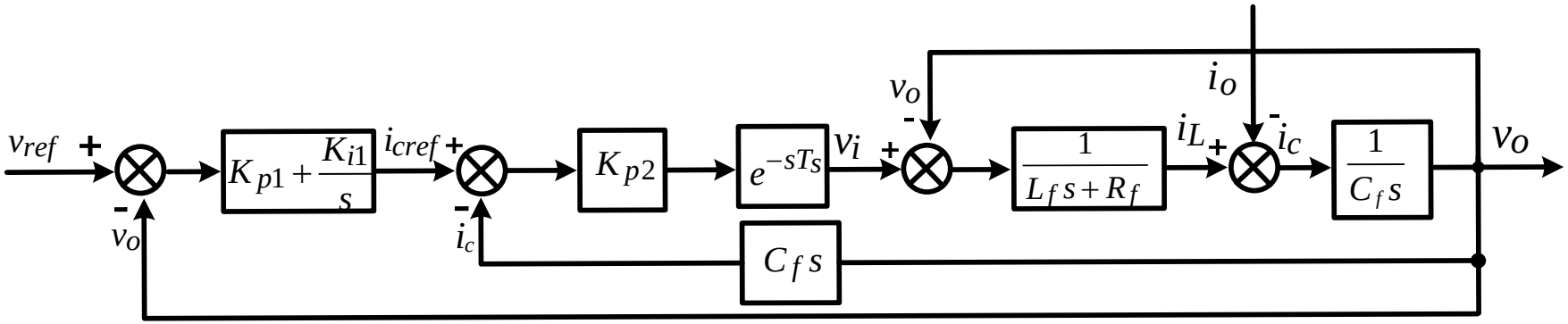


Fig.2.3. Bode diagrams of capacitor voltage differential feedback

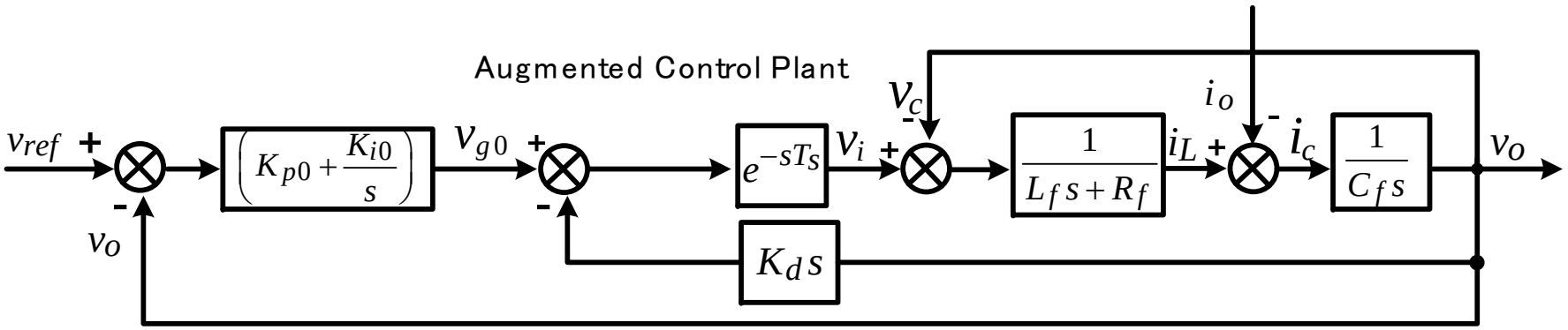


Fig.2.4. Simplified diagrams of capacitor voltage differential feedback

2.3.1. Control block diagram

2.3.1.1. Capacitor voltage differential feedback

A capacitor voltage differential feedback loop is used with the outer voltage regulation loop in order to damp the LC filter resonance thus increases the system stability margin, as shown in Fig. 2.3. The reason will be described as follows.

To prevent the pollution of the utility by high-frequency current ripple, an LC filter is used at the output of the inverter. The capacitor is used to provide a low-impedance path for the high frequency components. But the LC filter is virtually un-damped (especially at no load) and thus its resonance can severally affect the quality of V_o and the overall stability of the controller. Controllers with the inductor current feedback as inner loop can be used to actively damp the resonance, while capacitor current feedback can also be utilized since it has better disturbance rejection capability than that of inductor current feedback. In capacitor current feedback control, a highly accurate current sensor is needed because the capacitor current is in small scale. It also requires the sensor has fast dynamic response. Since capacitor current can be calculated from the voltage, capacitor voltage differential feedback can be used to replace capacitor current feedback so that the current sensor can be saved. Like the capacitor current feedback, the capacitor voltage differential feedback can also eliminate the resonant peak of L-C filter.

Also we can demonstrate this from another point of view. The control block diagram can be simplified into the form in Fig. 2.4. The inner loop is simplified a single capacitor voltage differential feedback loop with feedback coefficient. The closed-loop transfer function of the inner loop (without consideration the control delay) is

$$G_{vo\_vgo}(s) = \frac{v_o}{v_{g0}} = \frac{1}{L_1 C_f s^2 + R_1 C_f s + K_d s + 1} = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \qquad (2.1)$$

, where $K_d = C_s K_{p2}$, which is the differential feedback coefficient. The damping

ratio can be derived as

$$\xi = \frac{R_f C_f + K_d}{2\sqrt{L_f C_f}} \tag{2.2}$$

From (2.1)-(2.2), the LC filter transfer function has a high-resonant peak because the damping ratio ξ is close to zero; after introducing the output voltage differential feedback, the control plant from the traditional LC filter has become to an improved control plant. The damping ratio ξ changes from zero to a variable value, which can be adjusted by the differential coefficient K_d. When K_d is equal to the designed value, the damping ratio is about 0.67, which is very close to the technical optimum (TO) value 0.707. Thus this control method is consistent with the capacitor current feedback.

2.3.1.2. Low pass filter in the feedback loop

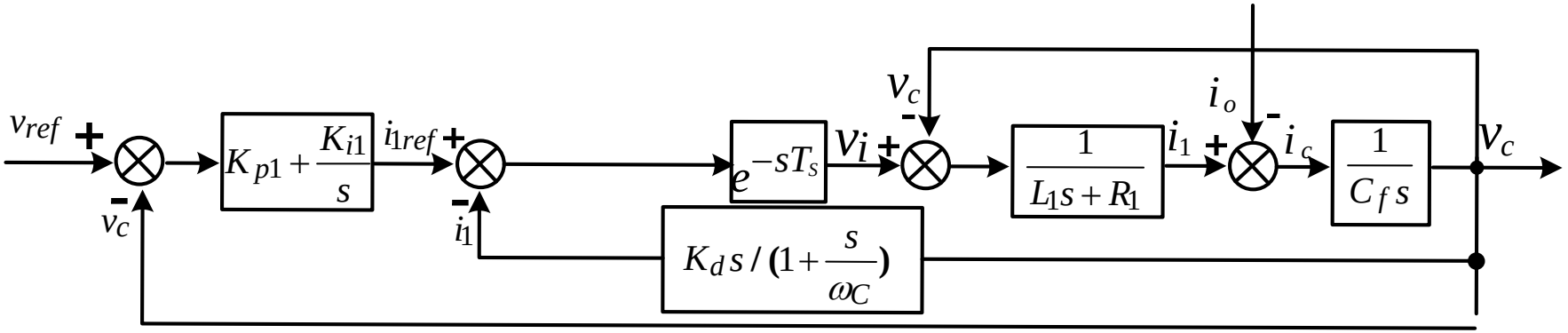


Fig.2.5. Bode diagrams of capacitor voltage differential feedback with low pass filter

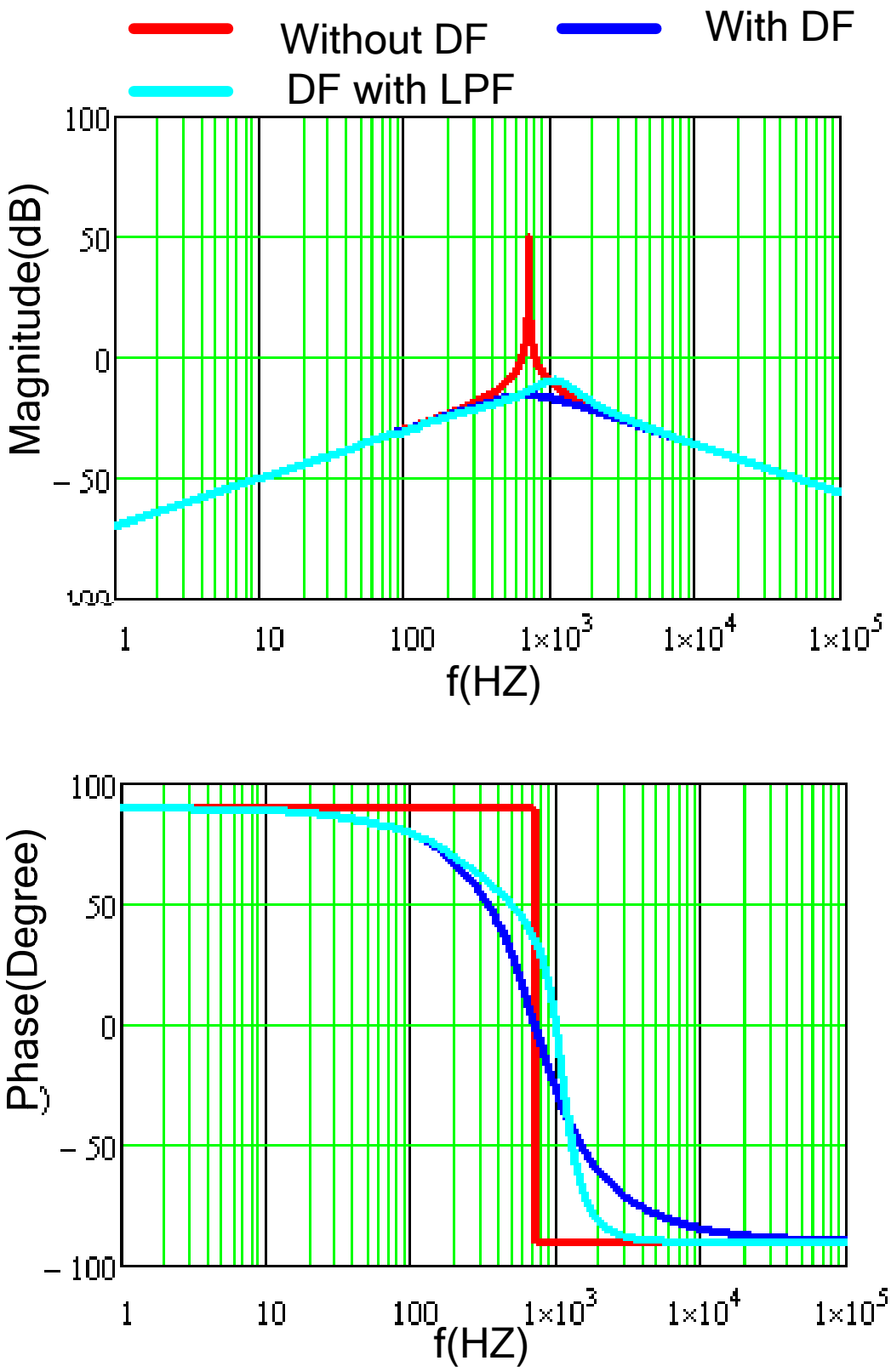


Fig.2.6. Bode diagrams of inner open loop transfer function

However, the differential function will enlarge some small disturbance in the output voltage, especially in the high frequency range so as to cause stability problem. Hence a low pass filter

(LPF) is introduced to use with differential feedback to eliminate the high frequency disturbance, as shown in Fig. 2.6. Fig. 2.6 shows the bode diagrams of inner current loop transfer function without considering the control delay (a) Without voltage DF (differential feedback) (b) With voltage DF (c) With voltage DF and LPF (low pass filter). As indicated, the voltage differential feedback eliminates the high resonant peak of output L-C filter. Moreover, using low pass filter increases the phase margin at crossover frequency hence improves the system stability.

2.3.1.3. Voltage reference feedforward in the outer loop

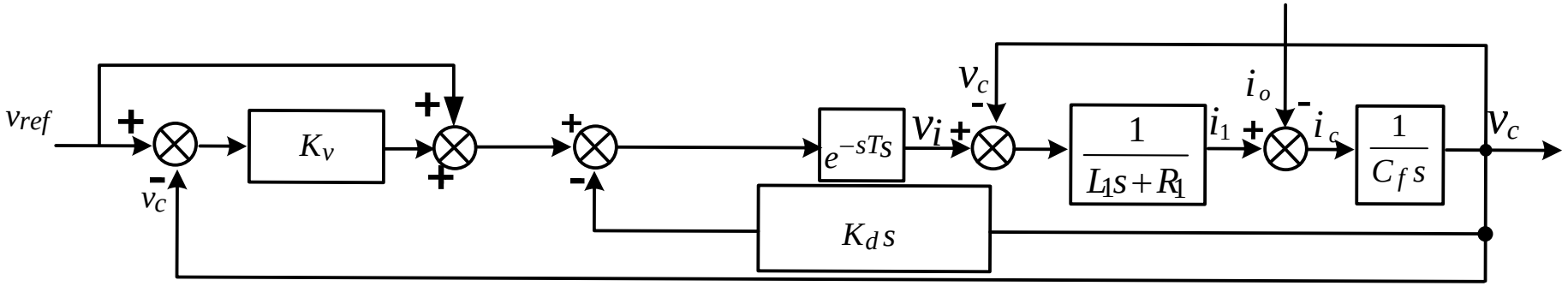


Fig.2.7. Proportional compensator plus feed-forward control strategy

Considering the transient performance when the inverter changes from grid-connected operation mode to standalone mode, with proposed outer voltage PI controller, the initial output voltage is zero which causes the voltage fall to zero immediately after the mode switching. So the voltage waveform becomes discontinuous in transition. In order to overcome this disadvantage, a voltage reference feed-forward path is added to the outer loop, which is shown in Fig. 2.7. The reference voltage is generated by multiplication of voltage amplitude and phase angle which is synchronized with grid voltage in grid-connected operation mode. So the initial output voltage of this standalone system which is equal to the feedforward reference voltage is in phase with grid voltage at the moment of control mode switching. Hence it maintains the continuity of voltage waveform.

In addition, the feedforward path can also improve the steady-state performance. Without feedforward path, the outer loop gain needs to be designed to be a large value to obtain small steady-state error which will make the system face stability problem. Moreover, feedforward path can enhance the dynamic response which is beneficial in transition process or nonlinear load case.

Also, a single proportional controller is used instead of PI controller to reduce the harmonics in the waveform which is analyzed as follows. With considering the control delay, the output voltage-to-reference voltage and output voltage-to-load current transfer function can be expressed as follows:

$$\begin{aligned} v_o(s) &= G'_{vo\_vref}(s)\cdot v_{ref} - G'_{vo\_io}(s)\cdot i_o \\ &= \frac{(1+K_v)e^{-sT_S}}{L_f C_f s^2 + (R_f C_f + K_d e^{-sT_S})s + K_v e^{-sT_S} + 1} v_{ref} \\ &\quad - \frac{L_f s + R_f}{L_f C_f s^2 + (R_f C_f + K_d e^{-sT_S})s + K_v e^{-sT_S} + 1} i_o \end{aligned} \tag{2.3}$$

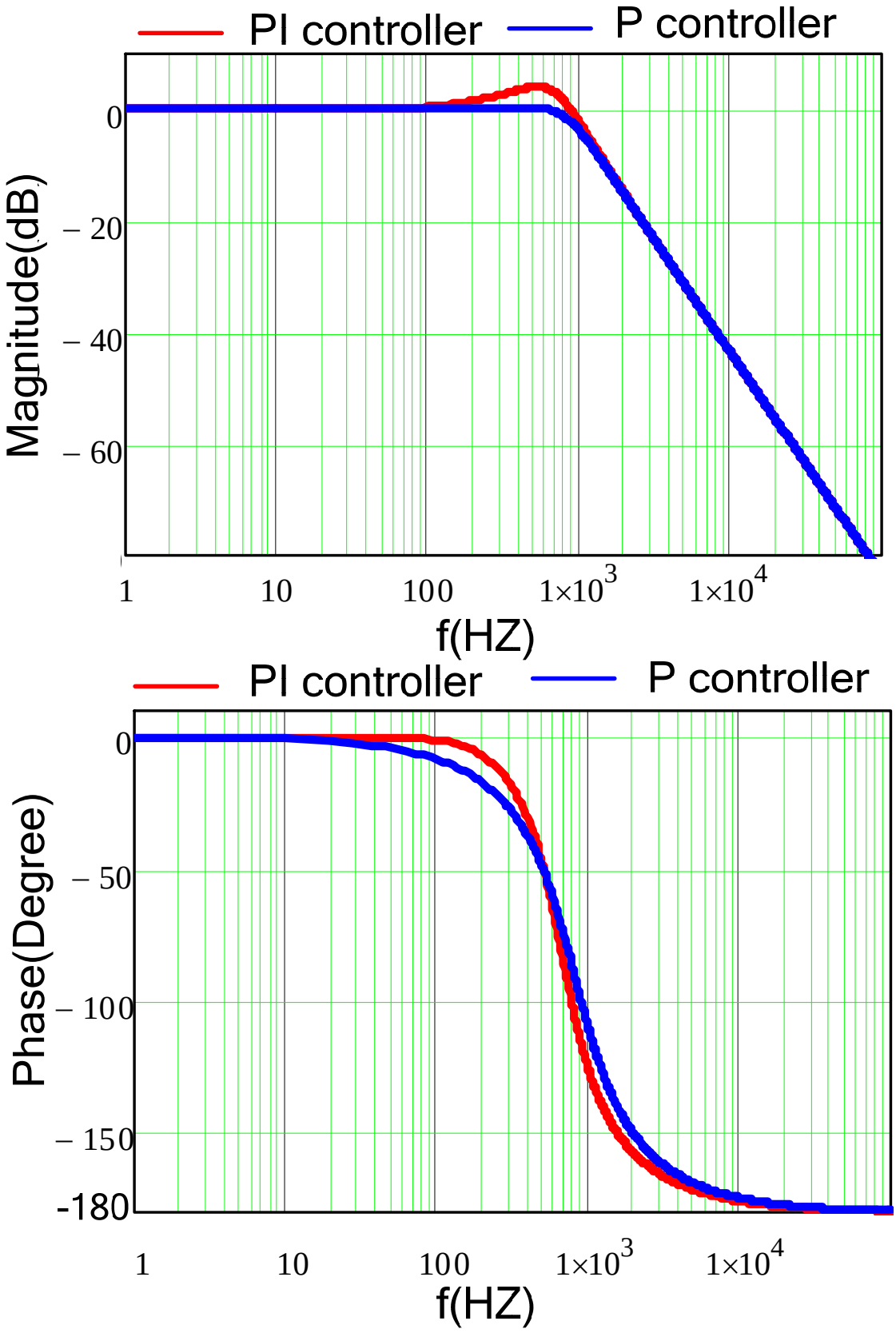


Fig.2.8. Bode diagrams of $G'_{vo\_vref}(s)$ with P and PI controller respectively

Fig. 2.8 compares the voltage closed-loop transfer function with P and PI controller. With PI controller in which $K_{p0} = 0.3, K_{i0} = 1800$, there is a peak at frequency between 60HZ to 900HZ. It raises the portion of the 5th, 7th and 11th harmonics in the output voltage. The peak magnitude decreases as K_i decreases and it decreases to zero when $K_i = 0$. Also with only P controller, the magnitude gain keeps around 0 dB thus the steady-state error stays in a reasonable range. So using a single proportional controller can reduce the harmonic components in the output voltage and still track the reference voltage very well.

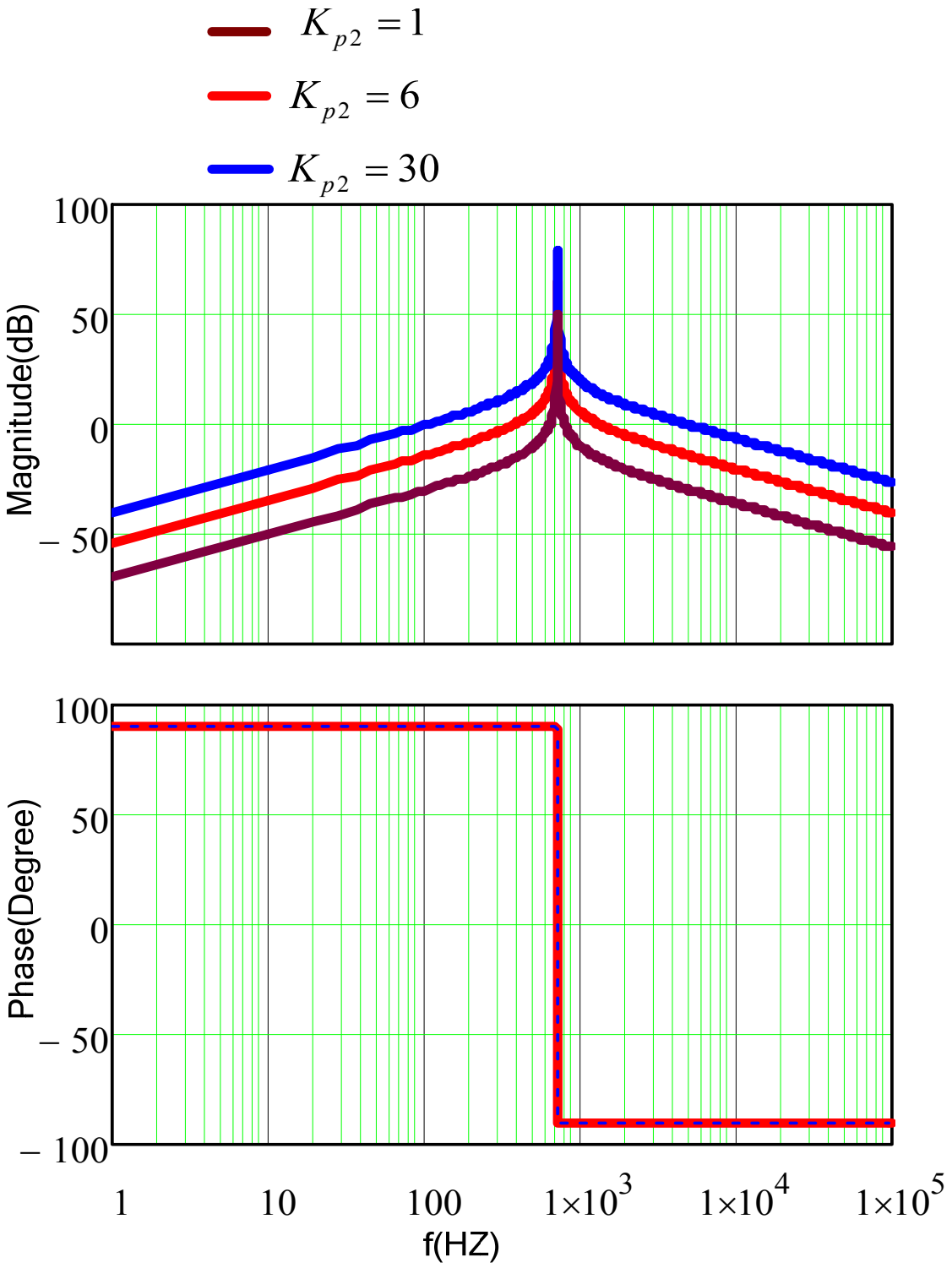
2.3.2. Controller design

2.3.2.1. Inner Current Controller Design

The inner loop controller design of multi-loop with capacitor differential feedback is consistent with the controller design of capacitor current feedback. The compensated open-loop transfer function of the inner current loop can be obtained as:

$$G_{c\_op}(s) = \frac{K_{p2} C_f e^{-sT_S} s}{L_f C_f s^2 + R_f C_f s + 1} \tag{2.1}$$

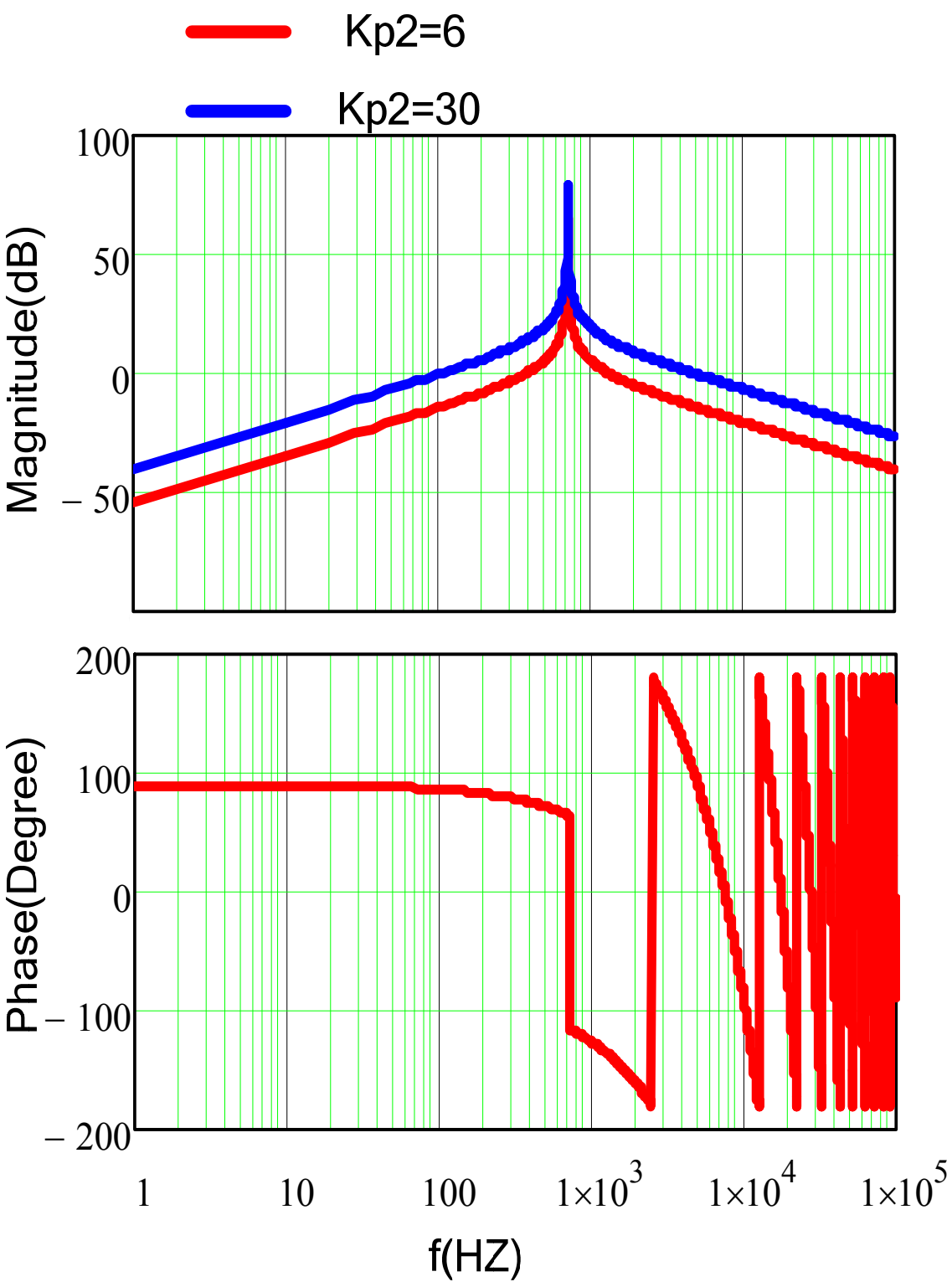
,where K_{p2} is the gain of current controller. Fig. shows the bode diagrams of the compensated



(a)

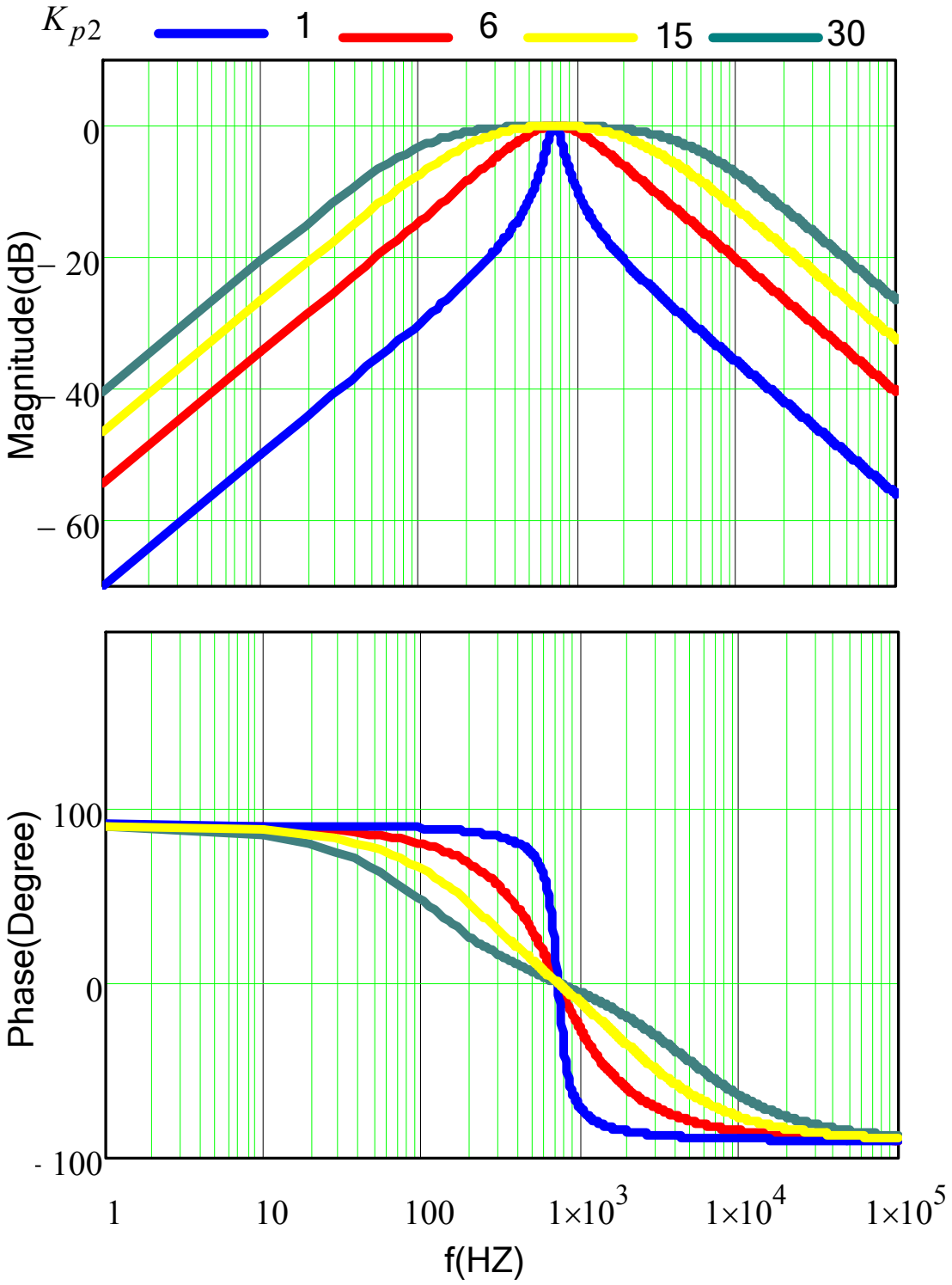
Fig.2.9. Bode diagrams of inner loop transfer function (a) open loop without delay (b) open loop with delay (c) closed-loop without delay at different K_{p2}

Figure 2.9 (cont'd)



(b)

Figure 2.9 (cont'd)



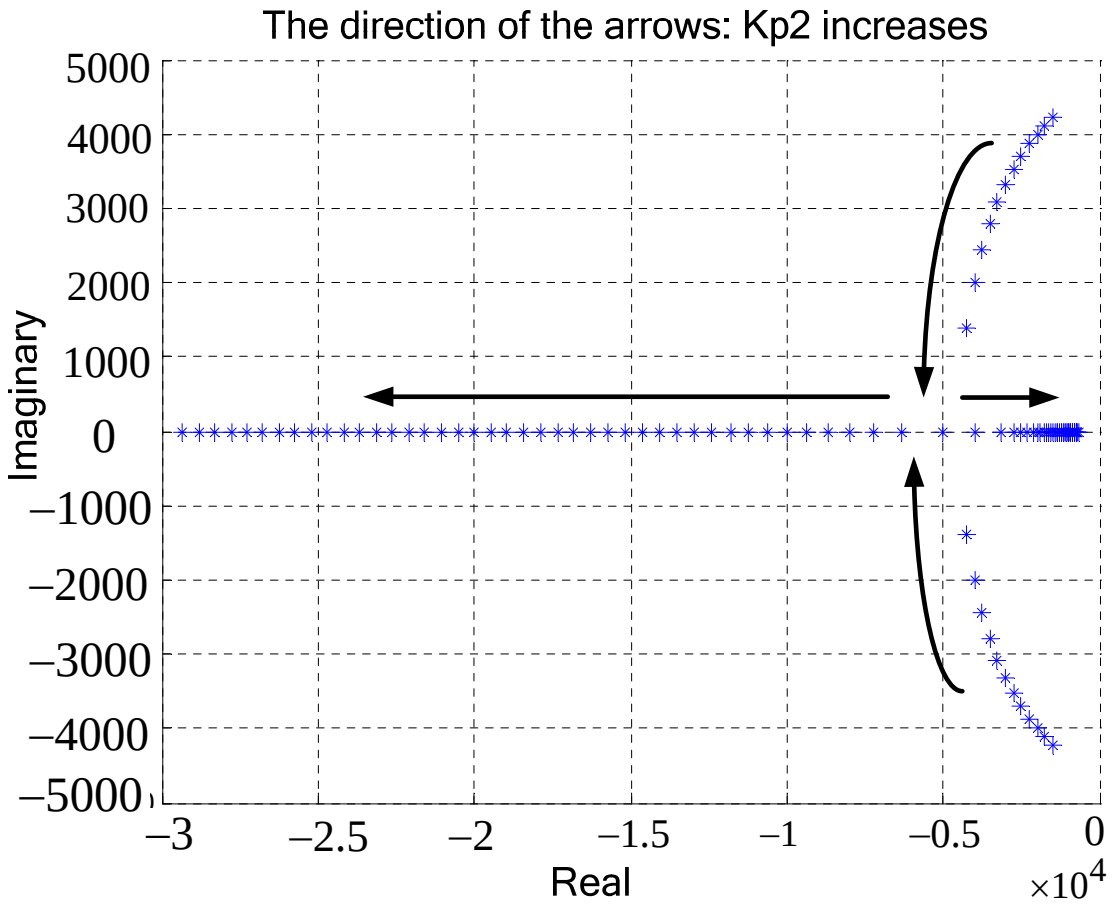
(c)

inner current open-loop at proportional gain $K_{p2} = 0, 6, 30$ for no load case (worst case condition). As K_{p2} increases, the high resonant peak increases which make it hard to design

the outer voltage control loop to achieve good system stability and dynamic response. However, the resonant peak can be eliminated by closed-loop control. The compensated closed-loop transfer function of the inner current loop is:

$$i_c = \frac{K_{p2}e^{-sT_s}C_f s}{L_f C_f s^2 + \left(K_{p2}e^{-sT_s} + R_f\right)C_f s + 1} i_{cref} - \frac{L_f C_f s^2 + C_f R_f s}{L_f C_f s^2 + \left(K_{p2}e^{-sT_s} + R_f\right)C_f s + 1} i_o \tag{2.4}$$

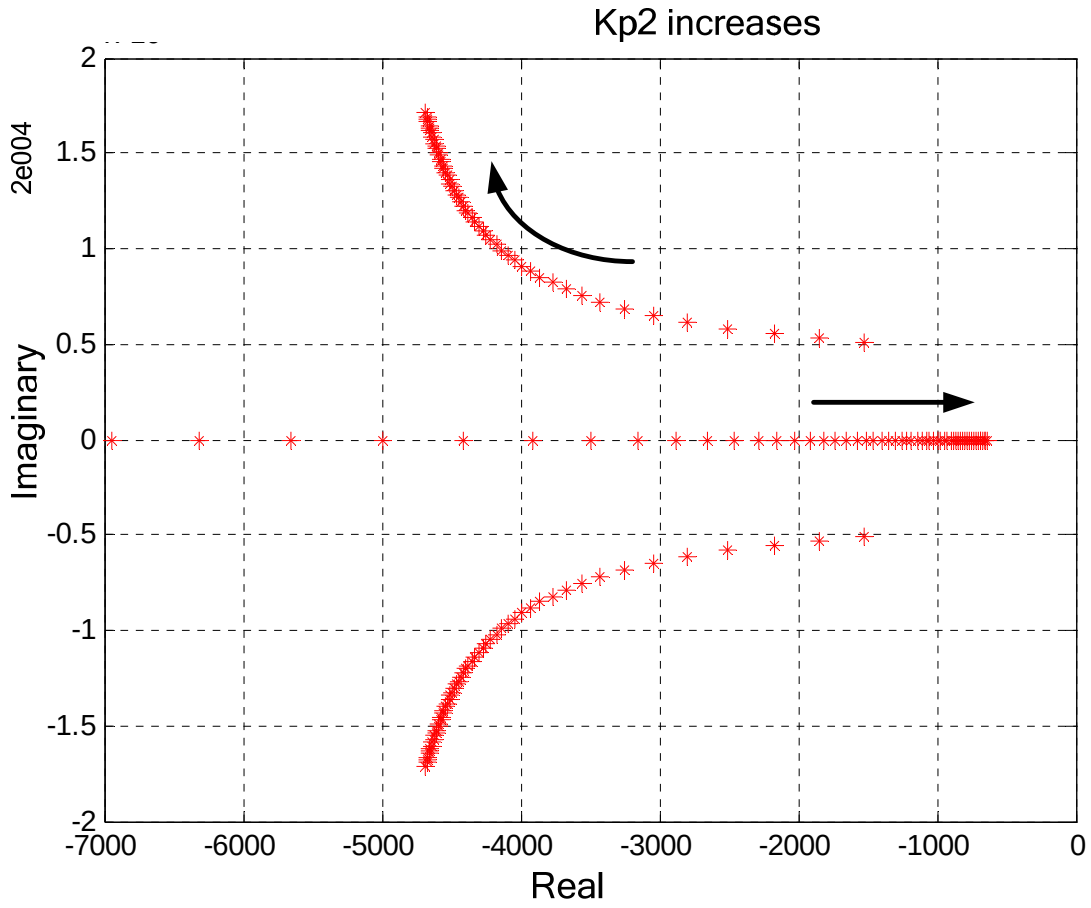
where i_{cref} is current reference generated by voltage loop, i_c is measured capacitor current and i_o is the load current.



(a) Without considering control delay

Fig.2.10. Root locus of inner current closed-loop without and with control delay when K_{p2} increases

Figure 2.10 (cont'd)



(b) With considering control delay

The design goal of inner current closed-loop in a multi-loop control is to obtain a high loop bandwidth to achieve enough stability margins rather than to obtain a small tracking error. So the current controller is designed to be a single proportional controller. Fig. 2.9 (a) shows the bode diagrams of current closed-loop transfer function at different K_{p2} values without considering the control delay. As indicated, the bandwidth can be widen and also the phase error can be reduced through increasing the proportional gain K_{p2}. Ideally, the bandwidth of I_C / I_C^* should be maximized by using a higher K_{p2}, to achieve perfect reference tracking at all input frequencies, a faster dynamic response and the complete blocking of disturbance input from feeding forward to the output ($I_C / I_{load} = 0$). In order to obtain unity gain from

output frequency to half of the switching frequency [61], the gain value should be designed to be 30. However, in practice, a digital control implementation for above multiple-loop control method introduces a time delay, usually equal to one switching period T_S, which strongly limits the system bandwidth and affects the dynamic performance [62-64]. The root-loci of the inner current closed-loop without control delay and with T_S control delay are shown in Fig. 2.10. The arrows show the moving direction of the root locus when K_{p2} increases. Without considering the delay, the complex roots will move towards the real axis and move far away from imaginary axis. With considering the delay, the complex roots will move away from real axis, which will cause the system oscillation; the real root will move towards the imaginary axis. A high gain would degrade the control loop stability. This can be further verified by the bode diagrams of the current open loop with control delay at different K_{p2}, as shown in Fig. 2.9(b). When K_{p2} =6, the phase margin is about 60^0; when K_{p2} =30, the phase angle at crossover frequency enters into the oscillation region and the system become unstable. Based on this gain selection criterion, K_{p2} is set as 6, which will give a reasonable closed-loop current gain I_C / I_{Cref} and negligibly small I_C / I_{load} gain at the fundamental frequency.

2.3.2.2. Outer Voltage Controller Design

For the outer voltage regulation loop, a PI controller is used to maintain high loop gain at low frequency and zero steady state error. The compensated open-loop voltage transfer function is:

$$G_{vop} = (K_{p1} + \frac{K_{i1}}{s}) \frac{K_{p2} e^{-sT_S}}{L_f C_f s^2 + \left(K_{p2} e^{-sT_S} + R_f\right) C_f s + 1} \tag{2.5}$$

, where K_{p1} and K_{i1} are parameters for PI controller. The crossover frequency f_{C1} is set to be 300HZ which guarantees enough attenuation at switching frequency and enough phase

margin at crossover frequency. K_{P1} *and* K_{i1} are selected to obtain unit gain at this crossover frequency. Also, the zero of the PI compensator is set the same as the corner frequency of LC filter, resulting in the following equations:

$$\frac{K_{i1}}{K_{P1}} \approx \frac{1}{\sqrt{LC}}, \qquad \left|G_{vop}(s)\right|_{s=j2\pi f_{c1}} = 1 \tag{2.6}$$

Which leads to $K_{P1} = 0.05, K_{i1} = 300$.

2.3.3. Demonstration of its advantage

Compared to inductor current feedback strategy, capacitor current feedback has better disturbance rejection capability.

If capacitor voltage differential term is used as inner current feedback variables, the closed-loop transfer function of the outer voltage loop can be expressed as:

$$\begin{aligned} v_o = & \frac{(K_{p1}s + K_{i1})K_{p2}e^{-sT_S}}{L_f C_f s^3 + (K_{p2}e^{-sT_S} + R_f)C_f s^2 + (K_{p1}K_{p2}e^{-sT_S} + 1)s + K_{i1}K_{p2}e^{-sT_S}} v_{ref} \\ & - \frac{L_f s^2 + R_f s}{L_f C_f s^3 + (K_{p2}e^{-sT_S} + R_f)C_f s^2 + (K_{p1}K_{p2}e^{-sT_S} + 1)s + K_{i1}K_{p2}e^{-sT_S}} i_o \end{aligned} \tag{2.7}$$

where v_{cref} is the given voltage reference and v_o is the output voltage.

If inductor current is used as inner current feedback variables, the closed-loop transfer function of the outer voltage loop can be expressed as:

$$\begin{aligned} v_o = & \frac{(K_{p1}s + K_{i1})K_{p2}e^{-sT_S}}{L_f C_f s^3 + (K_{p2}e^{-sT_S} + R_f)C_f s^2 + (K_{p1}K_{p2}e^{-sT_S} + 1)s + K_{i1}K_{p2}e^{-sT_S}} v_{ref} \\ & - \frac{L_f s^2 + (K_{p2}e^{-sT_S} + R_f)s}{L_f C_f s^3 + (K_{p2}e^{-sT_S} + R_f)C_f s^2 + (K_{p1}K_{p2}e^{-sT_S} + 1)s + K_{i1}K_{p2}e^{-sT_S}} i_o \end{aligned} \tag{2.8}$$

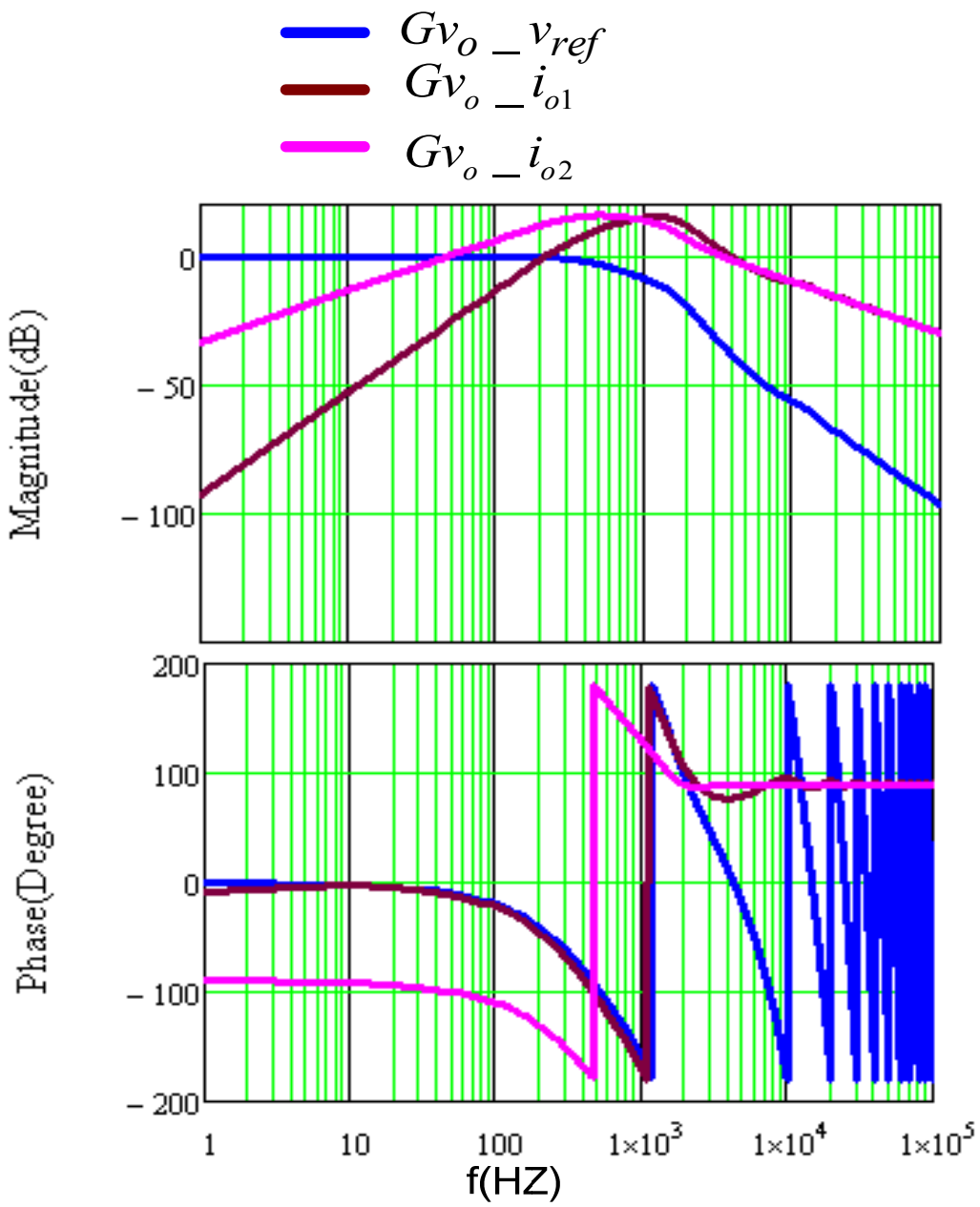


Fig.2.11. Bode diagrams of the outer voltage closed-loop transfer function with capacitor current or inductor current feedback as inner loop

From equation (2.5) and (2.6), it is notable that in the capacitor current feedback and inductor current feedback, the output voltage-to-reference voltage transfer function $G_{vo\_vref}(s)$ is exactly the same, while the voltage-to-output current transfer function $G_{vo\_io}(s)$ is different from each other, where $G_{vo\_io1}(s)$ and $G_{vo\_io2}(s)$ are corresponding to (2.5) and (2.6) respectively. Fig. 2.11 shows the bode diagrams of

closed-loop voltage transfer function using two control schemes respectively. Obviously, capacitor current feedback strategy has lower gain at low frequency range for output voltage to load current than inductor current feedback strategy, which means it has much better disturbance rejection capability.

2.4. Multi-Loop controller with both voltage differential feedback and voltage and current decoupling through only output voltage feedback [67]

2.4.1. Control block diagram

This section proposes a multi-loop controller with voltage differential feedback, output voltage decoupling and output current decoupling by only using the output voltage feedback. The decoupling of output voltage and current makes the inner loop equivalent to a first order system. Thus the system will exhibit a fast dynamic response to load disturbance. With considering the control delay, the inner loop gain has to be designed smaller than the design value from pole placement technique, in order to raise the system stability margin. This scheme possesses very fast dynamic response at load step change and can also achieve good steady state performance at both linear and nonlinear loads. In addition, it only uses the output voltage as the feedback variable, which reduces the system complexity. The theoretical conclusion has been verified by simulation and experiment results. This method is proved to be an effective solution for voltage control in standalone mode of grid-tie three phase voltage source inverters. The proposed new control block diagram has been shown in Fig. 2.12.

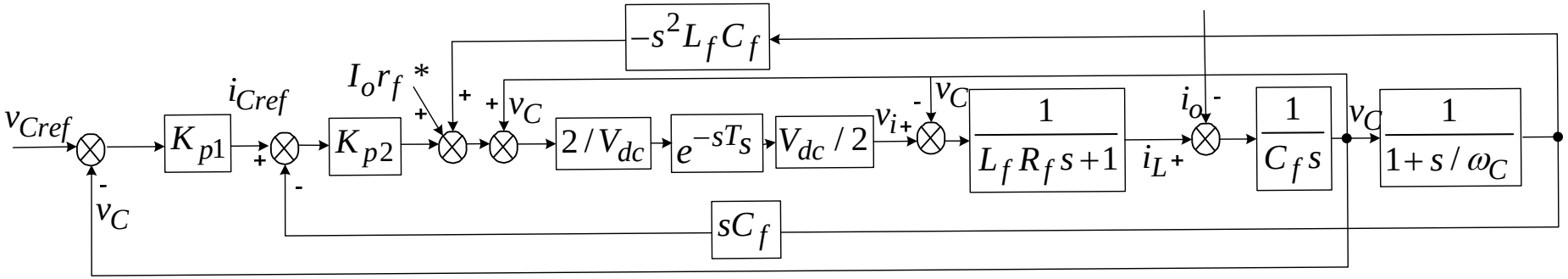


Fig.2.12. Control block diagram of proposed multi-loop controller

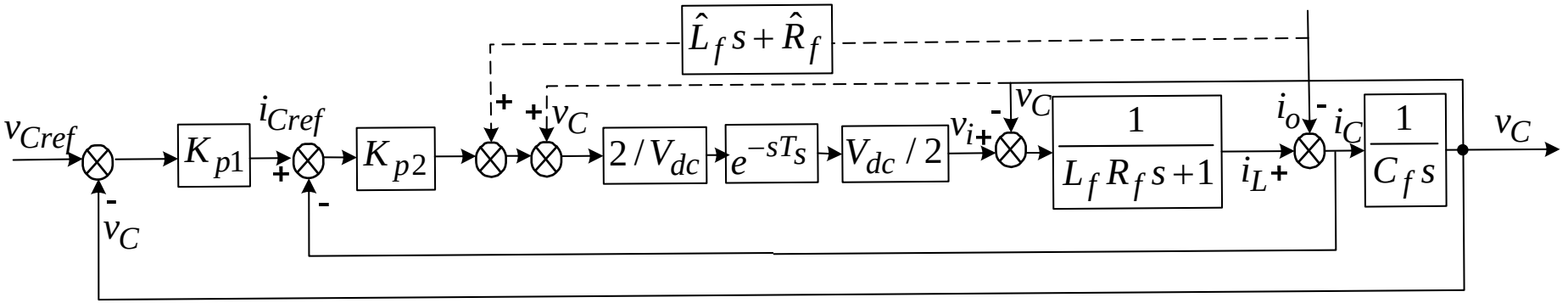


Fig.2.13. Control block diagram of a multi-loop controller with load current and output voltage sensed

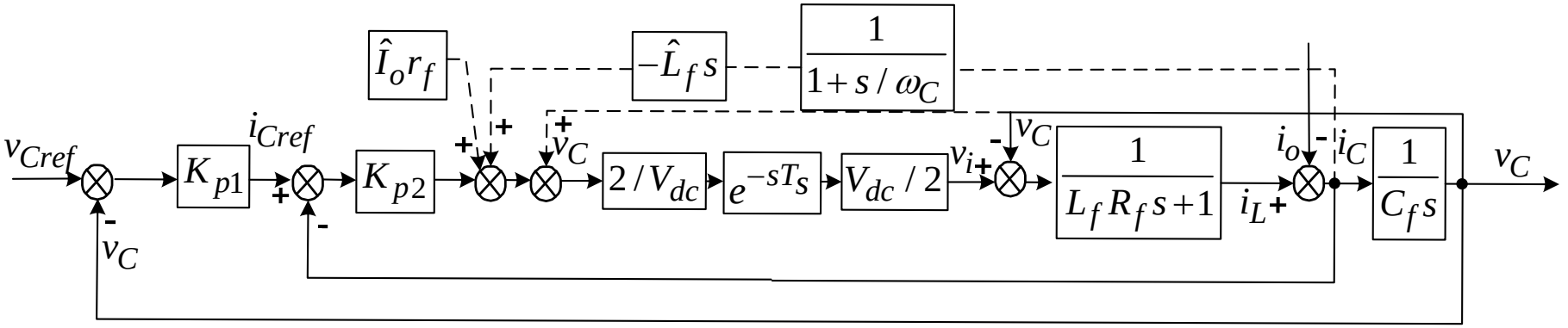


Fig.2.14. Control block diagram of a multi-loop controller with capacitor current and output voltage sensed

2.4.1.1. Output Voltage decoupling

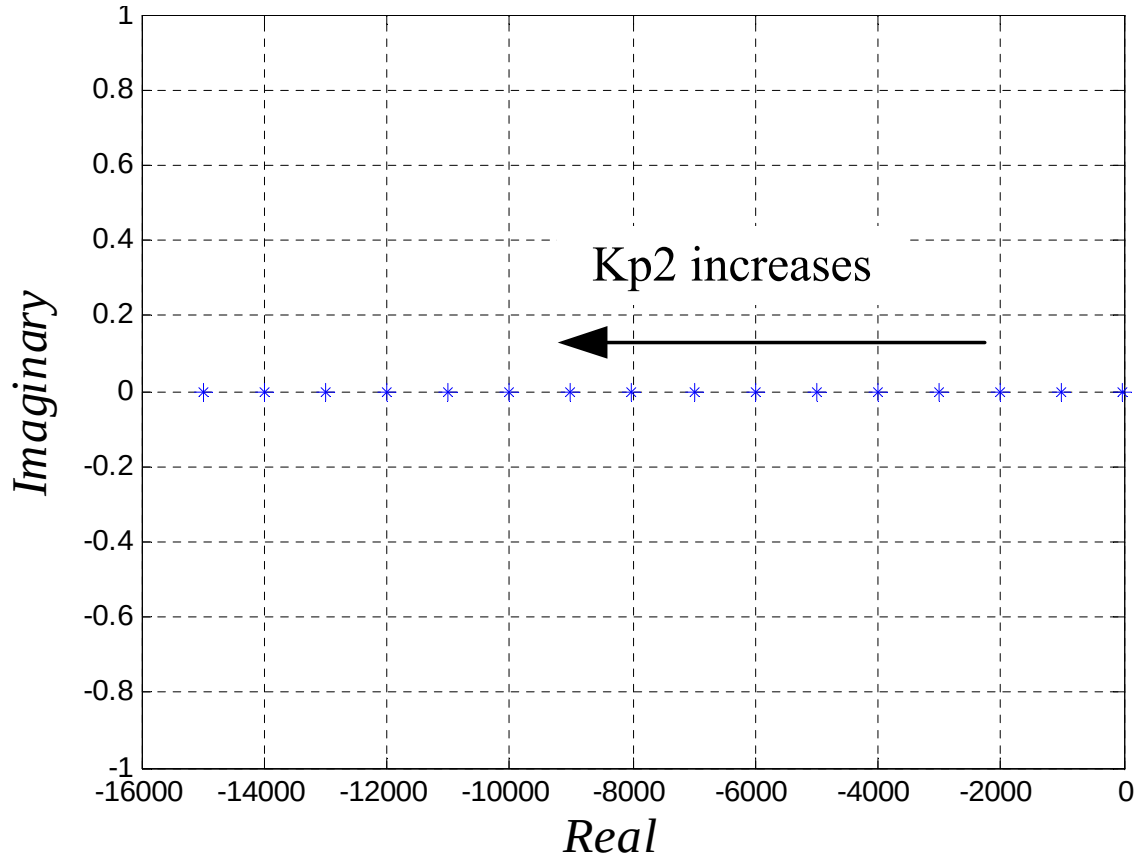
Except for the voltage differential feedback, in the inner loop, the sensed value of output voltage is positively feedback to decouple the output voltage in the augmented control plant in order to improve the system dynamic performance. It is also equivalent to feedback the integration value of capacitor current scaled by C_f. With this decoupling, only the voltage across the output inductor needs to be commanded. This will cause a relatively small voltage variation at load step change because the filter inductor impedance is small. In addition, since most of the inverter command v_i is constructed from the output voltage decoupling, the inner loop gain can be designed more robust. Thus the effect of phase delay introduced by the filtering in the capacitor current feedback will be reduced. In a word, system dynamic response will be faster with this output voltage decoupling. This can be further verified by comparing the root locus of the system with and without output voltage decoupling as follows.

Without v_C decoupling, the inner current closed-loop transfer function can be written as:

$$G_{i_{C\_}i_{Cref}} = \frac{sK_{p2}C_f}{s^2 L_f C_f + sC_f(r_f + K_{p2}) + 1} \tag{2.9}$$

With v_C decoupling, the transfer function becomes:

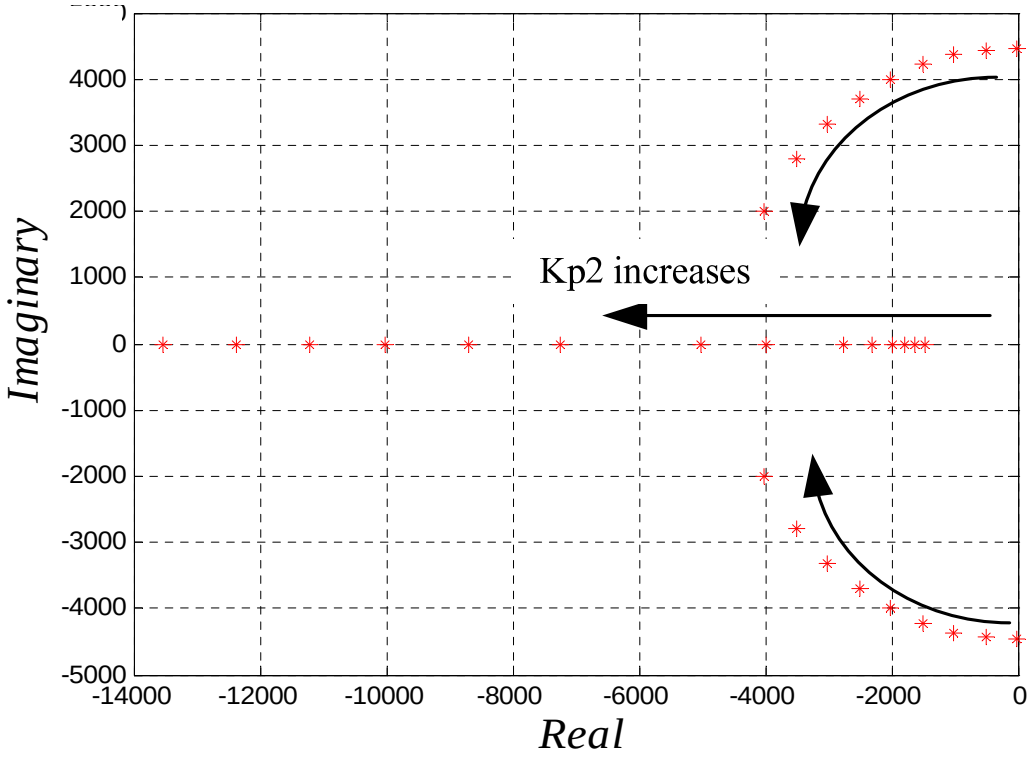
$$G_{i_{C\_}i_{Cref2}} = \frac{i_C}{i_{Cref}} = \frac{K_{P2}}{sL_f + R_f + K_{P2}} \tag{2.10}$$



(a) Kp2 increases

Fig.2.15. Root locus of inner closed-loop when K_{p2} increases from 0 to 15 with step equal to 1 for System (a) With output voltage decoupling (b) Without output voltage decoupling

Figure 2.15 (cont'd)



(b) Kp2 increases

The root locus of two systems when K_{p2} increases from 0 to 15 with step equal to 1 has been shown in Fig. (a), (b). G_{iC_iCref2} is a first order transfer function and all of its poles are on the negative real axis. Its biggest pole locates at $s=-1$ when $K_{p2}=0$. As K_{p2} increases, the poles are approaching infinity. G_{iC_iCref} is a second order transfer function, thus it has two poles at a fixed K_{p2} value. When K_{p2} is small, one pole moves far away from the imaginary axis on the real axis; another pole moves towards the real axis and far away from the imaginary axis from a location which has a big imaginary absolute value. Obviously, at the same K_{p2}, the poles of un-decoupled one locate closer to the y axis than the decoupled one, and with the same step, the dominant pole of the un-decoupled system moves less distances for real axis than the decoupled one. So it has longer response time and higher

the same K_{p2}, the poles of un-decoupled one locate closer to the y axis than the decoupled one, and with the same step, the dominant pole of the un-decoupled system moves less distances for real axis than the decoupled one. So it has longer response time and higher overshoot value at step response. Also its large imaginary part of the dominant pole will cause the oscillation in the dynamic response. Simply saying, the additional zero at the nominator of the un-decoupled system reduces the damping ratio of the system and increases the system overshoot at step response. So the decoupling term can improve the system dynamic response.

2.4.1.2. Load current decoupling

The load current decoupling is implemented by the negative capacitor voltage second differential feedback, as shown in Fig. 2.12, which is also equivalent to negative capacitor current differential feedback. It is an approximation to the positive load current differential feedback as shown in Fig. 2.13 which can fully decouple the load current in the inner loop. The reason of this approximation is: the capacitor current, inductor current and load current satisfies the equation $i_L = i_C + i_o$; and the inductor current will keep almost constant at the load step change. So the derivative of load current is identical to the negative derivative of capacitor current: $di_o / dt = -di_C / dt$.

In addition, the observe value of output current shown in equation (4) could be used to decouple the resistance term in the feedback, considering that the resistance in the inductor is very small and the inaccurate observe value will not affect much. The estimated load current used here is shown in the following expression:

$$\widehat{i_o} = (v_i^* - v_C) / (sL_f + r_f) - i_C \tag{2.11}$$

, in which v_i* represents the control command for the inverter.

This decoupling term provides an additional current loop command to produce the needed load current without waiting for errors in the voltage to occur, thus the system exhibit

infinite dynamic stiffness up to the bandwidth of the voltage modulator, provided that the estimation of the inductance L is accurate. It brings the load current in the closed loop thus increases the rejection gain for the load current disturbance. This also can be verified by the bode plot of disturbance to output transfer function of inner loop as shown in Fig. 2.16.

Without load current decoupling, the disturbance to output transfer function is:

$$G_{i_C\_i_O1} = \frac{i_C}{i_o} = -\frac{sL_f + R_f}{sL_f + (R_f + K_{P2})} \tag{2.12}$$

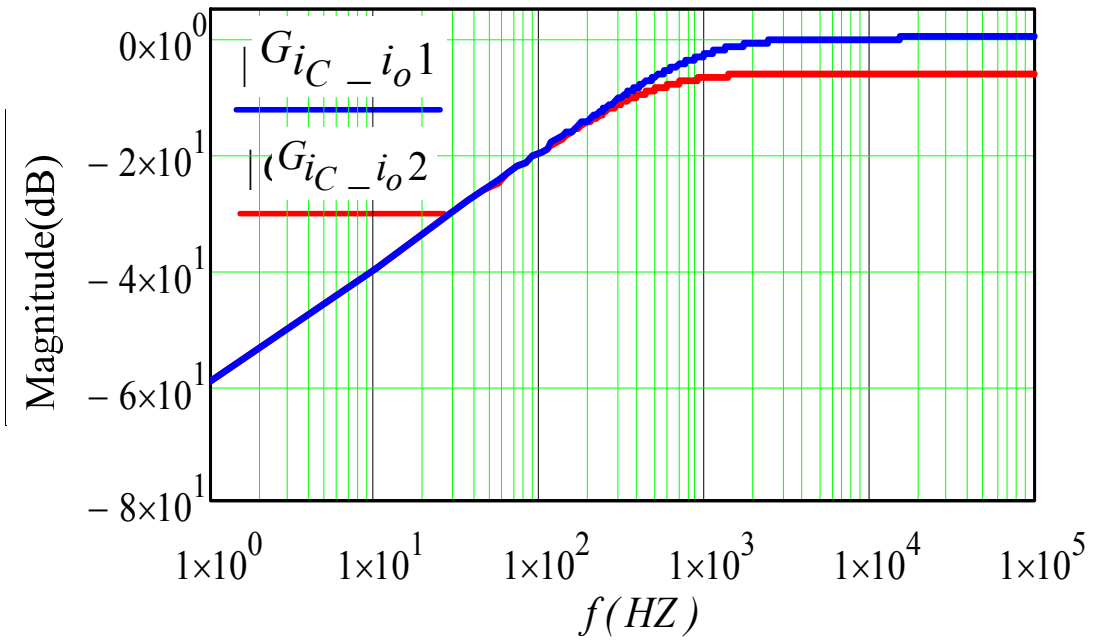


Fig.2.16. Bode plot for load current disturbance to output of inner current loop with and without load current decoupling

With load current decoupling, the transfer function becomes:

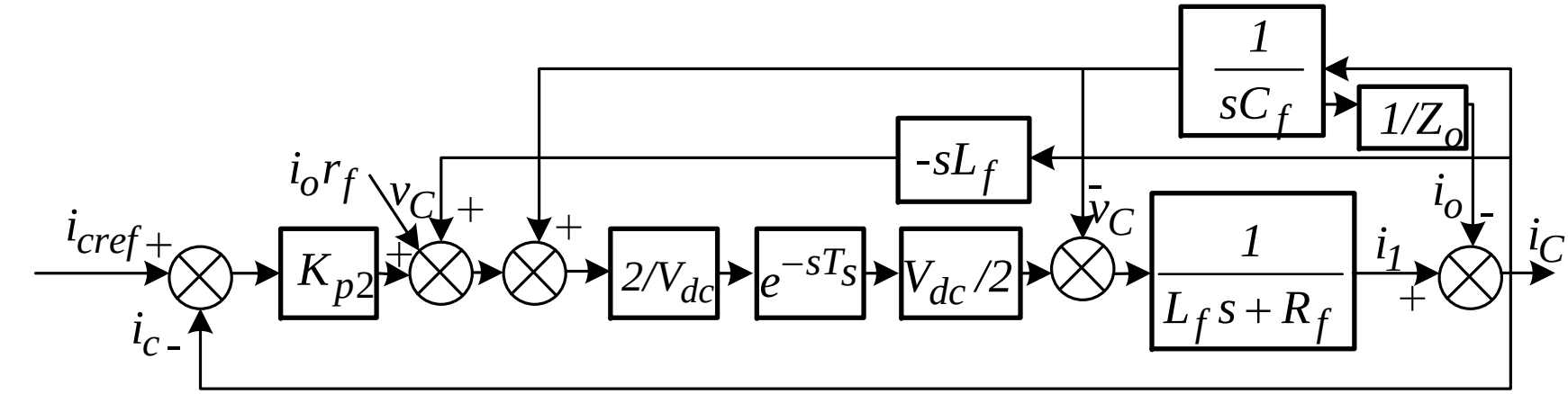
$$G_{i_C\_i_o2} = \frac{i_C}{i_o} = -\frac{sL_f}{s \cdot 2L_f + K_{P2}} \tag{2.13}$$

From the bode plot of these two transfer functions shown in Fig. 2.16, it can be seen that at low frequency, two methods have the same output stiffness to the load current disturbance; while at higher frequency range, the controller with load current decoupling has higher

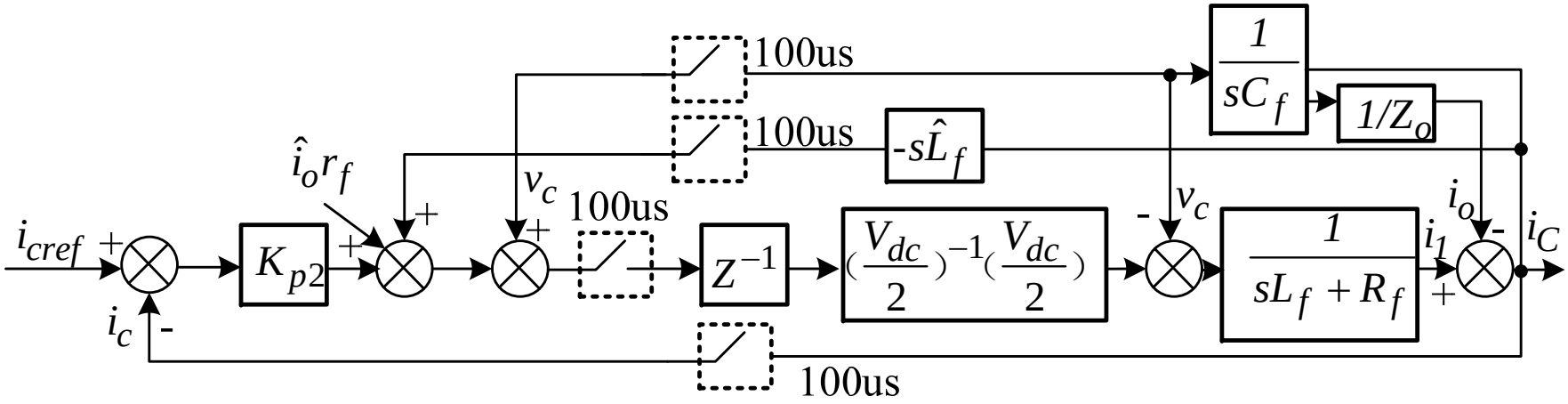
dynamic stiffness, in another word, a unit change of i_o will cause less i_C change. This can also be recognized by observing the pole in the denominator of the transfer function. The pole has been shifted towards the imaginary axis by adding a load current decoupling loop, which also decreases the rate of change of i_C caused by i_o because the damping factor has been reduced.

2.4.2. Controller Design

2.4.2.1. Inner current controller design



(a)



(b)

Fig.2.17. Control block diagram of Inner capacitor current loop at (a) Continuous (b) Digital case

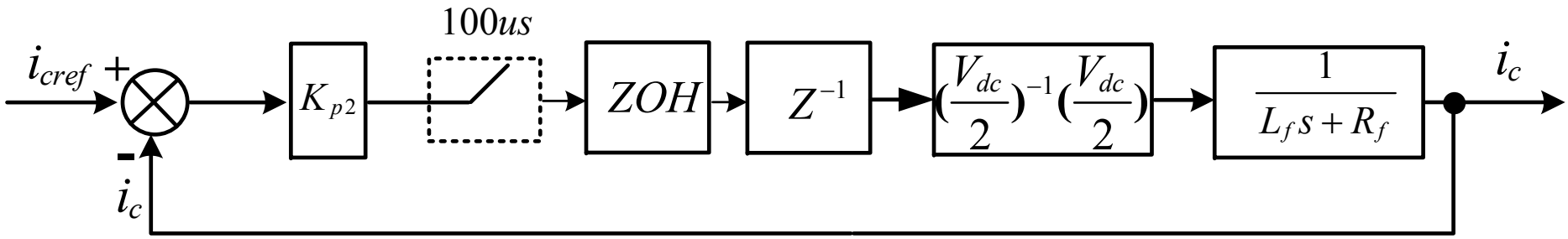


Fig.2.18. Simplified digital control block diagram of capacitor current loop after V_o and i_o decoupling

The inner current loop design is simplified to a first-order system design after applying the decoupling scheme. A pole placement technique is used here to design the loop gain, with considering the real discrete factor and system delay. Fig. 2.17 (a) and (b) shows the block diagram for inner current loop of the proposed control scheme at continuous and digital case respectively. The output voltage and output current act as an exogenous disturbance in this loop. As mentioned before, these disturbances have been suppressed by adding output voltage and current decoupling feedback. Owing to the canceling effect, the inner current loop can be simplified into a first order system shown in Fig. 2.18. The block ZOH represents a zero-order holder used in digital system. As known the analog system can response as fast as possible if all the poles are placed at minus infinity. But it is impossible to design a continuous system with proper transfer function. However, in digital system, it is realizable because $s=-\infty$ is mapped to z=0. Therefore, it is possible for a digital control system to achieve its fastest response if all the closed-loop poles are placed at zero. This pole placement technique is referred to deadbeat control.

For the simplified digital system, the closed loop transfer function without considering the control delay is

$$\frac{i_C}{i_{Cref}} = \frac{K_{p2}(e^{-(r_f/L_f)T_S} - 1)/r_f}{Z + K_{p2}(e^{-(r_f/L_f)T_S} - 1)/r_f + e^{-(r_f/L_f)T_S}} \tag{2.14}$$

, in which L_f, r_f represents the inductance and resistance of the filter inductor, and T_s is the switching period.

In order to place Z at zero, K_{p2} has to satisfy:

$$K_{p2} = \frac{r_f e^{-(r_f/L_f)T_S}}{1 - e^{-(r_f/L_f)T_S}} \tag{2.15}$$

According to the parameters stated in Table I, the K_{p2} is calculated to be 10.

However, in practice, a digital implementation will introduce a time delay, usually equal to one switching period T_s which strongly limits the system bandwidth and affects the dynamic performance [63][64].To redesign the inner loop gain, if the control delay Z^{-1} is considered, the expression for K_{p2} becomes:

$$K_{p2} = \frac{-r_f Z(Z - e^{-(rf/Lf)T_S})}{1 - e^{-(rf/Lf)T_S}} \tag{2.16}$$

The pole Z can not be placed at zero because the loop gain becomes zero in this case. If Z is placed at a small value between 0 and 1, K_{p2} can be calculated. Obviously K_{p2} value decreases compared to the non-delay case. Since the pole in s domain can not be placed at minus infinity, the system dynamic performance has been degraded due to the delay. If the poles are approaching the imaginary axis, the control delay could also cause the system stability problem. Based on the gain selection criterion in equation (2.17), K_{p2} is set as 6, which will give enough stability margin.. Also the bandwidth of the closed loop is enough to obtain a good tracking performance and disturbance rejection capability.

2.4.2.2. Outer Voltage Controller Design

2.4.2.3.

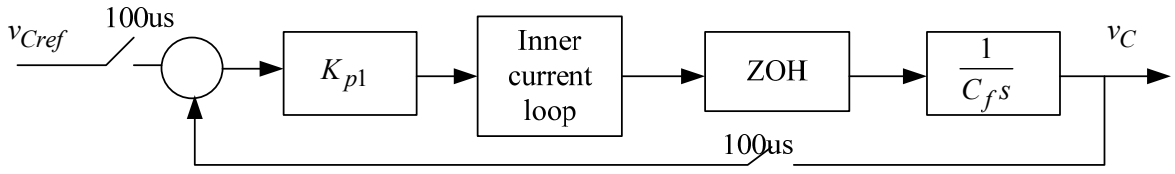


Fig.2.19. Digital Control Block diagram of Simplified voltage loop

The outer voltage controller design can still use the pole-zero placement technique after simplifying the inner loop as a simple gain. The digital control block diagram of outer voltage loop has been shown in Fig. 2.19. Without considering the control delay, the inner loop can be considered as a constant gain in the design of outer loop controller. However, the control

delay limits the value of K_{p2}, so the dynamic response can not be so perfect as placing the pole at minus infinity. The closed loop transfer function with considering the control delay can be expressed as:

$$G_C = \frac{i_C}{i_{cref}} = \frac{\frac{Kp2}{rf}(1-e^{-(rf/Lf)Ts})}{Z(Z-e^{-(rf/Lf)Ts})+\frac{Kp2}{rf}(1-e^{-(rf/Lf)Ts})} \tag{2.17}$$

With this accurate model, the outer voltage loop closed-loop transfer function can be derived with design value K_{p2}:

$$G_V = \frac{V_C}{V_{cref}} = \frac{0.6K_{p1}T_s / C_f}{Z^3 - 2Z^2 + 1.6Z - 0.6 + \frac{0.6Kp1Ts}{Cf}} \tag{2.18}$$

, in which C_f is the capacitance of the output filter and K_{p1} is the outer loop gain. The root of closed-loop system is placed at zero to achieve the deadbeat effect. The outer voltage loop gain is thus designed to be

$$K_{p1} = \frac{C_f}{T_s} \tag{2.19}$$

According to the parameter listed in table II, K_{p1} should be designed to be 0.5.

However, the proportional gain of outer loop can not be designed to be very big because the inner loop transfer function has a near-zero-pole. The increase of the P controller gain will make system unstable. But a small P gain will cause a relatively big steady-state error. So we can use a quasi-proportional resonant controller [65] here to provide high gain at fundamental frequency or harmonic frequencies thus reduce the steady state error. The expression is as follows:

$$G_V(s) = K_{p2} + \frac{2K_C\omega_C s}{s^2 + 2\omega_C s + \omega_0{}^2} \tag{2.20}$$

, in which ω_c is the equivalent bandwidth of the controller and K_C is the resonant gain; ω is

the frequency that needs a high gain on it. ω_c needs to be set as small as possible because a large ω_c will introduce a phase lag towards the cross-over frequency thus decrease the phase margin. The final designed parameters are: $\omega_c = 10rad/s, K_c = 50, K_{p2} = 2, \omega_0 = 377rad/s$. The comparison of simulation results with P controller and PR controller will be shown at last. In this proposed controller, the load current and capacitor voltage have been decoupled, so the inner loop becomes a first-order system. The outer loop gain can be designed to be a relatively large value. So the steady state error of the proposed P controller can also be limited to a very small range at both constant load or varied load condition, which can also be demonstrated by the simulation results at the last part. In order to simplify the control, P controller is preferred to be used here.

2.4.3. Demonstration of its advantage

2.4.3.1. Steady state performance

With the designed parameter, the proposed system could maintain a small steady state error compared to others. Without capacitor current inner loop while with outer voltage loop by using PI controller, the closed loop transfer function is

$$V_C(s) = \frac{K_{p2}(K_{p1} + K_{i1}/s)}{s^2 L_f C_f + sC_f r_f + ((K_{p1} + K_{i1}/s)K_{p2} + 1)} V_{cref}(s) = G_{vI}(s)V_i(s) \quad (2.21)$$

With current inner loop while without output voltage and load current decoupling, the closed loop transfer function is

$$V_C(s) = \frac{K_{p1}K_{p2}}{s^2 L_f C_f + sC_f(r_f + K_{p2}) + (K_{p1}K_{p2} + 1)} V_{cref}(s) = G_{vII}(s)V_i(s) \quad (2.22)$$

With current inner loop and also with output voltage decoupling and capacitor current Negative decoupling:

$$V_C(s) = \frac{K_{p1}K_{p2}}{s^2 \cdot 2L_f C_f + s(2r_f + C_f K_{p2}) + (K_{p1}K_{p2})} V_{cref}(s) = G_{vIII}(s)V_i(s) \quad (2.23)$$

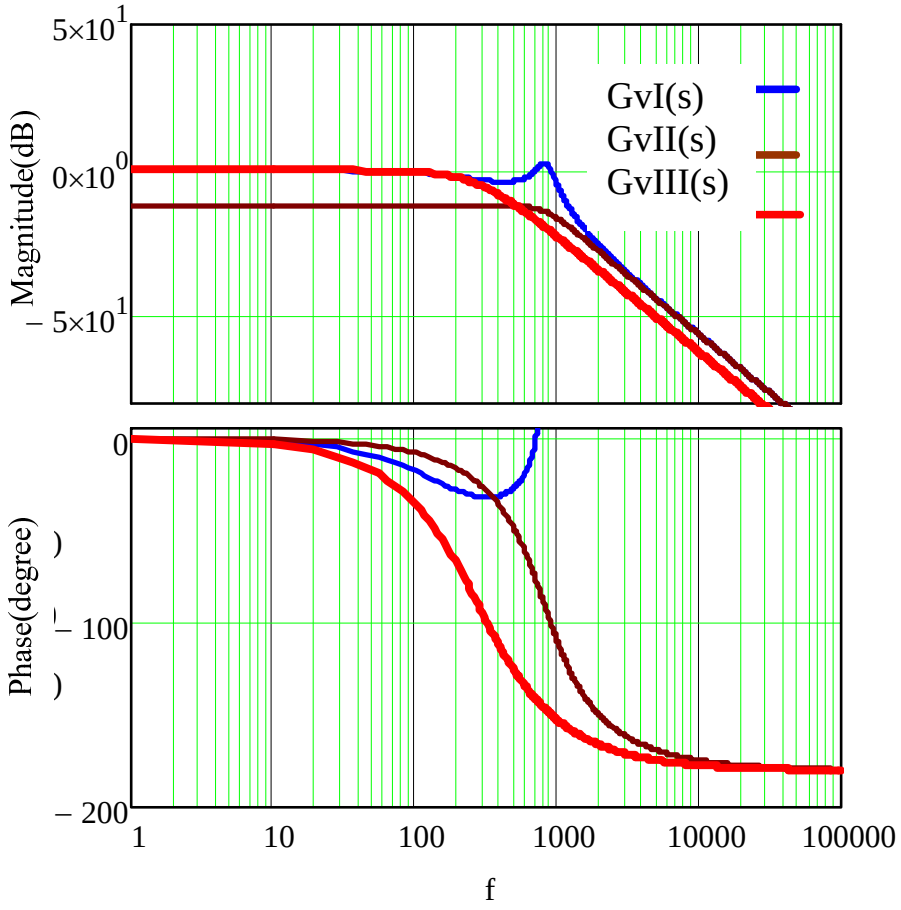


Fig.2.20. Bode plot of the closed-loop transfer function from voltage reference to output voltage with three control strategies

The bode plot of the control to output transfer function has been shown in Fig. 2.20. Table II lists the controller gain used for the outer and inner loop. The PI controller parameters for the first case are $K_{p0} = 0.05, K_{i1} = 300$. If estimated value of $\hat{L}_f, \hat{r}_f, \hat{C}_f$ are accurate, the controller will exhibit perfect tracking capability up to the bandwidth of the outer voltage loop. Without capacitor current loop, there is resonant peak at the corner frequency of L-C filter. Without V_C and I_o decoupling, the output can not track the reference well. Also both of them have relatively high gain at high frequency. The proposed control method exhibits very small tracking error at both low frequency and also exhibits low gain at high frequency. So it can reduce the tracking error and lower the THD component in the output voltage

very small tracking error at both low frequency and also exhibits low gain at high frequency. So it can reduce the tracking error and lower the THD component in the output voltage waveform.

2.4.3.2. Output Impedance

The closed-loop output impedance depends on the circuit configuration and also the control strategy. In this proposed controller, the output impedance can be expressed in equation (21) and the bode plot is shown in Fig. 2.21.

$$\left|\frac{v_c}{i_o}\right| = \frac{sL_f + R_f}{s^2 \cdot 2L_f C_f + s(K_{p2}C_f + r_f C_f) + K_{p1}K_{p2}} \tag{2.24}$$

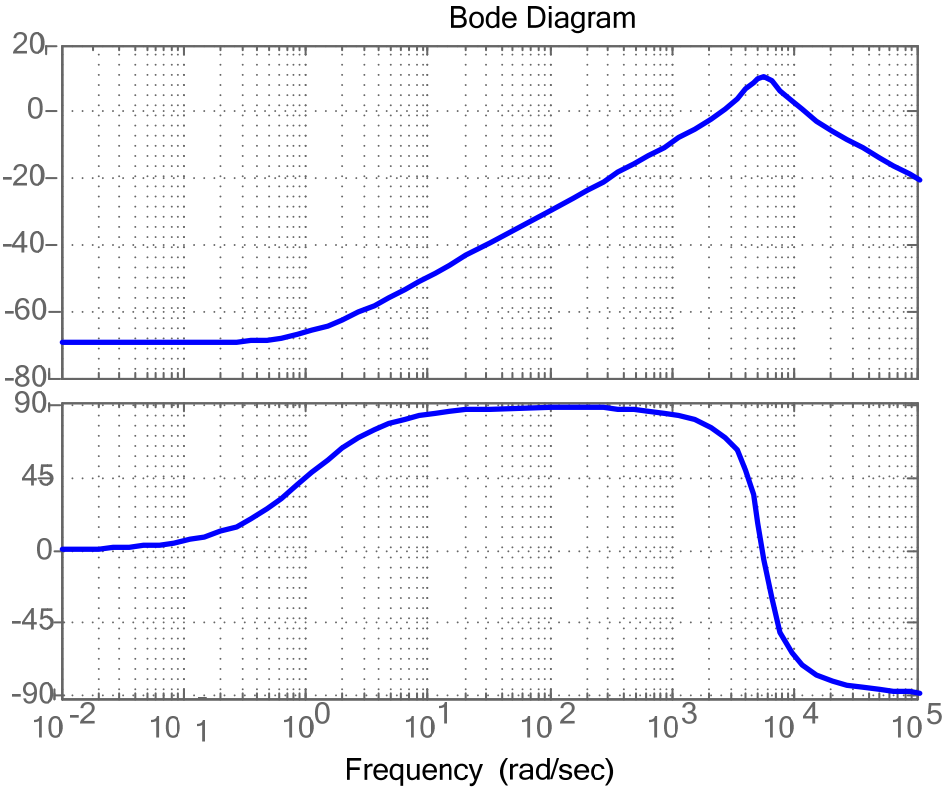


Fig. 2.21.Output impedance of stand-alone system

The impedance phase at fundamental frequency 60Hz is 90 degrees. It means it has nearly pure inductance characteristics.

2.5. Simulation and experimental results

The simulation and experimental verifications of the proposed control scheme were carried

out on a 3-kVA system. A DSP-based three-phase inverter is implemented to verify the proposed multiple-loop control scheme. An experimental prototype using a digital signal processor TMS320LF2407 digital controller is built. The sampling frequency of the output voltage and the PWM switching frequency are both 10kHZ. The reference command of outer voltage is a sampled sinusoidal wave table stored in the program memory of DSP. Table I lists the specifications of the inverter used in the tests. Table II lists the controller gains used. The inverter was designed to operate over a 200V dc bus. The filter inductor was designed such that the switching frequency current ripple is within 30% of rated current.

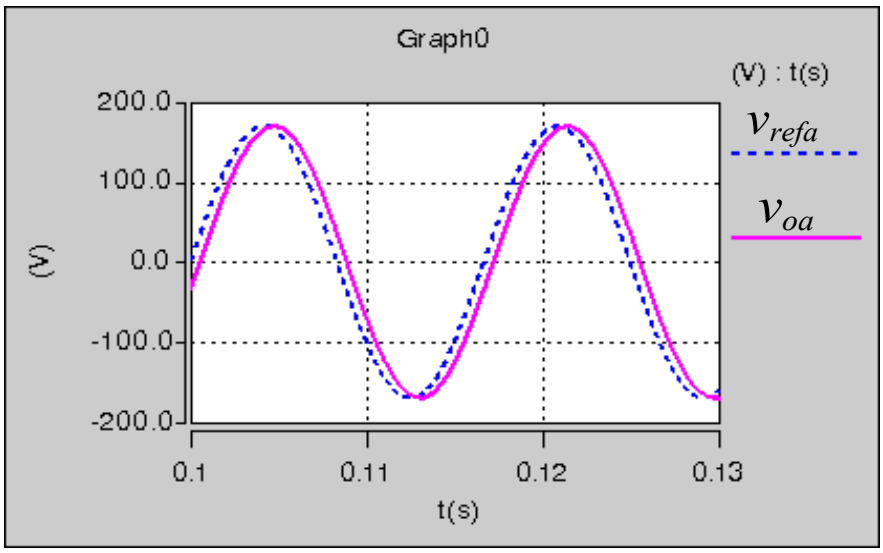
Table 2-1.System specifications

Switching frequency	10 kHz
Rated Output frequency	60 Hz
Dead time	1.5μs
DC-link voltage	200V
Output phase voltage(rms)	60V
Output capacity	3 k VA
Filter inductor and resistor (L_f , R_f)	1 mH, 1mΩ Y con.
Filter capacitor (C_f)	50 μF, Y con

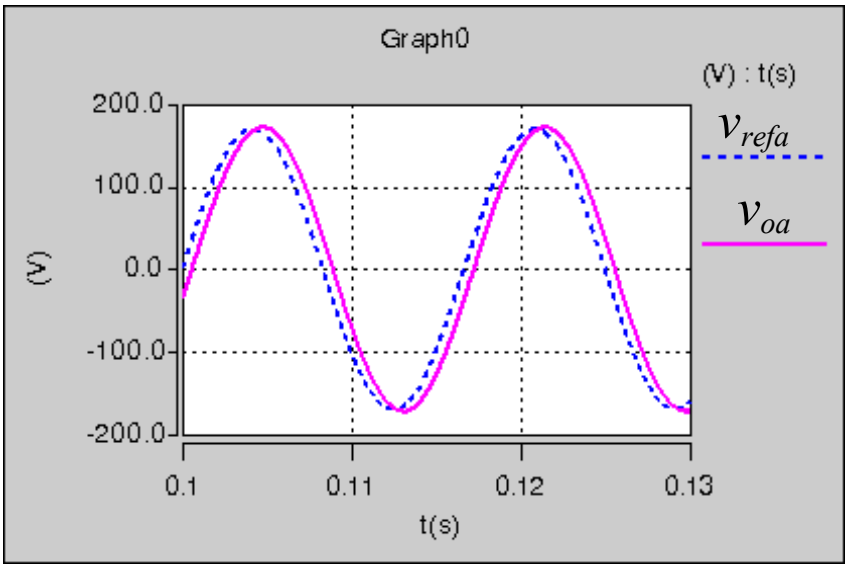
Table 2-2.Controller gains and parameters

Inner loop gain K_{p2}	6
Outer loop gain K_{p1}	0.5
Low pass filter cutoff frequency ω_c	6280 rad/s

2.5.1. Simulation Results



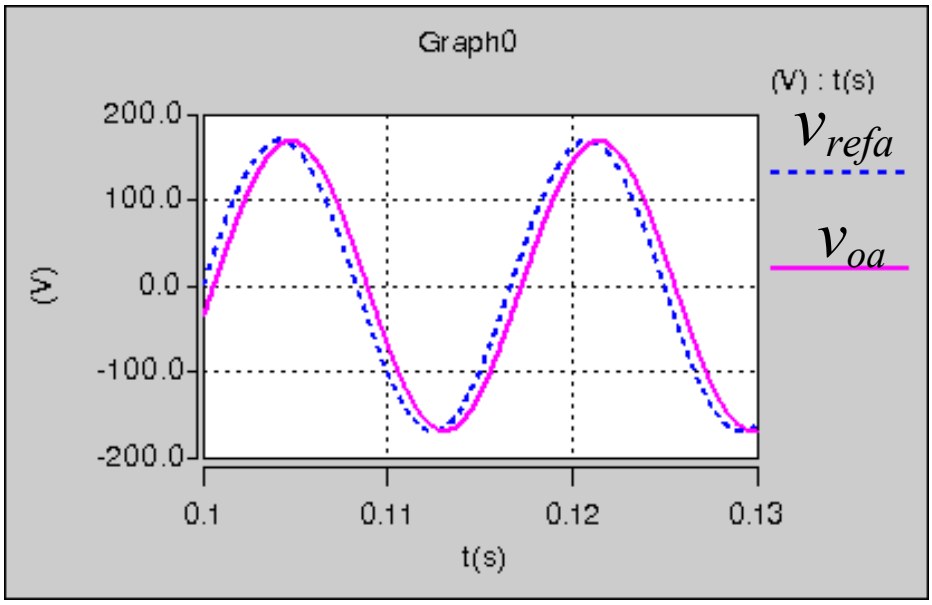
(a) $R = 100\,\Omega$ (Y con.) with CVDF



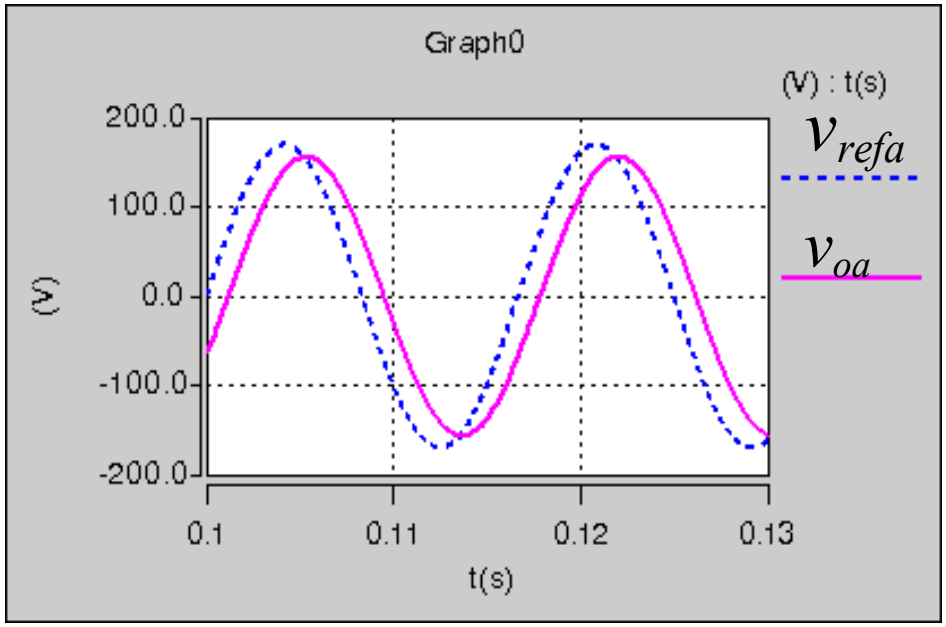
(b) $R = 5\,\Omega$ (Y con.) with CVDF

Fig. 2.22. Simulation results for output voltage (pink one) and reference voltage(blue one) at (a-b) capacitor voltage differential feedback (CVDF) (c-d) inductor current feedback (ICF)

Fig. 2.22 (cont'd)



(c) $R = 100\,\Omega$ (Y con.) with ICF



(d) $R = 5\,\Omega$ (Y con.) with ICF

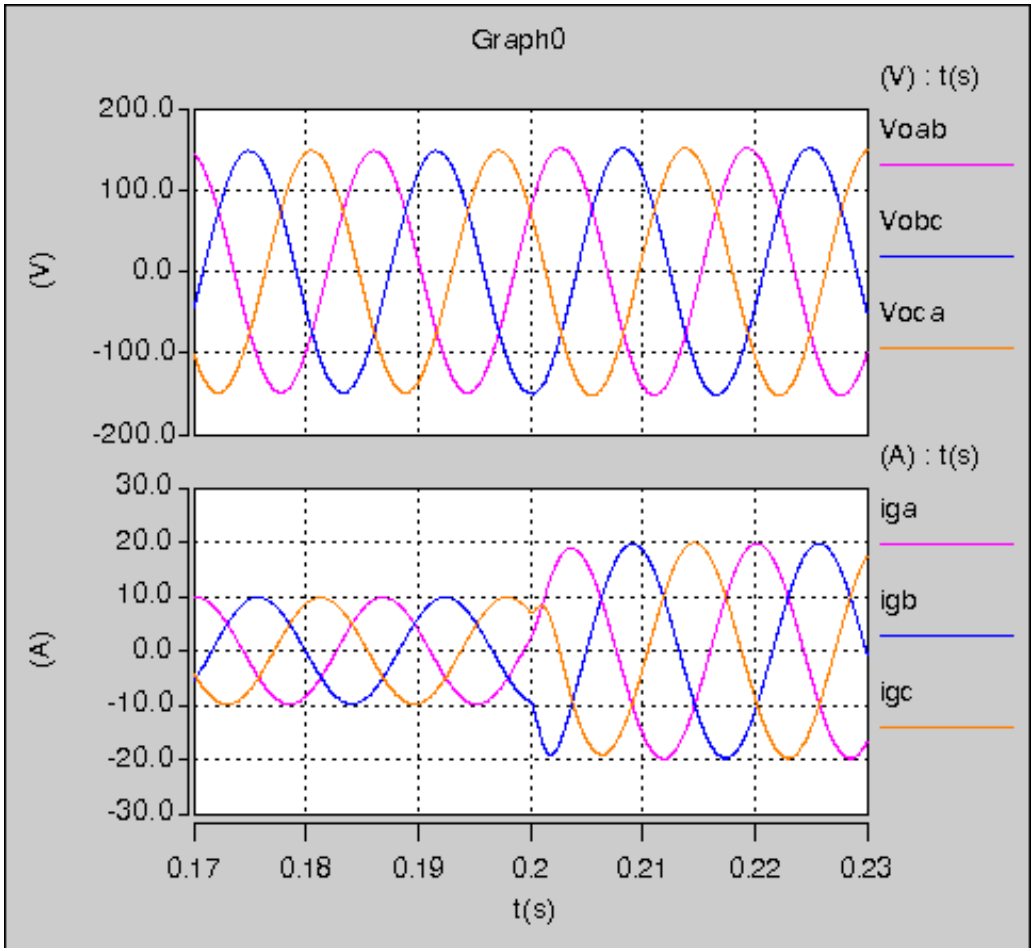


Fig.2.23. Output voltage and current with RL load of PF=0.5: $R = 5\Omega, L = 23mH$ with the multi-loop controller with voltage differential and load voltage current decoupling with only output voltage feedback

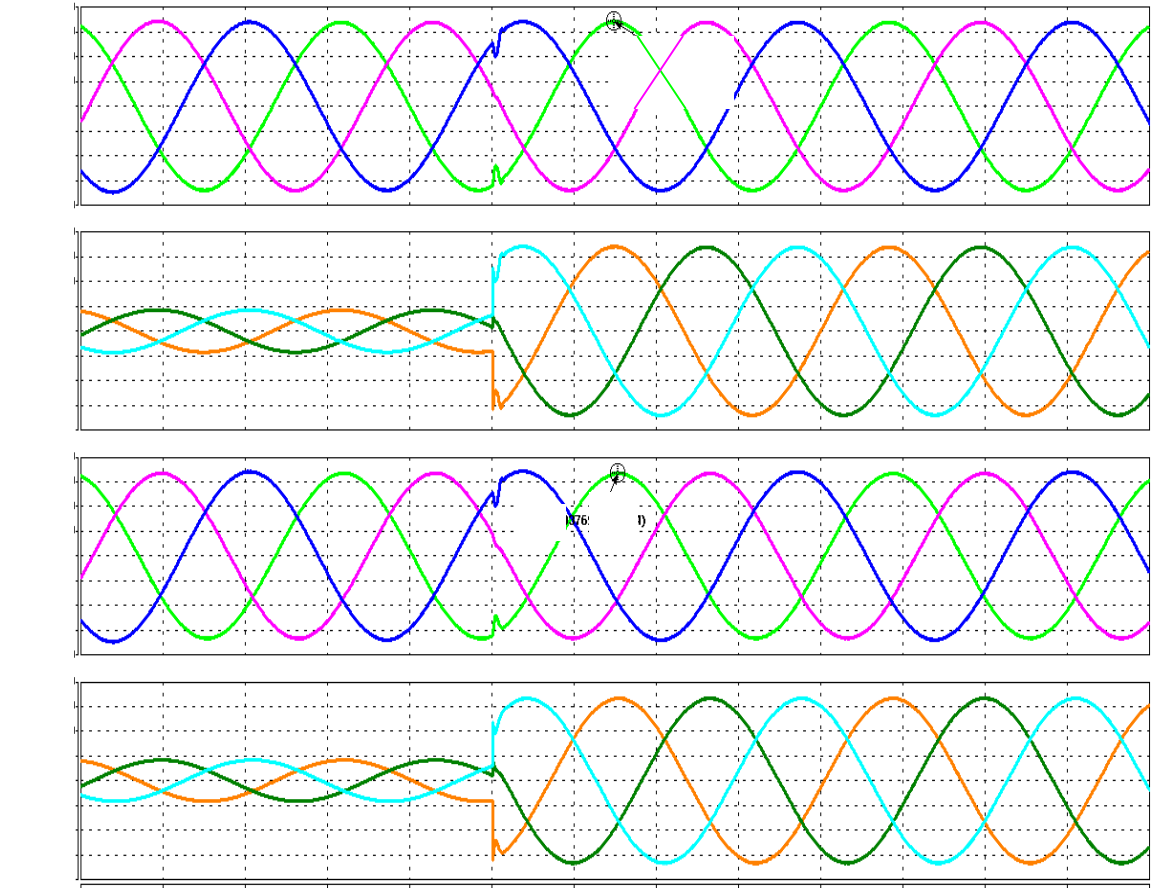


Fig.2.24. Transition response (output voltage and current) for step-load change- from 20Ω to 5Ω (from light load to full load) using (a) PR controller (b) PI controller for the decoupled multi-loop controller

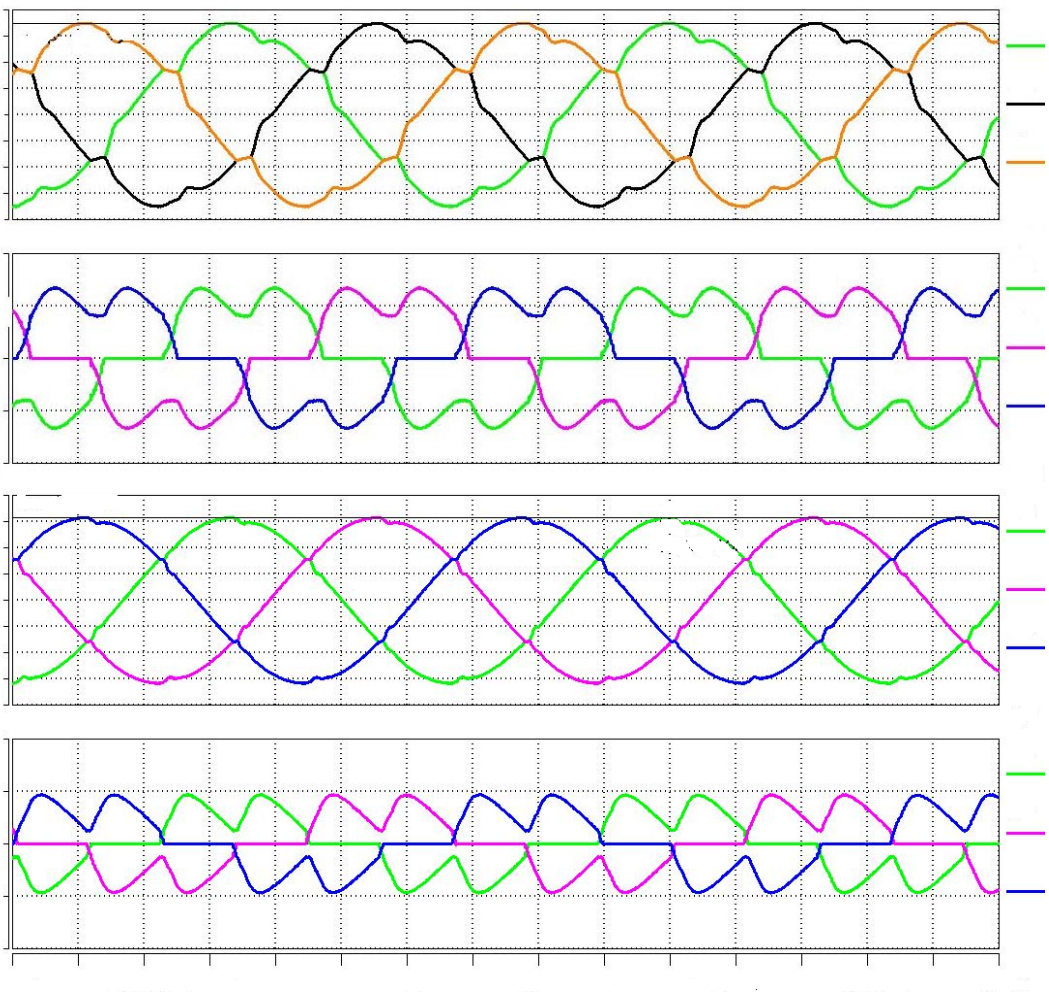


Fig.2.25. Simulation results for three phase rectifier load: output voltage and current (a) With proposed control strategy (b) Without load current decoupling (c) Without load voltage and load current decoupling

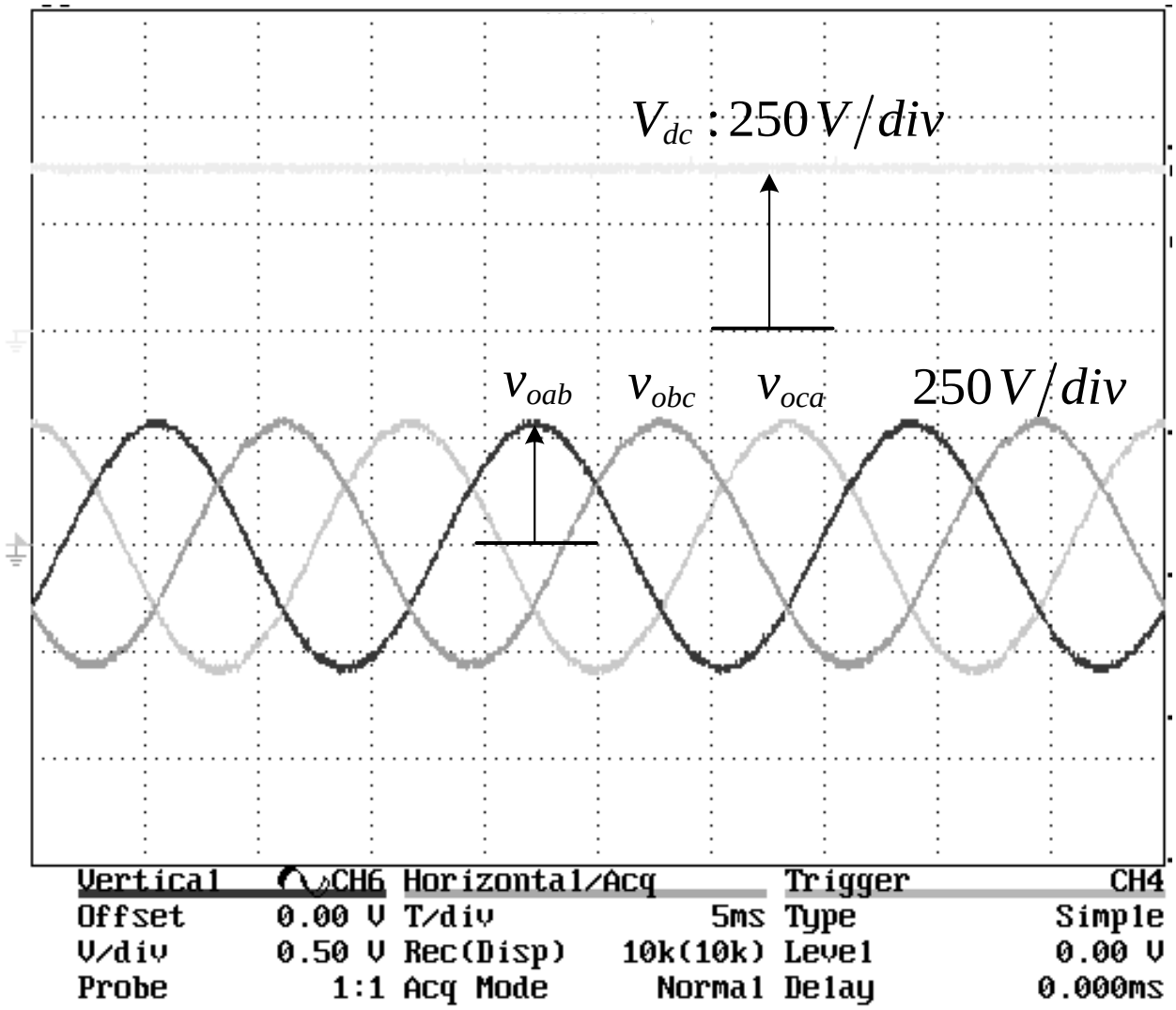
Fig. 2.22 compares capacitor voltage differential feedback control scheme and inductor current feedback control scheme with respect to the simulated output voltage at various load condition. It shows that the former scheme has much better stiffness to the load disturbance.

The simulation performances of the multi-loop controller which has both voltage differential feedback and voltage and current decoupling in the inner loop have been shown in Fig. 2.23-Fig. 2.25. The experiment results with low power factor load have been shown in Fig. 2.23. It shows that it can still achieve low THDs even with a low power factor load. Fig. 2.24 shows the dynamic response when the load changed from a light load to full load. As

shows the dynamic response when the load changed from a light load to full load. As expected, very fast dynamic response is obtained with the proposed controller. Fig. 2.25 compares the results under nonlinear load with the proposed controller and other two controllers (b) without load current decoupling (c) without both voltage and current decoupling. It can be shown that the proposed controller has lower THD in the output voltage waveform compared to the second case and also has much lower tracking error compared to the third case.

2.5.2. Experimental Results

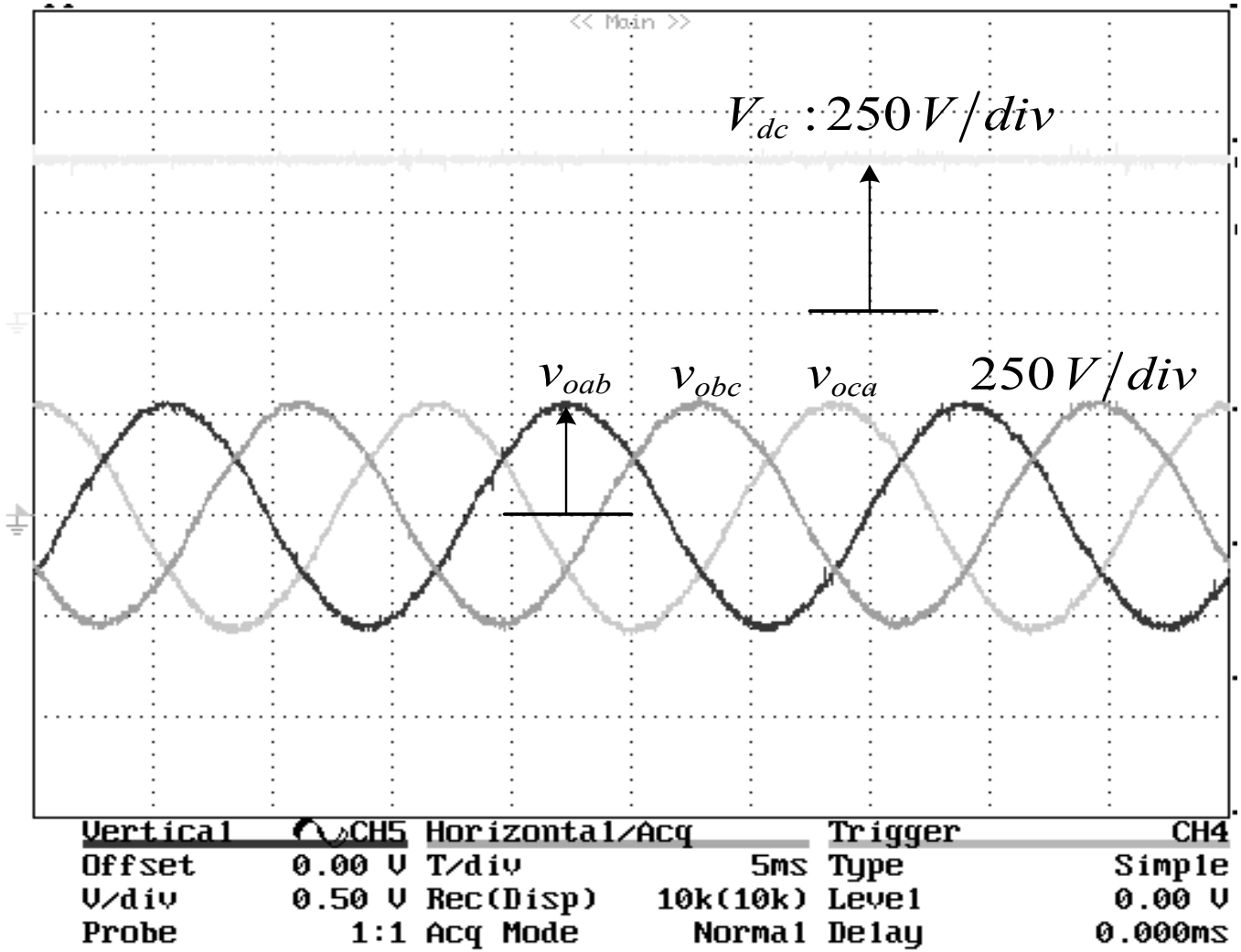
Fig. 2.26 (a) (b)(c)(d) shows the steady-state load voltage and DC voltage waveforms of the inverter at different load conditions. (a)(b)(c) shows the input dc voltage and output line to line voltage at different resistive load. (d) shows the output line to line voltage and phase a current at rectifier nonlinear load. These figures indicate that the proposed control strategy is capable of producing a nearly perfect sinusoidal load voltage with small steady-state error. Also shown in those figures is that the load current has no appreciable influence on the voltage loop performance. With nonlinear load, the output voltage THD is within 2.6%. Fig. 2.27 shows the dynamic response of the inverter system for 100% step change in the load from no load to full load. The figure shows the system exhibits very fast dynamic response with excellent load voltage regulation from no-load to full-load and with very little change in the load voltage at the point of applying the full load, indicating that the control scheme ensures a “stiff” load voltage.



(a) $R = \infty$

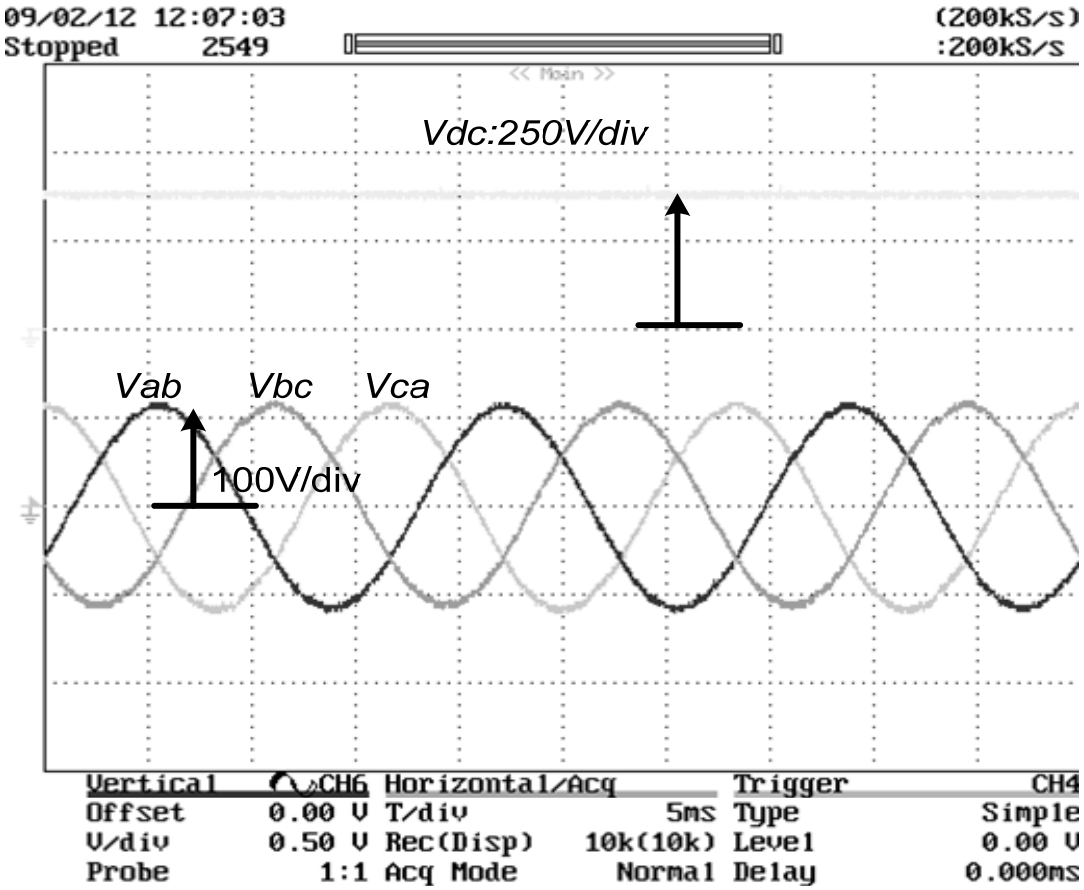
Fig. 2.26. Experimental results in standalone mode

Fig. 2.26 (cont'd)

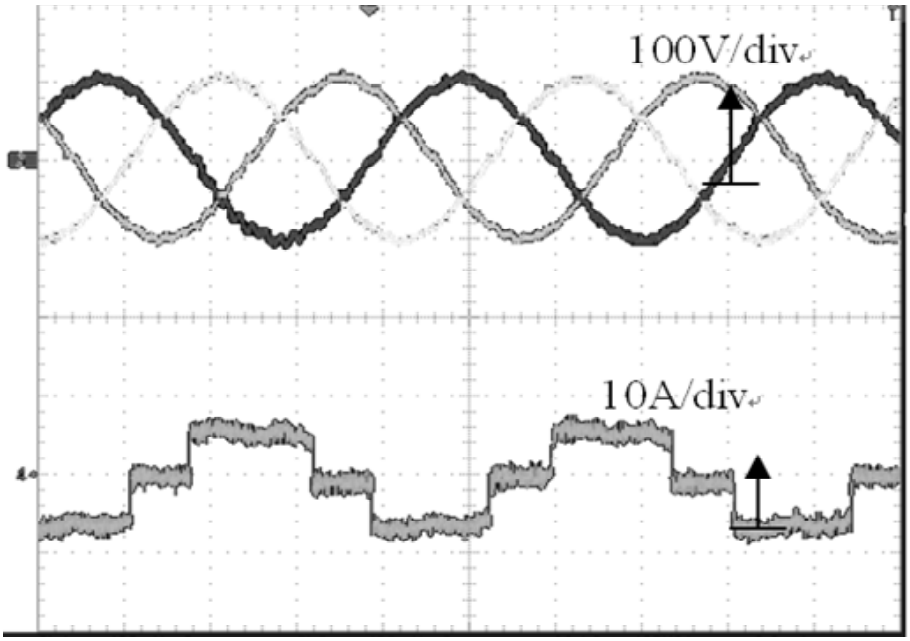


(b) $R = 10\,\Omega$

Fig. 2.26 (cont'd)



(c) $R = 5\,\Omega$



(d) Nonlinear Load

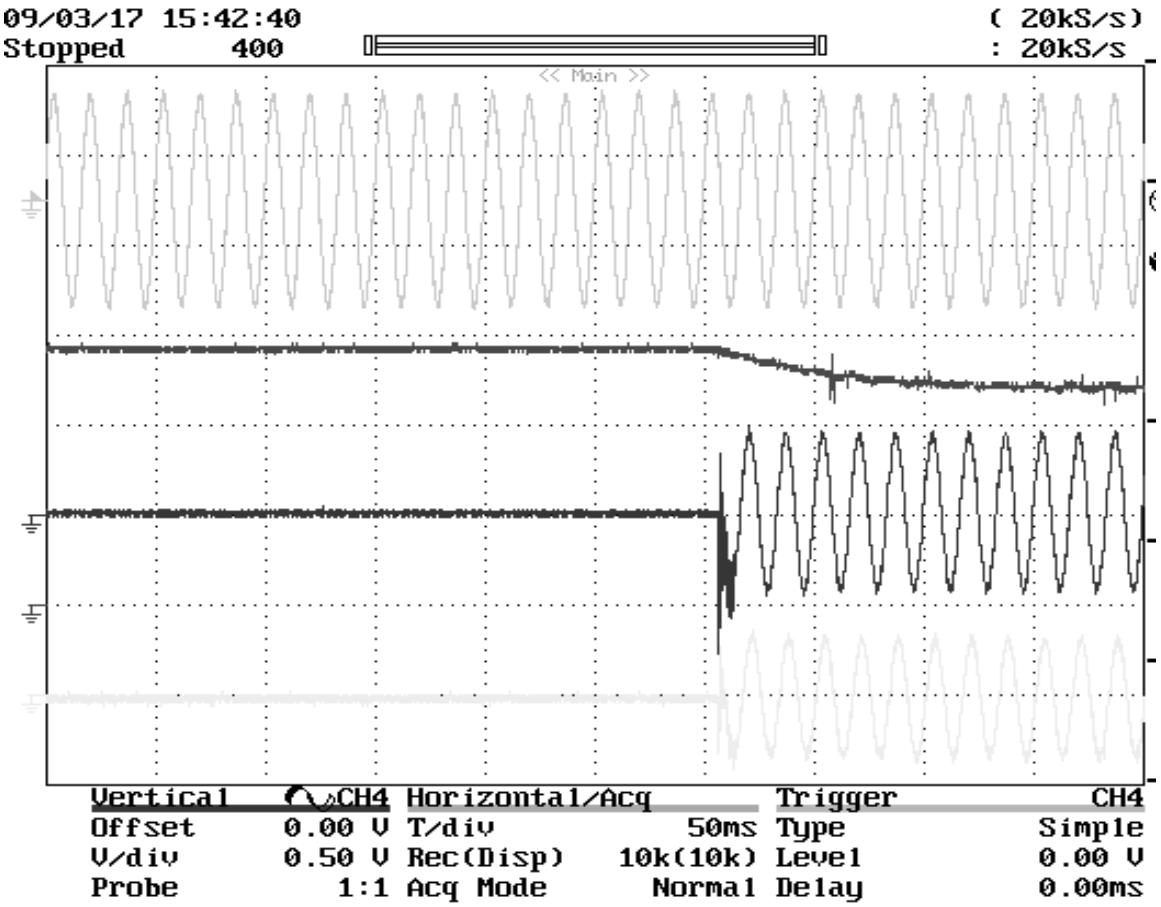


Fig.2.27. Load change from no load to $R = 5\Omega$

2.6. Summary

The proposed control strategy for standalone mode of grid-connected inverter is capable to achieve high-quality dynamic and steady state performances under both linear and non-linear loads. Moreover, its design is also simple and requires only an accurate knowledge of output filter parameters. Finally, only the output voltage needs to be sensed provided that dc-link voltage is constant. The results of the simulations and experiments demonstrate that the proposed controller can achieve low THD at nonlinear load and fast dynamic response at load step change.

CHAPTER 3 ROBUST CURRENT CONTROL SCHEME FOR MICRO-GRID INVERTER GRID-CONNECTED OPERATION

3.1. Introduction

In grid-connected DG systems, single-phase or three-phase pulse-width modulation (PWM) voltage-source inverters (VSIs) are often used for interfacing the renewable energy source to the utility grid [66],[67], and the current control of the grid-connected inverters plays a predominant role in feeding a grid with high-quality power.

The stationary reference frame proportional-integrator (PI) controller, also called the ramp comparison current controller, is commonly used for current controlled inverters because of its simplicity and easy implementation [68],[69]. Nevertheless, it is regarded as a unsatisfactory solution for ac current regulation because of large steady-state tracking error. Through this tracking error can be reduced by increasing the PI gain and bandwidth, unfortunately, it will also push the systems towards their stabilitiy limits. In contrast, the synchronous frame PI controller can theoretically achieve zero steady-state tracking error by shifting the base-band information back to dc, however, it requires significant computation arising from the need for multiple reference frames [69]-[71], [77]. Also it's difficult to be applied to single-phase inverters. The newly developed proportional-resonant (PR) can achieve virtually the same steady-state and transient performance as a synchronous frame PI controller for both single-phase and three-phase inverters, which is a potential candidate for the grid-connected inverters [72]-[75].

When connecting the inverter to the utility grid, either a pure inductor (L) or a LCL filter can be used as the inverter output stage. The LCL filter instead of L filter is more attractive because it can not only provide higher high-frequency harmonics attenuation with the same inductance value, but also allow the inverter to operate in both standalone and grid-connected modes, which makes it a universal inverter for DG applications [79]. However, the system

incorporating LCL filters is of third order, and it has an inherent high-resonant peak at the resonant frequency of the LCL filter, which will make the current control instable if the controller is not suitably designed. To avoid this stability problem, the passive or active damping methods are usually needed [76]-[78].

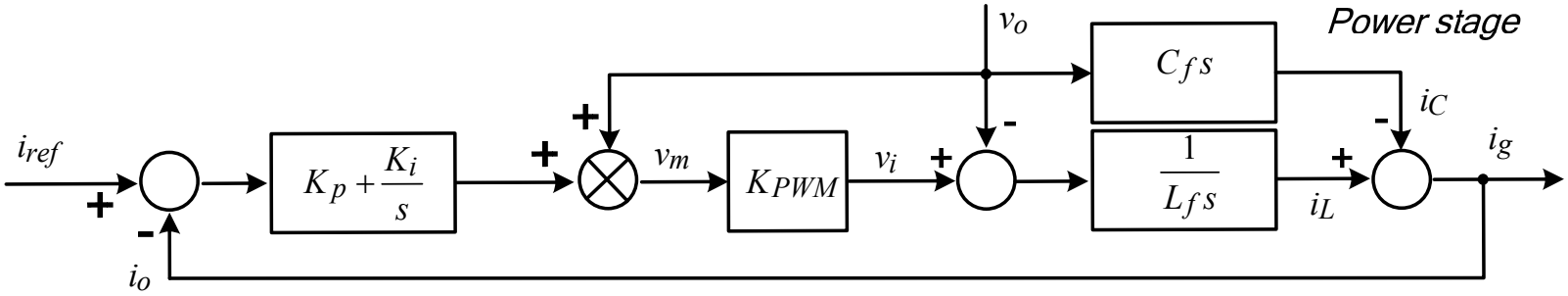
In [79], [80], an admittance compensator along with a quasi-resonant-proportional controller was proposed. Using the inverter output current instead of the grid current as the feedback signal, the control system can be simplified to a first-order system thus it is possible to keep the control loop stable with high loop gain and bandwidth. However, from the whole system view, the filter capacitor and the grid-side inductor form a parallel resonant circuit, and harmonic current from inverter output in the vicinity of resonant frequency can be amplified excessively and may cause the resonance of the grid current. Reference [81] proposed a new control strategy with feedback of grid current plus part of the capacitor current. In this way, the inverter control system can also be degraded from third-order to first-order due to the counteraction between zeros and poles. The main drawbacks of this method are that the grid current is not directly controlled and will be affected by capacitor current, moreover, the zeros counteract poles only when the values of both inverter-side inductor and grid-side inductor are well known, which is difficult in practice since the grid impedance is different depending on the grid stiffness, and changes with time, furthermore, it is hard to estimate. Alternatively adding a large inductor in grid side will make the variations of grid impedance relatively smaller, but it's not a cost-effective solution since manufactures tend to minimize the number and volume of the magnetic components. In fact, large grid impedance variation will seriously affect the performance of the current control, challenging the control of grid-connected inverter and the grid filter design in terms of stability. A theoretical analysis of the grid stiffness influence on current control is given in [82].

Taking the grid impedance into consideration, in the condition that the grid impedance is big enough when compared to the filter capacitor impedance at the switching frequency, the grid-side filter inductor can be eliminated, in other words, we can use LC filter instead of LCL filter to reduce one filter inductor. By optimally selecting the value of filter capacitor, this condition is easy to be satisfied since the total grid-impedance includes the line impedance and the internal impedance of the grid, in some applications, a transformer is used to couple the inverter to the grid which will equivalently increase the grid impedance.

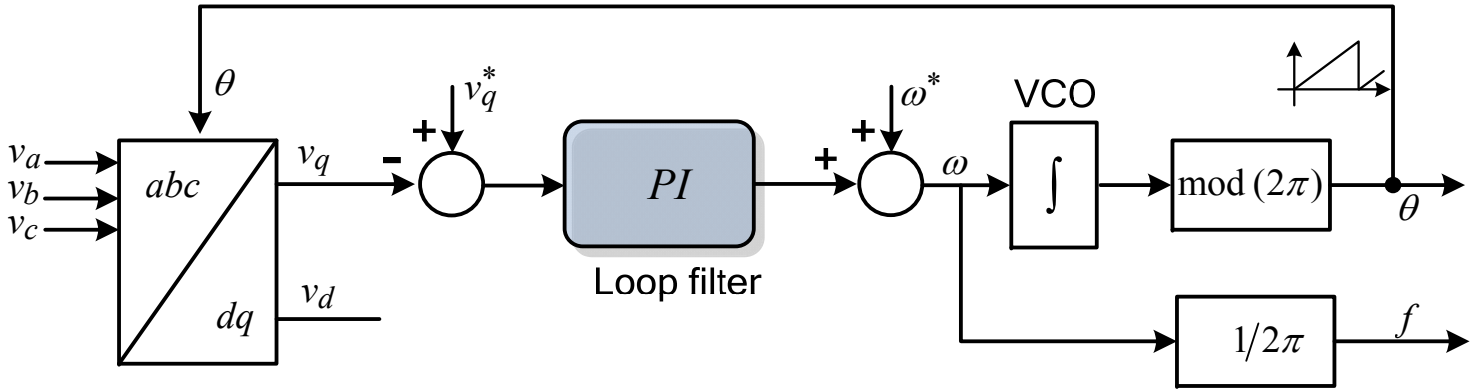
To address all the aforementioned issues, this paper proposes a robust control scheme for grid-connected voltage source inverters with LC filters. The objective is to achieve small steady-state tracking error and low total harmonic distortion (THD) of the grid current while keep the system stable in the predefined variation ranges of the grid impedance. In the beginning, this paper analyzes the stability problems of the conventional current controlled inverters caused by the possible grid-impedance variations. To deal with this stability problem, an H∞ controller with the explicit robustness in terms of grid impedance variations is proposed to incorporate the desired tracking performance and stability margin. By properly selecting the weighting functions, the synthesized H∞ controller exhibits high gains at the vicinity of the line frequency, similar to the traditional proportional-resonant (PR) controller, and enough high frequency attenuation to keep the control loop stable. An inner inverter-output-current loop with high bandwidth is also designed to get better disturbance (e.g. dead time effect) rejection capability. The selection of weighting functions, inner inverter-output-current loop design, and system disturbance rejection capability are discussed in detail in this paper. Both simulation and experimental results of the proposed H∞ controller as well as the conventional PI controller are given and compared, which validates the performance of the proposed control scheme.

3.2. Current control strategy for grid-connected mode

The Fig. 2.1 shows the configuration of the three-phase grid-connected VSI with LC filters, using LC filters. When the inverter operates in grid-connected mode, the solid state relay is turned on. The system parameters are as follows: $L_f = 1\,mH, C_f = 50\,\mu F$, the cut-off frequency $f_C = \frac{1}{2\pi\sqrt{LC}} = 712\,Hz$, $V_{dc} = 400V$, $f_S = 10\,kHz$, output phase voltage 120 V, frequency of output voltage $f_O = 60\,Hz$.



(a)



(b)

Fig.3.1.Block diagram of (a) the closed-loop current control, (b) three-phase PLL for grid synchronization.

The control strategy of the grid-connected inverter is shown in Fig. 3.1, where the line impedance and grid internal impedance are ignored, the output voltage v_o is equal to grid voltage v_g. By using dc-link voltage feed forward, we can keep $K_{PWM}=1$. Without considering the control delay, one has

$$\begin{aligned} I_g(s) &= \frac{K_p s + K_i}{L_f s^2 + K_p s + K_i} I_{ref}(s) - \frac{L_f s^2}{L_f s^2 + K_p s + K_i} I_C(s) \\ &= \frac{K_p s + K_i}{L_f s^2 + K_p s + K_i} I_{ref}(s) - \frac{L_f C_f s^3}{L_f s^2 + K_p s + K_i} V_O(s) \\ &= G_{iref\_ig}(s) I_{jref}(s) - D_{vo\_ig}(s) V_O(s) \end{aligned} \tag{3.1}$$

From (1), we can plot the bode diagrams of $G_{ref\_ig}(s)$, $D_{vo\_ig}(s)$ with $K_p=8, K_i=8000$, as shown in Fig. 3.2.

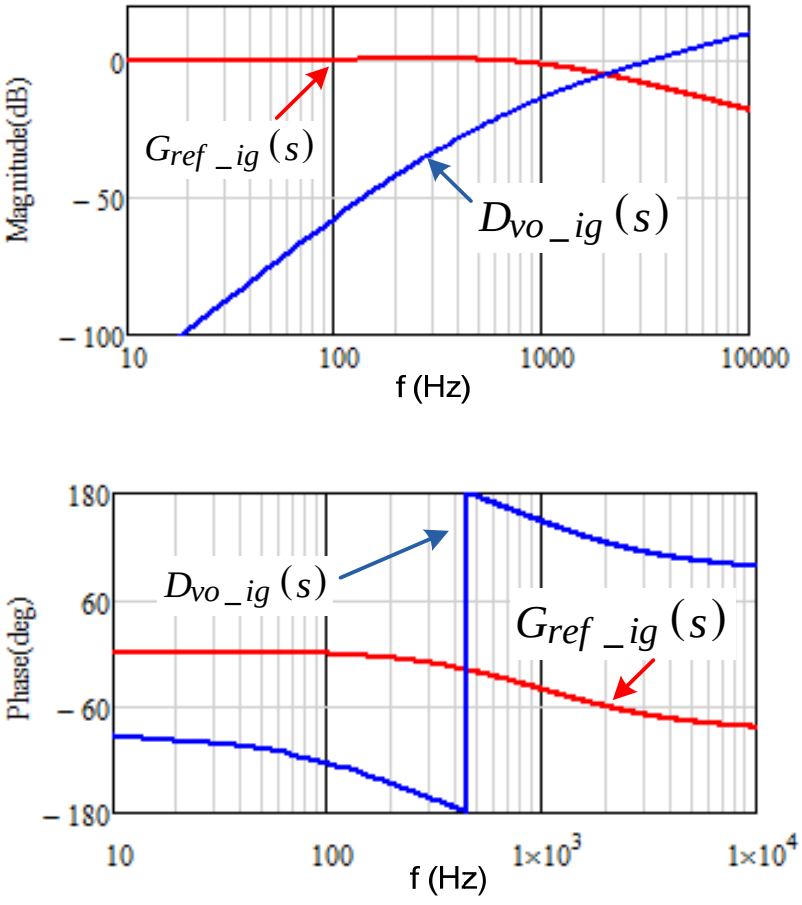
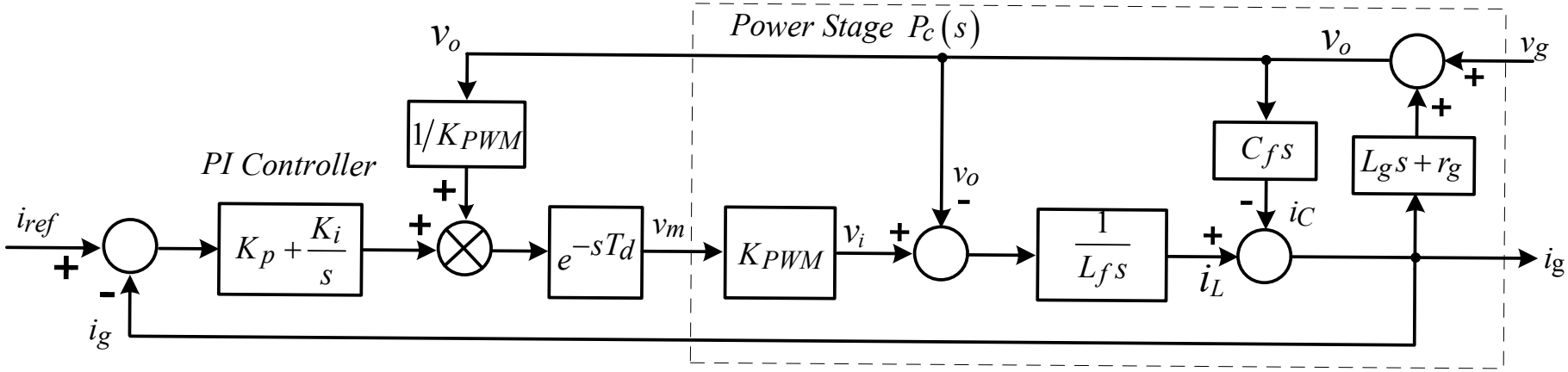
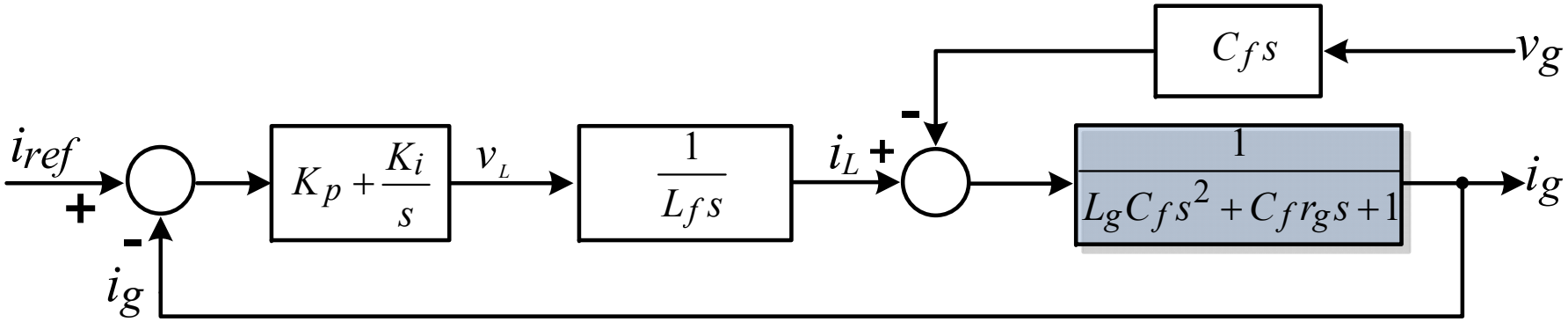


Fig.3.2. Bode diagrams of $G_{ref\_ig}(s), D_{vo\_ig}(s)$.

The influence of the grid-impedance variations on the current control is investigated and disscussed based on the stationary reference frame PI controller along with a capacitor voltage v_o feed-forward compensator, as shown in Fig. 3.1, where K_{PWM} is the inverter gain, which can be regarded as unity by measuring the dc-link voltage, e^{-sTd} represents the control delay, T_d is equal to one switching period in this paper, and v_m is the modulation signal. Here feed-forward controller is employed to reduce the effect of the grid voltage and to increase dynamic response [69], [73]. Fig.3.3 (b) shows the simplified control blcok diagram corresponding to Fig. 3.3(b) without considering the control delay.



(a)



(b)

Fig.3.3. (a) block diagram of the PI controller along with the capacitor voltage feed-forward compensator, (b) simplified control block diagram.

Table 3-1.System parameters

	Parameter	Value
Grid	Grid phase voltage	120 V_{RMS}
	Frequency	60 Hz
	Grid resistance r_g	$\in[0.1, 0.5]\,\Omega$, with nominal value $0.2\,\Omega$
	Grid inductance L_g	$\in[0.05, 0.3]\,mH$, with nominal value $0.15\,mH$
Inverter	Rated Power	5 kVA
	Switching Frequency	10 kHz
	Sampling frequency	10 kHz
	L_f	1 mH (4.4% p. u.)
	C_f	50 μF (6.1 p. u.)

Before embarking on studying the influence of grid impedance on the current control loop, let us consider the grid impedance Z_g is small enough and can be ignored first. Without considering the grid impedance, the output voltage v_o is equal to the grid voltage v_g, the current-loop transfer function is the same as an L-filter based inverter. Assuming K_{PWM}=1, the following closed-loop transfer function of the grid current can be obtained as:

$$\begin{aligned} I_g(s) &= G_{iref\_ig}(s) I_{ref}(s) - Z_{vg\_ig}(s) V_g(s) \\ &= \frac{K_p s + K_i}{L_f s^2 + K_p s + K_i} I_{ref}(s) - \frac{L_f C_f s^3}{L_f s^2 + K_p s + K_i} V_g(s). \end{aligned} \tag{3.1}$$

where $G_{iref\_ig}(s)$ and $Z_{vg\_ig(s)}$ represent reference-to-grid current and grid voltage-to-grid current transfer functions, respectively. With $K_p = 3$, $K_i = 3000$, the crossover frequency of the open loop is set at 500 Hz, and the bode diagrams of

$G_{i_{ref}\_i_g}(s)$ and $Z_{v_g\_i_g}(s)$ are shown in Fig..

When considering the grid impedance Z_g, there will be an additional second-order transfer function $G_g(s)$ in the control loop as shown in the shadow area of Fig. 3.3(b),

$$G_a(s) = \frac{1}{L_g C_f s^2 + C_f r_g s + 1}. \tag{3.2}$$

Equation (2) can be written as the following normalized form:

$$G_a(s) = \frac{\omega_n^2}{s^2 + 2\xi_a \omega_n s + \omega_n^2} \tag{3.3}$$

where $\omega_n = 1/\sqrt{L_g C_f}$ is natural angular frequency, and $\xi_a = 0.5 r_g \sqrt{C_f / L_g}$ is the damping ratio. As is well known, for ξ_a less than one, the unit-step response of (3) will exhibit over-shooting and ringing, while the frequency response of (3) will have a resonant peak, so called "under damping". Specifically, if the line impedance Z_g is highly inductive, ξ_a will be close to zero, thus leading to high resonant peak and may causing the system instable. The stability problem will be more serious when L_g is large, resulting ω_n close to line frequency. With considering Z_g, the closed-loop transfer function of the grid current can be rewritten as

$$\begin{aligned} I_g(s) &= G'_{iref\_ig}(s) I_{ref}(s) - Z'_{vg\_ig}(s) V_g(s) \\ &= \frac{K_p s + K_i}{L_f L_g C_f s^4 + L_f C_f r_g s^3 + L_f s^2 + K_p s + K_i} I_{ref}(s) \\ &\quad - \frac{L_f C_f s^3}{L_f L_g C_f s^4 + L_f C_f r_g s^3 + L_f s^2 + K_p s + K_i} V_g(s) \end{aligned} \tag{3.4}$$

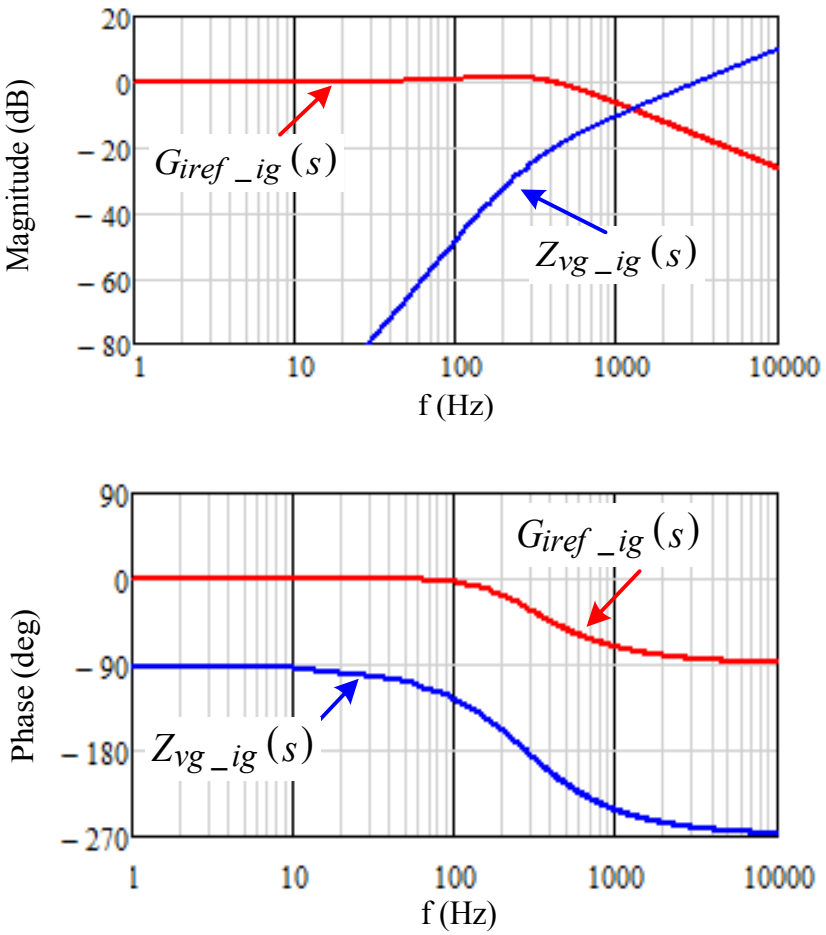


Fig.3.4. Bode diagrams of $G_{iref\_ig}(s)$ and $Z_{vg\_ig}(s)$.

Fig. 3.5 shows the root loci of the control system with (a) r_g=0.1 Ω and L_g changing from 1 μH to 100 μH, (b) L_g= 10 μH, 100 μH separately and r_g changing from1 mΩ to 1 Ω, where $K_p = 3, K_i = 3000$ and the arrow direction represents the corresponding value increasing. Fig. 3.5(a) reveals that with a constant r_g, as L_g increasing, the dominant roots of the characteristic equation move toward the right half-plane, while Fig. 3.5(b) depicts that with a constant L_g, as r_g increasing, the roots move toward the left half-plane and away the imaginary axis. Therefore, when grid impedance Z_g increases and keeps highly inductive, resulting a less damped system, the poles are attracted to imaginary or even right half-plane, which may cause the system oscillatory or even instable. In addition, even with the enough

damping ratio $\xi_a(\xi_a = 1)$, as both L_g and r_g increasing together, the poles are still attracted to the imaginary axis, resulting less stability margin, as shown in Fig. 3.6. Therefore, even with enough damping ratio, large value of L_g will still limit the system bandwidth and affect the system stability. In conclusion, the low-frequency gain and bandwidth will be seriously limited by large value of L_g, which will consequently decrease the tracking performance and disturbance rejection capability. Hence, large grid impedance variation is challenging the control of grid-connected inverter and the grid filter design in terms of stability.

It is notable that if we decrease the capacitance of C_f, with the same value of L_g, the natural frequency ω_n will increase and the system stability problem will be alleviated. Unfortunately, smaller C_f will increase the inverter output impedance in the stand-alone mode, thus increasing the THD of output voltage. In addition, the control delay between the sampling instant and duty-cycle update instant also decreases the stability margin of the system and strongly limits the bandwidth of the control loop [84]. Here we focus on analyzing the stability problem caused by the grid impedance variation, and we won't discuss the details of the control delay's impact on the system stability.

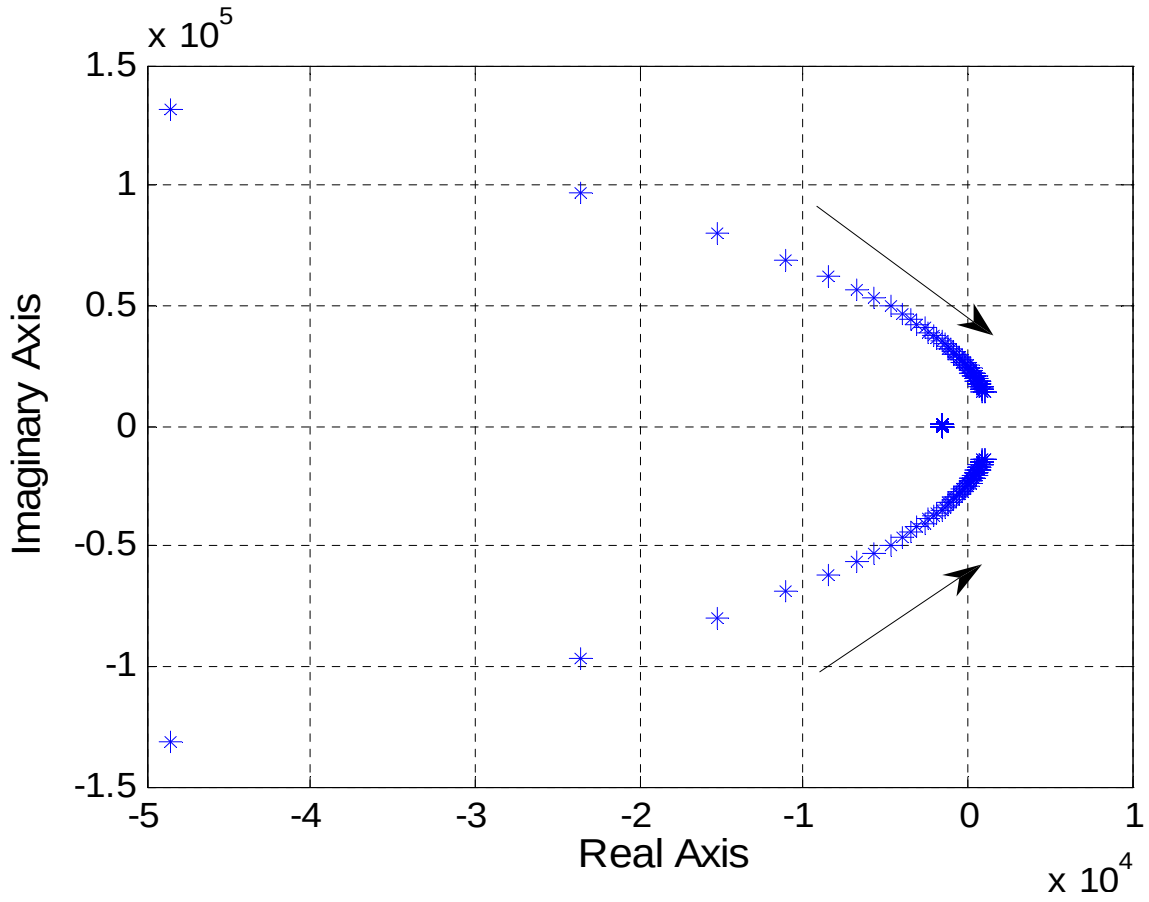


Fig.3.5. Root loci of the control system with $r_g = 0.1\Omega$ and L_g changing from 1 μH to 100 μH

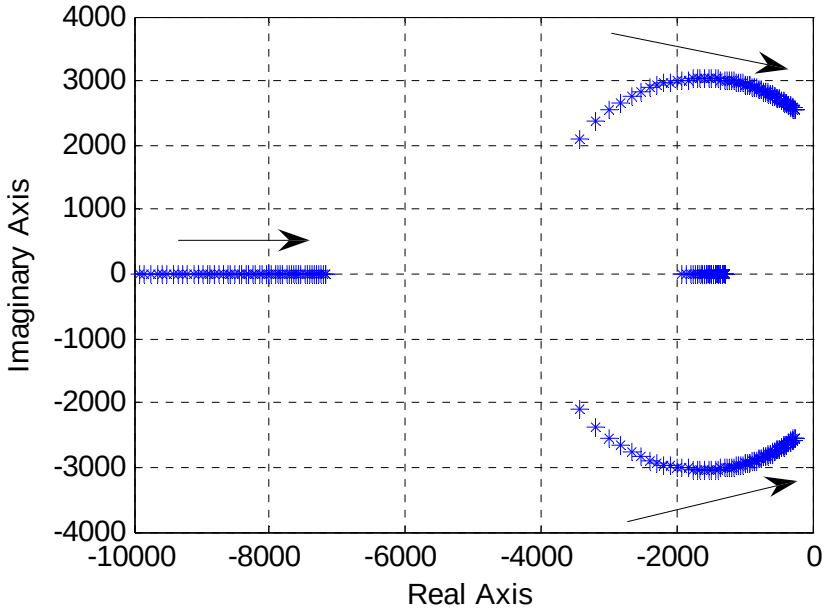


Fig.3.6. Root locus of the control system with L_g changing from 100 μH to 1 mH, and $\xi_a = 1$.

3.4. Design of the Robust Controller for Grid-connected Inverters [107]

To deal with the stability problem caused by the uncertainty of the grid impedance, an H∞ controller is proposed in this paper. The design goal is to get desired tracking performance, such as small steady-state tracking error and low THD of the grid current, while keep the system stable in the predefined variation ranges of the grid impedance as given in the Table. I. The H∞ control theory has been introduced in the early 1980s and opened a new direction in robust control design. Recently, this approach has been applied to the control of active power filters (APF), uninterrupted power supply (UPS), dc-dc boost converters, and dynamic voltage restorer (DVR) to effectively mitigate the effects of the uncertain parameters [85]–[89].

Fig. 3.7 shows (a) the proposed control block and (b) the standard H∞ control configuration with weighting functions. It's notable that $1/Lfs$ as shown in Fig. 3.3(b) is merged into the desired H∞ controller $K(s)$, then the H∞ controller only needs to deal with the uncertain second-order control plant, otherwise third-order control plant needs to be compensated, which will be more difficult. In Fig. 3.7 (a), i_d is the equivalent current disturbance, and the

design goal of $K(s)$ is to get both desired tracing performance and robustness in the predefined variation ranges of L_g , r_g . In Fig. 3.7 (b), $G_{aN}(s)$ is the nominal plant; z, y, w and u are the controlled output, the measured output, the exogenous input, and the control input, respectively, W_1, W_2, and W_3 are the weighting functions for tracking error performance, the weight on the controller transfer function, and robust performance, respectively. The H∞ controller synthesis is conducted by the singular value loop shaping using mixed-sensitivity approach. The objective is to synthesize the stabilizing controller $K(s)$ so that the H∞ gain from w to z is less than 1, i.e.,

$$\|T_{wz}\|_\infty < 1 \; or \text{ equivalently } \left\| \begin{matrix} W_1 S \\ W_3 T \end{matrix} \right\|_\infty < 1 \tag{3.5}$$

where $S(s) = 1/(1 + G_{aN}(s)K(s))$ is the sensitivity transfer function, and $T(s) = G_{aN}(s)K(s)/(1 + G_{aN}(s)K(s))$ is called the complementary sensitivity transfer function since they satisfy

$$T(s) + S(s) = 1. \tag{3.6}$$

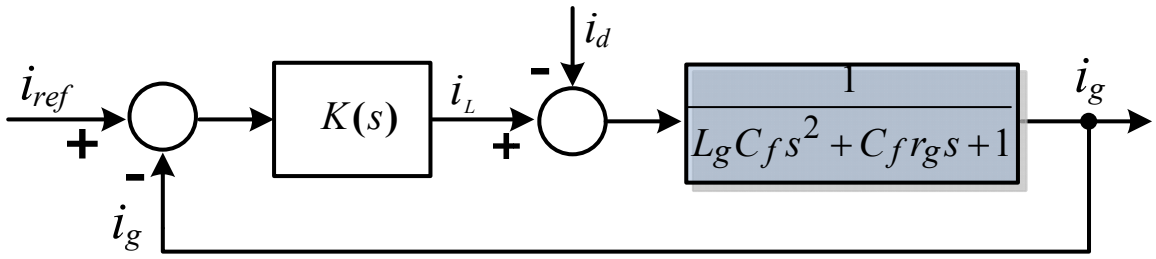
It can be seen from (5) that the mixed-sensitivity approach is simply the shaping of $T(s)$ (transfer function from reference to output, or closed-loop transfer function) and $S(s)$ (transfer function from reference to error), by properly selecting their respective weighting function W_1 and W_3, respectively. Typically, we would choose W_1 to have high gain inside the desired control bandwidth to achieve good disturbance attenuation (i.e., tracking performance), and choose W_3 to have high gain outside the control bandwidth, which helps to ensure good stability margin (i.e., robustness). W_2 is the weight on the controller transfer function. A small value (0.1) is assigned to W_2 to ensure the D_{12} matrix of the augmented plant is of full rank [88].

The H∞ loop-shaping design may be processed as following steps:

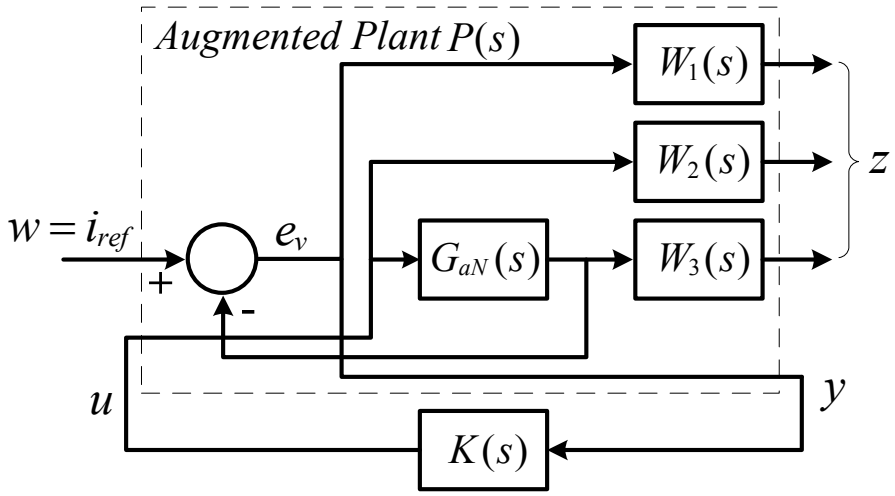
1) Make the proper selection of weighting functions

2) Perform a standard H∞ synthesis to obtain an adequate controller which makes the closed-loop system having the desired loop shapes.

3) Reduce the order of $K(s)$ for practical implementation while keep almost the same performance as the original controller.



(a)



(b)

Fig.3.7. (a) proposed robust control block, (b) standard H∞ control configuration with weighting functions.

3.4.1. Weighting Function Selection for Tracking Error Performance

According to the procedure described above, we consider the determination of weighting function W_1 first. Since the sensitivity transfer function $S(s)$ is the gain from reference to error, for the sinusoidal reference voltage, small tracking error means that the gain of $S(s)$ must be small at the line frequency or in a small neighborhood around the line frequency. From (5), $S(s)$ is shaped in frequency according to the profile specified by $1/W_1$. Hence the weighting

function W_1 should exhibits high gains at only the vicinity of the line frequency while providing smaller gains at all the other frequencies. Here, W_1 is selected as a standard second-order weighting function similar to [87], [88],

$$W_1 = \frac{k_1\omega_0^2}{s^2 + 2\xi\omega_0 s + \omega_0^2} \tag{3.7}$$

where ω_0 is set as the line frequency, $\omega_0=2\pi\cdot60$. The k_1 in the numerator gives a freedom for adjusting the tracking error over the whole frequency range, and the damping ratio ξ provides another degree of freedom for specifically regulating the tracking error performance at the line frequency ω_0, a smaller ξ gives a larger resonant peak but narrower bandwidth around the frequency ω_0. When $\xi\rightarrow0$, the resulting H∞ controller will act like an ideal PR controller, which can theoretically achieve zero steady-state error at the line frequency. In this paper, $k_1=2$, $\xi=0.01$.

3.4.2. Weighting Function Selection for Robust performance

From Fig. 3.7, the nominal plant $G_{aN}(s)$ is expressed as

$$G_{aN}(s) = \frac{1}{L_{gN}C_f s^2 + C_f r_{gN} s + 1} \tag{3.8}$$

where L_{gN}, r_{gN} is the nominal value of the grid equivalent inductance and resistance, respectively. The nominal value L_{gN}=0.15 *mH*, r_{gN}=0.2 Ω as given in Table I. This parameter uncertainty is transformed to multiplicative output uncertainty, and the resulting relative plant uncertainty with respect to the nominal plant, expressed as

$$\Delta(s) = \sigma(\frac{G_a - G_{aN}}{G_{aN}}) \quad . \tag{3.9}$$

$\Delta(s)$ is the plant uncertainty, G_a is the disturbed plant as given in (2), corresponding to the parameter variations $L_g \in [0.05, 0.3]\,mH$, $r_g \in [0.1, 0.5]\,\Omega$, and $\sigma(H)$ stands for the singular values of transfer function *H*. To achieve required robustness, the condition $\|W_3T\|_\infty < 1$ must

be satisfied. The weighting function W_3 is determined by the worst profile of $\Delta(s)$. One can choose the weighting function W_3 that just bounds the worst case uncertainty spectrum from above. The worst case of $\Delta(s)$ can be obtained when L_g is maximum (L_g=0.3 mH) and r_g (r_g=0.1 Ω) is minimum. Thus W_3 is chosen as

$$W_3 = k_3(2.066\cdot10^{-7}s^2 + 0.909\cdot10^{-3}s + 1) \quad . \tag{3.10}$$

where k_3=0.8. Fig. 3.8 shows relative plant uncertainty $\Delta(s)$ with different parameter variations (the solid line indicating the worst case of the plant uncertainty) and the weighting function W_3. In addition, the weighting functions $W_1 \sim W_3$ need to be proper transfer functions (i.e. the degree of the numerator does not exceed the degree of the denominator) as required by Matlab *mixsyn* function. Therefore, two poles far away with the line frequency are added in the denominator of W_3, leading to

$$W_3 = \frac{1.058\cdot10^5 s^2 + 4.655\cdot10^8 s + 5.12\cdot10^{11}}{s^2 + 1.6\cdot10^6 s + 6.4\cdot10^{11}} \tag{3.11}$$

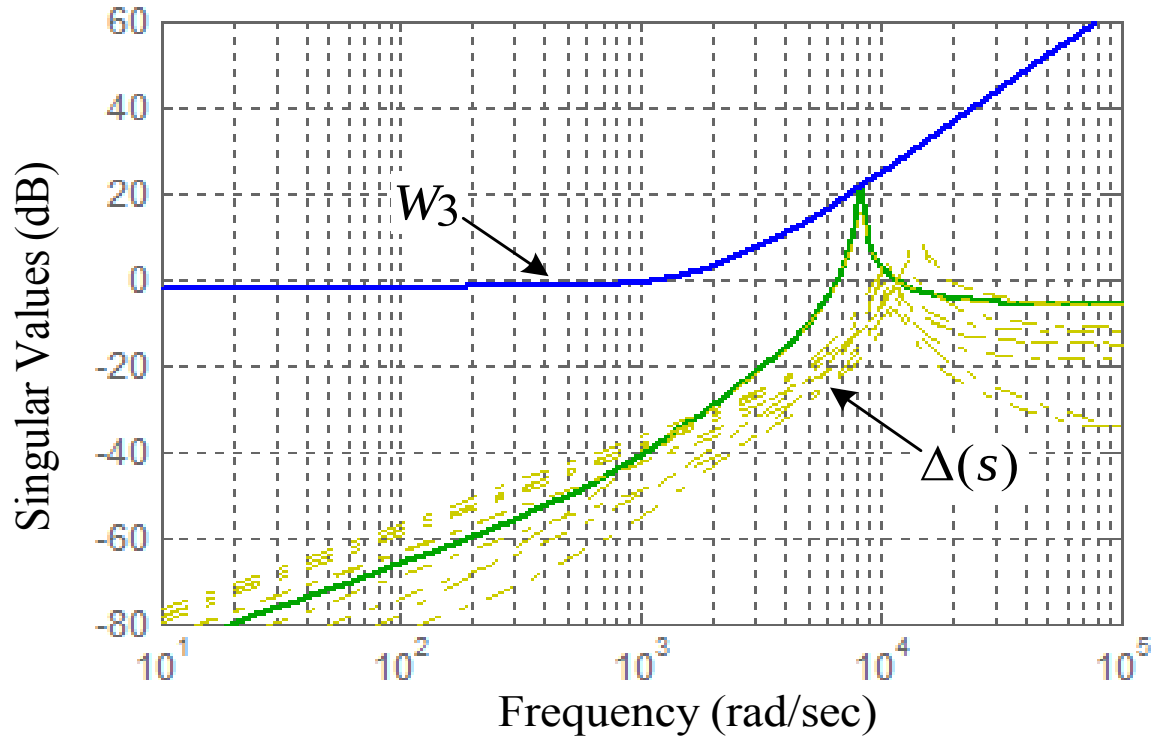


Fig.3.8. Singular values of $\Delta(s)$ and weighting function W_3.

3.4.3. Mixed-Sensitivity H∞ Controller Synthesis

After selecting the necessary weighting functions, mixed-sensitivity optimization control design can be conducted by the Robust Control Toolbox in Matlab software to synthesize an H∞ controller $K(s)$ such that the H∞ norm of the weighted mixed sensitivity is minimized. By using the model reduction function *reduce* in Matlab, the original sixth-order $K(s)$ is then reduced to following third-order for easy implementation with almost the same performance as the original controller

$$K(s) = \frac{608.4s^2 + 2.825 \cdot 10^6 s + 3.65 \cdot 10^8}{s^3 + 2122s^2 + 1.581 \cdot 10^5 s + 3.005 \cdot 10^8} \tag{3.12}$$

Fig. 3.9 shows the singular values of the original sixth-order $K(s)$ and the reduced third-order $K(s)$. The third-order $K(s)$ has almost the same singular values at low frequencies, but less high-frequency attenuation at the vicinity of natural angular frequency ω_n. The singular values of $W_1(s)$, $W_3(s)$, and the resulting $S(s)$, $T(s)$ are shown in Fig. 3.10. As expected, the designed H∞ controller in Fig. 3.8 exhibits significant gain at the line frequency to ensure nearly zero steady-state error. Also, it can be seen that the singular value of H∞ controller falls quickly at high frequencies, making the control system immune to the resonant peak of $G_a(s)$ in (3) as well as high-frequency switching or measurement noises.

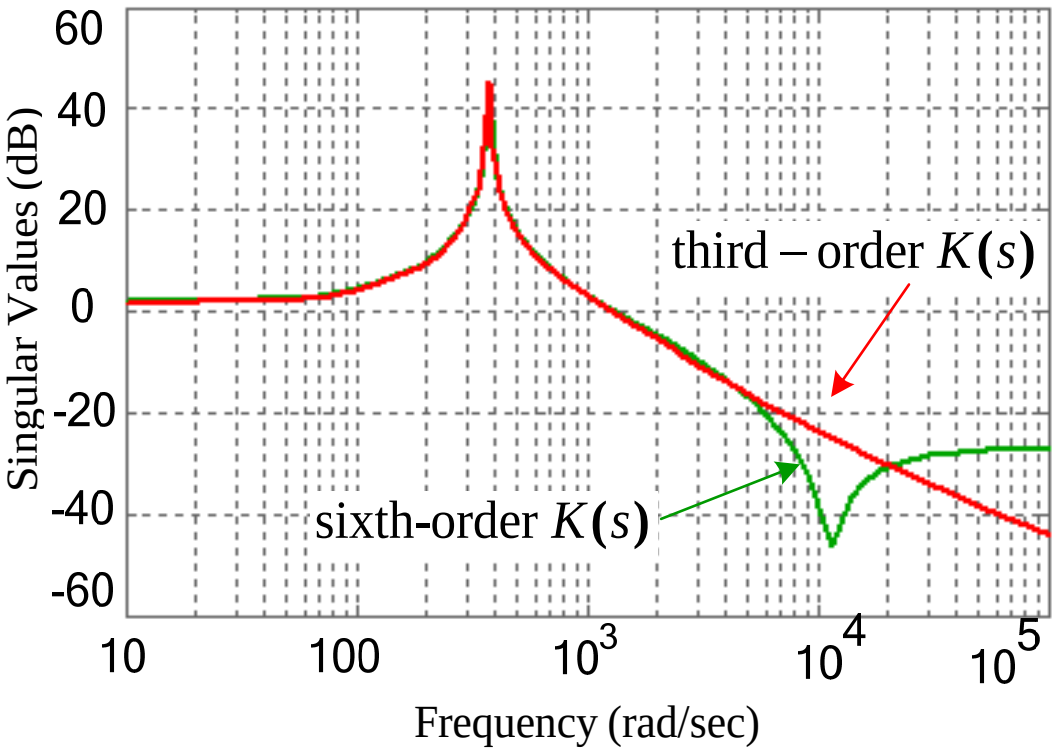


Fig.3.9. Singular values of the original sixth-order $K(s)$ and the reduced third-order $K(s)$.

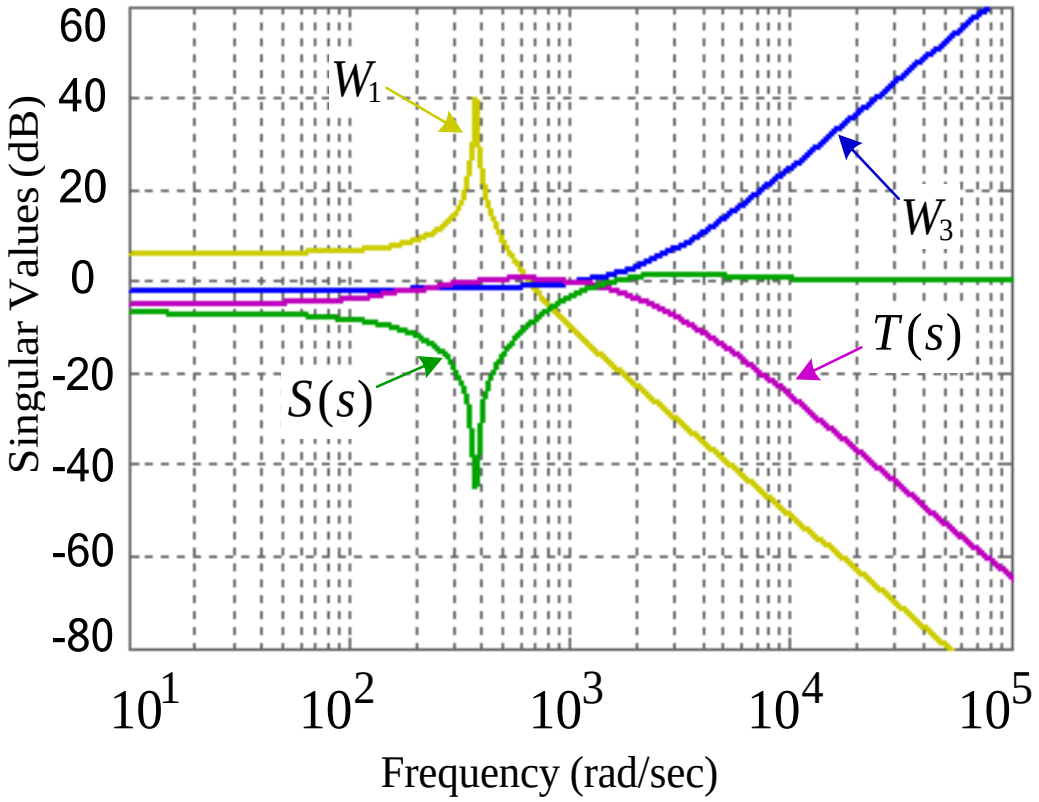


Fig.3.10. Singular values of W_1,W_3, $S(s)$, and $T(s)$.

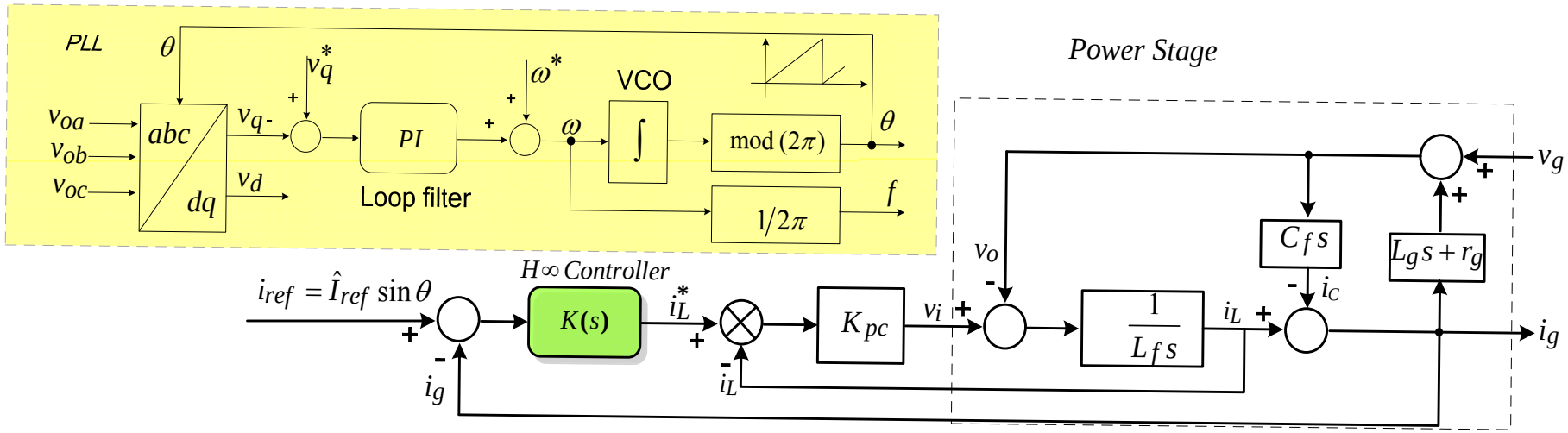


Fig.3.11. The overall control block diagram: H∞ controller combined with an inner inverter-output current control loop, and the three-phase PLL for grid synchronization

The $1/L_f s$ is a physical transfer function, and needs to be restored from $K(s)$. There are two options to restore it:

1) Split the designed $K(s)$ into two parts, the physical transfer function $1/L_f s$ and the controller $K'(s) = K(s) \cdot L_f s$.

2) Remain the designed $K(s)$, but add an inner inverter-output current feedback loop. Ideally, the closed-loop gain of this inner current loop, including the transfer function $1/L_f s$, can be regarded as unity.

From the control block shown in Fig. 3.3, method 2 employs a closed-loop control for inverter-output current, unlike the method 1 that uses an open-loop control. With properly designed high bandwidth, method 2 will have much better disturbance (e.g. dead time effect, model deviation and so on) rejection capability than method 1. Finally, Fig. 3.11 shows the overall control bock diagram: H∞ controller combined with an inner inverter-output current control loop, and the three-phase phase-locked loop (PLL) for grid synchronization [66]. In Fig. 3.11, for each phase, the three-phase grid-current reference

$$\begin{aligned} i_{refa} &= \hat{I}_{ref} \cdot \sin\theta \\ i_{refb} &= \hat{I}_{ref} \cdot \sin\left(\theta - 120^\circ\right) \\ i_{refc} &= \hat{I}_{ref} \cdot \sin\left(\theta + 120^\circ\right) \end{aligned} \tag{3.14}$$

where θ is the output of the PLL as shown in Fig.3.10.

A simple proportional compensator K_{pc} is used in the inner inverter-output current feedback loop to get better control performance. Ideally, the loop gain and bandwidth of the inner loop should be maximized by using a higher value of K_{pc}, to achieve perfect reference tracking at all input frequencies, a faster dynamic response and the complete disturbance rejection. A high gain of K_{pc} gives the desired performance, and meanwhile stability problem would arise during physical implementation due to the control delay, measurement

noises, and so on. In this paper, $K_{pc} = 5$ is chosen.

3.5. Simulation and Experimental Results

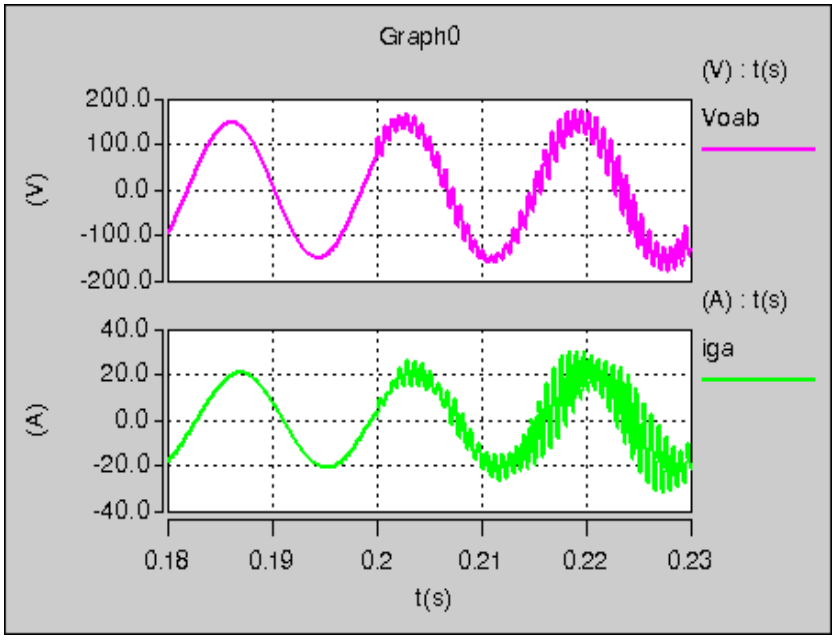


Fig.3.12. Simulation results of PI controller with grid impedance $[r_g, L_g]$ changing from [0.1 Ω, 0.05 *mH*] to [0.2 Ω, 0.2 *mH*] at the instant t=0.2*s*.

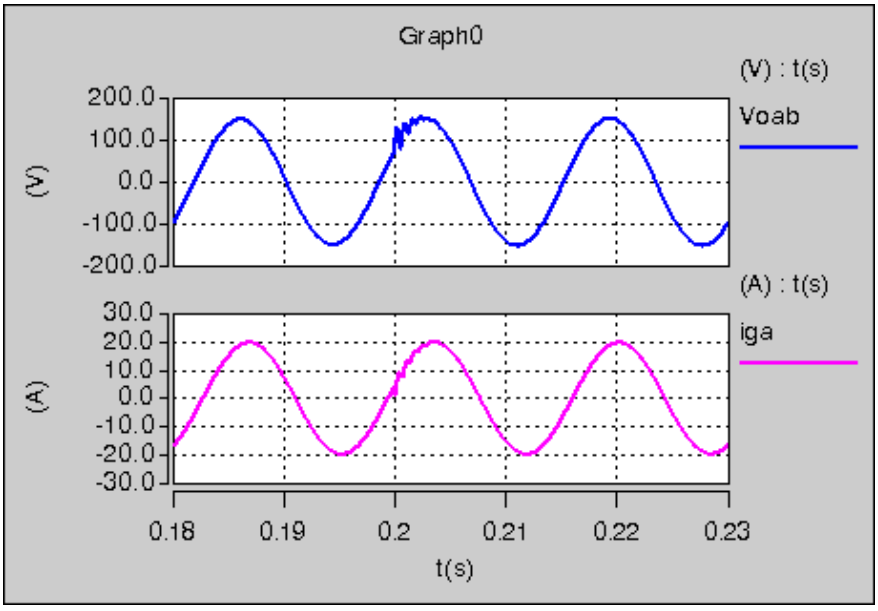


Fig. 3.13.Simulation results of H∞ controller with grid impedance $[r_g, L_g]$ changing from [0.1 Ω, 0.05 *mH*] to [0.2 Ω, 0.3 *mH*] at the instant t=0.2*s*.

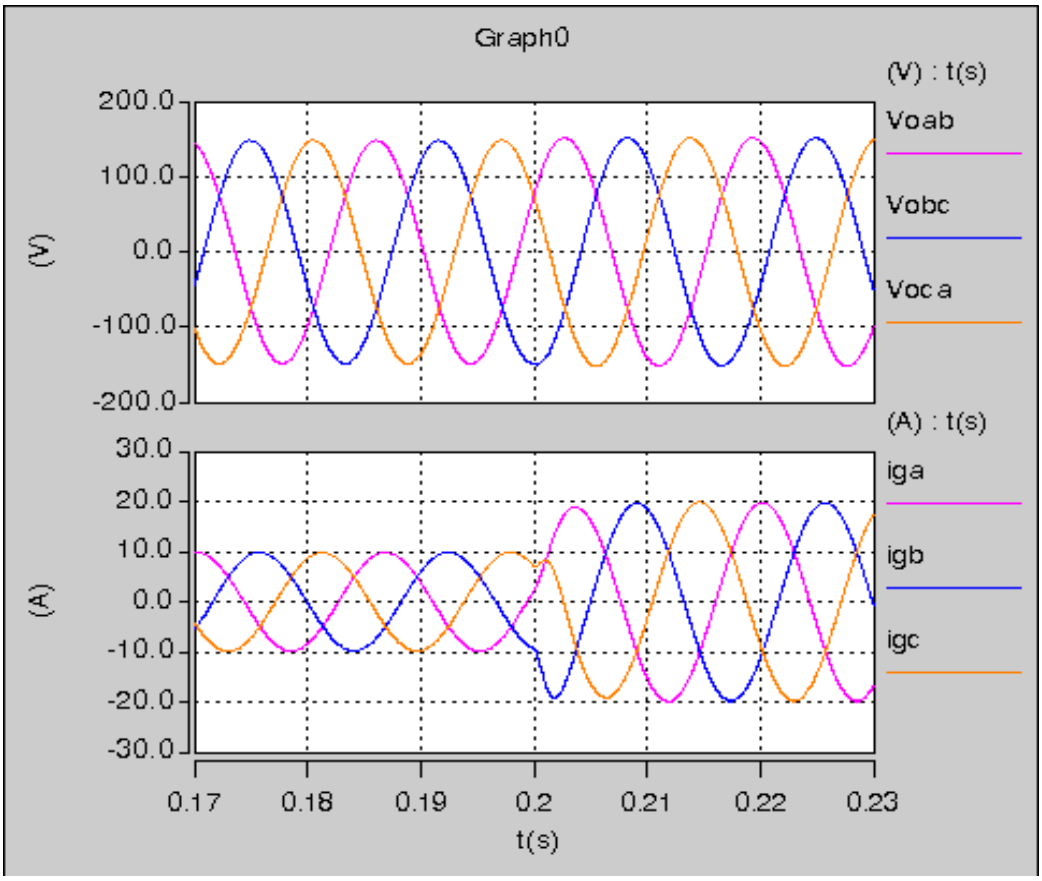


Fig.3.14. Simulation results of H∞ controller with $\hat{I}_{ref}$ changing from 10 A to 20A at the instant t=0.2s.

.The performance of the proposed H∞ controller was first verified via computer simulation, and then realized and tested in the laboratory. The simulation and experimental results based on conventional PI controller were also given as a comparison. In our simulation and experiment, a transformer with turn ratio 1: 2 is used to couple the 3-phase inverter to the grid. Therefore, the inverter output voltage v_o is about half of the grid voltage v_g. To be consistent, all the parameters in both simulation and experiment are the same as given in Table I.

3.5.1. Simulation Results

The simulations have been carried out under continuous domain with a switching frequency of 10 kHz and one switching period control delay. To investigate the tracking performance as well as the system stability, simulations have been developed under different (weak or stiff)

grid conditions.

Fig. 3.12 shows the simulation results of the PI controller with grid impedance $[r_g, L_g]$ changing from [0.1 Ω, 0.05 *mH*] to [0.2 Ω, 0.2 *mH*] at the instant *t*=0.2*s*, where $K_p = 4$, $K_i = 4000$. From Fig., it can be seen that with L_g increasing, the system exhibits oscillations and tends to instability, which is a good agreement with the analysis in section II. Through decreasing the loop gain (e.g. $K_p = 3, K_i = 3000$) can sustain the system stable, however, it will significantly decrease the tracking performance and the disturbance rejection capability, thus resulting higher THD of the grid current. Fig. 3.13 shows the simulation results of proposed H∞ controller with grid impedance $[r_g, L_g]$ changing from from [0.1 Ω, 0.05 *mH*] to [0.2 Ω, 0.3 *mH*] at the instant *t*=0.2*s*, which reveals that the system can keep stable with the grid impedance variations in a wide range. In addition, the simulation results of H∞ controller with amplitude of grid-current reference (denoted as $\hat{I}_{ref}$) step change from 10 A to 20A at the instant $t = 0.2\,s$ are also given in Fig. 3.14. This figure states that with the grid current reference step change, the output grid current can faithfully follow the reference after a short regulation time.

3.5.2. Experimental Results

In the simulation, the continuous-time controller is used, while in the experiment, the third-order H∞ controller in (3.12) need to be discretized as shown in the following expression with the coefficients calculated by the bilinear transformation method,

$$K(z) = \frac{b_0 + b_1 \cdot z^{-1} + b_2 \cdot z^{-2} + b_3 \cdot z^{-3}}{1 + a_1 \cdot z^{-1} + a_2 \cdot z^{-2} + a_3 \cdot z^{-3}} \tag{3.15}$$

The coefficients a_1~a_3 and b_1~b_3 in (3.14) should keep enough decimal digits to avoid loss of accuracy. The discrete H∞ controller in (3.15) was implemented with a 16-bit fixed-point

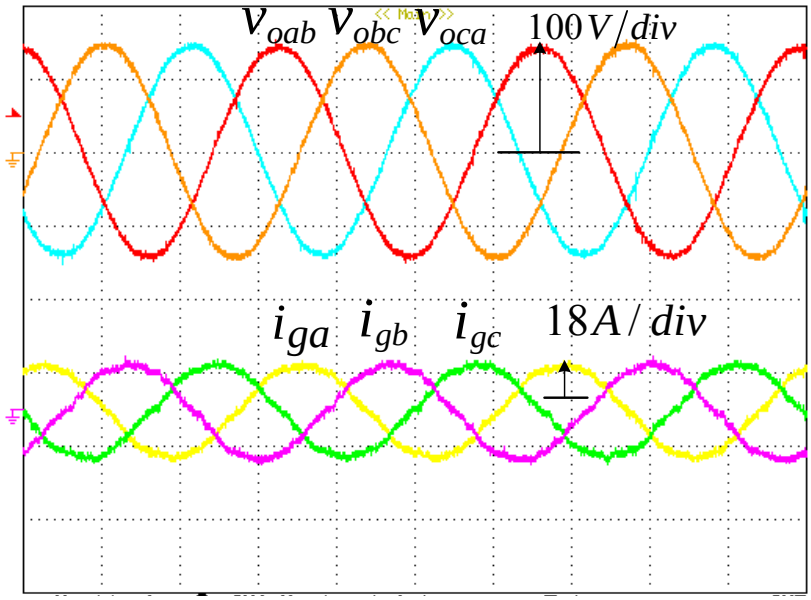
digital signal processor (DSP), TMS320LF2407 in our experiments, which can operate at 40 million instructions per second (MIPS). Nevertheless, 32-bit fixed-point or floating-point DSP is strongly recommended for better calculation speed and avoiding the numerical error during the calculation. To verify the advantages of the proposed control scheme, the experiments based on the conventional PI controller and the H∞ controller are developed with two different grid impedances. The tuned parameters of the PI controller in the experiment are $K_p = 3, K_i = 3000$. For PI control, this combination of parameters gives the best performance in terms of both THD of the grid current and system stability.

In the first case, the measured grid impedance $[r_g, L_g]$ =[0.1 Ω, 0.15 *mH*]. Fig. (a), (b) show the experimental results of the conventional PI controller with different amplitude of grid-current reference, $\hat{I}_{ref} = 10A, 20A$ respectively, while Fig. 3.16 (a), (b) show the corresponding experimental results of the proposed H∞ controller. The start-up processes for H∞ controller is also given in Fig. 3.16(c), respectively. From Fig.3.15-Fig.3.16, we see that in both control methods, the grid voltage and the corresponding grid current are in phase and near-unity power factor is achieved. However, the grid-current waveforms of the H∞ controller are much better than that of PI controller.

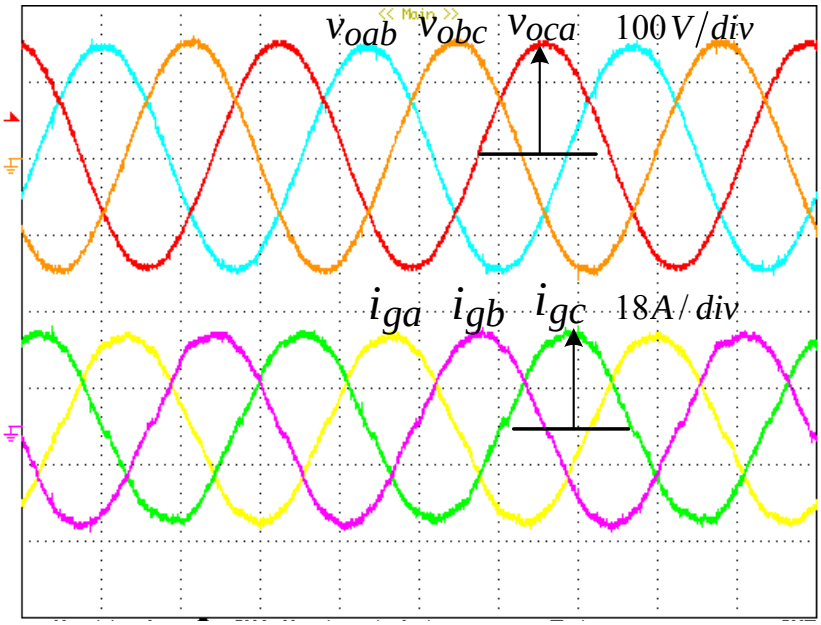
In the second case, with an intentionally added inductor, the grid $[r_g, L_g]$ = [0.1 Ω, 0.3 *mH*]. Due to the page limit, the experimental waveforms are not shown, but the measured THD of the grid current for all cases are listed in Table II. It can be seen that the grid current THD of H∞ controller are always lower than that of PI controller and almost keep unchanged with the grid-impedance variations, which satisfy the THD requirement of IEEE Std. 1547-2003 (i.e. 5%).

From the measured waveforms and THD of grid current, it is evident that proposed H∞ controller has satisfactory performance while applying to grid-connected inverters to deal

with the possible grid impedance variations. In the simulation and experiments, the grid impedance variations are within the predefined range as given in Table. I. In the condition that the grid impedance variations are beyond this range, we can use the same design method but re-select the weighting functions and synthesize a new H∞ controller to get the satisfactory control performance as well.

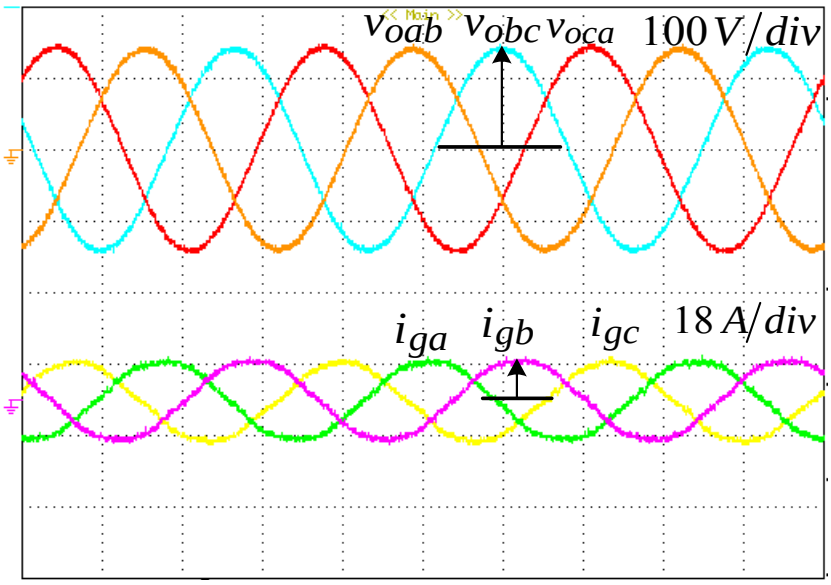


(a) $\hat{I}_{ref} = 10A$

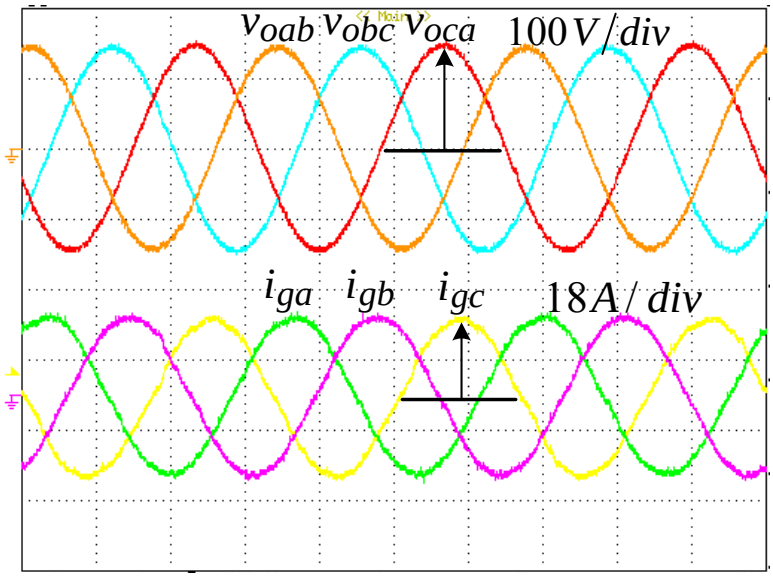


(b) $\hat{I}_{ref} = 20A$

Fig.3.15. Experimental results of the conventional PI controller with different $\hat{I}_{ref}$



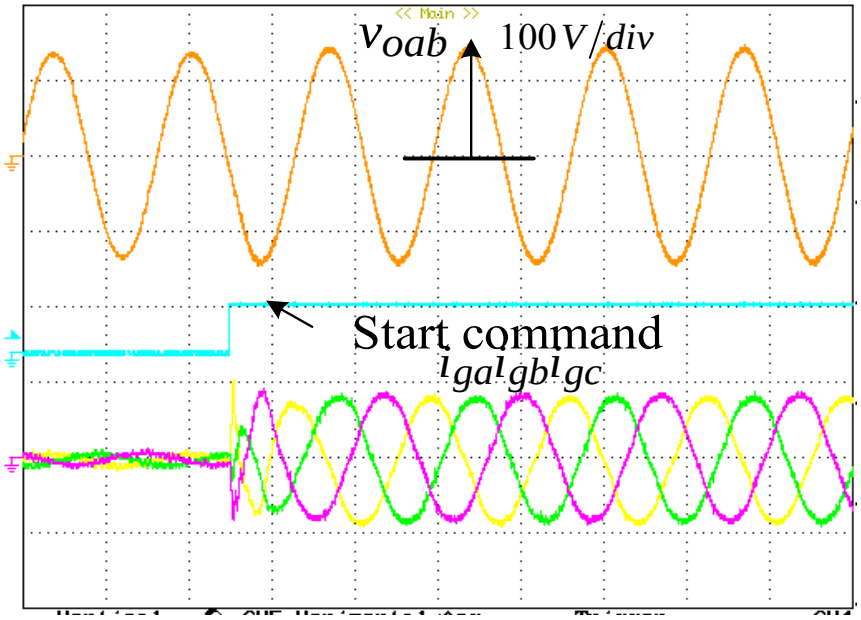
(a) $\hat{I}_{ref} = 10A$



(b) $\hat{I}_{ref} = 20A$

Fig.3.16. Experimental results of the proposed H∞ controller in steady-state and the start-up process.

Fig.3.16 (cont'd)



(c) Start-up process with $\hat{I}_{ref} = 15A$

Fig.3.16. Experimental results of the proposed H∞ controller in steady-state and the start-up process.

Table 3-2.THD of Grid Current (%)

Grid Impedance	Ctrl. Method	$\hat{I}_{ref} = 10A$	$\hat{I}_{ref} = 15A$	$\hat{I}_{ref} = 20A$
$[r_g, L_g] =$ [0.2 Ω, 0.15 mH]	PI Controller	4.327%	3.681%	3.184%
	H∞ Controller	3.398%	2.441%	2.385%
$[r_g, L_g] =$ [0.2 Ω, 0.3 mH]	PI Controller	5.277%	4.859%	4.553%
	H∞ Controller	3.709%	2.401%	2.206%

3.6. Summary

In the grid-connected voltage source inverter with LC filters, the possible wide range of

grid-impedance variations can challenge the design of the controller, especially when the grid-impedance is highly inductive. This paper proposes an H∞ controller with the explicit robustness in terms of grid impedance variations to incorporate the desired tracking performance and stability margin. By properly selecting the weighting functions, the synthesized H∞ controller exhibits high gains at the vicinity of the line frequency, similar to the traditional PR controller, meanwhile it has enough high frequency attenuation to keep the control loop stable. An inner inverter-output-current loop with high bandwidth is also designed to get better disturbance rejection capability. The selection of weighting functions, inner inverter-output-current loop design, and system disturbance rejection capability are discussed in detail in this paper. Both simulation and experimental results of the proposed H∞ controller, with comparison to the conventional PI controller, are given to validate the performance of the proposed control scheme. It should be noted again that the proposed H∞ controller can be easily applied to single-phase grid-connected inverter as well since it is developed in the stationary reference frame.

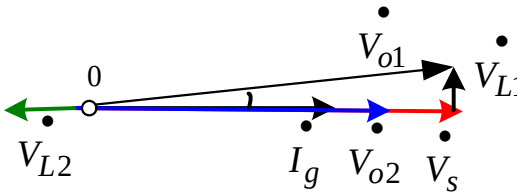
CHAPTER 4 SEAMLESS TRANSITION CONTROL SCHEME

4.1. Introduction

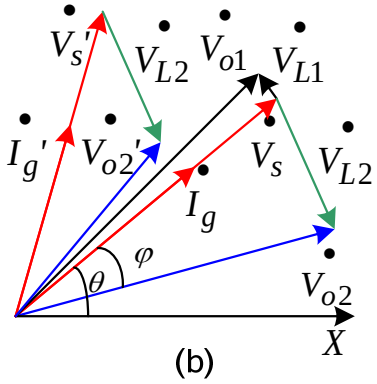
The grid-connected inverter works as a controlled current source in grid-connected mode, while operates as a controlled voltage source in standalone mode. So in case of utility faults or intentional islanding, the inverter has to change its control strategy from current control to voltage control. In the transition from grid-connected to standalone operation, Solid State Relay (SSR) is used here as the switch between DG and grid. However, the turn-off characteristics of the SSR makes the transition last for a long time up to half a cycle. So in order to force the grid currents through the SSR switches to decrease to zero at much less time and make the voltage fluctuates within permissible levels during SSRs turn-off period, the voltage control based voltage amplitude regulation, instantaneous voltage regulation algorithms and current control based zero current regulation algorithms have been adopted in transition. In standalone mode and grid-connected mode, the previously proposed controllers are adopted. After disconnection from the grid, the inverter will recover its voltage to a rated level. Simulation and experiments are carried out to verify the proposed controllers and algorithms.

4.2. Principle and Analysis of Transfer Strategies [108]

4.2.1. Voltage control based transfer strategies [90-92]



(a)



(b)

Fig.4.1.Phasor diagram at (a)Voltage amplitude regulation (b) Instantaneous voltage regulation

Table 4-1.Equations for voltage, current and transition time

Varibles	Voltage amplitude regulation	Instant voltage regulation
i_g	$I_g \sin(\omega t)$	$I_g \sin(\omega t+\theta)$
v_s	$V_{sm} \sin(\omega t)$	$V_{sm} \sin(\omega t+\theta)$
v_{o2}	$V_{02m} \sin(\omega t)$	$v_s + v_b$
v_L	$v_L = v_{o2} - v_s = L_g di_g / dt$	$v_L = V_b = kv_L(t_0)$
Δt	$\Delta t = \frac{-i_g}{di_g / dt} = \frac{L_g I_{gm}}{V_{sm} - V_{o2m}}$	$\Delta t = \frac{L_g i_g(t_0)}{V_b} = \frac{1}{k\omega} = Constant$

The voltage amplitude regulation, and instantaneous voltage regulation [95] are both based on applying voltage control strategy in transition time. Fig.4.1 shows the voltage and current phasor diagram for above two strategies. Voltage amplitude regulation method represses the current by increasing or decreasing voltage amplitude while keep phase the same in the transition. Once the grid current is force to decrease to zero, the SSR are turned off and the reference output voltage is recovered to the rated value. It takes less time to complete the transfer process hence minimize the voltage distortion. Instantaneous voltage regulation is to generate a constant voltage difference holding a fixed ratio to the initial grid current at transition start, which can settle the transition time to a fixed value. The detailed equations between transition time Δt and other parameters are shown in Table.1. The variables used are defined as: v_s -- grid phase voltage; v_{o1} -- initial inverter output phase voltage; v_{o2} --regulated inverter output phase voltage; i_g --grid side phase current; t_0 --the moment that the drive signal of SSR is given; v_L --grid side inductor regulated voltage; V_b --pre-set voltage drop on the inductor.

4.2.2. Current control based transfer strategies [93-95]

The principle of zero current regulation is to retain the current control mode in transition but change the current reference to zero. After the current drops to zero, SSR will turn off and the system shifts to voltage control. Due to the delay of zero current sensing, there is a blank time between disconnection and control mode shift in which voltage is out of control. However, the zero current regulation dynamic response depends on the step response time of current control loop, which is shorter than the time for voltage control loop, thus it gets better dynamic performance. However, this method doesn't rely on the grid side voltage and also don't need to sense the voltage accurately. So it is preferred in grid voltage short circuit or highly disturbed case.

4.3. Simulation and Experimental Result

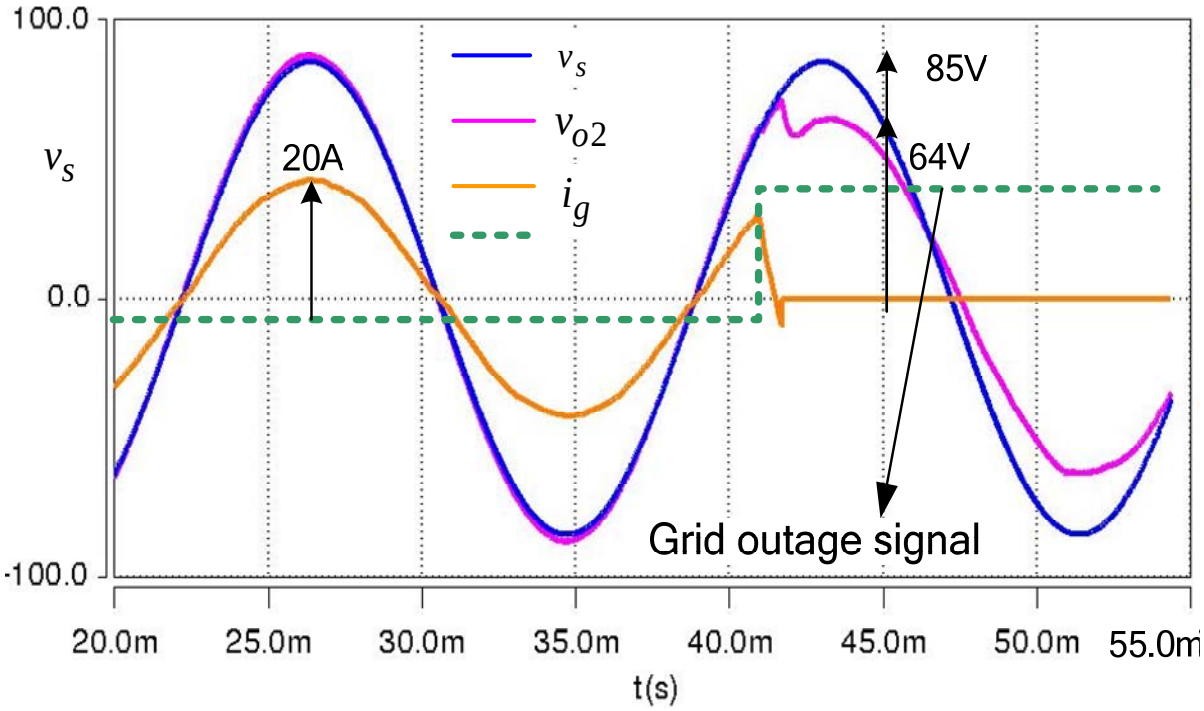
The system parameter in the simulation and experiment is:

$\omega = 377 rad/s,\ f_{sw} = 10kHZ, V_{sm} = 85V, V_{dc} = 200V, L_f = 1mH,$
$C_f = 50uF, L_g = 0.1mH, r_g = 0.1\Omega, I_{ref} = 20A$

Assume grid absorbs current from inverter.

4.3.1. Simulation results

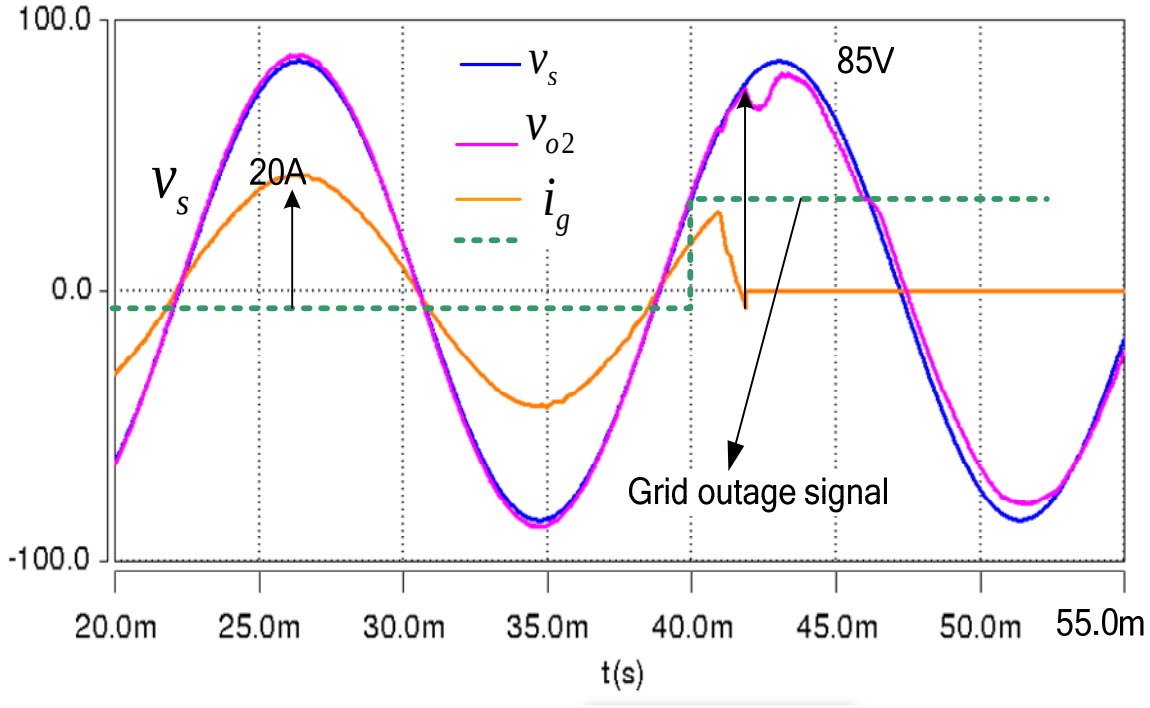
Fig.4.2 (a) (b) (c) shows the simulation results for the three strategies respectively. The current reference in grid-connected mode is set to be 20A. In Fig.4.2 (a), the inverter output voltage reference is set to be 0.8 times of the grid voltage in the transition. According to the equations in table I, the transition time is calculated to be 0.2ms. The total transition time is 0.8ms by adding the calculated value and voltage loop step response rising time 0.6ms, which is coincident with the simulation results.



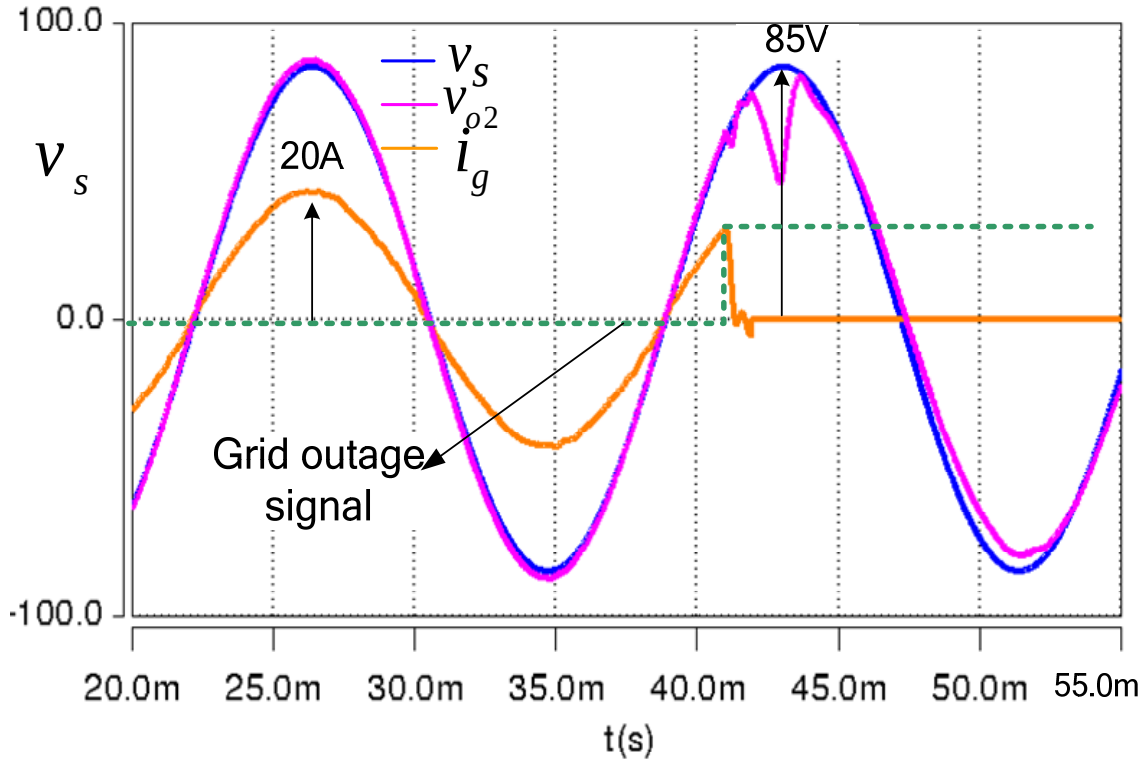
(a)

Fig.4.2. Simulation results for grid voltage V_s, inverter output voltage V_{o2}, grid side current i_g in transition using different strategy (a) voltage amplitude regulation (b) voltage instantaneous value regulation (c) zero current regulation

Fig.4.2 (cont'd)



(b)



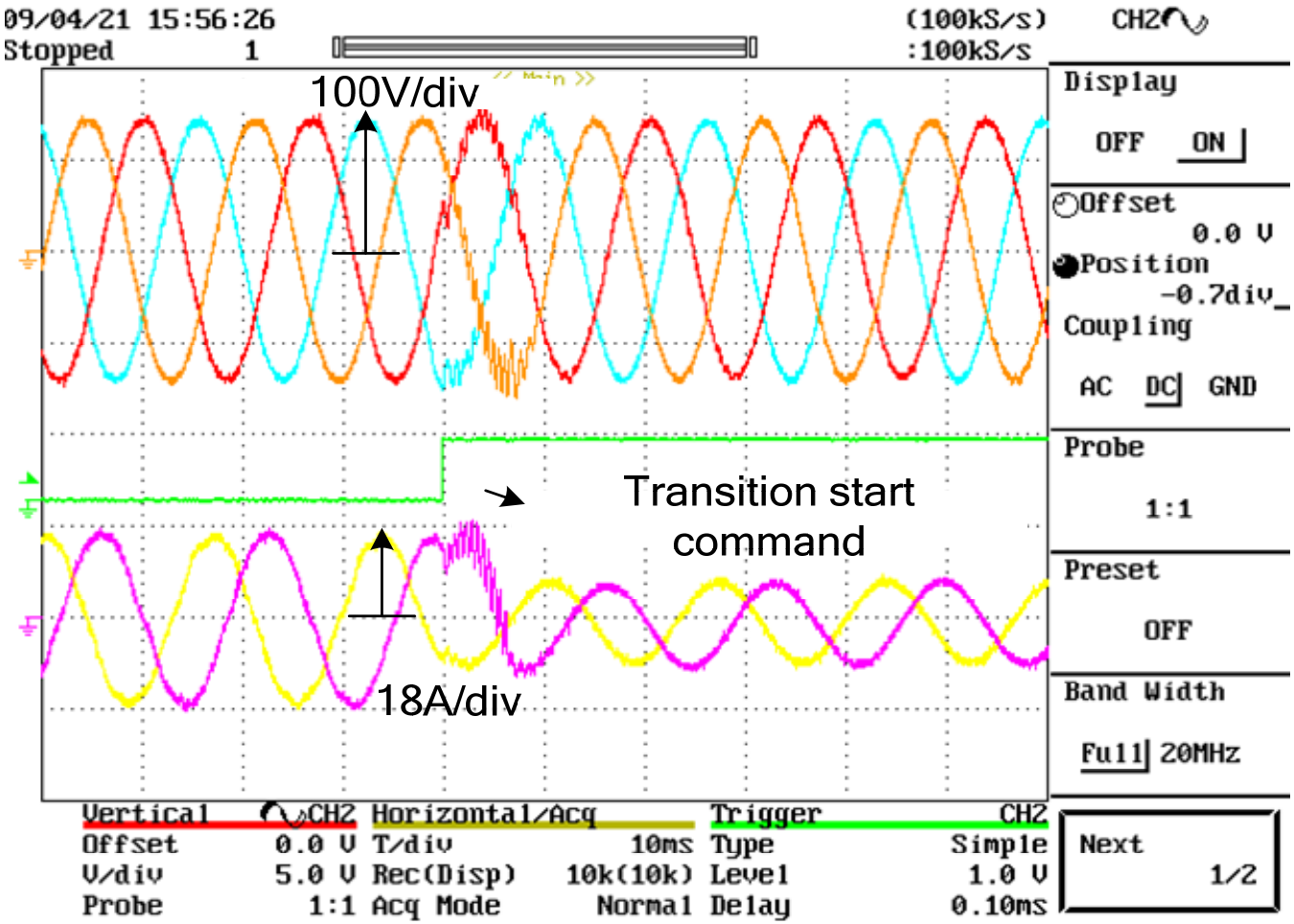
(c)

In Fig.4.2 (b), the constant voltage difference is 20V, so the transition time is fixed at 1ms as

calculated, which is the same as simulation result. In Fig.4.2 (c), as mentioned before current regulation method has relatively small transition time but bigger voltage distortion.

4.3.2. Experimental results

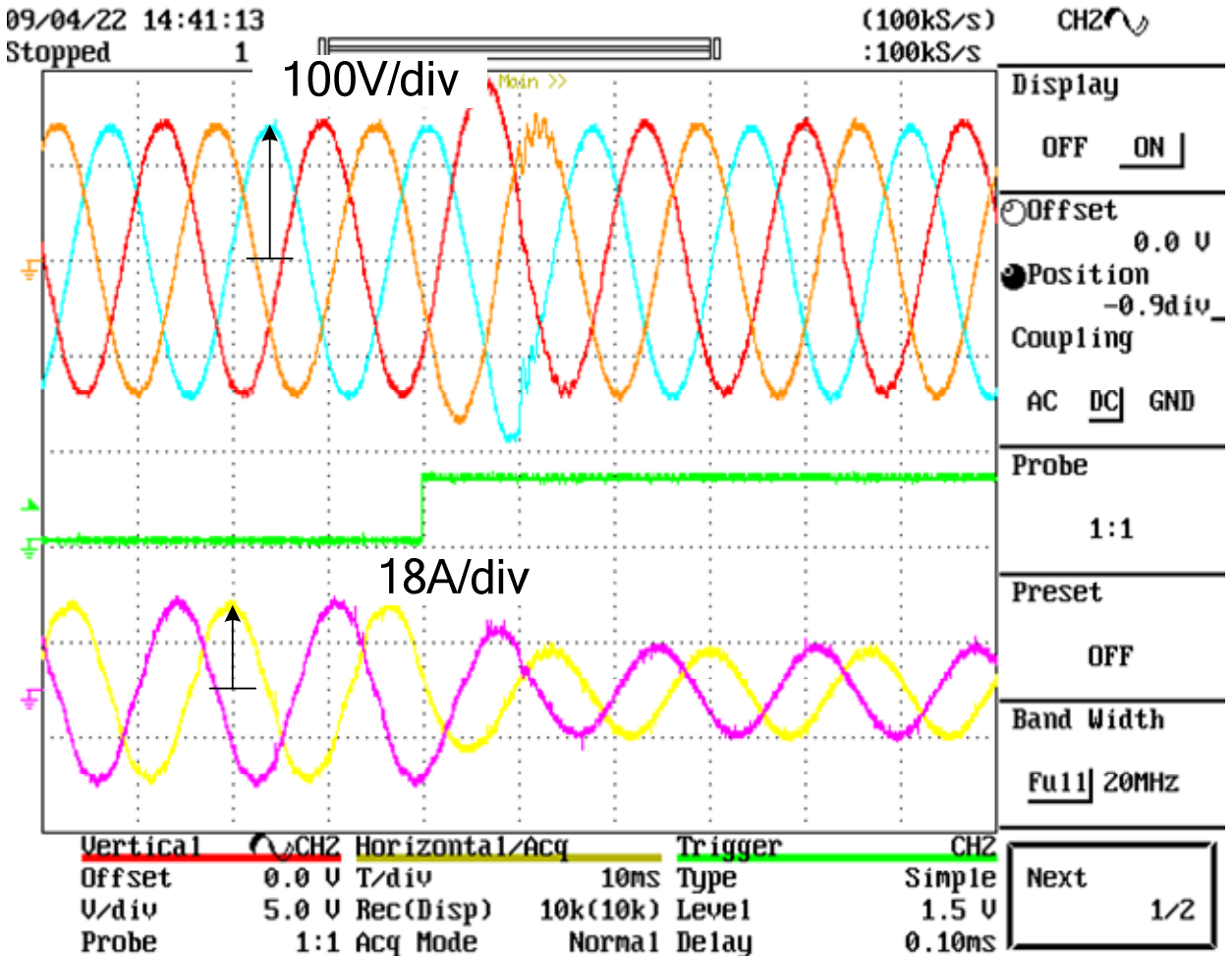
Fig.4.3 shows the experimental results for voltage instantaneous value regulation and zero current regulation. The three upper sinusoidal waveforms are the inverter output voltage and the three lower ones are the current before the load (load are connected in parallel with capacitor on the grid side). So the current after the transition is equal to the load current which is not zero as simulated one. The green one is the grid outage signal, which also indicates the time that the SSR off signal is sent out. From the experimental waveforms, it can be seen that the voltage distortion and transition time are both in a reasonable range. Voltage control based regulation will last for longer time than current control based strategy, while the current



(a)

Fig.4.3. Experiment results for inverter output line to line voltage and phase current in transition using two strategies (a) Instantaneous voltage regulation (b)zero Current regulation

Fig.4.3 (cont'd)



(b)

control one may cause a relatively big voltage amplitude and phase change. Voltage based algorithms are used when the grid maintain its voltage after transition and current based algorithm is used when grid voltage is highly distorted.

4.4. Summary

In this section, the voltage based and current control based algorithm are adopted in transition to force the current to decrease to zero at a short time. The simulation and experimental results show that the proposed control algorithms can provide seamless transfers between the two operating modes for the inverter, avoiding the temporarily uncontrolled output voltage. It can be valuable for grid-connected inverters such as PV and fuel cell generation system.

CHAPTER 5 INTELLIGENT ISLANDING DETECTION AND LOAD SHEDDING SCHEME

5.1. Introduction

Islanding is a condition that a portion of the microgrid which contains DG and load is isolated from the reminder of the utility system but continue to provide adequate power to local sensitive loads and maintain service within the microgrid [96]. Chapter 3 presents the current control strategy for the inverter grid-connected operation. Chapter 2 presents the voltage control strategy for the inverter standalone operation when the DG is in islanding condition, which is also called standalone operation. Chapter 4 presents the control strategy in the transition between these two operation modes. When the microgrid is cut off from the main grid, intentional islanding operation, each DG inverter system must detect this islanding situation and then switches from grid-connected mode to standalone mode. This section will concentrate on the analysis on characteristics of inverter voltage in the islanding moment. Also an islanding detection method has been provided based on the characteristics. Particularly, the following topics will be addressed: grid-connected system power control mode and current control mode, transient analysis during power outage, islanding detection and load shedding, standalone system control mode, synchronization in re-connection. Some simulation and experimental results are also shown in this paper to illustrate the above mentioned issues [109].

5.2. Constant power load

Typically, there are three types of loads: the constant impedance load, the constant power loads, and the constant current loads. Constant impedance load is just normal impedance and constant current loads can be modeled as constant current source. In order to study the effects of constant power loads in ac systems, a modeling approach considering small signal variations around the operating point is used [98]. AC constant power loads can be considered

as dc constant power loads with diode rectifier at the front stage. The voltage of the constant power load is assumed to be sinusoidal. However, the current is not sinusoidal. By neglecting the harmonics, we only consider the fundamental component of the current. Also a small-signal perturbation in the amplitude of the voltage and current is considered. So the average constant power can be expressed as:

$$P = \frac{1}{2} V_{\max} I_{\max} = V_{rms} I_{rms} = \frac{1}{2} (V_{\max} + \tilde{V}_{\max})(I_{\max} + \tilde{I}_{\max}) \tag{5.1}$$

Neglecting the second order term, we can conclude

$$\frac{\tilde{V}_{\max}}{\tilde{I}_{\max}} = -\frac{V_{\max}}{I_{\max}} = -R_{CPL} \tag{5.2}$$

So R_{CPL} is defined as

$$R_{CPL} = \frac{V_{\max}}{I_{\max}} = \frac{{V_{rms}}^2}{P_L} \tag{5.3}$$

Therefore, the ac constant power load behaves as a negative resistance of which the absolute value is equal to the impedance of the constant power load at its operating point. In another viewpoint, the CPL also can be considered as a voltage controlled current source, as shown in Fig.5.1. The gain between

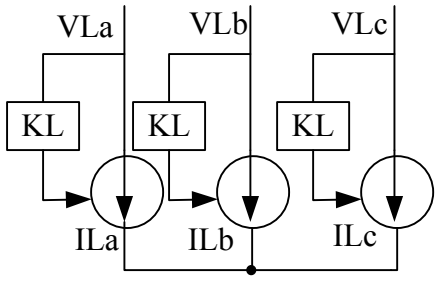


Fig.5.1. Constant power load equivalent model

load voltage and load current K_L is calculated by equation (4), and the three phase currents are calculated using equation (5).

$$K_L = \frac{P_L}{V_{l-lrms}{}^2} = \frac{P_L}{V_{La}{}^2 + V_{Lb}{}^2 + V_{Lc}{}^2} \tag{5.4}$$

$$i_{Li} = K_L V_{Li} \ (i = a, b, c) \tag{5.5}$$

5.3. Grid-connected system control method under constant power load

5.3.1. Constant power control method

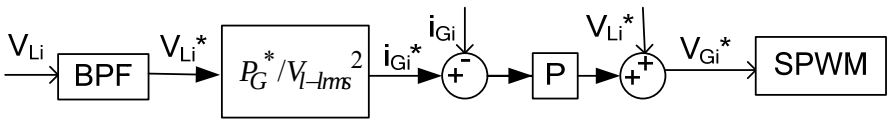


Fig.5.2.Constant power controller in grid-connected system

During normal grid operation, the DG supplies a pre-set (or available maximum from the source) power to the grid Fig.5.2 shows the control block diagram of the VSI-based DG. The objective of the controller is to control the VSI to inject real power to the grid according to a pre-set reference value $P_G{}^*$. The power reference and the voltages at the CPL (V_{La}, V_{Lb}, and V_{Lc}) are used to set references for the current controllers. The inductor current I_G in the LC filter is controlled to follow the reference current [98]. This reference current is given by equation (6), where $V_{l\text{-}lrms}$ is the RMS value of line to line voltage and $P_G{}^*$ is power reference. To implement synchronization and maintain the stability of the DG system, a band-pass-filter at the line frequency is used to generate the current reference without using a PLL circuit, which is beneficial. The transfer function to realize these parameters is shown in equation (7).

$$I_{Ga}{}^* = \frac{P_G{}^*}{V_{l-lrms}{}^2} V_{La}{}^* \tag{5.6}$$

$$BPF(s) = \frac{\frac{\omega_1}{Q} s}{s^2 + \frac{\omega_1}{Q} s + \omega_1{}^2} \tag{5.7}$$

5.3.2. Constant current control method

The details of constant current control mode have been shown in chapter 3.

5.4. Load voltage transient characteristics in the transition from grid-connected mode to standalone mode

5.4.1. Load voltage transient analysis in constant power control mode with constant power load during power outage

During normal grid operation, the DG provides a constant power to the grid. The power depends on many factors such as the availability of energy, energy cost, and so on. The main grid is supplying or absorbing the power difference between the DGs and the local load. When the main power grid is out, the DG delivering pre-set or available maximum power to the microgrid can create voltage and frequency transients which are dependent on the degree of the power difference.

The power difference causes the voltage to drift from nominal values. When the voltage drifts to a pre-defined level, it is deemed that islanding is occurring. This methodology is suitable for both islanding detection and anti-islanding operation (during an anti-islanding operation, the DGs cease providing power to loads).

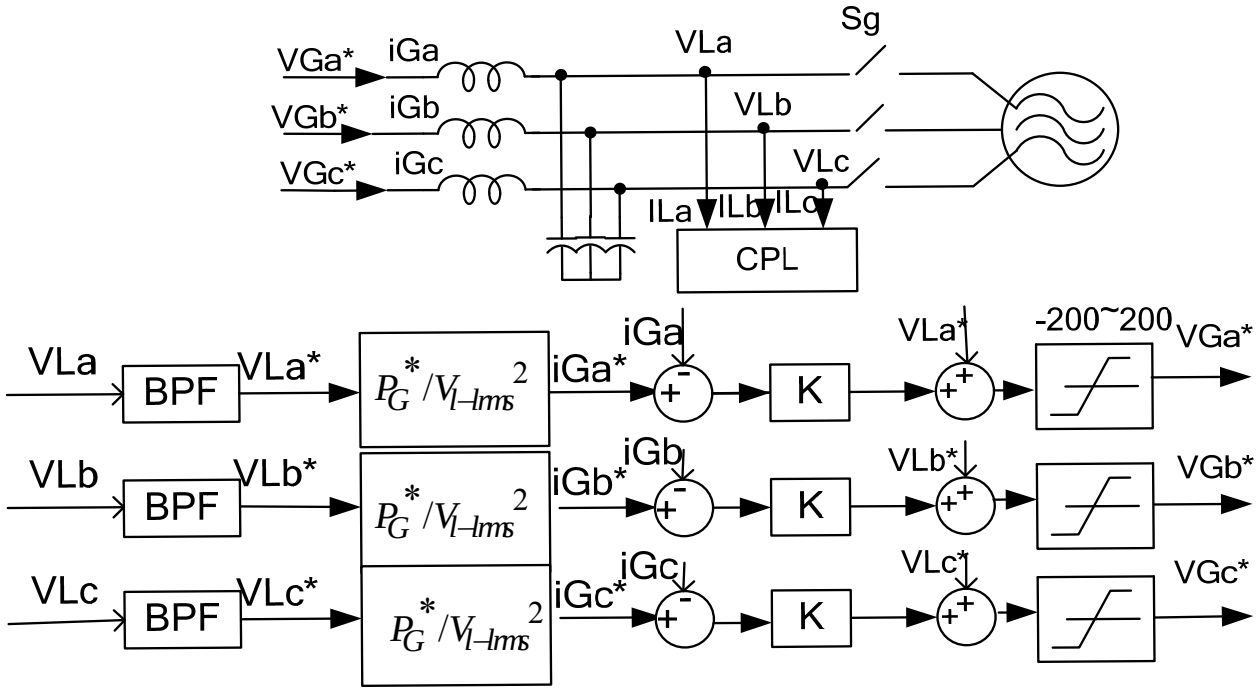


Fig.5.3. Model of the Constant-Power Controlled DG

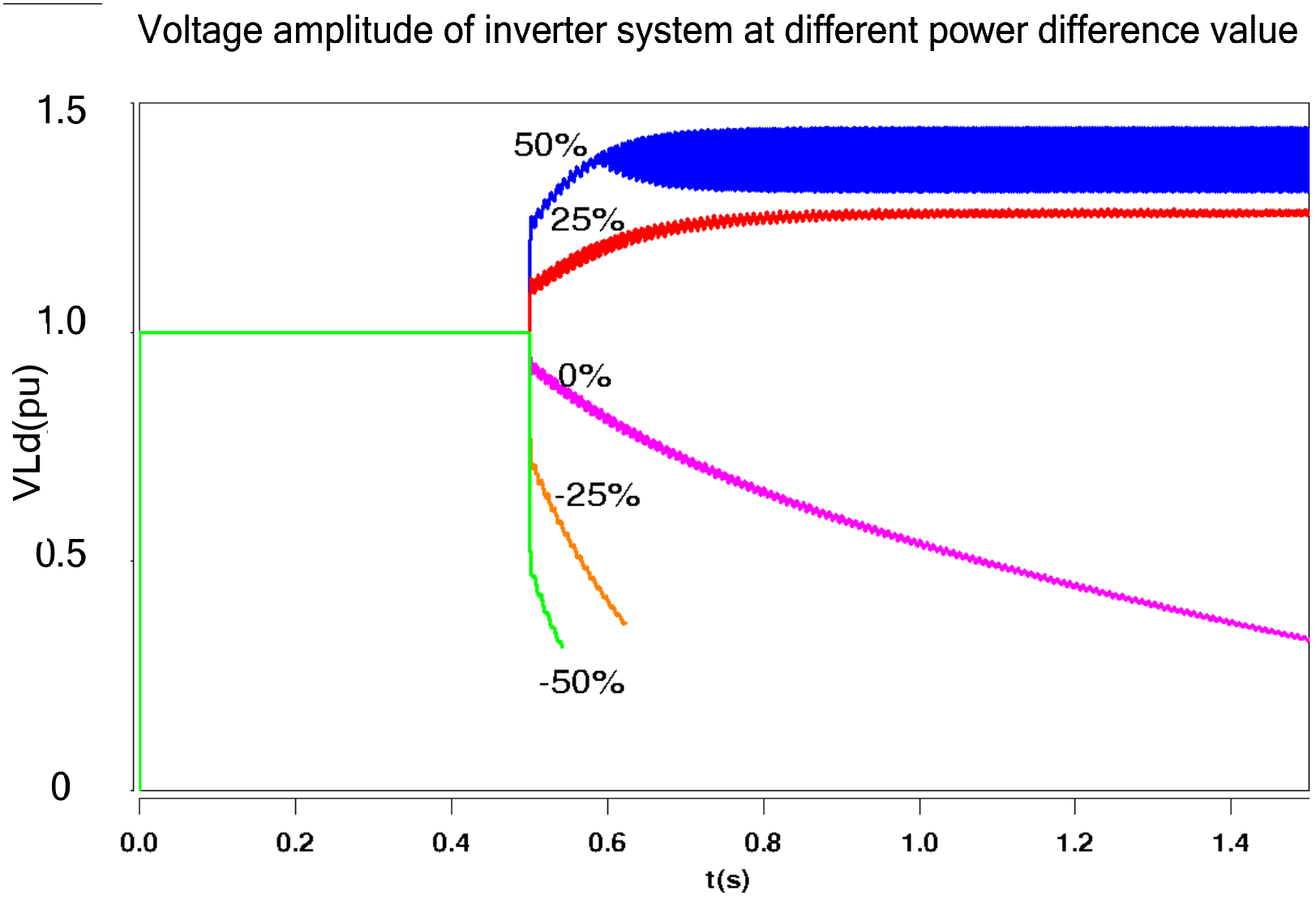


Fig.5.4. Voltage amplitude drift of inverter

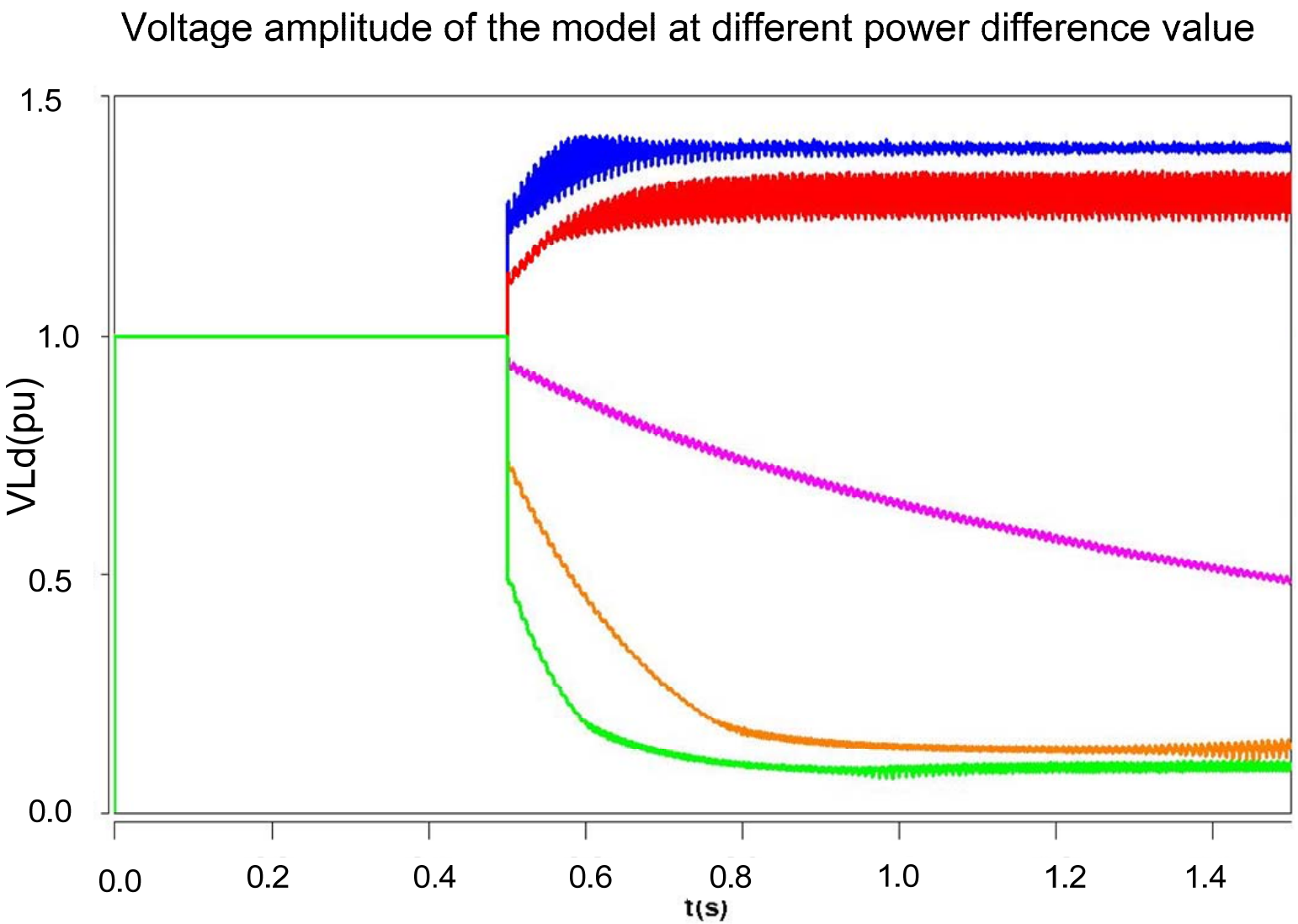


Fig.5.5. Voltage amplitude drift of the model

5.4.2. Load voltage transient analysis in constant current control mode with constant impedance load during power outage

In constant current control mode, the inverter and the filter together can be considered as a constant current source and the grid can be modeled as a constant voltage source supplying the power to impedance load. So the voltage drift in the transient from grid-connected to standalone is shown in Fig.5.6 in the degree of power differences. Assume the load impedance is a parallel resistor and capacitor of which $R_{pu} = 1, Z_{Cpu} = 2$.

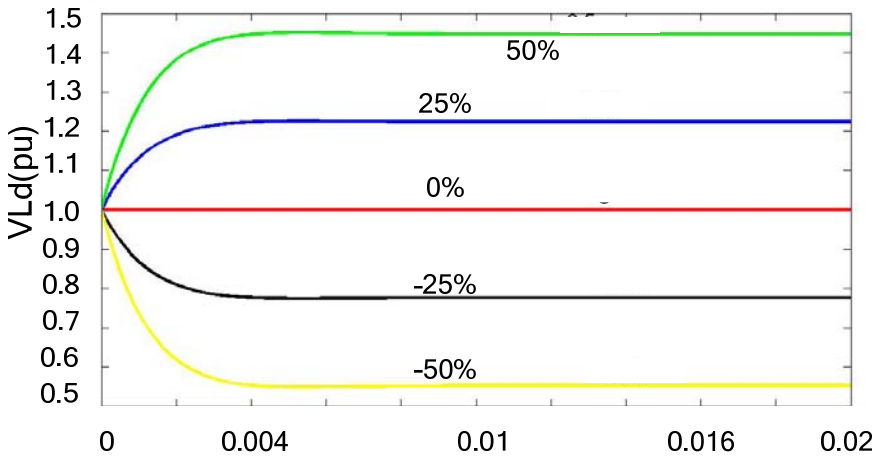


Fig.5.6. Voltage amplitude drift in constant current control mode with constant impedance load during power outage

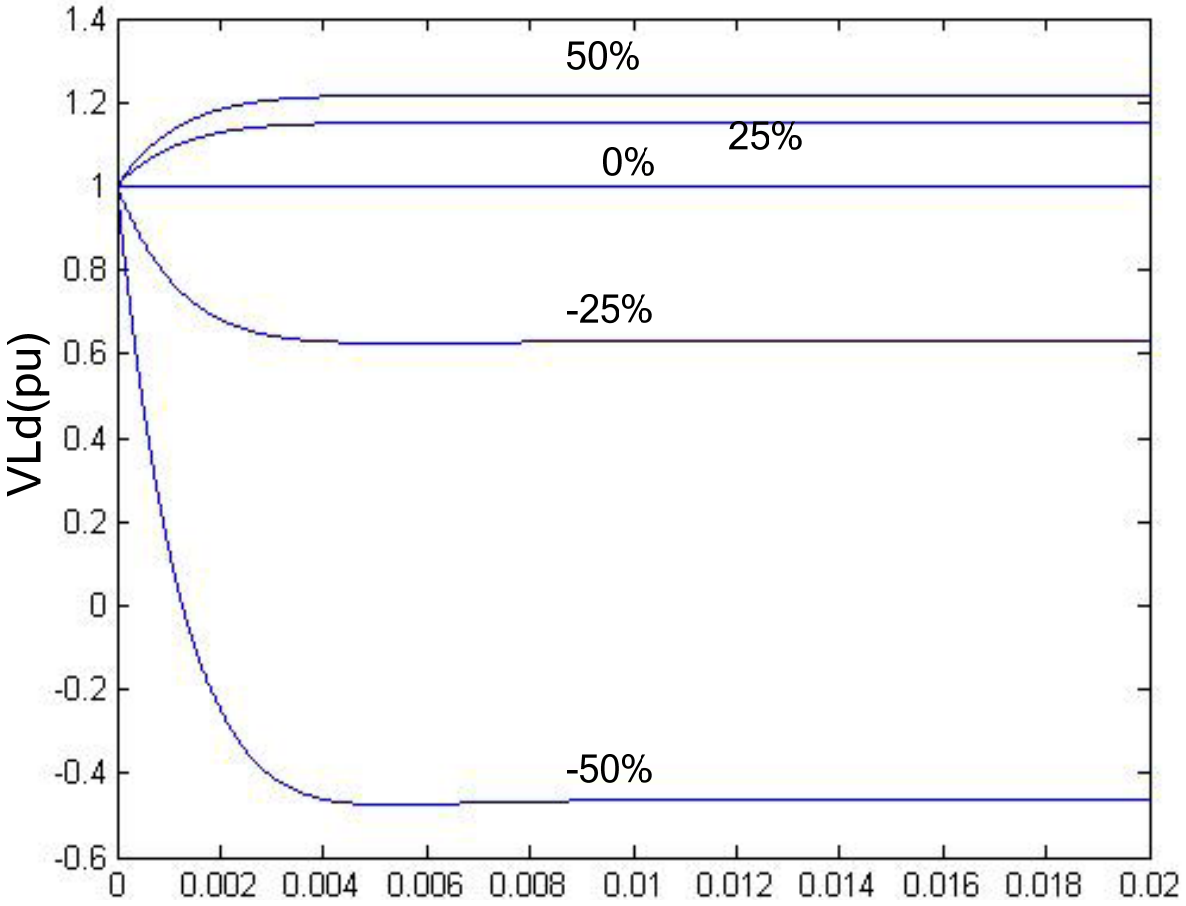


Fig.5.7. Voltage amplitude drift in constant current control with CPL during power outage

The voltage envelope expression in terms of system parameters and power difference value ΔP_{pu} is shown in equation (8):

$$V_d(t) = 1 + \Delta P_{pu} R_{pu} Z_{cpu} \sqrt{\frac{e^{-\frac{2\omega t Z_{cpu}}{R_{pu}}} (1 + e^{\frac{2\omega t Z_{cpu}}{R_{pu}}} - 2e^{\frac{\omega t Z_{cpu}}{R_{pu}}} \cos(\omega t))}{R_{pu}^2 + Z_{cpu}^2}} \tag{5.8}$$

5.4.3. Load voltage transient analysis in constant current control mode with constant power load

If the control mode is chosen to be constant current control but the load is CPL type, the voltage envelope is shown in Fig.5.7 and equation (9).

$$V_d(t) = 1 + \Delta P_{pu} Z_{2cpu} R_{2pu} \sqrt{\frac{e^{-2K}(1 + e^{2K} - 2e^{K} \cos(\omega t))}{R_{2pu}^2 + Z_{2cpu}^2}} \tag{5.9}$$

the voltage magnitude (and frequency) change. The voltage change rate is determined by the power differences between the DG generation and load demand. So the islanding operation can be successfully detected by monitoring DG terminal voltage before the voltage reaches pre-determined limits (e.g. 0.88pu to 1.1 pu).

Load shedding is defined as the process in which a part of the system loads is disconnected according to certain priority in order to steer the power system from potential dangers with the least probability of disconnecting the important loads [102]. To avoid microgrid operating out of the allowable voltage or frequency range quickly after islanding occurs, intelligent load shedding need to be implemented to cut off some least important loads to maintain the balance between load demands and DG generation. The approach for intelligent load shedding is to detect the voltage change rate after the main power outage. Fig.5.8 shows the voltage change rate when voltage amplitude reaches the limits (0.88pu/1.1pu) at constant power control mode with CPL case. As shown in Fig.5.8, the voltage change rate is closely related to the power difference between DG generation and load demand during power outage. The expression or plot of voltage change rate can be obtained by calculating the derivative of voltage envelope expression during the transition, from which the amount of load to be shed before switching to the voltage control mode for islanding operation can be determined.

However, in current control mode with constant impedance case, the equation for the voltage changing rate can be derived as equation (10), in which $K = \frac{\omega t_1 Z_{Cpu}}{R_{pu}}$. If the voltage changing rate at a time t_0 can be detected, the voltage envelope in the transient can be determined. Therefore, the power difference value and load shedding value can be calculated.

Fig.5.9 shows the smooth transition from constant current control to constant voltage control with intelligent load shedding based on voltage behavior for a pre-outage power mismatch of $\Delta P = -25\%$ and $\Delta P = -50\%$ respectively.

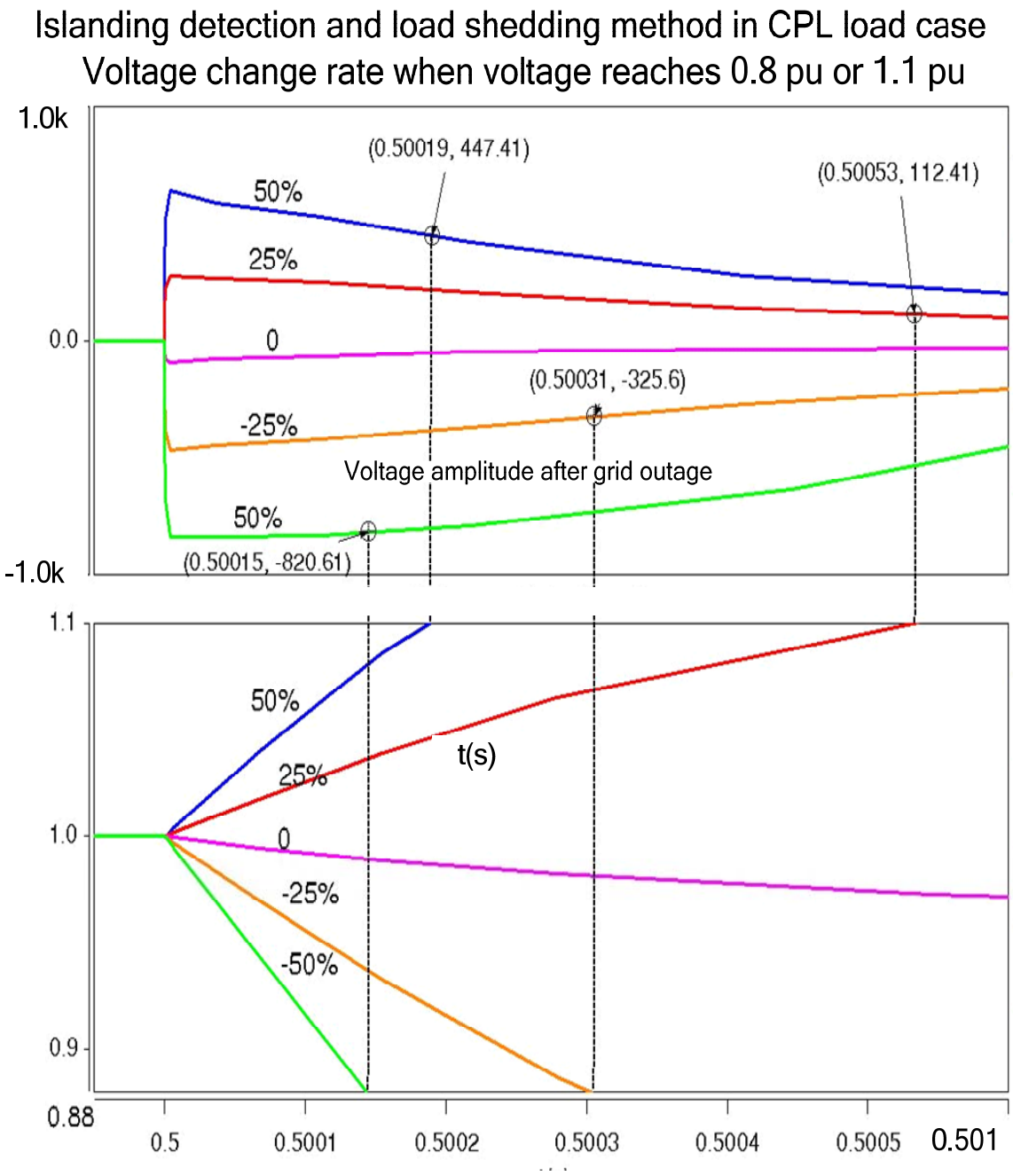


Fig.5.8. Voltage amplitude in transient and its change rate when voltage reaches 0.88 or 1.1pu

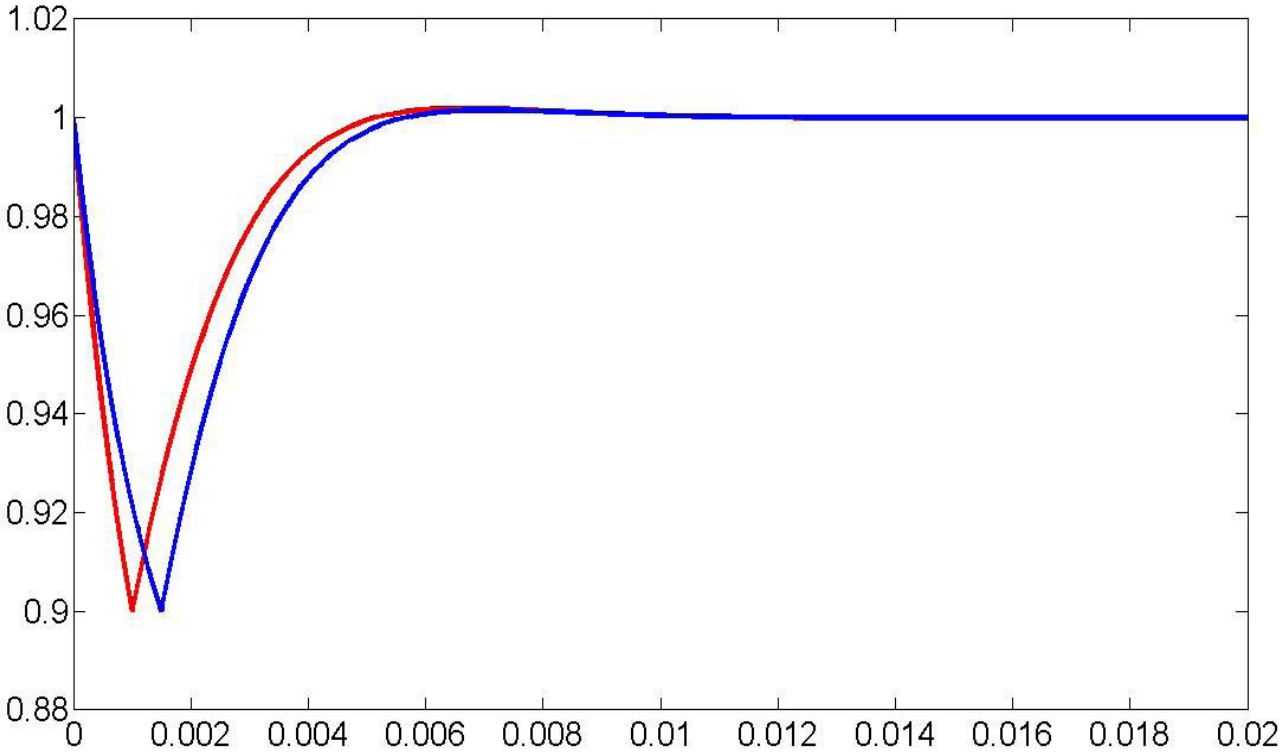


Fig.5.9. Transition from current control to voltage control with load shedding

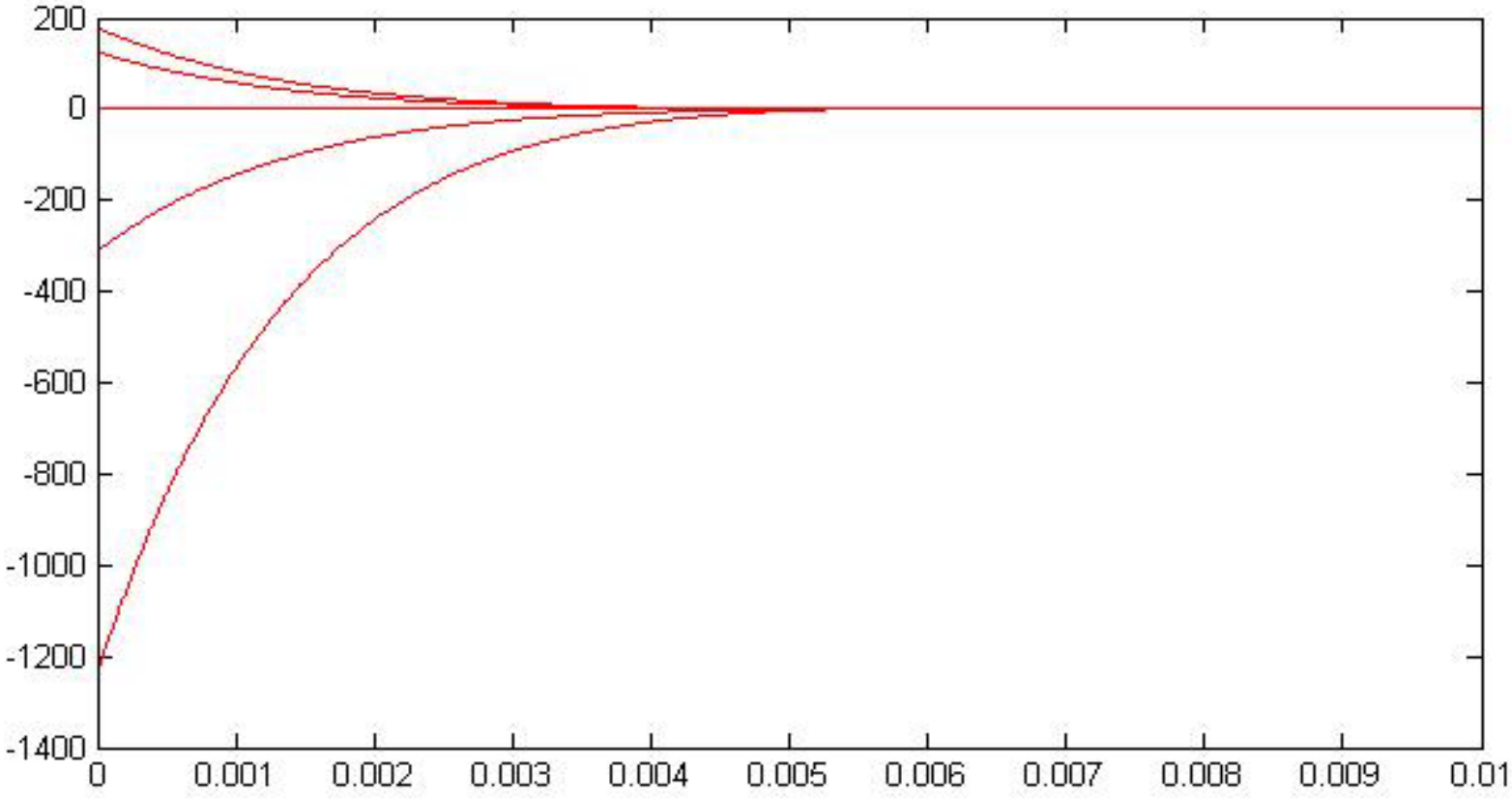


Fig.5.10. Voltage change rate vs power difference at constant current control mode with CPL

$$s = \frac{e^{-2K}\omega \cdot \Delta P_{pu} Z_{cpu}(e^{K}\sin(\omega t)R_{pu} + (-1 + e^{K}\cos(\omega t)))Z_{cpu})}{\sqrt{(1 + e^{-2K} - 2e^{-K}\cos(\omega t))({R_{pu}}^{2} + {Z_{cpu}}^{2})}} \tag{5.10}$$

Third, in current control mode with CPL case, the voltage amplitude slope at different power difference is shown in Fig.5.10 which can be used to determine the load shedding value at different voltage slope when the voltage reach 1.1pu/0.8pu or at a fixed time t_0.

5.6. Simulation results

When a power outage occurs on the main grid, and islanding has been detected, the DG system must switch to voltage control mode in standalone system to provide a constant voltage to local sensitive loads. Fig.5.11 shows the voltage amplitude waveform obtained from simulation for power differences of -50% and -25%. The power outage occurs at t=0.5s, and the voltage begins to drop. When it reaches the lower limit (0.88pu), the load shedding

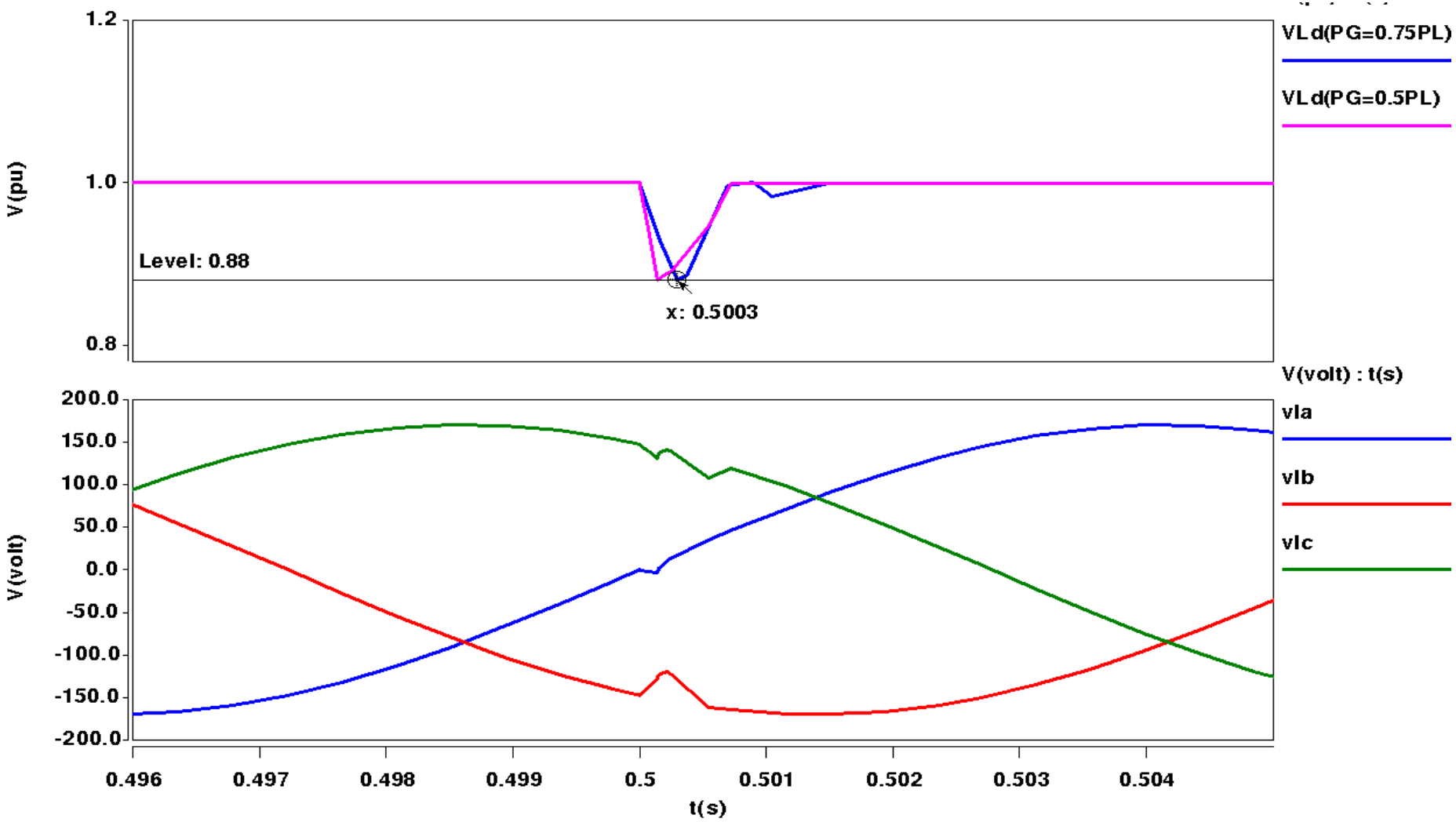


Fig.5.11. Voltage amplitude (with $\Delta P = -25\%, 50\%$) and three phase voltage waveforms(with $\Delta P = -25\%$) during an islanding transition

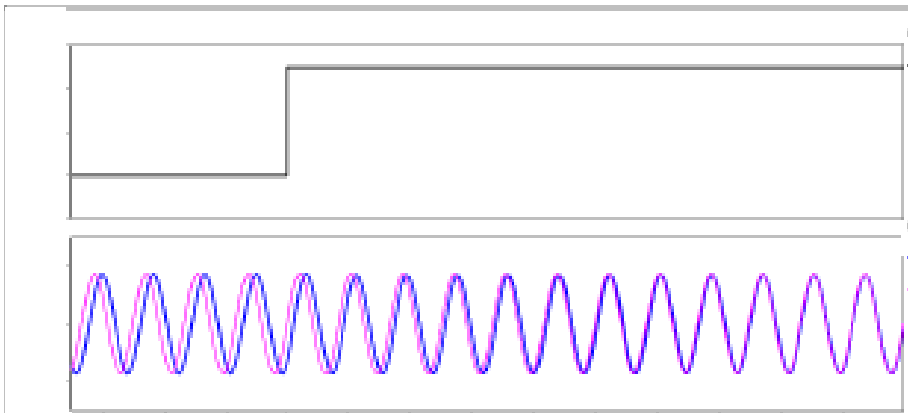


Fig.5.12. Synchronization for grid re-connection

method is used to cut off certain loads, and the DG system is switched from constant power control mode to constant voltage control mode. Then, the output voltage will be returned back to 1pu without oscillation.

Fig.5.12 shows the synchronization of voltages at both ends of the PCC when the synchronization algorithm start to work at t=0.6 seconds in the intentional islanding mode. The proposed algorithm successfully forces the voltage at the DG to track the voltage at the grid after 0.18 seconds.

5.7. Summary

Through this chapter, the voltage behavior in transition during power outage, islanding detection and load shedding algorithm have been studied. For constant power load, constant power control mode is usually been used in grid-connected system and for constant impedance load, current control mode is utilized. In the transient from grid-connected to standalone operation, the change of voltage amplitude and frequency,also the change rate varies with the power difference between DG generation and load demand. The islanding detection and load shedding algorithm is based on this feature. Some simulation results are shown to demonstrate above theory analysis.

CHAPTER 6 CONCLUSIONS AND FUTURE WORK

6.1. Contributions

In micro-grid inverter standalone mode, the proposed multi-loop control scheme is capable to achieve high-quality dynamic and steady state performances under both linear and non-linear loads. Moreover, its design is also simple and requires only an accurate knowledge of output filter parameters. Finally, only the output voltage needs to be sensed provided that dc-link voltage is constant.

In micro-grid inverter grid-connected mode, the possible wide range of grid-impedance variations can challenge the design of the controller, especially when the grid-impedance is highly inductive. The proposed robust current controller with the explicit robustness in terms of grid impedance variations to incorporate the desired tracking performance and stability margin. By properly selecting the weighting functions, the synthesized H∞ controller exhibits high gains at the vicinity of the line frequency, similar to the traditional PR controller, meanwhile it has enough high frequency attenuation to keep the control loop stable.

In the transition from grid-connected mode to standalone mode, the proposed voltage based and current control based algorithm can force the current to decrease to zero at a short time thus provide seamless transfers between the two operating modes for the inverter, avoiding the temporarily uncontrolled output voltage.

When the islanding happens, the inverter output voltage amplitude and frequency, also the change rate varies with the power difference between DG generation and load demand The proposed intelligent islanding detection and load shedding scheme can detect the grid outage fast and do the load shedding accurately.

6.2. Recommendations for future work

For parallel inverter operations, the power sharing between several inverters should be taken into account. So an outer power loop should be added to both of the voltage loop in standalone mode and current loop in grid-connected mode. Also the droop control law needs to be adopted according to the output impedance of the inverter.

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