POWER CONVERTER CIRCUITS FOR VOLTAGE BOOSTING, BALANCING AND RELIABLE OPERATION OF ENERGY SYSTEMS

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ABSTRACT

POWER CONVERTER CIRCUITS FOR VOLTAGE BOOSTING, BALANCING AND RELIABLE OPERATION OF ENERGY SYSTEMS

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Hybrid electric vehicle (HEV) and alternative energy have received growing attention nowadays, due to their contribution to the sustainable development. In these systems, power electronic circuits play a key role in bridging over the differences between sources and loads. The thesis investigates power converters to interface the energy sources and to prolong the life of the critical energy storage devices.

The boost converter in commercial HEV powertrains meets obstacles to upgrading the rating while downsizing the converter. A four-level dc-dc converter, and its special case—a 3X dc-dc converter that operates at three discrete voltage ratios, can overcome the drawbacks by dramatically reducing the inductance requirement. The operating principles, the current ripple, the power loss analysis and a clamping circuit are introduced. The concept is verified by the experimental results from two 30-kW and 55-kW prototypes.

Yet, for other applications like FC, PV and TEG, it is beyond the ability of the 3X dc-dc converter to attain high boost gain. Thus, a new switched-capacitor dc-dc converter is proposed. The component cost comparison and the power loss analysis demonstrate its many features such as low component power rating and count, low capacitance requirement, light weight and high efficiency. The features are validated by a 450-W prototype.

For the needs of converting the dc power to ac and vice versa, a family of transformer based impedance source (trans-Z-source) inverters is proposed. They possess the buck-boost functionality and the reliable operation against shoot-through/open-circuit fault, which are

unavailable in traditional voltage source and current source inverters. Compared to the existing Z-source inverters, they exhibit the increased voltage gain and reduced voltage stress in the voltage-fed trans-Z-source inverters, and the expanded motoring operation range in the current-fed trans-Z-source inverters. Two 3-kW prototypes prove the analysis of the voltage-fed and current-fed trans-Z-source inverters respectively.

To reduce the number of the serially connected battery cells/modules that are used in the energy systems, an improvement of a battery balance circuit is presented via phase-shift control. Each pair of battery cells are paralleled with a magnetically coupled half-bridge balance circuit. This cost-effective solution is able to achieve cell balancing and defective cell tolerance with more evenly distributed current stress, less component count and lower device ratings than its counterparts. Experimental results on Li-ion batteries verify the concept.

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Chapter 1 Introduction

1.1. Background and Motivation

As the concerns about energy crisis and climate change grow, governments and businesses are increasingly investing technologies of alternative energy sources and more environmentally friendly vehicles worldwide. Alternative energy sources encompass a host of types and applications, such as fuel cell (FC), photovoltaics (PV), wind, tide, microturbine, biomass, geothermal resources, and so on. Unlike traditional energy sources, they are green and offer sustainable solutions to the current energy needs. Another solution adopted worldwide is to mitigate the dependence and consumption of fossil fuel via hybrid electric vehicles (HEVs). The economical and environmental benefits from commercial HEVs now stimulate the global interest in developing plug-in hybrid electric vehicles (PHEVs) and pure electric vehicles (EVs). In addition, the research on thermal electric generation (TEG) recently emerges to reduce exhaust heat from internal combustion (IC) engines by converting waste heat into electricity to charge the 12-V battery and to power auxiliary loads in vehicles.

Yet, alternative energy sources like solar, wind and tidal wave are not dispatchable by their own. These are only available when there is adequate sun, wind and tide. Voltage swells and sags can occur by just injecting the power into the system when they are available. To accommodate the intermittent and variable behavior of these resources, energy storage devices can be engaged in a complete energy system. Energy storage devices include, but not limited to, batteries, super capacitors, superconducting magnetic energy storage (SMES), flywheels, compressed air energy storage, and pumped hydro. Among them, batteries have found the widest applications ranging from electronic devices like cellular phones and laptops to HEVs in addition

to their applications in alternative energy systems. With the aid of batteries, it is possible to continuously utilize the renewable energy, such that the power system capacity for high demand period is increased. It has already been well-known that batteries play a crucial role of storing energy from regenerative breaking and providing energy when it is needed HEVs and EVs.

Besides the fact that batteries are employed in both systems, there are many things in common between the applications of power electronics circuits for transportations and for renewable energy systems. Power electronic circuits interface energy sources and a variety of loads, as one means of fully utilizing the maximum energy available in the energy system, and meanwhile prolonging the cycle and calendar life of batteries. For instance, dc-dc converters and dc-ac inverters are employed both in a HEV and a PV generator. The dc power from the source needs to be boosted and then converted into the useful ac power that can drive a vehicle or that can be directly interconnected with the utility grid. Furthermore, a successful marriage has been made between a hybrid electric vehicle and a PV generator in a newly developed third-generation Toyota Prius [1]. Because of similar functions of these power electronics interfaces, the thesis will focus on power converters to address issues in HEVs/EVs and in alternative energy systems. The following paragraphs will begin with a briefly introduction of the common electrical characteristics of some typical alternative dc sources; afterwards it will review the characteristics and issues of the batteries; the reviews will disclose several common issues to be addressed; thereby, a comprehensive solution from the power electronics point of view will be given to improve the entire energy system from both system level and cell/module level.

1.2. Typical Electrical Characteristics and Issues of Some DC Energy Sources

Many alternative dc energy sources like FC, PV, TEG and etc are made up of serial and/or parallel connections of basic low-voltage cells. For instance, fuel cells are stacked in series to provide sufficient voltages, say, 240~380 V in a FC vehicle [2]. There are many types of fuel cells, among which the Proton Exchange Membrane (PEM) and Solid Oxide Fuel Cells (SOFCs) are mainly considered for automotive. FCs is sometimes also called as FC battery since it is also electrochemical device. In fact, FC creates electricity as long as the reactants (hydrogen and oxygen) are refueled externally, unlike a battery will either run down or need recharge. The energy density of a typical fuel cell stack is 200 Wh/L, which is nearly ten times of a battery. It has energy conversion efficiency of around 40~60%, and can be even higher with heat recovery [3]. It has been considered the highest among a variety of alternative energy sources. The V-I characteristics of a basic fuel cell is shown in Figure 1.1 [3]. The theoretical EMF of a cell at zero current and 80 °C and 1 atm gas pressure is $V_0 = 1.16V$. As the current density increases, the actual voltage at the electrical terminals drops dramatically. It indicates that, when directly fed by a FC stack in a vehicle, the inverter sees a wide variation from the dc bus. If not properly compensated for this variation in the motor control system, this may create stability problems in the drive system [4]. To this end, a unidirectional dc-dc boost converter is usually preferred. Another reason for the voltage boosting is that a large number of series cells are otherwise needed, which can lead to reduced reliability. That is, if a single cell fails open, the entire stack stops functioning because the current flow is interrupted [3]. Additionally, the FC stack is not fast enough to produce the needed hydrogen to meet the sudden load changes. Hence, battery and

supercapacitor have been employed as an energy buffer for it [5].

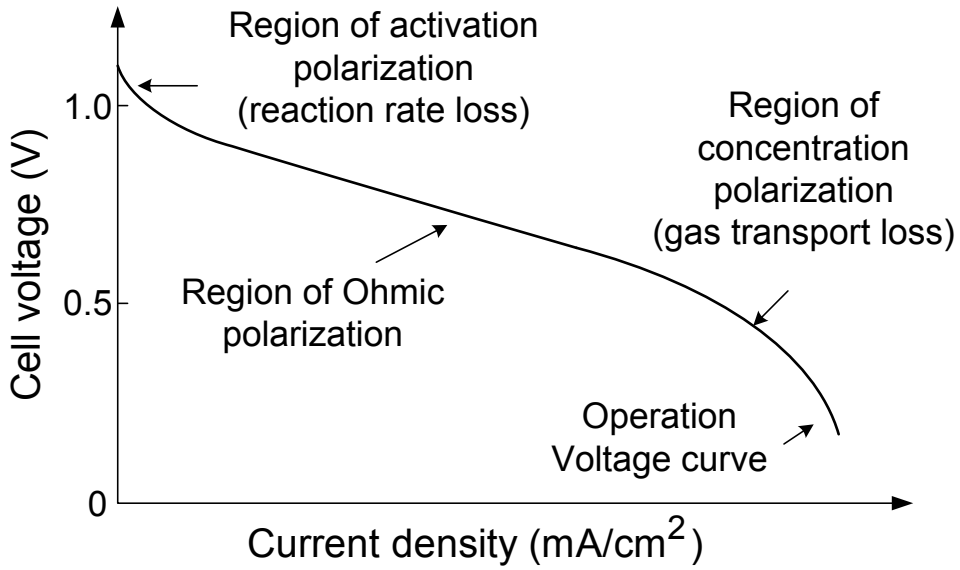


Figure 1.1. V-I characteristics of a basic fuel cell.

Similarly, a typical PV panel (or module) usually consists of 36~72 cells connected in series [6]. As can be seen from the V-I characteristics in Figure 1.2, each PV cell only has an open-circuit voltage of less than 1 V. A 160-W PV panel has an output voltage of only 24~38 V in the defined maximum power point range [7]. Depending on the power rating, an array of PV panels may be serially connected for enough voltage and power to fulfill the load demand. Indeed, PV panels in an array are never exactly identical and the scenario is deteriorated when some panels are shaded. The resultant current out of the whole array and the efficiency are thereby determined by the least efficient panel and indeed the cell. The present PV module light-to-electricity efficiency is still very low (<15%), and the power generation capability may be reduced to 75~80% of nominal value due to aging [6].

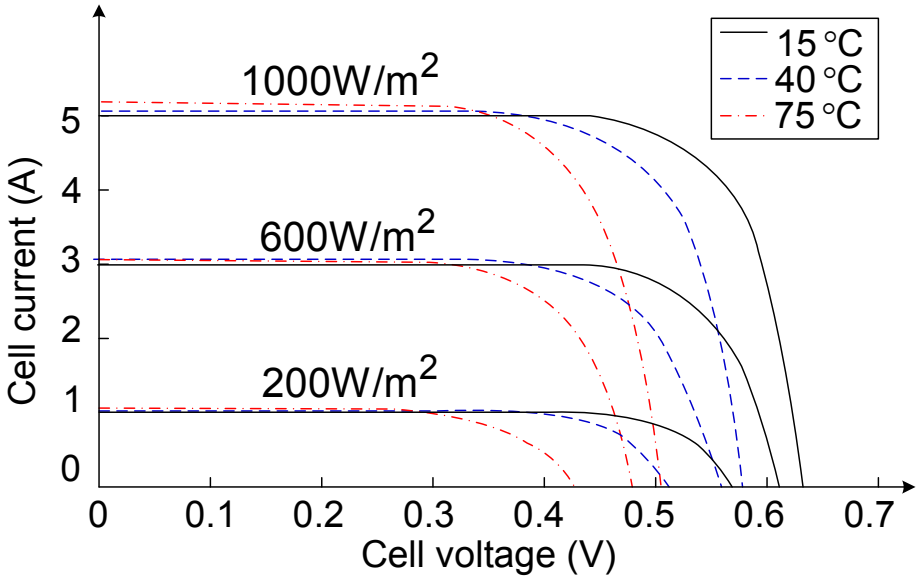


Figure 1.2. V-I and V-P characteristics of a PV cell*.

(For interpretation of the references to color in this and all other figures, the reader is referred to the electronic version of this dissertation.)

*Model based on the British Petroleum BP5170 crystalline silicon PV module. Power at standard test condition (1000 W/m irradiation, and a cell temperature of 25 °C): 170 W @ 36.0 V. Legend: solid at 15 °C, dotted at 40 °C, and dashdot at 75 °C.

Not as well-known as FC and PV, TEG was used for the applications for space and military purposes in the past. Nowadays it has drawn more and more attention in automotive, as there are more concerns over the efficiency and the environmental impact of the IC engines. As its name implies, a thermoelectric (TE) module can generate electricity from a temperature gradient. Actually, when electricity is applied across it in turn, the TE module can generate heat on one side and behave as a refrigerant on the other side. A TE module is normally comprised of an array of N TE couples that are joined thermally in parallel and electrically in series, and each TE couple is a pair of pellets made up of dissimilar p and n type semiconductor materials, as illustrated in Figure 1.3 [8]. The voltage that one TE module can produce depends on the number

of thermal couples in series and the temperature gradient across it. According to a test result in [9] as shown in Figure 1.4 on a commercial TE module, one module only produces less than 5 V at the maximum power of under 5 W at 150 °C. Therefore, several modules have to be connected in series and in parallel to supply enough voltage and power. Again, too many modules in series are vulnerable to open-circuit failure.

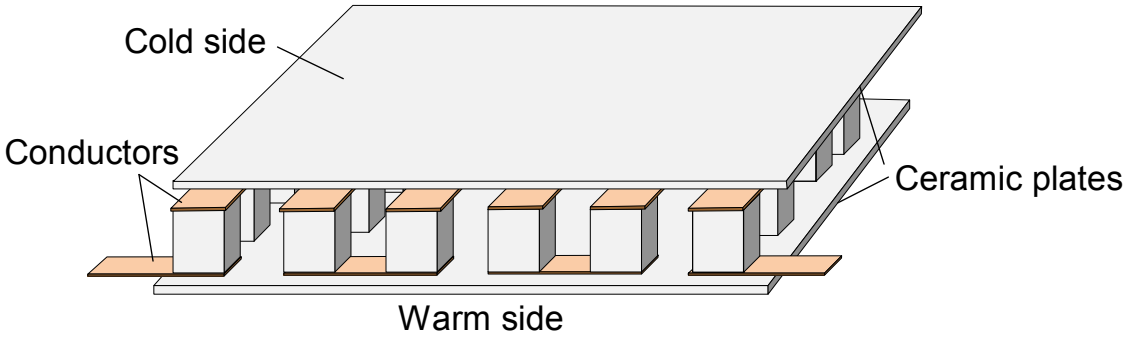


Figure 1.3. A TE module with two electrodes and ceramic plates.

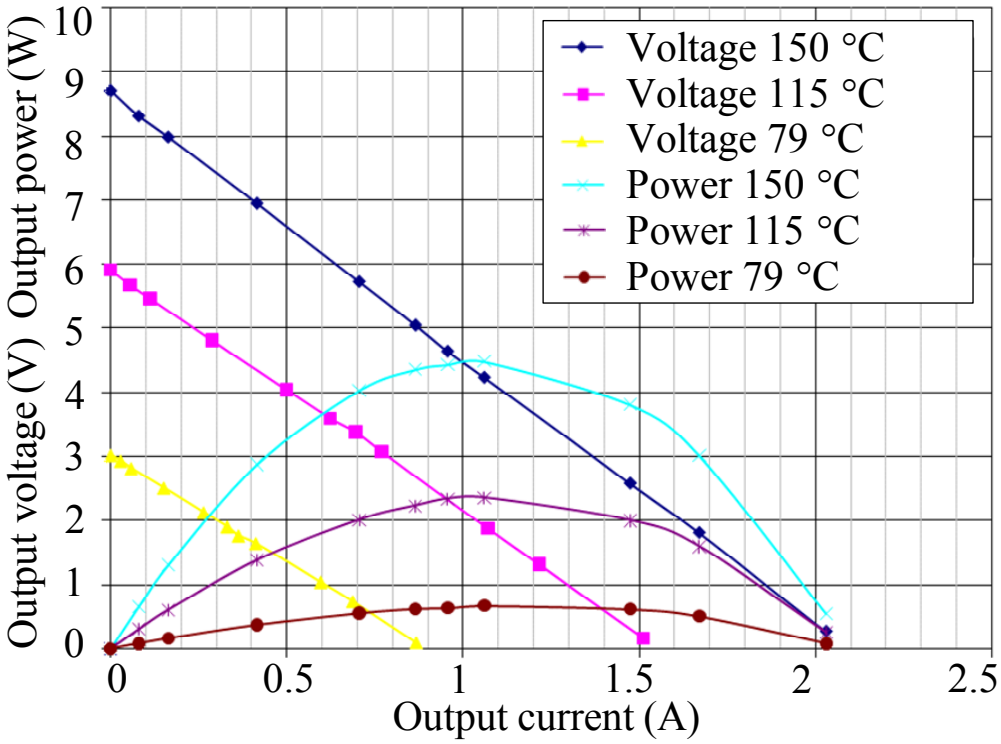


Figure 1.4. V-I characteristics of a commercial TEG module assembly from Tellurex.

1.3. Electrical Characteristics and Issues of Batteries

Before embarking on the issues associated with batteries, it is helpful to briefly review some of the important terminologies and characteristics. Viewed as a single unit, like in the HEV powertrain, a battery pack usually has many rechargeable battery cells connected in series to make sufficient voltage. One way to describe the battery capacity is Ampere-hour (Ah). It is the amount of current that a battery can deliver, at a constant rate (in fractions or multiples of "C") over a specified duration of time. For instance, a C/2 rate discharge of a 42-Ah battery can supply 21 A for two hours before the battery voltage reaches the end-of-discharge cut-off. Another property of most concern, especially for HEV designers, are the energy density (or specific energy) and power density (or specific power). The energy density is the amount of energy stored in terms of watt-hours per kilograms of a battery pack or cell; analogously, the power density is a measure of how much power can be extracted per weight at a specific rate of charge. While the battery is charged or discharged, the battery capacity is normally measured as state-of-charge (SOC). Although there are some different definitions of SOC, one common definition is defined as the percentage of energy currently stored in a battery compared to the battery's maximum capacity at the last full charge. The difference between the battery's maximum and minimum SOC is called the depth of discharge (DoD). The number of charge/discharge cycles is defined as cycle life when commonly referring to the battery life. When used over time, battery performance can substantially degrade in terms of capacity, power density, energy density and safety. Even when a battery is not in use, it is still aging by self-discharge [10]. Therefore, calendar life (service life/shelf life) is also specified to represent the ability of the battery to withstand degradation over time. Battery lifetime depends on battery chemistry, the depth of discharge, charge current and voltage profile, battery temperature and

battery capacity termination level.

There are a plenty of rechargeable battery chemistries, such as the Lead-acid, Nickel-Cadmium (NiCd), Nickel-Metal Hydride (NiMH), reusable Alkaline and so on. Their nominal cell voltages are quite low, as listed in Table 1.1. Among them, Lead-acid battery is widely used for the 12-V starting-lighting-ignition (SLI) battery in vehicles. They also find applications in hospital equipment, wheelchairs, emergency lighting and UPS systems. NiMH batteries are used in most HEVs currently sold in the US. It has the proven longevity in cycle life and calendar life, fast discharge capability and an overall history of safety. Plus, it is environmental friendly. However, its primary demerits are the limitation in energy density and power density, and low prospects for future cost reduction [11].

Recently, a class of Lithium-ion (Li-ion) and Li-ion-polymer batteries are expected to be more suited than NiMH for the more demanding HEVs, such as PHEV with all-electric operation in charge depleting mode. The main difference between the Li-ion and Li-ion-polymer is that a solid ion conductive polymer replaces the liquid electrolyte used in a standard Li-ion battery, although most polymer batteries also contain an electrolyte paste to lower the internal cell resistance [10]. There are various kinds of Li-ion batteries, but the most popular chemistries in production can be narrowed down to three according to the cathode materials: Lithium-cobalt-oxide, Lithium-manganese-oxide and Lithium-phosphate. The general characteristics of some Li-ion batteries are listed in Table 1.2. Their characteristics vary a lot from different electrode and electrolyte chemistries and manufacture technologies. Nevertheless, compared to other rechargeable batteries, they have relatively high cell voltage, high energy density, high power density, very good cycle life (from hundreds to a few thousand cycles [12, 13]), and low self-discharge (3~5% [10, 12]). They are also environmentally friendly. These properties make Li-ion

batteries have great potential for automotive applications. However, the high chemical reactivity of lithium brings in higher risk to longevity and safety, such as simultaneous Li-plating, oxygen gas evolution and the flammability of the electrolyte solvent. Therefore, Li-ion batteries call for more careful control over the cell voltage and operation temperature than other battery chemistries do. Overcharge and over-temperature will degrade the capacity quickly and even cause permanent damage.

Table 1.1. Nominal voltage per cell in general for typical batteries [12]

Battery type	Lead-Acid	NiCd	NiMH	Reusable Alkaline
Nominal cell voltage (V)	2	1.2	1.2	1.5

Table 1.2. General characteristics of Li-ion batteries using various chemistries [13]

Chemistry (Anode / Cathode)	Cell voltage max/nom. (V)	Energy Density (Wh/kg)	Cycle life (deep)
Graphite / $NiCoMnO_2$	4.2 / 3.6	100-170	2000-3000
Graphite / Mn spinel	4.0 / 3.6	100-120	1000
Graphite / $NiCoAlO_2$	4.2 / 3.6	100-150	2000-3000
Graphite / Iron phosphate	3.65 / 3.25	90-115	>3000
Lithium titanate / Mn spinel	2.8 / 2.4	60-75	>5000

The Ragone plot in [14] compares battery cells/packs vs. several PHEV goals. It represents trade-offs between power density and energy density for a given battery chemistry. The present battery technologies still fall short of the ever-growing demand especially for PHEVs and EVs

on power density and energy density, never mention the lifetime, safety, and cost. No matter what kind of battery is employed and what inherent trade-offs are among its attributes, the expected attributes of a battery pack can be summarized as:

- High capacity with small size and light weight;
- Safety and long-term reliability;
- Long cycle life and calendar life;
- Low cost;
- Environmental friendly.

When the battery cells are connected in series for the high voltage demand and have experienced hundreds of high-rate charge/discharge cycles, another problem comes out. Individual cells may age differently due to the variance in chemical and electrical characteristics and thermal condition. As time goes by, the capacity of some cells will deviate from the others over multiple charge/discharge cycles. If they are not periodically balanced with the rest of the cells, some could gradually be driven into over-charged or under-discharged, either of which is prone to damage and eventually completes the failure of the whole battery pack. As a result, without cell balancing, a battery may typically be used in the range of 20% to 80% SOC, providing a battery usage of only 60% [15]. If the SOC range can be enlarged, a smaller battery pack is allowed for a desired output capacity. This can result in a large saving in overall weight, even when the weight of the balancer is counted in. Furthermore, its environmental impact involves fewer chemical materials and the released recycle stress to some extent. In commercial products, the battery management system (BMS) monitors every cell or module, but can only discharge the surplus cells in a lossy manner.

1.4. Power Converter Interfaces

The above renewable energy sources and batteries face the common issues of low-voltage and uneven characteristics in cells. For the sake of reliability and life time, it is better to have a smaller number of cells or modules in series. However, the loads demand high voltage (e.g. 200~650-V dc bus in HEVs), high charge/discharge rates, high tolerance to faulty cells. Besides, there are a number of applications that need to convert the generated dc power into a regulated ac, and vice versa, depending on the applications. A power converter interface has to bridge over the differences between energy system and load. From the viewpoint of system level, an interface circuit should be capable of voltage boosting, dc-ac conversion and regulation, so as to properly rate the energy system. From the viewpoint of the energy storage device, another issue is how to boost the effective utilization, run-time and calendar life for uneven cells/modules, and thereby enhance the reliability, which will be discussed in the next section.

A general block diagram of typical dc-ac interfaces is shown in Figure 1.5. It is divided into two energy paths for two energy sources. In the first path, the upper dc-dc converter stage takes in the uncontrolled input dc voltage and boosts it to a higher voltage, with or without galvanic isolation. The followed dc-ac inverter produces the required voltage and frequency from the boosted dc voltage. The inverter is a generic circuit in renewable energy systems, motor drives, uninterruptible power supplies, active power filter and etc. Note that the general dc-ac inverter stage here includes the ac filter for the grid interconnection, but not for the vehicle applications. The second energy path involves the battery energy storage, or sometimes supercapacitors. The battery can be directly paralleled to the inverter dc bus, or can go through a dedicated bidirectional dc-dc boost converter as shown in Figure 1.5. When charging the battery, the inverter rectifies the ac back to dc.

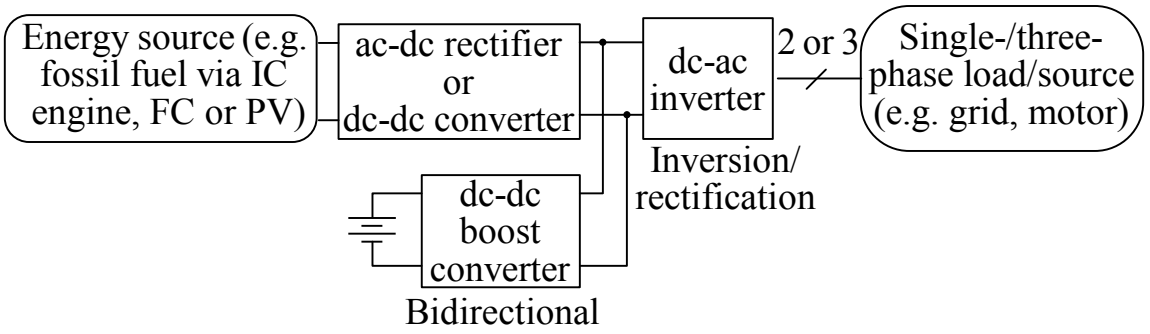


Figure 1.5. Block diagram of a typical power electronic interface for energy systems

More specifically, an example of the above system, a PHEV powertrain, is given in Figure 1.6. PHEV is like a conventional HEV, whereas it uses a larger battery pack that can be charged from the utility via an on-board charger. It has been reported that it can be driven up to 40~50 miles without using a drop of gasoline. When the electric charge of the battery is depleted to certain level, the downsized gasoline engine kicks in to either charge battery as the car moves, or it is the primary source of propulsion until re-plugging the charger. The power converter interface consists of a dc-dc boost converter for the high voltage (HV) battery, a dc-ac inverter for the traction motor to drive the vehicle, and a second dc-ac inverter for the generator that is linked to the engine. There are also configurations with no dc-dc converter between the battery pack and the inverter. Nonetheless, the configuration in Figure 1.6 provides more flexibility and improves system performance. The reason is well justified. If the battery pack feeds inverters directly, due to limited cell voltage, more cells are required for high voltage high speed operation. Plus, more cell monitor, balance and protection units have to get involved. Conversely, at the low speed operation, a low-voltage dc bus is expected. A less flexible dc bus voltage leads to degraded efficiency. Admittedly, the conventional dc-dc boost converter has its limits in terms of size, weight and efficiency for PHEVs, especially for high temperature operation.

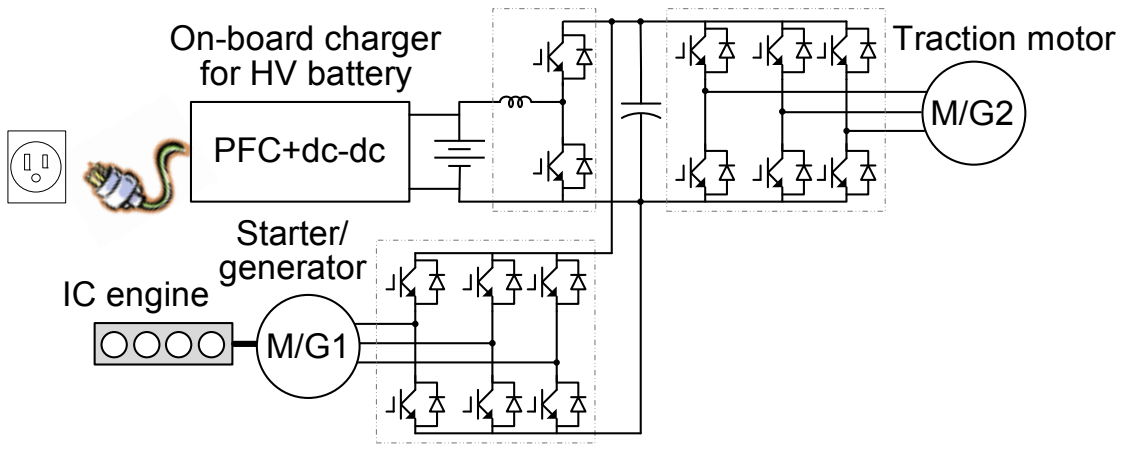


Figure 1.6. A power converter example for PHEV.

Replacing the energy path for the IC engine with a FC plus a dc-dc boost converter yields a powertrain configuration for a FCV, as shown in Figure 1.7 [16]. The power converter (dc-dc converter plus dc-ac inverter) matches the low-voltage and relatively slow output of fuel cell stack to the high voltage requirement and the rapid load change of the propulsion drive system. To start the motor, the power is sourced by the 12-V SLI battery, whose power electronic circuitry is not included in the powertrain configuration. When the vehicle is in the steady-state speed range, only the fuel cell stack provides the propulsion power, and it may also charge the battery. During rapid acceleration, both the fuel cell and the battery power the vehicle. When the break pedal is pressed, the battery gets charged, in which its bidirectional dc-dc converter operates in buck mode. For the sake of cost, there are also different configurations with either the fuel cell or the battery directly connecting to the inverter dc bus [4, 13]. Nevertheless, the addition of dc-dc converters allows for the use of low-voltage dc sources and the optimal design of the propulsion system irrespective of the fuel cell voltage. Alternatively, a new converter topology called Z-source inverter has been proposed in [17-20] to combine both the voltage boost and the dc-ac inversion.

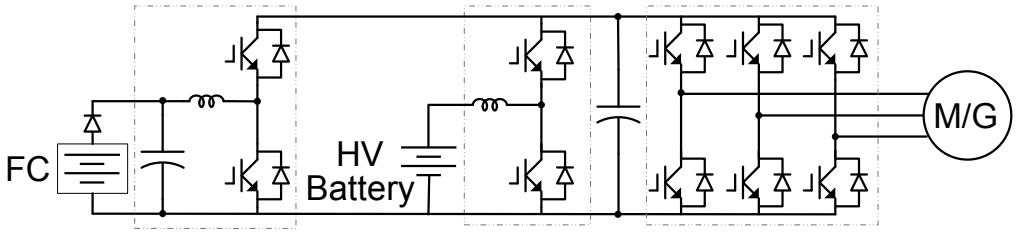


Figure 1.7. Power converter for fuel cell vehicle.

As for grid-connected PV systems, there have been many power converters, since they have less constraint than FCVs do. Most of them are transformer-isolated for high voltage gain and isolation ([6, 7, 17-23]). Meanwhile, non-isolated converters are adopted in Japan and European countries where galvanic isolation is not required [7, 24-26]. One of the PV inverters is shown in Figure 1.8, which embraces battery energy storage as well, such that it becomes possible to offset the daily and seasonal intermittency of the primary energy source, to smooth out load fluctuations, to damp out utility transients, and to facilitate islanding operation. In this configuration, several PV panels are connected in series and in parallel, and they feed a centralized two-stage power converter. In the first stage, the dc-dc converter boosts the PV voltage and tracks the maximum power point; in the second stage, the dc-ac inverter produces a regulated ac output to the local load and/or to the grid. This two-stage power converter is preferable to the one that has only a dc-ac inverter. The reasons are that the voltage from the PV panel is low and that the voltage-source inverter is essentially a buck-type converter. The shortcoming of the centralized configuration is that it cannot fully extract the maximum power point of individual PV panels due to the aforementioned unbalance from panel to panel. Hence, it has been reported in [6, 22, 27, 28] to equip each half-panel (or panel substring) with a modular dc–dc converter. These modular dc-dc converters can be in series (Figure 1.9(a)) or in parallel (Figure 1.9(b)) before connecting to a central dc-ac inverter.

Recently, there is a trend to also modularize the dc-ac inverter and integrate it with the dc-

dc converter into a plug-and-play device called as micro inverter [29, 30]. An example is shown in Figure 1.10. Its rating usually ranges from 150 to 300 W. Micro inverters attract much attention mainly because: 1) they are able to harvest the maximum capacity of each individual panels; 2) they are easy to install and are flexible to expand for any power rating; 3) the modular fabrication can yield high economical profits in massive production. Yet, the application of micro inverters presents some challenges, especially for the dc-dc converter. When fed by a 160-W PV panel with the voltage of 24 V at the maximum power point, the maximum voltage conversion ratio for the dc-dc converter has to be more than 12 times, so that the subsequent dc-ac inverter can produce a 110-V ac output for single-phase residential utility in US. The voltage ratio is more than doubled in Europe and in China. Transformers or coupled inductors [31, 32] have to be used for the dc-dc converter, since traditional non-isolated dc-dc boost converter has constrained voltage gain due to the parasitic resistive loss. Their demerit is the degraded efficiency and the high temperature issues on magnetic and electrolytic capacitors that precludes placing a micro inverter behind a PV panel. Even if this buck-type dc-ac inverter is replaced by the aforementioned Z-source inverter (or the later developed quasi-Z-source inverter) that have been proposed for PV generation in [33, 34], the attainable voltage boost gain is not high enough in practice.

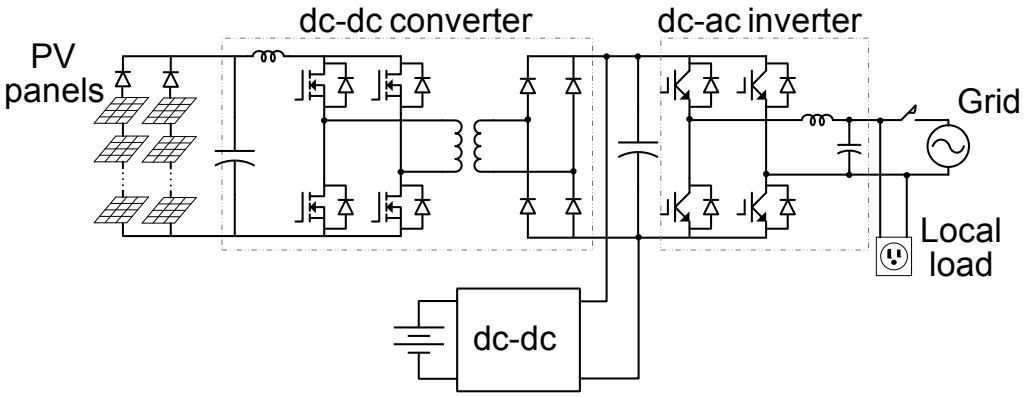
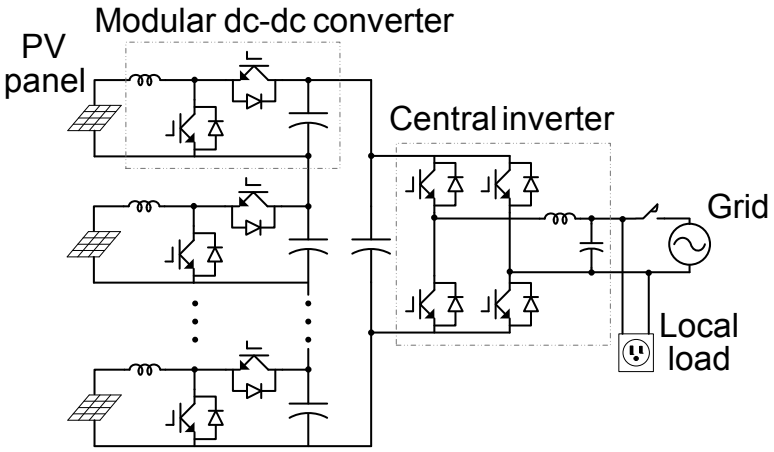


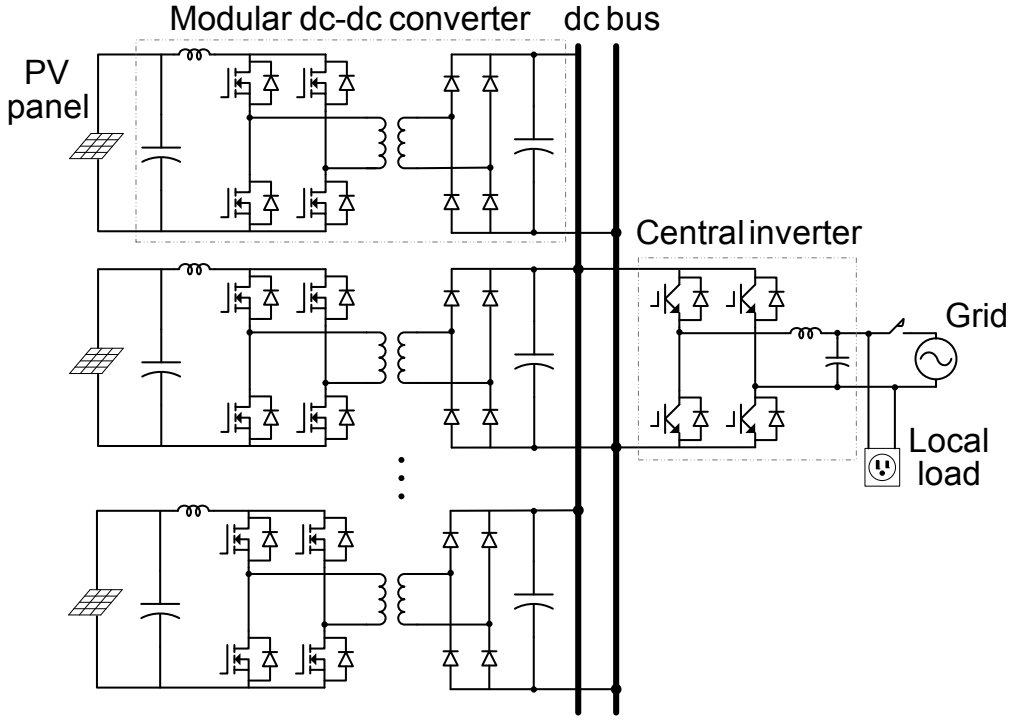
Figure 1.8. A centralized PV converter with battery energy storage.



(a) Series connection of modular dc-dc boost converters.

Figure 1.9. The configurations with modular dc-dc converters.

Figure 1.9 (cont'd)



(b) Parallel connection of modular dc-dc full-bridge converters.

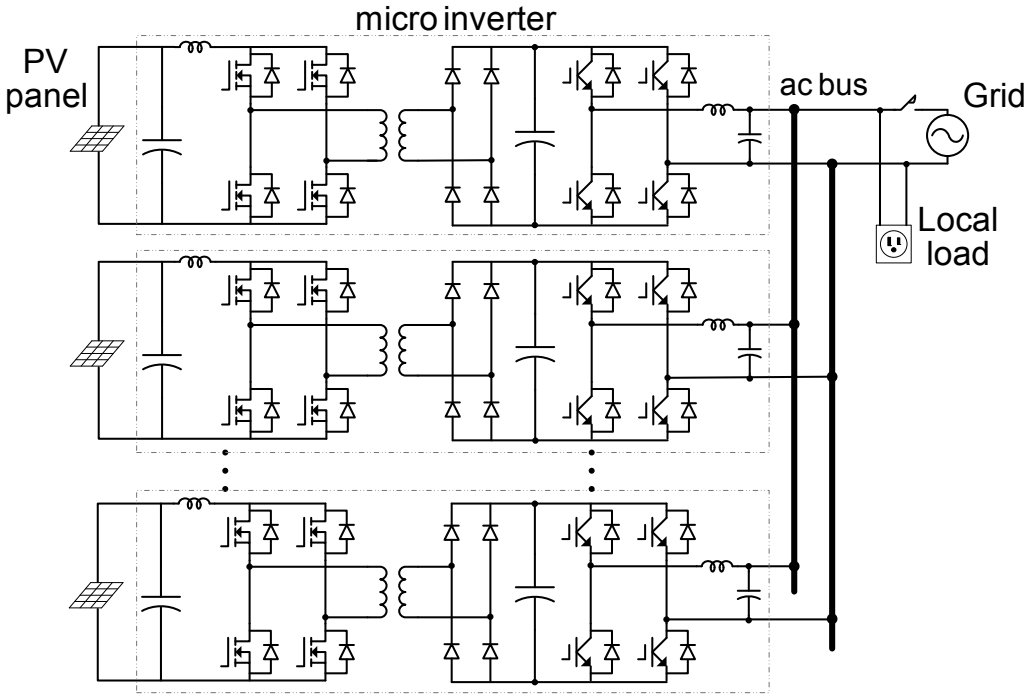


Figure 1.10. PV micro inverters.

Different from FC and PV, the present power converter interface for TEG is mainly a dc-dc converter [35-37]. Besides load interface, the dc-dc converter has to perform the maximum power point tracking or the power matching [38], since the produced voltage as well as the load varies.

It is expected that the development of scalable, modular, low-cost, highly reliable power electronic interfaces will improve the overall cost and durability of the above energy systems, because of similar functions of these power electronics interfaces [39]. It would be best if one circuit could fit into all the applications. Unfortunately, in the real world, no circuit is perfect to address all the issues in a variety of applications. Several dc-dc converters and dc-ac inverters are examined in this thesis to improve the power conversion systems. Firstly, a four-level flying-capacitor dc-dc converter is explored as an alternate to overcome the drawbacks of the conventional dc-dc boost converter interfacing the battery and the inverter in PHEVs. When it operates at three discrete output/input voltage ratios, the converter reduces the inductance requirement to a minimal value (almost zero). Yet, for other applications like FC, PV and TEG, it is beyond the ability of the flying-capacitor dc-dc converter to attain high boost gain. Therefore, secondly, a new switched-capacitor dc-dc converter is proposed. It has much lower current stress and lower total device power rating than the flying-capacitor dc-dc converter, which are fairly desirable features for dc-dc converters with high voltage gain. Thirdly, for the dc-ac power conversion, a class of transformer based impedance source (trans-Z-source) inverters is proposed. They possess the buck-boost functionality, and the reliable operation due to the immunity to shoot-through/open-circuit. None of these are unavailable in traditional voltage source and current source inverters. Moreover, their new features, thanks to their transformer windings, lend themselves to HEVs, FC and PV applications.

1.5. Approaches to Improve the Energy Storage System

When we take a closer look at the energy storage device itself besides the system-level circuitry, the problems of the over-charge and deep-discharge concerns, the restricted charge/discharge rate, low cell voltage and etc call for the micro-management of the cells connected in series. The success of PHEVs and EVs greatly depends on the performance and lifetime of the battery. The state-of-the-art electric vehicle can not go thus far with a full charge cycle as the internal combustion engine vehicles do with a tank of fuel. Moreover, it takes just a couple of minutes to refuel a 15-Gallon tank in the internal combustion engine vehicle, whereas it takes hours to recharge a PHEV. The battery pack made up of low-voltage cells is large, heavy, and costly. Even the Li-ion batteries, which are poised to be a preferable choice for the next generation of electric vehicles, face several technical challenges to be addressed as in the other batteries. Their sensitive nature leaves many concerns in terms of longevity and safety. The development of new materials and structures in the device level has been improving the performance of batteries. At the same time, the advanced circuitry and energy management are indispensable in boosting the performance and propelling the applications. Hence, this section summarizes some approaches to boost the effective capacity and the reliable lifetime of the batteries.

A. Cell balance and defective cell bypass

As posed to the passive balance method used in the commercial BMS, many active cell balance circuits were proposed in literature [40-69]. They are essentially small dc-dc converters transferring energy to equalize each cell actively and efficiently. In this way, each cell approaches the same float voltage at the end of the charging process, or the same cutoff voltage at the end of the discharging process. Consequently, a wider charge/discharge range can be

achieved, thus the effective battery pack capacity will be expanded. However, many existing solutions are either low-performance or high-cost, which preclude their implementation. Furthermore, it is more desirable that a battery pack can have some fault tolerance, so that as much juice can be squeezed out of the pack as possible. Otherwise, the capacity of the rest cells is wasted even though only one or very few cells are malfunctioning. A cost-effective solution to handle defective cells/modules will give rise to significant profit to the battery applications. Therefore, the battery balance circuits and its functionality of defective cell bypass will be investigated in the thesis.

B. Battery fault protection and status prognosis

Safety is a crucial criterion for battery usage. Batteries are very sensitive to voltage and current profiles, charging speed, depth of discharge and battery temperature. The overcharge, over-discharge, over-current, over-temperature and etc are taken care of by the battery monitor and protection circuits. These circuits are integrated in a single IC [70-72], with small profile, very low power consumption and strong immunity to EMI noise. Besides that, many ICs have been developed in some companies like Texas Instrument for not only monitoring the battery status but also providing the remaining SOC. Some researches have also been reported in [73-75] to diagnose the health status of batteries in advance. They aim to predict the battery usable capacity and the discharge termination level. Basically, the data from manufacturer or from periodic tests were first collected after necessary data processing. Battery model or empirical equation was built using regression methods off line, according to the data like open-circuit voltage, current, temperature. During operation, the pertinent data are sensed for calculating the present and remaining SOC, and/or impedance which are closely related to battery capacity. Compared to historic data, the life time or aging is forecasted. The health status prognosis can

actively enhance the battery reliability and offer information for maintenance and fault diagnosis. The onset of problems can be aware of, and actions can be taken before they develop to a cascade failure. This approach not just prevents permanent capacity loss, but also reflects the true end of battery life. Otherwise, a battery is considered to have come to the end of life when the battery capacity drops below 80% of its rated capacity. In fact, batteries can still deliver usable power, although they have shorter run-time [10]. As a mater of fact, very accurate estimation is a challenge for HEVs, due to the difficulty in correct battery model and state of health estimation. The methods so far are based on a series of user-prescribed charge/discharge profiles, and specified average current and duration, whereas the depth of cycle, load condition, and thermal environment may differ with various drive cycles and environmental conditions.

C. Combination of batteries and super-capacitors

Batteries naturally have high energy density yet low power density. It is favorable to size the battery in PHEVs and EVs by the energy demand for a desired all-electric range. At the same time, a battery pack also has to meet the frequently irregular and rapid acceleration and regenerative braking in vehicles. Unfortunately, batteries that are tailored for a little higher power density usually have to sacrifice the energy density and are more costly, which ends up with an oversized and expensive design [76, 77]. Nowadays super-capacitors (or so-called ultra capacitor, electrochemical double layer capacitor) are gaining popularity for their high pulse power, fast charge/discharge response, high efficiency and long calendar life. A general comparison with batteries is listed in Table 1.3. As shown in the table, supercapacitor is good at handling large impulse power with high efficiency due to its small time constant and very low ESR, whereas slow power exchange rate are preferential for batteries. Supercapacitors with longer cycle life are more suitable for frequent charge/discharge than batteries. Besides,

supercapacitors have long shelf life and excellent performance over a wide temperature range including both hot and extreme cold conditions [77, 78].

Table 1.3. Comparison between supercapcitors and batteries [77]

Characteristics	State-of-the-art Li-ion battery	Supercapacitor
*Charge time	~3-5 minutes	~1 second
*Discharge time	~3-5 minutes	~1 second
*Cycle life	<5,000 @ 1C rate	>500,000
Specific Energy (Wh/kg)	50-100	5
Specific power (kW/kg)	**1-2	5-10
Cycle efficiency (%)	From less than 50% to more than 90%	From less than 75% to more than 95%
Cost/Wh	$0.5-1/Wh	$10-20/Wh
Cost/kW	$50-150/kW	$15-30/kW

* Time for discharge and charge of the useable total energy stored in the devices

**Power capacity of the battery for short multi-second pulses at 90% efficiency

If batteries are designed for the maximum energy density and supercapacitors for the maximum power density, combining them together can gain the maximum capacity, fast response, long cycle life and high efficiency. Supercapacitors act as a temporary reservoir, it can be fully charged before acceleration and can be empty before regeneration [79]. Otherwise, in current HEVs, the SOC for the batteries is managed with specific margin for regeneration. Plus, batteries will suffer from less impulse power that affects its lifetime. It is a significant thermal

burden shift from batteries to super-capacitors, which has the potential to reduce the overall thermal loading and enhance the safe operation of the vehicle regenerative energy storage system.

Since the terminal voltage of a battery pack is relatively constant, direct paralleling supercapacitors with the battery pack will limit the charge transfer capability. Instead, they can be actively coupled via dc-dc converters. Yet, despite the above advantages, the addition of supercapacitors and dc-dc converter(s) to the energy storage system would not be PHEV and EV designers' first selection, unless it can deliver superior cycle performance with long-term reliability, lower total size, less total mass, lower cost.

In addition to the above approaches, researchers have also studied the charging methods to improve battery thermal performance and safety [80, 81] or to reduce charging time [82]. It has been found important to choose the proper charge methods and termination levels for different types of batteries. Besides that, another interesting innovation is to use TEG to adjust the battery thermal environment [83]. Battery life could be extended if battery temperature is maintained in the optimum range for that battery chemistry.

1.6. Scope of the Thesis

The thesis is divided into two parts: system level circuits for the power conversion, and the cell/module level solutions for the battery energy storage itself. Chapters 2 to 4 propose several novel dc-dc converters and dc-ac inverters for voltage boost and dc-ac conversion. Chapter 5 deals with solutions for voltage balancing and reliable operation of one of the most costly devices — the rechargeable batteries.

Chapter 2 first explores the operating principle and current ripple of a four-level flying-capacitor dc-dc converter. A special case of the four-level converter, the 3X dc-dc converter is

presented. The transient control to limit the inrush current and the power loss analysis are provided. Additionally, a clamping circuit is proposed to mitigate the voltage spike at the diode reverse recovery. The analysis is verified experimentally.

Chapter 3 proposes another novel dc-dc converter that is derived from the flying-capacitor dc-dc converter. It features low component (switching device and capacitor) power rating, small switching device count and low output capacitance requirement. In addition to its low current stress, the combination of two short symmetric paths of charge pumps further lowers power loss. Therefore, a small and light converter with high voltage gain and high efficiency can be achieved. The operating principle, the features, the component cost comparison with its counterparts and the power loss analysis are introduced. Simulation and experimental results validate the principle and features of this topology.

Chapter 4 proposes a class of trans-Z-Source inverters which have buck-boost capability with a single power stage. They employ an impedance network of two transformer windings and one capacitor to couple the dc source and the inverter bridge. While inheriting the main features of its origin — the Z-source inverters, the new networks exhibit some unique advantages, such as the increased voltage gain and reduced voltage stress in the voltage-fed trans-ZSIs and the expanded motoring operation range in the current-fed trans-ZSIs, when the turns-ratio of the transformer windings is over one. Simulation and experimental results are provided to prove the analysis of the voltage-fed and current-fed trans-ZSIs respectively.

Chapter 5 first reviews the battery balance circuits and discusses the functionality of defective cell bypass for the reliable operation. A battery balance circuit is introduced that employs phase-shift control for the purposes of reducing the component count and rating while improving the balancing performance. Each pair of battery cells are paralleled with a

magnetically coupled half-bridge balance circuit. Charge is transferred directly from the surplus cells to the weak ones. This cost-effective solution is able to achieve cell balancing and defective cell tolerance with more evenly distributed current stress, less component count and lower device ratings than its counterparts. The principle is demonstrated by experimental results on four Li-ion battery cells.

Chapter 6 summarizes the work and suggests the prospective future work.

Chapter 2 A Variable 3X DC-DC Converter for Plug-in Hybrid Electric Vehicles

2.1. Introduction

Many commercial hybrid electric vehicle (HEV) systems, such as Prius, Camry, and Fusion, use a traditional bidirectional dc-dc converter to interface the battery and the inverter dc bus. For example, the powertrain configuration of the Camry hybrid is shown in Figure 2.1. In this system, the dc-dc converter boosts the battery voltage, from 244 V to three optimized discrete voltage levels up to 650 V according to the motor/generator speeds [84]. Combined with the continuous adjustment of modulation indices of the inverters, then both the motor and generator and their individual inverters are able to operate in the most efficient region to accommodate the wide speed and power demand of the vehicle. In this traditional dc-dc boost converter, an inductor is employed. Besides its large size and heavy weight, the lossy inductor limits the operating temperature. Because of the inductor, the efficiency of the dc-dc converter is relatively low compared to the inverter.

Nowadays, the economical and environmental benefits from commercial HEVs have spurred the global interest in further developing plug-in hybrid electric vehicles (PHEVs). For the pure electric drive operation of PHEVs, the dc-dc boost converter has to deliver the full power needed by the traction drive, not just the difference between MG1 and MG2 as would be the case in blended operation mode with the engine running (Figure 2.1). For example, the Prius' present dc-dc converter is rated at 20-kW peak power (10-kW continuous power) [85], which is not enough for all-electric operation at higher speeds and has to be upgraded from 20-kW to 55-kW peak power (30-kW continuous) for PHEV's pure electric drive. It is not viable to simply

resort to increasing the switching frequency to limit the size, weight and cost of the converter since the core and copper loss of the inductor will go up as a result of the increased switching frequency and the power rating. In addition, the semiconductor heat dissipation in the converter limits the switching frequency. Thereby, multi-phase dc-dc converters [86-88] were developed for high power HEVs and fuel cell vehicles (FCVs). The inductor design is still a challenging issue for increasing the converter efficiency and power density.

Multilevel dc-dc converter topologies [89-92] have been proposed for many applications. By contrast to the traditional dc-dc converter, a three-level flying-capacitor dc-dc converter greatly reduces the inductance requirement in addition to other benefits such as much lower device voltage rating and fast dynamic response [90, 91]. In this paper, further investigation and theoretical analysis are performed to utilize the multilevel structure to achieve high voltage boost and high power for PHEVs. A four-level flying-capacitor dc-dc converter is presented as shown in Figure 2.2 to replace the traditional dc-dc converter. This four-level structure can further reduce the input current ripple. More interestingly, a closer and further look into the input current ripple will reveal that the inductor can be eliminated or minimized when the converter operates at three discrete voltage ratios: 1X, 2X, and 3X. Power loss induced by the bulky inductor is diminished. Therefore, the operation of the four-level dc-dc converter at three discrete voltage ratios (thus named a variable 3X dc-dc converter) will be proposed later in this paper. The transition to achieve the three variable voltage ratios will be analyzed, followed by the experimental verification on a 55-kW 3X dc-dc converter prototype. It should be noted that a fixed 1:3 voltage ratio dc-dc converter has been introduced in [93, 94], however, they cannot be used for the above-mentioned HEV and PHEV applications that require variable voltage levels. The main new contribution of this paper resides in the introduction of the variable 3X operation

and smooth transition between voltage levels.

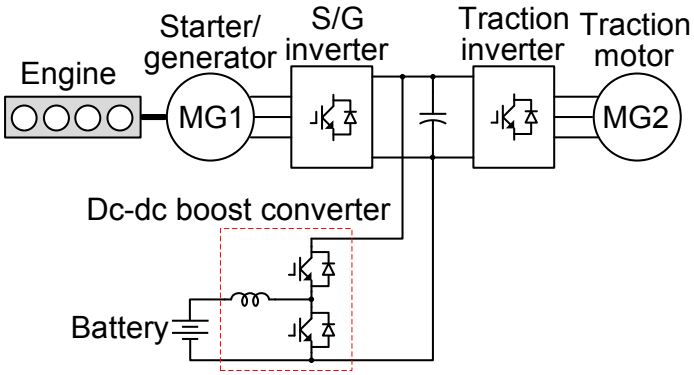


Figure 2.1. Powertrain configuration of conventional series-parallel HEV.

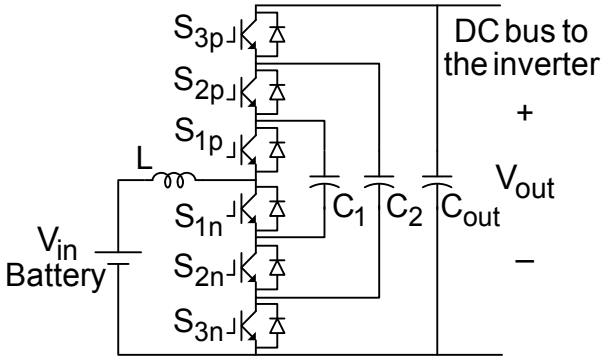


Figure 2.2. Four-level flying-capacitor dc-dc converter.

2.2. Four-Level Flying-Capacitor DC-DC Converter

In this section, the general operation and features of the four-level flying-capacitor dc-dc converter are explained and discussed first. The relationship between the input current ripple and voltage ratio is derived for the four-level converter and extended to the three- and two-level converters for comparison purposes. The current ripple comparison indicates a dramatic reduction of the inductance requirement. Analysis reveals three operation modes and the relationships between the different operation modes. In addition, the analytical results will be further used in a later section for transitions from one voltage level to another of the variable 3X

operation.

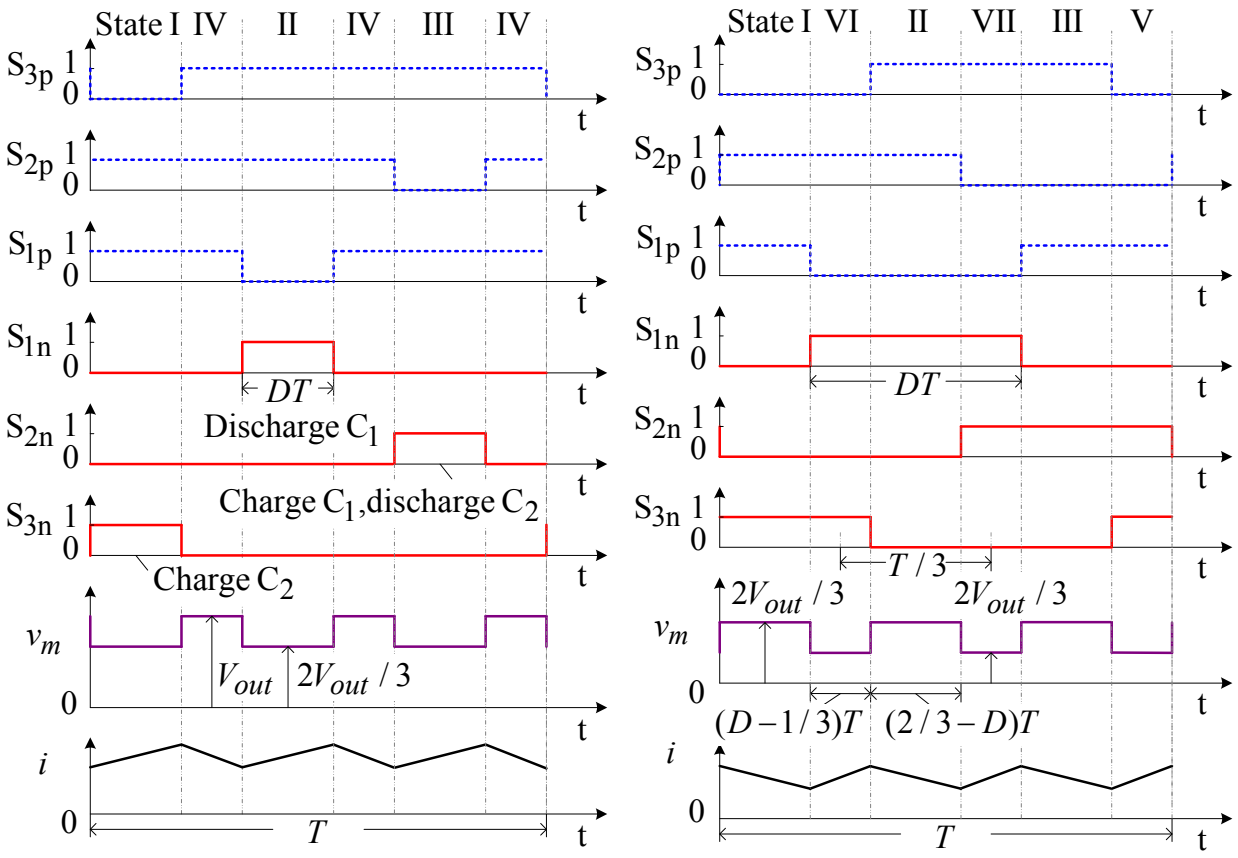
As shown in Figure 2.2, each pair of switches S_{jp} and S_{jn} (j=1, 2, 3) conduct complementarily and are clamped by capacitors C_1, C_2, and C_{out}. An input inductor (L) on the battery side plays the same role as in the traditional boost converter. It should be noted that this structure has the capability of bidirectional power flow. This paper focuses on the boost mode operation, that is, power flows from the battery (low voltage side, V_{in}) to the high voltage dc bus (V_{out}) to inverter(s). Under the boost mode, each lower-side switch S_{jn} is controlled as the active switch, and the anti-parallel diode of the high-side switch S_{jp} conducts as the complementary switch. This four-level converter can be operated as a three-level one as well, based on a switching pattern proposed in this paper.

First, the four-level operation can be divided into three operation ranges. The PWM signals and key waveforms in these three ranges are depicted in Figure 2.3(a), (b) and (c). The PWM signals for both upper and lower switches S_{jp} and S_{jn} are shown in the figures, thus valid for both boost and buck operations. For example, the PWM signals for S_{jp} as sketched in blue dash lines indicate the conduction intervals of the anti-parallel diodes in the boost mode, whereas they represent PWM signals for the switches in the buck mode. The switching states are shown in Figure 2.4. The voltages of capacitors C_1 and C_2 are controlled to be $V_{out}/3$ and $2V_{out}/3$, respectively. A duty cycle D is defined as the ratio of the duration that the switch S_{jn} conducts over one switching cycle, T. For $0 \le D \le 1/3$, as can be inferred from Figure 2.3(a), the converter operates in a sequence of Figure 2.4(a)-(d)-(b)-(d)-(c)-(d) over one switching cycle. The input

voltage V_{in} equals the average value of the leg voltage v_m in steady state according to the voltage-second balance of the inductor. The leg voltage v_m is switched between two potentials, $2V_{out}/3$ and V_{out}, as sketched in Figure 2.3(a). For instance, when only S_{3n} is turned ON as shown in the switching state of Figure 2.4(a), C_2 gets charged, making $v_m = 2V_{out}/3$; when S_{3n} is OFF as shown in Figure 2.4(d), the current freewheels through the anti-parallel diodes of S_{1p}, S_{2p} and S_{3p}, making $v_m = V_{out}$. Similarly for other switching states, when only one of the switches S_{jn} is ON as shown in Figure 2.4(a), (b) and (c), $v_m = 2V_{out}/3$; otherwise $v_m = V_{out}$ in the freewheeling states in Figure 2.4(d). Thus, one can get

$$V_{in} = \overline{V}_m = 3\left(\frac{1}{3} - D\right)V_{out} + 3D \cdot \frac{2V_{out}}{3} = (1-D)V_{out}. \tag{2.1}$$

During this operation range, each inner capacitor (C_1 and C_2) gets charged and discharged equally for a duration of DT over one switching cycle as shown in Figure 2.3(a). However, due to gate delays and device tolerance, the voltage of each capacitor C_1 and C_2 may settle down to a value slightly deviated from their theoretical values, $V_{out}/3$ and $2V_{out}/3$, respectively, as described in [95]. Therefore, in order to maintain their voltages as desired, an accurate duty cycle control is needed. This capacitor voltage balancing issue has been addressed and analyzed in the literature [91, 95-98].

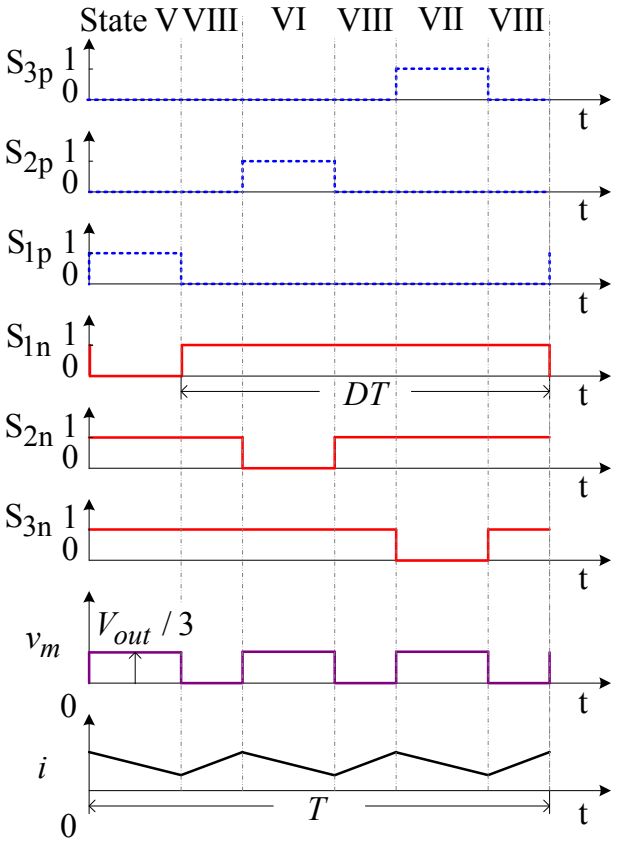


(a) 0 ≤ D ≤ 1/3.

(b) 1/3 ≤ D ≤ 2/3.

Figure 2.3. PWM signals and key waveforms of the four-level operation.

Figure 2.3 (cont'd)



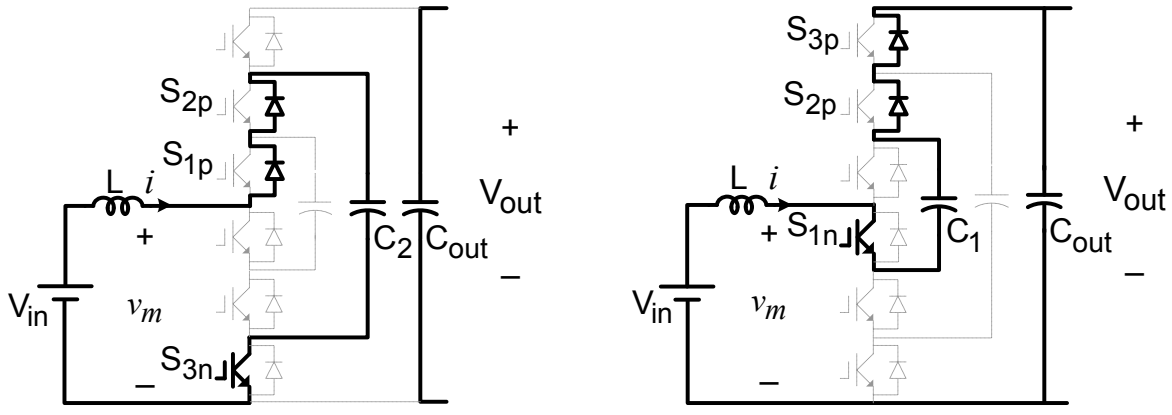
(c) $2/3 \leq D \leq 1$.

When the duty cycle increases and enters the range of $1/3 \leq D \leq 2/3$, three new switching states as shown in Figure 2.4(e), (f) and (g) replace the previous freewheeling state. As a result, v_m is switched between two potentials: $V_{out}/3$ and $2V_{out}/3$, as shown in Figure 2.3(b). The operating sequence follows Figure 2.4(a)-(f)-(b)-(g)-(c)-(e) over one cycle. Likewise, when $2/3 \leq D \leq 1$, a new state comes into play. All the switches S_{1n}, S_{2n} and S_{3n} conduct as shown in Figure 2.4(h). Consequently, v_m presents two voltage levels: 0 and $V_{out}/3$, as sketched in Figure 2.3(c). The corresponding operating sequence is Figure 2.4(e)-(h)-(f)-(h)-(g)-(h) repetitively. In spite of the above three variation ranges for D, it can be proven that the input and output voltage

relationship expressed in (1) always holds true. Apparently, it is the same as the traditional boost converter. The buck mode can be analyzed similarly. It can be proven that the output/input voltage ratio for the buck mode is also the same as that for the buck converter. However, it can be seen from Figure 2.3 that not only the effective switching frequency is tripled but also the volt-second across the inductor is minimized when seen from the inductor in this four-level converter, thus having great potential to reduce inductor requirements.

Given an input voltage V_{in} in (1), the duty cycle, D can be expressed as a function of V_{in} and V_{out}. According to the inductor current change in each state, the input current ripple can be expressed as a function of V_{in} and V_{out}:

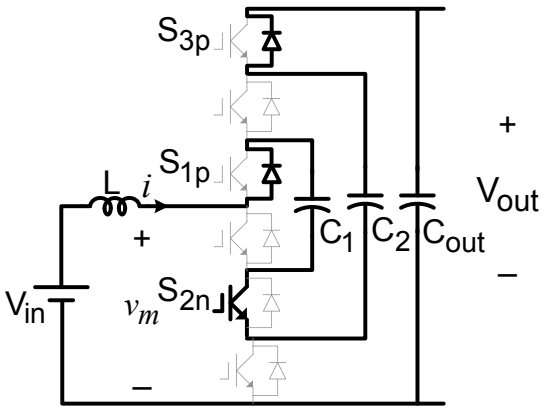
$$\Delta i = \begin{cases} \dfrac{V_{in}T}{L}\left(1-\dfrac{2}{3}\dfrac{V_{out}}{V_{in}}\right)\left(1-\dfrac{V_{in}}{V_{out}}\right), & for\ 1 \le \dfrac{V_{out}}{V_{in}} \le \dfrac{3}{2}; \\ \dfrac{V_{in}T}{L}\left(1-\dfrac{V_{out}}{3V_{in}}\right)\left(\dfrac{2}{3}-\dfrac{V_{in}}{V_{out}}\right), & for\ \dfrac{3}{2} \le \dfrac{V_{out}}{V_{in}} \le 3; \\ \dfrac{V_{in}T}{L}\left(\dfrac{1}{3}-\dfrac{V_{in}}{V_{out}}\right), & for\ \dfrac{V_{out}}{V_{in}} \ge 3. \end{cases} \tag{2.2}$$



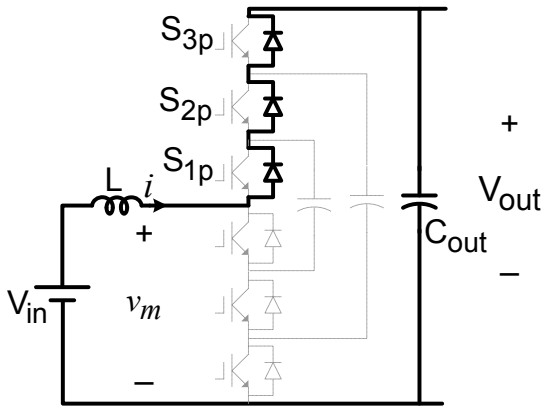
(a) State I. (b) State II.

Figure 2.4. Switching states of the four-level operation in boost mode.

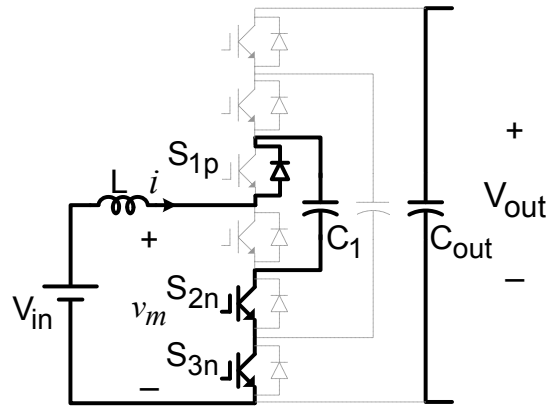
Figure 2.4 (cont'd)



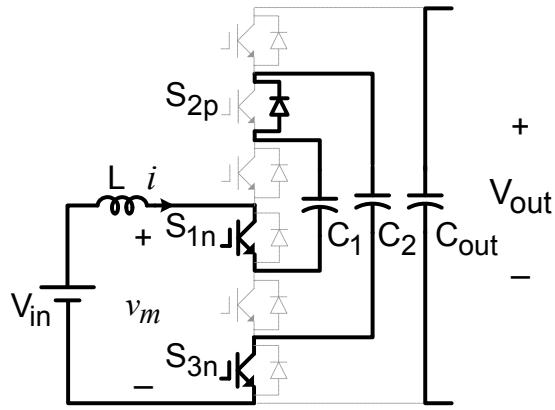
(c) State III.



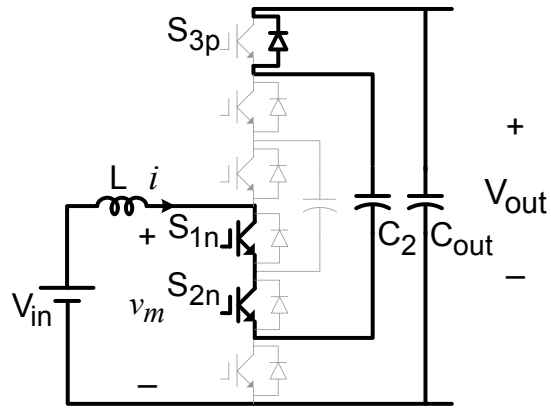
(d) State IV.



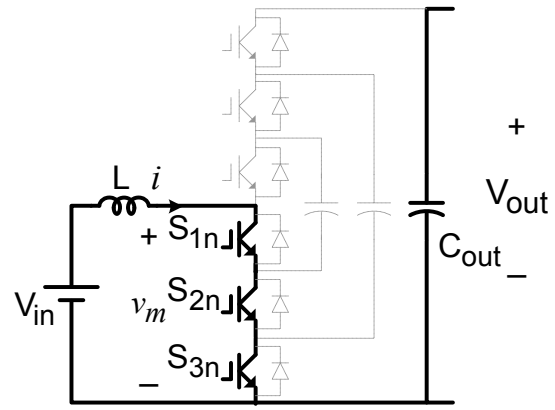
(e) State V.



(f) State VI.



(g) State VII.



(h) State VIII.

Second, the four-level converter can be operated as a three-level converter, when the

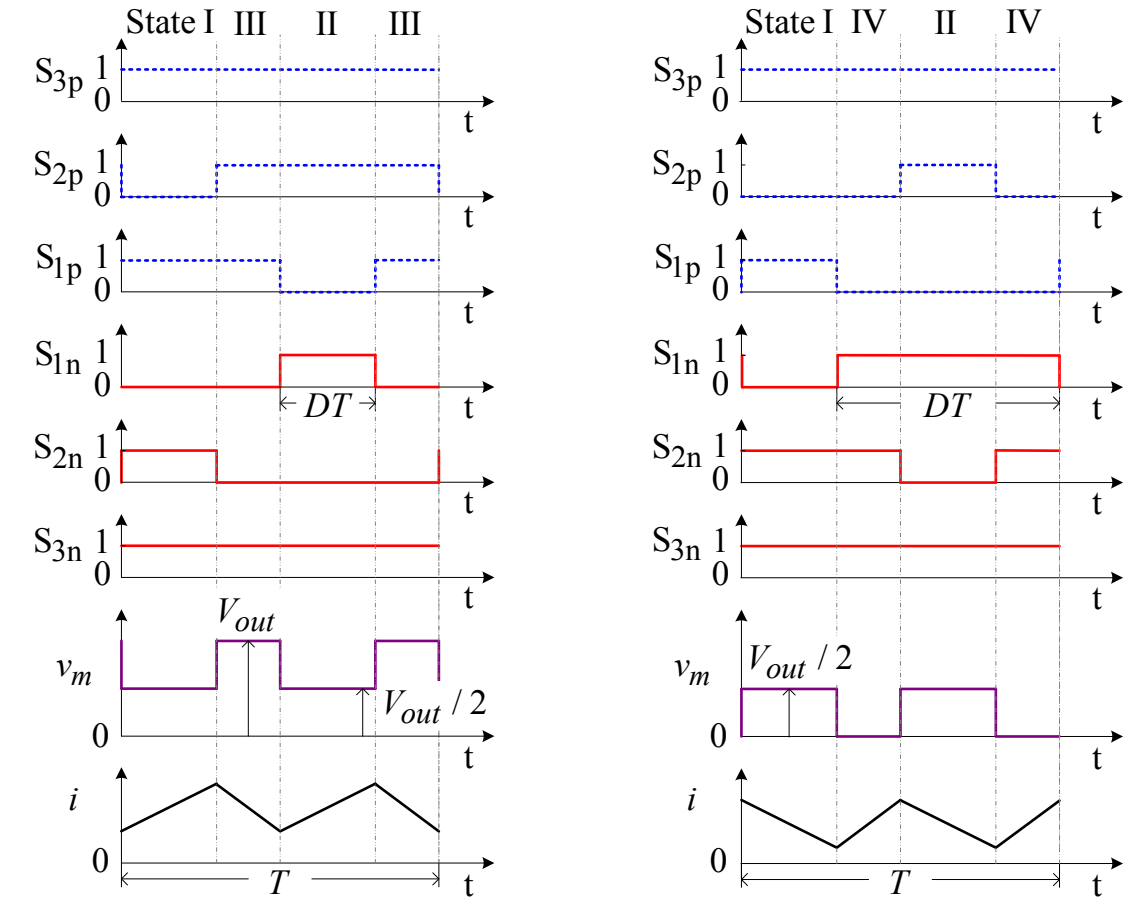
capacitors C_2 and C_{out} are connected in parallel by continuously turning ON switch S_{3n}. The PWM signals and key waveforms are shown in Figure 2.5. Note that the duty cycle, D is only the duty cycle for S_{1n} and S_{2n} in this case. Figure 2.6 shows the switching states for this three-level operation. The voltage of C_1 is controlled to equal $V_{out}/2$. By applying the same analysis as before, the three-level operation can be divided into two operation ranges. When $0 \le D \le 1/2$ as shown in Figure 2.5(a), the operation sequence is Figure 2.6(a)-(c)-(b)-(c); otherwise when $1/2 \le D \le 1$ as shown in Figure 2.5(b), the sequence is Figure 2.6(a)-(d)-(b)-(d). It was derived in [91] that the voltage relationship can be also expressed by (2.1). The current ripple can be obtained as

$$\Delta i = \begin{cases} \dfrac{V_{in}T}{L}\left(1-\dfrac{V_{out}}{2V_{in}}\right)\left(1-\dfrac{V_{in}}{V_{out}}\right), & for\ 1 \le \dfrac{V_{out}}{V_{in}} \le 2; \\ \dfrac{V_{in}T}{L}\left(\dfrac{1}{2}-\dfrac{V_{in}}{V_{out}}\right), & for\ \dfrac{V_{out}}{V_{in}} \ge 2. \end{cases} \tag{2.3}$$

For comparison purposes, the current ripple of the traditional two-level (2L) boost converter can be calculated as

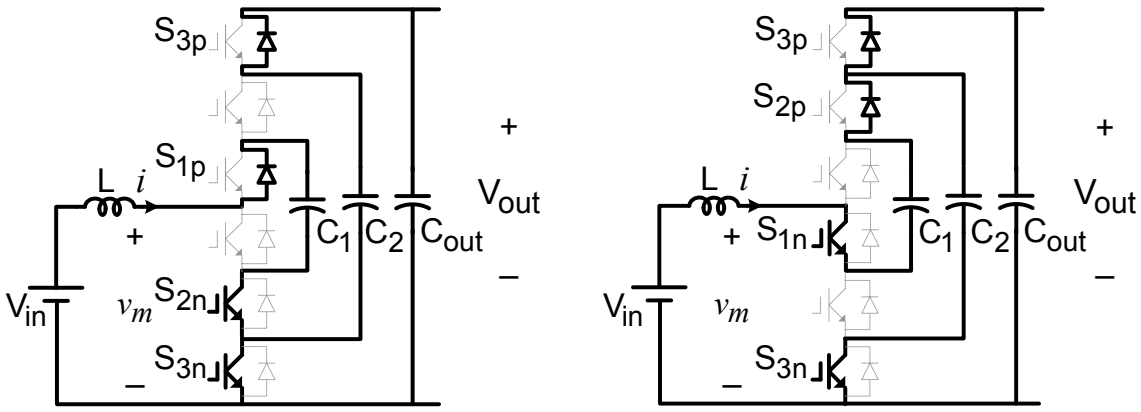
$$\Delta i = \frac{V_{in}T}{L}\left(1-\frac{V_{in}}{V_{out}}\right). \tag{2.4}$$

The normalized inductor current ripples of the four-level and three-level converters are compared with that of the traditional boost converter in Figure 2.7. The base value is the current ripple of the traditional boost converter at a boost ratio of three. It is evident that the maximum current ripple of the four-level converter is almost one tenth of the traditional dc-dc boost converter's over $1 \le V_{out}/V_{in} \le 4$. In other words, given the same current ripple specification, a much smaller inductor is sufficient for this four-level converter.



(a) $0 \le D \le 1/2$. (b) $1/2 \le D \le 1$.

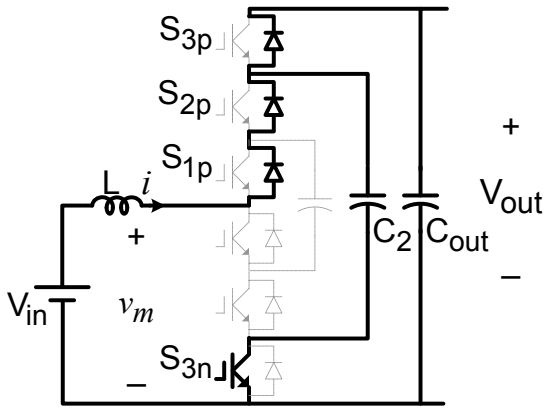
Figure 2.5. PWM signals and key waveforms of the three-level operation.



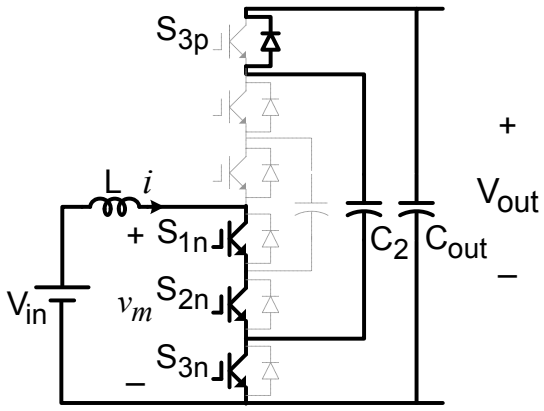
(a) State I. (b) State II.

Figure 2.6. Switching states of the three-level operation in boost mode.

Figure 2.6 (cont'd)



(c) State III.



(d) State IV.

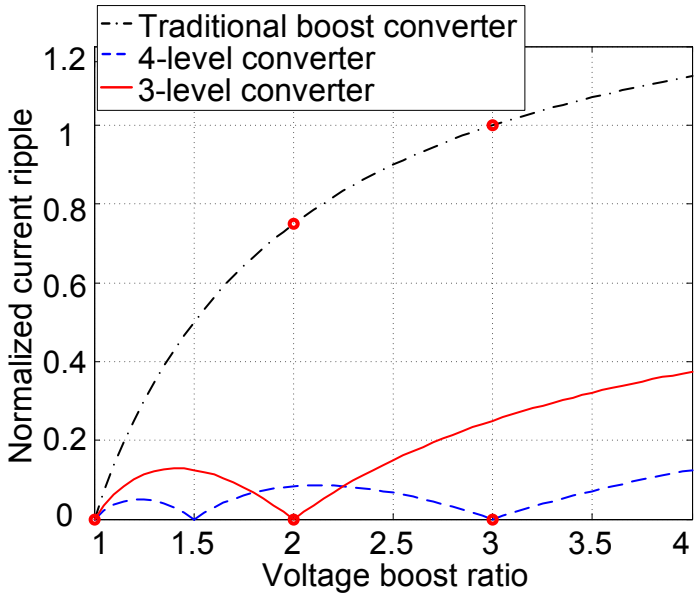


Figure 2.7. Comparison of normalized current ripples.

One concern about the four-level converter is that six semiconductor switching devices have to be used instead of two in the traditional two-level boost converter. The total switching device power rating (TDPR) or total device power stress (TDPS) of a converter circuit is an indication of how much the total silicon area is needed for the semiconductor devices. The following analysis shows that both two- and four-level converters have the same TDPR, thus requiring similar or the same amount of silicon areas. For the six switches in the four-level (4L) converter

operation, the TDPR is

$$TDPR\_4L = 6 \cdot (V_{out} / 3) \cdot I_{in} = 2 \cdot m \cdot P_o, \tag{2.5}$$

where $m = V_{out}/V_{in}$ and output power, $P_o = V_{in}\ I_{in} = V_{out}\ I_{out}$. For the two switches in the traditional two level bidirectional boost converter, the TDPR is

$$TDPR\_2L = 2 \cdot V_{out} \cdot I_{in} = 2 \cdot m \cdot P_o. \tag{2.6}$$

As can be seen from (2.5) and (2.6), they have the same total device power rating. For the traditional boost converter, each switch has to sustain the full dc voltage, whereas the switches in the four-level converter only sustain 1/3 of the dc voltage. For example, Camry hybrid uses the traditional dc-dc boost converter, in which each switch employs four IGBTs and four diodes in parallel to reach the current (400 A) and voltage (650 V) ratings [99]. However, if the four-level converter is used, each switch needs to sustain only 1/3 of the output voltage, thus much lower voltage and higher current IGBT can be used without the need for paralleling. A different way to look at the four-level converter is that it uses three IGBTs in series to reach the required power rating, instead of parallel in the traditional boost converter. Therefore, the four-level converter is an attractive candidate to replace the traditional boost converter for PHEVs. More interestingly, when the converter operates at three discrete voltage ratios: one, two and three times the input voltage (3X), as marked with dots in Figure 2.7, the inductor current in the four-level dc-dc converter becomes ripple free. This implies that the inductance requirement is zero. The question left to be answered is how to produce three discrete voltage ratios with smooth transition from one level to another. As mentioned previously, three discrete voltage levels are enough and have been used in many HEVs such as Camry for optimum operation of the power train.

2.3. Variable 3X DC-DC Converter and its Operation Principle

Figure 2.8 shows the proposed variable 3X dc-dc converter, in which no magnetic inductor is needed on the input side for three discrete voltage output levels: 1X, 2X, and 3X the input voltage. In the figure, L_S represents stray inductance of the circuit, which can be the equivalent series inductance (ESL) within the battery pack and the parasitic inductance of the cable connecting the converter to the battery in the PHEV. A fixed ratio of 1:3 was presented in [93, 94] to interface the 14/42 V accessory power supplies in vehicles. However, this fixed voltage ratio is not suited for HEV and PHEV applications, in which a variable dc voltage is needed. In this paper, we further explore the possible operation of variable voltage ratios and their smooth transitions. Compared with other switched-capacitor dc-dc converters [100-111], the following proposed variable 3X dc-dc converter has the simplest structure and finds its niche in the PHEV application where only discrete voltage ratios are desired from the battery to the traction drive dc bus voltage.

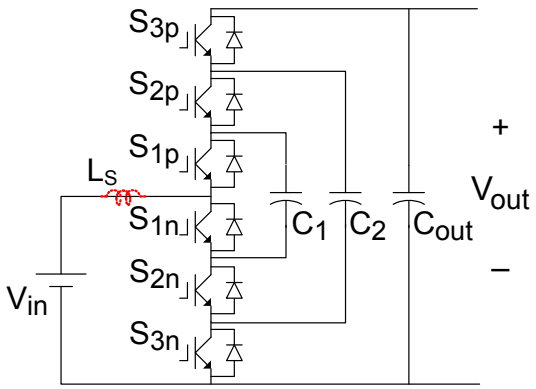


Figure 2.8. 3X dc-dc converter.

Because of its bi-directional nature, the 3X dc-dc converter can be viewed as a multiplier (step up) or a divider (step down) depending on power flow direction. The switching states as shown in Figure 2.9, Figure 2.10 and Figure 2.11 represent the boost mode operation for the

three voltage ratios, 1X, 2X, and 3X.

1X: To achieve the voltage ratio of 1, namely 1X, the converter operates in just one switching state as shown in Figure 2.9, with switches S_{2n} and S_{3n} always ON. Thus, all the capacitors are connected in parallel with the input voltage, which ensures the voltage ratio of 1X. Under this 1X operation, it is apparent that there is no voltage balancing problem.

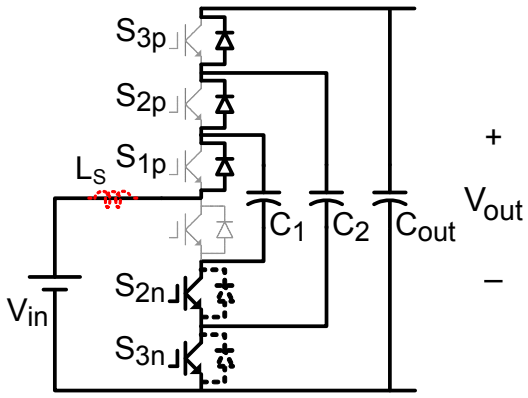
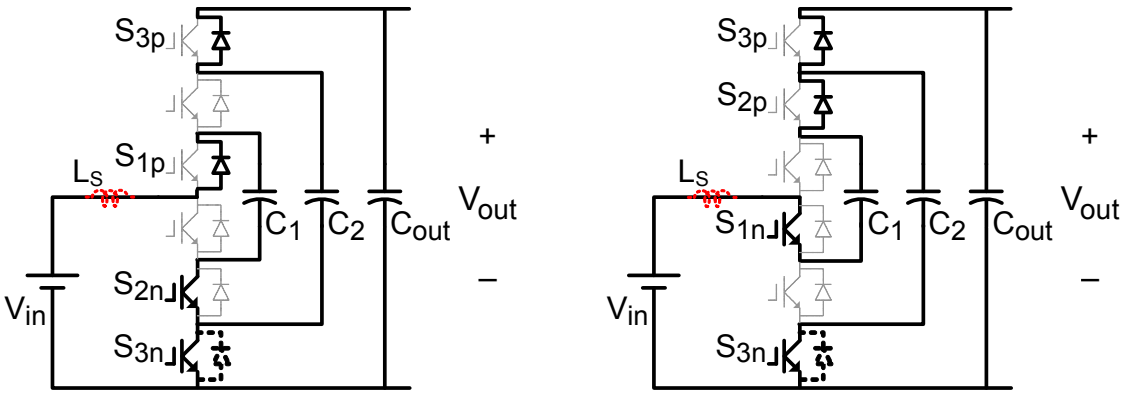


Figure 2.9. Switching state for 1X mode.

2X: While C_2 and C_{out} are always paralleled by having S_{3n} continuously ON, the converter alternates with 50-50% duty cycle between two switching states I and II as illustrated in Figure 2.10 (a) and (b). In the switching state I with S_{2n} ON, the capacitor C_1 is paralleled with the input battery and charged to the battery voltage, and in the switching state II with S_{1n} ON, C_1 is connected in series with the battery and discharged to the parallel of C_2 and C_{out}. As a result, the voltage of the capacitor C_1 is maintained close to the battery voltage and the output voltage becomes 2X input battery voltage. The capacitor voltages should be well clamped and balanced. Note that the anti-parallel diode (in bold dashed line) of S_{3n} may conduct when the discharge current of C_2 is greater than the input current charging C_1.



(a) Switching state I. (b) Switching state II.

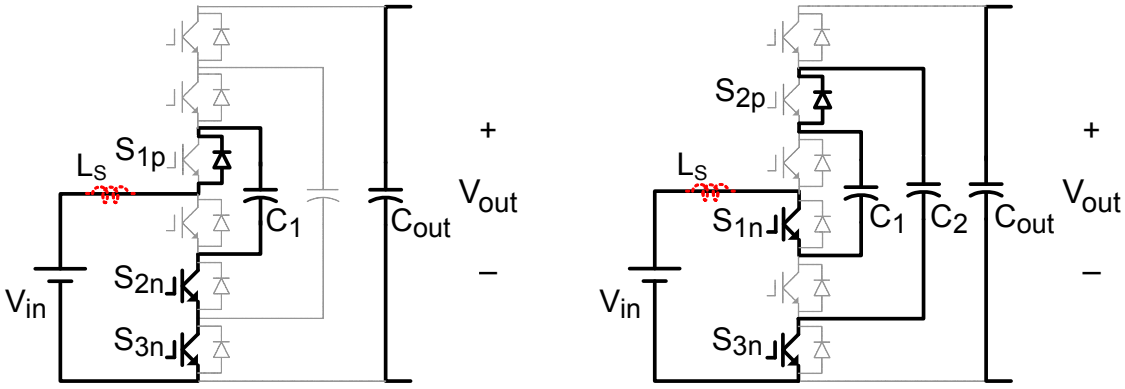
Figure 2.10. Switching states for 2X mode.

3X: When the desired ratio is 3X, the converter circulates among switching states I, II and III as shown in Figure 2.11 (a), (b) and (c), with 1/3 duty cycle each state. In state I, $V_{C1} = V_{in}$; in state II, $V_{C2} = V_{C1} + V_{in}$; in state III, $V_{out} = V_{C2} + V_{in}$. After these three states, the capacitor voltages will all be balanced automatically, as demonstrated in [93, 94]. The output voltage is three times (3X) the input voltage.

2.4. Transient Current Control during Voltage Transitions

In steady state, the capacitor voltages are well balanced and the voltage differences are very small, so the current through the switches is well limited as demonstrated in [93]. Theoretically, the 3X dc-dc converter does not need any input inductance in steady-state operation for any of the three output voltage levels. However, during a transition when the output voltage changes between V_{in} and $2V_{in}$, or between $2V_{in}$ and $3V_{in}$, the voltage differences are very large, which can lead to high transient current through the devices and capacitors. In order to limit this transient current, a variable duty-ratio PWM with a higher switching frequency is proposed for

the transitions. In addition, a minimum inductance indicated as L_s in Figure 2.8 is required for limiting the transient current, which will be discussed later.



(a) Switching state I.

(b) Switching state II.

(c) Switching state III.

Figure 2.11. Switching states for 3X mode.

A. Changing the output voltage from $1V_{in}$ to $2V_{in}$

Before changing the output voltage from $1V_{in}$ to $2V_{in}$, all three capacitors are initially charged to $1V_{in}$ in 1X mode. In the transition, C_2 and C_{out} should be charged up to $2V_{in}$ gradually. To simplify analysis, assume that the stray inductance is large enough for the inductor

current to be continuous. (The transient input current does not have to be continuous, in principle). Therefore, the transient operation can be referred to the same sequence of Figure 2.6(a)-(c)-(b)-(c) for the voltage ratio of $1 \le V_{out}/V_{in} \le 2$. The corresponding PWM signal in any switching cycle can be referred to Figure 2.5(a), except that the duty cycle, D has to be increased gradually over the transition to limit inrush current. The duty cycle is again defined in Figure 2.5(a) for S_{1n} and S_{2n}. As a result, the transition is divided into two active switching states and one freewheeling state between them. In the two active switching states, the switching signals are given to the switches as shown in Figure 2.6(a) and (b). The resultant leg voltage, v_m, equals V_{C1} in Figure 2.6(a), and it equals $V_{out} - V_{C1}$ in Figure 2.6(b) for the duration of DT, respectively. After each active state, the switches S_{1n} and S_{2n} are turned OFF. Therefore, the input current flows through the anti-parallel diodes in S_{1p} and S_{2p} as shown in Figure 2.6(c). The resultant leg voltage, v_m, equals V_{out} for the duration of $(1/2–D)T$. According to the inductor voltage-second balance in steady state, the relationship of the input voltage and output voltage still satisfies (1) as follows:

$$V_{in} = DV_{c1} + D\left(V_{out} - V_{c1}\right) + 2\left(\frac{1}{2} - D\right)V_{out} = \left(1 - D\right)V_{out}. \tag{2.7}$$

From the steady-state boundary condition of 1X and 2X modes, the duty cycle should vary from 0 to 1/2 to change the output smoothly to $2V_{in}$. As illustrated in Fig. 12, the PWM duty cycle of the active switches S_{1n} and S_{2n} have to increase gradually from 0 to 1/2, with a higher transient switching frequency.

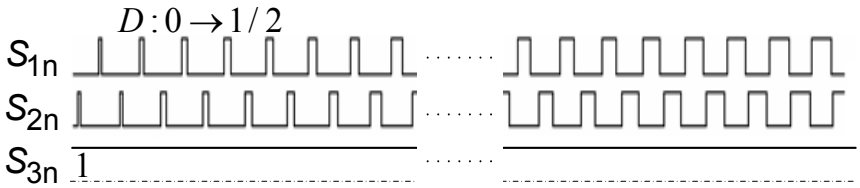


Figure 2.12. PWM signals of the active switches during the 1X to 2X transition showing gradual duty cycle increase from 0 to 1/2.

B. Changing the output voltage from $2V_{in}$ to $3V_{in}$

Applying the same principle to the transition from $2V_{in}$ to $3V_{in}$, the switching states can be referred to the sequence of Figure 2.4(e)-(a)-(f)-(b)-(g)-(c). The corresponding PWM signals and their time interval are marked in Figure 2.3(b) over one switching cycle. Likewise, by averaging the leg voltage, v_m, the same voltage relation can be derived as (1). For example, when S_{2n} and S_{3n} are turned on as shown in Figure 2.4(e), the leg voltage, v_m equals V_{C1}. After the duration of $(D–1/3)T$, S_{2n} is turned off as in Figure 2.4(a), the freewheeling current forces v_m to equal V_{C2} for the duration of $(2/3–D)T$ until the next switching state (Figure 2.4(f)) starts. Likewise, when the converter stays in Figure 2.4(f) and (g), v_m is equal to $V_{C2} - V_{C1}$ and $V_{out} - V_{C2}$ for $(D–1/3)T$, respectively. In their corresponding freewheeling states, v_m is equal to $V_{out} - V_{C1}$ in Figure 2.4(b) and equal to $V_{out} - V_{C2} + V_{C1}$ in Figure 2.4(c) for $(2/3–D)T$, respectively. Likewise, by averaging the leg voltage, v_m, the same voltage relation can be derived as (2.1).The ideal duty cycle for the active switches varies gradually from 1/2 to 2/3 during this transition, as illustrated in Figure 2.13.

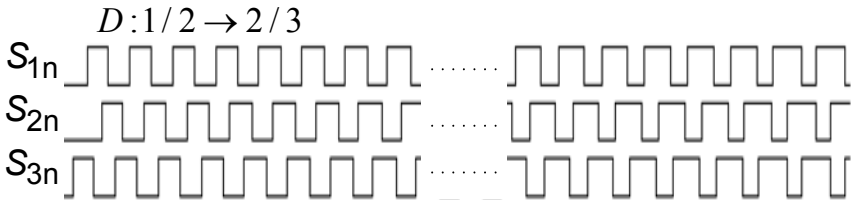


Figure 2.13. PWM signals of the active switches during 2X to 3X transition showing gradual increase of duty cycle from 1/2 to 2/3.

C. Changing the output voltage from $3V_{in}$ to $2V_{in}$

The control strategy for the transition from $3V_{in}$ to $2V_{in}$ is to reduce the initial three switching states (Figure 2.11(a), (b), and (c)) of the 3X operation to the first two switching states (Figure 2.11(a) and (b)) and to control the two switching states with 50-50% duty cycle. The output capacitor C_{out} is disconnected from the source and will be gradually discharged by the load. When the output voltage decreases to the voltage of C_2, the anti-parallel diode of S_{3p} conducts and clamps the output voltage to $2V_{in}$. The PWM signals for this transition are shown in Figure 2.14.

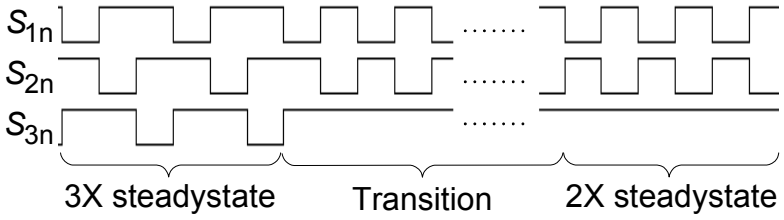


Figure 2.14. PWM signals of the active switches in the 3X to 2X transition.

D. Changing the output voltage from $2V_{in}$ to $1V_{in}$

In a similar manner, a transition from 2X to 1X can be implemented by the gate signals illustrated in Figure 2.15 to keep S_{2n} and S_{3n} ON. When the three capacitor voltages decrease

and become equal, the converter settles down to the 1X mode steady-state operation as shown in Figure 2.9.

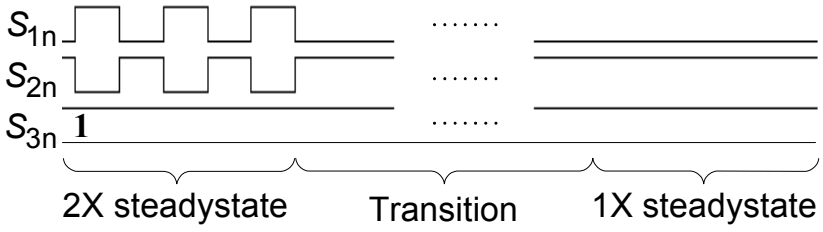


Figure 2.15. PWM signals of the active switches in the 2X to 1X transition.

2.5. Minimum Requirement of Parasitic Inductance

In this section, an analysis is made to determine how much parasitic inductance is needed to limit the transition current within the rated input current. The voltages across C_1 and C_2 are assumed constant in each short switching period, T_{tr}. Based on the above transient PWM control methods, the two worst cases for high transient currents are considered among all the transition modes.

A. V_{out}: $1V_{in} \rightarrow 2V_{in}$

During this transition, the input current change (ripple) can be calculated according to the active switching state II, illustrated in Figure 2.6(b):

$$\begin{aligned} \Delta i &= \frac{V_{Ls} \times DT_{tr}}{L_s} \\ &= \frac{\left(V_{in} + V_{c1} - V_{out}\right) DT_{tr}}{L_s} \\ &= \frac{V_{in}\left(1-2D\right) DT_{tr}}{L_s\left(1-D\right)} \\ &\le \Delta I_{\max} \end{aligned} \tag{2.8}$$

where $V_{c1} = V_{in}, V_{out} = V_{in}/(1-D)$ for $0 \le D \le 1/2$, and $\Delta I_{\max}$ is a given maximum current value allowed.

The maximum Δi occurs at $D = 0.29$ in the above function, which should be limited to no larger than the specified maximum current allowed, $\Delta I_{\max}$.

B. V_{out}: $2V_{in} \rightarrow 3V_{in}$

Similarly, the current change in the 2X to 3X transition is computed according to the active switching state III in Figure 2.4(g):

$$\begin{aligned} \Delta i &= \frac{(V_{in} + V_{c2} - V_{out}) D T_{tr}}{L_s} \\ &= \frac{V_{in}(2-3D)(D-1/3) T_{tr}}{L_s (1-D)} \\ &\le \Delta I_{\max} \end{aligned} \tag{2.9}$$

where $V_{c2} = 2V_{in}$, $V_{out} = V_{in}/(1-D)$ for $1/2 \le D \le 2/3$.

The maximum Δi occurs at $D = 0.53$ in the above function.

In comparison of the maximum current changes in both cases, the minimum inductance requirement can be calculated as 4.1 μH for a 480-A allowable current change, assuming that the 55-kW 3X dc-dc converter is switched at 20-kHz transient switching frequency and 230-V input voltage. The requirement of the parasitic inductance can be further reduced by increasing the switching frequency during transitions. In practice, a further lower parasitic inductance than the above conservative calculated value is tolerable, because the capacitance of C_1 and C_2 is finite and the voltages are not constant, which further reduces transient inrush current. In practice, the total ESL of a battery pack and connection cable should be sufficient, especially when the battery is placed in the trunk area far away from the converter under hood in most HEVs and PHEVs.

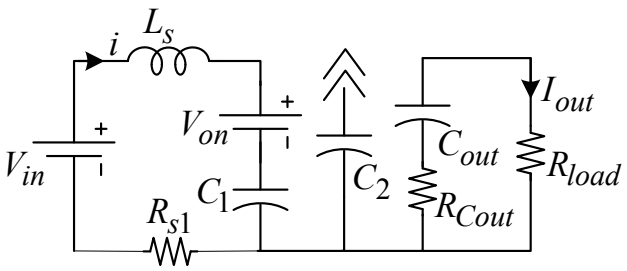
Otherwise, a small air-core inductor can be added when the parasitic inductance is not enough.

2.6. Power Loss Analysis

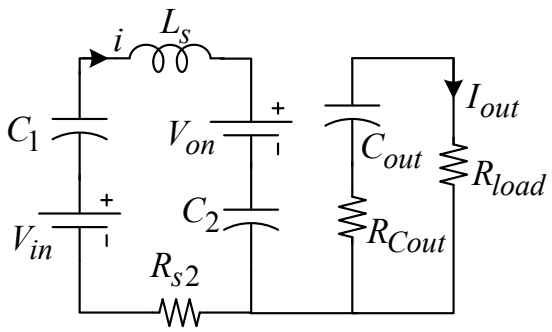
Power loss analysis is usually estimated for assessing the converter parameters. It can be calculated numerically based on the current in the charge/discharge loop. Thus, the following analysis starts with modeling the input current. Each *n*X steady-state operation can be modeled with its equivalent circuit. Take the 3X mode for instance. The equivalent circuits are illustrated in Figure 2.16. There is a lumped constant voltage drop V_{on} resulting from two IGBTs and one diode in the serial loop. The voltage drop of one IGBT is modeled as a constant voltage plus a current times its equivalent series resistance (ESR). In the first state of $t = 0 \sim \frac{T_S}{3}$, C_1 is charged by the battery, as modeled in Figure 2.16(a). The input current can be solved as:

$$i = e^{-\alpha_1 t}\left[I(0)\cos\omega_1 t + \left(C_1 \Delta V_1 \frac{{\alpha_1}^2 + {\omega_1}^2}{\omega_1} - \frac{\alpha_1 I(0)}{\omega_1} \right)\sin\omega_1 t \right] \tag{2.10}$$

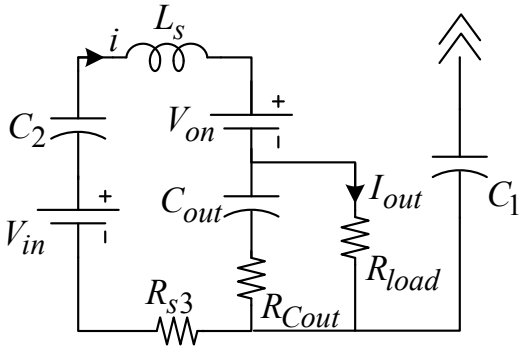
where $I(0)$ is the initial input current through the ESL in the charging loop, and $\Delta V_1 = V_{in} - V_{on} - V_{C1}(0)$ is the initial voltage difference. $\alpha_i = R_{si}/(2L_s)$ in each state; $i = 1, 2, 3$ implies three states; the resonance frequency in each switching state can be explicitly found by the equivalent loop capacitance and ESL: $\omega_i = \sqrt{\frac{1}{L_s C_{loopi}} - (\frac{R_{si}}{2L_s})^2}$. In State I, $C_{loop1} = C_1$.



(a) Switching state I.



(b) Switching state II.



(c) Switching state III.

Figure 2.16. Equivalent circuit for the 3X mode.

In the same way, for the second state of $t = \frac{T_s}{3} \sim \frac{2T_s}{3}$ as modeled in Figure 2.16 (b), the input current is expressed as

$$i = e^{-\alpha_2 (t-\frac{T_s}{3})} \left[I(\frac{T_s}{3}) \times \cos \omega_2 (t-\frac{T_s}{3}) + \left(C_{loop2} \Delta V_2 \frac{{\alpha_2}^2 + {\omega_2}^2}{\omega_2} - \frac{\alpha_2 \times I(\frac{T_s}{3})}{\omega_2} \right) \sin \omega_2 (t-\frac{T_s}{3}) \right] \quad (2.11)$$

where $\Delta V_2 = (V_{in} - V_{on}) + V_{C1}(\frac{T_s}{3}) - V_{C2}(\frac{T_s}{3})$, $C_{loop2} = \frac{C_1 \times C_2}{C_1 + C_2}$.

For $t = \frac{2T_s}{3} \sim T_s$, the output capacitor gets charged as modeled in Figure 2.16(c). The load

current, I_{out} can be approximated as a constant dc, considering the very small output voltage ripple. The input current can be expressed as a function of both initial input current and load current.

$$i = e^{-\alpha_3(t-\frac{2T_s}{3})}\left\{\left[I(\frac{2T_s}{3}) - \frac{C_2 I_{out}}{C_2 + C_{out}}\right]\cos\omega_3(t-\frac{2T_s}{3}) + \left[C_{loop3}(\Delta V_3 - K)(\alpha_3{}^2 + \omega_3{}^2) - \alpha_3\left(I(\frac{2T_s}{3}) - \frac{C_2 I_{out}}{C_2 + C_{out}}\right)\right]\cdot\frac{1}{\omega_3}\sin\omega_3(t-\frac{2T_s}{3})\right\} + \frac{C_2}{C_{out}+C_2} I_{out} \tag{2.12}$$

where $\Delta V_3 = (V_{in} - V_{on}) + V_{C2}(\frac{2T_s}{3}) - V_{Cout}(\frac{2T_s}{3})$, the constant $K = R_{s3} I_{out}\frac{C_2}{C_{out}+C_2}$, the loop capacitance $C_{loop3} = \frac{C_{out}\times C_2}{C_{out}+C_2}$.

By equalizing the initial value of the current in the first state and the final value in the third state, the initial current $I(0)$ and the current expression can be solved. For a simplified iteration, the voltage difference in every state can be approximated from half of the capacitor voltage ripples.

The total power loss includes conduction loss, switching loss, and gate drive loss. The conduction loss here refers to the loss dissipated in the semiconductor devices and in the ESR in the passive components. The latter is sometimes separated as the charge/discharge loss, although it is essentially consumed by the loop ESR. It is discussed in [94] that the charging loss is not relevant to the ESR when the switching period and the RC time constant satisfy $Ts \gg RC$ and the stray inductance is negligible. However, it is not true when the stray inductance is not negligible. The conduction loss can be summed up for every 1/3 switching cycle:

$$P_{con} = \left(\sum_{j=1}^{3} \frac{V_{on} \cdot I_{avg,j} + I_{RMS,j}^2 \cdot R_{sj}}{3} \right) + \frac{\left(3I_{out}^2 + I_{RMS,3}^2 - 2I_{avg,3} \cdot I_{out} \right) R_{Cout}}{3} \tag{2.13}$$

where $I_{avg,j}$ and $I_{RMS,j}$ are the average and RMS values of the input current respectively.

At the end of each switching state, two IGBTs and one diode are turned on/off. The IGBT switching loss is directly proportional to the switching current, given a fixed converter input voltage. The diode reverse recovery current can be expressed as a function of its snap-off current from the datasheet. Therefore, the switching loss is computed as the integration of the corresponding voltage and current:

$$P_{sw} = V_{ce\_pk} \cdot f_s \sum_{j=1}^{3} \left[\frac{1}{6} I\left(\frac{jTs}{3}\right) \cdot \left(t_{on} + t_{off} \right) + \frac{1}{2} I_{rr,j} \cdot t_{rr,j} \right] \tag{2.14}$$

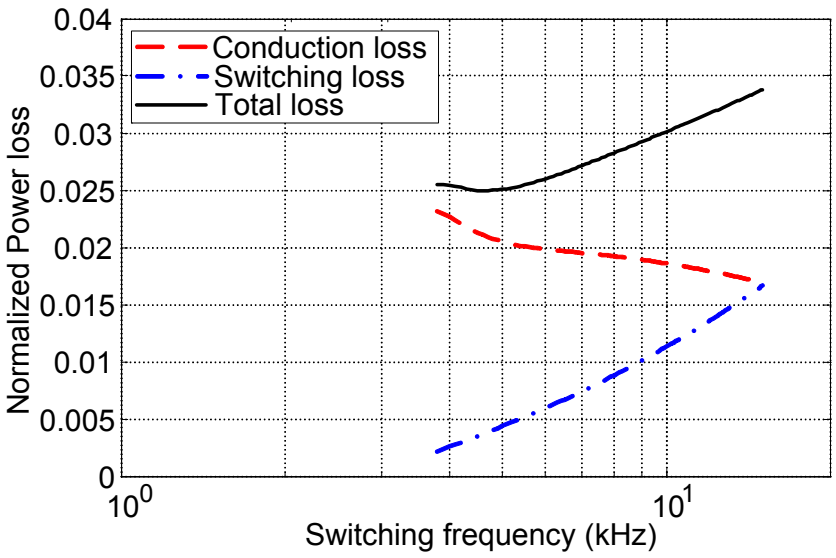


Figure 2.17. Power loss vs. switching frequency in 3X mode.

As one of the guidelines for selecting the switching frequency, the estimated power loss is normalized and plotted in Figure 2.17 according to (2.13) and (2.14). The circuit parameters are the same as in the next section. The total loss also includes gate drive loss. The base value is 30-

kW continuous power at 220-V input voltage. As can be seen, the conduction loss is dominant when the switching frequency is low. As the switching frequency keeps rising, the switching loss becomes dominant. In terms of the overall efficiency, the optimum switching frequency falls in the range of 4~6 kHz. At the same time, the input current ripple to the battery is another factor to be taken into account for determining the switching frequency within the desirable efficiency range.

2.7. Experimental Results of a 55-kW 3X DC-DC Converter

A 55-kW prototype as shown in Figure 2.18 was built to verify the functionality of the 3X dc-dc converter concept. The switching devices are commercially available 600-V IGBT/IPM modules, which is higher than what is required for the 3X dc-dc converter with 230-V input voltage. In fact, the efficiency of the converter would be higher if a lower (around 400 V) voltage rating module were available. The capacitors for C_1 and C_2 are 500 μF and 240 μF film capacitors, respectively. The output capacitor consists of 40-μF film capacitors in the 3X dc-dc converter and 820-μF capacitors at the inverter dc bus. In addition, a 10-kΩ bleeding resistor is paralleled across each IGBT. Besides draining the energy out of the capacitor at power-off, it helps balance the voltage across each IGBT under some particular conditions, for instance, the initial power-on stage. The duty cycle and frequency control is implemented by one CPLD XC95288XL, which can be readily integrated with the control board for the entire power converter system.

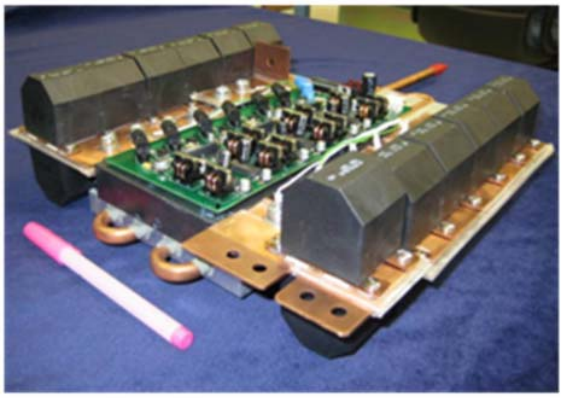
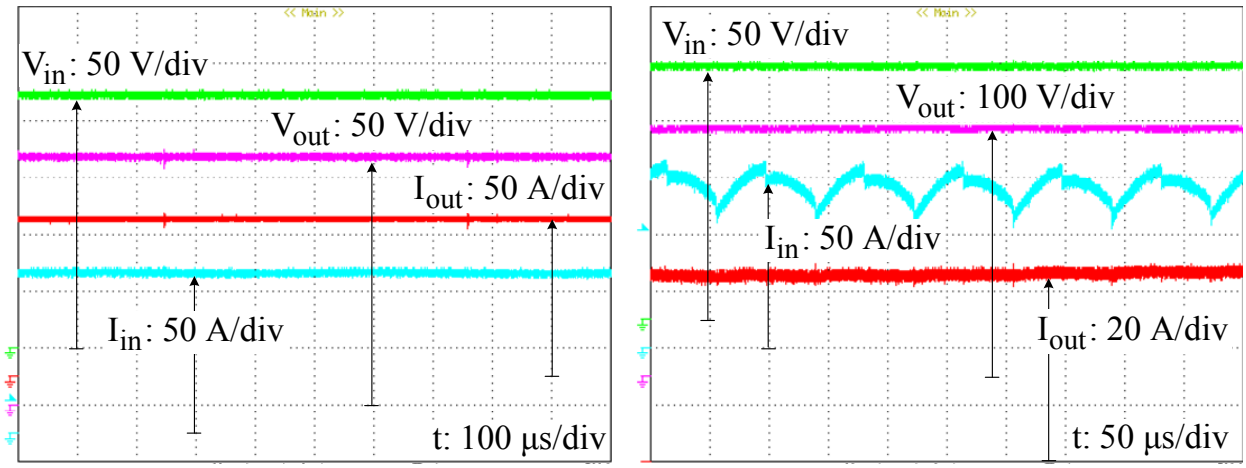


Figure 2.18. 55-kW dc-dc multiplier/divider prototype.

Experimental results in the steady-state and transient operation are shown in Figure 2.19 and Figure 2.20. A total 5-μH ESL in the battery and cable was estimated. The converter operates at 8 kHz in the 3X mode and 12 kHz in the 2X mode. Figure 2.19(a) and (b) show the input/output voltage and current waveforms in 1X and 2X modes at their 30-kW peak power. Figure 2.19(c) shows the waveforms in 3X mode at the 55-kW peak power. Figure 2.20 shows voltage transition waveforms, in which the converter operates at 20 kHz. As can be seen, the transient current was successfully limited below 240 A, the rated current of the converter. Figure 2.21 shows the measured efficiency at different output powers in nX mode (n=1, 2, 3). The overall efficiency in the 30-kW continuous power range is over 97%. Figure 2.22 gives an estimation of the power loss breakdown in the full power range of the 3X mode, with a comparison to the experimental results. The analysis well predicts the characteristics of the loss with respect to the output power.

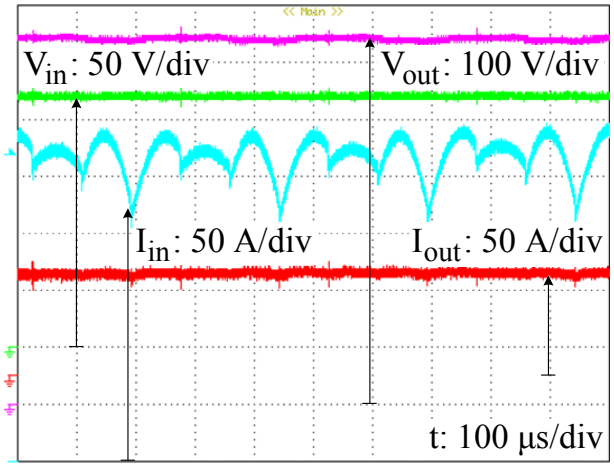
Compared to the design of the fixed 3X 1-kW converter in [93], the utilization of parasitic inductance in the proposed variable 3X converter reduces pulse current, the conduction loss, and the capacitance requirement. As a result, a compact size (27.2 cm × 24.4 cm ×8.8 cm) and light weight (5.6 kg) were achieved. Furthermore, the power density of the proposed converter is

considerably increased, compared to the power density (30 kW / 3483.55 cm^3 and 30 kW / 6.6 kg) of the dc-dc converter in a commercially mass-production vehicle [99]. The 3.5-kg 212-µH inductor alone contributes significantly to the volume and weight of the traditional boost converter. There is still great potential to make the converter even lighter by replacing the film capacitors with multilayer ceramic capacitors (MLCCs).



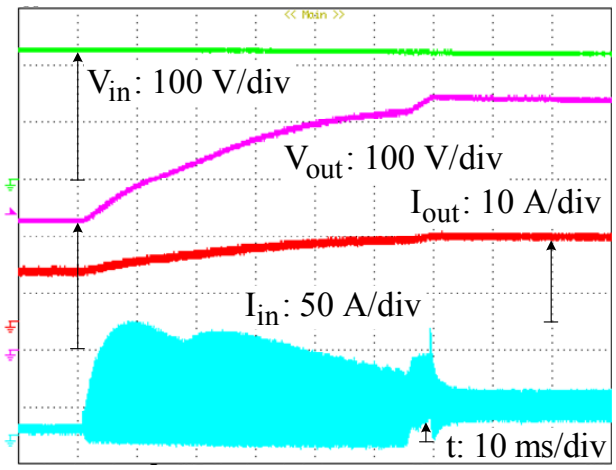
(a) 1X boost mode at 30-kW output.

(b) 2X boost mode at 30-kW output.

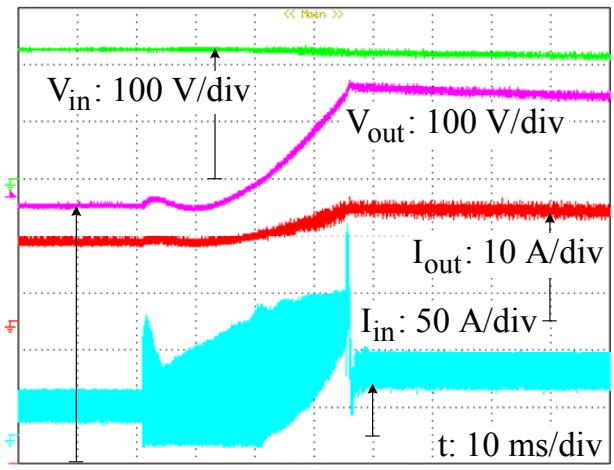


(c) 3X boost mode at 55-kW output.

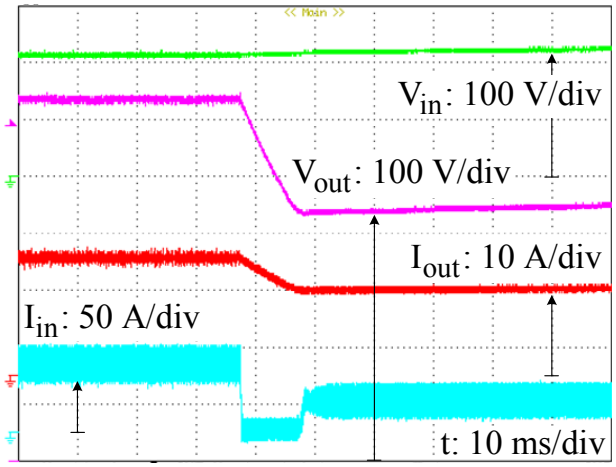
Figure 2.19. Experimental waveforms in the steady-state operation.



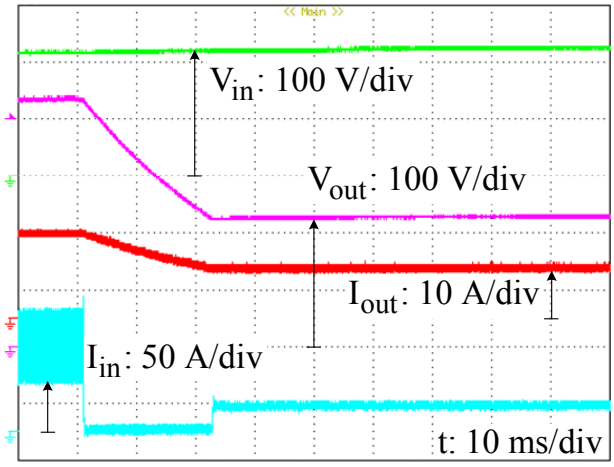
(a) Transition from 1X to 2X



(b) Transition from 2X to 3X



(c) Transition from 3X to 2X



(d) Transition from 2X to 1X.

Figure 2.20. Experimental waveforms of the *n*X mode transition.

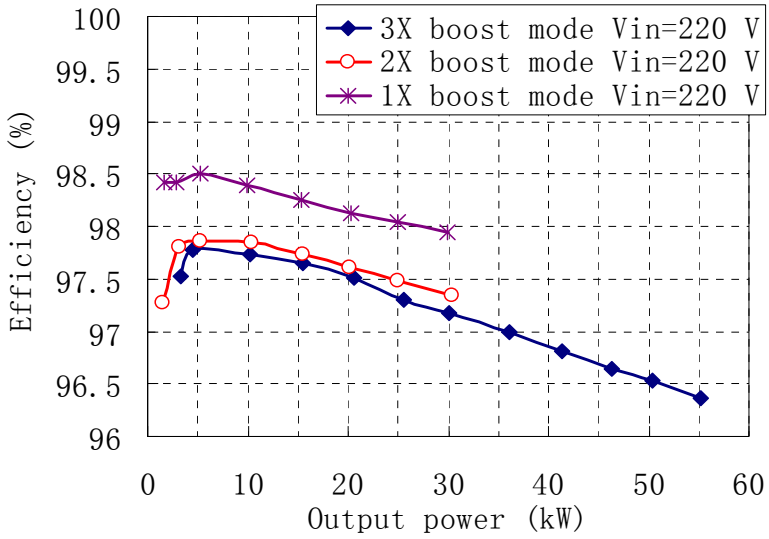


Figure 2.21. Measured efficiency of the 55-kW prototype.

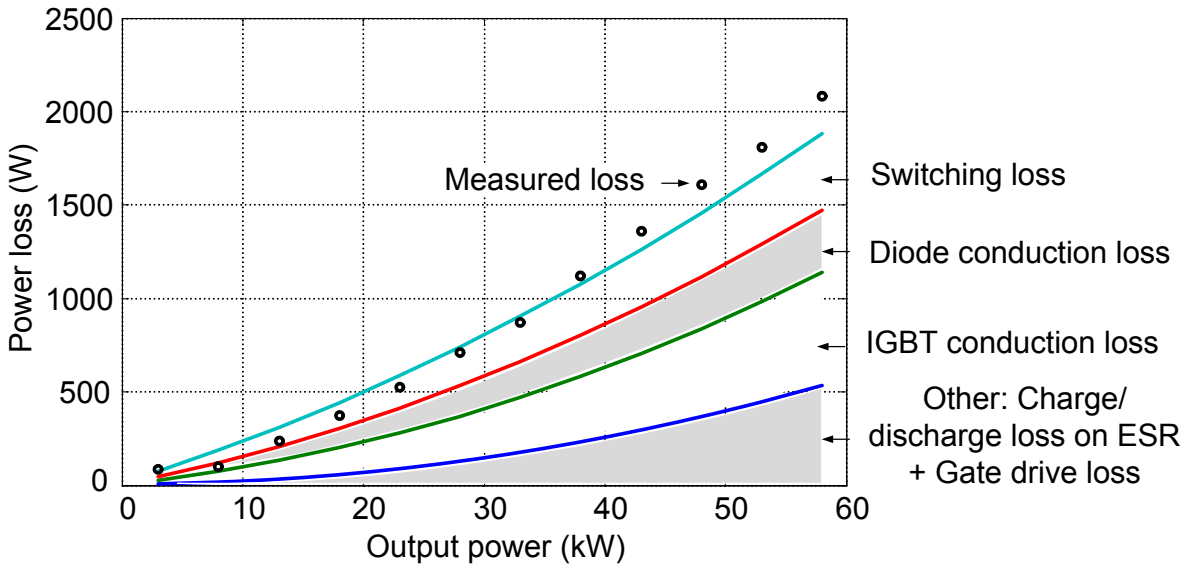


Figure 2.22. Power loss breakdown of the 55-kW prototype in 3X mode.

2.8. Auxiliary Clamping Circuit

2.8.1. Operating Principle

For the power rating of over tens of kilowatt, one of the challenges for the multi-level dc-dc

converters in high power application is the high frequency spikes during the diode reverse recovery. The voltage spikes add significant stress and additional losses to the device, and also bring in EMI problems to the system. In these converters, each pair of complementary switching devices is naturally capacitor-clamped, and thus the IGBT switching spike is ideally well clamped. However, in practice, the capacitor-clamped loop contains considerable ESL, due to the constraint of the package of commercial IGBT modules and the entire main circuit layout. Hence, the clamping effect to the high frequency voltage spikes could not be sufficient in some real-world designs. Therefore, a RCD clamping circuit as shown in Figure 2.23 is proposed for this multilevel dc-dc topology.

The basic operating principle is similar to that of the traditional RCD clamping circuit. When the switch is turned off, the current will be first diverted into the clamping capacitor through the clamping diode. Then the clamping capacitor regenerates the energy back to the main capacitor through a resistor. Such an example can be found in the energy regeneration loop for the clamping capacitors C_{1p} and C_{1n}. The clamping mechanism for all the switches is the same, but the discharge loops for other clamping cells are different, which innovatively make use of the switching devices in the main circuit to create the discharge loop. For instance, when the freewheeling diode in the switch S_{2n} turns off, the stray energy from the diode reverse recovery will flow into the clamping capacitor C_{2n}. When the switch S_{2n} is on, as shown in Figure 2.24(a), the stored energy will be fed back to C_1 through resistor R_{2n} and diode D_{d2n}. Such diodes in the discharge loop as D_{d2n} are added to guarantee the unidirectional current. That is, the voltage ripples of the main capacitors C_1, C_2 and C_{out} cannot make the clamping capacitors

get charged backward. The reason of having resistors in the discharge loop is to limit the current and to maintain a reasonable clamping voltage. Nevertheless, power loss is still very low. In the same way, the clamping capacitor C_{3n} will get a chance to recover the energy back to C_1 when the switches S_{2n} and S_{3n} are both conducting, as shown in Figure 2.24(a). It is noteworthy that in the boost mode operation, the actual conducting devices are the upper three freewheeling diodes in S_{xp} and the lower three IGBTs in S_{xn} (x=1, 2, 3), and vice versa in the buck mode operation. Nevertheless, the discharge current can still pass through either the IGBT or its freewheeling diode as any of them is carrying the load current.

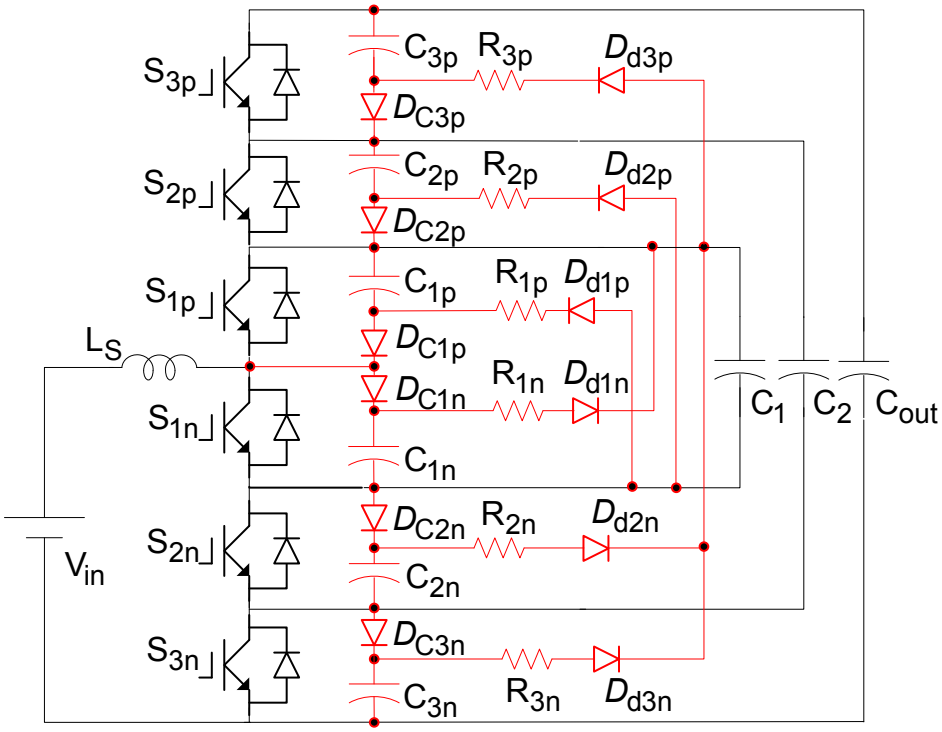
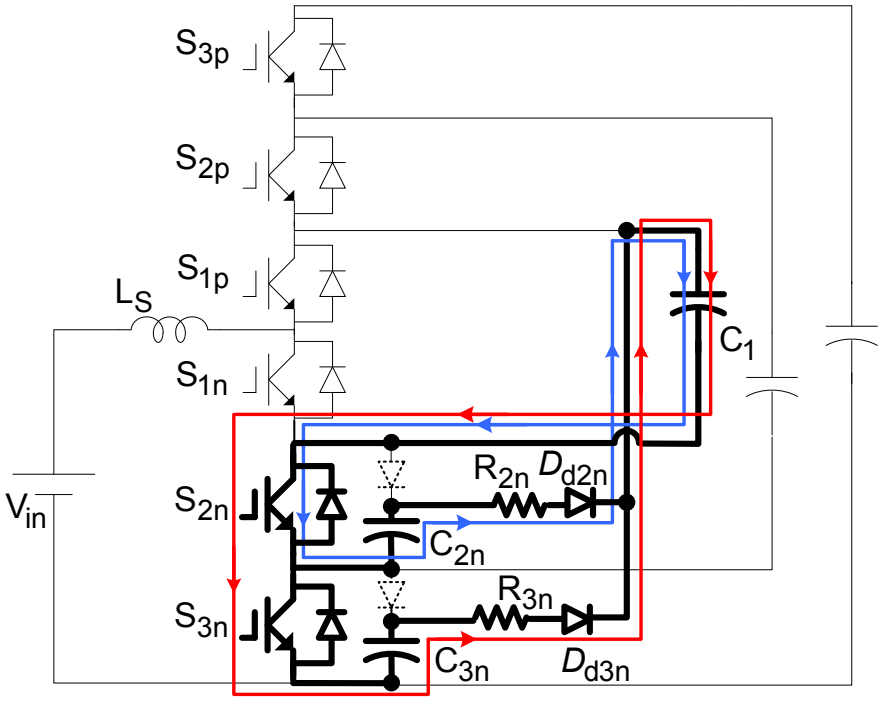


Figure 2.23. Clamping circuit

The discharge loop for the clamping capacitor C_{3p} behaves in the same fashion, but there are two discharging states for C_{3p} as shown in Figure 2.24(b) and (c). In the 1/3 switching period

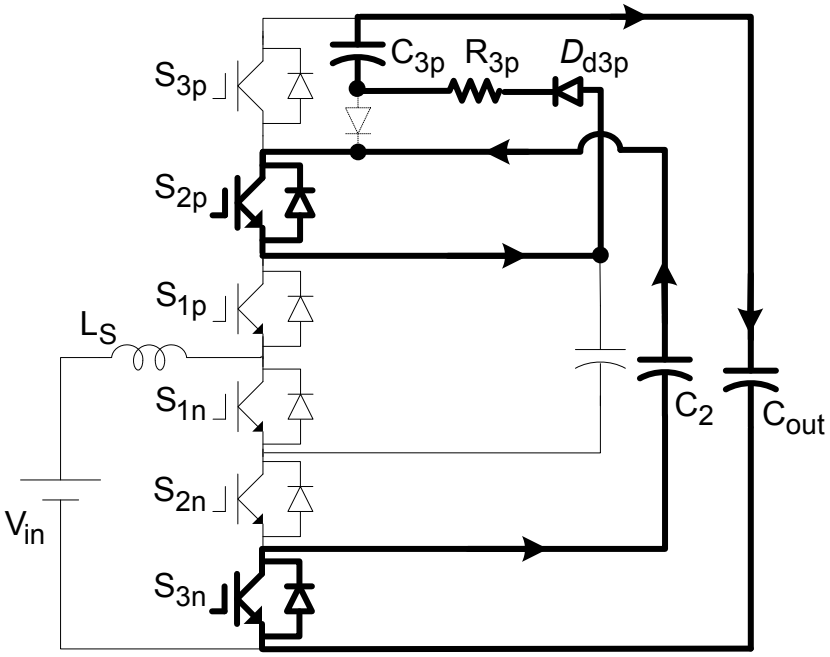
in Figure 2.24(b), when the switches S_{2p} and S_{3n} are on, the captured energy in C_{3p} will flow to C_{out} through C_2, R_{3p} and D_{d3p}. In another 1/3 period in Figure 2.24(c), the energy in C_{3p} will flow to C_2 through C_1, R_{3p} and D_{d3p}, when the switches S_{3p} and S_{2n} are on. Thus, the time constant of the discharge loop for C_{3p} can be designed twice the time constant of the other discharge loops, leading to less power loss.



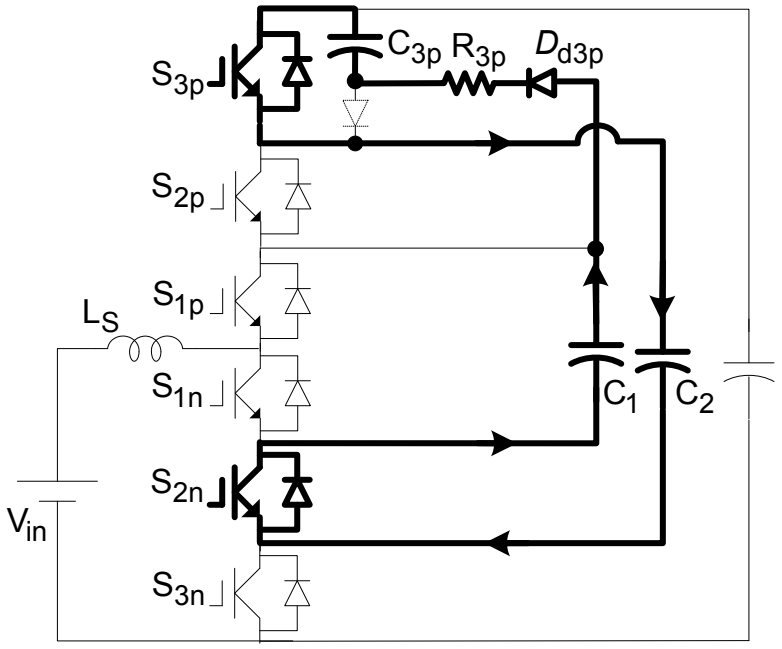
(a)The discharge loop for C_{2n} and C_{3n}.

Figure 2.24. Typical discharge loops.

Figure 2.24 (cont'd)



(b) The discharging state I for C_{3p}.



(c) The discharging state II for S_{3p}.

2.8.2. Experimental Results of the Clamping Circuit

The clamping circuit was designed for a 30-kW 3X dc-dc converter prototype. This converter was constructed by three 250-V 600-A CM600DU5F dual IGBT modules. The IGBT package imposes some layout restrict and difficulty. The capacitance for C_1 and C_2 are 500 μF and 160 μF. The capacitance at the output dc bus is 410 μF in total. The total input inductance is around 3.6 μH. The converter operated at 7 kHz. Without the clamping circuit, it could only handle the output power a little more than 10 kW. With the clamping circuit, the highest spike across switch is less than 15% at 30 kW in 3X boost mode, as shown in Figure 2.25. It demonstrates the effectiveness of the clamping circuit.

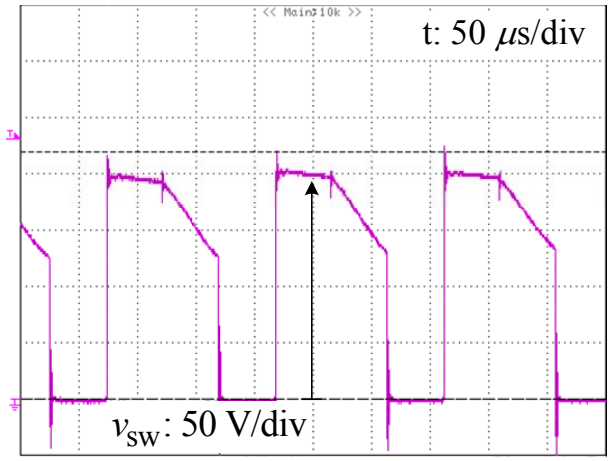


Figure 2.25. Experimental results of the voltage spike with the clamping circuit.

2.9. Summary

An alternative solution has been presented to overcome the demerits of the traditional boost converter for plug-in HEVs. Analysis has shown that a general four-level flying-capacitor dc-dc converter reduces the inductance requirement dramatically. Moreover, a variable 3X dc-dc converter has been proposed that was derived from the four-level dc-dc converter to further

minimize the inductance to null for HEVs and PHEVs that require three discrete voltage levels. The experimental results of a 55-kW prototype in steady-state and transient operation validated the operating principle and circuit analysis. Compared with the traditional low power switched capacitor dc-dc converters, the variable 3X converter achieves flexible voltage ratios without sacrificing efficiency (>97%) or the component count (only six switching devices and three capacitors) and with low voltage stress (V_{in}) across the switching devices. The transient current is well under control with the aid of the duty cycle control. By advantageously utilizing stray inductance, the variable 3X dc-dc converter achieves high efficiency with high power density. Therefore, it is a promising alternative to the existing boost converter for HEVs and PHEVs.

Chapter 3 A Switched-Capacitor DC-DC Converter with High Voltage Gain and Reduced Component Rating and Count

3.1. Introduction

When no input inductor is engaged, the 3X dc-dc converter in the previous chapter can essentially be categorized into the switched-capacitor dc-dc converters. Switched-capacitor dc-dc converters are a network of switching devices and capacitors. They are sometimes also called charge pump. Switched-capacitor dc-dc converters have gained popularity in industrial switched mode power supplies due to their attractive features such as magnetic-less structure and high efficiency. Since they can be easily integrated without bulky magnetic components, the power density of dc-dc converters can be significantly boosted. They can achieve high efficiency even at very light load condition, and can maintain good no-load output voltage regulation [100]. Therefore, many switched-capacitor dc-dc converters and the derived resonant switched-capacitor converters [102, 104, 107, 108, 112-120] have been developed. Yet, conventional circuits that are usually used in low power applications have some of the following drawbacks when a high voltage gain is desired: 1) quite diverse voltage/current stresses for switching devices in some circuits, which are not suitable for modular configuration or for high efficiency requirement; 2) a large number of switching devices in some other circuits; 3) pulsating input current and the resultant EMI; 4) unidirectional power flow. More importantly, their total device power ratings are unfavorable for a practical design to maintain high efficiency.

On the contrary to low-power switched-capacitor converters, the magnetic-less flying-

capacitor dc-dc converters have the advantages of small component (switching device and capacitor) count, low voltage stress across the switching devices, and bidirectional power flow. However, when it comes to high voltage conversion ratios in applications like PV generation, thermal electric generation, a pure magnetic-less flying-capacitor structure has its practical limits to reach high voltage gain. For an output/input voltage boost ratio of N times (namely NX), the input current has to go through N switching devices. An example is given in Figure 3.1, with a conversion ratio of four. The resultant voltage drop and power loss overshadow their advantages presented at the low voltage ratios.

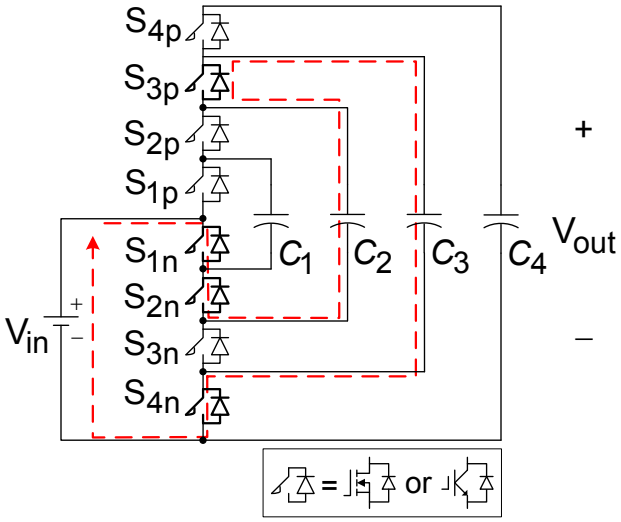


Figure 3.1. A flying-capacitor dc-dc converter with the voltage conversion ratio of four.

To address the above issues, a modular multilevel capacitor clamped dc-dc converter (MMCCC) was proposed in [121, 122]. A MMCCC is shown in Figure 3.2, with a voltage conversion ratio of four. Improved efficiency can be expected, because: 1) the current to charge a capacitor flows through at most three switching devices, regardless of the voltage ratio; 2) the currents through the switching devices and capacitors reduce to roughly 2/N times the corresponding currents in the original flying-capacitor structure for a voltage ratio of N, leading to the reduced total device power rating. However, the number of switching devices becomes

3N–2, rather than 2N for the conventional flying-capacitor structure, and the extra N–2 switching devices have to sustain the voltage stress of twice the input voltage (defined in boost mode). Additionally, as in many switched-capacitor dc-dc converters, while maintaining the device voltage (or current) stress low, it inevitably experiences the increased capacitor voltage with the increment of the voltage conversion ratio. The voltage diversity and the maximum voltage rating then affect the design, size and efficiency for a high voltage conversion ratio.

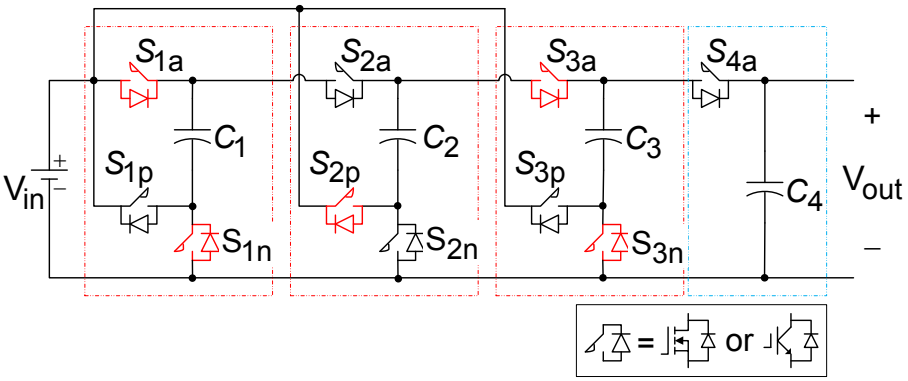


Figure 3.2. The original MMCCC with a voltage conversion ratio of four.

This paper presents a switched-capacitor dc-dc converter that is very suitable for high voltage gain applications. It sums up the output of two symmetric charge pumps to reduce the device count, capacitor voltage rating and power loss. Moreover, it keeps very low total device power rating (TDPR). As will be discussed later, its many merits lead to the possibility of a compact, light and high efficient converter. The following sections will start with a brief review on the structure of the MMCCC, such that the features of the proposed new converter could easily be brought to light. The operation principle and features of the proposed converter will be introduced afterward, followed by a quantitative comparison with other counterparts. The concept and analysis will be validated by simulation and experimental results.

3.2. A Brief Review of the MMCCC Structure

The MMCCC as shown in Figure 3.2 is composed of three basic cells, plus a switch S_{4a} and a capacitor C_4 connected to the output. In boost mode, it steps up the voltage from the low voltage input (defined as V_{in}) to the high voltage output (defined as V_{out}). From another point of view, the MMCCC can be reverted to the similar form as the flying-capacitor circuit and can be redrawn in Figure 3.3. The switch S_{ja} (j=1, 2, 3, 4) creates a path for charging the capacitor C_j in one of two alternate switching states. The capacitor C_1 is charged by the input, V_{in}, and the other capacitor C_j (j=2, 3) is charged via the addition of C_{j-1} and V_{in}. A phase leg of complementary switches S_{jp} and S_{jn} (j=1, 2, 3) from each basic cell is in parallel with the input source V_{in}, in order that C_j can be directly connected to the positive (or negative) terminal of the input through just one switch S_{jp} (or S_{jn}). By the same token, the switching states are reduced from four to two, since the current path becomes independent. This explains why the MMCCC has shorter current paths and lower current stress than the flying-capacitor circuit as shown in Figure 3.1 does.

3.3. The Proposed Switched-Capacitor DC-DC Converter and Operation Principle

Figure 3.4 shows the proposed switched-capacitor dc-dc converter with a voltage conversion ratio of six (named 6X). It can also function as a buck when the energy flows in the opposite direction. To explain the operating principle, its boost mode is taken as an example. The buck mode operation can be analyzed analogously. The charge pump splits into two symmetric

horizontal paths to build up the output voltage. In the upper path, the capacitor voltage is pumped up one by one to make the voltage of C_{3a} equal to $3V_{in}$; the lower path works in same manner, making the voltage of C_{3b} equal to $3V_{in}$.

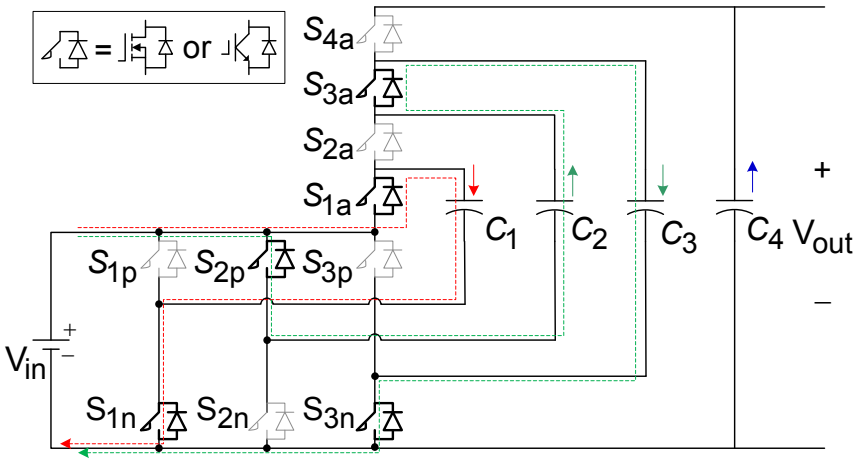


Figure 3.3. MMCCC in the similar form as the flying-capacitor circuit.

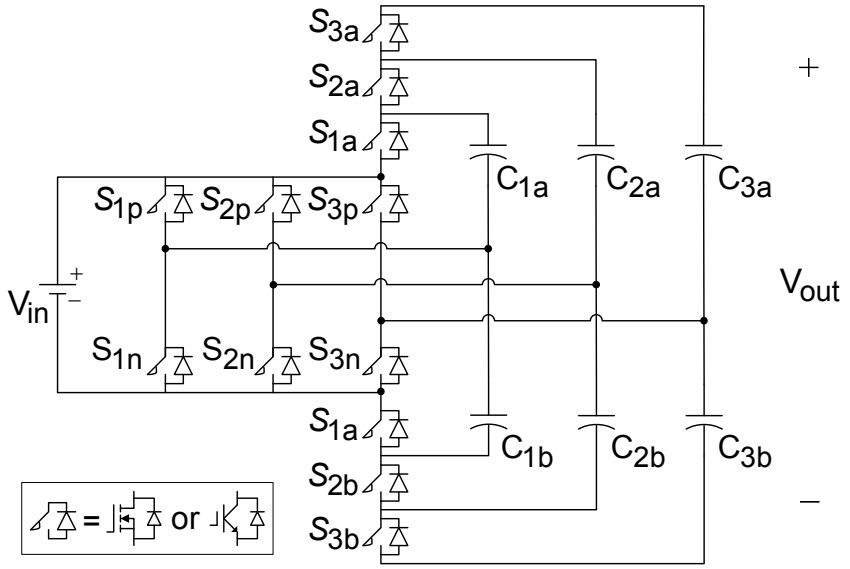
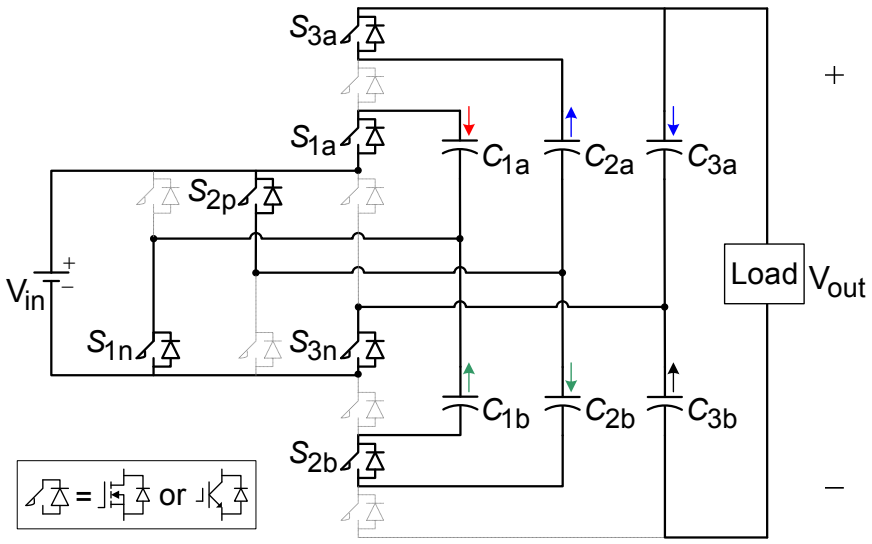


Figure 3.4. The proposed 6X switched-capacitor dc-dc converter.

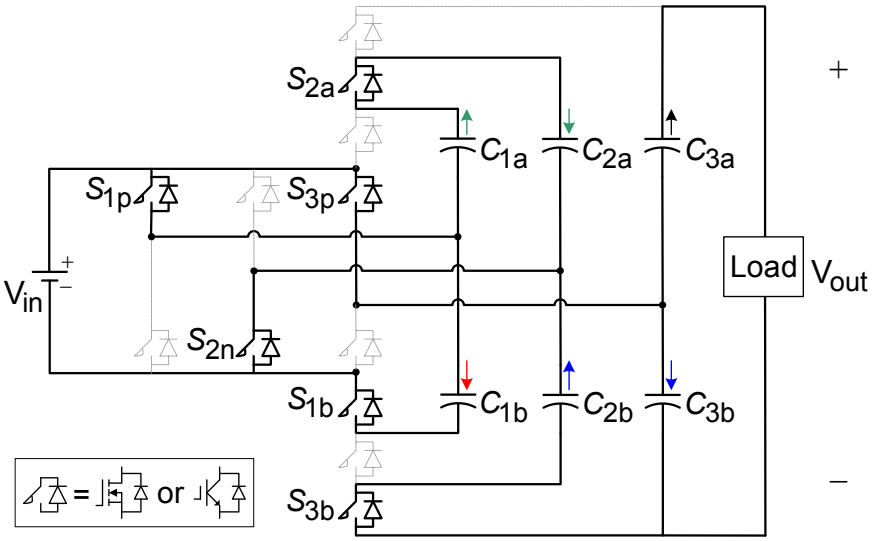
This converter alternates between two switching states as illustrated in Figure 3.5, with 50% duty ratio for each state as shown in Figure 3.6. The switching devices marked in solid line are

on-state devices and current paths; the remaining devices in dashed lines are off-state devices. Table 3.1 summarizes the switching states. The corresponding individual charge/discharge loops are shown in Figure 3.7. It is easy to infer that the switches S_{jp} and S_{jn} in the same phase leg are complementary; switches S_{ja} and S_{jb} are complementary as well (i.e., if one is on, the other should be off and vice versa. j=1, 2, 3). In the switching state I as shown in Figure 3.5(a), in the upper path, the capacitor C_{1a} is charged to V_{in} by the input through devices S_{1a} and $S_{1n,}$ as simplified in Figure 3.7(a); the capacitor C_{2a} is in series with the input to charge the capacitor C_{3a} through the switches S_{2p}, S_{3a} and S_{3n}, as simplified in Figure 3.7(b). In the lower path, the capacitor C_{1b} is in series with the input to charge the capacitor C_{2b} through the switches S_{1n}, S_{2p} and $S_{2b,}$ as simplified in Figure 3.7(c). C_{3b} is discharged by the load current. In the similar way, in the switching state II as shown in Figure 3.5(b), the complementary switches are gated on, so that the capacitors C_{2a}, C_{1b}, C_{3b} that are discharged in the first switching state become charged in the second switching state, while the capacitors C_{1a}, C_{3a}, C_{2b} become discharged. In particular, C_{3a} is discharged by the load current this time. Combining the voltage relations in the two switching states and neglecting the voltage drop, one can get the following voltage relations:

$$V_{Cja} = V_{Cjb} = j \times V_{in} \quad (j = 1, 2, 3). \tag{3.1}$$



(a) Switching states I.



(b) Switching states II.

Figure 3.5. Switching states of the 6X switched-capacitor dc-dc converter.

Consequently, as the sum of the voltages across C_{3a} and C_{3b}, the output voltage is six times the input. In reality, the two capacitors, C_{ja} and C_{jb} may be stabilized at a value slightly deviated from their theoretical values, because of the voltage drop, device tolerance and possibly diverse gate delays as analyzed and addressed in [95-97]. Nevertheless, the possible voltage difference

between a pair of capacitors, C_{ja} and C_{jb} are tolerable during operation, since they are involved in two independent upper and lower charge paths, as can be seen from the equivalent circuits in Figure 3.7.

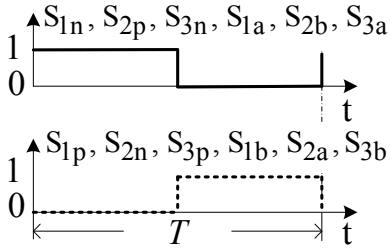
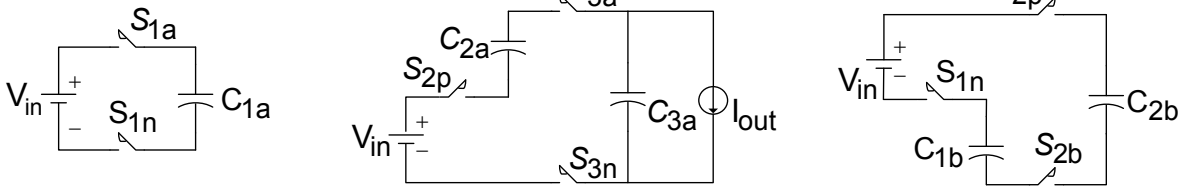


Figure 3.6. Complementary PWM signals

Table 3.1. Capacitor charge paths in two switching states

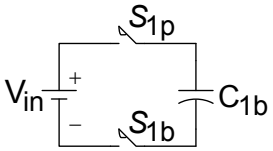
Switching state I		Switching state II	
Capacitor charge paths	On-state switches	Capacitor charge paths	On-state switches
$V_{in} \rightarrow C_{1a} \uparrow$	S_{1a}, S_{1n}	$V_{in} \rightarrow C_{1b} \uparrow$	S_{1b}, S_{1p}
$C_{2a} + V_{in} \rightarrow C_{3a} \uparrow$	S_{3a}, S_{3n}, S_{2p}	$C_{2b} + V_{in} \rightarrow C_{3b} \uparrow$	S_{3b}, S_{3p}, S_{2n}
$C_{1b} + V_{in} \rightarrow C_{2b} \uparrow$	S_{2b}, S_{2p}, S_{1n}	$C_{1a} \downarrow + V_{in} \rightarrow C_{2a} \uparrow$	S_{2a}, S_{2n}, S_{1p}



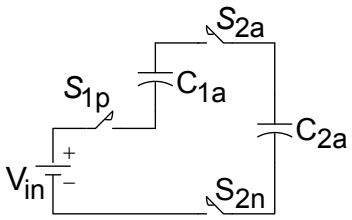
(a)Charging C_{1a}. (b) Charging C_{3a}. (c) Charging C_{2b}.

Figure 3.7. Charge/-discharge loops for two switching states.

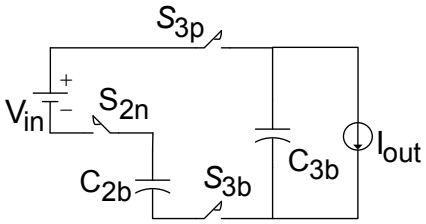
Figure 3.7 (cont'd)



(d) Charging C_{1b}.



(e) Charging C_{3b}.



(f) Charging C_{2a}.

3.4. Characteristics of the Proposed Switched-Capacitor DC-DC Converter

Evidently, the new circuit shares some of the salient features as the MMCCC: short current paths and low current stress, which are preferable for high voltage gain and high efficiency. Besides, it is much closer to a modular structure. A generalized NX dc-dc converter is depicted in Figure 3.8(a). It consists of N/2 basic cells (N=2k, k=1, 2,…) as shown in Figure 3.8(b). Inside each cell, a phase leg of two complementary switches S_{jp} and S_{jn} (j=1, 2, 3,…) and a pair of capacitors C_{ja} and C_{jb} are connected together at their respective midpoints. Externally, the switch phase leg is in parallel with the input voltage source; two terminals PC_{ja+} and PC_{jb-} are connected to the next cell; two terminals $PC_{(j-1)a+}$ and $PC_{(j-1)b-}$ from switches S_{ja} and S_{jb} respectively are connected to the preceding cell, expect that the first cell is directly fed by the input. Only the capacitor voltages in different cells differ, like in the MMCCC. Yet, in the new converter, since the capacitor voltages range from V_{in} to $N/2 \times V_{in}$ in different cells, rather than from V_{in} to NV_{in} as in MMCCC, it is easier for a modular design.

Moreover, the new converter has its unique features, compared to the original MMCCC for the same NX voltage ratio:

1) Two charge pump paths feed the load directly, leading to less power loss in the energy transfer.

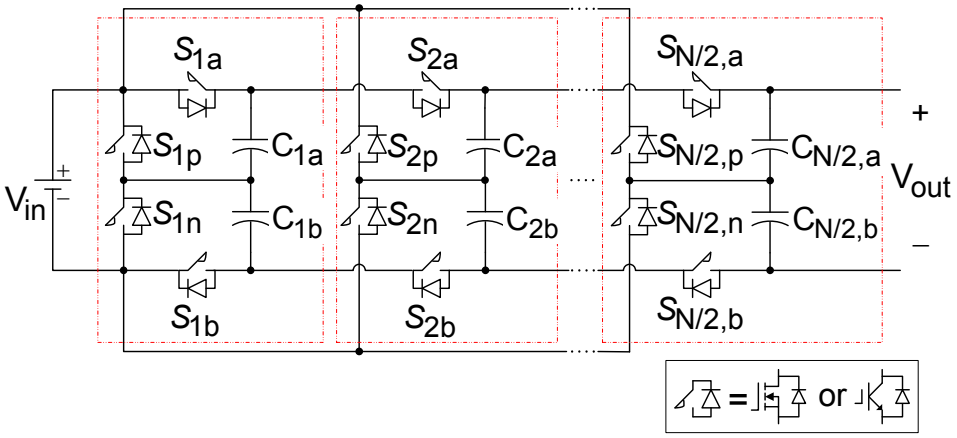
2) Half of the capacitors reduced their voltages by $N/2 \times V_{in}$. Switched-capacitor dc-dc converters rely on capacitors to transfer energy and to filter the output voltage. Normally the larger equivalent series resistance (ESR) associated with the higher capacitor voltage rating lowers the efficiency. Plus, capacitors contribute proportionally to the total volume and weight of the converter. High power density can be expected by employing low voltage capacitors.

3) There is lower capacitance and ripple current requirement for the two output capacitors. The output voltage ripples are reduced given the same capacitance as in the MMCCC, due to the interleaved charge/discharge of two output capacitors. It can be explained from the switching states in Figure 3.5: while one of the capacitors is being charged, the other one is being discharged. Consequently, the sum of two complementary voltage ripples makes the output voltage almost ripple-free. This feature is quite beneficial if the converter operates at zero-current switching (ZCS) as the ZCS-MMCCC does in [123], such that the output voltage ripples can be minimized. Besides, both output capacitors have smaller current ripples than the capacitors in the other basic cells, because they always supply load current while one of them gets charged alternatively.

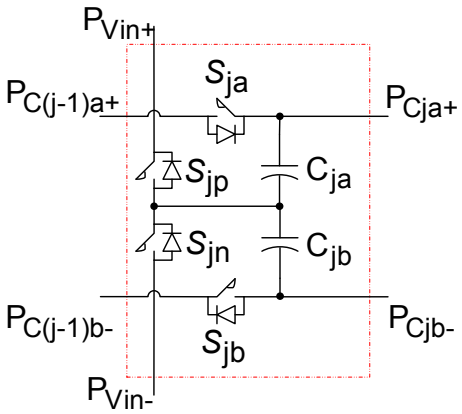
4) The new converter employs fewer switches (2N versus 3N–2 in MMCCC) with no penalty of total device power rating, as will be calculated in the later section. The associated gate drive and accessory power supply are saved accordingly.

5) Each pair of complementary switching devices is truly capacitor-clamped. For instance,

when S_{2a} in Figure 3.8(a) is gated off, the voltage across S_{2a} is clamped by a natural clamp circuit formed by capacitors C_{1a}, C_{1b}, C_{2a}, C_{2b} and the diode in S_{2b}. This is a virtue for designing a high power converter without assistance from extra clamping circuits.



(a) The generalized NX switched-capacitor dc-dc converter



(b) Basic cell.

Figure 3.8. A generalized NX switched-capacitor dc-dc converter constructed from basic cells.

In sum, its many features allow further higher efficiency with more compact package and lighter weight for high voltage boost gain than the MMCCC. Apparently, when N equals two, this converter reduces to the dc-dc converter module with a voltage conversion ratio of two in [111], in which very high efficiency was already demonstrated on a 10-kW converter.

3.5. Component Cost Comparison with Other Topologies

To compare the cost of the new converter with its counterparts, the total device power rating, the capacitor voltage stress, current rating and capacitance requirement are itemized. The total device power rating is based on the product of the maximum voltage imposed on the device and the average current flowing through it over the duration when the device conducts. Note that neither the peak current nor RMS current is used. In this way, the comparison is less dependent on the actual shape of the charge and discharge current, which is a function of the ESR and equivalent series inductance (ESL).

3.5.1. Total Device Power Rating

1) For the original flying-capacitor (FC) structure, all the 2N devices sustain the voltage equal to the input voltage and the input current. Its TDPR is the same as the traditional boost converter:

$$TDPR_{FC} = 2N \cdot (V_{in} \cdot I_{in}) = 2N \cdot P_{in} \tag{3.2}$$

where V_{in} is the input voltage and I_{in} is the input current.

2) The MMCCC also pumps charge from one capacitor to the next one, but its switching states reduce to two. Thus, the charge current into one capacitor is the discharge current from its preceding capacitor, except that the output capacitor has half the charge and discharge current. Also considering that the average charge current of one capacitor in half switching period equals its average discharge current in the other half switching period, the average current through each switching device is $2I_{out}$ in one of the two switching states. There are (N–2) switches sustain twice the input voltage, as stated earlier. Thus, the TDPR is

$$TDPR_{MMCCC} = 2N \cdot V_{in} \cdot (2I_{out}) + (N-2) \cdot 2V_{in} \cdot (2I_{out})$$
$$= \frac{8N-8}{N} P_{in} \qquad (N = 2,3,4,...). \tag{3.3}$$

3) For the new converter, the (N–2) switches in the complementary phase leg convey the sum of the current in two charge pump paths, $4I_{out}$, which is twice the current through the rest switches. It is not hard to find the voltage stress of each switch. Hence, the TDPR can be derived as:

$$TDPR_{new} = (N-2)V_{in} \cdot 4I_{out} + (2+2)V_{in} \cdot 2I_{out}$$
$$+(N-2)2V_{in} \cdot 2I_{out}$$
$$= \frac{8N-8}{N} P_{in} \qquad (N = 2,4,6,...). \tag{3.4}$$

The above equations clearly demonstrate that unlike the conventional flying-capacitor structure, the new converter has no penalty of total device power rating even with fewer devices than the MMCCC. The ratio of the TDPR and the input power is plotted with respect to the voltage gain in Figure 3.9. It is quite interesting that this ratio for the new converter will get saturated as N approaches infinite. This property is different from the TDPR in the FC as well as in the conventional two-level boost converter. It can be physically explained by the aforementioned fact that the charge/discharge current will only go through three switching devices at most, and that the maximum switching device voltage stress is no more than $2V_{in}$, in spite of the increment of voltage gain.

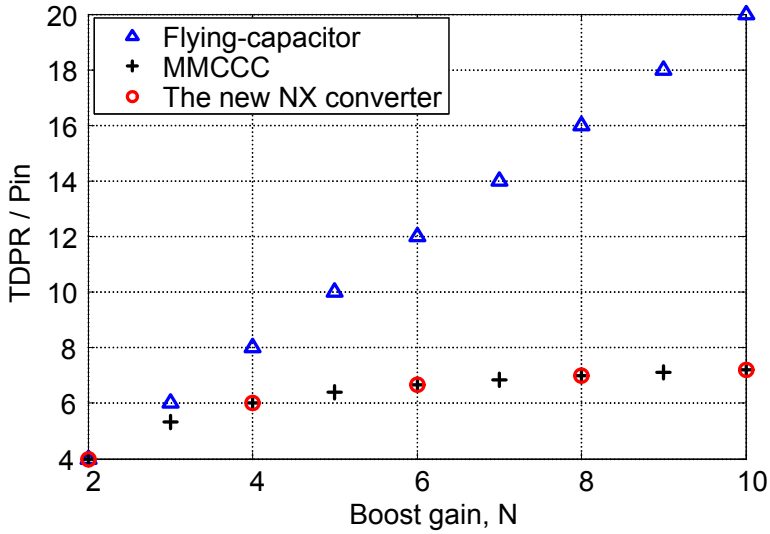


Figure 3.9. Normalized total device power rating vs. voltage boost gain

3.5.2. Capacitor Voltage, Current and Capacitance Requirement

Table 3.2 compares the total capacitor voltage, the current and the capacitance of the new converter with that of the FC and MMCCC. While the voltage ratings for the FC and the MMCCC are the same, the voltage rating for the new converter is reduced nearly by half, as plotted in Figure 3.10. The RMS current is related to the parasitic parameters in the circuit, but the average charge (/discharge) current of the internal capacitors in the new converter (and in the MMCCC) can be calculated as 2/N times of the current in the FC dc-dc converter, as stated before; the average charge (/discharge) current of the two output capacitors is 1/(N-1) times of that in the FC dc-dc converter. Thereby, the capacitance requirement can be obtained accordingly. The quantitative comparison supports the statement that the ripple current and capacitance requirement of the two output capacitors in new converter can be much lower.

Table 3.2. Comparison of capacitor voltage rating, current and capacitance

	Total capacitor voltage ratings	Average charge/discharge current	Capacitance requirement
FC	$\frac{(1+N)N}{2}V_{in}$	$I_j=\begin{cases}NI_{out}, & (j=1,2,...,N-1)\\(N-1)I_{out}, & (j=N)\end{cases}$	$C_j=\begin{cases}\frac{I_{out}}{f_s\Delta V_j}, & (j=1,2,...,N-1)\\\frac{(N-1)I_{out}}{Nf_s\Delta V_j}, & (j=N)\end{cases}$
MM-CCC	$\frac{(1+N)N}{2}V_{in}$	$I_j=\begin{cases}2I_{out}, & (j=1,2,...,N-1)\\I_{out}, & (j=N)\end{cases}$	$C_j=\begin{cases}\frac{I_{out}}{f_s\Delta V_j}, & (j=1,2,...,N-1)\\\frac{I_{out}/2}{f_s\Delta V_j}, & (j=N)\end{cases}$
NX	$\frac{(1+N/2)N}{2}V_{in}$ $(N=2,4,6,...)$	$I_{ja}=I_{jb}$ $=\begin{cases}2I_{out}, & (j=1,2,...,\frac{N-1}{2})\\I_{out}, & (j=\frac{N}{2})\end{cases}$	$C_{ja}=C_{jb}$ $=\begin{cases}\frac{I_{out}}{f_s\Delta V_j}, & (j=1,2,...,\frac{N-1}{2})\\\frac{I_{out}/2}{f_s\Delta V_j} & (j=\frac{N}{2})\end{cases}$

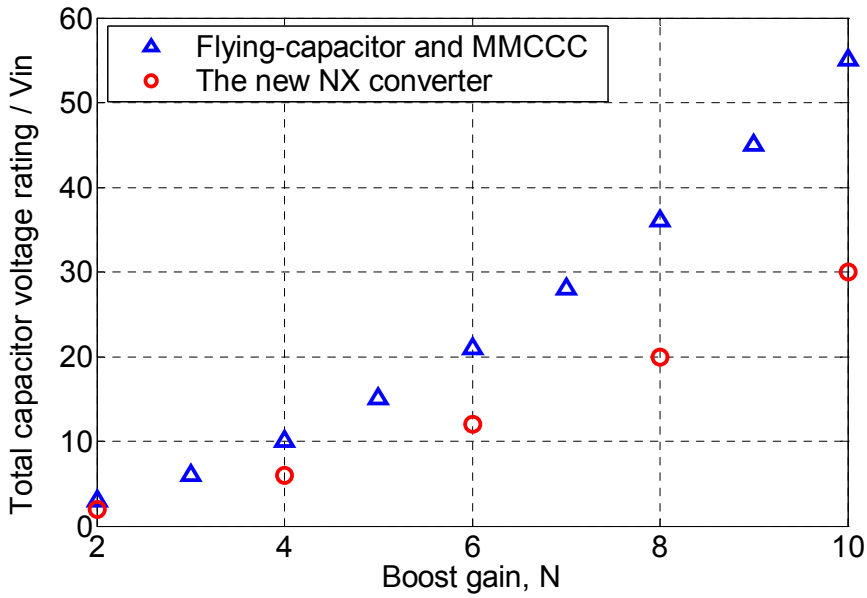


Figure 3.10. Normalized total capacitor voltage rating vs. voltage boost gain.

3.6. Power Loss Analysis

The power loss is broken down into the conduction loss, switching loss and gate drive loss. The conduction loss, which includes the charge/discharge loss due to the ESR of the capacitors, is the dominant loss in this design. Thereby, the problem turns to identifying the current in the individual charge/discharge loops in two switching states. Since the two states are essentially symmetric, the total loss is calculated based one of the switching states as shown in Figure 3.5(a) and multiplying it by two. This switching state is divided into three charge/discharge loops, as illustrated in Figure 3.11. In the modular design, each module is fed by two parallel electrolytic capacitors in a distributed way, and the ESR introduced in each module is defined as Rin. An MOSFET is modeled as an equivalent series resistance (ESR). To decouple the two loops sharing the same MOSFET $S_{jp(n)}$ (j=1, 2), the resistor $R_{Sjp(n)}$ is split into two equivalent resistors $2R_{Sjp(n)}$ in parallel, based on the fact that the average is ideally the same. In fact, they are equal only if the currents are exactly identical. Nonetheless, this approximation only makes the assumption a little more conservative.

Stray inductance lumped as L_S is advantageously utilized in the circuit to reduce the capacitance requirement and to mitigate the impulse charge current present in the switched-capacitor circuit where the capacitor and the ESR used to be the main players in the circuit. The presence of the ESL makes the initial current in each loop starts from zero. Define the resonant frequency in each loop as:

$$\omega_j = \sqrt{\frac{1}{L_S C_{loopj}} - \alpha_j^2}, \quad j = 1, 2, 3 \tag{3.5}$$

where the decay rate $\alpha_j = R_j / (2L_s)$, C_{loopj} is the equivalent loop capacitance as will be detailed later.

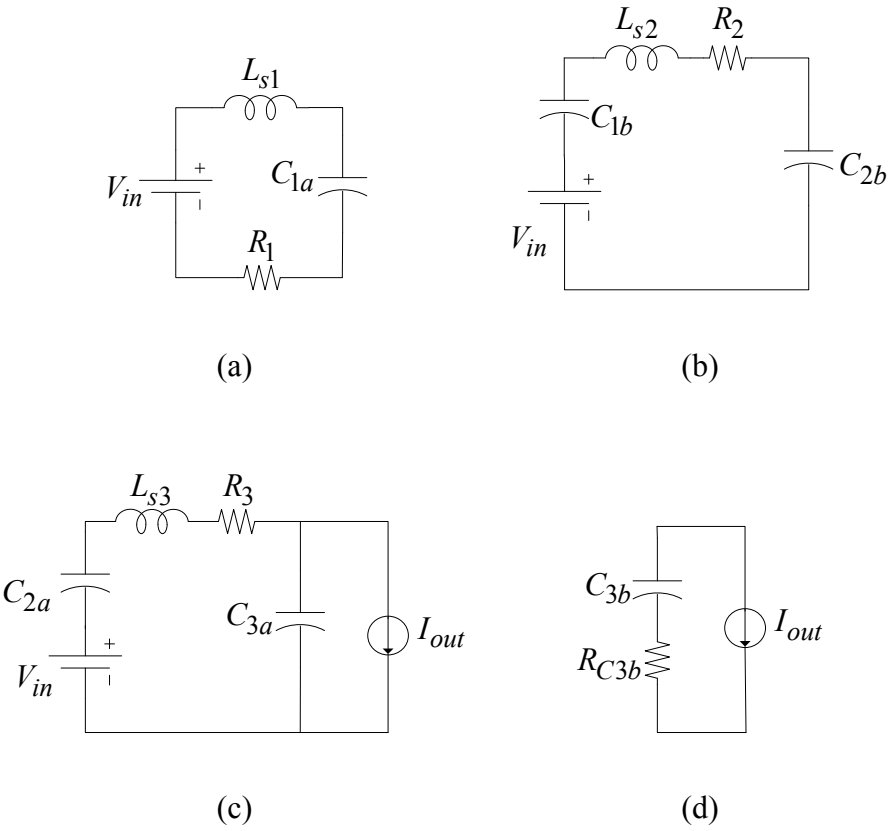


Figure 3.11. Equivalent circuits of Switching State I counting in the ESL and ESR.

1) The charge loop for C_{1a}

The capacitor C_{1a} gets charged by the input. The equivalent circuit is reduced to Figure 3.11(a). The current loop can be expressed as

$$i_1(t) = e^{-\alpha_1 t}(C_1 \Delta V_1 \frac{\alpha_1^2 + \omega_1^2}{\omega_1} \sin \omega_1 t) \tag{3.6}$$

where $C_1 = C_{1a} = C_{1b}$, ESR in the loop is: $R_1 = R_{Sja} + 2R_{Sjn} + R_{in} + R_{C1a} + R_{Ls1}$, and the

voltage difference is $\Delta V_1 = \frac{1}{2}\frac{2I_{out} \cdot T/2}{C_1} \approx \frac{P_{out}T}{C_1(12V_{in})}$.

2) The charge loop for C_{2b}

In this loop as shown in Figure 3.11(b), one more capacitor comes into the picture. The capacitors C_{1b} and C_{2b} are equivalently in series, making the loop capacitance $Cloop_2 = \frac{C_1 C_2}{C_1 + C_2}$, where $C_2 = C_{2a} = C_{2b}$.

The loop current can be computed as

$$i_2(t) = e^{-\alpha_2 t}(C_{loop2}\Delta V_2 \frac{\alpha_2^2 + \omega_2^2}{\omega_2}\sin \omega_2 t) \tag{3.7}$$

where the ESR in the loop is: $R_2 = R_{Sjb} + 2(2R_{Sjn}) + R_{in} + R_{C1b} + R_{C2b} + R_{Ls2}$ and the voltage difference is $\Delta V_2 \approx \frac{1}{2}\frac{P_{out}T}{6V_{in}}(\frac{1}{C_1} + \frac{1}{C_2})$.

In general, for a conversion ratio of NX (N=6, 8, 10, …), the charge/discharge loops, except the two final output stages, comply with a general equation:

$$i_j(t) = e^{-\alpha j t}(C_{loopj}\Delta V_j \frac{\alpha_j^2 + \omega_j^2}{\omega_j}\sin \omega_j t), \quad for\ j = 1, 2, ..., (N/2 - 1) \tag{3.8}$$

3) The charge/discharge loop for the output stage

The output stage is different from the others. The load current, I_{out} gets involved via discharging the output capacitors $C_{3a(b)}$, as shown in Figure 3.11(c). It can be approximated as a constant dc, due to the fact that the output voltage is almost ripple-free. The resultant loop current is:

$$i_3(t) = e^{-\alpha_3 t}\left[-k_1 \cdot \cos\omega_3 t + k_2 \cdot \sin\omega_3 t\right] + k_1 \tag{3.9}$$

where the ESR in the loop is: $R_3 = R_{Sja} + 2(2R_{Sjn}) + R_{in} + R_{C2a} + R_{C3a} + R_{Ls3}$, the constant is defined as $k_1 = \frac{C_2 I_{out}}{C_2 + C_3}$, $k_2 = \frac{\left(\alpha_3^2 + \omega_3^2\right) C_{loop3}\left(\Delta V_3 - \frac{C_2 R_{s3} I_{out}}{C_2 + C_3}\right) + \frac{\alpha_3 C_2 I_{out}}{C_2 + C_3}}{\omega_3}$. The loop capacitance is $Cloop_3 = \frac{C_2 C_3}{C_2 + C_3}$ with $C_3 = C_{2a} = C_{2b}$, and the voltage difference is: $\Delta V_3 \approx \frac{1}{2}\frac{P_{out} T}{6 V_{in}}\left(\frac{1}{C_2} + \frac{1}{2C_3}\right)$.

A. Conduction loss

With the loop current obtained, the conduction loss for three loops can be calculated:

$$P_{con1} = \frac{1}{T}\int_0^{\frac{T}{2}} i_1^2 R_1 dt$$
$$= \frac{1}{2T}\left(\frac{P_{out} T}{I_{out}} \cdot \frac{\alpha_1^2 + \omega_1^2}{\omega_1}\right)^2 R_1 \cdot \left[\frac{1 - e^{-\alpha_1 T}}{2\alpha_1} - \frac{\alpha_1 - e^{-\alpha_1 T}\left(\alpha_1 \cos\omega_1 T - \omega_1 \sin\omega_1 T\right)}{2\left(\alpha_1^2 + \omega_1^2\right)}\right] \tag{3.10}$$

$$P_{con2} = \frac{1}{T}\int_0^{\frac{T}{2}} i_2^2 R_2 dt$$
$$= \frac{1}{2T}\left(\frac{P_{out} T}{I_{out}} \cdot \frac{\alpha_2^2 + \omega_2^2}{\omega_2}\right)^2 R_2 \cdot \left[\frac{1 - e^{-\alpha_2 T}}{2\alpha_2} - \frac{\alpha_2 - e^{-\alpha_2 T}\left(\alpha_2 \cos\omega_2 T - \omega_2 \sin\omega_2 T\right)}{2\left(\alpha_2^2 + \omega_2^2\right)}\right] \tag{3.11}$$

For the output stage, the conduction loss counts in the loss of the output capacitor C_{3b} being discharged by the load current:

$$P_{con3} = \frac{1}{T}\left(\int_0^{\frac{T}{2}} i_3^2 R_3 dt + \frac{T}{2} \cdot I_{out}^2 R_{C3} \right)$$

$$= \frac{k_1^2 + k_2^2}{2T} \cdot \left[\frac{1 - e^{-\alpha_3 T}}{2\alpha_3} + \frac{k_1^2 - k_2^2}{2} \cdot \frac{\alpha_3 - e^{-\alpha_3 T}\left(\alpha_3 \cos \omega_3 T - \omega_3 \sin \omega_3 T\right)}{2\left(\alpha_3^2 + \omega_3^2\right)} \right]. \quad (3.12)$$

The total conduction loss is twice the sum of the above itemized losses:

$$P_{con} = 2(P_{con1} + P_{con2} + P_{con3}) . \quad (3.13)$$

B. Switching loss

For the purposes of estimating the current at the instant when the MOSFET is turned off, substitute the value of the actual duty cycle times the switching cycle, $D \cdot T$ into (3.6), (3.7) and (3.9). If the dead time (<100 ns) is neglected, $D \cdot T$ is simplified to $T/2$, and the current at the end of this half switching cycle is:

$$i_1(\frac{T}{2}) = e^{-\alpha_1 \cdot T/2}(C_1 \Delta V_1 \frac{\alpha_1^2 + \omega_1^2}{\omega_1} \sin \omega_1 \cdot T/2) . \quad (3.14)$$

When the resonant frequency of each charge/discharge loop is designed to be close to but below the switching frequency of the converter, the switching-off current is very small. More interesting, a natural zero-voltage turn-on and turn-off can occur for the MOSFETs $S_{jp(n)}$. For example, during the transition from Switching State I to Switching State II, the ESL in the circuit forces the loop current to charge the junction capacitors of S_{1n}, S_{2p} and S_{3n} and discharge the junction capacitors of their complementary switches. After S_{1n}, S_{2p} and S_{3n} turn off, the inductive currents freewheel through the diodes during the short dead time, if only they have not decayed to zero. The freewheeling loops are shown in Figure 3.12. When the converter enters

into the Switching State II, the MOSFETs S_{1p}, S_{2n} and S_{3p} can be turned on at zero-voltage. It is the same for the transition from Switching State II to Switching State I, due to the symmetry. Thus, their switching loss can be negligible. The total switching loss is mainly the loss of charging and discharging the junction capacitors of the MOSFETs $S_{ja(b)}$:

$$P_{sw} = \left(C_1 V_{in}^2 \times 2 + C_2 \left(2V_{in} \right)^2 \times 4 \right) \times f_s \,. \tag{3.15}$$

C. Gate drive loss

Turn-on and turn-off twice. Therefore, the gate drive loss is arrived at:

$$P_{gd} = V_{gs} \cdot (Q_{Sjp(n)} + Q_{Sja(b)}) f_s \cdot N \tag{3.16}$$

where N=6 indicating N pairs of MOSFETs $S_{jp(n)}$ and $S_{ja(b)}$, and $V_{gs} = 12\,V, Q_{Sjp(n)} = 195\,nC, Q_{Sja(b)} = 210\,nC$.

D. The total loss:

$$P_{loss} = P_{con} + P_{sw} + P_{gd} \,. \tag{3.17}$$

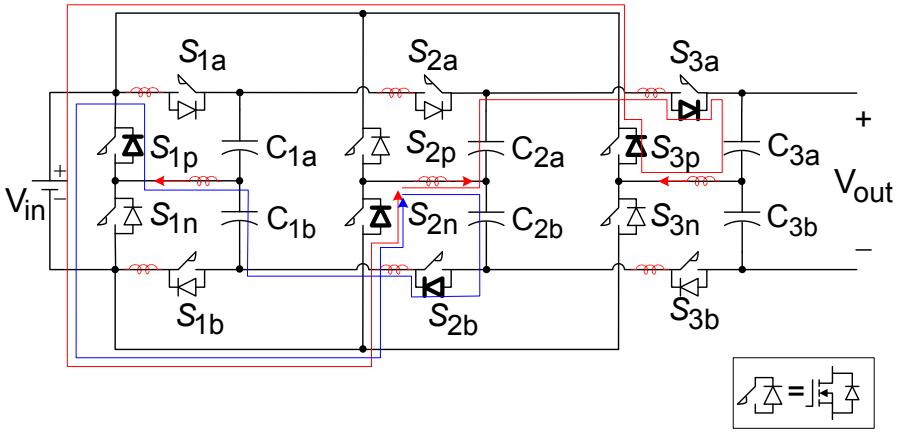


Figure 3.12. Transient state after the Switching States I.

3.7. Simulation and Experimental Verification

The principle and analysis are verified by simulation and experiments of a 6X 450-W prototype. The modular configuration in the simulation and experiment is depicted in Figure 3.13. Ceramic capacitors C5750X7S2A106M are used. Since their capacitance is affected by the operating voltage, the equivalent capacitance at their corresponding voltages is: $C_{1a(b)}$≈120 μF, $C_{2a(b)}$≈60 μF, $C_{3a(b)}$≈40 μF, according to the manufacture's data. The switching frequency is 100 kHz. The MOSFET IRF1324S-7PPbF is employed for the devices $S_{jp(n)}$, and IRFS3004-7PPbF is for $S_{ja(b)}$. The minimum stray inductance needs to be more than 21 nH in the first module, and to be more than 63 nH and 84 nH for the second and third module respectively, based on the critical zero current condition and the equivalent loop capacitance. Considering the parameter tolerance and variation, the stray inductance is intentionally designed to make the converter switch off at relatively small yet non-zero current.

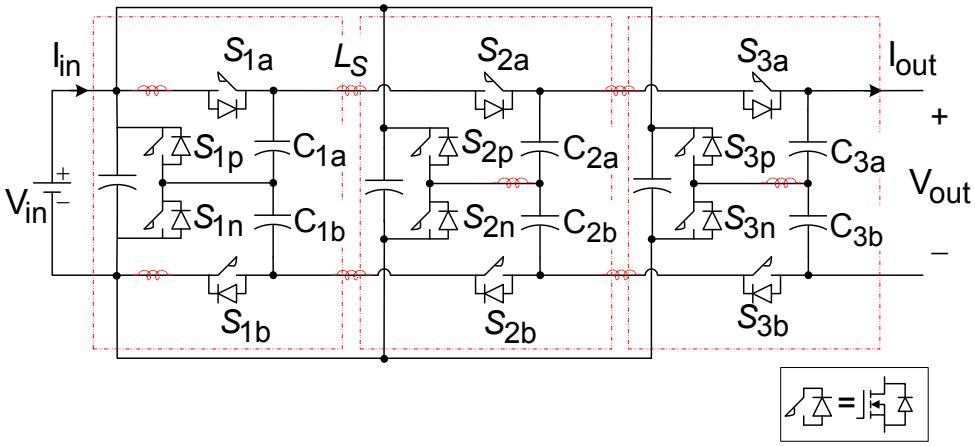


Figure 3.13. Simulation and experimental configuration.

Simulation results were shown from Figure 3.14 and Figure 3.16. In Figure 3.14, V_{GS1a} and V_{GS1b} represent two complementary gate drive signals, and voltages V_{S1a} ($/V_{S1b}$) and V_{S3a}

($/V_{S3b}$) represent two kinds of voltage stress across the switching devices. The capacitor voltages are shown in Figure 3.15. The input/output voltages and currents are shown in Figure 3.16. The corresponding experimental results are given from Figure 3.17 to Figure 3.20. The output voltage is boosted from a 12-V input to 68.2 V. Note that the input current, I_{in} is referred to the current before the capacitors across the input dc bus as shown in Figure 3.13. As can be seen from Figure 3.18 and Figure 3.19, the two symmetric capacitors in one basic cell have the same very low average voltage and nearly complementary voltage ripples. Hence, the output voltage ripple is quite small as shown in Figure 3.20. The experimental results agree with the analysis and simulation. The calculated efficiency and the experimental result are given in Figure 3.21. The input voltage is 12 V and the gate drive power loss of 2.9 W is included. The power loss analysis well predicts the trend of the efficiency variation vs. the power. The calculated efficiency is a bit more above the experimental result at the light-load condition because the loop current becomes insufficient to make the soft switching assumption valid.

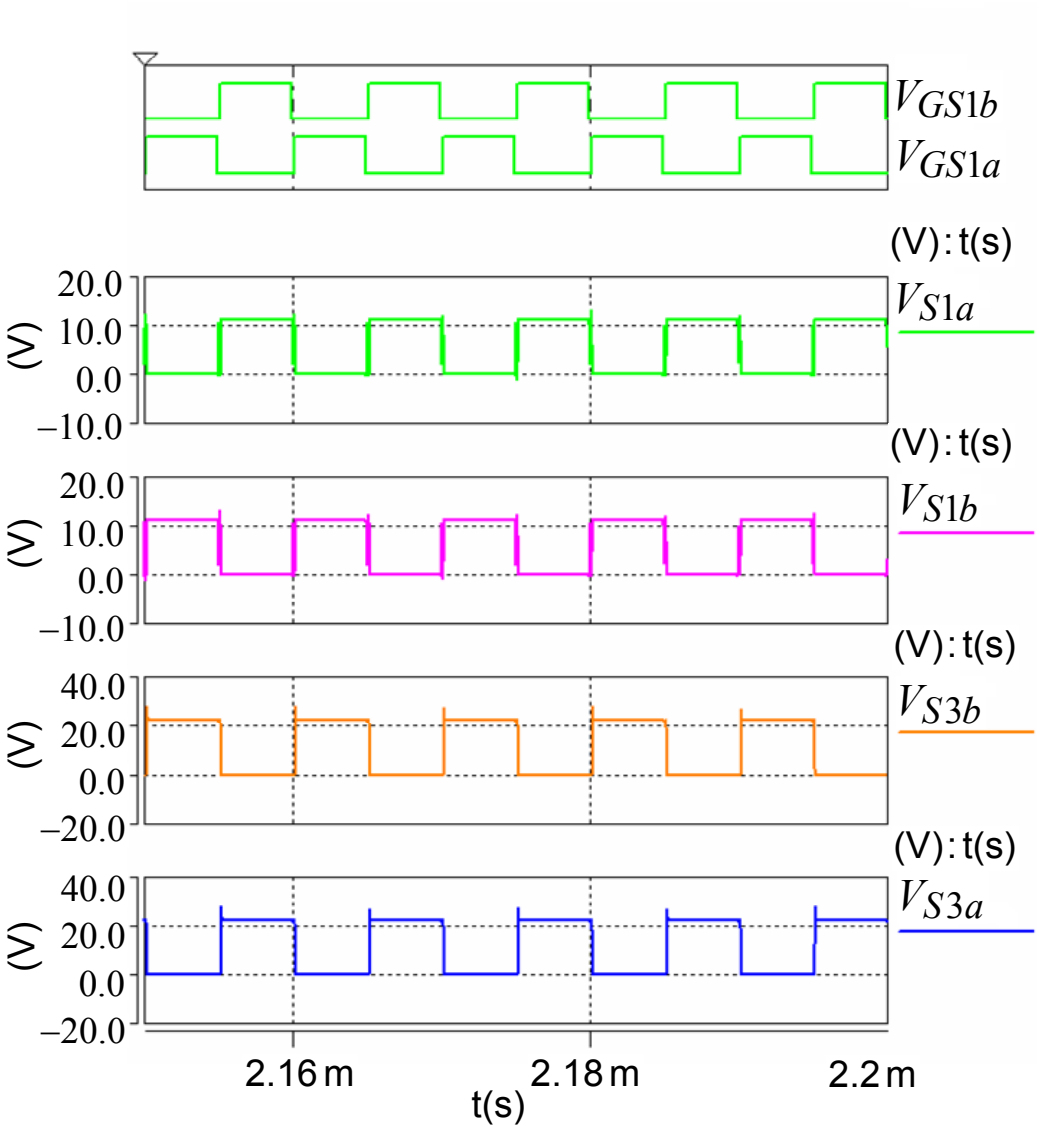


Figure 3.14. Simulation results of gate drive signals and typical switch voltages.

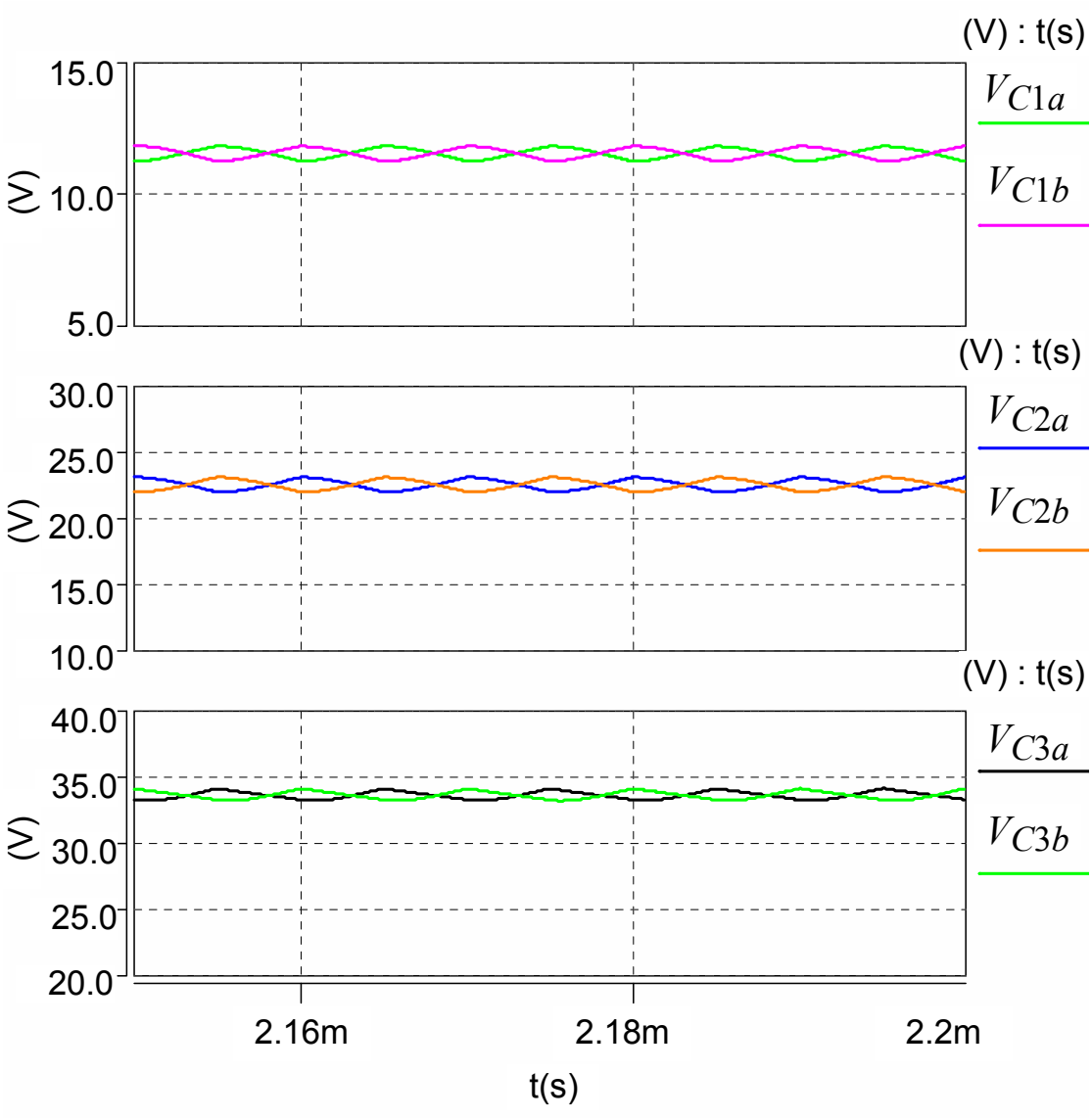


Figure 3.15. Simulation results of capacitor voltages.

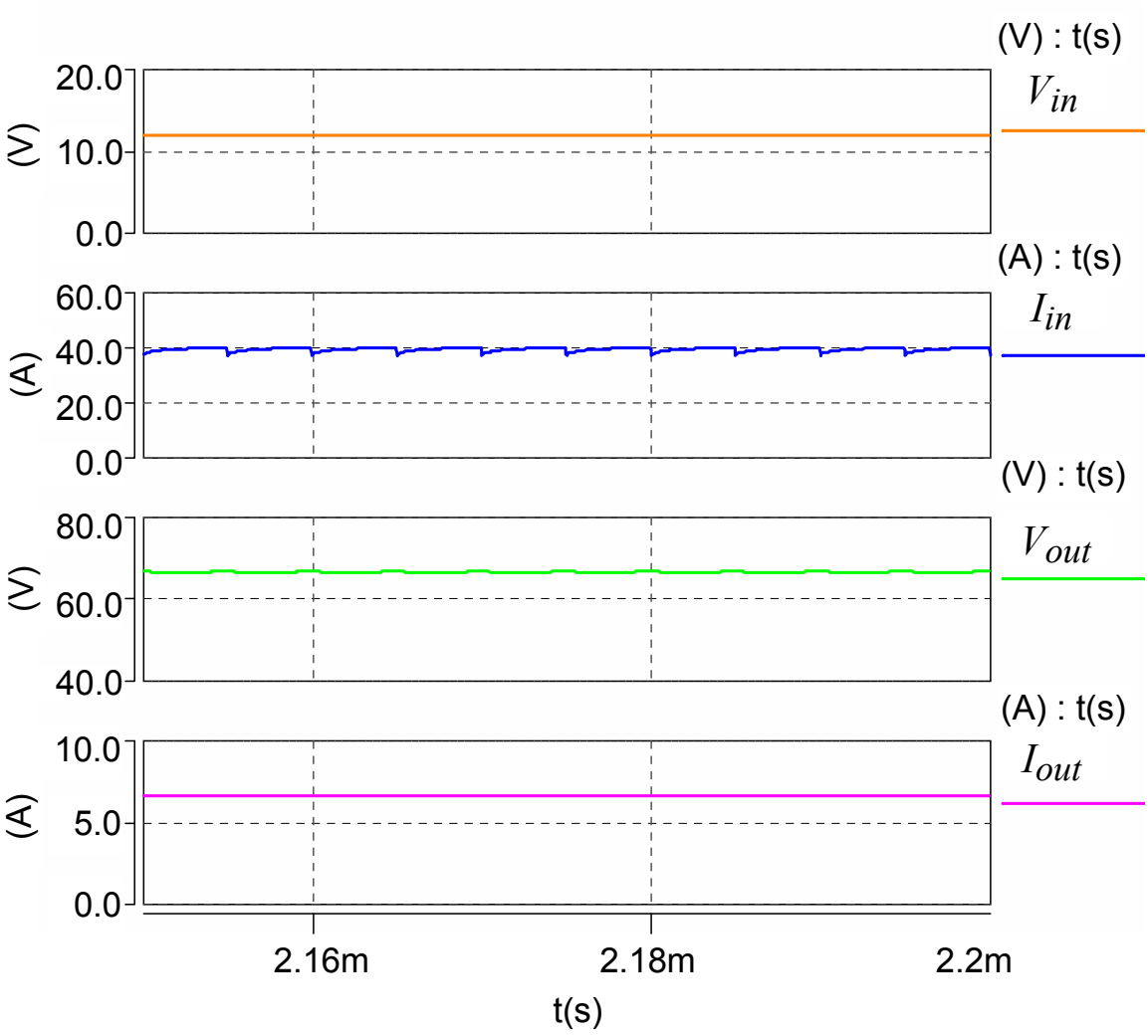


Figure 3.16. Simulation results of input/output voltages and currents.

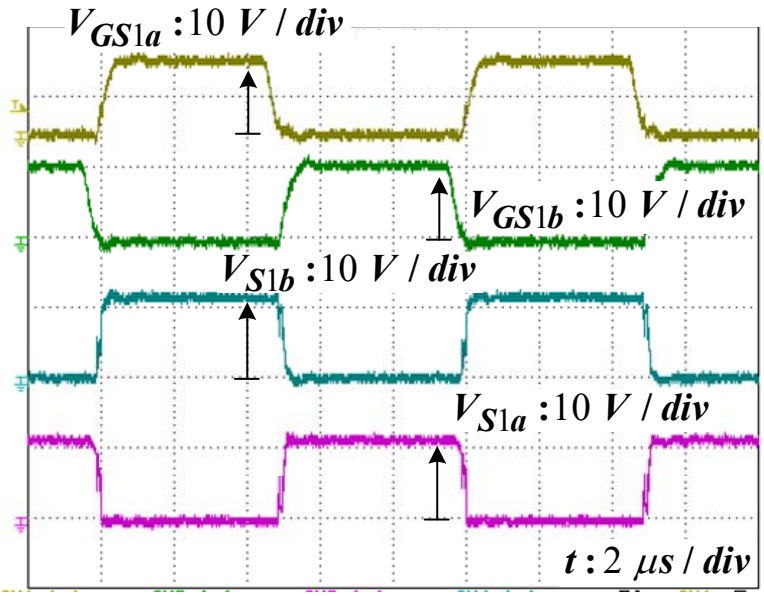


Figure 3.17. Experimental results of complementary gate drive signals and the corresponding switches.

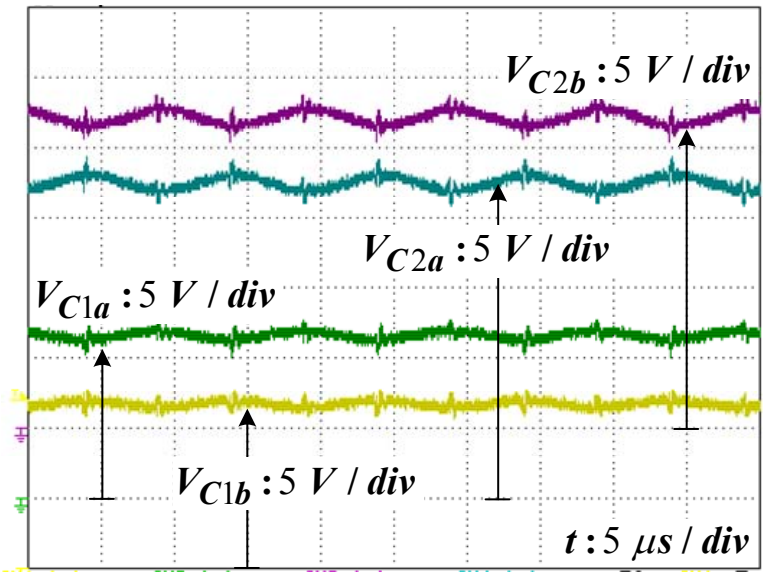


Figure 3.18. Experimental results of capacitor voltage $V_{C1a(b)}$ and $V_{C2a(b)}$.

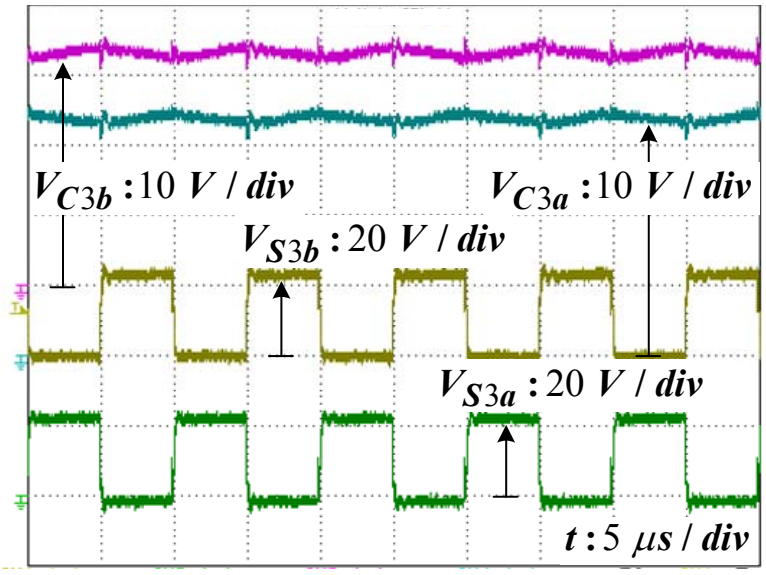


Figure 3.19. Experimental results of capacitor voltage $V_{C3a(b)}$ and switch waveform $V_{S3a(b)}$.

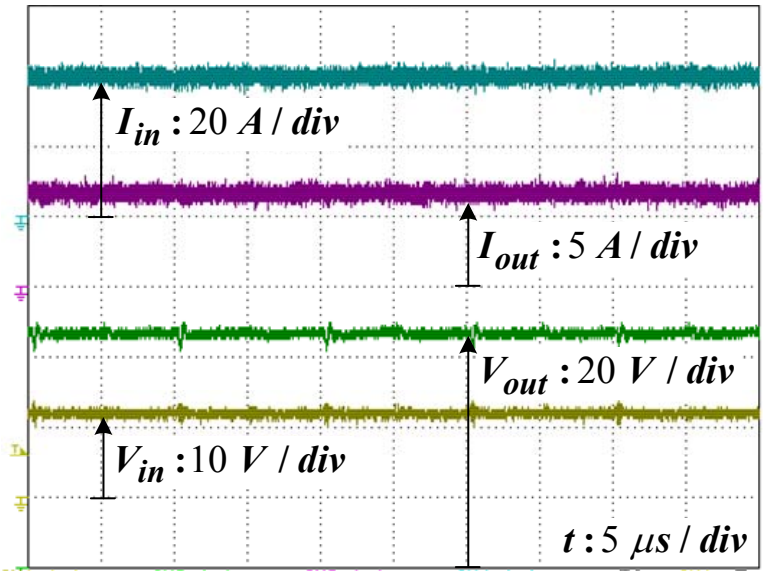


Figure 3.20. Experimental results of input/output voltage and current

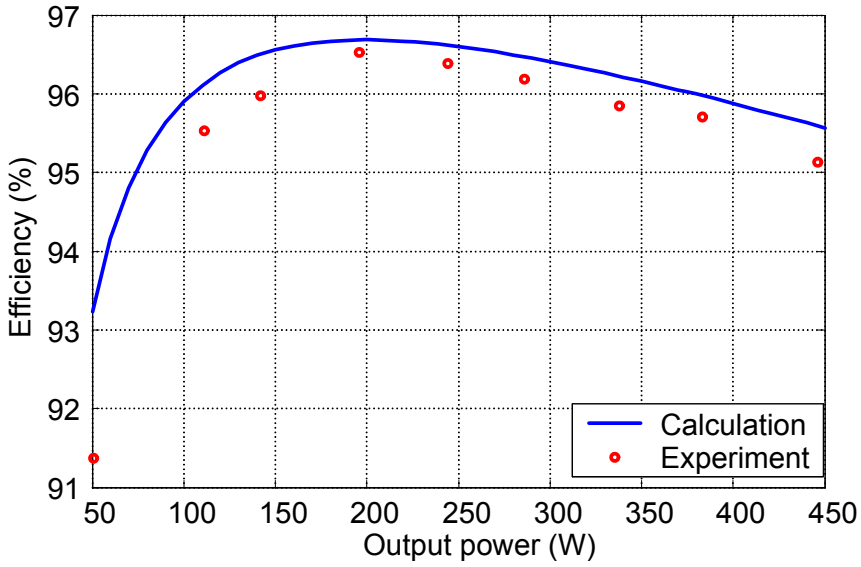


Figure 3.21. Comparison of calculated and tested efficiency

3.8. Application Examples

One of the applications of the new converter is the high-gain voltage boosting for TEG. Isolated dc-dc converters are usually applied to achieve high voltage gain, although no isolation is needed. The associated transformer degrades efficiency. A multi-phase ZCS MMCCC has been proposed in [124], which involves many switching devices, which affects reliability. A configuration example using the NX dc-dc converter is shown in Figure 3.22. The original $S_{ja(b)}$ can be either diode or MOSFET for the unidirectional operation. The NX converter produces an unregulated voltage of clearly N times the generated voltage from TE module(s). It can be followed by a boost- or buck-type dc-dc regulator, such as a traditional boost or buck converter, three-level flying capacitor dc-dc [91], resonant switched-capacitor [125] and so on. Since the regulator is only dedicated to voltage regulation, and the maximum power point tracking (MPPT) or load matching, their current stress and the power rating is dramatically mitigated. As a result, a high efficiency can still be expected.

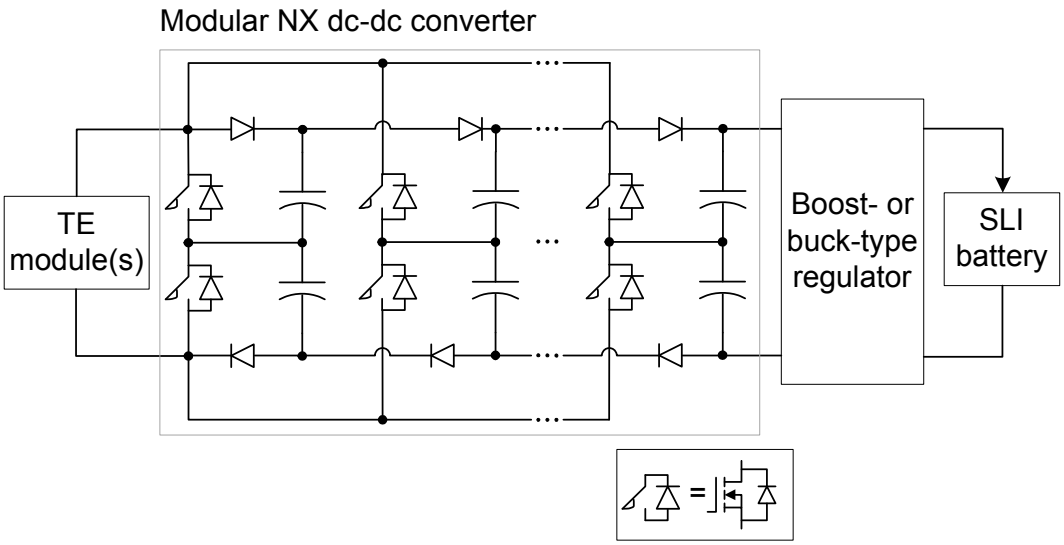


Figure 3.22. Modular NX dc-dc converter for the voltage boosting in TEG.

Another prospective application is PV micro inverters. As briefly introduced in Chapter 1, a micro inverter is comprised of a dc-dc converter and a dc-ac inverter. The NX dc-dc converter is employed to boost the low voltage from the PV panel to a decent voltage for the dc-ac inversion stage afterwards. It can be directly mounted underneath the PV panel. The next question is: what about the dc-ac inverter in the micro converter? It will be answered in the next chapter.

3.9. Summary

A novel switched-capacitor dc-dc converter with the potential of high voltage gain is proposed. Compared to its switched-capacitor dc-dc converter counterpart, it has the main advantages:

- Less power loss due to the two symmetric short paths of charge pumps;

- Substantially reduced total capacitor voltage ratings;

- Lower capacitance and ripple current requirement of the output capacitors;

- Reduced switching device count, low device current stress and low total device power rating;

- Improving efficiency;

- Lower cost;

- Able to have bidirectional operation;

- Quasi modular structure.

The experimental results verified the operation principle and features.

Chapter 4 Trans-Z-Source Inverters

4.1. Introduction

Generally, there exist two types of traditional inverters: voltage source inverters (VSI) and current source inverters (CSI) as shown in Figure 4.1 and Figure 4.2. Traditional VSIs and CSIs have similar limitations and problems. For VSIs: 1) The obtainable ac output voltage can not exceed the dc source voltage. So a dc-dc boost converter is needed in the applications, for instance, with limited available dc voltage or with the demand of higher output voltage. 2) Dead time is required to prevent the shoot-through of the upper and lower switching devices of each phase leg. However, it induces waveform distortion. For CSIs: 1) Their output voltage can not be lower than the dc input voltage. 2) Overlap time between phase legs is required to avoid the open-circuit of all the upper switching devices or all the lower devices. A Z-source inverter (ZSI) [126] as shown in Figure 4.3, as well as the derived quasi Z-source inverters (qZSI) [127, 128], has been proposed to overcome the above problems. They advantageously utilize the shoot-through of the inverter bridge to boost voltage in the VSIs (or open-circuit in the CSIs to buck voltage). Thus, buck-boost functionality is achieved with a single stage power conversion. They also increase the immunity of the inverters to the EMI noise [129], which may cause mis-gating and shoot-through (or open-circuit) to destroy the conventional VSIs and CSIs.

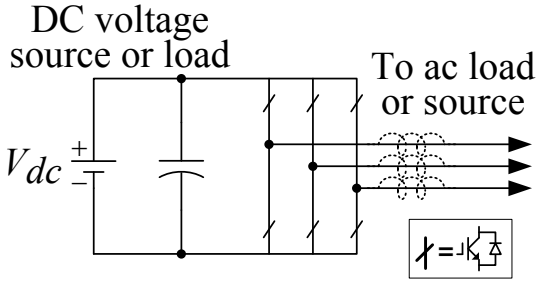


Figure 4.1. Voltage source inverter

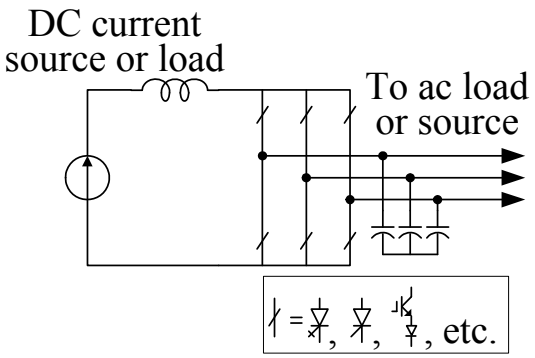


Figure 4.2. Current source inverter

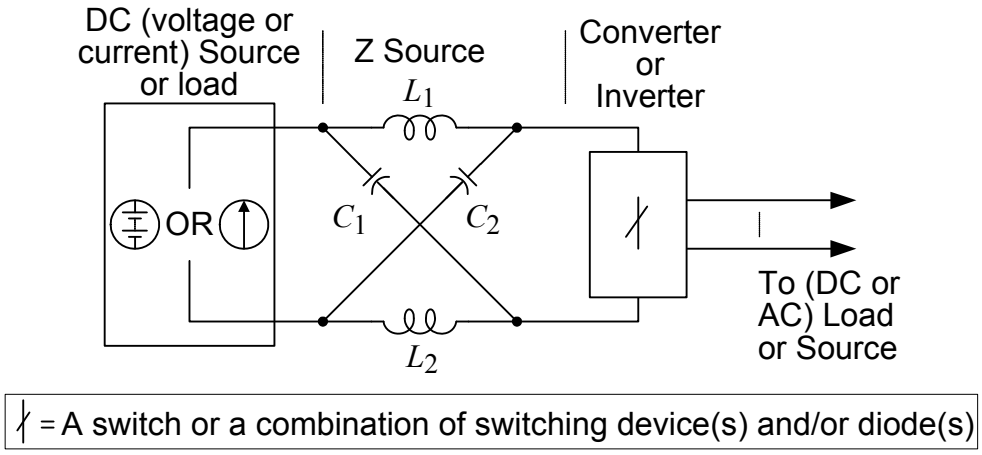


Figure 4.3. Z-source inverter

The voltage-fed (VF) Z-source inverter can have theoretically infinite voltage boost gain. However, the higher the voltage boost gain is, the smaller modulation index has to be used. In applications such as grid-connected photovoltaic (PV) generation and fuel cell power conversion, a low voltage dc source has to be boosted to a desirable ac output voltage. A small modulation index results in a high voltage stress imposed on the inverter bridge. Several pulse width modulation (PWM) methods [130, 131] have been developed with the attempt of obtaining as much voltage gain as possible and thus limiting the voltage stress across the switching devices. The maximum boost control [130] achieves the maximum voltage gain through turning all the zero states in the traditional VSIs to shoot-through zero states. Nevertheless, it brings in low

frequency ripples associated with the ac side fundamental frequency. So the constant boost control [131] has been proposed to eliminate those ripples and thus reduce the L and C requirement in the Z-source network, with slightly less voltage gain, compared to the maximum boost control. These PWM methods still have limits to further extend the voltage gain without sacrificing the device cost. Recently, some modified impedance source networks were proposed in [132-135] for the sake of increasing the output voltage gain. Among them, a T-source inverter [132] has the possibility of increasing voltage gain with the minimum component count. As will be discussed in the next section, it can be grouped into a general class of transformer based Z-source inverters (trans-ZSIs) presented in this paper, which employ two transformer windings in the impedance network.

The voltage-fed Z-source/quasi Z-source inverters can not have bidirectional operation unless replacing the diode with a bidirectional conducting, unidirectional blocking switch [136]. Neither can the traditional current source inverters ([137-139]) do unless they are fed by a phase-controlled rectifier in front that can change the dc link voltage polarity. Interestingly, the current-fed (CF) Z-source/quasi Z-source inverters [127, 140, 141] can have voltage buck-boost and bidirectional power flow only with a diode in the impedance network. With the newly developed reverse blocking IGBTs [142], this single stage power converter becomes a promising topology. Yet, their dc–ac voltage gain can not exceed two in the boost mode operation. In other words, the dc input voltage cannot be lower than half of the peak output line-to-line voltage. Hence, this paper further proposes two current-fed trans-Z-source inverters that are capable of reaching wider voltage boost range and bidirectional power flow with a single diode. As a result, a wider output voltage range can be obtained, which is essential to some applications such as HEV/EV motor drives.

The trans-Z-source inverters can be derived from the voltage-/current-fed quasi Z-source inverters or the voltage-/current-fed Z-source inverters. The trans-Z-source-inverters inherit their unique features, and they can be controlled using the PWM methods applicable to the Z-source inverters. This paper will begin with the derivation of two voltage-fed trans-Z-source inverters from one of the quasi Z-source inverters. Next, the same idea is extended to the development of two current-fed trans-Z-source inverters. Then the followed comparative analysis, simulation and experimental results will demonstrate their new properties different from the Z-source/quasi Z-source inverters.

4.2. The Voltage-fed Trans-Z-Source Inverters

In the voltage-fed quasi Z-source inverter with continuous input current, two dc inductors can be separated or coupled. When the two inductors are coupled as shown in Figure 4.4, the voltage across the inductor L_1 is reflected to the inductor L_2 through magnetic coupling. Then one of the two capacitors, for instance, C_2 can be removed from the circuit. The rearrangement of the circuit yields the structure as shown in Figure 4.5. Furthermore, the voltage across L_2 can be made proportional to the voltage across L_1 by changing the turns ratio n_2/n_1. As the voltage constraint associated with one of the capacitors is released, the two windings, to some extent, behave more like a flyback transformer rather than the original coupled inductors [143], except that the currents flow simultaneously through both windings in some of the operation states. Therefore, it is named as the voltage-fed trans-quasi-Z-source inverter (trans-qZSI).

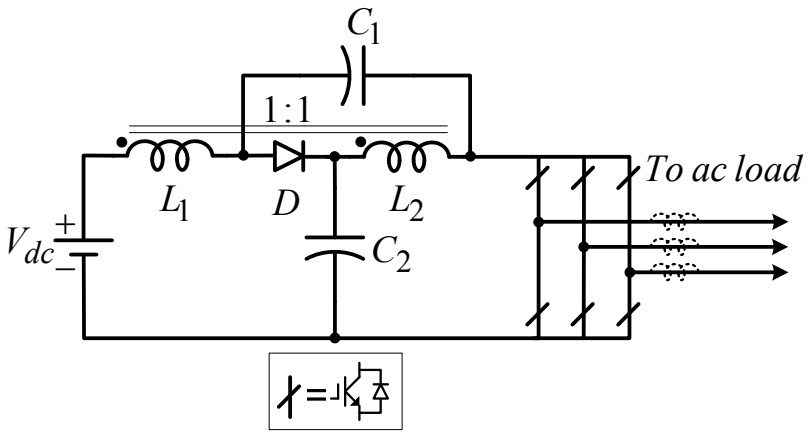


Figure 4.4. Voltage-fed quasi Z-source inverter with coupled inductors.

Like the Z-source inverter, the trans-quasi-Z-source inverter has an extra shoot-through zero state besides the six active states and two traditional zero states. The shoot-through zero state can be realized by short-circuiting both the upper and lower switching devices of any one phase leg, any two phase legs, or all three phase legs. The shoot-through zero state contributes to the unique buck-boost feature of the inverter. Otherwise, when the dc voltage is sufficient to produce the desirable ac output voltage, a traditional PWM without shoot-through zero state is used. For the purpose of analyzing the characteristics of the trans-Z-source inverters, this paper will focus on the two general continuous current modes as in the Z-source inverter: the shoot-through zero state and the non-shoot-through states [126, 144]. By replacing the two windings with an ideal transformer and a mutual inductance (L_m) (a model used in [145]), the overall equivalent circuit viewed from the inverter dc side can be obtained as shown in Figure 4.6(a).

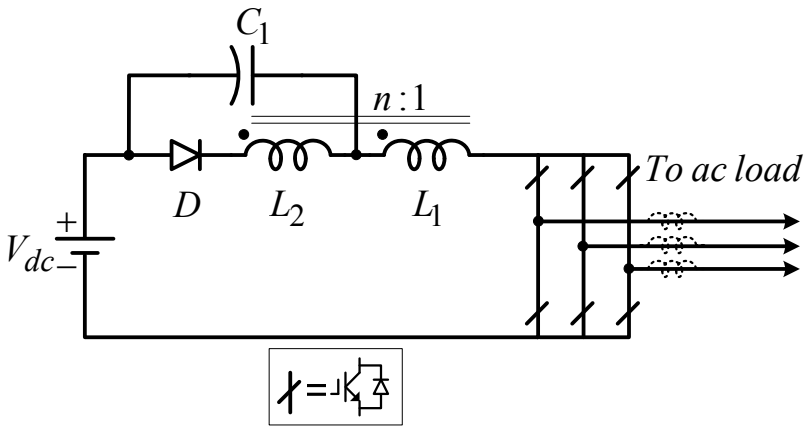


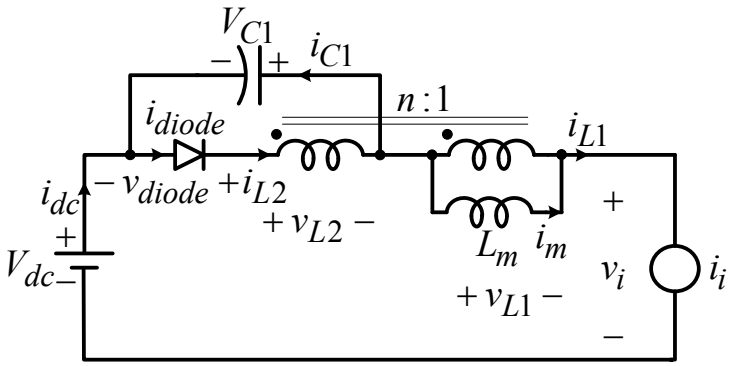
Figure 4.5. Voltage-fed trans-quasi-Z-source inverter.

In the shoot-through zero state, the inverter is equivalent to a short circuit as shown in Figure 4.6(b). Given that the inverter is in the shoot-through zero state for an interval of $D_{sh}T$ during a switching cycle, T, the voltages across L_1 and L_2 are:

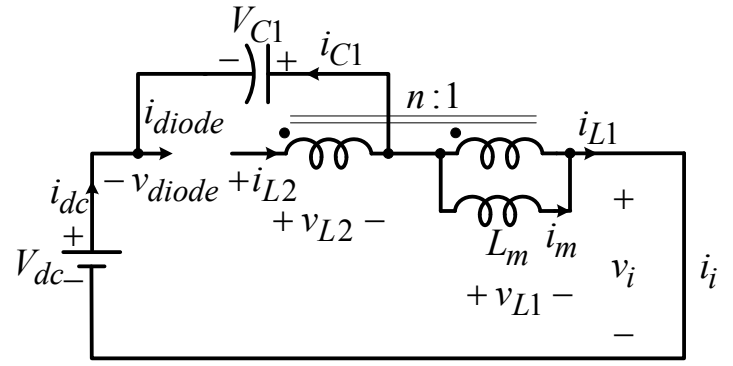
$$v_{L1} = V_{dc} + V_{C1} \tag{4.1}$$

$$v_{L2} = \frac{n_2}{n_1} v_{L1} \tag{4.2}$$

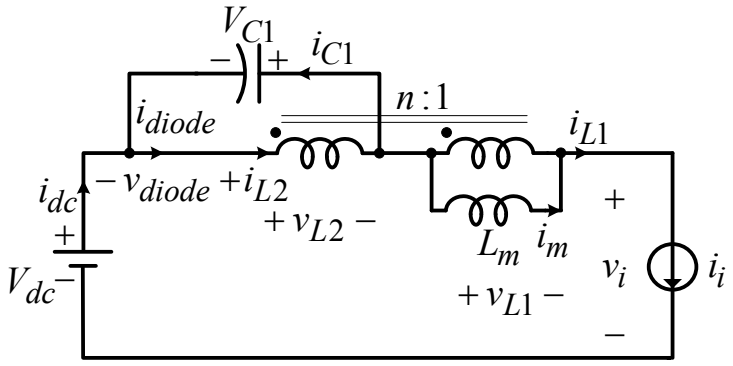
Thus, the diode is reversed biased. Note that the symbol D_{sh} is used here for shoot-through duty ratio in voltage-fed Z-source inverters.



(a) With the transformer equivalent circuit.



(b) Shoot-through zero states.



(c) Non-shoot-through states.

Figure 4.6. The equivalent circuits of the voltage-fed trans-qZSI viewed from the dc link.

In any of the non-shoot-through states for an interval of $(1—D_{sh})T$, the inverter bridge can be modeled as an equivalent current source as shown in Figure 4.6(c). The non-shoot-through

states include the six active states and two traditional zero states. For the traditional zero states, the current source has zero value (i.e. an open circuit). During one of the non-shoot-through states, one can get:

$$v_{L2} = -V_{C1} \tag{4.3}$$

$$v_{L1} = \frac{n_1}{n_2} v_{L2} = -\frac{n_1}{n_2} V_{C1} \tag{4.4}$$

The average voltage of both inductors should be zero over one switching period in the steady state. Thus, from (4.1) to (4.4), we have:

$$\langle v_{L1} \rangle = \frac{(V_{dc} + V_{C1}) D_{sh} T + (-\frac{n_1}{n_2} V_{C1})(1 - D_{sh}) T}{T} = 0 \tag{4.5}$$

From the above equation, the capacitor voltage can be calculated as:

$$V_{C1} = \frac{n \cdot D_{sh}}{1 - (1+n) D_{sh}} V_{dc} \tag{4.6}$$

where $n = n_2 / n_1 \geq 1$.

From (4.4) and (4.6), the dc link voltage across the bridge in the non-shoot-through states can be boosted to:

$$\hat{v}_i = \frac{1}{1 - (1+n) D_{sh}} V_{dc} = B V_{dc} \tag{4.7}$$

where the boost factor is:

$$B = \frac{1}{1 - (1+n) D_{sh}} \tag{4.8}$$

The peak value of the phase voltage from the inverter output is:

$$\hat{V}_{ph} = M \cdot \hat{V}_i / 2 = M \cdot B \cdot V_{dc} / 2 \tag{4.9}$$

where M is the modulation index.

When the constant boost control [131] is used, the voltage gain (MB) as defined in [130] is:

$$G = MB = \frac{M}{1-(1+n)(1-\frac{\sqrt{3}}{2}M)} \tag{4.10}$$

It can be seen that if the turns ratio is 1, the inverter dc link voltage boost gain is the same with that of the original Z-source/quasi Z-source inverters, but one capacitor is saved in the new trans-Z-source network. If the turns-ratio is over 1, the inverter dc link voltage boost gain can be higher given the same modulation index, M. In other words, it needs a smaller shoot-through duty ratio D_{sh} (accordingly a larger modulation index M) to produce the same ac output voltage than the Z-source/quasi Z-source inverters do. The voltage gain (MB) versus the modulation index for the voltage-fed trans-quasi-Z-source inverter (with a turns ratio n=2) is compared in Figure 4.7 with that for the Z-source/quasi Z-source inverters, using the constant boost control.

The voltage stress, V_s across the switching devices can be assessed by comparing its peak dc link voltage against the minimum dc voltage (GV_{dc}) [131] needed for the traditional VSI to produce the same ac output voltage at M=1. The ratio represents extra cost that the voltage-fed trans-quasi-Z-source inverter and Z-source/quasi Z-source inverters have to pay for the voltage boost in association with the higher voltage stress. The ratio of the voltage stress to the equivalent dc voltage for the trans-quasi-Z-source inverter is:

$$\frac{V_s}{GV_{dc}} = \frac{BV_{dc}}{GV_{dc}} = \frac{\sqrt{3}}{2}(1+\frac{1}{n}) - \frac{1}{n \cdot G} \tag{4.11}$$

When n=1, it is the same with the relative voltage stress in the Z-source inverter. When n>1,

as can be seen in Figure 4.8, the voltage-fed trans-Z-source inverter has less voltage stress across the inverter bridge for the same dc-ac output voltage gain. Hence, this circuit is beneficial to applications, in which a high voltage gain is required.

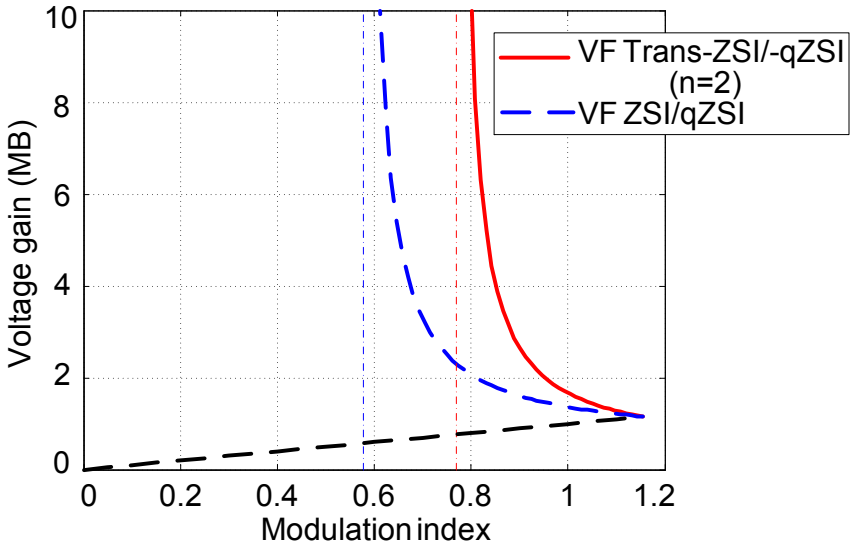


Figure 4.7. Voltage gain (*MB*) versus modulation index of the voltage-fed trans-ZSI/-qZSI (n=2) and ZSI/qZSI.

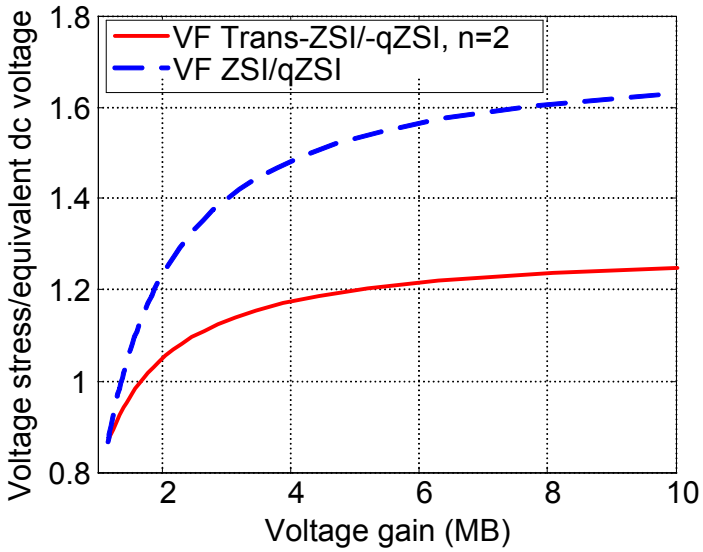


Figure 4.8. Active switch voltage stress of voltage-fed trans-ZSI/-qZSI (n=2) and ZSI/qZSI.

Similarly, another trans-Z-source inverter can be reconfigured as shown in Figure 4.9, if C_1

is removed in Figure 4.4 instead of C_2. This trans-Z-source inverter is the same as the T-source inverter proposed in [132]. It is obvious that it essentially has the same operation principle, voltage gain and voltage stress as the previously developed voltage-fed trans-quasi-Z-source inverter, except for different capacitor voltage stress and different input current drawn from the dc source. Therefore, Figure 4.4, Figure 4.5, and Figure 4.9 can be classified as a class of voltage-fed trans-Z-source inverters. In Figure 4.9, the capacitor voltage is:

$$V_{C1} = \frac{1 - D_{sh}}{1 - (1+n)D_{sh}} V_{dc} \tag{4.12}$$

When the turns-ratio, n of the trans-Z-source inverter in Figure 4.9 equals 1, (4.12) becomes the same equation for the capacitor voltage in the original Z-source inverter.

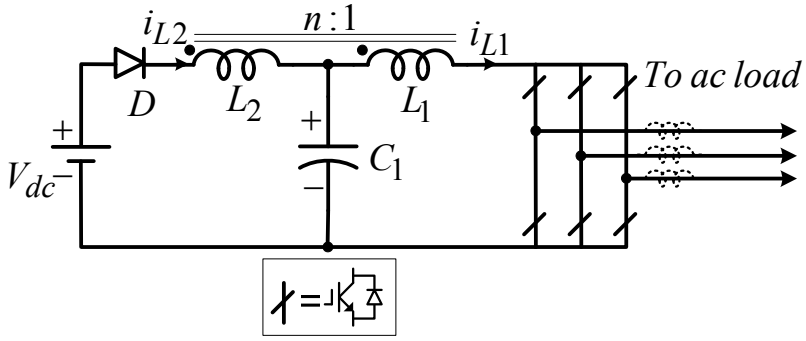


Figure 4.9. Voltage-fed trans-Z-source inverter.

4.3. The Current-fed Trans-Z-Source Inverters

Applying the similar concept to the current-fed Z-source and quasi Z-source inverters leads to the current-fed trans-Z-source and trans-quasi-Z-source inverters. The current-fed quasi Z-source inverter with continuous input current is shown in Figure 4.10, with inductors L_1 and L_2 coupled. The dc current source is provided by a dc inductor L_{dc}. Similarly, this circuit can be

further modified to a current-fed trans-quasi-Z-source inverter (trans-qZSI) as shown in Figure 4.11, where $n = n_2 / n_1 \geq 1$. The current-fed trans-quasi-Z-source inverters have two unique open zero states besides six active states and three traditional short-circuit (or shoot-through) zero states. The open zero states can be realized by turning off either all the upper switches or all the lower switches. The open zero states are forbidden in the conventional CSI. The new Z-source inverters, however, utilize the open zero state so that the inverter can step up and down the voltage.

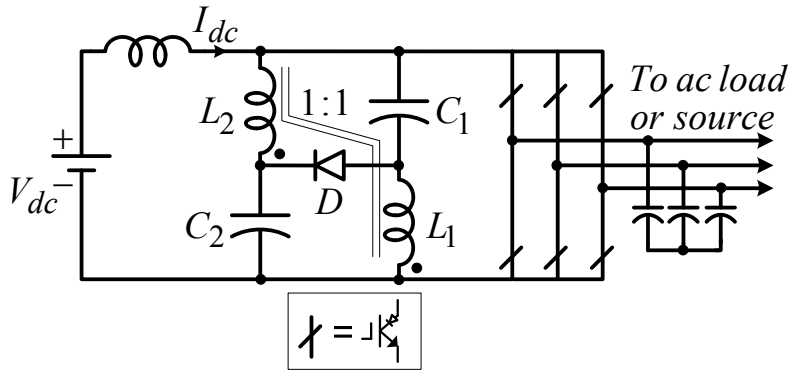


Figure 4.10. Current-fed quasi Z-source inverter with two inductors coupled.

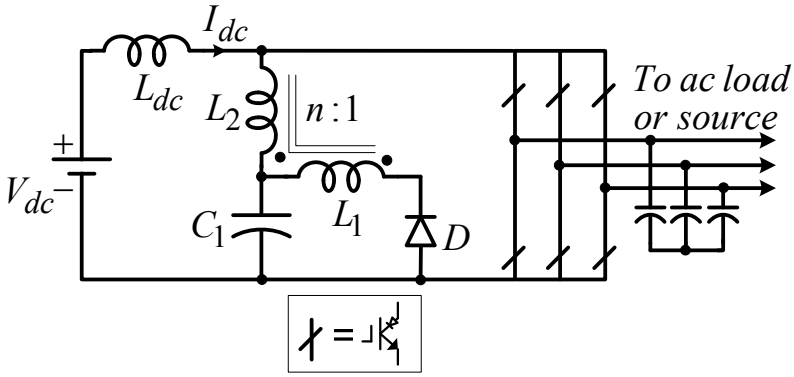
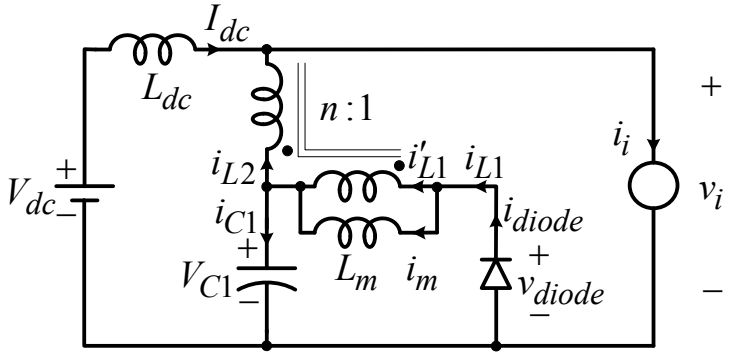


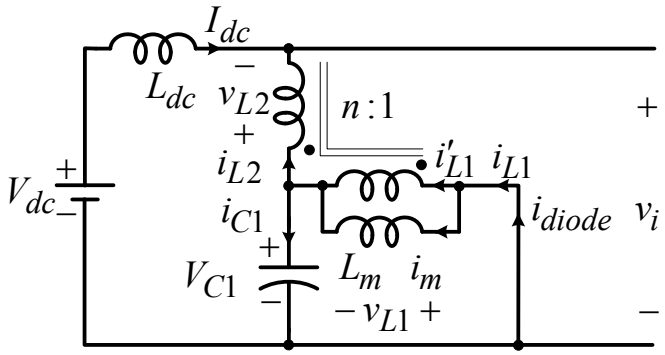
Figure 4.11. Current-fed trans-quasi-Z-source inverter.

Its equivalent circuit viewed from the inverter dc side is shown in Figure 4.12(a), assuming an ideal coupling for the transformer. When in an open zero state, the inverter bridge turns to an open circuit as shown in Figure 4.12(b). When in one of the non-open states (which includes the

traditional active states and short-circuit zero states), the inverter bridge can be modeled as an equivalent voltage source, v_i, as shown in Figure 4.12(c). The equivalent voltage source, v_i is the line-to-line voltage when in one of the six active states and is zero when in one of the short-circuit zero states.



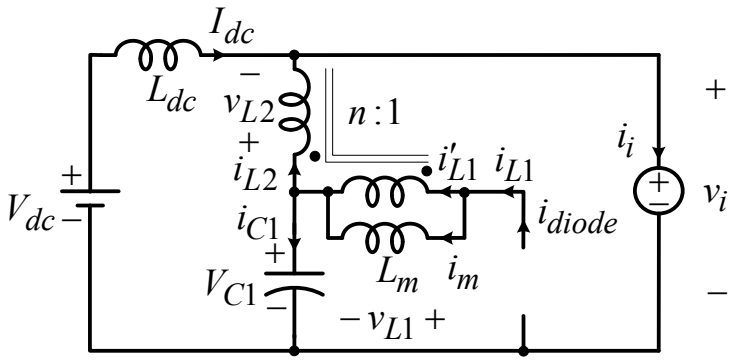
(a) With the transformer equivalent circuit.



(b) Open zero state.

Figure 4.12. The equivalent circuits of the current-fed trans-qZSI viewed from the dc link.

Figure 4.12 (cont'd)



(c) Non-open states.

Using the similar circuit analysis with the above voltage-fed trans-Z-source inverters, the following current relation and the dc-ac voltage gain can be obtained for the current-fed trans-Z-source inverters. According to the KCL and the relationship of the winding currents, the following relations hold:

$$i_{C1} = i_{L1} - i_{L2} \quad i_{L1} = i_m + i'_{L1} \quad i'_{L1} + ni_{L2} = 0 \tag{4.13}$$

In the open-zero states as shown in Figure 4.12(b) for a duration of $D_{op}T$, the diode is conducting to carry the current through L_1. From (4.13), the capacitor current can be expressed as

$$i_{C1} = (1+n)i_{dc} + i_m \tag{4.14}$$

In the non-open states for a duration of $(1-D_{op})T$, the diode D is biased off; no current flows through L_1. The capacitor current is

$$i_{C1} = -i_{L2} = -i_m / n \tag{4.15}$$

With the assumption that the inverter operates in the continuous current mode, given small

magnetizing current ripple and input current ripple, both i_m and i_{dc} can be approximated by their dc components I_m and I_{dc} respectively. Application of the amp-second balance to the capacitor yields

$$I_m = \frac{n(1+n)D_{op}I_{dc}}{1-(1+n)D_{op}} \tag{4.16}$$

Substituting I_m to the above expressions for the non-open states, the peak value of the current flowing through the inverter dc link can be obtained as

$$\hat{i}_i = \frac{1}{1-(1+n)D_{op}} I_{dc} = B \cdot I_{dc} \quad , \tag{4.17}$$

where B is the boost ratio in terms of current. Correspondingly, the ac voltage can be bucked (stepped down). Based on the operation principle of SPWM for the CSI, the maximum duty ratio of two active states in one switching period for each phase can be calculated by

$$D_{A\max} = \max\left\{\frac{M\sin\omega t}{2} - \frac{M\sin(\omega t - 2\pi/3)}{2}\right\} = \frac{\sqrt{3}}{2}M \tag{4.18}$$

where M is the modulation index based on the current reference.

Therefore, the peak value of the line current can be expressed as

$$\hat{i}_l = (\frac{\sqrt{3}}{2}M)\cdot\hat{i}_i \tag{4.19}$$

Assuming the energy conservation of the input and output, the peak value of the line-to-line voltage can be written as

$$\hat{v}_{ll} = \frac{V_{dc}\cdot I_{dc}}{\sqrt{3}\cdot(\hat{i}_l/\sqrt{2})\cdot\cos\varphi}\cdot\sqrt{2} = \frac{4\cdot V_{dc}[1-(1+n)D_{op}]}{3M\cos\varphi} \tag{4.20}$$

where $\cos\varphi$ is the power factor.

Similar to the voltage-fed ZSI, there are corresponding control methods: simple boost, maximum boost and constant boost controls in terms of current (or buck in terms of voltage) for the current-fed Z-source inverters. The constant current boost is used here to compare the operation region of the current-fed trans-ZSIs and current-fed ZSIs. In order to keep the active state unchanged, the maximum available open zero duty ratio is:

$$D_{op\max} = 1 - D_{A\max} = 1 - \frac{\sqrt{3}}{2}M \tag{4.21}$$

Hence, (4.20) can be rewritten as

$$\hat{v}_{ll} = \frac{4 \cdot V_{dc}[(1+n)(\frac{\sqrt{3}}{2}M - 1) + 1]}{3M\cos\varphi} \tag{4.22}$$

When n=1, (4.20) and (4.22) can be proven to be the same as in the Z-source and quasi-Z-source inverters. The ratios of the peak line-to-line voltage to the input voltage as a function of the modulation index are compared in Figure 4.13(a) and (b) for (quasi-)Z-source and trans-(quasi-)Z-source inverters, where n equals 2 for the trans-Z-source inverters. The blue dash line is the minimum voltage envelope for the buck mode and the regeneration mode, with the constant current boost control. The shaded areas are operable regions with only one additional diode, D in Figure 4.10 and Figure 4.11. When no open state is employed (that is, D_{op} = 0), the red envelop line in Figure 4.13(a) and (b) that can be obtained from (4.20) depicts the maximum voltage boost gain for both the current-fed (quasi-)Z-source inverters and the trans-quasi-Z-source inverters. It is noticeable that, however, the trans-Z-source has a wider boost range in the motoring operation mode. In the current-fed quasi Z-source inverter [140], the dc link voltage v_i cannot exceed the sum of capacitor voltages, because the diode will otherwise improperly

conduct in the active states and cause waveform distortion. For the same reason, in the trans-quasi-Z-source inverters, to maintain the diode reversed biased in the active state, the voltage across it should satisfy

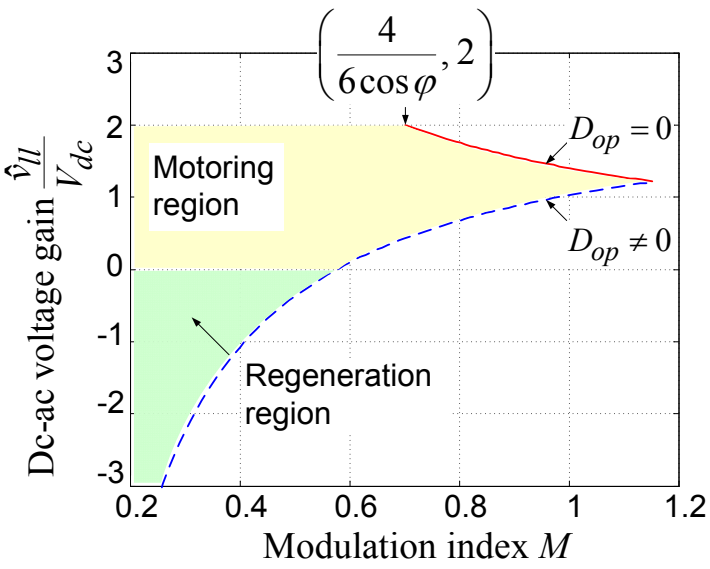
$$v_{diode} = \frac{1}{n}(V_{C1} - v_i) + V_{C1} = (1 + \frac{1}{n})V_{dc} - \frac{1}{n}v_i \geq 0 \tag{4.23}$$

Hence, the peak value of the line-to-line voltage is constrained to

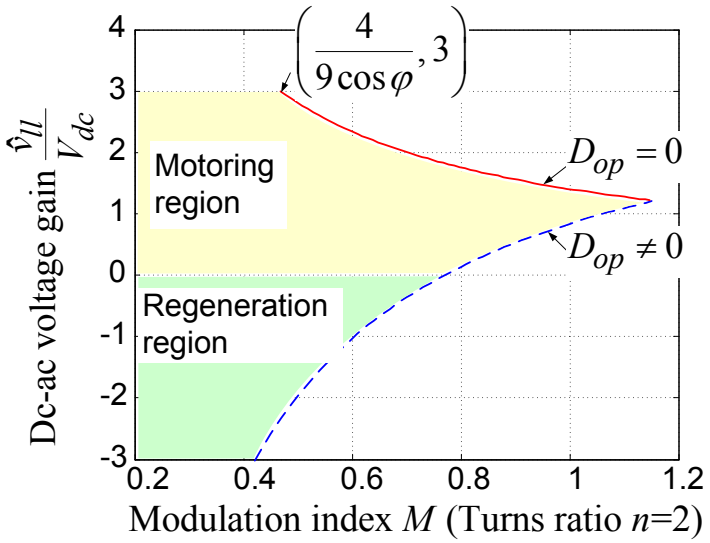
$$\hat{v}_i = \hat{v}_{ll} = \frac{4 \cdot V_{dc}}{3M \cos\varphi} \leq (1+n)V_{dc} \tag{4.24}$$

It implies that the minimum modulation index is related to the power factor seen from the inverter bridge. When n>1, the peak line-to-line voltage can reach $(n+1)V_{dc}$, as shown in Figure 4.13(b). Note that the dc-ac voltage gain can also be analyzed by calculating the voltage relation and active duty ratio in the same way as in [140], where the active and short-circuit zero states are depicted separately.

Similarly, a current-fed trans-Z-source inverter (trans-ZSI) can be derived as shown in Figure 4.14. It has the same operation principle, voltage gain and operation regions as the trans-quasi-Z-source inverter, but with different current stress, which will be discussed in the next section.



(a) The current-fed ZSI/qZSI.



(b) The current-fed trans-ZSI/-qZSI.

Figure 4.13. Dc-ac voltage gain and operation region in the current-fed ZSI/qZSI and trans-ZSI/-qZSI.

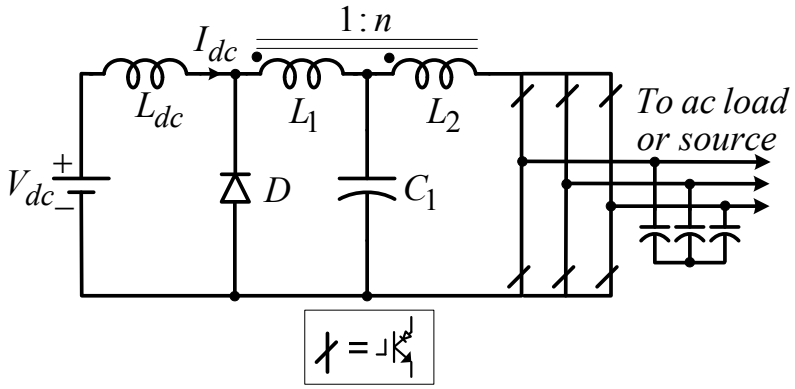


Figure 4.14. Current-fed trans-Z-source inverter.

4.4. Comparison with the Z-Source and Quasi Z-Source Inverters

Table 4.1 compares the governing equations for the voltage-fed trans-Z-source, trans-quasi-Z-source, Z-source and quasi Z-source inverters. Table 4.2 compares the class of current-fed Z-source inverters. Two tables also provide a guideline for determining the ratings of the components such as the active switch, the diode, the capacitor and the transformer. The voltage and current directions in the Z-source and quasi Z-source inverters follow the same definition as that shown in the equivalent circuits of the trans-Z-source and trans-quasi-Z-source inverters. All the magnetizing current is reflected to the primary winding. While S_D is the shoot-through switching function in the voltage-fed inverters, it is the open-circuit switching function in the current-fed inverters due to the duality between the voltage-fed and current-fed inverters. S_D is defined as 1 when the inverter is in the shoot-through zero states and 0 when it is in the non-shoot-through states in the voltage-fed inverters. It is 1 for the open zero states and 0 for the non-open states in the current-fed inverters.

In Table 4.1, when the turns-ratio is over 1, the voltage-fed trans-Z-source and trans-quasi-

Z-source inverters, with reduced component count, have higher dc link voltage gain than the voltage-fed Z-source and quasi Z-source inverters. When the turns-ratio is 1, some of the governing equations can be unified, including the relation for the magnetizing current of the two coupled windings. Comparing the voltage-fed trans-Z-source and trans-quasi-Z-source inverters, less capacitance is needed for an input filter capacitor in parallel with the low voltage dc source in the voltage-fed trans-Z-source inverter, whereas the capacitor voltage stress is reduced in the voltage-fed trans-quasi-Z-source inverter.

In Table 4.2, when the turns-ratio is over 1, besides a wider motoring operating range, the current-fed trans-Z-source and trans-quasi-Z-source inverters feature more voltage buck ratio. This feature can also be found in Figure 4.13. When the turns-ratio is 1, some of the governing equations in the Z-source inverter and quasi Z-source inverter are consistent with those for the trans-Z-source inverter and trans-quasi-Z-source inverter, respectively. Similarly as the Z-source and quasi Z-source inverters and as shown in Figure 4.15, the trans-quasi-Z-source inverter has less magnetizing current than the trans-Z-source inverter in the motoring operation (I_m>0) when the open zero duty ratio D_{op} is: 0<D_{op}<1/(n+1). However, the trans-Z-source inverter has less magnetizing current (absolute value) than the trans-quasi-Z-source inverter does in the regeneration operation (I_m<0) when the open zero duty ratio D_{op} is: 1/(n+1)<D_{op}<1.

Admittedly, as can be seen from Table 4.1, the new voltage-fed trans-Z-source inverters mitigate the switch stress while transferring the stress to the less costly passive device, the diode. Therefore, the boost ratio also cannot avoid its practical limit, although it is an improvement on the boost ratio to some extend from the voltage-fed Z-source inverters. Besides, from the inductor currents in Table 4.1 and Table 4.2, very high power transformer is difficult to

implement. Since the transformer has some characteristics like the transformer in the flyback dc-dc converter, the transformer should be designed with low leakage inductance. Similarly to the flyback dc-dc converter, the low component count is an attractive figure of merit that makes the trans-Z-source inverters suitable for low to medium power applications.

Table 4.1. Comparison of the voltage-fed Trans-ZSI/-qZSI and ZSI/qZSI

	VF trans-ZSI	VF trans-qZSI	VF ZSI with coupled inductors (CL)	VF qZSI with continuous input current and CL
Dc-link voltage v_i	$\bar{S}_D \cdot \frac{V_{dc}}{1-(1+n)D_{sh}}$	$\bar{S}_D \cdot \frac{V_{dc}}{1-(1+n)D_{sh}}$	$\bar{S}_D \cdot \frac{V_{dc}}{1-2D_{sh}}$	$\bar{S}_D \cdot \frac{V_{dc}}{1-2D_{sh}}$
Diode voltage v_{diode}	$S_D \cdot \frac{nV_{dc}}{1-(1+n)D_{sh}}$	$S_D \cdot \frac{nV_{dc}}{1-(1+n)D_{sh}}$	$S_D \cdot \frac{V_{dc}}{1-2D_{sh}}$	$S_D \cdot \frac{V_{dc}}{1-2D_{sh}}$
Capacitor voltage V_{C1}	$\frac{1-D_{sh}}{1-(1+n)D_{sh}}V_{dc}$	$\frac{n \cdot D_{sh}}{1-(1+n)D_{sh}}V_{dc}$	$\frac{1-D_{sh}}{1-2D_{sh}}V_{dc}$	$\frac{D_{sh}}{1-2D_{sh}}V_{dc}$
Capacitor voltage V_{C2}	Not applicable	Not applicable	$\frac{1-D_{sh}}{1-2D_{sh}}V_{dc}$	$\frac{1-D_{sh}}{1-2D_{sh}}V_{dc}$
Magnetizing current i_m	$(1+n)\frac{P}{V_{dc}}$ with ripple	$(1+n)\frac{P}{V_{dc}}$ with ripple	$\frac{2P}{V_{dc}}$ with ripple	$\frac{2P}{V_{dc}}$ with ripple
Inductor current i_{L1}	$\bar{S}_D \cdot i_i + S_D \cdot i_m$	$\bar{S}_D \cdot i_i + S_D \cdot i_m$	$\frac{P}{V_{dc}}$ with ripple	$\frac{P}{V_{dc}}$ with ripple
Inductor current i_{L2}	$\bar{S}_D \cdot (i_m - i_i)/n$	$\bar{S}_D \cdot (i_m - i_i)/n$	$\frac{P}{V_{dc}}$ with ripple	$\frac{P}{V_{dc}}$ with ripple
Input current i_{dc}	The same as i_{L2}	The same as i_{L1}	$\bar{S}_D \cdot (2i_{L1} - i_i)$	The same as i_{L1}
Diode current i_{diode}	The same as i_{L2}	The same as i_{L2}	$\bar{S}_D \cdot (2i_{L1} - i_i)$	$\bar{S}_D \cdot (2i_{L1} - i_i)$
Capacitor current i_{C1} (and i_{C2} for ZSI/qZSI)	$i_{L2} - i_{L1}$	$i_{L2} - i_{L1}$	$\bar{S}_D \cdot (\frac{P}{V_{dc}} - i_i)$ $+S_D \cdot (-\frac{P}{V_{dc}})$	$\bar{S}_D \cdot (\frac{P}{V_{dc}} - i_i)$ $+S_D \cdot (-\frac{P}{V_{dc}})$

Table 4.2. Comparison of the current-fed Trans-ZSI/-qZSI and ZSI/qZSI

	CF trans-ZSI	CF trans-qZSI	CF ZSI with L_1 and L_2 coupled	CF qZSI with continuous input current and L_1 and L_2 coupled
Peak line-to line voltage $\hat{v}_{ll}$	$\frac{4V_{dc}[1-(1+n)D_{op}]}{3M\cos\varphi}$	$\frac{4V_{dc}[1-(1+n)D_{op}]}{3M\cos\varphi}$	$\frac{4V_{dc}\left(1-2D_{op}\right)}{3M\cos\varphi}$	$\frac{4V_{dc}\left(1-2D_{op}\right)}{3M\cos\varphi}$
Diode voltage v_{diode}	$(1+\frac{1}{n})V_{dc}-\frac{1}{n}v_i \geq 0$	$(1+\frac{1}{n})V_{dc}-\frac{1}{n}v_i \geq 0$	$2V_{dc}-v_i \geq 0$	$2V_{dc}-v_i \geq 0$
Capacitor voltage V_{C1} (and V_{C2} for ZSI/qZSI)	V_{dc}	V_{dc}	V_{dc}	V_{dc}
Input current I_{dc}	$\frac{P}{V_{dc}}$	$\frac{P}{V_{dc}}$	$\frac{P}{V_{dc}}$	$\frac{P}{V_{dc}}$
Magnetizing current i_m	$\frac{(1+n)(1-D_{op})}{1-(1+n)D_{op}}I_{dc}$ with ripple	$\frac{n(1+n)D_{op}}{1-(1+n)D_{op}}I_{dc}$ with ripple	$\frac{2(1-D_{op})}{1-2D_{op}}I_{dc}$ with ripple	$\frac{2D_{op}}{1-2D_{op}}I_{dc}$ with ripple
Inductor current i_{L1}	$\overline{S}_D \cdot I_{dc} + S_D \cdot i_m$	$S_D \cdot \frac{nI_{dc}}{1-(1+n)D_{op}}$	$\frac{1-D_{op}}{1-2D_{op}}I_{dc}$ with ripple	$\frac{D_{op}}{1-2D_{op}}I_{dc}$ with ripple
Inductor current i_{L2}	$\overline{S}_D \cdot \frac{I_{dc}}{1-(1+n)D_{op}}$	$\overline{S}_D \cdot i_m / n$ $+S_D \cdot (-I_{dc})$	$\frac{1-D_{op}}{1-2D_{op}}I_{dc}$ with ripple	$\frac{D_{op}}{1-2D_{op}}I_{dc}$ with ripple
Diode current i_{diode}	$S_D \cdot \frac{nI_{dc}}{1-(1+n)D_{op}}$	$S_D \cdot \frac{nI_{dc}}{1-(1+n)D_{op}}$	$S_D \cdot \frac{I_{dc}}{1-2D_{op}}$	$S_D \cdot \frac{I_{dc}}{1-2D_{op}}$
Capacitor current i_{C1}, i_{C2}	$i_{L1}-i_{L2}$	$i_{L1}-i_{L2}$	$\overline{S}_D \cdot (I_{dc}-i_{L1})$ $+S_D \cdot i_{L1}$	$\overline{S}_D \cdot (-i_{L1})+$ $S_D \cdot (I_{dc}+i_{L1})$

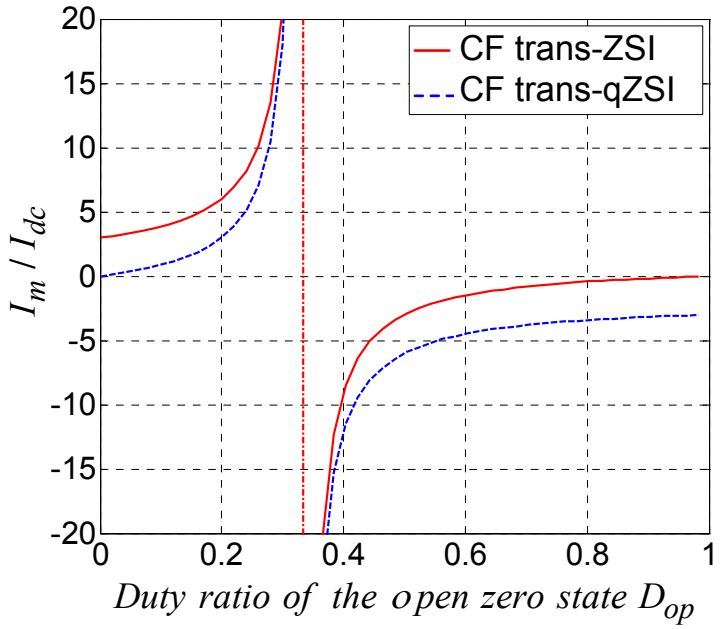


Figure 4.15 Comparison of normalized magnetizing currents in trans-ZSI and trans-qZSI.

4.5. Simulation and Experimental Results

Two prototypes for the voltage-fed trans-quasi-Z-source and current-fed trans-quasi-Z-source inverters were built to validate the analysis. The system configuration for the simulation and experiments of the voltage-fed trans-quasi-Z-source inverter is shown in Figure 4.16. The switching frequency for the SPWM is 10 kHz. The capacitance of C_1 is 400 μF. The transformer consists of two bifilar windings. The turns-ratio n_2/n_1 is 2:1. The magnetic inductance measured from the primary side is 207 μH. There is no snubber circuit for the inverter bridge, thanks to the very low the leakage inductance (around 100 nH mainly from the outside connection) and the parasitic capacitance in the tightly coupled bifilar windings. The parasitic capacitance lowers the dv/dt and more interestingly increases the effective boost ratio. That is because the inductor L_1 is still charged during the IGBT turn-off transition until the dc link voltage increases and the diode

then becomes forward-biased. However, it is still able to achieve the desired dc voltage boost ratio by controlling the shoot-though duty ratio. The simulation and experiment results of the boost mode operation are shown in Figure 4.17 and Figure 4.18 respectively. The output line-to-line voltage is boosted to 208 V RMS (or 294 V peak) with an input voltage of 130 V. The constant boost control is used, with the shoot-through duty ratio 0.2 and the modulation index 0.93. Both the input voltage and the voltage stress are lower than the reported results of Z-source inverter in [131] to produce the same output voltage. Besides, no significant voltage overshoot (less than 20%) was observed in the dc link voltage, due to tight coupling between the primary and secondary. The capacitor voltage of 152 V demonstrates the low capacitor voltage requirement in the voltage-fed trans-quasi-Z-source inverter. The simulation and experiment results are shown in Figure 4.19 and Figure 4.20 for the operation without boost, like the traditional voltage source inverters. It needs a dc input voltage of 339 V to output the same ac output voltage.

The new feature of the current-fed trans-Z-source inverters is demonstrated by the simulation and experiments of a trans-quasi-Z-source inverter. The configuration is shown in Figure 4.21. The inverter bridge is built with a RB-IGBT package from Fuji. The dc input inductor, L_{dc} is 1 mH. The magnetic inductance of the transformer is 207 μH from the primary side. The capacitance of C_1 in the impedance-source network is 100 μF. The three-phase ac outputs are loaded with three 10 Ω resistive loads in a Y-connection. Each ac filter capacitor is just 40 μF in a Δ-connection. The resultant power factor is 0.911. The switching frequency is 10 kHz. Figure 4.22 and Figure 4.23 compare the simulation and experimental results for a modulation index of 0.6, without open zero states. Figure 4.22(a) and Figure 4.23(a) show the input and output voltages/ currents, the output line-to-line voltages are 172 V RMS (243 V peak)

with an input voltage of 100 V and thus the ratio $\hat{v}_{ll} / V_{dc}$ is 2.43 times, which agree with the theoretical calculation. With this power factor, the original current-fed quasi Z-source inverter [140] can not exceed a voltage ratio of 2. Figure 4.22(b) and Figure 4.23(b) show the capacitor voltage V_{C1}, and voltages for the diode and the inverter bridge. Thus the average winding current can be inferred as being equal to zero from the capacitor voltage under this condition. The minimum diode voltage is more clearly zoomed in as shown in Figure 4.22(c) and Figure 4.23(c). As can be seen, the diode is reversed biased over the entire fundamental cycle. In sum, both the simulation and experimental results verify the extended motoring operating range of the current-fed trans-quasi-Z-source inverter.

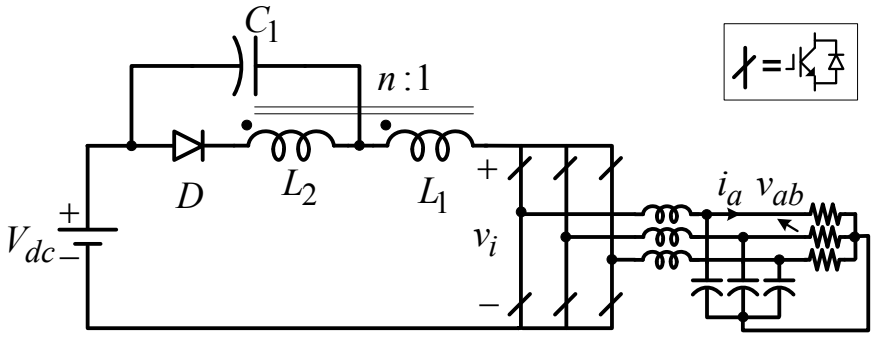
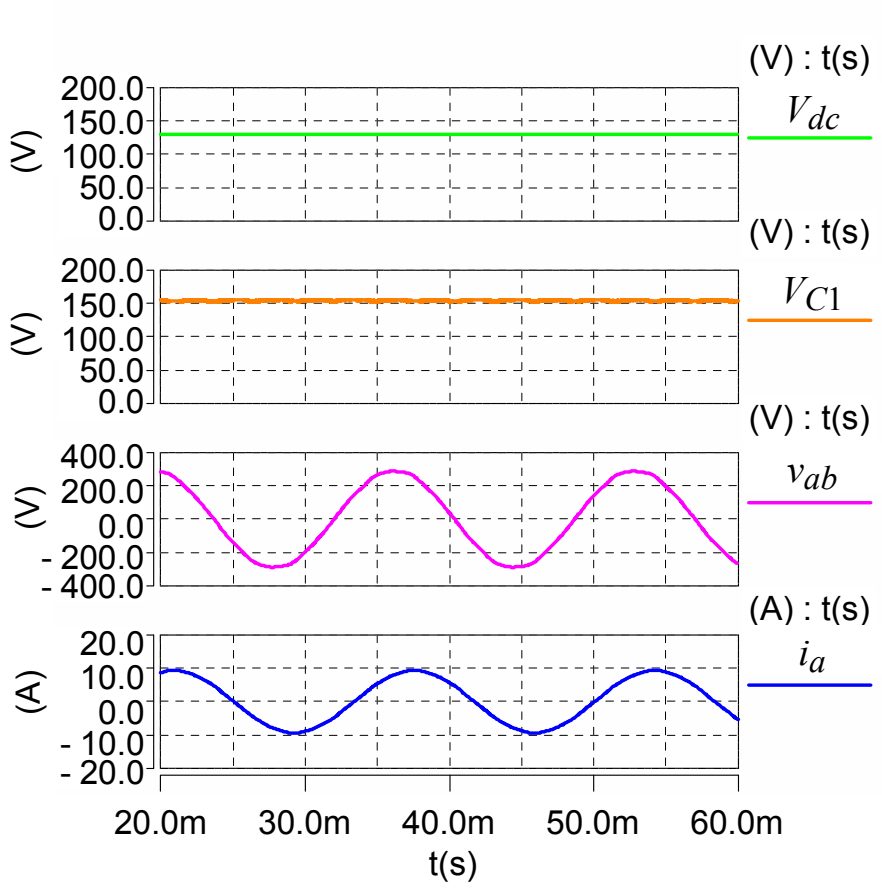
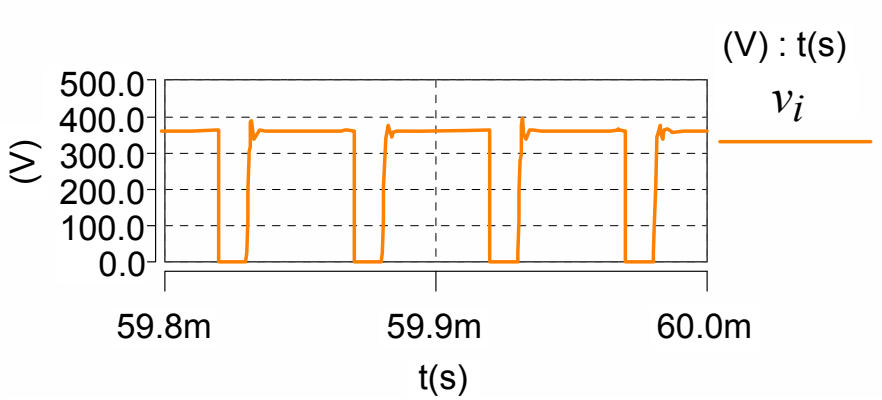


Figure 4.16. Simulation and experimental system configuration of the voltage-fed trans-qZSI.

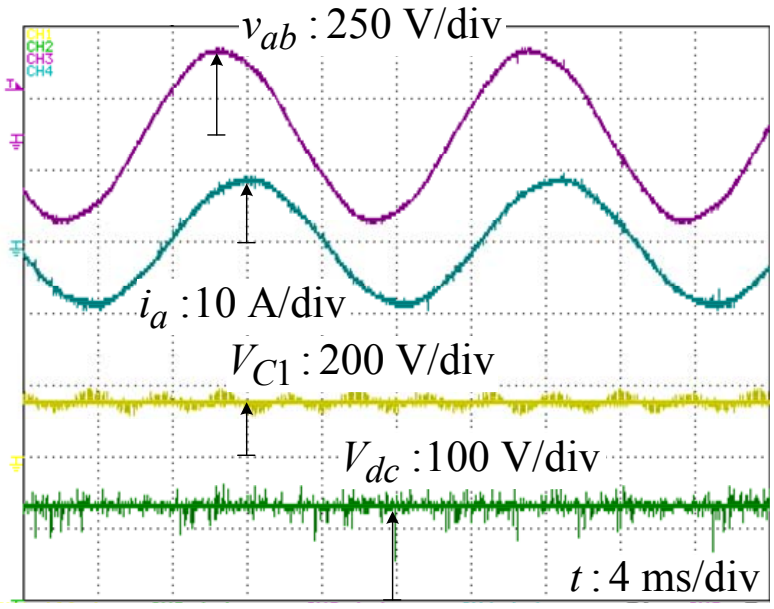


(a) Input and capacitor voltages and output voltage/current.

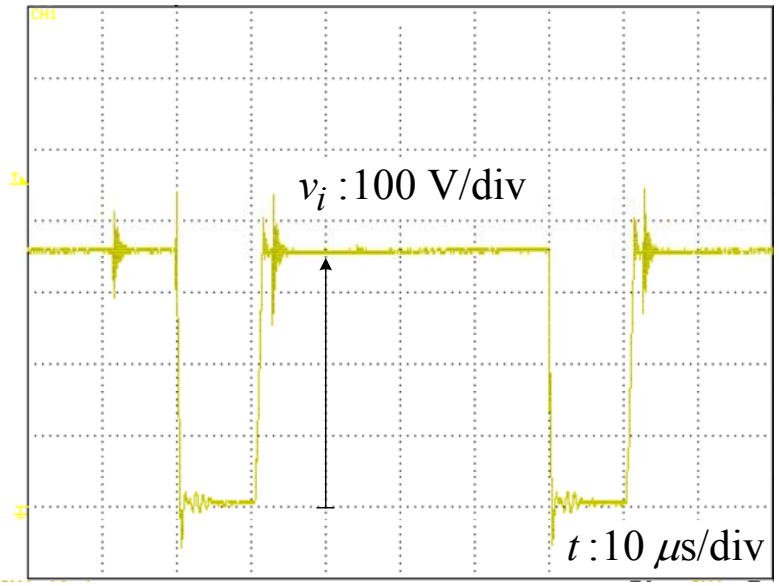


(b) The inverter dc link voltage.

Figure 4.17. Simulation results of the voltage-fed trans-qZSI considering the parasitic capacitance of the bifilar winding (constant boost control, M=0.93, D_{sh}=0.2).



(a) Input and capacitor voltages and output voltage/current.



(b) The inverter dc link voltage.

Figure 4.18. Experimental waveforms of the voltage-fed trans-qZSI (constant boost control, M=0.93, D_{sh}=0.2).

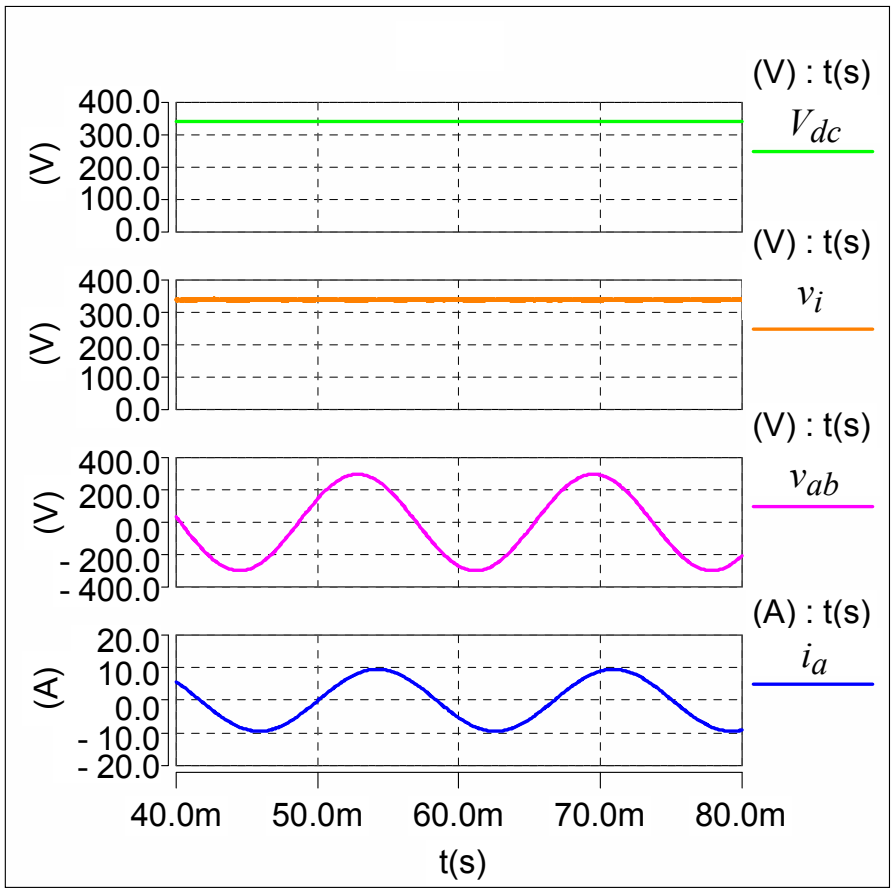


Figure 4.19. Simulation results of the voltage-fed trans-qZSI without boost (M=1).

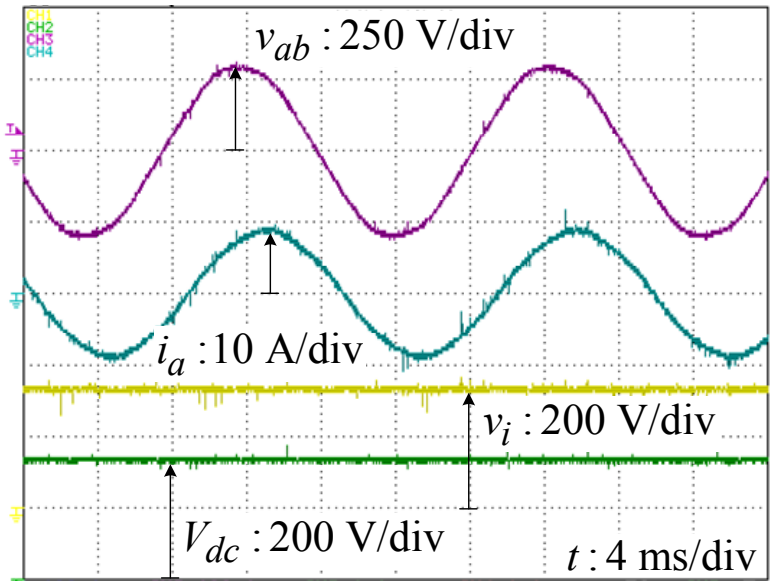


Figure 4.20. Experimental waveforms of the voltage-fed trans-qZSI without boost (M=1).

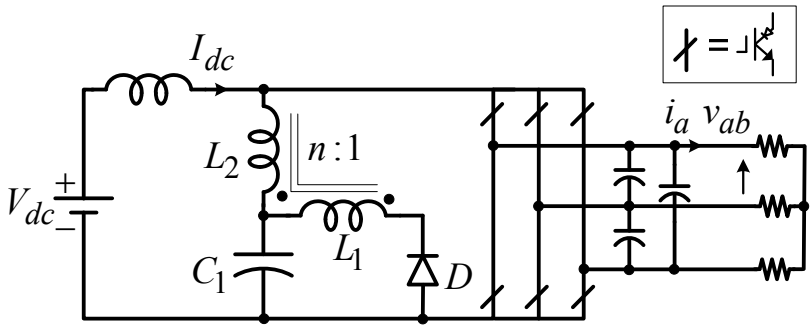
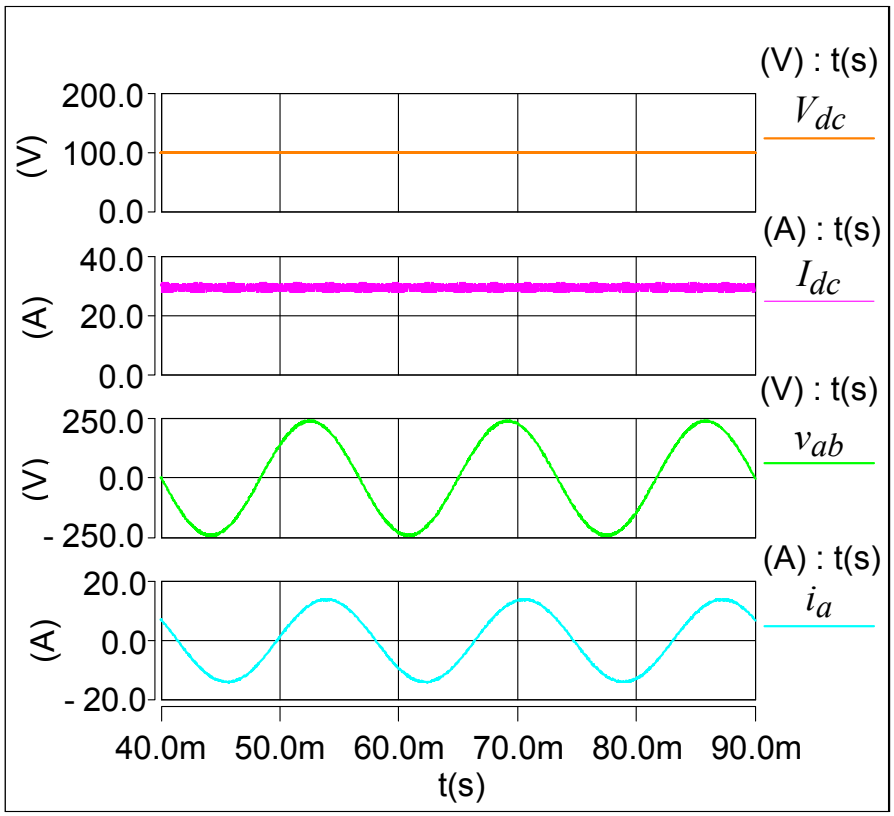


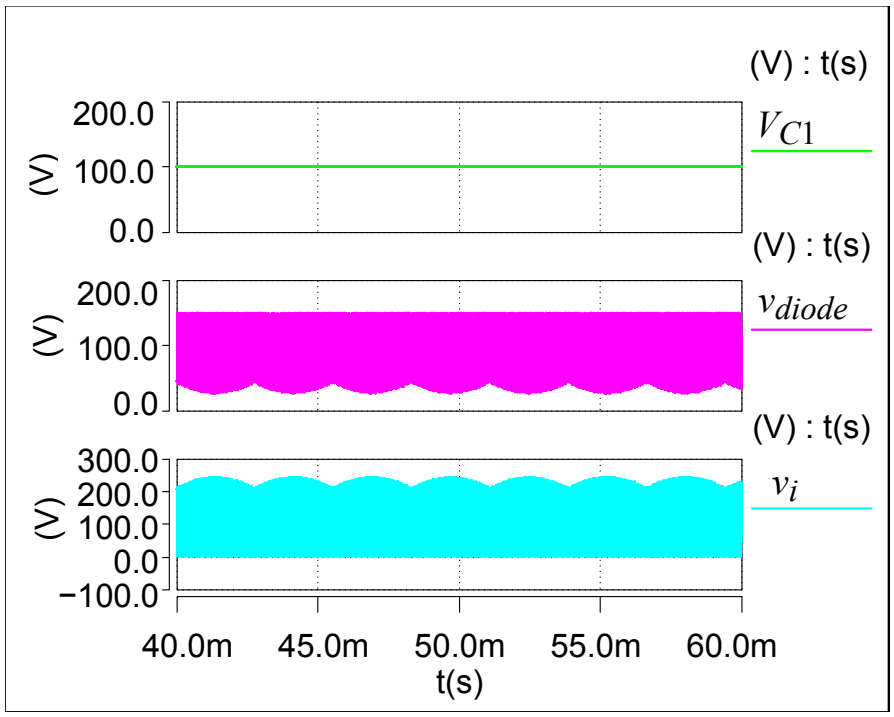
Figure 4.21. Simulation and experimental system configuration of the current-fed trans-qZSI.



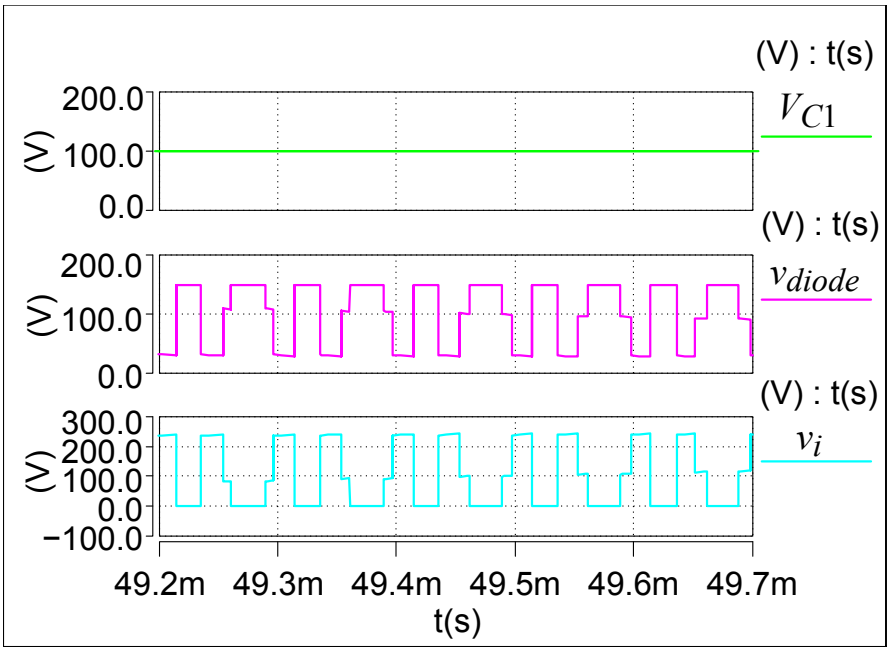
(a) Input and output voltage/current.

Figure 4.22 Simulation results of the current-fed trans-qZSI (M=0.6).

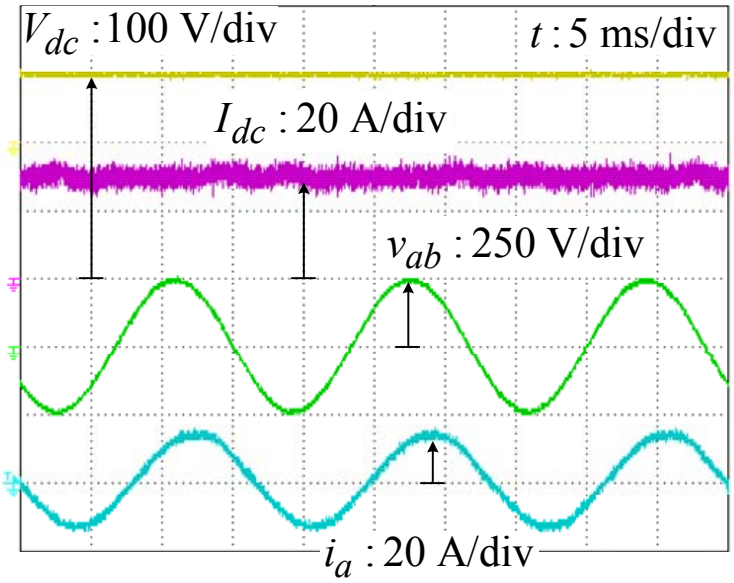
Figure 4.22 (cont'd)



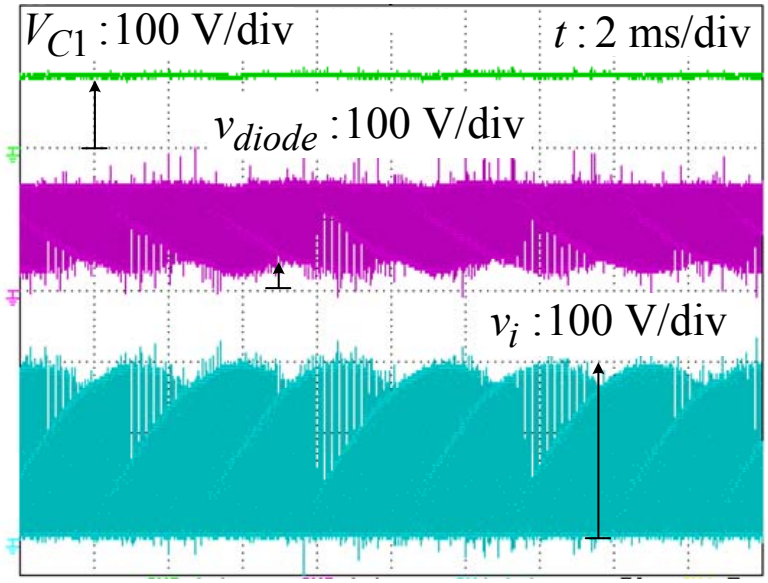
(b) Capacitor, diode and inverter bridge voltages.



(c) Zoom-in of capacitor, diode and inverter bridge voltage.



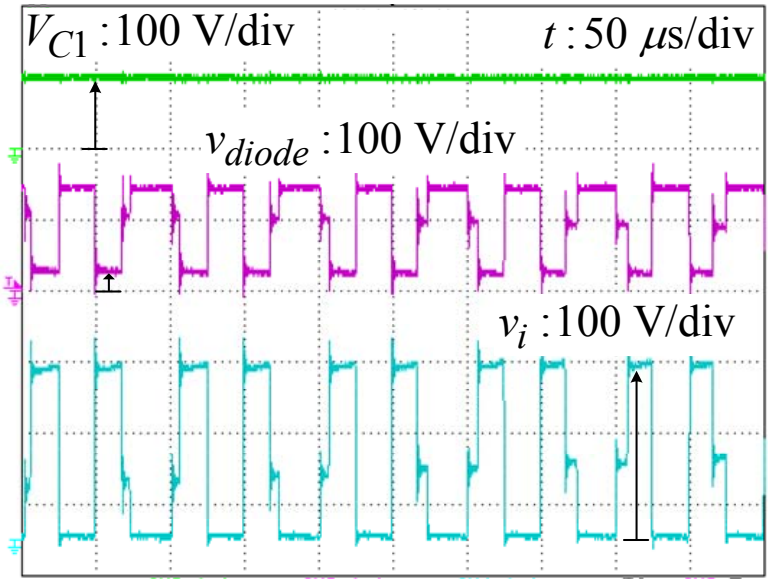
(a) Input and output voltage/current.



(b) Capacitor, diode and inverter bridge voltages.

Figure 4.23. Experimental waveforms of the current-fed trans-qZSI (M=0.6).

Figure 4.23 (cont'd)



(c) Zoom-in of capacitor, diode and inverter bridge voltage.

4.6. Application Examples

The voltage-fed trans-ZSIs can be applied in PV or FC dc-ac power conversions. One instance is shown in Figure 4.24 for a PV micro inverter. Unlike a centralized PV converter that is fed by the entire array of serially connected PV panels, a micro inverter directly interfaces a single PV panel with the ac bus. As mentioned in Chapter 3, an NX dc-dc converter in one micro inverter is suitable for high-gain voltage boosting. A voltage-fed trans-ZSI undertakes the dc-ac inversion and output regulation. It is capable of boosting the voltage to some extent, which facilitates the design of the NX dc-dc converter.

The current-fed trans-ZSIs are suitable for PHEVs. First, they have sinusoidal voltage and current to directly couple the motor/generator and the battery, as illustrated in Figure 4.25. The traditional voltage source inverters in the PHEVs present pulse voltage to the motor/generator as depicted in Figure 4.26. Voltage surges resulting from these rapid voltage transitions can cause

motor insulation degradation, bearing failure due to erosion caused by the resulting shaft leakage current, electromagnetic interference, and acoustic noise in the motor [146, 147]. Second, the current-fed trans-ZSIs accomplish bi-directional power flow and voltage buck-boost by the fewest switching devices (only one extra diode and six RB-IGBTs). Besides to that, they can have direct connection to the grid. Thus, it makes possible to save an additional on-board charger for single-phase 120-V and three-phase 220-V power.

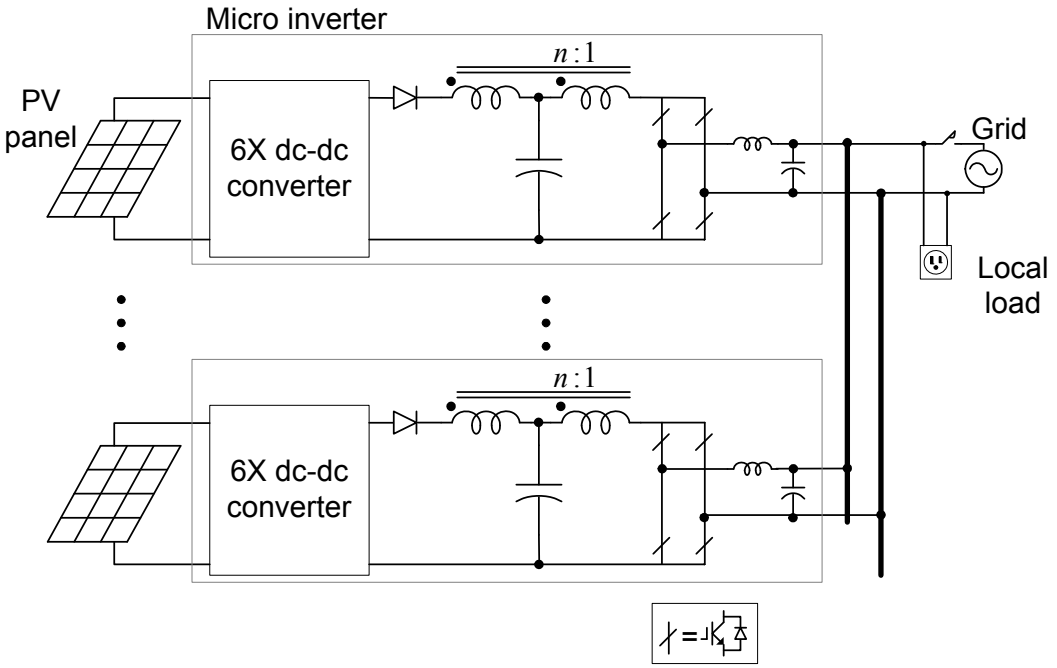


Figure 4.24. An example of PV micro inverter using NX dc-dc converter plus trans-ZSI.

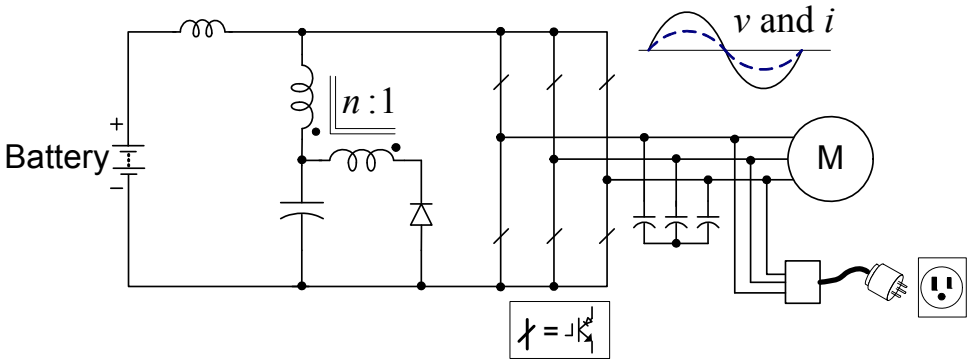


Figure 4.25. An example of the current-fed trans-qZSI for PHEV.

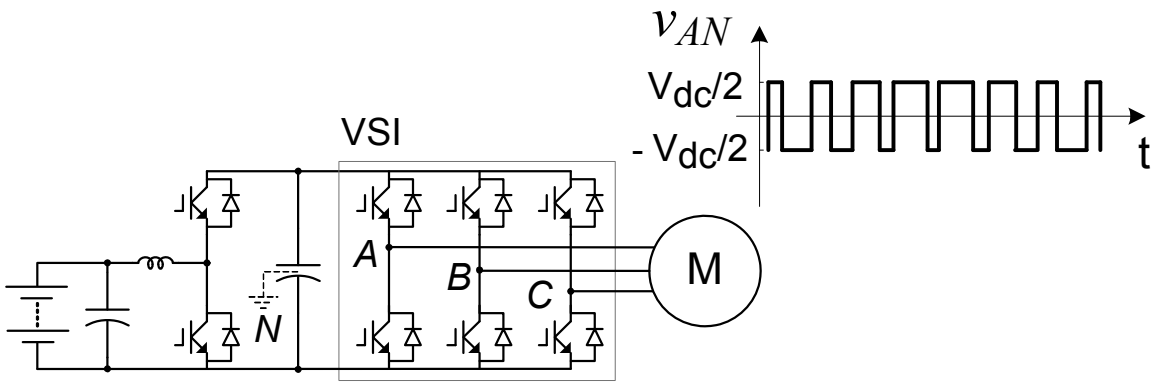


Figure 4.26. Voltage source inverter in HEV traction drives producing pulse voltage

4.7. Summary

A class of trans-Z-source inverters has been presented for voltage-fed and current-fed dc-ac inversion systems. When the turns-ratio of the two windings is over 1, the voltage-fed trans-Z-source inverter can obtain a higher boost gain with the same shoot-through duty ratio and modulation index, compared with the original Z-source inverter; the current-fed trans-Z-source-inverter can extend the motoring operation range to more than that can be achieved in the original Z-source and quasi Z-source inverters. With new unique features, they can broaden applications of the Z-source inverters. For instance, the voltage-fed trans-Z-source inverters provide a promising potential in the applications with very low input voltage, such as the micro inverter for the photovoltaic systems. Simulation and experimental results of the voltage-fed trans-quasi-Z-source and the current-fed trans-quasi-Z-source inverters have verified the analysis and feature.

Chapter 5 Balance and Long-life Operation of Battery Cells

5.1. Introduction

While the previous chapters have introduced the converters/inverters interfacing the energy storage systems at module level, this chapter will look into the power electronics circuits for one of the important energy storage devices, the rechargeable batteries at the cell level. Among a variety of battery energy storage systems, the high-power battery packs in HEVs and EVs face more problems and challenges than the low-power battery packs. The techniques and cost of batteries are deemed the bottleneck for the commercial development of PHEVs, never mention for EVs. Currently, a Li-ion battery pack up to 16 kWhr is nearly equal to the cost of the rest of the vehicle [77]. It would be superior if a battery did not have to be replaced in the life of the vehicle. Is it possible? What is the story behind a worn-out battery pack?

In HEVs, battery cells are normally connected in series for sufficient voltage. The serial cells inevitably have inherent diversity in terms of chemical and electrical characteristics. The diversity is aggravated by the thermal environment variety in the entire pack. After repetitive high rate charge/discharge, some battery cells may exhibit different SOCs and present a much larger internal resistance than others. As can be inferred from the battery linear model in [148], their terminal voltage tends to be higher than others during charging, and tends to be lower during discharging. Battery protection circuits will be mis-triggered as a detected over-charge (or over-discharge). What is more, since the same current flows through all the cells, they will deteriorate even faster due to the resultant heat. After a long time of usage, these cells normally become open circuit, which is essentially the extreme case of unbalance. As a result, the whole

battery pack cannot output the rest capacity and the battery needs replacement, even if there is only one or very few defective/bad cells.

So far in commercial battery management systems, a dissipative current shunt is paralleled to each battery cell to prevent over-voltage [44, 54, 149, 150]. The current shunt, as portrayed in Figure 5.1, consists of a resistor and a MOSFET controlled by a monitor circuitry. For charging operation, the maximum charging rate to the string is determined by the worst cell to guarantee that it will not exceed its maximum tolerable cell voltage. When one cell reaches certain voltage limit, the MOSFET will be turned on so that the extra charge from this cell will be bypassed through the resistor. When this cell hits the maximum voltage limit, a further protection strategy is to cut off the charging process of the whole serial string, even if the other cells still have room to be charged. Consequently, the surplus energy in HEV systems at vehicle braking has to be dissipated as mechanical heat. For discharge operation, there is an over-discharge cut-off protection. This method is simple but is merely an over-voltage protection. It limits the battery capacity utilization, since it cannot achieve real cell equalization. The constrained and intentionally limited state of charge (SOC) window results in an oversized battery package as much as 2-6 times the required useable energy. It is not suitable for upgraded power battery packs in HEVs and EVs, which experience a high charging/discharging rate in very short time, because considerable amount of energy is still wasted as heat. Moreover, this passive protection method is incapable of dealing with the defective cells.

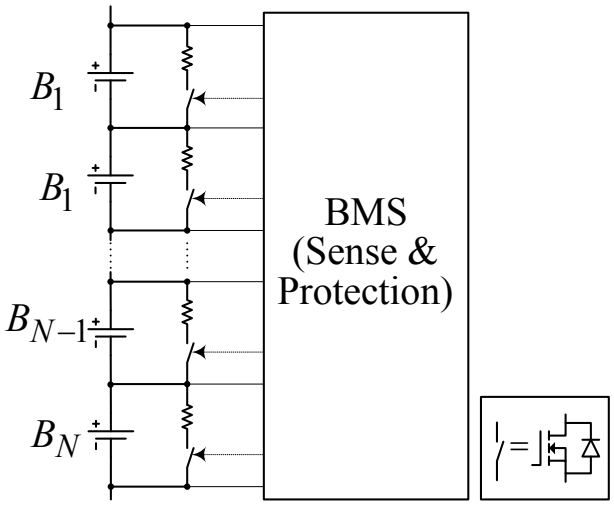


Figure 5.1. Dissipative method

Many literatures ([40-69]) reported non-dissipative balance (equalization) methods, plus some methods developed for balancing serial capacitors but also applicable for batteries [151-153]. The non-dissipative balance circuits can be classified as different groups according to different criteria. One of the classifications is according to the current direction. Some balance circuits can be grouped as charge-type (i.e. the charge balance circuit using a centralized flyback converter [44], as shown in Figure 5.2). They take energy out of the entire string and transfer it to the weaker ones by dc-dc converters. The second group is discharged-type (i.e. the one based on buck-boost converter [57], as shown in Figure 5.3). They shunt current from battery cells with the highest voltage back to other cells until the weak ones are fully charged. The third is the bidirectional charge-discharge type (i.e. the one based on bidirectional flyback converter [64] shown in Figure 5.4). The stronger batteries can be discharged and the weaker ones can be charged directly through bidirectional dc-dc converters. Obviously, the charge-discharge type is more desirable for fast bidirectional operation in HEVs and EVs, but has to employ more active switches.

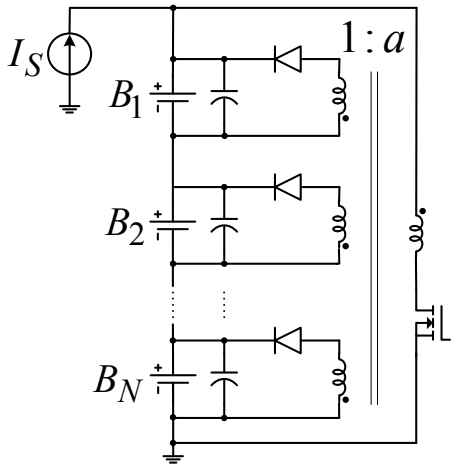


Figure 5.2. An example of the charge type battery balance circuit

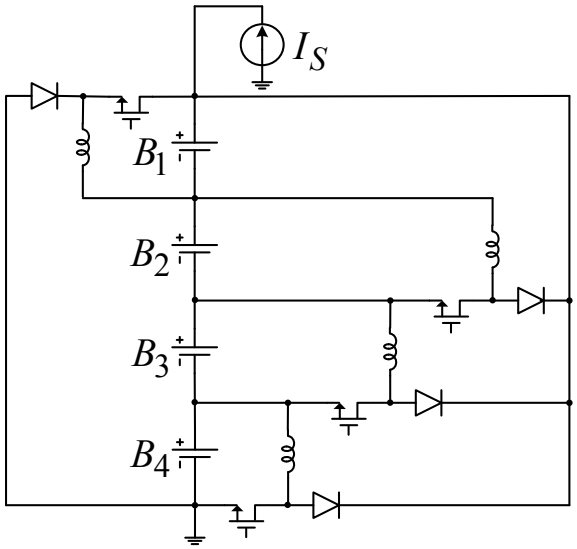


Figure 5.3. An example of the discharge type battery balance circuit

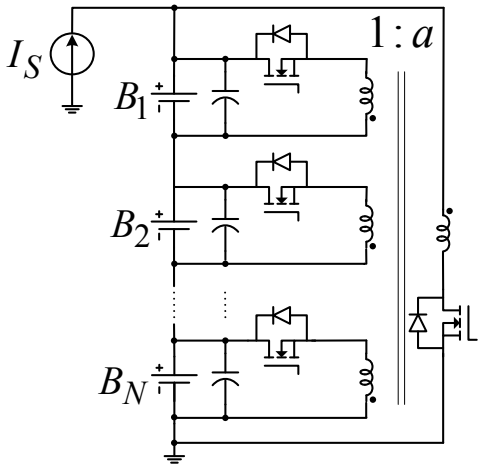


Figure 5.4. An example of charge-discharge type battery balance circuit

Most of the balance methods involve magnetic components in the dc-dc converters. They stemmed either from dc-dc converters with magnetic coupling, or from non-coupled buck-boost or boost type converters. As for the magnetically coupled dc-dc converters, they can achieve cell balance very fast, since it is not a one by one charge transfer. Ideally, the cell voltage can be balanced automatically. In reality, the cells voltage is fairly sensitive to winding leakage

inductance. A feedback control has to be employed for very high precision of cells voltage. A coaxial winding transformer was reported in [51] to minimize leakage inductance. It is still physically difficult to integrate many windings with high coupling coefficient in a core when the number of cells is large. Hence, a modularized circuit was presented in [62]. Yet, in terms of the internal circuit structure, it involves many transformer windings as many flyback balance circuits do. In fact, a centralized forward converter has been proposed in [44] with reduced number of secondary windings, as shown in Figure 5.5. The similar idea of reducing the number of windings was found in a bidirectional, simple, magnetically coupled buck-boost circuit in [52], as shown in Figure 5.6. Later on, the authors of [44] and [52] proposed the same buck-boost balance circuit as shown in Figure 5.7 in [50, 53]. This circuit was also patented earlier in [41], and is now commercialized as shown in [68]. One of the advantages of the non-coupled buck-boost circuit is a simple and modular structure. However, it is a cell-to-cell transfer, leading to different current stress, especially for balancing defective cells.

Meanwhile, there are some bidirectional balance methods based on switched-capacitor dc-dc converters [47, 63, 67] as shown in Figure 5.8. As well known, they can lead to a small and light integration, because of no magnetic components. Resonant switched capacitor circuits [59] have also been proposed for soft switching. They added a very small inductor, but the dominant energy storage component is still the capacitor. Unfortunately, none of the above switched-capacitor based circuits could reach high precision by sensorless implementation. Therefore, a resonant switched capacitor balance circuit as shown in Figure 5.9 was presented in [152] to precisely balance the voltage and SOC by phase shift control. This circuit can be applied to battery balancing as well. Its main features include: both the inductors and capacitors can be made very small, because the voltage imposed on every inductor is very small in most of the

time. High efficiency can be expected due to the zero-voltage-switching (ZVS) on the switches' turn-on and turn-off. It can be a very good candidate, if the balance circuit, including the voltage and current sensors and controllers, can be integrated with the battery cells with reasonable cost. Certainly, as a cell-to-cell transfer, the charge has to pass several modular balance units to reach the weak cells. Practically, a portion of energy is dissipated along the one-by-one transfer and uneven device current stress exists in each modular cell balance unit. Another concern for its acceptance in HEVs could be that a large number of switching devices get involved, even if the total device rating is still low.

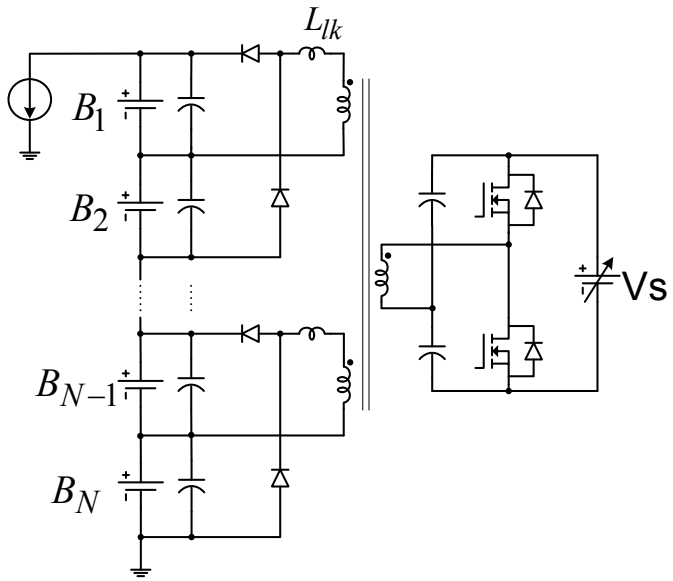


Figure 5.5. Centralized forward balance circuit with reduced number of secondary windings.

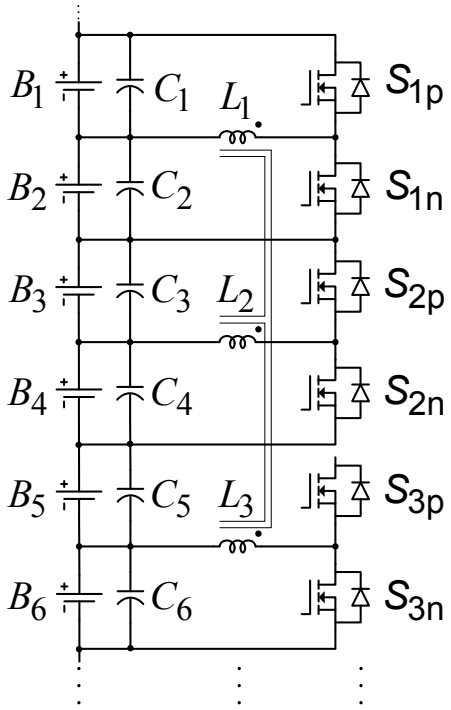


Figure 5.6. A magnetically coupled buck-boost balance circuit.

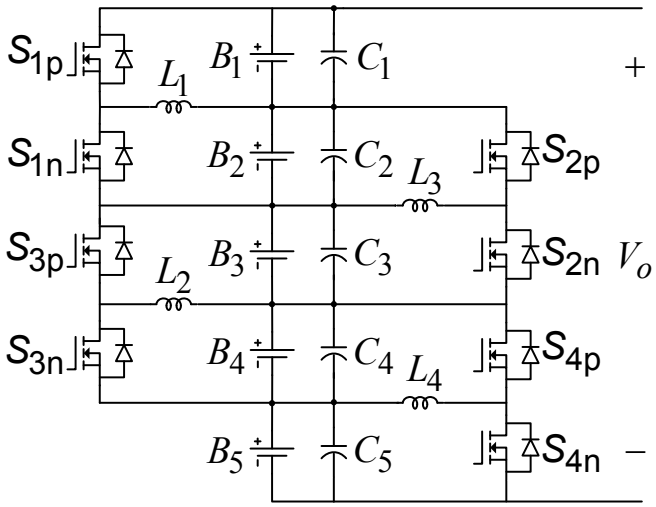


Figure 5.7. Modular non-coupled buck-boost balance circuit

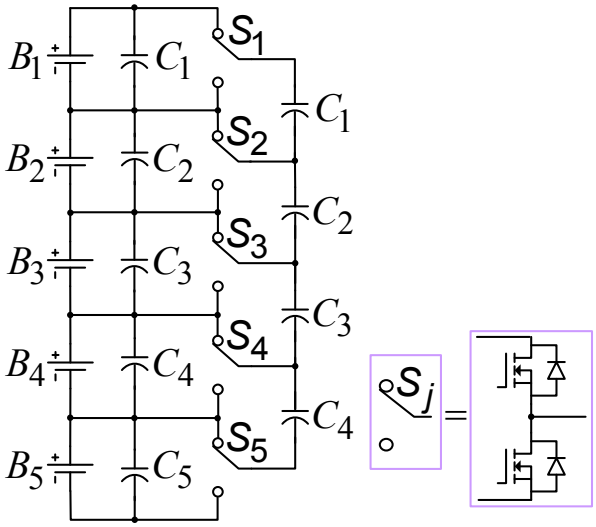


Figure 5.8. The switched-capacitor balance circuit.

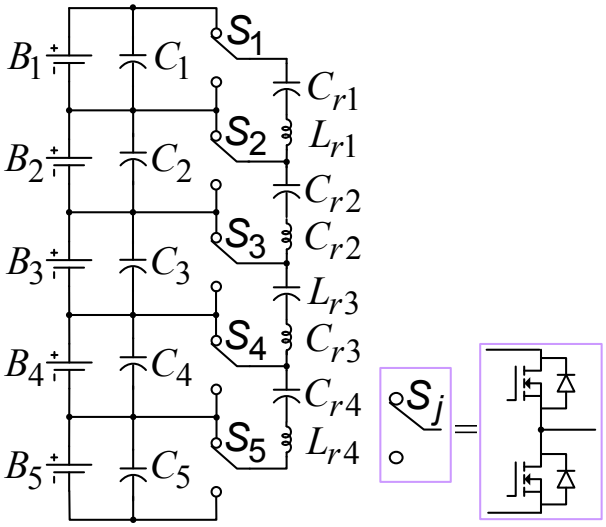


Figure 5.9. The resonant switched-capacitor balance circuit with phase-shift control

As can been seen, no matter which circuit is adapted for a large battery pack, it is better to group the battery cells into multiple modules [50, 62, 63]. Cell balancing is first achieved within each module. As a matter of fact, in the present HEVs like the Toyota Prius 2004, NiMH battery cells are also monitored as a whole module of around 7.2 V. Many of the aforementioned circuits are good candidates for modular balance, but the worst case of unbalance condition, the defective

cell bypass has not been analyzed as much as cell balance. Recently, a circuit was proposed in [65] for defective cell replacing functionality, but it has many switching devices.

As a matter of fact, despite of a variety of battery cell balance circuits developed in last two decades, they still have not beaten the traditional dissipative method in the commercial market for HEVs. The foremost reason is the cost and reliability. Also considering the large number of cells and many special constraints like space and weight in HEVs, a viable balance circuit should consist of the limited component count while not compromising the performance. Now the question is how a circuit can effectively and efficiently handle defective cells in a module such that the whole battery package can still be utilized.

The next sections will start with evaluating the defective cell bypass of the non-coupled buck-boost balance circuit. The analysis will shed light on the general benefit of bypassing defective cell, and at the same time will reveal the demerit of using the non-coupled buck-boost balance circuit. Thus, a magnetically coupled buck-boost with phase-shift control will be proposed. Its operating principle, circuit implementation and experimental verification will be introduced.

5.2. The Defective Cell Bypass Functionality in the Non-Coupled Buck-Boost Balance Circuit

This section discusses the pros and cons of the defective cell bypass using the buck-boost balance circuit as shown in Figure 5.7. The following analysis will first give a full picture of how the circuit behaves and will derive equations to describe how the current is shared by the remaining cells ideally. After the concept has been established, a more general analysis on the cell current will reveal the merits of the balance circuit, based on a more realistic model. Finally,

the component current stress indicates the shortcoming of this circuit in handling defective cells.

Generally, a buck-boost balance circuit for n serial cells can be decomposed as (n–1) modular bidirectional buck-boost converter units as illustrated in Figure 5.10. As well known, the output/input voltage ratios in the buck-boost converter can be controlled by the duty ratio. To simply explain the pros and cons of using this circuit for defective cell bypass, a simple battery model is used, and the two MOSFETs are assumed to switch with a duty ratio of 50% complementally. Combining the (n–1) modular units together, the balance circuit operates in two alternate switching states. Take a 5-cell balance circuit for instance. In the switching state I as shown in Figure 5.11(a), the switches S_{1p}, S_{3p}, S_{2n}, and S_{4n} are turned on for 50% duty cycle; in the switching state II in Figure 5.11(b), the complementary switches are on. If the second cell in Figure 5.11 fails as open-circuit, for example, the discharge current is temporally supplied by the capacitor paralleled with it in half the switching cycle; in the other half cycle, this capacitor gets charged by the energy transferred from the good cells via the inductors. Similarly for the charge mode, the charge current to the defective cell is bypassed. Note that the switch pattern is not unique for this circuit, but it can be easily found that this pattern minimizes the capacitor current and voltage ripples.

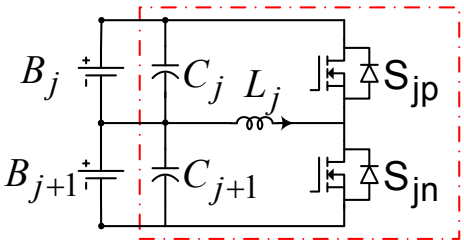
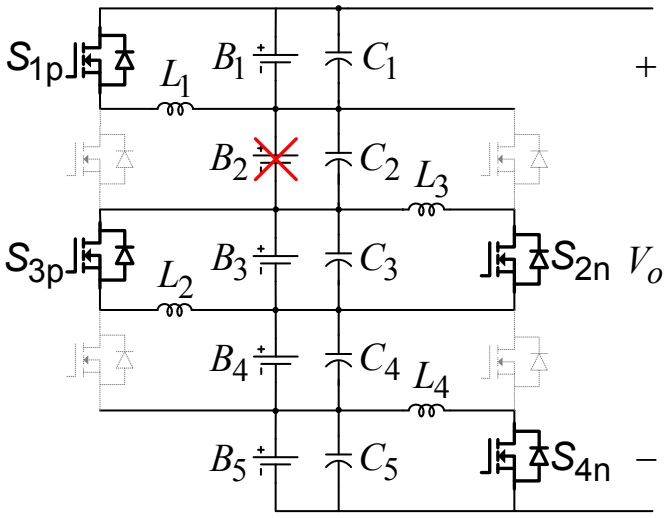
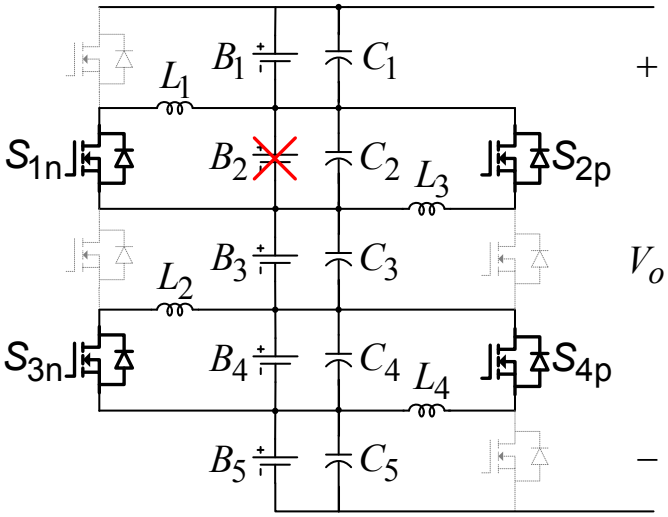


Figure 5.10. The modular unit in the buck-boost balance circuit.

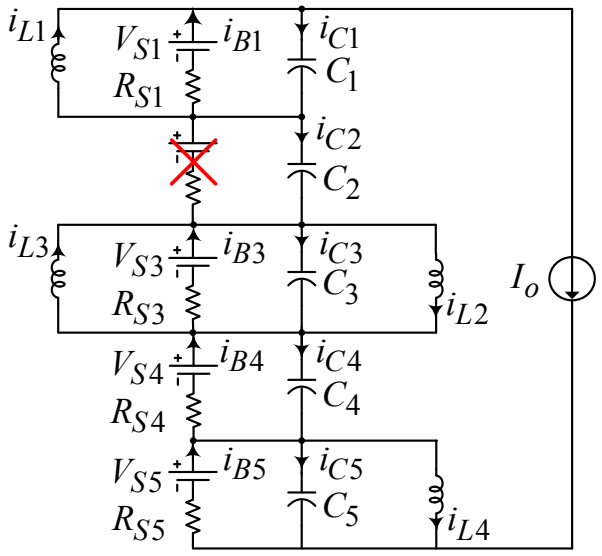


(a) Switching state I

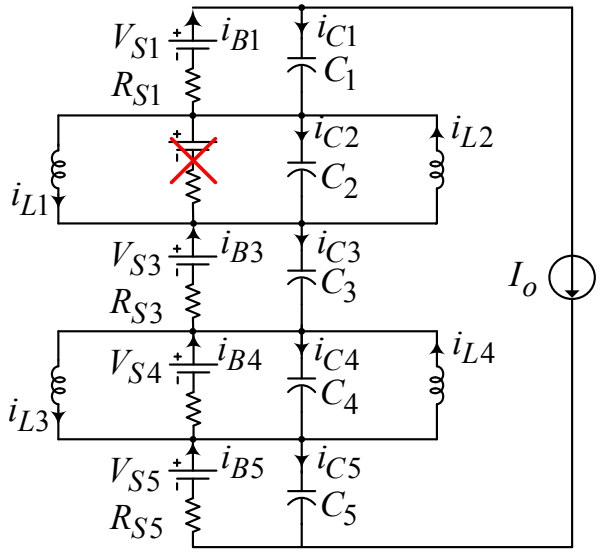


(b) Switching state II

Figure 5.11. The switching states of the 5-cell balance circuit



(a) The equivalent circuit of switching state I



(b) The equivalent circuit of switching state II

Figure 5.12 The equivalent circuit of the 5-cell balance circuit

It is natural to ask: how does the current transfer. It can be explained by the equivalent circuits for the two switching states are shown in Figure 5.12. The current direction is defined according to the discharge mode. Thus the defined current is negative in the charge mode. If

assuming ideal switching devices and negligible dead time, the terminal voltages of two cells end up being the same in each buck-boost converter. Further assuming the identical source voltage and internal dc resistance, the currents through each cell become ideally equal, which can be expressed as the sum of the discharge current, I_o and the extra current, I_x that is resulted from the defective cell:

$$I_{B1} = I_{B3} = I_{B4} = I_{B5} = I_o + I_x \tag{5.1}$$

Let us consider the average values of the capacitor currents in every half switching cycle. The average capacitor currents and inductor currents can be calculated by jointly solving the inductor and capacitor currents in two switching states. According to the defined direction in Figure 5.12(a), in the switching state I, the average capacitor currents are:

$$\langle i_{C1} \rangle_{0\sim Ts/2} = \langle i_{C3} \rangle_{0\sim Ts/2} = \langle i_{C5} \rangle_{0\sim Ts/2} = -I_x \tag{5.2}$$

$$\langle i_{C2} \rangle_{0\sim Ts/2} = -I_o \tag{5.3}$$

$$\langle i_{C4} \rangle_{0\sim Ts/2} = I_x \tag{5.4}$$

In the switching state II in Figure 5.12(b), the average capacitor currents are:

$$\langle i_{C1} \rangle_{Ts/2\sim Ts} = \langle i_{C3} \rangle_{Ts/2\sim Ts} = \langle i_{C5} \rangle_{Ts/2\sim Ts} = I_x \tag{5.5}$$

$$\langle i_{C2} \rangle_{Ts/2\sim Ts} = I_o = \bar{i}_{L2} - \bar{i}_{L1} - I_o \tag{5.6}$$

$$\langle i_{C4} \rangle_{Ts/2\sim Ts} = -I_x \tag{5.7}$$

The average currents through the inductors are:

$$\overline{i}_{L1} = -2I_x \tag{5.8}$$

$$\overline{i}_{L2} = 6I_x \tag{5.9}$$

$$\overline{i}_{L3} = 4I_x \tag{5.10}$$

$$\overline{i}_{L4} = 2I_x \tag{5.11}$$

From (5.6), (5.8)and (5.9), one can get:

$$I_x = I_o / 4 \tag{5.12}$$

So the current stress on the good cells is:

$$I_{Bj} = I_B = 5I_o / 4 \qquad (j = 1, 3, 4, 5) \tag{5.13}$$

Generally, if k arbitrary cells (rather than one) gradually turn to open circuit in an n-cell string, based on the above assumption, the output power and input power should satisfy:

$$\begin{aligned} P_o &= P_{in} \\ &= [(n-k)(V_S - I_B \cdot R_S)] \cdot I_B \end{aligned} \tag{5.14}$$

So the maximum output power can be calculated as:

$$P_{o\_\max} = (n-k)V_S^2 / (4R_S) \tag{5.15}$$

Hence, theoretically the remaining $(n-k)$ cells can still achieve their individual maximum output power of $V_S^2 / (4R_S)$, as if no defective cells exist in the string. Practically, there is some power loss in the gate drives and in the non-ideal circuit components.

Since the output voltage is: $V_O = n(V_S - I_B \cdot R_S)$, the current stress on the remaining cells

can be calculated from (5.14):

$$I_B = \frac{n}{n-k} I_o \tag{5.16}$$

This explains (5.13) from another point of view. In fact, in the real world, the presence of device voltage drop and ESR makes the cell closer to the defective cell undertake a little more current than the cell farther away from the defective one. Furthermore, considering the practically different internal voltage and resistance in individual modules, the input power can generally be represented as:

$$P_{in} = \sum_{j=1}^{n-k} (V_{sj} - I_{Bj} \cdot R_{sj}) I_{Bj} \tag{5.17}$$

Since the terminal voltage of each cell is equalized to V_o / n if the voltage drop in the balance circuit is negligible, the current through each cells can be written as:

$$I_{Bj} = (V_{sj} - V_o / n) / R_{sj} \qquad (j = 1, ..., (n-k)) \tag{5.18}$$

Some merits of the balance circuit can be observed from (5.18). When k=0, it implies that no cell is completely open-circuit. Nevertheless, if one of the battery cells is weaker than others, it tends to present a higher ESR and its internal voltage becomes lower than that across the other cells in discharge mode. Now thanks to the balance circuit, the individual cell currents are automatically distributed according to their output capacity. That is, the cells with higher internal voltage and lower internal resistance undertake more current and thereby more output power. Plus, the current drawn from a cell is reversely proportional to its internal resistance. So less power loss will be dissipated on the weak cell with larger internal resistance, compared to the case of no cell balance circuit. The life time of the cells can be prolonged. The chance is reduced that such cell turns to consume electric power from others.

However, the demerit for this circuit is the inductor current stress is quite uneven, according to the derivation of the current relationships, even if this switching pattern is applied to minimize the capacitor current stress. What is worse, using the same approach, it can be found that the overall inductor current stress is the worst case when the defective cell occurs at the top or at the bottom of the serial string. Hence, the inductors should be designed based on this worst case. The current stress problem exists in the switched-capacitor circuit in [152] as well. For defective cell bypass, too much current stress also results in more voltage drop and power loss in the balance circuit.

5.3. The Battery Balance Circuit with Phase-Shift Control

One possible way to circumvent the above dilemma is to adopt magnetic coupling. After all the windings are coupled together, if the modular buck-boost balance units on left side are removed, the circuit is then reduced to the same as the magnetically coupled buck-boost circuit Figure 5.6. Compared to the original buck-boost balance circuit, the magnetically coupled buck-boost circuit reduced the magnetic component and switching devices almost by half. However, very precise balance relies on a complete coupling in the magnetic coupled circuit. To obtain good balance with non-ideal magnetic coupling, a phase-shift control is proposed in this chapter. Generally speaking, N battery cells are paralleled with N/2 buck-boost (/half-bridge) balance circuit unit. Within the same buck-boost unit, each buck-boost converter makes the terminal voltage difference of two cells very small. Among every pairs of buck-boost unit, the magnetic coupling and phase-shift control diminishes the voltage difference. In fact, the phase-shift control method ([154]) plus a PWM control has also been reported in [155] for balancing capacitor voltages in a diode-clamped multi-level inverter. However, unlike the passive capacitors, the battery cells are independent voltage sources.

The operating principle of the new balance method is introduced via an example of a 4-cell balance circuit. The four cells can be grouped into two pairs. Within each pair, two adjacent cells, B_1/B_2 and B_3/B_4 are balanced by the buck-boost half-bridge. Admitted, a little voltage difference would exist considering the voltage drop on the switching devices. When the 50% PWM signals between two pairs of cells are further phase-shifted as shown in Figure 5.13, the balance circuit is essentially a bidirectional dc-dc converter that is able to transfer current from one half-bridge pair to the other. The corresponding switching sequences are illustrated in Figure 5.14, for a positive phase-shift angle. What is of our interest is the transferred charge or the corresponding current with respect to the phase-shift angle. Take the case that the cell B_1 is overcharged for instance.

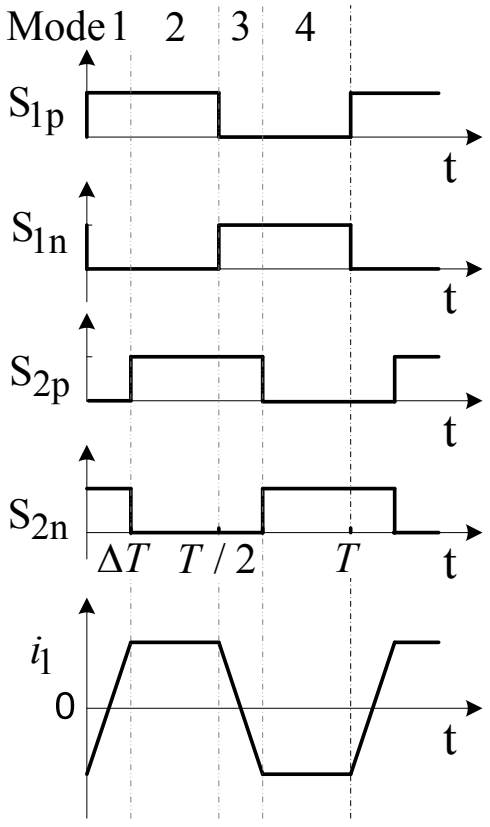
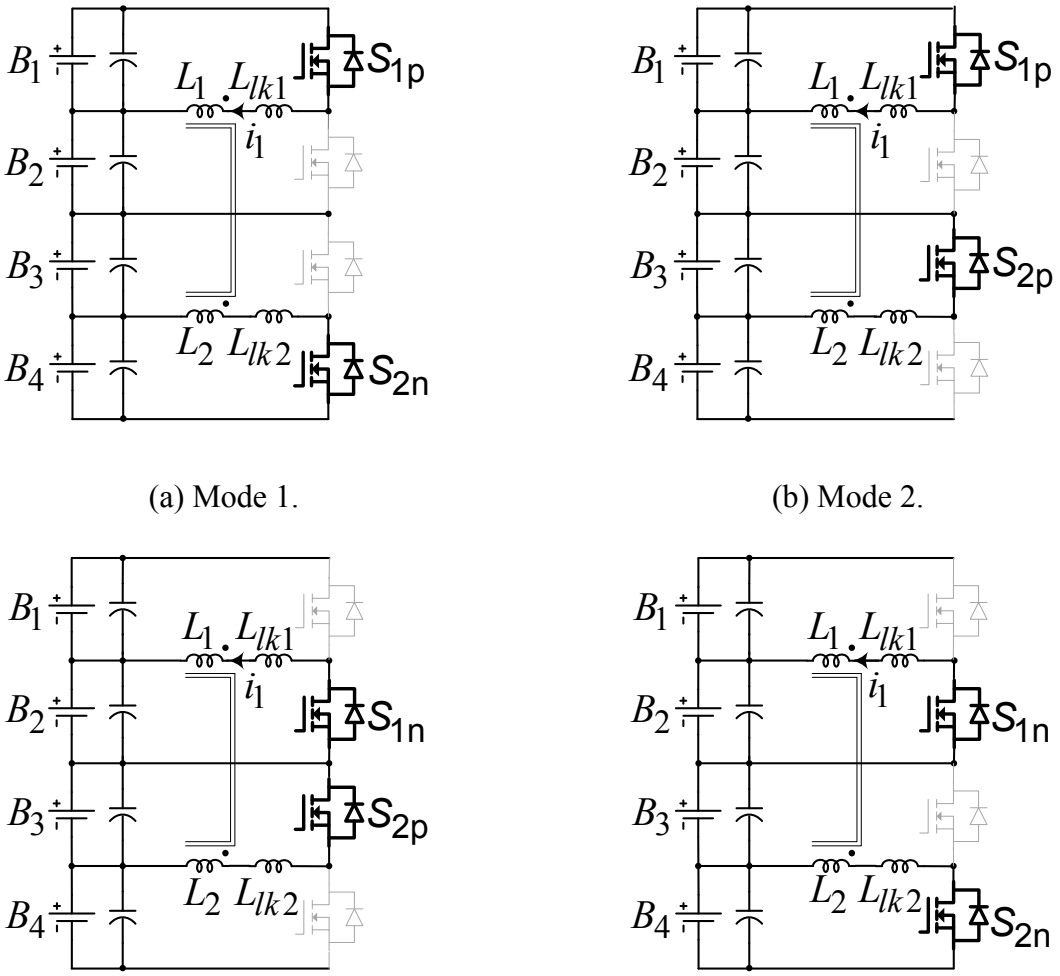


Figure 5.13. PWM signals and waveforms when cell #1 is overcharged.



(a) Mode 1.

(b) Mode 2.

(c) Mode 3.

(d) Mode 4.

Figure 5.14. Operation modes in phase-shift control.

The battery cell is modeled as an equivalent voltage source in series with a resistance, and they makes the terminal voltage of V_{BX} (X=1, 2, 3, 4). Their equivalent circuits can be simplified in Figure 5.15. Since the magnetizing inductance of the two windings is usually large, the transformer can be replaced by the series of the equivalent leakage inductance $L_{lk}=L_{lk1}+L_{lk2}$. Assuming the terminal voltages are equalized to V_{dc} in steady state and ignore the device

voltage drop, the voltage imposed on the lumped leakage inductance changes as follows,

$$v_{Llk}=\begin{cases}V_{B1}+V_{B4}=2V_{dc}, & \text{in mode 1}\\ V_{B1}-V_{B3}=0, & \text{in mode 2}\\ -(V_{B2}+V_{B3})=-2V_{dc}, & \text{in mode 3}\\ V_{B4}-V_{B2}=0, & \text{in mode 4}\end{cases}. \tag{5.19}$$

1) From the initial point to the phase-shift point ΔT, the current through the transformer windings can be written as

$$i_1(t)=i_1(0)+\frac{V_{B1}+V_{B4}}{L_{lk}}t=i_1(0)+\frac{2V_{dc}}{L_{lk}}t, \tag{5.20}$$

where $i_1(0)$ is the current at t=0.

2) From the time ΔT to half of the switching cycle, $T/2$, the winding current is

$$i_1(t)=i_1(\Delta T)+\frac{V_{B1}-V_{B3}}{L_{lk}}(t-\Delta T)=i_1(\Delta T). \tag{5.21}$$

3) From the time of $T/2$ to $T/2+\Delta T$, the winding current becomes

$$i_1(t)=i_1(T/2)-\frac{V_{B2}+V_{B3}}{L_{lk}}(t-T/2)=i_1(T/2)-\frac{2V_{dc}}{L_{lk}}t. \tag{5.22}$$

4) From the time $T/2+\Delta T$ to the end of one switching cycle, T, the winding current is

$$i_1(t)=i_1(T/2+\Delta T)+\frac{V_{B4}-V_{B2}}{L_{lk}}(t-T/2-\Delta T)=i_1(\Delta T). \tag{5.23}$$

In steady state, the winding current satisfies

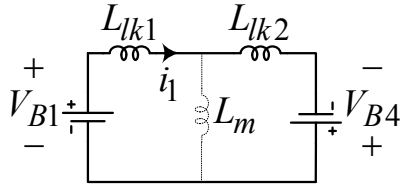
$$i_1(0)=i_1(T)=-i_1(T/2),\ \ i_1(T/2+\Delta T)=-i_1(\Delta T). \tag{5.24}$$

From (5.20)-(5.24), the initial condition can be solved as

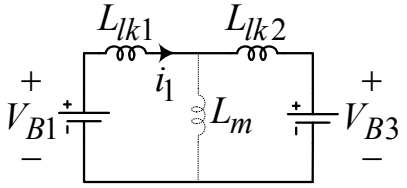
$$i_1(0) = \frac{V_{B4} - V_{B2}}{L_{lk}} \bullet \frac{T}{4} - \frac{V_{B4}}{L_{lk}} \bullet \Delta T$$
$$i_1(\Delta T) = \frac{V_{B4} - V_{B2}}{L_{lk}} \bullet \frac{T}{4} + \frac{V_{B1}}{L_{lk}} \bullet \Delta T \,. \tag{5.25}$$

Thus, the relationship of the average current from the battery cell $B_1$and the phase-shift angle is found in (5.26). It is illustrated in Figure 5.16. The phase-shift control provides a freedom to actively control the current flow among different pairs of battery cells. Only cell voltage balance is discussed here, because this way helps distribute the currents each cell sees according to the capacity as analyzed before. Nonetheless, the balancing SOC can also be implemented with the aid of more sophisticated SOC estimation.

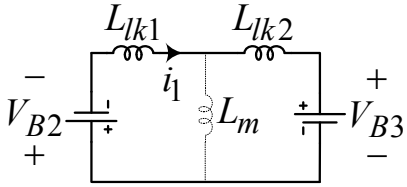
$$I_1 = \frac{1}{T/2}\int_0^{T/2} i_1 dt = \frac{2V_{dc}\Delta T(T/2 - \Delta T)}{T \cdot L_{lk}} \tag{5.26}$$



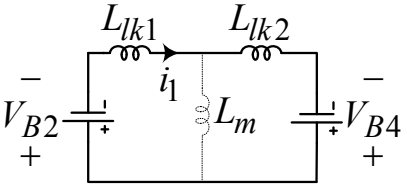
(a) Mode 1.



(b) Mode 2.



(c) Mode 3.



(d) Mode 4.

Figure 5.15. Equivalent circuits.

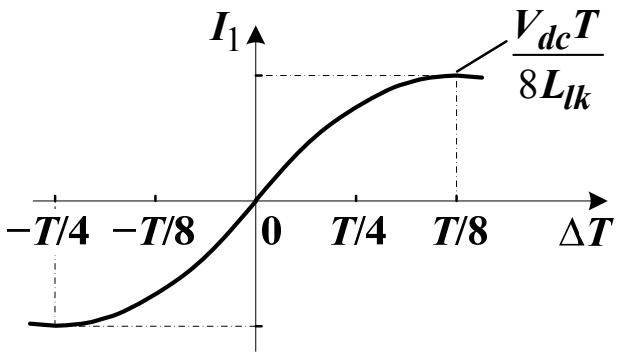


Figure 5.16. Transferred current vs. the phase-shift angle.

5.4. Experimental Results

A 4-cell balance circuit has been built to experimentally evaluate the magnetically coupled buck-boost balance and bypass circuit. 21-Ah lithium-ion polymer battery cells HA055275 are used. The voltage difference of the two half bridges is obtained via proportion and differential amplifier circuits. The voltage difference is fed to the phase-shift control and generation circuit, which phase-shifts the PWMs between two half-bridges using a phase-shift PWM controller ucc3895. To reduce the standby power consumption, the balance circuit is turned off when the voltage difference is within a predefined hysteresis band. And it is turned back on when the voltage difference is beyond the band. An additional soft-start AND logic controls the duty cycle to gradually increase from 0 to 50%, so as to prevent inrush current during start-up.

The comparative experiments were conducted with and without the balance circuit. The four cells are charged with a constant current of 12 A (0.6 C). Cell #1 always presents higher (/lower) voltage during charge (/discharge) according to historical data. Without any balance circuit connected, as shown in Figure 5.17, the terminal voltage difference among the four cells is around 200 mV, and the Cell #1 hits the preset charge limit much faster than the others. As a comparison, when the proposed magnetically coupled buck-boost balance circuit with phase-

shift control kicks in, the terminal voltage difference of four cells gradually shrinks to within 20 mV, as shown in Figure 5.18. As a result, the whole battery string can keep charging for a longer time, since the charging current into Cell #1 is diverted to other cells. In fact, it is found that the tolerance of the sensing and voltage differential circuit contributes considerable error to the 20-mV voltage difference, while the error present to the phase-shift control circuit is fairly close to zero. The comparison validates that the applied method can effectively balance battery cells and can extend the utilization of the whole serial string.

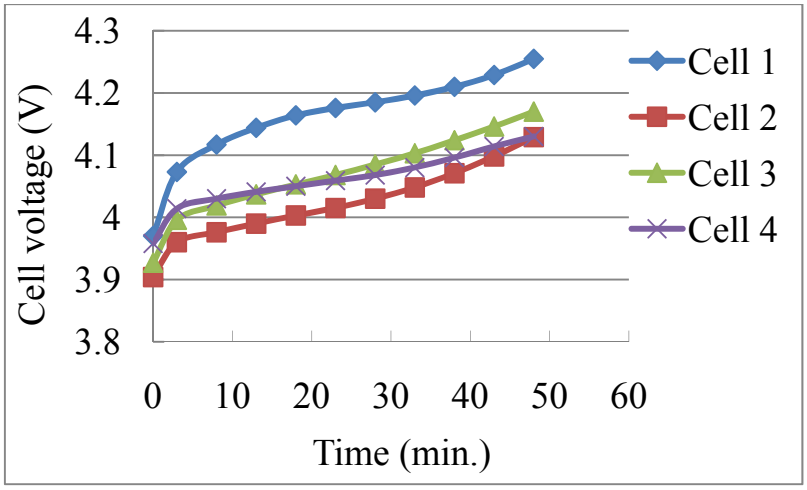


Figure 5.17. Experimental data of charging without balance circuit

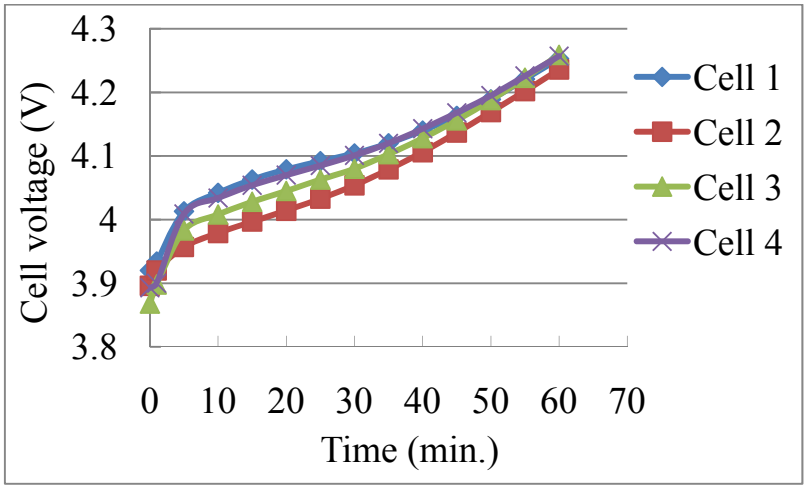


Figure 5.18. Experimental data of charging with the balance circuit and phase-shift control.

5.5. Summary

This chapter introduces the approaches of battery cell balance and defective cell bypass for a reliable operation of the energy storage system. Some existing battery balance circuits have been reviewed. Afterwards, the unbalance condition with defective cell(s) is discussed, which is a usual failure mode of batteries. The benefits and problems of bypassing defective cells using a traditional modular buck-boost circuit were analyzed as an example. The current and power that the individual cells sustain can be distributed according to their capacity. The utilization of the series connected cells is more effective. The life time of the serial battery cells/modules can be prolonged.

To achieve cell balance with better current stress distribution and a smaller component count, a new balance method using phase-shift control has been proposed. Each pair of battery cells are paralleled with a magnetically coupled half-bridge balance circuit. Charge is transferred directly from the surplus pairs to the weak ones. Experimental results on four Li-ion battery cells are provided to prove the concept. This method can also be applied to battery modules, e.g., to balance the serially connected 12-V lead-acid battery modules for the backup dc power supply in rail way.

Chapter 6 Conclusion and Recommendation

6.1. Conclusion

This thesis presents a class of power electronics circuits for voltage boost, balance and long-life operation in diverse applications of energy storage systems.

– A four-level flying-capacitor dc-dc converter has been explored to reduce the inductance requirement of the traditional dc-dc converter to almost 1/10. A special case of the four-level converter, a variable 3X dc-dc converter has been presented to further reduce the inductance requirement to a minimal value (almost zero). A 55-kW 3X dc-dc converter prototype has been developed that interfaces the battery module with the inverter dc bus for HEV traction drives. Its compact size, light weight and high efficiency make it a promising alternative to the present dc-dc boost converter in some commercial HEVs. With the trend of higher coolant temperature, this converter has the great potential of highly integrated power stage for future HEVs.

– For other applications that demand higher voltage gain in high temperature environment such as PV and thermal electrical generation, another topology of switched-capacitor dc-dc converter is proposed. The simulation and preliminary experimental results verifies its many advantages: considerably reduced total capacitor voltage ratings, lower power rating, smaller count of the switching devices, lower power loss, and etc.

– A family of trans-Z-source inverters is proposed for the dc-ac power conversions like gird-connected micro inverter for PV, and single stage dc-ac inverter without boost/buck converters for HEVs. While maintaining the main features of the original Z-source network, the new networks exhibit some unique advantages, such as the increased voltage gain in the voltage-fed trans-ZSIs and the expanded motoring operation range in the current-fed trans-ZSIs when the

turns-ratio of the transformer windings is over 1. Simulation and experimental results have verified their characteristics.

– Solutions of cell balance and defective cell bypass are investigated for one of the widely used energy storage devices − the battery. A phase-shift control method is proposed to improve the performance of a magnetically coupled buck-boost balance circuit. This method tends to make the current stress more balanced in each balance circuit unit, and thus is suitable for defective cell bypass.

6.2. Recommendation for Future Work

For the 3X dc-dc converter for PHEVs, the coordinative operation with the subsequent dc-ac inverter could be a very interesting topic. When the dc-dc converter operates at three discrete output/input voltage ratios without almost null input inductance, the final ac output is regulated by a continuous control of the modulation index in the inverter, with the aid of the three flexible voltage ratios. An optimal operating range of the 1X, 2X and 3X modes could be analyzed. The optimal transient time among different modes could be investigated, which is also pertinent to the control of the inverter during the transient. By contrast, when the output voltage of the dc-dc converter is desired to be regulated via a very small input inductor, the operating range could be similar as in some of the present commercial HEVs.

In addition, from the equivalent circuits of the 3X dc-dc converter in Chapter 2, the equivalent loop capacitance differs in three charge/discharge loops. This intrinsic characteristics result in the difference in charge/discharge current profile, turn-on/-off current, conduction loss and switching loss in different switching states. Local optimization with respect to switching frequency and input inductance could be further analyzed to get a better design of the converter.

For the NX dc-dc converter, its magnetic-less nature makes it easy to be integrated into a

chip or a micro converter module. Then it would be a convenient plug-and-play device. To achieve this goal, it is important to optimize the power density, efficiency, and performance of the converter. These figures of merit could be compared with the transformer-based boost converters for high voltage gain. It could be theoretically analyzed whether there is a voltage gain limit due to the ESR in the NX dc-dc converter. Besides, the comparison should take into consideration the voltage regulation. For the applications requiring only dc-dc conversion, an NX dc-dc converter cascaded with a regulated dc-dc converter is one applicable solution thus far. The efficiency can still be very high when the regulated dc-dc converter does not have to be stressed by the high current. Another approach in regulating some switched-capacitor dc-dc converters is adopting an extra inductor and phase-shift control [125]. Such a converter has high efficiency in a limited range of voltage ratios. More investigation could be done on alternative configurations and control methods that are suitable for regulating the NX dc-dc converter.

The present NX dc-dc converter was designed to switch off at a low yet not zero current. The zero-current-switching has also been explored in a later paper [156]. Either way, the resonant frequency of each charge/discharge loop is affected by the variation of the capacitance and inductance. Moreover, as mentioned before, the input voltage from a PV module usually varies with a ratio of 1:2. The capacitance of the current multilayer ceramic capacitors decreases dramatically as the voltage increases, although they are the most promising candidate for high temperature environment. Thus, the circuit should be able to automatically tune up the switching frequency to be close to or a little above the resonant frequency.

For the trans-Z-source inverters, ever since their debut, they have got immediate attention in [157-160]. However, besides pursuing high voltage boost ratio or extended operating range in impedance-source inverters, the optimal design and downsizing the magnetic component of Z-

source inverters could be studied. The challenge to the magnetic in trans-Z-source inverters arises from the pulse current. Another practical issue to be addressed is the voltage clamping for the diode in the voltage-fed trans-Z-source network. If a trans-Z-source-inverter is further to the NX dc-dc converter(s) for PV generation, the control strategy could be investigated. Meanwhile, new topologies rather than simple cascading are also possible.

For the balancing and long-life operation of batteries, a great deal of exciting work remains due to the time limit. Firstly, the thesis has only demonstrated the phase-shift control on the magnetically coupled buck-boost balance circuit. More research could be done on the viability of combining the duty cycle control and the phase-shift control with appropriate control strategy and sequence. In this way, the voltage or SOC of the two cells could be controlled and balanced within the pair of buck-boost half-bridge.

Secondly, four Li-ion battery cells were only considered, which have made a decent voltage of around 10.8~16.8 V. Nevertheless, if more cells are desired in series in a module, the balance circuit can be extended to multi-winding. The control algorithm could be more complicated, because more cells and more magnetically coupled windings come into the picture.

Thirdly, further research can be done on the capacity and health status prognosis for battery cells (or for battery modules), based on the information from the battery balance circuitry. For instance, when the battery balance circuit is launched after an unbalance condition is sensed, the diverted current flowing through the MOSFET is an indication of the capacity of individual battery cells. For a HEV or EV carrying hundreds of battery cells, the power consumption, reliability and cost of extra circuits to obtain very precise prognosis are of engineers' concern, whereas this approach makes use of the balance circuit itself.

Fourthly, the multiple functionalities should be integrated together with the battery cells.

Since the self-contained power supply and gate drives are sourced from the battery package itself, efficiency is a critical figure-of-merit, be in the operation and in standby mode. In terms of size and volume, design optimization is desired for the magnetic component. Planar transformers could be considered. Furthermore, in terms of integration and control complexity, it would be very helpful to compare the proposed balance method with the resonant switched-capacitor balance circuit with phase-shift control in [152].

Fifthly, the thesis only discusses the cell balancing inside a battery module. If a balance circuit is designed to tolerate the aforementioned open-circuit cells, its power rating will be larger. On the contrary, depending on the applications, one possibility is the existing two-level modular balance approach. Cell balance circuits are designed only for the ordinary unbalance condition within the same module. The top level modular balance circuits are able to handle the open-circuit in the event of any battery modules. Another approach could be the modular dc-dc converters or dc-ac inverters for the top level. As illustrated in Figure 6.1, one dc-dc converter is fed with one battery module, and multiple converters/inverters are connected in series and/or parallel for the required output voltage and power, similar as in [111, 161, 162]. To take it a step further, the voltages and SOCs can indeed be controlled to be balanced or to be different among modules, depending on their output capacity. That is, in event of any defective cell(s) in a module, this module can be controlled to handle less charge, or even completely bypassed via its dc-dc converter. Such a modular structure provides more flexibility, more redundancy and more fault tolerance.

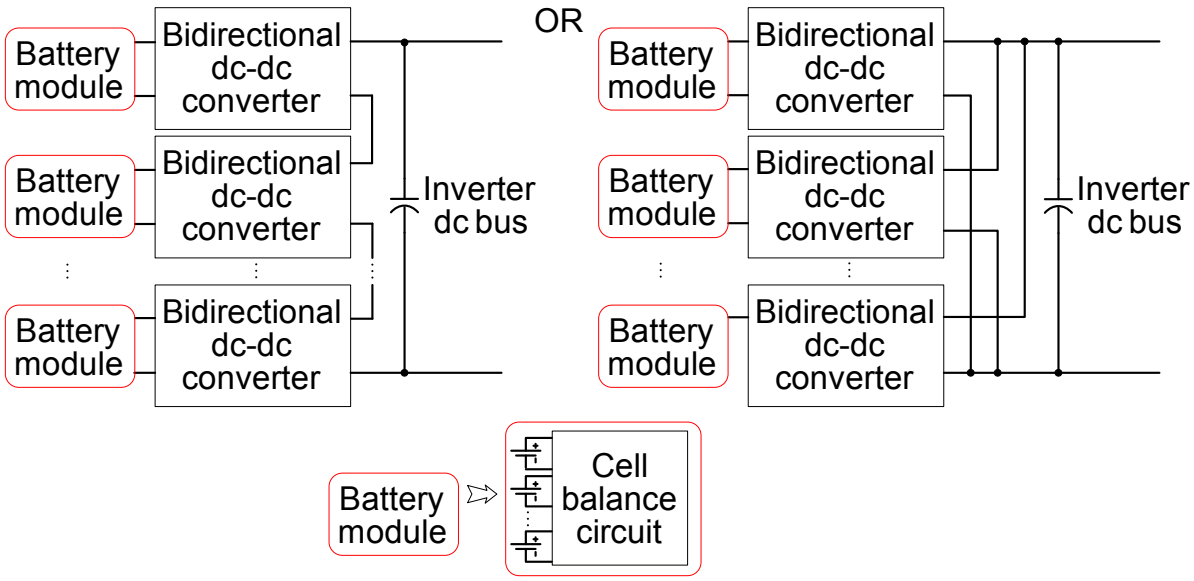


Figure 6.1. Modular dc-dc converter configuration

Finally, more investigation would need to be done in the systematic combination of the proposed circuits to fulfill the practical demand.

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