MINIMIZING DC CAPACITOR CURRENT RIPPLE AND DC CAPACITANCE REQUIREMENT OF THE HEV CONVERTER/INVERTER SYSTEMS

By

Xi Lu

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ABSTRACT

MINIMIZING DC CAPACITOR CURRENT RIPPLE
AND DC CAPACITANCE REQUIREMENT
OF THE HEV CONVERTER/INVERTER SYSTEMS

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Minimization of the dc capacitor is an essential step towards developing and manufacturing compact low-cost hybrid electric vehicle (HEV) converter/inverter systems for high temperature operation, long life and high reliability.

Traditionally, the dc capacitance has been determined according to empirical equations and computer simulations, which provides little insights into how to minimize the dc capacitor.

This thesis presents an accurate theory of calculating the dc link capacitor voltage ripples and current ripples for inverters and pulse-width modulation (PWM) rectifiers, which most commonly exist in HEV converter/inverter systems. The results are analyzed and summarized into graphs according to the theory, which helps to find the right capacitance value for a given voltage ripple tolerance and the rms ripple current that the capacitor has to absorb. Based on this theory, a PWM modulation method for the dc-dc converter that connects the battery to the dc link is developed to further minimize the current ripples through the dc link capacitor, so that further minimize the capacitance. A 150 kW inverter prototype has been built to verify the theory. The comparison between the calculation result and experimental result shows that they are in close agreement.

Dedicated to my Father and Mother:
Jiming Lu and Xuri Shen

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Finally, thanks from my deep heart go to my parents. Thank you for raising me up and teaching me everything. The love that I got from you is beyond expression.

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CHAPTER 1 Introduction and Motivation

1.1 Background

1.1.1 The Advantage of HEV in the Automotive Market

Emissions of CO_2 by human activities are currently amounting to about 27 billion tons per year [1]. The considerably high amount of CO_2 emission forces people to make every effort to minimize these emissions from the aspect of the human activities. Many excellent thoughts are considered, compared, analyzed, developed and finally built, tested and realized. One of these outstanding ideas, which protecting our mother earth from global warming and pollutions, is the development of hybrid electric vehicles (HEV), plug-in hybrid electric vehicles, and pure-electric vehicles. There are many worth reading websites and reviewed papers discussing the configurations of each kind and the comparison among them [2-4].

Nowadays, compared to the plug-in HEV and pure-electric vehicle, the HEV is the most popular and commercial type in the current automotive market. Similar to the ordinary vehicles, HEV possesses the power of fast acceleration and longer driving distance without the limitation of charging requirements.

The HEV system utilizes two different and independent energy sources, and hence, achieves a much higher fuel economy than the traditional vehicle with solely operated by the low-efficiency energy source—the internal combustion engine (ICE). Therefore, utilizing the HEV

can reduce the emissions of CO_2 and help clean the cities, at the same time save the limited energy resources for the world due to its higher efficiency (mile per gallon).

However, speaking to individuals, the cost of a HEV is still higher than the gas price that can be saved from it. Therefore, in order to impel more and more people to buy HEVs, the price needs to be further lowered down. That is why engineers have been doing researches on minimizing the cost, weight and size of the motors, generators, power electronics devices, and passive components in HEV systems during the past decades.

This thesis is mainly focusing on minimizing one of the biggest passive components in the HEV systems—the dc link capacitor, working for the same goal of minimizing the cost, weight and size of the whole HEV systems.

1.1.2 Types of HEV Systems

Focus on HEVs, there are many different ways to classify HEV systems, and the general classification is to classify HEVs according to the way in which power is supplied to the drivetrain. Hence, there are three categories: series hybrid electric vehicles (SHEV), parallel hybrid electric vehicles (PHEV), and series-parallel hybrid electric vehicles (SPHEV). Generally speaking, the SHEV is used on heavy duty vehicles (buses, trucks etc.), while the PHEV is usually applied to light duty vehicles (family sedan etc.).

In order to illustrate the power electronics modules that located in the HEV, take the SHEV system as an example. The general power electronics function blocks in the commercial SHEV systems can be demonstrated similarly as Figure 1.1, which consists of an internal combustion engine (ICE), a generator/motor, a bidirectional pulse-width modulation (PWM) rectifier, a dc link capacitor bank, a bidirectional inverter and a motor/generator. Additionally, instead of a

high voltage battery, a low voltage battery with a smaller size is usually preferred and connected to the dc link through a dc-dc boost converter. For the sake of having the PWM rectifier, the inverter, and the dc-dc converter each at the same power rating, the system can have two smaller inverters controlling two traction motors respectively (shown in Figure 1.1) instead of only one inverter, whose power rating is the summation of the PWM rectifier's and the dc-dc converter's.

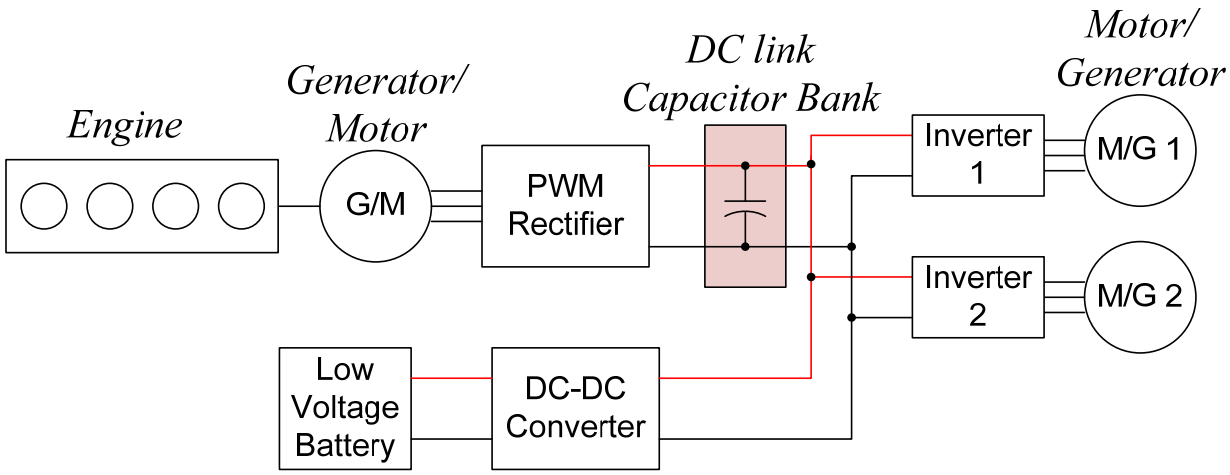

Figure 1.1 The power electronics function blocks of the series hybrid electric vehicle (SHEV) systems (**For interpretation of the references to color in this and all other figures, the reader is referred to the electronic version of this thesis**)

1.2 Power Electronics Challenge in HEV systems

As shown in Figure 1.1, in a SHEV converter/inverter system, the dc link capacitor bank, shown in the shaded block, is usually bulky, heavy and expensive. The reason for this is that, this dc link capacitor bank needs to absorb all the current ripples generated by two inverters, the PWM rectifier, as well as the dc-dc converter. However, traditionally, this dc capacitance has been determined according to empirical equations and computer simulations, which provide little insight into how to minimize the dc link capacitance. Therefore, they are usually much bigger than needed, so that they occupy an unnecessarily large space. It is certainly the biggest

component in an inverter box. As a result, minimization of the dc capacitance is an essential step towards developing and manufacturing compact, light, low-cost HEV converter/inverter systems for high temperature operation, long life and high reliability.

Therefore, in order to achieve an optimum minimization of the dc capacitor, an accurate theory to calculate the dc capacitor voltage and current ripple must be developed first, then PWM and control techniques can be further developed to minimize both dc voltage and current ripples.

1.3 Operation Modes in HEV

1.3.1 Sinusoidal Pulsewidth Modulation Mode

In the HEV converter/inverter systems, when the vehicle is at a relatively low speed, such as accelerating from a stop, battery is often chosen as the power supply, instead of the inefficient ICE. Plus, dc-dc converter is operated as a boost converter, to boost the low battery voltage to relatively high dc link voltage. Afterwards, the three-phase inverter used to drive the traction motor usually use sinusoidal pulse-width modulation (SPWM) mode. The SPWM mode can supply a smoothly increasing ac voltage to cooperate with the increasing speed, in order to ensure the maximum current and maximum torque. That comes from the *V/f* control. In this motoring situation, Figure 1.2 is the equivalent circuit.

Another important situation is when the generator/ICE started. In order to save the trouble of building another lower power rating starter and adding an additional 12-V battery, just utilizing the existed battery and the PWM rectifier instead could be a good choice. This requires the PWM rectifier works as an inverter at this time, which again Figure 1.2 is the equivalent circuit.

How about the regenerative modes? Regenerative mode happens at when the driver pushes

the brake pedal. At this time, the motor acts as a generator. The generated power is transferred through a three-phase PWM inverter (PWM rectifier mode in this case) and a dc-dc converter, and stored this power in the battery. By doing so, instead of wasting the energy to heat up the brakes or bleeding resistors, the energy is stored and can be reused later on. This results in energy saving, and high efficiency. Since the motor/generator is operating as a generator, the three-phase PWM inverter should operate as a PWM rectifier accordingly to convert the power from ac to dc. Although it sounds so different, the PWM rectifier is actually the same as the SPWM inverter. Therefore, in the regenerative mode, as the brake pedal is being pushed and the speed is decreasing, the PWM rectifier is operated by SPWM, which again Figure 1.2 is considered.

And of course, when the energy comes from ICE/generator side to the dc link side, the PWM rectifier is working as a PWM rectifier. Therefore, it is again Figure 1.2.

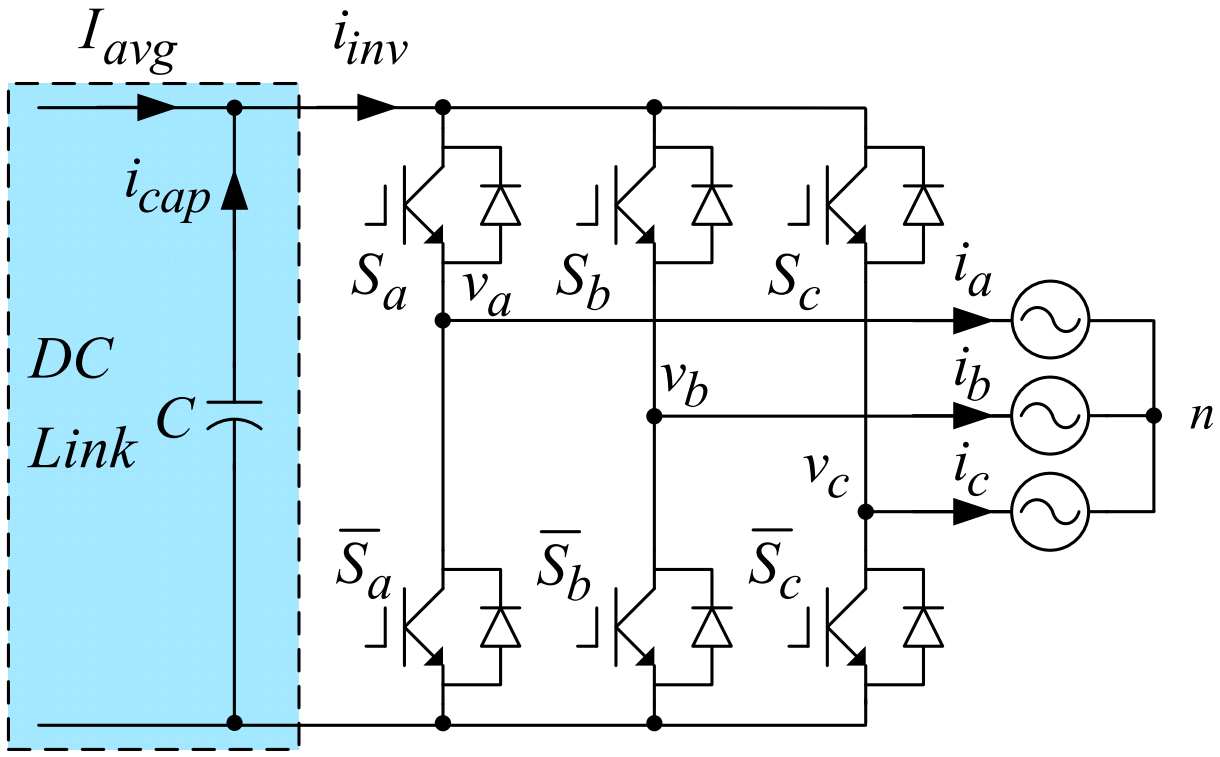

Figure 1.2 The schematic of a three-phase inverter/PWM rectifier using SPWM with three-phase current sources as load

1.3.2 Six-Step Mode

After the acceleration, the vehicle reaches at a much higher speed. This requires the inverter to output a higher voltage. In this case, six-step operation is often used, due to its higher dc voltage utilization. This is demonstrated in Figure 1.3. The only difference from the SPWM operation mode is that, for six-step operation, when the vehicle goes to higher speed, the back electromotive force (EMF) can no longer be ignored, that is what happened with those added voltage sources at the load side in Figure 1.3.

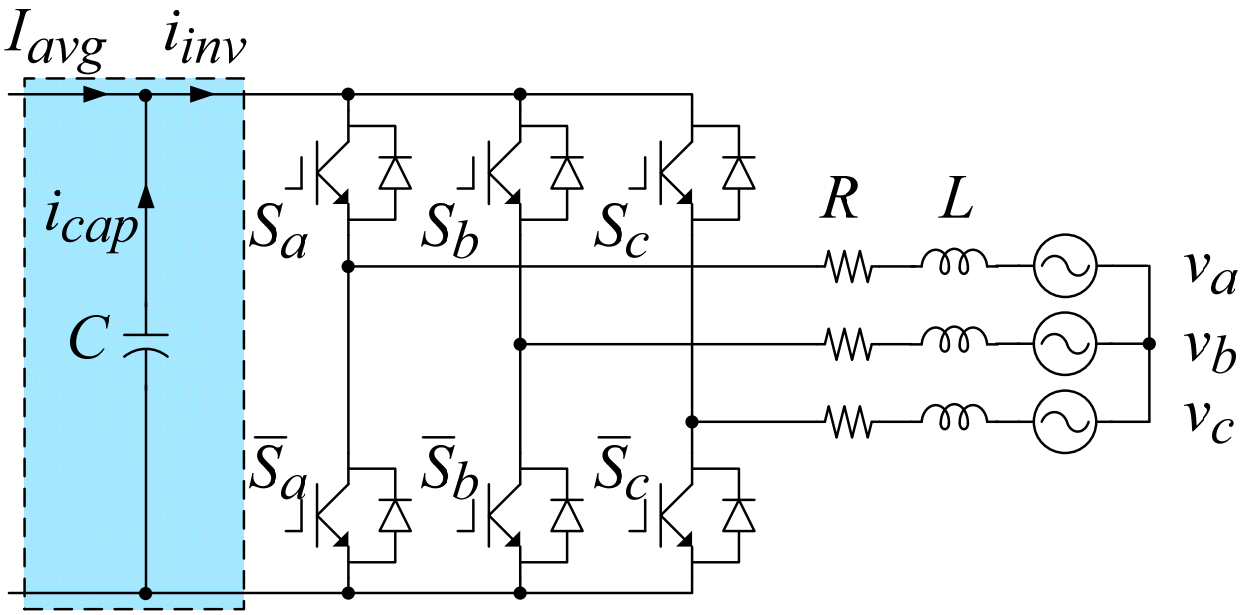

Figure 1.3 The simplified equivalent circuit of the inverter under six-step operation

1.3.3 Diode Rectifier Mode

The last mode is diode rectifier mode. For the PWM rectifier, if all the power switches switch off, and only the freewheeling diodes forced on and off the input voltages, the PWM rectifier becomes an uncontrolled diode rectifier, as shown in Figure 1.4.

If considered PHEV, there is no PWM rectifier connecting the generator/motor to the dc link. However, if considered SHEV, there is a PWM rectifier connecting the generator/motor to the dc link, which at most time rectifies the three-phase ac voltages generated by the generator/motor to dc voltage. As you may notice, this PWM rectifier can work as an uncontrolled diode rectifier, like Figure 1.4.

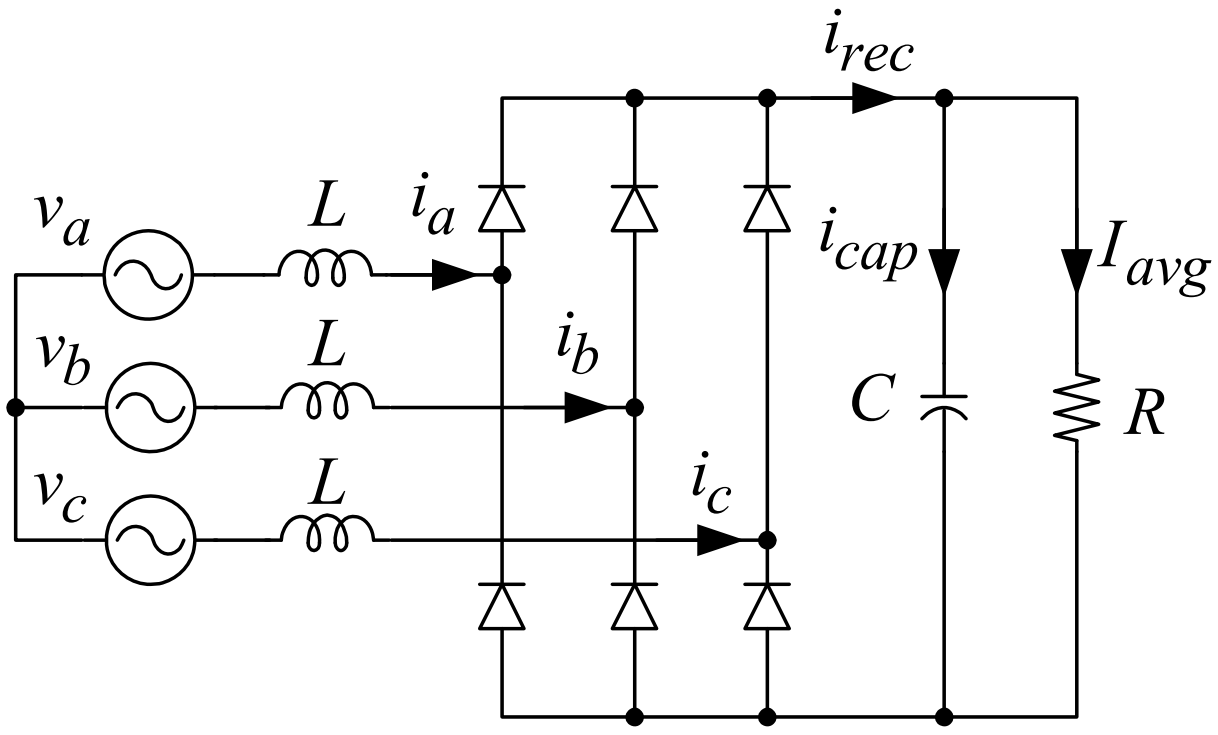

Figure 1.4 The schematic of a three-phase uncontrolled diode rectifier with line impedance on the ac side, and with dc link capacitor and resistive load on the dc side

1.3.4 Synchronization between DC-DC Converter and SPWM Inverter

One last converter that have not been mentioned above is the dc-dc converter that connects the battery—the energy storage system—to the dc link. Therefore, this dc-dc converter contributes a certain amount of current harmonics to the dc link capacitor as well, which results in voltage ripples on the dc link. Consequently, in order to minimize the dc capacitance of the HEV systems, this part should be considered as well, which shows in Figure 1.5.

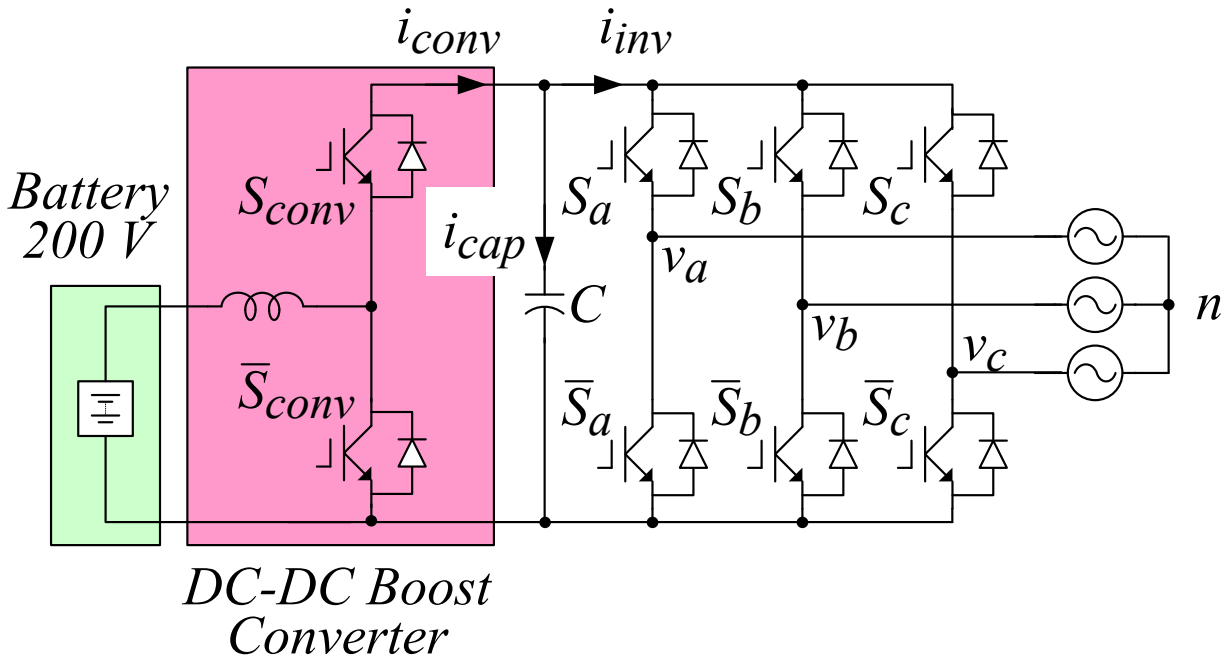

Figure 1.5 The schematic of a bidirectional dc-dc converter connected with a three-phase inverter with three-phase current sources as load

In conclusion, rectifiers and inverters, operated by SPWM and six-step mode, as well as the uncontrolled diode rectifier and dc-dc converter, are discussed in this thesis. Graphs, which show the right capacitance value for a given voltage ripple tolerance, are summarized at the end of each chapter.

1.4 Summary of Previous Work

1.4.1 Complicated AC-DC-AC PWM Converter Control Strategies

One of the typical AC-DC-AC PWM converters (sometimes called AC-AC converter) is shown in Figure 1.6. There are many papers discussing control strategies to reduce ripple current going through the dc link capacitor *C* by making the converter side dc link current the same as the inverter side dc link current, which theoretically needs no capacitance at all. For instance, direct capacitor current control [5], direct instantaneous input/output power balancing [6, 7], four-step commutation strategy [8], space vector modulation strategy [9], output current linearization feedback control (input/output current tracking) [10, 11], nonlinear control [12-14], and some other methods utilizing the current information. Also, there are a large number of papers discussing the matric converter or indirect matrix converter without dc link capacitor [15-17]. Similarly, they are all proposed with complicated close-loop control. However, there are few papers which discuss accurately obtaining the theoretical minimum capacitance for HEV systems by calculating the current ripple going through the dc link capacitor and voltage ripple across the dc link capacitor under open loop condition.

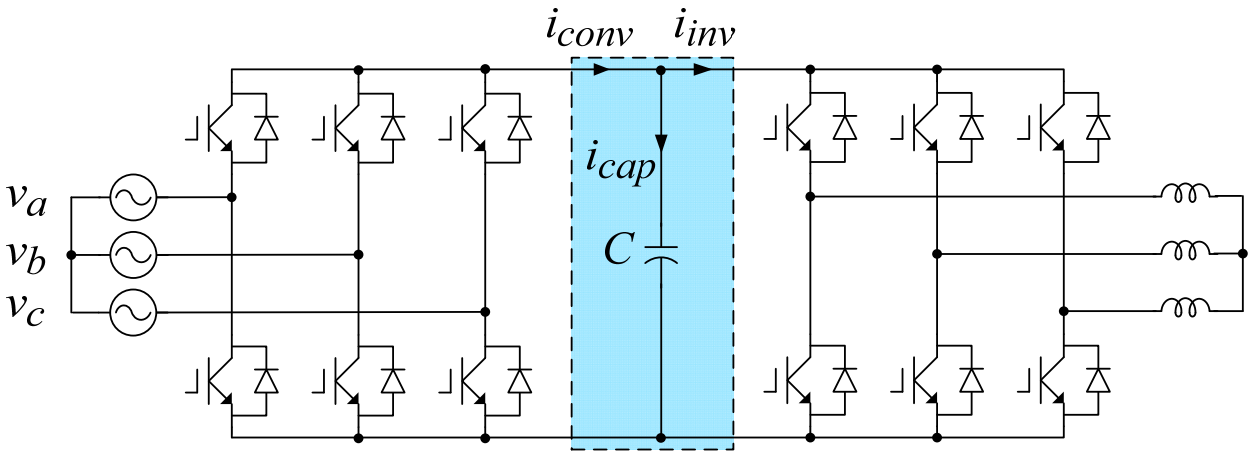

Figure 1.6 The schematic of a typical AC-DC-AC PWM converter system

1.4.2 Theoretical Analysis of Current Ripples and Harmonics of the DC Link Capacitor

Some studies have been done on current ripple and harmonics of the dc link capacitor. For example, [18] is a very good paper about the rms current stress on the dc link capacitor for voltage source inverter (VSI) systems. In addition, [19, 20] are both on the topic of dc link current harmonics analysis. [21] is closer to the designer's viewpoint, but no closed-form equations of current ripple and capacitance value is derived. [22] did not give a theoretical calculation either. These papers provide a theoretical basis of the current ripple and harmonics. However, there are few papers talking about the voltage ripple and harmonics of the dc link capacitor. Also, there are few papers analyzed the current and voltage ripples through the Ampere-Second point of view, which is actually the source of the voltage ripple.

1.4.3 Simple Synchronization between the DC-DC converter and the SPWM Inverter to Minimize the Required Capacitance

In the HEV converter/inverter system, inverters are always connected to dc-dc converters, for the sake of boosting the battery's low dc voltage to high dc voltage, and then converting into ac voltage to drive the traction motors, as shown in Figure 1.5. However, the dc link capacitor bank between the dc-dc converter and the inverter is usually bulky, heavy and expensive. Yet the bottleneck of the capacitor's size is determined by the current ripple requirement rather than the voltage ripple requirement. Hence, a better way to minimize the dc capacitance is narrowed down to minimize the current ripple through the capacitor by synchronizing the dc-dc converter and the SPWM inverter. The PWM and control techniques are fairly important. A good way will help minimizing the capacitance, whereas an unsuccessful one may need more capacitance than the normal operation.

Similar to the condition described in [5], in order to minimize the dc link capacitance between the dc-dc converter and SPWM inverter, making the converter side dc link current i_{conv} equals to the inverter side dc link current i_{inv} in a pulsewidth modulation (PWM) converter-inverter system is the final destination, so that ideally no current will flow through the dc link capacitor and no voltage fluctuation will be across the capacitor, meaning no capacitor needed at all. Till now, most papers that discussed the current ripple reduction and the dc link capacitance minimization are based on the AC-DC-AC PWM converter-inverter systems with relatively complicated close-loop control methods [5-7, 10, 23-25]. The best result that they can achieve is almost without any dc link capacitors. Besides, there are papers discussing innovating PWM strategies only on inverter side allowing reduction of the dc input current ripples [26-28]. Furthermore, for DC-DC-AC PWM converter [29]. However, very few papers have been written

focusing on the current ripple reduction by synchronizing between the DC-DC converter and the SPWM inverter, the so-called DC-DC-AC PWM converters, which is also commonly existed in the HEV systems. [30] was a good start for the synchronization by making the DC-DC converter's switching frequency twice as much as the inverter's switching frequency and optimizing the phase difference of the carrier waveforms between the inverter carrier and DC-DC carrier. This method does decrease the current ripple quite a lot. In spite of this, more improvement can be done.

1.5 Outline of Thesis

When designing a voltage source inverter, the dc link capacitor is an important parameter to the designer. It is always preferred to know the capacitance's per unit value if given a percentage of the tolerable dc link voltage ripple. As a result, once we get a curve showing the relationship between the per unit value of the dc link capacitor and the desired voltage ripple percentage of the dc link, as well as taking consideration of a certain value of power factor, we can easily find out the capacitance by only checking the curve and then multiplying the capacitance base value. This makes life much easier. In conclusion, our task is to find the curve mentioned above, which shows the relationship between the per unit value of the capacitance and the dc link voltage ripple percentage.

For the sake of calculating the capacitance, (1.1) is the basic equation that comes up to one's mind, which express the current going through a capacitor, i_{cap}, is equal to the capacitance, C, times the derivative of the voltage across this capacitor, v_{cap}.

$$i_{cap} = C\frac{dv_{cap}}{dt} \tag{1.1}$$

Extract the capacitance C out of (1.1), one can get (1.2).

$$C = \frac{i_{cap} \cdot dt}{dv_{cap}} \tag{1.2}$$

Let's take a closer look at (1.2), the numerator is $i_{cap} \cdot dt$, which is a current times a time interval. From now on, it will be called "Ampere-Second", short as $A{\cdot}sec$, in this thesis. Moreover, the denominator dv_{cap}, is actually the dc link voltage ripple, due to the assumption that this thesis is only dealing with dc link capacitance calculation.

For the sake of deriving the dc link capacitance, according to (1.2) obtaining an accurate expression, for the $i_{cap} \cdot dt$ —Ampere-Second ($A{\cdot}sec$)—of the ac ripple current i_{cap} that is flowing in and out of the dc link capacitor during one switching cycle, is the key point to get the required dc capacitance per unit (p.u.) value, of a given tolerable voltage ripple value, such as 10%.

Based on the previous discussion about the necessity and importance of finding the minimum dc capacitance for the HEV system, and the previous work that have done by others, here comes the outline of thesis.

Picking a dc link capacitor is decided by two constrains: one is the capacitance which is determined by the voltage ripple; the other one is the rms current ripple across the capacitor for the worst case, which will cause the capacitor internal temperature rise and has to be under a certain value to ensure the proper operation of the ordinary capacitors. Therefore, each chapter will be divided into basically two parts:

1. Calculation of the capacitance with a certain requirement of the voltage ripple endurance;
2. Calculation of the rms current ripple.

Voltage ripple is more directly related to the capacitance, as one can see from (1.3). Therefore, in order to get the minimum capacitance for the system, $i_{cap} \cdot dt$ (Ampere-Second) should be obtained first.

$$C = \frac{i_{cap} \cdot dt}{dv_{cap}} = \frac{i_{cap} \cdot dt}{\varepsilon V_{dc}} \tag{1.3}$$

These calculations have to be done for 3 different topologies that exists in the HEV systems: SPWM inverter (motoring low speed), 6-step inverter (motoring high speed), and diode rectifier (the PWM rectifier without controlling the switches).

In the second chapter, an accurate theory of calculating the dc link capacitor voltage ripple and current ripple for SPWM inverters and PWM rectifiers, which are most commonly used in HEV converter/inverter systems at low speed, is presented in the chapter. Most of all, the results are analyzed and summarized into graphs, which helps to find the right capacitance value for a given voltage ripple tolerance and the rms ripple current that the capacitor has to absorb.

In the third chapter, every goal is the same as chapter 2, and only difference is the topology changing to uncontrolled diode rectifier.

In the fourth chapter, the topology changes to a six-step inverter.

In the fifth chapter, a simple carrier modulation method is proposed to reduce the current and voltage ripple that going through the dc link capacitor. This chapter focuses on comparing different kinds of carrier modulation methods for the dc-dc converter, in order to match with the inverter input current so as to minimize the current ripple that going through the dc link capacitor. Comparing with the conventional triangle carrier or the saw tooth carrier, the proposed simple

carrier modulation is able to help minimizing the current ripple going through the dc link capacitor by a simple and easy implementation without complex close-loop control. The simulation and experimental results are provided to validate the effectiveness of the proposed method.

In this thesis, an accurate theory of calculating the voltage ripples and current ripples of the inverters and converters in HEV systems is presented, respectively. The topologies shown in Figure 1.2 (a) three-phase inverter/PWM rectifier, Figure 1.4 a three-phase uncontrolled diode rectifier, and Figure 1.5 a dc-dc converter, are mainly discussed in this thesis, which are the basic modules for a hybrid electric vehicle, both SHEV and PHEV. The voltage and current ripples of these cases are analyzed and summarized into graphs, which helps one to find the right capacitance value for a given voltage ripple tolerance and the rms ripple current that the capacitor has to absorb. Experiments are demonstrated with 510 μF of dc link capacitance for a 150 kVA inverter, and the results verify the derived expressions.

CHAPTER 2 DC Capacitance and Current Ripple Requirement of the Three-Phase SPWM Inverter/PWM Rectifier

Chapter 1 gives a general idea of why we need to minimize the dc link capacitor for HEV converter/inverter systems, and four topologies that are going to be discussed in this thesis. In this chapter, the objective is to find the requirement of the dc link capacitance and the current ripple for a three-phase SPWM inverter or a three-phase PWM rectifier. In fact, in terms of influence to the dc link capacitor voltage and current ripple, these two topologies are inherently the same. Therefore, only one needs to be analyzed, and the detailed analysis in this chapter is based on SPWM inverter [31].

In order to make the conclusions more general and convenient for other designers to apply to their own applications, the results of the dc link capacitance requirement are analyzed and summarized into graphs at the end of this chapter according to the proposed accurate theory. The conclusive graphs can help to find the right capacitance value for a given voltage ripple tolerance and the rms current ripple that the capacitor has to absorb for different power factors.

Finally, this chapter ends up with the experimental results from a 150 kVA inverter prototype, which proves the calculation result and experimental result are in close agreement.

First of all, let's start from the first topology in Figure 1.2—the three-phase SPWM inverter/rectifier. (For convenience, Figure 1.2 is redrawn here as Figure 2.1 on the next page.)

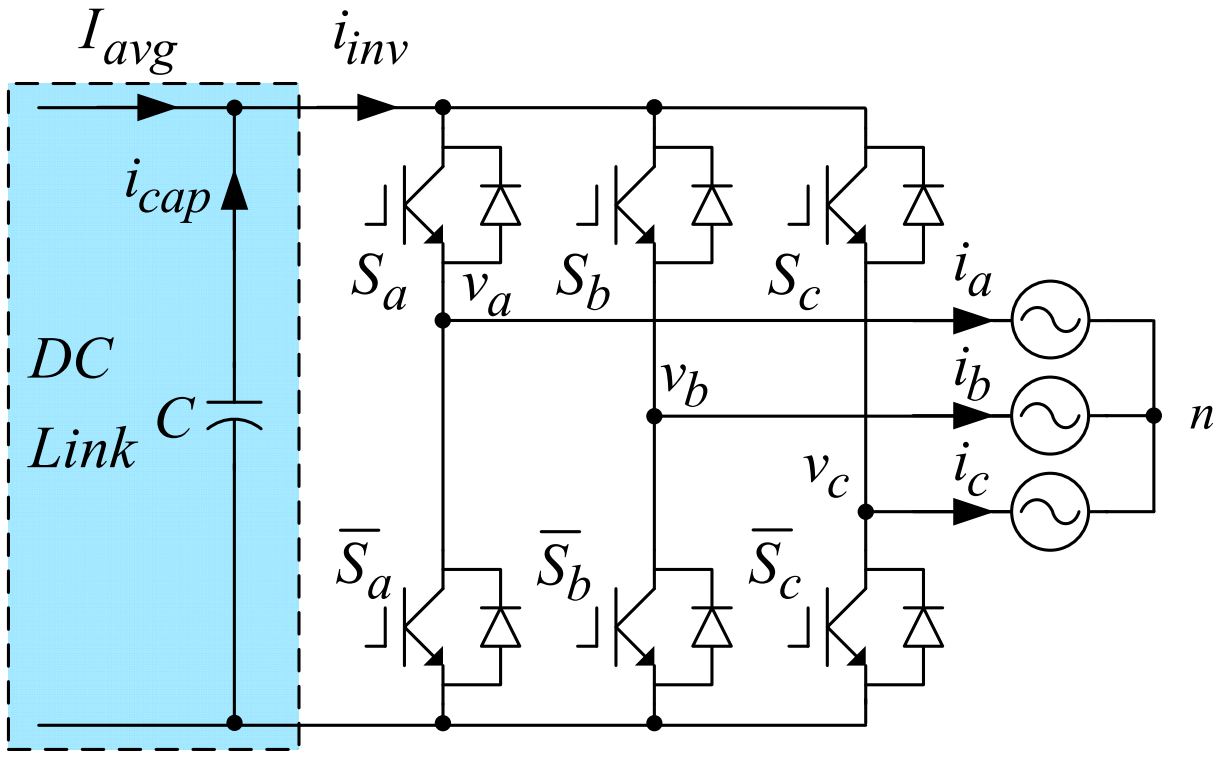

Figure 2.1 The schematic of a three-phase inverter/PWM rectifier using SPWM with three-phase current sources as load

2.1 Basic Idea of Calculating DC Link Capacitance

As mentioned in Chapter 1, for the sake of calculating the capacitance, (2.1) is the basic equation that comes up to one's mind, which express the current going through a capacitor, i_{cap}, is equal to the capacitance, C, times the derivative of the voltage across this capacitor, v_{cap}.

$$i_{cap} = C\frac{dv_{cap}}{dt} \tag{2.1}$$

Extract the capacitance C out of (2.1), one can get (2.2).

$$C = \frac{i_{cap} \cdot dt}{dv_{cap}} \tag{2.2}$$

In (2.2), the denominator, voltage ripple across the capacitor, dv_{cap}, is usually known for a design. In general, the smaller the capacitance is, the bigger the voltage ripple is. As a result, the bigger the voltage ripple on the dc link, the more harmonics goes to the ac side load. However, we want both small capacitor and low harmonics to the load. Obviously, there is a tradeoff between the two. This tradeoff is determined by the designer's target. Hence, this voltage ripple factor is considered a constant in the followed calculation.

Therefore, according to (2.2) and explanation in the above paragraph, the required dc capacitance C is proportional to the numerator, $i_{cap} \cdot dt$, which is called Ampere-Second ($A \cdot sec$) in the later paragraphs.

In conclusion, an accurate expression for the minimum required dc link capacitance can be obtained by finding an accurate $A \cdot sec$ expression of the ac ripple current i_{cap}, where i_{cap} represents the current going in and out of the dc link capacitor.

As explained above, the most challenging part of this calculation is to find an expression for $A \cdot sec$. This is achieved by integrating the positive/negative part of i_{cap} in one switching period. Obviously, if i_{cap} is integrated during one switching cycle, the result is zero because the dc link capacitor does not have a dc current offset, otherwise the dc link voltage will keep increasing and finally blow up the capacitor. That is why integrating the whole switching cycle does not help. Therefore, integrating either positive or negative part is the target.

2.2 Theoretical Basis

Figure 2.1 shows the schematic of a three-phase SPWM inverter/PWM rectifier with dc link capacitor and three-phase load/current source. Let's take a close look at this figure. First of all, it is desired to decompose the ideal inverter input current i_{inv} into two parts.

- A constant dc current I_{avg} is assumed to be supplied by a dc current source, which does not introduce any other current ripples. It can be imagined as a diode rectifier in series with a huge inductor. Although this does not really exist in the HEV system nowadays, the purpose of this assumption is eliminating all current ripples that coming from other sources, but only focusing on the current ripples that come from the SPWM inverter side, as shown in Figure 2.1.
- As one may already know, the other part of the ideal inverter input current i_{inv} is the ac ripple current i_{cap}, which flows in and out of the dc link capacitor bank, whose average is zero in every switching cycle and of course every fundamental cycle as well.

Therefore, I_{avg} is equal to the average of i_{inv}.

2.2.1 Switching Functions

First of all, assume the rms value of the inverter output line-to-line voltage is V_{ac}, the 3rd harmonic injection is $v_{3\omega}$ (the same to all three phases), the fundamental frequency in radian is

ω, the rms value of the inverter output line current is I_{ac}, the modulation index is M, and the power factor angle is ϕ.

The inverter three-phase output voltages v_{an}, v_{bn} and v_{cn} in Figure 2.1 can be expressed as shown in (2.3). Understand that the inverter three-phase output voltages are PWM waveforms. Equation (2.3) only shows their fundamental components. That is why they are sinusoidal expressions, without the summation of any higher order of sine terms.

$$\begin{aligned} v_{an} &= \frac{\sqrt{2}}{\sqrt{3}} V_{ac} \sin(\omega t) + v_{3\omega} \\ v_{bn} &= \frac{\sqrt{2}}{\sqrt{3}} V_{ac} \sin(\omega t - \frac{2}{3}\pi) + v_{3\omega} \\ v_{cn} &= \frac{\sqrt{2}}{\sqrt{3}} V_{ac} \sin(\omega t + \frac{2}{3}\pi) + v_{3\omega} \end{aligned} \tag{2.3}$$

Secondly, the inverter three-phase output currents i_a, i_b and i_c are all perfect sinusoidal currents. For one thing, it is relatively reasonable because the traction motors are usually equivalent to huge inductors, which are enough to smooth out most of the ripples. For another thing, similar as previous explanation, it is desired to eliminate all the other ripples influence, and only focus on the ripples that generated by the SPWM operation method.

Similarly, the inverter output three phase currents i_a, i_b and i_c can be expressed as shown in (2.4), where they are assumed to be perfect sinusoidal currents.

$$\begin{aligned} i_a &= \sqrt{2} I_{ac} \sin(\omega t - \phi) \\ i_b &= \sqrt{2} I_{ac} \sin(\omega t - \phi - \frac{2}{3}\pi) \\ i_c &= \sqrt{2} I_{ac} \sin(\omega t - \phi + \frac{2}{3}\pi) \end{aligned} \tag{2.4}$$

From Figure 2.2 and the proof in the Appendix, the switching functions of the three upper switches S_a, S_b and S_c are obtained in (2.5).

$$\begin{aligned} S_a &= \frac{1}{2} + \frac{1}{2} M \sin \omega t + \frac{v_{3\omega}}{V_{dc}} \\ S_b &= \frac{1}{2} + \frac{1}{2} M \sin(\omega t - \frac{2}{3}\pi) + \frac{v_{3\omega}}{V_{dc}} \\ S_c &= \frac{1}{2} + \frac{1}{2} M \sin(\omega t + \frac{2}{3}\pi) + \frac{v_{3\omega}}{V_{dc}} \end{aligned} \tag{2.5}$$

2.2.2 Relationship between V_{dc} and V_{ac}

Please note that the dc link voltage has a relationship with the ac output line-to-line voltage as shown in (2.6), under both normal modulation and over modulation, which means $M \in [0, 1.15]$.

$$M \frac{V_{dc}}{2} = \frac{\sqrt{2}}{\sqrt{3}} V_{ac} \tag{2.6}$$

2.2.3 Average Current

The input real power of the inverter on the dc side can be expressed as (2.7).

$$P_{dc} = V_{dc} I_{avg} \tag{2.7}$$

The output real power of the inverter on the ac side can be expressed as (2.8).

$$P_{ac} = \sqrt{3} V_{ac} I_{ac} \cos \phi \tag{2.8}$$

The efficiency of the inverter is usually above 90%. This means the power loss is relatively small comparing to the total power. Therefore, if the power loss in the inverter is ignored, the input real power is equal to the output real power, as shown in (2.10).

$$V_{dc} I_{avg} = \sqrt{3} V_{ac} I_{ac} \cos\phi \tag{2.9}$$

Put I_{avg} on one side of the equation, and others on the other side. Equation (2.10) can be obtained.

$$I_{avg} = \sqrt{3} \frac{V_{ac}}{V_{dc}} I_{ac} \cos\phi \tag{2.10}$$

Hence, substituting (2.6) into (2.10), the average current (2.11) is obtained.

$$I_{avg} = \frac{3\sqrt{2}M}{4} I_{ac} \cos\phi \tag{2.11}$$

Similarly, the average current expression (2.11) can be achieved by substituting (2.4) and (2.5) into (2.12) as well, which means the switching functions shown in (2.5) are actually indicating the average duty cycle in each switching cycle.

$$I_{avg} = S_a i_a + S_b i_b + S_c i_c \tag{2.12}$$

2.3 Calculation of Required DC Link Capacitance

Figure 2.2 shows the PWM switching details during two switching cycles. Figure 2.2 (b) (c) (d) shows the switching functions of three phases determined by the traditional SPWM strategy, whose duty cycle in each switching period can be calculated from (2.5). In addition, Figure 2.2 (e) is the ideal inverter input current i_{inv}. As it is assumed the inverter is fed by a constant current source of I_{avg}, it can be understood that the current waveform that is flowing in and out of the dc link capacitor bank, i_{cap}, is the waveform in (e), but with I_{avg} as the x-axis instead of 0.

Instead of looking at the whole 360°, it is the same to analyze only 60°, for the reason that the waveforms are repeated in a low frequency at 6ω due to the three-phase system. Therefore, the following analysis will only focus on the range of 30° to 90° (take v_a as a reference), where $v_a > v_c > v_b$, drawed in pink (or shaded area) in Figure 2.3.

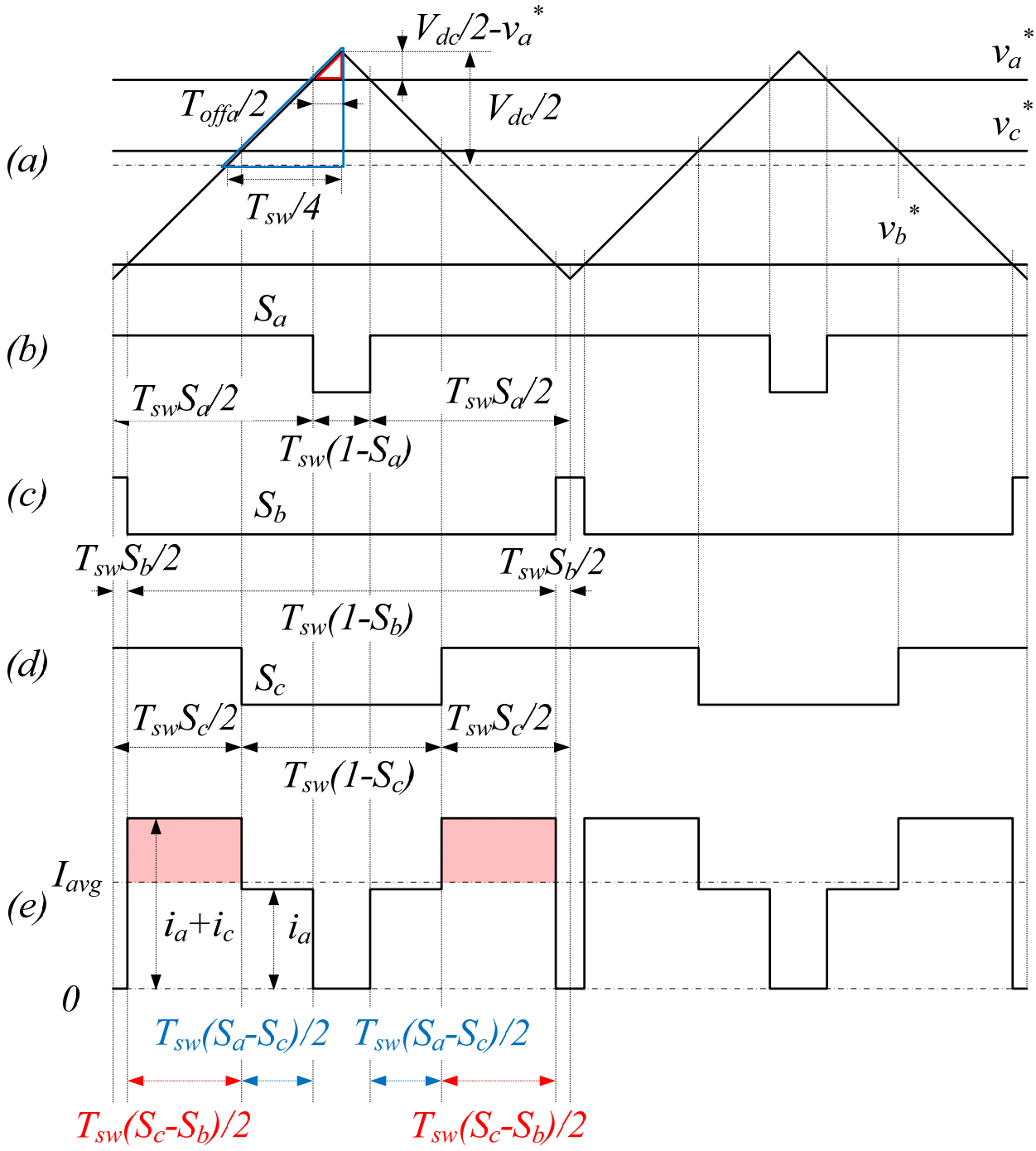

Figure 2.2 Detailed PWM waveforms in two switching periods
(a) sinusoidal reference and triangle carrier waveforms;
(b) switching function of phase A;
(c) switching function of phase B;
(d) switching function of phase C;
(e) ideal inverter input current i_{inv} with I_{avg} showing in the same graph.

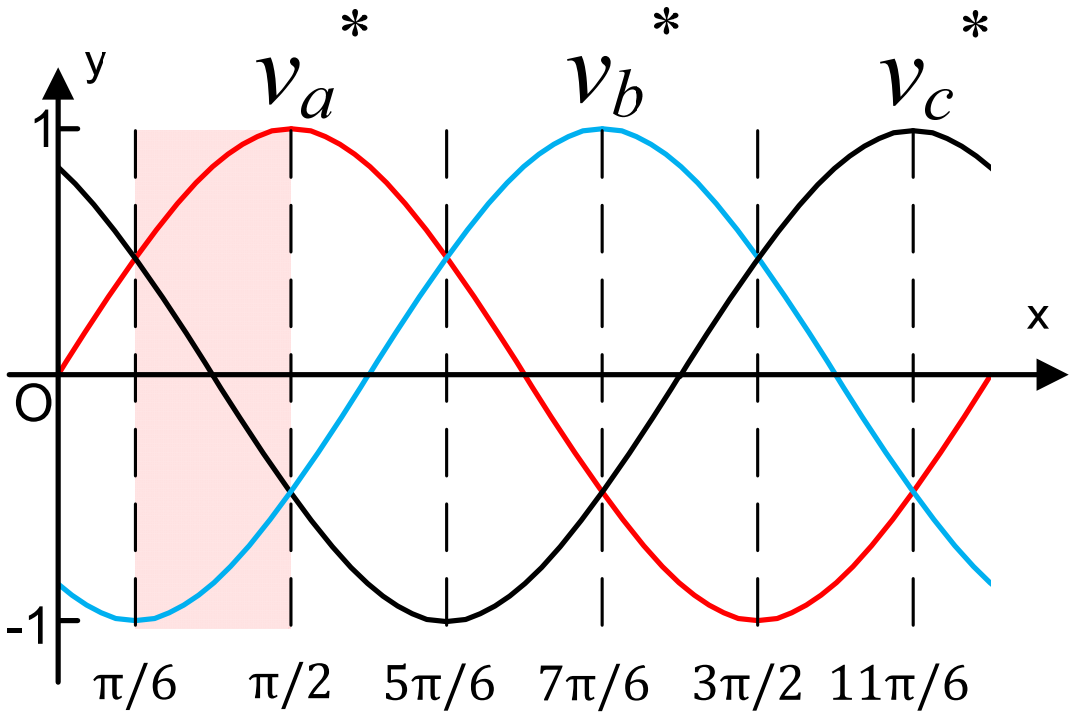

Figure 2.3 Six sectors for voltage references of phase A, B and C

From Figure 2.2(e), it is obvious to calculate $A \cdot sec$ by integrating the positive/negative half of i_{cap} during one switching period. If using the positive half, the expression for the area of the shaded blocks will be

$$A \cdot sec = T_{sw}(S_c - S_b)(i_a + i_c - I_{avg}) \tag{2.13}$$

By substituting (2.4), (2.5) and (2.11) into (2.13), we can get (2.14).

$$A \cdot sec = \frac{\sqrt{6}}{2} I_{ac} T_{sw} M \cos(\omega t)\left[\sin(\omega t - \phi + \frac{\pi}{3}) - \frac{3}{4} M \cos\phi\right] \tag{2.14}$$

As one can tell from (2.11), I_{avg} is related to power factor (pf) and modulation index (M). Therefore, if either of the two decreases, I_{avg} will decrease, which leads to the equation expressing the $A \cdot sec$ to be different, due to different blocks are involved into (2.13).

Here is the conclusion: during this 60°, $A{\cdot}sec$ is actually a piecewise function related to M, pf, rms line current, switching frequency and instantaneous time. For example, if it is assumed M=1 when pf=1, there are three expressions for $A{\cdot}sec$ listed in Table 2.1. The expression of $A{\cdot}sec$ is basically changing with the I_{avg} value level, depending on whether it is bigger or smaller than i_a or $i_a + i_c$. As mentioned before, pf can change the I_{avg} value, therefore the expression of Asec changes with pf. As pf decreases from unity to zero, the number of Asec expressions decreases from three to one as well, such as:

- pf=1, it has all three Asec expressions;
- pf=0.866, it has the first two Asec expressions;
- pf=0, it only has the first Asec expression;

Similarly, as M can modify the I_{avg} value as well, the expression of $A{\cdot}sec$ changes with M as expected. However, no matter what the condition is, the expression of $A{\cdot}sec$ will not come out from these three expressions.

Table 2.1 Expressions of $A{\cdot}sec$ ($v_a > v_c > v_b$)

Range	$A{\cdot}sec$	No.
$i_a < I_{avg} < i_a + i_c$	$T_{sw}(S_c - S_b)(i_a + i_c - I_{avg})$	Expression 1
$I_{avg} < i_a < i_a + i_c$ $I_{avg} < i_a + i_c < i_a$	$T_{sw}\left[(S_c - S_b)(i_a + i_c - I_{avg}) + (S_a - S_c)(i_a - I_{avg})\right]$ $= T_{sw}(1 - S_a + S_b)I_{avg}$	Expression 2
$i_a + i_c < I_{avg} < i_a$	$T_{sw}(S_a - S_c)(i_a - I_{avg})$	Expression 3

In conclusion, expression 1 will be effective for any pf and *M*. Expression 2 and expression 3 are only valid for pf=1 with any *M*. Table 2.2 shows the simplified expressions of $A \cdot sec$ by substituting (2.4) and (2.5) into Table 2.1.

Table 2.2 Simplified Expressions of $A \cdot sec$ ($v_a > v_c > v_b$)

Range	$A \cdot sec$	No.
$i_a < I_{avg} < i_a + i_c$	$\frac{\sqrt{6}}{2} I_{ac} T_{sw} MI \cos(\omega t) \left[\sin(\omega t - \phi + \frac{\pi}{3}) - \frac{3}{4} MI \cos\phi \right]$	Expression 1
$I_{avg} < i_a < i_a + i_c$ $I_{avg} < i_a + i_c < i_a$	$\frac{\sqrt{6}}{2} I_{ac} T_{sw} MI \cos\phi \left[\frac{\sqrt{3}}{2} - \frac{3}{4} MI \sin(\omega t + \frac{\pi}{6}) \right]$	Expression 2
$i_a + i_c < I_{avg} < i_a$	$\frac{\sqrt{6}}{2} I_{ac} T_{sw} MI \cos(\omega t + \frac{\pi}{3}) \left[\frac{3}{4} MI \cos\phi - \sin(\omega t - \phi) \right]$	Expression 3

2.3.1 Maximum $A \cdot sec$ during 60° with the Same Power Factor and Modulation Index

When pf=0, expression 1 becomes (2.15).

$$A \cdot sec = \frac{\sqrt{6}}{2} I_{ac} T_{sw} M \cos(\omega t) \sin(\omega t - \frac{\pi}{6}) \tag{2.15}$$

The maximum Asec during 60°, with the same pf and *M*, can be found by taking the partial derivative of (2.15) with respect to ωt.

Assume (2.16) to make things easier.

$$k = \sqrt{2} I_{ac} T_{sw} \tag{2.16}$$

The derivative can be expressed as (2.17).

$$\frac{d}{d\omega t} A \cdot sec = kM \cos(2\omega t - \frac{\pi}{6}) \tag{2.17}$$

Therefore, within the appropriate range of ωt, equation (2.18) can be derived. $m=1$ and $\omega t=\pi/3$ will give $A \cdot sec$ maximum value, where m is an integer in (2.18).

$$\omega t = m\frac{\pi}{2} - \frac{\pi}{6} = \frac{\pi}{3} \tag{2.18}$$

Put (2.18) back into (2.15),

$$A\sec = \frac{1}{4}\frac{\sqrt{3}}{2} kM \tag{2.19}$$

Equation (2.19) is drawn as the red line in Figure 2.5 by varying M from 0 to 1. If it is assumed that the base $A \cdot sec$ is (2.20), $A \cdot sec$ max can be derived in a per unit form as (2.21).

$$A \cdot sec_{base} = \sqrt{2} I_{ac} T_{sw} \tag{2.20}$$

$$A \cdot sec_{\max\ p.u.} = \frac{1}{4}\frac{\sqrt{3}}{2} M \tag{2.21}$$

Since Table 2.2 expression 2 is valid for pf=1, it is easier than Table 2.2 expression 1 to manipulate. In expression 2, please note that the term, that has ωt, has a negative sign in front, which will yield the minimum instead.

In this case, observation is necessary. For the expression 2, finding the minimum of sine will give a maximum value. $\omega t=\pi/6$ or $\pi/2$ will give the maximum Asec value.

The expression becomes (2.22).

$$A\sec_{\max} = \frac{\sqrt{6}}{2} I_{ac} T_{sw} M \cos\phi \left[\frac{\sqrt{3}}{2} - \frac{3}{4} M \sin(\frac{\pi}{3}) \right] \tag{2.22}$$

With (2.20), $A \cdot sec$ p.u. is obtained in (2.23).

$$A \cdot sec_{\max\ p.u.} = \frac{\sqrt{3}}{2} M \cos\phi \left[\frac{\sqrt{3}}{2} - \frac{3}{4} M \sin(\frac{\pi}{3}) \right] \tag{2.23}$$

In conclusion, the maximum Asec, standing for voltage ripple, can be expressed in (2.21) when pf=0 and in (2.23) when pf=1.

Similarly, the other power factors can be analyzed in the same way. However, it is a little bit harder to find the roots than the two shown here, since they will become a 4^{th} order polynomials.

Nevertheless, MATLAB can be used to achieve these solutions. Figure 2.4 shows the flowchart of calculating one point on Figure 2.5, such as on the pf=*u* line with M=*x*.

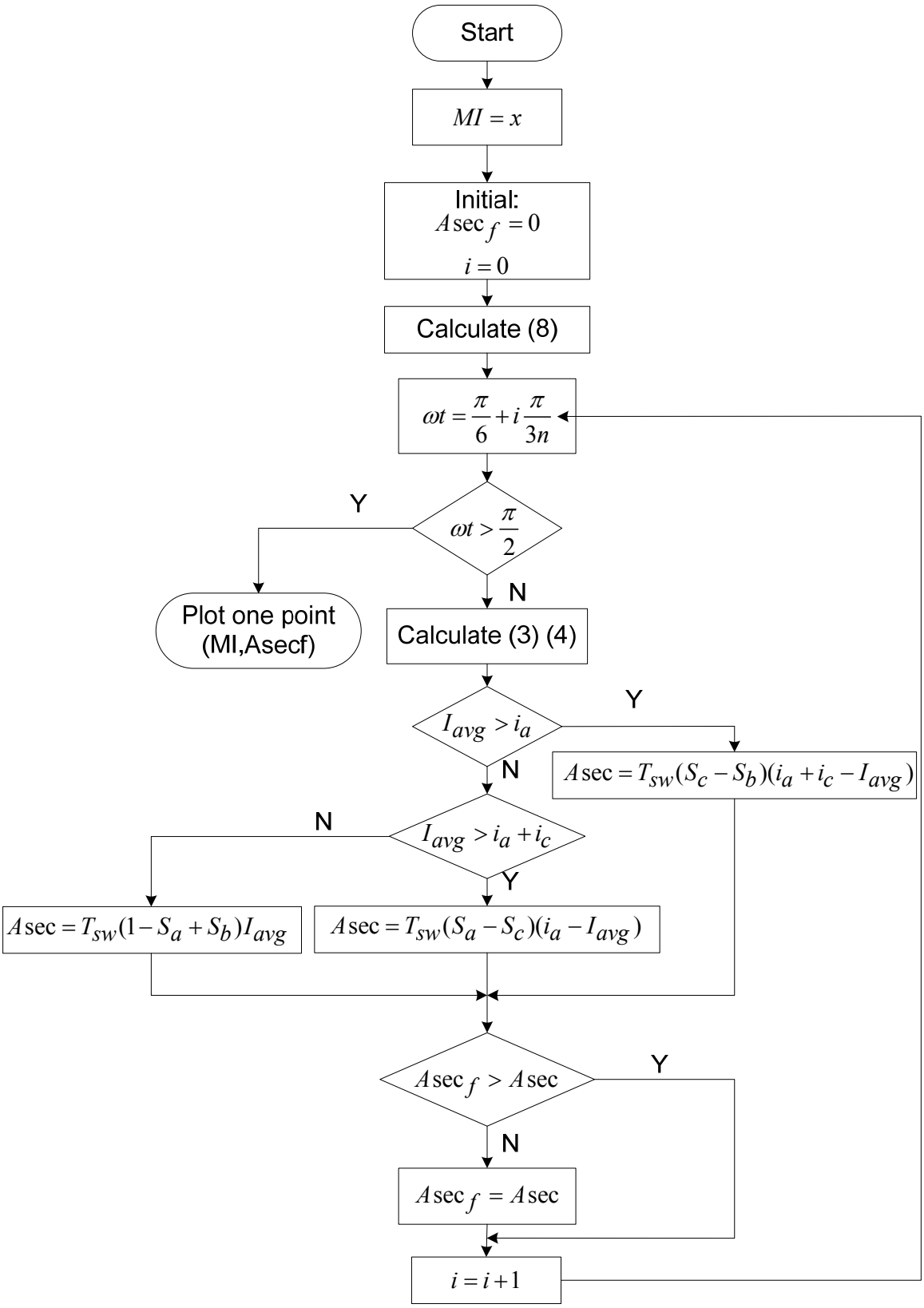

Figure 2.4 The flowchart of calculating the maximum Asec during 60° at a certain value of MI and pf

In the flowchart, n is the number of the switching cycles in 60° of the fundamental cycle, shown in (2.24).

$$n = \frac{f_{sw}}{f_{ref}} \tag{2.24}$$

f_{sw} is the switching frequency and f_{ref} is the fundamental frequency.

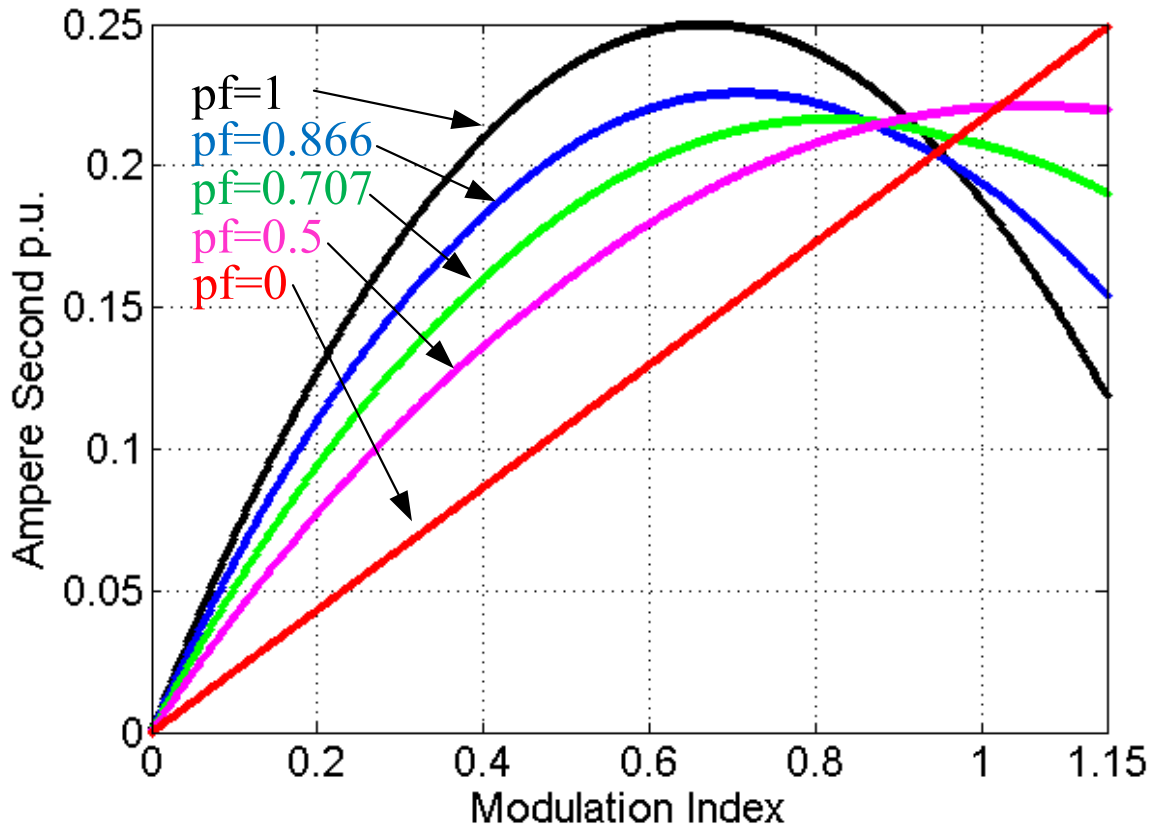

Figure 2.5 The relationship between Modulation Index (M) and Ampere Second ($A{\cdot}sec$)

Therefore, by varying M and pf, Figure 2.5 is obtained, which shows the relationship between the $A{\cdot}sec$ and modulation index by varying the pf from 0 to 1.

Please note that the three expressions shown in Table 2.1 possess a "$S_i - S_j$" term, so $v_{3\omega}$ in (2.5) disappears in the *A·sec* expression, meaning the voltage ripple will not be influenced by the 3rd harmonic injection. This happens to the current ripple as well, as one can see from section 2.4.

2.3.2 Maximum *A·sec* versus Power Factor

The maximum Asec at different power factor points must be determined, since it is necessary to consider the worst case when selecting capacitance values. For instance, this can be achieved by taking the partial derivative of (2.21) and (2.23) with respect to *M* for pf=0 and pf=1 respectively. Therefore, when pf=0 and *M*=1.15, *A·sec* reaches its maximum, while when pf=1, (2.25) is achieved.

$$\cos\phi - \frac{3}{2} M \cos\phi = 0 \tag{2.25}$$

If pf=$\cos\phi$=1, *M*=2/3 will give the maximum *A·sec*, which can be noticed in Figure 2.5 as well.

Finally, in order to get the per unit value of the desired capacitance, it is necessary to define the capacitance base formula. For the sake of eliminating the power rating of the inverter, C_{base} can be defined as (2.26).

$$C_{base} = \frac{\sqrt{3} I_{ac}}{2\pi f V_{ac}} \tag{2.26}$$

Considering V_{dc} is always constant, while V_{ac} is varied with frequency by changing the MI, C_{base} can be expressed using V_{dc} instead by substituting (2.6) into (2.26). Eq.(2.27) is obtained.

$$C_{base} = \frac{\sqrt{2} I_{ac}}{\pi f V_{dc} M} \tag{2.27}$$

In order to calculate (2.27), one has to find the maximum point for each pf on Figure 2.5 and record the specific M for that maximum point, as Table 2.3 shows.

Table 2.3 The M at the maximum *A·sec* for each pf

pf	**M**
1.000	0.667
0.866	0.744
0.707	0.816
0.500	1.150
0.000	1.150

Assume is Δv_{dc} the tolerable voltage ripple that the system requires, and ε is the voltage ripple percentage. The capacitance can be calculated through (2.28).

$$C = \frac{A\sec_{\max}}{\Delta v_{dc}} = \frac{A\sec_{\max}}{\varepsilon \cdot V_{dc}} \tag{2.28}$$

Therefore, the per unit value of the capacitance can be expressed as (2.29).

$$C_{p.u.} = \frac{f_{ref} A\sec_{\max}}{\sqrt{2} I_{ac}} \frac{\pi M}{\varepsilon} \tag{2.29}$$

Figure 2.6 shows the relationship between the per unit value of the desired capacitance $C_{p.u.}$ and a given DC link voltage ripple requirement ε.

Please note that Figure 2.6 is under the condition of switching at 5 kHz and having a fundamental frequency at 200 Hz because the experiment is under this condition and will be easier to compare later on.

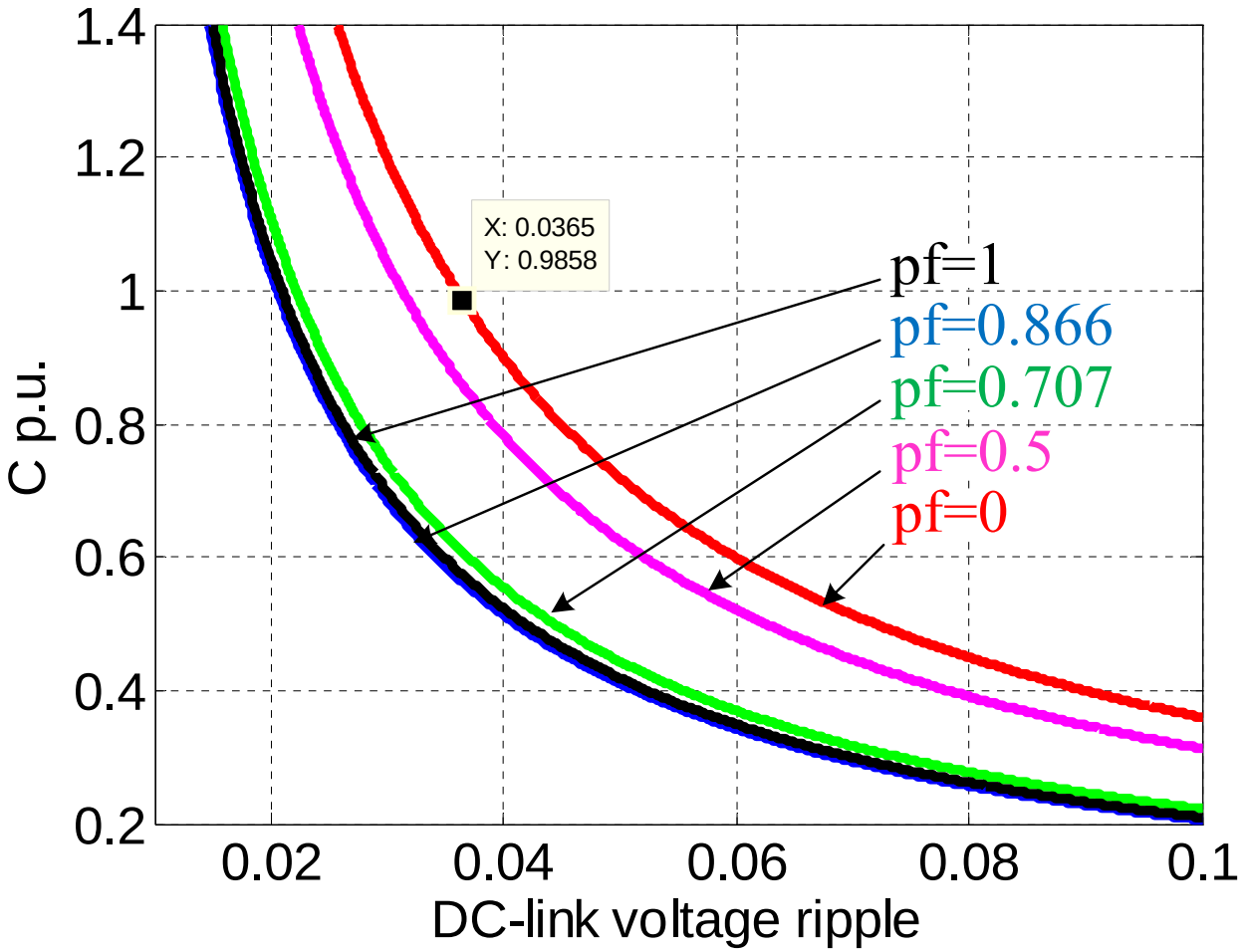

Figure 2.6 The relationship between per unit value of desired capacitance ($C_{p.u.}$) and DC link voltage ripple (ε)

2.4 Calculation of RMS Value of DC Current Ripple (ΔI_{rms})

Most dc ripple current has to be absorbed by the dc capacitor, which is also one of the most important factors for capacitor design and selection. For SPWM inverters, it is clear that calculating the rms current will be very similar to Asec. Eq.(2.30) can be obtained from Figure 2.2(e).

$$I_{rms}{}^2 = \frac{3}{\pi}\int_{\frac{\pi}{6}}^{\frac{\pi}{2}} \left\{ \begin{array}{l} (S_c - S_b)\left(i_a + i_c - I_{avg}\right)^2 \\ +\left(S_a - S_c\right)\left(i_a - I_{avg}\right)^2 \\ +\left(1 - S_a + S_b\right) I_{avg}{}^2 \end{array} \right\} d\omega t \tag{2.30}$$

By combining with (2.4), (2.5) and (2.11), eq. (2.31) is achieved.

$$I_{rms}{}^2 = \frac{3}{\pi}\left\{ \begin{array}{l} -\frac{\sqrt{3}}{12} M \cdot I_{ac}{}^2 \left[-4\cos(2\phi) + 3\sqrt{3}\pi M \cos^2\phi - \frac{27}{4}\cos^2\phi M^2 - 6 \right] \\ +\left(\frac{3\sqrt{2}}{4} I_{ac} \cos\phi M \right)^2 \left(\frac{\pi}{3} - \frac{\sqrt{3}}{2} M \right) \end{array} \right\} \tag{2.31}$$

It can be simplified to (2.32), which has been proved in [18] by Dr. Kolar. The agreement further proved both equations correctness.

$$I_{rms}{}^2 = 4 I_{ac}{}^2 M \left[\frac{\sqrt{3}}{4\pi} + \cos^2\phi \left(\frac{\sqrt{3}}{\pi} - \frac{9}{16} M \right) \right] \tag{2.32}$$

$v_{3\omega}$ does not appear in (2.31), which is the same as the three expressions in Table 2.2. This means the I_{rms} is not influenced by the 3rd harmonic injection, but varies with *MI* and power

factor. Please note that during over modulation operation, the expression of I_{rms} remains the same, as $A \cdot sec$ does. The only difference is that the MI is extend from 1 to 1.15.

The p.u. value of I_{rms} versus MI is summarized in Figure 2.7 for SPWM, and for the sake of comparison, simulation results of several six-step operation points are also shown.

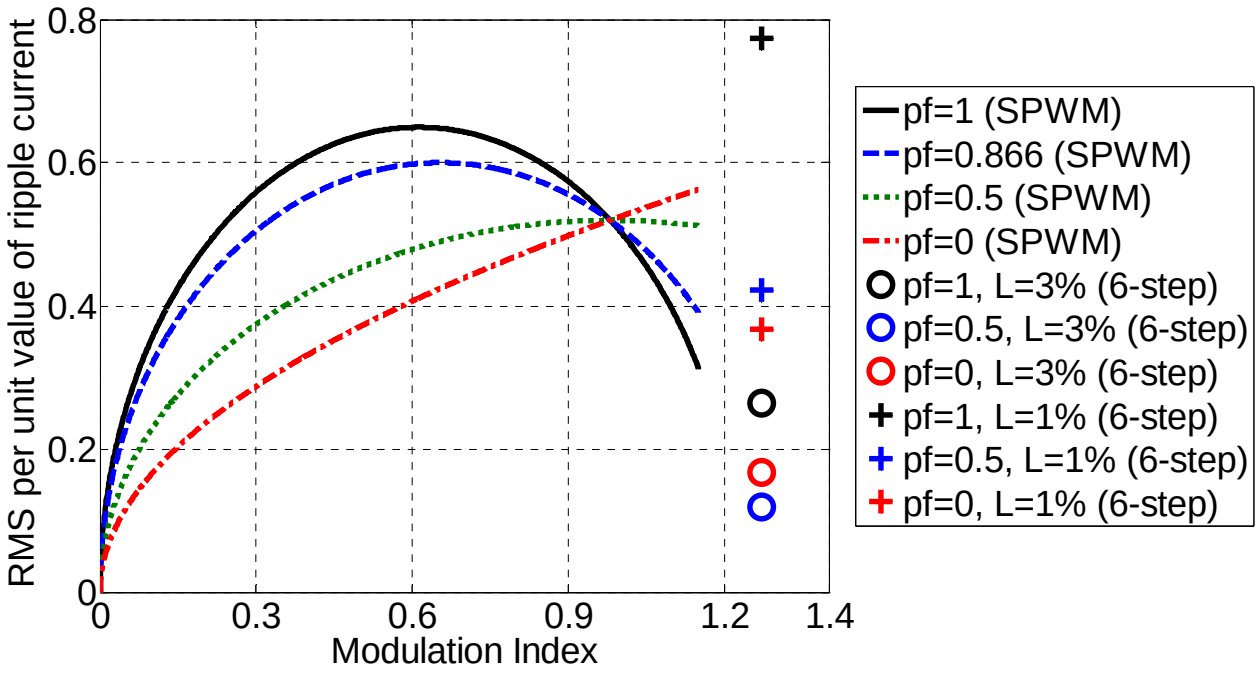

Figure 2.7 The relationship between the p.u. value of I_{rms} versus MI with different power factors for SPWM and 6-step operations

CHAPTER 3 DC Capacitance Requirement of the Three-Phase Diode Rectifier

The previous chapter is about the SPWM inverter/PWM rectifier. In this chapter, the dc capacitance and current ripple will be calculated for the traditional diode rectifier.

The three-phase diode rectifier is not specially built in a HEV system. However, every IGBT has a freewheeling diode paralleled with it. Therefore, when the traction motor is doing regenerative breaking, the energy from the motor will have to be sent back to the dc link side and intended to store in the battery or any other energy storage system connected on the other side of the dc-dc converter. When the firing angle is 0, that is to say, there is no control for the switches, but only the diodes, the converter is an uncontrolled diode rectifier as shown in Figure 1.4. Also, when the generator on the engine side is generating power, the PWM rectifier can work as a diode rectifier if there are no switching signals sent to the IGBTs.

In conclusion, in the HEV system, even if there is no diode rectifier purely consisted with diodes, the diode rectifier is still existed because of the freewheeling diode of the IGBT.

3.1 Introduction

Generally speaking, based on if there is current commutation when the phase current shifts, the diode rectifier can be divided into three cases:

a) Without line inductance;

b) With a small line inductance;

c) With a big line inductance.

How to determine this critical point between small and big inductance is the first question.

3.2 Calculation of the Critical Inductance

At this critical point, the output current i_d is between discontinuous current mode (DCM) and continuous current mode (CCM), where no phase current commutation happens. Therefore, there are always two diodes on at the same time, as shown in Figure 3.1. Therefore, (3.1) can be obtained from Figure 3.1.

$$v_{ab} - 2L\frac{di_{d2}}{dt} = V_{dc} \tag{3.1}$$

Assume α is the angle when the line current starts to rise from 0, as shown in Figure 3.3. Since current begins to flow only when the line-to-line voltage v_{ab} becomes equal to the dc link voltage, (3.2) is true.

$$\cos\alpha = \frac{V_{dc}}{\sqrt{2}V_{ac}} \tag{3.2}$$

Hence, by doing integration from 0 to t of (3.1), i_{d2} can be expressed as (3.3).

$$i_{d2} = \frac{1}{2L}\left\{\frac{\sqrt{2}V_{ac}}{\omega}\left[\sin(\omega t - \alpha) - \sin(-\alpha)\right] - V_{dc}t\right\} \tag{3.3}$$

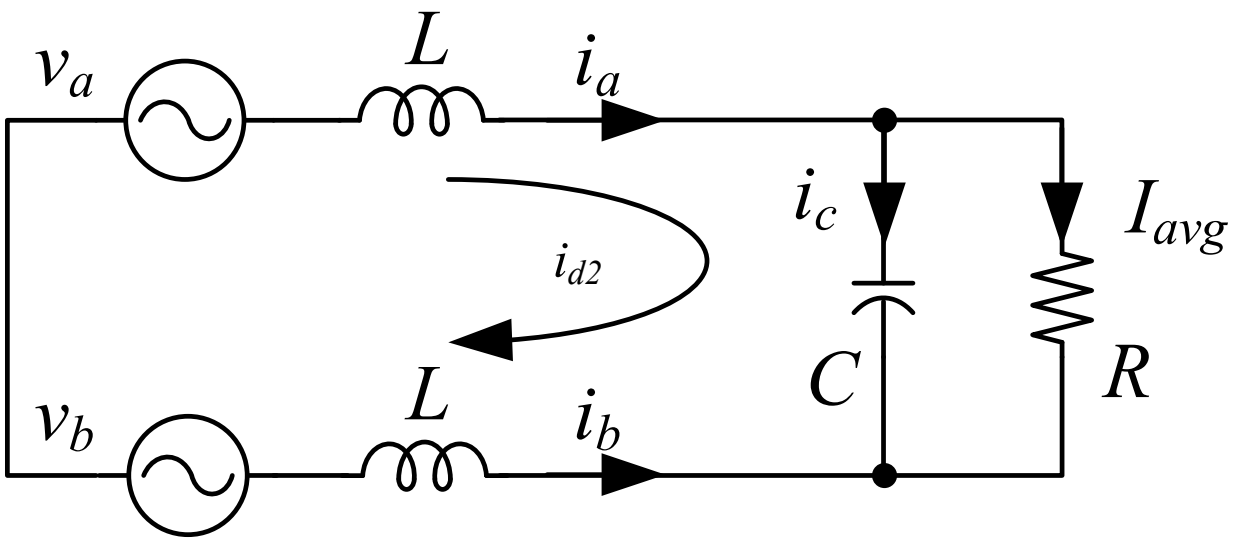

Figure 3.1 Simplified diode rectifier circuit with no line inductance or small line inductance

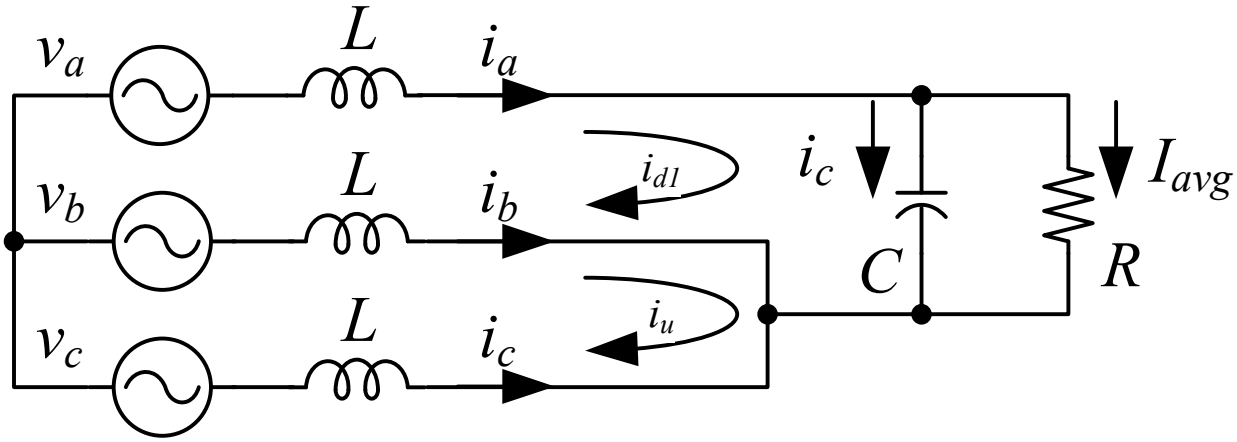

Figure 3.2 Simplified diode rectifier circuit with large line inductance

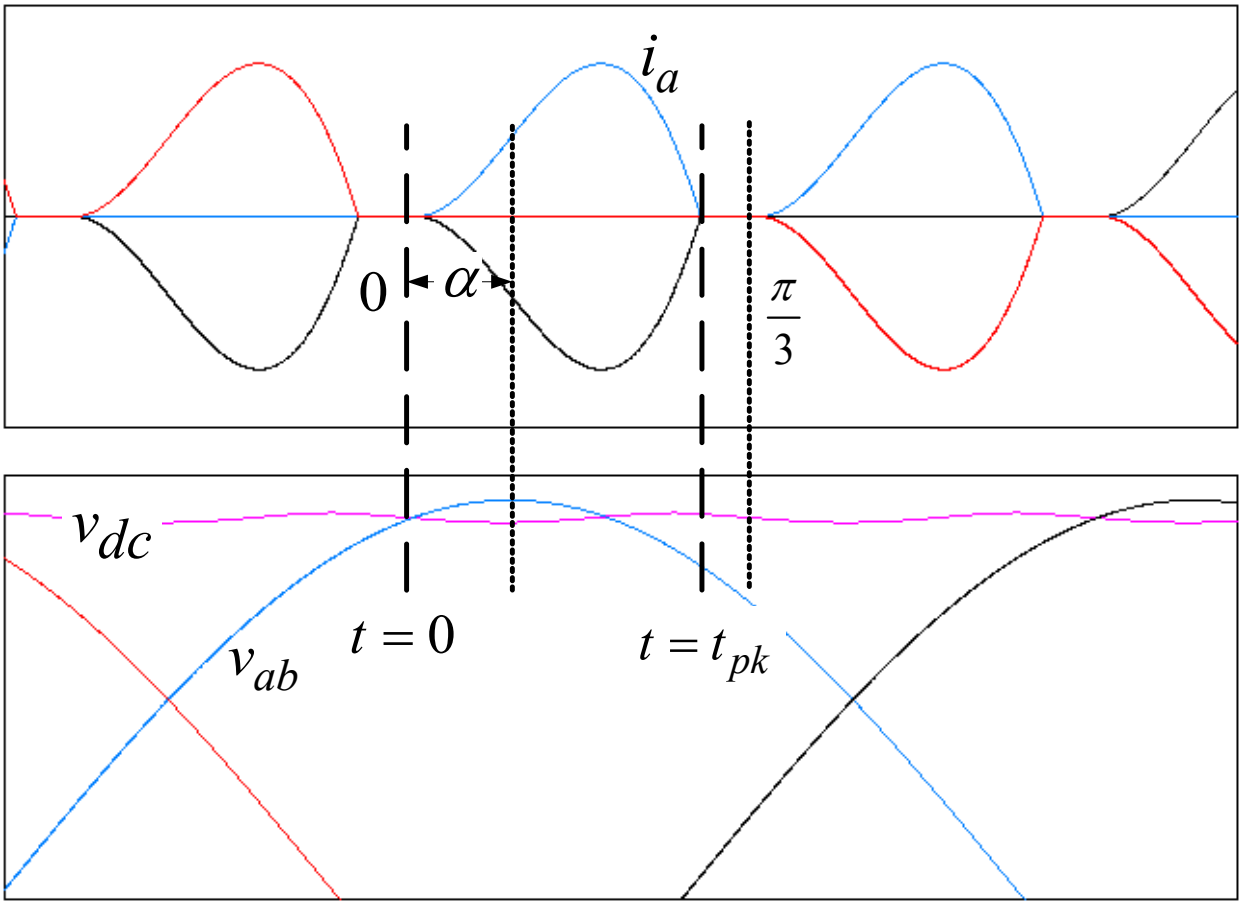

Figure 3.3 Critical inductance calculation of the diode rectifier (α definition) and Asec calculation of the diode rectifier with a small inductance

Since this case is the critical point of i_d , the initial condition is (3.4).

$$i_a = i_{d2}(0) = i_{d2}\left(\frac{T}{6}\right) = 0 \tag{3.4}$$

Assume the fundamental frequency is 60 Hz, so that $t=T/6=1/360$, and $\omega=2\pi 60$. Solving (3.2), (3.3) and (3.4) gives (3.5).

$$\alpha = 0.34767 = 19.92° \tag{3.5}$$

Assume the real power consumed by the load P remains the same. I_{avg} is the same as the

average value of i_a during 60°.

$$\frac{P}{V_{dc}} = I_{avg} = 360\int_0^{\frac{1}{360}} i_{d2}dt \tag{3.6}$$

Then, putting (3.2) and (3.3) into (3.6), the real value of the inductance is expressed as (3.7). By assuming the base value of the inductance is (3.8), the per unit value of critical inductance $L_{p.u.}$ is achieved to be 1.4639%.

$$L = \frac{\frac{360}{2}[-\frac{\sqrt{2}V_{ac}}{\omega^2}(\cos(\frac{\omega}{360}-\alpha)-\cos(-\alpha))-\frac{\sqrt{2}V_{ac}}{\omega}\frac{\sin(-\alpha)}{360}-V_{dc}\frac{(1/360)^2}{2}]}{\frac{P}{\sqrt{2}V_{ac}\cos\alpha}} \tag{3.7}$$

$$L_{base} = \frac{{V_{ac}}^2}{\omega P} \tag{3.8}$$

3.3 Calculation of Required DC Link Capacitance

3.3.1 With No Line Inductance

The voltage waveform of the diode rectifier when there is no line inductance is shown in Figure 3.4. The blue, green, magenta and red waveforms are v_{ab}, v_{bc}, v_{ca} and v_{dc} respectively. Assume the time interval is t_1 when the dc link capacitor is being charged through the diodes by the ac sources, and the time interval is t_2 when the capacitor is discharging to the load. During t_2, the dc link voltage is decreasing exponentially to be exact, like shown in (3.9).

$$V_{r(pp)} = \sqrt{2}V_{ac} - \sqrt{2}V_{ac}e^{-\frac{t}{RC}} \tag{3.9}$$

where R is the load resistance, C is the dc link capacitance and V_{ac} is the three-phase input line-to-line rms voltage. However, for the sake of convenience, the exponential function can be simplified to a linear function (3.10) without much error involved.

$$V_{r(pp)} = \frac{\sqrt{2}V_{ac}t_2}{RC} \tag{3.10}$$

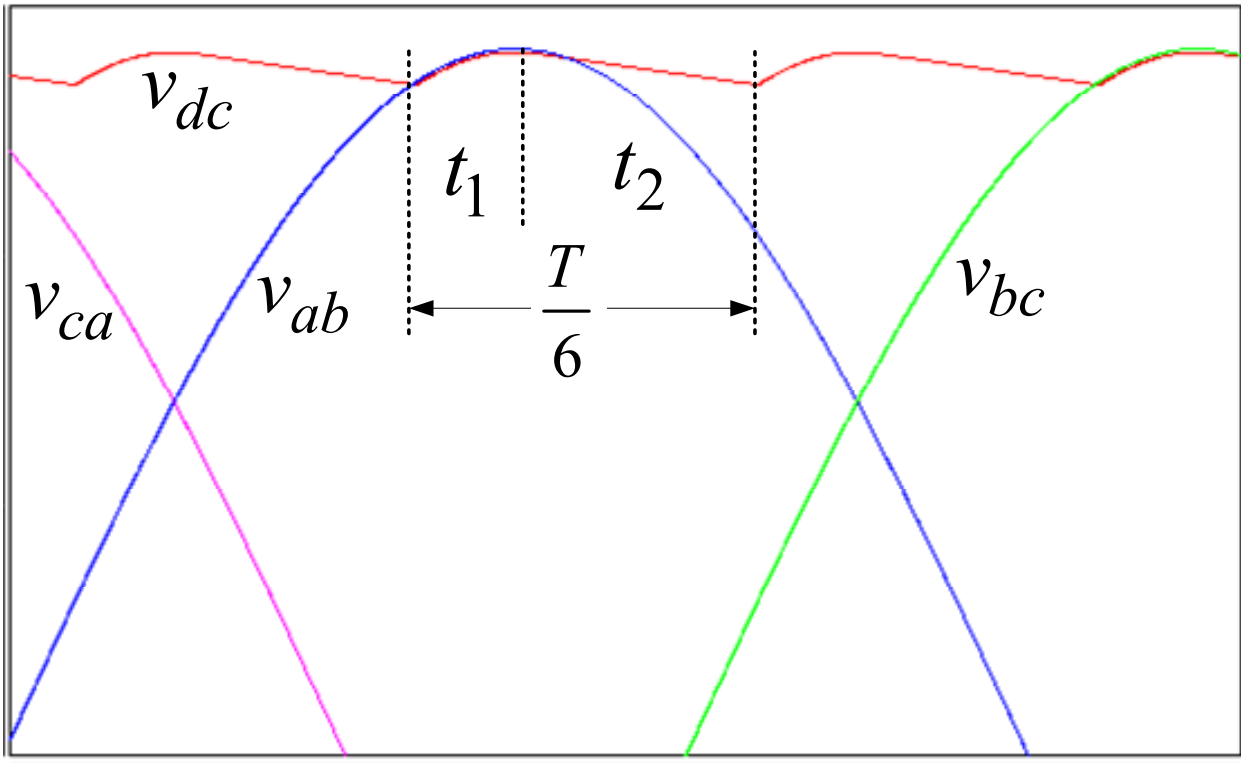

Figure 3.4 Asec calculation of the diode rectifier without line inductance

An approximated assumption is made here, in order to get the simple expression of the *A·sec*, which is $t_2 \approx$T/6. Therefore,

$$V_{r(pp)} = \frac{\sqrt{2}V_{ac}}{6fRC} \tag{3.11}$$

Hence, since a linearly decreasing voltage is assumed already, the average of the dc link voltage (3.12) is at the middle point of the peak to peak ripple voltage.

$$V_{dc} = \sqrt{2}V_{ac} - \frac{V_{r(pp)}}{2} \tag{3.12}$$

Again, assume the voltage ripple ε in (3.13) is the peak to peak ripple voltage divided by the average dc voltage.

$$\varepsilon = \frac{V_{r(pp)}}{V_{dc}} = \frac{2}{12fRC - 1} \tag{3.13}$$

One of the known conditions is (3.14).

$$R = \frac{{V_{dc}}^2}{P} \tag{3.14}$$

Consequently, substituting (3.13) into (3.14), will yield (3.15).

$$R = \frac{2{V_{ac}}^2\left(\frac{2}{2+\varepsilon}\right)^2}{P} \tag{3.15}$$

Substituting (3.15) into (3.13) will give the final capacitance expression as (3.16).

$$C = \frac{1}{96f}\frac{P}{{V_{ac}}^2}(2+\varepsilon)^2\left(\frac{2}{\varepsilon}+1\right) \tag{3.16}$$

The per unit value of the DC link capacitance (3.17) is only related the dc link voltage ripple factor ε, by assuming the base value in the form of (3.18).

$$C_{p.u.} = \frac{C}{C_{base}} = \frac{1}{96}(2+\varepsilon)^2\left(\frac{2}{\varepsilon}+1\right)2\pi \tag{3.17}$$

$$C_{base} = \frac{P}{2\pi f{V_{ac}}^2} \tag{3.18}$$

3.3.2 With 0%~1.46% Line Inductance

The primary method for this case is to first get the expression of the desired current i_c and secondly to integrate over a period to get *A·sec*. Matlab is used to get the initial value.

The equations for this case are almost the same as in the critical point calculation method. In Figure 3.3, α's assumption is the same as in the previous case. Therefore, (3.2) is again valid. The same (3.1) is obtained from the simplified circuit in Figure 3.1. The solution (3.3) of (3.1) is the phase current. When $t = t_{pk}$, $i_{d2} = 0$. (3.9) is obtained. The real power expression (3.6) is

valid as well.

$$\frac{\sqrt{2}V_{ac}}{2\omega L_s}[\sin(\omega t_{pk}-\alpha)-\sin(-\alpha)]-\frac{V_{dc}t_{pk}}{2L_s}=0 \tag{3.19}$$

Fortunately, only t_{pk} and α are unknowns in the system of equations (3.19) and (3.6), indicating that there exists a unique pair of solutions. Using Matlab, t_{pk} and α can be obtained.

Finally, integrating the positive half of i_c will give the expression of *Asec*. The upper and lower limit of the integration t_1 and t_2 are determined by (3.20) using Matlab. From all of these, (3.21) can be drawn in Figure 3.6 as the blue dashed line, of course by assuming the base value of the capacitance as (3.18).

$$i_c=\frac{\sqrt{2}V_{ac}}{2\omega L_s}[\sin(\omega t-\alpha)-\sin(-\alpha)]-\frac{V_{dc}t}{2L_s}-\frac{P}{V_{dc}}=0 \tag{3.20}$$

$$C=\frac{1}{\varepsilon}\int_{t_1}^{t_2}\left\{\frac{\sqrt{2}V_{ac}}{2\omega L_s}[\sin(\omega t-\alpha)-\sin(-\alpha)]-\frac{V_{dc}t}{2L_s}-\frac{P}{V_{dc}}\right\}dt \tag{3.21}$$

3.3.3 With Line Inductance Greater Than 1.46%

The primary method of this case is the same as the previous one with a small line inductance. However, this case includes two conditions: one is that three diodes are on at the same time as shown in Figure 3.2, and the other is that two diodes are on at the same time as shown in Figure 3.1, because of the phase current commutation.

For the first condition, derive (3.22) and (3.23) from the simplified diode rectifier circuit as shown in Figure 3.2.

$$v_{ab} = \sqrt{2}V_{ac}\cos(\omega t - \alpha) = 2L\frac{di_{d1}}{dt} - L\frac{di_u}{dt} + V_{dc} \tag{3.22}$$

$$v_{bc} = \sqrt{2}V_{ac}\cos(\omega t - \alpha - \frac{2\pi}{3}) = 2L\frac{di_u}{dt} - L\frac{di_{d1}}{dt} \tag{3.23}$$

By combining (3.22) and (3.23), i_{d1} and i_u are obtained.

$$\begin{aligned} i_{d1} = {} & \frac{2\sqrt{2}V_{ac}}{3\omega L}[\sin(\omega t - \alpha) - \sin(-\alpha)] - \frac{2V_{dc}t}{3L} \\ & + \frac{\sqrt{2}V_{ac}}{3\omega L}[\sin(\omega t - \alpha - \frac{2\pi}{3}) - \sin(-\alpha - \frac{2\pi}{3})] + i_{d1}(0) \end{aligned} \tag{3.24}$$

where $i_{d1}(0)$ is the initial condition.

$$\begin{aligned} i_u = {} & \frac{2\sqrt{2}V_{ac}}{3\omega L}[\sin(\omega t - \alpha - \frac{2\pi}{3}) - \sin(-\alpha - \frac{2\pi}{3})] \\ & + \frac{\sqrt{2}V_{ac}}{3\omega L}[\sin(\omega t - \alpha) - \sin(-\alpha)] - \frac{V_{dc}t}{3L} \end{aligned} \tag{3.25}$$

To calculate $i_{d1}(0)$, (3.26) is used, and (3.27) is achieved, where t_1 and the origin are demonstrated in Figure 3.5.

$$i_u(t_1) = i_{d1}(t_1) \tag{3.26}$$

$$i_{d1}(0) = \frac{\sqrt{2}V_{ac}}{3\omega L}(2\sqrt{3})\sin(\frac{\omega t_1}{2})\sin(\frac{\omega t_1}{2} - \alpha - \frac{\pi}{3}) + \frac{V_{dc}t_1}{3L} \tag{3.27}$$

For the second condition, (3.28) is derived from the simplified circuit, and please note that the time delay of π/3 is due to the reference voltage is v_{ab}.

$$v_{ac} = \sqrt{2}V_{ac}\cos(\omega t - \alpha - \frac{\pi}{3}) = 2L\frac{di_{d2}}{dt} + V_{dc} \tag{3.28}$$

where i_{d2} is shown in Figure 3.1.

Therefore, i_{d2} is obtained from (3.28).

$$i_{d2} = \frac{\sqrt{2}V_{ac}}{2\omega L}[\sin(\omega t - \alpha - \frac{\pi}{3}) - \sin(\omega t_1 - \alpha - \frac{\pi}{3})] - \frac{V_{dc}}{2L}(t - t_1) + i_{d2}(t_1) \tag{3.29}$$

where $i_{d2}(t_1)$ is the initial condition.

Since the condition is known:

$$i_{d2}(t_1) = i_u(t_1) \tag{3.30}$$

Substituting (3.30) into (3.25) yields (3.31).

$$\begin{aligned} i_{d2}(t_1) = {} & \frac{2\sqrt{2}V_{ac}}{3\omega L}[\sin(\omega t_1 - \alpha - \frac{2\pi}{3}) - \sin(-\alpha - \frac{2\pi}{3})] \\ & + \frac{\sqrt{2}V_{ac}}{3\omega L}[\sin(\omega t_1 - \alpha) - \sin(-\alpha)] - \frac{V_{dc}t_1}{3L} \end{aligned} \tag{3.31}$$

Finally, by utilizing (3.32) and (3.33), t_1 (the critical point from commutation to normal status) and V_{dc} can be achieved with Matlab. Using the same method as before, after getting the expression of *Asec*, the per unit value of capacitance can be obtained.

$$i_{d2}\left(\frac{1}{360}\right) = i_{d1}(0) \tag{3.32}$$

$$\frac{1}{1/360}\left(\int_0^{t1} i_{d1}dt + \int_{t1}^{\frac{1}{360}} i_{d2}dt\right) = \frac{P}{V_{dc}} \tag{3.33}$$

In conclusion, three curves, that show the relationship between the per unit capacitance value and the given tolerable voltage ripple percentage ε, for no line inductance, small inductance, and large inductance respectively, are drawn in the same graph in Figure 3.6, with comparison to the SPWM operation.

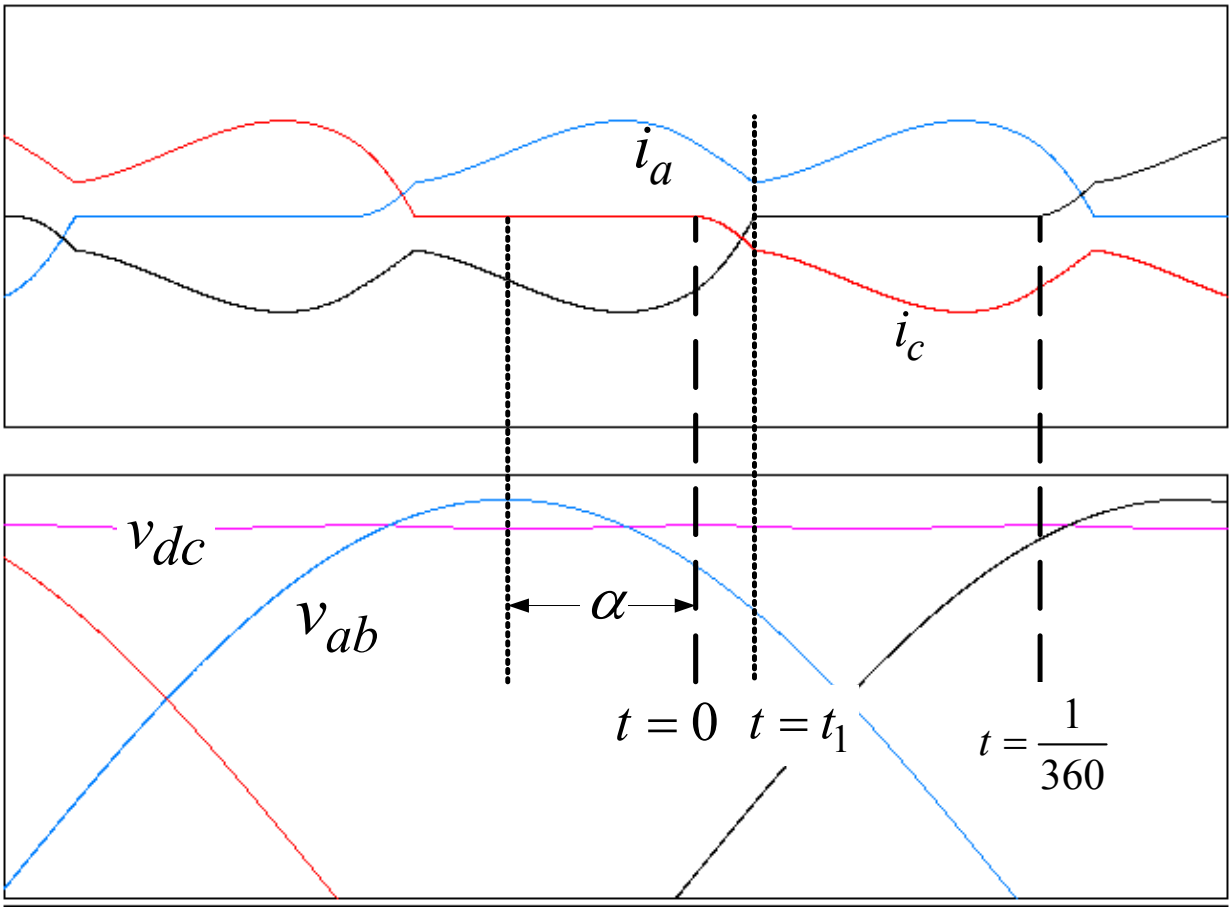

Figure 3.5 Asec calculation of the diode rectifier with a large inductance

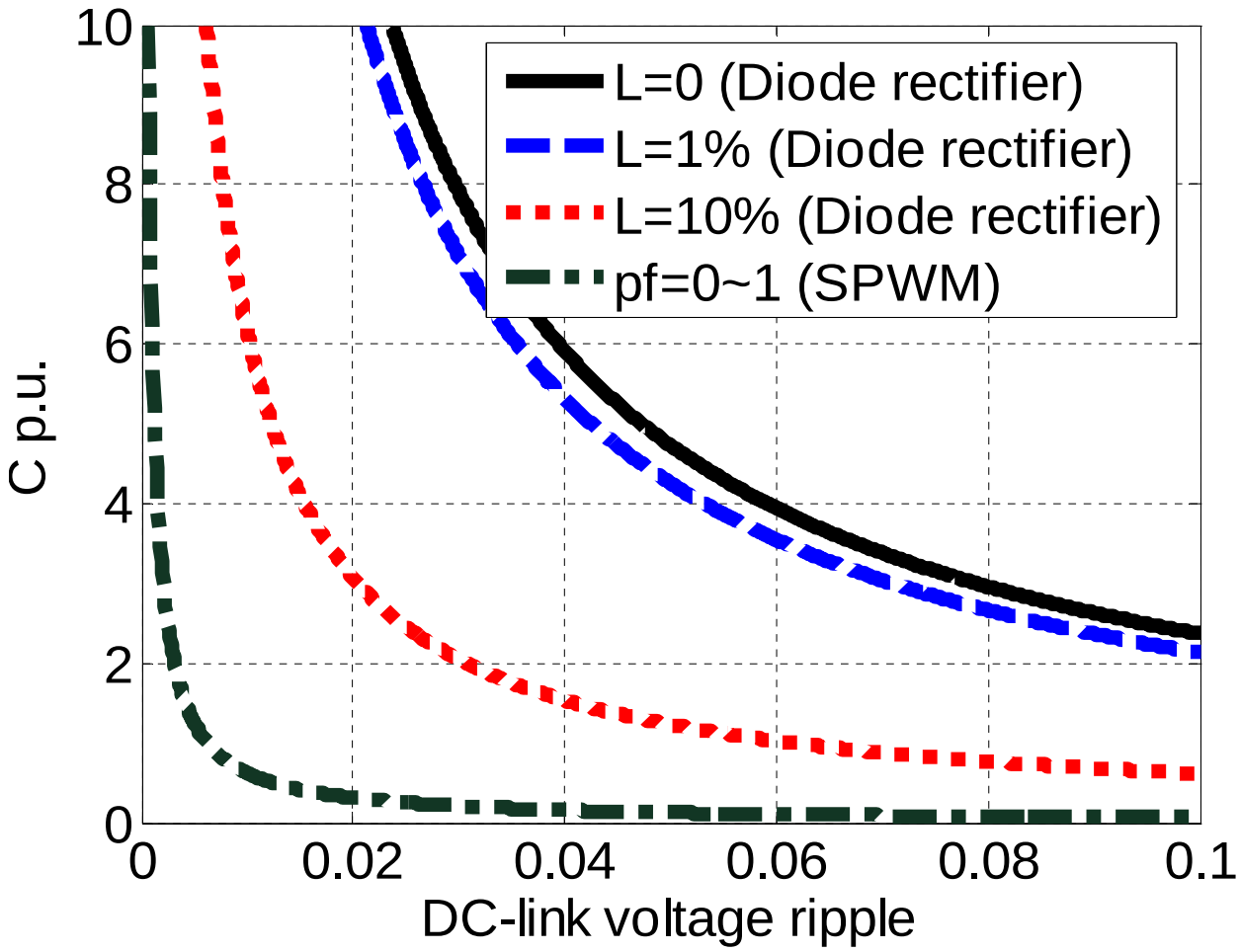

Figure 3.6 Cp.u. versus ε for rectifier operation compared with SPWM operation.

CHAPTER 4 DC Capacitance Requirement of the Six-Step Inverter

Six-step operation is used at a higher speed, when higher output voltage is required. It is because that six-step operation has higher dc utilization than the traditional SPWM operation.

4.1 Simplified Configuration and System Parameters

As the traction motors run to a higher speed, the back electromotive force (EMF) should be considered. In this case, the equivalent circuit of the inverter under six-step operation is shown in Figure 4.1. Assume that there are three more voltage sources v_a, v_b, and v_c, inserted in each phase leg at the load side, representing the three-phase back EMFs of the traction motors. Since the load is a traction motor, inductors and resistors should be added as well. In order to have unity power factor, the inserted voltage source will have a leading power factor, $v_a = V_i \sin(\omega t + \varphi)$ (V_i and φ are the amplitude and angle of the inserted voltage source—the back EMF, which are calculated by assuming a power factor and an inductance).

Assume the inductance *L* ranging from 0.3%, 1% and 3% of the per unit (p.u.) value, the resistance *R* is 1% p.u., the base system is as (4.1), the base speed of the traction motor is 1200 rpm, and the maximum speed is 5000 rpm. Therefore, the inductance of the system base would be as shown in Table 4.1.

$$\begin{cases} P = 150kW \\ V_{ll} = 480V \end{cases} \tag{4.1}$$

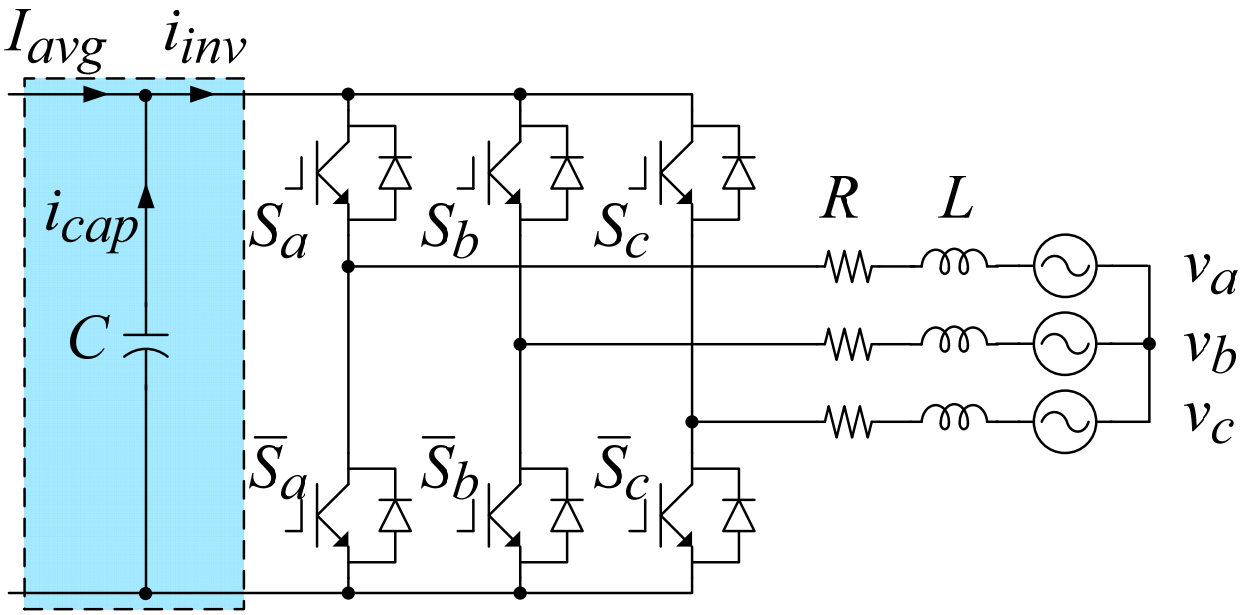

Figure 4.1 The simplified equivalent circuit of the inverter under six-step operation

Table 4.1 The list of Inductance and Resistance Changing Base

	Per unit (base speed)	L_{real}	$L_{new,base}$	**Per unit (max speed)**
L	0.3%	18.335 uH	1.466772 mH	1.25%
	1%	61.115 uH	1.466772 mH	4.17%
	3%	183.346 uH	1.466772 mH	12.5%
R	1%	0.01536 Ω		1%

By knowing the inductance and assuming a power factor, the amplitude and angle of the inserted voltage source, V_i and φ, are obtained in Table 4.2.

Table 4.2 The list of Inserted Voltage source Amplitude and Phase Angle Based on Different Power Factor and Load Impedance

p.f.	***L***					
	3%		**1%**		**0.3%**	
	$V_{i(peak)}$ / V	**φ/°**	$V_{i(peak)}$ / V	**φ/°**	$V_{i(peak)}$ / V	**φ/°**
1.0	391.08	7.19624	388.34	2.41002	388.03	0.72339
0.5	433.28	3.69049	404.27	1.63847	394.24	0.84928
0.0	440.93	0.50928	408.27	0.55002	396.84	0.56587

4.2 Calculation of Required DC Link Capacitance

From a simplified schematic of Figure 4.1, which is very similar to Figure 3.2, (4.2) is obtained.

$$\begin{cases} V_{dc} = Ri_a + L\dfrac{di_a}{dt} + v_a + R(-i_b) + L\dfrac{d(-i_b)}{dt} + (-v_b) \\ i_a + i_b + i_c = 0 \\ Ri_a + L\dfrac{di_a}{dt} + v_a = Ri_c + L\dfrac{di_c}{dt} + v_c \end{cases} \tag{4.2}$$

By combining them together, (4.3) is achieved.

$$\frac{di_a}{dt} + \frac{R}{L}i_a = \frac{V_{dc}}{3L} - \frac{v_a}{L} \tag{4.3}$$

Therefore, the solution of (4.3) should be in the general form of: $i_a = i_{a(p)} + i_{a(g)}$, where

$i_{a(p)}$ stands for the particular solution and $i_{a(g)}$ represent general solution. The particular solution $i_{a(p)}$ is (4.4).

$$i_{a(p)} = a + C\cos(\omega t - \varphi) + D\sin(\omega t - \varphi) \tag{4.4}$$

where $a = \frac{V_{dc}}{3R}, D = -\frac{V_i}{R^2 + \omega^2 L^2}, C = -\frac{D\omega L}{R}$.

and the general solution $i_{a(g)}$ is (4.5).

$$i_{a(g)} = k \cdot e^{-\frac{R}{L}t} \tag{4.5}$$

For i_a, the only unknown coefficient is *k*, the initial coefficient. To get this, Matlab can be utilized to calculate *k*, integrate i_a, and draw Figure 4.2 showing the relationship between the per unit value of the desired capacitance and a given dc link voltage ripple requirement.

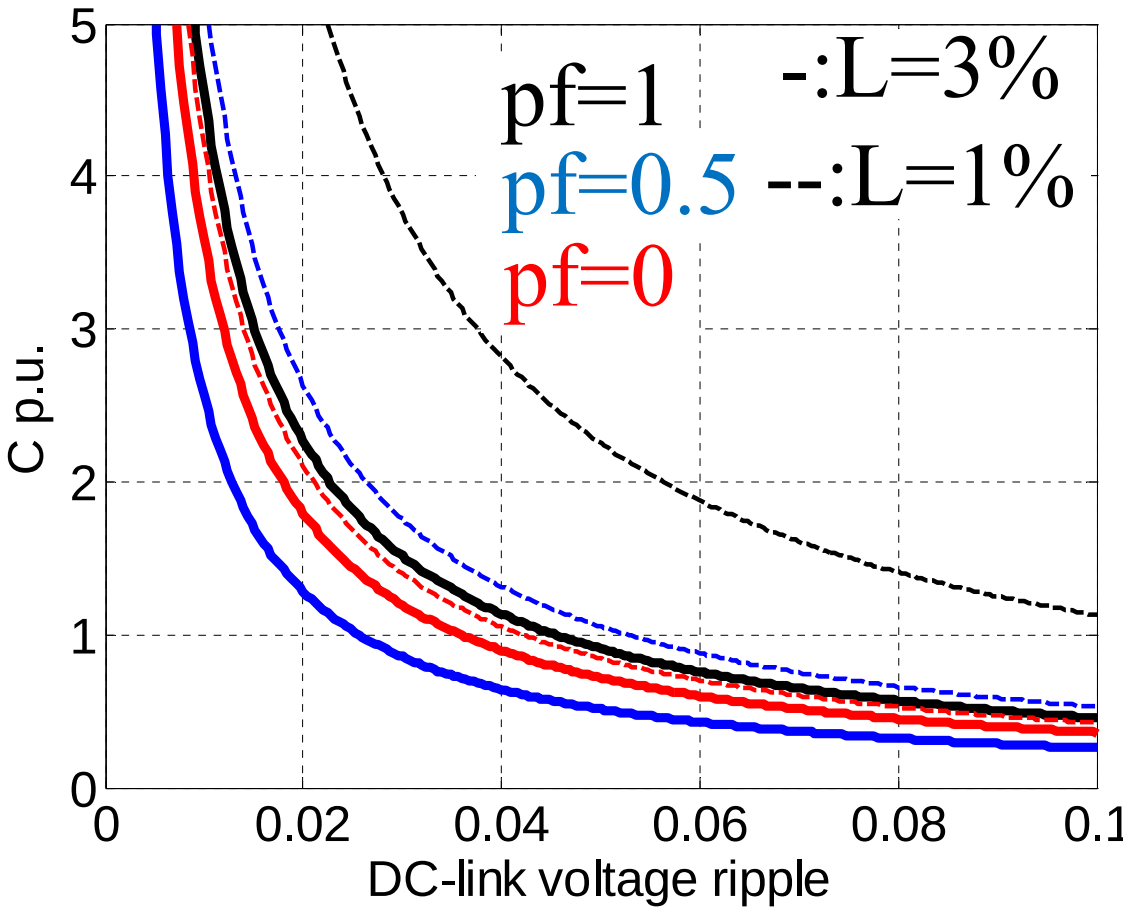

Figure 4.2 Cp.u. versus ΔV for 6-step

In conclusion, all figures above are aggregated and compared, in Figure 4.3 and Figure 4.4

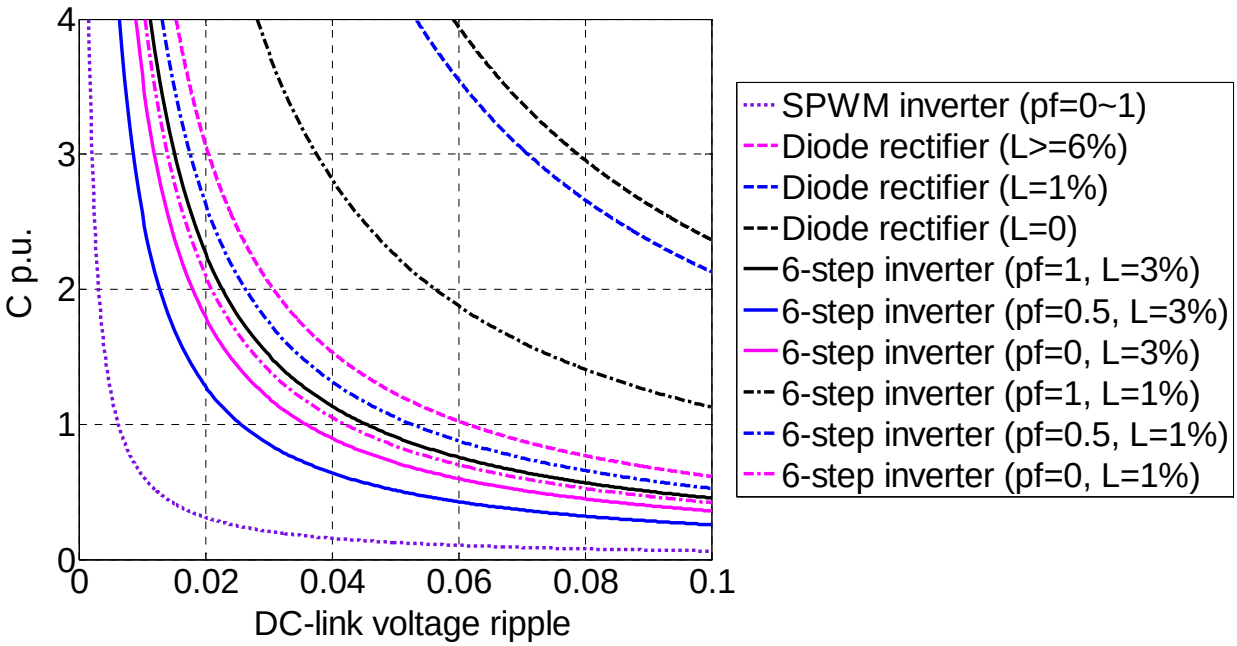

Figure 4.3 The aggregate of all figures above: Cp.u. versus ΔV for all operations

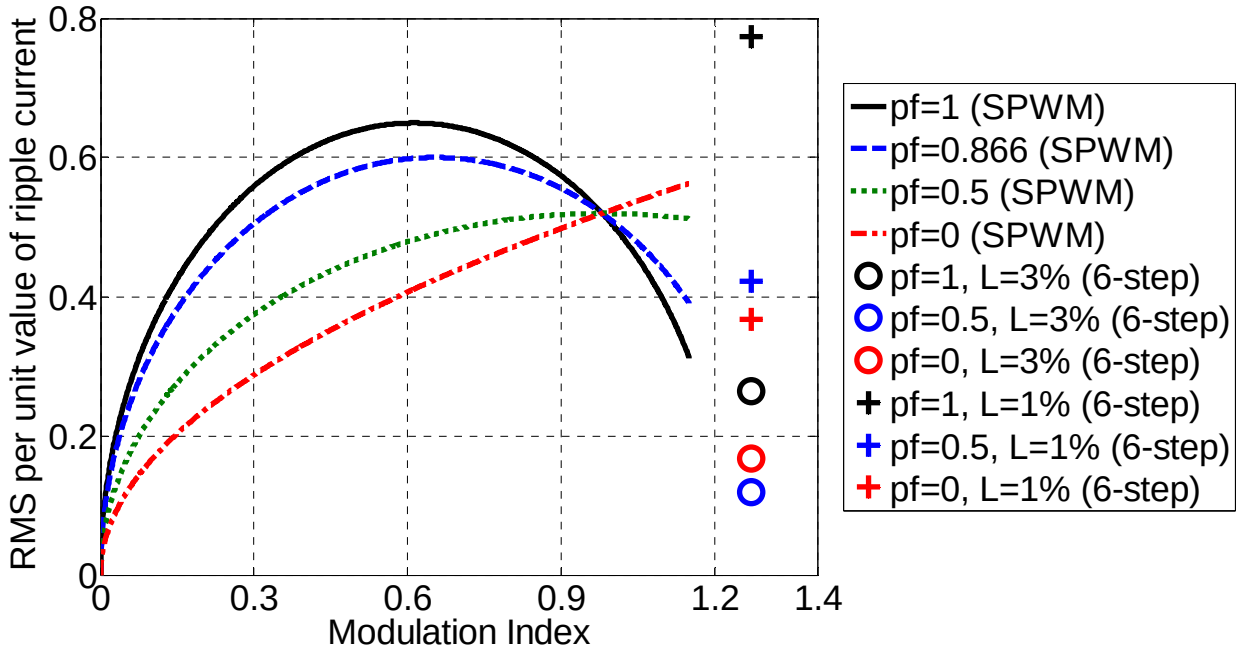

Figure 4.4 ΔI_{RMS} versus MI for SPWM and 6-step operation

CHAPTER 5 Prototype and Testing Results of SHEV Power Electronics Module

5.1 Prototype

The inverter module in Figure 5.1 was developed to achieve 100 kW continuous output power (150 kW peak power) for use in a series hybrid electric bus. The rated output line-to-line voltage is 480 V, and the rated line current is 180 A. Therefore, according to (2.29) and Table 2.3, C_{base} is 516.95 uF.

This paper shows calculations of the minimum capacitance that one system needs without any close-loop control strategy. Therefore, the experiments were done under open loop circumstances.

The experiment is done at the condition when the dc link voltages are 200 V, 300 V, 400 V, 500 V, 600V and 650 V, the switching frequency is 5 kHz, the fundamental frequency is 200 Hz, and the power factor is almost 0 with a purely inductive load—1 mH in each phase connected in wye. The inverter is operated under the SPWM normal modulation method. In this prototype, the parameters of the setup are listed in Table 5.1. In the system in Figure 5.1, the total dc link capacitance is 510 uF with six 85 uF 1000 V film capacitors in parallel.

The per unit value of dc capacitance can be obtained.

$$C_{p.u.} = \frac{510uF}{516.95uF} = 0.9866 \tag{5.1}$$

Table 5.1 The Configuration in the Prototype

Parameters	**Value**
Load inductor	*1 mH*
Power factor (pf)	*0*
DC link capacitance	*510 uF*
DC link voltage	*650 V*
AC current	*180 A*
Switching frequency	*5 kHz*
Fundamental frequency	*200 Hz*
Modulation index (MI)	*0.9*

From Figure 2.6, the nearest point of the per unit value of dc capacitance is 0.9858, whose y-coordinate indicates that the voltage ripples on the dc link would be 3.65%. This is verified by the following experiment results.

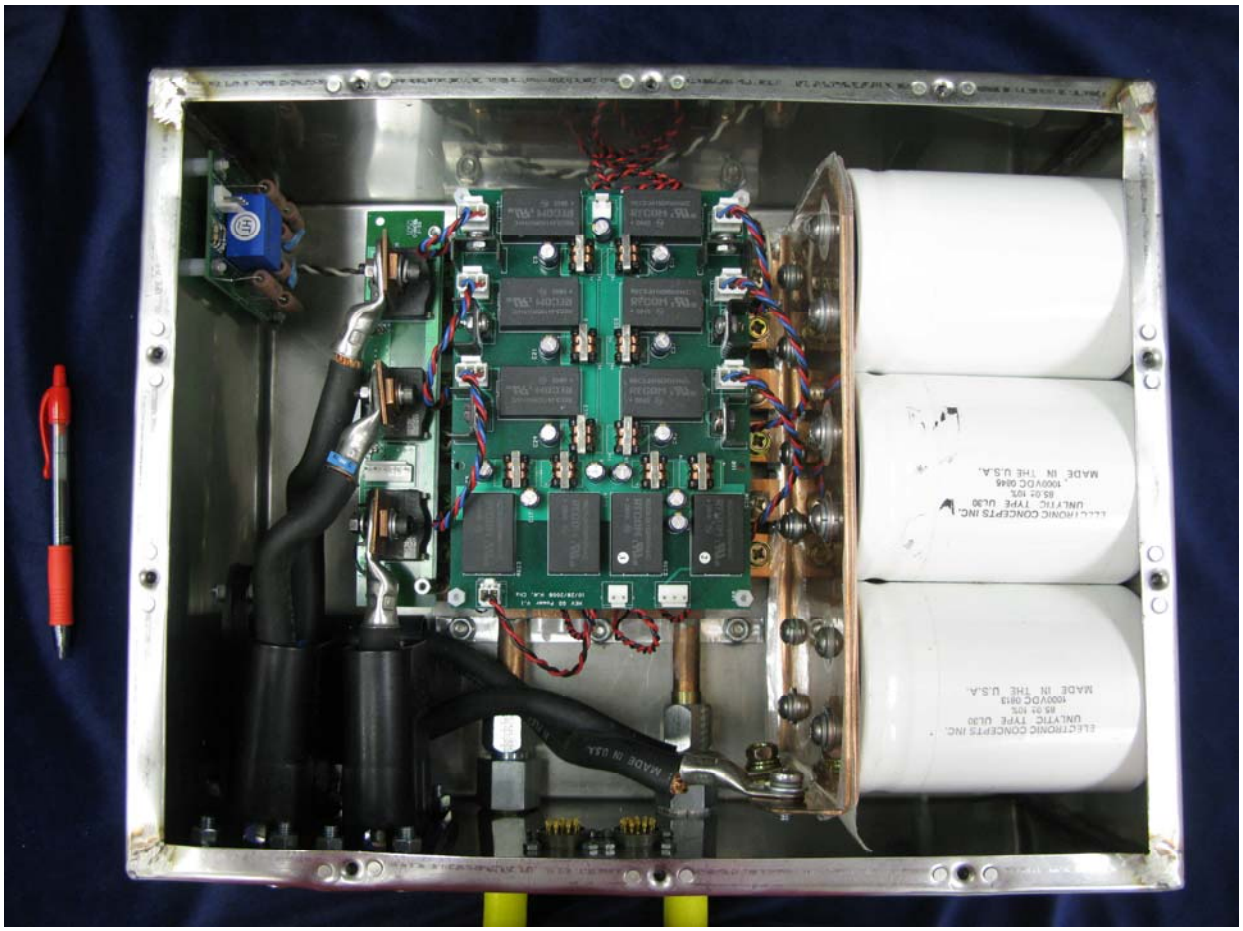

Figure 5.1 Inverter module assembly photos (including DC link capacitors, IGBT module, Gate Drive board and Gate drive power supply on top)

5.2 Test Results of Voltage Ripple

The experimental results are shown in Table 5.2.

Table 5.2 Expreimental Result of Voltage ripple

Vdc/V	**Iac/A**	**Vdc ripple/V**	**ε/%**
200	58	7.8	3.9
300	87	10.8	3.6
400	116	13.7	3.4
500	145	16.6	3.3
600	173	20.9	3.5
650	180	21.7	3.3

As mentioned before, the maximum voltage ripple on the dc link during one switching cycle should be around 3.6% of the dc voltage by the theoretical calcuation, which is in close agreement with the test result shown in Table 5.2. The purple, blue and yellow nearly sinusoidal waveforms in Figure 5.2, Figure 5.3, and Figure 5.4 are the load phase currents, and the green waveform is the dc link voltage ripple. The 6ω ripple component in the dc link voltage comes from the almost pure inductive load.

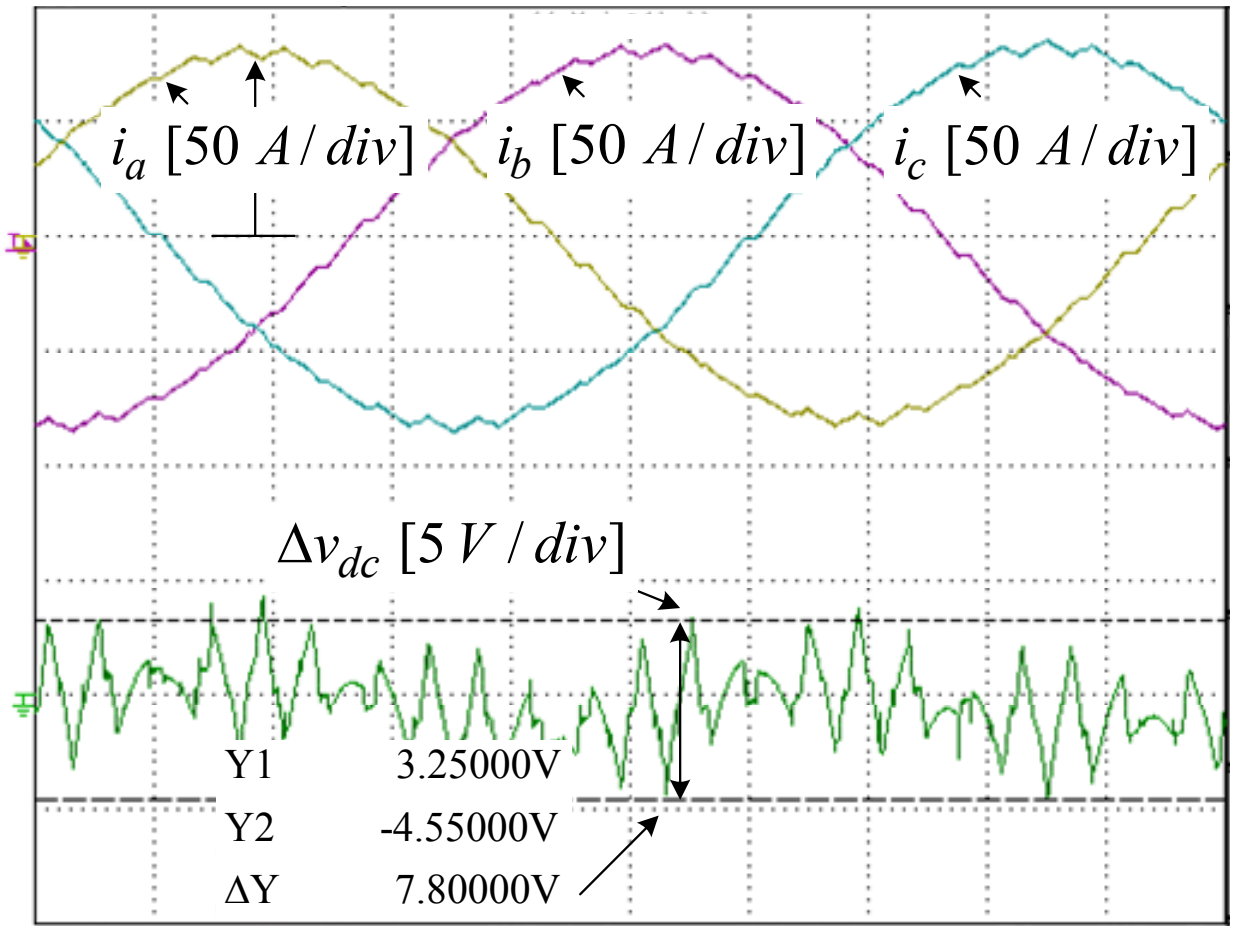

Figure 5.2 The experimental waveforms of three phase currents and DC link voltage ripple with DC link voltage at 200 V.

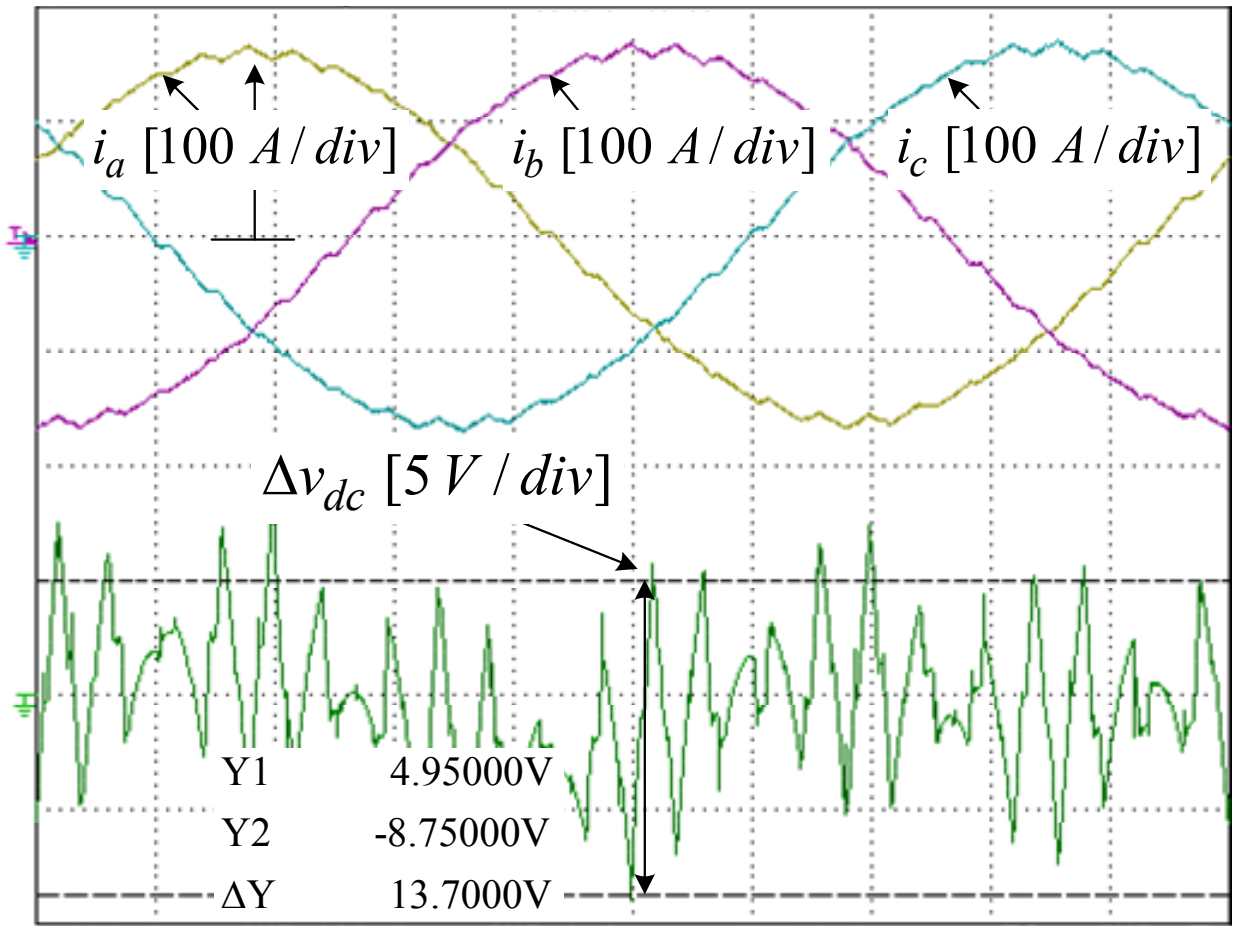

Figure 5.3 The experimental waveforms of three phase currents and DC link voltage ripple with DC link voltage at 400 V

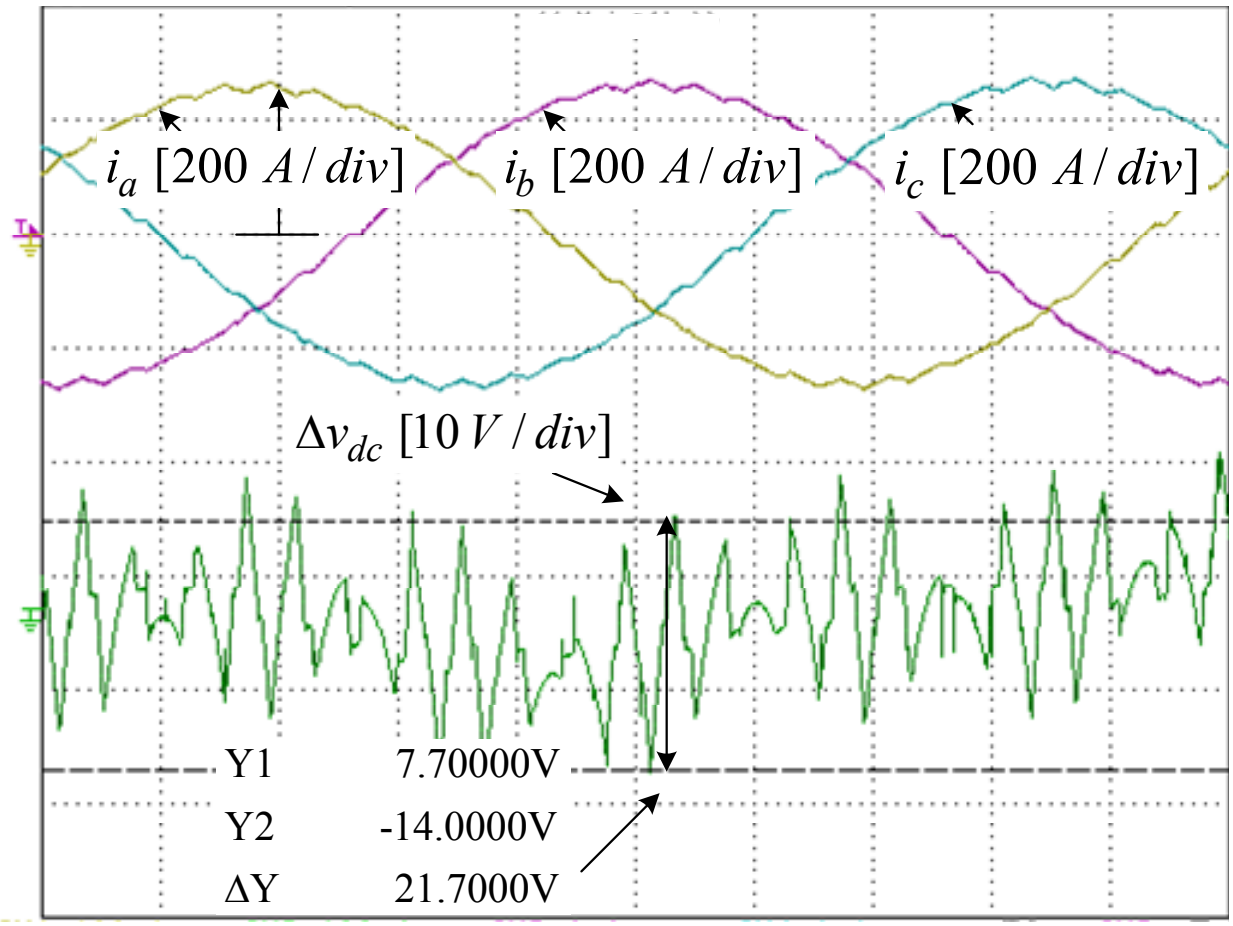

Figure 5.4 The experimental waveforms of three phase currents and DC link voltage ripple with DC link voltage at 650 V

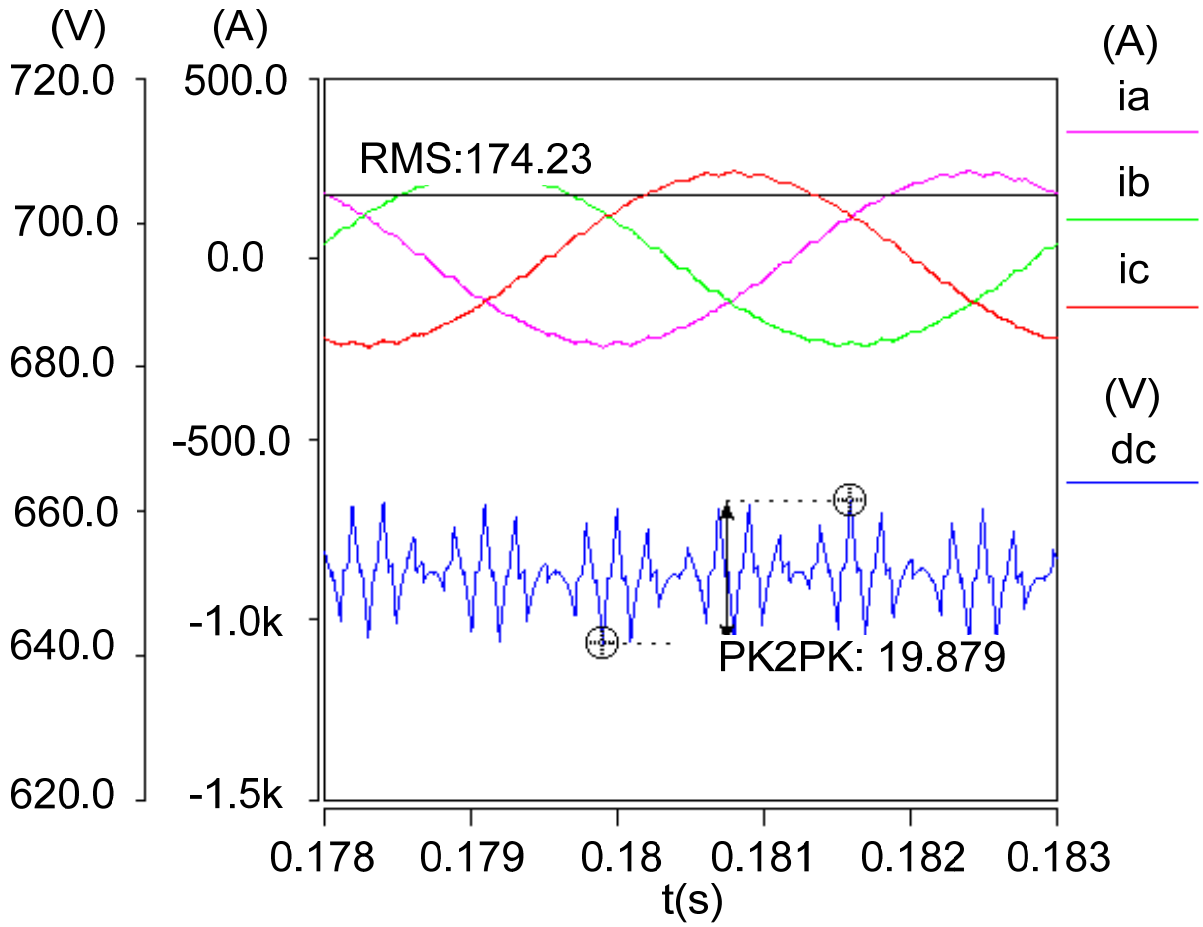

Figure 5.5 The simulation waveforms of three phase currents and DC link voltage ripple with DC link voltage at 650 V

5.3 Test Results of Current Ripple

From Figure 4.4, when pf=0 and MI=1, the rms current per unit value is 0.52; when MI=0.75, the p.u. is 0.46; when MI=0.5, the p.u. is 0.38; when MI=0.25, the p.u. is 0.27. The experimental results are shown in Table 5.3, which is in close agreement with the theoretical value.

$$i_d = S_a i_a + S_b i_b + S_c i_c \tag{5.2}$$

Table 5.3 Experimental Results of rms current of The Capacitor

Vdc/V	***MI=1***			***MI=0.75***		
	Iac/A	**Irms/A**	**ε**	**Iac/A**	**Irms/A**	**ε**
200	30.2	15.15	0.50	22.7	10.40	0.46
300	45.3	23.80	0.53	33.9	15.57	0.46
400	60.4	33.28	0.55	45.2	21.50	0.48
500	75.3	40.10	0.53	56.7	26.60	0.47
600	90.6	48.00	0.53	67.8	31.53	0.47
Vdc/V	***MI=0.5***			***MI=0.25***		
	Iac/A	**Irms/A**	**ε**	**Iac/A**	**Irms/A**	**ε**
200	15.1	5.73	0.38	7.22	1.93	0.27
300	22.5	8.83	0.39	10.9	3.02	0.28
400	30.0	11.4	0.38	14.3	3.88	0.27
500	37.6	15.0	0.40	18.1	4.80	0.27
600	44.9	17.7	0.39	21.6	5.65	0.26

The yellow and green waveforms in Figure 5.6 are V_{ce} waveforms of the lower switches of phase A and B. The red and orange sine waveforms are the phase currents of phase A and C. The middle PWM red waveform is the inverter input current and since pf=0, it is the capacitor current i_c as well due to I_{avg}=0. Since layout of the dc link is of the busbar design type, the capacitor current was measured by math function in oscilloscope by (5.2).

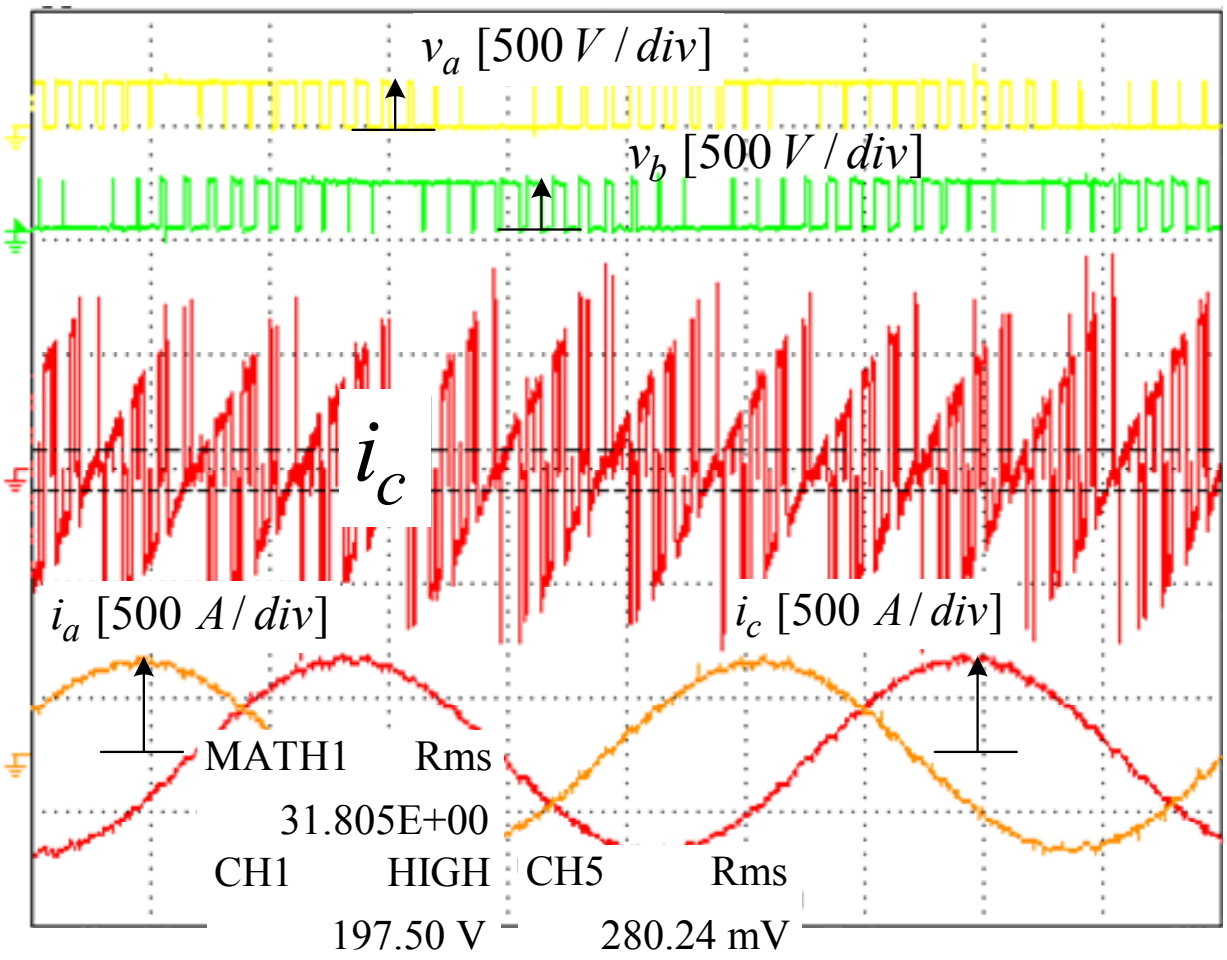

Figure 5.6 The experimental waveforms of the capacitor current with DC link voltage at 200 V, pf=0 and MI=0.9

Theoretical equations to express capacitance versus voltage ripple and rms ripple current versus modulation index have been developed for SPWM. These equations improve the design/calculation of the required dc capacitance and enhance insight into the limits and optimum operation of the HEV converter/inverter system as compared to the traditional empirical equations and simulations. The validity of the theory was verified by the experimental results of a three-phase SPWM inverter system.

CHAPTER 6 Minimizing the DC Capacitance between the DC-DC Converter and SPWM inverter—A Carrier Modulation Method

6.1 Introduction

In the HEV converter/inverter system, for the sake of boosting the battery's low dc voltage to high dc voltage, and then converting it into ac voltage to drive the traction motors, the inverters are always connected in series to the dc-dc converters, as shown in Figure 6.1. However, the dc link capacitor bank between the dc-dc converter and the inverter is usually bulky, heavy and expensive, due to the fact that it must absorb all the current ripples from every converter connected to it. Therefore, minimization of the dc capacitor is an essential step towards developing and manufacturing compact low-cost HEV converter/inverter systems for high temperature operation, long life and high reliability [32].

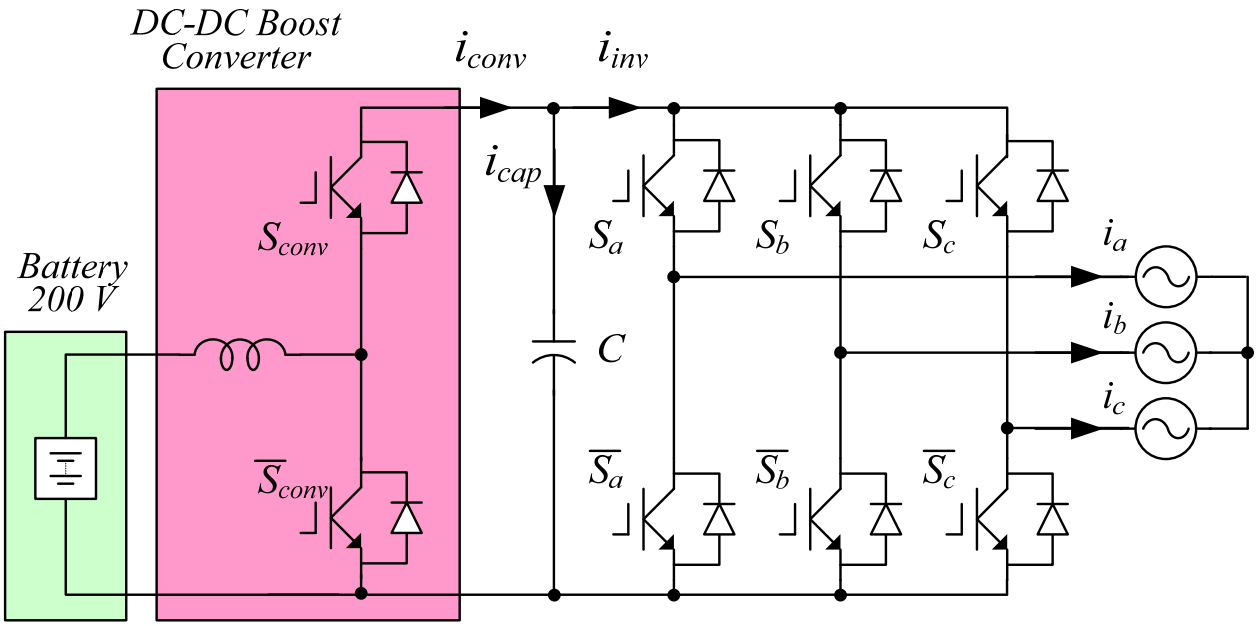

Figure 6.1 The schematic of the bidirectional DC-DC converter and the inverter

Yet the bottleneck of the capacitor's size is determined by the current ripple requirement rather than the voltage ripple requirement due to the existing capacitors-making technology. Similar to the condition described in [5], in order to minimize the dc link capacitance between the dc-dc converter and the SPWM inverter, making the converter side dc link current i_{conv} equal to the inverter side dc link current i_{inv} in a PWM converter-inverter system is the final destination. Ideally, no current will flow through the dc link capacitor and no voltage fluctuation will be across the capacitor, meaning no capacitor is needed at all. Till now, most papers that discussed the current ripple reduction and the dc link capacitance minimization are based on the AC-DC-AC PWM converter-inverter systems with relatively complicated close-loop control methods [5-7, 10, 20, 23-25]. The best result that they can achieve is almost without any dc link capacitors. Besides, there are papers discussing innovative PWM strategies only on the inverter side, allowing reduction of the dc input current ripples [26-28, 33], which is the same as reducing the capacitance. Still, there are a few papers related to DC-DC-AC PWM converters [29, 34]. [29]

used bang-bang control for the dc-dc converter to minimize the dc link capacitance, however it is a complicated close-loop control. Additionally, [34] developed a single-phase PWM method for the inverter to reduce 2/3 of the switching loss and achieve high efficiency; this kind of PWM method requires the system to have bigger ripple on the dc link so that only a tiny dc link capacitor is needed. These are either complicated close-loop control for the dc-dc converter, or the PWM strategy for the inverter. However, very few papers have been written focusing on the current ripple reduction by synchronizing between the dc-dc converter and the SPWM inverter. Shown in Figure 6.2 (c), the black solid line shows the converter output current when synchronized, while the blue dashed line shows the one that is unsynchronized. Therefore, in order to cancel the current ripple with the inverter input current shown in Figure 6.2 (a), the solid line one will definitely do a better job than the dashed line one. In conclusion, a synchronized PWM method will help minimize the capacitance, whereas an unsynchronized PWM may double the requirement of the capacitance. Hence, a better way to minimize the dc capacitance is to reduce the current ripple through the capacitor by synchronizing the dc-dc converter and the SPWM inverter. [30] made a good start for the synchronization by making the dc-dc converter's switching frequency twice as much as the inverter's switching frequency and optimizing the phase difference of the carrier waveforms between the inverter carrier and dc-dc carrier. This method does decrease the current ripple quite a lot, which is shown in Figure 6.2. In spite of this, more improvement can be made.

In this chapter, a simple carrier modulation method is proposed to reduce the current ripple going through the dc link capacitor. This paper proposes two different kinds of new carrier modulation methods for the dc-dc converter, and concludes to one that is easy to implement, in order to match with the inverter input current so as to minimize the current ripple that going

through the dc link capacitor. Comparing with the conventional triangle carrier, the proposed simple carrier modulation is able to help minimize the current ripple going through the dc link capacitor at unity power factor by a simple and easy implementation without complex close-loop control. The simulation and experimental results are provided to validate the effectiveness of the proposed method.

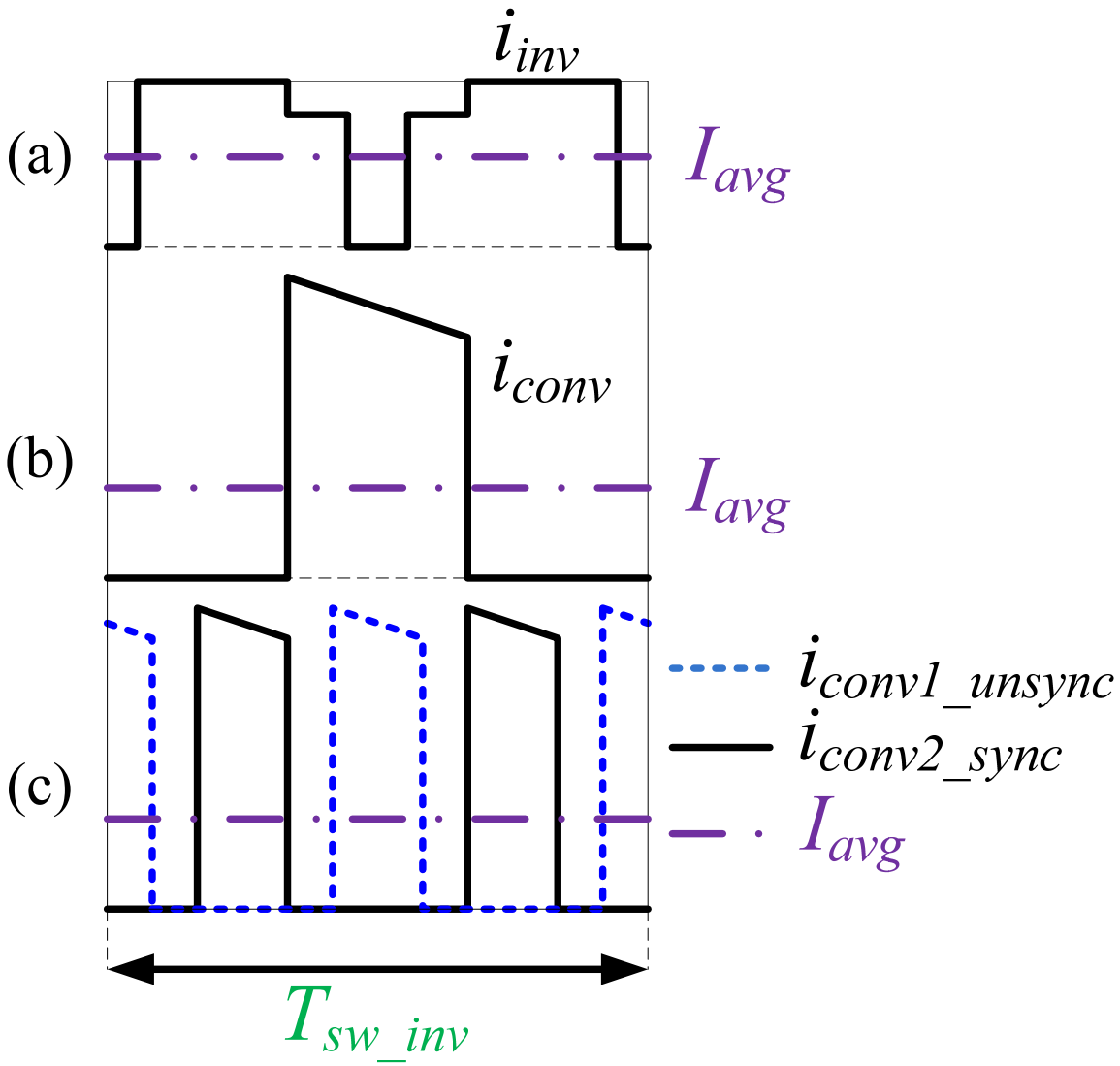

Figure 6.2 (a) One sample switching period of the inverter input current with average current drawn in the same figure; (b) The converter output current ($f_{conv} = f_{inv}$); (c) The converter output currents for unsynchronized case and synchronized case ($f_{conv} = 2 f_{inv}$).

6.2 The Conditions Under Consideration

6.2.1 Unity Modulation Index of the Inverter

Assume the dc-dc converter is working at boost mode; therefore the SPWM inverter operates at unity modulation index to maximize the output voltage. This assumption is made, because common sense states that lowering the voltage by decreasing the modulation index of the inverter is counter-productive, when dc-dc converter is doing boost. However, the method proposed in this paper is still applicable to modulation index other than unity, since different modulation index does not change the positions of the inverter current pulses.

6.2.2 Unity Power Factor of the Load

Depending on motor types and motor operation conditions, the motor power factor can range from 0.6 to unity. In this chapter, it is assumed that the load is at unity power factor, due to the reason that low power factor will result in low dc current, so that benefit of the proposed carrier modulation method will not be significant.

6.2.3 Constant Duty Cycle for the Boost Converter

The duty cycle of the dc-dc converter in every switching cycle is constant in steady state, and assume the dc-dc converter's duty cycle under 2/3, when doing boost. The reasons are as follows. First of all, the constant output voltage of the battery and the desired value of the dc link voltage determines the duty cycle of the dc-dc converter. Secondly, if one keeps the average duty cycle constant, but periodically changes it from cycle to cycle, the inductor current will end up with

much higher low frequency harmonic components, which is absolutely undesired. Therefore, it is better to keep the duty cycle constant in every switching cycle.

6.2.4 Sinusoidal Inverter Output Currents

Since the motors in HEV systems usually behave as huge inductors plus resistors, it is safe to assume that the output current is almost sinusoidal.

6.2.5 Analyze One of Six 60° Sectors

Instead of looking at the whole fundamental period of 360°, it is the same to analyze only 60°, for the reason that the waveforms are repeated at a frequency of 6ω due to the three phases. Therefore, the following analysis will only focus on the range of 30° to 90° (take v_a^* as a reference), where $v_a^* > v_c^* > v_b^*$, shown in pink shaded block in Figure 6.3.

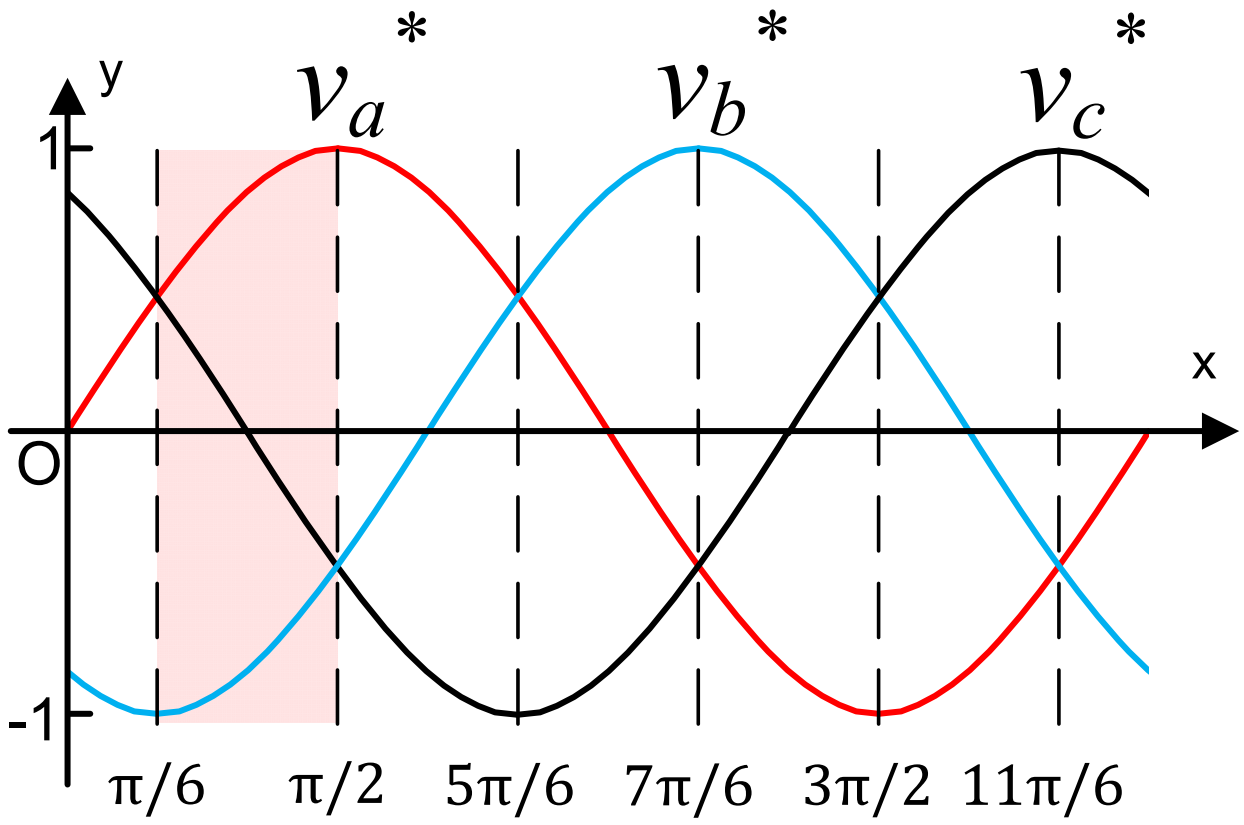

Figure 6.3 Three sinusoidal references v_a^*, v_b^*, and v_c^* of the SPWM inverter with one of the six sectors shown in pink shaded block, which will be discussed in this paper.

6.3 The Analysis of the Ideal SPWM Inverter Input Current Waveform

Figure 6.4 (a) shows the common sinusoidal PWM method for the inverter during the 60° sector ($v_a^* > v_c^* > v_b^*$) that specified in section II. Figure 6.4 (b) demonstrates the trend of the inverter input current's pulse positions within this sector. Each triangle indicates a switching cycle; therefore there are 6 switching cycles in Figure 6.4. From switching cycle No. 1 to No. 6, it can be seen that the two pulses in each switching cycle are shifting from the side to the middle.

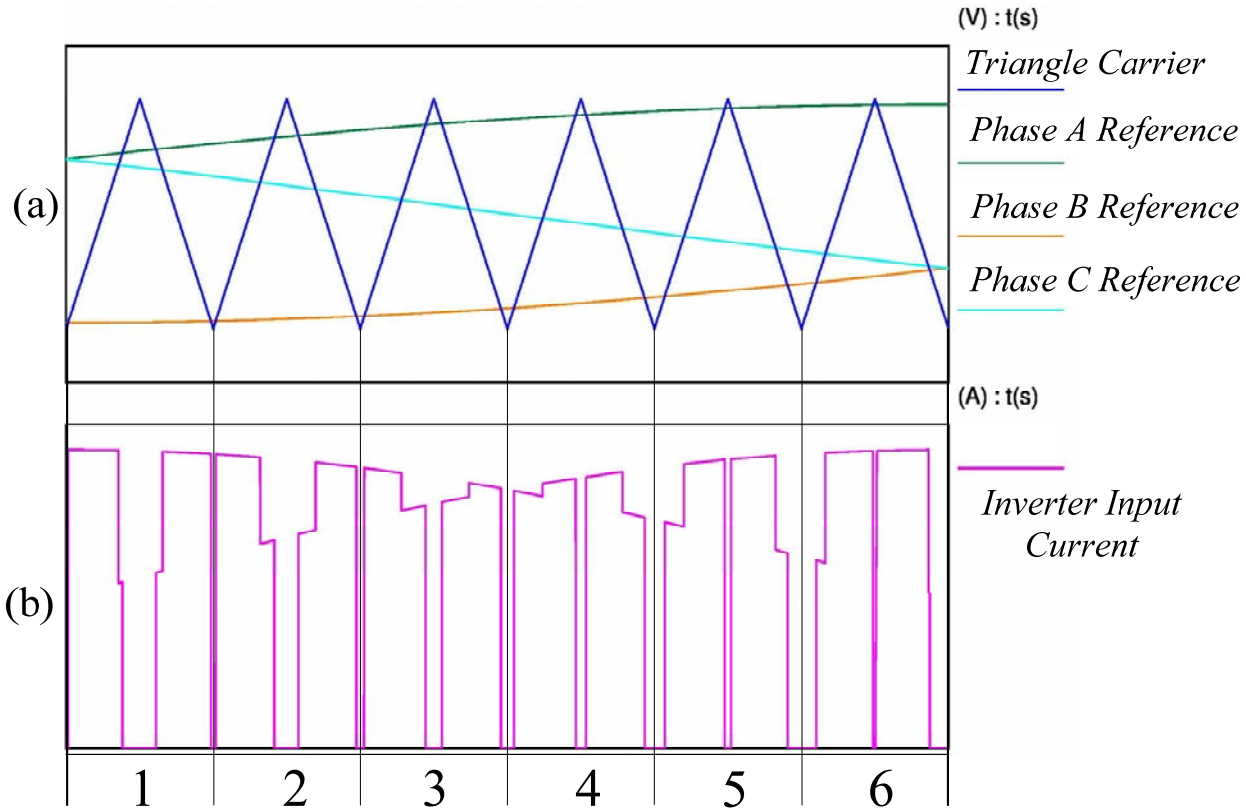

Figure 6.4 (a) Common sinusoidal PWM method for the inverter; (b) Simulation waveform of the inverter input current i_{inv}

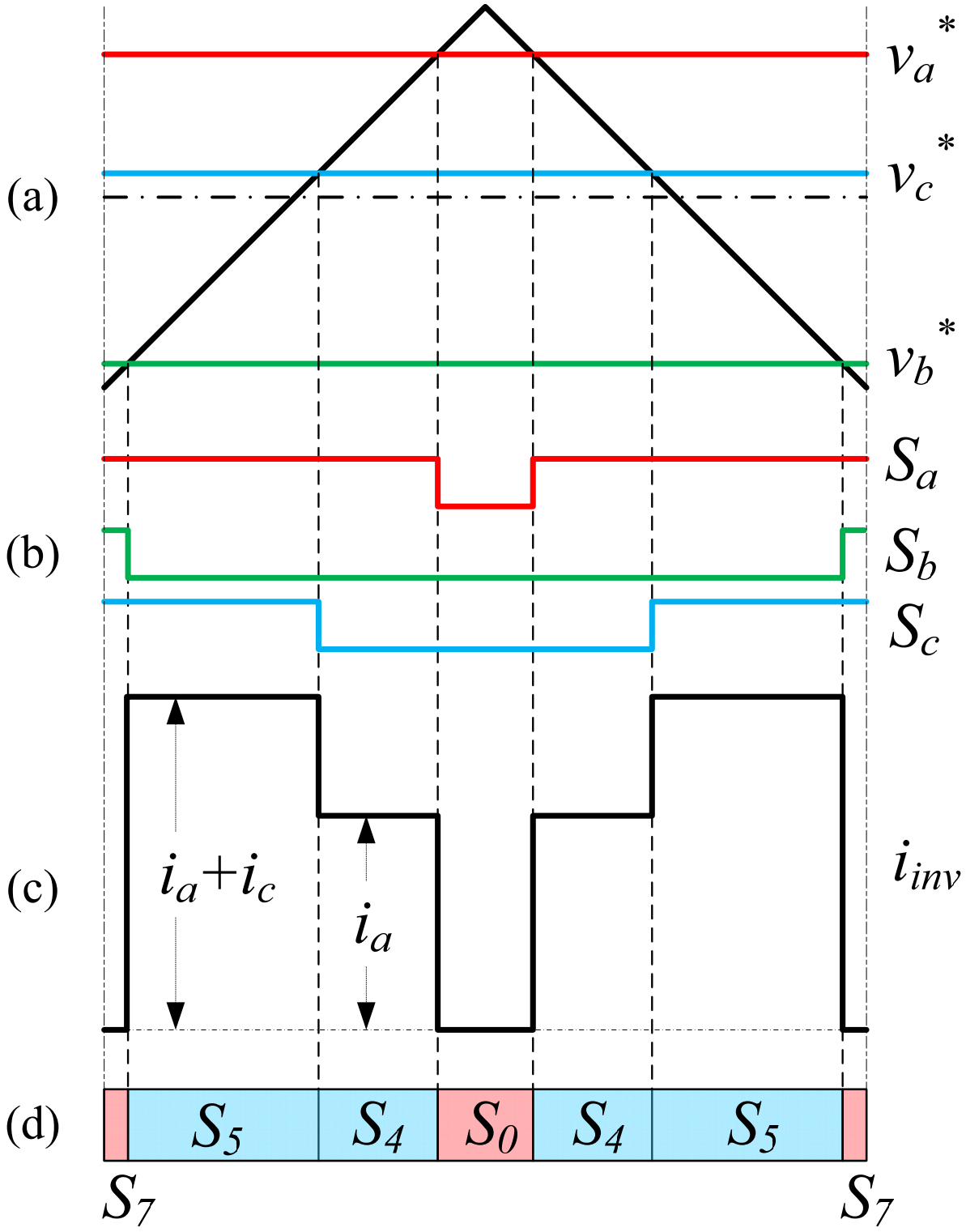

Figure 6.5 Detailed waveforms of SPWM in one switching period. (a) Sinusoidal reference and triangle carrier waveforms; (b) Switching functions S_a, S_b and S_c of phase A, B and C; (c) Ideal inverter input current i_{inv}; (d) Non-zero (active state) and zero (zero state) current portions in blocks.

Figure 6.5 shows the detailed SPWM inverter input current waveform in one switching period during this 60° sector of $v_a^* > v_c^* > v_b^*$. Therefore, v_a^* actually refers to the maximum phase voltage, v_c^* indicating the middle one and v_b^* represents the minimum phase voltage within this sector. It can be seen from Figure 6.5 (d) that the ideal SPWM inverter input current i_{inv} waveform is composed of two parts: the blue blocks indicating the non-zero current portion and the pink blocks stands for the zero current part. The analytical equations respect of the time for each portion can be obtained as shown in (6.1).

$$\begin{aligned} S_0 &= 1 - S_a \\ S_4 &= \frac{1}{2}(S_a - S_c) \\ S_5 &= \frac{1}{2}(S_c - S_b) \\ S_7 &= \frac{1}{2}S_b \end{aligned} \tag{6.1}$$

where S_a, S_b and S_c are the switching functions expressed as in (6.2) [35].

$$\begin{aligned} S_a &= \frac{1}{2} + \frac{1}{2}MI \cdot \sin \omega t \\ S_b &= \frac{1}{2} + \frac{1}{2}MI \cdot \sin(\omega t - \frac{2}{3}\pi) \\ S_c &= \frac{1}{2} + \frac{1}{2}MI \cdot \sin(\omega t + \frac{2}{3}\pi) \end{aligned} \tag{6.2}$$

MI stands for the modulation index and ωt represents the instantaneous time. From Figure 6.5 (c), it can be easily understood that the ideal SPWM inverter input side dc link current waveform i_{inv}, which is ideally expected to be cancelled as much as possible in order to minimize the dc capacitance, is composed of two almost symmetrical pulses. That is why the extended summary [30] made a big step towards minimizing the current ripple of the dc link capacitor by making the converter's switching frequency double that of the inverter switching frequency.

From (1), (2) and Figure 6.4, it is obvious that the zero current portions S_0 and S_7, as shown in the pink blocks in Figure 6.5 (d), are changing with ωt, while the duty cycle of the boost converter is fixed, determined by the battery's current voltage and the required dc link voltage. This conflict cannot be satisfied unless we shift the output converter current pulses left or right to fit the position of the inverter input current pulses. Figure 6.6 shows the trend of the S_0 and $2S_7$ v.s. the degrees. If $1-D$ is between 0.134 and 0.25, where D is the duty cycle of the dc-dc converter, the ripple cancellation will achieve a better result.

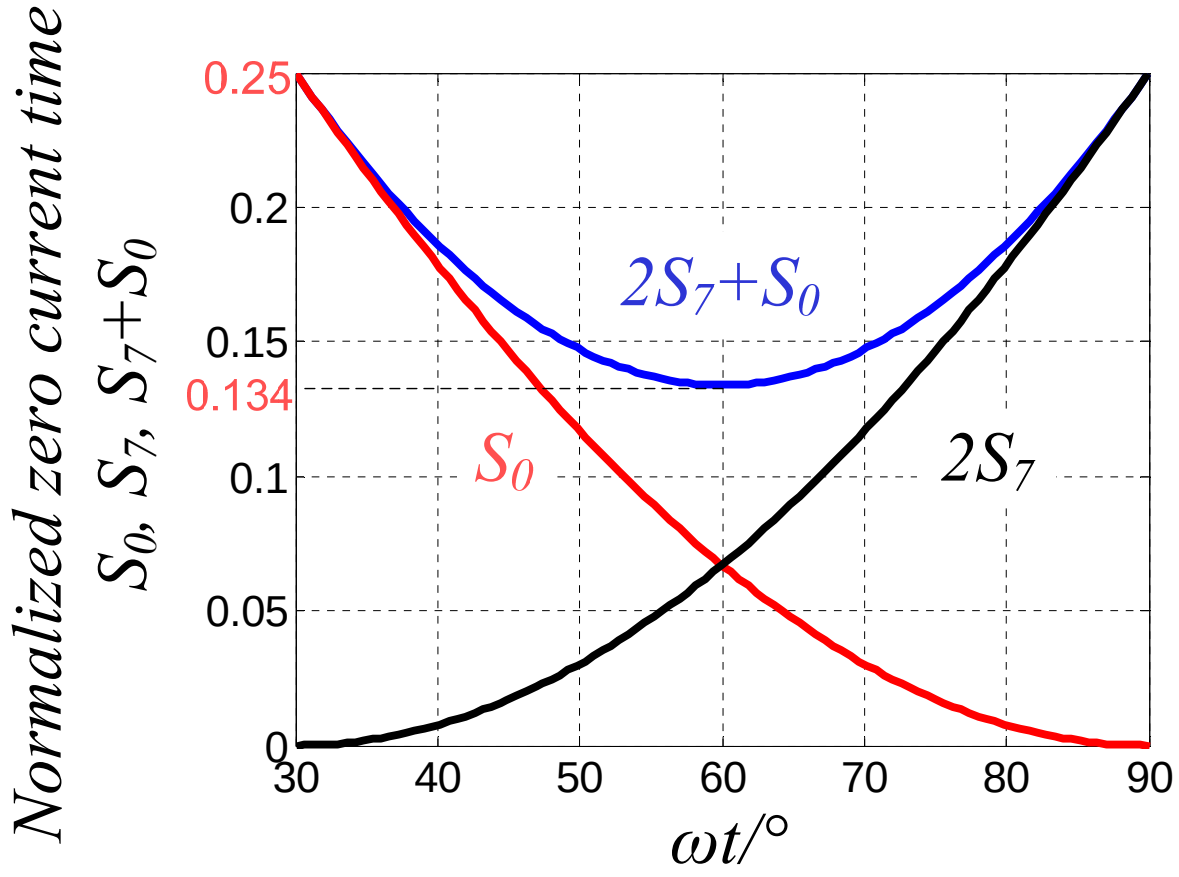

Figure 6.6 The trend of the S_0, $2S_7$, and S_0+2S_7 v.s. ωt

6.4 The Proposed Carrier Modulation Method for the Boost Converter

Considering pulse width modulation, there are usually two things that can be modified, the carrier and the reference. As discussed in section 6.2, the duty cycle of the boost converter is fixed. Hence, it is better to keep the reference as a straight horizontal line, and change the carrier to ensure the fixed duty cycle in each cycle, but at the same time shift the output current pulses of the dc-dc converter left or right to match with the inverter's input current.

In order to match the dc-dc converter output current pulses in Figure 6.2 (c), with the above described inverter input current pulses, there are several ways to generate this modulated carrier. Two of them are listed below as *A* and *B*. Please note that they are different, so that the resulted rms values of the dc link capacitor ripple current are different as well. However, since *A*—the linear method—involves in fewer harmonics, it has lower rms current ripples than the others.

6.4.1 Sine Carrier Modulation Method

If we just consider the middle point X of the left one pulse of the two shown as in Figure 6.7, the function of this shifting actually can be expressed as the length in (6.3).

$$\Delta T = \left(S_7 + \frac{S_5 + S_4}{2} \right) T_{sw} \tag{6.3}$$

where T_{sw} is the inverter switching period and ΔT is defined to be the time length from the starting point of the switching cycle to the above mentioned middle point X. Substitute (6.1) and (6.2) into (6.3) will achieve (6.4).

$$\Delta T = \frac{1}{4}(S_a + S_b)T_{sw} = \frac{T_{sw}}{4}\left[1 + \frac{1}{2}MI\sin\left(\omega t + \frac{\pi}{3}\right)\right] \tag{6.4}$$

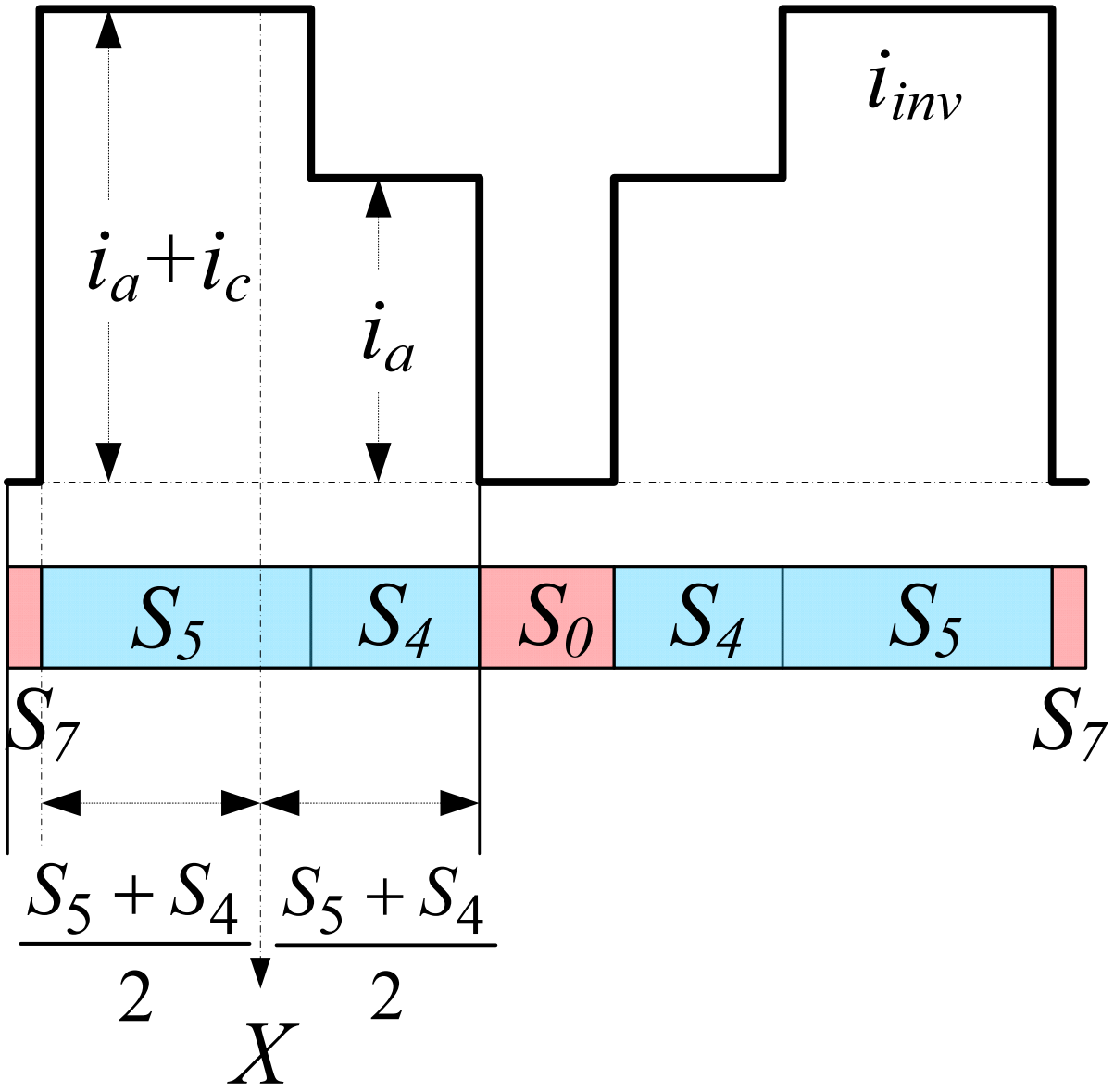

Figure 6.7 Sine carrier modulation method

6.4.2 Linear Carrier Modulation Method

A balanced system indicates that $S_a + S_b + S_c = 0$, therefore, $S_a + S_b = -S_c$. It can be noticed that ΔT in (6.4) is proportional to S_c, where again S_a is the maximum phase voltage, S_b is the minimum phase voltage, and S_c is the middle phase voltage.

As we all know, sine function is approaching linear around zero crossing point. Review Figure 6.3 or Figure 6.4 (a), the middle phase voltage can actually be simplified to a straight line crossing zero. This is the B method—linear carrier modulation method. The mathematical expression is written in (6.5).

$$\Delta T = \frac{T_{sw}}{2}\left(\frac{f_{sw}}{6f_0} - n\right), \quad n = 1, 2, \ldots, \frac{f_{sw}}{6f_0} \tag{6.5}$$

where ΔT is the same meaning as previous one, f_0 is the fundamental frequency, and n is the index number of each switching cycle.

It is quite simple and easy to realize both of them. Taking the sine carrier modulation method as an example, ΔT in (6.4) is actually a part of the sine function for each sector, but is very close to the ΔT in (6.5)—a triangle function. Based on the triangle theory and assuming the amplitude of the triangle carrier is 1, (6.6) and (6.7) are easy to get from observing Figure 6.8, where D is the boost converter's duty cycle. Please note that (6.4) has a minimum and maximum value of [1/4, 3/4], when ωt is between 30° and 90°, which means D in (6.6) and (6.7) can only be between [1/2, 1] to make sure V_x and V_y are between 0 and 1. With the assumption that the boost converter's duty cycle is usually under 2/3, in this case D is limited in the range of [1/2, 2/3]. Finally, the way to get S_{conv} is simply $S_x \oplus S_y$ as shown in Figure 6.8 .

$$\left.\begin{aligned} T_x &= \Delta T - \frac{1-D}{2}\frac{T_{sw}}{2} \\ \frac{T_x}{T_{sw}/2} &= \frac{V_x}{1} \end{aligned}\right\} \Rightarrow V_x = \frac{2\Delta T}{T_{sw}} - \frac{1-D}{2} \tag{6.6}$$

$$\left.\begin{aligned} T_y &= \Delta T + \frac{1-D}{2}\frac{T_{sw}}{2} \\ \frac{T_y}{T_{sw}/2} &= \frac{V_y}{1} \end{aligned}\right\} \Rightarrow V_y = \frac{2\Delta T}{T_{sw}} + \frac{1-D}{2} \tag{6.7}$$

The way to generate the sine carrier modulation is quite similar to [36].

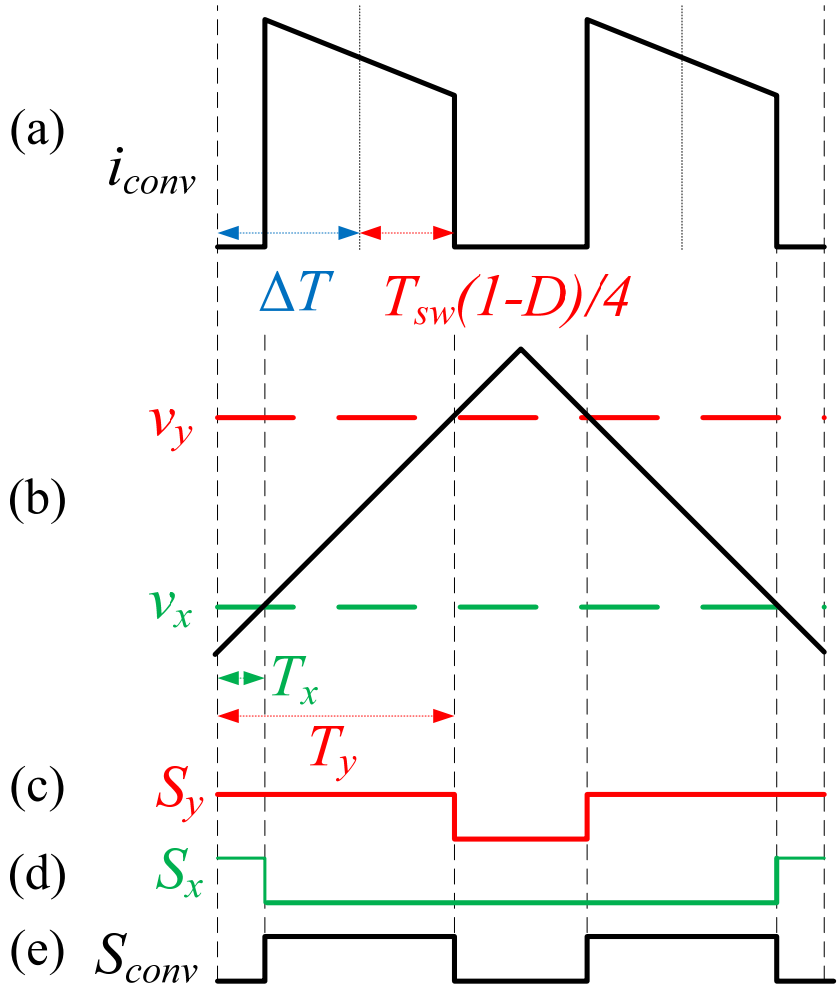

Figure 6.8 (a) The desired converter output current of the dc-dc converter; (b) Two references compared with the triangle carrier for the dc-dc converter; (c) Generated switching function of v_y; (d) Generated switching function of v_x; (e) Generate S_{conv} using $S_x \oplus S_y$

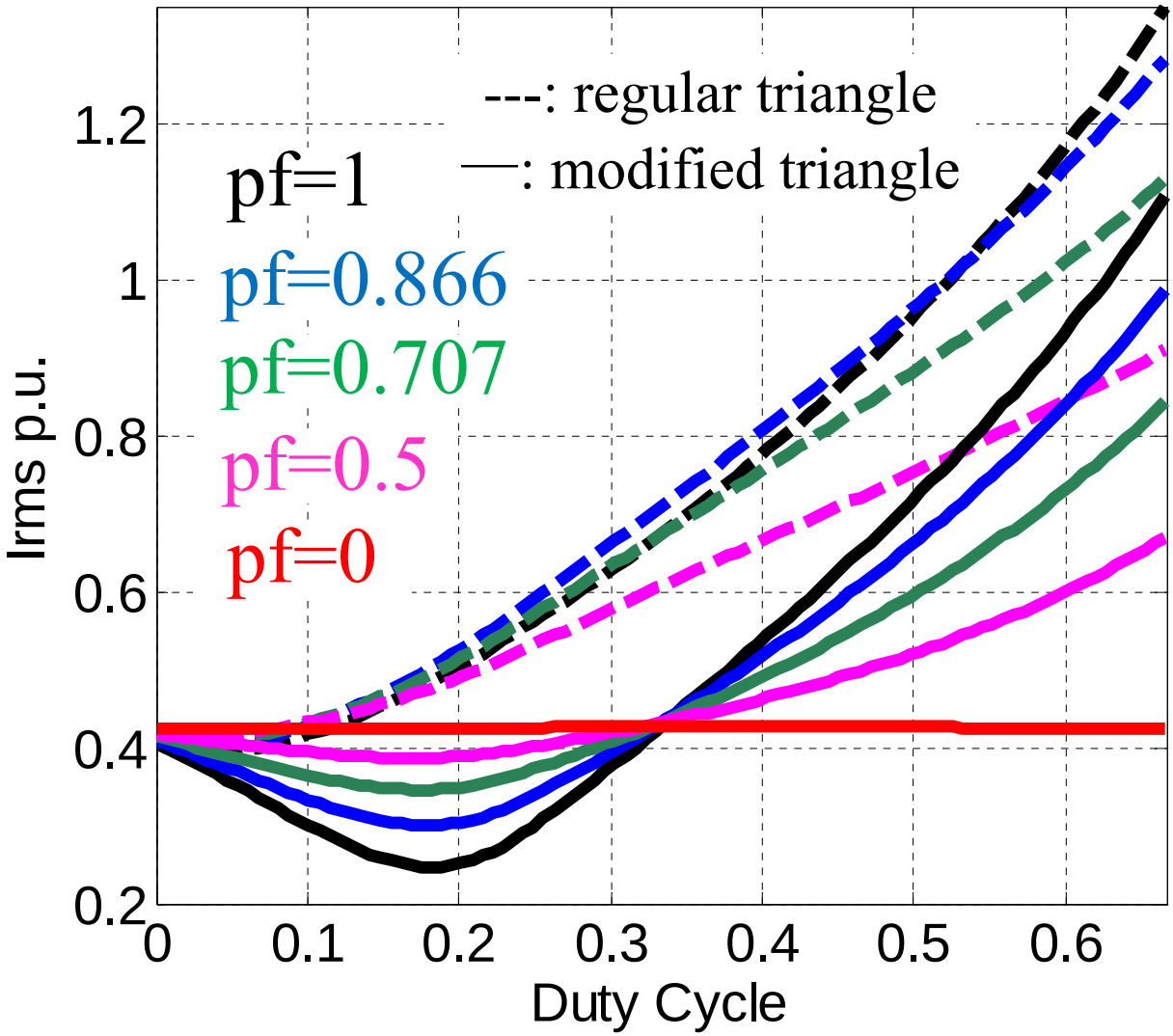

Figure 6.9 The comparison of I_{RMS} between the regular PWM strategy and modified linear carrier modulation method

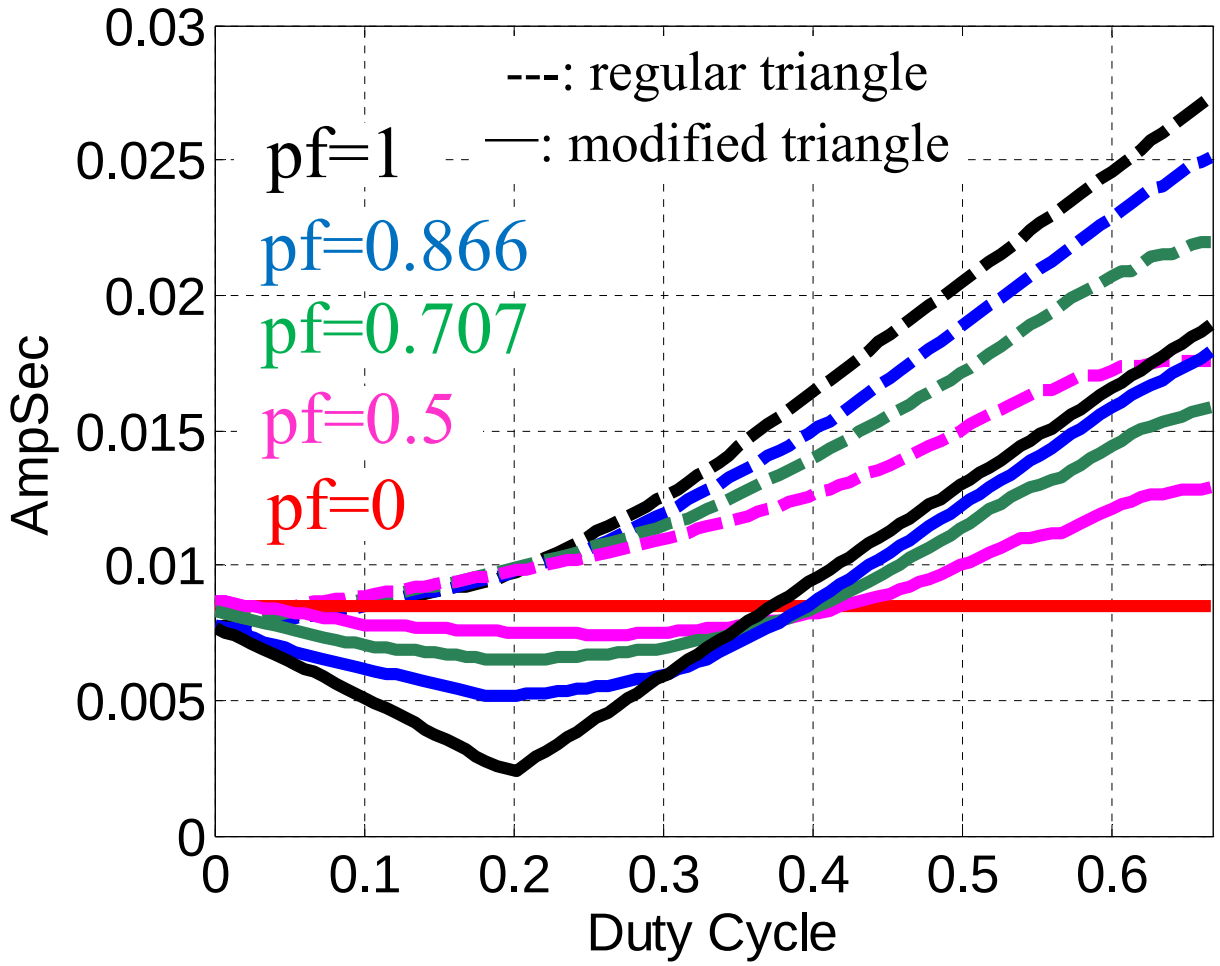

Figure 6.10 The comparison of *A·sec* between the regular PWM strategy and modified linear carrier modulation method

6.5 Experimental Results

The experiment was conducted under the following conditions: the dc-dc input voltage is 200 V generated by a three-phase diode rectifier with a large electrolytic capacitor bank, dc-dc converter duty cycle is 1/3, the dc link voltage is 300 V, the inverter switching frequency is 10.8 kHz, the equivalent dc-dc converter switching frequency is 21.6 kHz, the fundamental frequency is 60 Hz, and the p.f. is around 0.884 with a 3.5 mH inductor and a 2.5 Ω resistor in series

connected in wye. The inverter is operated under the SPWM normal modulation method with a modulation index of 0.92.

One thing has to be mentioned here: since the inverter's dc link capacitor banks are connected to the IGBT pack through busbars, which preventing direct measurement of the inverter input current, the same thing on the converter side. Therefore, the inverter current is obtained by (6.8) based on measurement of the output currents and switching signals from the DSP, while the converter output current is obtained by (6.9).

$$i_{inv} = S_a i_a + S_b i_b - S_c (i_a + i_b) \tag{6.8}$$

$$i_{conv} = S_{conv} i_L \tag{6.9}$$

This requires at least 2 current sensors and 3 voltage sensors for the inverter input current measurement and 1 current sensor and 1 voltage sensor for the converter output current measurement. The available oscilloscopes have 4 analog channels with enough digital inputs, however, the math function (6.10) cannot apply to the already calculated i_{inv} and i_{conv}. Therefore, the experimental results that have more than 3 waveforms on the same graph are done by saving "waveform"—data file *.wvf*—on the oscilloscope and redrawn on the computer by *WVF Viewer* software from Yokogawa.

$$i_{cap} = i_{conv} - i_{inv} \tag{6.10}$$

Table 6.1 shows the saber simulation of the four different modulation methods. First one is the original method with the same switching frequency for both the converter and inverter. Second is that the converter switching frequency is twice as much as the inverter switching frequency. Third method is, based on second one, shift the converter output current pulses using linear carrier modulation method proposed in this paper. The last one is the sine carrier

modulation method. It can be seen that the linear carrier modulation method achieves the best result, and around 17%~20% reduction of the current ripple based on the second method is made.

Table 6.1 Saber Simulation Result of The rms Value of The DC Link Capacitor's Ripple Current

Condition	I_{cap_rms}
$f_{conv} = f_{inv}$	*26.531 A*
$f_{conv} = 2f_{inv}$	*19.271 A*
$f_{conv} = 2f_{inv}$ with linear carrier modulation	*15.656 A*
$f_{conv} = 2f_{inv}$ with sine carrier modulation	*15.704 A*

Figure 6.11 Shows the experimental results of the rms ripple current of the dc link capacitor is 15.651 A at 300 V dc link voltage, and it is highly agreed with the SABER simulation in table I row 3. Figure 6.12 shows the synchronized the inverter phase A reference signal (yellow) with the converter V_x and V_y low frequency triangle reference signal (V_x is green and V_y is Purple). The ripples on these signals are due to the reason that they are got from the PWM signals after a low pass RC filter. Figure 6.13 shows the S_x, S_y and S_{conv} for the proposed linear carrier modulation method. It can be seen that the switching signal of S_{conv}, achieved by $S_x \oplus S_y$, is shifting its pulses in one inverter switching cycle left and right. Figure 6.14 shows how the converter output current is gotten from (6.9). Digital and analog signals are separated by the oscilloscope automatically. Figure 6.15 and Figure 6.16 show the how the inverter input current is gotten from (6.8). Figure 6.17 and Figure 6.18 show the capacitor current got from (6.10) with the converter output current and the inverter input current, for comparison. Finally, Figure 6.19 gives

the SABER simulation for a comparison with Figure 6.18. The simulation result and the experimental result are very similar, and the only difference is the experimental result has a 6ω component involved in the converter output current due to the diode rectifier at the input side.

Group1 Trigger Time: 10/07/22 22:14:43			Number of Data: 10020
	I_inv	I_conv	I_cap
Max	43.85254E+00 A	55.56641E+00 A	79.47754E+00 A
Min	-32.22656E+00 A	0.000000E+00 A	-43.73535E+00 A
High	43.37704E+00 A	54.41340E+00 A	53.88007E+00 A
Low	-7.061005E-03 A	0.000000E+00 A	-7.233532E+00 A
P-P	76.07910E+00 A	55.56641E+00 A	123.2129E+00 A
Ampl	43.38411E+00 A	54.41340E+00 A	61.11360E+00 A
Avg	26.06004E+00 A	26.11510E+00 A	54.39223E-03 A
Rms	31.00015E+00 A	32.65733E+00 A	15.65157E+00 A
Middle	5.812988E+00 A	27.78320E+00 A	17.87109E+00 A
StdDev	16.789	19.608	15.651
Oshoot	1.10 %	2.12 %	41.89 %
Ushoot	74.27 %	0.00 %	59.73 %
Rise	0.0000 s	0.0000 s	24.999us
Fall	0.0000 s	24.999us	19.999us
Freq	11.111kHz	28.571kHz	10.526kHz
Period	90.000us	35.000us	95.000us
+Duty	77.78 %	85.71 %	5.26 %
-Duty	22.22 %	14.29 %	94.74 %
+Width	70.000us	29.999us	4.9999us
-Width	19.999us	4.9999us	90.000us

Figure 6.11 The experimental result of the rms ripple current is 15.651 A at 300 V dc link voltage (Analyzed from the saved data by WVF Viewer from Yokogawa)

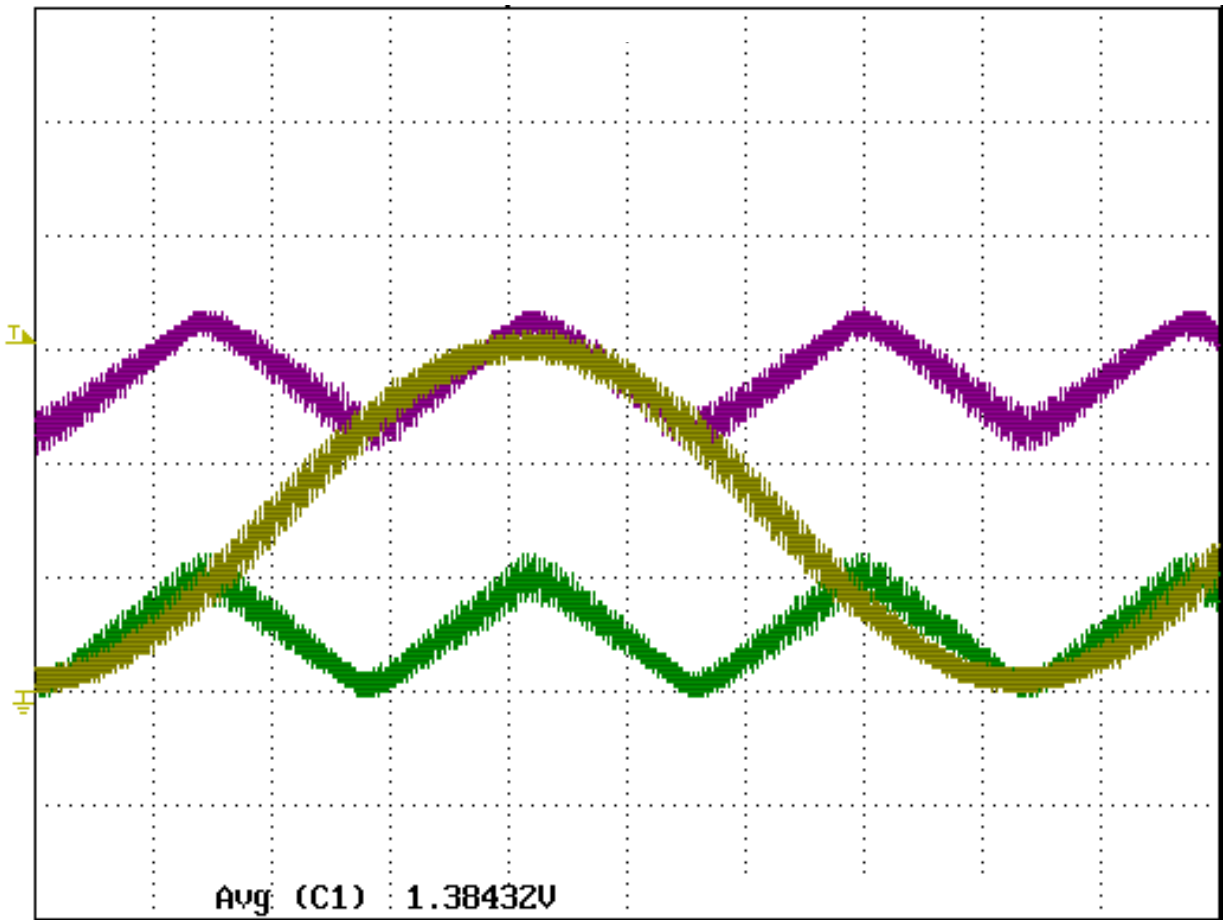

Figure 6.12 Synchronized the inverter phase A reference signal (yellow) with the converter V_x and V_y low frequency triangle reference signal (V_x is green and V_y is Purple)

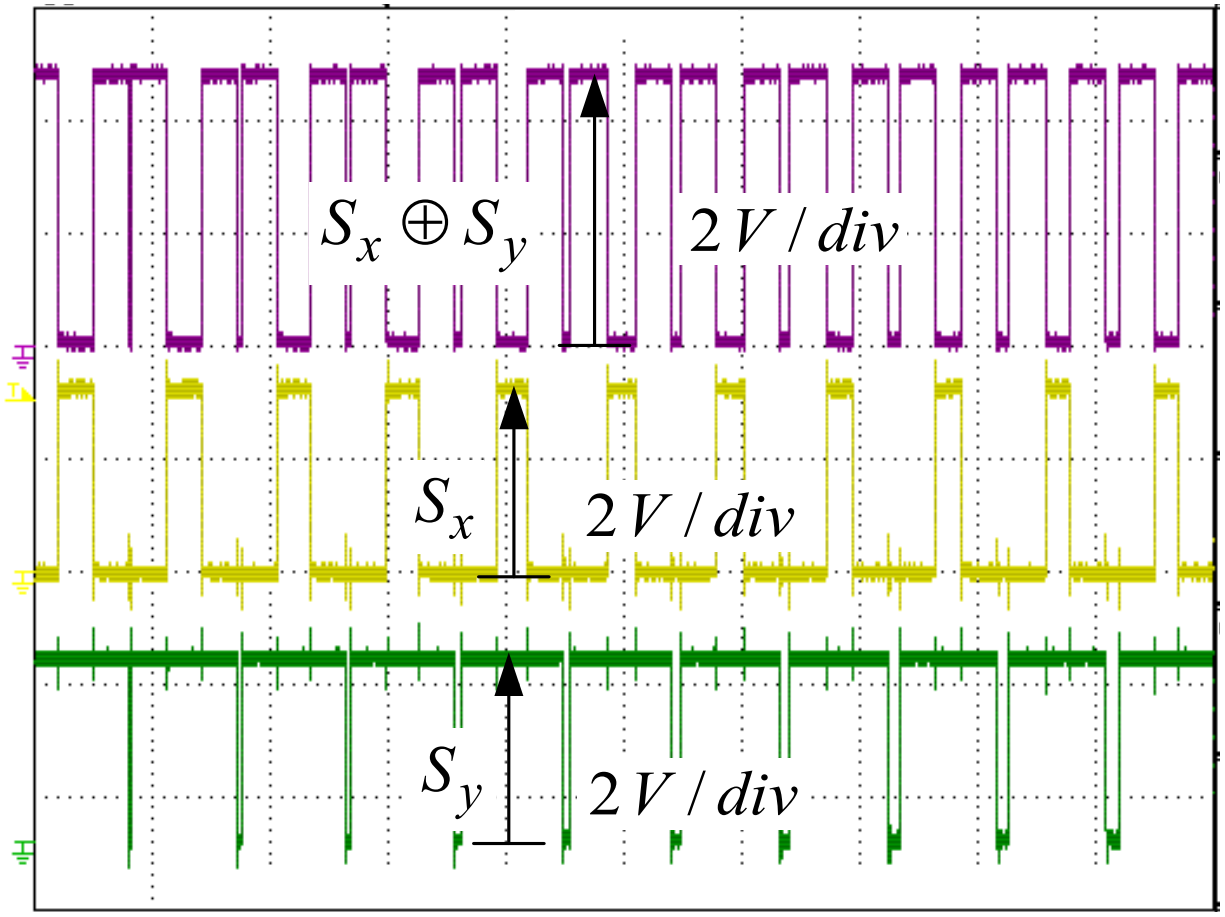

Figure 6.13 The experimental result of the proposed carrier modulation signal for dc-dc boost converter

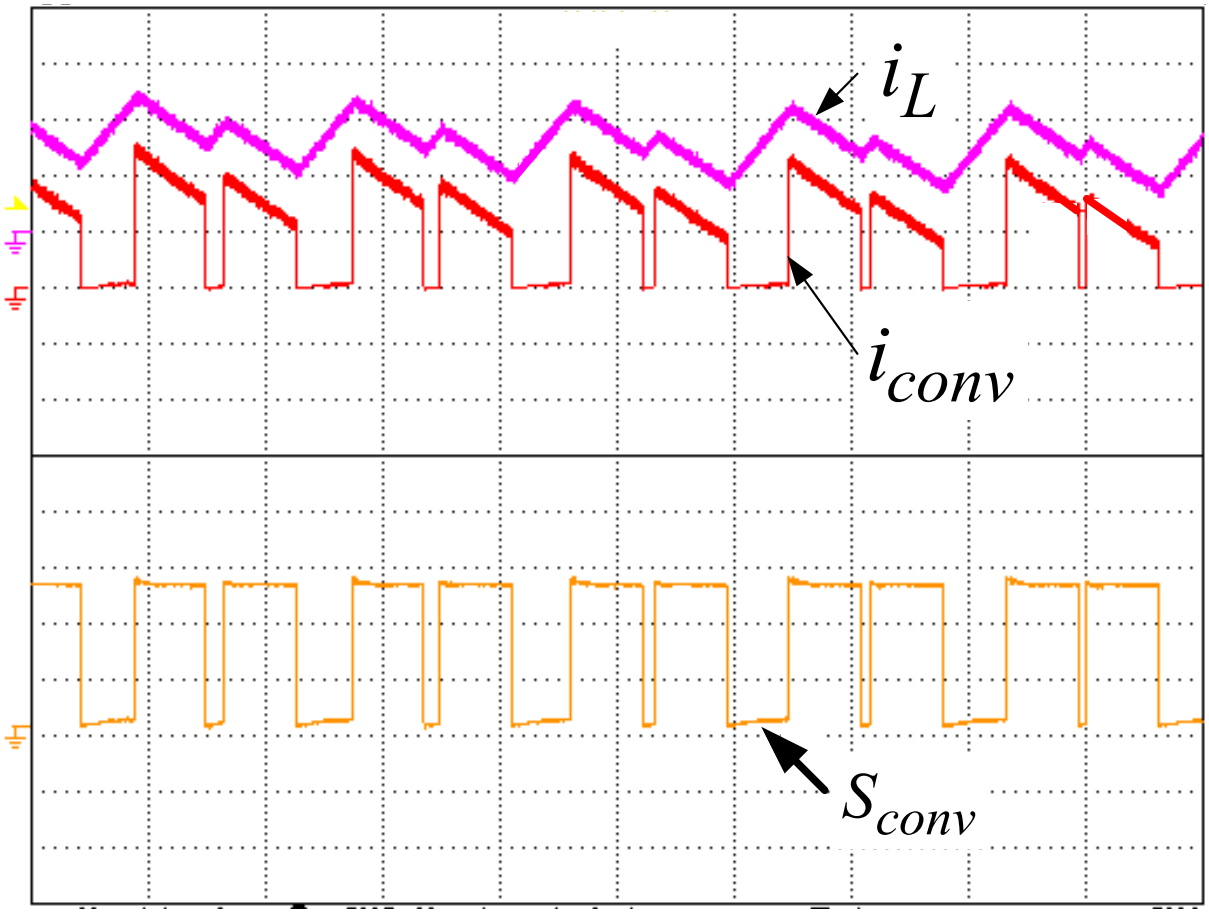

Figure 6.14 The experimental results of the inductor current, the converter output current and the switching signal of the dc-dc boost converter

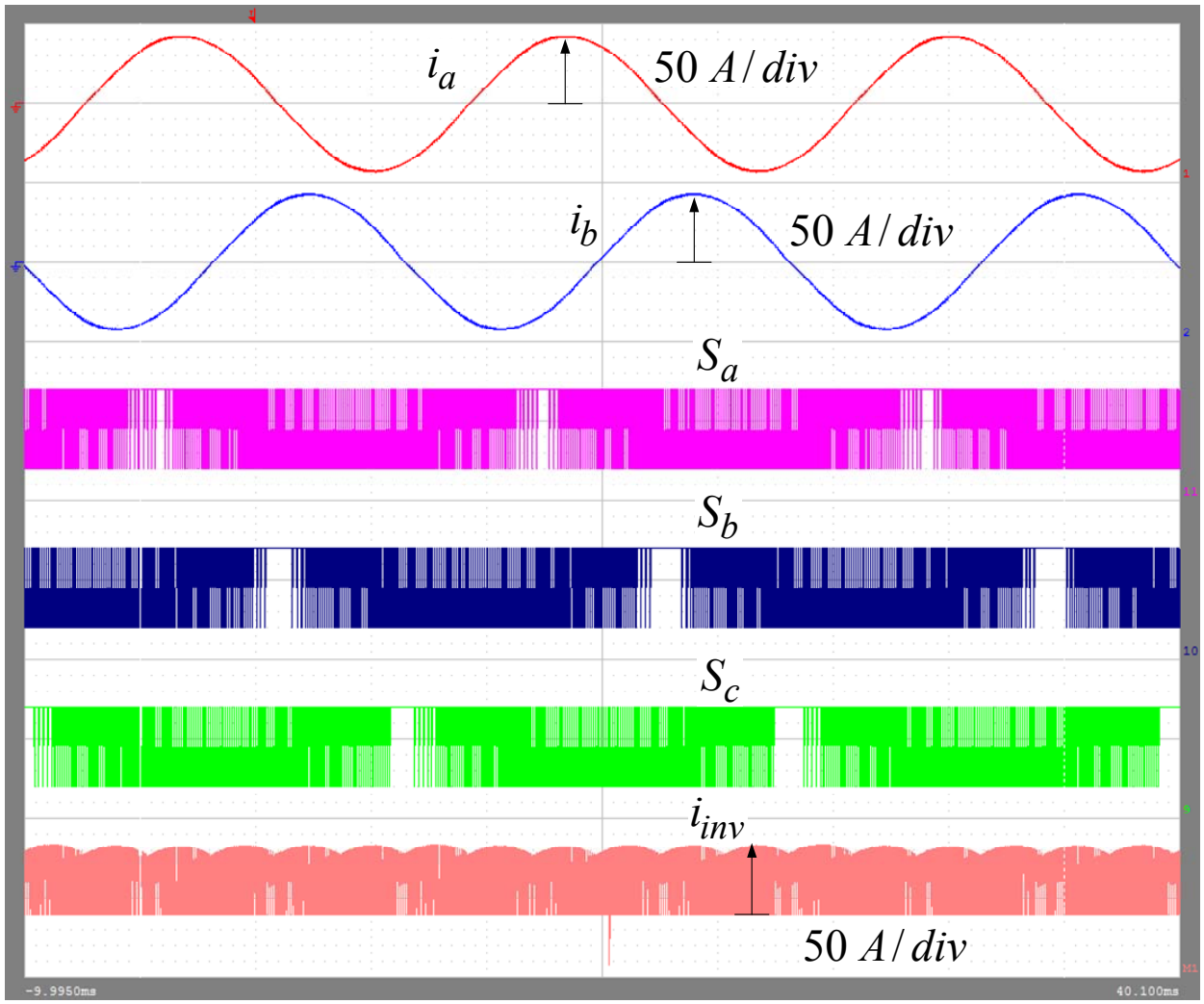

Figure 6.15 The experimental results of the inverter output currents, the switching functions, and the input current of the SPWM inverter (Redraw the waveforms from the saved data by WVF Viewer from Yokogawa)

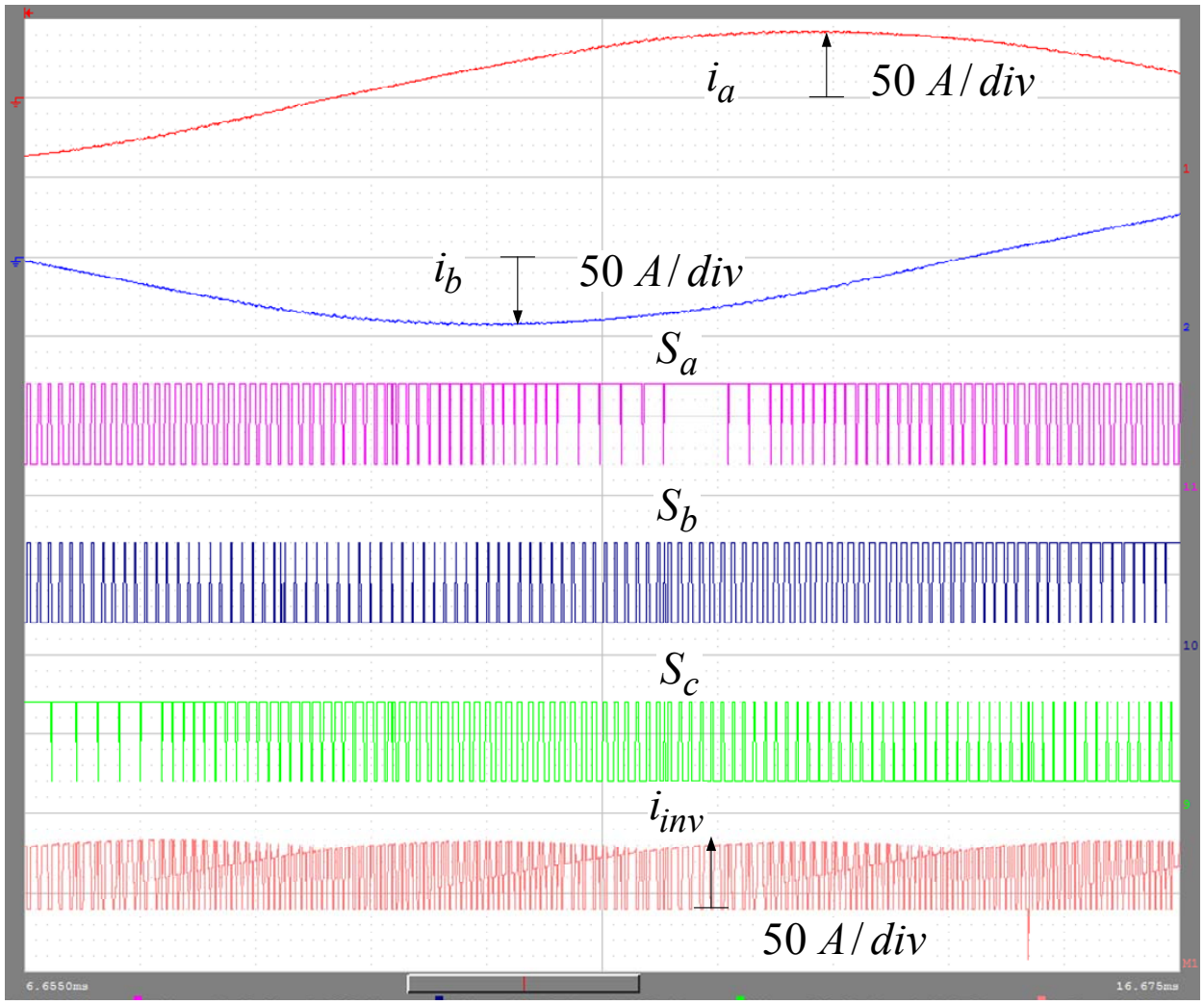

Figure 6.16 Zoom in view of Figure 6.15

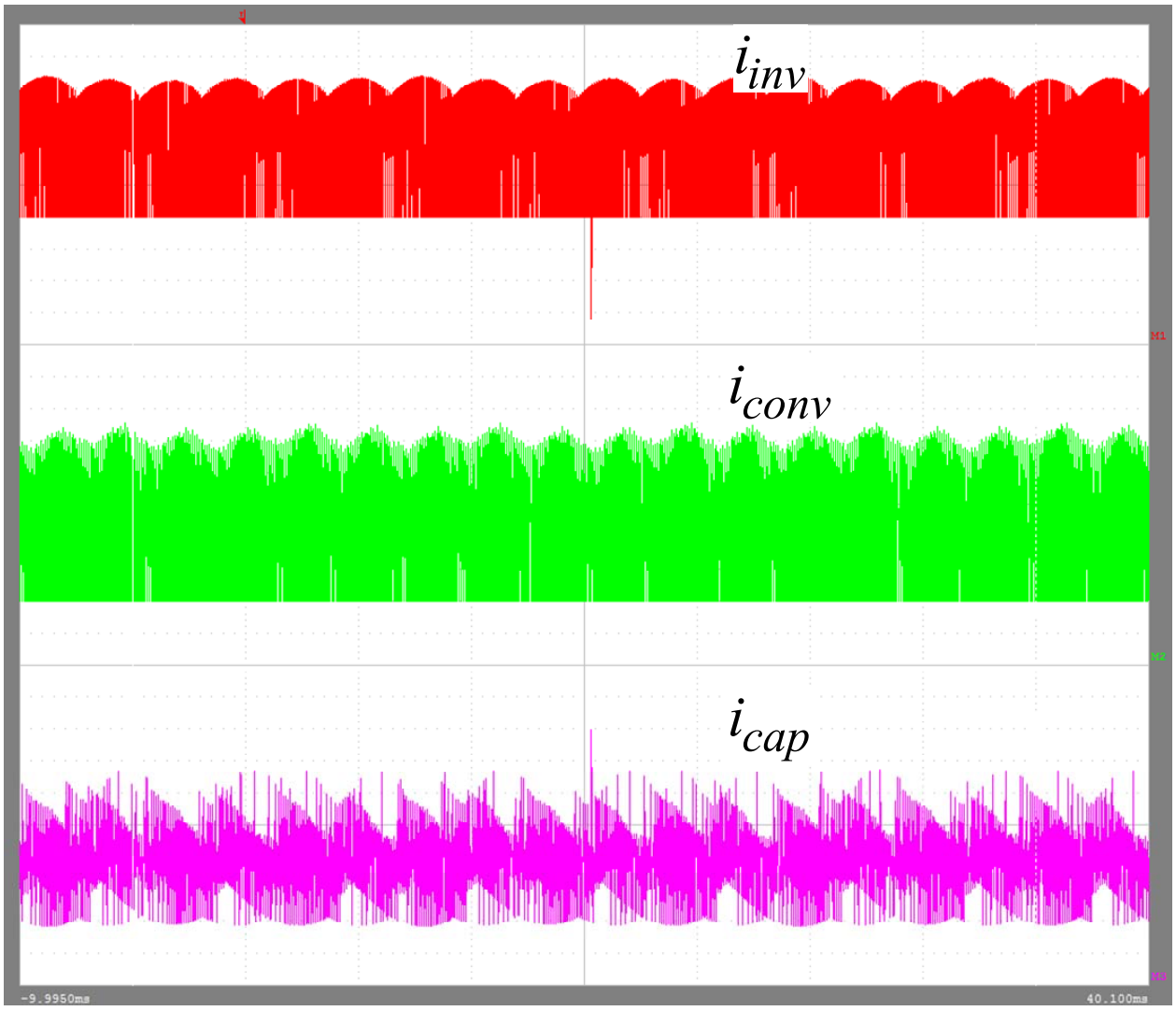

Figure 6.17 Experimental results of the inverter input current, the converter output current, and the DC link capacitor current (Redraw the waveforms from the saved data by WVF Viewer from Yokogawa)

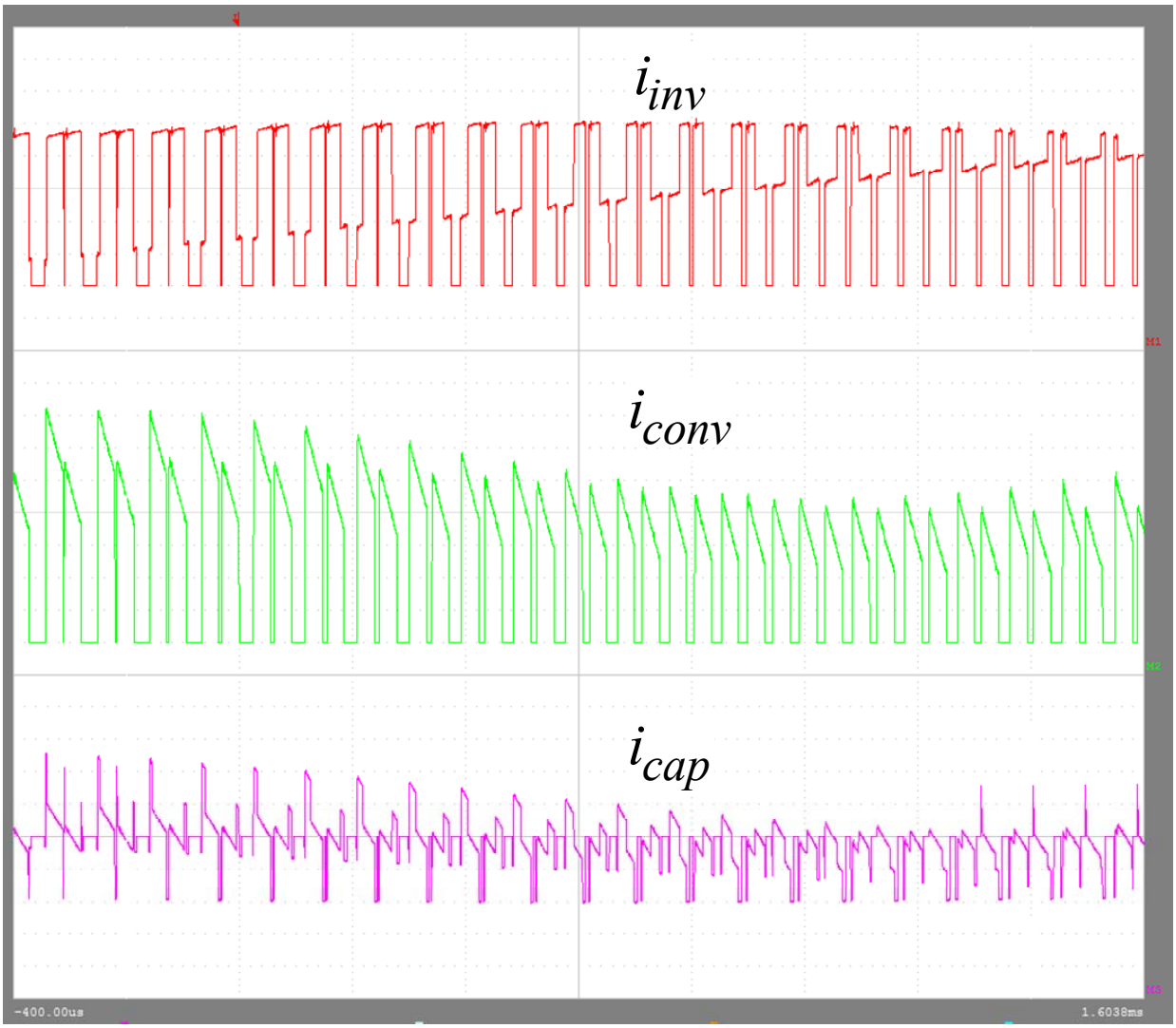

Figure 6.18 Zoom in of Figure 6.17.

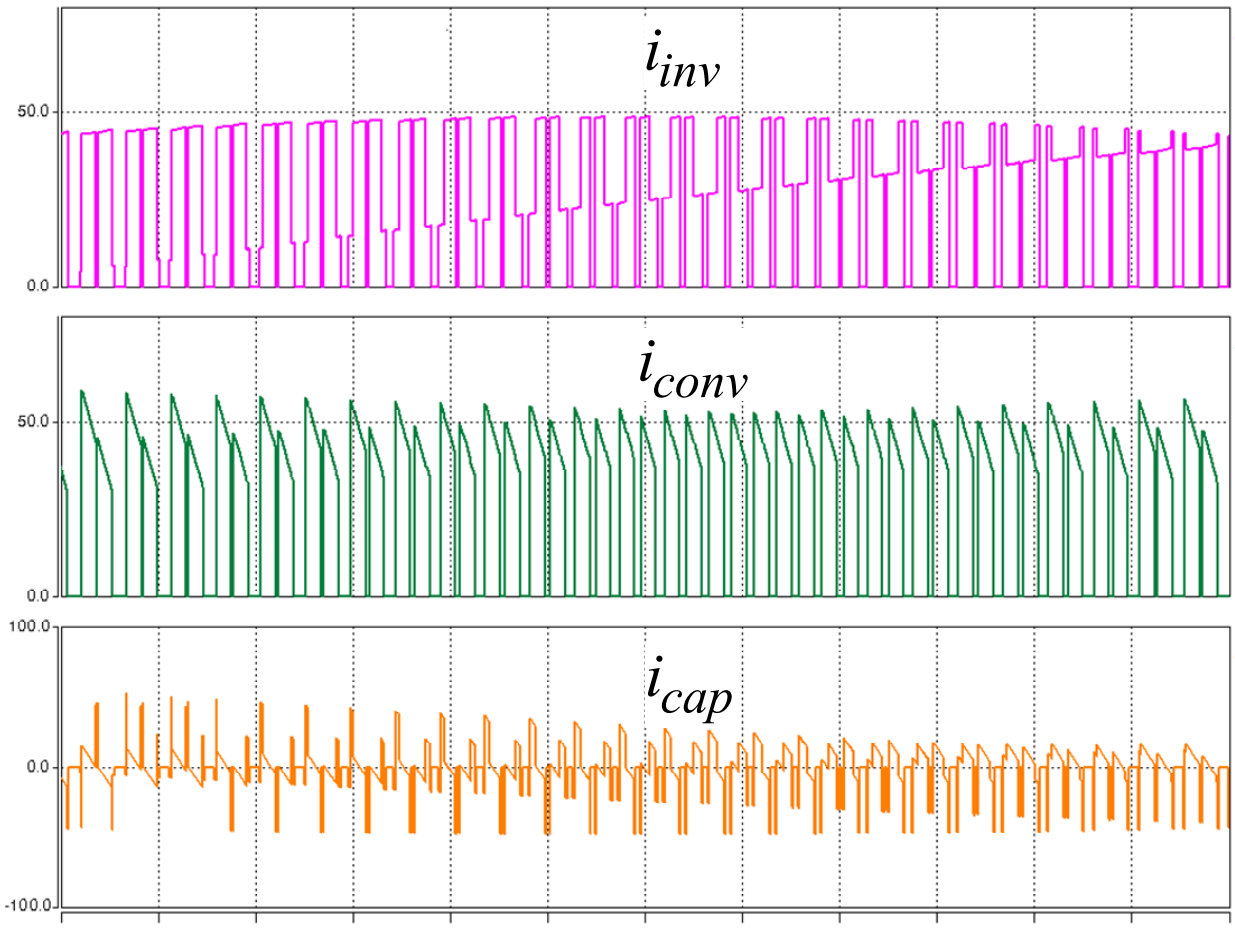

Figure 6.19 The SABER simulation results of the dc link capacitor current (comparison for Figure 6.18)

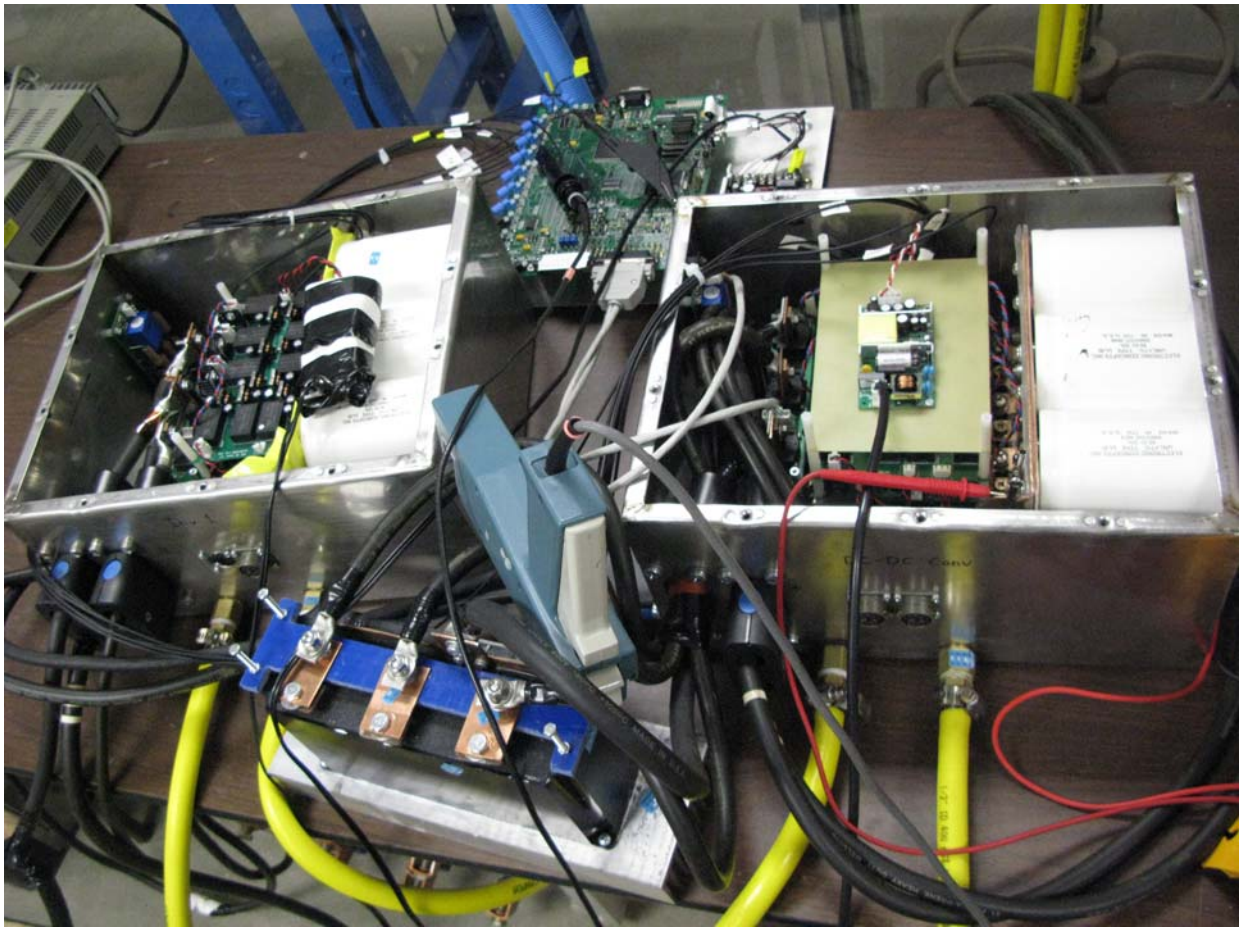

Figure 6.20 Prototype setup

6.6 Conclusion

Around 17%~20% reduction of the current ripple based on the already reduced current ripple in [30] is realized by using the proposed carrier modulation method, which leads to the minimization of the dc capacitance. Due to the reduced current ripple, the voltage ripple of the dc link is reduced as well. The proposed method has the merits of simple and easy realization. There is no requirement of any fast feedback and complicated close-loop control blocks, but gives significant dc link ripple reduction and dc link capacitance minimization.

CHAPTER 7 Contribution and Future Work

7.1 Contributions

The contributions presented in this thesis are listed in short conclusions below:

- Theoretical equations to express capacitance versus voltage ripple and rms ripple current versus modulation index have been developed for SPWM, 6-step operation, as well as for diode rectifier, which provides better design/calculation of the required dc capacitance and better insights into the limits and optimum operation of the converter/inverter system, than the traditional empirical equations and simulations.
- From the theory developed above, a carrier modulation method for the dc-dc converter, which synchronizes the dc-dc converter with the SPWM inverter in the HEV system, is further proposed. This is also able to minimize the dc capacitance and dc current ripples through the improved PWM methods.

7.2 Future Work

- Although this thesis has basically covered all the topologies and operation methods that exists in the HEV system nowadays, all the analysis are assumed to be ideal. However, in the real system, the situation would not be closed to ideal all the time. Any oscillation or saturation happened would push the circuit condition into a non-ideal case, which needs to be researched more in details.

- The proposed theory and PWM methods are all based on open loop control, which is the very first step of minimizing the dc link capacitance. The next step would be, on this basis by knowing the minimum value under open loop, further minimizing the dc capacitance would be realized by utilizing close-loop control.

Appendix

Appendix- Proof of Switching Functions

Fig. 3(a) shows the three sinusoidal references and the triangle carrier waveform for two switching periods. Assume the switching period is T_{sw}, the turn off time during a switching cycle of the phase A upper switch is T_{offa}, and the DC link voltage is V_{dc}.

As one may notice, the blue right angle triangle is similar to the red right angle triangle. Therefore, a relationship (A. 1) is obtained.

$$\frac{\frac{V_{dc}}{2} - v_{an}}{\frac{T_{offa}}{2}} = \frac{\frac{V_{dc}}{2}}{\frac{T_{sw}}{4}} \tag{A. 2}$$

By substituting (2.1) and (2.4), (A. 3) is achieved.

$$T_{offa} = T_{sw}\left(\frac{1}{2} - \frac{1}{2}MI \cdot \sin\omega t - \frac{v_{3\omega}}{V_{dc}}\right) \tag{A. 4}$$

Therefore, the expression of S_a is obvious:

$$S_a = (1 - \frac{T_{offa}}{T_{sw}}) \tag{A. 5}$$

Substituting (A. 6) into (A. 7) will give the expression of switching functions as (2.3).

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