ATOMICALLY THIN TWO-DIMENSIONAL MATERIALS FOR NANOELECTRONIC AND OPTOELECTRONIC DEVICE APPLICATIONS

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A DISSERTATION

Submitted
to Michigan State University
in partial fulfillment of the requirements
for the degree of

Electrical Engineering – Doctor of Philosophy

2018

ABSTRACT

ATOMICALLY THIN TWO-DIMENSIONAL MATERIALS FOR NANOELECTRONIC AND OPTOELECTRONIC DEVICE APPLICATIONS

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Through this thesis proposal, the author has demonstrated a variety of electronic and optoelectronic nanodevices including ultrascaled transistors, heterostructure diodes, chemical sensors, photodetectors and single-pixel infrared cameras using atomically thin two-dimensional (2D) materials such as graphene, molybdenum disulfide (MoS_2) and black phosphorus (BP).

As the scaling of the silicon-based transistor approaches its physical limit, exploratory research is needed to develop alternative channel materials for future sub-5 nm gate length devices. For such an ultrascaled electronic device, short channel effects would severely limit its performance and operation. In order to suppress the short channel effects at extreme scaling limits, the thickness of the channel material needs to be less than roughly one-third of the gate length in order to allow the gate to retain its effective electrostatic control of channel carrier concentration. However, for conventional bulk semiconductors such as silicon, germanium and gallium arsenide, the rough surface of the ultrathin body (a few atomic layers) would lead to severe surface scattering for carriers, resulting in severely degraded carrier mobility. In this regard, atomically thin 2D layered materials are excellent candidates for future ultimately scaled electronic and optoelectronic device applications. Compared with 3D bulk materials, 2D materials exhibit many exceptional properties. First, quantum confinement effect in the direction perpendicular to the 2D plane leads to many novel electronic and optical properties that are dramatically different from their bulk counterparts. Second, their surfaces are atomically smooth and free of dangling bonds and defect states, which lead to intrinsically low surface scattering and make it easy to integrate 2D films with photonic structures. It is also possible to construct heterostructures using different 2D

materials without the conventional lattice mismatch issues. Third, despite being atomically thin nature, many 2D materials interact strongly with light and cover a very broad range of electromagnetic spectrum. Finally, these atomically thin 2D materials are immune to short channel effects owing to their small thickness.

In this thesis, we will discuss the electronic and optoelectronic device applications using atomically thin 2D materials including graphene, MoS_2 and BP. We mainly discuss the 2D BP which is the most stable and least reactive form of element phosphorus, and was discovered in bulk form 100 years ago. Unlike zero bandgap graphene, BP is a direct bandgap semiconductor with a thickness-dependent bandgap ranging from 0.3 eV (bulk) to 2.0 eV (monolayer). Few-layer BP flakes have been used as channel materials in field-effect transistors (FETs). Such BP FETs exhibit high on-off current ratios of 10^4-10^5. And, the room temperature field-effect mobility of BP FETs is up to 1000 $cm^2V^{-1}s^{-1}$ which is much higher than that of 2D MoS_2 based FETs.

To my family and friends, for their unconditional support.

ACKNOWLEDGMENTS

During my Ph.D. program, I met many people who have influenced me a lot and shaped me into the person I am today. First, I would like to thank my advisor Dr. Chuan Wang who gives me the opportunity to do research in his group as a doctoral student. And I am very grateful to his continuous support, encouragement, inspiration and invaluable instruction throughout my doctoral period. I would also want to thank my committee members Dr. Lixin Dong, Dr. Nelson Sepulveda and Dr. Junghoon Yeom for their constructive guidance and valuable feedback.

I appreciate all the support from my colleagues in Flexible Electronics Group. Dr. Le Cai and Dr. Suoming Zhang have contributed a lot to my research. As co-workers, they provide a lot of helpful suggestions while doing research together. I would also express thanks to other group members: Zhihao Xu, Yiheng Zhang, Haochuan Wan, Dr. Lei Zhang, Dr. Min Yu, Martin Scherr, Dr. Qinqin Wei, Tianhang Sun and Qifan Wang. All of you guys have made my life in MSU splendid and enjoyable.

I would like to thank our collaborators. Thank Dr. Weida Hu and Qing Li for helping us simulate 2D nanodevices using Synopsys Sentaurus TCAD. Thank Dr. Zhixian Zhou and Arthur Bowman for helping us characterize 2D heterostructure diodes at low-temperature. Thank Dr. Lixin Dong and Dr. Bo Song for helping us design single-pixel infrared camera apparatus. Thank Dr. Timothy Grotjohn, Dr. Xiaobo Tan, Dr. Wen Li, Dr. Tim Hogan, Dr. Chunqi Qian for their guidance and valuable suggestions. Thank all the research stuff and secretary including Dr. Baokang Bi, Brian Wright, Karl Dersch, Roxanne Peacock, Laurie Rashild and Meagan Kroll for their assistance along my Ph.D. period.

I would be very grateful to my friends in MSU including Dr. Tongyu Wang, Dr. Wei Li, Dr. Yaozhong Zhang, Xiaolu Huang, Aryan Mehboudi, Hongyang Shi, Thassyo Pinto, Heyu Yin, Dan Liu, Kuan Zhu, Qi Wang, Yuchen Cao, Xingze Mao, Han Liu, Xue Jiang,

Chaojian Hou, Ziqing Cao, Dr. Tung-Yi Lin, et al. I cherish the friendship of you guys and me feverishly.

Finally, special thanks should go to my lovely family for their supports and unconditional love. Especially, my wife, Yuan Wu, has encouraged and supported me with her endless love. Thank you!

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CHAPTER 1

INTRODUCTION

For more than four decades, the silicon based metal-oxide-semiconductor field-effect transistors (MOSFETs) have been the workhorse of today's semiconductor electronics industry. MOSFETs are the basic building blocks of modern microprocessors, memory chips and telecommunication circuits. And the progress in these fields greatly depends on improvement of MOSFET performance. In recent years, the overall semiconductor chip market has an annual volume of about 300 billion US dollars.[3, 1, 2] And the digital integrated circuits (ICs) account for 70% of the overall chip market.[2] As we know, today's digital ICs are built from CMOS structure using both n-channel (electrons dominate transistor's current) and p-channel (holes dominate transistor's current) transistors. As the dimension of silicon MOSFET continues to scale down, the integration and speed level of silicon CMOS ICs have dramatically progressed in the past few decades.[3] A modern microprocessor has more than 2 billion silicon MOSFETs, and a 32 gigabyte memory card contains a staggering 256 billion transistors, which is comparable to the number of stars in the Milky Way.[1] MOSFETs are mainly used in logic devices and circuits, though they can fulfill other purposes.

1.1 Background

1.1.1 MOSFET Device Structure

A textbook example of typical silicon n-channel MOSFET is presented in Figure 1.1.[1] There are four basic MOSFET device types which are n-channel enhancement mode MOSFET, n-channel depletion mode MOSFET, p-channel enhancement mode MOSFET, and p-channel depletion mode MOSFET.[27] Here, we only show n-channel enhancement mode MOSFET for simplicity. The n-channel MOSFET device has two heavily doped n-type semiconductor

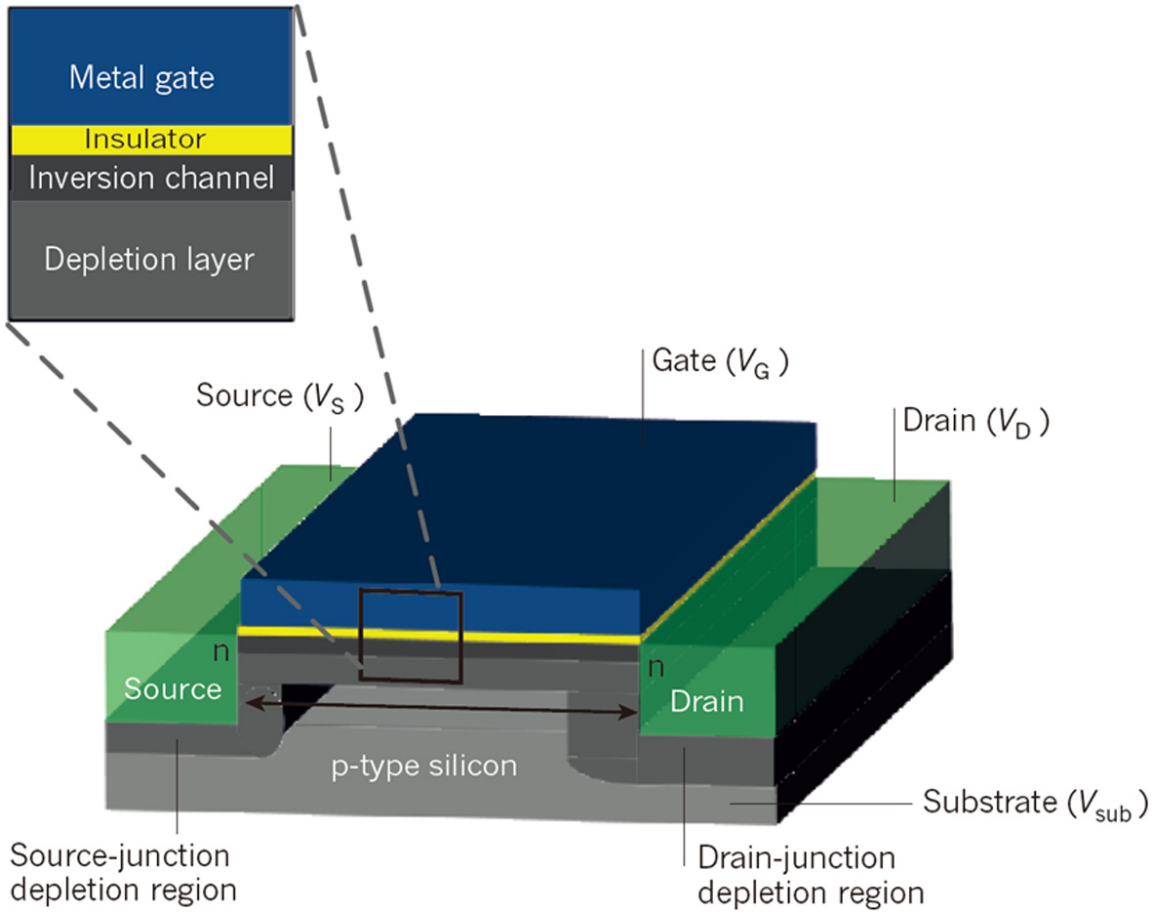

Figure 1.1 A schematic view of a classical bulk n-channel MOSFET. Two n-type regions called the source and the drain are formed on a p-type substrate. A gate stack composed of an insulator and a metal gate electrode is placed above the p-type substrate between the source and the drain. When a positive bias is applied to the gate, electrons from the source and the drain are attracted by the gate and form an inversion layer, which is called the channel. The channel connects the source and the drain. Holes in the substrate are repelled by the gate and absorbed by the source and the drain in the vicinity of the junctions, creating hole-starved regions, which are called depletion region.[1]

regions called the source and drain electrodes, which are separated by p-type semiconductor substrate region. The substrate region is electrically isolated from the gate electrode by gate dielectric which is a thin layer of insulating material such as silicon dioxide and this layer is topped by a metal electrode called the gate. The effective operation of MOSFETs normally relies on efficient electrostatic coupling between the gate induced electric field and semiconductor channel, without allowing electrons to flow between them. Under typical bias conditions, the source and the p-type substrate are grounded, and a positive voltage is applied to the drain electrode. The applied gate-source voltage can control the carrier concentration in the channel region and the drain-source voltage would drive a drain current through the MOSFET. Specifically, the p-type semiconductor substrate is not inverted directly under the oxide layer with applied gate voltage below threshold voltage. So there are no conductive carriers along the channel, then no current flows between the source and the drain electrodes. The transistor is turned off, playing the part of an open switch. If a large enough positive voltage is applied to the gate, then the electron-rich inversion layer is formed under the gate oxide layer. The channel forms a continuous electron bridge between the source and the drain, and the current can flow between these two electrodes. The MOSFET device is then turned on and acts as a closed switch.

1.1.2 Current-Voltage Relationship

In CMOS circuit, the MOSFET is supposed to switch between on and off state.[27] Take n-channel enhancement mode MOSFET as an example, when the device is biased in the on-state regime, the channel has high conductivity and a large on-current (I_{ON}) can flow through the channel region. As per definition, I_{ON} is the MOSFET current when the device is biased at V_{GS}=V_{DS}=V_{DD}. On the other hand, the device channel conductivity is very low, and only a very small off-current I_{OFF} is allowed to flow through it when the MOSFET is biased at V_{GS}=0V and V_{DS}=V_{DD}. The threshold voltage V_{Th} is defined as the gate voltage at which the MOSFET is just at the verge of switching on. Figure 1.2

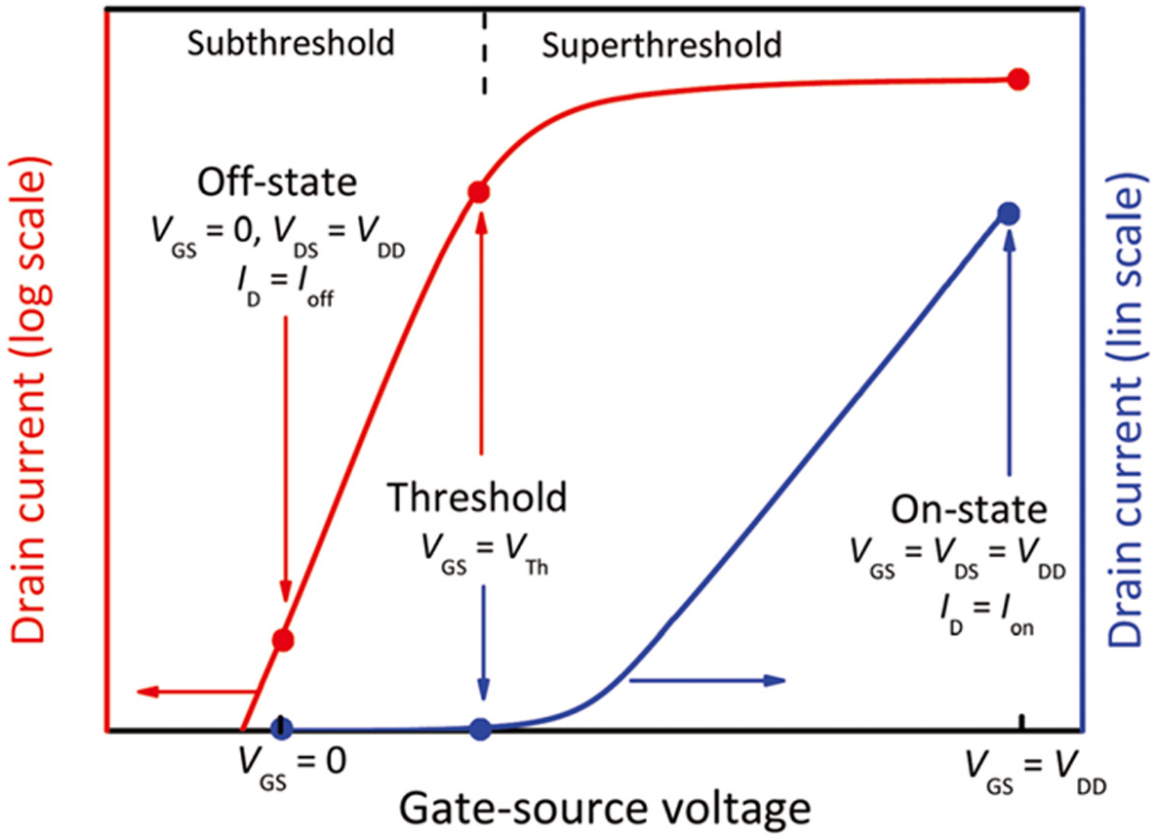

Figure 1.2 Transfer characteristics of an n-channel FET showing the drain current as a function of the gate voltage together with the on and off operating points for CMOS logic. Note that the scale of the left current axis is logarithmic and that of the right current axis is linear.[2]

shows the transfer characteristics of an n-channel enhancement mode MOSFET device.[2] One can see that the device drain current I_{DS} depends exponentially on gate voltage V_{GS} in the subthreshold regime, followed by a transition regime around threshold voltage and finally by the superthreshold regime where the drain current is essentially linearly dependent on gate voltage. In the past few decades, the supply voltage V_{DD} of logic CMOS circuit has been decreased dramatically with continuously miniaturization of MOSFET size and a further reduction is needed for future semiconductor electronics industry. In this regard, a very small gate voltage could switch the logic MOSFET from off- to on-state. Another important factor related to MOSFET switching is the current on-off ratio. For MOSFET used in today's digital logic, on-off ratios in the range of 10^4 to 10^7 are required.[2] The best

scenario is that both on-current and on-off ratio are as high as possible and off-current is as low as possible because a low off-current means low static power consumption in logic circuits while a high on-current is relevant for a high switching speed. Another important parameter related to MOSFET performance is the carrier mobility. High carrier mobility is always beneficial for device switching speed and power efficiency. For today's digital logic circuits, silicon offers only a moderate mobility of up to 1000 $cm^2V^{-1}s^{-1}$.[27] In this regard, extraordinary efforts are needed to implement alternative high-mobility MOSFET channel materials into the silicon transistor or explore new channel material to achieve even higher device performance.

1.1.3 Moore's Law

In 1965, Gordon Moore predicted that the density of transistors on a chip would double every 18 months which is called Moore's law.[28] The Moore's law has been used in the semiconductor electronics industry for more than half a century to guide long-term planning of silicon transistor miniaturization and IC integration. It is clear that reducing the transistor size will increase the transistor density on a single chip, which will increase the chip circuitry functionality. It is worth noting that the Moore's law is not only about the density of transistors that can be achieved, but also the cost per transistor is the lowest. More importantly, the performance of miniaturized MOSFETs would be improved as well. For example, the energy needed for a transistor switching would decrease and the processing speed of semiconductor microprocessor would largely increase. For decades, the silicon based CMOS ICs have integrated exponentially increased number of individual MOSFETs. And, simultaneously, the price per transistor has been dramatically reduced. Key to this fast evolution is the continuous miniaturization of silicon MOSFET size, for short scaling. As can be seen in Figure 1.3, since 2014, a single microprocessor containing 5 billion silicon MOSFETs with gate lengths of around 20 nm has been commercially available.[2]

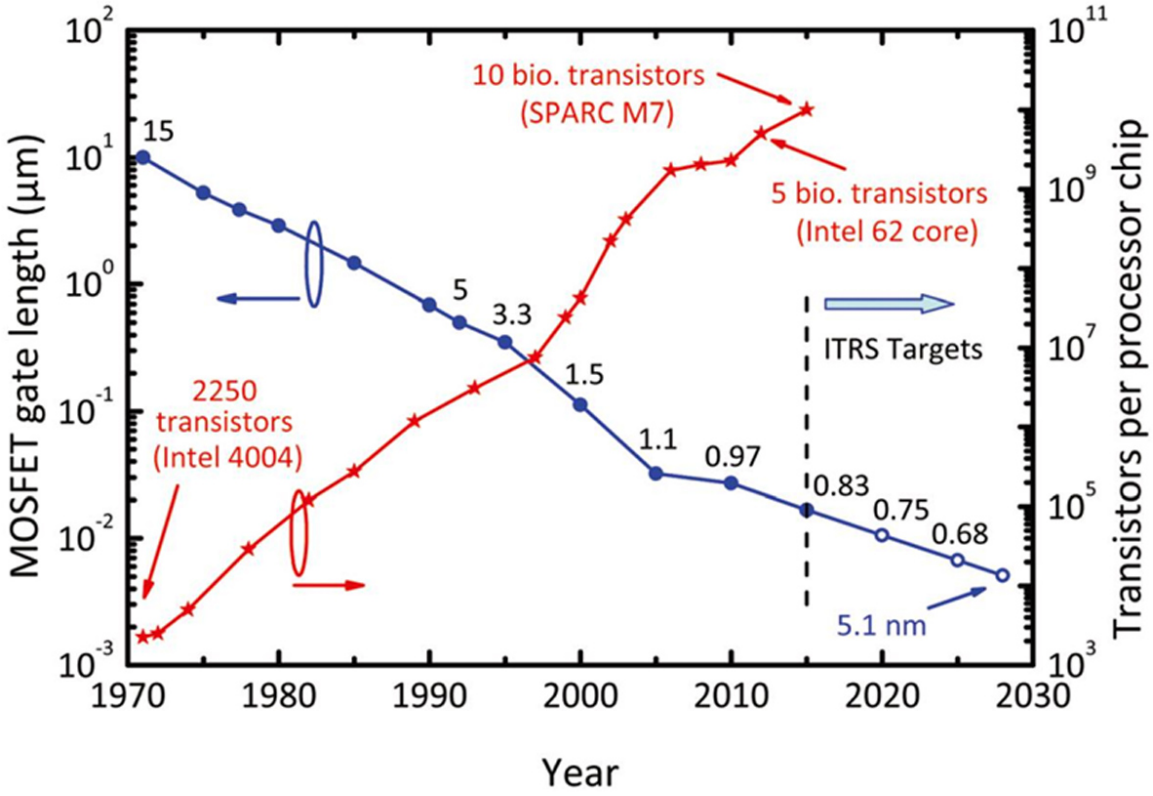

Figure 1.3 Evolution of the silicon MOSFET gate length and the number of transistors integrated on a single microprocessor chip. The numbers above the gate length curve indicate the processor supply voltage. Note the continuous decrease of V_{DD} in the past and the required continuation of this trend in the future. The ITRS targets refer to MOSFETs for high-performance logic as specified in the 2013 ITRS edition.[2]

1.1.4 Short Channel Effects

In recent years, however, it becomes more and more challenging to achieve desired performance improvement in digital ICs with miniaturized silicon MOSFET. These years of conventional scaling are almost over and the improvement in transistor performance due to scaling has researched saturation. This plateau results from the so-called short channel effects, which arise when the transistor channel length becomes very small.[1, 29] MOSFETs with ultrashort channel lengths have begun to experience high off-state currents which mean that some charge carriers are able to flow between the source and the drain electrodes even with gate voltage to suppress the current flow. The presence of an off-state current would increase the static power. As a result, the device miniaturization has been limited by the

rate at which heat, caused by static power, is dissipated. The current leakage and the challenges associated with heat dissipation caused by static power are termed as short channel effects.[3] The short channel effects are detrimental for the silicon MOSFET operation and energy efficiency to the extent that the International Technology Roadmap for Semiconductors (ITRS) predicts that the density of MOSFETs on a single chip would double every 3 years rather than every 2 years.

To address the short channel effects at extreme scaling limits, the thickness of the channel material needs to be less than roughly one-third of the gate length in order to allow the gate to retain its effective electrostatic control of channel carrier concentration.[30, 31] It is clear that one can continue the scaling by reducing the thickness of channel. However, ultrathin body semiconductors (a few atomic layers) made from decreasing 3D bulk materials suffer from dangling bonds, leading to scattering of the charge carriers and severe degradation in device carrier mobility, as shown in Figure 1.4a and b.[3, 4] For transistors made from ultrathin body 3D semiconductors, the substantial decrease in performance is observed due to the dandling bonds, undesirable coupling with phonons and the creation of interface states. This is a great challenge that all post-silicon electronics has to face. In this regard, 2D layered materials are promising candidates to advance future CMOS technology to smaller device size because they are atomically smooth and free of dangling bonds and defect states, as shown in Figure 1.4c and d.[3, 4] In addition, 2D layered materials are compatible with existing CMOS infrastructure. Another important advantage is that 2D layered materials are immunity to short channel effects owing to their small thickness nature. The rise of 2D layered materials began in 2004 with the successful exfoliation of atomically thin 2D graphene film.[9, 10, 32] Particularly, the high carrier mobilities in 2D graphene raised people's expectations that graphene could be the promising channel material for transistors and would become the successor of silicon semiconductors.[6, 33] Over a surprisingly short period of time, many types of new 2D materials such as TMDs and BP have been successfully exfoliated.[16, 34, 35, 19, 36, 37, 38, 22] Unlike zero-bandgap graphene, 2D TMDs and black phosphorus

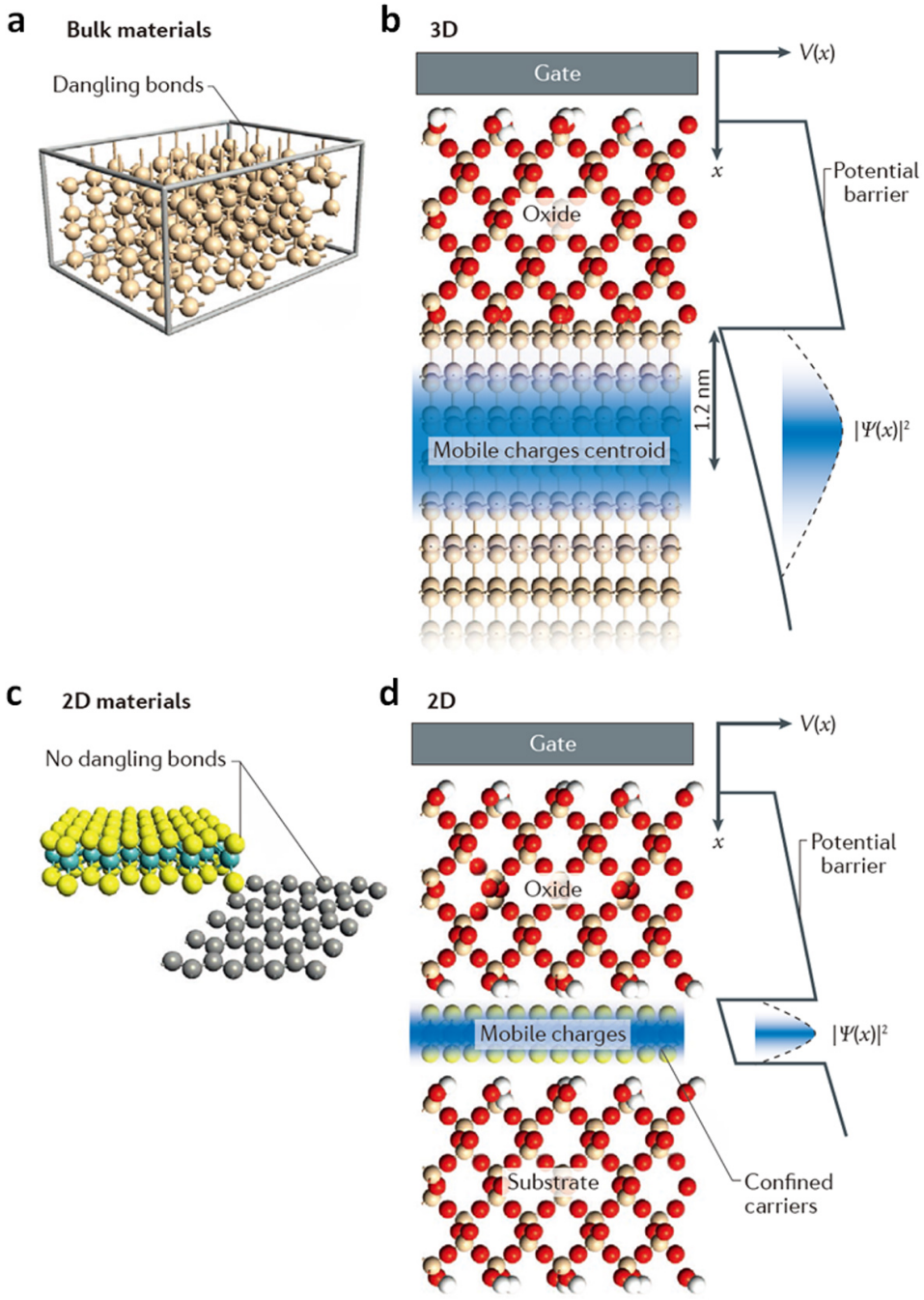

Figure 1.4 Advantages of 2D materials compared with 3D materials for FETs. (a) Ultrathin 3D (bulk) semiconductors have dangling bonds that form traps for electrons and reduce the performance of FETs. (b) Gate electrostatics and mobile charge distribution in 3D semiconductors. (c) By contrast, 2D materials have pristine surfaces. (d) In 2D materials, charge carriers are confined in the atomically thin semiconductor, resulting in a narrower mobile charge distribution. This confinement of charge carriers allows the carriers to be easily controlled by the gate voltage, leading to excellent gate electrostatics.[3, 4]

exhibit a sizable bandgap, making them suitable for logic transistors, memory devices and photodetectors. Moreover, the possibility of large-scale 2D film synthesis by chemical vapor deposition (CVD) shows great promise in wafer-scale device integration.[39, 40, 41, 42, 43]

1.2 Overview of 2D Materials

During the past decade, 2D layered materials have attracted considerable research interest from the electronic and optoelectronic device community. The first 2D material studied in detail was graphene and, since 2007, it has been intensively studied as a channel material for electronic and optoelectronic devices.[44, 45, 46, 47] Inspired by graphene, researchers have intensively explored other 2D layered materials beyond graphene and the number of 2D materials under investigation has literally exploded recently. And recent experiments have successfully demonstrated that a variety of 2D materials do exhibit diverse electronic properties, ranging from insulating hexagonal boron nitride and semiconducting TMDs such as MoS_2 and BP, to semimetallic graphene, as shown in Figure 1.5.[5] In this thesis, we will focus on electronic and optoelectronic device applications of three types of 2D materials and they are graphene, MoS_2 and BP.

1.2.1 Graphene

Graphene is an allotrope of carbon consisting of a flat monolayer of carbon atoms tightly packed into a 2D honeycomb lattice, and is a basic structural element of many other allotropes of carbon, such as graphite, carbon nanotubes and fullerences, as shown in Figure 1.6.[6] One can see that the monolayer 2D carbon atom sheet can be wrapped up into 0D fullerenes, rolled into 1D nanotubes and stacked into 3D graphite. The electronic structure of graphene rapidly evolves with the number of atom layers, and will approach the 3D limit of graphite at 10 layers.

Graphene has a hexagonal lattice structure, with two equivalent sublattices in each unit

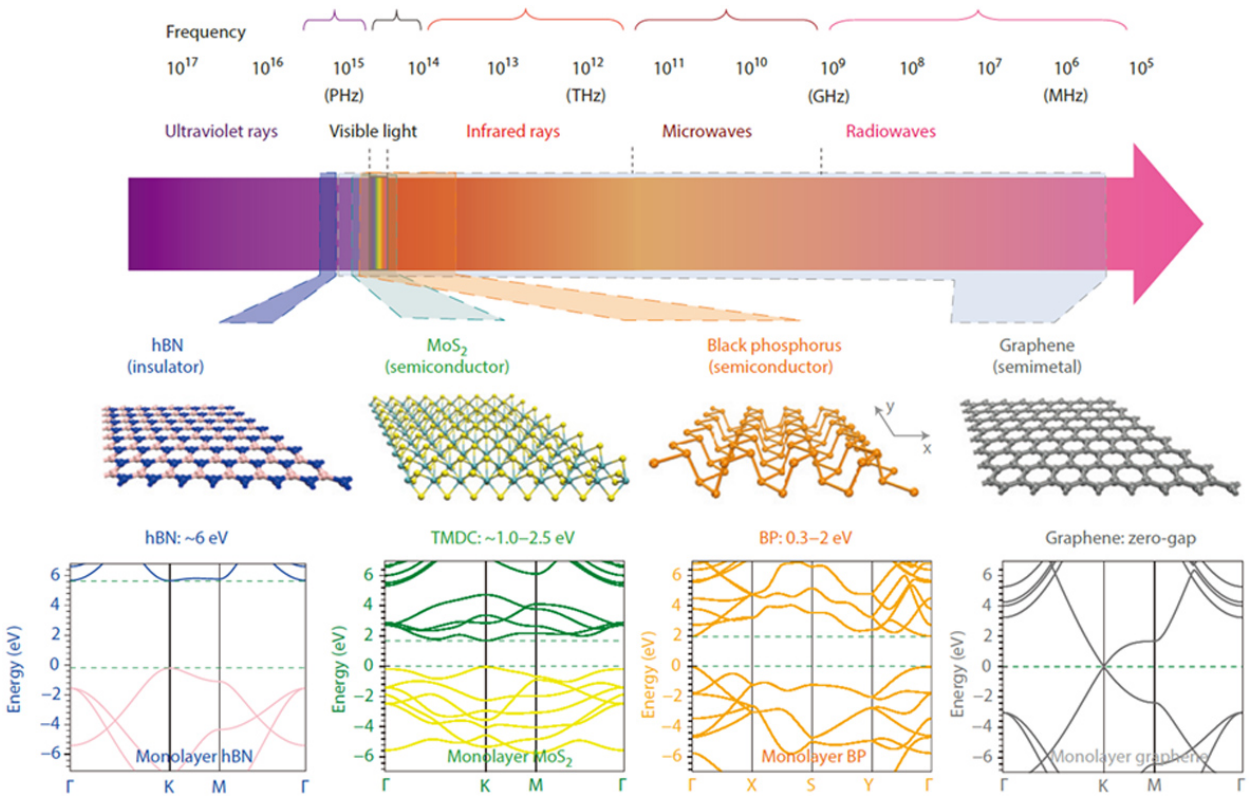

Figure 1.5 2D materials covering a broad spectral range. The atomic structures and band-structures of monolayer hexagonal boron nitride, MoS_2, BP and graphene.[5]

cell, as shown in Figure 1.7.[7, 8] The band structure of graphene is extremely different from that of conventional semiconductors, such as silicon, germanium and gallium arsenide, etc. First, graphene shows zero bandgap nature, with degenerate conduction and valance bands at the six corners of the Brillouin zone. Second, near the graphene zone corners, the energy dispersion relation is almost linear rather than quadratic which resembles ultrarelativistic particles and can be described by the massless Dirac equation. So the electrons in graphene are called massless Dirac fermions and the Brillouin zone corners are called Dirac points. Third, the density of states at the Dirac points is zero, making graphene a semimetallic material with tunable Fermi level.

Monolayer graphene flakes can be obtained by mechanical exfoliation of bulk graphite crystals.[9] The thickness of silicon dioxide plays an important role in observing monolayer graphene in an optical microscope. For example, only a 5% difference in silicon dioxide

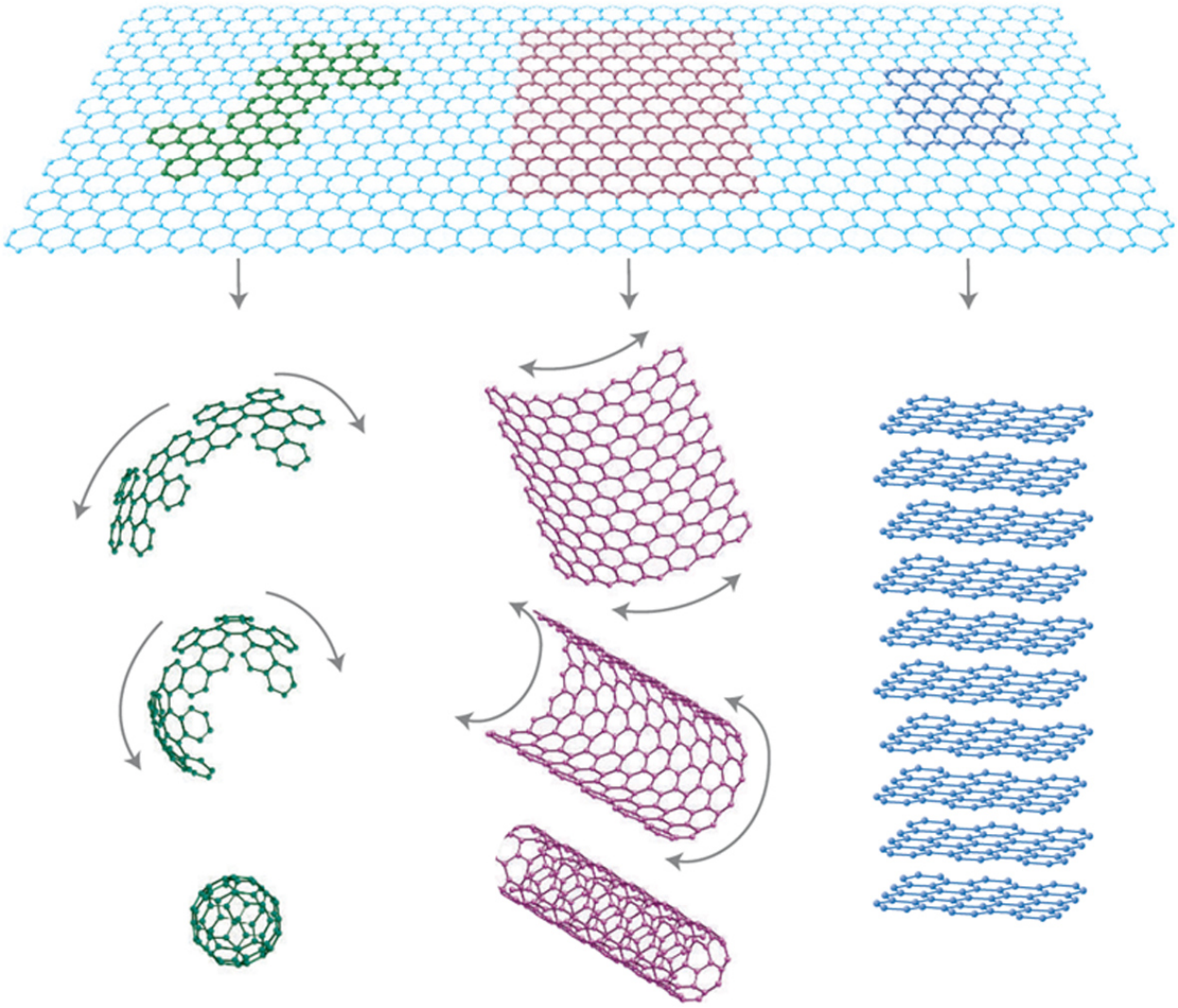

Figure 1.6 Mother of all graphitic forms. Graphene is a 2D building material for carbon materials of all other dimensionalities. It can be wrapped up into 0D buckyballs, rolled into 1D nanotubes or stacked into 3D graphite comparison between printing process and traditional process.[6]

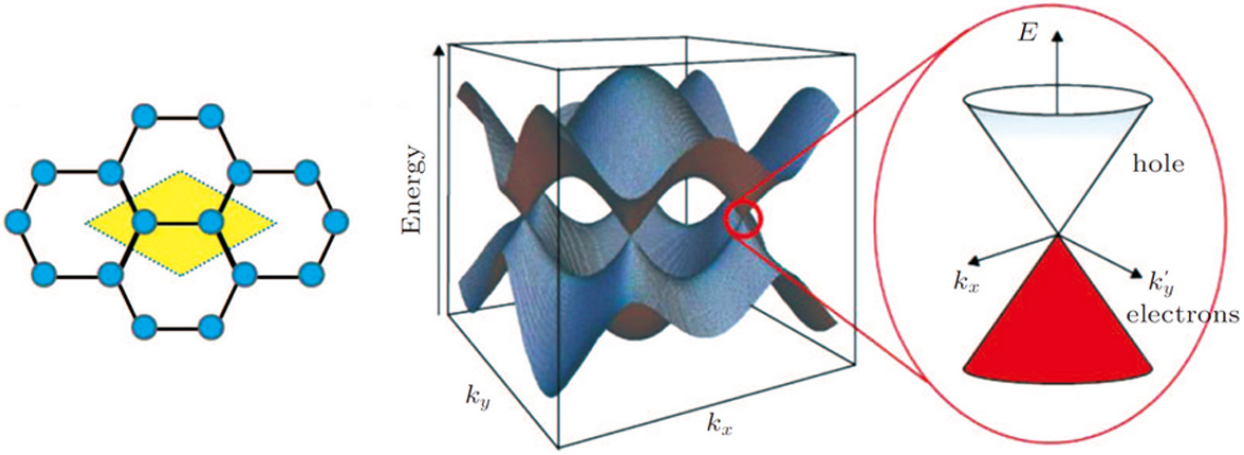

Figure 1.7 The lattice structure of graphene with the yellow region as the unit cell and graphene band structure showing the Dirac cones.[7, 8]

thickness (315 nm instead of current standard of 300 nm) can make monolayer graphene film completely invisible.[10] Figure 1.8a shows the AFM images of a representative graphene flake on silicon wafer.[10] One can see that the folded region showing a relative height of 0.4 nm clearly indicates that it is a single atomic layer. Figure 1.8b presents the graphene film freely suspended on a micrometer-size metallic scaffold.[10] Figure 1.8c exhibits the SEM image of a large-area graphene flake showing that most of crystals faces are zigzag and armchair edges as indicated by blue and red lines and illustrated in the inset.

Graphene based transistors exhibit ambipolar electric field effect which means that carriers in graphene can be tuned continuously between holes and electrons.[9] The device carrier concentration could be as high as 10^{13} cm^{-2} and its room-temperature mobility can exceed 15,000 cm^{2}V^{-1}s^{-1}. The dependence of graphene sheet resistivity on gate voltage shows a sharp peak to a value of several kilohms and decays to around 100 ohms at high gate voltage as shown in Figure 1.8d. The device conductivity increases linearly with gate voltage on both sides of the resistivity peak. One can see that the Hall coefficient R_H shows a sharp reversal of its sign at the same device gate voltage where conductivity has its peak as shown in Figure 1.8e. It extremely resembles the ambipolar electric field effect in semiconductors. A model of 2D metal with a very small overlap between conductance and valence bands can be used

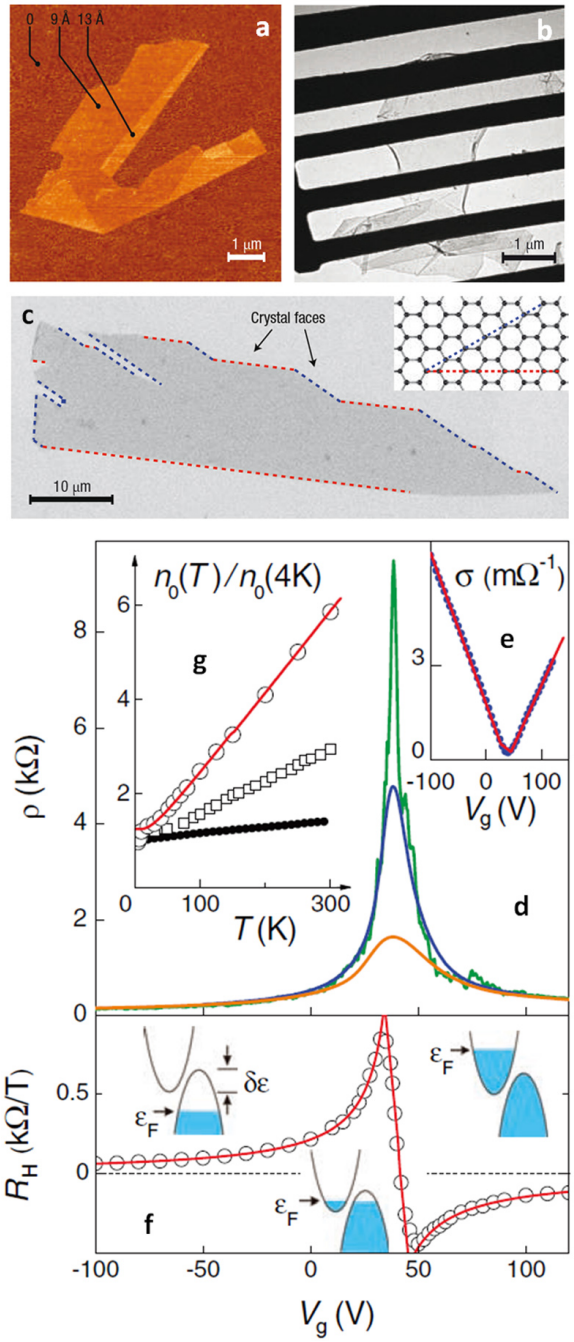

Figure 1.8 Graphene visualized by atomic force microscopy and field effect in few-layer graphene. (a) The folded region exhibiting a relative height of 0.4 nm clearly indicates that it is a single layer. (b) A graphene sheet is freely suspended on a micrometer-size metallic scaffold. (c) Scanning electron micrograph of a relatively large graphene crystal, which shows that most of the crystals faces are zigzag and armchair edges as indicated by the blue and red lines. (d) Typical dependence of FLGs resistivity on gate voltage for different temperatures. (e) Example of changes in the films conductivity obtained by inverting the 70 K curves. (f) Hall coefficient versus gate voltage for the same film (g) Temperature dependence of carrier concentration.[6, 9, 10, 11]

to quantitatively explain the ambipolar electric field effect in graphene. The Fermi level in graphene can also be tuned by gate voltage accordingly. From the formula we can find that the surface charge density of graphene is around 10^{12} cm^{-2} at a gate voltage of 100 V. The device gate voltage has electric field doping effect which can transform the shallow-overlap semimetal into either completely hole or completely electron dominated conductor through a mixed state where both holes and electrons exist. Figure 1.8f shows that the Hall coefficient R_H in graphene device decreases with increasing carrier concentration for the regions with only holes and electrons left. When the graphene device is biased in the mixed state where both holes and electrons present, small change in gate voltage will substitute one type of carrier with another. At the same time, the Hall coefficient will reverse its sign indicating that R_H is proportional to the difference between electron and hole concentrations. Graphene film is typically a hole dominated semimetal material without electric field doping which is attributed to an unintentional doping by absorbed water molecules. The peak in resistivity curve shifts to positive gate voltage and this peak can be shifted to zero gate voltage by annealing in vacuum conditions. Graphene is very attractive in electronics and optoelectronics applications mainly due to its high mobility which varied from sample to sample between 3,000 and 10,000 cm^{2}V^{-1}s^{-1}. The carrier mobility in graphene is independent of absolute temperature indicating that it is limited by scattering on defects. For example, the mean free path in graphene is around 0.4 μm with carrier mobility of 10,000 cm^{2}V^{-1}s^{-1} and concentration of 10^{12} cm^{-2}. It leads to the 2D gas at most a few angstroms away from the interfaces. Although graphene is a promising candidate for electronics applications, the unique electronic structure is actually not ideal for logic device and circuit applications. The zero bandgap nature leads to graphene transistors usually have an on-off ratio lower than 10 at room temperature. In addition, the massless spectrum at the Dirac point makes it difficult to confine electrons in a certain region, as they can easily tunnel through energy barriers by Klein tunneling.

1.2.2 Molybdenum Disulfide (MoS_2)

The successful preparation of monolayer graphene opened up new possibilities and research into other atomically thin 2D materials. TMDs are MX_2-type compounds where M is a transition elements and X represents the chalcogen species.[14] The TMDs can be semiconductors, metals and superconductors. 2D TMDs have strong molecular intralayer bonds but weak interlayer bonds, leading to their layered structure. MoS_2 has been one of the most studied TMDs since 1960s in the fields of dry lubrication,[48, 49] catalysis,[50, 51] photovoltaics [52, 53] and batteries [54, 55]. It is only very recently that monolayer or multilayer MoS_2 film has attracted intensive attention for its potential applications in semiconductor electronics and optoelectronics.[16, 34, 35]

MoS_2 has a 2D layered structure with individual layers stacked upon each other by weak van der Waals forces.[16] This property makes it possible to obtain monolayer or multilayer MoS_2 flakes using the scotch tape mechanical exfoliation. MoS_2 monolayer has a plane of hexagonally arranged molybdenum atoms sandwiched between two planes of hexagonally arranged sulfur atoms, with the covalently bonded S-Mo-S atoms in a trigonal prismatic arrangement forming a hexagonal crystal structure, as shown in Figure 1.9a.[12] MoS_2 has two crystal symmetry configurations which are hexagonal (semiconducting) and octahedral (metallic) structures.[12] The former one is more stable than the latter one. Electronic band structure of ultrathin MoS_2 film with different thicknesses can be calculated using density functional theory with generalized gradient approximation. The calculation results are shown in Figure 1.9b.[15] One can see that the direct excitonic transition energy at the Brillouin zone K point barely changes with layer thickness, but the indirect bandgap increases monotonically as the number of layers decreases. Remarkably, the indirect transition energy becomes so high in monolayer MoS_2 leading to a 2D direct bandgap MoS_2 semiconductor.

Single- and few-layer MoS_2 flakes can be identified by optical contrast in a microscope. Figure 1.10a shows an optical microscope image of a typical ultrathin MoS_2 flake on silicon

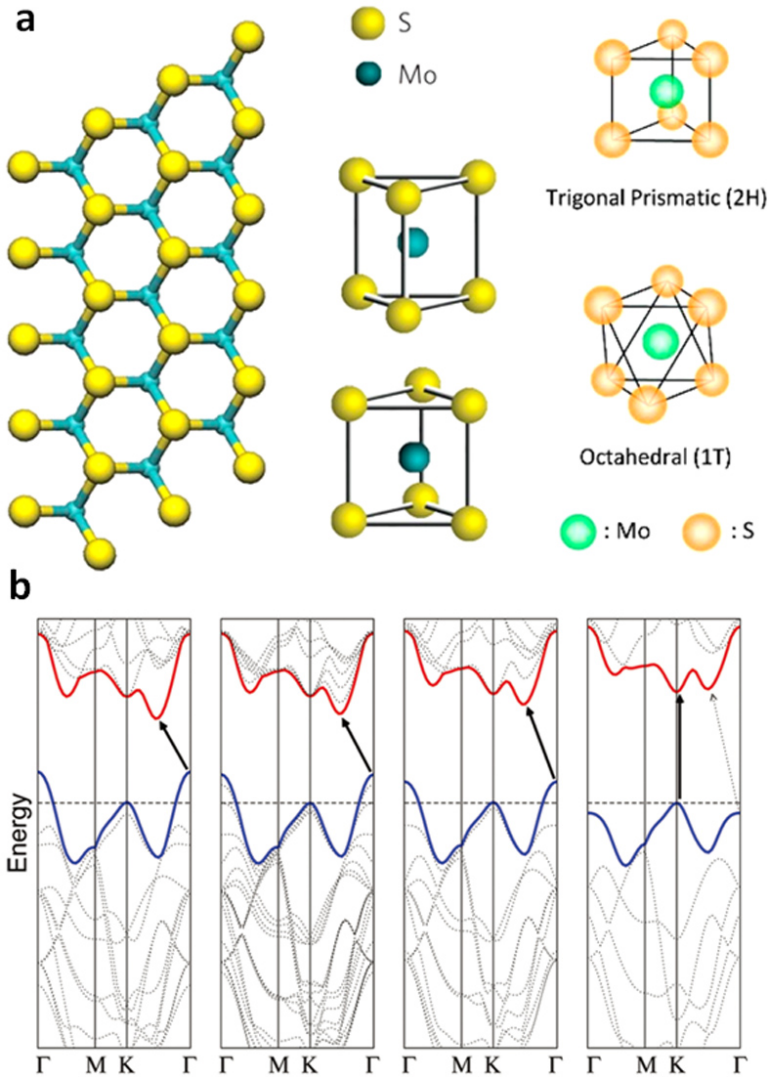

Figure 1.9 Crystal and band structure of MoS_2. (a) Crystal structure of MoS_2. Top view of monolayer hexagonal crystal structure of MoS_2. Trigonal prismatic (2H) and octahedral (1T) unit cell structures. (b) Thickness dependent band structure of MoS_2 flakes.[12, 13, 14, 15]

wafer with 280 nm thermal silicon dioxide.[15] These regions with different shades of blue correspond to MoS_2 layers with different thicknesses. Comparisons between the observed optical contrast and theoretical estimates indicate that region 1L is covered by monolayer of MoS_2. AFM (Figure 1.10b) is used to further confirm the thickness of MoS_2 flakes. The average step height from the substrate to the flake 1L is measured to be around 0.7 nm and agrees well with the single-layer thickness of 0.6 nm for S-Mo-S structures.[15] Optical measurements by PL spectroscopy and Raman scattering are performed on single- and few-layer MoS_2 flakes.[16, 17] All optical measurements are carried out under ambient conditions at room temperature. As an indirect bandgap semiconductor, PL in bulk MoS_2 is a weak phonon-assisted process and is known to have negligible quantum yield. Appreciable PL was, however, observed from few-layer MoS_2 flakes, and surprisingly bright PL was detected from monolayer MoS_2 flake. The PL spectrum of monolayer MoS_2 consists of a single narrow feature of around 50 meV width, centered at 1.9 eV. In contrast, the PL peak of a bilayer MoS_2 sample is strikingly weak, as shown in Figure 1.10c. Raman spectroscopy can be used to examine crystal quality and accurately identify the layer number. Figure 1.10d displays the Raman spectrum of MoS_2 flake with different thicknesses. The A_{1g} is an out-of-plane mode resulting from vibration of only S atoms in opposite directions, while the ${E_{2g}}^1$ mode is attributed to an in-plane opposite vibration of two S atoms with respect the Mo between them. The A_{1g} mode undergoes a blue shift while the ${E_{2g}}^1$ mode undergoes a red shift with increasing MoS_2 film thickness. The ${E_{2g}}^1$ mode is sensitive to the long-range interlayer Coulombic interaction between molybdenum atoms, while A_{1g} mode can be affected by adsorbates on the MoS_2 surface and electron doping. The A_{1g} mode shows a red shift and an increase in the peak width with increasing doping level owing to strong electron-phonon coupling. The frequency or frequency shift difference between these two modes on the Raman spectrum can be used to determine the MoS_2 thickness.

Figure 1.11 shows the schematic, optical microscope image and current-voltage characteristics of a typical monolayer MoS_2 based transistor with top gate.[18] The monolayer MoS_2

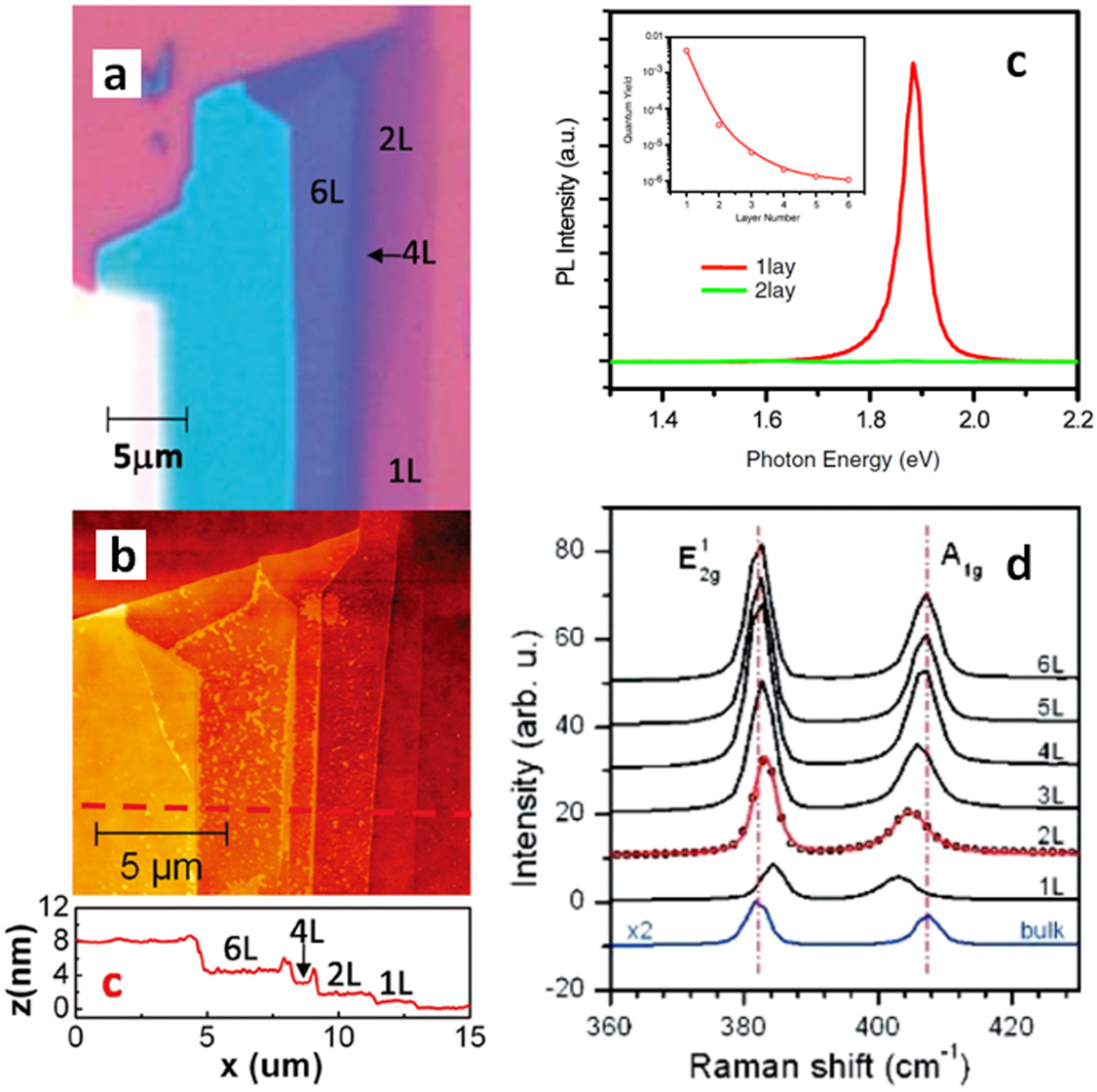

Figure 1.10 Material characterization of layered MoS_2 flakes. (a) Optical microscope image of MoS_2 flake with different thicknesses. (b) The AFM images of MoS_2 flake. PL (c) and Raman (d) spectrum of MoS_2 flake.[16, 15, 17]

flake was mechanically exfoliated using Scotch tape and then transferred onto degenerately doped silicon wafer covered with 270 nm thick silicon dioxide. Electrical contacts were fabricated using EBL followed by deposition of 50 nm thick gold film and lift-off processes. The as-fabricated MoS_2 transistor was then annealed at 200 degrees Celsius to remove the resist residue and reduce the contact resistance. ALD of 30 nm thick HfO_2 as a high-k gate dielectric for the local top gate and mobility booster can realize the full potential of the monolayer MoS_2 semiconductor. As can be seen from transfer characteristics, the device on-resistance of MoS_2 transistor was 27 kilohms for drain voltage of 10 mV and gate voltage of 10 V, with a gate width of 4 um and bottom gate length of 1.5 um. More importantly, the monolayer MoS_2 device shows a room-temperature current on-off ratio up to 10^8, subthreshold swing of around 74 mV/decade and field effect mobility of 217 $cm^2V^{-1}s^{-1}$. Such a transistor built from monolayer MoS_2 film could form the backbone of future electronics in which MoS_2 transistors could be fabricated on insulating boron nitride substrates. Being a thin, transparent semiconductor, MoS_2 is a very promising material candidate for electronics and low-standby-power integrated circuits.

1.2.3 Black Phosphorus

One hundred years after its first successful synthesis in the bulk form in 1914, BP was recently rediscovered as atomically thin 2D layered semiconductor, attracting tremendous research interest from electronics and optoelectronics community.[19, 56] Similar to graphite and TMDs, BP is a layered material in which individual atomic layers are stacked together by van der Waals interactions. Inside a single atomic layer, each phosphorus atom is covalently bonded with three adjacent phosphorus atoms to form a puckered honeycomb structure.[20] The three bonds take up all three phosphorus electrons, so, unlike graphene, BP monolayer is a semiconductor with a predicted direct bandgap of around 2 eV. For multilayer BP, interlayer interactions reduce the bandgap for each layer added, and eventually reach around 0.3 eV for bulk BP. Such a band structure provides a much needed electronic bandgap for

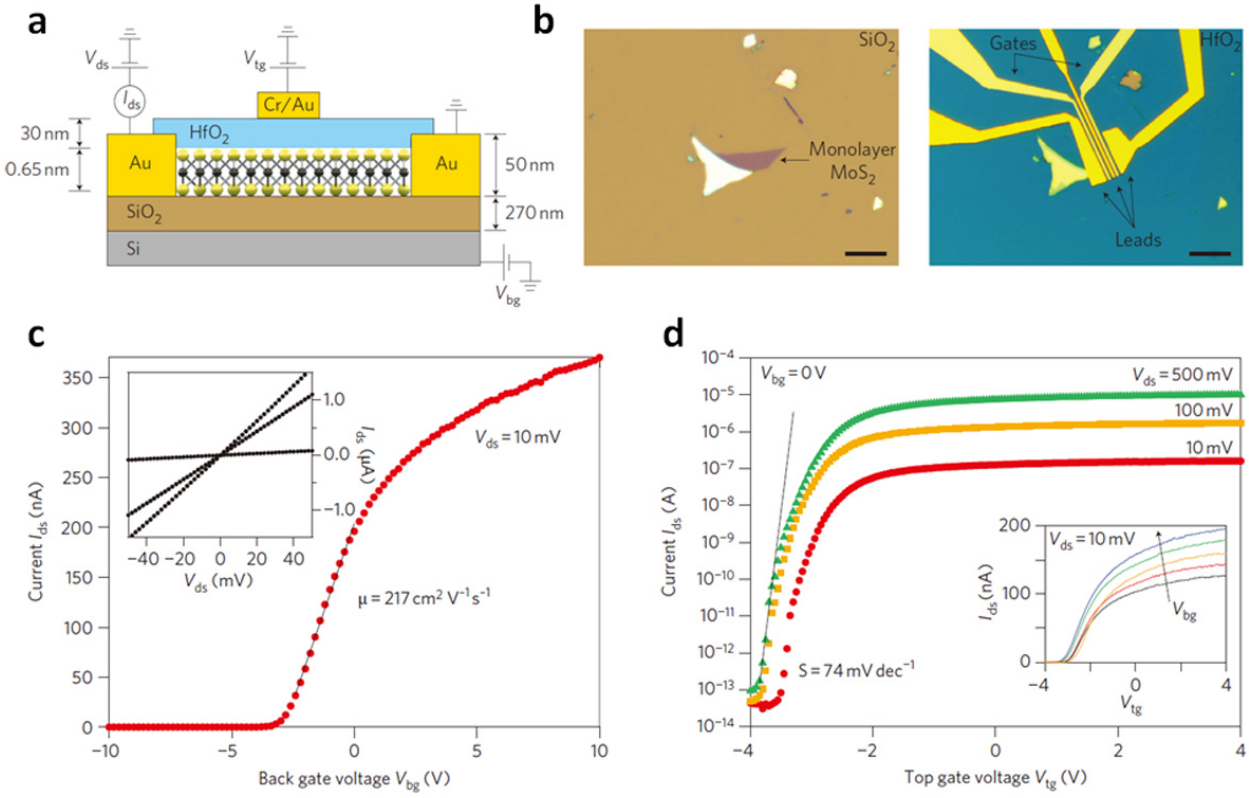

Figure 1.11 Characterization of MoS_2 monolayer transistors. (a) Cross-sectional view of the structure of a monolayer MoS_2 FET together with electrical connections used to characterize the device. (b) Optical microscope images of single-layer MoS_2 based FET. (c) Room-temperature transfer characteristic for FET with 10 mV applied drain voltage. (d) Transfer characteristic of top gated MoS_2 monolayer FET for a bias voltage ranging from 10 mV to 500 mV.[18]

the logic transistor applications of 2D materials and the thickness-dependent direct bandgap nature would lead to potential applications in photonics and optoelectronics, particularly in the infrared regime. BP has three crystalline structures: orthorhombic, simple cubic and rhombohedral. Semiconducting puckered orthorhombic BP is of interest here. For monolayer BP semiconductor, it includes two atomic layers and two kinds of P-P bonds, as shown in Figure 1.12a.[20] The longer bond length of 0.2244 nm connects P atoms between the top and bottom of a single layer and the shorter bond length of 0.2224 nm connects the nearest P atoms in the same plane. The top view of BP along the z direction shows a hexagonal crystalline structure with bond angles of 96.3° and 102.1°, as shown in Figure 1.12b.[20]

Angle-resolved photoemission spectroscopy (ARPES) was used to verify the band structure of the bulk BP crystals. The filled bands of freshly cleaved bulk BP crystals measured by ARPES agree well with screened hybrid functional calculations with no material-dependent empirical parameters (dashed and solid lines for filled and empty bands, respectively),as shown in Figure 1.12c.[19] Figure 1.12d shows the theoretical predication of bandgap in single- and few-layer BP indicating that the bandgap can vary from 0.3 eV in bulk form to above 2.0 eV in its single-layer form.[21]

Figure 1.13a presents a transmission mode optical image of a BP flake on a PDMS film indicating that the light absorbance of BP monolayer is around 2.8%.[23] Figure 1.13b and c show the optical microscope and AFM topographic images of few-layer BP on silicon wafer.[23] The topographic height of BP flake in the black square region is around 1.6 nm corresponding to a thickness of two BP atomic layers. PL of exfoliated monolayer BP flake is observed in the visible wavelengths as shown in Figure 1.13d.[22] For bulk BP flakes, no PL signal is observed within the detection spectrum range because the bandgap of bulk BP is around 0.3 eV, falling in the infrared wave region. In contrast, a pronounced PL signal centered at 1.45 eV with around 100 meV width is observed in a monolayer BP flake. The observed PL peak is likely of excitonic nature and thus a lower bound on the fundamental band gap value. The measured value of 1.45 eV further confirms that the bandgap in monolayer BP crystal is larger than that in bulk BP. The increased bandgap in monolayer BP flake can be attributed to the absence of interlayer hybridization near the top of the valence and bottom of the conduction band. Raman spectrum of the same BP fake with thickness varying from 1.6 nm to 9 nm is presented in Figure 1.13e. The peak at 520.9 cm^{-1} corresponds to the Raman peak of the silicon wafer. And the peaks at 362.5 cm^{-1}, 439.8 cm^{-1} and 467.1 cm^{-1} correspond to the $A_g{}^1$, B_{2g} and $A_g{}^2$ phonon modes observed in bulk BP crystals. The Raman spectroscopy characterization demonstrates that exfoliated BP flakes remain crystalline after mechanical exfoliation. In theory, the B_{2g} and $A_g{}^2$ modes correspond to vibration modes where the atoms oscillate within the intralayer plane, while

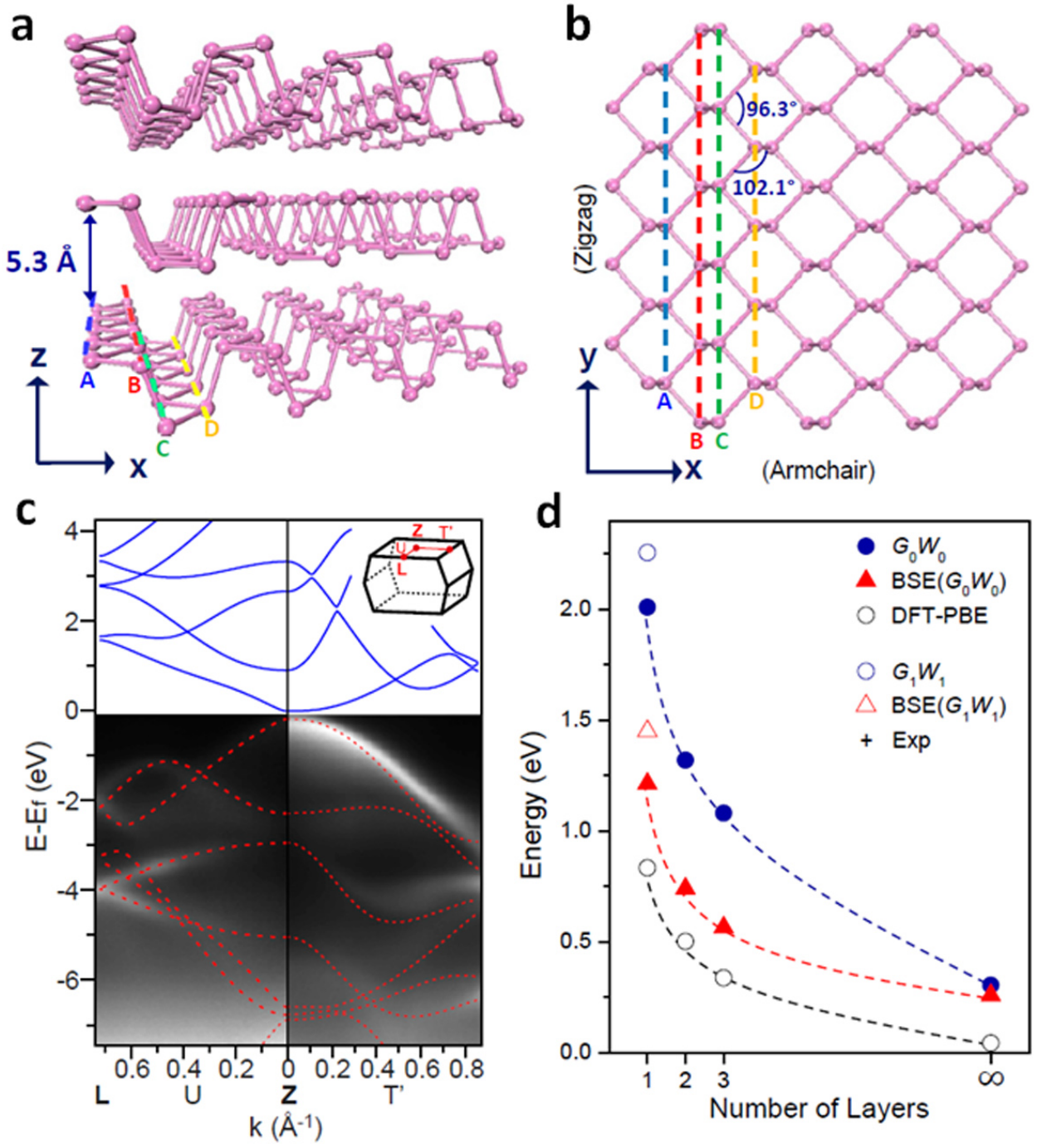

Figure 1.12 Crystal structure and band structure of BP. (a) Side view of the BP crystal lattice. The interlayer spacing is 0.53 nm. (b) Top view of the lattice of monolayer BP. The bond angles are shown. The corresponding x, y, and z directions are indicated in both panels a and b. x and y correspond to the armchair and zigzag directions of BP, respectively. (c) Band structure of bulk BP mapped out by ARPES measurements. A bandgap around 0.3 eV is clearly observed. (d) The evolution of bandgap calculated by different methods, and the energy of the optical absorption peak according to the stacking layer number of few-layer BP.[19, 20, 21]

the $A_g{}^1$ mode corresponds to atoms vibrate out-of-plane.[23]

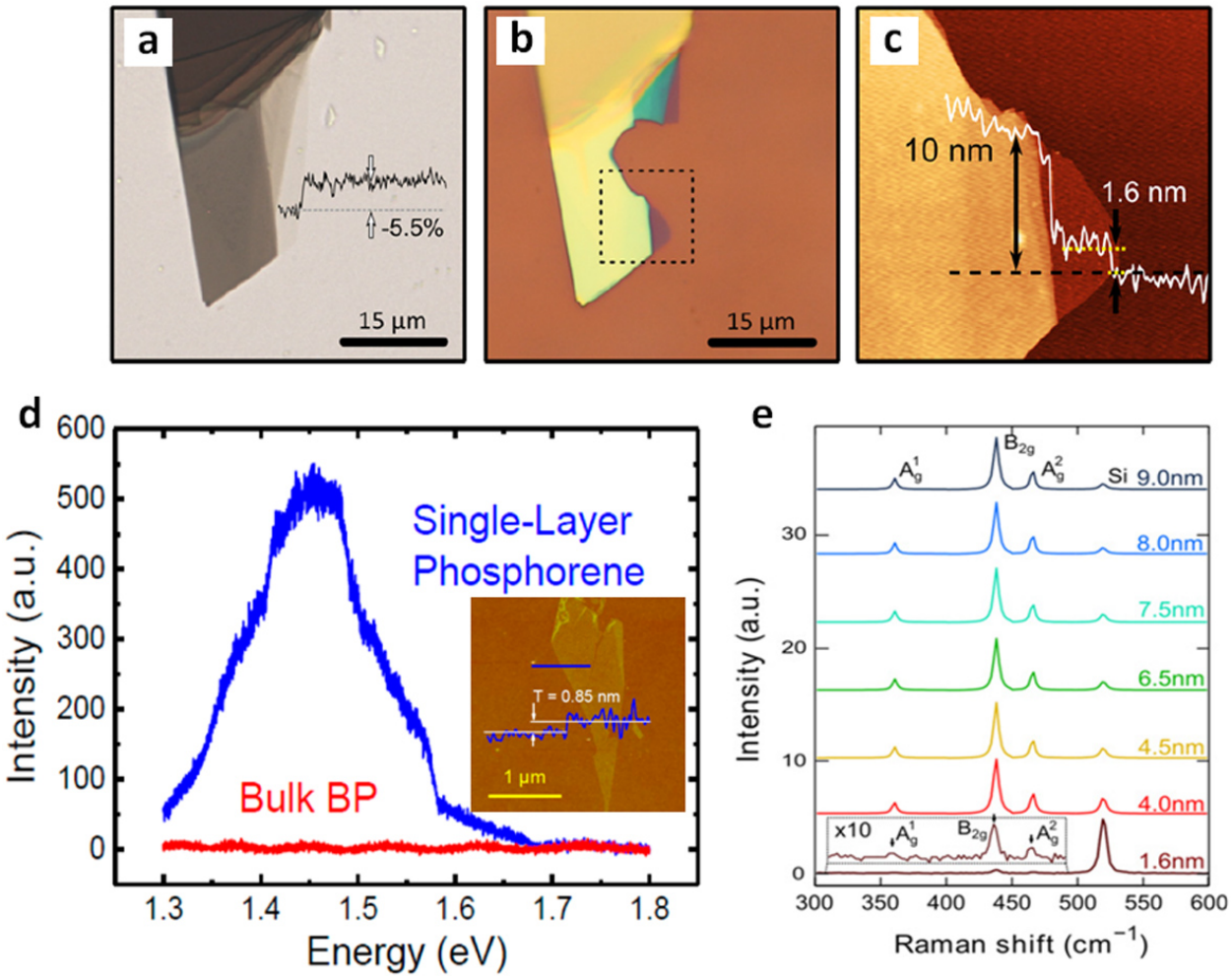

Figure 1.13 Optical characterization of few-layer BP flakes. (a) Transmission mode optical microscopy image of a few-layer BP flake exfoliated onto a PDMS substrate. (b) Bright field optical microscopy image of the same flake after transferring it onto a silicon wafer. Note that part of the flake was broken during the transfer. (c) AFM topography image of the region highlighted with a dashed square in panel b. (d) PL spectra for single-layer phosphorene and bulk BP samples. The inset is the single-layer BP flake. (e) Raman spectrum measured with a 514 nm excitation laser in different zones of a BP flake with thicknesses ranging from 9 nm down to 1.6 nm.[22, 23]

Figure 1.14 shows the electrical performance of few-layer BP based transistor.[19] A scotch tape-based mechanical exfoliation method was used to exfoliate thin flakes from bulk BP crystal onto silicon wafer covered with thermally grown silicon dioxide. Optical microscope and AFM were used to find the BP flakes and determine their thickness. Metal contacts

were then deposited onto BP thin flakes by EBL patterning, electron-beam evaporation of chromium and gold (typically 5 nm and 60 nm, respectively) and lift-off processes. The switching behavior of few-layer BP based transistor at room temperature was characterized in vacuum, in the configuration shown in Figure 1.14b. Here the BP flake is around 5 nm thick and the silicon dioxide thickness is around 90 nm. The BP device switched from the on state to the off state and a drop in drain current by a factor of around 10^5 was observed when the back gate voltage varied from -30 V to 0 V. The measured drain current modulation is four orders of magnitude larger than that in graphene devices. Such a high drain current modulation makes BP thin film a promising material for digital logic applications. More importantly, higher drain current modulation can be achieved by using high-k materials as gate dielectric. For potential applications in digital logic device and circuit, saturation of drain current is crucial to reach maximum possible operation speeds. By carefully choosing the ratio between channel length and silicon dioxide layer thickness, a well-defined current saturation can be achieved in the high drain-source bias region as shown in Figure 1.14c. Meanwhile, the electrical contacts remain ohmic in the linear region at low drain-source bias. Characterization of field effect mobility in few-layer BP devices is presented in Figure 1.14d. A hole mobility as high as 984 $cm^2V^{-1}s^{-1}$ is obtained for BP device with 10 nm thick channel, and is found to be strongly thickness dependent. The carrier mobility is limited by charge impurity scattering at low temperatures and electron-phonon scattering at high temperatures. The ability to fabricate high-performance field-effect transistors, combined with the fact that few-layer BP has a direct bandgap in the infrared regime, makes BP a promising candidate for next-generation nanoelectronic and optoelectronic applications.

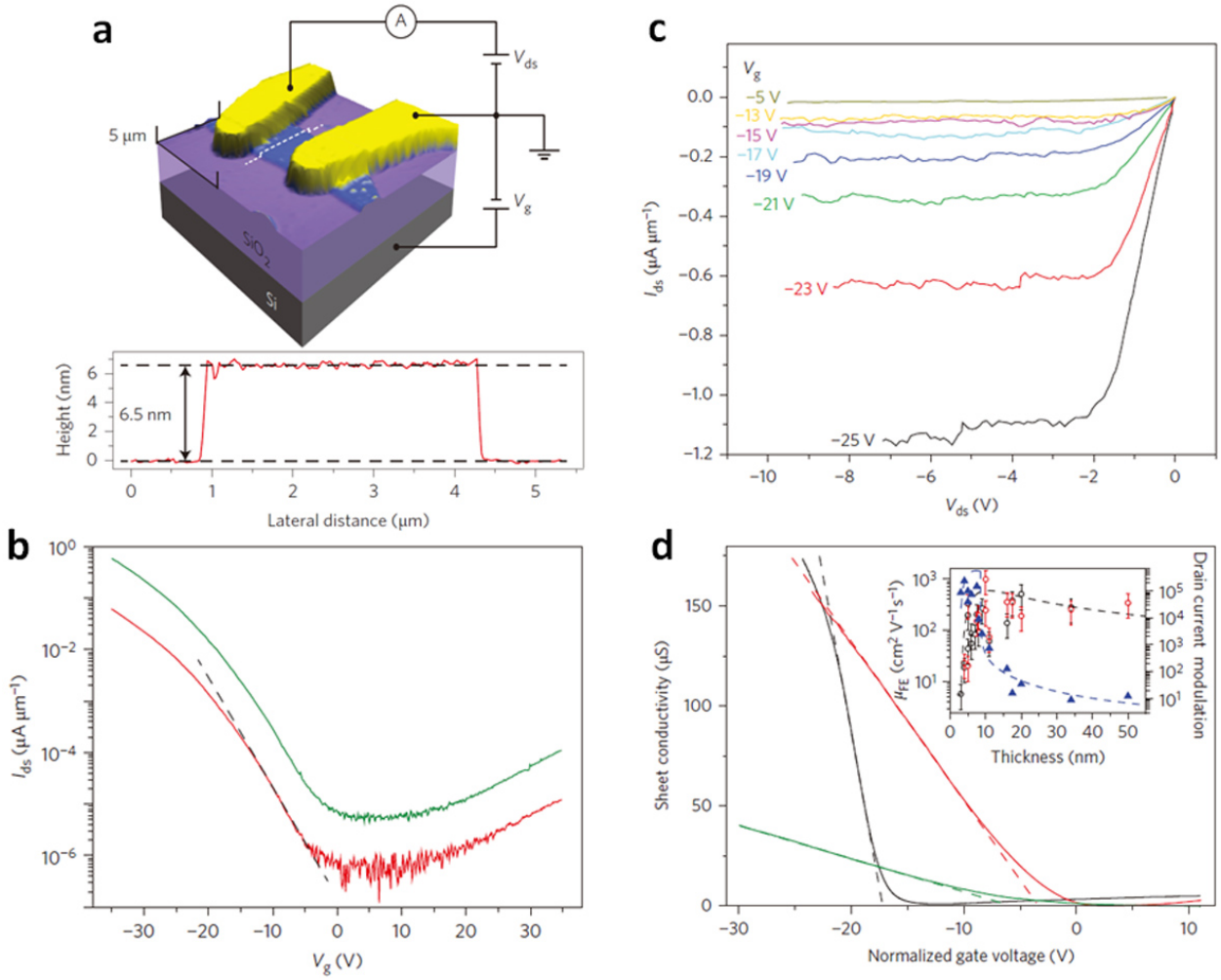

Figure 1.14 Few-layer BP based FET and its device characteristics. (a) Top: Schematic of device structure of a few-layer BP based FET. Bottom: Cross-section of device along the white dashed line in the schematic. (b) Logarithmic scale drain current as a function of gate voltage obtained from a 5-nm-thick device on a silicon wafer with 90 nm silicon dioxide at room temperature, with drain voltages of 10 mV and 100 mV. (c) Drain current as a function of drain voltage at different gate voltages collected from a 5-nm-thick device on a silicon substrate with 90 nm silicon dioxide. (d) Sheet conductivity and field-effect mobility of devices with different thicknesses.[19]

CHAPTER 2

ULTRASHORT CHANNEL BLACK PHOSPHORUS TRANSISTORS AND SCHOTTKY DIODES

In this chapter, we report a novel and facile process combining EBL and angle deposition to fabricate top-gated BP transistors and Schottky diodes with channel length down to 20 nm. With the high quality few-layer BP obtained from mechanical exfoliation, and ultrashort channel length, such devices exhibit respectable on-current and transconductance up to around 174 μA/μm and 70 μS/μm, respectively, at a small drain voltage of 100 mV. Additionally, although certain amount of short channel effects are observed at a channel length of 20 nm, the transistors still manage to retain a decent on-off ratio of more than 10^2, which is expected with the use of ultrathin 2D semiconductor channel material. The results demonstrate the potential of few-layer BP for ultimately scaled transistors. In addition, we have demonstrated BP-based Schottky diodes with current rectifying behavior by using asymmetric metal contacts. Inspired by angle deposition to achieve ultrascaled devices, we studied the channel scaling of BP Schottky diodes and showed that the channel length plays a critical role in determining the output characteristics of the Schottky diodes. If the channel length is aggressively scaled down to around 30 nm, the diode could lose its rectifying characteristics due to increased tunneling current caused by electric field induced Schottky barrier thinning. The results indicate that relatively long channel is preferred if the BP Schottky diode is to be used as high on-off ratio photodetectors. With a built-in potential caused by the metal work function difference in the asymmetrically contacted BP Schottky diode, photodetectors with fast response time of less than 2 ms has been demonstrated.

2.1 Introduction

The rediscovery of layered BP, an allotrope of the element phosphorus with layered structure, has attracted significant attention for nanoelectronics and optoelectronics applications.[19, 57, 58, 59, 60, 61, 62] Unlike semimetallic graphene, BP is a direct bandgap semiconductor with a thickness-dependent bandgap ranging from 0.3 eV (bulk) to 2.0 eV (monolayer).[19] Few-layer BP nanoflakes have been used as channel materials in FET.[19, 63, 64] Such BP FETs exhibit high on-off current ratios of 10^4-10^5 and room temperature field-effect mobility up to 1000 $cm^2V^{-1}s^{-1}$. These desirable properties make 2D layered BP a promising candidate for high-performance electronic and optoelectronic devices, such as radio-frequency transistors,[65] photodetectors,[66, 67, 68, 69, 70] memory devices,[71, 72, 73] and digital inverters.[74, 75] To the best of our knowledge, the smallest BP transistor demonstrated so far has a channel length of approximately 100 nm fabricated by EBL.[59] It gets significantly more challenging to further scale down the channel length to below 100 nm due to the limitations in the EBL process, e-beam resist, and lift-off process used. Here, we report a novel and facile process combining EBL and angle deposition to fabricate top-gated BP transistors and Schottky diodes with channel length down to 20 nm.

2.2 Device Fabrication and Material Characterization

The fabrication process used to obtain the ultrashort channel length BP FETs is illustrated in Figure 2.1a.[76] Briefly, few-layer BP nanoflakes (less than 10 nm) were mechanically exfoliated from bulk BP crystals and transferred onto a silicon wafer with 300-nm-thick silicon dioxide. "Long" channel (L $\approx$1 μm) BP FETs with 50-nm-thick gold (Au) source/drain (S/D) contacts were then fabricated by EBL patterning, metal evaporation, and lift-off processes. A second EBL step was carried out to open a window across the channel region of these "long" channel BP transistors, followed by deposition of 20-nm-thick Au film intentionally evaporated with an angle. With the sample placed at an angle (θ) to the metal

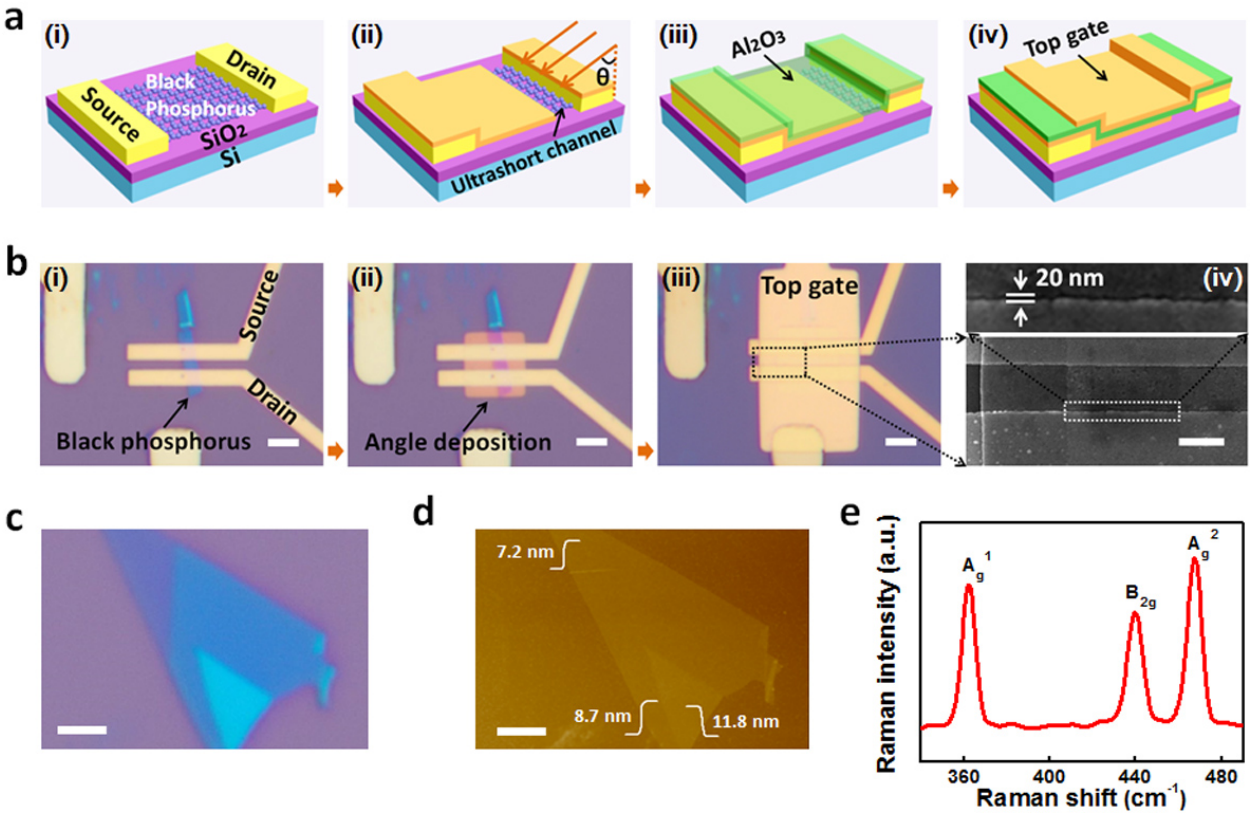

Figure 2.1 BP FET with a channel length of 20 nm fabricated by angle evaporation. (a) Schematic diagrams illustrating the fabrication process of the ultrashort channel length BP FETs. (i) "Long" channel BP FET obtained directly from EBL patterning and lift-off process; (ii) Back-gated ultrashort channel BP FETs obtained from angle evaporation; (iii) ALD of 10-nm-thick Al_2O_3 film as the gate dielectric; (iv) EBL patterning of the top-gate for the ultrashort channel BP FET. (b) Optical microscope and SEM images of a representative ultrashort channel length BP FET at various stages of the fabrication process. Optical micrograph of a "long" channel (L=1 μm) BP FET (i), a sub-20 nm back-gated BP FET obtained after the angle evaporation process (ii), and a sub-20 nm top-gated BP FET (iii). The scale bar for (i) to (iii) is 2 μm. Panel (iv) shows the SEM image of the same device with a 20 nm channel length. (c) Optical image of a representative BP nanoflake used in this study. Scale bar: 2.5 μm. (d) AFM image of the same BP nanoflake. Scale bar: 2.5 μm. (e) Raman spectra of BP nanoflake used in this study.

evaporation direction, the existing 50-nm-thick Au electrodes leave a shadow behind for the second metal deposition, allowing ultra-small gaps (L between 20 to 70 nm) to be obtained in a facile and controllable fashion. Finally, ALD was used to deposit a 10-nm-thick Al_2O_3 layer as the gate dielectric, followed by a third EBL patterning, metal evaporation, and lift-off process to obtain the top gate electrode. Figure 2.1b shows the optical and SEM images of a representative top-gated sub-20 nm BP FET at various stages of the fabrication process. An ultrashort channel length of around 20 nm is evident from the SEM image. BP nanoflakes used in this study typically have thickness below 10 nm and the representative optical micrograph and AFM image are shown in Figure 2.1c and d, respectively. Figure 2.1e shows the Raman spectra obtained from the BP flake, in which three peaks can be observed at 362, 439, and 467 cm^{-1}, corresponding to the $A_g{}^1$, B_{2g} and $A_g{}^2$ phonon modes for pristine BP materials.[38, 77]

2.3 Electrical Performance

The electrical characteristics of top-gated BP FETs with various channel lengths are presented in Figure 2.2. Figure 2.2a illustrates that the device channel length can be effectively controlled by varying the evaporation angle. The measured channel lengths from SEM (red open circle) agree well with the calculated values (blue dashed line) using the equation $L = t \times \tan(\theta)$, where L, t and θ correspond to channel length, first electrode thickness (50 nm in this work), and evaporation angle, respectively. For ultrashort channel FETs, the gate oxide layer needs to be thin enough to allow effective electrostatic control of the channel carrier concentration by the gate electrode.[78] If the gate is not sufficiently strong, then the drain fights with the gate over the channel control, resulting in poor gate dependence. As shown in Figure 2.3, the transfer characteristics (I_{DS}-V_{GS}) of a back-gated BP FET with L = 20 nm measured at a drain-to-source voltage of 1 mV indicates that the back-gate bias cannot fully deplete the channel due to the 300-nm-thick SiO_2 dielectric layer used. In this regard,

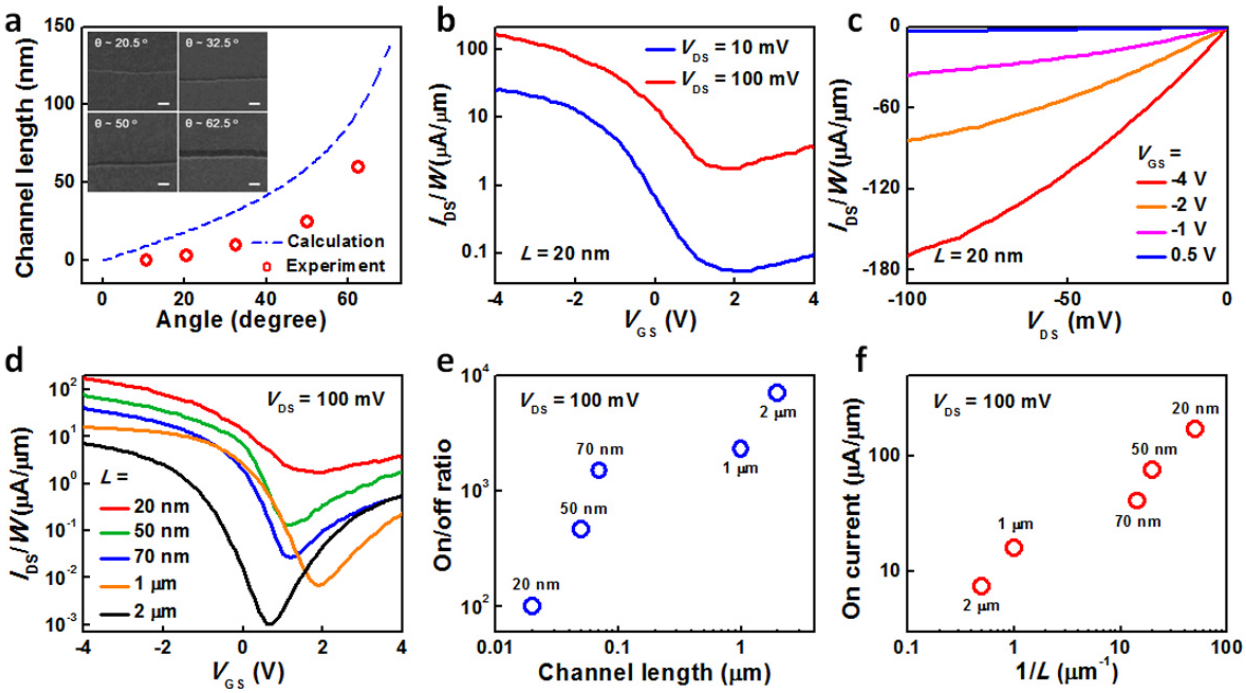

Figure 2.2 Electrical characteristics of ultrashort channel BP FETs. (a) Device channel length as a function of angle used during the metal deposition. Inset: SEM images of various channel lengths obtained. Scale bar: 50 nm. (b) Transfer characteristics (I_{DS}-V_{GS}) of a top-gated BP FET with a channel length of 20 nm. (c) Output characteristics (I_{DS}-V_{DS}) of the same device in (b). (d) Comparison of transfer curves for top-gated BP FETs with various channel lengths. (e) Device on-off current ratio plotted as a function of channel length. (f) Device on-current density plotted as a function of 1/L.

top gate with ultrathin dielectric layer is needed for effective gate control. Figure 2.2b shows the transfer characteristics of a top-gated 20-nm long BP FET with 10 nm Al_2O_3 gate dielectric measured at V_{DS} = 10 and 100 mV. The device exhibits a respectable on-current of around 174 μA/μm and decent on-off ratio of 10^2 with V_{DS} = 100 mV. The current increases as the top gate voltage sweeping from positive to negative, indicating the p-type transistor behavior. Output characteristics of the same device with various top-gate biases (-4, -2, -1, and 0.5 V) are shown in Figure 2.2c. At small V_{DS} values, the drain current varies linearly with the drain voltage, indicating the Schottky barrier is low and thin enough to allow Ohmic-contact-like bahavior between the Au metal and BP. More details about the Schottky barrier and contact resistance will be discussed later.

To assess the performance of the sub-20 nm top-gated BP FETs fabricated using our angle evaporation approach, the relevant figures-of-merit for recently reported BP based FETs are summarized and compared. Owing to the adoption of the smallest channel length (20 nm), our devices exhibit the highest on-state current to date at a small source drain bias of 100 mV. Slightly higher on-current values of 200 or 350 μA/μm have been reported, albeit at a much higher drain bias of 2 V.[65, 37]

To study the channel length scaling of BP FETs, the transfer characteristics of five BP FETs with channel lengths of 0.02, 0.05, 0.07, 1, and 2 μm measured at V_{DS} = 100 mV are presented in Figure 2.2d. The device on-off current ratio and unit-width normalized on-current (I_{DS}/W) are extracted from Figure 2.2d and plotted as functions of channel length as shown in Figure 2.2e and f, respectively. As the channel length aggressively scales from 2 μm to 20 nm, the average on-off current ratio decreases from 10^4 to 10^2, which can be attributed to the drain induced barrier lowering (DIBL) and thermal-assisted tunnelling process.[59] When the device channel length is extremely small, the drain bias will affect the energy barrier at the source side. As a result, the source barrier is now controlled simultaneously by both gate and drain voltages for ultrashort channel length devices, making such devices more difficult to turn off. The extent of the short channel effects depends on the thickness of the semiconductor body relative to the channel length. The channel length of 20 nm is already approaching the thickness of the BP nanoflakes used in this work (around 10 nm). With such BP transistors exhibiting an on-off ratio of 10^2 at an extremely small channel length of 20 nm, we consider the short channel effects to be relatively small and acceptable. In the future, the use of thinner or even monolayer BP nanoflakes could lead to ultrashort channel length transistors with even better immunity to short channel effects.

As for the on-current, it is approximately inversely proportional to the channel length as shown in Figure 2.2f, which agrees well with the classical FET theory. It is worth noting that compared with the "long" channel devices (L = 1 and 2 μm), the on-current for "short" channel devices (L = 20, 50, and 70 nm) is slightly below the predicated values from the

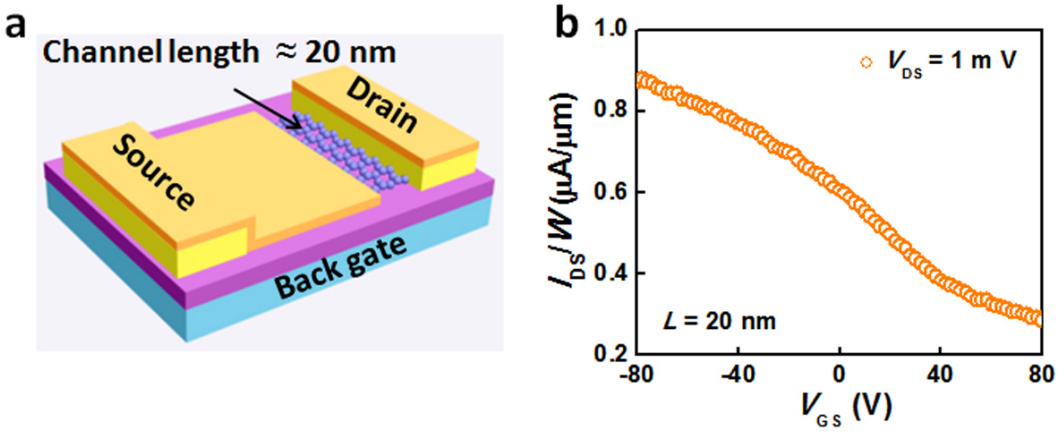

Figure 2.3 Schematic and transfer characteristics of a back-gated BP FET with a channel length of 20 nm measured at $V_{DS} = 1$ mV.

linear extrapolation of the "long" channel data points. The reason is that the "long" channel devices were fabricated with a single step EBL patterning with relatively thick (50 nm) Au S/D electrodes, while the "short" channel devices fabricated from angle evaporation had thinner (20 nm) S/D electrodes. The smaller S/D contact thickness leads to larger S/D series resistance, whose effect may not be significant for "long" channel devices, but could be dominant when the channel length becomes extremely small. Another possible mechanism that could lead to the slightly lower than predicted on-state current for ultrashort devices is the exposure of BP in ambient conditions, which is known to cause performance degradation in BP FETs.[57] We did our best to avoid the BP degradation during the fabrication from affecting the device performance by always passivating the sample with Poly (methyl methacrylate) (PMMA) between the fabrication steps and storing the samples in an argon-filled glovebox when not in use. Nevertheless, the ultrashort channel devices did go through one more step of EBL patterning, metal deposition, and lift-off process before the Al_2O_3 capping compared with the "long" channel devices, which could contribute to momentary exposure in ambient conditions and thereby slightly degraded performance.

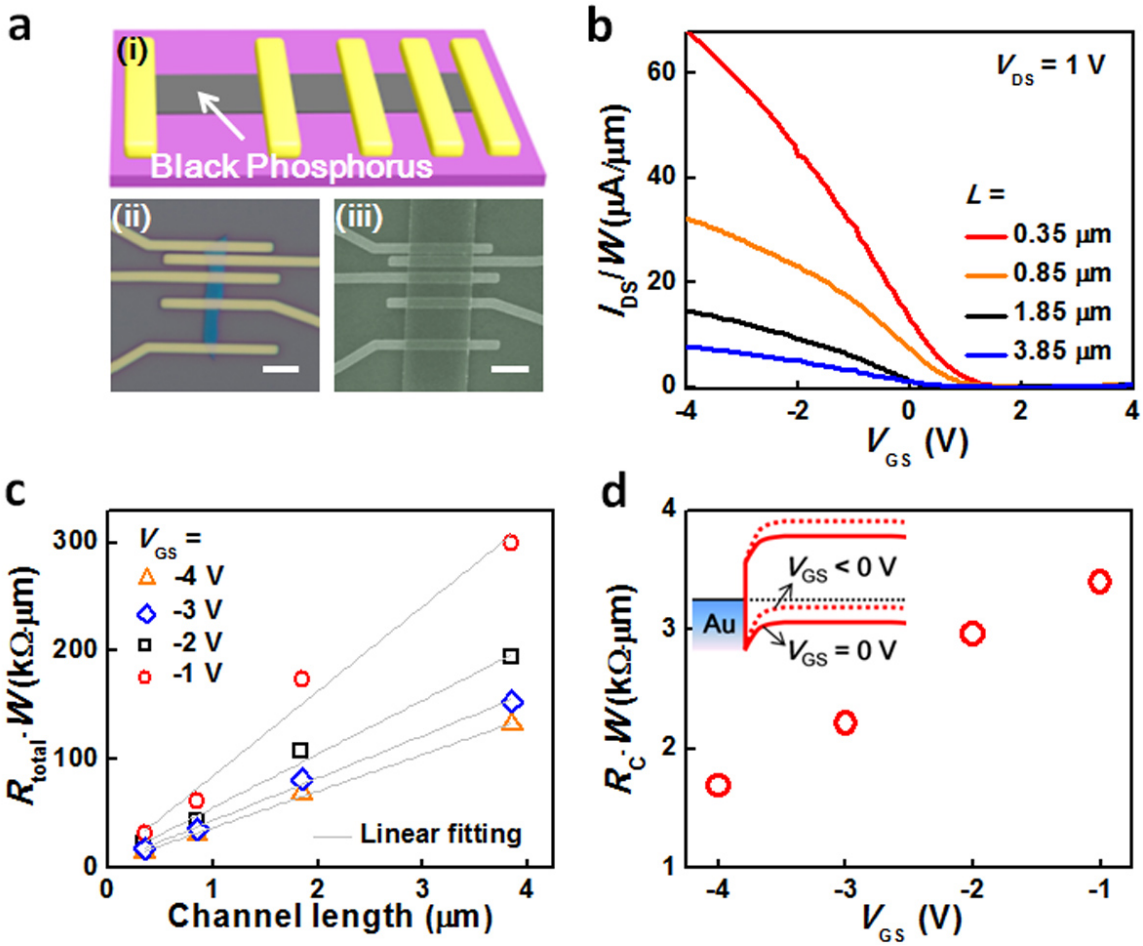

Figure 2.4 TLM method for extracting the contact resistance of BP FETs. (a) Schematic diagram (i), optical micrograph (ii), and SEM image (iii) showing the TLM structure with top-gated BP FETs of various channel lengths (0.35, 0.85, 1.85, and 3.85 μm) fabricated on the same BP nanoflake. A 10-nm-thick Al_2O_3 layer is used as the top-gate dielectric in panel iii. Scale bar: 4 μm. (b) Transfer characteristics of the top-gated BP FETs in the TLM structure measured at $V_{DS} = 1$ V. (c) Normalized total resistance (R_{total}) as a function of channel length for various gate biases. (d) Extracted contact resistance (R_c) as a function of top-gated voltage. Inset: Energy band diagram of the Au/BP contact.

2.4 Device Contact Resistance

Contact resistance (R_c) plays an important role in transistor performance particularly for those with ultrashort channel lengths.[79] Understanding the metal/BP contact is of great scientific and technological importance. The R_c can be extracted using the transfer length method (TLM) for BP FETs with long channel lengths.[80] In this case, the channel length is much larger than the carrier mean free path and the channel can be considered as entirely diffusive. A typical back- and top-gated BP FET array is presented in Figure 2.4, showing four transistors fabricated on the same BP nanoflake used for TLM measurements. Figure 2.4b shows the transfer characteristics measured at V_{DS} = 1 V for devices with various channel lengths (0.35, 0.85, 1.85, and 3.85 μm). The maximum on-current occurs at a top-gate voltage of -4 V. Figure 2.4c presents the normalized on-state total resistance (R_{total}), which includes both the channel resistance and R_c, plotted as a function of channel length. The decrease of R_{total} with more negative gate bias is simply due to the increase of carrier concentration in BP FETs. The S/D contact resistance ($2\times R_c$) can be extracted from the y-axis intercepts of the linear fitting. The extracted R_c is then plotted as a function of top-gate voltage in Figure 2.4d. The R_c exhibits clear gate dependence and decreases monotonically as the top gate voltage decreases from -1 to -4 V. This relationship can be explained using the energy band diagram of the metal/p-type BP junction presented as the inset of Figure 2.4d. A more negative gate bias would result in a narrower Schottky barrier between the Au metal and p-type BP interface, which would facilitate the hole injection from the metal into the valence band of BP, resulting in smaller R_c.

2.5 Extrinsic and Intrinsic Field-Effect Mobility

For the long channel devices whose L is much larger than carrier mean-free path, the devices operate entirely in diffusive regime and the contribution from the R_c is much smaller compared with the channel resistance. As a result, the R_c will have little effect on the ex-

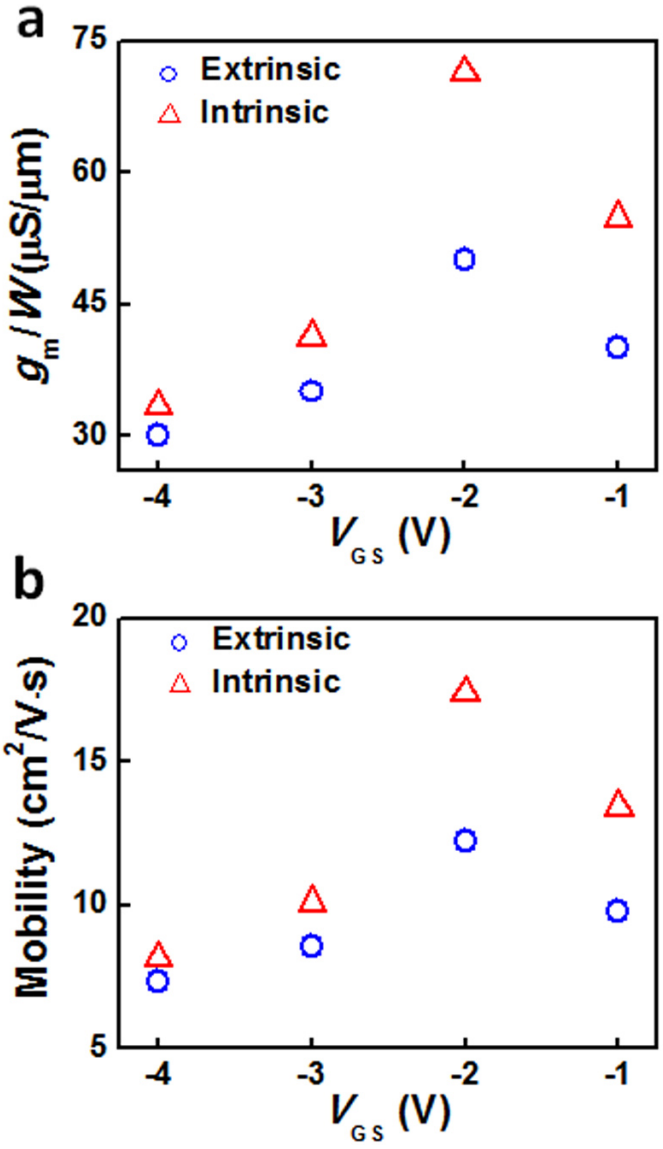

Figure 2.5 Extrinsic and intrinsic transconductance and field-effect mobility of the ultrashort channel BP FET. (a) Device transconductance (normalized to the width of the BP nanoflake) at various gate biases measured at a V_{DS} of 100 mV. (b) Extrinsic and intrinsic field-effect mobility at various gate voltages.

tracted field-effect mobility. Nevertheless, for ultrashort channel devices, contribution from R_c becomes dominant and needs to be taken into consideration for precise evaluation of the intrinsic field-effect mobility. In order to do so, the extrinsic transconductance values (blue open circles in Figure 2.5a) are first extracted by differentiating the transfer curves (V_{DS} = 100 mV) presented in Figure 2.2b. The peak extrinsic transconductance of 50 μS/μm occurs at V_{GS} = - 2 V. The intrinsic transconductance (g_{mi}) of the devices can be deduced by excluding the effect of R_c using the equation $g_{mi} = g_m/(1\text{-}2g_mR_c)$. Using the above equation, the peak intrinsic transconductance is found to be 70 μS/μm at V_{GS} = - 2 V as shown in Figure 2.5a (red open triangles). Both extrinsic and intrinsic field-effect mobilities can then be calculated using the equation $\mu = L\times(g_m/W)/\ (C_{ox}\times V_{DS})$, where C_{ox} is the unit-area capacitance of the 10 nm Al_2O_3 gate dielectric. Using extrinsic (intrinsic) g_m values for the equation would lead to extrinsic (intrinsic) mobility accordingly. For our top-gated BP FETs with 20 nm channel length, the peak extrinsic and intrinsic field-effect mobilities were extracted to be 10 and 14 $cm^2V^{-1}s^{-1}$, respectively, as shown in Figure 2.5b. It is worth noting that although mobility values of greater than 100 $cm^2V^{-1}s^{-1}$ have been reported for BP FETs in some other reports, those devices are either long channel or back-gated devices. It is widely known that top-gating causes increased surface scattering due to the addition of top gate dielectric layer and short channel length leads to carrier velocity saturation, both of which would result in reduced mobility. The mobility values of our top-gated ultrashort channel (L = 20 nm) BP FETs are comparable or slightly higher than the previously reported back-gated 100-nm-channel-length BP FETs whose intrinsic mobility is around 10 $cm^2V^{-1}s^{-1}$.[59] Additionally, for our top-gated long channel devices (L = 1 or 2 μm) presented in Figure 2.2, the intrinsic mobility values are extracted to be 57.3 and 50.8 $cm^2V^{-1}s^{-1}$, respectively.

2.6 Stability Study of Black Phosphorus Transistors

Pristine BP nanoflakes are known to be chemically unstable upon exposure to ambient conditions because the ambient adsorbates such as moisture irreversibly convert BP into PO_x compounds, fundamentally altering its electronic and material properties.[19, 57] Figure 2.6 provides the optical micrographs and AFM image showing the degradation of an unencapsulated BP nanoflake on silicon wafer when stored in ambient conditions. As time goes by, bubbles began to appear on the BP surface (AFM image) and the majority part of the BP flake disappeared after around 4 days. Similar behavior was observed in back-gated BP FETs as shown in Figure 2.6b. Specifically, Figure 2.6b panels i, ii, iii, and iv correspond to the optical micrographs of an as-fabricated back-gated BP FETs after being stored in ambient conditions for 0, 1, 2, and 3 days, respectively. Previous reports have shown that BP can be effectively protected from ambient degradation by appropriately chosen passivation layers. Similar to previous reports, we have found that the Al_2O_3 gate dielectric deposited by ALD serves as an effective passivation layer. As an example, Figure 2.6c shows the optical micrograph and AFM image of a BP nanoflake passivated by 10-nm-thick Al_2O_3 right after exfoliation. Compared with Figure 2.6a and b, no obvious degradation was observed on the encapsulated BP nanoflake after being stored for 7 days in ambient conditions. Figure 2.6d and e further compare the effect of Al_2O_3 passivating on the electrical characteristics of BP FETs. After fabrication and initial measurement, a back-gated BP FET (L = 2 μm) was exposed in ambient conditions. Within 64 hours of exposure, the device on-current fell drastically from 10 μA/μm to 0.2 nA/μm at a V_{DS} of 0.2 V, indicating severe degradation in BP. In contrast, for the top-gated ultrashort channel (L = 50 nm) BP FET, with the passivation from the 10-nm-thick Al_2O_3 gate dielectric layer, no noticeable change was observed in the transfer characteristics even after the device was stored under identical ambient conditions for more than 1 week (174 hours).

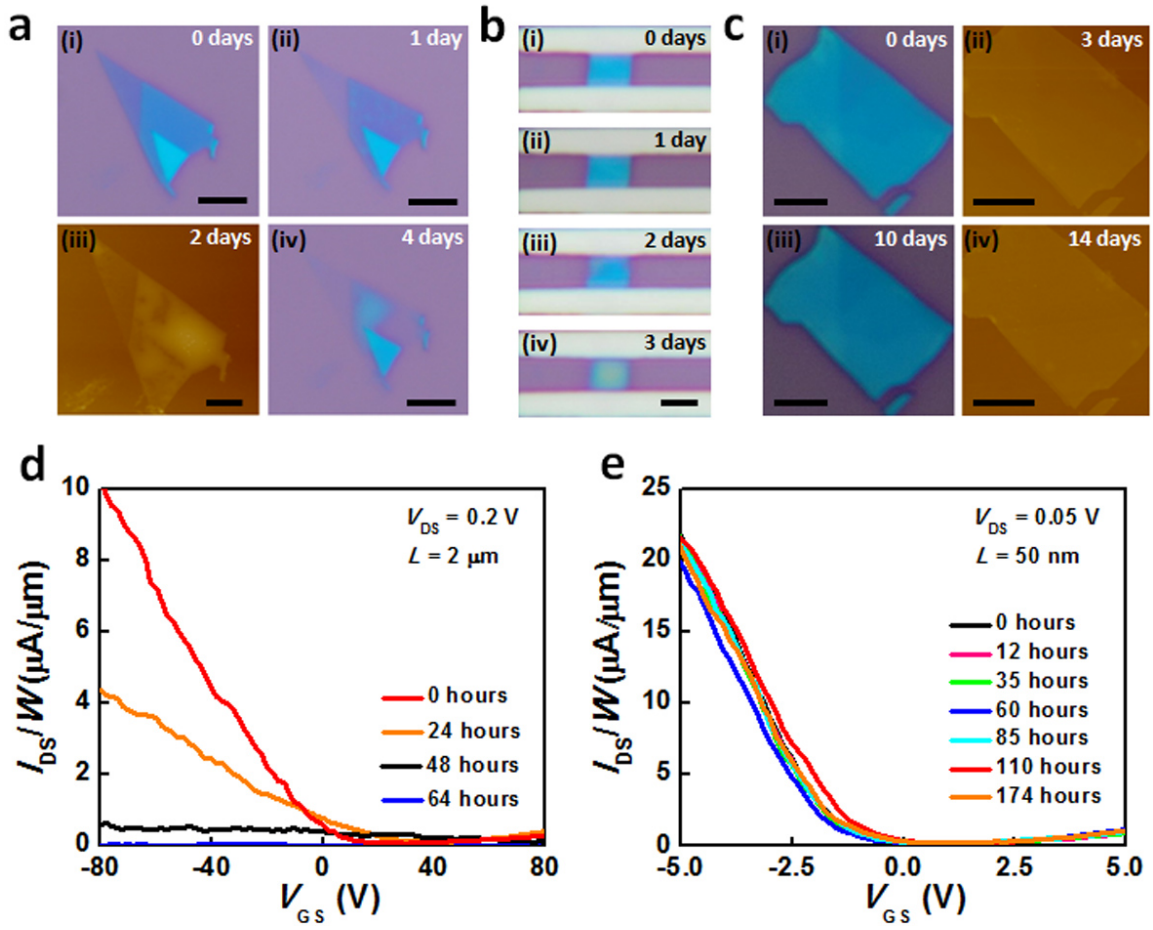

Figure 2.6 Air-stability of back-gated and top-gated BP FETs. (a) Optical micrographs and AFM image of an unencapsulated BP nanoflake right after exfoliation (i) and after being stored in ambient conditions for 1 (ii), 2 (iii), and 4 (iv) days, showing obvious degradation. Scale bar for panels i, ii, and iv: 4 μm. Scale bar for panel iii: 3 μm. (b) Optical micrographs of an unencapsulated back-gated BP FET right after fabrication (i) and after being stored in ambient conditions for 1 (ii), 2 (iii), and 3 (iv) days, showing similar degradation. Scale bar: 2 μm. (c) Optical micrograph and AFM images of a representative BP nanoflake passivated with 10 nm of Al_2O_3 after 7 days in ambient conditions. The scale bars are 3 μm for panel i and 2 μm for panel ii. (d) Transfer characteristics of an unencapsulated back-gated BP FET measured after being exposed to ambient conditions for various amount of time. (e) Transfer characteristics of an ultrashort (L = 50 nm) top-gated BP FET with 10-nm-thick Al_2O_3 gate dielectric measured after being exposed to ambient conditions for various amount of time.

2.7 Black Phosphorus Schottky Diodes

Metal-semiconductor junction plays a very important role in electronic devices and understanding metal-BP contact is of great scientific and technological importance. The electronic performance of BP devices is largely determined by the Schottky barrier at the metal-BP interface resulting from the difference between the metal work function and the Fermi level of BP.[59] It has been extensively studied and well understood from the early work on carbon nanotubes that metals with large work functions would form Ohmic contacts with p-type semiconductors, while metals with low work functions would form Schottky junctions with p-type semiconductors.[79, 81, 82, 83, 84] Therefore, in order to achieve high-performance BP transistors, recent reports employed high work function metals such as palladium (Pd) or gold (Au), as the S/D electrodes.[37, 59] In this section, we investigate the electronic properties of BP devices with asymmetric metal contacts one high work function Au contact and one low work function aluminum (Al) contact. In such device configuration, the metal work function difference between the two electrodes results in a built-in potential, leading to BP Schottky diodes with rectifying characteristics. Using the angle evaporation technique reported in the last section, the channel length of the BP Schottky diode was further scaled down aggressively to around 30 nm, allowing us to study the effect of channel length scaling on the properties of BP Schottky diodes with asymmetric metal contacts. The results indicate that the BP Schottky diode transitions from rectifying to non-rectifying characteristics at extremely small channel lengths due to drain-induced barrier thinning. With the built-in electric field for efficient separation of photogenerated electron-hole pairs, the use of the BP Schottky diode as a photodetector was also demonstrated.

To fabricate 2D BP Schottky diodes with asymmetric metal contacts, Au (work function $\approx$ 5.1 eV) and Al (work function $\approx$ 4.1 eV) metals are chosen as the S/D electrodes. Few-layer BP flakes (thickness $\approx$ 10 nm) were mechanically exfoliated onto a heavily doped silicon substrate with 300-nm-thick SiO_2 dielectric layer. A 50-nm-thick Au electrode was

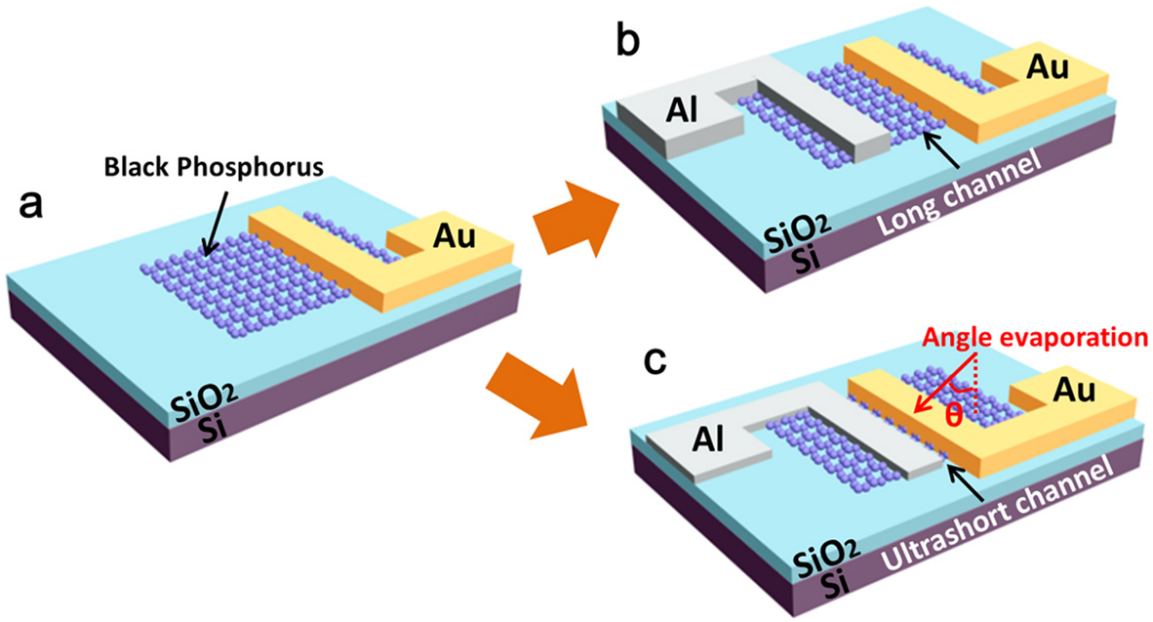

Figure 2.7 Schematics illustrating the fabrication processes of BP Schottky diodes with asymmetric metal contacts. (a) Mechanically exfoliated BP nanoflake contacted by one Au electrode patterned by EBL. (b) Patterning of a second Al electrode using EBL, resulting in the long channel length (1 μm) BP Schottky diodes with asymmetric contacts. (c) Ultrashort channel length (30 nm) BP Schottky diode can be obtained by patterning a window across the BP and Au electrode using EBL, followed by Al evaporation intentionally performed from an angle.

then patterned by EBL, metal evaporation, and lift-off processes as shown in Figure 2.7. To obtain long channel length (L $\approx$ 1 μm) BP Schottky diodes, a second step of EBL was used to pattern Al metal contact (Al/Au 15 nm/35 nm) over the same BP flake (Figure 2.7b). Similarly, ultrashort channel length (L $\approx$ 30 nm) BP Schottky diodes with asymmetric metal contacts can also be obtained using the angle evaporation process reported in our previous work. As illustrated in Figure 2.7a and c, after the patterning and deposition of a 70-nm-thick Au electrode, a second EBL step was used to open a window in the resist layer over both the BP nanoflake and the existing Au electrode, followed by deposition of Al/Au (15 nm/15 nm) metal intentionally evaporated from an angle. Because of the directional nature of the metal evaporation process, placing the sample at an angle (θ) from the evaporation direction would lead to shadowing from the existing 70-nm-thick Au electrode, allowing ultrashort

gaps (L $\approx$ 30 nm) between the S/D electrodes to be achieved. Both device configurations (long channel and ultrashort channel) were used in this work to study the effect of channel length scaling on the characteristics of BP Schottky diodes.

The electrical characteristics of long channel BP Schottky diodes with asymmetric metal contacts are presented in Figure 2.8. The carrier transport in BP transistors is mostly determined by the Schottky barrier at the BP-metal junction, which arises from the differences between the work function of metal and the Fermi level of BP. Metals with a high work function such as Au (5.1 eV) or Pd (5.4 eV) would form Ohmic-like contacts with BP, while metals with a low work function such Al (4.1 eV) would result in a significant Schottky barrier for holes at the BP-metal interface. Figure 2.8a shows the optical microscope image of a BP transistor with four metal contacts, allowing three different types of device configurations (Au-BP-Au, Au-BP-Al, and Al-BP-Al) to be measured on the same BP flake. The transfer characteristics of the three device configurations measured at V_{DS} = -1 V are presented in Figure 2.8b. The device with both Al metal contacts exhibits the lowest current, which is expected due to the existence of Schottky barrier that limits the carrier injection. The device with both Au metal contacts exhibits the highest current due to significantly smaller Schottky barrier height and the device with asymmetric metal contacts (Au-BP-Al) exhibits intermediate on-state current compared to the other two types of devices.

More information can be obtained from the output characteristics of the three types of device configurations. For the device with asymmetric metal contacts, the semi-logarithmic output curves measured at various back-gate voltages (Figure 2.8c) show clear rectifying behavior, which is caused by the built-in potential barrier formed by the work function difference between Au and Al. As the gate voltage varies from -20 to -80 V, the current rectification ratio ($I_{forward}/I_{reverse}$) decreases from 1.5 $\times$ 10^3 to 1.8 $\times$ 10^2, due to the increase in reverse current. The increase in reverse current can be explained by the thinning of Schottky barrier at more negative gate biases, leading to increased reverse tunneling current. The rectifying behavior in BP Schottky diode with asymmetric metal contacts is more evident

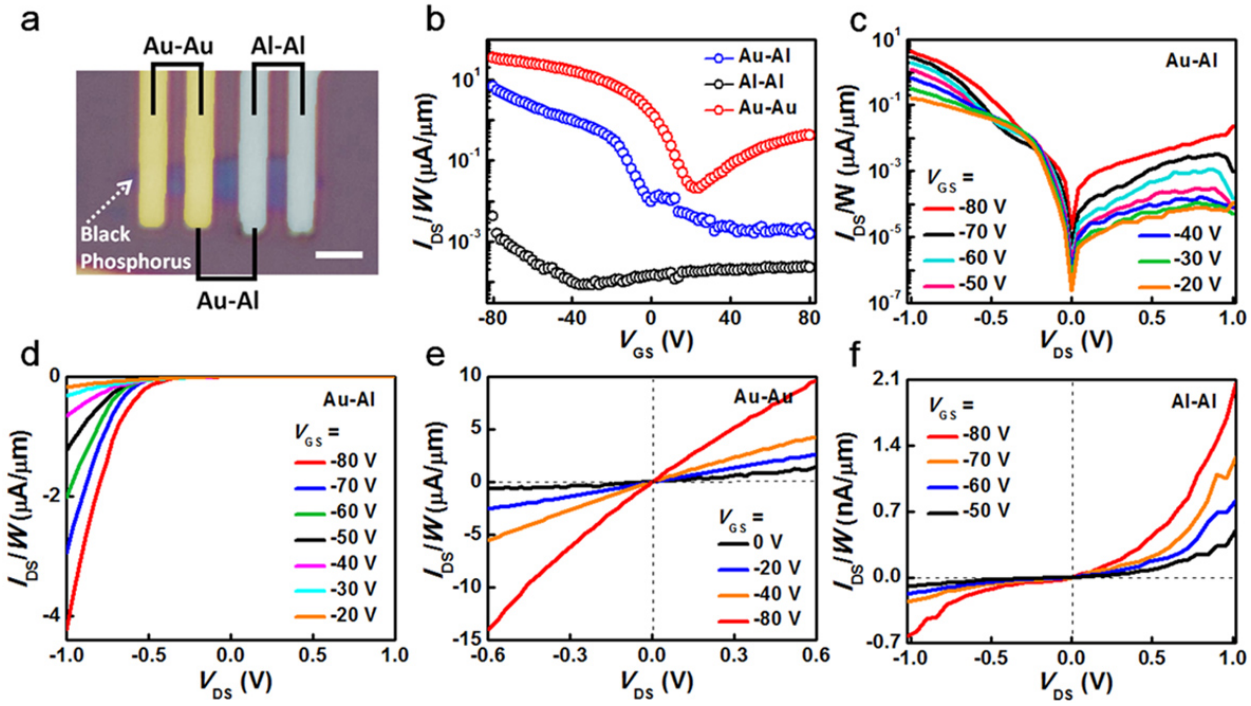

Figure 2.8 Electrical characteristics of long channel BP Schottky diodes with asymmetric metal contacts. (a) Optical micrograph showing the long channel BP transistor with different pairs of S/D electrodes. Scale bar: 2 μm. (b) Comparison of the transfer characteristics from the same BP nanoflake measured between different pairs of S/D electrodes. (c) Semi-logarithmic scale output characteristics of the BP transistor contacted by one Au electrode and one Al electrode. (d-e) Linear scale output characteristics of BP transistors contacted by (d) one Au electrode and one Al electrode, (e) two Au electrodes, and (f) two Al electrodes.

from the linear scale output characteristics shown in Figure 2.8d. In comparison, for the devices with both Au metal contacts (Figure 2.8e), the output curve is approximately linear, demonstrating the formation of Ohmic-like contacts between Au and BP. As for the device with both Al metal contacts (Figure 2.8f), extremely low current and very nonlinear output characteristics indicates the existence of significant Schottky barrier between BP and Al.

Thermionic emission (TE) and tunneling are the two mechanisms governing the carrier transport through the Schottky barrier in Schottky diodes.[85, 86] TE current dominates when the Schottky barrier is thick, resulting in rectifying behavior in Schottky diodes. On the other hand, when the Schottky barrier becomes extremely thin due to the existence of strong electric field, tunneling current would dominate the transport through the barrier,

leading to non-rectifying behavior.[87] The above-described phenomenon becomes evident as the channel length of the BP Schottky diode is aggressively scaled down to sub-100 nm. In order to study the effect of channel length scaling on BP Schottky diodes with asymmetric metal diodes, angle evaporation technique used in our previous publication was used to achieve ultrashort channel length of around 30 nm. The optical microscope and SEM images in Figure 2.9 illustrates the detailed fabrication process, where a 70-nm-thick Au electrode was first patterned on the BP flake, followed by a second EBL step to define a second electrode with Al metal intentionally evaporated from an angle, forming an ultrashort channel of around 30 nm.

Figure 2.9b and c compares the characteristics of the long channel (L = 1 μm) and ultrashort channel (L = 30 nm) BP Schottky diodes measured at a gate voltage of 0 V. The long channel BP Schottky diode exhibits rectifying behavior with a rectification ratio of 1.05 $\times$ 10^2 (blue circle in Figure 2.9b and c). However, as the channel length scales down to 30 nm, the device output characteristics become nonrectifying with a rectification ratio of merely 1.37 (red circle in Figure 2.9b and c). The loss of rectifying behavior in BP Schottky diodes at extremely small channel length can be explained using the energy band diagram in Figure 2.9d. When the channel length is long, the Schottky barrier is thick at the BP-Al junction under reverse bias. The TE mechanism dominates the carrier transport across the barrier and the large Schottky barrier height limits the reverse current flow. On the other hand, for ultrashort channel length of around 30 nm, the close proximity between the source and drain electrodes leads to very strong electric field, resulting in the so-called drain-induced barrier narrowing (DIBN) (blue dash line in Figure 2.9d).[87] In such scenario of a thinned Schottky barrier, the tunneling current significantly increases, leading to increased reverse current and non-rectifying output characteristics.

Few-layer BP flake has a thickness-dependent direct bandgap varying from 0.3 eV (bulk) to 2.0 eV (monolayer), making it a promising material candidate for photodetection from visible to infrared part of the spectrum. The BP Schottky diodes with asymmetric metal

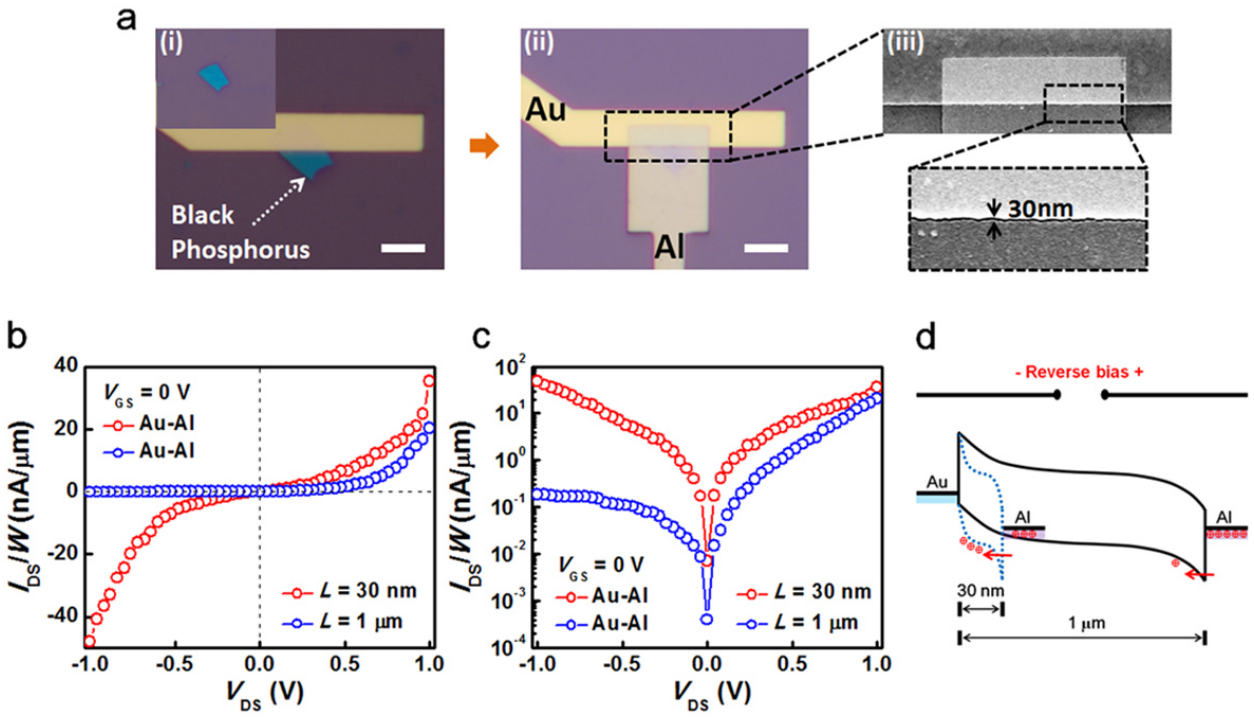

Figure 2.9 Electrical characteristics of ultrashort channel BP Schottky diodes with asymmetric metal contacts. (a) Optical and SEM images illustrating the fabrication process of an ultrashort channel BP Schottky diode: (i) Optical micrograph showing the BP flake contacted by one Au electrode. Scale bar: 4 μm. Inset: the same BP flake before electrode patterning; (ii) Optical micrograph of the same device after the patterning of a second Al electrode using angle evaporation. Scale bar: 4 μm; (iii) SEM images showing the details in the channel region of the BP Schottky diode. The small gap between the two electrodes is around 30 nm. (b) Linear scale output characteristics of long channel length (L = 1 μm) and ultrashort channel length (L = 30 nm) BP Schottky diodes. (c) Semi-logarithmic scale plot of panel b. (d) Energy band diagrams of long channel and ultrashort channel BP Schottky diodes under reverse bias.

contacts demonstrated in this work can be readily used as photodetectors. With the built-in potential created by the asymmetric metal contacts, electron-hole pairs created upon light illumination can be effectively separated, resulting in light current as illustrated in the energy band diagram in Figure 2.10a. The photoresponse of the BP Schottky diode is measured and presented in Figure 2.10b. Under light illumination (red curve in Figure 2.10b), the device exhibit photovoltaic effect with a short-circuit current (I_{sc}) of around 0.35 nA at a V_{DS} of 0 V and a V_{GS} of 10 V. The open-circuit voltage (V_{oc}) is relatively small at around 0.05 V which is comparable to preview BP photovoltaic work.[88] When V_{DS}

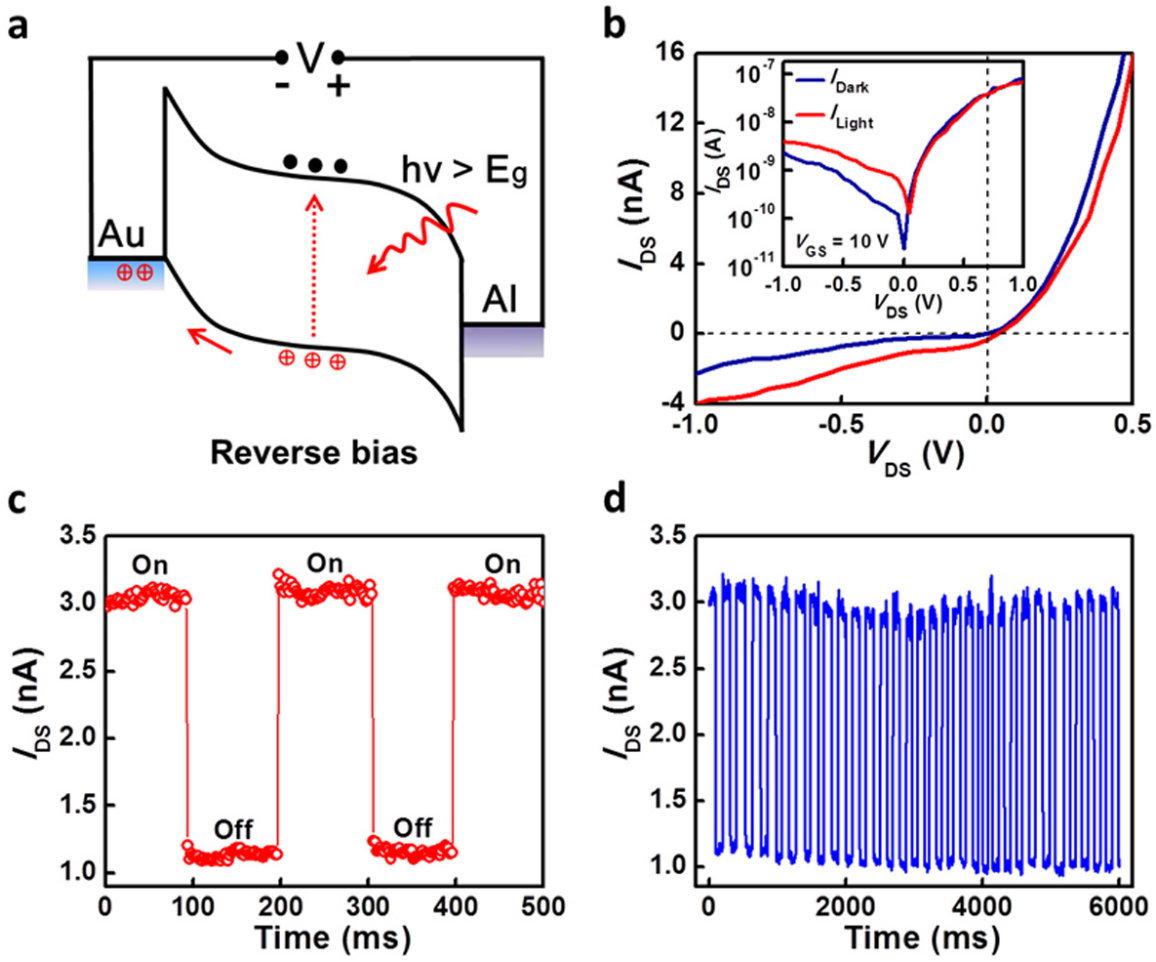

Figure 2.10 Photoresponse of BP Schottky diodes with asymmetric metal contacts. (a) Energy band diagram illustrating the photo-generated electron-hole pairs separated by the built-in potential, leading to photocurrent. (b) Output characteristics measured in the dark and under laser illumination at V_{GS} = 10 V. The inset shows the same plot in semi-logarithmic scale. (c) Photocurrent (measured at V_{DS} = -1 V and V_{GS} = 10 V) plotted as a function of time with incident laser chopped at a frequency of 5 Hz. (d) Photoswitching of the BP Schottky diode for extended period of cycles measured at V_{DS} = -1 V and V_{GS} = 10 V.

equals V_{oc}, the Schottky diode is forward biased with the forward current flowing in the opposite direction of the photocurrent, resulting in a zero net current. The presence of an open-circuit voltage and the fact that the BP is nearly depleted with V_{GS} = 10 V suggest that the photogeneration mechanism is most likely photovoltaic effect instead of bolometric effect.[89, 90, 91, 92] Furthermore, unlike the photoconductor type photodetectors whose switching speed is relatively slow (inversely proportional to the minority carrier lifetime), the BP Schottky diode exhibit fast photoresponse due to the existence of a built-in potential. The switching speed in such photodiodes is limited by the carrier transport velocity through the material, which is typically much faster. Figure 2.10c shows the photocurrent (measured at V_{DS} = -1 V and V_{GS} = 10 V) as a function of time under modulated light excitation with a frequency of 5 Hz. The BP Schottky diode exhibits fast response with rise and fall times of less than 2 ms. The cycling test of the BP Schottky diode photodetector (Figure 2.10d) also indicates that the photoswitching characteristics is well retained after repeated on-off switching cycles

2.8 Summary

In summary, we first report a facile method combining EBL and angle deposition to fabricate high-performance top-gated BP FETs with channel lengths down to 20 nm. With such small channel length, the devices show very high on-current. In addition, such ultrascaled BP transistors still preserve decent on-off current ratio (more than 10^2), and field effect mobility, which demonstrates the great potential of using BP for high-performance future ultimately scaled electronic devices. In addition, we have demonstrated BP-based Schottky diodes with current rectifying behavior by using asymmetric metal contacts. Inspired by angle deposition to achieve ultrascaled devices, we studied the channel scaling of BP Schottky diodes and showed that the channel length plays a critical role in determining the output characteristics of the Schottky diodes. If the channel length is aggressively scaled down to

around 30 nm, the diode could lose its rectifying characteristics due to increased tunneling current caused by electric field induced Schottky barrier thinning. The results indicate that relatively long channel is preferred if the BP Schottky diode is to be used as high on-off ratio photodetectors. With a built-in potential caused by the metal work function difference in the asymmetrically contacted BP Schottky diode, photodetectors with fast response time of less than 2 ms has been demonstrated.

CHAPTER 3

AIR-STABLE BLACK PHOSPHORUS HUMIDITY SENSORS

As a new family member of 2D layered materials, BP has attracted significant attention for chemical sensing applications due to its exceptional electrical, mechanical, and surface properties. However, producing air-stable BP sensors is extremely challenging because BP atomic layers degrade rapidly in ambient conditions. In this study, we explored the humidity sensing properties of BP transistors fully encapsulated by a 6-nm-thick Al_2O_3 encapsulation layer deposited by ALD. The encapsulated BP sensors exhibited superior ambient stability with no noticeable degradation in sensing response after being stored in air for more than a week. Compared with the bare BP devices, the encapsulated ones offer long-term stability with a tradeoff in slightly reduced sensitivity. Capacitance-voltage (C-V) measurement results further reveal that instead of direct charge transfer, the electrostatic gating effect on BP flakes arising from the dipole moment of adsorbed water molecules is the basic mechanism governing the humidity sensing behavior of both bare and encapsulated BP sensors. This work demonstrates a viable approach for achieving air-stable BP-based humidity or chemical sensors for practical applications.

3.1 Introduction

2D van der Waals crystals, such as graphene and TMDs, exhibit promising prospects for electronic and sensing applications due to their unique electrical, structural, and physicochemical properties.[93, 94] Also, the inherent large surface-to-volume ratio of 2D materials leads to a large number of adsorption/active sites (defects, vacancies, and edges) for selective molecular adsorption.[95] In the past few years, a variety of 2D materials have been extensively studied as potential chemical and gas sensing materials. For example, graphene has

been demonstrated as a promising material candidate for detecting humidity,[96] gases,[97] and biomolecules[98] owing to its ultrahigh carrier mobility, good mechanical and environmental stability, and high conductivity. Atomically thin TMDs such as MoS_2 and WSe_2 have also been widely studied for high-performance chemical and gas sensors,[99, 100, 101] and their performance can be further improved by surface functionalization.[102] Recently, mono- and few-layer BP, the most stable allotrope of phosphorus with a puckered orthorhombic structure, has demonstrated its potential applications in the field of electronic devices and sensors.[19, 95] Layered BP shows superior chemical sensing performance compared with other 2D materials (for example, graphene and MoS_2) because BP has higher molecular adsorption energy, lower out-of-plane electrical conductance, and larger surface-to-volume ratio than other 2D materials which can maximize the effect of adsorbed chemical molecules on BP thin flakes.[95, 103, 104] The previous studies have demonstrated that BP exhibits high sensitivity to humidity,[105] NO_2,[104] NH_3,[106] and other chemical vapors.[107] However, these BP sensors, using relatively thin BP flakes, will inevitably degrade rapidly in ambient conditions since O_2 saturated H_2O can react with BP to form oxidized phosphorus.[57] Relatively stable BP sensors can be achieved by using very thick and stacked BP flakes that were liquid exfoliated.[95, 107] However, such devices will lose the transistor behavior (no gate dependence) and can be very hard to scale down. Considering the above mentioned issues, achieving air-stable sensing performance is extremely critical to few-layer BP sensors for practical applications. To the best of our knowledge, few-layer BP-based ChemFET sensors with long-term ambient stability have not been reported. In fact, it was speculated that passivated BP FETs would not be applicable for chemical sensing applications due to lack of direct exposure of the device active materials to chemicals.

Here, we have systematically investigated the humidity sensing characteristics of few-layer BP FETs with and without the presence of passivation. Because the few-layer BP flakes are known to undergo degradation rapidly in ambient conditions, a thin Al_2O_3 dielectric layer (6 nm in thickness) was deposited on top using ALD to serve as the encapsulation

layer, which is thick enough to preserve BP devices from degradation as confirmed by AFM, Raman spectroscopy, and electrical measurements. We exposed the BP FETs to various controlled humidity levels at room temperature and monitored changes in their electrical characteristics. The BP sensor prior to Al_2O_3 encapsulation showed p-type behavior and exhibited a monotonic increase in conductance upon exposure to higher humidity levels. The transfer characteristics of the same BP device became ambipolar after Al_2O_3 encapsulation, and exhibited an increased p-branch current and decreased n-branch current upon exposure to water vapor. More importantly, the encapsulated BP sensors were found to exhibit drastically improved long-term stability in air with almost no change in sensing response after being stored in air for over a week. Finally, the C-V measurements revealed that the electrostatic interaction between dipole moment of water molecules and BP flakes is a probable mechanism governing the humidity sensing behavior of BP sensors. This work demonstrates the feasibility of achieving air-stable BP-based humidity or chemical sensors for practical applications.

3.2 Encapsulated Black Phosphorus for Humidity Sensors

Figure 3.1 shows the schematics of two types of BP FET-based humidity sensors (with and without Al_2O_3 encapsulation layer) compared in this study. Firstly, few-layer BP flakes were mechanically exfoliated from bulk BP crystals, using a scotch tape, onto a silicon substrate. Gold S/D electrodes with a thickness of 50 nm were then defined by standard EBL, metal evaporation, and lift-off processes. Finally, a 6-nm-thick Al_2O_3 dielectric layer was deposited by ALD to fully encapsulate the BP device, which can effectively prevent the underlying BP flake from reacting with water molecules and oxygen in the ambient conditions. Figure 3.1b shows the experimental setup used for BP humidity sensing measurements. The as-fabricated BP sensors were tested with different humidity levels at room temperature. An argon gas passes through a bubbler filled with water and delivers moisture to the surface of

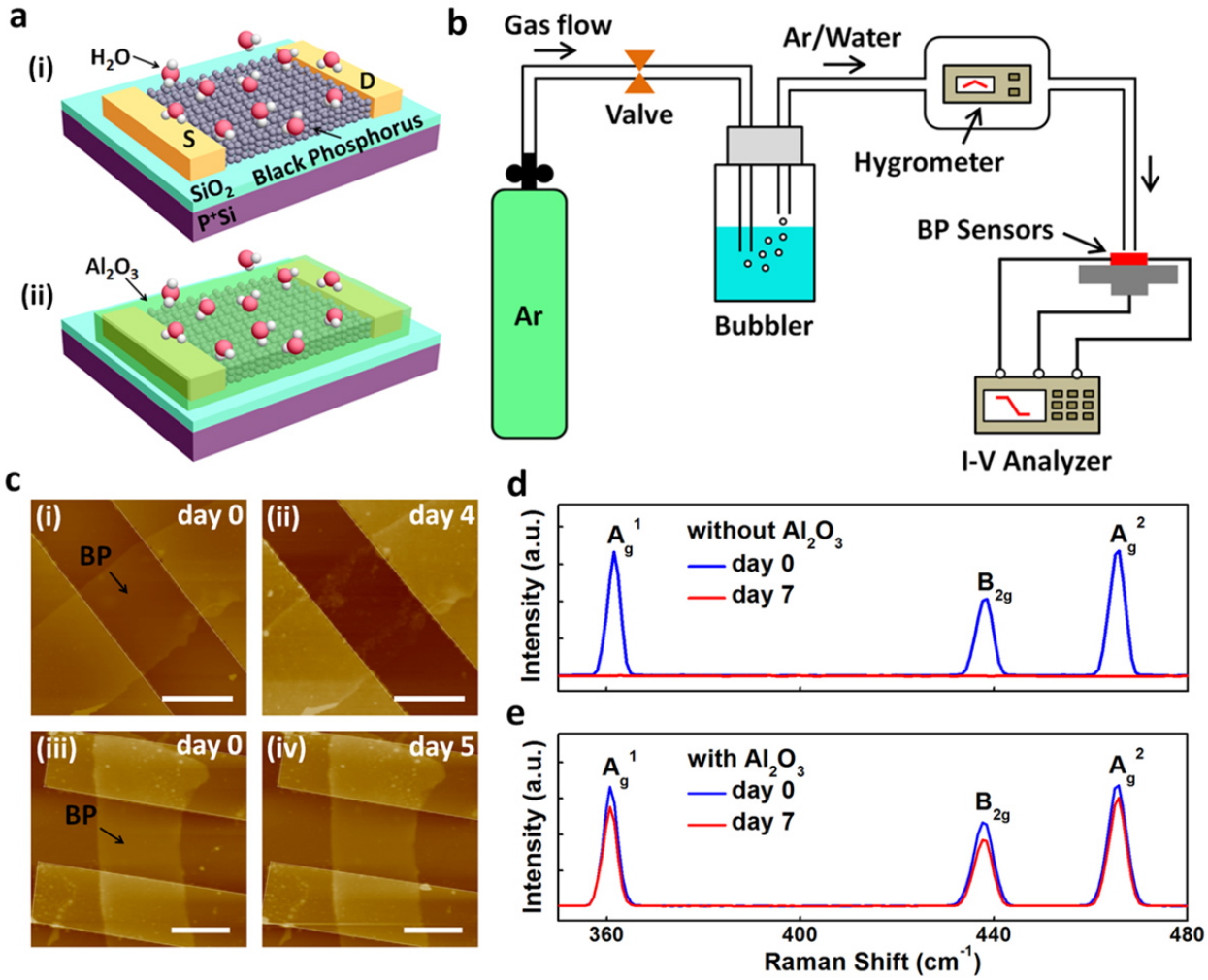

Figure 3.1 Air-stable humidity sensor using few-layer BP. (a) Schematic of BP FET based humidity sensors (i) without and (ii) with Al_2O_3 passivation layer. (b) Schematic illustrating the experimental setup used for humidity sensing measurements. (c) AFM images of BP humidity sensor without Al_2O_3 encapsulation (i) right after fabrication and (ii) after 4 days in ambient condition; (iii) with a 6-nm-thick Al_2O_3 encapsulation layer right after fabrication and (iv) after 5 days in ambient condition. The white dashed lines outline the device S/D electrodes. The scale bar is 2 m in (i) and (ii) and 2.5 m in (iii) and (iv). (d) Raman spectra of an unencapsulated BP flake right after exfoliation (blue line) and after 7 days in ambient condition (red line). (e) Raman spectra of an encapsulated BP flake with a 6-nm-thick Al_2O_3 encapsulation right after exfoliation (blue line) and after 7 days in ambient condition (red line).

the BP sensor. Relative humidity (RH) level was monitored in real-time by a hygrometer inside a sealed container along the gas flow path. The RH level can be effectively controlled by varying the argon flow rate. Figure 3.1c illustrates the efficacy of using Al_2O_3 as a passivation layer. Four days after it was fabricated, the bare BP device degraded completely under the ambient condition. In contrast, the BP device passivated by a 6-nm-thick Al_2O_3 layer did not show any noticeable change after being stored in the ambient condition for over 5 days. More details regarding the BP stability study are presented in Figure 3.2 and further demonstrate that ALD Al_2O_3 can effectively suppress the BP degradation. The Raman spectra of BP flakes with and without Al_2O_3 passivation are also studied and compared as shown in Figure 3.1d and e. The three Raman peaks located at 362, 438, and 466 cm^{-1} correspond to the ${A_g}^1$, B_{2g} and ${A_g}^2$ phonon modes of typical few-layer BP flake.[38, 22] For the bare BP flake, no Raman peaks were observed after 7 days of ambient exposure (red line, Figure 3.1d). In contrast, all of the three Raman peaks remain at the identical positions for the encapsulated BP flake and show very similar peak intensities before and after being exposed to the ambient condition for over 7 days (Figure 3.1e), further demonstrating the effectiveness of ALD Al_2O_3.

3.3 Doping Effect of ALD Al_2O_3 Encapsulation Layer

The influence of ALD Al_2O_3 passivation on the electrical characteristics of BP FETs is presented in Figure 3.3. The transfer curves of the same BP transistor before (blue line) and after (red line) depositing a 6-nm-thick Al_2O_3 dielectric show a transition from p-type to ambipolar transistor behavior with a dramatically enhanced n-branch current (before ALD 2.3 nA/μm, after ALD 260.6 nA/μm) and transconductance (before ALD 10^{-5} μS/μm, after ALD 10^{-2} μS/μm), as shown in Figure 3.3a and b. Statistical study on eight BP devices before and after Al_2O_3 encapsulation indicates that all devices exhibit similar transition to ambipolar behavio, as shown in Figure 3.4. It is also worth noting that the device hole

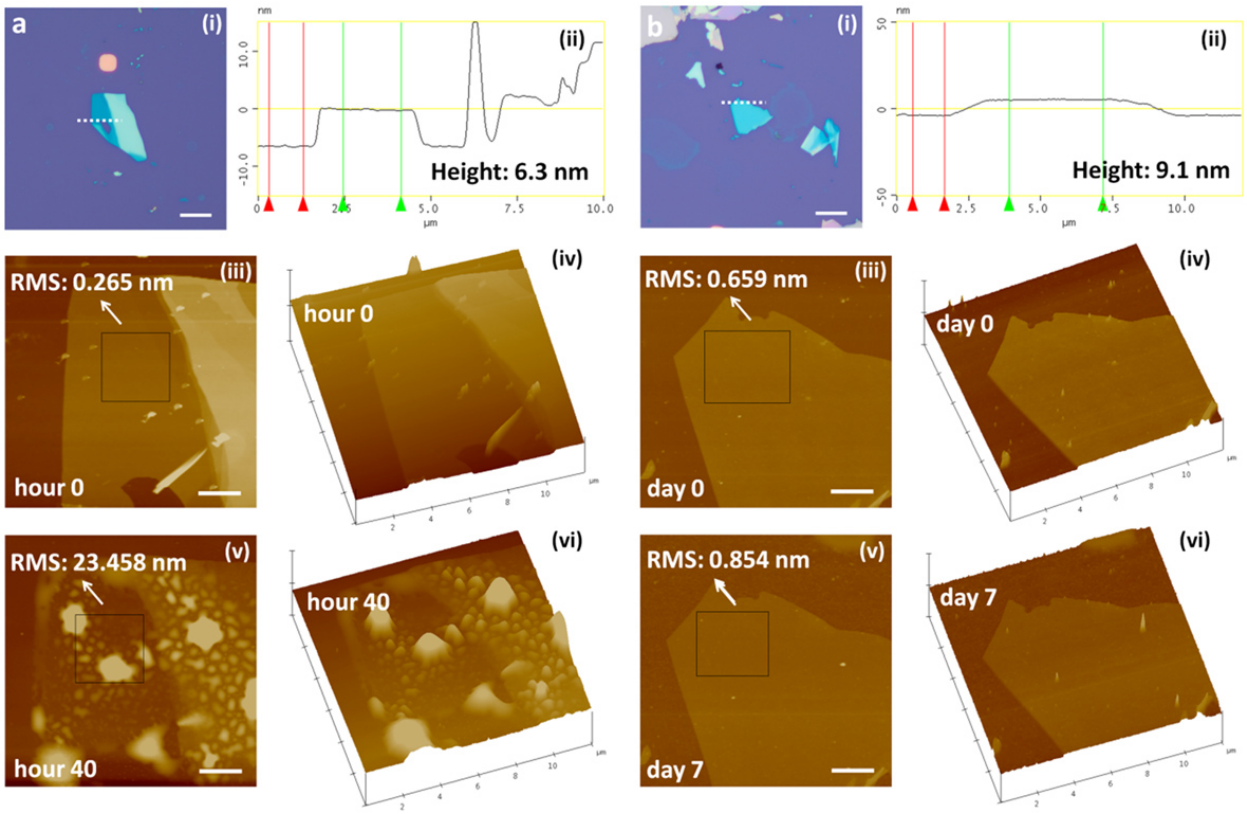

Figure 3.2 Optical microscope and AFM images of representative BP flakes (a) without Al_2O_3 encapsulation and (b) with a 6-nm-thick Al_2O_3 encapsulation layer. The scale bars are 10 μm for panel a (i) and b (i) and 2 μm for panel a (iii, v) and b (iii, v).

mobilities (100 $cm^2V^{-1}s^{-1}$) and current on-off ratios (10^4) show little change after Al_2O_3 passivation (Figure 3.3c and d). The enhanced n-branch current can be attributed to the doping effect of ALD Al_2O_3 and the subsequent reduction of Schottky barrier thickness for electrons at the BP-Au contact edge (Figure 3.3c).[108, 109] For the BP FETs with Au contact, Schottky barriers exist for both holes and electrons at the interface. The positive fixed charges in the Al_2O_3 dielectric induced by the deficiency of oxygen atoms will bend the energy band downward, leading to a reduced Schottky barrier thickness for electrons, which makes it much easier for electrons to inject from metal into conduction band through a tunneling process. Figure 3.3d and e show the device output characteristics before and after Al_2O_3 encapsulation under various gate voltages. It can be clearly seen again that the p-branch current (V_g = -70, -50 and -30 V) exhibits little change after depositing Al_2O_3

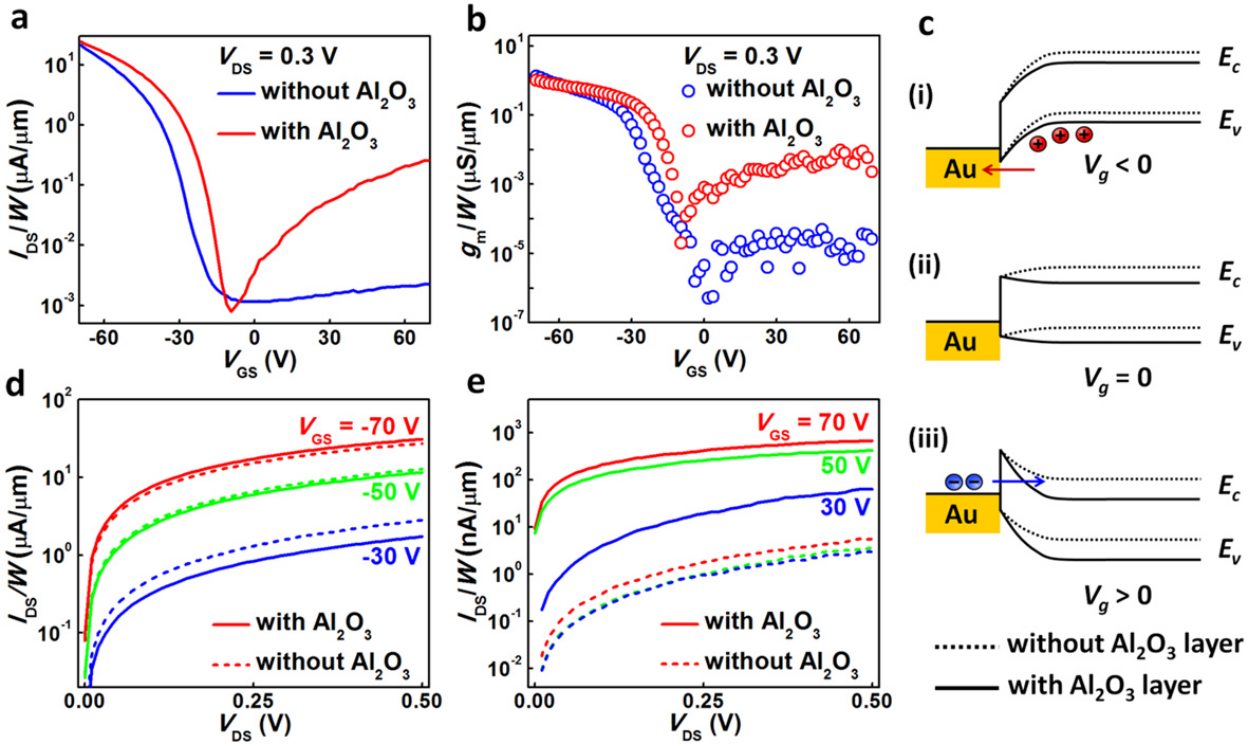

Figure 3.3 Electrical characteristics of the BP FET before and after ALD encapsulation. (a) Transfer characteristics of the same BP FET before (blue line) and after (red line) depositing a 6-nm-thick Al_2O_3 dielectric layer on top. (b) Device transconductance before (blue) and after (red) Al_2O_3 encapsulation deduced from panel (a). (c) Illustrations of the energy band diagram at BP-Au contact before (dashed line) and after (solid line) Al_2O_3 encapsulation under various gate voltages. (d, e) Semi-logarithmic scale plot of the output characteristics for the same BP device (d) under negative gate voltages and (e) under positive gate voltages. Dashed line: without Al_2O_3 layer. Solid line: with Al_2O_3 layer.

while the n-branch current (V_g = 70, 50 and 30 V) is significantly enhanced.

3.4 Humidity Sensing Response

The humidity sensing experiment results of both unencapsulated and encapsulated BP FET sensors are shown in Figure 3.5. Under the ambient condition (RH = 21% and room temperature), the BP FET without Al_2O_3 passivation exhibited p-type transistor behavior with a current on-off ratio of 3.4 × 10 ^{3} and on-current of 20 μA/μm at a V_{DS} = 0.5 V (black line, Figure 3.5a). An up-shift in the transfer curves was observed as the BP sensor was

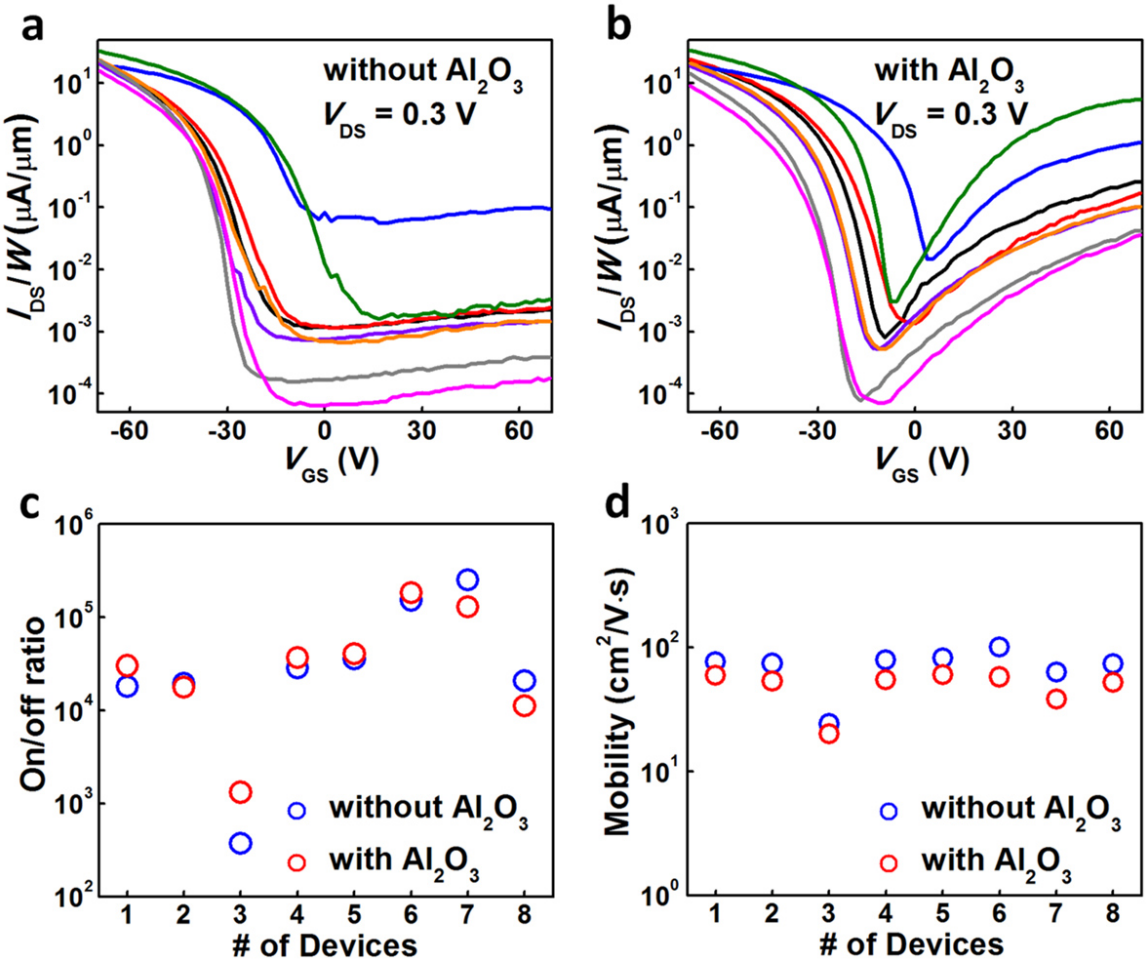

Figure 3.4 Transfer characteristics of eight representative BP FETs (a) before and (b) after depositing a 6-nm-thick Al_2O_3 dielectric layer on top. (c, d) Device on-off ratio (c) and mobility (d) before and after Al_2O_3 encapsulation.

exposed to increasing RH levels (blue line RH = 59%, orange line RH = 71%, and red line RH = 83%). The increased electrical conductivity can be attributed to the increased hole concentration induced by water molecules adsorbed on the BP flake. In addition, the subthreshold slope of the transfer curves decreased with the increasing RH level, indicating a reduced carrier mobility, which can be ascribed to the surface scattering caused by the adsorbed water molecules on top of the BP flake. Here it is important to recognize that the sensing mechanism of the unencapsulated BP FET sensors may be quite different depending on how the sensors are fabricated.

In case of the BP humidity sensors made of very thick films (tens of μm; synthesized by

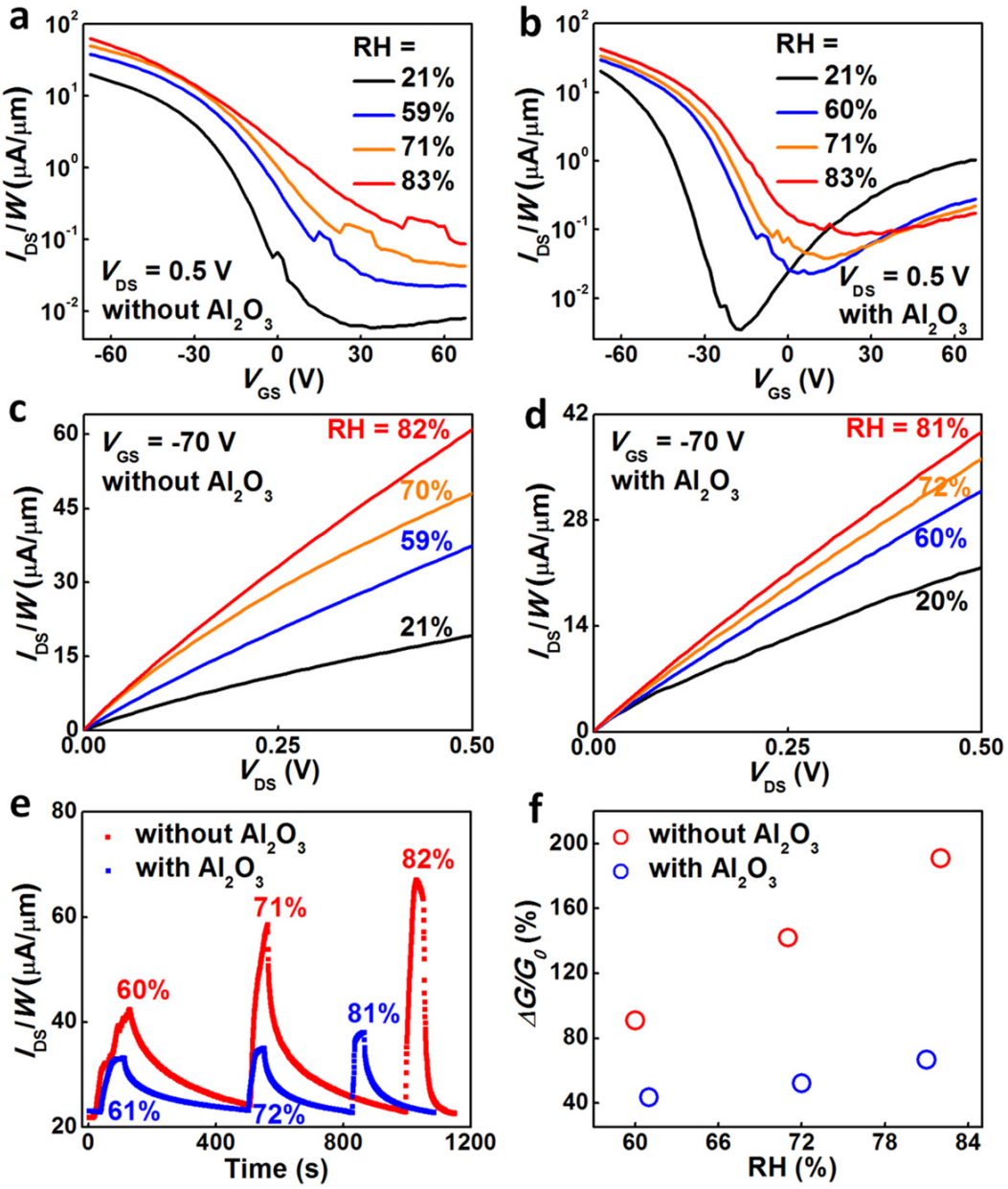

Figure 3.5 Sensing response of the BP humidity sensors. (a, b) Transfer characteristics of a representative BP sensor (a) without and (b) with a 6-nm-thick Al_2O_3 encapsulation layer upon exposure to different RH levels. (c, d) Output characteristics of the same BP device (c) before and (d) after depositing Al_2O_3 upon exposure to various RH levels. (e) Dynamic sensing response for the same BP sensor without (red) and with (blue) Al_2O_3 capping layer upon exposure to different RH levels. (f) Relative conductance change ($\Delta G/G_0$) plotted as a function of RH levels showing the sensitivity of the device.

depositing liquid-exfoliated BP flakes), the absorbed water molecules would form conducting ions within the highly resistive random network of BP flakes, significantly modulating the overall electric transport.[105] Meanwhile, working principles of humidity or gas sensors consisting of an individual few-layer BP flake is generally believed to rely on direct charge transfer from water or gas molecules to the BP surface.[103, 106, 110] For example, in case of NO_2 and NH_3 sensing, upon gas adsorption on the BP surface, the electron withdrawing molecule NO_2 (electron donating molecule NH_3) would lead to an increased (decreased) hole concentration and consequently higher (lower) device conductance in p-type BP FET device. The above is in good agreement with results found in the literature. However, the same charge transfer argument cannot be used to explain the increased conductance upon moisture injection as seen in our work and others.[110] This is because water molecules are electron donating, which should lead to decreased conductance in p-type BP FET upon exposure (similar to NH_3) if direct charge transfer was the main mechanism. Therefore, an alternative explanation is required to explain the observed response (increased conductance) of the bare BP sensor to humidity. As will be discussed later in the paper, we attribute the sensing mechanism to the electrostatic gating effect induced by the dipole moment of adsorbed water molecules.

Moreover, to address a concern that the bare BP devices may degrade rapidly during the humidity sensing experiments, we conducted a short-term stability study on one of the bare BP FET devices by exposing it to humidity, as shown in Figure 3.6. After initial injection of water vapor (RH = 69%) on the BP device, both transfer and output curves show an abrupt up-shift (red lines in Figure 3.6a and b). After the water vapor injection was turned off, the characteristics of the BP sensor gradually recovered to their original states. After around 1 hour, both transfer and output curves almost overlap with the original curves at 21% RH. From the results, one can safely conclude that although the bare BP sensor will inevitably degrade in ambient condition due the chemical reaction with moisture, the devices can remain stable for a short period of time, at least within the time frame of the

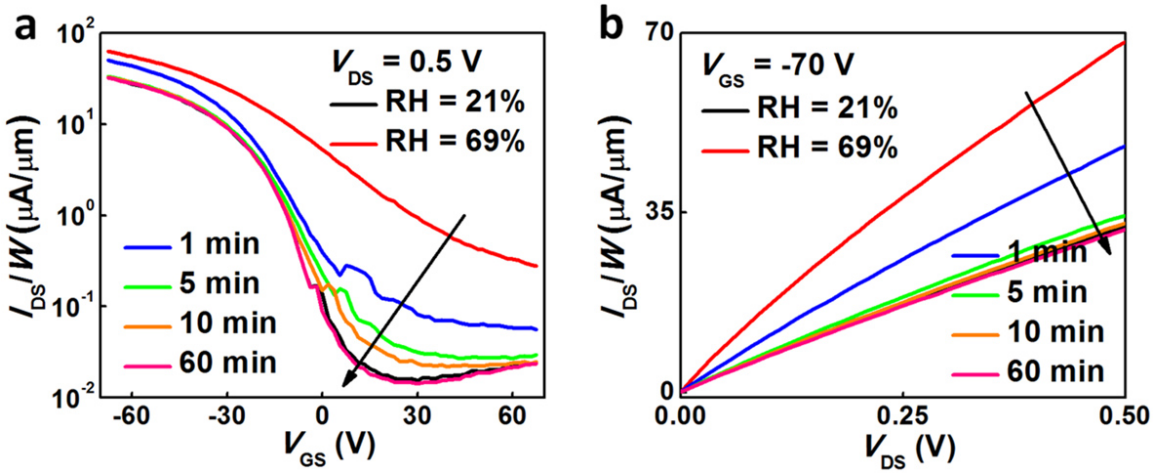

Figure 3.6 (a, b) Evolution of the transfer (a) and output (b) characteristics of an unencapsulated BP sensor upon initial exposure to water vapor (RH = 69%) and after the water vapor was switched off.

experiments. Therefore, it would be valid to compare the sensing response of the same BP device before and after encapsulation with the ALD Al_2O_3 layer.

Next, the sensing behavior of the same BP device in Figure 3.5a was studied after deposition of a 6-nm-thick Al_2O_3 dielectric layer on top. After encapsulation, the transfer curves (black line, Figure 3.5b) converted to ambipolar behavior, which is in agreement with the discussion above in Figure 3.3. Upon exposure to different RH levels, the encapsulated BP sensor exhibited increased p-branch current and decreased n-branch current, as shown in Figure 3.5b (blue line RH = 60%, orange line RH = 71%, and red line RH = 83%). The dynamic sensing response of BP device at a positive gate bias of V_{GS} = 70 V further demonstrates the p-branch current decrease upon multiple pulses of water vapor injection, as shown in Figure 3.7. Similarly, the behavior could also be attributed to the electrostatic dipole moment of the adsorbed water molecules on Al_2O_3 inducing an downward bending of the energy band, thus changing the Schottky barrier for both electrons and holes at the BP-Au contacts.[110, 111] More specifically, the electrostatic gating effect from the water molecules causes a positive shift of the threshold voltage, which leads to the increased p-branch current (due to the reduced Schottky barrier thickness for holes) and the decreased

n-branch current (due to the increased Schottky barrier thickness for electrons).

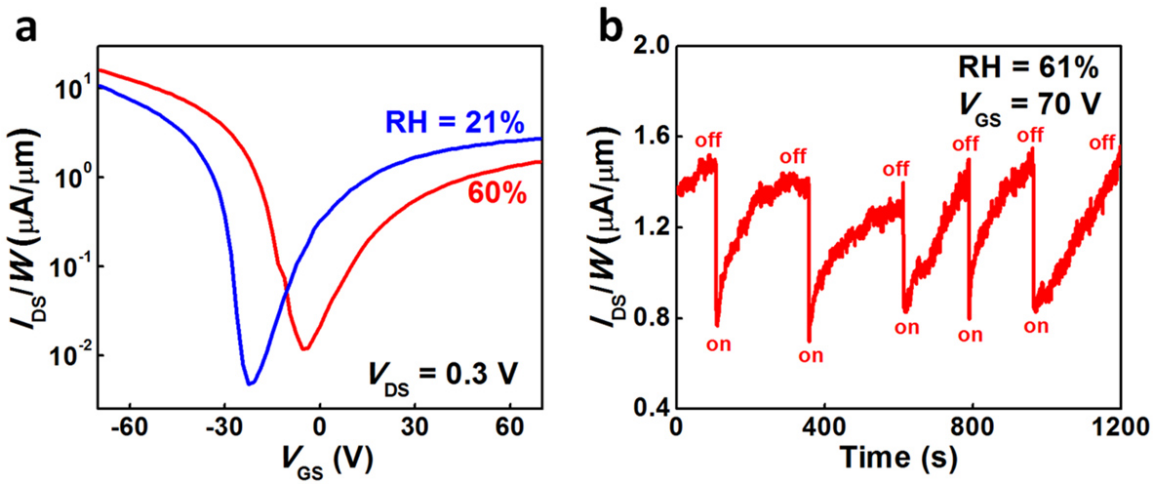

Figure 3.7 (a) Transfer characteristics of an encapsulated BP sensor upon exposure to different humidity levels. (b) Sensing response of the same device when exposed to multiple pulses of water vapor injection under positive gate voltage (V_{GS} = 70 V).

The output characteristics of the same BP sensor before (Figure 3.5c) and after (Figure 3.5d) Al_2O_3 encapsulation both exhibited monotonic current increase as the RH level increased. On the other hand, it is clear that the response (current increase) for the unencapsulated BP device is larger than the encapsulated one upon exposure to the same RH level. The slightly reduced response/sensitivity is caused by the existence of the 6-nm-thick Al_2O_3 dielectric layer, which weakens the electrical field induced by the electrostatic dipole moment of water molecules. The dynamic sensing response (V_{DS} = 1 V, V_{GS} = -60 V) for the BP sensor without (red) and with (blue) Al_2O_3 encapsulation are compared in Figure 3.5e. It clearly shows the increase in the drain current upon injection of water vapor (without Al_2O_3 dielectric: 3-fold enhancement in drain current at RH = 82%; with Al_2O_3 dielectric: 1.7-fold enhancement in drain current at RH = 81%), and the BP sensor can completely recover to its original state as the water vapor injection is switched off. In Figure 3.5f, the device relative conductance change ($\Delta G/G_0$) is plotted as a function of the RH level, where $\Delta G = G\text{-}G_0$, G is the instantaneous conductance exposure to various RH levels and G_0 is device conductance in ambient conditions (RH = 21%). The $\Delta G/G_0$ increases linearly with

the increasing RH level for both sensors, suggesting the sensor's linear dynamic behavior. With regard to sensitivity, defined as the slope in Figure 3.5f, the bare BP sensor (red cycles) shows higher performance than the encapsulated one (blue cycles).

3.5 Long-Term Stability of Black Phosphorus Humidity Sensors

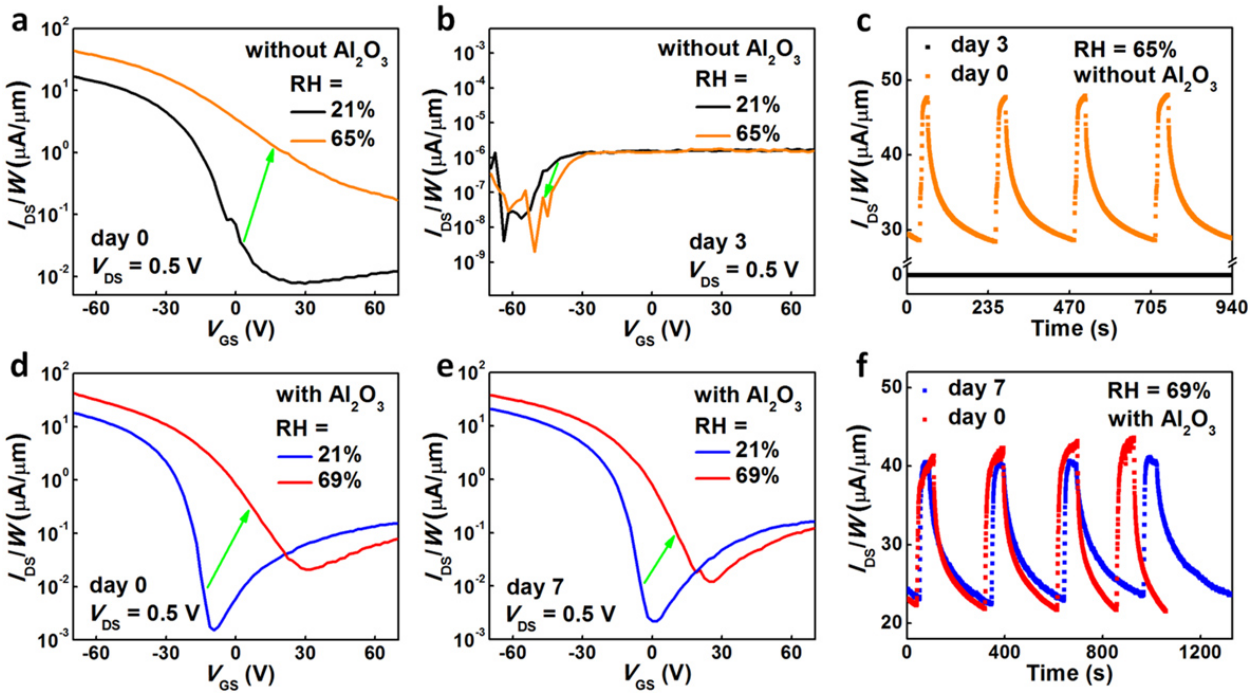

Figure 3.8 Long-term stability of the BP humidity sensors. (a, b) Transfer characteristics of a BP sensor without Al_2O_3 encapsulation exposed to various levels of RH when (a) it was freshly made and (b) after being stored in ambient condition for 3 days (black line RH = 21%, orange line RH = 65%). (c) Dynamic sensing response for the unencapsulated BP sensor right after fabrication (orange) and after being stored in ambient for 3 days (black). (d, e) Transfer characteristics of a BP sensor encapsulated by Al_2O_3 exposed to various levels of RH when (d) it was freshly made and (e) after being stored in ambient condition for 7 days (blue line RH = 21%, red line RH = 69%). (f) Dynamic sensing response for the encapsulated BP sensor right after fabrication (red) and after being stored in ambient for 7 days (blue).

Although the unencapsulated BP sensor is slightly more sensitive, it is challenging to make them air-stable for practical applications because atomically thin BP flakes are known to undergo degradation upon exposure to moisture. Therefore, adding a 6-nm-thick Al_2O_3

layer on top is a good tradeoff between sensitivity and long-term stability. Figure 3.8a, b and c show the sensing response of a representative unencapsulated BP sensor, when it was fresh and after exposure to ambient conditions for 3 days. Comparing Figure 3.8 a and b, one can clearly see that the fresh BP sensor without Al_2O_3 encapsulation is completely degraded and exhibits no response to water vapor after being stored in ambient for 3 days. The dynamic sensing response in Figure 3.8c also demonstrates the irreversible degradation. In contrast, a fresh BP sensor, when properly encapsulated by depositing a 6-nm-thick Al_2O_3 layer on top, could still preserve a good sensing response even when stored in ambient conditions for over 7 days (Figure 3.8d and e). The dynamic sensing response of the encapsulated device before and after 7 days of ambient exposure presented in Figure 3.8f also shows no noticeable change. On the basis of above experiments, one can conclude that the ALD Al_2O_3 dielectric layer provides a sufficient barrier for moisture diffusion and effectively suppress degradation of BP sensors while still maintaining good sensing sensitivity.

3.6 Capacitance-Voltage Characteristics of Black Phosphorus Humidity Sensors

To further shed light on the sensing mechanism of the BP humidity sensors with and without Al_2O_3 encapsulation, C-V measurements were further performed as illustrated in Figure 3.9. All C-V data presented are measured at a frequency of 1 MHz. Figure 3.9a shows the schematic of C-V measurement setup where the gate of the BP FET is connected to the HIGH terminal while the S/D electrodes are both connected to the LOW terminal of the C-V analyzer. Unlike the back-gated BP devices for the I-V measurements, it is crucial for the devices under C-V characterization to have a localized back-gate (Figure 3.9b) in order to minimize the parasitic pad capacitance. Otherwise, if a conventional back-gated BP FET was used for the C-V measurement, the device capacitance versus the gate voltage curve would just show a straight line due to the large parasitic capacitance of S/D electrodes and

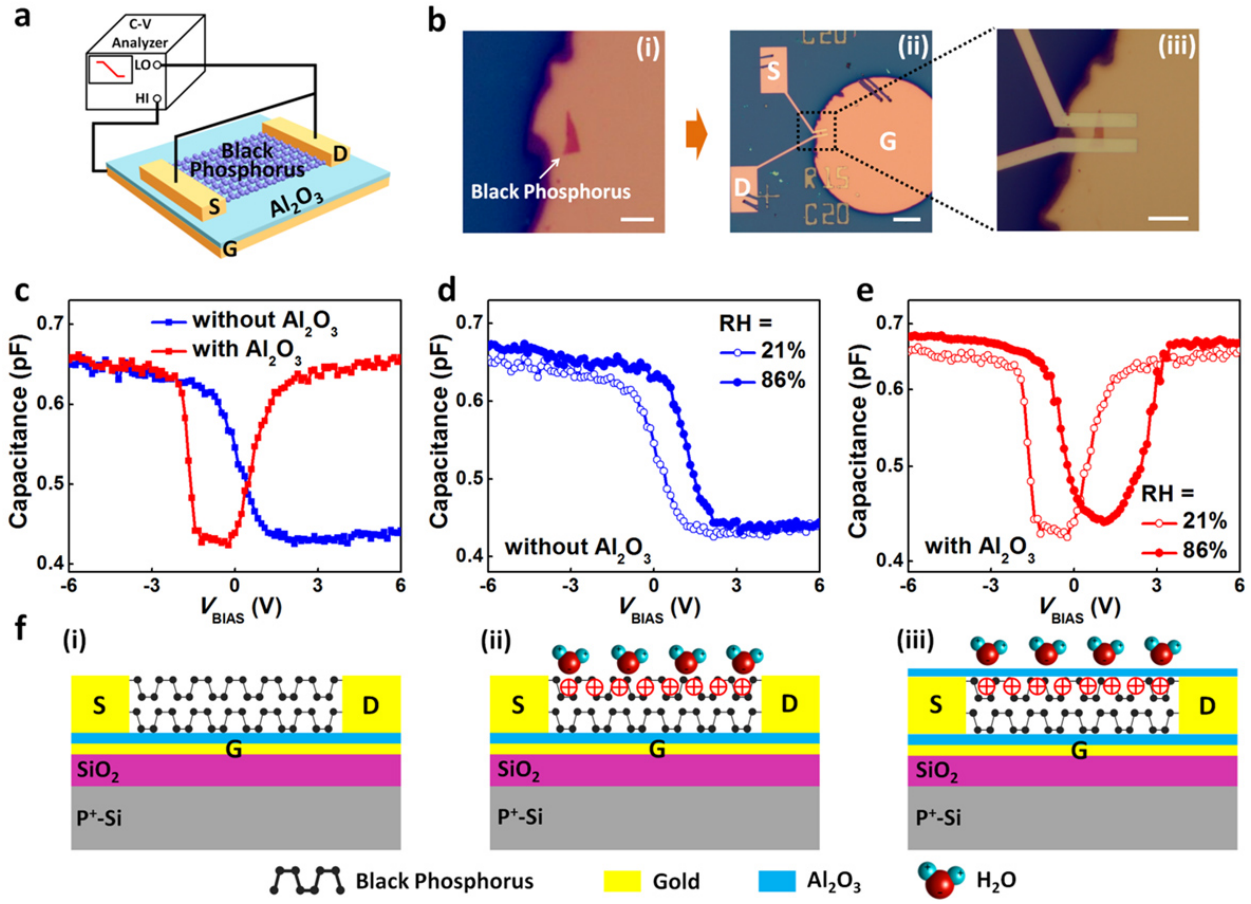

Figure 3.9 Capacitance-voltage characteristics of the BP humidity sensors. (a) Schematic illustrating the C-V measurement setup used in this study. (b) Optical microscope images of (i) the BP flake, (ii) the BP FET with localized gate, and (iii) zoomed-in view of the device channel marked by the dashed box in ii. The scale bars in i, ii, iii are 6 μm, 30 μm, and 8 μm, respectively. (c) C-V characteristics of the BP FET in panel b before (blue) and after (red) deposition of a 6-nm-thick Al_2O_3 capping layer. (d) C-V characteristics of the BP sensor without Al_2O_3 encapsulation upon exposure to different RH levels. (e) C-V characteristics of the same BP device with ALD Al_2O_3 encapsulation upon exposure to different RH levels. (f) Schematics of (i) a fresh unencapsulated BP FET, (ii) unencapsulated BP FET exposed to water vapor, and (iii) encapsulated BP FET exposed to water vapor, illustrating the humidity sensing mechanism.

pads. To achieve the locally-gated BP FET, we first fabricated periodic Ti/Au (1 nm/40 nm) disks on the silicon substrate and then deposited a 10-nm-thick Al_2O_3 layer by ALD on the entire substrate as the gate dielectric layer. The few-layer BP flakes were transferred onto the sample using standard mechanical exfoliation, and an optical microscope was used to locate the BP flakes that were near the edge of the metal disks. Finally, the BP devices with localized gate were fabricated using EBL, metal evaporation, and lift-off as described previously. Figure 3.9c presents the C-V characteristics of a representative BP FET before and after a 6-nm-thick Al_2O_3 layer was deposited on the top. Without encapsulation (blue line, Figure 3.9c), the BP FET can be fully depleted with V_{BIAS} greater than 1 V, which is expected for conventional p-type FET behavior. However, the same BP device after Al_2O_3 encapsulation (red line, Figure 3.9c) exhibits ambipolar transistor behavior and enters accumulation region for both negative and positive gate voltages. The channel is depleted only when the V_{BIAS} is in between -1.5 V and 0 V.

Figure 3.9d shows the C-V characteristics of the BP device without Al_2O_3 upon exposure to a high RH level of 86%. It is clear that the entire C-V curve underwent a positive shift of around 1 V upon exposure to high moisture levels. A similar positive shift of the C-V curve was also observed in the same BP device after Al_2O_3 encapsulation (Figure 3.9e). The underlying sensing mechanism of BP FET responding to humidity can be attributed to the electrostatic interaction between water molecules and BP flakes for both unencapsulated and encapsulated devices and explained using the schematics in Figure 3.9f. Water molecule is the only one having a dipole moment among all the gasses in ambient air. The surface defects of substrate (Al_2O_3 or SiO_2) will give rise to charge transfer and dipole moment will be formed in the substrate layer.[112, 113] Therefore, substrate surface defects can lead to an impurity band, and the electrostatic dipole of water molecules will change the impurity band resulting in increased hole concentration in the BP flake.[112, 113] For the encapsulated BP sensor with a 6-nm-thick Al_2O_3 dielectric between BP flake and water molecules, the electrostatic field induced by water molecules will be weakened leading to a slightly smaller

sensitivity to humidity.

3.7 Summary

In this chapter, we have studied the humidity sensing behavior of few-layer BP FETs under ambient conditions. Because the BP flakes are known to degrade rapidly in ambient conditions, a 6-nm-thick ALD Al_2O_3 dielectric layer was used to passivate the BP sensors in order to make them air-stable. Thorough characterizations reveal that the ALD Al_2O_3 encapsulation can effectively suppress BP degradation, which lead to devices with drastically improved long-term stability in air with a tradeoff in slightly reduced sensitivity. Lastly, C-V measurements were used to elucidate the humidity sensing mechanism of BP devices. The electrostatic interaction between water molecules and BP flakes would result in increased hole concentration in BP, thus enhancing the p-branch current. Our results demonstrate a viable approach for achieving air-stable BP-based chemical sensors for practical applications.

CHAPTER 4

BLACK PHOSPHORUS NEAR-INFRARED PHOTODETECTORS AND CAMERAS

This chapter reports the BP based near-infrared photodetectors and cameras on rigid (silicon wafer) and flexible (polyimide) substrates. We have observed negative photoconductivity in BP transistors built on freestanding polyimide film. Near-infrared laser (λ = 830 nm) excitation leads to significantly suppressed device on-state current with a very high responsivity of up to 53 A/W. The underlying mechanism of the negative photoconductivity is attributed to the strong photothermal effect induced by the low thermal conductivity of polyimide substrate used. The heat generated by the infrared light illumination results in enhanced phonon scattering, reduced carrier mobility, and consequently negative photocurrent. Such phenomenon was not observed in similar BP devices built on silicon substrate whose thermal conductivity is much higher. The above photothermal mechanism is also supported by temperature-dependent electrical characterization and device simulation. In addition, we also demonstrated the use of a single-pixel photodetector made with few-layer BP thin film for near-infrared imaging applications. The imaging is achieved by combining the photodetector with a digital micromirror device to encode and subsequently reconstruct the image based on compressive sensing algorithm. Stationary images of a near-infrared laser spot with up to 64 $\times$ 64 pixels were captured using our single-pixel BP camera with 2000 times of measurements, which is only half of the total number of pixels. The imaging platform demonstrated in this work circumvents the grand challenges of scalable BP material growth for photodetector array fabrication and shows the efficacy of utilizing the outstanding performance of BP photodetector for future high-speed infrared camera applications.

4.1 Introduction

Infrared photodetectors or imaging systems have a wide range of industrial applications such as optical imaging,[114, 115] biomedical sensing,[116, 117, 118] space exploration,[119] and environmental monitoring.[120] Over the past few decades, development of high-performance photodetection materials and chip-scale fabrication technologies has led to significant advancement of infrared imaging systems.[121, 122] Despite the progress, more superior optoelectronic components with higher speed and efficiency, broader detection wavelength range, or new form factor such as being mechanically flexible are becoming more urgently needed.[123] Since the discovery of graphene, 2D materials have attracted great research interest for optoelectronic applications, driven by their excellent electrical, optical, and mechanical properties. A variety of prototype optoelectronic devices based on graphene have been successfully demonstrated, such as light-emitting diodes (LED),[124] ultrafast lasers,[125] optical modulators,[126, 127] and solar cells.[128, 129] However, graphene has severe limitations in photodetection applications due to the absence of a bandgap.[130, 131] Although tremendous effort has been devoted to the development of graphene photodetectors, the high dark current inevitably leads to large shot noise.[132] Other 2D semiconducting materials such as TMDs have relatively large bandgap and strong light absorption. However, these materials exhibit relatively slow response and they do not work at the important telecommunication wavelengths.[133] The recently rediscovered 2D BP, which has a direct bandgap ranging from 0.3 eV (bulk) to 2.0 eV (monolayer), could be a very promising 2D material for visible to mid-infrared detector applications. Few-layer BP based field-effect transistors (FETs) have shown high room-temperature mobility up to 1000 $cm^2V^{-1}s^{-1}$, current modulation up to 10^5, and good current saturation. Compared with traditional narrow-bandgap infrared detection materials, BP-based devices can be easily implemented on flexible substrates owing to its layered crystal structure and small thickness.[134, 135] More importantly, low-noise photodetection can be achieved using BP due to its moderate

direct bandgap. Nevertheless, recent studies on few-layer BP photodetectors only report modest responsivity of 4-150 mA/W in both visible light and infrared regime.[136, 137] Although one group reported much higher responsivity of 82 A/W, the device responsivity decreases drastically from 82 A/W to 0.2 A/W with increasing light intensity.

In this chapter, we first demonstrate high-performance flexible near-infrared photodetectors using few-layer BP with ultrahigh responsivity of 53 A/W at a laser intensity of 16.5 W/cm^2. The device was built on an ultrathin polyimide substrate, whose low thermal conductivity (0.2 Wm^{-1}K^{-1}) leads to strong photothermal effect and substrate heating upon light illumination.[138] The photo-generated heat leads to enhanced phonon scattering and mobility degradation, which generate significant negative photocurrent of 20 to 30 μA at a light intensity of 16.5 W/cm^2. Temperature-dependent study of the device electrical characteristics and device simulation using Sentaurus TCAD further confirm the heating is the underlying mechanism governing the negative photoconductivity in flexible BP FETs. The photothermal effect-based flexible BP photodetector may find interesting potential applications in high-sensitivity broadband wearable and bio-integrated photodetectors or imaging systems.

4.2 Flexible Black Phosphorus Photodetectors on Polyimide Substrate

Figure 4.1 illustrates the fabrication process flow for a flexible BP FET on the polyimide substrate. Specifically, liquid polyimide was spun coated on a silicon handling wafer followed by annealing at 300 °C to form an ultrathin (10 μm) flexible polyimide film. The circular-shaped device bottom gate (Ti/Au 1 nm/40 nm) with a diameter of 150 μm was thermally evaporated onto the polyimide film through a shadow mask. Then, a 15-nm-thick Al_2O_3 gate dielectric layer was deposited on top of the bottom gate using ALD. Next, few-layer BP flakes (10 nm thick) were mechanically exfoliated from bulk BP crystals onto the Al_2O_3 capped

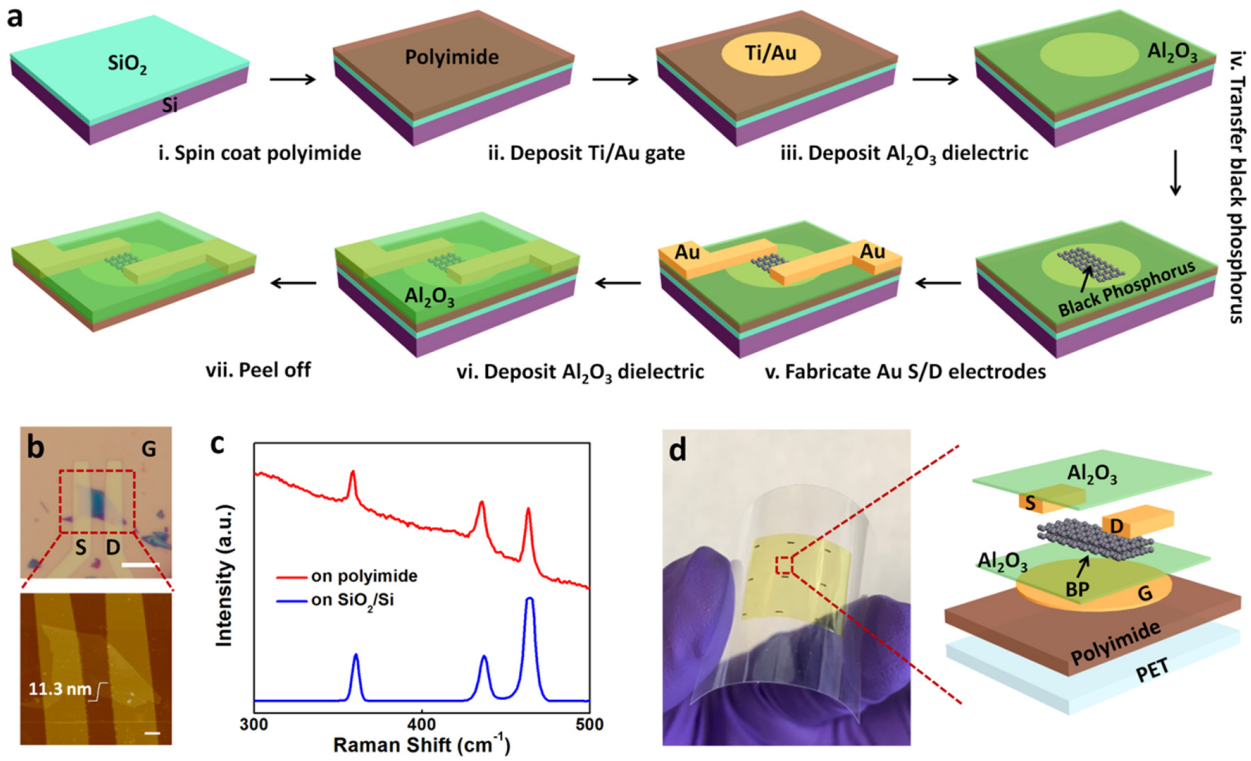

Figure 4.1 Flexible BP FET on polyimide substrate. (a) Schematic flow chart illustrating the fabrication process for a flexible BP FET on polyimide substrate. (b) Optical microscope and AFM images of a representative BP FET on polyimide film. The BP flakes used in the work have a thickness of 10 nm. The scale bar is 5 and 1 μm for the optical microscope and AFM images, respectively. (c) Raman spectra taken from BP flakes on polyimide (red) and silicon (blue) substrates. (d) Photograph of flexible BP FETs attached on a transparent PET handling substrate in its bending state. The schematic in the right inset shows the exploded view of the flexible BP FET structure.

bottom gate electrodes. A 50-nm-thick Au S/D electrodes were subsequently patterned onto the BP flake by EBL, metal evaporation, and lift-off processes. Another 10-nm-thick Al_2O_3 dielectric was grown by ALD to fully encapsulate the BP FET. Once the device fabrication was completed, the polyimide film was delaminated from the silicon handling wafer to obtain the flexible BP FETs on polyimide film. Figure 4.1b shows the optical microscope and AFM images of a representative BP FET fabricated on polyimide substrate. The Raman spectra collected from BP flakes on polyimide (red) and silicon (blue) substrates are presented in Figure 4.1c. Three distinct peaks can be observed at 360, 436, and 463 cm^{-1}, corresponding to the $A_g{}^1$, B_{2g} and $A_g{}^2$ phonon modes of few-layer BP flake. The Raman spectra baseline

for BP flake on polyimide film was slightly tilted compared with the one on silicon substrate. Moreover, we found it was very easy to get burned for the BP flakes on polyimide film during the Raman measurement (Figure 4.2), which is likely due to the significantly lower thermal conductivity of polyimide (0.2 $Wm^{-1}K^{-1}$) compared with silicon (150 $Wm^{-1}K^{-1}$).[139] The heat generated by the laser (λ=532 nm) of the Raman system was difficult to be quickly dissipated through the polyimide film, causing the BP flakes to be burned. So, we reduced the laser intensity during Raman measurement. Figure 4.1d shows the photograph of flexible BP FETs attached onto a transparent PET film being bent. The PET film is used as a handling substrate for the flexible BP device characterization and bending test.

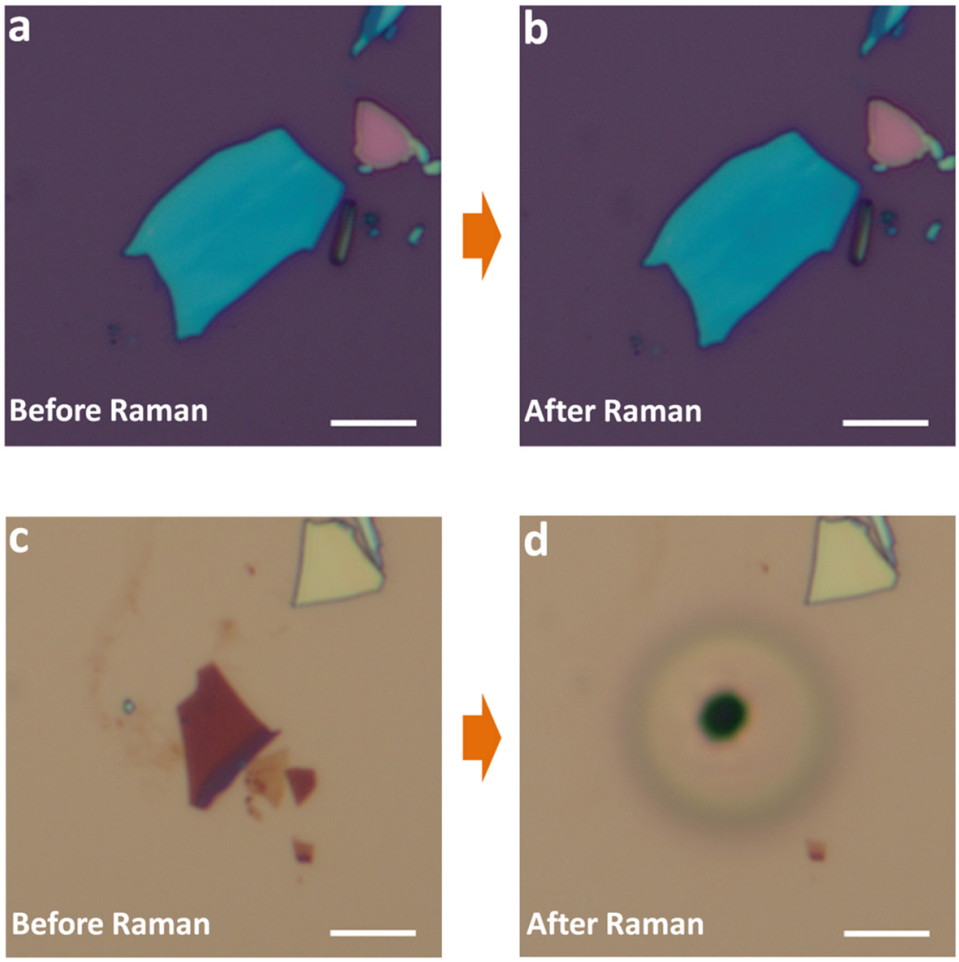

Figure 4.2 Optical microscope images of BP flake on silicon substrate before (a) and after (b) Raman measurement. Optical microscope images of BP flake on polyimide film before (c) and after (d) Raman measurement. The scale bar is 5 μm.

4.3 Negative Photoconductivity in Flexible Black Phosphorus Photodetectors

To fully elucidate the effect of the substrate, we compare the photoresponse of a BP device fabricated on the polyimide film before and after being delaminated from its silicon handling wafer. A near-infrared laser diode with a wavelength of λ = 830 nm was used. Figure 4.3 shows the transfer characteristics of a BP FET before being delaminated from silicon handing wafer measured in the dark (blue) and under illumination (red). Under illumination, the device exhibits photoresponse with slight current decrease in the on-state (V_{GS} = -6 V) and large current increase in its off-state (V_{GS} = -3 V). After the polyimide substrate was delaminated from the silicon handling wafer, the same BP FET shows much more predominant current decrease in its on-state (V_{GS} = -6 V) as shown in Figure 4.3b. The photoresponse in the output characteristics of the same device measured at V_{GS} = -5 V before and after polyimide delamination are shown in Figure 4.3c and d, respectively. Above experiment results further demonstrate that the flexible BP FET on freestanding polyimide shows much larger conductance decrease in its on-state (current decreases from 38.7 to 32.0 μA/μm under a laser intensity of 14.9 W/cm^2 before peel off and 50.5 to 21.2 μA/μm after peel off) under laser illumination. Figure 4.3e and f present the photoswitching characteristics of a flexible BP FET on freestanding polyimide substrate under different gate biases. The device shows current increase under illumination when biased in the off-state (V_{GS} = -3 V), as shown in Figure 4.3e. On the other hand, when biased in the on-state (V_{GS} = -5 V), the device current decreases under illumination, as illustrated in Figure 4.3f.

4.4 Positive Photoconductivity in Black Phosphorus on Silicon Substrates

As a comparison, we also studied the photoresponse in BP FETs fabricated directly on the silicon substrate using heaviliy doped silicon and 300-nm-thick SiO_2 as the gate electrode

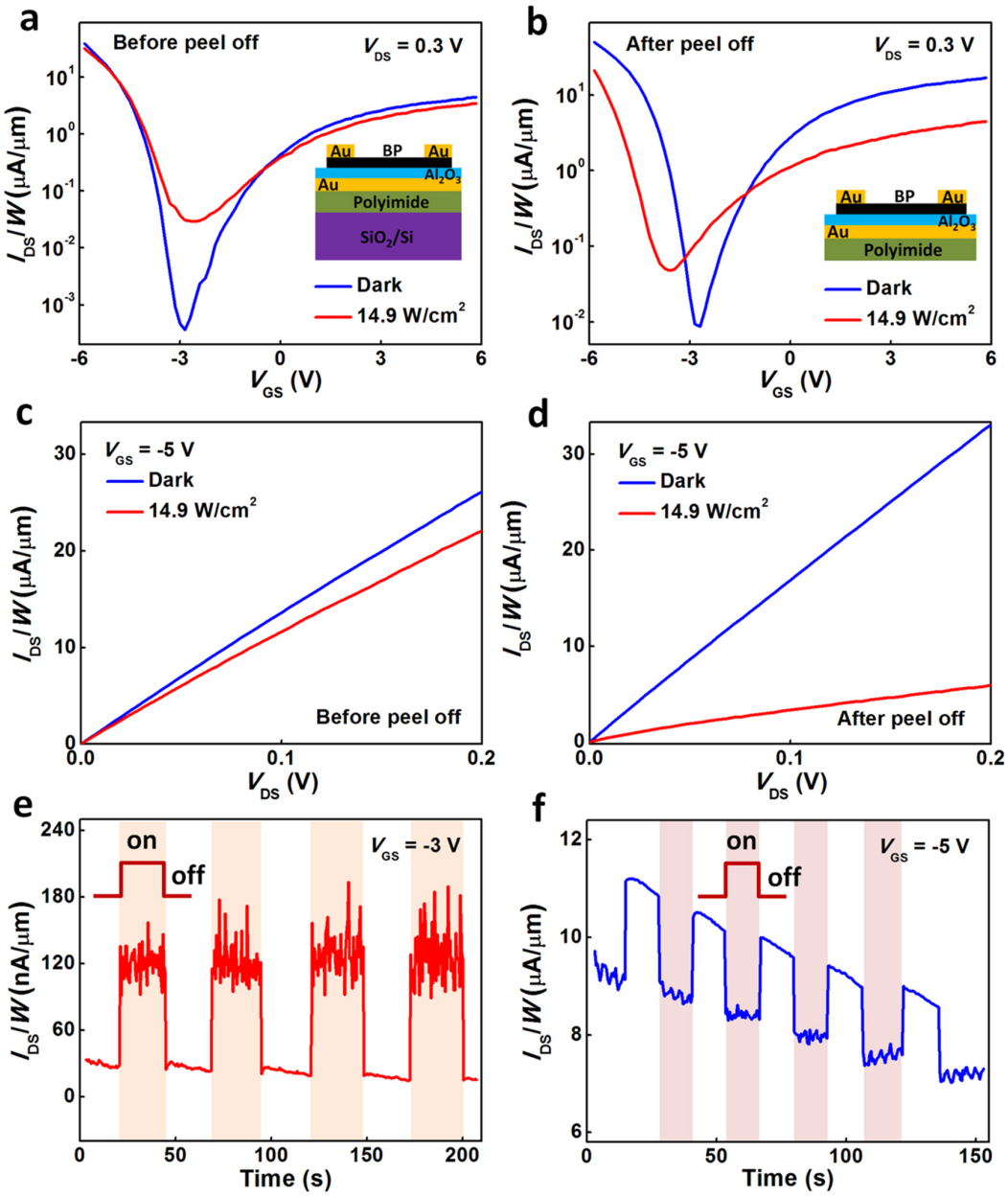

Figure 4.3 Photoresponse of the BP FET built on polyimide substrate. (a, b) Transfer characteristics of a BP FET fabricated on polyimide film before (a) and after (b) being delaminated from the silicon handling wafer measured in dark and under laser illumination. The inset shows the cross section of the device structure. (c, d) Output characteristics of the same device before (c) and after (d) being delaminated from the silicon handling wafer measured in dark and under illumination at a V_{GS} of -5 V. (e) Photoswitching behavior of the delaminated flexible BP FET (measured at V_{DS} = 0.2 V and V_{GS} = -3 V) showing positive photocurrent. (f) Photoswitching behavior of the same delaminated flexible BP FET measured at V_{DS} = 0.2 V and V_{GS} = -5 V showing negative photocurrent.

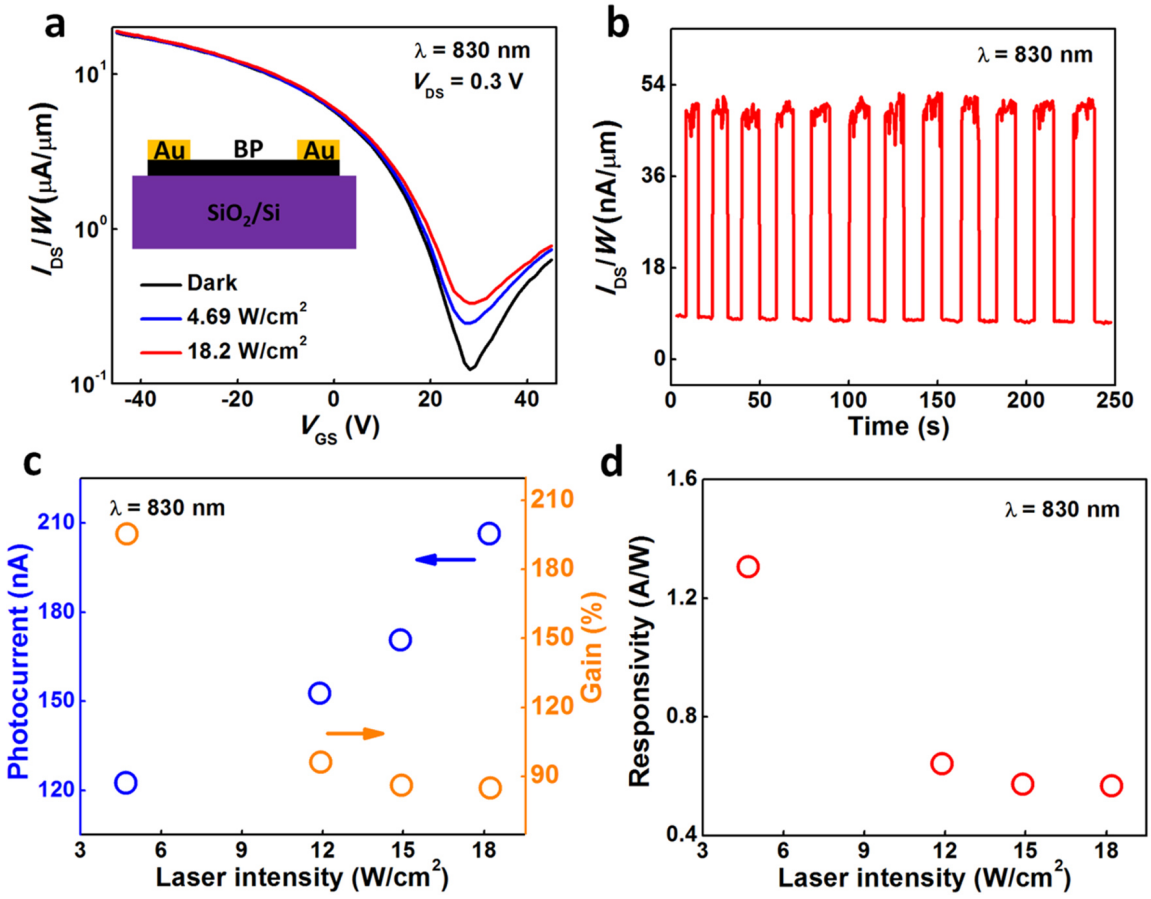

Figure 4.4 (a) Transfer characteristics of BP transistors fabricated on silicon substrate measured under near-infrared laser illumination. (b) Photo-switching characteristics of the same device plotted as a function of time. (c, d) Device photocurrent and photoconductive gain (c) and responsivity (d) plotted as a function of laser intensity.

and gate dielectric, as shown in Figure 4.4. The device transfer characteristics exhibited a monotonic current increase under laser illumination with gate voltage varying from -45 V to +45 V. No current decrease was observed at any gate bias even with laser intensity up to 18.2 W/cm^2. The calculated responsivity is 1.3 A/W at a laser intensity of 4.69 W/cm^2, which is comparable with reported works.[136] Therefore, we can conclude that the substrate plays an important role in the photoresponse of BP FETs. A possible explanation of negative photoconductivity in flexible BP FETs built on polyimide film, the photo-generated heat cannot be effectively dissipated through the substrate due to the low thermal conductivity of polyimide. In such scenario, the photothermal effect becomes dominated, which leads

to enhanced phonon scattering, reduced carrier mobility, and consequently decrease in current. In contrast, for BP devices fabricated directly on the silicon substrate whose thermal conductivity is much larger, the photothermal effect becomes much smaller, resulting in no observable current decrease under illumination.

4.5 Responsivity and Photoconductive Gain in Flexible Black Phosphorus Photodetectors

To further investigate the photoresponse in the flexible BP FET on freestanding polyimide film, we examined the light intensity dependent I-V characteristics. Figure 4.5a shows the transfer characteristics of a delaminated flexible BP FET under illumination with increasing laser intensities from 0 to 16.5 W/cm^2. The device current increases with increasing laser intensity when it is in the off-state (V_{GS} = -1 V). On the other hand, the incident laser results in significant current decrease when device is in the on-state (V_{GS} = -4 V). The output characteristics measured at V_{GS} = -4 V (Figure 4.5b) further demonstrate the decrease of on-state current under illumination. Figure 4.5c plots the device conductance (G = I/V) as a function of laser intensity indicating a drastic decrease with increasing laser intensity. The negative photoconductivity in flexible BP FETs is attributed to photothermal effect - a rise in device temperature upon light irradiation, as discussed previously.[140, 141] According to semiconductor physics, temperature rise would generate more free carriers in semiconductors due to thermal excitation, while also suppress the carrier mobility due to enhanced phonon scattering.[27] These two opposite factors in combination determine the device conductivity.

When the flexible BP FETs are in the off-state, the channel is depleted and the carrier concentration is very low. As a result, the increase in carrier concentration at elevated temperatures induced by photothermal effect would have a more predominant contribution to the conductivity than the reduction in carrier mobility. Under more negative gate biases when the BP device is fully turned on, the carrier concentration is very high and the device

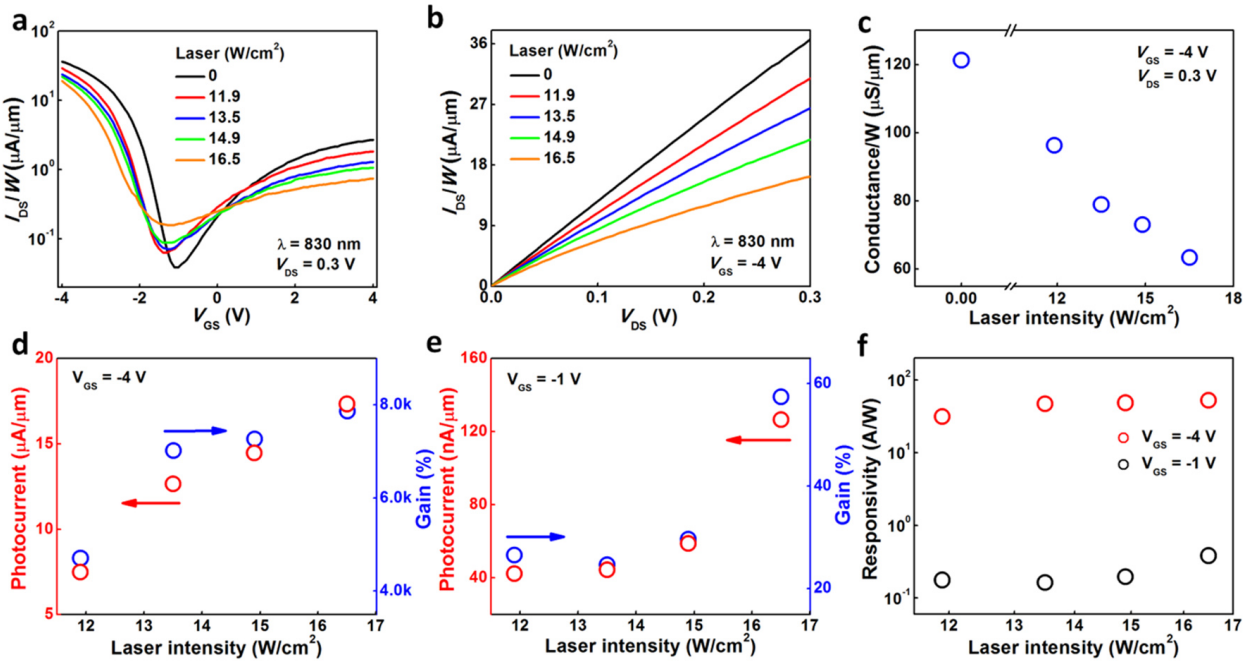

Figure 4.5 Light intensity dependent photoresponse in BP FETs on freestanding polyimide substrate. (a, b) Transfer (a) and output (b) characteristics of a BP FET after being delaminated from silicon handling wafer measured in dark and under laser illumination with various intensities. (c) Device conductance extracted from panel a plotted as a function of laser intensity. (d, e) Device photocurrent and photoconductive gain plotted as a function of laser intensity when the gate bias is set to be V_{GS} = -4 V (d) and V_{GS} = -1 V (e). (f) Comparison of device responsivity when it is biased at V_{GS} = -4 V and -1 V.

conductivity will be dominated by the factor of the reduced carrier mobility at elevated temperatures. Figure 4.5d and e present the photocurrent and photoconductive gain of flexible BP FET with gate voltage of V_{GS} = -4 (on-state) and -1 V (off-state), respectively. The device shows distinct photocurrent and photoconductive gain of 17 μA/μm and 8,000% in its on-state (V_{GS} = -4 V). However, in its off-state (V_{GS} = -1 V), the device photocurrent and photoconductive gain are only 0.13 μA/μm and 57%. The responsivity of a photodetector can be defined as R = I_{ph}/(PA), where I_{ph} is the net photocurrent, P is the incident laser power, and A is the effective area of the detector. Figure 4.5f shows the comparison of responsivity when the device is biased at V_{GS} = -4 and -1 V, respectively. The device on-state responsivity (red cycle) induced by photothermal effect is orders of magnitude higher than the off-state one (blue cycle) induced by photogenerated carriers. More importantly, the

responsivity is also significantly higher than other reported work on BP photodetectors.

4.6 Temperature-Dependent Electrical Performance of Flexible Black Phosphorus Photodetectors

Flexible BP FETs on freestanding polyimide film exhibit significant conductance decrease under near-infrared laser illumination. We attributed such photoresponse with negative photocurrent to the photothermal effect induced mobility reduction.[140, 141] To further support that the photothermal effect is indeed the underlying mechanism, we study the transfer and output characteristics when the device is heated to various temperatures using a Peltier heater. The BP device used here for the temperature study is the exact same device used in Figure 4.5 for the photoresponse measurements. The temperature study in Figure 4.6 was carried out before the photoresponse measurements in Figure 4.5 so the device on polyimide was still attached on the silicon handling wafer (before delamination) and can be easily attached onto the Peltier heater during heating. As the substrate temperature changes from 293 K to 373 K with a step of 20 K, the device shows similar on-state current decrease (V_{GS} = -4 V) with increasing substrate temperature, as shown in Figure 4.6a and b.

Compared with Figure 4.5a and b, the variation in both transfer and output characteristics induced by temperature is very similar to the ones induced by laser illumination. Figure 4.6c shows the field-effect mobility in BP FET as a function of substrate temperature. The mobility is extracted from the transfer characteristics in Figure 4.6a in the V_{GS} range from -2 to -4 V. An increase in temperature will result in mobility degradation in BP FETs because the phonon scattering becomes the dominant scattering mechanism at high temperatures. In the phonon-limited high temperature regime, the mobility is expected to follow a $\mu \sim T^{-r}$ temperature dependency.[27] We fit the curve in Figure 4.6c using the generic temperature dependency of the mobility $\mu \sim T^{-r}$, where the exponent depends on the phonon scattering mechanism.[27] From the fitted curve we find the value of r to be around 1.56. We also

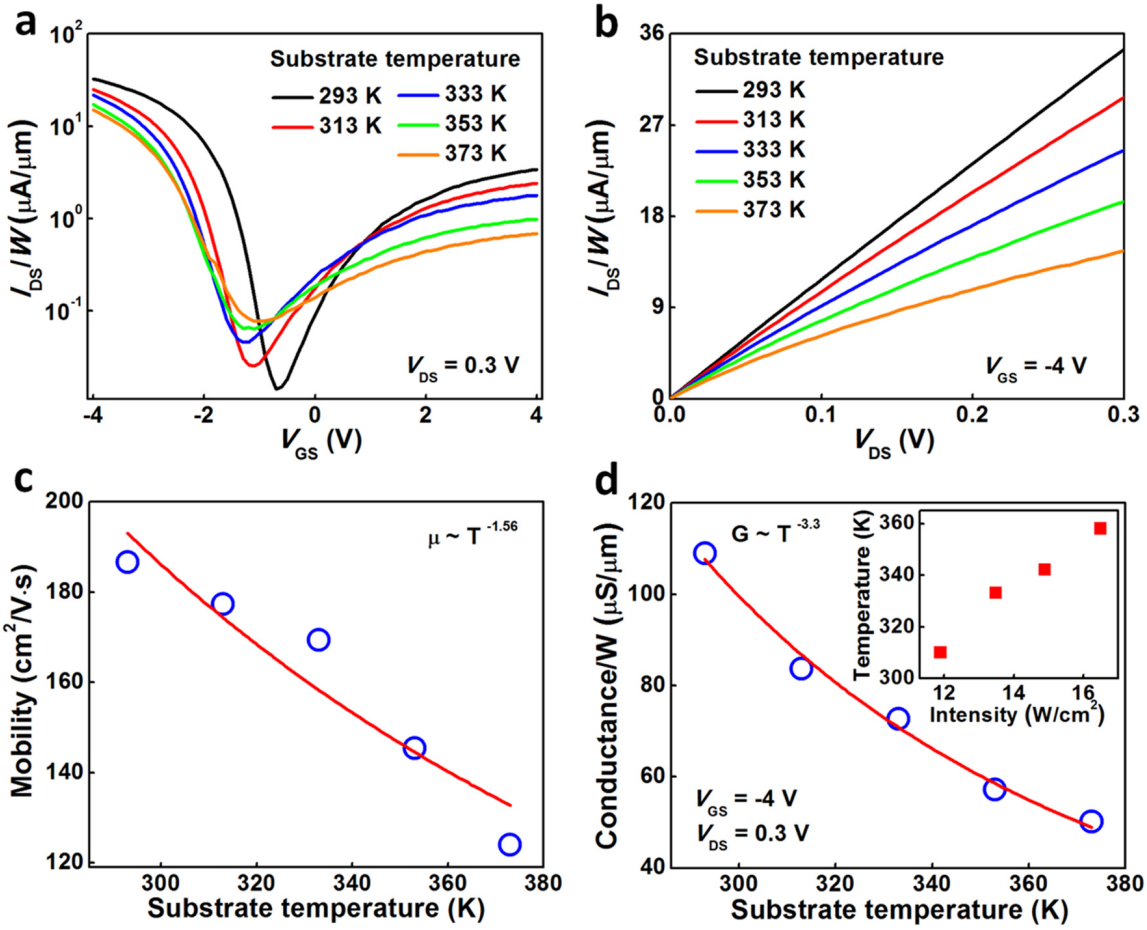

Figure 4.6 Temperature-dependent electrical characteristics of the flexible BP FETs. (a, b) Transfer (a) and output (b) characteristics of the same BP FET shown in Figure 4.5 before being delaminated from the silicon handling substrate measured at different substrate temperatures. (c) Device mobility at different substrate temperatures (293 K, 313 K, 333 K, 353 K, and 373 K). (d) Device conductance extracted from panel a plotted as a function of substrate temperature. The inset shows the deduced relationship between the incident laser intensity and device substrate temperature.

examine the temperature dependency of device conductance (G) using similar equation $G \sim T^r$, as shown in Figure 4.6d. The fitted curve gives a r value of around 3.3. As can be seen, the exponent ($r \sim 3.3$) for the temperature dependency of conductance is larger than the one for mobility. The main reason is that besides mobility, the device conductance is also dependent on carrier concentration, which is also temperature dependent, and other factors such as Au/BP contacts, charged impurities, and surface roughness.

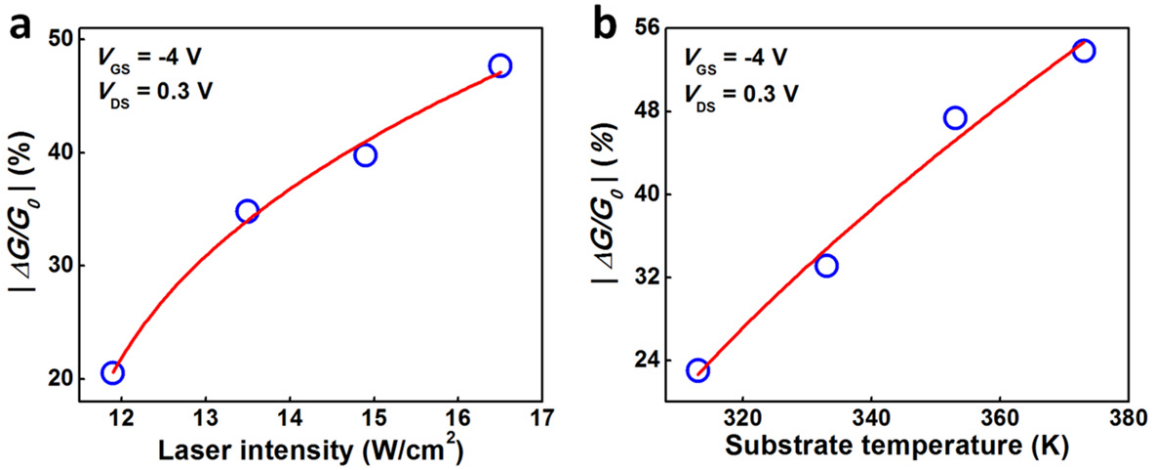

Figure 4.7 (a) Relative conductance change plotted as a function of laser intensity after the BP device is delaminated from the silicon handling wafer. (b) Relative conductance change of the same BP device plotted as a function of substrate temperature when it was still attached on silicon handling wafer. A Peltier heater was used the heat up the device from 293 K to 373 K.

The relationship between the device substrate temperature and incident laser intensity can also be obtained if we compare Figure 4.6d with Figure 4.5c. The inset in Figure 4.6d shows the extracted device substrate temperature as a function of laser intensity, indicating an almost linear relationship. One can find that the temperature of the polyimide substrate increases from 310 K to 358 K as the laser intensity is increased from 11.9 W/cm^2 to 16.5 W/cm^2. The magnitude of relative change in conductance $\Delta G/G_0$ (where $\Delta G = G\text{-}G_0$, G is the instantaneous conductance of the device and G_0 is the conductance of the device at room temperature or dark condition) plotted as a function of laser intensity is shown in Figure 4.7. The laser illumination and temperature exert almost the same effect on the

device conductance.

4.7 Device Simulation Using Sentaurus TCAD

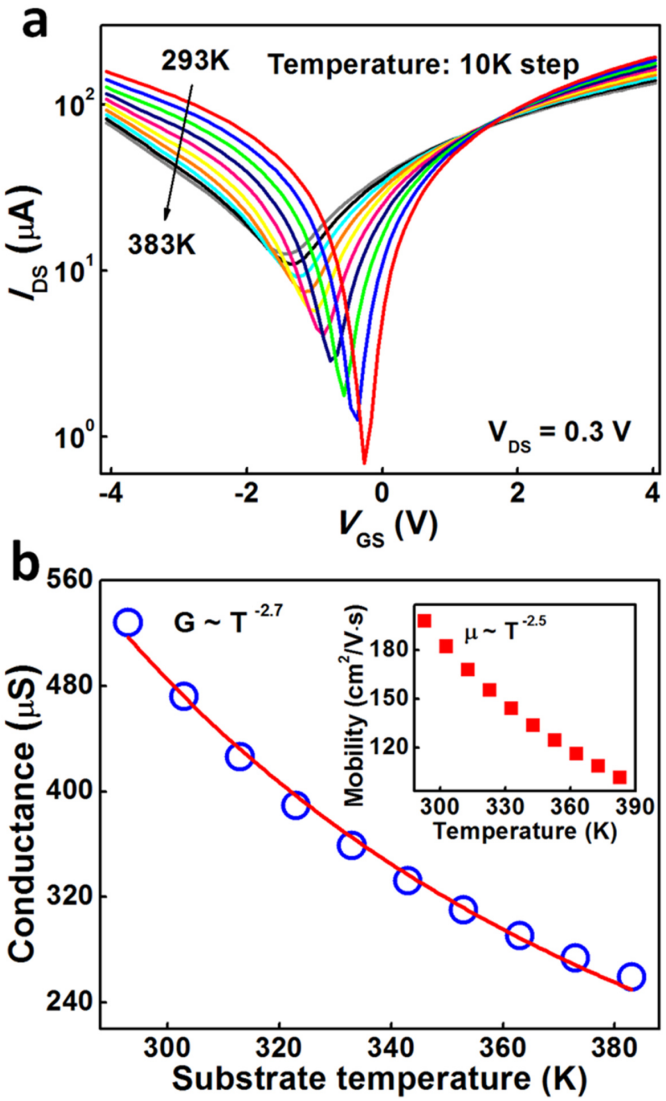

Figure 4.8 Device simulation results using Sentaurus TCAD. (a) Simulated transfer characteristics of a BP FET plotted as a function of substrate temperatures ranging from 293 K to 383 K in 10 K step. (b) Device conductance extracted from the transfer curves at V_{GS} = -4 V and V_{DS} = 0.3 V plotted as a function of substrate temperature. The inset shows the temperature-dependent mobility, where the exponent depends on the dominant scattering mechanism.

To further confirm that the substrate heating is the main mechanism governing the neg-

ative photoconductivity in flexible BP FETs, we also carried out detailed device simulation using Sentaurus TCAD. The BP flake used in the simulation has a thickness of 10 nm. Figure 4.8a shows the simulated transfer characteristics of the BP FET with substrate temperature varying from 293 K to 383 K. The simulated BP device shows an ambipolar behavior with room-temperature on-state current of 158 μA at V_{GS} = -4 V and V_{DS} = 0.3 V. The device also shows on-off ratio of more than 10^2 at room temperature, which is comparable to the device from experiments. Increase in substrate temperature leads to decrease in on-state current, which is also consistent with the experimental results. In the simulation, the room-temperature mobility is set to be 186.7 $cm^2V^{-1}s^{-1}$ which is obtained from the experiment. The mobility is set to follow a $\mu \sim T^r$ phonon-limited temperature dependency with r = 2.5. In this scenario, the simulated relative conductance change fully supports our experimental results. Figure 4.8b presents the simulated conductance plotted as a function of substrate temperature. The room-temperature (293 K) conductance of 528 μS (at V_{GS} = -4 V and V_{DS} = 0.3 V) decreases to 259 μS at a substrate temperature of 383 K. We also fit the curve in Figure 4.8b using the temperature dependency of conductance $G \sim T^r$. From the fitted curve, the value of r is found to be 2.7, which is again consistent with experimental result (r = 3.3). From the temperature study and device simulation, we can safely conclude that the negative photoconductivity in flexible BP FETs on freestanding polyimide substrate is caused by the photothermal effect induced by the incident light.

4.8 Bending Test of Flexible Black Phosphorus Photodetectors

BP based electronic and optoelectronic devices also show superior mechanical flexibility due to its layered crystal structure and small thickness. Figure 4.9 and Figure 4.10 show the systematic bending tests conducted on flexible BP devices. The device transfer and output characteristics show negligible variations when bent down to a small curvature radius of 5.9 mm (Figure 4.9a and b) and remain essentially unchanged throughout the process of up to

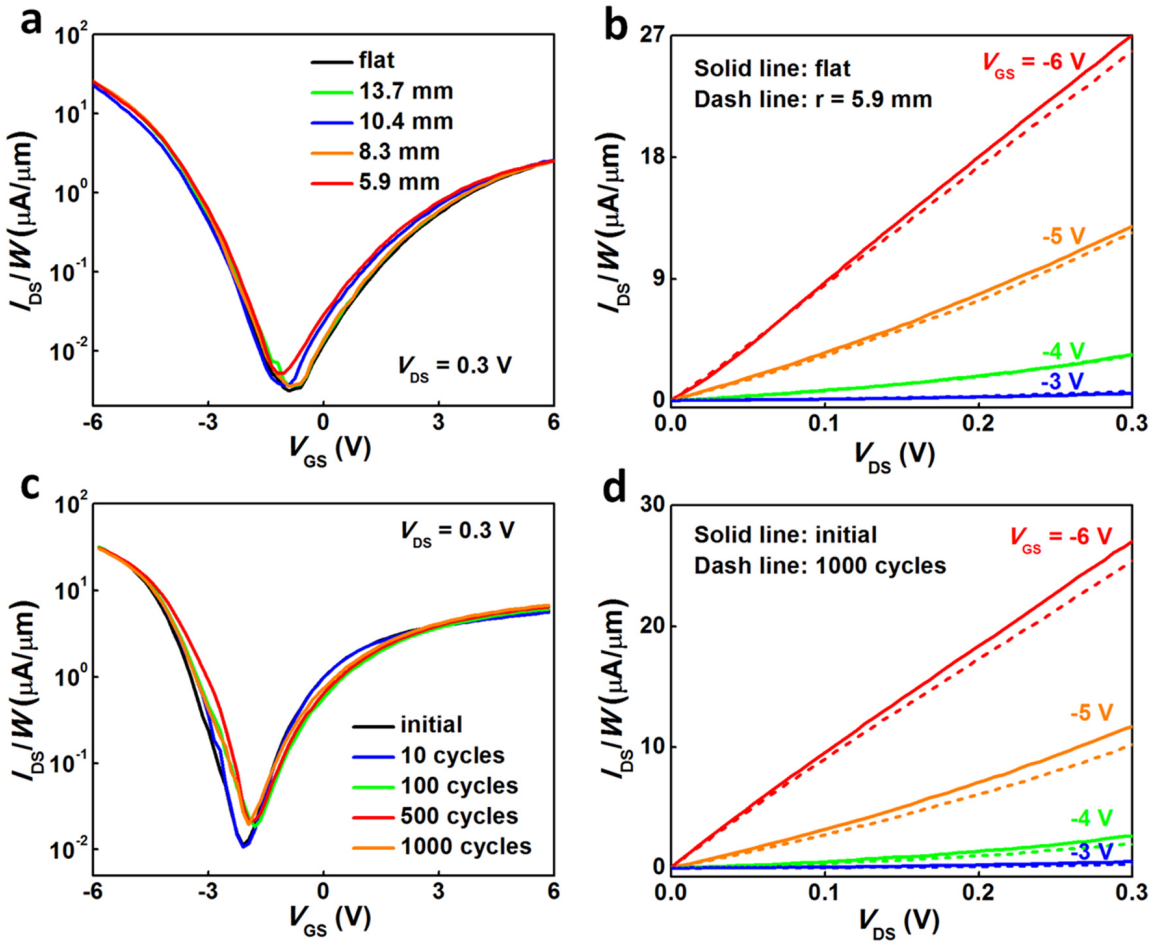

Figure 4.9 (a, b) Transfer (a) and output (b) characteristics of a flexible BP transistor measured at various curvature radii. (c, d) Transfer (c) and output (d) characteristics of another flexible BP transistor measured after various bending cycles.

1000 bending cycles (Figure 4.9c and d).

The device electrical performance metrics, including carrier mobility and on-off ratio are plotted as functions of curvature radius and bending cycle are shown in Figure 4.10a and b. The flexible BP devices shows stable carrier mobility of 150 $cm^2V^{-1}s^{-1}$ and on-off ratio of 6×10^3 when the polyimide substrate was bent down to 5.9 mm curvature radius. Another flexible BP device also exhibits negligible variations in mobility (130 $cm^2V^{-1}s^{-1}$) and on-off ratio (2×10^3) throughout 1000 bending cycles. The excellent stability of our flexible BP FET can be attributed to the mechanical robustness of ultrathin BP flake and ultrathin polyimide substrate used. Next, the device photoresponse during the bending tests

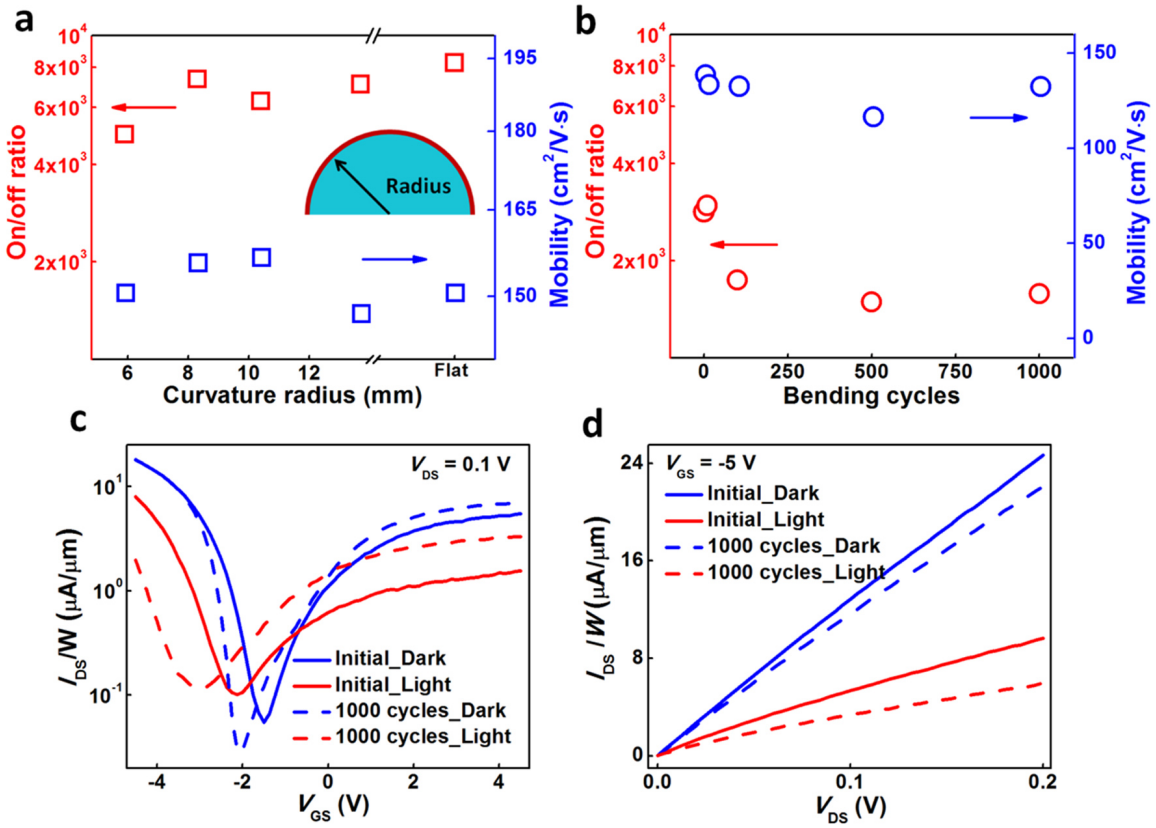

Figure 4.10 Bending test of flexible BP infrared photodetectors. (a, b) FET performance metrics including field-effect mobility and on-off ratio plotted as functions of curvature radius (a) and bending cycle (b). (c, d) Transfer (c) and output (d) characteristics of a flexible BP FET measured in dark and under laser illumination before and after 1000 bending cycles. The solid lines represent the pristine device characteristics and the dashed lines represent the device characteristics after 1000 bending cycles.

was also studied. Because it is very difficult to conduct the near-infrared laser alignment, we only measured the device photoresponse before and after 1000 bending cycles with a curvature radius of 6 mm. The dashed lines in Figure 4.10c and d are the device transfer and output curves measured in dark and under laser illumination after 1000 bending cycles. From the results, one can find that the device also exhibits very minor variations in its photoresponse. The slight difference in photoresponse before (solid line) and after (dashed line) 1000 bending cycles is most likely caused by the infrared laser alignment. Such flexible BP photodetectors with superior robustness under mechanical bending tests associated with superior responsivity can potentially be used as sensing components in future wearable and

bio-integrated imaging systems.

4.9 Single Pixel Black Phosphorus Near-Infrared Camera

Infrared imaging systems have wide range of military or civil applications and 2D nanomaterials have recently emerged as potential sensing materials that may outperform conventional ones such as HgCdTe, InGaAs, and InSb. As an example, 2D BP thin film has a thickness-dependent direct bandgap with low shot noise and non-cryogenic operation for visible to mid-infrared photodetection. In this section, we demonstrate the use of a single-pixel photodetector made with few-layer BP thin film for near-infrared imaging applications. The imaging is achieved by combining the photodetector with a digital micromirror device to encode and subsequently reconstruct the image based on compressive sensing algorithm. Stationary images of a near-infrared laser spot (λ = 830 nm) with up to 64 $\times$ 64 pixels were captured using our single-pixel BP camera with 2000 times of measurements, which is only half of the total number of pixels. The imaging platform demonstrated in this work circumvents the grand challenges of scalable BP material growth for photodetector array fabrication and shows the efficacy of utilizing the outstanding performance of BP photodetector for future high-speed infrared camera applications.

Conventional bulk semiconductors (HgCdTe, InSb, and InGaAs) and novel nanomaterials (0D quantum dots, 1D nanowires, and 2D layered materials) have been used to develop infrared photodetectors with high responsivity, speed, efficiency, and broad detection wavelength. Among all those materials, low-cost 2D materials have attracted great interest for optoelectronic applications because of their excellent optical, electrical, and mechanical properties. 2D BP, a direct bandgap semiconductor, has recently become a promising material candidate for visible to mid-infrared photodetection. Recent studies have demonstrated the ability of low-noise photodetection in BP film with a high responsivity and speed in both visible and infrared regimes. Nevertheless, the challenge that hinders the integration of 2D

material based photodetectors into an infrared image sensor is the difficulty of fabricating large scale photodetector arrays using current bottom-up fabrication techniques. Additionally, techniques for scalable and uniform growth of high-quality 2D semiconductor thin film are not mature enough.

4.9.1 Compressive Sensing Algorithm

In order to take advantage of the extraordinary performance of BP photodetectors for practical infrared imaging applications, we demonstrate the use of a single BP photodetector as an infrared camera using compressive sensing algorithm. Specifically, in our experimental configuration, an infrared image was projected onto a digital micromirror device (DMD) (instead of projecting onto the focal plane sensors in conventional infrared camera), generating predefined pattern according to the measurement matrix of compressive sensing algorithm. The projected image information from DMD will be detected by a BP photodetector and the original image can be recovered by compressive sensing reconstruction algorithm. In this study, infrared laser spot images with 32×32 and 64×64 pixels were successfully captured with only 500 and 2000 times of measurements. This single-pixel imaging technique serves as a proof-of-concept demonstration of using 2D semiconductors for next-generation infrared photodetector and camera applications.

The broadband photodetection and superior photoresponse of BP make it a promising sensing material for photodetectors and imaging systems. However, further progress on large-area material growth/assembly methods and scalable fabrication and integration schemes are required to achieve BP photodetector arrays for imaging applications. In such a scenario, an emerging technique called compressive sensing solves the problem and makes a single BP photodetector based imaging system possible. The main idea of compressive sensing is to capture sparse signal with limited samples which breaks through the limitation of Nyquist-Shannon sampling theorem, and then reconstructs the original image by advanced optimization algorithms.[142, 143, 144, 145, 146, 147, 148, 149]

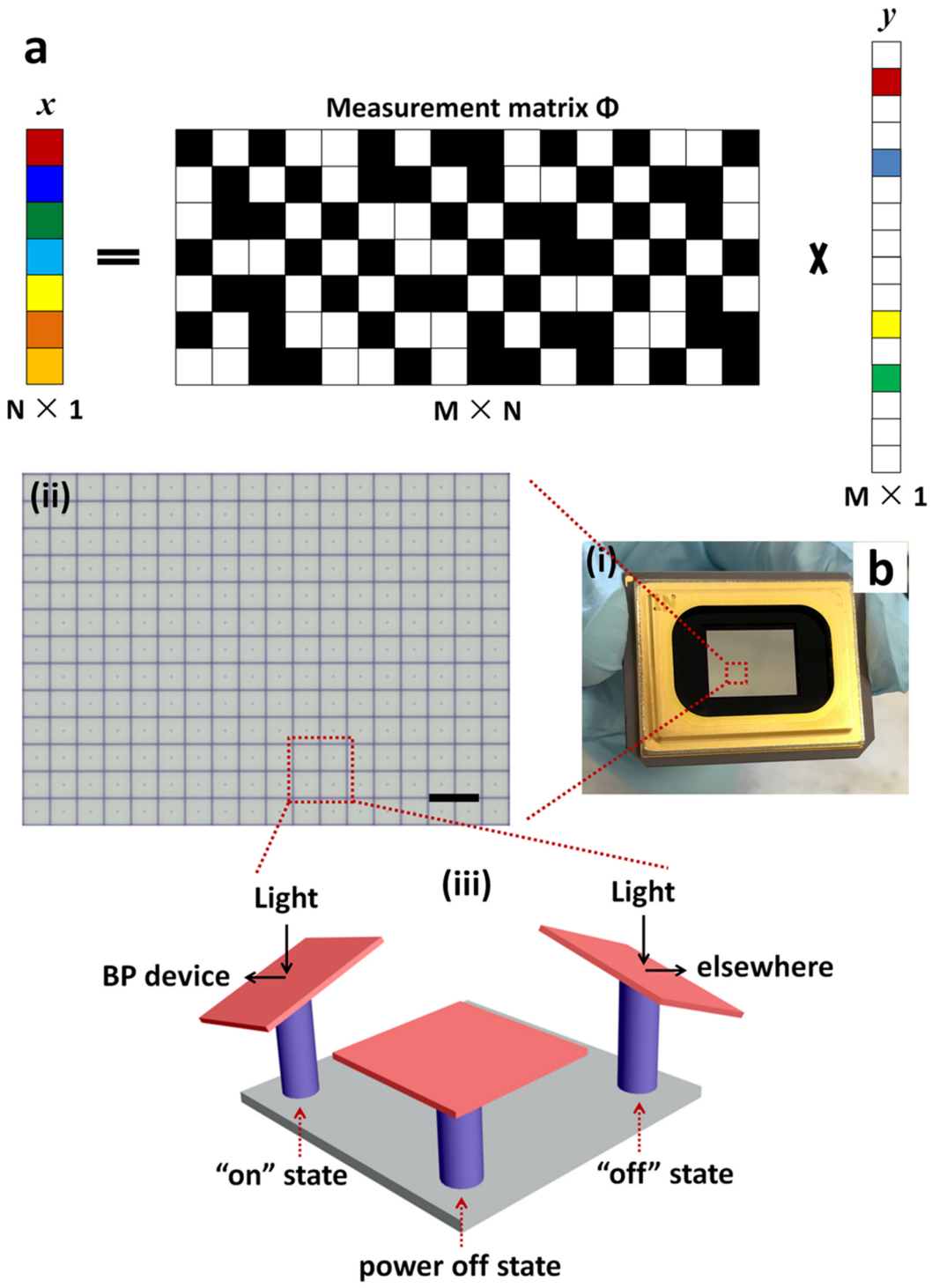

Figure 4.11 Compressive sensing algorithm and the DMD. (a) Schematic illustrating the data sensing based on compressive sensing algorithm. (b) Photograph (i), optical micrograph (ii), and schematic (iii) of a DMD system. The scale bar is 25 μm for the optical microscope image in panel ii. The size of a single micromirror is 12 μm $\times$ 12 μm.

Figure 4.11 shows the detailed schematic and flowchart of compressive sensing algorithm. Given an unknown signal (image), x $\in \Re^n$ if we can find a linear projection $\Phi \in \Re^{mn}$, and a measurable projection result y $\in \Re^m$, a compressive sampling can be achieved by following equation: y = Φx, where Φ is the measurement matrix with a dimension of m $\times$ n. The unknown signal x has the overwhelming probability to be recovered if Φ satisfies restricted isometry property (RIP) condition and x is sparse or could be considered as sparse in some other basis, by following recovery algorithm.[144, 145, 146, 147, 148] In order to apply the compressive sensing algorithm to our single BP photodetector imaging system, we need to build a hardware optical system that can realize the linear projection and measurement simultaneously. In this study, a DMD was used to realize a controllable and programmable measurement matrix and a semiconductor analyzer to physically realize single-pixel BP camera using compressive sensing algorithm.

The DMD (Figure 4.11b) in our BP imaging system is used to generate the measurement matrix Φ and achieve the linear projection. The DMD has 1024 $\times$ 768 micromirrors. As shown in Figure 4.11b, each micromirror is square in shape with a dimension of 12 μm $\times$ 12 μm and stands closely to adjoin mirror arrays with a very small gap and high fill factor. The DMD based imaging system can capture images that are projected onto the DMD screen. Specifically, a predesigned measurement matrix based on compressive sensing algorithm can be implemented by controlling the flip of each single micromirror in the DMD. Since each individual micormirror has two rotation angles (-10 degree and +10 degree), we define the "on" and "off" states of micromirrors as follows. When the micromirror is in the "on" state, the light irradiated on it will be directed to the BP photodetector, while in the "off" state the light that fell onto a micromirror will be reflected elsewhere, as shown in Figure 4.11b (iii). By controlling the "on" and "off" states of each single micromirror, the DMD can generate different patterns that forms a specific measurement matrix.[146, 147, 148]

4.9.2 Experimental Setup for the Single Pixel Near-Infrared Camera

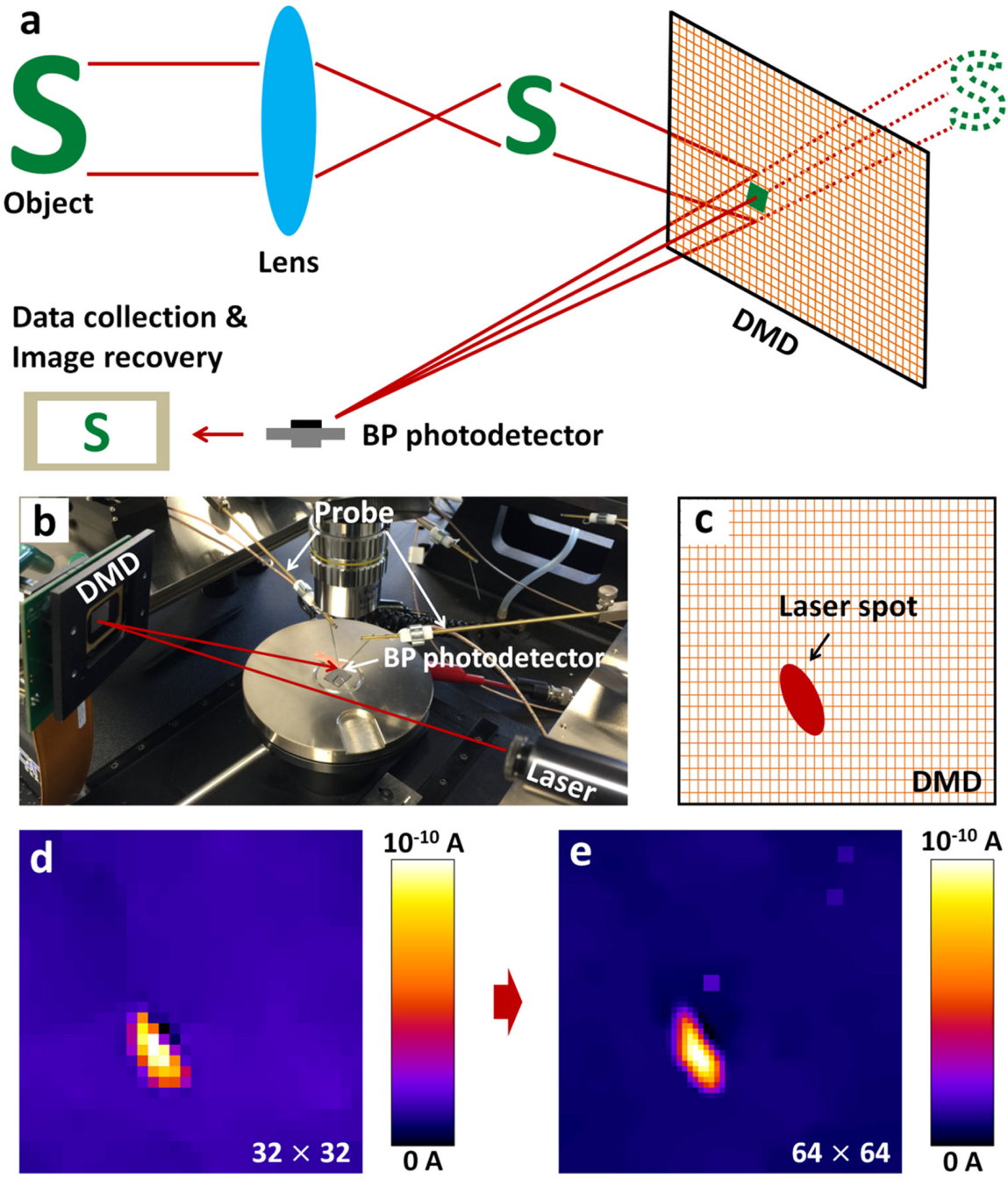

Figure 4.12 Near-infrared camera based on a Single-pixel BP photodetector. (a) Schematic diagrams illustrating the experimental setup for imaging an object. (b) Photograph showing the experimental setup of the single-pixel BP infrared camera. (c) Schematic showing the approximate location of the near-infrared laser spot on DMD screen during the measurement. (d, e) The image captured by the single-pixel BP camera with 32 × 32 (d) and 64 × 64 (e) pixels showing the near-infrared laser spot on DMD.

Figure 4.12a and b show the hardware experimental setup of our single-pixel BP infrared imaging system. Here, a near-infrared laser spot was directed onto a DMD through a set of lenses which have been integrated with the laser source. This laser spot on the DMD can be represented as the original signal (x) we want to capture. The DMD would generate projection patterns according to a predesigned measurement matrix (Φ) by controlling the rotation state ("on" or "off") of each single micromirror. Each projection pattern of the DMD comprised n pixels, and m different patterns were generated to construct the measurement matrix. In other words, the system projects m times of different pattern during the entire measurement process, and as a result, each measurement result from the BP photodetector obtains the inner product between an infrared image and a row of the measurement matrix. The laser spot images were reflected and focused onto a BP photodetector, as shown in Figure 4.12b. The infrared signal arrived at the BP photodetector can be considered as a linear projection from the laser spot image onto a predefined measurement matrix as the inner product of x and Φ. The photocurrent excited by the laser was collected by the semiconductor parameter analyzer. We recorded amplitudes of photocurrent as y. Once all the photocurrent data were collected, the infrared images were reconstructed by a compressive sensing image recovery algorithm (minimum total variation normal algorithm).

We first obtained an infrared image (schematic laser spot in Figure 4.12c) with a low resolution of 32 $\times$ 32 pixels (Figure 4.12d) to adjust the alignment and focus of the system. After that, an infrared image with a higher resolution of 64 $\times$ 64 pixels was captured. Traditional cameras require over 4000 measurements in order to obtain an image with 64 $\times$ 64 pixels, while our BP camera can recover the image with only 2000 times of measurements. The time for capturing an infrared image with a resolution of 32 $\times$ 32 or 64 $\times$ 64 pixels is 250 or 1000 seconds. The image with 64 $\times$ 64 pixels correspond to 1024 $\times$ 768 micromirrors, thus each pixel contains 192 micromirrors. It is worth noting that, the measurement matrix we used in this study is designed according to random Bernoulli distribution, which had a large probability of satisfying the RIP condition. The image was recovered via following

minimizing the total variation norm (TV-norm). Minimizing of TV-norm can make the intensity difference between neighboring pixels sparse, thus smoothing the images.[146, 147, 148, 149]

4.10 Summary

In summary, layered BP film is a direct bandgap semiconductor with tunable gap changing with 0.3 eV to 2 eV. So, it can be used as visible and infrared photodetection material. Here we have demonstrated flexible BP infrared photodetectors with high responsivity of around 53 A/W and gain of around 8,000% at room temperature. Such high responsivity is achieved due to the use of polyimide substrate with low thermal conductivity, which results in strong photothermal effect and substrate heating upon light illumination. The photo-generated heat leads to enhanced phonon scattering and mobility degradation, which generate significant negative photocurrent of 20 to 30 μA under infrared laser illumination (16.5 W/cm^2). To further elucidate the underlying mechanism governing the negative photoconductivity in flexible BP FETs, temperature study and detailed device simulation using Sentaurus TCAD were performed. The results confirm that the increase in substrate temperatures leads to almost the same device conductance decreases, which further demonstrate that the negative photoconductivity in flexible BP FETs is caused by heating effect. This works provides insights on understanding photothermal effect in photodetectors built on low thermal conductivity substrate and may also lead to novel high-sensitivity broadband wearable and bio-integrated photodetectors or imagers. To take advantage of the outstanding photoresponse of BP and overcome the difficulties of BP film growth and scalable photodetector array fabrication, a near-infrared camera based on a single BP photodetector was developed using the compressive sensing algorithm. We have demonstrated that by directing the original infrared image onto a DMD that projects the image onto the BP photodetector, the original infrared image can be decoded and reconstructed from the current signal collected

by the BP photodetector. For our single-pixel BP camera, the sampling rate of image acquisition is much smaller than the Nyquist rate. Infrared laser spot images with 32×32 and 64×64 pixels were successfully captured with only 500 and 2000 times of measurements. This work demonstrates the efficacy of using 2D black phosphorus based photodetector for practical infrared imaging applications.

CHAPTER 5

VERTICALLY STACKED AND SELF-ENCAPSULATED HETEROSTRUCTURE DIODES USING TWO-DIMENSIONAL LAYERED SEMICONDUCTORS

Van der Waals heterojunctions using 2D semiconducting materials could overcome the defect issues included by lattice mismatch in conventional epitaxially-grown heterojunctions with bulk materials and could enable a much wider palette for choice of materials and more sophisticated device design. Such 2D heterojunction devices are of great interest for important functional devices such as diodes, bipolar junction transistors, light-emitting diodes, and photodetectors. In this chapter, we demonstrate a truly vertical p-n heterojunction diode built from 2D semiconductors (MoS_2 and BP) and compare its performance against conventional lateral 2D heterojunction devices. Both vertical and lateral p-n heterostructure diodes exhibit strong rectification ratio even with no gate voltage applied. More importantly, the results show that the vertical diode delivers 70 times higher current density under forward bias than a conventional lateral device design and the improved device performance can be attributed to the complete elimination of series resistance. Low-temperature measurements and TCAD simulations are used to determine the barrier height at the junctions. Moreover, the vertical device structure allows certain ambiently unstable 2D semiconductors to be fully encapsulated by the materials on top, preventing the material from degradation. This work provides new insight into the vertically stacked 2D semiconductors for future nanoelectronic and optoelectronic devices with optimal performance.

5.1 Introduction

Semiconductor p-n junction is one of the fundamental building blocks for many important devices, such as bipolar junction transistors, light-emitting diodes, photodiodes, and solar

cells, etc. In conventional p-n heterojunctions, lattice mismatches may result in defects when epitaxially growing an n-type semiconductor on another p-type semiconductor.[150] However, by using layered 2D semiconductor materials, atomically sharp van der Waals p-n heterojunctions without defect issues can be easily achieved by assembling dissimilar 2D materials together.[151] Recently, a number of researchers have reported various 2D material heterostructures including BP/MoS_2,[152, 153] WSe_2/MoS_2,[154, 155, 156, 157] graphene/WSe_2,[158, 159] WSe_2/$SnSe_2$,[160] and graphene/MoS_2,[161, 162, 163] etc. Electrical transport measurements on those 2D heterostructure p-n junction devices consistently show diode-like rectifying behaviors with high rectification ratio. Others also reported quasi-vertically integrated heterostructures of 2D materials for p-n diodes, photodetectors, and inverters.[164, 165, 166] However, by carefully evaluating the device structure in all previously reported work, one can see that the devices are rarely truly vertical. Those heterojunctions are not strictly vertically stacked together because there is always a lateral 2D material channel outside the overlapped heterojunction region that is also involved in the current transport between the source/drain electrodes. Since the lateral region may contribute to very significant series resistance, it will greatly reduce the device output current. This is especially true when no gate voltage is applied. Moreover, for some sensitive 2D materials such as BP that are unstable in ambient conditions, a lateral heterostructure will have part of the material exposed and the device will inevitably degrade rapidly in ambient conditions.[19]

In this section, we report a device structure for achieving truly vertical 2D van der Waals p-n heterojunction diode using BP and MoS_2. Our design completely eliminates the series resistance that is ubiquitous in conventional lateral 2D heterostructues, which enables us to achieve up to 70 fold improvement in device forward current density. Furthermore, the vertical device design allows sensitive 2D materials that are susceptible to degradation under ambient conditions such as BP to be fully encapsulated by another chemically stable 2D material on top. Experimental results confirm that the vertical BP/MoS_2 heterojunction diodes

demonstrated in this work can preserve its electrical characteristics even after being store in ambient for extended periods of time. Such vertical 2D van der Waals heterostructure could be a viable approach for achieving high performance 2D semiconductor devices including photodetectors and heterojunction bipolar transistors.

5.2 Vertical Heterostructure Diode Fabrication Process

The fabrication procedure for the vertically stacked BP/MoS_2 p-n junction diode is schematically illustrated in Figure 5.1a. In brief, EBL was used to pattern a square opening (4×4 μm^2 or 5×5 μm^2) on a silicon wafer with a 50-nm-thick SiO_2 dielectric layer. Buffered oxide etch solution (NH_3F: HF (6:1)) was subsequently used to etch away the entire SiO_2 layer inside the opening, leaving behind a square trench on the wafer. A 50-nm-thick Au film deposited by thermal evaporation was used to fill the square trench followed by lift-off to form the bottom electrode (Figure 5.1a(i)). The Au electrode and the heavily doped silicon substrate form very good Ohmic contact, as confirmed by the linear I-V relationship with very small resistance (57 Ω). Few-layer p-type BP flake was then transferred onto the as-fabricated bottom electrode (Figure 5.1a(ii)). To achieve p-n junction diode, an n-type MoS_2 flake was dry-transferred onto the BP flake using polydimethylsiloxane (PDMS) as the supporting substrate. The MoS_2 flake fully covers the BP (Figure 5.1a (iii)) and due to van der Waals interactions, BP/MoS_2 heterojunctions can be formed at the overlapped regions. Finally, the top electrode was patterned onto the MoS_2 flake by EBL and thermal evaporation of 50-nm-thick Au film (Figure 5.1a (iv)). In such a device, the current can flow between the bottom Au/silicon electrode and the top Au electrode through the semiconducting BP/MoS_2 heterostructure (Figure 5.1a (v)). Figure 5.1b shows the optical microscope images of a representative vertical BP/MoS_2 p-n junction diode after each fabrication step. The total active cross-sectional area of the device is determined by the overlapping area, which is just the size of the bottom electrode (4×4 μm^2 or 5×5 μm^2).

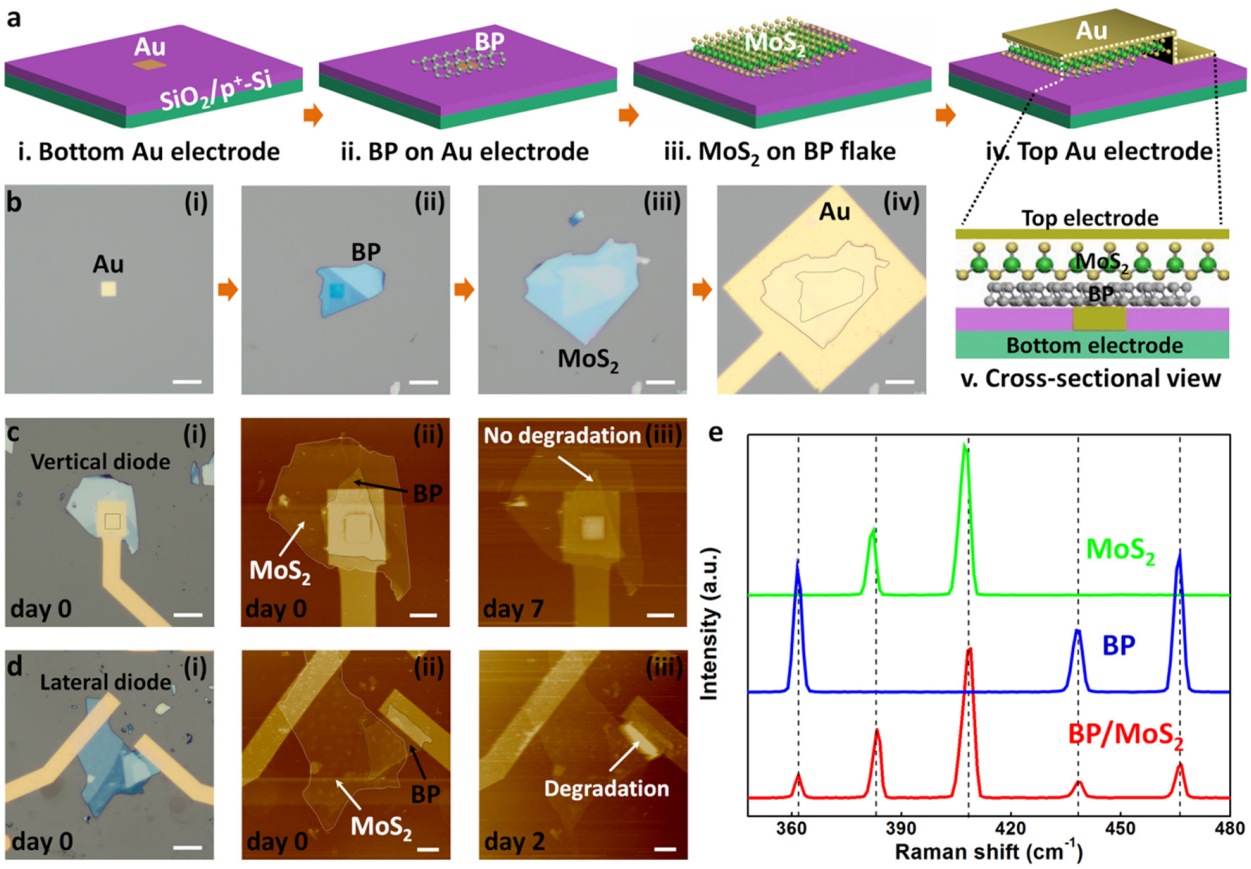

Figure 5.1 Fabrication procedure and characterization of vertically and laterally stacked BP/MoS_2 heterojunction p-n diodes. (a) Schematic diagrams illustrating the fabrication procedure of vertically stacked BP/MoS_2 p-n diodes. (b) Optical microscope images showing a representative vertical BP/MoS_2 p-n junction diode after each fabrication step. Scale bar: 10 μm. (c, d) Ambient stability study of (c) vertically and (d) laterally stacked BP/MoS_2 diodes. The scale bar for panels c (i) and d (i) is 10 μm. The scale bar for panels c (ii), (iii) and d (ii) and (iii) is 5 μm. (e) Raman spectra of MoS_2, BP, and BP/MoS_2 heterostructure.

One advantage of such truly vertical device structure is that it allows the material that might be susceptible to degradation under ambient condition to be fully encapsulated. Specifically for the device in this work, the BP surface which is known to degrade rapidly in air is fully sealed by the MoS_2 layer and Au electrode on top. Figure 5.1 and 5.2 compare the ambient stability of vertically and laterally stacked BP/MoS_2 p-n junction diodes. For the vertical p-n diode, no degradation was observed after 7 days of ambient exposure because the BP flake was fully sealed by the few-layer MoS_2 flake. In contrast, for a lateral p-n diode, the unprotected part of the BP flake underwent significant degradation after being

stored in ambient condition for merely 2 days. One can see that the few-layer MoS_2 can effectively protect sensitive BP material from ambient degradation. Figure 5.1e presents the Raman spectra of MoS_2, BP, and BP/MoS_2 heterostructure. The observed Raman-active modes of MoS_2 (green line) and BP (blue line) are consistent with previously reported work. The peaks from both MoS_2 and BP can be observed in the BP/MoS_2 overlap region (red line) indicating good film quality in the heterostructure after adhesive tape exfoliation and PDMS dry-transfer.

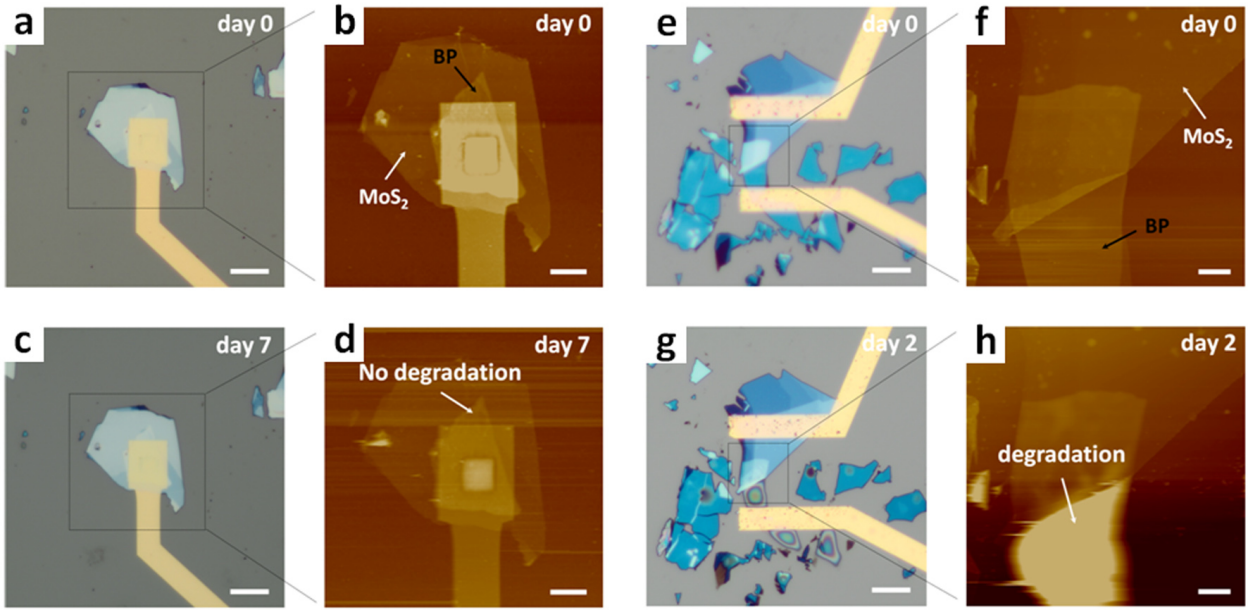

Figure 5.2 (a) Optical microscope and (b) AFM images of a fresh vertical BP/MoS_2 heterojunction p-n diode. (c) Optical microscope and (d) AFM images of the same device after being stored in ambient condition for 7 days. Scale bar: 10 μm for panels a and c; 5 μm for panels b and d.(e) Optical microscope and (f) AFM images of a fresh lateral BP/MoS_2 heterojunction p-n diode. (g) Optical microscope and (h) AFM images of the same device after being stored in ambient condition for 2 days. Scale bar: 10 μm for panels e and g; 2 μm for panels f and h.

5.3 Diode Electrical Performance

Electrical measurements were carried out under ambient conditions and at room temperature to compare the vertically stacked devices with different channel materials such as BP, MoS_2,

and BP/MoS_2 heterostructure (Figure 5.3).

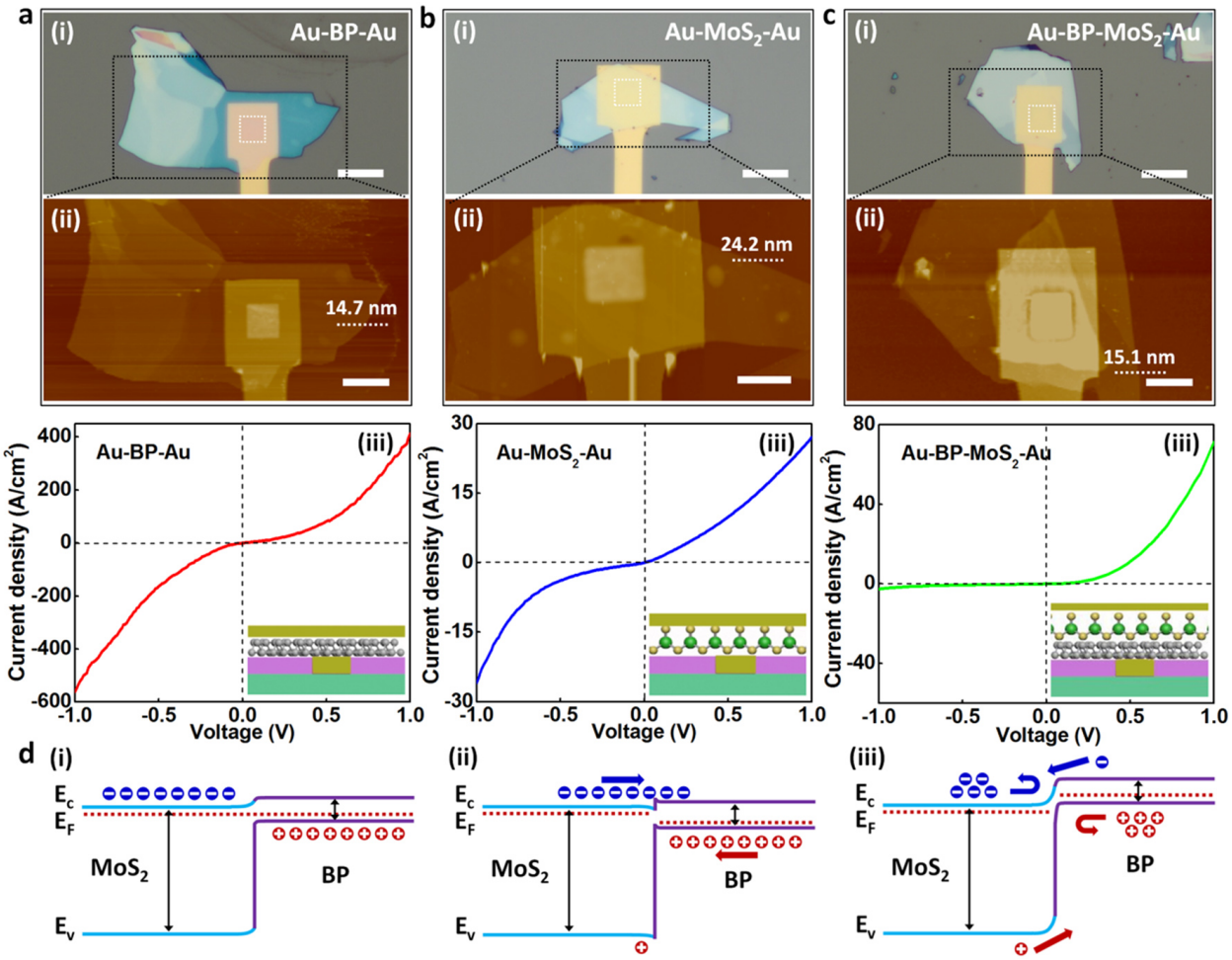

Figure 5.3 Comparison of vertically stacked devices with BP, MoS_2, and BP/MoS_2 heterostructure. Optical microscope images, AFM images, and electrical characteristics of (a) Au-BP-Au, (b) Au-MoS_2-Au, and (c) Au-BP-MoS_2-Au vertically stacked devices. The scale bar for panels a (i), b (i), and c (i) is 10 μm. The scale bars for panels a (ii), b (ii), and c (ii) are 7 μm, 5 μm, and 5 μm, respectively. (d) Schematic energy band diagrams of the BP/MoS_2 heterojunction with (i) zero bias, (ii) forward bias, and (iii) reverse bias.

We first compare the output characteristics of the three types of vertical devices with no external gate voltage applied. The current is normalized by the area of the bottom electrode to obtain the current density. In order to achieve decent current density without gate voltage, relatively thick MoS_2 or BP flakes ($\sim$ 10 nm) were used as the channel materials. Since the MoS_2 or BP film thickness is larger than the out-of-plane screening length of $\sim$ 10 nm, in this scenario, carriers still exist along the vertical channel even without gate voltage. More

importantly, thicker MoS_2 or BP films offer the benefit of higher carrier mobility, which is a crucial factor for un-gated vertical devices. Figure 5.3a shows the optical microscopy image, AFM characterization, and I-V characteristic of a representative Au-BP-Au vertical device. The device exhibits an almost symmetric I-V behavior with a low Schottky barrier and a very high current density of up to 600 A/cm^2 (corresponding to a current of $\sim$ 140 μA) at a voltage of -1 V. Figure 5.3b presents similar characterization performed on a vertical Au-MoS_2-Au device with a MoS_2 flake thickness of μ 24 nm. Similar to the BP device, the vertical MoS_2 device exhibits slightly Schottky-like I-V behavior. The current density on the other hand is significantly smaller than the BP device, at around 25 A/cm^2 (or $\sim$ 6.5 μA) for a voltage bias of 1V, which is due to a combination of the lower carrier mobility in MoS_2, a slightly larger Schottky barrier at the Au/MoS_2 contact, and a relatively low carrier density in the MoS_2 channel with no gate voltage is applied. Lastly, the Au-BP-MoS_2-Au heterostructure device is characterized as shown in Figure 5.3c. One can see that the device I-V curve shows predominant current-rectifying behavior with a rectification ratio of $\sim$ 28.5 and a forward current density of $\sim$ 71 A/cm^2. The Schottky barrier at the Au/MoS_2 contact can be ruled out as the cause of the rectifying behavior because the forward current of the Au-BP-MoS_2-Au heterostructure is measured when the Au/MoS_2 Schottky junction is reversely biased. By comparing the three types of vertical devices, we can safely conclude that the introduction of BP/MoS_2 heterostructure forms a heterojunction p-n diode. The schematic energy band diagrams for an ideal heterojunction diode at the BP/MoS_2 interface are presented in Figure 5.3d. When no external voltage is applied, the p-n junction is in thermal equilibrium and the Fermi energy level is constant throughout the entire system, as shown in Figure 5.3d (i). Under forward bias, the potential barrier decreases leading to majority carriers (electrons) in MoS_2 being injected into the BP side (Figure 5.3d (ii)). Under reverse bias, the potential barrier increases, preventing the electrons in MoS_2 from being injected into the BP side. The minority carriers (electrons in BP and holes in MoS_2) are extracted into the opposite side, resulting in reverse current. Since the concentrations of

minority carriers are very low, the current under reverse bias is very small, resulting in the conventional diode-like rectifying I-V curve.

5.4 Comparison of Vertical and Lateral Heterostructure Diodes

The truly vertical 2D van der Waals heterojunction p-n diode demonstrated in this work has significant performance advantage compared with the lateral one widely reported in the literature. We have fabricated and compared the performance of both vertical and lateral BP/MoS_2 p-n diodes. As shown in Figure 5.4a, while both types of devices clearly exhibit current rectifying behavior with rectification ratio of ~ 27 for the vertical diode and ~ 28 for the lateral one, the forward current density of the vertical diode is ~ 29.4 A/cm^2 (red trace) which is much higher than the ~ 0.43 A/cm^2 measured from the lateral device (blue trace). The results above can be explained by a simplified model by considering the different components that govern the current transport in the p-n junction diode. As illustrated in Figure 5.4b, the total resistance of a BP/MoS_2 heterojunction diode can be roughly divided into four parts, including: 1) the resistance of BP/MoS_2 p-n junction at the interface (R_j); 2) the sheet resistances of BP (R_{ob}) and MoS_2 (R_{om}) in the overlapped junction region; 3) the series resistance of BP (R_{sb}) and MoS_2 (R_{sm}) outside the overlapped region; and 4) the contact resistances of Au/BP (R_{cb}) and Au/MoS_2 (R_{cm}). The junction resistance R_j of the p-n diode governs the rectifying characteristics observed in both types of devices. While the values of the sheet resistance R_o and contact resistance R_c components are likely similar in both the vertical and lateral diode devices, the contributions from the series resistance R_s component are drastically different. For a vertical BP/MoS_2 p-n diode, the carriers only have to travel across a very thin channel of a ~ 30 nm with essentially no series resistance. In contrast, for a lateral BP/MoS_2 diode, since no gate voltage is applied to modulate the carrier concentration, the series resistances through the relatively long (a few μm) BP (R_{sb}) and MoS_2 (R_{sm}) layers are very significant. The fact that the vertical diode device exhibit

$\sim$ 70 fold improvement in forward current density compared to the lateral device indicates that the series resistance is the limiting factor for the device performance.

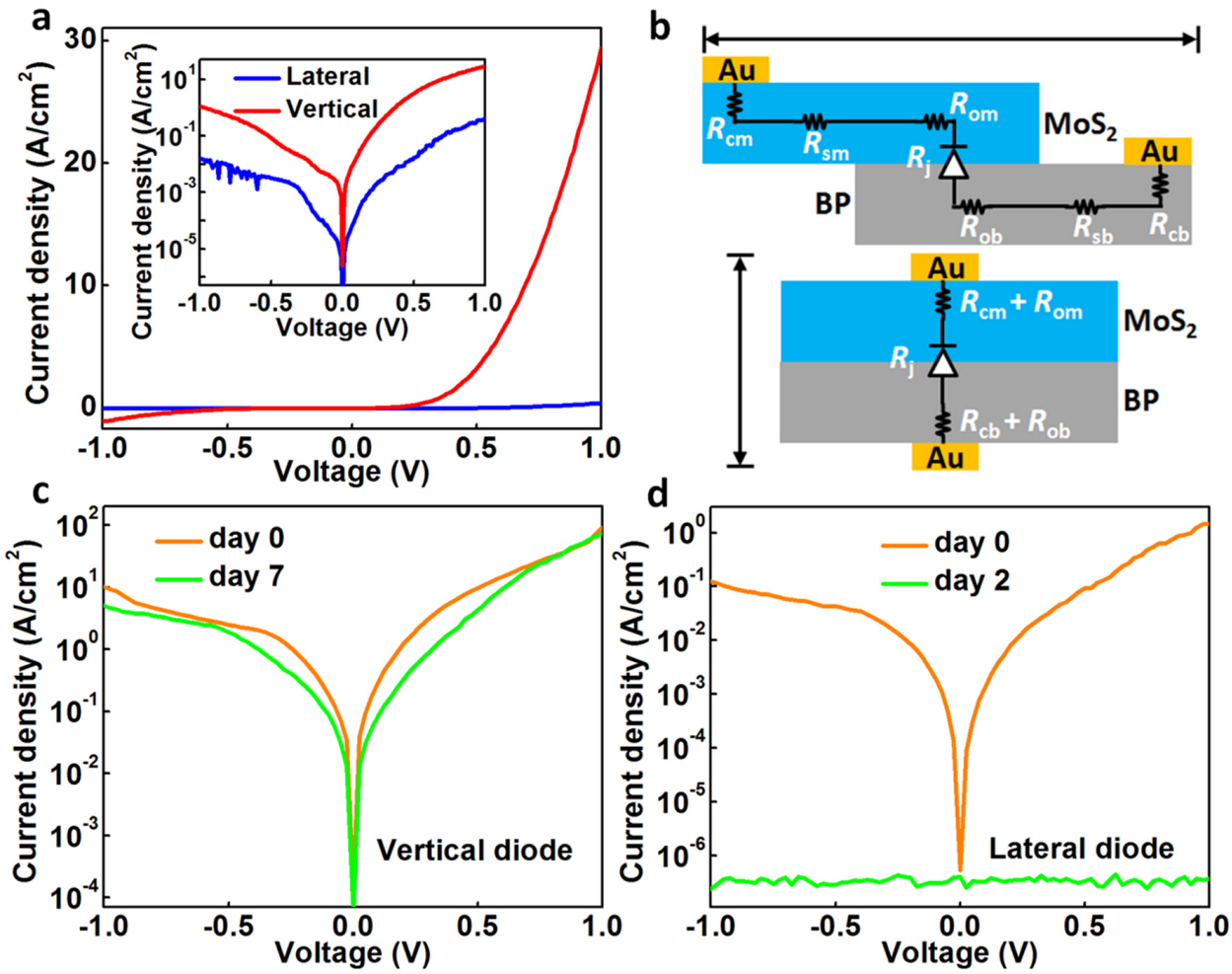

Figure 5.4 Comparison of vertical and lateral BP/MoS_2 heterostructure p-n junction diodes. (a) I-V curves of vertical and lateral BP/MoS_2 p-n diodes. Inset: Semi-logarithmic scale plot of the same I-V curves. (b) Schematic diagram showing the simplified device model of the lateral and vertical BP/MoS_2 p-n junction diodes. (c, d) Ambient stability study of (c) vertical and (d) lateral BP/MoS_2 heterojunction p-n diodes.

Another important advantage of the vertical heterojunction diode structure is its ability to get the sensitive material protected from ambient degradation. In our BP/MoS_2 p-n diode, the BP layer is intentionally placed at the bottom so that it can be fully encapsulated by the MoS_2 and Au electrode on top. Figure 5.4c and d show the ambient stability study of vertical and lateral BP/MoS_2 p-n junction diodes. The evolution of surface morphologies overtime

for both vertical and lateral BP/MoS_2 p-n diodes are presented in the Figure 5.2. From both the AFM image (Figure 5.2), one can find that a vertical BP/MoS_2 p-n diode could still preserve good electrical performance even after being stored in ambient conditions for 7 days. In contrast, a lateral BP/MoS_2 p-n diode whose BP layer is only partially covered by the MoS_2 completely degraded and exhibited no current signal after being stored in ambient conditions for 2 days (Figure 5.2). On the basis of above experiments, one can conclude that the MoS_2 layer in the vertical diode provides a sufficient barrier for moisture diffusion and effectively suppress device degradation.

5.5 Temperature-Dependent Study of Heterostructure Diodes

To further investigate the charge transport through the Au-BP-MoS_2-Au vertically stacked p-n diodes, we have also carried out low temperature electrical studies. Figure 5.5a shows the output characteristics of a representative vertical diode measured at a low temperature of 180 K. The diode exhibits good current-rectifying characteristic with slightly improved rectification ratio of $\sim$ 116. The diode ideality factor can be determined from a plot of the logarithmic output characteristics at the forward bias based on the following equation: I = I_{sat} - (exp(qV/nk_BT) - 1), where I is the diode current, V is the applied voltage, I_{sat} is reverse saturation current, n is the ideality factor, T is the temperature, q is elementary charge, and k_B is the Boltzmann's constant.[27] For voltage greater than a few k_BT, the "-1" term in the above equation can be ignored. Taking the logarithm of both sides of the equation gives the following equation: ln(I) = ln(I_{sat}) - qV/nk_BT. When plotting the natural logarithm of the diode current versus the applied voltage based on the above equation, the slope gives q/nk_BT, from which the ideality factor (n) for the vertical diode device in this work is extracted to be 1.32 (Figure 5.5b), indicating good interface qualities at the BP/MoS_2 junction.The temperature dependent transport characteristics allow us to determine the potential barrier height across the vertical BP/MoS_2 junction. Since the

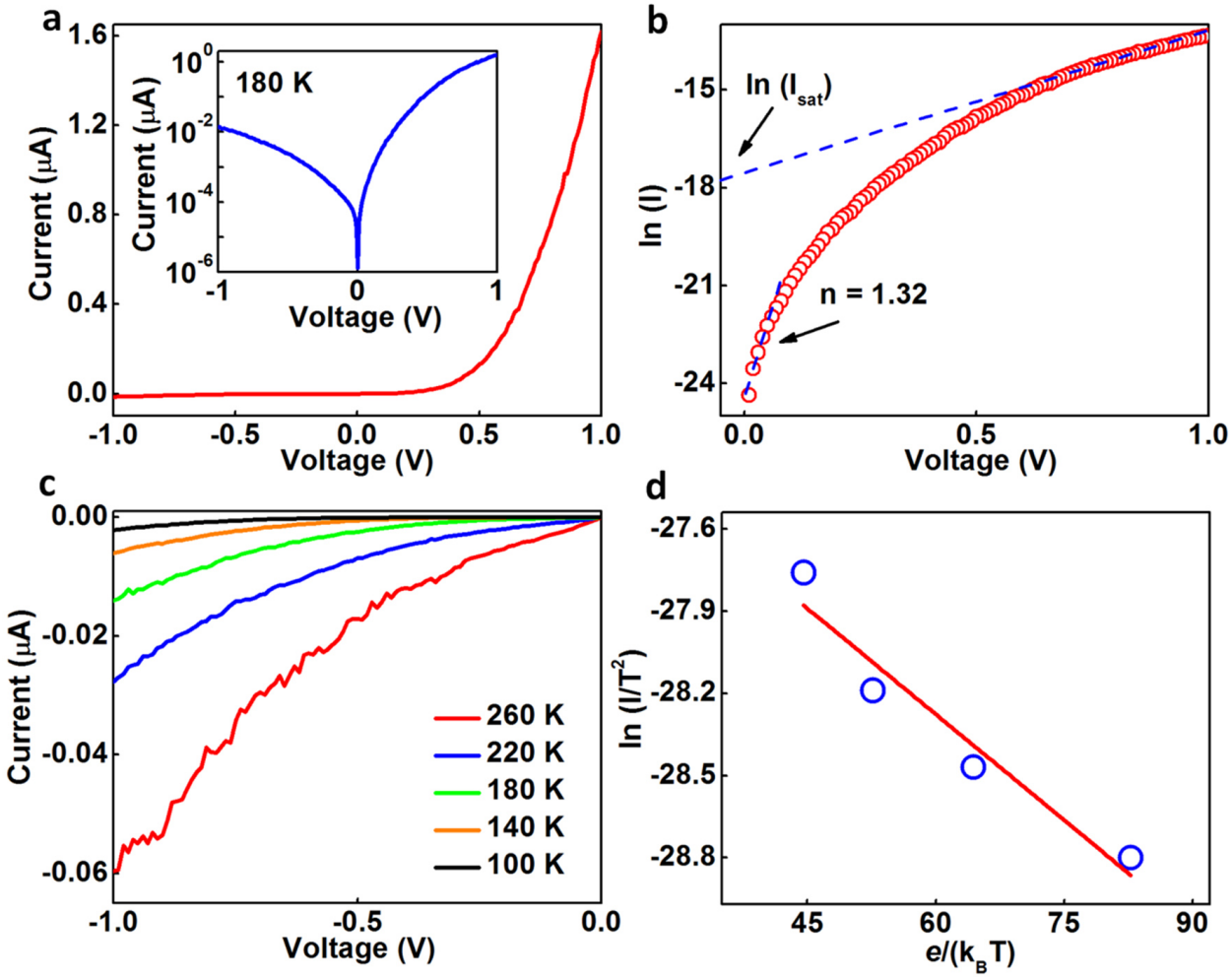

Figure 5.5 Temperature-dependent electrical characteristics of a vertical BP/MoS_2 heterojunction diode. (a) I-V characteristic of a representative vertical BP/MoS_2 p-n diode measured at a temperature of 180 K. The inset is its corresponding semi-logarithmic scale curve. (b) Device ideality factor determined from the slope of the semi-logarithmic graph of device forward-bias current. (c) Reverse bias I-V characteristics measured at different temperatures from 260 K to 100 K. (d) The $\ln(I/T^2)$ versus q/k_BT plot for extracting the potential barrier height at the BP/MoS_2 junction.

BP/MoS_2 junction dominates the rectifying characteristics in the vertical p-n diodes (Figure 5.5c) we can consider the heterojunction barrier as a Schottky barrier. The thermionic emission theory gives the relationship between the diode current and Schottky barrier height: $I = AA^*T^2\exp(-q\varphi_B/k_BT)\ (\exp(qV_{bias}/\eta_{id}k_BT))$, where A is the area of the Schottky junction, A^* is the effective Richardson constant, q is the elementary charge, k_B is the Boltzmann constant, and T is the temperature.[167] Quantitative analysis of the Schottky barrier height φ_B can be determined by investigating the temperature dependent diode current in the reverse bias saturation regime ($\exp(qV_{bias}/\eta_{id}k_BT)$ term $\ll 1$). In this scenario, the diode saturation current I_{sat} is proportional to the $T^2\exp(-q\varphi_B/k_BT)$ term. On the basis of above analysis, the Schottky barrier height at the BP/MoS_2 junction region can be estimated from the slope of the $\ln(I_{sat}/T^2)$ versus q/k_BT plot in the reverse bias saturation regime, as shown in Figure 5.5c and d. The extracted potential barrier height at the BP/MoS_2 junction is ~ 26 meV with a drain voltage of -1 V. The relatively low rectifying ratio of our vertical BP/MoS_2 p-n diode may be attributed to the low Schottky barrier in the BP/MoS_2 junction region.

5.6 Sentaurus TCAD Simulations of Heterostructure Diodes

To further understand the rectifying characteristics of vertical BP/MoS_2 heterostructure p-n diodes, we perform detailed simulations using Sentaurus TCAD. Figure 5.6a and b show the simulated temperature dependent I-V characteristics of a vertical BP/MoS_2 heterostructure p-n diode using commercial simulation package of SDEVICE. The thickness of both BP and MoS_2 films are set to 10 nm and the bandgaps of BP and MoS_2 used in the simulation are set to 0.4 eV and 1.2 eV, respectively. One can see that the simulated I-V curves shown in Figure 5.6a are consistent with experimental results. The calculation is achieved by drift-diffusion model which includes Poisson equation, current transport equations, and carrier continuity equations. The dominated current of a BP/MoS_2 p-n diode at 100 K is the

tunneling current which can be simulated using simplified band-to-band tunneling (BBT) model. When increasing device temperature, the generation-recombination (G-R) of minority carriers will lead to the increase of reverse saturation current, which can be simulated usng the Shockley-Read-Hall (SRH) and Auger recombination models. In the simulation, the carrier concentration in BP and MoS_2 increases with increasing temperature. The minority carrier lifetime of BP/MoS_2 p-n diodes also increases with increasing temperature. Based on the simulated I-V characteristics (Figure 5.6b), the potential barrier height at the BP/MoS_2 heterojunction is $\sim$ 23 meV (drain voltage = -1 V) showing very good agreement with experimental results. Figure 5.6c shows the electric field contour plots for the simulated vertical BP/MoS_2 diodes using TCAD. One can see that the p-n junction region has a peak electric field of around 6.5 $\times$ 10^5 V/cm.

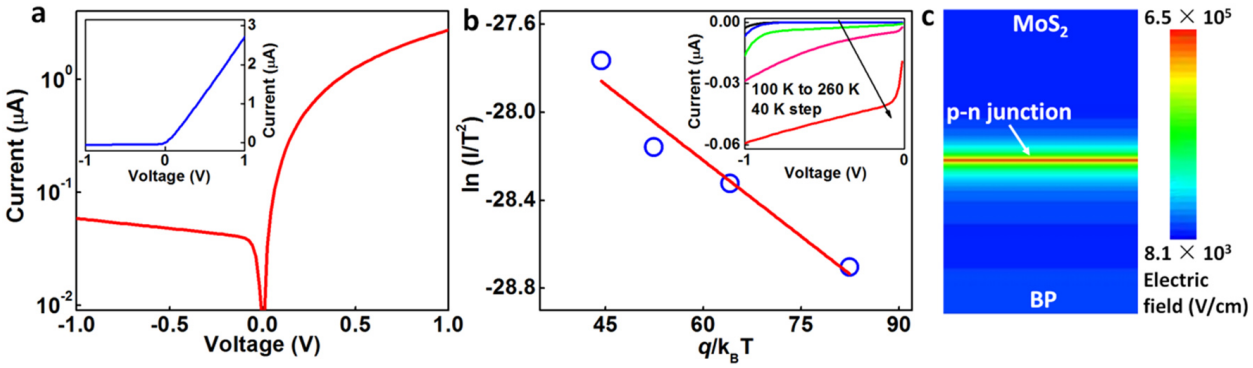

Figure 5.6 TCAD simulations of vertical BP/MoS_2 heterojunction p-n diodes. (a) Simulated semi-logarithmic scale I-V characteristics of a vertical BP/MoS_2 p-n diode. The inset shows its linear scale I-V curve. (b) The ln(I/T^2) versus q/k_BT plots for extracting the barrier height at the BP/MoS_2 junction. Inset: Simulated temperature-dependent I-V characteristics under reverse bias. (c) Simulated electric field contour plot for the vertical diode.

5.7 Summary

In summary, we have developed a truly vertical BP/MoS_2 heterostructure p-n junction diode by completely eliminating the lateral regions of the 2D layers and their corresponding series resistance. Such device design offers significant performance improvement in terms of

forward current density. Additionally, by comparing the vertical BP, MoS_2, and BP/MoS_2 heterostructure devices, we find that the introduction of BP/MoS_2 heterostructure results in devices with strong current-rectifying behavior. The vertical device design also allows the bottom BP layer to be fully protected from ambient degradation by the MoS_2 layer on top. Low-temperature measurements and TCAD simulations were used to further elucidate the operation of the vertical BP/MoS_2 diodes and extract the potential barrier height at the junction. This work provides new insight into the vertical assembly of 2D layered semiconductors for future high-performance nanoelectronic and optoelectronic electronics.

CHAPTER 6

CONCLUSION AND FUTURE WORK

In this chapter, all the completed work would be concluded and several ideas for the potential future work would be proposed.

6.1 Summary of Thesis

Through this report, the author has demonstrated a variety of 2D functional nanodevices such as ultrascaled transistors, heterostructure diodes, chemical sensors, photodetectors and single-pixel camera. This work opens up possibilities for future nanoelectronics and opto-electronics applications using 2D thin films.

We first report a facile method combining EBL and angle deposition to fabricate high-performance top-gated BP FETs with channel lengths down to 20 nm. With such small channel length, the devices show very high on-current. In addition, such ultrascaled BP transistors still preserve decent on-off current ratio (more than 10^2), and field effect mobility, which demonstrates the great potential of using BP for high-performance future ultimately scaled electronic devices. In addition, we have demonstrated BP-based Schottky diodes with current rectifying behavior by using asymmetric metal contacts. Inspired by angle deposition to achieve ultrascaled devices, we studied the channel scaling of BP Schottky diodes and showed that the channel length plays a critical role in determining the output characteristics of the Schottky diodes. If the channel length is aggressively scaled down to around 30 nm, the diode could lose its rectifying characteristics due to increased tunneling current caused by electric field induced Schottky barrier thinning. The results indicate that relatively long channel is preferred if the BP Schottky diode is to be used as high on-off ratio photodetectors. With a built-in potential caused by the metal work function difference in

the asymmetrically contacted BP Schottky diode, photodetectors with fast response time of less than 2 ms has been demonstrated.

Atomically thin 2D materials exhibit very large surface to volume ratio compared with their bulk counterparts. Therefore, 2D materials are very promising material candidate for chemical sensor applications. Here, we have studied the humidity sensing behavior of few-layer BP FETs under ambient conditions. Because the BP flakes are known to degrade rapidly in ambient conditions, a 6-nm-thick Al_2O_3 dielectric layer was used to passivate the BP sensors in order to make them air-stable. Thorough characterizations reveal that the Al_2O_3 encapsulation can effectively suppress BP degradation, which lead to devices with drastically improved long-term stability in air with a tradeoff in slightly reduced sensitivity. Lastly, C-V measurements were used to elucidate the humidity sensing mechanism of BP devices. The electrostatic interaction between water molecules and BP flakes would result in increased hole concentration in BP, thus enhancing the p-branch current. Our results demonstrate a viable approach for achieving air-stable BP-based chemical sensors for practical applications.

Layered BP film is a direct bandgap semiconductor with tunable gap changing with 0.3 eV to 2 eV. So, it can be used as visible and infrared photodetection material. Here we have demonstrated flexible BP infrared photodetectors with high responsivity of around 53 A/W and gain of around 8,000% at room temperature. Such high responsivity is achieved due to the use of polyimide substrate with low thermal conductivity, which results in strong photothermal effect and substrate heating upon light illumination. The photo-generated heat leads to enhanced phonon scattering and mobility degradation, which generate significant negative photocurrent of 20 to 30 μA under infrared laser illumination (16.5 W/cm^2). To further elucidate the underlying mechanism governing the negative photoconductivity in flexible BP FETs, temperature study and detailed device simulation using Sentaurus TCAD were performed. The results confirm that the increase in substrate temperatures leads to almost the same device conductance decreases, which further demonstrate that the negative photo-

conductivity in flexible BP FETs is caused by heating effect. This works provides insights on understanding photothermal effect in photodetectors built on low thermal conductivity substrate and may also lead to novel high-sensitivity broadband wearable and bio-integrated photodetectors or imagers. To take advantage of the outstanding photoresponse of BP and overcome the difficulties of BP film growth and scalable photodetector array fabrication, a near-infrared camera based on a single BP photodetector was developed using the compressive sensing algorithm. We have demonstrated that by directing the original infrared image onto a DMD that projects the image onto the BP photodetector, the original infrared image can be decoded and reconstructed from the current signal collected by the BP photodetector. For our single-pixel BP camera, the sampling rate of image acquisition is much smaller than the Nyquist rate. Infrared laser spot images with 32×32 and 64×64 pixels were successfully captured with only 500 and 2000 times of measurements. This work demonstrates the efficacy of using 2D black phosphorus based photodetector for practical infrared imaging applications.

Finally, we have developed a truly vertical BP/MoS_2 heterostructure p-n junction diode by completely eliminating the lateral regions of the 2D layers and their corresponding series resistance. Such device design offers significant performance improvement in terms of forward current density. Additionally, by comparing the vertical BP, MoS_2, and BP/MoS_2 heterostructure devices, we find that the introduction of BP/MoS_2 heterostructure results in devices with strong current-rectifying behavior. The vertical device design also allows the bottom BP layer to be fully protected from ambient degradation by the MoS_2 layer on top. Low-temperature measurements and TCAD simulations were used to further elucidate the operation of the vertical BP/MoS_2 diodes and extract the potential barrier height at the junction. This work provides new insight into the vertical assembly of 2D layered semiconductors for future high-performance nanoelectronic and optoelectronic electronics.

6.2 Future Work

Based on the results achieved so far, several potential research projects related to atomically thin 2D materials may be carried out for the next step. And they are listed as follows:

6.2.1 Large-Scale Growth and Integration of 2D Thin Films

Atomically thin semiconductor films with vertical compositions that are designed to atomic-scale precision would provide the foundation for future integrated circuitry. To realize such film integration, layer-by-layer assemble of 2D thin films is a very good approach.[24] With this approach, graphene and TMDs have been used to realize previously inaccessible heterostructures with interesting physical properties. However, no large-scale integration method exists at present that maintains the intrinsic properties of these 2D building blocks while producing pristine interlayer interfaces, thus limiting the layer-by-layer integration method to small-scale proof-of-concept demonstrations. Therefore, there is a need for integration of large-scale 2D thin films with a high level of spatial uniformity and pristine interfaces.

CVD technique is a very good approach to achieve large-scale epitaxial growth monolayer graphene and TMDs. The CVD system contains three-temperature zone used for heating, and Sulfur source, MoO_3 source and substrates are separately placed in each zone. During growth, the carrier gases for the Sulfur and MoO_3 sources are Ar and Ar/O_2, respectively. A small amount of O_2 mixed with Ar is used to protect MoO_3 from sulfurization for steady evaporation and balancing the growth rate by etching. Monolayer TMD continuous films with very high uniformity and quality can be achieved using this method.

Layer-by-layer assembly of 2D thin films under vacuum proposed by J. Park's group can fabricate large-scale, high quality heterostructrue films and devices, including superlattice films with vertical compositions.[24] Figure 6.1 shows a representative high-quality semiconductor heterostructure film generated using a programmed vacuum stack (PVS) process. The

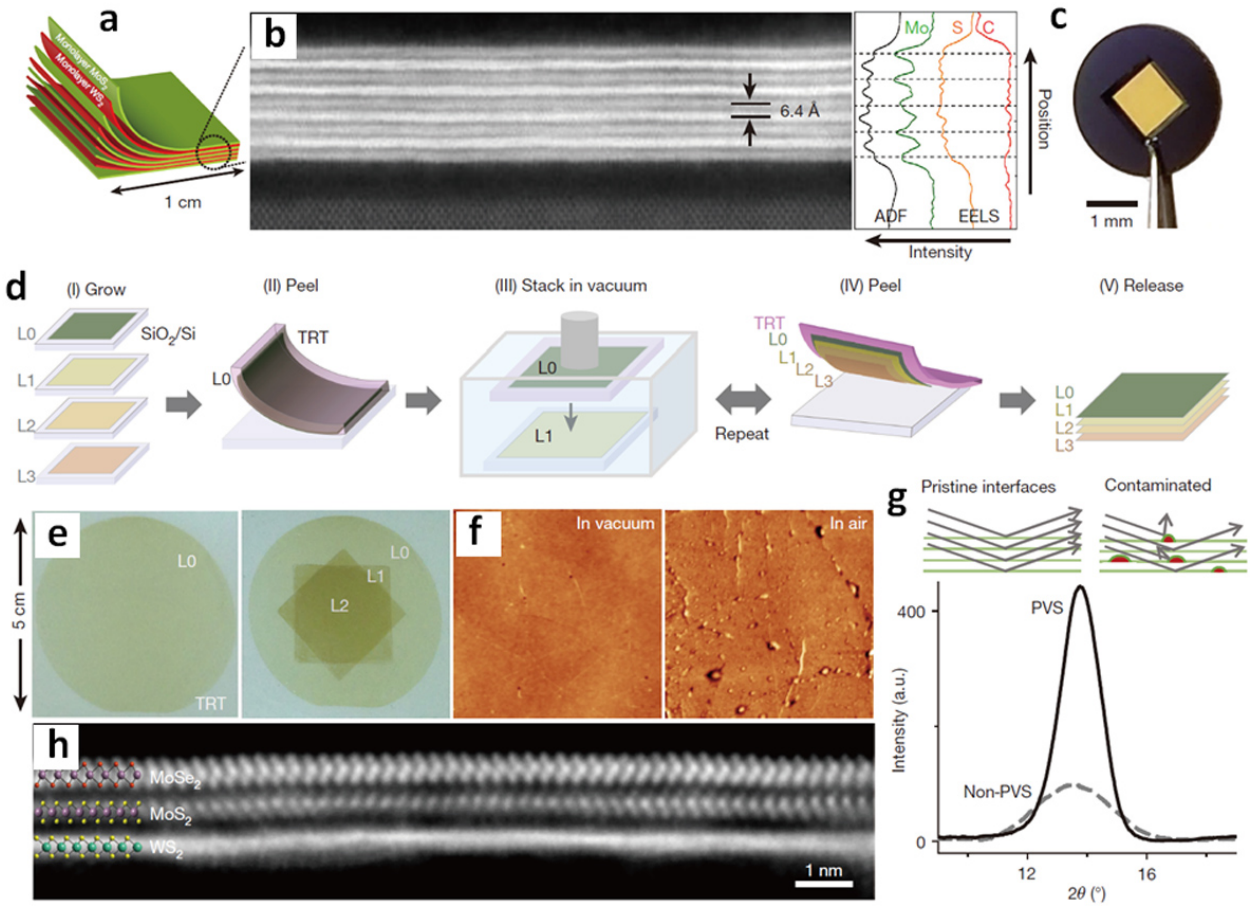

Figure 6.1 High-quality vertically designed semiconductor films using layer-by-layer assembly. (a) Schematic of a vertically stacked MoS_2/WS_2 superlattice. (b) Cross-sectional ADF STEM image of a superlattice film transferred onto a silicon wafer. (c) Image of a large-scale freestanding ultrathin semiconductor film. (d) A schematic of the PVS process. (e) Optical microscope images of wafer-scale MoS_2 films after layer-by-layer assembly. (f) AFM height images of three-layer MoS_2 films stacked in vacuum and air. (g) XRD pattern of four-layer MoS_2 generated by the PVS process and by conventional dry transfer. (h) Cross-sectional STEM image of a $MoSe_2/MoS_2/WS_2$ film with the electron beam aligned with the armchair axis of $MoSe_2$ (top) and MoS_2 (middle).[24]

film is assembled by vertically stacking nine layers of individual wafer-scale TMD monolayer, alternative between MoS_2 and WS_2. The STEM confirms the vertically stacked design, and reveals a composition with atomic-scale precision and clean interfaces. The chemical composition of each layer is further confirmed by electron energy loss spectroscopy indicating that Mo peaks for only the MoS_2 layers, but a uniform sulfur signal everywhere within the film. AFM and XRD characterizations show that the film interface is very clean. Therefore, the PVS process provides a versatile way of systematically generating large-scale 2D heterostructures and devices, the properties of which are designed with atomic-scale precision. It will accelerate the discovery of new materials and large-scale development of ultrathin multifunctional integrated circuitry.

6.2.2 3D Integrated Circuits Built from 2D Materials

The computing demands of future data-intensive applications will greatly exceed the capabilities of current planar CMOS based electronics, and are unlikely to be met by isolated improvements in transistors, data storage technologies or IC architectures alone. Instead, 3D transformative nanosystems, which use new nanotechnologies to simultaneously realize improved devices and new integrated circuit architectures, are required.[25] Unlike conventional 2D CMOS based IC architectures, the layered fabrication of nanomaterials can realize 3D IC architecture with fine-grained and dense vertical connectivity between layers of computing, data storage and input and output. Figure 6.2 presents an experimental prototype of a new computing nanosystem, which integrates multiple new nanotechnologies to realize 3D IC architecture. This nanosystem contains resistive random-access memory (RRAM) arrays, silicon and carbon nanotube field-effect transistor (CNFET) computation units and memory access circuitry, and more than one million CNFET-based gas sensors for inputs, all fabricated on overlapping vertical layers. The key advantages of this 3D nanosystem compared to current technologies are that it uses: (1) CNFETs instead of silicon transistors; (2) on-chip nonvolatile RRAM for data storage instead of dynamic random-access memory

based off-chip memory; (3) monolithic 3D integration of all the function devices; (4) dense back-end-of-line metal wire vias to connect vertical layers of computing and data storage within the monolithic 3D ICs.

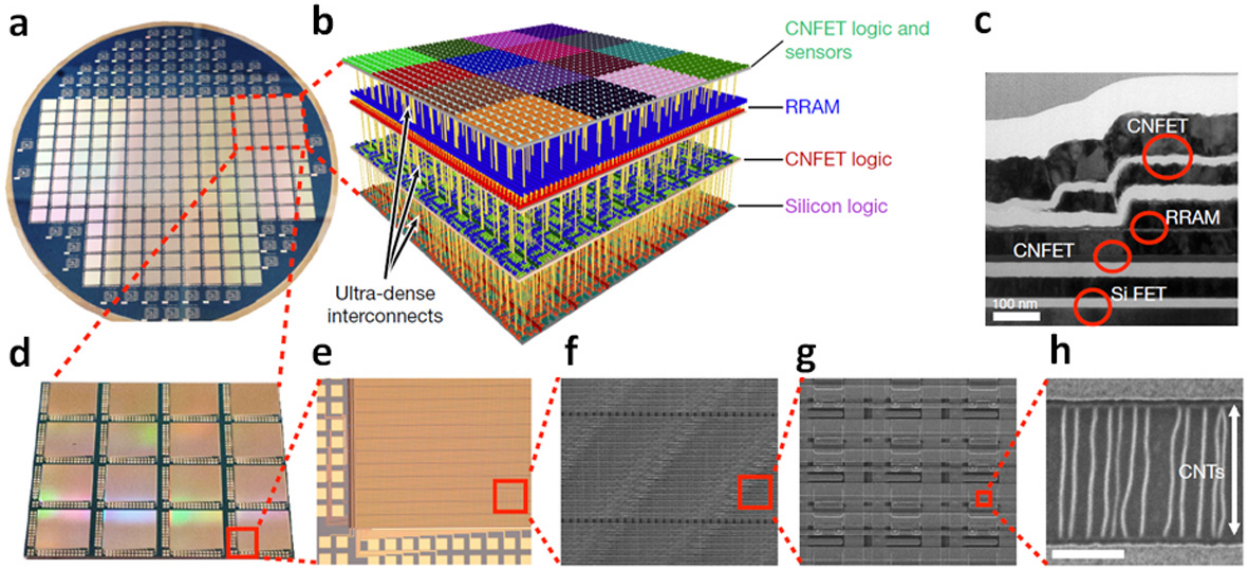

Figure 6.2 3D nanosystem. (a) A 100-mm-wide wafer on which the ICs are fabricated. One chip is outlined in red. (b) Illustration of 3D nanosystem consisting of four monolithically integrated vertical layers, connected through dense vertical inter-connects. (c) Cross-sectional TEM image of the four-layer chip, highlighting each layer. (d-h) Progressively magnified top views of 3D nanosystem.[25]

Inspired by 3D nanosystems built from CNFET arrays mentioned above, atomically thin 2D materials are also perfect building blocks for future 3D integrated devices and circuits. 2D material such as graphene, MoS_2 or BP and hexagonal boron nitride can be used as device metal electrode, semiconducting channel and gate dielectric, respectively. Therefore, all 2D material based 3D nanosystem will be a very hot research topic in the near future.

6.2.3 Flexible and Transparent 2D Electronics

The outstanding electrical, mechanical and chemical properties of atomically thin 2D materials make them dramatically attractive for applications in flexible electronics. More importantly, monolayer 2D films are almost transparent, thus they can be used to make transparent

electronics. Here, we take the graphene as an example. Bae and colleagues reported the roll-to-roll production and wet-chemical doping of predominantly monolayer 30-inch graphene films grown by CVD onto flexible copper substrates.[26] The as-fabricated graphene films have sheet resistances as low as 125 $\Omega/square$ with 97.4% optical transmittance, and exhibit the half-integer quantum Hall effect, indicating their high quality. They further used layer-by-layer stacking technique to fabricate a doped four-layer graphene film and measured its sheet resistance at values as low as 30 $\Omega/square$ at 90% transparency, which is superior to commercial transparent electrodes such as indium tin oxides.

Figure 6.3 shows the photographs of the roll-based synthesis and transfer process. An 8-inch-wide tubular quartz reactor is used in the CVD system, allowing a single-layer graphene film to be synthesized on a roll of copper foil with dimensions as large as 30 inches in the diagonal direction. After CVD growth, the graphene film grown on copper foil is attached to a thermal release tape by applying soft pressure between to rollers. After etching the copper foil followed by deionized water rinsing, the transferred graphene film on the tape is ready to be transferred to any substrates. The graphene film on the thermal release tape is inserted between the rollers together with a target substrate and exposed to mild heat resulting in the transfer of the graphene films from the tape to the target substrate. Screen-printing process is used to fabricate four-wire touch-screen panels based on graphene transparent conducting films. After printing electrodes and dot spacers, the upper and lower panels are carefully assembled and connected to a controller installed in a laptop computer, which shows extraordinary flexibility. Given the scalability and processability of roll-to-roll and CVD methods and the flexibility and conductivity of 2D graphene films, commercial production of large-scale flexible and transparent graphene electronics will be realized in the near future.

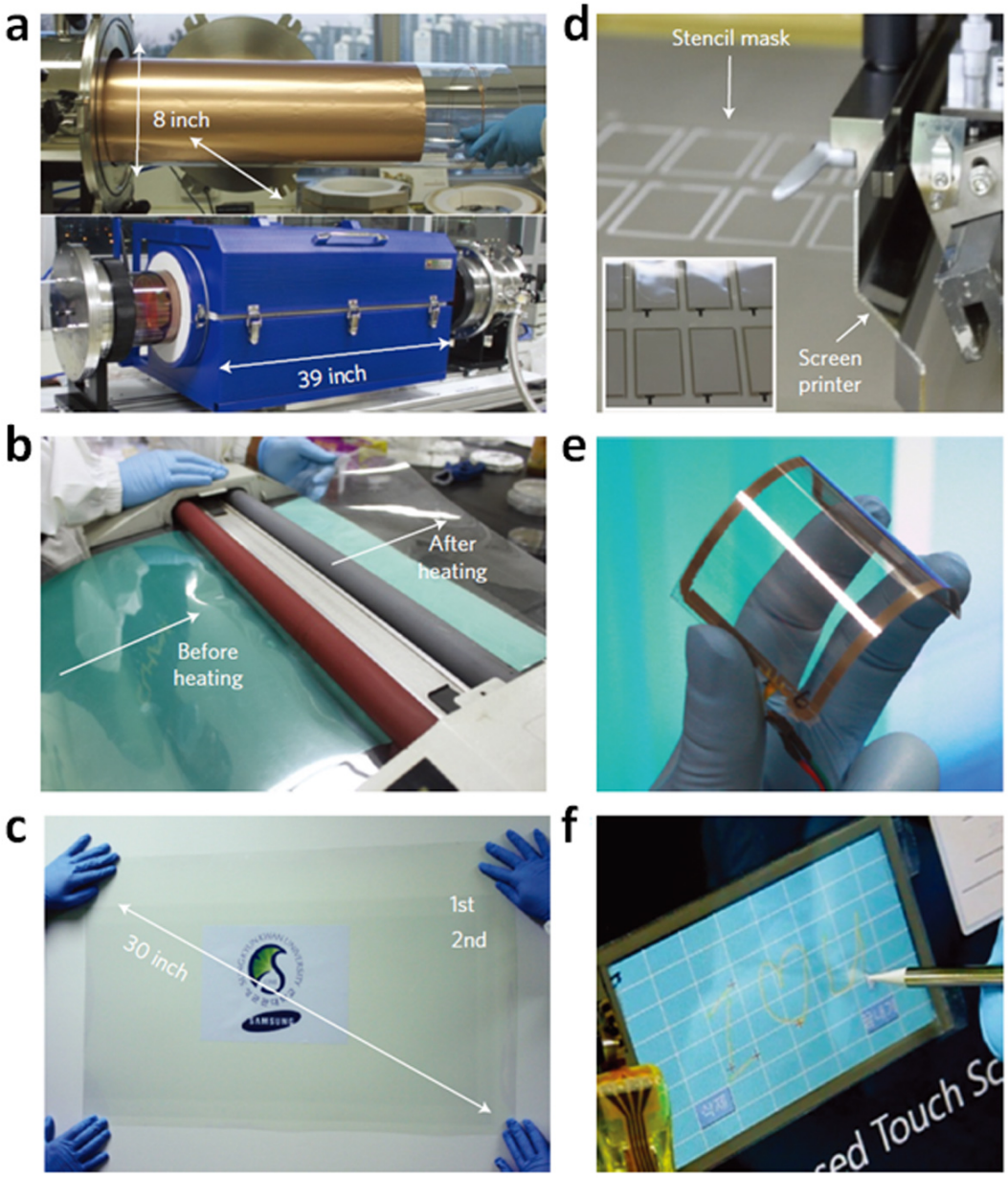

Figure 6.3 Photographs of the roll-based production of graphene films. (a) Copper foil wrapping around a 7.5-inch quartz tube inserted into an 8-inch quartz reactor. The lower image shows the stage in which the copper foil reacts with CH_4 and H_2 gases at high temperatures. (b) Roll-to-roll transfer of graphene films from a thermal release tape to a PET film at 120°. (c) A transparent ultralarge-area graphene film transferred on a 35-inch PET sheet. (d) Screen printing process of silver paste electrodes on graphene/PET film. The inset shows 3.1-inch graphene/PET panels patterned with silver electrodes before assembly. (e) An assembled graphene/PET touch panel showing outstanding flexibility. (f) A graphene-based touch-screen panel connected to a computer with control software.[26]

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