ON THE DESIGN OF SWITCHED-CAPACITOR CONVERTERS FOR LOW POWER APPLICATIONS

By

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A DISSERTATION

Submitted to
Michigan State University
in partial fulfillment of the requirements
for the degree of

Electrical Engineering — Doctor of Philosophy

2018

ABSTRACT

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Power conversion is crucial to most electronic systems due to different voltage levels requirement within the system. Switched-capacitor converters are a subset of switching mode converters, where the energy is transferred from the input to the output using only capacitors and switches. SC converters provide compact solution due to its magnetic-less structure, which makes them ideal to fulfill the high density requirement in low power applications. In literature, Dickson SC converter is considered a good candidate for low power applications compared to other SC topologies. Yet, Fibonacci SC (FSC) topology can be competitive due to their minimum area requirement and relatively good efficiency performance. In addition, FSC provides the highest voltage-conversion-ratio (VCR) using the least number of components, and hence can be useful in high gain applications. Therefore, the main goal of this dissertation is to introduce FSC as a viable solution for low power applications. This dissertation contributes in three domains: (1) SC theory, (2) FSC synthesis and (3) FSC design and implementation.

For the first part, the well-known SC fundamental limit theory, proposed in 1995 by Mark S. Makowski et al, is revisited. This theory sets the VCR boundaries for a specific number of k flying capacitors in a SC converter. Although this limit is valid for the positive VCR, we found that another condition must be satisfied for the negative VCR. As a result, we propose a generalized version of the theory to overcome these limitations, which establishes the foundation for the rest of the work in this dissertation. Second part of the dissertation

explores the FSC synthesis problem. In fact, synthesizing nonlinear SC converters like FSC to achieve certain/multiple VCR is not trivial, and usually performed using ad-hoc approach. Therefore, an efficient algorithm to address the SC synthesis problem is proposed, which is made available as an open-source tool, called *FSC Synthesizer*, to promote the use of FSC. The proposed tool is verified by implementing FSC converter that achieves four VCRs.

Finally, the design procedure and analysis of a variable FSC converter is investigated in both, discrete and on-chip implementation. For the first part, discrete FSC design is studied, and a prototype for a variable FSC is built and tested. The PCB occupies an area of 2.7inch^2, which includes the controller and FSC. The adaptive VCR technique is employed to regulate the output voltage. For 300-600mV input voltage, the proposed converter provides a mean output voltage of almost 1.46V with a 2.67% discrepancy from 1.5V nominal designed voltage. For the second part, the on-chip integration challenges including parasitic charge loss and start-up from low voltage, are studied. A charge recycling technique exploiting the presence of parasitic capacitors in each other phase of FSC converter has been employed resulting in 27% reduction in the power loss, which improves the overall efficiency by 12.7%. For a proof-of-concept, a monolithic FSC is implemented in 0.5μm CMOS technology on 4mm^2 die area. The post-layout simulation is carried out using Virtuoso ADE. With 0.3V input voltage, the system achieves 47.5% peak power efficiency with 5μW load.

This dissertation is dedicated to the memory of my beloved father, Alhussain Mahnashi, who always believed in his son. Rest in peace, father...

ACKNOWLEDGMENTS

I would like to take this opportunity to express my sincere appreciation for all the support and encouragement that have led to the completion of this dissertation. I am greatly indebted to my advisor, Prof. Fang Z. Peng, for his continuous support, help and encouragement throughout my PhD studies at Michigan State University.

I would also like to thank Prof. Bingsen Wang, Prof. Wen Li, and Prof. Chunqi Qian for serving on my committee. I am deeply grateful to them for their valuable comments and insightful discussions. I owe a sincere acknowledgment to Saudi Arabia government through King Fahd University of Petroleum and Minerals to grant me a prestigious scholarship to peruse my PhD studies.

Special thanks go to my colleagues in the Power Electronics and Motor Drives Lab: Dr. Shuitao Yang, Dr. Gujing Han, Dr.Wei Qian, Deepak Gunasekaran, Ujjwal Karki, Hulong Zeng, Xiaorui Wang, Yunting Liu, Allan Taylor, Nomar Gozález-Santini, Omar Aljawhari and Petros Taskas, for making my stay at Michigan State University more enjoyable, and for their insightful and helpful academic inputs.

I am greatly grateful to my family and friends for their tremendous support and encouragement. My profound gratitude is to my mother for her endless love, prayers and support. I could not be more grateful to my beloved wife and sons, Yusuf and Albara. This dissertation would not have been accomplished without their love, care, patience and support. Thank you all for making this dream a reality.

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KEY TO ABBREVIATIONS

ADE Analog Design Environment

SC Switched-Capacitor

SI Switched-Inductor

FSC Fibonacci Switched-Capacitor

VCR Voltage Conversion Ratio

aVCR adaptive Voltage Conversion Ratio

LDO Linear Regulator

EMI Electromagnetic Interference

IC Integrated Circuit

PCB Printed Circuit Board

WSN Wireless Sensor Network

CW Cockroft-Walton

CP Charge Pump

LQP Linear Charge Pump (Dickson converter)

MIMO Multiple Input Multiple Output

SIMO Single Input Multiple Output

MISO Multiple Input Single Output

LUT Look Up Table

MOS Metal Oxide Semiconductor

CMOS Complementary Metal Oxide Semiconductor

MOM Metal Oxide Metal

MIM Metal Insulator Metal

PIP Poly Insulator Poly

ANTZ All Negative terminals connected To Zero

SPTT Single Pole Triple Throw

SSL Slow Switching Limit

FSL Fast Switching Limit

VCE Voltage Conversion Efficiency

PCE Power Conversion Efficiency

ZVS Zero Voltage Switching

RO Ring Oscillator

CSRO Current-Starved Ring Oscillator

EH Energy Harvesting

AQP Auxiliary Charge Pump

NCP1 modified Dickson Charge Pump Version 1

NCP2 modified Dickson Charge Pump Version 2

CCCP Cross-Coupled Charge Pump

TP Top Plate

BP Bottom Plate

Chapter 1

Introduction

In this chapter, the switched-capacitor (SC) converter is introduced. For lower power applications, many SC configurations can be utilized. However, Fibonacci SC converter (FSC) [1,2] and Dickson converter [3] are considered to be the best topologies due to their less area requirement and good efficiency performance. Therefore, an overview of these topologies will be presented, and followed by the research scope and summary of contributions.

1.1 Overview

The power conversion is crucial in most electronic systems. As shown in Figure 1.1, there are two ways to implement DC-DC converters: passive and switching-mode implementation. The DC-DC converters are used to step-down or step-up the input voltage based on the system requirement. For step-down conversion, passive implementation or so-called linear regulators (LDO) are commonly used due to less area requirement and easy control. Figure 1.2 illustrates a simple implementation of LDO, which is basically a voltage divider circuit implemented around an active controlled switch that works as a variable resistor. Despite its simplicity and minimal active area requirement, LDO suffers from low efficiency and only can be used for step-down conversion [4]. Note that, the LDO efficiency can be very high if the output voltage is close to the input voltage, i.e theoretically 100% efficiency can be achieved when no conversion is performed (V_{in}=V_{out}).

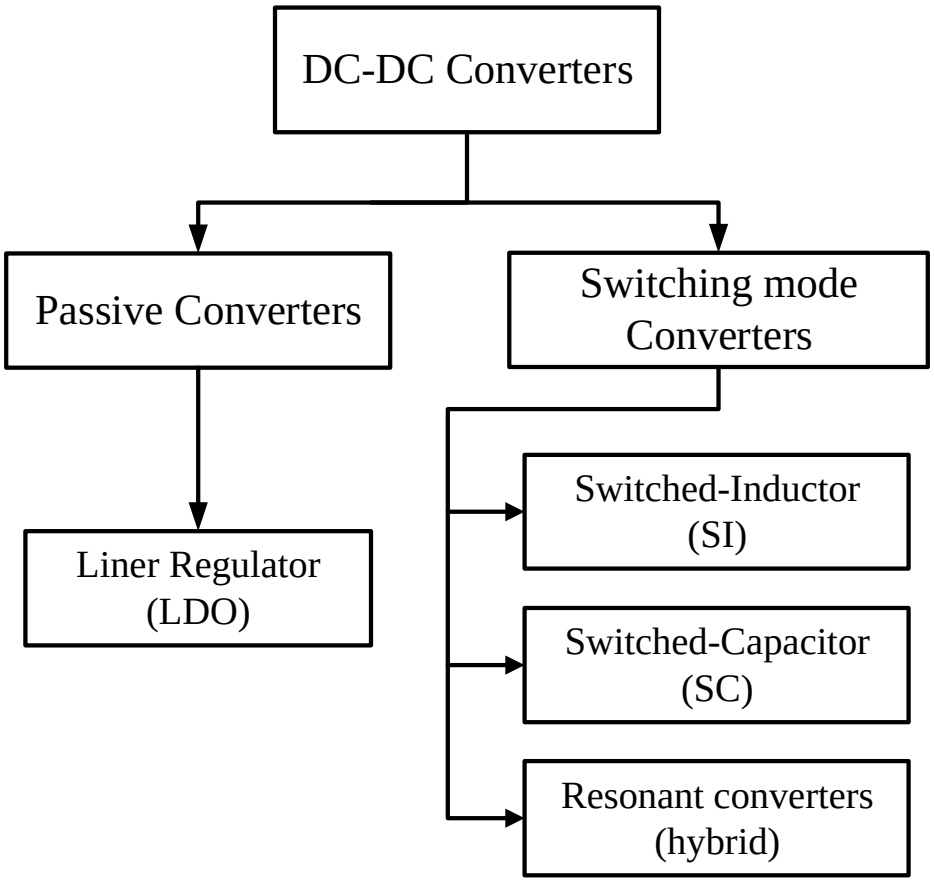


Figure 1.1: Types of DC-DC converters.

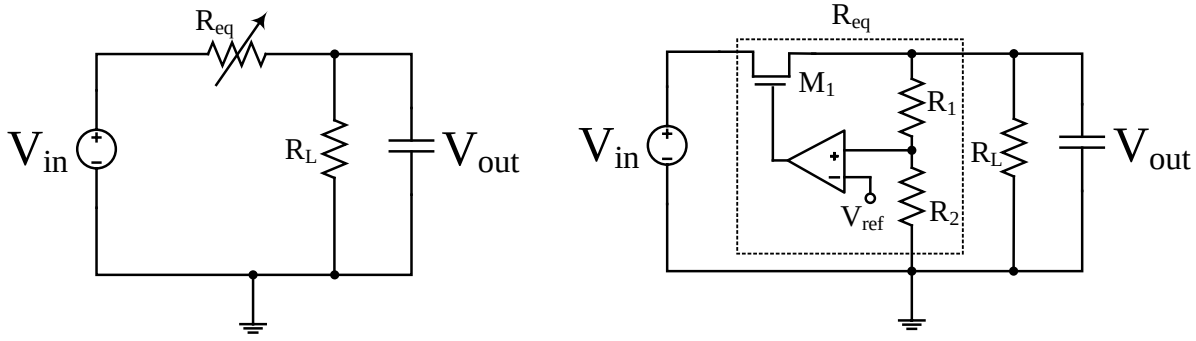


Figure 1.2: Linear regulator (LDO) circuit.

The switching mode converters are more versatile as they can be implemented to step-down or step-up the input voltage [5]. In addition, some converters are capable of both conversions owing to the intelligent control circuit and converter design. Switching mode converters are implemented using switch networks (SN) and storage elements to transfer the input energy to the output. Based on the storage element, the switching converters can be categorized into three main groups: switched-capacitor (SC), switched-inductor (SI) and resonant converters (hybrid), see Figure 1.1. Examples of SI converters include buck, boost, SEPIC, Ćuk, Flyback converters and many others [6]. They are widely used in commercial products due to their high efficiency and relatively simple design. However, the main disadvantage of SI converters is the use of an inductor which is a bulky element and usually associated with poor EMI performance.

On the other hand, the SC converters, sometimes referred to as charge pumps [7], use capacitors as storage elements, commonly referred to as flying capacitors, which makes them attractive for monolithic IC integration due to their compact and magnetic-less features, the functional blocks diagram is depicted in Figure 1.3. Dickson, Fibonacci, ladder, series-parallel and voltage doubler and their variants are examples of SC converters. Most SC converters can be driven in open loop scenario using at least two non-overlapping clocks to avoid shoot-through states. Despite these advantages, SC converters suffer from poor output regulation and the conversion efficiency drops drastically when the output voltage deviate from the target voltage due to the input voltage change and/or loading effect. Therefore, achieving more voltage-conversion-ratios (VCR) minimizes the error between the output and target voltage which effectively improve the efficiency. Ideally, a the better conversion performance can be achieved by increasing the number of VCR. Yet, synthesizing SC converter to perform multiple VCR is considered a major challenge, commonly referred to as SC synthesis

problem.

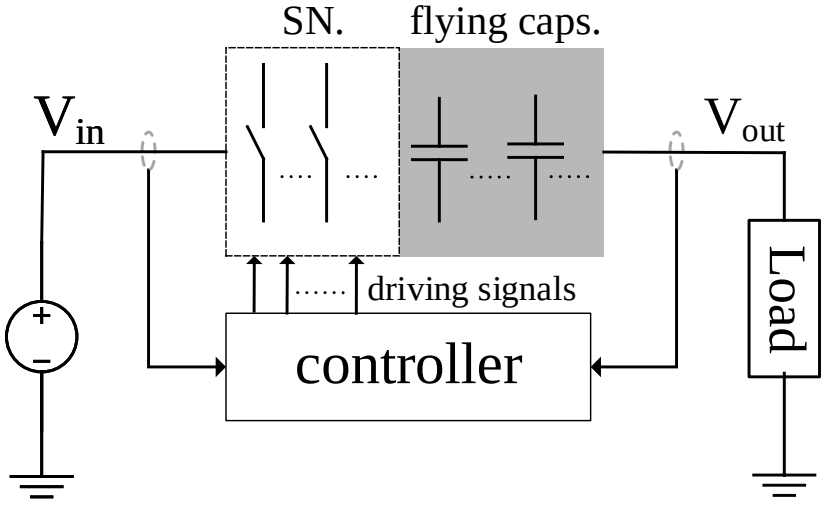


Figure 1.3: Functional SC converter building blocks.

Generally, solar energy is abundant and can be utilized to prolong the battery life for applications that require expensive or invasive battery replacement, such as wireless sensor nodes (WSN) and bio-implementable devices. To drive this work to a practical implementation, we consider a smart solar cell which consists of an on-chip solar cell, implemented using photo-diodes, and SC boost converter as shown in Figure 1.4. The concept of smart solar cell is to replace conventional solar cell with low open circuit voltage, V_{oc}, with a system containing the solar cell and boost converter to output higher voltage level that can recharge a battery or power a system. Also, smart solar cell is expected to be autonomous meaning, the integrated converter starts up and operate without any external biasing. In addition, the converter needs to smart enough to detect V_{oc} variations, usually $0.3-0.6$V in miniaturized solar cells, and apply any technique for output regulation. Referring to Figure 1.4, the smart solar cell supplies the power management unit (PMU) with a dc voltage >1V which is adequate to power up microsystem in some applications. Then, PMU is responsible

to power up the system, WSN or implanted device ..etc, from the smart solar cell. In case if there is no enough power, PMU bypasses the smart solar cell and supply power to the system using the battery. For this operation, we need to design a SC converter that can startup from low voltage and configures itself to provide enough supply voltage and all are done autonomously and without any external component. There are some challenges that limits a high efficiency in IC SC converters. Therefore, in this work, we will focus only on the SC converter block. In the following section, a brief history of SC development is presented.

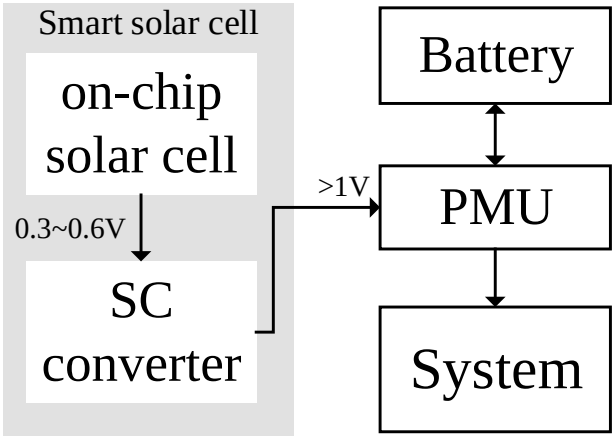


Figure 1.4: Conceptual smart cell building blocks.

1.2 A Brief History on SC Development

SC converters can be traced back to the first high voltage Cockroft-Walton (CW) multiplier [8]. This multiplier suffers from high stray capacitance and to have efficient multiplication, pumping capacitors need to be very large which is impractical in monolithic integration. To overcome this problem, the CW multiplier was modified by connecting pumping capacitors in parallel to the input instead of being connected in series. This is a well-known Dickson

charge pump (CP) [3], or sometimes referred to as linear charge pump (LQP) because the VCR is linear and can take any integer from 1...n, where $n \geq 1$. Therefore, CW multiplier and Dickson CP are quite similar in basic structure and operation, but working in two different power and voltage levels.

The CW multiplier was developed for high voltage generation of $800k$V whereas Dickson CP was intended for low power applications enabling integration in the same substrate. Figure 1.5 illustrates both circuits, highlighting the similarities between them. Dickson basically connected the flying capacitors to the clock instead of being connected in series as in CW circuit. This decreases the stray capacitance at the junctions, x and y, which improves the total converter performance. Since then, Dickson CP has been the main voltage multiplier in IC circuits. The output voltage in Dickson CP can be found using the following equation:

$$V_{out} = n(V_{in} - V_D), \tag{1.1}$$

where n is the number of stages, and each stage consists of a diode and flying capacitor. V_D is the diode voltage drop which is approximately 500-700mV, and it equals the threshold voltage (V_{th}) if the diode is implemented using a MOS transistor. Dickson converter suffers from the diode voltage drop. Therefore, to achieve higher voltage level, the diode voltage drop needs to compensated by adding more stages.

Following Dickson invention, many topologies have been proposed in three main trends: solving the voltage regulation, decreasing the component stress and shrinking the converter size. The authors in [1] proposed a SC converter where the VCR follows Fibonacci series, which since then has been considered the first brick in FSC development. Later, the the-

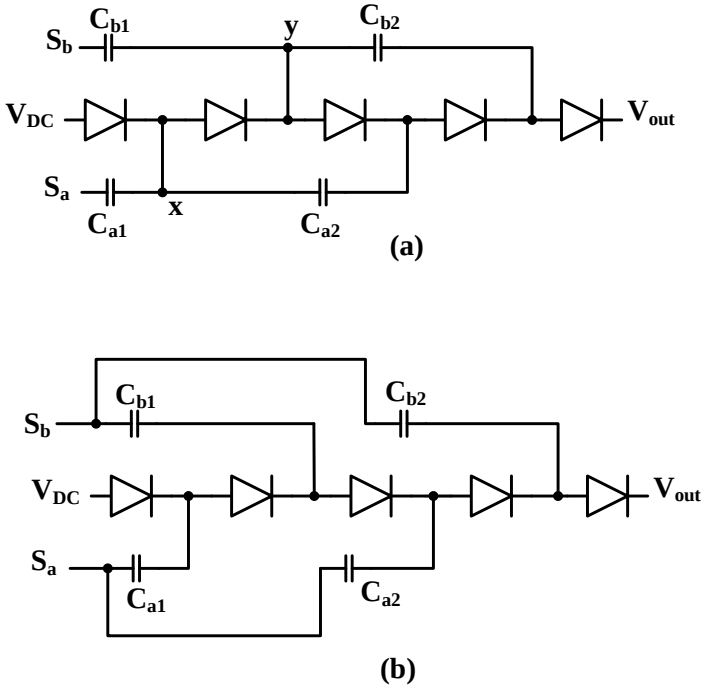


Figure 1.5: (a) Cockroft-Walton multiplier, (b) Dickson charge pump.

oretical limits of SC converter is proved in [2], resulting in two important theorems which help to set guidelines for developing SC converters. This is well-known as the SC fundamental limit theory. Also, FSC has been proved to have the least number of number of flying capacitors and switches to implement specific VCR, which lends itself to high power density applications. Multi-phase FSC can be also implemented to achieve higher and/or balanced VCR [9, 10], and the performance limits of multi-phase can be found in [11]. However, multi-phase requires complicated control unit compared to a simple two on-off states control in the two-phase FSC converter. Therefore, two-phase FSC converter will be considered throughout this work.

1.3 Research Scope and Contributions

The aim of this work is to present theoretical analysis of the SC converter, investigate the multi VCR SC synthesis, and discuss the design of a variable FSC converter in discrete and IC implementations targeting low power applications. The contributions of this dissertation can be summarized in the following:

1. Generalizing the SC fundamental limit theory.

2. Proposing a novel algorithm to synthesize variable FSC converters. To the best knowledge of the author, this is the first generic method to configure a variable FSC converter. An open-source tool is built based on this algorithm to promote the FSC use.

3. Proposing design procedures and optimization to implement FSC converter in low power applications for both discrete and IC implementation.

4. Proposing an IC controller with charge recycling technique to minimize the parasitic charge loss in IC FSC converter. Ideally, this technique decreases the parasitic capacitors power loss by 50%. The concept of charge recycling is not new but implementing this technique to FSC without transforming the FSC to interleaved structure is proposed here.

1.4 Report Organization

The rest of the report is structured as follows. In Chapter 2, we present the proposed generalized equation to the SC fundamental limit. Synthesizing FSC converters is discussed in Chapter 3 and the proposed algorithm is presented. In Chapter 4 and 5, we present the

design and implementation of discrete and integrated FSC converter, respectively. Finally, the report is concluded and future work is provided in Chapter 7.

Chapter 2

SC Converter Fundamental Theory

In this chapter, the fundamental limit theory in SC converter is introduced and studied. This theory is insufficient to determine the accurate boundaries for all negative VCRs in a SC converter. This work extends the theory to all possible cases of SC converters resulting in a general form[1]. The proposed theory in this chapter will be used later in synthesizing FSC converter.

2.1 Introduction

The fundamental limit in SC converter design which was proved in [2] is a well-known theory in the literature. The limit creates the foundation for SC converters design and synthesis. The fundamental limit theory consists of two theorems that define the voltage-conversion-ratio ($VCR = V_{out}/V_{in}$) boundaries for k flying capacitors in a SC converter, and the minimum number of switches to realize that converter. The first theorem is the main concern in this work. It states that for k flying (pumping) capacitors in an SC converter, the numerator and denominator of achievable VCR follow the Fibonacci series. They are bounded by 1 as the minimum limit and F_{k+2} as a maximum limit, as shown in the following

[1]The work presented in the chapter has been published in IEEE Transaction of Power Electronics [12].

equation:

$$\frac{V_{out}}{V_{in}} = \frac{P}{Q}, \tag{2.1}$$

where $1 \leq (P, Q) \leq F_{k+2}$, k is the number of flying capacitors in the circuit and F_k is the k^{th} Fibonacci number found in the Fibonacci series, $F = (1, 2, 3, 5, 8, 13, 21...F_k)$. The SC converter that has VCR follows or implement this limit is called FSC converter.

This fundamental limit is a powerful basis to minimize the effort of designing and implementing new SC converter topologies. It also helps providing a figure of merit to compare between different topologies in terms of achievable VCR and element counts. However, this limit only discusses the positive VCR boundaries and it does not explore the negative VCR boundaries which is considered as a first limitation. In this paper, we propose a general expression that overcomes this limitation and sets the boundaries for all possible VCRs.

The second limitation of the fundamental limit arises from the focus on single-input-single-output structure only. However, the multiple-input-multiple-output (MIMO) SC converter structures is desired in some applications. Extending the fundamental limit in (2.1) to include MIMO concept leads to provide a truly generic theory of the fundamental limit. This chapter is intended to explore and study these two limitations and propose generic expressions in both cases using FSC topology because it is the best to represent the theory. Examples of different cases and the practical implications are also discussed to verify the theory.

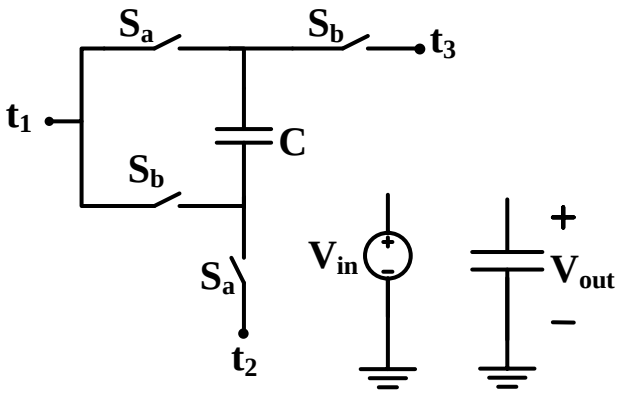
2.2 General SC Fundamental Limit

In some applications, negative output voltage polarities are desired. In this case, however, the fundamental limit fails to define the real boundaries that SC converter can achieve for the negative VCR. Generalizing the fundamental limit to cover all possible combinations of VCR is needed. The following expression divided the VCR in two regions, positive and negative. In both, the VCR still follow the Fibonacci series but the boundaries are different. As (2.2) describes,

$$\frac{V_{out}}{V_{in}} = \begin{cases} +\frac{P}{Q} & 1 \leq max|Q,P| \leq F_{k+2} \\ -\frac{P}{Q} & 1 \leq max|Q,P| < F_{k+2} \end{cases}, \tag{2.2}$$

negative VCRs are less than positive VCRs for the same converter. Note that, P/Q should be represented in their simplest form, for example $4/4$ is considered as $1/1$. The conditions in (2.2) are used to estimate the absolute minimum number of flying capacitors for desired VCR. More details about the practical implication of this expression are presented below.

To better understand the expressions presented in (2.2), let us illustrate by using an FSC converter with one flying capacitor, shown in Fig. 2.1. The flying capacitor can be connected to V_g, V_o or ground through the terminals $t_1 - t_3$. This converter can achieve $(1/2, 1, 2)$ VCRs neglecting the sign, which can be found using (2.1). The negative VCRs were left out as a default, assuming that this converter is capable to achieve $(-1/2, -1, -2)$ voltage conversion, which is incorrect. In fact, (2.2) reveals that with one flying capacitor, the converter can achieve only one negative VCR, which is -1. The look-up-table (LUT) for all possible terminal connections is presented in Figure 2.1, showing that this converter can achieve four distinct VCRs in total, $(-1, 1/2, 1, 2)$.



VCR	t_1	t_2	t_3
2	V_g	0	V_o
1	V_g	V_g	V_g
1/2	V_o	0	V_g
-1	0	V_g	V_o

Figure 2.1: One cell FSC converter.

On the other hand, the minimum number of flying capacitors needed to achieve other negative VCRs $(-2, -1/2)$ can be found using (2.2). In this case, it can be found that a Fibonacci number of two or greater is required because $\max|P, Q|$=2. Hence, $F_4 = 3$ is the right limit for this converter, meaning two flying capacitors are needed to achieve the missing VCRs. Yet another example, if a $(-1/4)$ Fibonacci SC converter needs to be designed. Applying the above steps resulted in $F_5 = 5$, which means the converter needs at least three flying capacitors. The design procedure has two steps:

1. Defining the real boundary limit using (2.2), i.e F_{k+2}.

2. Finding the number of required flying capacitors, which is k.

Spice simulation was conducted using ideal switches with $R_{ds_{on}}$=10$m\Omega$, f_s=500kHz and 15μF flying capacitor. The MOSFET based switches are turned on and off, using 50% duty-cycle complementary non-overlapping square signals to avoid shoot-through states. All possible VCRs were plotted in steady-state and depicted in Figure 2.2. The simulation result agrees with the proposed theoretical expression. One note here, in case if the summation of P and Q is not a Fibonacci number, the next Fibonacci number is selected. For instance,

using $VCR = -1/3$, the summation of absolute values of the numerator and denominator is four which is not a Fibonacci number. Thus, $F_5 = 5$ is assigned as a limit for this converter instead of four.

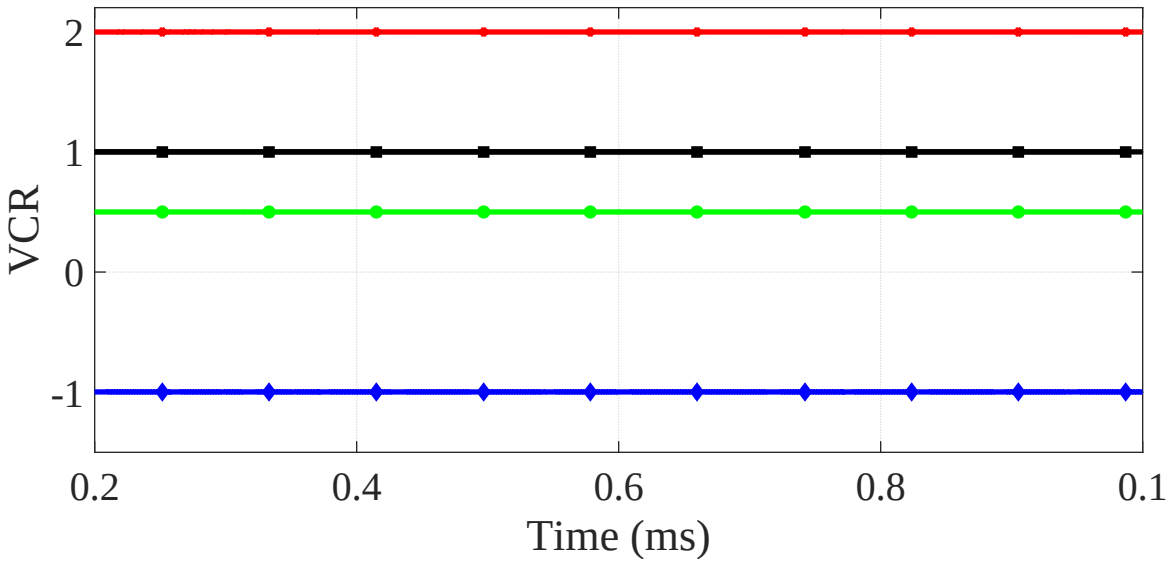


Figure 2.2: VCRs for one flying capacitor FSC converter in steady state.

2.3 MIMO SC converter

The MIMO SC converter and its special cases, the single-input-multiple-outputs (SIMO) and the multiple-input-single-output (MISO), are discussed here. As mentioned earlier, some applications require multiple outputs generated from one or multiple inputs, like the power management in microprocessors [13]. Usually, different DC-DC converters are employed to generate these different output levels. On the other hand, SIMO SC converters can do the job effectively achieving a real compact solution. Considering MISO SC converter implementation, a circuit for low power energy harvesting is used as an example. In this circuit, a single point-of-load is usually powered by multiple ambient sources to harvest more power. It can either be implemented by using different conventional SC converters,

or by simply using the MISO SC converter which offers better solution in terms of power density. However, synthesizing these converters without knowing the VCR boundary limits is a tedious job. MIMO implementation is proposed in this paper by employing the terminal weight concept found in [14]. Although MIMO implementation can be extended to all SC converter topologies, only the MIMO Fibonacci SC converter is considered because the interest here is to investigate the fundamental limit theory.

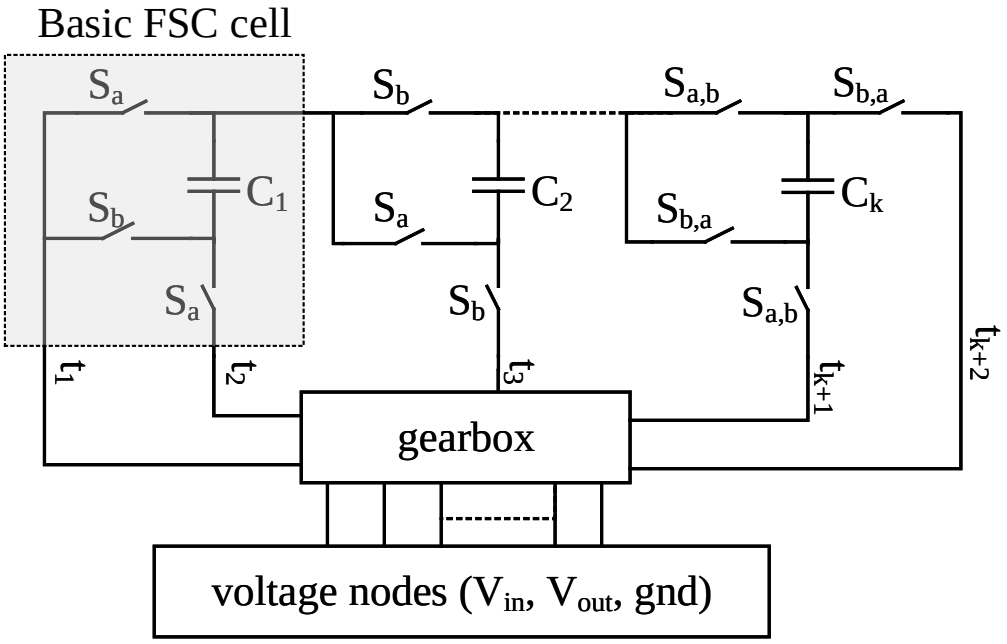


Figure 2.3: General structure for FSC converter.

The general structure of the MIMO FSC converter is depicted in Figure 2.3. It consists of two main blocks: the converter core, which is composed of FSC cells, and a pool of voltage nodes. The voltage nodes are connected to the core using terminals. The number of these terminals depend on the number of available FSC cells in the core. For instance, the number of terminals in k cells FSC converter equals $k + 2$. These terminals are assigned a weight that depends on its position in the circuit. There are four conditions need to be met to

assign the terminal weight and achieve FSC converter structure [14]. These conditions are as follows:

1. $w_1 = F_{k+2}$,
2. w_{k+2}=-1,
3. $\sum_{i=1}^{k+2} w_j = 0$,
4. $|w_j| = (1, 1, 2 \ldots F_{k+2})$.

The first condition implies that the first terminal (t_1) has a positive weight equals to the maximum achievable VCR, which is F_{k+2}. The other terminals are assigned negative weights using the *b-d* conditions. Note that all terminal weights follow the Fibonacci series as suggested in step (4).

Suppose that the MIMO FSC converter consists of n inputs and m outputs. With careful terminal weight assignment, the following equation relates the input and output voltages, where n+$m \leq k + 2$:

$$\sum_{i=1}^{n} w_{v_{g_i}} v_{g_i} + \sum_{j=1}^{m} w_{v_{o_j}} v_{o_j} = 0. \tag{2.3}$$

This equation deals with MIMO realization. It defines the possible output voltage levels for MIMO converters. It incorporates all conditions mentioned above. In the following, a detailed procedure is presented to show how to use (2.2) and (3.1) in designing and realizing SC converters.

Suppose we have a system that requires two multiple output levels of 1.8V and 3.3V from one input source, which is common in power management circuits. There are two

approaches to design a DC-DC converter for this application, either using two different DC-DC converters or using the MIMO converter design concept. The latter has less component counts and makes it the optimal choice for this application. The steps to design the MIMO converter are as follows:

1. Defining how many inputs and outputs which allows us to find minimum limit for k.
2. Determining the maximum VCR using (2.2). Then, find new k and choose the highest value for k amongst the two steps (1) and (2).
3. Assigning terminal weight following the conditions listed in section 2.3.
4. Connecting the voltage nodes to terminals based on their weight.

Let us use the example stated earlier to verify the design procedure steps. We have an input voltage of 1V and we need to get 1.8V and 3.3V outputs. So, following the same design steps:

1. n=1, m=2 which implies 1+2 $\leq$ k+2, and consequently, k need to be greater or equals one.
2. Maximum VCR here is 3.3 which is close to 7/2, Using equation (2.2), k greater than or equals four is required which corresponds to F_6=8. Therefore, the circuit needs at least four flying capacitors and six terminals (Figure 2.4) using FSC converter topology.
3. Terminal weights are assigned as following:
   (a) $w_1 = F_{k+2} = 8$ and $w_6 = -1$.
   (b) $w_2 + w_3 + w_4 + w_5 = -7$, using a trial and error approach, $w_2 = -3$, $w_3 = -2$, $w_4 = w_5 = -1$. Note that, these terminal weights should follow the Fibonacci

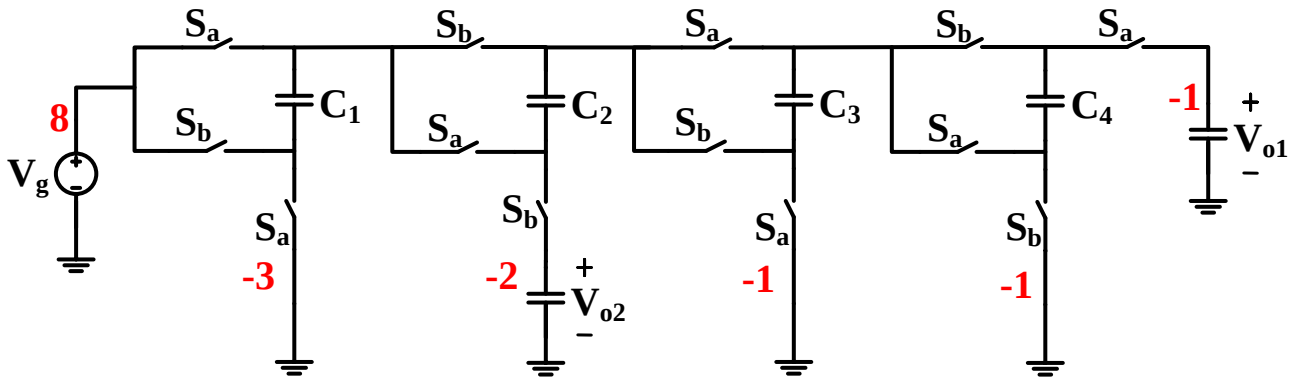


Figure 2.4: Circuit realization for FSC converter with dual outputs.

series as stated earlier. For convenience, the terminal weights are also highlighted next to each terminal in Figure 2.4.

4. Output voltages relation is examined which helps in assigning the terminals. Detailed discussion of this step is to follow.

In this example, we have $V_{o_2} \simeq 2V_{o_1}$ as a design requirement (1.8V, 3.3V). Accordingly, terminals need to be selected to guarantee this relation between the outputs. For instance, if V_{o_1} is connected to the second terminal in this converter which has a weight of three (Figure 2.4), the second output needs to be connected to a terminal that provides a weight of six which is impractical with this converter. In this case, V_{o_2} is connected to the third terminal which has a weight of two and V_{o1} can connected to any of the last three terminals because they have same weights, w_4, w_5 and w_6. For convenience, V_{o_1} is connected to the last terminal. The input is connected to the first terminal, because positive VCRs are required. Using (3.1), $8v_g = 2v_{o_2} + v_{o_1}$ which implies $8v_g = 5v_{o_1}$ and $8v_g = 3v_{o_2}$.

Spice simulation was conducted for the example discussed above. Figure 2.4 shows the circuit realization where four 15μF flying capacitors were used. The output capacitors are

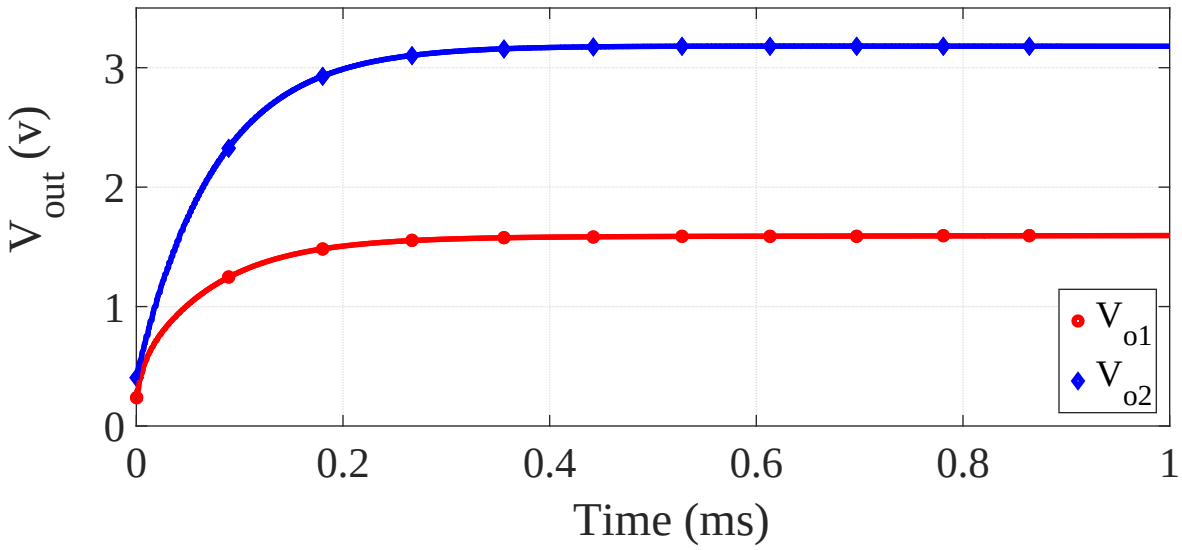


Figure 2.5: Output voltage waveforms for dual outputs FSC converter.

kept high to maintain small output voltage ripple. The converter is operated using 50% duty-ratio complementary non-overlapping gate signals, S_a and S_b, in open loop control. These gate signals are provided using 500kHz pulse clock generator. Ideal switches with $R_{ds_{on}}$=10$m\Omega$ are used as power switches. The output voltage waveforms of 3.2V and 1.6V are achieved using an input voltage of 1V. These converters outperform the single output voltage converter in terms of complexity and component count.

2.4 Summary

In this chapter, two limitations in SC converter fundamental limit were discussed, and general expressions to overcome these limitations have been proposed. The design procedure using these expressions was introduced, which helps in designing SC converter for a variety of applications. The MIMO FSC converter has been reported for the first time in literature and the same concept can be extended to other SC topologies. Simulation results show an agreement with the theoretical analysis.

Chapter 3

SC Converter Synthesis

Synthesizing SC converter is a tedious and time consuming job and usually performed in an ad-hoc approach. This chapter discuses existing works to overcome this problem. Then, we propose an efficient algorithm to realize multi VCR FSC converter which is expected to be useful for wide input applications[1].

3.1 Related Work

Generally, there are many ways to configure the SC converter. For instance, if one FSC cell of Figure 2.1 is considered, there are three possible combinations and it increases to seven combinations if we add another FSC cell. Considering FSC converter with k flying capacitors, there are $F_{k+2}(F_{k+2}-1)+1$ possible combinations. So, synthesizing the FSC converter is not trivial and considered a major challenge in SC converter design compared to SI counterpart. A generic SC structure has been studied in [16] but the proposed synthesizing technique is not systematic and considers only one condition: whether the converter is designed for step-down or step-up. Details of configuring specific VCR were not discussed. Different approaches and algorithms were proposed to tackle the SC synthesis problem [14, 17–19] which are focused to realize the FSC or its variants.

In [17], an interesting approach to configure SC converter was proposed by connecting all

[1]Part of the work presented in this chapter has been published in the proceedings of IEEE Workshop on Control and Modeling for Power Electronics (COMPEL), 2017 [15].

capacitor negative plates to the ground in the charging phase, and hence it is known as All Negative terminal connected To Zero topology (ANTZ), and then configuring the capacitors to deliver the charge to the output based on optimal vector path from the ANTZ tree. The ANTZ tree is composed of two main levels, the voltage source level, usually (V_{in},V_{in}) or simply (1,1), and flying capacitor levels. Each flying capacitor level is assigned a vector based on the possible voltage appears in the flying capacitor terminals (V_{c_i},Φ_1,V_{c_i},Φ_2). Using ANTZ, many SC topologies can be configured including Fibonacci topology. However, this topology targets only step-up converters with non-fractional VCR and cannot be considered as a generic model for SC converter synthesis. In addition, composing the ANTZ tree is quite complicated especially for large number of flying capacitors and hence the design procedure is not straightforward.

The algorithm found in [18] is quite simple but not effective in finding all configurations for FSC converter. As an example, using this algorithm a $VCR = 5/3$ was found to be realizable in only three configurations (Figure 6 in [18]). However, it can be realized in four configurations using the proposed algorithm in this work, see Table 3.1. Details of the proposed algorithm is discussed Also, assigning capacitor polarities needs to be done by inspection which cannot be automated. In addition, the configuration table grows with the increase in the number of flying capacitors which complicates the synthesis process.

The third algorithm we want to discuss here is proposed in [19]. It takes two steps to synthesize the SC converter: (i) generating fundamental VCR using basic FSC converter and (ii) summing these fundamental VCR to generate the desired one. This method works the best with high VCR as it has less voltage stress than conventional FSC converter. However, it fails to maintain the minimum number of flying capacitors required for specific VCR based on the fundamental limit (2.2). Basically, it uses extra capacitors in the second part of the

Table 3.1: All possible realizations for FSC with VCR=5/3

Terminal	t_1	t_2	t_3	t_4	t_5
Weight	5	-2	-1	-1	-1
SPTT code	1	0	2	2	2
	1	2	0	0	2
	1	2	0	2	0
	1	2	2	0	0
Final SPTT code	1	2	0	0	2
Number of Switches	0	0	0	0	0
Voltage nodes	V_{in}	V_{out}	gnd	gnd	V_{out}

system to perform the addition. Also, it can be used only for an integer step-up SC converters like the ANTZ topology.

Recently, an algorithm to evaluate the SC converters is proposed in [20]. The evaluation is based on charge-multiplier concept which will be discussed thoroughly in the following chapters. However, their claim to be first attempt towards solving the SC synthesis is misleading as we already discussed some prior works in the literature. Moreover, the work in [20] shows only the ability to find charge-multiplier vectors for evaluation purposes, but the synthesis approach is not clear. For example, there is no limits for the number of required cells for specific VCR. Also, the algorithm targets a one-VCR applications and hence is not practical for multi-VCR. Despite all of that, the generic nature of the approach can be credited compared to topology-dependent approaches.

A canonical model was proposed in [14] to solve the realizability problem of FSC converter. This model was successful to synthesize the FSC converter to achieve any VCR including fractional and negative VCR. It proposed a gearbox circuit that configures the converter such a way to be able to perform certain VCR. Each flying capacitor terminal is assigned a weight based on Fibonacci series. Based on the terminal's weight and specified VCR, the gearbox circuit directs each terminal to specific voltage node (V_{in}, V_{out}, gnd) via

switches. However, it was developed only for a specific VCR and did not target multi VCRs which is sometimes desirable. Here, we extends the canonical model to synthesize a truly variable FSC converter by adjusting the gearbox switches. Details of the proposed algorithm is discussed in the following section. Table 3.2 summarizes the synthesis techniques with general comparison which concludes the effectiveness of the proposed algorithm in this work where a general FSC that provide any VCR can be synthesized.

Table 3.2: Comparison of SC converter synthesis techniques

	COMPEL'14 [14]	TCAS-II'07 [17]	COMEL'15 [18]	EDSSC'09 [19]	This work
Complexity level	Low	High	Avg.	Avg.	Low
Capacitor count	min.	min.	min.	High	min.
Variable VCR	No	Yes	No	No	Yes

3.2 Proposed FSC Synthesis

The canonical model proposed in [14] is shown in Figure 2.3. It consists of Fibonacci converter cells and a gearbox to change the voltage conversion requirement. The synthesis approach is approved mathematically, and hence it is used here as a basis to help synthesizing variable FSC converter. The Makowski general SC converter starts with selecting the minimum number of capacitors to achieve the maximum VCR by using equation (2.1). This step determines the number of converter cells and the number of the terminals to the gearbox.

The second step involves weight function assignments based on the VCR, this step is done using equation (3.1). It is assumed that each path in the gearbox has a fictitious single pole triple throw (SPTT) switch that connects the converter core to one of the three voltage nodes (V_{in}, V_{out}, gnd) in the blue box. These terminals carry some weight depending on the

Fibonacci series, $F = (1, 1, 2, 3, 5 \ldots F_{k+2})$, either in positive or negative values. Equation (3.1) is a condition that ensures all weight function values are part of Fibonacci series as follow:

$$w(t_1) + \sum_{i=2}^{k+2} w(t_i) = 0, \tag{3.1}$$

where $w(t_1)$=F_{k+2}, $w(t_{k+2})$=-1 and $w(t_k)\subset[-F_{k+1}, -F_k .... -2, -1, -1]$. Finally, the SPTT switch is assigned a code $(0, 1$ or $2)$ where $0, 1$, and 2 means that the terminal is connected to ground, V_{in} and V_{out}, respectively. These steps allow synthesizing the SC Fibonacci converter for any VCR. Examples of positive and negative VCRs with thorough explanations and mathematical proof can be found in [14]. So, this canonical converter is very efficient in synthesizing SC converters but when considering a multi-VCR, an additional step is required to ensure the optimal realization. In fact, the converter in Figure 2.3 may be extended to other modular structural SC like serial-parallel, which was already covered in [14] and called semi-canonical, ladder and other topologies. Also, this method can be extended to multiple inputs and/or outputs which may find its way to different applications, such as harvesting energy from multiple ambient sources. However, these extensions are out of the scope of this work. The proposed algorithm to synthesize a variable FSC converter takes the following steps:

1. All three steps mentioned in section 3.2;
    (a) capacitor requirements.
    (b) terminals weight function assignment.
    (c) SPTT code assignment.

2. Unique/optimal realization assignment.

The first step including (a)-(c), is already discussed in chapter 3. For the second step, the algorithm will search for the minimum number of state transitions in each realization compared to a reference set by the code, usually the SPTT code that corresponds to the maximum VCR. The number of state transitions here represents the number of switches in the gearbox circuit. Note that, these switches configure the SC converter in such a way that it can achieve all pre-assigned VCRs and hence they are considered the main attribute to the complexity level of the controller.

The whole algorithm flow chart is depicted in Figure 3.1. In this code, the user needs to specify the VCRs and degree of freedom, i.e resolution. The code will generate the minimum number of capacitors and terminals for each VCR using (2.2). Then, the weight functions are next to be determined. After that, the SPTT code for each realization is found, and an SPTT code reference is set by the code which is an important step to ensure all VCRs are realizable with the final solution. Next, the code allows to compare all SPTT codes to the reference and return SPTT codes that have a minimum number of state transitions. Note that, a state transition occurs whenever there is a change in the SPTT code for each terminal from (0 to 1), (0 to 2), (1 to 2), (2 to 1), or (2 to 0). The final SPTT code is found to be the optimal realization in terms of number of switches in the gearbox. The SPTT code is $m \times t$ matrix where m represents the number of realizable VCR and t represents the number of terminals in the gearbox.

In some cases, the VCR required by the used can be relaxed, i.e 0.75 is assigned instead of 0.76, which allows realizing the converter by less number of capacitors. Therefore, to account for this degree of freedom, the resolution feature is added. It simply allows the algorithm to search for optimal VCRs that have the least number of capacitors. For exam-

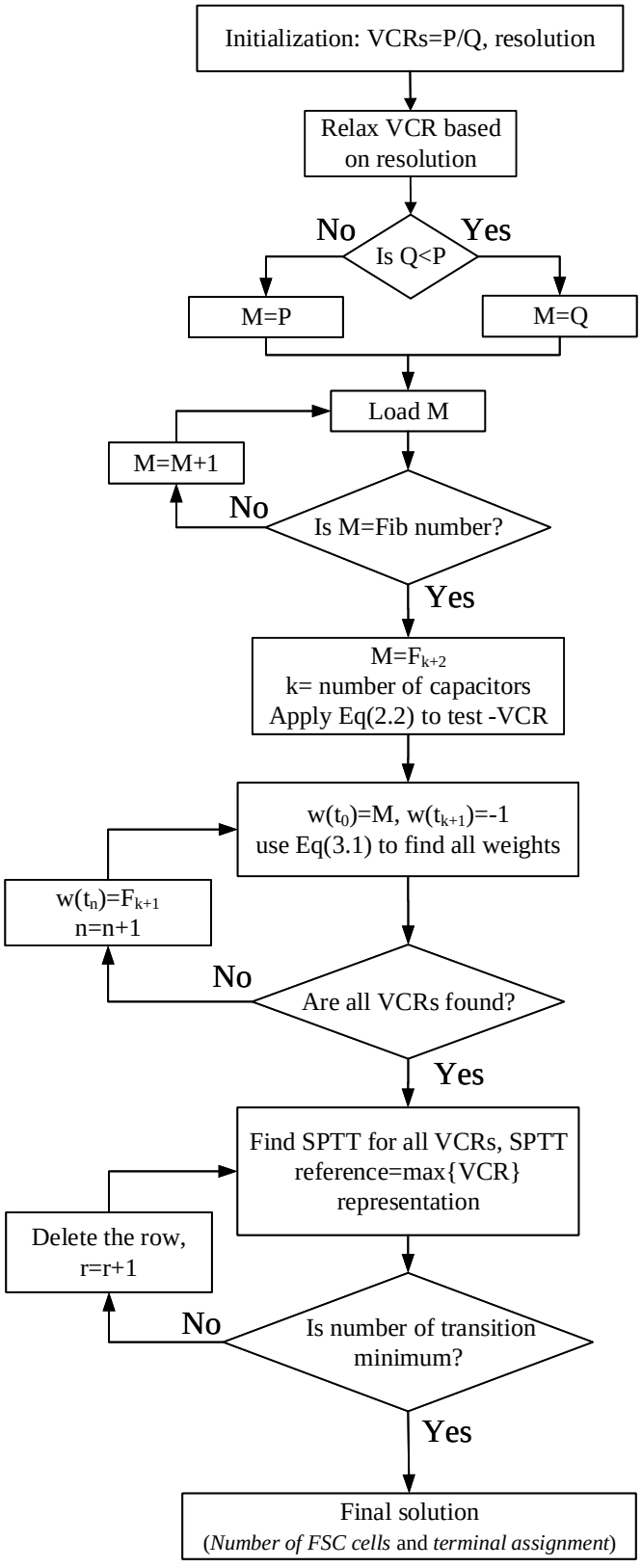


Figure 3.1: Flow chart for the proposed algorithm.

ple, for VCR=0.76 and zero resolution, the code will assign seven flying capacitors because 0.76=19/20 in the simplest form. However, a resolution of 0.01 would relax the VCR to 0.75 and hence, only three flying capacitors are assigned. In fact, this feature allows finding all VCRs and helps the user to optimize the number of flying capacitors based on the specifications. The algorithm is implemented in MATLAB, and is made available as an open-source tool, called *FSC Synthesizer*. Using this open-source tool, the user can realize any VCR for FSC more efficiently, saving the time and effort required to go through trial and error route. In the following sections, some cases are presented to illustrate the workflow of *FSC Synthesizer*.

3.3 Case Study and Results

In this section, three cases will be discussed. These cases cover all types of FSC converter, single VCR and variable VCR. The last example shows the effectiveness of the proposed approach to simplify the controller circuit of an FSC converter.

3.3.1 FSC Converter with VCR=30

The first example is to implement an FSC that has a single VCR equals to 30, which is one of the cases discussed in [14]. Using the proposed method, all solutions are validated and shown in Table 3.3. In addition, the proposed method selected the optimized SPTT code as shown in the Table which shows where the terminals are need to be connected. It also can be seen that no gearbox switches are needed which is expected in single VCR FSC converter.

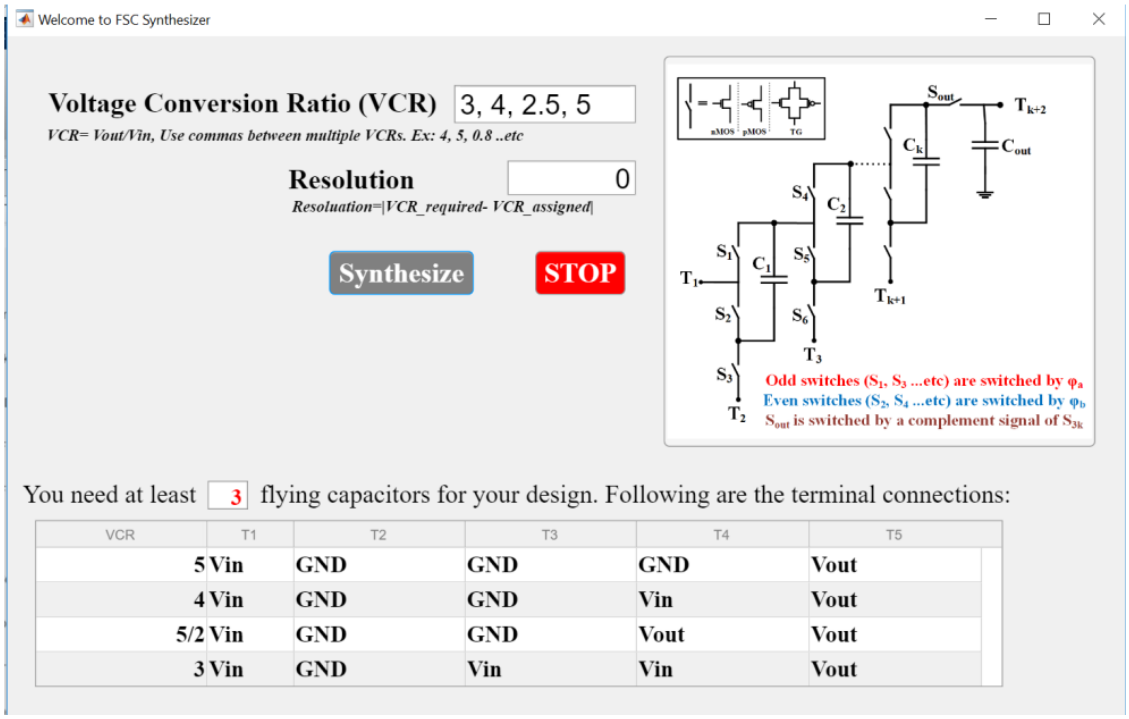
Table 3.3: All possible realizations for VCR=30/1

Terminal	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9
Weight	34	-13	-8	-5	-3	-2	-1	-1	-1
SPTT code	1	0	0	0	0	1	2	1	1
	1	2	0	0	0	1	1	2	1
	1	2	0	2	0	1	1	1	2
	1	2	2	0	1	0	0	2	1
	1	0	0	0	1	0	2	0	1
	1	0	0	0	1	0	0	1	2
	1	0	0	0	1	0	2	1	0
	1	0	0	0	1	0	1	0	2
	1	0	0	0	1	0	1	2	0
Final SPTT code	1	0	0	0	1	0	0	1	2
Number of Switches	0	0	0	0	0	0	0	0	0
Voltage nodes	V_{in}	gnd	gnd	gnd	V_{in}	gnd	gnd	V_{in}	V_{out}

3.3.2 Variable FSC Converter with VCR=5, 4, 3, 5/2

The second example considers the application discussed in chapter 1, where a variable FSC is required. As mentioned earlier, the miniaturized solar cell has a typical open voltage of 0.3∼0.6V and we want a regulated output voltage of 1.5V. Therefore, the VCR=5, 4, 3 and 5/2 are required. These VCRs are fed to the proposed code in section 3.2 to get the optimal circuit realization. This application needs only three flying capacitors using FSC topology. The SPTT gearbox code and number of switches are presented in Table 3.4. In this example, terminals 1, 2, and 5 preserve only one value along all circuit states which means *no switch* is required and the terminal is connected directly to its corresponding voltage node. In third terminal, however, the rows are toggling between *zero* and *one* which means *two switches* are required. For the forth terminal, the rows are changed between all voltage nodes which means *three switches* are required. Also by using *FSC synthesizer* as shown Figure 3.2, this converter requires three flying capacitors and five transistors for the gearbox control. Note that, due to the presence of all VCR in their simplest form, a zero resolution is chosen. The

SC converter realization is drawn in Figure 3.3. Note that, $S_{g1} - S_{g5}$ transistors[2] configure the SC converter to change VCR if needed. Also, they are the only transistors that are controlled in closed loop, all other switches are driven by simple two complementary non-overlapping clocks that are enabled when the converter starts up. This converter will be used in next chapters as a case study to implement variable FSC in both discrete and IC implementation.



VCR	T1	T2	T3	T4	T5
5	Vin	GND	GND	GND	Vout
4	Vin	GND	GND	Vin	Vout
5/2	Vin	GND	GND	Vout	Vout
3	Vin	GND	Vin	Vin	Vout

Figure 3.2: Terminal assignments using *FSC Synthesizer* for variable FSC with VCR=5, 3, 4, 5/2.

3.3.3 Variable FSC Converter with VCR=1, 3/4, 2/3

The complexity of the converter control circuit is also another issue in SC converter design and can be related to the number of driving signals generated in close loop. Therefore, the less number of closed loop driving signals the simpler is the control circuit. We claim that

[2]Note that, M_x and S_x are exchangeably used throughout this dissertation.

Table 3.4: Optimized realization for variable FSC with VCR=5, 4, 3, 5/2

Terminal	t_1	t_2	t_3	t_4	t_5	Gain
Weight	5	-2	-1	-1	-1	NA
Final SPTT code	1	0	0	0	2	5
	1	0	0	1	2	4
	1	0	1	1	2	3
	1	0	0	2	2	5/2
Number of Switches	0	0	2	3	0	NA
Voltage nodes	V_{in}	gnd	V_{in} gnd	V_{in} V_{out} gnd	V_{out}	NA

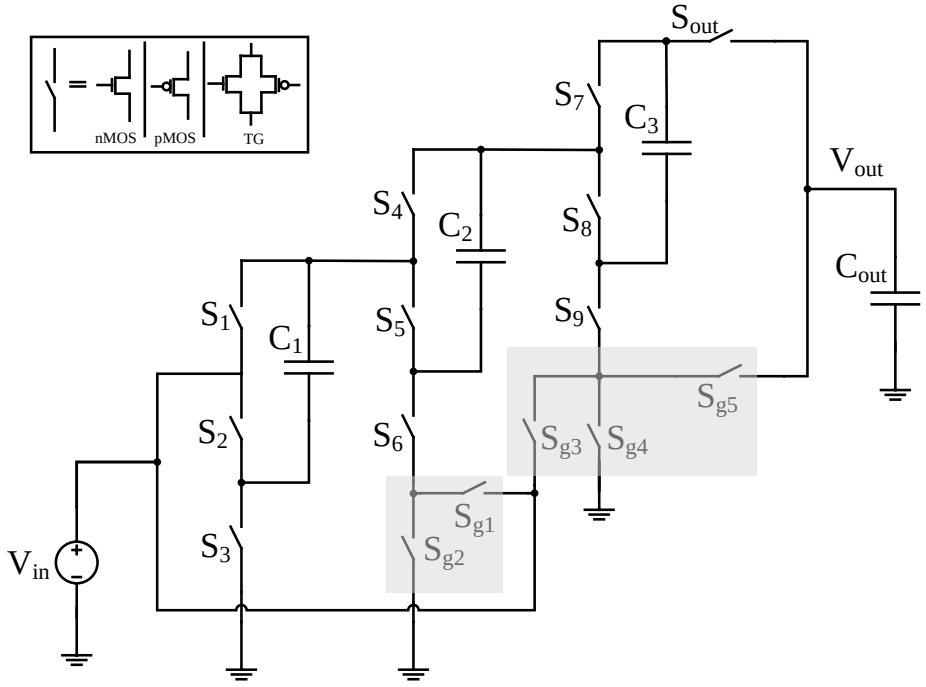
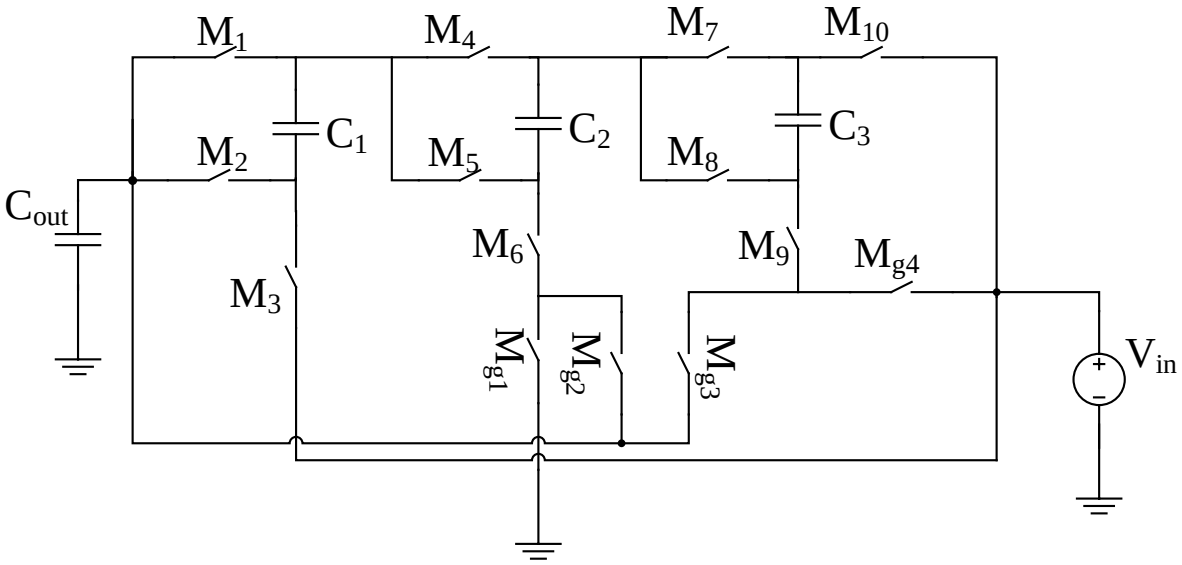


Figure 3.3: Variable FSC with VCR=5, 3, 4, 5/2.

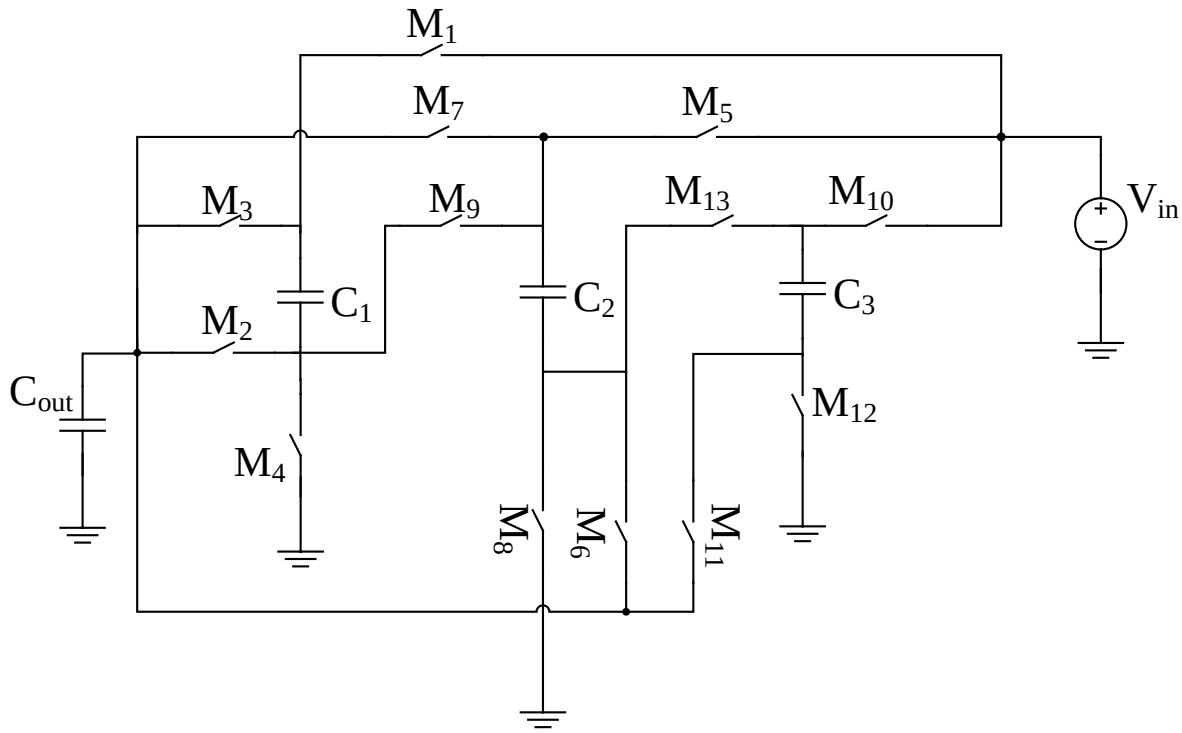
by using the proposed algorithm, the simplest controller circuit is achieved. We illustrate by comparing the control circuit of a buck converter that has three VCR $(1, 3/4, 2/3)$ implemented using our method and the same converter in the literature implemented in ad-hoc way [21]. Implementing this buck converter using our methodology resulted in a circuit shown in Figure 3.4(a) with an LUT shown in Table 3.5. In [21], three capacitors and 13 switches were used to realize a buck converter with $VCR = (1, 3/4, 2/3)$ with an LUT control signals shown in Table 3.6, their circuit realization is redrawn in Figure 3.4(b). With a close look to the switch signals in Tables 3.5 and 3.6, one can see that ten switches *(all except* M_1, M_3 *and* M_5*)* of the circuit in Figure 3.4(b) need to be controlled in a closed-loop, i.e. they are not just a simple on-off *(two states)* control. On the other hand and for the same VCR, only four switches ($M_{g1} - M_{g4}$) are controlled adaptively as illustrated in Table 3.5 using the proposed method. Not only that, but also each two switches among the four are complementary, $M_{g1} = \bar{M}_{g2}$ and $M_{g3} = \bar{M}_{g4}$. Thus, only two signals are required to control the gearbox switches. Other switches, M_{1-10}, are controlled by the non-overlapping clocks (ϕ_1 and ϕ_2) directly. This greatly simplifies the converter control unit.

Table 3.5: LUT for converter synthesized by proposed method

VCR	1	3/4	2/3
$M_{1-10(odd)}$	ϕ_1	ϕ_1	ϕ_1
$M_{1-10(even)}$	ϕ_2	ϕ_2	ϕ_2
M_{g1}	0	1	1
M_{g2}	1	0	0
M_{g3}	1	1	0
M_{g4}	0	0	1



(a)



(b)

Figure 3.4: Buck SC converter with VCR=1, 3/4, 2/3: (a) FSC topology using proposed method. (b) Converter proposed in [21].

Table 3.6: LUT for converter in [21]

VCR	1	3/4	2/3
M_1	ϕ_1	ϕ_1	ϕ_1
M_2	0	ϕ_1	ϕ_1
M_3	ϕ_2	ϕ_2	ϕ_2
M_4	1	0	0
M_5	ϕ_1	ϕ_1	ϕ_1
M_6	0	ϕ_1	ϕ_1
M_7	ϕ_2	0	0
M_8	1	0	ϕ_2
M_9	0	ϕ_2	ϕ_2
M_{10}	0	ϕ_1	ϕ_2
M_{11}	0	ϕ_1	0
M_{12}	0	ϕ_2	0
M_{13}	0	ϕ_2	0

3.4 Summary

The SC converter synthesis problem is introduced and solutions are discussed. The proposed algorithm achieves an optimal SC realization for mulit-VCR in almost no time which makes it desirable as a fast tool to synthesize SC converters. As practical examples, three cases were presented. The proposed method also simplifies the converter control by decreasing the number of close loop driving signals. A comparison between the control method for one converter found in literature and the other synthesized in the proposed method is discussed. For the same number of VCRs, it is found that the control of the proposed one is much easier compared to the other.

Chapter 4

Reconfigurable FSC Converter: Discrete Design

This chapter aims to study the design and implementation of discrete FSC converter. Although multi-phase FSC converters provide more VCR as discussed earlier, the two-phases FSC are to be considered in this work due their simplicity in design and control. The discrete differs from the IC integration in terms of power loss analysis and components selection.

4.1 Theoretical Analysis

The SC converter equivalent circuit is shown in Figure 4.1. It consists of an ideal conversion term ($n = VCR$), and equivalent impedance (R_{eq}) which models all switch turn-on resistances and charge redistribution in the flying capacitors. The output voltage can be calculated using the following equation:

$$V_{out} = nV_{in}\frac{1}{1+\frac{R_{eq}}{R_L}}. \tag{4.1}$$

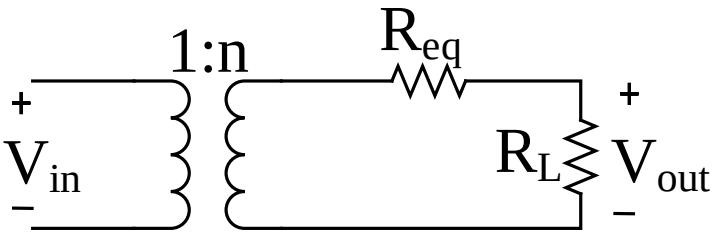


Figure 4.1: SC converter steady state model.

4.1.1 Converter Equivalent Resistance

There are enormous published works trying to improve the SC models. Some models are summarized and compared in recent work [22]. The model proposed in [23] will be utilized in this paper due to its generic nature and easy implementation for complex SC topologies like FSC. Also, it provides useful insight to component sizing and converter optimization.

There are two switching limits for R_{eq} as shown in Figure 4.2: slow switching limit (SSL) and fast switching limit (FSL) [23–26]. The slow switching occurs when the switching period (T_s) is less than the flying capacitor time constant ($\tau_c = RC_{fly}$), in other words $f_s < f_c$ as illustrated in Figure 4.2, and the switches in SSL region can be assumed to be ideal, i.e $R_{r_{on}} = 0$ and $R_{r_{off}} = \infty$. On the other hand, the fast switching spans the region where f_s is much higher than f_c, and R_{eq} is minimized. In fact, R_{FSL}, which is the converter impedance at FSL, is considered the minimum impedance value a converter can achieve. Nevertheless, the converter is usually operated around f_c or less to avoid high switching loss and achieve smooth charge transfer. In fast switching mode, the flying capacitor can be modeled as an ideal voltage source, which implies there is no charge loss in charging and discharging the capacitor or so-called charge redistribution loss [16]. To get an optimal equivalent resistance, both switching regions need to be considered. The converter impedance at SSL and FSL,

R_{SSL} and R_{FSL}, and the total converter equivalent resistor (R_{eq}) can be calculated as following:

$$R_{SSL} = \sum_{i=1}^{k} \frac{(a_{c_i}^2)}{C_i f_s}, \tag{4.2}$$

$$R_{FSL} = \sum_{j=1}^{m} \frac{(a_{r_j}^2) R_{on_j}}{D_j}, \tag{4.3}$$

$$R_{eq} = \sqrt{R_{SSL}^2 + R_{FSL}^2}, \tag{4.4}$$

where where f_s is the switching frequency, R_{on} is the switch turn-on resistance, D is the duty ratio of the gate signals which is normally equals 0.5, k is the number of flying capacitors and m is the number of switches. The a_{c_i} and a_{r_j} are the charge multiplier of the i^{th} capacitor and the j^{th} switch respectively.

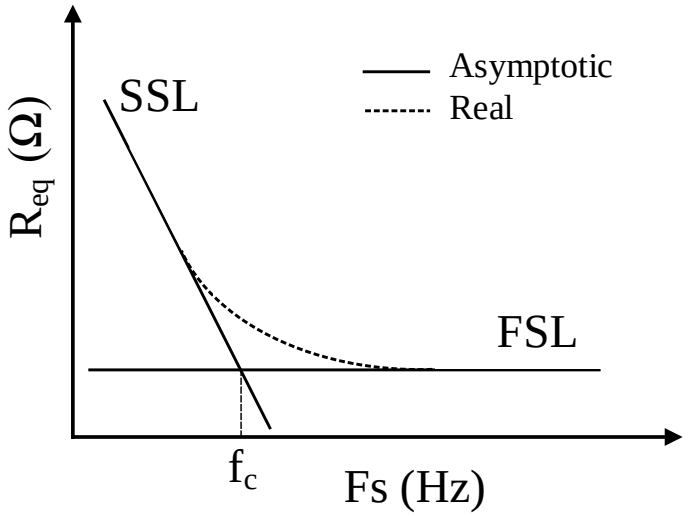


Figure 4.2: SC converter equivalent impedance vs switching frequency.

The charge multiplier vectors, a_r and a_c, relate the charge flows into the capacitor and switch to the output charge, meaning $a_{r_j} = q_{r_j}/q_{out}$ and $a_{c_i} = q_{c_i}/q_{out}$. The charge vectors are very useful in converter optimization as will be discussed later. To find the charge vectors, sub-vectors $a^1_{r,c}$ and $a^2_{r,c}$ which define the charge vectors in each phase, need to be determined by drawing the converter in each state and finding the charge in each element. Due to the charge conservation, the following equations; $q^1_{out} + q^2_{out} = 1$ and $a^1_{r_j,c_i} + a^2_{r_j,c_i} = 0$, helps identifying the charge quantity in each phase. Then, a_{c_i} can be found by taking the absolute value of $a^1_{c_i}$. Likewise, a_{r_j} can be determined by taking the corresponding nonzero element in $a^1_{r_j}$ and $a^2_{r_j}$.

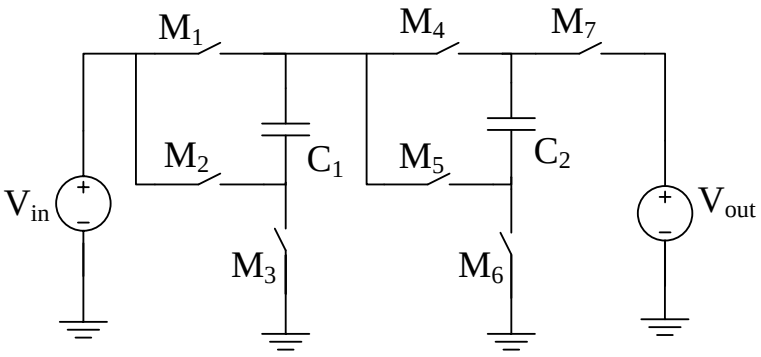
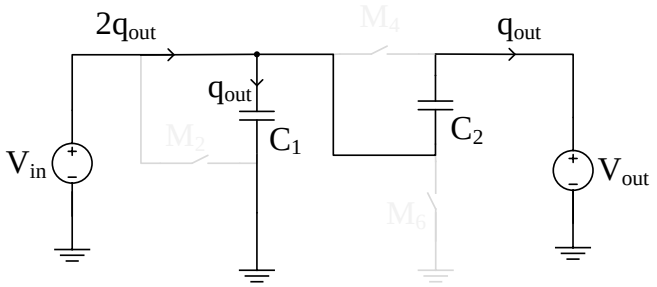


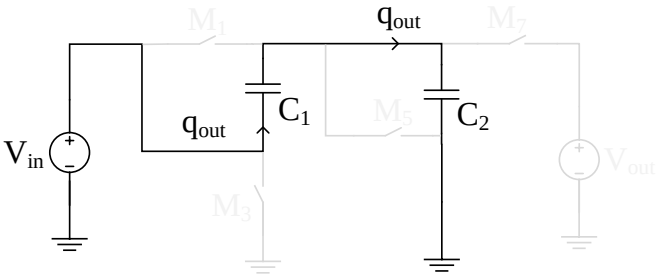
Figure 4.3: FSC converter with VCR=3.

To follow with theoretical analysis, an example of FSC converter with VCR equals three is shown in Figure 4.3. The converter has two states as shown in Figure 4.4, which will be used to compose $a^1_{c,r}$, $a^2_{c,r}$ and $a_{c,r}$ as following:

$$\begin{bmatrix} a^1_{c_1} & a^1_{c_2} \\ a^2_{c_1} & a^2_{c_2} \end{bmatrix} = \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}$$



(a)



(b)

Figure 4.4: FSC converter with VCR=3: (a) state I, S_a=1, S_b=0. (b) state II, S_a=0 S_b=1.

$$\implies a_c = \begin{bmatrix} 1 & 1 \end{bmatrix} \tag{4.5}$$

$$\begin{bmatrix} a_{r_1}^1 & a_{r_2}^1 & a_{r_3}^1 & a_{r_4}^1 & a_{r_5}^1 & a_{r_6}^1 & a_{r_7}^1 \\ a_{r_1}^2 & a_{r_2}^2 & a_{r_3}^2 & a_{r_4}^2 & a_{r_5}^2 & a_{r_6}^2 & a_{r_7}^2 \end{bmatrix} = \begin{bmatrix} 2 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 0 & 1 & 0 \end{bmatrix}$$

$$\implies a_r = \begin{bmatrix} 2 & 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix} \tag{4.6}$$

In this work, a blocking voltage vector is also introduced, $a_{v_{c,r}}$. This vector defines the blocking and rated voltages for the capacitors and switches with respect to the output voltage, $a_{v_{c,r}} = V_{c,r}/V_{out}$. To do this, we first find $V_{c,r}$ in terms of V_{in}, and then divide by VCR to get $V_{c,r}$ as a function of V_{out}. Also, we could find $V_{c,r}$ in terms of V_{out} in

one step by reversing the analysis. Note that, all previous analysis is related to the output voltage and charge. Therefore, we need $V_{c,r}$ to be as a function of V_{out} to be consistent and get a meaningful results that helps analyzing and optimizing the converter. For the switches, the blocking voltage is the maximum voltage which the switch can withstands without breaking out, and usually determined during the off state. Likewise, the blocking voltage for the capacitor is defined to be the maximum voltage across the capacitor in both states. Defining the blocking voltage vectors is very useful in power analysis calculation which will be discussed in the next section. As an example, let us consider the converter discussed earlier (Figure 4.3), $a_{v_{c,r}}$ can be found as following:

$$\begin{bmatrix} a^1_{v_{c_1}} & a^1_{v_{c_2}} \\ a^2_{v_{c_1}} & a^2_{v_{c_2}} \end{bmatrix} = \begin{bmatrix} 1/3 & 2/3 \\ 1/3 & 2/3 \end{bmatrix}$$

$$\implies a_{v_c} = \begin{bmatrix} 1/3 & 2/3 \end{bmatrix} \tag{4.7}$$

$$\begin{bmatrix} a^1_{v_{r_1}} & a^1_{v_{r_2}} & a^1_{v_{r_3}} & a^1_{v_{r_4}} & a^1_{v_{r_5}} & a^1_{v_{r_6}} & a^1_{v_{r_7}} \\ a^2_{v_{r_1}} & a^2_{v_{r_2}} & a^2_{v_{r_3}} & a^2_{v_{r_4}} & a^2_{v_{r_5}} & a^2_{v_{r_6}} & a^2_{v_{r_7}} \end{bmatrix} = \begin{bmatrix} 0 & 1/3 & 0 & 2/3 & 0 & 1/3 & 0 \\ 1/3 & 0 & 1/3 & 0 & 2/3 & 0 & 1/3 \end{bmatrix}$$

$$\implies a_{v_r} = \begin{bmatrix} 1/3 & 1/3 & 1/3 & 2/3 & 2/3 & 1/3 & 1/3 \end{bmatrix} \tag{4.8}$$

Finally and to have a concrete theoretical analysis, let us study the optimized converter expressions. The optimization procedure proposed in [24] explicitly derived the expressions of optimized R^*_{SSL} and R^*_{FSL} based on a_c and a_r respectively. This optimization minimizes

P_{loss} by sizing the flying capacitor and transistors according to a_c and a_r vectors. Therefore, R^*_{SSL} and R^*_{FSL} can be calculated as following:

$$R^*_{SSL} = \frac{1}{C_t f_s}(\sum_{i=1}^{k} a_{c_i})^2, \tag{4.9}$$

$$R^*_{FSL} = 2R_{on_t}(\sum_{j=1}^{m} a_{r_j})^2, \tag{4.10}$$

$$C^*_i = \frac{a_{c_i}}{\sum_k a_{c_k}} C_t, \tag{4.11}$$

$$R^*_{on_j} = \frac{\sum_m a_{r_m}}{a_{r_j}} R_{on_t}, \tag{4.12}$$

where C_t is the total flying capacitance in the converter and R_{on_t} is the total turn-on resistances of all switches in the converter. For discrete implementation, (4.3) and (4.9) will be used to quantify R_{eq} because the switch turn-on resistance is fixed once the transistor is selected and hence it can not be optimized. The flying capacitors are sized using (4.11). The a_v and a_r vectors are useful for selecting suitable capacitor and switch rating.

4.1.2 Power Loss Analysis

The efficiency in SC converters can be categorized into two parts: the voltage conversion efficiency (VCE) and power conversion efficiency (PCE or commonly η). They can be quantified by the following equations:

$$VCE = \frac{V_{out}}{V^T_{out}}, \tag{4.13}$$

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}}, \tag{4.14}$$

where V_{out}^{T} is the target output voltage, and equals nV_{in} seen across the secondary side of the ideal transformer in the average state model (Figure 4.1). Excluding the bottom-plate charge loss, the power losses (P_{loss}) in low power SC converters are due to two main factors [27] as following:

1. Linear losses (P_{lin}): these include the conduction loss and charge redistribution loss in the flying capacitors. Due to their negligible effect, effective series resistor (ESR) of the flying capacitors, trace impedance are usually ignored. Then, P_{lin} can be calculated as following:

$$P_{lin} = I_{out}^2 R_{eq}, \tag{4.15}$$

$$\implies P_{lin} = I_{out}^2 \sqrt{\left[\frac{\left(\sum_{i=1}^{k} a_{c_i}\right)^2}{C_t f_s}\right]^2 + \left[2\sum_{j=1}^{m} (a_{r_j}^2) R_{on_j}\right]^2}. \tag{4.16}$$

2. Switching losses (P_{sw}): these primarily include gate driving loss, diode reverse recovery loss, switch turn-on and turn-off losses. The diode reserved recovery will be neglected due to the low voltage across the switches. During turn-on, the SC converter is assumed to be driving a soft load and it drives a hard load in the turn-off interval, Figure 4.5. Therefore, P_{on} and P_{off} can be found using the following:

$$P_{on} = \frac{1}{2} I_{ds} V_{ds} f_s t_f, \tag{4.17}$$

$$P_{off} = \frac{1}{6} I_{ds} V_{ds} f_s t_r. \tag{4.18}$$

Then by using the charge and blocking voltage vectors, (4.17) and (4.18) can be modified to the following:

$$P_{on} = \frac{a_{r_i} a_{v_i}}{2} I_{out} V_{out} f_s t_f, \tag{4.19}$$

$$P_{off} = \frac{a_{r_i} a_{v_i}}{6} I_{out} V_{out} f_s t_r. \tag{4.20}$$

$$\implies P_{sw} = \sum_{j=1}^{m} Q_{g_j} V_{gs_j} f_s + \left(\frac{t_f}{2} + \frac{t_r}{6}\right) I_{out} V_{out} f_s \sum_{j=1}^{m} a_{r_j} a_{v_j}. \tag{4.21}$$

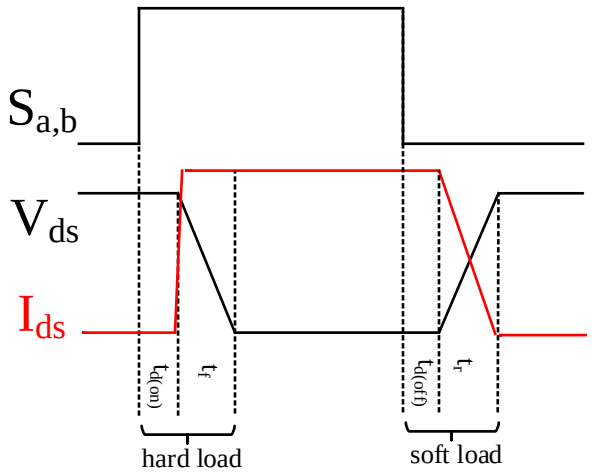


Figure 4.5: Gate switching intervals.

The switching power loss can be further optimized by employing soft-charging, or commonly referred to as zero-voltage-switching (ZVS) or zero-current-switching (ZCS), where

the switch is allowed to turn-on when V_{ds} reach zero or close to zero and the same for the turn off state with ZCS. The soft-switching can be achieved in resonant SC converters which has inductors in series with the flying capacitors. However, this technique limits the switching frequency to the resonant frequency, and it is undesirable to implement in converters targeting IC integration. The other way is to allow high output voltage ripple of the SC converter by reducing C_{out} (ideally $C_{out} = 0$) and then the output voltage ripple is controlled using a buck converter [28]. Nevertheless, in both techniques magnetic element is required which contradicts with the motivation for implementing purely capacitive converters. In addition, P_{sw} is very small compared to P_{lin} in low power SC converters. Therefore, the soft-switching is not considered in this work.

4.1.3 Output Regulation Methods

The SC converters suffer from poor output regulation which considered the second main challenge. Obviously from (4.1) and (4.13), there are two approaches to achieve relatively good output regulation: intrinsic and extrinsic control methods. Many of the control methods are discussed and compared in [26]. In general, intrinsic control involves changing R_{eq} through the parameters seen in (4.4), which consequently fine tunes the output voltage. These methods include duty ratio modulation (D), capacitor modulation (C_t), transistor width modulation (R_{on} and switching frequency modulation (f_s). Although R_{FSL} is highly dependent on the duty ratio, this technique resulted in very minimal effect in the total power profile. In addition, 50% duty ratio complementary driving signals requires a simple control circuit, compared to adaptive duty ratio signals, hence this technique is excluded. Component size modulation including C_t and R_{on} can be utilized, but in price of adding more components which increases the switching losses due to added switches that performs

Table 4.1: Variable FSC converter design specifications

Parameter	V_{in}	V_{out}	VCR	P_{out}
Value	0.3-0.6 V	1.5 V	5, 4, 3, 5/2	50 mW

modulation, and it also decreases the power density. However, these techniques can be employed in IC with careful size matching and efficient control. The frequency modulation is commonly used to regulate the output voltage in SC converters.

The extrinsic control method involves changing the VCR, i.e adaptive VCR, which offers a course tuning improving the VCE. Due to the ability of SC converters to provides multiple VCRs, the adaptive VCR method is quite effective to regulate the output voltage for applications that encounter wide input voltage range [29, 30]. For example, in FSC converter with two flying capacitors, seven possible VCR can be achieved. By enabling the adaptive VCR, this converter can be used to maintain relatively good VCE for wide input voltage range. We believe the adaptive VCR is an efficient regulation method compared to the intrinsic techniques for wide input range applications. However, there is a trade off by adding more switches to control transitions between different VCR. The addition of these transistors would increase P_{lin} and P_{sw}. Nevertheless, this technique is adopted in this work and careful optimization to these transition switches is considered.

4.2 Converter Design

In this section, we demonstrate the use of the theoretical analysis discussed in previous section by designing a variable FSC converter. The summary of the design specifications are listed in Table 4.1. This converter can be synthesized using the proposed algorithm discussed in chapter 3. For convenience, the circuit realization is redrawn in Figure 4.6.

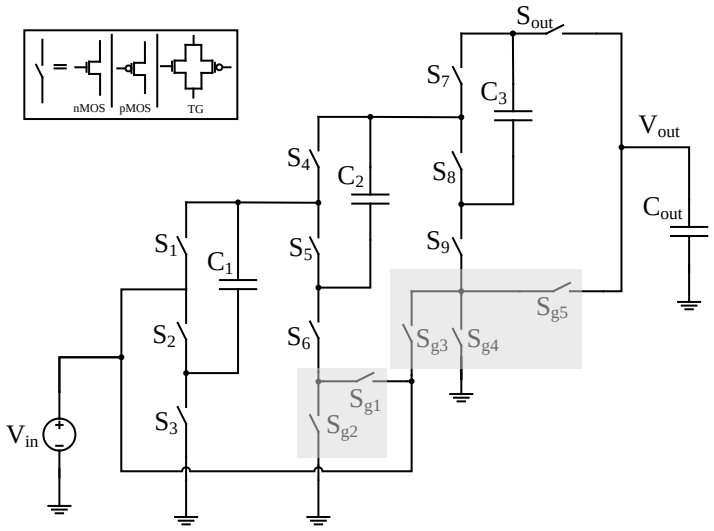


Figure 4.6: Variable FSC with VCR=5, 3, 4, 5/2.

4.2.1 Power Loss Calculation

Referring to the circuit states of the converter in Figure 4.7 and following the same procedure in section 4.1.2, a_c, a_r and a_v can be found as following:

$$\begin{bmatrix} a_{c_{VCR=5}} \\ a_{c_{VCR=4}} \\ a_{c_{VCR=3}} \\ a_{c_{VCR=5/2}} \end{bmatrix} = \begin{bmatrix} 2 & 1 & 1 \\ 2 & 1 & 1 \\ 2 & 1 & 1 \\ 1 & 1/2 & 1/2 \end{bmatrix}$$

$$\begin{bmatrix} a_{r_{VCR=5}} \\ a_{r_{VCR=4}} \\ a_{r_{VCR=3}} \\ a_{r_{VCR=5/2}} \end{bmatrix} = \begin{bmatrix} 3 & 2 & 2 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 0 & 1 & 0 & 1 & 0 \\ 3 & 2 & 2 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 0 & 0 & 1 & 0 \\ 2 & 2 & 2 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 0 & 1 & 0 & 0 \\ 3/2 & 1 & 1 & 1/2 & 1/2 & 1/2 & 1/2 & 1/2 & 1/2 & 1/2 & 0 & 1/2 & 0 & 0 & 1/2 \end{bmatrix}$$

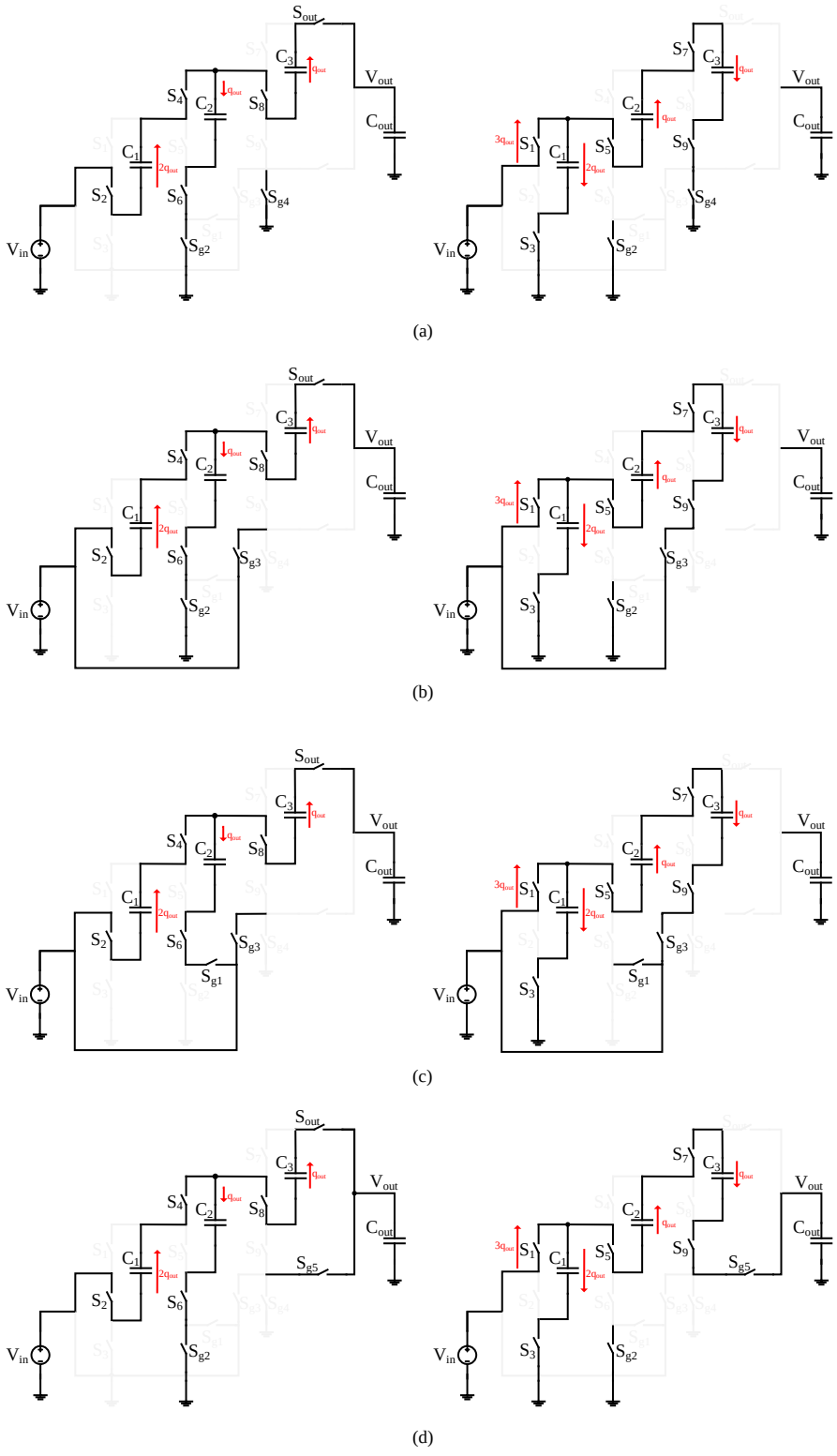


Figure 4.7: All operation states for proposed FSC: (a) VCR=5, (b) VCR=4, (c) VCR=3, and (d) VCR=5/2.

$$\begin{bmatrix} a_{v_c VCR=5} \\ a_{v_c VCR=4} \\ a_{v_c VCR=3} \\ a_{v_c VCR=5/2} \end{bmatrix} = \begin{bmatrix} 1/5 & 2/5 & 3/5 \\ 1/4 & 1/2 & 1/2 \\ 1/3 & 2/3 & 1/3 \\ 2/5 & 2/5 & 1/5 \end{bmatrix}$$

$$\begin{bmatrix} a_{v_r VCR=5} \\ a_{v_r VCR=4} \\ a_{v_r VCR=3} \\ a_{v_r VCR=5/2} \end{bmatrix} = \begin{bmatrix} \frac{1}{5} & \frac{1}{5} & \frac{1}{5} & \frac{2}{5} & \frac{2}{5} & \frac{1}{5} & \frac{3}{5} & \frac{3}{5} & \frac{2}{5} & \frac{2}{5} & \frac{1}{5} & 0 & \frac{1}{5} & 0 & 1 \\ \frac{1}{4} & \frac{1}{4} & \frac{1}{4} & \frac{1}{2} & \frac{1}{2} & 0 & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & 0 & \frac{1}{4} & \frac{1}{4} & 0 & 1 \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & \frac{2}{3} & \frac{1}{3} & 0 & \frac{1}{3} & \frac{1}{3} & \frac{2}{3} & \frac{2}{3} & 0 & \frac{1}{3} & 0 & \frac{1}{3} & \frac{2}{3} \\ \frac{2}{5} & \frac{2}{5} & \frac{2}{5} & \frac{4}{5} & \frac{4}{5} & \frac{2}{5} & \frac{1}{5} & \frac{1}{5} & \frac{1}{5} & \frac{1}{5} & \frac{2}{5} & 0 & \frac{3}{5} & 1 & 0 \end{bmatrix}$$

In this converter, we will consider the case of highest VCR which is associated with the worst case in terms of P_{loss}. Therefore, the following vectors is used:

$$\begin{bmatrix} a_c \\ a_{v_c} \end{bmatrix} = \begin{bmatrix} 2 & 1 & 1 \\ 1/5 & 2/5 & 3/5 \end{bmatrix} \tag{4.22}$$

$$\begin{bmatrix} a_r \\ a_{v_r} \end{bmatrix} = \begin{bmatrix} 3 & 2 & 2 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 0 & 1 & 0 & 1 & 0 \\ 1/5 & 1/5 & 1/5 & 2/5 & 2/5 & 1/5 & 3/5 & 3/5 & 2/5 & 2/5 & 1/5 & 0 & 1/5 & 0 & 1 \end{bmatrix} \tag{4.23}$$

Due to the zero elements of the gearbox transistor , $S_{g1} - S_{g5}$, their switching losses will result in zero loss when we multiply a_r by a_{v_r}, which increases the error in calculation. Thus, a way to account for their loss is need. From Figure 4.7, only two gearbox switches are observed to *on* at each VCR. Besides that, they are turned *on* in the transition between different VCR only. Therefore, we could account for their loss by considering the maximum

value for their charge and voltage representations. Referring to the matrices, one can notice that the maximum values for S_{g4} with a_r=1 at VCR=(4,5) and a_{v_r}=1 at VCR=5/2 states. As a result, gearbox control switch losses carry a weight of two, which is considered a worst case because usually the gearbox is not switching at the rate of system clocking signal. Then by using (4.16) and (4.21), the P_{loss} can be found as following:

$$P_{loss} = I_{out}^2 \sqrt{\frac{256}{C_t^2 f_s^2} + 2352 R_{on}^2} + 12 Q_g V_{gs} f_s + 3.2\Big(t_f + \frac{t_r}{3}\Big) I_{out} V_{out} f_s. \tag{4.24}$$

4.2.2 Components Selection

Using (4.11), the flying capacitance is sized as following, $C_1 = \frac{1}{2}C_t$ and $C_2 = C_3 = \frac{1}{4}C_t$. $C_t = 9.1\mu F$ have been selected based on rigorous simulation runs using genetic algorithm to find the global minimum of P_{loss} in each run. Different commercial switches have been examined and compared to select the optimal switch with highest efficiency to be use as a power switch in the variable FSC converter. Table 4.2 summarizes the important parameters of the chosen commercial switches. Various MATLAB simulations using real coded genetic algorithm GA developed in [31] have been conducted. Figure 4.8 shows the P_{loss} verses f_s for all switches. Then and once optimal switching frequency for each switch is selected, the efficiency profiles are plotted against the output power, Figure 4.9. Obviously, SW_1 has superior performance amongst all switches scoring 70% efficiency for $50mW$ output power at $90.1kHz$ switching frequency. Therefore, SW_1 (BSS816NW from Infineon) has been selected as a power switch for this variable FSC converter and the switching frequency is rounded to 100kHz for easier manipulation and implementation. A complete design flow chart of

Table 4.2: Different chimerical switches with their specifications.

No.	Switch	Manufacturer	Q_g (nC)	R_{ds} ($m\Omega$)	t_r (ns)	t_f (ns)
SW1	BSS816NW	Infineon	0.6	240	9	2.2
SW2	SSM3K324R	Toshiba	2.2	110	9	9.5
SW3	STR2N2VH5	ST	4.6	40	14.4	4
SW4	PSMN4R5	NXP	20.5	6.1	18.7	8.75
SW5	RYM002N05	ROHM	1.3	9000	8	43

variable FSC converter using discrete components is developed and can be found in Figure 4.10. It combines all the steps discussed in chapter 3 and 4 providing a design guide to implement FSC converter.

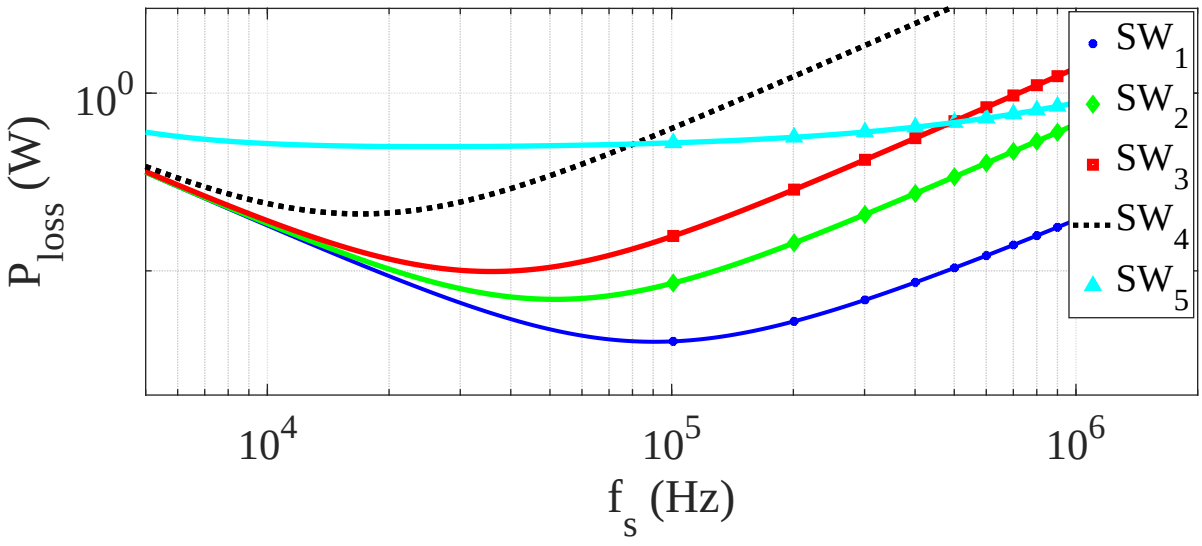


Figure 4.8: P_{loss} verses switching frequency for different switches.

4.2.3 Control Circuit

The LUT for gate signals control is shown in Table 4.3 (same as Table 3.5). The control circuit provides two types of signals: (1) main clock signals S_a and S_b to drive $S_1 - S_{10}$ and (2) gearbox closed loop control signals for driving $S_{g1} - S_{g5}$[1]. The clock signals can be

[1]Hereafter, S_r means the driving signal of r^{th} switch (M_r). S_a and S_b are the same as Φ_1 and Φ_2.

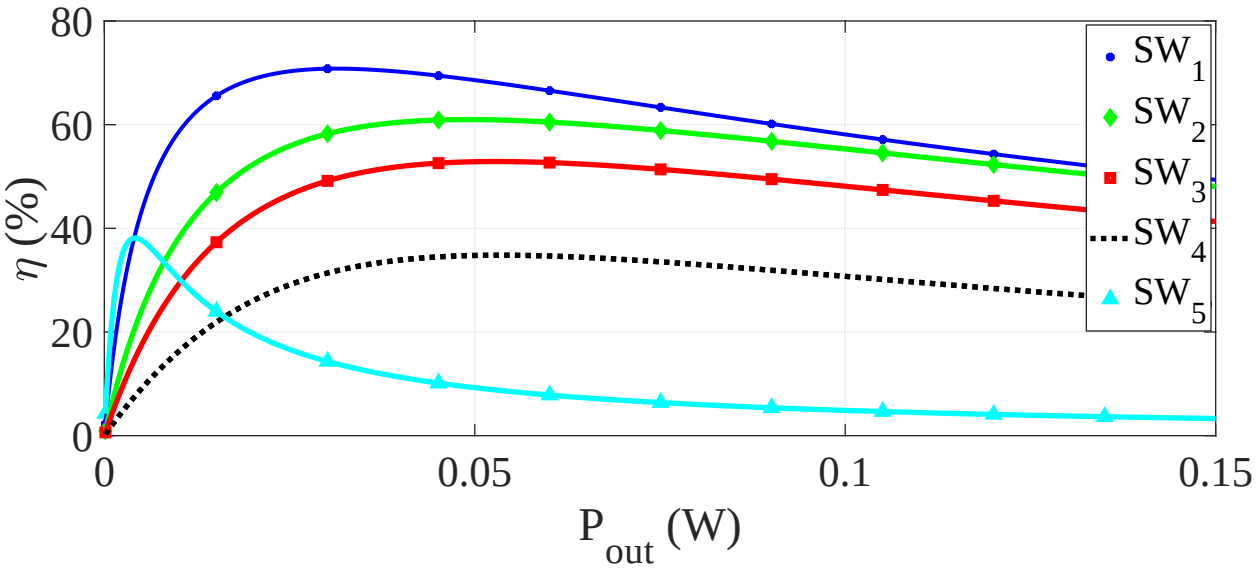


Figure 4.9: Efficiency for different loads.

generated using simple ring oscillator (RO) where odd number of logic inverters are connected together as shown in Figure 4.11. The frequency of oscillation can be calculated using the following equation:

$$f_{os} = \frac{1}{2n_{ro}\tau_d}, \tag{4.25}$$

where n_{ro} is the number of logic inverters, $n_{ro} = 3, 5, 7, ...(odd)$. τ_d is the logic inverter propagation delay and it is usually reported in the data sheet of commercial logic inverters[2]. For low f_{os} using RO, usually higher n_{ro} and/or τ_d is required. Therefore, $C_(ro)$ is placed in each stage to increase τ_d as shown in Figure 4.11. Then, non-overlapping clocks can be generated using the circuit in Figure 4.11, where C_d is added to control the dead-time period.

Using Karnaugh's map [32] and the LUT shown in Table 4.3, the expressions of these signals can be found as following: $S_{g1} = \bar{A}B = \overline{S_{g2}}$, $S_{g3} = \bar{A}(B + C)$, $S_{g4} = \bar{A}\bar{B}\bar{C}$ and $S_{g5} = A$, where A, B and C are the comparators output signals. The complete control circuit

[2]The inverter equivalent resistance seen at the output can be approximated by calculating the frequency generated from minimum RO of three stages for two or three different $C_(ro)$ values for comparison purposes.

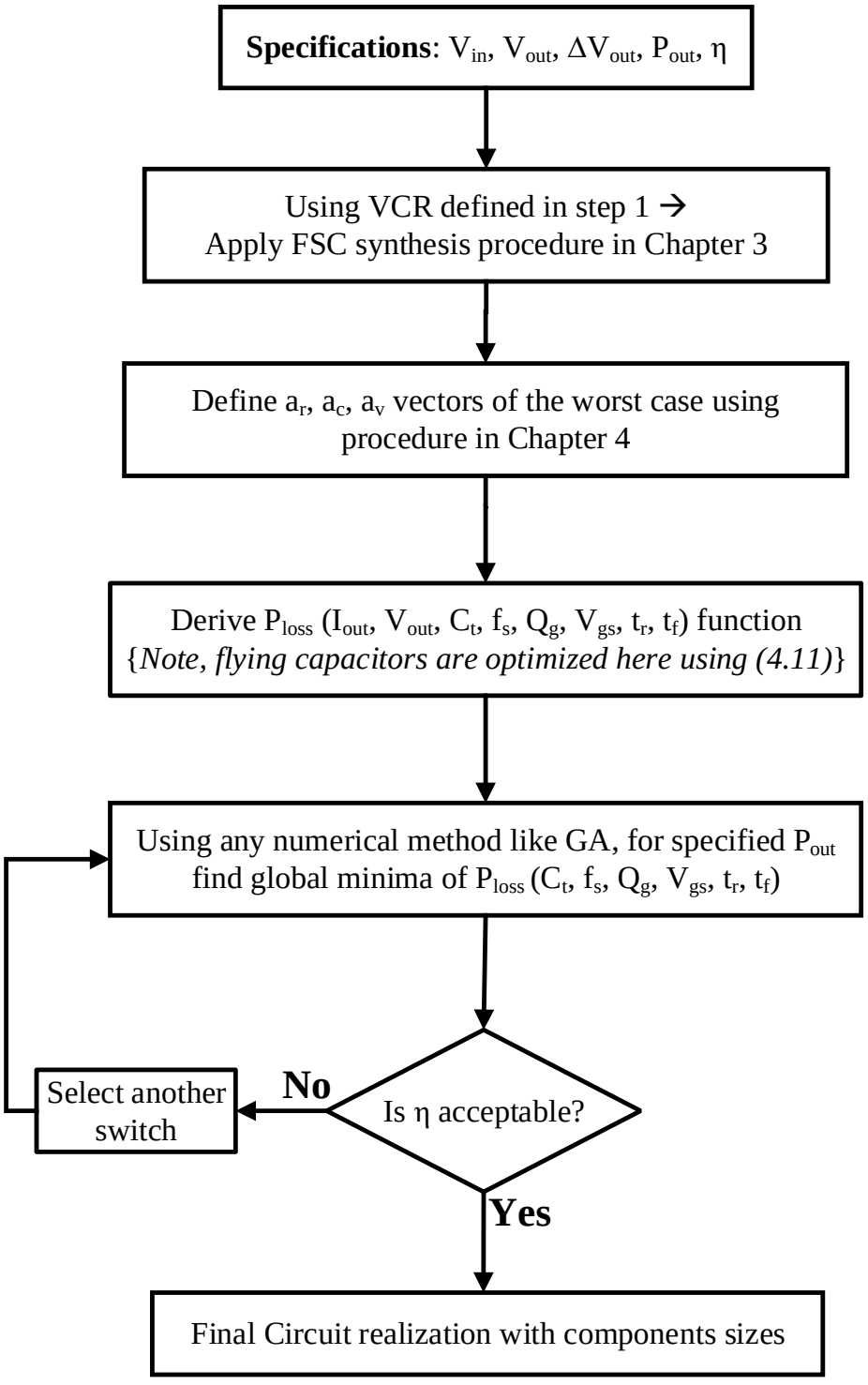


Figure 4.10: Variable FSC converter design flow chart using discrete components.

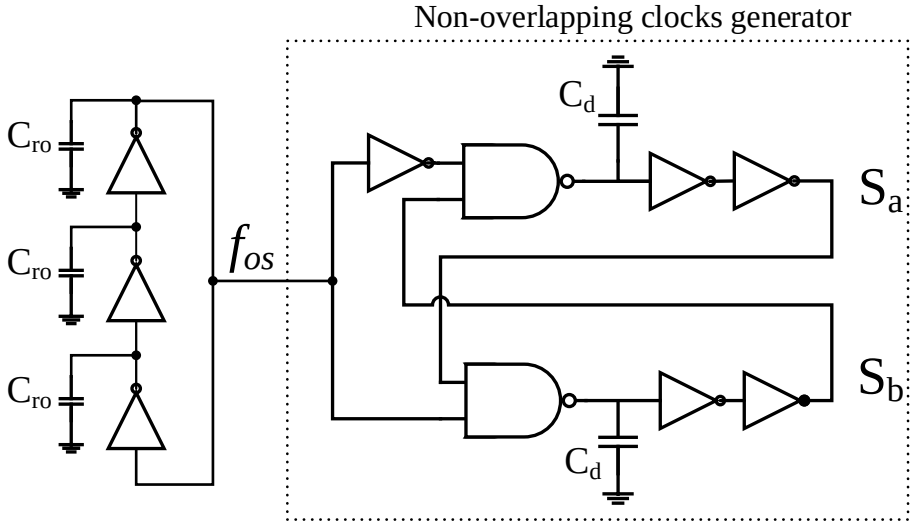


Figure 4.11: Ring oscillator with non-overlapping clocks generator.

Table 4.3: LUT for variable FSC converter.

VCR	5	4	3	5/2
$S_{1-10(odd)}$	S_a	S_a	S_a	S_a
$S_{1-10(even)}$	S_b	S_b	S_b	S_b
S_{g1}	off	off	on	off
S_{g2}	on	on	off	on
S_{g3}	off	on	on	off
S_{g4}	on	off	off	off
S_{g5}	off	off	off	on

that generates $S_{g1} - Sg5$ is depicted in Figure 4.12. We use dual ultra-power comparators (LTC6702 from Linear Inc.).

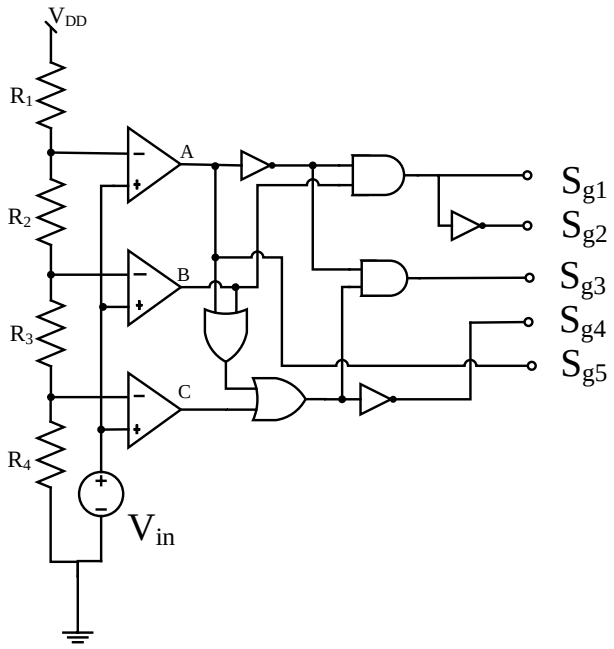


Figure 4.12: The gearbox signals control circuit.

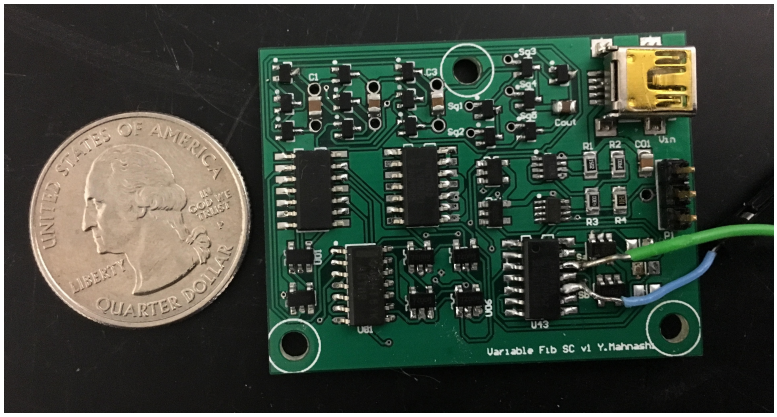


Figure 4.13: Variable FSC converter PCB.

4.3 Results

A prototype pf the designed variable FSC is implemented using two layers printed circuit board (PCB), see Figure 4.13. It occupies an area of $(36 * 48mm^2)$. We implement the ring oscillator using 74HC04 inverters and C_{ro}=15pF. Regarding the dead-time, and as shown in Table 4.2, SW_1 needs only a few ns to switch off. For the non-overlapping clock generator we used, we got around 125ns dead-time but when they are loaded by the switches, the clocks experience overlapping period which is something we want to avoid. To overcome this problem, the delay time in the non-overlapping circuit is increased by adding 1.5nF delay capacitance.

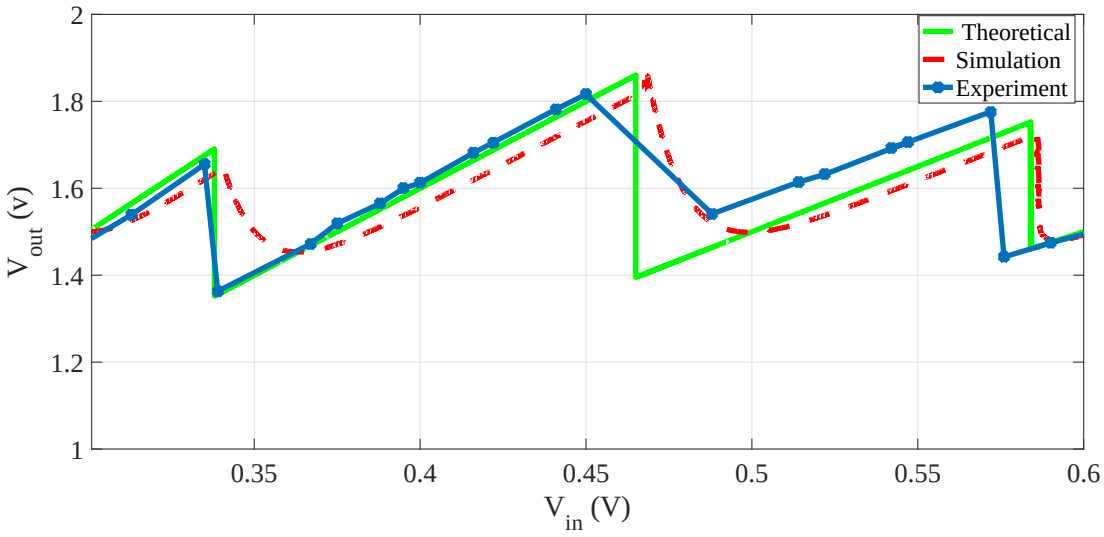


Figure 4.14: V_{out} response to V_{in} for variable FSC converter.

The output voltage response for different number of input voltages is drawn in Figure 4.14. It is clear that the output voltage response is as expected in the theory and synthesis process. The mean values of the output voltage are 1.51V and 1.46V for the simulation and experiment, respectively. Therefore, the output voltage mean value deviates a little from the nominal value (1.5), with an error of almost 2.67% for the experiment results. Overall, the

experiment and simulation results show an agreement with the theory.

4.4 Summary

In this chapter, we discussed the design and analysis of discrete variable FSC converter. We developed a design procedure flow that helps designing an efficient FSC converter. A variable FSC prototype is implemented using discrete components to show the functionality of the proposed converter. Experiment results show an agreement to the theory with an error of 2.46% in the output voltage mean value over an input voltage range of 0.3-0.6V.

Chapter 5

Integrated FSC Converter

In this chapter, an overview on integrated FSC converter (IC FSC) challenges and design is discussed. The proposed converter is designed and simulated using standard 0.5μm CMOS[1] technology provided by ON Semiconductor foundry, commonly called C5 [33]. Details about this technology and layout implementation of the devices are to be discussed in this chapter. The details of the startup circuit and controller design, layout and measurement results are presented in chapter 6.

5.1 On-chip Devices

In this section, the on-chip implementation of the switch, the solar cell and the capacitor is discussed. The later two devices comprised most of the die area. Optimizing their area is the road to high power density circuits. The switch area can be optimized to achieve minimum R_{on}, which helps improving efficiency performance. In this work, however, solar cells are not considered for same die integration. Nevertheless, remarks on IC solar cells are presented to pave the road for an ultimate smart solar cell[2].

[1] Complementary Metal Oxide Semiconductor

[2] Smart solar cell concept is introduced in chapter 1.

5.1.1 Switch Implementation

The switch can be implemented using PMOS, NMOS or transmission gate (TG) which is a parallel combination of PMOS and NMOS. The PMOS and NMOS transistor structures in CMOS are shown in Figure 5.1. They have four terminals: drain (D), source (S), gate (G) and body (B). For simplicity, we can assume that these transistors are working in triode region, also called ohmic or linear region in some references. The switch-on resistance is the channel resistance between D and S terminals of the transistor, and can be quantified as following:

$$R_{on_p} = \frac{1}{\mu_p C_{ox}(\frac{W}{L})_p(V_{sg} - |V_{t_p}|)}, \tag{5.1}$$

$$R_{on_n} = \frac{1}{\mu_n C_{ox}(\frac{W}{L})_n(V_{gs} - V_{t_n})}, \tag{5.2}$$

where μ_p and μ_n are the mobility of electrons, c_{ox} is the oxide capacitance per unit area, V_{t_p} and V_{t_n} are the threshold voltages of PMOS and NMOS, and they are all technology dependent parameters. W and L are the gate width and length of the transistor, respectively. In case of using TG, $R_{on_{TG}} = R_{on_p}//R_{on_n}$.

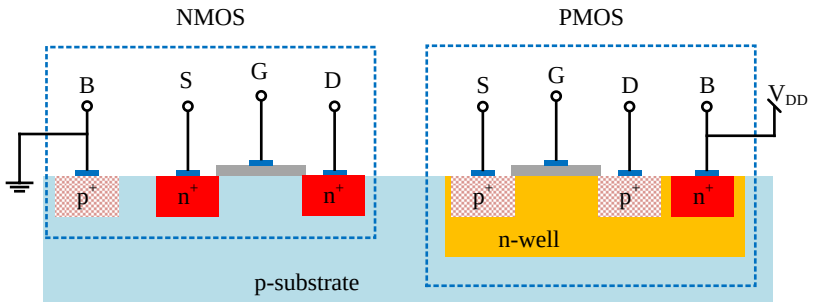


Figure 5.1: CMOS structure.

Usually, the body terminal of NMOS is connected to lowest potential to avoid latch-up that may occurs due to the connectivity of internal diode between B and S/D. For PMOS and for the same latch-up concern, the body terminal is commonly connected to the highest potential. In most cases where their is freedom in body connection, source terminals are usually connected to body terminals. However, there are some cases in n-well process[3] where the source terminal can not be connected to *gnd* or V_{DD} like most of the flying switches in SC converter structure. There are some non-idealities associated with MOSFET when it is used as a flying switch [34], summarized as follows:

1. Charge injection: when the MOSFET is turned on, some charge (Q_{ch}) accumulates in the transistor channel formed between the source and the drain, and the charge is traped with no path to discharge. During MOSFET switch-off state, Q_{ch} is injected to the load capacitor (C). Consequently, the voltage across the capacitor decreases to maintain a charge balance. The charge injection phenomena can be studied using the following equations:

$$Q_{ch} = WLC_{ox}(V_c - V_x), \tag{5.3}$$

$$V_c = \frac{WLC_{ox}(V_c - V_x)}{C}. \tag{5.4}$$

   The charge injection can be solved by placing a dummy switch in the charging path with an inverted gate signal to the main switch. This dummy switch prevents the charge injection by soaking the charge during turning off the main switch. Another

[3]CMOS can be fabricated using n-well, p-well or triple-well process. C5 used in this work is an n-well process.

solution is to use TG switch where two channels of PMOS and NMOS are available at the same time, and they work as a reservoir that maintains Q_{ch} from leaking to either terminals. A third option can be considered by keeping the ratio of C_{ch} to C very low meaning $WLC_{ox} << C$.

2. The turn on resistance of the flying switch depends on the input and/or output voltages if they are connected to the source terminal. In fact, when V_{gs} approaches V_t, the R_{on} increases drastically as described by (5.2) and (5.1). On the other hand, using TG, this effect can be minimized due to the parallel combination of R_n and R_p. Second approach to tackle this problem is to apply higher gate voltage to maintain enough potential difference between V_{gs} and V_t.

3. Body effect: the threshold voltage of a transistor (V_t) is proportional to the the change in V_{SB} as shown in the following equation:

$$V_t = V_{t0} + \gamma(\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F}), \tag{5.5}$$

where V_{t0} is the threshold voltage when $V_{SB} = 0$, γ is the body effect coefficient, Φ_F is the Fermi-potential and they are all process dependent parameters.

The body effect occurs when $V_{SB} \neq 0$ which is the case of all flying NMOS switches in n-well process. Obviously, body effect increases the transistor threshold voltage, which consequently increases the R_{on}, and in extreme cases the switch will not turn on. One solution to avoid this scenario is to increase the gate signal to maintain the R_{on}. Other techniques involving forward body biasing can be also emplyed, but it all depends on the structure and the technology used.

In our design, we use NMOS switch because $R_{on_n} < R_{on_p}$, and it has lower parasitics than TG. The charge injection effect is minimized by using higher flying capacitor. In addition, gate signal level-shifting is implemented to overcome any possible body effect in the flying switches.

5.1.2 IC Solar Cells

The on-chip solar cell is basically a photo-diode that generates electricity when it is exposed to a light source. The light photons excite the electrons in the PN junction which allows them to move to higher potential. This is translated to an electricity generation. In CMOS technology, there are two main on-chip PN junctions: D_1 and D_2 which can be found between the channel and substrate, see Figure 5.2. Prior works show how these photo-diodes can be utilized to generate electricity [35–42]. Obviously,D_1 provides more energy than D_2, because D_1 is exposed and close to the surface. However, if D_1 is used, the energy generated by D_2 will be lost. In [36], an on-chip solar cell is implemented in 0.5μm CMOS technology, by utilizing D_1 and grounding D_2. This solar cell achieves $20\mu W/mm^2$ in exposure to 60klux[4] light source. On the other hand, a $60\mu W/mm^2$ is achieved using D_2 under 25klux ultraviolet light source using $130nm$ CMOS technology [38]. In this context, It is worth mentioning that the surface area shape of the on-chip solar cell greatly effects the power density. For example, a fractal on-chip solar achieves 6% improvement compared to rectangular counterpart [42]. In this work, the solar cell is not considered for same die integration. However, a photo-diode power density $P_{ph_{\square}} = 20\mu W/mm^2$ is selected based on [36], that helps in choosing the power rating of the converter.

[4]Lux is the unit of light intensity, the daylight intensity without exposing to direct sun light is 10-25klux.

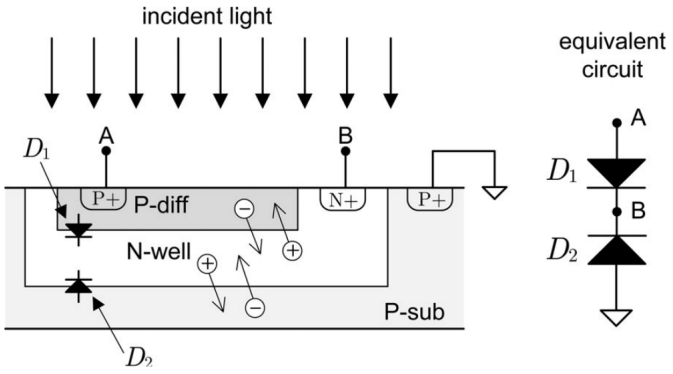


Figure 5.2: Photo-diodes available in CMOS process. Reproduced from [36].

5.1.3 IC Capacitors

The on-chip capacitor is usually associated with parasitic capacitance that is formed between top-plate, bottom-plate and ground due to the fabrication process, see Figure 5.3 where α is the ratio of the bottom-plate parasitic capacitor, C_{BP}, to the flying capacitor and β is the ratio of the top-plate parasitic capacitor, C_{TP}, to the flying capacitor. In fact, α is at least two times β, because of the minimum insulator diameter of C_{BP} compared to C_{TP}. For FSC configuration, C_{TP} maintains the charge because it does not have a path to fully discharge in whole switching period. Therefore, only C_{BP} is considered in this work. The effect of the parasitic capacitors on the converter efficiency is discussed in section 5.3.

There are many ways to implement capacitors on-chip. Excluding exotic capacitor configurations like trench capacitors, there are two main implementation for on-chip capacitors CMOS technology as following:

1. Conductor-insulator-conductor capacitor: this kind of capacitors are formed by sandwiching an insulator layer between two conductor layers like poly-silicon layer (PIP capacitor) or metal layers (MIM capacitors). This type of capacitor has lower capacitance density ($C_{\square}$) than MOS capacitors but features less parasitic capacitance.

MOM, metal-oxide-metal, is also considered another subset of conductor-insulator-conductor capacitors, but it requires no additional masks as it exploits the oxide layer as an insulator. However, MOM has poor capacitance density and substantial parasitic capacitor.

2. MOS capacitor is implemented by connecting the drain and source terminals of a transistor together forming one terminal for the capacitor, and the gate works as a second terminal for the capacitor. This configuration requires no additional masks, but the capacitance is highly nonlinear and changes based on V_{gs} value.

For C5 technology, an PIP capacitor is available with a $C_{\square}$[5] of $950aF/\mu m^2$. Therefore, PIP is used to implement all capacitors on-chip including C_{in}, C_{out} and flying capacitors.

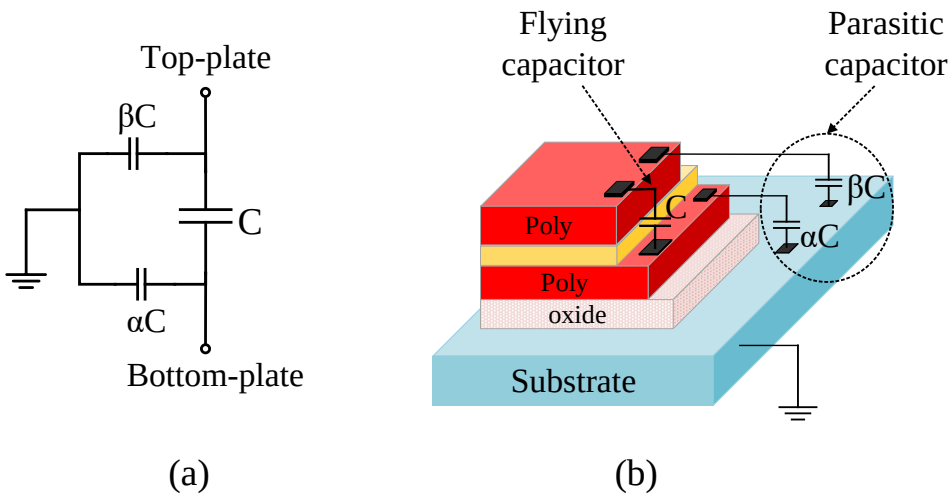


Figure 5.3: On-chip PIP capacitor: (a) simple model, (b) 3D layout structure.

[5]This is a design parameter provided by MOSIS, but after pos-layout extraction using Cadence Diva tool, only a $790aF/\mu m^2$ is achieved. This reduction results in 20% increase in the die area. Hence, the whole design is reevaluated based on the extracted value.

5.2 IC FSC challenges

In this section, two main challenges, i.e startup and parasitic loss, for monolithic FSC implementation are discussed. Solutions to overcome these challenges are proposed. The circuit implementation with simulation results are to be discussed in the following chapter.

5.2.1 Startup Mechanism

In energy harvesting (EH) circuits like our application example, the startup circuit is very critical. It provides the system with adequate power for proper operation. The minimum supply voltage for standard CMOS process is 36mV based on the well-known Meindl limit[6] [43]. However, MOS transistor based on EKV model[7] requires at least $V_{gs} = 4U_T$ to start operating in weak inversion where the transistor exhibits high channel resistance, before it still is not considered as completely turned off [44]. Note that, U_T is the thermal voltage which approximately equals to $26m$V at 300 K. Based on this discussion, we consider $104mV$ to be the minimum voltage to bias a transistor in normal conditions.

The ambient power sources are low voltage in nature, $10 - 600mV$, which complicates the startup process. Therefore, external startup circuit is commonly employed [45]. Table 5.1 summaries most ambient sources voltage range and power density [46, 47]. Considering the minimum voltage requirement mentioned earlier, starting up a circuit from lower voltage requires passive resonating circuits to build up the voltage. For example, in [45], a mechanical switch with inductor are used to build up the charge to higher level which can be transferred to startup the converter. On the other hand, when enough voltage is available like the case

[6] The Meindl limit defines the minimum operation voltage for a binary switching signal transfer.

[7] EKV defines three operating regions for MOSFET: weak, moderate and strong inversion. The MOSFET drain current in weak inversion has an exponential relation to the V_{gs}.

Table 5.1: Ambient sources.

	Voltage range	Power density	Source
Photovoltaic (PV)	0.3-0.6V	10-100μW/cm^2	Indoor light
		<15mW/cm^2	Outdoor light
Piezoelectric (PZ)	0.5V	50-300μW/cm^3	vibration
Thermoelectric (TEG)[a]	25mV	1.5μW/cm^3	ΔTemperature

[a]Reported values based on 1 K temperature difference between cold and heat plates.

of a solar cell, an active solution can be used to startup the circuit. It can can be realized using RO with auxiliary charge pumps (AQP) [21, 48–51].

Other possible startup mechanisms are reported in [52]. Most reported startup circuits employ magnetic elements except for the RO where no inductor is required. Owing to inductor-less solution, we think RO with AQP is more applicable to our application. RO circuit with non-overlapping clocks generator is shown in Figure 4.11, the frequency of oscillation can be found using (4.25), (5.2), (5.1) and substituting $\tau_d = C_L(R_p + R_n)$.

The AQP is usually implemented using Dickson CP or its modified variants; NCP1, NCP2 and cross-coupled charge pump (CCCP). The improved Dickson CPs are developed originally to solve the threshold voltage drop problem in conventional Dickson CP. However, the output stage still suffers from the body effect, which increases the threshold voltage as we discussed earlier. Therefore, body biasing techniques have been proposed to address this issue [50, 51, 53]. Nevertheless, the body biasing requires extra circuitry and complicate the startup circuit. To startup the system in this work, we consider using RO integrated with a simple 8-module CCCP as shown in Figure 6.3. The detailed implementation of the startup circuit is to discussed in chapter 6.

5.2.2 Parasitic Capacitor

The parasitic capacitance loss is unavoidable in IC design, as shown in Figure 5.7 for a simulated converter losses. The effect of the parasitic capacitors on the gain, startup and charge consumption of linear and Fibonacci-like SC converters is investigated in [54, 55], showing the gain dependency on parasitic capacitors and number of stages. Therefore, techniques to minimize the parasitic effect would improve the converter performance.

In general, the charge stored in the bottom-plate parasitic capacitor (Q_p) due to charging process either be lost, delivered to the load or recycled. Delivering Q_p to the load (intrinsic Q_p recycling) is quite interesting [56]. However, this technique is a structure-dependent and it is not practical in FSC converters. A novel technique to minimize the parasitic power loss P_{BP} was proposed in [57] by identifying the flying capacitor with highest bottom-plate loss. Then, the SN is configured in a way such that this capacitor is discharged once in each three cycles. This resulted in almost 50% reduction in the the power loss (14.68μW to 7.47μW in Table III [57]). Nevertheless, this technique can not be implemented in FSC structure because all flying capacitors in FSC are switched simultaneously in each switching cycle.

Another approach to perform charge recycling is to transfer Q_p in the dead-time periods. As mentioned earlier, SC converters are driven by two non-overlapping clocks. Therefore, besides the charging and pumping (active) states in SC converters, there are two *dead-time* zones to allow S_a to turns off completely before S_b turns on and vice versa, see Figure 5.4(a) in a two-capacitor FSC example. Obviously, all C_{BP} is charged to Q_p during the charging state and discharged to *zero* in the pumping state. Hereinafter, by QR is referred to the Q_p dead-time recycling. In [58], QR is proposed using an additional capacitor, C_{REC}, that works as a charge reservoir. In the first dead-time period, $\frac{1}{2}Q_p$ is stored in C_{REC}, and then

the same charge is pumped back to the C_{BP} in the second dead-time interval. Therefore, effectively $\frac{1}{2}Q_p$ is conserved in each switching cycle. However, adding C_{REC} increases the area on-chip, which is always something we need to avoid in IC design.

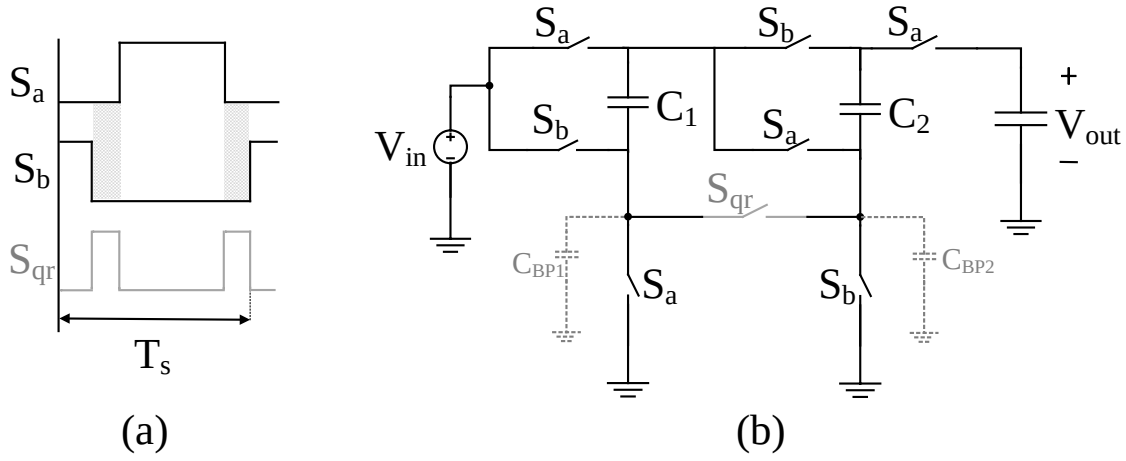


Figure 5.4: Dead-time charge recycling (QR): (a) Timing signals, (b) FSC converter.

In [59–61], the same concept of QR is employed, but now using internal C_{BP} owing to the interleaved SC structure. However, this comes in price of adding additional components.

Inspired by this literature, dead-time charge recycling can be used in the proposed FSC converter by exploiting the availability of C_{BP} in each other state without transforming the converter into interleaved structures nor adding additional capacitor. Therefore, a charge recycling unit (QRU) is proposed to transfer and maintain the charge between parasitic capacitors, C_{BP_1}, C_{BP_2} and C_{BP_3}, during the dead-time periods. Note that, the dead-time periods should be long enough for Q_p to be completely transferred from one capacitor to another. On the other hand, increasing the dead-time period increases the voltage ripples and may also affects the conversion performance. Therefore, optimizing the timing is essential to perform a safe charge recycling. The implementation of QR circuit is to be discussed in chapter 6.

5.3 IC FSC Converter Analysis

The area on-chip (A_t) and P_{loss} are considered the main constrains in IC SC converter design. The component sizes and optimal switching frequency can be determined by A_t and P_{loss} constrained optimization [27, 62, 63]. In the following, these two factors are studied and analyzed.

5.3.1 Die Area Analysis

The total area on-chip can be found using the following:

$$A_T = A_{ph} + A_c + A_{sw} + A_{cnt}, \tag{5.6}$$

where A_{ph} is the area of the photo-diodes, A_c is the area of all capacitors, A_{sw} is the area of all power switches and A_{cnt} is the area of the control unit. For sizing and optimization, only A_c and A_{sw} are considered because they have great effect on the P_{loss} function as will be discussed next section. The control unit constitutes negligible area on chip compared others and hence can be neglected. The photo-diodes occupy the largest portion of the die area. Nevertheless, optimizing photo-diode is out of the scope of this work. Therefore, A_{ph} can be estimated using the following equation:

$$A_{ph} = \frac{Pph}{P_{ph_\square}}. \tag{5.7}$$

where P_{ph} is the required input power to our circuit. Also, the A_c can be estimated by dividing the total required capacitance C_t by the capacitance density $C_\square$. Finally, A_{sw} is the gate width multiplied by the gate length. Then, the total area on-chip in m^2 excluding

the photo-diodes can be found as following:

$$A_t = \frac{C_t}{C_\square} + L_{min} W_t. \tag{5.8}$$

One note worth mentioning here, A_t is mainly determined by total capacitance on-chip, and having same total capacitance on chip for two SC different topologies does not imply equal number of stages (check Figure 2 in [63]). However, FSC has the least number of stages for any VCR compared to other topologies and the capacitance can be optimized. Consequently less number of switches are required which simplifies the control circuit.

5.3.2 Power Loss Analysis

Let us now analyze the power loss in IC FSC converter. As discussed in section 4.1.2, P_{loss} of FSC converter can be quantified using (4.16) and (4.21). However, gate driving loss is usually considered the main source of P_{sw} in IC design, all other losses can be neglected because of their minimal effect. Therefore, P_{sw} of IC FSC can be calculated as following:

$$P_{sw} = f_s \sum_{j=1}^{m} (WL)_j C_{ox} V_{gs_j}^2. \tag{5.9}$$

where WLC_{ox} is the gate capacitance of j^{th} transistor. In addition, the bottom-plate power loss (P_{BP}), due to charging and discharging C_{BP}, is very critical and needs to be analyzed and optimized. P_{BP} can be quantified using the following equation:

$$P_{BP} = f_s \sum_{i=1}^{k} \alpha C_{f_i} V_{BP_i}^2. \tag{5.10}$$

In discrete implementation of FSC, once a switch is selected, the transistor width can not

be optimized. On the other hand, the switch is designed from scratch in IC implementation. In fact, optimizing both the capacitor and switch sizes minimize the P_{lin} losses. Therefore, both (4.9) and (4.10) are used here. To simplify the analysis, a device resistivity (ρ_x) with minimum length L_{min} is defined and can be quantified as following:

$$\rho_x = \frac{L_{min}}{\mu_n C_{ox}(V_{gs} - V_{t_n})}, \tag{5.11}$$

where L_{min} equals $0.6\mu m$ in C5 technology. Based on the foregoing discussion, the total P_{loss} of IC FSC can be found using the following:

$$P_{loss} = f_s \sum_{i=1}^{k} \alpha C_{f_i} V_{BP_i}^2 + f_s \sum_{j=1}^{m} (WL)_j C_{ox} V_{gs_j}^2 + I_{out}^2 \sqrt{\frac{\Big(\sum_{i=1}^{k} a_{c_i}\Big)^4}{C_t^2 f_s^2} + \frac{4\rho_x^2 \Big(\sum_{j=1}^{m} a_{r_j}\Big)^4}{W_t^2}}, \tag{5.12}$$

In conclusion, the constrained optimization can be used where the P_{loss} in (5.12) is the objective function and A_t in (5.8) is the constrain. The design flow chart for designing an IC FSC converter is depicted in Figure 5.5.

5.4 IC FSC Converter Design

Using the same converter in chapter 4, this section explores the design and optimization of the converter specifications. The converter is redrawn in Figure 5.6 including parasitic capacitors. Table 5.2 shows the C5 parameters used to quantify A_t and P_{loss} functions. Note that, PIP capacitance density is found to be $790a\text{F}/\mu\text{m}^2$. In this work, we are limited to

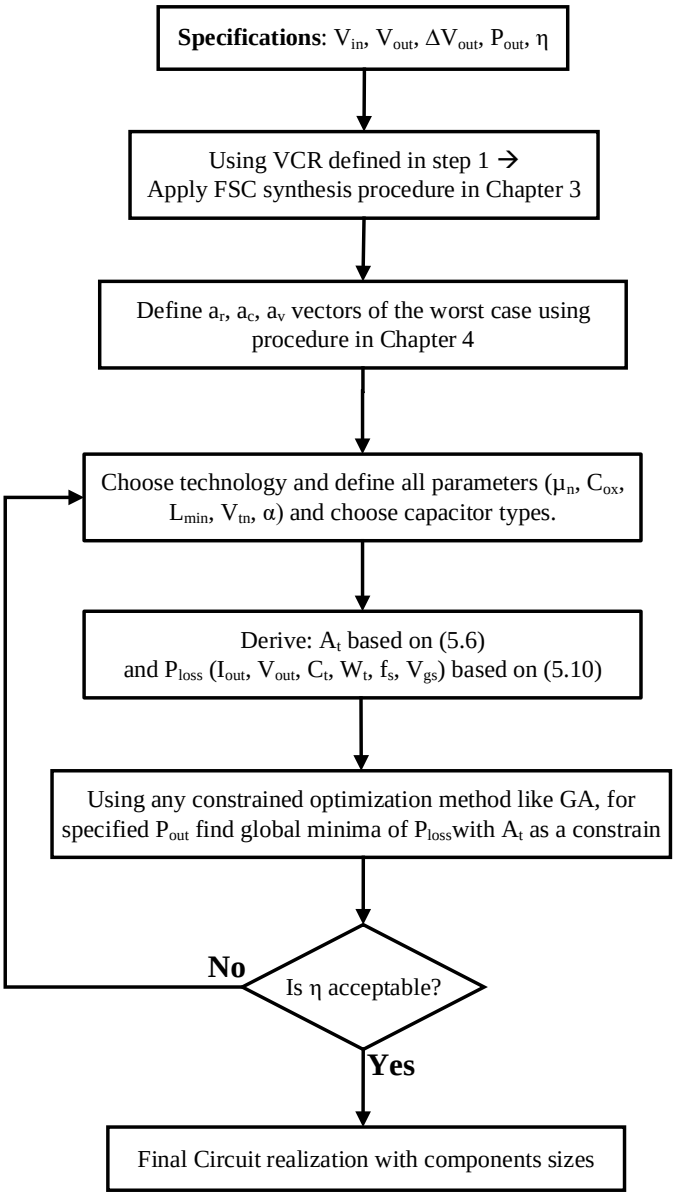


Figure 5.5: IC FSC design procedure flow chart.

Table 5.2: C5 technology parameters

Parameters	μ $(cm^2/V.s)$	t_{ox} (nm)	C_{ox} (nF/cm^2)	V_t (V)	L_{min} (μm)
NMOS	445	13.5	260.4	0.7	0.6
PMOS	201	13.5	260.4	-0.9	0.6

$4mm^2$ die area[8]. However, considering the IO pads[9], which usually constitutes close to 30% of the area, only $2.8mm^2$ is assumed to be the available active area. In addition, the input and output capacitors are integrated on-chip and sized as the minimum flying capacitor. Therefore, we can define the total area (A_t) constrain as following:

$$A_t = 0.002C_t + 0.6W_t \leq 2.8mm^2, \tag{5.13}$$

where the units of C_t and W_t are in pF and μm, respectively. Second step is to find optimized parameters using charge vectors found in section 4.2.1. They are rewritten here for convenience:

$$\begin{bmatrix} a_c \end{bmatrix} = \begin{bmatrix} 2 & 1 & 1 \end{bmatrix}$$

$$\begin{bmatrix} a_r \end{bmatrix} = \begin{bmatrix} 3 & 2 & 2 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 0 & 1 & 0 & 1 & 0 \end{bmatrix}$$

Therefore, $C_1 = C_t/2$, $C_2 = C_3 = C_t/4$ using (4.11). To account for zero-elements in a_r, we assume the worst case for switches S_{g1}, S_{g3}, S_{g5} as 1, 1, and 1/2, respectively. They are found using the whole a_r matrix in section 4.2.1. Then, the switch-on resistances can be found using (4.12) as following, $W_1 = 6W_t/37$, $W_2 = W_3 = 4W_t/37$, $W_{4-10} = W_{g1-g4} = 2W_t/37$

[8]This project is considered to be fabricated under MOSIS Educational Program (MEP), where the die area is limited to $4mm^2$.

[9]IO pads connect the IC to the outside world, and it is extremely important for proper operation. Some details for the used IO pads are available in chapter 6.

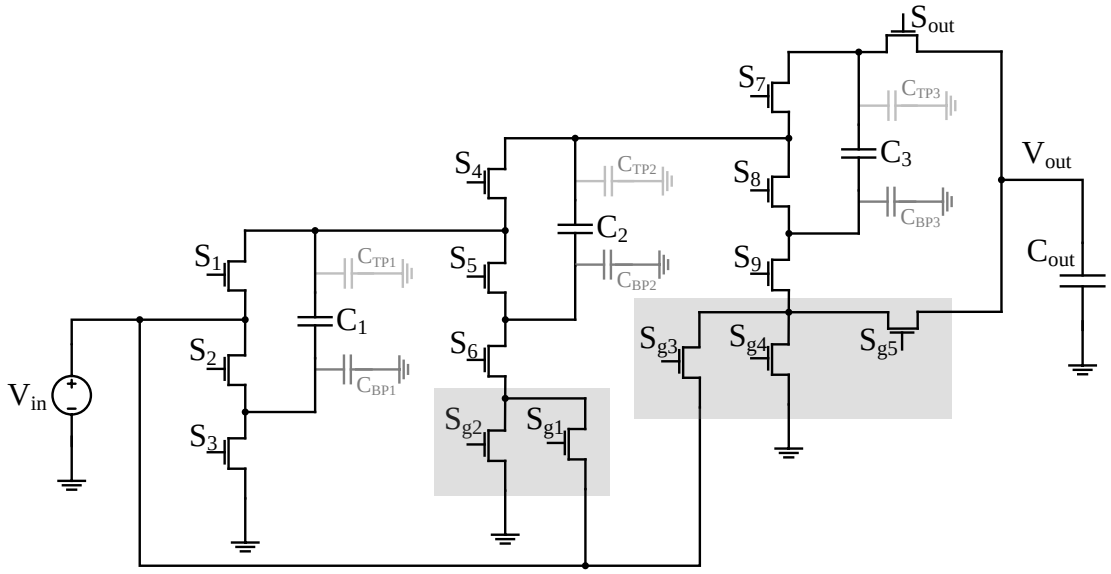


Figure 5.6: Proposed FSC with parasitic capacitors.

and $W_{g5} = W_t/37$, where W_t is the total width for all switches. Now, let us find the device resistivity, ρ_x using (5.11). First, consider the worst case where $V_s = 3V_{in}$ which is the case of S_{out}, $V_{gs} - V_{tn} = V_g - 3V_{in} - V_{tn}$. Using $V_g \geq 2$, $V_{in} = 0.3$ and $V_{tn} = 0.7$, ρ_x is found to be $0.0129\Omega \cdot m$. Combining these results, the optimal R_{eq} can be found using (4.9) and (4.9), as following:

$$R_{eq} = \sqrt{\frac{256}{C_t^2 f_s^2} + \frac{79}{W_t^2}}, \tag{5.14}$$

Let us now find the power loss of the bottom-plate parasitic capacitor. By analyzing the voltage across C_{BP} in each phase, it was found that $V_{BP_1} = V_{BP_2} = \frac{1}{2}V_{BP_3} = V_{in}$. By relating $V_{in} = \frac{1}{5}V_{out}$, $P_{BP}(C_t, f_s, V_{out})$ can be found as following:

$$P_{BP} = 0.09\alpha C_t f_s V_{out}^2, \tag{5.15}$$

Then, by using $V_{gs} = 2$ and subsisting (5.9), (5.14) and (5.15) in (5.12), the total P_{loss}

of the designed FSC converter can be found as following:

$$P_{loss} = 0.09\alpha C_t f_s V_{out}^2 + 6.25 \times 10^{-9} W_t f_s + I_{out}^2 \sqrt{\frac{256}{C_t^2 f_s^2} + \frac{79}{W_t^2}}. \tag{5.16}$$

Referring to the design flow chart in Figure (5.5), we are ready for optimization step. We formulate our optimization problem using objective function as P_{loss} in (5.16), the constrain as A_t found in (5.13), and using three variables C_t, f_s and W_t. Multiple runs have been conducted using GA for 10μW output power and the parameters are selected as following: 960pF total capacitance, $200k$Hz switching frequency and total transistor width of 388.5μ m. The total power loss is found to be almost 6.85μW with 59% efficiency. Figure 5.7 shows the contribution of losses. It can be seen that P_{BP} loss constitutes large amount of the total power loss. Applying the dead-time charge recycling (QR) decreases the P_{loss} by almost 27% as shown in Figure 5.7, which is translated to an increase of 15% in the total efficiency. More details about the advantages gained from applying QR is discussed in chapter 6.

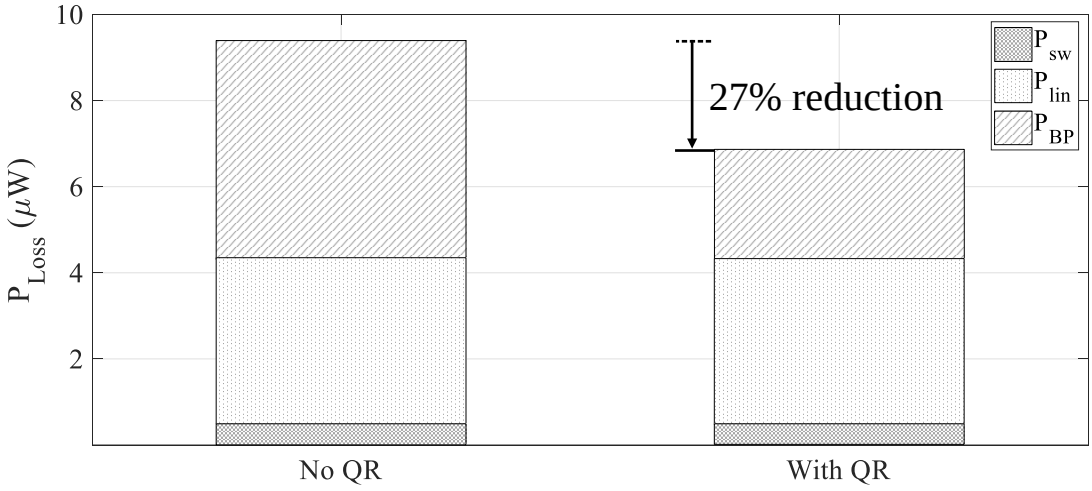


Figure 5.7: Power losses shares with and without charge recycling (QR).

5.5 Summary

In this chapter, challenges of implementing IC FSC converter are discussed. Devices implementation is covered. The design procedure for IC FSC converter is illustrated through the solar energy harvesting case. It is shown that parasitic effects have a substantial effect on the converter performance. Charge recycling (QR) technique is implemented to minimize the P_{BP} loss and improve the converter overall efficiency. Ideally, this technique reduces the P_{BP} by almost 50% which is translated to a 27% reduction in P_{loss}, and 15% improvement in the converter efficiency. In next chapter, the whole system design, optimization, layout and post-layout simulation are to be covered.

Chapter 6

Analog and Digital Circuit Design

Following previous chapter, this chapter continues to discuss the details of designing IC FSC and concludes with the post-layout simulation results. The complete IC circuit is shown in Figure 6.1. The startup circuit includes ring oscillator, auxiliary cross-coupled charge pump (CCCP), current starved ring oscillator (CSRO) and non-overlapping clock generator (N-OV). This circuits is designed to generate clocking signals and DC voltage of >1V to operate the controller.

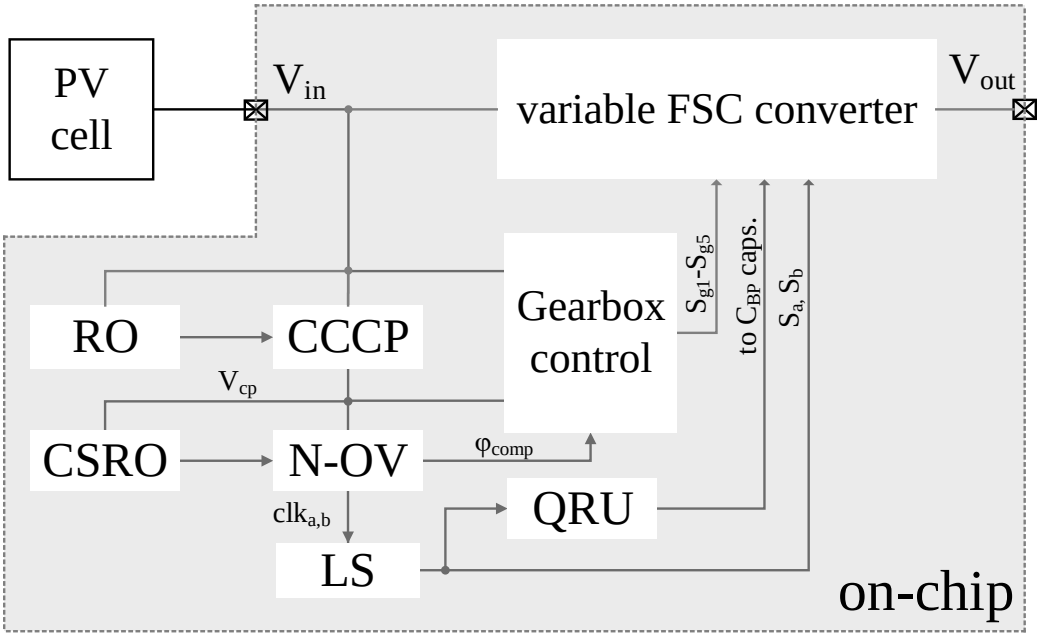


Figure 6.1: FSC IC building blocks.

The gearbox controller can be implemented in two possible structures as shown in Figure 6.2, either using a feed-forward scheme which is the same circuit used in chapter 4, or in a feedback topology if there is a way to sustain a reference voltage. For the latter, a hysteresis controller can be employed. It senses the output voltage and sends count up/down signal to a counter which drives the gearbox switches to sustain the load voltage between V_H and V_L. The feedback controller provides better stability and controllability over VCR. However, the feed-forward controller is used here due to the lacking of the high reference voltage. In the following sections, proposed startup, clock generation and comparator circuits are discussed. Then, the simulation results are presented with discussion.

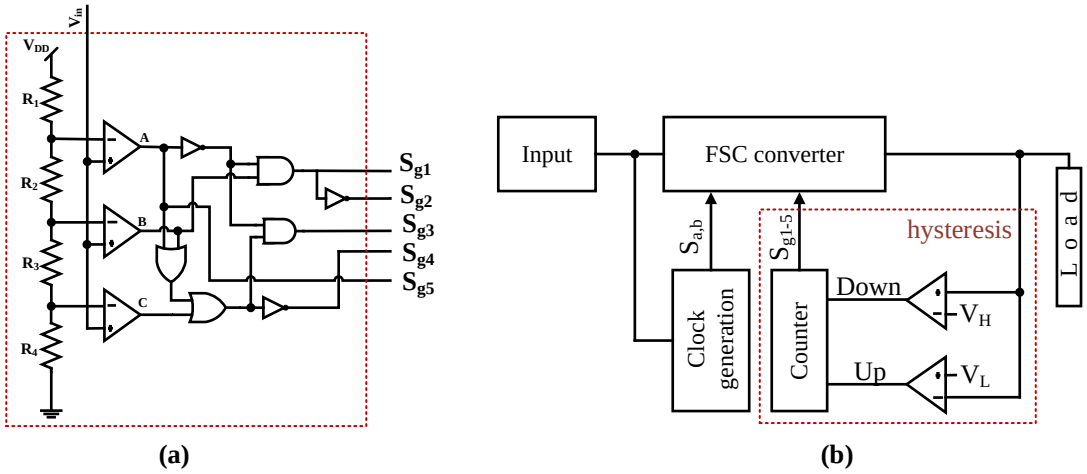


Figure 6.2: Possible FSC controller structures: (a) Feed-forward, (b) Hysteresis controller.

6.1 Cross-Coupled Charge Pump Design

Due to its structure, CCCP can boost sub-threshold input voltage to higher levels, but it suffers from poor efficiency. Therefore, CCCP is employed as an axillary charge pump for the system. This circuit requires also two complementary clocking signals. A simple three-

stage ring oscillator (RO) is used to generate these signals. The complete circuit is shown in Figure 6.3. Eight-module CCCP is used to boost the voltage to relatively usable level.

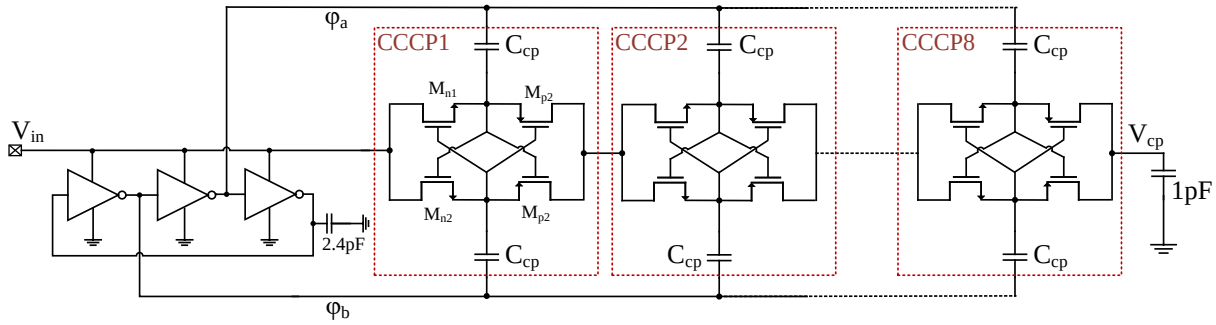


Figure 6.3: Three-stage RO with eight CCCP modules.

In C5 technology, p-substrate is used which means NMOS transistors suffer from body effect when their source and bulk (body) are not shorted. Whereas, the body effect can be avoided in PMOS transistors by applying PMOS in separate n-wells. Due to the body effect in NMOS transistors, W/L needs to be optimized achieving minimum channel resistance. Assuming NMOS transistor is in weak inversion (WI) region, the following derivation can be applied:

$$I_{ds(WI)} = \frac{W}{L} I_{d_0} \left(e^{\frac{V_{gs}-V_{th}}{nU_T}} \right) \left(1 - e^{\frac{-V_{ds}}{U_T}} \right), \tag{6.1}$$

$$R_{ds(WI)} = \left[\frac{\partial I_{ds(WI)}}{\partial V_{ds}} \right]^{-1}, \tag{6.2}$$

$$R_{ds(WI)} = \frac{1}{\mathbf{W}} \left(\frac{L_{min} U_T}{I_{d_0}} \right) e^{\left(\frac{nV_{ds}-V_{gs}+V_{th}}{nU_T} \right)}, \tag{6.3}$$

where I_{d_0} is the drain current that flows when V_{gs}=V_{t_n}, and n is the inversion slope factor which is sensitive to body effect.

The MOS channel length is chosen to be the minimum, L_{min}. So, one can combine the explicit first order process parameters, $\left(\frac{L_{min}U_T}{I_{d_0}}\right)$. Due to the complexity of this derivation, only the MOS channel width, **W**, is considered for optimization alongside with the flying capacitor, C_{cp}. Therefore, extensive runs of spice simulation in Virtuoso ADE reveal that W=6μm and C_{cp}=240fF has the best performance, and hence they are selected. The capacitance seen at ϕ_a and ϕ_b nodes is around 2.4pF and hence a capacitance of the same value is added to the RO third terminal to ensure smooth oscillation. Also, 1pF capacitance is added at the CCCP output to minimize the output ripple. The final layout is shown in Figure 6.4.

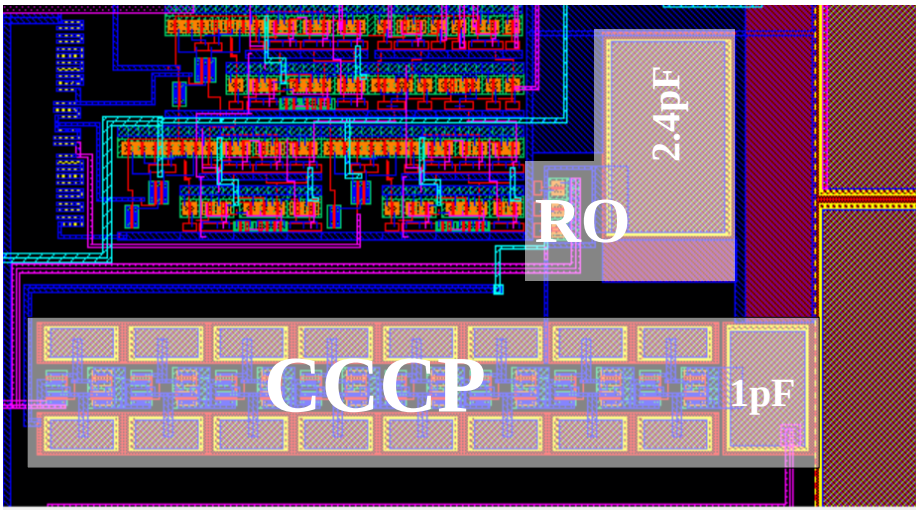


Figure 6.4: Layout of RO with CCCP.

The post-layout simulation is shown in Figure 6.5. The unloaded output voltage, V_{cp}, is around 2.3V in response to 0.5V input. But, when the CCCP is loaded, the output voltage drops down. In ADE, a noise that is required for oscillation can be injected in some nodes by setting initial conditions to zero.

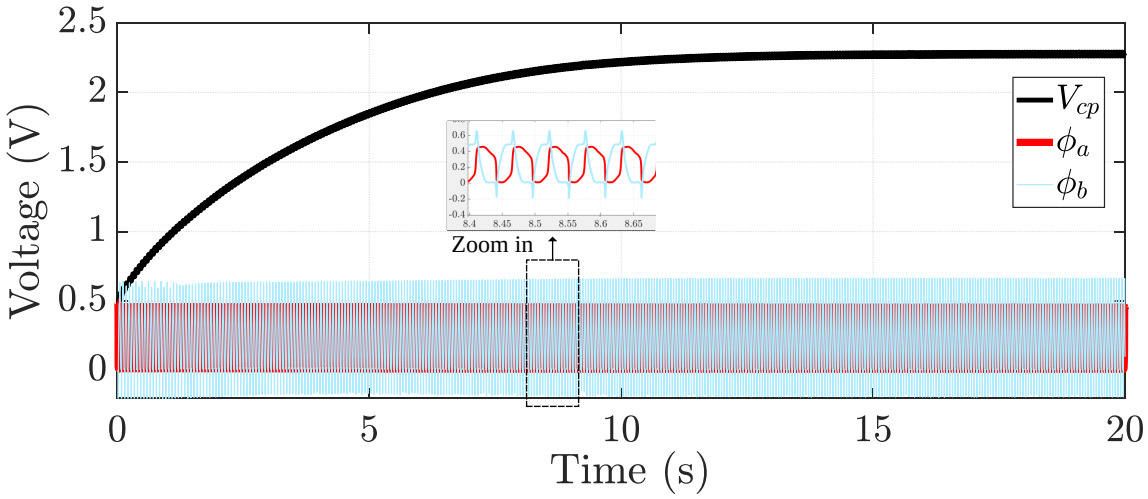


Figure 6.5: Post-Layout simulation for the startup circuit using 0.5V input voltage.

6.2 Clock Generation

To drive the FSC converter, two non-overlapped clocks need to be generated on-chip. Here, a current-starved ring oscillator (CSRO) is used to generate $200k$Hz clock signal, which is then fed to a non-overlapping clocks generator to induce a dead-time period between clk_a and clk_b. The later two signals are fed to a level-shifter to get S_a and S_b. The circuit realization is shown in Figure 6.6.

The CSRO is a voltage controlled oscillator. It works like a regular RO discussed previously in chapter 5, but with additional feature of being controllable through current mirrors, M_1-M_4, by controlling the amount of current I_D flowing to the inverters. Due to process and temperature variations in IC fabrication, CSRO is employed here to control and calibrate the frequency of oscillation to be around the designed value of $200k$Hz. The frequency of oscillation equation is derived in [64], and can be quantified as following:

$$f_{osc} = \frac{I_D}{n_{ro} C_{tot} V_{DD}}, \tag{6.4}$$

where C_{tot} is the total capacitance seen at the output of each inverter which equals to C_{in}+C_{out}+C_{ro}, and n_{ro} is the number of inverters.

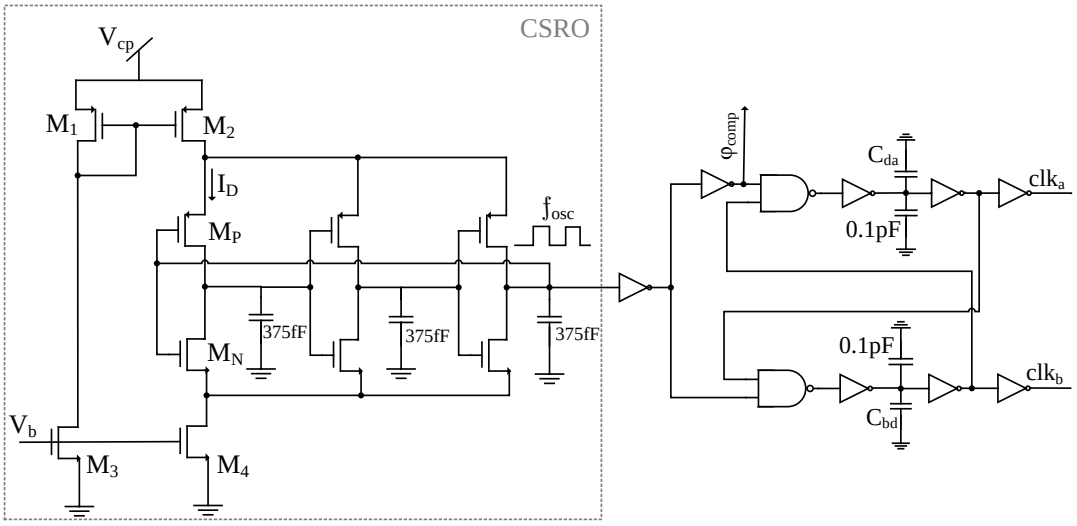


Figure 6.6: Three-stage CSRO with non-overlapping clock generator.

After optimization process of considering both area and power consumption, three-stages CSRO have been selected with current mirrors sized at W=5μm and L=1μm and load capacitor of 375fF for each inverter. The frequency of oscillation is calibrated off-chip using V_b pin. Also, note that the dynamic comparator requires undistorted clock signal, so the output of CSRO is buffered by an inverter. For the non-overlapping circuit, 100fF and off-chip delay capacitors, C_{da} and C_{db} are added to control the dead-time off-chip.

Level-shifter is also employed for another voltage boosting stage to overcome the need of higher gate voltage in the high nodes like the source of S_{out} in the main FSC converter. The level-shifter circuit is shown in Figure 6.7, M_{LS2} turns on when clk_a goes high pulling node x to zero. Then, the PMOS transistor, M_{LS3}, turns on and hence S_a node clamps to V_{DD2}. For next cycle when clk_aN is high, M_{LS1} conducts and it pulls S_a node down to zero. The same procedure are repeated for S_b level shifter. The level-shifter transistor

sizes are optimized for the delay between clk signals and driving signals, S_a and S_b, and the power consumption. The sizes M_n=10.5μm/0.6μm and M_p=1.5μm/0.6μm are selected.

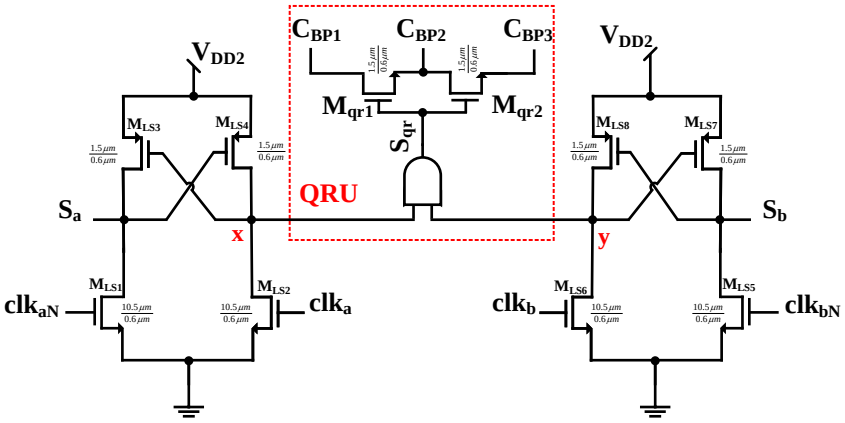


Figure 6.7: Level shifters with QRU.

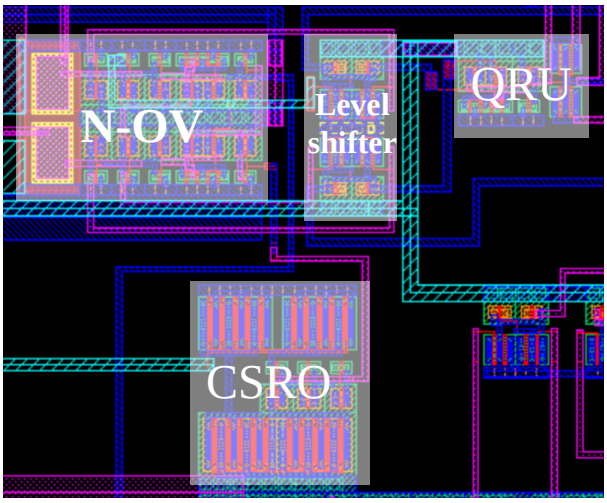


Figure 6.8: Clocks generation layout.

Moreover, a charge recycling unit (QRU) is used to transfer the charge between parasitic capacitors. QRU consists of a simple AND gate with minimum sized transistors M_{qr1} and M_{qr2} with a size of 1.5μm/0.6μm. The AND gate output, S_{qr} goes high in the dead-time where S_a and S_b are low. S_{qr} is driving the charge-transfer transistors, M_{qr1} and M_{qr2}.

Therefore, during the dead-time, the charge accumulated in the parasitic capacitor of C_2 is transfered to the parasitic capacitors of C_1 and C_3 fulfilling the charge recycling concept. The post-layout simulation for this chain of clock generation is conducted using Virtuoso ADE in Spectre simulator and is shown in Figure 6.9. The frequency of oscillation is around 200kHz and S_{qr} is generated as expected.

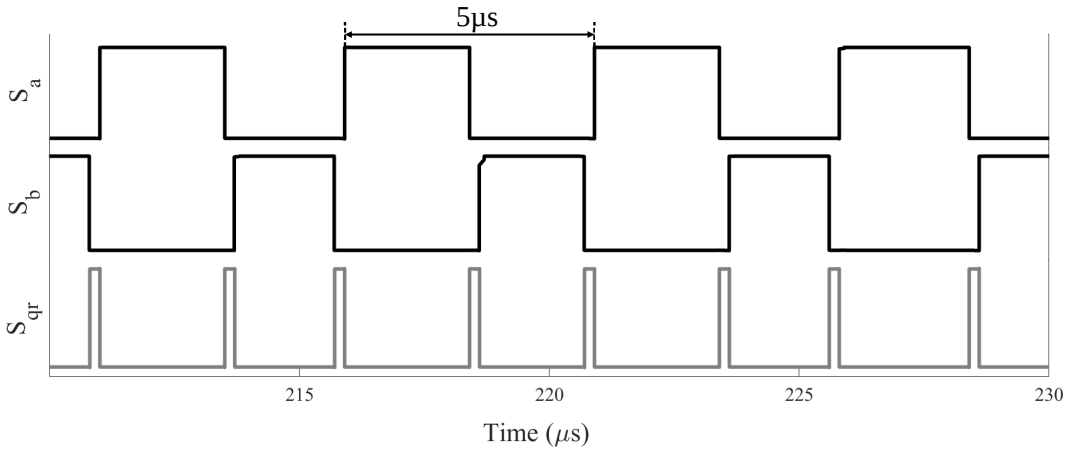


Figure 6.9: Clocks waveforms (post-layout simulation).

6.3 Comparator

The comparator circuit is considered the bottle neck of achieving ultra-low power consumption for the control circuit [64]. There are two main comparator circuit operation schemes, static and dynamic as shown in Figure 6.10. For both, the comparator consists of preamplifier stage, latch circuit and sometimes separate output stage. The preamplifier stage, which is usually implemented by a transistor differential pair, amplifies the input difference voltage to make it readable by the latch circuit. The latter decides whether the v_p is greater or less than v_n and outputs a logic signal, V_{DD} or ground, and sometime referred to as a decision circuit.

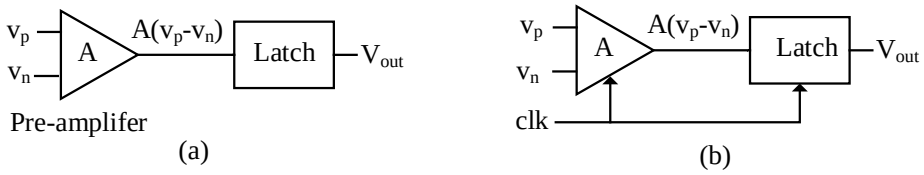


Figure 6.10: Comparator functional blocks: (a) Static comparator. (b) Dynamic comparator.

Generally, the static comparator consumes more power than the dynamic but requires no clocking signals. Figure 6.11 shows the CMOS implementations for a static and a dynamic comparator. It can be noticed that static comparator can be implemented using a conventional operational amplifier (opamp) CMOS circuit without internal compensation or feedback. The dynamic comparator requires a clock signal which is connected to the pre-amplifier stage as well as the latch circuit, M_8-M_{11}. Dynamic comparators are preferred due its low power profile [21]. Both comparators are studied and simulated for comparison purposes. Dynamic comparator is selected due its highly power efficient performance.

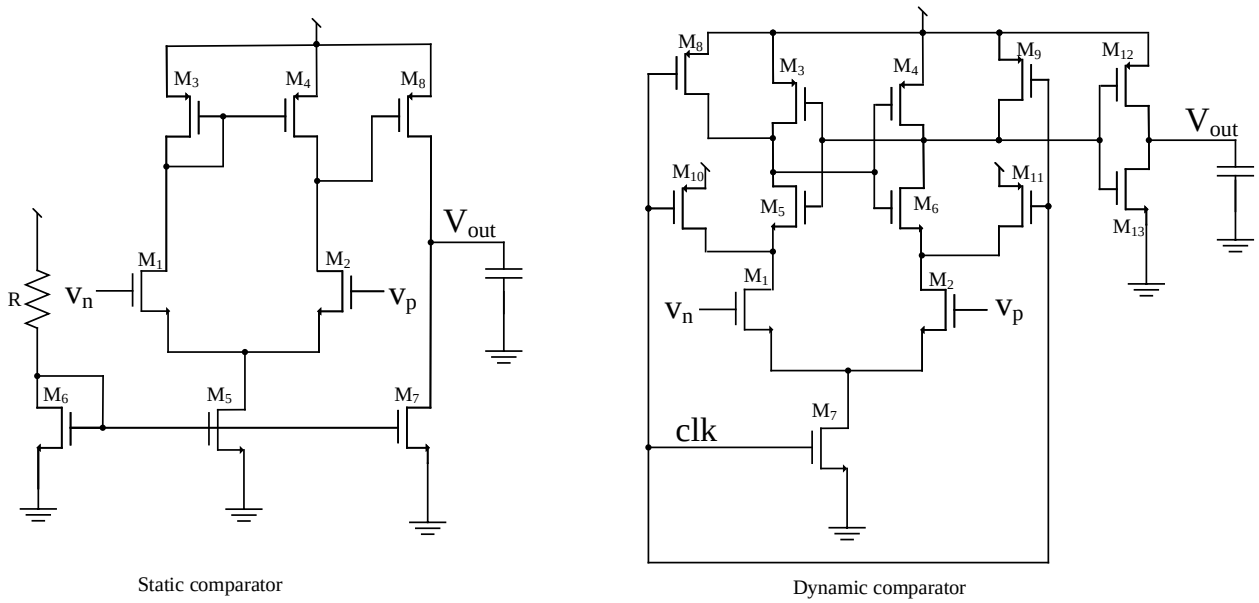


Figure 6.11: CMOS comparator structures.

For designing comparators, there are many static and dynamic merits need to be considered [65]. However, for this application we consider two parameters, offset voltage (V_{os}) and power consumption. The offset voltage is the minimum amount of input voltage difference that makes the output reaches mid-point. This is can be characterized easily for static comparators by applying DC simulation. On the other hand, finding V_{os} for the dynamic comparators is not trivial because transient analysis is needed due to the presence of a clocking signal [66, 67]. Nevertheless, a simple technique to estimate the offset is developed in three steps:

(1) V_{os} of a static comparator is found using DC simulation as mentioned earlier.

(2) The same static comparator is simulated in transient analysis, and we measure the minimum (v_p-v_n) that makes the output reaches mid-point, which is defined as $V_{os_{tr}}$. Then, a fitting factor is defined as x=$V_{os}/V_{os_{tr}}$.

(3) Using the same transient simulation, the dynamic comparator offset voltage can be approximated as $x * V_{os_{tr}}$, where $V_{os_{tr}}$ here is the dynamic comparator offset voltage in transient response.

The two comparators are simulated using Cadence Spectre simulator in C5 technology. For both, a 0.5V reference voltage (V_{ref}) is connected to v_n terminal and an input voltage that varies from 0-1V is connected to v_p, it is expected that when $Vin > V_{ref}$ the comparator outputs logic 1, i.e V_{out}=V_{DD}, and it outputs logic 0, i.e V_{out}=0, otherwise. The simulation for the static comparator with R=100$k\Omega$ shows that it has an offset voltage of 62mV, and consumes 1.6μW. On the other hand, the dynamic comparator consumes only 51nW which is almost thirty times less than the static comparator, and it experiences a 74mV offset voltage. Both comparators are loaded with 5pF capacitor. The dynamic comparator is operated using

200kHz which is provided by the CSRO circuit as discussed earlier, this is enough because input fluctuation is much less frequent [64]. Although we ignore the system propagation delay when designing the comparator, this parameter can be detrimental to the operation of the controller when there is a fast and abrupt variation in the input signal, i.e V_{in} changes from 0.3V to 0.5V in $> \phi_{comp}$ rate. This results in violating Nyquist rate theorem and hence unwanted results can be reported. The transistors in both circuits are sized to the inverter, i.e W_p=3μm and W_n=1.5μm and L_p=L_n=0.6μm. However, the differential pair use wider transistors, M_1 and M_2 with W=7.5μm, to provide enough gain for amplification.

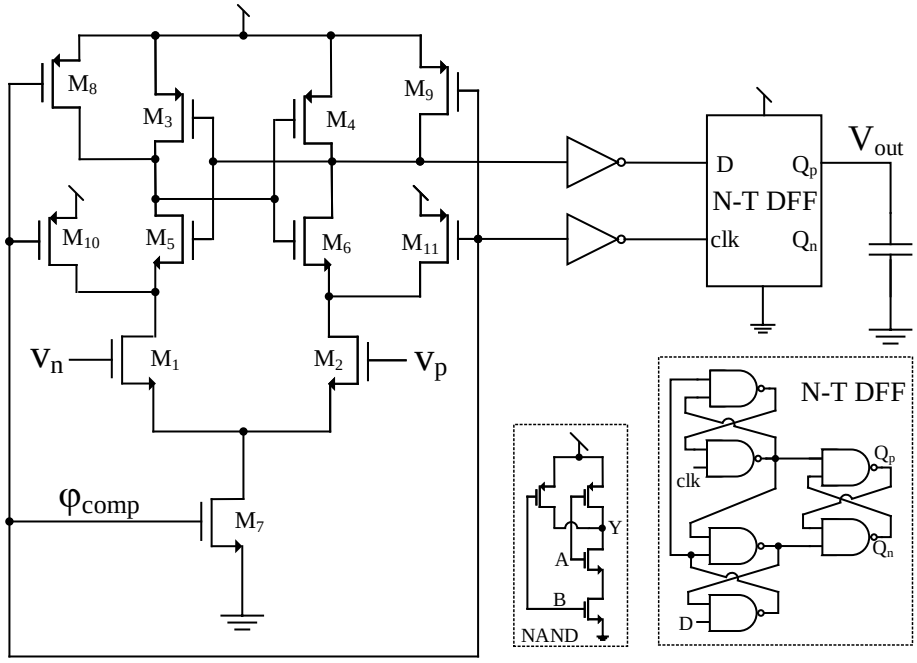


Figure 6.12: Proposed CMOS dynamic comparator.

The dynamic comparator is chosen for the intended circuit. However, this comparator makes a decision each clock which means it goes to zero as a stable state after clamping the output to V_{DD} in the case of higher positive terminal. This needs to be overcome by a mono-stable latch circuit, so the output will remain at the decision level, 0 or 1, until

Table 6.1: Truth table for N-T DFF.

Input		Output	
D	ϕ_{comp}	Q_p	Q_n
0	$\downarrow$	0	1
1	$\downarrow$	1	0

it makes another transition based on the change of the input. A Negative-Triggered D-flip flop (N-T DFF) is used to clamp the output voltage to either V_{DD} or gnd. The truth table of N-T DFF is shown in Table 6.1. The proposed dynamic comparator with N-T DFF is shown in Figure 6.12. The layout is shown in Figure 6.13, and it occupies an area of only $0.003mm^2$. The post-layout simulation is performed to account for parasitics and to allow re-optimizing the transistors sizes. Figure 6.14 shows the waveforms for V_{out}, V_{ref} and V_{in}. It can be seen that the proposed comparator outputs V_{DD} when $V_{in} > V_{ref}$ which meets the expectations. The gearbox controller layout is depicted in Figure 6.15.

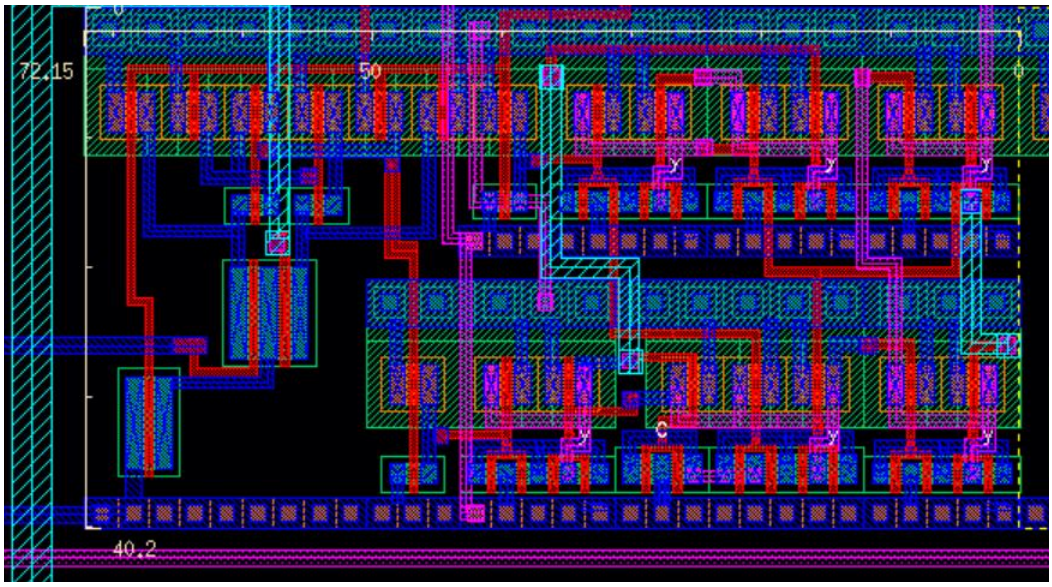


Figure 6.13: CMOS dynamic comparator layout.

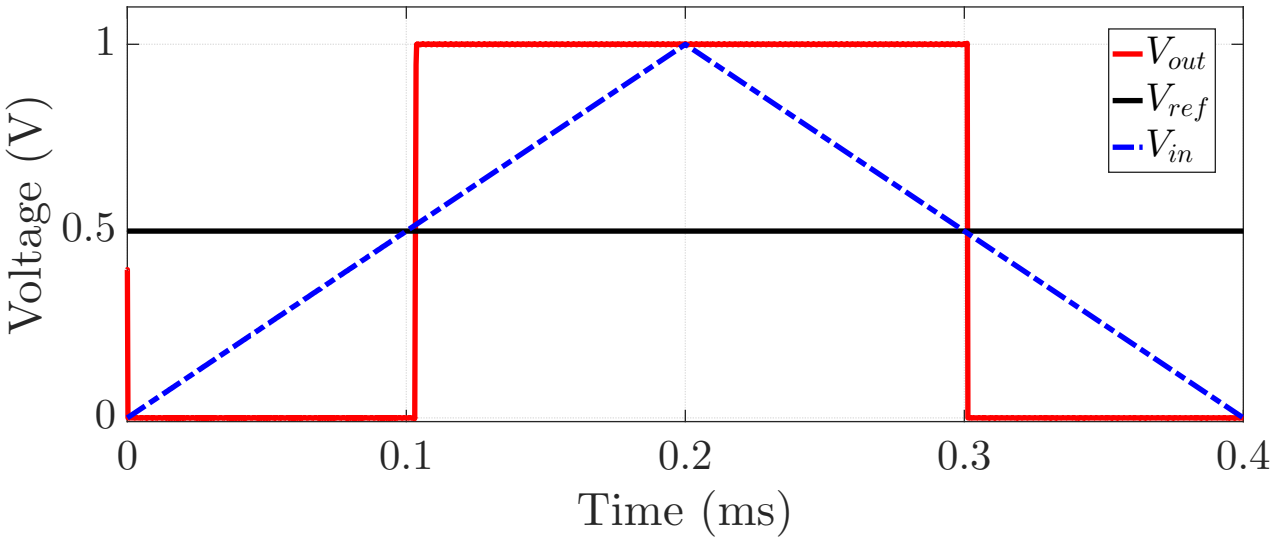


Figure 6.14: Post-layout simulation for the proposed dynamic comparator.

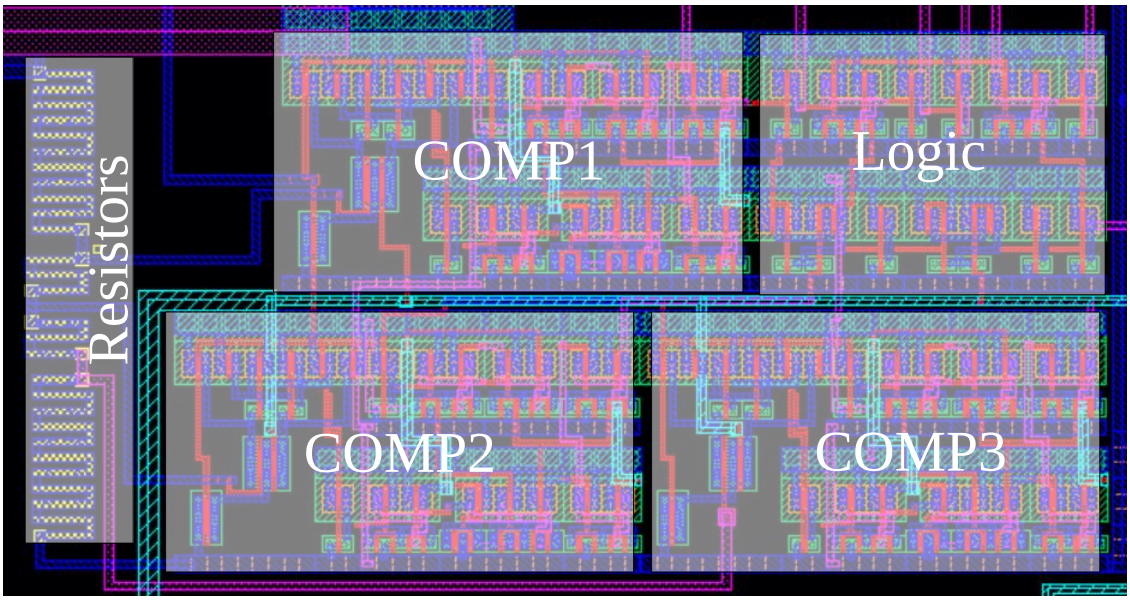


Figure 6.15: The gearbox controller layout.

6.4 IO Pad Design

The IO pads design is very critical as it connects the IC to the outside world. IO pads should have Electro-Static-Discharge (ESD) to protect the IC from excessive charge that may damages the devices, especially switches. There are very advanced techniques to implement ESD. However, in the proposed IC, a simple ESD circuit is used as shown in Fig. 6.16. Two diodes, D_1 and D_2, with large areas are used to clamp the internal pin to the power rails, V_{DD} or gnd. When the pin is exposed to a high static voltage greater than V_{DD}+V_{diode}, D_1 conducts discharging the excessive charge and clamping the pin to V_{DD} as illustrated by the red line in Figure 6.16. On the other hand, if the IO pin experienced a negative charge with voltage less than the diode voltage, D_2 conducts discharging it to gnd and grounding the pin potential (the green dashed line).

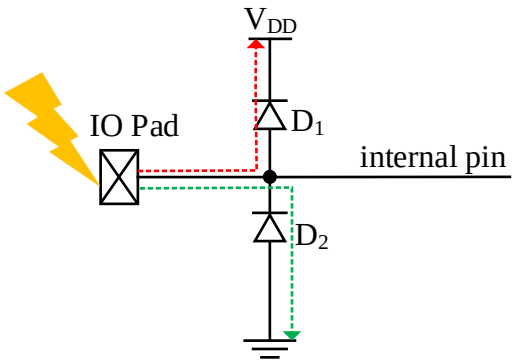


Figure 6.16: ESD for IO pads.

This circuit provides a relatively good ESD protection and consumes no active switching or complex structure. However, for circuits that are meant for commercial use, other complicated ESD can be applied.

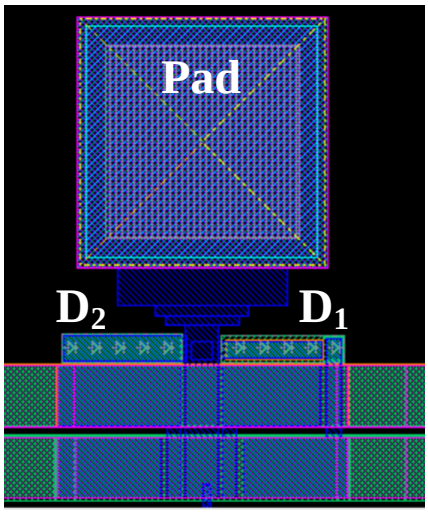


Figure 6.17: Layout of an IO pad with ESD.

6.5 Final Layout and Post-Layout Results

The final chip layout including flying capacitors, input and output coupling capacitors, is shown in Figure 6.18, and it occupies 4mm^2 die area. Also, it can be seen that the controller circuit with the converter switches occupy only 0.0754mm^2 which is almost 1.89% of the total die area. For the pin configurations, the main IC pins are V_{in}, V_{out}, gnd and the tuning pins (C_{da}, C_{db} and V_b). The biasing pins (V_{DD1}, V_{DD2} and V_{DDRef}) are added as a backup if the on-chip auxiliary charge pump fails to provide power for the circuit. The gate signal pins (S_{qr}, S_{aRO}, S_{bRO}, S_{g1-g5}) are utilized for debugging purposes. All other pins are used for additional FSC cells. Table 6.2 defines all IO pins.

Before tape-out, the design-rule-check (DRC), the layout-vs-schematic check (LVS) and parasitic extraction have been done using Diva tool in Cadence. Analog Design Environment (ADE) has been used to perform all simulations using Specter simulator. All circuits have been re-optimized after extensive round of simulations including the parasitics, referred to as a post-layout simulation.

Table 6.2: IC pin configurations.

No.	Pin	Description
1	T_{k_4}	Mid-point connection for cell_4
2	T_{B_4}	Bottom-plate flying capacitor connection for cell_4
3	T_{P_4}	Top-plate flying capacitor connection for cell_4
4	SO_{in}	Input for S_{out} switch
5	SO_{out}	Output for S_{out} switch
6	SO_g	Gate driving signal for S_{out} switch
7	S_{g_5}	Probing gearbox control signal for S_{g_5} switch
8	S_{g_4}	Probing gearbox control signal for S_{g_4} switch
9	S_{g_3}	Probing gearbox control signal for S_{g_3} switch
10	S_{g_2}	Probing gearbox control signal for S_{g_2} switch
11	S_{g_1}	Probing gearbox control signal for S_{g_1} switch
12	$S_{b_{RO}}$	Probing on-chip ring oscillator signal {S_b}
13	$S_{a_{RO}}$	Probing on-chip ring oscillator signal {S_a}
14	S_{qr}	Probing on-chip QRU signal
15	C_{da}	Dead-time tuning capacitor for on-chip N-OV circuit
16	C_{db}	Dead-time tuning capacitor for on-chip N-OV circuit
17	V_b	Oscillation frequency tuning for on-chip CSRO
18	V_{cpIn}	Input for on-chip auxiliary CCCP
19	V_{in}	Input for the configurable FSC chip
20	gnd	Ground reference for the configurable FSC chip
21	V_{out}	Output of the configurable FSC chip
22	V_{cp}	Output of the on-chip auxiliary CCCP
23	V_{DD_1}	Backup biasing source for all controller circuits
24	V_{DD_2}	Biasing source for level shifters
25	V_{DDRef}	Backup biasing source for gearbox reference voltage
26	S_a	External gate driving signal to all additional FSC cells
27	S_b	External gate driving signal to all additional FSC cells
28	T_{in_1}	Input connection for cell_1
29	T_{k_1}	Mid-point connection for cell_1
30	T_{B_1}	Bottom-plate flying capacitor connection for cell_1
31	T_{P_1}	Top-plate flying capacitor connection for cell_1
32	T_{in_2}	Input connection for cell_2
33	T_{k_2}	Mid-point connection for cell_2
34	T_{B_2}	Bottom-plate flying capacitor connection for cell_2
35	T_{P_2}	Top-plate flying capacitor connection for cell_2
36	T_{in_3}	Input connection for cell_3
37	T_{k_3}	Mid-point connection for cell_3
38	T_{B_3}	Bottom-plate flying capacitor connection for cell_3
39	T_{P_3}	Top-plate flying capacitor connection for cell_3
40	T_{in_4}	Input connection for cell_4

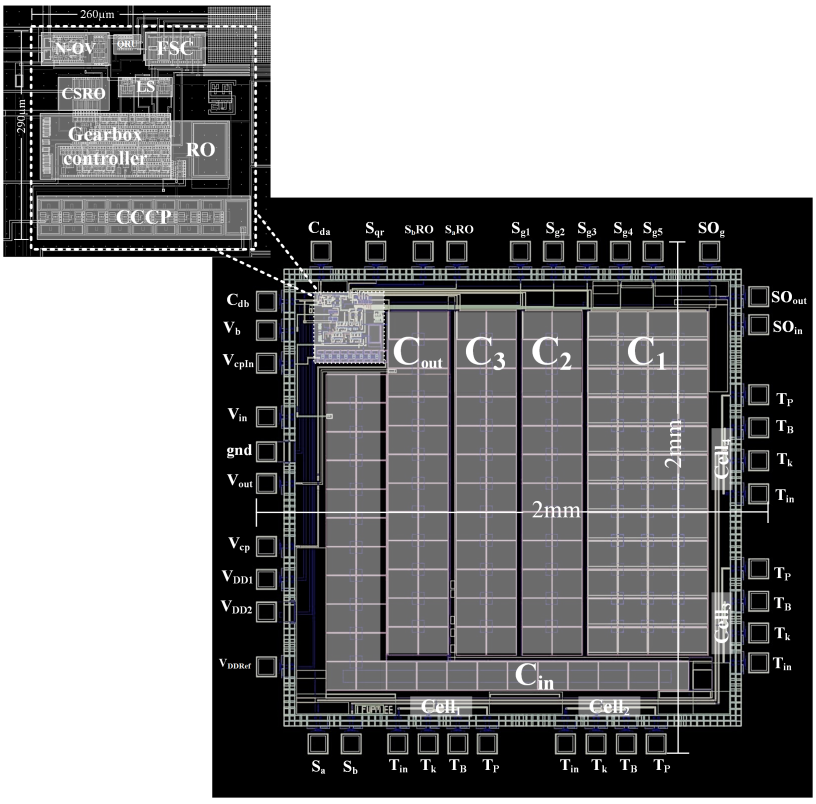


Figure 6.18: The chip layout with pin configuration.

The final IC has been simulated for 0.3-0.6V input voltage range and various load changes. Previously in the design stage, the optimal efficiency was found at 59% but with assumption of regulated output voltage of 1.5V. The adaptive VCR is built using forward controller, and hence the system does not respond to load change. As a result, the output voltage is not fully regulated, see Figure 6.19 that shows the transient response of the output voltage for two load cases, no load and 1μA load. With only a capacitive load, the system provides an output voltage of 1.4V and it drops to 1.24V with 4.6mV ripple in response to 1μA load. This μW power level is useful in many applications. For example, a neural signal detector presented in [68] consumes only 0.78μW. The miniaturized pacemaker proposed in [69], requires 1.2μW using 1.3V supply voltage. In addition, a wireless temperature/pressure sensor is presented in [70] for continuous intraocular pressure monitoring, and dissipates

2.3μW with 1.5V source. Considering WSN application,we can point to two examples. The first one is a wireless receiver that works on a wake-up approach, and consumes around 2.4μW at 1V supply [71]. The second example is a CMOS image senor found in [72], which can be used for monitoring, and it requires 1.36μW power. These are few examples of many for μW and sub-μW level applications.

The efficiency profile for different loads is shown in Figure 6.20, including the theoretical case where no charge recycling is applied. Only an error of less than 6.3% has been noticed in the efficiency between the post-layout simulation and the analytical estimation of P_{loss} in equation (5.12). The converter has a peak efficiency of 47.5% for 5.2μA load current, and maintains efficiency $\geq$ 40% for 2.4$\sim$8.8μA. Nevertheless, the output voltage is not fully regulated to the load due to the absence of a feedback controller. Figure 6.21 shows the output voltage verses different loads. It is found that V_{out} $\geq$1V is available for $\leq$ 6.5μA load current. Regarding the VCR, a discrepancy of $\leq$ 6% is noticed between the expected and simulated VCR as depicted in Figure 6.22 for $V_{in} \leq$ 520mV, and it is kept under 11.5% for 0.52-0.6V input voltage.

Finally, a performance comparison between the proposed converter and other state-of-the-art converters is summarized in Table 6.3. One can notice that the proposed controller exhibits low power consumption which is almost 2.8x less than the minimum controller, i.e 342nW compared to 971nW in [49]. Also, the proposed converter provides a monolithic solution, i.e no off-chip components are required, as same as [73]. But converters in [73] and [74] use a native NMOS device which is not available in some process like C5. Therefore, they are considered as unportable[1] compared to all others. In terms of efficiency, despite

[1]Technology portability means that the proposed structure can be implemented in all standard technologies because there are no special devices involved in the design.

the fact that [49] and [75] score higher than 80%, a high input voltage was used in [49], 1-1.5V, along with dual MIM capacitor which has lower parasitics and it is not available in C5. For example, the parasitic ration, α, in [75] is only 1%. Moreover, the losses reported in [75] are around 31μW, for all losses, which means for few μW the efficiency will drop below 30%. The efficiency of the proposed converter is relatively below 50% because we are limited to PIP capacitors which has almost 13% parasitic ratio and starting up from low voltage (300-600mV).

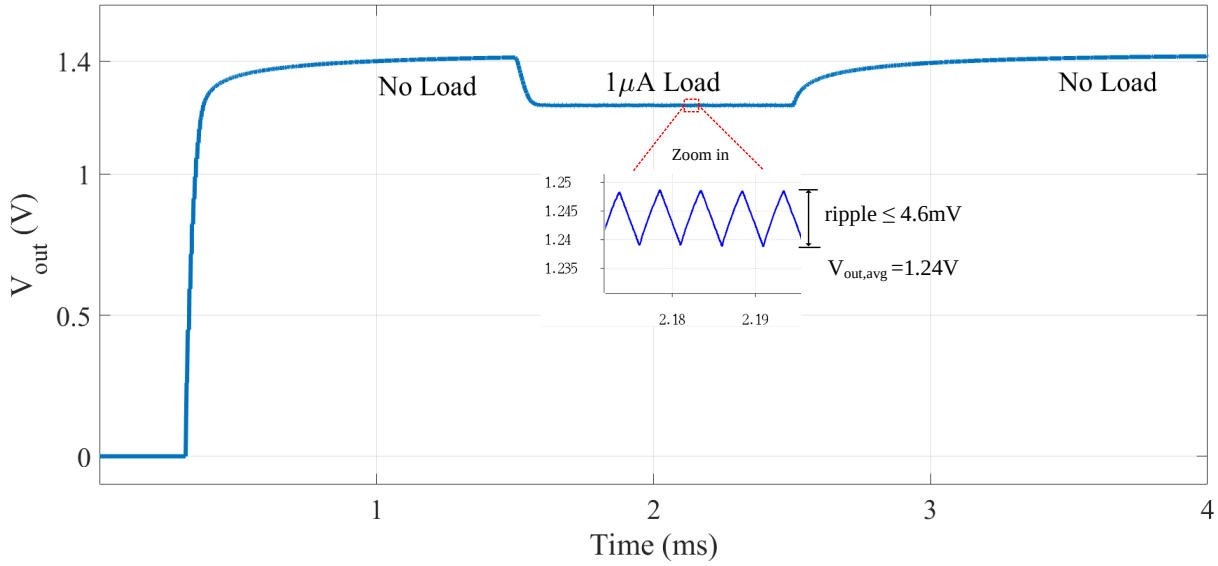


Figure 6.19: Efficiency verses I_{out} for the proposed FSC converter with 300mV input voltage.

6.6 Summary

In this chapter, the details of designing, simulating and testing the IC FSC has been covered. The proposed converter boosts the low input voltage to 1.4V (with no load) and 1.24V (with μA load) which can be used to power up a battery-less system like a wireless sensor node and/or an implanted biomedical sensor which usually requires few μW to wake-up and sends

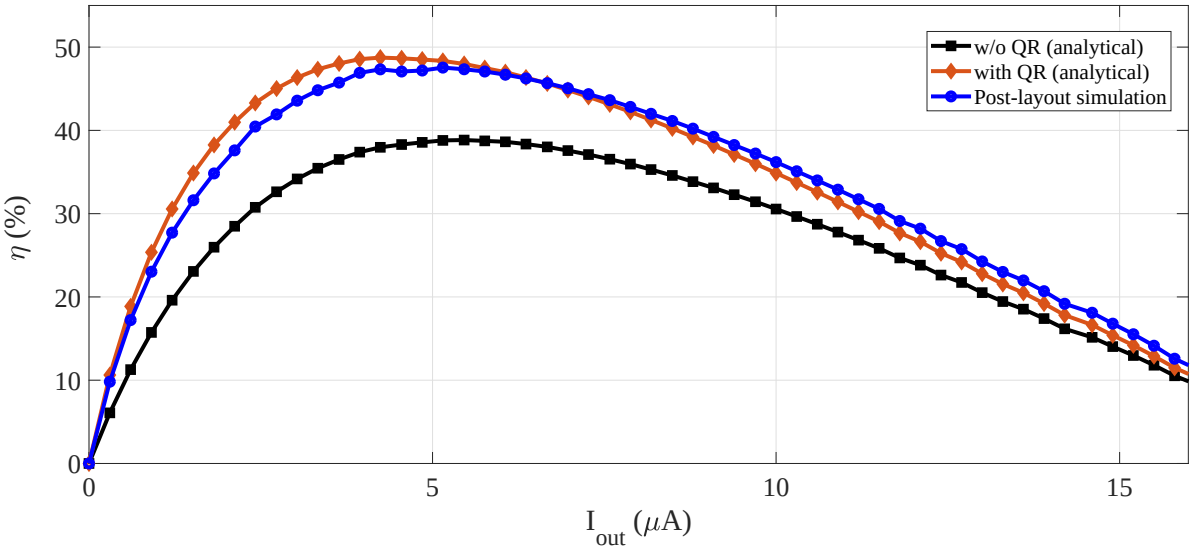


Figure 6.20: Efficiency verses I_{out} for the proposed FSC converter with 300mV input voltage.

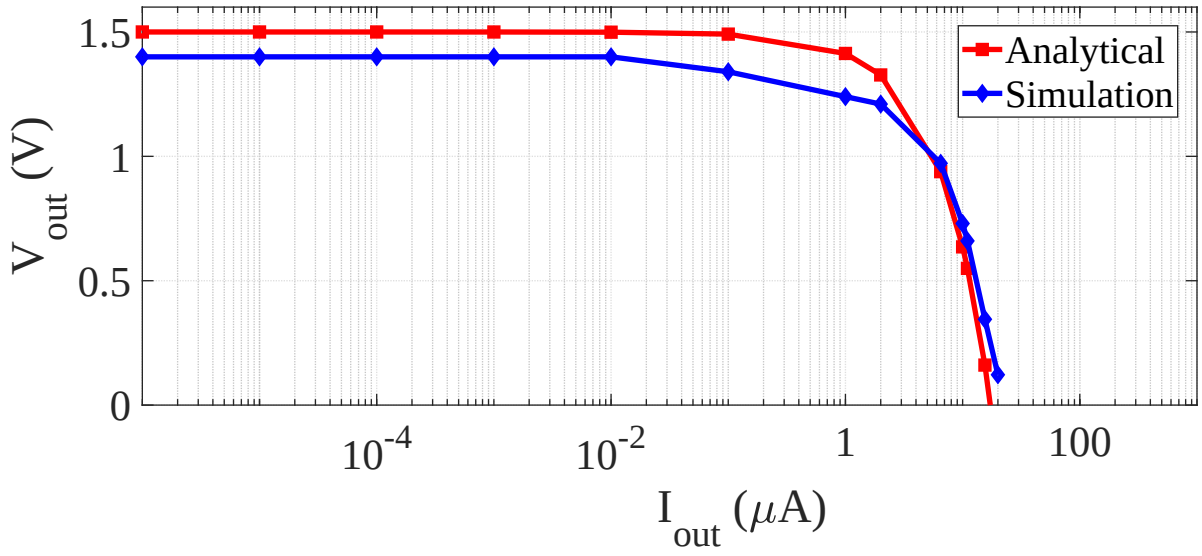


Figure 6.21: V_{out} verses I_{out} for the proposed FSC converter with 300mV input voltage.

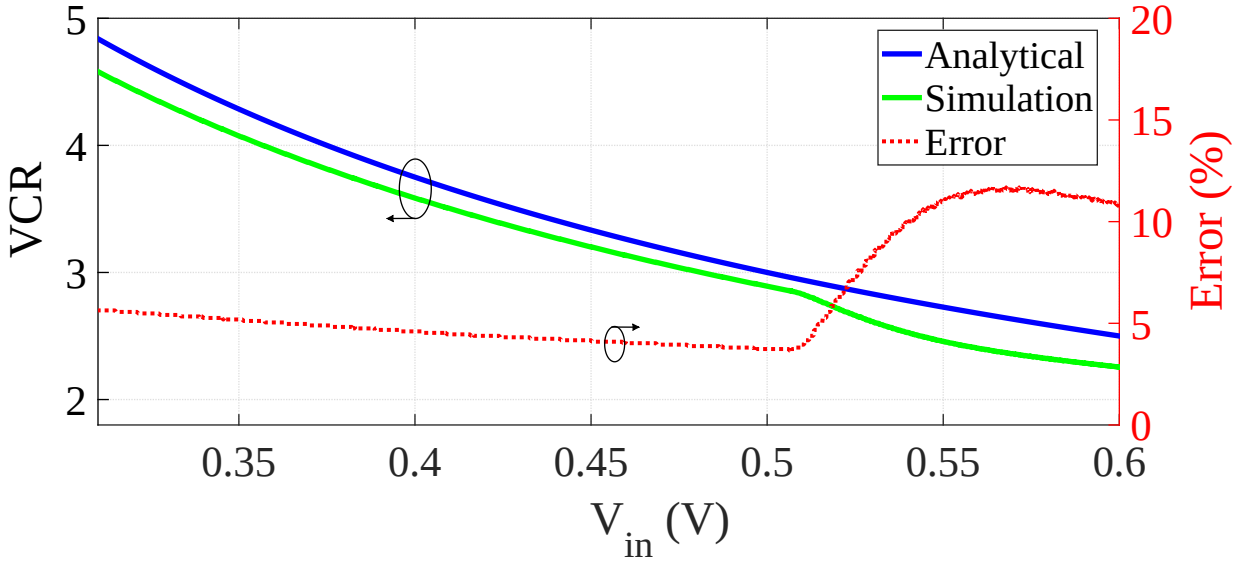


Figure 6.22: VCR verses V_{in} for the proposed FSC converter.

Table 6.3: Performance Comparison with SC converters in the literature.

Reference	JSSC'16 [76]	JSSC'15 [49]	TCAS'11 [73]	TBCAS'17 [74]	TCAS'15 [75][a]	This Work[a]
Tech. node	180nm	130nm	65nm	250nm	250nm	500nm
Topology	Dickson	2-stage SC doubler	4-stage Dickson	8-stage Dickson	4-stage Series-Parallel	3-stage Fibonacci
Input voltage	0.25-1.1V	1.1-1.5V	0.35-0.48V	0.22V	0.5- 2.5V	0.3-0.6V
Output voltage	1.8-2V	3.3V	1.4V	1.8V	1-1.4V	1-1.4V
Controller loss	1.18μW	971nW[b]	3μW	NA	6μW	**342nW**
Capacitor type	MIM	Dual MIM	NA	NA	MIM	PIP
Peak efficiency	48%	86.4%	58%	68%	83%	47.5%
Max. P_{out}	70μW[c]	21μW	11μW	645μW	120μW	6μW
Tech. portable?	Yes	Yes	Restricted	Restricted	Yes	**Yes**

[a]Post-layout simulation

[b]Calculated from the results

[c]Three power domains were reported. Low ($< 40\mu$A load) , medium ($40 - 210\mu$A load) and high (0.21-1mA load)

or process information.

Chapter 7

Conclusions and Future Work

7.1 Conclusions

In this dissertation, we introduced the variable FSC converter as a good candidate for low power applications. We first studied the fundamental theory of SC converters where we proposed a generalized equation to overcome some limitations found in the theory. This generalization allows to identify the true voltage conversion performance limits of specific number of k capacitors. In addition, the theory developed in chapter 2 leads us to propose a unified algorithm to solve the FSC converter synthesize problem as discussed in chapter 3.

Moreover, the power loss analysis and optimization techniques for both discrete and integrated implementation of variable FSC have been discussed throughly in details in chapters 4and 5. Design procedure flow for both converters was proposed. An on-line variable FSC synthesizer using proposed algorithm in chapter 3 is developed and available as an open-source tool to help synthesizing FSC converters.

Also in this work, the challenges of implementing monolithic FSC converters were studied, such as startup and parasitic capacitors losses, see chapters 5 and 6. We proposed a startup circuit using cross-coupled charge pump with ring oscillator which is a magnetic-free startup. To overcome the parasitic loss, the dead-time charge recycling was employed by maintaining the charge in the parasitic capacitors during the dead-time bands. For the controller circuit, a dynamic comparator was designed and simulated. Despite that fact that this comparator

was optimized for the proposed FSC controller, it can be employed in many low power applications.

7.2 Future Work

In academia, there is always a room for improvement. The SC converter research has a potential for many applications involving any kind of power conversion. Therefore, for a future work, the following directions can be considered:

- **Design tool:** as part of the FSC synthesizer development, the design process of finding the multiplier vectors, i.e a_r, a_c and a_v discussed in chapter 4, can be automated.

- **MIMO SC converters:** these converters can be useful in applications that has many inputs and/or delivering power to different loads with distinct voltage levels. An overview study has been conducted in [77], and a recent MIMO SC converter is proposed in [78] where the parasitic capacitors were employed to perform the charge transfer. Speaking of applications, see Figure 7.1, MIMO SC converter shows a potential to be utilized as an on-chip power management unit that responds to different voltage domains required by on-chip processors [79–81]. In addition, MIMO SC converters can be employed as a centralized DC-DC converter block in energy harvesting system extracting energy from more than one ambient source with low voltage profile. Therefore, the following questions can be further explored to promote the implementation of these converters: (**Q1**) How to synthesize MIMO SC converters? Initial thoughts were proposed in our published work [12], and (**Q2**) How to model MIMO structure? which helps understanding the system behavior in response to presence/absence of some inputs and outputs.

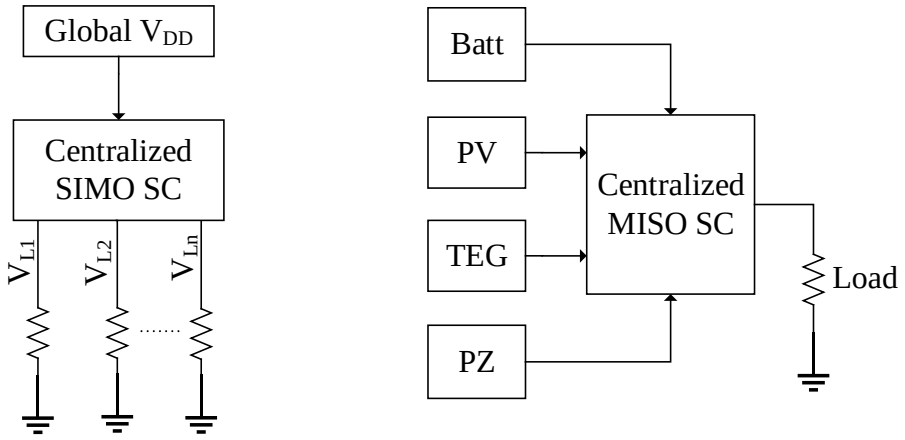


Figure 7.1: MIMO SC conceptual blocks for possible applications: (left) on-chip power management unit for microprocessors, and (right) energy harvesting system.

- **On-chip devices:** in this work, the on-chip capacitors is considered a major obstacle towards high efficient SC converters. In fact, there are many integarble capacitor structures like trench capacitor with higher capacitance density. Nevertheless, the capacitance density can be further increased to 100-200x using on-chip supercapacitors which can be considered as a game changer device. Supercapacitors were introduced in 1950, whereas the on-chip version took almost 60 years to be demonstrated. These capacitors are based on double layers structure, and hence they can soak the energy much faster and deliver them with a relatively constant voltage profile. So, supercapacitor are featured with higher energy storage, low ESR which enables fast charging and high surge current delivery. In fact, utilizing on-chip supercapacitors minimize the overhead die area improving both, the power density and converter efficiency. The on-chip supercapacitors are now achievable on silicon substrate as demonstrated in [82, 83], but it needs some time to be introduced in the normal foundry process. Meanwhile, developing on-chip supercapacitors featuring low parasitics and using a simple fabrication process and structure, leads to high efficient on-chip converters.

- **High Gain Operation**: Fibonacci converter provides highest gain possible with least number of capacitors and switches as discussed in chapter 2, which lends itself to a high gain requirement on-chip. Examples of on-chip high gain systems include LCD driver [84], LED driver [85] and MEMS, **M**icro-**E**lectro-**M**echanical-**S**ystems, driver [86], which usually require high voltage operation, i.e >20V. Also, a high VCR is needed for energy harvesting systems that employ TEG sensors, because the open-output-voltage of the TEG can be in the range of few tens of mV for 1-2K. So, FSC issues in high-gain operation can be also investigated to find out the limits and design requirements.

- **AC operation:** although in this work we only consider DC-DC operation, the SC converters can be synthesized in a way to introduce inversion for the V_{in} or V_{out} as verified in chapter 2. Consequently, AC-DC or DC-AC operation can be achieved. However, high voltage seen at the AC mains (120-230VAC) is considered a major limiting factor for the fabrication process because most standard technology processes offer low voltage ratings, e.g C5 has 5V rating. As an example for possible on-chip inverter implementation, [87] demonstrated a monolithic 120/230VAC to 3.3V inverter that delivers power to 3mW load targeting Internet-of-Things (IoT) and smart home applications. But, this on-chip inverter was implemented using two stages, rectification and step-down dc-dc conversion. Other possible option is to employ only one stage of SC converter that can performs both operations at once.

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