BUCK/BOOST CURRENT-SOURCE-INVERTER TOPOLOGIES, MODULATION AND APPLICATIONS IN HEV/EV MOTOR DRIVE

by

Qin Lei

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ABSTRACT

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To provide higher boost ratio in motor drive or PV application, a new family of switched-coupled-inductor inverters has been proposed in this work, with voltage buck-boost function. The voltage-fed switched-coupled-inductor inverter has higher boost ratio and lower active device voltage stress than Z-source inverter at the same voltage gain, and has wider voltage buck/boost range than conventional boost-converter inverter. The current-fed switched-coupled-inductor inverter is a capacitor-less solution among the buck-boost inverters, which reduces the system size significantly. Compared to traditional boost-converter-inverter, it has less switch count, and less active device current stress.

To achieve higher efficiency with a single-stage buck-boost inverter for HEV/EV motor drive application, a current-fed quasi-Z-source inverter topology has been selected and a 24kW prototype has been built in the lab. A zero vector placement technique in SVPWM has been proposed for this inverter to obtain lowest switching loss, lowest current ripple, lowest output harmonics and lowest voltage spike on the device in both constant torque and constant power operation regions, in order to achieve higher efficiency, higher power density and lower cost. A 24kW current-fed quasi-Z-source inverter has been built in the lab and tested. The full power rating efficiency reaches 97.6%, and peak efficiency reaches 98.2%, both of which have a 3%-4% improvement on traditional two stage configuration. The power density is 15.3KW/L, which also has 30% improvement on the commercial unit in HEV.

To achieve higher switching loss reduction, a Space-Vector-Pulse-Width-Amplitude Modulation (SVPWAM) method has been proposed for buck-boost current source inverter. By using this method, the switching loss is reduced by 60%, and the power density is increased by a factor of 2 to 3, with a less output harmonic distortion than normal SVPWM method. A 1 kW boost-converter-inverter prototype has been built and tested using this method. The overall system efficiency at full power rating reaches 96.7% and the whole system power density reaches 2.3 kW/L and 0.5 kW/lb, all of which are remarkable at this power rating. As a result, the proposed SVPWAM can make the buck-boost inverter suitable for applications that require high efficiency, high power density, high temperature, and low cost, such as EV motor drive or engine starter/alternator.

To implement buck-boost function on direct matrix converter, four control methods including simple maximum boost, maximum boost, maximum constant boost control and hybrid minimum stress control have been proposed for the newly proposed direct Z-source matrix converter, and verified with simulation/experiments.

Two new discontinuous operation modes have been proposed for current-fed quasi-Z-source inverter topology. Simulation and experiment results are given to verify the theoretical analysis. A transient state-space model has been built for current-fed quasi-Z-source inverter to demonstrate its fast transient response in motoring and regenerating transition. The analytical, simulated and experimental results all show that the inverter only needs several switching cycle to complete the transition, which makes it suitable for HEV/EV motor drive application.

Dedicated to:
My parents, Chuping Lei and Airong Wang
My husband Junjun Xin,
And my brother Qiwei

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CHAPTER 1 INTRODUCTION

The Z-source inverters (ZSIs) have been proposed in [1] to overcome the limitations and problems of the traditional voltage-source inverter (VSI) and current-source inverter (CSI), which provide an attractive single-stage dc-ac conversion that is able to buck-boost voltage, increase efficiency and reduce cost. However, the ZSIs still have some drawbacks. The main drawback of the voltage-fed ZSI is that the input current is discontinuous in the boost mode and the capacitors must sustain at a high voltage, while the main drawback of the current-fed ZSI is that the inductors must sustain high currents. The quasi-Z-source inverters (qZSIs) have been proposed in [2] to further improve on the traditional ZSIs. Besides the advantages inherited from the ZSIs, the qZSIs also have their own merits, including reduced passive component ratings, continuous input current, a common dc rail between the source and inverter, and so on.

Since the publication of ZSIs, the voltage-fed ZSI received more attention than the current-fed ZSI. The performance, control methods and applications of voltage-fed ZSI are well-investigated in [3]–[11]. Nevertheless, it has a significant drawback that cannot maintain bidirectional power flow. The bidirectional power flow can only be achieved by replacing the diode with a bidirectional conducting, unidirectional blocking switch [12]–[13]; however, in this case, the advantages of single-stage topology are missing. The current-fed ZSI/qZSI, unlike the voltage-fed ZSI/qZSI, is bidirectional with a diode. The regeneration capability with a single-stage configuration makes the current-fed ZSI/qZSI a competitive power converter topology. Moreover, with the newly developed reverse blocking IGBT (RB-IGBT), the CSI is becoming more efficiency and thereby more attractive [14], [15].

1.1. Problems of conventional current source inverter topology

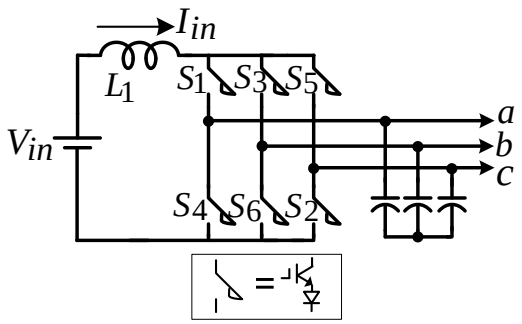


Figure 1.1. Conventional IGBTs and series diodes based CSI

The conventional current-source inverter as shown in Figure 1.1 has two major problems: unidirectional power flow and voltage boost operation, which make it impossible to be used in many applications, such as hybrid electric vehicles and general purpose variable-speed motor drives.

The CSIs are less investigated and applied, compared to the VSIs, partly because the switches of the CSI have to be reverse blocking. If IGBTs are used for the current-source inverter, the reverse blocking capability can only be achieved with diodes connected in series to the IGBTs as shown in Figure 1.1. This yields to relatively high semiconductor conduction loss. The newly developed RB-IGBT has the symmetrical voltage blocking characteristic. That is, it can block both forward and reverse voltage in its off state [14], [15]. The improvement of the semiconductor switches has made CSIs more attractive in several applications, as in uninterrupted power supplies (UPSs), ac drives and reactive power compensators due to its intrinsic output short-circuit protection, ruggedness and direct current control ability [16-17].

The conventional CSI has nine possible switch states, of which three are zero states (vectors) and six are active states. Three zero states can be assumed by turning ON an upper

switch (S_1, S_3 or S_5) and a lower switch (S_4, S_6 or S_2) from the same phase-leg. Six active states can be assumed by turning ON the switches from different phase-legs. A relationship between the *rms* value of output phase voltage (V_o), power factor ($\cos\phi$), input dc voltage (V_{in}) and the modulation index (m) can be determined:

$$V_o = \frac{2\sqrt{2}V_{in}}{3\sqrt{3}m\cos\phi} \tag{1.1}$$

Equation (1.1) indicates the CSI can only boost voltage. For a given power factor load, decreasing m leads to higher output voltage, as in the boost converter the increment of the duty cycle leads to higher output voltage. When m is the maximum value (i.e. $m = 2/\sqrt{3}$), we can get minimum output ac voltage, $V_{o\_\min} = \frac{\sqrt{2}V_{in}}{3\cos\phi}$. Let's define two operation modes: motoring operation (power flows from dc side to ac side) and energy regeneration operation (power flows from ac side to dc side). If $\cos\phi < 0$, the CSI can draw energy from ac side to dc side. However, the polarity of the input voltage in motoring and in energy regeneration operation is opposite from each other. Since the input voltage source, such as battery, cannot change the polarity in practice, the CSI is effectively unidirectional. In conclusion, the conventional CSI has two major problems: unidirectional power flow and voltage boost operation, which makes it impossible to be used in many applications such as hybrid electric vehicles (HEVs) and general purpose variable speed motor drives.

1.2. Problems of conventional current source inverter modulation

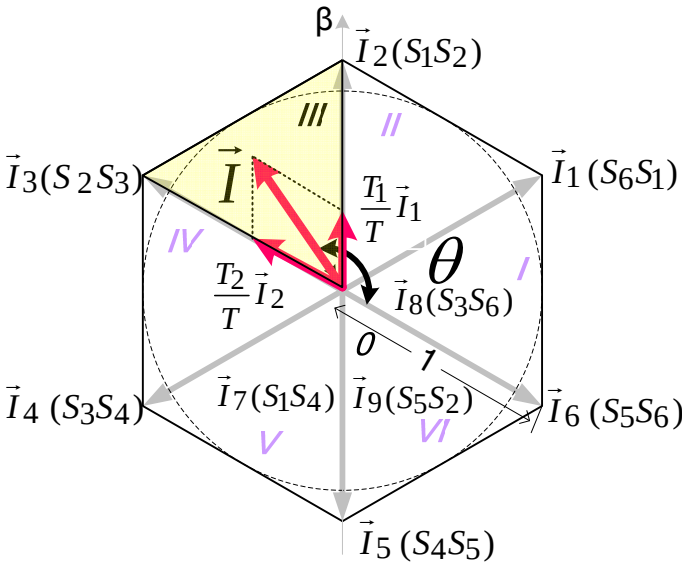


Figure 1.2. Space vectors of the CSI (For interpretation of the references to color in this and all other figures, the reader is referred to the electronic version of this dissertation)

There are many kinds of modulation methods for current source inverter and voltage source inverter proposed previously. There are two basic types of modulation methods: carrier based regular sampled method (including continuous PWM[18-23] and discontinuous PWM[24-28]); space vector PWM control [27, 29-31]. Paper[22] utilized master and slave references to be compared with carrier directly to generate a switching pattern instead of using mapping method [20], but it didn't reduce switching frequency or increase current utilization compared to SVPWM control. Paper[26] proposed two generalized discontinuous carrier-based pulse width modulation (GDPWM) methodologies for CSI to reduce the switching frequency further by 1/3. However, the discontinuous PWM introduces higher harmonics in the output and also higher temperature variation of the device package. paper[28] presented a vector PWM method to minimize the switching loss, by placing zero vector at proper sector and by injecting triplet harmonics. Similarly for current source inverter, the zero vectors can be intentionally arranged to bring down the switching loss.

Paper[24] presented a dead-band PWM pattern which makes a 33% switching frequency reduction for a equivalent harmonic spectrum, compared to SPWM, but it has the same problem as DPWM. Paper[34] concluded that the third harmonic injection method is better for low modulation but modified SPWM is better for high modulation in terms of harmonic and ripple current.

Various types of Z-source inverter modulation have also been proposed in the old literatures. Papers [1, 4, 32-33] proposed the carrier-based PWM control method. Paper [4] presented a method utilizing the maximum shoot through duty ratio in order to achieve minimum voltage stress on active devices; however, the varied shoot through duty cycle may introduce six times base frequency harmonics in output. In order to overcome this problem, paper [32] proposed a maximum constant boost control which injects a zero sequence voltage in the reference to make the shoot through duty cycle constant. Papers [1, 33] presented a method which inserts the open zero state into the edge of PWM, in order to reduce the number of switching, however, it may cause larger power loss due to multiple times of diode reverse recovery.

The evaluation process for different modulation methods has been researched by many papers [27, 35-38]. Basically the evaluation criteria includes switching losses[84, 27, 28, 38-40], current/voltage ripple[34], harmonics[29, 36, 41, 42] and implementation complexity.

PWM sequence is defined as a function of modulation index and power factor. From the state average point of view, each switching vector can be displaced anywhere within the switching cycle because the displacement has no effect on the amp-second average of the resulting current pulses corresponding to the reference vector[39]. The sequence of switching

vectors should minimize the inverter switching loss, inductor current ripple and output voltage/current harmonics[31].

Paper[39] presented several kinds of switching sequences such as FSM, HSM, MHSM, MFSM, CSVM, and also concluded that CSVM is better than others if M<0.64.

This dissertation selects the SVPWM control to achieve higher input current utilization, lower switching loss and lower total harmonic distortions. For both voltage-fed and current-fed Z-source inverter, there are four switching states at any switching cycle, including two active states, one short zero state (shoot through state in voltage-fed Z-source inverter), and one open zero state. So there is more flexibility to arrange them to get the same volt-second equation, but different performance. In the modified SVPWM control method for this circuit, different PWM sequences can lead to different switching loss, current ripple, total harmonic distortion, and also the voltage spike on the switching devices. For each optimizing target, several rules which results in better performance have been summarized. A group of sequences have been sieved according to these rules. A complete analysis has been given to select the optimized sequence.

In order to further reduce the switching loss in the inverter, a space vector pulse-width-amplitude modulation (SVPWAM) has been proposed. If it is used in voltage source inverter, a front stage dc-dc converter is needed to generate a variable dc link voltage, and then fed to inverter. In HEV/EV motor drive application, the two stage boost-converter-inverter is a classical topology, since the battery voltage is designed to be lower or equal to half of the motor drive input voltage. Also because of this boost converter, the dc link voltage of inverter is possible to be controlled. A 1kW boost-converter-inverter

system is built here to demonstrate the power loss reduction of SVPWAM. Both simulation and experimental results are given. Secondly, for SVPWAM application in current source inverter, the topology “current-fed quasi-Z-source inverter” is selected to be a representative of a voltage buck/boost current source inverter. The dc link voltage can be controlled to be desired variable voltage by regulating the extra control freedom “open zero state duty cycle”. Simulation results are given to demonstrate the power loss reduction in this CSI case.

1.3. Topology synthesis literature

The increasing diversity of possible applications and the continuous demand for smaller, lighter and more efficient power converters have spurred the interest in fundamental topological properties of PWM converter and the construction of new converter topologies. Converter synthesis method is procedure to generate a converter to implement the desired functions, which is also useful for getting a better understanding of conversion principles. A number of previous works related to the problem of synthesis have been reported, most of them are related to DC-DC conversion. Several circuit manipulations have been sued for converter synthesis: cascade connections of existing converters [45]; duality transformations [46, 47], inversion of source and the load [129], differential or parallel connections of two converters [129], recognition of topological properties and constrains [122-125], canonical switching cell [126-127]. An analytical approach for generating switched-mode converters is proposed in [130], the main idea of which is to find an algebraic representation for the converter topology so that synthesis of complete classes of converters can be reduced to synthesis of all possible algebraic representations. To extract the useful topologies in this method, some general properties and conditions for dc-dc conversion are established

[131-132]. In [133] and [134], there is a reexamination about the fundamental topological assumptions on PWM converters.

This dissertation also tries to investigate the synthesis techniques for inverter topology and develop new topologies based on that. Some dc-dc conversion topology derivation technique have been reviewed and summarized first. One inverter derivation technique is summarized from the Z-source inverter topology. It has been applied on various types of basic dc-dc converter topologies and new converters with desired properties has been found.

A new family of switched-coupled-inductor inverters has been proposed in this dissertation, with voltage buck-boost function. In voltage-fed switched-coupled-inductor inverter, a boost function can be implemented by introducing an extra shoot-through state on the inverter bridge. It utilizes the same principle as the Z-source inverter, but has higher boost ratio and lower active device voltage stress at the same voltage gain. It also has wider voltage buck/boost range than conventional boost-converter inverter. In current-fed switched-coupled-inductor inverter, a buck function can be implemented by introducing an extra open zero state on the inverter bridge. The current-fed topologies are capacitor-less solution among the buck-boost inverters, which reduces the system size significantly. In addition, compared to traditional boost-converter-inverter, it has less switch count, and less active device current stress. Compared to current-fed Z-source inverter, it has higher boost ratio and lower active device current stress. The inverter can sustain minimum voltage and current stress at a certain operation point, through adjusting the trans-ratio and the shoot through/open circuit duty cycle. The simulation results are given to verify the theory analysis and demonstrate the great merits of the switched-coupled-inductor inverter. It is beneficial to

be applied in dc-ac applications that demand a high voltage gain from a very low voltage dc source, such as the micro-inverter in photovoltaic, or G/M in HEV

1.4. Problems of traditional direct matrix converter

The matrix converter (MC) is a direct ac/ac converter with sinusoidal input/output waveforms and controllable input power factor [49-51]. It has less passive component compared to the existing back-to-back converter. Its control methods, circuit operation and possible applications have been investigated in paper [52-70]. It has a good perspective especially when the reverse-blocking IGBT is available now.

In a traditional matrix converter, the three switches on the same output phase leg can not be gated on at the same time because doing so would cause a short circuit(shoot through) to occur, which would destroy the converter. In addition, the maximum voltage gain can not exceed 0.866. These limitations can be overcome by Z-source matrix converter [1], which adds an ac impedance network (Z-network) in the input. The Z-source matrix converter advantageously utilizes the shoot through states to boost the ac voltage by gaiting on three switches on the same output phase leg, to boost the voltage to be greater than the input voltage. In addition, the reliability of the converter is greatly improved because the shoot through states can no longer destroy the circuit. The commutation steps can be simplified. Therefore, it provides a low-cost, reliable, and efficient structure for buck and boost ac/ac conversion.

1.5. Scope of the thesis

This dissertation focuses on the following subjects:

Chapter 2 explores the topology synthesis process for voltage/current-fed Z/quasi-Z/trans-Z

source inverter, direct Z-source matrix converter family, and proposes a new family of topology “switched-coupled-inductor inverter”, to provide a high boost ratio and compact solution for HEV/EV motor drive.

Chapter 3 presents a comprehensive circuit analysis of five topologies: current-fed quasi-Z-source inverter, current-fed Z-source rectifier, switched-coupled-inductor inverter and Direct Z-source matrix converter. It includes the equivalent circuit states, voltage and current gain, operation regions, calculation of ac output voltage and current, passive component stress and active switch device power rating.

Chapter 4 presents two modulation methods for current source inverter both in SVPWM point of view: DPWM and CSVPWM, and proposes the third method PWAM, all of which is based on different selection and placement of zero vectors. The different switching sequences are proposed and compared in terms of spectrum, THD and switching loss.

Chapter 5 proposes the zero vector placement technique in SVPWM control of Z-source inverter, in order to achieve lower harmonics, lower switching loss, lower voltage spike and lower current ripple and also demonstrates it through a 24 kW current-fed quasi-Z-source inverter prototype experiments.

Chapter 6 analyzes the switching loss reduction function and harmonic performance of SVPWAM method which has been proposed in chapter 4 for both VSI and CSI, through the

case studies. A 1kW boost-converter-inverter prototype has been built to experimentally demonstrate the stated advantages of the method.

Chapter 7 proposes three shoot through control methods and the hybrid minimum stress control method for direct Z-source matrix converter family and demonstrates them through experiments.

Chapter 8 presents the two new found discontinuous operation modes for current-fed quasi-Z-source inverter when the power factor is low or capacitance is small, and analyzes the capacitor voltage waveform and the critical conditions for this circuit at different modulation methods.

Chapter 9 proposes the large signal and small-signal circuit model for current-fed quasi-Z-source inverter, current-fed Z-source rectifier and switched-coupled-inductor inverter. The transient performance of the first topology has been investigated and demonstrated through experiments.

Chapter 10 discusses the major contributions of this dissertation and the future work recommendations.

CHAPTER 2 CURRENT SOURCE INVERTER TOPOLOGIES

2.1. Introduction

The increasing diversity of possible applications and the continuous demand for smaller, ligher and more efficient power converters have spurred the interest in fundamental topological properties of PWM converter and the construction of new converter topologies. Converter synthesis method is procedure to generate a converter to implement the desired functions, which is also useful for getting a better understanding of conversion principles. A number of previous works related to the problem of synthesis have been reported, most of them are related to DC-DC conversion. Several circuit manipulations have been sued for converter synthesis: cascade connections of existing converters [45]; duality transformations [46-47], inversion of source and the load [129], differential or parallel connections of two converters [129], recognition of topological properties and constrains [122-125], canonical switching cell [126-127]. An analytical approach for generating switched-mode converters is proposed in [130], the main idea of which is to find an algebraic representation for the converter topology so that synthesis of complete classes of converters can be reduced to synthesis of all possible algebraic representations. To extract the useful topologies in this method, some general properties and conditions for dc-dc conversion are established [131-132]. In [133] and [134], there is a reexamination about the fundamental topological assumptions on PWM converters.

The purpose of this chapter is to investigate the synthesis techniques for inverter topology and develop new topologies based on that. Some dc-dc conversion topology derivation technique have been reviewed and summarized first. One inverter derivation

technique is summarized from the Z-source inverter topology. It has been applied on various types of basic dc-dc converter topologies and new converters with desired properties has been found. Most importantly, a new family of switched-coupled-inductor-inverter topology has been proposed to implement high boost ratio single stage buck-boost function. It has less switching count, smaller passive size and less device stress than the other topologies with the same function.

2.2. Topology synthesis techniques

2.2.1. Graph theory

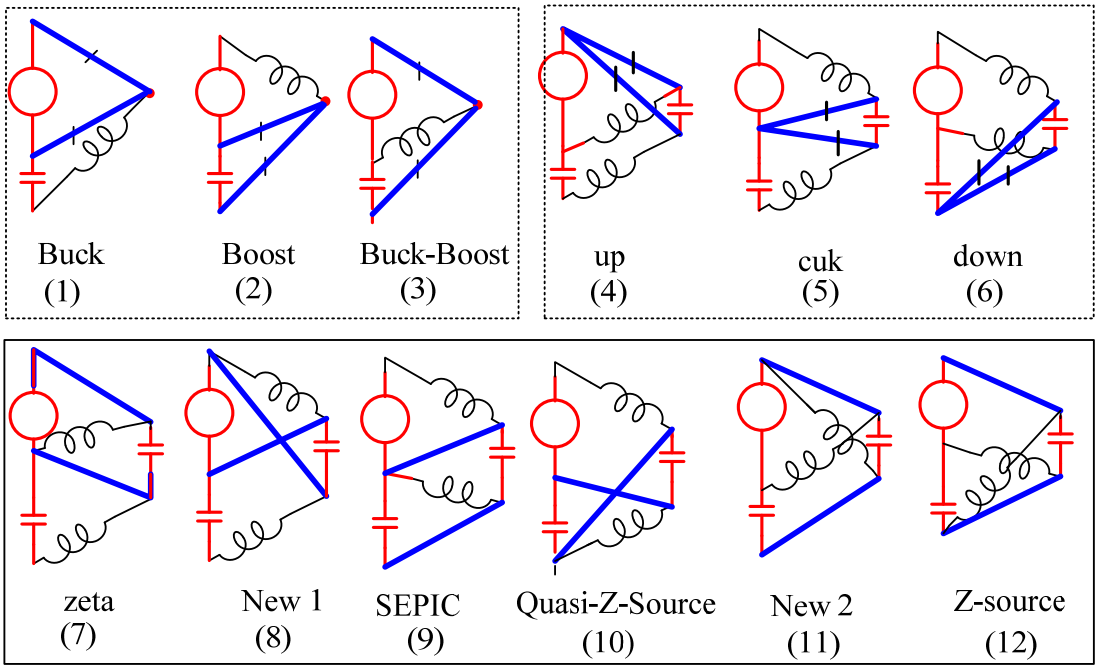


Figure 2.1 Twelve basic dc-dc converter topology from graph theory

In 1970s, based on the switching mode converter concept proposed by professor Middlebrook, various kinds of methods are proposed for topology derivation. The Caltech group proposed the mathematic method to derive topology based on connection matrix and the basic rules for the circuit existence [131]. They even developed the computer program to exhausting all the possible two state or three states converter topologies. A Poland professor

proposed how to derive the basic dc-dc converter from graph theory [122]. Figure 2.1 is a review for the twelve basic topology derived from the graph theory. They are classified into three categories. In the first group, the two trees are voltage source-capacitor branch and a dot; three circuits are formed by connecting the dot to two different nodes in the first tree, in which the connections means the switch. In second group, another branch is a two node capacitor; three circuits are formed by connecting the two nodes to a single node in the first tree. In third group, the branches are the same as the second group; but the two nodes are connecting to two different nodes in the first tree, to form six circuits. It is found that the Z-source and quasi-Z-source dc-dc converter appear in the last group.

2.2.2. Duality

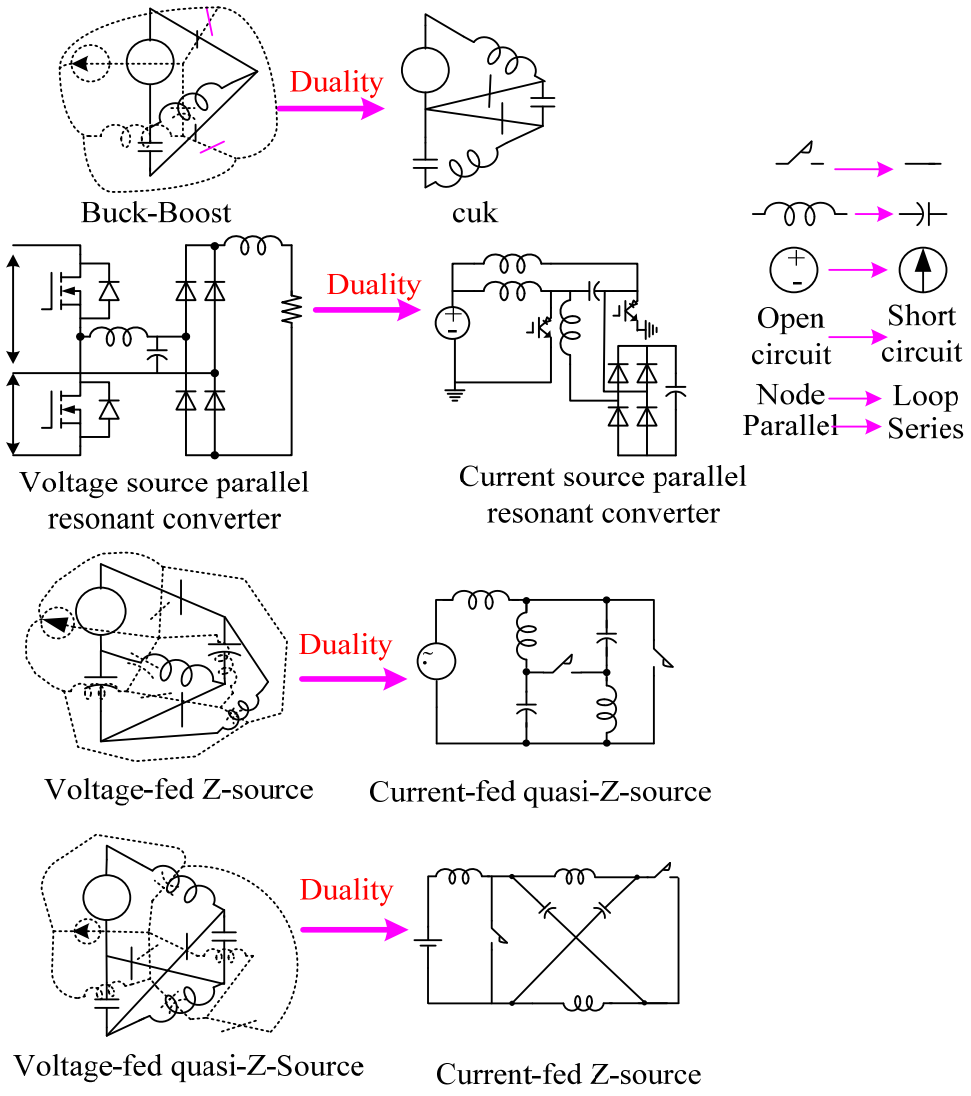


Figure 2.2.Current source dc/dc converter from duality of voltage source converter

In electrical circuits, electrical terms are associated into pairs called duals. A dual of a relationship is formed by interchanging voltage and current in an expression. The following is the list of electrical dualities: voltage and current; parallel and serial; resistance and conductance; impedance and admittance; capacitance and inductance; reactance and susceptance; short circuit and open circuit; Kirchhoff's current law and Kirchhoff's voltage law; Thevenin's theorem and Norton's theorem.

Figure 2.2 listed some classical duality examples and also proposed the new duality circuits. As well known, Cuk converter is the dual of buck-boost converter. The voltage

source parallel resonant converter and current source one are dual. It is found that the recently proposed Z-source converter family also has dual circuit.

The voltage-fed Z-source converter is dual of current-fed quasi-Z-source converter; the voltage-fed quasi-Z-source converter is dual of current-fed Z-source converter. This also means the derivation of previously proposed quasi-Z-source topology can start from applying duality on Z-source topology. As shown in Figure 2.1 the dotted line, the duality principle is like this: mesh is transformed into node; inductor changes to capacitor; capacitor changes to inductor; resistance becomes admittance; voltage source becomes current source, and the direction obeys right hand discipline. For the switch, it is special. Actually for duality circuit derivation, each switching state equivalent circuit needs to be transformed. For example, the two state dc-dc converter in Figure 2.1 left hand side. The duality needs to be applied to each state. Thus the switch is either on or off in each state. To transform to dual circuit, the switch on state needs to be changed to off; and off state needs to be changed to on. Thus the dual circuit for each state could be obtained. Finally, they are combined into one switching circuit.

2.2.3. Bilateral inversion transformation

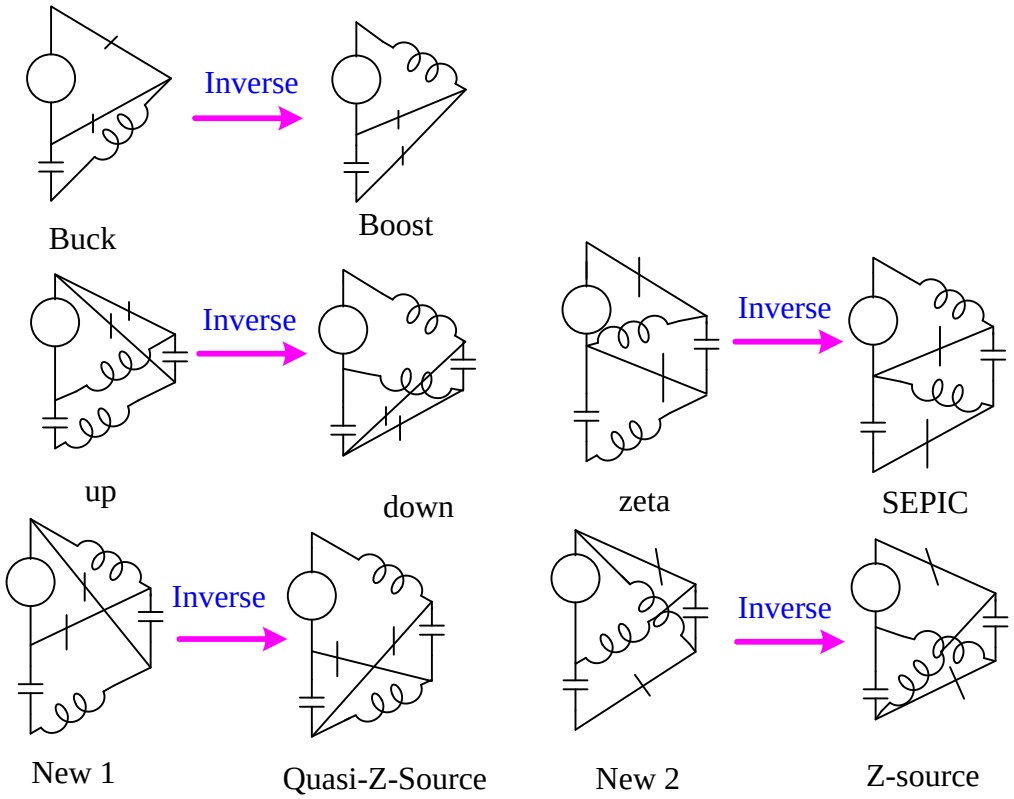
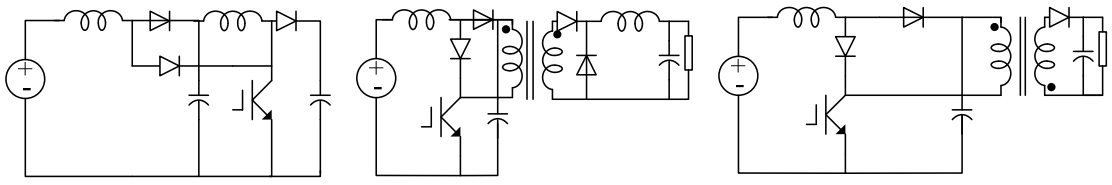


Figure 2.3. DC/DC converter derivation from inverse transformation

By inversing the input and output, a new group of dc/dc converter topologies can be derived from the existing 12 structures in Figure 2.1, as shown in Figure 2.3. The resulting voltage gain is equal to the inverse of the gain of the original circuit on the left. The original circuit which conducted quasi-Z-source and Z-source dc/dc converter is also featured as a buck-boost converter, with the voltage gain equal to $\frac{1-2D}{1-D}$.

2.2.4. Cascade



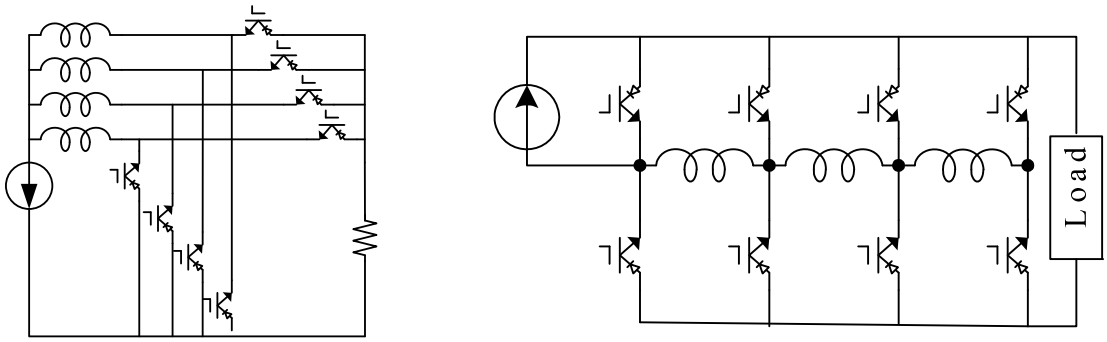
(a) Boost + Boost (b) Boost + Forward (c) Boost + Flyback

Figure 2.4. Topologies generated by cascading basic circuit

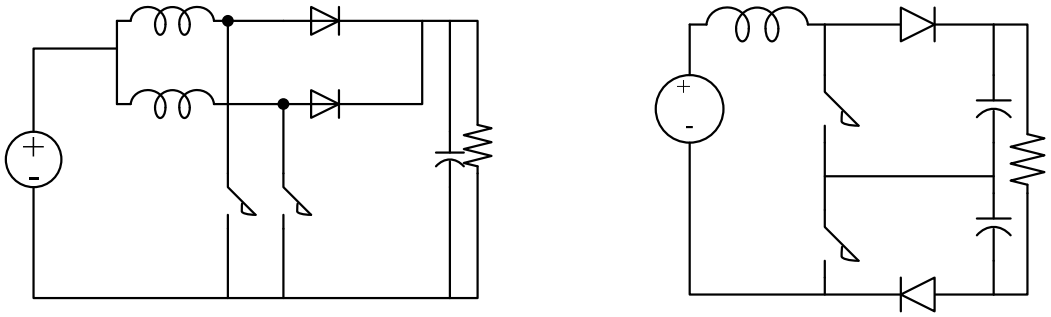
If the number of switches is allowed to exceed two, more combinations of circuits can

bring the advanced features. Like the ones shown in Figure 2.4, the cascade connection of the circuits increase the circuit boost ratio, and also add some new features such as isolation to the circuit. A good design makes them all only utilize one active switch.

2.2.5. Parallel



(a) Multi-level current source inverter/converter (b) Multi-level CSI

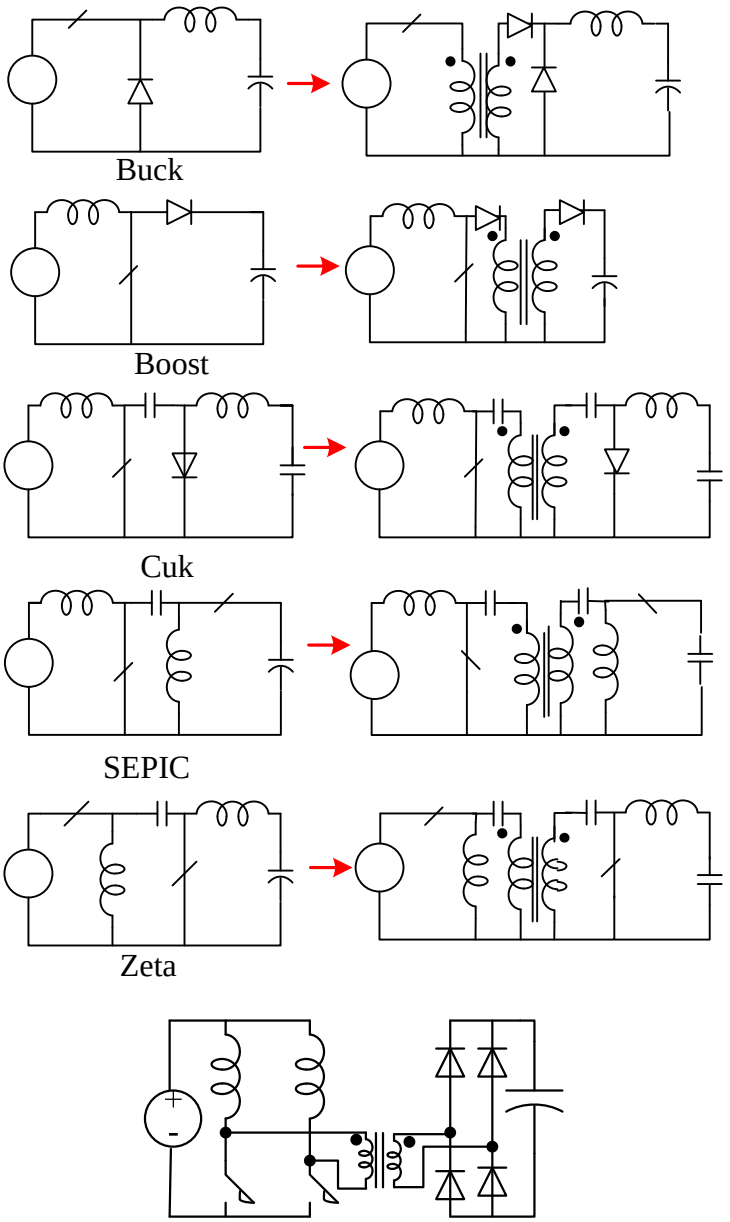


(c) Interleaved boost converter (d) Two level boost converter

Figure 2.4. Topologies generated by paralleling basic circuit

Another technique is paralleling circuit, in order to reduce the current stress, or form a interleaved circuit, or reduce the current ripple. Figure 2.4 lists some examples of the parallel connection. The multilevel voltage or current source converter/inverter is utilizing this parallel technique, as well as the interleaved converter.

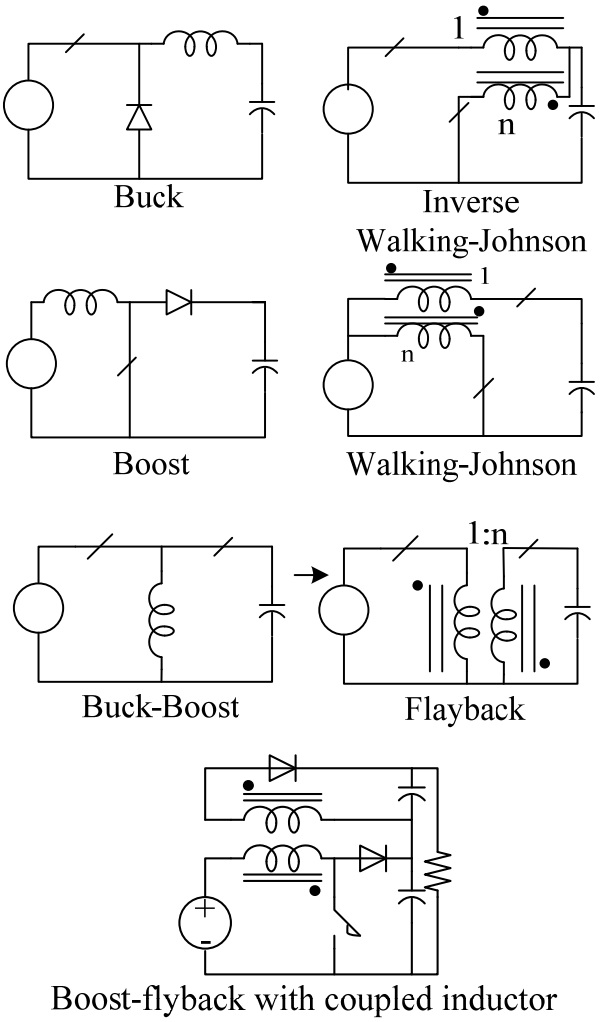
2.2.6. With transformers



(a) Isolated version of basic dc-dc converter

Figure 2.5 Topologies derived from adding isolation transformer between input and output

Figure 2.5 (cont'd)



(b) Coupled-inductor isolated basic dc-dc converter

In some applications, the isolation between input and output is required, such as PV inverter. The isolated transformer can be used here to implement this goal. The place to add this transformer is the node that has zero voltage. Thus the transformer will not change the basic operation states of the circuit. There are two methods to apply the isolation: one is by transformer like Figure 2.5 (a) shows; the transformer is inserted between two capacitors, which are the split single capacitor in the original circuit; another is by coupled inductor like Figure 2.5 (b) shows; a single inductor is changed to coupled inductor with opposite coupling;

the energy will transform from one inductor to another one completely depending on the switching state. The new finding here is that: the so called “Walking-Johnson” circuit is derived from boost converter; the so called “Inverse Walking-Johnson” circuit is derived from buck converter; the flyback circuit is derived from buck-boost converter. The feature of this inductor that can be transformed is one of its terminals is connected to two complementary switch.

2.2.7. Extension of canonical switching cell

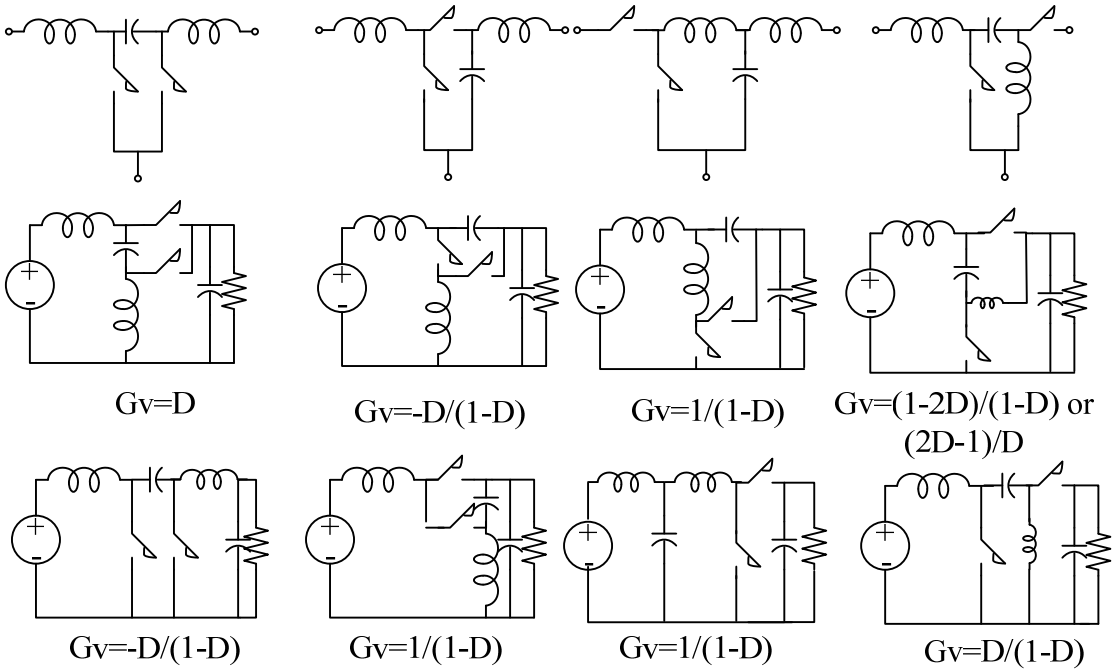


Figure 2.6. Topologies derived from adding isolation transformer between input and output

Another important technique to extend the converter topology is “switching cell”. If the number and kinds of passive components, and the number of switches are fixed, several different structures of switching cells can be constructed. Except for those that does not obey the basic circuit rule, each switching cell can be used for constructing several topologies, depending on the way to connect the source and load to it. Figure 2.6 lists some examples of the topologies deriving from the switching cells. They are referred to paper []. All those

mentioned topologies derived from duality, inversion and graph theory can all be derived by playing the switching cell.

2.3. Derivation of buck-boost Z-source inverters

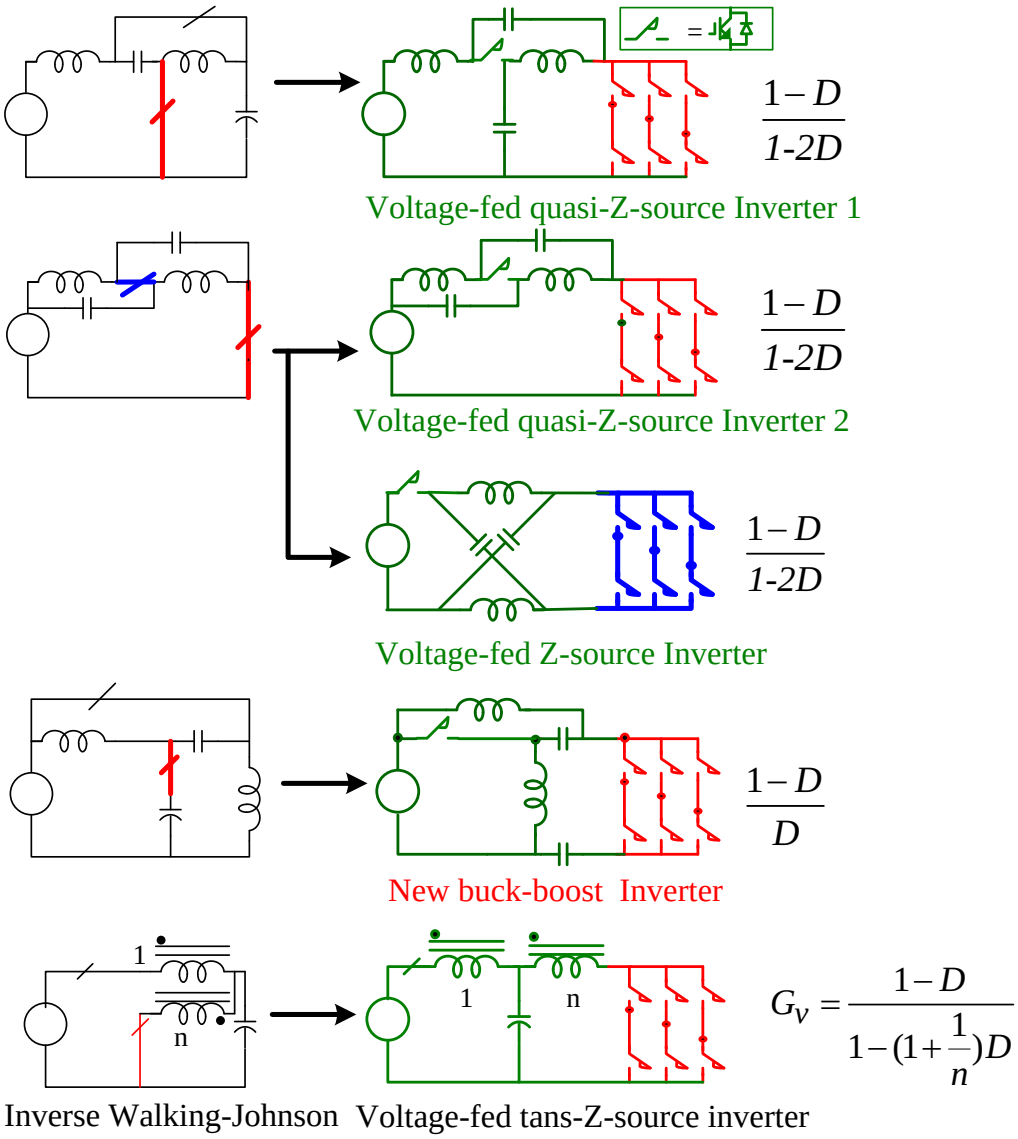


Figure 2.7. Voltage-fed Z-source inverter topologies derived from basic dc-dc converter (D is the shoot through duty cycle, *Gv* is the voltage gain between output equivalent voltage and input)

The voltage-fed Z-source inverter can all be derived from the converter, as Figure 2.7 shows. The left hand side of this figure shows the circuit (10),(12)， inverse-walking-Johnson

and (8) from the basic circuits in Figure 2.1. From dc-dc converter to inverter transformation, one special technique is used here: replacing one switch by inverter bridge. Thus the on state of this switch is corresponding the shoot through of the inverter bridge, the off stat of this switch is corresponding to the active and open zero state of the switch. For each dc-dc circuit, there are two ways of doing this replacement since they have two active switches. But some of new inverters do not have the voltage buck-boost function. As shown in Figure 2.7, the voltage-fed quasi-Z-source inverter is derived by replacing the lower switch of the left circuit by the voltage source inverter bridge. Similarly, another voltage-fed quasi-Z-source inverter topology and the voltage-fed Z-source inverter topology are obtained by replacing different switches in the left dc-dc converter respectively. These three Z-source topologies, their voltage gains are all $(1-D)/(1-2D)$, which is a buck-boost function with the variation of D. The fourth inverter is the recently proposed voltage-fed tans-Z-source inverter[], which has extended voltage gain range than traditional Z-source inverter because of the trans-ratio. It can be derived by replacing one of the active switches in the inverse-Walking-Johnson circuit by an voltage source inverter bridge. This circuit works similarly to Z-source inverter, but with higher boost ratio. The energy transfers from one winding to another winding in the coupled inductor at different switching states. The fifth inverter is a new found circuit here, which is also a buck-boost inverter with gain $(1-D)/D$, from the transformation of the left side dc-dc circuit, which is also one of the basic 12 circuits. In summary, from this derivation principle, it can be seen that the inverter bridge has an extra shoot through state, in which all the switches are turned on. The more this shoot through state is applied, the more the voltage can be boosted.

The feature of this group is that all the circuits are the single-stage buck-boost inverter with only one diode in front. The advantages are: (1)voltage buck-boost function (2) shoot-through can be tolerated (3) less active switch (4) coupled-inductor can be utilized to reduce the size. The disadvantages include: (1) high current stress on the bridge switch (2) increased number of passive components.

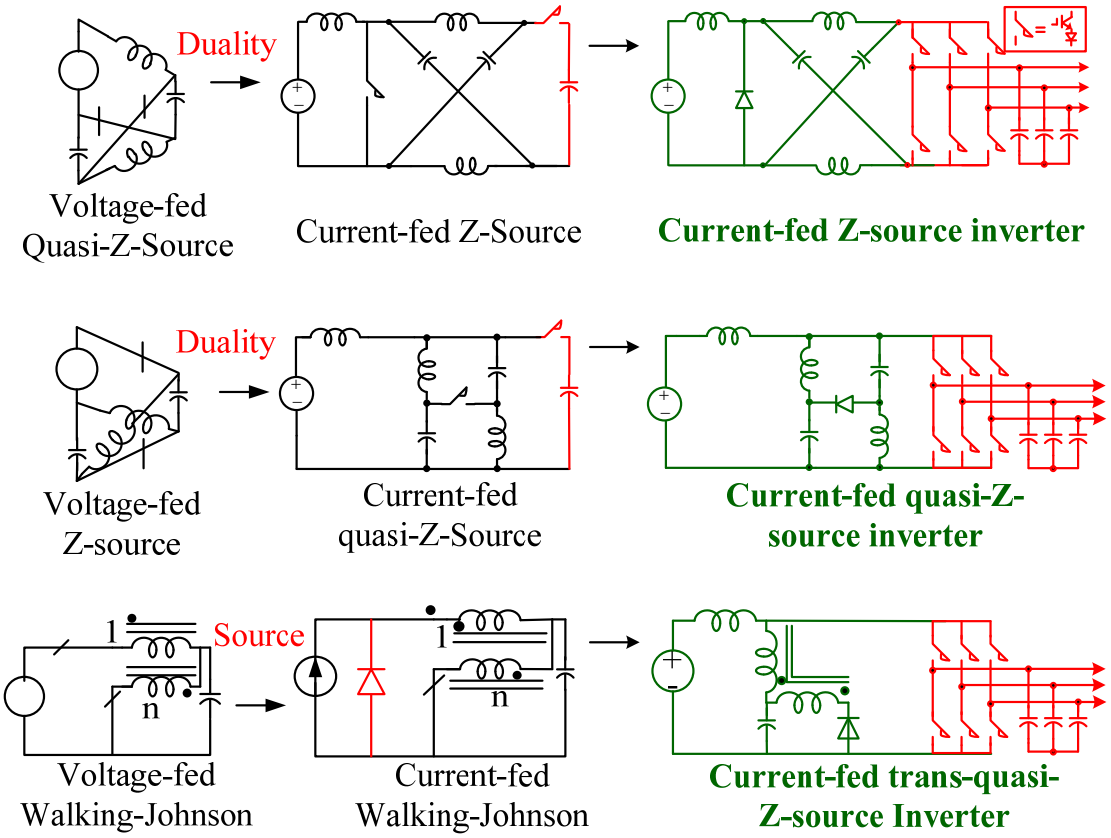


Figure 2.8. Current-fed Z-source inverter topologies derived from basic dc-dc converter

(CF=current-fed; ZSI=Z-source inverter QZSI=quasi-Z-source inverter)

Table 2-1.Voltage gain of current-fed Z-source inverter topologies in Figure 2.8

Circuit	CF-ZSI	CF-QZSI	CF-QZSI2	CF-trans-ZSI
Voltage gain	$\frac{1-2D_{op}}{D_A}$	$\frac{1-2D_{op}}{D_A}$	$\frac{1-2D_{op}}{D_A}$	$\frac{1-(1+n)D_{op}}{D_A}$

The current-fed Z-source/quasi-Z-source/trans-Z-source inverter also can all derived

from the basic dc-dc converters, as shown in Figure 2.8. For current source inverter bridge, the corresponding unit in dc-dc converter is a series combination of one active switch and one capacitor, because the switch is equivalent to inverter bridge, and the capacitor is equivalent to output capacitor. The first dc-dc circuit generates current-fed Z-source inverter; the second dc-dc generates two current-fed quasi-Z-source inverters; the last group the current-fed walking-johnson dc-dc converter is first derived from the voltage-fed one, and then by using the same technique, the current-fed trans-Z-source inverter is derived. Therefore, the off state of the corresponding switch in dc-dc converter is transferred into the extra open zero state of current source inverter, which is not allowed in the traditional current-source inverter. This extra state brings the buck function to CSI, just as the voltage gain shown in the Table 2-1. D_A represents active duty cycle, which is proportional to modulation index. And D_{op} represents extra open zero state duty cycle.

The feature of this group is that all the circuits are the single-stage buck-boost current source inverter with only one diode in front. The advantages are: (1)voltage buck-boost function (2) regeneration with only a diode (3) open-circuit can be tolerated (4) less active switch (5) both output voltage and current are sinusoidal (6) coupled-inductor can be utilized to reduce the size. The disadvantage is high voltage stress on the bridge switch.

2.4. Newly derived inverter topologies with buck-boost function

From other basic or extended dc-dc converters, by applying the same technique, some new topologies are derived here, as shown in Figure 2.9. Inverter (a) and (b) are similar, both of which have the mixed voltage/current source. The disadvantage of these two inverters is high voltage and current stress on the front active switch. Inverter (c) and (d) is buck-boost

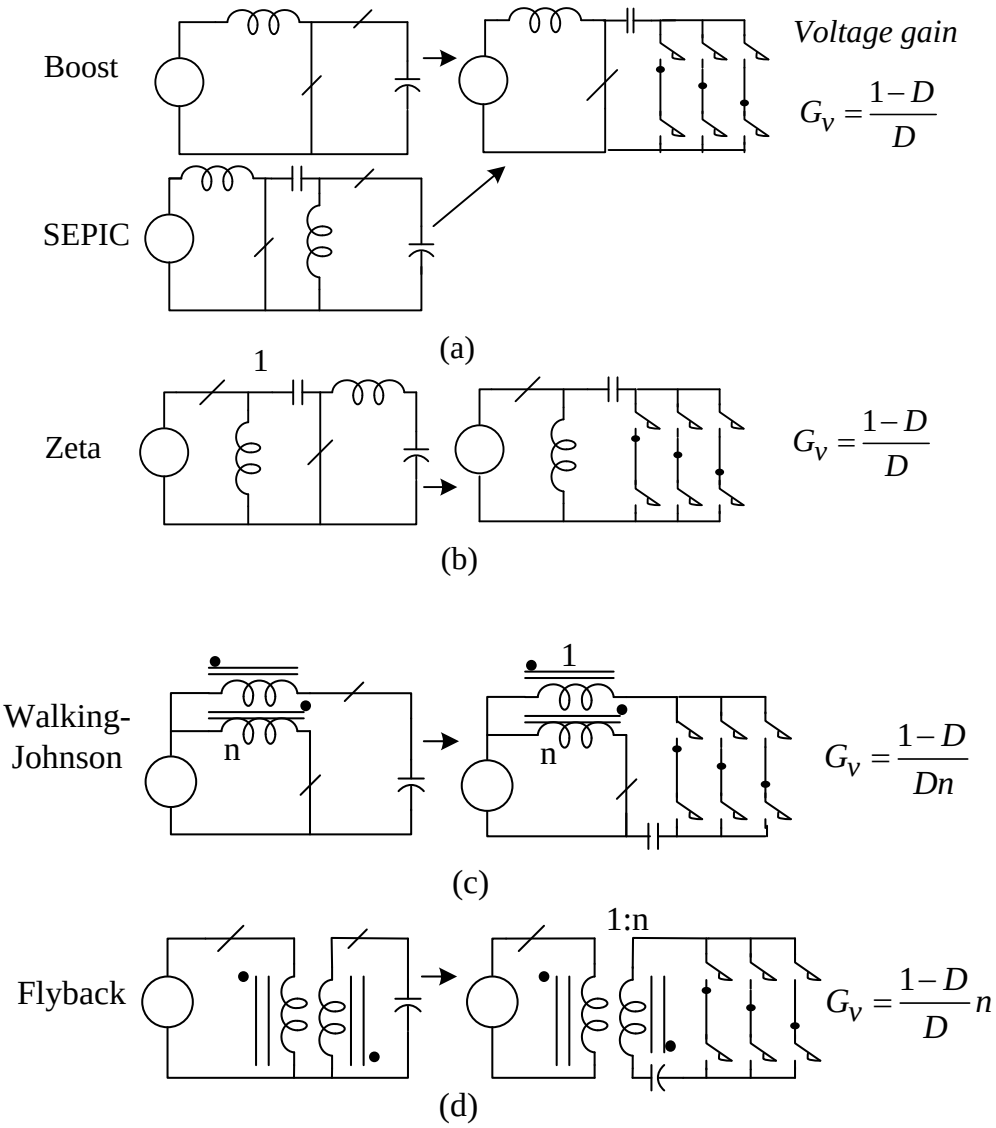


Figure 2.9. New inverter topologies with buck-boost functions derived from basic dc-dc converter (D is the shoot through duty cycle, *Gv* is the voltage gain between output equivalent voltage and input)

inverter with trans-ratio n. The coupled inductor implements two functions: isolation and voltage regulation. From the voltage gain equation, it can be found that it has one more control freedom, the trans-ratio n. Thus wider voltage buck/boost range can be achieved. Also for a certain voltage gain equation, the duty cycle D and trans-ratio n can be tuned at the same time to minimize the voltage and current stress on either active device or passive.

2.5. Proposed switched-coupled-inductor inverter family with buck/boost function

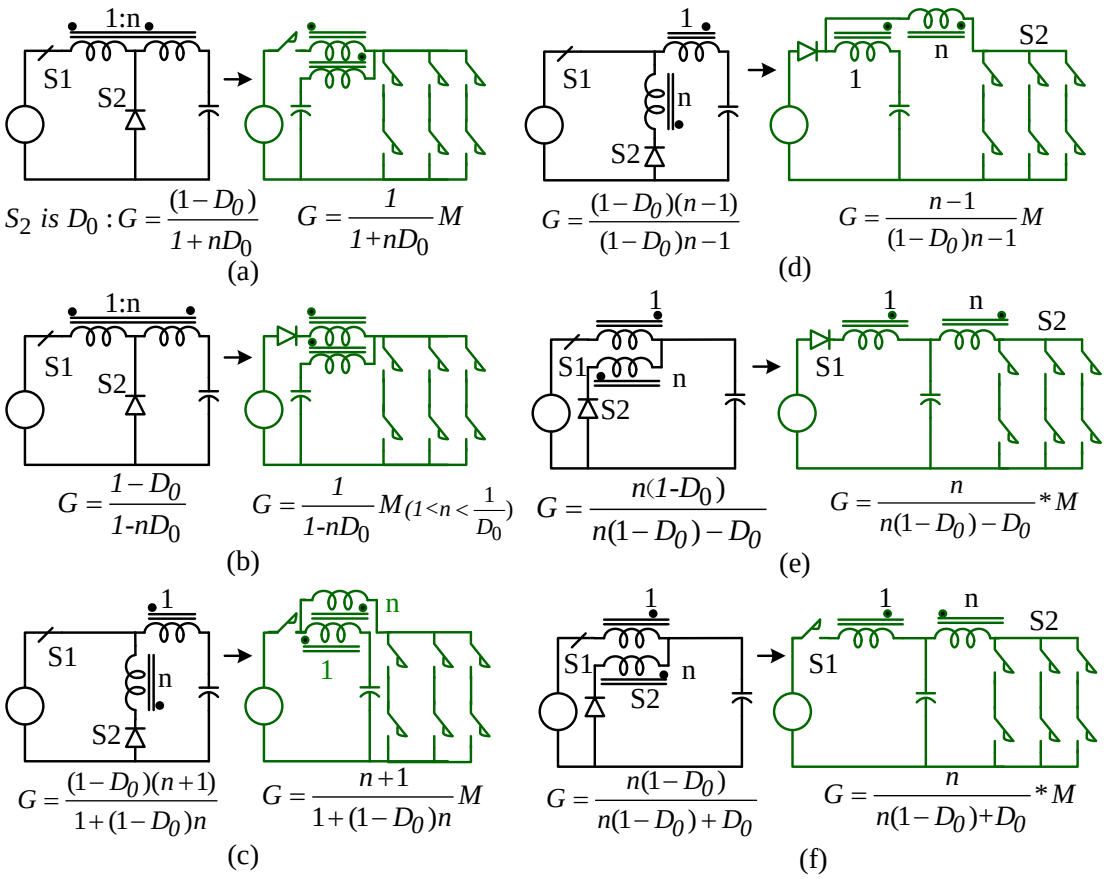
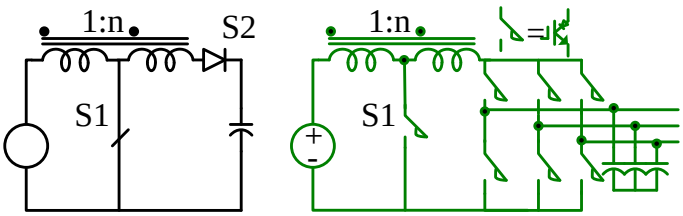


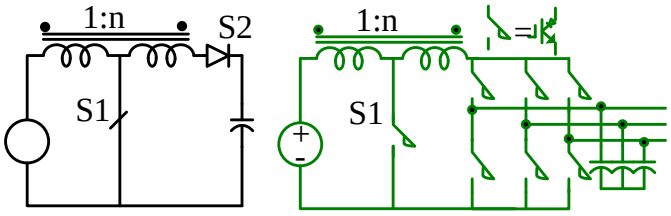
Figure 2.10. Voltage-fed switched-coupled-inductor inverter topologies

A new family of switched-coupled-inductor inverters has been proposed here, with voltage buck-boost function. In voltage-fed switched-coupled-inductor inverter, a boost function can be implemented by introducing an extra shoot-through state on the inverter bridge. It utilizes the same principle as the Z-source inverter, but has higher boost ratio and lower active device voltage stress at the same voltage gain. It also has wider voltage buck/boost range than conventional boost-converter inverter. In current-fed switched-coupled-inductor inverter, a buck function can be implemented by introducing an extra open zero state on the inverter bridge. The current-fed topologies are capacitor-less solution among the buck-boost inverters, which reduces the system size significantly. In



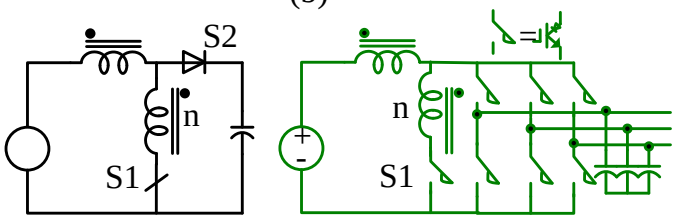
S1 is D0: $G = \frac{1+nD_0}{1-D_0}$ $G = \frac{1+nD_0}{1-D_0}$

(a) (D0 is open state)



S1 is D0: $G = \frac{1-nD_0}{1-D_0}$ $G = \frac{1\text{-}nD_0}{1-D_0}$

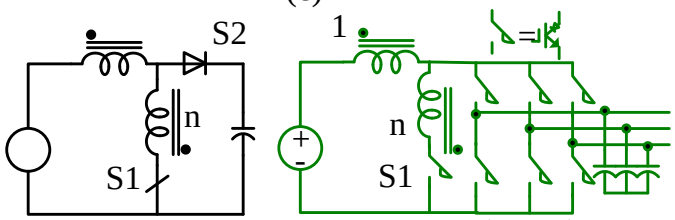
(b)



S1 is D0:

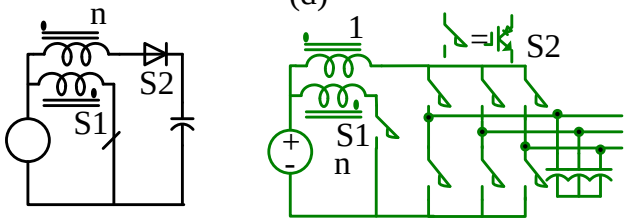
$G = \frac{n(1-D_0)+1}{(n+1)(1-D_0)}$ $G = \frac{n(1-D_0)+1}{(n+1)(1-D_0)}$

(c)



S1 is D0: $G = \frac{1\text{-}n(1-D_0)}{(1\text{-}n)(1-D_0)}$ $G = \frac{1\text{-}n(1-D_0)}{(1\text{-}n)(1-D_0)}$

(d)

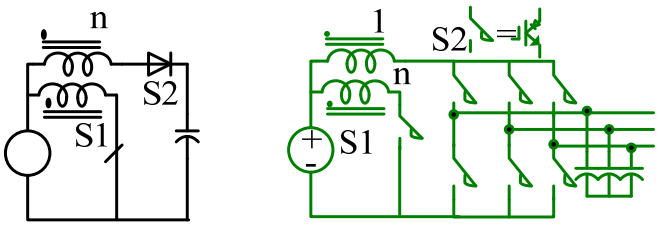


S1 is D0: $G = \frac{(1-D_0)n-D_0}{n(1-D_0)}$ $G = \frac{(1-D_0)n-D_0}{n(1-D_0)}$

(e)

Figure 2.11. Current-fed switched-coupled-inductor inverter topologies

Figure 2.11 (cont'd)



S1 is D0:

$$G = \frac{(1-D_0)n+D_0}{n(1-D_0)} \qquad G = \frac{(1-D_0)n+D_0}{n(1-D_0)}$$

(f)

addition, compared to traditional boost-converter-inverter, it has less switch count, and less active device current stress. Compared to current-fed Z-source inverter, it has higher boost ratio and lower active device current stress. The inverter can sustain minimum voltage and current stress at a certain operation point, through adjusting the trans-ratio and the shoot through/open circuit duty cycle. The simulation results are given to verify the theory analysis and demonstrate the great merits of the switched-coupled-inductor inverter. It is beneficial to be applied in dc-ac applications that demand a high voltage gain from a very low voltage dc source, such as the micro-inverter in photovoltaic, or G/M in HEV

The simplest method of extending the duty cycle range of classical dc–dc converters consists of connecting the tapped point of the single inductor to other components such as main switching device, freewheeling diode, input or output rails giving rise to the well-known tapped-inductor converter circuits [1]. One of the buck converter derived version is named as Watkins-Johnson converter [2, 3].

By using tapped-inductor converters, the weight, size, complexity, and cost associated are reduced when compared with other duty cycle extension methods (such as cascading several basic dc–dc converters and the use of multi-winding transformers). Using tapped

inductor, it forms an additional control parameter, the trans-ratio of the tapped inductor. So the high step down or step up function can be implemented [4,5] Since the tapped inductor is similar to the auto transformer, the energy is stored in the inductor when the transistor is turned on and released to the output when it is turned off. Different connection ways of the tapping point to the outside components generate different topologies, thus brings different voltage and current stress on active device and passive components [6]. The best topology can be chosen at a given voltage gain requirement.

The tapped inductor can also assist soft-switching of the active switch in dc-dc converter [7, 8]. It can also be utilized as the output filter [9, 10] to form a soft-switching loop for full bridge converter [9, 10].

A novel switched-coupled-inductor inverter is proposed here, inspired by the principle of the tapped inductor converter. It utilizes an extra shoot through state in VSI and open zero state in CSI to implement voltage buck-boost function. It has been demonstrated through theory and simulations that the proposed switched-coupled-inductor inverter has much wider range for voltage buck/boost, and lower voltage/current stress than other extended buck-boost inverter, including boost converter inverter and Z-source inverter. Both of the voltage-fed and current-fed topologies have fewer active switch than other extended topologies. Current-fed topologies are a capacitor-less solution, which greatly reduces the system size.

In a word, the proposed family of topologies provides a high boost, low cost and compact solution for a buck-boost inverter. It is suitable to use in photovoltaic micro-inverter and electrical vehicle motor drive.

The concept of tapped-inductor structure is to utilize the trans-ratio variation to extend

the duty cycle range of the conventional dc-dc converter. It permits a different mix of voltage and current ratings for the various elements of the circuit, and particular for the switch and diode. This idea can be transformed into inverter to get the similar benefits. The voltage-fed(VF)/current-fed(CF) switched-coupled-inductor inverter (SCII) topologies are shown in Figure 2.10 and Figure 2.11.

The front switch can be either a diode or an active switch, depending on the polarity of its flowing current and blocking voltage. It is found from calculations that: in voltage-fed topologies, circuit 2, 4, and 6 could use a diode for front switch, as long as they meet certain design parameter conditions; in current-fed topologies, all the circuits have to use an active switch in front. This active switch is a single device without any anti-parallel or series diode. Compared to boost-converter-inverter system, it has less active switch.

In summary for voltage-fed switched-coupled-inductor inverter, it is featured as a single-stage buck-boost voltage source inverter with coupled-inductor. Its advantages contain: (1) high boost ratio (2) tolerating shoot-through (3) reduced size. Its disadvantages include: (1) high voltage stress on the device when boost ratio is high (2) clamp circuit is needed because of the leakage inductance of coupled inductor (3) discontinuous input current. However, the first disadvantage can be overcomed because different topologies can be selected at different voltage gain requirement to achieve minimum voltage/current stress on devices or passives.

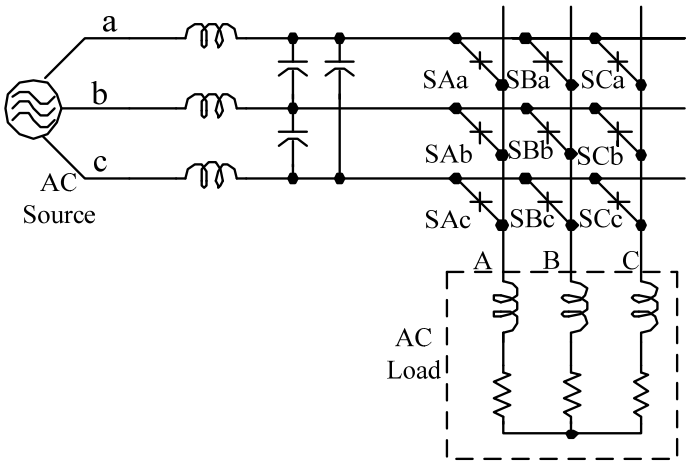
In summary for current-fed switched-coupled-inductor inverter, it is featured as a single-stage buck-boost current source inverter with coupled-inductor. Its advantages contain: (1) no dc capacitor (2) two inductor are coupled together on the same core to achieve size reduction (3) high voltage boost ratio; Its disadvantages include: (1) device must sustain high

current stress when boost high (2) the front switch has to be active device (3) clamp circuit is needed because of the leakage inductance of the coupled inductor (4) input current is discontinuous. However, the first disadvantage can be overcomed because different topologies can be selected at different voltage or current gain requirement to achieve minimum voltage/current stress on devices or passives.

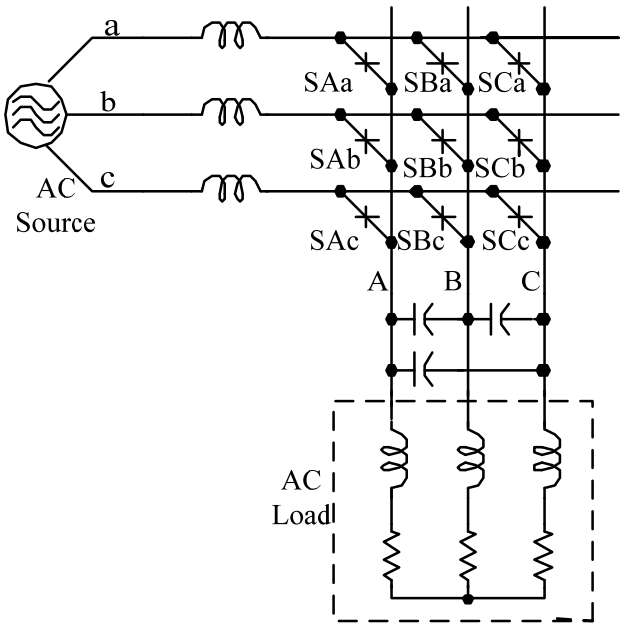
2.6. Direct Z-source matrix converter topology

The matrix converter (MC) is a direct ac/ac converter with sinusoidal input/output waveforms and controllable input power factor [2-4]. It has less passive component compared to the existing back-to-back converter. Its control methods, circuit operation and possible applications have been investigated in paper [5-24]. It has a good perspective especially when the reverse-blocking IGBT is available now.

The Z-source matrix converter advantageously utilizes the shoot through states to boost the ac voltage by gaiting on all the three switches on the same output phase leg. Therefore, the Z-source matrix converter can boost the voltage to be greater than the input voltage. In addition, the reliability of the converter is greatly improved because the shoot through states can no longer destroy the circuit. Also the current commutation steps can be simplified. Therefore, it provides a low-cost, reliable, and highly efficient structure for buck and boost ac/ac conversion.



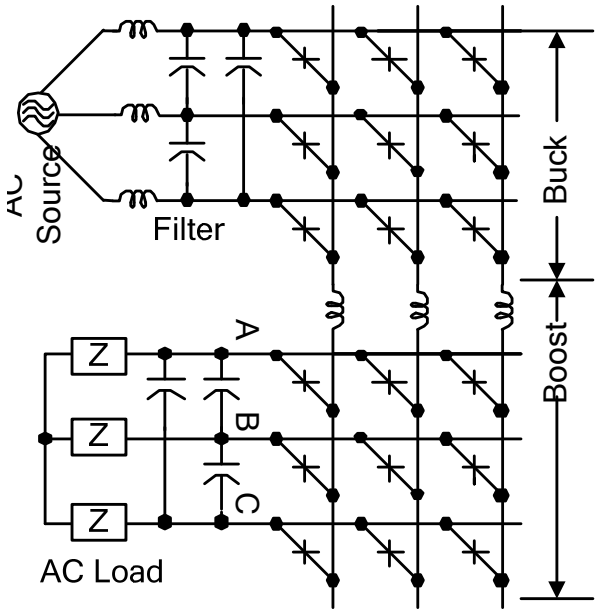
(a) Voltage-source matrix converter.



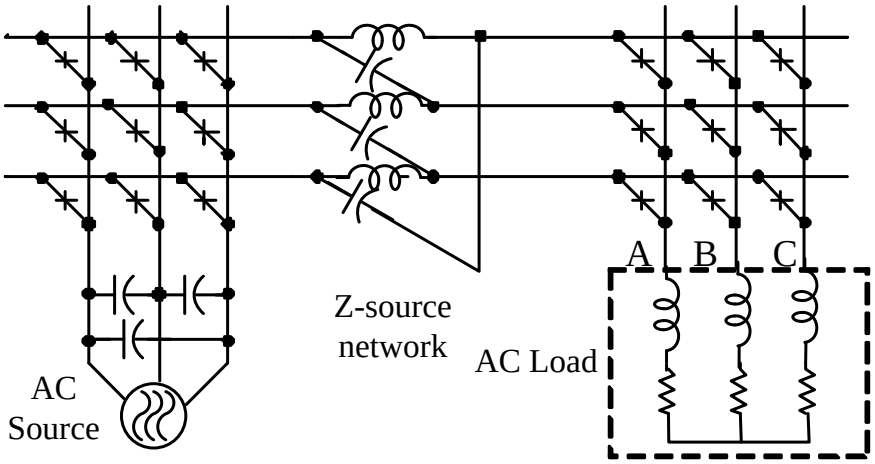
(c) Current-source matrix converter

Figure 2.12. Topologies of (a-c) traditional MC (d-l) direct Z-source MC family

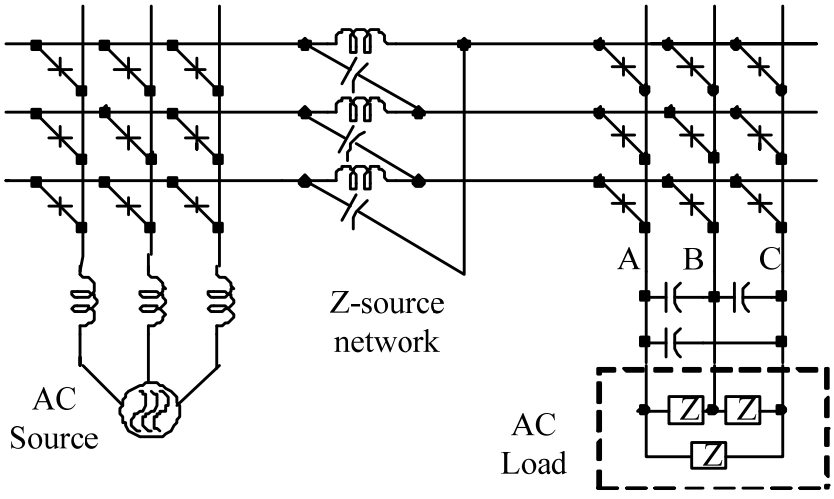
Figure 2.12 (cont'd)



(c) Buck-boost matrix converter using the traditional configurations

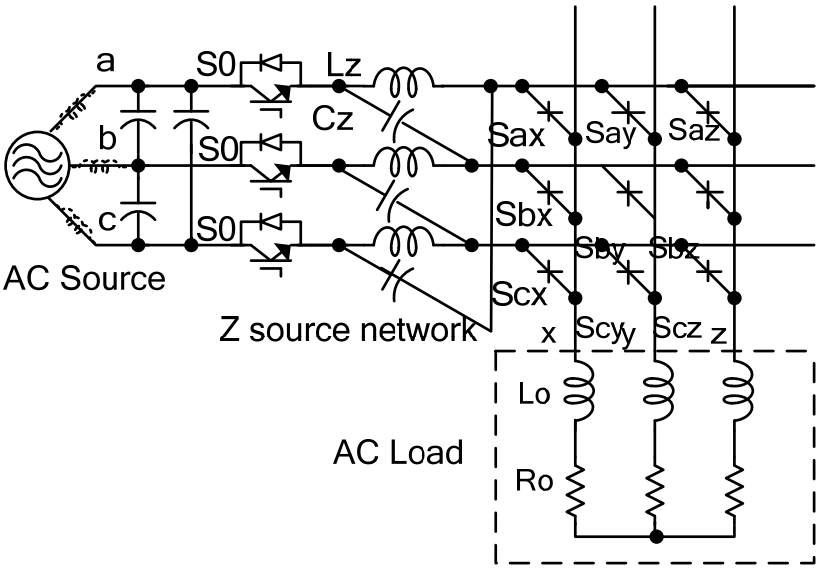


(d) Voltage-fed ZS matrix converter

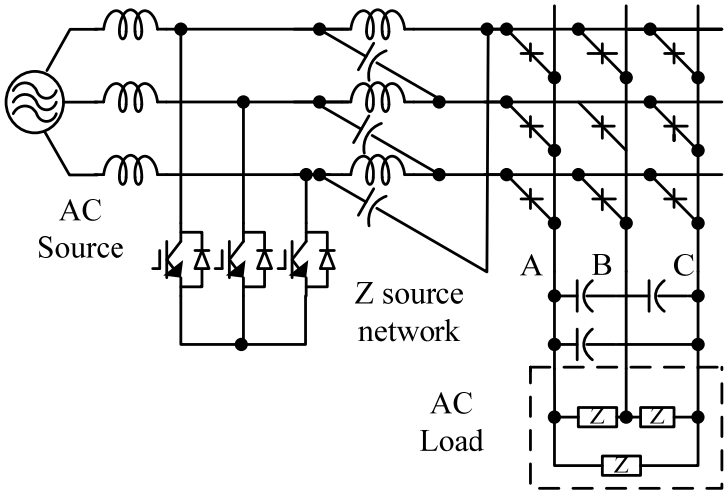


(e) Current-fed ZS matrix converter

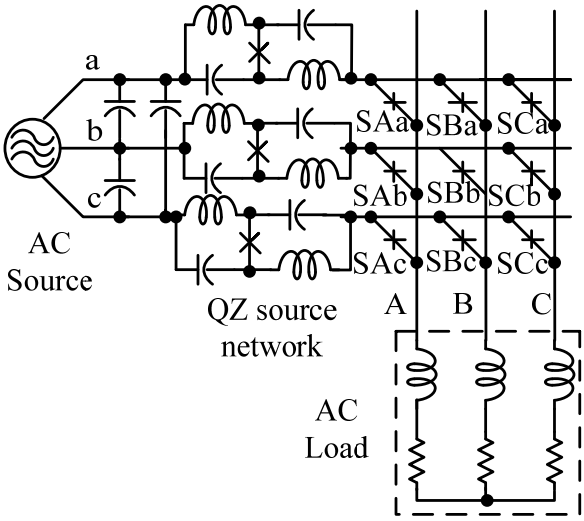
Figure 2.12 (cont'd)



(f) voltage-fed Z-source MC

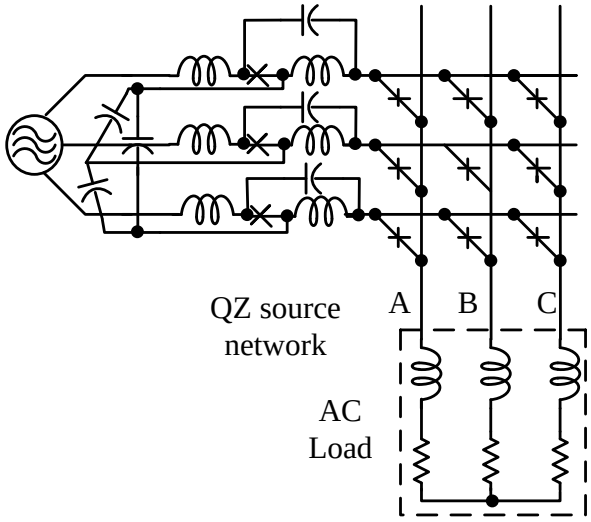


(g) Current-fed Z-source MC

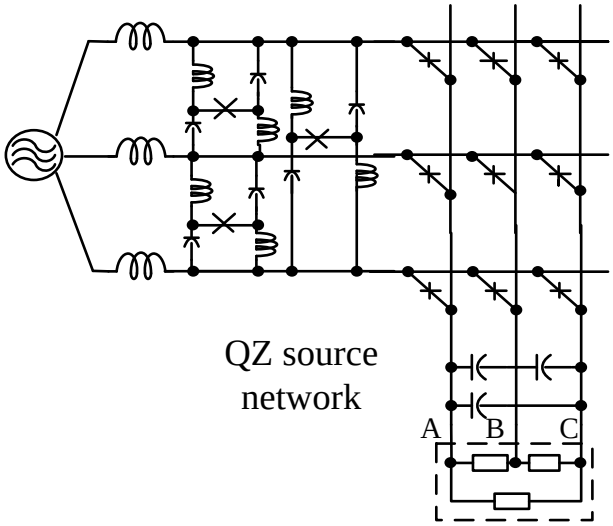


(h) Voltage-fed quasi-Z-source MC with discontinuous input current

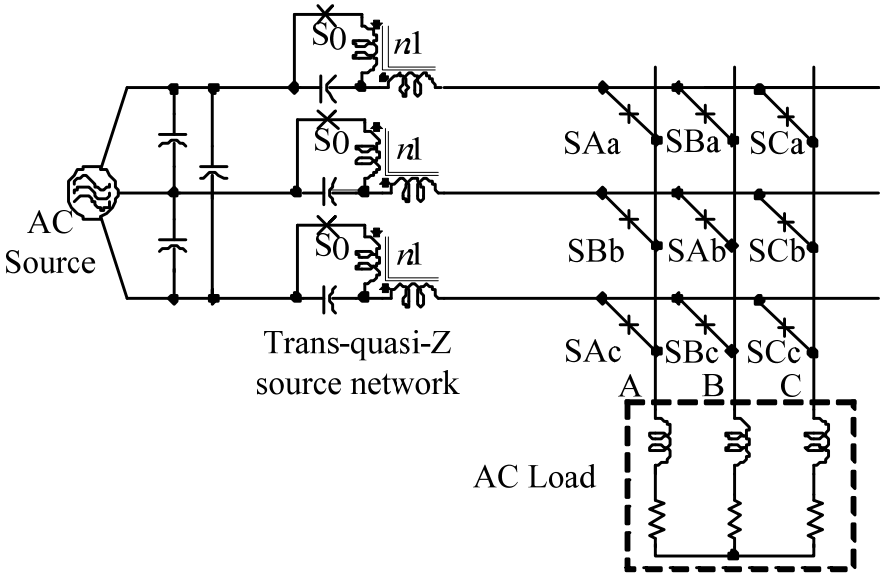
Figure 2.12 (cont'd)



(i) Voltage-fed quasi-Z-source MC with continuous input current

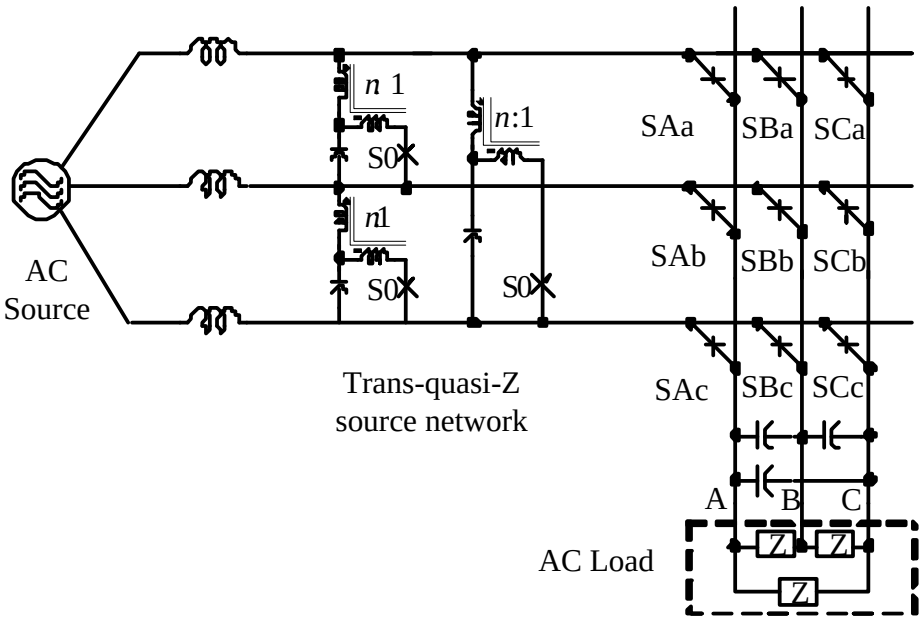


(j) Current-fed quasi-Z-source MC



(k) Voltage-fed trans-Z-source matrix converter

Figure 2.12 (cont'd)



(l) Current-fed trans-Z-source matrix converter

A family of direct Z-source matrix converter is shown in Figure 2.12, which has been proposed from our lab in paper []. The basic principle to derive these topologies is: apply the basic cell of Z-source/quasi-Z-source/trans-Z-source to each input phase of matrix converter. Thus the shoot through state in Z-source inverter is equivalent to the shoot through on three input phases of the matrix converter. The value and size of the Z-source LC network on the input side of matrix converter is much smaller than the ones in Z-source inverter dc side, because they are ac component, so they don't need to flow the dc current or undertake dc voltage. For example, compared to the Z-source indirect matrix converter proposed in other literatures, this ac capacitor and inductor are much smaller. However, the number of passive components also increases by 3 or 2/3. The sacrifice of the numbers of passives brings the benefits of reduced passive ratings. In addition, there is another advantage of direct matrix converter over the indirect one. Since the Z-network is separate from the matrix converter, the 18 switch RB-IGBT matrix converter module can be used. This module is more compact

than the two inverter structure. Also the passive size is reduced because the value and rating are significantly reduced. Thus the size of the inverter may be reduced by using this Z-source direct matrix converter topology.

For voltage-fed (VF) Z-source MC, its voltage gain can only reach 1.15, and also the phase shift caused by the Z-network makes the control not accurate. But for voltage-fed quasi-z-source matrix converter, the voltage gain can go to 4-5 times or even higher depending on the voltage rating of the switch. Although Z-source matrix converter has least amount of LC components, but it has limited voltage boost ratio, inherited phase shift caused by the Z-network, and also discontinuous current in the front of Z-source network. Quasi-Z-source matrix converter has higher boost ratio, no phase shift and lower switch voltage and current stress. In addition, the circuit in Figure 2.12(d) has continuous input current. In conclusion, voltage-fed quasi-Z-source matrix converter is a component less, size compact, high efficient, wide range buck-boost matrix converter.

2.7. Summary

Several converter synthesis techniques have been summarized and discussed, including graph theory, duality, inversion, cascade, parallel, switching cell, transformer and so on. A special inverter derivation technique “replacing one active switch by an inverter bridge” has been found from the relationship between basic dc-dc topology and Z-source inverter topology. By using this technique, several other single stage buck-boost inverter has been derived. More importantly, a group of switched-coupled-inductor inverter topologies, including voltage-fed and current-fed family, has been derived based on the tapped-inductor dc-dc converters, by using the same technique. The proposed new inverter topology has

higher boost ratio, less passive component, and smaller size than traditional dc-dc converter. It has three control freedoms: modulation index, extra shoot through/open zero state duty cycle, trans-ratio of the transformer. Different topologies and different control parameters can be selected according to different voltage/current gain requirement, in order to achieve minimum voltage and current stress on active devices and passive components.

CHAPTER 3 STEADY STATE CIRCUIT ANALYSIS

3.1. Introduction

The circuit analysis of five topologies has been given in this chapter: current-fed quasi-Z-source inverter, current-fed Z-source rectifier, switched-coupled-inductor inverter and Direct Z-source matrix converter. It includes the equivalent circuit states, voltage and current gain, operation regions, calculation of ac output voltage and current, passive component stress and active switch device power rating. For switched-coupled-inductor inverter, the voltage gain and voltage/current stress are compared among different topologies in the family. For Z-source matrix converter (MC), voltage-fed Z-source MC and voltage-fed quasi-Z-source MC have been selected to be analyzed on boost ratio and phase shift. The relationship between voltage gain and the control parameters such as modulation index, shoot through/open zero duty cycle are all derived, in order to aid the modulation of the circuit. The general analysis technique is the volt-seconds balance of dc inductor and the am-seconds balance of dc capacitor during one switching period.

The conventional current-source inverter has two major problems: unidirectional power flow and voltage boost operation, which makes it impossible to be used in many applications such as hybrid electric vehicles (HEVs) and general purpose variable speed motor drives. The Z-source inverters (ZSIs) can solve both problems. The quasi-Z-source inverters (qZSIs) were recently proposed as an important improvement to the traditional Z-source inverters. Besides the advantages inherited from the ZSIs, the qZSIs also have several of their own merits. This chapter presents a comprehensive study on the new features of the current-fed qZSI, including the advantageous buck-boost function, improved reliability, reduced passive

component ratings, and unique regeneration capability. The current-fed qZSI are bidirectional with an additional diode, unlike the voltage-fed Z-source inverter that needs a switch to achieve bidirectional power flow. A modified space vector pulse-width modulation (SVPWM) method is proposed and the available operating regions for motoring and regeneration operation are analyzed in this chapter. Since the current-fed qZSI has the same operation with the current-fed ZSI, many results of this chapter are also applicable to the current-fed ZSI. A reverse blocking IGBT (RB-IGBT) based current-fed qZSI prototype was developed in the laboratory. Both simulation and experimental results are shown to verify the theoretical analysis.

The voltage-source PWM rectifier (VSR) is a boost converter, thus its dc output voltage is much greater than the ac voltage, whereas the current-source PWM rectifier (CSR) is a buck converter and having a dc voltage smaller than its ac voltage. In addition, the CSR can only provide unidirectional power flow, thus unsuitable for regenerative operation. Recently, reverse blocking IGBT (RB-IGBT) has been developed for current-source and matrix converters. In this chapter, a current-fed Z-source PWM rectifier is proposed to overcome the limitations of the traditional VSR and CSR. The current-fed Z-source PWM rectifier with only six active switches can buck and boost voltage and provide bidirectional power flow. This chapter describes the operating principle of this current-fed Z-source PWM rectifier, presents a detailed steady state analysis and transient analysis. A RB-IGBT based current-fed Z-source PWM rectifier has been developed in laboratory. Both simulation and experimental results are shown to verify the operation and theoretical analysis.

A new family of switched-coupled-inductor inverters has been proposed in this thesis, with voltage buck-boost function. In voltage-fed switched-coupled-inductor inverter, a boost function can be implemented by introducing an extra shoot-through state on the inverter bridge. It utilizes the same principle as the Z-source inverter, but has higher boost ratio and lower active device voltage stress at the same voltage gain. It also has wider voltage buck/boost range than conventional boost-converter inverter. In current-fed switched-coupled-inductor inverter, a buck function can be implemented by introducing an extra open zero state on the inverter bridge. The current-fed topologies are capacitor-less solution among the buck-boost inverters, which reduces the system size significantly. In addition, compared to traditional boost-converter-inverter, it has less switch count, and less active device current stress. Compared to current-fed Z-source inverter, it has higher boost ratio and lower active device current stress. The inverter can sustain minimum voltage and current stress at a certain operation point, through adjusting the trans-ratio and the shoot through/open circuit duty cycle. The simulation results are given to verify the theory analysis and demonstrate the great merits of the switched-coupled-inductor inverter. It is beneficial to be applied in dc-ac applications that demand a high voltage gain from a very low voltage dc source, such as the micro-inverter in photovoltaic, or G/M in HEV

The matrix converter (MC) is a direct ac/ac converter with sinusoidal input/output waveforms and controllable input power factor [49-51]. It has less passive component compared to the existing back-to-back converter. Its control methods, circuit operation and possible applications have been investigated in paper [52-70]. It has a good perspective especially when the reverse-blocking IGBT is available now.

In a traditional matrix converter, the three switches on the same output phase leg can not be gated on at the same time because doing so would cause a short circuit(shoot through) to occur, which would destroy the converter. In addition, the maximum voltage gain can not exceed 0.866. These limitations can be overcome by Z-source matrix converter [1], which adds an impedance network (Z-network) in the input phase lines. The Z-source matrix converter advantageously utilizes the shoot through states to boost the ac voltage by gaiting on all the three switches on the same output phase leg. Therefore, the Z-source matrix converter can boost the voltage to be greater than the input voltage. in addition, the reliability of the converter is greatly improved because the shoot through states can no longer destroy the circuit. Also the current commutation steps can be simplified. Therefore, it provides a low-cost, reliable, and highly efficient structure for buck and boost ac/ac conversion.

3.2. Current-fed quasi-Z-source inverter

The Z-source inverters (ZSIs) have been proposed in [1] to overcome the limitations and problems of the traditional voltage-source inverter (VSI) and current-source inverter (CSI), which provide an attractive single-stage dc-ac conversion that is able to buck-boost voltage, increase efficiency and reduce cost. However, the ZSIs still have some drawbacks. The main drawback of the voltage-fed ZSI is that the input current is discontinuous in the boost mode and the capacitors must sustain at a high voltage, while the main drawback of the current-fed ZSI is that the inductors must sustain high currents. The quasi-Z-source inverters (qZSIs) have been proposed in [2] to further improve on the traditional ZSIs. Besides the advantages inherited from the ZSIs, the qZSIs also have their own merits, including reduced passive component ratings, continuous input current, a common dc rail between the source and

inverter, and so on. Since the publication of ZSIs, the voltage-fed ZSI received more attention than the current-fed ZSI. The performance, control methods and applications of voltage-fed ZSI are well-investigated in [3]–[11]. Nevertheless, it has a significant drawback that cannot maintain bidirectional power flow. The bidirectional power flow can only be achieved by replacing the diode with a bidirectional conducting, unidirectional blocking switch [12]–[13]; however, in this case, the advantages of single-stage topology are missing. The current-fed ZSI/qZSI, unlike the voltage-fed ZSI/qZSI, is bidirectional with a diode. The regeneration capability with a single-stage configuration makes the current-fed ZSI/qZSI a competitive power converter topology. Moreover, with the newly developed reverse blocking IGBT (RB-IGBT), the CSI is becoming more efficiency and thereby more attractive [14], [15].

This section focuses on the new features of the current-fed qZSI, especially the regeneration capability. Since the current-fed qZSI, in a manner, is consistent with the current-fed ZSI, the study results of this paper are also applicable to the current-fed ZSI. A current-fed qZSI prototype using RB-IGBTs was developed in the laboratory. Both simulation and experimental results are given to verify the theoretical analysis.

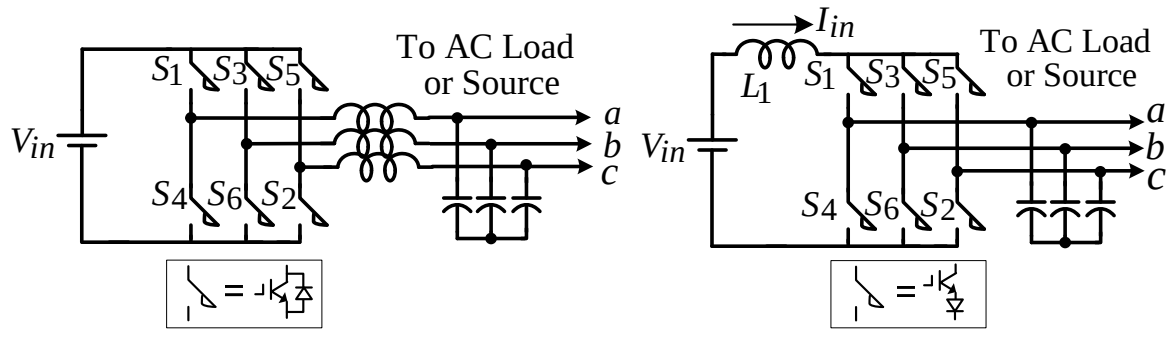


Figure 3.1. Traditional voltage source inverter and current source inverter

Figure 3.1 shows the conventional voltage source inverter and current source inverter. When they are applied in hybrid electrical vehicle motor drive, they have the following disadvantages: they are either a buck or boost converter, which limits the high voltage operation of VSI motor controllers and the low voltage low speed operation of CSI motor controllers; they are vulnerable to EMI noise, which is caused by shoot through states in VSI and open zero state in CSI; CSI only has unidirectional power flow since the input voltage source can not change its polarity.

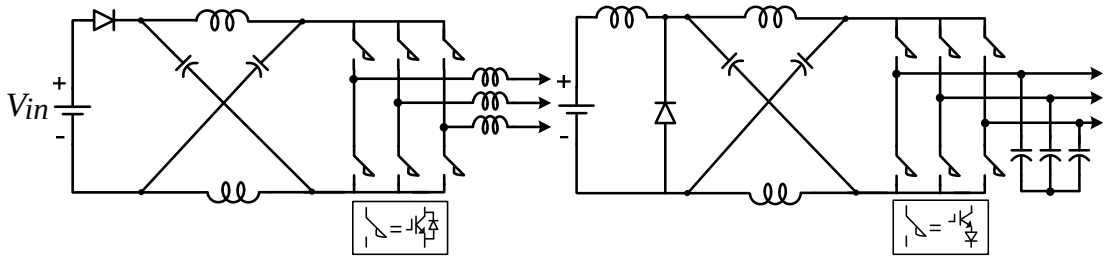


Figure 3.2. (a) voltage-fed Z-source inverter (b) current-fed Z-source inverter

An alternative approach is Z-source inverters (ZSIs), which provide an attractive single-stage dc-ac conversion that is able to buck-boost voltage, increase reliability and reduce cost.

However, voltage/current-fed ZSI also have their own limits: for voltage-fed ZSI, its input current is discontinuous in boost mode and its capacitor sustains high voltage; for current-fed ZSI, its inductor must sustain high currents.

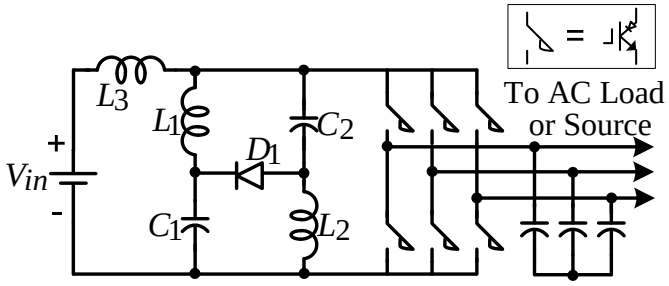
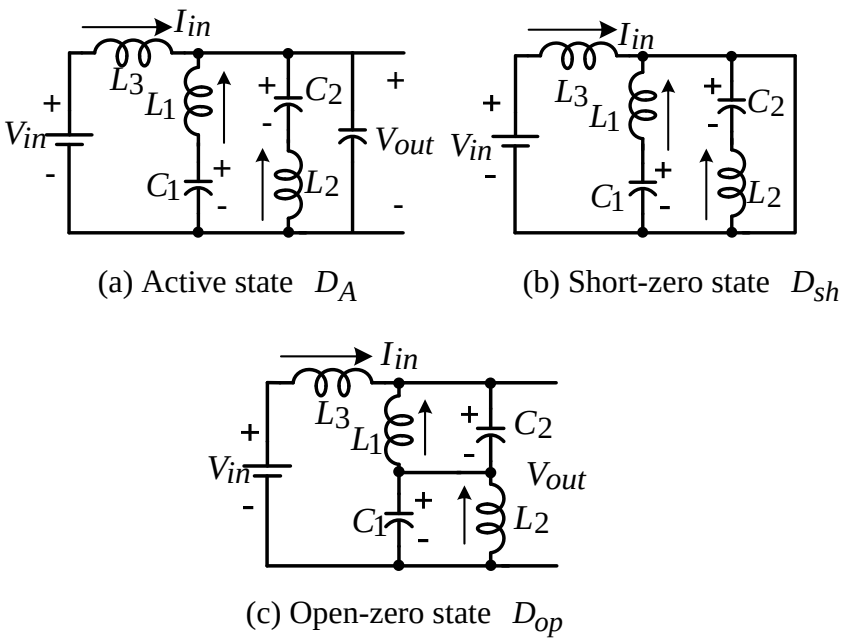


Figure 3.3 (a)voltage-fed quasi-Z-source inverter (b) current-fed quasi-Z-source inverter

Thus the recently proposed current-fed quasi-Z-source inverter in Figure 3.3 has been utilized in the HEV motor drive application to replace the Z-source topology. The current-fed quasi-Z-source inverter has the following advantages. Compared to voltage source inverter: it is a single-stage buck-boost inverter; it can tolerant short circuit in the bridge; and its output voltage is not PWM type but continuous sinusoidal. Compared to current source inverter: it can buck and boost voltage; it can tolerant open circuit in the bridge; it provides regeneration capability. Compared to two stage boost converter inverter: it is a single stage; it has two less active switches, which reduce the cost. Compared to voltage-fed Z-source inverter: it can regenerate power with only a diode in front; it has common dc rail between input and output. Compared to current-fed Z-source inverter: it has much less inductor current stress, which reduces the power loss; it has common dc rail. Compared to voltage-fed quasi-Z-source inverter: it can regenerate power without changing the front switch into active switch, thus reduces the switch count. Except for the above advantages, when this topology is adopted in hybrid electrical vehicle motor drive, it has the following additional benefits: the output current has less harmonics, and the motor has no high frequency loss, because both of the output voltage and current are sinusoidal; in addition, the motor has less bearing leakage current because of the reduced common mode voltage.

3.2.1 Equivalent circuit states



(a) Active state D_A (b) Short-zero state D_{sh}

(c) Open-zero state D_{op}

Figure 3.4 Equivalent circuits of the current-fed qZSI in continuous mode

During one switching period, there are three basic operation states depending on the inverter bridge's switching state. Figure 3.4 (a) (b) (c) shows the equivalent circuits of the three states. The traction motor can be considered as a three-phase RL load connected in Y connection. State I: Active state. Inverter bridge is operating in one of the six traditional active vectors, equivalent to a voltage-source (denoted as V_{out}). The

Table 3-1.The passive and device voltage in each circuit state

Operation states	Variables			
	V_C	V_L	V_{pn}	V_D
State I- Active State	V_{in}	$V_C - V_{eq}$	$V_C - V_L$ or V_{eq}	$2V_C - V_{pn}$
State II - Short zero state	V_{in}	V_C	0	$-2V_C$
State III- Open zero state	V_{in}	$-V_C$	$2V_C$	0

-quasi-Z network capacitor is being discharged during this process and the diode is off. The load current in the third phase flows through the capacitor and back to another phase. State II:

Short zero state. The dc link is shorted and separated from the load. The capacitor is still being discharged and the diode is off. The load current circulates through the capacitor path. State III: Open zero state. The inverter bridge is equivalent to an open circuit. The capacitor is being charged and the diode is on in this state.

Note that the open-circuit zero state doesn't affect the PWM control of the inverter, because it equivalently produce the same zero current to the load terminal. The available open circuit period is limited by the zero-state period that is determined by the modulation index.

Generally, the voltage on the diode is expressed as:

$$V_D = V_{pn} - (V_{C1} + V_{C2}) \tag{3.1}$$

Considering the circuit symmetry and zero average voltage on the inductor, the voltages on two capacitors are the same and equal to the input voltage. So the diode is off in short zero state and is on in open zero state. In active state, when the input and output voltage satisfies: $2V_{in} > V_{out}$, the diode is also in off state. If the condition can not be met or the capacitor is too small to maintain the voltage when it is discharged, the circuit will turn into new states which will be discussed later. The summary of capacitor voltage V_C, inductor voltage V_L, dc link voltage V_{pn} and diode voltage V_D are shown in Table 3-1.

3.2.2 Voltage gain and current gain

Considering the average voltage of the inductor L_3 over one switching period should be zero in steady state:

$$V_{out} = \frac{D_A + D_{sh} - D_{OP}}{D_A} V_{in} = \frac{1 - 2D_{OP}}{D_A} V_{in} \tag{3.2}$$

Where, D_A, D_{sh}, D_{OP} are the duty ratios of state I, state II, and state III respectively. Obviously, $D_{sh} + D_A + D_{OP} = 1$. In the same way, considering the average current of the

capacitors C_1 and C_2 over one switching period should be zero in steady state, one has

$$I_{L1} = I_{L2} = \frac{D_{OP}}{D_{sh} + D_A - D_{OP}} I_{in} = \frac{D_{OP}}{1 - 2D_{OP}} I_{in} \tag{3.3}$$

3.2.1. Operation regions

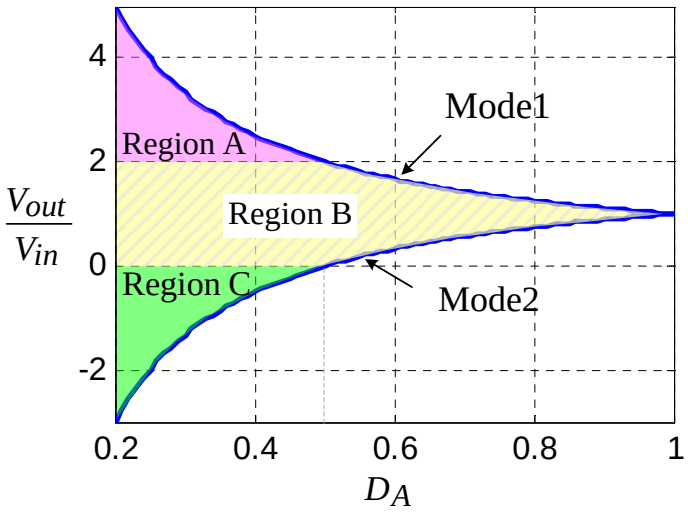


Figure 3.5 Operation region according to voltage gain vs. D_A curve

According to the constrains, the voltage gain can be plotted as a function of active duty cycle, in which for a certain D_A, the voltage gain occupies an area, not a single line, as shown in Figure 3.5.

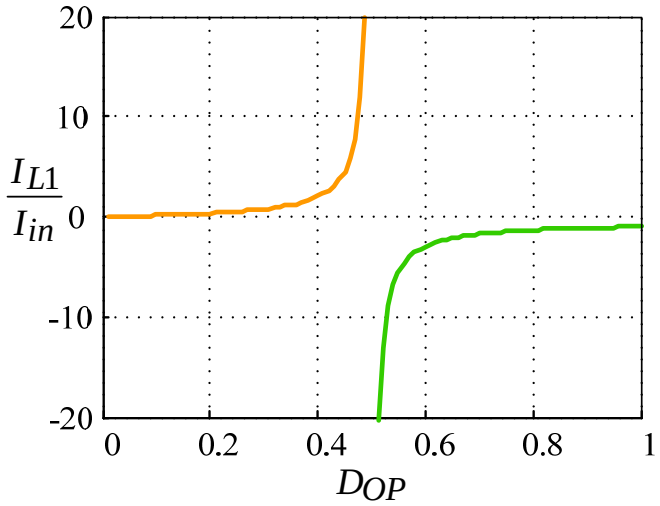


Figure 3.6. I_{L1} / I_{in} versus D_{OP} of the current-fed qZSI

The gain I_{L1} / I_{in} is only controlled by D_{op} according to equation (3.3), and its

relationship with D_{op} is shown in Figure 3.6. The direction of quasi-z source inductor current will always keep unchanged, so the direction of I_{in} will be changed when the sign of current gain changes. Obviously, when D_{op} is smaller than 0.5, I_{in} is positive, so the inverter works in motoring operation; when D_{op} is bigger than 0.5, I_{in} is negative, so the inverter works in energy regeneration operation. In another point of view, seeing from the output of the quasi-z network, I_{PN} can not be reversed because the inverter bridge is unidirectional conducting, so the power flow direction only depends on the polarity of V_{out}. As shown in Figure 3.5, motoring operation is corresponding to region A and region B when V_{out} is positive. However, as previously mentioned, region A is only available when the diode is replaced by a RB-IGBT. The polarity of V_{out} will be reversed when $\cos\phi < 0$. So energy regeneration operation corresponds to region C.

In summary, according to the sign of voltage gain, region B is motoring region, and region C is regenerative region. Region A is not available because voltage gain can not exceed 2 in this case; otherwise, the diode will un-properly turn on in active state since V_{out} is always bigger than two times of capacitor voltage (which is equal to input voltage).

At certain voltage gain requirement, there are infinite combinations of two control freedoms. The criterion to judge the best operation point is to obtain minimum voltage and current stress on the device when the voltage gain can reach the same requirements. Mode 1 and mode at the edge of the shadowed operation region at which D_A is the maximum available value are demonstrated to be the best operation point. In mode1, $Dop=0$, the current-fed qZSI operates like the conventional CSI. The gain is also the potential maximum gain that the current-fed qZSI can obtain with a given active duty ratio. In mode

2, $D_{op} = 1 - D_A$, the voltage gain is the potential minimum gain that the current-fed qZSI can obtain with a given active duty ratio *DA*. Therefore, we can get the desired voltage gain by tuning the two degrees of control freedom, D_A, D_{op}. The sum of these two control freedoms should be smaller than one, thus a parameter which represents the ratio of the D_{op} in zero state duty cycle as follows:

$$k = \frac{D_{op}}{1 - D_A} \tag{3.4}$$

When the current-fed qZSI operates in mode1, one has *k=0* because no open-zero states exist in this mode, we have

$$V_o = \frac{2\sqrt{2}V_{in}}{3\sqrt{3}m\cos\phi} \tag{3.5}$$

When the current-fed qZSI operates in mode2, one has *k=1,* because all short-zero states are turned into open-zero states in this mode

$$V_o = \frac{6\sqrt{6}m - 2\sqrt{2}\pi}{3\sqrt{3}\pi \cdot m\cos\phi} V_{in} \tag{3.6}$$

Above equations indicate that the output ac voltage can be stepped up and down by appropriately choosing operation mode and modulation index.

3.2.1. Calculation of the ac output voltage and current

Taking section II as example, the average equivalent voltage V_{out}, can be calculated as:

$$\overline{V_{out}} = \frac{\pi}{3}\int_{\frac{\pi}{2}}^{\frac{2\pi}{3}} \frac{T_1 v_{ab} + T_2 v_{ac}}{T_1 + T_2} d\theta = \frac{\sqrt{2}\pi}{2} V_o \cos\phi \tag{3.7}$$

The average equivalent duty cycle D_A can be expressed as

$$\overline{D_A} = \frac{3}{\pi}\int_{\frac{\pi}{2}}^{\frac{2\pi}{3}} \frac{T_1 + T_2}{T} d\theta = \frac{3\sqrt{3}}{2\pi} m \tag{3.8}$$

From (3.2), (3.7) and (3.8), the ac output voltage can be expressed as :

$$V_o = \frac{2\sqrt{2}\pi - 2\sqrt{2}k(2\pi - 3\sqrt{3}m)}{3\sqrt{3}\pi m \cos\phi} V_{in} \tag{3.9}$$

When the current-fed qZSI operates in mode 1, k=0, so the expression of V_o is the same as equation (3.5). While it operates in mode 2, k=1, the output phase voltage V_o in mode 2 can be derived. It has already been shown in equation (3.6).

So the output ac voltage can be stepped up and down by appropriately choosing operation mode and modulation index.

The dc output current of the quasi-z network i_{PN} is calculated as:

$$i_{PN} = i_{in} + i_{L1} + i_{c2} = \frac{1}{1-2D_{op}} i_{in} - S_D \frac{1}{1-2D_{op}} i_{in} \tag{3.10}$$

Where S_D is the switching function of the diode.

Since the average current of the capacitor over one switching period in steady state should be zero, the dc link current can be simplified as:

$$i_{PN} = \frac{1-D_{op}}{1-2D_{op}} i_{in} \tag{3.11}$$

So the output peak phase current from the inverter can be expressed as

$$i_{ac} = \frac{\sqrt{3}}{2} m i_{pn} = \frac{\sqrt{3}}{2} m \frac{1-D_{op}}{1-2D_{op}} i_{in} \tag{3.12}$$

Equation (3.12) shows that the output current can be stepped up and down by choosing an appropriate modulation index and open zero state duty cycle. Also in another view, if the required output power is fixed, the battery charging and discharging current can be controlled through regulating the open zero duty cycle D_{op}. Note that the open-circuit zero state doesn't affect the PWM control of the inverter, because it equivalently produce the same zero current to the load terminal. The available open circuit period is limited by the zero-state period that

is determined by the modulation index. Obviously the instantaneous input and output power are equal, since the output current could be boosted, the output voltage could be proportional bucked, and the motor can operate in the low speed operation.

3.2.1. Passive component stress and total switching device power rating

Both current-fed qZSI and current-fed ZSI have the energy regeneration ability with only a diode. Similarly to current-fed qZSI, current-fed ZSI also has three states in continuous mode. Its capacitor voltage is also equivalent to input voltage which is the same as qZSI. Also it has the same voltage gain V_{out}/V_{in} which is illustrated in Figure 3.5. However, its inductor current can be expressed as $I_{L1} = I_{L2} = \frac{1-D_{op}}{1-2D_{op}}$, which is different from qZSI shown in equation (3.3). For the same D_{op}, in motoring operation, qZSI has lower inductor current stress than ZSI, which is beneficial; while in energy regeneration operation, ZSI has lower inductor current stress than qZSI. For both topologies, the capacitor voltage is equal to the input voltage, so they have the same capacitor voltage stress.

For both qZSI and ZSI, at a given output power, the voltage gain is fixed at a certain value. But there are infinite choices for D_A and D_{op} at a given voltage gain as shown in Figure 3.5. In order to make the current stress on the inductor lowest, D_{op} should be designed to be zero at motoring operation mode and to be maximum at regeneration operation mode according to Figure 3.5. So the best operation point in region B for a given voltage gain which is bigger than 1 is on the curve of mode 1 and the best point for voltage gain smaller than 1 is on the curve of mode 2 because the D_{op} can be smallest when the D_A is maximum. For region C, the best operation point is on curve of mode 2 because D_{op} is maximum. Compared to traditional configuration with bidirectional DC/DC converter and VSI, the

current-fed qZSI has lower average switching device power rating.

3.3. Current-fed Z-source rectifier

The voltage-source PWM rectifier (VSR) is a boost converter, thus its dc output voltage is much greater than the ac voltage, whereas the current-source PWM rectifier (CSR) is a buck converter and having a dc voltage smaller than its ac voltage. In addition, the CSR can only provide unidirectional power flow, thus unsuitable for regenerative operation. Recently, reverse blocking IGBT (RB-IGBT) has been developed for current-source and matrix converters. In this chapter, a current-fed Z-source PWM rectifier is proposed to overcome the limitations of the traditional VSR and CSR. The current-fed Z-source PWM rectifier with only six active switches can buck and boost voltage and provide bidirectional power flow. Section 3.2 describes the operating principle of this current-fed Z-source PWM rectifier, presents a detailed steady state analysis and transient analysis.

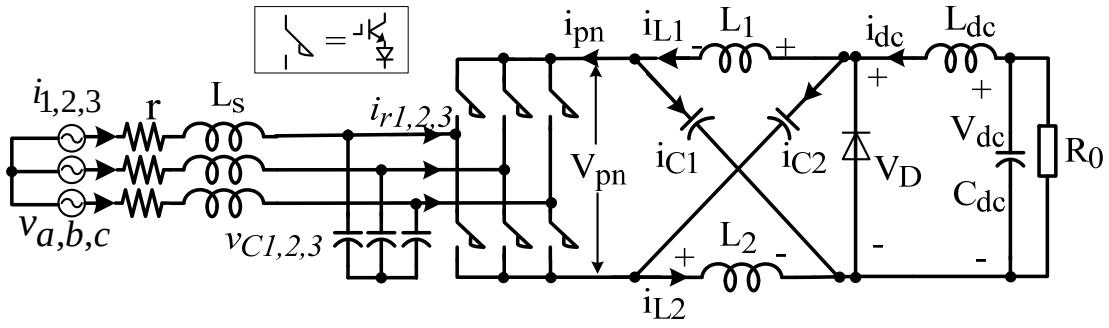
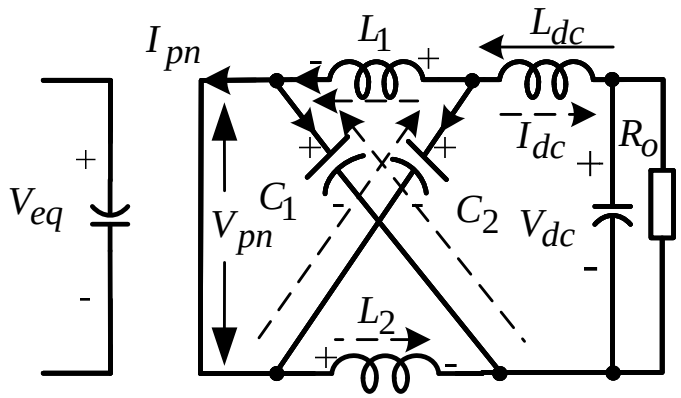
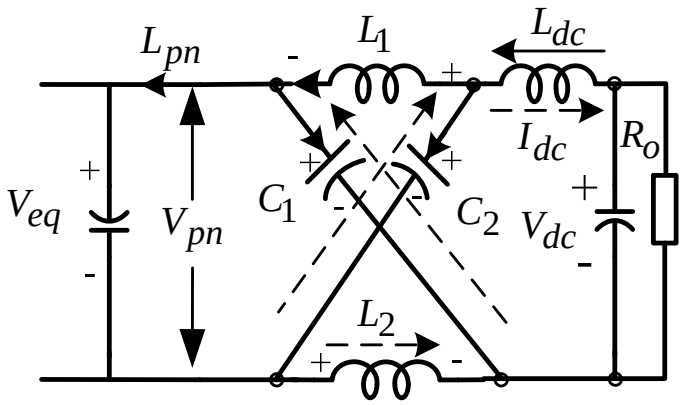


Figure 3.7. Current-fed Z-source rectifier

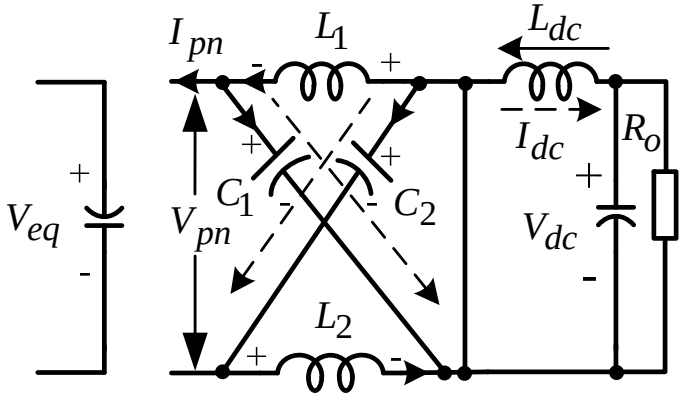
3.3.1. Equivalent circuit states



(a). State I – Short Zero: D_{sh}



(b). State II—Active: D_A



(c). State III—Open Zero: D_{op}

Figure 3.8.Operation states of current-fed Z-source PWM rectifier

Figure 3.8 shows the equivalent circuits of the current-fed Z-source PWM rectifier, where rectifier bridge becomes an equivalent voltage-source (V_{eq}). The solid arrows in Figure 3.8 define the positive direction of the current in $L_1, L_2, C_1, C_2, L_{dc}$ and the dotted

arrows show the actual direction in rectification operation. The sign + and – shows the defined positive direction of the voltage. In state I, short zero state, the rectifier bridge is equivalent to a short circuit, the dc-link voltage V_{pn} is zero, and the diode D is off because the voltage on the diode is equal to two times of the capacitor voltage which is a negative value. In state II, active state, shown in Figure 3.8 (b), the dc-link voltage V_{pn} is equal to V_{eq} and the diode D is off because the V_{eq} is negative in rectification operation; in state III, open zero state, shown in Figure 3.8(c), the rectifier is equivalent to an open circuit and the diode D is on which makes $V_L = V_C$. In all three states, the following equations are satisfied, assuming the Z-network has symmetric parameters that $C_1 = C_2 = C, L_1 = L_2 = L$:

$$V_{C1} = V_{C2} = V_{dc}, V_{pn} = V_C - V_L, V_D = 2V_C - V_{pn} \tag{3.13}$$

In SVPWM control, the instantaneous value of V_{eq} in one sector can be expressed as follows:

$$V_{eq} = \frac{T_1 \cdot v_{ab} + T_2 \cdot v_{ac}}{T_1 + T_2} = \frac{\frac{3\sqrt{2}}{2}\cos\phi}{\sin\theta} V_{srms} \tag{3.14}$$

, where V_{srms} is the rms value of the input phase voltage ; ϕ is the angle between input voltage and current; θ is the angle of the current reference vector; V_{eq} contains dc value and 6ω voltage ripple and changes with phase angle, nevertheless, the average value in every sector is constant, calculated as:

$$\overline{V_{eq}} = \left(\int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} \frac{\frac{3\sqrt{2}}{2} V_{srms}\cos\phi}{\sin\theta}\right) / \frac{\pi}{3} = \frac{\sqrt{2}\pi}{2} V_{srms}\cos\phi \tag{3.15}$$

When the rectifier input voltage and current has unity power factor, $\cos\phi = -1$, the average equivalent voltage is $\overline{V_{eq}} = -\sqrt{2}\pi V_{srms}/2$, which is always a negative value in rectification operation.

3.3.2. Voltage gain equation

D_{sh}, D_A, D_{op} are the duty ratios of state I, state II, and state III respectively. Obviously that $D_{sh} + D_A + D_{op} = 1$. According to equation (3.13),

In state I, $V_{pn} = 0, \quad V_C = V_L, V_{Ldc} = V_{dc} - 2V_c = -V_{dc}$;

In state II, $V_{pn} = V_{eq}, V_{Ldc} = V_{dc} - 2V_C + V_{eq} = V_{eq} - V_{dc}$;

In state III, $V_{L_{dc}} = V_{dc}$;

The average voltage on L_{dc} in an overall switching period is zero. So from voltage seconds balance, one has:

$$-V_{dc} \cdot D_{sh} + (V_{eq} - V_{dc}) \cdot D_A + V_{dc} \cdot D_{op} = 0 \tag{3.16}$$

$$V_{dc} = \frac{D_A}{D_A + D_{sh} - D_{OP}} V_{eq} = \frac{D_A}{1 - 2D_{OP}} V_{eq} \tag{3.17}$$

So the voltage gain is

$$\frac{V_{dc}}{V_{eq}} = \begin{cases} D_A & D_{OP} = 0 \\ \dfrac{D_A}{2D_A - 1} & D_{sh} = 0 \end{cases} \tag{3.18}$$

In the same way, considering average current of capacitor over one switching period should be zero in steady state, one has:

$$I_{dc} = \frac{D_{sh} + D_A - D_{OP}}{1 - D_{OP}} = \frac{1 - 2D_{OP}}{1 - D_{OP}} I_L \tag{3.19}$$

$$\frac{I_{dc}}{I_L} = \begin{cases} \dfrac{2D_A - 1}{D_A} & D_{OP} = 1 - D_A \\ 1 & D_{OP} = 0 \end{cases} \tag{3.20}$$

3.3.3. Operation regions

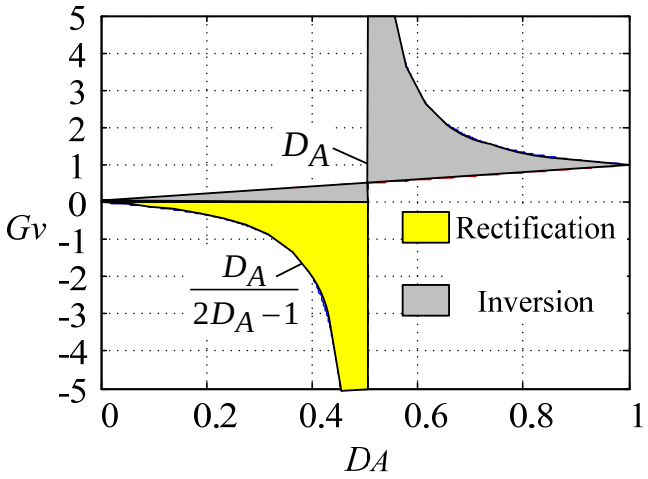


Figure 3.9. Voltage gain V_{dc}/V_{eq} v.s. D_A in all D_{op}

The voltage gain versus D_A is graphically illustrated in Figure 3.9, in case 1 ,without any open zero states and in case 2, turning entire short zero states to open zero states. When turning parts of short zero states into the open zero states, the voltage gain will be in the shadow operation region. Voltage gain can not be positive because it can cause the diode improperly conducting in state I. Diode Voltage is $V_D = 2V_C - V_{pn}$ .In state I, $V_{pn} = 0$, $V_D = 2V_C = 2V_{dc}$; When D_A is 0~0.5, $V_{dc}/V_{eq} < 0$ and when D_A is 0.5~1, $V_{dc}/V_{eq} > 0$. For rectifier, $V_{eq} < 0$ because $\cos\phi = -1$ and V_{eq} is reversed. So in order to get positive V_{dc} to prevent diode from unexpected conducting, the voltage gain should be negative. Note that, the output voltage can be higher or lower than the input voltage. In energy regenerative operation, D_A range is 0.5~1.

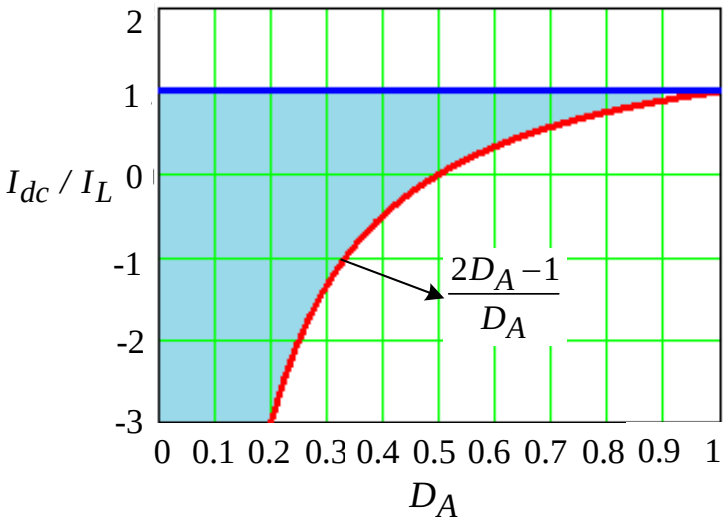


Figure 3.10. Current gain I_{dc} / I_L vs D_A in all D_{op}

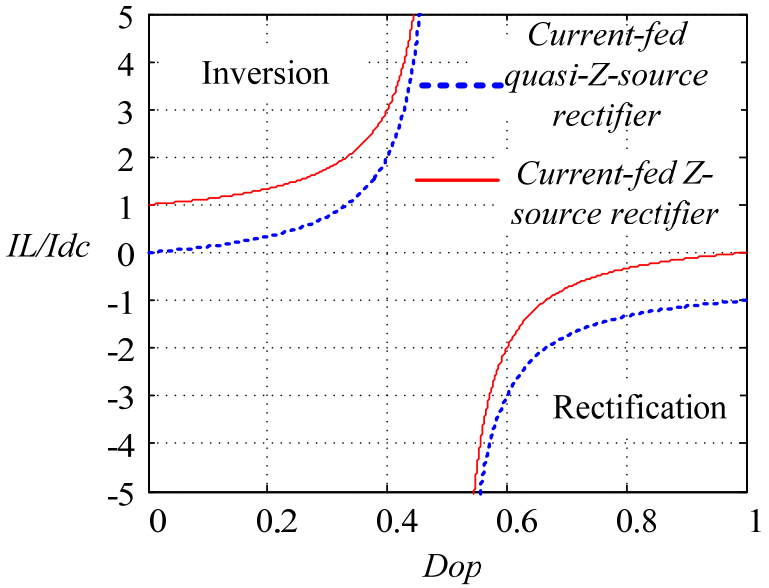


Figure 3.11. Current gain I_L / I_{dc} vs D_{op} in all D_{op}

The current gain versus D_A and current gain versus D_{op} are shown in Figure 3.10 and Figure 3.11 respectively. The shadow area is the rectification operation region. In rectification operation, the dc current on L_{dc} is flowing from AC side to DC side. Since the direction of Z-source network inductor current will keep unchanged, the current gain of Idc/IL2 will be negative which means $D_{op} > 0.5$. The current gain vs. D_{op} is also plot for current-fed quasi-Z-source inverter. It can be seen that the current-fed Z-source rectifier has

lower current stress than quasi-Z-source rectifier at the same D_{op}. Thus Z-source topology has better efficiency and lower cost than quasi-Z-source topology in rectification operation.

3.3.4. Calculation of the ac output voltage and current

To get voltage gain between dc and input ac rms phase voltage, the average value of D_A and average value of V_{eq} need to be derived from three phase AC system.

According to the space vector control diagram, the instantaneous duty ratio of active state can be calculated as:

$$D_A = \frac{T_1 + T_2}{T} = \frac{2}{\sqrt{3}} \left| \vec{I} \right| \sin\theta = \frac{\sqrt{3}}{2} m \sin\theta \tag{3.21}$$

, where m is the modulation index of the PWM rectifier and θ is the angle of the space vector. Obviously that D_A changes with the angle in every sector. However, the average value of D_A keeps the same in all sectors, which can be calculated as:

$$\overline{D_A} = \frac{T_1 + T_2}{T} = \frac{\sqrt{3}}{2} m \frac{3}{\pi} \int_{\frac{\pi}{2}}^{\frac{2\pi}{3}} \sin\theta d\theta = \frac{3\sqrt{3}}{2\pi} m \tag{3.22}$$

In addition, the average value of V_{eq} is the same as conventional CSI which is calculated in equation (3.14). From equation (3.17), (3.18), (3.22), the voltage gain between output dc voltage and input three phase rms voltage can be derived as:

$$V_{dc} = \frac{D_A}{1 - 2D_{op}} V_{eq} = \frac{1}{2D_{op} - 1} \frac{3\sqrt{6} m \cos\phi}{4} V_{srms} \tag{3.23}$$

When $D_{op} = 0$, the equation is the same as conventional current source shown in (3.14); when $D_{op} = 1 - D_A$, it stands for changing all the zero state into open zero state, which is corresponding to mode 2. When D_{op} is fixed at a certain value, the voltage gain only depends on the modulation index and input power factor. The relationships between them at $D_{op} = 0.65$ are shown in Figure 3.12.

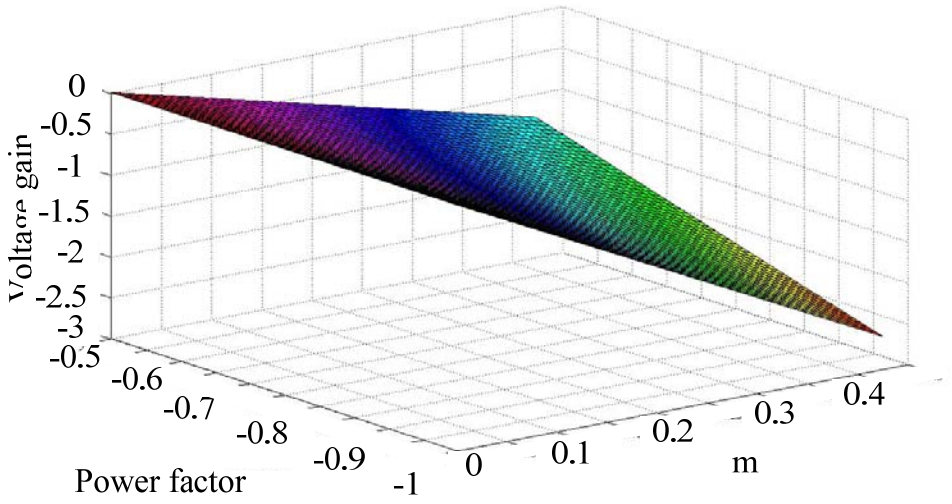


Figure 3.12. The dc output gain V_{dc}/V_{srms} m and power factor, at $D_{op} = 0.65$

3.3.5. Design of Z-network L and C in continuous mode

For the three operation states shown in Figure 3.8, in short zero state and active state, inductor current is increasing and the inductor is in its charging time; during the open zero state the inductor current is decreasing and the inductor is in its discharging time. But the average current of L is a constant value which has been derived in equation (3.19), written as:

$$I_L = I_{dc}\frac{1-D_{OP}}{1-2D_{OP}} \tag{3.24}$$

Assume that the capacitor voltage keeps equal to the dc voltage, so the current ripple peak to peak value of L is:

$$\Delta I_L = \frac{V_L}{L}D_{op}T = \frac{-V_C}{L}D_{op}T = \frac{-V_{dc}}{L}D_{op}T \tag{3.25}$$

, which takes D_{op} to calculate since it is relatively constant.

So the minimum current can be calculated as:

$$I_{Lm} = \frac{1-D_{op}}{1-2D_{op}}I_{dc} - \frac{V_{dc}}{2L}D_{op}T \tag{3.26}$$

In order to make it working in the CCM, it must have

$$I_{Lm} > 0 \tag{3.27}$$

Therefore

$$L > \frac{V_{dc} D_{op} (1 - 2D_{op}) T}{2(1 - D_{op}) I_{dc}} \tag{3.28}$$

Furthermore, the expressions for capacitor voltage in non-open zero state and open zero state are shown as follows:

$$\begin{cases} I_C = I_{dc} - I_L = \dfrac{-D_{op}}{1 - 2D_{op}} I_{dc} < 0 & \left[Non - open\ zero\ state \right] \\ I_C = I_L = \dfrac{1 - D_{op}}{1 - 2D_{op}} I_{dc} > 0 & \left[Open\ zero\ state \right] \end{cases} \tag{3.29}$$

Obviously the capacitor discharges in non-open zero state and charges in open zero state. The peak to peak value of the voltage ripple is

$$\Delta V_C = \frac{I_C}{C} (1 - D_{op}) T = \frac{D_{op} (1 - D_{op})}{C(2D_{op} - 1)} I_{dc} T \tag{3.30}$$

So the minimum capacitor voltage is

$$V_{C\min} = \overline{V_C} + \frac{\Delta V_C}{2} = V_{dc} + \frac{D_{op} (1 - D_{op})}{2(2D_{op} - 1)C} I_{dc} T \tag{3.31}$$

In order to avoid the diode improperly conducts in active state, the diode voltage V_D has to be a negative value.

In active state:

$$\left.\begin{array}{l} V_D = V_L + V_C \\ V_{eq} = V_C - V_L \end{array}\right\} \Rightarrow V_D = 2V_C - V_{eq} > 0 \Rightarrow V_C > \frac{V_{eq}}{2} \tag{3.32}$$

While in rectification operation, V_{eq} is a negative value. So the minimum capacitor voltage should be bigger than zero. Therefore the requirement for capacitor value in continuous mode is

$$C > \frac{D_{op}(1-D_{op})I_{dc}T}{2(1-2D_{op})V_{dc}} \tag{3.33}$$

Assumed the operation condition is $V_{dc} = 85V$, $D_{op} = 0.65$, $T = 100us$, $\overline{I_{dc}} = -8A$, then the design value for L and C should satisfy:

$$L > 0.25mH,\ C > 3.6uF \tag{3.34}$$

In the simulation and experiments, *L=2mH, C=200uF*.

3.4. Switched-coupled-inductor inverter

The simplest method of extending the duty cycle range of classical dc–dc converters consists of connecting the tapped point of the single inductor to other components such as main switching device, freewheeling diode, input or output rails giving rise to the well-known tapped-inductor converter circuits [93]. One of the buck converter derived version is named as Watkins-Johnson converter [94, 95].

By using tapped-inductor converters, the weight, size, complexity, and cost associated are reduced when compared with other duty cycle extension methods (such as cascading several basic dc–dc converters and the use of multi-winding transformers). Using tapped inductor, it forms an additional control parameter, the trans-ratio of the tapped inductor. So the high step down or step up function can be implemented [96, 97] Since the tapped inductor is similar to the auto transformer, the energy is stored in the inductor when the transistor is turned on and released to the output when it is turned off. Different connection ways of the tapping point to the outside components generate different topologies, thus brings different voltage and current stress on active device and passive components [98]. The best topology can be chosen at a given voltage gain requirement.

The tapped inductor can also assist soft-switching of the active switch in dc-dc converter [99, 100]. It can also be utilized as the output filter [101, 102] to form a soft-switching loop for full bridge converter [101, 102].

A novel switched-coupled-inductor inverter is proposed here, inspired by the principle of the tapped inductor converter. It utilizes an extra shoot through state in VSI and open zero state in CSI to implement voltage buck-boost function. It has been demonstrated through theory and simulations that the proposed switched-coupled-inductor inverter has much wider range for voltage buck/boost, and lower voltage/current stress than other extended buck-boost inverter, including boost converter inverter and Z-source inverter. Both of the voltage-fed and current-fed topologies have fewer active switch than other extended topologies. Current-fed topologies are a capacitor-less solution, which greatly reduces the system size.

In a word, the proposed family of topologies provides a high boost, low cost and compact solution for a buck-boost inverter. It is suitable to use in photovoltaic micro-inverter and electrical vehicle motor drive.

3.4.1. Voltage-fed switched-coupled-inductor inverter

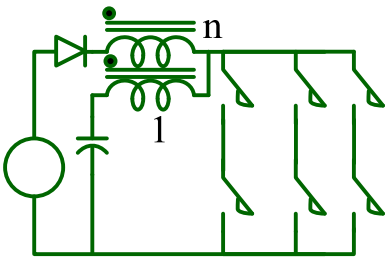
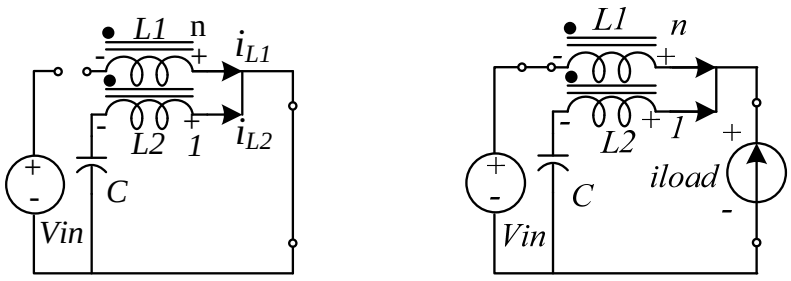


Figure 3.13. Voltage-fed switched-coupled-inductor inverter 2 (VF-SCII 2)

3.4.1.1. Equivalent circuit states

Take VF-SCII 2 as the representative of voltage source inverter. VF-SCII 2 has two operating states: shoot through state and non-shoot through state, as shown in Figure 3.14. Shoot through means turning on the upper and lower switches on the same phase leg at the same time. If the shoot through is chosen to happen during the normal



(a) (b)

Figure 3.14. Inverter b operating states

(a) shoot through state D_0 (b) non-shoot-through state $1-D_0$

zero state, it will not affect the output voltage and current. However, the front inductor gets charged during shoot through state, so the inverter can boost voltage. The two equivalent circuit states of VF-SCII 2 are shown in Figure 3.14. When the inverter bridge shoot through happens, the front diode automatically turns off, and inductor 2 gets charged. In non-shoot through state, the diode is on, and inductor 1 gets discharged. The inverter can be considered as a current source with equivalent voltage V_{out} in this case. In the whole switching period, the energy in the coupled inductor gets balanced, which means the total turns current product *(N*I)* keeps constant.

3.4.1.2. Voltage and current gain

The inductor current volts-seconds balance and the capacitor voltage am-seconds balance are taken as the criterion to derive the voltage and current gain equation for this

circuit. Neither inductor current has been taken as the research target but a combination of the two current. The reason will be illustrated in the following.

In shoot through state, L_1 has zero current, but L_2 is charged by C_1. In non-shoot-through state, L_1 and L_2 are in series and charged by the voltage difference between source and capacitor. The inductor voltages in two states are:

$$\begin{cases} V_{L1\_1} = -\dfrac{n}{n-1}(V_{in} - V_{C1});\ V_{L2\_1} = -\dfrac{1}{n-1}(V_{in} - V_{C1}) & [at\ (1-D_0)] \\ V_{L1\_2} = nV_{L2} = -nV_{C1};\ \ V_{L2\_2} = -V_{C1} & [at\ D_0] \end{cases} \tag{3.35}$$

, in which n is the trans ratio between L1 and L2, and D_0 is the shoot through duty cycle. Each inductor current is discontinuous since it has different expressions at different circuit states during one switching cycle. In another word, it has jump during one switching period. But the total flux in the inductor keeps constant. So a continuous unit inductor current can be defined here:

$$i_L = \frac{ni_{L1} + i_{L2}}{(n+1)} \tag{3.36}$$

This current can be taken as the state variable in the state space model since it is continuous.

Therefore, take unit inductor current i_L and capacitor voltage V_C as the state variables, then the state space equation of VF-SCII 2 is:

$$\begin{cases} L\dfrac{di_L}{dt} = \dfrac{1}{1+n}(V_{L1\_1} + V_{L2\_1}) = \dfrac{1}{1-n}(V_{in} - V_C) \\ C\dfrac{dv_C}{dt} = i_L + \dfrac{n}{n-1}i_{load} \end{cases} \quad [at\ (1-D_0)]$$

$$\begin{cases} L\dfrac{di_L}{dt} = \dfrac{1}{1+n}(V_{L1\_2} + V_{L2\_2}) = -V_C \\ C\dfrac{dv_C}{dt} = (1-n)i_L \end{cases} \quad [at\ D_0] \tag{3.37}$$

The steady state solution for inductor current and capacitor voltage could be obtained by

using state space average method. The average inductor current and capacitor voltage are:

$$\begin{cases} \overline{L\frac{di_L}{dt}} = \frac{1-D_0}{1-n}(V_{in}-V_C)-D_0V_C \\ \overline{C\frac{dv_C}{dt}} = (1-D_0)(i_L+\frac{n}{n-1}i_{load})+D_0(1-n)i_L \end{cases} \tag{3.38}$$

The volt-seconds and ampere-seconds balances impose:

$$\overline{L\frac{di_L}{dt}} = 0; \quad \overline{C\frac{dv_C}{dt}} = 0; \tag{3.39}$$

Thus the averaged i_L and v_C can be derived as:

$$I_L = \frac{-n(1-D_0)}{1-nD_0}i_{load}; \quad V_C = \frac{1-D_0}{1-nD_0}V_{in} \tag{3.40}$$

The equivalent output voltage in non-shoot-through state in average model can also be derived as:

$$V_{out} = \frac{V_C}{1-D_0} = \frac{1}{1-nD_0}V_{in} \tag{3.41}$$

Thus the boost ratio of the switched-coupled-inductor network is:

$$B = \frac{1}{1-nD_0} \tag{3.42}$$

The voltage gain between input and output then can be expressed as, by using that $D_0 = 1-\sqrt{3}M/2$:

$$G = MB = \frac{M}{1-nD_0} = \frac{M}{1-n(1-\frac{\sqrt{3}}{2}M)} \tag{3.43}$$

, from which it can be seen that this inverter has voltage buck-boost function.

The current stress on the active devices in inverter bridge is equal to output current in non-shoot through state. But the maximum current stress depends on the current in shoot through state, which is the inductor 2 current in this case. According to the flux constant

equation:

$$(n+1)\bar{i}_L = 1 \cdot i_{L2}' \tag{3.44}$$

Table 3-2.Voltage gain and active/passive device stress for VF-SCII

	Passive Stress		**Voltage Gain**
	Vc/Vin	**IL/iload**	**Vout/Vin**
VF-SCII 1	$\frac{(1-D_0)}{1+nD_0}$	$\frac{n(1-D_0)}{1+nD_0}$	$\frac{1}{1+nD_0}$
VF-SCII 2	$\frac{(1-D_0)}{1-nD_0}$	$\frac{-n(1-D_0)}{1-nD_0}$	$\frac{1}{1-nD_0}$
VF-SCII 3	$\frac{(n+1)(1-D_0)}{1+n(1-D_0)}$	$\frac{n(1-D_0)}{1+n-nD_0}$	$\frac{(n+1)}{1+n(1-D_0)}$
VF-SCII 4	$\frac{(-n+1)(1-D_0)}{1-n(1-D_0)}$	$\frac{-n(1-D_0)}{1-n+nD_0}$	$\frac{-n+1}{1-n(1-D_0)}$
VF-SCII 5	$\frac{n(1-D_0)}{n(1-D_0)-D_0}$	$\frac{n(1-D_0)}{(n+1)D_0-n}$	$\frac{n}{n(1-D_0)-D_0}$
VF-SCII 6	$\frac{n(1-D_0)}{n(1-D_0)+D_0}$	$\frac{-n(1-D_0)}{(-n+1)D_0+n}$	$\frac{n}{n(1-D_0)+D_0}$
	INV I Stress	**Frong Switch Stress**	
	Isw/Iload	**Vfs/Vin**	**Ifs/Iload**
VF-SCII 1	$\left\lvert\frac{n(1-D_0)}{1+nD_0}\right\rvert$	$\frac{1+n}{1+nD_0}$	$\frac{-1}{1+nD_0}$
VF-SCII 2	$\left\lvert\frac{-n(1-D_0)}{1-nD_0}\right\rvert$	$\frac{1-n}{1-nD_0}$	$\frac{-1}{1-nD_0}$
VF-SCII 3	$\left\lvert\frac{n(1-D_0)}{1+n-nD_0}\right\rvert$	$\frac{1}{1+n-nD_0}$	$\frac{-1-n}{1+n-nD_0}$
VF-SCII 4	$\left\lvert\frac{-n(1-D_0)}{1-n+nD_0}\right\rvert$	$\frac{1}{1-n+nD_0}$	$\frac{-1+n}{1-n+nD_0}$
VF-SCII 5	$\left\lvert\frac{(n+1)(1-D_0)}{(n+1)D_0-n}\right\rvert$	$\frac{n(1-D_0)-1}{n(1-D_0)-D_0}$	$\frac{n}{nD_0+D_0-n}$
VF-SCII 6	$\left\lvert\frac{(-n+1)(1-D_0)}{(-n+1)D_0+n}\right\rvert$	$\frac{-n(1-D_0)-1}{-n(1-D_0)-D_0}$	$\frac{-n}{-nD_0+D_0+n}$

The L2 current in shoot through state can be derived as:

$$i_{L2}' = \frac{n(1-D_0)}{1+nD_0} \tag{3.45}$$

, which is also the current stress on the active device.

Similarly, the voltage gain and voltage/current stress on device can be derived for other voltage-fed topologies, as shown in Table 3-2.

3.4.2. Current-fed Switched-Coupled-Inductor Inverter

3.4.2.1. Equivalent circuit sates

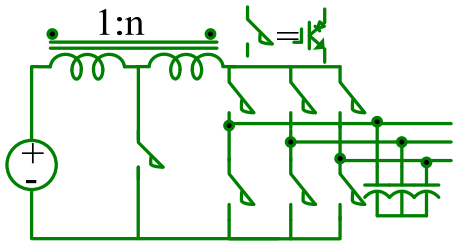
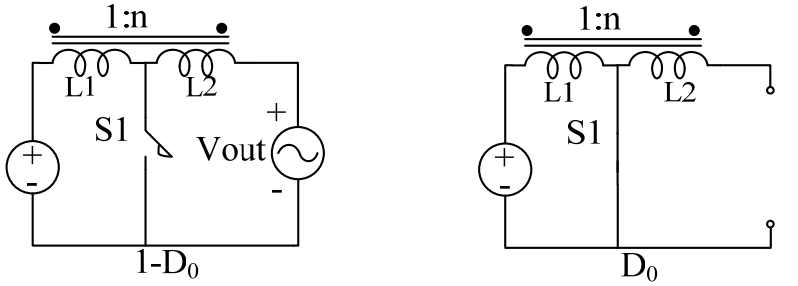


Figure 3.15 Current-fed switched-coupled-inductor inverter 2 (CF-SCII 2)



(a)Active state (b) open zero state D_0

Figure 3.16. Two operation states of CF-SCII 2

CF-SCII 2 in Figure 3.15 is taken as an study example here. It has two operating states shown in Figure 3.16. The extra open zero state has a duty cycle of D_0 .

3.4.2.2. Voltage gain and current gain

The volt-seconds equation on L1 leads to:

$$(1-D_0)(V_{in}-V_{out})\frac{1}{1-n}+D_0V_{in}=0 \tag{3.46}$$

Thus voltage gain V_{out}/V_{in} is:

$$V_{out}/V_{in}=\frac{1-nD_0}{1-D_0} \tag{3.47}$$

Table 3-3.Voltage Gain and Active/Passive Device Stress for CF-SCII

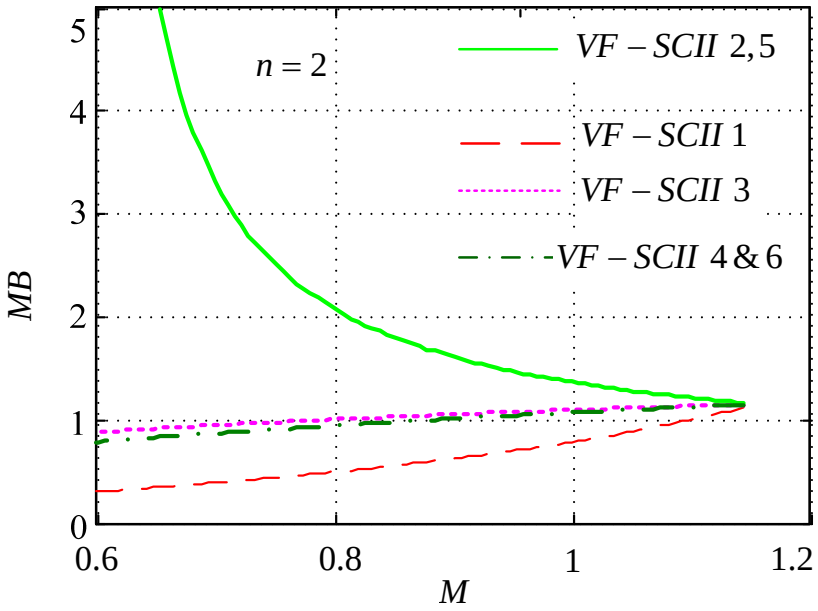
	Voltage Gain	Inductor	INV switch
		current stress	voltage stress
	Vout/Vin	IL/(Vin/2R)	Vsw/Vin (D0)
CF-SCII 1	$\frac{1+nD_0}{1-D_0}$	$\frac{1}{1-D_0}\cdot G$	$\frac{1+nD_0}{1-D_0}$
CF-SCII 2	$\frac{1-nD_0}{1-D_0}$	$\frac{1}{1-D_0}\cdot G$	$\frac{1-nD_0}{1-D_0}$
CF-SCII 3	$\frac{n(1-D_0)+1}{(n+1)(1-D_0)}$	$\frac{1}{(n+1)(1-D_0)}\cdot G$	$\frac{n(1-D_0)+1}{(n+1)(1-D_0)}$
CF-SCII 4	$\frac{1-n(1-D_0)}{(1-n)(1-D_0)}$	$\frac{1}{(1-n)(1-D_0)}\cdot G$	$\frac{1-n(1-D_0)}{(1-n)(1-D_0)}$
CF-SCII 5	$\frac{n(1-D_0)-D_0}{n(1-D_0)}$	$\frac{1}{(n+1)(1-D_0)}\cdot G$	$\frac{n(1-D_0)-D_0}{n(1-D_0)}$
CF-SCII 6	$\frac{n(1-D_0)+D_0}{n(1-D_0)}$	$\frac{1}{(1-n)(1-D_0)}\cdot G$	$\frac{n(1-D_0)+D_0}{n(1-D_0)}$
	Inverter switch	Front switch stress	
	current stress		
	Isw/(Vin/2R)	Vs/Vin	Is/（Vin/2R)
CF-SCII 1	$\frac{1}{1-D_0}\cdot G$	$\frac{1}{1-D_0}$	$\frac{1+n}{1-D_0}\cdot G$
CF-SCII 2	$\frac{1}{1-D_0}\cdot G$	$\frac{1}{1-D_0}$	$\frac{1-n}{1-D_0}\cdot G$
CF-SCII 3	$\frac{1}{1-D_0}\cdot G$	$\frac{1}{1-D_0}$	$\frac{1}{(1+n)}\frac{1}{(1-D_0)}\cdot G$
CF-SCII 4	$\frac{1}{1-D_0}\cdot G$	$\frac{1}{1-D_0}$	$\frac{1}{(1-n)}\frac{1}{(1-D_0)}\cdot G$

Thus when n<1, it can boost voltage; when n>1, it can buck the voltage; when n goes to even bigger that $n>\frac{1}{D_0}$, it enters into regeneration mode.

In each state, the similar state space equations can be built. The voltage gain, active and passive device stress can all be derived from the state equations. All the equations for current-fed switched-coupled-inductor inverter family are derived and demonstrated by simulation. They are shown in Table 3-3.

3.4.2.3. Voltage and current stress comparison

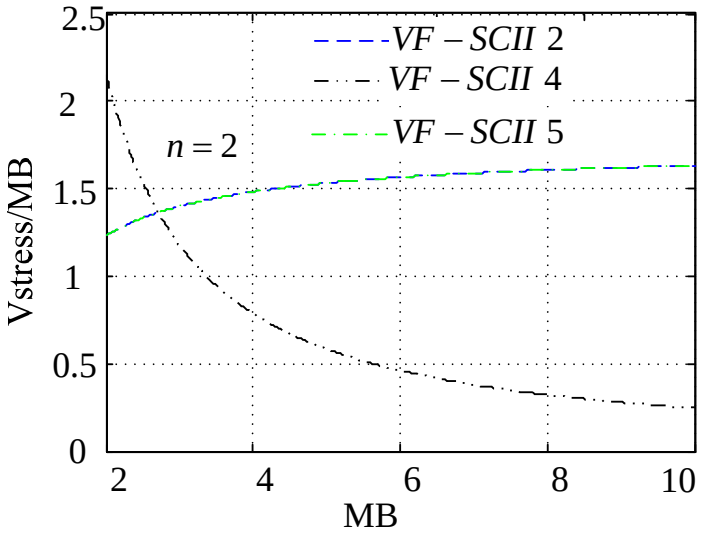
The comparison among voltage-fed switched-coupled-inductor inverters are shown in Figure 3.17.The features of the family of voltage-fed SCI inverter are: (1) Only SCI 2, 4, 5 have boost function; (2) VF-SCII 2 has higher voltage stress than VF-SCII 5 when boost ratio is over 2, but VF-SCII 2 has lower current stress than VF-SCII 5 in the same condition.



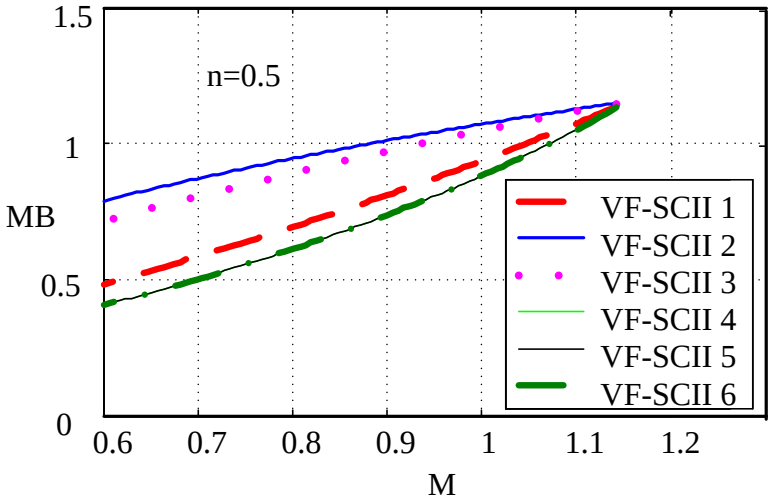
(a) Voltage gain(MB) versus modulation index for voltage-fed switched-coupled-inductor inverter at n=2

Figure 3.17. Comparison among the voltage-fed switched-coupled-inductor inverters

Figure 3.17 (cont'd)

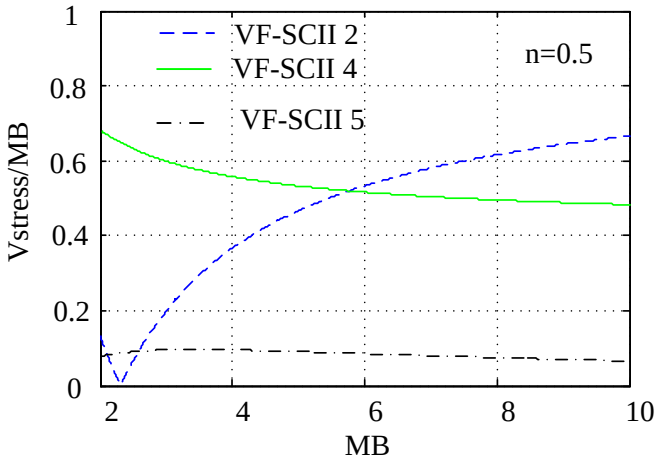


(b) Active switch voltage stress of voltage-fed switched-coupled-inductor inverter

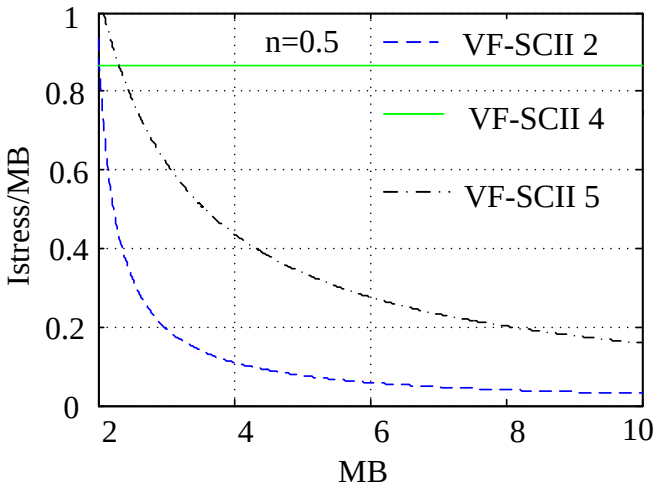


(c) Voltage gain vs. M for voltage-fed topologies at n=0.5

Figure 3.17 (cont'd)



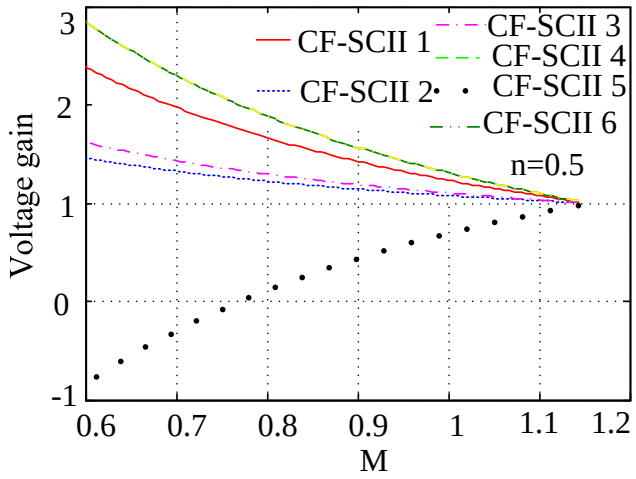
(d) Active switch voltage stress for voltage-fed topologies



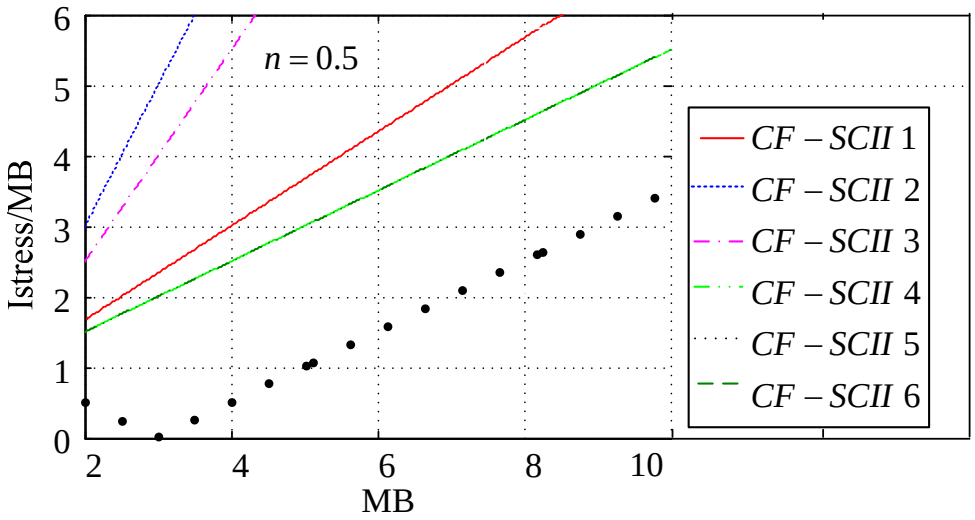
(e) Active switch current stress for voltage-fed topologies

The comparison among the current-fed switched-coupled-inductor inverters are shown in Figure 3.18. The plot of voltage gain versus the modulation index and current stress versus voltage gain are shown in two cases: n=0.5 and n=2. When n=0.5 is chosen, inverter 1, 2, 3, 4, 6 all have voltage boost function. And inverter 4 and 6 have the lowest current stress among the five, at all gains bigger than 2. When n=2 is chosen, inverter 1, 3, 6 have voltage boost function, and the others can only buck voltage. Among the ones with boost function,

current-fed inverter 1 has much lower current stress than the other two. Since the voltage gain of current-fed switched-coupled-inductor inverters is a function of multiple variables: trans-ratio, open zero duty cycle and modulation index. Different trans-ratio and open zero duty cycle can be chosen to obtain minimum active switch or passive component voltage/current stress, at a certain voltage gain requirement.



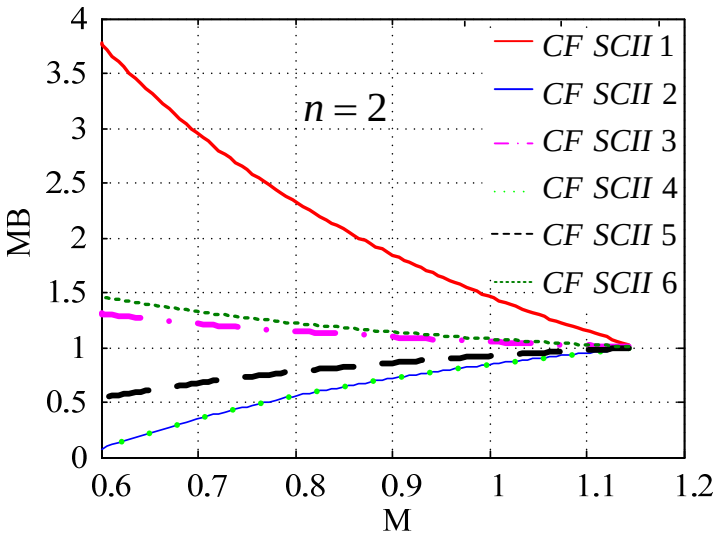
(a) Voltage gain vs. M at n=0.5 for current-fed topologies



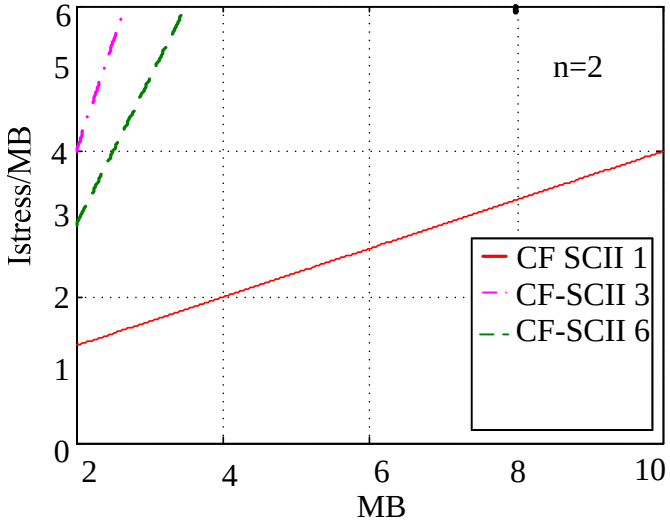
(b) Current stress vs. voltage gain at n=0.5 for current-fed topologies

Figure 3.18. Comparison among the current-fed switched-coupled-inductor inverters

Figure 3.18 (cont'd)



(c) Voltage gain vs. M at n=2 for current-fed topologies



(d) Current stress vs. voltage gain at n=2 for current-fed topologies

The comparison between voltage-fed switched-coupled-inductor inverter and voltage-fed Z/quasi-Z-source inverter are shown in Figure 3.19. The comparison target is the voltage stress over voltage gain ratio at the same voltage gain. Among the buck-boost inverter topologies, voltage-fed Z/quasi-Z-source inverter has been found a good topology that has low cost, high reliability and low voltage stress. Thus the comparison has been made

between voltage-fed switched-coupled-inductor inverter 5 and voltage-fed Z/quasi-Z-source inverter. Their voltage stress versus voltage gain are shown in Figure 3.19. It can be seen that at the same voltage gain above 1, the proposed topology has lower voltage stress, which can bring lower cost and higher efficiency.

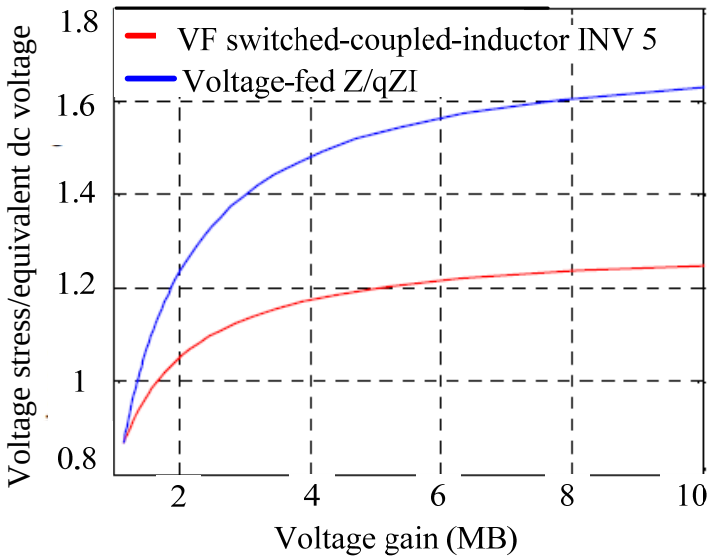


Figure 3.19. Voltage stress vs. voltage gain at n=0.5 for both voltage-fed switched-coupled-inductor inverter and voltage-fed Z/quasi-Z-source inverter

Comparison of voltage gain has been conducted between current-fed switched-coupled-inductor inverter and current-fed quasi-Z-source inverter, as shown in Figure 3.20. Recently published current-fed quasi-Z-source inverter also has similar voltage buck-boost function as the proposed current-fed SCII. By using active switch in front, both topologies have no upper limitation for the voltage gain. However, in terms of active switch current stress, the proposed topology has the same current stress as the current-fed qZSI in boost mode, but lower current stress in buck motoring mode and regeneration mode. The reason is for the two mentioned modes, at the same voltage gain, the current-fed SCII is

possible to use bigger modulation index, which brings smaller open zero duty cycle. According to equations in Table 3-3, lower active switch current stress can be obtain by decreasing the open zero duty ratio. In summary, compared to current-fed quasi-Z-source inverter, the current-fed switched-coupled-inductor inverter is more compact due to its capacitor-less feature, and has lower switch current stress at buck motoring and regenerative mode.

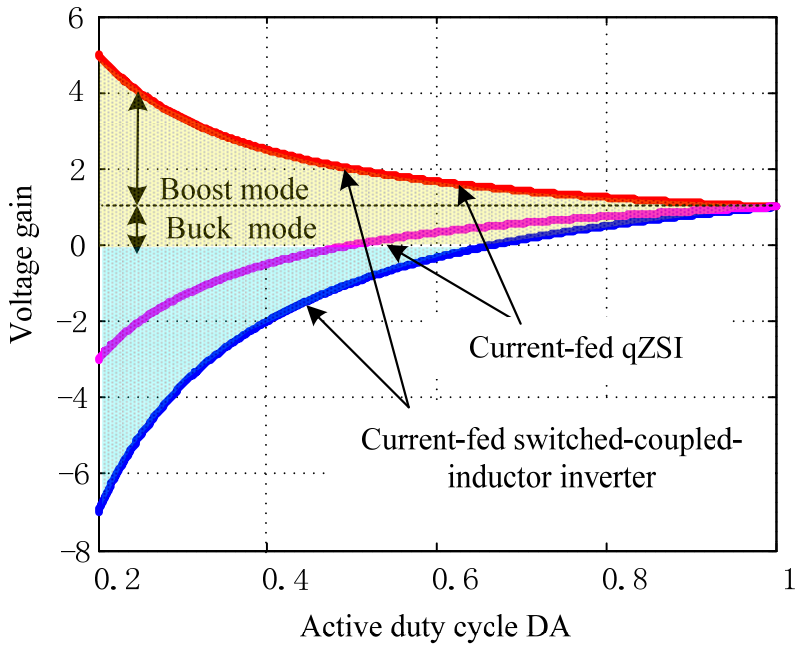


Figure 3.20. Voltage boost ratio B versus active duty cycle D_A *(0.866M)* for current-fed qZSI and current-fed switched-coupled-inductor inverter

3.5. Direct Z-source matrix converter

A family of direct Z-source matrix converter (MC) is shown in Figure 2.12. For voltage-fed (VF) Z-source MC, its voltage gain can only reach 1.15, and also the phase shift caused by the Z-network makes the control not accurate. But for voltage-fed quasi-z-source matrix converter, there is no upper and lower limit for voltage gain, and in addition, the phase shift at two sides of quasi-Z-network is equal to zero, which can cause much less error in the

control. One of the quasi-Z MC topologies has continuous input current, which is beneficial to the input voltage source. Compared to traditional MC, voltage-fed Z-source and quasi-Z-source matrix converter both can boost voltage higher than 0.866. The boost ratio depends on the duty cycle of extra shoot through state, which has constrain that it is complementary with active state duty cycle. Z-source topology has lower voltage gain range than quasi-Z-source topology. Also the quasi-Z-source topology can conduct less voltage/current stress on the switch and passives, less input and output harmonics and higher power factor than Z-source matrix converter. In another word, compared to Z-source topology, quasi-Z-source matrix converter is a component less, size compact, high efficient, wide range buck-boost matrix converter. The boost ratio is derived for both topologies as follows.

3.5.1. Voltage-fed Z-source matrix converter

Compared to matrix converter in circuit structure, Z-source matrix converter has extra L-C network and three switches in the input side. Compared to matrix converter in circuit states, the Z-source matrix converter has an extra shoot through state except the traditional 27 switching states of matrix converter. Figure 3.22 (a) and (b) show the two equivalent circuit states. In the shoot through state, the three switches on the same column, or two columns or all three columns will short together. At the same time, the front three switches are controlled to be open. In non-shoot through state, the front switches are turned on, and matrix converter part works like traditional case.

The introduction of Z-source network into the conventional matrix converter is equivalent to cascade a boost converter in the front stage. The boost ratio of Z-source network can be derived by applying the volt-seconds balance on the Z-source inductors in the

state average model of the equivalent simplified ZS matrix converter [28].

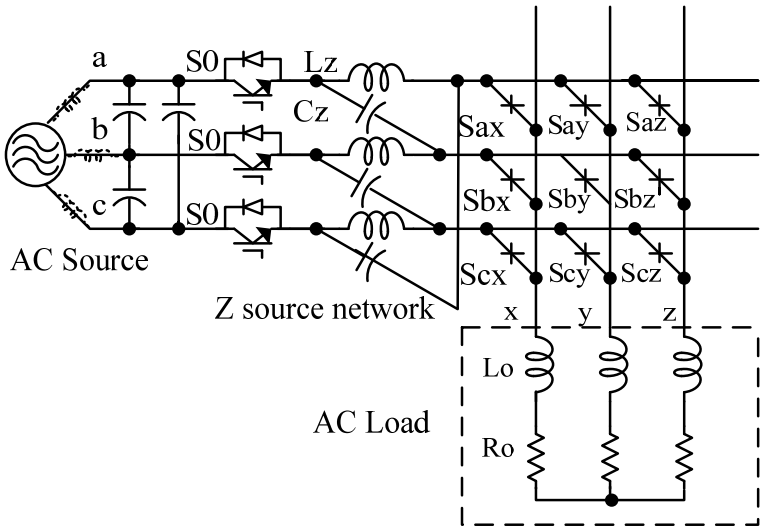
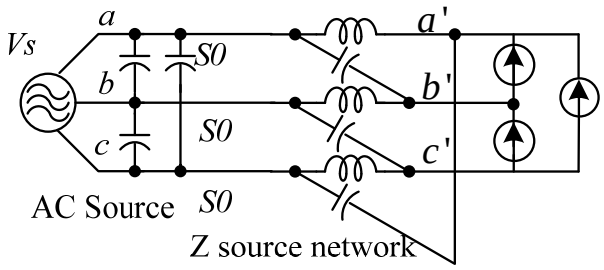
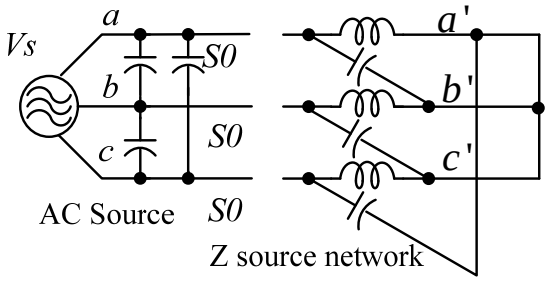


Figure 3.21. Voltage-fed Z-source matrix converter



(a) I: active state



(b).II: shoot through state

Figure 3.22. Equivalent circuit states of Z-source matrix converter

For one switching cycle, T_c, assuming the interval of shoot-through state is T_0; and the total interval of non-shoot-through states is T_1; thus $T_c=T_0+T_1$ and the shoot-through duty ratio, $D=T_0/T_c$. From Figure 3.22 (a), during the interval of non-shoot-through states, T_1, one

has the following voltage equations:

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} v_{C1} \\ v_{C2} \\ v_{C3} \end{bmatrix} - \begin{bmatrix} v_{L2} \\ v_{L3} \\ v_{L1} \end{bmatrix} \tag{3.48}$$

$$\begin{bmatrix} v_{a'b'} \\ v_{b'c'} \\ v_{c'a'} \end{bmatrix} = \begin{bmatrix} v_{C1} \\ v_{C2} \\ v_{C3} \end{bmatrix} - \begin{bmatrix} v_{L1} \\ v_{L2} \\ v_{L3} \end{bmatrix} \tag{3.49}$$

, where v_{L1}, v_{L2} and v_{L3} are the voltages across the inductors L_1, L_2, and L_3, respectively; v_{C1} , v_{C2} and v_{C3} are the voltages across the capacitors C_1, C_2, and C_3 , respectively. v_{ab} ,v_{bc} , and v_{ca} are the line-to-line voltages of the source and $v_{a'b'}$, $v_{b'c'}$, and $v_{c'a'}$ are the line-to-line voltages across the MC bridge.

From Figure 3.22 (b), during the interval of the shoot-through states, T_0, one can get

$$\begin{bmatrix} v_{C1} \\ v_{C2} \\ v_{C3} \end{bmatrix} = \begin{bmatrix} v_{L1} \\ v_{L2} \\ v_{L3} \end{bmatrix} \tag{3.50}$$

In steady state, the average voltage of the inductors over one switching cycle should be zero, neglecting fundamental voltage drop and assuming the switching frequency is far greater than the fundamental frequency. From (3.48) and (3.50), one has

$$\begin{aligned} Dv_{C1} + (1-D)(v_{C3} - v_{ca}) &= 0 \\ Dv_{C2} + (1-D)(v_{C1} - v_{ab}) &= 0 \\ Dv_{C3} + (1-D)(v_{C2} - v_{bc}) &= 0 \end{aligned} \tag{3.51}$$

From (3.49) and (3.50), one has

$$\begin{aligned} v_{C1} &= (1-D)v_{a'b'} \\ v_{C2} &= (1-D)v_{b'c'} \\ v_{C3} &= (1-D)v_{c'a'} \end{aligned} \tag{3.52}$$

Assume that the source is a three-phase symmetric system, namely

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = V_i \begin{bmatrix} \sin \omega t \\ \sin(\omega t - 120^\circ) \\ \sin(\omega t + 120^\circ) \end{bmatrix} \tag{3.53}$$

, where V_i and ω are the voltage amplitude and angular frequency of the source. Assume the voltages across the capacitors have a phase difference ϕ_C in reference to the source, i.e.,

$$\begin{bmatrix} v_{C1} \\ v_{C2} \\ v_{C3} \end{bmatrix} = V_C \begin{bmatrix} \sin(\omega t + \phi_C) \\ \sin(\omega t + \phi_C - 120^\circ) \\ \sin(\omega t + \phi_C + 120^\circ) \end{bmatrix} \tag{3.54}$$

, where V_C is the amplitude of capacitor voltages. Assume the voltage across the MC bridge has a phase difference ϕ_m referred to the source, thus

$$\begin{bmatrix} v_{a'b'} \\ v_{b'c'} \\ v_{c'a'} \end{bmatrix} = V_m \begin{bmatrix} \sin(\omega t + \phi_m) \\ \sin(\omega t + \phi_m - 120^\circ) \\ \sin(\omega t + \phi_m + 120^\circ) \end{bmatrix} \tag{3.55}$$

, where V_m is the output voltage amplitude of Z-source network. From (3.51), (3.52), (3.53) and (3.54), we have

$$V_C \begin{bmatrix} D\sin(\omega t + \phi_C) + (1-D)\sin(\omega t + \phi_C + 120^\circ) \\ D\sin(\omega t + \phi_C - 120^\circ) + (1-D)\sin(\omega t + \phi_C) \\ D\sin(\omega t + \phi_C + 120^\circ) + (1-D)\sin(\omega t + \phi_C - 120^\circ) \end{bmatrix} = (1-D)V_i \begin{bmatrix} \sin(\omega t + 120^\circ) \\ \sin \omega t \\ \sin(\omega t - 120^\circ) \end{bmatrix} \tag{3.56}$$

Applying trigonometric functions, such as $\sin^2\omega t + \sin^2(\omega t\text{-}120°) + \sin^2(\omega t\text{+}120°) = 1.5$, to (3.56), the relationship between the capacitor and source voltage amplitudes can be derived:

$$\frac{V_C}{V_i} = \frac{1-D}{\sqrt{3D^2 - 3D + 1}} \tag{3.57}$$

So the boost ratio between V_m' and V_m can be obtained:

$$B = \frac{V_m'}{V_m} = \frac{1}{\sqrt{3{D_0}^2 - 3D_0 + 1}} \tag{3.58}$$

At the same time, the phase shift between source voltage V_{abc} and terminal voltage

$V_{a'b'c'}$ can be derived as:

$$\phi_Z = \arcsin \frac{\sqrt{3}D_0}{2\sqrt{3D_0{}^2 - 3D_0 + 1}} \tag{3.59}$$

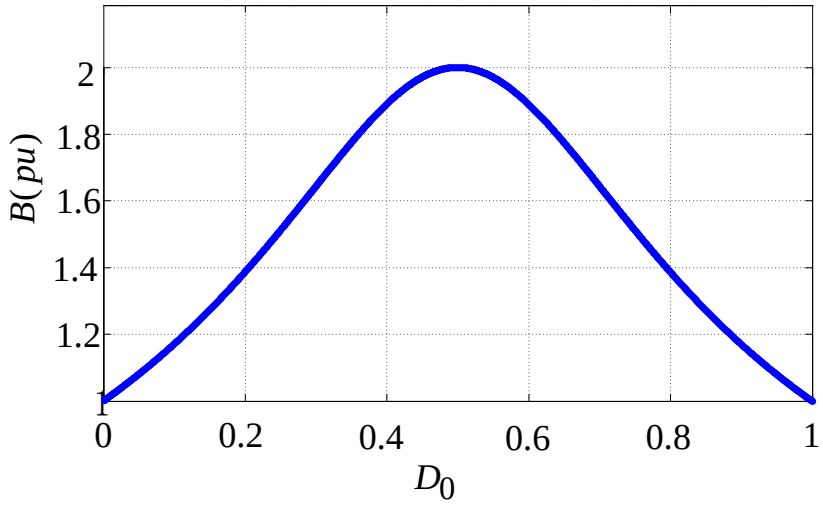


Figure 3.23.Voltage boost ratio B vs D_0 for Z-source matrix converter (MC)

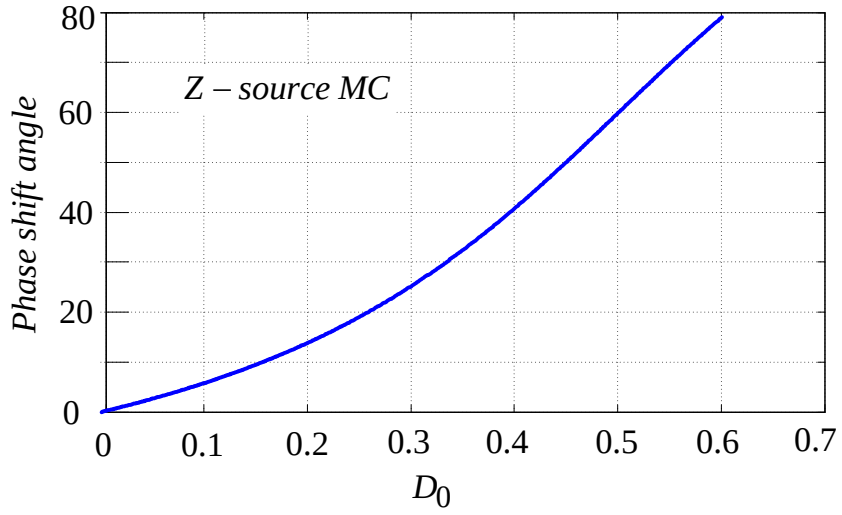


Figure 3.24.Phase angle between $V_{a,b,c}$ and $V_{a',b',c'}$ for Z-source MC

The maximum boost ratio 2 happens at $D_0 = 0.5$, as shown in Figure 3.23. Similarly to Z-source inverter, the voltage conversion ratio between output line voltage amplitude V_{om} and input V_m is:

$$G = \frac{V_{om}}{V_m} = MB = \frac{M}{\sqrt{3D_0{}^2 - 3D_0 + 1}} \tag{3.60}$$

The phase shift between two voltage is a monotonic function of open zero duty cycle, as shown in Figure 3.24. The larger the D_0, the bigger the phase shift angle. This issue only happens at the topology in Figure 3.21 due to its twist structure of the Z-network. It is a disadvantage of this topology, because if the source voltage is taken as the reference waveform in generating the control PWM signal, this phase shift will cause the phase inaccuracy of the control signal. Of course, the terminal voltage can be taken as the reference waveform instead, however, this waveform is a discontinuous PWM type, which is hard to be used. Adding a low pass filter to purify the PWM waveform can create a smooth reference curve, but the filter itself also introduces a phase shift. This problem doesn't exist in quasi-Z-source matrix converter topology, due to its phase-decoupled quasi-z-network structure.

3.5.2. Voltage-fed quasi-Z-source matrix converter

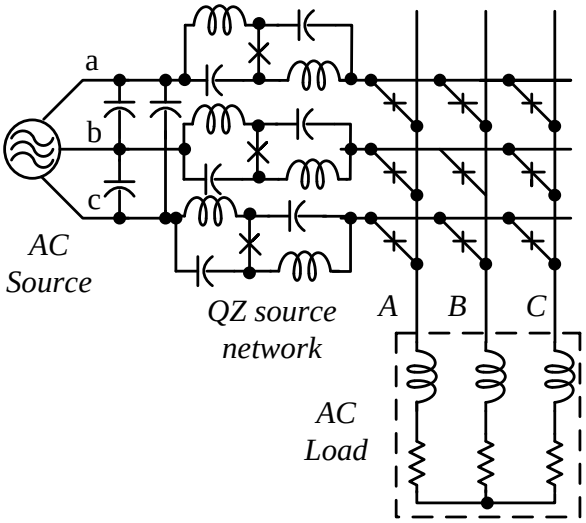
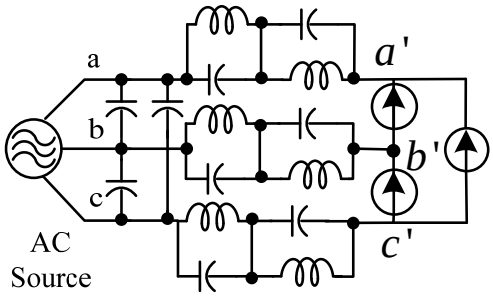
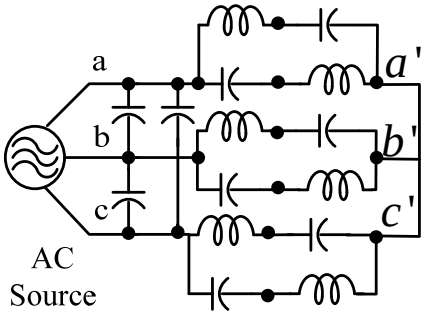


Figure 3.25. Voltage-fed quasi-Z-source inverter



(a) I: active state



(b).II: shoot through state

Figure 3.26. Equivalent circuit states for qZ-source MC

As another example, the voltage-fed qZS-MC is deduced to compare its voltage gain with the simplified voltage-fed ZS-MC. During the interval of the shoot-through states, T_0, the voltage-fed qZS-MC has equivalent circuits as shown in Figure 3.26 (b), and one can get

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} v_{Ca1} \\ v_{Cb1} \\ v_{Cc1} \end{bmatrix} + \begin{bmatrix} v_{La2} \\ v_{Lb2} \\ v_{Lc2} \end{bmatrix} - \begin{bmatrix} v_{Lb1} \\ v_{Lc1} \\ v_{La1} \end{bmatrix} - \begin{bmatrix} v_{Cb2} \\ v_{Cc2} \\ v_{Ca2} \end{bmatrix} \tag{3.61}$$

$$\begin{bmatrix} v_{Ca1} \\ v_{Cb1} \\ v_{Cc1} \end{bmatrix} + \begin{bmatrix} v_{La2} \\ v_{Lb2} \\ v_{Lc2} \end{bmatrix} = \begin{bmatrix} v_{La1} \\ v_{Lb1} \\ v_{Lc1} \end{bmatrix} + \begin{bmatrix} v_{Ca2} \\ v_{Cb2} \\ v_{Cc2} \end{bmatrix} \tag{3.62}$$

, where v denotes the voltage, and the subscript C_{x1} and C_{x2} are capacitors 1 and 2 of phase-x (x=a, b, c); L_{x1} and L_{x2} for inductors 1 and 2 of phase-x.

During the interval of the non-shoot-through states, T_1, its equivalent circuits is shown in Figure 3.26 (a), and one can get

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} v_{Ca1} \\ v_{Cb1} \\ v_{Cc1} \end{bmatrix} + \begin{bmatrix} v_{Ca2} \\ v_{Cb2} \\ v_{Cc2} \end{bmatrix} + \begin{bmatrix} v_{a'b'} \\ v_{b'c'} \\ v_{c'a'} \end{bmatrix} - \begin{bmatrix} v_{Cb1} \\ v_{Cc1} \\ v_{Ca1} \end{bmatrix} - \begin{bmatrix} v_{Cb2} \\ v_{Cc2} \\ v_{Ca2} \end{bmatrix} \tag{3.63}$$

$$\begin{bmatrix} v_{Ca1} \\ v_{Cb1} \\ v_{Cc1} \end{bmatrix} = \begin{bmatrix} v_{La1} \\ v_{Lb1} \\ v_{Lc1} \end{bmatrix} \tag{3.64}$$

$$\begin{bmatrix} v_{La2} \\ v_{Lb2} \\ v_{Lc2} \end{bmatrix} = \begin{bmatrix} v_{Ca2} \\ v_{Cb2} \\ v_{Cc2} \end{bmatrix} \tag{3.65}$$

Due to symmetry of quasi-Z network, there are

$$\begin{bmatrix} v_{La2} \\ v_{Lb2} \\ v_{Lc2} \end{bmatrix} = \begin{bmatrix} v_{La1} \\ v_{Lb1} \\ v_{Lc1} \end{bmatrix}, \begin{bmatrix} v_{Ca1} \\ v_{Cb1} \\ v_{Cc1} \end{bmatrix} = \begin{bmatrix} v_{Ca2} \\ v_{Cb2} \\ v_{Cc2} \end{bmatrix} \tag{3.66}$$

In steady state, the average voltage of the inductors over one switching cycle should be zero, and (3.67) can be derived from (3.61), (3.64), and (3.66).

$$\begin{bmatrix} v_{Cb1} \\ v_{Cc1} \\ v_{Ca1} \end{bmatrix} - \begin{bmatrix} v_{Ca1} \\ v_{Cb1} \\ v_{Cc1} \end{bmatrix} = \frac{D_0}{1-2D_0} \begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} \tag{3.67}$$

Due to symmetric voltages of three-phase capacitors, (3.67) becomes

$$\begin{bmatrix} v_{Ca1} \\ v_{Cb1} \\ v_{Cc1} \end{bmatrix} = \frac{D_0}{6D_0-3} \begin{bmatrix} v_{ab}-v_{ca} \\ v_{bc}-v_{ab} \\ v_{ca}-v_{bc} \end{bmatrix} \tag{3.68}$$

Combining (3.63) in (3.68), there is

$$\begin{bmatrix} v_{a'b'} \\ v_{b'c'} \\ v_{c'a'} \end{bmatrix} = \frac{1}{1-2D_0} \begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} \tag{3.69}$$

Similar to the process used for the simplified voltage-fed ZS-MC, the boost factor of the voltage-fed qZS-MC can be expressed as

$$B = \frac{V_m}{V_i} = \frac{1}{1-2D_0} \tag{3.70}$$

From (3.68), the capacitor voltage amplitude is

$$V_C = \frac{D_0}{1-2D_0} V_i \tag{3.71}$$

The phase shift between source and terminal voltage is: $\phi_Z = 0$

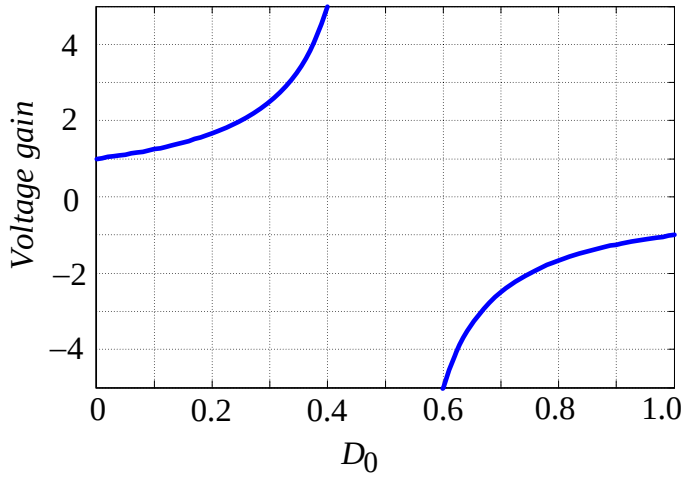


Figure 3.27.Voltage boost ratio B vs D_0 of voltage-fed quasi-Z-source matrix converter

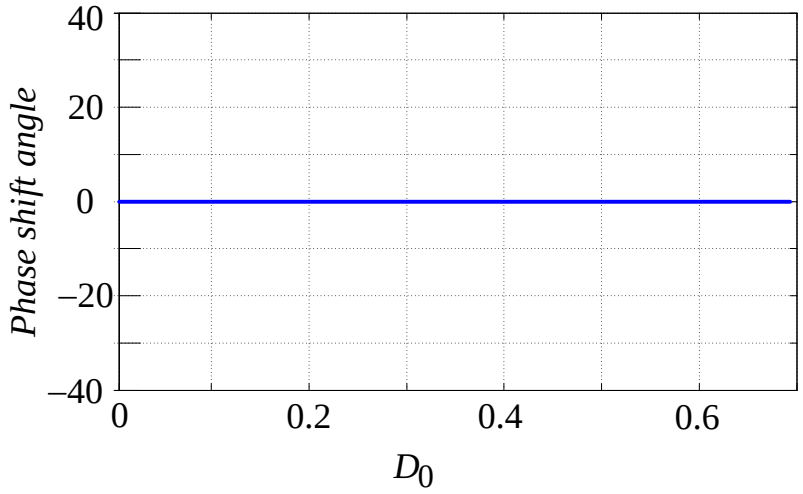


Figure 3.28.Phase angle between $V_{a,b,c}$ and $V_{a',b',c'}$ for qZ-source MC

The voltage boost ratio is plot as a function of D_0 in Figure 3.27. This boost ratio is similar to the boost gain in quasi-Z-source VSI and quasi-Z-source dc/dc converter. The advantage of this topology is that there is no upper limit on the voltage boost ratio, thus it can bring the voltage much higher than Z-source MC topology.

The phase shift between input source and the voltage at the terminals of matrix converter

is equal to zero, which is derived from equations, as shown in Figure 3.28. This is due to the decoupled quasi-Z-source network in qZ-source MC. There is no coupling between different phases. Also the small ac capacitor and inductor will not cause a big phase difference. This zero phase shift feature significantly reduces the control error. Thus the input current harmonics and output current harmonics are also minimized.

3.6. Summary

In summary, the current-fed qZSI has the following advantages:

1) The current-fed qZSI can buck-boost voltage and achieve bidirectional power flow with a single stage configuration.

2) In motoring operation (power flows from dc source to ac side), the current-fed qZSI can work in region B as shown in Figure 3.5. The equivalent output voltage $V_{out} = 0 \sim 2V_{in}$.

3) In energy regeneration operation (power flows from ac source to dc side), the current-fed qZSI can work in region C as shown in Figure 3.5, which can produce dc voltage from 0 ~ infinite theoretically.

4) By replacing the diode with a RB-IGBT, region A is also available for motoring operation which means the current-fed qZSI can completely overcome the voltage limitation and output any desired voltage theoretically in either motoring operation or energy regeneration operation. Because of the above advantages, the current-fed qZSI can be easily applied to HEVs and general purpose variable speed motor drives. Applying the current-fed qZSI in the HEVs as shown in Figure 3.1, both motor drive and the control of state of charge (SOC) of the battery can be implemented in a single stage configuration, which is less complex, more reliable and more cost effective when compared to conventional

two-stage configuration (i.e a bidirectional dc-dc converter combined with a VSI).

In summary, the current-fed Z-source PWM rectifier has the following advantages:

1) It can buck/boost voltage which provides a wide range of output voltage as shown in Figure 3.9;

2) The bidirectional power flow can be achieved without replacing the diode with a bidirectional conducting, unidirectional blocking switch.

3) The current gain has a wide range from 1 to minus infinity theoretically.

4) The voltage gain can be varied by adjusting two independent degrees of control freedom, the duty ratios of active state and open zero state. The current gain can be varied by adjusting duty ratio of open zero state.

In summary, for the proposed new family of buck-boost inverter topologies: voltage/current-fed switched-coupled-inductor inverter (SCII). The following features have been demonstrated by circuit fundamentals analysis and simulations:

(1) At the correct selection of trans-ratio n and extra switching state duty cycle, both voltage/current-fed topologies have candidates that can buck-boost voltage.

(1) Voltage-fed SCII has only half number of passive components compared to Z-source inverter, but higher voltage boost ratio and lower active switch voltage stress.

(2) Voltage-fed SCII has less active switch, smaller size and higher reliability than two stage boost-converter-inverter.

(3) Current-fed SCII is a capacitor-less solution, which is much more compact than the ones with capacitors (boost-converter-inverter and Z-source inverter)

(4) Current-fed SCII has lower active switch current stress than current-fed Z/quasi-Z-source

inverter at the same voltage gain, in buck motoring and regeneration mode.

(5) With active front switch, both voltage and current-fed SCII can have regenerative capability.

Due to the benefits, this voltage-fed switched-coupled-inductor inverter is beneficial to be used in the dc-ac applications that demand a high voltage gain from a very low voltage dc source, such as the micro-inverter in photovoltaic, or G/M in HEV. The current-fed switched-coupled-inductor inverter is potential candidate for compact, regenerative, high temperature, high efficiency, low cost HEV/EV motor drive or engine starter.

In summary for Z-source matrix converters, with only three additional switches, it can have the buck-boost function, which can reduce cost and increase reliability for those applications that have a requirement for wide input and output voltage ranges.

All those features of each topology has been demonstrated by simulations and experiments in later chapters based on the modulation method proposed in chapter 4, 5, 6. All the experiment results can be found in chapter 5, 6, 7, 8 and 9.

CHAPTER 4 MODULATION

4.1. Introduction

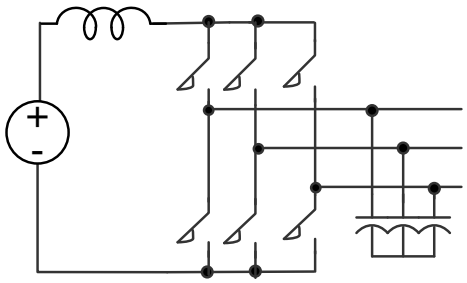
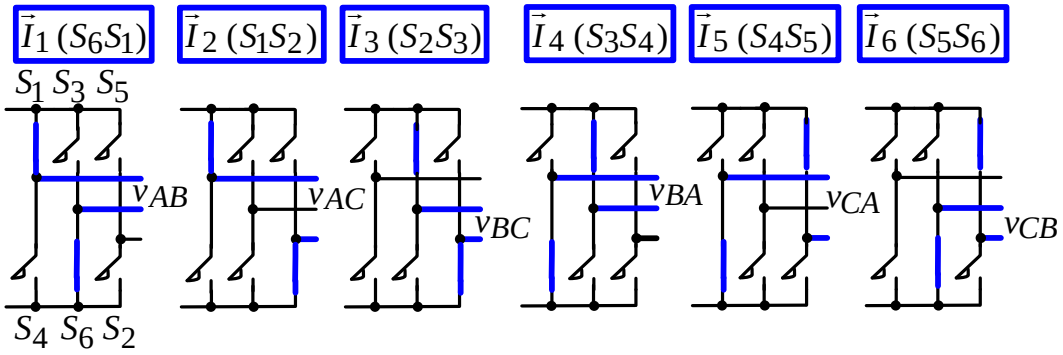
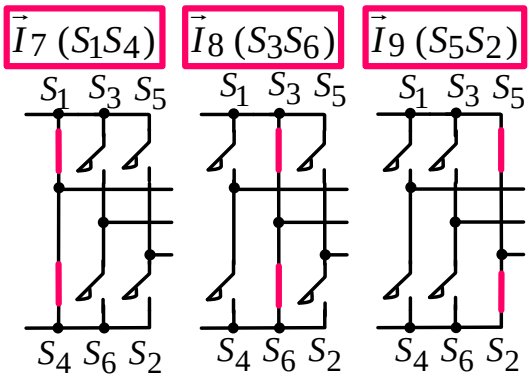


Figure 4.1. Conventional current source inverter

Conventional current source inverter is composed of input current source, six active reverse-blocking switches, and three ac capacitors which is directed connected to the output lines. Figure 4.1 shows the basic circuit configuration.



(a) Conventional six active states



(b) Conventional three zero states

Figure 4.2. Nine switching states for conventional current source inverter

It has nine switching states: six active states and three zero states. In active state, one and only one switch on upper leg, and also one and only one switch on the lower leg conduct at any time; the three switches on either half leg turn on and off complementarily with each other. The reason for this is: the output three phases are connected with capacitors, thus if any two phase legs in the same half bridge are conducting at the same time, a short circuit can form. At the same time, the input current has to have path to flow, so one phase leg in each half bridge has to be conducted.

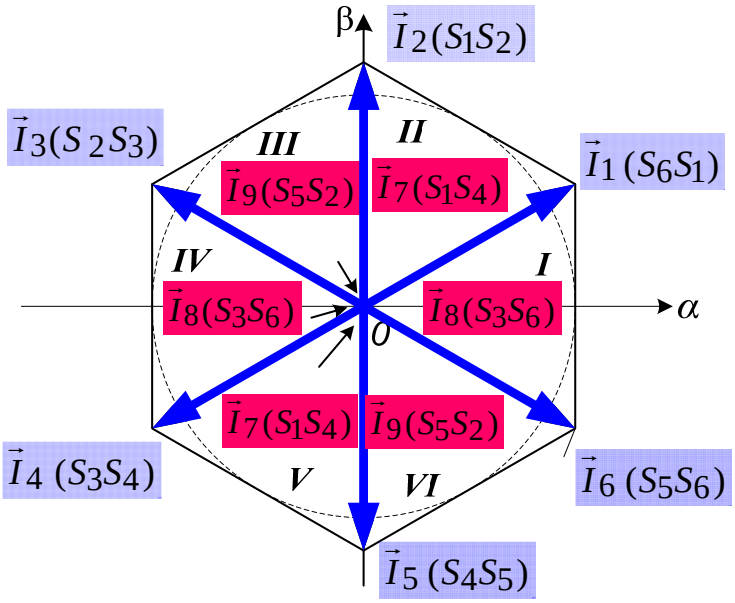


Figure 4.3 Conventional discontinuous modulation for current source inverter

This section concentrates on the modulation of current source inverter. The most common modulation method is the space vector PWM control, which use active vectors and zero vectors to synthesize the rotating current vector. The block diagram is shown in Figure 4.3. The hexagon is composed of six vectors, each of which is corresponding to one active switching state. Thus the hexagon is divided into six sectors by these vectors, and each vector occupies sixty degrees. In each sector, usually the adjacent two active vectors are selected to generate output current, in order to utilize a common switch. The selection of zero vectors is

more flexible. One, two or three zero vectors can be selected in each sector. In the assumption of the three phase balanced system, the output current synthesis equation is:

$$I_{ref}T_s = I_iT_i + I_{i+1}T_{i+1} + I_0T_0 \tag{4.1}$$

, where T_i, T_{i+1}, T_0 are the dwell times for the adjacent vectors I_i , I_{i+1} and I_0 respectively.

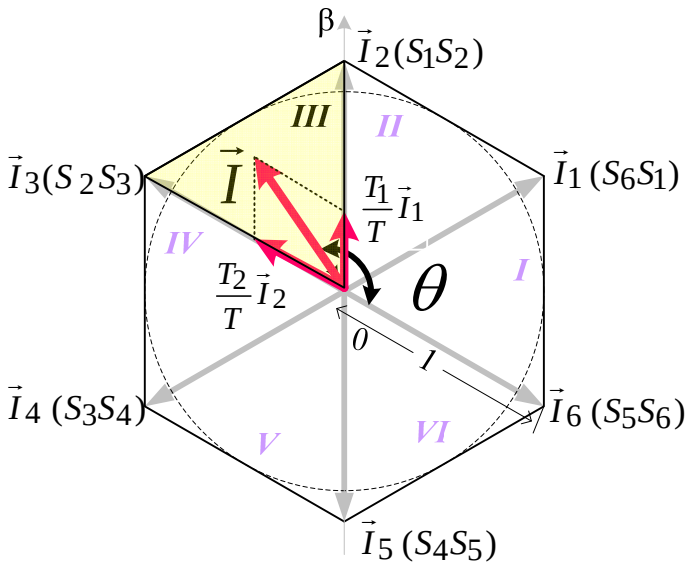


Figure 4.4. Output current vector synthesis

$$\frac{\left|\vec{I}\right|}{\sin(2\pi/3)} = \frac{T_1}{T}\frac{1}{\sin(2\pi/3-\theta)} = \frac{T_2}{T}\frac{1}{\sin(\theta-\pi/3)} \tag{4.2}$$

As shown in Figure 4.4, the synthesis process can be illustrated as follows: (1) project the output current vector into two adjacent vectors; (2) in the formed triangle, apply trigonometric theory that the division of side length to $\sin\theta$ is equal for each side; (3) express the angle in terms of current vector angle. Equation (4.1) is the resultant synthesis equation, from which, the time period for each active vector and zero vector can be derived. And their expressions are as follows:

$$T_i = \frac{\sqrt{3}}{2}m\sin(60^0-\theta)\cdot T_s;\quad T_i = \frac{\sqrt{3}}{2}m\sin(\theta)\cdot T_s;\quad T_0 = T_s - T_i - T_{i+1} - T_{op} \tag{4.3}$$

4.2. Discontinuous SVPWM and Equivalent Carrier-based modulation

4.2.1. Selection of zero vector in terms of minimum switching times

Table 4-1.Selection of vectors in each sector

Sector	Sector I	Sector II	Sector III	Sector IV	Sector V	Sector VI
Vector1	I1 (S6S1)	I2 (S1S2)	I3 (S2S3)	I4 (S3S4)	I5 (S4S5)	I6 (S5S6)
Vector2	I2 (S1S2)	I3 (S2S3)	I4 (S3S4)	I5 (S4S5)	I6 (S5S6)	I1 (S6S1)
Vector0	I7 (S1S4)	I9 (S2S5)	I8 (S3S6)	I7 (S1S4)	I9 (S2S5)	I8 (S3S6)

Table 4-2.Conduction Time for S1 and S4 in Each Sector

	Sector I	Sector II	Sector III
S1	1	$\frac{\sqrt{3}}{2}m\sin(60^0-\theta)$	0
S4	$1-\frac{\sqrt{3}}{2}m\sin(60^0-\theta)$ $-\frac{\sqrt{3}}{2}m\sin(\theta)$	0	$\frac{\sqrt{3}}{2}m\sin(\theta)$
	Sector IV	Sector V	Sector VI
S1	$1-\frac{\sqrt{3}}{2}m\sin(60^0-\theta)$ $-\frac{\sqrt{3}}{2}m\sin(\theta)$	0	$\frac{\sqrt{3}}{2}m\sin(\theta)$
S4	1	$\frac{\sqrt{3}}{2}m\sin(60^0-\theta)$	0

In every sector, except the two active vectors, there are three zero vectors for selection. In order to reduce the switching times, the zero vector with the common switch in two active vectors is selected. For example, in sector I, two active vectors are S_6S_1 and S_1S_2, in which the common switch is S_1. So the zero vector I_7 which contains S_1 is selected so that S_1 has no PWM switching in the whole 60 degree region. Similarly, each switch only does PWM

switching in every other 60 degree, as shown in Figure 4.3. The selection of vectors in each sector is shown in Table 4-1, and the resultant conduction time is in Table 4-2.

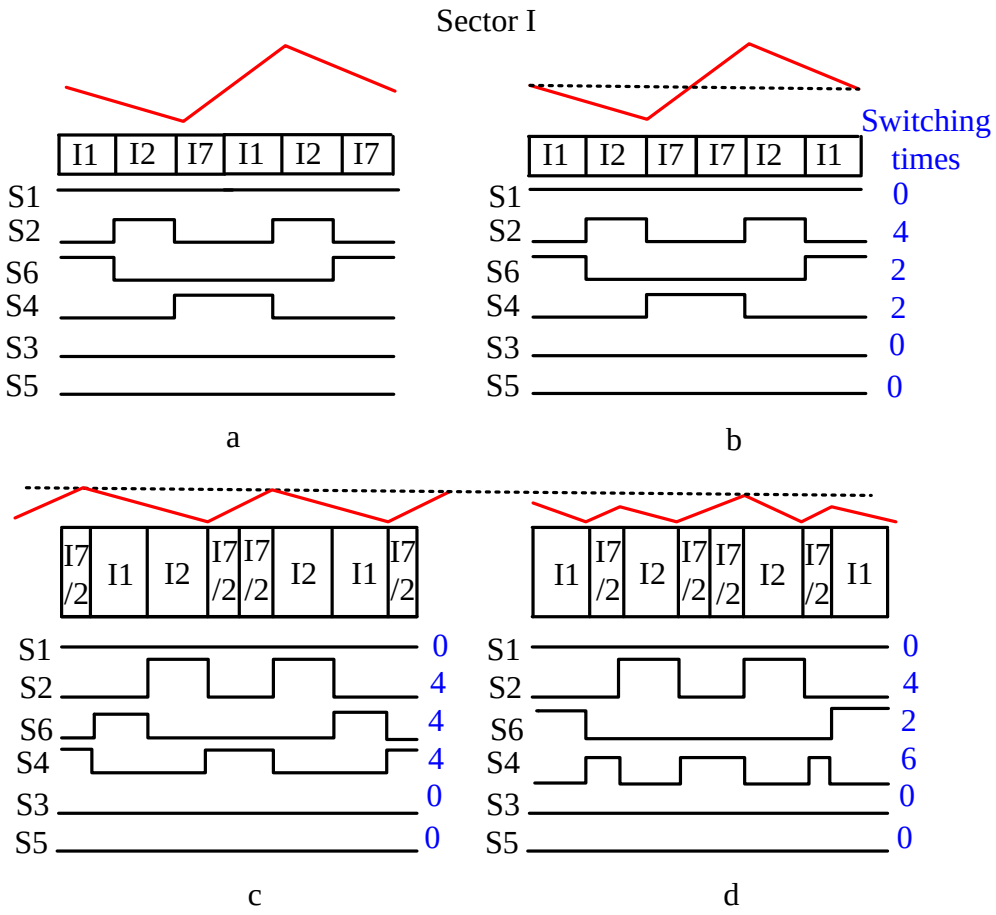


Figure 4.5. Four different switching sequences in sector I

4.2.2. Selection of switching sequence in each sector

As long as the Ampere-seconds in one switching period keeps constant, the sequences of vectors will not affect the output. However, it does affect the output THD and device switching loss. Taking sector I as an example, four switching sequences including symmetrical and unsymmetrical ones are shown in Figure 4.5.

In these sequences, type a is an unsymmetrical sequence. In order to get the same harmonic performance as the other symmetrical ones, the switching frequency has to be doubled. In this case, the benefits of less switching counts in one switching period can not be

hold.

Type b seems a good choice since the zero vector I_7 connects together, and I1 also connects together with the previous switching period, which reduces the switching counts. However, the zero vectors are all allocated in the middle, so the active vectors are pushed to the edge, not in the middle of every half switching cycle, which may increase harmonics. It can be illustrated by the input current ripple which has been shown as the red line in Figure 4.5. The input current will decrease in active state and increase in zero state. Since the zero vectors are connected together, as well as the active vectors, so the current ripple frequency is the same as switching frequency, which results in a double ripple amplitude. These low frequency and high amplitude harmonic contents are directly transferred into output current. Therefore, in the harmonics point of view, this sequence is not preferred.

Type c makes an improvement for type b in terms of harmonics, by splitting the zero states into two parts, one of which is placed in the middle, and one of which is put at the side. The input current ripple amplitude changes to half of type b, and in addition, the ripple frequency is doubled, both of which decreases the size of the passive component, as well as lower the output harmonics. This is consistent with the statement that the output harmonics can be minimized by putting the active state in the middle of half switching cycle.

Type d inserts each active state into separate zero states. The switching counts maintain the same as type b, but the ripple is unevenly distributed due to the non-middle allocation of active vectors, because of which it doesn’t have the same effect as type c in terms of harmonic reduction.

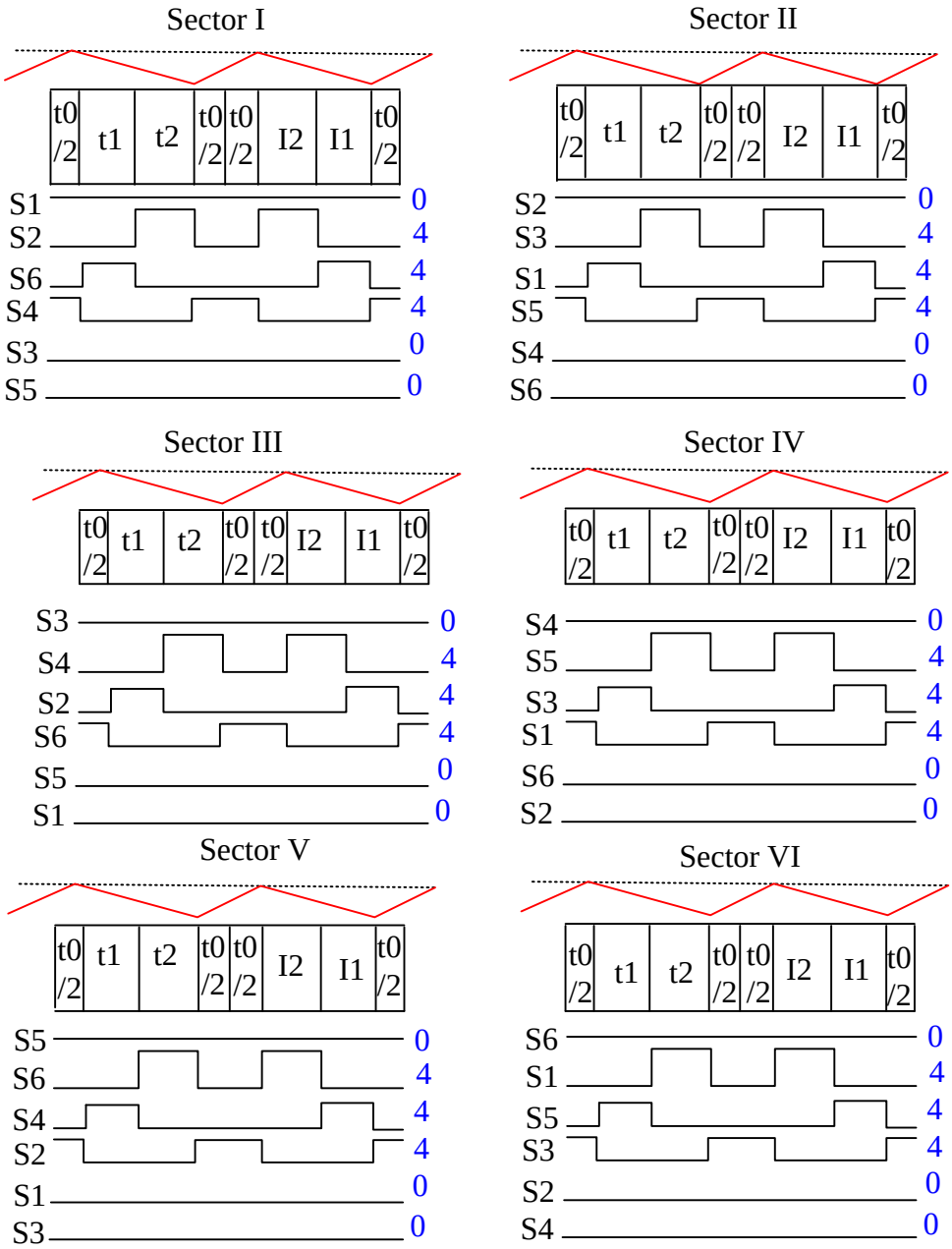


Figure 4.6. Switching state in 6 sectors for sequence c

4.2.3. Equivalent reference-carrier modulation for DPWM

In the practical implementation, the SVPWM control could be transformed into equivalent carrier based control. The reference waveform instantaneous value of the switch is proportional to the corresponding conduction time at that moment t, as shown in Figure 4.7, where one is for S_1 and one is for S_4. The switching functions generates the output current I_{ao} in the form of

$$I_{ao} = (S_1 - S_4) * I_{dc} \tag{4.4}$$

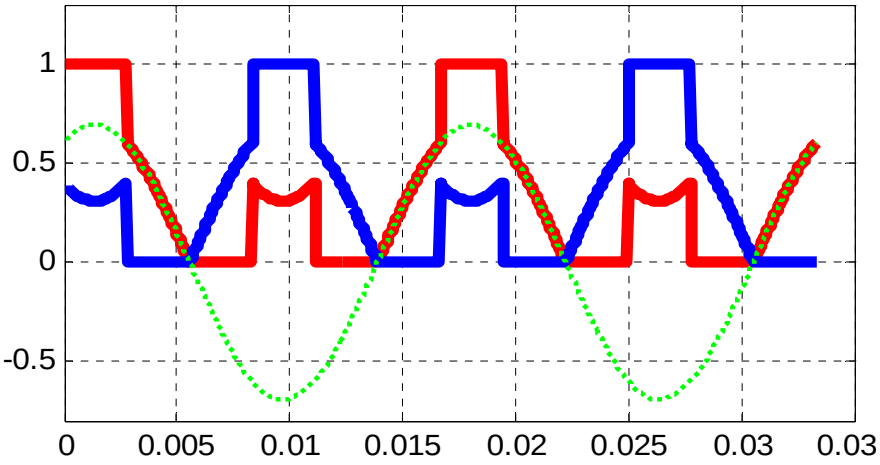
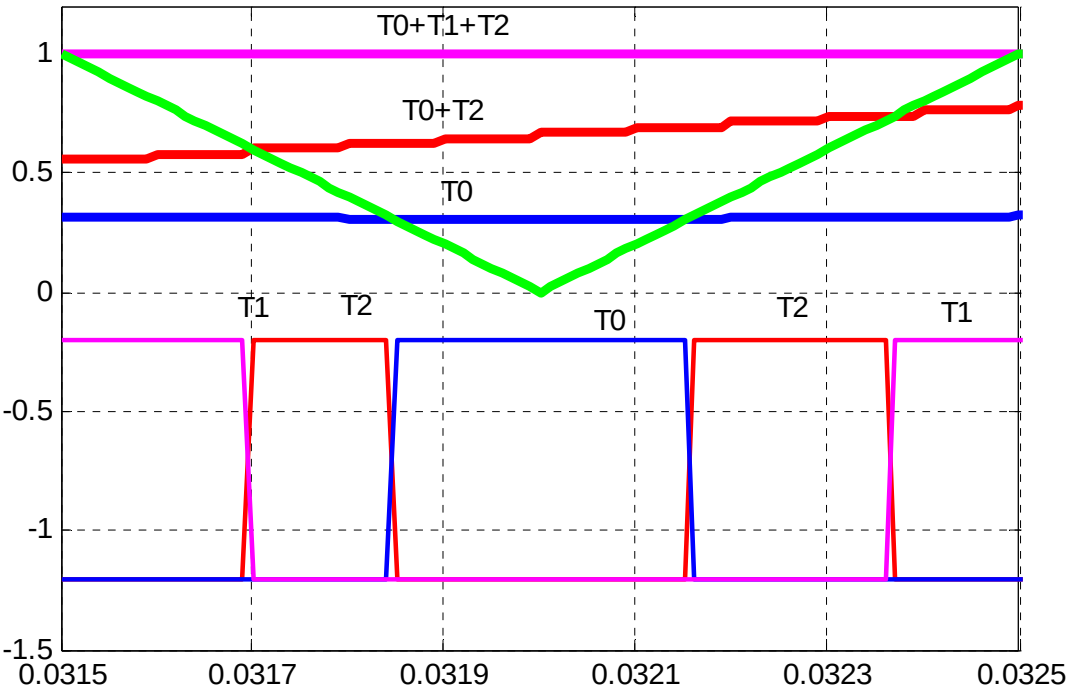


Figure 4.7. References for S1 and S4 and the output line current waveform

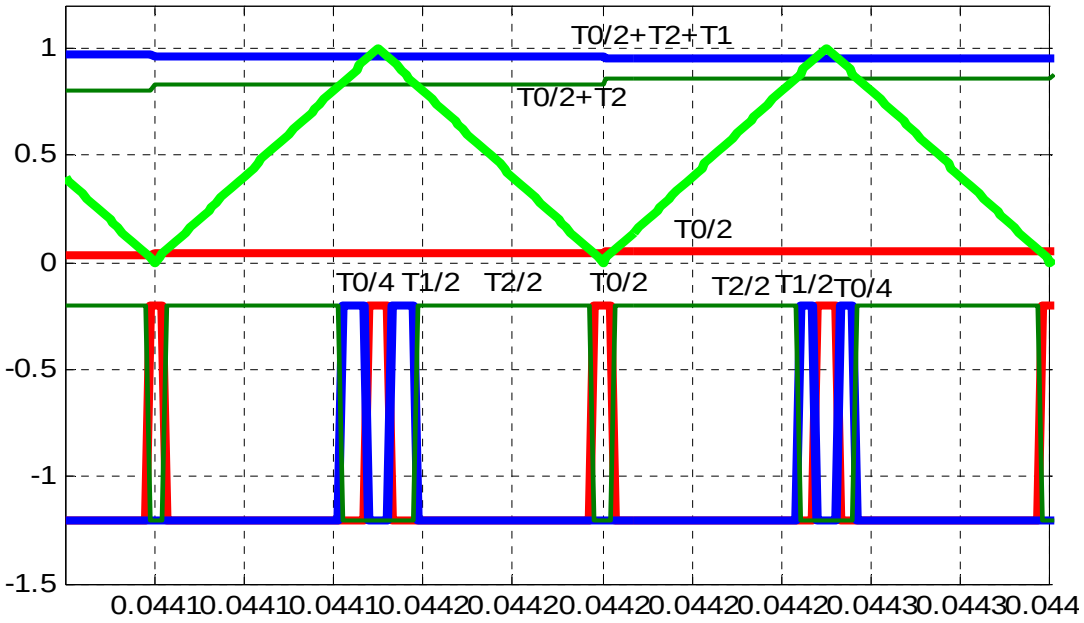
For the same output current requirement, there are infinite choices for S1 and S4. The aforementioned references definitely generate a sinusoidal waveform, as the dotted line.

However, the switching function characteristics are little bit different from the voltage source inverter modulation carrier. The upper switch and the lower switch on the same phase leg are not necessary complementary to each other, but the three switches on the same half leg must be, like S_1, S_3, S_5. Thus the PWM generated from reference waveform can not follow the rules that be positive if reference exceeds carrier, and be negative if reference is below carrier. A new group of three references have been designed to generate the correct PWM for CSI, which are proportional to (T_0), ($T_0 + T_2$) and ($T_0 + T_1 + T_2$) respectively. The switches corresponding to the turn on time T_0, T_1 and T_2 are defined as Z_0, Z_1 and Z_2 respectively. The new rule is: if the carrier is below reference T_0, Z_0 is turned on; if the carrier is between T_0 and $T_0 + T_2$, Z_2 is turned on; if the carrier is between $T_0 + T_2$ and $T_0 + T_1 + T_2$, Z_1 is turned on, just like Figure 4.8 (a). Different references and different placement sequences can be used for different switching sequence in Figure 4.5. But each

PWM



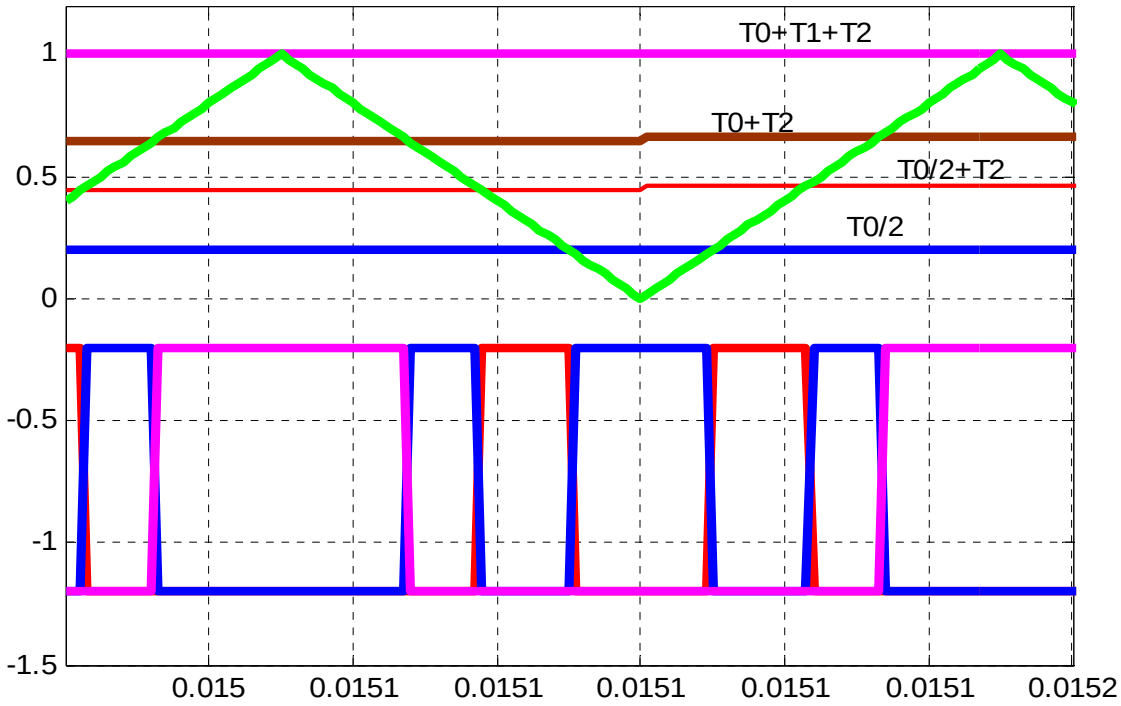
(a) Sequence b



(b) Sequence c

Figure 4.8. PWM implementation for three sequences

Figure 4.8 (cont'd)

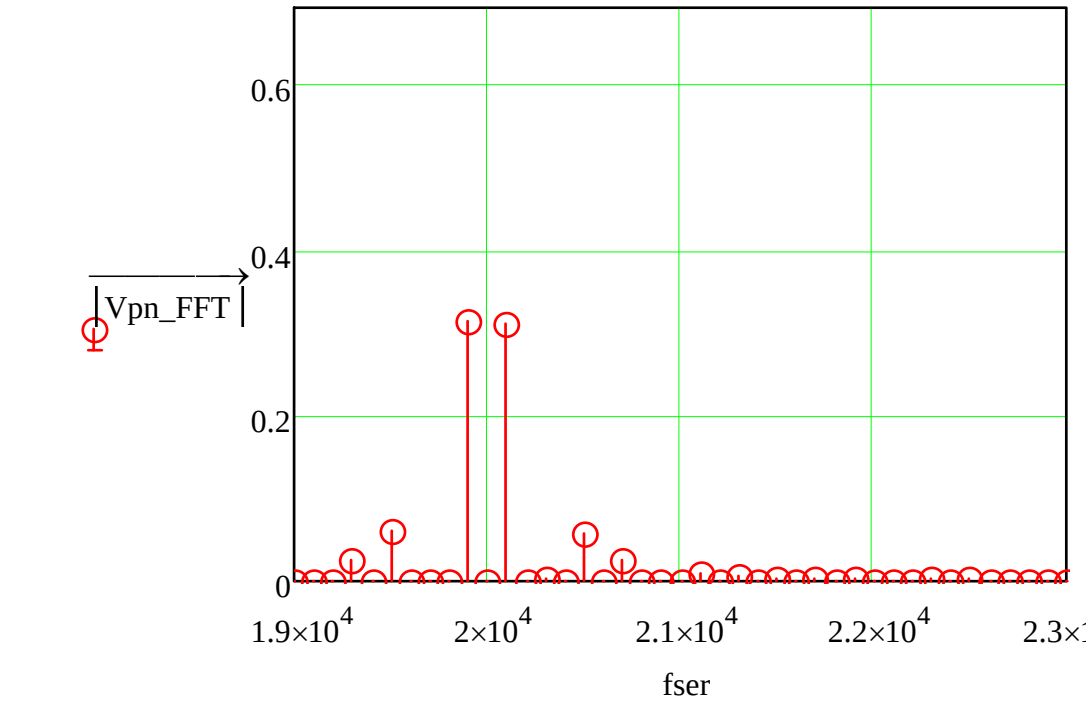


(c) Sequence d

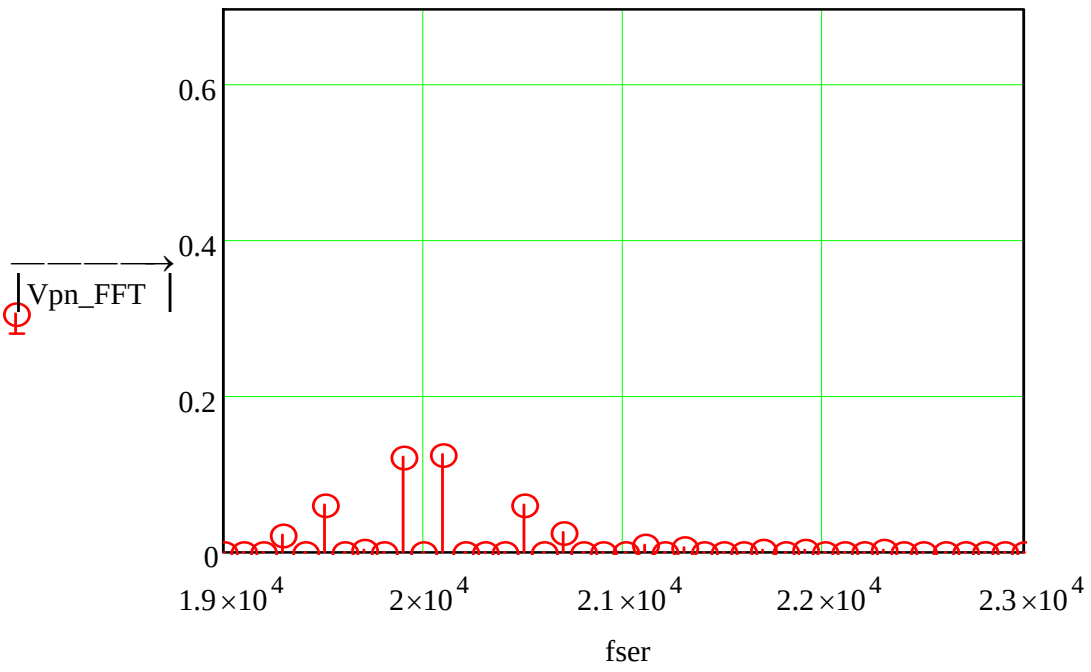
waveform is generated when the carrier is between two reference waveforms, which make the three PWM for the upper switches complementary. The implementation method for sequence b, c, d are shown in Figure 4.8.

4.2.4. Numerical Spectrum analysis

According to switching state assignment in Figure 4.4, switching time calculation from equation (4.2) and the switching waveform implementation in Figure 4.8, the numerical switching waveform in one fundamental cycle could be obtained for each DPWM sequence by using equation (4.3). Set the parameters as: M=0.8, f_o =100Hz, f_s =20kHz. The spectrum distribution diagrams of each sequence at switching frequency are shown in Figure 4.9 (a)(b)(c). The weighted THD has been used to be a criterion for evaluating the total harmonics distortion of each method. The definition of WTHD and results for each sequence



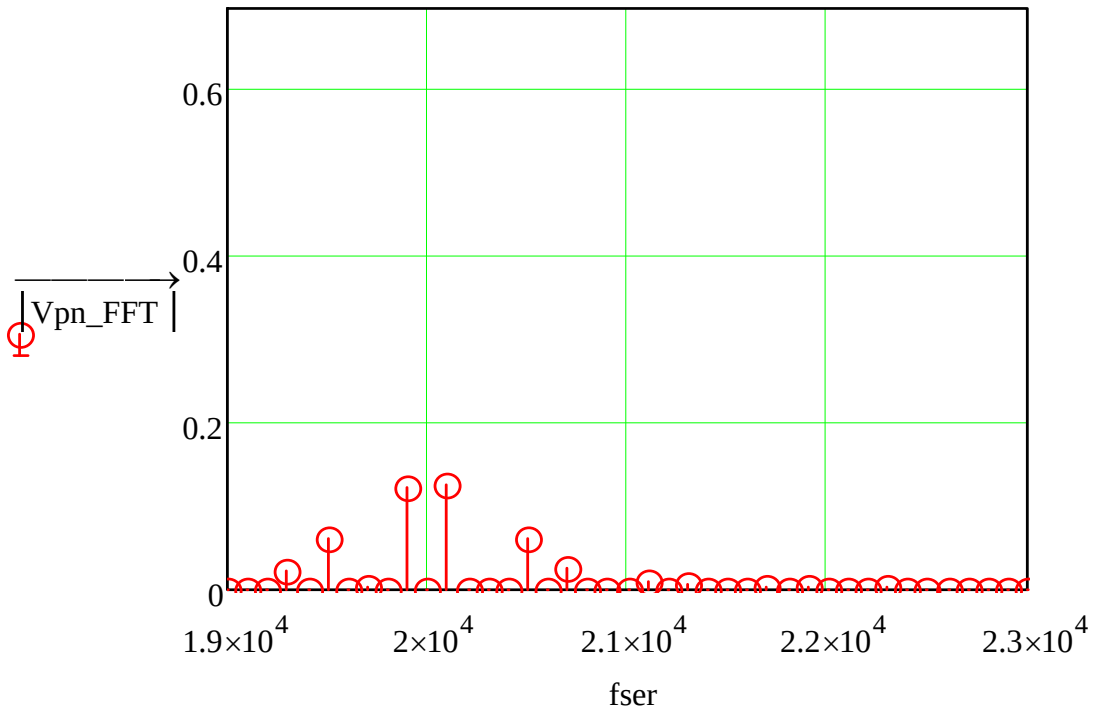
(a) Sequence b $WTHD = 3.607 * 10^{-3}$



(c) Sequence c $WTHD = 2.663 * 10^{-3}$

Figure 4.9. Numerical FFT results for b, c, d at m=0.8 for switching frequency range

Figure 4.9 (cont'd)



(c) Sequence c $WTHD = 3.306 * 10^{-3}$

are shown in the following:.

$$WTHD = \sqrt{\sum_{kk=2}^{2^{me-1}-1} \left(\frac{\left|\overrightarrow{V_{pn\_FFT\,kk}}\right|}{kk}\right)^2 / \left|\overrightarrow{V_{pn\_FFT1}}\right|} \qquad (4.5)$$

4.2.5. Analytical double Fourier analysis

Since the SVPWM has two main frequency component: one is fundamental frequency, and the other is sitching frequency, an analytical double Fourier series form could also be derived for each sequence in DPWM, according to the rising edge and falling edge time point according to the time duration for each switch at different sector in Table 4-2 and the detailed PWM arrangement in Figure 4.8. Take DPWM sequence b as an example.

The double Fourier expression for the DPWM is a sum of the integrations in six sectors since no general equation for the rising and falling edges in terms of angle in six sectors

exists, but does in one sector. Equation (4.6) gives the general double Fourier equation and Table 4-3 gives the integration upper limit and lower limit of S_1 for sequence b in each sector. However, the FFT analysis target should be the line current, which can be represented by the subtraction of upper switching function to lower switching function in the same phase leg as shown in equation (4.4), which presents as an ac symmetric waveform.

Table 4-3.Integration limit of S1 for sequence b

ys(i)	ye(i)	xr(i)	xf(i)
0	$\frac{\pi}{3}$	0	2π
$\frac{\pi}{3}$	$\frac{2\pi}{3}$	$x_{r1}=0;$ $x_{r2}=\frac{2\pi}{T_s}(T_s-\frac{T_1}{2})$ $=2\pi-\pi\cdot\frac{\sqrt{3}}{2}m\sin(\frac{2\pi}{3}-y)$	$x_{f1}=\frac{2\pi}{T_s}\frac{T_1}{2}$ $=\pi(\frac{\sqrt{3}}{2}m\sin(\frac{2}{3}\pi-y))$ $x_{f2}=2\pi$
$\frac{2\pi}{3}$	π	0	0
π	$\frac{4}{3}\pi$	$\frac{2\pi}{T_s}(\frac{T_1}{2}+\frac{T_2}{2})$ $=\pi(\frac{\sqrt{3}}{2}m\sin(y-\frac{2}{3}\pi))$	$\frac{2\pi}{T_s}(T_s-\frac{T_1}{2}-\frac{T_2}{2})$ $=2\pi-\pi\cdot\frac{\sqrt{3}}{2}m\sin(y-\frac{2}{3}\pi)$
$\frac{4}{3}\pi$	$\frac{5}{3}\pi$	0	0
$\frac{5}{3}\pi$	2π	$x_{r1}=\frac{2\pi}{T_s}\frac{T_1}{2}$ $=\pi\frac{\sqrt{3}}{2}m\sin(2\pi-y)$ $x_{r2}=\frac{2\pi}{T_s}(T_s-\frac{T_1}{2}-\frac{T_2}{2})$ $=2\pi-\pi\frac{\sqrt{3}}{2}m\sin(y-\frac{4}{3}\pi)$	$x_{f1}=\frac{2\pi}{T_s}(\frac{T_1}{2}+\frac{T_2}{2})$ $=\pi\frac{\sqrt{3}}{2}m\sin(y-\frac{4}{3}\pi)$ $x_{f2}=\frac{2\pi}{T_s}(T_s-\frac{T_1}{2})$ $=2\pi-\pi\frac{\sqrt{3}}{2}m\sin(2\pi-y)$

The coefficient of $S_1(t)$ is shown in Table 4-3. The coefficient of $S_4(t)$ is equal to the coefficient of $S_1(t)$ in the sector of 180 degree apart. Thus the phase current double Fourier

integration limit is derived and shown in Table 4-4. According to the symmetry, the integration could be conducted in the positive half cycle, two times of which is the final coefficient, as shown in equation (4.6).

$$A_{mn} + jB_{mn} = \frac{1}{2\pi^2}\sum_{1}^{6}\int_{y_s(i)}^{y_e(i)}\int_{x_r(i)}^{x_f(i)} I_{dc}e^{j(mx+ny)}dxdy \tag{4.6}$$

Table 4-4.Integration limit for Ia(t) of sequence b

i	Pulse	ys(i)	ye(i)	xr1(i)	xf1(i)	xr2(i)
1	I_{dc}	0	$\frac{\pi}{3}$	0	$\pi-\frac{T_0}{2}\cdot\frac{2\pi}{T_S}$	$\pi+\frac{T_0}{2}\cdot\frac{2\pi}{T_S}$
2	I_{dc}	$\frac{\pi}{3}$	$\frac{2\pi}{3}$	0	$\frac{2\pi}{T_s}(\frac{T_1}{2})$	$\frac{2\pi}{T_s}(T_s-\frac{T_1}{2})$
3	$-I_{dc}$	$\frac{2\pi}{3}$	π	$\frac{2\pi}{T_s}(\frac{T_1}{2})$	$\frac{2\pi}{T_s}(\frac{T_1+T_2}{2})$	$2\pi-\frac{2\pi}{T_s}(\frac{T_1+T_2}{2})$
4	$-I_{dc}$	π	$\frac{4}{3}\pi$	0	$\pi-\frac{2\pi}{T_s}(\frac{T_0}{2})$	$\pi+\frac{2\pi}{T_s}(\frac{T_0}{2})$
5	$-I_{dc}$	$\frac{4}{3}\pi$	$\frac{5}{3}\pi$	0	$\frac{2\pi}{T_s}(\frac{T_1}{2})$	$2\pi-\frac{2\pi}{T_s}(\frac{T_1}{2})$
6	I_{dc}	$\frac{5}{3}\pi$	2π	$\frac{2\pi}{T_s}(\frac{T_1}{2})$	$\frac{2\pi}{T_s}(\frac{T_1+T_2}{2})$	$2\pi-\frac{2\pi}{T_s}(\frac{T_1+T_2}{2})$

4.2.6. Simulation results

A current source inverter with the configuration of Figure 4.1 is constructed in simulation with the parameters: $V_{in}=100V, L_{in}=1mH, C_o=30uF, P_r=1kW$, $f_o=100Hz$, $f_s=20kHz$ Figure 4.10 shows the phase a current after the output capacitor for sequence b, c and d respectively. It is observed that they have the same fundamental rms value, but different switching ripple. Sequence c has lower current ripple than sequence b and d.

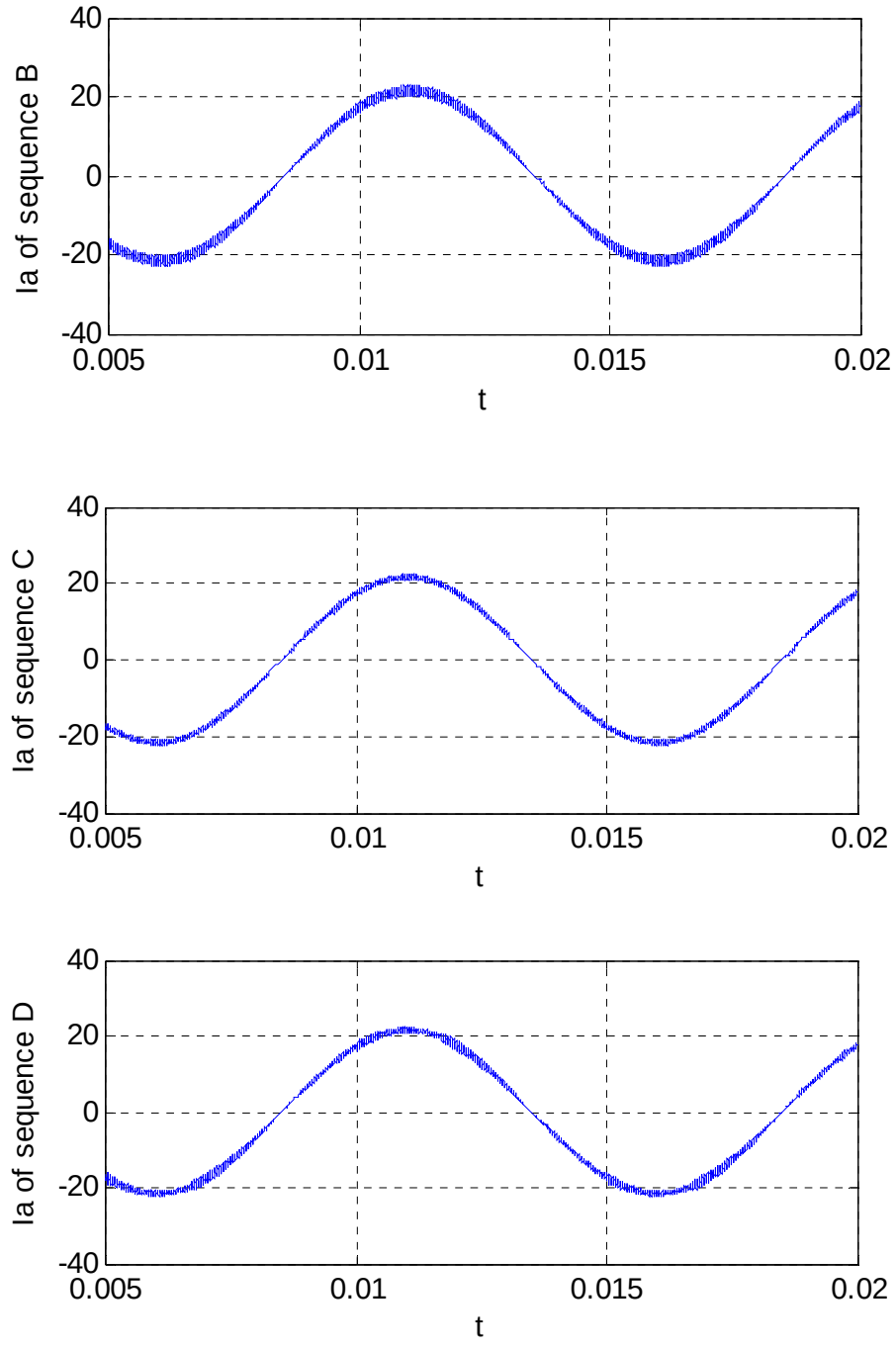


Figure 4.10. Simulated phase a current after the C filter for sequence b, c, d

4.3. Continuous SVPWM and Equivalent Carrier-based modulation

4.3.1. Selection of zero states in each sector

If the zero states I7, I8 and I9 are all used in each sector, as shown in Table 4-5, all six switches will be switching on and off in each sector. The number of switching for each switch can be derived shown in Figure 4.11. The zero state period T0 is divided into 3 equal ones

and assigned to I7, I8, I9 respectively. Figure 4.11 shows one example in Sector I. The I9 and I8 are put at sides. Thus every switch has switching action in one switching period. The switching counts for each one is shown in the figure. The total switching counts is 20 in the example, which is 2.5 times of the previous proposed discontinuous SVPWM method.

Table 4-5.Selection of vectors in each sector in Continuous SVWPM

Sector	Sector I	Sector II	Sector III	Sector IV	Sector V	Sector VI
Vector1	I1 (S6S1)	I2 (S1S2)	I3 (S2S3)	I4 (S3S4)	I5 (S4S5)	I6 (S5S6)
Vector2	I2 (S1S2)	I3 (S2S3)	I4 (S3S4)	I5 (S4S5)	I6 (S5S6)	I1 (S6S1)
Vector0	I7,I8,I9	I7,I8,I9	I7,I8,I9	I7,I8,I9	I7,I8,I9	I7,I8,I9

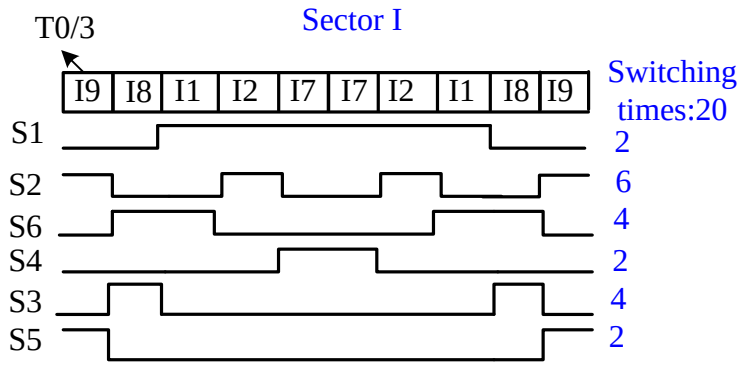


Figure 4.11. Continuous SVPWM modulation switching states in Sector I

4.3.2. Equivalent carrier-based modulation for continuous SVPWM

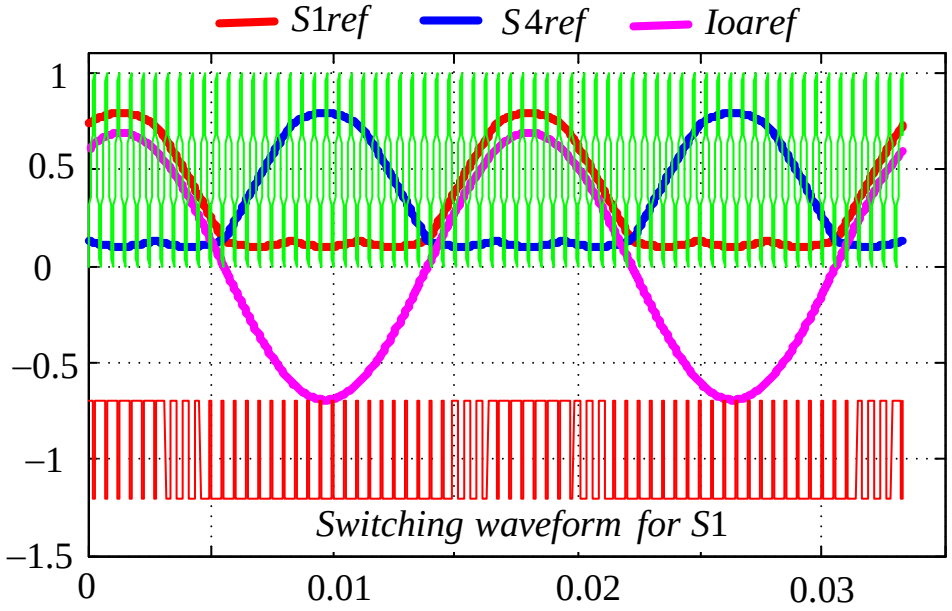


Figure 4.12. Equivalent carrier-based modulation for continuous SVPWM

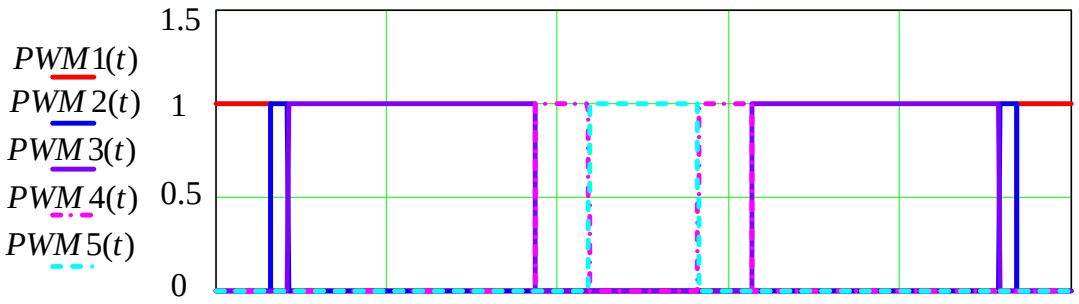


Figure 4.13 Implementation of switching waveform in Figure 4.12 by carrier-based continuous SVPWM

Similarly, the equivalent carrier based modulation for this method can be derived similarly as Table 4-2. The equivalent references for switch S1 and S4 are shown in Figure 4.12. The subtraction of S1 by S4 is the output current reference, which is a sinusoidal shown as the pink curve in Figure 4.12. Figure 4.12 also shows the switching waveform of switch S1, which is a continuous PWM as expected. Figure 4.13 shows the actual implementation process and final switching PWM in one switching cycle.

4.3.3. Sequences of vectors in each switching cycle

For the sequences of the five vectors in half switching cycle, T1,T2, T7,T8,T9, there are many choices. Also the zero state time period is not necessary evenly divided into 3 to be assigned to three zero vectors. Different portion can be assigned to different zero vectors in different sectors. The basic principle to guarantee a lower harmonic content is to put the T1 and T2 in the middle of each half switching cycle.

Compare the continuous SVPWM with the discontinuous SVPWM, it can be seen that discontinuous method has much lower switching times than the continuous one, so as the switching loss. However, in terms of spectrum, continuous SVPWM may have lower harmonics. This needs to be studied in the following.

4.3.4. Numerical FFT spectrum analysis

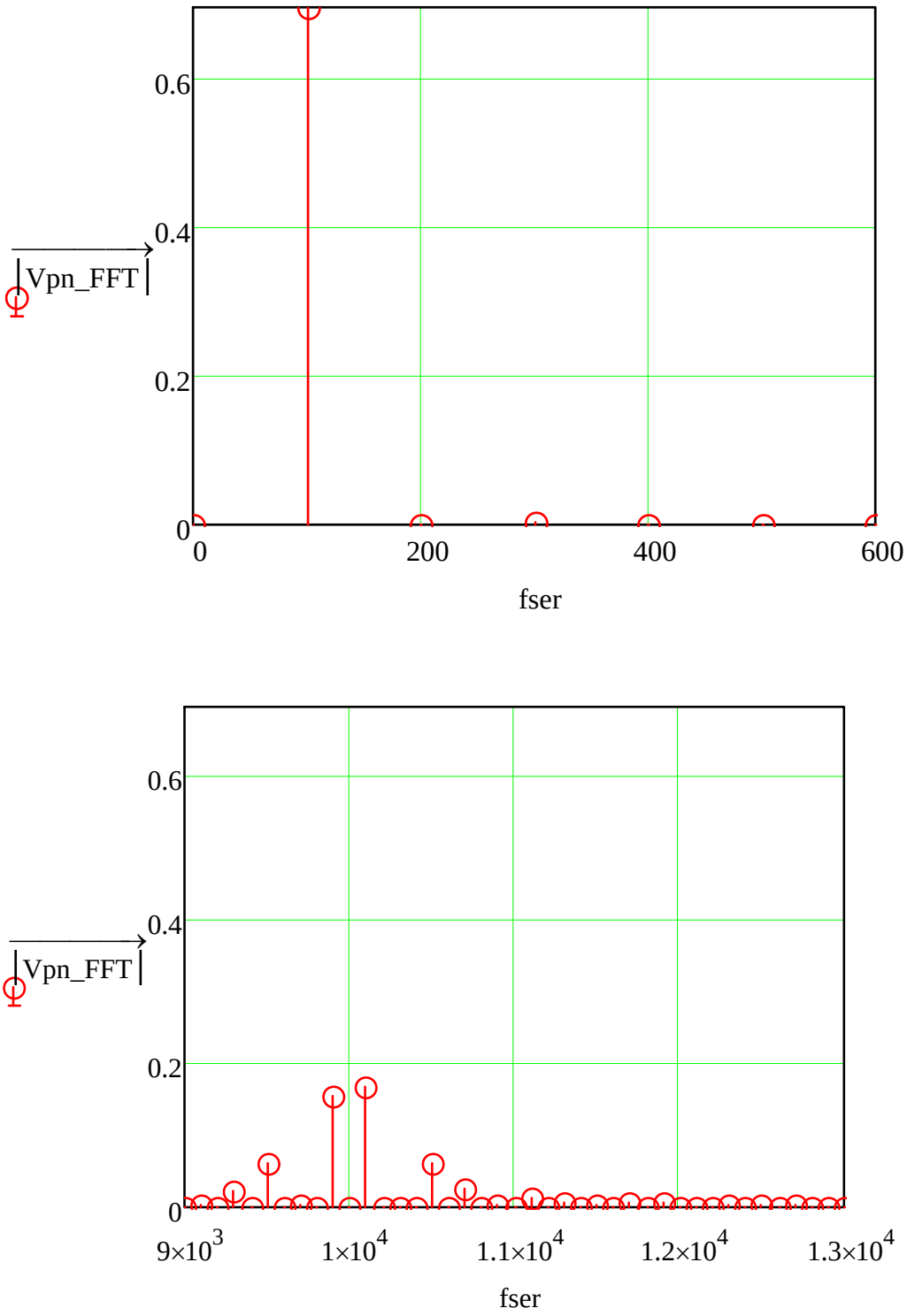
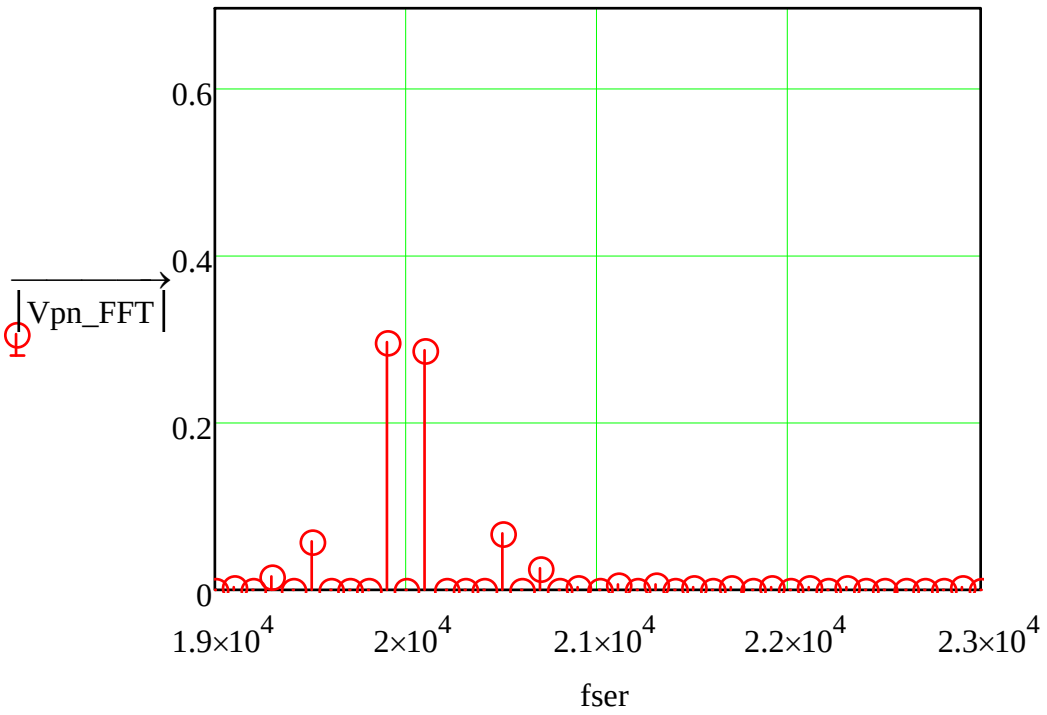


Figure 4.14. Numerical spectrum analysis of phase current for continuous SVPWM at M=0.8

Figure 4.14 (cont'd)



According to the selection in Table 4-5 and the sequence in Figure 4.11, the theoretical switching waveforms and also the phase current PWM form can be obtained. Set the parameters as: $M = 0.8$, $f_O = 100Hz$, $f_S = 10kHz$. Compared to continuous SVPWM, DPWM only has half fundamental period doing PWM switching. So in order to keep the same average switching frequency, the carrier frequency of continuous SVPWM is set to be half of DPWM, which is 10kHz here. The spectrum distribution diagrams at fundamental frequency and f_{sw}, $2f_{sw}$ are shown in Figure 4.14. The WTHD in this case is 0.5107%.

4.3.5. Simulation results

Figure 4.15 and Figure 4.16 shows the switching and output current waveforms. Compared to Figure 4.10, the output current contains higher switching ripple, thus higher total harmonic distortion.

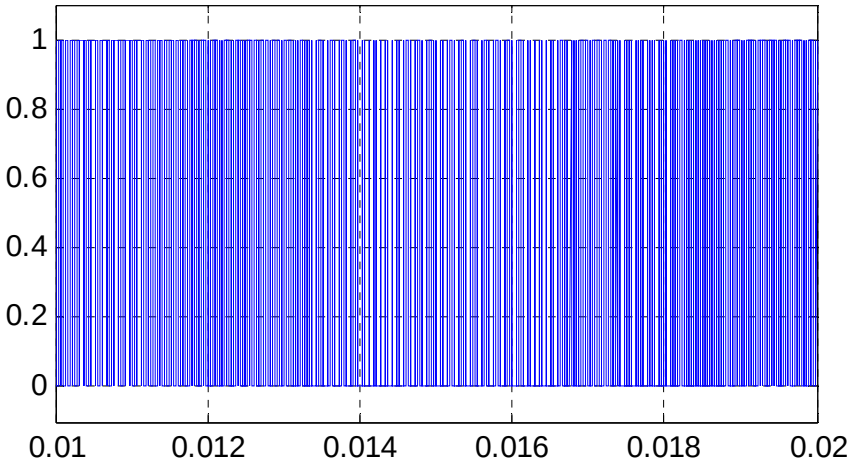


Figure 4.15. Switching waveform of continuous SVPWM

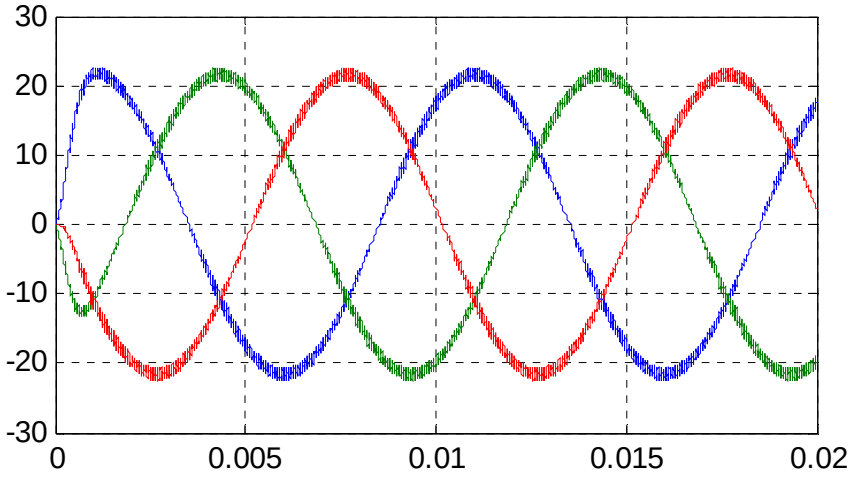


Figure 4.16. Simulated three phase output current after the filter

4.4. Space-Vector-Pulse-Width-Amplitude-Modulation (SVPWAM)

PWM methods are all about zero vector selection and zero vector placement. In order to further reduce the switching times, at the same time not affect the output sinusoidal waveform, one method is to eliminate the zero state in each sector. The switching period for each switch reduces to only 120 degree per 360 degree. Take S_1 as an example, it only has PWM switching in sector II and sector VI, so only for 120 degree. The elimination of zero state doesn't affect the output waveform, but do affect the input current, which can not be a

dc current but a dc current with 6ω ac ripple. ω refers to the fundamental frequency. Thus a dc-dc stage or an integrated dc-dc stage like the Z-source network has to be cascaded in front to generate this 6ω current on the dc link, instead of using of single stage inverter.

Thus a new modulation method SVPWAM "Space-Vector-Pulse-Width-Amplitude-Modulation" is proposed here, in order to reduce the switching loss. The reason it is named as "Space-Vector-Pulse-Width-Amplitude-Modulation" is that the amplitude of carrier waveform is not a constant but a varied waveform, and also it is based on different zero vector selection in SVPWM method. In order to implement this method, a front stage regulator needs to be connected in series with CSI to generate this varied dc link voltage.

4.4.1. SVPWAM for Voltage Source Inverter(VSI)

4.4.1.1. Principle of SVPWAM control in VSI

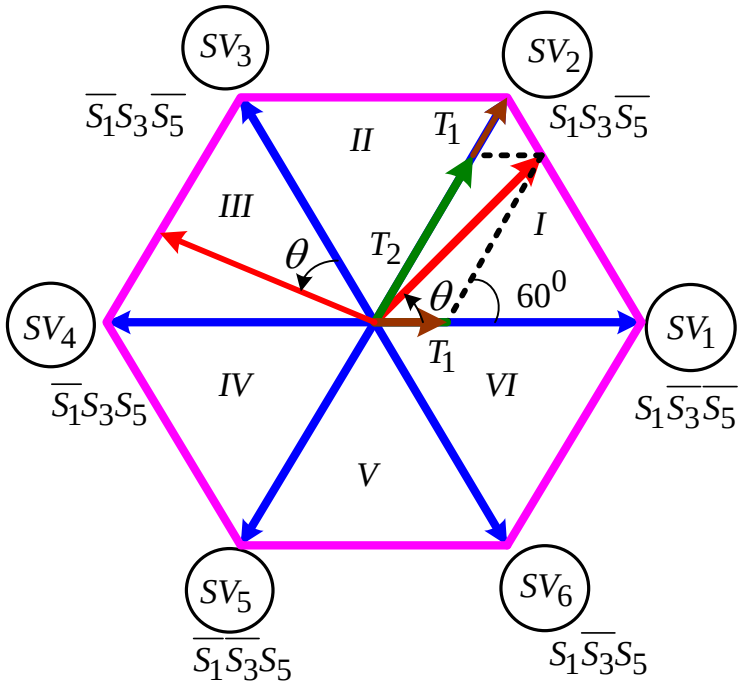


Figure 4.17. Space-Vector-Pulse-Width-Amplitude-Modulation for VSI

The principle of SVPWAM control is to eliminate the zero vector in each sector. The modulation principle of SVPWAM is shown in Figure 4.17. This imposes zero switching for one phase leg in the adjacent two sectors. For example in sector VI and I, phase leg A has no switching at all. The dc link voltage thus is directly generated from the output line to line voltage. In Sector I, no zero vector is selected. Therefore S_1 and S_2 keep constant on, and S_3 and S_6 are doing PWM switching. As a result, if the output voltage is kept the normal three phase sinusoidal voltage, the dc link voltage should be equal to line to line voltage V_{ac} at this time. In Sector II, it should be equal to V_{bc}. Other vectors are similar. Consequently the dc link voltage should present a 6ω varied feature to maintain a desired output voltage. In another word, it should be designed as the envelope of maximum output line to line voltage:

$$V_{dc} = \begin{cases} \sqrt{3}V_{peak}\sin(\omega_f t + \pi/3) & (0 \le \omega_f t \le \pi/3) \\ \sqrt{3}V_{peak}\sin\omega_f t & (\pi/3 \le \omega_f t \le 2\pi/3) \\ \sqrt{3}V_{peak}\sin(\omega_f t - \pi/3) & (2\pi/3 \le \omega_f t \le \pi) \\ \sqrt{3}V_{peak}\sin(\omega_f t - 2\pi/3) & (\pi \le \omega_f t \le 4\pi/3) \\ \sqrt{3}V_{peak}\sin(\omega_f t - \pi) & (4\pi/3 \le \omega_f t \le 5\pi/3) \\ \sqrt{3}V_{peak}\sin(\omega_f t - 4\pi/3) & (5\pi/3 \le \omega_f t \le 2\pi) \end{cases} \quad (4.7)$$

, assuming that phase-*a* voltage reference starts from angle 0. V_{peak} is the amplitude of the phase voltage. The dc link corresponding waveform is shown in solid line in Figure 4.18. A dc-dc conversion is needed in the front stage to generate this 6ω voltage. The topologies to implement this method will be discussed later.

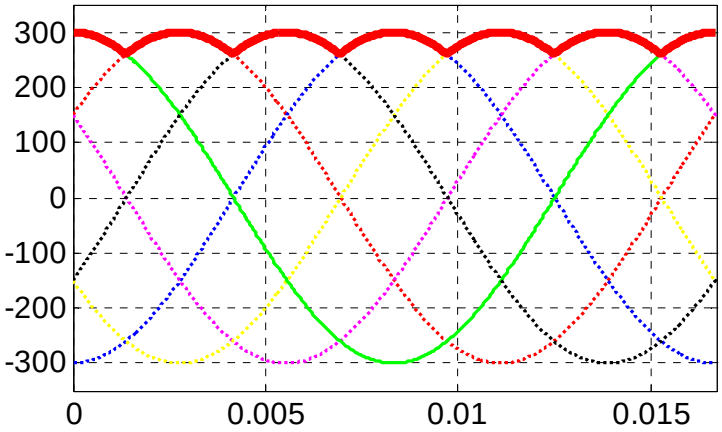


Figure 4.18 DC link voltage of SVPWAM in VSI

The benefit of this method is the significant switching loss reduction. In each sector, only two switches of the same phase leg are doing PWM switching. For each switch, it only does PWM switching in two sectors, which correspond 120 degrees in every fundamental cycle. Compared to conventional SPWM method, the switching frequency is reduced by 2/3. Compared to discontinuous PWM, the switching frequency is reduced by 1/3. The switching loss reduction can reach further to 87% if the power factor is unity, because the switching actions happen at the current zero crossing region. The details of switching loss reduction will be analyzed later.

For the time period calculation in SVPWAM, the switching time period is varied if original equations are used for T_1 and T_2:

$$T_1 = \frac{\sqrt{3}}{2} m \sin(\frac{\pi}{3} - \theta); T_2 = \frac{\sqrt{3}}{2} m \sin(\theta) \tag{4.8}$$

, where $\theta \in [0, \pi/3]$ is relative angle from the output voltage vector to the first adjacent basic voltage vector as shown in Figure 4.17. If T_1, T_2 maintain the same value as equation (4.8), the total switching period at angle θ is equal to the sum of these two since no zero vector is applied. This switching period is a varied value, which would cause additional

harmonic component in the output. Because the volt-seconds is the key point that affect the output voltage, a constant switching period can be used and two new active state period which holds the same proportion as the previous ones in eq. 4.8 can be created. Thus in order to keep the switching period constant but still keep the same pulse-width as the original one, the new time periods can be calculated in a constant proportion norm as:

$$\begin{aligned} T_1' + T_2' &= T_s \\ \frac{T_1'}{T_s} &= \frac{T_1}{T_1 + T_2} \\ \frac{T_2'}{T_s} &= \frac{T_2}{T_1 + T_2} \end{aligned} \tag{4.9}$$

In this case, the pulse width doesn't change while the switching period is kept constant.

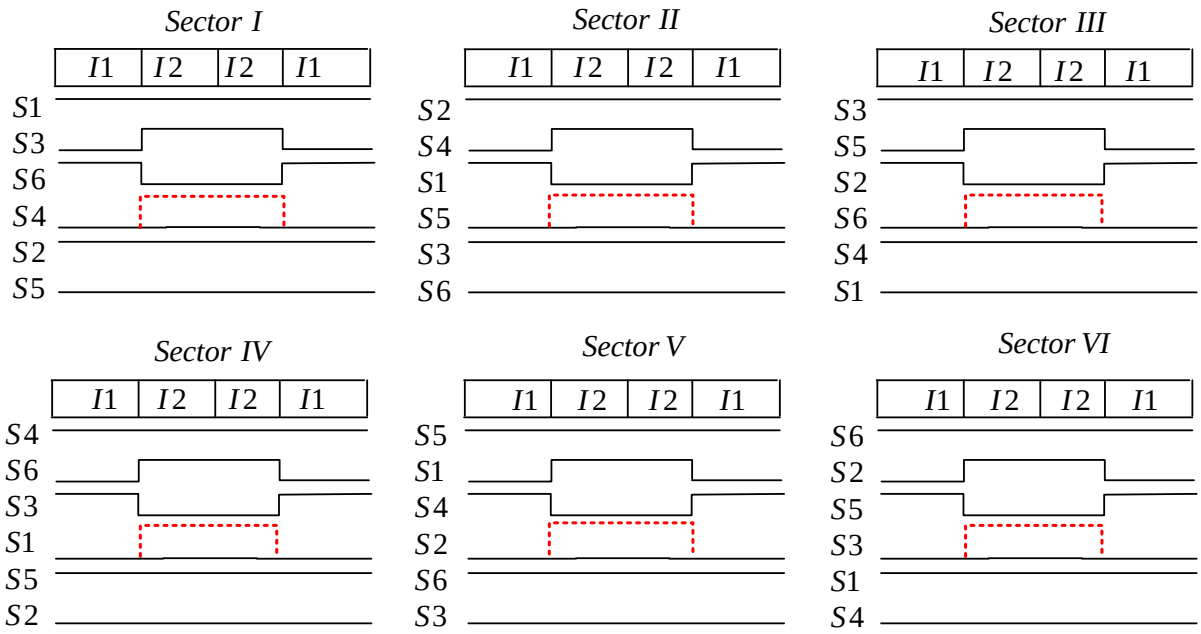


Figure 4.19. Vector placement in each sector for VSI

The vector placement within one switching cycle in each sector is shown in Figure 4.19. In practical implementation, the two PWM waveforms generated from DSP can be assigned to different switches in different sectors. There are only two PWM for six switches. One in three original PWM has been eliminated. That is also corresponding to the switch that

generates zero vector, as shown in dotted line in Figure 4.19. The relative position of T_1 and T_2 can only have one choice, but the starting and ending time can be flexible, which may cause different output harmonics. In another work, how to assign the time period for each section of I_1 or I_2 is flexible.

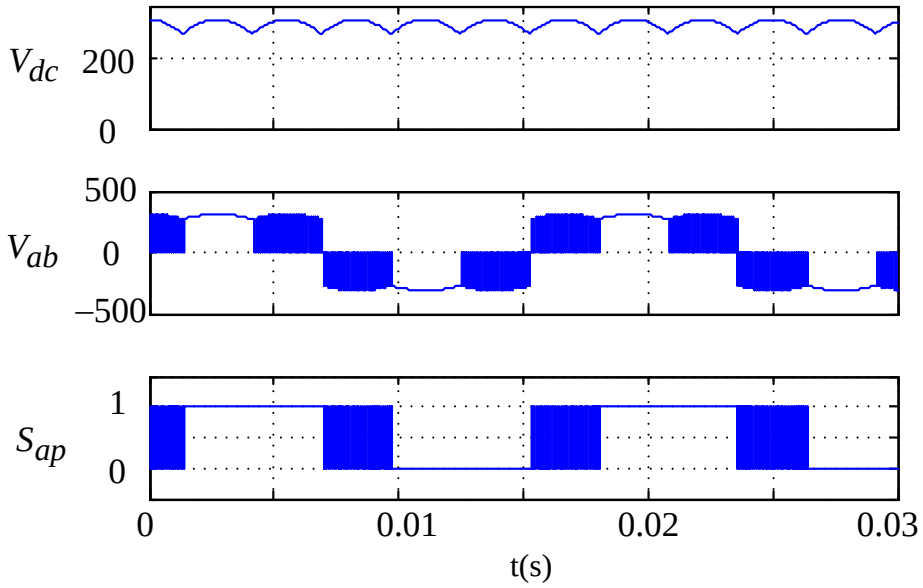


Figure 4.20. Theoretic waveforms of dc link voltage, output line to line voltage and switching signals

Figure 4.20 shows the ideal waveforms of the bus voltage V_{dc}, the output line to line voltage of the first inverter phase leg, and the switching signals of S_1. Unlike the conventional SVPWM and SPWM control, the SVPWAM technique combines the pulse width modulation and amplitude modulation together such that each inverter phase leg only switches during one third of the fundamental period. The output line to line voltage partly overlaps with the dc link voltage, which potentially reduce the its harmonics content, as long as the dc link voltage doesn't have high harmonics. However, the dc link voltage generated by dc-dc converter usually has switching ripple, which will add to the output line to line voltage of inverter. It

may increase the harmonic level also.

4.4.1.2. Inverter switching loss reduction for VSI

For unity power factor case, the inverter switching loss is reduced by 86% although the switching phase-span has only been reduced by 2/3. Such difference is because the switching current is in zero crossing region, as shown in Figure 4.21. The phase voltage can be divided into four sections: $[-30^0, 30^0], [30^0, 150^0], [150^0, 210^0], [210^0, 330^0]$. During $[30^0, 150^0]$ and $[210^0, 330^0]$, the phase voltage exhibits the maximum and minimum voltage among the whole period, which is directed connected to the dc link voltage, so there is no PWM switching in these two periods. However, in another two 60 degree sections, the voltage is in middle range, so it is generated from PWM switching referenced to the 6ω varied dc link voltage envelope. The PWM switching region is shown in the shadow area of Figure 4.21. The current is $\pm 30^0$ around its zero point, as well as the phase voltage. The voltage and current slop is the slowest in this region among all 360 degree period.

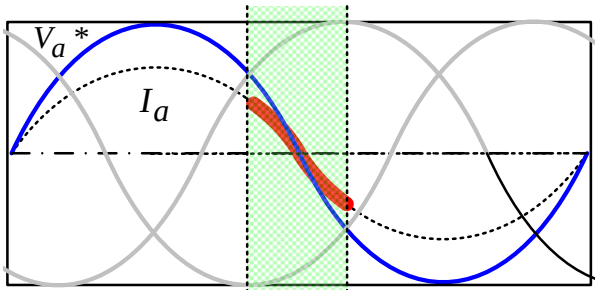


Figure 4.21. Switch voltage and current stress when pf=1 (In shadow area)

In voltage source inverter, the voltage stress on the switch is equal to dc link voltage, and the current stress is equal to output current. Thus the voltage stress is always maximum line to line voltage and the current stress is always from $I_{peak}(-\sin 30^0)$ to $I_{peak}(\sin 30^0)$.

The general equation for switching loss calculation of each switch is:

$$P_{SW\_VSI} = \frac{1}{2\pi}\int_0^{2\pi} E_{SR}\frac{|i_a|\cdot V_{DC}}{V_{ref}\,I_{ref}}\cdot f_{sw}\,d\omega t \tag{4.10}$$

, where i_a represents the output current; V_{DC} is the average dc link voltage, which is an approximate switching voltage here; and $E_{\mathrm{SR}}, V_{ref}, I_{ref}$ are the switching energy, reference voltage and current, respectively. The total switching loss is $6\times P_{SW\_I}$.

Since the SVPWAM only has PWM switching in two 60 degree sections, the integration over 2π can be narrowed down into integration within two 60 degrees:

$$\begin{aligned} P_{SW\_I} &\approx \frac{1}{2\pi}\Big[\int_{-\pi/6}^{\pi/6} E_{SR}\frac{|I_m\sin(\omega t)|\cdot\overline{V_{DC}}}{V_{ref}\,I_{ref}}\cdot f_{sw}\,d\omega t \\ &\quad + \int_{5\pi/6}^{7\pi/6} E_{SR}\frac{|I_m\sin(\omega t)|\cdot\overline{V_{DC}}}{V_{ref}\,I_{ref}}\cdot f_{sw}\,d\omega t \\ &= \frac{2-\sqrt{3}}{\pi}\cdot\frac{I_m\overline{V_{DC}}}{V_{ref}\,I_{ref}}E_{SR}\cdot f_{sw} \end{aligned} \tag{4.11}$$

The average value during each 60 degree section is:

$$\overline{V_{DC}} = \int_{-\pi/6}^{\pi/6}\cdot V_{peak}\cos\theta\,d\theta = \frac{3}{\pi}\cdot V_{peak} \tag{4.12}$$

The switching loss for conventional SPWM method is:

$$\begin{aligned} P_{SW\_I}' &= \frac{1}{2\pi}\Big[\int_0^{2\pi} E_{SR}\frac{|I_m\sin(\omega t)|\cdot V_{DC}}{V_{ref}\,I_{ref}}\cdot f_{sw}\,d\omega t \\ &= \frac{2}{\pi}\cdot\frac{I_m V_{DC}}{V_{ref}\,I_{ref}}E_{SR}\cdot f_{sw} \approx \frac{2}{\pi}\cdot\frac{I_m V_{peak}}{V_{ref}\,I_{ref}}E_{SR}\cdot f_{sw} \end{aligned} \tag{4.13}$$

In result, the switching loss of SVPWAM over SPWM is: $f = \frac{2-\sqrt{3}}{\pi}\cdot\frac{3}{\pi}/\frac{2}{\pi} = 12.8\%$. The switching loss has been reduced by 87%.

However, when the power factor decreases, the switching loss reduction amount decreases because the switching current increases. As shown in Figure 4.21, the voltage remains in that section but the current switching region shifts. Thus the equation (4.11)

should be re-written as:

$$P_{SW\_I} \approx \frac{1}{2\pi}\left[\int_{-\pi/6}^{\pi/6} E_{SR}\frac{|I_m \sin(\omega t-\phi)|\cdot\overline{V_{DC}}}{V_{ref} I_{ref}}\cdot f_{sw}\, d\omega t + \int_{5\pi/6}^{7\pi/6} E_{SR}\frac{|I_m \sin(\omega t-\phi)|\cdot\overline{V_{DC}}}{V_{ref} I_{ref}}\cdot f_{sw}\, d\omega t\right] \quad (4.14)$$

Figure 4.22 shows the relationship between the power loss percentage ratio and the power factor calculated according to eq. (4.14).

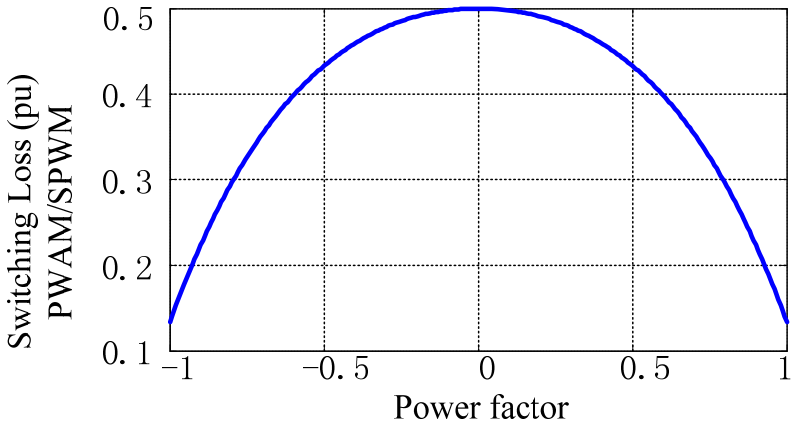


Figure 4.22. (SVPWAM power loss / SPWM power loss) vs. power factor in VSI

As indicated, the worst case happens when power factor is equal to zero, because the switching current is in maximum 60 degrees area. But the switching loss reduction in this case still reaches 50%. In conclusion, SVPWAM can bring the switching loss down by 50% ~ 87% according to different power factor.

4.4.2. SVPWAM for Current Source Inverter(CSI)

4.4.2.1. Principle of SVPWAM in CSI

The principle of SVPWAM in current source inverter is also to eliminate the zero vectors. As shown in Figure 4.23, for each sector, only two switches are doing PWM switching, since only one switch in upper phase legs and one switch in lower phase legs are

conducting together at any moment. Thus for each switch, it only needs to do PWM switching in two sectors, which is 1/3 of the switching period. Compared to the SVPWM that with single zero vector selected in each sector, this method brings down the switching frequency by 1/3, since

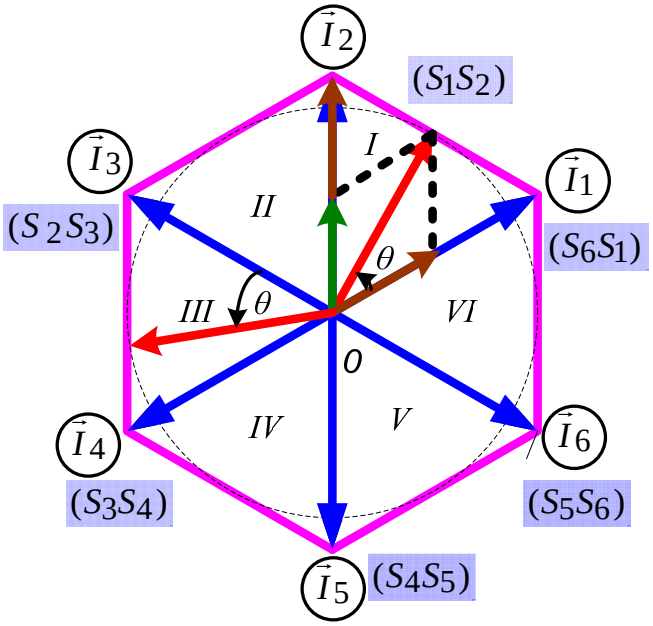


Figure 4.23 Current source inverter SVPWAM diagram

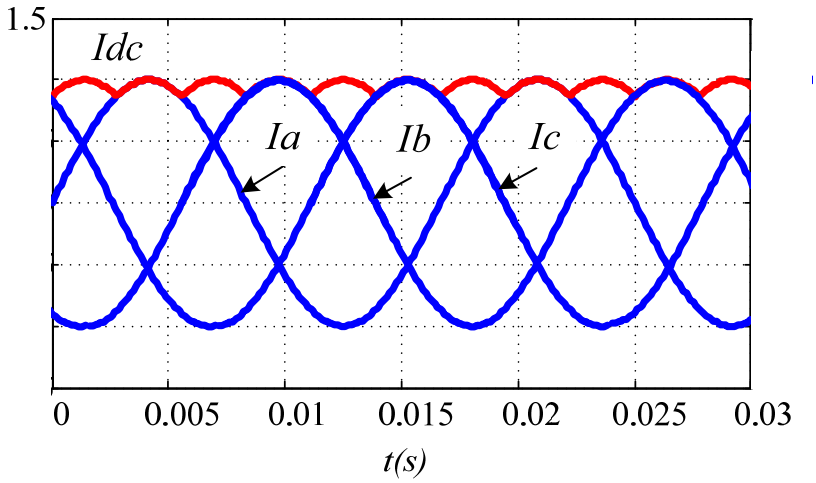


Figure 4.24. DC current and output phase current waveform

the previous one requires switch to do PWM switching in half switching period, but this one only 120^0.

Similarly, the dc link current in this case is a 6ω varied current. It is the maximum envelope of six output currents: $I_a, I_b, I_c, -I_a, -I_b, -I_c$, as shown in Figure 4.24. For example, in Sector I, S_1 always keeps on, so the dc link current is equal to I_a. In Sector II, S_2 is constantly on, so dc link current is equal to -I_c. Assume the output phase current reference starts from angle 0, the required dc link current is:

$$I_{dc} = \begin{cases} I_{peak}\sin(\omega_f t + \pi/3) & (0 \le \omega_f t \le \pi/3) \\ I_{peak}\sin\omega_f t & (\pi/3 \le \omega_f t \le 2\pi/3) \\ I_{peak}\sin(\omega_f t - \pi/3) & (2\pi/3 \le \omega_f t \le \pi) \\ I_{peak}\sin(\omega_f t - 2\pi/3) & (\pi \le \omega_f t \le 4\pi/3) \\ I_{peak}\sin(\omega_f t - \pi) & (4\pi/3 \le \omega_f t \le 5\pi/3) \\ I_{peak}\sin(\omega_f t - 4\pi/3) & (5\pi/3 \le \omega_f t \le 2\pi) \end{cases} \tag{4.15}$$

The time intervals for two adjacent vectors can be calculated in the same way as equation (2) and (3). The angle θ is shown in Figure 4.23.

According to diagram in Figure 4.23, the vector placement in each switching cycle for six switches can be plotted in Figure 4.25.

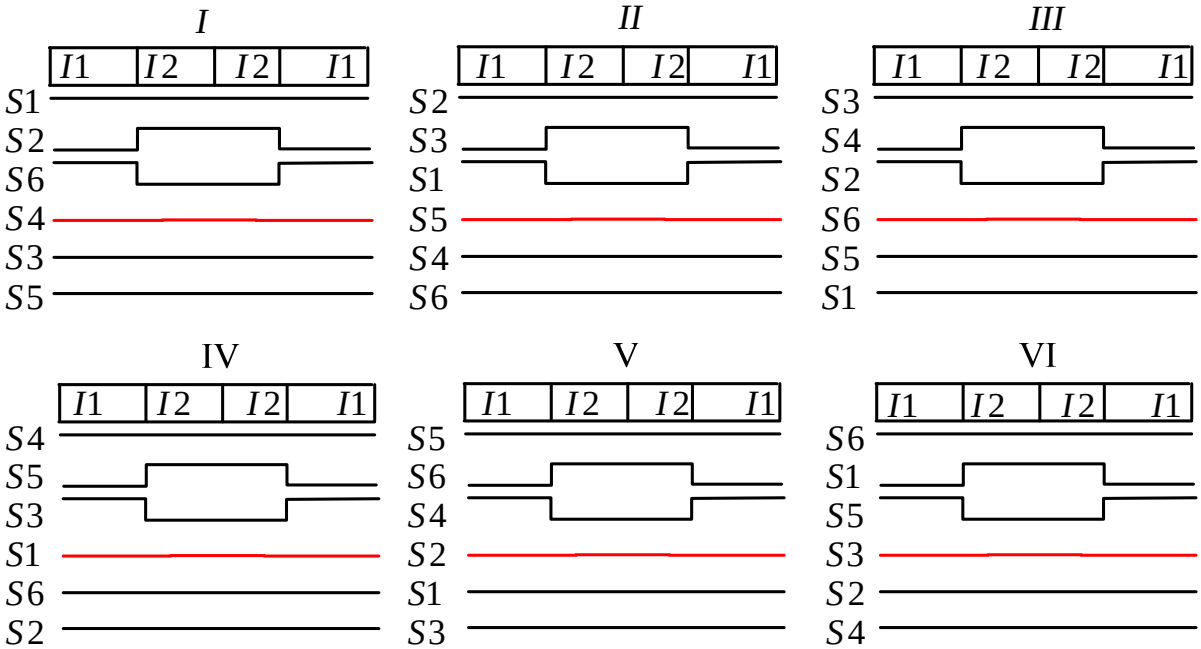


Figure 4.25. Vector placement for each sector for CSI

Figure 4.26 shows the ideal waveforms of the dc current I_{dc}, the output phase a current and the switching signals of S_1. The switching signal has two sections of PWM in positive cycle, but no PWM in negative cycle at all. However, the conventional SVPWM with only one zero vector selected, has an additional 60 degree PWM section in negative half cycle. So the switching frequency is reduced by 1/3.

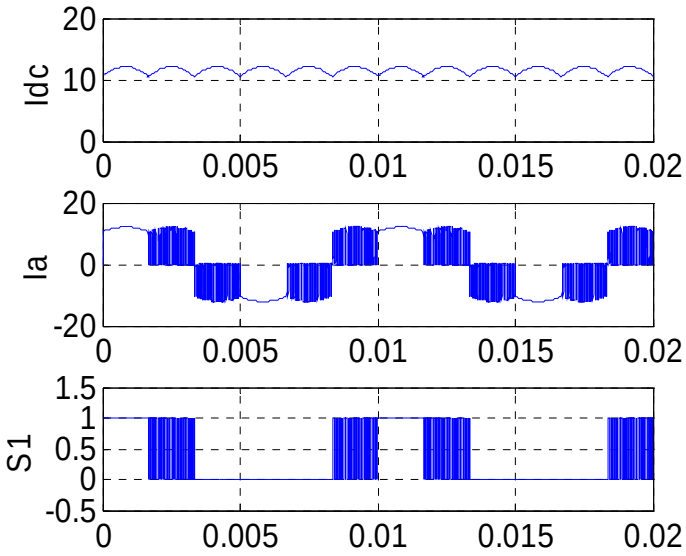


Figure 4.26. Theoretic waveforms of dc link current, output line current and switching signals

4.4.2.2. Inverter switching loss reduction for CSI

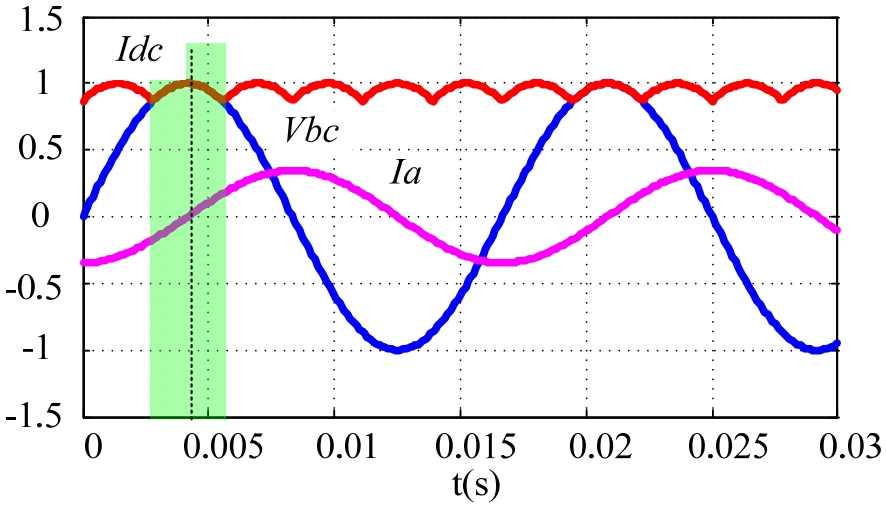


Figure 4.27. Switching voltage and current when pf=1

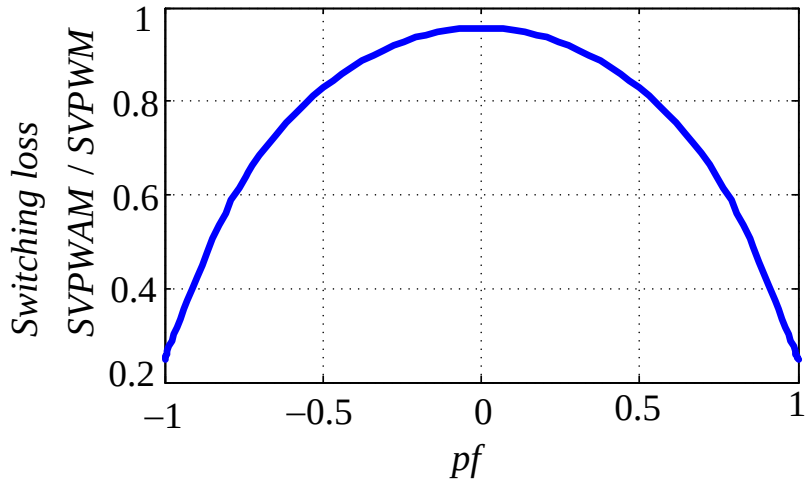


Figure 4.28. CSI switching loss SVPWAM/SVPWM vs. power factor

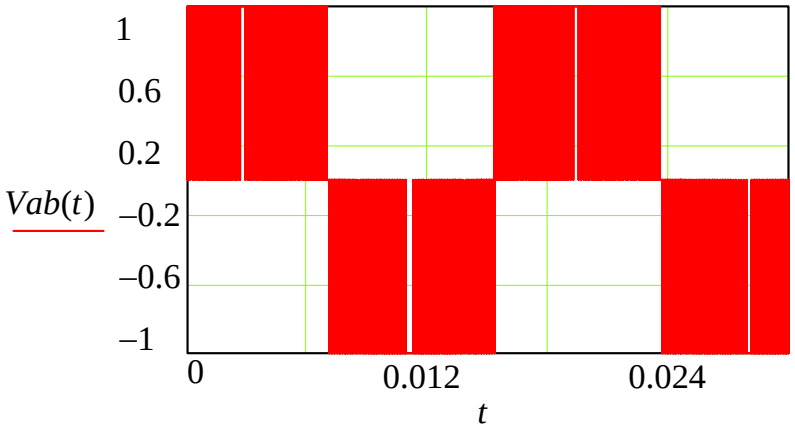
In current source inverter, the current stress on the switch is equal to the dc link current, and the voltage stress is equal to output line to line voltage. The shadow area in Figure 4.27 shows the switching current and voltage in Sector I. For a single switch, the switching loss is determined by

$$P_{SW\_CSI} = 2*\frac{1}{2\pi}\int_{\pi/3}^{2\pi/3} E_{SR}\frac{|i_a|\cdot|V_{bc}|}{V_{ref}\,I_{ref}}\cdot f_{sw}\,d\omega t \qquad (4.16)$$

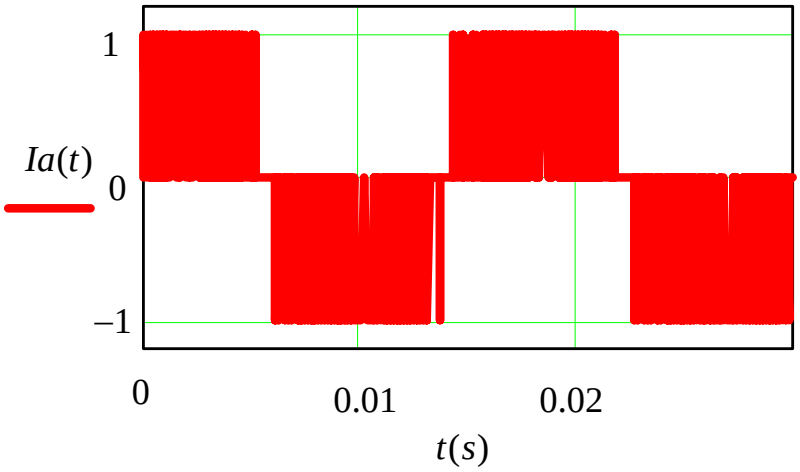
The voltage is within $\pm 30^0$ of the zero-crossing region, and the current is at the maximum 60^0 area. Thus this switching loss is similar to the one in voltage source inverter. But the comparison object switching loss in SVPWM of CSI becomes only half of the SPWM if the same switching frequency is used. So the switching loss reduction relative to SVPWM method can be plotted with power factor in Figure 4.28. The value is half of the value in Figure 4.22. The maximum switching loss reduction is 73.2% at unity power factor. The minimum switching loss reduction is 4.3% at power factor equal to zero.

4.4.3. Spectrum Analysis of SVPWAM

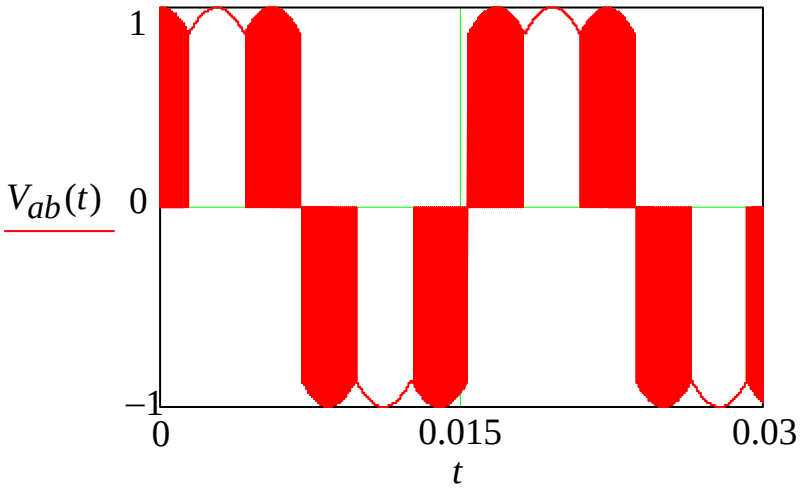
4.4.3.1. Spectrum comparison between SPWM, DSVPWM and SVPWAM in VSI



(a) Output line to line voltage in VSI at SPWM control



(b) Output line to line voltage in VSI at discontinuous SVPWM control



(c) Output line to line voltage in VSI at SVPWAM control

Figure 4.29. Output line to line voltage waveform for three methods: (a) SPWM; (b) discontinuous SVPWM; and (c) SVPWAM

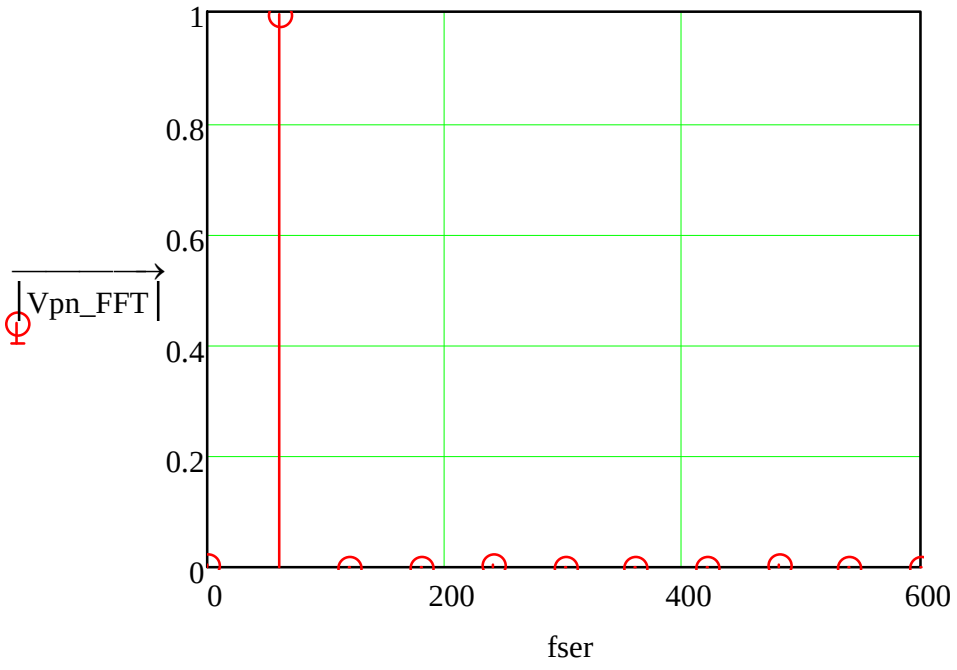
The object of spectrum analysis is the output voltage or current before the filter, not a single switch. The output spectrum is different from a single switch because certain orders of harmonics can be eliminated by sum of subtraction of switching functions. In voltage source inverter, the output voltage is equal to half dc voltage times the summation of two switching functions on the same phase leg. However, in current source inverter, the output current is equal to dc current times the subtraction of upper switching function to lower switching function on the same phase leg. Their waveforms are shown in Figure 4.29.

The comparison is conducted between SVPWAM, discontinuous SVPWM and continuous SVPWM in VSI.

The switching frequency selected for each method is different, because the comparison is built on a basis of equalized average switching frequency over a whole fundamental cycle, in order to not sacrifice the output harmonic performance. Assume the base frequency is f_0. Thus $3f_0$ should be selected for SVPWAM, $2f_0$ should be selected for discontinuous SVPWM and f_0 should be selected for continuous SVPWM in VSI, since they switches for 120 degrees, 180 degrees and 360 degrees respectively for every 360 degree fundamental cycle. In CSI, $3f_0$, $2f_0$ and f_0 should be selected for SVPWAM, discontinuous SVPWM, and continuous SVPWM, respectively, because the PWM switching range is 120 degrees, 180 degrees and 360 degrees respectively. In another word, only by increasing the average switching frequency of SVPWAM or discontinuous SVPWM to the same level of continuous SVPWM, the harmonics are comparable at both low modulation and high modulation range. Here the base switching frequency is selected to be 10.8 kHz, because it is the integer times of the fundamental frequency 60 Hz, which eliminates lots of sub-frequency harmonic component. .

The modulation index selected for all methods here is the maximum modulation index 1.15, since the SVPWAM always only has the maximum modulation index. In this case, the fundamental components are all 1.

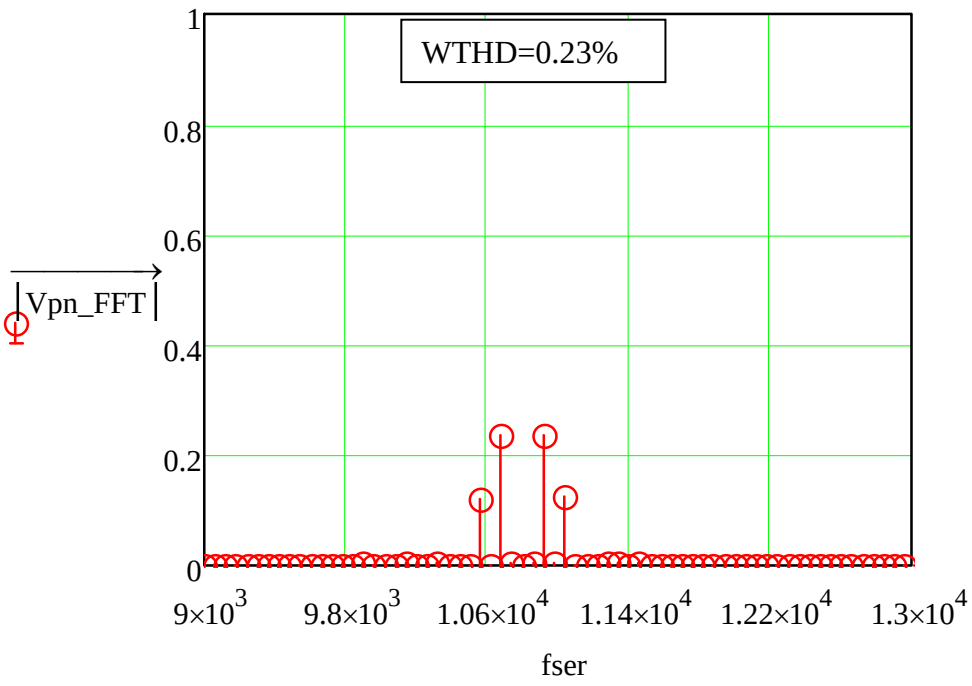
The dc link voltage is designed to be a constant for SVPWM and an ideal 6ω envelope of the output six line to line voltages for SVPWAM. Thus the harmonic of the SVPWAM here doesn't contain the harmonics from the dc-dc converter output. It is direct comparison between two modulation methods themselves from mathematics point of view, not involving the harmonics brought by other factors. In practice, the SVPWAM may have higher harmonic components because of the distortion in the dc link voltage/current. For example, if the front stage is a dc-dc converter, the dc link voltage contains switching frequency ripple.



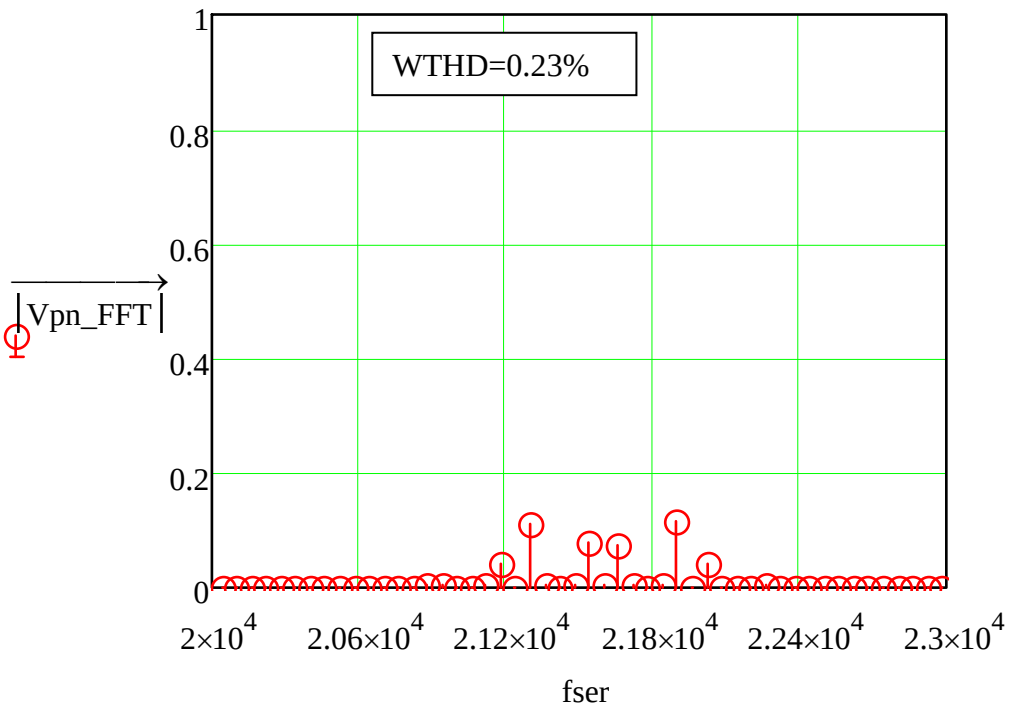
(a)

Figure 4.30. Spectrum of SPWM: (a) zoom-in at fundamental frequency; (b) zoom-in at switching frequency; (c) zoom-in at double its own switching frequency

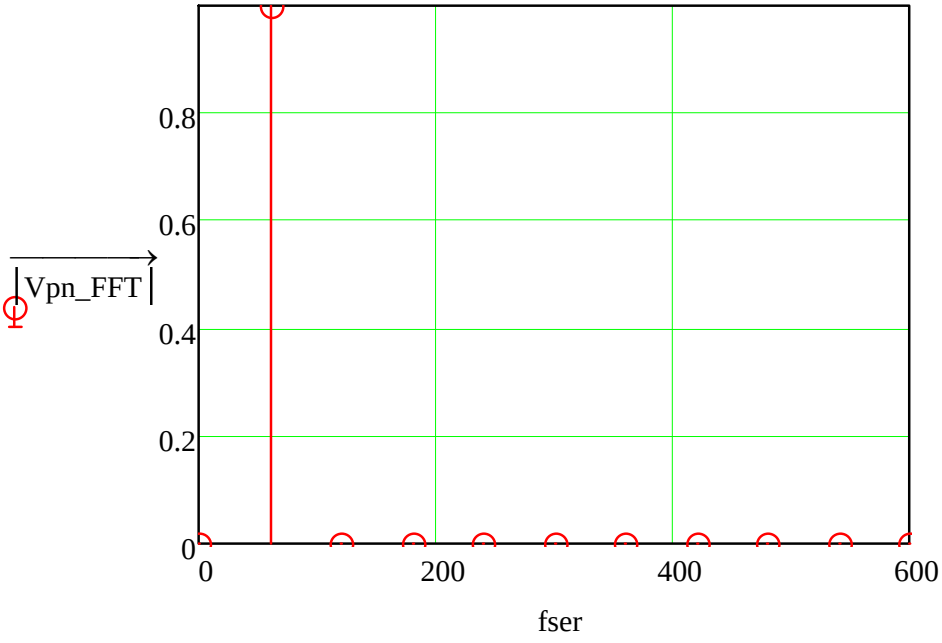
Figure 4.30 (cont'd)



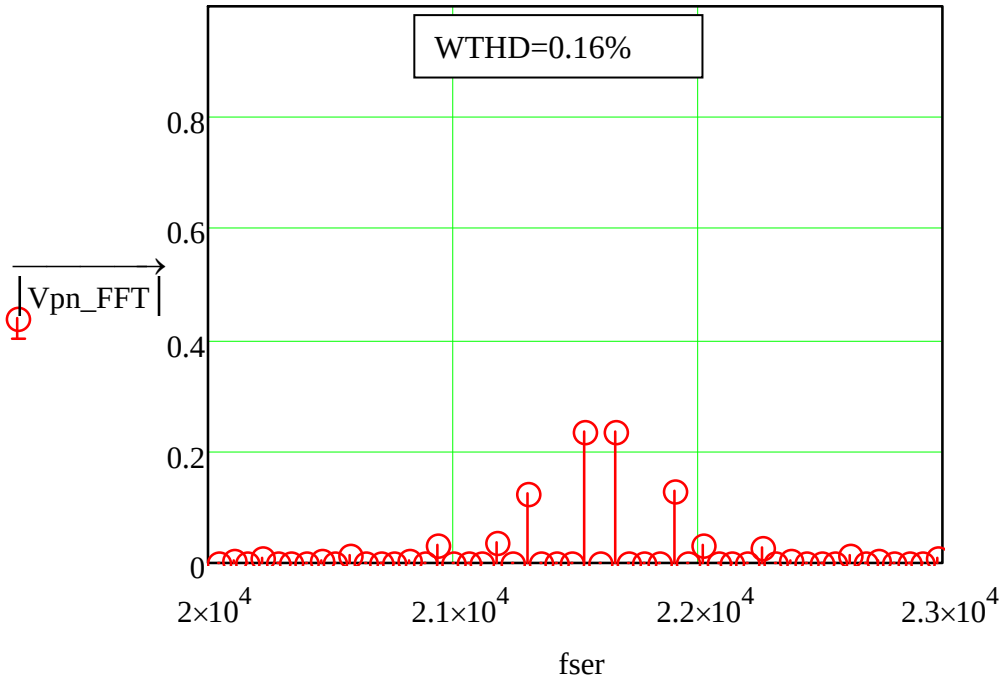
(b)



(c)

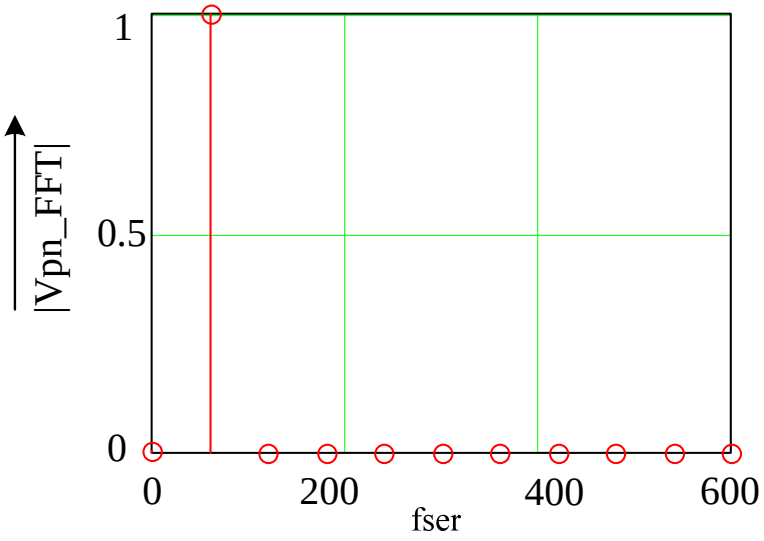


(a)

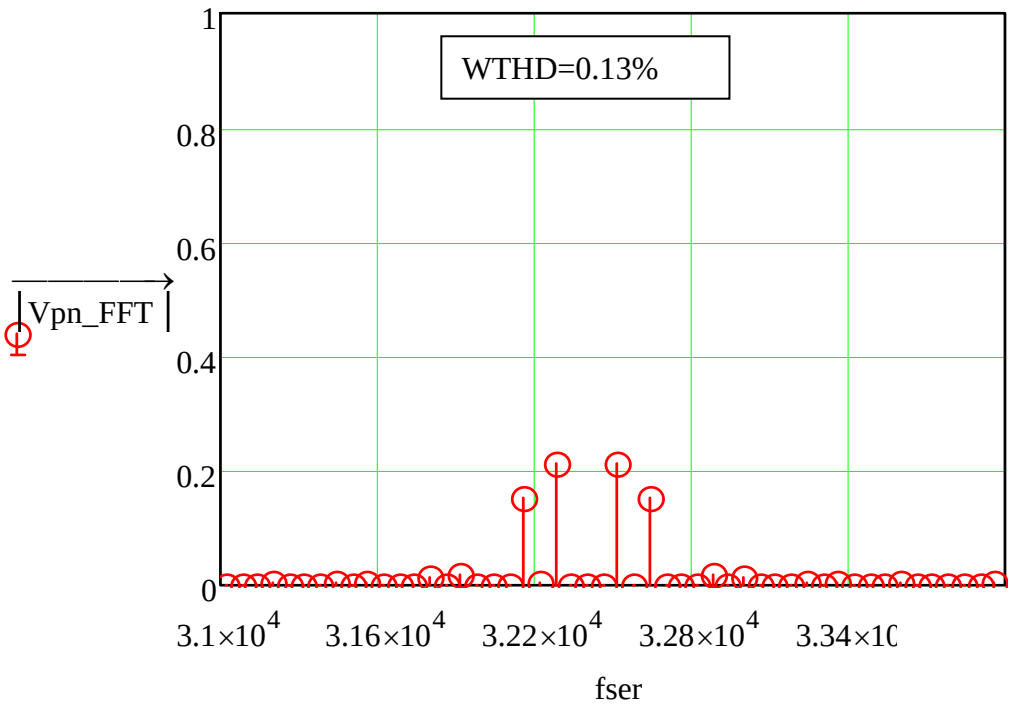


(b)

Figure 4.31. Spectrum of discontinuous SVPWM: (a) zoom-in at fundamental frequency; (b) zoom-in at switching frequency.



(a) Spectrum at fundamental frequency



(b) Spectrum at switching frequency

Figure 4.32. Spectrum of SVPWAM: (a) zoom-in at fundamental frequency; (b) zoom-in at switching frequency

Figure 4.30 – Figure 4.32 show the calculated spectrum magnitude at fundamental frequency range and integer times of switching frequency range for three methods. As mentioned before,

for a fair comparison, different switching frequency has been used for different methods, in order to reach the same average switching frequency. 10kHz, 20kHz and 30kHz have been used for SPWM, discontinuous SVPWM and SVPWAM respectively. The weighted total harmonic distortion (WTHD) is defined as:

$$WTHD = \frac{\sqrt{\sum_{kk=2}^{N}\left(\frac{\left|V_{FFT_{kk}}\right|}{kk}\right)^2}}{V_{FFT_1}} \tag{4.17}$$

The difference between WTHD and THD is the amplitude for certain order harmonics in WTHD needs to be divided by the order number. It can better represent the THD level for different methods because the importance of the harmonics decreases as the frequency increases. High frequency harmonics can be more easily reduced by the output low pass filter, but not the lower ones. WTHD is calculated to be 0.23% for SPWM, 0.16% for discontinuous SVPWM and 0.13% for SVPWAM. It can be concluded that the ideal switching function of SVPWAM has less or comparable harmonics with SPWM and DPWM. However, the 6ω dc link voltage is generated by the front stage dc-dc converter, so it contains additional switching ripple from the dc-dc converter switching, which may increase the harmonic content in SVPWAM. From the numerical analysis of the simulation results, this increase has no significant increase for the THD of output waveform. Thus it can be concluded that the SVPWAM features better or at least comparable harmonic performance as the other modulation methods.

4.4.3.2. Spectrum comparison between discontinuous SVPWM, continuous SVPWM and SVPWAM in CSI

(1) Discontinuous SVPWM

According to switching state assignment in Figure 4.5, switching time calculation from equation (4.2) and the switching waveform implementation in Figure 4.8, the numerical switching waveform in one fundamental cycle could be obtained for each DPWM methods. Set the parameters as: *M*=0.8, *fo*=100Hz, *fs*=20kHz. The spectrum distribution diagrams of each sequence at frequency range of fundamental frequency and switching frequency are shown in Figure 4.33 (a)(b)(c). The weighted THD has been used to be a criterion for evaluating the total harmonics distortion of each method. The definition of WTHD and results for each sequence are shown in equation (4.17).

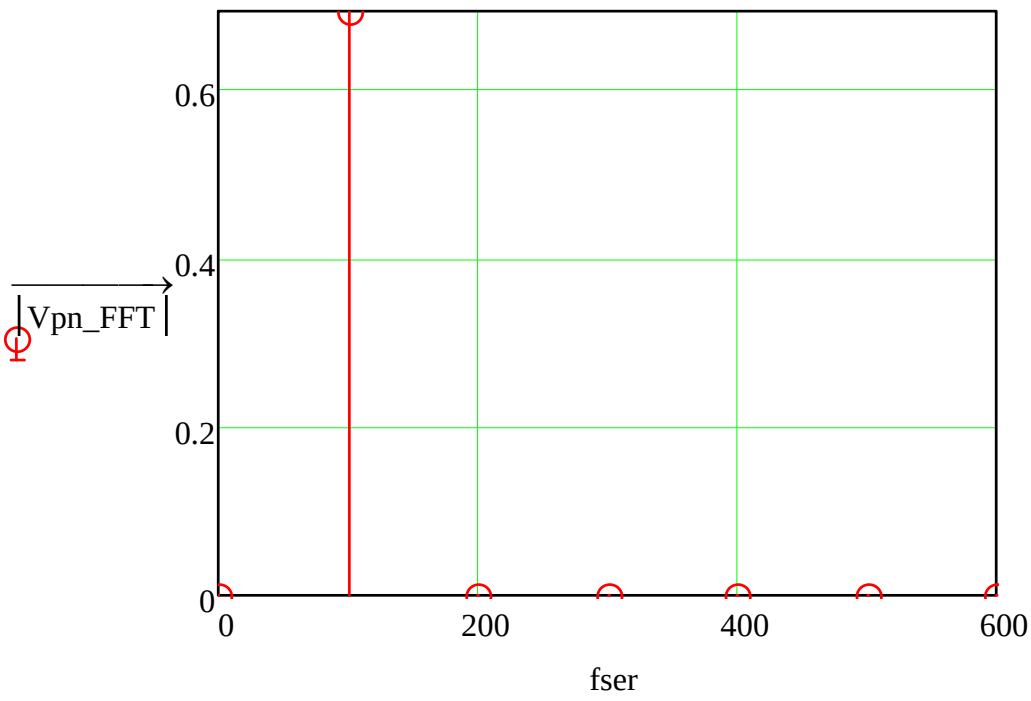
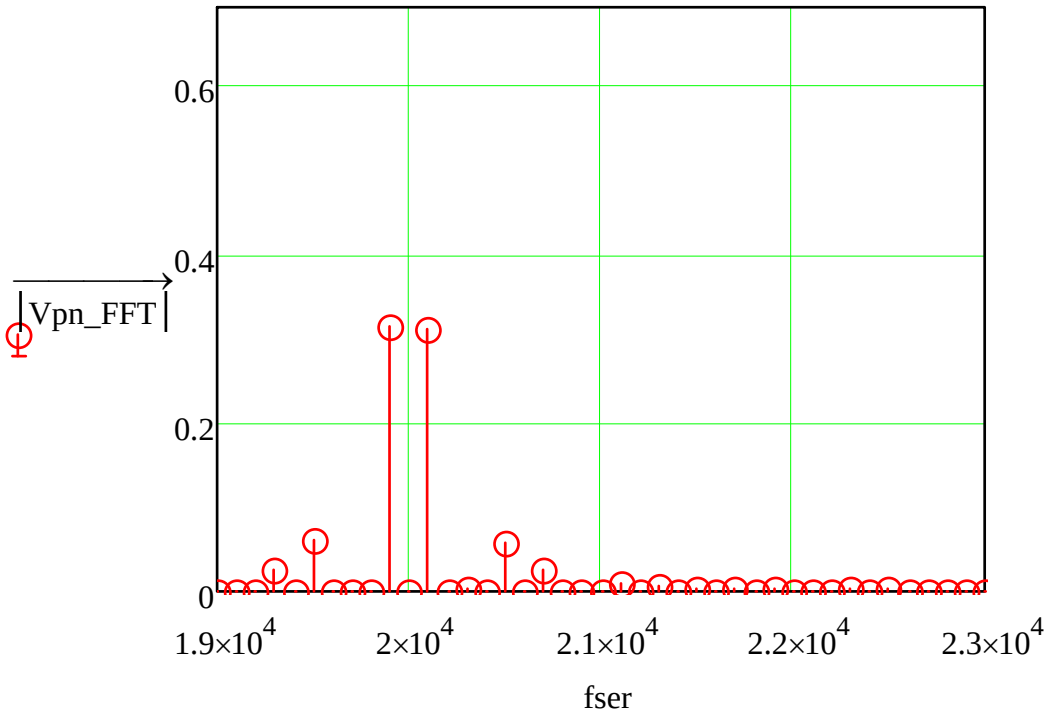


Figure 4.33. Numerical FFT results for b, c, d at m=0.8 for both fundamental frequency range and switching frequency range

Figure 4.33 (cont'd)



(a) FFT for phase current of DPWM sequence b at m=0.8

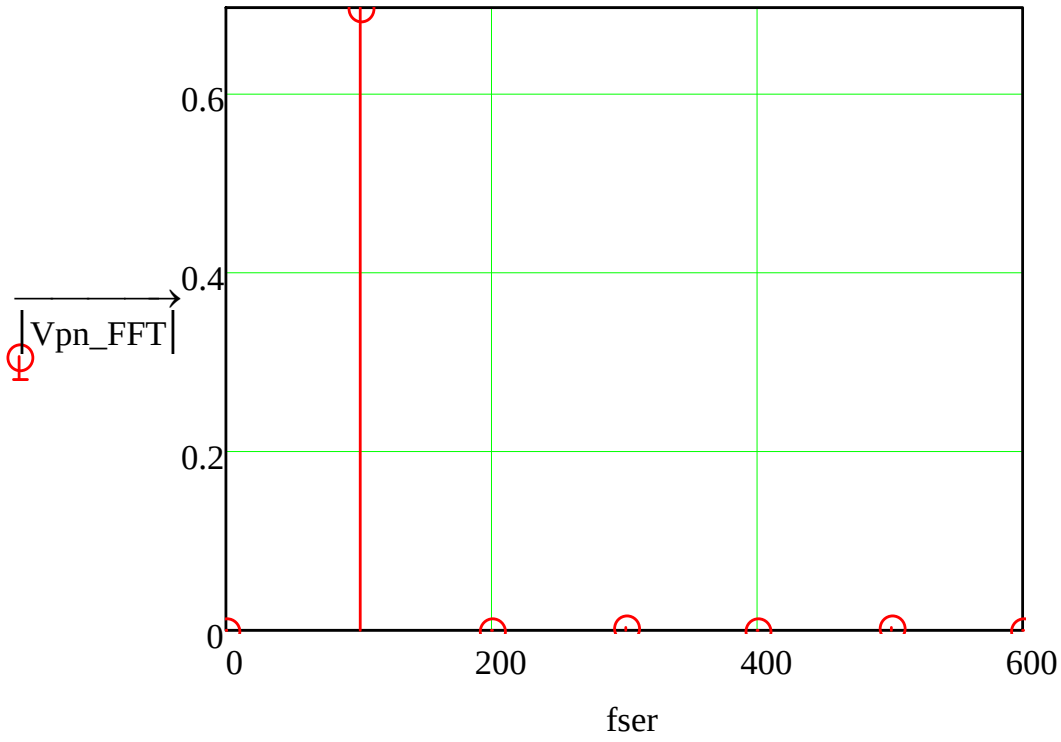
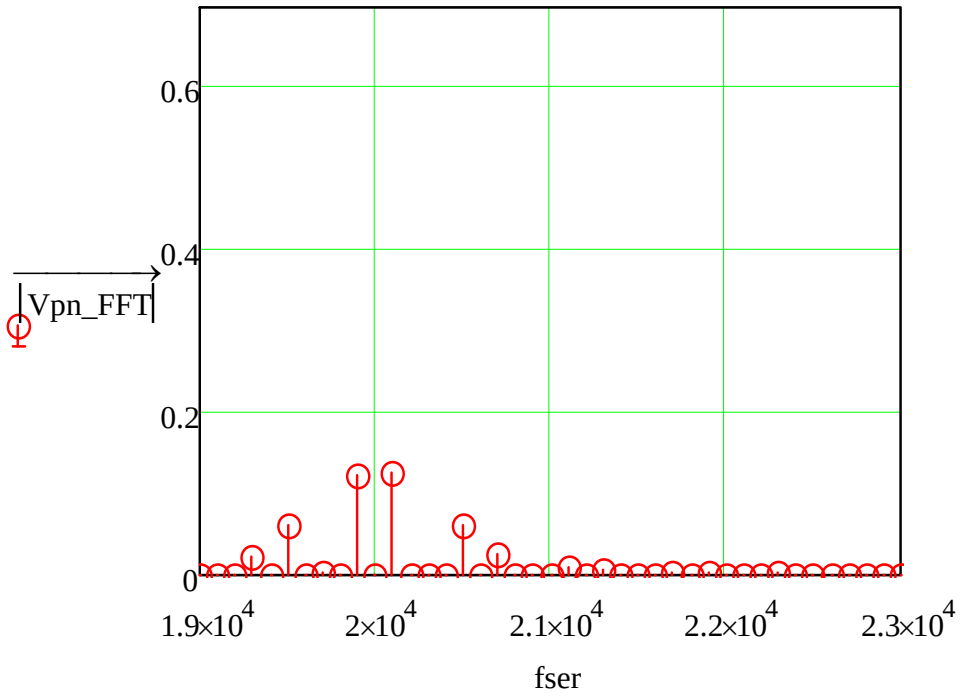


Figure 4.33 (cont'd)



(b) FFT for phase current of DPWM sequence c at m=0.8

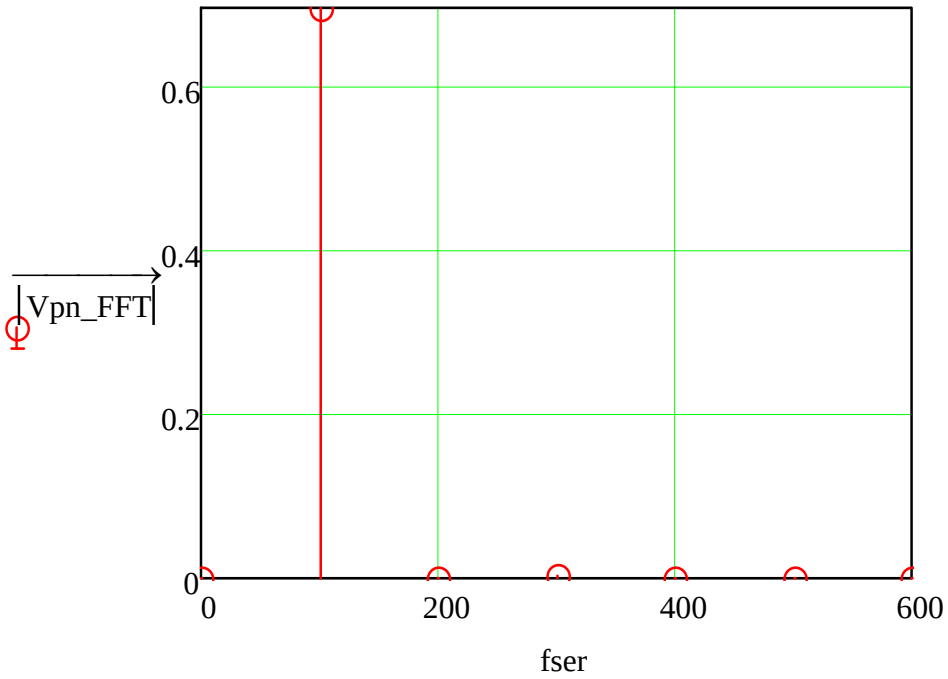
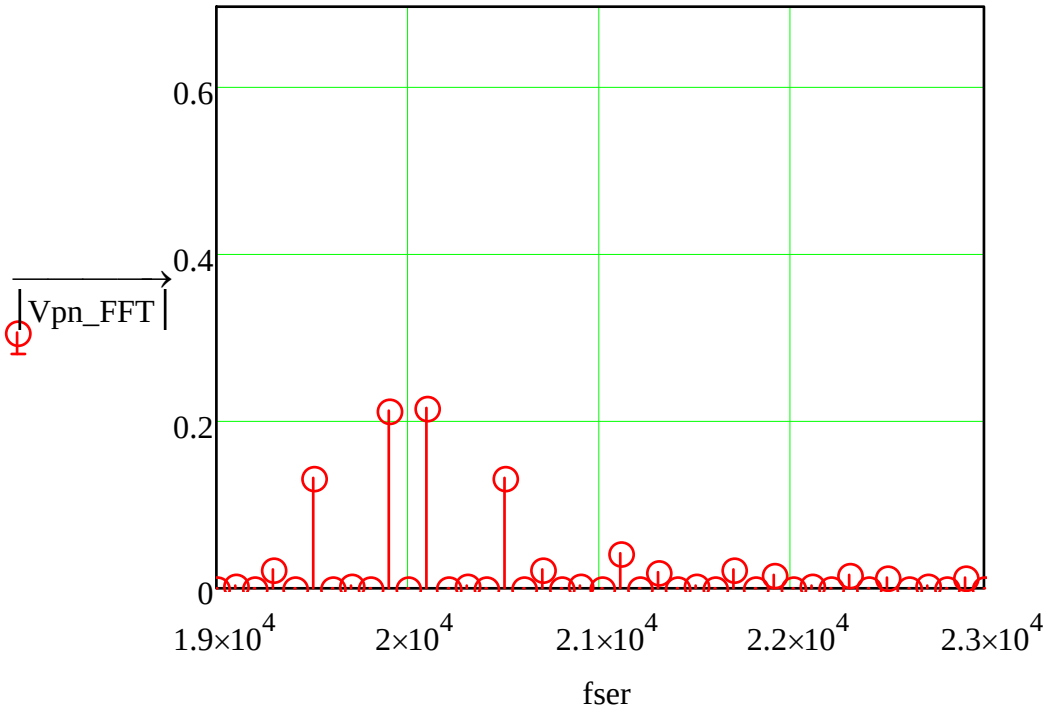


Figure 4.33 (cont'd)



(c) FFT for phase current of DPWM sequence d at m=0.8

$$WTHD = \frac{\sqrt{\sum_{kk=2}^{2^{me-1}-1} \left(\frac{\left|\overrightarrow{V_{pn\_FFTkk}}\right|}{kk}\right)^2}}{\left|\overrightarrow{V_{pn\_FFT1}}\right|} \tag{4.18}$$

$$WTHD\_sequence\_b = 3.607*10^{-3}$$

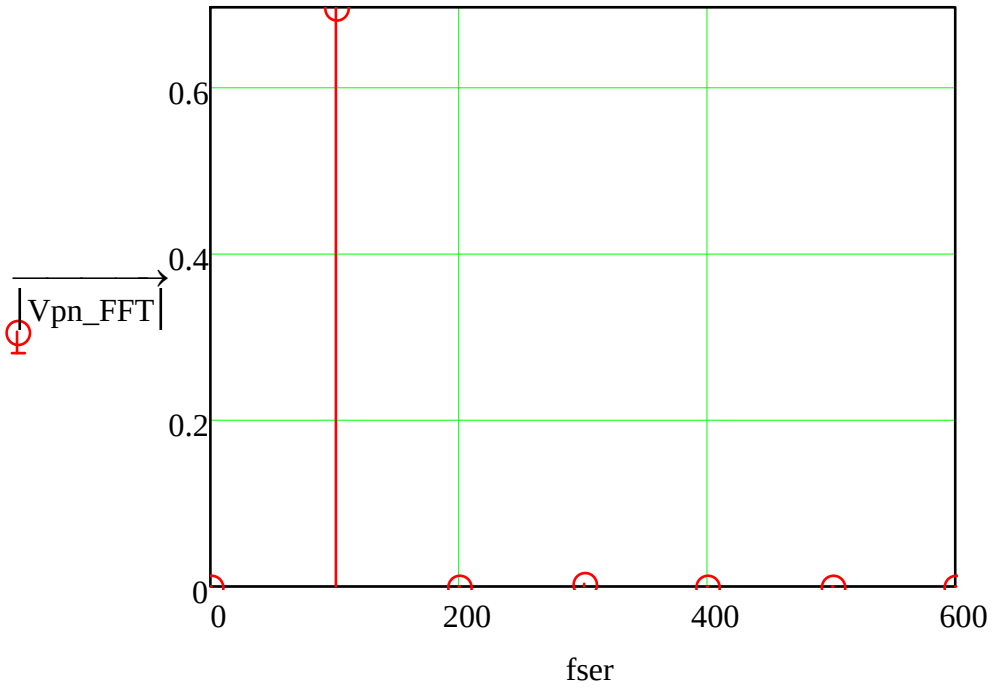
$$WTHD\_sequence\_c = 2.663*10^{-3}$$

$$WTHD\_sequence\_d = 3.306*10^{-3}$$

(2) Continuous SVPWM

According to the selection in Table 4-5, and the sequence in Figure 4.11, the theoretical switching waveforms and also the phase current PWM form can be obtained. Set the parameters as: M=0.8, *fo*=100Hz, *fs*=10kHz. Compared to continuous SVPWM, DPWM only has half fundamental period doing PWM switching. So in order to keep the same average switching frequency, the carrier frequency of continuous SVPWM is set to be half of DPWM,

which is 10kHz here. The spectrum distribution diagrams at fundamental frequency and one and two times switching frequency are shown in Figure 4.34 (a)(b)(c). The WTHD in this case is 0.5107%.



(a)

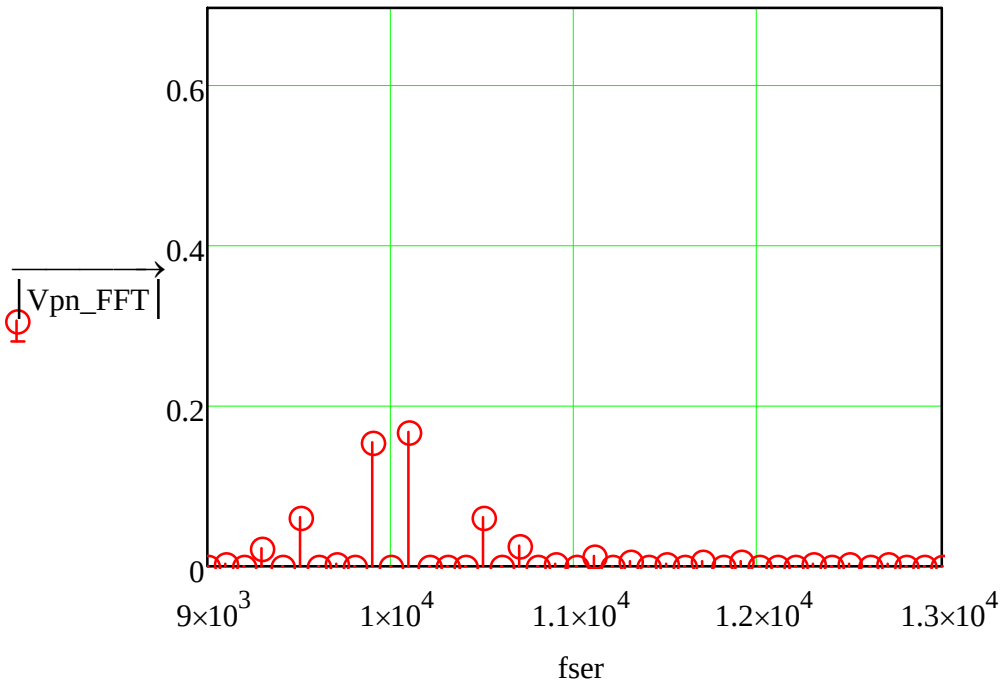
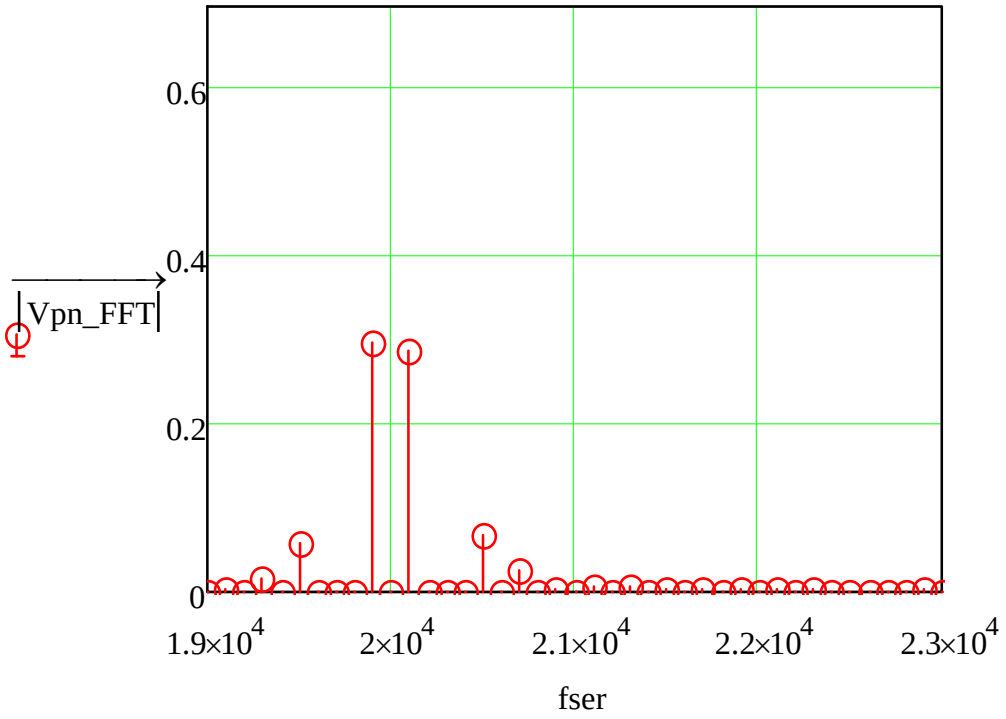


Figure 4.34. Numerical spectrum of phase current for continuous SVPWM at M=0.8

Figure 4.34 (cont'd)



(c)

The output theoretical output line current could be calculated by equation (4.19), which is also shown in Figure 4.35. A FFT analysis is conducted based on this waveform and the results are shown in Figure 4.36.

$$I_a(t) = I_{dc}(t) * (S_1(t) - S_4(t)) \tag{4.19}$$

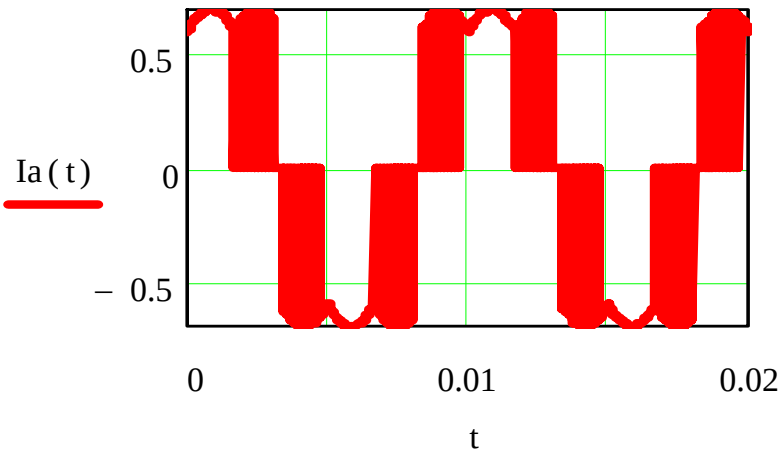
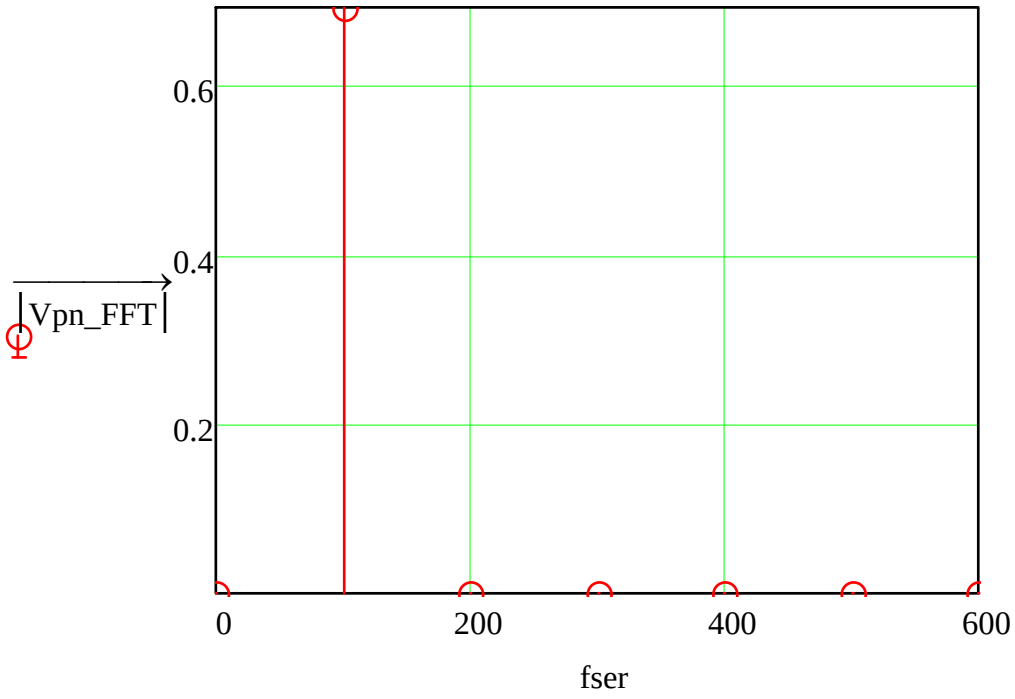


Figure 4.35. theoretical output line current in SVPWAM



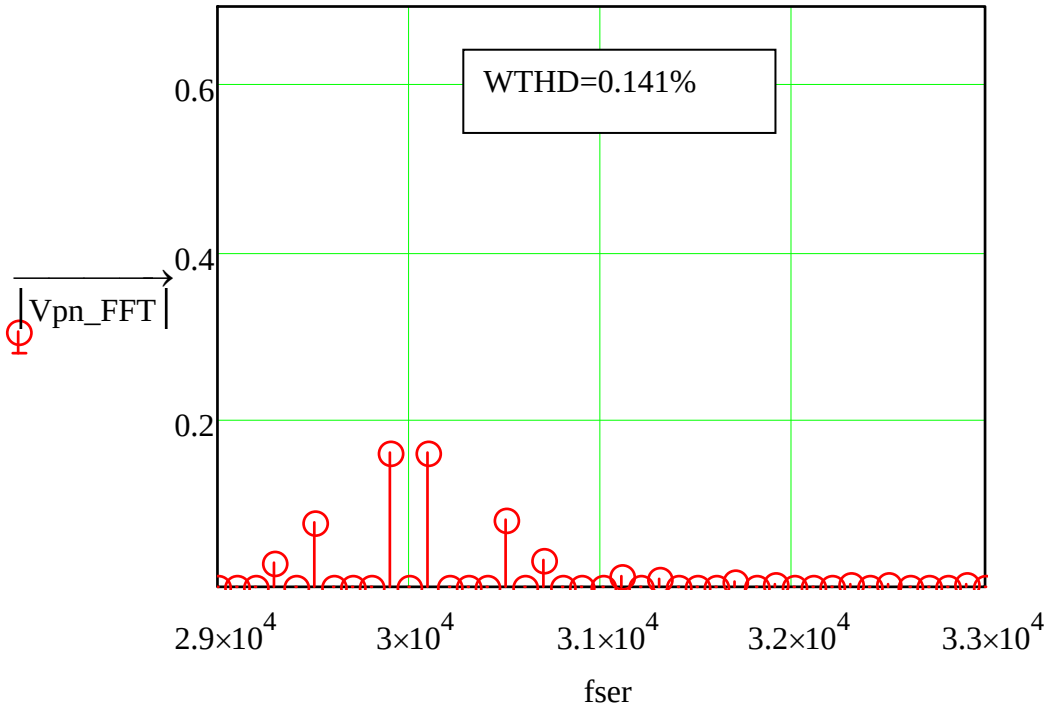


Figure 4.36. Numerical spectrum of output current for SVPWAM

(3) Comparison of WTHD between discontinuous SVPWM, continuous SVPWM and SVPWAM in CSI

The aforementioned three PWM methods for current source inverter can be compared in

THD, by using the same average switching frequency. The DPWM only switches for half cycle, and SVPWAM only switches for 1/3 cycle, but continuous SVPWM switches for the whole cycle. The WTHD presents different value in different modulation index. So Figure 4.37 shows the relationship between WTHD and the modulation index for each method. SVPWAM only has unity M, so it only shows one point. The plot indicates that SVPWAM has the smallest WTHD and DPWM C the second. Continuous SVPWM has the worst harmonic performance.

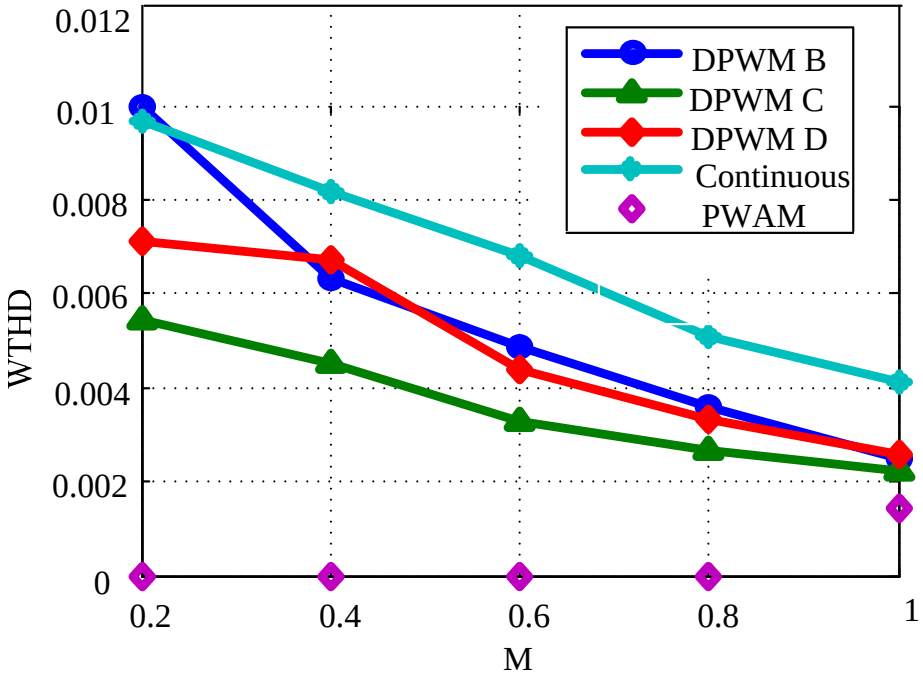


Figure 4.37 WTHD vs. M for different methods

4.4.3. Analytical double Fourier expression for SVPWAM

In VSI, the general expression of double Fourier coefficient is:

$$A_{mn} + jB_{mn} = \frac{1}{2\pi^2} \sum_{1}^{6} \int_{y_s(i)}^{y_e(i)} \int_{x_r(i)}^{x_f(i)} V_{dc} e^{j(mx+ny)} dxdy \qquad (4.20)$$

, where $y \in [0, 2\pi]$ represents the fundamental cycle; $x \in [0, 2\pi]$ represents one switching cycle. Since the PWM waveform for each switch in different sectors are known in Figure

4.19, and also the time for rising edge and falling edge for each switch in each switching cycle can be calculated from (4.8) and (4.9). Thus the double Fourier expression coefficients in (4.20) can then be derived.

The output line to line voltage V_{ab} of a voltage source inverter is used as an illustrative example. It can be expressed using switching functions as follows:

$$V_{ab}(t) = V_{dc}(S_1(t) - S_3(t)) \tag{4.21}$$

So the double Fourier equation for V_{ab} is transferred into the subtraction of double Fourier equation for $S_1(t)$ and double Fourier equation for $S_3(t)$. The integration limits for $S_1(t)$ and $S_3(t)$ are shown in Table 4-6 and Table 4-7, and the corresponding line to line voltage integration limits are shown in Table 4-8.

Table 4-6.Integration limit for switching function $S_1(t)$

i	ys(i)	ye(i)	xr(i)	xf(i)
1	0	$\frac{\pi}{3}$	0	2π
2	$\frac{\pi}{3}$	$\frac{2\pi}{3}$	$x_{r1} = 0;$ $x_{r2} = 2\pi - \pi \cdot \frac{\sin(2\pi/3 - y)}{\sin y}$	$x_{f1} = \pi \frac{\sin(2\pi/3 - y)}{\sin y}$ $x_{f2} = 2\pi$
3	$\frac{2\pi}{3}$	π	0	0
4	π	$\frac{4}{3}\pi$	0	0
5	$\frac{4}{3}\pi$	$\frac{5}{3}\pi$	$x_{r1} = \pi \cdot \frac{\sin(5\pi/3 - y)}{\sin(y-\pi)}$	$x_{f1} = 2\pi - \pi \cdot \frac{\sin(5\pi/3 - y)}{\sin(y-\pi)}$
6	$\frac{5}{3}\pi$	2π	0	2π

Table 4-7.Integration limit for switching function $S_3(t)$

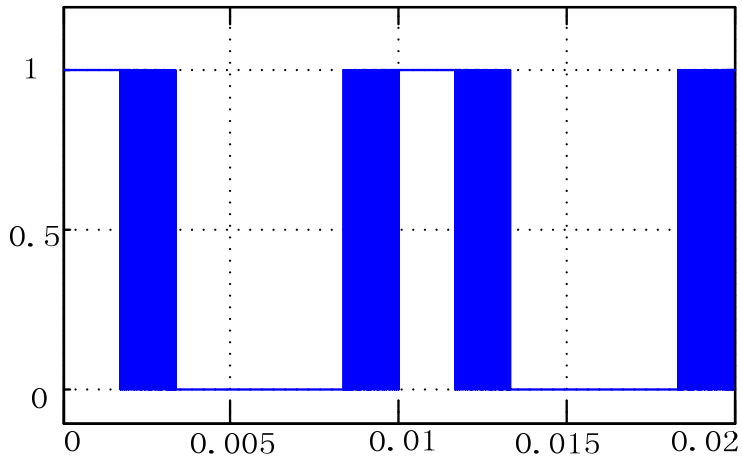
i	ys(i)	ye(i)	xr(i)	xf(i)
1	0	$\pi/3$	$x_{r1}=\pi\cdot\frac{\sin(\pi/3-y)}{\sin(y+\pi/3)}$	$x_{f1}=2\pi-\pi\cdot\frac{\sin(\pi/3-y)}{\sin(y+\pi/3)}$
2	$\pi/3$	$2\pi/3$	0	2π
3	$2\pi/3$	π	0	2π
4	π	$4\pi/3$	$x_{r1}=0;$ $x_{r2}=2\pi-\pi\cdot\frac{\sin(4\pi/3-y)}{\sin(y-2\pi/3)}$	$x_{f1}=\pi\cdot\frac{\sin(4\pi/3-y)}{\sin(y-2\pi/3)}$ $x_{f2}=2\pi$
5	$4\pi/3$	$5\pi/3$	0	0
6	$5\pi/3$	2π	0	0

Table 4-8.Integration limit for line to line voltage $V_{ab}(t)$

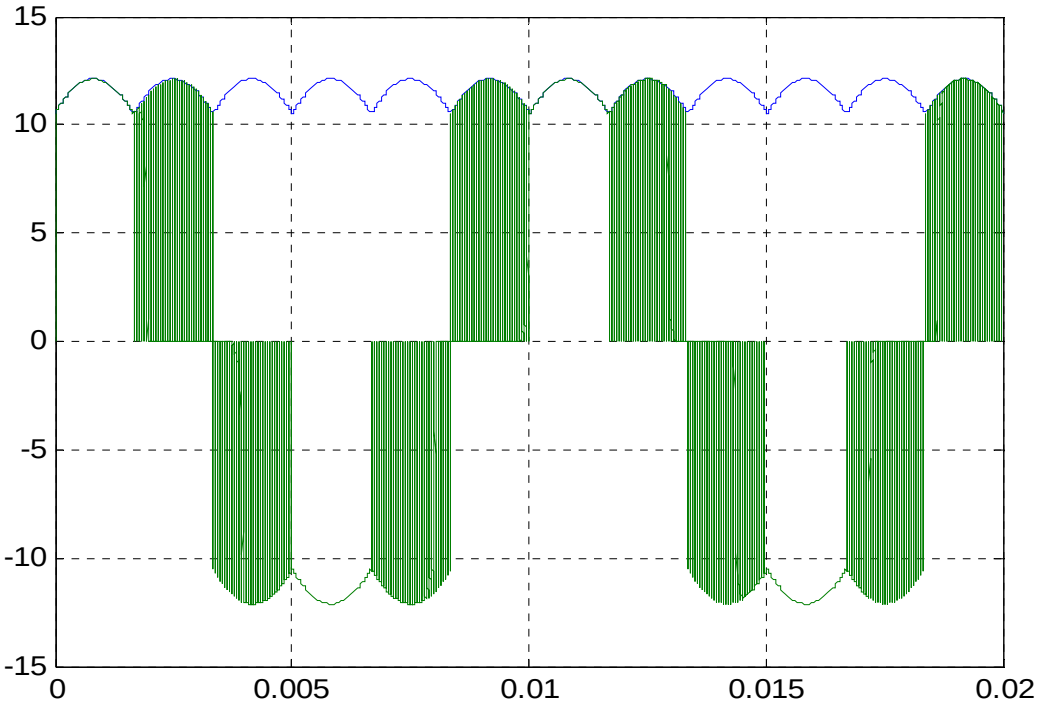
i	*ys(i)*	*ye(i)*	*xr(i)*	*xf(i)*	*Idc*
1	*0*	$\frac{\pi}{3}$	$x_{r1}=0;$ $x_{r2}=2\pi-\pi\cdot\frac{\sin(\pi/3-y)}{\sin(\pi/3+y)}$	$x_{f1}=\pi\cdot\frac{\sin(\pi/3-y)}{\sin(\pi/3+y)};$ $x_{f2}=2\pi$	*1*
2	$\frac{\pi}{3}$	$\frac{2\pi}{3}$	$x_r=\pi\cdot\frac{\sin(2\pi/3-y)}{\sin y}$	$x_r=2\pi\text{-}\pi\cdot\frac{\sin(2\pi/3-y)}{\sin y}$	*-1*
3	$\frac{2\pi}{3}$	π	*0*	2π	*-1*
4	π	$\frac{4}{3}\pi$	$x_{r1}=0;$ $x_{r2}=2\pi-\pi\cdot\frac{\sin(4\pi/3-y)}{\sin(y\text{-}2\pi/3)}$	$x_{f1}=\pi\cdot\frac{\sin(4\pi/3-y)}{\sin(y\text{-}2\pi/3)};$ $x_{f2}=2\pi$	*-1*
5	$\frac{4}{3}\pi$	$\frac{5}{3}\pi$	$x_{r1}=\pi\cdot\frac{\sin(5\pi/3-y)}{\sin(y\text{-}\pi)}$	$x_{f1}=2\pi-\pi\cdot\frac{\sin(5\pi/3-y)}{\sin(y\text{-}\pi)}$	*1*
6	$\frac{5}{3}\pi$	2π	*0*	2π	*1*

The coefficients finally could be simplified into a closed-form expression in terms of Bessel functions, according to the following basic equality

$$e^{j\xi\cos\theta} = J_0(\xi) + 2\sum_{k=1}^{\infty} j^k J_k(\xi)\cos(k\theta) \tag{4.22}$$



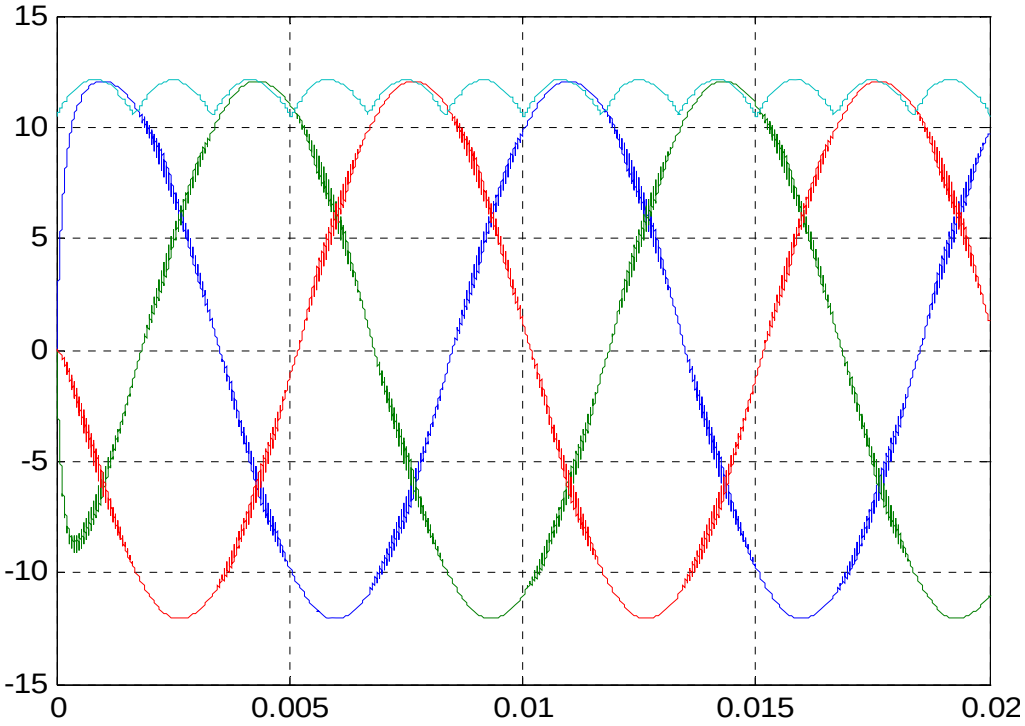
(a)



(b)

Figure 4.38. Simulation results for SVPWAM CSI: (a) switching waveform (b) Input dc link current and output one phase current before the filter (c) input dc link current and output three phase current after the filter

Figure 4.38 (cont'd)



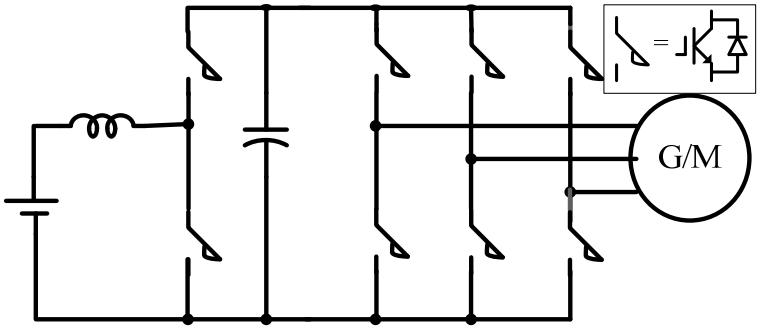
(c)

For current source inverter SVPWAM, the theoretical output line current could be calculated, which is also shown in Figure 4.38 (b) the green waveform. The numerical FFT analysis shown in previous section is conducted based on this waveform

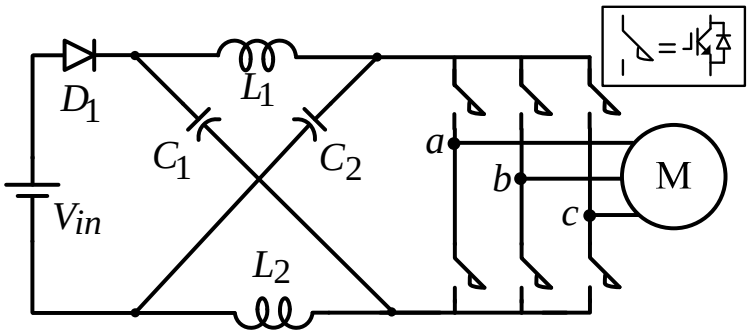
For the theoretical double Fourier Series form derivation for the output current, the same general equation as (4.21) has been adopted, but different integration limits are assigned for SVPWAM. Take S_1 as an example. For sector I, the integration limit for x is $[0, 2\pi]$; for sector III, IV and V, the limit for x is [0,0]; for sector II, the integration limit for x is $[0, 2\pi T_1 / T_s] \& [2\pi - 2\pi T_1 / T_s, 2\pi]$; for sector VI, integration limit for x is $[2\pi T_1 / T_s, 2\pi - 2\pi T_1 / T_s]$. The time range in a certain sector for S_4 is the same with the time range of S_1 in a sector which is 180 apart from the sector of S_4 .The detailed closed-form expression will not be discussed here in detail.

4.4.4. Topologies for SVPWAM

Basically the topologies that can utilize SVPWAM have two stages: dc-dc conversion which converts a dc voltage or current into a 6ω varied dc link voltage or current; VSI or CSI for which SVPWAM is applied. However, the two stage conversion can also be implemented in a single stage in some topologies, such as Z/quasi-Z/trans-Z source inverter. Some examples from these two categories of topologies are shown in Figure 4.39. Topologies (a)(b)(c)(e)(f) are proposed in previous literatures [26-29]. Topology (d) is a newly proposed topology here. These inverters all have voltage buck-boost function. All topologies except (b) have regenerative capability. However, if the front diode in (b) is replaced by an active switch, it can also conduct power in both directions.



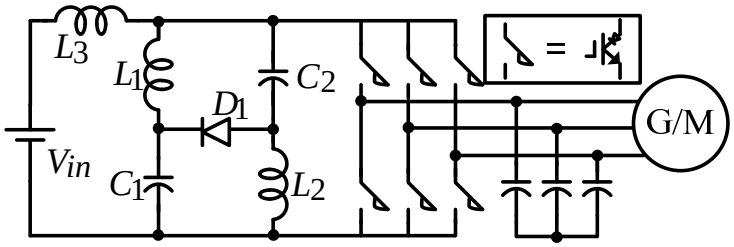
(a) Boost converter inverter



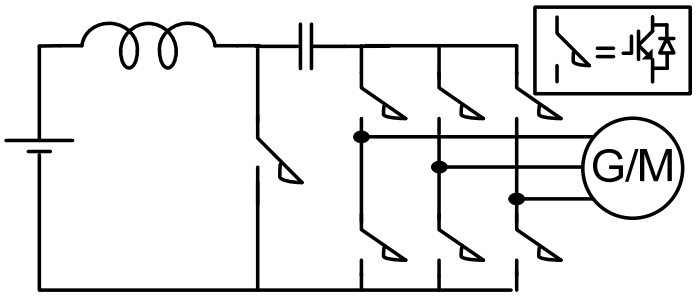
(b) Voltage-fed Z-source inverter [26]

Figure 4.39. Possible topologies for using SVPWAM

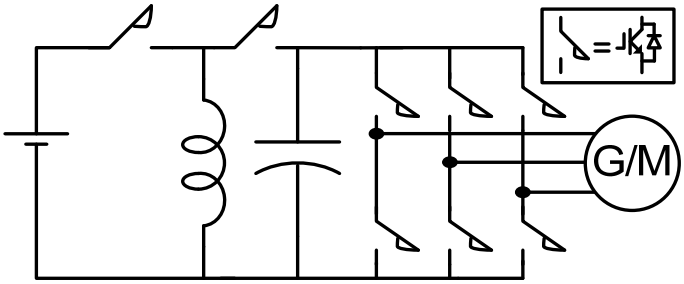
Figure 4.39 (cont'd)



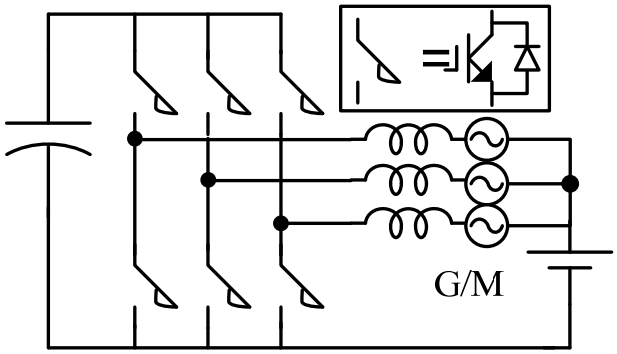
(c) Current-fed quasi-Z-source inverter [27,28]



(d) Buck-boost-inverter



(e) Buck-boost-converter-inverter



(f)Two stage boost converter using the neutral point of motor[29]

4.5. Summary

This section gives the general theory for three PWM modulation methods for current

source inverter. The new contributions of this section over the previous literature are:

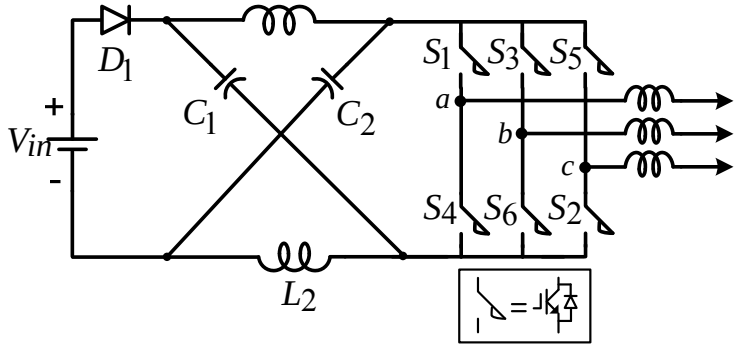
- A SVPWAM method has been proposed for current source inverter, to reduce the switching loss;
- DPWM, CSVPWM and SVPWAM are all derived from SVPWM theory, and their equivalent carrier based modulation has also been derived;
- Double Fourier form of DPWM and SVPWAM have been derived;
- WTHD has been compared for all methods and the conclusion is:

  SVPWAM < DPWM_c < DPWM_d < DPWM_b < CSVPWM;
- The SVPWAM method reduces the switching loss by 90% in VSI, by 70% in CSI at unity power factor condition, thus the power density is increased and the cost is reduced.

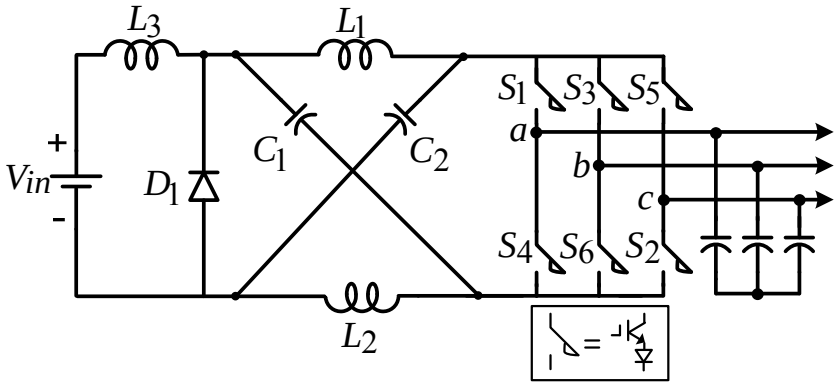
CHAPTER 5 SVPWM FOR Z-SOURCE INVERTER —ZERO VECTOR PLACEMENT

5.1. Introduction

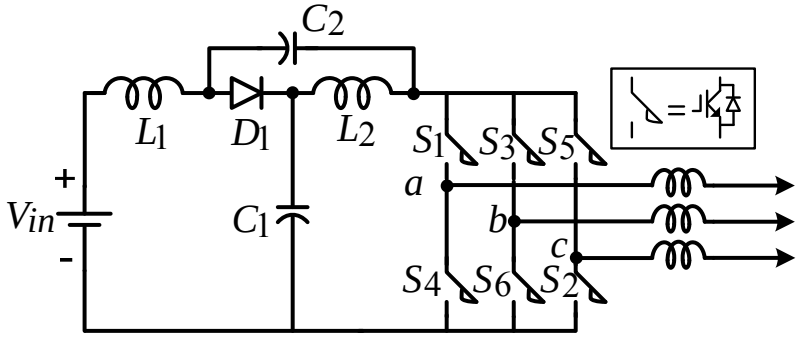
For motor drive application, the Z-source inverter is a promising new inverter to achieve lower cost and higher efficiency, which has been discussed in several papers [1-13]. It can



(a) Voltage-fed Z-source inverter



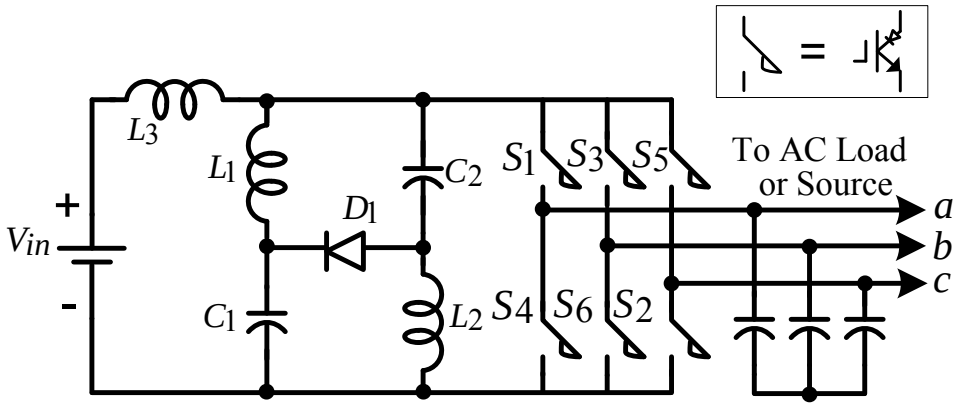
(b) Current-fed Z-source inverter



(c) Voltage-fed quasi-Z-source inverter

Figure 5.1. Circuit configurations of Z-Source inverter

Figure 5.1 (cont'd)



(d) Current-fed quasi-Z-source inverter

buck/boost voltage in a single stage, which overcomes the efficiency problem of the traditional two stage boost converter inverter solution.

There are many kinds of modulation methods for current source inverter and voltage source inverter proposed previously. There are two basic types of modulation methods: carrier based regular sampled method (including continuous PWM [18-23] and discontinuous PWM[24-28]); space vector PWM control [27, 29-31]. Paper[22] utilized master and slave references to be compared with carrier directly to generate a switching pattern instead of using mapping method [20], but it didn't reduce switching frequency or increase current utilization compared to SVPWM control. Paper[26] proposed two generalized discontinuous carrier-based pulse width modulation (GDPWM) methodologies for CSI to reduce the switching frequency further by 1/3. However, the discontinuous PWM introduces higher harmonics in the output and also higher temperature variation of the device package. paper[28] presented a vector PWM method to minimize the switching loss, by placing zero vector at proper sector and by injecting triplet harmonics. Similarly for current source inverter, the zero vectors can be intentionally arranged to bring down the switching loss. Paper[24] presented a dead-band PWM pattern which makes a 33% switching frequency reduction for a equivalent harmonic spectrum, compared to SPWM, but it has the same

problem as DPWM. Paper[34] concluded that the third harmonic injection method is better for low modulation but modified SPWM is better for high modulation in terms of harmonic and ripple current.

Various types of Z-source inverter modulation have also been proposed in the old literatures. Papers [1, 4, 32-33] proposed the carrier-based PWM control method. Paper [4] presented a method utilizing the maximum shoot through duty ratio in order to achieve minimum voltage stress on active devices; however, the varied shoot through duty cycle may introduce six times base frequency harmonics in output. In order to overcome this problem, paper [32] proposed a maximum constant boost control which injects a zero sequence voltage in the reference to make the shoot through duty cycle constant. Papers [1, 33] presented a method which inserts the open zero state into the edge of PWM, in order to reduce the number of switching, however, it may cause larger power loss due to multiple times of diode reverse recovery.

The evaluation process for different modulation methods has been researched by many papers [27, 35-38]]. Basically the evaluation criteria includes switching losses[84, 27, 28, 38-40], current/voltage ripple[34], harmonics[29, 36, 41, 42] and implementation complexity.

PWM sequence is defined as a function of modulation index and power factor. From the state average point of view, each switching vector can be displaced anywhere within the switching cycle because the displacement has no effect on the amp-second average of the resulting current pulses corresponding to the reference vector[39]. The sequence of switching vectors should minimize the inverter switching loss, inductor current ripple and output voltage/current harmonics[31].

Paper[39] presented several kinds of switching sequences such as FSM, HSM, MHSM, MFSM, CSVM, and also concluded that CSVM is better than others if $M<0.64$.

This paper selects the SVPWM control to achieve higher input current utilization, lower

switching loss and lower total harmonic distortions. For both voltage-fed and current-fed Z-source inverter, there are four switching states at any switching cycle, including two active states, one short zero state (shoot through state in voltage-fed Z-source inverter), and one open zero state. So there is more flexibility to arrange them to get the same volt-second equation, but different performance. In the modified SVPWM control method for this circuit, different PWM sequences can lead to different switching loss, current ripple, total harmonic distortion, and also the voltage spike on the switching devices. For each optimizing target, several rules which results in better performance have been summarized. A group of sequences have been sieved according to these rules. A complete analysis has been given to demonstrate the performance of the selected sequence based on aforementioned four criterions. A 15kW rated current-fed quasi-Z-source inverter has been built in the lab. This inverter has buck-boost and regenerative function [81]. Space vector PWM with optimized vector placement has been utilized on the hardware. In order to bring the prototype into real application in hybrid electrical vehicle[82-84], the inverter efficiency is measured according to the motor P-V curve. The estimated efficiency curve and experiment results are plot and compared. The best efficiency at full power rating reaches 97.6% at unity voltage gain. The peak efficiency reaches 98.2%. The efficiency from 3.5KW to 15KW is between 94% and 98%. Compared to two stage boost-converter-inverter in traditional HEV system, the efficiency has been improved by 3-4%. The power density of the 15kW prototype is around 15.3KW/L, which is also 5KW/L higher than the commercial unit in HEV.

5.2. The Influence of Zero Space Vector Placement

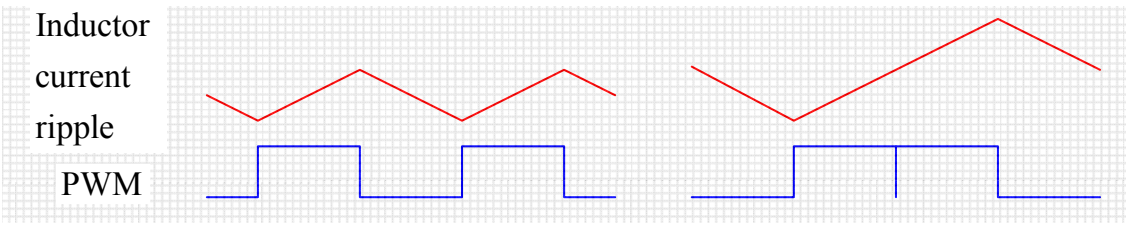


Figure 5.2 Centered PWM and back to back PWM and their corresponding current ripple

The main function of any PWM strategy is to identify the active pulse width within each carrier interval which contributes the same fundamental volt-second average as the original target reference waveform over that interval. While the position of the pulse within the carrier interval does not affect its cumulative volt-second average over that interval, it does significantly influence the harmonic performance of the switched output voltage. This is illustrated in Figure 5.2, which shows two possible pulse placements for a 50% duty cycle switched voltage applied to an inductive load which has a back electromotive force (EMF) equal to half the switched voltage. While the average current is zero in both cases, the current ripple magnitude when the pulses are centered in the carrier interval is significantly less than the current ripple magnitude which occurs when the pulses are positioned back to back to span across two carrier intervals. Furthermore, when the switched pulses are centered in each carrier interval, the current ripple frequency is twice that of the back to back pulse placement (this reflects the switched output voltage harmonics seen by the load in both cases). The conclusion to be drawn from this simple example is that modulation strategies which place their switched pulses closer to the center of each carrier interval have a superior harmonic performance compared to those which do not center the pulses, irrespective of how the switched pulse width is calculated. For a three-phase system, the placement of the active voltage pulses is constrained by the need to balance the pulse position across all three phases. From the way of how the active voltage pulses are distributed within a carrier period for the first 120 degree of the fundamental component, for regular sampled PWM, PWM+3rd harmonic injection, and space vector modulation where the active space vectors have been explicitly centered in each half carrier interval, it can be seen how the progression from regular PWM through third harmonic injection to space vector modulation progressively centers and improves the voltage pulse placement.

An alternative modulation strategy which also achieves an improved pulse placement is

to add a common mode third harmonic of 1/4 reference magnitude, instead of 1/6 as described before. This approach centers the space vector pulses at 30 degree steps during the fundamental cycle, with minor deviations from the center within each 30 degree interval. Note however that the maximum possible modulation range without saturating is slightly reduced to $0<m'<1.12$ under this modulation strategy.

It would be expected that the improved voltage pulse placement achieved by space vector modulation would be reflected in the harmonic spectrum of the line to line voltage, with an increase in the spectral energy at twice the switching frequency and lower harmonic components at the switching frequency. Furthermore, only a slight improvement would be anticipated when moving from third harmonic injection PWM to space vector modulation, twice the position of the active space vectors only varies slightly between these two approaches. These responses have been verified by both simulation and experiment as described in the next section.

Finally, the benefit of centering the active space vectors should diminish as the modulation depth increases, since a larger part of the carrier interval becomes taken up with the active space vector components, and the position skew caused by the constraints of three-phase pulse placement overshadow any benefits of centering the active pulses.

5.3. Consequential modulation Implementation Issues

Once the active space vectors have been identified, they can be placed and sequenced in a number of ways which trade harmonic performance against implementation complexity.

One obvious alternative is to not reverse the switching sequence every half cycle, i.e., to replace the space vector sequence of S0-S2-S1-S7-S7-S1-S2-S0 by S0-S2-S1-S7-S0-S2-S1-S7. This can achieve some simplicity in hardware implementation, but has the cost of changing the modulation process to single edged (sawtooth carrier) with a resulting increase in harmonic levels. In addition, this type of modulation implementation for

regular sampled systems creates 2^{nd} and 4^{th} harmonics of approximately 1% (the magnitude depends on the switching frequency), and this is generally unacceptable. Single-edged space vector modulation is therefore not recommended.

Another alternative that has been reported is to combine the two zero space vectors into one interval which is placed at the end or the start of the half carrier interval for the forward or reverse switching sequence, respectively. This sequence allows each phase leg to stay switched on for 60 degree or 120 degree continuously, depending on which zero vectors are combined. The switching sequence then becomes (for one 60 degree segment) S2-S1-S7-S7-S1-S2 while phase leg C is held at –Vdc during this period. The advantage of this discontinuous implementation is that the overall switching frequency can be increased by 3/2, while still maintaining the same overall number of phase leg commutations as for regular PWM and centered space vector modulation. However, the price is a loss of symmetry for each line to line output voltage, which is reflected in the harmonic spectrum for this implementation.

At higher modulation ratios, the benefits of the double switching frequency harmonics for centered space vector modulation lessen as the active space vector regions within the half carrier interval increase, and discontinuous modulation becomes more attractive because of its higher net switching frequency. The weighted THD of regular PWM+3^{rd} and centered space vector modulation are almost identical over the entire linear modulation range, while 60 degree discontinuous modulation achieves a lower weighted THD above a modulation depth of about 0.9.

5.4. Effect of Zero Vector Placement For SVPWM of Voltage-fed Z-source Inverter

5.4.1. SVPWM control method for voltage-fed Z-source inverter

Figure 5.3 shows the SVPWM diagram for voltage-fed Z-source inverter. There is an extra shoot through state introduced except the normal zero states. In each sector, two normal

zero states and one shoot through state are selected. The shoot through state is corresponding to turning on all the switches, in order to achieve minimum current stress on the switch. Figure 5.4 shows three basic circuit states in one switching interval. The corresponding conducting time of each vector follows the equations:

$$
\begin{aligned}
T_1 &= \frac{2}{\sqrt{3}} m \sin(60^0 - \theta) \cdot T_s \\
T_2 &= \frac{2}{\sqrt{3}} m \sin(\theta) \cdot T_s \\
T_0 &= T_7 = \frac{1}{2}(T_s - T_i - T_{i+1} - T_{sh})
\end{aligned}
\tag{5.1}
$$

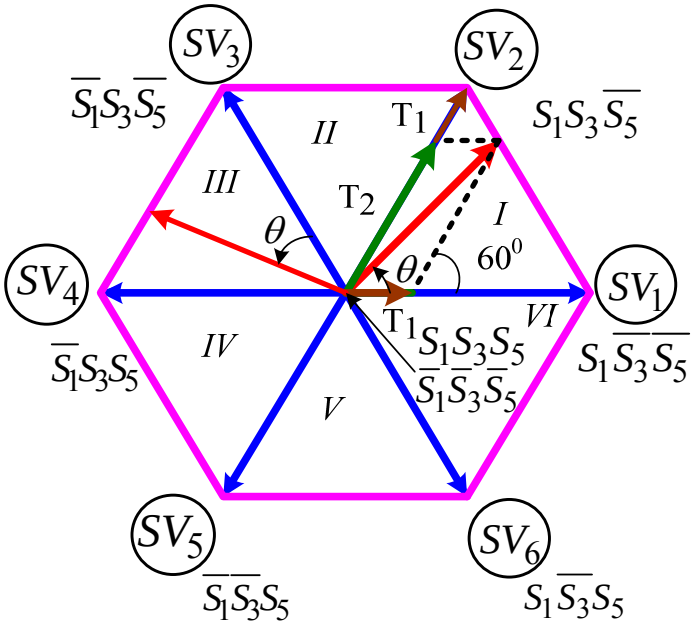
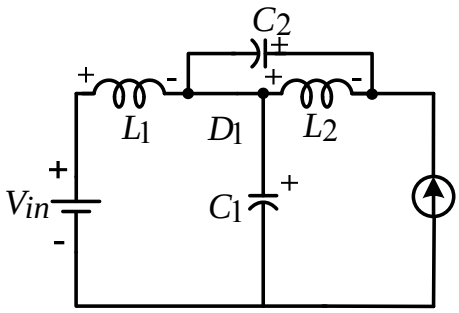


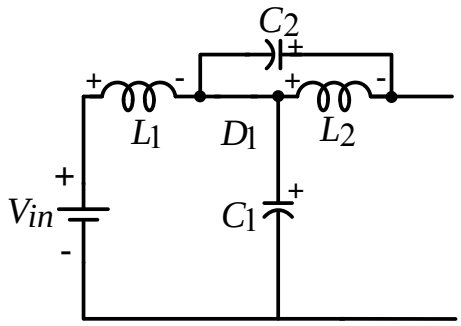
Figure 5.3. SVPWM control for voltage-fed Z-source inverter



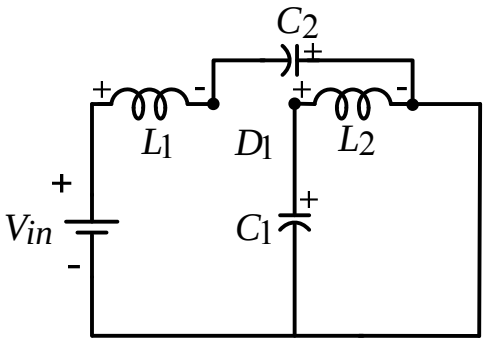
(a) Active state (T_1, T_2)

Figure 5.4. Three equivalent circuit states for voltage-fed quasi-Z-source inverter

Figure 5.4 (cont'd)



(b) Open zero state (T_0, T_7)



(c) Shoot through state (T_{sh})

Figure 5.4. Three equivalent circuit states for voltage-fed quasi-Z-source inverter

5.4.2. Vector placement for SVPWM control of voltage-fed Z-source inverter

Five vectors appear in SVPWM control of voltage-fed Z-source inverter, including two active vectors and three zero vectors.

If all the zero vectors are utilized in a single switching interval, the vector arrangement complexity is raised from O(4) in normal case to O(5). Six different sequences have been summarized in Figure 5.5, after deleting some of the overlapped choices.

The corresponding relationship is:

$$t0 = S_1S_3S_5,\quad t7 = \overline{S_1}\,\overline{S_3}\,\overline{S_5},\quad t1 = S_1\overline{S_3}S_5,\quad t2 = S_1\overline{S_3}\,\overline{S_5}, t_{sh} = S_1S_2S_3S_4S_5S_6$$

Thus in all these sequences, there are several types of transition as follows:

$$t0 \Leftrightarrow t1,\quad t1 \Leftrightarrow t2,\quad t2 \Leftrightarrow t7, t0 \Leftrightarrow t7, t0 \Leftrightarrow t2, t7 \Leftrightarrow t1, tsh \Leftrightarrow t1,$$
$$tsh \Leftrightarrow t2, tsh \Leftrightarrow t7, tsh \Leftrightarrow t0$$

They can be classified into groups by the number of switching action in the transition: only one switching action includes $t0 \Leftrightarrow t1$, $t1 \Leftrightarrow t2$, $t2 \Leftrightarrow t7$; one and half switching actions include $tsh \Leftrightarrow t1, tsh \Leftrightarrow t2$, $tsh \Leftrightarrow t0, tsh \Leftrightarrow t7$;two switching actions include $t0 \Leftrightarrow t2, t7 \Leftrightarrow t1$; three switching actions include $t7 \Leftrightarrow t0$.

1	t0	t1	t2	t7	tsh	tsh	t7	t2	t1	t0
2	t0	t1	t2	tsh	t7	t7	tsh	t2	t1	t0
3	tsh	t1	t2	t0	t7	t7	t0	t2	t1	tsh
4	tsh	t1	t0	t2	t7	t7	t2	t0	t1	tsh
5	t0	t1	tsh	t2	t7	t7	t2	tsh	t1	t0
6	t0	t1	tsh	t2	t7	t0	t1	tsh	t2	t7

Figure 5.5. Six sequences of the vector placement for SVPWM of voltage-fed Z-source inverter

1	t0	t1	t2	t0	tsh	tsh	t0	t2	t1	t0
2	t0	t1	t2	tsh	t0	t0	tsh	t2	t1	t0
3	tsh	t1	t2	t0	t0	t0	t0	t2	t1	tsh
4	tsh	t1	t0	t2	t0	t0	t2	t0	t1	tsh
5	t0	t1	tsh	t2	t0	t0	t2	tsh	t1	t0
6	t0	t1	tsh	t2	t0	t0	t1	tsh	t2	t0

Figure 5.6. Discontinuous vector placement sequence for SVPWM of voltage-fed Z-source inverter

Therefore the first sequence in Figure 5.5 is labeled as the one with least number of switching. However, least number of switching is not equalized to least current ripple, least switching loss and least harmonics. The fair comparison should have all the criterions fixed except one varied. First of all, the inductor current ripple caused by different sequences should be guaranteed to be the same, because it will affect the inductor size and efficiency. Secondly, the output current harmonics should be kept the same, in order to provide the same quality of power to the load. Based on these assumptions, the one with the minimum switching loss could be defined as the optimized placement sequence.

5.4.3. Effect of vector placement for current ripple

The inductor current ripple is affected by the vector placement. As shown in Figure 5.2, an alternative placement for two different types of zero vector(shoot through zero vector and open zero vector) would reduce the current ripple amplitude to half , and also increases the ripple frequency to twice, compared to the one without alternative consequence. Take voltage-fed quasi-Z-source inverter as an example to explain here. Inductor 2 is considered as the research object since it is directly clamped by capacitor 2 active and open zero state and by capacitor 1 in shoot through state. According to the circuit states in Figure 5.4, inductor 2 is charged in shoot through state and discharged in the other two states, so as inductor 1. Since the capacitor voltage is stiff, the discharge rate in active and open zero state are the same, but much smaller than the charge rate in shoot through state. This phenomenon could be explained from the energy storage point of view. All the energy dissipated in the long active and normal zero state has to be restored in a short period of shoot through state. It results in an excessively big shoot through current ripple. Sequences 2, 5, 6 in Figure 5.5 reduce the ripple to half of the original by dividing the shoot through period into two equal ones. In another word, sequences 1, 3, 4 have to double their switching frequency to reach the same ripple level as the other group of sequences. From this stand point, sequences 2, 5, 6 are considered to have much less switching actions, thus less switching loss, at the same current ripple premise.

5.4.4. Effect of vector placement for output harmonics

First of all, the sequences with smaller current amplitude and higher current ripple frequency would have lower THD at output. The reason is the output current is equal to inductor current in active state, since the high frequency capacitor current component is filtered out by the output filter. Different placement brings different inductor current shape, thus different output current shape. Thus sequence 2, 5, 6 have lower THD than the other

three placement.

Second, the modulation strategies which place their switched pulses closer to the center of the each half carrier interval have a superior harmonic performance compared to those which do not center the pulses, irrespective of how the switched pulse width is calculated [31]. The improvement would also be reflected in the harmonic spectrum of the line to line voltage, with an increase in the spectral energy at twice the switching frequency and lower harmonic components at the switching frequency [31]. In Figure 5.5, obviously sequence 4,5,6 have more centered active states than the other three. This benefit of centering the active space vectors increases as the modulation depth decreases, since a smaller part of the carrier interval becomes taken up with the active space vector components.

Third, the single edged (sawtooth carrier) PWM possesses higher harmonics than the symmetrical PWM. For example in Figure 5.5, sequence 6 is not recommended. This type of modulation implementation for regular sampled systems creates unacceptable 2^{nd} and 4^{th} harmonics.

In conclusion, sequence 5 is marked to generate lowest harmonics among the six. In addition, there is an alternative is to combine the two zero vectors into one interval, which is placed at the end or the start of the half carrier interval for the forward or reverse switching sequence, respectively, similarly to discontinuous PWM(DPWM). Figure 5.6 shows the six DPWM corresponding to the six continuous PWM in Figure 5.5. The advantage of this DPWM is the number of switching is reduced since one phase leg keeps continuous on or off in normal active or open zero state. The difference between DPWM for Z-source inverter and normal DPWM is that 60 degree or 120 degree no switching of one phase leg doesn't exist any more, because all the switches need to be turned on in shoot through state. In addition, the loss of symmetry for each line to line output voltage in DPWM causes higher THD. Only when the modulation goes high, the benefits of double switching frequency harmonics for

centered space vector modulation lessen as the active space vector regions within the half carrier interval increase. DPWM presents lower THD than the continuous PWM.

There are two methods to evaluate the spectrum performance. One is through analytical double Fourier analysis of the output PWM waveform. Another is numerically calculation of the PWM spectrum. The second method is adopted here. The weighted THD (WTHD) is the final divide to classify the different placement, which is defined here:

$$WTHD = \frac{\sqrt{\sum_{kk=2}^{N}\left(\frac{\left|V_{FFT_{kk}}\right|}{kk}\right)^2}}{V_{FFT_1}} \tag{5.2}$$

WTHD is a relative THD which considered the effect of the harmonic frequency. The higher the harmonic frequency is, the less important of that affects the total THD. Thus a weighting factor $1/kk$ is included in equation (2). The research object is output line to line voltage before the filter, which is the PWM type, because it can eliminate the effect of output filter design. For voltage type inverter, this variable is equal to the subtraction of the switching function on the same half leg. For example, V_{ab} is equal to dc link voltage times $(S_1(t) - S_3(t))$. According to above mentioned three rules, sequence 5 is the optimized sequence, which can be further demonstrated by the spectrum later.

5.5. Space Vector Control of Current-fed Z-source Inverter

5.5.1. SVPWM control method for current-fed Z-source inverter

The modulation of current-fed qZSI is still based on the SVPWM of conventional CSI, but change the zero state into three short zero state and one extra open zero state, as shown in Figure 5.7. In current-fed quasi-z-source inverter, there is one extra open zero state except nine conventional switching states as shown in Figure 5.8. For the output, this extra state is still zero state, which means the output current is zero in this case. It is the same as the state occurring in traditional short zero state. So as long as this extra open zero state is assigned

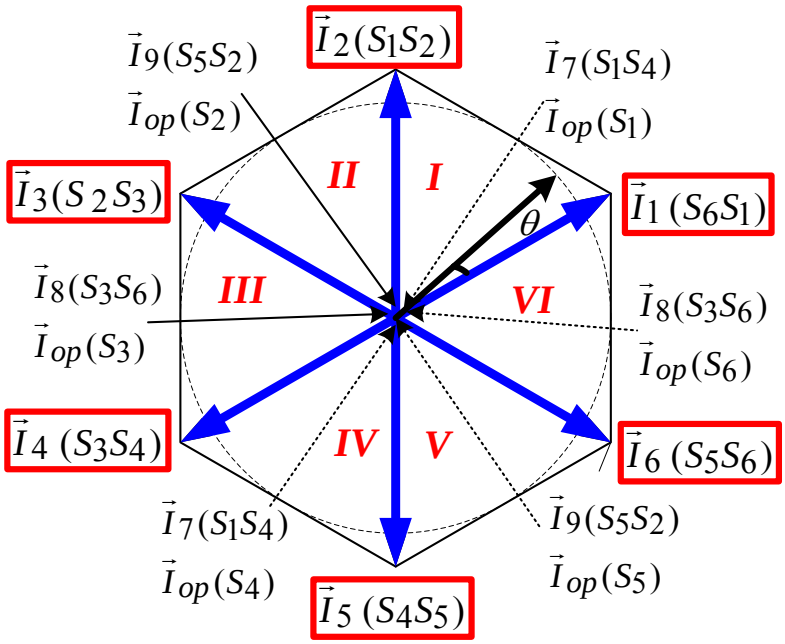
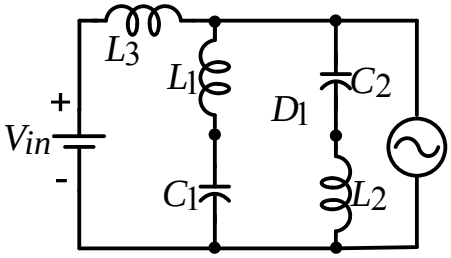
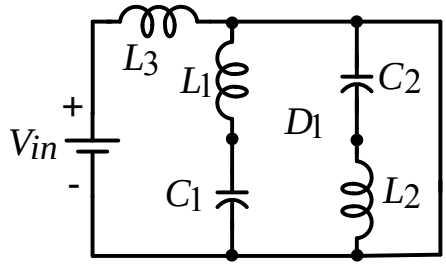


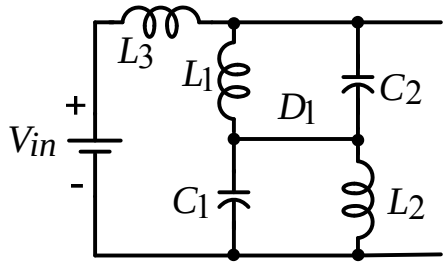
Figure 5.7. Control diagram of space vector PWM method (SVPWM)



(a) Active state



(b) Short zero state



(c) Open zero state

Figure 5.8. Three basic circuit states of current-fed quasi-Z-source inverter

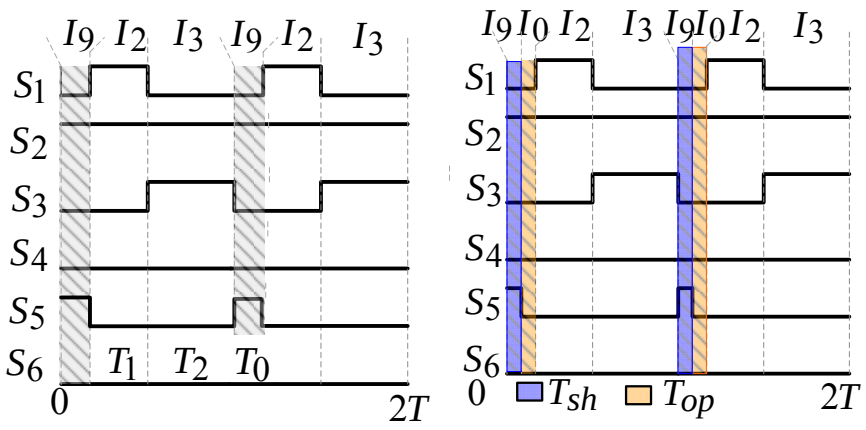


Figure 5.9. Modified discontinuous SVPWM in one switching period in sector III

Table 5-1.Current-fed QZSI governing equations

Variables	$\frac{I_{L1,L2}}{P/V_{IN}}$	$\frac{I_{L3}}{P/V_{IN}}$	$V_{C_{1,2}}$	$V_{L1,2,3}$	
Expression	$\frac{D_{op}}{1-2D_{op}}$	*1*	V_{IN}	$V_{PN}-V_{C1}$	
Variables	$\frac{I_{C1}}{P/V_{IN}}$	$\frac{I_{PN}}{P/V_{IN}}$	$\frac{I_D}{P/V_{IN}}$	V_D	V_{out}/V_{in}
Expression	$\frac{D_{op}}{1-2D_{op}}$ $-S_D*\frac{1}{1-2D_{op}}$	$\overline{S_D}*\frac{1}{1-2D_{op}}$	$S_D*\frac{1}{1-2D_{op}}$	$V_{C1}+V_{C2}$ $-V_{PN}$	$\frac{1-2D_{op}}{D_A}$

Table 5-2.Control parameters and gain for current-fed QZSI

T_1	T_2	T_{sh}
$\frac{\sqrt{3}}{2}m\sin(\frac{\pi}{3}-\theta)\cdot T_s$	$\frac{\sqrt{3}}{2}m\sin(\theta)\cdot T_s$	$1-T_1-T_2-T_{op}$
$\overline{D_A}$	$\overline{V_{out}}/V_o$	V_o/V_{in}
$\frac{3}{\pi}\int_0^{\frac{\pi}{3}}\frac{T_1+T_2}{T}d\theta$ $=3\sqrt{3}m/(2\pi)$	$(\frac{\pi}{3}\int_0^{\frac{\pi}{3}}\frac{T_1v_{ab}+T_2v_{ac}}{T_1+T_2}d\theta)/V_o$ $=\sqrt{2}\pi\cos\phi/2$	$\frac{2\sqrt{2}\pi-2\sqrt{2}k(2\pi-3\sqrt{3}m)}{3\sqrt{3}\pi m\cos\phi}$ $(k=\frac{1-D_{op}}{D_A})$

within the period that the normal short zero state should happen, it will not affect the output.

Therefore, the control method here is to replace part of short zero state with open zero state, as shown in Figure 5.9.

The governing equations, control parameters and voltage gain are shown in Table 5-1 and Table 5-2.

In order to obtain the value of open zero duty cycle, the relationship between output ac rms voltage and input voltage should be expressed as a function of modulation index and open zero duty cycle. The analysis process is shown in chapter 3 section 3.1.3 and 3.1.4.

After the T_{op} and T_1, T_2 value are fixed, the left part in the switching period is assigned to short zero state T_{sh}. They satisfy the following relationship:

$$\begin{aligned} T_0 &= T_{sh} + T_{op} \\ T_{sh} &= T - T_1 - T_2 - T_{op} = (1 - \frac{\sqrt{3}}{2} m \sin(\theta) - D_{op})T \end{aligned} \tag{5.3}$$

5.5.2. Vector placement for SVPWM control of current-fed Z-source inverter

In current-fed Z/quasi-Z source inverter, there are four pre-calculated time period in one switching cycle: active state period t_1, active state period t_2, short zero state period t_0 and open zero state period *top*. Those time period relate PWM waveforms, here called $PWM\_T_0, PWM\_T_1, PWM\_T_2$ should be assigned to different switches in different sectors, according to the switching state selection in different sectors. The relative position of the four time related PWM within one switching cycle can be random because it does not affect the volt-sec product of one cycle. However, it affects the switching loss, inductor current ripple and also the output PWM current harmonics. Nineteen basic switching sequences have been summarized as shown in Table 5-4. They are divided into three groups according to coupled inductor current ripple introduced by different sequences.

Table 5-3.Average and ripple current for input branches

		Average I	*Ripple I(p2p)*
L_{in}	*Boost*	I_{in}	$\frac{1}{L}\cdot T_s(1-\frac{3}{4}m)\cdot V_{in}$
	Buck	I_{in}	$\frac{1}{L}\cdot T_s(1-\frac{\sqrt{3}}{2}m)\cdot V_{in}$
L_Z	*Boost*	0	$\frac{1}{L}\cdot T_s(1-\frac{3}{4}m)\cdot V_{in}$
	Buck	$\frac{D_{op}}{1-2D_{op}}\overline{I_{in}}$	$\frac{1}{L}\cdot T_s(1-\frac{\sqrt{3}}{2}m)\cdot V_{in}$
DC Link	*Boost*	$\overline{I_{in}}$	$\frac{3}{L}\cdot T_s(1-\frac{3}{4}m)\cdot V_{in}$
I_{pn}	*Buck*	$\frac{1}{1-2D_{op}}\overline{I_{in}}$	$\frac{3}{L}\cdot T_s(1-\frac{\sqrt{3}}{2}m)\cdot V_{in}$

Table 5-4.Nineteen Switching Sequences for CF-QZSI SVPWM control

I.A	t_0		t_{op}		t_1		t_2		t_0		t_{op}		t_1		t_2		
I.B	t_{op}		t_0		t_1		t_2		t_{op}		t_0		t_1		t_2		
I.C	t_0		t_1		t_{op}		t_2		t_0		t_1		t_{op}		t_2		
II.A	t_{op}	t_0	t_1	t_2	t_2	t_1	t_0	t_{op}	t_{op}	t_0	t_1	t_2	t_2	t_1	t_0	t_{op}	
II.B	t_0	t_{op}	t_1	t_2	t_2	t_1	t_{op}	t_0	t_0	t_{op}	t_1	t_2	t_2	t_1	t_{op}	t_0	
II.C	t_0	t_1	t_{op}	t_2	t_2	t_{op}	t_1	t_0	t_0	t_1	t_{op}	t_2	t_2	t_{op}	t_1	t_0	
II.D	t_0	t_1	t_2	t_{op}	t_{op}	t_2	t_1	t_0	t_0	t_1	t_2	t_{op}	t_{op}	t_2	t_1	t_0	
II.E	t_{op}	t_1	t_0	t_2	t_2	t_0	t_1	t_{op}	t_{op}	t_1	t_0	t_2	t_2	t_0	t_1	t_{op}	
II.F	t_1	t_{op}	t_0	t_2	t_2	t_0	t_{op}	t_1	t_1	t_{op}	t_0	t_2	t_2	t_0	t_{op}	t_1	
II.G	t_0	t_m	t_1	t_2	t_{op}	t_2	t_1	t_m	t_0	t_0	t_m	t_1	t_2	t_{op}	t_2	t_1	t_m	t_0
II.H	t_0	t_1	t_m	t_2	t_{op}	t_2	t_m	t_1	t_0	t_0	t_1	t_m	t_2	t_{op}	t_2	t_m	t_1	t_0
II.I	t_1	t_0	t_m	t_2	t_{op}	t_2	t_m	t_0	t_1	t_1	t_0	t_m	t_2	t_{op}	t_2	t_m	t_0	t_1
III.A	t_m	t_0		t_1		t_2		t_{op}		t_2		t_1		t_0		t_m	
III.B	t_m	t_1		t_0		t_2		t_{op}		t_2		t_0		t_1		t_m	
III.C	t_1		t_m	t_0		t_2		t_{op}		t_2		t_0	t_m		t_1		
III.D	t_1		t_m	t_2		t_0		t_{op}		t_0		t_2	t_m		t_1		
III.E	t_1		t_2		t_m	t_0		t_{op}		t_0	t_m		t_2		t_1		
III.F	t_n	t_{op}		t_1		t_2		t_0		t_2		t_1		t_{op}		t_n	
III.G	t_n	t_1		t_{op}		t_2		t_0		t_2		t_{op}		t_1		t_n	

First of all, different vector placement sequences result in different current ripple. Take

buck mode as an example, not only the duration of open or short zero state affects the ripple amplitude, also the placement because current always increases at short zero state and decreases at open zero state. If short zero state and open zero state happen alternately, the smallest ripple can be achieved. Based on this, the 19 sequences can be classified in three groups as shown in Table 5-4. Group I is featured as unsymmetrical sequences with alternate short zero state and open zero state. Group II is featured as symmetrical sequences with non-alternate zero states, so it needs double the switching frequency to obtain the same current ripple; in another word, the current ripple will be doubled if keeping the switching frequency the same. Group III is featured as symmetrical sequences with alternate zero states. The T_S in current ripple equations of Table 5-3 refers to the whole switching period in group I and II, or half period in group III. The current ripple is related to switching period, inductance, input voltage and modulation index. And it decides the maximum current on the IGBT. When the devices and passive component have already been designed and built, the fixed current ripple is required. The current ripple will also affect the switching current thus affects the switching loss, as well as the inductor core loss. So group II sequences can only be utilized in the case of double switching frequency. As a result, group II is expelled because of high switching loss.

Secondly, different sequences cause different switching voltage and current and also different switching times in one switching period thus different switching loss. Table 5-5-Table 5-7 list the blocking voltage and conducting current for each commutation, and also the switching loss for the representative in each group. The turn on/off loss is equal to half of the product of blocking voltage and conducting current in each switching period. Also the average values of the absolute values of the blocking voltage over a 60^0 period are proportional to switching losses. For example, in commutation $t_{op} \rightarrow t_1$, the average voltage in sector I can be calculated as:

$$\overline{V_{s6}} = 2V_{in} - \frac{3}{\pi}\int_{\frac{\pi}{6}}^{\frac{\pi}{2}} V_{ab}\, d\omega t = 2V_{in} - \frac{3}{\pi}\hat{V}_{l-l} \tag{5.4}$$

The average value of $(|V_{bc}|+|V_{ca}|)$ in commutation $t_1 \to t_2$ and $t_2 \to t_0$ in sequence I.A will be constant over 60^0, calculated as:

$$\overline{|V_{bc}|+|V_{ca}|} = \frac{3}{\pi}\int_{\frac{\pi}{6}}^{\frac{\pi}{2}} (|V_{bc}|+|V_{ca}|)\, d\omega t = \frac{3}{\pi}\hat{V}_{l-l} \tag{5.5}$$

So the switching loss for buck mode depends on V_{in}, dc link current and switching frequency. The switching current in this case can be expressed as:

Table 5-5.Switching loss for sequence I.A in group I

Switching transition	Switching state	Switching loss
$t_0 \to t_{op}$	S_4 *off*	$\frac{1}{2}\frac{2V_{in}\cdot I_{pn\_\max}}{V_{ref} I_{ref}} E_{off} f_{sw}$
$t_{op} \to t_1$	S_6 *on*	$\frac{1}{2}\frac{(2V_{in} - \frac{3}{\pi}\cdot V_{l-l}) I_{pn\_\min}}{V_{ref} I_{ref}} E_{on} f_{sw}$
$t_1 \to t_2$	S_6 *off* S_2 *on*	$\frac{1}{2}\frac{(\frac{3}{2\pi}) V_{l-l} I_{pn\_\min}}{V_{ref} I_{ref}} (E_{on} + E_{off}) f_{sw}$
$t_2 \to t_0$	S_2 *off* S_4 *on*	$\frac{1}{2}\frac{(\frac{3}{2\pi}) V_{l-l} I_{pn\_\min}}{V_{ref} I_{ref}} (E_{on} + E_{off}) f_{sw}$

Table 5-6.Switching loss for sequence II.A in group II

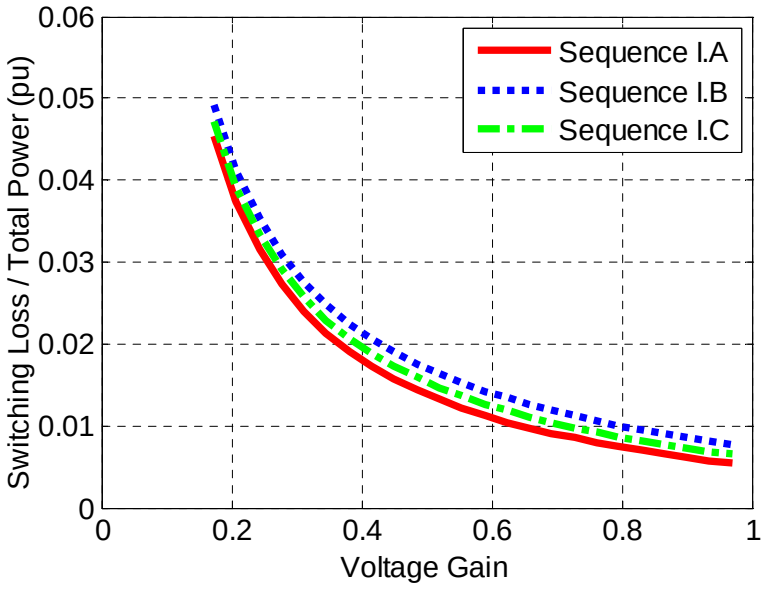
Switch transition	Switch state	Switching loss
$t_{op} \to t_0$	S_4 *on*	$\frac{1}{2}\frac{2V_{in}I_{pn\_\min 2}}{V_{ref}I_{ref}}E_{on}f_{sw}$
$t_0 \to t_1$	S_4 *off* S_6 *on*	$\frac{1}{2}\frac{\frac{3}{\pi}V_{l-l}(I_{pn\_\min 2}+\frac{1}{2}\Delta i)}{V_{ref}I_{ref}}(E_{on}+E_{off})f_{sw}$
$t_1 \to t_2$	S_6 *off* S_2 *on*	$\frac{1}{2}\frac{\frac{3}{2\pi}V_{l-l}(I_{pn\_\min 2}+\frac{1}{2}\Delta i)}{V_{ref}I_{ref}}(E_{on}+E_{off})f_{sw}$
$t_2 \to t_1$	S_2 *off* S_6 *on*	$\frac{1}{2}\frac{\frac{3}{2\pi}V_{l-l}(I_{pn\_\min 2}+\frac{1}{2}\Delta i)}{V_{ref}I_{ref}}(E_{on}+E_{off})f_{sw}$
$t_1 \to t_0$	S_6 *off* S_4 *on*	$\frac{1}{2}\frac{\frac{3}{\pi}V_{l-l}(I_{pn\_\min 2}+\frac{1}{2}\Delta i)}{V_{ref}I_{ref}}(E_{on}+E_{off})f_{sw}$
$t_0 \to t_{op}$	S_4 *off*	$\frac{1}{2}\frac{2V_{in}(I_{pn\_\min 2}+\Delta i)}{V_{ref}I_{ref}}E_{off}f_{sw}$

$$
\begin{aligned}
I_{pn\_\max/\min} &= \frac{I_{in}}{1-2D_{op}} \pm \frac{3}{2L}(1-0.866m)*V_{in}\cdot T_s \\
I_{pn\_\max 2/\min 2} &= \frac{I_{in}}{1-2D_{op}} \pm \frac{3}{2L}(1-0.866m)*V_{in}\cdot 2T_s
\end{aligned}
\tag{5.6}
$$

Switching current is the instantaneous current at the turn on/off point. Group I and III has the $I_{pn\_\max}$ and $I_{pn\_\min}$ in equation (5.6) because it has alternate short zero state and open zero state; Group II has $I_{pn\_\max 2}$ and $I_{pn\_\min 2}$ which has $2T_s$ in their equations because of their non-alternate zero states.

Table 5-7.Switching loss for sequence III.B in group III

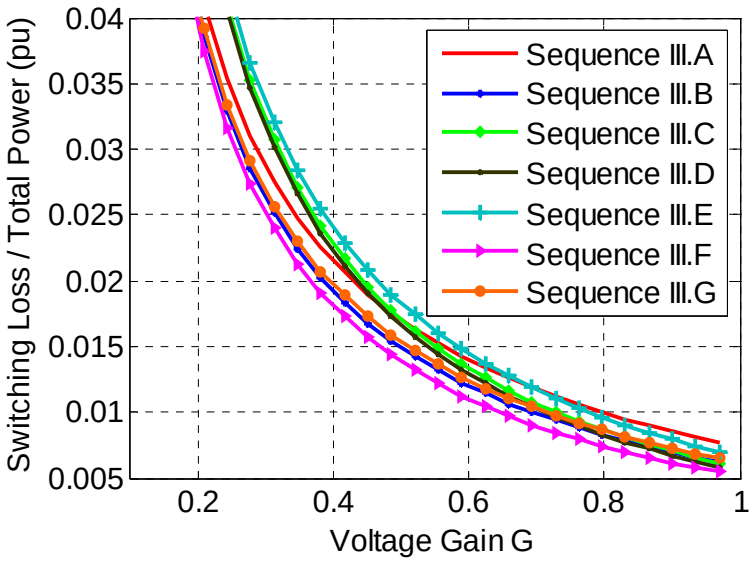
Switching transition	Switching state	Switching loss
$t_{op}/2 \rightarrow t_1$	S_6 *on*	$\frac{1}{2}\frac{(2V_{in}-(\frac{3}{\pi})V_{l-l})I_{pn\_\min}}{V_{ref}I_{ref}}E_{on}f_{sw}$
$t_1 \rightarrow t_0$	S_6 *off* S_4 *on*	$\frac{1}{2}\frac{(3/\pi)V_{l-l}I_{pn\_\min}}{V_{ref}I_{ref}}(E_{on}+E_{off})f_{sw}$
$t_0 \rightarrow t_2$	S_4 *off* S_2 *on*	$\frac{1}{2}\frac{(\frac{3}{2\pi})V_{l-l}I_{pn\_\max}}{V_{ref}I_{ref}}(E_{on}+E_{off})f_{sw}$
$t_2 \rightarrow t_{op}/2$	S_2 *off*	$\frac{1}{2}\frac{(2V_{in}-(\frac{3}{2\pi})V_{l-l})I_{pn\_\max}}{V_{ref}I_{ref}}E_{off}f_{sw}$



(a) Switching loss pu vs. voltage gain in group I

Figure 5.10. Switching losses (a) group I (b) group III

Figure 5.10 (cont'd)



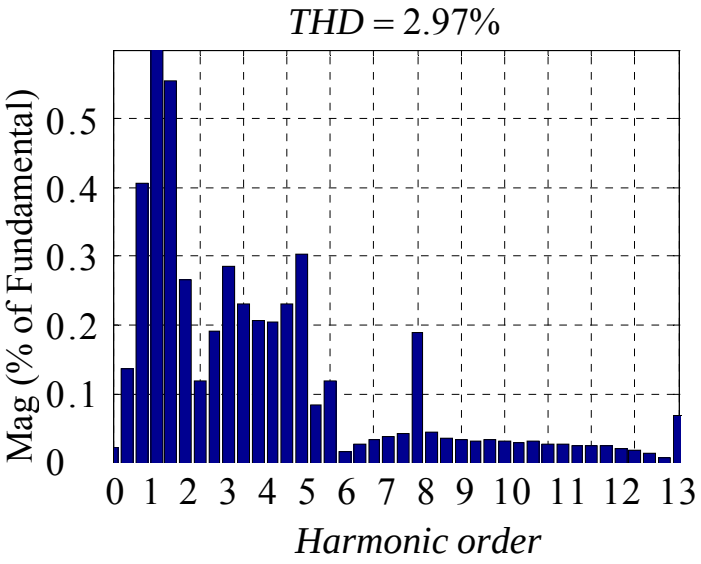
(b) Switching loss pu vs. voltage gain in group III

In buck mode, the switching loss can be theoretically calculated at different voltage gain point according to the equations above. A 600V/200A RB-IGBT module with 18 switches inside from Fuji Electric Device has been used in the prototype. The switching parameters from the data sheet are: *Eon=12mJ, Eoff=8mJ, Err=2mJ at Vref=300V, Iref=200A*. Thus the switching loss equations in the tables can be calculated accordingly. Figure 5.10 shows the percentage of switching loss in total power loss when voltage gain increases from 0 to 1 for different groups of switching sequences.

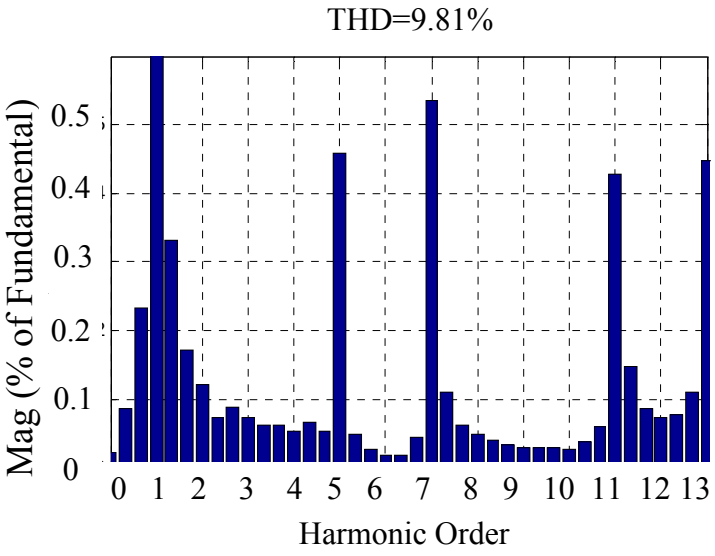
In conclusion, in buck mode, sequence I.A, I.B, I.C, III.A, III.B, III.F, III.G have better performance in terms of switching loss, at equal current ripple case.

Third, the best vector placement sequence has also to be chosen according to the output voltage THD. In this section, harmonic analysis of output current waveform of each sequence is presented as shown in Figure 5.11. The output phase current is the research target. The waveform is got from the simulation results. According to modulation theory, the output signal will have all the harmonics of the reference signal and sidebands associated with the sampling frequency. It can be seen that some sequences obviously have lower harmonics such

as I.A, II.A, III.B.



a. Sequence I.A

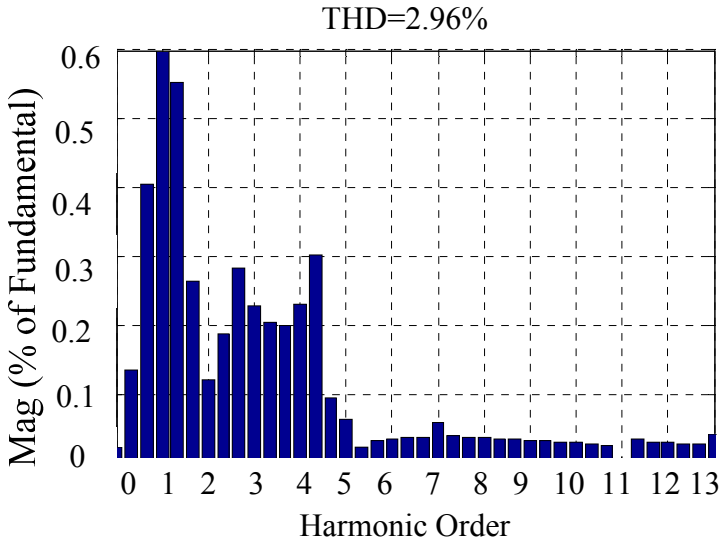


b. Sequence I.C

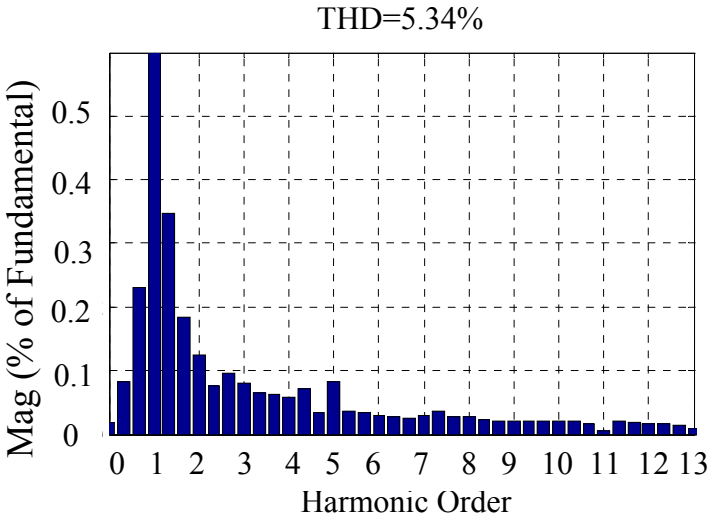
Figure 5.11. Spectrum for sequences from each group in buck mode at *M*=0.8, *Dop*=0.3

For each sequence, the total harmonic distortion is different at different modulation index. Three typical sequences I.A, II.A, III.B, which can represent the characteristics of that group proximately, are selected from different groups to do comparison in THD at different modulation index, as shown in Figure 5.12. In conclusion, control sequence which is

Figure 5.11 (cont'd)



c. Sequence II.A

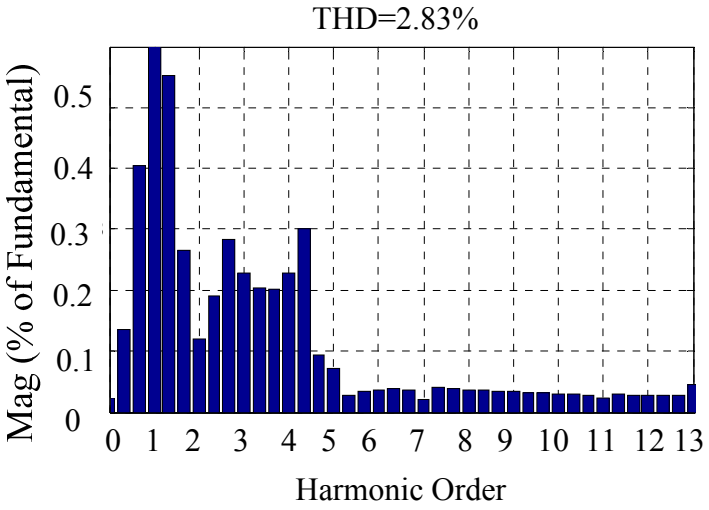


d. Sequence II.D

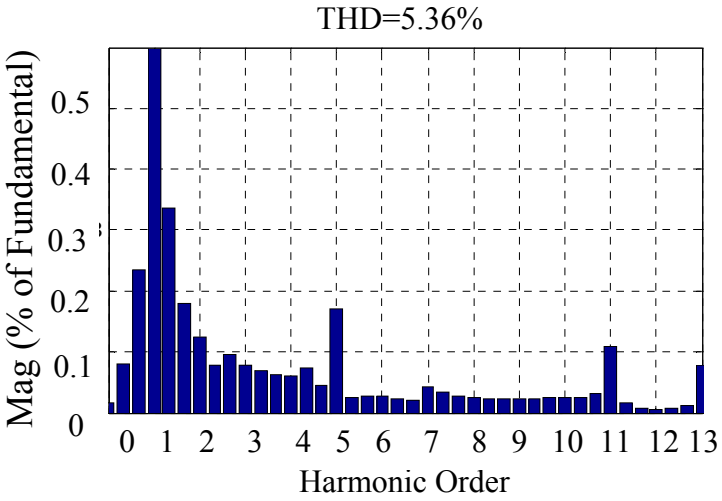
symmetrical and which posses low current ripple, low switching frequency has lower harmonics contents. In conclusion, sequence III. B which represents group III is preferred to sequences in group I and II since it generates lower THD in the output.

Fourth, voltage spike on the active device is also affected by the vector placement. The best sequence is required to achieve lowest voltage spike. The voltage rating of the RB-IGBT in this experiment is 600V/200A. In order to maximally utilize the IGBT voltage rating, the

Figure 5.11 (cont'd)



e. Sequence III.B



f. Sequence III.G

average maximum operation voltage on the IGBT is selected to be 400V, which means the input voltage is set as 200V because the dc link voltage is two times of input in open zero state. This happens in buck mode. The voltage spike on the pn voltage when the open zero state is not applied is tested to be 25% of the voltage level. However, when the short zero state is put before open zero state, the voltage spike caused by the cut off of the pn current will be added on the maximum pn voltage which happens in open zero state. Thus the sequences I.A, II.B, II.G, II.I, III.F, are not preferred in buck mode considering the RB-IGBT

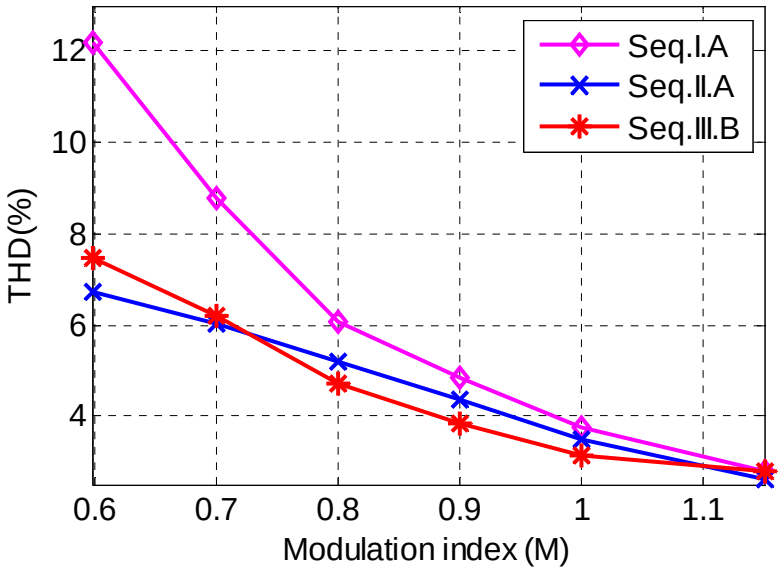


Figure 5.12. THD for each representative sequence from each group vs. Modulation index in buck mode

voltage spike. In addition, the Z-source diode will undertake the same voltage stress as the pn voltage according to the governing equation. The diode voltage rating is also selected as 600V in this prototype. In short zero state, the diode voltage stress becomes maximum which is two times of the input voltage. In open zero state, the diode voltage stress is equal to zero. The biggest voltage spike on the diode happens in the reverse recovery process when the diode turns off at the end of open zero state. Therefore, if open zero state is put before short zero state, the highest voltage spike will add on the highest voltage level, which is not desirable. So the sequences I.B, II.A, II.F, III.A, III.C, III.E are not preferred in buck mode considering the diode maximum voltage stress. In conclusion, in the consideration of voltage stress on RB-IGBT and Z-source diode, the sequences in which t0 and top are adjacent to each other should not be selected in buck mode.

Concluded from above four criterions, sequence III. B is selected in buck mode to obtain lower switching loss, lower current ripple, lower THD and lower voltage spike on the devices.

5.6. Case Study: 98% Efficiency 24KW Current-fed Quasi-Z-Source Inverter

A 24KW current-fed quasi-Z-source inverter has been built in the lab to verify the proposed optimized vector placement. The three input inductors have been coupled together, and designed to maintain 30% current ripple. The active switch voltage spike is designed to be within 30% of the normal voltage. Efficiency is the optimization target. A single stage buck-boost inverter with much higher efficiency than a two stage boost-converter-inverter is expected.

5.6.1. Power loss analysis for 24KW current-fed quasi-Z-source inverter

1) RB-IGBT Conduction Loss

In open zero state, the conduction loss is equal to zero since the bridge has no current flowing; in short zero state or active state, there is always one upper switch and one lower switching on at the same time, and the conducting current is always equal to the dc link current. IGBT conduction loss increases as voltage gain increases in both buck and boost mode. The average dc link current shown in table III is used here to approximately calculate the conduction loss:

$$P_{cond\_buck} = 2(V_{CE}\frac{\overline{I_{pn}}}{1-2D_{op}}(1-D_{op}) + (\frac{\overline{I_{pn}}}{1-2D_{op}}(1-D_{op}))^2 R_{ds}) \tag{5.7}$$

$$P_{cond\_boost} = 2(V_{CE}\overline{I_{pn}} + \overline{I_{pn}}^2 R_{ds}) \tag{5.8}$$

The parameters from the datasheet is V_{CE}=*2.8V*. Thus the conduction loss can be obtained.

2) Z-Source Diode Power Loss

In boost mode, the diode loss is zero because the diode keeps off during non-open zero state.

In buck mode, the diode conducts only in open zero state, and its loss is composed of conduction loss and reverse recovery loss, which can be expressed as follows:

$$P_D = P_{cond\_loss} + P_{Rev\,Rec\_loss} RR$$
$$= \overline{I_{pn}} U_{cond} D_{op} + Q_{rr}(2V_{in} - \hat{V}_{pn}) \cdot \frac{\overline{I_{pn}}}{I_{ref}} \cdot f_{swD} \quad (5.9)$$

$\hat{V}_{pn}$ refers to the instantaneous value of the pn voltage at the moment that diode is turned off.

f_{swD} refers to the equivalent switching frequency of the z-source diode, which depends on the times that open zero state happens during one switching period.

In all those sequences, the expression of $\hat{V}_{pn}$ has three conditions: If short zero state is placed after open zero state, $\hat{V}_{pn} = 0$; If active state one is placed after open zero state, for example, in sector I, $\hat{V}_{pn} = \hat{V}_{ab}$; If active state two is placed after open zero state, $\hat{V}_{pn} = \hat{V}_{ac}$.

The parameters for the diode from the datasheet are:

$Q_{rr} = 3.0\ \mu C \quad (IF = 1000A, di/dt = -2000A/\mu s), V_{FM} = 1V \quad (I_F = 100A)$. In boost mode, the diode always keeps off since there is no open zero state. So diode power loss is equal to zero in this case.

3) Inductor core loss

Table 5-8.Inductor Voltage in buck mode and boost mode

		D_{OP}	D_1	D_2	D_{sh}
V_L	buck	$-V_{in}$	$V_{in} - V_{ab}$	$V_{in} - V_{ac}$	-------
	boost		$V_{in} - V_{ab}$	$V_{in} - V_{ac}$	V_{in}

$$P_{ind} = P_{core} + P_{dcr} + P_{acr} = kf\,(kHZ)^x B^y V_{olume} + {I_{dc}}^2 R_{ind} + {I_{ac\_rms}}^2 R_{ind} \quad (5.10)$$

The inductor power loss is composed of core loss and winding loss accordingly (5.10).

A high flux 60 core has been used in the coupled inductor. The parameters for the core are: $A_e = 20cm^2, l_e = 34.57cm, V_{core} = 760cm^3$. Number of turns is N=18. In the core loss

part, to calculate core loss, the instantaneous B_{ac} is needed. Since the voltages on three inductors are the same from the governing equations, B_{ac} for each inductor is also the same. In addition, three inductors are coupled together, the magnetic flux are forced to be the same and it is equal to 3 times of volt-sec product for a single inductor. The equation to calculate B_{ac} is:

$$B_{ac} = \frac{\Delta B}{2} = \frac{\lambda}{2NS} = \frac{3\int_0^{T_{sw}} v_L dt}{2NS} \tag{5.11}$$

The inductor voltage is listed in Table 5-8. In buck mode, the inductor voltage is negative in open zero state and positive in active state, so the volt-seconds could be calculated only by the open zero state because the voltage and time period are all constant in this state.

$$B_{ac\_buck} = \frac{3V_{in}D_{op}T_s}{2NS} \tag{5.12}$$

In boost mode, the volt-seconds product varies in every switching period, and it can be calculated by integration with time as eq. (5.11). The volt-sec integration in boost mode can be calculated as follows:

$$(\int_0^{T_{sw}} v_L dt)\_boost = \frac{3\int_0^{\frac{\pi}{3}} [V_{in}t_0 + (V_{in} - v_{ab})t_1 + (V_{in} - v_{ac})t_2) d\theta}{\pi/3} \tag{5.13}$$

Due to the symmetry, the core loss of three inductors are the same at any time point. So the total inductor core loss is three times of the single one.

4) Inductor winding loss

For each inductor, the winding loss can be expressed as a general form as follows:

$$P_{cond} = {I_{dc}}^2 R_{ind} + \frac{1}{12}\Delta {i_p}^2 R_{ind} \tag{5.14}$$

In the winding loss part, dc current is equal to the average current of each inductor; ac current rms value is equal to the integration of ripple current square in one switching cycle divided

by time. Assume that the ripple current amplitude remains the same all the time, then the ac rms current is $\sqrt{\Delta i_p{}^2/12}$, in which Δi_p is the peak to peak ripple current. In buck mode, all three inductors have both of the dc and ac winding loss; however, in boost mode, the two Z-source inductors don't have the dc winding loss. The average current and current ripple for three inductors in buck and boost mode respectively are shown in Table 5-3. The parameters for the copper here is cross area AL=27.1 mm^2 and current density is 2.76A/mm^2. The measured input inductor resistance is 5.9mOhm, and Z-source inductor resistance is 4.2mOhm. The total winding loss can be calculated.

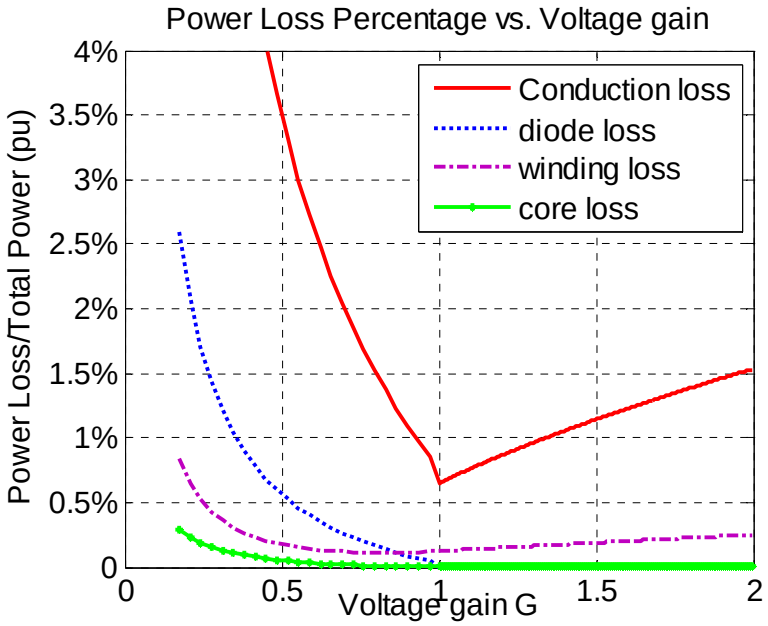


Figure 5.13. Power loss percentage vs. voltage gain

Figure 5.13 shows the percentage of conduction loss, diode loss, winding loss and core loss in the total power as a function of voltage gain. It presents that at buck mode, the loss decreases when the voltage gain increases; at boost mode, the loss increases when the voltage gain increases.

5) Efficiency test reference curve

In hybrid electrical vehicle application, the start-up process is in voltage buck mode. The output power should be proportional to the output voltage, in order to achieve constant torque.

After it reaches the maximum output power, it enters into voltage boost mode, the power always keeps constant as output voltage increases in order to attain the maximum efficiency. Figure 5.14 shows this characteristics curve. For a given power rating, make the inverter operate on the corresponding curve by fixing input voltage but varying load resistors. The modulation index and output voltage is derived from voltage ratio and input voltage according to equations in Table 5-2. Load resistance can be calculated by the output power and output voltage at each point. Two curves are selected to measure the efficiency, as shown in Figure 5.14.

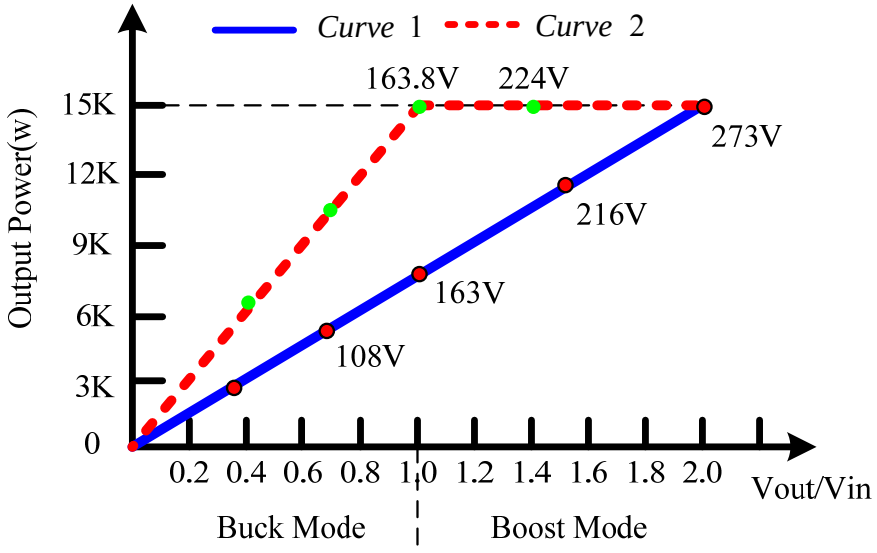


Figure 5.14. Efficiency measurement reference curve

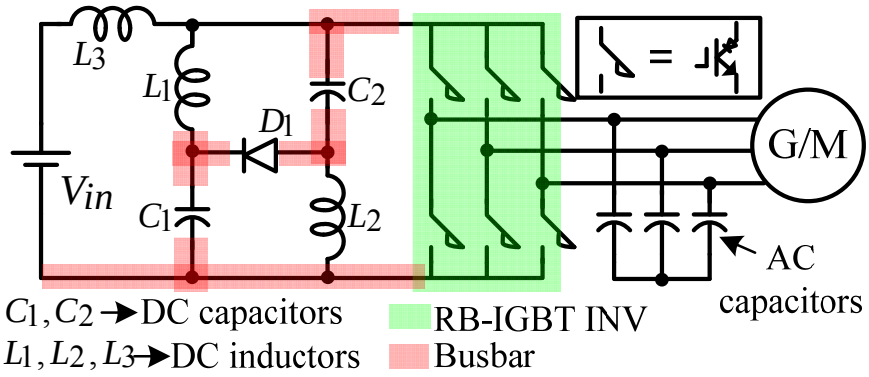
According to the circuit configuration and power loss analysis, the total power loss of this circuit can be approximately calculated as:

$$P_{loss} = (P_{sw} + P_{cond})_{IGBT} + (P_{cond} + P_{rr})_D + (P_{core} + P_{winding})_L \qquad (5.24)$$

According to the datasheet of RB-IGBT and diode, also the design parameters for the inductors, the efficiency at every operation point can be calculated. The results will be shown in the next section. It can be seen that the best efficiency happens at unity voltage gain.

5.6.2. Basic buck/boost function test on first version 5KW prototype

In order to verify the circuit operation and the control strategy, a 5kW current-fed quasi-Z-source inverter prototype has been built in the lab, as shown in Figure 5.15 A circuit configuration figure is also shown to compare with the prototype.



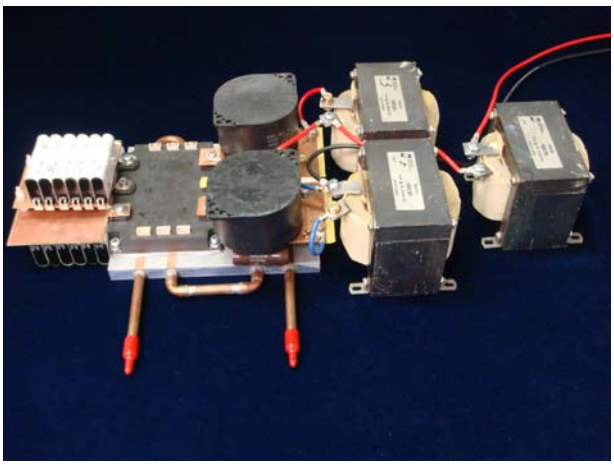


Figure 5.15. 5kW current-fed quasi-Z-source inverter prototype

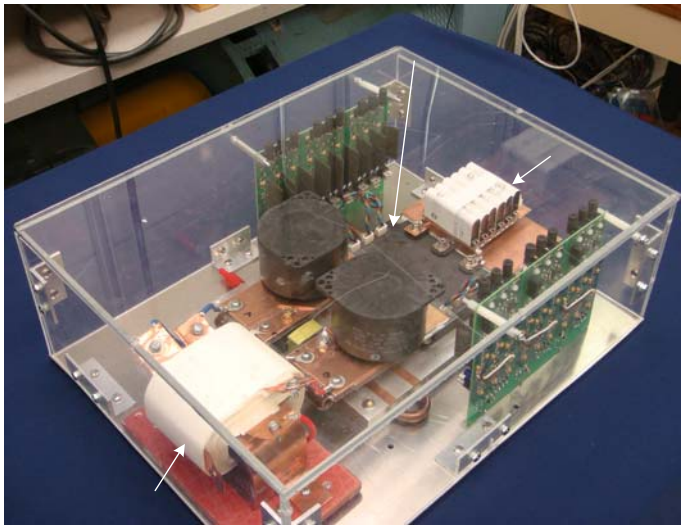


Figure 5.16. 5kW current-fed quasi-Z-source inverter with coupled inductors

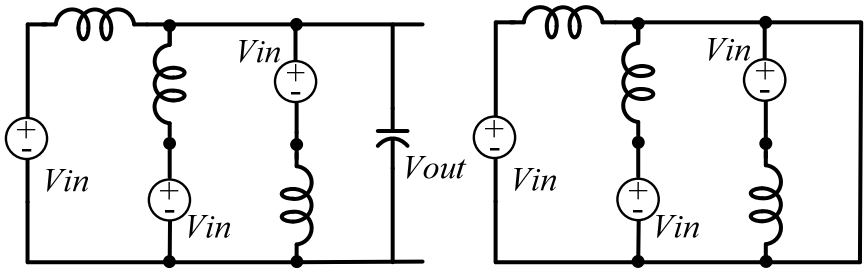
The system specifications for the experiments are:

$$
\begin{aligned}
&L_1 = L_2 = 2m, \\
&C_1 = C_2 = 200u\ , \\
&C_{sa} = C_{sb} = C_{sc} = 60u, \\
&f_s = 10kHZ \\
&IGBT : 600V / 200A\ RB - IGBT \\
&Power\ Rating : 5KVA
\end{aligned}
$$

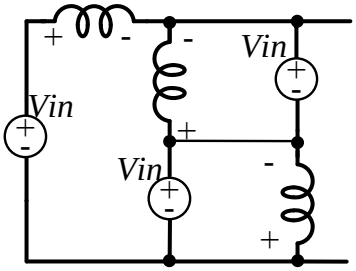
In the prototype, the input inductor and two Z-source inductors have different average dc current. The average input inductor current is equal to input current, which forms the major input power. The average current of the Z-source inductor satisfies that:

$$I_L = \frac{D_{op}}{1 - 2D_{op}} I_{in}$$

But all inductors share the same current ripple. It can be simply illustrated by the equivalent circuit shown in Figure 5.17 as follows.



(a) Active state (b) Short zero state



(c) Open zero state

Figure 5.17. Equivalent circuits in active state, short zero state and open zero state

Figure 5.17 shows the equivalent circuits in three states. Since the capacitor voltage is equal to input voltage if the assumption of big capacitor is made, the capacitor is replaced by

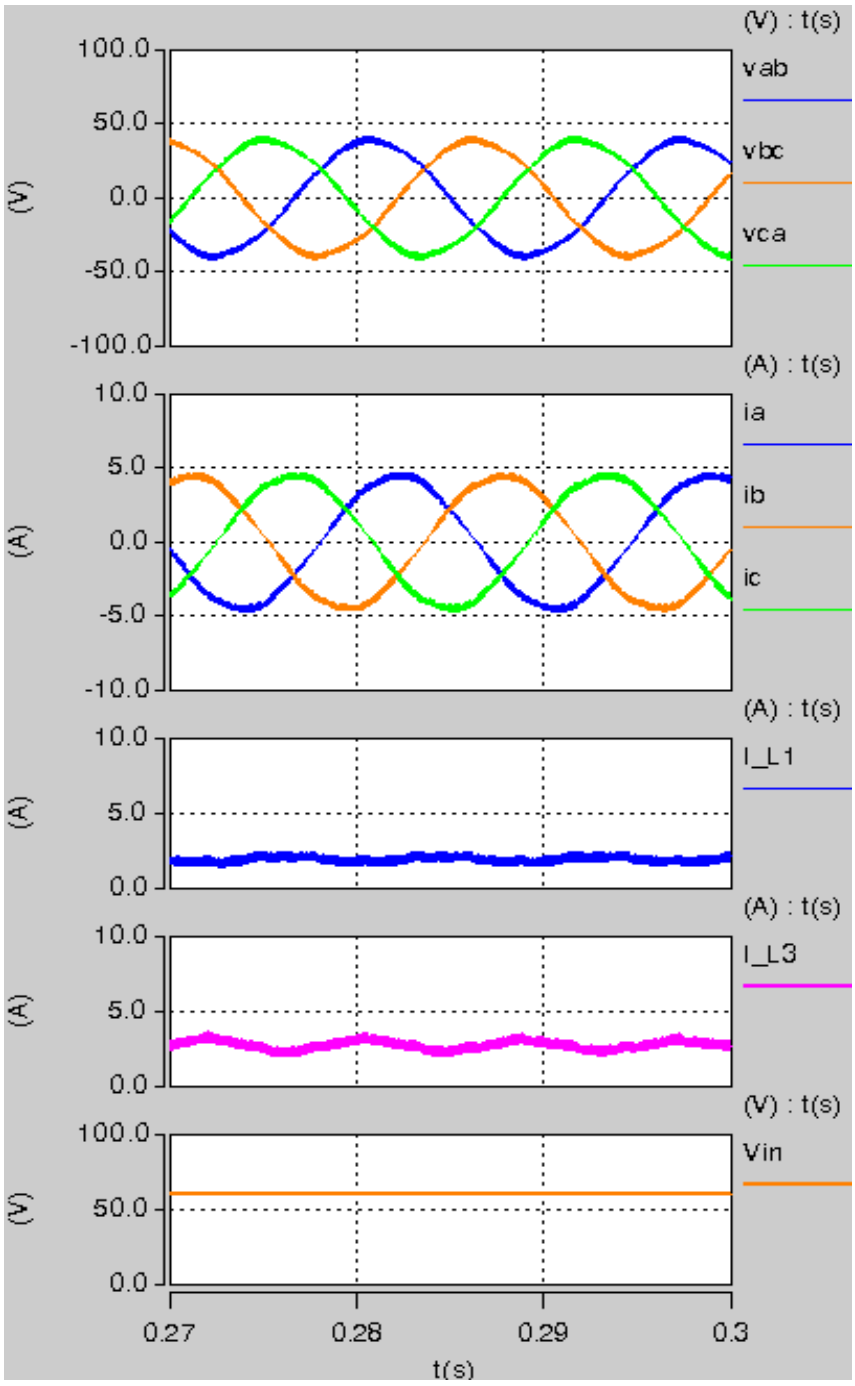
a dc voltage source. In active state, each inductor has the same voltage drop, which is equal to input voltage subtracting the active state dc link voltage; in short zero state, each inductor voltage is the same, equal to input voltage; in open zero state, each inductor undertakes a negative input voltage. Therefore, the three inductors always have the same voltage stress. It also means they can be coupled on the same core. A coupled inductor design can save the space thus reduce the system size, no matter whether it really reduces the total volume of the inductors or not. The three inductors are coupled together on the same AMCC core with copper sheet wiring, as shown in Figure 5.16.

Four operation conditions are selected for simulation and experiment demonstration. They are listed in Table 5-9. The first three cases are in motoring mode with same modulation index but different open zero duty cycle. The last case is in regeneration mode.

Table 5-9.Different Operation Points in Simulation and Experiments

	V_o	V_{in}	$\overline{V_{out}}$	D_{op}	$\overline{D_A}$	m	$\cos\phi$
Case 1	40.8V	60V	90.6V	0	0.662	0.8	1
Case 2	32.6V	60V	72.5V	0.1	0.662	0.8	1
Case 3	16.3V	60V	36.3V	0.3	0.662	0.8	1
Case 4	32.5V	80V	72.5V	0.65	0.331	0.4	-1

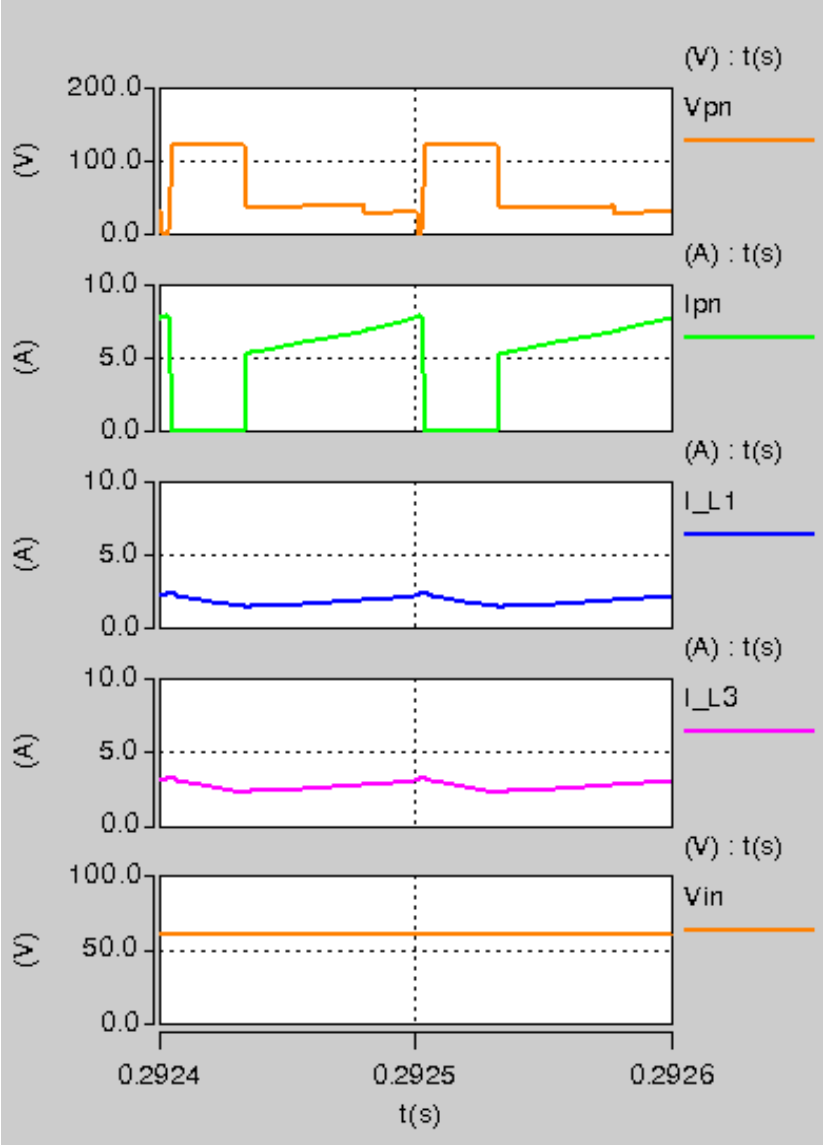
The simulation results of case 3 and 4 are shown in Figure 5.18. The experimental results are shown in Figure 5.19 - Figure 5.20. In both simulation and experiment results, the dc link voltage is a four level stair waveform. The highest level is two times of input voltage, which happens in open zero state; the two middle level is equal to output line to line voltage, corresponding to two active states; another level is zero, which happens in short zero state. The overall dc link voltage in a zoom out view follows a 6ω envelope, which is equal to the output line to line voltage envelope. For dc link current, it is continuous in active and short zero state because it is always equal to the sum of three inductor current; however, it becomes



(a) Case 3

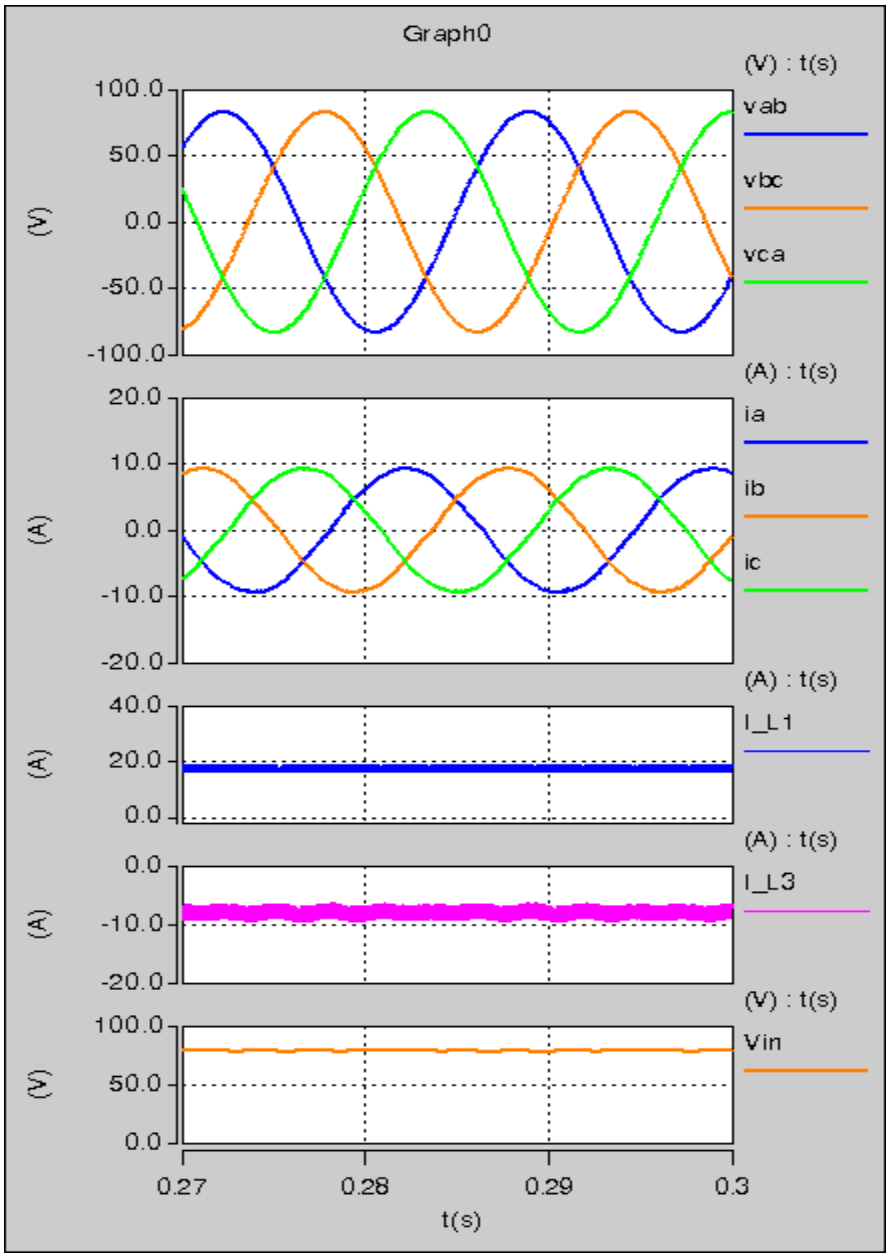
Figure 5.18. Simulation results: left figure (from top to bottom): output line to line voltage, output phase current, Z-source inductor current, input inductor current, input voltage; right figure: dc link voltage, dc link current, Z-source inductor current, input inductor current, input voltage

Figure 5.18 (cont'd)



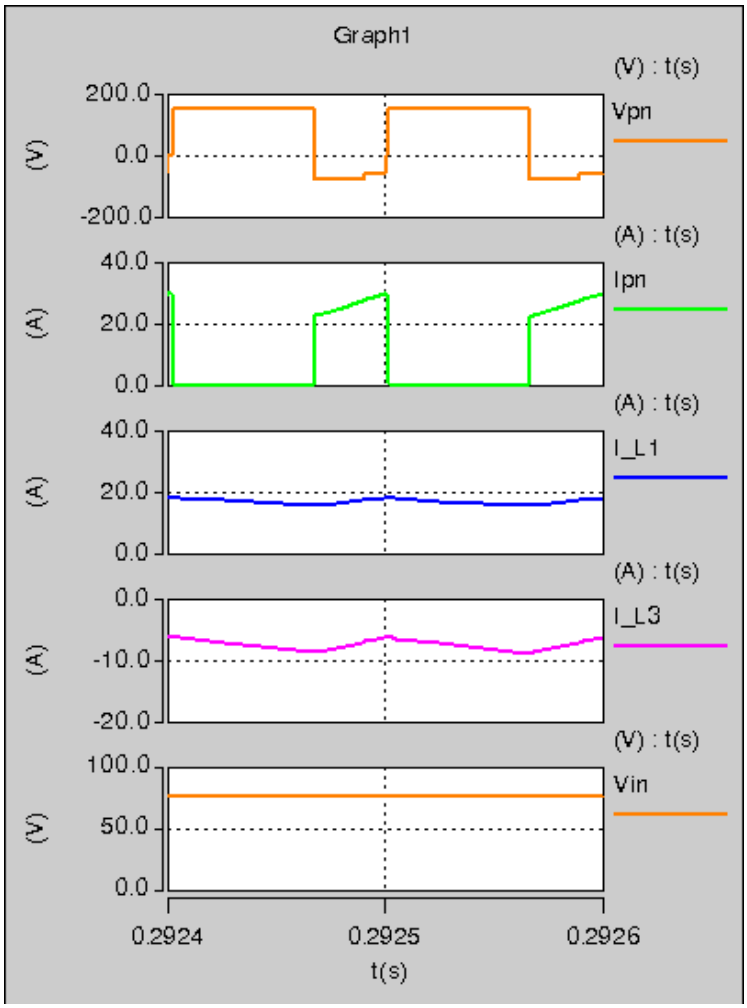
(b) Case 3

Figure 5.18 (cont'd)



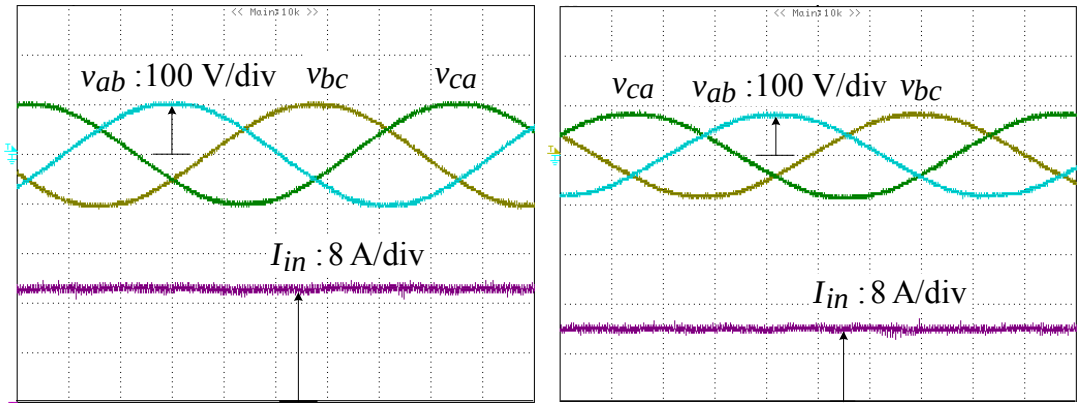
(c) Case 4

Figure 5.18 (cont'd)

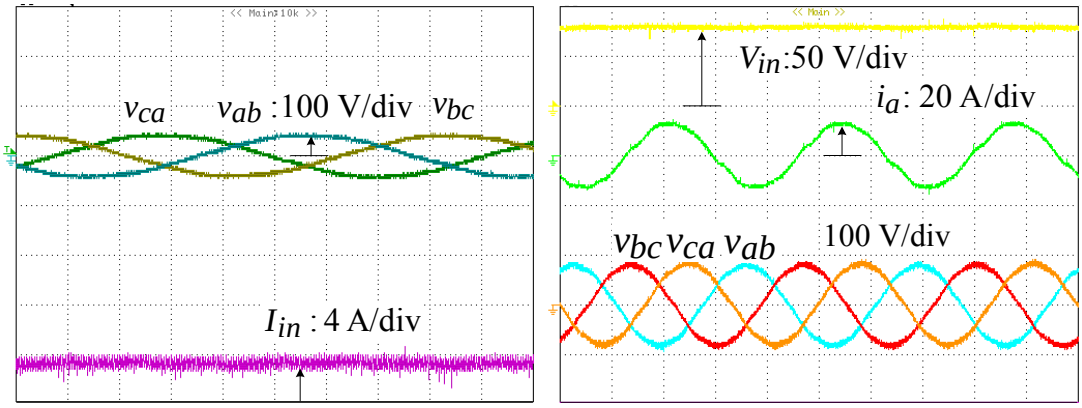


(d) Case 4

Figure 5.18. Simulation results: left figure (from top to bottom): output line to line voltage, output phase current, Z-source inductor current, input inductor current, input voltage; right figure: dc link voltage, dc link current, Z-source inductor current, input inductor current, input voltage

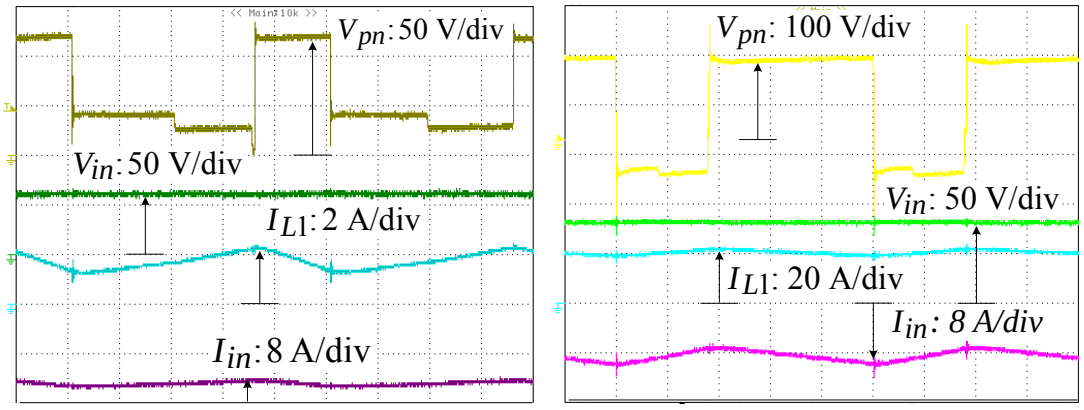


(a) Case 1 (b) Case 2



(c) Case 3 (d) Case 4

Figure 5.19. Case 1-3: from top to bottom is output line to line voltage and input current; case 4: from top to bottom: input voltage, output phase current, output l-l voltage



(a) Case 3 (b) Case 4

Figure 5.20. Zoom in waveform for case 3 and 4: from top to bottom: DC link voltage, input voltage, Z-source inductor current, input current

zero in open zero state. For the inductor current, in motoring mode, the Z-source inductor and input inductor has the same ripple and same direction. However, in regenerative mode, the ripple still maintains the same but the sign of current changes. The input inductor has negative current, but the Z inductor has positive current. In experiment results, the output voltage decreases when the open zero duty cycle increases from 0 to 0.3 from case 1 to case 3, which demonstrate this current source inverter has voltage buck/boost function. In regenerative mode, the open zero duty cycle exceeds 0.5, at the same time the modulation index is smaller than 0.5. The output current is in 150^0 with output line to line voltage in this case. The overall simulation and experimental results demonstrate the derived voltage gain equation and also the current gain, current ripple equations, as well as the regenerative mode operation. The dc link voltage waveform clearly shows the four state operation. The change of output voltage with change of open zero duty cycle demonstrates the circuit's voltage buck/boost function. At last, the prototype has been well designed and assembled. Thus there is no obvious voltage spike on dc link and also the current ripple is relatively small. The output voltage and current waveforms all have very small THD.

5.6.3. Basic function and efficiency test on final 24KW prototype

1) Experiment set up and hardware parameters

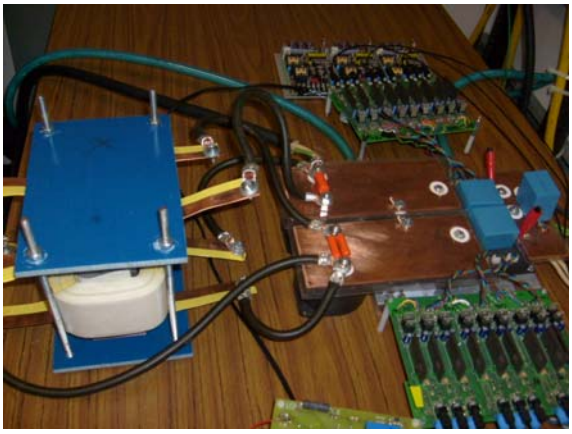


Figure 5.21. Hardware picture

Table 5-10.Experiment hardware part number and parameters

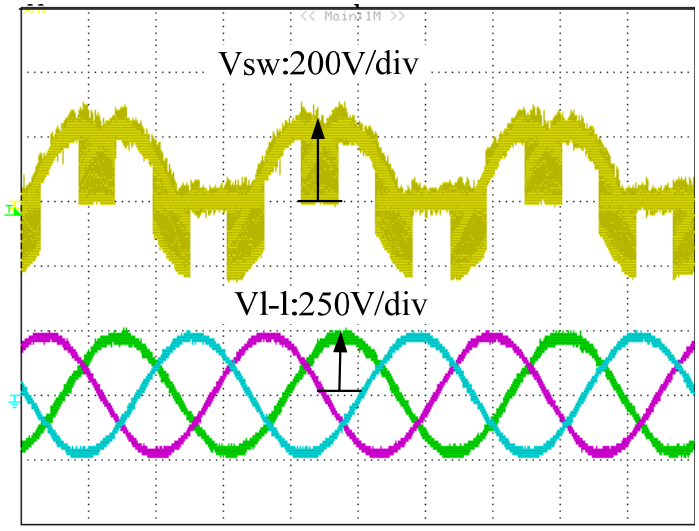
Components	*Part number and parameters*
IGBT	*RB-IGBT, 600V, 200A*
Diode	*QRS061K001, 600V*
Coupled inductor	$L_1 = L_2 = L_3 = 141uH;\ R_1 = 5.9m\Omega;\ R_2 = R_3 = 4.2m\Omega;$ $A_e = 20\ cm^2, l_e = 34.6\ cm, Vol = 0.798L;\ N = 18;\ Core: High\ Flux\ 60u$
Output capacitor	*UL35Q207K, C=30uF*

In this experiment, the IGBT used is the 600V, 200A RB-IGBT module from FUJI corp. The coupled inductor with high flux 60u core and 18 turns which is valued at 141uH is used. Fix the input voltage at 200V and output power rating at 15kw and calculate the efficiency at different V_{out} / V_{in} ratio according to the aforementioned equations and all the parameters from the datasheet. The results are shown in Figure 5.22-5.25. Also a prototype has been built to verify the theoretical analysis, as shown in Figure 5.21. In Figure 5.26 and Figure 5.27, the experimental results are shown in blue star, which matches with the estimated efficiency curve very well. It proves that the calculation method is valid.

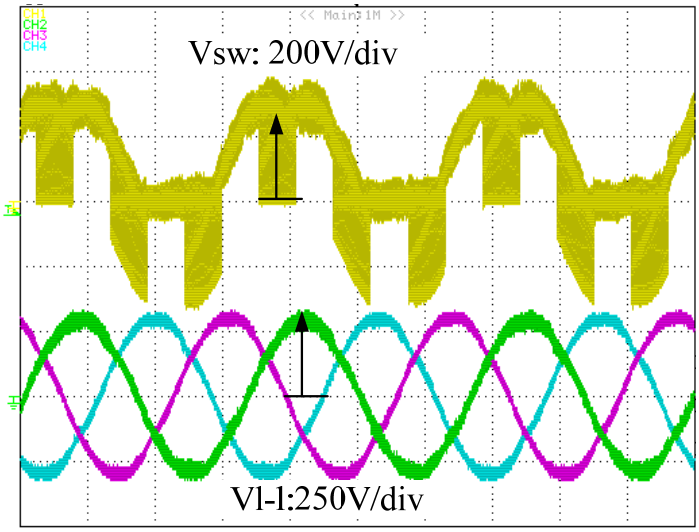
5.6.4. Experiment results

Figure 5.22 shows the three phase output line to line voltage and one device voltage at power equal to 8.54KW, 11.6KW and 14.7KW. The operation points are selected from the operation curve 1 in Figure 5.20. Figure 5.16 shows the results on curve 2. With proper control parameters, for each point, the measured voltage amplitude showing in the footnote of the figures matches with the calculated results in Figure 5.20. Figure 5.24 shows the output voltage, current, input voltage, current waveforms and also the measured values at five operation points on the curve 1 in Figure 5.14. The results are obtained from the YOKOGOWA power meter measurement. The upper three sinusoidal traces are output line to

line voltage, the lower three sinusoidal traces are output line current. The upper flat trace is input dc voltage, and the lower flat trace is input dc current. The detailed notations are shown at the right side of the figure. The numbers show the output line to line voltage rms and current rms, and also the input dc voltage and current value. Figure 5.25 shows the results on curve 2. The best efficiency on curve 1 is 98.2%, at P=8.66KW; the best efficiency on curve 2 is 97.6%, at P=14.7KW, $V_{l-lrms}=163V$, which is at unity voltage gain, shown as the turning point on curve 2 in Figure 5.14.



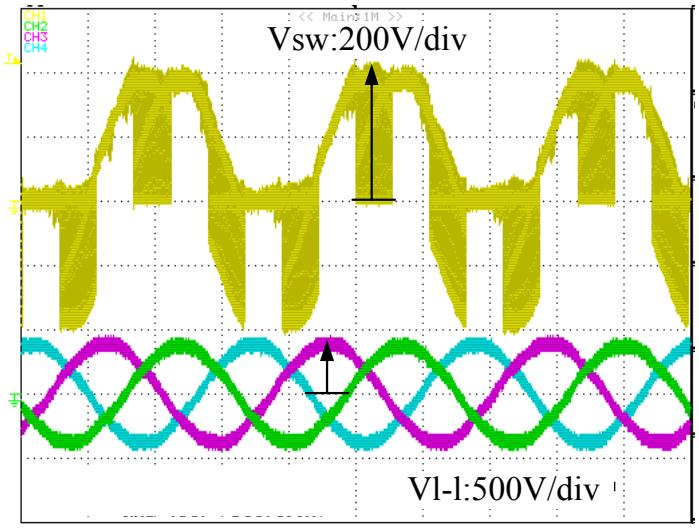
(a) $R=3\Omega,[P_o,V_{l-lrms}]=[8.54KW,162V]$



(b) $R=4\Omega,[P_o,V_{l-lrms}]=[11.6KW,213V]$

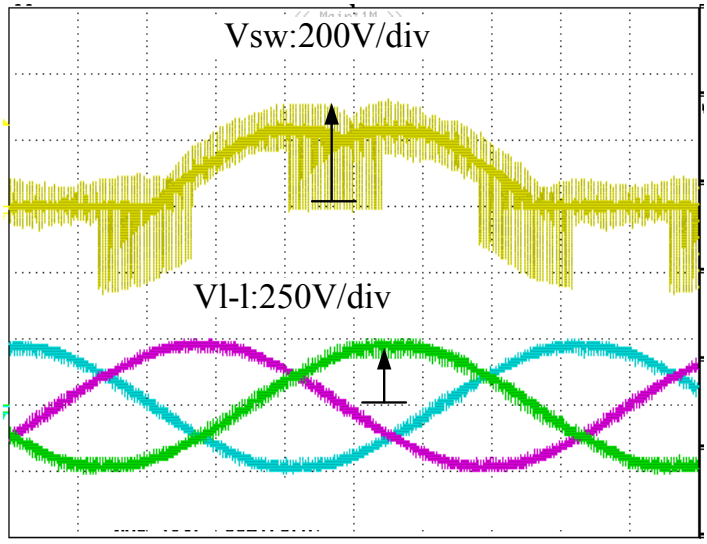
Figure 5.22. Three phase output line to line voltage and device voltage on curve 1

Figure 5.22 (cont'd)



(c) $R = 5\Omega, [P_o, V_{l-lrms}] = [14.7KW, 273V]$

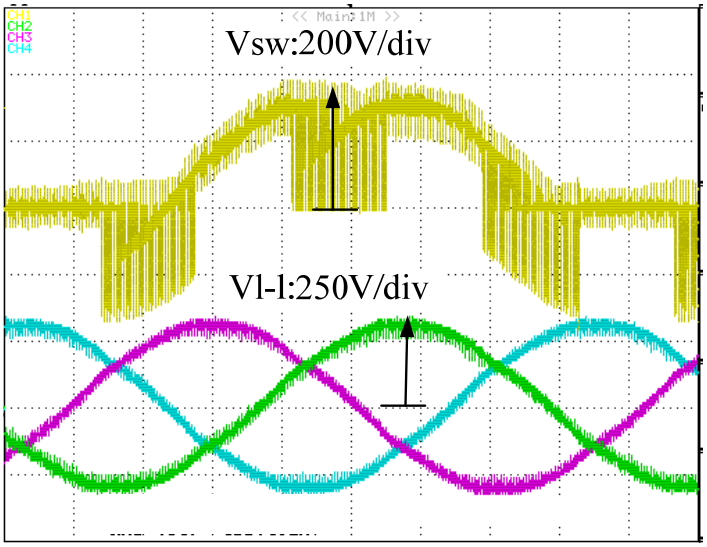
Figure 5.22. Three phase output line to line voltage and device voltage on curve 1



(a) $R = 1.8\Omega, [P_o, V_{l-lrms}] = [14.7KW, 163V]$

Figure 5.23. Three phase output line to line voltage and device voltage on curve 2

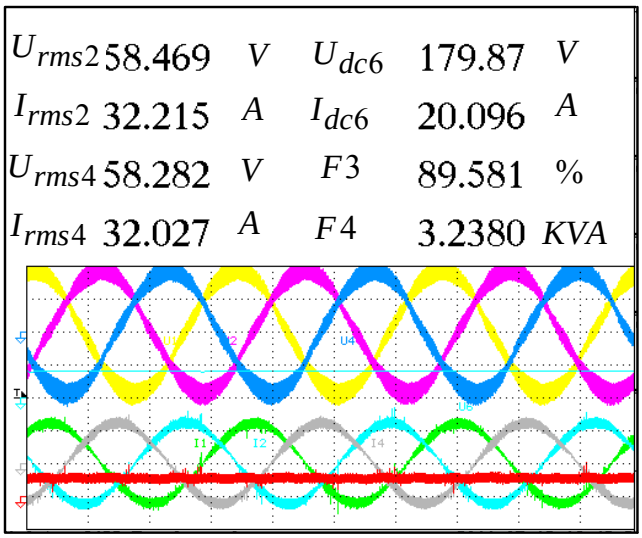
Figure 5.23 (cont'd)



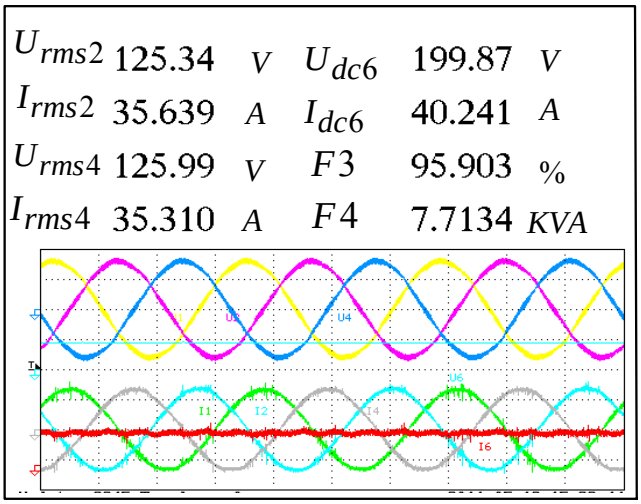
(b) $R = 3.45\Omega, [P_o, V_{l-lrms}] = [14.25KW, 220V]$

5.6.5. Efficiency vs. voltage gain plot

Figure 5.26 shows the system overall efficiency at different voltage gain when operates on the curve 1 of Figure 5.14. Figure 5.26 presents that the highest efficiency 98.2% happens at unity voltage gain at half 15kW power rating. In buck mode, the efficiency increases dramatically as the power increases; in boost mode, the efficiency decrease gradually as the power increases. Figure 5.27 shows the overall efficiency on curve 2. It presents that at full power rating 15KW, the best efficiency 97.6% is also obtained at the unity voltage gain. In conclusion, based on our hardware design and control method optimization, the best efficiency that can be obtained is 98%. And the best efficiency at 15KW is 97.6%.



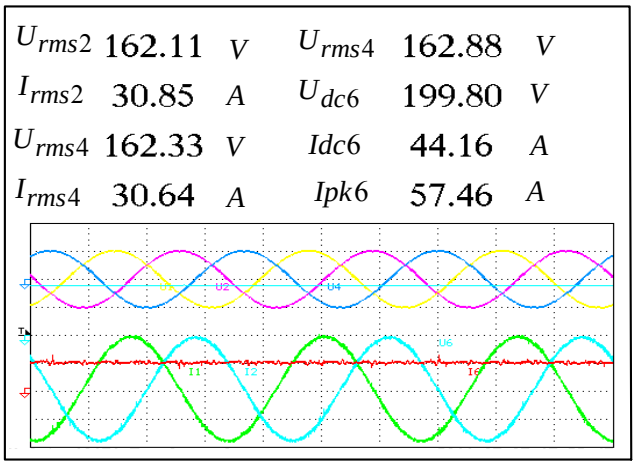
(a) $R = 1\Omega, [P_o, \eta] = [3.2KVA, 89.6\%]$



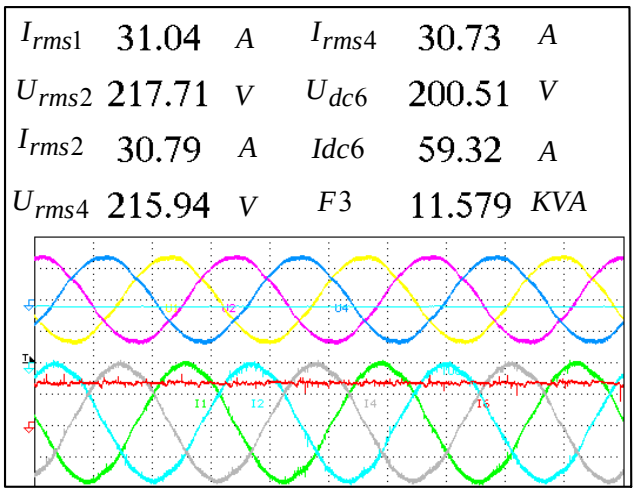
(b) $R = 2\Omega, [P_o, \eta] = [7.7KVA, 95.9\%]$

Figure 5.24. Output voltage, current, input current waveforms and its measured value for operation curve from the power meter on curve 1

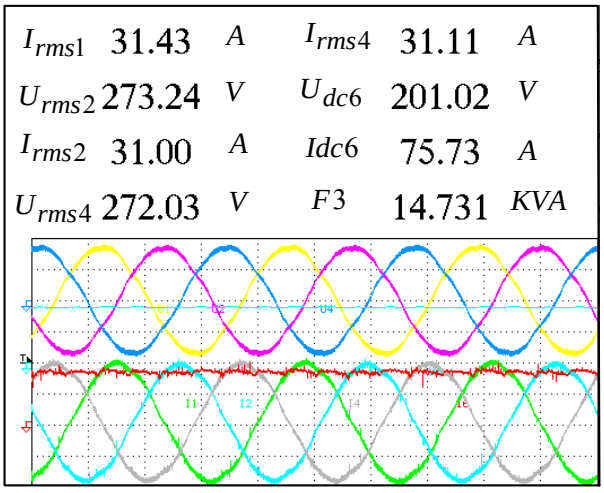
Figure 5.24 (cont'd)



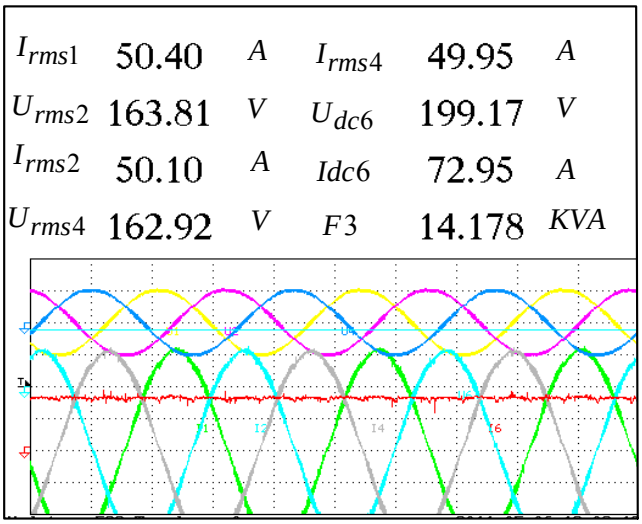
(c) $R = 3\Omega, [P_O, \eta] = [8.66KVA, 98.2\%]$



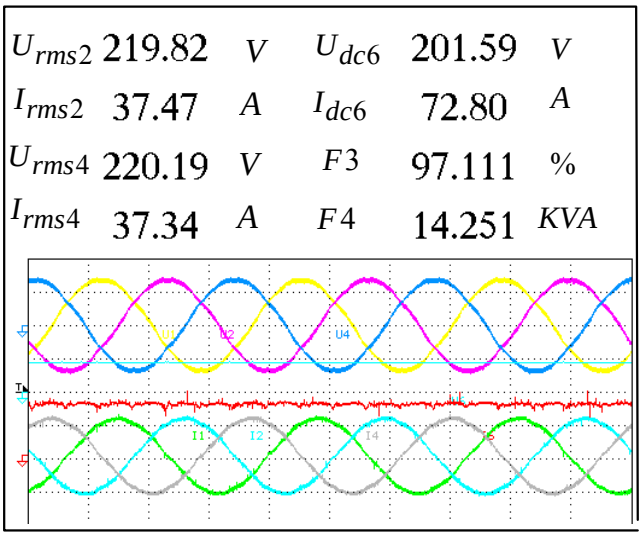
(d) $R = 4\Omega, [P_O, \eta] = [11.6KVA, 97.6\%]$



(e) $R = 5\Omega, [P_O, \eta] = [14.7KVA, 96.8\%]$



(a) $R = 1.8\Omega, [P_O, \eta] = [14.7KVA, 97.6\%]$



(b) $R = 3.45\Omega, [P_O, \eta] = [14.25KVA, 97.1\%]$

Figure 5.25. Output voltage, current, input current waveforms and its measured value for operation curve from the power meter on curve 2

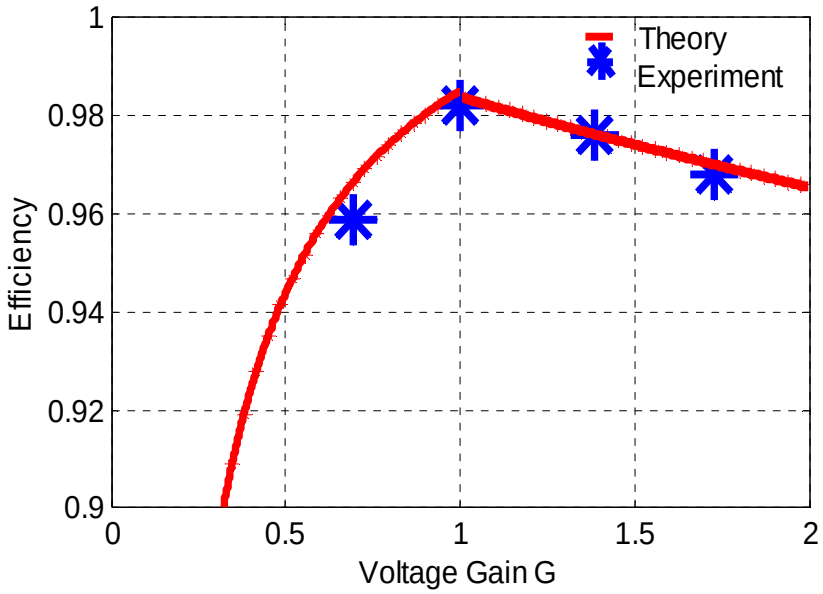


Figure 5.26. Measured & theoretic efficiency vs. Voltage gain G on curve 1

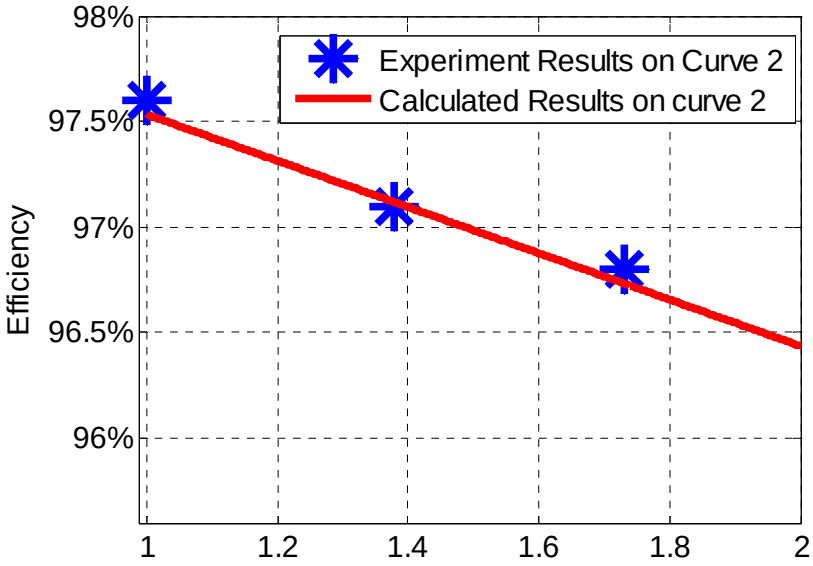


Figure 5.27. Measured & theoretic efficiency vs. Voltage gain G on curve 2, at constant P=15KW

5.6.6. Power Loss Breakdown

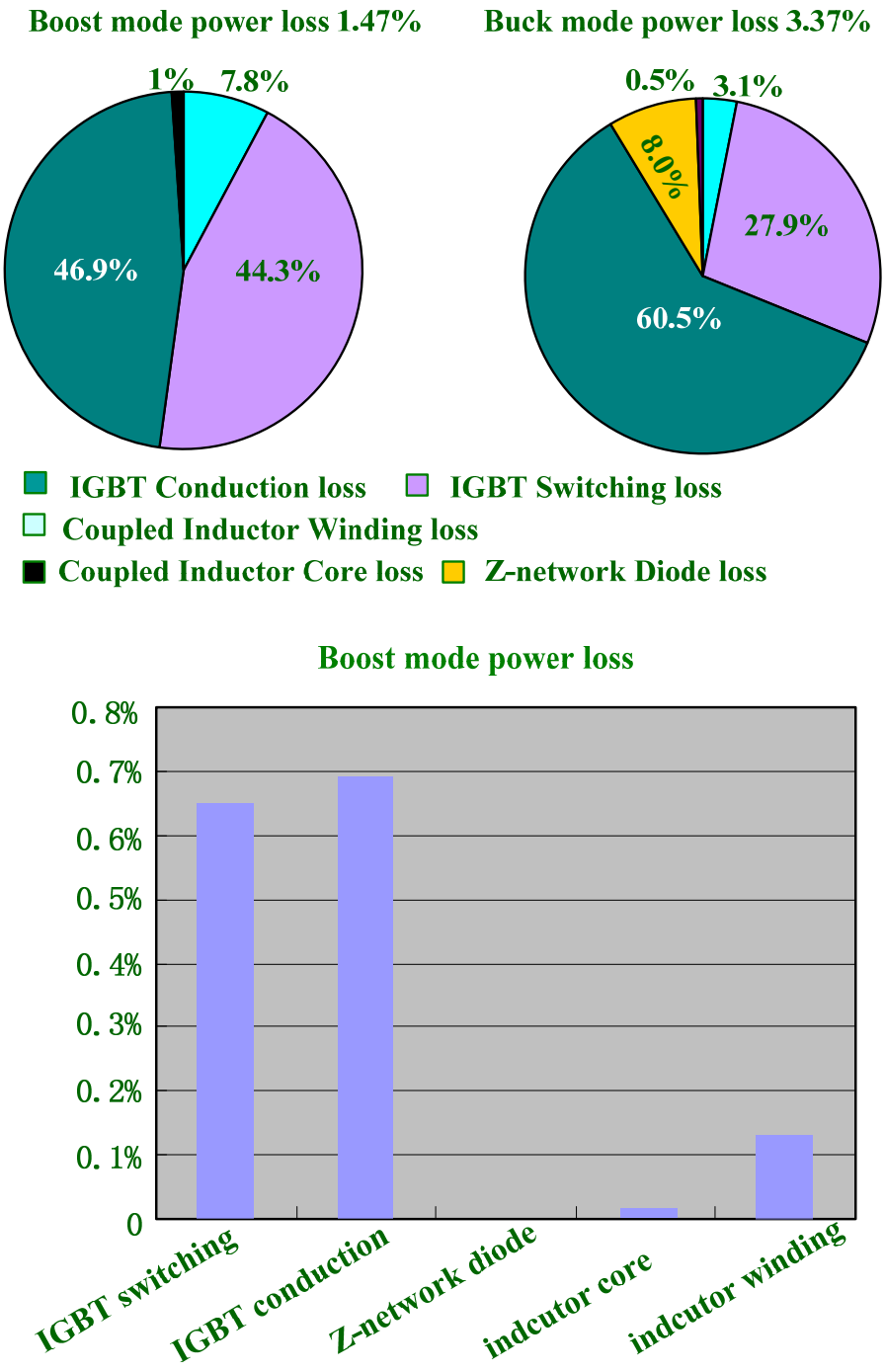


Figure 5.28. Power loss break down

Figure 5.28 (con'd)

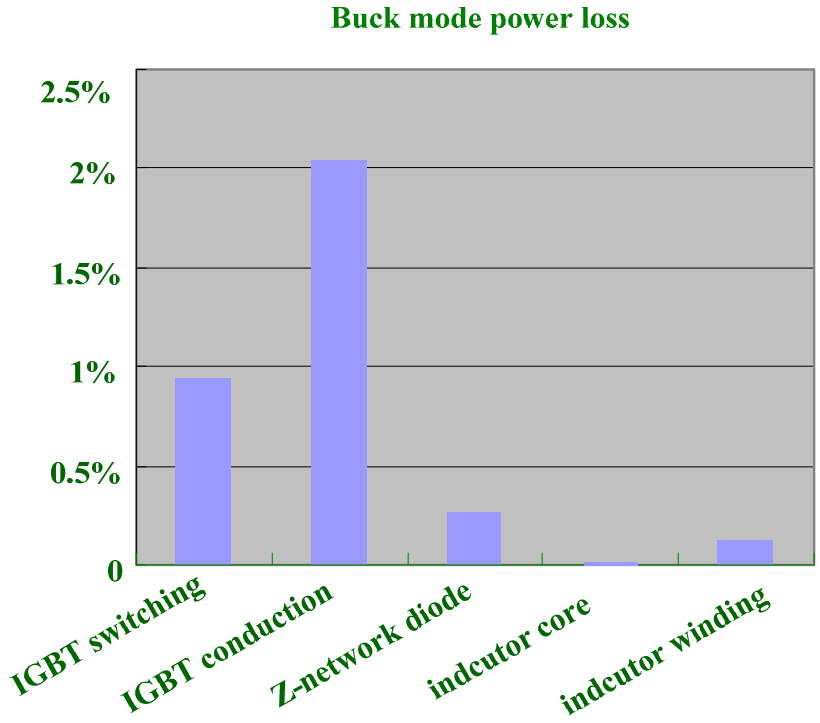


Figure 5.28. Power loss break down

Figure 5.28 shows the power loss break down between conduction, switching, diode, winding and core. It presents that the switching and conduction loss take up 90% of the total loss. The inductor loss takes only a small part of the whole power loss.

5.7. Summary

In the modified SVPWM control method for this circuit, different PWM sequences are listed and compared in terms of switching loss, current ripple, total harmonic distortion, and also the voltage spike on the switching devices. Concluded from different criterions, sequence III. B is selected in buck mode and sequence 3 is selected in boost mode as best sequences that can be utilized to obtain lower switching loss, lower current ripple, lower THD and lower voltage spike on the devices. It is utilized with the optimized hardware design together to achieve the best efficiency at full operation range. The experiment efficiency curve in terms of voltage gain from 0 to 2 at 15kW power rating is given. The best efficiency at 15kW reaches 97.6% at unity voltage gain.

CHAPTER 6 SVPWAM IN VSI AND CSI

-EXPERIMENTAL DEMONSTRATION

6.1. Introduction

In order to reduce the switching loss in the inverter, a space vector pulse-width-amplitude modulation (SVPWAM) has been proposed. If it is used in voltage source inverter, a front stage dc-dc converter is needed to generate a variable dc link voltage, and then fed to inverter. In HEV/EV motor drive application, the two stage boost-converter-inverter is a classical topology, since the battery voltage is designed to be lower or equal to half of the motor drive input voltage. Also because of this boost converter, the dc link voltage of inverter is possible to be controlled. This chapter proposes a Space-Vector-Pulse-Width-Amplitude Modulation (SVPWAM) method for buck-boost voltage/current source inverter. For voltage source inverter, the switching loss is reduced by 87%, compared to conventional SPWM method. For current source inverter, the switching loss is reduced by 60%. In both cases, the power density is increased by a factor of 2 to 3. In addition, it is also verified that the output harmonic distortions of SVPWAM is lower than SPWM, by only using 1/3 switching frequency of the latter one. A 1 kW boost-converter-inverter prototype has been built and tested using this modulation method. The maximum overall system efficiency of 96.7% has been attained at full power rating. The whole system power density reaches 2.3 kW/L and 0.5 kW/lb. The numbers are remarkable at this power rating. As a result, it is feasible to use SVPWAM to make the buck-boost inverter suitable for applications that require high efficiency, high power density, high temperature, and low cost. Such applications include EV motor drive or

engine starter/alternator. Secondly, for SVPWAM application in current source inverter, the topology “current-fed quasi-Z-source inverter” is selected to be a representative of a voltage buck/boost current source inverter. The dc link voltage can be controlled to be desired variable voltage by regulating the extra control freedom “open zero state duty cycle”. Simulation results are given to demonstrate the power loss reduction in this CSI case.

Currently, two existing inverter topologies are used for hybrid electric vehicles (HEVs) and electric vehicles (EVs): the conventional 3-phase inverter with a high voltage battery and a 3-phase PWM inverter with a dc/dc boost front end. Because of a wide voltage range and the limited voltage level of the battery, the conventional PWM inverter imposes high stress on switching devices and motor thus limits the motor’s constant power speed range (CPSR). The dc-dc boosted PWM inverter can alleviate the stress and limitations.

For example for series plug-in electric vehicle (PHEV), all the power generated by the generator has to flow through a synchronous rectifier to provide power to motor drive system. The battery is connected directly to the dc link if its voltage is high. Otherwise, a dc-dc boost converter is utilized as an interface. The inverter is required to inject low harmonic current to the motor, in order to reduce the winding loss and core loss. For this purpose, the switching frequency of the inverter is designed within a high range from 15 to 20 kHz, resulting in the switching loss increase in switching device and also the core loss increase in the motor stator. To solve this problem, various soft-switching methods have been proposed [86-92]. Active switching rectifier or a diode rectifier with small DC link capacitor have been proposed in [93-96, 98-99, 101-109]. Varies types of modulation

method have been proposed previously such as optimized pulse-width-modulation [110], improved Space-Vector-PWM control for different optimization targets and applications [111-116], and discontinuous PWM (DPWM) [117]. Different switching sequence arrangement can also affect the harmonics, power loss and voltage/current ripples [118-119]. DPWM has been widely used to reduce the switching frequency, by selecting only one zero vector in one sector. It results in 50% switching frequency reduction for both voltage source inverter and current source inverter. However, if an equal output THD is required, DPWM can not reduce switching loss than SPWM. Moreover, it will worsen the device heat transfer because the temperature variation caused by this discontinuous PWM. A double 120 flattop modulation method has been proposed in [97],[100] to reduce the period of PWM switching to only 1/3 of the whole switching period. That paper only mentioned the application in grid-connected inverter. It didn't compare the spectrum of this method with others. So its switching loss comparison is not fair. In addition, the method is only specified to a fixed topology, which can not be applied widely.

This chapter proposes a novel generalized space-vector -pulse-width-amplitude modulation (SVPWAM) method for the buck/boost voltage source inverter (VSI) and current source inverter (CSI). By eliminating the conventional zero vector in the space vector modulation, two third and one third switching frequency reduction can be achieved in VSI and CSI respectively. If a unity power factor is assumed, a 87% switching loss reduction can be implemented in VSI, and a 74% reduction can be implemented in CSI. A 1 kW boost-converter-inverter system has been developed and tested based on the SVPWAM method. A 90% power loss reduction compared to SPWM has been observed. The two

stage efficiency reaches 96.7% at the full power rating. The power volume density of the prototype is 2.3 kW/L. The total weight of the system is 1.51 lb. Therefore, a high efficiency, high power density, high temperature and low cost 1 kW inverter is achieved by using SVPWAM method.

6.2. Case study 1: 1kW SVPWAM-controlled boost-converter-inverter system for EV motor drive

6.2.1. Basic principle

The circuit schematic and control system for a 1 kW boost-converter-inverter motor drive system is shown in Figure 6.1. A 6ω dc link voltage is generated from a constant dc voltage by a boost converter, using open loop control. Inverter then could be modulated by SVPWM

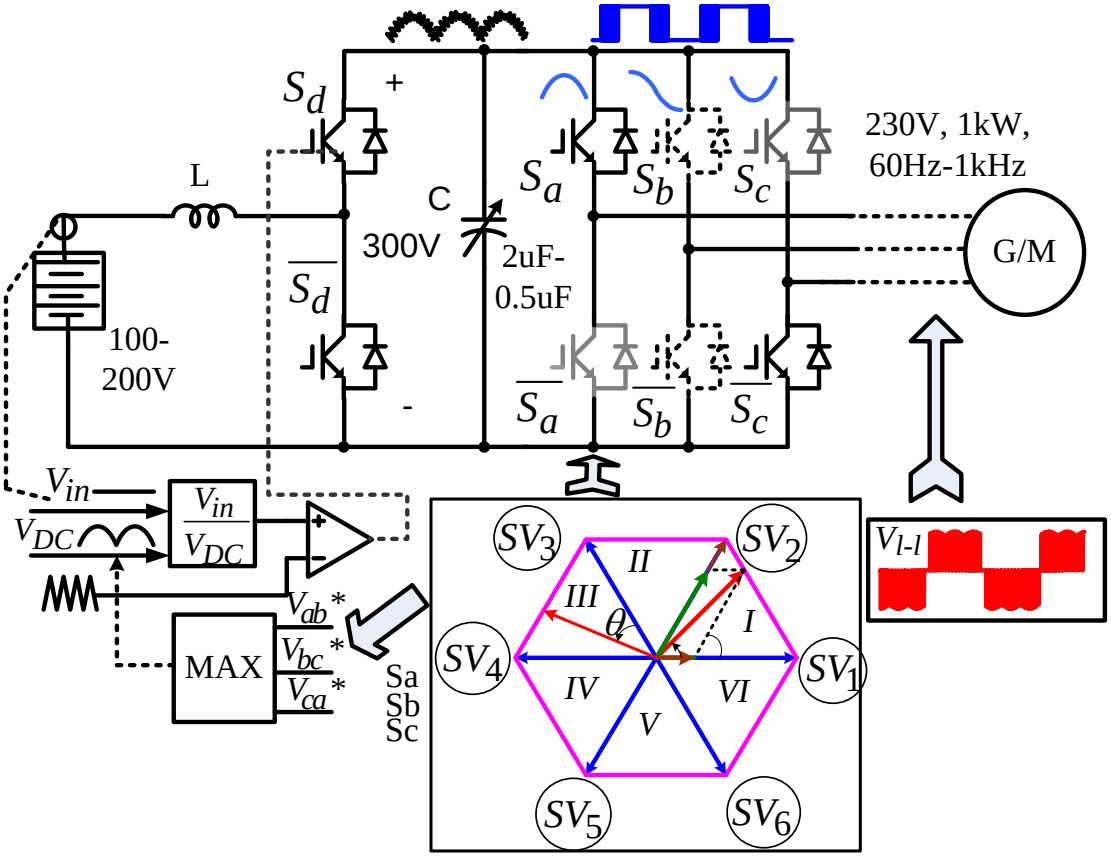


Figure 6.1. SVPWAM based boost-converter-inverter motor drive system

, to reduce the switching loss by 87%. The output line to line voltage has 6ω envelope at the top of PWM waveform.

The specifications for the system are: input voltage is 100-200 V; the average dc link voltage is 300 V; output line to line voltage rms is 230 V and frequency is from 60 Hz to 1 kHz.

6.2.2. DC link capacitor sizing

The purpose of the dc link capacitor is to absorb the current ripple and maintain a fairly constant voltage, here, a 6ω envelope voltage on the dc link. Thus the capacitance requirement is not as high as the traditional SPWM converter. Also a much faster control response can be achieved in this case.

In SVPWAM, the inverter operation has no zero state, thus the current flowing into the inverter varies between the maximum current and minimum current which occurs at maximum dc link voltage and minimum dc link voltage, respectively. The worst case capacitor voltage ripple happens at two cases:

(1) The upper switch of boost converter turns off, and maximum dc current flows into inverter;

(2) The upper switch of boost converter turns on, and minimum dc current flows into inverter;

The capacitor current in these two cases are:

$$\begin{cases} i_C = \dfrac{P_o}{V_{dc\_\min}} & case\ (1) \\ i_C = \dfrac{P_o}{V_{in}} - \dfrac{P_o}{V_{dc\_\max}} & case\ (2) \end{cases} \tag{6.1}$$

The nominal output line to line voltage for output is 230 V in this system. So the maximum

dc link voltage is 324 V and minimum is 280 V. When dc link voltage is minimum, the duty cycle for the lower switch is $1-V_{in}/V_{dc\_\min}=0.644$; when dc link voltage is maximum, the duty cycle for the upper switch is $V_{in}/V_{dc\_\max}=0.309$. Assume the switching frequencies for both boost bridge and inverter bridge are 20 kHz, and rated power is 1 kW. Assume the dc link voltage ripple is required to be within 10% of the nominal value. The capacitance can be calculated by:

$$C = i_C \cdot DT_s / (10\% \cdot 300) \tag{6.2}$$

The calculated capacitance for case 1 is 3.8 F and for case 2 is 3.3 F. So the final design value is 3.3 F here. The current capacity of the capacitor is determined by the maximum current flowing in the capacitor, which is the maximum between case 1 and case 2. The value of the maximum current here is 7 A.

Therefore, film capacitor can be used to replace the bulky and heavy electrolytic capacitor and thus the total volume and weight can be reduced significantly.

6.2.3. Voltage constraint and operation region

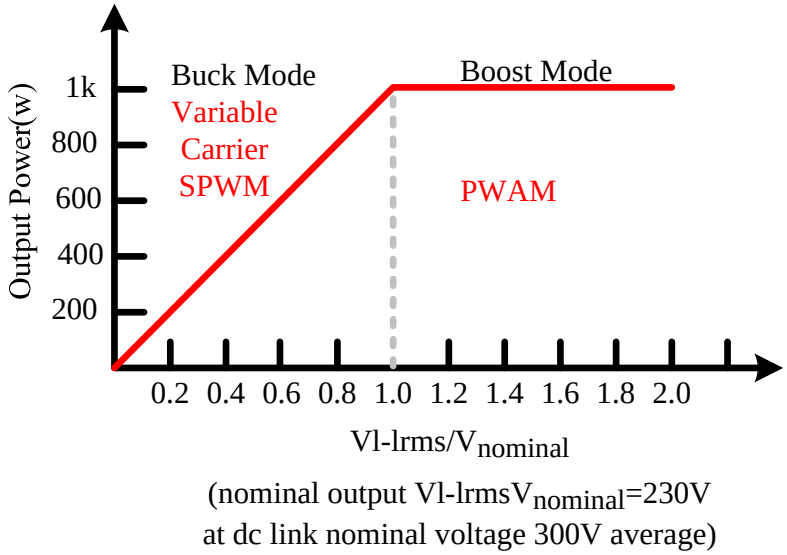


Figure 6.2. Operation region of the proposed boost-converter-inverter EV traction drive

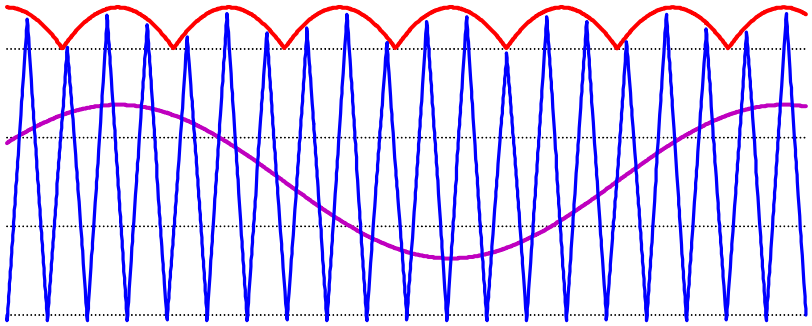


Figure 6.3. Variable Carrier SPWM control in buck mode

It is worth noting that the SVPWAM technique can only be applied when the batteries voltage falls into the region $V_{in} \le \frac{\sqrt{3}}{\sqrt{2}} V_{l-l}$ due to the step-up nature of boost converter. The constraint is determined by the minimum point of the 6ω dc link voltage. Beyond this region, conventional SPWM can be implemented. However, the dc link voltage in this case still varies with 6ω because of the small film capacitor we selected. Thus a modified SPWM with varying dc link voltage will be adopted during the motor start up as shown in Figure 6.2 and Figure 6.3. With 100~200 V batteries, the operation regions of the boost-converter-inverter motor drive are sketched as in Figure 6.2. Hence, the system will achieve optimum efficiency when the motor is operating a little below or around nominal voltage. When the motor demands a low voltage during start-up, efficiency is the same as conventional SPWM controlled inverter.

In SVPWAM control of boost mode, dc link voltage varies with the output voltage, in which the modulation index is always kept maximum. So when dc link voltage is above the battery voltage, dc link voltage level varies with the output voltage. The voltage utilization increased and the total power stress on the devices has been reduced.

6.2.4. Variable dc link SPWM control at high frequency

When the output needs to operate at a relative high frequency, like between 120 Hz

and 1 kHz, it is challenging to obtain a 6ω dc link voltage without increase of the switching frequency of boost converter. Furthermore, increasing boost converter switching frequency would cause a substantial increase of the total switching loss, as mentioned before. Because boost converter can not switch at a relatively low current as the three-phase inverter, so it takes up more than 75% of the total switching loss even though its switching frequency is the same as the one of inverter bridge.

Also a normal SPWM can not be used in this range because the capacitor is designed to be small in SVPWAM method. So it can not hold a constant dc link voltage even it is controlled to be. At a fixed design of dc link capacitor, the dc link voltage can not be controlled to be a six times a wide range of fundamental frequency.

Therefore, an optimum option is to control the dc link voltage at six times of a certain range of fundamental frequency, which the dc capacitor can hold, but do a variable dc link SPWM modulation for inverter to generate required high frequency fundamental voltage. The principle of this can be explained in Figure 6.4.

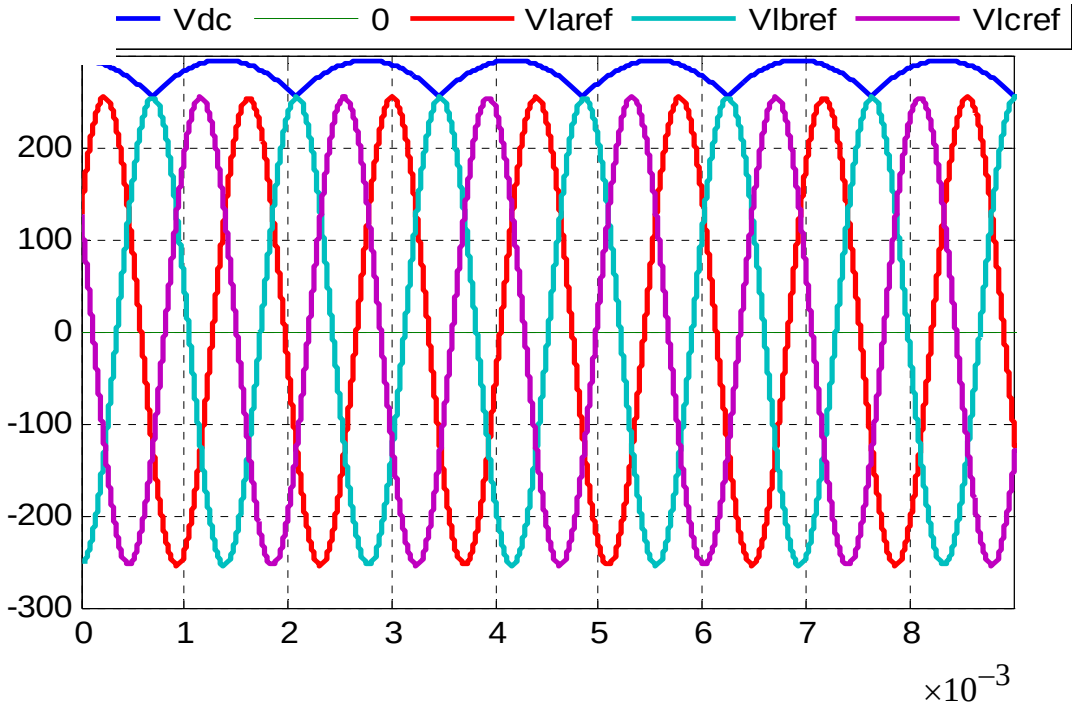


Figure 6.4. Variable dc link SPWM control at output frequency 720 Hz, and dc link frequency 720×1 Hz

In this variable dc link SPWM control, in order to get better utilization of the dc link voltage, an integer times between the dc link fundamental frequency and output frequency is preferred. When the output frequency is in [60 Hz, 120 Hz], a 6ω dc link is chosen; when the frequency is in [120 Hz, 240 Hz], a 3ω dc link is chosen; when the frequency is in [240 Hz, 360 Hz], a 2ω dc link is chosen; when the frequency is higher, a 1ω dc link can be chosen. An empirical formula can be used to select the proper frequency on dc link according to output frequency in order to obtain better voltage utilization and lower harmonic distortion. The dc link frequency ranges in [360 Hz, 720 Hz], thus the capacitor can be designed within this range.

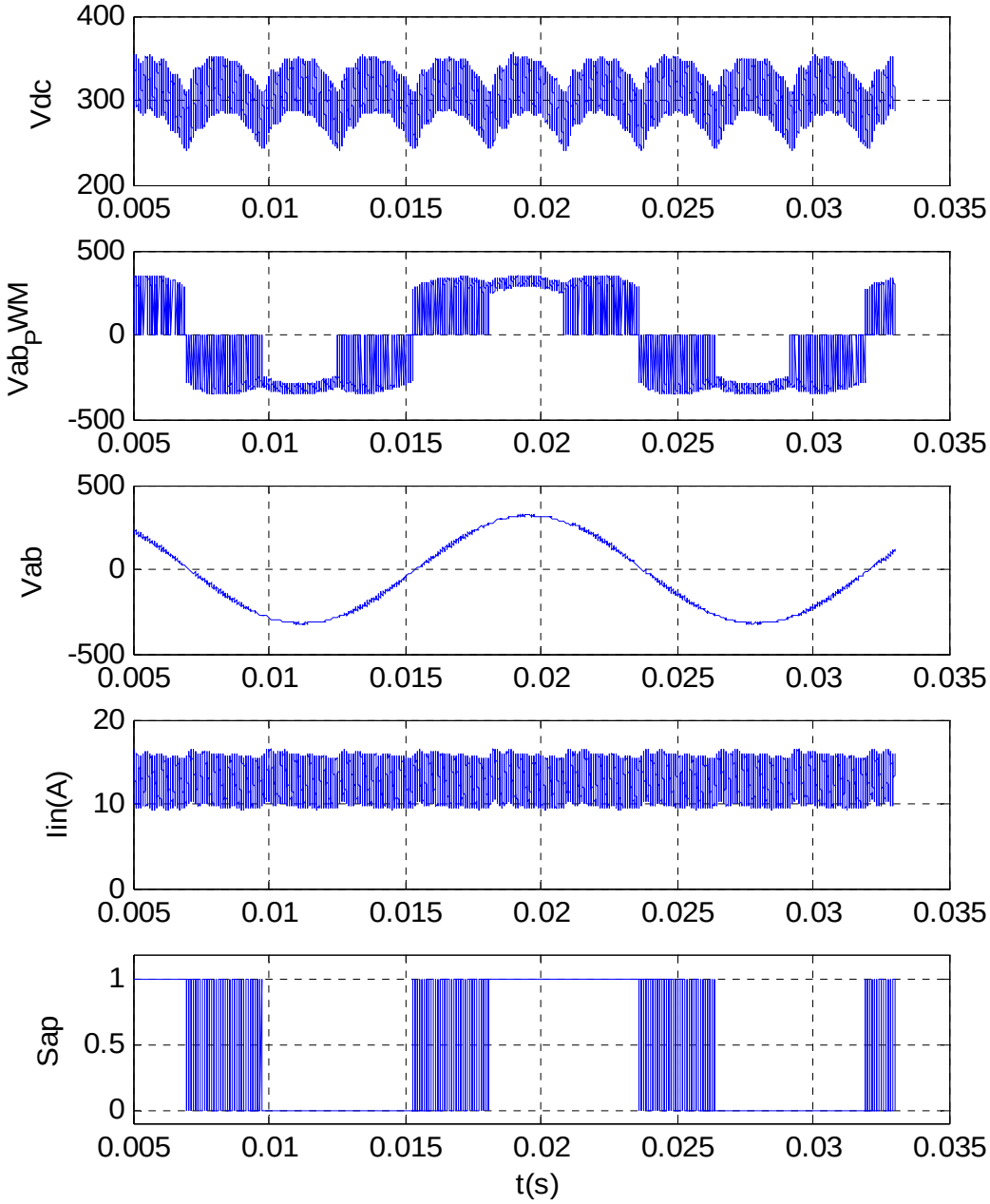


Figure 6.5. Simulation results of SVPWAM at 60 Hz, 1 kW

6.2.5. Simulation Results

The system parameters in the simulations and experiments are:

Continuous power: 1 KW; battery voltage: 100 -200 V;

output line voltage rms: 230 V; DC link voltage peak: 324 V; switching frequency: 20 kHz;

output frequency: 60 Hz - 1 kHz

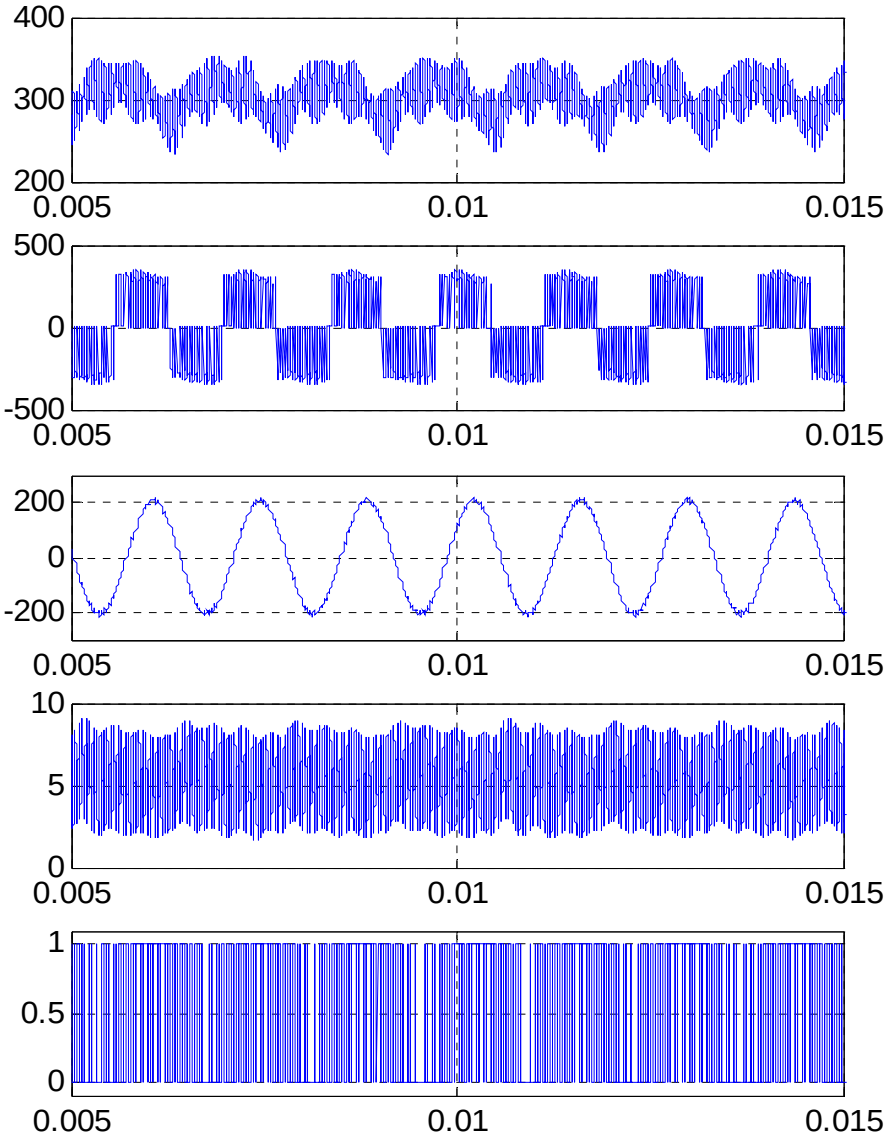


Figure 6.6. Simulation results of SPWAM at 720 Hz, 1 kW

Figure 6.5 shows the simulation waveforms of the proposed boost-converter-inverter HEV/EV traction drive in the SVPWAM operation region, at 60 Hz, 1 kW. The fundamental line-to-line voltage $V_{uv}(f_{un})$, phase leg center-tap voltageV_{un}, The DC bus voltageV_{dc}, the line-to-line voltage before filter and after filter, the input dc current, and the drive signal for Sap. Figure 6.6 shows the results of SPWM control at high frequency of 720 Hz, also at 1 kW.

6.2.6. Experiment results

(1) Experiment set up

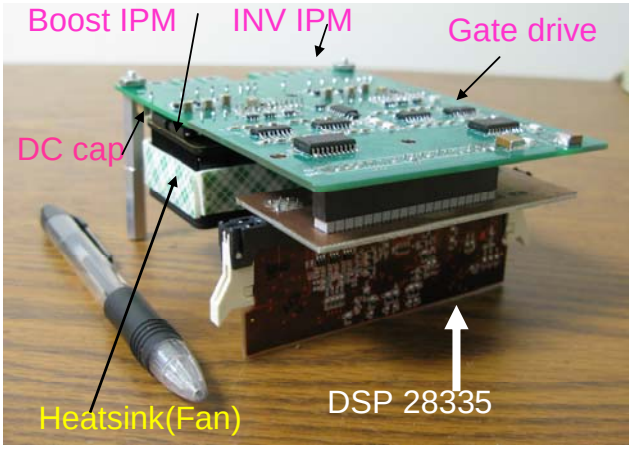


Figure 6.7. Hardware picture of the 1kW SVPWAM boost-converter-inverter

A 1 kW boost-converter-inverter prototype has been built in the laboratory to implement the SVPWAM control at 60 Hz and SPWM control at 1 kHz, in order to demonstrate their merits in reducing power loss and reducing the size compared to traditional methods. The picture of the hardware is shown in Figure 6.7. It includes DSP board, gate drive board, boost converter, three-phase inverter, heatsink and fan cooling system. The dimension is 11 cm × 8 cm × 5 cm, and the total weight is 1.5 lb.

The parameters used in the test are: rated power: 1 KW; battery voltage: 100-200 V; rated line voltage rms: 230 V; DC link voltage peak: 324 V; switching frequency: 20 kHz; output frequency: 60 Hz – 1 kHz

(2) SVPWAM control at 60 Hz

Figure 6.8-Figure 6.10 show the output and input voltage, current waveform when input voltage increases from 20 V to 100 V, while keeping the boost ratio constant. In this case, the output voltage increases linearly with input voltage increase. The output power increases in proportion to square of the input voltage. The output line to line voltage before the filter has the same shape as the second waveform in Figure 6.5, which demonstrates the

SVPWAM operation. The output line to line voltage after the filter overlaps with the 6ω dc link voltage by 60 degrees every fundamental cycle.

Figure 6.11 shows the three-phase line to line voltage and dc link voltage, and they overlapped very well. Figure 6.12 shows the efficiency test results by YOKOGAWA WT1600 Series power meter when the input voltage increases from 100 V to 200 V, while keeping the output power constant at 1 kW. The output line to line voltage rms keeps at 230V, and the dc link voltage is a 6ω varied waveform with 325V peak value. The output frequency is 60Hz, and switching frequency is 20kHz. In the data record on the power meter, Umn6, Umn4, Umn1 represent the phase line voltages; Irms6, Irms4, Irms1 represent 10 times of phase currents, because 10 circles of wires have been wound on the current transducer core of the power meter, in order to improve the measurement accuracy. Udc2 is input dc voltage and Idc2 is 10 times of average input dc current. F1 and F2 are the measured output and input power respectively. F3 is the efficiency that is calculated using F1/F2. F4 is the overall power loss. Figure 6.13 shows the efficiency test results when the power increases in proportional to square of input voltage. In this case, the dc link voltage and input voltage holds a constant boost ratio, since the output voltage is clamped by dc link voltage with modulation index always equal to one in the proposed SVPWAM method.

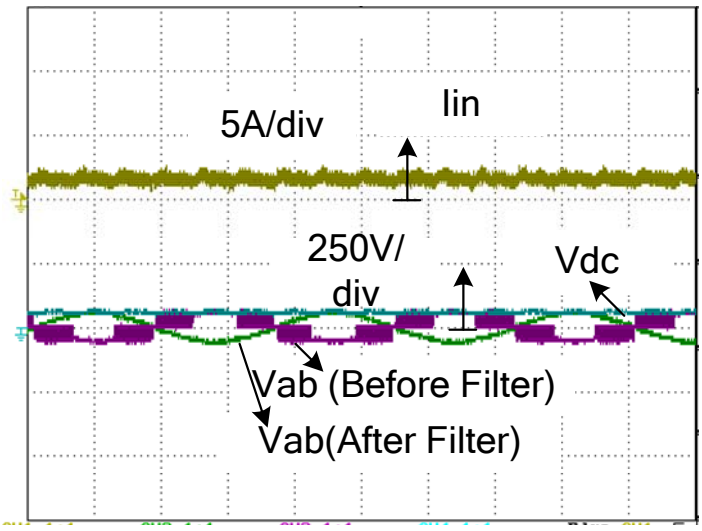


Figure 6.8. Output voltage and input current at *Vin=20V, Vdc_avg=60 V ,Vlrms=46V, Po=40W, fo=60Hz, fsw=20KHz*

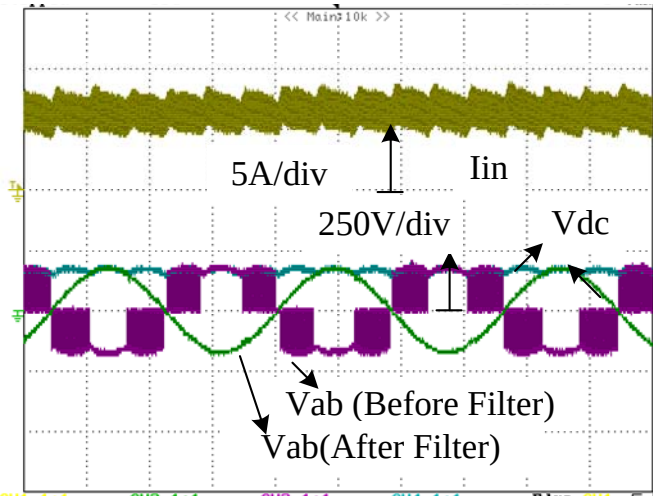


Figure 6.9. Output voltage and input current at *Vin=60V, Vdc_avg=180 V, Vlrms=138 V, Po=360 W, fo=60Hz, fsw=20KHz*

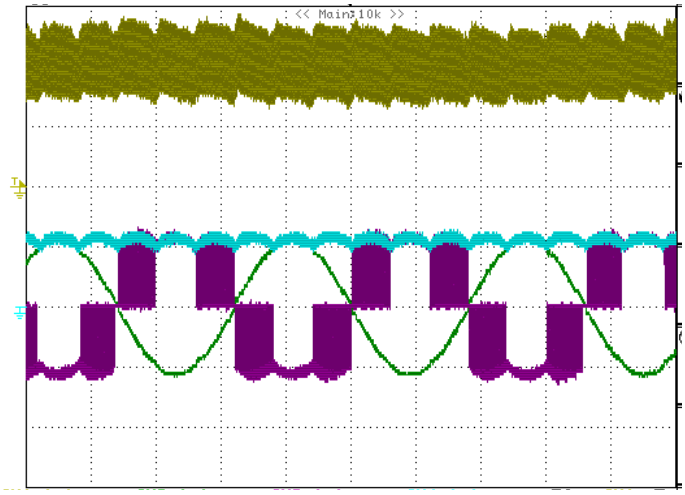


Figure 6.10. Output voltage and input current at *Vin=100 V, Vdc_avg=300 V, Vlrms=230 V, Po=1 kW, fo=60Hz, fsw=20KHz.*

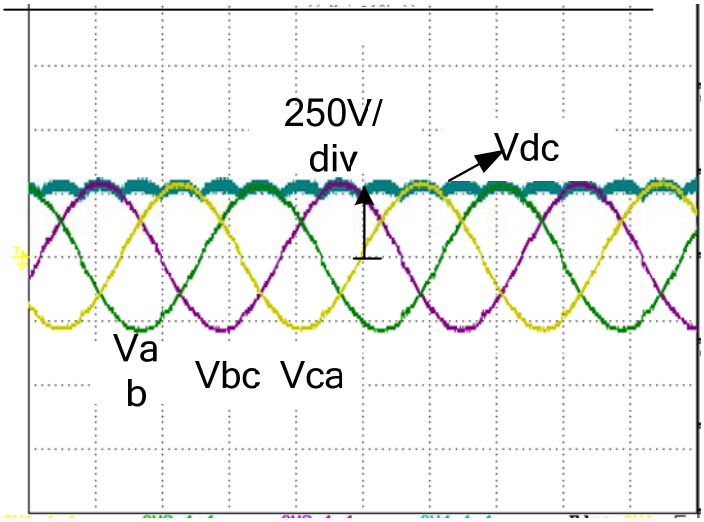
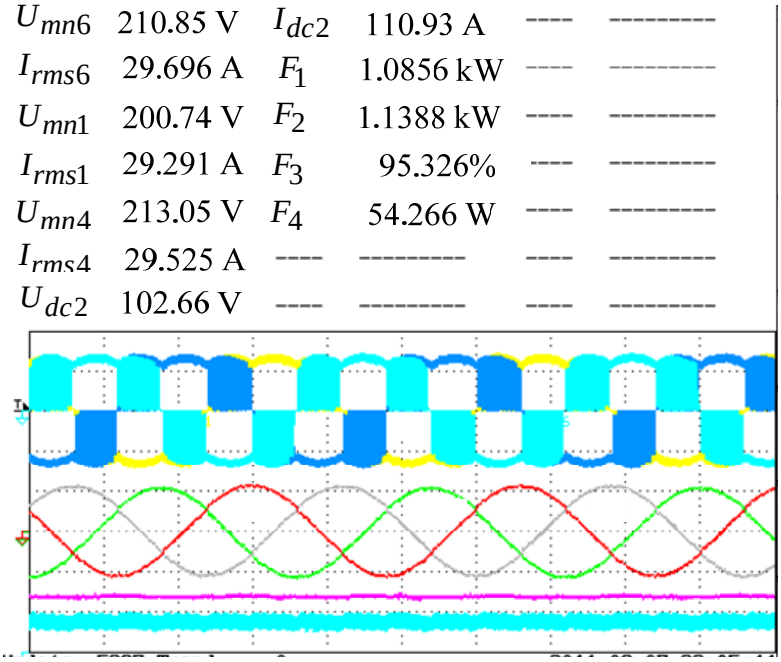
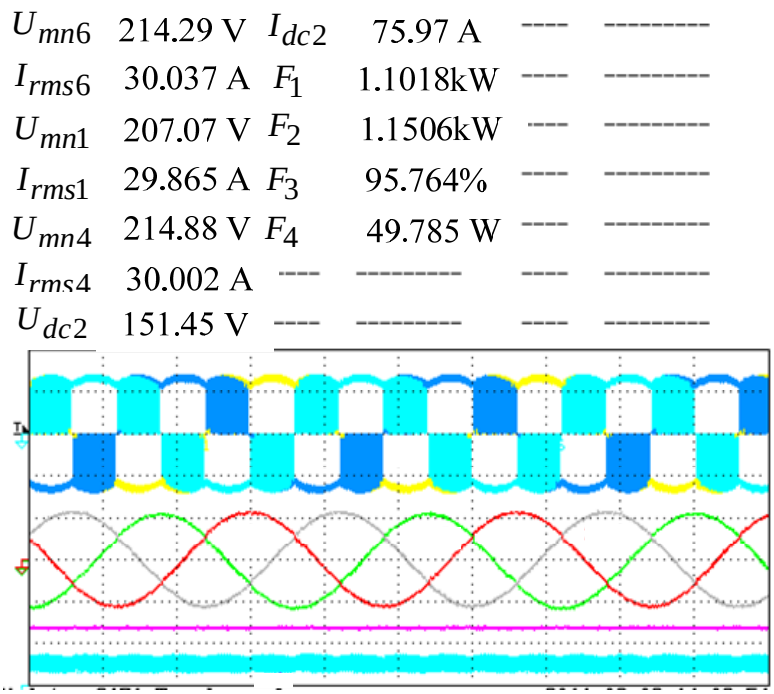


Figure 6.11. Output three phase line voltage and dc link voltage at *Vin=100 V, Vdc_avg=300 V, Vlrms=230 V, Po=1 kW, fo=60Hz, fsw=20KHz.*



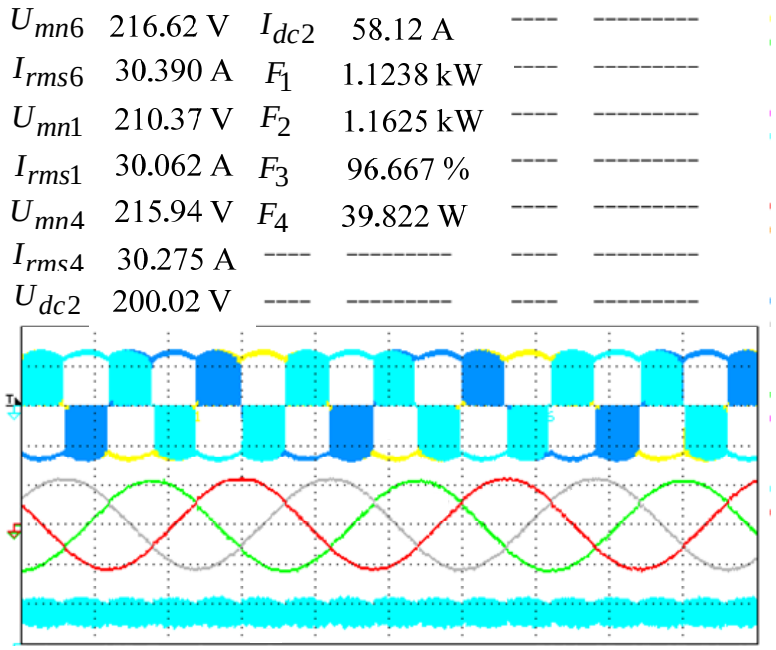
(a) *Vin=100V, Vdc_avg=300V, Vlrms=230V, Po=1kW, fo=60Hz,fsw=20kHz*



(b) *Vin=150 V, Vdc_avg=300 V, Vlrms=230 V, Po=1 kW, fo=60Hz, fsw=20kHz*

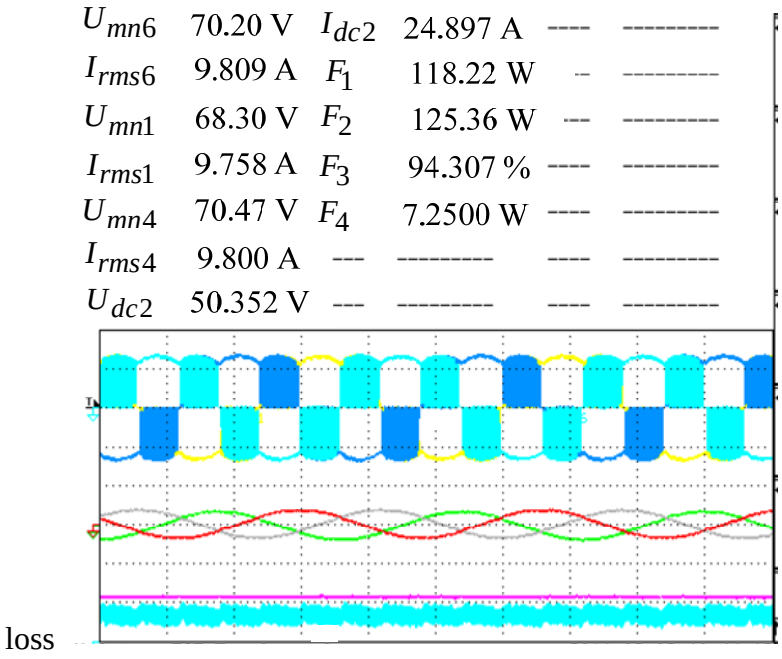
Figure 6.12. The results of efficiency test at constant full power rating 1kW

Figure 6.12 (cont'd)

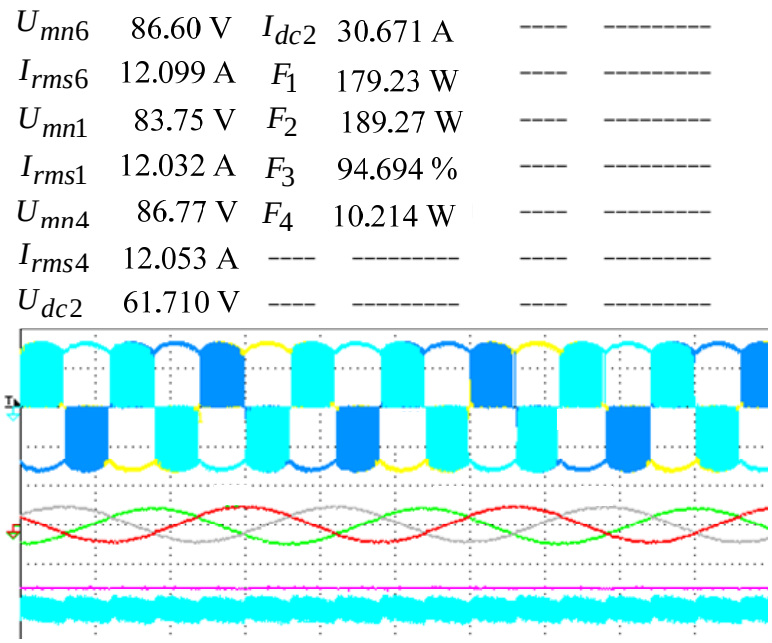


(c)*Vin=200 V, Vdc_avg=300 V, Vlrms=230 V, Po=1 kW, fo=60Hz, fsw=20kHz*

Figure 6.12. The results of efficiency test at constant full power rating 1kW but different input voltage by YOKOGAWA WT1600 Series power meter. Waveforms from the top to bottom: output line to line voltage before LC filter, output current, input voltage, input current. The numbers displayed on the screen represent: Umn6, Umn1, Umn4: RMS value of output line to line voltage before LC filter, like the first waveform shows; Irms6, Irms1, Irms4: 10 times of output line current; Udc2: input voltage; Idc2: 10 times of input current; F1: output power; F2: input power; F3: efficiency calculated from F1/F2; F4: total power



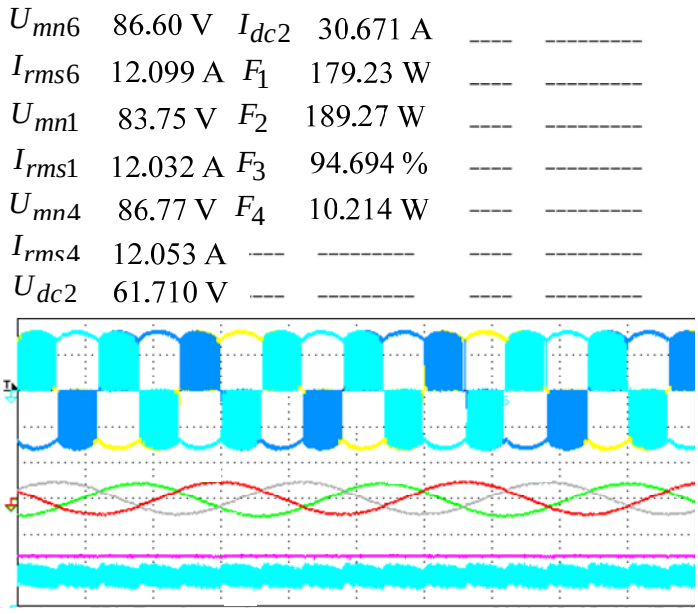
(a) *Vin=50V, Po=118W, Vdc_avg=100V, Vlrms=70V,Efficiency=94.3%*



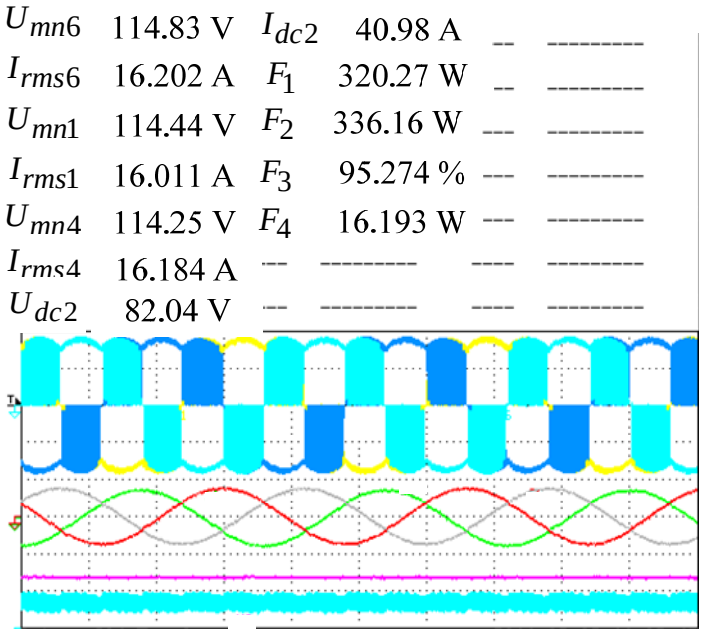
(b) *Vin=60V, Po=180W, Vdc_avg=120V, Vlrms=86V ,Efficiency=94.7%*

Figure 6.13. The efficiency test results when output power change proportionally with input voltage, in which the boost ratio of front dc-dc converter is constant; the waveforms have the same definition as Figure 6.12

Figure 6.13 (cont'd)

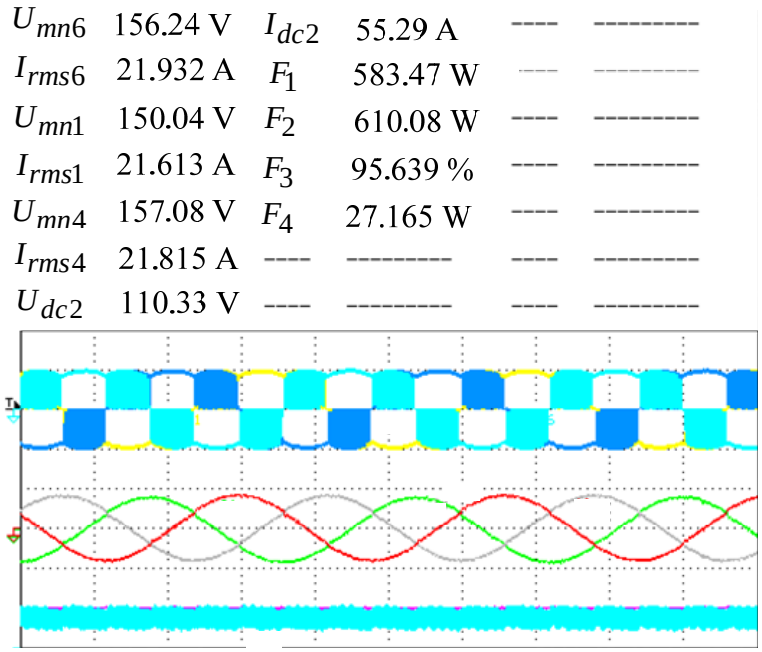


(c) *Vin=80V, Po=320W, Vdc_avg=160V, Vlrms=115V, Efficiency=95.3%*

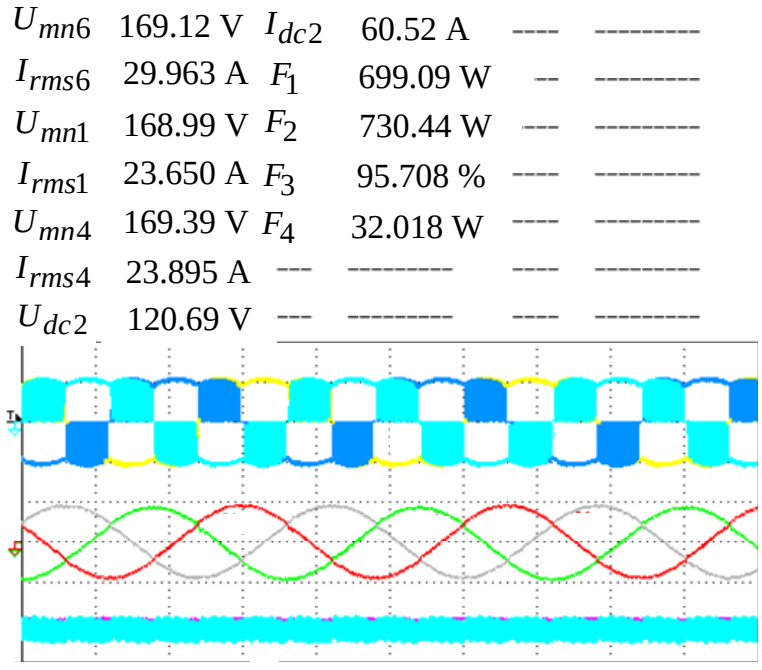


(d) *Vin=100V, Po=485W, Vdc_avg=200V, Vlrms=141V,Efficiency=95.5%*

Figure 6.13 (cont'd)

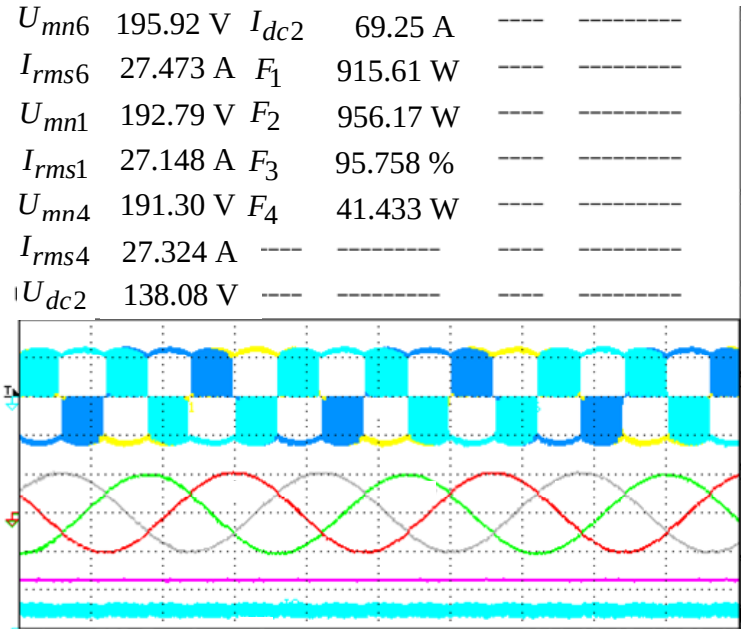


(e) *Vin=110V, Po=583W, Vdc_avg=220V,Vlrms=156,Efficiency=95.6%*

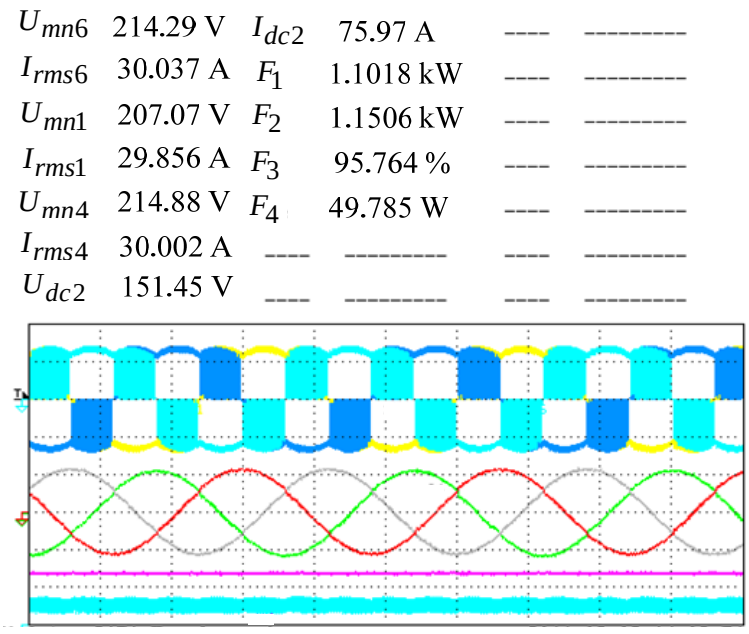


(f) *Vin=120V, Po=700W, Vdc_avg=240V,Vlrms=169V, Efficiency=95.7%*

Figure 6.13 (cont'd)



(g) *Vin=140V, Po=915W, Vdc_avg=280V, Vlrms=195V,Efficiency=95.8%*

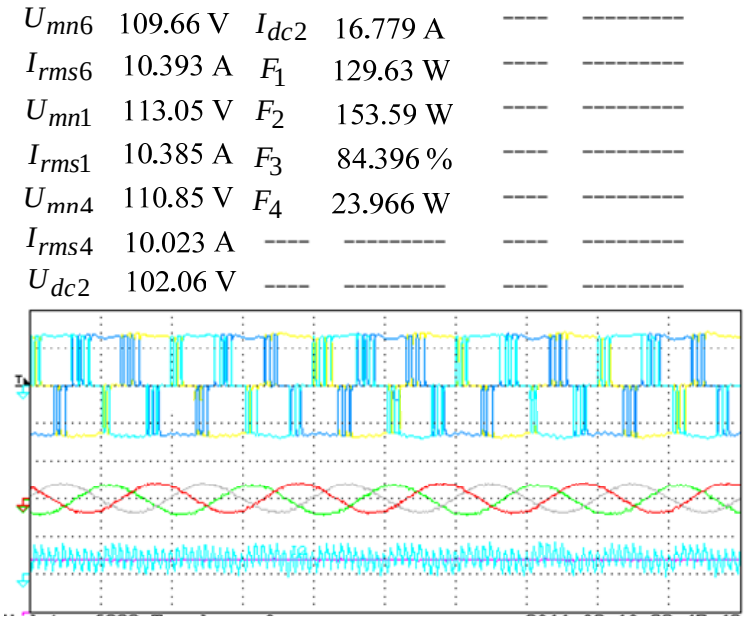


(h) *Vin=150V, Po=1102W, Vdc_avg=300V, Vlrms=230V,Efficiency=95.8%*

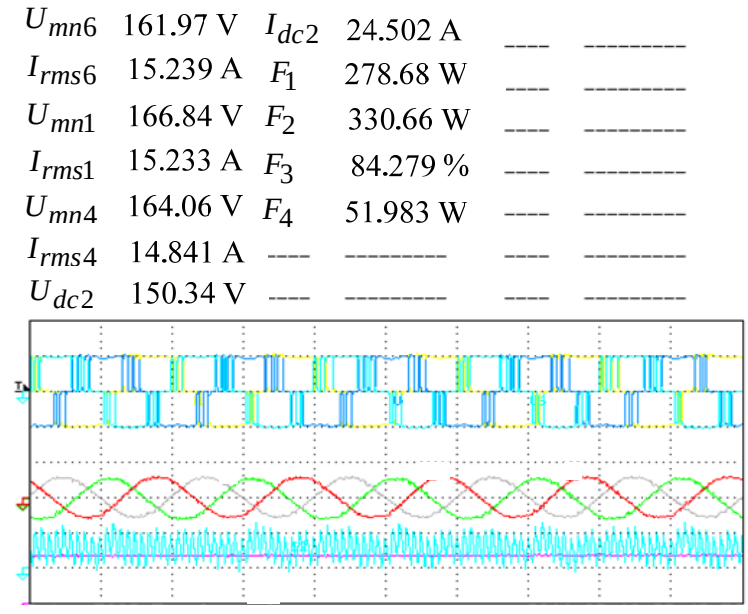
Figure 6.13. The efficiency test results when output power change proportionally with input voltage, in which the boost ratio of front dc-dc converter is constant; the waveforms have the same definition as Figure 6.12

(3) Output three phase voltage at 1kHz

When the output frequency increases to 1kHz, the measured voltage and current waveforms and efficiency are shown in Figure 6.14 at input voltage of 100V and 150V. The efficiency is around 84% for both cases, lower than 60Hz case.



(a) *Vin=100 V* at *fo=1 kHz*



(b) *Vin=150 V* at *fo=1 kHz*

Figure 6.14. The efficiency test at 1kHz: output l-l voltage, output current, input current

(4) Overall efficiency and Power loss comparison between SVPWAM and SPWM

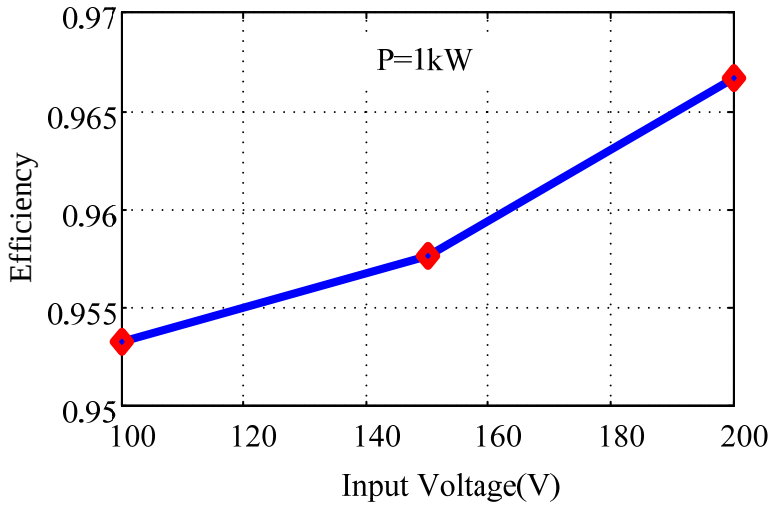


Figure 6.15. Measured overall efficiency when input voltage changes from 100 V to 200 V at 1 kW power rating corresponding to Figure 6.12

($f_o = 60Hz, f_{sw} = 20kHz, V_{dc\_peak} = 325V, Vo_{l-lrms} = 230V$)

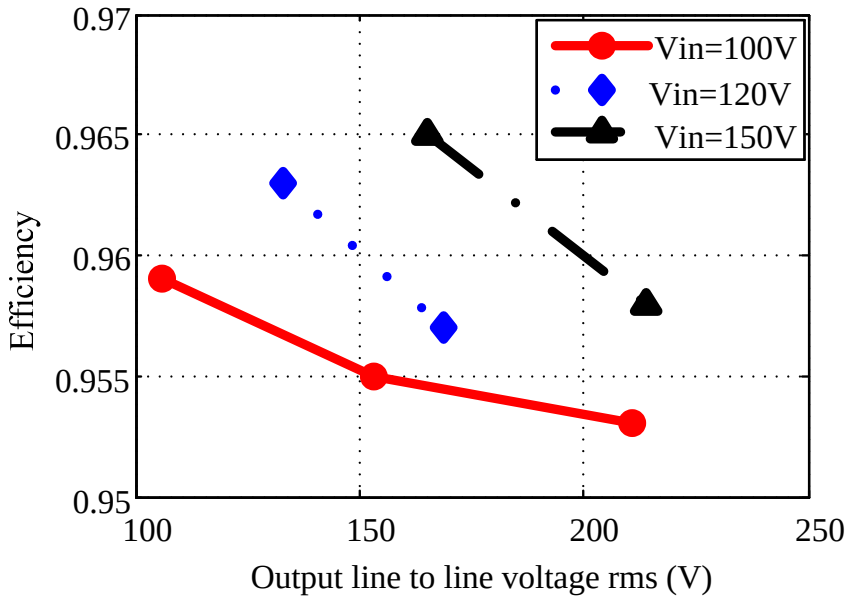


Figure 6.16. The efficiency test results when output voltage/output power changes with a constant input voltage: at different voltage level including 100V, 120V and 150V from Figure 6.12 (a), Figure 6.13(d) and other results

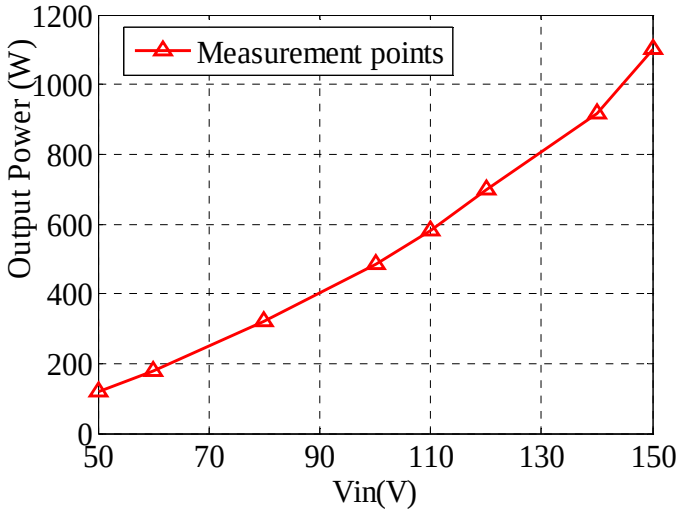


Figure 6.17. The efficiency test curve when output power changes proportionally with input voltage (Vin from 50V to 150V, Po from 120W to 1kW), corresponding to experimental waveforms in Figure 6.13

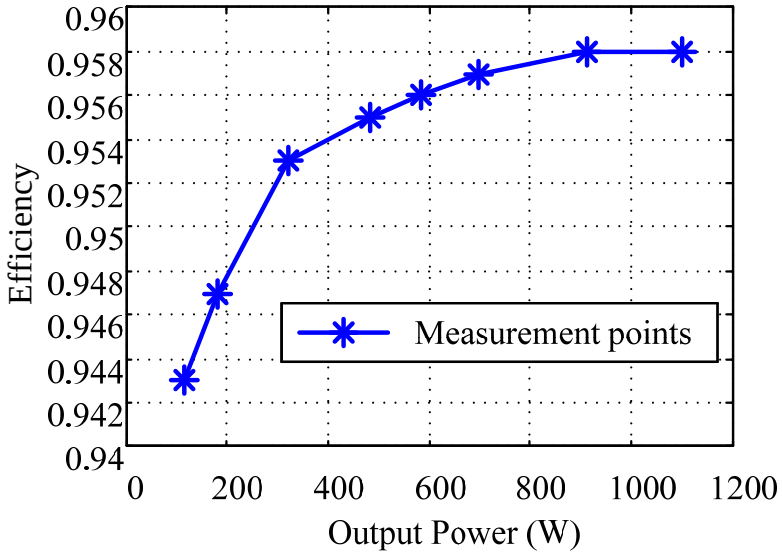
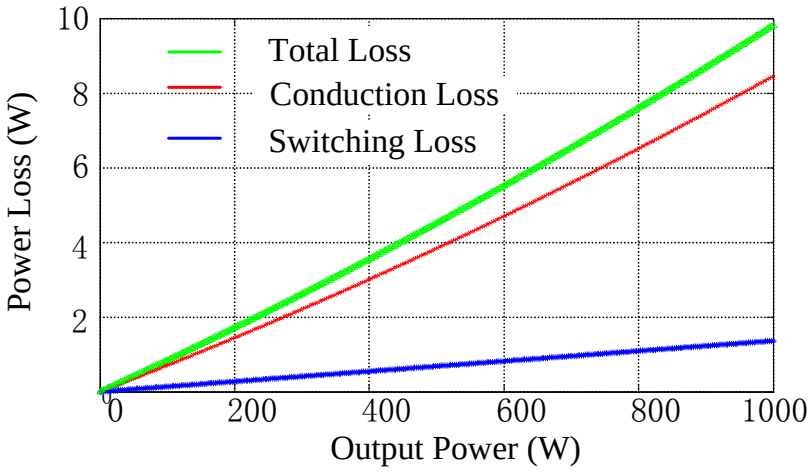
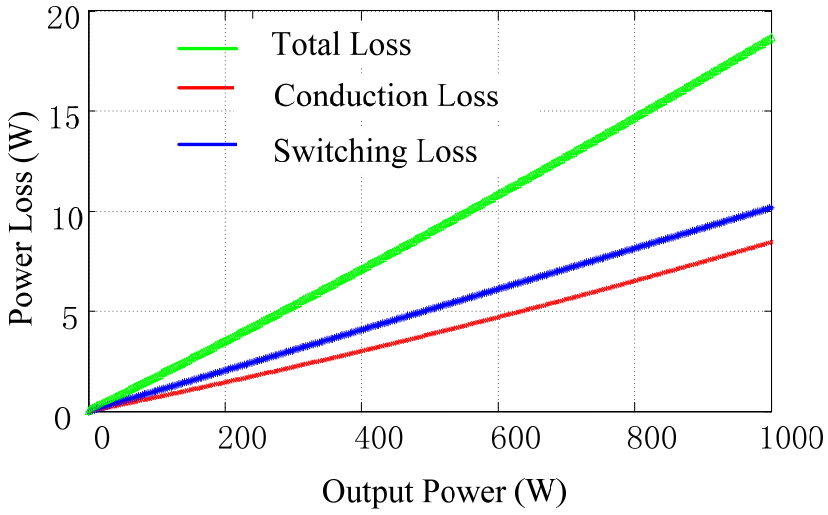


Figure 6.18. The efficiency test results corresponding to curve in Figure 6.17

Figure 6.15 shows the measured efficiency when the input voltage increases from 100 V to 200 V, all at 1 kW power rating. The DC link is a 6ω varied voltage with constant peak value of 325V, and the output line to line voltage is also a constant 230V in rms. The output frequency is 60Hz, and the switching frequency is designed at 20kHz for both inverter and boost converter. The overall efficiency increases as the input voltage increases, because the efficiency of boost converter increases when the input voltage increases. The maximum efficiency at 1 kW reaches 96.7% at input voltage 200 V. Figure 6.16 shows the measured efficiency at a constant input voltage but different output voltage, which also results in different output power. It is observed that when output voltage/power increases, the efficiency decreases a little bit, partly because of the increased conduction loss and switching loss caused by higher input current and output current. Figure 6.17 shows the measured voltage and power corresponding to the waveforms in Figure 6.13, and Figure 6.18 is the corresponding efficiency results. In these two results, the power increases proportional with the input voltage square, in another word, the dc link voltage increases proportionally with input voltage. In SVPWAM, the output voltage is clamped by dc link voltage, which means the inverter modulation is always equal to 1. The efficiency results reveal that the higher efficiency can be achieved at higher power rating in this case.



(a) SVPWAM



(b) SPWM

Figure 6.19. Comparison between inverter power losses in the condition that dc link voltage changes from 0 to full rating at 300V

Figure 6.19 (a) and (b) show the power loss estimation (from the loss model mentioned before) of the inverter when the power increases from 0 to full rating under two methods. Since the research target is only inverter, the test condition is based on varying the output power by changing output voltage from 0 to 230V. It is observed that in SVPWAM method, conduction loss accounts for 80% of the total power loss, but in SPWM method, switching

loss is higher than conduction loss. The switching loss is reduced from 10 W to 1.4 W from SPWM to SVPWAM. An estimated 87% switching loss reduction has been achieved.

6.2.7. Conclusion for case study 1

The SVPWAM control method preserves the following advantages compared to traditional SPWM and SVPWM method:

◆ The switching power loss is reduced by 90% compared with the conventional SPWM inverter system.

◆ The power density is increased by a factor of 2 because of reduced dc capacitor (from 40 F to 6 F) and small heat sink is needed.

◆ The cost is reduced by 30% because of reduced passives, heat sink, and semiconductor stress.

A high efficiency, high power density, high temperature and

low cost 1 kW inverter engine drive system has been developed and tested. The effectiveness of the proposed method in reduction of power losses ahs been validated by the experimental results that obtained from the laboratory scale prototype.

6.3. Case study 2 : SVPWAM for normal current source inverter with 6ω dc link current

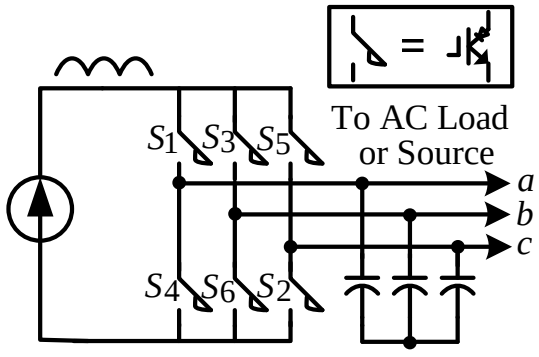
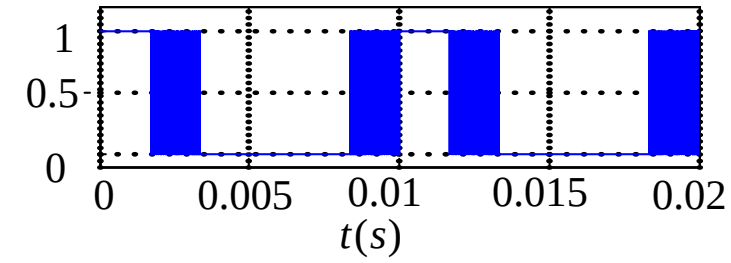


Figure 6.20 Conventional current source inverter for PWAM

In SVPWAM, the elimination of zero state doesn't affect the output waveform, but do affect the input current, which can not be a dc current but a dc current with 6ω ac ripple. ω refers to the fundamental frequency. Thus a dc-dc stage or an integrated dc-dc stage like the Z-source network has to be cascaded in front to generate this 6ω current on the dc link, instead of using of single stage inverter. For the first example here an ideal 6ω ripple dc current source is utilized for conventional current source inverter as Figure 6.20.

The simulation parameters are: $I_{dcm} = 20A, f_s = 20kHz$, $f_0 = 100Hz$. Figure 6.21 shows the simulation results for switching function, input and output current before and after the filter. It can be observed that, the output current directly utilizes the input current during two 60 degree sections, one positive and one negative. The current after the filter has a little phase shift with input dc current because of the capacitor.



(a)

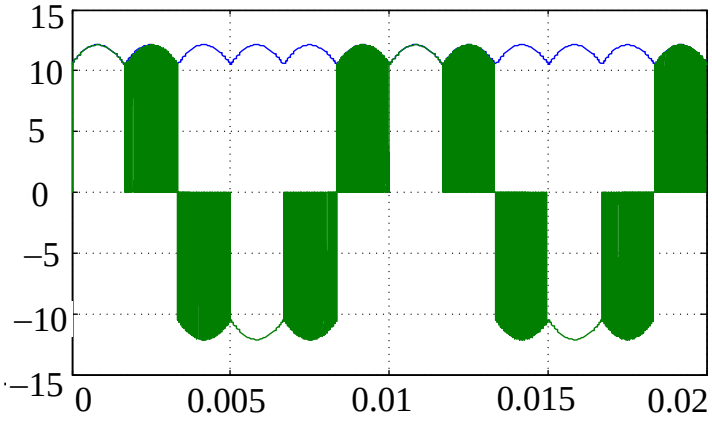
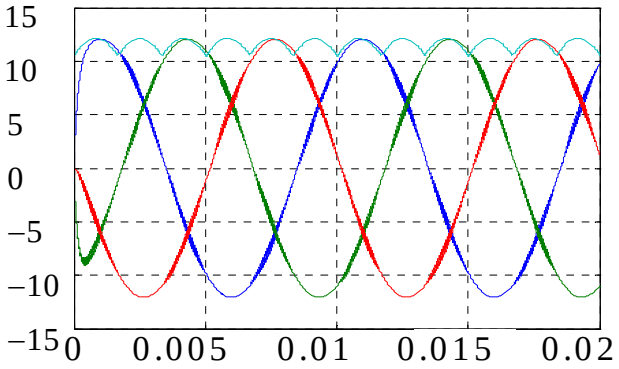


Figure 6.21. Simulation results for PWAM CSI: (a) switching waveform (b) Input dc link current and output one phase current before the filter (c) input current and output current

Figure 6.21 (cont'd)



(c)

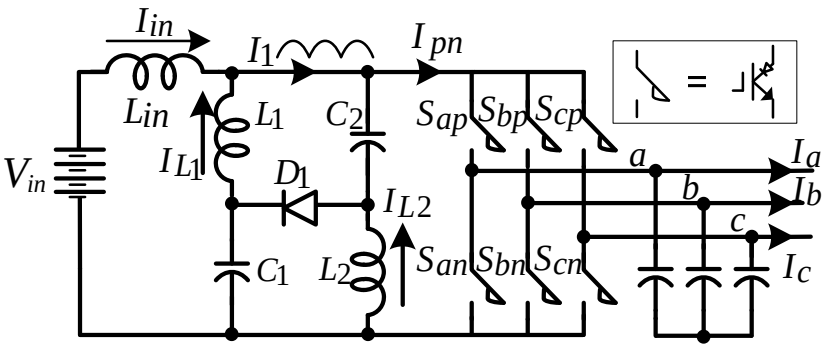


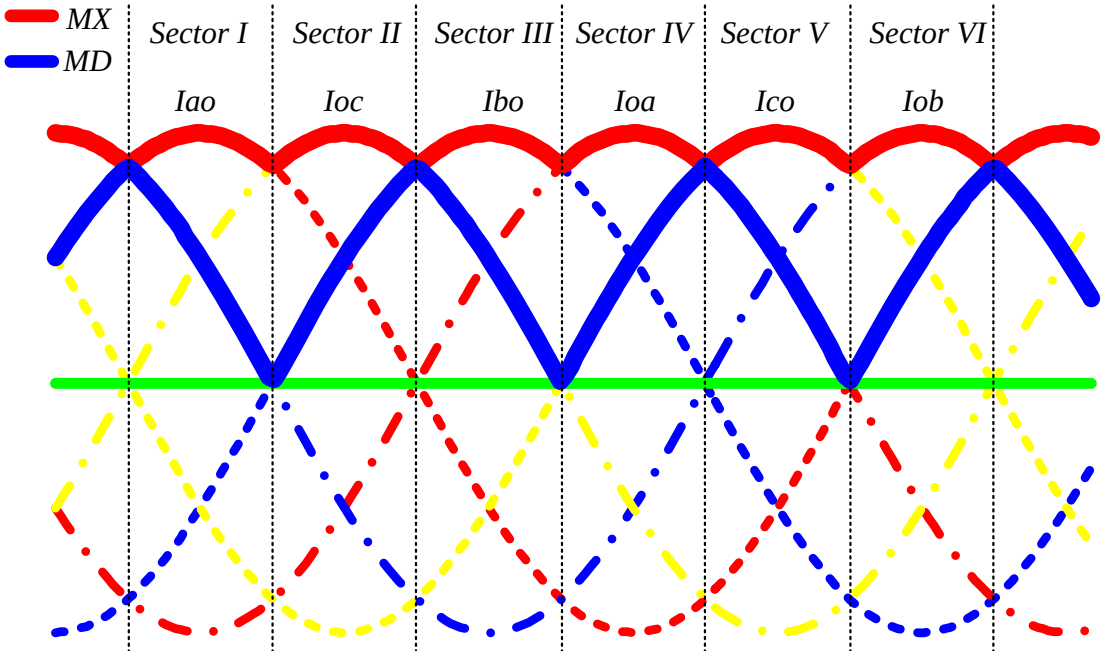
Figure 6.22. Circuit configuration of current-fed Quasi-Z-Source-Inverter

6.4. Case study 3: SVPWAM for current-fed quasi-Z-source inverter

The front stage can also be integrated with inverter to form a single stage. Take current-fed quasi-Z-source inverter as an example. Instead of controlling the dc link current *Ipn* to have a constant average value, the open zero state duty cycle will be regulated instantaneously to generate a 6ω fluctuate dc average current, which is overlapped with the output three line current. It is also equivalent to control I_1 to be a 6ω fluctuate dc current. The reason is that the average dc link current I_1 shown in Figure 6.22 is related to the input dc current I_{in} by a transfer function:

$$I_1 = \frac{1-D_{op}}{1-2D_{op}} I_{in} \tag{6.3}$$

, in which D_{op} is the open zero state duty cycle [1-2]. With this transfer function, I_1 can be controlled to be a 6ω varied waveform by regulating D_{op} , resulting in a pulse type 6ω waveform at the real dc link current I_{pn} .



Sap	*	1	*	0	0	0
Sbp	0	0	*	1	*	0
Scp	*	0	0	0	*	1
San	0	0	0	*	1	*
Sbn	1	*	0	0	0	*
Scn	0	*	1	*	0	0

** : Switching between 0 and 1*
MX: Maximum line current envelope, also the average DC link current Ipn
MD: Medium line current, also the PWM reference

Figure 6.23. PWAM modulation principle

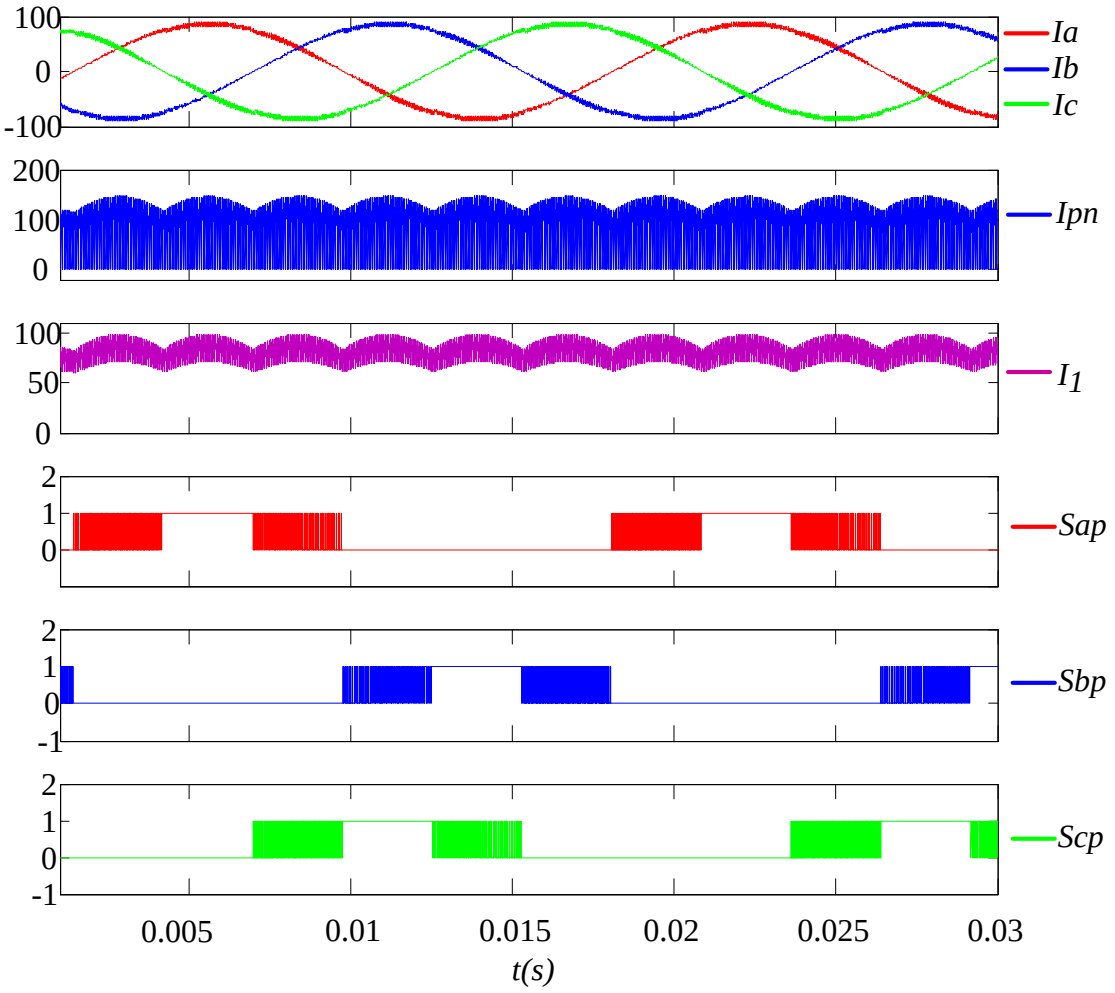


Figure 6.24 Simulation results

The basic switching patterns for PWAM current-fed quasi-Z-source inverter are shown in Figure 6.23. The red curve is the reference dc link current, which is also the envelope of the three-phase current because no zero state exists in the circuit. For each 60 degree range, only two switches are doing PWM modulation. It reduces the switching times of the original SPWM method by 2/3. In open zero state, only one switch is turned on; in non-open zero state, one switch in upper or lower half legs keeps on all the time, and another two switches in another half legs but in different phase legs are turned on and off complementarily, except some dead-time between them created by the insertion of the open zero state. Figure 6.24 shows the simulated output current, dc link pn current, input average

current Il, and also the switching waveforms of S_{ap}, S_{bp}, S_{cp}.

6.5. Summary for chapter 6

For VSI application, the SVPWAM control method preserves the following advantages compared to traditional SPWM and SVPWM method:

- The switching power loss is reduced by 90% compared with the conventional SPWM inverter system.
- The power density is increased by a factor of 2 because of reduced dc capacitor (from 40 F to 6 F) and small heat sink is needed.
- The cost is reduced by 30% because of reduced passives, heat sink, and semiconductor stress.

A high efficiency, high power density, high temperature and low cost 1 kW inverter engine drive system has been developed and tested. The effectiveness of the proposed method in reduction of power losses ahs been validated by the experimental results that obtained from the laboratory scale prototype.

For CSI application, the SVPWAM control method posses the following benefits compared to commonly used DSVPWM method:

- Switching loss is reduced by 60% at PF=1
- Lower inductance is required for the inductor
- Lower harmonics at output current

An example of current-fed quasi-Z-source inverter is simulated to verify the effectiveness of SVPWAM in current source inverter.

CHAPTER 7 SVPWM FOR DIRECT Z-SOURCE MATRIX CONVERTER – SHOOT-THROUGH CONTROL

7.1. Introduction

The matrix converter (MC) is a direct ac/ac converter with sinusoidal input/output waveforms and controllable input power factor [49-51]. Different from direct AC/AC converter, its input and output frequency can be arbitrary. Compared to traditional variable frequency back to back topology, it has three less passive component. However, it can only buck the voltage. Its control methods, circuit operation and possible applications have been investigated in paper [52-70]. It has a good perspective especially when the reverse-blocking IGBT is available now.

The switching rule of MC is that in each phase leg, only one and at least one switch is at on state. In a traditional voltage-fed matrix converter, the three switches on the same output phase leg can not be gated on at the same time because doing so would cause a short circuit(shoot through) to occur, which would destroy the converter. In addition, the maximum voltage gain can not exceed 0.866. These limitations can be overcome by Z-source matrix converter [1], which adds an impedance network (Z-network) in the input phase lines. The Z-source matrix converter advantageously utilizes the shoot through states to boost the ac voltage by gaiting on all the three switches on the same output phase leg. Therefore, the Z-source matrix converter can boost the voltage to be greater than the input voltage. In addition, the reliability of the converter is greatly improved because the shoot through states can no longer destroy the circuit. Also the current commutation steps can be simplified. Therefore, it provides a low-cost, reliable, and highly efficient structure for buck and boost

ac/ac conversion.

Z-source direct matrix converter has several topologies, depending on the different structure of the Z-network, each of which has advantages over others and also disadvantages. A family of direct Z-source matrix converter has been shown in Figure 2.12. For voltage-fed (VF) Z-source MC, its voltage gain can only reach 1.15, and also the phase shift caused by the Z-network makes the control not accurate. But for voltage-fed quasi-z-source matrix converter, the voltage gain can go to 4-5 times or even higher depending on the voltage rating of the switch. Although Z-source matrix converter has least amount of LC components, but it has limited voltage boost ratio, inherited phase shift caused by the Z-network, and also discontinuous current in the front of Z-source network. Quasi-Z-source matrix converter has higher boost ratio, no phase shift and lower switch voltage and current stress. In addition, the circuit in Figure 2.12(i) has continuous input current. In conclusion, voltage-fed quasi-Z-source matrix converter is a component less, compact, high efficient, wide range buck-boost matrix converter.

Pulse-width-modulation (PWM) control for traditional matrix converter has to be modified to utilize the shoot-through states for voltage boost. A extra shoot through reference needs to be designed to compare with carrier to generate extra shoot through signal. It can be inherited from the control methods for Z-source inverter [4, 32]. A simple maximum boost control is proposed which inherits the straight lines of the simple boost control; a maximum boost control is proposed which utilizes all available zero states. Maximum constant boost control utilizes maximum zero states in the precondition of keeping the shoot through duty ratio constant. From analysis, at voltage gain smaller than 0.866, no shoot through needs to

be applied, in order to preserve the minimum voltage and current stress on the devices. At voltage gain bigger than 0.866, maximum constant boost control can introduce much lower harmonics to the output because its time-invariant shoot through duty ratio.

This chapter explores control methods for the Z-source Matrix converter and their relationships between voltage gain, voltage/current stress and modulation index for each method. Simple maximum boost control, maximum boost control and maximum constant boost control have been proposed according to different shoot through reference. Different methods can achieve different voltage gain. At a certain voltage gain, different methods can lead to different switching loss, total harmonic distortion and voltage stress on the devices, which are considered as three criterions to estimate the performance of modulation method. The control method, relationships of voltage gain versus modulation index, and voltage stress versus voltage gain are analyzed in detail. A complete analysis and calculation for the three mentioned criterions are presented for different methods. Finally, an optimum hybrid control according to voltage gain range has been concluded to have the best performance under all three criterions. Simulation and experiment results are given to demonstrate the conclusion.

7.2 Quasi-SVPWM for Traditional Matrix converter

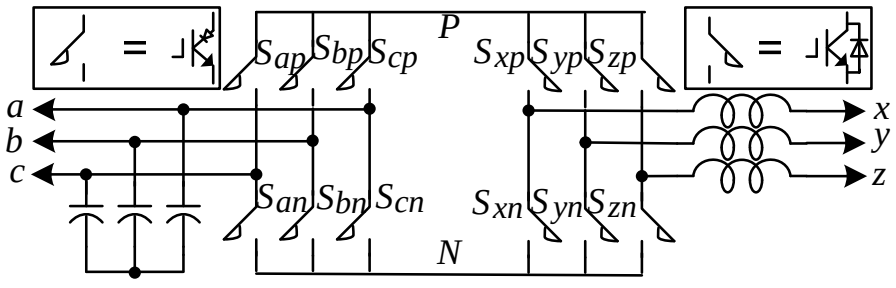


Figure 7.1. Equivalent circuit of direct matrix converter

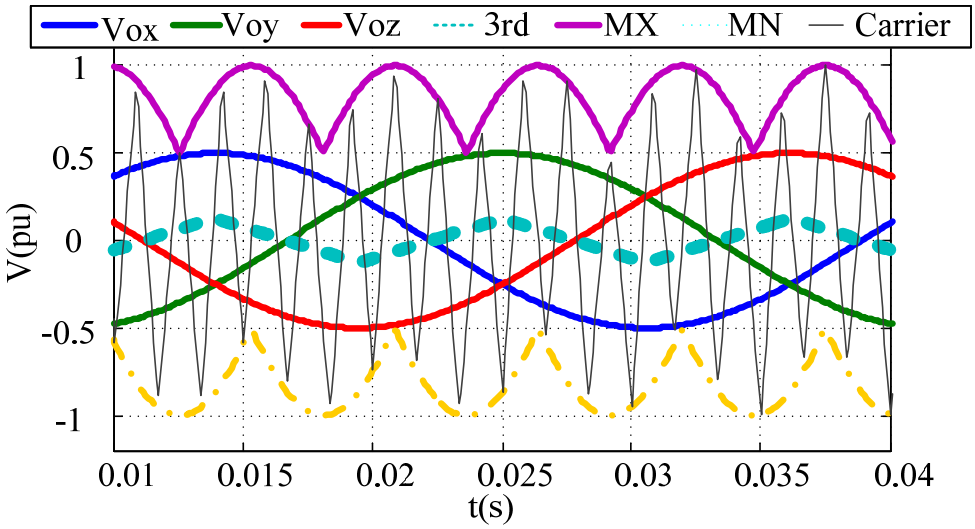


Figure 7.2. SVPWM modulation method for traditional matrix converter

In MC, the carrier waveform switches between variable positive and negative levels. The maximum envelope of the three input phase voltages MX and the minimum envelope MN can be considered as the positive level and negative level of the imaginary dc link voltage respectively, as shown in Figure 7.1. So each output phase voltage is switched between these two levels, as shown in Figure 7.2. In Figure 7.2, the input frequency is 60Hz and the output frequency is 30Hz. Assume the input phase voltage amplitude is equal to 1.

The switching state matrix of 9 switches can be obtained by multiplication of two switching matrix:

$$\begin{bmatrix} S_{ax} & S_{ay} & S_{az} \\ S_{bx} & S_{by} & S_{bz} \\ S_{cx} & S_{cy} & S_{cz} \end{bmatrix} = S_C S_V = \begin{bmatrix} S_{ap} & S_{an} \\ S_{bp} & S_{bn} \\ S_{cp} & S_{cn} \end{bmatrix} \begin{bmatrix} S_{xp} & S_{yp} & S_{zp} \\ S_{xn} & S_{yn} & S_{zn} \end{bmatrix} \tag{7.1}$$

S_C is obtained by making one of the upper switches on when its corresponding input phase voltage is the maximum among three, and making one of the lower switches on when its corresponding input phase voltage is the minimum among three. S_V is obtained by turning on the upper switch in one phase leg when its corresponding output reference voltage is

bigger than the MX, MN enveloped carrier voltage, as shown in Figure 7.2.

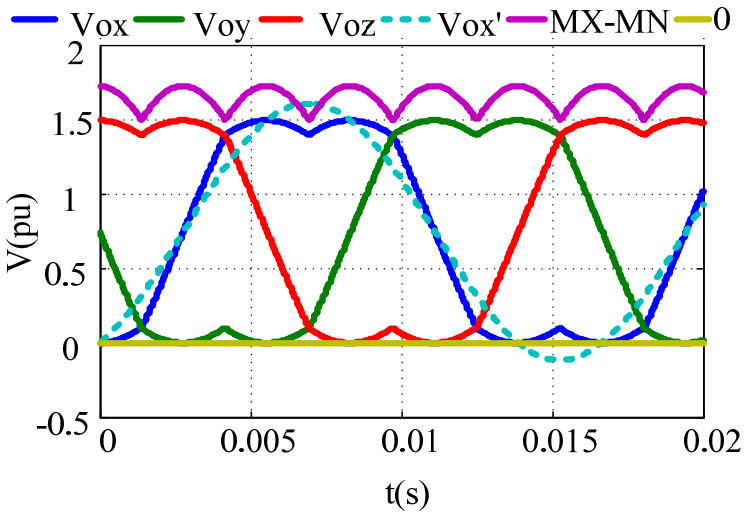


Figure 7.3. Third harmonic injection for traditional matrix converter

In order to bring the modulation index to 0.866, a third harmonic injection is utilized. In the previous method，the modulation index can not exceed 0.5. However, the maximum modulation index can increase to 0.866 by third harmonic injection. A triangle third-harmonic voltage is injected into the references as shown as dotted line in Figure 7.2, which is equivalent to space vector PWM method. Figure 7.3 shows the proposed third harmonic injection method. MX and MN in Figure 7.2 have been shifted to (MX-MN) and 0 respectively. The carrier waveform is enveloped by this (MX-MN). And the three phase output reference voltages cannot exceed carrier voltage at any time, thus it is contained in this envelope. By third harmonic injection, the reference voltages are shown as *Vox, Voy, Voz*,. The original reference before injection is shown as *Vox*'. The maximum modulation index can reach 0.866. The injected third harmonic expression is:

$$V_{oref\_3} = (\max(Vox^*, Voy^*, Voz^*) + \min(Vox^*, Voy^*, Voz^*))/2 \qquad (7.2)$$

Vox^*, Voy^*, Voz^* are the original sinusoidal three phase voltage references. This method is

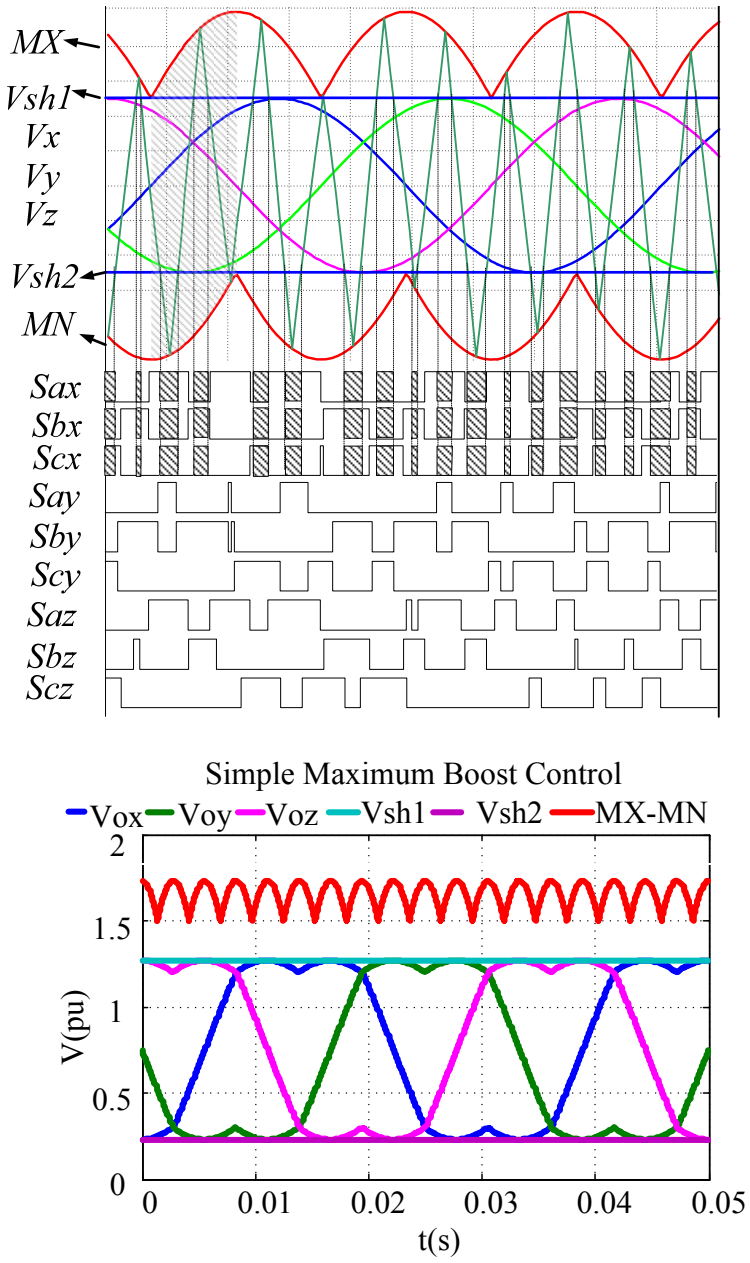
equivalent to the space vector modulation.

7.3. Simple boost, maximum boost, maximum constant boost shoot through control methods based on quasi-SVPWM

7.3.1. Principle of three control methods

The method of inserting the shoot through state by using carrier comparison is illustrated here. For ZS-MC, the principle of applying shoot through state is to replace some of the zero state of the converter by shoot through state, in order to not affect the output voltage. Thus the shoot through states should be within the normal zero states. The zero output voltage state in MC is corresponding to the switching state that all three output phases are connected to the same input phase. It happens when all three phase output voltages are either higher or lower than the carrier voltage. So the shoot through reference voltage should be either higher than the maximum reference voltage or lower than the minimum reference voltage.

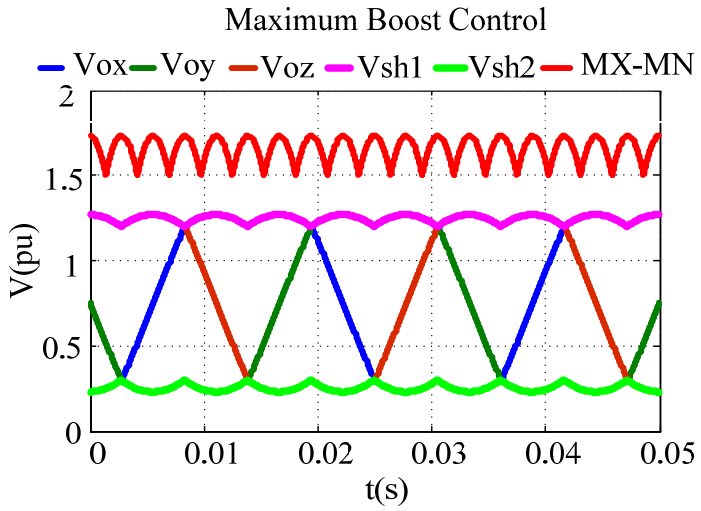
Three methods to insert shoot through state by applying different types of shoot through references are shown in Figure 7.4. Vsh1 represents the upper shoot through reference that to be compared with the carrier voltage enveloped by (MX-MN) and 0, and Vsh2 represents the lower shoot through reference. Simple maximum boost control uses a straight line as the reference to bond the upper envelope of output reference and the lower envelope. Maximum boost control utilizes all the zero state as the shoot through state, thus its shoot through reference is overlapped with the upper and lower output voltage envelope. Maximum constant boost control keeps the shoot through duty ratio constant at any moment, while reach maximum value.



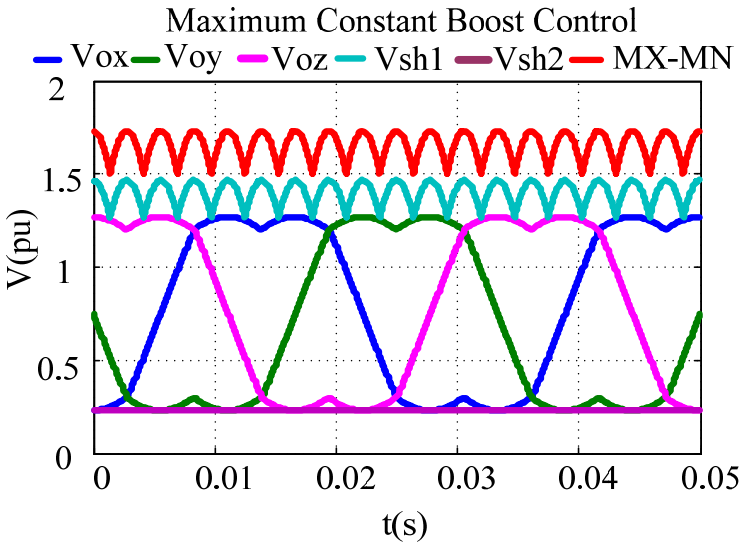
(a) Simple maximum boost control

Figure 7.4. Shoot through control for Z-source Matrix Converter (a) simple maximum boost control (b) maximum boost control (c) maximum constant boost

Figure 7.4 (cont'd)



(b) maximum boost control



(b) maximum constant boost control

7.3.2. Voltage gain and stress equations for each method

The shoot through duty cycle can be expressed as a function of modulation index, which can be used to derived the relationship between voltage gain and modulation index in order to guide the control parameter design. In each method, the shoot through duty cycle can be calculated according to the magnitude of the shoot through reference. It can be expressed as follows:

$$D_0(t) = \frac{(MX(t) - MN(t) - V_{sh1}(t)) + V_{sh2}(t)}{MX(t) - MN(t)} \tag{7.3}$$

Table 7-1.Shoot through reference and duty cycle

	Vsh1(t)	*Vsh2(t)*	*D0(t)*
Simple	*0.75+sqrt(3)*M/2*	*0.75-sqrt(3)*M/2*	*f(M,t)*
maximum	*max(Vox,y,z)*	*min(Vox,y,z)*	*f(M,fin,fo,t)*
max-constant	*(MX(t)-MN(t))*(1-D0(t))*	*0.75-sqrt(3)*M/2*	*5/4-5*sqrt(3)*M/6*

Thus the key value is the shoot through reference. Table 7-1 shows the shoot through references and duty cycle for each method. It can be found that duty cycle is constant only in maximum constant control. All the others are time-varied function. In order to derive voltage gain equation, the average shoot through duty cycle needs to be obtained.

The relationship between D_0 and M can be derived according to eq. (7.3) and table 7.1, for three methods. In simple maximum boost control, due to the symmetry, the average value of D_0 in one output reference voltage fundamental cycle is equal to the average value in 60 degrees wide area. Take $[\pi / 6, \pi / 2]$ as an example. There is $MX(t) = \sin(\omega_i t), MN(t) = \sin(\omega_i t - 2\pi / 3)$ during this period. So the average $D_0(t)$ is:

$$\overline{D_0(t)} = \int_{\frac{\pi}{6}/\omega_i}^{\frac{\pi}{2}/\omega_i} \frac{\sin(\omega_i t) - \sin(\omega_i t - \frac{2\pi}{3}) - \sqrt{3}M}{\sin(\omega_i t) - \sin(\omega_i t - \frac{2\pi}{3})} dt = 1 - \frac{2\pi}{3} M \tag{7.4}$$

In maximum boost control, the average D_0 is associated with input/output frequency, input/output angle, modulation index and time. Take the integration time equal to integer times of 1/3 of input fundamental period and also integer times of 1/3 of output fundamental period $t = m \cdot \frac{1}{3}\frac{2\pi}{\omega_i} = n \cdot \frac{1}{3}\frac{2\pi}{\omega_o}$, to do average as:

$$\overline{D_0(t)} = \frac{\int_0^t ((MX(t) - MN(t) - MXo(t) + MNo(t))dt}{\int_0^t (MX(t) - MN(t))dt} = 1 - M \qquad (7.5)$$

Similar process can be done for maximum constant boost control, as shown in Table 7-3.

7.3.3. The voltage gain comparison among three methods

The proposed three control methods plus the traditional non-shoot through control need to be evaluated and compared at different criterions. Voltage gain, output current harmonics, device stress and switching loss have been selected here as three main aspects for comparison. A case study has been completed for the comparison. The circuit parameters and control parameters used here is listed in Table 7-2

Table 7-2.Parameters used in the case study

Vm	fi	fo	Load Z	Z-source L	Z-source C	Power
100	60Hz	85Hz	4+j0.6	600uH(3.7%	200uF(2% pu)	2.5kW

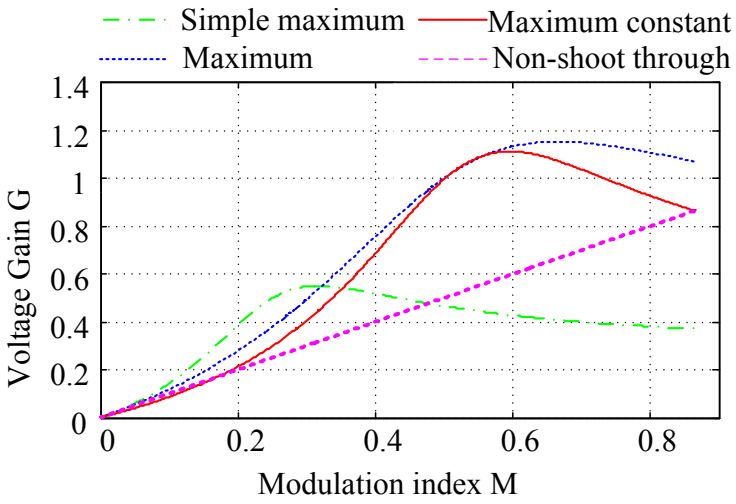


Figure 7.5. Voltage gain vs. modulation index for three methods

Table 7-3.Boost ratio and voltage gain of three methods

	Simple	*Maximum*	*Max-Constant*
D0	$1-\frac{2\pi}{3}M$	$1-M$	$\frac{5}{4}-\frac{5\sqrt{3}}{6}M$
B	$\frac{1}{\sqrt{\frac{4}{3}\pi^2M^2-2\pi M+1}}$	$\frac{1}{\sqrt{3M^2-3M+1}}$	$\frac{1}{\sqrt{\frac{25}{4}M^2-\frac{15\sqrt{3}}{4}M+\frac{31}{16}}}$
G	$\frac{M}{\sqrt{\frac{4}{3}\pi^2M^2-2\pi M+1}}$	$\frac{M}{\sqrt{3M^2-3M+1}}$	$\frac{M}{\sqrt{\frac{25}{4}M^2-\frac{15\sqrt{3}}{4}M+\frac{31}{16}}}$

Table 7-4.Maximum Gain of Each Method

	Simple	*Maximum*	*Max-Constant*	*Non-shoot*
Gmax	*0. 551*	*1.155*	*1.114*	*0.866*
M	*0.321*	*0.663*	*0.595*	*0.866*

For different method, the voltage gain at the same modulation index is different since the relationship between $D_0(t)$ and m is different, as shown in Table 7-3. Substituting Table--7-1 equation into boost ratio equation, the relationship between voltage boost ratio B and modulation index M can be obtained, as well as voltage gain from input to output. They are summarized and shown in Table 7-3. Figure 7.5 shows the plot of voltage gain vs. modulation index for three methods and the traditional non-shoot through control. The six crossing point of four curves are [0.323,0.551], [0.355, 0.548], [0.477,0.477], [0.519, 1.038], [0.564, 1.101], [0.866,0.866]. The maximum gains of each method are shown in Table 7-4.

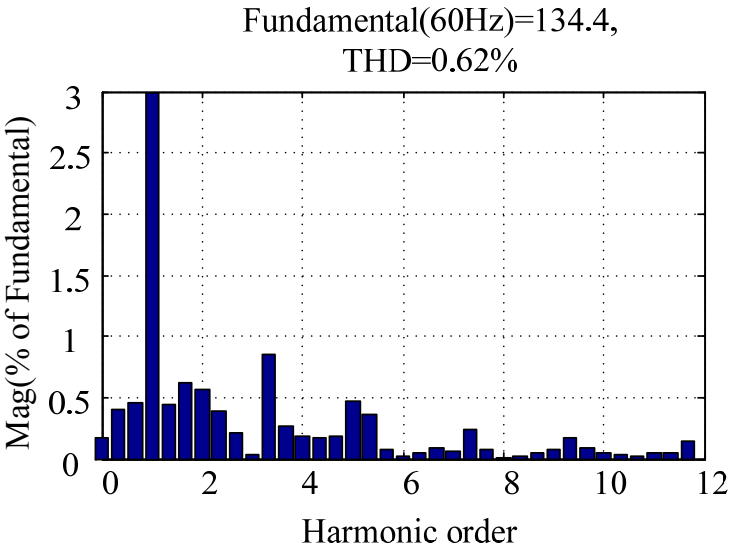
In conclusion, the simple maximum boost control can only be used in voltage gain below 0.55, maximum boost control has 1.155 gain, which is a little bit higher than maximum constant boost control.

7.3.4. THD comparison among three methods

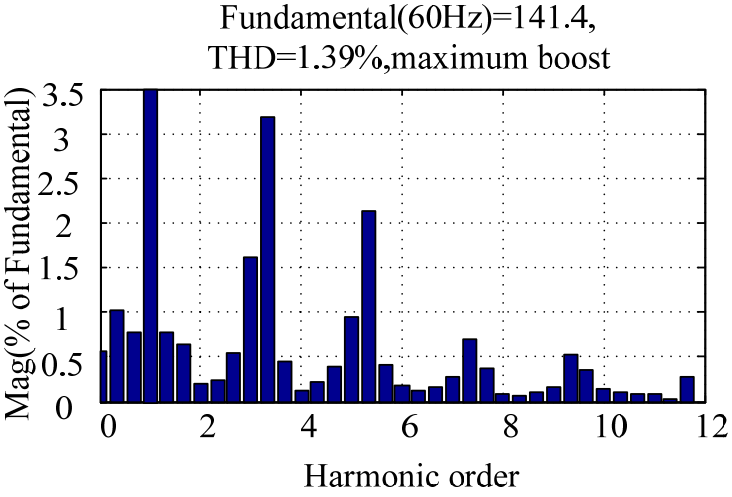
In Z-source matrix converter, the variation of shoot through duty cycle will affect the

output current harmonics. The reason is as follows. From equation (7.4) and (7.5), if $D_0(t)$ is time-variant function, the output voltage amplitude will be time-variant, thus the current will be distorted as well. In simple maximum boost control, $D_0(t)$ varies at six times of the input frequency as shown in Figure 7.4(a). Therefore the output current contains the harmonics at the same frequency. In maximum boost control, $D_0(t)$ is no longer periodic, but a function of input frequency, output frequency, input output phase angle difference, and time. So the output harmonics contains harmonics at all those frequencies. In order to verify this analysis, a FFT spectrum analysis is conducted based on the parameters set in Table 7-2. The output line to line voltage across the resistive load has been taken as the target because it has the same information as the line current. Figure 7.6 shows the spectrum of output line voltage in each method. The fundamental frequency is equal to output frequency 85Hz. It can be seen that maximum boost control has the highest THD and maximum constant boost has the lowest. Different methods possess different harmonic characteristics. Simple maximum boost and maximum boost have similar harmonic distribution but different magnitude.

In addition, THD is affected by the variation of the D_{op}. In simple boost control, D_{op} is a periodic function with $1/6$ input frequency. It mainly contains DC offset and 6ω harmonics. In maximum boost control, D_{op} is a function of time, output frequency and phase shift between input and output $D_0(t) = f(M, t, \theta)$ because of the arbitrary output frequency. So the output voltage/current contains not only 6ω but multiple frequency harmonics, which is difficult to be filtered out. However, in maximum constant boost control, D_{op} is a constant value, which eliminates all low order output harmonics. The comparison will be



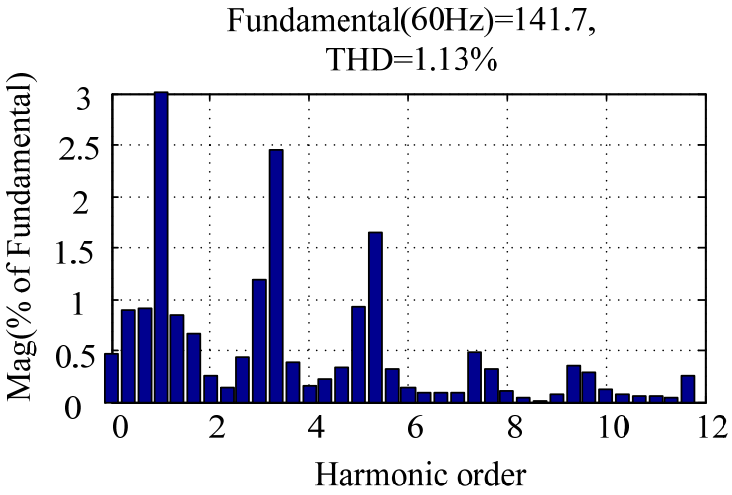
(a) Spectrum of maximum constant boost control



(b) Spectrum of maximum boost control

Figure 7.6. Spectrum of different methods at $f_o = 80Hz$

Figure 7.6 (cont'd)



(c) Spectrum of simple maximum boost control

shown later.

Maximum constant boost control possess the following advantages than the other methods: (1) no low-order output current harmonics (2) low input current spike (lower input current value) (3) low input and output line voltage spike (lower input and output voltage value) (4) low switch voltage and current stress (5) high power factor. In conclusion, maximum constant boost control presents better control characteristics in terms of switch voltage stress and the output harmonics than other methods.

7.3.5. Switching loss comparison among three methods

A 600V/200A 18-switch RB-IGBT module has been used here, in order to improve the efficiency. The switching loss can be estimated by the instantaneous voltage V_{sw} and current I_{sw} on the device. In each switching time interval, there is one and only one switch is conducting in one phase leg. So when this switch is open, its voltage V_{sw} is equal to the input line to line voltage. If this switch is on, it provides the only path for the output phase current, thus the switching current I_{sw} is equal to the output current. In one fundamental period, the

three switches on the same column should have several commutations according to the control strategy. Therefore, V_{sw} is a pulse type voltage enveloped by two sinusoidal input line to line voltages; I_{sw} is a pulse type current enveloped by output current. Since the amplitude and shape of V_{sw} is closed to input line to line voltage envelope and the shape of V_{sw} is closed to output line current, the input PWM line voltage and the output line current can be used as the switching voltage and current envelope to calculate the approximate switching loss.

The general equation for switching loss calculation is:

$$P_{sw} = \frac{1}{2}\frac{|V_{sw}||I_{sw}|}{V_{ref} I_{ref}}(E_{on} + E_{off} + E_{rr})\, f_{sw} \tag{7.6}$$

It needs to be noted here that the switching loss caused by shoot through is not considered because that part of loss has small difference among different methods. Assume $V_{sw} = V_m' \sin(\omega_i t)$ *and* $I_{sw} = I_{om}' \sin(\omega_o t + \theta)$, where V_m' represents amplitude of $V_{a'b'}$ and I_{om}' represents amplitude of I_{ox}; ω_i and ω_o represents the input and output frequency respectively. The maximum switching loss would happen when power factor is 1. The parameters in this case study is set to be: $V_m = 100V, Z_L = 4 + j0.6$.

Because of the voltage gain limit of simple maximum boost control, this method is not considered here. The efficiency comparison among maximum constant boost control, maximum boost control and non-shoot through control is conducted when an equal voltage gain is obtained by all of them. The switching voltage and current at a certain voltage gain can be expressed as:

$$V_m' = B * V_m \tag{7.7}$$

$$I_{om} = \frac{G * V_m / \sqrt{3}}{|Z_L|} \tag{7.8}$$

The average $|V_{sw}||I_{sw}|$ can be derived by:

$$\overline{|V_{sw}||I_{sw}|} = \int_0^T |V_{sw}||I_{sw}| / T \tag{7.9}$$

, where $T = m \cdot T_i = nT_o$; T_i, T_o are input and output switching periods; m and n are integers.

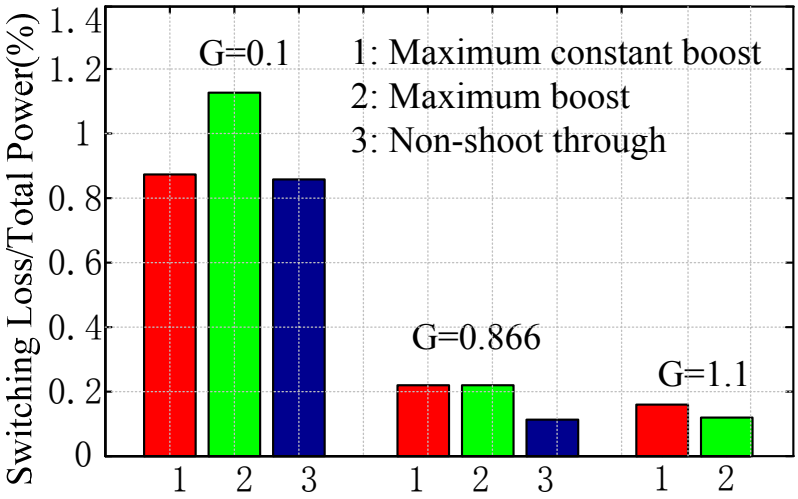


Figure 7.7. Switching loss comparison at different G

Figure 7.7 shows the switching loss comparison among the three methods at G=0.1, G=0.866 and G=1.1. It can be seen that at G<0.866, non-shoot through method has the highest efficiency, and at G>0.866, maximum constant boost and maximum boost have similar efficiency, which coincides with the voltage stress analysis.

The conclusion is non-shoot through control would achieve minimum switching loss at voltage gain G<0.866; and above that, maximum constant boost control and maximum boost control can either be selected to achieve minimum switching loss.

7.4. Maximum Voltage Gain Control

In ZS-MC, the boost factor B is not a monofonic function of D_0 like the traditional Z-source inverter, thus the maximum voltage gain is not necessarily achieved at maximum

available D_0. In ZS-MC, voltage gain is the function of M and D_0, as shown in Table 7-3, with the restriction that $\overline{D_0(t)} \le 1-M$, in which the equal sign can only be obtained at maximum boost control.

To get the maximum G, assume that $\overline{D_0(t)} = 1-k\cdot M \quad (k \ge 1)$, thus:

$$G = MB = \frac{M}{\sqrt{3M^2[(k-\frac{1}{2M})^2 + \frac{1}{12M^2}]}} \tag{7.10}$$

The maximum G happens at $k = \frac{1}{2M}$, which leads $\overline{D_0(t)} = 0.5$. Considering the restriction $\overline{D_0(t)} \le 1-M$, when M>0.5, $\overline{D_0(t)}$ should be the maximum available $\overline{D_0(t)}$, which is *1-M*, because *B* is a monotone increasing function at $D_0 \in [0, 0.5]$; thus the control strategy is identical to maximum boost control. When M<0.5, $\overline{D_0(t)}$ should be equal to 0.5. So the maximum gain control law is:

$$\begin{cases} \overline{D_0(t)} = 0.5 & (M \le 0.5) \\ \overline{D_0(t)} = 1-M & (M > 0.5) \end{cases} \tag{7.11}$$

And the voltage gain G_g equations are:

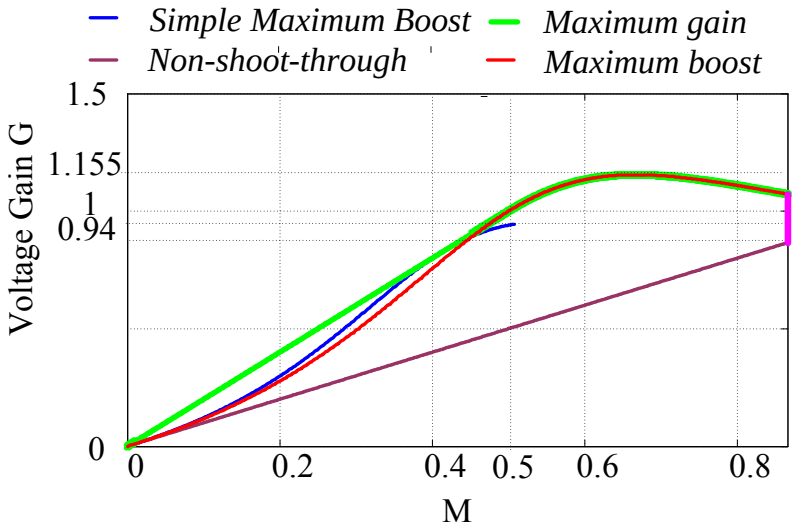


Figure 7.8. Maximum voltage gain vs. M

$$\begin{cases} G_g = 2M & (M \le 0.5) \\ G_g = \dfrac{M}{\sqrt{3M^2 - 3M + 1}} & (M > 0.5) \end{cases} \tag{7.12}$$

As shown in the green line in **Error! Reference source not found.**7.8.

To implement the constant D_0 at M<0.5, the shoot through reference curve has to be located between *MX* and *MXo*, or between *MNo* and *MN*, while keeping $\overline{D_0(t)}$=0.5. Assume the upper and lower reference curves for maximum gain control at M<0.5 is V_{sh1} and V_{sh2}, thus:

$$\overline{D_0(t)} = 1 - (\frac{\overline{V_{sh1}(t) - V_{sh2}(t)}}{MX(t) - MN(t)}) = 0.5 \tag{7.13}$$

Similar to the maximum boost control case, one choice of the two curves are *MXo* and *MNo* at a constant M=0.5.

In summary, the V_{sh1}, V_{sh2} equations for maximum gain control are:

$$\begin{aligned} V_{sh1} &= Max(V_{xo}, V_{yo}, V_{zo}) \quad (V_{x,y,zo} = 0.5\sin(\omega_0 t + \alpha + \cdots)\ (M \le 0.5)) \\ V_{sh2} &= Min(V_{xo}, V_{yo}, V_{zo}) \quad (V_{x,y,zo} = M\sin(\omega_0 t + \alpha + \cdots)\ (0.5 < M < 0.866)) \end{aligned} \tag{7.14}$$

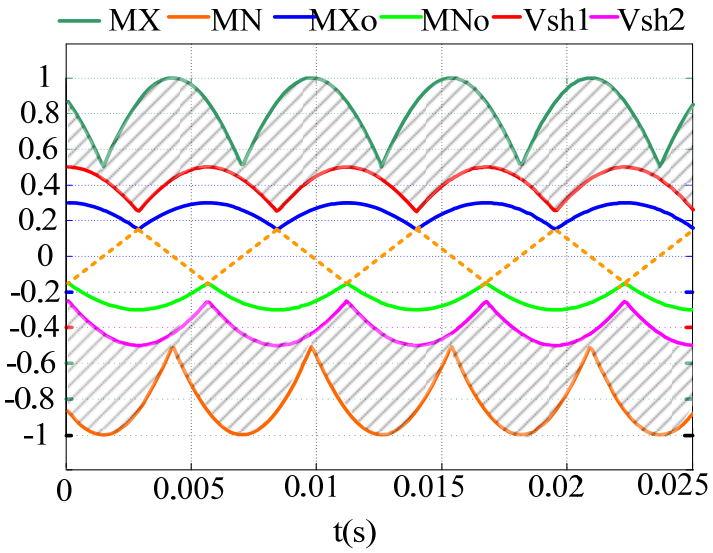


Figure 7.9. Shoot through references to generate $\overline{D_0(t)} = 0.5$

They are compared with the triangle to generate the shoot through PWM, as shown in **Error!**

Reference source not found.7.9. the red line is reference curve at M<0.5. The shadow part is the available shoot through area.

7.5. Hybrid minimum voltage stress control

At a given target voltage gain, one criterion to select the control strategy is to minimize the voltage stress on the switch. Take voltage-fed Z-source matrix converter in Figure 2.12 (f) as an example. The voltage stress in ZS-MC is equal to *B* times the input line to line voltage. B is illustrated in Table 7-3. Different from traditional Z-source inverter, B here is not a monotonic function of D_0 thus the minimum voltage stress is not necessarily achieved at maximum available D_0.

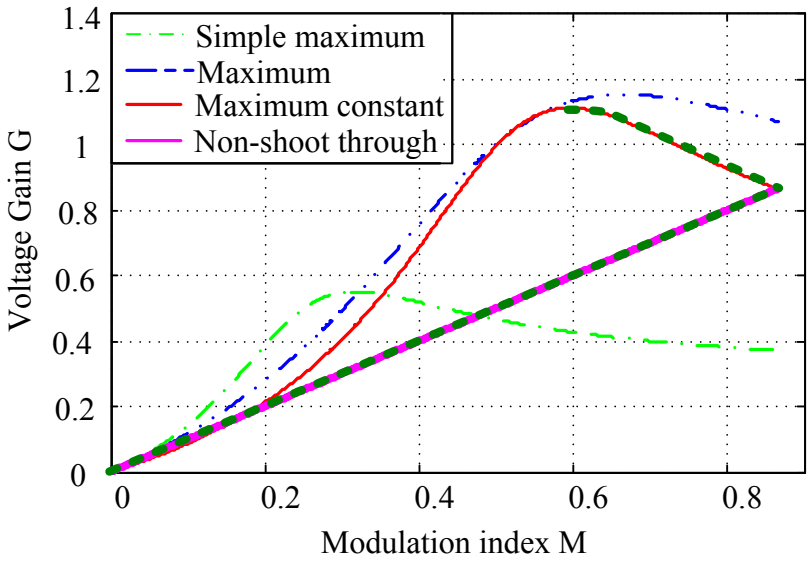


Figure 7.10. Control strategy selection at different gain ratio for ZS-MC

From equation "$G = MB$", to minimize voltage stress ratio B for a defined G, M is required to be the biggest available M.

From the G-M curves in Figure 7.10 for four control strategies, different control strategy can be selected during different voltage gain range to obtain the maximum modulation index. The dash symbols show the selection of different curves in different sections. The executive

law of this kind of hybrid control is illustrated in Table 7-5 according to the cross points of the four G-M curves. By following this hybrid control curve, minimum voltage and current stress on the device can be achieved.

Table 7-5.Control strategy for different G

Control strategy	Range of G
Non-shoot-through	$G \in [0, 0.866]$
Maximum constant boost	$G \in [0.866, 1.114]$
Maximum Boost	$G \in [1.114, 1.155]$

In the third range, only maximum boost can be utilized even it has higher harmonics because only this method can achieve high voltage gain. *G=f(M)* function becomes a quadratic function of which the maximum M is obtained in the section of $M \in [0.667,\ 0.866]$ at the same voltage gain.

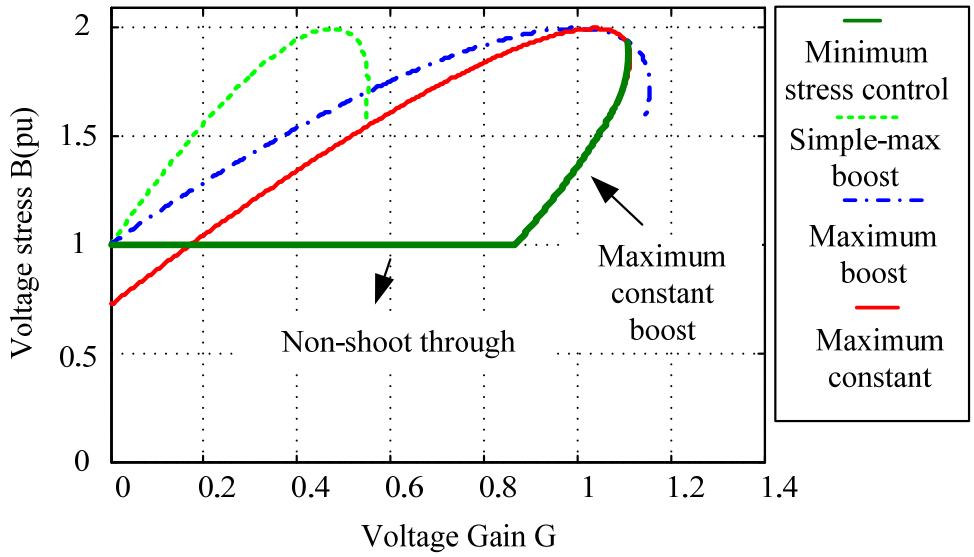


Figure 7.11. Voltage stress at different voltage gain of hybrid control

From equations in Table 7-3, the voltage stresses across the devices with different control strategies are shown in Figure 7.11. As can be seen, the hybrid minimum stress

control has the smallest voltage stress at the whole voltage gain range.

In conclusion, for minimum stress purpose, traditional non-shoot through control is selected when voltage gain G<0.866; maximum constant boost control is selected when voltage gain is within [0.866, 1.114]; maximum boost control is selected when voltage gain is within [1.114, 1.155], in order to achieve minimum voltage stress on the device in the whole voltage gain range.

7.6. PWAM Control Method for Matrix Converter

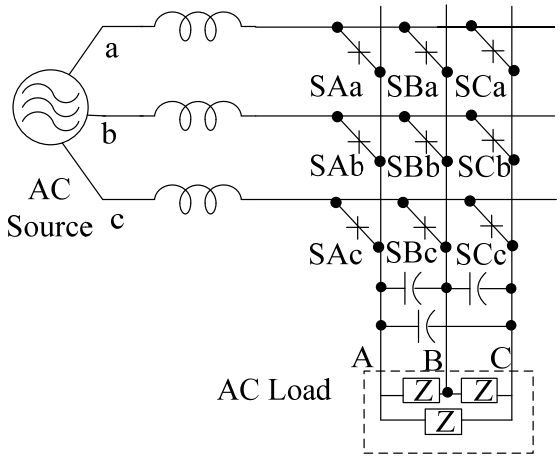


Figure 7.12. Nine switch direct matrix converter

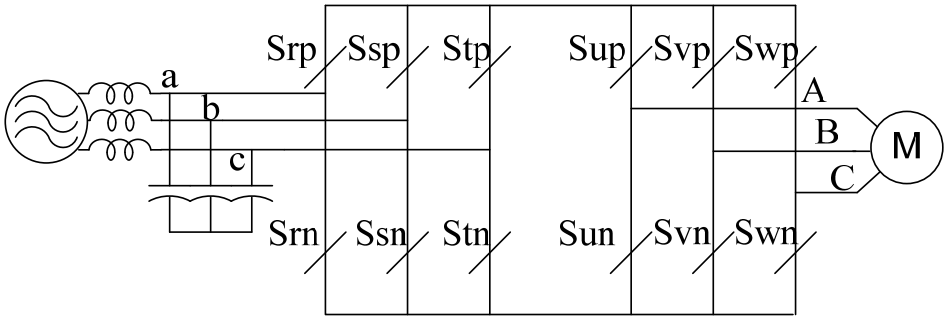


Figure 7.13. Equivalent decomposed circuit for nine switch direct matrix converter

The 9 switch matrix converter can be equivalent to a series connection of a six switch rectifier and a six switch inverter, as shown in Figure 7.12. The dc link is an imaginary dc

link. This equivalence happens when two groups of switching functions have the following relationship:

$$\begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix} = \begin{bmatrix} S_{up} & S_{un} \\ S_{vp} & S_{vn} \\ S_{wp} & S_{wn} \end{bmatrix} \begin{bmatrix} S_{rp} & S_{rn} \\ S_{sp} & S_{sn} \\ S_{tp} & S_{tn} \end{bmatrix}^{T} \tag{7.15}$$

This equation is derived by utilizing the concept: If same switching function is obtained from different topologies, the waveform will be exactly the same.

Since in nine switch matrix converter, the relationship between input and output is:

$$\begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{7.16}$$

In equivalent circuit, the relationship between input and output can be derived through the middle imaginary dc link:

$$\begin{bmatrix} v_{An} \\ v_{Bn} \\ v_{Cn} \end{bmatrix} = \begin{bmatrix} S_{up} & S_{un} \\ S_{vp} & S_{vn} \\ S_{wp} & S_{wn} \end{bmatrix} \begin{bmatrix} V_{DC}^{+} \\ V_{DC}^{-} \end{bmatrix} = \begin{bmatrix} S_{up} & S_{un} \\ S_{vp} & S_{vn} \\ S_{wp} & S_{wn} \end{bmatrix} \begin{bmatrix} S_{rp} & S_{rn} \\ S_{sp} & S_{sn} \\ S_{tp} & S_{tn} \end{bmatrix}^{T} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{7.17}$$

If the equivalence concept is applied into these two topologies, (7.26) can be derived.

The space vector PWM control if used for modulation of direct matrix converter, this equivalent circuit also will be utilized. In Figure 7.13, the left side can be considered as a current source inverter, and the right hand side is a voltage source inverter. The current source inverter SVPWM takes dc link current as reference, including six active vectors and three zero vectors. Its equation and control diagram are as follows:

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} S_{rp} & S_{rn} \\ S_{sp} & S_{sn} \\ S_{tp} & S_{tn} \end{bmatrix} \begin{bmatrix} I_{DC}^{+} \\ I_{DC}^{-} \end{bmatrix} \tag{7.18}$$

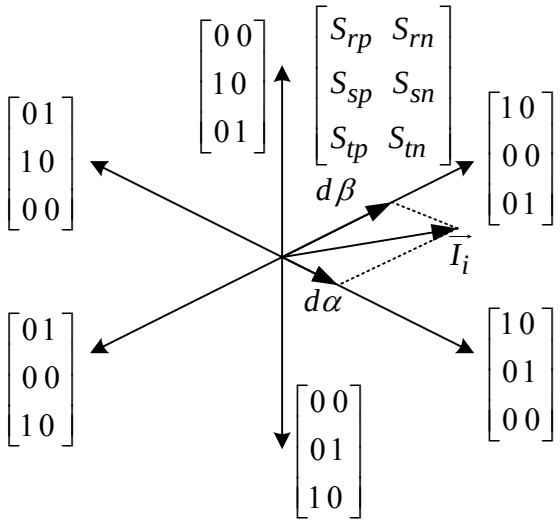


Figure 7.14. Current source inverter space vector modulation diagram

The synthesis equation for input current vector is:

$$\overrightarrow{I_i} = d\alpha \cdot \overrightarrow{I_1} + d\beta \cdot \overrightarrow{I_2} \tag{7.19}$$

As shown in Figure 7.14, the switching state for $\overrightarrow{I_1}$ is $\begin{bmatrix} 1\,0 \\ 0\,1 \\ 0\,0 \end{bmatrix}$ and the switching state for $\overrightarrow{I_2}$ is $\begin{bmatrix} 1\,0 \\ 0\,0 \\ 0\,1 \end{bmatrix}$. $d\alpha \cdot T_s$ is the pulse width for vector 1 and $d\beta \cdot T_s$ is for vector 2.

The dc current can have lots of choices. For example, the envelope of the maximum line current is one of them. According to the power balance, the dc link voltage waveform is the inverse of the current.

The output voltage equation and SVPWM diagram are as follows:

$$\begin{bmatrix} v_{An} \\ v_{Bn} \\ v_{Cn} \end{bmatrix} = \begin{bmatrix} S_{up} & S_{un} \\ S_{vp} & S_{vn} \\ S_{wp} & S_{wn} \end{bmatrix} \begin{bmatrix} V_{DC}^{+} \\ V_{DC}^{-} \end{bmatrix} \tag{7.20}$$

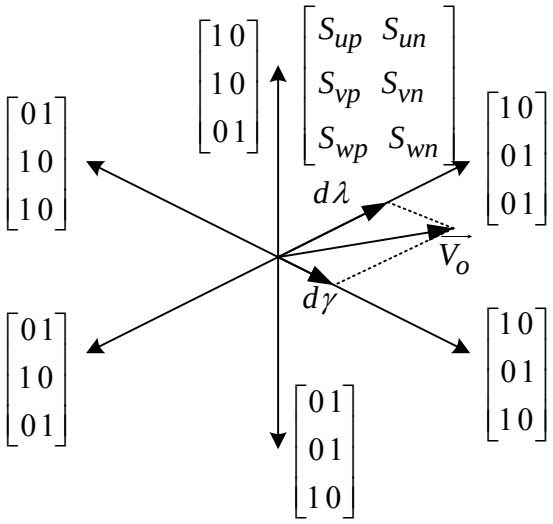
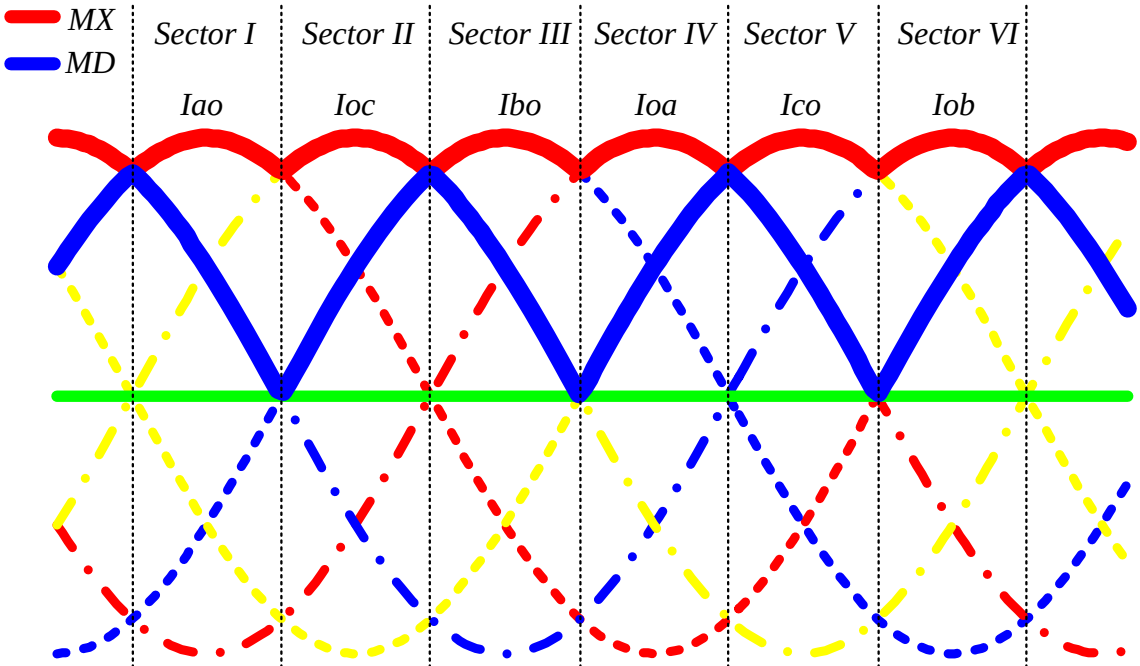


Figure 7.15. Voltage source inverter space vector modulation diagram

The output voltage synthesis process is similar to input current synthesis.

The zero vector period calculation is different from the traditional matrix converter because there are two extra states: the open zero state in input current source inverter and the shoot through zero state in output voltage source inverter. The traditional zero state periods thus can be calculated as:

$$\begin{aligned} t0 &= 1 - t1 - t2 - t_{op} \\ t0 &= 1 - t1 - t2 - t_{sh} \end{aligned} \tag{7.21}$$



Sap	*	1	*	0	0	0
Sbp	0	0	*	1	*	0
Scp	*	0	0	0	*	1
San	0	0	0	*	1	*
Sbn	1	*	0	0	0	*
Scn	0	*	1	*	0	0

* : Switching between 0 and 1

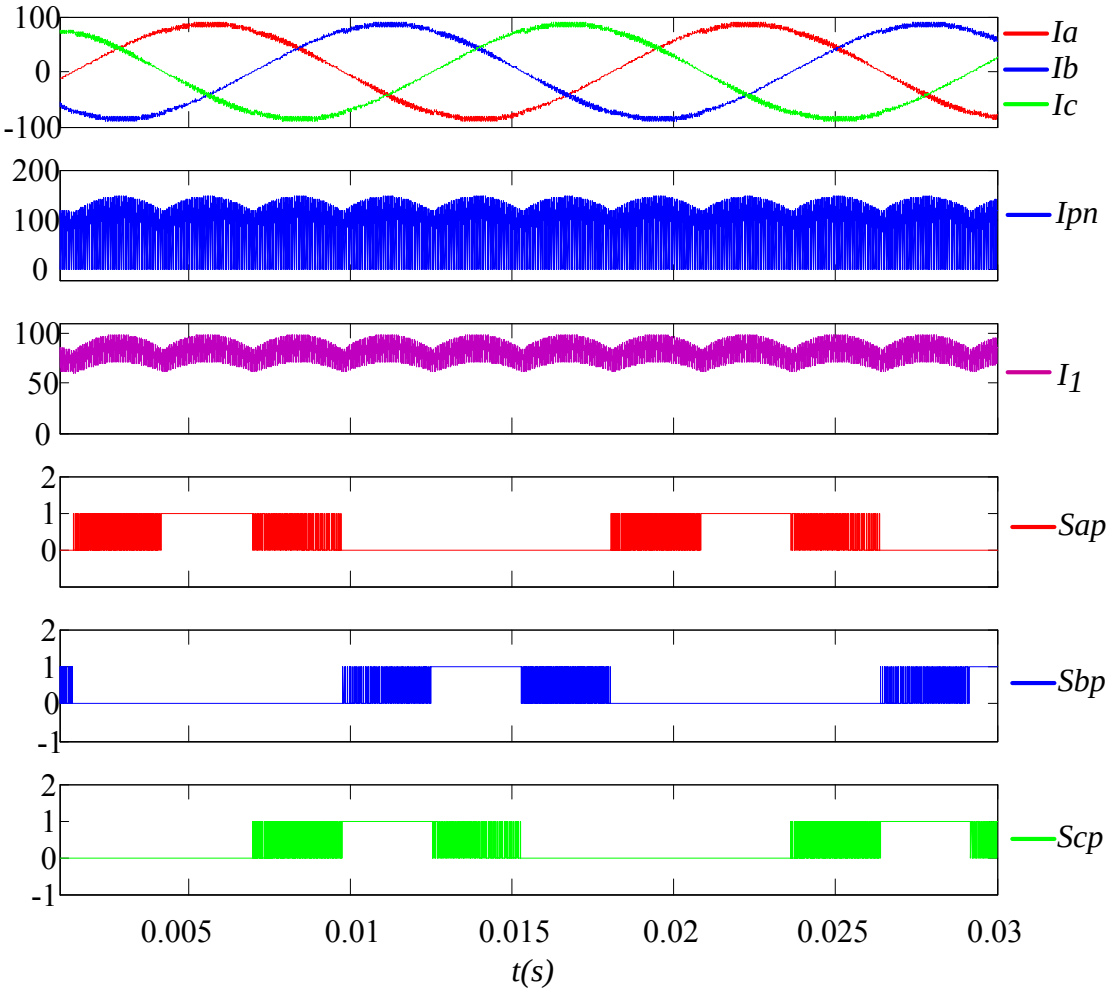
MX: Maximum line current envelope, also the average DC link current Ipn

MD: Medium line current, also the PWM reference

(a)

Figure 7.16. PWAM control (a) DC current waveform and switching pattern in different sections (b) Simulated output current, dc current and switching state

Figure 7.16 (cont'd)



(b)

Figure 7.16. PWAM control (a) DC current waveform and switching pattern in different sections (b) Simulated output current, dc current and switching state

PWAM method proposed in paper [7] can be used here to control either rectifier or inverter, in order to reduce the switching loss and frequency. For example, if PWAM method is used for current source inverter, the control diagram is shown in Figure 7.16(a). DC link current will be the maximum envelope of three phase current, which is a 6ω ripple current. The switching state changes according to which current takes up the maximum envelope. The total switching time will be reduced by 1/3 compared to SVPWM method, as shown in Figure

7.16 (b). If the voltage source inverter utilizes this modulation method, the switching loss can be reduced by 87.6% because the switching current is within [-60^0, 60^0], which is the smallest switching current portion in one cycle. Matrix converter can be considered as a rectifier in series with an inverter with no dc link capacitor. Thus the dc link current or voltage has more plasticity. Two control methods are proposed based on PWAM strategy, to achieve smaller switching loss, as shown in Figure 7.16 (a) and (b).

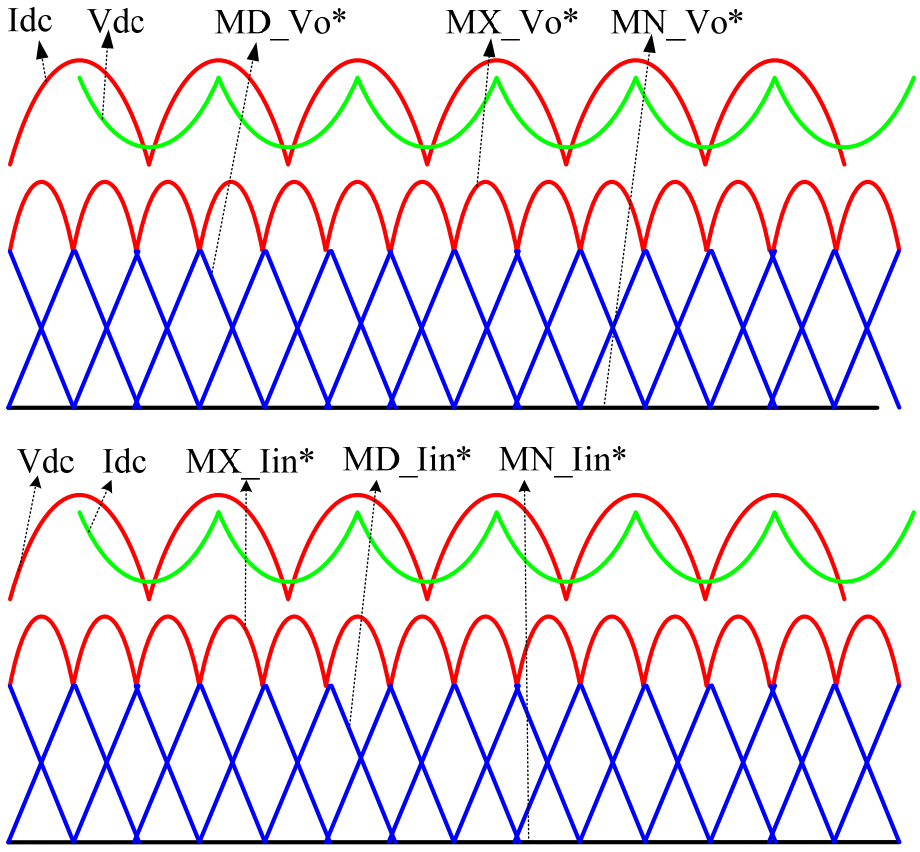


Figure 7.17. PWAM control +PWM control for low switching loss MC: (a) method 1: PWAM rectifier + PWM inverter (b) method 2: PWM rectifier +PWAM inverter

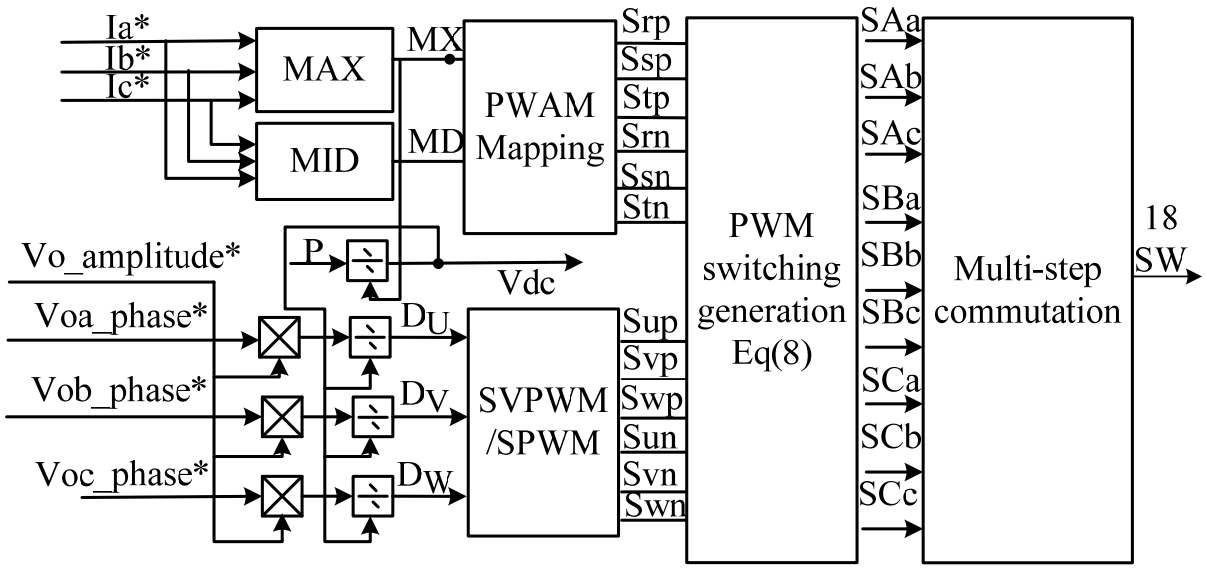


Figure 7.18. PWAM control + PWM control for low switching loss MC

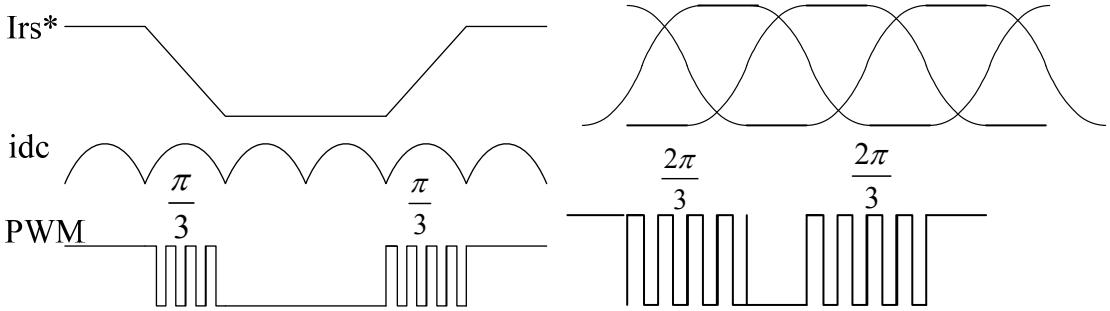


Figure 7.19. (a) switching waveform for current source inverter (b) switching waveform for voltage source inverter

The detailed control block diagram is shown in Figure 7.18. In this method, both input current and output voltage are controlled with desired waveform and power factor. The CSR bridge power loss can be reduced by 1/3 in unity power factor compared to SVPWM. The efficiency is greatly improved when the input current varies in a large range because the dc link current is regulated according to the input current reference.

Method 2 is to assign Vdc according to the output voltage command, as shown in Figure 7.17 (b). In this method, both input current and output voltage are controlled with desired waveform and power factor. The inverter bridge power loss can be reduced by 86% in unity

power factor compared to SPWM. The efficiency is greatly improved when the output voltage varies in a large range (since the dc link voltage is changed with the output voltage).

As shown in Figure 7.17(b), the switching only happens in 1/3 switching cycle, thus compared to 1/2 switching cycle in SVPWM, PWAM can reduce the switching frequency by 1/3, thus the switching loss by more than 1/2; compared to SPWM, PWAM can reduce the switching loss by 87% since all its switching are at small current region.

Since *Idc* becomes zero when shoot through state happens, when this PWAM method is transplanted to quasi-Z-source matrix converter, *Idc* is a pulse type PWM, but its maximum envelope is still the maximum envelope of the six line to line current, which happens in active state, as shown in Figure 7.16 (a) and (b). Thus the active switching state remains the same just part of the zero state has been transported into shoot through state. Figure 7.16 (b) shows the simulation result of the dc link current Ipn and also the maximum envelope of input three phase current.

7.7. CSR and VSI coordination

Two CSR commutation happens during zero state of VSI. Zero dc link current is obtained during zero state of VSI. The first method is shown in Figure 7.20 (a). Its VSI carrier rising and falling rate depends on the width of the CSR PWM. The advantages of this method include (1) CSR commutates with zero current, which eliminates the switching losses; (2) no need for overlap between switches. The disadvantages of this method include: (1) unsymmetric carrier waveform (2) variable zero voltage vector.

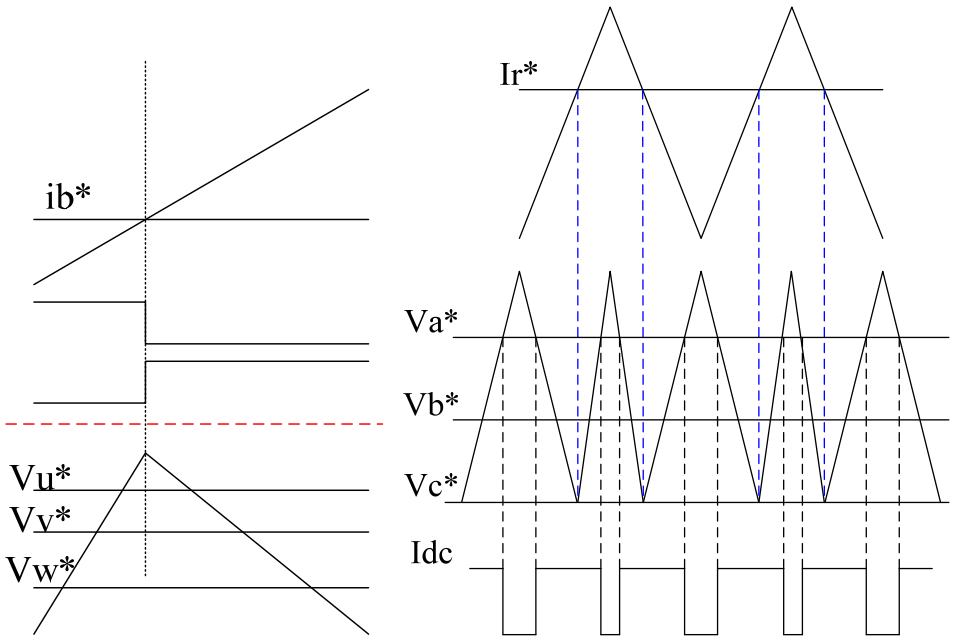


Figure 7.20 (a) Coordination method 1 (b) coordination method 2

The second method is shown in Figure 7.20(b). The principle is to make zero vector of VSI happen when Idc is zero. Thus the zero current period is controlled by the carrier of VSI. The benefit of this method is that it has constant zero vector duty cycle. The switching frequency of VSI is 2 times of switching frequency of CSR.

7.8. New commutation and protection strategy

For the nine switch direct matrix converter switching functions, two constrains have to be satisfied in order not to cause the short circuit of input voltage or open circuit for output current: one is the switches on the same output phase leg need to have deadtime; the other is the switches on the same output phase leg need to have overlap. These two seems contradictory with each other. However, the four step commutation for the two bidirectional switches on different input phases can implement this. The four step commutation can take source voltage as criterion or

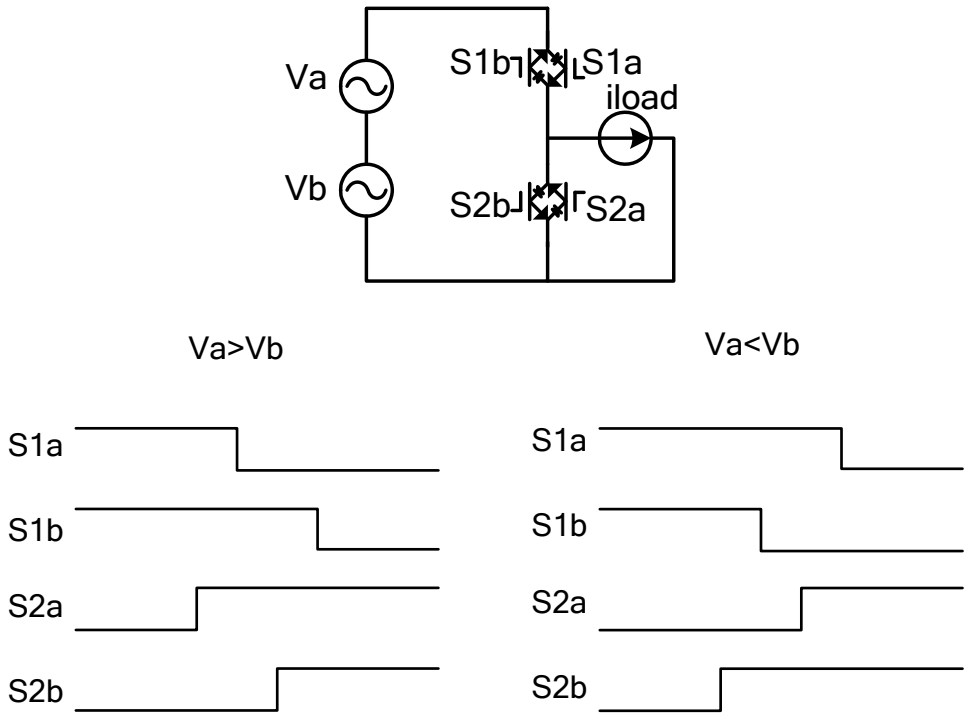


Figure 7.21. Voltage-based four step commutation

load current as criterion.

Figure 7.21 shows the equivalent circuit in four step commutation and also the voltage based commutation method. The current will change from phase a to phase b, so S_{1a}, S_{1b} need to be turned off and S_{2a}, S_{2b} need to be turned on. If load current is flowing out of the terminal, if S_{1a} needs to be turned off, S_{2a} has to be turned on first to provide a path for the load current. Thus S_{2a} is turned on first. This also avoid the short circuit because when $v_a > v_b$, it is impossible for S_{2a} and S_{1b} to form short circuit, so they can have overlap. After that, S_{2b} needs to be turned on before turning off S_{1b}, in order to provide a path for current. The short circuit through S_{1a} and S_{2b} doesn't exist because they have deadtime. Similar analysis can be given when $v_a < v_b$. These two cases have different switching sequence. Thus the problem comes out at the zero line to line voltage. Due to the sensor delay or inaccuracy, the following case can happen: the actual voltage still maintains

$v_a > v_b$, but the measurement already becomes $v_a < v_b$, thus the switching sequence already becomes $v_a < v_b$. As shown in Figure 7.21, in this condition, the overlap of S_{1a} and S_{2b} forms a short circuit between phase a and phase b, and also the deadtime between S_{2a} and S_{1b} forms an open circuit for output phase A current. These two will cause high current spike and high voltage spike in the devices.

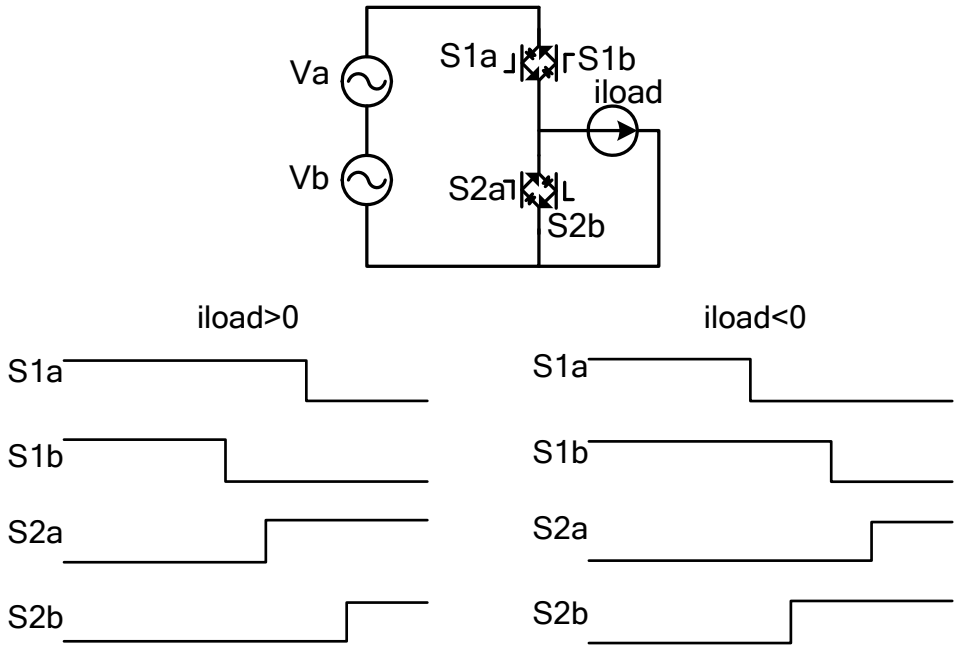


Figure 7.22. Traditional load current based four step commutation method

The output load current can also be taken as the criterion to do the commutation, as shown in Figure 7.22. When iload>0, S_{1b} and S_{2a} can not have overlap; S_{1a} and S_{2b} can not have overlap; but S_{1a} and S_{2a} needs to have overlap, as well as S_{1b} and S_{2b}. The similar process happens when iload<0. The disadvantage of this commutation method is that failure will happen when the load current crosses zero. For example, when the actual iload is smaller than zero, but the measured iload is still bigger than zero, the sequence will be judged by the measured iload. So the overlap between input two phases and open circuit in one output phase will happen, to cause high voltage and current spike on the device.

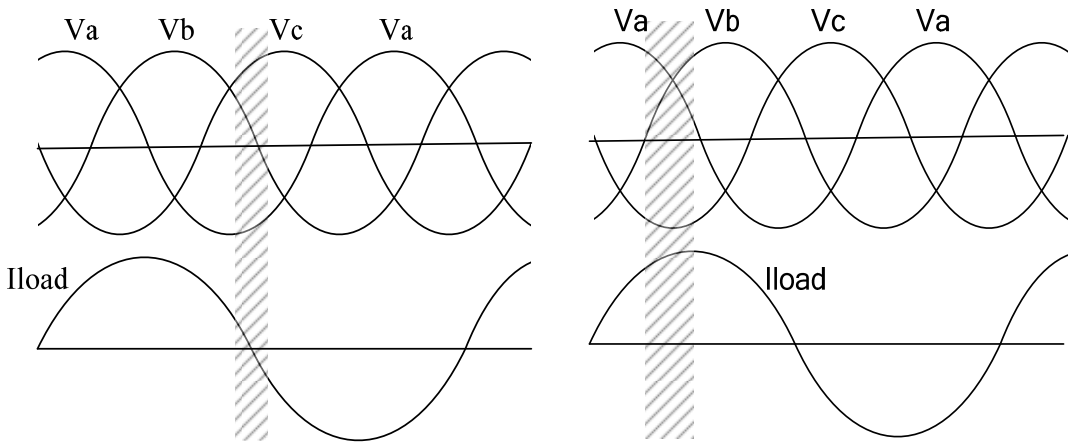


Figure 7.23. Combined commutation method (a) current-based master voltage-based slave (b) voltage-based slave current based slave

To be concluded, for voltage based commutation, the failure will happen in the zero line voltage point, due to the misdetection of the line voltage polarity; this can be caused by the detection delay and sensor offset, and it will cause the short circuit of input voltage sources. For current based commutation, the failure will happen in the zero line current point, which will cause the open circuit of the output. In order to solve this problem, the voltage and current based method can be combined to be alternately used, as shown in Figure 7.23. When the output current is small, voltage-based commutation can be used, but current-based method will also be used when the line voltage approaches zero. Similarly, when the input voltage is small, current based method will be the master and voltage based will be the slave method when line current approaches zero.

7.9. Protection strategy

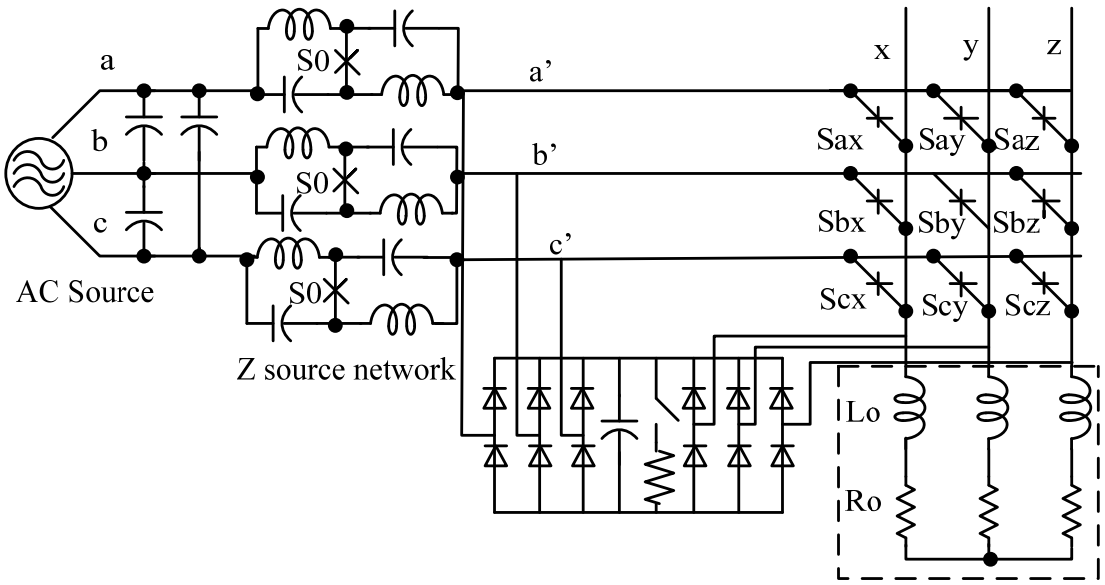


Figure 7.24. Improved protection method for voltage-fed quasi-Z-source inverter

Since the commutation failure still may happen in every utility cycle, the protection for the output open circuit is very important [8-9]. The conventional protection double rectifier method [8] can not be directly used in z-source matrix converter because the condition that input voltage is higher than the output no longer exists. The proposed method inherits the double rectifier circuit, but moves the input connection to the other side of the z-source network, as shown in Figure 7.24. The voltage at a', b',c' is a PWM voltage with boosted voltage envelope. Because the shoot through happens at the same time for the nine switches, the three line to line voltage at a'b'c' reach zero level at the same time in each switching period. Thus the diode bridge capacitor voltage will be clamped at the maximum envelope of the PWM type voltage, which is higher than the output voltage. So in normal condition, the right hand side diode bridge will not work. However, when output open circuit fault happens, the high spike voltage in the output will be clamped at the capacitor voltage, the diode bridge provides a path for the output inductor current in this case.

7.10. Practical Implementation of Control Method

The proposed PWM control for the simplified voltage-fed ZS-MC can be implemented in simple way when a digital signal processor (DSP) and a complex programmable logic device (CPLD) are employed. Then the duty cycle, t_{on}, is calculated as

$$\Delta t_{on1} = \frac{M \sin \omega t_1 - MN}{MX_1 - MN} \cdot \frac{T_C}{2} \tag{7.22}$$

$$\Delta t_{on2} = \frac{M \sin \omega t_2 - MN}{MX_2 - MN} \cdot \frac{T_C}{2} \tag{7.23}$$

$$\Delta t_{on} = \Delta t_{on1} + \Delta t_{on2} \tag{7.24}$$

where MX_1 and MX_2 are the voltage values of top voltage envelope at instants t_1 and t_2, respectively; MN is the voltage value of bottom voltage envelope at instant t_2. This can be illustrated by Figure 7.25. The upper figure shows the original carrier variable triangle waveform and the sinusoidal reference; the lower figure shows the newly generated constant carrier and new reference waveform. They generate the same PWM for the switches.

The same equations (7.22)-(7.24) can be applied to a three-phase system to produce three PWM pulse sequences S_A, S_B, and S_C. The produced PWM pulse sequences should be distributed to 9 ac switches in order to generate the expected PWM pulses. For this purpose, six additional logical signals are used to help the PWM pulse generation, where S_{z1}, S_{x1}, and S_{y1} denote the indicators for their respective phase-c, phase-a, and phase-b of the top voltage envelope. For example, S_{z1}=1 when phase-c voltage is the largest value among the three phase voltages. S_{y2}, S_{z2}, and S_{x2} denote

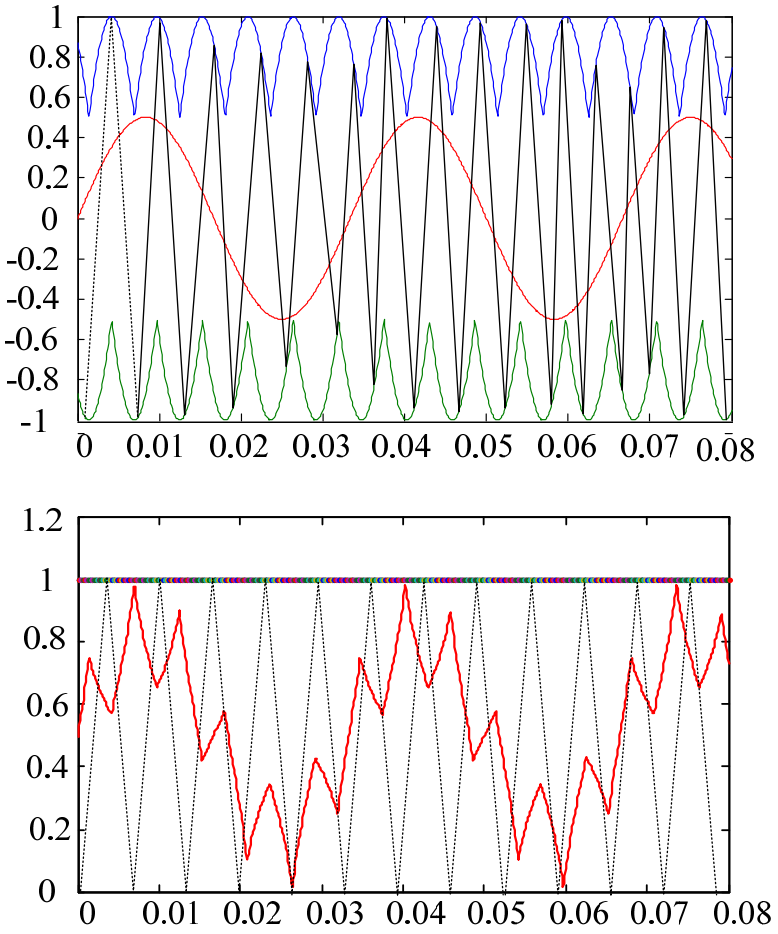


Figure 7.25. Transformation of the duty cycle

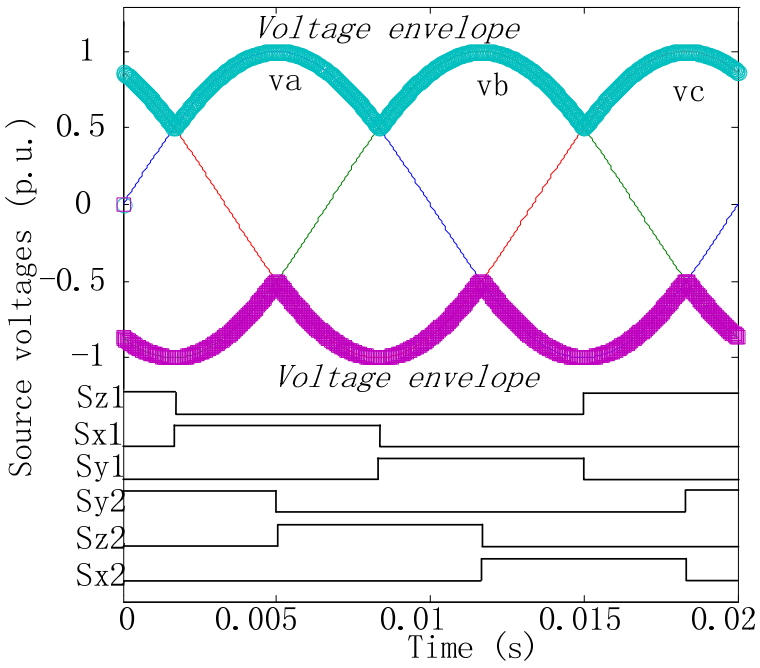


Figure 7.26. Indicators of the voltage envelopes

the indicators for their respective phase-b, phase-c, and phase-a of the bottom voltage envelope. For example, S_{y2}=1 when phase-b has the minimum voltage among the three phase voltages.

7.11. Experiments results to demonstrate voltage boost function by using maximum boost control

A prototype of the simplified voltage-fed ZS-MC has been built in the laboratory. Simulations and experiments have been carried out to verify the concept and theoretical analysis. In the experiment, the simplified voltage-fed ZS-MC was fed from the grid (source) and a R-L load was connected to the output of the ZS-MC. System parameters for both simulations and experiments are as follows: the Z-source network with L_z=1mH, C_z=330μF, the R-L load with R=20Ω, L=6.3mH, and the grid source frequency is 60 Hz. In order to demonstrate the operation of the simplified voltage-fed ZS-MC and to verify the control method, three cases have been investigated: (1) buck mode without shoot-through; (2) boost mode; (3) transition from buck mode to boost mode.

(1) Case 1: buck mode without shoot-through

The simplified voltage-fed ZS-MC works in the buck conversion mode when no shoot-through is inserted, operating just like the traditional MC. Figure 7.27 (a) and (b) show the simulation and experimental waveforms for the buck operation: shoot-through duty ratio $D = 0$, boost factor B=1, and $G = BM = 0.5$. The voltage gain measured at 0.43, which is consistent with the theoretical value of 0.5 considering voltage drops across the line impedance and MC switches. Figure 7.28 shows the PWM duty cycles calculated by (29)-(31), output 3-phase currents, and output phase voltage. The output 3-phase currents are

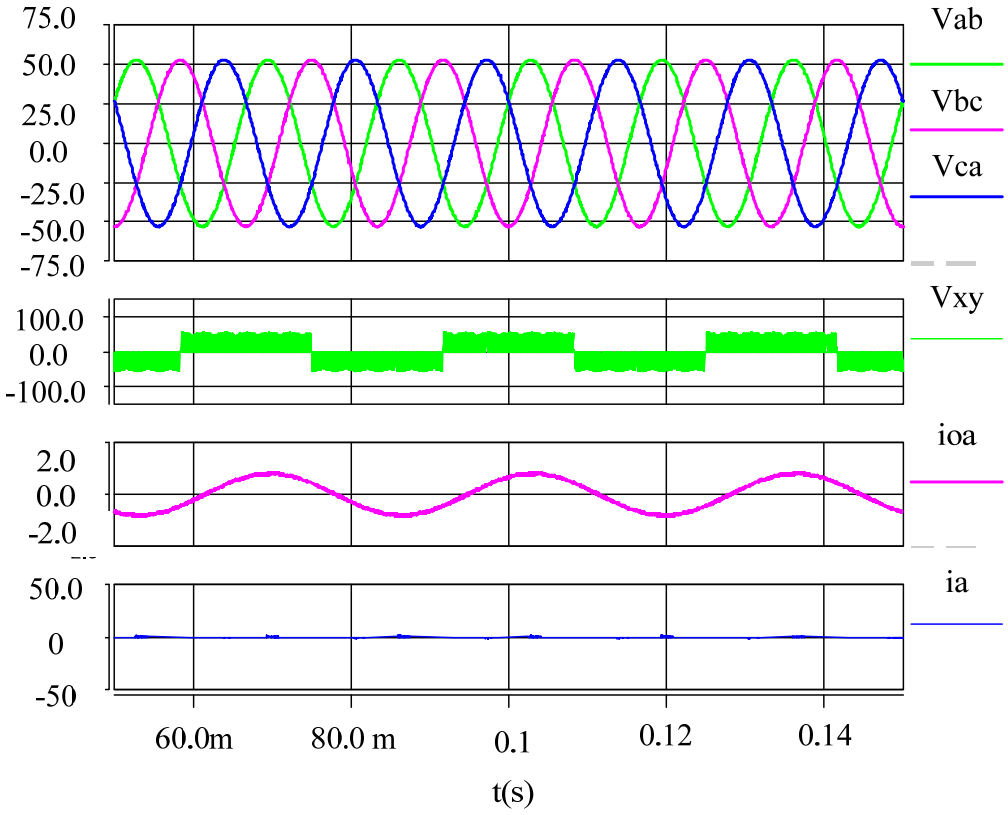
perfectly sinusoidal, which verify the proposed PWM method based on (29)-(31), and the logical functions.

(2) Case 2: Boost mode with shoot-through

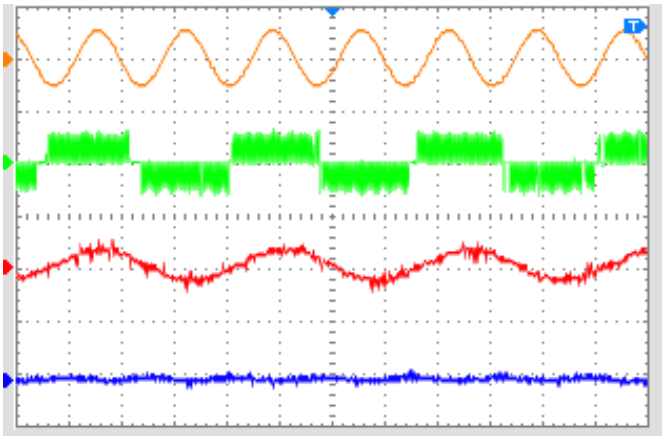
Figure 7.29 (a) and (b) show the simulation and experimental results, in which M=0.5 and the maximum boost control was employed to boost voltage. From (21) and Figure 3.23, we know that the boost factor B should be 2.0 and the voltage gain should be one, i.e., G=MB=1.0. The measured voltage gain from the experiment was 0.992, which agreed well with the theoretical value. In the simulation, source harmonics and line impedance were included to mimic the real source power from the grid. Both simulation and experiment agreed well with each other.

(3) Case 3: Transition from buck mode to boost mode

This case shows the transition process from the buck mode to boost mode. At the beginning, the simplified voltage-fed ZS-MC operates in the buck mode without inserting any shoot-through, shoot-through states were suddenly added in the PWM pulses. Figure 7.30 shows this transition. It can be seen that both output voltage and load current suddenly increased after the shoot-through with the maximum boost control was introduced. The voltage gain increased from 0.43 to 0.992. The well-agreed simulation and experimental results confirm the operation of the simplified voltage-fed ZS-MC.



(a) Simulation results



(b) Experimental results

Figure 7.27. Buck operation of the simplified voltage-fed ZS matrix converter: from top to bottom, four traces are the input line-line voltage to the Z-source network, the output line-line voltage from the matrix converter, the output phase current from the matrix converter, and the input phase current to the matrix converter.

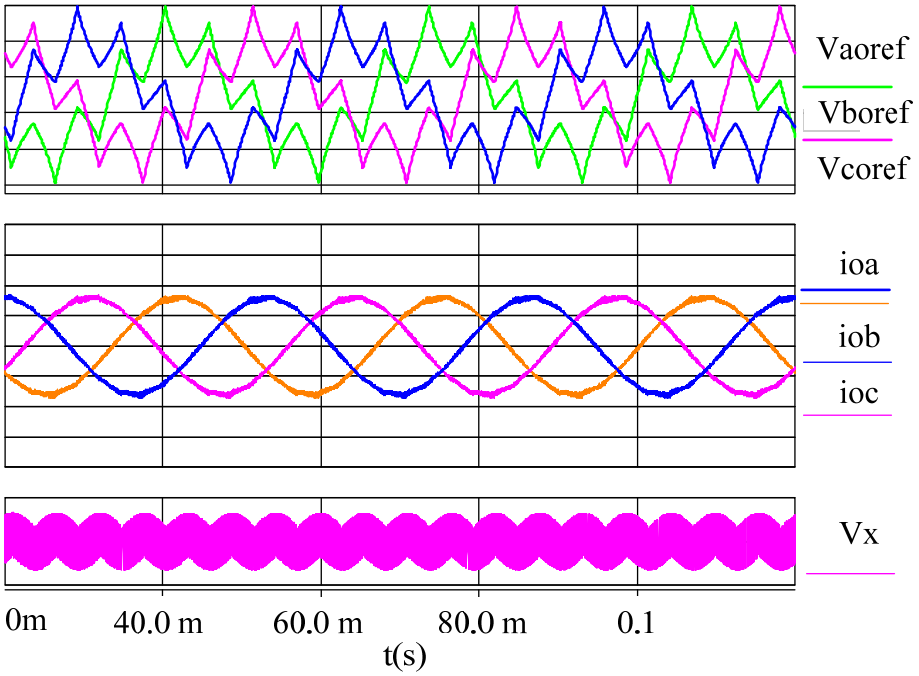
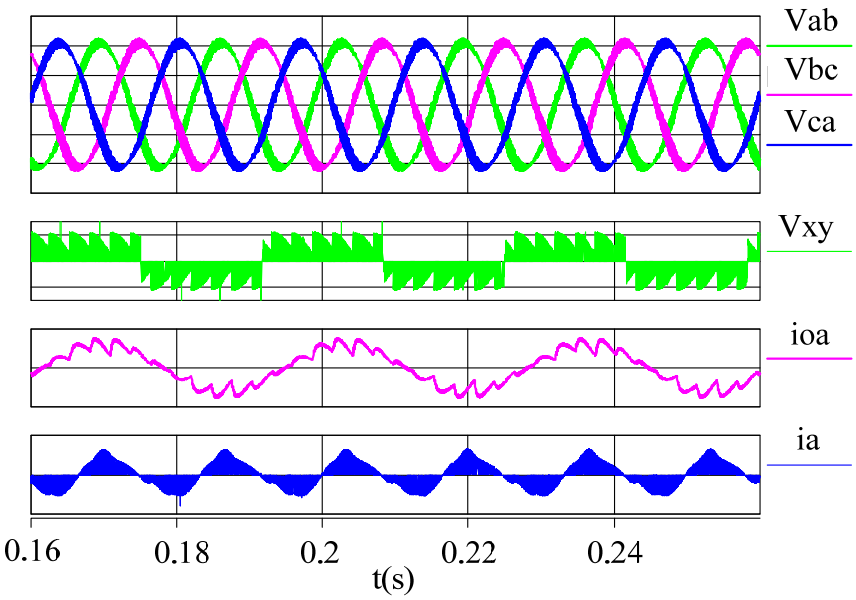
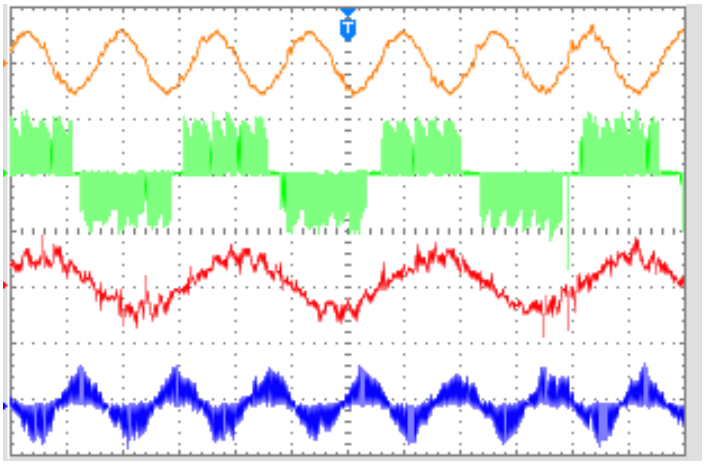


Figure 7.28. PWM duty cycles, output currents of three phases from the matrix converter, and the matrix converter's output phase voltage, from top to bottom, respectively

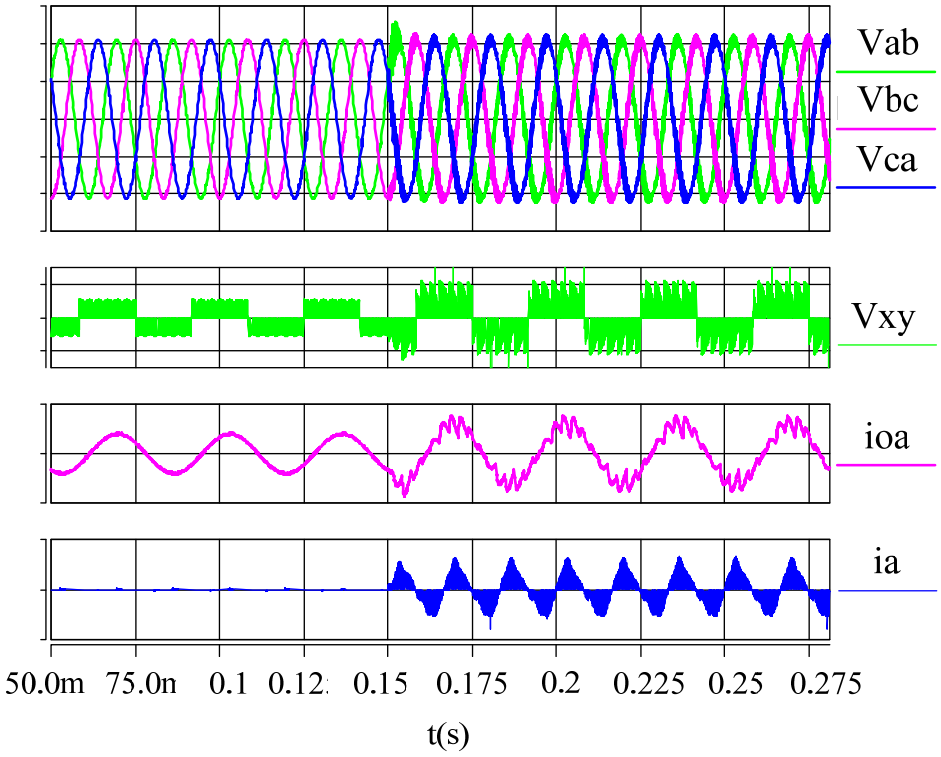


(a) Simulation results

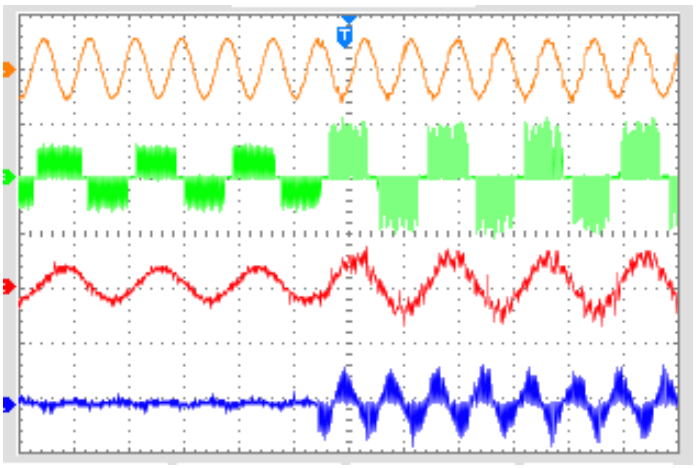


(b) Experimental results

Figure 7.29. Boost operation of the simplified voltage-fed ZS matrix converter: from top to bottom, four traces are the input line-line voltage to the Z-source network, the output line-line voltage from the matrix converter, the output phase current from the matrix converter, and the input phase current to the matrix converter.



(a) Simulation results



(b) Experimental results

Figure 7.30. Transition from the buck mode to the maximum boost control: from top to bottom, four traces are the input line-line voltage to the Z-source network, the output line-line voltage from the matrix converter, the output phase current from the matrix converter, and the input phase current to the matrix converter.

7.12. Simulation and Experimental Results to demonstrate hybrid minimum stress control

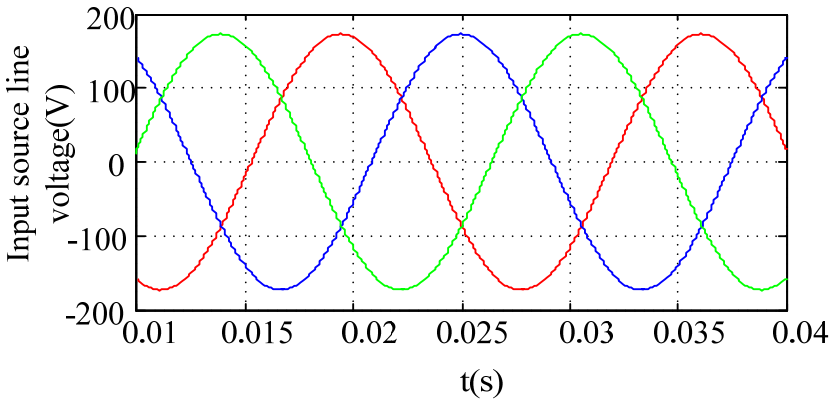
To verify the theory analysis of the four control strategies, the simulations are conducted with the following parameters:

$V_{im} = 100V,\ f_i = 60Hz,\ f_o = 85Hz, L = 600uH, C = 200uF, L_o = 6mH, R_o = 4\Omega$

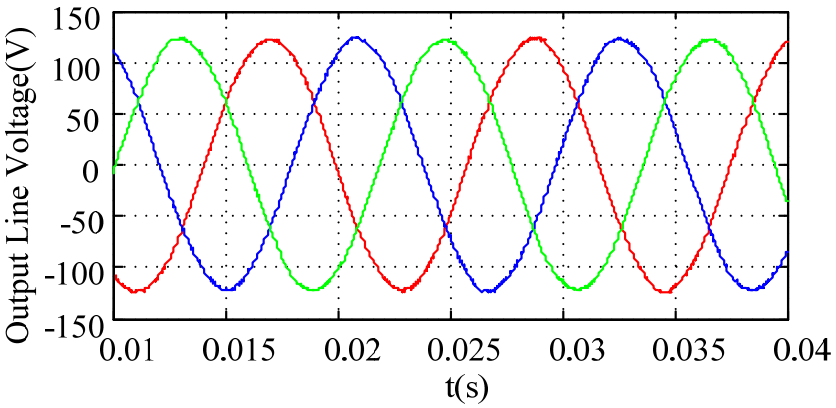
$P_{rated} = 2.5kW$

(1) Demonstration of voltage gain equations and output harmonics through simulation

To demonstrate the G-M curves in Figure 7.8, maximum constant boost control, simple maximum boost control and maximum boost control are simulated under M=0.6. Figure 7.13 shows the input source line voltage, output line voltage for traditional non-shoot through control. Figure 7.14 shows the output line voltage, input current at the source, input current before matrix converter and also the input voltage before matrix converter, for maximum constant boost control. Compared with the first case, this method increases the voltage gain. Figure 7.15 and Figure 7.16 shows simulation results for simple-maximum boost control and maximum boost control respectively. It can be seen that for simple-max and max boost, the output line voltage and input current is distorted, although it preserves a little big higher gain. For maximum constant boost control, both output voltage and input line current are controlled in a good shape, which posses much lower THD.

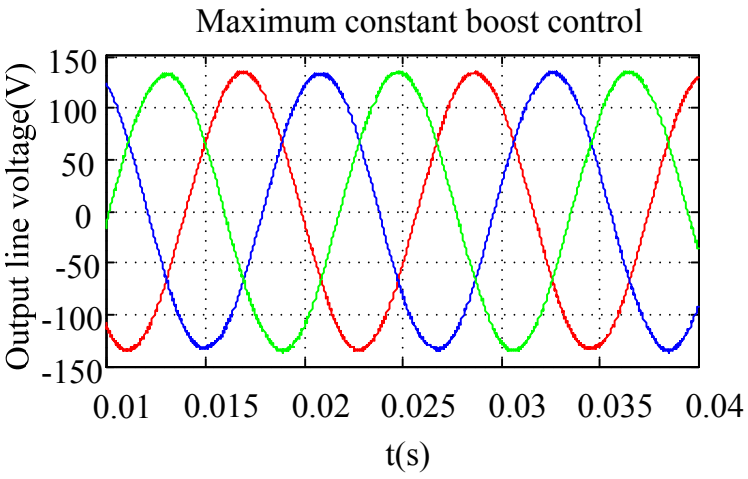


(a) Input voltage source line to line voltage

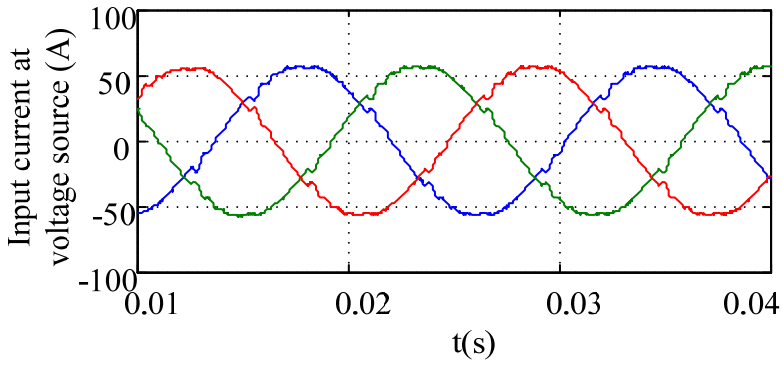


(b) Output line to line voltage at the resistive load

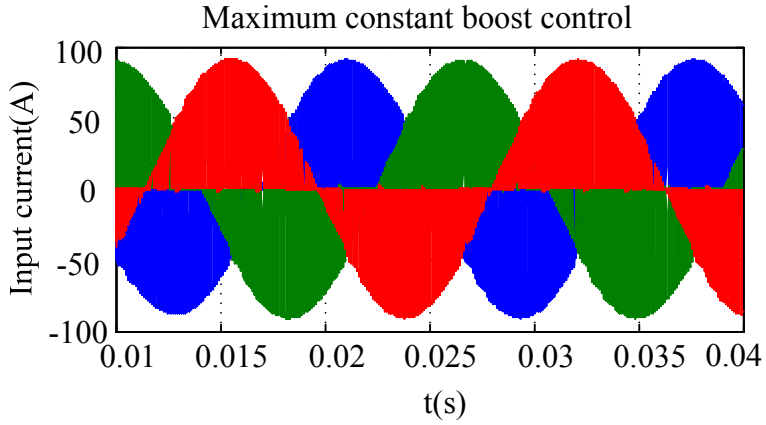
Figure 7.31.Simulation results at non-shoot through at M=0.6



(a) Output line to line voltage at the resistive load



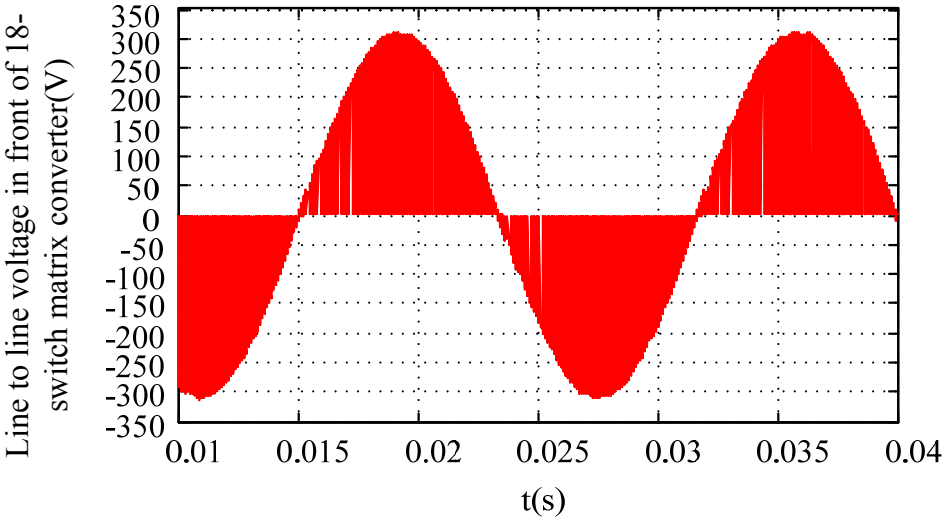
(b) Input current at the voltage source



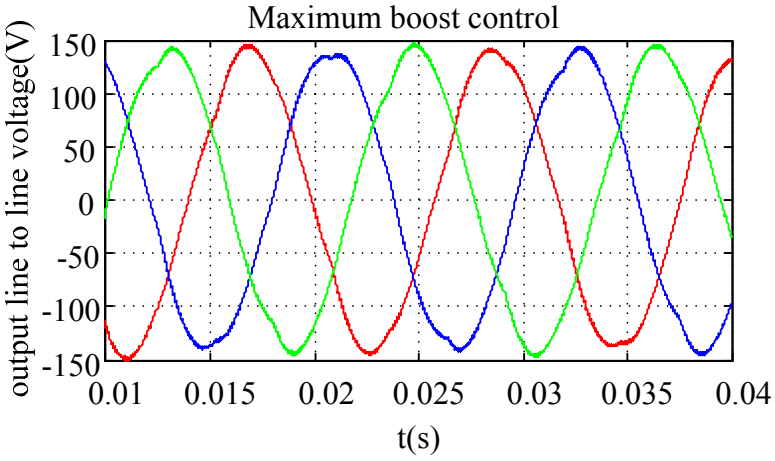
(c) Input current right before matrix converter

Figure 7.32.Simulation results at maximum constant boost at M=0.6

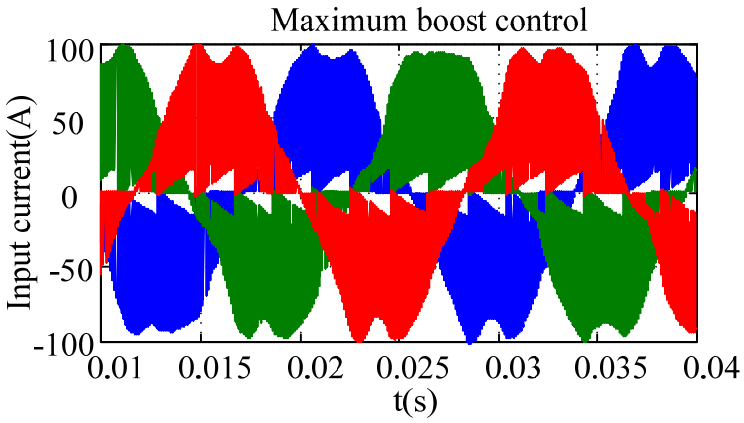
Figure 7.32 (cont'd)



(d) Input line to line voltage right before matrix converter

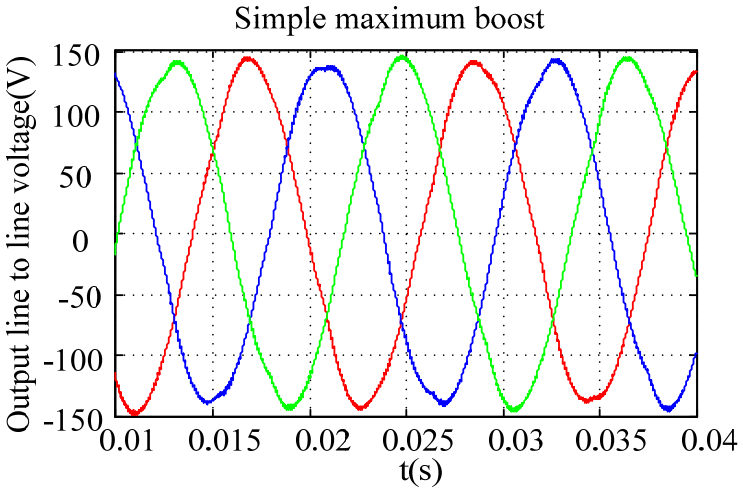


(a) Output line to line voltage at the resistive load

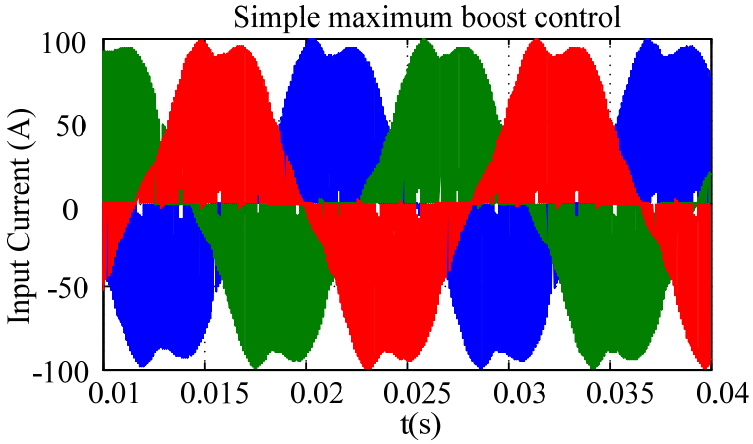


(b) Input current right before matrix converter

Figure 7.33.Simulation results at maximum boost control at M=0.6



(a) Output line to line voltage at the resistive load



(b) Input current right before matrix converter

Figure 7.34.Simulation results at simple-max boost at M=0.6

(2) Demonstration of voltage stress comparison analysis through simulation and experiments

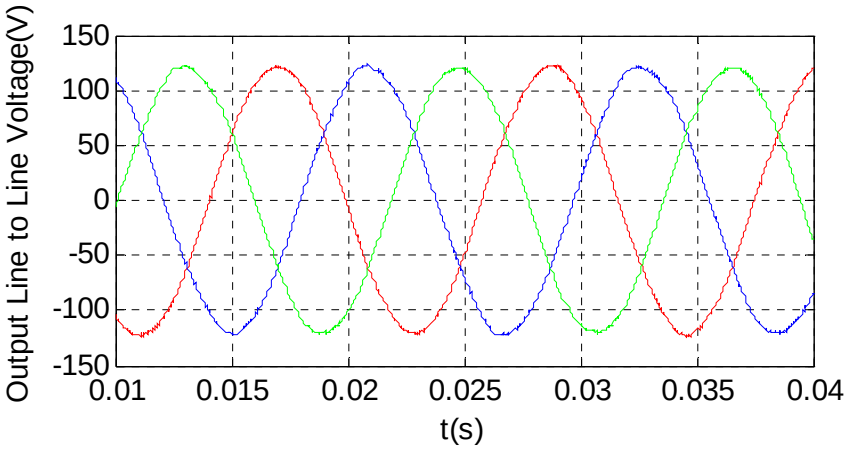
To demonstrate the B-G curves in Figure 7.11, simulation waveforms with different voltage stresses at the same voltage gain G=0.866 are shown in Figure 7.36, in which the switch voltage stress is represented by input line to line voltage right before matrix converter. It can be seen that at the voltage gain smaller or equal to 0.866, non-shoot through control preserves smaller voltage stress on the switch. In this special case G=0.866, maximum

constant boost posses the same voltage gain and voltage stress. But when G<0.866, non-shoot through has lower stress. At any case, maximum boost control has the highest stress among the three.

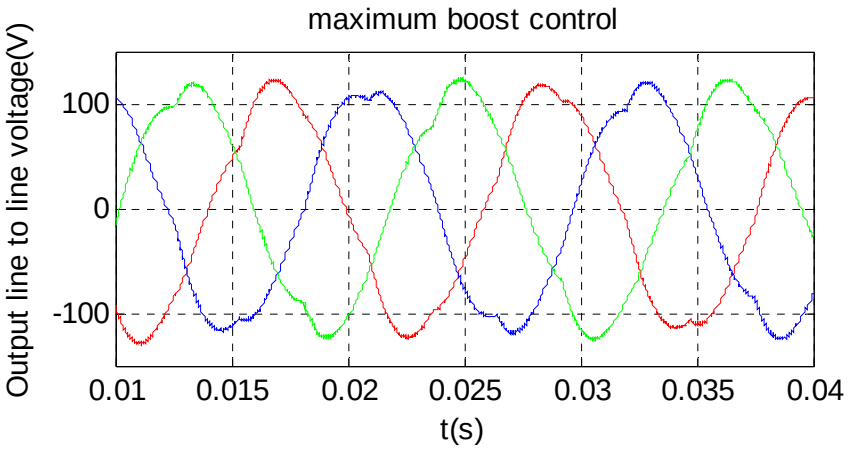
A prototype is built in the lab to verify the proposed control methods. A 18-switch 600V/200A RB-IGBT module from FUJI corp. has been used as the matrix converter. And a Z-network with the aforementioned simulation parameters has been built and installed between dc voltage source and matrix converter. An inductive load with 6mH inductance and 4ohm resistor has been utilized. Input voltage is set to be 100V, 60Hz. The output voltage frequency is set to be 30Hz.

To demonstrate the G-M curves in Figure 7.8, experiment waveforms of different voltage gains at M=0.661 and M=0.2 of four control strategies (non-shoot-through, simple maximum boost, maximum boost and maximum gain) are shown in Figure 7.37 and Figure 7.38, where the voltage gain is represented by the load current. Table 7-6 lists the theoretical voltage gains and measured simulation and experimental voltage gains. It can be seen that the simulation and experimental results are consistent with the theory analysis at both M>0.5 and M<0.5 cases.

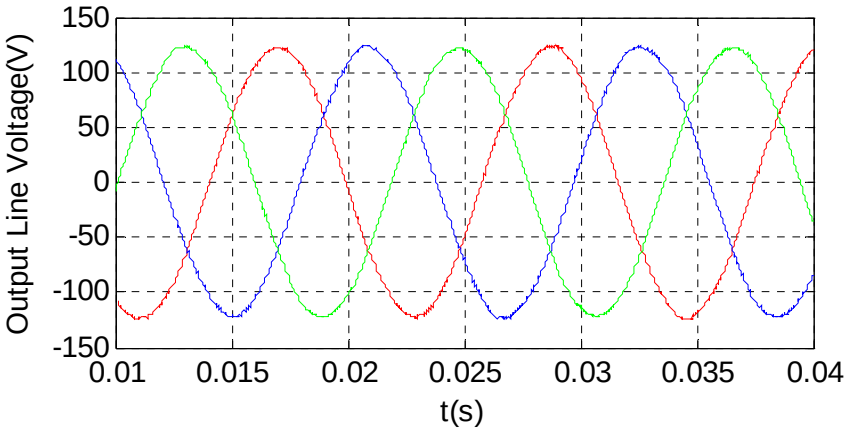
To demonstrate the B-G curves in Figure 7.11, experimental results with different voltage stresses at the same voltage gain G=1.073 and G=0.8 respectively are shown in Figure 7.39 and Figure 7.40, in which the switch voltage stress is represented by line to line voltage right before matrix converter $V_{a'b'}$. The theory analysis, measured simulated results and experimental results for voltage gain and voltage stress at the



(a) Maximum constant boost control

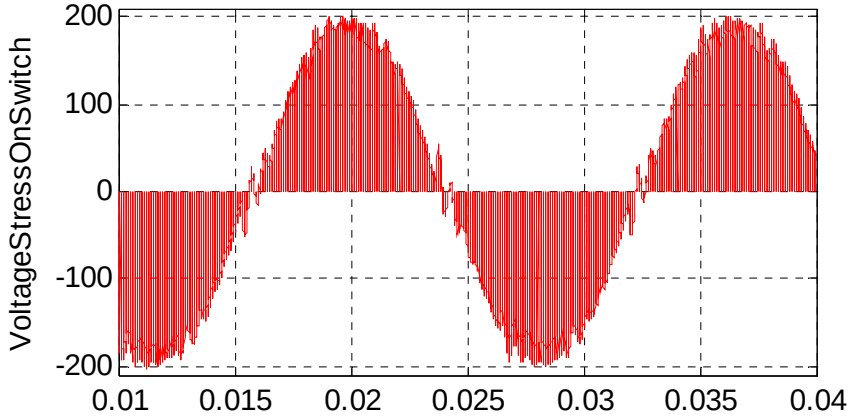


(b) Maximum boost control

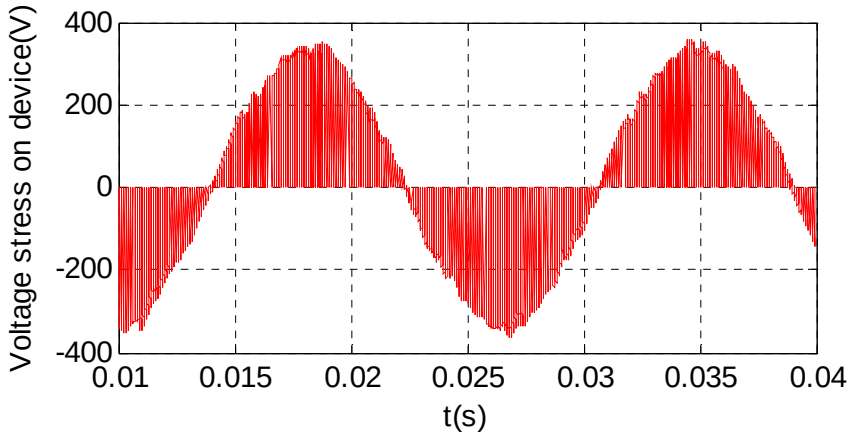


(c) Non-shoot through control

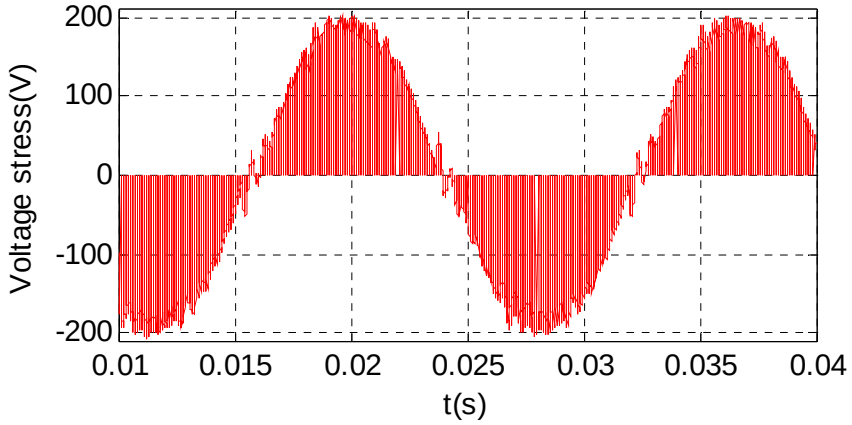
Figure 7.35. Output line to line voltage at G=0.866 for three methods



(a) Maximum constant boost control



(b) Maximum boost control



(c) Non-shoot through control

Figure 7.36. Input line voltage right before matrix converter at G=0.866

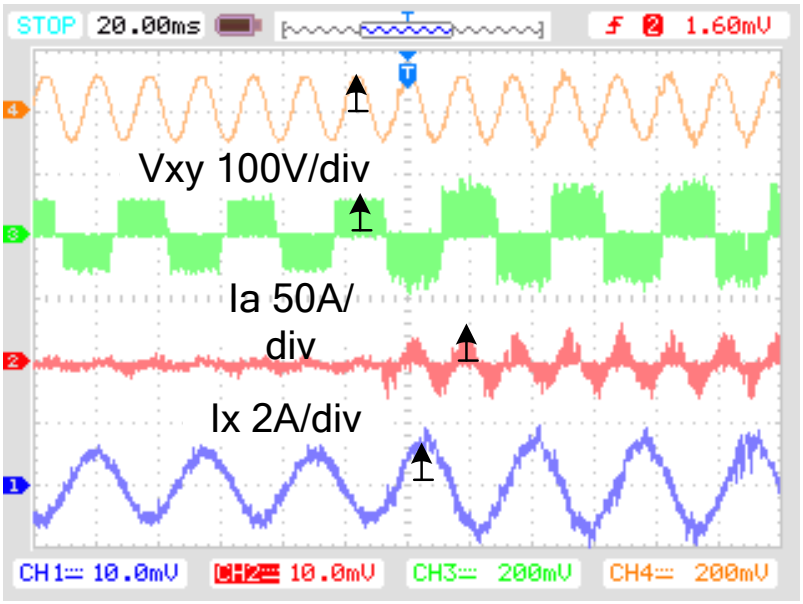


Figure 7.37. Voltage gain comparison at M=0.661: non-shoot-through control at $t \in [0, 0.1]$ and maximum constant boost control at $t \in [0.1, 0.2]$

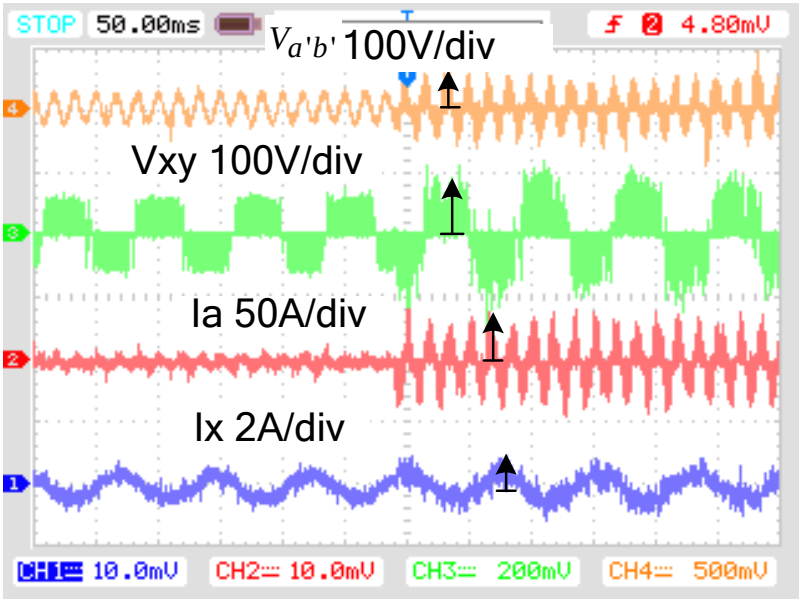


Figure 7.38.Voltage gain comparison at M=0.2: non-shoot-through control at $t \in [0, 0.1]$; maximum constant boost control at $t \in [0.1, 0.2]$; simple maximum boost control at $t \in [0.2, 0.4]$

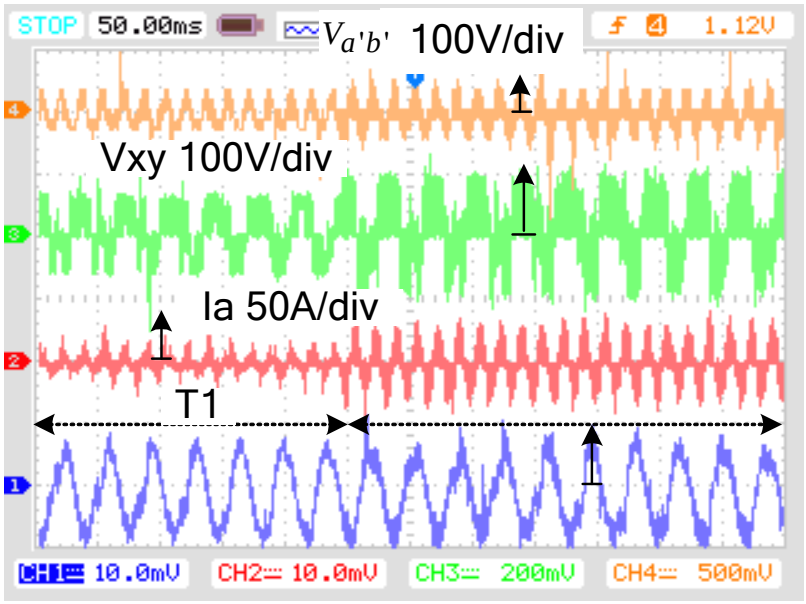


Figure 7.39 Voltage stress comparison at G=1.073: maximum boost control with M=0.542 at $t \in [0, 0.1]$; hybrid minimum voltage stress control with M=0.866 at $t \in [0.1, 0.2]$.

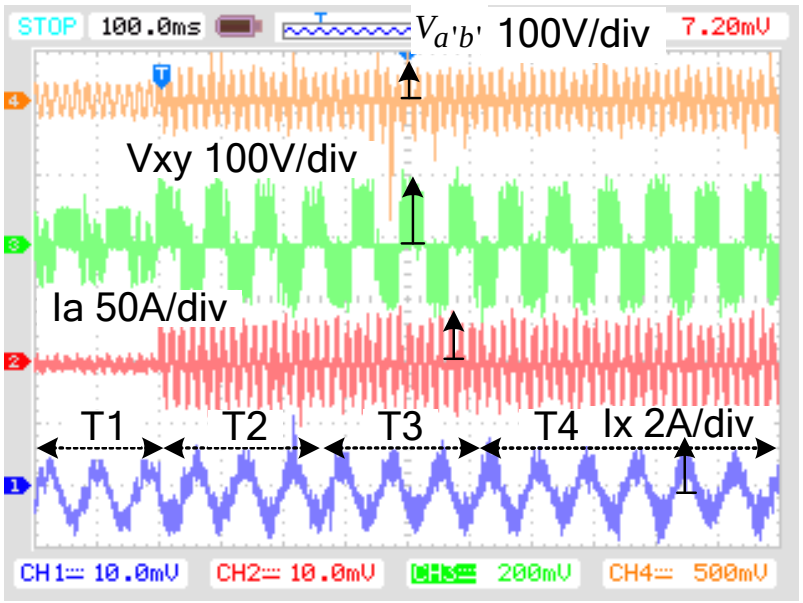


Figure 7.40. Voltage stress comparison at G=0.8: Hybrid minimum stress control at $t \in [0, 0.1]$; simple maximum boost control at $t \in [0.1, 0.2]$; maximum boost control at $t \in [0.2, 0.4]$;

same G are shown in Table 7-6 and Table 7-7 and they are consistent with each other. It also can be seen that the hybrid control can achieve less voltage stress than other control strategies

In conclusion, the simulation and experiment results demonstrate that maximum gain

can be achieved at the maximum gain control and minimum voltage stress across the switch can be achieved through hybrid minimum voltage stress control.

Table 7-6.Voltage gain comparison at certain M

			N-S	Simple-Max	Max	Max-Const
M=0.661	theory	G	0.66	0.41	1.16	1.08
	Simulation	G	0.69	0.35	1.2	1.01
	Experiment	G	0.72	0.33	1.15	0.95
M=0.2	theory	G	0.2	0.3	0.28	0.21
	Simulation	G	0.22	0.15	0.12	0.23
	Experiment	G	0.19	0.1	0.08	0.18

Table 7-7.Voltage stress comparison at certain G

			Minimum stress	Maximum Boost	Simple Max
G=1.073	Theory	B	1.24	1.696	--
	Simulation	B	1.42	1.923	--
	Experiment	B	1.442	1.73	--
G=0.8	Theory	B	1	--	1.997
	Simulation	B	1	--	2.08
	Experiment	B	1.08	--	2.13

7.13. Summary

In Z-source matrix converter, the insertion of shoot through state brings the voltage boost function to the traditional matrix converter. This chapter proposes three methods to introduce shoot through state: simple maximum boost, maximum boost and maximum constant boost. In terms of voltage gain, maximum boost control and maximum constant

boost control can make voltage gain exceed 1. In terms of harmonic distortion, maximum constant boost control and non-shoot through control posses much lower THD than other methods. In terms of voltage stress and switching loss, maximum boost and simple maximum boost control would bring higher voltage stress and switching loss to the devices. In conclusion, at voltage gain smaller than 0.866, traditional non-shoot through control is the optimum control for Z-source matrix converter, and at voltage gain higher than 0.866, maximum constant boost control should be utilized. At voltage gain higher than 1.144, which is out of the voltage gain range of maximum constant boost control, maximum boost control can be used. The proposed hybrid minimum stress control has been fully demonstrate by simulations and experiments. In addition, a concept of Pulse-Width-Amplitude-Modulation (PWAM) has been proposed for Z-source MC control. In summary, the benefits of PWAM with maximum constant boost shoot through control for this circuit are (1) High efficiency at wide output voltage and current range;(2) low low-order output current harmonics;(3) low input current spike (lower input current value);(3)low input and output line voltage spike (Lower input and output voltage value);(4)low switch voltage and current stress;(5)high power factor.

CHAPTER 8 DISCONTINUOUS OPERATION MODE

8.1. Introduction

The circuit analysis and control methods proposed for current-fed quasi-Z-source inverter are based on one important assumption: the capacitor voltage is almost constant and equal to the input voltage. This assumption becomes invalid when the capacitor is very small or the lower power factor is low in some applications that the volume is a very crucial factor. The capacitor voltage has high ripple or even becomes discontinuous in these cases. This is similar to the discontinuous operation mode of boost converter, which has discontinuous inductor current instead at low inductance and low power factor. In these cases, the circuit has two new operations modes except for the normal three modes, which is called discontinuous operation modes. This section analyzes the characteristics of the discontinuous operation modes, and derives the critical conditions for these new modes under different control strategies. Simulation and experiment results are given to verify the theoretical analysis.

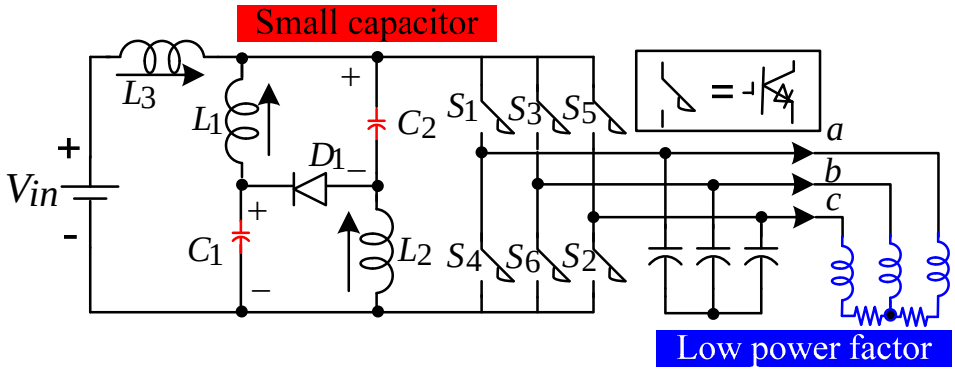


Figure 8.1. RB-IGBT based current-fed qZSI configuration

with discontinuous input current

Table 8-1. Definitions of the variables

C	*Capacitance of capacitors in Quasi-Z network*
L	*Inductance of inductors in Quasi-Z network*
Iin	*Input current of the current-fed qZSI*
IL	*Current through the inductors of the Quasi-Z network*
IC	*Current through capacitors of the Quasi-Z network*
Ipn	*Current fed to the inverter bridge*
Is	*Current through the switch of inverter bridge*
iac	*Output peak phase current*
Iorms	*Output phase rms current*
Vin	*Input dc bus voltage*
VC	*Voltage across the capacitors of the Quasi-Z network*
Vl-lpeak	*Output peak line to line voltage*
Vorms	*Output phase rms voltage*
M	*Modulation index*
Dop	*Open zero duty ratio*
B	*Current boost factor*
Top	*Open zero state in one switching cycle*
Ts	*Switching period*
Z	*Load impedance*
cos(Φ)	*Load power factor*

8.2. Two discontinuous modes when capacitance is small or load power factor is low

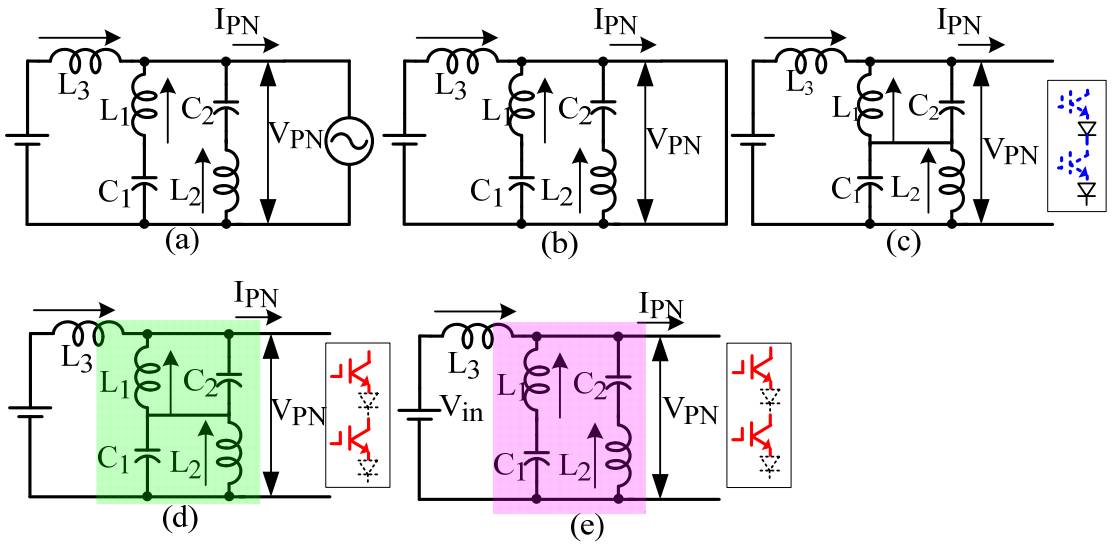


Figure 8.2. Possible operations modes of current-fed qZSI: (a) mode 1(b) mode 2, (3) mode 3, (4) mode 4, (5) mode 5

The novel current-fed qZSI can buck/boost voltage and achieve bidirectional power flow without replacing the diode with an active switch, due to the two extra open zero states. The basic control principle is to turn some of the short zero state into open zero state. Figure 8.2. (a) (b) (c) shows the equivalent circuits of the current-fed qZSI in continuous mode which is detailed analyzed in paper [3]. The basic operating principle assumes that the capacitor voltage is almost constant and equal to the input voltage. However, the capacitor voltage can have high ripple or even becomes discontinuous when the capacitance is low or the load power factor is low. So there are two additional operation modes in discontinuous mode, similar to the new modes in voltage-fed Z-Source inverter [4]. (Miaosen's paper)

Mode 1-3 (Continuous modes): Mode 1: active state, the inverter bridge is in an active state and the dc link voltage V_{pn} is equal to the equivalent output voltage V_{eq}; the diode is off if the equivalent voltage satisfies $V_{eq} < 2V_{in}$. Mode 2: Short zero state, the inverter bridge is equivalent to a short circuit by turning on the upper and lower switches in the same phase leg

or in the same two phase legs, or three phase legs together. The dc link voltage is zero, so the diode is off. Mode 3: Open zero state, the inverter bridge is equivalent to an open circuit by turning off all the upper switches or turning off all the lower switches. The diode is turned on, so the dc link voltage is equal to sum of the two capacitor voltage.

Mode 4 (Discontinuous mode I): In open zero state, the diode is on and the inverter bridge is off. So the capacitor is being charged. But in other two states, the capacitor keeps discharging because the unchanged inductor current. At the end of mode 2, if the capacitor voltage decreases to be smaller than half of the output line to line peak voltage in short zero state, at the moment that the inverter is switched to active state again, the diode in quasi-Z network will be turned on because the voltage drop on the diode is positive. But the diode in RB-IGBT will be reverse biased; the inverter is equivalent to an open circuit. The capacitor will be charged again in this new open zero state. This state is described in Figure 8.2(d). In mode 4, the capacitor voltage satisfies $V_C < V_{l-lpeak} / 2$.

Mode 5 (Discontinuous mode II): At the end of Mode 4, when capacitor voltage increases to be equal to half of the output peak line to line voltage and the inverter bridge is still switched in active state, the diode in QZ-network will be reverse-biased. So the capacitor voltage will stay at $V_{l-lpeak} / 2$ until the end of active state. But the voltage drop on the RB-IGBT is still smaller or equal to be zero, the inverter bridge is still in open circuit state. The equivalent circuit of Mode 5 is shown in Figure 8.2(e). This mode will also happen when the capacitor voltage decreases to be equal to half of the $V_{l-lpeak}$ in mode 1. The switch will still be switched in active state, but the circuit will enter into mode 5 until the end of active state. In mode 5, the capacitor voltage and inductor current satisfies:

$$V_C = \frac{V_{l-lpeak}}{2}, \quad I_L = -\frac{I_{in}}{2}$$

In this paper, the discontinuous mode is defined as a new mode when the capacitor voltage satisfies $V_C \le V_{l-lpeak}/2$. In another word, when open zero state or critical open zero state happens during the time of active switching, discontinuous mode happens. So mode 4 and 5 are included in discontinuous mode. At the same time, two assumptions have been made to discuss these modes: (1) The inductor is big enough to maintain constant current direction in motoring mode; (2) RB-IGBT has enough voltage rating.

To be concluded, mode 4 happens when capacitor voltage already falls below $V_{l-lpeak}/2$ when active state switching starts; in this case, the QZ source diode will be forced on and inverter switch will be reverse biased; the circuit is equivalent to the open zero state. Mode 5 happens when capacitor voltage increases from lower than $V_{l-lpeak}/2$ to equal in active state switching period; in this case, inverter switch will be reverse biased and capacitor voltage stays at $V_{l-lpeak}/2$ until the end of active state. These two discontinuous operation modes change: (1)voltage gain equation, due to that part of active states is transferred into open zero state, in which the output equivalent voltage is equal to two times of capacitor voltage, not the output line to line voltage; (2) capacitor voltage ripple, which becomes much bigger than continuous mode; (3) device voltage stress, because the device voltage stress is equal to two times of capacitor voltage, of which the maximum value is greatly increased.

8.3. Capacitor voltage waveform in discontinuous modes

DCM has two basic degrees defined here: the first is the capacitor voltage decreases to below half of output line to line voltage but above zero; the second is the capacitor voltage

decreases to zero. In discontinuous mode, the capacitor voltage has big ripple. It decreases below half of output line voltage in mode 4 and keep equal to that in mode 5. When capacitance reduces even more, in mode 4, it may decrease to zero and maintain zero in mode 5. The advantages and disadvantages of these discontinuous operation modes are: this DCM mode if can be utilized, it will only need a much smaller capacitance. And the voltage boost ratio can go beyond 2; However, the voltage stress on the capacitor and device will be increased to even 2 times.

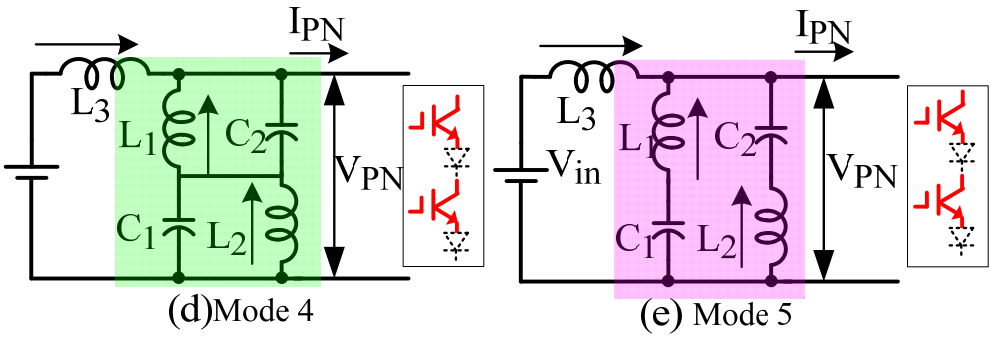
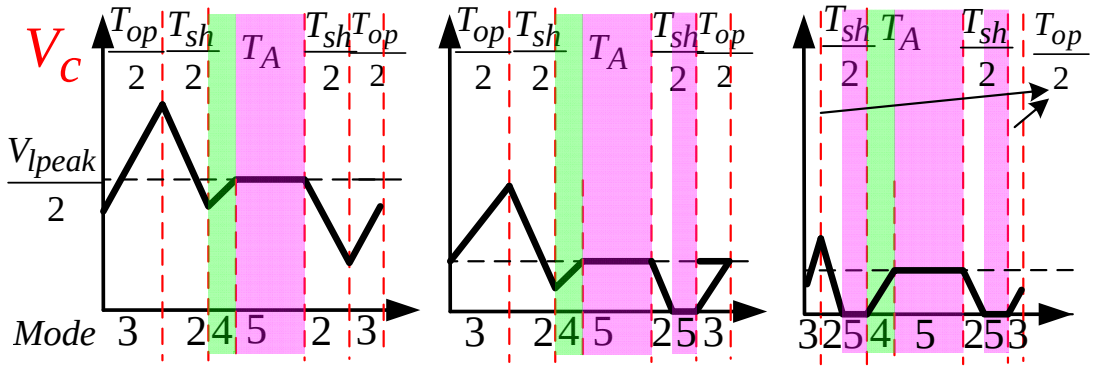
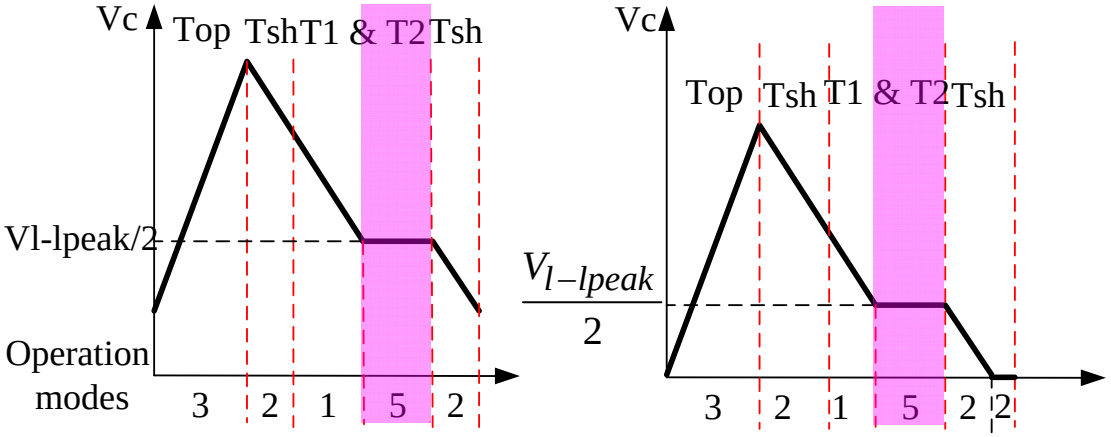


Figure 8.3 Two discontinuous operation modes

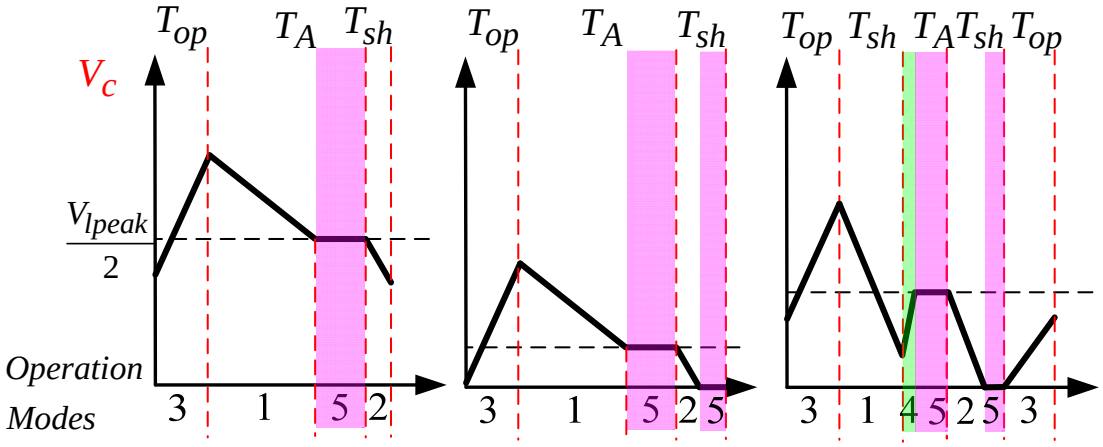
Different modulation methods will yield different discontinuous waveforms due to different sequences and combinations of the operation modes. The specialty of current-fed quasi-Z-source inverter is it has four basic circuit states in one switching cycle including two active states, one short zero state and one open zero state. Thus the switching sequence is more flexible and complex, which makes more variations in discontinuous mode characteristics. For example, in SPWM based modulation, different design and location of the shoot through control reference waveforms result in different control strategy, such as simple boost control, maximum boost control, maximum constant boost control etc. In SVPWM control, there are totally 24 sequences to place the four vectors. Although it is reduced to 19 after eliminating some redundant cases, the variation is still much bigger than 6 in three



(a) Capacitor voltage waveform under SPWM control



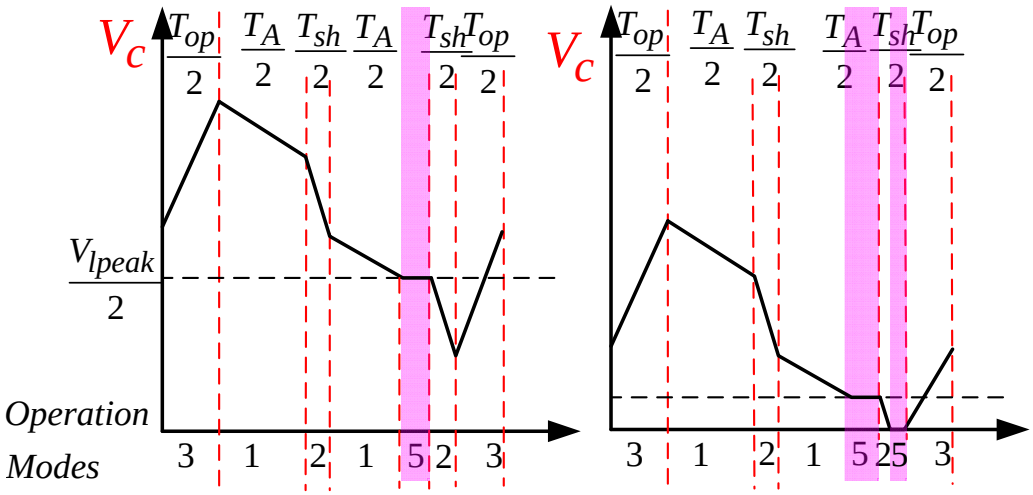
(b) Capacitor voltage waveform under SVPWM control sequence 1 (maximum constant boost control)



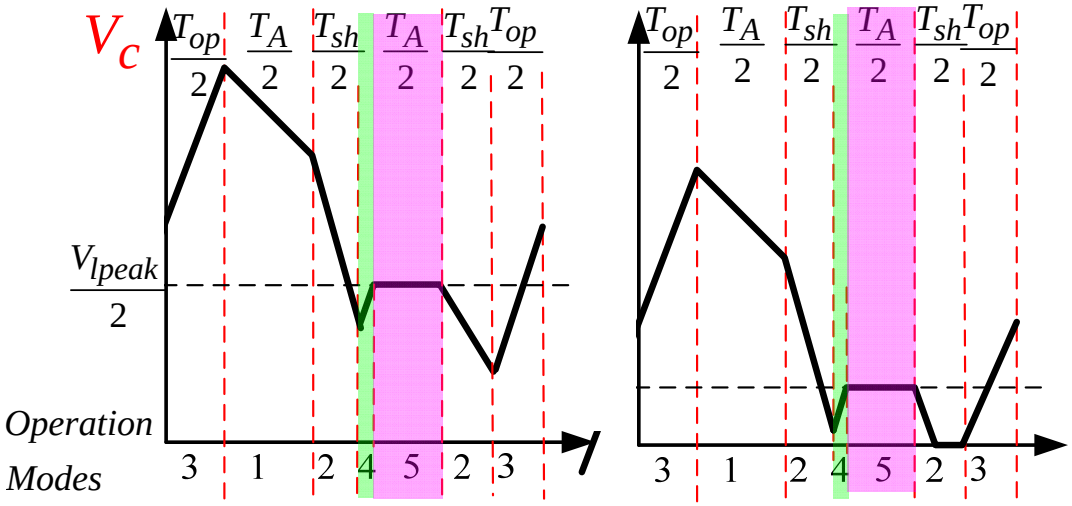
(c). Capacitor voltage waveform under SVPWM control sequence 2

Figure 8.4. Capacitor voltage waveforms at different modulation methods

Figure 8.4 (cont'd)



(d). Capacitor voltage waveform under SVPWM control sequence 3



(e). Capacitor voltage waveform under SVPWM control sequence 4

vector cases. Several examples from SPWM method and SVPWM method are listed below to present the different capacitor voltage waveforms.

8.3.1. SPWM Control -Maximum Constant Boost Control

The SPWM control for traidtional current source inverter is based on the on-line carrier-based PWM pattern generator. The principle is to first generate the votage source inverter control signal and then map them into current source inverter through the state machine equations. The mapping equations are derived by matching the SVPWM diagram of

VSI and CSI. To be extended, the principle to control current-fed Z-source inverter in SPWM way is first to generate the control signals for voltage-fed Z-source inverter and then map them to current-fed ones. There are two differences from the traditional ones: 1) To utilize the extra switching state, part of traditiona state needs to replaced by new state; to implement this, an extra shoot through reference is utilized to also compared with the carrier voltage; by different waveforms and placement of the shoot through reference, the control method is categoried into simple boost control, maximum boost control, maximum constant boost control, and so on. 2) the shoot through state in voltage-fed ZSI is mapped into open zero state in current-fed ZSI; thus a new mapping equation about these two need to be built.

In every switching cycle, one open zero state, one of the three short zero states are used along with two adjacent active states to synthesize the desired current. The basic principle of maximum constant boost control is to generate a maximum available constant shoot through duty ratio. It can not boost voltage as high as maximum boost control since the shoot through duty ratio is not the maximum all the time, but it can eliminate the low frequency current ripple, which greatly reduces the output harmonics. The side effect is to reduce the size of qZ-source network and at the same time, to reduce the current stress of the switches [5], by using a greater current boost for any given modulation index.

The time sequence of the PWM is as following: $T_{op}, T_{sh,} T_1, T_2, T_{sh,} T_{op}$. Assume the output voltage are the same in two active states during one switching cycle, then there will be two possible operation conditions, continuous voltage mode (CVM) and discontinuous voltage mode (DVM), shown as the second and the third waveforms in Figure 8.4 (a), respectively. The CVM is characterized as that the capacitor voltage is not decreased to zero.

The DVM is characterized as that the capacitor voltage falls to zero and stay in zero for a certain period of time, which happens when the capacitor is in a much smaller value or the power factor is very low.

In each switching cycle, the circuit starts with an open zero state T_{op}, during which the capacitor is being charged and the capacitor voltage increases with time. After T_{op}, the inverter switches to traditional short zero state. The capacitor voltage keeps decreasing until it reduces to half of the output line to line peak voltage. If short zero state still doesn't end at this point, the capacitor voltage will continue to decrease to be smaller than that. When active state starts, capacitor voltage begins to increase, which is characterized as mode 4. If it increases to be equal to half of output peak voltage before the active state ends, mode 5 comes into play by keeping the capacitor voltage almost constant and turning off the diode D until the end of active state. When the circuit turns into traditional short zero state the second time, the capacitor voltage will continue to decrease until the end of short zero state. During the whole switching cycle, the capacitor voltage is continuous; therefore this operation condition is termed as CVM. If the capacitance is extremely small or the load power factor is relatively low, it is possible that the capacitor voltage decreases to zero in the second half short zero state and remains zero until the next switching action. It is called DVM shown in the second one in Figure 8.4 (a). If the capacitor is even smaller, the capacitor voltage is also possible to fall to zero at the first time it enters into short zero state, as shown in the third figure of Figure 8.4 (a). At these two DCM case, the output voltage waveform will be affected and also the voltage gain will be tuned.

8.3.2. SVPWM Control

The basic idea of SVPWM control for current-fed qZSI is to turn some of the short zero states to open zero states [3]. In order to make the current stress on the inductor lowest, Dop should be designed to be zero at motoring operation and to be maximum at regeneration operation [3]. So the best operation point for voltage boost mode is when $D_{op} = 0$, which is same as traditional CSI; and the best operation point for voltage buck mode is when $D_{op} = 1 - D_A$, which means turning all the short zero state into open zero state at a fixed modulation index [3]. The instantaneous D_{op} varies with time, but the average duty ratio in each sector is constant. In order to keep D_{op} a constant value during a whole switching cycle to reduce the output harmonics and switching current stress, the average D_{op} is used. So the short zero state still exists with open zero state.

As long as the volt-seconds satisfy the voltage gain requirement, the division of the switching period and the placement of each vector can be flexible without affecting the output voltage waveform and value. The thing it affects is the input current ripple, device switching loss and output harmonics. Four examples of SVPWM have been given in Figure 8.4 (b), (c), (d). (e). Take sequence (c) as an example. Its sequence is T_{op}, T_A, T_{sh}. In T_{op}, the capacitor voltage increases; in T_A, capacitor voltage decreases. If it decreases to be equal to $V_{l-lpeak} / 2$ before the active state ends, the circuit enters into mode 5, in which the capacitor voltage will keep at $V_{l-lpeak} / 2$ level until the end of this active state. After that, in short zero state, the it will continue to decrease until the end, which is in mode 2. The next period starts with capacitor voltage being charging in open zero state. Thus there is only mode 5 in this sequence. In this process, if the capacitor is small enough or the power factor is extremely low, it is possible for the voltage to fall to zero during short zero state. In this

case, the mode 4 appears. The other sequences can be analyzed similarly to sequence (c). It is found that only sequence (e) has mode 4 & 5, and others only has mode 5 unless it enters into DCM. To be concluded, different modulation methods result in different capacitor voltage ripple; same modulation method but different switching sequences also cause different capacitor voltage ripple. Different ripple contributes to different output voltage ripple, thus harmonics. These differences also affect the critical conditions for discontinuous mode to happen.

8.4. Critical conditions for discontinuous mode

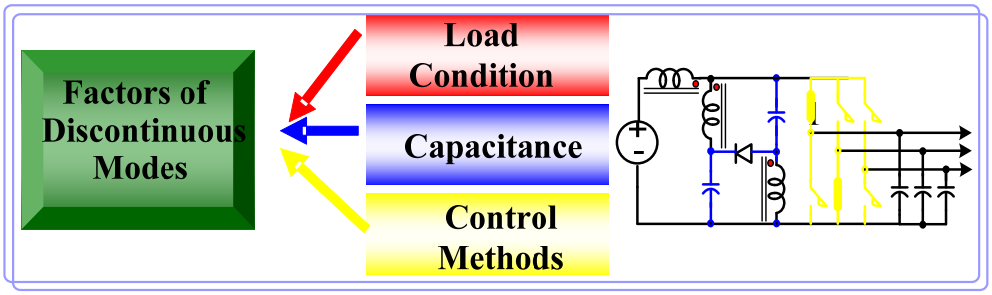


Figure 8.5. The factors causing discontinuous operation mode

Using a small capacitance can reduce the volumn and cost of the system, but at the same time, discontinuous operation modes will occur, in which the device understakes higher voltage stress. In addition, the current fed into the inverter is no longer always constant during active states, which causes additional harmonics in output voltage and current. So the critical condition of the discontinuous operation mode becomes important to the design of the capacitor.

The basic discontinuous operation critical condition is:

$$V_{C\min} \le \frac{V_{l-lpeak}}{2} \tag{8.1}$$

To guide the design procedure, this condition has to be transformed into the inequality in terms of the circuit parameters or control parameters. The possible factors that affect this operation mode is shown in Figure 8.5. The following related variables or parameters is summarized: (1) output power factor (2) output impedance (3) Z-network dc capacitance (4) control methods and variables, such as modulation index, shoot through duty cycle etc. In order to derive this, the general capacitor voltage ripple equation has to be derived first, and then the basic critical condition can be applied to that to obtain a complete critical condition equation.

8.4.1. Capacitor voltage ripple

As analyzed above, the capacitor voltage increases only in open zero state. So the peak to peak value of voltage ripple is:

$$\Delta V_c = \frac{i_C T_{op}}{C} = \frac{(I_{in} + I_L) T_{op}}{C} \tag{8.2}$$

Since the average capacitor voltage is equal to the input voltage [3], which can be obtained from input power and current, the minimum V_C can be obtained from (3.2) and (8.2):

$$V_{C\min} = V_{in} - \Delta V_c / 2 = \frac{P}{I_{in}} - \left(\frac{1 - D_{op}}{1 - 2D_{op}} I_{in} T_{op} \middle/ 2C\right) \tag{8.3}$$

Assume the load impedance is Z. From the power balance, the input power can be calculated by output current as:

$$P = \frac{3}{2} Z (\hat{i}_{ac})^2 \cos\phi \tag{8.4}$$

8.4.2. Critical Condition of different shoot through control methods in SPWM method:

For maximum constant boost control, the basic principle is to make the open zero duty cycle constant at the maximum limit of available short zero state period. In order to make the open zero duty ratio constant and maximum, the maximum open zero duty ratio is achieved as:

$$D_{op} = 1 - (\frac{M \sin\theta - M \sin(\theta - \frac{2\pi}{3})}{2})_{\max} = 1 - \frac{\sqrt{3}}{2} M \tag{8.5}$$

, where θ is the phase angle of current vector .The expressions for upper envelope V_p and lower envelope V_n is similar to voltage-fed ZSI which has been derived in paper [5]. (to state this equation here for further references)

Since the basic critical equation for the discontinuous mode is:

$$V_{C\min} \le \frac{V_{l-lpeak}}{2} \tag{8.6}$$

Substitute the derived maximum Dop into the equation for $V_{C\min}$, the critical condition for discontinuous mode can be derived as follows:

$$\frac{3M}{2(\sqrt{3}M - 1)} \cos\phi - \frac{\sqrt{3}}{6} \frac{(2 - \sqrt{3}M)T_S}{CZ} \le 1 \tag{8.7}$$

When this condition is satisfied, the circuit starts to have discontinuous modes.

For constant boost control, the shoot through reference is equal to the modulation index M. The maximum open zero duty cycle is (1-M). Thus the critical condition can be expressed as:

$$\frac{3M}{2(2M - 1)} - \frac{2(1 - M)T_S}{3ZC} \le 1 \tag{8.8}$$

For maximum boost control, D_{op} is maximum available open zero duty cycle at any moment, which varies with phase angle:

$$D_{op} = 1 - (\frac{M \sin\theta - M \sin(\theta - \frac{2\pi}{3})}{2}) \tag{8.9}$$

But its average value is a constant value, which can also be taken to calculate the critical condition:

$$\overline{D_{op}} = \frac{\int_0^{\pi/3} 1-(\frac{M\sin\theta - M\sin(\theta-\frac{2\pi}{3})}{2})}{\pi/3} = 1-\frac{3\sqrt{3}M}{2\pi} \tag{8.10}$$

Together with the voltage gain equation, the critical condition of discontinuous mode for maximum boost control is:

$$\frac{3M\pi}{2(3\sqrt{3}M-\pi)}\cos\phi - \frac{\sqrt{3}(2\pi-3\sqrt{3}M)}{2\pi^2}\frac{T_s}{CZ} \le 1 \tag{8.11}$$

8.4.3. Critical condition for SVPWM method

The best operation point for voltage boost mode is when $D_{op}=0$, which is same as traditional CSI; and the best operation point for voltage buck mode is when $D_{op}=1-D_A$, which means turning all the short zero state into open zero state at a fixed modulation index [3]. The instantaneous D_{op} varies with time, but the average duty ratio in each sector is constant. In order to keep D_{op} a constant value during a whole switching cycle to reduce the output harmonics and switching current stress, the average D_{op} is used. So the short zero state still exists with open zero state. The average D_{op} can be calculated through integrating and averaging in one 60^0 sector:

$$D_{op} = \int_0^{\frac{\pi}{3}} (1-\frac{\sqrt{3}}{2}M\sin(\frac{\pi}{3}+\theta))d\theta \Big/ \frac{\pi}{3} = 1-\frac{3\sqrt{3}}{2\pi}M \tag{8.12}$$

In order to achieve least switching times[3], choose the time sequence of the PWM in SVPWM control in voltage buck mode is as following: T_{op}, T_1, T_2, T_{sh}. The CVM and DVM condition are shown in Figure 8.4 (c). The critical condition for SVPWM control can be obtained from (8.3), (8.6) and (8.12) as follows:

$$\begin{cases} \dfrac{3}{2}\dfrac{\cos\phi}{\dfrac{3\sqrt{3}}{\pi}M-1}<1 & \text{Voltage boost mode} \\ \dfrac{3}{2}\dfrac{M}{\dfrac{6}{\pi}M-\dfrac{2}{\sqrt{3}}}\cos\phi-\dfrac{1-\dfrac{3\sqrt{3}}{2\pi}M}{\pi}\dfrac{2T_s}{CZ}<1 & \text{Voltage buck mode} \end{cases} \tag{8.13}$$

Table 8-2.Characteristics of different control strategies

Control strategy	Dop	B	G
Constant Boost	1-M	$\dfrac{1}{2M-1}$	$\dfrac{M}{2M-1}$
Maximum Boost	$1-\dfrac{3\sqrt{3}M}{2\pi}$	$\dfrac{\pi}{3\sqrt{3}M-\pi}$	$\dfrac{\pi M}{3\sqrt{3}M-\pi}$
Maximum constant boost	$1-\dfrac{\sqrt{3}M}{2}$	$\dfrac{1}{\sqrt{3}M-1}$	$\dfrac{M}{\sqrt{3}M-1}$
SVPWM(Buck Mode)	$1-\dfrac{3\sqrt{3}}{2\pi}M$	$\dfrac{\pi}{3\sqrt{3}M-\pi}$	$\dfrac{\pi M}{3\sqrt{3}M-\pi}$
SVPWM(Boost Mode)	0	1	$\dfrac{2\pi}{3\sqrt{3}M}$
Control Strategy	**Is**	**Critical Condition**	
Constant Boost	$\dfrac{1}{2M-1}I_{in}$	$\dfrac{3M}{2(2M-1)}-\dfrac{2(1-M)T_s}{3ZC}\le 1$	
Maximum Boost	$\dfrac{\pi}{3\sqrt{3}M-\pi}I_{in}$	$\dfrac{3M\pi}{2(3\sqrt{3}M-\pi)}\cos\phi-\dfrac{\sqrt{3}(2\pi-3\sqrt{3}M)}{2\pi^2}\dfrac{T_s}{CZ}\le 1$	
Maximum constant boost	$\dfrac{I_{in}}{\sqrt{3}M-1}$	$\dfrac{3M}{2(\sqrt{3}M-1)}\cos\phi-\dfrac{\sqrt{3}(2-\sqrt{3}M)T_s}{6CZ}\le 1$	
SVPWM(Buck Mode)	$\dfrac{\pi I_{in}}{3\sqrt{3}M-\pi}$	$\dfrac{3}{2}\dfrac{\sqrt{3}\pi M}{6\sqrt{3}M-2\pi}\cos\phi-\dfrac{2\pi-3\sqrt{3}M}{2\pi^2}\dfrac{2T_s}{CZ}<1$	
SVPWM(Boost Mode)	Iin	$\dfrac{3}{2}\dfrac{\cos\phi}{3\sqrt{3}M/\pi-1}<1$	

At this point, all the critical conditions for different modulation methods have been derived and listed in Table 8-1.

8.5. Simulation and experimental demonstration

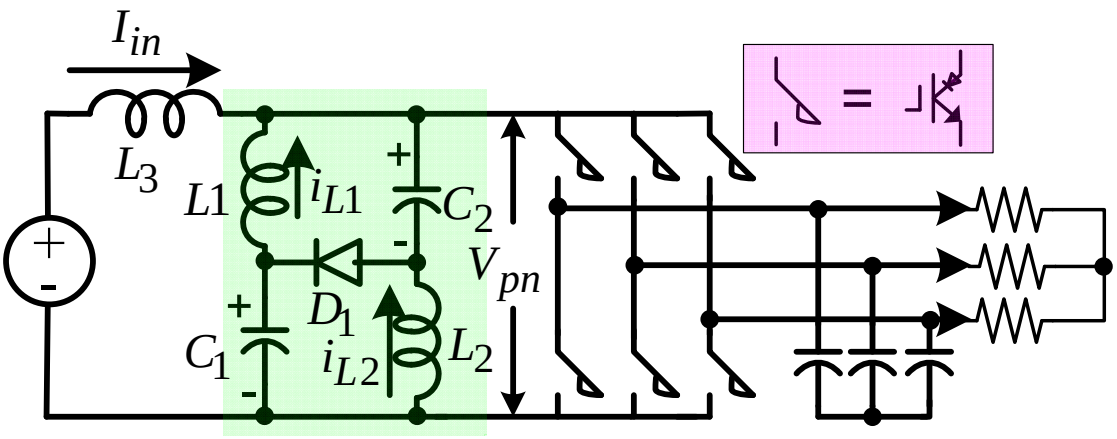


Figure 8.6. The circuit configuration in the experiment

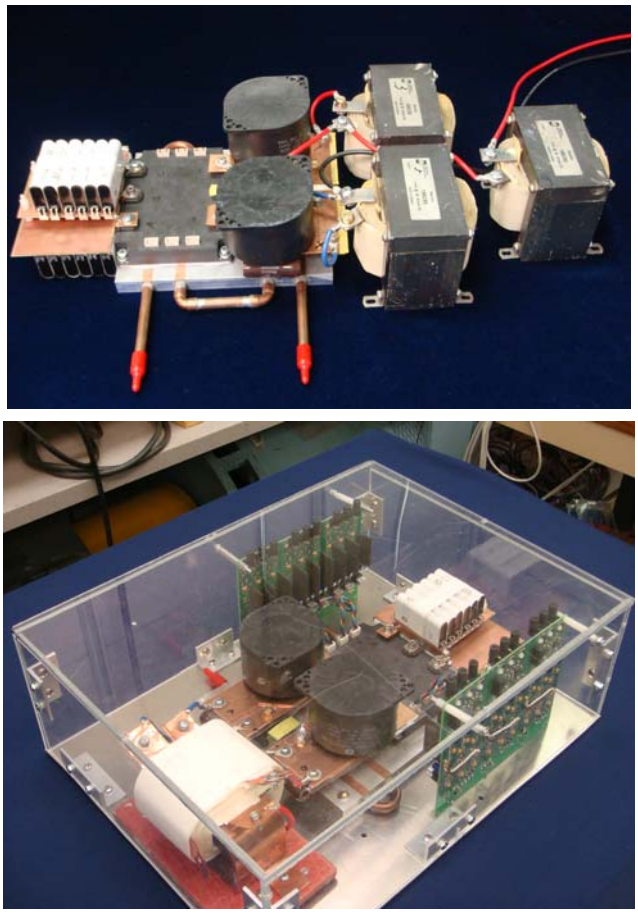
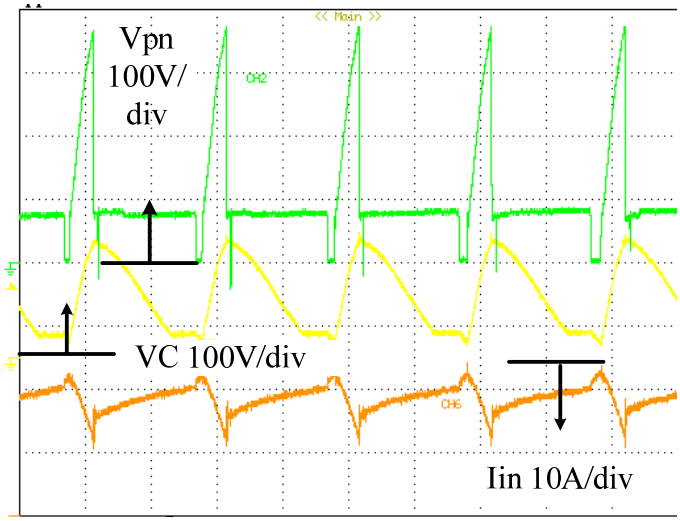
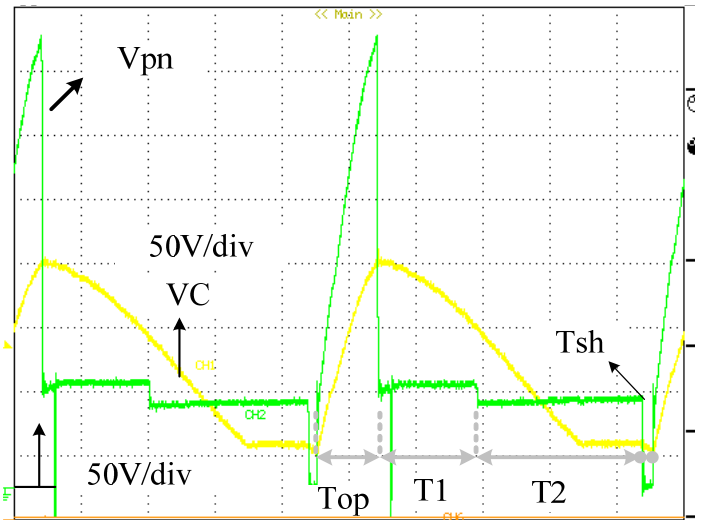


Figure 8.7. (a) First version of 5kW current-fed quasi-Z-source inverter with separate inductors (b) second version of 5kW current-fed quasi-Z-source inverter with coupled inductors.



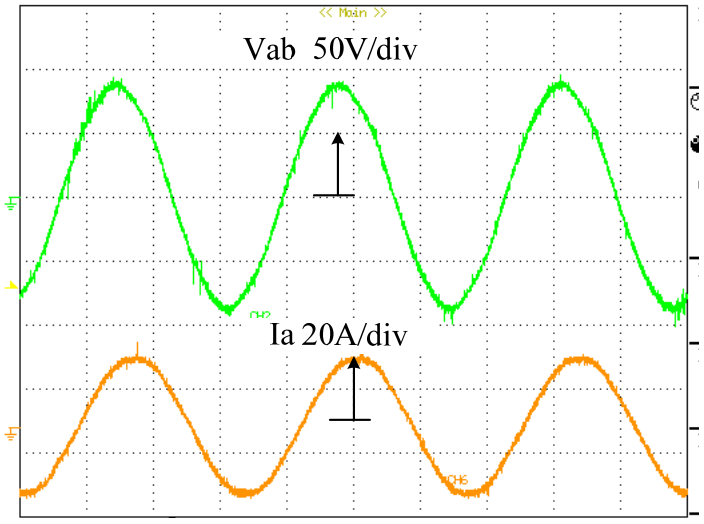
(a) From the top to bottom: device voltage stress, dc capacitor voltage, input current



(b) From the top to bottom: device voltage stress, dc capacitor voltage (Zoomed in)

Figure 8.8. Experimental results of the CVM condition under SVPWM control for voltage buck operation (Vpn: DC link voltage across the inverter bridge; Vc: qZ-network capacitor voltage; Iin: input inductor current; Vab: load line to line voltage; Ia: load phase current)

Figure 8.8 (cont'd)



(c) From the top to bottom: output line to line voltage, output phase current

To verify the aforementioned theoretical analysis, a RB-IGBT module based current-fed qZSI prototype has been built in the laboratory with the following parameters: C=1uF, L=1mH, V_{in} =100V, f_s =10kHz, f=60Hz (output frequency), and $Z = 5\Omega$ per phase Y-connection. Experiments of the system using SVPWM control and modulation index of 0.923 are performed. Under these parameters, the system works in CVM condition. Figure 8.8 (a) (b) (c) show the experimental results in voltage buck mode. The open zero duty ratio satisfies equation (8.12), which is set to be 0.19: In Figure 8.8 (a), V_{pn} has four levels: the highest level is equal to two times of the capacitor voltage which happens in open zero states; two output line to line voltage, which happens in active states; and the zero level is corresponding to short zero states. The capacitor voltage increases in open zero state and decreases when it enters into active states; when it decrease to be equal to half of the output line to line voltage, it remains constant until the end of active state; when the short zero state starts, it decreases again until the next switching action. This waveform agrees with theoretical analysis result shown in Figure 8.4 very well. Figure 8.8 (b) is the enlarged

waveform for V_C and V_{pn}. It demonstrates the discontinuous mode 5. The maximum pn voltage is 375V, which is equal to two times of maximum capacitor voltage. It is obvious that the output voltage range becomes smaller than the continuous case because of the high ripple of the capacitor voltage Figure 8.8 (c) shows the output line to line voltage and phase current. The current gain in continuous mode with this parameter should be 1.75. But from the experiment results it can be seen that I_{in} =16.25A and $\hat{i}_{ac}$ =20A; so the current gain becomes $\hat{i}_{ac} / (\sqrt{3} I_{in} / 2) = 1.42$. It shows that the current boost factor in discontinuous mode is lower than in continuous mode with the same modulation index and the same control method, which is because some of the active states become open zero states in discontinuous operation, and make the inductor current decreases more than normal condition.

The System specifications are:

$$L_1 = L_2 = L_3 = 1mH, \quad (Coupled), C_1 = C_2 = 10uF, V_{IN} = 100V,$$
$$f_o = 60Hz, \; f_{sw} = 10kHz, Z = 5\Omega;$$

8.6. Summary

- The discontinuous modes can happen in the condition the capacitance in the quasi-Z network is small or the load power factor is low;
- There are two discontinuous modes except the normal continuous modes;
- The changed variable in discontinuous mode compared to continuous mode is the capacitor voltage; the non-changed variable is the output voltage and current.
- Different control methods can yield different circuit characteristics due to different modulation methods and different switching sequences. The key point to derive the critical condition in order to avoid or utilize this discontinuous mode is to analyze the maximum available open zero duty cycle, since the maximum capacitor voltage

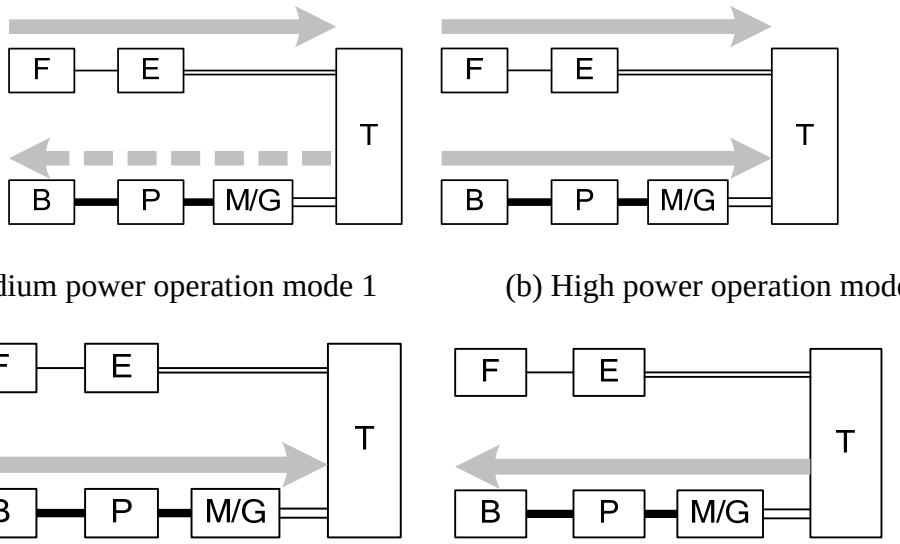
ripple ΔV_C is obtained at maximum open zero duty cycle. The critical condition for discontinuous mode is a function of dc capacitance, modulation index, load power factor, load impedance and switching frequency.

- To be utilized, the discontinuous operation can reduce the requirement for capacitance, thus reduce the system size; in addition, its voltage boost ratio can exceed the limit at 2. However, the capacitor voltage rating and device voltage rating, as well as output voltage harmonics will be increased. From this stand point, this mode should be avoided. One method is to make the parameters not satisfy the critical condition; another method is to replace the diode with an active switch which can be controlled to be turned off at all active states and traditional short zero states.

CHAPTER 9 CIRCUIT MODELING AND TRANSIENT ANALYSIS

9.1. Introduction

In hybrid electrical vehicle (HEV) motor drive, the operation mode changes from motoring to regenerating very frequently, either in decelerating period or braking period. In order to analyze precisely in which condition the motor drive inverter needs to do this transition, the complete operation modes of both parallel HEV and series HEV are illustrated as follows [3].



(a). Medium power operation mode 1 (b) High power operation mode 2

(c)Low power operation mode 3 (d)Regenerative braking operation mode 4

Figure 9.1. Four operation modes of parallel hybrid vehicles (F: Fusion tank; E: Engine; B: Battery; P: Power converter; M: Motor; T: Transmission)

In parallel hybrid vehicle configuration, there are two independent paths connected with transmission line. One path is composed of fuel tank and engine. Another path is composed of battery, power inverter and motor. They both can provide power directly through the transmission line. It has four utilized operating modes [3] shown in Figure 9.1. and outlined in the following:

A. Mode 1, medium power

At medium power, the power of vehicle traction motor is only provided by the engine. And the motor can operate as a generator to charge the battery when its SOC (State Of Charge) is low.

B. Mode 2, high power

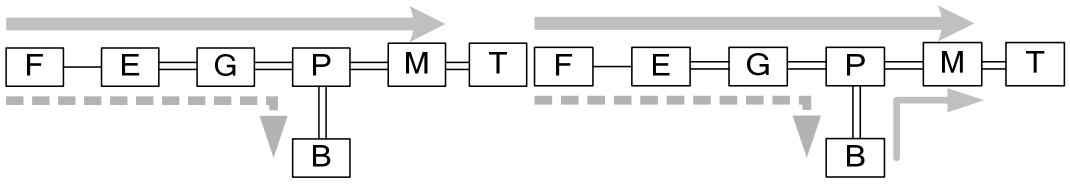
During acceleration, both engine and battery will provide power to the motor. Battery speeds up the vehicle's response time for acceleration and also maintains a safe and efficient operation point for engine.

C. Mode 3, low power

The engine efficiency decreases when operated under low power. So the engine is turned off and the traction motor is only driven by the battery.

D. Mode 4, Regenerative braking

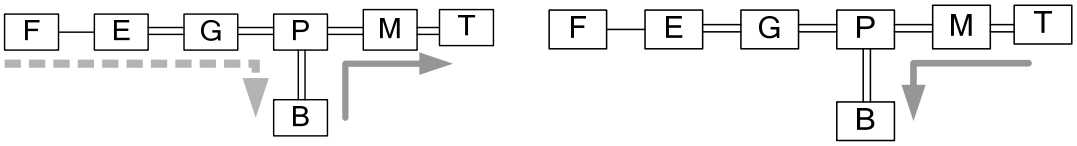
During regenerative braking, the electric motor acts as a generator to generate electric power from the torque of the motor which slows down the vehicle. This electrical energy will be used to charge the battery. Thus the motoring to regenerating transition happens each time when the vehicle switch to either mode A or D.



(a). Medium power operation mode 1 (b) High power operation mode 2

Figure 9.2. Four operation modes of series hybrid vehicles

Figure 9.2 (cont'd)



(c). Low power operation mode 3 (d) Regenerative braking operation

In series hybrid vehicle configuration, both of engine energy and battery energy go through power converter to drive the motor. It also has four utilized operating modes but different with the parallel hybrid vehicle since all the power in battery needs to be provided through power converter, as shown in Figure 9.2 with the following outline:

A. Mode 1, medium power

At medium power, the power of vehicle traction motor is provided by the engine; at the same time the engine needs to provide power through power generator side power converter to charge the battery when its SOC (State Of Charge) is low. At this moment, the generator side power converter operates at regeneration mode.

B. Mode 2, high power

During acceleration, both engine and battery will provide power to the motor. Battery speeds up the vehicle's response time for acceleration and also maintains a safe and efficient operation point for engine. At the same time, the engine will charge the battery when its SOC becomes low.

C. Mode 3, low power

The engine efficiency decreases when operated under low power. So the engine is turned off and the traction motor is only driven by the battery. But at the same time, the engine will charge the battery through converters when the battery's SOC is low.

D. Mode 4, Regenerative braking

During regenerative braking, the electric motor acts as a generator to generate electric power from the torque of the motor which slows down the vehicle. This electrical energy will be used to charge the battery.

To be concluded for series HEV, the transition from motoring to regenerating happens in all four modes when its SOC goes low.

Therefore, a fast transient response is a necessary characteristic that the HEV motor drive converter should possess. The traditional motor drive is implemented by a series boost converter and a voltage source inverter, since the battery voltage is usually only half of the dc link voltage that the inverter needs. A approximate 2 boost ratio is required in the front stage of inverter. It is common sense that this topology can implement the transition from motoring to regenerating very fast, because the transition is presented in the form of input current direction change, which is supposed to be fast in voltage source inverter. Here comes the doubt about current source inverter: the big inductor in the input of current source inverter may cause a much slower response to the current direction change command. If this is a problem, the big inductor in boost converter also causes a slow transition response. If this problem can be overcame by properly designing the inductor and capacitor parameters in the circuit, the same procedure can be conducted for the single-stage current-fed quasi-Z-source inverter.

The structure of this chapter: (1) A state space model has been built for current-fed quasi-Z-source inverter to demonstrate that it has fast transient response that it only needs several switching cycles to transfer from motoring mode to regeneration mode, which makes it very suitable to be used for HEV or EV motor drive. (2) Both abc and dq state space model

is built for current-fed Z-source rectifier to demonstrate its transient performance theoretically. (3) A generalized state space model based on connection matrix has been built for all the topologies in switched-coupled-inductor inverter family, in order to derive all the governing equations including voltage/current gain and voltage/current stress, and also for transient analysis.

9.2. Current-fed quasi-Z-source inverter

9.2.1. Research target

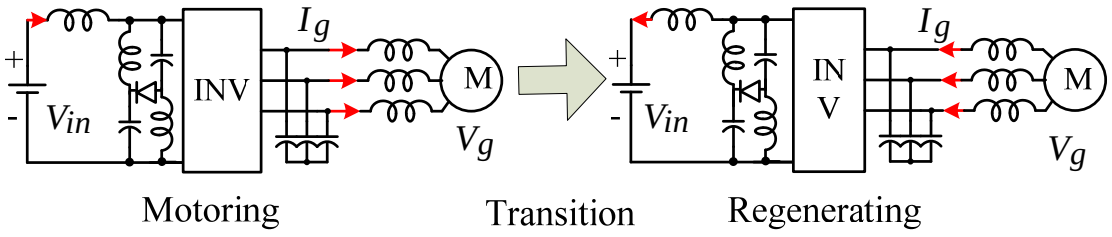
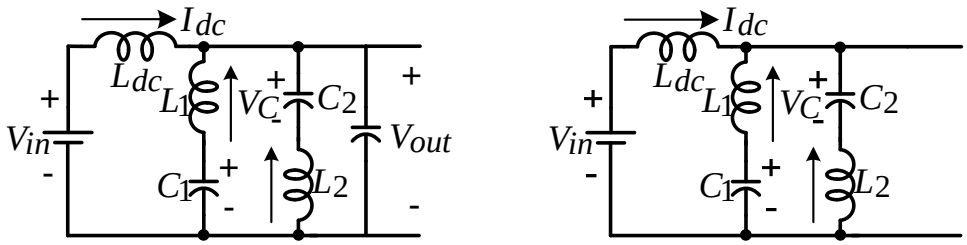


Figure 9.3. Block diagram of transition from motoring mode to regenerating mode

The research target topology is the current-fed quasi-Z-source inverter, which introduces the extra open zero states and makes buck-boost and regeneration capability possible. The plot of its voltage gain versus the active duty cycle D_A has been shown in Figure 3.5. In motoring mode, the maximum voltage gain is 2. But the negative voltage gain in regeneration mode has no such limit. However the 2 boost ratio is enough for the normal design of battery voltage and dc link voltage.

This section concentrates on the transition performance of this inverter from motoring operation mode to regenerating operation mode, which is presented in the form of that the input inductor reverses its current direction, as well as the output inductors, as Figure 9.3 shows. Theoretical model and simulation, experiment demonstrations will be given in the following parts to get the transition time duration for the reverse of input current.

9.2.2. Circuit Modeling



(a) *(1- Dop)* (b) *Dop*

Figure 9.4. Circuit model for two basic circuit states

(a) non-open-zero state (b) open zero state

The mathematical model for this transition can be built to predict the transient performance of the pre-designed circuit, in terms of response time, voltage/current overshoot/undershoot amplitude and phase, rise time, settling time and so on, thus form a design guideline. The transient performance of the circuit can be simplified into the transient waveform of the input current. The basic idea is to obtain the input current waveform in the transition from solving the differential equations. The state average model method is used to solve the equation for the input dc current I_{dc} in the transition. There are two basic circuit states (a) non open-zero state (b) open zero state shown in Figure 9.4. So the general state space equation of this switching mode circuit should have state space averaging method applied. In non open-zero state, the inverter is considered as a voltage source, and in open zero state it is an open circuit. The state average model of this equivalent circuit states are expressed in eq. (9.1):

$$\begin{bmatrix} \frac{dI_L}{dt} \\ \frac{dV_C}{dt} \\ \frac{dI_{dc}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \frac{1-2D_{op}}{L} & 0 \\ \frac{2D_{op}-1}{C} & 0 & \frac{D_{op}}{C} \\ 0 & \frac{-2D_{op}}{L} & \frac{-r}{L} \end{bmatrix} \begin{bmatrix} I_L \\ V_C \\ I_{dc} \end{bmatrix} + \begin{bmatrix} -\frac{V_{out}}{L}(1-D_{op}) \\ 0 \\ \frac{V_{in}-(1-D_{op})V_{out}}{L} \end{bmatrix} \quad (9.1)$$

, where the definitions of the variables are lined out in Figure 9.5 and also the inductance, capacitance satisfy: $L_1 = L_2 = L_{dc} = L, C_1 = C_2 = C$;

There are three differential equations in terms of three variables I_L (Z-network inductor current), V_C (Z-network capacitor voltage) and I_{dc} (Input current). The D_{op} is considered as a constant in every steady-state, which is assigned by the voltage boost ratio requirement and also the best operation point constraint. The only unknown variable here is the average pn voltage in active state V_{out}; however, it can be derived from voltage and the duty cycle function as: $V_{out} = D_a V_{ca} + D_b V_{cb} + D_c V_{cc}$. In order to calculate V_{out}, assume the output capacitor voltage to be sinusoidal function with amplitude V_m as follows:

$$\begin{bmatrix} v_{ca} \\ v_{cb} \\ v_{cc} \end{bmatrix} = \begin{bmatrix} V_m \sin(\omega t) \\ V_m \sin(\omega t - \frac{2\pi}{3}) \\ V_m \sin(\omega t + \frac{2\pi}{3}) \end{bmatrix} \tag{6.2}$$

The duty cycles can also be considered as sinusoidal with amplitude M (modulation index) and angle β with respect to voltage:

$$\begin{bmatrix} D_a \\ D_b \\ D_c \end{bmatrix} = \begin{bmatrix} M \sin(\omega t + \beta) \\ M \sin(\omega t + \beta - \frac{2\pi}{3}) \\ M \sin(\omega t + \beta + \frac{2\pi}{3}) \end{bmatrix} \tag{6.3}$$

, in which $\beta = 0$ for motoring mode, and $\beta = \pi$ for regenerating mode.

Through calculation it is found that the average pn voltage in active state is a constant value:

$$V_{out} = \frac{3}{2} M' V_m \tag{6.4}$$

,where $M' = M$ for motoring mode and $M' = -M$ for regenerating mode. So the final simplified equation with all variables known except the ones that is going to be solved is:

$$\begin{bmatrix} \frac{dI_L}{dt} \\ \frac{dV_C}{dt} \\ \frac{dI_{dc}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \frac{1-2D_{op}}{L} & 0 \\ \frac{2D_{op}-1}{C} & 0 & \frac{D_{op}}{C} \\ 0 & \frac{-2D_{op}}{L} & \frac{-r}{L} \end{bmatrix} \begin{bmatrix} I_L \\ V_C \\ I_{dc} \end{bmatrix} + \begin{bmatrix} -\frac{\frac{3}{2}M'V_m}{L}(1-D_{op}) \\ 0 \\ \frac{V_{in}-(1-D_{op})\frac{3}{2}M'V_m}{L} \end{bmatrix} \quad (6.5)$$

To be concluded, the state space average mode of this circuit in motoring and regenerating mode is shown in equation (6.5), with *M'=M* in motoring mode and *M'=-M* in regenerating mode. The next step is to solve the input current I_{dc} from this equation.

9.2.3. Initial conditions and steady state conditions

The transition process is simulated by connecting the current-fed quasi-Z-source inverter to the grid at the output side. The grid current is the control object. The motoring operation is equivalent to inject current to the grid, and the regenerating operation is equivalent to absorb current from the grid. The transition between the two starts from grid current control command change, and ends up with the output phase current and input inductor current reach a steady state with negative direction. Figure 9.5. shows the circuit configuration to demonstrate the transition performance. The current-fed quasi-z-source inverter is supplied by the dc source generated by the rectified grid voltage, and the inverter output is connected to grid to supply a constant current. An important note here is a resistor has to be connected in parallel with the dc link capacitor, to provide an energy consumption path for regeneration mode. Otherwise, the capacitor will be charged up continuously since the diode rectifier can

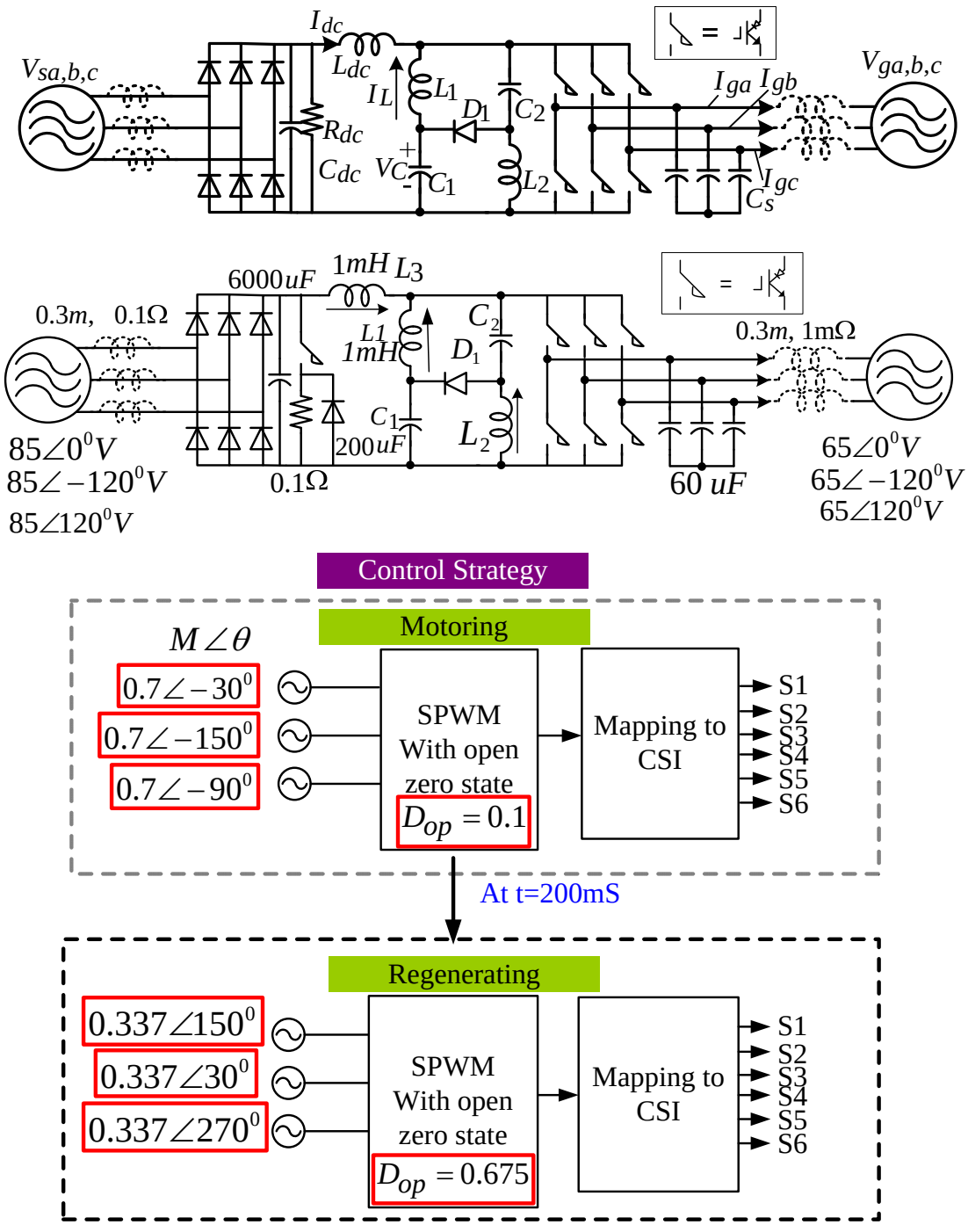


Figure 9.5. Circuit configuration to monitor the transition process

not send the energy back to the input side. This circuit configuration actually is also similar to the series hybrid vehicle motor drive system, in which the input voltage is its generator and the output voltage is its traction motor.

To simulate the transition process, the grid current I_{ga} command is changed from $18\angle 0^0 A$

to $18\angle 180^0 A$ (0 degree means the current is in phase with the grid voltage and 180 degrees means the current is out of phase with the grid voltage), so as the command of phase b and c, at the time of t=0.2s. The mathematical model for the transition has been built to calculate the transition time for the mode change. The reason to build this mathematics model is to form a pre-design guide line for the system. The transition time is defined by the time that the input dc current changes from positive direction steady-state to negative direction steady-state here.

When the circuit mode changes from motoring to regenerating, the transient response of the output line current has the linear relationship with the input dc inductor current. If the input current can reverse its direction fast, the output current can also change its phase from 0 degree to 180 degree in a short time. The transient expression for the input dc inductor current as a function of time can be derived using the state space average model in equation (5).

From *t=0s*, the circuit works in motoring mode and the grid current command is $I_{gref} = 18\angle 0^0 A$, which is in phase with the grid voltage. At *t=200ms*, the current command changes to $I_{gref} = 18\angle 180^0 A$, which is out of phase with grid voltage. The circuit is changed to regeneration mode. The direct command change according to the voltage and current ratio equation of this circuit, is: the modulation index and open zero duty cycle change from [0.65, 0.3] to [0.25, 0.6].

The initial conditions of the system are:

$$I_L(0^-) = I_L(0^+) = 0; V_C(0^+) = V_C(0^-) = V_{in} = 100V; I_{dc}(0^+) = I_{dc}(0^-) = 30A; V_m = 85V$$
$$M(0^-) = 0.65, D_{op}(0^-) = 0.03; M(0^+) = -0.25, D_{op}(0^+) = 0.6$$

And the parameters are: L=1mH, r=0.7, C=200uF;

9.2.4. Solution for input current

Simplify the differential equation into the single equation about *Idc* as the following third order differential equation:

$$\frac{1}{-1.2e006} I_{dc}'''(t) - \frac{7}{1.2e004} I_{dc}''(t) - \frac{19}{6} I_{dc}'(t) - \frac{1400}{12} I_{dc}(t) + 6050 = 0 \tag{6.6}$$

The characteristic equation of this time domain differential equation is:

$$s^3 + 700s^2 + 19*1.2e006/6 \cdot s + 1400*1.2e006/12 = 0 \tag{6.7}$$

And the roots are $s_1 = -37; \quad s_2 = -331 + j1915; \quad s_3 = -331 - j1915$

Solve the equation with the following initial and steady-state conditions:

$$I_{dc}(0^+) = 30A; I_{dc}(\infty) = -8.3A; I_{dc}'(0^+) = 132$$

Thus the final solution is：

$$I_{dc}(t) = -3.79e^{-37t} + 42.19e^{-331t}\sin(1915t + 1.4) - 8.4 \tag{6.8}$$

Plot the $I_{dc}(t)$ in Figure 9.5. It is shown that the transition time from motoring to regenerating $t_T = 1ms$, which is 10 switching cycles in this case (*fsw=10kHz*).

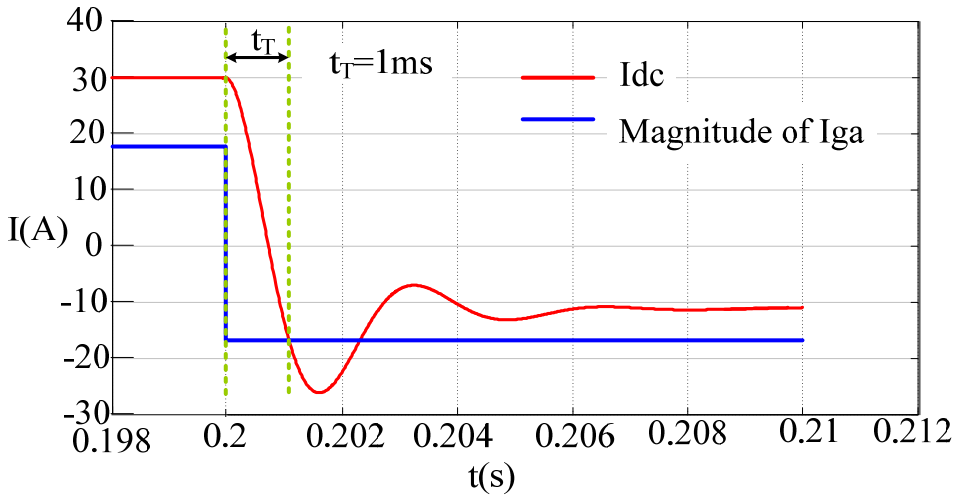


Figure 9.6. Calculated input current waveform in transition starting at t=0.2s

9.2.5. Simulation and experiment demonstration

In order to verify the theory analysis, the circuit in Figure 9.5 has been simulated with the following parameters:

$L_{dc} = 1m, r_{dc} = 0.7\Omega, C_{dc} = 12000uF, R_{dc} = 4.12\Omega; C_1 = C_2 = 200uF, L_1 = L_2 = 1mH$

$C_S = 60uF; L_g = 0.3mH, r_g = 10m\Omega, V_{ga} = 85\angle 0^0 V; R_S = 0.3m, r_S = 0.1m\Omega, V_{sa} = 63\angle 0^0 V.$ Mode changes from motoring to regeneration at t=200ms.

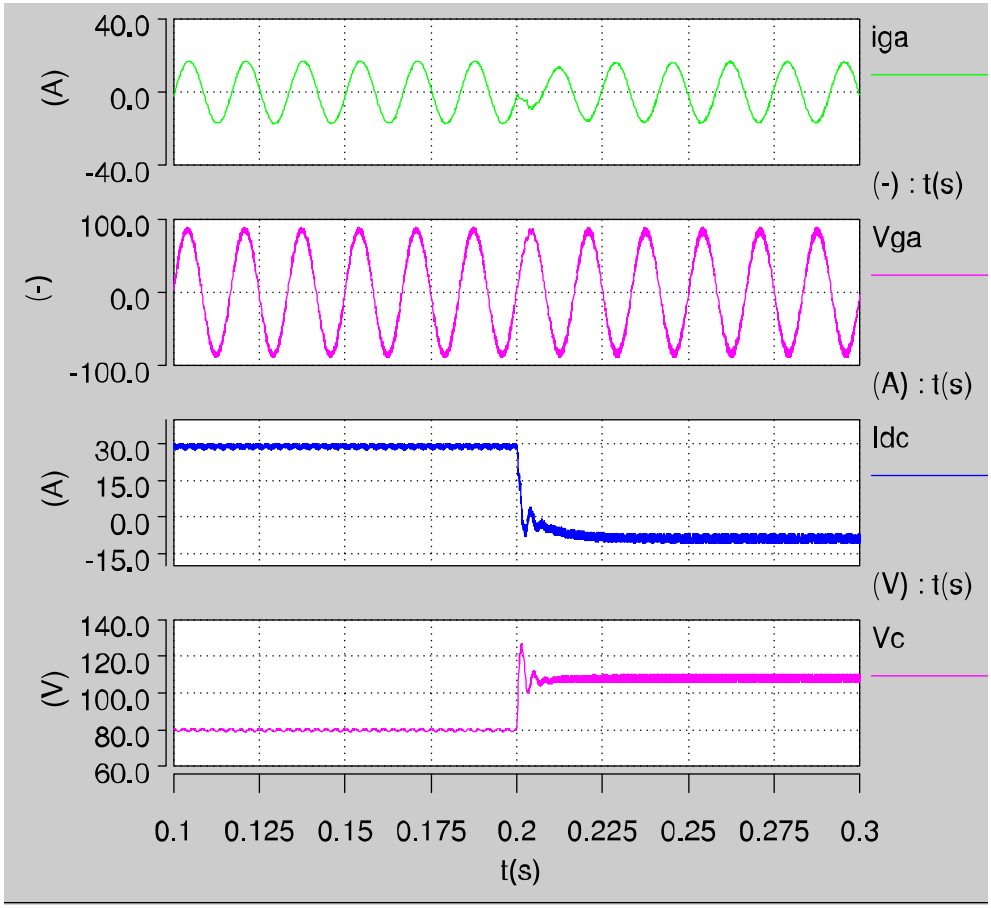


Figure 9.7. (a)Simulation results (1) Output phase A Current (2) output phase A Voltage (3) input inductor current (4) Z-source capacitor voltage in motoring to regeneration transition (at t=0.2s) (b) Zoom in results of (a)

Figure 9.7 (cont'd)

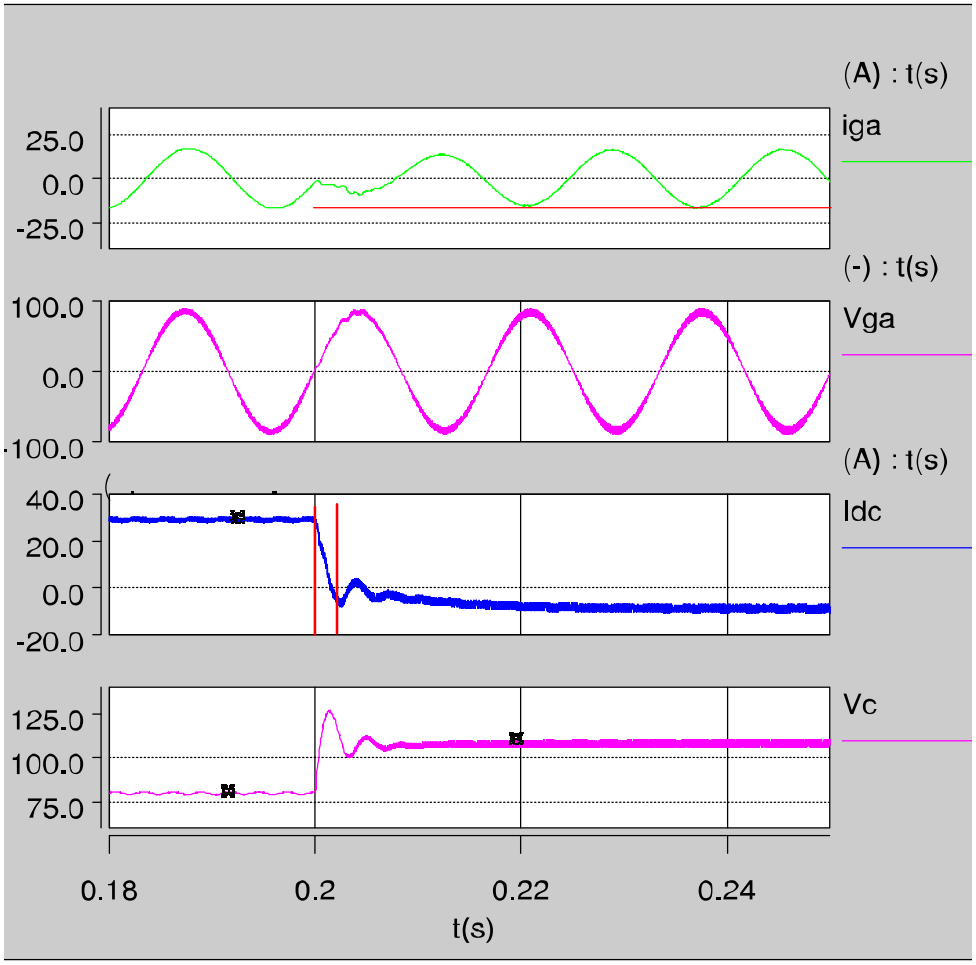


Figure 9.7. (a)Simulation results (1) Output phase A Current (2) output phase A Voltage (3) input inductor current (4) Z-source capacitor voltage in motoring to regeneration transition (at t=0.2s) (b) Zoom in results of (a)

The simulation results are shown in Figure 9.7. The mode changes from motoring to regenerating happens at t=200ms. The measured other variables changes are shown in Table 9.1:

Table 9-1. Simulation results in mode change transition

	Ioa(A)	Idc(A)	Vin(V)	M	Dop	transition time(s)
Motoring	18∠0	30	89	0.65	0.25	0.00109
Regenerating	18∠180	-14	103.89	0.03	0.6	

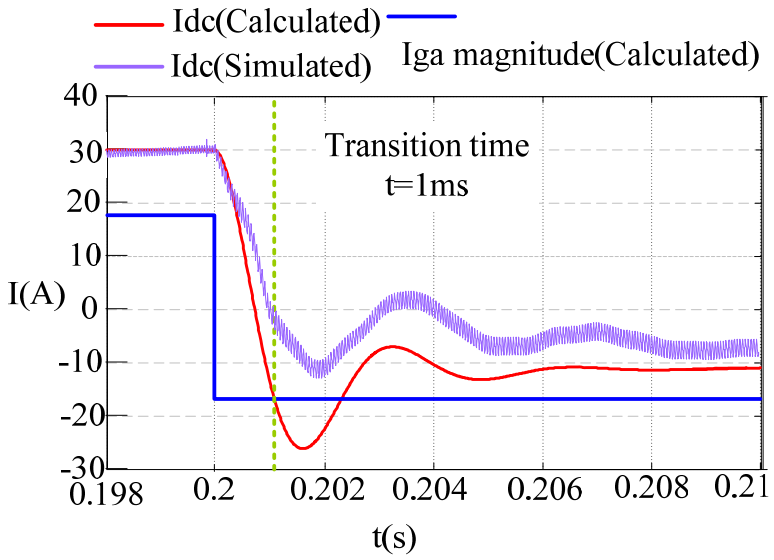


Figure 9.8. Comparison between calculated Idc and simulated Idc

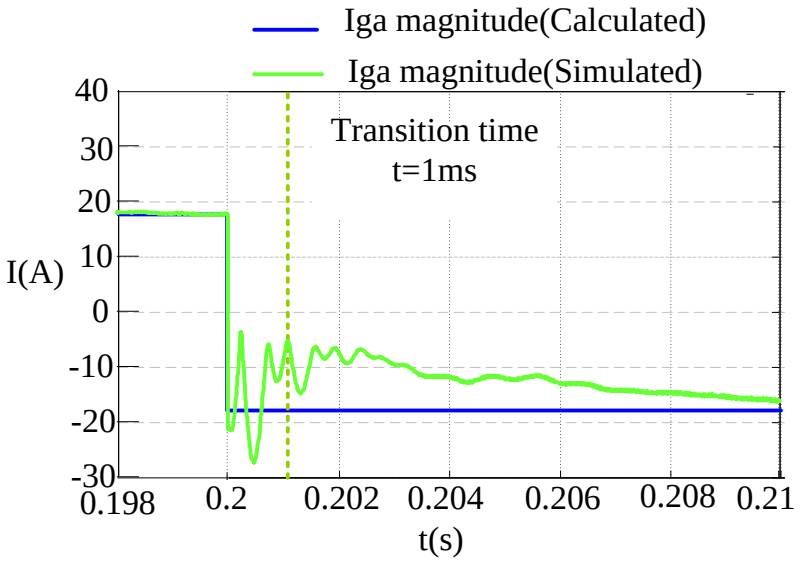


Figure 9.9. Comparison between calculated *Iga* amplitude and simulated *Iga* amplitude

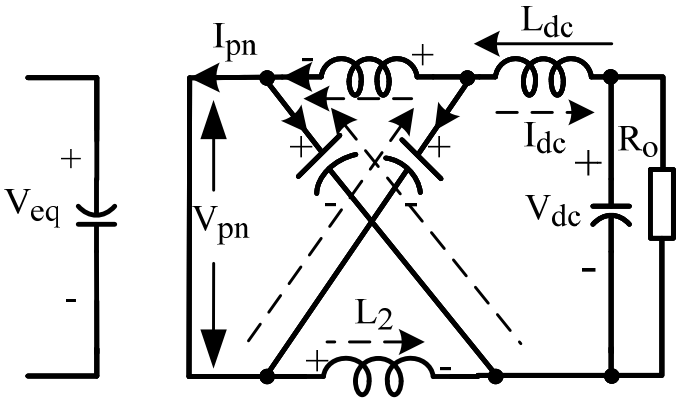
The simulation demonstrates that the transition time is around 10 switching cycles. The comparisons between calculated results in section I and the simulation results are shown in Figure 9.8. and Figure 9.9. It can be seen that the simulation results match with the theory equation (6.8) quite well. And the transition time from motoring to regenerating is about 10 switching cycles. The exact number of switching cycles that the transition requires is not a fixed one but not very different for different cases.

9.2.6. Conclusion

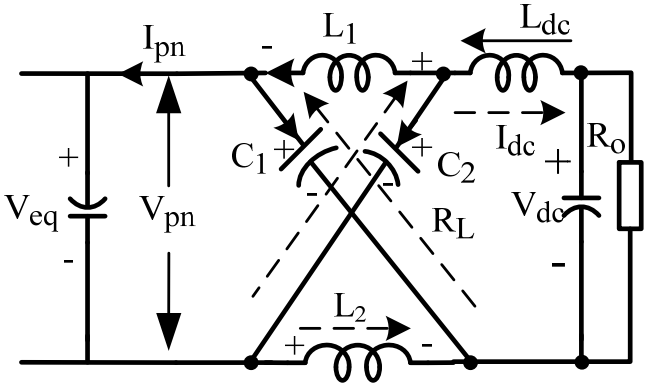
The current-fed quasi-Z-source inverter exhibit a fast transient response when its operation mode changes from motoring to regenerating. It only needs several switching cycles to reach a steady state. This feature makes it suitable for HEV/EV application. The large signal state-space average model effectively estimates the transient.

9.3. Three phase current-fed Z-source PWM rectifier

9.3.1. PWM rectifier state space model



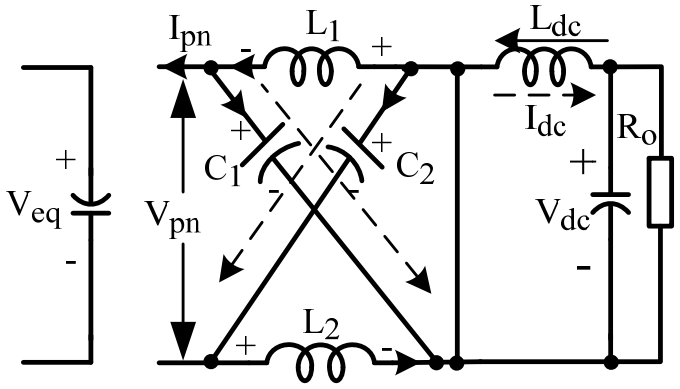
(a). State I – Short Zero: D_{sh}



(b). State II—Active: D_A

Figure 9.10.Operation states of current-fed Z-source PWM rectifier

Figure 9.10 (cont'd)



(c). State III—Open Zero: D_{op}

The equivalent circuit of modeling for current-fed Z-source rectifier has been shown in Figure 9.10 and all the variables are defined. The switching function of a switch in Figure 9.10 is defined as

$$S_i(t) = \begin{cases} 1, \textit{switch closed} & i \in \{a,b,c\} \\ 0, \textit{switch open} \end{cases} \tag{6.9}$$

If the switching frequency is much higher than the utility frequency, the switching function S_i can be replaced by its average value in non-open zero state of one switching period. The three-phase source voltages and the average switching function for each leg of the converter D_n $(n = a,b,c)$ in non-open zero state are defined in (9.10).

$$\begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} = \begin{bmatrix} V_m \sin(\omega t) \\ V_m \sin(\omega t - \frac{2\pi}{3}) \\ V_m \sin(\omega t + \frac{2\pi}{3}) \end{bmatrix}; \begin{bmatrix} D_a \\ D_b \\ D_c \end{bmatrix} = \begin{bmatrix} D_m \sin(\omega t + \beta) \\ D_m \sin(\omega t - \frac{2\pi}{3} + \beta) \\ D_m \sin(\omega t + \frac{2\pi}{3} + \beta) \end{bmatrix} \tag{6.10}$$

,where β stands for the angle between input current and phase voltage. From Figure 9.10, the input currents satisfy:

$$\frac{d}{dt}i_{1,2,3} = -\frac{r}{L_s}i_{1,2,3} - \frac{1}{L_s}v_{C1,2,3} + \frac{v_{a,b,c}}{L_s} \tag{6.11}$$

While in non-open zero state,

$$I_{pn} = 2I_L - I_{dc} = \frac{1}{1-2D_{op}}I_{dc} \tag{6.12}$$

So the overall equation for capacitor voltage in non-open zero state and open zero state can be derived as:

$$\frac{d}{dt}v_{C1,2,3} = (1-D_{op})(\frac{i_{1,2,3}}{C_s} + \frac{i_{pn}D_{a,b,c}}{C_s}) + D_{op}\frac{i_{1,2,3}}{C_s} = \frac{i_{1,2,3} + D_{a,b,c}\frac{(1-D_{op})}{1-2D_{op}}I_{dc}}{C_s}$$

(6.13)

For dc output voltage and current, one has :

$$\begin{aligned} \frac{d}{dt}I_{dc} &= \frac{V_{dc}}{L_{dc}} - \frac{r_{dc}I_{dc}}{L_{dc}} - \frac{V_D}{L_{dc}} \\ \frac{d}{dt}V_{dc} &= -\frac{I_{dc}}{C_{dc}} - \frac{V_{dc}}{C_{dc}R_0} \end{aligned} \tag{6.14}$$

The dc link voltage V_{pn} has different expressions in open zero state and non-open zero state:

$$V_{pn} = \begin{cases} -D_a v_{C1} - D_b v_{C2} - D_C v_{C3} & non-open\ zero\ state \\ 2V_{dc} & open\ zero\ state \end{cases} \tag{6.15}$$

The average value for V_{pn} is

$$V_{pn} = (1-D_{op})(-D_a v_{C1} - D_b v_{C2} - D_c v_{C3}) + D_{op} \cdot 2V_{dc} \tag{6.16}$$

In Z-network, $V_{pn} = V_C - V_L$ and $V_D = V_C + V_L$

So

$$V_D = 2V_C - V_{pn} == (1-D_{op})(D_a v_{C1} + D_b v_{C2} + D_C v_{C3} + 2V_{dc}) \tag{6.17}$$

9.3.2. Z-Source network state space model

From equivalent circuit for Z-network in Figure 9.10, one has:

In non-open zero state $(1-D_{op})$,

$$\begin{pmatrix} \frac{d}{dt}I_L \\ \frac{d}{dt}V_C \end{pmatrix} = \begin{pmatrix} 0 & \frac{1}{L} \\ -\frac{1}{C} & 0 \end{pmatrix} \begin{pmatrix} I_L \\ V_C \end{pmatrix} + \begin{pmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{pmatrix} \begin{pmatrix} I_{dc} \\ V_{pn} \end{pmatrix} \tag{6.18}$$

In open zero state D_{op},

$$\begin{pmatrix} \frac{d}{dt}I_L \\ \frac{d}{dt}V_C \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{pmatrix} \begin{pmatrix} I_L \\ V_C \end{pmatrix} + \begin{pmatrix} 0 & 0 \\ 0 & 0 \end{pmatrix} \begin{pmatrix} I_{dc} \\ V_{pn} \end{pmatrix} \tag{6.19}$$

So the overall state space equations for Z-network is

$$\begin{pmatrix} \frac{d}{dt}I_L \\ \frac{d}{dt}V_C \end{pmatrix} = \begin{pmatrix} 0 & \frac{1-2D_{op}}{L} \\ \frac{2D_{op}-1}{C} & 0 \end{pmatrix} \begin{pmatrix} I_L \\ V_C \end{pmatrix} + \begin{pmatrix} 0 & \frac{D_{op}-1}{L} \\ \frac{1-D_{op}}{C} & 0 \end{pmatrix} \begin{pmatrix} I_{dc} \\ V_{pn} \end{pmatrix} \tag{6.20}$$

9.3.3. Current-fed Z-source rectifier dq state space model

From Figure 9.10 and equations (6.9)-(6.20), the state model of current-fed Z-source rectifier can be obtained. It is a time varying three phase system because of the average switching functions; however, it can be converted into a rotating synchronous frame (d-q-0) using Park transformation, and the transformed matrix is shown in (6.21).

$$\begin{bmatrix} \frac{di_d}{dt} \\ \frac{di_q}{dt} \\ \frac{dV_{cd}}{dt} \\ \frac{dV_{cq}}{dt} \\ \frac{dI_{dc}}{dt} \\ \frac{dV_{dc}}{dt} \\ \frac{dI_L}{dt} \\ \frac{dV_C}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{r}{L_s} & \omega & -\frac{1}{L_s} & 0 & 0 & 0 & 0 & 0 \\ -\omega & -\frac{r}{L_s} & 0 & -\frac{1}{L_s} & 0 & 0 & 0 & 0 \\ \frac{1}{C_s} & 0 & 0 & \omega & \frac{D_d(1-D_{op})}{C_s(1-2D_{op})} & 0 & 0 & 0 \\ 0 & \frac{1}{C_s} & -\omega & 0 & \frac{D_q(1-D_{op})}{C_s(1-2D_{op})} & 0 & 0 & 0 \\ 0 & 0 & -\frac{D_d(1-D_{op})}{L_{dc}} & \frac{-D_q(1-D_{op})}{L_{dc}} & \frac{-r_{dc}}{L_{dc}} & \frac{2D_{op}-1}{L_{dc}} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{C_{dc}} & -\frac{1}{C_{dc}R_0} & 0 & 0 \\ 0 & 0 & \frac{1-D_{op}}{L}D_d & \frac{1-D_{op}}{L}D_q & 0 & 0 & 0 & \frac{1-2D_{op}}{L} \\ 0 & 0 & 0 & 0 & \frac{1-D_{op}}{C} & 0 & \frac{2D_{op}-1}{C} & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ V_{cd} \\ V_{cq} \\ I_{dc} \\ V_{dc} \\ I_L \\ V_C \end{bmatrix} + \begin{bmatrix} \frac{v_{sd}}{L_s} \\ \frac{v_{sq}}{L_s} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{6.21}$$

The equivalent duty ratios in the d-q domain can be obtained form the Park' transformations as given below:

$$\begin{bmatrix} d_q \\ d_d \end{bmatrix} = \begin{bmatrix} \frac{1}{2} m \cos\beta \\ \frac{1}{2} m \sin\beta \end{bmatrix} \tag{6.22}$$

The obtained model is a non-linear time invariant system. Small signal linearization around its DC operating point can be done by assuming that:

$$\begin{aligned} &i_d = I_d + \hat{i}_d, i_q = I_q + \hat{i}_q, v_{Cd} = V_{Cd} + \hat{v}_{Cd}, v_{Cq} = V_{Cq} + \hat{v}_{Cq}, \\ &i_{dc} = I_{dc} + \hat{I}_{dc}, v_{dc} = V_{dc} + \hat{v}_{dc}, v_C = V_C + \hat{v}_C, i_L = I_L + \hat{i}_L; \\ &d_{op} = D_{op} + \hat{d}_{op}, d_d = D_d + \hat{d}_d, d_q = D_q + \hat{d}_q \end{aligned} \tag{6.23}$$

By substituting these equations into (6.21) and separating steady state components from dynamic variables, the small signal AC model can be obtained in equation (6.24).

$$
\begin{bmatrix} \frac{d}{dt}\hat{i}_d \\ \frac{d}{dt}\hat{i}_q \\ \frac{d}{dt}\hat{v}_{cd} \\ \frac{d}{dt}\hat{v}_{cq} \\ \frac{d}{dt}\hat{i}_{dc} \\ \frac{d}{dt}\hat{v}_{dc} \\ \frac{d}{dt}\hat{i}_L \\ \frac{d}{dt}\hat{v}_C \end{bmatrix} = \begin{bmatrix} -\frac{r}{L_s} & \omega & -\frac{1}{L_s} & 0 & 0 & 0 & 0 & 0 \\ -\omega & -\frac{r}{L_s} & 0 & -\frac{1}{L_s} & 0 & 0 & 0 & 0 \\ \frac{1}{C_s} & 0 & 0 & \omega & \frac{D_d(1-D_{op})}{C_s(1-2D_{op})} & 0 & 0 & 0 \\ 0 & \frac{1}{C_s} & -\omega & 0 & \frac{D_q(1-D_{op})}{C_s(1-2D_{op})} & 0 & 0 & 0 \\ 0 & 0 & -\frac{D_d(1-D_{op})}{L_{dc}} & -\frac{D_q(1-D_{op})}{L_{dc}} & -\frac{r_{dc}}{L_{dc}} & \frac{2D_{op}-1}{L_{dc}} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{C_{dc}} & -\frac{1}{C_{dc}R_0} & 0 & 0 \\ 0 & 0 & \frac{1-D_{op}}{L}D_d & \frac{1-D_{op}}{L}D_q & 0 & 0 & 0 & \frac{1-2D_{op}}{L} \\ 0 & 0 & 0 & 0 & \frac{1-D_{op}}{C} & 0 & \frac{2D_{op}-1}{C} & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_d \\ \hat{i}_q \\ \hat{v}_{cd} \\ \hat{v}_{cq} \\ \hat{i}_{dc} \\ \hat{v}_{dc} \\ \hat{i}_L \\ \hat{v}_C \end{bmatrix}
$$

$$
+ \begin{pmatrix} 0 & 0 \\ 0 & 0 \\ \frac{I_{dc}(1-D_{op})}{C_s(1-2D_{op})} & 0 \\ 0 & \frac{I_{dc}(1-D_{op})}{C_s(1-2D_{op})} \\ \frac{-V_{Cd}(1-D_{op})}{L_{dc}} & \frac{-V_{Cq}(1-D_{op})}{L_{dc}} \\ 0 & 0 \\ \frac{1-D_{op}}{L}V_{Cd} & \frac{1-D_{op}}{L}V_{Cq} \\ 0 & 0 \end{pmatrix} \begin{pmatrix} \hat{d}_d \\ \hat{d}_q \end{pmatrix} + \begin{pmatrix} 0 \\ 0 \\ \frac{D_d I_{dc}}{C_s}\left(\frac{1}{2}+\frac{1}{4}\frac{1}{(D_{op}-\frac{1}{2})^2}\right) \\ \frac{D_q I_{dc}}{C_s}\left(\frac{1}{2}+\frac{1}{4}\frac{1}{(D_{op}-\frac{1}{2})^2}\right) \\ \frac{D_d}{L_{dc}}V_{Cd}+\frac{D_q}{L_{dc}}V_{Cq}+\frac{2}{L_{dc}}V_{dc} \\ 0 \\ \frac{-D_d V_{Cd}-D_q V_{Cq}-2V_C}{L} \\ \frac{-I_{dc}+2I_L}{C} \end{pmatrix} \hat{d}_{0p} + \begin{bmatrix} \frac{\hat{v}_{sd}}{L_s} \\ \frac{\hat{v}_{sq}}{L_s} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{9.24}
$$

9.3.4. Initial conditions and steady state conditions

The steady state operating point affects the dynamic response and it can be obtained from solving the state space equation (6.21). Assume that the position of q axis is the same as the ac side capacitor voltage space vector, which makes $V_{Cd}=0$, so the solution can be

further simplified into:

$$V_{dc} = \frac{D_q R_0 (2D_{op} - 1)(1 - D_{op})(\omega L_s V_{sd} - r V_{sq})}{(r^2 {D_q}^2 + \omega^2 {D_q}^2 {L_s}^2)(1 - D_{op})^2 - r R_0 (1 - 2D_{op})^2} \tag{6.25}$$

$$V_{cq} = \frac{V_{dc}(2D_{op} - 1)}{D_q (1 - D_{op})} \tag{6.26}$$

$$I_L = \frac{I_{dc}(1 - D_{op})}{(1 - 2D_{op})} = \frac{V_{dc}(1 - D_{op})}{-R_0 (1 - 2D_{op})} \tag{6.27}$$

$$V_c = \frac{(1 - D_{op}) D_q V_{cq}}{2D_{op} - 1} = V_{dc} \tag{6.28}$$

, which are coincident with the circuit analysis in section III. From (44), due to the limit of voltage step down operation, i.e. the highest output voltage is determined by the maximum value of D_q, which is 0.5 from (38). Therefore the maximum output to input voltage conversion ratio for a given open zero duty cycle is given as: $\frac{V_{dc}}{V_{cq}} = \frac{D_q (1 - D_{op})}{2D_{op} - 1} = \frac{(1 - D_{op})}{2(2D_{op} - 1)}$, which is coincident with (3.23).

9.3.5. Initial conditions and steady state conditions

Small-signal frequency analysis has been carried out to determine how certain rectifier state variables vary with input variables within a given frequency range. The general model for DC side variables can be obtained from the lower four rows of equation (6.24).

The transfer function of $\hat{V}_C / \hat{d}_{op}$ can be obtained as follows:

$$G_1 = \frac{\hat{V}_C(s)}{\hat{d}_{op}(s)} = \frac{(2D_{op} - 1)(V_{cq} - 2V_C) + sL(2I_L - I_{dc})}{s^2 LC + 4{D_{op}}^2 - 4D_{op} + 1} \tag{6.29}$$

Dynamic response is shown in Figure 9.11 for the operation condition

$V_{cq} = 64V, m = 0.4, L = 2mH, C = 200uF, D_{op} = 0.65, V_C = V_{dc} \approx 85V, I_L = 9.5A, I_{dc} \approx -8A;$

Based on this dynamic response, the closed loop controllers are adjusted for required bandwidth and phase margin. The details of the controller design will not be discussed here.

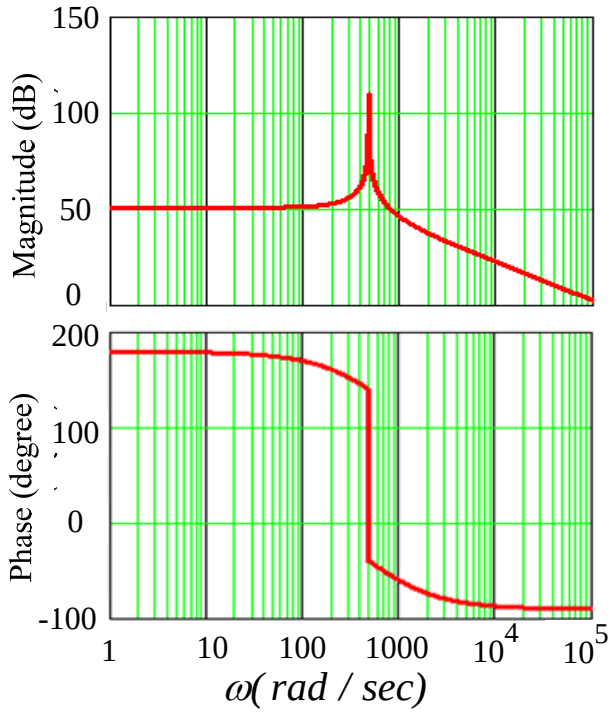


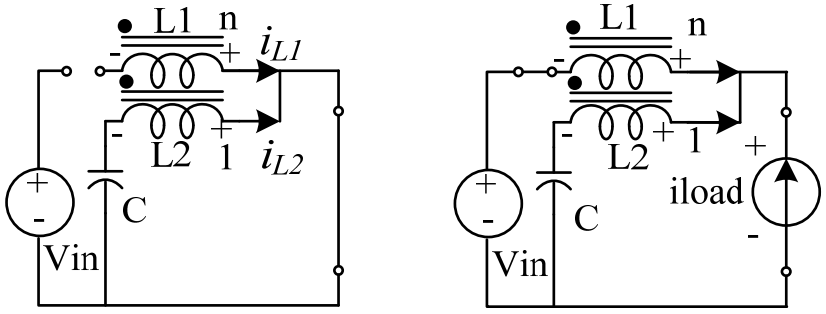
Figure 9.11 Frequency response of the transfer function of $\hat{V}_C / \hat{d}_{op}$

9.4. Switched-coupled-inductor inverter

9.4.1. Steady state analysis for voltage-fed topology

Take VF-SCII 2 as the representative of voltage source inverter. VF-SCII 2 has two operating states: shoot through state and non-shoot through state, as shown in Figure 9.12. Shoot through means turning on the upper and lower switches on the same phase leg at the same time. If the shoot through is chosen to happen during the normal zero state, it will not affect the output voltage and current. However, the front inductor gets charged during shoot through state, so the inverter can boost voltage. The two equivalent circuit states of VF-SCII 2 are shown in Figure 9.12. When the inverter bridge shoot through happens, the front diode automatically turns off, and inductor 2 gets charged. In non-shoot through state, the diode is

on, and inductor 1 gets discharged. The inverter can be considered as a current source with equivalent voltage V_{out} in this case. In the whole switching period, the energy in the coupled inductor gets balanced, which means the total turns current product (N*I) keeps constant.



(a) (b)

Figure 9.12. Inverter b operating states (a) shoot through state D_0

(b) non-shoot-through state $1-D_0$

In shoot through state, L1 has zero current, but L2 is charged by C1. In non-shoot-through state, L1 and L2 are in series and charged by the voltage difference between source and capacitor. The inductor voltages in two states are:

$$\begin{cases} V_{L1\_1} = -\dfrac{n}{n-1}(V_{in} - V_{C1});\ V_{L2\_1} = -\dfrac{1}{n-1}(V_{in} - V_{C1}) & //at\ (1-D_0) \\ V_{L1\_2} = nV_{L2} = -nV_{C1};\ V_{L2\_2} = -V_{C1} & //at\ D_0 \end{cases} \tag{6.30}$$

, in which n is the trans ratio between L1 and L2, and D_0 is the shoot through duty cycle. Each inductor current is discontinuous since it has different expressions at different circuit states during one switching cycle. In another word, it has jump during one switching period. But the total flux in the inductor keeps constant. So a continuous unit inductor current can be defined here:

$$i_L = \frac{ni_{L1} + i_{L2}}{(n+1)} \tag{6.31}$$

This current can be taken as the state variable in the state space model since it is continuous.

Therefore, take unit inductor current i_L and capacitor voltage V_C as the state variables, then the state space equation of VF-SCII 2 is:

$$\begin{cases} L\dfrac{di_L}{dt} = \dfrac{1}{1+n}(V_{L1\_1} + V_{L2\_1}) = \dfrac{1}{1-n}(V_{in} - V_C) \\ C\dfrac{dv_C}{dt} = i_L + \dfrac{n}{n-1} i_{load} \end{cases} \quad [at\ (1-D_0)]$$
$$\begin{cases} L\dfrac{di_L}{dt} = \dfrac{1}{1+n}(V_{L1\_2} + V_{L2\_2}) = -V_C \\ C\dfrac{dv_C}{dt} = (1-n) i_L \end{cases} \quad [at\ D_0] \tag{6.32}$$

The steady state solution for inductor current and capacitor voltage could be obtained by using state space average method. The average inductor current and capacitor voltage are:

$$\begin{cases} \overline{L\dfrac{di_L}{dt}} = \dfrac{1-D_0}{1-n}(V_{in} - V_C) - D_0 V_C \\ \overline{C\dfrac{dv_C}{dt}} = (1-D_0)(i_L + \dfrac{n}{n-1} i_{load}) + D_0(1-n) i_L \end{cases} \tag{6.33}$$

The volt-seconds and ampere-seconds balances impose:

$$\overline{L\frac{di_L}{dt}} = 0; \quad \overline{C\frac{dv_C}{dt}} = 0; \tag{6.34}$$

Thus the averaged i_L and v_C can be derived as:

$$I_L = \frac{-n(1-D_0)}{1-nD_0} i_{load}; \quad V_C = \frac{1-D_0}{1-nD_0} V_{in} \tag{6.35}$$

The equivalent output voltage in non-shoot-through state in average model can also be derived as:

$$V_{out} = \frac{V_C}{1-D_0} = \frac{1}{1-nD_0} V_{in} \tag{6.36}$$

Thus the boost ratio of the switched-coupled-inductor network is:

$$B = \frac{1}{1-nD_0} \tag{6.37}$$

The voltage gain between input and output then can be expressed as, by using that $D_0 = 1-\sqrt{3}M/2$:

$$G = MB = \frac{M}{1-nD_0} = \frac{M}{1-n(1-\frac{\sqrt{3}}{2}M)} \tag{6.38}$$

, from which it can be seen that this inverter has voltage buck-boost function.

The current stress on the active devices in inverter bridge is equal to output current in non-shoot through state. But the maximum current stress depends on the current in shoot through state, which is the inductor 2 current in this case. According to the flux constant equation:

$$(n+1)\overline{i_L} = 1 \cdot i_{L2}' \tag{6.39}$$

The L2 current in shoot through state can be derived as:

$$i_{L2}' = \frac{n(1-D_0)}{1+nD_0} \tag{6.40}$$

, which is also the current stress on the active device.

9.4.2. Generalized state space model for the voltage-fed family

Assuming the non-shoot-through state is state I and shoot through state is state II, the generalized state space equation for all topologies in the voltage-fed family in no load case is:

$$\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix} \begin{bmatrix} \dot{I}_L \\ \dot{V}_C \end{bmatrix} = \begin{bmatrix} 0 & \frac{F_{LC}}{K_{LC}} \\ \frac{-F_{LC}(n+1)}{K_{LC}} & 0 \end{bmatrix} \begin{bmatrix} I_L \\ V_C \end{bmatrix} + \begin{bmatrix} \frac{F_{Lg}}{K_{Lg}} \\ F_{Cg} \end{bmatrix} V_{in} \tag{6.41}$$

The definitions of the coefficients are:

F_{LC}: connection between L & C: when L charges C, $F_{LC} = -1$; when C charges L, $F_{LC} = 1$; when there is no connection $F_{LC} = 0$;

K_{LC} : per unit number of turns of the inductor that injects current to capacitor; the base value is the smaller number of turns in two inductors.

F_{Lg} : connection between L and source; if current flows from source to inductor, $F_{Lg}=1$; otherwise $F_{Lg}=-1$.

F_{Cg} : connection between C and source; $F_{Cg}=0$ in this case.

Therefore for each circuit state shown in Figure 9.12, a state space equation can be obtained for each circuit. The average capacitor voltage and average inductor current then can be derived by using average method. Their general forms are:

$$V_C=\frac{-[D_0\frac{F_{Lg1}}{K_{Lg1}}+(1-D_0)\frac{F_{Lg2}}{K_{Lg2}}]}{D_0\frac{F_{LC1}}{K_{LC1}}+(1-D_0)\frac{F_{LC2}}{K_{LC2}}}V_{in} \tag{6.42}$$

$$I_L=\frac{D_0F_{Cg1}+(1-D_0)F_{Cg2}}{D_0\frac{F_{LC1}(n+1)}{K_{LC1}}+(1-D_0)\frac{F_{LC2}(n+1)}{K_{LC2}}}V_{in} \tag{6.43}$$

The general form for the voltage-fed switched-coupled-inductor inverter family can be further derived as:

$$\begin{cases} L\dfrac{di_L}{dt}=(1-h_0)\cdot(G_{LC1}v_C+G_{Lg1}V_{in})+h_0\cdot(G_{LC2}v_C+G_{Lg2}V_{in})-ri_L \\ C\dfrac{dv_C}{dt}=(1-h_0)(G_{CL1}i_L+G_{CR1}v_C+G_{cg1}V_{in}) \\ \qquad\qquad +h_0(G_{CL2}i_L+G_{CR2}v_C+G_{cg2}V_{in}) \\ L_i\dfrac{di_i}{dt}=(h_i-h_0-\dfrac{1}{M}(\sum_{i=1}^{M}h_i-M\cdot h_0))(1-h_0) \\ \qquad\qquad \cdot[V_{in}-k_w(G_{LC1}v_C+G_{Lg1}V_{in})]-v_i \qquad (i=1,2..M) \\ C_i\dfrac{dv_i}{dt}=i_i-\dfrac{v_i}{R} \qquad (i=1,2..M) \end{cases} \tag{6.44}$$

, in which

$$G_{LCi} = \frac{F_{LCi}}{K_{Li}}; G_{CLi} = \frac{F_{CLi}}{K_{Ci}}; G_{CRi} = \frac{F_{CRi}}{R}; G_{Lgi} = \frac{F_{Lgi}}{K_{Si}}; G_{Cgi} = F_{Cgi};$$

$i = 1, 2, ..N$ (N *is the number of circuit states in one switching cycle*)

Definition of the coefficients in the generalized state space equation of the voltage-fed SCII family:

F_{CLi}: $F_{CLi} = -F_{LCi}$;

F_{CRi}: when resistor current flows into positive side of capacitor, $F_{CRi} = 1$; when it flows into negative side, $F_{CRi} = -1$; when there is no connection, $F_{CRi} = 0$.

K_{Li}: the total number of turns in per unit of the inductors that connect with the corresponding capacitor and also exchange energy with it.

K_{Ci}: the number of turns in per unit of the single inductor that connects with the capacitor and also exchanges energy with it.

K_{Si}: the total number of turns in per unit of the inductors that connect with the voltage source and also exchange energy with it.

K_w: the number of turns in per unit of the inductors that between source and the inverter bridge; it is positive when the inductor voltage positive side connects with the source, and negative when the negative side connects with the source.

K_{sw}: per unit number of turns between input source and the dc side switch; it is positive when the source current flows into the positive side of the inductor with per unit 1 number of turns; otherwise it is negative.

9.4.3. Governing equations for voltage-fed family

From the generalized state space equation, the governing equations for the inverter voltage

TABLE 9-2. VOLTAGE GAIN AND ACTIVE/PASSIVE DEVICE STRESS FOR VF-SCII

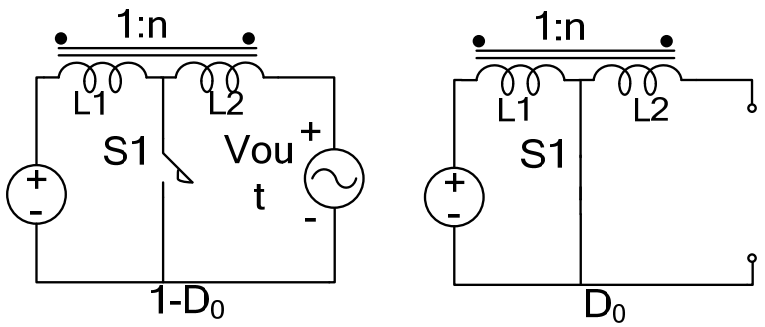
	Passive Stress		Voltage Gain
	Vc/Vin	IL/iload	Vout/Vin
VF-SCII 1	$\frac{(1-D_0)}{1+nD_0}$	$\frac{n(1-D_0)}{1+nD_0}$	$\frac{1}{1+nD_0}$
VF-SCII 2	$\frac{(1-D_0)}{1-nD_0}$	$\frac{-n(1-D_0)}{1-nD_0}$	$\frac{1}{1-nD_0}$
VF-SCII 3	$\frac{(n+1)(1-D_0)}{1+n(1-D_0)}$	$\frac{n(1-D_0)}{1+n-nD_0}$	$\frac{(n+1)}{1+n(1-D_0)}$
VF-SCII 4	$\frac{(-n+1)(1-D_0)}{1-n(1-D_0)}$	$\frac{-n(1-D_0)}{1-n+nD_0}$	$\frac{-n+1}{1-n(1-D_0)}$
VF-SCII 5	$\frac{n(1-D_0)}{n(1-D_0)-D_0}$	$\frac{n(1-D_0)}{(n+1)D_0-n}$	$\frac{n}{n(1-D_0)-D_0}$
VF-SCII 6	$\frac{n(1-D_0)}{n(1-D_0)+D_0}$	$\frac{-n(1-D_0)}{(-n+1)D_0+n}$	$\frac{n}{n(1-D_0)+D_0}$
	INV I Stress	Frong Switch Stress	
	Isw/Iload	Vfs/Vin	Ifs/Iload
VF-SCII 1	$\left\lvert\frac{n(1-D_0)}{1+nD_0}\right\rvert$	$\frac{1+n}{1+nD_0}$	$\frac{-1}{1+nD_0}$
VF-SCII 2	$\left\lvert\frac{-n(1-D_0)}{1-nD_0}\right\rvert$	$\frac{1-n}{1-nD_0}$	$\frac{-1}{1-nD_0}$
VF-SCII 3	$\left\lvert\frac{n(1-D_0)}{1+n-nD_0}\right\rvert$	$\frac{1}{1+n-nD_0}$	$\frac{-1-n}{1+n-nD_0}$
VF-SCII 4	$\left\lvert\frac{-n(1-D_0)}{1-n+nD_0}\right\rvert$	$\frac{1}{1-n+nD_0}$	$\frac{-1+n}{1-n+nD_0}$
VF-SCII 5	$\left\lvert\frac{(n+1)(1-D_0)}{(n+1)D_0-n}\right\rvert$	$\frac{n(1-D_0)-1}{n(1-D_0)-D_0}$	$\frac{n}{nD_0+D_0-n}$
VF-SCII 6	$\left\lvert\frac{(-n+1)(1-D_0)}{(-n+1)D_0+n}\right\rvert$	$\frac{-n(1-D_0)-1}{-n(1-D_0)-D_0}$	$\frac{-n}{-nD_0+D_0+n}$

gain, inverter switch current stress, capacitor voltage stress, inductor current stress and front switch voltage and current stress could be derived, as listed in Table 9-2. The trans-ratio are

defined in Figure 9.12.

9.4.4. Steady state analysis for current-fed family

CF-SCII 2 is taken as an study example here. It has two operating states shown in Figure 9.13. The extra open zero state has a duty cycle of D_0.



(a)Active state (b) open zero state D_0

Figure 9.13. Two operation states of current source inverter h

The volt-seconds equation on L1 leads to:

$$(1-D_0)(V_{in}-V_{out})\frac{1}{1-n}+D_0V_{in}=0 \tag{9.14}$$

Thus the expression for V_{out}/V_{in} is:

$$V_{out}/V_{in}=\frac{1-nD_0}{1-D_0} \tag{9.15}$$

Thus when n<1, it can boost voltage; when n>1, it can buck the voltage; when n goes to even bigger that $n>\frac{1}{D_0}$, it enters into regeneration mode.

9.4.5. Generalized state space model for current-fed family

Similar to previous voltage-fed equations, the generalized state space equation for the family of current-fed SCI inverter in no load condition is:

$$\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix} \begin{bmatrix} \dot{I}_L \\ \dot{V}_C \end{bmatrix} = \begin{bmatrix} 0 & \frac{F_{LC}}{K_{LC}} \\ \frac{F_{LC}}{K_{LC}} & 0 \end{bmatrix} \begin{bmatrix} I_L \\ V_C \end{bmatrix} + \begin{bmatrix} \frac{F_{Lg}}{K_{Lg}} \\ F_{Cg} \end{bmatrix} V_{in} \tag{9.16}$$

, which share the same definitions of the coefficients as voltage-fed equations.

The generalized state space equation for the normal case is:

$$\begin{cases} L\dfrac{di_L}{dt} = h_0 \cdot V_{in} \cdot \dfrac{1}{K_{sw}} + (1-h_0) \cdot (V_{in} - \sum_{i=1}^{M} h_i v_i) \cdot \dfrac{1}{k_w} \\ C_i \dfrac{dv_i}{dt} = h_i \cdot i_L - \dfrac{v_i}{R} \\ (i = 1, 2..M,\ h_i = h1_i - h2_i, \textit{where } h1_i \textit{is the switching function for} \\ \textit{upper switch, and } h2_i \textit{ is the switching function for lower switch}) \end{cases} \tag{9.17}$$

9.4.6. Governing equations for current-fed family

TABLE 9-3. VOLTAGE GAIN AND ACTIVE/PASSIVE DEVICE STRESS FOR CF-SCII

	Voltage Gain	Inductor current stress	INV switch voltage stress
	Vout/Vin	IL/(Vin/2R)	Vsw/Vin (D0)
CF-SCII 1	$\frac{1+nD_0}{1-D_0}$	$\frac{1}{1-D_0}\cdot G$	$\frac{1+nD_0}{1-D_0}$
CF-SCII 2	$\frac{1-nD_0}{1-D_0}$	$\frac{1}{1-D_0}\cdot G$	$\frac{1-nD_0}{1-D_0}$
CF-SCII 3	$\frac{n(1-D_0)+1}{(n+1)(1-D_0)}$	$\frac{1}{(n+1)(1-D_0)}\cdot G$	$\frac{n(1-D_0)+1}{(n+1)(1-D_0)}$
CF-SCII 4	$\frac{1-n(1-D_0)}{(1-n)(1-D_0)}$	$\frac{1}{(1-n)(1-D_0)}\cdot G$	$\frac{1-n(1-D_0)}{(1-n)(1-D_0)}$
CF-SCII 5	$\frac{n(1-D_0)-D_0}{n(1-D_0)}$	$\frac{1}{(n+1)(1-D_0)}\cdot G$	$\frac{n(1-D_0)-D_0}{n(1-D_0)}$
CF-SCII 6	$\frac{n(1-D_0)+D_0}{n(1-D_0)}$	$\frac{1}{(1-n)(1-D_0)}\cdot G$	$\frac{n(1-D_0)+D_0}{n(1-D_0)}$

	Inverter switch current stress	Front switch stress	
	Isw/(Vin/2R)	Vs/Vin	Is/（Vin/2R)
CF-SCII 1	$\frac{1}{1-D_0}\cdot G$	$\frac{1}{1-D_0}$	$\frac{1+n}{1-D_0}\cdot G$
CF-SCII 2	$\frac{1}{1-D_0}\cdot G$	$\frac{1}{1-D_0}$	$\frac{1-n}{1-D_0}\cdot G$
CF-SCII 3	$\frac{1}{1-D_0}\cdot G$	$\frac{1}{1-D_0}$	$\frac{1}{(1+n)}\frac{1}{(1-D_0)}\cdot G$
CF-SCII 4	$\frac{1}{1-D_0}\cdot G$	$\frac{1}{1-D_0}$	$\frac{1}{(1-n)}\frac{1}{(1-D_0)}\cdot G$

9.4.7. Simulation Results demonstration

Take voltage-fed SCII 2 as an example. Figure 9.14 - Figure 9.15 shows the simulation results for voltage-fed switched-coupled-inductor inverter 2, at m=0.6, n=2. Figure 9.16 - Figure 9.17 shows the simulation results for voltage-fed switched-coupled-inductor inverter 5, at m=0.75, n=0.5. The input voltage is fixed at 100V. From Figure 9.14, it can be seen that

the voltage has been boosted by 3 times. The dc link voltage is around 4.5 times of the input voltage, which

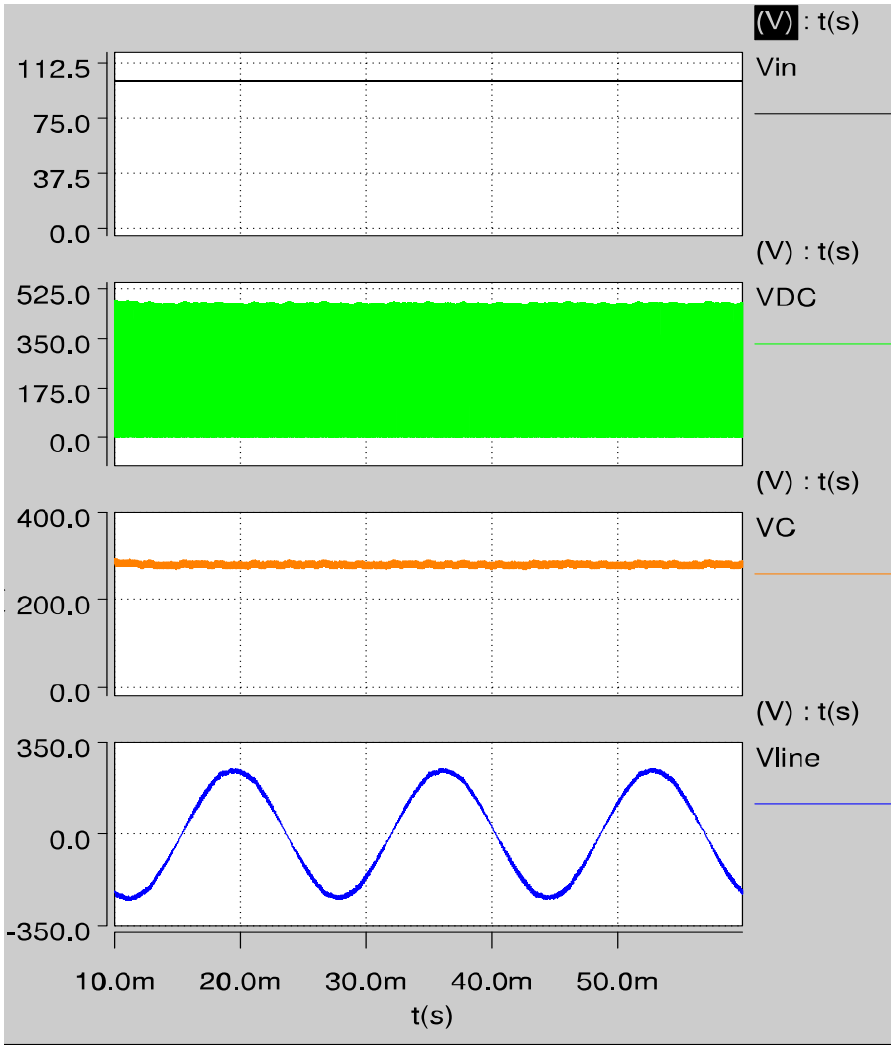


Figure 9.14 Simulation results for voltage-fed switched-coupled-inductor inverter 2 at M=0.6, n=2 (from the first to last: input voltage, dc link voltage before inverter bridge, input capacitor voltage, output line to line voltage)

is equal to the active switch voltage stress. Figure 9.15 demonstrates that both inductor current are discontinuous. However, the total ampere-turns keep the same. So the unit inductor current has been taken as the state

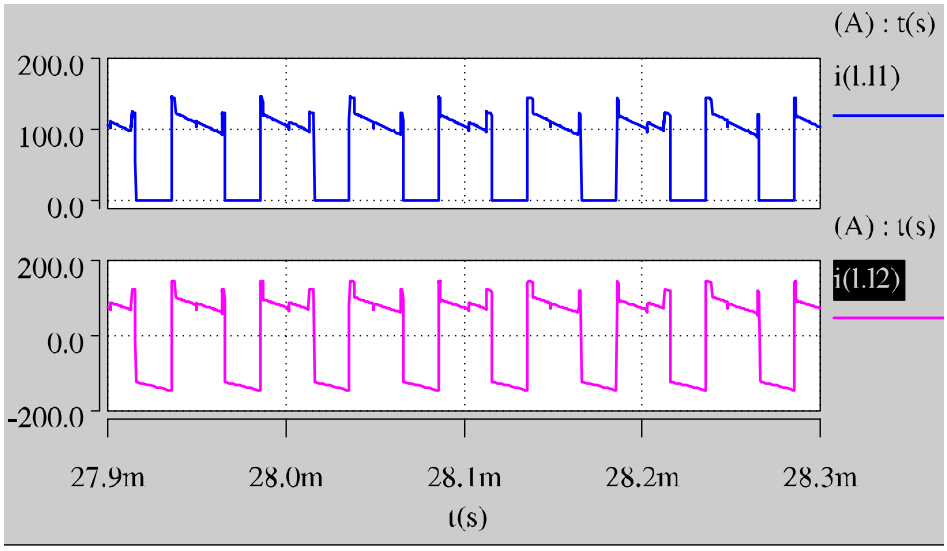


Figure 9.15 Input inductor L1 and L2 current (from first to last, input inductor 1 current, input inductor 2 current)

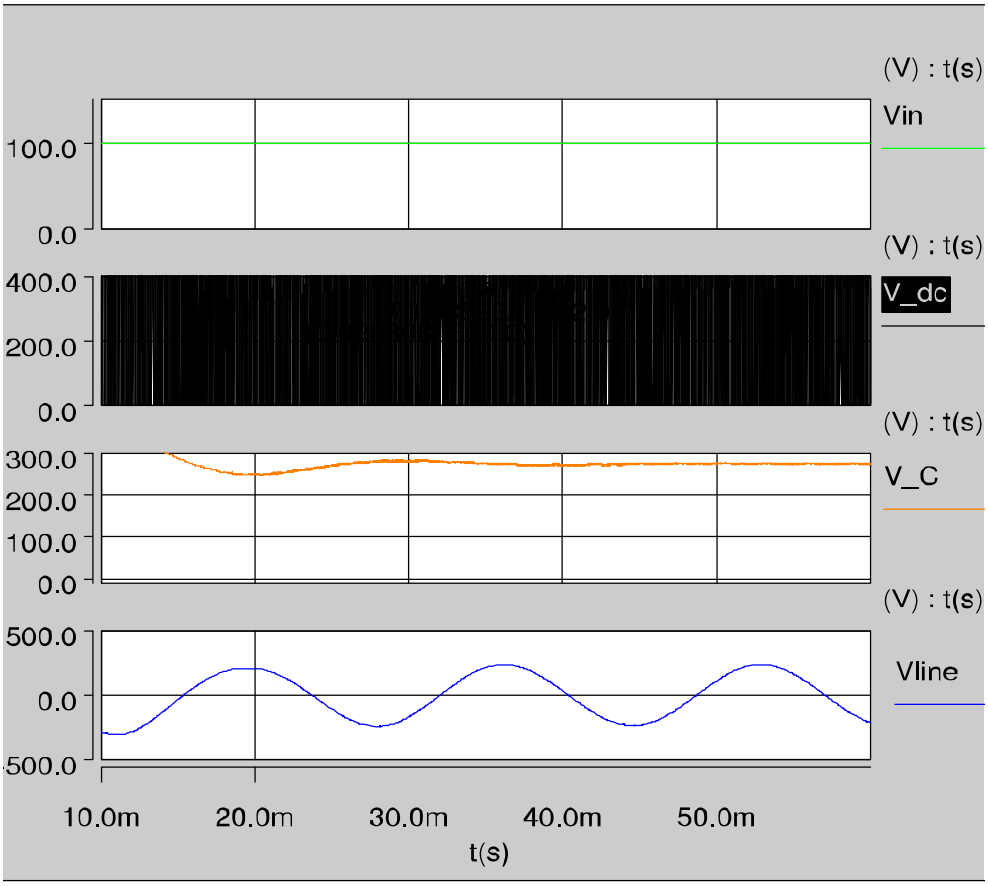


Figure 9.16. Simulation results for voltage-fed switched-coupled-inductor inverter 5 at M=0.75, n=0.5

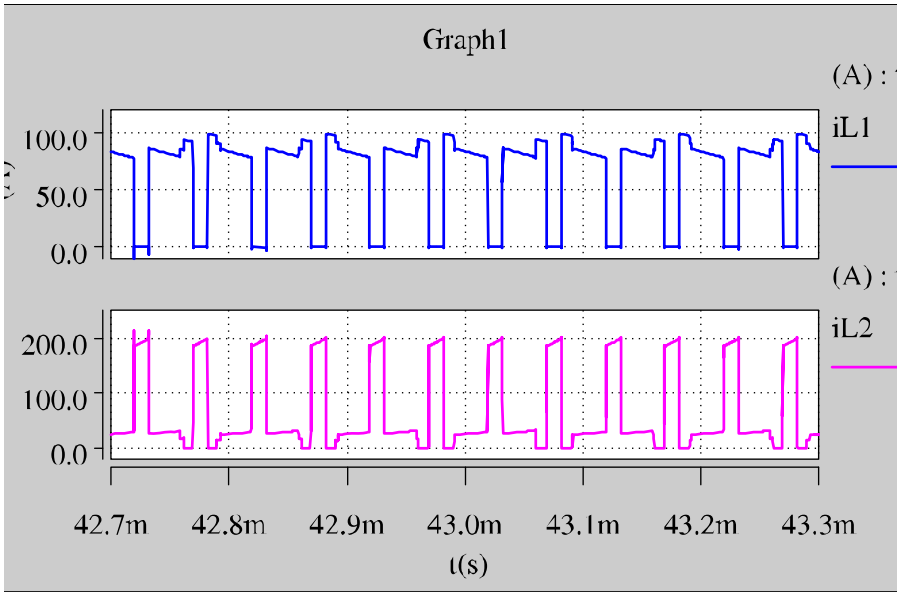


Figure 9.17. Input inductors L1 and L2 current

variables in the equation. In Figure 9.16, the voltage has been boosted by 2.75 times in voltage-fed topology 5, at the control parameters set. In Figure 9.17, both inductors current are positive, but discontinuous still.

These results have been measured accurately, to compare with the governing equations in Table 9-2 and Table 9-3. They match with each other very well, which verify the correctness of the previous analytical equations and theory analysis.

9.4.8. Conclusion for switched-coupled-inductor inverter

This section proposed a new family of buck-boost inverter topologies: voltage/current-fed switched-coupled-inductor inverter (SCII). The following features have been demonstrated by circuit fundamentals analysis and simulations:

(1) At the correct selection of trans-ratio n and extra switching state duty cycle, both voltage/current-fed topologies have candidates that can buck-boost voltage.

(1) Voltage-fed SCII has only half number of passive components compared to Z-source inverter, but higher voltage boost ratio and lower active switch voltage stress.

(2) Voltage-fed SCII has less active switch, smaller size and higher reliability than two stage boost-converter-inverter.

(3) Current-fed SCII is a capacitor-less solution, which is much more compact than the ones with capacitors (boost-converter-inverter and Z-source inverter)

(4) Current-fed SCII has lower active switch current stress than current-fed Z/quasi-Z-source inverter at the same voltage gain, in buck motoring and regeneration mode.

(5) With active front switch, both voltage and current-fed SCII can have regenerative capability.

Due to the benefits, this voltage-fed switched-coupled-inductor inverter is beneficial to be used in the dc-ac applications that demand a high voltage gain from a very low voltage dc source, such as the micro-inverter in photovoltaic, or G/M in HEV. The current-fed switched-coupled-inductor inverter is potential candidate for compact, regenerative, high temperature, high efficiency, low cost HEV/EV motor drive or engine starter.

9.5. Summary

This chapter analyzes the state space model for three circuits: current-fed quasi-Z-source inverter (CF-qZSI), current-fed Z-source rectifier (CF-ZSR), switched-coupled-inductor inverter family (SCII). The transient performance of CF-qZSI has been analyzed according to the state space model and also has been demonstrated by the simulation and experiments. A dq state space model has been built for CF-ZSR, from which a linearized transfer function for the rectifier is derived, in order to guide the control loop design. For SCII, a generalized state space model based on the connection matrix has been built for all the topologies of voltage-fed or current-fed family, in order to derive all the governing equations including

voltage/current gain and device/passive voltage/current stress equations. This chapter could be extended to closed-loop control for each topology in the future work.

CHAPTER 10 CONCLUSIONS AND RECOMMENDATIONS

10.1. Contributions

This work has the following contributions:

◆ A new family of switched-coupled-inductor inverters has been proposed in this work, with voltage buck-boost function. The voltage-fed switched-coupled-inductor inverter has higher boost ratio and lower active device voltage stress than Z-source inverter at the same voltage gain, and has wider voltage buck/boost range than conventional boost-converter inverter. The current-fed switched-coupled-inductor inverter is a capacitor-less solution among the buck-boost inverters, which reduces the system size significantly. Compared to traditional boost-converter-inverter, it has less switch count, and less active device current stress. The features of the circuit are verified with simulation results.

◆ A zero vector placement technique in SVPWM has been proposed for current-fed quasi-Z-source inverter for HEV motor drive application, to obtain lowest switching loss, lowest current ripple, lowest output harmonics and lowest voltage spike on the device in both constant torque and constant power operation regions, in order to achieve higher efficiency, higher power density and lower cost. A 24kW current-fed quasi-Z-source inverter has been built in the lab and controlled by this technique. The full power rating efficiency reaches 97.6%, and peak efficiency reaches 98.2%, both of which have a 3%-4% improvement on traditional two stage configuration. The power density is 15.3KW/L, which is also 5KW/L higher than the commercial unit in HEV.

◆ A Space-Vector-Pulse-Width-Amplitude Modulation (SVPWAM) method has been proposed for buck-boost current source inverter. By using this method, the switching loss is

reduced by 60%, and the power density is increased by a factor of 2 to 3, with a less output harmonic distortion than normal SVPWM method. A 1 kW boost-converter-inverter prototype has been built and tested using this method. The overall system efficiency at full power rating reaches 96.7% and the whole system power density reaches 2.3 kW/L and 0.5 kW/lb, all of which are remarkable at this power rating. As a result, the proposed SVPWAM can make the buck-boost inverter suitable for applications that require high efficiency, high power density, high temperature, and low cost, such as EV motor drive or engine starter/alternator.

◆ Four control methods including simple maximum boost, maximum boost, maximum constant boost control and hybrid minimum stress control have been proposed for the newly proposed direct Z-source matrix converter, and verified with simulation/experiments.

◆ Two new discontinuous operation modes have been proposed for current-fed quasi-Z-source inverter topology. The characteristics of the discontinuous operation modes have been analyzed and the critical conditions under different control have been derived. Simulation and experiment results are given to verify the theoretical analysis.

◆ A transient state-space model has been built for current-fed quasi-Z-source inverter to demonstrate its fast transient response in motoring and regenerating transition. The analytical, simulated and experimental results all show that the inverter only needs several switching cycle to complete the transition, which makes it suitable for HEV/EV motor drive application.

10.2. Recommendations for future works

◆ The proposed switched-coupled-inductor inverter family needs to be verified through

experiments. Thus future work includes building a prototype for one topology in voltage-fed family and one topology in current-fed family to verify their unique features.

◆ The proposed SVPWAM modulation method has only been verified on the voltage source inverter through experiments. Thus the future work should be done with the buck-boost current source inverter in experiments, such as current-fed quasi-Z-source inverter topology.

◆ The discontinuous operation mode needs to be explored further to see if it can be utilized in order to bring some good features for the inverter, like higher boost ratio and so on.

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