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HIGH POWER DC-DC CONVERTER AND DISTRIBUTED
Z-SOURCE NETWORK DC-DC CONVERTER

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Honnyong Cha

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HIGH POWER DC-DC CONVERTER AND DISTRIBUTED Z-SOURCE NETWORK DC-DC CONVERTER

By

Honnyong Cha

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ABSTRACT

HIGH POWER DC-DC CONVERTER AND DISTRIBUTED Z-SOURCE NETWORK DC-DC CONVERTER

By

Honnyong Cha

Dc-dc converters are extensively used for various applications in industry to regulate output voltage when the input voltage of converter or output load changes. However, a lot of research activities are focused mainly on small or medium power converters, for example, less than 5 kW. High power dc-dc converters are now in great demand in many applications such as renewable energy interface systems, utility power electronics, electric vehicle system, and so on.

There are several challenging issues in designing high power and high frequency transformer isolated dc-dc converters. First, selection of the switching devices and soft switching techniques are essential to achieve high converter efficiency. Secondly, a high power and high frequency transformer design is becoming more and more important as power level of the power electronics systems increases. Thirdly, snubber or voltage clamping circuit that prevent switching devices from high voltage overshoot is also important.

In the second part of this dissertation, a 3 phase interleaved boost dc-dc converter for series hybrid electric bus system is introduced. The converter is designed to meet both 30 kW average and 120 kW peak power demand of bus. Therefore, the dc-dc converter in the HEV system plays an important role to maximize fuel efficiency. However, dominant part of the boost converter, both in terms of size and cost, belongs to the magnetic components. Consequently, better use of the magnetic content of the dc-dc converter may

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lead to substantial performance and cost improvements. In this section, a boost inductor using integrated magnetic approach is used to minimize inductor volume and power loss.

In order to overcome theoretical barriers of the traditional V-source or I-source converters, a novel dc-dc converter incorporating a distributed (or transmission line) Z-source network to achieve the buck (step-down) and boost (step-up) function of a transformer isolated dc-dc converter is presented in the third section. In this section, a distributed Z-source network composed of an array of inductors and capacitors is coupled between the power source and main switching devices. The great and unique feature about the distributed Z-source network dc-dc converter is that unlike the traditional V-source or I-source converters, it can be open- and short-circuited without damaging switching devices. Therefore, the desired buck and boost function can be achieved. Moreover, converter reliability can be greatly improved.

Dedicated to:
my grandmother, Woesung Kim
my parents, Sanghwa Cha and Deokin Bae
and my beloved family, Juhee Park, Yeonwoo Cha, Arin Cha

ACKNOWLEDGEMENTS

With my heartfelt gratitude, I would like to thank my advisor, Dr. Fang Z. Peng for his guidance, encouragement and continuous support throughout my studies here. Without his guidance, I could not have finished this work. I am also very grateful to my committee members, Dr. Schlueter, Dr. Strangas, and Dr. Jongeun Choi for their valuable suggestions and help.

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Many thanks are also extended to my colleagues in PEMD Lab. for their delightful discussion and friendship, Dr. Yi Huang, Ms. Wei Qian, Mr. Craig Rogers, Mr. Uthane Supatti, Mr. Irvine Balaguer, Mr. Dong Cao, Mr. Joel Anderson, Ms. Xi Lu, Ms. Qin Lei, Mr. Sangmin Han, Mr Shuai Jiang.

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TABLE OF CONTENTS

LIST OF TABLES viii

LIST OF FIGURES ix

Chapter 1. Introduction 1
1.1. Motivations and Objectives of Research 1
1.2. Scope of the dissertation 4

Chapter 2. Design and Development of 210 kW DC-DC Converter for Auxiliary Power Supply for Metro Vehicle 6
2.1. System Topology and Ratings 6
2.2. Design of Isolated Full-Bridge DC-DC Converter 8
2.2.1 Energy Recovery Passive Snubber Circuit 8
2.2.2 Selection of PSSS and ERCC Parameters 13
2.2.3 Operational modes 14
2.2.4 Selection of PWM Control Method 16
2.3. Experimental Results 19
2.4. Conclusion 21

Chapter 3. High Power Transformer and Inductor Design 22
3.1. Losses in Magnetics 22
3.2. Transformer design 23
3.2.1 Core loss 23
3.2.2 Winding (Copper) loss 26
3.3. Inductor design 38
3.3.1 Inductance Calculation by Permeability vs. DC Bias Curves 39
3.3.2 Core loss 41
3.3.3 Winding loss 42
3.4. Conclusion 43

Chapter 4. Voltage Oscillation Problem in Secondary Rectifier Diode 45
4.1. Introduction 45
4.2. Review of Previously Proposed ERCC 48
4.3. Proposed ERCC 53
4.3.1 Principle Operation of Proposed ERCC 53
4.3.2 Simulation and Experimental Results 62
4.4. Conclusion 71

Chapter 5. Power Loss Breakdown and Overall System Test 72
5.1. Power loss breakdown 73
5.2. Overall system test 76
5.3. Conclusion 79

Chapter 6. Integrated Magnetics for Interleaved Boost DC-DC Converter for Series Hybrid Electric Bus 80

6.1.
6.2.
6.
6.
6.3.
6.4.
6.5.

Chapte
7.1.
7.2.
7.3.
7.3
7.3
7.4.
7.5.
7.6.

Chapter
8.1.
8.2.
8.3.
8.3.
8.3.
8.4.
8.4.
8.4.
8.5. S
.....
8.6. C

Chapter
9.1. C
9.2. R

Bibliog

6.1. Introduction 80
6.2. Interleaved Boost Converter and Integrated Magnetics 83
6.2.1 Review of Interleaved Boost Converter. 83
6.2.2 Integrated Magnetics 87
6.3. Design of High Efficient and High Density Integrated Magnetics 91
6.4. Experimental Results 101
6.5. Conclusion 107

Chapter 7. Distributed Z-Source Network DC-DC Converter 108
7.1. Introduction 108
7.2. Why buck-boost converter? 111
7.3. Literature Survey for Buck-Boost Converters 114
7.3.1 Non-Isolated Buck-Boost Topologies 114
7.3.2 Transformer Isolated Buck-boost Topologies 117
7.4. The Z-Source Concept and Distributed Z-Source Network 126
7.5. Transmission Line Based Z-Source Network-Distributed Z-Source Network 128
7.6. Conclusion 133

Chapter 8. Principle Operation of Distributed Z-Source Network DC-DC Converter 135
8.1. Input Impedance of Distributed Z-Source Network 135
8.2. Voltage and Current distribution along DZSN 141
8.3. Output Voltage Control of the Proposed DZSN DC-DC Converter 143
8.3.1 Buck mode (Vin>Vo) 144
8.3.2 Boost mode (Vin<Vo) 148
8.4. Derivation of Voltage Gain 152
8.4.1 Buck mode 152
8.4.2 Boost mode 154
8.5. Simulation and Experimental Results of the Proposed DZSN DC-DC Converter. 157
8.6. Conclusion 163

Chapter 9. Contributions and Future Works 164
9.1. Contributions 164
9.2. Recommendations for future works 165

Bibliography 166

Table
Table
Table
Table
Table
Table
Table
Table
Table
Table
Table
Table
Table 8
Table 8
convert

LIST OF TABLES

Table 2-1 Comparison of Power Loss 19

Table 3-1 Current Waveform and Electrical Parameter of Copper Foil. 31

Table 3-2 Coupled inductor design parameters. 39

Table 4-1 Operational Conditions and Circuit Parameters of dc-dc Converter 63

Table 5-1 Power loss breakdown in 70 kW dc-dc converter 75

Table 6-1 Electrical Specifications of battery and boost dc-dc converter. 81

Table 6-2 Calculation of $f(D)$ for N=2, 3 and 4 84

Table 6-3 Basic Material Characteristics 93

Table 6-4 Parameters of IM core 97

Table 6-5 Measured inductances of flat IM at 40 A 99

Table 6-6 Calculation of power losses in IM 106

Table 8-1 Electrical specifications of DZSN. 139

Table 8-2 Test conditions and electrical specifications of proposed DZSN dc-dc converter. 158

Figure
Figure
Figure
Figure
Figure
Figure
Figure
Figure
Figure
Figure
Figure
Figure
Figure
Figure
Figure
Figure
circuited
Figure 3-
Figure 3-
Figure 3-
interleave
Figure 3-
Figure 3-
Figure 3-
interleave
Figure 3-
Figure 3-

LIST OF FIGURES

Figure 1-1 A V-source FB PWM DC-DC converter. 3

Figure 1-2 An I-source FB PWM DC-DC converter. 3

Figure 2-1 Overall system configuration for 260 kVA auxiliary power supply. 7

Figure 2-2 Common IGBT snubber circuits 8

Figure 2-3 Overall schematic of 70 kW DC-DC converter 11

Figure 2-4 Energy recovery circuit 12

Figure 2-5 Operational modes of dc-dc converter. 15

Figure 2-6 Duty cycle control 18

Figure 2-7 Phase-shift PWM control 18

Figure 2-8 Transformer primary current and IGBT voltage waveforms 20

Figure 2-9 Recovery current in primary snubber resistor and IGBT voltage waveform. 20

Figure 3-1 Losses in Magnetics. 22

Figure 3-2 Core loss measurement 24

Figure 3-3 Transformer voltage and current waveforms with secondary side open-circuited 24

Figure 3-4 Core loss measurement waveforms 25

Figure 3-5 Core loss curves for 3C90 material. 25

Figure 3-6 Winding arrangement and MMF waveform in transformer with single interleaved winding 30

Figure 3-7 Primary winding loss in single interleaved winding. 32

Figure 3-8 Secondary winding loss in single interleaved winding. 32

Figure 3-9 Winding arrangement and MMF waveform in transformer with double interleaved winding 34

Figure 3-10 Primary winding loss in double interleaved winding 35

Figure 3-11 Secondary winding loss in double interleaved winding 35

Figu
Figu
Figu
Figu
Figu
Figu
Figu
Figur
Figur
Figur
Figure
Figure
Figure
Figure
Figure
Figure
Figure
Figure
Figure
Figure
Figure
Figure
Figure
Figure

Figure 3-12 Transformer winding geometry 37

Figure 3-13 Transformer assembled with core and housed in aluminum case 37

Figure 3-14 Block core assembly 38

Figure 3-15 % permeability vs H curve of Changsung megaflux block core 40

Figure 3-16 Copper resistivity vs. temperature 42

Figure 3-17 Inductor assembly (Side view) 44

Figure 3-18 Inductor assembly (Top view) 44

Figure 4-1 Voltage oscillation problem in secondary rectifier diode 45

Figure 4-2 RCD clamped circuit 46

Figure 4-3 Active clamp circuit 47

Figure 4-4 Voltage oscillation reduction circuit using C_b 47

Figure 4-5 Energy recovery clamp circuit. 48

Figure 4-6 ERCC modified from Figure 4-5 (ERCC #1) 49

Figure 4-7 Diode voltage (V_{rec}) waveform of ERCC #1. 49

Figure 4-8 V_{rec_pk} vs duty cycle (D) of ERCC #1 50

Figure 4-9 ERCC modified from the circuit in [29] 52

Figure 4-10 Proposed ERCC. 54

Figure 4-11 Key waveforms of proposed ERCC. 54

Figure 4-12 Operational modes of proposed ERCC 55

Figure 4-13 Comparison of V_{rec_pk} as a function of D. 62

Figure 4-14 Simulation waveforms of proposed ERCC when D=0.483 64

Figure 4-15 Simulation waveforms of proposed ERCC when D=0.8 64

Figure 4-16 Experimental waveforms measured without calmp circuit 65

Figure 4-17 Experimental waveforms measured with proposed ERCC 65

Figure 4
Figure 4
Figure 4-
Figure 4-
Figure 4-
Figure 4-2
Figure 4-2
Figure 4-2
Figure 5-1
Figure 5-2
Figure 5-3
Figure 5-4
Figure 5-5
Figure 5-6
Figure 5-7
Figure 6-1
Figure 6-2
Figure 6-3
Figure 6-4
Figure 6-5
Figure 6-6
Figure 6-7
Figure 6-8
Figure 6-9
Figure 6-10

Figure 4-18 Experimental waveforms with proposed ERCC when D=0.483 66
Figure 4-19 Zoom-in waveforms of Figure 4-18 66
Figure 4-20 Experimental waveforms using proposed ERCC when D=0.8 67
Figure 4-21 Zoom-in waveforms of Figure 4-20 67
Figure 4-22 Experimental waveforms of ERCC #1 69
Figure 4-23 Proposed ERCC 69
Figure 4-24 Measured and theoretical results of V_{rec_pk} vs. C_{s1}. 70
Figure 4-25 Measured efficiency at 50 kW output power. 70
Figure 5-1 3-D design of 70 kW dc-dc converter 72
Figure 5-2 Photo of 70 kW dc-dc converter 72
Figure 5-3 Loss breakdown of 70 kW dc-dc converter. 76
Figure 5-4 Overall system configuration of 210 kW aux. power supply 77
Figure 5-5 210 kW system test 77
Figure 5-6 Power meter measurement of overall system test 78
Figure 5-7 Transformer primary current of three DC-DC converter module. 78
Figure 6-1 Overall system configuration of series hybrid electric bus 80
Figure 6-2 A 3-Phase interleaved boost converter 82
Figure 6-3 Normalized input current ripple of IBC 85
Figure 6-4 Inductor current interleaving when 0 < D <1/3 85
Figure 6-5 Inductor current interleaving when 1/3 < D <2/3. 86
Figure 6-6 Inductor current interleaving when 2/3 < D <1 86
Figure 6-7 Core structure of 3 phase IM 87
Figure 6-8 IM assembled with winding 87
Figure 6-9 Reluctance model of IM 88
Figure 6-10 Normalized current ripple as a function of D for several values of k. 91

Figure
Figure
Figure
Figure
Figure
Figure
Figure 6
Figure 6
Figure 6-
Figure 6-
Figure 6-
Figure 6-
Figure 7-1
Figure 7-2
Figure 7-3
Figure 7-4
Figure 7-5
Figure 7-6
Figure 7-7
Figure 7-8
Figure 7-9
Figure 7-10
Figure 7-11
Figure 7-12
Figure 7-13

Figure 6-11 Proposed flat IM. (Front view) 95
Figure 6-12 Proposed flat IM. (Side view) 95
Figure 6-13 % permeability vs. H curve of Changsung 40μ block core 96
Figure 6-14 Modified reluctance model when a voltage is applied to only outer leg 2. . 98
Figure 6-15 Inductance measurement of IM 99
Figure 6-16 Experimental waveforms of IBC using IM when D=0.5. 102
Figure 6-17 Experimental waveforms of IBC using IM when D=2/3. 102
Figure 6-18 Inductor current and IGBT switching waveforms at 120 kW. 104
Figure 6-19 Input current and IGBT switching waveforms at 120 kW. 104
Figure 6-20. Photo of prototype IM before molding. 105
Figure 6-21 Photo of molded IM after molding 105
Figure 6-22 Temperature increase of IM 106
Figure 7-1 V-source FB PWM DC/DC converter. 109
Figure 7-2 I-source FB PWM DC/DC converter. 109
Figure 7-3 The effect of EMI or misgating on switching device 110
Figure 7-4 Buck converter 111
Figure 7-5 Boost converter 111
Figure 7-6 Input and output voltage range of buck, boost and buck-boost converter ... 112
Figure 7-7 Efficiency profile of buck, boost and buck-boost converter 112
Figure 7-8 Buck and boost two stage converter 114
Figure 7-9 Buck-boost converter 115
Figure 7-10 Cuk converter 116
Figure 7-11 SEPIC converter 117
Figure 7-12 Flyback converter 118
Figure 7-13 Transformer model of flyback converter 118

Figure 7-

Figure 7-

Figure 7-

Figure 7-

Figure 7-

Figure 7-1

Figure 7-2

Figure 7-2

Figure 7-2

Figure 7-2

Figure 7-2

Figure 7-2

Figure 7-2

Figure 7-2

Figure 7-2

Figure 7-29

Figure 7-30

Figure 7-31

Figure 8-1

Figure 8-2

Figure 8-3

Figure 8-4

Figure 8-5

length cond

Figure 7-14 Isolated Cuk converter 119

Figure 7-15 Back-to-back bi-directional converter 120

Figure 7-16 LLC series resonant dc-dc converter 121

Figure 7-17 Voltage gain of LLC series resonant converter 121

Figure 7-18 Z-source dc-dc converter 122

Figure 7-19 qZ-Source dc-dc converter. 123

Figure 7-20 Key waveforms in buck mode 124

Figure 7-21 Key waveforms in boost mode 125

Figure 7-22 Voltage gain of Z(qZ)-Source dc-dc converter. 126

Figure 7-23 A general topology of the Z-source converter. 127

Figure 7-24 A general topology of the distributed Z-source converter [46] 128

Figure 7-25 A basic structure of DZSN or transmission line network. 129

Figure 7-26 Electrical representation of DZSN. 129

Figure 7-27 Common-mode connected DZSN. 130

Figure 7-28 Differential-mode connected DZSN. 130

Figure 7-29 Photos of DZSN implemented (Top view) 132

Figure 7-30 Photos of DZSN implemented (front view) 132

Figure 7-31 Proposed DZSN dc-dc converter. 133

Figure 8-1 Input impedance measurement 135

Figure 8-2 Simulation results of Z_{in} with $Z_L = 0$ 139

Figure 8-3 Z_{in} measurement of DZSN with $Z_L = 0$ (Magnitude) 140

Figure 8-4 Z_{in} measurement of DZSN with $Z_L = 0$ (Phase) 140

Figure 8-5 Voltage and current distribution along DZSN when $f_{ex} = f_1$, Quarter wave-length condition ($l = \frac{\lambda}{4}$) 142

Figure 8-
length co
Figure 8-
Figure 8-
Figure 8-
Figure 8-
Figure 8-
Figure 8-
Figure 8-
Figure 8-
Figure 8-
Figure 8-
Figure 8-
Figure 8-
Figure 8-
Figure 8-
Figure 8-
Figure 8-
Figure 8-
Figure 8-

Figure 8-6 Voltage and current distribution along DZSN when $f_{ex} = 2f_1$. Half wave-length condition ($l = \frac{\lambda}{2}$) 143

Figure 8-7 DZSN dc-dc converter. 144

Figure 8-8 Operation point at buck mode (point "A") 145

Figure 8-9 Key waveforms of the proposed dc-dc converter at buck mode 146

Figure 8-10 Voltage overshoot in Vpn at buck mode 148

Figure 8-11 Operation point at boost bode (between point "A" and point "B") 149

Figure 8-12 Key waveforms of the proposed dc-dc converter at boost mode 151

Figure 8-13 Waveforms at buck mode 152

Figure 8-14 Waveforms at boost mode 154

Figure 8-15 Relationship between f_{sw} and D 156

Figure 8-16 Voltage gain of the DZSN dc-dc converter 157

Figure 8-17 Simulation waveforms at buck mode (Vin>Vo). 159

Figure 8-18 Experimental waveforms at buck mode(Vin>Vo). 159

Figure 8-19 Simulation waveforms at boost mode (Vin<Vo). 160

Figure 8-20 Experimental waveforms at boost mode (Vin<Vo). 160

Figure 8-21 Simulation waveforms at normal mode (Vin=Vo). 161

Figure 8-22 Experimental waveforms at normal mode (Vin=Vo). 161

Figure 8-23. Efficiency of proposed converter vs. input voltage. 162

Chapter 1. Introduction

1.1. Motivations and Objectives of Research

Dc-dc converters are extensively used for various applications in industry to regulate output voltage when input voltage of the converter or the output load changes. However, a lot of research activities are focused mainly on small or medium power converters, for example, less than 5 kW. High power dc-dc converters are now in great demand in many applications such as renewable energy interface systems, utility power electronics, electric vehicle system, and so on.

There are several design issues and challenges for high power and high efficiency dc-dc converters. In this dissertation, we focus on three major issues in high power transformer isolated dc-dc converters especially for V-source type transformer isolated dc-dc converters. The same problems in V-source converter exist in I-source type converters as well.

First, an energy recovery passive snubber circuit is introduced to reduce voltage spike and power loss in switching devices. With the energy recovery circuit, a considerable amount of energy which is otherwise dissipated in conventional RCD snubber circuits can be recovered back to the DC link and thus increases system efficiency. Duty cycle and phase-shifted pulse width modulation (PWM) control methods are compared in terms of power loss in switching devices and transformer.

Secondly, high frequency and high power transformers are not very common in present day power supplies. A considerable effort has been directed towards high frequency transformers in the low power range. For a transformer with a power rating

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around 100 kW, the core selection and structure design are quite challenging. In this dissertation, the high frequency and high power transformer is designed using an interleaved winding method in order to reduce the proximity effect in transformer windings. An optimum copper (layer) thickness is found to minimize winding loss and transformer size.

Thirdly, diode voltage oscillation problem in the secondary rectifier diode is discussed and solutions are provided. For a PWM converter with a wide range of input voltage, especially when duty cycle of the converter is less than 0.5, voltage stress across the rectifier diodes could be very high. The use of higher voltage diodes increases power loss and voltage overshoot because higher voltage diodes have poor recovery characteristics.

Another important part for high power and high frequency dc-dc converter design is about magnetics such as transformers and inductors. The magnetics design is essential for achieving high efficiency and high density power converter design. Generally, the power loss in transformer and inductor in dc-dc converter is smaller than that of IGBT and rectifier diode. However, their thermal resistance from inside to outside is much greater than that of IGBT and rectifier diodes. The high thermal resistance causes heat accumulation inside transformer and inductor. As a result, it will leads to thermal runaway and finally system failure. Thus, magnetic design in high power converter system is very important and should not be overlooked

In addition to the above mentioned problems/issues, there is conceptual and theoretical barriers in traditional transformer isolated dc-dc power conversion circuits. Traditional transformer isolated dc-dc power conversion circuits are based on either a

voltage-source (V-source) or current-source (I-source) structure [1]. A V-source converter is fed from a power source with relatively constant voltage that is generally supported with capacitors. Figure 1-1 shows a V-source type full bridge (FB) pulse width modulation (PWM) dc-dc converter. Likewise, an I-source converter is fed from a power source with relatively constant current that is generally smoothed through inductors. Figure 1-2 shows the I-source type FB PWM dc-dc converter.

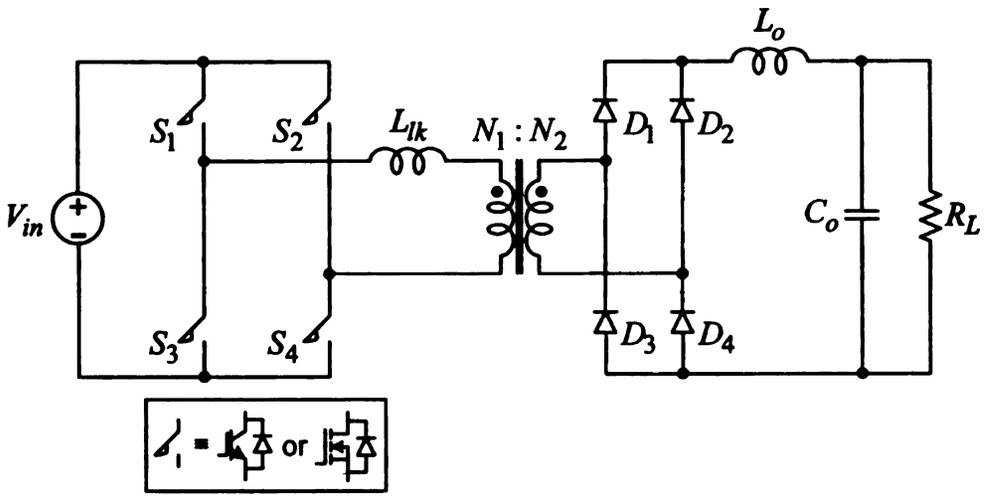

Figure 1-1 A V-source FB PWM DC-DC converter.

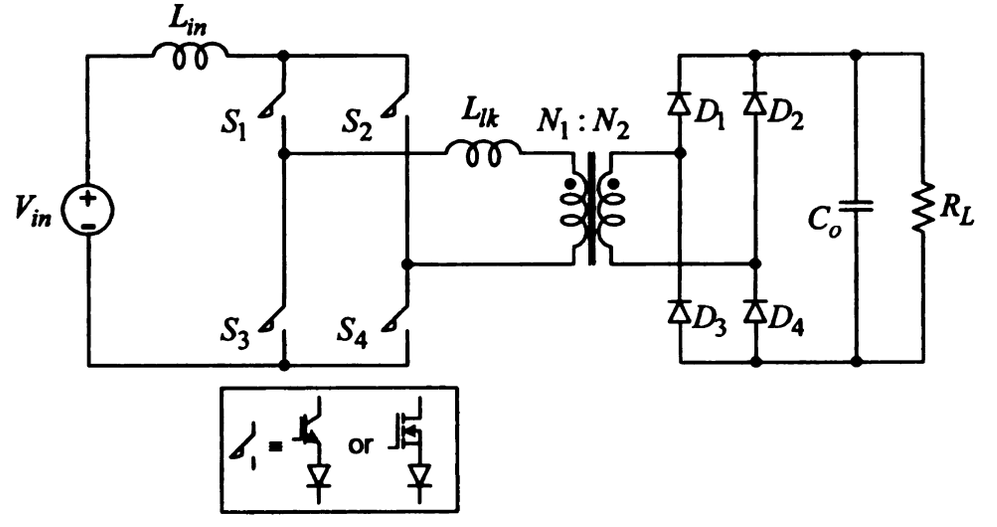

Figure 1-2 An I-source FB PWM DC-DC converter.

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Both structures have been used in many industry applications and have shown quite good performances. However, both converters have some conceptual limitations which will be explained later in this dissertation.

In order to overcome the limitations of the conventional bridge type converter shown in Figure 1-1 and Figure 1-2, a novel distributed Z-source network dc-dc converter is proposed in this dissertation

1.2. Scope of the dissertation

Based on the aforementioned problems in conventional V-source or I-source dc-dc converters, this dissertation is focused on the following subjects to increase converter efficiency, reliability, and power density.

Chapter 2 discusses the dc-dc converter using an energy recovery passive soft switching snubber circuit for a 210 kW auxiliary power supply for a metro vehicle.

Chapter 3 describes the 70 kW high power transformer and inductor design. Efforts are made to reduce copper loss in transformer windings. Optimum copper thickness that gives minimum copper loss is found.

Chapter 4 describes voltage oscillation problem in the secondary rectifier diodes. Classical snubber and energy recovery circuits are reviewed and problems are addressed. A new energy recovery clamp circuit is developed and its performances are compared with classical ones.

Chapter 5 analyzes power losses of the 70 kW dc-dc converter developed in this work and its losses are summarized.

Chapter 6 shows design and development of the integrated magnetics for a 3 phase interleaved boost converter for SHEB system. A very detailed design guideline is presented and the analytical results are compared with experimental results.

Chapter 7 proposes a distributed Z-source network. Its properties and characteristics are examined in great detail.

Chapter 8 presents novel dc-dc converter utilizing the distributed Z-source network. The operational principle of the proposed dc-dc converter is analyzed. Performances of the proposed dc-dc converter are verified experimentally.

Chapter 9 discusses future works that need to be done.

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Chapter 2. Design and Development of 210 kW DC-DC Converter for Auxiliary Power Supply for Metro Vehicle

2.1. System Topology and Ratings

The energy supplied to the low-voltage equipment in systems, such as metro vehicles, powered by a high dc voltage, typically goes through multiple power conversion stages. In general, the dc-dc-ac structure with a high frequency isolation transformer features many advantages over the traditional dc-ac structures with a 50/60 Hz transformer. The major advantages include lower cost, smaller size and less acoustic noise. Figure 2-1 shows the overall system configuration for an auxiliary power supply for metro vehicle.

The electric power is transmitted to a train from a high dc voltage overhead line (1000-2000 V) and is converted into intermediate dc voltage (750 V) which is then inverted into a 3-phase ac voltage (e.g. 380V, 60Hz). The ac voltage supplies power to various electrical loads in the train such as an air conditioner, air compressor, lighting, heating, and etc.

The dc-dc converter is the key part of the whole dc-dc-ac system. In this dissertation, the isolated dc-dc converter is divided into three modules as shown in Figure 2-1 in order to use standard 1200 V IGBTs because IGBTs rated over 1200 V usually have very high switching losses at switching frequencies higher than 10 kHz [2]. Therefore, each dc-dc converter module carries 70 kW power for a combined 210 kW output power rating.

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The primary sides of the dc-dc converters are connected in series to achieve high input voltage and the secondary sides are connected in parallel to generate high output current. Thus, each dc-dc converter accepts an input voltage of 333-666 Vdc, the output voltage is regulated to 750 Vdc with maximum current of 93 A. The design of one of the three dc-dc converter modules will be addressed in great detail in this chapter and chapter 3, 4 and 5

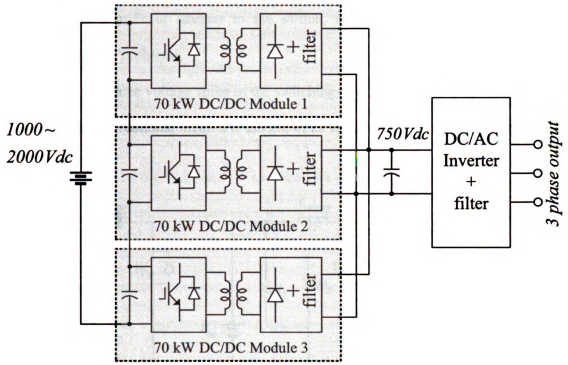

Figure 2-1 Overall system configuration for 260 kVA auxiliary power supply.

As shown in Figure 2-1, the 210 kW isolated dc-dc converter is divided into three 70 kW modules in order to use standard 1200 V IGBTs. As already mentioned in Chapter 1, the conventional transformer isolated dc-dc converter consists of either a V-source type or I-source type converter. In this work, a voltage source type FB PWM dc-dc converter is selected.

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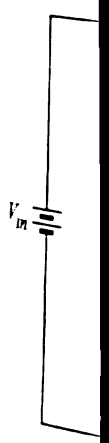

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2.2. Design of Isolated Full-Bridge DC-DC Converter

2.2.1 Energy Recovery Passive Snubber Circuit

High power and high frequency switching power converters experience high voltage oscillation/spike problems across the switching devices due to the inherent circuit stray inductances (L_{stray}) associated with the physical circuit layout [2, 3]. The high voltage spike presents significant stresses to the switch, increases loss and electromagnetic interference (EMI) problems.

In order to reduce voltage spike in the switching devices, several methods have been proposed. The conventional method is the use of an RCD clamp/snubber circuit as shown in Figure 2-2 [2].

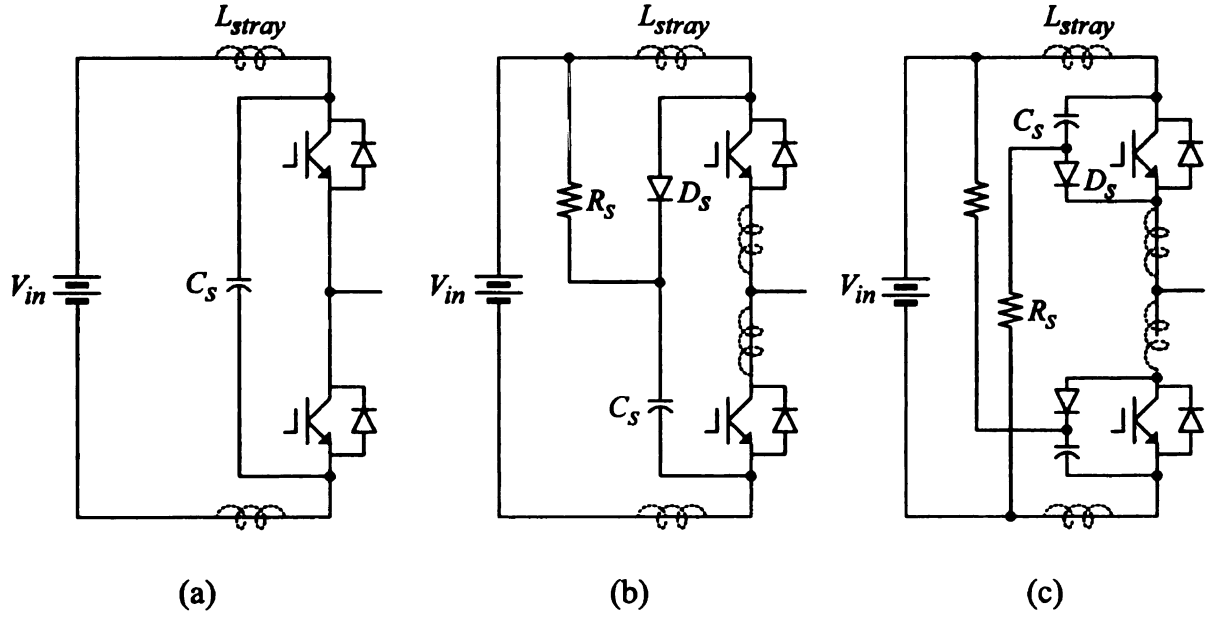

Figure 2-2 Common IGBT snubber circuits

Figure 2-2 (a) consists of a single low inductance film capacitor connected from C1 to E2 on a dual IGBT module or from P to N on a six pack IGBT module. In low power

designs, this snubber will often provide effective, low cost control of transient voltage. As power level increases, snubber circuit (a) may begin to ring with parasitic bus inductance, L_{stray} unless L_{stray} is not minimized. Snubber circuit (b) solves this problem by using a fast recovery diode to catch the transient voltage and block oscillations. As power rating of the system increases, however, dual IGBT modules or six pack modules may not be able to be used due to the IGBTs available in the market. In this case, L_{stray} between the top and bottom IGBT of a phase would be bigger than that of dual IGBT module or six pack modules because of physical layout. Therefore, the parasitic loop inductance of snubber (b) may become too high for it to effectively control transient voltage. In these high current applications, snubber circuit (c) is usually used. This snubber functions similar to snubber (b) but it has lower loop inductance than snubber (b) because it is connected directly to the collector and emitter of each IGBT. However, the power losses in snubber resistors, R_s, would be very high as the output power increases. As a result, it degrades system efficiency.

From the above results, it is obvious that L_{stray} between DC link capacitor and IGBT phase legs should be well minimized to reduce voltage spike in IGBT. In addition to that, L_{stray} between the top and bottom IGBT should be minimized as well to further reduce voltage spike in IGBT. One way among others that can effectively minimize L_{stray} between the top and bottom IGBTs of a phase is to use P-cell and N-cell structured IGBT. This IGBT structure has already been suggested by Dr. Fang Z. Peng in several previous literatures [4-6]. Added benefit of this structure is that it can also minimize L_{stray} between the DC link capacitor and IGBT phase leg, significantly. Recently,

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several semiconductor manufacturers are moving to the packaging based on the P- and N-cell structures [6].

Another conventional method is using phase-shifted PWM (PS-PWM). Soft switching operation is possible in PS-PWM by using transformer leakage inductance and intrinsic capacitance of switches without an additional circuitry [7, 8]. However, this topology requires that certain minimum commutation energy be stored in transformer leakage inductance. If this energy is insufficient, the incoming device turn-on, which is hard switched, leads to significant turn on loss due to the capacitor dump. In addition to this, PS-PWM suffers from large circulating current problem during freewheeling interval, which results in increased RMS current in switching devices and transformer. Therefore, it increases conduction loss in IGBT and transformer.

So far, a couple of zero-voltage and zero-current-switching (ZVZCS) full-bridge (FB) PWM converters have been presented and their primary currents are reset during freewheeling period using the auxiliary circuit in secondary side [9, 10]. However, voltage overshoot in the secondary rectifier diode could be very high when the converter input voltage varies in a wide range. Therefore, all those topologies mentioned above are not applicable to the system discussed in this dissertation.

Figure 2-3 shows overall circuit configuration of the 70 kW dc-dc converter developed in this work to overcome the aforementioned problems in both primary and secondary side. A passive snubber circuit, which consists of a diode/capacitor for each leg, and an energy recovery circuit shared by two phase legs, is used to reduce voltage spike and power loss in the IGBT. The snubber circuit includes a diode D_{sp} and a capacitor C_{sp} for the upper switching devices (S_1 and S_2), and symmetrically D_{sn} and

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C_{sn} for the lower switching devices (S_3 and S_4). The functions of the snubber diodes D_{sp} and D_{sn} and snubber capacitors C_{sp} and C_{sn} are very similar to those of the traditional RCD snubber shown in Figure 2-2.

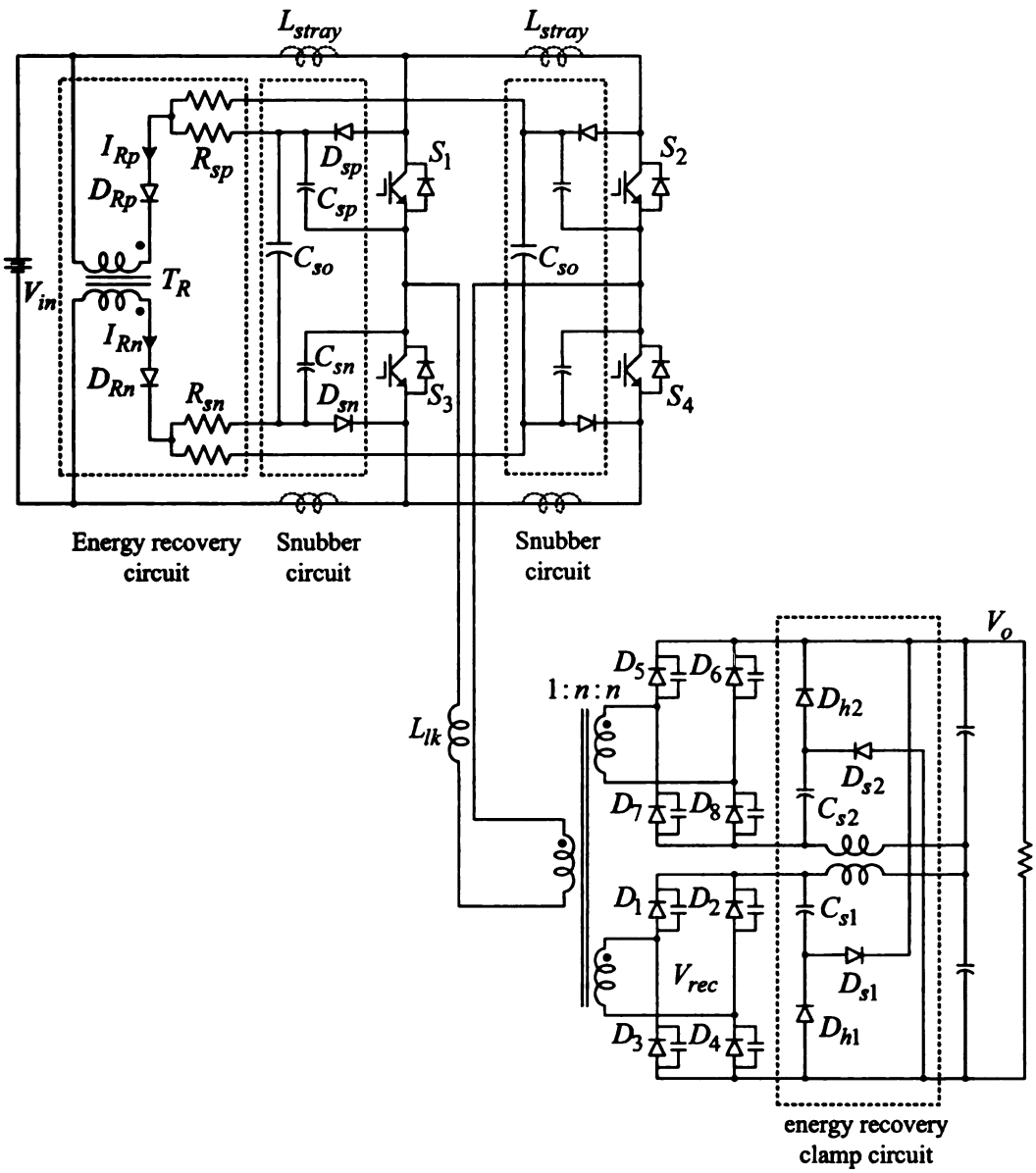

Figure 2-3 Overall schematic of 70 kW DC-DC converter

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They are, however, arranged differently so that both snubber capacitors are connected to the midpoint of the phase leg [11]. Therefore, the sum of both snubber capacitors' voltages should remain constant and equal to the DC link voltage, which is further guaranteed by a larger snubber capacitor C_{so} connected across the two snubber capacitors.

The energy recovery circuit that is shared by all the snubber circuits has two diodes D_{Rp} and D_{Rn}, two resistors R_{sp} and R_{sn}, and a transformer T_R. The two diodes, D_{Rp} and D_{Rn}, guarantee the energy recovery current (power) flows in one direction, i.e., from the snubber capacitors back to the DC link. The transformer T_R is connected like a common mode choke and thus presents a large inductance to loops I-IV as shown in Figure 2-4. The resistors R_{sp} and R_{sn} are used to further limit the circulating current in the loop I-IV.

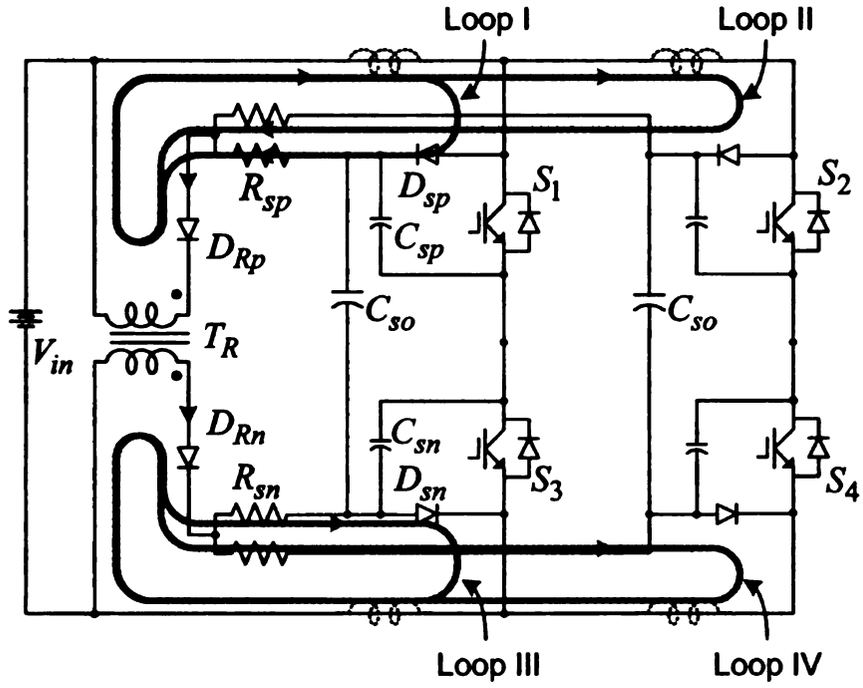

Figure 2-4 Energy recovery circuit

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2.2.2 Selection of PSSS and ERCC Parameters

Properly designed and selected snubber parameters are crucial to the performance of the dc-dc converter with passive soft switching snubber (PSSS) technology. The dv/dt and di/dt are determined by the snubber capacitors, C_{sp} and C_{sn}, stray inductance L_{stray}, and partially by the load current. Theoretically the capacitance C_{so} should be chosen as high as possible to lower the harmonics as well as the mean value of $V_{C_{so}}$, which contributes to limit both dv/dt and di/dt. In the development of the 70 kW dc-dc converter, we selected $0.47\,\mu F$ for C_{so}.

The selection of optimum snubber capacitors, C_{sp} and C_{sn}, are somewhat complex to calculate because they are related to busbar stray inductance, IGBT voltage overshoot and snubber diode power loss. When the snubber capacitors are big, for example, the IGBT overshoot and IGBT turn-off switching loss will be decreased. However, the power loss in snubber diodes will increase. Therefore, the optimum snubber capacitance can be determined through experiment in practice by considering IGBT voltage overshoot and power loss in the snubber diode. In this work, 30 nF capacitors are chosen for C_{sp} and C_{sn}. The resistors inserted in the energy recovery circuit are to reduce circulating current in the path shown in Figure 2-4. Theoretically, these resistors are not necessary in an energy recovery circuit because the transformer T_R has an airgap in its ferrite core, which imposes significant inductance in current loop I-IV. In this work, 8.6 Ω resistors are used for R_{sp} and R_{sn} to further reduce circulating current.

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2.2.3 Operational modes

The operational modes of leading leg switches in the duty cycle control method are shown in Figure 2-5. The lagging leg switch operation can be analogously explained.

Mode 1: S_1 and S_4 are on and input power is delivered to output. During this mode, V_{Csp} remains at zero and V_{Csn} is equal to V_{Css}.

Mode 2: S_1 and S_4 are turned off and snubber capacitor C_{sp} starts charging and C_{sn} starts discharging through snubber diode D_{sp}. By solving differential equations with initial conditions $V_{Csp}(0^-)=0$, $I_{Ls}(0^-)=I_o$ and $V_{Css}(0^-)=V_{in}$, V_{Csp} can be expressed as

$$V_{Csp}(t)=\frac{V_{in}}{2}-\left(\frac{V_{in}}{2}-V_{Csp}(0^-)\right)\cos(w_o t)+\frac{I_o}{w_o C_s}\sin(w_o t) \tag{2.1}$$

In (2.1), snubber capacitance $C_{sp}=C_{sn}=\frac{C_s}{2}$ and $w_o=\frac{1}{\sqrt{2L_sC_s}}$ is resonant frequency.

Mode 3: When V_{Csp} reaches V_{Css} and V_{Csn} becomes zero, the diode D_{sn} and D_3 start conducting. Therefore, the upper snubber capacitor voltage V_{Csp} can be clamped to V_{Css}. After this mode, there is a resonance between transformer leakage inductance (L_{lk}) and snubber capacitance until current in the transformer leakage inductance decreases to zero. As a result, snubber capacitor voltage V_{Csp} and V_{Csn} is maintained at half of the input voltage.

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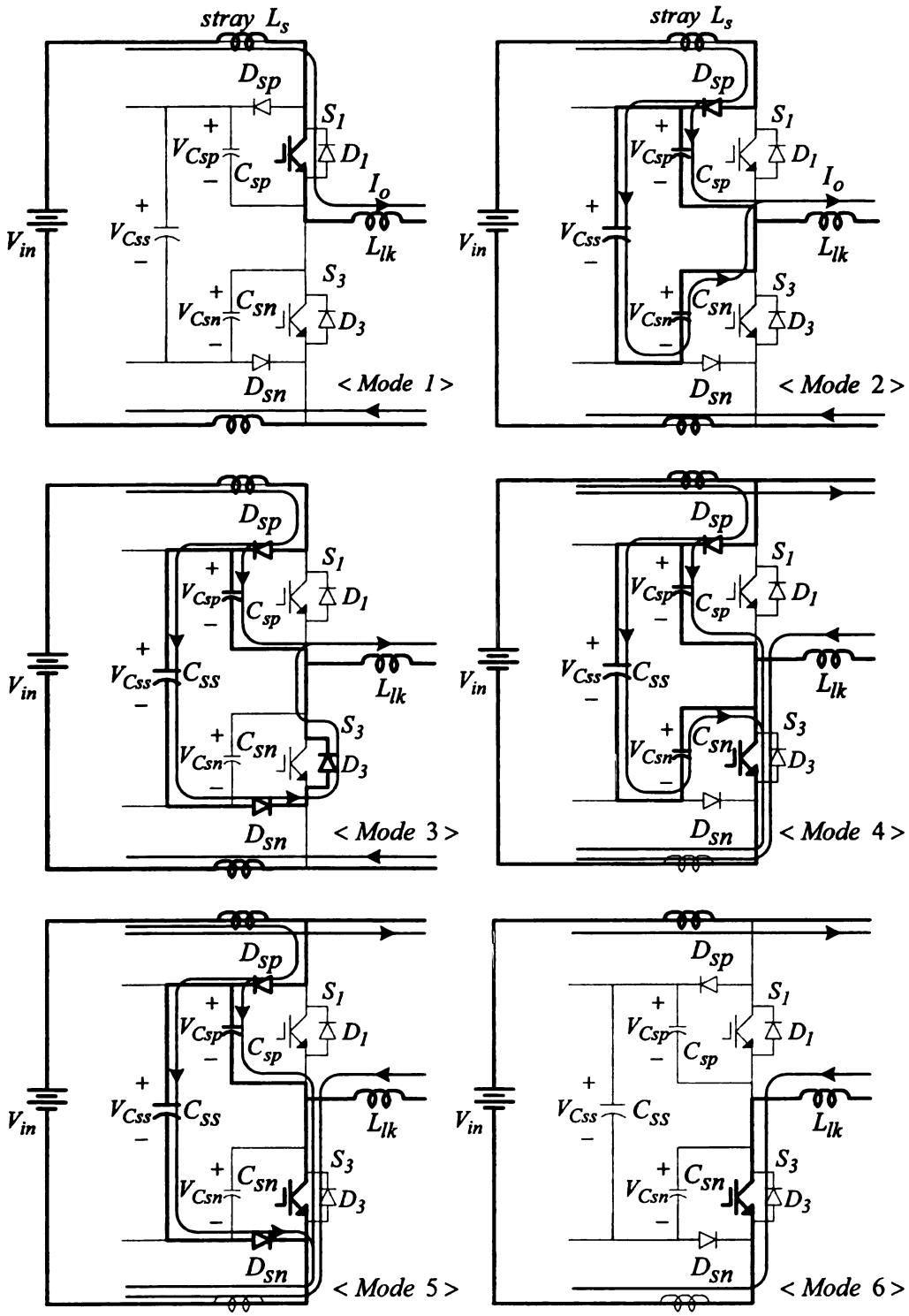

Figure 2-5 Operational modes of dc-dc converter.

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Mode 4: S_2 and S_3 are turned on and S_3 carries load current $-I_o$. As the same operation in mode 2, snubber capacitor C_{sp} starts charging and C_{sn} starts discharging again through snubber diode D_{sp} and this causes additional current flow in switch S_3. As a result, there is an additional power loss incurred by capacitive turn on. With the initial conditions $V_{Csp}(0^-) = \frac{V_{in}}{2}$, $I_{Ls}(0^-) = 0$ and $V_{Css}(0^-) = V_{in}$, ,and, V_{Csp} can be expressed as

$$V_{Csp}(t) = V_{in} - \left(V_{in} - \frac{V_{in}}{2}\right)\cos(w_o t) \tag{2.2}$$

Mode 5: The operation of this mode is quite similar to mode 3 except that snubber capacitor charging and discharging current flows through S_3 instead of body diode D_3. Therefore, the upper snubber capacitor voltage V_{Csp} is clamped to V_{Css} again.

Mode 6: S_3 carries only load current.

2.2.4 Selection of PWM Control Method

The full bridge converter shown in Figure 2-3 can be operated by a duty cycle control or phase shift PWM (PSPWM) control. In this work, duty cycle control is chosen because transformer leakage inductance is minimized due to the following reasons.

1) A double interleaved winding method, which is explained later in chapter 3, is used to reduce the proximity effect in transformer winding and this winding method reduces transformer leakage inductance by a factor of 4 [12].

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2) A large leakage inductance decreases the effective duty cycle in the secondary rectified voltage, V_{sec} (see Figure 2-3), therefore, requiring a larger transformer turns ratio to compensate for the reduced duty cycle, which eventually increases voltage stress of the secondary rectifier diodes [13], [14]. Therefore, power loss in the secondary snubber (or clamp) circuit will be increased. In this work, measured transformer leakage inductance in the primary side is around $0.25\,\mu H$.

Figure 2-6 and Figure 2-7 depict the IGBT switching (V_{ce}) and transformer primary current (i_{tr}) waveforms for both duty cycle and PS-PWM control methods. Table 2.1 compares power loss in the IGBT and transformer based on the assumption that the transformer leakage inductance is not sufficient to achieve zero voltage switching (ZVS) at the leading leg switches.

As shown in Table 2-1, turn-on and turn-off losses in the IGBT are same with both duty cycle and PS-PWM control methods. However, duty cycle control has lower capacitive turn-on loss and conduction loss than PS-PWM because the voltage across the device is half of the input voltage during the turn-on and turn-off transitions. It also has negligible circulating current during free-wheeling period because leakage inductance of the transformer is very small.

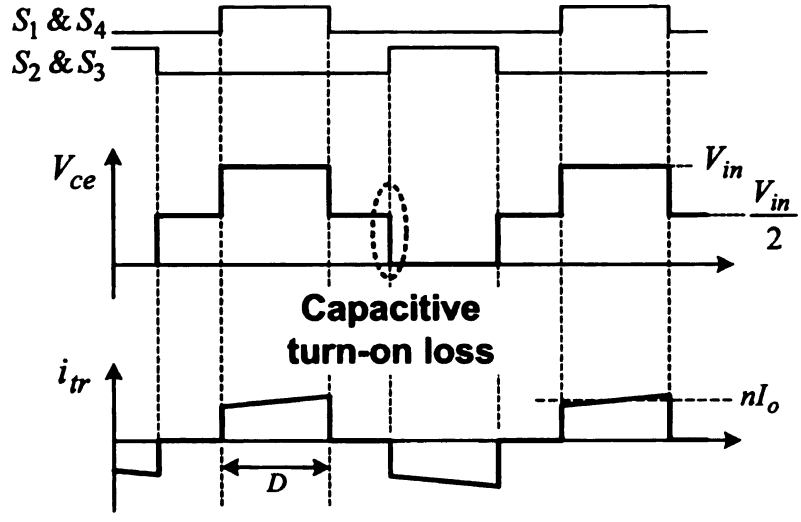

Figure 2-6 Duty cycle control

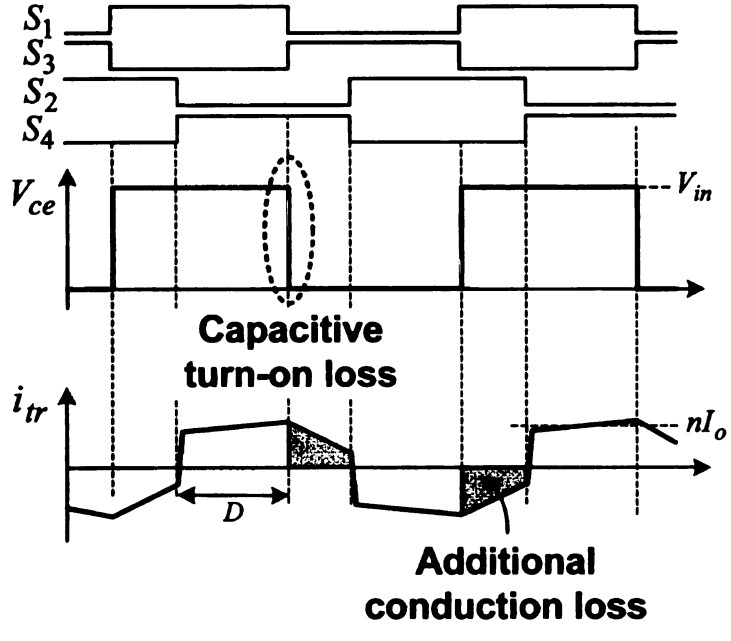

Figure 2-7 Phase-shift PWM control

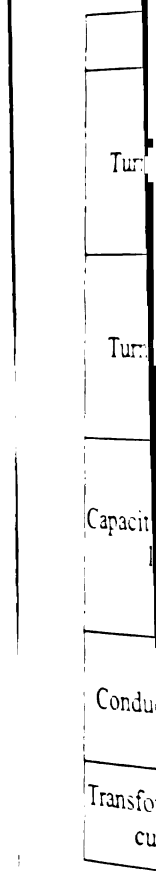

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Table 2-1 Comparison of Power Loss

	Duty cycle control	Phase-shift PWM control
Turn-on loss	$\left(E_{on} \cdot \frac{\frac{V_{in}}{2}}{V_{cc}} \cdot f_{sw} \right) \cdot 4$	$\left(E_{on} \cdot \frac{V_{in}}{V_{cc}} \cdot f_{sw} \right) \cdot 2$
Turn-off loss	$\left(E_{off} \cdot \frac{\frac{V_{in}}{2}}{V_{cc}} \cdot f_{sw} \right) \cdot 4$	$\left(E_{off} \cdot \frac{V_{in}}{V_{cc}} \cdot f_{sw} \right) \cdot 2$
Capacitive turn-on loss	$\left(\frac{1}{2} \cdot (2C_s) \cdot \left(\frac{V_{in}}{2} \right)^2 \cdot f_{sw} \right) \cdot 4 = C_s \cdot V_{in}{}^2 \cdot f_{sw}$	$\left(\frac{1}{2} \cdot (2C_s) \cdot V_{in}{}^2 \cdot f_{sw} \right) \cdot 2 = 2 \cdot C_s \cdot V_{in}{}^2 \cdot f_{sw}$
Conduction loss	$(v_{ce\_sat} \cdot nI_o \cdot D) \cdot 4$	$(v_{ce\_sat} \cdot nI_o \cdot D) \cdot 4$ + additional conduction loss
Transformer RMS current	$nI_o \cdot \sqrt{D}$	$nI_o \cdot \sqrt{D} < i_{tr\_rms} < nI_o$

* E_{on}, E_{off} : switching energy of IGBT under the test condition of $V_{cc} = 600V$, n : transformer turns ratio, I_o : Output current

** $C_s = C_{sp} = C_{sn}$

2.3. Experimental Results

The 70 kW dc-dc converter using energy recovery passive snubber circuit has been built and tested to verify the principle of operation. Figure 2-8 shows the experimental waveforms of primary transformer current and the IGBT collector-emitter voltage (V_{ce})

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Figure 2-9

waveforms of the dc-dc converter developed in this work under the test condition of $V_{in} = 666V$, $V_o = 750\ V$, $P_o = 70\ kW$ and $f_s = 13\ kHz$.

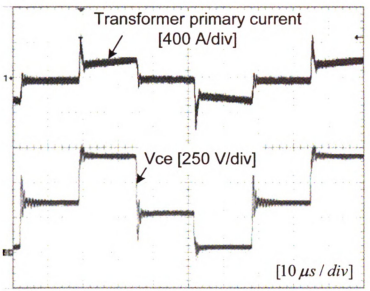

Figure 2-8 Transformer primary current and IGBT voltage waveforms

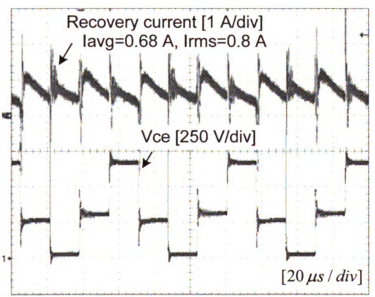

Figure 2-9 Recovery current in primary snubber resistor and IGBT voltage waveform.

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As shown in Figure 2-8, voltage spike in the IGBT was well clamped to approximately 1.2 times of the input voltage.

Figure 2-9 shows the recovery current waveform of the primary snubber resistor (R_{sp} and R_{sn}) and is synchronized with the V_{ce} waveform. With input voltage of 666 V, the measured RMS and average current in each snubber resistor was 0.8 A and 0.68 A, respectively. Thus, the total amount of power recovered to the DC link through the energy recovery circuit can be calculated as $(2\times 0.68)\times 666 = 906W$, while the total power losses in the snubber resistors were only $(0.8^2\times 8.6)\times 4 = 22W$ at full-load operation.

2.4. Conclusion

In this chapter, an energy recovery passive snubber circuit is proposed to reduce EMI, voltage overshoot, and switching loss of the semiconductor devices. A duty cycle and phase-shifted PWM control method are compared to analyze power loss of the switching devices. Operating modes of the passive snubber circuit is explained and the design criteria for selecting snubber parameters are presented. The experimental results are measured to show performance of the energy recovery snubber circuit.

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Chapter 3. High Power Transformer and Inductor Design

3.1. Losses in Magnetics

A transformer is a device that transfers electrical energy from one circuit to another through inductively coupled conductors—the transformer's coils. Unfortunately, not all of this energy is recoverable in electrical form: a fraction is lost as heat [15]. Figure 3-1 shows the general losses of magnetic devices such as transformers and inductors. In general, the losses in magnetic device are consisted of core loss and winding loss. For the transformers designed with ferrite cores, the eddy current loss is almost negligible because the resistivity of ferrite core is much higher than other materials [16]. Therefore, the eddy current loss in core is not considered in this work.

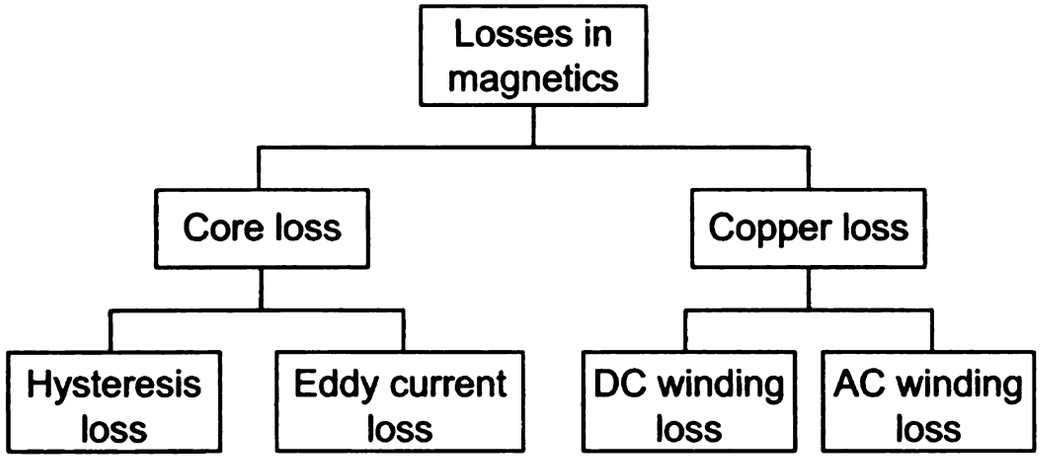

Figure 3-1 Losses in Magnetics.

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3.2. Transformer design

3.2.1 Core loss

Core loss is caused by the energy required to effect a change in the magnetization of a core material. This power loss can be observed electrically as hysteresis of the B-H loop [15]. For a high frequency and high power transformer, the core selection and structure design face many difficulties.

In this work, 6 pairs of U93/76/30-3C90 ferrite cores are used to achieve high power rating. The number of turns in the primary winding is 6 turns and the secondary winding is 14 turns considering input and output voltage range and duty cycle loss. Figure 3-2 shows a test setup for the transformer core loss measurement. To measure core loss, the transformer secondary winding is open circuited and a square voltage waveform is applied in the primary winding to magnetize the core.

In general, the core loss can be represented by a resistance R_c because the core flux is proportional to the applied voltage. L_m represents magnetizing inductance of the transformer. A core with finite permeability requires a magnetizing current I_{L_m} to maintain mutual flux in the core. Therefore, the transformer primary current I_{pri} is the sum of I_{R_c} and I_{L_m}. In Figure 3-2, transformer leakage inductance and winding resistance are not included in the transformer model to make analysis simple.

Figure 3-3 shows theoretical waveforms of the transformer current and voltage when core loss in considered. When the transformer voltage changes polarity from positive to negative, there is a drop in transformer current waveform which is labeled as $2I_x$. This is

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the indication of core loss in the transformer. In addition to this, the transformer voltage and current are not 90 degree apart. Instead, there is a phase difference labeled as δ in Figure 3-3. This is another indication of core loss in the transformer.

In this work, core loss is measured by integrating the product of voltage and current on the winding by using an oscilloscope and the resultant waveforms are shown in Figure 3-4. The measured core loss was around 110 W.

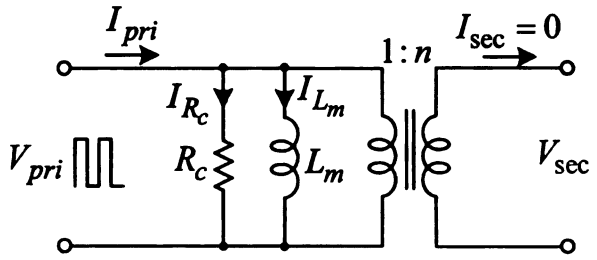

Figure 3-2 Core loss measurement

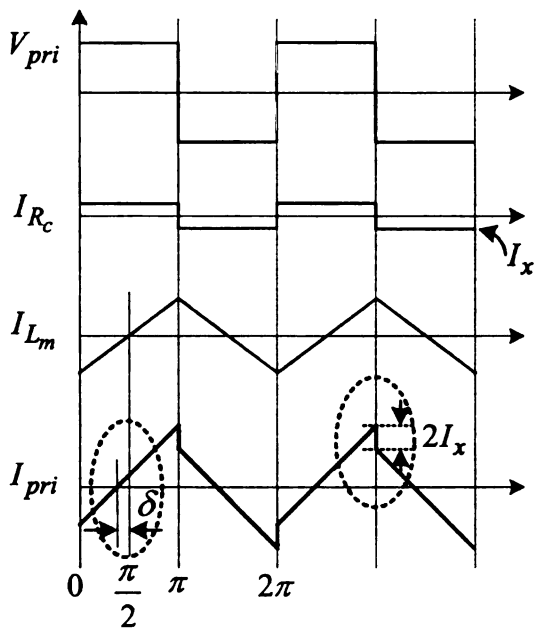

Figure 3-3 Transformer voltage and current waveforms with secondary side open-circuited

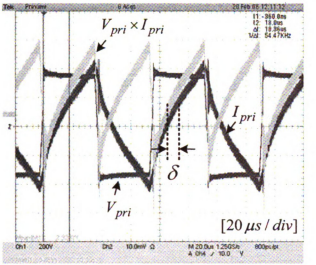

Figure 3-4 Core loss measurement waveforms

On the other hand, transformer core loss can also be found by using the core loss curve provided by the manufacture [17]. Figure 3-5 shows the calculated core loss density (P_c) in kW / m^3 of the 3C90 ferrite material plotted against flux density ($\frac{\Delta B}{2}$) and frequency (f_{sw}) with sinusoidal excitation.

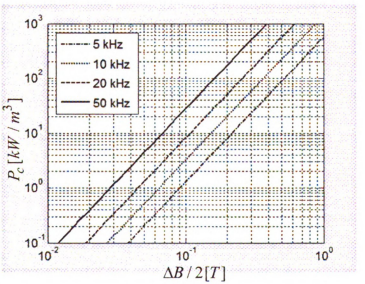

Figure 3-5 Core loss curves for 3C90 material.

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From the core loss curves, we can derive the core loss equation for 3C90 material as (3.1).

$$P_{core} = 65.3 \times (f_{sw}/1000)^{1.36} \times \left(\frac{\Delta B}{2}\right)^{2.64} \quad [kW/m^3] \tag{3.1}$$

By choosing 6 turns for the primary winding and the resultant magnetizing inductance (L_m) was $1.7\,mH$. Flux swing (ΔB) of the transformer can also be calculated as follows

$$\Delta B = \frac{V_{in} \times T_{on}}{N_p \times A_e} = 0.424\,T \tag{3.2}$$

where, $T_{on} = 38.5\ \mu s$, $A_e = 50.4\ cm^2$

From (3.1), (3.2) and by multiplying total core volume (V_e) of the transformer to (3.1), the calculated core loss becomes (3.3).

$$P_{core} = 65.3 \times (f_{sw}/1000)^{1.36} \times B^{2.64} \times V_e = 101W \tag{3.3}$$

where, $f_{sw} = 13\ kHz$, $B = 1.11 \times \frac{\Delta B}{2}$, $V_e = 1782000\ mm^3$

The core loss calculated in (3.3) is close to the measured value.

3.2.2 Winding (Copper) loss

The skin effect increases resistance and copper loss in the conductors since high-frequency currents do not penetrate to the center of the conductor. Thus, the effective

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wire cross-sectional area is reduced which results in increased ac resistance (R_{ac}) [15], [18].

Dowell solved this problem for sinusoidal waveforms in his 1966 paper [19]. However, skin effect alone is not sufficient to explain the increased high-frequency copper losses observed in multiple-layer transformer windings. A conductor that carries a high-frequency current induces copper loss in an adjacent conductor by a phenomenon known as the proximity effect [12], [15], [19-22]. In a multiple layer winding, especially for foil windings, the proximity effect is the main efficiency killer of high frequency transformers because R_{ac} caused by the proximity effect increases greatly as the number of layers increases.

An arbitrary periodic current waveform is represented by its Fourier series and all the harmonic components are orthogonal so that the total power loss is equal to the sum of the losses calculated by Dowell's formula for the amplitude and frequency of each harmonic in turn. Therefore, the total power loss due to all the harmonics is expressed as

$$P = \overline{R_{dc}} I_{dc}^2 + \overline{R_{dc}} \sum_{n=1}^{\infty} \overline{F_R} I_n^2 \tag{3.4}$$

where $\overline{R_{dc}}$ is dc winding resistance/turn, I_{dc} is the dc component of current, n is harmonic number, and I_n is the RMS value of the nth harmonic. For the transformer winding, the first term in (3.4) becomes zero because there is no dc component in current. $\overline{F_R}$ is expressed as

$$\overline{F_R} = \sqrt{n}\varphi\left[(2m^2 - 2m + 1)G_1(\sqrt{n}\varphi) - 4m(m-1)G_2(\sqrt{n}\varphi)\right] \tag{3.5}$$

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In (3.5), φ is the ratio of the layer (copper) thickness h to the skin depth δ, $G_1(\sqrt{n\varphi})$ and $G_2(\sqrt{n\varphi})$ are expressed as follows

$$G_1(\sqrt{n\varphi}) = \frac{\sinh(2\sqrt{n\varphi}) + \sin(2\sqrt{n\varphi})}{\cosh(2\sqrt{n\varphi}) - \cos(2\sqrt{n\varphi})} \tag{3.6}$$

$$G_2(\sqrt{n\varphi}) = \frac{\sinh(\sqrt{n\varphi})\cos(\sqrt{n\varphi}) + \cosh(\sqrt{n\varphi})\sin(\sqrt{n\varphi})}{\cosh(2\sqrt{n\varphi}) - \cos(2\sqrt{n\varphi})} \tag{3.7}$$

The value for m in (3.5) is defined as follows.

$$m = \frac{F(h)}{F(h) - F(0)} \tag{3.8}$$

where, $F(0)$ and $F(h)$ are the magneto-motive-force (MMF) for the left and right sides of the layer of thickness h [15]. To calculate the total power loss in an M layer winding, F_R is found by summation $\overline{F_R}$ over all of the layers as

$$F_R = \sum_{m=1}^{M} \overline{F_R} = \sum_{m=1}^{M} \sqrt{n\varphi}\left[(2m^2 - 2m + 1)G_1(\sqrt{n\varphi}) - 4m(m-1)G_2(\sqrt{n\varphi})\right] \tag{3.9}$$

With the help of identities expressed in (3.10) and (3.11), (3.9) can be rewritten as (3.12) [15]

$$\sum_{m=1}^{M} m = \frac{M(M+1)}{2} \tag{3.10}$$

$$\sum_{m=1}^{M} m^2 = \frac{M(M+1)(2M+1)}{6} \tag{3.11}$$

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$$F_R = M\sqrt{n\varphi}\left[G_1(\sqrt{n\varphi}) + \frac{2}{3}(M^2-1)\left(G_1(\sqrt{n\varphi}) - 2G_2(\sqrt{n\varphi})\right)\right] \quad (3.12)$$

Therefore, the total power loss in an M layer winding is expressed as

$$P_{total} = R_{dc}\sum_{n=1}^{\infty} I_n^2\sqrt{n\varphi}\left[G_1(\sqrt{n\varphi}) + \frac{2}{3}(M^2-1)\left(G_1(\sqrt{n\varphi}) - 2G_2(\sqrt{n\varphi})\right)\right] \quad (3.13)$$

,where R_{dc} is the total dc winding resistance in an M layer winding and is equal to $R_{dc} = M\overline{R_{dc}}$.

In this work, copper foil is used rather than litz wire because transformer size can be reduced by using copper foil because higher fill factor than litz wire can be achieved. Added benefits of using copper foil are better heat transfer capabilities than those wound with litz wire especially for air cooled transformers, and low leakage inductance.

To reduce the proximity effect mentioned above, the number of layers should be reduced by breaking up the windings into smaller sections through interleaving.

Figure 3-6 shows the winding geometry and MMF waveform in the window region of the core with single interleaved winding. The 6 primary turns are split into two sets of 3 turns which sandwich the 14 secondary turns.

To calculate the m values for each layer, it is assumed that the transformer primary winding carries current i. Therefore, $\frac{3}{7}i\left(=\frac{N_p}{N_S}i\right)$ current flows through the secondary winding. In the leftmost primary winding of Figure 3-6, the layer carries current i. The MMF changes from 0 to i. The m value for this layer is found by using the definition shown in (3.8) as.

$$m = \frac{F(h)}{F(h) - F(0)} = \frac{i}{i - 0} = 1 \tag{3.14}$$

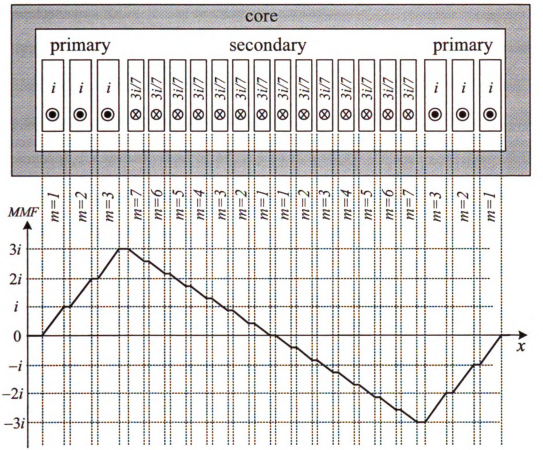

Figure 3-6 Winding arrangement and MMF waveform in transformer with single interleaved winding

For the leftmost secondary winding of Figure 3-6, the layer carries current $\frac{3}{7}i$ and the MMF changes from $3i$ to $(3i - \frac{3}{7}i)$. It should be noted that the roles of $F(0)$ and $F(h)$ can be interchanged when $F(0)$ is greater than $F(h)$ [15]. Therefore, the value m for this layer can be calculated as

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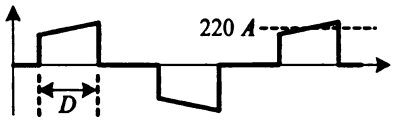
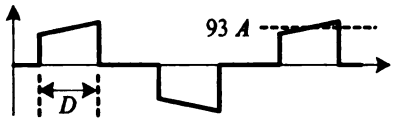
$$m = \frac{F(0)}{F(0) - F(h)} = \frac{3i}{3i - (3i - 3i/7)} = 7 \tag{3.15}$$

All the values for m in can be calculated similarly.

Table 3-1 lists the transformer current waveforms in both primary and secondary windings and the electrical parameters of copper foil used to calculate winding loss. By using the equation (3.13) and the electrical parameters listed in Table 3-1, total power loss versus φ, for several values of M, is plotted in Figure 3-7 and Figure 3-8. The total power loss is calculated up to the 29th harmonics of current. With the switching frequency of 13 kHz, the skin depth at 100 $°C$ is calculated as

$$\delta = \frac{7.5}{\sqrt{f}}[cm] = \frac{75}{\sqrt{13000}} = 0.658 \ mm \tag{3.16}$$

Table 3-1 Current Waveform and Electrical Parameter of Copper Foil.

Vin=500, D=0.32, Po=70 kW, fs=13 kHz	
Primary current	
Secondary current	
Copper width	100 mm
Insulation	0.13 mm Nomex paper
Mean length / turn	460 mm

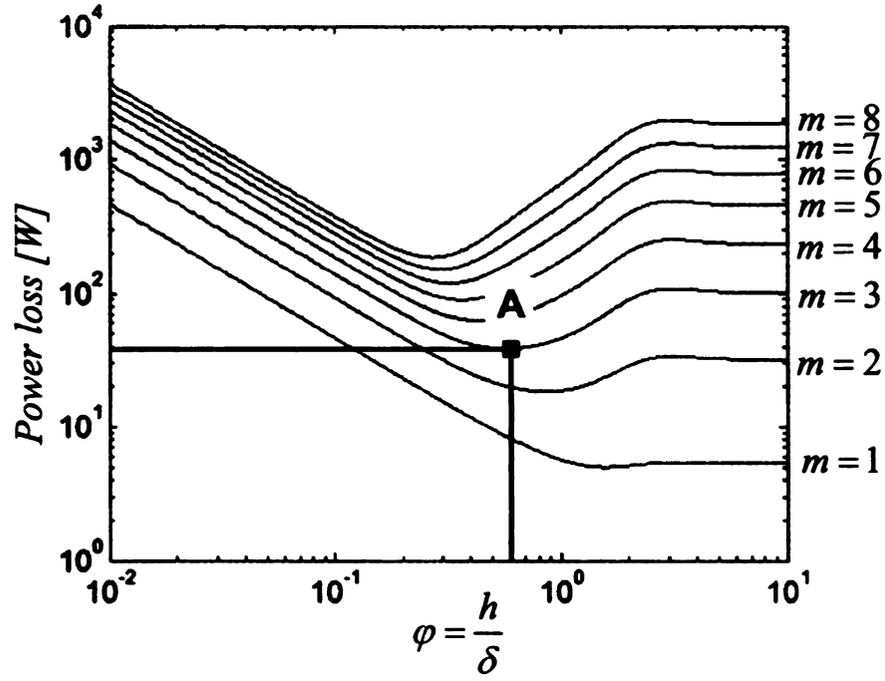


Figure 3-7 Primary winding loss in single interleaved winding.

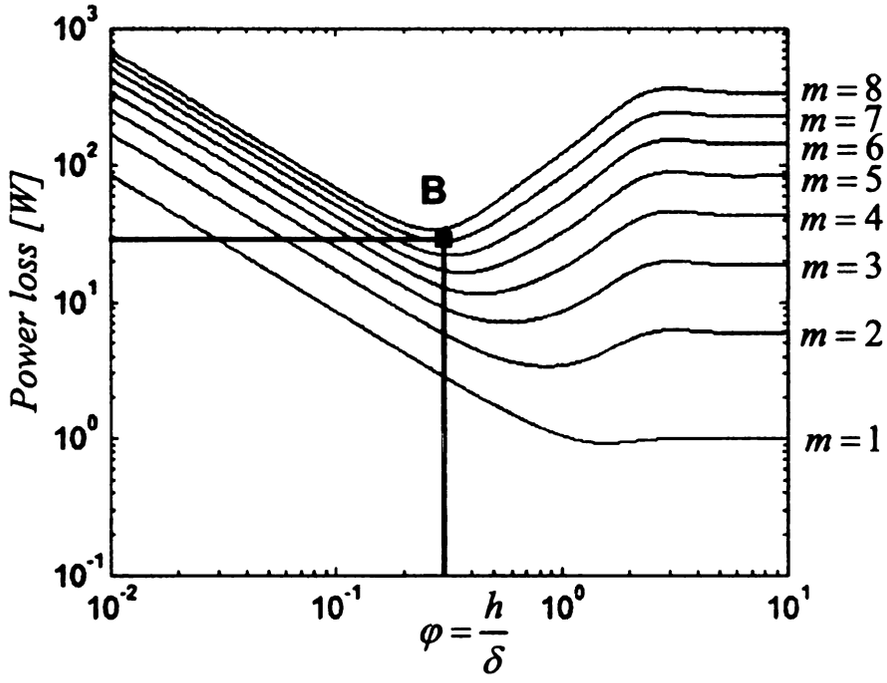


Figure 3-8 Secondary winding loss in single interleaved winding.

As shown in Figure 3-7 and Figure 3-8, the total winding loss increases greatly due to the proximity effect as M increases. Larger copper loss is obtained for small φ simply because the layer is thin and hence the dc resistance of the layer is large. For large M and φ, the proximity effect leads to large power loss. Between these extremes, there is a value of φ which minimizes the layer copper loss [15]. When the ac resistance of a copper foil is too high because the copper thickness is too great, it is tempting to simply subdivide it into several thinner strips, insulated from each other. It should be noted that this does not work unless they are twisted like litz wire [12]. From the result of Figure 3-7 for $M = 3$, the first half of the primary windings yield a minimum power loss of 40 W at $\varphi = 0.6$ (point "A"). Similarly, from Figure 3-8 for $M = 7$, the first half of the secondary windings yield a minimum power loss of 30 W at $\varphi = 0.3$ (point "B"). As a result, total minimum power loss in the transformer winding is $2 \times (40 + 30) = 140W$.

In this work, the transformer winding is interleaved again to further reduce power loss and the resultant winding geometry and MMF waveform are shown in Figure 3-9

The 6 primary turns are split into 3 sets of 2 turns. Again the 14 secondary turns are sandwiched evenly between the primary turns. The m values are calculated using the same method used for single interleaved winding. For the leftmost secondary winding of Figure 3-9, for example, the layer carries current $\frac{3}{7}i$ and the MMF changes from $2i$ to $(2i - \frac{3}{7}i)$. Therefore, the m value for this layer is

$$m = \frac{F(0)}{F(0) - F(h)} = \frac{2i}{2i - (2i - 3i/7)} = \frac{14}{3} \tag{3.17}$$

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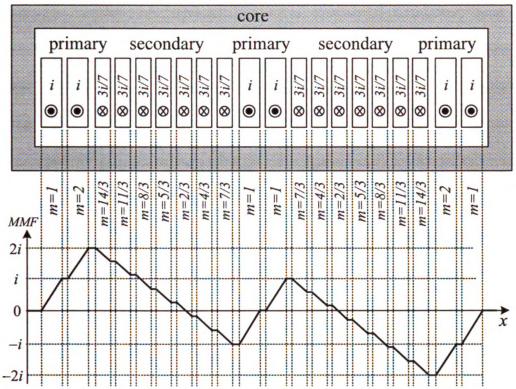

Figure 3-9 Winding arrangement and MMF waveform in transformer with double interleaved winding

All m values for the primary and secondary winding in Figure 3-9 can be calculated similarly. However, m values for the secondary winding in this case are not integers. Therefore, we cannot use equation (3.13) to calculate the total power loss in an M layer winding because (3.13) is derived by using (3.10) and (3.11) which are only valid for integers. In order to find the total power loss when m is not integers, the power loss versus φ is first plotted for each layer using (3.5) and the m values in Figure 3-9

Then the power loss in each layer is simply added together to plot the total power loss versus φ. The total power loss and optimum layer thickness can be found and the results are shown in Figure 3-10 and Figure 3-11.

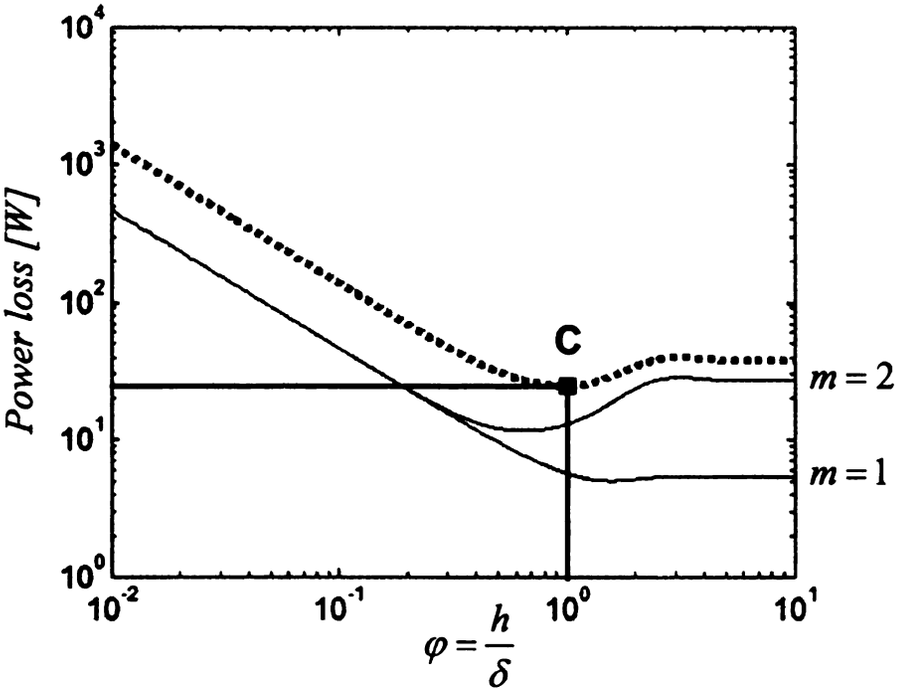

Figure 3-10 Primary winding loss in double interleaved winding

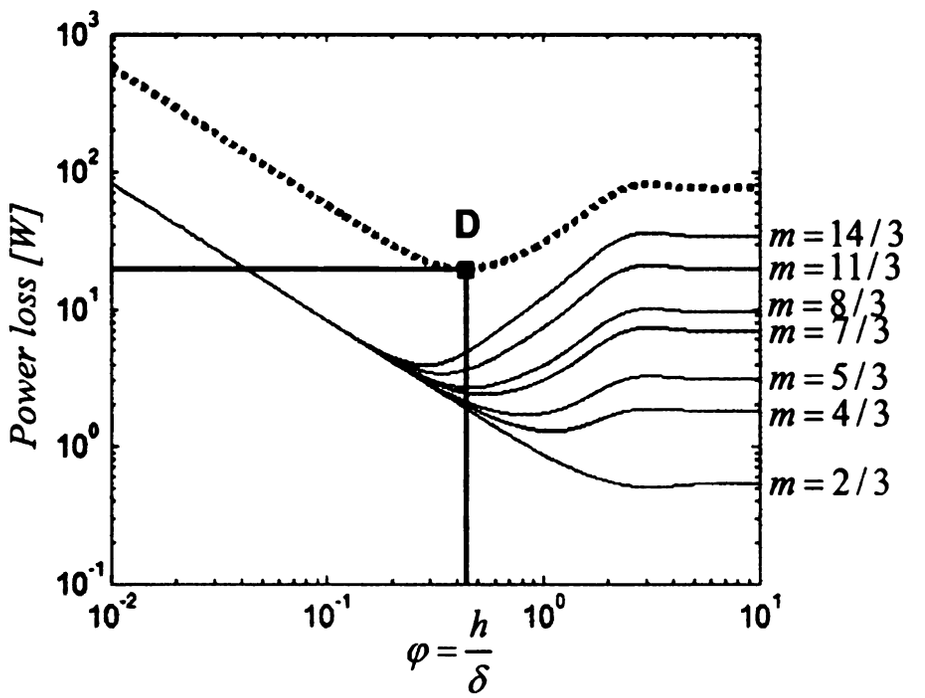

Figure 3-11 Secondary winding loss in double interleaved winding

The power loss in each layer is plotted (solid line) and is added to plot the total power loss (dotted line). From the result of Figure 3-10, the first half of minimum power loss in the primary winding occurs at point "C" where the power loss is 26 W at $\varphi = 1.0$. Likewise, from Figure 3-11, the first half of minimum power loss in the secondary winding occurs at point "D" where the power loss is 20 W at $\varphi = 0.45$. Therefore, total power loss in both the primary and secondary winding is $2 \times (26 + 20) = 92W$. Compared with single interleaved winding, there is 35 % reduction in winding loss. With the skin depth value calculated in (3.16), the copper (layer) thickness in both the primary and secondary winding can be calculated as follows

$$\varphi_{pri.} = \frac{h}{\delta} \rightarrow h = \varphi_{pri.} \times \delta = 1 \times 0.658 \cong 0.658 \ mm \tag{3.18}$$

$$\varphi_{\text{sec.}} = \frac{h}{\delta} \rightarrow h = \varphi_{\text{sec.}} \times \delta = 0.45 \times 0.658 \cong 0.296 \ mm \tag{3.19}$$

From Figure 3-6 to Figure 3-11, the double interleaved winding has lower copper loss than the single interleaved winding. It also decreases transformer leakage inductance since the peak value of MMF in double interleaved winding is less than the value of the single interleaved winding. Reduced leakage inductance is helpful in minimizing voltage overshoot in the rectifier diodes. In this dissertation, a standard 0.6 mm and 0.4 mm thickness copper foil are used for primary winding and secondary winding, respectively.

Figure 3-12 and Figure 3-13 show 3-D pictures of the 70 kW transformer designed in this work. After assembled with ferrite cores, the transformer was molded in an aluminum case to prevent the transformer from vibration and other possible mechanical stresses. Finally, the transformer is mounted on the main heatsink for heat dissipation.

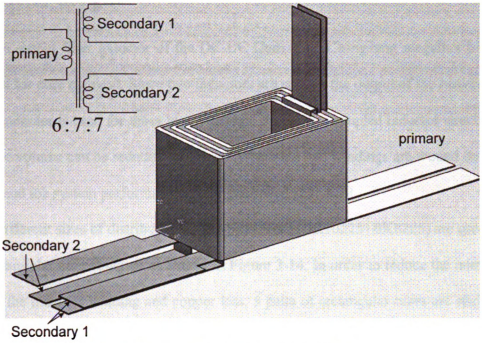

Figure 3-12 Transformer winding geometry

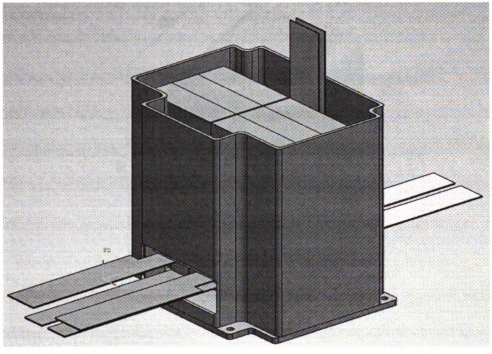

Figure 3-13 Transformer assembled with core and housed in aluminum case

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3.3. Inductor design

For the output filter inductor of the DC-DC Converter, Changsung megaflux block core is used for core material. Since two inductors are used in the output of the converter, a coupled inductor is used for those two windings. By using a coupled inductor structure, the inductor volume can be reduced significantly because two windings are wound on the same core and the system performance can be improved [23], [24].

Two different sizes of distributed air-gap block core (BK10225+BK8225) are used to form a rectangular core structure as shown in Figure 3-14. In order to reduce the number of turns in the inductor winding and copper loss, 5 pairs of rectangular cores are stacked together. Table 3-2 shows the detailed information of the coupled inductor designed in this work.

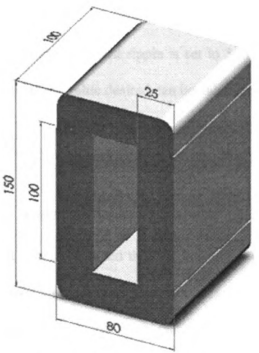

Figure 3-14 Block core assembly

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Table 3-2 Coupled inductor design parameters.

Core Unit	Assembled core [W×L×H mm]	AL value [nH/N^2]	Magnetic path length [cm]	Core cross-sectional area [cm^2]	Window area [cm^2]	Volume [cm^3]
BK10225-10 pcs + BK8225-10pcs	80×150×100	362	33.85	25	30	891

3.3.1 Inductance Calculation by Permeability vs. DC Bias Curves

In this work the output inductor value was calculated with maximum input voltage because inductor current ripple is maximum at this condition if output voltage is regulated (constant). The inductor current ripple is set to 30 % of output current in this design. Therefore, the inductance value desired can be calculated easily as

$$L = \frac{V_L}{\Delta I} \times DT_s = \frac{(nV_{in} - V_o)}{\Delta I} \times DT_s = \frac{2.33 \times 666 - 750}{0.3 \times 93 \times 26000} \times \frac{750}{2.33 \times 666} = 534\,\mu H \quad (3.20)$$

,where V_L is voltage across the inductor, D is duty cycle, T_s is period and ΔI is inductor current ripple. It should be noted that the inductance calculated in (3.20) is the inductance value when two inductor windings are connected in series. Therefore, the inductance value measured at one side with the other side open-circuited would be $534\,\mu H / 4 = 133.5\,\mu H$.

As already shown in Figure 3-14, 5 pairs of block core are stacked together to increase core cross-sectional area (A_e) and to reduce the number of turns. With this core configuration, the A_L value was 362 [nH / N^2] and 23 T is wound in each winding of the coupled inductor. From the A_L values and number of turns, the inductance can be calculated as follows.

$$L_{@0A} = 362\ nH \times 46^2 = 766\ \mu H \tag{3.21}$$

The inductance calculated in (3.21) is the inductance value at 0 A. As current increases, however, the inductance value decreases because permeability of the core decreases. This is a typical characteristic of power (or distributed airgap) core which is different from ferrite core.

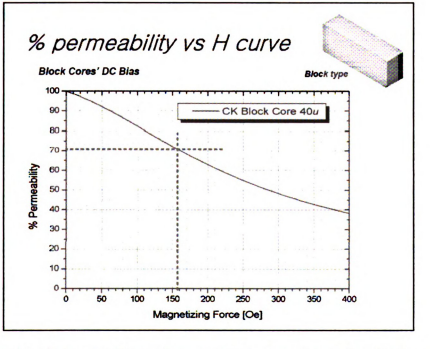

Figure 3-15 % permeability vs H curve of Changsung megaflux block core

Figure 3-15 shows the change in core permeability as magnetizing force (H) increases. To determine H in Figure 3-15, Ampere's law is applied as

$$H = \frac{\mu_o NI}{l_m} = \frac{0.4\pi \times 46 \times 93}{33.85} = 158.8\,[O_e] \tag{3.22}$$

Once H is found, % permeability of the core can be estimated from the curve shown in Figure 3-15. According to the H value calculated in (3.22) and Figure 3-15, % permeability is almost 70 %. This means that permeability of the core rolls off to 70 % of its initial value when current flow is 93 A. Therefore the inductance at rated current (93 A) is calculated as

$$L_{@93A} = 0.7 \times 766\ \mu H = 536\,\mu H \tag{3.23}$$

3.3.2 Core loss

Core loss can be calculated by using the core loss equation given by the manufacturer. Eq. (3.24) is the core loss equation for Changsung megaflux core [25].

$$P_c = 1.78 \times B^{2.05} \times f^{1.535}\ \ [mW/cm^3] \tag{3.24}$$

, where B is flux density in kilogauss, f in kHz, and V_e is the total core volume.

The flux density (ΔB) can be calculated as

$$\begin{aligned} \Delta B &= \frac{V_L \times T_{on}}{N \times A_e} = \frac{(nV_{in} - V_o) \times DT_s}{N \times A_e} \\ &= \frac{(2.33 \times 666 - 750)}{46 \times 25 \times 10^{-4} \times 26000} \times \frac{750}{2.33 \times 666} \approx 0.13T \end{aligned} \tag{3.25}$$

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With the flux density (ΔB) calculated in (3.25) and core volume in Table 3-2, the total core loss is calculated as follows

$$P_{core} = 1.78 \times B^{2.05} \times f^{1.535} \times V_e = 120\ W \tag{3.26}$$

where, $f_{sw} = 26\ kHz$, $B = 1.11 \times \frac{\Delta B}{2}$, $V_e = 891\ cm^3$

3.3.3 Winding loss

Figure 3-16 shows the copper resistivity as copper temperature varies. The copper resistivity ρ increases as temperatures increases [26]. For example, ρ at room temperature (25 °C) is about 17 nΩ.m or 1.7 μΩ.cm. However, ρ at 125 °C is almost 1.4 times bigger than that of at room temperature. Therefore, care should be taken in calculating copper loss of the inductor. In this work, copper loss was calculated at 125 °C.

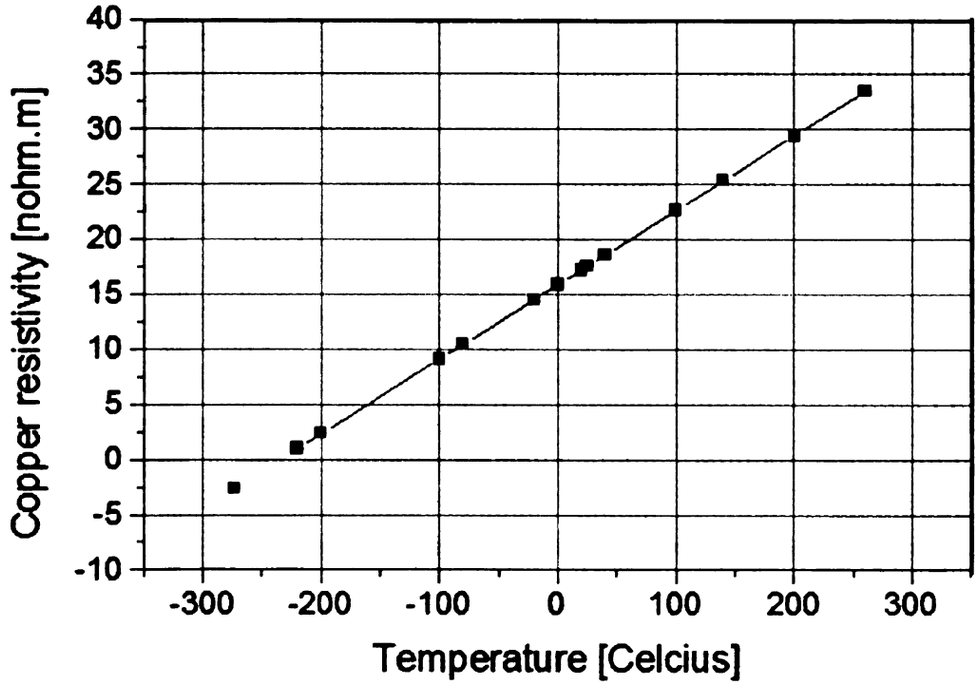

Figure 3-16 Copper resistivity vs. temperature

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A 10 mm×3 mm rectangular copper wire is used and the total winding length of 46 T inductor is approximately $0.31\ M \times 46 = 14.26\ M$. Therefore, the total DC winding resistance is calculated as

$$R_{DC} = 1.4 \times 17 \times 10^{-9} \times \frac{14.26}{30 \times 10^{-6}} = 11.3\ m\Omega \tag{3.27}$$

Thus, the winding loss of inductor at 93 A is

$$P_w = 93^2 \times 11.3 \times 10^{-3} \approx 98\ W \tag{3.28}$$

The AC winding loss caused by the skin and proximity effect is not considered in this calculation because AC ripple current of the inductor is relatively small compared with DC current. From the above calculated results, total loss of the output inductor is $120 + 98 = 218\ W$.

Figure 3-17 and Figure 3-18 are the side and top view of the coupled inductor designed in this work.

3.4. Conclusion

In this chapter, a 70 kW high power and high frequency transformer and inductor are designed. To reduce proximity effect in the transformer, two winding structures were invoked and its copper losses were calculated and compared. The optimum copper thickness which gives minimum power loss was found. Thus, the power loss and transformer size can be minimized with this approach.

The output coupled inductor is designed with the distributed airgap core. The very detailed design procedures are explained and core and winding losses are calculated.

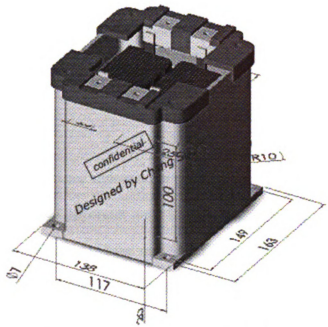

Figure 3-17 Inductor assembly (Side view)

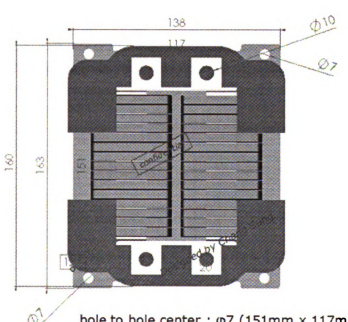

Figure 3-18 Inductor assembly (Top view)

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Chapter 4. Voltage Oscillation Problem in Secondary Rectifier Diode

4.1. Introduction

Besides the two key issues addressed in previous chapters in designing high power dc-dc converters, one more important issue in full-bridge dc-dc converters employing a diode rectifier in the output is voltage oscillation problem in the rectifier diodes. This oscillation is caused by the resonance between junction capacitances (C_j) of the rectifier diodes and leakage inductance (L_{lk}) of the transformer since the rectifier diodes are located between the two current sources, i.e. transformer leakage inductance and output filter inductor (L_o) [27, 28].

Figure 4-1 shows a conventional V-source type transformer isolated dc-dc converter.

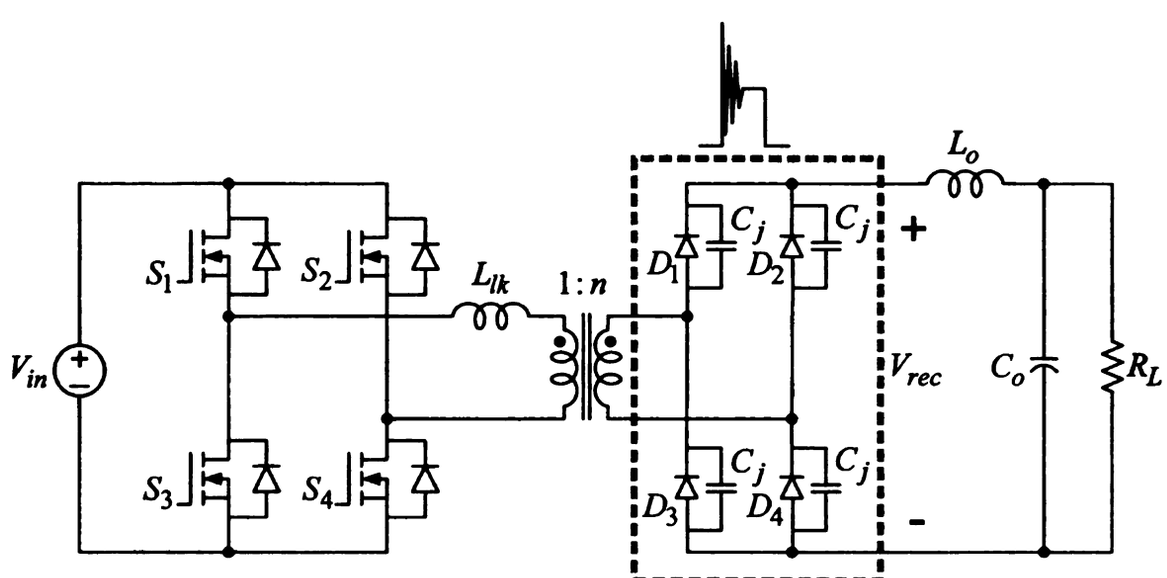

Figure 4-1 Voltage oscillation problem in secondary rectifier diode

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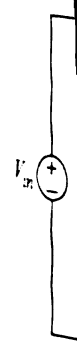

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Moreover, reverse recovery current of the rectifier diodes increases the voltage spike across the diode significantly [29]. Therefore, it increases the diode voltage rating, cost and causes EMI problem. As the output voltage of the dc-dc converter increases, higher voltage diodes are required. However, the use of a higher voltage diodes increases power loss and voltage overshoot in the diodes because higher voltage diodes have poor recovery characteristics.

In order to reduce voltage spike in the rectifier diodes, several techniques have previously been proposed. The conventional method is the use of an RCD snubber circuit which consists of diode (D_s), capacitor (C_s), and resistor (R_s) as shown in Figure 4-2 [27]. However, power loss in the snubber resistor R_s is very high as the output power increases. As a result, it degrades system efficiency.

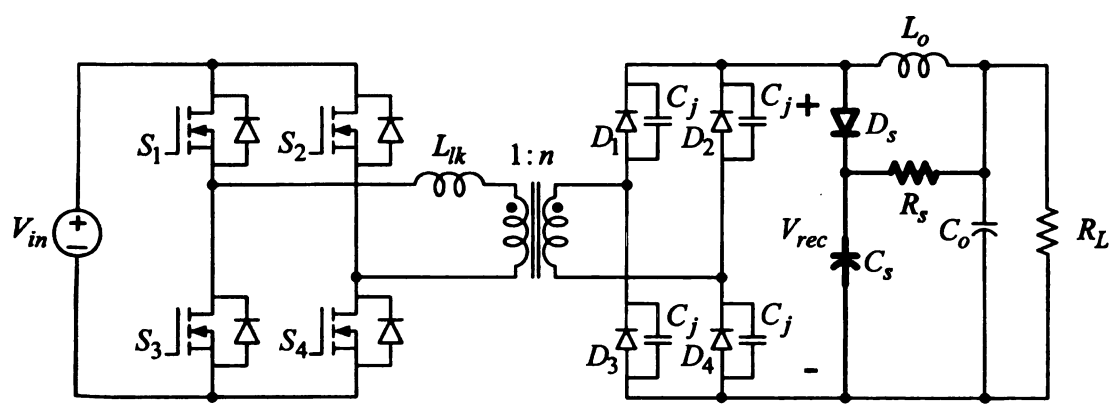

Figure 4-2 RCD clamped circuit

The active clamp method shown in Figure 4-3 can solve the efficiency degradation problem and the voltage overshoot can be clamped effectively with this method. However, this method degrades system reliability and increase complexity because

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additional switching device and gate drive signal are required to control the switch, Q_s [30]. Therefore, it is not desirable in high-power applications, either.

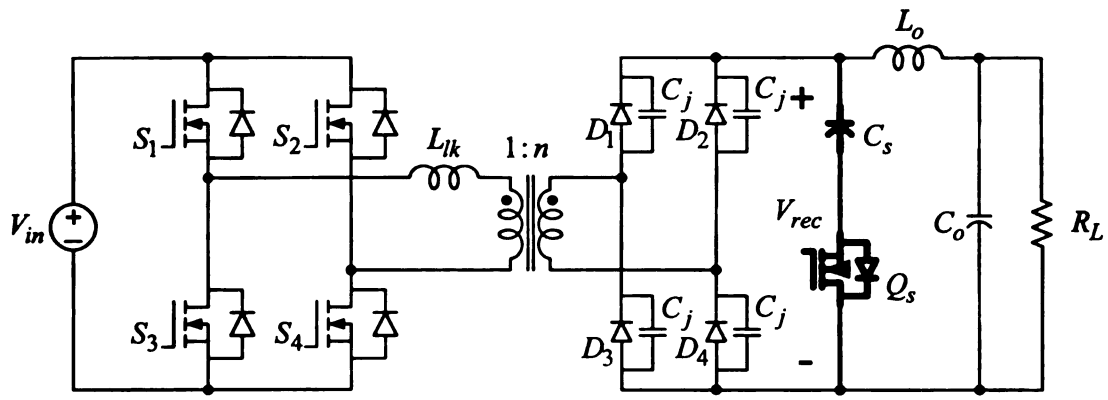

Figure 4-3 Active clamp circuit

The converter circuit shown in Figure 4-4 uses a capacitor (C_b) connected in series with the transformer to eliminate the voltage oscillation problem in the secondary rectifier diode and showed good performance [31]. However, this method is also not desirable in high power applications due to the series connection of the bulky capacitor.

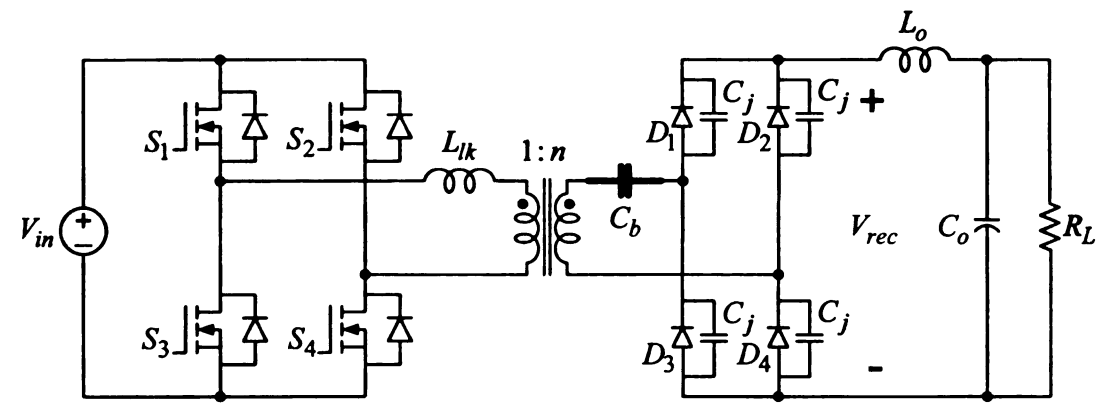

Figure 4-4 Voltage oscillation reduction circuit using C_b

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4.2. Review of Previously Proposed ERCC

To overcome the aforementioned problems, several energy recovery clamp circuits (ERCC) have been proposed [9, 10], [32-34]. Figure 4-5 shows one example of an ERCC employed in a V-source type PWM dc-dc converter [9]. It consists of one capacitor (C_s) and two diodes (D_{s1}, D_{s2}) to clamp diode voltage and there is no dissipative resistor. Therefore, the circuit can achieve lossless clamping function and no active switches are used.

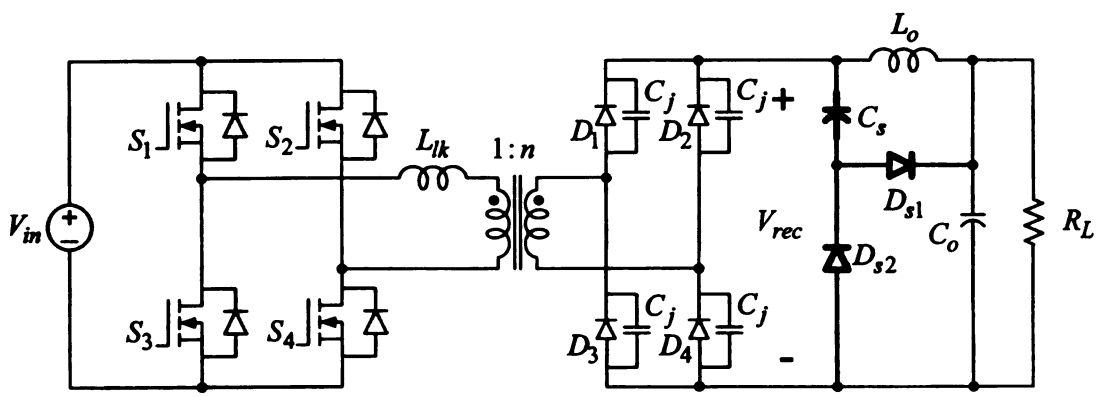

Figure 4-5 Energy recovery clamp circuit.

Figure 4-6 shows the ERCC slightly modified from Figure 4-5 and is labeled as ERCC #1 in this dissertation. In this dissertation, the transformer secondary winding is split into two windings to achieve high output voltage and to use standard 1200 V diodes. Two rectifier bridges are used and their outputs are connected in series. With this configuration, each bridge needs to sustain only one half of the output voltage. Transformer turns number is set to 6:7:7 ($N_p : N_{s1} : N_{s2}$) by considering the duty cycle loss caused by transformer leakage inductance and others. L_{lk} is the transformer leakage

inductance reflected to the secondary side of the transformer. In Figure 4-6, the switching devices in the transformer primary side are not included for the sake of simplicity.

The same ERCC used in Figure 4-5 is attached to the top and bottom rectifier of Figure 4-6. Therefore, operation of the circuit is exactly the same as the one shown in Figure 4-5.

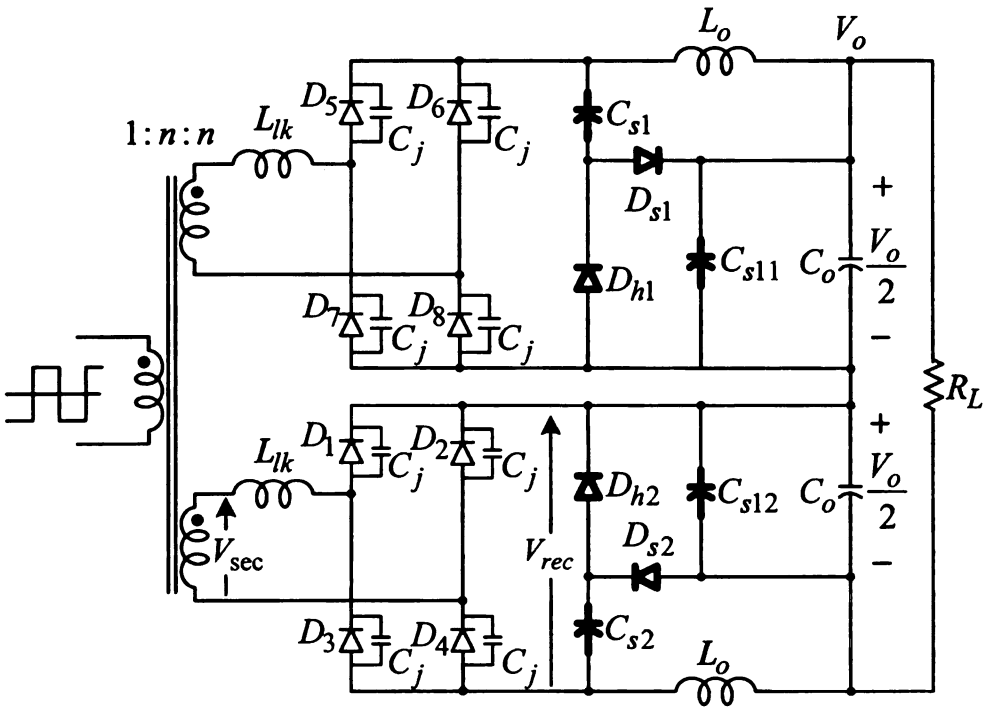

Figure 4-6 ERCC modified from Figure 4-5 (ERCC #1)

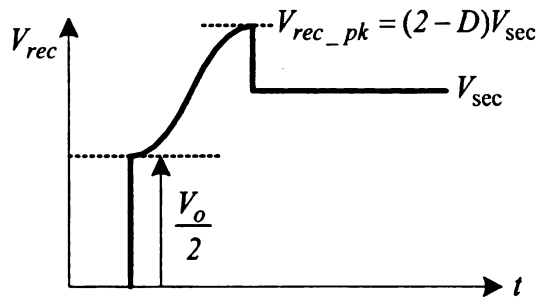

Figure 4-7 Diode voltage (V_{rec}) waveform of ERCC #1.

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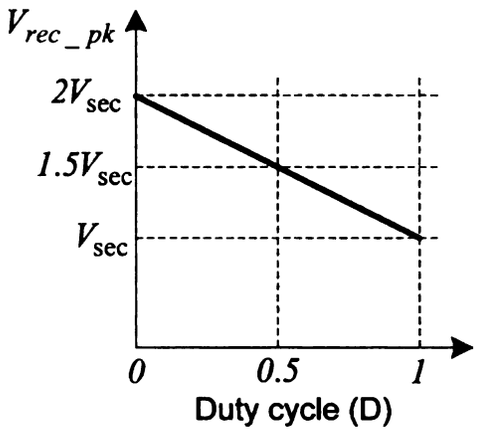

Figure 4-8 V_{rec_pk} vs duty cycle (D) of ERCC #1

Figure 4-7 depicts the peak voltage V_{rec_pk} across the rectifier diodes without considering diode reverse recovery current and with the assumption that snubber capacitors, C_{s1} and C_{s2}, are much bigger than diode junction capacitance, C_j. With this assumption, V_{rec_pk} can be expressed as (4.1) [9]. C_{s11} and C_{s22} are added to minimize stray inductance of the clamp path and they can be removed if output capacitor is very close to ERCC.

$$V_{rec\_pk} = 2(V_{sec} - \frac{V_o}{2}) + \frac{V_o}{2} = 2V_{sec} - \frac{V_o}{2} = (2 - D)V_{sec} \tag{4.1}$$

where, V_{in} is input voltage of the dc-dc converter, n is transformer turns ratio ($n = \frac{N_{s1}}{N_p} = \frac{N_{s2}}{N_p}$), V_{sec} is voltage in the transformer secondary winding ($= nV_{in}$), V_o is output voltage and D is duty cycle of the converter ($= \frac{1}{2}\frac{V_o}{V_{sec}}$).

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Figure 4-8 shows the V_{rec_pk} as D changes. In this work, V_{in} changes from 333-666 V and V_o is regulated to 750 V. With this input voltage range, the minimum duty cycle can be determined as.

$$D_{\min} = \frac{\frac{V_o}{2}}{V_{\sec}} = \frac{\frac{750}{2}}{\frac{7}{6} \times 666} \approx 0.483 \tag{4.2}$$

From (4.1) and (4.2), V_{rec_pk} can be calculated as.

$$V_{rec\_pk} = (2 - D)V_{\sec} = (2 - 0.483) \times \frac{7}{6} \times 666 = 1180V \tag{4.3}$$

Considering the reverse recovery current in the rectifier diodes, the voltage stress in diodes would be easily higher than 1200 V. Thus, we cannot use standard 1200 V diodes in this case. Again, the use of higher voltage diodes increases power loss and voltage overshoot across diodes because higher voltage diodes have poor recovery characteristics. Therefore, the ERCC #1 shown in Figure 4-6 is not applicable to the system described in this work, although it has the advantages of resetting circulating current in the primary side and achieves zero-voltage and zero-current switching (ZVZCS) in switching devices using the phase shift PWM control method [9].

Figure 4-9 shows another example of an ERCC modified from [29]. In [29], the two top and bottom output filter inductors are positioned to face each other at the middle of the circuit. The circuit in [29] works only when $V_{\sec}$ is less than V_o (i.e., $D > 0.5$) and the V_{rec_pk} is clamped to V_o. However, when $V_{\sec}$ is higher than V_o (i.e., $D < 0.5$), this

circuit does not work because a huge current will flow through snubber diodes, D_{s1} and D_{s2}, eventually destroying them. One possible way is to insert additional snubber resistors, R_{s1} and R_{s2}, as shown in the dashed box in Figure 4-9. By inserting R_{s1} and R_{s2} in the discharging path of snubber capacitors, C_{s1} and C_{s2}, a portion of energy stored in L_{lk} is dissipated in R_{s1} and R_{s2}, and the rest of the energy can be transferred to the output capacitor. The total power loss in R_{s1} and R_{s2} is calculated as (4.4).

$$P = P_{Rs1} + P_{Rs2} = 2\frac{(V_{rec\_pk} - V_o)^2}{R_s} = 2\frac{(V_{rec\_pk} - 2DV_{\sec})^2}{R_s} \tag{4.4}$$

where, $R_s = R_{s1} = R_{s2}$.

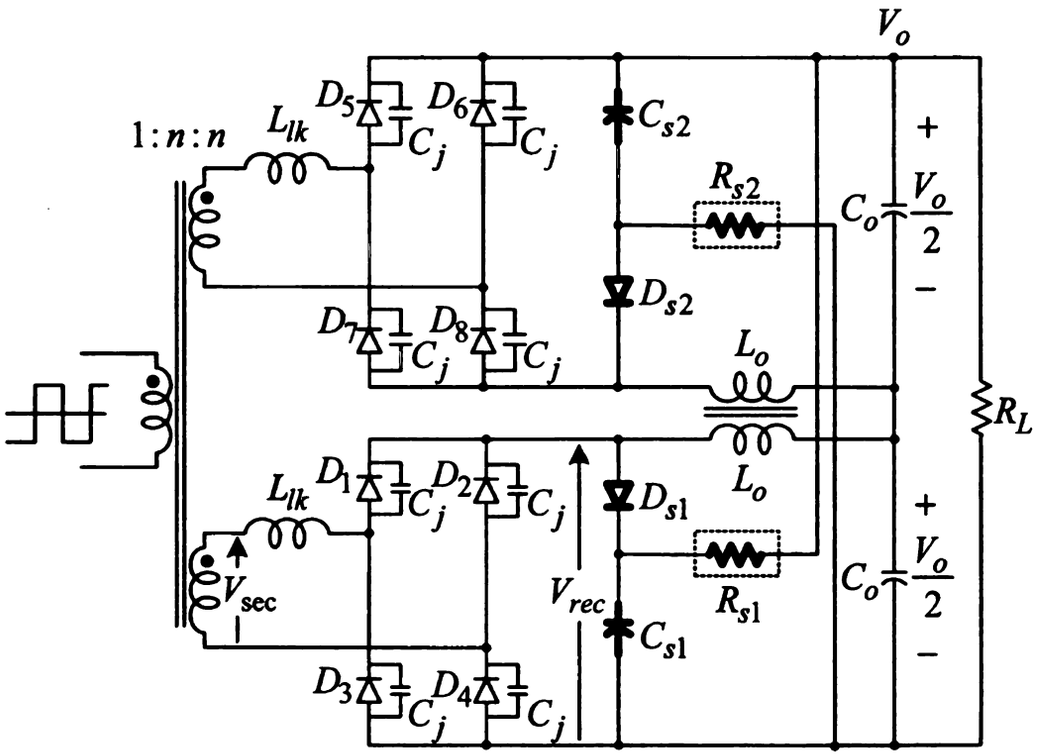

Figure 4-9 ERCC modified from the circuit in [29]

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Compared with conventional RCD snubber circuits, such as the one shown in Figure 4-2, the power loss in R_{s1} and R_{s2} is reduced significantly because the voltage across R_{s1} and R_{s2} can be reduced a lot [35]. The power losses in R_{s1} and R_{s2}, however, are not negligible when D varies in a wide range. Therefore, the ERCC shown in Figure 4-9 also suffers from the efficiency degradation problem and are not applicable to the system discussed in this dissertation.

4.3. Proposed ERCC

4.3.1 Principle Operation of Proposed ERCC

The two ERCCs discussed in Figure 4-6 and Figure 4-9 have some limitations and are not desirable for systems with wide ranges of input voltage, especially when $D < 0.5$.

Figure 4-10 shows the ERCC proposed in this work that overcomes the drawbacks of the previously proposed circuit. The proposed circuit employs a simple auxiliary circuit in which neither lossy components nor active switches are used. Therefore, the efficiency and reliability of the dc-dc converter can be improved with this proposed ERCC. C_{s11} and C_{s22} are added to minimize stray inductance of the clamp path

The transformer secondary current $I_{lk}(t)$ and diode voltage $V_{rec}(t)$ waveforms are sketched in Figure 4-11.The output filter inductor L_o is assumed big enough and thus I_o can be modeled as constant. Operational modes of the proposed ERCC are explained as follows and are shown in Figure 4-12. For the sake of simplicity, only the diode rectifier located at the bottom is considered and analyzed because the top and bottom rectifiers operate in the same manner.

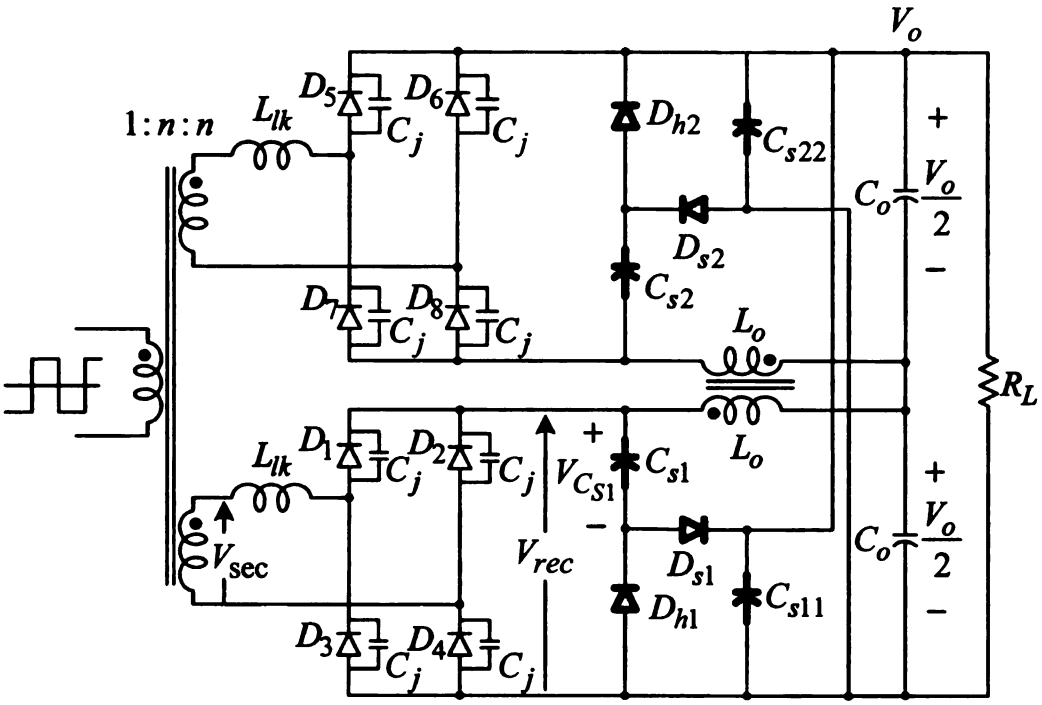


Figure 4-10 Proposed ERCC.

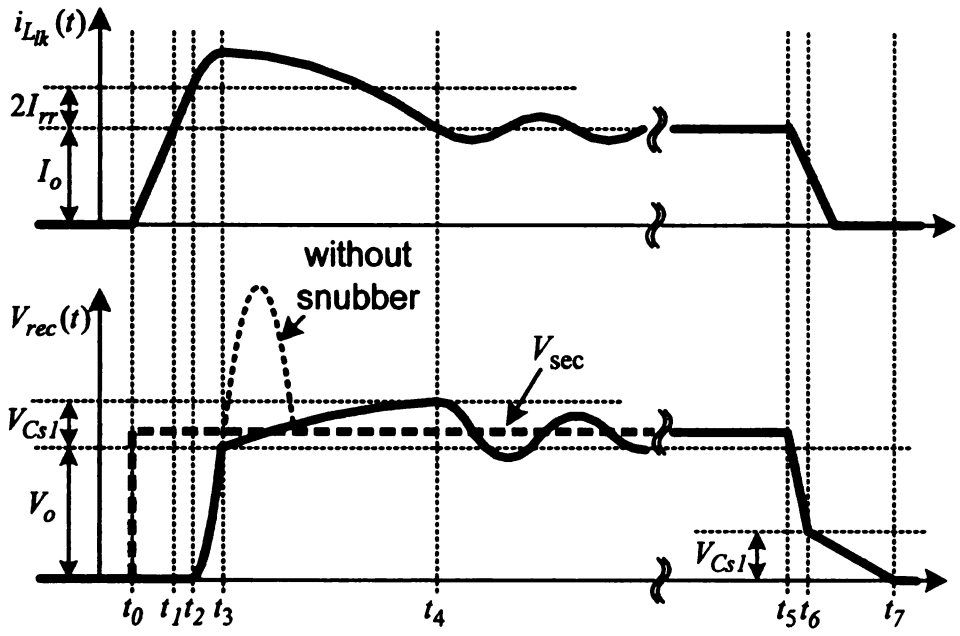
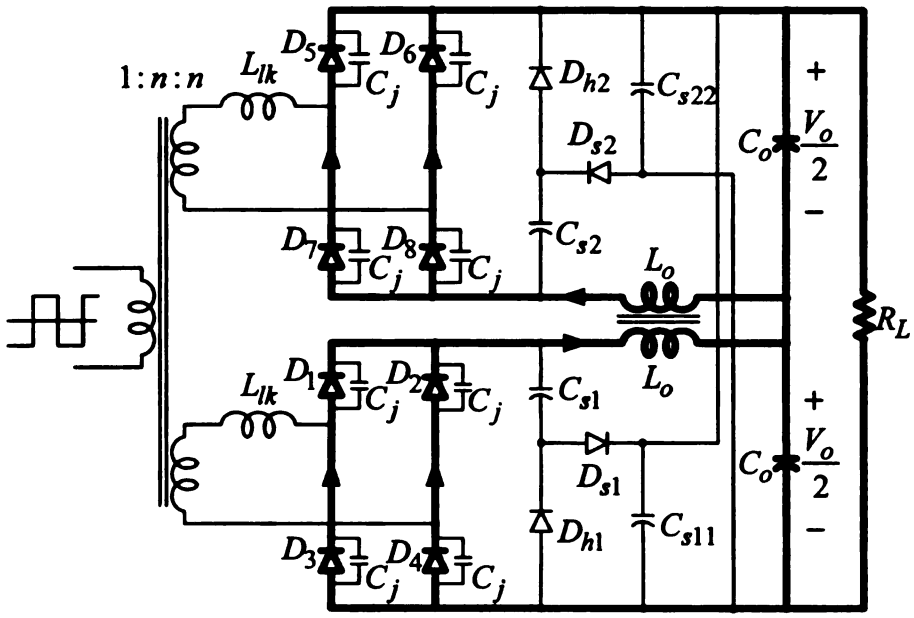
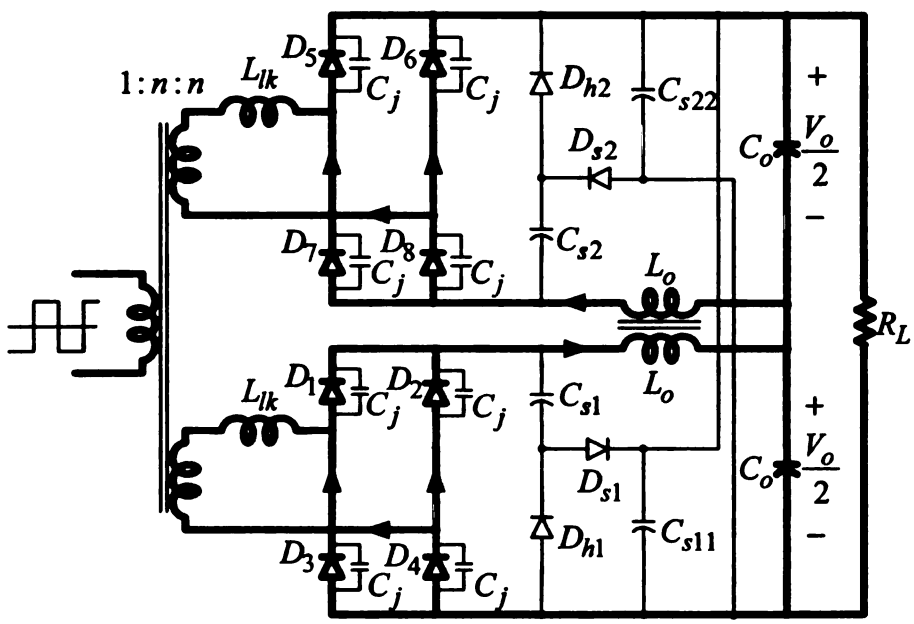


Figure 4-11 Key waveforms of proposed ERCC.



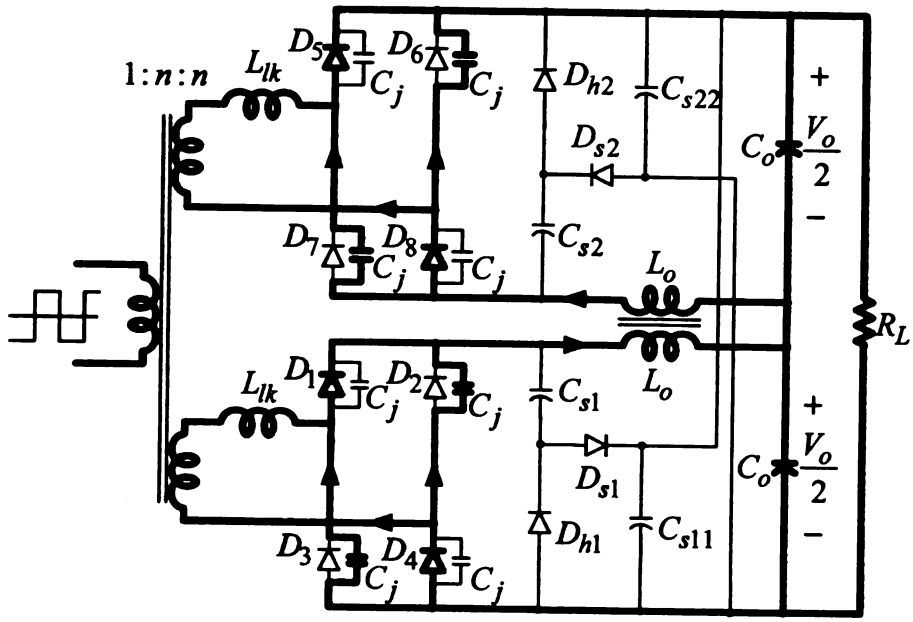
<Mode 1>



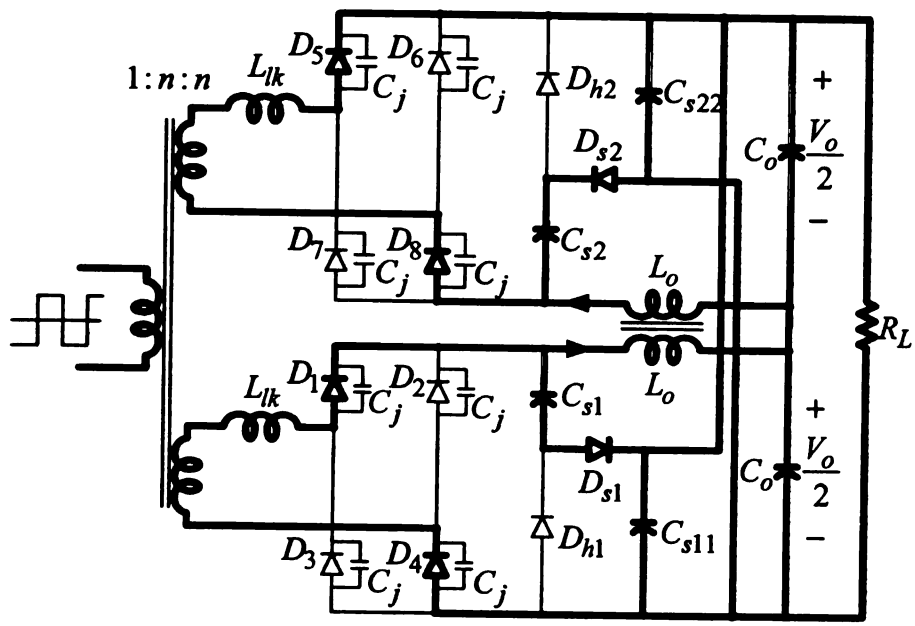
<Mode 2,3>

Figure 4-12 Operational modes of proposed ERCC

Figure 4-12 continued.

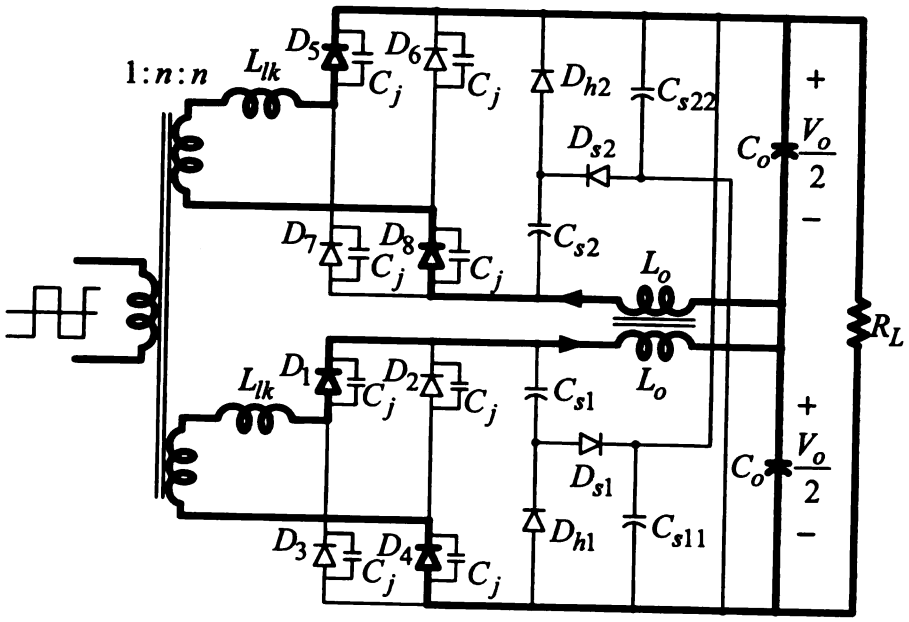


<Mode 4>



<Mode 5>

Figure 4-12 continued.



<Mode 6>

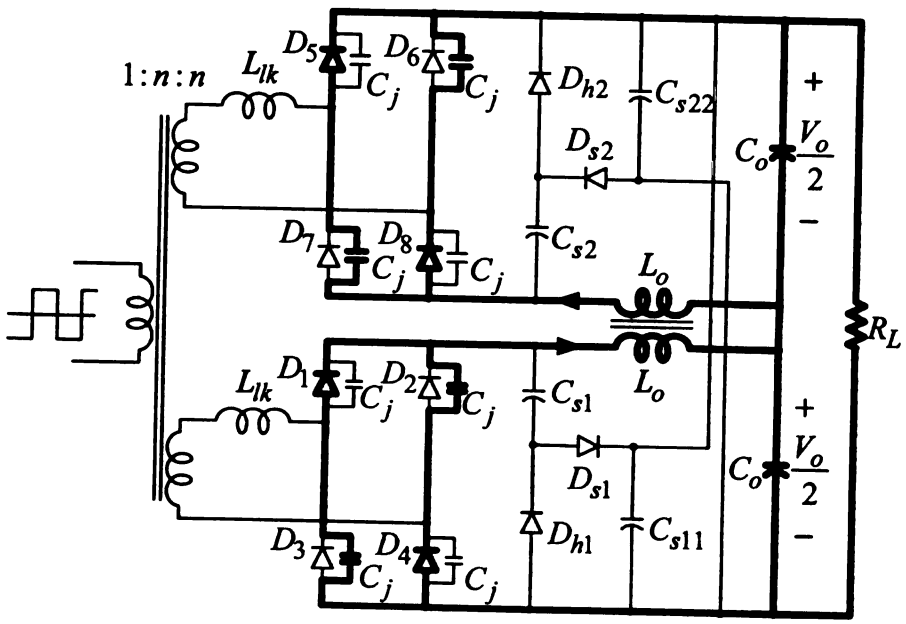


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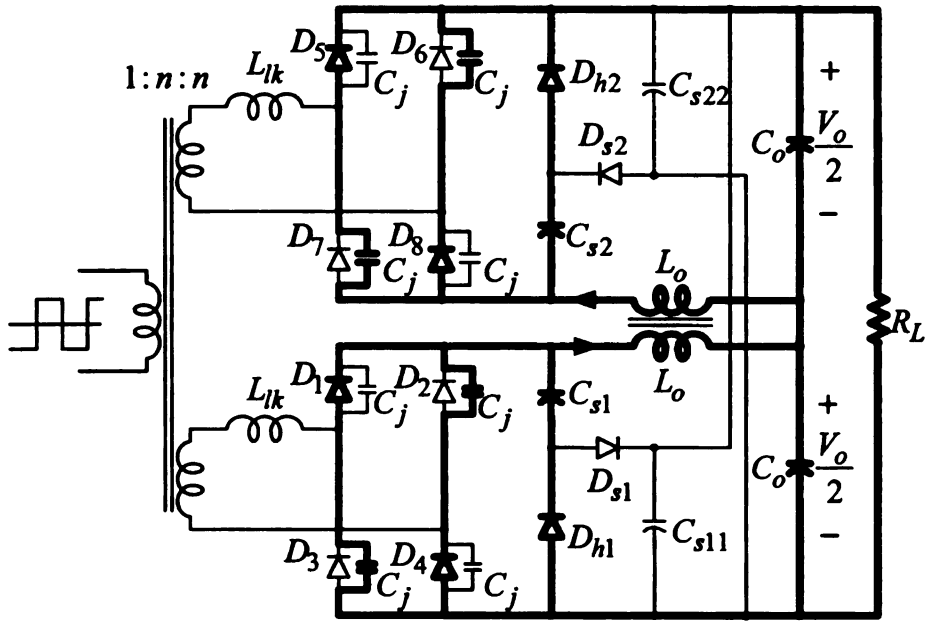
Figure 4-12 continued.



<Mode 8>

- *Mode 1* ($\sim t_o$): $S_1 - S_4$ turned off and rectifier diodes are in freewheeling period. V_{sec} remains zero. $D_1 - D_4$ are on and each diode carries $\frac{I_o}{2}$

- *Mode 2* ($t_o - t_1$): S_1 and S_4 turn on. V_{sec} changes from zero to nV_{in} and transformer secondary current builds up linearly with the slope of $\frac{nV_{in}}{L_{lk}}$ until it reaches I_o. The current in D_1 and D_4 increases, while the current in D_2 and D_3 decreases in this mode.

- *Mode 3* ($t_1 - t_2$): reverse recovery period of D_2 and D_3. The current in D_1 and D_4 builds up with the same slope of $\frac{nV_{in}}{L_{lk}}$ until D_2 and D_3 turn off at t_2.

At $t = t_2$, the current in L_{lk} becomes $I_o + 2I_{rr}$, where I_{rr} is the reverse recovery current of the rectifier diode. Until this mode, V_{rec} remains zero because D_2 and D_3 are still on (conducting).

- *Mode 4* $(t_2 - t_3)$: D_2 and D_3 snap off at t_2 and its junction capacitors, C_j, start resonance with L_{lk}. During this mode, V_{rec} and $I_{L_{lk}}$ are expressed as follows with the initial conditions $V_{rec}(0) = 0$, $I_{L_{lk}}(0) = I_o + 2I_{rr}$.

$$V_{rec}(t) = nV_{in}\left[1 - \cos(w_o t)\right] + (I_R Z_c)\sin(w_o t) \tag{4.5}$$

$$I_{L_{lk}}(t) = I_o + \frac{nV_{in}}{Z_c}\sin(w_o t) + I_R \cos(w_o t) \tag{4.6}$$

where, $Z_c = \sqrt{\frac{L_{lk}}{2C_j}}$, $w_o = \frac{1}{\sqrt{L_{lk}(2C_j)}}$, $I_R = 2I_{rr}$

- *Mode 5* $(t_3 - t_4)$: When V_{rec} reaches V_o at t_3, D_{s1} starts conducting and there is another resonance between C_{s1} and L_{lk}. Because C_{s1} is much bigger than C_j, the current flowing through C_j can be ignored in this mode analysis. C_{s11} is added to minimize circuit stray inductance in the snubber path, $C_{s1} - D_{s1} - C_{s11}$, and can be assumed large enough because it is connected in parallel with the output capacitor. During this mode, V_{rec} and $I_{L_{lk}}$ are expressed as (4.7) and (4.8) with the initial conditions $V_{rec}(0) = V_o$, $I_{L_{lk}}(0) = I_p$. I_p is the current at $t = t_3$ and can be calculated from (4.5) and (4.6).

$$V_{rec}(t) = V_o + (nV_{in} - V_o)[1 - \cos(w_d t)] + \frac{Z_d}{Z_c}\sqrt{(I_R Z_c)^2 + 2nV_{in}V_o - V_o^2}\sin(w_d t) \quad (4.7)$$

$$I_{L_{lk}}(t) = I_o + \frac{nV_{in} - V_o}{Z_d}\sin(w_d t) + \frac{\sqrt{(I_R Z_c)^2 + 2nV_{in}V_o - V_o^2}}{Z_c}\cos(w_d t) \quad (4.8)$$

where, $Z_c = \sqrt{\frac{L_{lk}}{2C_j}}$, $Z_d = \sqrt{\frac{L_{lk}}{C_{s1}}}$, $w_d = \frac{1}{\sqrt{L_{lk}C_{s1}}}$

At $t = t_4$, $V_{rec}(t)$ reaches its peak value V_{rec_pk} because $I_{L_{lk}}(t)$ becomes equal to I_o at this point. From (4.7) and (4.8), V_{rec_pk} can be derived as.

$$V_{rec\_pk} = nV_{in} + \sqrt{(nV_{in} - V_o)^2 + \frac{L_{lk}}{C_{s1}}I_R^2 + \frac{2C_j}{C_{s1}}(2nV_{in}V_o - V_o^2)} \quad (4.9)$$

V_o can be expressed as

$$V_o = 2 \times D \times nV_{in} \quad (4.10)$$

Substituting (4.10) into (4.9) yields

$$V_{rec\_pk} = nV_{in} + \sqrt{[nV_{in}(1-2D)]^2 + \frac{L_{lk}}{C_{s1}}I_R^2 + \frac{2C_j}{C_{s1}}(nV_{in})^2 4D(1-D)} \quad (4.11)$$

- *Mode 6* ($t_4 - t_5$): when $I_{L_{lk}}$ is equal to I_o at t_4, D_{s1} stops conducting and there is a resonance between L_{lk} and C_j. This resonance is similar to that of Mode 4. During this mode, V_{rec} and $I_{L_{lk}}$ starts decaying with oscillation and finally converges to nV_{in} and I_o, respectively. The voltage in C_{s1} is kept constant to $V_{C_{S1}}$ during this mode.

- *Mode 7* ($t_5 - t_6$): S_1 and S_4 turned off at t_5. $I_{L_{lk}}$ and V_{rec} start decreasing.

- *Mode 8* ($t_6 - t_7$): V_{rec} is equal to $V_{C_{S1}}$ at t_6 and D_{h1} starts conducting at this point. C_{s1} can be discharged through D_{h1} and supplies a portion of the load current I_o. $V_{C_{S1}}$ is fully discharged at t_7 and $D_1 - D_4$ turn on and start freewheeling after t_7.

The operational mode analysis shown above is applied to the condition of $D < 0.5$ (i.e., $V_{\text{sec}} > V_o$). For $D > 0.5$, V_{rec_pk} ($= V_{C_{s1}} + V_o$) is almost equal to V_o because the current in the transformer leakage inductance is not sufficient to charge C_{s1}. From the results mentioned above, V_{rec_pk} can be expressed as (4.12) and (4.13) for $D < 0.5$ and $D > 0.5$, respectively. It should be pointed out that reverse recovery current of the rectifier diode is not included in (4.12) and (4.13) for the sake of simplicity.

$$V_{rec\_pk} = 2(V_{\text{sec}} - V_o) + V_o = 2(1-D)V_{\text{sec}} \qquad (D < 0.5) \tag{4.12}$$

$$V_{rec\_pk} \approx V_o = 2 \times \frac{V_o}{2} = 2DV_{\text{sec}} \qquad (D > 0.5) \tag{4.13}$$

Using (4.12) and (4.13), V_{rec_pk} of the proposed ERCC is plotted in Figure 4-13 as a function of D with V_{sec} and V_o. V_{rec_pk} in Figure 4-8 is plotted again for comparison with the proposed ERCC. As shown in Figure 4-13, V_{rec_pk} is clearly reduced by using the proposed ERCC within the duty cycle range of $0 < D < 2/3$. When $D = 0.5$, for example, V_{rec_pk} of the proposed ERCC is V_{sec} (or V_o) while V_{rec_pk} of ERCC #1 is $1.5 \times V_{\text{sec}}$ (or $1.5 \times V_o$). Thus, there is a 50 % reduction in V_{rec_pk} by using the proposed

ERCC, which enables the use of low voltage diodes and leads to higher efficiency of the dc-dc converter.

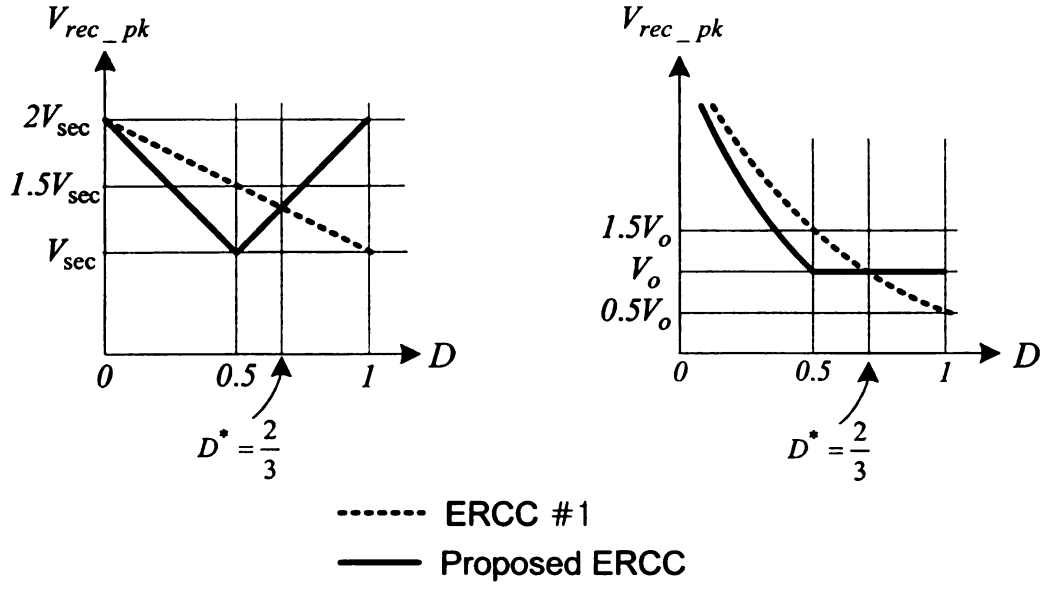


Figure 4-13 Comparison of V_{rec_pk} as a function of D.

Although the proposed ERCC has higher voltage spike when $D > 2/3$, it does not degrade performance of the proposed ERCC because diode voltage rating is determined with maximum input voltage or minimum duty cycle of converter. In other words, the increased voltage spike when $D > 2/3$ is still within the range of diode voltage rating.

4.3.2 Simulation and Experimental Results

A 70 kW prototype dc-dc converter employing the proposed ERCC has been built and tested to verify the principle of operation and is compared with simulation results.

Table 4-1 shows operational conditions and circuit parameters of the dc-dc converter developed in this work.

Table 4-1 Operational Conditions and Circuit Parameters of dc-dc Converter

Input Voltage	*333 - 666 Vdc*
Output Voltage / Current	*750 Vdc / 93 A*
Switching frequency	*13 kHz*
IGBT	*Powerex CM600HU-24F (1200V, 600 A)*
Rectifier Diode ($D_1 - D_8$)	*Powerex QRD1230T30 (1200 V, 150 A) trr=130 ns, Irr=30 A*
Transformer turns number	6:7:7
Transformer leakage inductance (L_{lk}) in secondary	1 μH
C_j	1 nF
C_{s1}, C_{s2}	100 nF
C_{s11}, C_{s22}	470 nF
D_{s1}, D_{s2}, D_{h1}, D_{h2}	*IXYS DSEI 2×61-12*
L_o	500 μH
C_o	9.4 mF

Figure 4-14 and Figure 4-15 shows the simulation results of the dc-dc converter when D=0.483 and 0.8, respectively. The simulation waveforms shown in Figure 4-14 are well consistent with theoretical ones shown in Figure 4-11. When $D > 0.5$, V_{rec_pk} is almost clamped to V_o as expected because the current in L_{lk} is not sufficient to charge snubber capacitors, C_{s1} and C_{s2}.

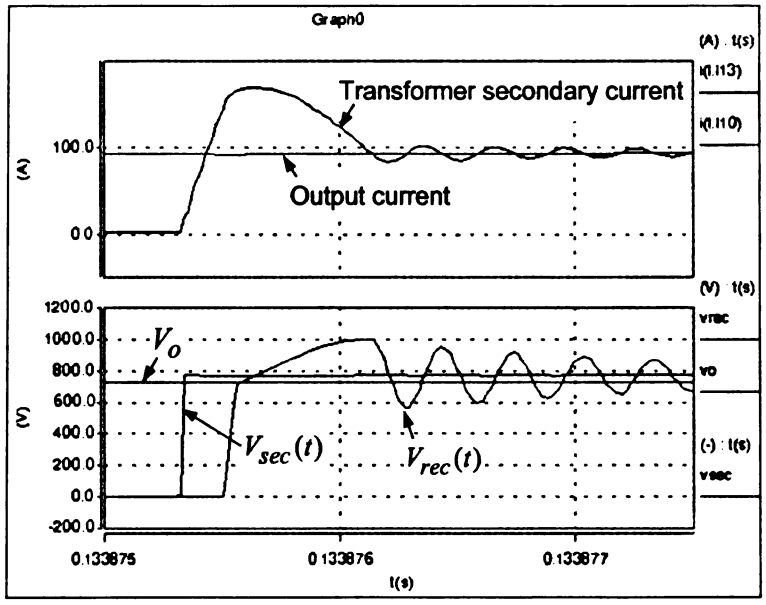


Figure 4-14 Simulation waveforms of proposed ERCC when D=0.483

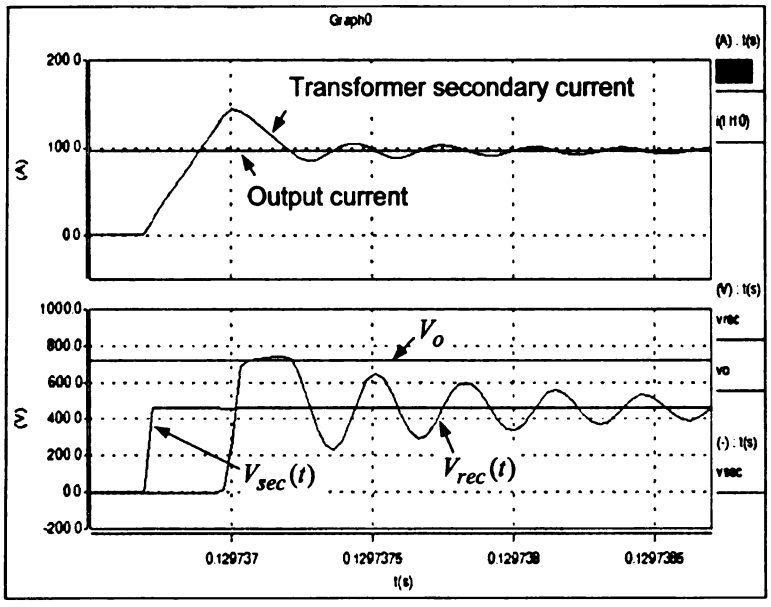


Figure 4-15 Simulation waveforms of proposed ERCC when D=0.8

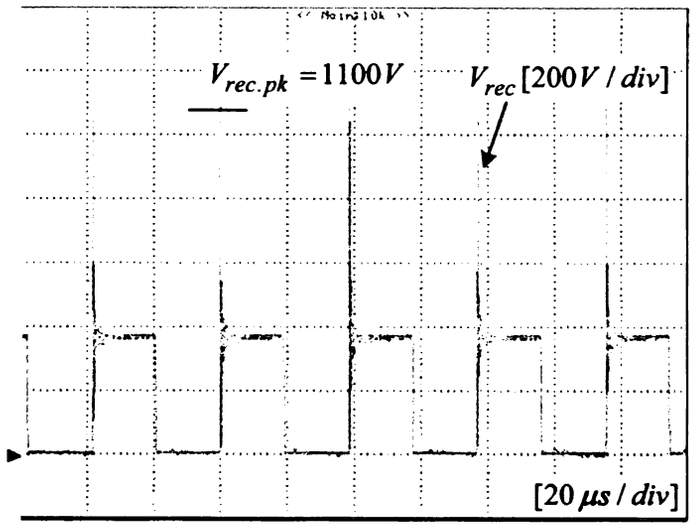


Figure 4-16 Experimental waveforms measured without calmp circuit

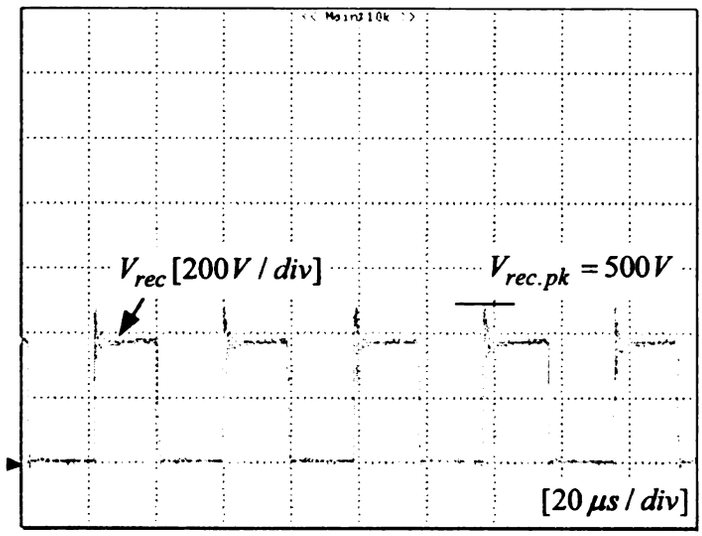


Figure 4-17 Experimental waveforms measured with proposed ERCC

Figure 4-16 shows V_{rec} measured without clamp circuit under the test conditions of $V_{in} = 328V, V_o = 374V \text{ and } P_o = 14kW$. Without the clamp circuit, V_{rec_pk} was increased to 1100 V when transformer secondary voltage V_{sec} was $328 \times (7/6) \approx 383\,V$. V_{rec_pk} was almost 2.9 times that of V_{sec} because the reverse recovery currents of the rectifier diodes contribute significantly to this voltage overshoot.

Figure 4-17 shows V_{rec} measured with the proposed ERCC under the same test conditions above. As shown in Figure 4-17, V_{rec_pk} was well clamped to almost 1.3 times that of V_{sec} with the proposed ERCC.

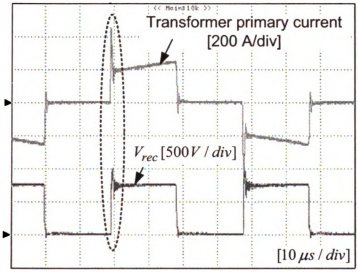


Figure 4-18 Experimental waveforms with proposed ERCC when D=0.483

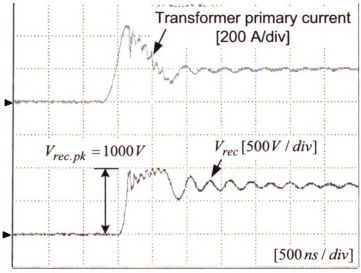


Figure 4-19 Zoom-in waveforms of Figure 4-18

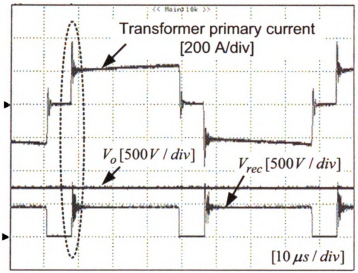


Figure 4-20 Experimental waveforms using proposed ERCC when D=0.8

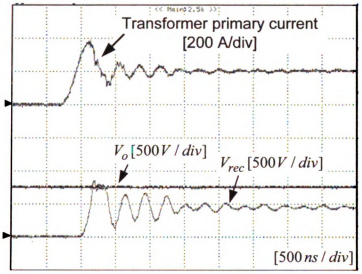


Figure 4-21 Zoom-in waveforms of Figure 4-20

Figure 4-18 shows the experimental waveforms of the transformer primary current and V_{rec} using the proposed ERCC under the worst case conditions of $V_{in} = 666V$, $V_o = 750V$, $D = 0.483$ and $P_o = 70kW$. Due to the physical layout of the **secondary busbar**, transformer primary current is measured instead of secondary. Figure

4-19 shows the expanded waveforms of Figure 4-18. V_{rec_pk} is effectively clamped to almost 1000 V . The current and voltage waveforms in Figure 4-19 are compatible to those of theoretical waveforms shown in Figure 4-11 and simulation waveforms shown in Figure 4-14.

Figure 4-20 shows the experimental waveforms of transformer primary current and V_{rec} using the proposed ERCC under the test conditions of $V_{in} = 400V, V_o = 750V, D = 0.8$ and $P_o = 70kW$. V_{rec_pk} is almost clamped to V_o as expected and is close to the simulation results shown in Figure 4-15

Figure 4-22 and Figure 4-23 shows the zoom in waveforms of transformer primary current and V_{rec} when $V_{in} = 600V, V_o = 670V, D = 0.48$ and $P_o = 50kW$ to compare the performance of the proposed ERCC with ERCC #1. V_{rec_pk} was decreased from 1060 V to 850V with the proposed ERCC which is almost 30 % reduction in V_{rec_pk}. In addition to voltage reduction in V_{rec_pk}, the proposed ERCC has lower transformer peak current than the ERCC #1. This is because snubber capacitors C_{s1} and C_{s2} in the proposed ERCC start charging when V_{rec} reaches V_o instead of. $\frac{V_o}{2}$. Therefore, it will decrease conduction loss in transformer and IGBT which results in improved system efficiency (see Figure 4-25).

Figure 4-24 shows the measured V_{rec_pk} as C_{s1} (or C_{s2}) changes from 10 nF to 600 nF under the test conditions of $V_{in} = 450V, V_o = 510V$ *and* $I_o = 55A$. The measured V_{rec_pk} is compared with the theoretical results plotted using (4.11).

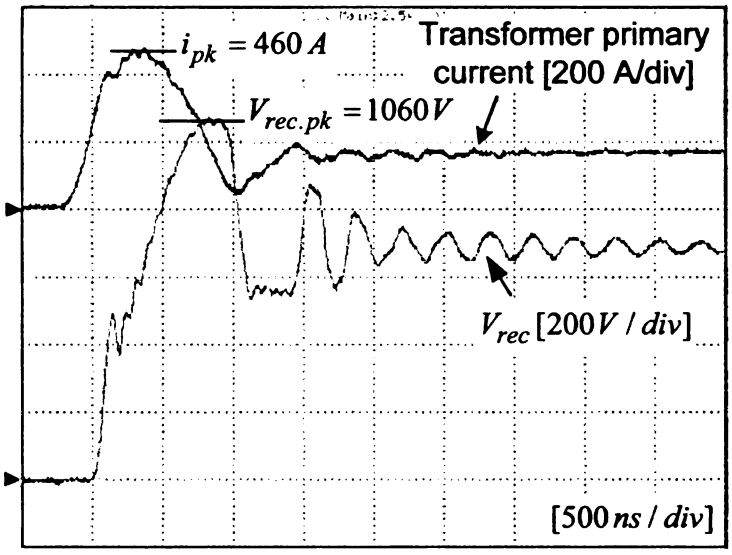


Figure 4-22 Experimental waveforms of ERCC #1

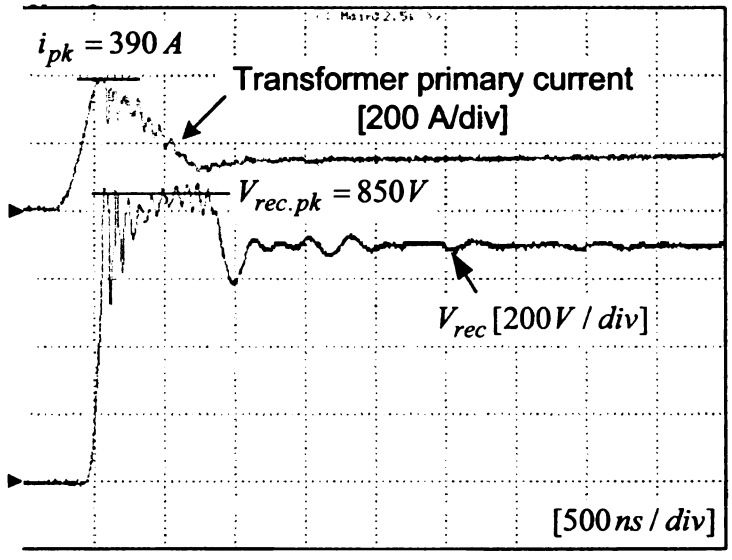


Figure 4-23 Proposed ERCC

The measured V_{rec_pk} is very close to the theoretical value. V_{rec_pk} is inversely proportional to snubber capacitance C_{s1}. In this work, a 100 nF capacitor is selected for C_{s1} and C_{s2} because a larger than necessary capacitor will increase current in the transformer and IGBT. Therefore, converter efficiency will be decreased.

Figure 4-25 shows the measured efficiency of dc-dc converter using the proposed ERCC and is compared with the efficiency measured with ERCC #1. Efficiency of the proposed converter was almost the same as ERCC #1 when V_{in} is low and slightly improved as V_{in} towards maximum value as expected. In the test, a digital power meter (YOKOGAWA, WT1600) was used to measure the input and output power and the output power was 50 kW.

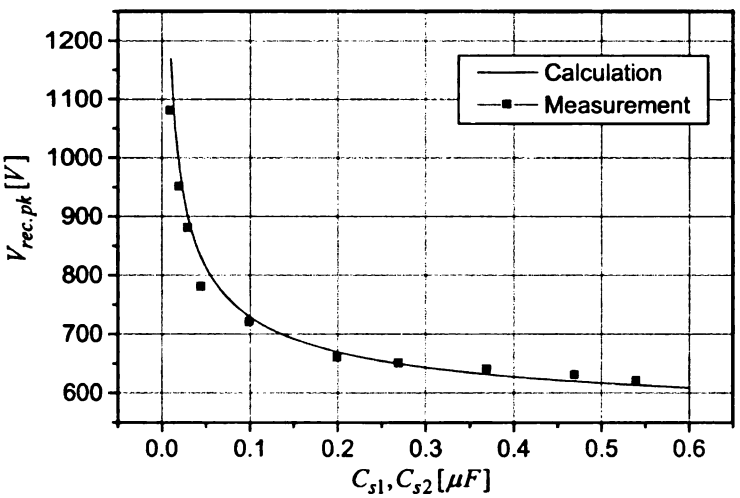


Figure 4-24 Measured and theoretical results of V_{rec_pk} vs. C_{s1}.

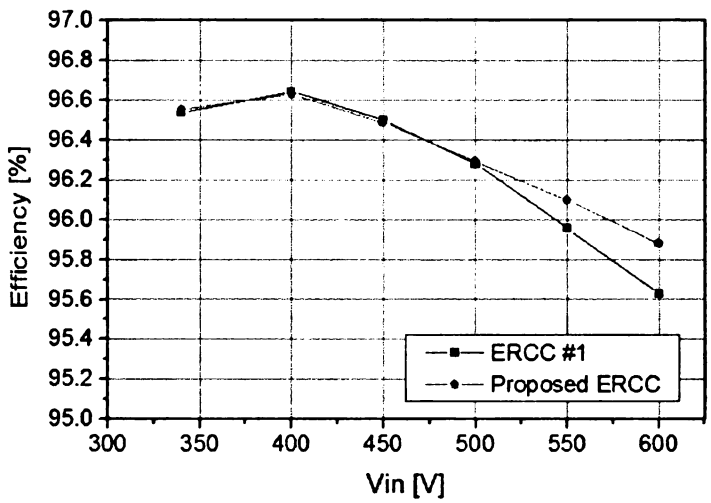


Figure 4-25 Measured efficiency at 50 kW output power.

4.4. Conclusion

In this chapter, a novel ERCC for PWM dc-dc converters for wide ranges of input voltage is introduced. The limitations and drawbacks of previously proposed ERCCs have been pointed out. Detailed analysis has been presented and performance of the proposed ERCC was compared with the previously proposed ERCCs.

A 70 kW prototype dc-dc converter employing the proposed ERCC has been built and tested to verify the principle of operation. The proposed ERCC consists of two small capacitors and two diodes in each bridge. Neither lossy components nor additional active switches are used to clamp diode voltage. Therefore, the efficiency and reliability of the dc-dc converter can be improved by using the proposed ERCC. The proposed ERCC is very promising for high voltage and high power dc-dc converters with wide ranges of input voltage.

Chapter 5. Power Loss Breakdown and Overall System Test

Figure 5-1 and Figure 5-2 show 3-D design of 70 kW dc-dc converter developed in this work.

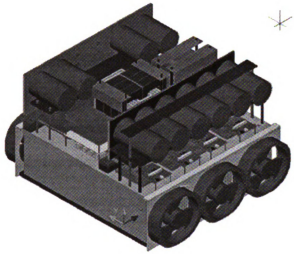


Figure 5-1 3-D design of 70 kW dc-dc converter

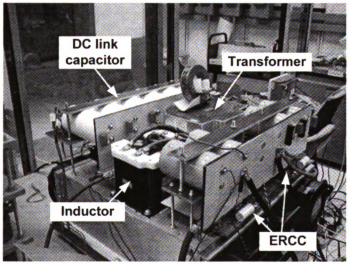


Figure 5-2 Photo of 70 kW dc-dc converter

5.1. Power loss breakdown

From the results of Chapter 2-4, the power loss breakdown of converter system can be made. Following are the loss calculations in each component in the 70 kW dc-dc converter and its associated power losses are tabulated in Table 5-1.

1. Power losses in IGBT [36]

   - Switching loss/IGBT

     - Turn-on loss: $12\,mJ \times 13\ kHz \times \frac{250}{600} = 65\ W$

     - Turn-off loss: $28\,mJ \times 13\,kHz \times \frac{250}{600} = 152\ W$

   - Conduction loss: $v_{ce\_sat} \times I_{sw} \times D = 1.5 \times 220 \times 0.32 = 106\ W$

   - Capacitive turn-on loss in snubber capacitor (C_{sp}, C_{sn}):

     $$\frac{1}{2}(2C)(\frac{V_{in}}{2})^2 f_{sw} = \frac{1}{2}(2 \times 15\ nF) \times (\frac{500}{2})^2 \times 13\,kHz = 12.2\ W$$

   - Total power loss in 4 IGBT:

     $$P_{IGBT} = (P_{sw} + P_{con} + P_{cap}) \times 4 = (217 + 106 + 12.2) \times 4 = 1341\ W$$

2. Power loss in primary snubber resistor (R_{snub})

   $$I_{rms}{}^2 \times R_{snub} \times 4 = 0.8^2 \times 8.6 \times 4 = 22\ W$$

3. Power loss in DC link capacitor

   $$I_{rms}{}^2 \times R_{esr} = 106^2 \times 15\ m\Omega = 169\ W$$

4. Power loss in transformer

   - core loss: *110 W*

   - copper loss: *92 W*

- total power loss in transformer : 202 W

5. Power loss in inductor
    - core loss: 121 W
    - copper loss: 98 W
    - total power loss : 219 W
6. Power loss in secondary rectifier diode
    - conduction loss: 707 W
    - recovery loss: 68 W
    - total power loss : 775 W
7. Others : 100 W

Figure 5-3 shows loss breakdown of the 70 kW dc-dc converter. As shown in Figure 5-3, most of the power loss occurs in the IGBT and rectifier diodes. Power loss in transformer and inductor takes significant portion as well.

It should be noted that although the power loss in transformer and inductor is smaller than that of IGBT and rectifier diodes, their thermal resistance from inside to outside is much greater that of IGBT and rectifier diodes. The high thermal resistance causes heat accumulation inside transformer and inductor. As a result, it will leads to thermal runaway and finally system failure. Thus, magnetic design in high power converter system is very important and should not be overlooked

Table 5-1 Power loss breakdown in 70 kW dc-dc converter

Loss component			loss			
IGBT	Switching loss	Turn-on	260	868	1341	W
		Turn-off	608			W
	Conduction loss		424			W
	Capacitive turn-on loss in snubber capacitor		49			W
Primary snubber resistance (Rsnub) loss			22			W
Power loss in ESR of DC link capacitor			169			W
Transformer	Core loss		110		202	W
	Copper loss		92			W
Inductor	Core loss		121		219	W
	Copper loss		98			W
Rectifier diode	Conduction loss		707		775	W
	Reverse recovery loss		68			W
Others			100			W
Total			***2818***			W

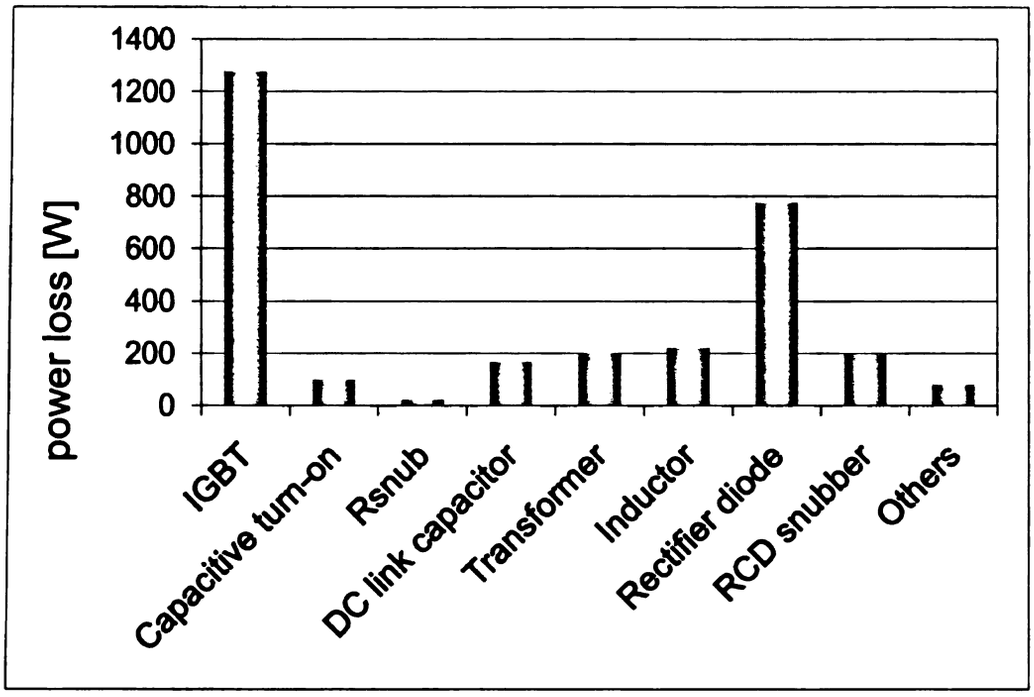


Figure 5-3 Loss breakdown of 70 kW dc-dc converter.

5.2. Overall system test

The overall system configurations are redrawn in Figure 5-4. The three 70 kW dc-dc converter modules are connected in series at the input and in parallel at the output. In this configuration, the duty ratio to all the converter modules connected in input-series and output-parallel (ISOP) configuration is made common. Therefore, this configuration does not require a dedicated input-voltage or load-current share controller. It relies on the inherent self-correcting characteristic of the ISOP connection when the duty ratio of all the converters is the same [37, 38].

To verify operation of the whole system, three dc-dc converter modules are connected in series at the input and a 260 kVA inverter is connected as shown in Figure 5-4 to produce the desired 3-phase output. In this test, 1500 Vdc is applied to the input of the dc-dc converter.

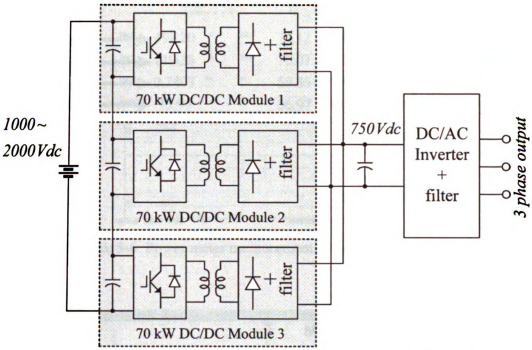


Figure 5-4 Overall system configuration of 210 kW aux. power supply

Figure 5-5 shows photo of the whole system test with three 70 kW converters are connected for a combined 210 kW.

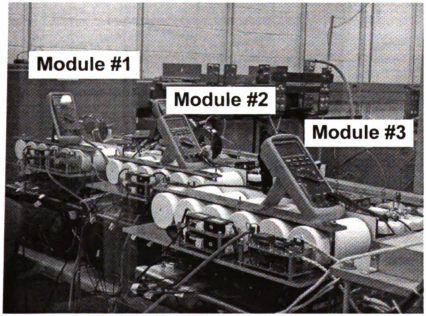


Figure 5-5 210 kW system test

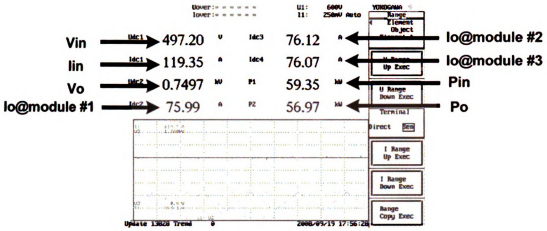


Figure 5-6 Power meter measurement of overall system test

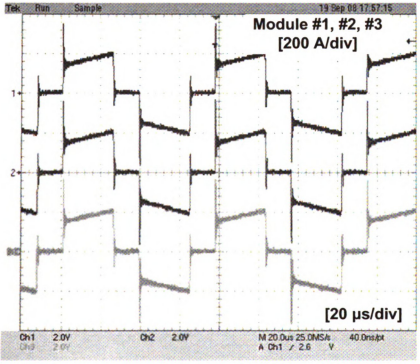


Figure 5-7 Transformer primary current of three DC-DC converter module.

Figure 5-6 shows the power meter measurement of the system test. The output power drawn from each dc-dc converter module is almost 57 kW, thus 57 kW×3=171 kW is drawn from dc-dc converter and output of the converter is maintained at 750 V. The three

output currents of the dc-dc converter module are quite well balanced as expected. Due to the isolation voltage limitation of the power meter, three input voltages of the DC-DC converter were not monitored. Instead, a multi-meter is used to monitor these voltages. The three input voltages of the DC-DC converter were also well balanced. Figure 5-7 shows the transformer primary current of each converter module measured during the system test.

5.3. Conclusion

In this chapter, a power loss breakdown is performed and its losses are compared. Three dc-dc converter modules are connected to test the whole system operation. The input voltage of dc-dc converters are connected in series and the output currents are connected in parallel. Due to the active voltage balancing and current sharing of the system, the system operation was performed successfully.

Chapter 6. Integrated Magnetics for Interleaved Boost DC-DC Converter for Series Hybrid Electric Bus

6.1. Introduction

In order to reduce CO_2 emission and to increase fuel efficiency of vehicles, electric vehicles (EVs), hybrid electric vehicles (HEVs), plug-in hybrid electric vehicles (PHEVs), and fuel-cell electric vehicles (FCEV) are now in increasing demand [39].

Figure 6-1 shows the overall system configuration of a series hybrid electric bus (SHEB). Mechanical energy from the diesel engine is first converted to electrical energy by the generator and this energy is used to drive motors through traction inverters.

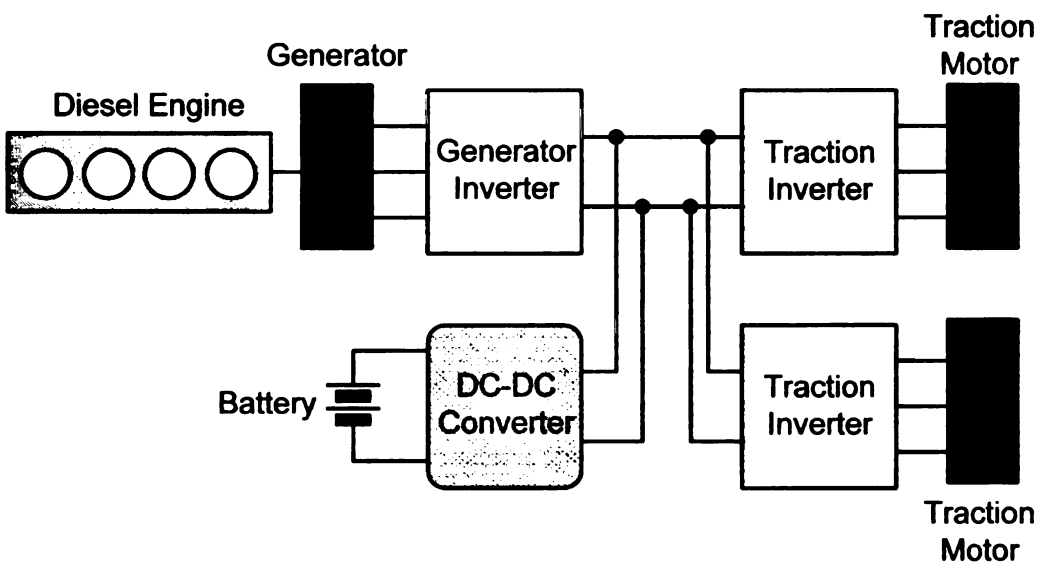


Figure 6-1 Overall system configuration of series hybrid electric bus

To maximize engine (fuel) efficiency, a battery is coupled to the dc link of the traction inverters through a bi-directional dc-dc boost converter. The dc-dc converter supplies battery energy to traction motors to meet the high power demand of traction motors during startup or acceleration and it delivers regenerated braking energy from the traction motors to the battery.

Table 6-1 shows electrical specifications of the battery and boost dc-dc converter considered in this work. Typically, dc-dc converters in HEV systems should handle both average and peak power demand. Therefore, the dc-dc converter in the HEV system plays an important role to maximize fuel efficiency. However, the dominant part of the boost converter, both in terms of size and cost, belongs to the magnetic components. Consequently, better use of the magnetic content of the dc-dc converter may lead to substantial performance and cost improvements.

Table 6-1 Electrical Specifications of battery and boost dc-dc converter.

Battery	• Voltage range: 240 – 340 VDC • Maximum current: 500 A
DC-DC converter	• Average power: 30 kW • Peak power: 120 kW • Input voltage: 240 – 340 VDC • Output voltage: 600-700 VDC • Switching frequency: 15 kHz

For the SHEB system considered in this work, a 3-phase interleaved boost converter (IBC) is considered and its schematics are shown in Figure 6-2. A 3-phase topology is chosen in order to meet the high power demand of the system and a standard six-pack IGBT module is used for this.

As already well known, the input (battery) current and output voltage ripple of IBC can be minimized by virtue of an interleaving operation [40-43]. Moreover, the converter input current can be shared among the phases, which is desirable for heat dissipation. Therefore, the converter reliability and efficiency can be improved significantly.

In this chapter, a very detailed design procedure for the integrated magnetic (IM) is presented and efforts are made to minimize core and winding loss of the IM. The input and inductor current ripples of IM are calculated theoretically and compared with measurements to verify the design of the IM. A 30 kW average and 120 kW peak power prototype IBC is built for the SHEB system and tested.

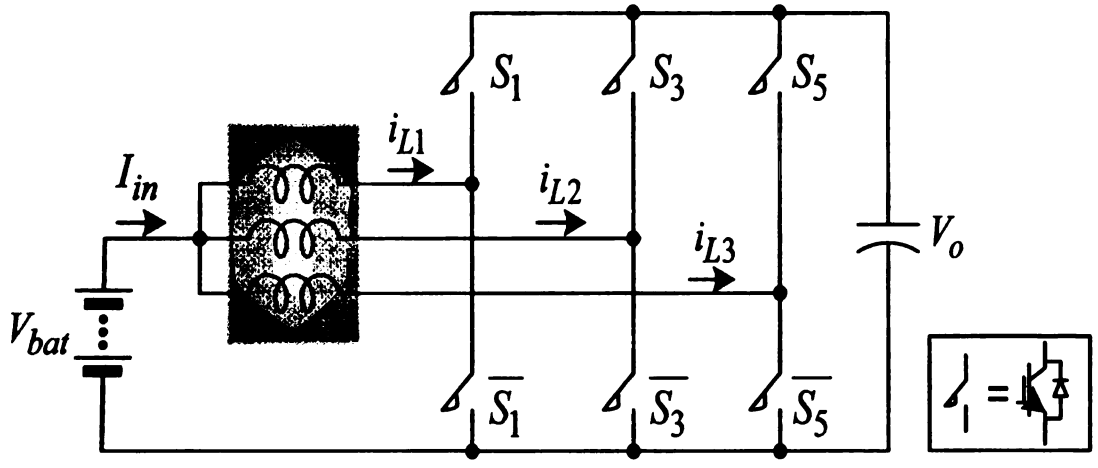


Figure 6-2 A 3-Phase interleaved boost converter

6.2. Interleaved Boost Converter and Integrated Magnetics

6.2.1 Review of Interleaved Boost Converter.

As already well known, the relationship between input current ripple (ΔI_{in}) and inductor current ripple ($\Delta I_{L.dis}$) in a multi-phase IBC is expressed as [40], [44].

$$\Delta I_{in} = f(D)\Delta I_{L.dis} \tag{8.1}$$

,where $\Delta I_{L.dis}$ is the current ripple of a discrete (or non-coupled) per-phase inductor, L_{dis}. The generalized equation for $f(D)$ for multi phase IBC is shown in (6.2). The derivation of $f(D)$ is out of the scope of this chapter and it is well explain in [40].

$$f(D) = \left(\frac{N_{on} + 1 - ND}{1 - D}\right)\left(1 - \frac{N_{on}}{ND}\right) \tag{6.2}$$

,where N is the number of phase and N_{on} is the number of switches that are always in the ON state during the sub-period, $\tau = \frac{T_s}{N}$.

Table 6-2 summarizes $f(D)$ derived for several values of N. From Table 6-2, the input current ripple normalized with respect to the inductor current ripple can be plotted for several multi phase IBC and the results are shown in Figure 6-3.

With the help of the interleaving effect, the input current ripple can be reduced significantly and the current interleaving effect becomes better as N increases. The effect of interleaving on the input current of 3 phase IBC, for example, is depicted in Figure 6-4, Figure 6-5 and Figure 6-6 for each converter duty cycle range.

Table 6-2 Calculation of $f(D)$ for N=2, 3 and 4

N=2				
	$0 \le D \le \frac{1}{2}$		$\frac{1}{2} \le D \le 1$	
N_{on}	0		1	
$f(D)$	$\frac{1-2D}{1-D}$		$\frac{2D-1}{D}$	
N=3				
	$0 \le D \le \frac{1}{3}$	$\frac{1}{3} \le D \le \frac{2}{3}$		$\frac{2}{3} \le D \le 1$
N_{on}	0	1		2
$f(D)$	$\frac{1-3D}{1-D}$	$\left(\frac{2-3D}{1-D}\right)\left(1-\frac{1}{3D}\right)$		$\frac{3D-2}{D}$
N=4				
	$0 \le D \le \frac{1}{4}$	$\frac{1}{4} \le D \le \frac{2}{4}$	$\frac{2}{4} \le D \le \frac{3}{4}$	$\frac{3}{4} \le D \le 1$
N_{on}	0	1	2	3
$f(D)$	$\frac{1-4D}{1-D}$	$\left(\frac{2-4D}{1-D}\right)\left(1-\frac{1}{4D}\right)$	$\left(\frac{3-4D}{1-D}\right)\left(1-\frac{1}{2D}\right)$	$\frac{4D-3}{D}$

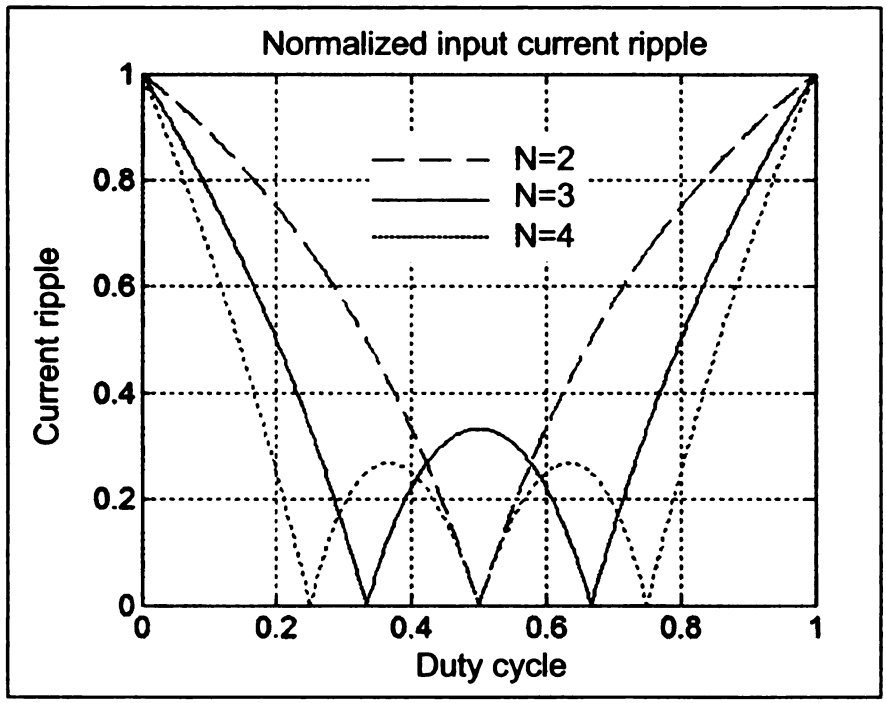


Figure 6-3 Normalized input current ripple of IBC

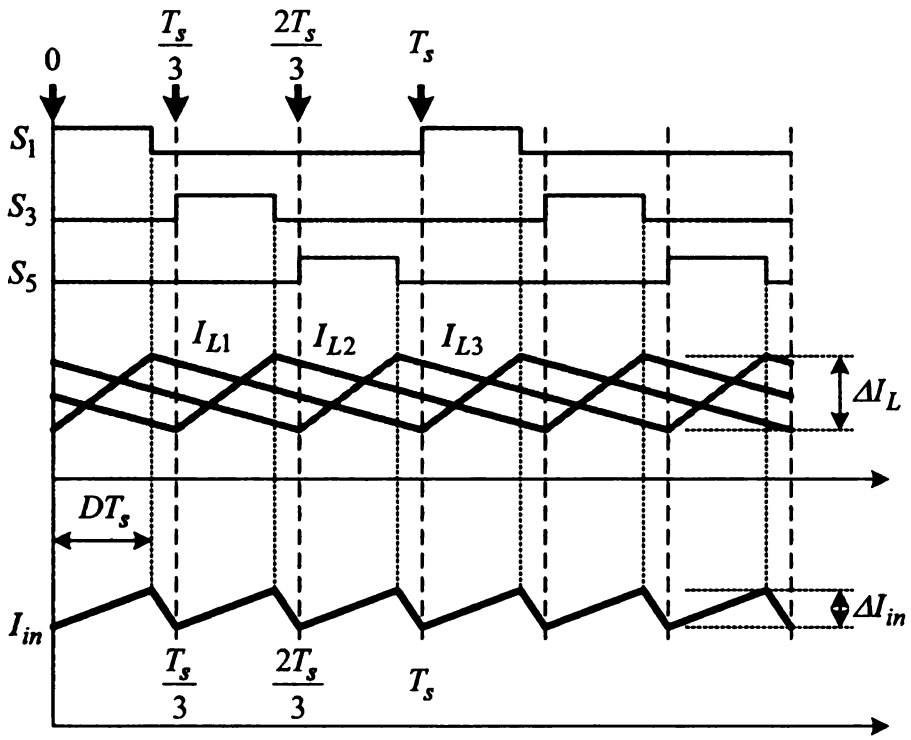


Figure 6-4 Inductor current interleaving when 0 < D <1/3.

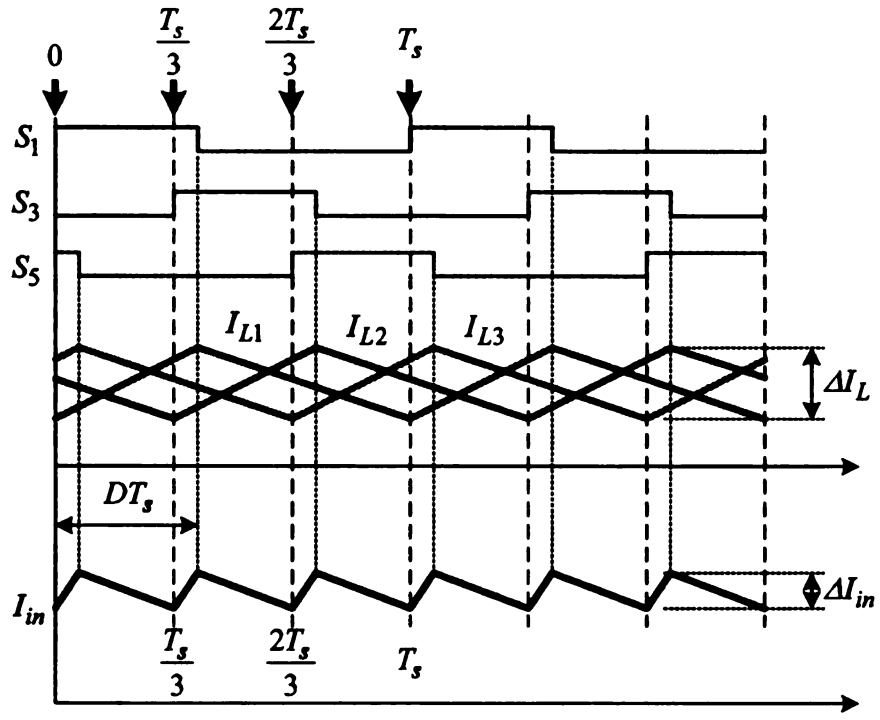


Figure 6-5 Inductor current interleaving when 1/3 < D <2/3.

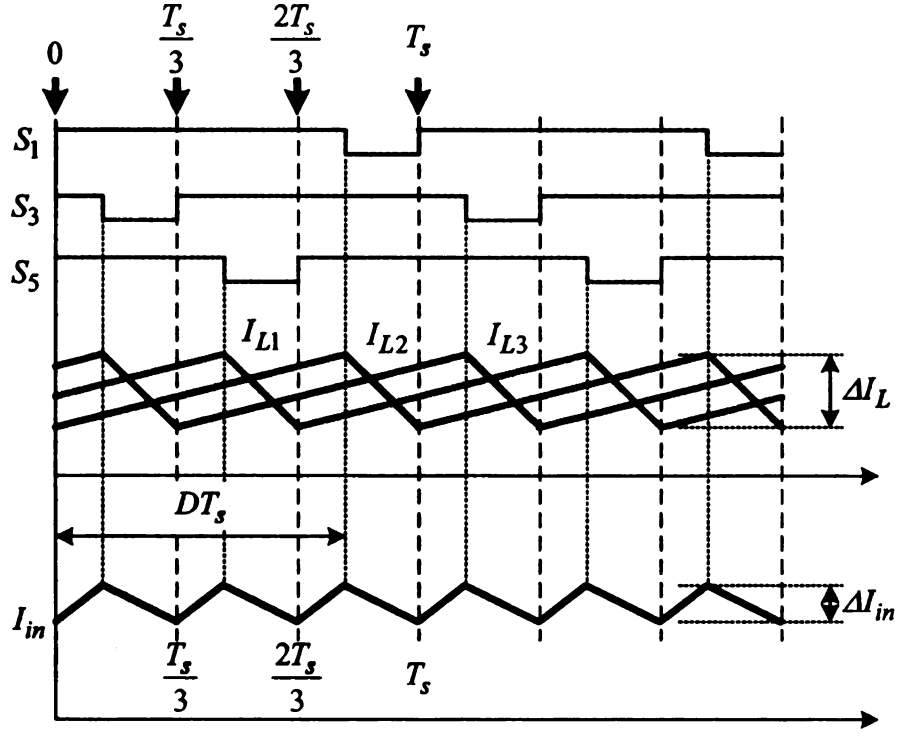


Figure 6-6 Inductor current interleaving when 2/3 < D <1.

6.2.2 Integrated Magnetics

Recently, an interesting integrated magnetic (IM) structure having 3 outer legs and one common leg using different core material for outer and common legs was introduced in [44]. Figure 6-7, Figure 6-8, and Figure 6-9 show the core structure, winding geometry, and the reluctance model of IM, respectively. Two different core materials are used for common leg and outer legs. The 3 phase windings are wound on each outer leg.

The R_L and R_c in Figure 6-9 represent the reluctance in outer and common leg, respectively. N is the number of turns in each winding. I_{L1}, I_{L2}, I_{L3} represent the winding current in the IM core.

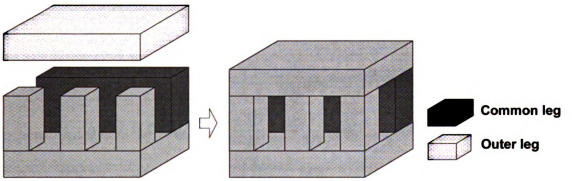


Figure 6-7 Core structure of 3 phase IM

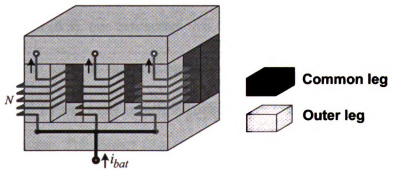


Figure 6-8 IM assembled with winding

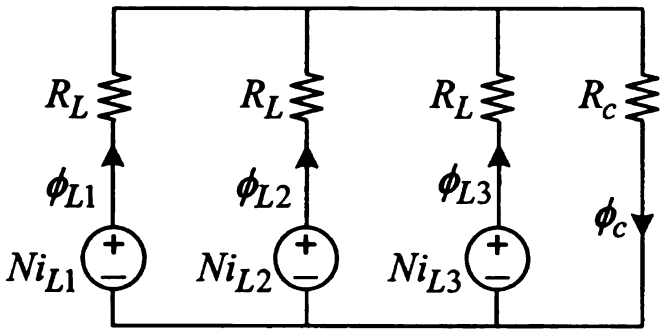


Figure 6-9 Reluctance model of IM

The common leg flux (ϕ_C) is equal to the sum of the three outer leg fluxes (ϕ_{L1}, ϕ_{L2}, ϕ_{L3}) due to the IM core structure shown in Figure 6-7. In this case, the common leg flux ripple ($\Delta\phi_C$) can be reduced due to flux interleaving. The relationship between $\Delta\phi_C$ and $\Delta\phi_L$ is expressed as follows.

$$\Delta\phi_c = f(D)\Delta\phi_L = \begin{cases} \left(\frac{1-3D}{1-D}\right)\Delta\phi_L & , 0 \le D \le \frac{1}{3} \\ \left(\frac{2-3D}{1-D}\right)\left(1-\frac{1}{3D}\right)\Delta\phi_L & , \frac{1}{3} \le D \le \frac{2}{3} \\ \left(\frac{3D-2}{D}\right)\Delta\phi_L & , \frac{2}{3} \le D \le 1 \end{cases} \tag{6.3}$$

where, D is duty cycle of the converter.

From (6.1) and (6.3), one can notice that the relationship between $\Delta\phi_C$ and $\Delta\phi_L$ in (6.3) is exactly the same as the relationship between ΔI_{in} and $\Delta I_{L.dis}$ in (6.1) because they are governed by the same principle called interleaving. The only difference is the object of interleaving. The former (Eq. (6.1)) is current and the latter (Eq. (6.3)) is flux. Therefore, the flux ripple waveforms in IM can be similarly represented as the current waveforms in Figure 6-4, Figure 6-5 and Figure 6-6 . From the reluctance model in

gure 6-9, the outer leg fluxes and the winding currents in the IM core are related by

4]

$$\begin{bmatrix} I_{L1} \\ I_{L2} \\ I_{L3} \end{bmatrix} = \frac{1}{N} \begin{bmatrix} R_L + R_c & R_c & R_c \\ R_c & R_L + R_c & R_c \\ R_c & R_c & R_L + R_c \end{bmatrix} \begin{bmatrix} \phi_{L1} \\ \phi_{L2} \\ \phi_{L3} \end{bmatrix} \tag{6.4}$$

Therefore, the inductor current ripple is expressed as

$$\Delta I_{L1} = \frac{1}{N}\left(R_L \Delta\phi_{L1} + R_C \Delta\phi_c\right) \tag{6.5}$$

It should be noted in (6.5) that the inductor current ripple is related to both outer leg and common leg flux ripple through the multiplication of reluctance values. However, the common leg flux ripple is relatively small compared with outer leg flux ripple due to the flux interleaving. Therefore, by making $R_C \Delta\phi_c$ term dominant in (6.5) ΔI_{L1} can be reduced significantly. In other words, R_C should be bigger than R_L.

In Figure 6-2, I_{in} is the sum of the three inductor currents. Thus, the relationship between ΔI_{in} and $\Delta\phi_C$ is found from (6.4) as

$$\Delta I_{in} = \left(\frac{R_L + 3R_C}{N}\right)\Delta\phi_c \tag{6.6}$$

$\Delta\phi_C$ in (6.6) is expressed as

$$\Delta\phi_c = f(D)\Delta\phi_L = f(D)\left(\frac{V_{in} D T_s}{N}\right) \tag{6.7}$$

The discrete per-phase inductance L_{dis} is

$$L_{dis} = \frac{V_{in} D T_s}{\Delta I_{L.dis}} \tag{6.8}$$

Therefore, from (6.1), (6.6), (6.7) and (6.8), L_{dis} can be derived as

$$L_{dis} = \frac{N^2}{R_L + 3R_c} \tag{6.9}$$

In this work, L_{dis} is chosen to have the same flux ripple (waveform) in both non-integrated inductor and IM implementation.

The relationship between ΔI_L and $\Delta I_{L.dis}$ can be determined from the above equations as

$$\Delta I_L = \left(\frac{1 + \frac{R_c}{R_L} f(D)}{1 + 3\frac{R_c}{R_L}} \right) \Delta I_{L.dis} = \left(\frac{1 + \frac{f(D)}{k}}{1 + \frac{3}{k}} \right) \Delta I_{L.dis} \tag{6.10}$$

From (6.10), one can notice that the inductor current ripple of IM (ΔI_L) is related to $\Delta I_{L.dis}$ by the ratio of R_L to R_c, which is defined as k in this work.

By using (6.1) and (6.10), ΔI_{in} and ΔI_L normalized with respect to $\Delta I_{L.dis}$ are plotted in Figure 6-10 as a function of D for several values of k. As shown in Figure 6-10, ΔI_{in} (dotted line) was reduced significantly by the effect of interleaving and ΔI_L is strongly related to k. Therefore, k should be kept low to reduce ΔI_L.

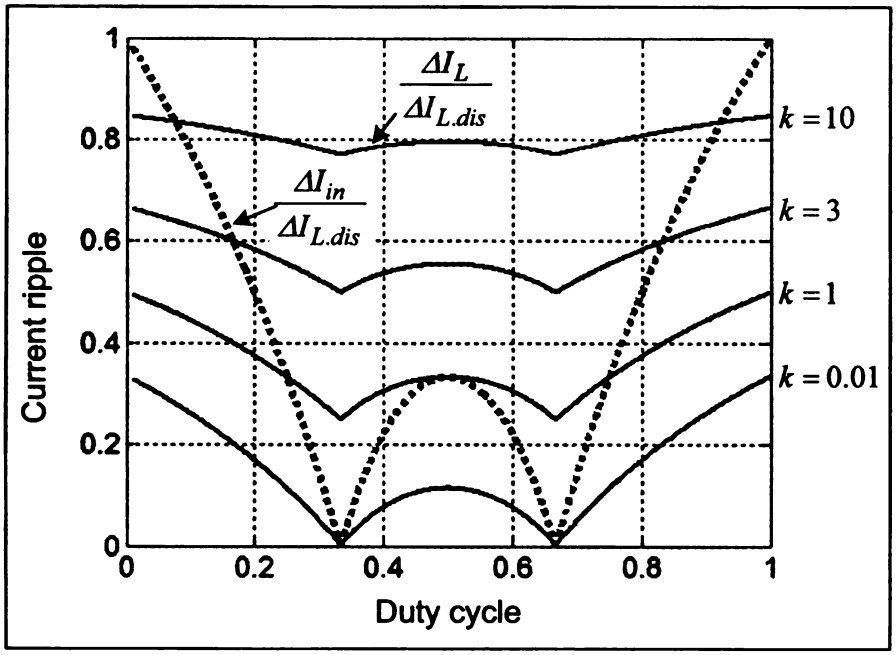


Figure 6-10 Normalized current ripple as a function of D for several values of k.

6.3. Design of High Efficient and High Density Integrated Magnetics

The previously proposed scheme shown in Figure 6-7 used ferrite core for outer leg and powdered iron core for the common leg in order to maintain low values of k because the permeability of ferrite core is several hundred times bigger than that of powdered iron core. Therefore, inductor current ripple in IM can be reduced significantly. In addition to this, core loss in the outer legs can be minimized by using ferrite core.

Although the core loss of powdered iron core used for common leg is typically higher than ferrite, the core loss in the common leg in this structure, however, can also be minimized because $\Delta\phi_C$ is reduced significantly through flux interleaving. As a consequence, the IM showed good performance, low total core loss, and minimized inductor size.

However, there are some limitations of using ferrite core in high current and high temperature applications such as HEVs, EVs, and PHEVs for the following reasons.

First, the peak power of dc-dc converters used in HEVs or EVs is usually 3-5 times greater than the average power of dc-dc converter to meet the high power demand of traction motors during startup and acceleration (see Table 6-1). Thus, the maximum inductor current is greater than nominal inductor current by the same amount as power. In this condition, inductor design using ferrite core is very difficult because the maximum flux density (B_{max}) of ferrite core is usually low (≈0.4-0.45 T) when compared with that of distributed airgap cores such as MPP, high flux, mega flux, etc [16], [45].

Secondly, the B_{max} of ferrite cores usually decreases as core temperature increases. The result is earlier saturation of the core than designed when ambient temperature is high.

In order to be applicable to high current and high temperature systems, the core B_{max} should be high enough and be kept fairly constant even at elevated core temperature.

Table 6-3 compares the key properties of several magnetic powder cores considered in this work and they are compared with ferrite core [25]. From the results of Table 6-3, the "high flux" core is selected for core material for both outer and common leg in this work because it has low core loss, high saturation flux density, and good temperature stability. The core loss of "high flux", however, is normally higher than that of ferrite. This will increase core loss and temperature in outer legs and eventually decreases converter efficiency.

Table 6-3 Basic Material Characteristics

Core materials	Core loss	Permeability vs. DC bias	Cost	Saturation Flux density (Gauss)	Temperature stability
MPP	Lowest	Better	High	7,000	Best
High flux	**Low**	**Best**	**Medium**	**15,000**	**Better**
Iron	Highest	Poor	Lowest	10,000	Poor
Amorphous (gapped)	Medium	Better	Highest	15,000	Poor
Ferrite (gapped)	Lowest	Poor	Low	4,500	Poor

* 1 Tesla=10^4 Gauss

However, there are several ways of minimizing core loss in the outer legs. 1) Increase number of turns to reduce flux swing of core, but it will increase winding loss of inductor. 2) Reduce core volume because core loss is directly proportional to core volume. However, the core cross-sectional area should not be reduced. Otherwise, the flux swing will increase and result in higher core loss.

In this work, the height of IM is reduced as much as possible while maintaining same outer leg core cross-sectional area for the following reasons: 1) Core loss in the outer leg is the dominant loss factor because the flux in this leg is not interleaved. Thus, one can

reduce outer leg core loss with minimized core height. 2) Thermal resistance from the inside of the core to the outside can be decreased with this flat inductor approach, which is good for heat dissipation.

However, $B_{\max}$ of the core increases as core height decreases because the airgap in powder (or distributed airgap) core is also reduced when core height decreases. The result is that the magnetic core is more susceptible to core saturation [16].

In this work, however, the core saturation problem caused by reduced core height can be resolved by using "high flux" core that has high saturation flux density (see Table 6-3). In addition to that, the core saturation problem in the outer leg can be mitigated by using low permeability core material for the common leg because it will decrease $B_{\max}$ of the outer leg core. Therefore, $B_{\max}$ of the outer and common leg core can be controlled to a reasonable number by the optimal combination of outer leg and common leg core structure and selection of core permeability. This will be explained later in this section.

Figure 6-11 and Figure 6-12 show the core structure of the flat IM designed in this work. In this work, the magnetic core surrounded by inductor winding is defined as outer leg and the rest of them are defined as common leg.

The reluctance R_L and R_C are calculated by using the following equation as [16]

$$R = \frac{l_m}{\mu_o \mu_r S} \tag{6.11}$$

where, l_m is the magnetic path length of IM, $\mu_o = 4\pi \times 10^{-7}$ is the permeability in air, μ_r is the relative permeability of "high flux" core and S is the core cross-sectional area.

However, permeability of the distributed airgap core rolls off as the DC magnetizing force ($H[Oe]$) increases [25].

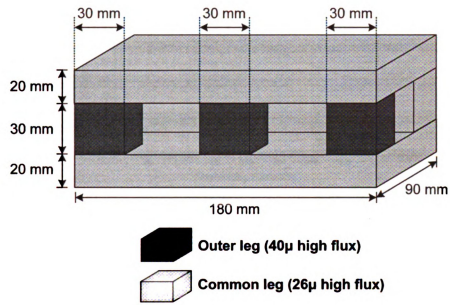


Figure 6-11 Proposed flat IM. (Front view)

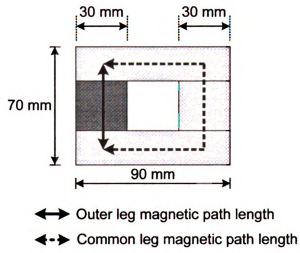


Figure 6-12 Proposed flat IM. (Side view)

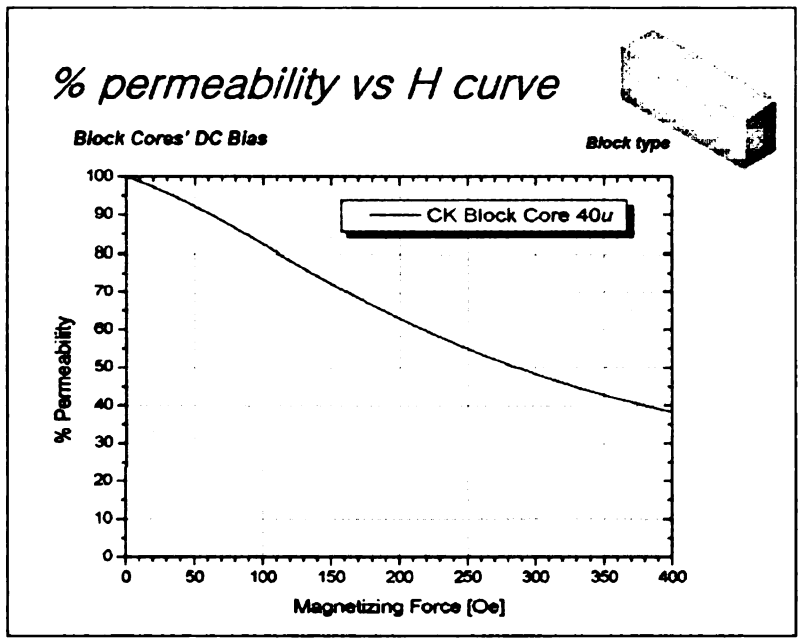


Figure 6-13 % permeability vs. H curve of Changsung 40μ block core

Figure 6-13 shows one example of this characteristic. Thus, care must be taken when designing inductors with distributed airgap cores.

H is calculated by using Ampere's law as follows and its unit is oersteds.

$$H = \frac{0.4\pi NI}{l_m}[Oe] \tag{6.12}$$

In (6.12), I is the DC current that flows through the inductor and l_m is the magnetic path length in cm. Detailed parameters for calculating reluctances are summarized in Table 6-4. In Table 6-4, the core cross-sectional area for the common leg is calculated separately because of its structure. (see Figure 6-11 and Figure 6-12). Therefore, the R_C is also calculated individually and they are added together to make total R_C. The % permeability of "high flux" core is obtained from the manufacturer datasheet.

Table 6-4 Parameters of IM core

	Outer leg (40μ)	Common leg (26μ)
Core cross-sectional area (S)	30×30=900 mm^2	Top and Bottom piece: 180×20=3600 mm^2 Middile piece: 180×30=5400 mm^2
Magnetic path length (l_m)	10+10+30=50 mm	60+60+50=170 mm
H@40 A	$\frac{0.4\times\pi\times28\times40}{5}=281[Oe]$	$\frac{0.4\times\pi\times28\times40}{17}\approx83[Oe]$
% permeability	50	96
μ_r @40 A	40×0.5=20	26×0.96=24.96
Reluctance	2687952	1358625
$k=\frac{R_L}{R_C}$	$k=\frac{2687952}{1358625}=1.978$	

In this work, I is set to 40 A, which is the nominal DC current at 30 kW average power. If I is known, H can be determined from (6.12). Therefore, the permeability at this point is determined from the % permeability curve and they are shown in Table 6-4 as 50 % and 96 % for outer leg and common leg core, respectively.

With the parameters in Table 6-4, the R_L and R_C can be calculated by using (6.11) and the results are also shown in Table 6-4.

In order to verify the reluctance values calculated in Table 6-4, a square wave voltage is applied to the winding of outer leg 2, and the windings in outer leg 1 and 3 are left open-circuited. Figure 6-14 shows the modified reluctance model with this condition.

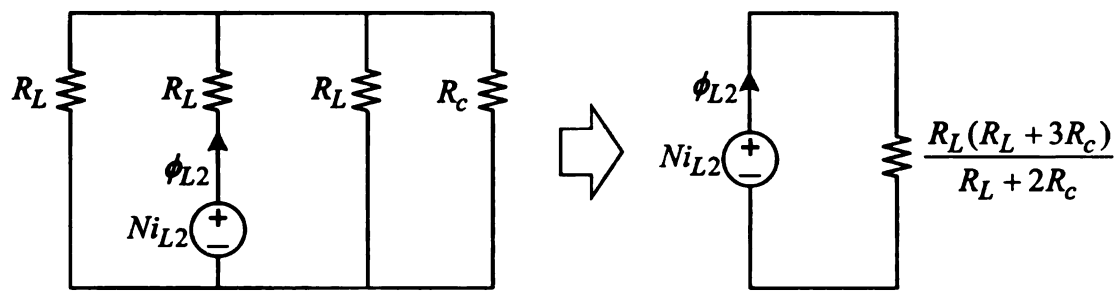


Figure 6-14 Modified reluctance model when a voltage is applied to only outer leg 2.

When the windings are left open-circuited, the mmfs in those windings become zero because there is no current that flows in those windings. Therefore, the mmfs in winding 1 and 3 are short-circuited as shown in Figure 6-14 and the circuit is simplified to one mmf and one reluctance value.

From Figure 6-14, the inductance in leg 2 is calculated as follows

$$L_{(@I=40A)} = N^2 \frac{(R_L + 2R_C)}{R_L(R_L + 3R_C)} = 233\,\mu H \tag{6.13}$$

The inductances in leg 1 and leg 3 can be calculated with similar method and they should be the same as the inductance in leg 2 if they experience the same flux path.

In order to confirm the calculated inductance value in (6.13), a square wave voltage is applied in each winding one by one and the corresponding inductances are measured. Figure 6-15 shows the inductances in each leg measured by increasing applied current. As we expected, the inductance drops as current increases.

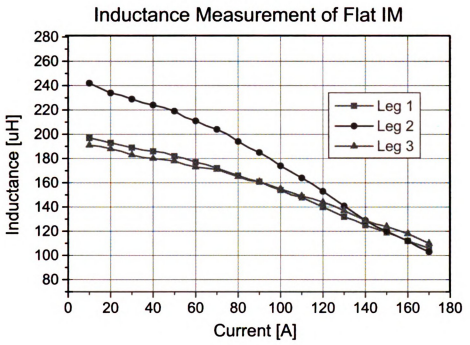


Figure 6-15 Inductance measurement of IM

The measured and calculated inductances are shown in Table 6-5 for comparison.

Table 6-5 Measured inductances of flat IM at 40 A

		Calculation	Measurement
Inductance @ 40 A	L1, (Leg 2,3 open)	$233\,\mu H$	$186\,\mu H$
	L2, (Leg 1,3 open)	$233\,\mu H$	$224\,\mu H$
	L3, (Leg 1,2 open)	$233\,\mu H$	$180\,\mu H$

From the results of Table 6-5, the measured inductance is smaller than the calculated ones. This is caused by the unwanted airgap that inserted between block cores when they are glued together. In addition to that, the three measured inductances are not the same because the magnetic path length of each leg is different. For example, the magnetic path length in leg 2 is shorter than that of leg 1 and 3. Therefore, leg 2 has greater inductance than leg 1 and leg 3.

With the reluctance values calculated in Table 6-5, the inductance value of a non-coupled inductor can be calculated by using (6.9) as follows

$$L_{dis} = \frac{N^2}{R_L + 3R_C} \approx 116\,\mu H \tag{6.14}$$

The dc-dc converter discussed in this paper should operate at 120 kW peak power during startup and acceleration and the battery (or input) current is 500 A at this condition. Therefore, the maximum inductor current ($I_{L.\max}$) becomes 500 A/3=167 A. The magnetic cores used in IM should not be saturated at this harsh condition. Maximum flux density in the outer leg ($B_{L.\max}$) and common leg ($B_{C.\max}$) are calculated using the following equations as

$$B_{L.\max} = \frac{N \times i_{L.\max}}{S_L(R_L + 3R_C)} \approx 0.69T \tag{6.15}$$

$$B_{C.\max} = \frac{\phi_C}{S_C} = \frac{3\phi_L}{S_C} = \frac{3N \times i_{L.\max}}{S_C(R_L + 3R_C)} \approx 0.52T \tag{6.16}$$

where, S_L and S_C are the core cross-sectional area of the outer leg and common leg, respectively. From (6.15) and (6.16), the maximum flux density of both outer and common leg is well below "high flux" core saturation flux density which is 1.5 T.

6.4. Experimental Results

A 30 kW average and 120 kW peak power IBC using IM is built and tested. Figure 6-16 shows the experimental waveforms of the dc-dc converter with the test conditions of Vin=300 V, Vo=600 V, D=0.5, fsw=15 kHz and Po=37 kW.

Current ripple of the non-coupled inductor, $\Delta I_{L.dis}$, at this condition can be calculated as

$$\Delta I_{L.dis} = \frac{V_{in} \times D}{L_{dis} \times f_{sw}} = \frac{300 \times 0.5}{116\,\mu H \times 15 kHz} \approx 86\,A \tag{6.17}$$

Therefore, ΔI_{in} and ΔI_L of IM are calculated by using (6.1), (6.10) and the k value in Table 6-4 as

$$\Delta I_{in} = f(D)\Delta I_{L.dis} \approx 29\,A \tag{6.18}$$

$$\Delta I_L = \left(\frac{1 + \frac{f(D)}{k}}{1 + \frac{3}{k}} \right) \Delta I_{L.dis} \approx 40\,A \tag{6.19}$$

The measured current ripples of IM in Figure 6-16 are close to the calculated current ripple in (6.18) and (6.19).

The current ripple in outer leg 1 (ΔI_{L1}) is bigger than that of leg 2 (ΔI_{L2}) because the inductance of leg 1 is smaller than leg 2 (see Table 6-5).

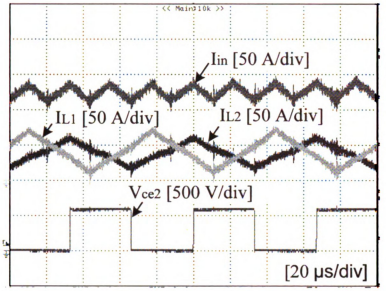


Figure 6-16 Experimental waveforms of IBC using IM when D=0.5.

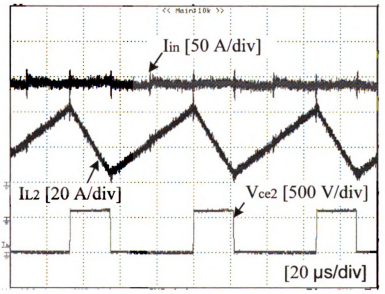


Figure 6-17 Experimental waveforms of IBC using IM when D=2/3.

Figure 6-17 shows the experimental waveforms of IM when Vin=200 V, Vo=600 V, D=2/3, fsw=15 kHz and Po=37 kW. From the curves shown in Figure 6-10, ΔI_{in} when D=2/3 is ideally zero and ΔI_L is calculated as

$$\Delta I_L = \left(\frac{1+\frac{f(D)}{k}}{1+\frac{3}{k}} \right) \Delta I_{L.dis} = \left(\frac{1}{1+\frac{3}{k}} \right) \Delta I_{L.dis} \approx 30\,A \qquad (6.20)$$

The experimental waveforms are also close to theoretical analysis.

Figure 6-18 and Figure 6-19 show the inductor and input current waveforms when Vin=300 V, Vo=600 V, D=0.5, fsw=15 kHz and Po=120 kW. At this peak power condition, the input and inductor current are 500 A and 167 A, respectively. When compared with 30 kW average power, the input and inductor current increase to 4 times. The increased currents cause more roll-off in core permeability. As a consequence, inductance drops and current ripple increases.

Figure 6-20 shows a photo of the prototype IM developed in this work. In order to protect the inductor from mechanical vibration and other stresses, the IM is molded in an aluminum case and the final assembly is shown in Figure 6-21. An added benefit of the molded inductor is better heat dissipation than an air cooled inductor.

In order to calculate the core loss in both outer and common leg, a peak-to-peak flux swing of the core is calculated. Table 6-6 summarizes detailed parameters of the IM and calculated core and winding loss of the IM.

To confirm the calculated power loss in Table 6-6, internal temperature of the IM is measured. Figure 6-22 shows the measured temperature increase under the test condition of Vin=330 V, Vo=660 V, D=0.5, fsw=15 kHz and Po=33 kW. After 1 hour and 40

minutes of operation at 60 °C ambient temperature, the internal temperature was almost saturated to 93 °C.

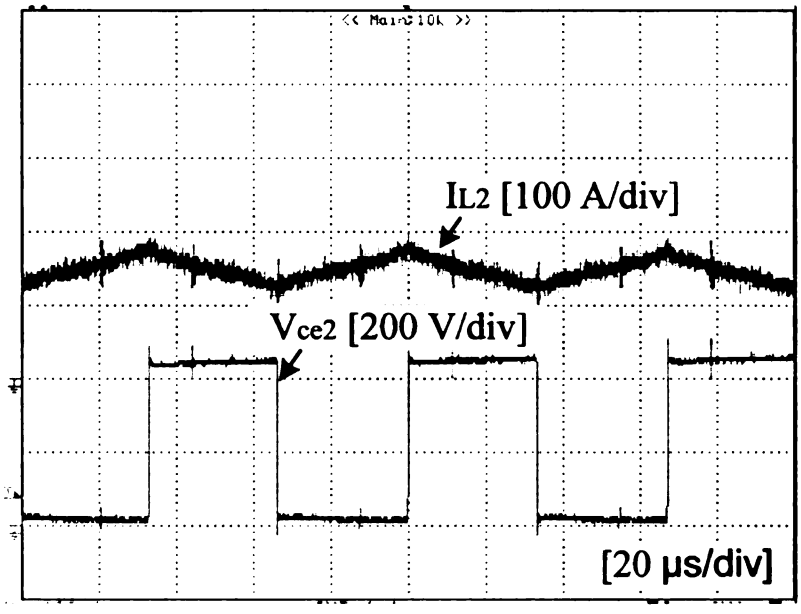


Figure 6-18 Inductor current and IGBT switching waveforms at 120 kW.

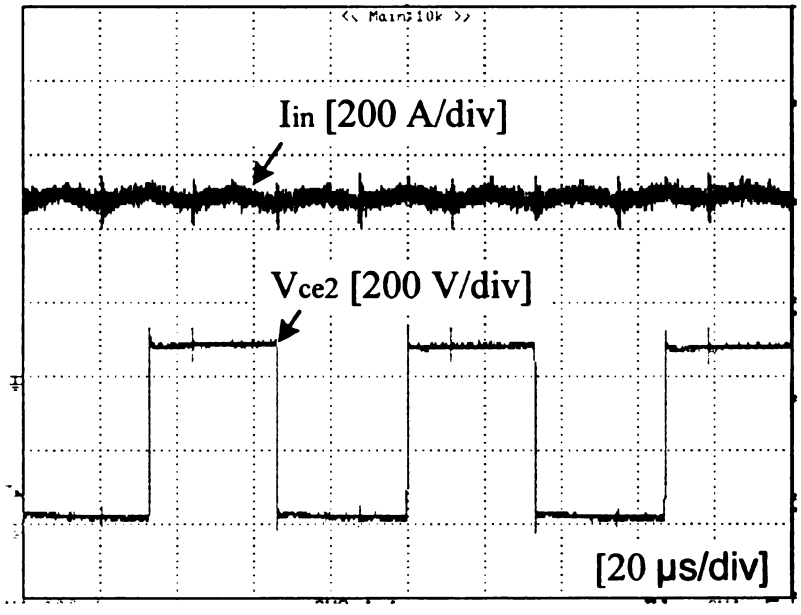


Figure 6-19 Input current and IGBT switching waveforms at 120 kW.

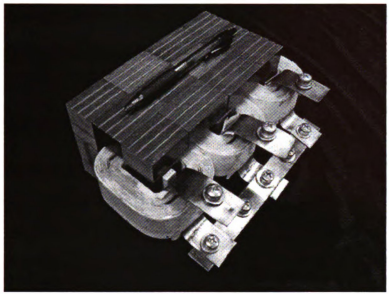


Figure 6-20. Photo of prototype IM before molding.

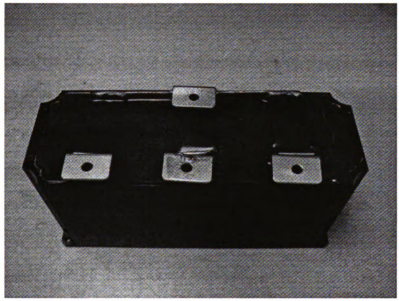


Figure 6-21 Photo of molded IM after molding

Table 6-6 Calculation of power losses in IM

<table>
<tr><td colspan="2">Copper winding</td><td colspan="2">• Thickness: 0.533 mm
• Width: 25.4 mm
• Mean length/turn: 188 mm
• No. of turns: 28</td></tr>
<tr><td colspan="2">Total winding loss @ 40 A</td><td colspan="2">44 W</td></tr>
<tr><td rowspan="2">Flux swing</td><td>Outer leg</td><td colspan="2">0. 4 T</td></tr>
<tr><td>Common leg</td><td colspan="2">0.03 T</td></tr>
<tr><td rowspan="2">Core loss</td><td>Outer leg</td><td>25 W</td><td rowspan="2">33 W</td></tr>
<tr><td>Common leg</td><td>8 W</td></tr>
<tr><td colspan="2">Total power loss in IM</td><td colspan="2">77 W</td></tr>
</table>

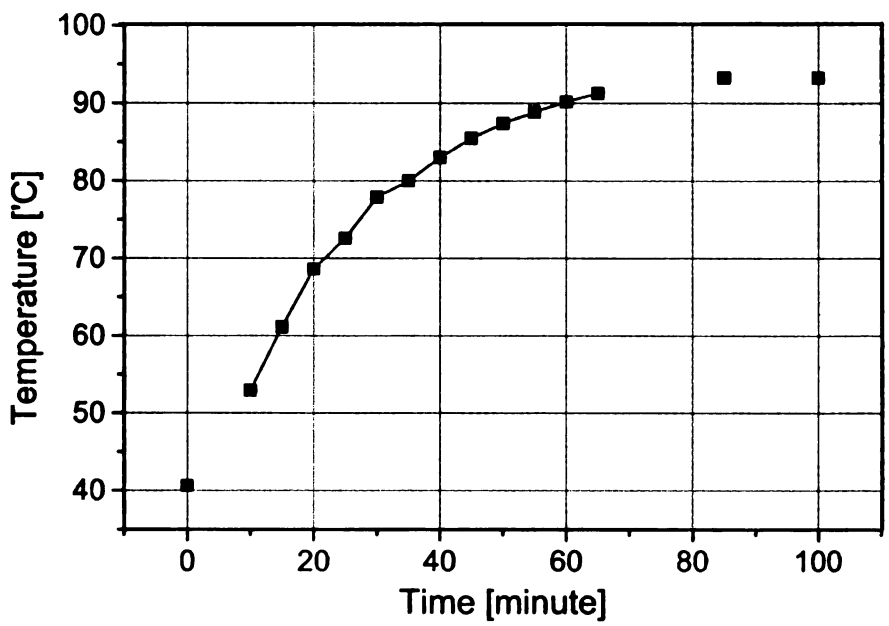


Figure 6-22 Temperature increase of IM

6.5. Conclusion

In this chapter, a very detailed design procedure, for designing high efficient and high density IM for 3-phase interleaved boost dc-dc converter for series hybrid electric bus, is presented. A flat IM is designed to reduce core loss in the outer leg. Theoretical calculation of inductor and input current ripples are compared with experimental waveforms to verify the performance of IM. A 30 kW average and 120 kW peak power IBC was built and successfully tested to verify the operation of IM.

Chapter 7. Distributed Z-Source Network DC-DC Converter

7.1. Introduction

As already mentioned and pointed out in Chapter 1, traditional transformer isolated dc-dc power conversion circuits are based on either a voltage-source (V-source) or current-source (I-source) structure. A V-source converter is fed from a power source with relatively constant voltage that is generally supported with capacitors (Figure 7-1) and an I-source converter is fed from a power source with relatively constant current that is generally smoothed through an inductor (Figure 7-2) [46]. The V-source FB converter shown in Figure 7-1 has the following limitations [1], [46].

- The output voltage of converter is always lower than input voltage. In other words, the input voltage has to be greater than output voltage.
- The upper and lower devices of each phase leg cannot be gated on simultaneously either by purpose or by EMI noise. Otherwise, a shoot-through would occur and destroy the devices. The shoot-through problem by electromagnetic interference (EMI) noise's misgating-on is a major killer to the converter's reliability.
- The voltage overshoot problem in secondary rectifier diodes is severe [27], [9], [47]. Therefore, a voltage snubber (or clamp) circuit is required to limit voltage overshoot in rectifier diodes. The added circuitry, however, may decrease converter efficiency and system reliability.

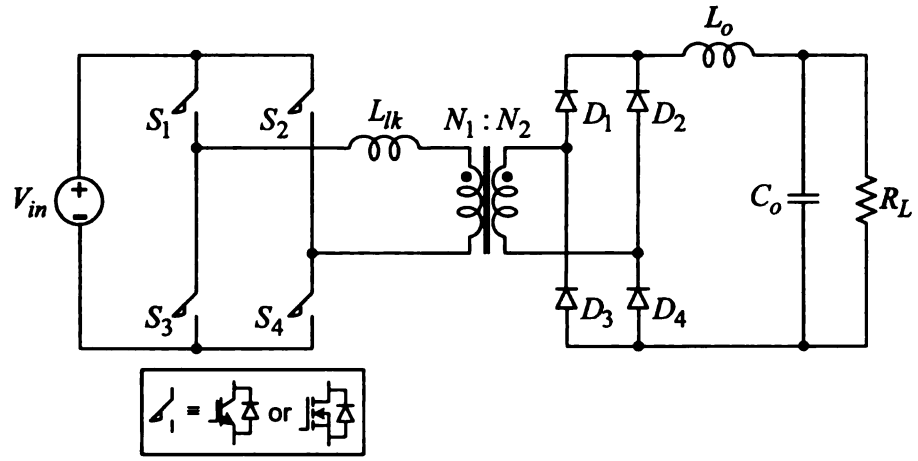


Figure 7-1 V-source FB PWM DC/DC converter.

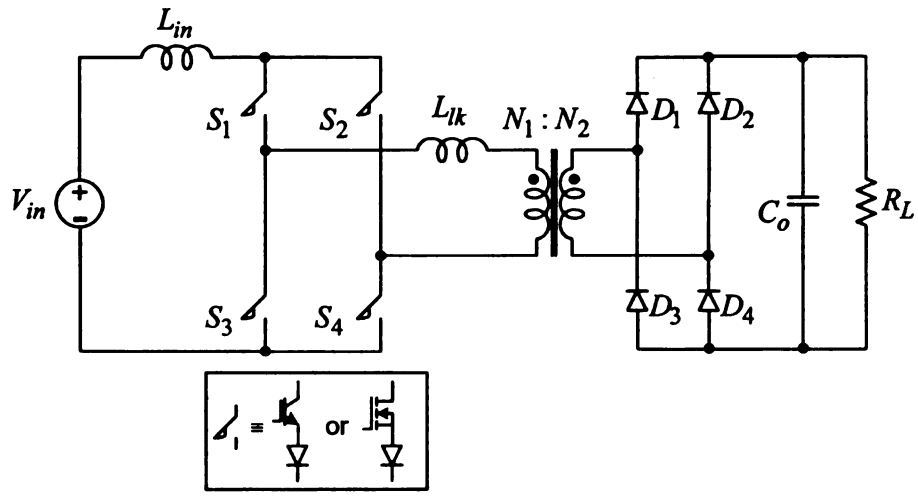


Figure 7-2 I-source FB PWM DC/DC converter.

Likewise, the I-source FB converter shown in Figure 7-2 has the following limitations.

- Output voltage of the converter is always greater than input voltage. In other words, the input voltage has to be smaller than output voltage.
- At least one of the upper devices and one of the lower devices have to be gated on and maintained on at any time. Otherwise, an open circuit of the dc inductor

would occur and destroy the devices. The open-circuit problem by EMI noise's misgating-off is a major concern of the converter's reliability.

- The voltage overshoot problem in primary switches (S1-S4) is also a big concern [48-51].

From the aforementioned reasons, the two traditional circuits shown in Figure 7-1 and Figure 7-2 can only produce output voltage smaller than or greater than input voltage. Therefore, there is only buck (step down) or boost (step up) function in conventional bridge-type converters and they do not have both the buck and boost function.

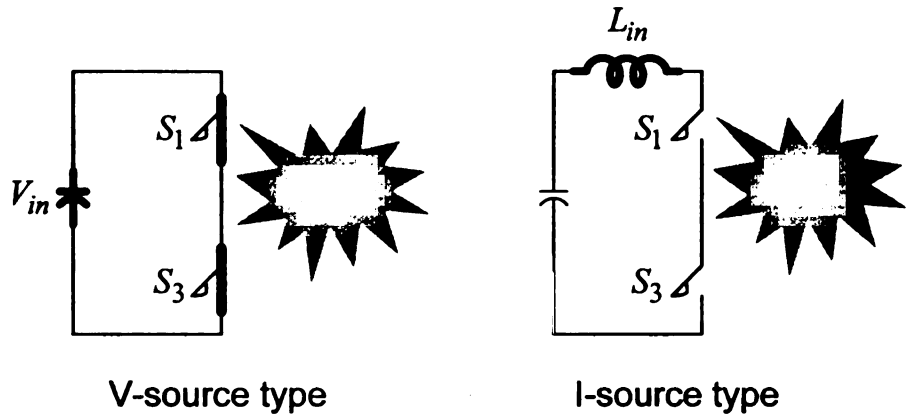


Figure 7-3 The effect of EMI or misgating on switching device.

Figure 7-3 summarizes the effect of EMI noise or misgating on/off on switching devices. The left circut in Figure 7-3 shows the switch failure mechanism of V-source type converter system where upper and lower devices of each phase leg are connected in series with source. When there is a misgating-on in the gate signal, the phase leg is short-circuited and the input capacitor will be discharged through the phase leg. Therefore, the switching devices in the phase leg would be damaged by over current.

Similarly, when there is a misgating-off in the gate signal of an I-source type converter system shown in the right of Figure 7-3, the energy stored in the input inductor will be transferred to the junction capacitance of the switching devices. Therefore, the switching devices in the phase leg would be damaged by over voltage. From the reasons mentioned above, the conventional V-source or I-source converters are very vulnerable to EMI noise. As a result, system reliability of these converters is greatly impaired.

7.2. Why buck-boost converter?

In section 7.1, it is mentioned that the conventional dc-dc converters have only buck or boost function and they do not have the desired buck and boost function. In this section, a buck-boost converter is examined and its main advantages over buck (or boost) converter will be addressed. Figure 7-4 and Figure 7-5 show the two very basic converter topologies used in power electronics; buck converter and boost converter.

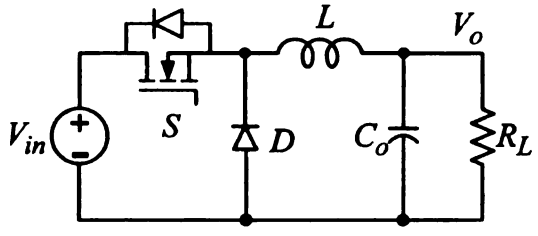


Figure 7-4 Buck converter

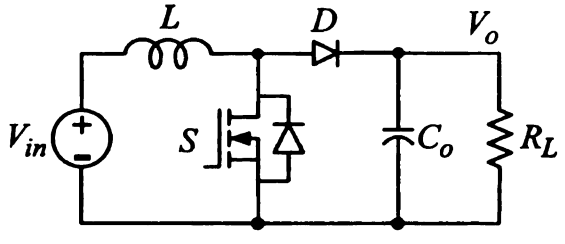


Figure 7-5 Boost converter

Figure 7-6 depicts the input and output voltage relationships of the buck, boost and buck-boost converter. For the buck converter, the output voltage is always equal or smaller than minimum input voltage. For the boost converter, the output voltage is always equal or greater than maximum input voltage. For the buck-boost converter, however, the output voltage lies in between the input voltage range of the converter.

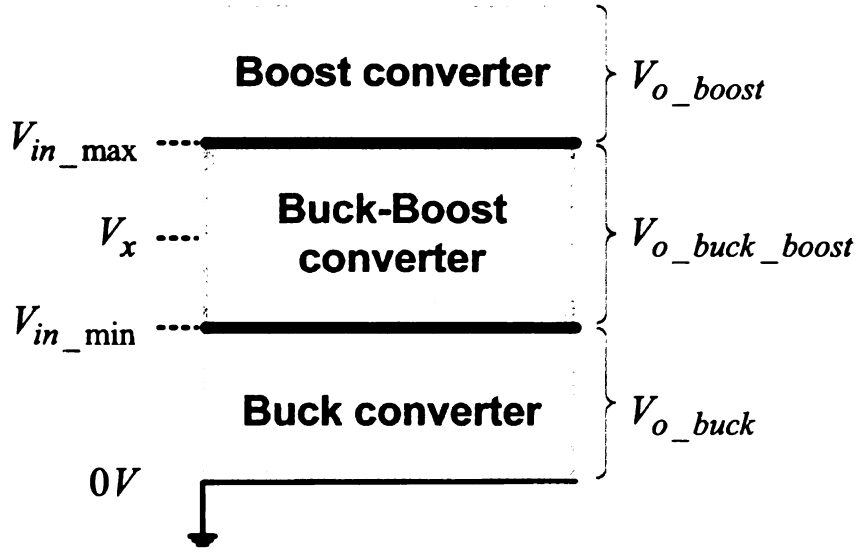


Figure 7-6 Input and output voltage range of buck, boost and buck-boost converter

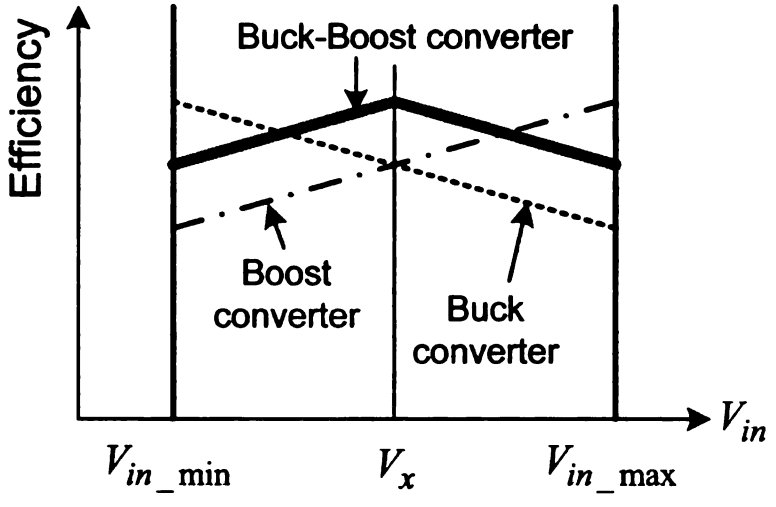


Figure 7-7 Efficiency profile of buck, boost and buck-boost converter

Figure 7-7 shows an efficiency map of the buck, boost and buck-boost converter as converter input voltage varies within its minimum and maximum value.

Generally speaking, efficiency of the power electronics converter becomes maximum when the input and output voltage difference is minimum. For example, efficiency of the buck converter shown in Figure 7-4 reaches maximum value when the input voltage is equal to output voltage, i.e., when duty cycle is one. This means that the switch (S) is always turned on to transfer energy to the load. With this condition, there is minimum power loss in the switching device and freewheeling diode (D), and minimum core and winding loss in the inductor. Therefore, the efficiency would be maximum at this condition.

As input voltage increases, D decreases to regulate the same output voltage. In this case, power loss in the switch and diode increases because its RMS current increases. In addition to that, core and winding loss of the inductor increases because the flux swing of the inductor increases. As a consequence, the converter efficiency will decrease. The same explanation can be applied to the boost converter.

Unlike the buck converter or boost converter mentioned above, output voltage of the buck-boost converter is within the input voltage range as shown in Figure 7-6. Therefore, the input and output voltage difference of the buck-boost converter either in buck mode or boost mode becomes narrower than that of the buck converter and boost converter. Therefore, the converter efficiency can be improved for the same reasons mentioned above.

7.3. Literature Survey for Buck-Boost Converters

7.3.1 Non-Isolated Buck-Boost Topologies

The most basic converter in power electronics is the buck converter as show in Figure 7-4. It is so named because it always steps down, or bucks, the input voltage. The output of the converter is given by

$$V_o = DV_{in} \tag{7.1}$$

Interchange input and output of the buck converter, we have the second basic converter – the boost. The boost always steps up, hence its name. The output voltage is always higher than the input voltage, and is given by

$$V_o = \frac{V_{in}}{1-D} \tag{7.2}$$

When we need an application where we need to both step up and step down, depending on the input and output voltage, we could use two cascaded converters – a buck and a boost as shown in Figure 7-8.

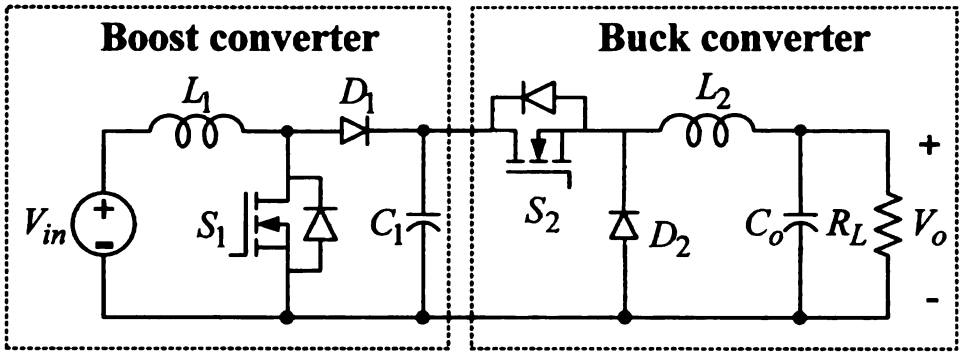


Figure 7-8 Buck and boost two stage converter

Unfortunately, this requires two separate controllers and switches. Moreover, the efficiency of this topology is low because it has two stages of power conversion. The effective power-conversion efficiency is the product of both the buck regulator' s and boost converter' s efficiencies. Typical efficiency numbers for buck-and-boost converters are between 90-95 % each. Therefore, the total converter efficiency would be between 81-90%. The two separate converters increase the number of parts and increase the size of system. An additional drawback is the additional cost associated with two separate converters.

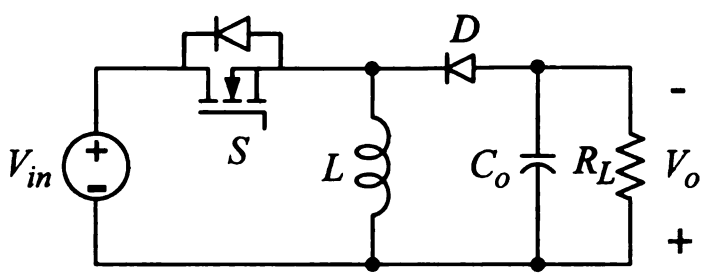


Figure 7-9 Buck-boost converter

The buck-boost converter shown in Figure 7-9 has the desired step up and step down functions and it can be realized with a single power conversion stage. The output voltage is given by

$$V_o = -\frac{D}{1-D} V_{in} \tag{7.3}$$

A distinct drawback of the buck-boost converter is that its output is inverted as illustrated in (7.3). Therefore, switch (S) and diode (D) voltage rating should be high enough to sustain the sum of Vin and Vo. The use of high voltage rating device will

reduce converter efficiency. This is one of the reasons why the buck-boost converter shown in Figure 7-9 cannot achieve high efficiency in practice. Furthermore, the input current is discontinuous because the switch is connected in series with the input voltage source.

In order to overcome the input current discontinuity of the buck-boost converter, the Cuk converter was invented by California Institute Professor Slobodan Cuk in 1976 [52], [53]. This converter performs a dc conversion function similar to the buck-boost converter and it operates via capacitive energy transfer. It can either increase or decrease output voltage. Compared with the buck-boost converter shown in Figure 7-9, input and output current of the Cuk converter is continuous because the two inductors in the input and output surround the switch. However, its output voltage polarity is still inverted like the buck-boost converter shown in Figure 7-9.

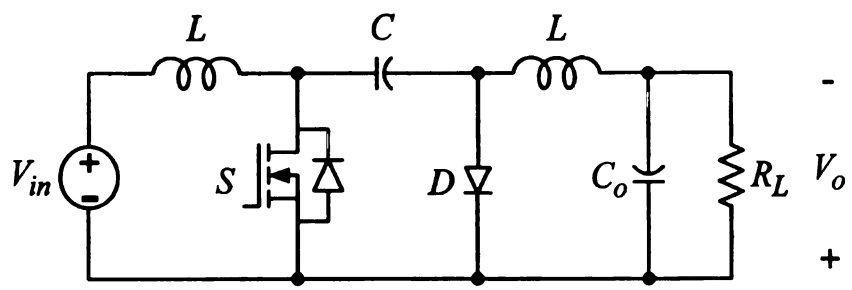


Figure 7-10 Cuk converter

One converter that can provide both step up and step down of the input voltage, while maintaining the same polarity is the SEPIC (single ended primary inductor converter) [15]. Figure 7-11 shows the SEPIC and it shares the same input and output ground reference. Like the Cuk converter, the SEPIC uses two inductors. The SEPIC transposes the position of the inductor and the diode so that the output voltage is positive.

The input current is non-pulsating because the input inductor is connected in series with input voltage. However, the pulsating current has to charge the output capacitor.

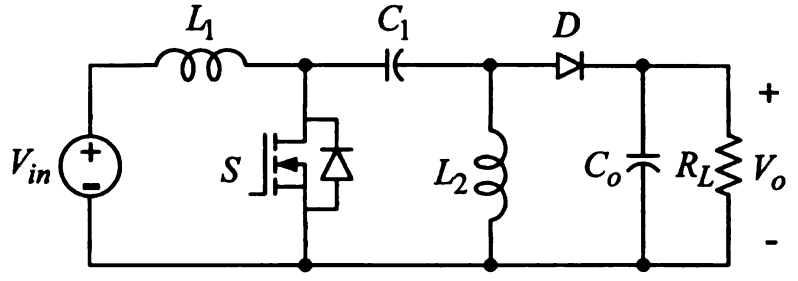


Figure 7-11 SEPIC converter

7.3.2 Transformer Isolated Buck-boost Topologies

The dc-dc converters shown in the previous section are all non-isolated converters. In other words, the input and output of the converter are not electrically isolated. In many practical dc-dc power converters, however, an electrical isolation between the input and output port is frequently required primarily due to safety considerations. The most common and easiest way is to insert an isolation transformer in the middle section of the converter because transformers can transfer electrical power without any electrical connection between primary and secondary. It transfers power through magnetic coupling. Moreover, transformers can convert voltage and current easily by simply changing transformer turns ratio. Thus one can get any desired voltage and current by using a transformer.

The flyback converter depicted in Figure 7-12 is a very typical example of a transformer isolated buck-boost converter. It is evolved from the buck-boost converter shown in Figure 7-9 by adding an isolation transformer and simplifying the resulting circuit. The flyback converter has a very simple structure with a minimal component

count, while providing desired input-to-output isolation. The flyback converter has thus been widely used in cost-sensitive commercial applications, such as consumer electronics and low-power home applications.

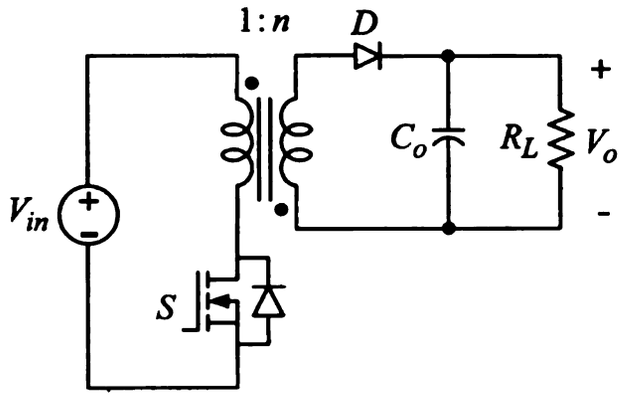


Figure 7-12 Flyback converter

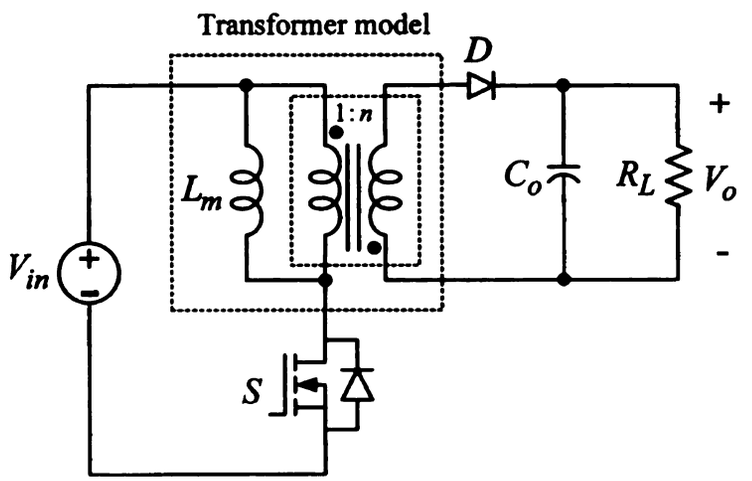


Figure 7-13 Transformer model of flyback converter

The transformer polarity marks are reversed to obtain a positive output voltage. Unlike the ideal transformer, current does not flow simultaneously in both windings of the flyback transformer [15]. Figure 7-13 illustrates the practical configuration of the flyback transformer. Energy from the DC source is stored in magnetizing inductance L_m when switch is on. When diode D conducts, this stored energy is transferred to the load,

with the inductor voltage and current scaled according to the *1:n* turns ratio. Therefore, the voltage conversion ratio of the flyback converter is

$$V_o = n\frac{D}{1-D}V_{in} \tag{7.4}$$

If the transformer turns ratio is 1:1, the voltage gain of flyback converter is equal to that of buck-boost converter.

Figure 7-14 shows the isolated Cuk converter derived from the basic non-isolated Cuk converter shown in Figure 7-10 [15]. The energy transfer capacitor in the nonisolated Cuk converter is split into two series capacitors, C_1 and C_2. A transformer can now be inserted between these capacitors because C_1 and C_2 ensure that no dc voltage is applied to the transformer. The polarity marks in the transformer have been reversed, so that a positive output voltage is obtained. Similar to the flyback converter, the isolated Cuk converter can only be applied to low power systems requiring several hundred watts. This is because the capacitors C_1 and C_2 are used as the main energy transfer element.

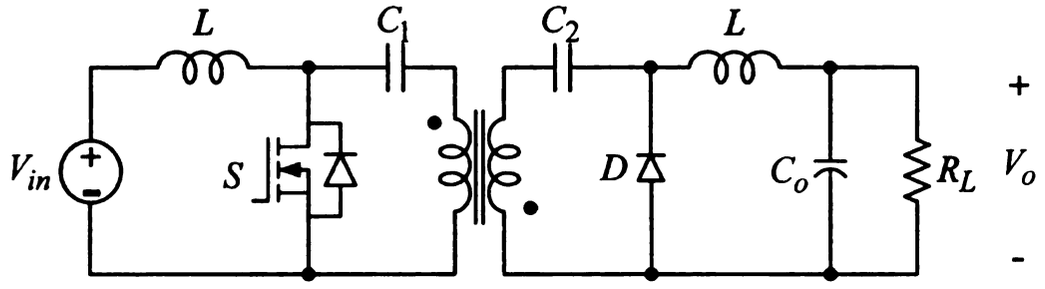


Figure 7-14 Isolated Cuk converter

In order to meet high power demand, buck and boost function and transformer isolation, a back-to-back bi-directional dc-dc converter is introduced in several applications [54, 55].

Figure 7-15 shows one example of such a converter. By replacing rectifier diodes with active switches in the transformer secondary side and adjusting phase angle between transformer primary and secondary, a desired buck-boost operation is achieved in this topology. However, active switches are needed in the transformer secondary side to have buck-boost function. Therefore, it will increase system complexity and cost of the converter.

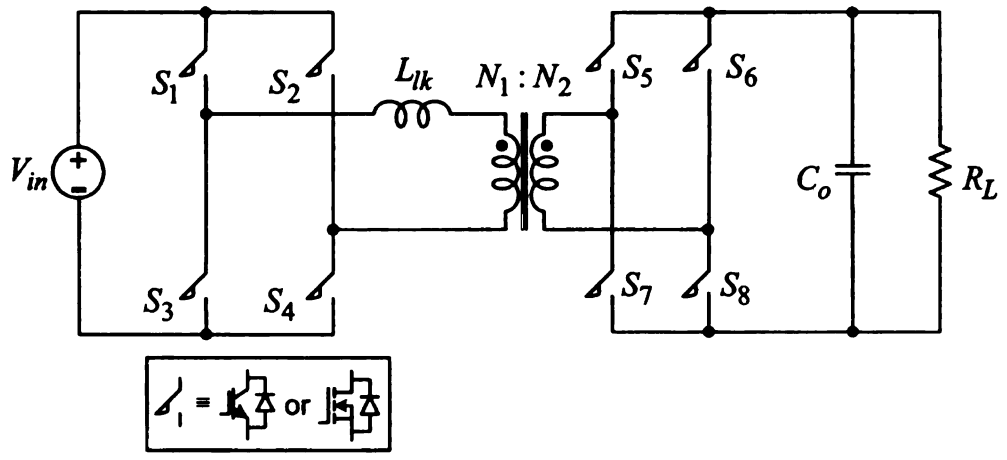


Figure 7-15 Back-to-back bi-directional converter.

Another circuit topology that can achieve buck and boost function is LLC series resonant converter (LLC SRC) shown in Figure 7-16 [56, 57]. This circuit uses transformer magnetizing inductance to have both boost and soft-switching function of converter. The voltage gain of LLC SRC is shown in Figure 7-17. This circuit is mainly used for front-end dc-dc converter for distributed power system and showed good performances such as high density, high efficiency especially at light load condition.

However, the attainable voltage gain of the LLC SRC decreases as Q factor (or load) increases as shown in Figure 7-17. The reason for this is that the LLC SRC is basically a variation of the traditional SRC, but it uses low transformer magnetizing inductance. When the load becomes heavy, the effect of magnetizing inductance becomes less and this circuit eventually takes properties of the SRC.

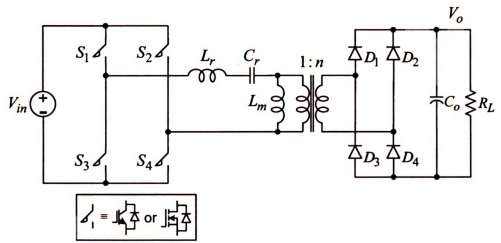


Figure 7-16 LLC series resonant dc-dc converter

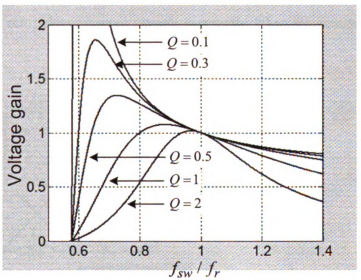


Figure 7-17 Voltage gain of LLC series resonant converter

This problem can be solved by either reducing magnetizing inductance of the transformer or reducing characteristic impedance of the resonant network. In this case, however, current flowing through the magnetizing inductance becomes big. This will increase switch turn-off current and results in efficiency drop. Thus, the LLC SRC is not applicable to the system that requires wide input voltage and load variation.

Figure 7-18 shows a transformer isolated Z-source dc-dc converter. The Z-source concept which was originally developed as a Z-source inverter by Dr. Peng can also be applied to a Z-source dc-dc converter [1], [58, 59]. The great and unique feature of the Z-source converter/inverter is that it can be short and open circuited without damaging switching devices. Therefore, the converter reliability can be greatly improved. However, the main drawback of the Z-source converter (or inverter) is that the input (source) current is discontinuous because the input source of the converter is connected in series with a diode which is periodically on and off by switching action of switching devices. Therefore, an input LC filter or C filter should be included between the DC source and diode to smooth out pulsating input current especially when the source is a fuel cell or battery.

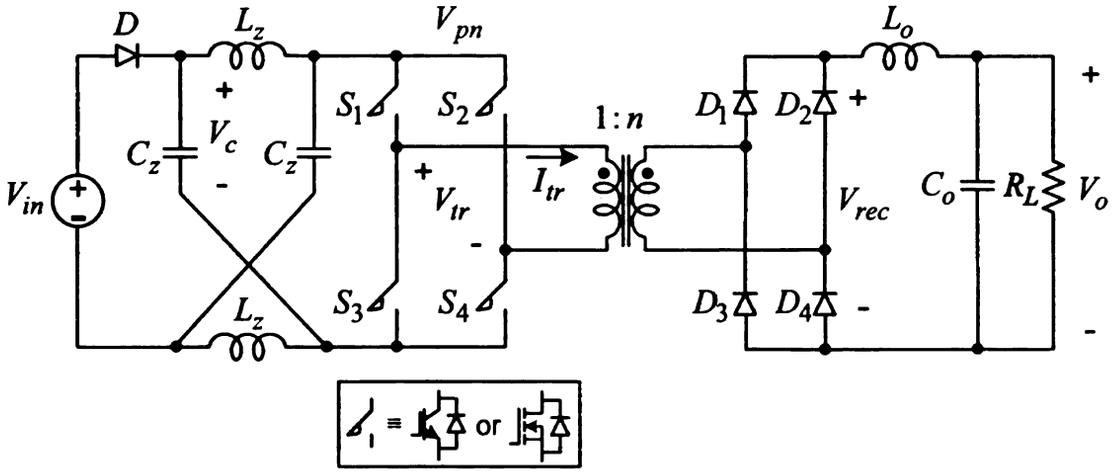


Figure 7-18 Z-source dc-dc converter

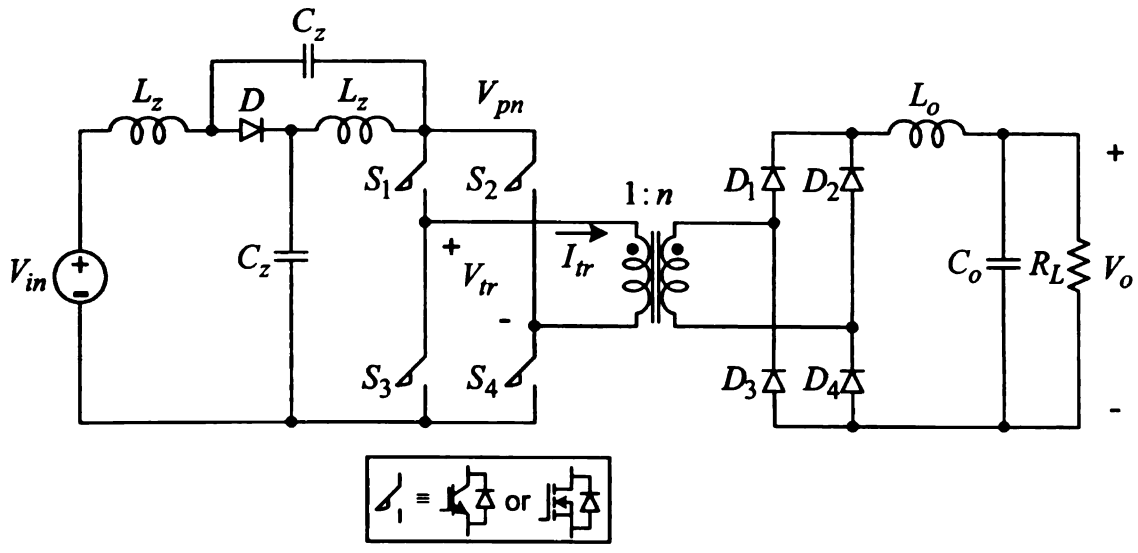


Figure 7-19 qZ-Source dc-dc converter.

In order to overcome the aforementioned drawback of the Z-source converter (or inverter), a quasi Z-source inverter was proposed recently [60-62]. The qZ-source inverter can also be applied to qZ-source dc-dc converter as shown in Figure 7-19. In this scheme, one of the Z-source inductors in Figure 7-18 is placed in series with DC the source without sacrificing the circuit operation. Thus, the converter input current can be continuous in this structure, which is a great advantage over the original circuit shown in Figure 7-18.

Figure 7-20 shows the Z(or qZ)-source dc-dc converter operating at buck mode. In this mode, there is open-circuit interval in gate signal to step down output voltage. The input and output voltage relationship is exactly same as the conventional buck type converter and is expressed as

$$\frac{V_o}{V_{in}} = nD \tag{7.5}$$

Figure 7-21 shows the Z(or qZ)-source dc-dc converter operating at boost mode. In this mode, there is short-circuit interval in gate signal to step up output voltage. The input and Z-source capacitor voltage (V_{cz}) relationship is

$$\frac{V_{cz}}{V_{in}} = \frac{1-D_s}{1-2D_s} \tag{7.6}$$

, where D_s Figure 7-20 is shoot-through duty cycle and is equal to $(1-D)$. Similarly, input and V_{pn} voltage relationship is

$$\frac{V_{pn}}{V_{in}} = \frac{1}{1-2D_s} \tag{7.7}$$

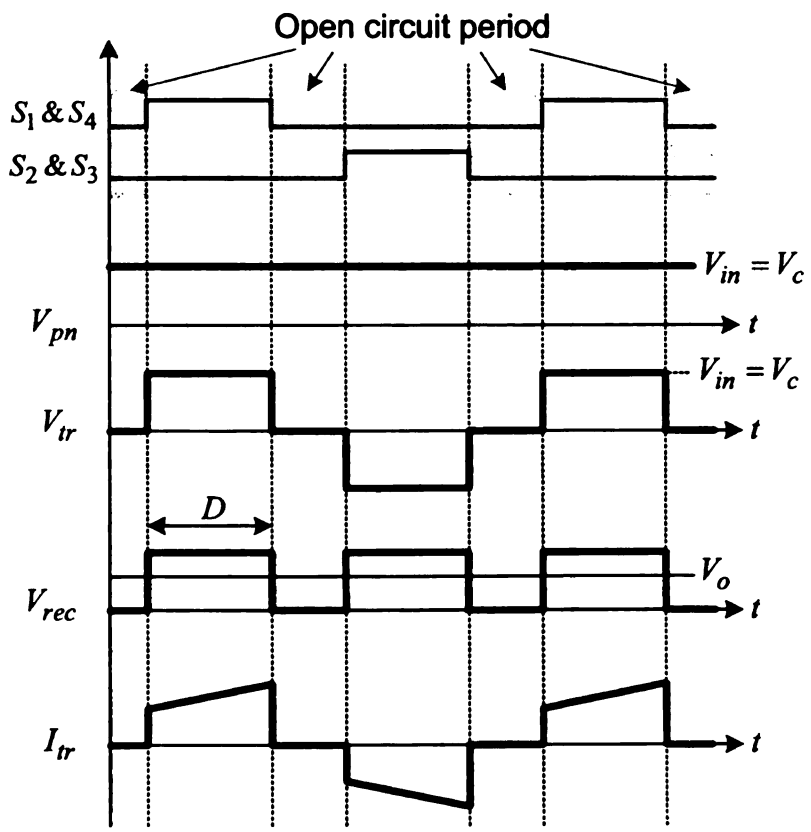


Figure 7-20 Key waveforms in buck mode

In boost mode, the output voltage is equal to V_{cz}. Therefore, input and output voltage relationship is

$$\frac{V_o}{V_{in}} = \frac{1-D_s}{1-2D_s} = \frac{D}{2D-1} \tag{7.8}$$

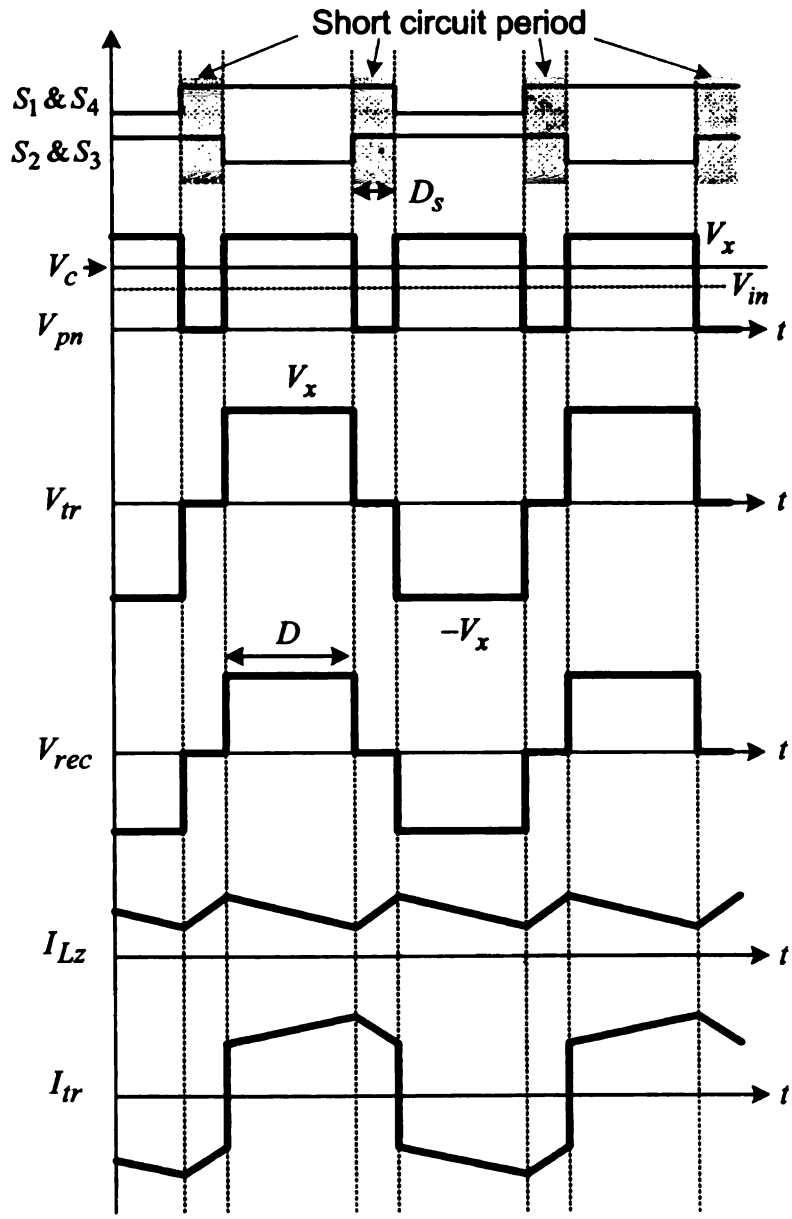


Figure 7-21 Key waveforms in boost mode

From (7.5) and (7.8), the overall voltage gain of Z-source dc-dc converter can be drawn and is shown in Figure 7-22.

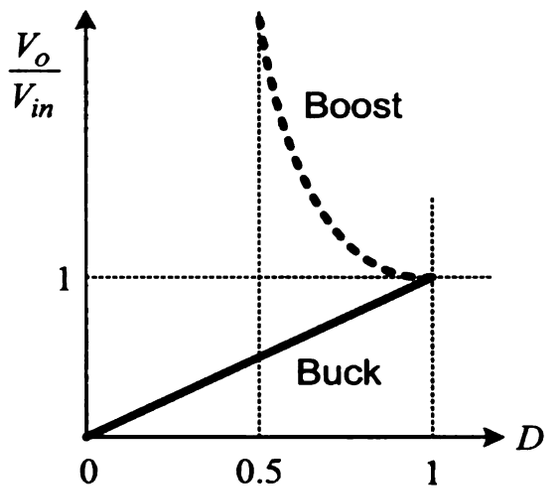


Figure 7-22 Voltage gain of Z(qZ)-Source dc-dc converter.

The Z-source (or qZ-source) converter mentioned above, however, has a bulky inductor in the output to make a fairly constant DC output. In this case, there exists high voltage oscillation across the diode rectifier due to resonance between the transformer leakage inductance and junction capacitance of the rectifier diodes. This voltage oscillation problem is already discussed in great detail in Chapter 4. In addition to that, the diode in the Z-source network makes additional power loss.

In order to solve these problems, a novel dc-dc converter using a distributed Z-source network is proposed in this chapter and is shown in the next section.

7.4. The Z-Source Concept and Distributed Z-Source Network

The Z-source power converter provides a new converter topology and theory with the intention to overcome the problems of the traditional V-source and I-source

converters [1]. The Z-source converter comprises an impedance network to couple the main converter circuit to the power source or load, which is different from the V-source and I-source converters and has none of the previously mentioned problems.

Figure 7-23 shows a general topological arrangement of the Z-source concept [46]. A two-port network that consists of inductors *L1* and *L2* and capacitors *C1* and *C2* connected across both sides is employed to provide an impedance source (Z-source) coupling the converter (or inverter) to the dc source or load.

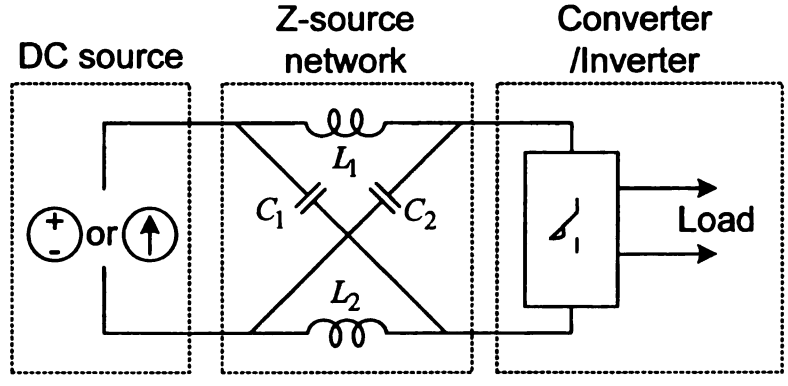


Figure 7-23 A general topology of the Z-source converter.

The great and unique feature about the Z-source network is that unlike the traditional V-source or I-source, it can be open and short-circuited, which provides a mechanism for the main converter circuit to step-up or step-down voltage as desired. The Z-source network provides great flexibility for the source, main circuit, and load. The Z-source network shown in Figure 7-23 can be short- and open-circuited on either side. Therefore, the Z-source concept can be generalized as to provide a two-port network (or circuit) that can be short- and open-circuited at any time according to operation needs. These two-port circuits include a transmission line and a capacitor-inductor hybrid that have been investigated by many contributors for other purposes [63-68].

7.5. Transmission Line Based Z-Source Network-Distributed Z-Source Network

A transmission line network is a two-port network and naturally satisfies the Z-source concept's requirements: that is, the network can be open- and short-circuited by switching devices [46]. Because the capacitance and inductance are distributed along the network, this type of networks is called "distributed Z-source network". Efforts have been made to utilize the parasitics and transmission line networks in power electronics circuits [64, 65].

Figure 7-24 illustrates a general topology of the transmission line based power conversion or distributed Z-source network (DSZN) power converter. The proposed DZSN intentionally utilizes the parasitics and distributed inductance and capacitance for power conversion and at the same time for EMI attenuation.

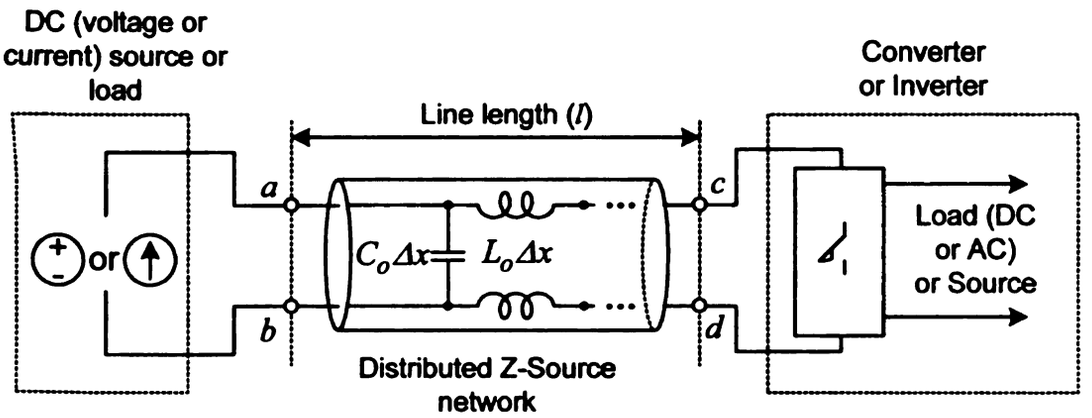


Figure 7-24 A general topology of the distributed Z-source converter [46].

Recently, an interesting Z-source network which has similar functions as the conventional Z-source network shown in Figure 7-23, but a little different in structure, is introduced and its basic conceptual structure is shown in Figure 7-25 [46], [69].

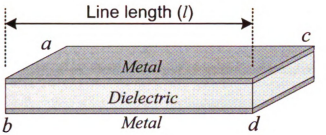


Figure 7-25 A basic structure of DZSN or transmission line network.

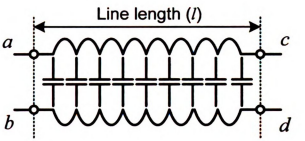


Figure 7-26 Electrical representation of DZSN.

The structure is a typical parallel plate two-port network (or transmission line network) with line length l. It consists of two conductors with dielectric insulation in the space between the conductors. The top and bottom conductors sandwich dielectric material to form capacitance. At the same time, the two current carrying conductors are insulated by magnetic core to form inductance. Figure 7-26 shows the electrical representation of the two-port network shown in Figure 7-25.

In order to implement the proposed network, the DZSN can be implemented in either common-mode or differential-mode connected structures. Figure 7-27 and Figure 7-28 show a common-mode connected and differential-mode connected DZSN, respectively. The L and C represent the total inductance and capacitance of the line. M is the mutual inductance of the coupled inductor. The $L\Delta x$ and $C\Delta x$ is the inductance and capacitance

in each cell, where Δx is the line length of each cell. In Figure 7-27 and Figure 7-28, the winding resistance and conductance of the network are neglected for the sake of circuit simplicity.

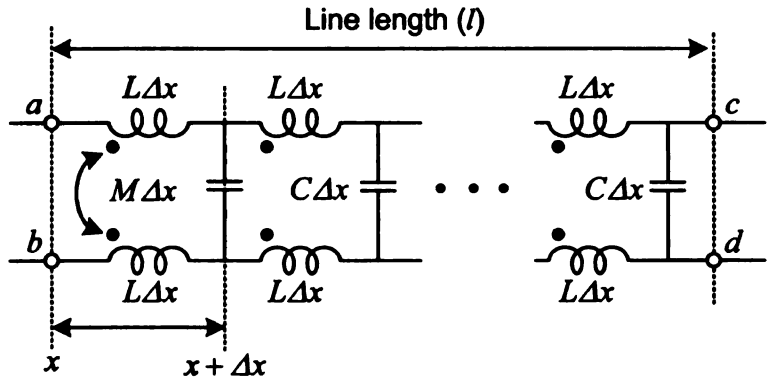


Figure 7-27 Common-mode connected DZSN.

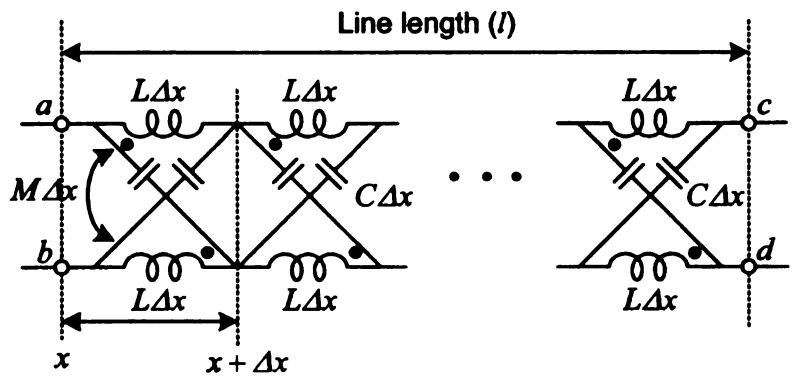


Figure 7-28 Differential-mode connected DZSN.

Although, the two common-mode and differential-mode DZSN have slightly different structures, they both have very similar electrical properties to that of a transmission line network. This is well explained in [70].

The two inductors in each cell can be either tightly or loosely coupled and can be built in one core. For example, the inductors in common-mode connected DZSN should

be loosely or non-coupled inductors. Otherwise, there is a flux cancellation between top and bottom conductors, which results in very small (leakage) inductance in each cell. On the other hand, the inductors in differential-mode connected DZSN should be tightly or non-coupled inductors to have a high or moderate inductance value. In this dissertation, common-mode connected DZSN is selected because it is relatively easy to build.

Figure 7-29 and Figure 7-30 show a photo of the prototype DZSN developed in this work. Two small toroidal powder cores are inserted in each conductor to make inductance and to avoid magnetic coupling between them and a small value of capacitor is connected across the top and bottom conductors. Thus, the two inductors and one capacitor form a single cell and many of these cells are connected in series in a similar fashion as shown in Figure 7-25 to form (or mimic) the characteristics of a transmission line network. The inductance and capacitance values used in each cell are $2\times 66\ nH$ and $3.3\ nF$, respectively. 80 cells are connected in series to set the operating frequency of the converter in a reasonable range.

Figure 7-31 shows the overall circuit configuration of the proposed dc-dc converter using DZSN. In order to achieve the buck and boost function of the proposed dc-dc converter, the DZSN is coupled between power source and main switching devices. The great and unique feature about the DZSN is that it can be open- and short-circuited by switching devices like the conventional Z-source converter shown in Figure 7-23. As a result, the proposed DZSN dc-dc converter has buck and boost functions, which cannot be obtained with the traditional transformer isolated FB dc-dc converters shown in Figure 7-1 and Figure 7-2.

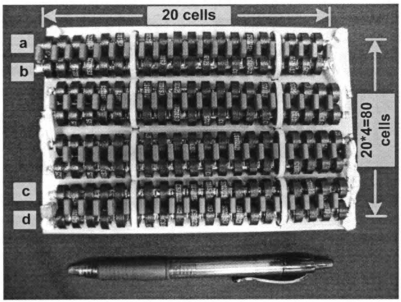


Figure 7-29 Photos of DZSN implemented (Top view)

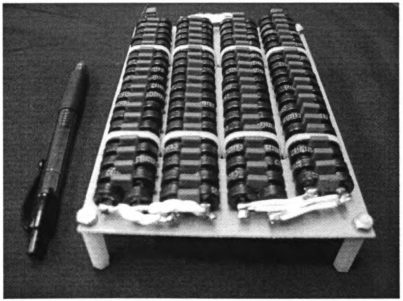


Figure 7-30 Photos of DZSN implemented (front view)

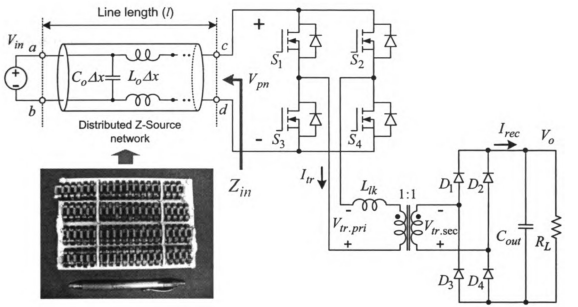


Figure 7-31 Proposed DZSN dc-dc converter.

Compared with the Z-source (or qZ-source) dc-dc converters mentioned before, the proposed DZSN dc-dc converter does not suffer from the rectifier diode oscillation problem because an output filter capacitor is connected to the rectifier diode directly. No diode is needed in the Z-source network while maintaining the same buck-boost function as the Z-source dc-dc converter.

7.6. Conclusion

In this chapter, a conventional non-isolated and transformer isolated buck-boost dc-dc converters are reviewed. Limitations of the conventional buck-boost dc-dc converters are addressed. A distributed Z-source network composed of an array of inductors and capacitors is introduced and its properties and characteristics are examined in detail. The

proposed DZSN can be used as a dc-dc converter that can overcome the theoretical barriers of the conventional dc-dc converters.

Chapter 8. Principle Operation of Distributed Z-Source Network DC-DC Converter

8.1. Input Impedance of Distributed Z-Source Network

The input impedance (Z_{in}) of DZSN plays an important role in the operation of the proposed DZSN dc-dc converter. The unit of measurement is the ohm, but we cannot simply attach an ohm-meter to the network to measure its impedance. Figure 8-1 shows the measurement setup for the input impedance Z_{in} of DZSN. In order to measure Z_{in} of the network, the line is terminated with a load (Z_L) and Z_{in} is measured on the other end.

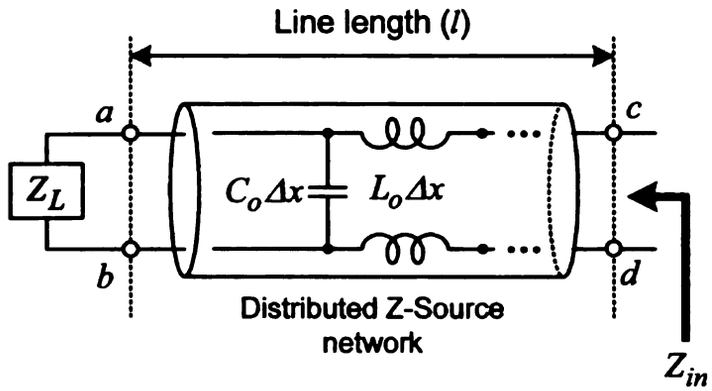


Figure 8-1 Input impedance measurement.

As already well known, the Z_{in} of a lossless transmission line terminated with a load is defined as follows [67, 68], [71]

$$Z_{in} = Z_c \frac{\frac{Z_L}{Z_c} + \tanh(\gamma l)}{\frac{Z_L}{Z_c}\tanh(\gamma l) + 1} \tag{8.1}$$

In (8.1), Z_L is the load resistance connected to one end of the two-port network. Z_c is the characteristic impedance and γ is the propagation constant of the network and they are defined as

$$Z_c = \sqrt{\frac{2(L' - M')}{C'}} \tag{8.2}$$

$$\gamma = jw\sqrt{2(L' - M')C'} \tag{8.3}$$

,where L', C' and M' are the per-unit length self inductance, capacitance and mutual inductance of the line, respectively.

The Z_c of a line is not dependent on its length but on the physical arrangement of the size and spacing of the conductors. From (8.1), Z_{in} of the lossless transmission line is a transcendental function with an infinite number of j-axis poles and zeros [64, 65].

In this dissertation, Z_{in} is measured with a short-circuited load ($Z_L = 0$) because the one (left) port of DZSN of proposed dc-dc converter is connected to DC voltage source and we measure Z_{in} from the other side (right) of network (see Figure 7-31).

When the line is terminated in a short circuit, then $Z_{in} = Z_c \tanh(\gamma l)$. The zeroes of Z_{in} lie at $s = jw_v$, where

$$w_v = \frac{v\pi}{2l\sqrt{2(L' - M')C'}} \quad for\ v = 0, 2, 4, \ldots \tag{8.4}$$

Likewise, the poles of Z_{in} are located at odd multiples ($v = 1,3,5,....$) of the principal quarter-wave resonance, w_1. In order to understand the characteristics of the DZSN, and to calculate the pole and zero frequencies of the network, the following definitions are necessary.

First, the wave velocity on the line is defined as

$$v = \frac{1}{\sqrt{2(L' - M')C'}} \tag{8.5}$$

Secondly, the travel time, T_d, (or transmission delay) of the electric signal on the line is defined as

$$T_d = \frac{l}{v} \tag{8.6}$$

Thirdly, the wavelength λ of electric signal is

$$\lambda = \frac{v}{f} \tag{8.7}$$

,where f is applied frequency to line. From (8.5)-(8.7), the principal quarter-wavelength ($l = \frac{\lambda}{4}$) resonant frequency, f_1 can be calculated as

$$f_1 = \frac{1}{4T_d} = \frac{1}{4l\sqrt{2(L' - M')C'}} \tag{8.8}$$

From definitions, $L' = \frac{L}{l}, C' = \frac{C}{l}, M' = \frac{M}{l}$, where L, C and M are the total inductance, capacitance, and mutual inductance of the network, respectively. Therefore, (8.8) can be expressed as

$$f_1 = \frac{1}{4T_d} = \frac{1}{4l\sqrt{2(L'-M')C'}} = \frac{1}{4\sqrt{2(L-M)C}} \tag{8.9}$$

Eq. (8.9) can also be expressed using a number of cells as follows.

$$f_1 = \frac{1}{4\sqrt{2(L_{cell}-M_{cell})C_{cell}}} \times \frac{1}{n} \tag{8.10}$$

,where $L = nL_{cell}, C = nC_{cell}, M = nM_{cell}$, n is the number of cells and $L_{cell}, C_{cell}, and\ M_{cell}$ are the inductance, capacitance, and mutual inductance of each cell of the n cell network, respectively.

Table 8-1 summarizes the electrical specifications of the prototype DZSN shown in Figure 7-29. From the information in Table 8-1 and Eq. (8.10), the principal quarter-wavelength resonant frequency f_1 was 150 kHz. Figure 8-2 shows the simulated magnitude response of Z_{in} of DZSN. As expected, the f_1 is placed at 150 kHz and all the other poles and zeroes are located at the integer multiple of f_1. Since the network is assumed as lossless transmission line, there is no high frequency attenuation in magnitude.

Table 8-1 Electrical specifications of DZSN.

Distributed Z-source network	Magentic core: Changsung Sendust core • Part number: CS102125 • permeability (μ)=125 • A_L value=66 nH/N^2 Capacitor: WIMA
Electrical values	$n=80, L_{cell}=66nH, C_{cell}=3.3nF, M_{cell}=0$
Characteristics impedance of network	$Z_o=\sqrt{\frac{2(L-M)}{C}}=\sqrt{\frac{2\times 66nH}{3.3nF}}=6.32\Omega$
Principal quarter wave resonance frequency	$f_1=\frac{1}{4\sqrt{2(L_{cell}-M_{cell})C_{cell}}}\times\frac{1}{n}$ $=\frac{1}{4\sqrt{2\times 66nH\times 3.3nF}}\times\frac{1}{80}\approx 150kHz$

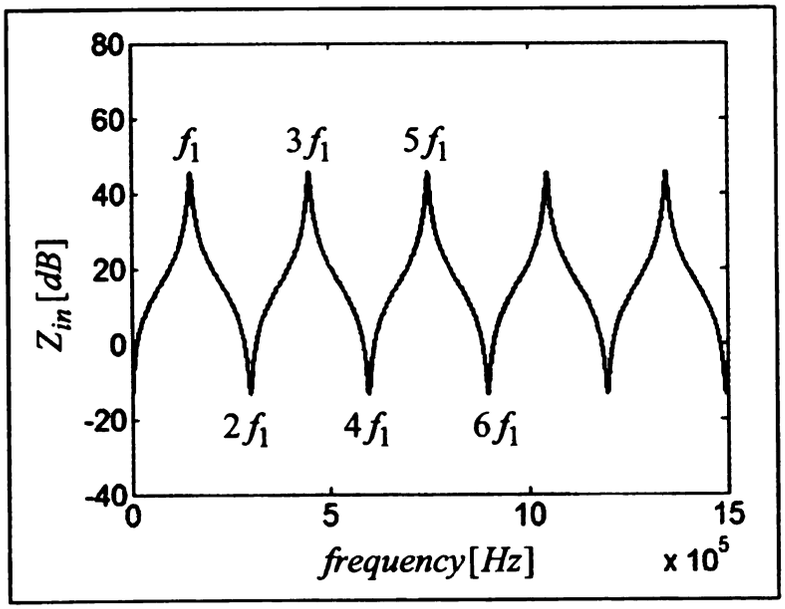


Figure 8-2 Simulation results of Z_{in} with $Z_L=0$.

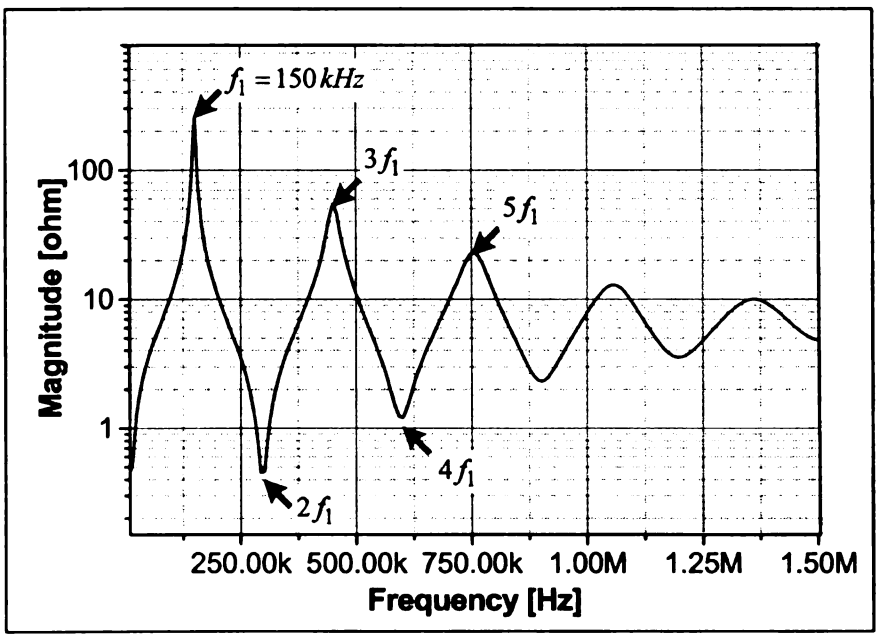


Figure 8-3 Z_{in} measurement of DZSN with $Z_L = 0$ (Magnitude)

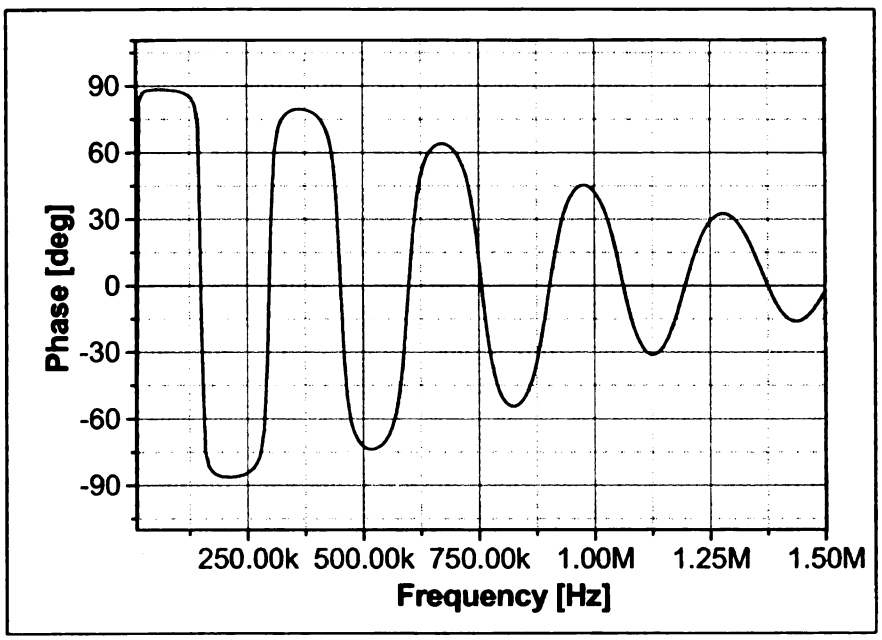


Figure 8-4 Z_{in} measurement of DZSN with $Z_L = 0$ (Phase)

Figure 8-3 and Figure 8-4 show the measured magnitude and phase response of Z_{in} of the prototype DZSN shown in Figure 7-29 when Z_L is zero (shot-circuited). An HP 4194 impedance analyzer is used to measure Z_{in}. The f_1 was very close to 150 kHz. However, there is quite considerable attenuation in magnitude and phase as frequency increases. This is because the AC winding resistance, caused by skin and proximity effect, becomes dominant at high frequency.

8.2. Voltage and Current distribution along DZSN

From the impedance measurement of Figure 8-3, the Z_{in} of DZSN varies as the excitation frequency f_{ex} changes. Therefore, the voltage and current distribution along DZSN change, too. f_{ex} is twice the switching frequency (f_{sw}) of the dc-dc converter because of the full-bridge circuit configuration.

Figure 8-5 and Figure 8-6 show the DZSN terminated with a DC voltage source at left end and the input impedance is seen at the right end where switching devices are present. The rest of the FB circuit is omitted for the sake of simplicity. Figure 8-5 shows the voltage and current distribution when f_{ex} is set to f_1, the principal quarter wave resonance frequency. In this condition, the line length of the network is one quarter wave-length and the input impedance of the network is very high-approaching infinity. This result can also be expected from the impedance measurement shown in Figure 8-3. On the other hand, impedance at the DC source (short-circuit) is zero.

Figure 8-6 shows the voltage and current distribution when f_{ex} is set to $2f_1$, the half wave resonance frequency. In this condition, line length of the network is equal to one

half wave length and input impedance of the network becomes minimum or equal to impedance at the DC source. This result can also be expected from the impedance measurement shown in Figure 8-3.

Voltage V_{pn} measured at the switching side is equal to input voltage V_{in} at this condition, which is a unique and interesting phenomenon of DZSN. In other words, V_{pn} is forced to be equal to V_{in} due to the waveform shaping function of DZSN. However, impedance at the middle of the line length is high.

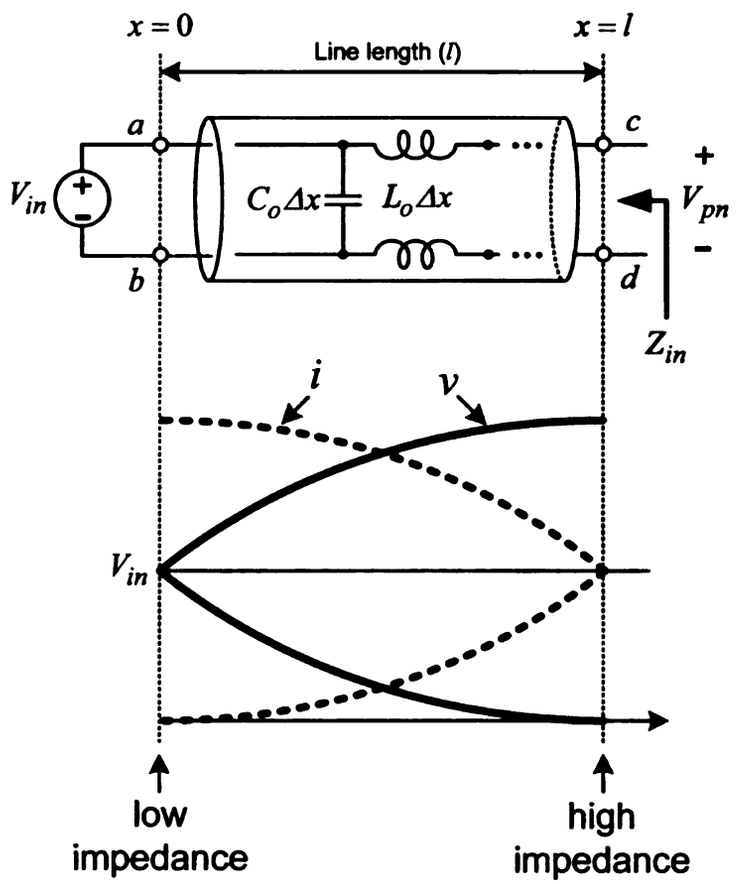


Figure 8-5 Voltage and current distribution along DZSN when $f_{ex} = f_1$, Quarter wave-length condition ($l = \frac{\lambda}{4}$)

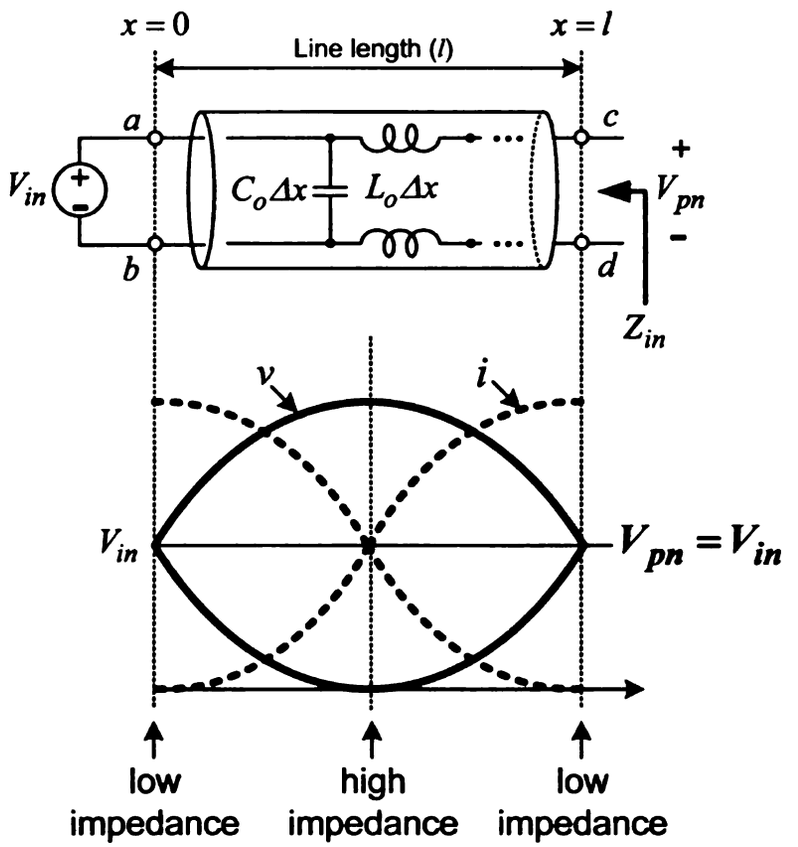


Figure 8-6 Voltage and current distribution along DZSN when $f_{ex} = 2f_1$. Half wave-length condition ($l = \frac{\lambda}{2}$)

8.3. Output Voltage Control of the Proposed DZSN DC-DC Converter

The overall circuit configuration of the proposed DZSN dc-dc converter is shown again in Figure 8-7 for mode analysis. The transformer turns ratio is set to 1:1 for the sake of simplicity. The necessary voltage and current are labeled in this figure.

The proposed dc-dc converter shown in Figure 8-7 can be short- and open-circuited without damaging switching devices because DZSN is coupled between DC source and switching devices. In this section, detailed operating modes will be explained to illustrate

the buck and boost function of the proposed dc-dc converter. Voltage gain of the proposed DZSN dc-dc converter in both buck and boost mode will be derived.

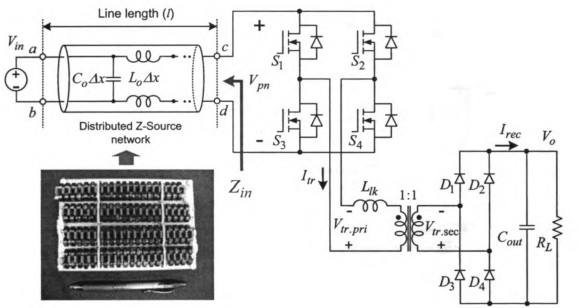


Figure 8-7 DZSN dc-dc converter.

8.3.1 Buck mode (Vin>Vo)

Figure 8-8 shows the operation point at buck mode. From the result of Figure 8-6, V_{pn} is clamped to V_{in} when $f_{ex} = 2f_1$ or $f_{sw} = f_1$ (point "A"). f_{sw} is the switching frequency of the converter. Thus, the proposed dc-dc converter at this half wave length condition becomes similar to the conventional V-source type PWM dc-dc converter shown in Figure 7-1 because V_{pn} is equal to V_{in}. However, the proposed converter cannot have an output filter inductor to control V_o. Otherwise, V_o cannot be boosted in boost mode operation.

In this dissertation, transformer leakage inductance L_{lk} is used to control V_o, instead. Therefore, a conventional duty cycle control method with fixed switching frequency can be used to control V_o.

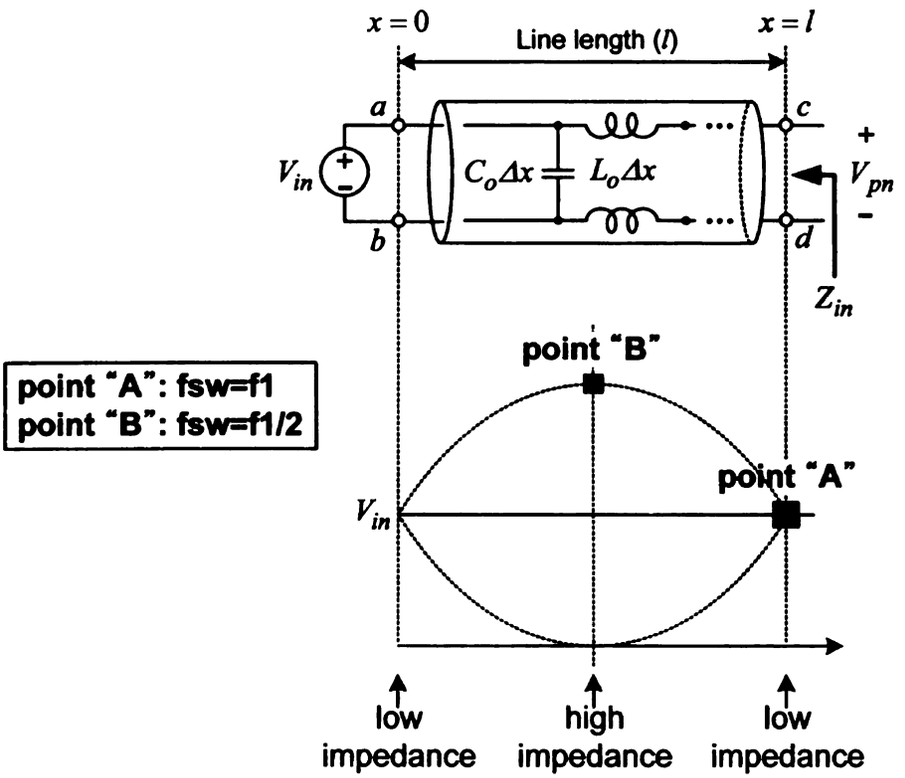


Figure 8-8 Operation point at buck mode (point "A")

Figure 8-9 depicts the key waveforms in buck mode. The proposed dc-dc converter at this mode operates with duty cycle control by modulating open circuit duty cycle as the conventional V-source FB PWM converter. However, the conventional V-source converter suffers from the shoot-through problem caused by EMI misgating-on and can destroy switching devices because the input DC link capacitor is directly discharged through the switching devices.

On the other hand, the proposed converter can be short-circuited without damaging switching devices because all the capacitors in the network can only be discharged

through the inductors that are distributed along the network and the capacitance of each cell is very small. Therefore, current flowing in the switching device is limited by distributed inductors.

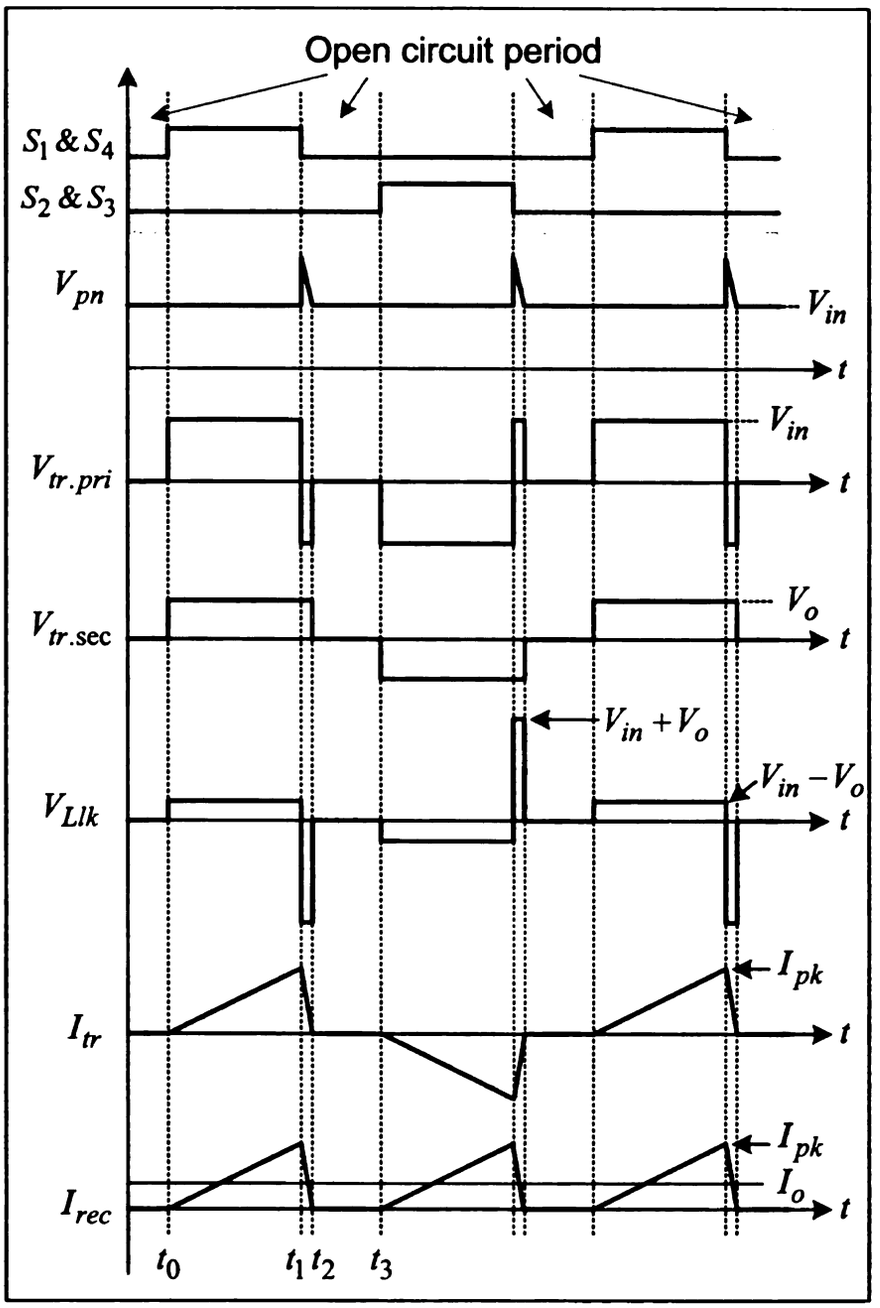


Figure 8-9 Key waveforms of the proposed dc-dc converter at buck mode

The operational modes of the proposed converter in buck mode are explained as follows.

- *Mode 1* ($\sim t_o$): All switches and rectifier diodes are turned off and V_{pn} is equal to V_{in}. Transformer voltage and currents are zero.

- *Mode 2* ($t_o - t_1$): S_1 and S_4 turn on and D_2 and D_3 start conducting. Therefore, V_{in} is applied to the transformer primary winding. Transformer current starts increasing with the slope of $\frac{V_{in} - V_o}{L_{lk}}$ until t_1. The peak transformer current is calculated as

$$I_{pk} = i(t_1) = \frac{V_{in} - V_o}{L_{lk}} T_{on} \tag{7.11}$$

,where T_{on} is switch turn-on time.

- *Mode 3* ($t_1 - t_2$): S_1 and S_4 are turned off and the transformer current flows through the anti-parallel diodes of S_2 and S_3. Therefore, $-V_{in}$ is applied to the transformer primary winding. The transformer current starts decreasing with the slope of $\frac{V_{in} + V_o}{L_{lk}}$ until it reaches zero at t_2. In this mode, D_2 and D_3 are still conducting because the transformer current is positive. Thus, transformer current is regenerated into DZSN. The voltage overshoot in V_{pn} is caused by this regenerated current.

- *Mode 4* ($t_2 - t_3$): The transformer current reaches zero at t_2. D_2 and D_3 are turned off and transformer secondary voltage becomes zero. This is the end of half cycle operation.

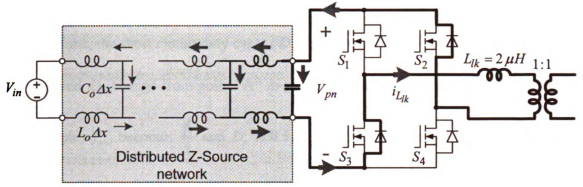


Figure 8-10 Voltage overshoot in Vpn at buck mode

Figure 8-10 explains the mechanism of voltage overshoot in V_{pn} in more detail. The voltage overshoot in V_{pn} when switch off is caused by the regenerative energy stored in L_{lk} that flows back to DZSN through body (anti parallel) diodes of switch. Unlike the conventional V-source type converter which has big DC link capacitance, the capacitance value of each cell of DZSN is very small, 3.3 nF. Therefore, even a small amount of energy that flows back to DZSN is high enough to make a voltage overshoot in V_{pn}.

8.3.2 Boost mode (Vin<Vo)

Figure 8-11 shows the operation point at boost mode. In this mode, a short circuit interval is required to store energy in the DZSN as the conventional I-source PWM converter shown in Figure 7-2.

As already mentioned in buck mode operation, the short circuit at point "A" or short circuit at $f_{sw} = f_1$ will not damage the switching devices, but efficiency of the system at this condition would be low because the input impedance at point "A" is minimum. In

this dissertation, f_{sw} is decreased in order to increase input impedance of the network. At the same time, the short circuit duty cycle (D_s) of the converter is increased to boost V_o. The f_{sw} and D_s change from point "A" to point "B" linearly as shown in Figure 8-11. For example, f_{sw} becomes $\frac{f_1}{2}$ and D_s is 0.5 at point "B", quarter wave length condition.

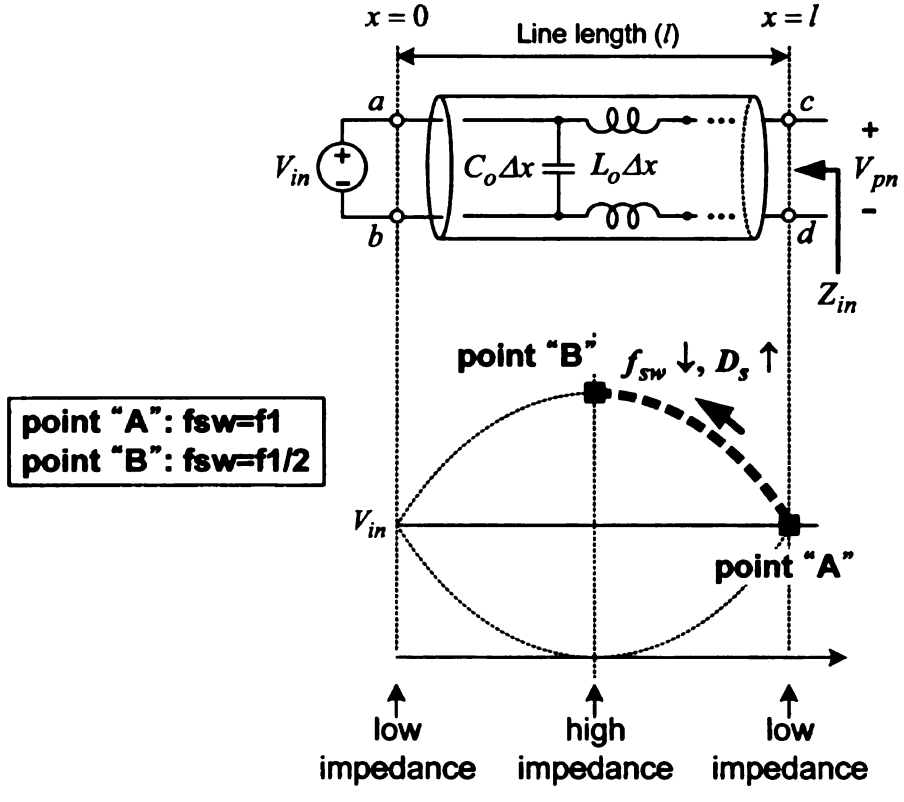


Figure 8-11 Operation point at boost bode (between point "A" and point "B")

The proposed dc-dc converter at this mode operates with duty cycle control by modulating a short circuit duty cycle as the conventional I-source PWM converter. However, the conventional I-source converter suffers from the open-circuit problem caused by EMI misgating-off. Therefore, the switching devices are damaged by overvoltage because the input inductor has no path to discharge its energy and it will finally charge the junction capacitance of the switching devices.

On the other hand, the proposed converter can be open-circuited in this mode without damaging switching devices because the inductors in DZSN are connected between capacitors distributed along the network. Thus, energy stored in the distributed inductors of the network can be transferred to capacitors distributed along the network and the inductance of each cell is very small. Therefore, voltage overshoot in the switching device is limited by distributed capacitors in the network. Figure 8-12 depicts key waveforms at boost mode.

Operational modes of the proposed converter in boost mode are explained as follows.

- *Mode 1* ($\sim t_o$): All switches are on and the rectifier diodes are all off. V_{pn} is equal to zero. Transformer voltage and currents are zero. Input energy is stored in DZSN.

- *Mode 2* ($t_o - t_1$): S_2 and S_3 turn off and D_1 and D_4 start conducting. In this mode, V_{pn} becomes a little greater than V_o because there is a voltage drop across L_{lk}. This voltage is labeled as V_x in Fig. 12.

Therefore, V_x is applied to the transformer primary winding and transformer secondary voltage is equal to V_o. Transformer current starts increasing with the slope of $\frac{V_x - V_o}{L_{lk}}$ until t_1.

- *Mode 3* ($t_1 - t_2$): S_2 and S_3 turn on again and V_{pn} becomes zero. The transformer current starts decreasing with the slope of $\frac{V_o}{L_{lk}}$ until it reaches zero at t_2. Transformer secondary voltage is maintained to V_o because D_1 and D_4 are still conducting.

- *Mode 4* ($t_2 - t_3$): The transformer current becomes zero at t_2. D_1 and D_4 are turned off. This is the end of half cycle operation.

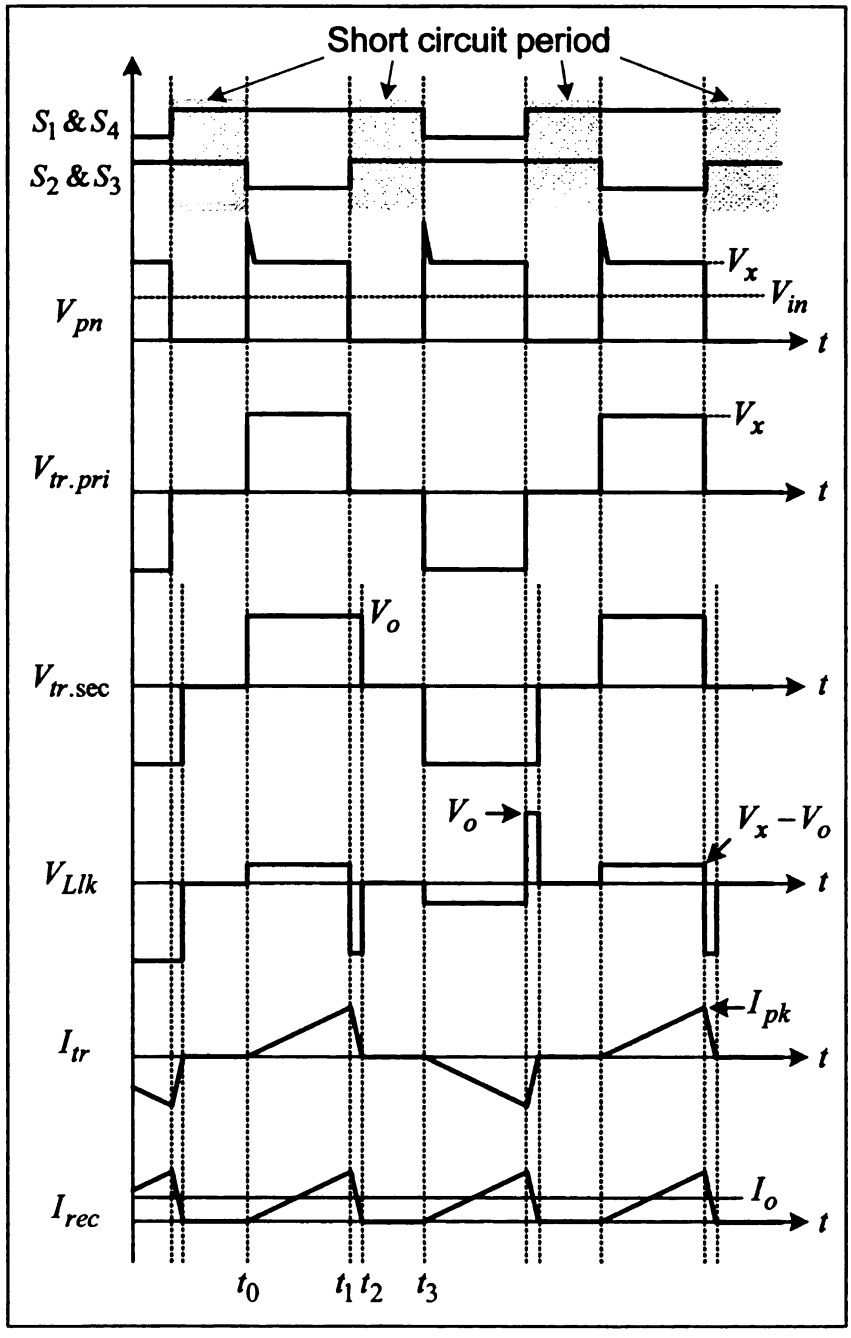


Figure 8-12 Key waveforms of the proposed dc-dc converter at boost mode

8.4. Derivation of Voltage Gain

8.4.1 Buck mode

In order to derive voltage gain at buck mode, the transformer leakage inductance voltage (V_{Llk}) and the rectified transformer current (I_{rec}) waveforms in Figure 8-9 are shown again in Figure 8-13.

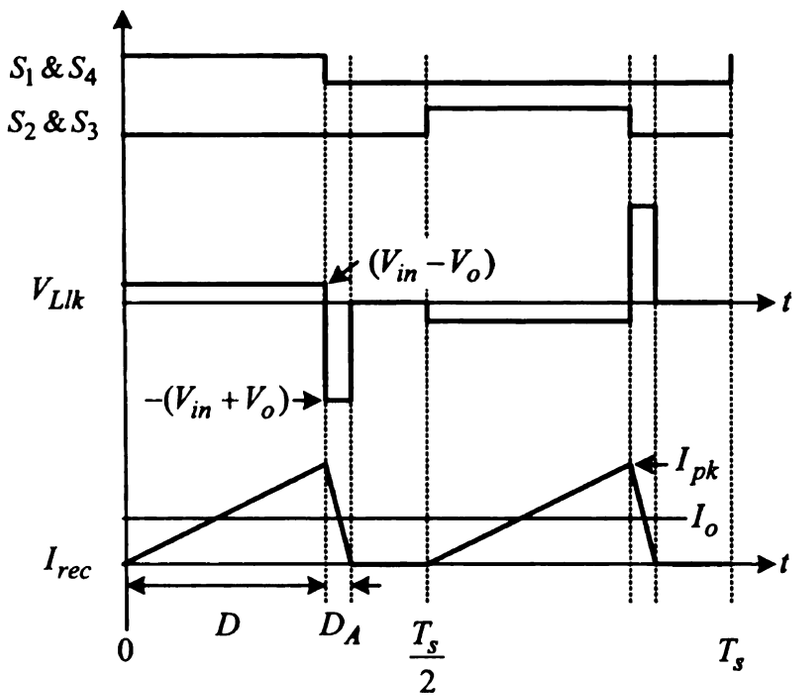


Figure 8-13 Waveforms at buck mode

Defining duty cycle D as the time interval when the switches are closed over the half switching period ($T_s/2$) and D_A as the time interval when transformer current returns to zero from its peak value (I_{pk}), average voltage across the transformer leakage inductance (L_{lk}) during this half switching cycle must be zero due to flux balance condition on L_{lk}. The results is expressed as

$$D(V_{in} - V_o) = D_A(V_{in} + V_o) \tag{8.12}$$

$$\frac{V_o}{V_{in}} = \frac{D - D_A}{D + D_A} \tag{8.13}$$

Similarly, the average value of rectified transformer current (I_{rec}) is output current and it is represented as

$$\frac{1}{2}(D + D_A)I_{pk} = \frac{V_o}{R_L} \tag{8.14}$$

,where I_{pk} is defined as

$$I_{pk} = \left(\frac{V_{in} - V_o}{L_{lk}}\right)D\frac{T_s}{2} \tag{8.15}$$

From (8.14) and (8.15), D_A can be found as

$$D_A = \left(\frac{4L_{lk}f_{sw}}{R_L}\right)\left(\frac{\frac{V_o}{V_{in} - V_o}}{D}\right) - D \tag{8.16}$$

Therefore, voltage gain at buck mode can be found from (8.13) and (8-16) as follows

$$\frac{V_o}{V_{in}} = \frac{\sqrt{(2D^2 + K)^2 + 8KD^2} - (2D^2 + K)}{2K} \tag{8.17}$$

,where K is defined as $\frac{4L_{lk}f_{sw}}{R_L}$ in (8.17) for the sake of simplicity.

8.4.2 Boost mode

Voltage gain at boost mode is a little more complex than that of buck mode because both the switching frequency and duty cycle of converter changes in this mode. The V_{pn}, transformer leakage inductance voltage (V_{Llk}) and the rectified transformer current (I_{rec}) waveforms in Figure 8-12 are shown again in Figure 8-14 to derive voltage gain.

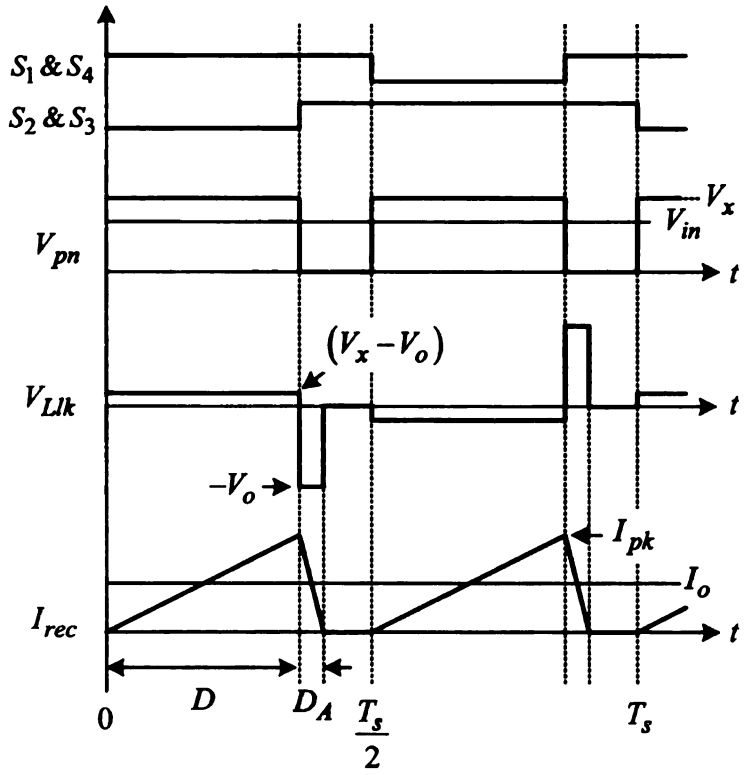


Figure 8-14 Waveforms at boost mode

Defining duty cycle D as the time interval when only two diagonal switches (S_1, S_4 or S_2, S_3) are closed over the half switching period ($T_s/2$) and D_A as the time interval when transformer current returns to zero from its peak value (I_{pk}), average voltage across the DZSN inductor and transformer leakage inductance (L_{lk}) during this half switching cycle must be zero due to flux balance condition.

First, the average value of V_{pn} is equal to input voltage V_{in}. This relationship is expressed as

$$D(V_x - V_{in}) = (1-D)V_{in} \tag{8.18}$$

$$\frac{V_x}{V_{in}} = \frac{1}{D} \tag{8.19}$$

Secondly, the average value of V_{Llk} during the half switching interval is zero. Thus

$$D(V_x - V_o) = D_A V_o \tag{8.20}$$

$$\frac{V_o}{V_x} = \frac{D}{D + D_A} \tag{8.21}$$

Thirdly, the average value of rectified transformer current (I_{rec}) is output current and it is represented as

$$\frac{1}{2}(D + D_A) I_{pk} = \frac{V_o}{R_L} \tag{8.22}$$

,where I_{pk} is defined as

$$I_{pk} = \left(\frac{V_x - V_o}{L_{lk}}\right) D \frac{T_s}{2} \tag{8.23}$$

In this boost mode, the converter switching frequency changes with D proportionally and the relationship is explained in Figure 8-15.

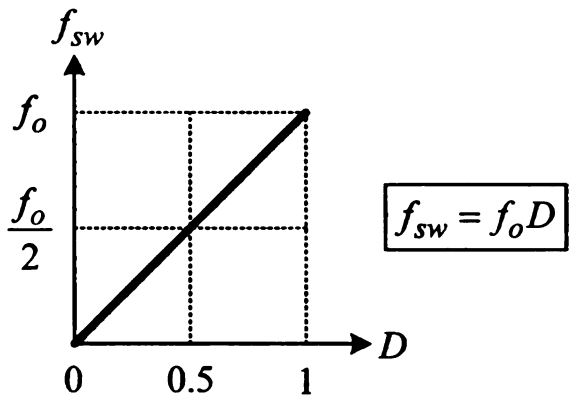


Figure 8-15 Relationship between f_{sw} and D

In Figure 8-15, f_o is defined as the frequency when D is equal to 1. Thus, f_o is 150 kHZ.

From (8-19), (8-21), and the equation in Figure 8-15, the voltage gain at boost mode is expressed as

$$\frac{V_o}{V_{in}} = \frac{\sqrt{P^2 + 4\frac{P}{D}} - P}{2} \tag{8.24}$$

,where P is defined as $\frac{R_L}{4L_{lk}f_o}$ in (7-24) for the sake of simplicity.

From (8-17) and (8-24), overall voltage gain of the proposed DZSN dc-dc converter is plotted in Figure 8-16.

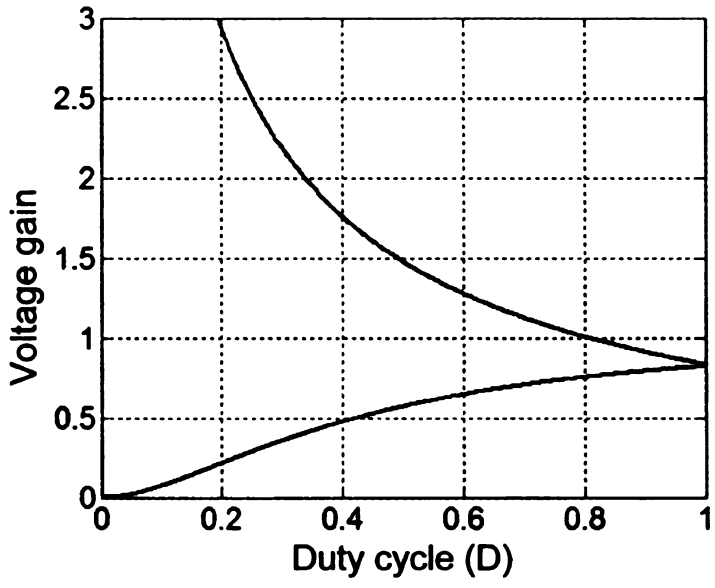


Figure 8-16 Voltage gain of the DZSN dc-dc converter

8.5. Simulation and Experimental Results of the Proposed DZSN DC-DC Converter.

Based on the above mentioned theoretical analysis, a prototype using DZSN was built and tested to verify the operation of proposed dc-dc converter and its results are compared with simulation results.

Table 8-2 summarizes the test conditions and electrical specifications of the proposed converter. In this work, transformer leakage inductance (L_{lk}) is almost $2\,\mu H$.

Figure 8-17 and Figure 8-18 show the simulation and experimental results of the proposed dc-dc converter operating at buck mode. In this mode, an open circuit gate signal is employed and its gate signals are modulated to control V_o.

The experimental waveforms in Figure 8-18 are measured when Vin=70 V, Vo=50 V, Po=500 W and fsw=150 kHz. As can be seen, the simulation and experimental

waveforms are quite well matched. In this paper, the voltage overshoot in V_{pn} is measured without any snubber or clamp circuit. In practical use, a snubber or clamp circuit may have to be used to suppress the overshoot.

Table 8-2 Test conditions and electrical specifications of proposed DZSN dc-dc converter.

Electrical specifications		• V_{in}=30 -70 V • V_o=50 V • P_o=500 W • $R_L = 5\Omega$ • $L_{lk} = 2\mu H$
Devices used		• MOSFET: IRFB4620 (200 V/25 A), 2 in parallel • Diode: Schottky STPS41L60CG (60 V/20 A), 2 in parallel
Switching frequency	Buck mode	150 kHz
	Boost mode	75 kHz – 150 kHz

The waveforms at boost mode operation are shown in Figure 8-19 and Figure 8-20. In order to boost output voltage, a short circuit gate signal is used. Duty cycle and switching frequency of the converter are modulated to control V_o. The experimental waveforms are measured when Vin=30 V, Vo=50 V, Po=500 W and fsw=75 kHz. As can be seen, the simulation and experimental waveforms are quite well matched. The output voltage is clearly boosted in this mode.

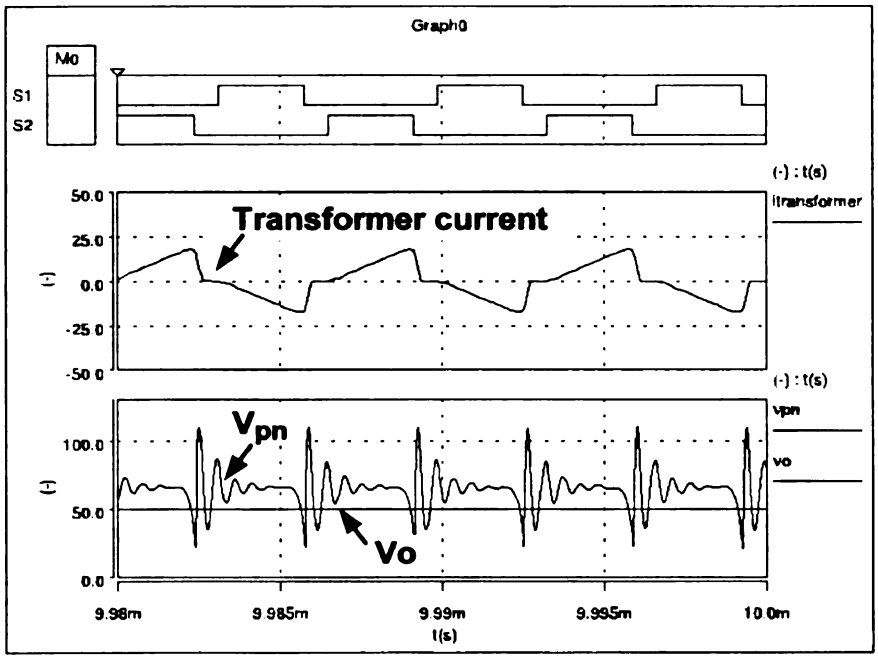


Figure 8-17 Simulation waveforms at buck mode (Vin>Vo).

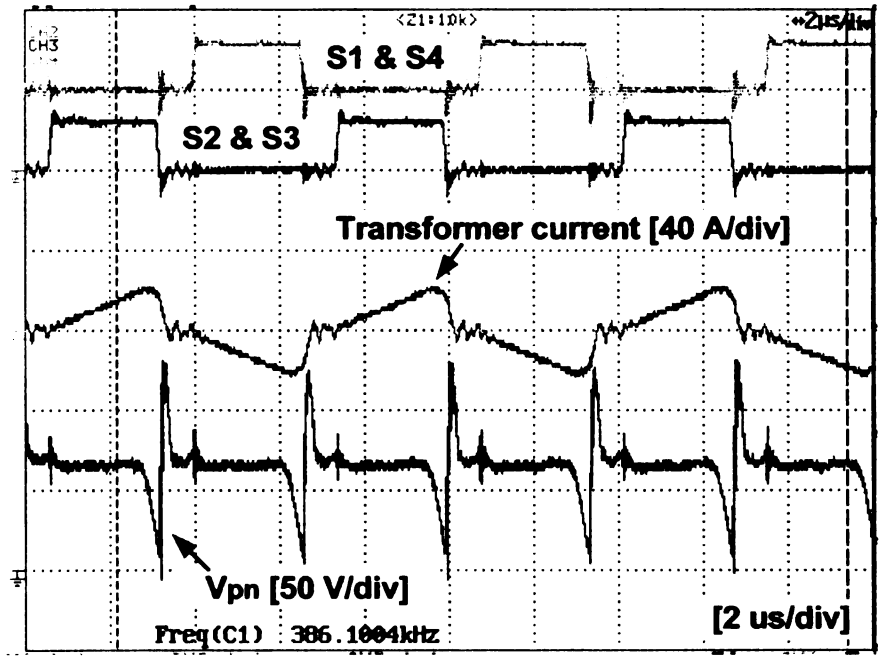


Figure 8-18 Experimental waveforms at buck mode(Vin>Vo).

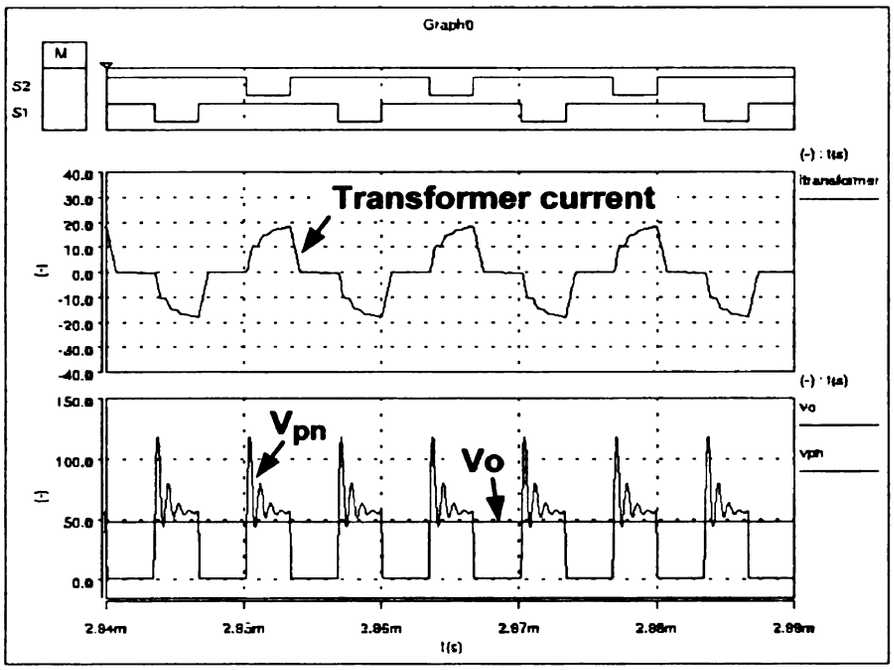


Figure 8-19 Simulation waveforms at boost mode (Vin<Vo).

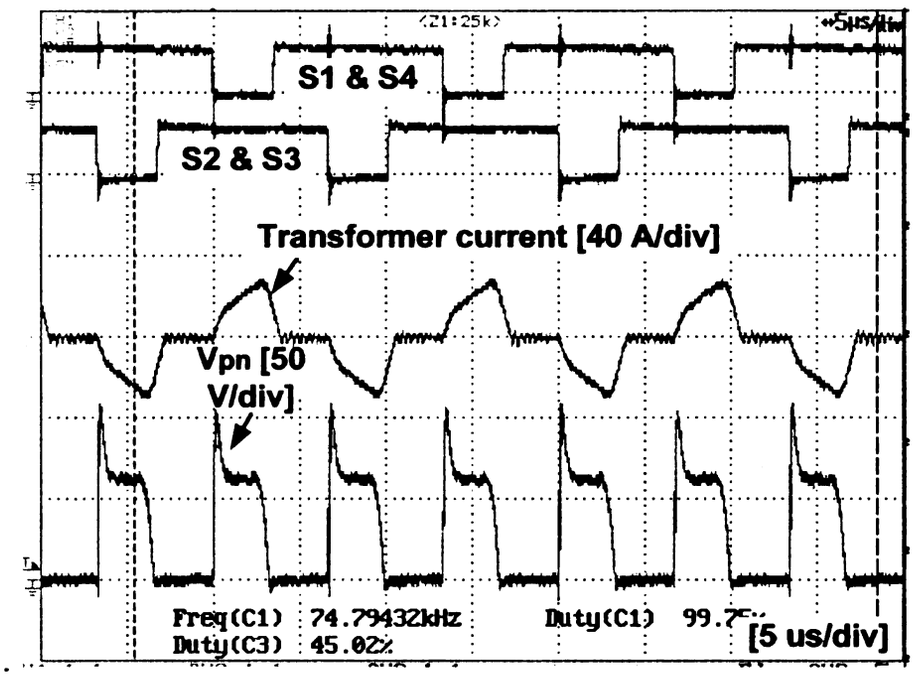


Figure 8-20 Experimental waveforms at boost mode (Vin<Vo).

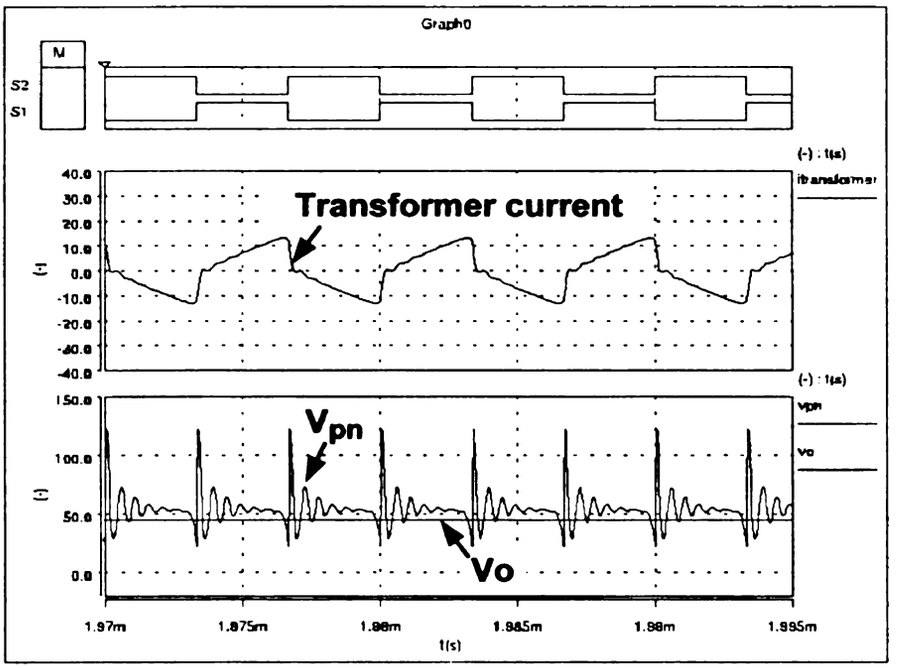


Figure 8-21 Simulation waveforms at normal mode (Vin=Vo).

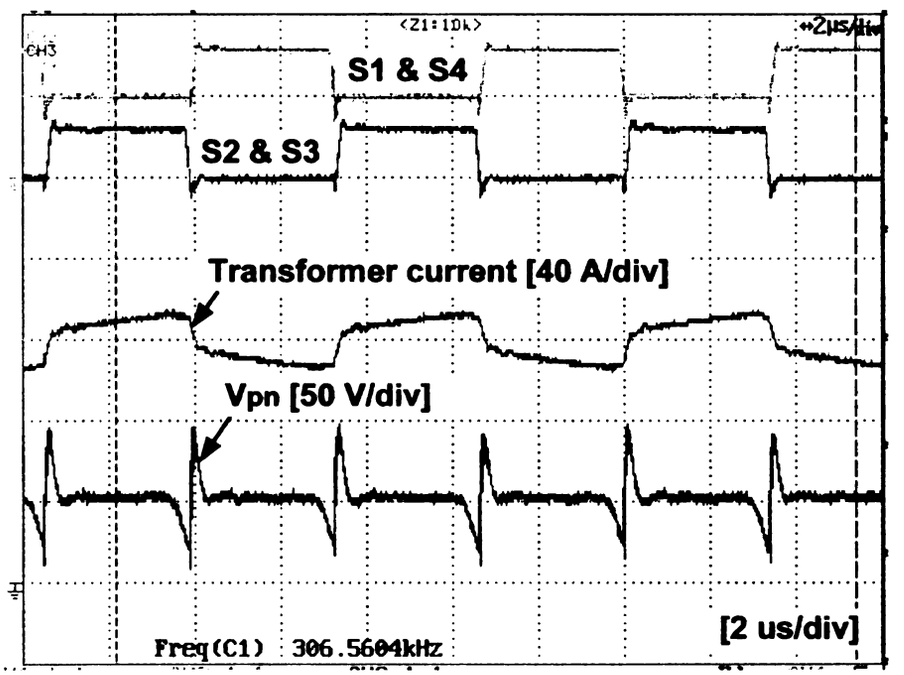


Figure 8-22 Experimental waveforms at normal mode (Vin=Vo).

Figure 8-21 and Figure 8-22 show the simulation and experimental waveforms tested at normal mode when V_{in} is equal to V_o. In this mode, the converter duty cycle is set to 0.5 and there is no open- or short-circuit in gate signal. Since transformer leakage inductance is used between input and output of the converter, there is a voltage drop across leakage inductance. Thus V_o is slightly lower than V_{in}.

Finally, efficiency of the proposed converter is measured when input voltage changes from 30 V to 70 V. Figure 8-23 shows the measured efficiency curve of the proposed converter. Maximum 94 % efficiency is achieved with the proposed dc-dc converter. The efficiency in buck mode is lower than that of boost mode. This is mainly caused by the switching loss in MOSFET because the switching frequency in buck mode is higher than that of boost mode. However, efficiency of the proposed converter can be improved if a soft switching method such as PSPWM is used.

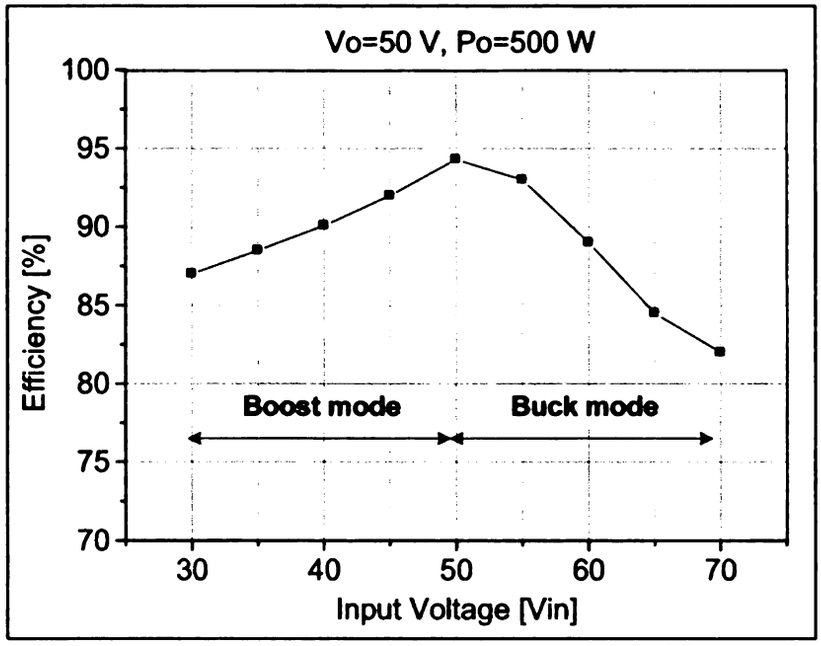


Figure 8-23. Efficiency of proposed converter vs. input voltage.

8.6. Conclusion

In this chapter, a novel power transfer concept has been proposed. The proposed distributed Z-source network dc-dc converter has the desired buck and boost converter functions. The advantages of the proposed dc-dc converter are as follows.

- The proposed dc-dc converter has buck and boost function. The output voltage can be greater than or smaller than input voltage. Therefore, the proposed dc-dc converter is a very desirable circuit topology when the input voltage range of the converter is wide.
- The proposed converter can be short- and open-circuited without damaging switching devices. Thus, it is very strong to EMI, and converter robustness and reliability are significantly improved.
- No snubber circuit is required in the output of the converter because a bulky output inductor is removed. Therefore, a low voltage diode can be used, which results in improved efficiency.

A 500 W prototype has been built and tested to verify the principle operation of the proposed converter.

Chapter 9. Contributions and Future Works

9.1. Contributions

This dissertation has the following contributions

- The soft switching passive snubber circuit is introduced to minimize the switching loss and voltage overshoot in IGBT. Its performances are verified with experimental results.
- A very compact and high efficiency transformer was designed to improve converter efficiency. Very detailed analysis on proximity effect was conducted and optimum copper thickness was found to minimize the proximity effect. The efficiency of transformer designed in this work is over 99.5 %.
- The voltage oscillation problem in transformer secondary rectifier diodes is introduced and several voltage clamping methods were compared. Finally, a new energy recovery clamp circuit is proposed. Neither lossy components nor additional active switches are used to clamp diode voltage. Therefore, the proposed ERCC is very promising for high voltage and high power dc-dc converters with wide ranges of input voltage.
- The 3 phase interleaved boost dc-dc converter using the integrated magnetic was developed for the series hybrid electric bus. Detailed design steps for the compact and high efficiency inductor was presented.

- In order to overcome the limitations of traditional V-source and I-source dc-dc converters, a novel dc-dc converter using the distributed Z-source network was introduced. The main properties of the distributed Z-source network was analyzed.
- The output voltage control method of the proposed dc-dc converter was presented. The proposed dc-dc converter can be short and open-circuited without damaging switching devices and it has the desired buck and boost function. Therefore, reliability of the proposed converter can be greatly enhanced

9.2. Recommendations for future works

The proximity effect in transformer winding is related to the distance (or space) between layers (or windings). Thickness of the insulation material (for example, the thickness of nomex paper) will have some effect on the proximity effect. However, this effect is not included in this work. Further research work should be done on this.

The proposed distributed Z-source network dc-dc converter was developed and tested with 500 W output power in this dissertation to prove the basic concept and principle of converter. Further work should be continued to extend power rating of the proposed converter and to increase converter efficiency. In addition to that, the core loss in network should be minimized to improve efficiency either by using ferrite core or by changing network structure.

Bibliography

[1] P. Fang Zheng, "Z-source inverter," IEEE Transactions on Industry Applications, vol. 39, no. 2, pp. 504-510, 2003.

[2] www.pwrx.com.

[3] R. S. Chokhawala, and S. Sobhani, "Switching voltage transient protection schemes for high-current IGBT modules," Industry Applications, IEEE Transactions on, vol. 33, no. 6, pp. 1601-1610, 1997.

[4] L. M. Tolbert, P. Fang Zheng, F. H. Khan *et al.*, "Switching cells and their implications for power electronic circuits." pp. 773-779.

[5] F. Z. Peng, L. M. Tolbert, and F. Khan, "Power electronics' circuit topology - the basic switching cells." pp. 52-57.

[6] F. Z. Peng, "Revisit power conversion circuit topologies-recent advances and applications." pp. 188-192.

[7] L. H. Mweene, C. A. Wright, and M. F. Schlecht, "A 1 kW 500 kHz front-end converter for a distributed power supply system," Power Electronics, IEEE Transactions on, vol. 6, no. 3, pp. 398-407, 1991.

[8] C. Jung-Goo, J. A. Sabate, H. Guichao *et al.*, "Zero-voltage and zero-current-switching full bridge PWM converter for high-power applications," Power Electronics, IEEE Transactions on, vol. 11, no. 4, pp. 622-628, 1996.

[9] C. Jung-Goo, B. Ju-Won, J. Chang-Yong *et al.*, "Novel zero-voltage and zero-current-switching full-bridge PWM converter using a simple auxiliary circuit," Industry Applications, IEEE Transactions on, vol. 35, no. 1, pp. 15-20, 1999.

[10] C. Jung-Goo, B. Ju-Won, J. Chang-Yong *et al.*, "Novel zero-voltage and zero-current-switching full bridge PWM converter using transformer auxiliary winding," Power Electronics, IEEE Transactions on, vol. 15, no. 2, pp. 250-257, 2000.

[11] F. Z. Peng, S. Gui-Jia, and L. M. Tolbert, "A passive soft-switching snubber for PWM inverters," Power Electronics, IEEE Transactions on, vol. 19, no. 2, pp. 363-370, 2004.

[12] L. H. Dixon, "Eddy current Losses in Transformer Windings and Circuit Wiring," Unitrode/TI Magnetics Design Handbook, 2000.

[13] J. A. Sabate, V. Vlatkovic, R. B. Ridley *et al.*, "Design considerations for high-voltage high-power full-bridge zero-voltage-switched PWM converter." pp. 275-284.

[14] V. Vlatkovic, J. A. Sabate, R. B. Ridley *et al.*, "Small-signal analysis of the phase-shifted PWM converter," Power Electronics, IEEE Transactions on, vol. 7, no. 1, pp. 128-135, 1992.

[15] R. W. Erickson, and D. Maksimovic, *Fundamentals of Power Electronics* 2nd ed ed.: Norwell, MA: Kluwer, 2001.

[16] C. W. T. McLyman, "Transformer and Inductor Design Handbook," 2004.

[17] www.ferroxcube.com.

[18] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics-converters, applications and design*, 3rd ed.: John Wiley & Sons Inc., 2003.

[19] P. L. Dowell, "Effect of eddy current in transformer windings." pp. 1387-1394.

[20] W. G. Hurley, E. Gath, and J. G. Breslin, "Optimizing the AC resistance of multilayer transformer windings with arbitrary current waveforms," Power Electronics, IEEE Transactions on, vol. 15, no. 2, pp. 369-376, 2000.

[21] E. C. Snelling, *Soft Ferrites, Propertise Applications*, 2nd ed.: London U. K. Butterworths, 1988.

[22] J. A. Ferreira, "Improved analytical modeling of conductive losses in magnetic components," Power Electronics, IEEE Transactions on, vol. 9, no. 1, pp. 127-131, 1994.

[23] S. Cuk, "Coupled Inductor and Integrated Magnetics Techniques in Power Electronics." pp. 269-275.

[24] A. F. Witulski, "Introduction to modeling of transformers and coupled inductors," Power Electronics, IEEE Transactions on, vol. 10, no. 3, pp. 349-357, 1995.

[25] www.changsung.com.

[26] http://en.wikipedia.org/wiki/Resistivity.

[27] L. Song-Yi, and C. Chern-Lin, "Analysis and design for RCD clamped snubber used in output rectifier of phase-shift full-bridge ZVS converters," Industrial Electronics, IEEE Transactions on, vol. 45, no. 2, pp. 358-359, 1998.

[28] A. Jangwanitlert, and J. C. Balda, "Phase-shifted PWM full-bridge DC-DC converters for automotive applications: reduction of ringing voltages." pp. 111-115.

[29] A. Bendre, S. Norris, D. Divan *et al.*, "New high power DC-DC converter with loss limited switching and lossless secondary clamp," Power Electronics, IEEE Transactions on, vol. 18, no. 4, pp. 1020-1027, 2003.

[30] J. A. Sabate, V. Vlatkovic, R. B. Ridley *et al.*, "High-voltage, high-power, ZVS, full-bridge PWM converter employing an active snubber." pp. 158-163.

[31] P. Ki-Bum, K. Chong-Eun, M. Gun-Woo *et al.*, "Voltage Oscillation Reduction Technique for Phase-Shift Full-Bridge Converter," Industrial Electronics, IEEE Transactions on, vol. 54, no. 5, pp. 2779-2790, 2007.

[32] K. Eun-Soo, J. Kee-Yeon, K. Moon-Ho *et al.*, "An improved soft-switching PWM FB DC/DC converter for reducing conduction losses," Power Electronics, IEEE Transactions on, vol. 14, no. 2, pp. 258-264, 1999.

[33] K. Eun-Soo, and K. Yoon-Ho, "A ZVZCS PWM FB DC/DC converter using a modified energy-recovery snubber," Industrial Electronics, IEEE Transactions on, vol. 49, no. 5, pp. 1120-1127, 2002.

[34] S. TingTing, and H. Nianci, "A novel zero-Voltage and zero-current-switching full-bridge PWM converter," Power Electronics, IEEE Transactions on, vol. 20, no. 2, pp. 286-291, 2005.

[35] H. Cha, R. Ding, Q. Tang *et al.*, "Design and Development of High-Power DC-DC Converter for Metro Vehicle System," Industry Applications, IEEE Transactions on, vol. 44, no. 6, pp. 1795-1804, 2008.

[36] S. A. Kharitonov, M. A. Petrov, D. V. Korobkov *et al.*, "A principle of calculation dynamic and static power losses with hard-switching IGBT." pp. 147-149.

[37] R. Ayyanar, R. Giri, and N. Mohan, "Active input-voltage and load-current sharing in input-series and output-parallel connected modular DC-DC converters using dynamic input-voltage reference scheme," Power Electronics, IEEE Transactions on, vol. 19, no. 6, pp. 1462-1473, 2004.

[38] R. Giri, V. Choudhary, R. Ayyanar *et al.*, "Common-duty-ratio control of input-series connected modular DC-DC converters with active input voltage and load-current sharing," Industry Applications, IEEE Transactions on, vol. 42, no. 4, pp. 1101-1111, 2006.

[39] A. Emadi, L. Young Joo, and K. Rajashekara, "Power Electronics and Motor Drives in Electric, Hybrid Electric, and Plug-In Hybrid Electric Vehicles," Industrial Electronics, IEEE Transactions on, vol. 55, no. 6, pp. 2237-2245, 2008.

[40] H. B. Shin, J. G. Park, S. K. Chung *et al.*, "Generalised steady-state analysis of multiphase interleaved boost converter with coupled inductors," Electric Power Applications, IEE Proceedings -, vol. 152, no. 3, pp. 584-594, 2005.

[41] P.-L. Wong, "Performance Improvements of Multi-Channel Interleaving Voltage Regulator Modules with Integrated Coupling Inductors," Ph. D Dissertation, Virginia Tech, 2001.

[42] W. Pit-Leong, X. Peng, P. Yang *et al.*, "Performance improvements of interleaving VRMs with coupling inductors," Power Electronics, IEEE Transactions on, vol. 16, no. 4, pp. 499-507, 2001.

[43] L. Jieli, C. R. Sullivan, and A. Schultz, "Coupled-inductor design optimization for fast-response low-voltage." pp. 817-823 vol.2.

[44] S. Chandrasekaran, and L. U. Gokdere, "Integrated magnetics for interleaved DC-DC boost converter for fuel cell powered vehicles." pp. 356-361 Vol.1.

[45] J. K. Watson, "Applications of Magnetism," 1985.

[46] F. Z. Peng, "Z-source networks for power conversion." pp. 1258-1265.

[47] H. Cha, L. Chen, R. Ding *et al.*, "An Alternative Energy Recovery Clamp Circuit for Full-Bridge PWM Converters With Wide Ranges of Input Voltage," Power Electronics, IEEE Transactions on, vol. 23, no. 6, pp. 2828-2837, 2008.

[48] P. J. Wolfs, "A current-sourced DC-DC converter derived via the duality principle from the half-bridge converter," Industrial Electronics, IEEE Transactions on, vol. 40, no. 1, pp. 139-144, 1993.

[49] H. Sang-Kyoo, Y. Hyun-Ki, M. Gun-Woo *et al.*, "A new active clamping zero-voltage switching PWM current-fed half-bridge converter," Power Electronics, IEEE Transactions on, vol. 20, no. 6, pp. 1271-1279, 2005.

[50] E. Adib, and H. Farzanehfard, "Zero-Voltage Transition Current-Fed Full-Bridge PWM Converter," Power Electronics, IEEE Transactions on, vol. 24, no. 4, pp. 1041-1047, 2009.

[51] M. Domb, R. Redl, and N. O. Sokal, "Nondissipative turn-off snubber alleviates switching power dissipation, second-breakdown stress and Vce overshoot: Analysis, design procedure, and experimental verification." pp. 445-454.

[52] R. D. Middlbrook, and S. Cuk, "A general unified approach to modelling switching converter power stages." pp. 73-86.

[53] http://boostbuck.com/TheFourTopologies.html.

[54] W. Jin, F. Z. Peng, J. Anderson *et al.*, "Low cost fuel cell converter system for residential power generation," Power Electronics, IEEE Transactions on, vol. 19, no. 5, pp. 1315-1322, 2004.

[55] B. Hua, and C. Mi, "Eliminate Reactive Power and Increase System Efficiency of Isolated Bidirectional Dual-Active-Bridge DC-DC Converters Using Novel Dual-Phase-Shift Control," Power Electronics, IEEE Transactions on, vol. 23, no. 6, pp. 2905-2914, 2008.

[56] Y. Bo, F. C. Lee, A. J. Zhang *et al.*, "LLC resonant converter for front end DC/DC conversion." pp. 1108-1112 vol.2.

[57] B. Yang, "Topology Investigation for Front End DC/DC Power Conversion for Distributed Power System," Ph. D Dissertation, Virginia Tech, 2003.

[58] P. Fang Zheng, S. Miaosen, and Q. Zhaoming, "Maximum boost control of the Z-source inverter," Power Electronics, IEEE Transactions on, vol. 20, no. 4, pp. 833-838, 2005.

[59] C. Dong, and F. Z. Peng, "A Family of Z-source and Quasi-Z-source DC-DC Converters." pp. 1097-1101.

[60] J. Anderson, and F. Z. Peng, "Four quasi-Z-Source inverters." pp. 2743-2749.

[61] J. C. Rosas-Caro, F. Z. Peng, H. Cha *et al.*, "Z-Source-Converter-Based Energy-Recycling Zero-Voltage Electronic Loads," Industrial Electronics, IEEE Transactions on, vol. 56, no. 12, pp. 4894-4902, 2009.

[62] Y. Tang, S. Xie, C. Zhang *et al.*, "Improved Z-Source Inverter With Reduced Z-Source Capacitor Voltage Stress and Soft-Start Capability," Power Electronics, IEEE Transactions on, vol. 24, no. 2, pp. 409-415, 2009.

[63] R. Reeves, "Inductor-Capacitor Hybrid," ibid, vol. 122, no. 11, pp. 1323-1326, 1975.

[64] J. W. Phinney, D. J. Perreault, and J. H. Lang, "Synthesis of Lumped Transmission-Line Analogs," Power Electronics, IEEE Transactions on, vol. 22, no. 4, pp. 1531-1542, 2007.

[65] J. W. Phinney, D. J. Perreault, and J. H. Lang, "Radio-Frequency Inverters With Transmission-Line Input Networks," Power Electronics, IEEE Transactions on, vol. 22, no. 4, pp. 1154-1161, 2007.

[66] T. Sato, S. Ikeda, K. Yamasawa *et al.*, "Transmisson-line low-pass filter for switching power supplies." pp. 1972-1978 vol.2.

[67] Z. Lingyin, and J. D. van Wyk, "Wideband modeling of integrated power passive structures: the series resonator," Power Electronics, IEEE Transactions on, vol. 19, no. 2, pp. 523-530, 2004.

[68] Z. Lingyin, and J. D. van Wyk, "Frequency-domain modeling of integrated electromagnetic power passives by a generalized two-conductor transmission structure," Circuits and Systems I: Regular Papers, IEEE Transactions on, vol. 51, no. 11, pp. 2325-2337, 2004.

[69] H. Cha, and F. Z. Peng, "Distributed Z-source network DC-DC converter." pp. 816-821.

[70] I. S. B. Pedro L. D. Peres, Amauri Lopes, "Transmission Line Modeling: A Circuit Theory Approach," Jstor, vol. 40, no. 2, pp. 347-352, 1998.

[71] L. Zhao, "Generalized Frequency Plane Model of Integrated Electromagnetic Power Passives," Ph. D Dissertation, Virginia Tech, 2004.