This is to certify that the
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PHOTOVOLTAIC SYSTEM FOR STANDALONE/
GRID-CONNECTED APPLICATIONS

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SANGMIN HAN

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Major Professor's Signature

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PHOTOVOLTAIC SYSTEM FOR STANDALONE/GRID-CONNECTED APPLICATIONS

By

Sangmin Han

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ABSTRACT

PHOTOVOLTAIC SYSTEM FOR
STANDALONE/GRID-CONNECTED APPLICATIONS

By

Sangmin Han

This Research develops design, analysis, and implementation of a series connected PV system for stand-alone/grid-connected photovoltaic power generation. The objective of the gateway dc-ac conversion system is to develop a low-cost conversion system based on the intelligent controller to provide clean residential electricity. The feature of the prototype includes: (1)the combination of dc-dc, dc-ac and/or ac-dc converters for the flexible and uninterruptible energy utilization; (2)a smart algorithm for optimizing the power consumption and defining priority on the demand system. A buck converter is used for the MPPT implementation and presents the functions of battery charger and step-down converter. The dc-dc converter realize phase shifting to control power flow through a transformer with a MOSFET full bridge on the low voltage side. In addition, a voltage doubler on the high voltage side is installed to achieve enough high voltage to run the inverter. The operation principle, theoretical analysis, simulation and experimental results are presented in this paper.

To my parents, Youngyul Han and Eunmo Kim

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CHAPTER 1

1.1 Motivations and Objectives of Research

Renewable energy sources become a more and more important contribution to the total energy consumed in the world. Because of their independence from limited fossil and nuclear fuels and their low impact on the environment will become the only crisis-proof and reliable energy supply within the next decades. Although PV energy has received considerable attention over the last few years, the high installation cost of PV systems and the low conversion efficiency of PV modules are the major obstacles to using this alternative energy source on a large scale. Therefore, many studies are being researched in order to minimize these disadvantages [1]–[5]. In 2009 the idea of the Gateway project was introduced with the goal to develop a low cost sustainable source of electrical power to residential applications. Development of a low-cost DC/AC inverter and controller system to support the commercialization of a maximum 1kW photovoltaic cell module providing clean residential electricity (each input and output is rating on 1kW). The system also needs to provide an AC/DC inverter with the same capacity. Ideally the optimization of the system will reduce the number of electronic components in each inverter (it is requirement to have a single inverter for the system). A smart algorithm for optimizing the power consumption and defining priority on the demand system are also required. The design of the inverter should optimize a share DC bus between the DC inputs and the rectified AC inputs considering the best trade-off between efficiency and cost. It consists of a photovoltaic (PV) array for electricity generation, battery for energy storage, digital control system to perform maximum power point

tracking (MPPT) and battery charge control, and various DC loads and AC loads.

1.2 Background

Highly reliable and efficient power processing systems allow exploitation of the enormous potential of the renewable sources by transforming the maximum available power into an electrical one, fed into the grid or converted into a high density energy vector for being stored and used in another place or at another time, when the primary source is not available. PV industry is growing at more than 30% per year and the cost of PV energy will reach the break-even point very soon in many countries. The most relevant goals of PV energy include 40% cost reduction of PV panels and of the power-converter stage within five years, increased efficiency of both panels and converters, and considerable improvement in converter reliability. These goals are driving the research toward several directions: Higher efficiency of the power converter such as transformerless topologies and converters based on silicon carbide devices, maximum power extraction algorithms, integration of the power converter in the panel to reduce the problem of minor energy production due to panel mismatch and advanced islanding detection algorithms that help monitor grid connection and compliance with grid standard and codes. These will have impact on safety, since undetected island in the power grid may cause hazards to user and utility workers. The main objective of our project is to design and construct a PV based system that produces electric energy and operates in dual mode, supplying stand alone AC loads or the grid, while minimizing its cost and size. The system's main properties are production of quality electricity from a renewable source to reduce dependence on fossil fuels and the associated emissions of pollutants, reduce cost of energy consumption by being able connect to the grid: sell energy and

charge the energy in storage batteries which are the most expensive system components per watt. Our goal is to design and develop an 3 module series connected system that will handle the task described and implement the Maximum Power Point Tracking (MPPT) algorithm to achieve the maximum power possible from the PV panel and synchronization with the utility grid.

1.3 System Configuration

The developed conversion system depicted in Figure 1 provides energy to both dc and ac load from PV panels and ac grid together. The PV panels are connected via the dc input terminal; the utility ac grid is plugged in through the ac input. Besides, a 48 V battery stack is paralleled with the dc output terminal on the purpose of energy storage. In order to extract the maximum power of the PV array, the implementation of the maximum power point tracking (MPPT) in stand-alone/grid-connected systems is generally accomplished by the series connection of a dc–dc buck converter between the PV array and the load or the energy storage element.

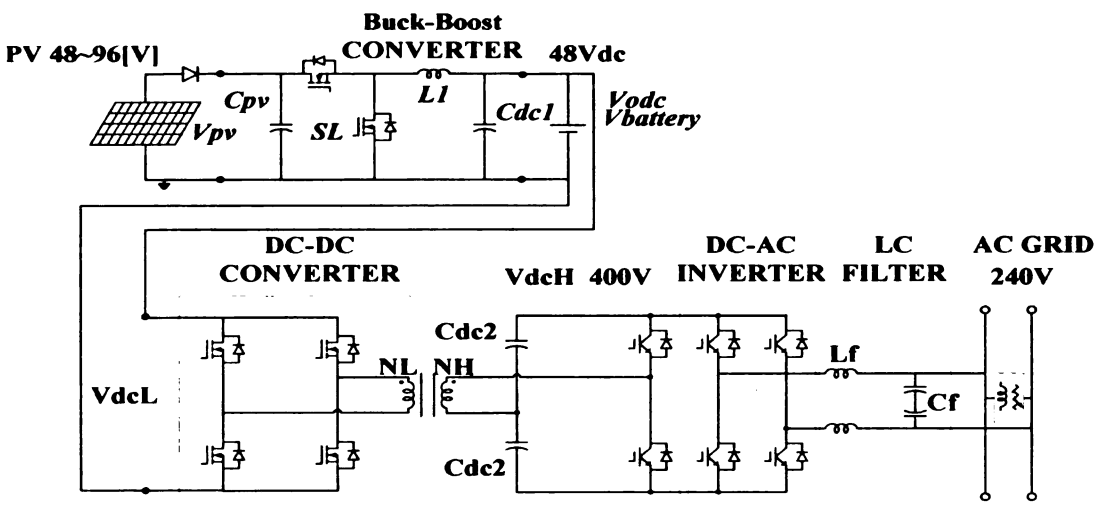


Figure 1 Overall PV System Configuration

Since the desired dc voltage is 400 V which is much higher than the dc bus voltage of 48V, that is, a large step-up conversion ratio is required for the dc-dc converter, the use of a transformer can allow better converter optimization. By proper choice of the transformer turns ratio, the voltage or current stresses imposed on the switches and diodes can be minimized, leading to improved efficiency and lower cost. On the other hand, the transformer can provide galvanic isolation between the high voltage and the low voltage to satisfy safety requirements. As shown in , a full-bridge in low voltage side (LVS) and a half-bridge in high voltage side (HVS) coupled by a high-frequency transformer are used for the dc-dc converter.[6] Proposed topology is shown in Figure 1 and a general description is explained next chapters. The inverter module consists of one IPM switches along with 3000uF of input capacitor. The output of the inverter is fed to the inductor-capacitor (LC) line filter. The series-connected, 2mH inductors and parallel 7.5uF capacitors are used in order to achieve desired voltage and current ripple characteristics. The output of the inverter is a single-phase, 60 Hz, 240V waveform. The test setup includes: the inverter; a 240V, 60Hz AC source that emulates the utility grid; and one sets of resistances representing the local load. The inverter and utility are connected to each other through 1 single-phase breakers. When breaker is closed; the inverter operates in the utility-connected mode. In that scenario, both the inverter and utility provide power to the local load. When breaker is opened; the inverter operates in the stand-alone mode. In this scenario, only the inverter provide power to the local load.

CHAPTER 2

2.1 DC-DC CONVERTER Topology

The dc-dc converter between the dc source and 48 V dc bus, termed as PV-connected converter, is used to transmit electricity from photovoltaic array (variable) to the dc bus (constant). Figure 2 shows the circuit of the PV-connected converter. It is a dc-dc buck converter consisting of two switches with anti-parallel diode, an inductor and two capacitors. As described in specifications, the maximum output power of PV array is 1 kW, so the capacity of the converter should match the demand. The PV-connected converter will work in buck mode (*variable input constant output*) when power flows from PV to dc load.

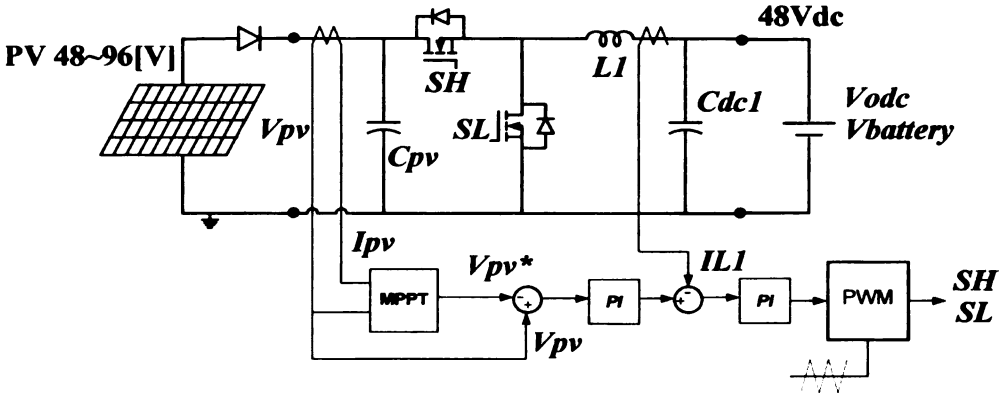


Figure 2 PV-Connected Converter (between PV array and 48V DC bus)

Given that the output voltage is *Vodc* = 48 V and the input voltage *Vpv* varies in a wide range from 48V to 96 V. The maximum input/output power is 1 kW. So, the maximum output current is *Iodc,max* = 1kW/48 V = 20.83 A, and the input current is *Iin* = 1kW/(48 ~ 96 V) = 20.83 ~ 10.41 A. The equivalent load resistance is *R* = 48 V / 20.83 A = 2.3 Ω. The basic relationship of the PV-connected converter in buck mode

is $V_{Odc} = V_{PV} \times D_{bu}$,and $I_{Odc} = I_{in} / D_{bu}$ where D_{bu} is the duty cycle. Therefore, D_{bu} is in a range of 1.0 ~ 0.5.

2.2 PV Source Model & MPPT Algorithm

Figure 3 shows the current and voltage (I-V) characteristics of the typical PV array used for residential power generation. These characteristics show the PV array behaving as a current source, in the sense that the current remains constant as the voltage varies. The standard Buck topology would have limited performance with a current source for its electrical power input, since the output current of the converter could never be higher than the maximum input current.

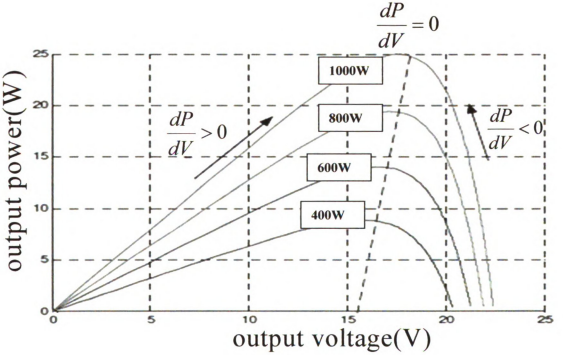


Figure 3 Typical PV panel characteristic

The understanding of solar cell source behavior is necessary to specify the size of solar array system or to study the stability of regulators. Placing the solar panels in an

optimal way is an effective measure to take to maximize the energy yield from a photovoltaic-installation. Shading can rarely be completely avoided, certainly not in urban or suburban environments. At higher latitudes the sun is often close to the horizon, which makes the shading problem more severe than at low latitudes. Therefore, especially for high-latitude locations and urban/suburban sites, a shading-tolerant system should be chosen. Furthermore, the direction south/north (azimuth) and elevation angle should also be considered. Any shading of the solar panels will lead to considerable reduction in energy yield, even if just a small fraction of the panels is shaded. Consequently, the case in which the solar cells in the generation system do not operate under uniform generation conditions should be examined. The connection of photovoltaic modules with different operating currents and/or voltages characteristic may result in the performance of the array being less than the sum of the potential performances of individual modules. When connected in series, the current flowing through the lowest productive cell limits the entire array output. The problem arises when modules have different sizes, which may be a result of individual modules not exposed to the same lighting conditions, such as is the case with differently oriented modules or irregular shading of the array. Mismatch is more likely in large systems than in independent arrays, because individual modules may be oriented differently or they may be subject to varying degrees of shading and heating.

Taking into account that real operating conditions of a solar array are difficult to reproduce during tests, simulations to determine electrical characteristics will allow the researcher to gain more insight for better understanding and design. Performance gain is beneficial and can find applications in numerous areas such as the one described in

reference [6]. As the fine modeling of a cell's behavior is the basis for any solar generator, the solar cell model needs to be properly determined. Methods for simulation of general solar array configuration have been proposed; however, these implementations are associated with special-purpose simulation tools, and detailed modeling has not been performed.

2.2.1 Solar Cell Modeling

Solar cells are essentially a very large area p-n junction diode, where such a diode is created by forming a junction between the n-type and p-type regions. As sunlight strikes a solar cell, the incident energy is converted directly into electrical energy. Transmitted light is absorbed within the semiconductor by using the energy to excite free electrons from a low energy status to an unoccupied higher energy level. When a solar cell is illuminated, excess electron-hold pairs are generated by light throughout the material; hence the p-n junction is electrically shorted and current will flow. The equivalent circuit of a solar cell is represented by four components: a light-induced current source, a diode parallel to the source, a series resistor and a shunt resistor. The light-induced current is due to the separation and drift of the photon-generated electron–hole pairs under the influence of the built-in field. The corresponding current vs. voltage curves (I-V) equation is:

$$I = I_{ph} - I_{S1}(e^{\frac{q(V+IR_S)}{n_1 kT}} - 1) - I_{S2}(e^{\frac{q(V+IR_S)}{n_2 kT}} - 1) - \frac{V + IR_S}{R_S} \qquad (2.1)$$

where, I and V are the solar cell output current and voltage, I_{ph} is the generated photo-current, and I_{S1}, I_{S2} are the reverse saturation currents of each diode. The

parameters n_1, n_2 are diode ideality factors, T is the absolute temperature in Kelvin, k is the Boltzmann's constant $1.38\times10^{-23} J/K$ and q is the elementary charge $1.602\times10^{-19} C$. Consider a fixed environmental condition, a typical I-V characteristic of a solar cell is shown in Figure 4. The operating point on power vs. voltage curve (P-V curve) will depend on the solar array characteristic and the load. Assuming that initially there is no load, the operating point will be at the far right at the open-circuit voltage, Voc, of the solar array with zero current (*V = Voc, I = 0*). As the load increase, the operating point will move up and to the left, i.e. voltage at the solar array terminal decreased, while the power increases. As the load increases further, it will reach the maximum power point (MPP), where the power drawn from the solar cell is maximized. The voltage at this point is denoted by the maximum-power voltage (*Vmp*), and the current by maximum-power current (*Imp*). If the load increases beyond this point, the voltage decreases and power drawn from the solar array decreases. Eventually, the operating point will reach the far left at the short-circuit current, *Isc*, with zero voltage output (*V = 0, I = Isc*).

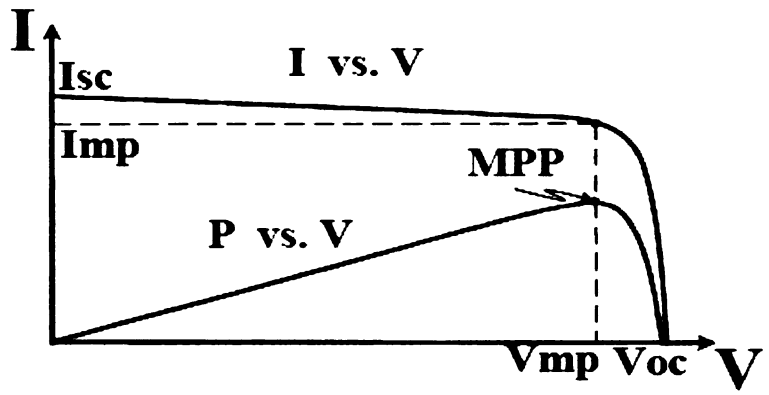


Figure 4 Typical I-V and P-V characteristic of solar cell

Solar cell model parameters vary with environmental conditions, the two most

important effects being temperature and irradiance. Solar cell open-circuit voltage decreases with increasing temperature, and the short circuit current is proportional to the amount of irradiance. The current vs. voltage curves (*I-V* curves) for various irradiance and temperature are shown in Figure 5 and Figure 6, respectively. The equations showing modeling effects of irradiance and temperature on model parameters are:

$$Iph = Iph\_tref\left[1 + K_O(T - Tref)\right] \tag{2.2}$$

$$I_S = I_{S\_tref}\left(\frac{T}{T_{ref}}\right)^3 \exp\left\{\frac{-qE_g}{nk}\left(\frac{1}{T_{ref}} - \frac{1}{T}\right)\right\} \tag{2.3}$$

$$R_S = R_{S\_tref}\left[1 - K_3(T - T_{ref})\right] \tag{2.4}$$

where T_{ref} is the cell reference temperature. E_g is the band gap energy of the semiconductor. K_O is the short-circuit temperature coefficient, and K_3 *is* the resistance temperature coefficients. Each parameter value is varied relative to the value at the cell reference temperature.

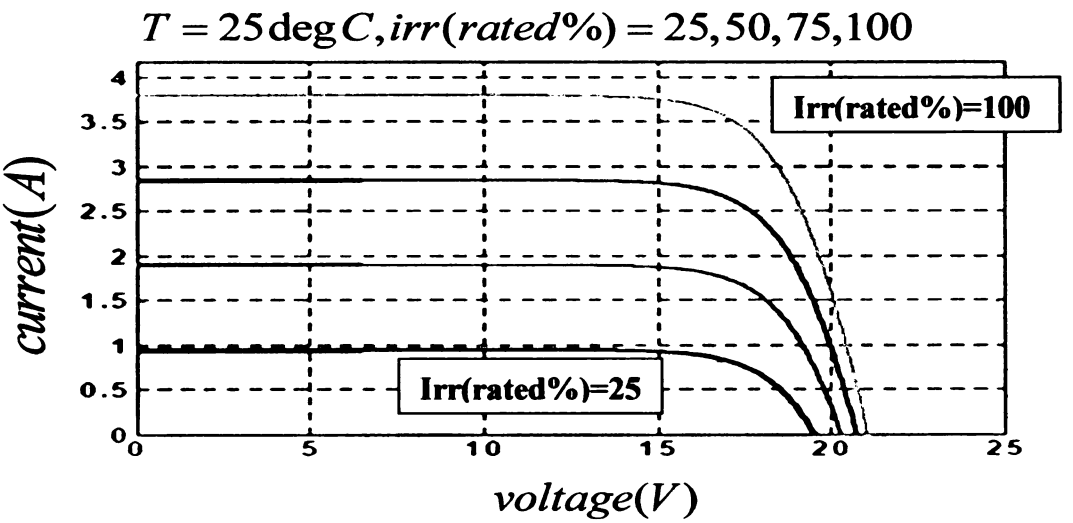


Figure 5 I-V curves for various irradiance

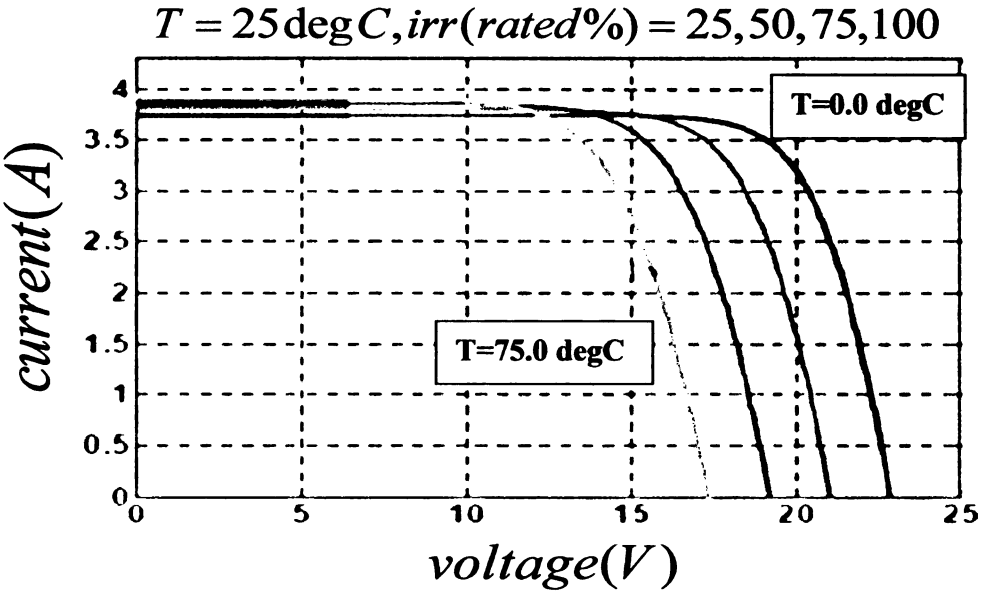


Figure 6 I-V curves for various temperature

2.2.2 MPPT Algorithm

The environmental condition under which a solar power system operates can be wide, as shown in I-V curves in Figure 7. The current-voltage relation of a solar array is variable throughout the day, as it varies with environmental conditions such as irradiance and temperature. In terrestrial applications, Low Irradiance, Low Temperature (LILT) condition reflects morning condition where the sun just rises. A High Irradiance, High Temperature (HIHT) condition might represent a condition near high noon in a humid area. High Irradiance, Low Temperature (HILT) condition can represent a condition with healthy sunlight in the winter. Finally, condition near sunset can be described by Low Irradiance, High Temperature (LIHT) condition. For space application, LILT characterizes a deep space mission or aphelion period, while HIHT condition is when satellite orbits near the sun (perihelion).

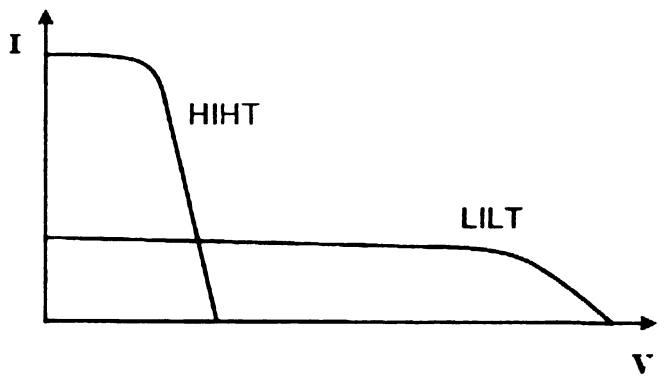


Figure 7 I-V characteristics under wide operating conditions

For a uniformly illuminated array, there is only one single point of operation that will extract maximum power from the array. In a battery charging system where the load seen by the solar modules is a battery connected directly across the solar array terminals, the operating point is determined by the battery's potential. This operating point is typically not the ideal operating voltage at which the modules are able to produce their maximum available power.

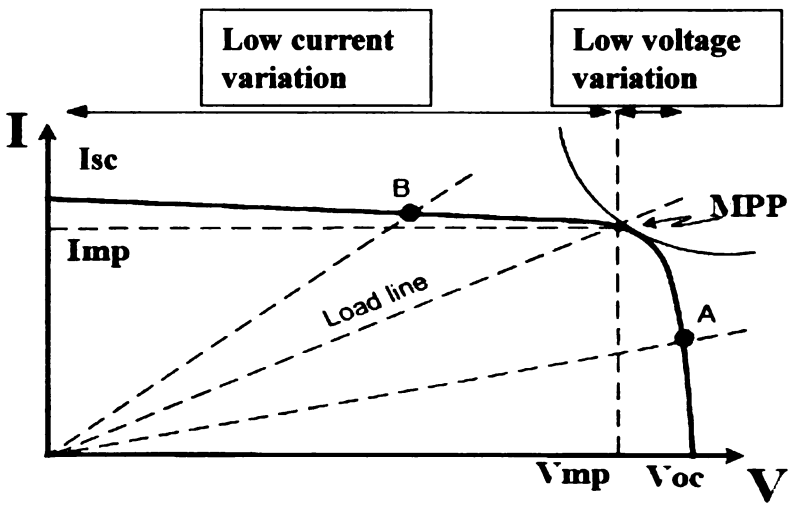


Figure 8 Direct coupled method

In the direct coupled method [7], in which the solar array output power is delivered directly to the loads, as shown in Figure 8. To match the MPPs of the solar array as closely as possible, it is important to choose the solar array I-V characteristic according to the I-V characteristics of the load. A general approach for the power feedback control

is to measure and maximize the power at the load terminal, and it assumes that the solar array maximum power is equal to the maximum load power. However, this maximizes the power to the load not the power from the solar array. The direct-coupled method cannot automatically track the MPPs of the solar array when the insulation or temperature changes. The load parameters or solar array parameters must be carefully selected for the direct coupled method. To be able to extract the maximum power from the solar array and to track the changes due to environment, therefore, a maximum power point tracking should be implemented. Devices that perform the desired function are known as Maximum Power Point Trackers, also called MPPTs or trackers. A tracker consists of two basic components, as shown in Figure 9: a switch-mode converter and a control with tracking capability. The switch-mode converter is the core of the entire supply. The converter allows energy at one potential to be drawn, stores as magnetic energy in an inductor, and then releases at a different potential. By setting up the switch-mode section in various topologies, either high-to-low (buck converter) or low-to-high (boost) voltage converters can be constructed. The goal of a switch-mode power supply is to provide a constant output voltage or current. In power trackers, the goal is to provide a fixed input voltage and/or current, such that the array is held at the maximum power point, while allowing the output to match the load voltage.

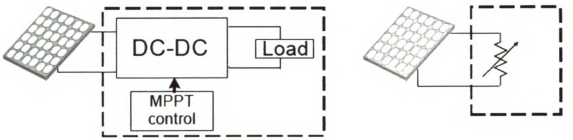


Figure 9 Basic components of a maximum power pointer tracker

When properly applied, a maximum power point tracking control can prevent the collapse of the array voltage under excessive load demand, particularly when supplying a signals, such as the array current and voltage, to determine a proper direction to move the operating point. Eventually, this continuously updated set point will fluctuate around the voltage corresponding to the array peak power point. By adjusting the operating point of the array to the point Vmp(maximum power point voltage), power output of the array is maximized, and the most efficient use of the solar array may be realized.

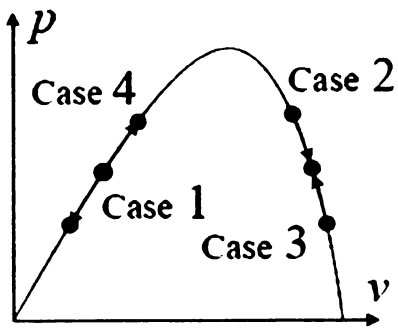
For a system without MPPT, the voltage will quickly collapse to zero. This phenomenon can be understood from the I-V characteristic of a solar array. The flatness of the I-V curve on the left of the MPP implies that a small incremental increase in current demand leads to large voltage change. A system with MPPT avoids the voltage collapse by keeping the operating point near the MPP. On the I-V curve, the operating point corresponding to the maximum-power point is around the "knee" region. Therefore, unlike other power systems with stiff voltage sources, power conversion from solar array sources with MPPT requires more robust design due to risks of an array voltage collapse under peak load demand or severe changes in the array characteristics. The location of the MPP of an I-V characteristic is not known a priori, and must be located.

2.2.3 Perturb and Observe Approach

As the name of the perturb-and-observe (P&O) states, this process works by perturbing the system by increasing or decreasing the array operating voltage and observing its impact on the array output power. The operating voltage is perturbed with every MPPT cycle. As soon as the MPP is reached, V will oscillate around the ideal operating voltage Vmp. Figure 10 summarized the control action of the P&O method.

The value of the reference voltage, *Vref*, will be changed according to the current operating point. For example, for when the controller senses that the power from solar array increases ($dP > 0$) and voltage decreases ($dV < 0$), it will decrease (-) *Vref* by a step size *C1*, so *Vref* is closer to the **MPP**. The **MPP** represents the point where *Vref* and scaled down *Vsa* become equal.

The oscillation around a maximum power point causes a power loss that depends on the step width of a single perturbation. The value for the ideal step width is system dependent and needs to be determined experimentally to pursue the tradeoff of increased losses under stable or slowly changing conditions. In fact, since the AC component of the output power signal is much smaller than the DC component and will contain a high noise level due to the switching DC-DC converter, an increase in the amplitude of the modulating signal had to be implemented to improve the signal to noise ratio (SNR), however, this will lead to higher oscillations at the MPP and therefore increase power losses even under stable environmental conditions.



Case	dP	dV	Action
1	< 0	< 0	-
2	< 0	> 0	+
3	> 0	< 0	+
4	> 0	> 0	-

Figure 10 Perturb & Observe(P&O) control action

Several improvements of the P&O algorithm have been proposed. One of the simplest

entails the addition of a 'waiting' function that causes a momentary cessation of perturbations if the algebraic sign of the perturbation is reversed several times in a row, indicating that the MPP has been reached. This reduces the oscillation about the MPP in the steady state and improves the algorithm's efficiency under constant irradiance conditions. However, it also makes the MPPT slower to respond to changing atmospheric conditions, worsening the erratic behavior on partly cloudy days. Another modification involves measuring the array's power P1 at array voltage V1, perturbing the voltage and again measuring the array's power, P2, at the new array voltage V2, and then changing the voltage back to its previous value and remeasuring the array's power, P1, at V1. From the two measurements at V1, the algorithm can determine whether the irradiance is changing. Again, as with the previous modifications, increasing the number of samples of the array's power slows the algorithm down. Also, it is possible to use the two measurements at V1 to make an estimate of how much the irradiance has changed between sampling periods, and to use this estimate in deciding how to perturb the operating point. This, however, increases the complexity of the algorithm, and also slows the operation of the MPPT. The MPPT techniques have much wider application than just photovoltaic alone, since similar functionality of power output versus loading can be seen in the *I-V* curves of other sustainable energy sources. Such sources are small water turbines and wind-power turbines; however, the actual physics behind the *I-V* curves for the various sources are different. The voltage, current, and power produced by such sources is variable in response to environmental conditions (insolation, pressure, or wind speed) and dependent on the electrical impedance of the load. Under any combination of environmental conditions, each of these sources is characterized by exactly one ideal load

impedance, which will result in operation at V_{MPPT} and maximum power transfer.

2.3 Design of DC-DC Converter

2.3.1 Inductance Value Selection

There are three passive components. One is inductor and the other two are capacitors. Generally, passive components are designed according to switching frequency and their current ripple or voltage ripple requirements. This section focuses on the inductor design and the capacitor design will be discussed in the later section. It is desired that the current ripple through the inductor has a peak magnitude equaling to 20% of the full-load value of the dc component current. For the buck converter, the current ripple is

$$\Delta I_{L1} = \frac{D_{bu} \cdot T_S}{2L_1}\left(V_{pv} - V_{odc}\right) = \frac{(1-D_{bu})T_S}{2L_1} \cdot V_{odc} \tag{2.5}$$

So, for the range duty cycle (1.0 ~ 0.5), we can select the inductance value:

$$\Delta I_{L1} = \frac{D_{bu} \cdot T_S}{2L_1} \cdot V_{odc} \le I_{odc,\max} \cdot 20\% \Rightarrow L_1 \ge \frac{(1-D_{bu})T_S}{2 \cdot I_{odc,\max} \cdot 20\%} \cdot V_{odc} \tag{2.6}$$

$$L_1 \ge \frac{(1-D_{bu})T_S}{2 \cdot I_{odc,\max} \cdot 20\%} \cdot V_{odc} = \frac{(1-D_{bu})T_S}{2 \cdot 20.83 \cdot 20\%} \cdot 48 = \frac{2.618}{f_S} \tag{2.7}$$

For a switching frequency of 10 kHz, the inductance must be no less than:

$$L_1 \ge \frac{2.618}{f_S} = \frac{2.618}{10 \cdot 10^3} = 0.2618 \cdot 10^3 (H) = 0.2618(mH)$$

For this inductance value, the current ripple is:

$$\Delta I_{L1} = \frac{(1-D_{bu}) \cdot T_S}{2L_1} \cdot V_{odc} = \frac{(1-0.5) \cdot 10^{-4}}{2 \cdot 0.2618 \cdot 10^{-3}} \cdot 48 = 4.58(A)$$

2.3.2 Inductor Design

Use area product, A_p, approach to design the inductor $L1$. First, calculate the A_p:

$$A_p = \frac{L_1 \cdot I^2_{pk} \cdot 10^4}{B_m J K_u} = \frac{0.000262 \times (20.83 + 4.584)^2 \times 10^4}{1 \times 300 \times 0.3} = 18.72(cm^4) \tag{2.8}$$

where Bm is operating flux density in [Tesla], J is current density in $[A/cm^2]$, K_u is copper fill factor. Second, select a powerlite C core from Metaglas because this kind of core has high saturation flux density and low power loss. The part number is AMCC-25 which $A_p = 18.72[cm^4]$, $A_w = 8.4[cm^2]$.Then the minimum number of turns can be calculated as

$$N_{\min} = \frac{L_1 \cdot I_{pk}}{B_m \cdot A_{core}} = \frac{0.000262 \times 25.4}{1 \times 2.7 \times 10^{-4}} \approx 26 \tag{2.9}$$

Now use the magnetization curves of AMCC-25 to check the design. The selected magnetizing force at peak power is 25×25.4 = 635[AT]. From the curve shown in Figure 11, we choose an air gap of 0.5 mm to prevent the core from getting in to saturation. Then the inductance can be computed as follows:

$$L_{1,cal} = A_L \cdot N^2 = 0.38 \cdot 26^2 \cong 256.8(uH) \tag{2.10}$$

In order to reduce the skin effect, Litz wire is the suitable selection for winding. Basically, AWG 33 wire is the recommended wire for 10 kHz – 20 kHz application. Here we select 310-33 AWG Litz wire which insulated area, $A_{cu} = 0.146[cm^2]$. Then the window utilization factor is

$$K_u = \frac{N \cdot A_{cu,ins}}{A_w} = \frac{26 \times 0.146}{8.4} = 0.45 \tag{2.11}$$

2.3.3 Capacitance of *Cdc*1 Selection

For PV-connected converter (in buck mode), the output voltage ripple (peak-to-peak) is expressed as

$$\triangle V_{p-p} = (2 \cdot \triangle V_{odc}) = \frac{V_{odc} \cdot T_S}{8L_1 \cdot C_{dc1}} \cdot (1 - D_{bu}) T_S = \frac{V_{odc} \cdot {T_s}^2}{8L_1 \cdot C_{dc1}} \cdot (1 - D_{bu}) \tag{2.12}$$

$$\frac{2 \cdot \triangle V_{odc}}{V_{odc}} = \frac{1}{8} \cdot \frac{{T_s}^2}{L_1 \cdot C_{dc1}} (1 - D_{bu}) = \frac{\pi^2}{2} (1 - D_{bu}) \left(\frac{f_c}{f_s} \right)^2$$

Where $f_c = \frac{1}{2\pi\sqrt{L_1 C_{dc1}}}$

Equation shows that the voltage ripple can be minimized by selecting a corner frequency of the low-pass filter at the output such that $f_c << f_s$ (Generally, f_s / f_c is with a factor of at least 10. It is desired that the voltage ripple (peak magnitude) is required to be 1%, hence, the necessary capacitance is calculated as

$$1\% \geq \frac{\triangle V_{odc}}{V_{odc}} = \frac{{T_s}^2}{8L_1 \cdot C_{dc1}} \cdot (1 - D_{bu}) \tag{2.13}$$

$$C_{dc1} \geq \frac{(1 - D_{bu}) {T_s}^2}{8L_1 \cdot 1\%} = \frac{(1 - 0.5) {T_s}^2}{8 \cdot 0.26 \cdot 10^{-3} \cdot 1\%} = \frac{2.4 \times 10^3}{{f_s}^2}$$

For a switching frequency of 10 kHz, the capacitance must be no less than

$$C_{dc1} \geq \frac{2.4 \times 10^3}{{f_s}^2} \geq \frac{3.97 \times 10^3}{(10 \times 10^3)^2} = 240 \times 10^{-6} (F) = 240 (uF)$$

Considering the operating voltage is 48 V, a 3paralled 100-V/100-μF film capacitor is selected for $Cdc1$.

Hence, the voltage ripple is

$$\triangle V_{odc} = \frac{V_{odc} \cdot {T_s}^2}{8L_1 \cdot C_{dc1}} \cdot (1 - D_{bu}) = \frac{48 \times (1-0.5) \times (10^{-4})^2}{8 \times 0.26 \times 10^{-3} \times 240 \times 10^{-6}} = 0.48(V) \tag{2.14}$$

2.3.4 Capacitance of Cpv Selection

C_{pv} is designed to smooth the current from PV and keep the voltage ripple of output of PV small to achieve good MPPT. For the capacitor C_{pv}, the value can be calculated in boost mode (D_{bo} = 0~0.5) as follows:

$$\triangle V_{pv} = (2 \cdot \triangle V_{pv}) = \frac{I \cdot D \cdot T_S}{C_{pv}} = \frac{P \cdot D \cdot T_S}{V_{pv} \cdot C_{pv}} = \frac{P \cdot D(1-D) \cdot T_S}{V_{odc} \cdot C_{pv}} \tag{2.15}$$

$$\frac{\triangle V_{pv}}{V_{pv}} = \frac{P \cdot D(1-D) \cdot T_S}{V_{odc} \cdot V_{pv} \cdot C_{pv}} = \frac{P \cdot D(1-D)^2 \cdot T_S}{{V_{odc}}^2 \cdot C_{pv}}$$

where Dbo = 0~0.5, P = 1kW. It is desired that the voltage ripple (peak magnitude) is required to be 1%, Hence

$$1\% \geq \frac{\triangle V_{odc}}{V_{odc}} = \frac{P \cdot D^2{}_{bu}(1-D_{bu}) \cdot T_S}{{V_{odc}}^2 \cdot C_{pv}} \tag{2.16}$$

$$C_{pv} \geq \frac{P \cdot D^2{}_{bu}(1-D_{bu}) \cdot T_S}{{V_{odc}}^2 \cdot 1\%}$$

The C_{pv} has its maximum at D = 0.66. It means

$$C_{pv} \geq \frac{1000 \times 0.66^2 \times (1-0.66) \cdot T_S}{48^2 \times 1\%} = \frac{6.42}{f_S}$$

For a switching frequency of 10 kHz, the capacitance must be no less than

$$C_{pv} \geq \frac{6.42}{f_S} = \frac{6.42}{10 \times 10^3} = 642(uF)$$

The highest operating voltage of C_{pv} is about 96 V, so four 200-V/390-μF aluminum electrolytic capacitor is chosen for C_{pv} in case of bigger capacity solar cell.

Device selection

The maximum voltage output by PV is 96 V. However, the switch and diode shall sustain the open-circuit voltage of the PV which is higher than the maximum output voltage usually. The open-circuit voltage of 96 V PV is about 120 V. The switch should be capable to sustain the voltage of 120 V. Generally, the voltage spike across switch is considered below 50% of the maximum voltage applied to switch. So, we can selected the rated voltage of the switch is

$$V_{switch} = 96 \times (150\%) = 144(V)$$

It is a buck converter from PV to dc load, so the output current is not less than the input current. The peak current through the switch occurs at maximum power of 1 kW. As calculated above, the current ripple is 4.584 A (at D = 0.5). So, the peak current through the switch is Ip = 20.83+ 4.584 = 25.4 [A]. The current rating of the switch should be at least 1.5~2.0 times the peak current. So, two 150-V/50-A MOSFETs are selected for PV-connected converter. 2 MOSFET devices are connected in parallel per switch to reduce the power loss.

2.4 DC-DC Converter Control Scheme

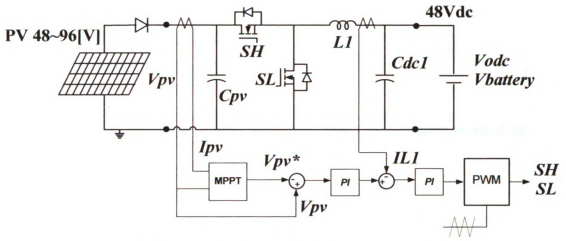


Figure 11 MPPT scheme for buck/boost converter

The converter will be controlled in the buck mode (variable input and constant output). When the converter works in the continuous conduction mode (CCM), the input and output voltages are related as follows:

$$V_{odc} = D_{bu} \cdot V_{PV} \tag{2.17}$$

Where V_{odc} is battery output voltage, V_{PV} is PV voltage and D_{bu} is the duty cycle in range 0.5 ~ 1. When the converter operates in the discontinuous conduction mode (DCM), the input and output voltage relation is: For constant input voltage:

$$\frac{V_{odc}}{V_{PV}} = \frac{D^2_{bu}}{D^2_{bu} + \frac{1}{4}(\frac{I_{odc}}{I_{LB,max}})} \tag{2.18}$$

Where I_{odc} is buck converter output current and $I_{LB,max}$ is max ripple in buck converter inductor current.

$$I_{LB,max} = \frac{T_S \cdot V_{PV}}{8 \cdot L_1} \tag{2.19}$$

Where T_s is switching period and L_1 is inductor value. For constant output voltage:

$$D_{bu} = \frac{V_{odc}}{V_{PV}} \cdot \left(\frac{I_{odc}}{(\frac{I_{LB,max}}{1-\frac{V_{odc}}{V_{PV}}})^{1/2}} \right) \quad \text{Where, } I_{LB,max} = \frac{T_S \cdot V_{odc}}{2 \cdot L_1} \tag{2.20}$$

The duty cycle is the unique control variable to adjust the operation point of the buck converter. Based on above equation, we can get

$$\frac{dD_{bu}}{dV_{PV}} = -\frac{V_{odc}}{{V_{PV}}^2} < 0 \text{ or } \frac{dV_{PV}}{dD_{Q1}} = -\frac{V_{odc}}{{D_{bu}}^2} < 0$$

From above equation, we can also get the same conclusion: $\frac{dD_{bu}}{dV_{pv}} < 0$

Considering all equation we've discussed, D_{bu} and V_{pv} have an inverse proportion relation in both CCM and DCM. Thus a duty cycle reduction causes a PV array output voltage increment if the battery voltage keeps invariable. Based on the conclusion, a control scheme with maximum power point tracking (MPPT) technology can be designed for buck converter, as shown in Figure 11. An inner current loop is applied to limit current.

2.4.1 Simulation Result of Buck Converter

Figure 12 shows the output current transient waveform. As we calculated above, output current is near 20.8[A] at 1Kw. Transient time is 0.03sec which satisfy our operation time.

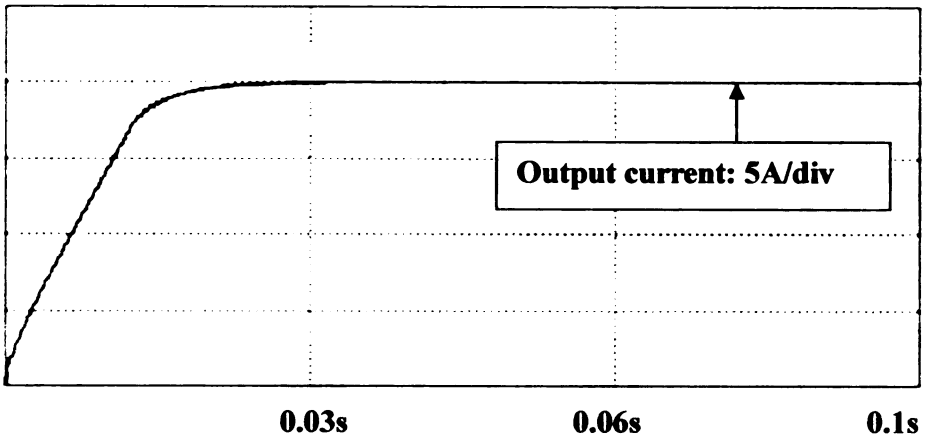


Figure 12 Buck converter output current

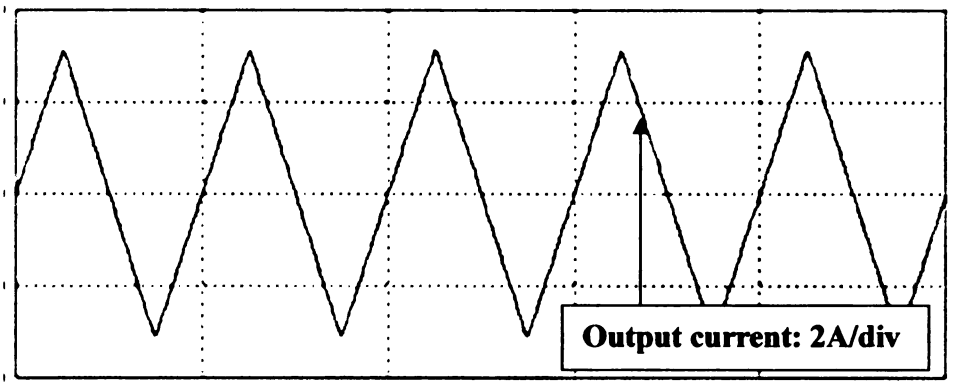


Figure 13 Buck converter output current ripple

Figure 13 shows the buck converter output current ripple which corresponds to what we calculated previous section. We set current ripple as 20% of output current which is near 4.5[A]. This ripple value satisfies inductor saturation point. Figure 14 shows the MPPT control algorithm in DC-DC converter system. By detecting PV current and voltage, MPPT algorithm can deduce the Vpv* voltage which value leads to maximum power point of PV panel. Vpv* compare with real PV voltage and(Vpv) go through PI controller with result of IL1* current. This value is updated every 1msec compare with real output inductor current to achieve desired output current.

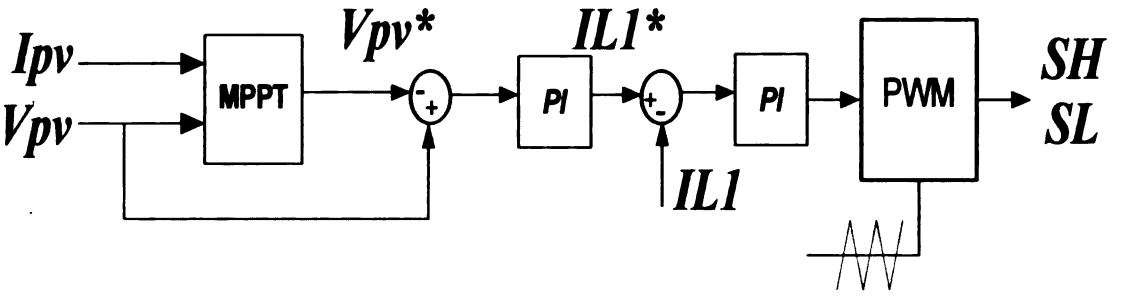


Figure 14 Control block diagram of MPPT system

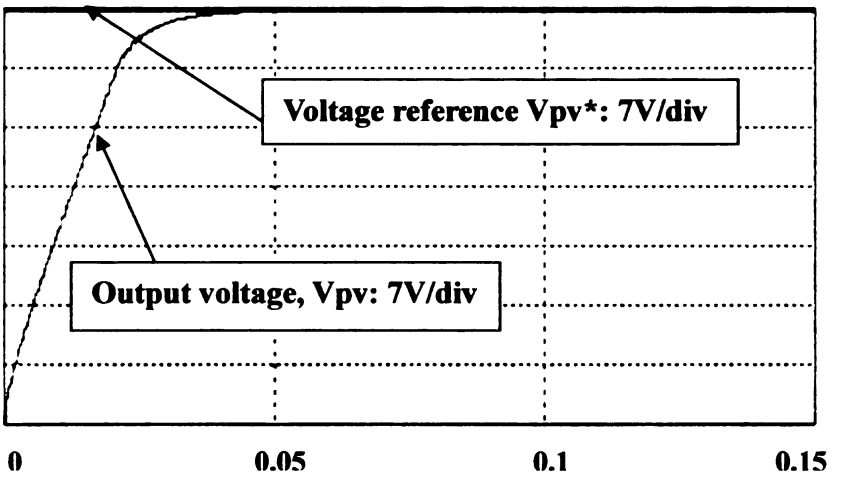


Figure 15 dc-dc converter voltage control waveform

Figure15 shows the voltage reference and real output voltage of buck converter.Voltage control loop is outer loop to current control loop. Voltage loop is 1kHz period while current loop is 10times faster than voltage loop period. Figure 16 shows the buck converter output current reference and real output current. This simulation is achieved in order to get appropriate Kp and Ki value. Blue waveform shows the output current reference which is near 20.8[A] and therefore red waveform follows its reference current in 0.03sec.

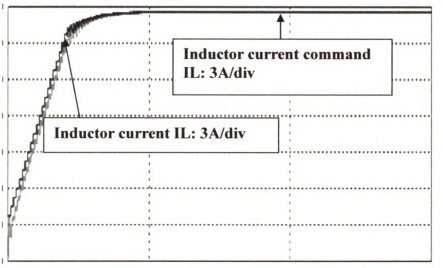


Figure 16 DC-DC converter current control waveform

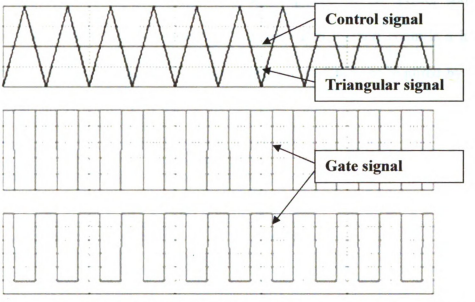


Figure 17 Switch signal at duty cycle 0.5(blue: triangular wave, red: gate signal)

Figure 17 shows the gate signal of both high side switch and lower side switch at the duty cycle 0.5. This signal shows when input voltage is 96V and output voltage is 48V in which to keep constant output voltage.

2.4.2 MPPT Simulation

In simulation, perturb and observation method is used to measure the PV array output power and to change the duty cycle of the dc/dc converter control signal. By measuring the array voltage and current using P&O method, the PV array output power is calculated and compared to the previous PV array output power. Depending on the result of the comparison, the duty cycle is changed accordingly and the process is repeated until the maximum power point has been reached. From Figure 18, PV voltage is around 66V and PV current is 15A. The implementation of the proposed method was only realized by matlab simulink simulation. Experimental results was replaced by DC power source which is same function as PV panel. However, this algorithm method controls a high efficiency Buck-type dc/dc converter and performs all control functions required by the MPPT process and battery charging, if required.

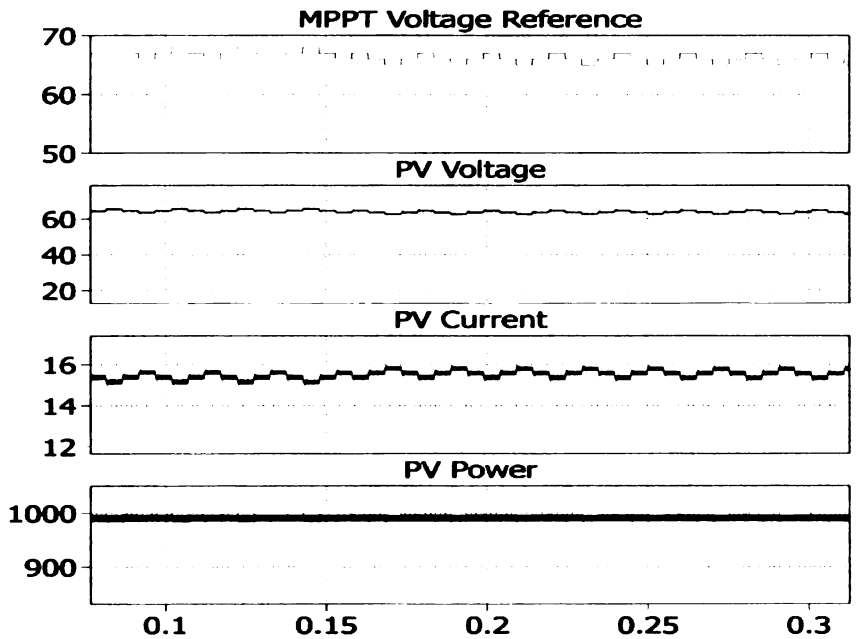


Figure 18 Simulation results of the MPPT(P&O)

2.4.3 Experimental Result

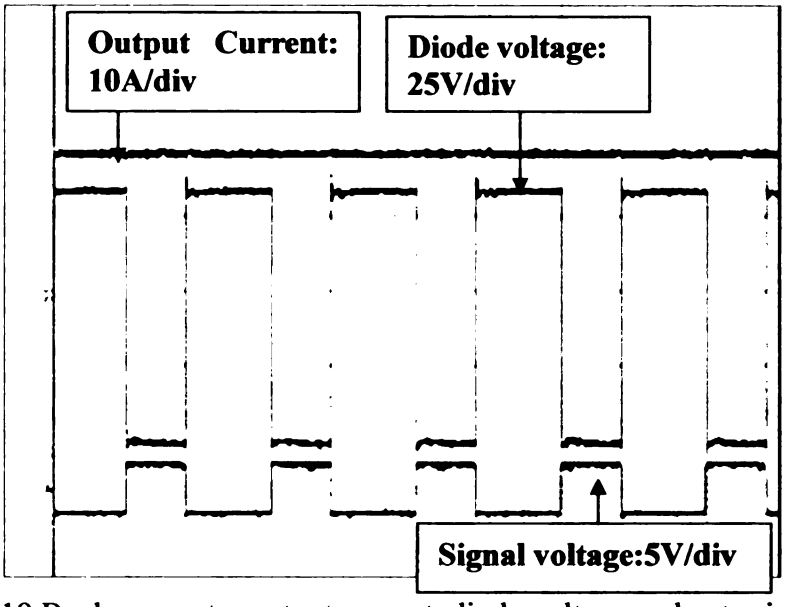


Figure 19 Buck converter output current, diode voltage and gate signal

We applied dc source with rectified grid voltage in order to replace PV source power. Verifying DC-DC buck converter control system with this configuration was appropriate since we only need to prove current controller of system. Figure 19 shows basic function of buck converter with 0.7 duty cycle. Figure 20 shows experimental control block diagram of DC-DC buck converter. However realizing MPPT control at the input side have not applied. By changing reference voltage to output voltage instead of PV voltage, control system give right duty cycle in order to follow reference output voltage.

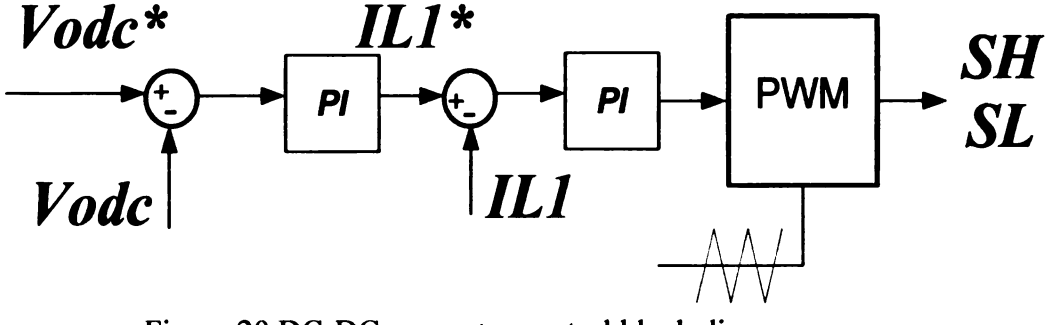


Figure 20 DC-DC converter control block diagram

Figure 21 shows the buck converter inductor current and output voltage. In order to verify 1kw power, input voltage was 75[V], average inductor current was 20[A] and output voltage was 48[V].

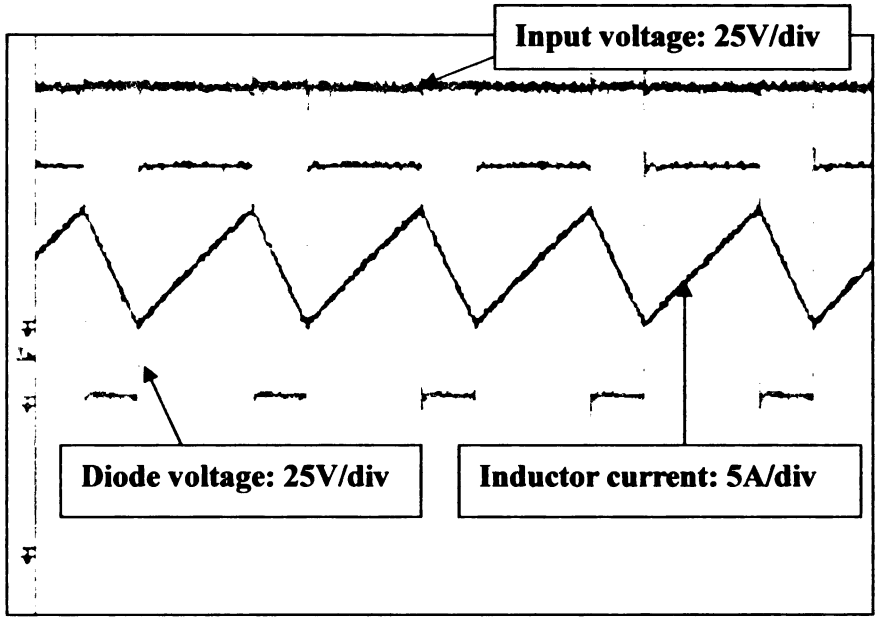


Figure 21 Buck/Boost converter 1kW power experiment

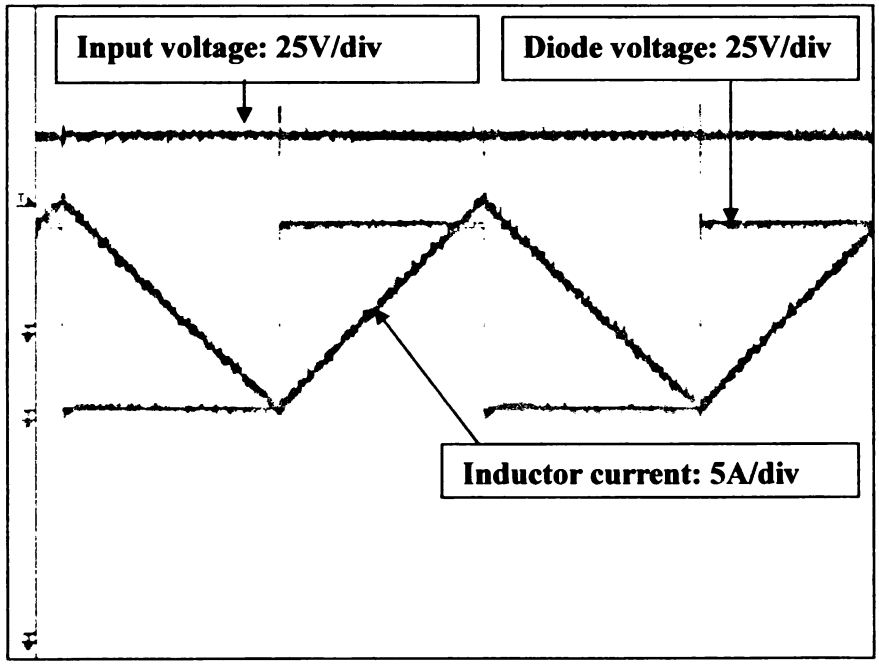


Figure 22 Inductor current, input output voltage & diode voltage

From Figure 22, we can calculate inductor value by knowing current ripple and inductor voltage. $L = V_L \times \frac{\Delta T}{\Delta I} = 52[v] \times \frac{48[\mu sec]}{10[A]} = 249.6[\mu H]$. Inductor value is similarly same as what we have calculated at the previous section. At 1Kw, current ripple was near 5[A].

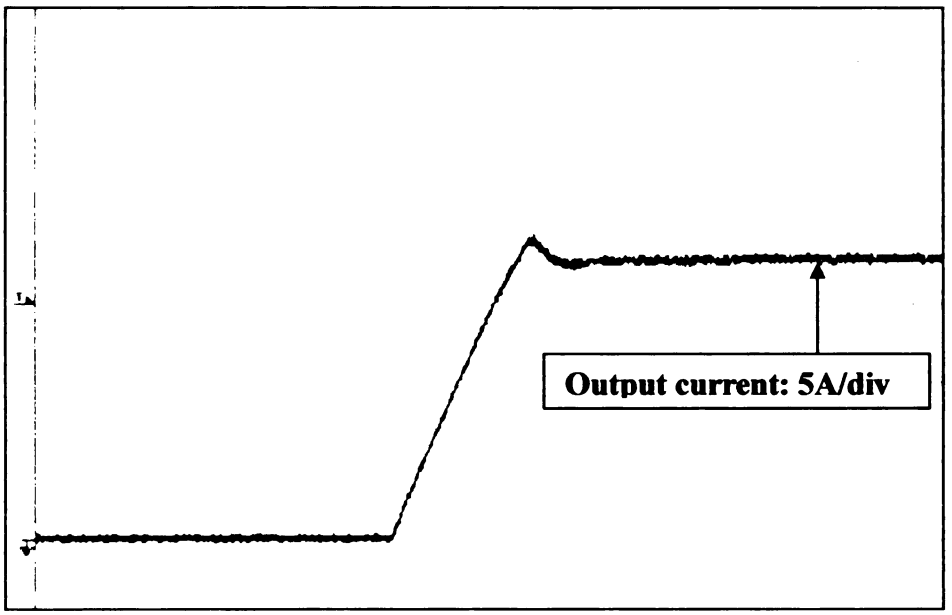


Figure 23 Current control transient waveform

Figure 23 shows output current which follows 18[A] current reference with 2.6[Ω] load resistor. Output voltage is 50[V]. It takes 6msec to reach command reference value. 6mesc is current transient time that is appropriate for current control for PV panel since PV don't need in high speed feedback for MPPT.

Figure 24 shows output voltage which follows 50[V] voltage reference with load resistor was 2.6[Ω]. It takes 60msec to reach command reference voltage. Transient condition is stable since voltage loop is 10times slower than current loop. It reaches steady state slower than current.

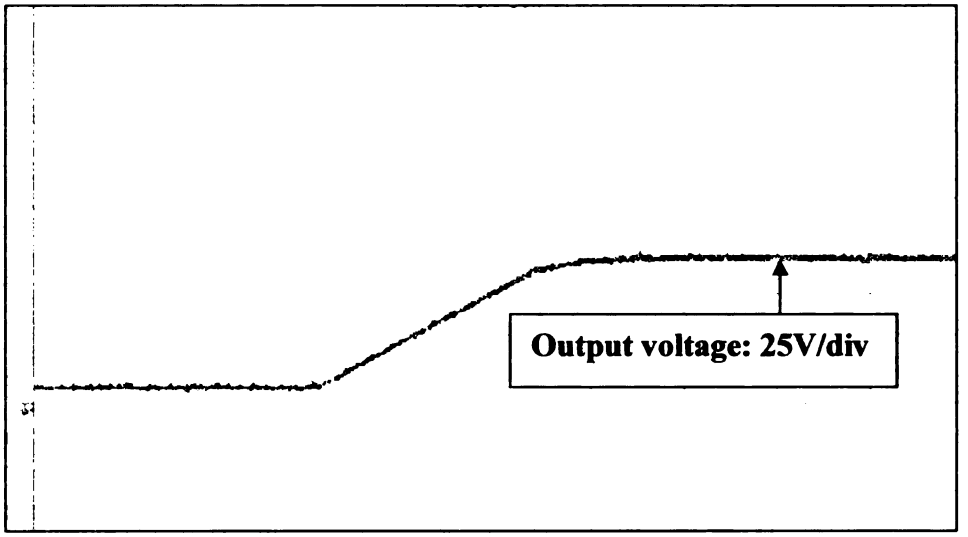


Figure 24 Voltage control transient waveform

CHAPTER 3

3.1 Isolated DC-DC Converter Topology

The dc-ac converter between PV or 48 V dc bus and utility grid, termed as grid-connected converter, is used to feed PV power into utility grid to supply ac load. On the other hand, it also can absorb real power from utility grid and transmit to dc load when PV power is not enough. Here, the power flow is bidirectional, so the grid-connected converter must be designed bidirectional. Because 48 ~ 96 V dc voltage cannot direct produce 240 V ac voltage by a single stage inverter, an additional step-up dc-dc converter is needed to produce sufficient voltage (400 Vdc) for the inverter input. Since the utility grid is a single-phase system, the following inverter should meet this demand. Figure 25. shows the configuration of the grid-connected PCS. As shown in Figure 25, the grid-connected PCS includes two stages: a dc-dc converter and a dc-ac inverter with a filter.

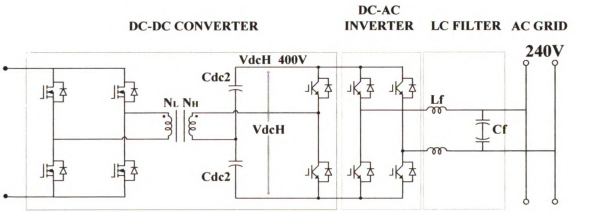


Figure 25 Grid-connected converter(between 48V DC bus and 240V AC bus)

Since the hoped dc voltage is 400 V which is much higher than the dc bus voltage of 48V, that is, a large step-up (or step-down for reversed power flow) conversion ratio is required for the dc-dc converter, the use of a transformer can allow better converter

optimization. By proper choice of the transformer turns ratio, the voltage or current stresses imposed on the switches and diodes can be minimized, leading to improved efficiency and lower cost. On the other hand, the transformer can provide galvanic isolation between the high voltage and the low voltage to satisfy safety requirements. Since battery input voltage is almost fixed, transformer primary and secondary is equal which in turn causes flat transformer current. Decreasing stress on the low and high voltage capacitors. It also leads to lower losses in the semiconductor switches, transformer, and capacitors.

3.1.1 DC-DC Circuit Selection

In general, there are two types of DC-DC converters: isolated and non-isolated. Usually, non-isolated DC-DC converters like buck, boost, buck-boost, and Cuk converter are used at low power applications. In the cases of distributed generation such as fuel cell or photovoltaic system, utilizing these types of converters will result in high cost and low efficiency. Moreover, in the circuit shown in Figure 26, isolation is needed. So this chapter mainly focuses on comparisons of isolated dc-dc converters. The general diagram of an isolated DC-DC converter is shown in Figure 26. For isolated DC-DC converters, forward, push-pull, half bridge and full bridge can be considered as topology candidates. In general, forward and push-pull converters are not suitable for high power applications. Forward converters have restrained duty cycles and lossy resetting of excitation; in push-pull converters, the two halves of a center-tapped winding cannot be equal or symmetrically wound, and the power switch on/off times as well as their forward voltage drops are never equal.

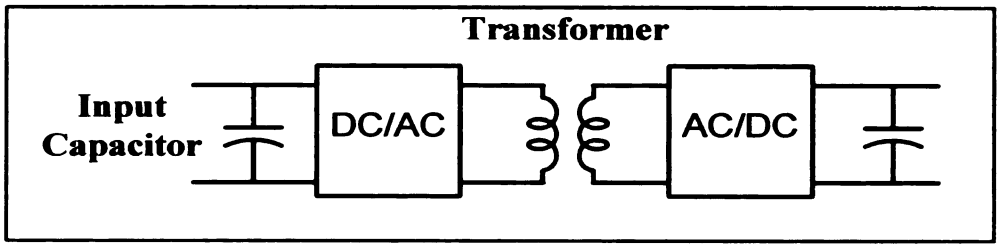


Figure 26 Isolated DC-DC Converter model

These irregularities, which exist in practice, can contribute to transformer core saturation and result in the converter failure. In both forward and push-pull converters, the voltage rating of the device is two times that of the half and full bridge. Though the full bridge, compared with the half bridge, has more components, the current in the devices and the transformer turns ratio can both be reduced to half. The current ripple in the front end capacitor is also minimized. The voltage and current stresses on the devices in the full bridge are the smallest in all of the four topologies. There are also several topology options for the secondary side of the DC-DC converter, such as diode rectifier, controlled rectifier, voltage doubler and controlled voltage doubler. All these four topologies have the same device voltage rating. For the secondary side, which is directly connected with the inverter module, the major concerns for the topology selection should be efficiency, cost, the resulted transformer turns ratio and power control flexibility.

Voltage doubler circuits will give smaller transformer turns ratio. But it will also lead to a large current ripple in the output capacitor. The current ripple will result in low efficiency, and possible overheat of the capacitor and reduced lifetime of the capacitors. So in the applications of distribute generation, a voltage doubler should only be used when the power is less than 10 kW. By using the active switches, there will be more flexibility in controlling the power flow and voltage. Active devices will also create more possibility

in the control the current waveforms over the transformer, thus the current stress on switches will be depressed. Furthermore experimental results also show that active control of the secondary side, in order to achieve a higher voltage transfer ratio than in the non-controlled case, will little lower the system efficiency.

3.1.2 Controlled Rectifier and Uncontrolled Rectifier

The circuit structures of controlled and non-controlled case are shown in Figure 27(1) and (2).

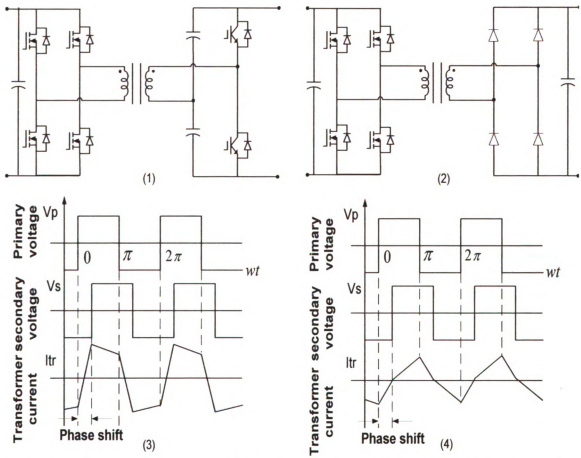


Figure 27 Two configurations of the secondary side in the isolated dc-dc converter

The correspondent voltages and current waveform over the transformer are shown in Figure 27(1) and (2). It is found that the voltage doubler and full bridge rectifiers yield the same voltage and current waveforms. The only thing that will make a difference in

the current and voltage waveforms is whether the secondary is controlled or not. So, the controlled voltage doubler and uncontrolled full bridge are shown in Figure 27(3) and(4), respectively.

A. Uncontrolled Rectifier

In uncontrolled case, θ is no longer controllable, the relationship between $\theta$and V_S, is found as

$$\theta = \pi \cdot \frac{V_P - V_S}{2 \cdot V_P} \tag{3.1}$$

where $V_P > V_S$.

The power transferred over the transformer and RMS value of the current are

$$P = \frac{1}{T}\int V_P \cdot I_S \cdot dt = \frac{(V_P{}^2 - V_S{}^2) \cdot V_S}{8 \cdot V_P \cdot f \cdot L_S} \tag{3.2}$$

$$I_{rms} = \sqrt{\frac{1}{T}\int_0^T i_s{}^2 dt} = \frac{\sqrt{3}(V_P{}^2 - V_S{}^2)}{12 \cdot V_P \cdot f \cdot L_S} \tag{3.3}$$

It can be seen that θ decides both the secondary side voltage, *Vs* , and the transferred power, P . For the diode rectifier, V_S cannot be equal to or larger than V_P, thus, the controllable ranges of output voltage and power are quite limited.

B. Controlled rectifier

In Figure 27, *Ls* is the leakage inductance of the transformer. The full bridge and voltage doubler are controlled to switch at high frequency to produce two square voltage waveforms with a phase shift, θ, as shown in Figure 27(3). The two square-wave voltages are impressed across the both sides of the transformer, respectively. So the current over the leakage inductance would look like the I_{tr} as shown in the Figure 27(3).

As I_{tr} is a function of wt, where w is the switching frequency, the current waveform can be analyzed as following: At 0 radian in Figure 27(3), the primary side voltage becomes positive while the secondary side voltage remains negative, creating a positive voltage across the leakage inductance making the current increase until $wt = \theta$, where the secondary voltage changes polarity from negative to positive. The current at this point can be written as

$$i_{tr}(\theta) = \frac{V_P + V_S}{wLs}\theta + i_{tr}(0),\ wt = \theta \tag{3.4}$$

where Vp and Vs are the amplitudes of the transformer primary side and secondary side voltage. With proper control, VS can be smaller, bigger or equal to Vp. The peak current will be minimized when $Vs = Vp$ is met.

At $wt = \pi + \theta$, the secondary side voltage becomes positive while the primary side voltage remains positive, making the voltage across the leakage inductance negative, allowing the current to decay until $wt = \pi$, where the primary voltage changes from positive to negative,

$$i_{tr}(\pi) = \frac{V_P - V_S}{wLs}(\pi - \theta) + i_{tr}(\theta),\quad wt = \pi \tag{3.5}$$

At this point, the primary side voltage becomes negative while the secondary side voltage remains positive, creating a negative voltage across the leakage inductance, making the current keep decreasing until $wt = \pi + \theta$, where the secondary voltage changes polarity again,

$$i_{tr}(\pi + \theta) = -\frac{V_P + V_S}{wLs}(\pi - \theta) + i_{tr}(\pi),\quad wt = \pi + \theta \tag{3.6}$$

After the secondary voltage changes polarity, the secondary side voltage becomes

negative while the primary side voltage remains negative, making the voltage across the leakage inductance positive allowing the current to increase to point 1, where

$$i_{tr}(2\pi) = -\frac{V_P - V_S}{wLs}(\pi - \theta) + i_{tr}(\pi + \theta), \quad wt = 2\pi \tag{3.7}$$

Because $i_s(\theta) = -i_s(\pi + \theta)$ and $i_s(\pi) = -i_s(2\pi)$, the exact relationship between the current and voltages can be found as equation (3.8) and (3.9) by solving equation (3.5)-(3.6)

$$i_{tr}(\theta) = \frac{2V_P\delta + (V_S - V_P)\pi}{2wLs} \tag{3.8}$$

$$i_{tr}(\pi) = \frac{2V_S\theta + (V_P - V_S)\pi}{2wLs} \tag{3.9}$$

From the representation of $i_s(wt)$, the power transferred through the transformer can be found as:

$$P = -\frac{1}{2} \cdot \theta \cdot V_P \cdot V_S \cdot \frac{(-\pi + \theta)}{(\pi^2 \cdot f \cdot L_S)} \tag{3.10}$$

Three conclusions can be made based on the Figure 27(3) and the equations obtained above. First, the power is transferred through the leakage inductance. Second, by controlling the phase shift of the voltages between the two sides of the transformer, the power transferred over the transformer as well as the secondary side dc voltage, *Vs* , can be precisely controlled. Third, if the system is controlled to have $Vs \approx Vp$, the current wave form would be rather flat, which means the peak current can be smaller. In summary, for the controlled rectifier case, the voltage angle difference, θ, and the secondary side voltage, *Vs* , are both controllable by properly coordinating the control of the primary side and secondary side. The power transferred over the transformer, P, can be variable at fixed secondary dc voltage, *Vs* . *Vs* can be equal to or larger than the

primary voltage Vp .

3.1.3 Isolated DC-DC Converter Control

The topology of the isolated dc-dc converter is shown in Figure 28. For isolated dc-dc converter, the primary side refers to low voltage side and the secondary side refers to high voltage side. And, forward power flow will be defined as from low voltage side to high voltage side. The primary and secondary voltages are fully controlled with a phase shift. So, the power transferred using this control strategy is given by the following equation.

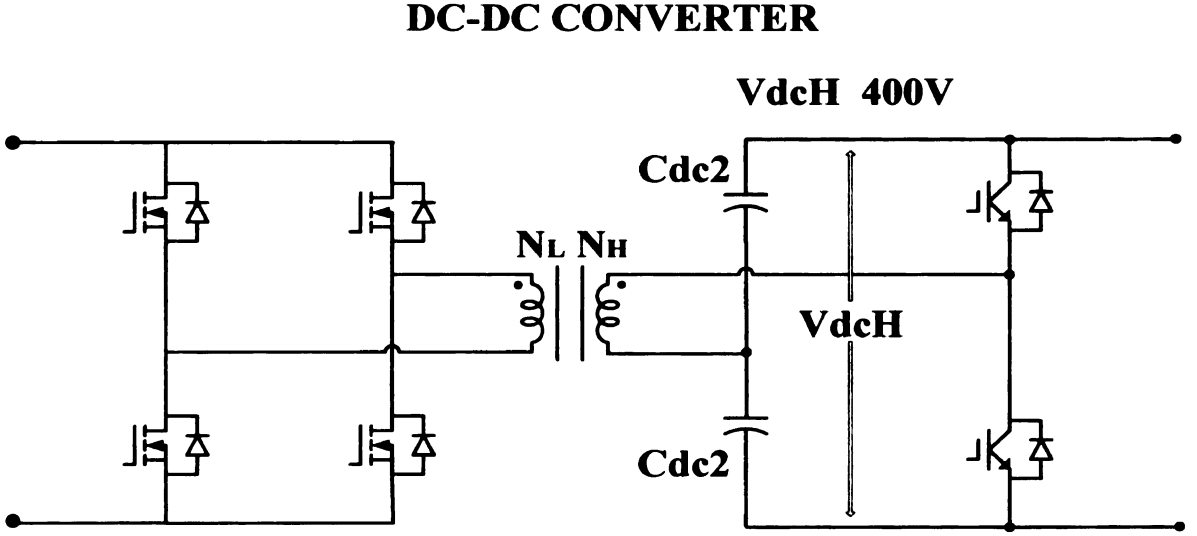


Figure 28 topology of the isolated dc-dc converter

$$P = \frac{V_{dcL}\left(\frac{V_{dcH}}{2n}\right)\cdot\phi\cdot(\pi-\phi)}{2\cdot\pi\cdot f_s\cdot L_s\cdot\pi} \tag{3.11}$$

Where ϕ is the phase shift angle of the secondary side, f_S is the switching frequency, L_S is leakage inductance of the transformer, n is turn ratio of transformer and V_{dcL}, V_{dcH} are low voltage and high voltage side of dc-dc converter. Based on (3.11), we can get

$$\frac{dP}{d\phi} = \frac{V_{dcL}\left(\frac{V_{dcH}}{2n}\right)\cdot(\pi - 2\phi)}{2\cdot\pi\cdot f_S\cdot L_S\cdot\pi} \tag{3.12}$$

$$\frac{dV_{dcL}}{d\phi} = \frac{P\cdot 2\cdot\pi\cdot f_S\cdot L_S\cdot\pi}{\left(\frac{V_{dcH}}{2n}\right)}\cdot\phi^{-2}(\pi-\phi)^{-1} + \frac{P\cdot 2\cdot\pi\cdot f_S\cdot L_S\cdot\pi}{\left(\frac{V_{dcH}}{2n}\right)}\cdot\phi^{-1}(\pi-\phi)^{-2}$$

$$= \frac{P\cdot 2\cdot\pi\cdot f_S\cdot L_S\cdot\pi}{(\frac{V_{dcH}}{2n})}\cdot\frac{2\phi-\pi}{\phi^2(\pi-\phi)^2} \tag{3.13}$$

$$\frac{dV_{dcH}}{d\phi} = \frac{P\cdot 2\cdot\pi\cdot f_S\cdot L_S\cdot\pi}{\left(\frac{V_{dcL}}{2n}\right)}\cdot\phi^{-2}(\pi-\phi)^{-1} + \frac{P\cdot 2\cdot\pi\cdot f_S\cdot L_S\cdot\pi}{\left(\frac{V_{dcL}}{2n}\right)}\cdot\phi^{-1}(\pi-\phi)^{-2}$$

$$= \frac{P\cdot 2\cdot\pi\cdot f_S\cdot L_S\cdot\pi}{(\frac{V_{dcL}}{2n})}\cdot\frac{2\phi-\pi}{\phi^2(\pi-\phi)^2} \tag{3.14}$$

Since the phase shift varies in the range of (0 , $\frac{\pi}{2}$) under forward power flow, thus

$$\frac{dP}{d\phi} > 0 \tag{3.15}$$

Considering (3.12), a phase shift increase causes a transferred power increment. We have to use isolated dc-dc converter to keep the 400V high voltage side (HVS) dc link voltage constant if the whole system works on stand-alone state. Here, this situation is considered firstly. Now, let us consider the dc voltage over capacitors *Cdc2* which is inverter dc link capacitance. Generally, the voltage of the *Cdc2* will increase when the input power (*Pin*) is larger than output power (*Pout*). This means the voltage of the *Cdc2* variation indicates power change or the difference between *Pin* and *Pout*. So, the voltage control loop can be used to substitute the power control loop. Figure 29 shows the control

scheme of isolated dc-dc converter when working on stand-alone state (forward power flow). Here, dc-link voltage *VdcH* is feedback to obtain the phase shift to control the power from primary side to secondary side. The dc-link voltage reference will be about 400 V. The isolated dc-dc converter will carry out the different control strategy in the situation where the whole system is working on grid-connected mode. Because the HVS dc link voltage V_{dcH} can be controlled by the inverter which will be discussed later, the isolated dc-dc converter just need control the penetrating power by adjusting phase shift angle between the full-bridge legs and the voltage doubler leg.

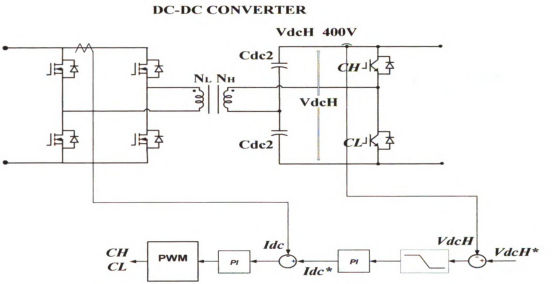


Figure 29 Control scheme for isolated dc-dc converter

Figure 30 shows power transfer curve of utilizing leakage inductance of transformer. Since transformer leakage inductance is too small that we added additional leakage inductance with 11uH. By adding this leakage inductance, we can realize more stable control. Deriving from power transfer formula, we can transfer 1kw power at the 10usec phase shift delay between low voltage side and high voltage side. If primary referred to secondary voltage is negative, which is negative phase shift, power is transferred from

secondary side to primary side. By giving Phase shift control, we can control power either forward or backward direction.

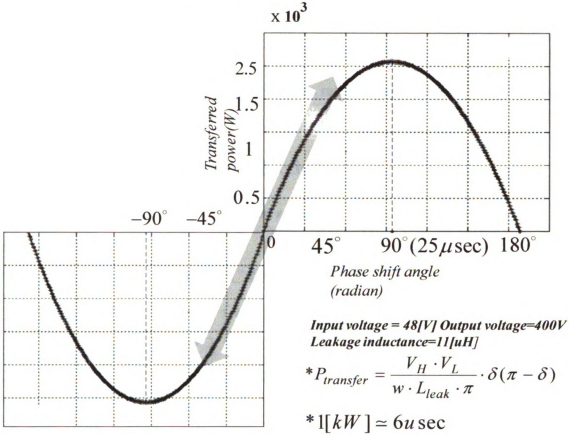


Figure 30 Power transfer curve of utilizing leakage inductance

3.2 Design and Development of DC-DCFull-Bridge Converter

3.2.1 Turns Ratio Selection of Transformer

The dc-dc converter stage is a typical dual-active-bridge dc-dc converter. The LVS full bridge generates a square-wave voltage applied to the primary of the transformer, and the HVS half bridge also generates a square-wave voltage applied to the secondary of the transformer. Phase shift control and duty cycle control can be applied to obtain desired performance. The current waveform is determined by the phase shift and voltage

relationship of *VdcL* and *VdcH*. The current through transformer and switches would have minimum peak when the voltages of primary and secondary are almost same in primary side (or secondary side) referred. The high voltage *VdcH* is almost constant (400 V) but the low voltage *VdcL* is 48[V]. In order to decrease the current spike, the turns ratio is selected between 48/200. Here, the turns ratio is fixed at 1:4 (*Nl* : *Nh*) with using voltage doubler circuit.

3.2.2 Leakage Inductance Selection

Figure 31 shows the equivalent circuit referred to LVS of dc-dc converter.

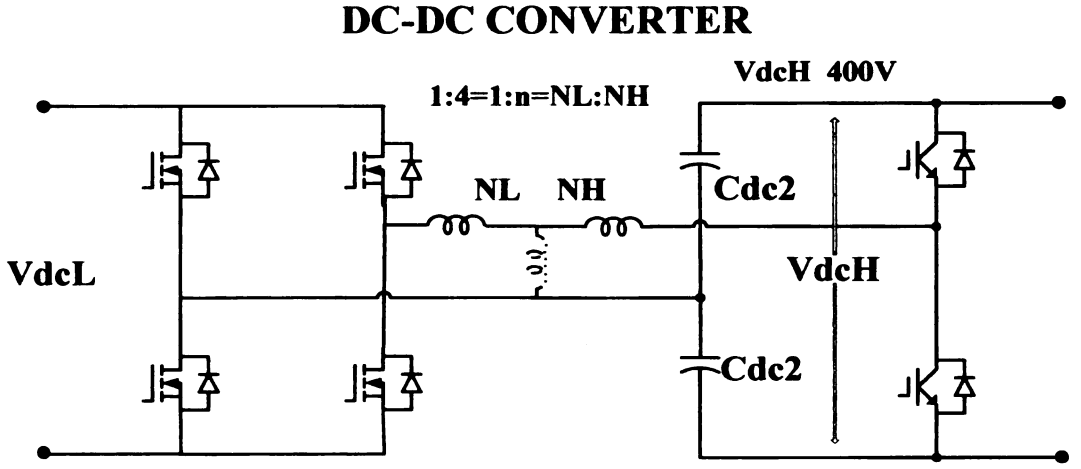


Figure 31 Simplified equivalent circuit referred to the primary(low voltage side)

If only phase shift control is applied, the amount of power transferred through the transformer can be calculated as

$$P = \frac{V_{dcL}(\frac{V_{dcH}}{2n}) \cdot \phi(\pi - \phi)}{2\pi f_S L_S \pi} \tag{3.16}$$

where ϕ is the phase shift between the two square voltage waveforms generated by the

LVS bridge and HVS bridge, respectively, f_s is the switching frequency, L_s is leakage inductance of the transformer. Suppose the maximum power through transformer (dc-dc converter) is P_{max}, the expected phase shift angle at P_{max} is ϕ,the Ls can be computed as

$$L_S = \frac{V_{dcL}(\frac{V_{dcH}}{2n}) \cdot \phi(\pi - \phi)}{2\pi^2 f_S P_{\max}} \tag{3.17}$$

So, the leakage inductance Ls shall not be greater than $L_{s,\max}$ when phase shift is $\pi/2$ and V_{dcL} is minimum.

$$L_{s,\max} = \frac{V_{dcL}(\frac{V_{dcH}}{2n})}{8 \cdot f_S P_{\max}} \tag{3.18}$$

If the switching frequency is 10 kHz, Pmax is 2 kW, then

$$L_{s,\max} = \frac{48 \cdot (\frac{400}{2n})}{8 \cdot 1 \cdot 10^4 \cdot 2000} = \frac{60uH}{n} = 15uH \tag{3.19}$$

Here, the leakage inductance of the transformer is selected as 11 μH. And then

$$V_{dcL} = \frac{L_S \cdot 2\pi^2 \cdot f_S \cdot P_{\max}}{(\frac{V_{dcH}}{2n}) \cdot \phi(\pi - \phi)} = \frac{86.85}{\phi(\pi - \phi)} \tag{3.20}$$

Thus, $\phi = 0.78$ when VdcL = 48 V

3.2.3 Core and Winding Selection

The selected core for the transformer is Powerlite C core from Metaglas. The most benefit from this core is ultra low power loss. The core has very high saturation flux

density. Like inductor, the high-frequency transformer can also be designed using area product (*Ap*) approach. Firstly, *Ap* is calculated as

$$Ap = \frac{P_O C \cdot 10^8}{4\eta B f K_u} = \frac{KP_O}{Bf} = \frac{0.00528 \times 2000 \times 10^8}{2000 \times 10 \times 10^3} = 52.8(cm^4) \tag{3.21}$$

Where $K = 0.00528$ for E-U-I core, P_O is the output power in (W), C (= $1/J$) is current capacity in (cm^2 / A) which is the reciprocal of current density, η is transformer efficiency, B is flux density in (Gauss), f is operation frequency in (Hz), and K_u is winding factor. Here, we assume η = 90% for transformer. Secondly, the E core is selected from Magnetics Inc. 3 pairs of E cores are used to reduce number of turns. Selected core area product $Ap = 55.7[cm^4]$, core area $A_{core} = 3.92[cm^2]$ and window area $A_W = 8\ [cm^2]$. In order to reduce the core loss, the magnetic flux density should be small. Here, it is 2000 Gausses. Then the number of HVS turns, *NHVS* can be calculated using Faraday's Law.

$$N_{HVS} = \frac{V_{\sec} \times 10^8}{K_f B A_{core,eff} \times f_O} = \frac{200 \times 10^8}{4 \times 2000 \times 3 \times 3.92 \times 10^4} = 21.25 \text{ use } 16(\text{turns})$$

$$N_{LVS} = \frac{1}{n} \cdot N_{HVS} = \frac{1}{4} \times 16 = 4(turns) \tag{3.22}$$

We could chosen $N_{HVS} = 20$ but that would have made $N_{HVS} = 5$,which means that the secondary would probably either be a single section of 5layers or 5section of 1layer. This would have greatly reduce the flexibility in designing a sectionalized transformer winding.

The core loss per unity volume at B=0.2362T is

$$P_{L,R} = a \cdot f^c B^d = 0.074 \times 10^{1.43} \times 2.362^{2.85} = 23(mW/cm^3) \qquad (3.23)$$

The actual total core loss is $P_{core} = P_{L,R} \cdot V_e = 23 \times 48 \times 4 = 4.4(W)$ .The ac resistance of LVS winding and dc resistance of HVS will be very large if there are just one primary section(with 4 layers) and one secondary section(with 16 layers). So the transformer winding should be reselected and rearranged. Generally, the transformer winding can be interleaved to reduce power loss. The 4 LVS layers(turns) are split into 2 sets of 2 layers.And the 16HVS layers are divided into 3section,with the central section having 8 layers and the outer two section having 4 layers. Window length is about 5.6cm, we selected standard copper foil with standard width of 5.08cm. The resistance per turn of the windings in bout HVS and LVS shown in following equation.

$$r_{HVS@0.01"} = \frac{\rho \cdot MLT}{A_{CU,HVS}} = \frac{2.2 \times 10^{-6} \times 33}{5.08 \times 0.0254} = 5.63 \times 10^{-4}(\Omega/turn)$$

$$r_{LVS@0.021"} = \frac{\rho \cdot MLT}{A_{CU,LVS}} = \frac{2.2 \times 10^{-6} \times 33}{5.08 \times 0.0533} = 2.68 \times 10^{-4}(\Omega/turn) \qquad (3.24)$$

Where 0.01" is thickness of copper foil at high side voltage and 0.021" is thickness of low side voltage. MLT is mean length per turn and A_{CU} is copper foil width times copper foil thickness. The equivalent resistance in both HVS and LVS is

$$R_{HVS@0.01"} = r_{HVS} \times (1.1 \times 8 + 1 \times 8) = 5.63 \times 10^{-4} \times (1.1 \times 8 + 1 \times 8) = 9.45 \times 10^{-3}(\Omega)$$
$$R_{LVS@0.021"} = r_{HVS} \times 1.2 \times 4 = 2.68 \times 10^{-4} \times 1.2 \times 4 = 1.286 \times 10^{-3}(\Omega) \qquad (3.25)$$

The total copper power loss is $P_{CU@0.021"+0.01"} = I^2_{HVS} R_{HVS} + I^2_{LVS} R_{LVS}$

$$= 10.5^2 \times 9.45 \times 10^{-3} + 42^2 \times 1.286 \times 10^{-3} = 3.31[W] \qquad (3.26)$$

We consider of 1.5 for our application. So the modified total copper power loss is

$$P_{CU}@0.021"+0.01" = 1.5P_{CU} = 1.5 \cdot 3.31 = 5[W]$$

Total loss from calculation would be following value.

$$P_{total} = P_{core,loss} + P_{cu,loss} \cong 10[W] \tag{3.27}$$

Figure32 shows the transformer with 230 uH magnetizing inductance and 0.1 uH leakage inductance. This small leakage inductance may cause some problem in controlling the power transfer. Small leakage inductance can cause unstable power transfer to high voltage side which brings controller to be more sensitive to feedback system. Therefore, we made additional inductor beside transformer to achieve higher leakage inductance with 11 uH . Our system needs to transfer maximum 2KW from dc to ac side. Leakage inductance with additional wire satisfy enough margin to control the power flow of dc-dc converter.

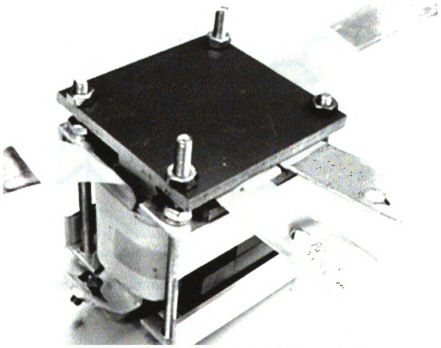


Figure 32 DC-DC converter transformer design

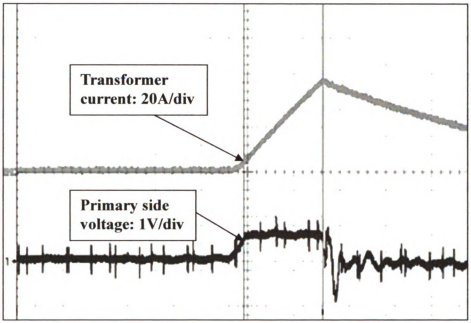


Figure 33 Transformer short circuit test (leakage inductance test)

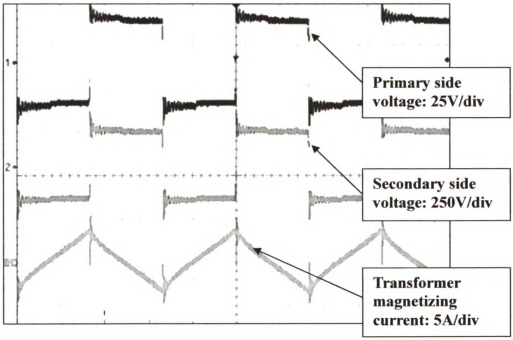


Figure 34 Transformer open circuit test (magnetizing current)

3.2.4 Device Selection

The maximum voltage across the switches on LVS is the open-circuit voltage (50[V]) of DC-DC buck converter. The voltage rating of the switch should not be less than it. The voltage rating of the switches on LVS is selected at 150 V. The maximum voltage across the switches on HVS is the dc-link voltage of 400 V. So the rated voltage of the switch on HVS is selected as 600 V. As analyzed above, the maximum peak current through the switches of LVS is 58.7[A] occurring at $V_{dcL} = 48[V]$. The peak current through HVS switches is *Ip(HVS)* =58.7/4=14.67[A]. The current rating of the switches is at least 1.5 ~ 2 times the peak current. So, 2 MOSFET modules are selected for LVS full-bridge and two MOSFET are paralleled per switch. And a 600-V/75-A IGBT-IPM is selected for HVS half-bridge.

3.3 Simulation & Experimental Result

3.3.1 Simulation Result

From Figure 35,before turning on the inverter, dc-dc converter charging the capacitor on the high voltage side before it reaches 0.5 sec. Turning on the inverter at 0.5sec, voltage on the high side drops suddenly, then turn into stable voltage after controller start to get reference voltage of high side. From Figure 36, after charging the high side voltage up to 360[V], Phase angle keeps almost zero in order to block current from dc side. After turning on the inverter phase is keeping constant phase angle in order to transfer the power that load needs as shown in Figure 37. When load(80Ω) is connected, 5A output current is flowing.

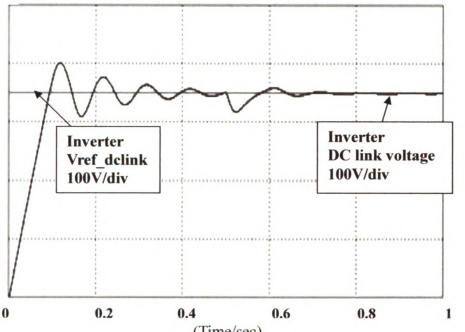


Figure 35 DC-DC High side voltage & voltage reference

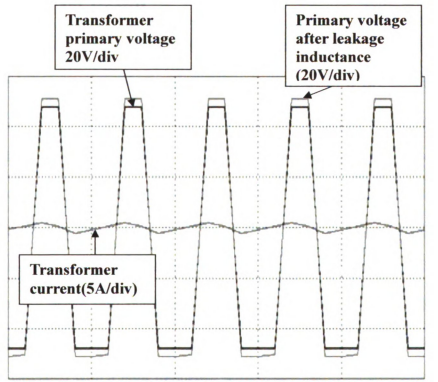


Figure 36 Transformer Primary voltage & Secondary voltage before turning on the inverter

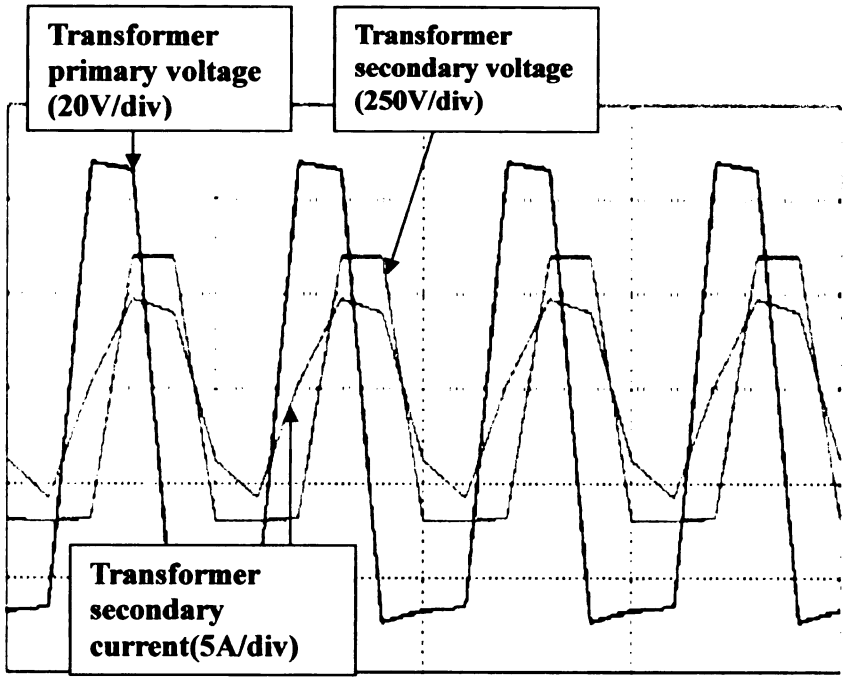


Figure 37 Transformer voltage & current after turning on inverter

3.3.2 Experimental Result

Experimental results of 2 kW DC-DC converter is shown in Figure 38 and 39. In the experiment, the input power to the dc-dc converter is supplied by a 48V dc source. The transformer turns ratio is 1:4. The secondary side is a voltage doubler with two IGBTs which is one phase part of 3phase IPM. The DC-DC converter is connected to a inverter module. Before turning on the inverter, two phase leg of IPM(inverter side) is not switching while the one phase leg of IPM(dc-dc converter side) is using free wheeling diodes to establish 400V in dc-link. Once ac load is installed, one phase leg of IPM start to switching for the phase shift purpose, (secondary side voltage refer to primary side voltage) transferring power to ac load through inverter. It can be concluded that the full bridge inverter cascaded with a high frequency transformer and controlled switch would be the optimized circuits for the isolated DC regulator in the PV inverter system. The

controlled rectifier has a larger controllable output voltage and power range. In Figure 39 and 40, the phase shifting of the voltages over the transformer is clearly shown; the transformer current is not exactly flat. This reason is coming from voltage difference between leakage inductance is exsiting. In Figure 39, the secondary side voltage is 405V, which is little bit higher than desired reference voltage. The primary side voltage is 48 V. This two voltages shows an equivalent boost ratio of 8.43, whereas the transformer turns ratio is only 1:4 with voltage doubler. This verifies that the high side voltage can be further boosted and precisely controlled by adjusting the phase shift angle.

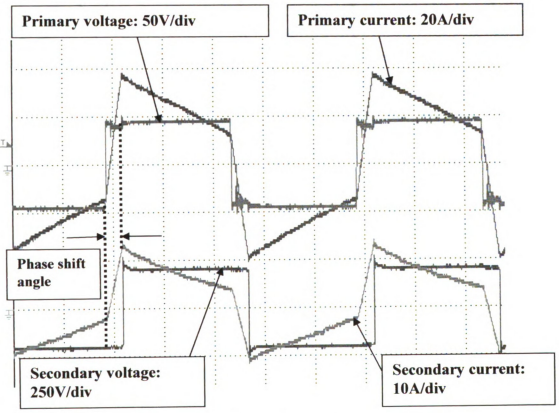


Figure 38 the experimental result of the dc–dc converter.

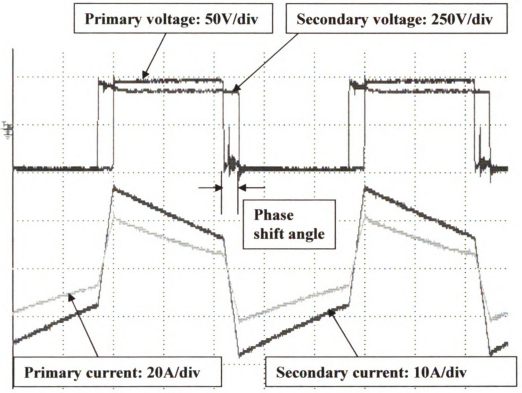


Figure 39 the experimental result of the dc–dc converter.

Chapter 4

4.1 Inverter Design

4.1.1 Overall Inverter Configuration

The inverter circuit converts a DC input (as would commonly be from a distributed energy source after proper conditioning) into a grid-suitable AC output. The DC input voltage is nominally 400 V ± 5%. Conversion is done by a power electronics bridge circuit that operates to produce a pulse-width modulation (PWM) AC output, which for this model will be nominally 240 V AC. To allow a seamless transition between utility connected mode and stand-alone mode, the inverter must transition its operations from current control to voltage control. The power circuit can be divided into four essential parts: (1) DC input stage; (2) bridge stage; (3) AC filter stage; and (4) utility stage. A number of small resistances are included throughout the model to make the model more realistic and to facilitate convergence of the model in experiment. To meet the requirement of the single-phase utility grid, the dc-ac inverter stage is realized using a three-leg PWM converter. It is connected to the utility grid through the LC filter. Here, they are termed as the grid-tied-VSC. It is noticed that the dc-ac inverter stage shares a common two-switch leg with the dc-dc converter stage. There are two states for the dc-ac inverter stage: when injecting real power into the grid, the PWM converter is operated as a single-phase PWM inverter to transform the dc voltage into ac voltage. When absorbing real power from the grid, the PWM converter is treated as a single-phase PWM rectifier to transform the ac voltage into dc voltage. Although the ac load power is about 2 kW, the capacity of the grid-tied-VSC is near 2 kW since the PV power is only about 1kW

and the dc load is about 1 kW. Actually, the capacity of the grid-tied-VSC just need be designed to match the demand of the dc load or PV power production. According to the specification, the battery is only charged by PV. Here, we suppose the battery has the same power of 1 kW as the dc load. So, for the grid-tied-VSC, the extreme case is that both of PV and battery supply to the ac load when the dc load are not in operation. That is, the grid-tied-VSC should transmit 2 kW power from dc side (1 kW from PV and 1 kW from the battery) to the ac grid at the extreme case. However, in order to ensure the unity of the AC input power factor of the gateway grid unity, the grid-tied-VSC may need work as a VAR compensator. Consider the worst case when the inverter needs to compensate the 2 kW ac load from the power factor of 0.7 to nearly 1. Plus, it still supplies 1 kW active power to the ac load if no dc load absorbs power from the PV. The required apparent power is:

$$S = \sqrt{1^2 + \left(\frac{2}{0.7} \times \sqrt{1 - 0.7^2}\right)^2} = \sqrt{1^2 + 2.03^2} = 2.27[kVA] \tag{4.1}$$

If the ac grid is temporarily unavailable and PV and battery is designed to support the load as they can. Assuming the condition that the 2 kW is all consumed by the ac load, the maximum apparent power passing through the inverter can be:

$$S = \frac{2kW}{0.7} = 2.85[kVA]$$

Based on the above two cases, the capacity of the grid-tied-VSC is designed as 2.5[kVA] and LC filter is adopted in the grid-tied-VSC. Given that the nominal output voltage (utility grid voltage) V_{oac} = 240 V, the maximum voltage = 252 V and the minimum voltage is 220 V. So the nominal output current I_o = 2 kW/240 V = 8.3 [A], maximum

output current is $I_{o,\max}$ =2 kW/220 V=9.09[A]. And the dc-link voltage (input voltage) should be selected as V_{indc}=400V. For the grid-connected PV system, the total harmonic current distortion at the point of common coupling (PCC) shall be less than 5% of the fundamental frequency current at rated output. So, how to design the LC filter is a very important issue.

4.1.2 DC Input Stage

The inverter is designed to accommodate a DC input from a 400 V DC source. In the model, the input consists of a controlled DC voltage source. The design also incorporates an input filter capacitor of 1500[uF] to reduce input voltage disturbances.

DC-link capacitor (Cdc2) selection

The dc-link capacitance is selected to guarantee that the 2nd harmonic is controlled below 1% of the rated dc voltage. So

$$\frac{C_{dc2}}{2} \geq \frac{m^2 \cdot I_{oac}}{4w_o \cdot \sqrt{2} \cdot V_{odc} \cdot 1\%} = \frac{V_{oac} \cdot I_{oac}}{4w_o \cdot \sqrt{2} \cdot V_{odc} \cdot 1\%}$$

$$= \frac{240 \times 8.3}{2\sqrt{2} \times 2\pi \times 60 \times 400^2 \times 1\%} = 12.67 \times 10^{-4} = 1267[uF] \qquad (4.2)$$

As stated in previous section, the dc-link capacitance must be designed taking into account that: during the delay time of the voltage control loop, the output power demand must be sustained by the dc-link capacitor energy. Hence the value of dc-link capacitance turns out to be:

$$C_{dc2} \geq \frac{T_r \Delta P_{\max}}{2 V_{indc} \Delta V_{indc,\max}} \tag{4.3}$$

where response time Tr of the voltage control loop, is in the order of a few modulation periods; $\Delta Pmax$ is maximum expected variation of the output power. Give that $Tr = 10Ts$ = 1 ms, $\Delta Pmax$ = 2.0 kW, voltage ripple below 1%, then

$$C_{dc2} \geq \frac{10^{-3} \times 2000}{2 \times 400 \times (400 \times 1\%)} = 12.25 \times 10^{-4} (F) = 1225[uF] \tag{4.4}$$

4.1.3 Bridge Stage

The bridge stage is made up of IPM that are controlled using a unipolar switching scheme. In a unipolar switching scheme, each leg of the bridge is controlled as a separate pair. The two switches in each pair are controlled in a complimentary fashion. In other words, when the top switch in a leg is closed, the bottom is open, and vice versa for the next switching interval. The control for each leg of the bridge is accomplished by comparing a control signal (on A) with a triangular waveform (sig1). This results in the following logic signals being applied to the gates of the IPM (using leg A as an example):

on A < sig1 : A1 on and A2 off

on A > sig1 : A1 off and A2 on

The control signal (on B) for the B leg is the negative of on A, but is compared to the same triangular waveform (sig1). This is shown below in Figure 40 with the frequency of triangular waveform significantly reduced for illustrative purposes.

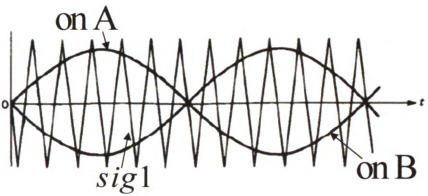


Figure 40 Relationship between A and B leg control signal
& triangular carrier waveform

This results in the following gate signals being applied to the leg B IPMs:

On B (or –on A) < sig1 : B1 on and B2 off

On B (or –on A) > sig1 : B1 off and B2 on

Figure 41 illustrates the results of this switching scheme for leg A. The bottom graph shows the comparison of the control signal with the triangular waveform and the other two graphs show the control logic being applied to the IPM gates. The IPM switches are closed when their logic inputs are high.

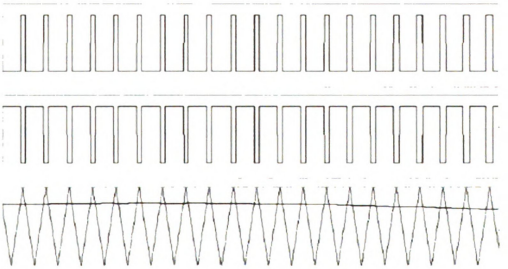


Figure 41 . PWM Switching Scheme for leg A of inverter

When on A is less than sig1, A1 is commanded on (top graph) and A2 is off (middle graph). The opposite also holds true, as shown. Combining the effects of switching the A and B legs in this manner results in four output voltage states:

A1, B2 on : output = DC input

A2, B1 on : output = -DC input

A1, B1 on : output = 0

A2, B2 on : output = 0

Notice that when either both the top or both the bottom switches are on at the same time, the output is zero and current flows through the forward biased diodes. Controlling the IPMs in this manner generates an output with an average that follows the control signal on A. Moreover, as long as the frequency of the control signal is much smaller than that of the triangular waveform, the output can effectively be a scaled mirror of the control signal. Thus, a controlled inverter output can be achieved by precisely controlling the signal on A.

The on A signal is either generated using a sine function (with variable magnitude, phase, or frequency components) or by a comparator output depending on whether the inverter is in current or voltage control mode. Details on these modes and how they affect on A are discussed in the next subsection. The result of this switching scheme is illustrated in Figure 42 which shows the PWM positive and negative pulses in green and red, respectively, along with their average values traced in blue showing it to be a sinusoidal signal. Another thing to note is that the actual hardware used for the IPM bridge stage can be configured to operate as either a single phase inverter or a three phase inverter, as they actually consist of six IGBTs.

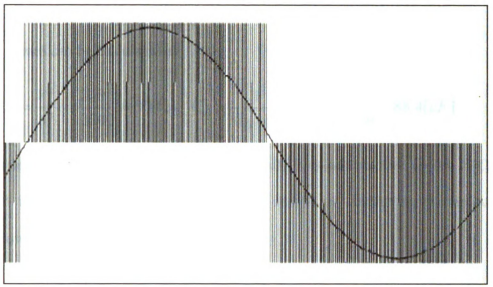


Figure 42 Combined PWM Switching for inverter

During single-phase inverter operations, two of the six switches are not the part of inverter operation but these switches operate as phase shift function with full-bridge converter in the isolated DC-DC converter.

4.1.4 AC Filter Stage

The bridge output goes into the filter stage, which contains the energy storage elements necessary for circuit operation. The 2mH inductors and parallel, 7.5uF capacitors are sized in order to achieve desired voltage and current ripple characteristics. The output is a single phase, 60 Hz, 240 V AC waveform. PV system has certain source referencing (grounding) requirements for voltage and current sources that need a ground on the negative side of the input DC voltage. This arrangement does not accommodate utility grounding, therefore improper current paths are created. To prevent this from affecting the modeling performance, an ideal 1:1 turns ratio transformer is placed on the output. Actual system hardware implementation will not include this transformer.

Inductance and capacitance selection of LC filter

The base values can be calculated as

$$R_b = \frac{V^2}{P} = \frac{240^2}{2000} \approx 30[\Omega],\ \ C_b = \frac{1}{w_o \cdot R_b} = \frac{1}{2\pi \cdot 60 \cdot 30} = 88.4[uF] \tag{4.5}$$

The selection of filter capacitance *Cf* is a trade-off between reactive power in *Cf* and equivalent inductance *Lf*. Filter capacitance *Cf* should be limited by the amount of reactive power absorbed in the capacitor.

$$\left(\frac{C_f}{2}\right) \le 0.1 \cdot C_b \rightarrow 2 \times 0.1 \times 88.4 = 17.68[uF] \tag{4.6}$$

Firstly, the inductance *Lf* is chosen to limit the ripple at the VSC output current to 10% of the rated amplitude value. For the filter inductance design, the VSC can be treated as a buck converter at the switching frequency. So, we know

For unipolar PWM

$$\left(2L_f\right) \ge \frac{V_{oacm}}{2 \cdot \Delta i_{Lf,\max}} \cdot \frac{V_{indc} - V_{oacm}}{V_{indc} \cdot f_s} = \left\{ \frac{V_{indc} - V_{oacm}}{2 \cdot \Delta i_{Lf,\max}} \cdot D \cdot \frac{1}{f_s} \right\} \tag{4.7}$$

For bipolar PWM

$$\left(2L_f\right) \ge \frac{V_{indc} + V_{oacm}}{2 \cdot \Delta i_{Lf,\max}} \cdot \frac{V_{indc} - V_{oacm}}{2 \cdot V_{indc} \cdot f_s} = \left\{ \frac{V_{indc} - V_{oacm}}{2 \cdot \Delta i_{Lf,\max}} \cdot D \cdot \frac{1}{f_s} \right\} \tag{4.8}$$

For a switching frequency of 10 kHz, the filter inductance *Lf* must be no less than

$$\left(2L_f\right)_{for\ \text{unipolar}} \ge \frac{240 \times \sqrt{2}}{2 \times 13.3 \times \sqrt{2} \times 10\%} \cdot \frac{400 - 240 \times \sqrt{2}}{400} \times \frac{1}{10^4} = 1.367[mH]$$

$$\left(2L_f\right)_{for\ \text{bipolar}} \ge \frac{(400 + 240 \times \sqrt{2})}{2 \times 11.5 \times \sqrt{2} \times 10\%} \cdot \frac{400 - 240 \times \sqrt{2}}{2 \times 400} \times \frac{1}{10^4} = 1.82[mH]$$

On the other hand, the inductance should not be selected too large to meet the demand of the current tracking capability and the demand of the power transmission.

$$L_f \geq 910.5[uH]$$

Through out numerous experiment, Lf is selected as near 2 [mH] to make smooth ac sinusoidal wave form. The resonant frequency if LC is

$$f_{res} = \frac{1}{2\pi\sqrt{L_f C_f}} = \frac{1}{2\pi\sqrt{2\times10^{-3}\times7.5\times10^{-6}}} = 1.29[kHz]$$

The resonant frequency is in the range nearly between twenty times the line frequency and about one-tenth of switching frequency. The utility stage consists of a 240 V AC source and a circuit breaker. The breaker is controlled with on/off switch facilitate opening and closing during a simulation run. The utility source is a constant magnitude, frequency, and phase AC source with some nominal series impedance. The state of the breaker is represented by switching between logic level 0 or 1, depending on whether the breaker is open (0) or closed (1).

4.2 Inverter Control Methodology

4.2.1 The Overall Inverter Control

The basic inverter controls can be broadly classified into two types: current control and voltage control. When the inverter is connected to the utility, the grid controls the amplitude and frequency of the inverter output voltage and the inverter itself operates in the current control mode. Other types of inverter controls such as power flow control and VAR/voltage control can be derived from the basic current control. In contrast, in case of

grid failure (grid faults, maintenance, etc.), the connected loads have to be supplied by the inverter. In such a scenario, which is often referred to as islanded operation, the inverter has to maintain the amplitude and the frequency of the voltage so that the connected loads are not affected by the utility interruption. The inverter operates in voltage control mode for such scenario providing the reference voltage and frequency. For inverter, forward power flow will be defined as from the dc-link. In the stand-alone mode where the inverter is only connected to passive loads, the inverter shall control the output ac voltage (*Va* and *Vb*) constant. The laboratory hardware setup consists of several components as shown in Figure 43: inverter power and control circuits, DC voltage source, utility grid, resistive-inductive-capacitive (RL) load bank, and electronic load bank.

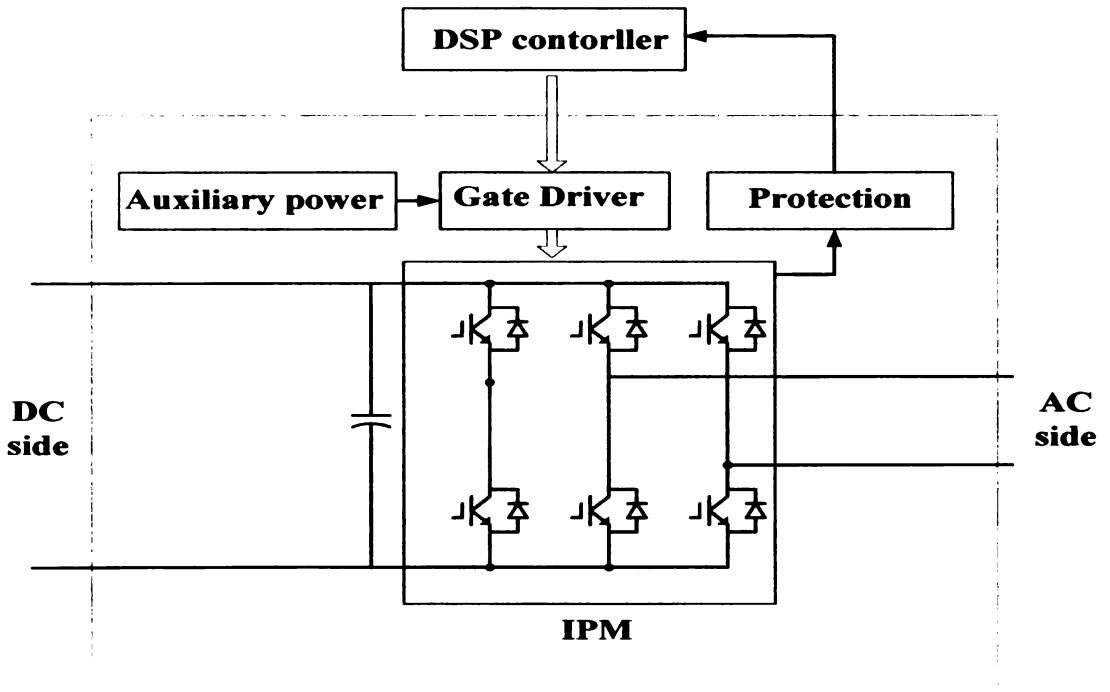


Figure 43 Inverter control system

Powerex Intelligent Power Modules (IPMs) are advanced hybrid power devices that combine high speed, low loss IGBTs with optimized gate drive and protection circuitry. 3phase,75A/600V IGBT type inverter and has monolithic gate drive & protection logic. Detection, protection, status indication circuits for short circuit, over-temperature and under-voltage is performed. The DC bus filter capacitor, voltage and current sensors, auxiliary power supply, and gate drivers are on a common heat sink. An external DSP is selected for this particular design to have more flexibility.

The control board is designed with a DSP 2407 which contains the TMS320F2407 DSP by Texas Instruments. To simplify code development and shorten debugging time, a C2000 Tools Code Composer Studio (Texas Instruments) driver is provided. The inputs to the control board are DC bus voltage, phase currents and fault signals from the PV system. Voltage and current measurement signals from the external sensors and mode selection and startup signals from the external central processing unit (CPU). The main outputs of the control board are the gate drive PWM signals for the PV system. Additionally, the control board also provides enabling signals for the PV system, PWM status signals to the external CPU. The local controller is designed to provide control and communication functions for the associated gate signal. As the DSP module has sufficient calculation power, we preferred to carry out all control calculations inside the local controller in addition to the PWM generation for the switches. The control board has 2 main input port for sensing voltage and current from those sensors. The power is supplied to the control board by an external AC/DC converter that converts 240V, 60 Hz AC into 15/48V DC. The signals from the voltage and current sensors are fed directly into the control board, as it has several voltage and current conditioning systems that

convert the measured voltage/current into DSP input compatible quantities. The connection between the PV system and DSP is obtained using a D-sub 25 pin connector with ribbon cable. The higher level controller in the CPU is currently connected to the DSP board through JTAG-compatible parallel port. An annotated picture of the control board is shown in Figure 44.

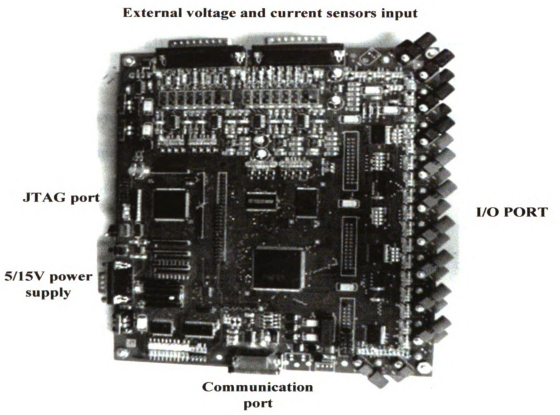


Figure 44 Picture of control board with input/output connection

Initially the DSP code was written in C programming language with TI's Code Composer Studio–all the results that are presented in this section are obtained using these C-based control codes. The C codes were compiled and loaded into the DSP on-chip random access memory (RAM) using Code Composer Studio. Then the controller was activated using the serial interface. The program code is interrupt driven and runs at a

fixed sampling frequency of 10 kHz based on the interrupt set up. For the inverter platform, the switching frequency was set at 10 kHz. Therefore, the service routine ran once in each PWM cycle and was used to compute duty cycles for the next cycle.

4.2.2 Voltage Control

For the voltage control mode, the IPM switches are controlled using biipolar pulse-width modulation (PWM) switching such that the inverter output voltage follows the reference voltage. The voltage control loop block diagram is shown in Figure 45. The voltage control system consists of a negative feedback loop containing a proportional integral (PI) compensator We compared the actual voltage to the reference signal and the error was then fed to a proportional controller. In this case the reference value is unity, as it is assumed that utility voltage is constant. The output of the controller was then scaled and added to a feed forward loop. Then V_{ref} signal is fed to the gate driver block where it is compared with a triangular waveform to determine the duty cycle. As V_{ref} increases, the average duty cycle of the gate driver circuit also increases raising the average output voltage of the inverter. The final output of the controller is a duty cycle value (D), as given by equation.

$$D = \left(0.5 + \frac{V_{ref}}{2 \times V_{dc}}\right) + \frac{K_v \times (V_{ref} - V_{inv})}{2 \times V_{dc}} \tag{4.10}$$

where, V_{ref} is the reference voltage, V_{inv} is the inverter output voltage, V_{dc} is the input DC voltage and K_v is the proportional gain. The initial gains of the compensator are determined using the Ziegler-Nichols Oscillation method. Further tuning is achieved

by performing multiple simulations of several scenarios. Best performance is observed when the Kp=0.3 and Ki=0.1 values. Duty cycle, D, is computed and then compared to a 10kHz triangular wave to generate a 10kHz PWM switching signal with positive duty cycle of D. Based on the PWM switching pattern, IPM switches are turned on and off in a bipolar fashion, such that two diagonally opposite switches in the H-bridge turn on and off simultaneously.

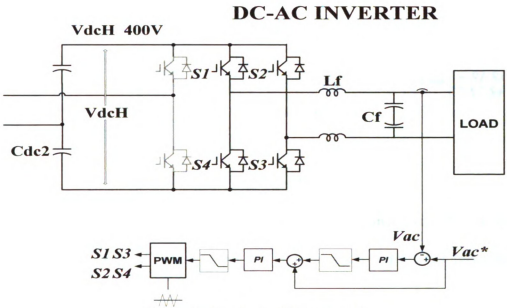


Figure 45 Inverter voltage control

4.2.3 Current Control

In the utility-connected mode, the inverter operates as a current-controlled source to generate an output current based on a reference current signal. The inverter shall not actively regulate the voltage at the PCC (point of common coupling). So, in the grid-connected mode, the inverter does not control the output ac voltage but control the output current (or output power). And at the same time, DC-DC converter should also keep the dc-link voltage constant. When the inverter is utility connected mode, I_{ref} (Iac*) becomes the controlling variable.

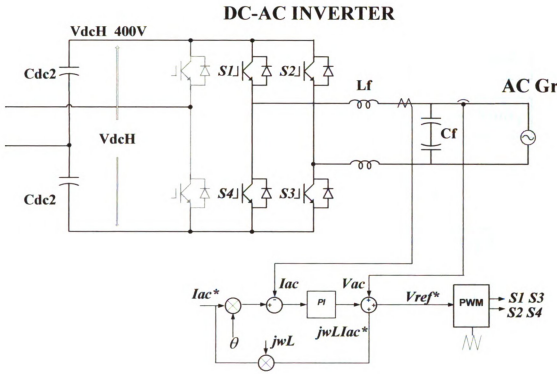


Figure 46 Grid connected current control

The block diagram of the current control loop is shown in Figure 46. An external voltage signal with 240V AC, 60Hz is first fed into a discrete single-phase phase-locked-loop (PLL). The PLL is necessary to make sure that when utility voltage is present, the inverter voltage is synchronized with the utility voltage. Discrete PLL is used to find the phase angle of the utility voltage. Figure 47 shows the PLL structure we used for synchronize grid current to grid voltage. First we generate 60Hz sine signal and make product with real grid voltage. Once it go pass by digital low pass filter, average goes to zero in few cycle. This means Vgrid and Vsyn voltage getting close enough to get synchronized. Then next step is that different value is amplified and sum up with fundamental radian velocity. Integration of radian velocity is phase angle. This angle makes feedback voltage and continuing this same process until it get close with grid voltage phase.

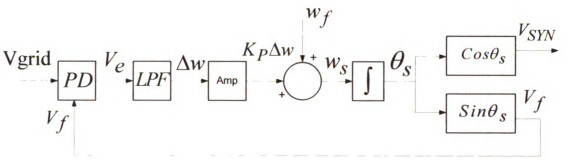


Figure 47 Block diagram of product type PLL

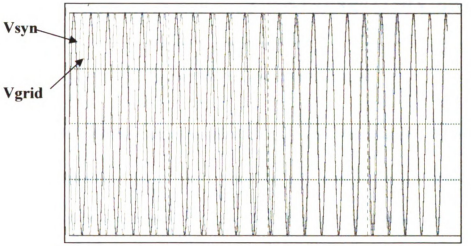


Figure 48 PLL simulation result

Figure 48 shows the simulation result of PLL. V_{syn} and V_{grid} waveform become same phase in a few cycle. Figure 49 shows the inverter output voltage and grid voltage realizing product type PLL control. Inverter output voltage become same magnitude and phase with grid voltage after operating PLL control.

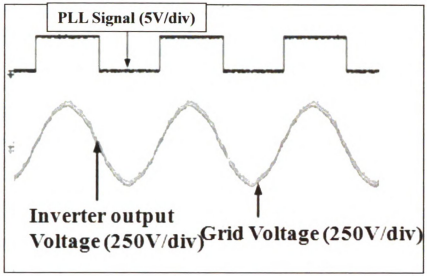


Figure 49 PLL experimental result

The user defined rms current amplitude ($I_{ac}*$) and phase angle (θ) are then used to generate the reference current waveform. This sine wave is compared to I_{ac} and the controlling output I_command is generated. I_command current then sum up with V_{ac} and $jwL \cdot I_{ac}^{*}$ in order to make desired current. To ensure stability for high-duty cycle conditions, a stabilizing saw tooth wave is added to the phase adjusted sine wave. The final output of the current controller is a duty cycle value (D), and is given by equation

$$D = \left(0.5 + \frac{V_{ac}}{2 \times V_{dc}} \right) + \frac{K_i \times (I_{ac}* - I_{ac}) \times L \times f_{sw}}{2 \times V_{dc}} \tag{4.11}$$

where, V_{ac} is the inverter output voltage, V_{dc} is the DC link voltage, $I_{ac}*$ is the reference current, I_{ac} is the inverter output current, K_i is the proportional gain, L is the gain and is set to a filter inductance of 2[mH] and f_{sw} is the gain equal to a switching

frequency of 10 kHz. As with the voltage control loop, this duty value is then compared to a 10kHz triangular wave to generate a 10kHz PWM switching signal with positive duty cycle of D.

4.3 Test Setup and Software Implementation

4.3.1 Test Setup

The power circuit for the complete inverter system is shown in Figure 50.

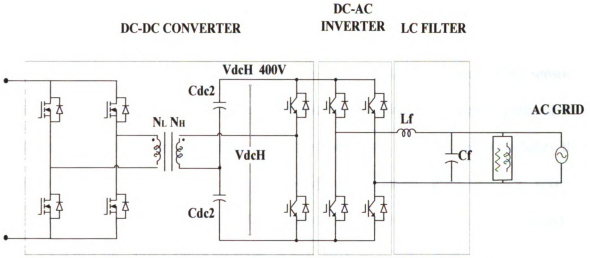


Figure 50 Power circuit of Inverter system connected with grid

The DC input stage of the inverter consists of a 400V DC source along with a small series resistance of 0.4Ω. This series resistance is required in order to facilitate convergence of the model in the simulation environment. The power electronics devices are modeled based on the IPM module parameters used in the hardware setup. The IPM module consists of six IGBT switches along with 1500uF of input capacitor. The output of the inverter is fed to the inductor-capacitor (LC) line filter. The series-connected, 2mH inductors and 7.5uF capacitors are used in order to achieve desired voltage and current ripple characteristics. The output of the inverter is a single-phase, 60 Hz, 240V AC rms

waveform. . Though an optional DSP controller can also be included inside the module, but in the laboratory setup an external DSP was selected for this particular design to have more flexibility. Various low DC voltages are required to operate different parts of the hardware. The PV system module requires 15V DC, the DSP board requires 5V DC, and additional 48V DC is required for all the electronic integrated circuits (ICs). A small DC power supply is used for generating 48V DC from 120V AC utility. The 5V DC is developed from the additional power supply PCB board. A precision micro-power, low dropout voltage reference IC is used for generating the voltage references for analog-to-digital (A/D) converters in the DSP. The phase current sensors, DC bus voltage sensor, and heat-sink temperature sensor are built on the PCB board. In addition to those sensors, battery voltage and converter input current sensors are added to different parts of the hardware to achieve control and protection requirements. The test setup includes the inverter; a 240V, 60Hz AC source that emulates the utility grid; and one sets of resistances representing the local load. The inverter and the local loads are connected to each other through single-phase breakers. When breakers are closed; the inverter operates in the utility-connected mode. In that scenario, both the inverter and utility provide power to the local load. To test islanded operation of the inverter, the utility breaker is opened so that the inverter supplies power to the local load.

The maximum voltage across the switches in the grid-tied VSC is 400V. The peak current through the switch occurs at maximum ac load power of 2 kW and at minimum ac voltage of 220 V. The peak current through the switches is 13A.

As mentioned in previous section, a 600-V/75-A (IGBT-IPM) is selected.

In addition to the inverter platform, other components such as DC voltage source,

utility grid, RL load bank, and electronic load bank were connected in the test setup. The DC supply for the inverter was from output of isolated DC-DC converter from previous chapter. An ac power source is directly connected to 240[V] local grid. 1kW RL load bank, mimicking the local load, was placed in parallel to the grid. The load terminal of the inverter was connected to a 1kW/1Kva AC Load. A 1:1 isolation transformer was placed between the inverter output and the grid. The single line diagram of the complete test setup is shown in Figure 51.

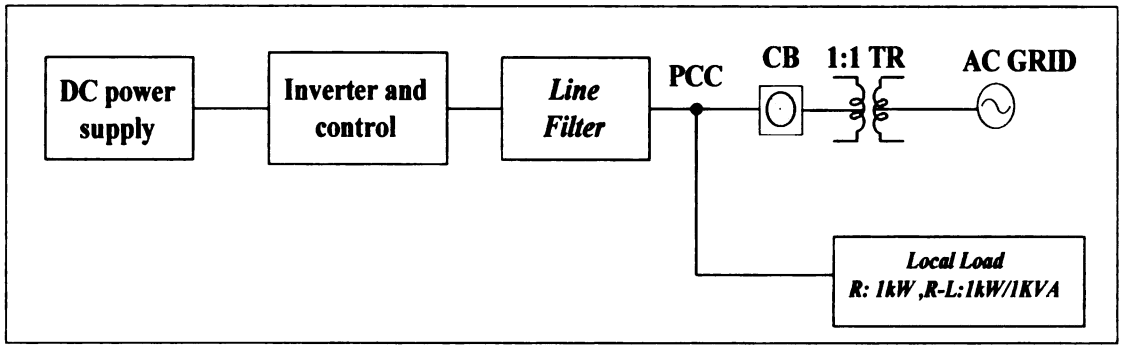


Figure 51 Single line diagram of test setup

4.3.2 Software Development

Up to this point, the voltage and current control for the inverters are implemented in the DSP controller. The program for the DSP is written using Texas Instruments Code Composer Studio which offers robust, mature core functions with easy-to-use configuration and graphical visualization tools for faster system design. The codes are written based in C programming language and then compiled and load into the DSP on-chip random access memory (RAM) using Code Composer Studio. Then the controller is activated using the serial interface. In future, the on-chip flash memory will be used for utilization of larger codes and retaining the compiled codes in the DSP. The program code is interrupt driven and runs at fixed sampling frequency of 10 kHz based on the interrupt

set up. For the inverter platform, the switching frequency is set at 10 kHz. The actual program codes for PWM calculations are written inside the interrupt service routine. This service routine runs once in each PWM cycle and is used to compute duty cycles for the next cycle. The controller was designed so that the control functions are interrupt driven. After completing A/D conversion (ADC), an interrupt is generated and the program goes to the interrupt service routine (ADC-PWM subsystem block).The ADC start occurs based on the period interrupt of the PWM. Therefore, the interrupt service routine runs once in each PWM cycle and is used to compute duty cycles for the next cycle. For the experimental evaluation, the PWM operates at 10 kHz, therefore the interrupt routine is called at every 100μs. A new fixed point PLL was developed which accepts a sinusoidal signal and outputs the phase angle for the input signal. The phase angle output is a ramp signal varying between 0 to 2π and is synchronized on the zero-crossing (rising) of the input signal. The grid voltage signal is fed from the ADC-PWM subsystem block to the PLL and the angle output from PLL is fed back to the same subsystem block. As the calculations inside the ADC-PWM subsystem block are done asynchronously with a sample time of 100μs defined by the hardware interrupt setting, several rate transition blocks are used in the model. Also the amplitude (I_{ac*}) and the phase (θ) of the current reference are fed into the ADC-PWM subsystem block.

The ADC-PWM subsystem block is a triggered subsystem and activated when the hardware interrupt occurs. Inside this subsystem, DSP's ADC channels are configured to perform analog-to-digital conversion of input signals. Both the ADC module A and B are selected and the simultaneous conversion mode is used. The ADC start occurs based on the period interrupt of the PWM using Event Manager A and an interrupt is posted at the

end of the A/D conversion. The output of the ADC goes into the scaling block where the digital signals are converted to their corresponding analog values. These scaled voltage and current measurements along with the PLL-calculated phase angle are then used for the voltage and current controller. The output of the controller is the percentage duty cycle value which is fed to the PWM block to generate 10kHz SPWM switching signals. When the operational mode is selected as islanded voltage control, the voltage control subsystem is activated. In the voltage control subsystem, the reference voltage signal is generated first using the phase angle (Theta) information. An offset is added to the PLL-calculated phase angle to take care of the phase shifts produced by sensors and control board filters. The amplitude of the reference voltage is set to 240V AC rms. A proportional–integral controller (PI controller) was used in the voltage loop. The final output from the voltage control subsystem is the percentage duty cycle and a saturation block was used to limit its output between 5% and 95%. For the operational mode of utility-connected current control, circuit breaker was closed and the current control was activated. Again, frequency and phase of the utility voltage were obtained using the PLL which was then used along with the user-defined phase angle and current amplitude to calculate reference current waveform. The PI controller was finally used to generate percentage duty cycle outputs.

4.4 Simulation and Experimental Results

4.4.1 Simulation Results for Voltage and Current Control

The inverter model is simulated in Simulink PLECS to allow researchers to observe both voltage and current control. In the simulation, the inverter is turned on at time=0.05s in current control mode. The rms value of the reference current is set to 8A and the phase angle is set to zero degrees. In the current control mode, breakers are closed and the inverter operates in utility-connected mode. At 0.5s, the utility breaker is opened, thus transforming the inverter control to voltage control to maintain 120V, 60Hz AC voltage to the local load. Finally the inverter is turned off at 0.95s. During the simulation, the local load is set as 10Ω resistive and the utility load is set at 6 Ω resistive. The simulation results for current control mode are shown in Figure 53-56. The waveforms for the inverter voltage (V inverter), inverter current (I inverter), utility voltage (Vs), and utility current (Is) are given in Figure 52,(1)-(8). We can observe from these figures that the waveforms are very clean with only some higher order current harmonics present in the inverter current waveform. During utility connected mode, the inverter supplies current equal to the reference current. The local load requires 12A current, of which 8A are supplied by the inverter and the remaining 4A are delivered from the utility through point-of-common-coupling (PCC). The PCC voltage and currents are denoted by V_g and I_g respectively.

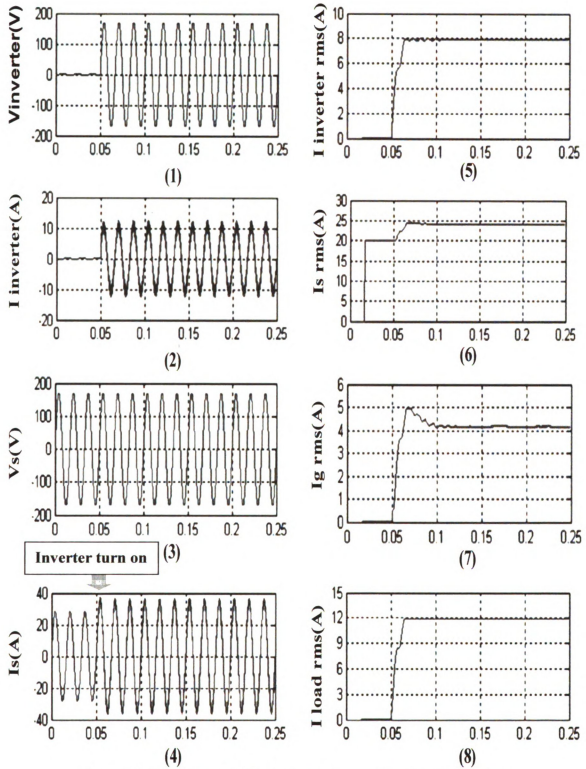


Figure 52 Simulation results for current control mode of operation

Before the inverter is turned on, breakers are opened, and the utility supplies 20A rms

to the utility load. When the inverter is operating, the utility supplies its own load along with the residual current required by the local load. The rms calculations for the currents are shown in Figure 52,(5)-(8). The simulation suggests that the inverter current control loop does a very good job of maintaining an 8A rms current when operated in the utility connected mode. Figure 53 shows the grid-connected mode single diagram of simulation.

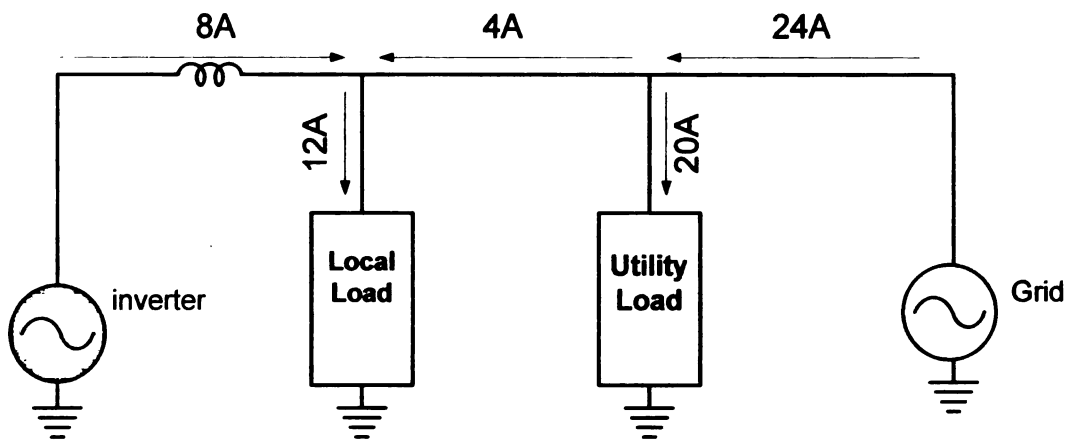


Figure 53 Single diagram of simulation circuit grid-connected mode

When the utility breaker is opened, the inverter switches to islanded operation to supply power to the local load. The simulation shows that the utility keeps supplying the utility load but there is no power flowing through the PCC. In the islanded mode of operation, the inverter is voltage controlled to maintain 120V AC, 60Hz voltage for the local load. The voltage and current waveforms in this mode of operation are shown in Figure 54,(1)-(6). From Figure 54-(2), we see that the inverter is maintaining 120V AC rms and supplying current to the local load. The utility voltage and current waveforms are shown in Figure 54,(5)-(6) and it is evident that the utility is supplying power to the utility load.

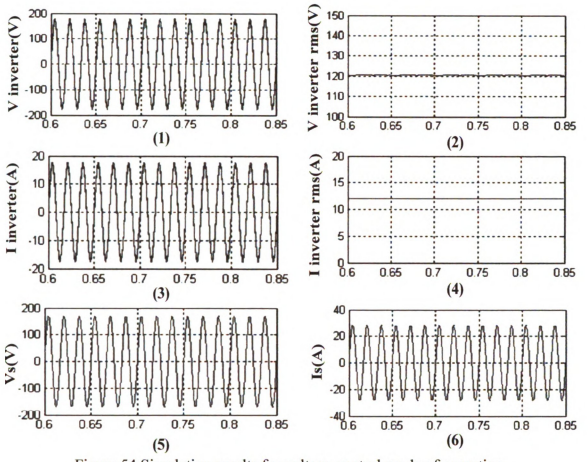


Figure 54 Simulation results for voltage control mode of operation

Finally, in Figure 55 the voltage and current waveforms from the complete simulation sequence of operation. Figure 56 shows diagram of transition of two control mode. From these waveforms, we see that the simulated transients during the change in mode of operation from current to voltage control are small. The local load does not experience any variation in voltage Figure 55-(5), when the inverter is disconnected from the utility. Also from Figure 55-(4), it is evident that the power is transferring through the PCC only when the inverter is utility connected. From the inverter current waveform, as in Figure 55-(2), we see that the transition from utility-connected to islanded mode is smooth. In the utility-connected mode, the inverter is supplying 8A rms current which is increased to 12A rms when the inverter is in islanded mode supplying the local load.

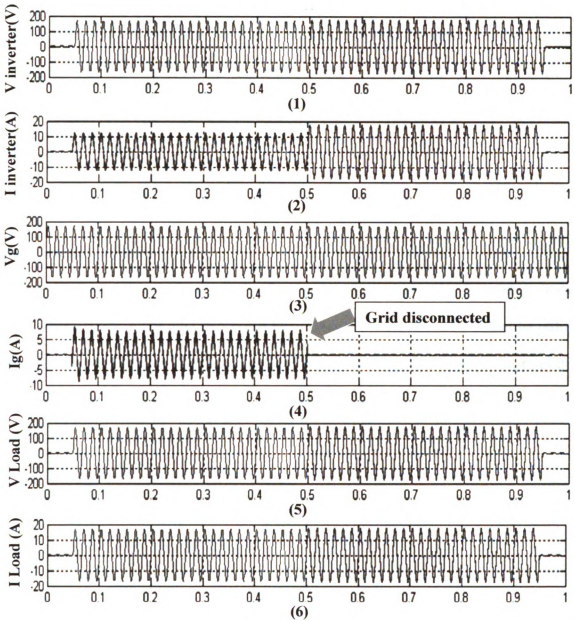


Figure 55 Simulation Waveforms for Complete Inverter Operation

It is important to note that, in Figures 52 to 55, only some representative results are shown based on particular load settings and set points. The inverter model was tested with a variety of different types of loads and different voltage and current reference settings to verify its operation under various scenarios.

The inverter platform was initially evaluated using both islanded-mode voltage

control and utility-connected-mode current control. Based on successful operation of the inverter in the voltage control mode, current control mode tested experimentally.

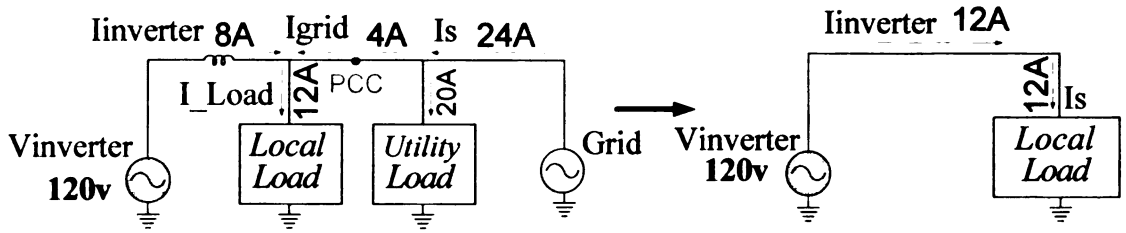


Figure 56 Single diagram figure of current and voltage control: transition of control mode

Experimental Setup

For the voltage control tests, the DC bus voltage was set at 400V DC and the local load resistance was set at 60Ω resistive which consumes 1Kw at 240V. When the utility circuit breaker is left open, the inverter supplies the local load and the utility supplies the utility load. The local load resistance was varied from no load to full load. We observed that the inverter output voltage operates close to 240V AC rms for both the no load and full load cases. In this test the DC bus voltage was set at 400V DC, the local load was set with 60Ω and 0.2[H] L load was added. The amplitude of the reference current was set at 8.3A rms and the phase was set unity power factor as we seeing from inverter side.

4.4.2 Experimental Results for the Stand-Alone Mode Operation

Series connected PV system can be grouped into two categories from the relationship between the inverter output and utility grid. The first category is the situation where the inverter is not connected with utility grid, which is named as "stand-alone", as shown in Figure 57. In this situation, because the output of PV and battery is limited, only part of loads (critical loads) is admitted to connect. An MPPT algorithm is executed for PV to obtain maximum power to meet the demand of the critical ac loads. If the produced

obtain maximum power to meet the demand of the critical ac loads. If the produced electric power from PV is less or more than the load need, the battery is used to compensate the difference. That is, the actual charging (or discharging) current depends on the PV power production and the demand of onsite critical loads. In this case, the isolated dc-dc converter shall use the constant dc link control strategy and the inverter shall use the voltage/current control strategy. Because the buck converter should be utilized to realize MPPT for PV if both the battery current and voltage do not exceed the safe limit, it shall carry out the control shown in previous section. Otherwise, the buck converter will carry out battery current or voltage limit control. It should be noticed that, under stand-alone mode, when the battery is discharged so deeply that its voltage reaches a minimum threshold, the load (or converter) shall be automatically disconnected (or shut down).

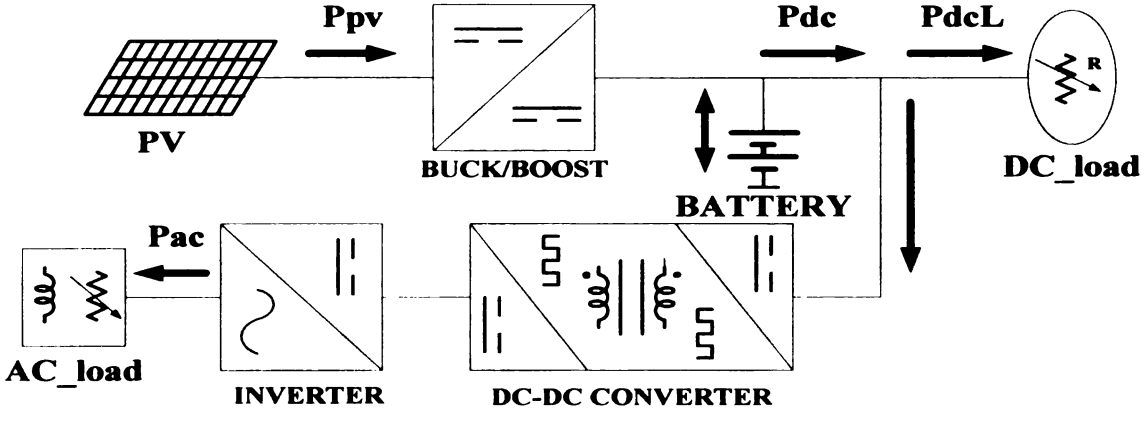


Figure 57 First category operation mode: stand-alone

In islanded operation, the inverter has to maintain the amplitude and the frequency of the voltage so that the connected local loads are not affected by utility interruption. The voltage control loop for the inverter is designed for such islanded mode of operation. When the utility voltage is present, software zero-crossing detection is used to obtain the

frequency and phase of the voltage reference, whereas the frequency is set to 60Hz when there is no utility. We have found that the fixed amplitude of the reference voltage causes bigger steady-state errors depending on the change in local load. To overcome this problem, a slower control loop (running at 1/60 s) was designed that changes the amplitude of the reference voltage depending on the output current. The final output of the controller is a duty cycle value (D). The DC input voltage was set at 400V DC. The screenshot of experimental results for the voltage control is given in Figure 58.

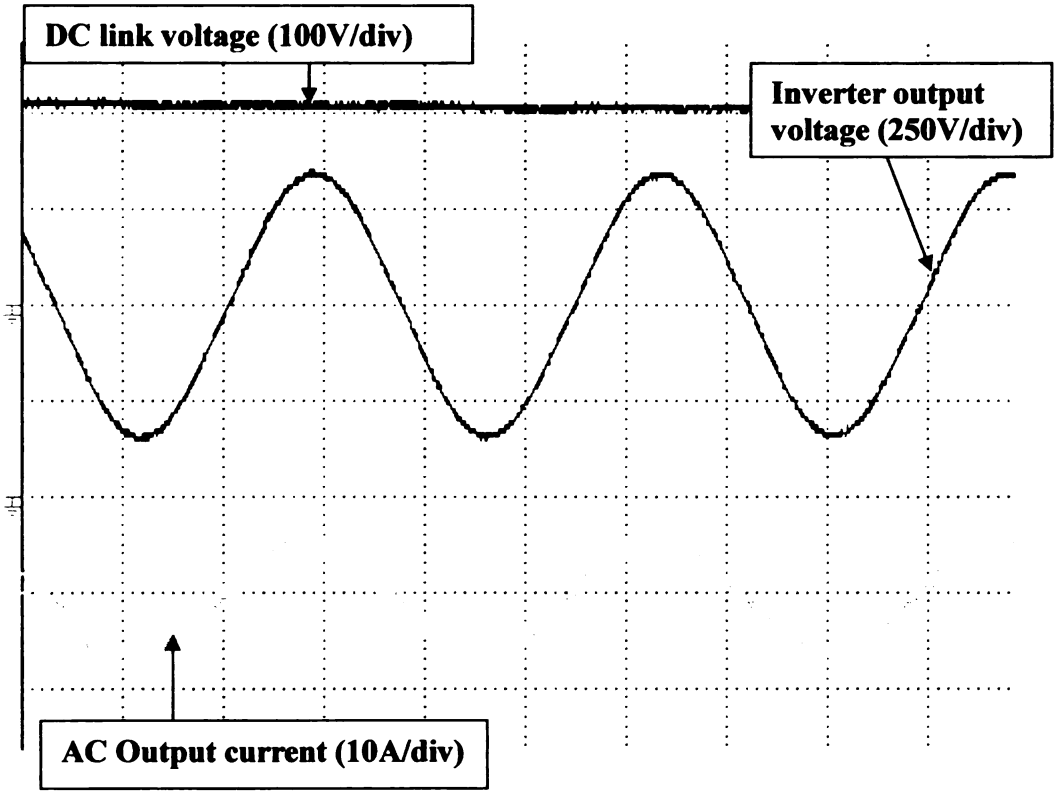


Figure 58 Experimental results of inverter.(Stand alone mode.)

The local load is set at 60Ω at this time. The inverter is islanded from the utility and no connection exists between the inverter and the utility as the circuit breaker is kept open. We can see from the waveforms that the harmonics present in the inverter voltage are low and the inverter voltage is in phase with the inverter current.

Stand-alone mode R-L load test.

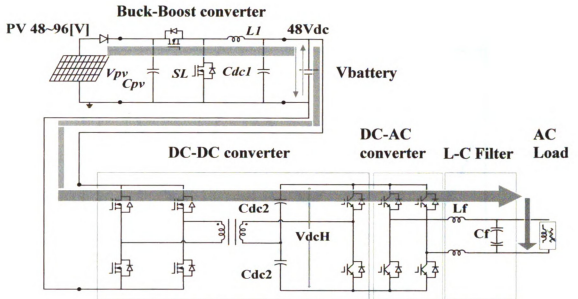


Figure 59 Stand-alone mode power flow

To verify variety of load condition, we set the R-L load condition in stand-alone mode. First we set the L with $0.2[H]$ using transformer to get high reactance at the primary side of the L load. Picture 59 shows 60Ω Resistor is parallel with L load at the ac output side. Since output voltage is 240V, we can calculate estimate real power and reactive power of the load. Real power consumed by resistor is $960[W]$ and reactive power at the L is near $763[VAR]$. From knowing the P,Q value we can derive apparent power which is $1.22[KVA]$ with 38° lagging. This setup is appropriate for replacing motor load in real situation. The theoretical power factor was 0.79.

Figure 60 and Figure 61 shows the waveform of inverter output voltage and output current at the ac side. It shows almost similar angle between voltage and current as we calculate before. Since apparent power is $1.22[KVA]$, the current is near 5.1[A]at the

load. It is obvious that with low power factor, inverter have to generate higher current than at the power factor 1.

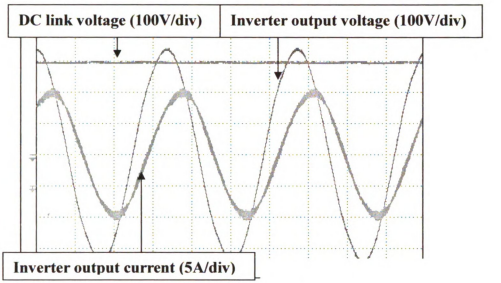


Figure 60 L-R Load waveform at PF 0.73

Actual power factor value was 43° due to line impedence effect. From measuring the time delay between voltage and current shown in Figure 61, we can derive power factor of inverter. 1.99msec is phase angel delay time between voltage and current while 16.66msec is the time for 60Hz.

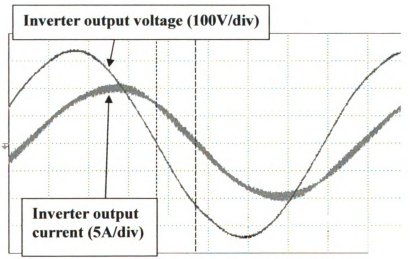


Figure 61 L-R Load waveform at PF 0.73

The inverter in the voltage controlled mode was also run for differe

maximum load for the inverter is limited to 15A rms by the measurement and protection circuits. Therefore the local loads were adjusted in such a way that the maximum inverter output current did not exceed 12A rms.

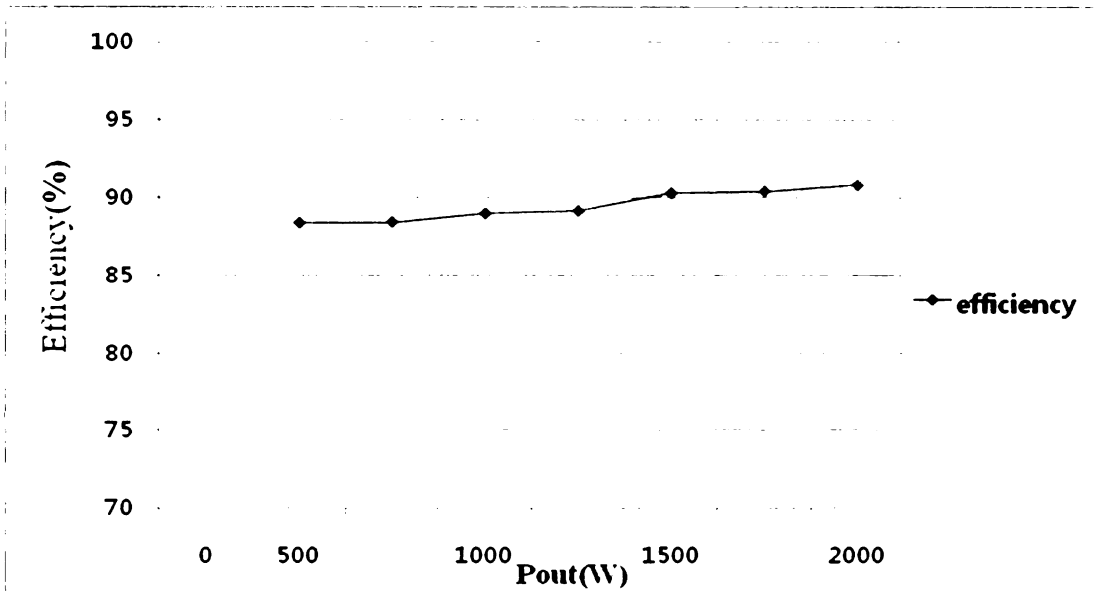


Figure 62 Efficiencies of the Voltage-Controlled Inverter

Finally the input-output efficiencies of the inverter are shown in Figure 62 over varying load conditions. It is evident from the figure that the lowest efficiency of 86% occurs at the light load condition and, as loading increases, efficiency also increases. The range of efficiencies are good considering the fact that the inverter is operating at much lower power levels than the full load of the IGBTs, which are rated for 75A continuous current and 600V AC rms. Also the inverter platform is built to have some flexibility so that different distributed energy sources can be connected to it in future.

4.4.3 Experimental Results for the Utility-Connected Operation

The second category in Figure 63 is the situation where the gateway grid is connected to utility grid. Part of the PV produced power is transferred to the battery and dc loads, and the excess power is transferred to utility grid and ac loads (termed as forward grid-connected). On the other hand, the whole system will draw real power from utility grid if the PV produced power is not enough to supply dc loads and the battery (termed as reverse grid-connected). In this case, the isolated dc-dc converter shall use the constant dc link control strategy and the inverter shall use the current control strategy. The buck converter should realize MPPT control and the control strategy shall apply.

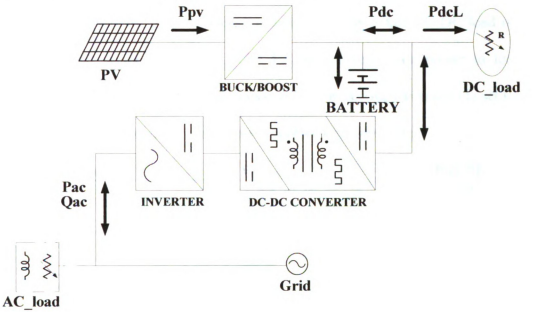


Figure 63 Second category operation mode: grid-connected

When the inverter is connected to the utility, the grid controls the amplitude and frequency of the inverter output voltage, and the inverter itself operates in the current control mode. The currents required by the local load is shared by the inverter and the utility, where the inverter provides the amount of current based on the reference current.

In the current controller, software zero-crossing detection was used to obtain the frequency and phase of the utility voltage, which was then used along with the user-defined phase angle and current amplitude to calculate the reference current waveform. After obtaining the reference current waveform the current controller was designed. The final output of the current controller is a duty cycle value (D). The PWM generation is the same as described in the voltage controller section. The DC input voltage was set at 400V DC. The current control loop was tested with different amplitude and phase reference values.

Test setup for grid connected mode

The test parameter for grid connected system is shown in table 1. DC load of buck converter is 10Ω which consumes 250W. DC source supply dc power to load and surplus power is send to ac load or grid. Leakage inductance for the system is set up with $11\,uH$ which could realize more stable power control with this value.

Component	Value	P/Q/PF
R_{dc}	10Ω	$250W$
C_{dc2}	$3000uF$ each	
L_f	$2mH$	
C_f	$7.5uF$	
$Cutoff\_frequency$	$1.3KHz$	
R_{ac}	60Ω	$960W$ **(actual:1.3Kw)**
L_{ac}	$0.2[H]$	
X_{Lac}	75.39Ω	$763VAR$ **(actual:1KVA)**
$Power\_factor$ of inverter side	$PF = 360 \times \frac{1.99}{16.66} = 43^{\circ}$	$Cos43^{\circ} = 0.731$
$Ac\_grid\_voltage$	$240V$	

Table 1 Test setup parameters

Situation #1 (Resistive load experiment)

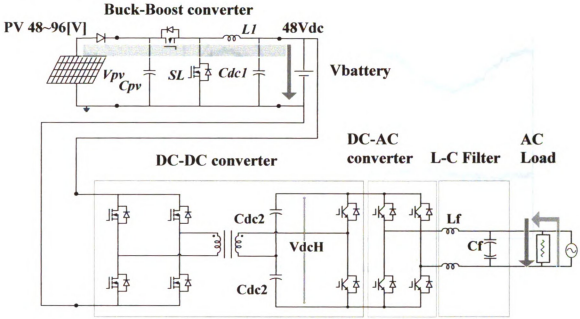


Figure 64 Grid-connected mode power flow before turning on the inverter

To test the current controlled mode of operation, it is necessary to make sure that the current control loop is working before actually making utility connection. In this test setting, the inverter output terminals are connected with grid where grid resistance is very small. First, the reference current is set to zero, then the system is turned on. After system become stable, the reference current value is increased to a higher value.

Figure 64 shows that DC source only provides power to dc load and battery since inverter is turned off. This situation is possible when PV power and battery energy is insufficient or not available during the night time. Before turning on the inverter, only grid can supply power to ac load as shown in Figure 65. Both PV power and battery supply power to the dc load when PV don't have enough power. It can be seen from the figure that, the inverter current is nearly zero.

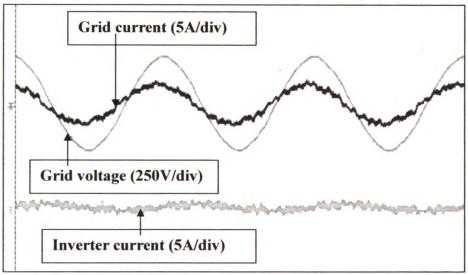


Figure 65 Inverter output voltage and current

Situation #2 (Resistive load experiment)

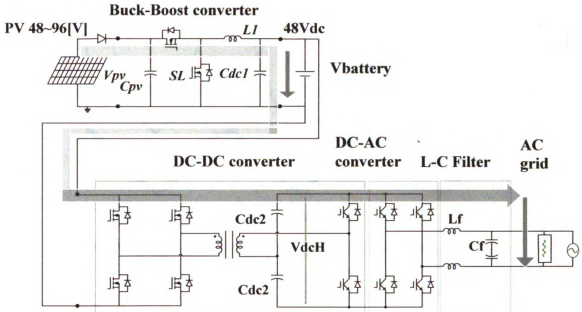


Figure 66 Grid-connected mode power flow after turning on the inverter

In this situation, only inverter provide power to the load which means ac load power is same as PV power. Figure 66 shows grid-connected mode power flow after turning on the inverter. When system is connected to the grid with 1KW active power demanded by the ac load, system is operated with only the PV panel connected in the system and the

inverter is used to feed the maximum available power to the ac load. The power transmitted into grid was 0 W since PV power is limited to 1KW. DC link voltage is 400V, line to line ac voltage is 240V and output ac current is 4A. Output power is around 1KW at 60Ω resistive load. It can be seen from the Figure 67 that, the grid current is nearly zero. Only inverter provides the current to a resistive load which is about 1KW and also indicating that the inverter side power factor is equal to 1.

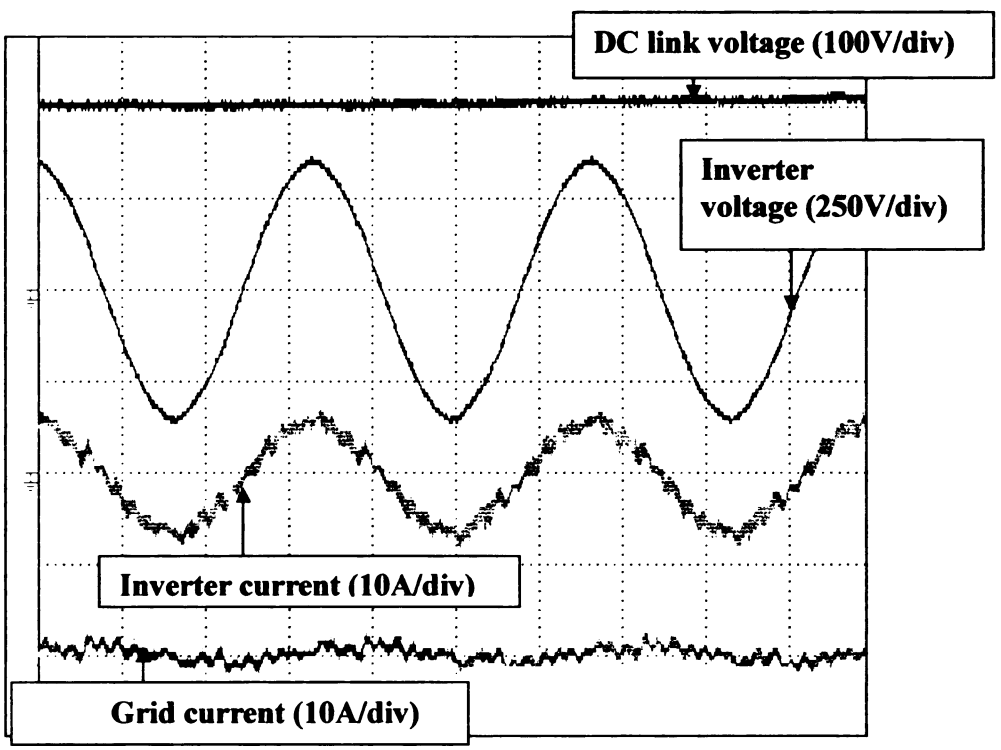


Figure 67 Experimental results of inverter.(Grid connected mode.-1KW)

Situation #3 (Resistive load experiment)

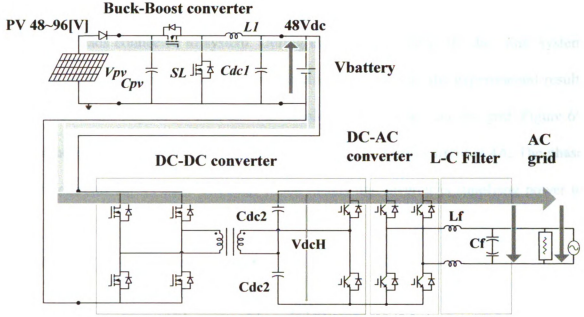


Figure 68 Inverter output voltage, current and grid current

When PV can transfer 1KW as well as battery(1KW), whole system can supply 2KW power to both ac load and grid as shown in Figure 68.

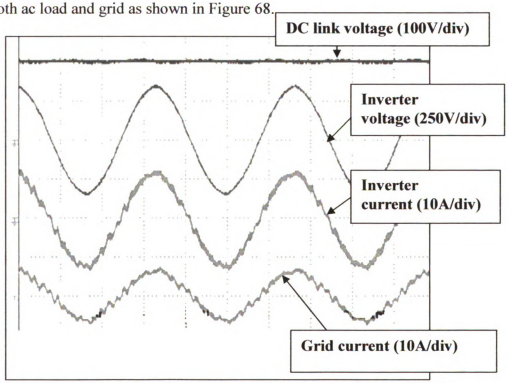


Figure 69 Experimental results of inverter.(Grid connected mode.-2KW)

This situation can be possible when PV and battery power have big enough power to supply all loads connected to system. During the peak sunlight in the day time, system can send surplus power to grid for cost reducing purpose.From the experimental result, 1KW is consumed by the ac load and the remaining 1KW is fed into the grid. Figure 69 shows the waveform that inverter output current is 8A and grid current is 4A. The phase of both currents shows same direction which means that inverter is supplying power to grid.

Situation #4 (only R load experiment)

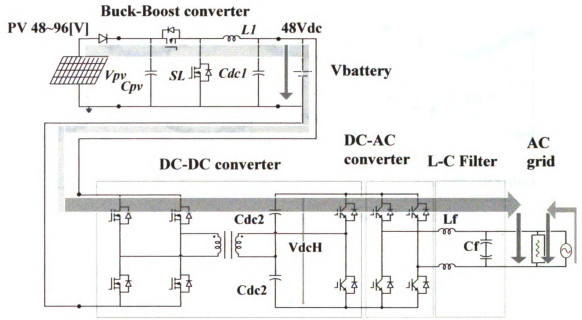


Figure 70 Inverter output voltage, current and grid current.

In this situation, inverter and the grid provide the power to the ac load as shown in Figure 70. Both the PV system and grid are operated in parallel. When PV can not supply enough power to ac load during the night time or when the battery has no energy to discharge, grid should supply its power to ac load with inverter side power. Figure 71 shows the inverter output voltage and current waveforms and the grid current. After

reducing power of PV side to 500W, both inverter and grid is supplying active power to 1KW ac load. From the curve, we could observe that each current curve has 180 phase difference representing that both current are flowing opposite direction in order to supply power to ac load. Above experiment was based on Resistive load condition.

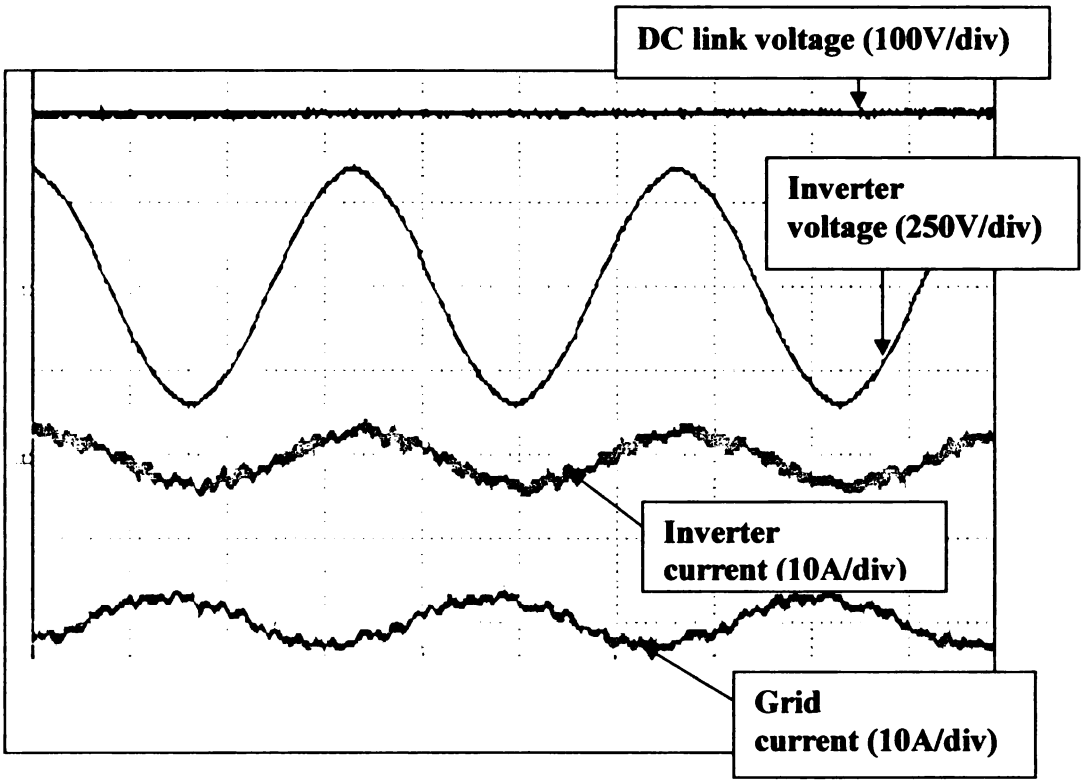


Figure 71 Inverter output voltage, current and grid current

Situation #5 (Inductive load experiment)

Installing inductive load to see verity of load condition of system. Since inverter is working with unity power factor control, grid power factor become lower. After turning on the inverter, grid supply power to ac load and PV supply power to DC load(250W). Inverter supply real power (520W) to ac load and at the same time grid supply real power(780W) to ac load which consumes near 1.3[KW]. Figure72 waveform shows DC load current, voltage, AC load voltage and current waveform. Seeing from the inverter

side, we could observe that power factor is near 1 by using unity power factor control. L load was about 0.15[H] in real experiment situation. Reactive power consumed by inductor is near 1KVA. Different phase angles is shown between grid voltage and grid current due to inductive load. Figure 73 shows that grid current is 52 degree lagging to voltage which means grid is supplying real power(780W) to the ac load as well as reactive power(1KVA).

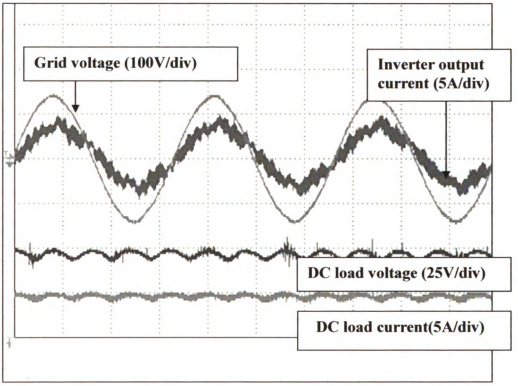


Figure 72 Ac load voltage, current & Dc load voltage and current

We could verify that inverter controlled with unity power factor with lack of power to supply ac load, grid always supply both real power and reactive power to the R-L load. In this experiment, since ac load consumes 1.3KW, both inverter and grid supplying real power. In addition, grid supplying 1KVA reactive power. As a result, grid shows 0.61 power factor as shown in Figure 73.

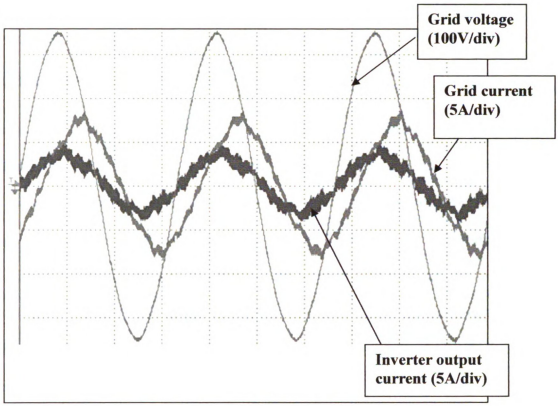


Figure 73 Inverter output voltage, current and grid current(inductive ac load test)

	Inverter	Grid
KW	*520w*	*-780w*
KVA	*0*	*1KVA*
PF	*1*	*-0.61pf*
Degree	0°	52°

Table 2 Inverter and grid power factor

Chapter 5

Conclusion

A new low cost series connected PV system for Stand-alone/Grid-connected applications has been presented in this paper. The operation, analysis, features, and control scheme were explained. Simulation and experimental results for the 1kW prototype are shown to verify the operation and control principle. A buck converter is used for the MPPT implementation and presents the functions of battery charger and step-down converter. The dc-dc converter realize phase shifting to control power flow through a transformer with a MOSFET full bridge on the LVS.(low voltage side) In addition, a voltage doubler on the HVS(high voltage side) is installed to achieve enough high voltage to run the inverter. The feature of the prototype includes the combination of dc-dc, dc-ac and/or ac-dc converters for the flexible and uninterruptible energy utilization and a smart algorithm for optimizing the power consumption and defining priority on the demand system. For energy sources such as PV or fuel cell that generate DC, an inverter is required to convert DC into AC for utility connection and consumer use. Though low power single-phase inverters are very common and available from different manufacturers, these inverters mainly work as a controlled current source when they are operating in the utility-connected mode. This thesis outlines the detailed modeling, design, and testing of a single phase PV inverter system that operates in both islanded mode and utility-connected mode. Both modeling and experimental results are given to demonstrate the ability of the developed inverter to provide advanced control functions. We used the Simulink PLECS simulation to develop the single-phase inverter model and the control

algorithms before they were implemented in hardware. The parameters and simulation conditions for the model were carefully selected to accurately emulate the hardware. Also, the control designs have been developed in such a way that they could be implemented on a hardware DSP platform. In addition to the inverter power and control circuits, the laboratory test setup consisted of several other components, such as a DC voltage source, a utility grid and a RL load bank. Two techniques were demonstrated for DSP code generation. Initially the DSP code was written in C- language using Code Composer Studio and experimental results proved that the inverter successfully operates for all functional modes, namely the islanded voltage control mode, and utility-connected current control. Future work will concentrate on developing and testing additional ancillary functions such as power quality control and seamless transfer for the inverter associated with distribute energy sources.

Future work

First, the increase interest in novel architectures based on the adoption of switching converters employing a PV module-dedicated decentralized MPPT function is giving rise to new challenging problems. The distributed-MPPT method, which is also stimulating some industries to the production of DMPPT dedicated devices, allows for reducing the impact of the mismatching effect, but its implementation requires further studies in terms of interactions among different systems, employing the MPPT function at the same time.

Second, Sic semiconductors have a high potential for enhancements of the electrical conversion efficiency of PV systems. In addition, high switching frequencies inherent to such devices will also enable decrease of weight and cost. The most significant characteristics of Sic is the very high electric breakdown field, resulting in very low specific on-state resistance even at higher blocking voltages, as can be observed below for different switch technologies. This will allow the use of simplified circuits with fewer semiconductors and power state as well as allow a considerable diminution of the heat-sink size and cooling effort, again reducing the weight and cost of the converter.

Third, multilevel PWM converters are gaining popularity in the field of renewable energies because of the need of connecting several distributed power sources, whose power is continuously growing, guaranteeing at the same time good power-quality levels. They can be used as rectifiers in the case of wind and hydroenergy, where the electricity is generated by ac generator and inverters in the case of wind, solar, hydro and fuel cell generation. Multilevel active rectifiers improve the absorbed ac currents, thus reducing generator stress; at the same time, they allow precise output voltage regulation, thus eliminating the need for a dc/dc convert

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