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ZERO CURRENT SWITCHING SWITCHED-CAPACITOR DC-DC
CONVERTERS FOR THERMOELECTRIC GENERATION
APPLICATIONS

presented by

Dong Cao

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of the requirements for the

M.S. degree in Electrical Engineering

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**ZERO CURRENT SWITCHING SWITCHED-CAPACITOR DC-DC
CONVERTERS FOR THERMOELECTRIC GENERATION APPLICATIONS**

By

Dong Cao

A THESIS

**Submitted to
Michigan State University
in partial fulfillment of the requirements
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ABSTRACT

ZERO CURRENT SWITCHING SWITCHED-CAPACITOR DC-DC CONVERTERS FOR THERMOELECTRIC GENERATION APPLICATIONS

By

Dong Cao

Thermoelectric generation (TEG) module as a renewable energy source for automotive industry is becoming more and more popular recently. Because of the inherent characteristics of TEG modules, a low input voltage, high input current and high voltage gain dc-dc converters are needed for the automotive load. Traditional high voltage gain dc-dc converters are not suitable for automotive application in terms of size and high temperature operation. Switched-capacitor dc-dc converters have to be used for this application.

However, high voltage spike and EMI problems exist in traditional switched-capacitor dc-dc converters. Huge capacitor banks have to be utilized to reduce the voltage ripple and achieve high efficiency.

A series of zero current switching (ZCS) switched-capacitor dc-dc converters have been proposed to overcome the aforementioned problems of the traditional switched-capacitor dc-dc converters. By using the proposed ZCS strategy, high voltage spike is reduced, high EMI noise is restricted, and the huge capacitor bank is eliminated. High efficiency, high power density and high temperature ZCS switched-capacitor dc-dc converters could be made for the TEG interface in automotive applications. Several prototypes have been made to validate the proposed circuit and confirm the circuit operation.

Dedicated to:
my wife, Ying Ding

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CHAPTER 1

Introduction and Motivation

Recently, renewable energy sources are used more and more in automotive industry for hybrid electric vehicle (HEV), such as photovoltaic (PV) cells, fuel cells, and thermoelectric generation (TEG) modules. Because of the newly developed materials for the efficiency improvement of TEG modules, TEG for automotive application has drawn more attentions. However, TEG modules are still not widely used in the automotive industry; there are several problems of TEG modules that limit their applications. Because of the inherent low output voltage and high output current characteristics of TEG modules, special dc-dc converter interface is required for the automotive applications such as battery charging. This thesis will concentrate on developing a high efficiency, high input current, high voltage gain step-up dc-dc converter as the interface circuit for TEG modules in automotive application.

The following discussion starts with the background information introduction of TEG modules, literature review of the traditional step-up dc-dc converters and their application limits for the automotive application, conventional switched-capacitor dc-dc converters for automotive applications, and their limitations.¹

¹ This chapter was presented in part at the 39th IEEE Power Electronics Specialists Conference, Island of Rhodes, Greece, Jun.15-19, 2009

1.1 Background

1.1.1 TEG Modules Basic Structures and Potential Automotive Applications

Thermoelectric modules (thermoelectric devices) are solid state devices that can convert thermal energy from a temperature gradient into electric energy as power generators or vice versa (convert electrical energy into a temperature gradient across the modules) for cooling applications [1]. Unlike the thermocouples used for temperature measurement, the TEG modules can generate enough electricity for many applications [2]. Compared to other energy conversion methods, TEG modules are reliable without any noise or vibration and are attracting more attention as renewable energy sources where temperature gradients are available. Because of the low efficiency and cost issues, previously the TEG modules have been restricted to special applications, such as powering the onboard electronics of a satellite in deep space, and providing electricity from nuclear heat for a submarine in deep waters [3, 4]. Recently, due to environmental concern and global warming issues, TEG modules have received more attention as a method to convert wasted heat to electricity. For example, converting the waste heat from the exhausting pipe of automobiles to power accessory electric loads such as air conditioner in a vehicle or put the energy back to the wheel to increase efficiency [3, 4]. Many new materials have also been developed to increase the heat to electricity conversion efficiency of TEG modules [5, 6, 7].

Thermoelectric modules consist of p -type and n -type semiconductors connected electrically in series and thermally in parallel as shown in Figure 1.1 and Figure 1.2 [8].

Figure 1.1(a) shows a pn module used for cooling applications while (b) shows the same device being used for power generation. By the Seebeck effect, heat flow through this thermoelectric material will tend to move the charge carriers in the same direction as the heat flow. As shown in Figure 1.2, TEG modules for power generation usually consist of an array of $2N$ pellets (n- and p- type semiconductor thermoelements) that make up N thermoelectric couples thermally in parallel and electrically in series to achieve high output voltage and high power [8]. Usually these pellets are connected by high conductive metal strips and sandwiched between thermal conducting while electrically insulating metalized ceramic plates. The pellets, tabs and substrates thus form a layered assembly, which is shown in the Figure 1.3 [9].

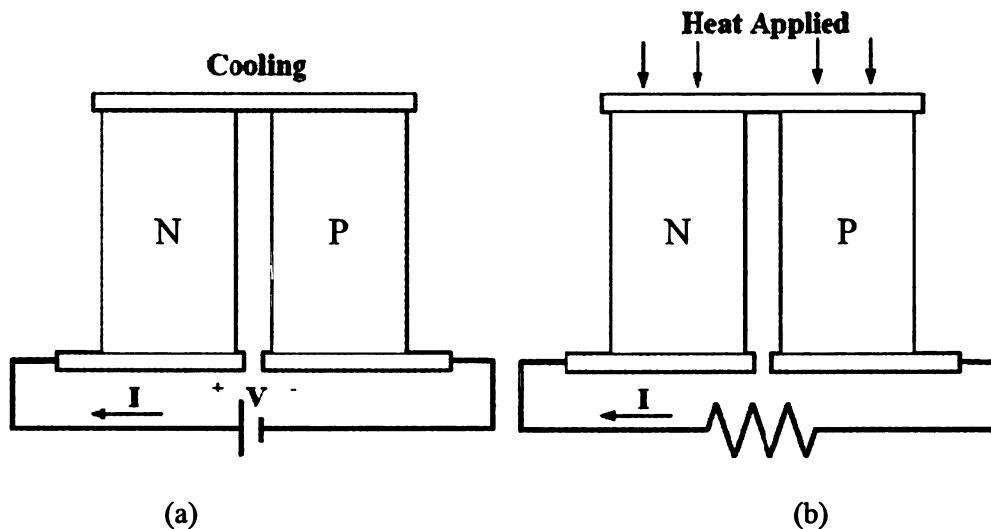


Figure 1.1 PN Thermoelectric modules. (a) Cooling applications. (b) Power generation.

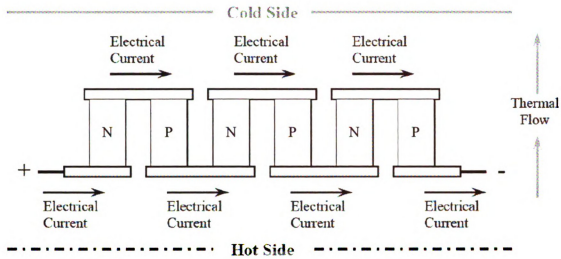


Figure 1.2 TEG module configuration.

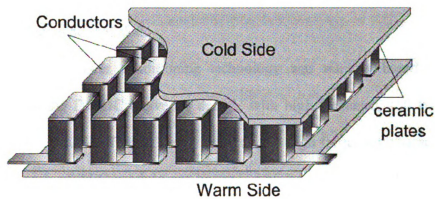


Figure 1.3 Typical TEG module assembly.

By adding TEG modules around the car exhausting pipe, the waste heat energy can be converted into electricity shown in Figure 1.4 The new developed materials for TEG modules has about 10% electricity conversion efficiency, which means 10% waste heat energy can be converted into electricity. In this case, more than 5% of fuel can be saved. The generated electricity by the TEG modules is around 500 W~ 1kW in some big truck. And this depends on how many TEG modules are put around the exhausting pipe.

TEG
Modules

Exhaust

Coolant

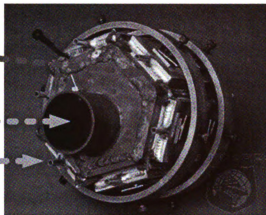


Figure 1.4 TEG modules around the exhausting pipe

1.1.2 TEG Modules Electrical Characteristics

In order to apply TEG modules to automotive application, electrical characteristics of TEG modules has to be modeled.

At present, the power conditioning technology was majorly based on the high frequency switching DC-DC converter design, with high frequency (50 KHz~1 MHz) switching device (MOSFET, IGBT etc.) used. So the high frequency characteristics and dynamic response of TEG module are becoming major concerns in the outside power conditioning circuit design. In order to design a suitable switching dc-dc converter special for the TEG module usage, the high frequency electrical characteristics of TEG module in steady state and in transient procedure have to be known. In the following parts, a method will be proposed to test the TEG module outside electrical characteristics in steady state and in transient procedure, and a high frequency electrical model will be put forward to help design the switching power supply DC-DC converter.

To characterize TEG modules, a heat exchanger capable of outputting 100 W electrical power was designed and fabricated. Figure 1.5 shows the decomposed structure of the heat exchanger. Heat elements are distributed evenly within the hot plate to

generate a uniform hot side temperature. A total of twenty TEG modules, G1-1.4-219-1.14, from Tellurex® Corp. shown in Figure 1.6 [10], are installed on both sides of the hot plate, ten pieces on the top of the hot plate and ten pieces on the bottom of it. Two radiators are clamped on both sides to cool the TEG modules' cold surface. When a temperature gradient exists between the hot plate and the radiator, electric power is generated by the TEG modules as a result of heat flow through them. Thermal couple was used as temperature sensor that was installed in the hot plate and the heat sink to monitor the temperature between hot side and cold side during the tests.

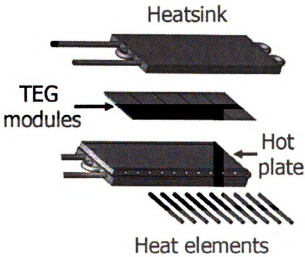


Figure 1.5 Heat exchanger configurations

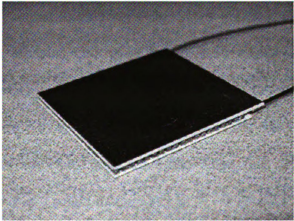


Figure 1.6 One TEG module G1-1.4-219-1.14 from Tellurex® Corp

Figure 1.7 shows the TEG module heating and testing system flowchart. And this system was used to measure the steady-state and dynamic response of TEG modules. By taking advantage of thermo-coupler as the temperature sensor, a temperature PID controller can be used to adjust a solid state contactor to control the power flow from the AC power supply to the heating elements of the TEG modules. And in this way, the temperature of the hot plate accurately controlled. By using this temperature close loop control, stable hot plate temperature could be achieved when the steady state and dynamic response of TEG modules are tested.

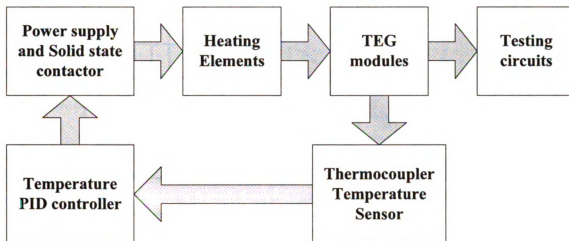


Figure 1.7 TEG module heating and testing system

Figure 1.8 shows the measured steady-state electrical output characteristics of a single TEG module. Three thermal conditions were tested and the V-I curves are plotted. During tests, the heat exchanger hot plane temperature is controlled to 150°C, 115°C, 79°C; the heatsink temperature are 27°C, 29°C, and 31°C, respectively. From the three curves shown in Figure 1.8, the internal resistances of the TEG modules under those thermal conditions are calculated and are 3.5Ω, 3.9Ω, and 4.2Ω, respectively. The maximum power output of a single module at 150 °C is about 4.5 W. From the plotted

V-I curve of the TEG module, the TEG module can be modelled as an ideal voltage source with internal resistance shown in Figure 1.9

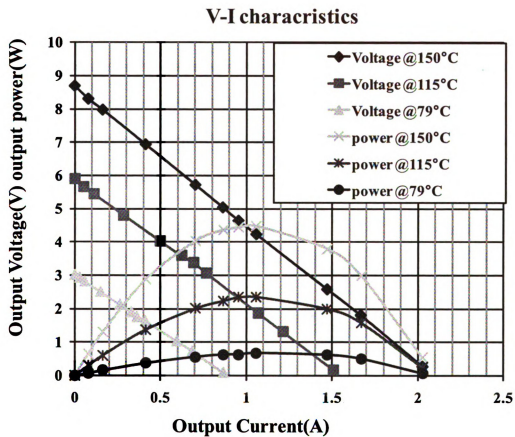
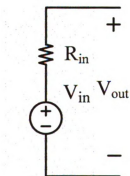


Figure 1.8 TEG module steady-state testing results



TEG module

Figure 1.9 Electrical equivalent circuit of one TEG module.

Figure 1.10 shows the test circuit of the electrical characteristics of the TEG module's dynamic behaviors. Figure 1.11 shows the captured single TEG module output voltage and current waveforms. Test results reveal that the TEG module has a very fast dynamic response and it will not influence the converter design. Because the TEG module output current can increase in the range of nanoseconds and the switching speed of DC-DC converter is usually in the range of 50K~1MHz, the switching period will be 1 μ s~20 μ s. So, the ideal voltage source with the internal resistance model can represent the TEG steady state and dynamic model very well.

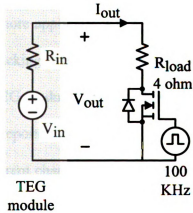


Figure 1.10 TEG module dynamic test circuit

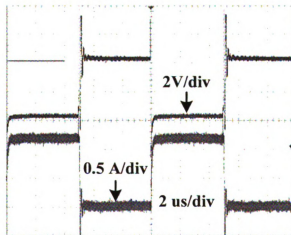


Figure 1.11 TEG module output waveforms

1.2 Power Electronic Challenges for TEG

Initially, the TEG module output voltage and power will change distinctly with the temperature gradient, which means it cannot output stable voltage or constant current. In order to utilize the TEG modules as the power source, a power conditioning circuit as interface between the TEG module and loads is needed. In order to solve this problem, the electrical characteristic of the TEG module should be modeled for circuit analysis and design. Some modeling method has been previously proposed [11]. Some DC-DC converter circuits have been investigated to output stable voltage and improve the TEG module power condition for more applications [12, 13]. And some control methods such as Maximum Power Point Tracking (MPPT) and constant voltage control have also been investigated to apply to the TEG module [14]. The TEG modules have also been used for battery charging applications reported in [15].

Moreover, due to the inherent characteristics of the materials making TEG modules, bigger pellets with larger heat conduction areas can produce high output current with the same output voltage compared to the smaller pellets with smaller conduction areas [5, 7, 8]. At the same time, by using the same amount of materials to manufacture TEG modules, it is much easier to manufacture bigger pellets. That means, in order to output the same amount of power, it is much easier to produce a TEG module with low output voltage and high output current than a low output current and high output voltage version. The reliability and the total heat-electricity conversion efficiency of the high output current and low output voltage module is also much higher than the low output current and high output voltage version, because the latter one needs more small pellets in series. By putting more pellets in series means more electric connectors are needed, which will

cause the increase of the internal resistance of the whole TEG module, and the reliability of the whole module will also reduce accordingly. Therefore, the low output voltage with high output current TEG modules are preferred in the manufacturing process and application. And this features add special challenges to the power electronics interface circuit design. Following provides the power electronics circuit requirements for the TEG module interface and some challenges in the circuit design for automotive application:

TEG module interface circuit requirements:

- Maximum power point tracking control
- Constant output voltage or current control

TEG module interface circuit design challenges for automotive application

- Low input voltage
- High input current
- High voltage conversion ratio
- High temperature operation
- High efficiency
- Small size

Among these challenges, the low input voltage, high input current, and high voltage conversion ratio are the requirements from TEG modules, and high temperature operation and small size are the features preferred by the automotive application. And high efficiency is always a preferred feature.

In order to meet all these requirements, traditional step-up dc-dc converter with a transformer or coupled inductor for high voltage conversion ratio applications are

reviewed in the following discussions. Switched-capacitor dc-dc converter topologies for the automotive application are also summarized; drawbacks of each circuit are addressed.

1.3 Summary of Previous Works

1.3.1 Traditional Step-up DC-DC Converter

Traditional step-up dc-dc converter utilizes the inductor charging and discharging to boost the voltage. We will discuss the basic step-up circuit topology from the very beginning to the improvements of them proposed recently.

1.3.1.1 Boost dc-dc converter

Figure 1.12 shows the traditional boost dc-dc converter. There are several benefits of the traditional boost converter. The structure of the traditional boost converter is simple. There are only one switch S , one diode D_o , one inductor L , and one capacitor C_o . The control and gate drive of this circuit is also very simple, only one switch needs to be controlled and gate drive shares the same ground with the input voltage source. The input current ripple is small; the total cost of the circuit is also relatively low. Because of these good features of traditional boost circuit, it has more and more applications in normal dc-dc step-up applications with voltage gain less than three and power factor correction (PFC) circuit [16, 17].

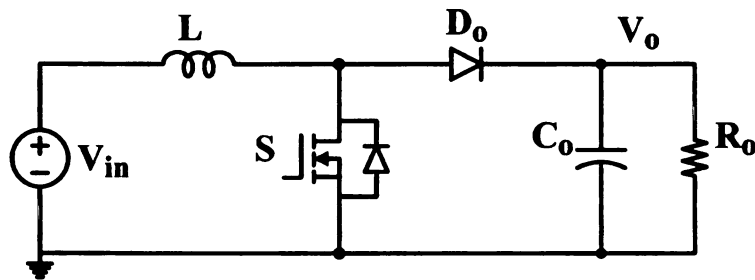


Figure 1.12 Traditional boost dc-dc converter.

Theoretically, the traditional boost dc-dc converter has infinite voltage gain, but considering the internal resistance of switch and inductor, the voltage gain of the boost converter is limited [18]. Figure 1.13 shows the boost converter circuit configuration considering the internal resistance of the inductor R_L . Actually, R_L is also can be considered as the whole circuit power loss equivalent resistance. By considering the internal resistance of the boost converter, the new voltage gain can be expressed as follows:

$$V_{gain} = \frac{V_o}{V_{in}} = \frac{1}{(1-D)(1 + \frac{R_L}{R_o(1-D)^2})} \quad (1.1)$$

Figure 1.14 shows the voltage gain curve vs. duty cycle considering the internal equivalent resistance describe as equation (1.1). With the increase of the equivalent resistance to the load resistance ratio, the voltage gain of the boost converter reduced accordingly. When the $R_L / R_o = 0.01$, which means the total power loss of the converter is 1%, the boost converter can achieve five times voltage gain. In the real application, the equivalent resistance is usually larger the 1%, which means for a regular boost converter, it is nearly impossible to achieve a voltage gain higher than five.

In order to solve the hard switching problem of the traditional boost converter and reduce the switching loss and solve the reverse recovery problem of the diode. Some soft switching strategies have been proposed [19, 20, 21, 22, 23]. Adding an active clamp circuit or passive clamp circuit to achieve the soft switching of the main switch can reduce the switching loss and improve the converter efficiency. The diode reverse recovery current is also restrained effectively. But these improvements are only for the

boost converter in regular applications. The voltage gain of these converters is not improved.

Moreover, if the power rating of the boost converter is increased, or if the input current rating is increased, a huge inductor with high current rating has to be used; more devices have to be put in parallel to meet the current rating requirements. However, because of the negative temperature coefficient of the diode and IGBT, when many devices are paralleled together, the current will not equalize with each other. Some of the devices may flow more and more current than others until burn out. Therefore, In order to increase the input current rating of the boost converter, interleaving strategy has to be used.

1.3.1.2 Interleaved boost dc-dc converter

Interleaved boost dc-dc converter are proposed to increase the input current rating and power rating of the boost converter [24, 25, 26, 27, 28, 29, 30, 31]. Figure 1.15 shows the two-phase interleaved boost dc-dc converter with higher input current rating. By the interleaving several phase of boost converter together, the current can be shared with each phase equally automatically, the input current ripple could also be reduced significantly. The converter dynamic response could be increased. The input inductor size could also be reduced accordingly [29, 32, 33, 34, 35]. Figure 1.16 shows ripple reduction effect as a function of duty cycle [34]. For an N-phase boost dc-dc converter, the current ripple cancellation effect K_I can be qualified as:

$$K_I = \frac{\Delta I_L}{\Delta I_{LS}} = \frac{N(D - \frac{m}{N})(\frac{m+1}{N} - D)}{D(1-D)} \quad (1.2)$$

where $m = \text{floor}(ND)$ is the maximum integer that does not exceed the ND . N is the number of phase interleaved together, and D is duty cycle. At some of the duty cycle point, the current ripple of multi-phase boost converter can be eliminated.

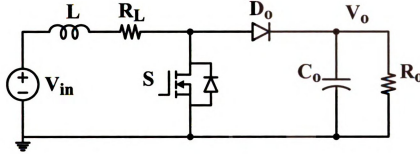


Figure 1.13 Boost converter considering internal resistance.

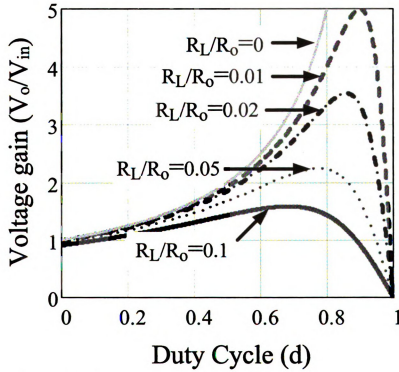


Figure 1.14 Voltage gain vs. duty cycle considering power loss.

For a traditional boost dc-dc converter, the current ripple can be expressed by:

$$\Delta I_{LS} = \frac{V_{in} D}{L f_s} \quad (1.3)$$

where V_{in} is the input voltage, L is the inductance value, f_S is the switching frequency and ΔI is the current ripple. The current ripple is poor when a very large duty cycle is present. The large duty cycles further increase the input current ripples by increasing the individual inductor current ripples, as can be seen from equation (1.3). Substituting equation (1.3) into equation (1.2), the magnitude of the output current ripples for multiphase boost converters can be easily derived, as follows:

$$\Delta I_L = K_I \Delta I_{LS} = \frac{V_{in}}{Lf_S} \frac{D(1 - \frac{m}{N})(\frac{m+1}{N} - D)}{D(1 - D)} \quad (1.4)$$

By setting $\frac{V_{in}}{Lf_S}$ equal to 1, we can derive the normalized input current ripple equation.

Figure 1.17 shows the relationship of normalized input current ripple curve with duty cycle and number of phase interleaved in equation (1.4). It can be shown from the curve that, even for the four-phase interleaved boost dc-dc converter, the best operation point is around 0.75 duty cycle. When the duty cycle is increased for the high voltage gain application, the input current ripple will increase accordingly. And the benefits of the interleaved strategy will disappear too. Besides, for the traditional interleaved boost dc-dc converter, the main switches still switch with hard switching, the switching loss of the main switch is still quite huge, and the diode also have sever reverse recovery problem. And the efficiency of the whole converter is low.

In order to increase the efficiency of the interleaved boost dc-dc converter, reduce the switching loss and solve the voltage spike problem of the diode caused by the diode reverse recovery. Some soft-switching strategy has been proposed [36].

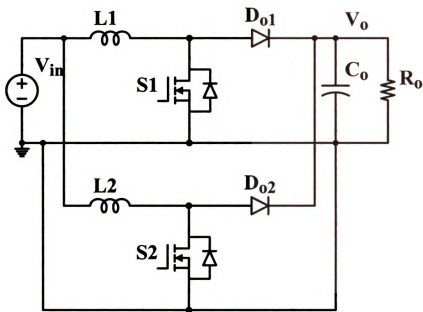


Figure 1.15 Two-phase interleaved boost dc-dc converter.

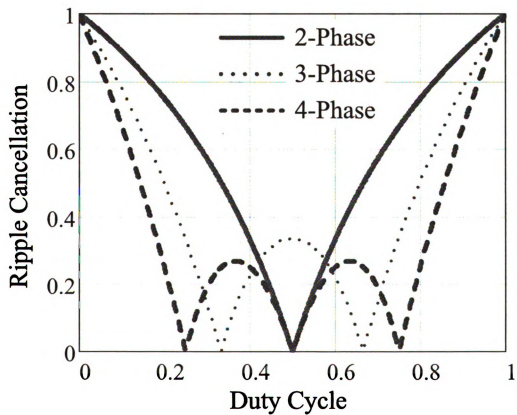


Figure 1.16 Current ripple cancellation in multiphase boost converters.

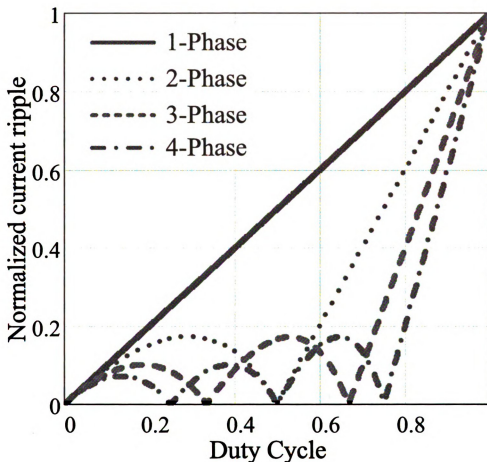


Figure 1.17 Normalized input current ripple with duty cycle and the number of interleaved phase.

Figure 1.18 shows the two-phase interleaved boost converter with an active clamp resonant zero current transition (ZCT) network [36]. By using an active switch with an inductor and a capacitor, the main switch can achieve zero current turn on using critical conduction mode. Zero current and zero voltage during turn off can be achieved using the resonant network. In this case the main switch voltage stress is reduced. The output diode reverse recovery problem can also be solved using the resonant network. However, in order to maintain the critical conduction operation, switching frequency has to be

changed accordingly. This will obviously increase the control complexity and increase difficulty of the EMI filter design

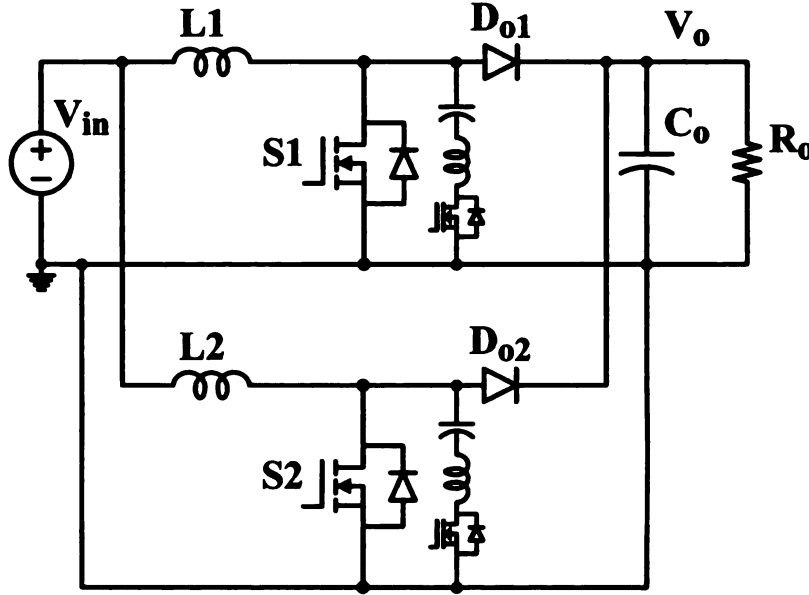


Figure 1.18 Two phase interleaved boost converter with active clamp ZCT network.

Using coupled inductor for the interleaved boost dc-dc converter can reduce the inductor size, and achieve the main switch zero current switching and suppress the diode reverse recovery current [29, 31, 32, 33, 35, 37, 38, 39, 40]. There are two different coupling method, common mode coupling and differential mode coupling shown in Figure 1.19 and Figure 1.20. Both method could realize the zero current turn on of the main switch, and solve the reverse recovery problem of output diode. The common mode coupled method could reduce the current ripple of main switch, and reduce the conduction loss of the switch. But the main switch turn off at hard switching, which will have high switching loss. The differential mode coupled method has larger current ripple, because the circuit operates at discontinuous mode. This will increase the conduction loss of the main switch. But the main switch can achieve zero current switching when the switch turns off. These two different coupling methods have their own features, and

which coupling method should be chosen depends on the specific application and circuit design trade off.

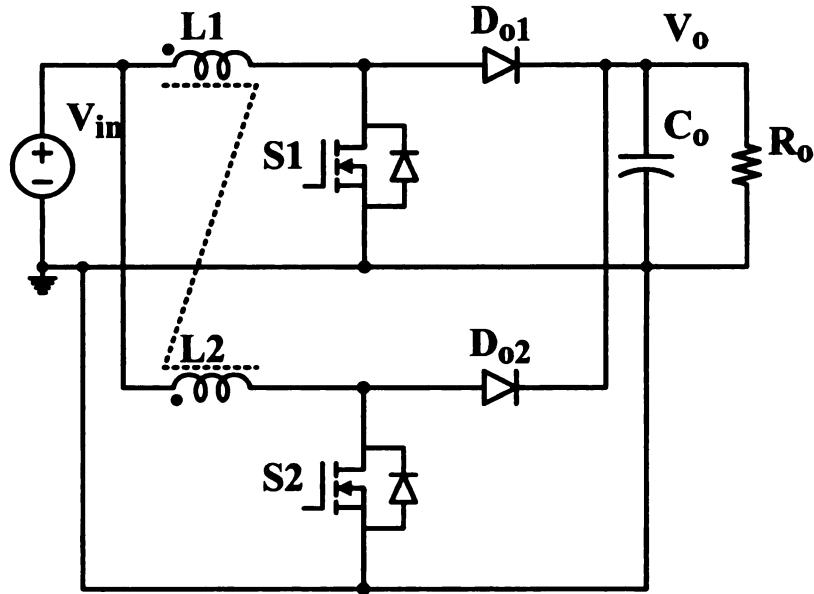


Figure 1.19 Common mode coupled interleaved boost dc-dc converter.

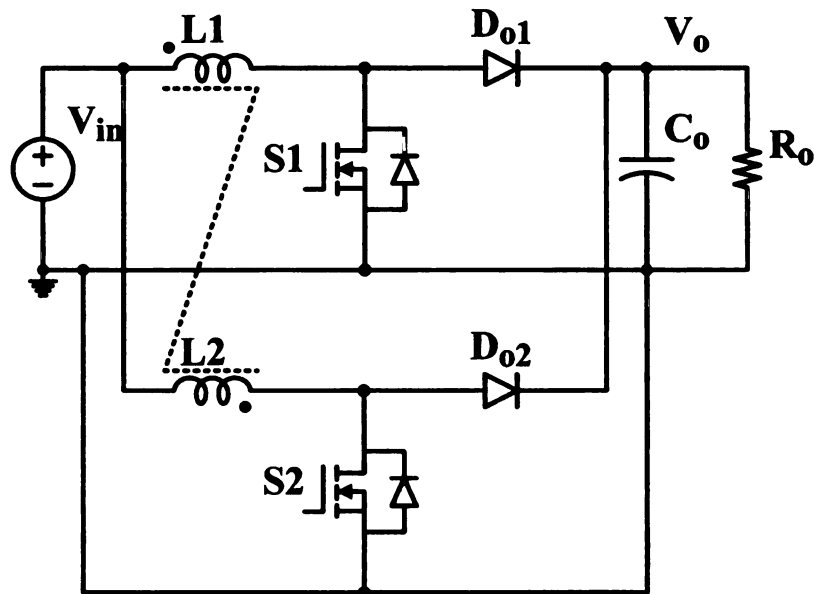


Figure 1.20 Differential mode coupled interleaved boost dc-dc converter.

In order to maintain the low conduction loss features of common mode couple interleaved boost dc-dc converter and overcome the hard switching turn off problem. An

active clamp soft switching strategy has been proposed recently [31, 41, 42, 43]. Figure 1.21 shows the common mode coupled inductor interleaved boost dc-dc converter with active clamp circuit. By using two active clamp switches, the main switch can achieve zero voltage turn off. The introduction of the active clamp switch also reduces the voltage stress of the main switch. The active clamp switch can achieve zero voltage turn on and turn off, no inductor need to be added too. The control and gate drive of the active clamp switch is also easy to implement. This circuit is suitable for regular voltage boost operation with normal voltage gain.

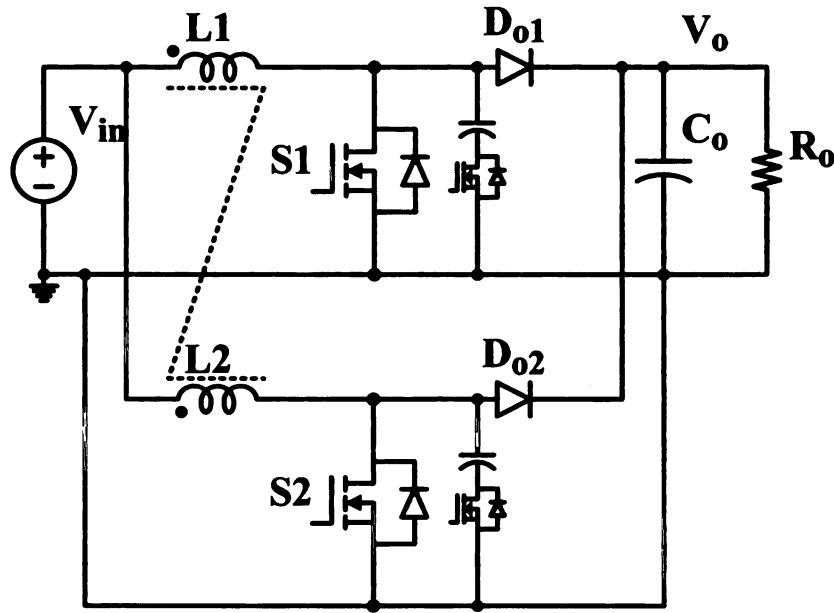


Figure 1.21 common mode coupled inductor interleaved boost dc-dc converter with active clamp.

The interleaved boost dc-dc converter can increase the input current rating and the converter power rating effectively. The input current ripple can be reduced significantly by choosing proper duty cycle and the number of interleaved phase. By using the coupled inductor strategy, the inductor size can also be reduced. However, the interleaving

technique does not increase the converter voltage gain; other techniques have to be used to increase the converter conversion ratio.

1.3.1.3 Multilevel boost dc-dc converter

In order to reduce the voltage stress of main switch and increase voltage gain of the boost converter. Three-level boost dc-dc converter and N-level boost dc-dc converter are proposed [44, 45, 46, 47, 48, 49]. Figure 1.22 shows the three-level boost dc-dc converter. Figure 1.23 shows the N-level dc-dc boost converter. In the high voltage output application, using multilevel structure can reduce the voltage stress of each switch, where low voltage devices could be used.

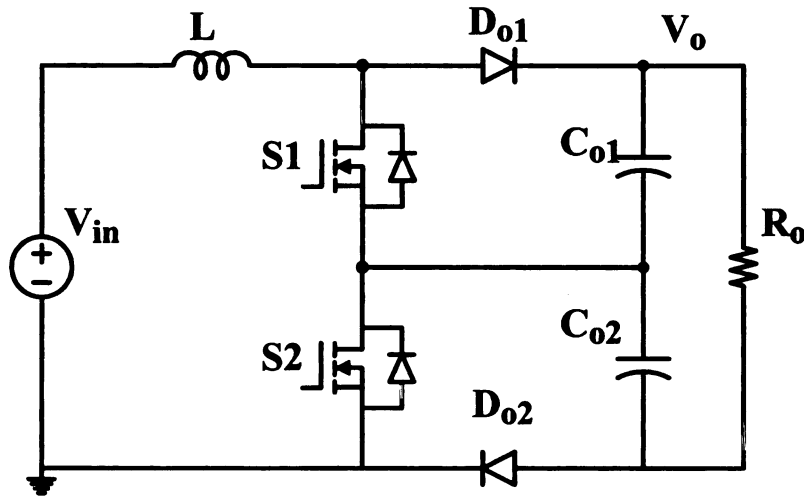


Figure 1.22 Three level boost dc-dc converter.

However, by using the multilevel structure will not increase the voltage gain of the converter assuming $\frac{R_L}{R_o}$ is the same. In reference [48], the voltage gain equation considering the influence of R_L has been mentioned as follows:

$$V_{gainN} = \frac{1}{\frac{1-D}{N_L} + \frac{N_L}{1-D} \frac{R_L}{R_o}} \quad (1.5)$$

Where N_L is number of levels.

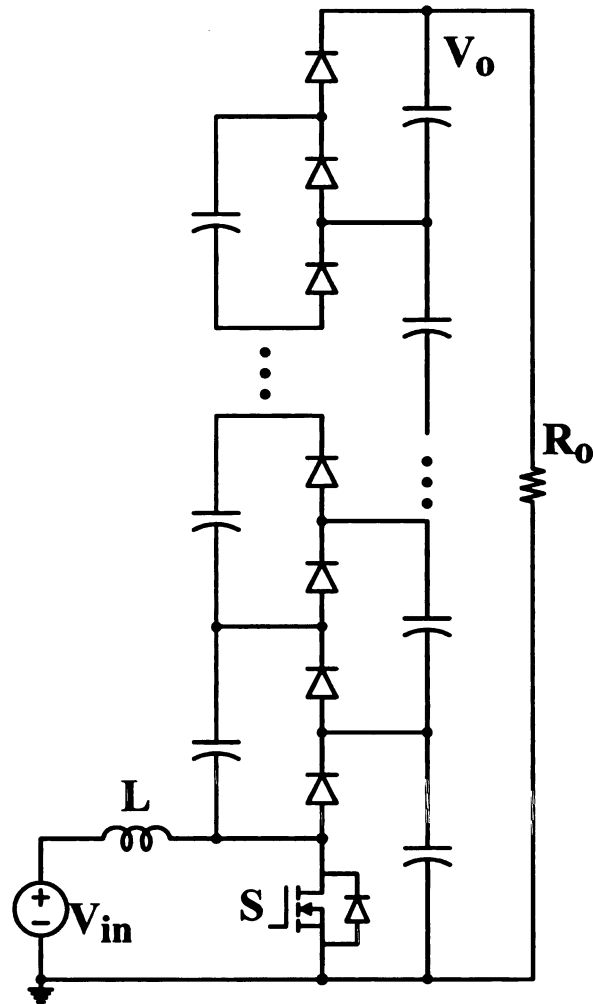


Figure 1.23 N-level boost dc-dc converter.

Figure 1.24 shows the voltage gain curve by change number of level and duty cycle described in equation (1.5) assuming $\frac{R_L}{R_o} = 0.01$. It can be seen from the curve that, with the increase of number of levels, the maximum voltage gain will not change. The duty cycle of maximum output voltage has been reduced, which will increase the dynamic response of the converter.

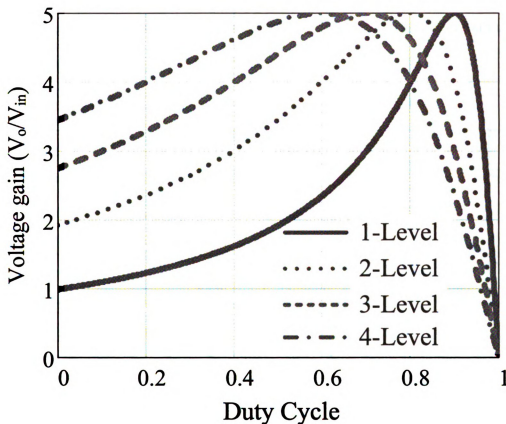


Figure 1.24 Multilevel boost dc-dc converter voltage gain curve considering internal resistance.

In order to achieve high efficiency, and minimize the switching loss, several soft-switching strategies have been proposed by adding an auxiliary circuit [50, 51, 52]. However, because of the inherent characteristics of multilevel boost converter, the voltage gain of the converter is not increased, and not suitable for high voltage gain application. By cascading multilevel boost converter, some other converter topologies have been proposed [53]. Figure 1.25 shows the cascade three level boost dc-dc converter. By cascading two boost dc-dc converters together, the voltage conversion ratio is doubled obviously, and the device voltage stress of the first stage is reduced, the device current stress of the second stage is also reduced. However, the cascaded boost converter needs

two sets of power devices, two inductors, and two sets of control circuits. The control signal of the two different control chips has some difference, the total system may have stability problem [54, 55].

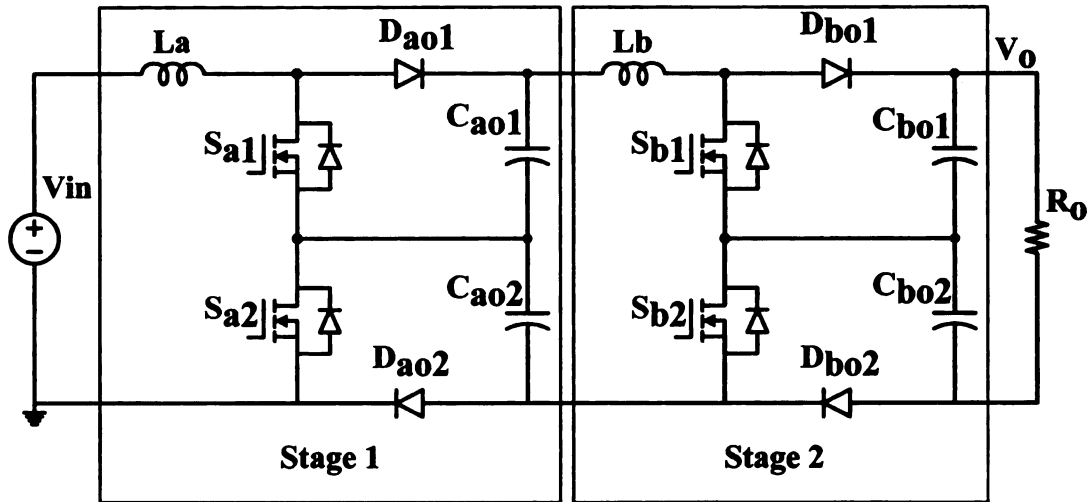


Figure 1.25 Cascaded three level boost dc-dc converter.

The multilevel boost dc-dc converters reduce the device voltage stress by using multilevel technique, but the voltage gain is not increased as expected considering the internal resistance. In order to increase the voltage gain of the boost converter, other techniques, such as coupled inductor have to be used.

1.3.1.4 Coupled inductor boost dc-dc converter

Flyback transformer actually is a coupled inductor. If the circuit does not require the isolation, a non-isolated flyback transformer or coupled inductor could be used. By adding a non-isolated flyback dc-dc converter with a boost converter. A high voltage gain coupled inductor boost dc-dc converter can be derived [56, 57, 58, 59, 60, 61, 62, 63]. Figure 1.26 shows the boost flyback step-up dc-dc converter. The output voltage is the sum of a flyback converter which consists of $L1/L2$, $D1$, $C1$ and S , and a boost converter

which consists of L_1 , S , D_2 , and C_2 . Since the flyback output is $V_o = V_{in} \frac{nD}{1-D}$ and boost output is $V_o = V_{in} \frac{1}{1-D}$, the total output voltage is $V_o = V_{in} \frac{1+nD}{1-D}$. Here, n is the turns ratio between the secondary and primary, and D is the switch duty cycle. When the switch S is turned on, the energy is stored in L_1 , and when S is turned off, the energy is released to charge both C_1 and C_2 through diodes D_1 and D_2 . The problem is when S turns on these diodes need to be turned off, and a parasitic capacitance across D_1 and the leakage inductance can cause severe ringing and additional voltage stress on D_1 .

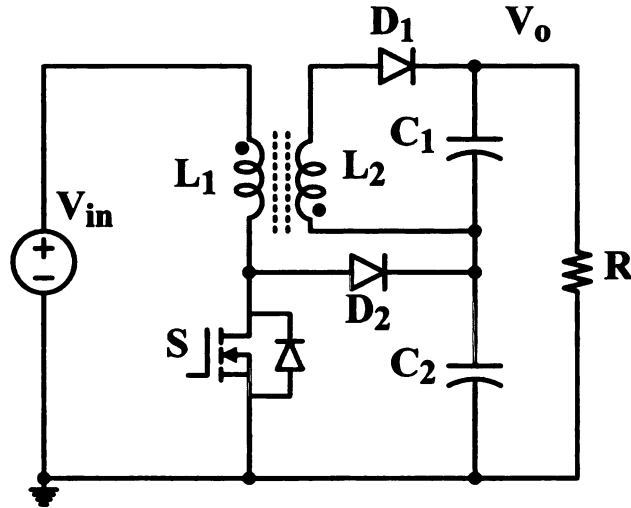


Figure 1.26 Boost flyback step-up dc-dc converter.

In order to solve the diode voltage spike problem of boost flyback step-up dc-dc converter, some other topologies have been proposed using capacitor coupling or charge pump circuits [63, 64, 65, 66, 67]. Figure 1.27 shows the improved boost flyback dc-dc converter with coupling inductor between the primary side and secondary side of the transformer. A diode is added between boost output and secondary of the flyback winding to circulate the energy, as shown in Figure 1.27. The added capacitor, C_1 , stores the energy when the switch S is turned on and maintains a constant voltage related to the

turns ratio n , duty cycle D , and input voltage V_{in} . During switch-off state during which D_1 and D_3 conduct, C_1 energy is released to output, and the output voltage equals the sum of the two capacitor voltage and the secondary winding voltage. If the leakage inductance is negligible, then the output voltage equals $V_o = V_{in} \frac{2+n}{1-D}$. Compared with the version with combination of flyback and boost converters, this circuit allows a higher-voltage boost ratio, and thus the turns ratio or duty cycle can be reduced for the same output voltage.

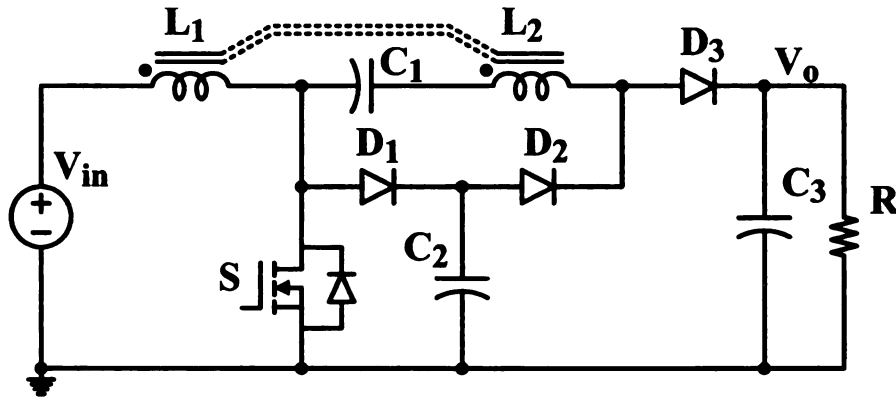


Figure 1.27 Improved boost flyback dc-dc converter with capacitor coupling.

The circuit shown in Figure 1.27 has the problem to filter out the low frequency ripple in the input side if a large inductor is not used in the high voltage dc link. Another improvement of boost flyback dc-dc converter has been proposed by combining the boost flyback with a charge pump circuit shown in Figure 1.28. Compared to the circuit shown in Figure 1.27, this circuit sacrifice some voltage gain to achieve the wide input voltage range operation. Moreover, this circuit have to insert a small inductor to limit the inrush current of the charge pump. The output voltage of this circuit is $V_o = V_{in} \frac{2+nD}{1-D}$.

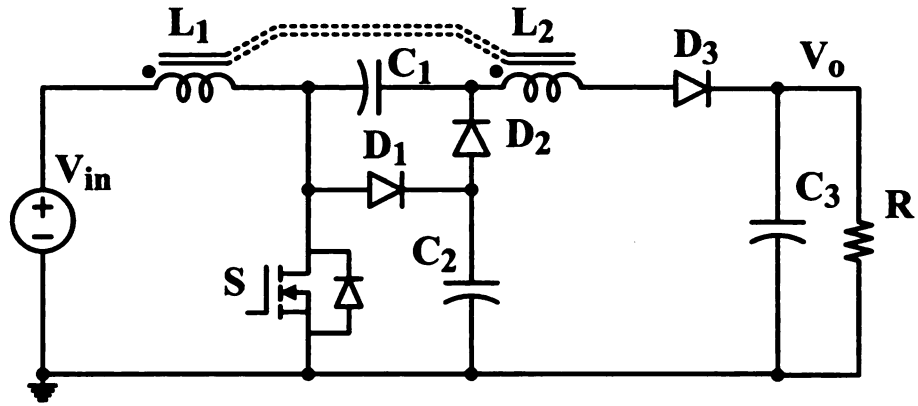


Figure 1.28 Improved boost flyback dc-dc converter with charge pump.

In order to increase the input current rating of the boost flyback dc-dc converter, an interleaved three coupled inductor boost dc-dc converter are proposed [31, 68, 69, 70, 71, 72] shown in Figure 1.29. The extra inductor is added in order to simplify the circuit small signal mode to a boost converter, and the close loop control circuit design is becoming easy.

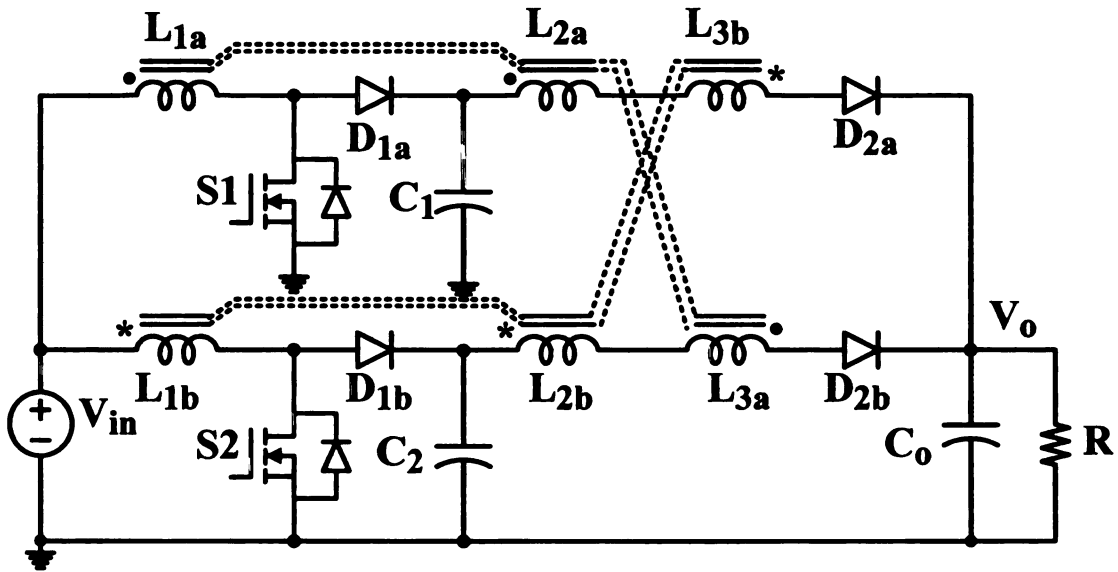


Figure 1.29 Interleaved three coupled inductor boost flyback dc-dc converter

Figure 1.30 shows the ideal voltage gain curve of boost flyback and its improvements when the transformer conversion ratio $n=3$. By using a coupled inductor the voltage gain of the converter can be improved significantly.

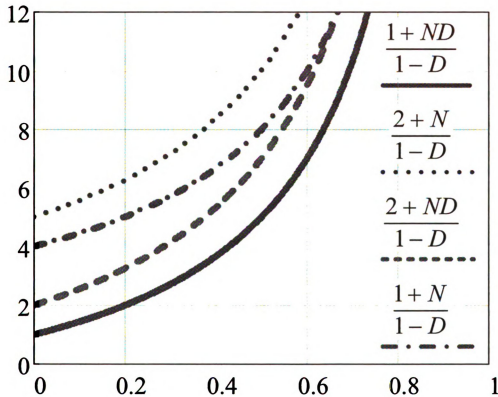


Figure 1.30 Ideal voltage gain curve of boost flyback and its improvements.

In conclusion, for the traditional step-up dc-dc converter, there are several limitations related to the high voltage gain and high current applications. Coupled inductor has to be used in order to increase the converter voltage gain. Interleaved strategy has to be used in order to increase the converter input current rating. Active-clamp or passive devices clamp strategies have to be used to ease switching, reduce the switching loss and increase the converter efficiency. Moreover, if the converter input current rating is increased, more and more interleaved circuits have to be used, which will obviously increase the

complexity of the control and gate drive. Besides, more and more inductors in parallel are hard to couple and increase the difficulty of circuit layout. And because of the leakage inductance and the internal resistance of the coupled inductor, the converter voltage gain will be limited too.

Furthermore, all the traditional step-up dc-dc converters have to utilize coupled inductors or transformers for the high voltage gain application. And the magnetic components are usually the most bulky and lossy part in the converter. Also, in high temperature automotive application, the magnetic parts become dysfunctional. So, in order to achieve small size, high efficiency dc-dc converters with high temperature operation features, magnetic-less switched-capacitor dc-dc converter is needed to be considered. Traditional switched-capacitor dc-dc converter is going to be reviewed in next section. Problems related to the traditional switched-capacitor dc-dc converter will be addressed and discussed. New soft-switching strategy will be proposed to solve the traditional circuit limitations and improve the circuit performances in next three chapters.

1.3.2 Switched-Capacitor DC-DC Converter

Switched-capacitor dc-dc converters have been proposed since 1970s due to their integration capability and small size, light weight features. The three basic structures of switched capacitor dc-dc converter will be discussed in detail in the following parts. The advantages and disadvantages of each structure will be addressed and discussed. The appropriate structure for high voltage gain and high current TEG application will be summarized.

1.3.2.1 Marx converter type switched-capacitor voltage multiplier

Figure 1.31 shows the traditional switched-capacitor voltage multiplier structure [73, 74, 75]. The control signal of switched-capacitor voltage multiplier is complementary, and duty cycle can be set as 50% duty cycle or other value to achieve some voltage regulation. The voltage stress of the capacitor $C_1 \sim C_{N-1}$ is the input voltage. When the conversion ratio is high, low voltage rating capacitor can be used, which can reduce the converter size. The current stress of the capacitor $C_1 \sim C_{N-1}$ is the same, which means same current rating capacitor could be used. The current stress of all the switching devices is also the same, which means the same current rating switching devices could be used. However, the voltage stress of the switching devices increases as the conversion ratio increases. When the output voltage is low (less than 60 V), this is not a problem. However, when the output voltage is high, high voltage rating devices have to be used in the output side. However, the turn on resistance of high voltage switching devices is much higher than the low voltage devices, so this structure is not suitable for the high output voltage applications.

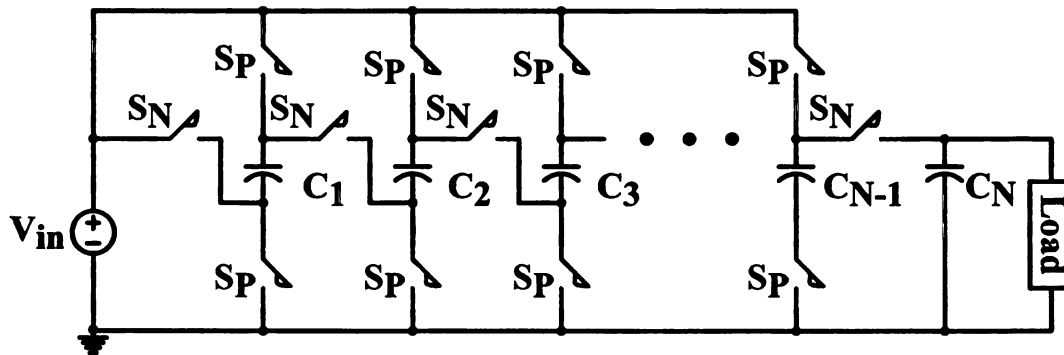


Figure 1.31 Traditional switched-capacitor voltage multiplier.

1.3.2.2 Dickson charge pump type multilevel modular switched-capacitor dc-dc converter

Figure 1.32 shows the traditional Dickson charge pump type multilevel modular switched-capacitor dc-dc converter [76, 77, 78, 79, 80]. The control signal of this type converter is complementary with 50% duty cycle which is very easy to implement. The current stress of all the switches and capacitors are the same, which means same current rating device could be used. And when the current rating of the converter is increased, the current through each devices could be equally distributed thus making this converter especially suitable for the high current application. The voltage stress of the switches is one or twice the input voltage, which is also relatively low, when the conversion ratio is high. However, for this converter, the capacitor voltage stress is increased with the increasing of converter voltage gain. When the output voltage is high, a high voltage stress capacitor has to be employed. Therefore, this structure is suitable for the relatively low output voltage (less than 100 V), high current, high voltage gain application.

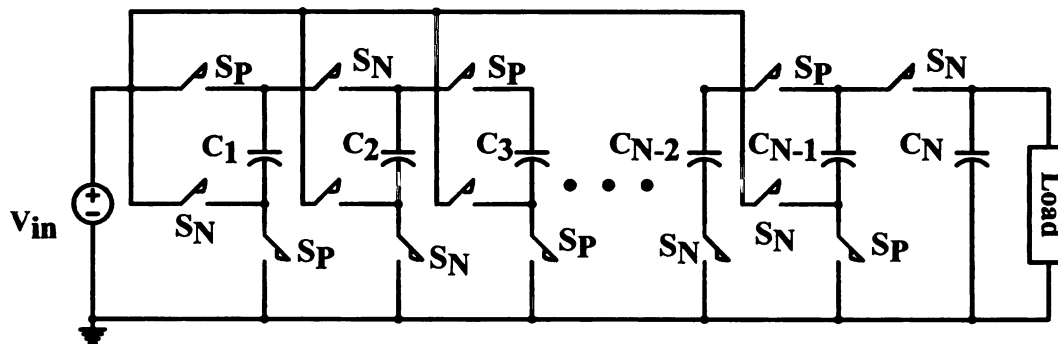


Figure 1.32 Traditional multilevel modular switched-capacitor dc-dc converter.

1.3.2.3 Generalized multilevel switched-capacitor dc-dc converter and the derivative circuits

Figure 1.33 shows the generalized multilevel switched-capacitor dc-dc converter [81, 82, 83].

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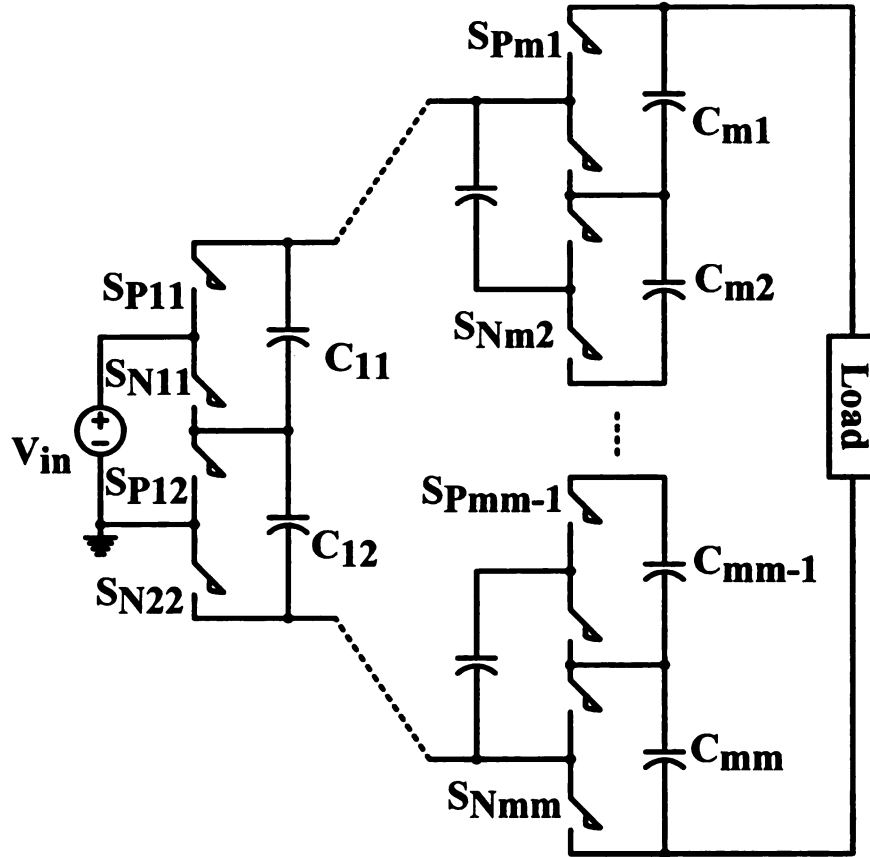


Figure 1.33 Traditional generalized multilevel switched-capacitor dc-dc converter.

Figure 1.34 shows the one three level generalized multilevel converter derivation circuit. Figure 1.35 shows some other derivation by reducing the capacitor and switch numbers. The device voltage stress of the generalized switched-capacitor dc-dc converter is as the same as the input voltage. The capacitor voltage stress of circuit shown in Figure 1.33, Figure 1.34 and Figure 1.35(b) are also the same, which is the input voltage. The structure shown in Figure 1.35(b) is also known as the Cockcroft-Walton generator. The capacitor voltage stress of the derivation circuit shown in Figure 1.35(a) increases with the conversion ratio. Because of the low voltage stress features of the generalized switched-capacitor dc-dc converter, this type of converter is suitable for the very high output voltage application. However, the current stress of this type of converter is not

equal, and the control signal is very complex with the increase of voltage level except the derivation shown in Figure 1.35(b) with complementary control signal. Consequently, this type of converter is not suitable for high current and high voltage gain application.

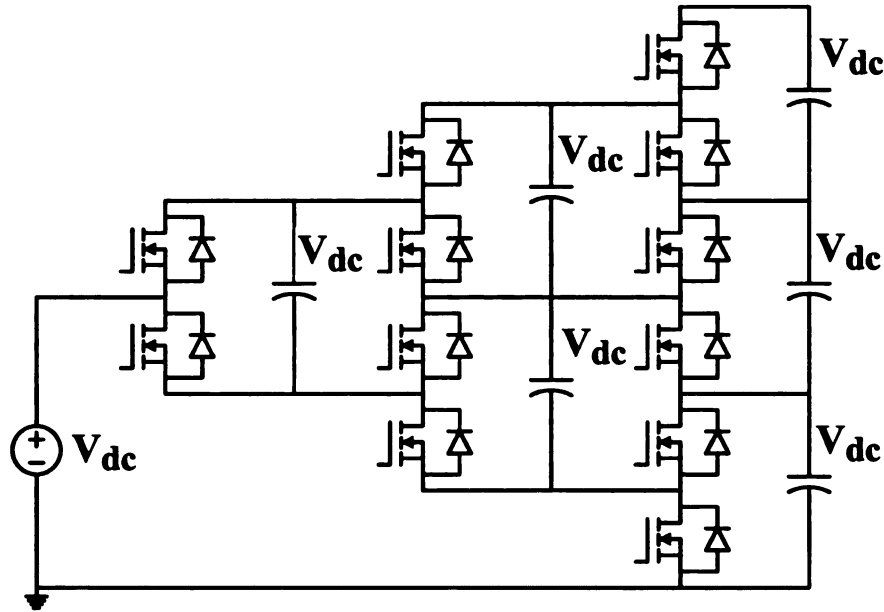


Figure 1.34 Three level generalized multilevel converter derivation.

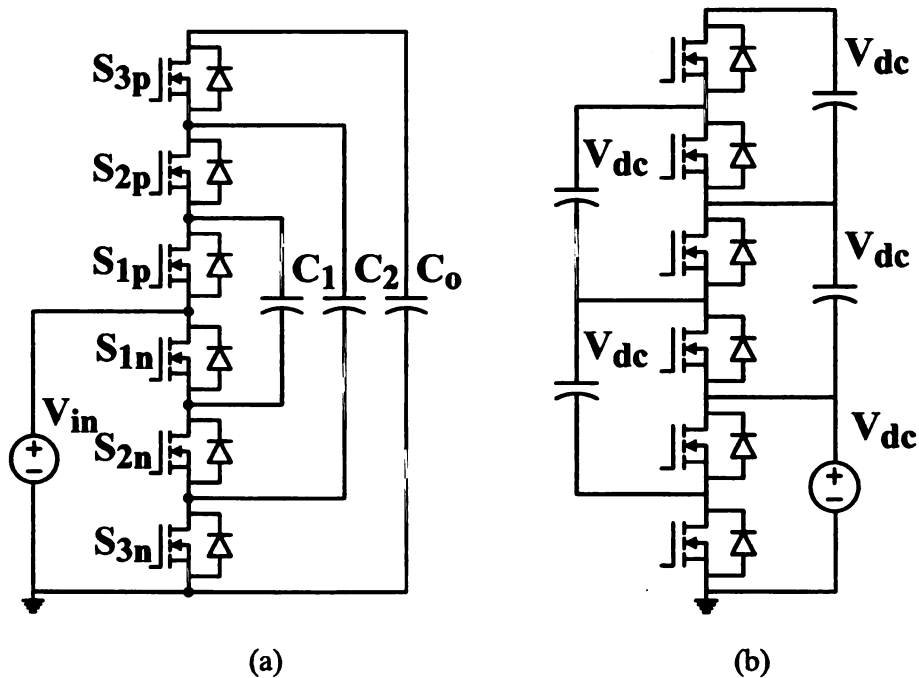


Figure 1.35 Some other three level generalized multilevel converter derivations.

In summary, the Marx converter type and charge pump type switched-capacitor circuits are suitable for the high current, high voltage gain application with output voltage relatively low. And the generalized multilevel type is more suitable for the high output voltage, low voltage gain, and low current application.

1.3.2.4 Traditional Zero current switching (ZCS) switched-capacitor dc-dc converter

But these traditional switched-capacitor dc-dc converter circuits have some common problems such as high voltage spike, high switching loss and EMI problem. In order to reduce the switching loss, high voltage spike and EMI, several ZCS switched-capacitor dc-dc converter have been proposed to solve the problem by inserting an inductor in series with the capacitor to achieve the ZCS of the main switches [84, 85, 86, 87, 88].

Figure 1.36 shows a four level switched-capacitor resonant converter as an example. By inserting an inductor L_r resonating with the capacitor C_{2a} , the ZCS of the main switches S_1 and S_2 can be achieved. The switching loss can be minimized, the voltage overshoot across the switching devices can be reduced and the EMI noise is also restricted. However, by inserting a relatively big inductor in the switched-capacitor circuit is a contradiction by itself which means many good features of switched-capacitor circuit will lose, such as good integration capability and high temperature operation. So the traditional ZCS method is not practical, new method need to be proposed.

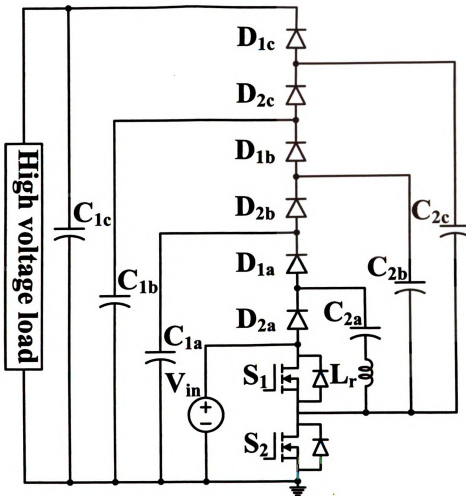


Figure 1.36 Four level switched-capacitor resonant converter main circuit.

1.4 Outline of Thesis

The goal of this research is to develop a high efficiency, small size, high voltage gain dc-dc converter with low input voltage and high input current features especially for TEG modules in automotive application. In this thesis, a new soft-switching strategy of realizing ZCS for switched-capacitor dc-dc converter has been proposed. By utilizing the stray inductance distributed in the circuit to resonate with the capacitor, the ZCS of all the switching devices can be achieved. By applying this strategy to the traditional switched-capacitor dc-dc converter, switching loss is minimized, huge di/dt , dv/dt and EMI noises

are reduced, high voltage spike problem is also solved. In this case, the efficiency and reliability of traditional switched-capacitor dc-dc converter would be improved. Several new ZCS switched-capacitor dc-dc converters have been proposed and analyzed.

Chapter 2: A ZCS multilevel modular switched-capacitor dc-dc converter (MMSCC) for high input current high voltage gain TEG application is proposed. By using the proposed ZCS strategy for MMSCC, the capacitor size is reduced, voltage overshoot is eliminated and EMI noise is restricted. Prototypes are designed and built. Simulation and experiment results are provided to validate the proposed topology.

Chapter 3: A family of ZCS switched-capacitor dc-dc converters is proposed and analyzed. By using the ZCS strategy, very high power density (above 300 W/in³) with high efficiency switched-capacitor dc-dc converters could be made by eliminating the lossy magnetic cores and bulky capacitor bank. Simulation and experiment results are provided to confirm the operation of proposed circuits.

Chapter 4: Other circuit improvements for the ZCS switched-capacitor dc-dc converter are proposed and analyzed. By using the proposed improved ZCS switched-capacitor dc-dc converter topologies, interleaved operation of ZCS switched-capacitor dc-dc converters become possible. The input current of ZCS switched-capacitor dc-dc converters becomes continuous due to the interleaving operation. In this case, the input capacitor size could be reduced significantly. Continuous input current is also preferable by many renewable energy sources. Simulation and experiment results are provided to validate the proposed topologies.

Chapter 5: Conclusions of the thesis. Contributions are summarized, suggestions for future work are provided.

CHAPTER 2

Zero Current Switching Multilevel Modular Switched-Capacitor DC-DC Converter for TEG Applications

This Chapter presents the quasi-resonant technique for multilevel modular switched-capacitor circuit (MMSCC) to achieve zero current switching (ZCS) without increasing cost and sacrificing reliability. This zero current switching multilevel modular switched-capacitor circuit (ZCS-MMSCC) employs the stray inductance existing in the circuit as the resonant inductor to resonate with the capacitor and provide low dv/dt and low switching loss for the device. The ZCS-MMSCC does not utilize any additional components to achieve ZCS and solves the voltage spike problem during the switching transition, thus leading to reliable and high efficiency advantages over traditional MMSCC. Furthermore, the ZCS-MMSCC reduces the capacitance needed the circuit; in this case, the bulky capacitors present in traditional MMSCC to attain high efficiency is not necessary any more. A 150 W four-level ZCS-MMSCC prototype has been built. Simulation and experimental results are given to demonstrate the validity and features of the soft switching switched-capacitor circuit.²

² This work was presented in part at the first annual IEEE Energy Conversion Congress and Expo, San Jose, CA USA, Sep.20 – Sep.24 2009 and an extended paper titled “Zero Current Switching Multi-level Modular Switched-Capacitor DC-DC Converter for TEG Applications” has been submitted to IEEE Transactions on Industry Applications.

2.1 Introduction

In order to obtain the high input current, high voltage gain, light weight, small size, high temperature high efficiency and high power density dc-dc converter for TEG in automotive application, switched-capacitor dc-dc converters have to be used as discussed in Chapter 1. Switched-capacitor circuits have been investigated since 1970s [76, 89]. Conventional Switched-Capacitor dc-dc converters have some common drawbacks: 1) weak output regulation ability and structurally determinate voltage conversion ratio; 2) pulsating input current and high current spike; 3) high voltage spike across the switching device; 4) high electromagnetic interference (EMI); 5) unidirectional power conversion ability. Many approaches have been proposed to achieve voltage regulation by using duty cycle control [75, 89, 90]. But all these methods have to sacrifice efficiency to achieve the voltage regulation, which is only acceptable in low power conversion field. Several zero current switching (ZCS) techniques by inserting an inductor to Switched-Capacitor circuit have been proposed to solve the voltage spike, current spike and EMI problem [84, 87, 88, 91]. However, by adding a relatively big resonant inductor into the switched-capacitor circuit to achieve ZCS is a contradiction by itself. Switched-capacitor circuit with a magnetic core is not a switched-capacitor circuit any more, and all the good features such as, high temperature operation, good integration, and small size will lose [92, 93].

Another type of switched-capacitor circuit, flying capacitor multilevel dc-dc converter (FCMDC) has become more and more popular recently because of the potential automotive application [83, 94, 95, 96, 97]. Nevertheless, there are several limitations of FCMDC, such as non-modular structure, complex control strategy and high conversion

ratio unreachability. When the conversion ratio is larger than five or more than five levels have to be used, the control of FCMDC is becoming very complex. The high current stress of the switching device of FCMDC also prevents it for high current application.

In order to solve the problems of FCMDC in high voltage conversion ratio, high current automotive application, multilevel modular switched-capacitor dc-dc converter (MMSCC) was proposed recently, shown in Figure 2.1[78]. MMSCC has modular structure, complementary control scheme, capability of reaching high voltage gain and reduced current stress of each switch and shows good application potential in automotive application [98]. Nevertheless, because MMSCC still use hard switching, there still exist several problems limiting its power rating such as huge current spike, huge voltage spike, high switching loss and sever EMI noise. With the increasing of power rating or current rating of the MMSCC, the voltage spike and switching loss problems become more and more serious. Also, in order to increase the total system efficiency, higher capacitance capacitors, aluminum electrolytic capacitors have to be used [78, 79, 96, 98]. The current rating and life time of the aluminum electrolytic capacitor is small to some extent. In order to meet the high current ripple requirement a huge capacitor bank has to be used, which will increase the size of the converter significantly. Multi-layer chip type ceramic (MLCC) capacitor has much better performance than the aluminum electrolytic capacitor, in current rating, equivalent series resistance (ESR), life time, and size in terms of current rating. But the capacitance of MLCC capacitor is very small, so it is not feasible to use MLCC capacitor for the traditional MMSCC.

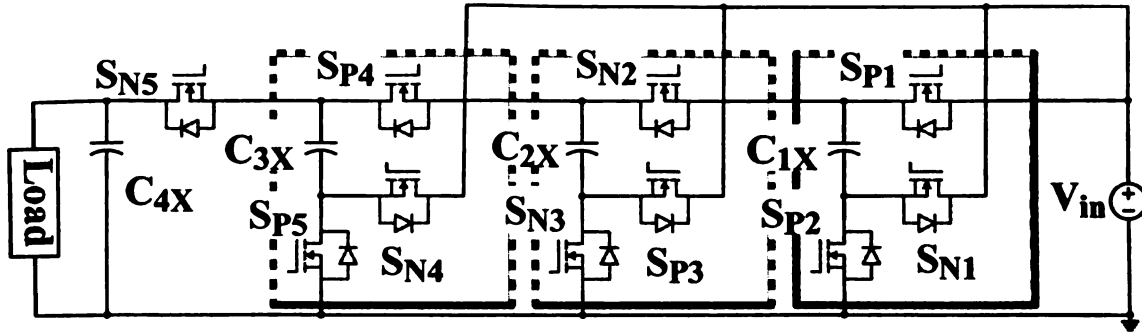


Figure 2.1 Four-level MMSCC with three modular blocks

This chapter presents a quasi-resonant technique for MMSCC that is able to achieve ZCS without increasing cost and sacrificing reliability. The proposed ZCS strategy employs the distributed stray inductances present in each module of the circuit resonating with the capacitors to provide zero current turn-on and turn-off to the devices. Because the MMSCC is especially suitable for high voltage gain with high input current application [78, 79, 80, 98, 99, 100], the ZCS version also inherit all the benefits from it. By using the ZCS, the switching loss of the traditional MMSCC is minimized, current spike, voltage spike and EMI is reduced. Besides the benefits gained from ZCS and MMSCC, the proposed ZCS-MMSCC has other special features:

- Different from other soft-switching techniques, this ZCS strategy does not use additional active devices or passive components, thus making it reliable and cost efficient.
- Because of the module structure, the required resonant inductance is quite small for each module, thus making it feasible to be realized by the distributed stray inductance existing in the circuits.
- The ZCS-MMSCC doesn't need high capacitance to achieve high efficiency like traditional MMSCC. In this case, small capacitance, high current rating, low ESR and small size MLCC capacitor could be used. The total size of the converter is reduced

significantly, the power density and the converter current rating is increased correspondingly.

Hence, the proposed ZCS-MMSCC solves aforementioned problems of traditional MMSCC and achieves ZCS without inserting big magnetic cores. For the same current rating and voltage gain, the ZCS version of MMSCC is smaller, higher power density, and higher efficiency than the traditional MMSCC. So the proposed ZCS-MMSCC is especially suitable to the high current high voltage gain automotive application. A 150 W four-level ZCS-MMSCC prototype was built to confirm the operation. A 630 W 5V input twelve-level ZCS-MMSCC prototype was built for the TEG interface in automotive battery charging application. Simulation and experimental results are given to demonstrate the validity and features of proposed ZCS-MMSCC.

2.2 Proposed Circuit Topology

Figure 2.2 shows the proposed four-level ZCS-MMSCC as an example. The circuit works as a four times step-up converter. Figure 2.3 shows the proposed ZCS-MMSCC converter modular block. The capacitor and the switch label is the same as the Figure 2.1 shown before.

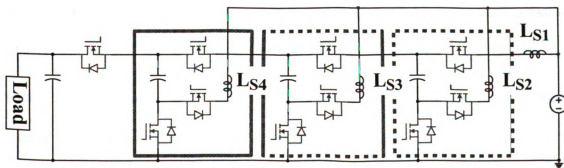


Figure 2.2 Four-level ZCS-MMSCC with three modular blocks

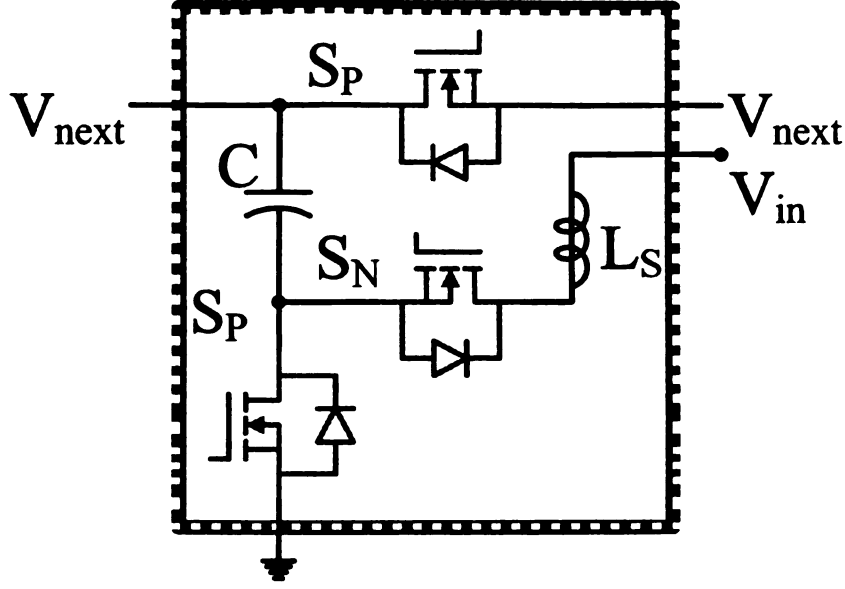


Figure 2.3 proposed ZCS-MMSCC modular block

By using $n-1$ modular blocks, a switch and a capacitor, n -level ZCS-MMSCC with n times voltage gain can be generated. V_{in} represents the ideal input voltage source. L_S represents the equivalent stray inductance present in each module of the circuit. S_P and S_N are the same switching devices controlled complementary at 50% duty cycle. C_{1X} to C_{4X} are the capacitors with the average voltage from one time to four times of input voltage. L_S does not have to be in the position drawn in Figure 2.2, it could be distributed anywhere in series with switches or capacitors in the circuit shown in Figure 2.4. It could be sum of the connection wire parasitic inductance L_{SW} , capacitor parasitic inductance L_{ESL} and the MOSFETs package parasitic inductance L_{Sp} . Usually the connection wire parasitic inductance L_{SW} is the major part of the stray inductance. Because all the stray inductance is in series when the current flows through. In each simplified equivalent circuit discussed in the next section, only one equivalent L_S is needed to represent the total stray inductance present in the circuit.

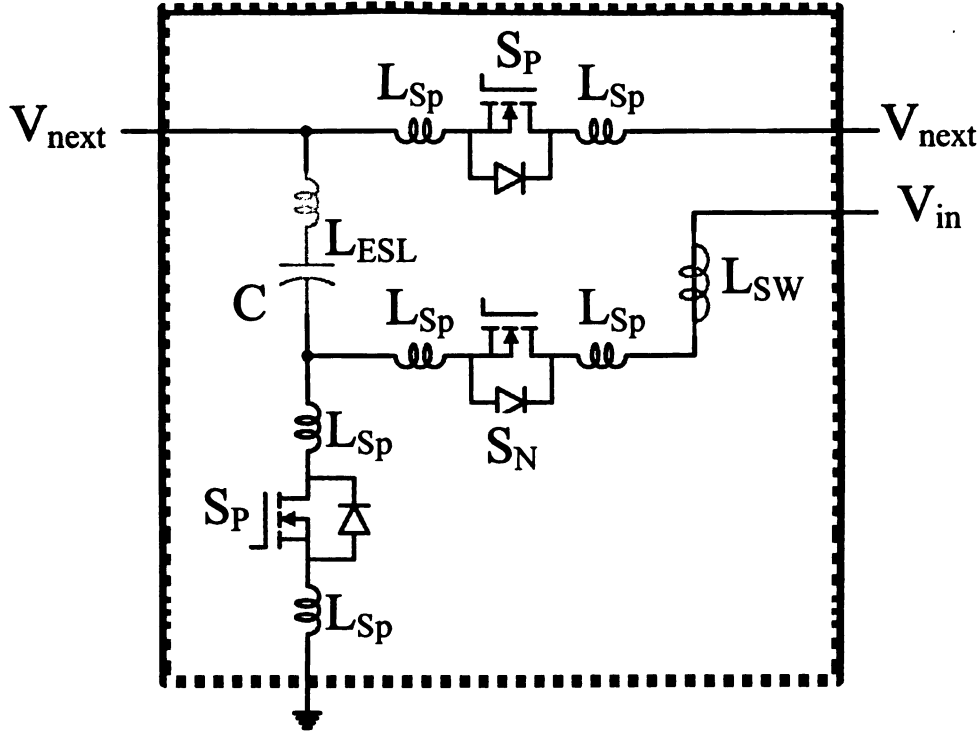


Figure 2.4 ZCS-MMSCC modular block with all the stray inductance.

Because of the modular structure of the circuit, and the stray inductance is distributed in each module, the required stray inductance for resonant is more than 100 times smaller (2 nH~13.5 nH) than other ZCS strategies using same switching frequency [84, 85, 86, 87, 88]. In case the stray inductance is not sufficiently large or equal in each module, a small air core could be utilized to promise each module have the same stray inductance for resonant.

For traditional MMSCC in high power and high current application, a huge capacitor bank has to be employed in order to sustain current and increase efficiency, which increases the converter size in a significant manner. The huge switching loss and voltage spike caused by the large turn-off current is another problem. Considering the stray inductance present in each module of MMSCC, the capacitance can be designed to resonate with the stray inductance at switching frequency to provide the zero current

switching to the devices. In this case, small size, low ESR, high current rating and high temperature rating MLCC capacitor with relatively small capacitance can be utilized. The switching loss of device is minimized, capacitor conduction loss and EMI is also reduced accordingly. Smaller size and higher efficiency is achieved by using ZCS in MMSCC. Hence, ZCS-MMSCC is more suitable to high power, high current and high temperature application.

2.3 Operation Principle

Figure 2.5 shows the idealized waveform of proposed ZCS-MMSCC under steady-state conditions. The gate signal of switch S_P and S_N is complementary, and duty cycle is 50%. Assume input voltage is an ideal voltage source. By considering the stray inductance present in the circuit, when the switch is turned on, the current through the stray inductance, capacitors and the switch will begin to resonate from zero. By adjusting switching frequency to the resonant frequency, the current through switch S_P , S_N and stray inductance will decrease to zero when the switch is turned off, which is the half period of the sinusoidal waveform. Therefore, the ZCS of the switch is achieved in both turn on and turn off. The capacitor is charged in half-period with the sinusoidal current waveform and discharged in another half-period also in the sinusoidal shape. So, the current through the capacitor is the sum of the current through the switch, which is a sinusoidal waveform. When the capacitor is charged, the current is positive; when the capacitor discharges, the current is negative. The voltage across the capacitor has a dc offset with a sinusoidal ripple. The dc voltage offset is determined by the capacitor position in the circuit from one time input voltage to n times input voltage. The voltage

ripple is determined by the capacitor current and capacitance. The operation of the circuit can be described in two states as shown in Figure 2.6 and Figure 2.7 with different switch is turned on.

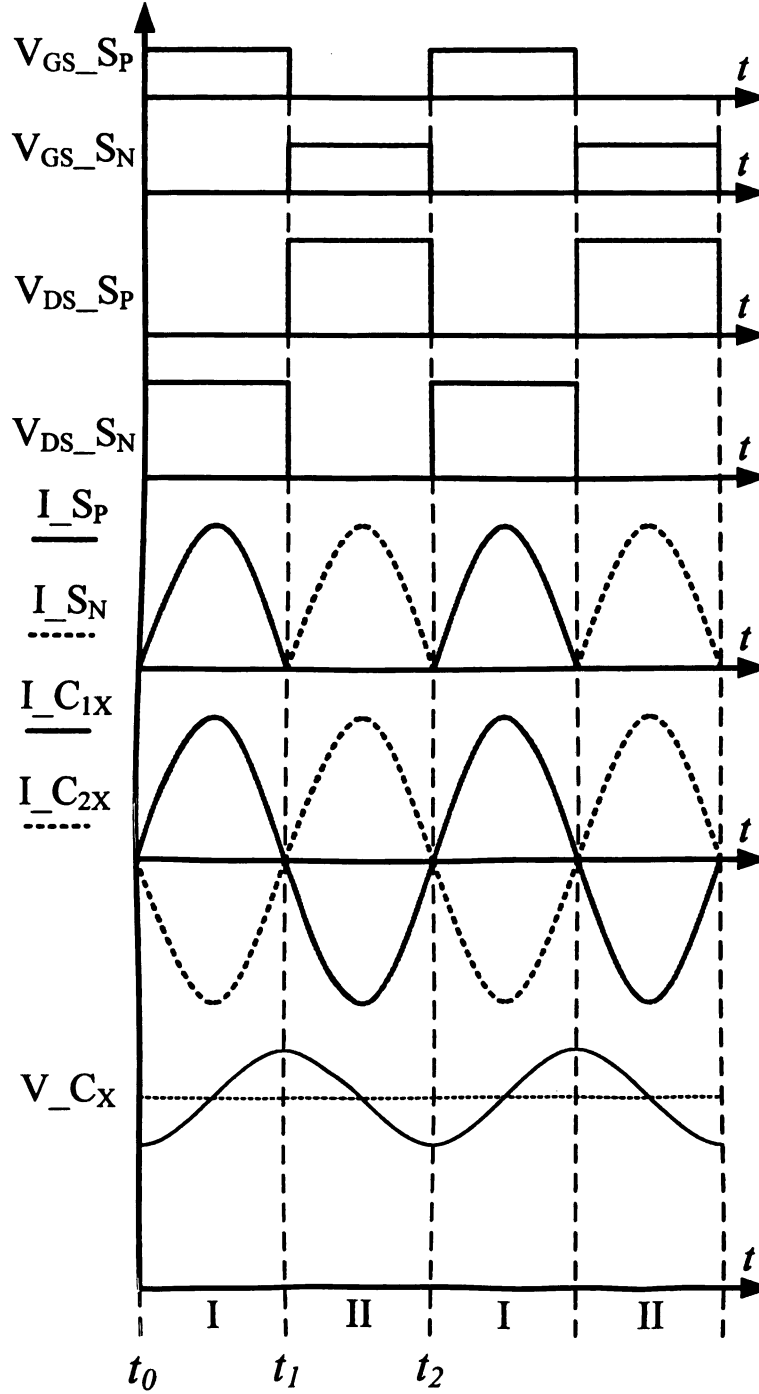


Figure 2.5 Typical waveforms of proposed ZCS-MMSCC

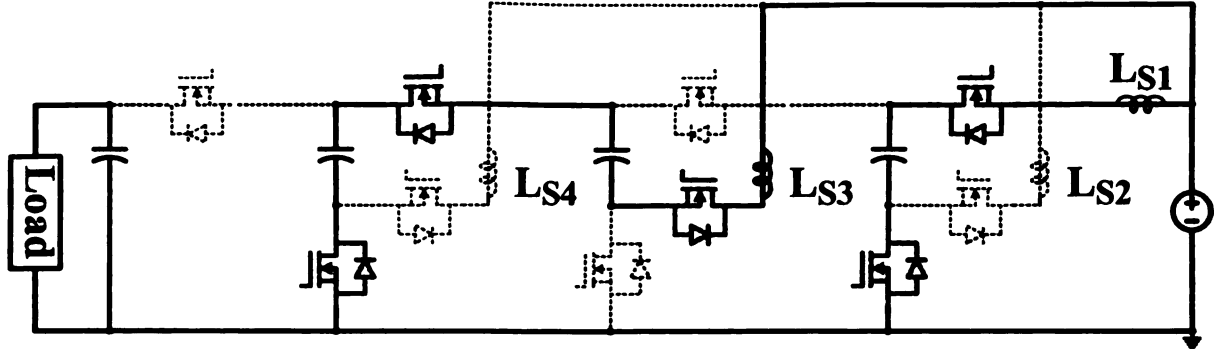


Figure 2.6 Operation modes State I S_P is on

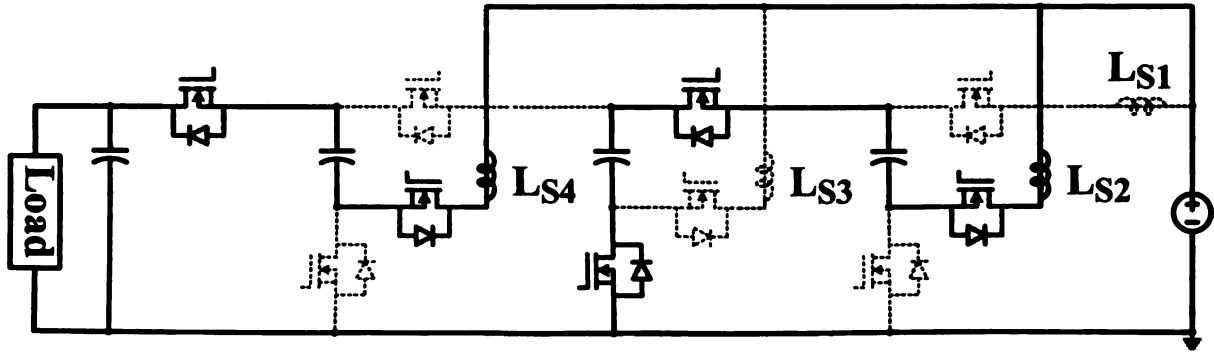


Figure 2.7 Operation modes State II S_N is on

2.3.1 State I

Figure 2.6 shows the state when S_P is turned on at $t = t_0$ while S_N is off. During this state C_{1X} is charged by V_{in} . C_{3X} is charged by V_{in} and C_{2X} in series with. Figure 2.8 and Figure 2.9 shows the two simplified equivalent circuits of state I. Figure 2.8 shows the situation when V_{in} , L_{S1} , S_{P1} , C_{1X} and S_{P2} form a resonant loop. Figure 2.9 shows the situation when V_{in} , L_{S3} , S_{P3} , C_{2X} , S_{P4} , C_{3X} and S_{P5} form a resonant loop. Because of the presence of the stray inductance L_S , before the switch is turned on, the current through L_S already decreases to zero. The current through S_P will increase from zero when the switch is turned on, so S_P is turned on at zero current. For the case shown in Figure 2.8, after L_{S1} and C_{1X} resonate for half cycle, the current through S_{P1}

and S_{P2} falls to zero. Therefore S_{P1} and S_{P2} turn off at zero current. For the case shown in Figure 2.9, after L_{S3} resonate with C_{2X} and C_{3X} in series for half cycle, the current through S_{P3} , S_{P4} and S_{P5} will decrease to zero too. So, zero current turn off is also realized on these switches. For the situation shown in Figure 2.8, there is only one capacitor in the equivalent circuit other than two capacitors in series in other equivalent circuits. The required stray inductance value is two times smaller than the other circuits assuming the capacitance are the same. This will not be a problem in the real circuit design and layout, one only need to pay attention to make sure the stray inductance of first resonant loop is twice smaller than all the other stray inductance.

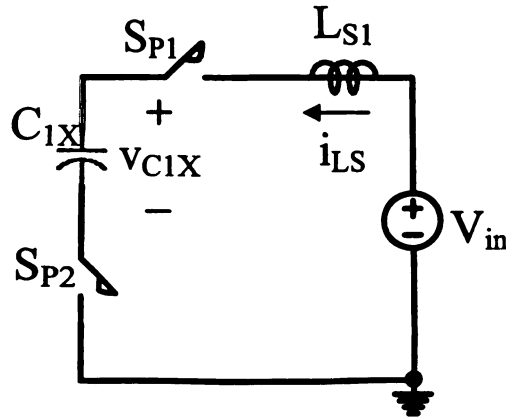


Figure 2.8 Simplified equivalent circuits of state I (a)

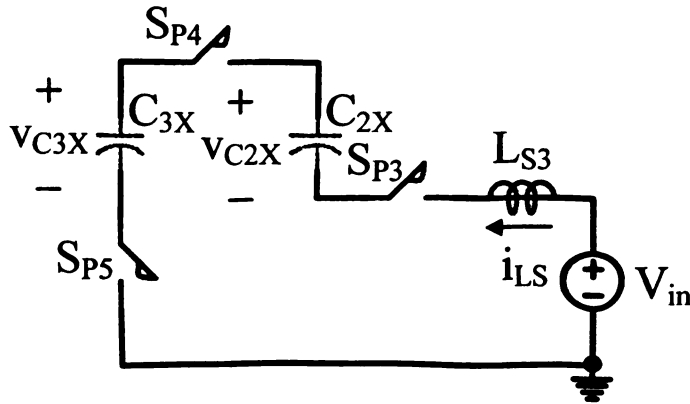


Figure 2.9 Simplified equivalent circuits of state I (b)

Without loss of generality, the following assumptions have been made for the analysis: all the switches are ideal, i.e. no conduction resistance is considered; input voltage source is ideal, i.e. constant and no internal impedance; the capacitor ESR is zero. Assuming $C_{1X} = C_{2X} = C_{3X} = C_{4X}$, so in order to have the same resonant frequency, $L_{S2} = L_{S3} = L_{S4} = 2L_{S1}$. The state equations of Figure 2.8 are

$$V_{in} = L_{S1} \frac{di_{LS1}}{dt} + v_{C1X} \quad (2.1)$$

$$i_{LS1} = C_{1X} \frac{dv_{C1X}}{dt} \quad (2.2)$$

The solutions are:

$$i_{LS1}(t) = \frac{\pi P_o}{4V_{in}} \sin \omega_r t \quad (2.3)$$

$$v_{C1X}(t) = V_{in} - \frac{\pi P_o}{4V_{in} C_{1X} \omega_r} \cos \omega_r t \quad (2.4)$$

Where V_{in} is the value input voltage, L_{S1} is the value of stray inductance, ω_r is the resonant frequency equals to $1 / \sqrt{L_{S1} C_{1X}}$, and P_o is the output power. After half cycle, the capacitor voltage is charged to

$$v_{C1X}(t_1) = V_{in} + \frac{\pi P_o}{4V_{in} C_{1X} \omega_r} \quad (2.5)$$

The capacitor C_{1X} voltage ripple is

$$\Delta v_{C1X} = \frac{\pi P_o}{4V_{in} C_{1X} \omega_r} \quad (2.6)$$

The state equations of Figure 2.9 are

$$V_{in} = L_{S3} \frac{di_{LS3}}{dt} + v_{C3X} - v_{C2X} \quad (2.7)$$

$$i_{LS3} = C_{3X} \frac{dv_{C3X}}{dt} \quad (2.8)$$

$$i_{LS3} = -C_{2X} \frac{dv_{C2X}}{dt} \quad (2.9)$$

Plug (2.17) into (2.7) and (2.9) to solve the equations

$$i_{LS3}(t) = \frac{\pi P_o}{4V_{in}} \sin \omega_r t \quad (2.10)$$

$$v_{C3X}(t) = 3V_{in} - \frac{\pi P_o}{4V_{in}C_{1X}\omega_r} \cos \omega_r t \quad (2.11)$$

The capacitor C_{3X} voltage ripple is

$$\Delta v_{C3X} = \frac{\pi P_o}{4V_{in}C_{1X}\omega_r} \quad (2.12)$$

2.3.2 State II

Figure 2.7 shows the state when S_N is turned on at $t = t_1$ while S_P is off. During this state, C_{2X} is charged by the V_{in} and C_{1X} in series; C_{4X} is charged by V_{in} and C_{3X} in series. Figure 2.10 and Figure 2.11 show the simplified equivalent circuits of state II. Figure 2.10 shows the situation when V_{in} , L_{S2} , S_{N1} , C_{1X} , S_{N2} , C_{2X} and S_{N3} form a resonant loop. And Figure 2.11 shows the situation when V_{in} , L_{S4} , S_{N4} , C_{3X} , S_{N5} , C_{4X} form a resonant loop. Because of the presence of the L_S , the current through S_N will also increase its value from zero in a resonant manner. The zero current turn-on of S_N can be achieved. For the case shown in Figure 2.10, after L_{S2} , C_{1X} and C_{2X} resonate for half cycle at $t = t_2$, S_{N1} , S_{N2} and S_{N3} will have a zero current turn-off when the current through them decreases to zero. For the case shown in Figure 2.11,

after L_{S4} resonate with C_{3X} and C_{4X} in series for a half cycle, the current through S_{N3} , S_{N4} and S_{N5} will also decrease to zero. Hence, zero current turn off is also realized on these switches.

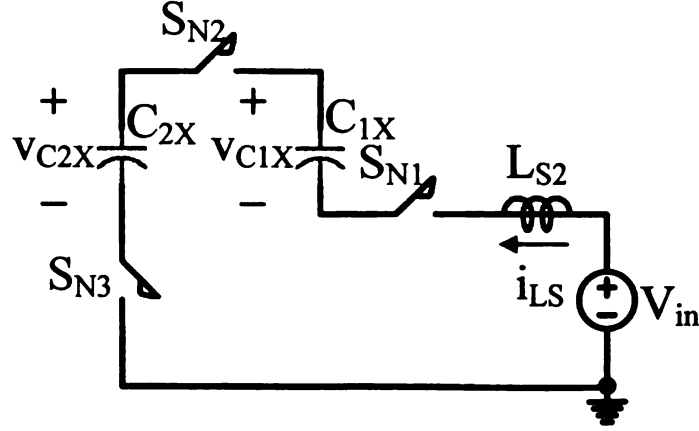


Figure 2.10 Simplified equivalent circuits of state II (a)

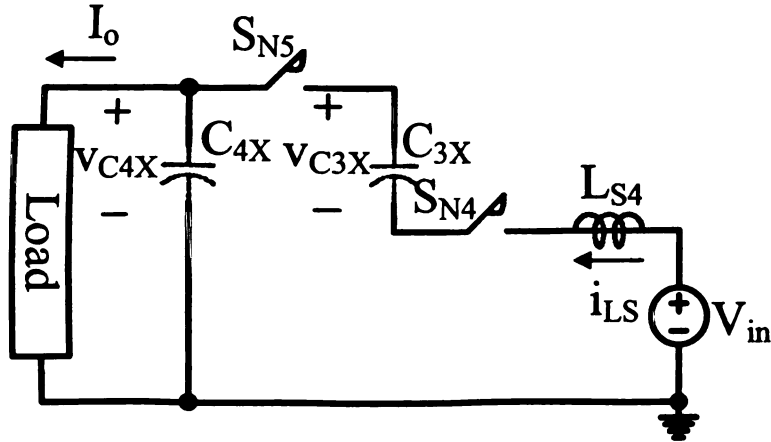


Figure 2.11 Simplified equivalent circuits of state II (b)

The state equations of Figure 2.10 are:

$$v_{in} = L_{S2} \frac{di_{LS2}}{dt} + v_{C2X} - v_{C1X} \quad (2.13)$$

$$i_{LS2} = C_{2X} \frac{dv_{C2X}}{dt} \quad (2.14)$$

$$i_{LS2} = -C_{1X} \frac{dv_{C1X}}{dt} \quad (2.15)$$

Plug (2.4) into (2.13) and (2.15) to solve the equations

$$i_{LS2}(t) = -\frac{\pi P_o}{4V_{in}} \sin \omega_r t \quad (2.16)$$

$$v_{C2X}(t) = 2V_{in} + \frac{\pi P_o}{4V_{in}C_{1X}\omega_r} \cos \omega_r t \quad (2.17)$$

The capacitor C_{2X} voltage ripple is

$$\Delta v_{C2X} = \frac{\pi P_o}{4V_{in}C_{1X}\omega_r} \quad (2.18)$$

The state equations of Figure 2.11 are

$$V_{in} = L_{S4} \frac{di_{LS4}}{dt} + v_{C4X} - v_{C3X} \quad (2.19)$$

$$i_{LS4} = C_{4X} \frac{dv_{C4X}}{dt} + I_o \quad (2.20)$$

$$i_{LS4} = -C_{3X} \frac{dv_{C3X}}{dt} \quad (2.21)$$

Where I_o is the output current. Since this converter is a four times boost circuit

$V_o = 4V_{in}$, so $I_{in} = 4I_o$. Plug (2.11) into (2.19) and (2.21) to solve the equations

$$i_{LS4}(t) = -\frac{\pi P_o}{4V_{in}} \sin \omega_r t \quad (2.22)$$

$$v_{C4X}(t) = 4V_{in} + \frac{\pi P_o}{4V_{in}C_{1X}\omega_r} \cos \omega_r t \quad (2.23)$$

The capacitor C_{4X} voltage ripple is

$$\Delta v_{C4X} = \frac{\pi P_o}{4V_{in}C_{1X}\omega_r} \quad (2.24)$$

The soft switching conditions in both states is $f_s = f_r$, where f_s is the switching frequency and f_r is the resonant frequency.

2.4 Design Guidelines

The 150 W four-level ZCS-MMSCC design procedure is shown here as an example.

The specification of the prototype converter is $V_{in}=5$ V, $V_o=20$ V, $P_o=150$ W, $f_s=45$ kHz.

2.4.1 Capacitance

Capacitance value should be chosen according to the voltage ripple.

$$C = \frac{\pi P_o}{4V_{in}\Delta v_C \omega_r} \quad (2.25)$$

Because of the special structure of the circuit, the voltage ripple across all the capacitors is the same. And the value of the voltage ripple is determined by the input current, capacitance and the resonant frequency. The capacitor voltage ripple should be chosen smaller than the input voltage to prevent the voltage across the first capacitor from resonating to the negative region and lose the zero current switching. That means, the first capacitor should have a positive dc voltage offset. Actually because of the special structure of the converter the output voltage is n times of input voltage, even when the voltage ripple is as large as the input voltage, the voltage ripple on the last capacitor is still $1/n$. When the conversion ratio is large, the ripple will be small enough in the output side. And high capacitance is not needed to reduce the output voltage ripple.

The output ripple is chosen around 9% of output voltage. According to the (2.25), the capacitance is chosen 47 μ F in the prototype. Another parameter to determine the capacitance value is the current rating of the capacitor, if the current rating of the capacitor is too small to meet the current requirements, then more capacitors in parallel have to be used. In this prototype, high current rating MLCC capacitors are used. Ten 100

V 4.7 μF C5750X7R2A475K capacitors from TDK are used in parallel. The current rating of each capacitor is around 3 A each.

2.4.2 Stray inductance

The circuit layout should be designed carefully, in order to make the stray inductance of each equivalent circuit equal. In case the stray inductance is not equal or large enough, small air cores can be inserted to equalize the stray inductance of each module. The switching frequency can be adjusted according to the stray inductance present in the circuit if the circuit layout is already fixed. Required stray inductance for ZCS can be determined by the following equation, using the equivalent circuit shown in Figure 2.8.

$$L_{S1} = \frac{1}{C_{1X} (2\pi f_S)^2} \quad (2.26)$$

When the resonant capacitance is 47 μF , Figure 2.12 shows the curve of switching frequency vs. stray inductance.

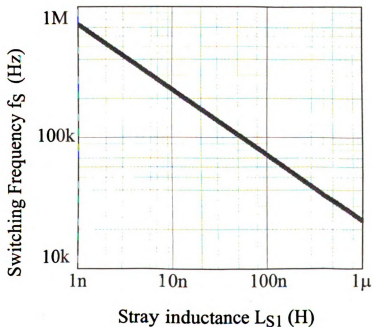


Figure 2.12 ZCS stray inductance and switching frequency

Table 2.1 shows the relevant required stray inductance according to the switching frequency, when the capacitance is 47 μF .

Table 2.1 Required stray inductance according to switching frequency

Switching Frequency f_s	Stray inductance L_{S1}
500kHz	2.15 nH
400 kHz	3.37 nH
300 kHz	6 nH
200 kHz	13.5 nH
100 kHz	54 nH
50 kHz	215 nH

Obviously, for other equivalent circuits shown in Figure 2.9, Figure 2.10, Figure 2.11, the stray inductance values of L_{S2} , L_{S3} , L_{S4} for resonant needs to be doubled. The capacitance value becomes half when two capacitors are connected in series in these equivalent circuits. The switching frequency can be easily determined by the actual stray inductance in the circuit. Around 100 kHz and 200 kHz, the most often used switching frequency in dc-dc converter, the needed stray inductance for resonating is less than 55 nH. This value is small enough to be realized by the stray inductance in the circuit layout or by a small air core. The inductance of a 10 cm long wire or air core inductor is already about 50 nH. Only about 2 nH stray inductances are needed when the switching frequency is increased to 500 kHz. But the stray inductance inside a normal MOSFETs package such as TO-220, is already about 1~2 nH, when several MOSFETs are connected in series, this value could be higher considering the stray inductance of

MOSFET leg which means the switching frequency does not need to be higher than 500 kHz to achieve ZCS.

2.4.3 Switching frequency

Switching frequency should be set the same as resonant frequency in order to promise the zero current switching. Usually, the stray inductance of the circuit is already determined when the circuit layout is finished. The capacitance is also determined by the required voltage ripple. Assume the air core inductor is used, and the stray inductance of each module is equalized. The switching frequency can be twisted by monitoring the power device current when the switch is turned off. The switching frequency should be set exactly at the point when the switch current resonates to zero when the switch is turned off.

2.5 Power Loss Analysis

2.5.1 Power device loss

2.5.1.1 Conduction loss

Assume the input power is P_{in} , power device turn on resistance is R_{on} , the RMS value of switch current is I_{S_RMS} , the average value of input current is I_{in_ave} , the conversion ratio of the converter is N_T , the conduction loss of power device is P_{S_con} .

So the power device conduction loss equation can be derived as follows:

$$I_{in_ave} = \frac{P_{in}}{V_{in}} \quad (2.27)$$

$$I_{S_RMS} = \frac{I_{in_ave}}{N_T} \frac{\pi}{2} \quad (2.28)$$

$$P_{S_con} = I_{S_RMS}^2 R_{on} \quad (2.29)$$

Plug (2.27) and (2.28) to (2.29), the conduction loss can be derived:

$$P_{S_con} = \frac{\pi^2 P_{in}^2}{4 N_T^2 V_{in}^2} R_{on} \quad (2.30)$$

2.5.1.2 gate drive loss

Assume the gate drive voltage is V_{GS} , gate total charge is Q_g , the gate drive loss of power device is P_{S_drv} . So the power device gate drive loss can be derived using the following equation:

$$P_{S_drv} = V_{GS} Q_g f_s \quad (2.31)$$

2.5.2 Capacitor conduction loss

2.5.2.1 Resonant capacitor conduction loss

Assume the capacitor RMS current is I_{C_RMS} , the capacitor ESR is R_{ESR} , the capacitor conduction loss is P_{C_con} . So the capacitor conduction loss can be derived using the following equation:

$$I_{C_RMS} = \frac{\pi I_{in_ave}}{\sqrt{2} N_T} \quad (2.32)$$

$$P_{C_con} = I_{C_RMS}^2 R_{ESR} \quad (2.33)$$

Plug (2.32) into (2.33),

$$P_{C_con} = \frac{\pi^2 I_{in_ave}^2}{2 N_T^2} R_{ESR} \quad (2.34)$$

Plug (2.27) into (2.34),

$$P_{C_con} = \frac{\pi^2 P_{in}^2}{2N_T^2 V_{in}^2} R_{ESR} \quad (2.35)$$

2.5.2.2 Input capacitor conduction loss

Assume the RMS value of input current is I_{in_RMS} , the capacitor ESR is R_{ESR_in} , the conduction loss of input capacitor is P_{Cin_con} . The input current can be shown Figure

2.13

$$I_{in_RMS} = \frac{\pi I_{in_ave}}{2\sqrt{2}} \quad (2.36)$$

$$P_{Cin_con} = I_{in_RMS}^2 R_{ESR_in} \quad (2.37)$$

Plug (2.36) into (2.37) one can get,

$$P_{Cin_con} = \frac{\pi^2 I_{in_ave}^2}{8} R_{ESR_in} \quad (2.38)$$

Plug (2.27) into (2.38) one can get,

$$P_{Cin_con} = \frac{\pi^2 P_{in}^2}{8V_{in}^2} R_{ESR_in} \quad (2.39)$$

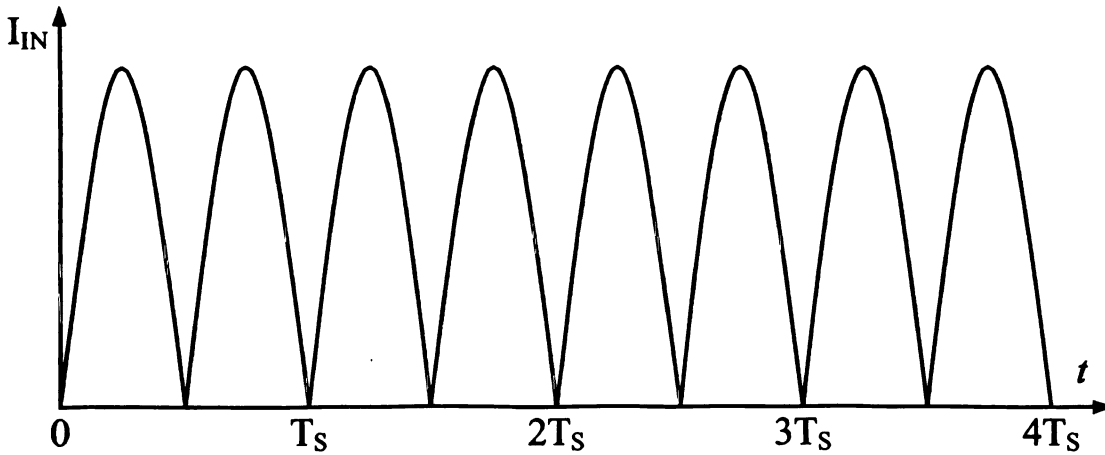


Figure 2.13 Ideal input current waveform

2.5.3 Total power loss

There are $3N_T - 2$ switching devices and N_T capacitors in a N_T level ZCS-MMSCC, so the total power loss P_{loss} is:

$$P_{loss} = (3N_T - 2)(P_{S_con} + P_{S_drv}) + N_T P_{C_con} + P_{Cin_con} \quad (2.40)$$

Plug (2.30), (2.31), and (2.34) into (2.40), one can get

$$P_{loss} = (3N_T - 2) \left(\frac{\pi^2 P_{in}^2 R_{on}}{4N_T^2 V_{in}^2} + V_{GS} Q_g f_s \right) + \frac{\pi^2 P_{in}^2 R_{ESR}}{2N_T V_{in}^2} + \frac{\pi^2 P_{in}^2 R_{ESR_in}}{8V_{in}^2} \quad (2.41)$$

Assume η is the converter efficiency

$$\eta = \frac{P_{in} - P_{loss}}{P_{in}} \quad (2.42)$$

Plug (2.41) into (2.42), one can get:

$$\eta = \frac{P_{in} - (3N_T - 2) \left(\frac{\pi^2 P_{in}^2 R_{on}}{4N_T^2 V_{in}^2} + V_{GS} Q_g f_s \right) - \frac{\pi^2 P_{in}^2 R_{ESR}}{2N_T V_{in}^2} - \frac{\pi^2 P_{in}^2 R_{ESR_in}}{8V_{in}^2}}{P_{in}} \quad (2.43)$$

2.6 Simulation and Experiment Results

2.6.1 A 150 W four-level ZCS-MMSCC prototype

Figure 2.14 shows saber® simulation waveforms of a 150 W four-level ZCS-MMSCC, where V_{gs_Sp} and V_{gs_Sn} are the switch gate-source control voltage, V_{ds_Sp1} and V_{ds_Sn2} are the switch drain-source voltage, I_{d_Sp1} and I_{d_Sn2} are the switch drain-source current. The input voltage is 5 V. Switching frequency is about 45 kHz. Capacitance is 47 μ F and stray inductance L_{S1} is about 250 nH and 500 nH for others. The simulation results is quite consistent with the theoretical analysis, which verifies the above analysis.

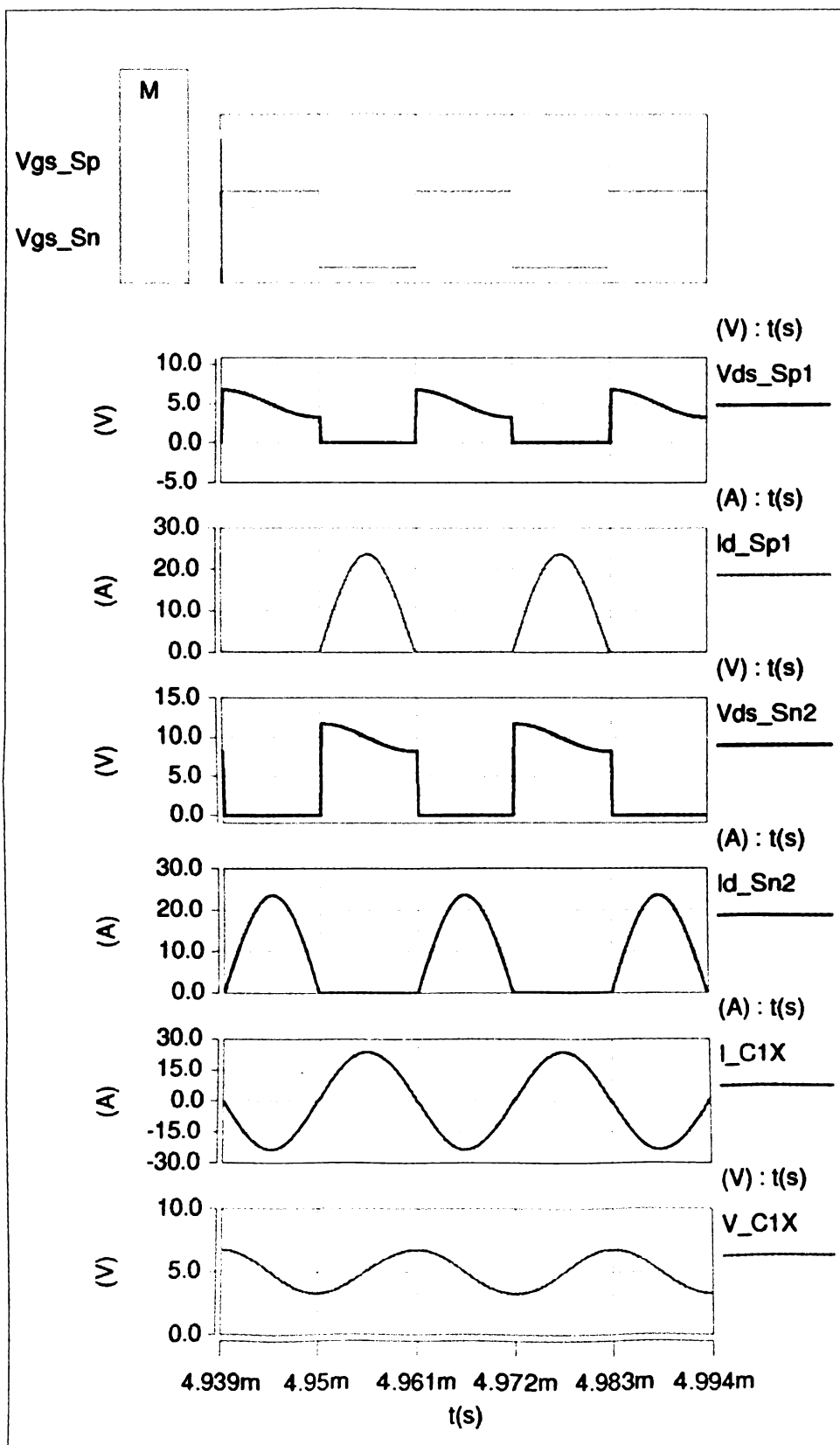


Figure 2.14 Simulation waveforms of 150 W four-level ZCS-MMSCC

In the 150 W 4-level ZCS-MMSCC prototype, the switching devices are two 30 V 180 A MOSFETs IPB009N03L from infineon connected in parallel. Resonant capacitor are ten 100 V 4.7 μ F MLCC capacitors C5750X7R2A475K from TDK connected in parallel. Input capacitor are fourteen 6.3 V 470 μ F conductive polymer aluminum solid electrolytic capacitors PLE0J471MDO1 from nichicon connected in parallel. Gate drive voltage is 15 V. Figure 2.15-Figure 2.18 shows the experiment waveforms of the 150 W 4-level ZCS-MMSCC prototype with the parts mentioned above. Figure 2.15 shows the complementary gate drive signals of S_P and S_N with duty cycle about 48% due to some dead time. V_{GS_SP} and V_{GS_SN} are the complementary gate-source control voltage.

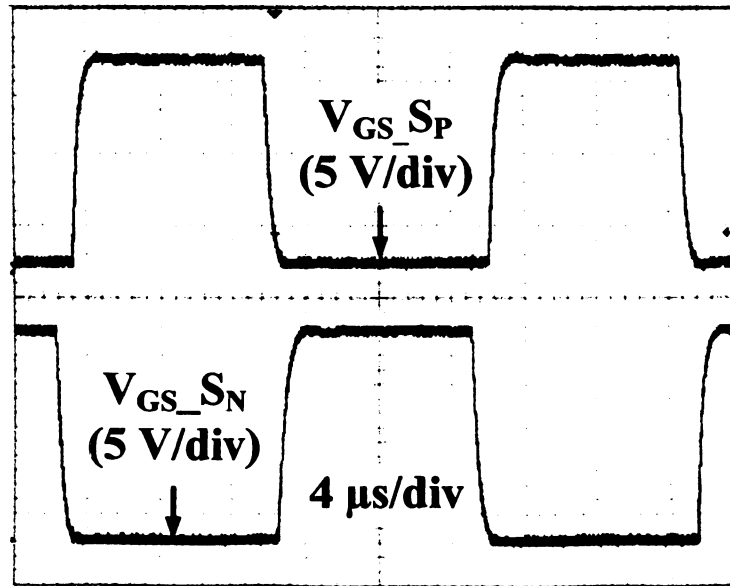


Figure 2.15 Gate drive signal of S_P and S_N

Figure 2.16 shows the voltage and current waveforms of S_{P1} . V_{GS} is the gate-source voltage of S_{P1} , V_{DS} is the drain-source voltage of S_{P1} and I_D is drain-source current of S_{P1} . The resonant current waveform realizing ZCS is shown. Figure 2.17 shows the

zoomed in waveforms of the switch S_{P1} turn off transient, which indicates that the switch achieves ZCS during turn off. From the experiment results, we can derive that the switch S_{P1} can achieve ZCS in both turn on and turn off. Other switches have the same voltage and current waveforms similar to S_{P1} which will not shown here.

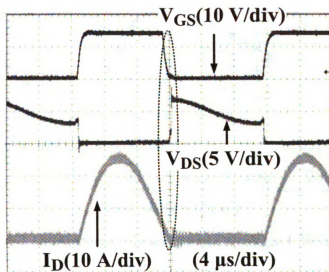


Figure 2.16 Voltage and current waveform of S_{P1}

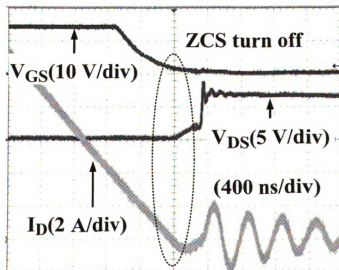


Figure 2.17 Zoomed in voltage and current waveforms of S_{P1}

Figure 2.18 shows the measured efficiency curve using Yokogawa WT1600 digital power meter of proposed ZCS-MMSCC and the calculated efficiency using (2.43). And the efficiency is above 97% which is a big improvement than traditional MMSCC.

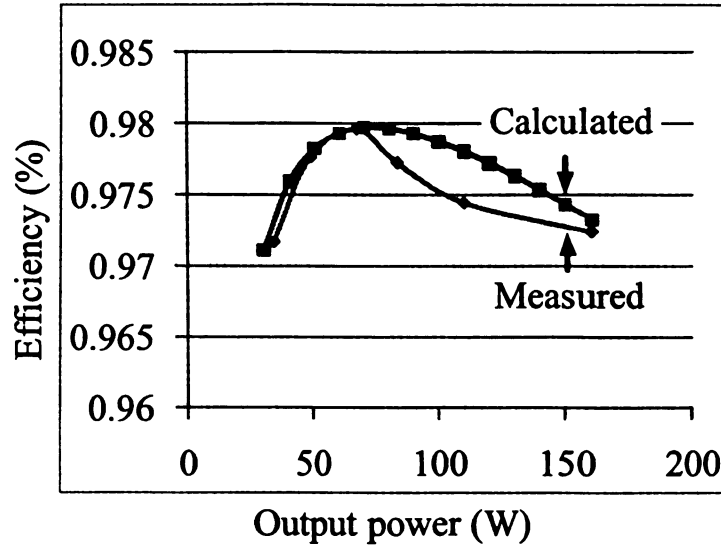


Figure 2.18 Measured Efficiency and Calculated Efficiency

2.6.2 A 630 W twelve-level ZCS-MMSCC prototype

A 630 W twelve-level ZCS-MMSCC prototype is built and tested. In the 630 W twelve-level ZCS-MMSCC prototype, the switching devices are two 30 V 180 A MOSFETs IPB009N03L from infineon connected in parallel. Resonant capacitor are ten 100 V 4.7 μ F MLCC capacitors C5750X7R2A475K from TDK connected in parallel. Input capacitor are sixty-five 6.3 V 470 μ F conductive polymer aluminum solid electrolytic capacitors PLE0J471MDO1 from nichicon connected in parallel. Gate drive voltage is 6 V. Different with the four-level prototype, this new prototype use switching frequency around 70 kHz. The required stray inductance is about 110 nH for L_{S1} and 220 nH for all the other switches. Figure 2.19 shows the twelve-level ZCS-MMSCC input voltage, output voltage and one switch current waveforms under 480 W output.

Figure 2.20 shows the gate drive voltage, drain-source voltage and drain-source current of one switch under 630 W condition. From the experiments waveforms we can derive that, ZCS was achieved in both turn on and turn off of the switch. The voltage gain of the converter is about 12 times.

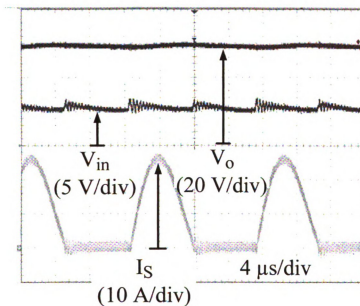


Figure 2.19 Input voltage, output voltage and switch current waveforms

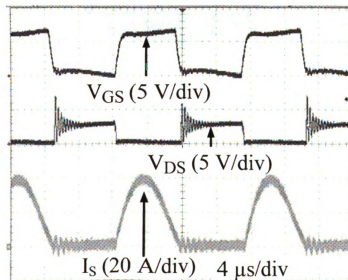


Figure 2.20 Switch voltage and current waveforms

Figure 2.21 shows the estimated loss break down of 630 W prototype using equation (2.41), the estimated efficiency is around 96.7% using equation (2.43). MOSFET and capacitor conduction loss are still the major part. Because of a huge input capacitor bank is using, the input capacitor conduction loss is not that significant. When the input power rating is increased, the input capacitor conduction loss percentage could be bigger caused by the huge input current ripple in an optimized design. Input current ripple should be reduced in order to reduce the total converter size and increase the efficiency.

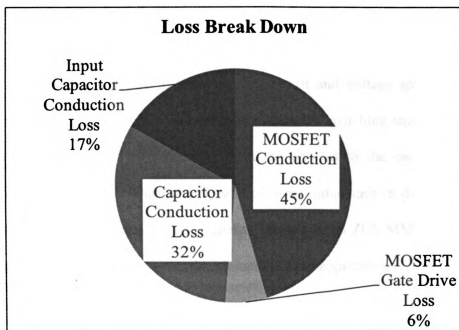


Figure 2.21 Loss break down of the 630 W prototype.

2.7 Conclusion

The presented ZCS-MMSCC has all the advantages of ZCS and MMSCC. And it has some special features besides the features got from ZCS and MMSCC. All the features can be concluded as follows:

- reduces dv/dt , di/dt and EMI because of ZCS;
- reduces the switching loss which improves efficiency;

- uses simple control strategy and possesses modular structure and bidirectional power conversion;
- increases the potential power rating by using MLCC capacitor;
- reduces the capacitance and capacitor size, which lowers the cost
- utilizes distributed stray inductance to achieve ZCS which improves reliability.

A new soft-switching operation strategy to the existing MMSCC has been proposed and validated by both simulation and experiment results. A 150 W, 5 V input four-level converter prototype has been built based on proposed circuit and the efficiency is higher than 97%. A 630 W, 5V input twelve-level converter prototype is also built for the TEG application. The ZCS-MMSCC overcomes the current and voltage spike problems of traditional MMSCC and provides a technically viable soft-switching strategy with circuit layout stray inductance. This technique could be applied to the switching-capacitor circuits on a semiconductor chip with very small stray inductance in the circuit without pushing the switching frequency to megahertz. The proposed ZCS-MMSCC also shows great potential to high voltage gain and high input current applications.

CHAPTER 3

A Family of ZCS Switched-Capacitor DC-DC Converters

This Chapter presents a new zero current switching technique for a family of switched-capacitor dc-dc converters. Compared to the traditional ZCS switched-capacitor dc-dc converter by inserting a relatively big inductor in the circuit, these new ZCS switched-capacitor dc-dc converters employ the stray inductance present in the circuit as the resonant inductor and provide soft-switching for the devices. These ZCS switched-capacitor dc-dc converters do not utilize any additional components to minimize switching loss and reduce current and voltage spike, thus leading to high efficiency and reliable benefit over traditional switched-capacitor dc-dc converters. Moreover, the bulky capacitor bank existing in traditional switched-capacitor circuits for high power high current application to achieve high efficiency was reduced significantly. So, small size, low capacitance, low ESR, high current rating and high temperature rating ceramic capacitors can be employed. Therefore, by using proposed ZCS technique, smaller size, higher power density, higher efficiency, higher temperature rating, and higher current rating switched-capacitor dc-dc converter could be built. Simulation and experimental results are given to demonstrate the validity and features of the soft switching switched-capacitor dc-dc converters.³

3.1 Introduction

³ This work is going to present in part at the 25nd annual IEEE Applied Power Electronics Conference and Exposition, Palm Spring, CA USA, Feb. 21 – Feb. 25 2010.

With the technological development of silicon carbide (SiC) and ceramic materials, very high temperature (250 °C) SiC switching devices and ceramic capacitors will be available. But the magnetic cores become dysfunctional at very high temperature. Therefore, magnetic-less switched-capacitor dc-dc converters operating at very high temperatures become possible and attractive with the adoption of natural air cooling by eliminating bulky heat sinks and magnetic cores. There are three main basic structures of switched-capacitor of dc-dc converters that is most popular, Marx generator type voltage multiplier shown in Figure 3.1 [73, 74, 75], charge pump type multi-level modular switched-capacitor dc-dc converter shown in Figure 3.2 [76, 78], and generalized multi-level type switched-capacitor dc-dc converter shown in Figure 3.3 [81, 82, 83, 96, 101].

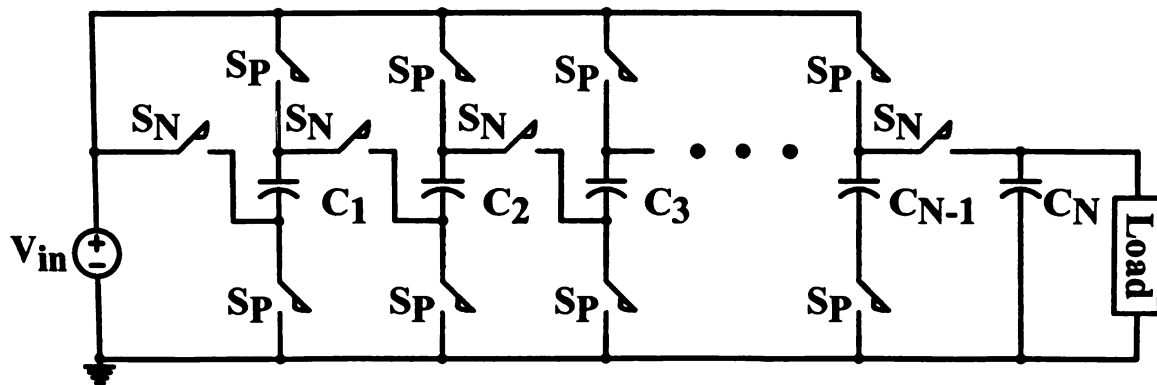


Figure 3.1 Voltage multiplier

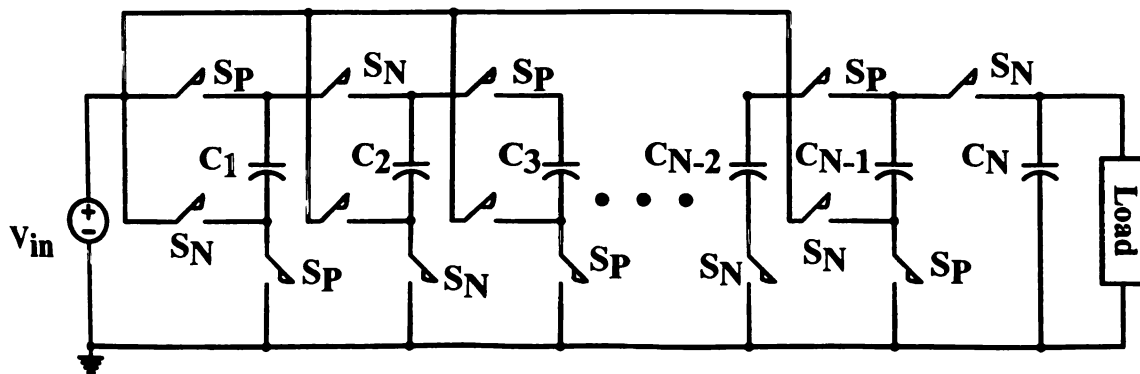


Figure 3.2 Multilevel modular switched-capacitor dc-dc converter.

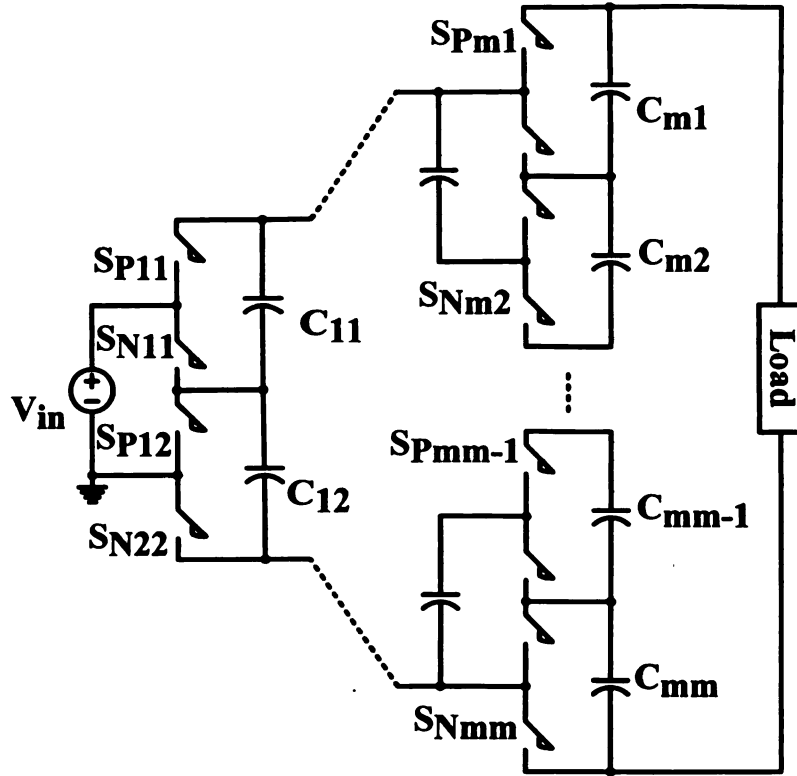


Figure 3.3 Generalized multi-level switched-capacitor dc-dc converter.

However, there are many common drawbacks in traditional switched-capacitor dc-dc converters in high power and high current automotive application. A huge capacitor bank with high capacitance has to be utilized in order to reduce the voltage ripple of the capacitors and achieve high efficiency, which will undoubtedly increase the size of the converter [82, 94, 95, 102]. Besides, with the increase of switching frequency, the switching loss of the device becomes more and more unneglectable. Moreover, huge current spikes, big voltage overshoot caused by large turn off current and EMI problems caused by the di/dt and dv/dt generated during the switching transient are undesirable in automotive applications. In order to reduce the switching loss, voltage spikes, current spikes and EMI, several ZCS methods have been proposed [84, 85, 86, 87, 88, 103]. But adding a relatively big resonant inductor in the switched-capacitor circuit to achieve ZCS is a contradiction by itself. Also, by using the methods mentioned above, switching

frequency has to be pushed to tens of megahertz to utilize parasitic inductance which is not technically feasible [92, 93, 104]. A charge pump type ZCS multi-level modular switched-capacitor dc-dc converter has been proposed recently. By utilizing the distributed parasitic inductance present in the circuit, switching frequency need not to be increased to megahertz, no big inductors are needed to be inserted [105]. By applying the ZCS strategy proposed in [105] to the existing switched-capacitor circuits, a family can be generated.

This chapter presents a family of ZCS switched-capacitor dc-dc converters that is able to overcome the aforementioned drawbacks of traditional switched-capacitor dc-dc converters without inserting big magnetic cores or increasing switching frequency. This new strategy can achieve the ZCS of all the switches without losing the good features of switched-capacitor circuit compared to the traditional ZCS strategy. This ZCS strategy employs the distributed parasitic inductance in the circuit resonating with the capacitors to provide low di/dt and dv/dt to the switching devices. So, the switching loss is minimized, current spike and voltage spike are reduced and EMI is limited. In case the stray inductance is not sufficiently large or equalized, small air core inductors (less than 100n) can be used to meet the requirement of the stray inductance. The power loss is only related to the conduction loss and gate drive loss of switching devices and capacitors by considering the influence of stray inductance. Therefore, bulky capacitor banks with high capacitance are no longer needed to achieve high efficiency, while small MLCC capacitors with low ESR and low capacitance can be adopted to increase efficiency reduce the size. No extra components are added in the presented soft switching strategy, thus making it reliable and low in cost. A 630 W twelve-level ZCS charge pump type

switched-capacitor dc-dc converter and a 480 W ZCS voltage doubler were built to confirm the operation.

3.2 Proposed ZCS Switched-Capacitor DC-DC Converter Family

Figure 3.4, Figure 3.5, and Figure 3.6 show the proposed ZCS switched-capacitor family utilizing the distributed parasitic inductance existing in the circuit. Figure 3.4 shows the N-level ZCS voltage multiplier. Figure 3.5 shows the N-level ZCS MMSCC which has already been discussed in detail in chapter 3. Figure 3.6 shows the N-level ZCS generalized multi-level switched capacitor dc-dc converter.

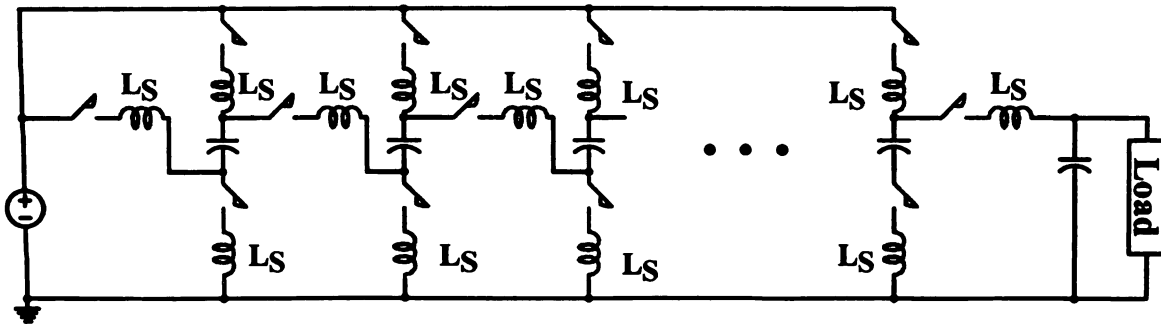


Figure 3.4 ZCS voltage multiplier

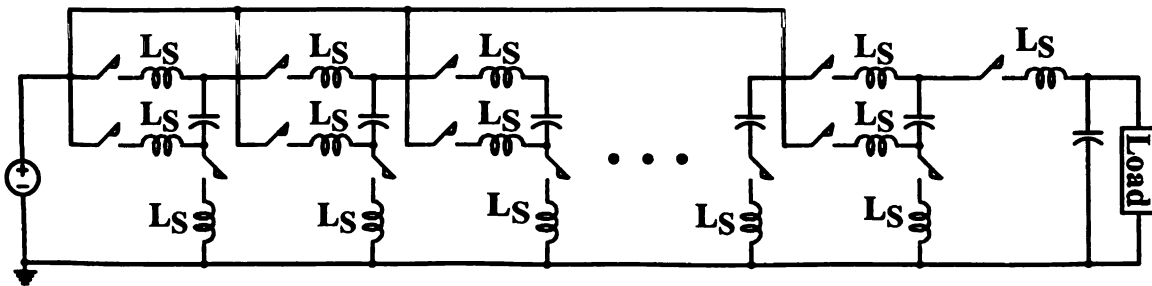


Figure 3.5 ZCS multi-level modular switched-capacitor dc-dc converter

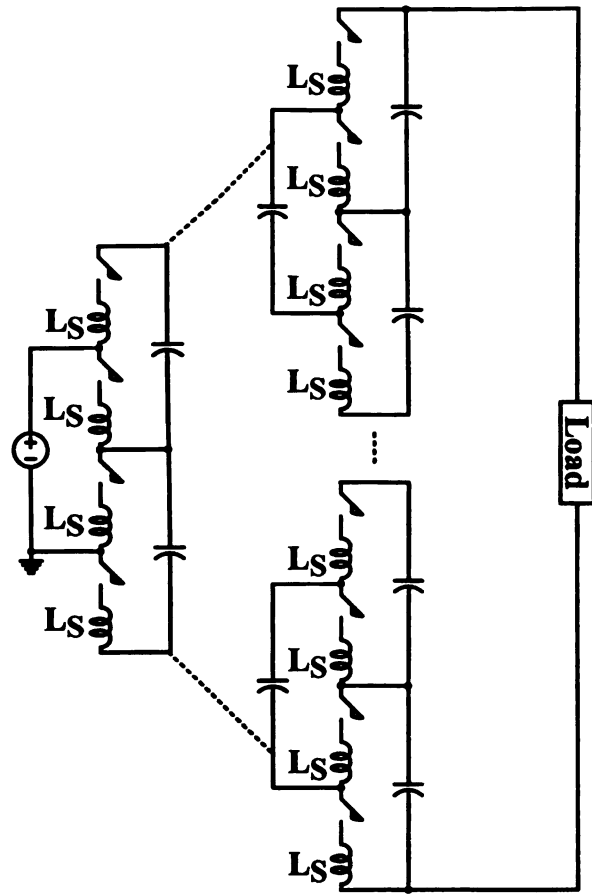


Figure 3.6 ZCS generalized multi-level switched-capacitor dc-dc converter.

The parasitic inductance mainly includes the stray inductance due to the circuit layout, MOSFETs package parasitic inductance and the capacitor ESL. The stray inductance caused by circuit layout is usually the dominant part. By designing the circuit layout specially or inserting specific length of wires which is an air core inductor in the circuit, the inductance needed for resonant is achieved. Because resonant inductors or the inserted wires are distributed in the circuit properly, only small resonant inductance is needed for resonant. Therefore, ZCS of all the switching devices can be achieved by the resonant of the capacitor and the circuit layout stray inductance or inserted wires. In the following parts, two examples of proposed ZCS switched-capacitor dc-dc converters are analyzed, simulation and experimental results are given.

3.3 Operation Principle

Since ZCS-MMSCC has already been discussed in detail in chapter 3, only ZCS voltage multiplier and ZCS generalized switched-capacitor dc-dc converter is going to be discussed here.

3.3.1 ZCS voltage multiplier

Figure 3.7 shows the four-level ZCS voltage multiplier as an example. Similar to the four-level ZCS-MMSCC, this circuit also works as a four times step-up dc-dc converter. V_{in} represents the ideal input voltage source. L_S represents the equivalent stray inductance present in the circuit. L_{S2} , L_{S4} and L_{S6} are the equivalent stray inductance when the capacitor is charged in parallel. L_{S1} , L_{S3} , L_{S5} and L_{S7} are the equivalent stray inductance between each capacitor when the capacitor discharges in series. S_P and S_N are the same switching devices controlled complementary at 50% duty cycle. C_1 to C_3 are the capacitors with the average voltage of input voltage, while C_4 has the average voltage of four times of input voltage. L_S does not have to be in the position drawn in Figure 3.7, it could be distributed anywhere in series with switches or capacitors in the circuit shown in Figure 3.4 or similar to Figure 2.4. Similar to the ZCS-MMSCC, the total stray inductance could be sum of the connection wire parasitic inductance L_{SW} , capacitor parasitic inductance L_{ESL} and the MOSFETs package parasitic inductance L_{Sp} . Usually the connection wire parasitic inductance L_{SW} is the major part of the stray inductance. For the analysis convenience, only one equivalent L_S is used to represent the

total stray inductance present in each parallel resonant loop. And one equivalent L_S is used between two capacitors in the series resonant loop.

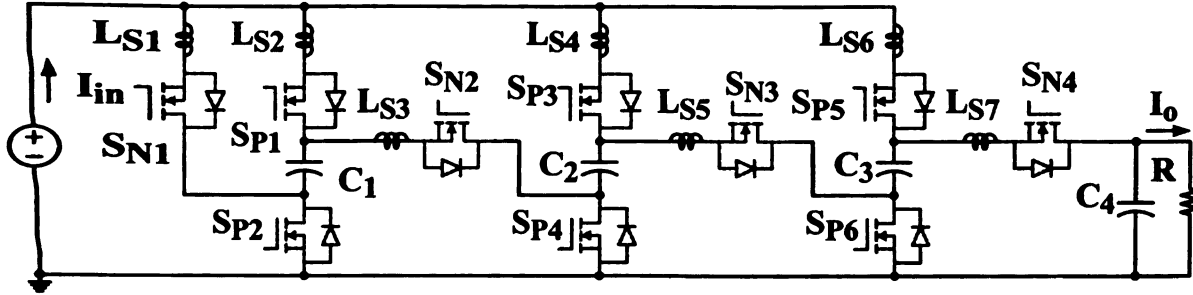


Figure 3.7 Four-level ZCS voltage multiplier main circuit.

Figure 3.8 shows the idealized waveform of proposed ZCS voltage multiplier under steady-state conditions. The gate signal of switch S_P and S_N is complementary, and duty cycle is 50%. Assume input voltage is an ideal voltage source. By considering the stray inductance present in the circuit, when the switches are turned on, the current through the stray inductance, capacitors and the switch will begin to resonate from zero. By adjusting switching frequency to the resonant frequency, the current through switches S_P , S_N and stray inductance will decrease to zero when the switches are turned off, which is the half period of the sinusoidal waveform. Therefore, the ZCS of all the switches is achieved in both turn on and turn off. The capacitor C_1 , C_2 and C_3 are charged in parallel in half-period with the sinusoidal current waveform when S_P is on. And they are discharged in series with the input voltage source in another half-period also in the sinusoidal shape when S_N is on. So, the current through the capacitor C_1 , C_2 , and C_3 is the sum of the current through the switch, which is a sinusoidal waveform.

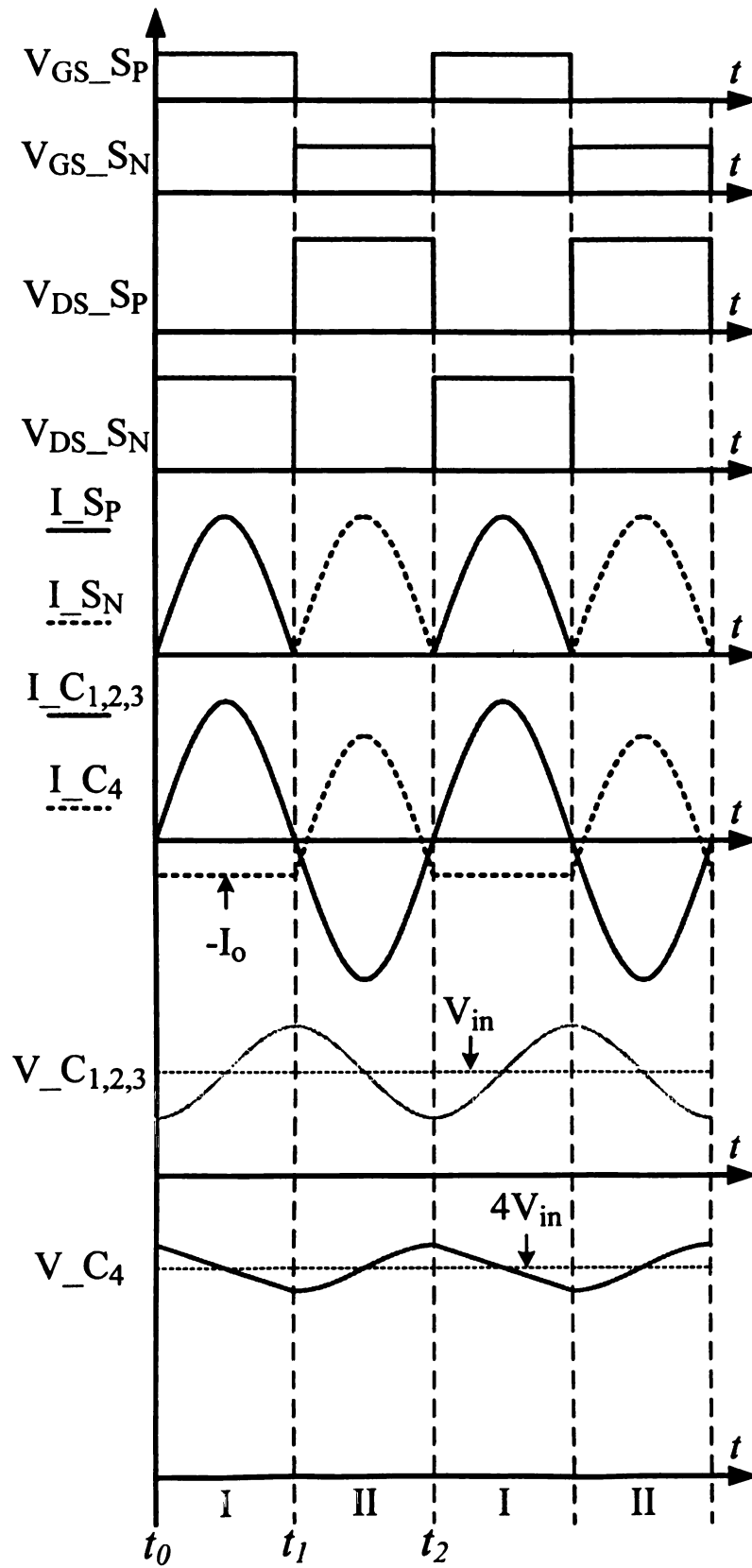


Figure 3.8 Ideal waveforms of four-level ZCS voltage multiplier.

The capacitor C_4 is charged when other capacitors are in series with input voltage.

And it is discharged to the load. So the current through capacitor C_4 is a sinusoid waveform when S_N is on with a negative dc output current offset. When S_P is on, the current through C_4 is the load current. When the capacitor is charged, the current is positive; when the capacitor discharges, the current is negative. The voltage across the capacitor C_1 , C_2 and C_3 has a dc offset of input voltage with a sinusoidal ripple. The voltage ripple is determined by the capacitor current and capacitance. The voltage across the capacitor C_4 has a dc offset of four times input voltage with voltage ripple also determined by the capacitor current and capacitance. The operation of the circuit can be described in two states as shown in Figure 3.9 and Figure 3.10 with different switch is turned on.

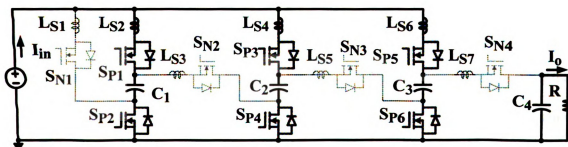


Figure 3.9 Operation modes state I S_P is on.

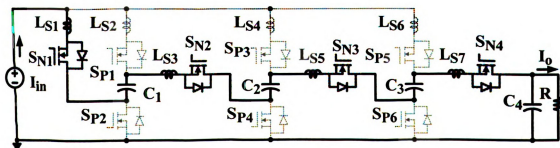


Figure 3.10 Operation modes state II S_N is on.

3.3.1.1 State I [t_0, t_1]

Figure 3.9 shows the state when S_P is turned on at $t = t_0$ while S_N is off. During this state C_1 , C_2 and C_3 are charged by V_{in} . Figure 3.11 shows the three simplified equivalent circuits of state I. Figure 3.11(a) shows the situation when V_{in} , L_{S2} , S_{P1} , C_1 and S_{P2} form a resonant loop. Figure 3.11(b) shows the situation when V_{in} , L_{S4} , S_{P3} , C_2 and S_{P4} form a resonant loop. Figure 3.11(c) shows the situation when V_{in} , L_{S6} , S_{P5} , C_3 and S_{P6} form a resonant loop. Because of the presence of the stray inductance L_S , before the switch is turned on, the current through L_S already decreases to zero. The current through S_P will increase from zero when the switch is turned on, so S_P is turned on at zero current. For the case shown in Figure 3.11(a), after L_{S2} and C_1 resonate for half cycle, the current through S_{P1} and S_{P2} falls to zero. Therefore S_{P1} and S_{P2} turn off at zero current. Similarly, for the case shown in Figure 3.11(b) and Figure 3.11(c) the current through S_{P3} , S_{P4} , S_{P5} and S_{P6} will realize zero current turn on and turn off too. So, ZCS is achieved on all the switches. The required stray inductance value is the same for the three circuit and is easy to be achieved by the circuit layout due to the symmetry of the circuit, assuming the capacitance are the same.

Without loss of generality, the following assumptions have been made for the analysis: all the switches are ideal, i.e. no conduction resistance is considered; input voltage source is ideal, i.e. constant and no internal impedance; the capacitor ESR is zero.

Assuming $C_1 = C_2 = C_3 = C_4$, so in order to have the same resonant frequency,

$$L_{S1} = L_{S2} = L_{S3} = L_{S4} = L_{S5} = L_{S6} = L_{S7}.$$

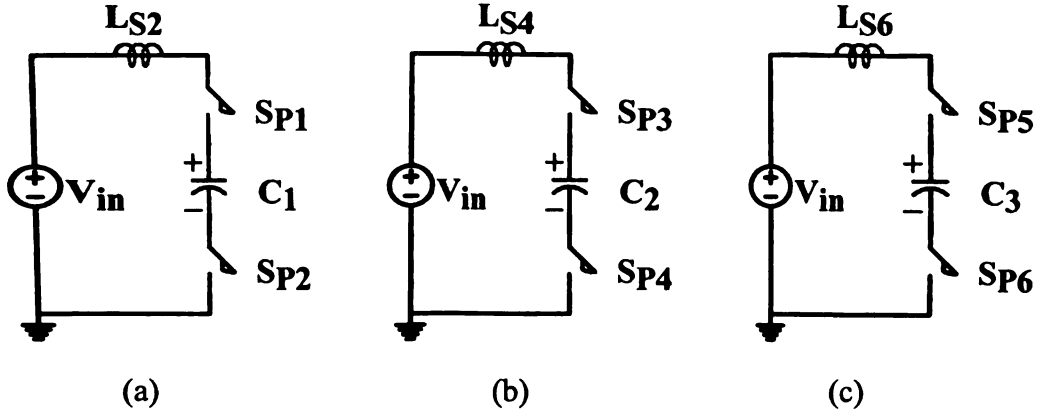


Figure 3.11 Simplified equivalent circuits of state I

The state equations of Figure 3.11(a) are

$$V_{in} = L_{S2} \frac{di_{LS2}}{dt} + v_{C1} \quad (3.1)$$

$$i_{LS2} = C_1 \frac{dv_{C1}}{dt} \quad (3.2)$$

The solutions are:

$$i_{S2}(t) = \frac{\pi P_o}{4V_{in}} \sin \omega_r t \quad (3.3)$$

$$v_{C1}(t) = V_{in} - \frac{\pi P_o}{4V_{in}C_1\omega_r} \cos \omega_r t \quad (3.4)$$

Where V_{in} is the value input voltage, L_{S2} is the value of stray inductance, ω_r is the resonant frequency equals to $1/\sqrt{L_{S1}C_1}$, and P_o is the output power. After half cycle, the capacitor voltage is charged to:

$$v_{C1}(t_1) = V_{in} + \frac{\pi P_o}{4V_{in}C_1\omega_r} \quad (3.5)$$

The capacitor voltage ripple is:

$$\Delta v_{C1} = \frac{\pi P_o}{4V_{in}C_1\omega_r} \quad (3.6)$$

The state equations of Figure 3.11(b) and Figure 3.11(c) are similar to the state equations of Figure 3.11(a). The voltage across C_2 and C_3 are exactly the same as the voltage across C_1 . The voltage ripple of C_2 and C_3 are also the same as Δv_{C_1} .

3.3.1.2 State II [t_1, t_2]

Figure 3.10 shows the state when S_N is turned on at $t = t_1$ while S_P is off. During this state, C_4 is charged by the V_{in} . C_1 , C_2 and C_3 in series. Figure 3.12 shows the simplified equivalent circuits of state II. It shows the situation when V_{in} , L_{S1} , S_{N1} , C_1 , L_{S3} , S_{N2} , C_2 , L_{S5} , S_{N3} , C_3 , L_{S7} , S_{N4} , and C_4 form a resonant loop. Similar as the last state, because of the presence of the L_S , the current through S_N will also increase its value from zero in a resonant manner. The zero current turn-on of S_N can be achieved. After stray inductance L_{S1} , L_{S3} , L_{S5} and L_{S7} in series resonate with capacitor C_1 , C_2 , C_3 and C_4 in series for half cycle at $t = t_2$, S_{N1} , S_{N2} , S_{N3} and S_{N4} will have a zero current turn-off when the current through them decreases to zero. Hence, zero current switching can be achieved on these switches.

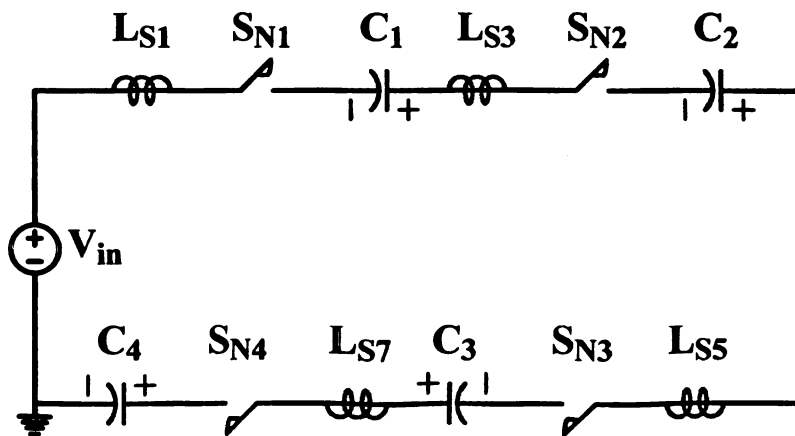


Figure 3.12 Simplified equivalent circuits of state II

The state equations of Figure 3.12 are:

$$V_{in} + v_{C1} + v_{C2} + v_{C3} = 4L_{S1} \frac{di_{LS1}}{dt} + v_{C4} \quad (3.7)$$

$$i_{LS1} = C_4 \frac{dv_{C4}}{dt} \quad (3.8)$$

The solutions are:

$$v_{C4}(t) = 4V_{in} - \frac{\pi P_o}{4V_{in}C_4\omega_r} \cos \omega_r t \quad (3.9)$$

$$i_{LS1}(t) = \frac{\pi P_o}{4V_{in}} \sin \omega_r t \quad (3.10)$$

After half cycle, the capacitor voltage is charged to

$$v_{C4}(t_2) = 4V_{in} + \frac{\pi P_o}{4V_{in}C_4\omega_r} \quad (3.11)$$

The capacitor voltage ripple is:

$$\Delta v_{C4} = \frac{\pi P_o}{4V_{in}C_4\omega_r} \quad (3.12)$$

All the capacitors have the same voltage ripple and the voltage ripple depends on the output power, input voltage, capacitance and the resonant frequency.

3.3.2 ZCS voltage doubler

Figure 3.7 shows the two-level ZCS generalized multi-level switched-capacitor dc-dc converter an example. This circuit can be also called as the ZCS voltage doubler in short, because this circuit works as a two times step-up dc-dc converter. V_{in} represents the ideal input voltage source. L_S represents the equivalent stray inductance present in the circuit. L_{S1} , L_{S2} , L_{S3} and L_{S4} can be considered as the stray inductance in series with the switch during the circuit layout. S_P and S_N are the same switching devices controlled complementary at 50% duty cycle. C_1 and C_2 are the capacitors with the average voltage

the same as the input voltage. Because of the symmetry of the circuit, the distributed stray inductance L_{S1} , L_{S2} , L_{S3} and L_{S4} can be replaced with an equivalent stray inductance L_S in the input side shown in Figure 3.14 for the analysis convenience. Only one equivalent stray inductance L_S is needed to represent the total stray inductance in two resonant loop.

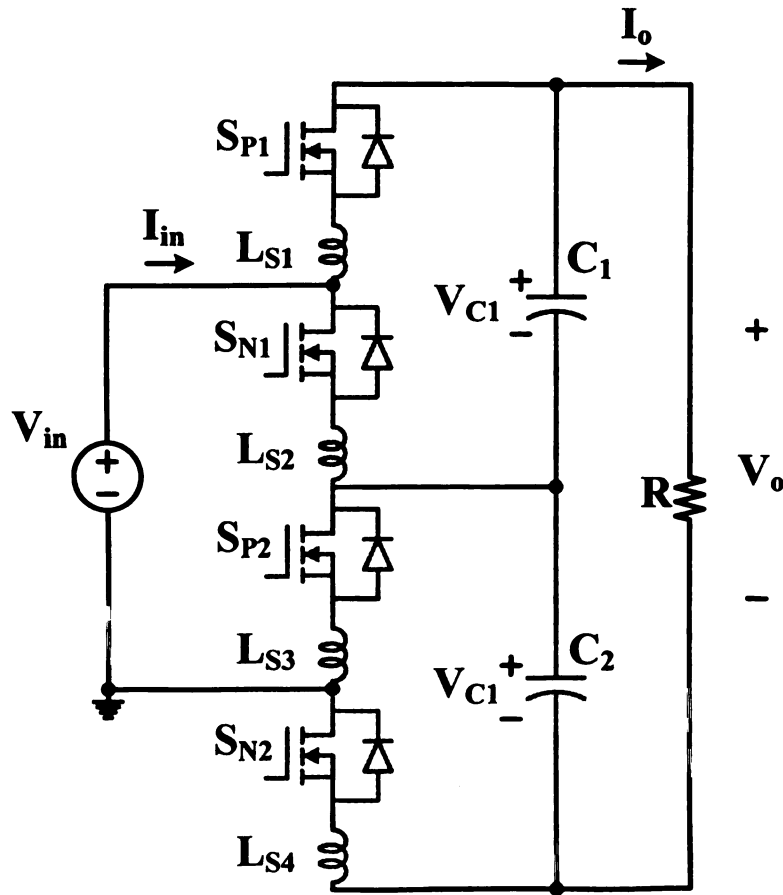


Figure 3.13 ZCS voltage doubler main circuit.

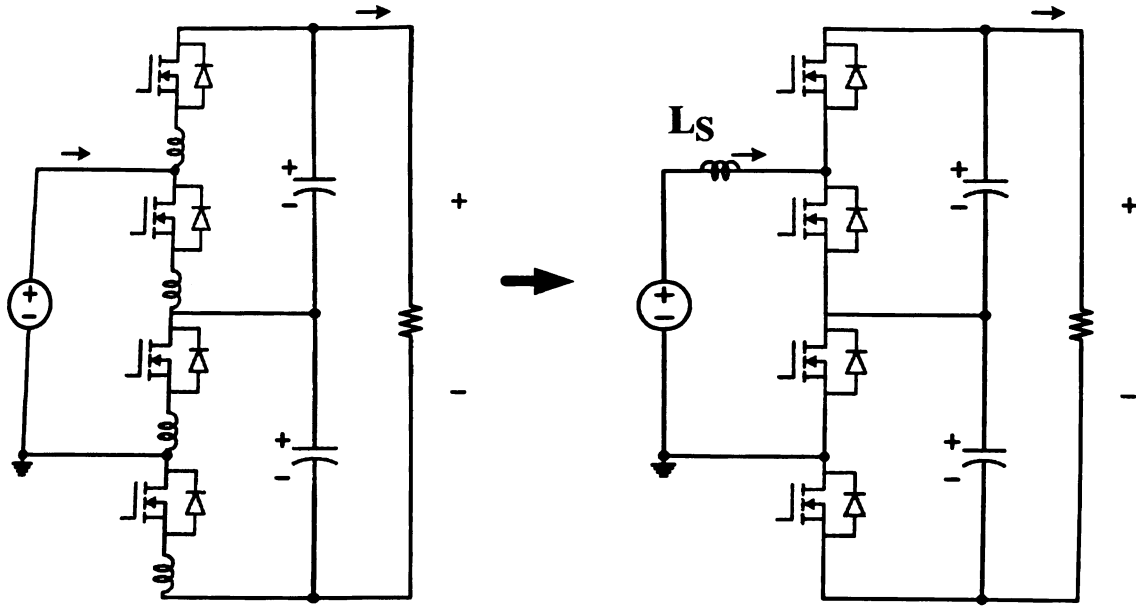


Figure 3.14 ZCS voltage doubler topology simplification.

Figure 3.15 shows the idealized waveform of proposed ZCS voltage doubler under steady-state conditions. The gate signal of switch S_P and S_N is complementary, and duty cycle is 50%. Assume input voltage is an ideal voltage source. By considering the equivalent stray inductance in the input side, when the switches are turned on, the current through the stray inductance, capacitors and the switch will begin to resonate from zero. By adjusting switching frequency to the resonant frequency, the current through switches S_P , S_N and stray inductance will decrease to zero when the switches are turned off, which is the half period of the sinusoidal waveform. Therefore, the ZCS of all the switches is achieved in both turn on and turn off. The capacitor C_1 and C_2 are charged in each half-period with the sinusoidal current waveform when S_P or S_N is on. And they are always discharged in series. So, the current through the capacitor C_1 , and C_2 , is the current through the switch subtracts the output current. The output voltage ripple is half of the voltage ripple of the capacitor, because of the 180 degree phase shift of the

capacitor voltage ripple. The capacitor voltage ripple will cancel with each other. The operation of the circuit can be described in two states as shown in Figure 3.16 and Figure 3.17 with different switch is turned on.

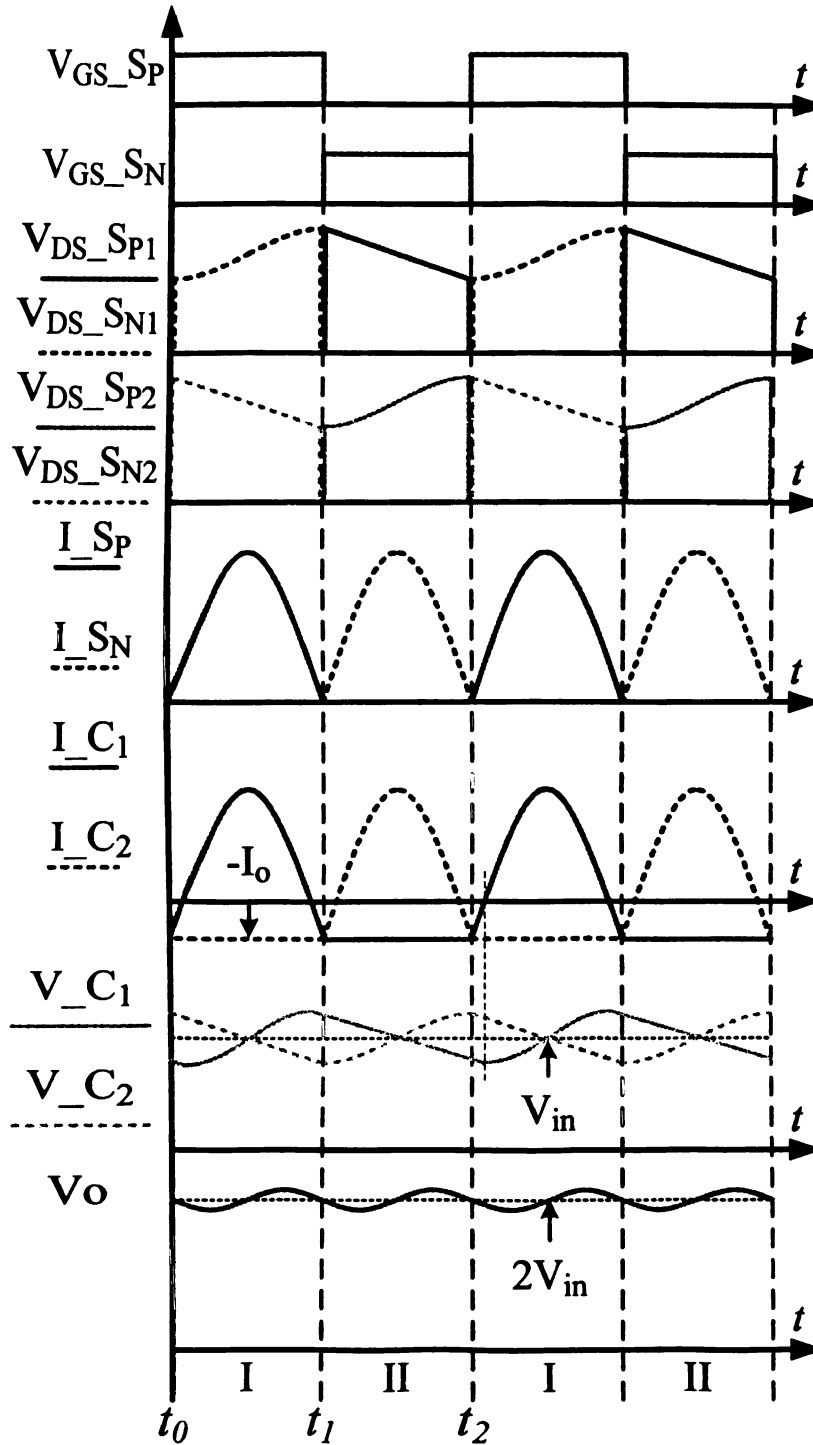


Figure 3.15 Ideal waveforms of ZCS voltage doubler.

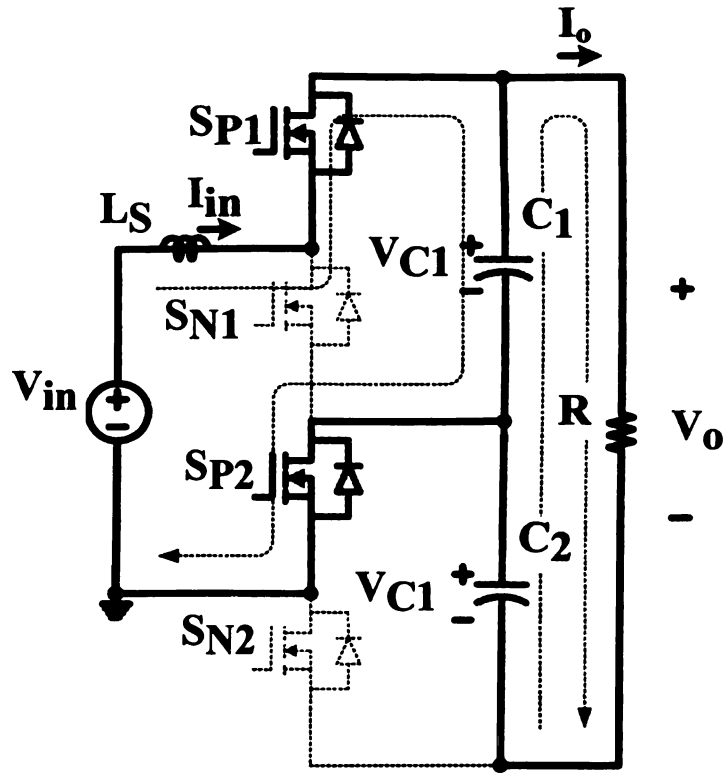


Figure 3.16 Operation modes of state I when S_P is on.

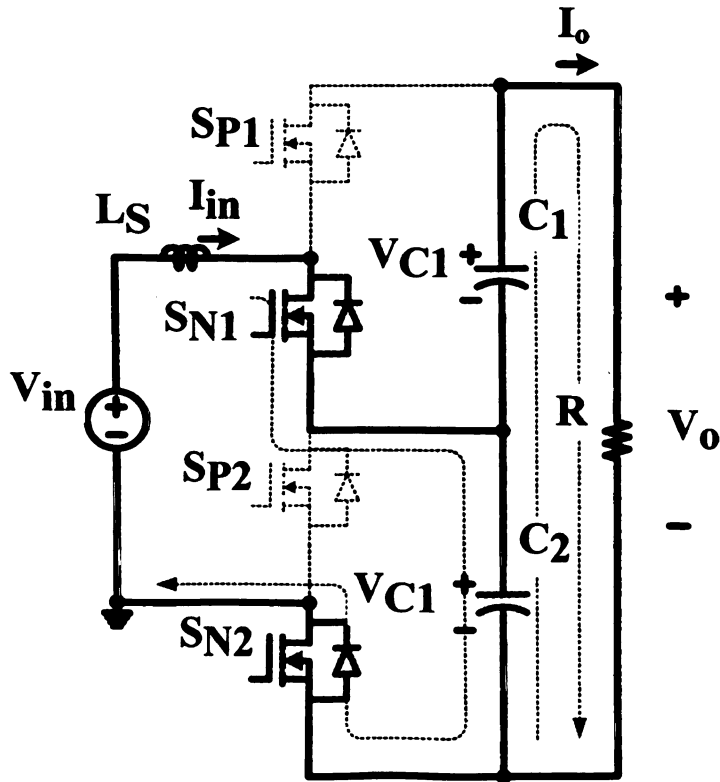


Figure 3.17 Operation modes of state II when S_N is on.

3.3.2.1 State I [t_0, t_1]

Figure 3.16 shows the state when S_P is turned on at $t = t_0$ while S_N is off. During this state C_1 is charged by V_{in} . Figure 3.18 shows the simplified equivalent circuits of state I. It shows the situation when V_{in} , L_S , S_{P1} , C_1 and S_{P2} form a resonant loop. Because of the presence of the stray inductance L_S , before the switch is turned on, the current through L_S already decreases to zero. The current through S_P will increase from zero when the switch is turned on, so S_P is turned on at zero current. After L_S and C_1 resonate for half cycle, the current through S_{P1} and S_{P2} falls to zero. Therefore S_{P1} and S_{P2} turn off at zero current. So, ZCS is achieved on all the switches.

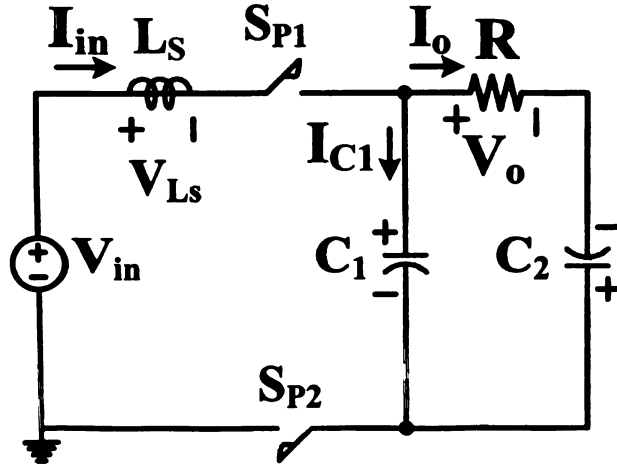


Figure 3.18 Simplified equivalent circuits of state I

Without loss of generality, the following assumptions have been made for the analysis: all the switches are ideal, i.e. no conduction resistance is considered; input voltage source is ideal, i.e. constant and no internal impedance; the capacitor ESR is zero. Assume $C_1 = C_2$. The state equations of Figure 3.18 are:

$$V_{in} = L_S \frac{di_{L_S}}{dt} + v_{C1} \quad (3.13)$$

$$i_{LS} = C_1 \frac{dv_{C1}}{dt} + I_o \quad (3.14)$$

$$-I_o = C_2 \frac{dv_{C2}}{dt} \quad (1.15)$$

$$I_o = \frac{P_o}{2V_{in}} \quad (1.16)$$

And the solutions are:

$$v_{C1}(t) = V_{in} - \frac{\pi P_o}{2V_{in}C_1\omega_r} \cos \omega_r t \quad (3.17)$$

$$v_{C2}(t) = -\frac{P_o}{2V_{in}C_2}t + V_{in} + \frac{\pi P_o}{2V_{in}C_2\omega_r} \quad (1.18)$$

$$i_{LS}(t) = \frac{\pi P_o}{2V_{in}} \sin \omega_r t \quad (3.19)$$

Where V_{in} is the value input voltage, L_S is the value of stray inductance, ω_r is the resonant frequency equals to $1/\sqrt{L_S C_1}$, and P_o is the output power. After half cycle, the capacitor voltage is charged to:

$$v_{C1}(t_1) = V_{in} + \frac{\pi P_o}{2V_{in}C_1\omega_r} \quad (3.20)$$

The capacitor voltage ripple is:

$$\Delta v_{C1} = \frac{\pi P_o}{2V_{in}C_1\omega_r} \quad (3.21)$$

3.3.2.2 State II [t_1, t_2]

Figure 3.17 shows the state when S_N is turned on at $t = t_1$ while S_P is off. During this state C_2 is charged by V_{in} . C_1 and C_2 in series form the output current. Figure 3.19 shows the simplified equivalent circuits of state II. It shows the situation when V_{in} , L_S , S_{N1} , C_2 and S_{N2} form a resonant loop. Because of the presence of the stray inductance

L_S , before the switch is turned on, the current through L_S already decreases to zero. The current through S_N will increase from zero when the switch is turned on, so S_N is turned on at zero current. After L_S and C_2 resonate for half cycle, the current through S_{N1} and S_{N2} falls to zero. Therefore S_{N1} and S_{N2} turn off at zero current. So, ZCS is achieved on all the switches. The state equations of Figure 3.19 are:

$$V_{in} = L_S \frac{di_{L_S}}{dt} + v_{C_2} \quad (3.22)$$

$$i_{L_S} = C_2 \frac{dv_{C_2}}{dt} + I_o \quad (3.23)$$

And the solutions are:

$$v_{C_2}(t) = V_{in} - \frac{\pi P_o}{2V_{in}C_1\omega_r} \cos \omega_r t \quad (3.24)$$

$$i_{L_S}(t) = \frac{\pi P_o}{2V_{in}} \sin \omega_r t \quad (3.25)$$

After half cycle, the capacitor voltage is charged to:

$$v_{C_2}(t_2) = V_{in} + \frac{\pi P_o}{2V_{in}C_1\omega_r} \quad (3.26)$$

The capacitor voltage ripple is:

$$\Delta v_{C_2} = \frac{\pi P_o}{2V_{in}C_1\omega_r} \quad (3.27)$$

The soft switching conditions in both states is $f_s = f_r$, where f_s is the switching frequency and f_r is the resonant frequency.

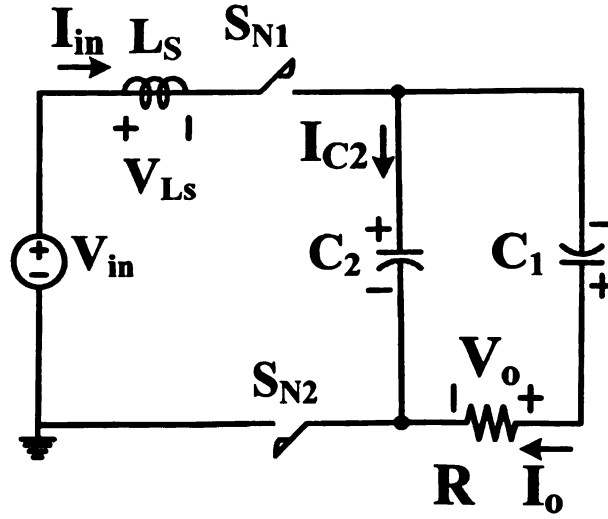


Figure 3.19 Simplified equivalent circuits of state II

3.4 Design Considerations

3.4.1 ZCS voltage multiplier

The 160 W four-level ZCS voltage multiplier design procedure is shown here as an example. The specification of the prototype converter is $V_{in}=5$ V, $V_o=20$ V, $P_o=160$ W, $f_s=70.4$ kHz.

3.4.1.1 Capacitance

Capacitance value should be chosen according to the voltage ripple.

$$C = \frac{\pi P_o}{4V_{in}\Delta v_C \omega_r} \quad (3.28)$$

Because of the special structure of the circuit, the voltage ripple across all the capacitors is the same. And the value of the voltage ripple is determined by the output power, input voltage, capacitance and the resonant frequency. The capacitor voltage ripple should be chosen smaller than the input voltage to prevent the voltage across the capacitor from resonating to the negative region and lose the zero current switching. That

means, the capacitors should have a positive dc voltage offset. The output voltage ripple is two times smaller than the capacitor voltage ripple because of the 180 degrees phase shift operation of switches.

The output ripple is chosen around 6% of output voltage. So the capacitor voltage ripple is 12% of the capacitor voltage. According to the (3.28), the capacitance is chosen 47 μ F in the simulation.

3.4.1.2 Stray inductance

The circuit layout should be designed carefully, in order to make the stray inductance of each equivalent circuit equal. In case the stray inductance is not equal or large enough, small air cores can be inserted to equalize the stray inductance. The switching frequency can be adjusted according to the stray inductance present in the circuit if the circuit layout is already fixed. Required stray inductance for ZCS can be determined by the following equation, using the equivalent circuit shown in Figure 3.11.

$$L_{S2} = \frac{1}{C_1(2\pi f_S)^2} \quad (3.29)$$

Considering the output current influence, required stray inductance for L_{S1} , L_{S3} , L_{S5} and L_{S7} are a little bit smaller than the stray inductance of L_{S2} , L_{S4} and L_{S6} . So in the design, attention should be paid in order to achieve the ZCS of all the switches.

3.4.1.3 Switching frequency

Switching frequency should be set the same as resonant frequency in order to promise the zero current switching. Usually, the stray inductance of the circuit is already determined when the circuit layout is finished. The capacitance is also determined by the required voltage ripple. Assume the air core inductor is used, and the stray inductance of

all the parallel charging loop is equalized. The stray inductance for the series loop is also chosen properly. The switching frequency can be twisted by monitoring the power device current when the switch is turned off. The switching frequency should be set exactly at the point when the switch current resonates to zero when the switch is turned off.

3.4.2 ZCS voltage doubler

The 480 W ZCS voltage doubler design procedure is shown here as an example. The specification of the prototype converter is $V_{in}=12$ V, $V_o=24$ V, $P_o=480$ W, $f_s=44.2$ kHz.

3.4.2.1 Capacitance

Capacitance value should be chosen according to the voltage ripple.

$$C = \frac{\pi P_o}{2V_{in}\Delta v_C \omega_r} \quad (3.30)$$

Because of the special structure of the circuit, the voltage ripple across all the capacitors is the same. And the value of the voltage ripple is determined by the output power, input voltage, capacitance and the resonant frequency. The capacitor voltage ripple should be chosen smaller than the input voltage to prevent the voltage across the capacitor from resonating to the negative region and lose the zero current switching. That means, the capacitors should have a positive dc voltage offset. The output voltage ripple is two times smaller than the capacitor voltage ripple because of the 180 degrees phase shift operation of the switches.

The output ripple is chosen around 8% of output voltage. So the capacitor voltage ripple is 40% of the capacitor voltage. According to the (3.30), the capacitance is chosen 47 μ F in the simulation.

3.4.2.2 Stray inductance

The circuit layout should be designed carefully, in order to make the stray inductance of each equivalent circuit equal. Assume all the stray inductance in the circuit is equalized. And the required stray inductance can be satisfied by using proper input inductance. Required stray inductance for ZCS can be determined by the following equation, using the equivalent circuit shown in Figure 3.18.

$$L_S = \frac{1}{C_1(2\pi f_S)^2} \quad (3.31)$$

3.4.2.3 Switching frequency

Switching frequency should be set the same as resonant frequency in order to promise the zero current switching. Usually, the stray inductance of the circuit is already determined when the circuit layout is finished. The capacitance is also determined by the required voltage ripple. Assume the air core inductor is used for the input inductance, and the switching frequency can be determined by the input inductance value. If the input inductance is determined, the switching frequency can be twisted by monitoring the power device current when the switch is turned off. The switching frequency should be set exactly at the point when the switch current resonates to zero when the switch is turned off.

3.5 Simulation and Experiment Results

3.5.1 ZCS voltage multiplier

Figure 3.20 shows saber® simulation waveforms of a 160 W four-level ZCS voltage multiplier, where V_p and V_n are the switch gate-source control voltage, V_{ds_Sp} and

V_{ds_Sn} are the switch drain-source voltage, I_{Sp} and I_{Sn} are the switch drain-source current. $I_{C1,2,3}$ is the current through capacitor C_1 , C_2 and C_3 . I_{C4} is the current through capacitor C_4 . $V_{C1,2,3}$ is the voltage across the capacitor C_1 , C_2 and C_3 . V_{in} is the input voltage. V_o is the output voltage or the voltage across the capacitor C_4 . The input voltage is 5 V. Switching frequency is about 70 kHz. Capacitance is 47 μ F and stray inductance $L_{S2} = L_{S4} = L_{S6} = 108$ nH $L_{S1} = L_{S3} = L_{S5} = L_{S7} = 98$ nH. The simulation results is consistent with the theoretical analysis, which verifies the above analysis.

3.5.2 ZCS voltage doubler

Figure 3.21 and Figure 3.22 shows saber® simulation waveforms of a 480 W ZCS voltage doubler, where S_p and S_n are the switch gate-source control voltage, V_{ds_Sp1} , V_{ds_Sn1} , V_{ds_Sp2} , V_{ds_Sn2} are the switch drain-source voltage of switch S_{P1} , S_{N1} , S_{P2} and S_{N2} . I_{Sp1} and I_{Sn1} are the switch drain-source current of switch S_{P1} and S_{N1} . The current through S_{P2} is the same as S_{P1} , the current through S_{N2} is the same as S_{N1} . I_{in} is the current through the input stray inductance L_S . I_{C1} and I_{C2} are the current through capacitor C_1 and C_2 . V_{C1} and V_{C2} are the voltage across the capacitor C_1 and C_2 . V_{in} is the input voltage. V_o is the output voltage. The input voltage is 12 V. Switching frequency is about 44 kHz. Capacitance is 52.6 μ F and stray inductance $L_S = 110$ nH. The simulation results is consistent with the theoretical analysis, which verifies the above analysis.

In the 480 W ZCS voltage doubler prototype, the switching devices are two 30 V 180 A MOSFETs IPB009N03L from infineon connected in parallel. Resonant capacitor are

ten 100 V 4.7 μ F MLCC capacitors C5750X7R2A475K from TDK connected in parallel. Input capacitor are twelve 16 V 470 μ F conductive polymer aluminum solid electrolytic capacitors PLG1C471MDO1 from nichicon connected in parallel. Gate drive voltage is 7 V.

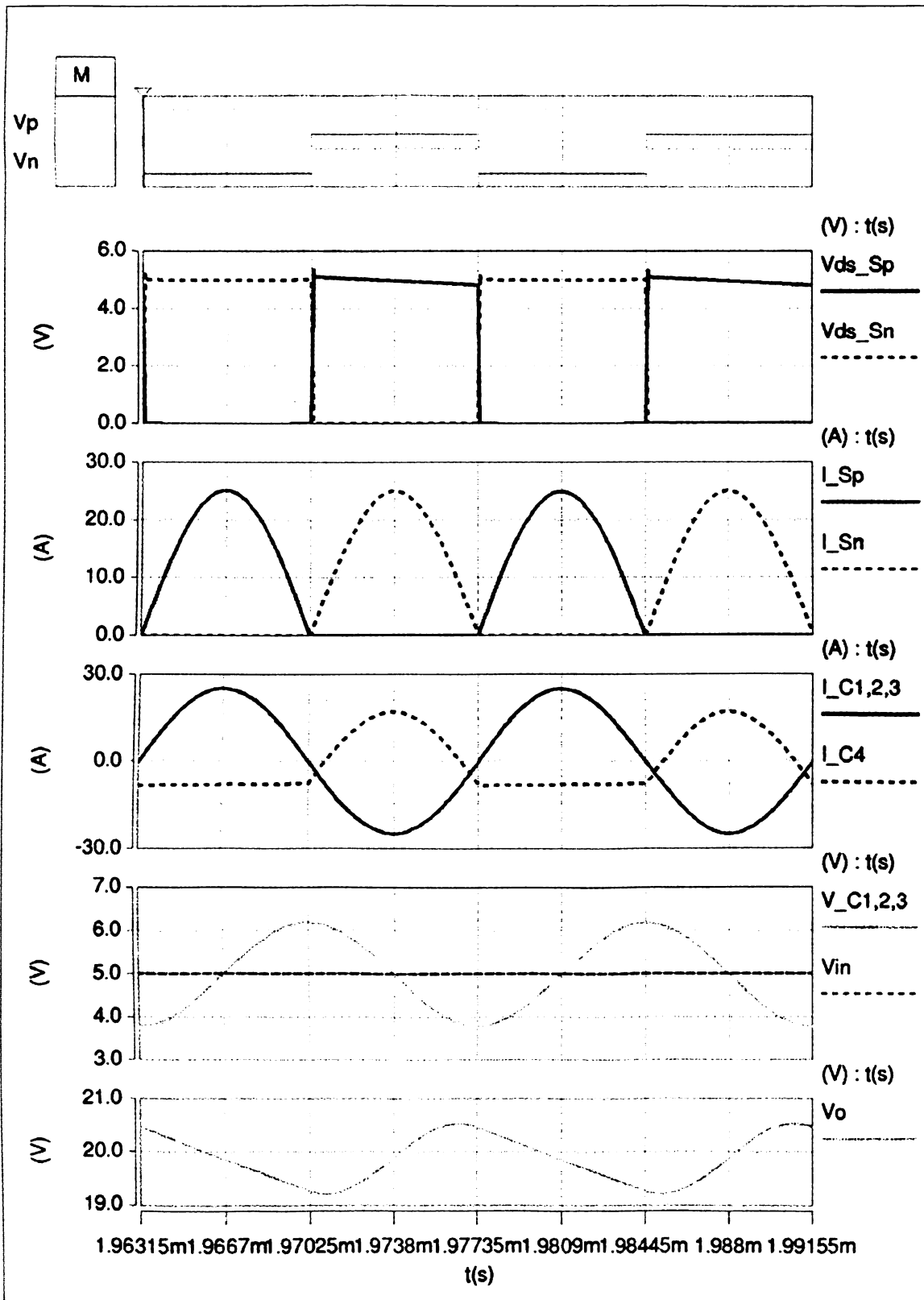


Figure 3.20 Simulation results of 160 W ZCS voltage multiplier.

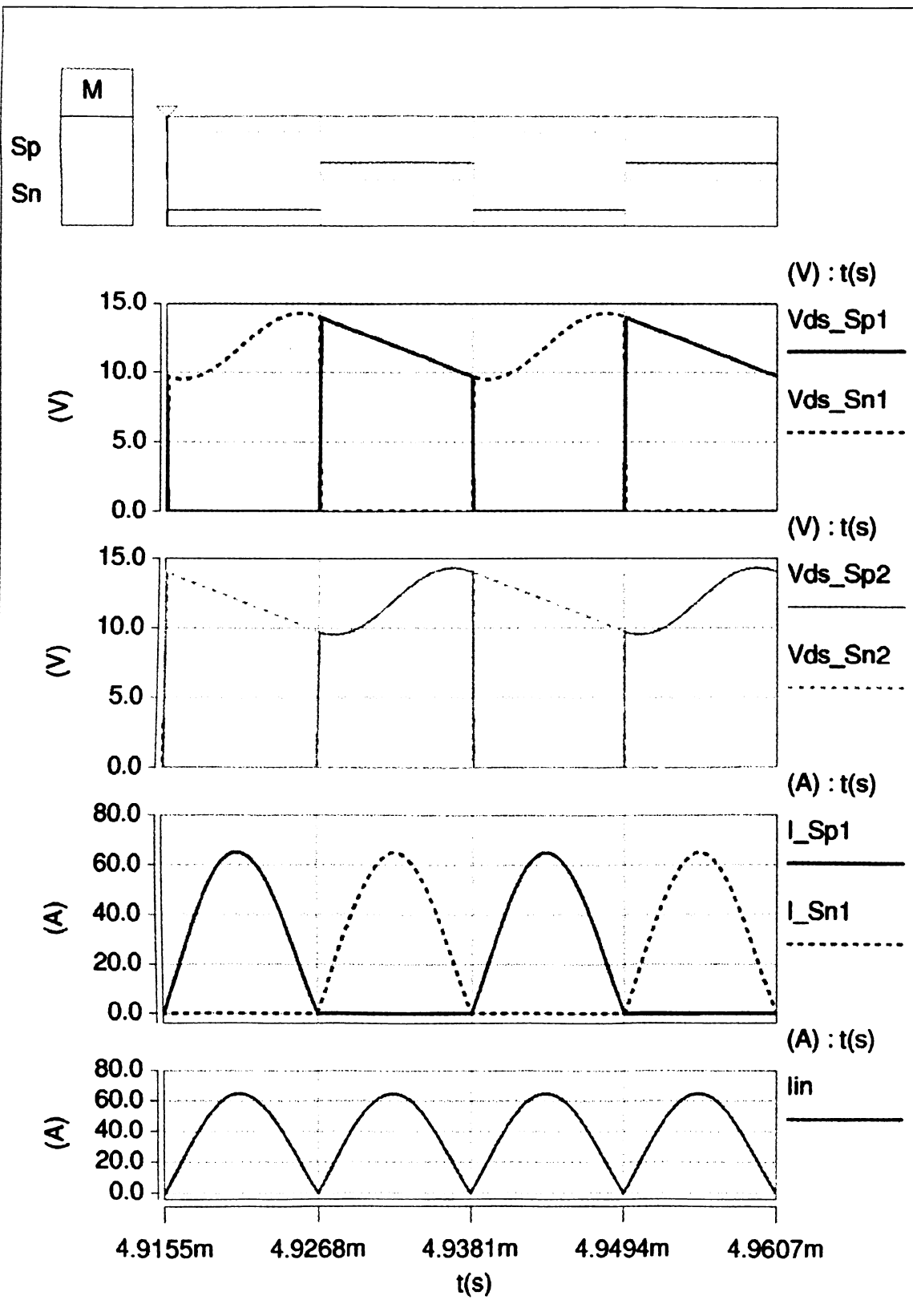


Figure 3.21 Simulation results of 480 W ZCS voltage doubler.

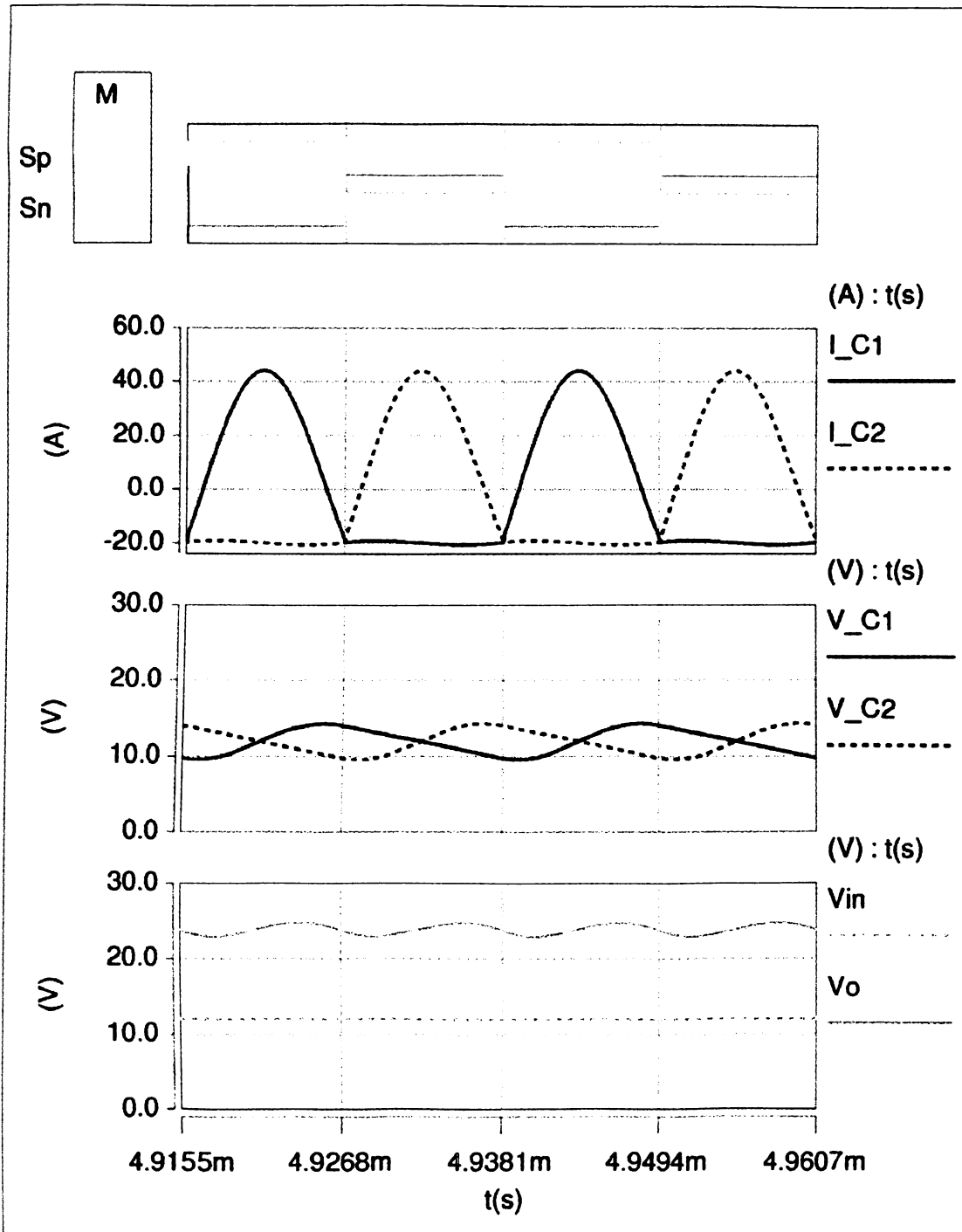


Figure 3.22 Simulation results of 480 W ZCS voltage doubler.

Figure 3.23 and Figure 3.24 show the experiment waveforms of the 480 W ZCS voltage doubler prototype with the parts mentioned above. Figure 3.23 shows the

complementary gate drive signals of S_P and S_N with duty cycle about 49% due to some dead time. V_{GS_SP} and V_{GS_SN} are the complementary gate-source control voltage.

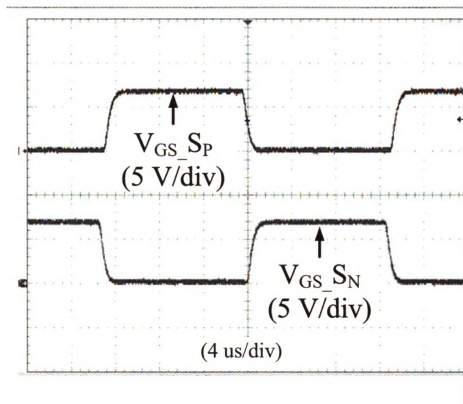


Figure 3.23 Gate drive signal of ZCS voltage doubler

Figure 3.24 shows the voltage waveforms of S_{P2} and input current waveforms. V_{GS_SP} is the gate-source voltage of S_{P2} , V_{DS_SP} is the drain-source voltage of S_{P2} and I_{IN} is the current through input stray inductance L_S . The resonant current waveform realizing ZCS is shown. Because the sum of the switch current is input current and the input current is critical discontinuous sinusoid waveform, the switch current is also zero when the switches are turned on and turned off. From the experiment results, we can derive that all the switches can achieve ZCS in both turn on and turn off.

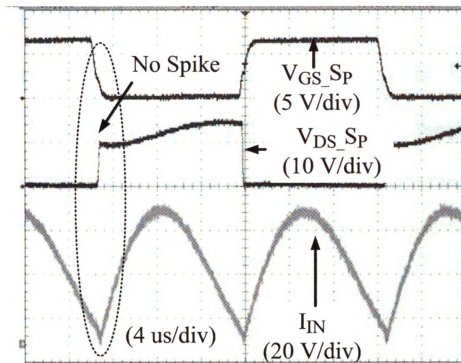


Figure 3.24 Switch voltage and input current waveform of ZCS voltage doubler

3.6 Conclusion

In this chapter, A Family of zero current switching switched-capacitor dc-dc converters has been proposed. By eliminating the bulky, lossy inductive component with a magnetic core, the converter is able to operate at very high temperatures with high efficiency. By using a soft-switching strategy, switching loss has been minimized and EMI has been restricted; the size of capacitors has been reduced, making the converter small and light. Owing to the proposed utilization of distributed stray inductance or distributed air core inserting technique, the big inductor is avoided to achieve ZCS. Hence, the proposed ZCS switched-capacitor converter family shows great potential in high temperature, high power future automotive applications.

CHAPTER 4

Improved ZCS Switched-Capacitor DC-DC Converters with Continuous Input Current for High Power Application

This chapter presents a family of ZCS switched-capacitor dc-dc converters with continuous input current. It includes all the positive characteristics of ZCS switched-capacitor dc-dc converter with small size, light weight, soft-switching and high efficiency, and it also has the prominent features of continuous input current. Compared to the traditional ZCS switched-capacitor dc-dc converters working at critical discontinuous mode with huge input current ripple, the proposed converters have continuous input current without inserting any magnetic cores. Therefore, the huge input capacitor bank in traditional ZCS switched-capacitor dc-dc converter to meet the current ripple requirement could be reduced correspondingly. The power loss related to the input capacitor ESR was reduced significantly. Smaller size, higher efficiency and higher power density switched-capacitor dc-dc converter could be made. The proposed converters show better potential in high input current and high power renewable energy application such as TEG where continuous current is preferable. Analysis, simulation and experiment results are given to demonstrate the validity and features of the proposed converter.⁴

⁴ This work is submitted in part at the 32nd International Telecommunications Energy Conference, Orlando, FL USA, June. 6 – June. 10 2010.

4.1 Introduction

To achieve small size, light weight, high efficiency and high power density dc-dc power supplies, switched-capacitor dc-dc converters has been investigated since 1970s [73, 74, 75, 76, 90, 101, 104, 106, 107, 108, 109, 110, 111, 112, 113]. For traditional switched-capacitor dc-dc converters, high voltage spike, current spike and EMI problems are common. In addition, when switching frequency is increased, the switching loss becomes more and more innegligible. For purpose of reducing the current spike, voltage spike, EMI and switching loss of switched-capacitor dc-dc converter, many ZCS type switched-capacitor dc-dc converters have been proposed [84, 85, 86, 87, 88, 103]. By inserting an inductor in series with the capacitor to resonate, zero current switching of main switches can be achieved. However, inserting a relatively big magnetic core to the switched-capacitor circuit loses the original intention of developing magnetic-less small size IC chip converters and limits the application areas [92, 93]. In the meanwhile, in high power automotive application, a huge capacitor bank has to be employed for the sake of achieving high efficiency and sustaining current ripple. [82, 83, 94, 95, 96, 97, 102]. In order to reduce the huge capacitor bank in high power application and achieve ZCS without adding extra inductors, a family of zero-current-switching switched-capacitor dc-dc converter has been proposed in chapter 3 and 4. By utilizing the distributed stray inductance present in the circuit, ZCS of all the switches can be achieved and the capacitor size can be reduced [105, 114].

However, when all the switches achieve ZCS in a sinusoid manner, the input current also becomes critical discontinuous sinusoidal waveforms shown in Figure 4.1 or Figure 4.2. Therefore, the input current ripple will be huge in high power and high input current

application. A huge input capacitor bank has to be adopted to meet the current ripple requirements and to increase efficiency. The power loss related to the input capacitor is also a big part of the converter total power loss. Also, for the renewable energy source in automotive application such as TEG, dc-dc converter with continuous input current is preferred. The output voltage ripple of the traditional ZCS switched capacitor dc-dc converter is also relatively big. Because the output capacitor also joined the resonant and a relatively small capacitance MLCC capacitor is usually used as the resonant capacitor.

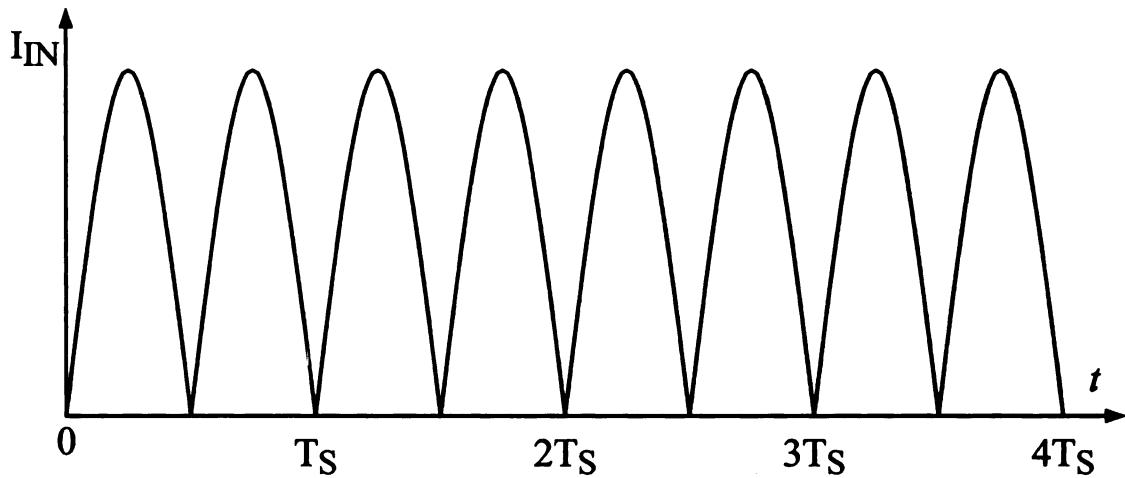


Figure 4.1 ZCS-MMSCC input current.

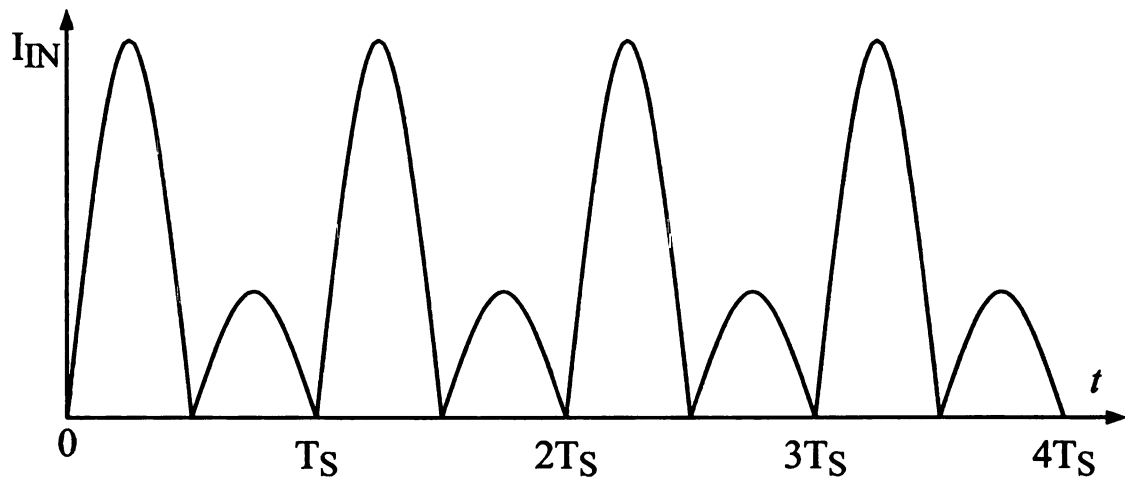


Figure 4.2 ZCS voltage multiplier input current

This chapter presents a series of ZCS switched-capacitor dc-dc converters with continuous input current, which overcomes the huge input current ripple drawbacks of traditional ZCS switched-capacitor dc-dc converter without inserting any filters. The output voltage ripple of the proposed converter is also reduced by using a relatively small output capacitor. These proposed converters employ four phase interleaved traditional ZCS switched-capacitor dc-dc converters with an extra switch in each phase and an extra common output capacitor. By operating the proposed converter with 90 degrees phase-shift angle of control signal of each phase, the input current becomes continuous with ripple current four times of switching frequency. For example, for the continuous current version ZCS-MMSCC, the input current ripple can be reduced by about 80% which means the RMS value of ripple current is also reduced by five times. Therefore, the power loss caused by the input capacitor ESR is reduced by 96% because of the square relationship between the power loss and ripple current. The huge input capacitor bank of traditional ZCS switched-capacitor dc-dc converter to meet the capacitor ripple current and thermal requirement could be eliminated. Smaller size, higher efficiency with higher input current rating switched-capacitor dc-dc converter could be made by using the proposed converter. Analysis of input current ripple reduction is given for the proposed converters. Simulation and experiment results are also given to demonstrate the validity and features of the proposed converters.

4.2 Proposed Improved ZCS Switched-Capacitor DC-DC Converters with Continuous Input Current

4.2.1 Improved ZCS-MMSCC with continuous input current

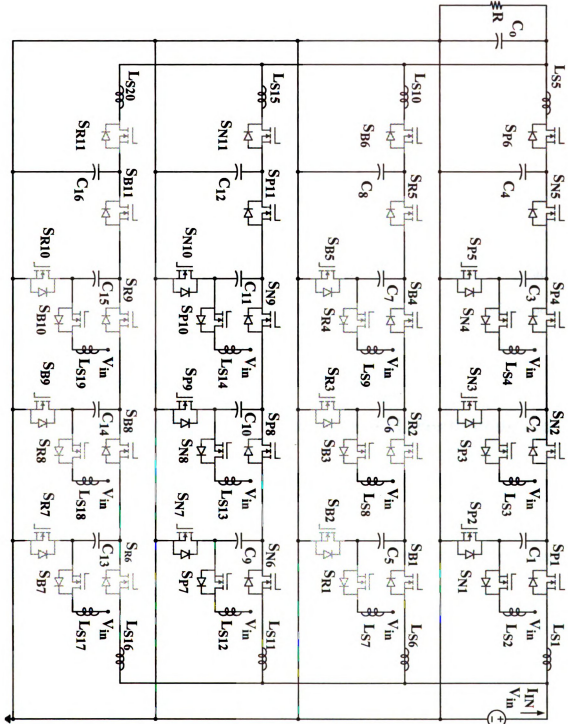


Figure 4.3 Proposed ZCS-MMSCC 10 with continuous input current main circuit

Figure 4.3 shows a four-level ZCS-MMSCC with continuous input current main circuit as an example. The circuit also works as a four times step-up converter.

Four phase traditional ZCS-MMSCCs are connected in parallel with the same input voltage source. Each phase is controlled with 90 degrees phase shift. Only four different control signals are needed because of the special structure of the ZCS-MMSCC. One extra switch is added in each phase of the traditional ZCS-MMSCC, which are S_{P6} , S_{B6} , S_{N11} and S_{R11} . The added switches are also controlled with 90 degrees phase shift and ZCS can be also achieved. One output capacitor with higher capacitance is added to reduce the output voltage ripple. The output capacitor with higher capacitance can be treated as a voltage source considering the resonant of stray inductance of the added switch and original output capacitor of ZCS-MMSCC to achieve the ZCS of the added switches. The required stray inductance of the extra switch to achieve the ZCS is the same with the first resonant loop, for example, $L_{S5} = L_{S1}$.

4.2.2 Improved ZCS voltage multiplier with continuous input current

Figure 4.4 shows a four-level ZCS voltage multiplier with continuous input current main circuit as an example. Similar to the ZCS-MMSCC with continuous input current this circuit also works as a four times step-up converter. Four phase ZCS voltage multipliers are connected in parallel with the same input voltage source. Each phase is controlled with 90 degrees phase shift. Only four different control signals are needed because of the special structure of the ZCS voltage multiplier. One extra switch is added in each phase of the ZCS voltage multiplier, which are S_{P7} , S_{N11} , S_{B7} and S_{R11} . The added switches are also controlled with 90 degrees phase shift and ZCS can be also achieved.

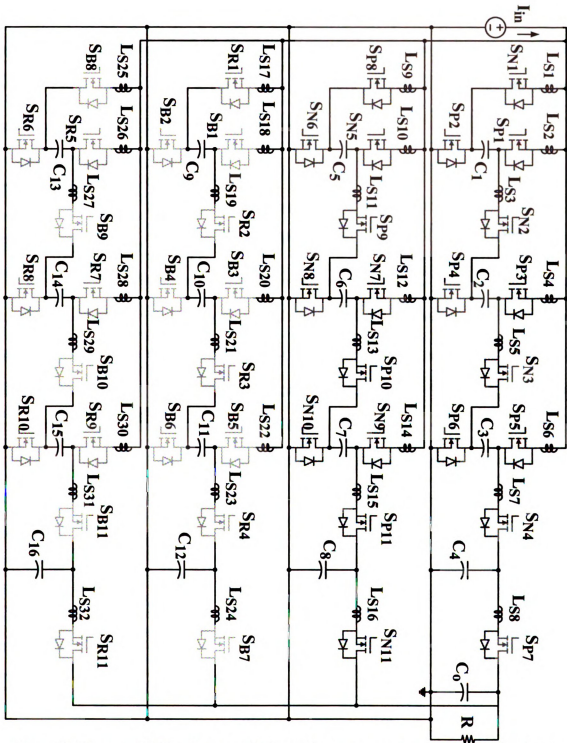


Figure 4.4 Proposed ZCS voltage multiplier with continuous input current main circuit

One output capacitor with higher capacitance is added to reduce the output voltage ripple. The output capacitor with higher capacitance can be treated as a voltage source

considering the resonant of stray inductance of the added switch and original output capacitor of ZCS voltage multiplier to achieve the ZCS of the added switches. The required stray inductance of the extra switch to achieve the ZCS is the same with all the other equivalent stray inductance, for example, $L_{S8} = L_{S1} = L_{S2}$.

4.3 Operation Principles

4.3.1 Improved ZCS-MMSCC with continuous input current

Figure 4.5 shows the idealized waveforms of the ZCS-MMSCC with continuous input current. There are only four different control signals with 90 degrees phase shift. Because of the special structure of ZCS-MMSCC with complementary control signal and 50% duty cycle, the control signal of the third phase is 180 degrees phase shift of the first phase where the control signal of the first phase could still be used for the third phase. Compared to the traditional ZCS-MMSCC, the current of each switch is reduced by four times. The input current is become continuous with current ripple only 20% of the traditional ZCS-MMSCC. There are four states in total of the new converter compared to two states of traditional ZCS-MMSCC. During each state, two types of switches turn on while the others turn off. Each state has the same equivalent circuit which means the impedance of each state is the same. So the input current of each state is the same.

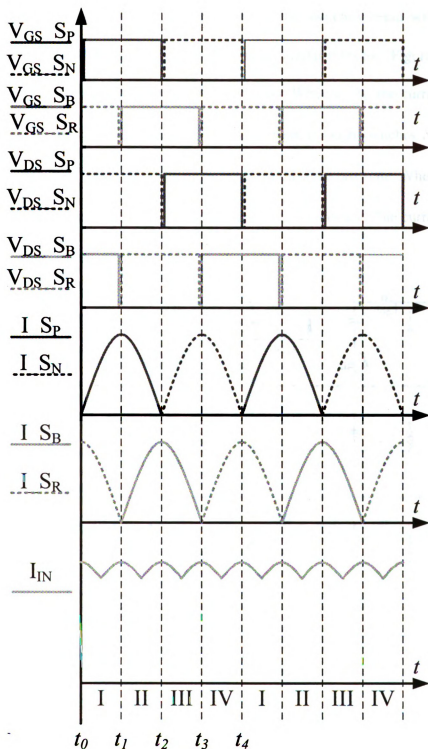


Figure 4.5 Ideal waveforms of ZCS-MMSCC with continuous input current.

4.3.1.1 State I [$t_0 - t_1$]

In the following analysis, S_P will represent all the switches begin with S_P with numbers after it. And all the other switches follow the similar rules too. Figure 4.6 shows the operation mode of state I with S_P and S_R conduct. When $t = t_0$, the current through switches S_P begin to increase from zero, and the current through switches S_R begin to decrease from the maximum point, since S_R is turned on since last state. When $t = t_1$ the current through S_R resonate to zero and S_R turn off at zero current. The current through switches S_P reach the maximum point.

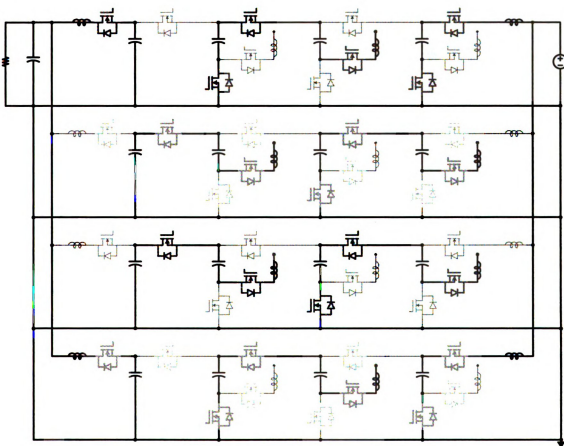


Figure 4.6 State I S_P and S_R conduct.

Figure 4.7, Figure 4.8, Figure 4.9, and Figure 4.10 shows the equivalent simplified circuits of State I. It can be shown from the figure that there are eight loops connected

with the input voltage source which mean the input current is divided by eight times. Two loops are connected with output capacitor, which means output current is divided by two times. By using one extra switch, the output capacitor is decoupled with the input voltage source. Because the output capacitor C_o is big enough, only L_{S5} and C_4 will resonate.

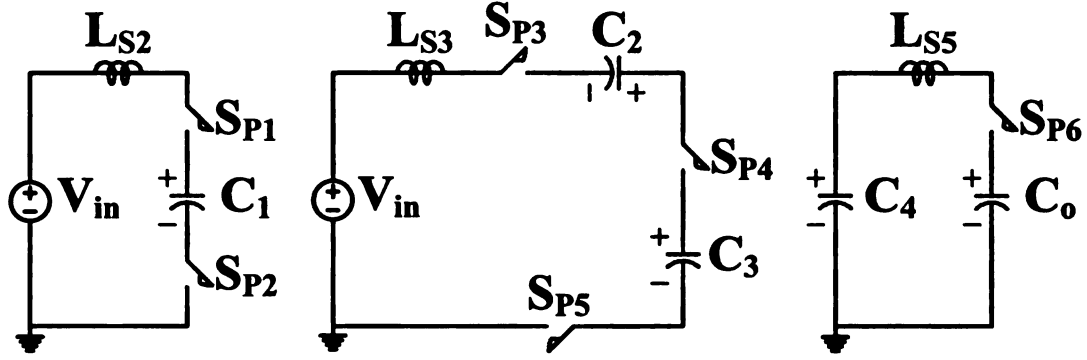


Figure 4.7 Simplified equivalent circuits of state I (a)

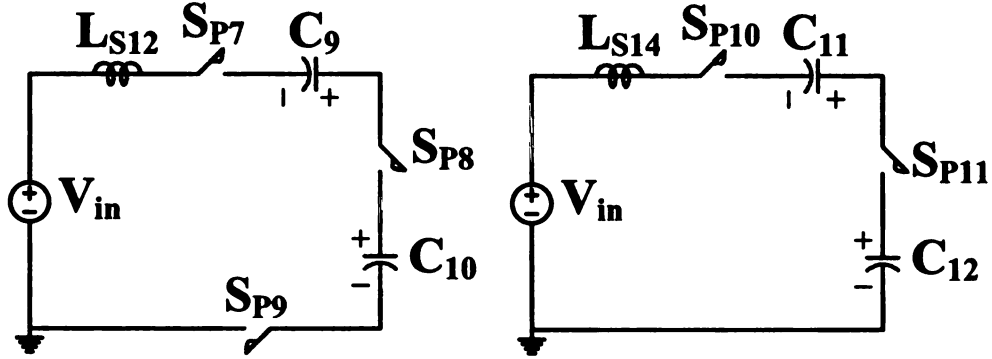


Figure 4.8 Simplified equivalent circuits of state I (b)

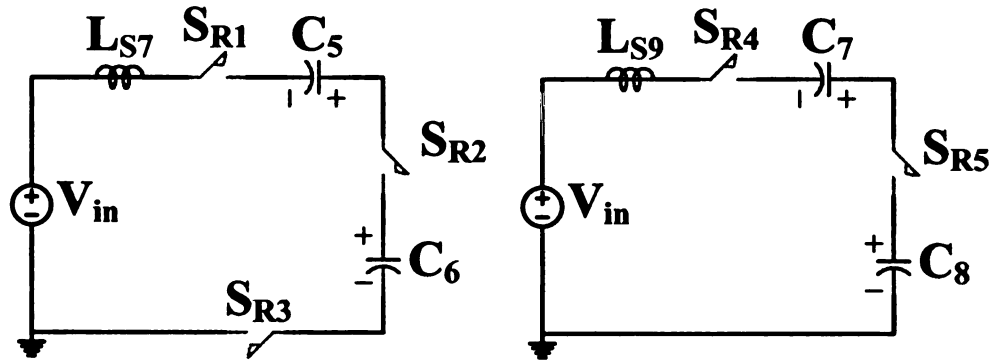


Figure 4.9 Simplified equivalent circuits of state I (c)

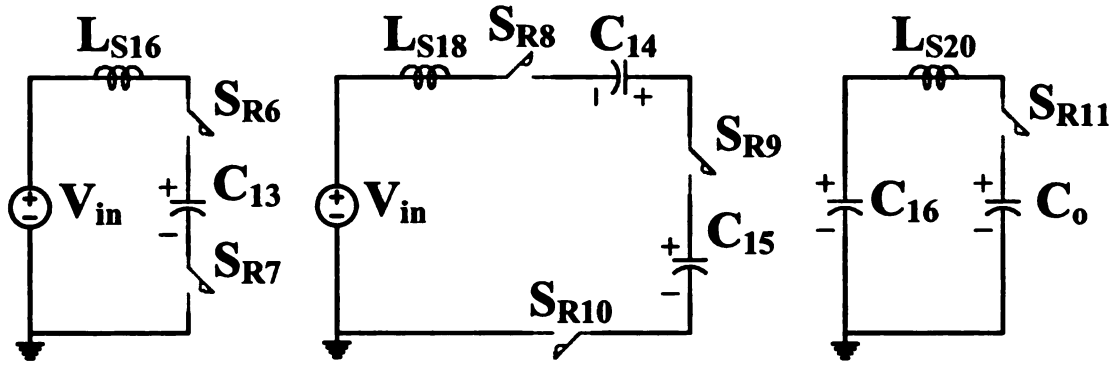


Figure 4.10 Simplified equivalent circuits of state I (d)

It can be also derived that, for first and third loop shown in Figure 4.7 and for the first and third loop shown in Figure 4.10, the needed stray inductance value is two times smaller than other resonant loop, because there is only one capacitor in the resonant loop compared to others with two capacitors in series for resonating.

4.3.1.2 State II [$t_1 - t_2$]

Figure 4.11 shows the operation mode of state II with S_P and S_B conduct. When $t = t_1$, the current through S_P begin to decrease from the maximum point. And the current through S_B begin to increase from zero. When $t = t_2$, the current through S_P decreased to zero, and zero current turn off of S_P can be achieved. The current through switches S_B reach its maximum point.

Figure 4.12, Figure 4.13, Figure 4.14, Figure 4.15 shows the equivalent simplified circuits of State II. Similar to State I, this state still have eight loops with input voltage source. And two loops with output capacitor. The required stray inductance for each resonant loop to achieve ZCS is similar with state I too. There are four loop with only one capacitor in the resonant loop, which means the required stray inductance is also smaller than other loops with two capacitors in series for resonant.

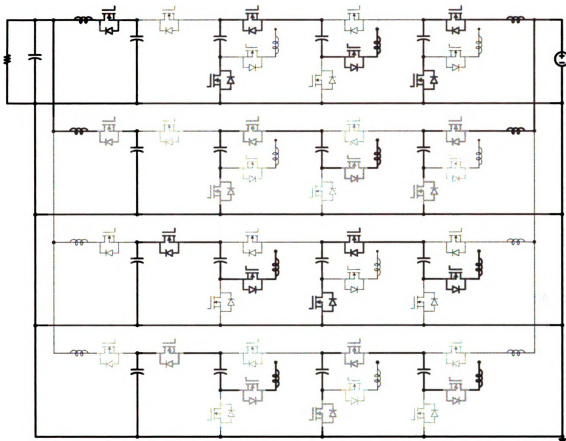


Figure 4.11 State II S_P and S_B conduct.

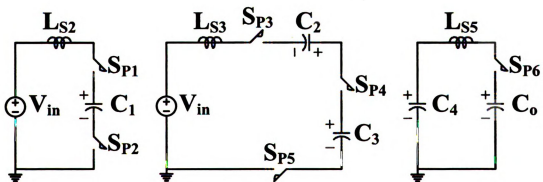


Figure 4.12 Simplified equivalent circuits of state II (a)

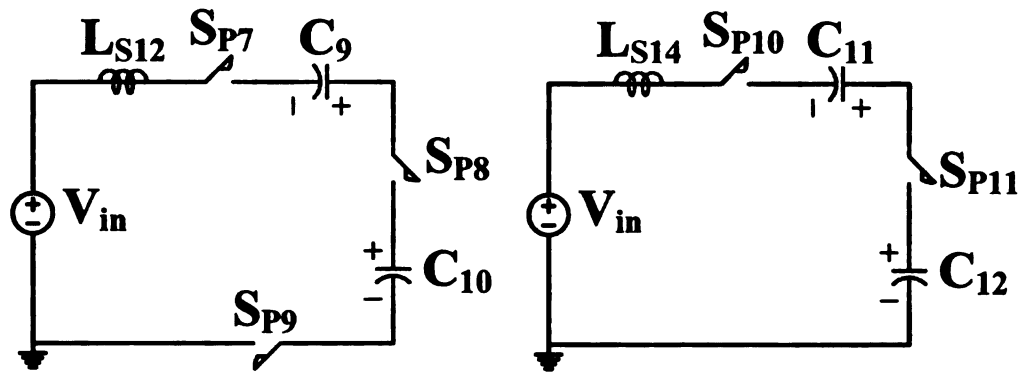


Figure 4.13 Simplified equivalent circuits of state II (b)

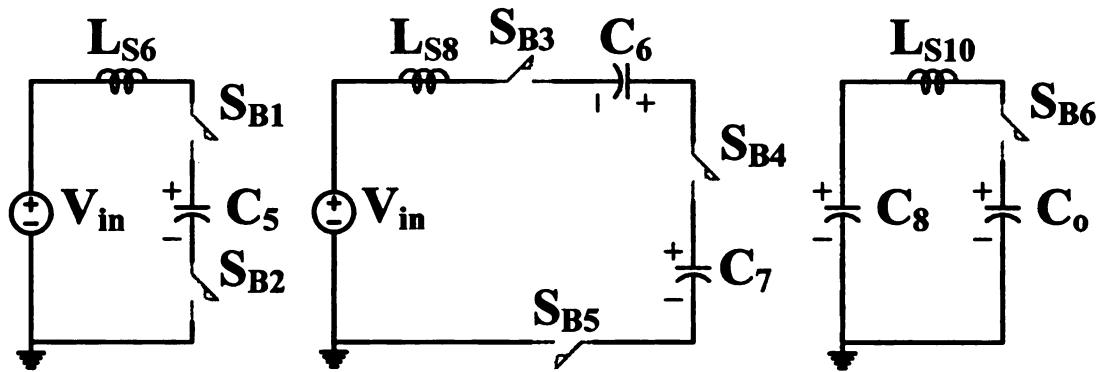


Figure 4.14 Simplified equivalent circuits of state II (c)

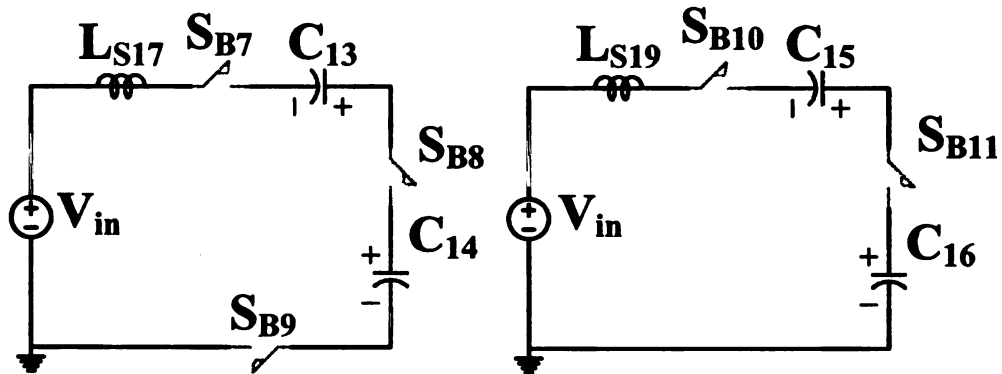


Figure 4.15 Simplified equivalent circuits of state II (d)

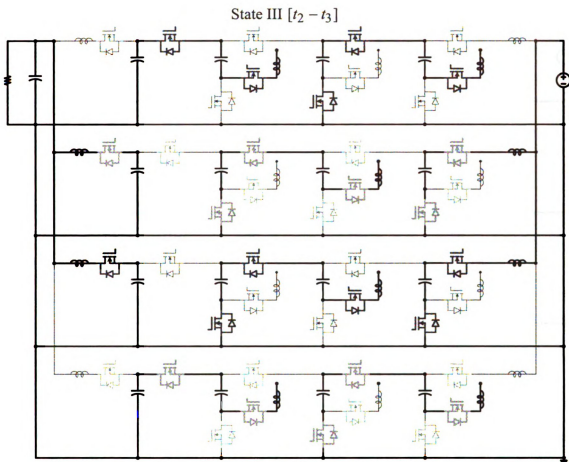


Figure 4.16 shows the operation mode of state II with S_N and S_B conduct. When $t = t_2$, the current through S_B begin to decrease from the maximum point. And the current through S_N begin to increase from zero since S_P is already turned off during last state. When $t = t_3$, the current through S_B decreased to zero, and zero current turn off of S_B can be achieved. The current through switches S_N reach its maximum point.

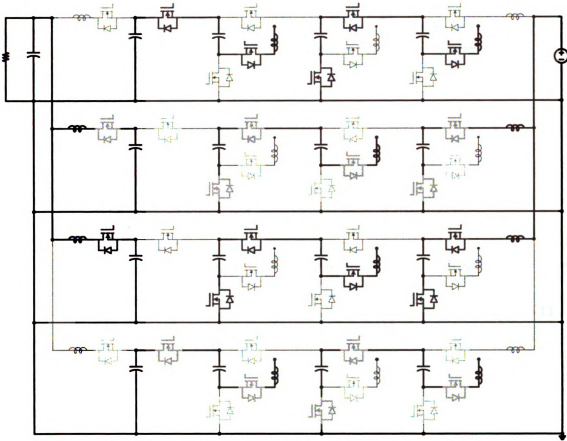


Figure 4.16 State III S_N and S_B conduct.

Figure 4.17, Figure 4.18, Figure 4.19, Figure 4.20 shows the equivalent simplified circuits of State III. Similar to State I, this state still have eight loops with input voltage source. And two loops with output capacitor. The required stray inductance for each resonant loop to achieve ZCS is similar with state I too. There are four loop with only one capacitor in the resonant loop, which means the required stray inductance is also smaller than other loops with two capacitors in series for resonant. The only difference is the conduction switch is changed from S_P and S_R to S_N and S_B .

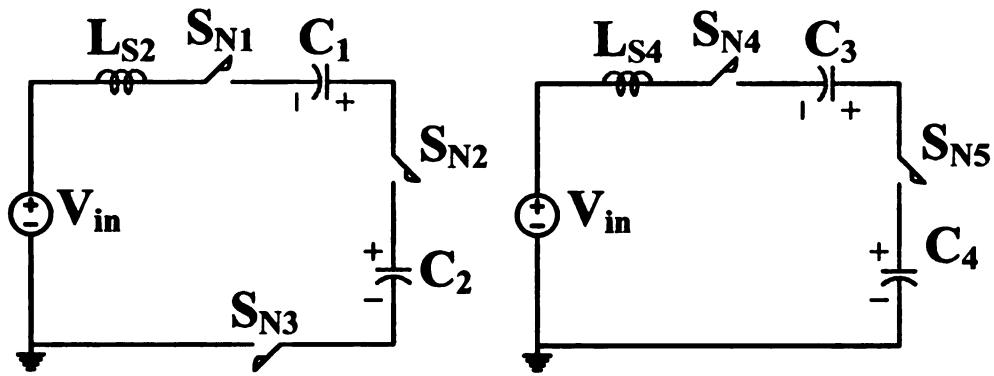


Figure 4.17 Simplified equivalent circuits of state III (a)

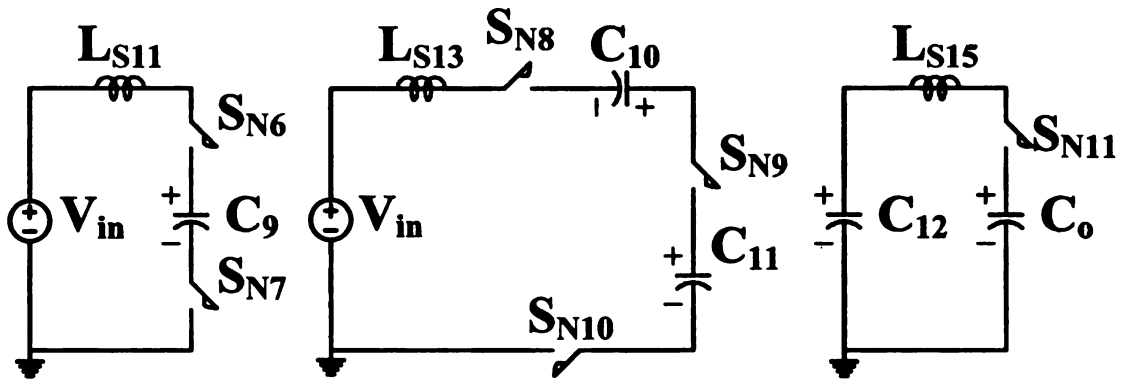


Figure 4.18 Simplified equivalent circuits of state III (b)

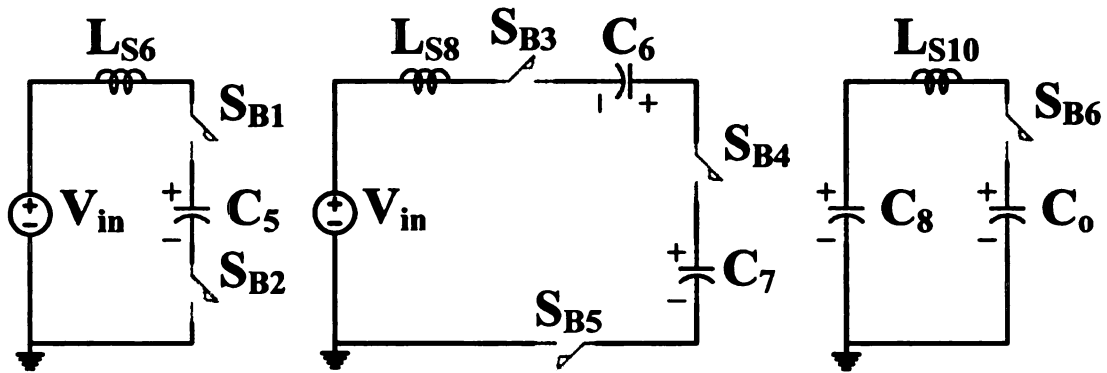


Figure 4.19 Simplified equivalent circuits of state III (c)

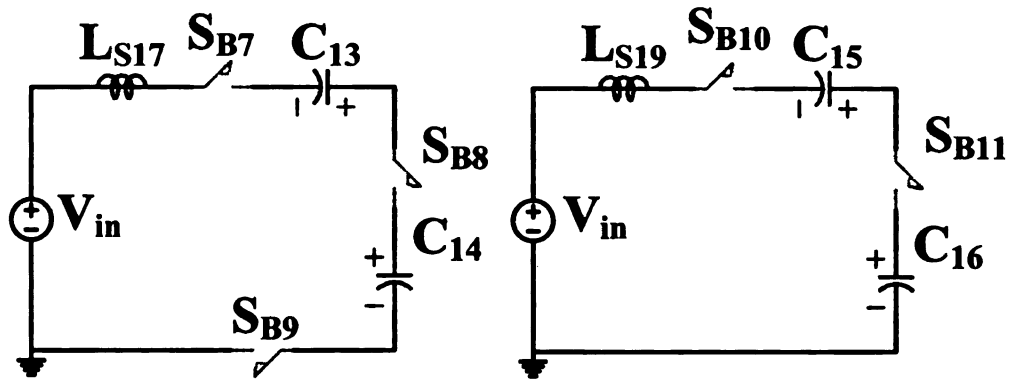


Figure 4.20 Simplified equivalent circuits of state III (d)

4.3.1.3 State IV [$t_3 - t_4$]

Figure 4.21 shows the last operation mode of state IV with S_N and S_R conduct. When $t = t_3$, the current through S_N begin to decrease from the maximum point. And the current through S_R begin to increase from zero since S_B is already turned off during last state. When $t = t_4$, the current through S_N decreased to zero, and zero current turn off of S_N can be achieved. The current through switches S_R reach its maximum point. And one period is over. In the next period, the switches will repeat the operation from State I. Figure 4.22 - Figure 4.25 shows the equivalent simplified circuits of State IV. The description of operation is omitted here, since it is similar with other state.

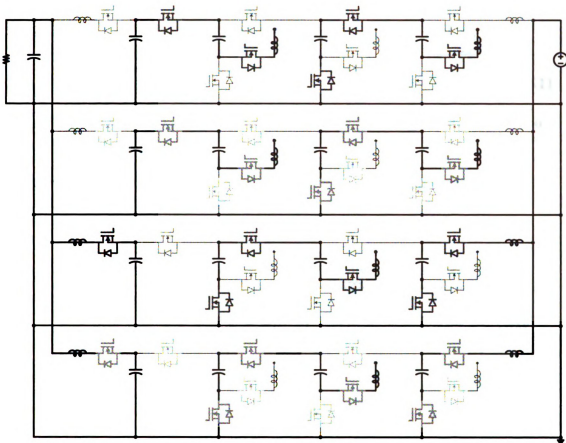


Figure 4.21 State IV S_N and S_R conduct.

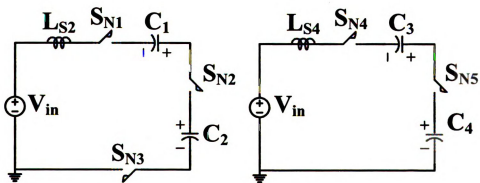


Figure 4.22 Simplified equivalent circuits of state IV (a)

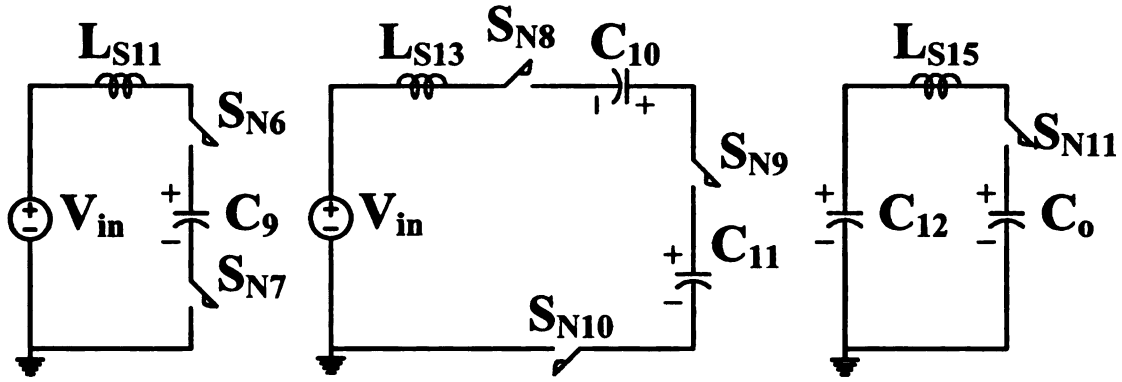


Figure 4.23 Simplified equivalent circuits of state IV (b)

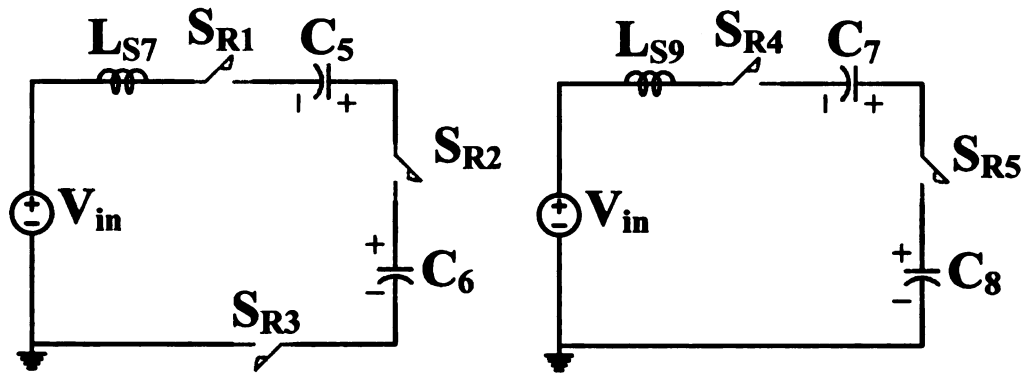


Figure 4.24 Simplified equivalent circuits of state IV (c)

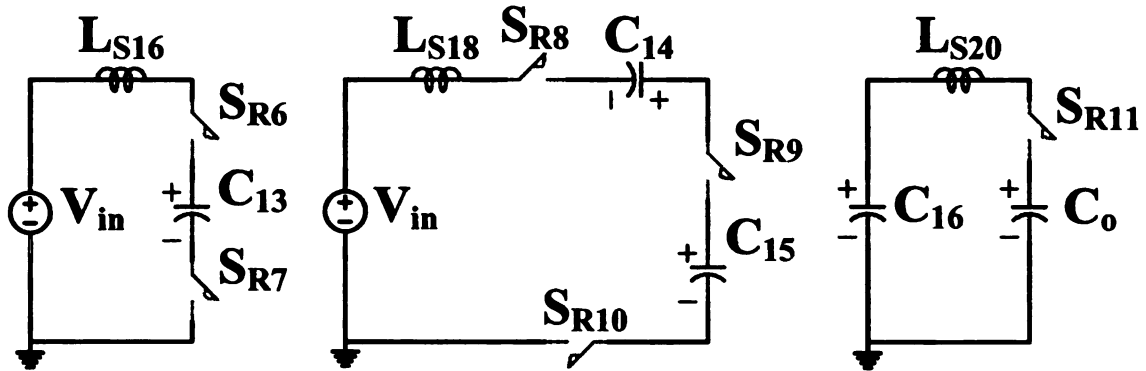


Figure 4.25 Simplified equivalent circuits of state IV (d)

4.3.2 Improved ZCS voltage multiplier with continuous input current

Figure 4.26 shows the idealized waveforms of the improved ZCS voltage multiplier with continuous input current. Similar with ZCS-MMSCC with continuous input current,

there are also four different control signals with 90 degrees phase shift. Because the ZCS voltage multiplier also has complementary control with 50% duty cycle. When four phases ZCS voltage multiplier with four extra switches and one output capacitor interleaved together, only four different control signals with 90 degrees phase shift angle from each other are needed. Compared to the traditional ZCS voltage multiplier, the current of each switch is reduced by four times due to the four phase interleaving strategy. The input current is become continuous, compared to the discontinuous current with different peak current of traditional ZCS voltage multiplier. Similar to the ZCS-MMSCC with continuous input current, there are also four states in total of the new converter compared to two states of traditional ZCS voltage multiplier. During each state, two types of switches turn on while the others turn off. In each state, there are two phases circuit charges all the capacitor in parallel, while other two phases with all the capacitors in series with the input voltage source and charge the last capacitor. Because of the inserting of the extra switch, there are two extra loop in each state with the last resonant capacitor such as C_4 and C_{16} in the first state to charge the output capacitor C_o . In this case, each state has the same equivalent circuit which means the impedance of each state is the same. So the input current of each state is the same similar to the ZCS-MMSCC with the continuous input current.

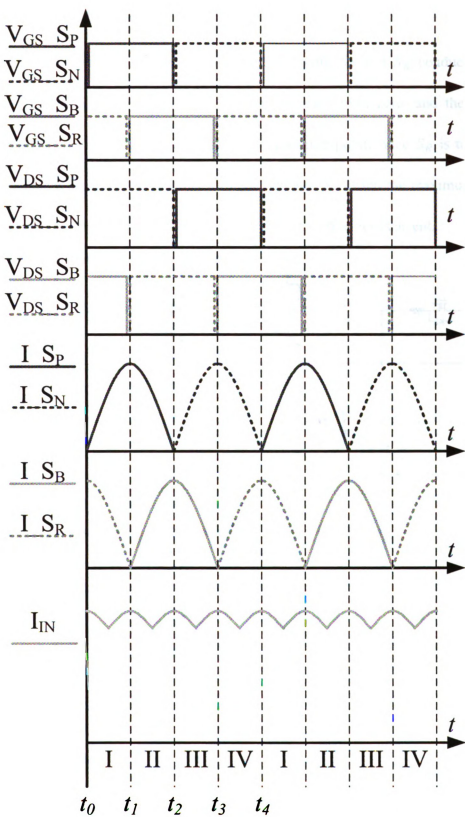


Figure 4.26 Ideal waveforms of ZCS voltage multiplier with continuous input current.

4.3.2.1 State I [$t_0 - t_1$]

Figure 4.27 shows the operation mode of state I with S_P and S_R conduct. When $t = t_0$, the current through switches S_P begin to increase from zero, and the current through switches S_R begin to decrease from the maximum point, since S_R is turned on since last state. When $t = t_1$ the current through switches S_P reach the maximum point. And the current through S_R resonate to zero and S_R turn off at zero current.

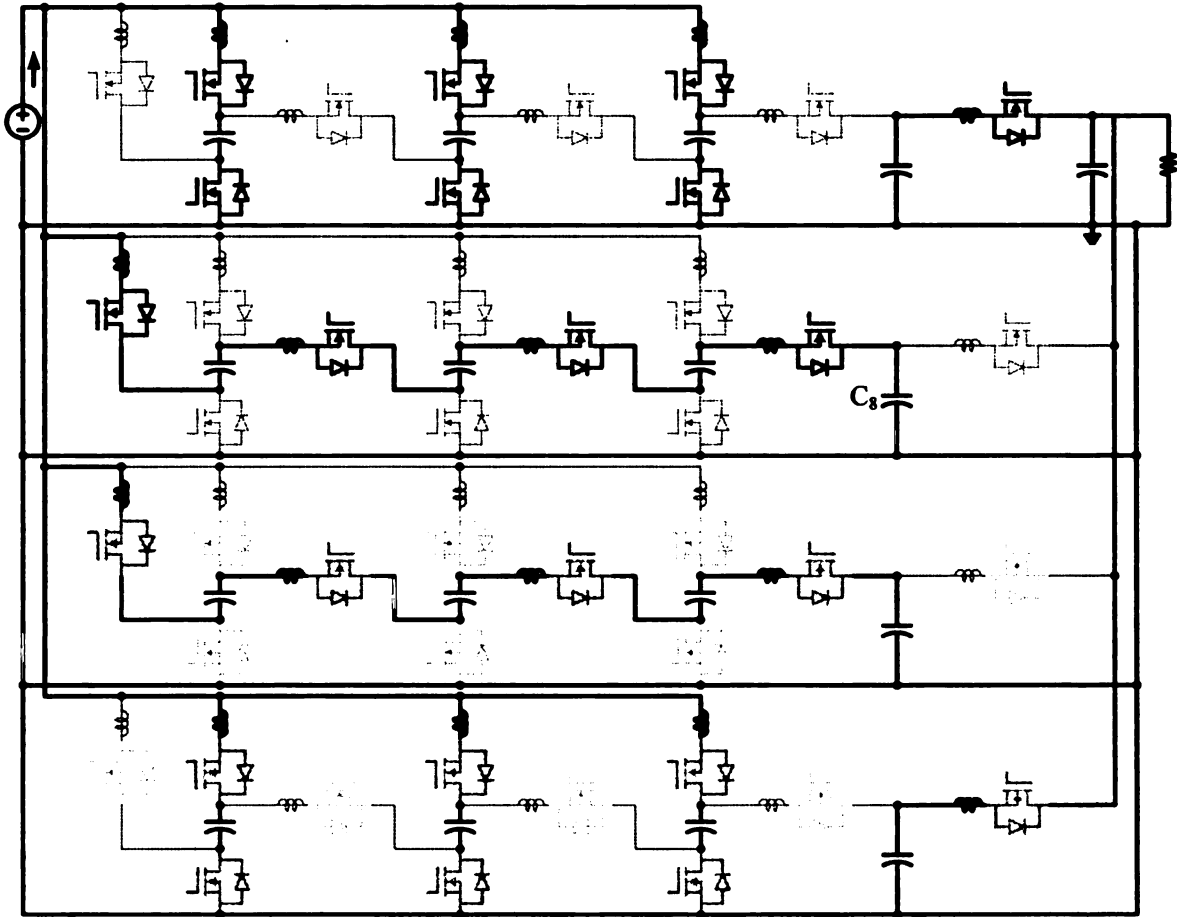


Figure 4.27 State I S_P and S_R conduct.

Figure 4.28 - Figure 4.31 shows the simplified equivalent circuit of State I. Similarly to ZCS-MMSCC with continuous input current, there are also ten resonant loops in each state, eight of them are connected with input voltage, and two of them are connected with

output capacitor. Different with ZCS-MMSCC with continuous current, there are only equivalent circuits with one resonant capacitor or four capacitors in series. If the level is increased, the capacitors in series will also be increased.

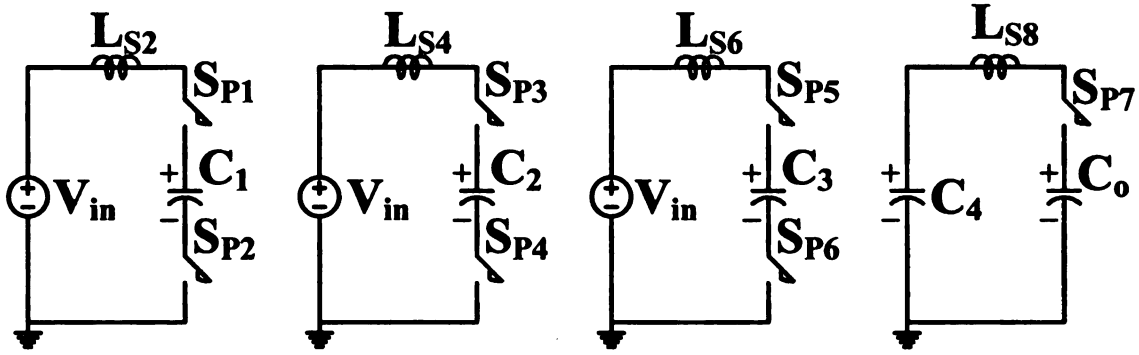


Figure 4.28 Simplified equivalent circuits of state I (a)

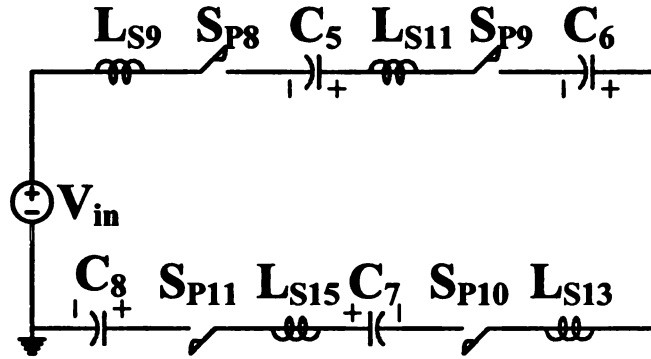


Figure 4.29 Simplified equivalent circuits of state I (b)

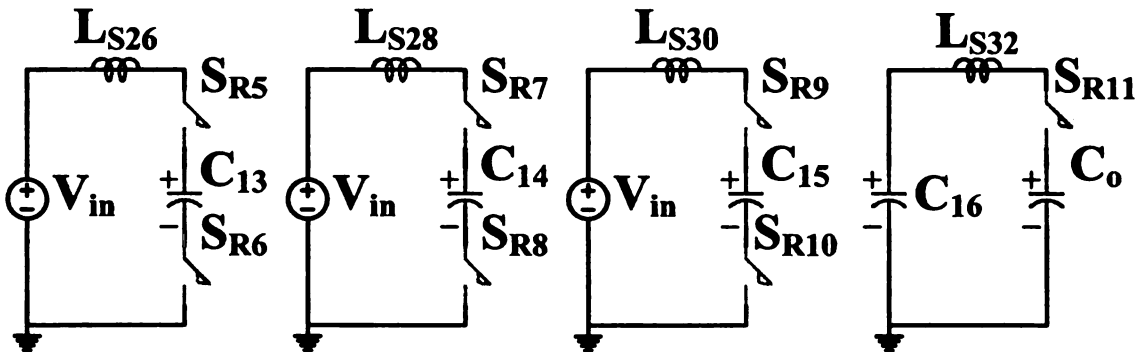


Figure 4.30 Simplified equivalent circuits of state I (c)

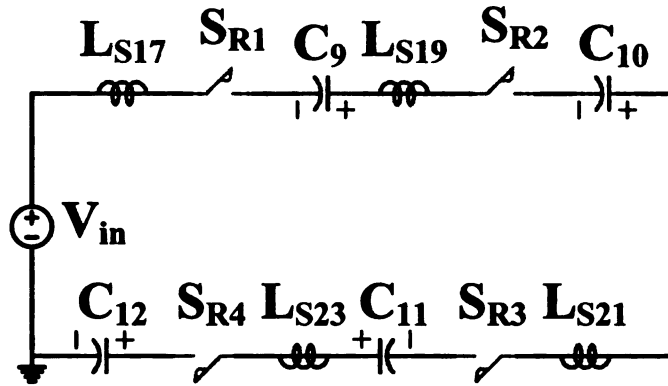


Figure 4.31 Simplified equivalent circuits of state I (d)

4.3.2.2 State II $[t_1 - t_2]$

Figure 4.32 shows the operation mode of state II with S_P and S_B conduct.

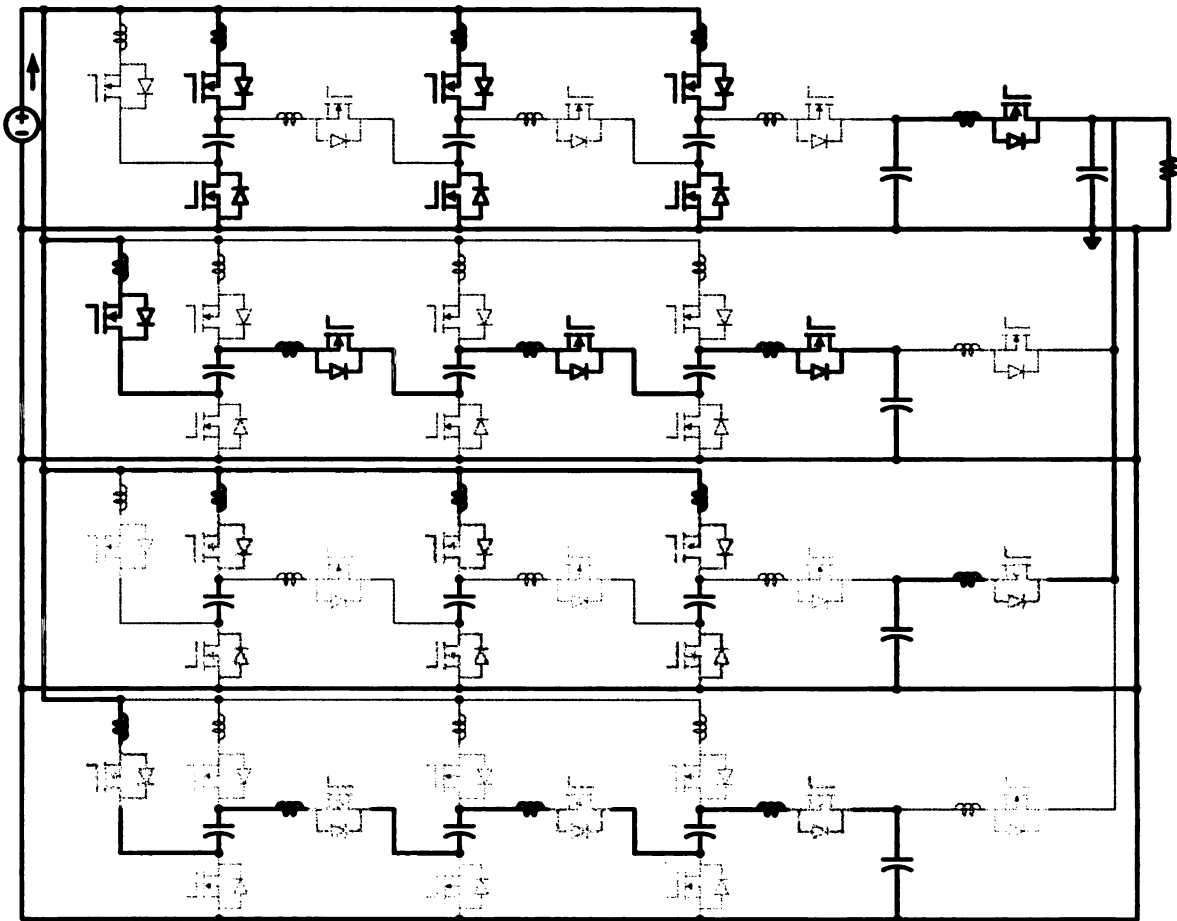


Figure 4.32 State II S_P and S_B conduct.

When $t = t_1$, the current through switches S_B begin to increase from zero, and the current through switches S_P begin to decrease from the maximum point, since S_P is turned on since state I. When $t = t_2$ the current through switches S_B reach the maximum point. And the current through S_P resonate to zero and S_P turn off at zero current.

Figure 4.33 - Figure 4.36 shows the simplified equivalent circuit of State II.

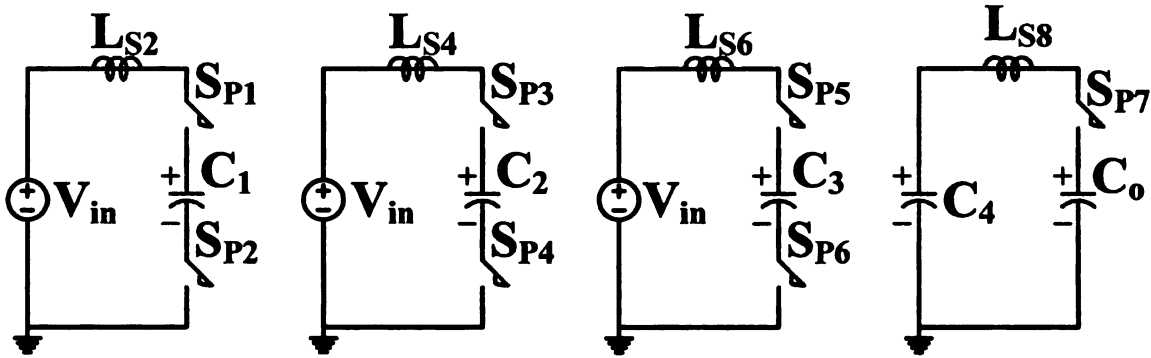


Figure 4.33 Simplified equivalent circuits of state II (a)

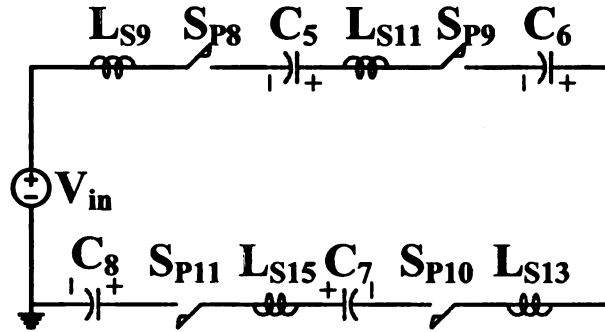


Figure 4.34 Simplified equivalent circuits of state II (b)

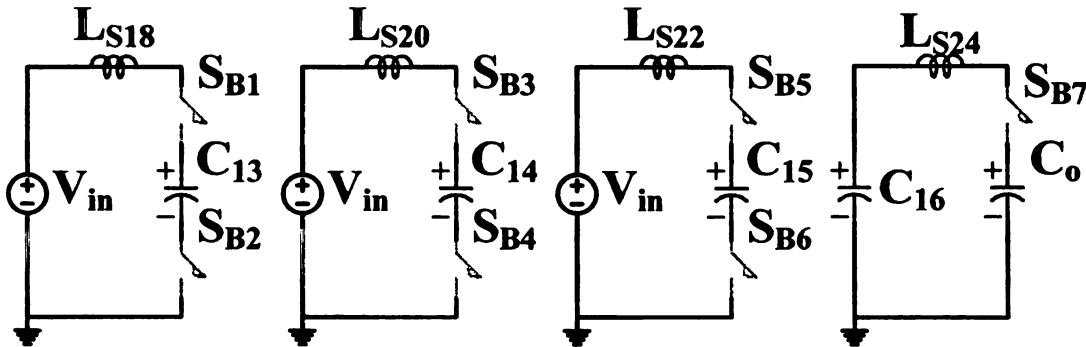


Figure 4.35 Simplified equivalent circuits of state II (c)

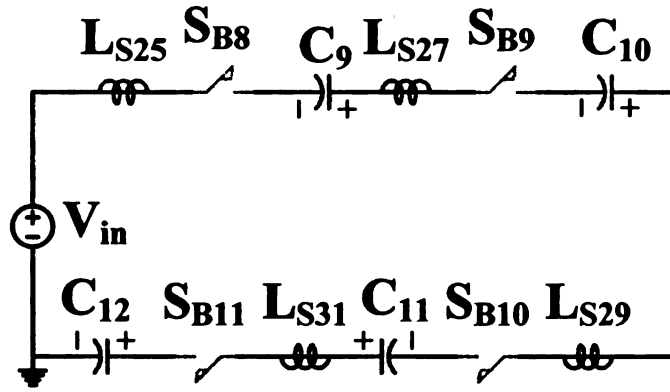


Figure 4.36 Simplified equivalent circuits of state II (d)

4.3.2.3 State III [$t_2 - t_3$]

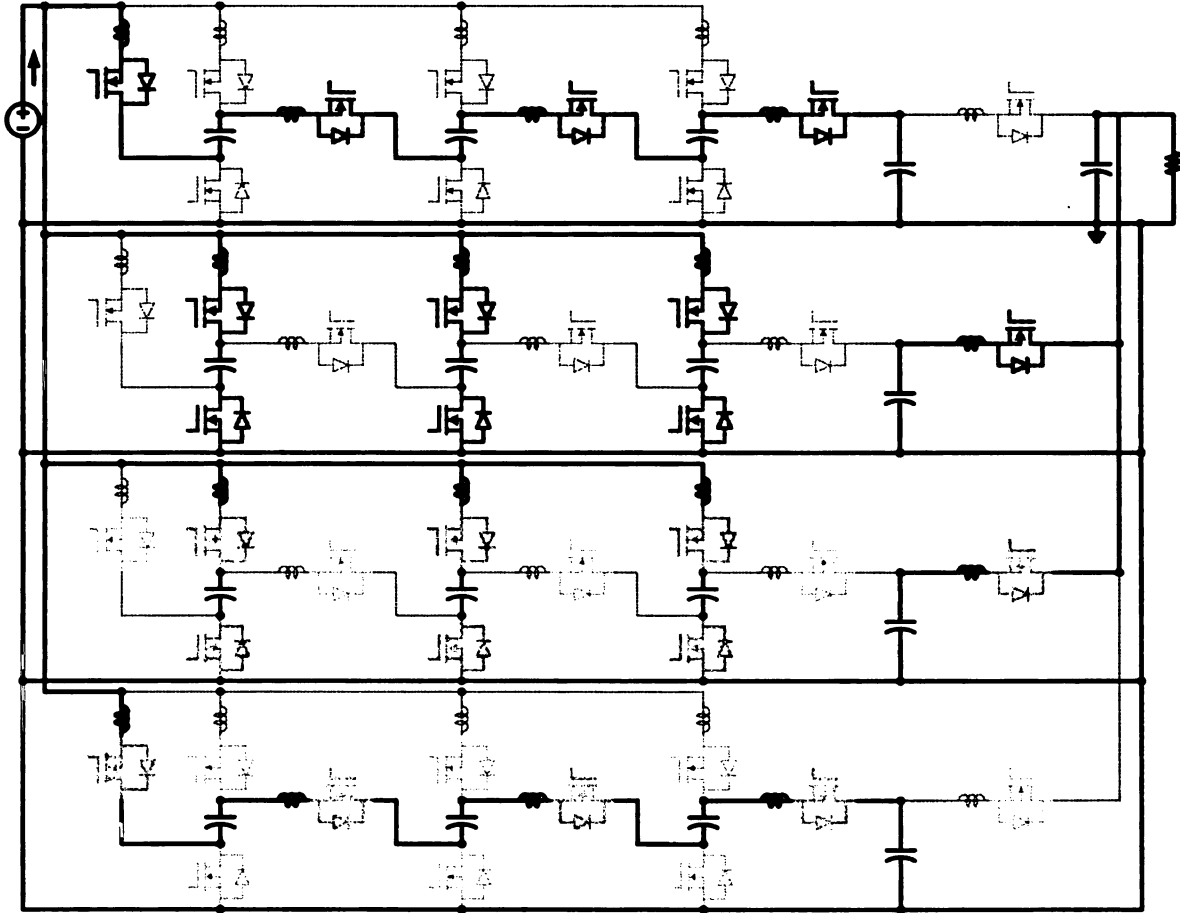


Figure 4.37 State III S_N and S_B conduct.

Figure 4.37 shows the operation mode of state III with S_N and S_B conduct. Figure 4.38 - Figure 4.41 shows the simplified equivalent circuit of State III. When $t = t_2$, the

current through switches S_N begin to increase from zero, and the current through switches S_B begin to decrease from the maximum point, since S_B is turned on since state II. When $t = t_3$ the current through switches S_N reach the maximum point. And the current through S_B resonate to zero and S_B turn off at zero current.

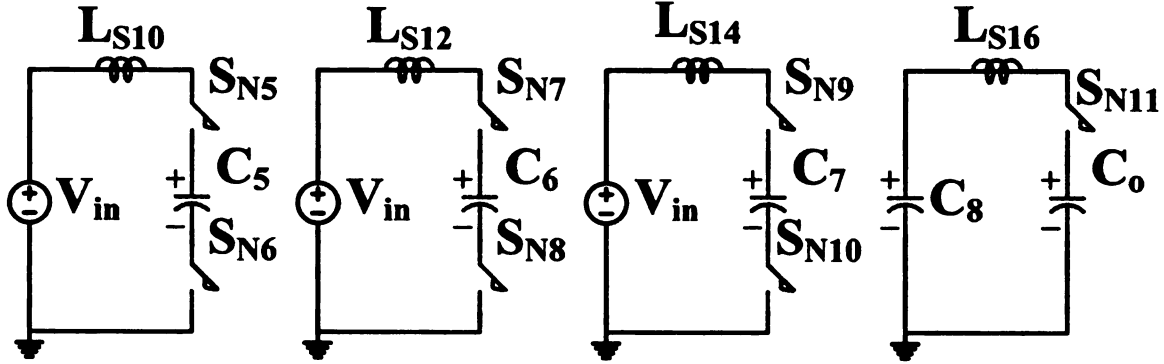


Figure 4.38 Simplified equivalent circuits of state III (a)

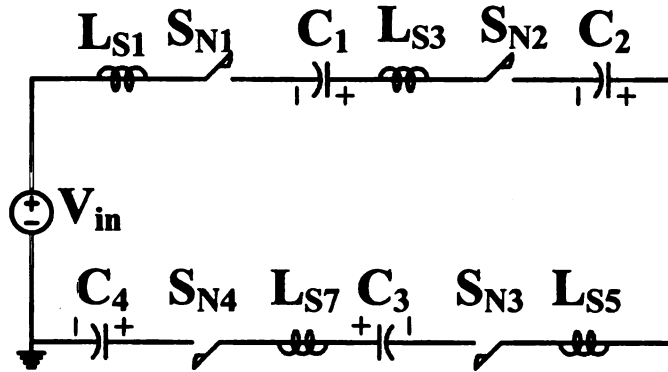


Figure 4.39 Simplified equivalent circuits of state III (b)

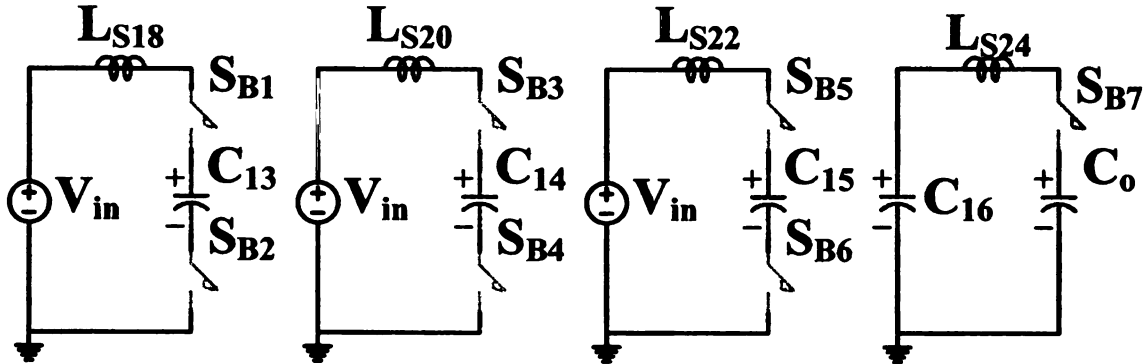


Figure 4.40 Simplified equivalent circuits of state III (c)

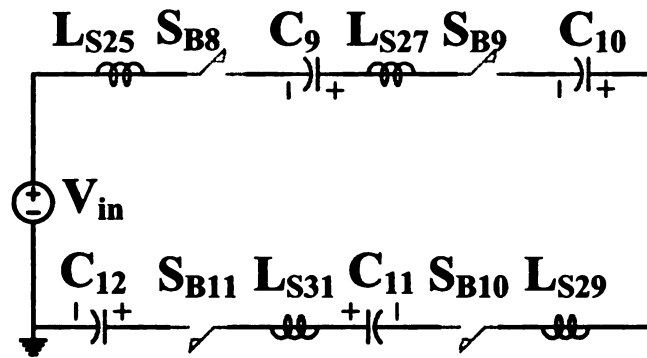


Figure 4.41 Simplified equivalent circuits of state III (d)

4.3.2.4 State IV [$t_3 - t_4$]

Figure 4.42 shows the operation mode of state IV with S_N and S_R conduct. Figure 4.38 - Figure 4.46 shows the simplified equivalent circuit of State IV. All the operation is similar with the other states, the detail analysis will be omitted.

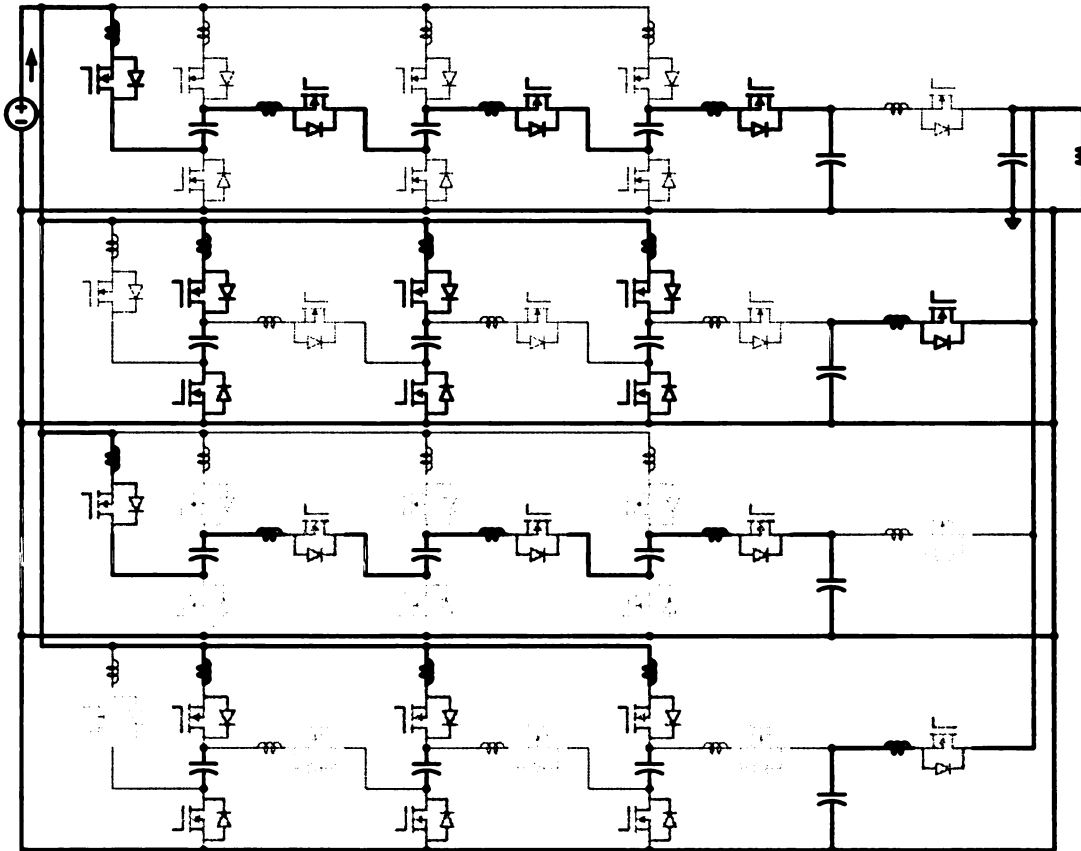


Figure 4.42 State IV S_N and S_R conduct.

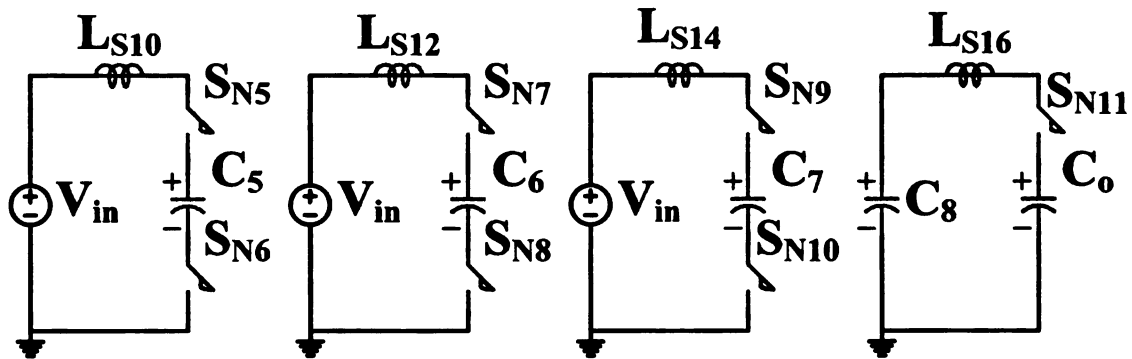


Figure 4.43 Simplified equivalent circuits of state IV (a)

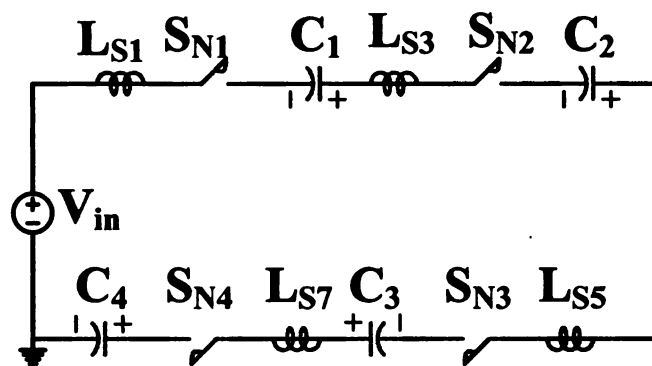


Figure 4.44 Simplified equivalent circuits of state IV (b)

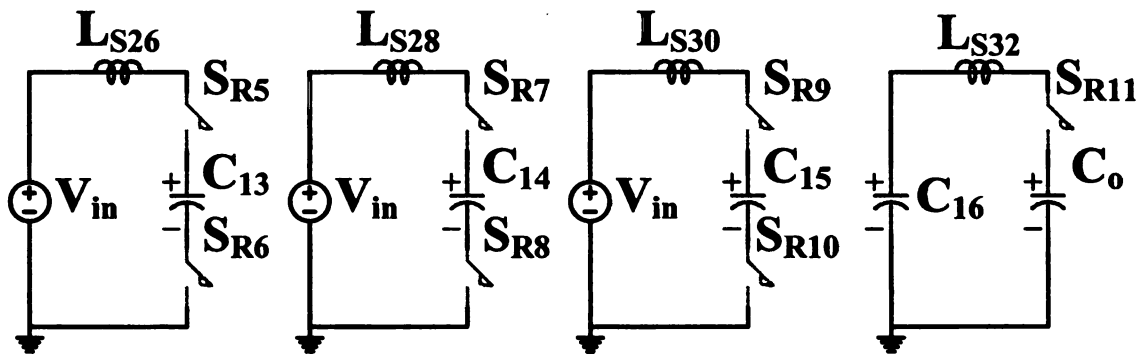


Figure 4.45 Simplified equivalent circuits of state IV (c)



Figure 4.46 Simplified equivalent circuits of state IV (d)

4.4 Analysis of Input Current Ripple Reduction

4.4.1 ZCS-MMSCC type

Assume both converters are 500 W with 5 V input voltage, and all the components are ideal

4.4.1.1 Traditional ZCS-MMSCC input current ripple calculation

Assume $I_{in} = A_1 \sin \theta, \theta \in [0, \pi]$, Because $I_{in_ave} = 100A$ So,

$\frac{1}{\pi} \int_0^{\pi} A_1 \sin \theta d\theta = 100$. $A_1 = 50\pi \approx 157$, the input current ripple I_{in_1} is

$I_{in_1} = A_1 = 157A$. The RMS value of the input current ripple

$$I_{in_1_RMS} = \sqrt{\frac{1}{\pi} \int_0^{\pi} (50\pi \sin \theta - 100)^2 d\theta} , I_{in_1_RMS} = 48.3A .$$

So, the loss of the input capacitor is $Loss1 = I_{in_1_RMS}^2 \cdot ESR$

4.4.1.2 Improved ZCS-MMSCC input current ripple calculation

Assume $I_{in} = B_1 \sin \theta, \theta \in [\pi/4, 3\pi/4]$, Because $I_{in_ave} = 100A$ So

$\frac{2}{\pi} \int_{\pi/4}^{3\pi/4} B_1 \sin \theta d\theta = 100$, $B_1 = 50\pi / \sqrt{2} \approx 111$, the input current ripple I_{in_2} is

$I_{in_2} = B_1(\sin\frac{\pi}{2} - \sin\frac{\pi}{4}) = \frac{50\pi}{\sqrt{2}}(1 - \frac{\sqrt{2}}{2}) \approx 32.5A$. The RMS value of the input current

ripple is $I_{in_2_RMS} = \sqrt{\frac{2}{\pi} \int_{\pi/4}^{3\pi/4} (\frac{50\pi}{\sqrt{2}} \sin\theta - 100)^2 d\theta}$, $I_{in_2_RMS} = 9.7A$ which is about 20% of $I_{in_1_RMS}$.

So, the loss of the input capacitor is $Loss2 = I_{in_2_RMS}^2 \cdot ESR$. So the reduced power loss ratio is $P_{reduce_ratio} = Loss2/Loss1 = I_{in_2_RMS}^2 / I_{in_1_RMS}^2 = 4\%$

Hence, by using Four-phase interleaved strategy of improved ZCS-MMSCC, the input current ripple RMS value is reduced by 80%, and Input capacitor ESR loss is reduced by 96% which is a huge reduction. Much smaller capacitor bank could be adopted; the converter efficiency and power density is improved significantly.

4.4.2 ZCS voltage multiplier type

4.4.2.1 Traditional ZCS voltage multiplier input current ripple calculation

Assume $I_{in} = 3A_2 \sin\theta + A_2 \sin\alpha$, ($\theta \in [0, \pi], \alpha \in [\pi, 2\pi]$), Because $I_{in_ave} = 100A$

So, $\frac{1}{\pi} \int_0^{\pi} 3A_2 \sin\theta d\theta + \frac{1}{\pi} \int_{\pi}^{2\pi} A_2 \sin\theta d\theta = 100$. $A_2 = 25\pi \approx 78.5$, the input current ripple is $I_{in_3} = 3A_2 = 235.5A$. The RMS value of the input current ripple is

$$I_{in_3_RMS} = \sqrt{(\frac{1}{\pi} \int_0^{\pi} (75\pi \sin\theta - 100)^2 d\theta + \frac{1}{\pi} \int_{\pi}^{2\pi} (-25\pi \sin\theta - 100)^2 d\theta) / 2}$$

$$I_{in_3_RMS} = 73.63A.$$

So, the loss of the input capacitor is $Loss3 = I_{in_3_RMS}^2 \cdot ESR$

4.4.2.2 Improved ZCS voltage multiplier input current ripple calculation

Assume $I_{in} = B_2 \sin \theta, \theta \in [\pi/4, 3\pi/4]$, Because $I_{in_ave} = 100A$ So,

$\frac{2}{\pi} \int_{\pi/4}^{3\pi/4} B_2 \sin \theta d\theta = 100$. $B_2 = 50\pi / \sqrt{2}$, the input current ripple is about 32.5 A. The

RMS value of the input current ripple is $I_{in_4_RMS} = \sqrt{\frac{2}{\pi} \int_{\pi/4}^{3\pi/4} (\frac{50\pi}{\sqrt{2}} \sin \theta - 100)^2 d\theta}$,

$I_{in_4_RMS} = 9.7A$ which is about 13% of $I_{in_3_RMS}$. So, the loss of the input capacitor

is $Loss4 = I_{in_4_RMS}^2 \cdot ESR$. So the reduced power loss ratio is

$$P_{reduce_ratio} = Loss2/Loss1 = I_{in_4_RMS}^2 / I_{in_3_RMS}^2 = 1.7\%.$$

Hence, by using four phases interleaved strategy of improved ZCS voltage multiplier, the input current ripple RMS value is reduced by 87%, and Input capacitor ESR loss is reduced by 98.3% which is a huge reduction. Much smaller capacitor bank could be adopted; the converter efficiency and power density is improved significantly.

4.5 Simulation and Experiment Results

4.5.1 Improved ZCS-MMSCC with continuous input current

Figure 4.47 shows the simulation results of a 500 W 5 V input 20 V output improved ZCS-MMSCC with continuous input current waveforms. All the capacitors ($C_1 \sim C_{16}$) are 47 μF . Output capacitor C_o is 672 μF . $L_{S1}, L_{S5}, L_{S6}, L_{S10}, L_{S11}, L_{S15}, L_{S16}, L_{S20}$ are 108 nH, $L_{S2} \sim L_{S4}, L_{S7} \sim L_{S9}, L_{S12} \sim L_{S14}, L_{S17} \sim L_{S19}$ are 216 nH. Switching frequency is 70.4 kHz. The input current maximum value is about 110 A, the

input current minimum value is about 77.8 A, so ripple current is 32.2 A, which is about one fifth of the value of the non-interleaved version as calculated. The RMS value of the ripple current is about 9.7 A which is also about 20% of the traditional ZCS-MMSCC. Figure 4.48 and Figure 4.49 shows the experiment waveforms of a 500 W improved ZCS-MMSCC with continuous input current prototype with the same parameter of simulation.

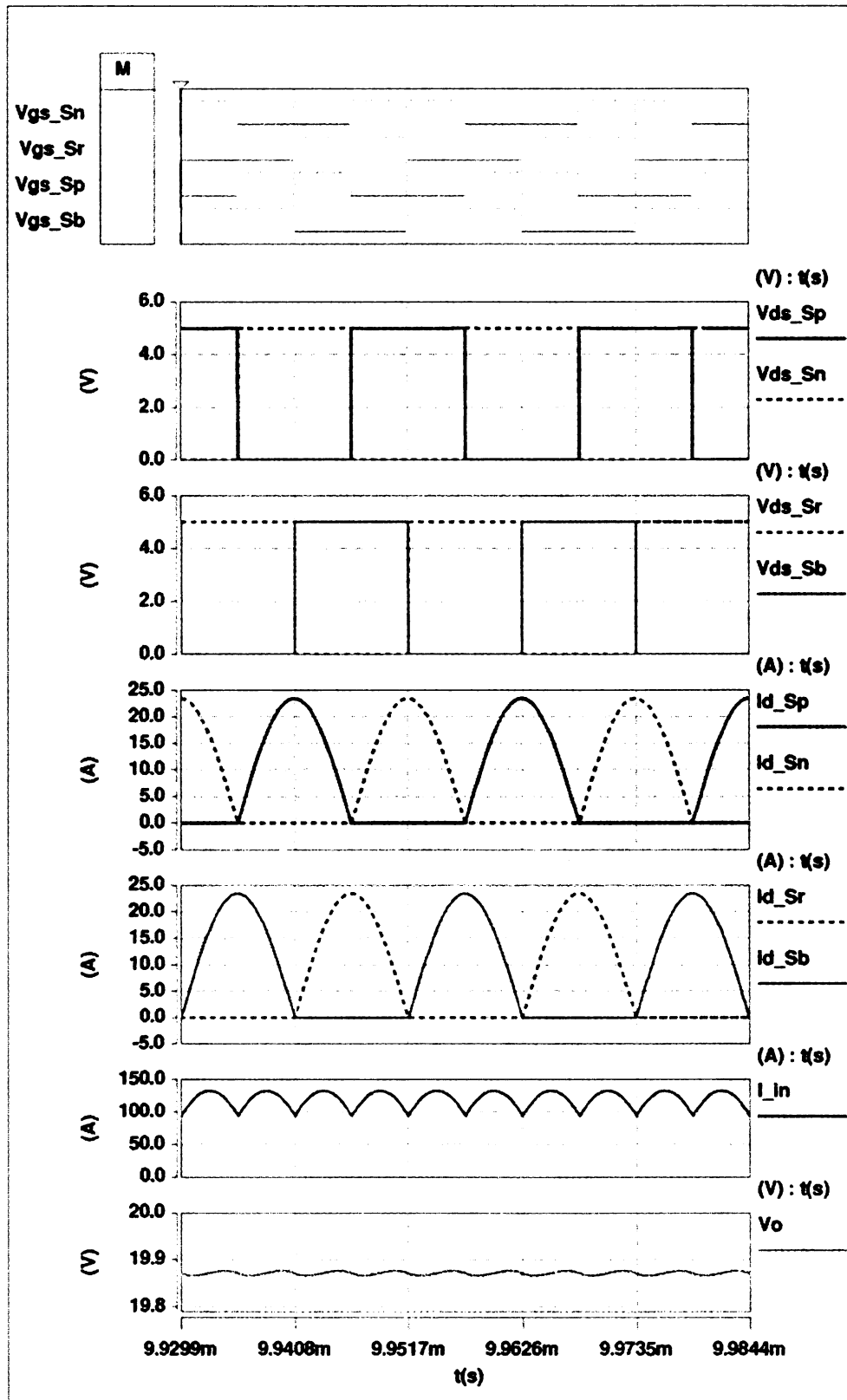


Figure 4.47 Simulation results of ZCS-MMSCC with continuous input current.

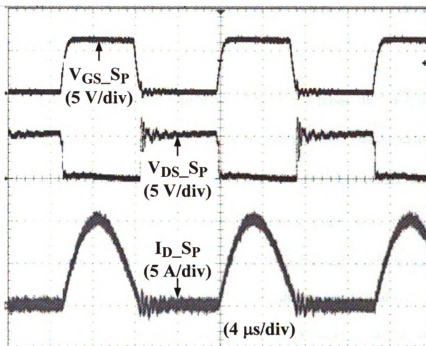


Figure 4.48 Switch voltage and current waveform.

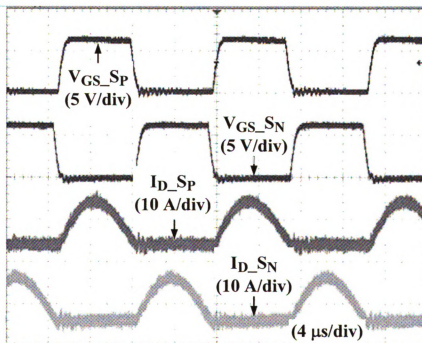


Figure 4.49 two switches control signals and current waveforms.

4.5.2 Improved ZCS voltage multiplier with continuous input current

Figure 4.50 shows the simulation results of a 500 W 5 V input 20 V output improved ZCS voltage multiplier with continuous input current waveforms. All the capacitors (C_1 - C_{16}) are 47 μF . Output capacitor C_o is 672 μF . All the stray inductance value are 108 nH (L_{S1} - L_{S32}), Switching frequency is 70.4 kHz. The average input current is 100 A. The input current maximum value is about 110 A, the input current minimum value is about 77.8 A, so ripple current is 32.2 A, which is about one seventh of the value of the traditional ZCS voltage multiplier as calculated. The RMS value of the ripple current is about 9.7 A. which is also about 13% of the traditional ZCS voltage multiplier.

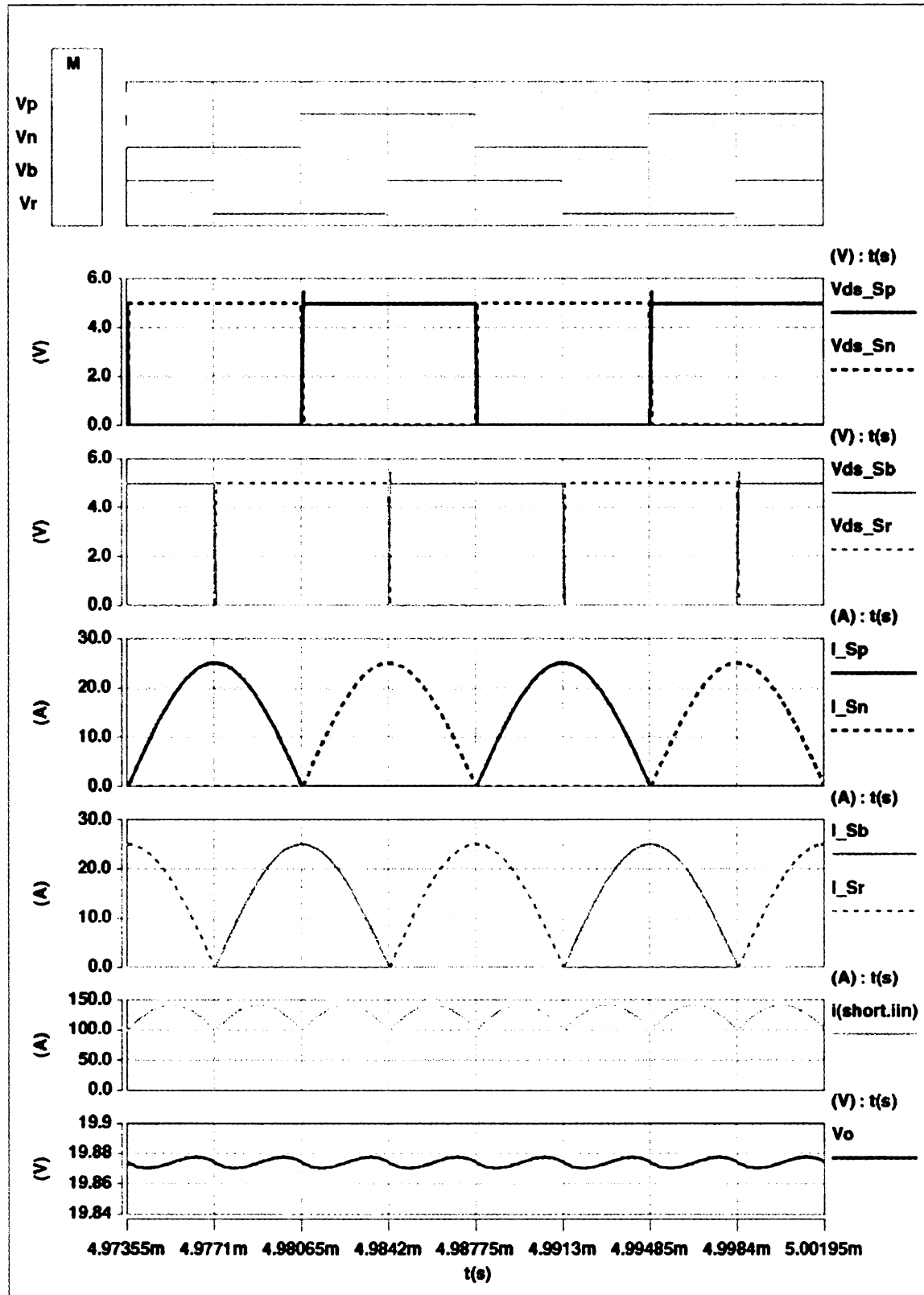


Figure 4.50 Simulation results of ZCS voltage multiplier with continuous input current.

4.6 Conclusion

In this chapter, a series of improved switched-capacitor dc-dc converter has been proposed. An extra switch and a relatively big output capacitor are added into the traditional ZCS switched-capacitor dc-dc converter to decouple the input voltage source and the output. The output capacitor will not join the resonant anymore, and output voltage ripple is reduced significantly. By interleaving four phases of improved switched-capacitor dc-dc converters together, input current becomes continuous. The input current ripple is reduced more than five times accordingly. The huge power loss related to the input capacitor is minimized. The operation, analysis and features are illustrated. Simulation and experiment result for a 500 W 5 V input, 70 kHz improved ZCS-MMSCC with continuous input current prototype were shown to verify the operation principal. As a result, the proposed improved ZCS switched-capacitor dc-dc converter with continuous input current has smaller size, higher efficiency and higher power density. So they are more suitable to the high power, high current automotive application.

CHAPTER 5

Conclusion and Future works

5.1 Contributions

This work has the following contributions:

- Electrical characteristics of TEG modules in steady state and high frequency are proposed and modeled. The problems related to dc-dc converter design of TEG modules in automotive application are addressed. The problems of traditional step-up dc-dc converters and switched-capacitor dc-dc converters are summarized.
- A quasi-resonant soft switching strategy of utilizing the distributed stray inductance in the circuit for the switched-capacitor dc-dc converter is proposed. By using the proposed soft switching strategy, the high voltage and current spike of traditional switched-capacitor dc-dc converter are reduced. The huge di/dt and dv/dt in the switching transition and EMI noise are restricted. The huge capacitor bank to reduce the voltage ripple and achieve high efficiency is eliminated.
- A ZCS multi-level modular switched-capacitor dc-dc converter as the high input current, high voltage gain interface circuit for TEG in automotive application is proposed. This new converter includes the advantages of both zero current switching and multi-level modular switched-capacitor dc-dc converter. Also this new converter does not employ extra devices to achieve ZCS which increase the circuit reliability.
- A family of ZCS switched-capacitor dc-dc converter for the automotive application is proposed and analyzed. By using the proposed ZCS switched-capacitor dc-dc

converter, very high power density dc-dc converter operating at high temperature could be made.

- A family of improved ZCS switched-capacitor dc-dc converter with interleaving capability is proposed in order to reduce the input capacitor current stress by reducing the input current ripple using interleaving strategy. By interleaving the improved ZCS switched-capacitor dc-dc converter, a family of ZCS switched-capacitor with continuous input current is achieved. Much higher power density with higher input current rating switched-capacitor dc-dc converters could be made.

5.2 Recommendations for Future Works

- More detailed theoretical analysis could be done to compare the traditional switched-capacitor dc-dc converter and the ZCS version in terms of size, efficiency and etc. The optimal design point of switched-capacitor dc-dc converter could be addressed in terms of capacitance, stray inductance and switching frequency.
- The ZCS switched-capacitor with voltage regulating capability could be investigated. The stray inductance for the voltage regulation could be considered.
- Other improvements of switched-capacitor dc-dc converter could be proposed, while the device and the capacitor have the voltage stress, current stress for more generalized high power operation.
- The integrated version of switched-capacitor dc-dc converter working at higher switching frequency around (200 kHz~500 kHz) with ZCS by utilizing the stray inductance could also be investigated.

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