HIGH POWER INDUCTIVE WIRELESS CHARGER FOR PHEV AND EV

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ABSTRACT

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Electric vehicles (EVs) are getting more attractive for the sake of reducing air pollutions in urban areas. Wireless power transfer (WPT), a key enabling technology, affects the acceptance of EVs in the market. For high power WPT, inductive power transfer (IPT) has been researched for decades and successfully used in several EV systems. However, higher efficiency and higher power density IPT systems are still in demand.

The unique feature of this IPT system is that the coupling coefficient of the primary side and secondary side windings is usually less than 0.1. Compensation networks are needed on both primary and secondary side to cancel the huge leakage inductances. Series resonant converter (SRC), with simply compensation networks, is widely adopted as a high efficiency topology for IPT system. Owing to the small coupling coefficient, the SRC acts like a band-pass filter, which only allows the resonant frequency component passing to the secondary side. The band-pass filter can be designed to match one harmonic frequency and only that frequency component carries the power. The passive components can shrink a lot if the resonant frequency is far higher than the switching frequency, and this leads to a more compact IPT system. A harmonic oriented IPT system is proposed. The design considerations of the proposed system and the comparison of different harmonic systems are presented in Chapter 2.

Load regulation function is required for battery chargers. However, for the SRC, Small drift away from resonant frequency leads to huge drop on gain and huge increment on circulating current. Traditional frequency modulation control loses soft switching when doing load regulation,

which is the main advantage of a resonant converter. A harmonic burst control is proposed to achieve soft switching at both turn-ons and turn-offs under all load conditions. It improves the system efficiency over 10% for light-load conditions. Chapter 3 illustrates this harmonic burst control in detail.

IPT systems also includes a power factor correction (PFC) front end, which is usually a boost PFC converter, and an isolated DC-DC converter. In order to reduce the cost of two stage solution, a Z-source resonant converter is researched as a single stage solution that can perform PFC and load regulation at the same time. The mechanism of this Z-source resonant converter is presented in Chapter 4. And the high power factor control schemes are proposed for this Z-source resonant converter in Chapter 5.

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CHAPTER 1 Introduction

Research on WPT for EVs battery charger is actively carrying on, for the sake of its advantages of convenience, reliability and environmental adaptation [1]. For a stationary application, WPT charger system allows the driver simply to park and charge without getting out of the vehicle. Inductive power transfer is the mainstream technology for static charging as the power rating can be scaled up easily with more core material and bigger converter. Capacitive power transfer (CPT) relying on electric field instead of magnetic field shows better misalignment performance and less sensitive to metal object in the air gap [2]. Owning to the appearance of high speed power switches such as GaN device, a few high-power CPT systems have been reported in [3, 4] recently. However, transferring high power in MHz range brings new problems to the system such as safety voltage for human and electromagnetic interference (EMI) [5].

Further, a dynamic WPT charger system also called on-line inductive power transfer (OLPT), can charge the running EVs with embedded transmit coils under a road (Figure 1. 1). A proper energy storage and charging system design could reduce 20% battery capacity of the EVs [6], minimizing the weight and cost. Therefore, this thesis focuses on high power inductive wireless charger for PHEV and EV.

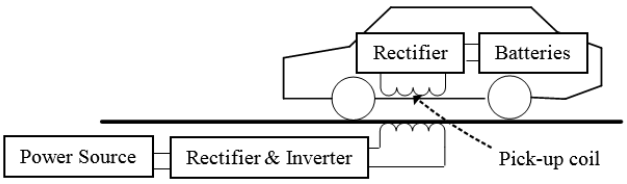


Figure 1. 1 Configuration of a wireless power transfer system for OLPT

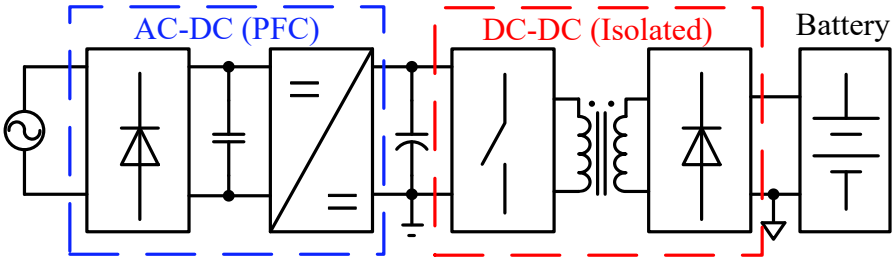


Figure 1. 2 Block diagram of a conventional OBC

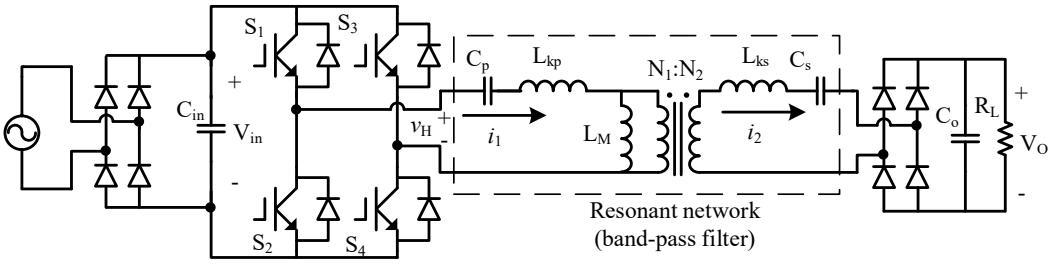


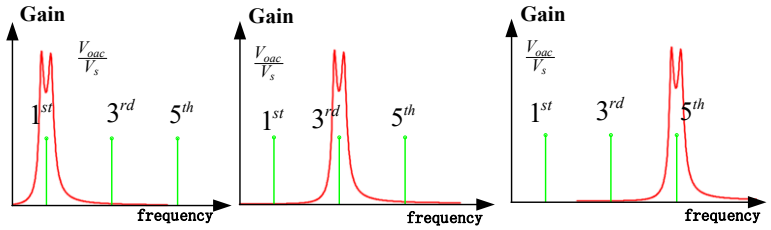
Figure 1. 3 Overall schematic diagram for the conventional IPT prototype

Conventional on-board battery charger (OBC) is usually a two-stage structure; a PFC front end part and a DC-DC converter part with high-frequency transformer as Figure 1. 2 shows. In WPT application, the SRC (Figure 1. 3) is widely adopted as the DC-DC converter because of its simplicity and high efficiency [7], and the primary side and secondary side windings are designed with a relatively large size to increase the coupling coefficient. The ultimate goal for next generation wireless charger is high power density, high efficiency and low cost. The thesis is organized through these three approaches.

1.1 High power density wireless charger

The core structure of the coupling windings is one key factor to reduce the overall size. After several generations of core structure design, KAIST proposed a narrow width I-type structure which reduces the primary side size significantly [8]. Another example of weight reduction is using evenly distributed bars instead of a round pie, which can reduce the total weight of the cores [9]. However, the overall volume remains nearly the same. In [10], a third coil is used to pick up the horizontal flux and enhance the coupling coefficient. Paper [11] evaluates the core size and

coefficient when the window area is fully occupied. But the improvement is merely incremental. Core structure design is continuously being researched to achieve a more compact system [12-17].



(a) 1st-SRC (b) 3rd-SRC (c) 5th-SRC

Figure 1. 4 Output to input voltage gain curves vs. frequency

It is generally acknowledged that raising the switching frequency can reduce the volume of passive components. For EV battery chargers, the power level is usually up to several kilo watts and they are more likely to use IGBT instead of MOSFET for the inverter. High current IGBT usually can only run up to around 20 kHz [18, 19], which limits the system frequency of IPT. Thus, low frequency switches limit the size of the ferrite core and the copper winding. However, a typical characteristic of IPT is a band-pass filter gain curve from output to input [20] as shown in Figure 1. 4(a). This special feature only allows the resonant current flowing to the secondary side with other frequency components greatly attenuated. Since the output voltage of H-bridge is a quasi-square waveform with rich harmonics, the system can be designed for one of the harmonics only Figure 1. 4(b)&(c) show. Therefore, the system frequency increases to three times, five times, or even higher with the harmonic current as the power carrier, while the switching frequency maintains the same. As a result, the resonant components in SRC could be reduced to 1/3, 1/5, or even smaller. IPT system designed for third harmonic (3rd-SRC) has been illustrated in [21, 22]. It is reported in [21] that a 3rd-SRC reaches over 90% efficiency, and shows competitive merits with respect to volume, weight, and efficiency over the conventional fundamental system (1st-SRC). However, with higher order harmonics, the DC bus voltage utilization is low and the

switches suffer from large current stress even though the Ampere-turns for the primary side winding is the same. There is a trade-off between size and efficiency.

1.2 High efficiency wireless charger

Load regulation function is required for the DC-DC converter as the battery charger has constant current (CC) mode and constant voltage (CV) mode as shown in Figure 1. 5. In order to shorten the charging time, the 3.3-kW WPT system is no longer satisfied and people are interested in higher power (6.6 kW or more) WPT OBC systems [7]. Hence, the DC-DC converter would always try to output maximum current in CC mode without regulation. However, it should be noted that the low-medium load range in CV mode consumes 40% of the total charge time [8]. In other words, load regulation in CV mode is essential in terms of the overall performance of the OBC.

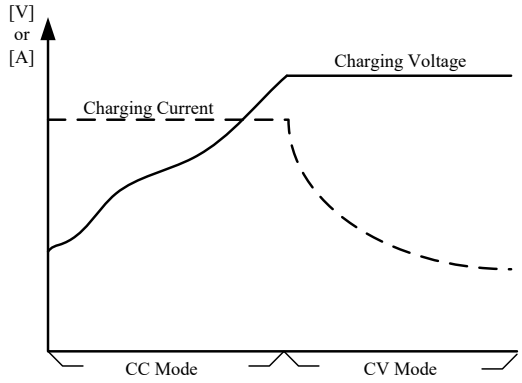


Figure 1. 5 On-board battery charger (OBC) charging mode

The SRC, like other resonant converters, can realize load regulation by frequency modulation method (PFM). However, owing to the large ratio between the leakage inductance and magnetizing inductance (greater than 10:1) in WPT application, SRC has a high quality-factor. Small drift away from resonant frequency leads to huge drop on gain and huge increment on circulating current [18]. In [19, 20] from Oak Ridge National Laboratory (ORNL), SRC is investigated and verified that the peak power range is broader for a given frequency band and then

drops quickly outside the band. In their later work [21], they change to series-parallel configuration that has a wider plateau in the power versus frequency curve, which gives them more freedom on PFM control.

In [23], the topology is changed according to the charging mode. However, this hybrid solution needs redundant bulky resonant components. In their later work [24], another hybrid topology with good misalignment performance is proposed. But the component count is still high and extra AC switches are needed.

In [25, 26], phase-shift and amplitude control on the secondary side was implemented for better impedance match. Light load efficiency is improved, but extra circuit is needed on the secondary side. A self-tuning method was proposed in [27], where the resonant frequency could be tracked automatically. This method is suitable for component variation compensation, but not for load regulation as the resonant frequency is usually independent of the load.

A traditional burst control was proposed in [22, 28] over 20 years ago. Several variations are presented in [28], however, the conventional bang-bang control is used as a benchmark in this paper. Its basic idea is to control the time duration of power transferring from source to output side. The H-bridge produces a resonant frequency square waveform to excite the resonant network for a period T_1 and then outputs zero voltage to cut off the power source for a period T_2. The ratio of T_1 and T_2 is used to regulate the output power. Hence, the converter always operates at resonant frequency and achieves soft switching at any time instant. However, the traditional burst control causes large pulsed power on both input filter and output filter. Therefore, traditional burst control is usually adopted at light loads only.

A harmonic burst control strategy which regulates the output power via different harmonics according to the load is proposed. The proposed method achieves soft switching at both turn-ons and turn-offs for a wide range of loads. This burst control improves the EV battery charger's efficiency by over 10% during light loads without any additional hardware. Additionally, compared to the traditional burst control, it has much smaller pulsed power over a wide range load. A 1-kW prototype with 20-cm air gap between the primary and secondary side of the converter has been built to verify the proposed method.

Recently, some control strategies which share similar concept as harmonic burst control are found in [29, 30].

1.3 Low cost wireless charger

In some designs, the resonant converter is left unregulated and freewheeling with different air gap or load [31-33]. Thus, one more front-end stage is needed to regulate the DC bus voltage [34], and this front-end stage usually also performs power factor correction [35-37]. In [38], a 7-kW charger system is divided into three stages—a front end PFC converter, a buck converter for voltage regulation, and a SRC, such that the SRC can always operate at resonant frequency with high efficiency.

Two or more stage solutions are high cost and complicated, even though the design for each stage is simple. The overall performance may not be the best. Z-source inverter [39], well known for its boost feature and being immune to shoot-through problem, can be applied to any kind of power conversion between DC and AC. A combination of Z-source network (ZSN) and SRC has been studied in [40]. It can improve the efficiency over a wide input voltage and load

variation. Furthermore, Z-source resonant converter was proposed in [41] and proved its advantage over conventional boost PFC with a cascaded DC-DC. Figure 1. 6 shows the overall schematic for ZSRC. The input diode is a SiC device with almost zero reverse recovery loss, which is suitable for high frequency switching application. A Z-source network is placed between the input diode and the H-bridge inverter of the conventional SRC system. The SRC converts the DC power to high frequency AC power and pass it to the secondary side. This is a single stage solution that saves the cost and complicity.

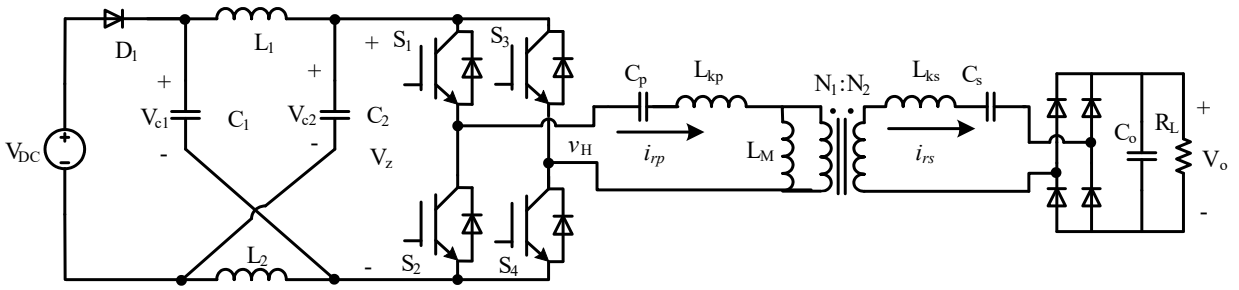


Figure 1. 6 Circuit schematic of the ZSRC

Sinusoidal charging, which had already been brought out in the early 1990s [42], allows the low frequency ripple to propagate to the battery and does not require energy storage component for the low frequency ripple. Research done on lead-acid battery [43] shows that there is no significant influence on battery temperature and capacity by utilizing sinusoidal charging. Recently, a comparison of low frequency (120 Hz) sinusoidal charging and DC charging shows negligible impact on the performance of Li-ion batteries [44-46], which is the mainstream energy storage component for EV [47,48]. Therefore, sinusoidal charging is a promising technique for EV battery charger. In OBC application, sinusoidal charging can be easily realized by changing the algorithm on the PFC stage [47-53]. However, most of these solutions still maintain two-stage

structure with the only benefit of reducing the bulky bus capacitor. ZSRC, as a single stage solution, can maximize the volume and cost reduction of utilizing sinusoidal charging.

1.4 Scope of the thesis

Based on the previous works of wireless charger for EV and PHEV, this thesis focuses on the following subjects:

Chapter 2 provides a theoretical and practical design for harmonic system, and a 1-kW prototype that reaches 83% efficiency at 20-cm air gap using harmonic power has been built to verify the proposed method and comparison.

Chapter 3 discusses the harmonic burst control strategy for load regulation. The soft switching characteristic is explained. Experimental results prove the efficacy of harmonic burst control over wide load range.

Chapter 4 presents the mechanism of Z-source resonant converter. Two PWM methods for Z-source resonant converter are compared for efficiency and load regulation performance.

Chapter 5 focuses on the PFC control schemes for Z-source resonant converter, both the conventional way and the sinusoidal charging.

Chapter 6 is conclusions and future works.

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CHAPTER 2 Wireless Power Transfer Via Harmonic Current

For inductive WPT, the coupling between the two windings is relatively weak. Therefore, resonant topologies are usually used for WPT applications to boost the output gain. The output from the H-bridge inverter is a quasi-square voltage waveform, which contains rich harmonics. Traditional resonant converters deliver power through fundamental frequency component. The switching frequency of the switch defines the upper limit of the resonant frequency. The volume of the passive components in the resonant tank is directly related to the resonant frequency. Higher resonant frequency results in smaller passive components. In large power rating (several kilo watt) applications, IGBT is usually used and the maximum switching frequency is around 20 kHz. To shrink the size of the passive components, harmonic component can be utilized for power transferring. For example, the resonant converter can be designed for third harmonic (around 60 kHz) while using IGBT. The design consideration and comparison of wireless charger via harmonic current will be presented in this chapter.

2.1 Basic operation principle of IPT

The resonant network in the SRC exhibits a unique band-pass filter characteristic, which makes this harmonic system concept feasible. Regardless of the frequency components lower or higher than resonant frequency, the passive components in the resonant network only need to take care of one frequency (resonant frequency) component. Hence, these passive components could be easily analyzed and optimized with simple equations.

2.1.1 Band-pass filter characteristic of SRC

A simplified circuit is shown in Figure 2. 1. The H-bridge inverter is modeled as a voltage source v_H, and the equivalent AC resistance R_{ac} of the load (which is seen from the input side of the output rectifier) is given in

$$R_{ac} = \frac{8}{\pi^2} R_L . \tag{2-1}$$

N equals N_2/N_1, and R_p and R_s are the AC resistances of the primary and secondary side windings, respectively. Secondary side components in Figure 2. 1 are all reflected to the primary side.

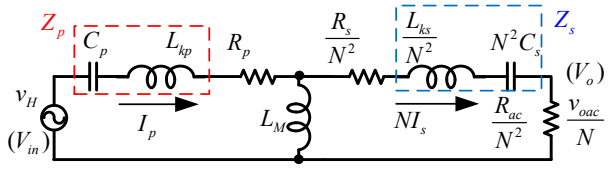


Figure 2. 1 Equivalent simplified circuit for IPT

For simplicity, we assume N=1 and R_p=R_s=0. Because of loose coupling of the windings, L_{kp} and L_{ks} are at least ten times larger than L_M. C_p and C_s are the compensation capacitors, which determine the resonant frequency by compensating the leakage inductance. For example, as shown in Figure 2. 1, the impedances in the dash box (Z_p & Z_s) are zero at resonant frequency. Thus, changing C_p and C_s is actually changing resonant frequency. A resonant frequency at 50 kHz, with L_M=5 uH, is chosen for the demonstration in Table 2. 1.

Table 2. 1 Band-pass filter parameter

L_{kp}=L_{ks}=10L_M=50 uH	C_p=C_s=200 nF
ω=2πf_{re}=2π50 kHz	R_{ac}=0.1ωL_M, ωL_M or 10ωL_M

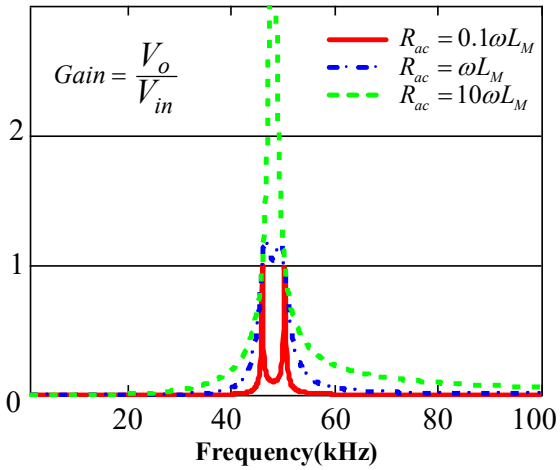


Figure 2. 2 Gain curve of IPT with different load (R_{ac}=0.1ωL_M, ωL_M and 10ωL_M)

Once the coupled windings have been designed, the mutual inductance does not change with a fixed air-gap distance and a fix alignment. But the effective leakage inductance (Z_p & Z_s) changes according to the compensation method. Therefore, it is reasonable to use the mutual impedance L_M as a base value for the AC resistance. Figure 2. 2 shows the frequency characteristic of the voltage gain with different AC resistance. It is worth pointing out that the gain curve has a bifurcation phenomenon as the load increases. Two extra resonant frequencies (the two peaks) emerge. No matter how the AC resistance varies, the gain curves act like a band-pass filter with a very narrow window.

2.1.2 Harmonic Power from H-bridge Inverter

Each phase leg of the H-bridge is operating with 50% complementary duty cycle, and the phase shift between the two legs actually controls the output voltage v_H. A graphical interpretation is shown in Figure 2. 3. When the gate signal S_1 and S_4 are on, v_H equals input voltage V_{in}. On the other hand, when S_2 and S_3 are on, v_H equals negative V_{in}. These two states are called active states as there is energy exchange between the DC source and the resonant network. The rest of the states are labeled as zero states with either both upper switches on or both bottom switches on. The

energy is circulating inside the resonant network while the load is continuously consuming power at zero states. The H-bridge's output voltage (v_H) is a quasi-square waveform and is rich in harmonics. Its Fourier series expansion is expressed as

$$v_H = \sum_{n=1}^{\infty} \frac{4V_{in}}{n\pi} \sin(n\pi D)\sin(nt)\,, \tag{2-2}$$

and its 1st, 3rd, and 5th harmonic components' waveforms are shown in Figure 2. 3. They all have a maximum amplitude that equals to $4V_{in}/n\pi$, when the term $\sin(n\pi D)$ equals 1. Thus, the nth harmonic only utilizes 1/n of the DC bus voltage. Due to the sharp peak characteristic (band-pass filter feature) of the resonant network, only the resonant frequency component of i_1 can pass to the secondary side of the converter, with all other frequency components filtered out by large impedance. Therefore, if the resonant frequency is equal to the fundamental frequency of v_H, the power transferred to the secondary side of the SRC is carried by the fundamental frequency. Furthermore, if the resonant frequency is exactly three times the switching frequency, the 3rd harmonic is selected; or, if the resonant frequency is five times the switching frequency, the 5th harmonic is chosen, and so on. An example of 3rd harmonic is shown in Figure 2. 4. Only the selected harmonic is picked up at the output side. The passive components in the resonant network are mainly processing the 3rd harmonic component which can shrink the size and weight.

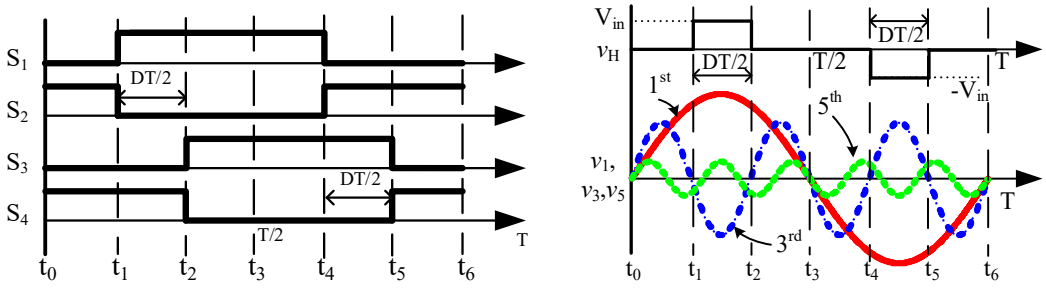


Figure 2. 3. PWM waveforms, H-bridge output voltage v_H, and H-bridge output voltage harmonics

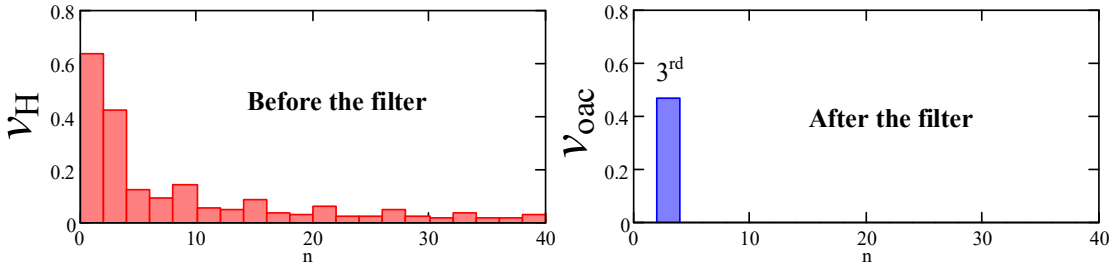


Figure 2. 4 Harmonic component of v_H&v_{oac} (D=0.33, filter $R_{ac}=\omega L_M$ in Figure 2. 2, 3rd harmonic selected as an example)

2.2 Design consideration of harmonic system

The hardware design focuses on the normal operation at full rating without misalignment on the windings. This design procedure is universal for all harmonic systems.

2.2.1 Transformer design

As shown in later discussion, the leakage inductance can be compensated by capacitor, but the mutual inductance is always fixed once the core size and shape are chosen. Therefore, the first parameter to begin with is the mutual inductance. There are many ongoing researches about the core structure design [1, 2]. KAIST has developed several generations of different core structure for IPT [3]. In [4], they proposed an I-type core structure which has less construction time and good alignment performance. Here, we follow this I-type core structure as our starting point. A normal air gap distance for EV application is around 20 cm [5]. A finite element analysis (FEA) model is built by Ansoft Maxwell software and shown in Figure 2. 5. In this single turn model, both the single-turn self-inductances and single-turn mutual inductance can be achieved by simulation and labeled as L_{p0}, L_{s0} and M_0.

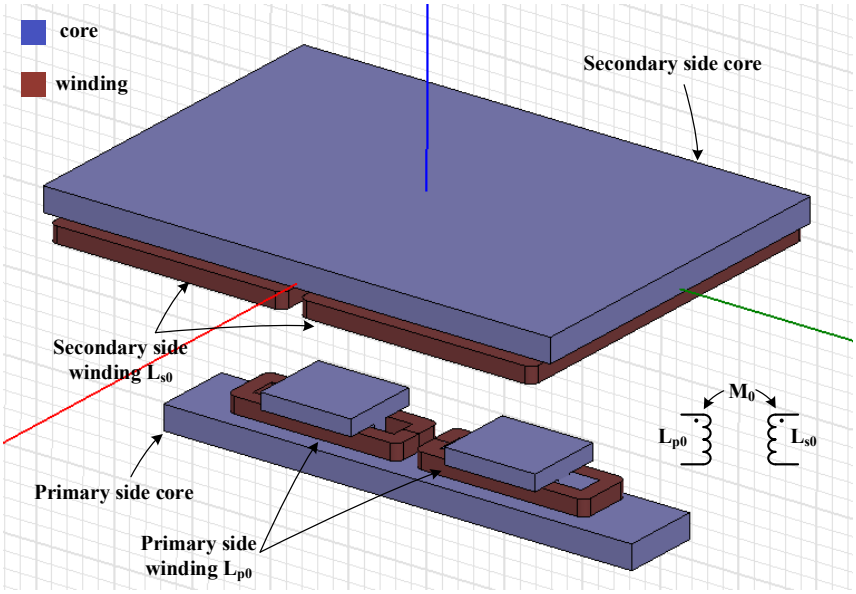
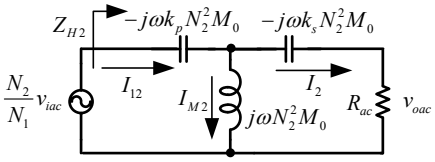
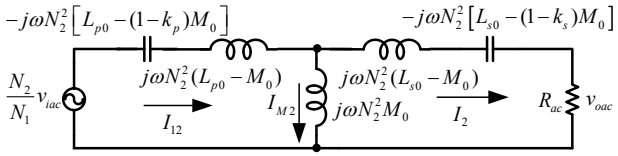


Figure 2. 5 FEA model for transformer



(a) Resonant LCs are replaced by short circuit



(b) Original circuit

Figure 2. 6 Equivalent circuit at resonant frequency seen from secondary side (without winding resistances)

At the first stage of the design, it is reasonable to neglect winding resistances for approximately optimum point estimation. The winding resistance will have an important role in the final optimization process, but it does not change the principle of choosing N_1 and N_2. Figure 2. 6(a) shows a simplified circuit for SRC from the secondary side view. The impedances of the compensation capacitors are expressed in the form of an inductor at resonant frequency. The parameter k_p and k_s indicate compensation depth of M_0. We have

$$C_p = \frac{1}{4\pi^2 f_{re}^{\ 2} N_1^2 (L_{p0} + k_p \cdot M_0)} \tag{2-3}$$

and

$$C_s = \frac{1}{4\pi^2 f_{re}^{\ 2} N_2^2 (L_{s0} + k_s \cdot M_0)} . \tag{2-4}$$

For example, if k_s equals 1, it is full compensation on the secondary side. Although it is reported in [4] that full compensation has advantage over partial compensation, we present a different approach using an extended quality factor (Q). This extended quality factor is defined as

$$Q(f) = 2\pi f \times \frac{Maximum\ energy\ stored}{Power\ dissipation} . \tag{2-5}$$

The power dissipation includes resistive power loss and output power. This definition is different from the conventional definition of Q only considers power loss. High Q indicates large amount of energy circulating inside the circuit, thus high loss and high stress are observed. In order to get Q, we expressed I_{12} and I_{M2} in terms of I_2 (reference phasor), and we have

$$I_{M2} = -k_s I_2 - j \cdot (R_{ac} I_2 / \omega N_2^2 M_0)$$

and

$$I_{12} = (1 - k_s) I_2 - j \cdot (R_{ac} I_2 / \omega N_2^2 M_0) . \tag{2-6}$$

From Figure 2. 6(b), we can calculate the Q as

$$Q(\omega_0, R_{ac}, k_p, k_s, N_2) = \omega_0 \times \frac{EC_p + EL_{kp} + EL_M + EL_{ks} + EC_s}{I_2^{\ 2} \cdot R_{ac}}$$

$$= \frac{\omega_0 \cdot N_2^2}{R_{ac}} \left\{ L_{p0}(1 - k_s)^2 + M_0 \left[(k_p - 1)(1 - k_s)^2 + (k_s - 1) \right] + L_{p0} \left(\frac{R_{ac}}{\omega_0 N_2^2 M_0} \right)^2 + L_{s0} \right\} . \tag{2-7}$$

In WPT applications, L_{p0} is much larger than M_0. Therefore, only considering variable k_s in (2-7), the variation of Q is dominated by the first term in the numerator. When k_s equals 1, which is fully compensated, it gives the minimum Q approximately. Further, the impedance of the entire resonant network (Z_{H2} in Figure 2. 6(a)) should be resistive to achieve soft switching at full load. By forcing the imaginary part of Z_{H2} to be zero, we have

$$k_p = 1 - \frac{(1-k_s)\cdot\left(\omega_0 N_2^2 M_0\right)^2}{R_{ac}^2 + (1-k_s)^2\cdot\left(\omega_0 N_2^2 M_0\right)^2}. \tag{2-8}$$

It is clear that k_p would be 1 if k_s is 1, and the circuit is simple and symmetric. Hence, Q can be reduced to

$$Q(N_2) = \frac{\omega_0}{R_{ac}}\cdot\left[L_{p0}\left(\frac{R_{ac}}{\omega_0 M_0}\right)^2\frac{1}{N_2^2} + L_{s0}N_2^2\right]. \tag{2-9}$$

Since N_2 is the only variable in (2-9), Q achieves minimum value when the two terms equal each other, and one has

$$N_2 = \left(\frac{L_{p0}}{L_{s0}}\right)^{0.25}\cdot\sqrt{\frac{R_{ac}}{\omega_0 M_0}}. \tag{2-10}$$

Secondary side turns N_2 is determined without the information of primary side control scheme or the order of harmonic carrier; therefore, N_2 is the third parameter in this procedure. The next step is to choose N_1 based on the output power rating and the order of harmonic carrier. The magnitude of n^{th} harmonic (v_{nth}) is expressed as

$$v_{iac} = v_{nth} = 2\sqrt{2}V_{dc}/(n\cdot\pi). \tag{2-11}$$

By applying power balance in this lossless model, we have

$$P_o = \left(v_{nth} \frac{N_2}{N_1} \right)^2 / |Z_{H2}| = \left(v_{nth} \frac{N_2}{N_1} \right)^2 / R_{H2} . \quad (2\text{-}12)$$

As mentioned before, Z_{H2} is resistive at full load. By solving (2-12), we get a value of primary side turns N_1 as

$$N_1 = \frac{v_{nth}}{\omega_0 M_0 N_2} \sqrt{\frac{R_{ac}}{P_o}} = \frac{2\sqrt{2} V_{dc}}{n\pi\omega_0 M_0 N_2} \sqrt{\frac{R_{ac}}{P_o}} . \quad (2\text{-}13)$$

After calculating the turns, we have an approximately optimum design based on the judgment of Q. In the next stage, current density of the windings will be chosen, and we will have information of R_p and R_s. All the previous calculations could be recalculated and justified with R_p and R_s. N_1 and N_2 may be adjusted to find the real optimum point. The last step is to check the window utilization factor to see if the transformer is big enough to hold all the windings. If not, change to a bigger core and redo all these steps.

An IPT system is designed with 190 V input, 200 V output and 1-kW rating power. The 1st-SRC, the 3rd-SRC and the 5th-SRC are chosen as the examples to illustrate the analysis. The same core structure is used; thus, they share the same L_{p0}, L_{s0} and M_0. The switching frequency is slightly lower than 20-kHz which is the maximum limit for the IGBT in our prototype. Following the design procedure mentioned above, Table 2. 2 shows the design results for different harmonics as the power carrier.

Table 2. 2 Calculation parameter for the resonant network in terms of different harmonic power carrier

	1st-SRC	3rd-SRC	5th-SRC
Common parameters	R_o=40 Ohm (R_{ac}= 32 Ohm)	f_{sw}=18 kHz	M_0=0.275 uH
Winding turns	N_1=25 N_2=32	N_1=5 N_2=20	N_1=3 N_2=12*
Transformer ratio	N=1.28	N=4	N=4
Winding AC resistance	R_p=0.53Ohm R_s=2.32Ohm	R_p=0.11Ohm R_s=1.45Ohm	R_p=0.06Ohm R_s=0.87Ohm
Self-inductance	L_1=1.33mH L_2=3.03mH	L_1=53uH L_2=1.18mH	L_1=19uH L_2=426uH
Mutual inductance	L_M=172uH	L_M=6.88uH	L_M=2.48uH
Leakage inductance	L_{kp}=1.15mH L_{ks}=2.74mH	L_{kp}=46uH L_{ks}=1.07mH	L_{kp}=16.6uH L_{ks}=386uH
Compensation Capacitance	C_p=590nF C_s=25.8nF	C_p=164nF C_s=7.3nF	C_p=164nF C_s=7.3nF

*The calculation result should be N_2=14, but N_1 lies between 2 and 3. Both 2 and 3 have so large error that N_2 is adjusted to 12.

2.2.2 Design verification

In this section, winding resistances are taken into consideration. More numeral results are presented to support the approximation we made in previous section. We choose the 3rd-SRC in Table 2. 2 as an example for the following analysis.

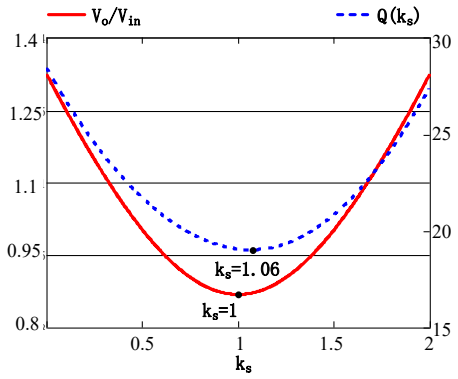


Figure 2. 7 Voltage gain and quality factor curves vs. k_s with resistive impedance (Z_{H2}) constrain and fixed turns (N_1=5, N_2=20)

Figure 2. 7 shows that the minimum point of Q happens at k_s=1.06, which justifies the approximation with k_s=1 in (2-7). Even though this minimum point settles around the minimum voltage gain, high efficiency with lower Q is more attractive and the required voltage gain can be achieved by adjusting N_1.

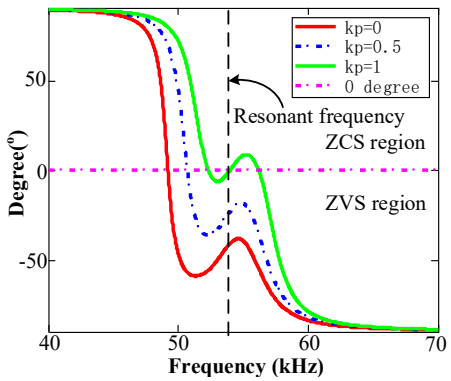


Figure 2. 8 Primary side current phase of H-bridge vs. frequency with different k_p @k_s=1

Figure 2. 8 shows k_p's impact on the primary side current phase. To achieve zero voltage switching (ZVS), the total impedance seen from the output of H-bridge should be inductive. The resonant network impedance would be more inductive with a smaller k_p. However, a k_p marginally less than 1 can also perform zero current switching (ZCS) at turn-offs. Therefore, k_p is selected to be a value close to 1.

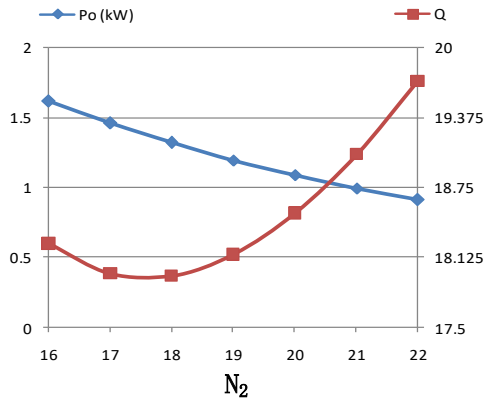


Figure 2. 9 Maximum power and quality factor curve vs. secondary turns N_2 (@Vin=190 V, N_1=5, Ro=40 Ohm)

The winding resistances and semiconductor switches affect the maximum output power in a real system. By taking these non-ideal factors into account, the maximum power and the quality factor curves are plotted in Figure 2. 9. In previous section, the approximate optimum result gives us the turns pair of N_1=5 and N_2=17. The minimum Q happens at N_2=18 which is slightly affected by the winding resistance. However, its maximum output power shifts to a value much larger than

1-kW rating output power, which does not fully utilize the DC voltage. Since N_1 is a small integer, there is not much margin left to adjust N_1. Therefore, N_2 is adjusted to 20 for 1-kW rating output power sacrificing the Q as shown in Figure 2. 9.

In summary, a full compensation on secondary side (k_s=1) helps reduce the Q and a corresponding full compensation on primary side (k_p=1) ensures soft switching at full load. The number of secondary side turns (N_2) are selected based on the structure and parameters of the core and the load. The number of primary side turns (N_1) is determined by the amplitude of harmonic carrier and output power. These design principles of a harmonic system have been verified for a system without approximation. In the next section, a comprehensive comparison is carried out among the three harmonic systems.

2.3 Comparison items, conditions and results

Regarding to the total size of an IPT system, heat (which is efficiency), insulation (which relates to window utilization factor), and energy storage components are the main concern in the total volume. These are the physical limitations that one cannot break. Therefore, several items such as efficiency, window utilization factor, and compensation capacitor volume are compared below based on theoretical calculation.

Conditions: All those three systems in Table 2. 2 share the same H-bridge inverter, output diode bridge, and current density (7 A/mm^2) on the windings. Core material is the same ferrite. The material for compensation capacitor is also the same even with different voltage ratings. The IGBTs and output diode bridge part number can be found in Table 2. 4. All IGBTs are doing soft switching at full rated power condition.

2.3.1 Harmonic systems' efficiency

The power loss in this converter mainly contains the following parts:

P_s: Switching device loss, the conduction loss of IGBT;

P_c: Compensation capacitor loss, AC loss calculated by capacitor dissipation factor tan δ;

P_d: Secondary rectifier loss, the conduction loss of diode bridge;

P_w: Copper loss of the winding; and

P_t: Core loss of the transformer.

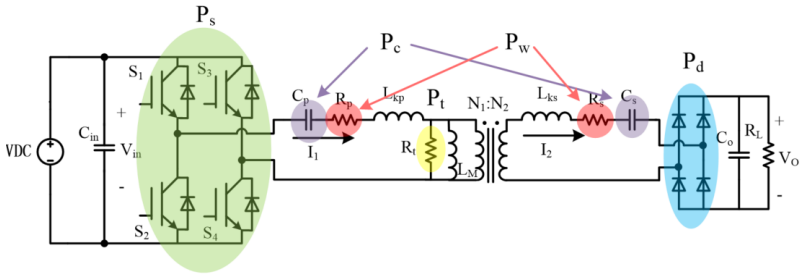


Figure 2. 10 Schematic diagram for conventional IPT prototype

P_s is the H-bridge's loss. As achieving soft switching at full load, only conduction loss is considered. For a IGBT, reversed current flows through the antiparallel diode inside the IGBT. Hence, both the forward voltage for the IGBT (V_{CE}) and the forward voltage for the antiparallel diode (V_F) contribute to P_s. Since v_H is an alternate quasi-square wave, it only has odd order harmonic components. Therefore, the "n" term in (2-2) can be replaced by "(2k+1)", where the integer "k" goes from zero to infinity. Then the P_s can be calculated as

$$P_s = \frac{k+1}{2k+1} I_1 \cdot 2V_{CE} + \frac{k}{2k+1} I_1 \cdot 2V_F \,. \tag{2-14}$$

P_c is an AC loss caused by the equivalent series resistance (ESR) in the compensation capacitors. Film capacitor is chosen as it has the best AC performance over other materials. Usually,

the manufacturers provide a dissipation factor (DF or loss tan δ) instead of an ESR for film capacitor. The definition of loss tan δ is the ratio of the resistive power loss in the ESR to the reactive power oscillating in the capacitor. A capacitor with the smallest dissipation factor would minimize the resonant capacitor loss as

$$P_c = V_{Cp} \cdot I_1 \cdot \tan\delta_1 + V_{Cs} \cdot I_2 \cdot \tan\delta_2 . \tag{2-15}$$

P_d is the output diode bridge loss and is simply the conduction loss caused by the diode's forward voltage drop (V_d). The expression of P_d is

$$P_d = 4V_d \cdot I_2 . \tag{2-16}$$

P_w is the copper loss on the windings. R_p and R_s are the AC resistances at resonant frequency which are estimated by FEA software. Since the resonant network is dominated by resonant frequency component, P_w only accounts for one frequency component into consideration and it leads to a simple expression

$$P_w = I_1^2 R_p + I_2^2 R_s . \tag{2-17}$$

Core loss (P_t) calculation is based on Steinmetz model [9]. It is an integration on the volume (V) of the whole magnetic core. One has

$$P_t = \int C_m \cdot f^{\alpha} \cdot B^{\beta} \cdot (ct_0 - ct_1 \cdot T + ct_2 \cdot T^2) dV \ , \tag{2-18}$$

where, parameters (C_m, α, β and *ct*) are determined by core material and operating frequency. These parameters are usually provided by manufacturers. T is the temperature of the core; B is the magnetic flux density and f is the excitation frequency (resonant frequency). For the proposed IPT harmonic system, the selected harmonic current is dominant and flowing in the resonant tank. As a result, the flux in the core is at a fixed resonant frequency and is purely sinusoidal which matches

the simplest Steinmetz model. Because all the parameters in (2-18) become constant except magnetic flux density B, we have

$$P_t = C_m \cdot f^{\alpha} \cdot (ct_0 - ct_1 \cdot T + ct_2 \cdot T^2) \cdot \int B^{\beta} dV \,. \tag{2-19}$$

Fortunately, the integration of B^{β} over the whole core volume could be calculated and integrated by FEA software as Figure 2. 11 shows. FEA results also can show where the maximum magnetic flux (B_{max}) is. We should pay attention to B_{max} to avoid magnetic saturation with different core designs.

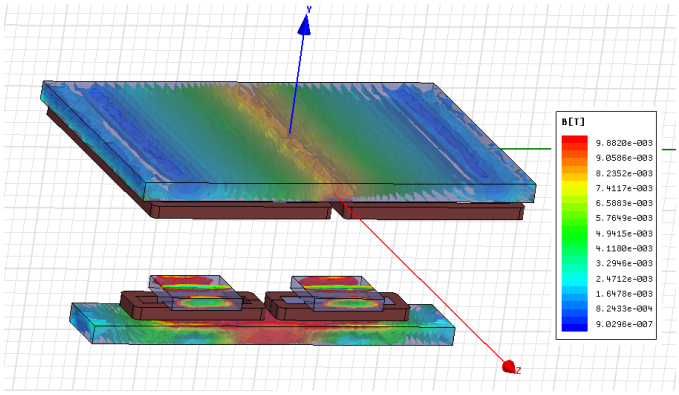


Figure 2. 11 FEA simulation result, magnetic flux plot on cores

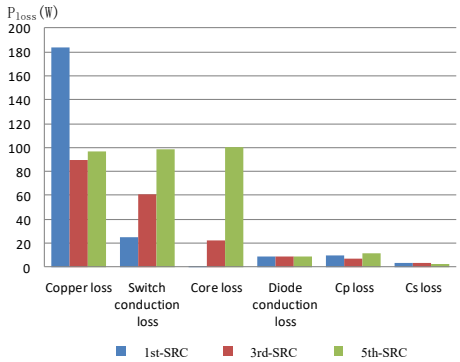


Figure 2. 12 Loss breakdown of the three IPT systems

Figure 2. 12 shows loss comparison between the three IPT systems. The secondary side losses, including diode conduction loss and C_s loss, are almost the same; this proves the previous discussion, that the secondary side only sees resonant frequency excitation from the primary side

and offers no information on which order of harmonic is being used. This also justifies that the design procedure begins from the secondary side parameter first.

The core loss increases dramatically as the excitation frequency increases, while the core material maintains the same. It is clear that for the 5th-SRC, a proper core material (which can work at around 100 kHz for this application) should be chosen to improve the efficiency.

The rest three losses (Copper loss, switch conduction loss, and C_p loss) are all related to primary side current's amplitude. Since the amplitude of I_1 increases almost linearly as the order of harmonic increases, the switch conduction loss increases linearly too. The AC losses on C_p are close to each other, because the series compensation capacitor C_p processes the same rated power. As for the copper loss, a higher order harmonic system has less turns on the windings; meanwhile, it needs more windings in parallel to handle the larger primary side current. In order to achieve a fair comparison, the three systems' current density is designed to be the same. The result shows that a higher order harmonic system indeed has less copper loss. However, in Figure 2. 12, the 5th-SRC exhibits a higher copper loss compared to that in the 3rd-SRC. This is because the 5th-SRC is not at its best performance which needs a factional turn number as Table 2. 2 shows. The circulating power in this 5th-SRC is not a minimum design. For harmonic orders even higher than 5^{th}, this mismatch problem would become worse and result in a degraded system. Therefore, only several low order harmonics are practical as the power carrier. In current design, the overall efficiency is 81%, 83% and 76% for the 1st-SRC, the 3rd-SRC and the 5th-SRC respectively.

2.3.2 Harmonic systems' window utilization factor

For a traditional transformer, the window utilization factor is the amount of copper (which includes insulation material) that appears in the window area of the transformer. This factor judges

if all the windings under a certain design could be squeezed inside the bobbin of the transformer. A large window utilization factor means the core is too small for these windings. On the other hand, a small window utilization factor indicates that there is some space left after winding the wires, and thus a smaller core could be an option. In WPT applications, the primary side and the secondary side are torn apart and the shapes of the core varies a lot. It is hard to describe it as a "window". Therefore, in order to give a comparison among these three systems regardless of the specific core's shape, a total winding length (TWL) and a winding insulation voltage are used to represent window utilization factor for comparison in WPT applications.

A. Total winding length

TWL is the sum of all the parallel wires' length. In order to maintain the same current density, higher current requires more wires in parallel. TWL is calculated as

$$TWL = N_1 \cdot num_1 \cdot MLT_1 + N_2 \cdot num_2 \cdot MLT_2 , \tag{2-20}$$

where num is the number of wires paralleled and MLT is mean turn length. Based on calculation, the 3rd-SRC reduces the total winding length to 62% of that in the 1st-SRC, and the 5th-SRC reduces to 37%. Higher order harmonic systems can reduce the window utilization factor dramatically and results in a smaller core design.

B. Winding insulation voltage

The maximum voltage imposed on the windings equals the maximum voltage on the compensation capacitor as they are a series resonant network. The maximum capacitor voltage happens at the instant that the 1-kW rated power fully charges the capacitor. Table 2. 3 shows the winding terminal voltage and the voltage between the adjacent turns for the three systems. In each row, the

values from the 1st-SRC are used as the based value for the other two harmonic systems. Higher order harmonic system has less voltage stress on the inductors' terminals as the total number of turns reduces. However, there is more voltage stress between the adjacent turns in higher order harmonic systems. The 5th-SRC has over three times the voltage stress on the winding insulation in primary side compared to that in the 1st-SRC. This leads to a thicker insulation layer and a higher window utilization factor. Fortunately, the minimum breakdown voltage for an enameled wire is around 700 V, following North America standard NEMA MW 1000 [6], and a usual commercial product provides 2.4 kV insulation with nylon served [7]. Therefore, the volume of insulation material does not increase under such power rating. The effect of insulation would kick in when the system's power rating becomes several times larger.

Table 2. 3 Winding insulation voltage for the three IPT systems

SRC-system		**1st (%)**	**3rd (%)**	**5th (%)**
Winding terminal voltage V_{max}	V_p	100 (1372 V)	35	27
	V_s	100 (2074 V)	108	84
Voltage in adjacent turns $V_{max}/(n-1)$	$V_p/(n-1)$	100 (57 V)	207	323
	$V_s/(n-1)$	100 (67 V)	178	236

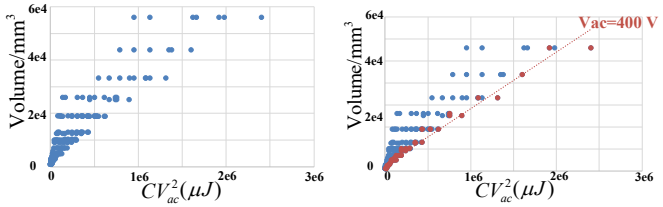
2.3.3 Harmonic systems' energy storage components

In the resonant network, there is one component, capacitor, that hasn't been addressed yet. The compensation capacitor in SRC is an AC energy storage component. In order to match the desired resonant frequency, it is more feasible to tune the compensation capacitance instead of modifying the cores and windings. Therefore, different capacitors with different values and ratings would be in series or parallel to achieve the designed rating and capacitance. Evaluating the total volume of all capacitors is a difficult task as there are different combinations in the way of series

or parallel. However, an approximate estimation could be made based on the energy that the capacitors process. Figure 2. 13 shows an example of capacitor volume-energy map from the datasheet of KEMET's R73 series capacitors [8]. The x-axis is the product of capacitance and rated AC voltage's square, which is the rated energy; and the y-axis is the volume calculated by its physical dimensions. Each capacitor in the datasheet becomes a point on the map as Figure 2. 13(a) shows. The points closer to the bottom right corner mean higher power density. Among all the data, one set of capacitors with 400 V AC rating voltage is marked red in Figure 2. 13(b). First, the capacitors in this set show a good linear relationship, which means the volume of the capacitor is strongly linearly related to the rated energy. Second, this set of capacitors is superior to other capacitors within the same series (which is usually the same material). By choosing capacitors along the red dash line in Figure 2. 13(b), no matter how we arrange the capacitors in series or parallel, which is a linear combination, the total volume would be minimum and approximately the same for the same rated energy. Different manufacturers or different materials may have different curves, but they share similar rules on volume-energy relationship. Since in all three systems, the compensation capacitors in series with the windings handle full rated power, their total volume would be approximately the same if we follow the selection rules discussed above.

The harmonic systems have their impact on both the input filter C_{in} and the output filter C_o. On the secondary side, the ripple current's frequency increases as the resonant frequency increases. The output filter C_o, which is carried on the vehicle, can be reduced to 1/n in a n^{th} harmonic system. On the other hand, the input filter C_{in} communicates with the load at switching

frequency that leads to n times ripple current in a n^{th} harmonic system. However, it is a good trade-off since less weight on the vehicle side is more attractive than the concern in primary side.



(a) (b)

Figure 2. 13 An example of capacitor volume-energy map from KEMET R73 series capacitors

2.4 Experimental results

A third harmonic IPT system rated 1 kW is originally designed with key parameters shown in Table 2. 4. The third harmonic system is changed to a fundamental operation for comparison with minimum modifications. Primary side winding turns and compensation capacitors in the resonant network for fundamental system are updated on the right-hand side of Table 2. 4. An efficiency comparison is carried out to verify the loss analysis in previous section.

Table 2. 4 Key parameters of the experimental prototype

Parameters	**Value**	**Parameters**	**Value**
Output	200 V/5 A	H-bridge	6MBP100VEA120
Switching frequency	f_{sw}=18 kHz	Output rectifier	15ETH03PBF
3rd-SRC		**1st-SRC**	
Turn ratio	5:20	Turn ratio	15:20
L_M	6.88uH	L_M	61.87uH
L_{ks}	1.07mH	L_{ks}	1.07mH
L_{kp}	46uH	L_{kp}	415uH
C_p	164nF	C_p	180nF
C_s	7.35nF	C_s	65.8nF
Resonant frequency	f_{re}=54 kHz	Resonant frequency	f_{re}=18 kHz

The experimental gain curve in Figure 2. 14 matches with calculation quite well. It exhibits a band-pass filter characteristic as discussed at the beginning. The resonant network has two peaks and one valley in the gain curve. Although the peak points give higher gain, the valley point (resonant frequency) gives minimum circulating current for the winding and provides the best efficiency. As the frequency band is so narrow, it is hard to regulate the load by only changing the frequency. This chapter concentrates on hardware design and the prototype always operates at the valley point in the efficiency test with different input or output voltages, regardless of the load regulation.

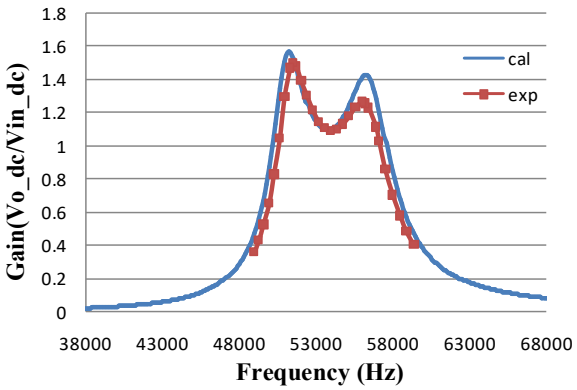
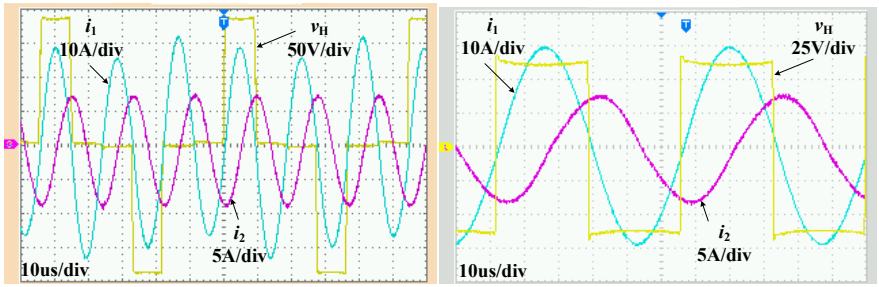


Figure 2. 14 Gain curve from output to input

Figure 2. 15 shows the key waveforms for both the 3rd-SRC and the 1st-SRC at full load with R_o=40 Ohm. In the 3rd-SRC, primary side current i_1 is in phase with the third harmonic component of v_H. It achieves soft switching both at turn-ons and turn-offs. Also, some fundamental and 5th harmonic components in primary side current I_1 are still visible but they would not cause any unstable issues. In contrast, secondary side current i_2 is purely sinusoidal at resonant frequency. The same variables are plotted in Figure 2. 15(b) for the 1st-SRC as a comparison. As the primary side winding turns is changed from 5 turns to 15 turns, it is not an optimal design for the 1st-SRC. The 1st-SRC has similar feature as the 3rd-SRC. The experimental waveforms here only justify that the band-pass filter concept works for different harmonic power carriers.



(a) (b)

Figure 2. 15 Experimental waveforms for third harmonic system (a) and for fundamental system (b) @Ro=40 Ohm

The efficiency curves for both systems are plotted in Figure 2. 16. The efficiency is measured with a fixed load (1-kW) without load regulation; therefore, the converter is always doing soft switching. The best efficiency point is predicted successfully for both systems. The best efficiency point for the 3rd-SRC is around R_o=40 Ohm, which verifies the analysis discussed above. The best efficiency point for the modified 1st-SRC is not at rated output condition (R_o=40 Ohm) and is shifted to around R_o=20 Ohm, as it is not the optimum design. However, this only proves the methodology proposed in this paper. For future research, a new prototype with the parameters in Table 2. 2 would be built to make a comparison side by side to draw the final conclusion in terms of size, weight and efficiency.

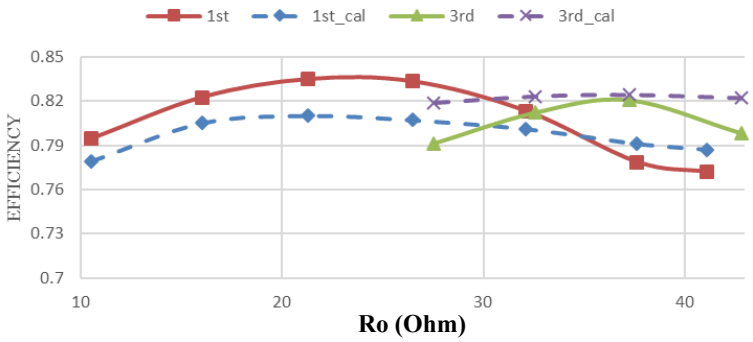


Figure 2. 16 Efficiency curve for the 1st-SRC and 3rd-SRC with different output resistances (fixed load 1-kW)

2.5 Summary

This chapter provides a design consideration on the usage of harmonic currents for PHEV and EV charger and a comprehensive comparison between different harmonic orders as the power

carrier. By taking advantage of the special band-pass feature of the resonant network in WPT applications, a harmonic system can be designed with less copper loss and less winding turns compared to that of the fundamental system. This extends the frequency limit of high voltage high current IGBT and shrinks the size of the resonant network dramatically. Moreover, a harmonic system enables a full load range operation of harmonic burst control, which achieves soft switching under any load conditions without any extra hardware, with acceptable pulse power stress. This harmonic burst control combined with the harmonic system can potentially save one stage for load regulation in WPT applications. The drawbacks are higher conduction loss on the switches and higher insulation voltage between adjacent turns that may degrade the window utilization factor. Higher harmonic system has higher resonant frequency that might need different core material. The total volume of compensation capacitor remains the same. For a given core structure, the analysis proposed in this chapter can be applied to determine the optimal order of harmonic that carries power. To verify the proposed design method, a 1-kW third harmonic system was built with 20-kHz IGBT achieving around 60-kHz system frequency. Furthermore, the prototype was modified to a fundamental system to prove the design methodology and the loss analysis.

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CHAPTER 3 Harmonic Burst Control for Wireless Charger

For battery charger, different charging stages need different charging specification to prolong the battery life. The series compensated wireless charger exhibits constant output current inherently and achieves CC mode without much effort. However, the CV mode may consume 40% of the total charging time. The efficiency in CV mode is essential for overall performance. Therefore, an efficiency way of load regulation is in demand. Both duty cycle control and PFM control have their own limitations on SRC. The SRC is left unregulated and freewheeling with varied air gaps or loads [1-3]. Then, one more front-end stage is needed to regulate the DC bus voltage [4]; and usually, this front-end stage also performs power factor correction [5-7]. Further, in [8], a 7-kW charger system is divided into three stages—a front end PFC converter, a buck converter for voltage regulation and a SRC, allowing the SRC to operate always at resonant frequency with high efficiency. To overcome the aforementioned load regulation issues within one single stage, this chapter illustrate a harmonic burst control which can achieve soft switching at any load conditions without any additional hardware.

3.1 Harmonics burst control

3.1.1 Power from harmonics

Each phase leg of the H-bridge inverter is operating at 50% complementary duty cycle, and the phase shift between the two legs actually controls the output voltage v_H. The PWM signals, together with the H-bridge output voltage waveform and its harmonics are shown in Figure 3. 1.

The H-bridge's output voltage (v_H) is a quasi-square waveform and is rich in harmonics. Its Fourier series expansion is expressed as

$$v_H = \sum_{n=1}^{\infty} \frac{4V_{in}}{n\pi} \sin(n\pi D)\sin(nt)\,. \tag{3-1}$$

and its 1st, 3rd, and 5th harmonic components' waveforms are shown at the right of Figure 3. 1. Due to the sharp peak characteristic (band-pass filter feature) of the resonant network, only the resonant frequency component of i_1 can pass to the secondary side of the converter, with all other frequency components filtered out by large impedance. Therefore, if the fundamental frequency of v_H is equal to the resonant frequency, the power transferred to the secondary side of the SRC is carried by the fundamental frequency. It is worth to specify that, if the switching frequency is 1/3 of resonant frequency, the 3rd harmonic is selected as shown in Figure 3. 2(a); or if the switching frequency is 1/5 of resonant frequency, the 5th harmonic is chosen as Figure 3. 2(b) shows, and so on.

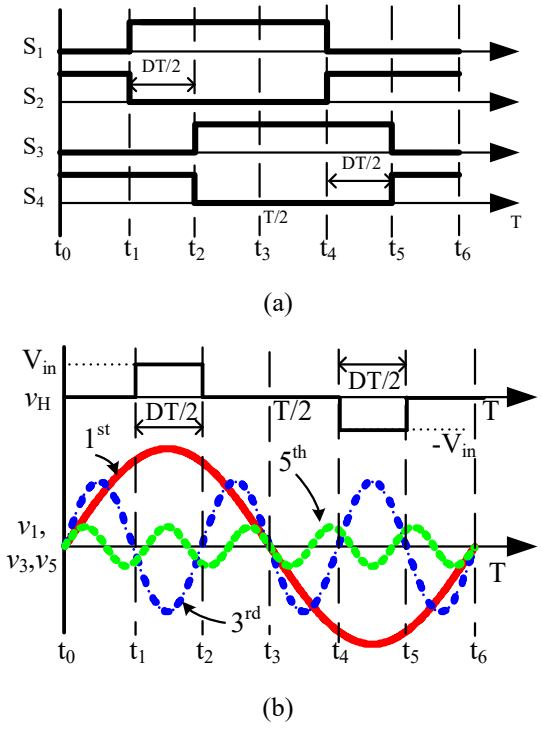


Figure 3. 1 PWM waveforms, H-bridge output voltage v_H, and H-bridge output voltage harmonics

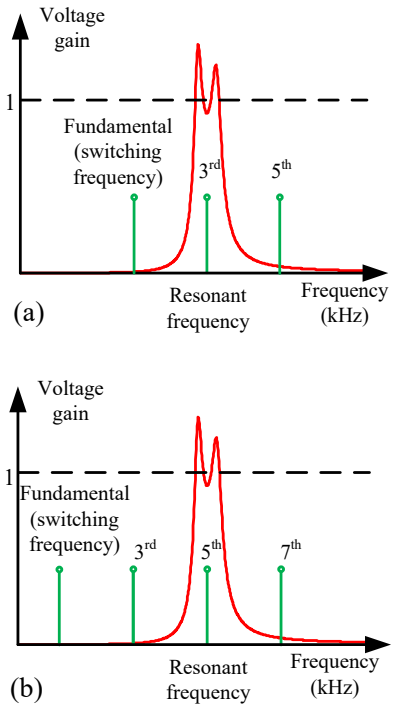
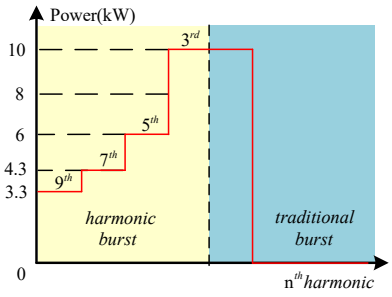
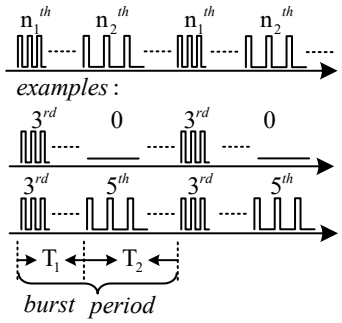


Figure 3. 2 Illustration of the harmonic power

Theoretically, every harmonic component can be used to transfer power. By selecting different harmonic components as the one, the converter can output distinct power levels to meet the demand from full load to light loads. These power levels are directly related to the order of harmonic when V_{in} and duty cycle are constant. They all have a maximum amplitude, when the n^{th} harmonic voltage $v_{H,n}$ equals to $4V_{in}/n\pi$ with $\sin(n\pi D)=1$ from (3-1). Figure 3. 3(a) shows an example of power levels provided by the 3^{rd}, 5^{th},7^{th} and 9^{th} harmonic components at their maximum amplitude conditions. As it can be seen, any power level between two adjacent harmonic components is out of reach. The traditional burst control is plotted on the right-hand side of Figure 3. 3(a) as a comparison. To cover all the load range, it only bursts with two power levels: full rated power and zero power. Thus, there would be huge pulsed power on both input and output side, which increases the ripple current stress for both input and output filters. Therefore, in order to cover all the load conditions and reduce the pulsed power stress, a harmonic burst control method is proposed.



(a) Power levels of harmonics



(b) Burst control examples

Figure 3. 3 Illustration of harmonic burst control

The methodology of the harmonic burst control method can be visualized in Figure 3. 3(b). Its basic idea is to combine two harmonic components in one burst period for different amounts of time depending on the output power P_o. One harmonic component (n_1^{th}) provides a power greater than or equal to P_o for a period T_1, and a second component (n_2^{th}) provides power less than P_o for a period T_2. One special combination contains a state called "silence state". This "silence state" means the converter continuously stays on zero state and its time duration belongs to T_2. By changing the duty cycle of each harmonic in one burst period, the output power can be continuously regulated.

For example, if any power between 3^{rd} and 5^{th} harmonic is needed (i.e. 8 kW in Figure 3. 3(a)), the converter can burst 3^{rd} harmonic for period T_1 and burst 5^{th} harmonic for period T_2, to keep the average power meeting the demand. Another way to get the same amount of power is by

combining the 3rd harmonic and the "silence state", which is actually the traditional burst control. In fact, there are infinite combinations of harmonic components. However, in practice, the more power difference between two harmonic components exists, the more chances the system would have to run into oscillation and pulsed power stress problems. Therefore, using two adjacent power levels to meet the demand can reduce this risk of oscillation and pulsed power stress.

3.1.2 Soft switching of each harmonic component

One appealing characteristic of the proposed method is the inherent soft-switching feature in each harmonic component of the H-bridge's output voltage. This feature can be explained by analyzing the v_H. Since v_H is an alternate quasi-square wave, it only has odd order harmonic components. Therefore, the "n" term in (3-1) is replaced by "(2k+1)", where the integer "k" goes from zero to infinity. Then, the mathematical expression of the harmonic components results in

$$v_{H,2k+1} = \frac{4V_{in}}{(2k+1)\pi}\sin[(2k+1)\pi D]\sin[(2k+1)t], \tag{3-2}$$

where the term $v_{H,2k+1}$ is the n^{th} harmonic component of v_H, V_{in} is the DC input voltage to the H-bridge, and D is the duty cycle. The maximum amplitude of the $(2k+1)^{th}$ harmonic is achieved when the first sinusoidal term in (3-2) becomes "1", and we have

$$D = \frac{1}{2(2k+1)}. \tag{3-3}$$

Figure 3. 4 shows the soft-switching characteristic of the 5^{th} harmonic component (k =2) under this maximum amplitude circumstance. Here, t_{on} is the time that two diagonal switching devices in the H-bridge are conducting, which equals half resonant period (T_{re}). Mathematically, t_{on} can be expressed as

$$t_{on} = D \cdot T_{sw} = D \cdot (2k+1)T_{re} = T_{re}/2. \tag{3-4}$$

The switching period T_{sw} is chosen to be (2k+1) times the resonant period T_{re}. Thus, the $(2k+1)^{th}$ harmonic at resonant frequency could pass to the secondary side. By defining the half resonant period as "time base" (T_{base}) in

$$T_{base} \equiv T_{re} / 2 \text{ ,} \tag{3-5}$$

T_{sw} and t_{on} can be expressed in terms of T_{base}, and one has

$$T_{sw} = 2(2k+1) \cdot T_{base} \tag{3-6}$$

and

$$t_{on} = 1 \cdot T_{base} \text{ .} \tag{3-7}$$

For the 5^{th} harmonic, t_{on} would be 1/10 of the switching period, which is T_{base}, and T_{re} is 1/5 of the switching period. In addition, the time intervals "t_1", "t_2", "t_3" and "t_4" (in Figure 3. 4) are all twice of T_{base}.

The output voltage of the full bridge inverter "v_H" and its harmonics have an odd symmetry with respect to the origin. Since the 5^{th} harmonic was selected for power transferring in this example, the primary side current i_1 is dominated by the 5^{th} harmonic component. Moreover, if the resonant network is fully compensated, the current i_1 is in phase with $v_{H,5}$, and it also has an odd symmetry with respect to the origin. Notice that the time that i_1 needs to return to zero is half resonant period ($0.5T_{re}$), which is exactly one t_{on} (T_{base}), and this leads to soft switching. This means that with a fully compensated resonant network, and a maximum amplitude control of $v_{H,5}$, soft switching can be achieved at both turn-ons and turn-offs. The previous analysis can be applied to any order harmonic selected to transfer power. Thus, we can conclude that the system can always

achieve soft switching both at switching on and switching off for any harmonic component selected to transfer power.

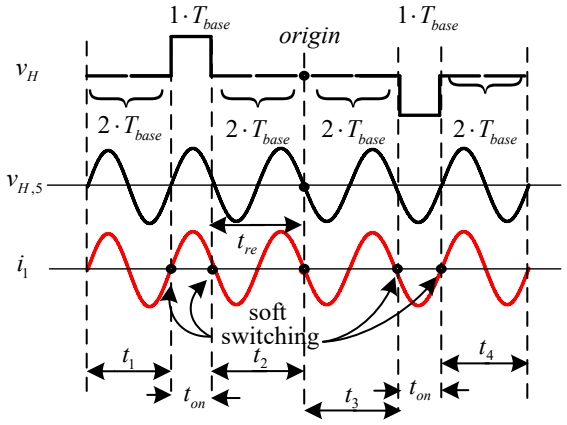


Figure 3. 4 H-bridge's output voltage and current of the full bridge inverter when passing through 5th harmonic (k=2)

3.1.3 Control diagram for harmonic burst

Burst control acts like an on-off control or bang-bang control. The basic idea to maintain the required output voltage is charging the output capacitor with a harmonic power larger than the demanded power until the output voltage reaches the upper limit. After this, switch to a harmonic power smaller than the demanded power and wait for the output voltage to hit the bottom limit. Figure 3. 5 shows the complete control diagram for harmonic burst. Only one output voltage sensor is needed to perform this control. The bang-bang control will make the output voltage to track a reference V_{o_ref} within a desirable ripple. The harmonics switching action takes place in the harmonic lookup table block. The output of this block is the phase shift φ between two phase legs and the switching frequency f_s, and each phase leg is operating at 50% duty cycle. Therefore, this harmonic burst control can be categorized into a variable-frequency phase-shift control. Specific phase shift φ and the switching frequency f_s can generate the required harmonic power, which is calculated off-line and stored in the harmonic lookup table. Since the only feedback is the output

voltage, the controller does not know the output power initially and cannot burst with the optimal harmonic combination according to the output power. As a result, one power estimation block is added to the controller. This block estimates the output power as a unified power reference P_{o_ref} (with full rating power as the base), by knowing the two bursting harmonics and the time duration of each harmonic (where D_1 is the duty cycle for the one with larger power). According to P_{o_ref}, some strategies for the harmonics selection can be applied to achieve the best performance. The selection algorithm is also implemented in the harmonic lookup table block. The discussion of these strategies will be presented in the next section.

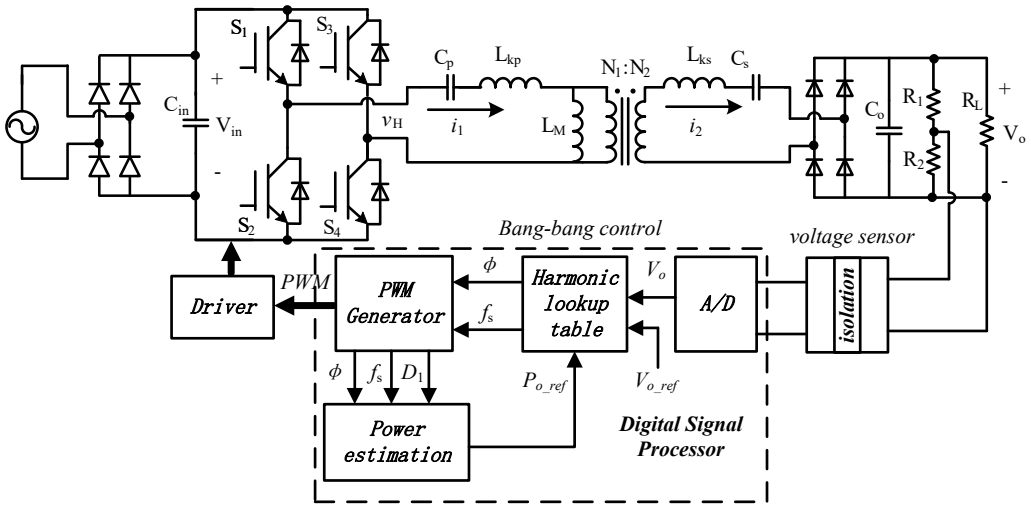


Figure 3. 5 Control diagram for harmonic bust

3.2 Design consideration for harmonic burst control

3.2.1 Loss analysis for a single harmonic

To make the loss analysis, the equivalent simplified circuit shown in Figure 3. 6 is used. In this figure, N equals N_2/N_1, and R_p and R_s are the AC resistances of the primary and secondary side windings, respectively. The ratio between the system copper loss and output power is obtained and expressed as

$$\frac{P_{copper}}{P_o} = \frac{I_p^2 \cdot R_p + I_s^2 \cdot R_s}{I_s^2 \cdot R_{ac}} = k_{cop} \,. \tag{3-8}$$

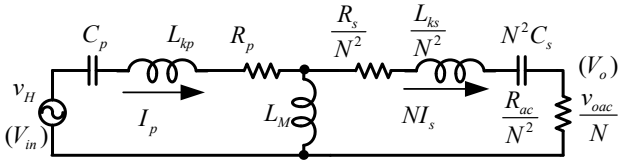


Figure 3. 6 Equivalent simplified circuit for SRC

This ratio (k_{cop}) is an important indicator of the system's efficiency and its graphical interpretation is shown in Figure 3. 7. Figure 3. 7 relates k_{cop} to the equivalent AC output resistance (labeled as mR_{ac}, where m =1 represents full load) without any control. A minimum point is observed in Figure 3. 7, which means there exists an optimum operation point at where the load impedance matches the resonant network impedance. For example, k_{cop} at 10% load would be four times higher than that at full load when full load is set at the minimum point of this curve. Furthermore, the corresponding quality factor curve is plotted in the same chart. One interesting phenomena is that the minimum point of Q is almost the same as that of k_{cop}. The circulating energy generates both copper loss and core loss and the quality factor takes both losses into account. However, different from traditional transformer design (which is optimized when the copper loss and the core loss are equal), the core loss and the copper loss are strongly related in WPT applications. Because of the weak coupling between the two windings, each winding behaves more like a single inductor. Hence, the flux density in the core is dominated by its winding current, and peak winding current induces peak flux density in the core. As a result, the k_{cop} and Q curves share a similar trend. The k_{cop} is directly related to efficiency. This k_{cop} is used instead

of quality factor as it is easier for understanding. For example, if k_{cop} equals 0.2, the efficiency must be below 80%. The following analysis is based on this k_{cop} instead of quality factor.

The harmonic selection takes the AC equivalent load into consideration. It is necessary to analyze the resonant network with different harmonic excitation before we get a full picture of loss analysis. Figure 3. 8 shows an equivalent circuit at resonant frequency, where all the leakage inductances are fully compensated with turn ratio N=1 for simplification.

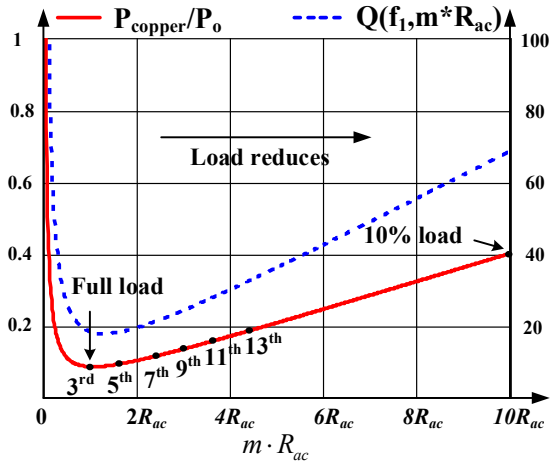


Figure 3. 7 Copper loss to output power ratio vs. output load at resonant frequency without regulation (open loop)

The switching frequency of the inverter is chosen deliberately such that the selected harmonic frequency equals the resonant frequency. Other harmonic components are greatly attenuated due to the band pass feature of the resonant network. The only difference among the harmonics selected ($v_{H,n}$) are their amplitudes which come from

$$v_{H,n} = \frac{4V_{in}}{n\pi}\sin(n\pi D)\sin(nt)\,. \tag{3-9}$$

When D equals 1/(2n), the maximum RMS value of $v_{H,n}$ is obtained and expressed as

$$\left|v_{H,n}\right|_{RMS} = 2\sqrt{2}V_{in}/n\pi\,. \tag{3-10}$$

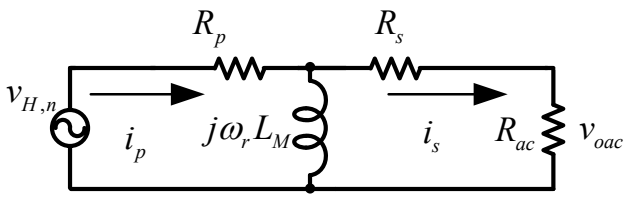


Figure 3. 8 Equivalent simplified circuit for SRC at resonant frequency (N=1)

Equation

$$|v_{oac}|_{RMS} = |v_{H,n}|_{RMS} \left| \frac{R_{ac} \cdot j\omega_r L_M}{R_p(R_s + R_{ac}) + j\omega_r L_M (R_p + R_s + R_{ac})} \right|$$

$$= |v_{H,n}|_{RMS} \left| \frac{j\omega_r L_M}{\left[R_p R_s + j\omega_r L_M (R_p + R_s) \right] / R_{ac} + R_p + j\omega_r L_M} \right| \quad (3\text{-}11)$$

shows the relationship between $v_{H,n}$ and the AC output voltage v_{oac} (AC voltage across the output rectifier). $|V_{oac}|_{RMS}$ only changes according to the order of harmonic selected and R_{ac}, since all the other parameters are constant. For example, if the selected harmonic changes from 3rd to 5th, $v_{H,n}$ would become 3/5 of $v_{H,n}$. Because R_p, R_s, L_M and ω_r are fixed, R_{ac} should be increased to maintain the same AC output voltage ($|V_{oac}|_{RMS}$) in the CV mode. As R_{ac} increases (load decreases), the selected harmonic and the percentage of copper loss also increases as mentioned before. Figure 3. 7 also illustrates the location of different harmonic components in the k_{cop} curve, with respect to R_{ac}. For example, the 13th harmonic has reached 20% copper loss and this loss keeps increasing as the order of selected harmonic increases. Since the harmonic selection affects the system efficiency, it has to be limited to a maximum value based on application. As a consequence, instead of infinite harmonic combinations, there are finite combinations. The next section focuses on predicting the burst efficiency with selected harmonics. This prediction is the key for the harmonic selection in the controller.

3.2.2 Efficiency analysis for burst control

As mentioned in the previous sections, each selected harmonic has its own efficiency. When doing burst control, the burst efficiency lies between the individual efficiency of the two selected harmonics. Therefore, the burst efficiency is the average of the two and it is expressed as

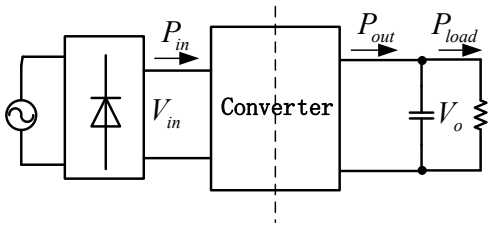
$$\eta_{burst} = \frac{P_{o\_avg}}{P_{i\_avg}} = \frac{D_1 P_{o1} + (1-D_1)P_{o2}}{D_1 P_{i1} + (1-D_1)P_{i2}}$$

$$= D_1 \frac{P_{o1}}{P_{i1}} \cdot \frac{P_{i1}}{D_1 P_{i1} + (1-D_1)P_{i2}} + (1-D_1)\frac{P_{o2}}{P_{i2}} \cdot \frac{P_{i2}}{D_1 P_{i1} + (1-D_1)P_{i2}} . \quad (3\text{-}12)$$

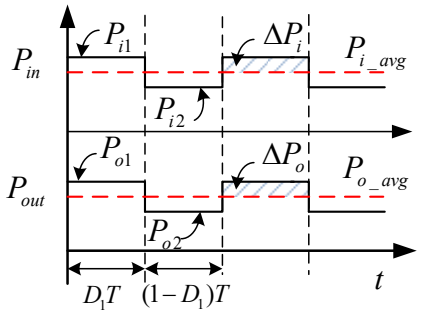
Here, D_1 is the percentage of time that the n_1^{th} harmonic is used, and $1\text{-}D_1$ represents the percentage of time that the n_2^{th} harmonic is used. A graphical illustration for this efficiency calculation is shown in Figure 3. 9(a) and (b), where P_{in} and P_{out} are the instantaneous power that the converter is possessing. On the output side, there is a big capacitor smoothing the power for the load (P_{load}). Furthermore, η_{n_1} is the efficiency of the system when using the n_1^{th} harmonic only, and η_{n_2} is the one when using the n_2^{th} harmonic. If P_{i1} is approximately equal to P_{i2}, equation (3-12) can be reduced to

$$\eta_{burst} \approx D_1 \frac{P_{o1}}{P_{i1}} + (1-D_1)\frac{P_{o2}}{P_{i2}} = \eta_{n_1} \cdot D_1 + \eta_{n_2} \cdot (1-D_1) . \quad (3\text{-}13)$$

This equation shows that the overall burst efficiency is approximately a linear combination of the two selected harmonics' efficiencies (η_{n_1} & η_{n_2}). In addition, for those containing "silence state", since the input (P_{i2}) and output power (P_{o2}) from the converter are zero in (3-12), η_{burst} would be equal to η_{n_1}.



(a) Power flow in circuit diagram



(b) Power flow in time domain

Figure 3. 9 Power flow with burst control

From the view of efficiency, high order harmonics would not be the best choice for power transfer and only several low order harmonics are feasible. This means that even though there are infinite combinations of harmonics, the practical combinations are limited. The combination of 3rd harmonic and "silence state" would always give the best efficiency according to Figure 3. 7 for current design. However, the large power difference between 3rd harmonic and "silence state" would cause large pulsed power and oscillation as there is a step response whenever switching from one to another.

3.2.3 Pulsed power in burst control

In order to illustrate the pulsed power in a simple way, we assume the converter in Figure 3. 9 is ideal and its efficiency is 100%. Thus, the input power equals output power. The pulsed power is the integration of ΔP_i or ΔP_o in Figure 3. 9(b), and we have

$$\Delta P = (P_1 - P_o)\frac{P_o - P_2}{P_1 - P_2}. \tag{3-14}$$

where P_1 and P_2 are the power ratings of the two bursting harmonics (P_1 is larger than P_2). Equation (3-14) is quadratic with respect to P_o and its maximum point is found when P_o equals $(P_1+P_2)/2$. The maximum pulsed power is expressed as

$$\Delta P_{\max} = (P_1 - P_2)/4 . \tag{3-15}$$

A unified pulsed power (using 10 kW as a base) in harmonic burst control is plotted in Figure 3. 10 with several harmonic combinations. The data for each harmonic is acquired from Figure 3. 3(a). Notice that the burst between 3rd harmonic and "silence state", which is the traditional burst control, has a pulsed power as high as one fourth of full rated power at half load. This high pulsed power would dramatically increase the current stress for both input and output filters. Actually, traditional burst control is widely adopted at light loads (which can be up to 30% of full load) to improve the efficiency, but it is seldom used at heavy loads due to this high pulsed power characteristic. From (3-15), the maximum pulsed power is determined by the power difference between the two burst components. For traditional burst control, the maximum pulsed power is around 0.2 per unit. On the other hand, harmonics provide more elements to burst, and therefore, the pulsed power can be minimized by selecting the proper harmonics. Several different combinations are explored in Figure 3. 10. Using the 5th harmonic or the 7th harmonic to burst with "silence state" can reduce the pulsed power at the middle range of load, but it does not provide a significant improvement for light loads. Bursting between two adjacent power levels (ex. 3rd and 5th, 5th and 7th) gives us the smallest pulsed power, as the power step is relatively small between two adjacent harmonics. By doing so, harmonic burst control can be applied to heavy load situations with an acceptable pulsed power, extending the traditional burst zone to all load conditions. However, the high order harmonics exhibit high copper loss, which makes it a trade-off between efficiency and pulsed power. Also, the system we analyzed here takes the benefit from

a 3rd harmonic oriented hardware design. If the system is designed for fundamental frequency, the first power gap between fundamental and 3rd harmonic is much larger than that between 3rd and 5th harmonics.

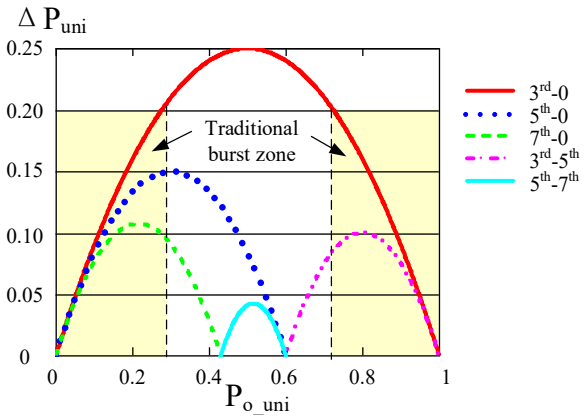


Figure 3. 10 Unified pulsed power vs. unified output power in harmonic burst control

3.3 Experimental results

The analysis and design guidelines of the proposed control system for EV battery charging applications are verified on a 1-kW prototype, whose parameters are summarized in Table 3. 1. Three control schemes were tested: the traditional frequency modulation method, burst with the adjacent harmonic, and burst with "silence state".

Table 3. 1 Key parameters of the experimental prototype

Items	Parameters	Items	Parameters
DC input voltage	190 V	H-bridge	6MBP100VEA120
Output	200 V/5A	Output rectifier	15ETH03PBF
Switching frequency	f_{sw}=18 kHz	Transformer ratio	5:20
Resonant frequency	f_{re}=54 kHz	L_M	6.88 uH
L_{kp}	46 uH	L_{ks}	1.07 mH
C_p	164 nF	C_s	7.35 nF
R_p	0.1 Ohm @f_{re}	R_s	1.4 Ohm @f_{re}

Figure 3. 11 shows the H-bridge's output voltage v_H and primary side resonant current i_1 at full load under the frequency modulation control method applied to region B. As it can be seen, there is a voltage spike during the switches' turn-offs at v_H due to some parasitic inductances around in the circuit.

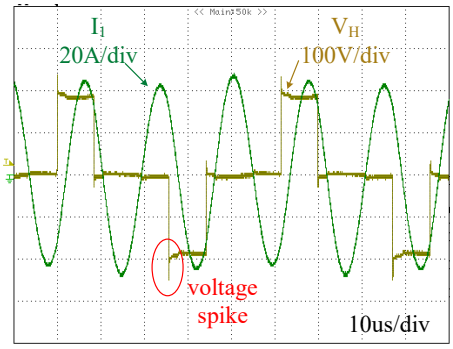
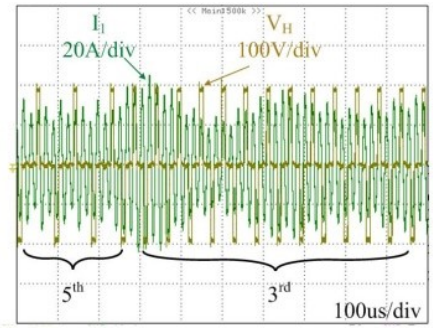


Figure 3. 11 Experimental waveforms of PFM @Full load

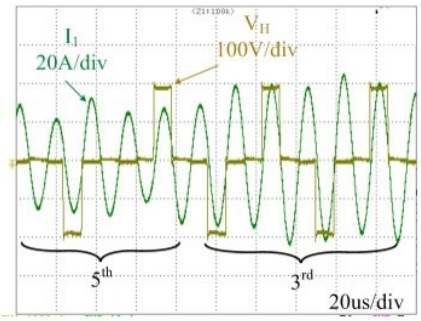
Figure 3. 12 illustrates the waveforms when the converter is controlled by harmonic burst between 3rd and 5th at 66% load. Soft switching is achieved at both turn-ons and turn-offs. Also, the transition from 5th to 3rd harmonic is smooth, since the power levels of these two harmonics is close.



(a) Transient from 5th harmonic to 3rd harmonic

Figure 3. 12 Experimental waveforms of burst between 3rd& 5th @66% load

Figure 3. 12 (cont'd)



(b) Zoom in of (a)

The waveform of harmonic burst between 3rd and "silence state" is shown in Figure 3. 13. It is stable and there is almost no overshoot when transitioning between 3rd and "silence state". The switching period of the two harmonics depends on the output voltage ripple and the size of output filter, which was 4.7 mF here to simulate a battery load. Figure 3. 14 shows a zoom-in image of Figure 3. 13. When switching from "silence state" to 3rd harmonic, there is some oscillation before it reaches stable state. To avoid or damp this oscillation, a harmonic sequence of 3rd, 7th and 3rd is implemented into the startup period as shown in Figure 3. 14(a). On the other hand, when changing from 3rd harmonic to "silence state", the current i_1 decreases to zero quickly after the "silence state" begins as shown in Figure 3. 14(b). When this happens, the diode bridge in the secondary side would be off and the energy stored in the resonant tank begins to flow back to the primary side. Therefore, the current i_1 oscillates again for several cycles until all the energy in the resonant tank is zero.

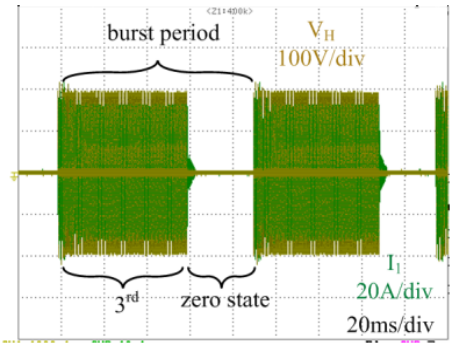
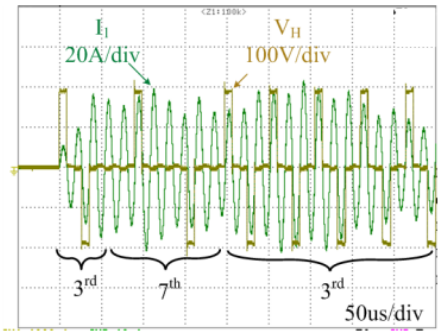
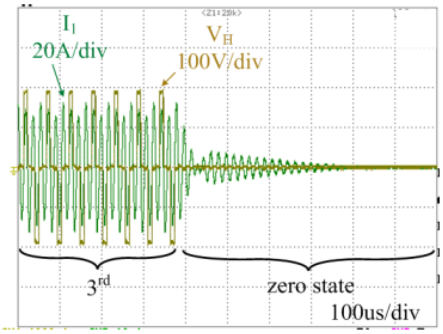


Figure 3. 13 Experimental waveforms of burst between 3rd harmonic and "silence state" @66% load



(a)Switching from "silence state" to 3rd



(b)Switching from 3rd to "silence state"

Figure 3. 14 Zoom in waveforms of burst between 3rd harmonic and "silence state" @66% load

The efficiency comparison among these control methods is shown in Figure 3. 15. The traditional frequency modulation method gives the lowest efficiency because it does not work at the best efficiency point. The burst between low order harmonics and "silence state" has a flat efficiency over a wide range of load. The burst between two adjacent harmonic shows good efficiency at heavy loads but poor efficiency at light loads. For practical applications, the control strategy can be a combination of adjacent mode and the mode with "silence state" according to the load conditions. For example, adjacent harmonics is preferred at 60% load or higher due to its low pulsed power, and relative high efficiency compared to traditional burst (3rd and silence state). For the load range from 20% to 60%, burst between 5th harmonic and silence state becomes a better candidate as the efficiency for adjacent harmonics drops significantly. At light loads (below 20%),

pulsed power performance for burst between 5th harmonic and silence state, and traditional burst are similar, therefore, traditional burst is chosen as it has the best efficiency.

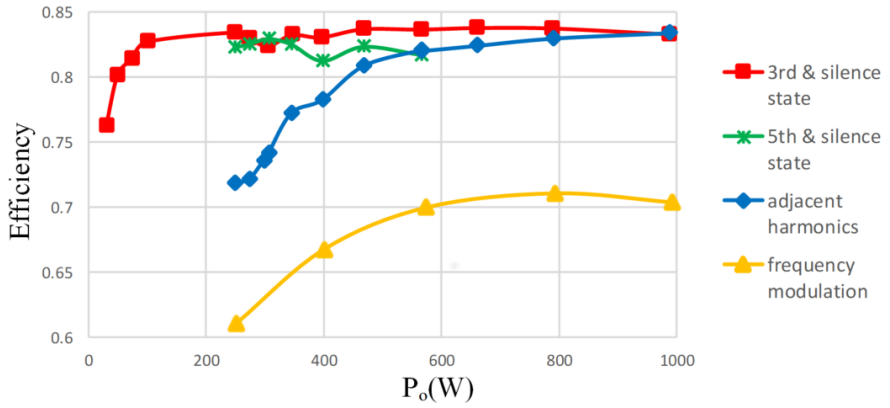


Figure 3. 15 Experimental result of efficiency with different regulation method

The loss break-down chart at full load is shown in Figure 3. 16. The labels "C_p loss" and "C_s loss" are short for primary side compensation capacitor loss and secondary side compensation capacitor loss, respectively. Switching loss is not included for comparison as they are not present in harmonic burst control. The two control methods have the same loss on the system's secondary side, which includes the diode conduction loss and the C_s loss. The main difference in terms of losses between the two control methods are in the primary side. Frequency modulation control has a much higher k_{cop} than that of harmonic burst control, therefore, it has a much larger circulating current in the primary side. Because of this, the winding's copper loss, the switches conduction loss, and the C_p loss dramatically increase. It is worth to notice that the core loss has a reverse trend. The magnetic field in the core is the joint effect of the primary and secondary side current. Even though the amplitude of the primary side current increases, the phase shift variation between this current and secondary side one could also affect the intensity of the magnetic field in the core. However, as we can see in the loss break-down chart, the conduction loss is dominant and the harmonic burst control has less total loss than that of frequency modulation control.

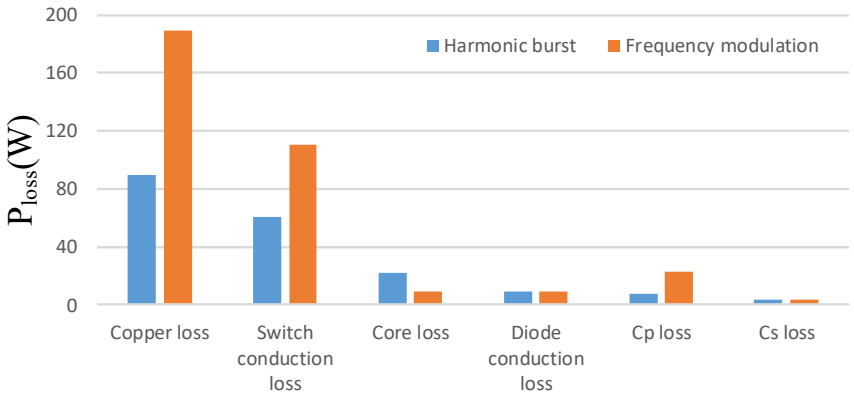


Figure 3. 16 Calculation result of loss break down with different regulation method at full load

3.4 Summary

This chapter proposes an effective output voltage control method using harmonic burst control for EV battery charging applications. By bursting between different harmonics, not only the load regulation is realized but also soft switching at both turn-ons and turn-offs is achieved. Compared to the traditional burst control, it has much smaller pulsed power over a wide range load. A 1-kW prototype with 20-cm air gap using power from harmonics was built to verify the proposed method. The overall efficiency of harmonic burst control is over 10% higher than the traditional frequency modulation control, especially for light-load conditions.

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CHAPTER 4 Z-source Resonant Wireless Charger: Operation Principle

A complete WPT system usually consists of a front-end AC/DC stage and a cascaded DC/DC stage. The power factor correction function and load regulation function are handled by each stage. Recently, a Z-source resonant wireless charger which performs the power factor correction and load regulation for the conventional WPT system without adding extra semiconductor switches was proposed [1] as Figure 4. 1 shows. This topology saves the PFC front end stage, and therefore the system has low cost and high efficiency. Also, the Z-source network can operate at continuous conduction mode (CCM) and has high reliability as being immune to shoot-through problems. Both of these features make it suitable for high power application. However, the control scheme is complicated and challenging as the two functions are realized within a single H-bridge. This chapter illustrates the mechanism of Z-source resonant converter and analyzes the modulation methods for DC/DC performance.

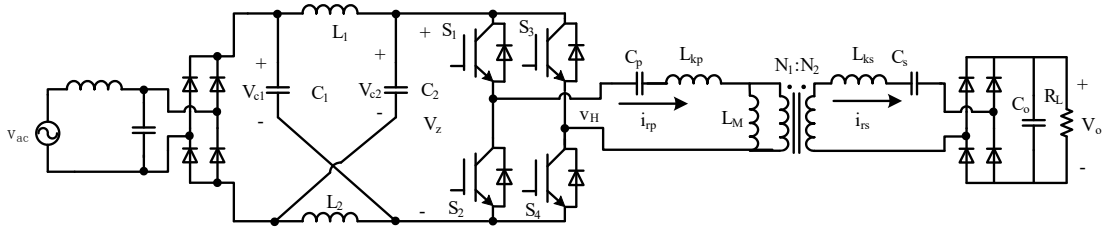
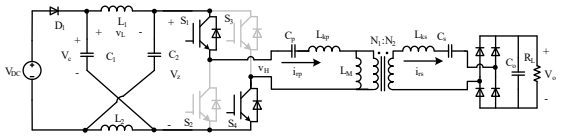


Figure 4. 1 Circuit schematic of the proposed Z-source wireless charger

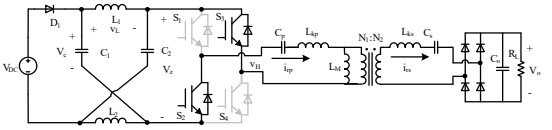
4.1 Mechanism of Z-source resonant converter

To describe the mechanism of ZSRC, the AC input stage is simplified as a DC source input with one series diode. Assumes that the ZSN is symmetrical ($C_1 = C_2 = C$, and $L_1 = L_2 = L$), therefore, $V_{C1} = V_{C2} = V_C$, and $v_{L1} = v_{L2} = v_L$. Figure 4. 2 shows the simplified circuit in different

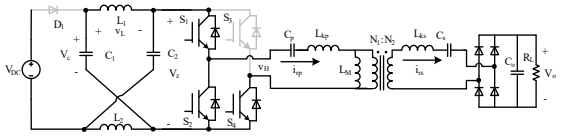
mode—active state, shoot-through zero state and normal zero state. The time domain waveforms of these states are illustrated in Figure 4. 3. The fundamental component of H-bridge output voltage is in phase with the primary side current i_{rp} at resonant frequency, and the total time of shoot-through zero state (T_{st}) is evenly distributed over one switching cycle. With such PWM modulation method, no extra switching action is needed to realize shoot-through zero state.



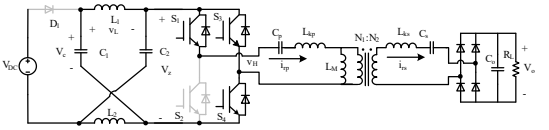
(a) Active state, t_2~t_3



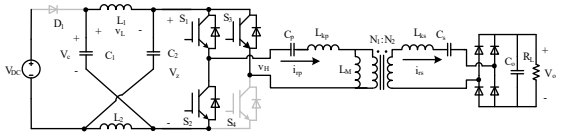
(b) Active state, t_6~t_7



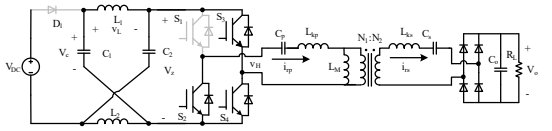
(c) Shoot-through zero state, t_1~t_2



(d) Shoot-through zero state, t_3~t_4



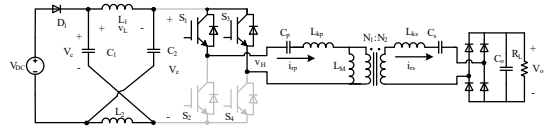
(e) Shoot-through zero state, t_5~t_6



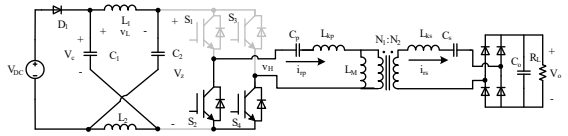
(f) Shoot-through zero state, t_7~t_8

Figure 4. 2 Simplified ZSRC circuit diagram in different mode

Figure 4. 2 (cont'd)



(g) Normal zero state, t_4~t_5



(h) Normal zero state, t_0~t_1 & t_8~t_9

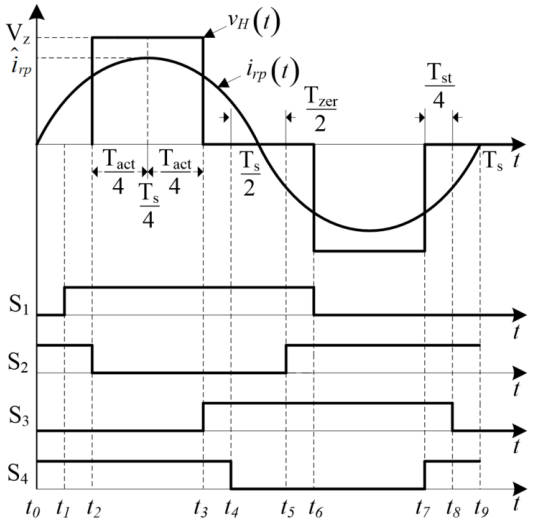


Figure 4. 3 ZSRC H-bridge output voltage, primary side resonant current, and PWM waveforms (phase shift control)

4.1.1 Shoot-through state duty cycle derivation

Active state

During the two active states time interval (Figure 4. 2 (a)&(b)), the diagonal switches are ON, and the input side diode D_1 is conducting. The resonant network draws current both from the ZSN inductor and capacitor. The difference between load current (i_{rp}) and ZSN inductor current i_L is provided by a series connection of the two ZSN capacitor and DC source [2]. The current going through the switches are only load current (i_{rp}). The ZSN inductor voltage for this time interval is given as

$$v_L = v_{DC} - V_C = |\hat{v}_{ac} \sin(\omega t)| - V_C . \tag{4-1}$$

Shoot-through zero state

Four shoot-through zero states time intervals are demonstrated in Figure 4. 2(c), (d), (e) and (f). Three of the switches are ON. The two horizontal switches are carrying the load current and the switches in one phase leg are carrying the ZSN inductor current. Hence, there is one switch carrying the sum of the two currents. Since the ZSN inductor current is always one direction and the load current would be bipolar, these two currents subtract each other in Figure 4. 2(c)&(d) and add to the sum with their absolute value in Figure 4. 2(e)&(f). Here the ZSN capacitors will charge ZSN inductors (this is how the ZSRC can boost the voltage) [2]. The ZSN inductor voltage for this time interval is given as

$$v_L = V_C . \tag{4-2}$$

Normal zero state

During the normal zero states time interval (Figure 4.2 (g)&(h)), two horizontal switches are ON. The ZSN is isolated from the load. The load current is freewheeling and the ZSN inductors charge the ZSN capacitors. The ZSN inductor voltage for this time interval is given as

$$v_L = v_{DC} - V_C = |\hat{v}_{ac} \sin(\omega t)| - V_C . \tag{4-3}$$

To derive the expression for the shoot-through duty cycle, use voltage second balance across the ZSN inductor over one switching cycle. Therefore, by using (4-1), (4-2), and (4-3) we have

$$\frac{T_{act}}{T_S}\left(|\hat{v}_{ac} \sin(\omega t)| - V_C\right) + \frac{T_{st}}{T_S} V_C + \left(1 - \frac{T_{act}}{T_S} - \frac{T_{st}}{T_S}\right)(|\hat{v}_{ac} \sin(\omega t)| - V_C) = 0 , \tag{4-4}$$

where the switching cycle is defined as $T_S = T_{act} + T_{st} + T_{zer}$, the active state duty cycle is defined as $D_{act}=T_{act}/T_s$, and the shoot-through state duty cycle is defined as $D_{st}=T_{st}/T_s$. By solving (4-4), we have

$$V_C = \frac{1-D_{st}}{1-2D_{st}}\left|\hat{v}_{ac}\sin(\omega t)\right|, \tag{4-5}$$

and

$$D_{st} = \frac{v_z - \left|\hat{v}_{ac}\sin(\omega t)\right|}{2v_z} = \frac{V_C - \left|\hat{v}_{ac}\sin(\omega t)\right|}{2V_C - \left|\hat{v}_{ac}\sin(\omega t)\right|}. \tag{4-6}$$

This relationship in (4-6) gives us a hint that the voltage on ZSN capacitor is irrelevant to active state duty cycle D_{act}.

4.1.2 Output voltage derivation

An expression for the output voltage (V_o) in terms of the active and shoot-through state duty cycles (D_{act} and D_{st} respectively), and the AC input voltage (v_{ac}) is derived in this section. Also, if we assume that the system is ideal, the average AC power at the resonant network is the same as the instantaneous output power. Mathematically this is given by the following relationship derived from Figure 4. 3. The instantaneous output power over one switching cycle is

$$P_o = \frac{1}{T_s}\int_0^{T_s} v_H(\tau) i_{rp}(\tau) d\tau . \tag{4-7}$$

Further developing (4-7), we have

$$P_o(t) = \frac{2}{T_s}\int_{\frac{T_s}{4}-\frac{T_{act}(t)}{4}}^{\frac{T_s}{4}+\frac{T_{act}(t)}{4}} \hat{v}_H(t)\hat{i}_{rp}(t)\sin(\omega_s\tau) d\tau , \tag{4-8}$$

where $\hat{v}_H(t) = v_Z$ is the peak value of $v_H(t)$, and ω_s is the angular switching frequency which is equal to the angular resonant frequency. After integration, one has

$$P_o(t) = \frac{4\hat{v}_H(t)\hat{i}_{rp}(t)}{T_s}\sin(\frac{\pi D_{act}(t)}{2}). \tag{4-9}$$

Assuming that the average value of the absolute value of the resonant network secondary side current $|i_{rs}(t)|$ is equal to the output current (I_o), the instantaneous value of $i_{rs}(t)$ will be given by

$$i_{rs}(t) = \frac{\pi I_o}{2}\sin(\omega_s t). \tag{4-10}$$

By transferring $i_{rs}(t)$ to the primary side, the expression for the resonant network primary side current peak value $\hat{i}_{rp}$ will be given as

$$\hat{i}_{rp}(t) = \frac{\pi I_o}{2k_{res}} = \frac{\pi V_o}{2k_{res}R_o}, \tag{4-11}$$

where the resonant gain factor k_{res} not only depends on the transformer turns ratio but also on the resonant network characteristics.

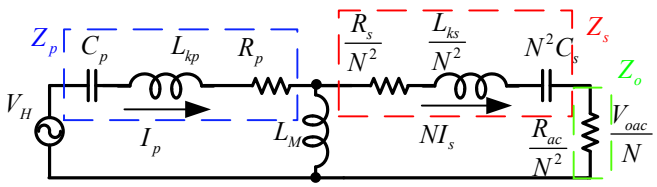


Figure 4. 4 A simplified circuit of the resonant network.

Figure 4. 4 shows a simplified circuit of the resonant network. R_{ac} is the AC equivalent resistor that can be expressed as

$$R_{ac} = \frac{8}{\pi^2}R_o. \tag{4-12}$$

Z_p and Z_s are primary side impedance and secondary side impedance respectively. Z_o represents the output impedance. N is the turn ratio. By analyzing this simplified circuit, the value of k_{res} can be obtained as

$$k_{res}(\omega) = \frac{I_s}{I_p} = \frac{\frac{1}{N} \cdot j\omega L_M}{j\omega L_M + Z_s + Z_o}. \tag{4-13}$$

It is a frequency depended variable. For this resonant network, only resonant frequency component (ω_0) is considered. Substituting (4-6) and (4-11) in (4-9) we have

$$P_o(t) = \frac{V_o |v_{ac}(t)|}{k_{res}(\omega_0) R_o (1 - 2D_{st}(t))} \sin(\frac{\pi D_{act}(t)}{2}). \tag{4-14}$$

The output power is the integration of (4-14) over one fundamental period as

$$\bar{P}_o(v_{ac}, D_{st}, D_{act}) = \int_0^{\frac{1}{60}} P_o(t) dt. \tag{4-15}$$

Then, the expression for the output voltage is as follows

$$V_o(t) = \frac{|v_{ac}(t)|}{k_{res}(\omega_0)(1 - 2D_{st}(t))} \sin(\frac{\pi D_{act}(t)}{2}). \tag{4-16}$$

The average of the latest expression is the one actually used in the controller to regulate the output voltage as

$$\bar{V}_o(v_{ac}, D_{st}, D_{act}) = \int_0^{\frac{1}{60}} V_o(t) dt. \tag{4-17}$$

As (4-15) and (4-17) show, the output power and voltage can be control by D_{st} and D_{act}. One simple control method is using D_{act} to regulate the voltage and realize PFC function by D_{st}.

4.2 Load regulation methods

As the present of shoot-through state, the H-bridge has one more control freedom to cope with. For resonant converters, the resonant current is changing in one switching cycle. The arrangement of shoot-through state and active state matters. These two factors make the control scheme challenging. This section presents two load regulation methods for DC/DC case, traditional phase-shift control and pulse notch control.

4.2.1 Traditional phase-shift control

The fundamental component of H-bridge output is in phase with the primary side current i_{rp} at resonant frequency, and the total time of shoot-through state (T_{st}) is evenly distributed over one switching cycle as Figure 4. 5 shows. With such phase shift PWM modulation method, no extra switching action is needed to achieve arbitrary active state and shoot-through state duty cycle.

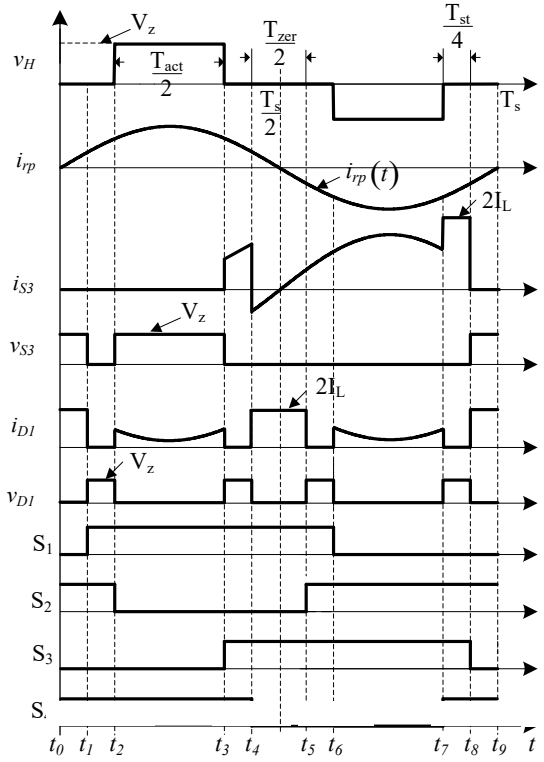


Figure 4. 5 Time domain waveforms for phase-shift control in ZSRC

To derive the expression for the shoot-through state duty cycle in DC/DC case, equation (4-4) can be reduced to

$$\frac{T_{act}}{T_S}(V_{DC}-V_C)+\frac{T_{st}}{T_S}V_C+\left(1-\frac{T_{act}}{T_S}-\frac{T_{st}}{T_S}\right)(V_{DC}-V_C)=0, \tag{4-18}$$

where the switching period is defined as $T_s=T_{act}+T_{st}+T_{zer}$. The active state duty cycle is defined as $D_{act}=T_{act}/T_s$, and the shoot-through state duty cycle is defined as $D_{st}=T_{st}/T_s$. By solving (4-18), we have

$$V_C=\frac{1-D_{st}}{1-2D_{st}}V_{DC}, \tag{4-19}$$

$$D_{st}=\frac{V_z-V_{DC}}{2V_z}=\frac{V_C-V_{DC}}{2V_C-V_{DC}}, \tag{4-20}$$

and

$$V_z=\frac{V_{DC}}{1-2D_{st}}. \tag{4-21}$$

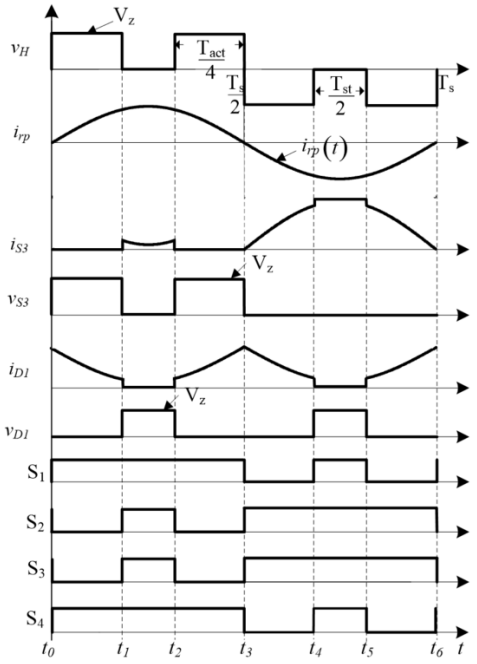
This relationship in (4-20) gives us a hint that the voltage on ZSN capacitor is irrelevant to active state duty cycle D_{act}.

These three states are all the possible states in ZSRC. Different allocation of these three states along one switching period would generate different load regulation characteristic.

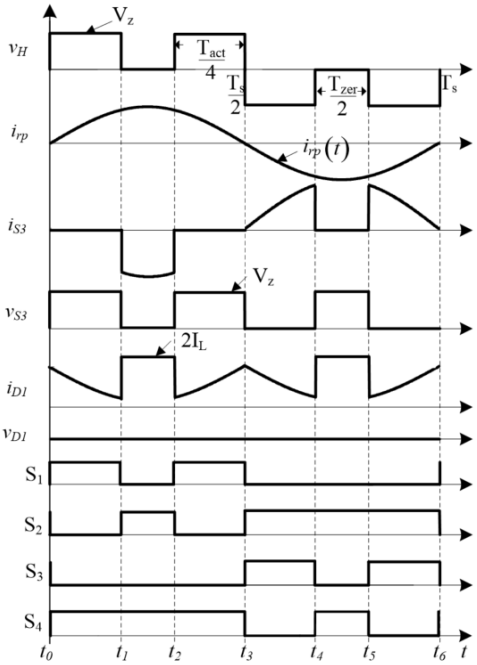
4.2.2 Pulse notch control

In phase shift control, different phase shifts actually generate different amplitudes of the fundamental component at switching frequency. Thus, controlling a notch width shares a similar idea as Figure 4. 6 shows. Pulse notch control is usually used in a 3-phase system [3], as it does

not damage the symmetry of the 3-phase system. In the case of single phase ZSRC, this notch can be either shoot-through state or zero state, which is illustrated in Figure 4. 6(a)&(b) respectively.



(a) Shoot-through notch



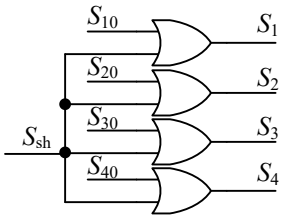
(b) Zero notch

Figure 4. 6 Time domain waveforms for pulse notch control in ZSRC

The shoot-through notch will increase the output power as the boost from the shoot-through state surpasses the loss in active state. The mathematic explanation will be expanded in the next section. The original control signals (S10, S20, S30 and S40) come from a 50% duty cycle with constant frequency PMW signal. Apart from that, one control logic block (Figure 4. 7(a)) is inserted between these original signals and gate signals (S1, S2, S3 and S4). When the shoot-though control signal S_{sh} is high, all the gate signals are forced high as t_1~t_2 and t_4~t_5 in Figure 4. 6(a). The shoot-through notch is placed in the middle of active state for the sake of symmetry.

Figure 4. 6(b) shows another kind of notch. Zero state is filled in the middle of active state. Zero notch will help regulating the output power downward. The control concept is similar to the previous one. The original control signals (S10, S20, S30 and S40) come from a 50% duty cycle with constant frequency PMW signal. One control logic block (Figure 4. 7(b)) is inserted between these original signals and gate signals (S1, S2, S3 and S4). When the zero control signal S_{zer} is high, S2&S4 are forced high and S1&S3 are forced low. For simplicity, here only utilize the zero state with two bottom switches. It is worth noting that S3 and S4 have the same current waveform with notch as shown in Figure 4. 7(b). And, S1 and S2 have half sinusoidal current waveform without notch because of the asymmetric control.

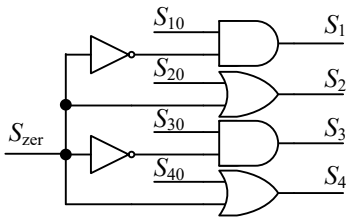
This pulse notch control actually doubles the switching frequency, but the excitation frequency for the resonant network remains the same.



(a) Shoot-through notch

Figure 4. 7 Control logic block inserted for pulse notch control

Figure 4. 7 (cont'd)



(b) Zero notch

4.2.3 Output power regulation

In order to get the output power derivation, the WPT system can be simplified as one voltage source v_H and a resonant network with all the parameters reflected to primary side. In Figure 4. 8, the voltage source v_H is the output of H-bridge and it contains different frequency components.

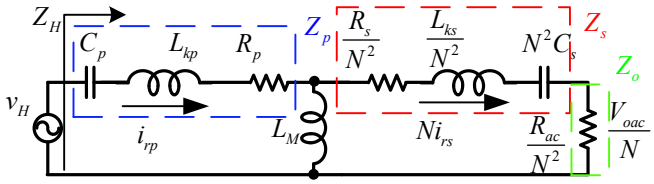


Figure 4. 8 A simplified circuit of the resonant network

R_{ac} is the AC equivalent resistor. Z_p and Z_s are primary side impedance and secondary side impedance respectively. Z_o represents the output impedance. N is the turn ratio. The impedance from the output terminals of H-bridge (Z_H) is

$$Z_H(\omega) = Z_p(\omega) + \frac{(Z_s(\omega) + Z_o) \cdot j\omega L_M}{j\omega L_M + Z_s(\omega) + Z_o}. \tag{4-22}$$

Also, at resonant frequency ω_0, with certain compensation, the impedance Z_H is purely resistive (R_H). We have

$$R_H = Z_H(\omega_0) = R_p + \frac{(\omega_0 L_M)^2}{(R_{ac} + R_s)/N^2}. \tag{4-23}$$

In WPT system, only the resonant frequency component is carrying power, while other frequency components are greatly attenuated by the resonant network. Therefore, the resonant component of $v_H(t)$ is

$$v_{H,1} = \frac{\sqrt{2}}{T_s}\int_0^{T_s} v_H(\tau)\sin(\omega_s\tau)d\tau\,. \tag{4-24}$$

Based on different time domain waveforms of different control methods in Figure 4. 5 and Figure 4. 6, the integration of active state in (4-24) will give us

$$v_{H,1} = \frac{2\sqrt{2}}{T_s}\int_{\frac{T_s}{4}-\frac{T_{act}}{4}}^{\frac{T_s}{4}+\frac{T_{act}}{4}} V_z\sin(\omega_s\tau)d\tau = \frac{V_{in}}{(1-2D_{st})}\frac{2\sqrt{2}}{T_s}\int_{\frac{T_s}{4}-\frac{T_{act}}{4}}^{\frac{T_s}{4}+\frac{T_{act}}{4}}\sin(\frac{2\pi}{T_s}\tau)d\tau = \frac{2\sqrt{2}V_{in}}{\pi(1-2D_{st})}\sin(\frac{\pi D_{act}}{2})\,, \tag{4-25}$$

and

$$v_{H,1} = \frac{4\sqrt{2}}{T_s}\int_0^{\frac{T_{act}}{4}} V_z\sin(\omega_s\tau)d\tau = \frac{2\sqrt{2}V_{in}}{\pi(1-2D_{st})}\left[1-\cos(\frac{\pi D_{act}}{2})\right]. \tag{4-26}$$

Formula (4-25) is for phase shift control and (4-26) is for pulse notch control. Then, the output power from H-bridge is

$$P_H = \frac{v_{H,1}^2}{R_H}\,. \tag{4-27}$$

As the resonant network is all passive components and they are all linear, the final output power P_o is proportional to P_H. For the sake of examining output power regulation, a unified expression for both control methods is enough. We have

$$P_{o,uni} = \frac{P_H}{P_{H,uni}} = \frac{\left[\frac{2\sqrt{2}V_{in}}{\pi(1-2D_{st})}\sin(\frac{\pi D_{act}}{2})\right]^2/R_H}{P_{H,uni}} = \frac{\frac{8V_{in}^{\,2}}{\pi^2 R_H}\left[\frac{\sin(\frac{\pi D_{act}}{2})}{(1-2D_{st})}\right]^2}{P_{H,uni}} = \left[\frac{\sin(\frac{\pi D_{act}}{2})}{(1-2D_{st})}\right]^2, \tag{4-28}$$

and

$$P_{o,uni} = \left[\frac{1-\cos(\frac{\pi D_{act}}{2})}{(1-2D_{st})} \right]^2, \tag{4-29}$$

where $P_{H,uni}$ is the base value that equals $8V_{in}^2/(\pi^2 R_H)$. These two unified power expressions are plotted in Figure 4. 9 and Figure 4. 10 respectively. When the shoot-through duty cycle D_{st} is zero and active state duty cycle D_{act} is 1, both of them generate one unit of power. They are actually the same with 50% duty cycle. From this unit power point upward, it needs certain amount of D_{st} to boost the power for both control methods. From this point downward, D_{act} is the leading role of regulation.

The upward difference between these two control methods is the slope of the full duty cycle boundary ($D_{act}+D_{st}=1$). Phase shift control has a higher slope which means the same amount of D_{st} will generate more power. Hence, for the same output power (larger than 1), phase shift control would have less voltage stress on the switch compared to the other one. Also, phase shift control can work in the entire continuous region, while the pulse notch control can only work at the downward curve where $D_{st}=0$. In order to work at the entire continuous region for pulse notch control, it needs to combine shoot-through notch and zero notch in one switching cycle, which increases the switching frequency a lot and is not preferred. However, the continuous region can reach zero in pulse notch control, while the other one is clamped at a certain point. This important characteristic of discontinuous boundary will be discussed in next section. For both control schemes, less D_{st} results in less voltage stress on the switches, thus the right-hand side boundary is more preferred in both control schemes.

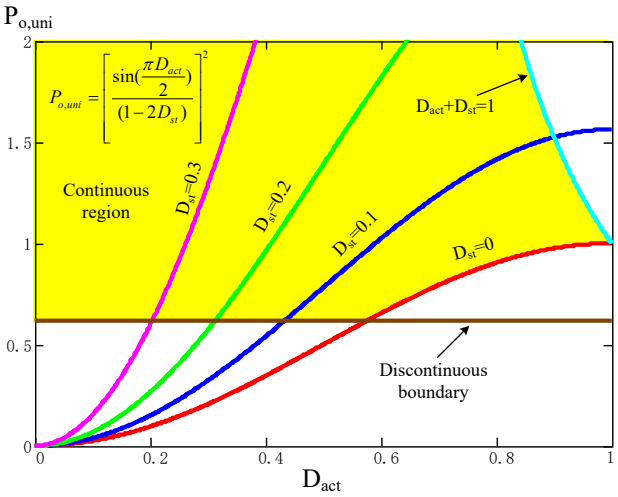


Figure 4. 9 Unified power curves for phase shift control

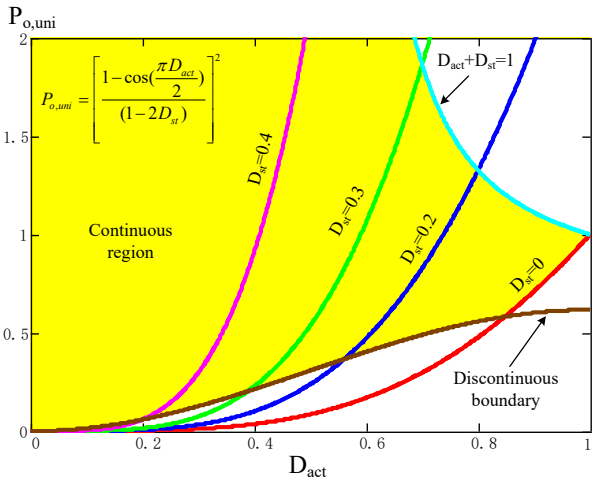


Figure 4. 10 Unified power curves for pulse notch control

4.2.4 Boundary of discontinuous mode

Discontinuous mode happens when the load current reaches twice ZSN inductor current limitation. In this section, the boundary of discontinuous mode will be developed and the working state in discontinuous mode will be analyzed next.

In order to get the peak value of load current, P_H in (4-27) is revised as

$$P_H = \frac{2}{T_s}\int_{\frac{T_s}{4}-\frac{T_{act}}{4}}^{\frac{T_s}{4}+\frac{T_{act}}{4}} V_z \hat{i}_{rp} \sin(\omega_s \tau) d\tau \,, \tag{4-30}$$

and

$$P_H = \frac{4}{T_s}\int_0^{\frac{T_{act}}{4}} V_z \hat{i}_{rp} \sin(\omega_s \tau) d\tau \ . \tag{4-31}$$

The variable $\hat{i}_{rp}$ is the peak value of the load current. In phase shift control, the converter enters discontinuous mode when $\hat{i}_{rp}$ reaches $2I_L$ as Figure 4. 5 shows. In contrast, for pulse notch control, the converter enters discontinuous mode when $\hat{i}_{rp}\sin(\pi D_{act}/2)$ reaches $2I_L$ as Figure 4. 6 shows. Further developing (4-30) and (4-31), we have

$$\hat{i}_{rp} = \frac{P_H}{V_{in}} \cdot \frac{\pi(1-2D_{st})}{2\sin(\pi D_{act}/2)}, \tag{4-32}$$

and

$$\hat{i}_{rp}\sin(\pi D_{act}/2) = \frac{P_H}{V_{in}} \cdot \frac{\pi(1-2D_{st})\sin(\pi D_{act}/2)}{2\left[1-\cos(\pi D_{act}/2)\right]} \ . \tag{4-33}$$

The ZSN inductor current is the same as input current [4], assuming no loss in the ZSN. One has

$$I_L = P_{in}/V_{in} = P_H/V_{in} \ . \tag{4-34}$$

From (4-32), (4-33) and (4-34), we can derive the relationship between D_{st} and D_{act} when the load current reaches $2I_L$. This relationship is plotted in terms of unified power in Figure 4. 9 and Figure 4. 10. The discontinuous boundary is flat in phase shift control while it declines in pulse notch control. If the converter is always working in continuous region, pulse notch control has the ability to regulate the load down to zero theoretically. However, due to the complexity of controlling D_{st} in the downward curve for pulse notch control, discontinuous mode is unavoidable at light load conditions.

4.2.5 Power correction in discontinuous mode

In discontinuous mode, the load current i_{rp} is clamp at $2I_L$. The input diode is off and an equivalent circuit is shown in Figure 4. 11. The impedance of the resonant network is much smaller (at least ten times smaller) than the ZSN impedance, thus the voltage drop on resonant network (V_z) is almost zero. At the same time, the ZSN inductor's current is charging the ZSN capacitor, which is exactly the same as shoot-through state. The only difference is that the shoot-through current is bypassed by the switch or it flows through the resonant network. Discontinuous mode will decrease the active state duty cycle which affects the output power.

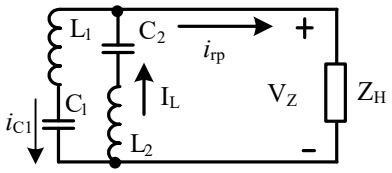


Figure 4. 11 Equivalent circuit in output voltage discontinuous mode

When the discontinuous mode happens, the resonant current is clamped as $2I_L$ and part of the active state is lost. Figure 4. 12 shows an example of pulse notch control in discontinuous mode. The zero notches are from t_2 to t_3 and t_7 to t_8 in Figure 4. 12, but part of the active state is eaten by shoot-through state in discontinuous mode. The actual active state duty cycle is defined as $D_{0,act}$, and the command of active state duty cycle is still D_{act}.

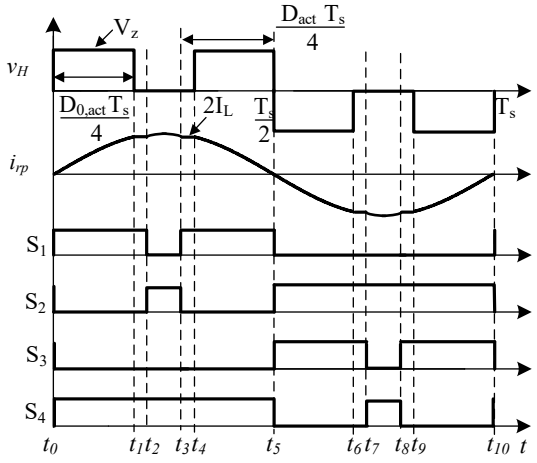


Figure 4. 12 Time domain waveforms in discontinuous mode for pulse notch control

The fundamental component of v_H is

$$v_{H,1} = \frac{4\sqrt{2}}{T_s}\int_0^{\frac{T_{act}}{4}} V_z \sin(\omega_s \tau) d\tau = \frac{2\sqrt{2}V_z}{\pi}\left[1-\cos(\frac{\pi D_{0,act}}{2})\right]. \tag{4-35}$$

The DC output voltage V_z is determined by average shoot-through duty cycle as

$$V_z = \frac{V_{in}}{1-2D_{st}} = \frac{V_{in}}{1-2\cdot(D_{act}-D_{0,act})}. \tag{4-36}$$

From (4-35) and (4-36), we have the unified power expression as

$$P_{o,uni} = \left[\frac{1-\cos(\frac{\pi D_{0,act}}{2})}{(1-2D_{act}+2D_{0,act})}\right]^2. \tag{4-37}$$

$D_{0,act}$ is a variable that depends on D_{act}, and their relationship can be derived when $\hat{i}_{rp}\sin(\frac{\pi D_{0,act}}{2})$ reaches $2I_L$ as Figure 4. 12 shows. We have

$$\frac{\pi(1-2D_{act}+2D_{0,act})\sin(\frac{\pi D_{0,act}}{2})}{2\left[1-\cos(\frac{\pi D_{0,act}}{2})\right]} = 2. \tag{4-38}$$

However, formula (4-38) is a transcendental equation and it can only be solved by numerical calculation. This discontinuous unified power curve is plotted in Figure 4. 13. The load can be regulated all the way down to zero as the black dash curve shows.

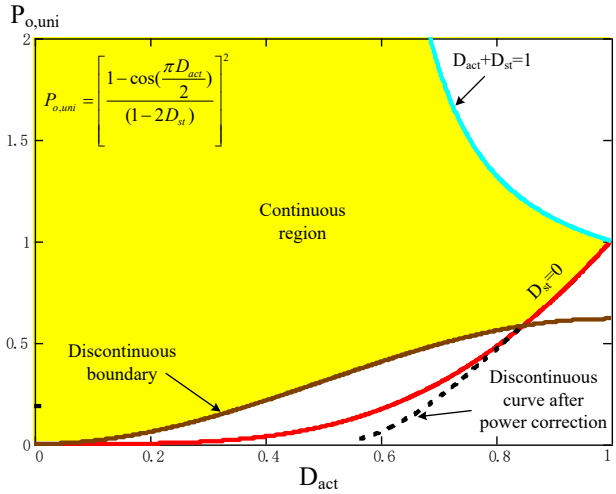


Figure 4. 13 Unified power curves for pulse notch control with power correction

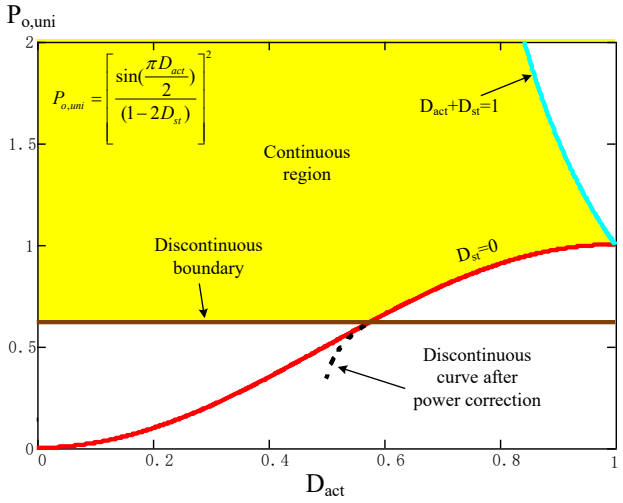


Figure 4. 14 Unified power curves for phase shift control with power correction

Following the same procedure, the power correction for phase shift control is calculated and plotted in Figure 4. 14. However, its transcendental equation only has solution when D_{act} is larger than 0.5. This means phase shift control cannot regulate the load down to zero, or the output voltage v_H is no longer a quasi-square waveform. To control the output power in continuous mode,

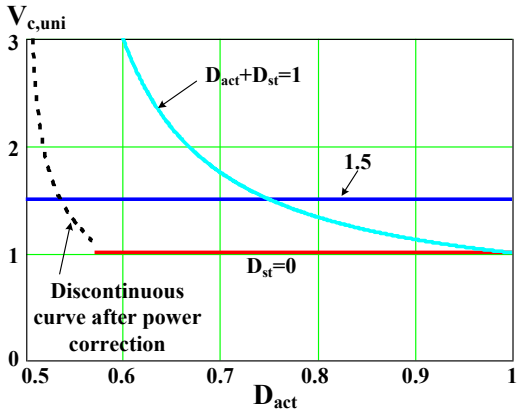
one can follow the equation (4-28) and (4-29). However, there is no mathematical expression for discontinuous mode. An output power look-up table should be made off-line as the dash line shows in Figure 4. 13 and Figure 4. 14. By searching the lookup table, the controller can give the actual command (D_{act}) according to the power required.

4.2.6 Power loss in ZSRC

Different from traditional SRC system, ZSN brings an extra shoot-through state to the H-bridge. The shoot-through state will affect both switching loss and conduction loss for the switches, especially when the ZSRC is doing hard switching.

A. Switching loss for H-bridge

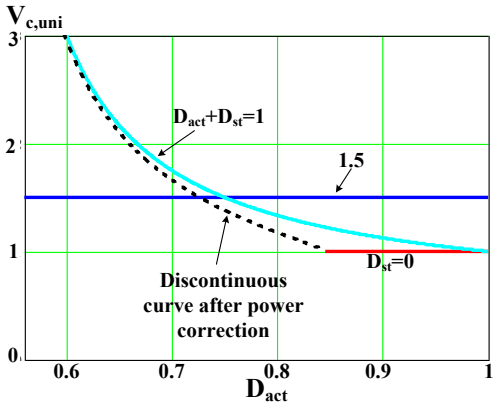
Both control schemes experience hard switching between different states. The switching loss depends on the voltage stress and current stress at the switching moment. For ZSRC, the voltage stress for the H-bridge is constant ($2V_c$-V_{DC}) over one switching cycle and only related to shoot-through duty cycle.



(a) Phase shift control (corresponding to Figure 4. 14)

Figure 4. 15 Unified Z-source capacitor voltage curves for different loads

Figure 4. 15 (cont'd)



(b) Pulse notch control (corresponding to Figure 4. 13)

A unified Z-source capacitor voltage ($V_{c,uni}$) curve for both control methods are shown in Figure 4. 15. The base is V_{DC}. $V_{c,uni}$ increases a lot with either heavy load in light blue curve or light load in dash line. It is also reported [5] that Z-source inverter has advantage over boost converter plus inverter with boost ratio lower than 2, which is 1.5 for Z-source capacitor. To avoid high voltage stress on the device, ZSRC should be designed in the region lower than 1.5 in Figure 4. 15 for most load conditions.

On the other hand, the current stress for switching action depends on the instantaneous current value and the switching between specific states. Table I shows the instantaneous current difference expressions between different states during the switching action.

For both control methods, the upward section (larger than 1) on power curve only has active state and shoot-through state. The switching action takes place at the peak of i_{rp} for pulse notch control, while i_{rp} is zero for phase shift control. Therefore, pulse notch control has soft switching at the region slightly larger than 1 unit power.

When the shoot-through duty cycle is zero, the ZSRC is reduced to a traditional SRC. As the active state duty cycle decreases from 1, phase shift control has soft switching while pulse notch control experiences hard switching at peak current.

As the load further decreases, both control schemes enter discontinuous mode. Phase shift control still has the same situation as above, since the discontinuous behavior happens in the middle of active state without any switching action. However, for pulse notch control, the discontinuous mode appears at the edge of active state and results in the switching action between shoot-through state and zero state. This is the worst case in Table 4. 1, which is a drawback of pulse notch control.

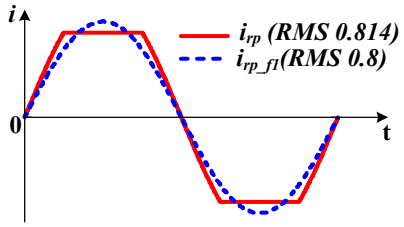
Table 4. 1 The instantaneous current difference between different states

	Active state	Zero state	Shoot-through state
Active state	0	$\hat{i}_{rp}\lvert\sin(\theta)\rvert$	$2I_L-\hat{i}_{rp}\lvert\sin(\theta)\rvert$
Zero state	$\hat{i}_{rp}\lvert\sin(\theta)\rvert$	0	$2I_L$
Shoot-through state	$2I_L-\hat{i}_{rp}\lvert\sin(\theta)\rvert$	$2I_L$	0

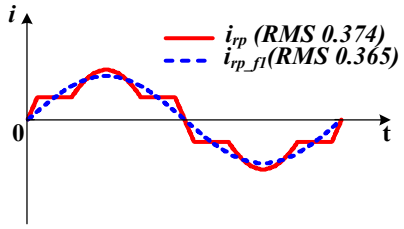
B. Conduction loss for the resonant network

As the simplified circuit in Figure 4. 8 shows, the Z-source network does not affect the resonant network characteristic. The output of H-bridge can still be modeled as a voltage source. With this voltage source, the resonant current only relates to the resonant network and the load. Therefore, the conduction loss caused by the primary side resonant current i_{rp} is the same as traditional H-bridge SRC system in continuous mode. As there is distortion of i_{rp} in discontinuous mode, the RMS value of i_{rp} may change and induce more conduction loss on H-bridge and winding.

Figure 4. 16 shows the distorted i_{rp} in deep discontinuous mode for both control methods. The fundamental component (i_{rp_f1}) of i_{rp} carries the power to the secondary side, while other harmonics circulate in primary side and cause extra conduction loss. One can observe that even in deepest discontinuous mode, the RMS values for i_{rp} are 1.8% (phase shift control) and 2.5% (pulse notch control) higher than that of i_{rp_f1}. Hence, the distortion in discontinuous mode has limited effect on the conduction loss. For simplification, this distortion is not considered into any theoretical calculation.



(a) Phase shift control with D_{act}=0.5



(b) Pulse notch control with D_{act}=0.56

Figure 4. 16 Primary side resonant current i_{rp} in deep discontinuous mode

C. Conduction loss for H-bridge

As Table 4. 1 shows, the ZSRC switches will carry extra shoot-through current ($2I_L$) compared to that of traditional SRC. The switch current's RMS value is the integration of i_{s3} from Figure 4. 5 and Figure 4. 6 respectively, and its expression is

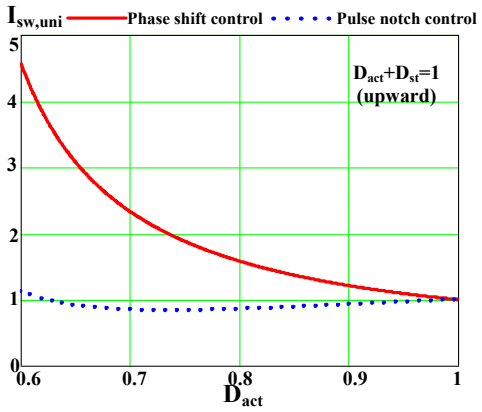
$$i_{s3,RMS}(D_{st}, D_{act}) = \sqrt{(1/T_s)\int_0^{T_s} i_{s3}(D_{st}, D_{act}, t)^2 dt} \quad . \tag{4-39}$$

This switch current's RMS value is converted to a unified value ($I_{sw,uni}$) with the resonant current's fundamental component as the base. One has

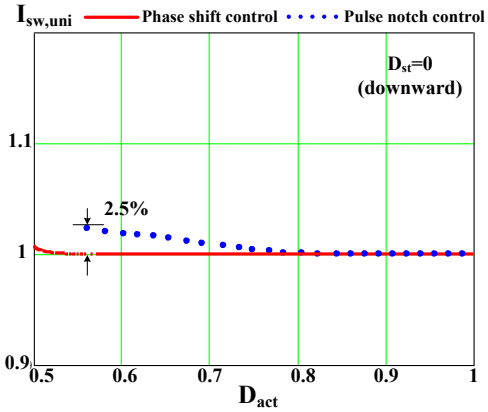
$$I_{sw,uni} = \frac{i_{s3,RMS}(D_{st}, D_{act})}{\sqrt{(1/T_s)\int_0^{\frac{T_s}{2}} i_{rp\_f1}(D_{st}, D_{act})^2 dt}}. \tag{4-40}$$

As each switch in one phase leg conducts 50% of time, the base current only considers the integration of half cycle in (4-40). Figure 4. 17 shows the unified switch current curves for different loads corresponding to Figure 4. 16. In Figure 4. 17(a), the shoot-through state is dominating and leads to extra loss for phase shift control. That is because the shoot-through state happens at the absolute minimum point of the resonant current. In contrast, the shoot-through notch locates at the absolute maximum point of the resonant current, such that the extra current stress is limited. Also, pulse notch control allows all four switches to turn on and share the shoot-through current, which further helps with the conduction loss. As Figure 4. 17(a) shows, the $I_{sw,uni}$ of pulse notch control even has values less than 1, and this implies it has less conduction loss with ZSN compared to the traditional SRC.

Figure 4. 17(b) shows the unified switch current curves for the power less than $P_{H,uni}$ (downward). In continuous mode, the H-bridge actually is a current chopper. As the switch action is symmetric, the current's RMS value is the same as one unit. When ZSRC enters discontinuous mode, there is current distortion as described above. However, each phase leg still behaves as a current chopper and there is limited RMS increment from the distorted current in deep discontinuous mode.



(a) For power curve larger than unit power (upward)



(b) For power curve smaller than unit power (downward)

Figure 4. 17 Unified switch current curves for different loads corresponding to Figure 4. 16

Since the input diode is SiC device, it has negligible switching loss. Its conduction loss depends on the RMS value of input current and is almost irrelevant to control schemes.

4.3 Experimental results

The analysis and design guidelines of the proposed ZSRC system are verified based on a 200 W scale-down prototype, whose parameters are summarized in Table 4. 2.

Table 4. 2 Prototype parameters and values

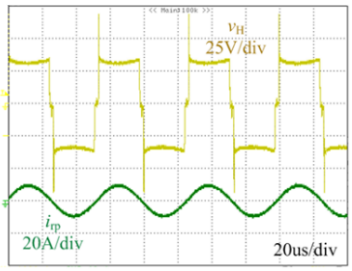
Parameters	Value	Parameters	Value
Input voltage (V_{dc})	33 V	Primary side compensating capacitor (C_p)	180 nF
Output	88 V / 2.28 A	Primary side leakage inductance (L_{kp})	0.415 mH
Resonant frequency	18.2 kHz	Magnetizing inductance (L_M)	61.87 μH
Transformer turns ratio	15:20	Secondary side leakage inductance (L_{ks})	1.07 mH
ZSN capacitors (C_1, C_2)	4.7 mF	Secondary side compensating capacitor (C_s)	65.8 nF
ZSN inductors (L_1, L_2)	1 mH	Output filter capacitor (C_o)	1 mF
H-bridge	6MBP100VEA120	Output rectifier	15ETH03PBF
Input diode (SiC)	GHXS020A060S		

The full bridge output voltage v_H and primary side resonant current i_{rp} for both control methods are shown in Figure 4. 18. The ZSRC is working at full load, half load and 1/4 load with constant output voltage. Full load is set at a point larger than $P_{H,uni}$. At full load in Figure 4. 18(a) and Figure 4. 18(b), we can observe that the DC bus voltage V_z is higher in pulse notch control compared to phase shift control. That is because the power curve for phase shift control is steeper than pulse notch control when regulating the power upward. Pulse notch control needs more shoot-through duty cycle to maintain the same output power as phase shift control does. In terms of voltage stress on the switches, phase shift control is better in the region larger than $P_{H,uni}$.

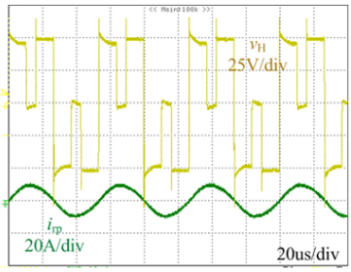
At half load in Figure 4. 18(c) and Figure 4. 18(d), both control methods show similar performance in the light discontinuous mode. Phase shift control would have extra shoot-through state in the middle of active state. The extra shoot-through state in pulse notch control merge with zero state, such that one cannot tell the difference in v_H.

As the load further decrease as Figure 4. 18(e) and Figure 4. 18(f) show, phase shift control has a very high voltage spike around 125 V while the pulse notch control only has a peak voltage value around 60 V. For theoretical analysis, there is no solution for phase shift control's transcendental equation at light load in Figure 4. 14, which means the waveform of phase shift

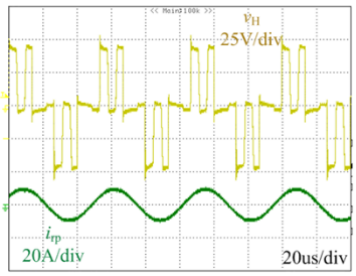
control has huge distortion and is uncontrollable. Drawing power under such a condition results in high voltage spike. On the other hand, pulse notch control maintains quite good quality waveforms as expected.



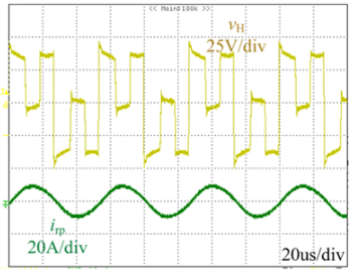
(a) Full load, phase shift control command D_{act}=0.9, D_{st}=0.1



(b) Full load, pulse notch control command D_{act}=0.78, D_{st}=0.22



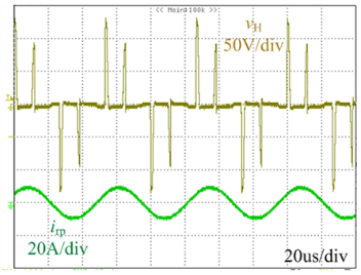
(c) Half load, phase shift control command D_{act}=0.53, D_{st}=0



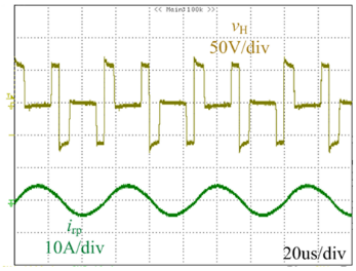
(d) Half load, pulse notch control command D_{act}=0.79, D_{st}=0

Figure 4. 18 Experimental waveforms of v_H and i_{rp} (V_o=88 V, full load @R_L=40 Ohm, half load @ R_L=80 Ohm and 1/4 load @R_L=160 Ohm)

Figure 4. 18 (cont'd)



(e) 1/4 load, phase shift control command D_{act}=0.47, D_{st}=0



(f) 1/4 load, pulse notch control command D_{act}=0.66, D_{st}=0

Figure 4. 19 shows the unified power curve for both control methods. Expermental results match with calculation very well for pusle notch control as there is almost no distortion in deep discontinuous mode. For phase shift control, it is predictable with continuous mode below $P_{H,uni}$ and light discontinuous mode. As the upward power curve for phase shift control is steep when regulating the power upward, a small error in control command would be amplified. Gate signal delay difference between different switches or the turn-on and turn-off transient may cause the partial loss in shoot-through state duty cycle. These are the problems phase shift control has, while pulse notch control matches theoretical analysis quite well.

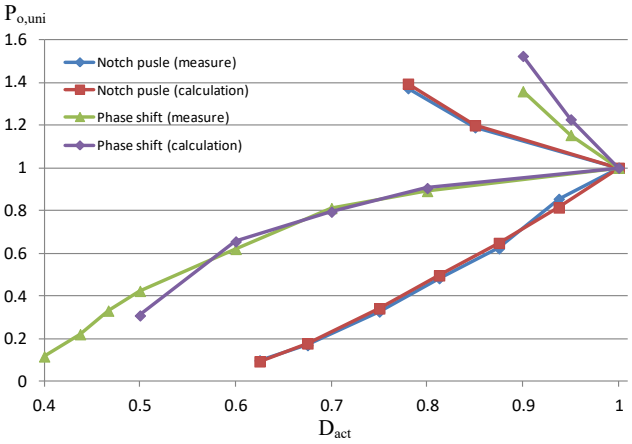


Figure 4. 19 Experimental unit power curve (R_L=40 Ohm, open loop, unit power=150 W)

4.4 Summary

This chapter focus on the load regulation methods in SiC based Z-source resonant converter for wireless power transfer application. Two constant frequency control methods—phase shift control and pulse notch control are presented with comparison on load regulation performance. Phase shift control is easier in implementation but it suffers from high distortion at light load in discontinuous mode. On the other hand, pulse notch control is more predictable than phase shift control over the entire load range. However, both control methods are doing hard switching, which is a drawback for ZSRC. Fortunately, it does not have much switching loss since the switching frequency is less than 20 kHz in this IPT application. Experimental results based on a 200-W scale-down prototype with ZSRC are presented.

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REFERENCES

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CHAPTER 5 Z-source Resonant Wireless Charger: Power Factor Correction

In single-phase PFC applications, there is double line-frequency power (2ω ripple power) circulating in the system, which needs energy storage component for absorption. In the ZSRC, large capacitance in ZSN would help the stability, thus it is possible to utilize the ZSN capacitor to absorb the 2ω ripple power. In [1], an idea that controlling the 2ω ripple power directly to follow the power reference is proposed and it successfully decouples 2ω ripple power from DC line. Similar concept can be applied to the ZSRC.

On the other hand, sinusoidal charging, which allows the double line-frequency ripple to propagate to the output, is another solution aiming at reducing the bulky capacitors. Recently, a comparison of low frequency (120 Hz) sinusoidal charging and DC charging shows negligible impact on Li-ion batteries' performance. Therefore, the ZSRC's capacitor, the biggest component, can be reduced dramatically from millifarad to several microfarads with sinusoidal charging technique, which features the ZSRC high power density. Also, it keeps the Z-source's benefit of boost ability and being immune to shoot-through problems.

In this chapter, a conventional PFC control scheme is exercised. The sinusoidal charging behavior for the ZSRC is modeled, and a control scheme that has both PFC function and load regulation for sinusoidal charging is presented.

5.1 Conventional power factor correction for ZSRC

In previous chapter, pulse notch control shows the ability of regulating the output power down to zero in discontinuous mode. This is an essential feature for power factor correction as the AC transient varies to zero every line-frequency cycle. Figure 5. 1 shows the unified power curves for pulse notch control analyzed from previous chapter as a lookup table for the PFC control schemes in this chapter.

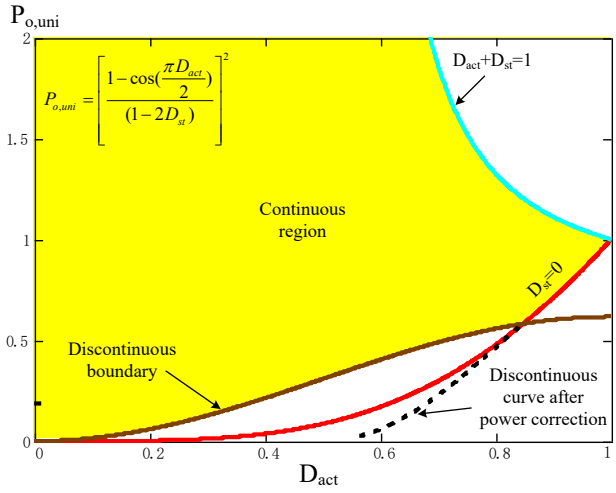


Figure 5. 1 Unified power curves for pulse notch control with power correction

5.1.1 PFC implementation

Figure 5. 2 shows the concept of this 2ω ripple power rejected control. Initially, in the ZSRC DC/DC application, a constant duty cycle can output a constant power as shown in Figure 5. 1. Considering that the input side is perturbed with 2ω ripple power, the 2ω ripple power would propagate to the output side. In order to reject this perturbation from output side and absorb it in the ZSN, a negative 2ω ripple power reference is injected into the control reference. The control reference can be calculated by only sensing the AC input voltage, and one has

$$P_{ref} = k_p(1-\frac{|v_{ac}|^2}{v_{ac\_\max}^2}) . \quad (5\text{-}1)$$

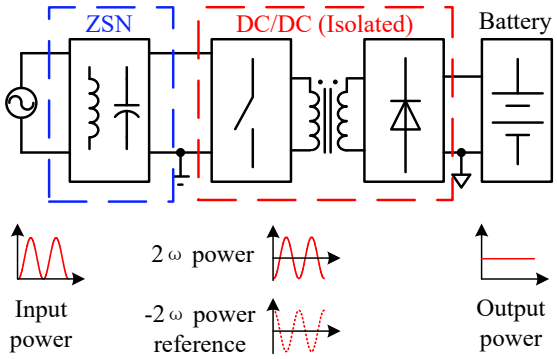


Figure 5. 2 Illustration of 2ω ripple power rejected control

The parameter k_p controls the output power. Once we have the power reference P_{ref}, the actual control command (D_{act}) can be located in a look-up table based on Figure 5. 2. To fully compensate the 2ω ripple power, P_{ref} needs to go down to zero and only the pulse notch control has the ability to do so. However, such control scheme only holds true when all the working points are in discontinuous mode. The mix operation with both continuous and discontinuous mode will result in surge current from input source to ZSN capacitors, as the AC peak input voltage exceeds ZSN capacitor voltage.

5.1.2 Light load limitation

In steady state, the output power is pure DC ideally. The active state duty cycle that is directly related to the output power is irrelevant to the 2ω ripple perturbation. Table 5. 1 shows the duty cycle in each state and the corresponding current to the ZSN capacitors. The 2ω ripple perturbation is ΔD in zero state. As the total duty cycle should be 1, the response of the perturbation can only be found in shoot-through state (-ΔD). As shown in the third column, the net current in one line-frequency cycle that the perturbation contributes to the ZSN capacitors is zero, and the system is stable. However, when the load goes up, the ZSRC is partially operating in continuous mode, where the shoot-through state duty cycle is zero. The perturbation ΔD affects the active state duty cycle and the net current balance in one line-frequency cycle is broken.

Table 5. 1 2ω ripple perturbation in duty cycle and capacitors voltage balance

	Duty cycle	Current to the ZSN capacitors
Active state	D_{act0}	I_L-i_{rp}
Shoot-through state	D_{act}-D_{act0}- ΔD	-I_L
Zero state	1-D_{act}+ ΔD	I_L

5.2 Line-frequency sinusoidal charging for ZSRC

Different from the conventional PFC methods, sinusoidal charging allows the 2ω ripple to the output and eliminates the bulky energy storage component in the Z-source network. This section gives the modeling of sinusoidal charging, examples of control schemes and the calculation of passive components.

5.2.1 Modeling of sinusoidal charging

In PFC application, the source is usually a voltage source from the grid. To achieve unity PF, one can directly control the input current to follow the input voltage simultaneously. The other way is to control the input power such that the current matches automatically. The equations for these two approaches are derived below.

A. Input current approach

The DC characteristic of the ZSRC can be found in detail in [2]. The secondary side rectifier can be modeled as an AC resistor (R_{ac}) by fundamental harmonic approximation (FHA) as shown in Figure 5. 3. Assuming all the power is carried by fundamental component, the expression of R_{ac} is

$$R_{ac} = \frac{v_{D(1)}}{i_{rs}} = \frac{V_o^2}{P_o}, \tag{5-2}$$

where $v_{D(1)}$ is the fundamental component of v_D. For conventional DC charging, the output power P_o is constant. However, in sinusoidal charging, the output power follows the input power simultaneously, and battery voltage V_o is constant. Therefore, R_{ac} is changing over one line-frequency period. The expression of R_{ac} is revised to

$$R_{ac}(t) = \frac{V_o^2}{P_{o\_peak}\left|\sin(120\pi t)\right|^2} = \frac{R_{ac\_peak}}{\left|\sin(120\pi t)\right|^2}. \tag{5-3}$$

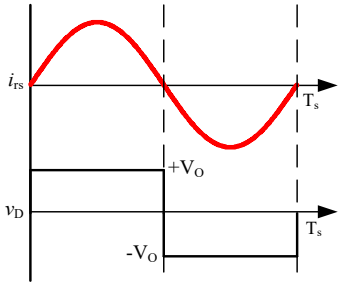


Figure 5. 3 Secondary side waveform in one switching period

The WPT system can be simplified as one voltage source v_H and a resonant network with all the parameters reflected to primary side as Figure 5. 4 shows. The voltage source v_H is the output of H-bridge and v_H contains different frequency components. Z_p and Z_s are primary side impedance and secondary side impedance respectively. Z_o represents the output impedance. N is the turn ratio. The impedance from the output terminals of H-bridge is Z_H. Also, at resonant frequency ω_0, with certain compensation [6], the impedance Z_H is purely resistive (R_H). According to [2], the input current of traditional phase shift control is

$$i_{in} = \left[\frac{2\sqrt{2}v_{in}}{\pi(1-2D_{st})}\sin(\frac{\pi D_{act}}{2})\right] / R_H, \tag{5-4}$$

where,

$$R_H = Z_H(\omega_0) = R_p + \frac{(\omega_0 L_M)^2}{(R_{ac}+R_s)/N^2} \approx \frac{(N\omega_0 L_M)^2}{R_{ac}}. \tag{5-5}$$

Considering R_{ac} is no longer a constant, i_{in} can be derived by inserting (5-3) & (5-5) into (5-4) as

$$i_{in}(t)=\frac{v_{in}(t)\cdot\sin(\pi D_{act}(t)/2)}{\left[1-2D_{st}(t)\right]\left|\sin(120\pi t)\right|^2}\frac{2\sqrt{2}R_{ac\_peak}}{\pi\left(N\omega_0 L_M\right)^2}. \tag{5-6}$$

For the ideal unity PF case, $i_{in}(t)$ should follows $v_{in}(t)$ and the rest of the terms in (5-6) should be constant. The PFC control scheme is illustrated in next section.

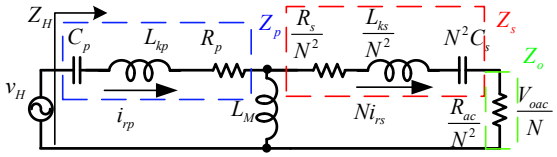


Figure 5. 4 A simplified circuit of the resonant network

B. Input power approach

Similar to the input current approach, assuming a lossless system, the input power expression in [2] should be modified with a time varying R_{ac}. For phase-shift control, we have

$$P_{in}(t)=\left[\frac{2\sqrt{2}v_{in}}{\pi(1-2D_{st}(t))}\sin(\frac{\pi D_{act}(t)}{2})\right]^2\frac{R_{ac\_peak}}{\left(N\omega_0 L_M\right)^2\left|\sin(120\pi t)\right|^2}. \tag{5-7}$$

Adopting the per-unit concept in [2], a unit-power variable $P_{o,uni}$ is introduced for (5-7) as

$$P_{o,uni}(t)=\left[\frac{\sin(\pi D_{act}(t)/2)}{(1-2D_{st}(t))}\right]^2. \tag{5-8}$$

Then equation (5-7) can be reduced to

$$P_{in}(t)=\frac{8v_{in\_peak}^2R_{ac\_peak}}{\left(\pi N\omega_0 L_M\right)^2}\cdot P_{o,uni}(t). \tag{5-9}$$

It is worth emphasizing that equation (5-9) is a general expression regardless of specific control scheme. The two control methods, phase-shift control and pulse notch control in [2], differs in unit-power $P_{o,uni}$ expression. Even for one control method, continuous mode and discontinuous

mode have different $P_{o,uni}$ expressions. However, all of these cases can be unified to (5-9) with specific $P_{o,uni}$ functions. Moreover, $P_{o,uni}$ is not related to any input or output information. Therefore, $P_{o,uni}$ can be calculated off-line and stored into one lookup table. This allows us to apply and test different control methods rapidly by updating just one lookup table.

C. Secondary side power discontinuous phenomenon

The modeling of secondary side in Figure 5. 3 is an ideal case. The diode bridge input voltage v_D changes with a limited slope as Figure 5. 5 shows (ignoring harmonics). With strong excitation from primary side, v_D is clamped at output voltage most of the time in one period while delivering power to output capacitor C_o. As the excitation intensity decreases to medium, the on-time of the diode bridge reduces with less output power. Further, light excitation as shown in Figure 5. 5 even cannot drive the diode bridge; therefore, no power is flowing between the resonant circuit and the output capacitor. At this power discontinuous point, an equivalent circuit of the resonant network is shown in Figure 5. 6. As there is no current flowing through Z_s, there is no voltage drop on Z_s and the peak voltage on magnetizing inductor L_m is DC output voltage V_o over N at discontinuous mode boundary. The fundamental component of v_D is marked as $v_{D(1)}$, and $v_{D(1)}$'s peak value is $4V_o/\pi$ where v_D is a square wave at full load.

Based on this boundary value, one can predict when the ZSRC enters this power discontinuous mode at DC steady state. However, in PFC application, the power is time varying and the resonant network serves as an energy buffer. The true boundary point in one line cycle has minor error if determined only by this DC method as the time constant for this energy buffer is closed to line frequency and the AC transient exists every line cycle. Another explanation is that the resonant network is compensated to be pure resistive at resonant frequency. However, the resonant network is capacitive at line frequency. The DC method only holds true for resistive case.

For example, when the AC input voltage is rising from zero, the resonant network needs some time to be charged to the boundary point; and when the AC input voltage is decreasing from the peak, the resonant network can still provide power to the output for some time even without sufficient input voltage. In power discontinuous mode, the resonant network continuous draws some amount of current from the input to support its conduction loss. This input current is called "tail current". On one hand, this tail current helps improving power factor by increasing the fire angle. On the other hand, it is uncontrollable as it depends on the system's efficiency. More detail discussion of its effect on PFC would be presented in next section.

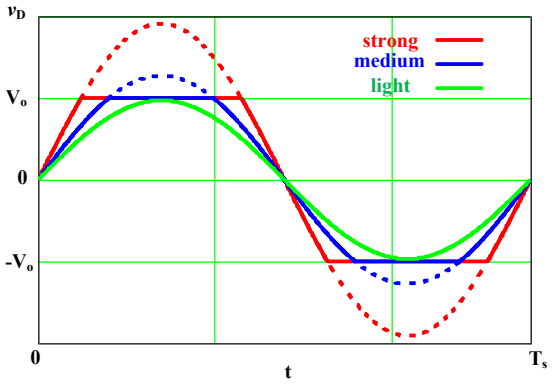


Figure 5. 5 Secondary side waveform in one switching period with different excitations

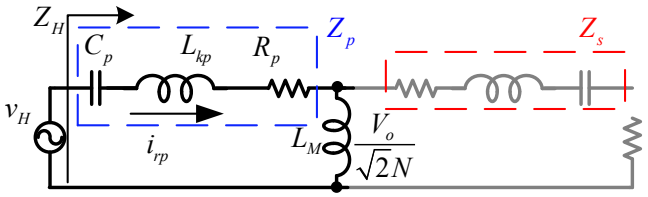


Figure 5. 6 A simplified circuit of the resonant network at power discontinuous mode

5.2.2 PFC control schemes for sinusoidal charging

In the ZSRC, there are two control freedoms, which are active state duty cycle (D_{act}) and shoot-through state duty cycle (D_{st}). For the input current approach, these two control freedoms are independent, with the only constrain that the sum of them should be less than 1. On the other hand, D_{act} and D_{st} are dependent in the input power approach, as there is only one variable, input

power, in the equation (5-9). In this section, two specific control schemes are picked up from each approach to illustrate the implementation of the two approaches.

A. Input current control

One easy way of control freedoms distribution is to do load regulation with D_{act} and to achieve PFC function by controlling D_{st}. As shown in (5-6), the input current is monotonically increasing with D_{act}. Therefore, D_{act} can be used for load regulation and left as a constant over one line period. On the other hand, the denominator of (5-6) also should be a constant to achieve unity power factor, and we have

$$D_{st}(t) = 0.5 - \frac{C}{\left|\sin(120\pi t)\right|^2}, \tag{5-10}$$

where C is a constant. Figure 5. 7 shows D_{st} curve over half line period with different parameter C. Since D_{st} must be above zero, part of the curve losses tracking to the sinusoidal term. Smaller C results in higher D_{st} and higher voltage stress on the switching device, while larger C has less controllable region and more distortion in the input current. It is a tradeoff to determine the constant C.

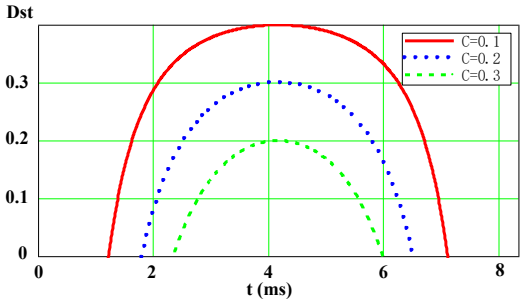


Figure 5. 7 D_{st} in half line period with different constant C

By inserting (5-10) into (5-6), we have the input current expression as

$$i_{in}(t)=\frac{\sqrt{2}v_{in\_peak}\sin(\pi D_{act}/2)R_{ac\_peak}}{C\cdot\pi\left(N\omega_0 L_M\right)^2}\cdot\left|\sin(120\pi t)\right|. \tag{5-11}$$

The first term in (5-11) is constant over one line period and the second term shapes the input current to pure sinusoidal. However, formula (5-11) only hold true when the secondary side is drawing power. When the output rectifier is off, tail current is observed on the input side. Figure 5. 8 shows the input current waveform with different constant C. The conclusion is coordinate with previous discussion, where a smaller C leads to larger D_{st} and larger portion of controllable i_{in}. On the opposite, a larger C results in smaller D_{st} and lower voltage stress on the switch, but the tail current portion is longer in one line period. The boundary of secondary side power discontinuous mode is roughly around the instant that D_{st} goes to zero. That is because shoot-through duty cycle can still pump energy into the resonant network regardless of the reflection of output voltage.

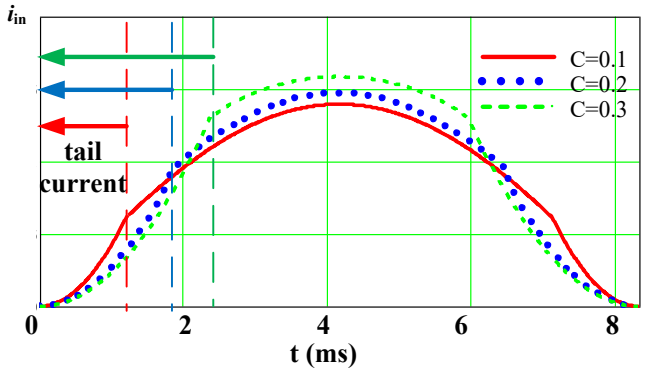


Figure 5. 8 Input current waveform with different constant C

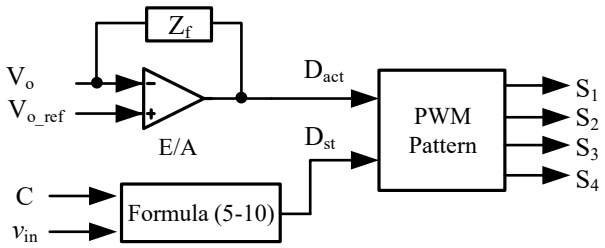


Figure 5. 9 block diagram of input current control

The control block diagram for input current control is shown in Figure 5. 9. Two input signals are needed from the circuit. One is the output voltage indicating the output power.

Impedance Z_f has a bandwidth lower than line frequency. The output of the error amplifier is the D_{act} signal for load regulation. The other input signal is the input voltage. Constant C is pre-determined by the required shape of the input current shown in Figure 5. 8. The output of the formula (5-10) serves as D_{st}. The PWM pattern is required to generate arbitrary D_{act} and D_{st}. In this case, the phase shift control in [2] is adopted as the PWM pattern. The input current control is essentially a feedforward control.

B. Input power control

For input power approach, $P_{o,uni}$ actually is a specific combination of D_{st} and D_{act} which are stored in a look-up table. As mentioned in [2], some control schemes may involve the need of solving transcendental equation, and therefore, there is no expression for online calculation. Here we adopt the pulse notch control in [2] as an example since pulse notch control is able to regulate the power all the way down to zero. From (5-9), the first term is constant and the $P_{o,uni}$ is required to track the double line frequency power ripple all the way down to zero as

$$P_{o,uni}(t) = \left|\sin(120\pi t)\right|^2 . \tag{5-12}$$

Figure 5. 1 from [2] gives a clear image of $P_{o,uni}$ for pulse notch control. The dash line below the discontinuous boundary and the two solid lines above discontinuous boundary are the working points which are stored in a look-up table. The definition of discontinuous boundary is when the current peak in the resonant network reaches twice of the Z-source inductor current. More discussion could be found in [2].

The section below discontinuous boundary (dash line) has shoot-through duty cycle which can pump energy to the resonant network even at low line voltage. As a result, the tail current phenomenon is not that serious as the input current approach.

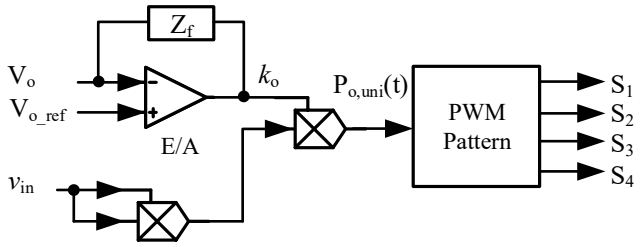
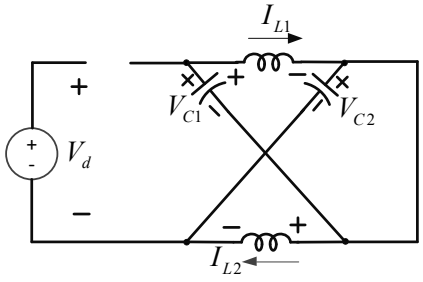


Figure 5. 10 block diagram of input power control

The control block diagram for input power control is shown in Figure 5. 10. Two input signals are needed from the circuit. One is the output voltage indicating the output power. Impedance Z_f has a bandwidth lower than line frequency. The output of the error amplifier is a scaler signal (k_o) for load regulation. The other input signal is the input voltage. The square of input voltage together with the scaler signal contributes to $P_{o,uni}(t)$ which is the sole input of the PWM pattern block. In this case, the pulse notch control in [2] has been adopted as the PWM pattern. The input power control is also essentially a feedforward control.

5.2.3 Z-source network design for sinusoidal charging

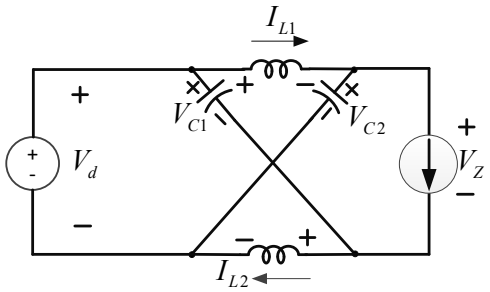
To design the Z source network, we can analyze the circuit by studying it under different operation modes [4] such as shoot-through state and non-shoot-through state as shown in Figure 5. 11.



(a) Shoot-through state

Figure 5. 11 Equivalent circuits of Z-source network

Figure 5. 11 (cont'd)



(b) Non-shoot-through state

The Z source network is symmetrical, therefore, $V_c=V_{c1}=V_{c2}$ and $v_L=v_{L1}=v_{L2}$. From [4] we have

$$V_C = \frac{1-D_{st}}{1-2D_{st}} V_d \,. \tag{5-13}$$

As the phase shift control's shoot-through duty cycle is distributed evenly over one switching cycle [5] as shown in Figure 5. 12, the Z-source inductor's current bounces back and forth four times in one switching cycle.

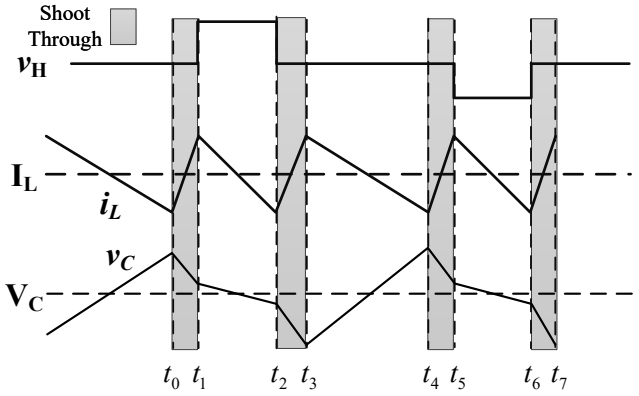


Figure 5. 12 Z-source inductor current and capacitor voltage in one switching period

To find the maximum current ripple on the Z-source inductor, we focus on the shoot-through section from t_0 to t_1. We have

$$L = \frac{V_c \cdot 0.25D_{st} \cdot T_{sw}}{\Delta i} = \frac{1-D_{st}}{(1-2D_{st})} \cdot \frac{V_d \cdot 0.25D_{st}}{\Delta i \cdot f_{sw}}, \tag{5-14}$$

where "$0.25D_{st}$" is used here due to the phase shift control. By choosing the current ripple to be 10 A at AC peak (110 Vac) and D_{st} as 0.2 with the prototype parameters in Table 5. 2, we can derive the inductance to be

$$L = \frac{1-0.2}{(1-2\times 0.2)} \cdot \frac{110\times 1.414\times 0.05}{10\times 18200} H = 57\, uH\ . \tag{5-15}$$

For the Z-source capacitor design, we can follow the same ripple approach. The difference from inductor design is that the capacitor voltage bounces only twice in one switching cycle. Considering the zero state (t_3 to t_4), we have the capacitor current as

$$i_C = i_L = P_{in} / V_d\ . \tag{5-16}$$

And the maximum voltage ripple happens at AC peak (110 V_{ac}) as

$$\Delta V_c = \frac{i_C}{C}\Delta t = \frac{\sqrt{2}P_{in}}{V_Z C} \cdot \frac{0.5D_{zero}}{f_{sw}}, \tag{5-17}$$

where "$0.5D_{zero}$" represent the zero state (t_3 to t_4). To maintain that the ripple is less than 5%, one has

$$\Delta V_C \le 5\% \cdot (\frac{1-D_{st}}{1-2D_{st}}\sqrt{2}V_d)\ . \tag{5-18}$$

By pulping in the parameters from Table 5. 2 into (5-11) with constant C=0.3, we have D_{st}=0.2, D_{act}=0.4 and D_{zero}=0.4. Then the minimum capacitance for 5% ripple would be

$$C \ge \frac{P_{in}}{V_Z^2} \cdot \frac{(1-2D_{st})0.5D_{zero}}{5\%(1-D_{st})f_{sw}}$$

$$= \frac{1000}{110^2} \cdot \frac{(1-2\times 0.2)\times 0.2}{5\%(1-0.2)\times 18200} F = 13.6uF\ . \tag{5-19}$$

In summary, the Z-source inductor is 50 uH and the Z-source capacitor is 20 uF for the experimental prototype. Compared to conventional Z-source inverter [6], the Z-source capacitor is tremendously reduced from 4.7 mF to 20 uF. Moreover, the corresponding Z-source inductor is shrunk from 1 mF to 50 uH as the stability issue at line frequency no longer exists [5].

5.3 Experiment results

The analysis and design guidelines of the proposed ZSRC system are verified on a 1-kW prototype, whose parameters are summarized in Table 5. 2.

Table 5. 2 Prototype parameters and values

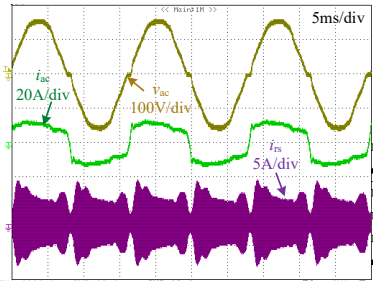
Parameter	Value		Parameter	Value
Input voltage (V_{ac})	115 V		Primary side compensating capacitor (C_p)	164 nF
Output	200 V / 5 A		Primary side leakage inductance (L_{kp})	0.414 mH
Resonant frequency	18.2 kHz		Magnetizing inductance (L_M)	63 μH
Transformer turns ratio	15:20		Secondary side leakage inductance (L_{ks})	1.07 mH
H-bridge	6MBP100VEA120		Secondary side compensating capacitor (C_s)	66 nF
Charging methods	Conventional charging	Sinusoidal charging	Output filter capacitor (C_o)	4.7 mF
ZSN capacitors (C_1, C_2)	4.7 mF	20 uF	Input rectifier (SiC)	GHXS020A060S
ZSN inductors (L_1, L_2)	1 mH	50 uH	Output rectifier	15ETH03PBF

5.3.1 Conventional PFC for the ZSRC

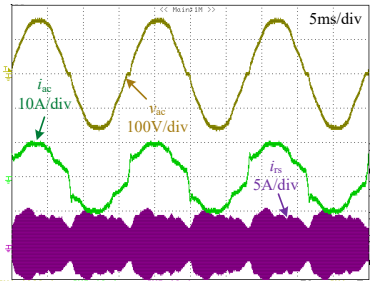
Since the proposed control aims at discontinuous mode, the prototype operates at half load instead of full load in order to enter the discontinuous mode. Figure 5. 13 shows the AC side waveforms for both phase-shift control and pulse notch control. The AC voltage comes from an variac, and therefore it has some crossover distortion. High distortion on the input current is observed in Figure 5. 13(a), and the fluctuation on secondary side current is clearly larger than the other one. More key waveforms for pulse notch control are presented in Figure 5. 14. They match

with the theorectical analysis. From Figure 5. 14(c), the 1.65 V output voltage ripple on 1 mF output capacitance indicates that only 8% of the 2ω ripple power propogates to the output side. This verifies the concept of 2ω ripple power rejected control introduced before.

Figure 5. 15 shows the input current spectrum of these two control schemes. IEC61000-3-2 Class A criterion is transformed from 220 V to 115 V and plotted in Figure 5. 15 as a reference. Phase-shift control barely pass Class A with 29% THD, while pulse notch control has much more margin in harmonics with 14% THD.

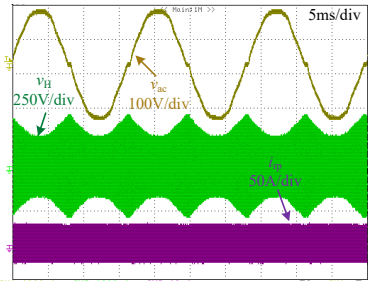


(a) Phase-shift control



(b) Pulse notch control

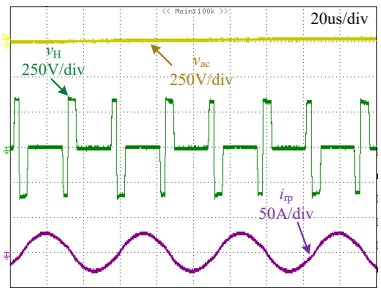
Figure 5. 13 Experimental waveforms of AC side and secondary side current at half load (200 V/500 W)



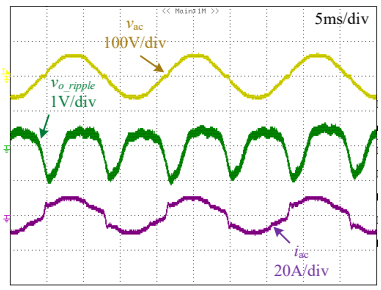
(a) H-bridge output voltage and current

Figure 5. 14 Key experimental waveforms for pulse notch control at half load (200 V/500 W)

Figure 5. 14 (cont'd)



(b) Zoom-in of (a)



(c) Secondary side output voltage ripple

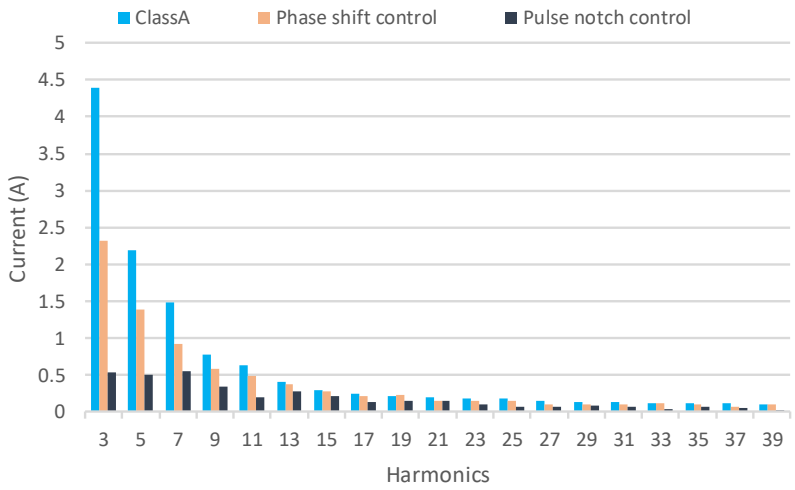


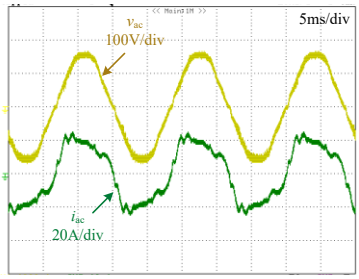
Figure 5. 15 Input current spectrum at half load (200 V/500 W)

5.3.2 Sinusoidal charging for the ZSRC

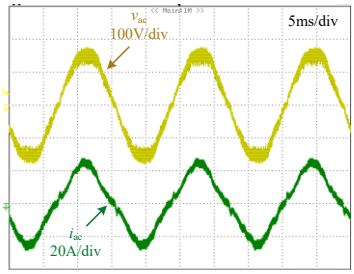
A. Steady state waveforms

Figure 5. 16 shows the AC side waveforms for the proposed input current and input power approaches at full load and half load. Constant duty cycle control was tested as a comparison in

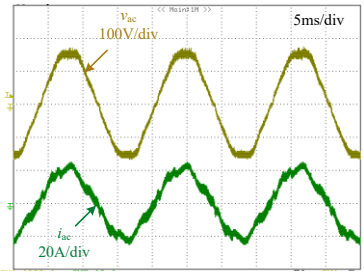
Figure 5. 16(a). The input current of the constant duty cycle control appears to be a square waveform and is full of harmonics. Also, the Z-source network is not active when D_{st}=0, and the ZSRC reduces to normal SRC. If single stage DC-DC converter is directly fed with AC source, the power factor is low. From Figure 5. 16(b) to (e), both of the proposed controls can reshape the input current to be symmetric and less harmonics. In terms of the input current quality, the two proposed controls have similar performance both at full load and half load.



(a) Constant D_{st}=0&D_{act}=0.52, @full load



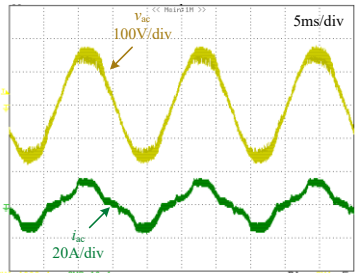
(b) Proposed input current approach, D_{act}=0.39&C=0.3 @full load



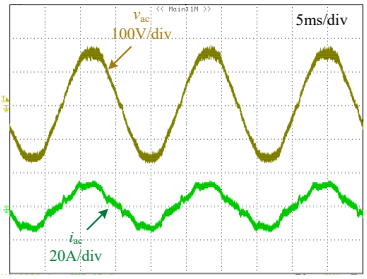
(c) Proposed input power approach, pulse notch control @full load

Figure 5. 16 Experimental waveforms of AC side voltage and current

Figure 5. 16 (cont'd)



(d) Proposed input current approach, D_{act}=0.29&C=0.35 @half load



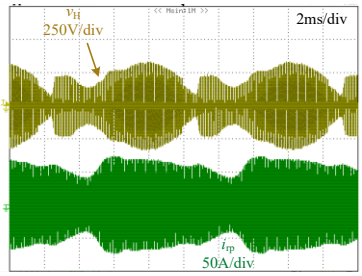
(e) Proposed input power approach, pulse notch control @half load

Figure 5. 17 and Figure 5. 18 show more key waveforms for the two proposed controls at full load. The peak H-bridge voltage v_H is higher in the input current control as the shoot-through duty cycle is allocated only around the AC peak. The input current approach actually is phase shift control in [2], and the voltage stress is high when it enters deep light load, which is the case of low input voltage points around zero crossing. That is the reason why the envelop of v_H in Figure 5. 17(a) bounces up several times in one line period. On the other hand, the example of the input power approach is pulse notch control in [2], and it can regulate the load smoothly all the way down to zero. The envelop of v_H in Figure 5. 18(a) is symmetric and smooth.

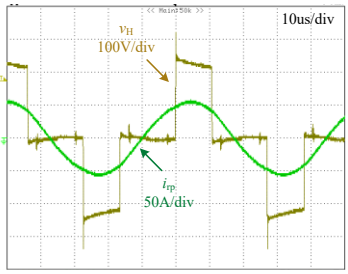
Figure 5. 17(b) and Figure 5. 18(b) show the switching pattern for the two proposed controls which are corresponding to phase shift control and pulse notch control in [2].

Figure 5. 17(c) and Figure 5. 18(c) show the output voltage ripple and secondary side current for both controls. The secondary side rectifier's off time in the first proposed control is

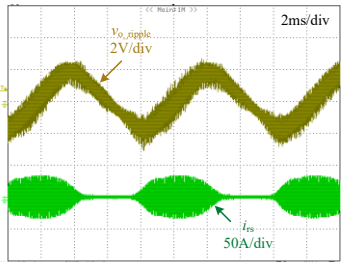
longer than the second one, as the shoot-through duty cycle is allocated all around one line period for the second one.



(a) H-bridge output voltage and current

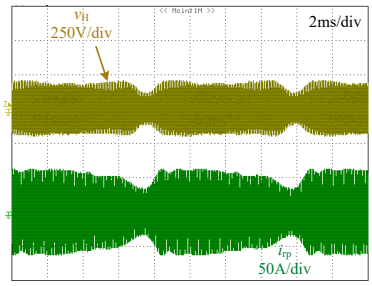


(b) Zoom-in of (a)



(c) Secondary side output voltage ripple

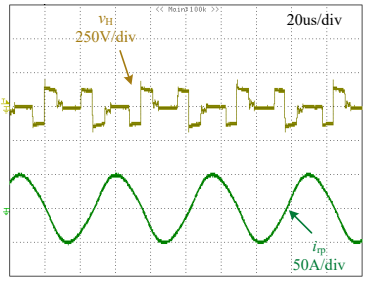
Figure 5. 17 Key experimental waveforms for the proposed input current control (D_{act}=0.39&C=0.3) at full load (200 V/1 kW)



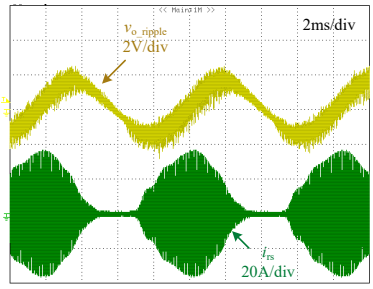
(a) H-bridge output voltage and current

Figure 5. 18 Key experimental waveforms for the proposed input power control at full load (200 V/1 kW)

Figure 5. 18 (cont'd)



(b) Zoom-in of (a)



(c) Secondary side output voltage ripple

Figure 5. 19 shows the input current spectrum of these two control schemes. IEC61000-3-2 Class A criterion is transformed from 220 V to 115 V and plotted in Figure 5. 19 as a reference. Constant duty cycle control fails in the 15th and the 17th harmonics with 23% THD, while the proposed controls pass Class A criterion with 12% THD (input current control) and 10% THD (input power control).

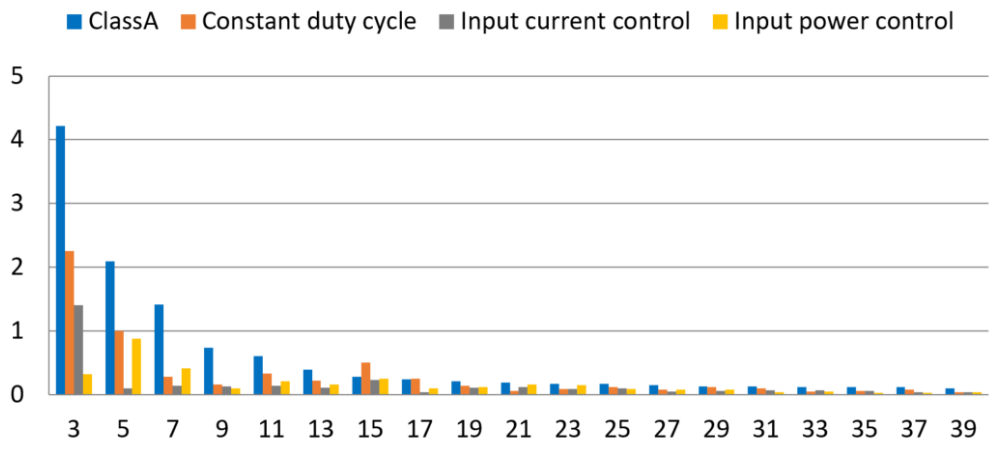


Figure 5. 19 Input current spectrum at full load (200 V/1 kW)

B. Soft startup issue

Soft startup for traditional boost PFC is always an issue and it needs an extra diode to charge the output capacitor before startup. Since there is no bulky energy storage component for sinusoidal charging, the inrush current at startup would be substantially smaller than conventional DC charging. Furthermore, Z-source network can limit the shoot-through current or inrush current inherently. Therefore, the ZSRC does not need any extra hardware or delicate engineering solution for soft startup. However, there are four possible instants in one line period to start up the circuit. It is worth examining all candidates to find the best one.

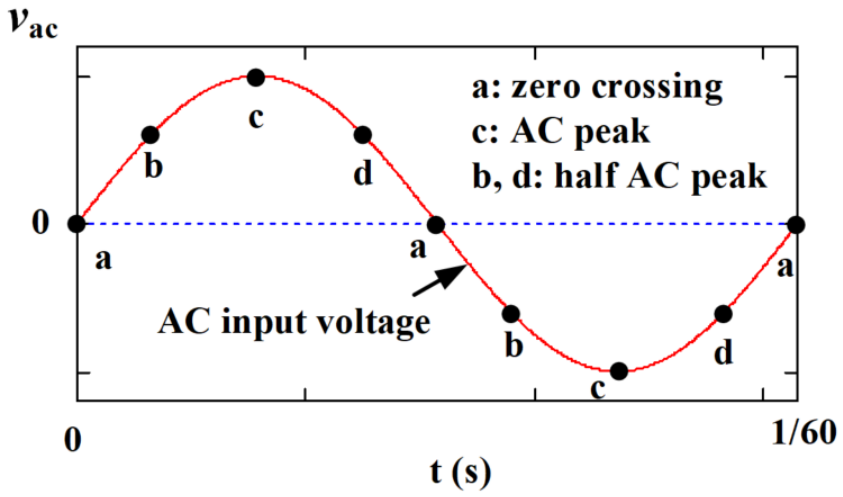
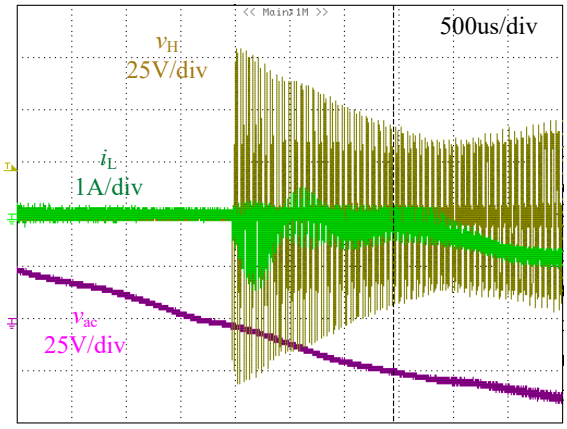


Figure 5. 20 Four candidates of soft startup instant in one line cycle

Before the circuit starts up, the Z-source capacitors are charged to AC peak voltage. In Figure 5. 21(a), if the ZSRC starts up at the AC voltage zero crossing (point a in Figure 5. 20), the voltage across the H-bridge would be twice of the AC peak voltage as v_H is the difference between the sum of the Z-source capacitors' voltage and the AC input voltage. In this case the Z-source inductor current is almost zero as the input voltage experiences zero crossing. In Figure 5. 21(b), if the ZSRC starts up at the rising edge of the AC voltage (point b in Figure 5. 20), the voltage across the H-bridge would be around 2/3 of point a's voltage. The inrush current is higher than

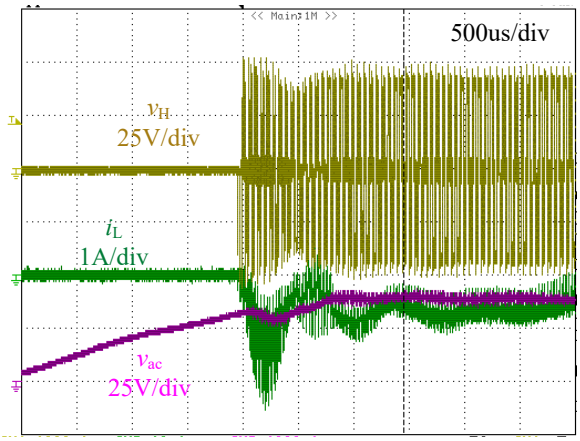
point a's current but it is still small compared to the steady state current. In Figure 5. 21(c), if the ZSRC starts up at the AC voltage peak (point c in Figure 5. 20), the voltage across the H-bridge would be minimum among these candidates. However, the inrush current is the highest and the sudden change of high di/dt would cause some voltage drop due to line impedance from variac. In Figure 5. 21(d), if the ZSRC starts up at the falling edge of the AC voltage (point d in Figure 5. 20), the initial voltage across the H-bridge and the inrush current are similar to those of point b. However, as the AC input voltage falls, not much energy is being drawn from the output, and the Z-source capacitors voltage are still around AC peak. Therefore, the v_H rises when the AC voltage falls to zero and introduces higher voltage stress on the switches than that of point b. In summary, startup at the rising edge of AC voltage (point b in Figure 5. 20) is the best option with minimum voltage stress on the switches and acceptable inrush current. Figure 5. 22 shows the start-up waveforms at rated input voltage and full load, which is coordinated with the discussion above.



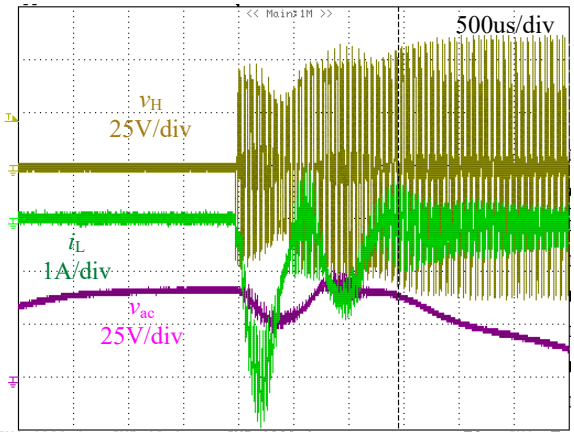
(a) Startup at the AC voltage zero crossing

Figure 5. 21 Soft startup waveforms for the proposed input power control at 32 V AC input voltage

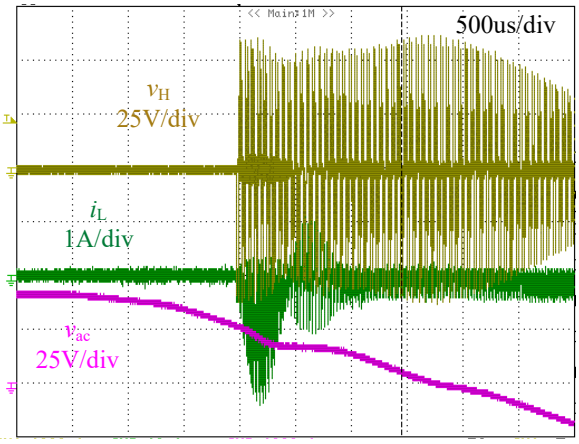
Figure 5. 21 (cont'd)



(b) Startup at the rising edge of the AC voltage



(c) Startup at the AC voltage peak



(d) Startup at the falling edge of the AC voltage

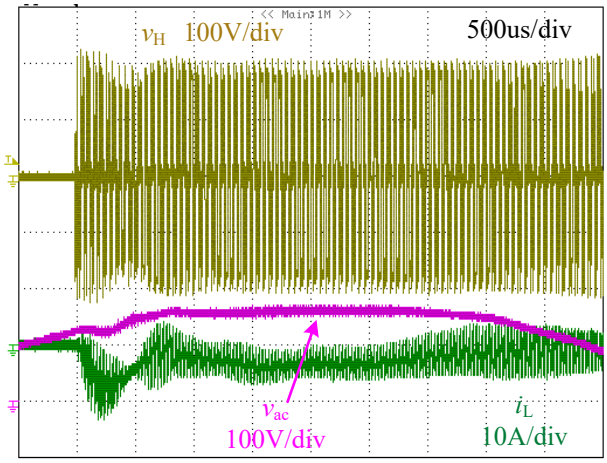


Figure 5. 22 Soft startup waveforms for the proposed input power control at full load (120 Vac/1 kW)

5.4 Summary

ZSRC is a single-stage solution with low cost and high efficiency for EV wireless charger application. To perform both PFC and load regulation functions, the control scheme is more challenged and sophisticated. This paper focus on light load situations in discontinuous mode. A pulse notch control is proposed to realize both PFC and load regulation. Pulse notch control has a relatively good performance in THD and it passes IEC61000-3-2 Class A. Moreover, it absorbs almost all the 2ω ripple power into the ZSN capacitors, which helps minimizing the output capacitance. The limitation of this control is its narrow operation region in discontinuous mode only.

To further reduce the size of bulky capacitors in single phase application, sinusoidal charging technique has been applied to the ZSRC. The Z-source capacitor has been reduced from 4.7 mF to 20 uF to handle the switching ripple only. Both PFC and load regulation functions have been successfully achieved with the two proposed control schemes. They have a relatively good performance in THD and pass IEC61000-3-2 Class A. The input power control has less voltage

stress on the switches than the input current control, and therefore, is preferable. Moreover, the ZSRC has inherent soft startup capability. The limitation of these controls is that the input current cannot be perfectly compensated as sinusoidal wave without distortion due to the tail current.

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CHAPTER 6 Conclusions and Future Works

6.1 Contributions

This work has the following contributions:

- A theoretical and practical design for harmonic system is proposed. A comprehensive comparison between different harmonic orders as the power carrier is made. A third harmonic prototype is built to verify the proposed design.
- An effective output voltage control method using harmonic burst control for EV battery charging is developed. By bursting between different harmonics, not only the load regulation is realized but also soft switching at both turn-ons and turn-offs is achieved. The efficacy of the proposed control scheme is verified with experimental results.
- Two constant frequency control methods are proposed for the load regulation methods in SiC based Z-source resonant converter for wireless power transfer application. A comparison is carried out by both theoretical analysis and experimental results.
- The conventional charging and the sinusoidal charging methods have been demonstrated on the Z-source resonant converter. A pulse notch control is proposed to realize both PFC and load regulation for the ZSRC. In addition, sinusoidal charging can reduce the bulky capacitor in Z-source network. Experimental results illustrate the above proposed methods.

6.2 Future works

The Z-source resonant converter has less components than the two-stage solution, boost PFC plus DC/DC. Only the theoretical comparison has been given. Future work should include a side by side comparison on the size of the capacitor and inductor, the total cost of the

semiconductor devices and the overall efficiency. Also, an optimal design for the ZSRC is required to achieve the best performance.

For conventional charging, the proposed control method is only suitable for light load conditions. In heavy load condition, there is unstable issue for current control method. Although this issue can be avoided by adopting sinusoidal charging, a complete solution is needed to fill the blank in the theory.