SWITCHED CAPACITOR-BASED DC-DC CONVERTER WITH ULTRA-HIGH EFFICIENCY, POWER DENSITY AND VOLTAGE REGULATION CAPABILITY

By

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ABSTRACT

SWITCHED CAPACITOR-BASED DC-DC CONVERTER WITH ULTRA-HIGH EFFICIENCY, POWER DENSITY AND VOLTAGE REGULATION CAPABILITY

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High efficiency and high power-density DC-DC converters are a key requirement in modern Power Electronics systems. Solar photovoltaic (PV) systems, EV/HEV powertrains and Data-centers are a few key examples. Traditional bridge-based DC-DC converters are commonly used in most systems that need a high voltage-gain. The presence of multiple stages in them affects the overall efficiency of the converter. In comparison, Dickson type switched capacitor DC-DC converters (SCCs) offer a single stage solution that lead to key advantages such as high efficiency, high power density, ease of control and elimination of central magnetic components in the system. However, their application in power conversion is limited due to the following reasons:

1. Conventional SCCs have two fixed operating states. Operating the converter between these states leads to a fixed voltage gain in boost mode and fixed step-down ratio in buck mode operation. The output voltage cannot be regulated for varying inputs and results in larger output capacitor ratings and larger voltage stress on downstream converters.
2. As the required voltage-gain increases, it leads to increased switch count and larger volume of required passives. Due to the presence of multiple floating switches, it also increases the complexity of gate drive and auxiliary power stages. This leads to lower efficiency and power density at high gains.

The key contributions of this dissertation to the field of switched capacitor-based power conversion are as follows:

1. The concept of utilizing additional transition mode operating states for Dickson type SCCs is introduced. This enables the possibility of achieving real-time gain variation using SCCs without adding additional stages or passive components down-stream. These states are designed to not affect the steady-state efficiency of the converter. In comparison to traditional SCCs, it results in a 30% reduction in the voltage rating of output capacitors and down-stream converter switches when used for a PV system application. A peak efficiency of 96+% is achieved for a 1-kW prototype.
2. During gain transition, transient current at the input side of the SCCs relies (to some extent) on the trace inductance present in individual switched capacitor cells. A capacitive energy re-distribution approach for switched capacitor cells is proposed to minimize the input current transitions seen at the input of the converter. This enables 'smooth' gain transitions in the SCCs. Experimental results on a 1-kW prototype converter illustrate that peak current transient is limited to well-within 1.5 times the rated current through the converter.
3. A resonant Dickson type SCC configuration using GaN HEMTs that enables ultra-high efficiency and power density at high voltage step-down ratios is proposed. Some of the key aspects of the proposed configuration are the ability to maintain minimum number of switches, a distributed inductive-capacitive approach to power transfer in each individual SCC cell, a highly-efficient integrated gate drive stage and optimally designed passive components. The proposed configuration is designed to meet specifications of a 270 V/28 V (nominal) power converter in a more-electric aircraft. A peak efficiency of 99.1% and a power density of over 5 kW/L is achieved for a 300 W converter prototype.

Dedicated to my wife, Vidhya Ramalingam,
for always being my pillar of strength.

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1 INTRODUCTION

A power converter/inverter system (PCIS) is a key part of several different power electronics systems. Figure 1.1 illustrates the PCIS present in three key applications. In Figure 1.1 (a), the case of a residential solar photovoltaic (PV) power system is illustrated. In this configuration, the varying DC output voltage output of a solar panel, V_{in} is converted to a nominal DC-link voltage of 200 V. The subsequent inverter stage produces the required AC voltage, V_{out} (typically 120 V) to deliver power to standalone loads or the utility. Such implementations are commercially known as "PV micro-inverter" and are being widely installed in residential solar rooftops around the world [1]. String inverters that use a centralized inverter to interface to the grid also use require a DC-DC converter to interface to the utility or load.

Figure 1.1 (b) illustrates the case of a commercial hybrid electric/ electric vehicle power train [2]-[4]. Here, output voltage from the High-voltage (HV) battery pack, V_{in} (typically about 200 V) is converted to a DC link voltage, V_{DC} of 450 to 600 V using the step-up DC-DC converter. The subsequent inverter stages provide the required AC voltage for driving the traction motor and/or additional motor/generator unit. The HV battery pack is also charged by means of the generator feeding power through the inverter and step-up converter back to the battery pack. Hence, a bidirectional step-up DC-DC converter is needed for this application.

Figure 1.1 (c) illustrates part of the power system within a commercial more-electric-aircraft (MEA) [5]. Here, voltage output from the generator, V_{in} (typically 115 V) is converted to a DC link voltage, V_{DC} of 270 V using the rectifier. The 270 V DC-link voltage is converted to 28 V

using a step-down DC-DC converter to generate the required 28 V power supply in the aircraft. The 270 V power supply required in the aircraft is directly derived from the DC-link voltage.

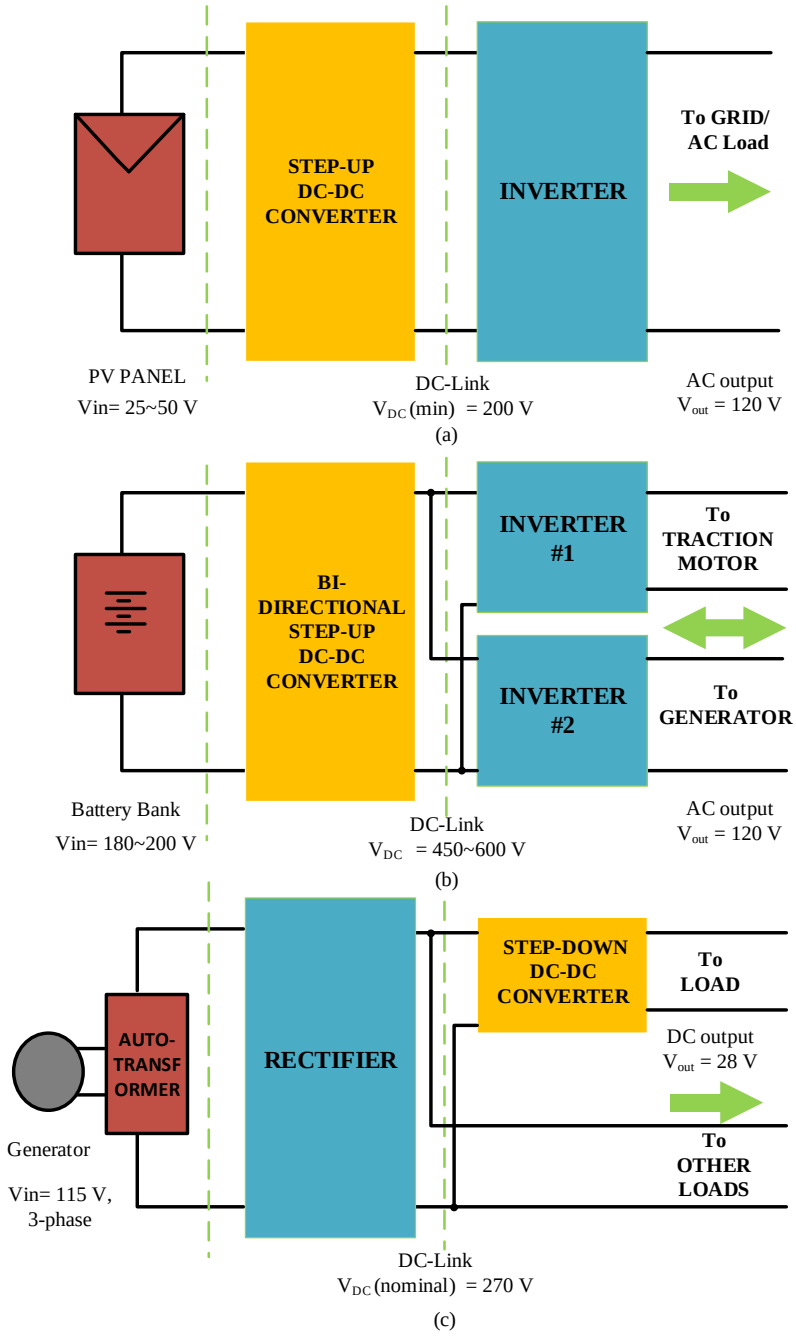


Figure 1.1: Block diagrams of power converter/inverter systems in different applications: (a): Residential solar PV system, (b): Hybrid/Electric Vehicle (HEV/EV) powertrain, (c): More Electric-aircraft (MEA) power system.

From the illustrations in these figures, it is clear that the role of the DC-DC converter is crucial for the operation of the overall PCIS. The ideal specifications of a DC-DC converter used in these cases can be generalized as follows:

1. High power density: Weight and size of the power converter translates to system cost in most cases. This is of added importance in case of airborne and automotive applications.
2. High efficiency: A more efficient system implies lesser auxiliary cooling systems leading to reduction in weight and hence cost.
3. Capable of large voltage gains: A gain of 8 required in case of residential PV systems, A gain of 10 required in a MEA.
4. Capable of bidirectional operation: To facilitate battery charging in the case of HEV powertrains.
5. Capable of operation at high temperature: In the case of a PV application, the entire unit is mounted outdoors, below the PV panel. In the case of EV and MEAs, the internal powertrain temperature is also much higher than the regular ambient temperature.

Existing high-gain DC-DC converters can be broadly classified into two different technologies depending on the type of power transfer involved in the converter. The benefits and limitations of each of these technologies are listed below:

1.1 Centralized magnetics-based DC-DC converters

Figure 1.2 illustrates the basic power circuit of two key types of bidirectional centralized magnetics-based DC-DC converters. The semiconductor switches used in these circuits are

represented by means of generic switches. This convention is followed throughout this dissertation.

The two-switch bidirectional boost/buck converter in

Figure 1.2 (a) is suitable for gains in the range of 1 to 3. However, at higher gains, the efficiency of the converter reduces [6]. Additionally, perhaps more importantly, the overall voltage and current stress of the devices increase as the gain increases. In view of these, these converters are limited to voltage gains below 3 in a practical system. A centralized inductor designed to carry the highest current of the converter is indispensable to this converter structure. The size and packaging constraints of the central inductor limits the overall power density (W/in^3) of the converter. In most cases, the required inductance is realized by using a magnetic core. However, the permeability of these materials reduces at higher temperatures leading to potential problems in control and operation of the converter.

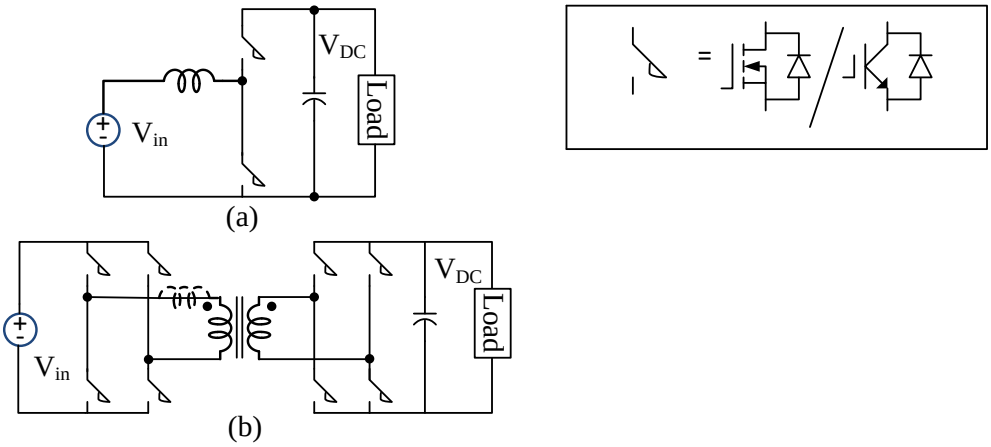


Figure 1.2: Two types of magnetics-based DC-DC converters, (a): Two-switch bidirectional boost/buck converter, (b): Bidirectional Full-bridge DC-DC converter.

A generic structure of the bridge converter and its variants is illustrated in

Figure 1.2 (b). They are widely used in cases of high gains where the usage of a two-switch converter illustrated in

Figure 1.2 (a) is no longer practical. In this case, the converter essentially uses three power stages. In the first stage, the input DC voltage is converted to a high-frequency AC voltage across the transformer input terminals. In the next stage, this high frequency voltage is transferred to the secondary side or the output terminals of the transformer. In the final stage, the high-frequency AC voltage is rectified to provide a DC output voltage to the load. By designing the high-frequency transformer suitably, a large voltage gain can be obtained without significantly compromising the efficiency of the converter. However, the overall efficiency of the converter is now a function of the product of the individual power stages. Assuming a hypothetical 99% efficiency each for the input inverter stage, the transformer stage and the output rectifier stage leads to a system efficiency of about 97%. The voltage rating of the switches on the load side of the transformer has to be designed for the output voltage. On similar lines, the current rating of the switches on the input side of the converter has to be designed for the input current.

1.2 Switched Capacitor based DC-DC converters (SCCs)

Traditionally, switched-capacitor based DC-DC converter technology (also known as charge-pump) was used in low-voltage, low-power applications where the requirement for high efficiency was not a major concern [7]. Several different types of switched capacitor converters exist in literature [8]. However, one particular type, “Dickson converter” [9] offers numerous advantages for implementation at higher power levels and large voltage gains suitable for modern day PCIS. The key difference between the general structure of the centralized magnetics-based converters and the switched capacitor type converters lie in the overall energy storage and power transfer schemes. Switched capacitor converters use an entirely distributed approach in terms of storing energy. There is no single bulk energy storage capacitor or inductor. This leads to the ability to

have multiple power transfer loops occurring in parallel thereby avoiding the requirement for a three-stage cascaded power conversion scheme. This leads to high efficiency and low device stress (voltage and current rating of individual switches). The number of devices conducting the input current at any given time is also fixed irrespective of the voltage gain. This makes it suitable for a high efficiency, high power density converters.

Since then, two other variants of the Dickson converter for a PCIS have been proposed. The three variants of the Dickson converter configured for a gain of 4 are illustrated in Figure 1.3. In all these variants, the switches clamped by the input voltage, V_{in} are termed as "leg switches", the remaining switches are termed as "arm switches". The leg switches are labeled with subscripts p and n. The arm switches are labeled with subscripts a and b. This notation is followed throughout this dissertation.

The "original" Dickson converter proposed in [9] is illustrated in Figure 1.3 (a). Here, the converter is configured to have a gain of 4. The voltages across individual arm capacitors are V_{in}, $2V_{in}$, $3V_{in}$ and $4V_{in}$ respectively. The total number of switches and capacitors along peak voltage and average current ratings of individual switches are summarized in Table 1.1. From the table, it can be seen that the number of leg switches are fixed as 4 irrespective of the voltage gain. This leads to an average current rating of $N*I_o$ for the 'leg' switches, where 'N' is the gain of the converter. The average current, I_o for the arm switches arises from an average current of $2I_o$ during one half-cycle and 0 during the other in a switching period.

The MMCCC converter illustrated in Figure 1.3 (b) [10] essentially modularizes the leg switches in the original Dickson type converter. This leads to all the leg switches having identical current

ratings. While, the converter switch ratings are modular in nature, the number of capacitors and the voltage across individual capacitors remains the same.

The NX converter [11] illustrated in Figure 1.3 (c) reduces the voltage ratings of individual capacitors by essentially interleaving the arms of two Dickson type converters. However, the current ratings of the leg switches are doubled compared to the MMCCC type converter. Also, due to the interleaving nature, the output voltage ripple is minimized. This configuration leads to a compact and modularized configuration compared to the other two types.

Dickson Type	Arm Switches (a,b)			'Leg' Switches			Capacito-rs	Total Capacito-rs	Total Switc-hes
	No.of switc hes	Avg. Curre -nt	Peak Volta- ge	Numb -er	Curre -nt	Volta- ge	Voltage Range		
Original	N-2	I_o	$2V_{in}$	4	(N/2)I	V_{in}	V_{in} to NV_{in}	N	N+4
	2	I_o	V_{in}	-	-	-	-	-	-
MMCCC	N-2	I_o	$2V_{in}$	2N-2	I_o	V_{in}	V_{in} to NV_{in}	N	3N-2
	2	I_o	V_{in}	-	-	-	-	-	-
NX	N-2	I_o	$2V_{in}$	N	$2I_o$	V_{in}	V_{in} to $2V_{in}$	N	2N
	2	I_o	V_{in}	-	-	-	-	-	-

Table 1.1: Summary of switch and capacitor ratings in Dickson type converters.

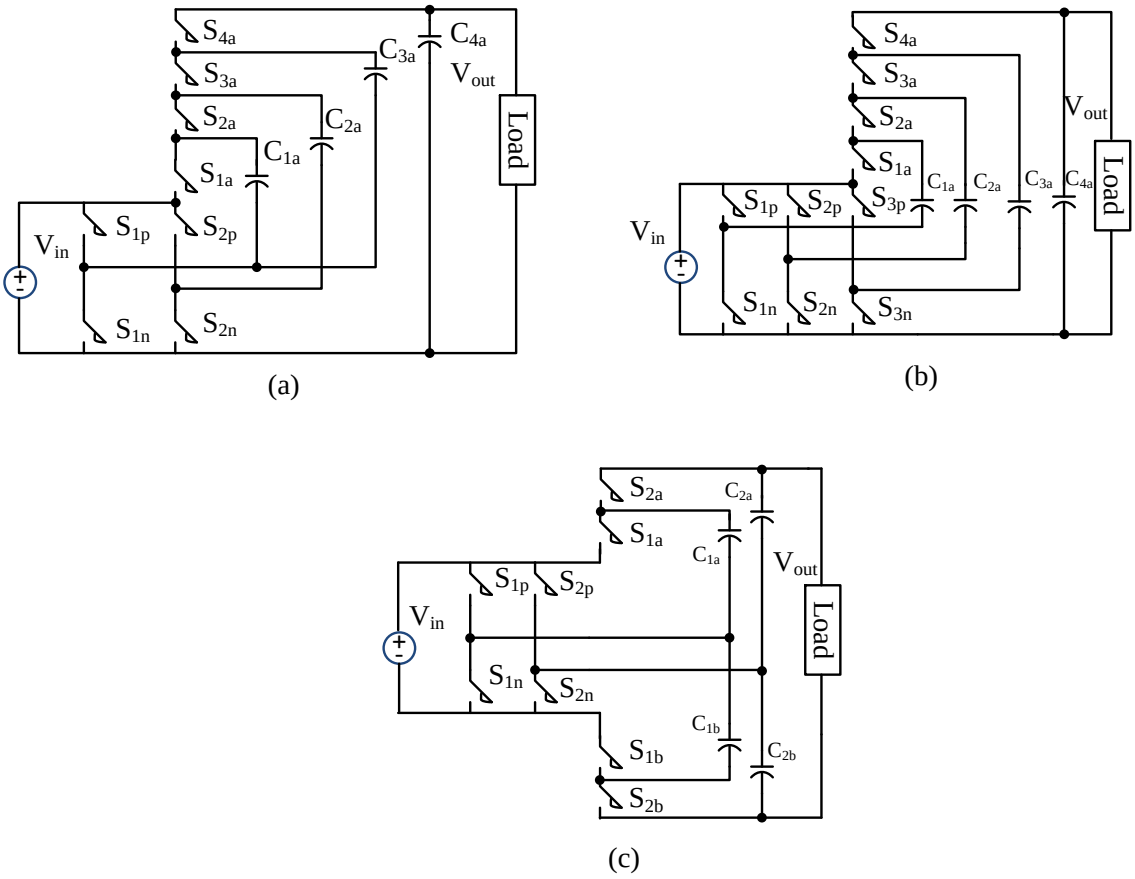


Figure 1.3: The three variants of Dickson converter: (a) The original Dickson converter[8], (b): Modular Multi-level Clamped Capacitor converter (MMCCC[10]), (c): NX converter[11].

1.3 The need for voltage regulation in Dickson type converters

While the Dickson type converters have several advantages (as described above), they have some major limitations. First, the gain of the converter is fixed by design. Continuous voltage regulation is theoretically not possible without compromising the high efficiency of the converter. This essentially means that the downstream inverter in a PCIS has to be rated for the maximum output voltage of the DC-DC converter. For instance, in the PV case described in Figure 1.1(a), if the DC-DC stage is designed for a fixed gain of 8, the voltage rating of the switches has to be rated for 400 V. This is an over-design for generating the required 170 V at the AC terminals of the inverter. This leads to a larger size of the overall system.

Next, the Dickson type converters are only capable of achieving integer voltage gains. This is a major limitation in applications that need fractional voltage gains. In order to provide voltage regulation capability to the Dickson type converters, a few different methods are proposed in literature. These methods are reviewed here.

In [12], one method to achieve variable gains using the MMCCC variant of the Dickson converter is proposed. Here, individual MMCCC cells are cascaded by means of additional switches. By controlling the switching state of these additional switches, individual cells can either be bypassed or inserted into the path of power flow from the input to output. So, this method essentially uses multiple cascaded cells to achieve variable gains. This leads to large number of switches conducting the input current and leads to lower efficiency. This negates one of the key advantages of the Dickson type converter. The increased switch count further increases the overall cost and size of the system.

Yet another method to achieve a variable gain for the Dickson converter is proposed in [13]. Here, by introducing additional inductors and selecting the appropriate phase relationship between the two operating states of the converter, a fractional variation in gain can be achieved. By combining this gain variation with the method proposed in [12], a larger/finer regulation in gain is proposed. However, the maximum gain variation is a function of the load and the degree of gain variation is limited at lower loads. Also, the current ratings of individual devices are expected to be higher when the phase relationship between the operating states deviates from 50%. A peak efficiency of about 90% is reported for such a configuration. An identical method has also been proposed in [14], where the phase relationship between the two operating states is varied to achieve a continuous output voltage variation. In this case, the current rating of the individual switches increases drastically, and the system is no longer practical.

Yet another method to achieve variable output gains using the Dickson type converter has been proposed in [15]. Here, an additional switch/voltage divider network is provided to vary the input voltage provided to the switched capacitor network. This leads to increase in overall size of the converter and increased current stress for the input voltage source. In case of input voltage derived from large battery packs (such as EVs), this may also lead to charge unbalance between different cells of the battery. Fractional gains can be achieved by tapping into a fractional input voltage.

Other methods to achieve a variable and fractional gain for the Dickson type converters include the usage of an external/integrated downstream buck converter to provide the necessary voltage regulation and fractional gain [16]-[19]. However, for the purpose of this dissertation, this is considered as an external stage not part of the switched capacitor power stage.

Several other articles in literature discuss methods to achieve a variable output voltage using switched capacitor converters. However, they can all be classified into the above described types.

In order to advance the switched capacitor technology, especially for the Dickson type converters, there is a need to investigate methods to achieve variable and fractional output voltage without compromising on efficiency or adding large external magnetic components.

1.4 Ultra-high efficiency and power density SCC s for large voltage gains/step-down ratio

In order to achieve ultra-high efficiencies (over 98%) using SCCs, there is a need to minimize the overall losses in the system. In theory, operating SCCs with a minimum capacitor voltage ripple across individual capacitors [8] leads to improved efficiency. However, at a system level this

translates to increased switching frequencies for the individual switches. This can lead to increased switching losses for individual switches that can offset the benefits of operating at a lower capacitor voltage ripple. In order to overcome this limitation, resonant zero-current switched capacitor circuits and topologies have been investigated [20]-[24] overcome losses in each switched capacitor cell. While one part of switching losses can be eliminated by zero-current switching, the losses due to charging and discharging of the switch parasitic output capacitor, C_{oss} and the input capacitor, C_{iss} is not influenced by this scheme.

The power semiconductor device space has truly evolved in the past decade. Gallium Nitride (GaN) power semiconductor device technology is mature and is commercially available at a viable price point to reap its benefits. These devices have extremely good figure of merit (FOM) numbers when compared to their Silicon counterparts. This has considerably changed the landscape of power electronics systems and is continuing to evolve [25]. The voltage ratings of GaN switches along with its small footprint and much improved C_{oss} and C_{iss} parameters makes it a suitable candidate for switched capacitor type applications. It enables further improvement in efficiency and system power density. A few GaN based SCC topologies have been investigated for a 4:1 voltage step down ratio [26]-[28]. But, several applications require a much higher voltage step-down ratio (as discussed in the beginning of this section). As the required step-down ratio increases, the number of switches and capacitors in each arm of the converter increases. Increased component count is a potential concern for power density and efficiency. As majority of these switches are floating, efficient gate drive stage for each of these switches is another bottleneck. Thorough investigation on a suitable topology and system design optimization techniques for high-

gain resonant SCCs can go a long way in achieving high efficiency, high-power density SCC systems for a variety of applications discussed before.

1.5 Theses and their potential impact in power electronics systems

Thesis 1: Real-time voltage regulation and fractional voltage gains in Dickson type switched capacitor DC-DC converter is achievable by means of controlled intermediate operating states in an otherwise constant operating state trajectory. Doing so does not impact steady-state efficiency of the converter or the sizing of passive components in the system.

Impact: For a PV micro-inverter system, this provides the unique opportunity to achieve real-time gain variation in a switched capacitor-based DC-DC converter stage. The overall voltage stress of the downstream inverter stage is reduced by over 30% (in comparison to traditional SCC) resulting in improved efficiency and reduced system cost. The dynamic response time of the overall system is also improved as the inverter DC link voltage is now well regulated. The ability to provide fractional voltage gains also enables optimal system design and unlocks newer applications that aren't possible with an integer voltage gain in the DC-DC stage.

Thesis 2: An improved voltage regulation method for Dickson type DC-DC converter that minimizes or eliminates large input current transients is achievable by utilizing the load and adjacent switched capacitor cells to re-distribute the energy in the switched capacitor network during gain transition.

Impact: Further improves usability of the Dickson type SCCs in applications that have tighter constraints in the transient/in rush current requirements. A typical example is that of an xEV

powertrain where there are tighter requirements for current transients drawn from batteries during normal operation.

Thesis 3: A resonant Dickson converter configuration that uses GaN switches, distributed inductive and capacitive elements in individual power transfer stages, combined with an integrated efficient gate drive and system-level loss optimization can result in an ultra-high efficiency (>99+%) and high power-density (~100 W/in^3) DC-DC converter suitable for high voltage step-down ratios (>8).

Impact: So far, GaN based resonant Dickson converters have only been adopted for the power stage in low step-down ratio applications such as data-center power supplies (4:1 ratio). At higher step-down ratios, the increased number of switches and capacitor cells constrains the efficiency and power density of the system. By means of the configuration and system optimization techniques proposed here, ultra-high efficiency and power densities at high-gains (>8) are made possible. This leads to improved efficiency and power density in applications such as more-electric aircrafts that require a 270 V to 28 V step down at a high efficiency and power density.

1.6 Structure and Scope of the dissertation

Chapter 2 is aimed at addressing Thesis 1. The need for voltage regulation and fractional voltage gains in switched capacitor converters is first introduced and the configuration of the converter termed as variable (n/m)X converter is introduced. New operating states for the (n/m)X converter are then proposed to achieve dynamic variation in gain. The proposed operating states utilize all the trace/stray inductance in the converter to achieve mode transition. No external magnetic

components are necessary. Detailed transient analysis and design methodology for a A 1-kW (n/m)X converter prototype suitable for a PV application along with the control blocks are presented. An example case is demonstrated to illustrate reduction in overall voltage stress of a PV PCIS by 33%. A peak efficiency of 96% is achieved for a Si based prototype. Experimental results obtained for the prototype validate the proposed theory.

Chapter 3 is aimed at addressing Thesis 2. Improved gain transition methods for the (n/m)X converter are proposed. Here, the concept of soft-transition in gain is first introduced. Next, two different control methods to achieve a variation in gain with reduced input current transient are proposed. Using the proposed method, the input current transient is limited to within 150% of the peak load input current. Experimental results on a 1 kW prototype is then presented to validate the proposed theory.

Chapter 4 is aimed at addressing Thesis 3. A GaN HEMT based resonant Dickson converter configuration is proposed that achieves ultra-high efficiency and power densities for high voltage step-down ratios (>8). System level loss optimization, efficient gate drive and optimization of passive component design form the key aspects of the chapter. The power stage of a 270 V/28 V (nominal gain of 10) converter in a more-electric aircraft (MEA) forms a good use case for the proposed converter. To this effect, a 300 W converter prototype is designed for this specification. A peak efficiency of 99.1% and a power density of 87 W/in^3 is achieved using this prototype. Every aspect of the converter design revolves around utilizing and extracting key benefits of GaN HEMTs for this application. The configuration and design methodology introduced here can be extended to other GaN based high gain (or step-down ratio) applications.

Chapter 5 provides concluding remarks and possible avenues for future research based on this dissertation.

CHAPTER 2 VARIABLE (N/M)X SWITCHED CAPACITOR DC –DC CONVERTER

2.1 Introduction

High voltage-gain bidirectional DC-DC converters play a major part in solar photovoltaic (PV) and electric vehicle (EV) applications. In the case of EV applications, a bidirectional high boost converter is used to interface power between the motor and generator units (in case of a power split based EV) and the battery bank as in [29]-[31]. In the case of solar PV module connected to the power grid or a standalone AC load, a high boost converter is essential to convert the varying input DC voltage (typically 1:2) to a fixed output DC voltage. This output DC voltage serves as the DC link voltage for the power inverter stage as in [30],[31]. For both these applications, a conventional boost converter (two-switches for bidirectional capability) is the preferred choice when the boost ratio is not too high. An isolated DC-DC converter is typically used when the boost ratio is high. While both these forms of boost converters can work reliably, both of them require bulky magnetic components. This reduces the power density of such converters. Additionally, the permeability of these magnetic components varies with change in temperature. This can lead to decrease in inductance with increasing temperature. This is a major bottleneck for both control and reliability at high temperatures. Depending on the magnitude of the required voltage gains, the switches also undergo high stress levels. The need to reduce inductance, achieve high power density and high efficiency output in DC-DC converters has seen an interesting development over the years. DC-DC converters based on multi-level converters (MLCs) have been known to increase power density [33]-[38]. In the flying capacitor structure in [32],[35], [36] and [37] the number of switches conducting the input current increases with increase in gain. Thus, at higher gain levels, this would lead to a larger voltage drop leading to low efficiency [38]. The Dickson converter introduced in [9] uses a switched capacitor circuit with no external magnetic components to

alleviate this problem by ensuring that only a minimum number of switches conduct current in any given path. The other benefits and limitations of switched capacitor-based circuits when used in power converters have been discussed in [17], [39] and [40]. But, it is established that Dickson based circuits offer superior performance in terms of modularity and scalability compared to other switched capacitor [8] configurations. More recently, a multilevel modular capacitor-clamped converter (MMCCC) circuit based on the Dickson converter has been proposed [10]. The circuit offers numerous advantages such as low device current conduction and the ability to eliminate external inductors. For any given current path, only a maximum of three devices conduct. This leads to high efficiency and makes the circuit suitable for high voltage gains. Also, the control mechanism for this circuit is extremely simple. However, the circuit has a total of 3N-2 switches for a given 'NX' conversion ratio. This circuit has been improved upon by [11], where a double wing structure is proposed in order to further reduce the current ripple in the output capacitors. The voltage ratings of individual capacitors have also been reduced significantly. The number of devices have also been brought down from 3N-2 to 2N leading to a reduction in overall device count. Additional embodiments such as multi-phase structure and soft-switching have been proposed in [23], [41]. The optimal design procedure for the double wing based switched capacitor circuit has been presented in **[**42]. In **[**43], a compact, high power density "NX converter" has been designed based on the double wing structure proposed in [11], [23] and [41]. The circuit uses a modular design for the entire power converter based on equal capacitances and trace inductances for every stage. But, the nX converter in [43] has just one operating point, where the output voltage is a fixed integer multiple of the input voltage. It is severely limited by its inability to provide dynamically varying voltage gains and fractional voltage gains. In [12], [13]embodiments of the "variable gain" MMCCC have been proposed. But, the design in [12] involves modification to the

basic cell and the cascading of several cells. This leads to a much higher switch count and lower efficiency due to multiple cascaded cells. In [13], the achievable maximum voltage gain is a function of the load, which limits its application. In [16], [45], variable voltage gains are achieved using cascaded switched capacitor cells. In [46], a binary and Fibonacci based switched capacitor circuit have been combined to provide variable voltage gains. In [15] and [47], fractional voltage gains using a ladder based switched capacitor converter and a Dickson based converter are achieved by using multiple tappings. But, in order to vary the gain during regular operation, an additional switch network is necessary. Although, in theory or for low power implementations, these circuits are capable of variable and fractional voltage gains, they are not used for over 100 W. Based on the limitations of existing switched capacitor-based circuits, there is a need for a power converter based on a switched capacitor circuit that can provide variable and fractional voltage gains at high efficiencies at higher power levels (close to 1 kW or more). The aim of this chapter is to propose a circuit configuration and its control method to achieve these functionalities using a generalized configuration of a Dickson based switched capacitor converter. The proposed converter is termed, (n/m)X converter owing to its ability to provide a variable fractional gain, n/m. The (n/m)X converter can be designed to achieve fractional gains that can be varied in discrete steps during regular operation of the converter. In order to achieve higher efficiency and high power density in the proposed circuit, cascading of multiple cells or additional switches are not used. Instead, new degrees of freedom within a switched capacitor cell are exploited to achieve the target. While, the proposed converter cannot offer continuous voltage regulation, the voltage gain can be varied in discrete steps. By suitably designing the converter for a set of variable voltage gains, the device voltage stress of the inverter in a converter/inverter system can be reduced significantly (over 33% in an example case disclosed in this chapter). Comparison with existing

two-stage/integrated converters as in [18], [55]in terms of voltage regulation is avoided in this chapter as the proposed converter is not considered a replacement for such a system. The proposed converter has the potential to be used as the front end in any such two-stage or integrated converter systems to further improve voltage regulation with lower device voltage stress. Such an embodiment is beyond the scope of this chapter. Analysis of the different operating stages, description of multiple control methods, design procedure for an example converter/inverter system, efficiency analysis and experimental results for a 1kW prototype of a (4/0.5) X converter form the main crux of this chapter. An efficiency of over 95% is achieved using the converter when the gain is allowed to vary every 100 ms.

The rest of this chapter is organized as follows: Section 2.2 derives the structure of the (n/m)X converter from a generic (k/m) X structure. The various degrees of freedom present in the circuit are explored in this section. Sections 2.3 and 2.4 describe two methods to dynamically vary the gain of the (n/m)X converter (termed as "mode-change" throughout this chapter), one using assistance from the load and the other independent of the load. Various operating stages (during transition and steady state) encountered in both these methods are clearly described. Section 2.5 describes the equivalent circuits for every mode transition. Sections 0 describes the method to calculate the worst-case transient over-voltage. In section 2.7, the design procedure and specifications for a 1kW prototype of (4/0.5)X converter have been presented. Section 2.8 provides experimental results to demonstrate both, fractional voltage gains and variable voltage gains. Section 2.9 presents the efficiency curves obtained experimentally for the (4/0.5)X converter while in different operating states and during dynamic mode-change.

2.2 The (N/M)X Converter: General Configuration

The (n/m)X converter is derived from a more generic (k/m)X structure. This section describes the generalized structure of the (k/m)X converter and proceeds to explain the (n/m)X converter. The basic configuration is illustrated in Figure 2.1. It can be seen that the proposed converter has 'n' different arms and 'n' different legs leading to a total of '2n' limbs. Each arm comprises of a series connection of two capacitors and two arm switches labeled with suffixes 'a' and 'b'.

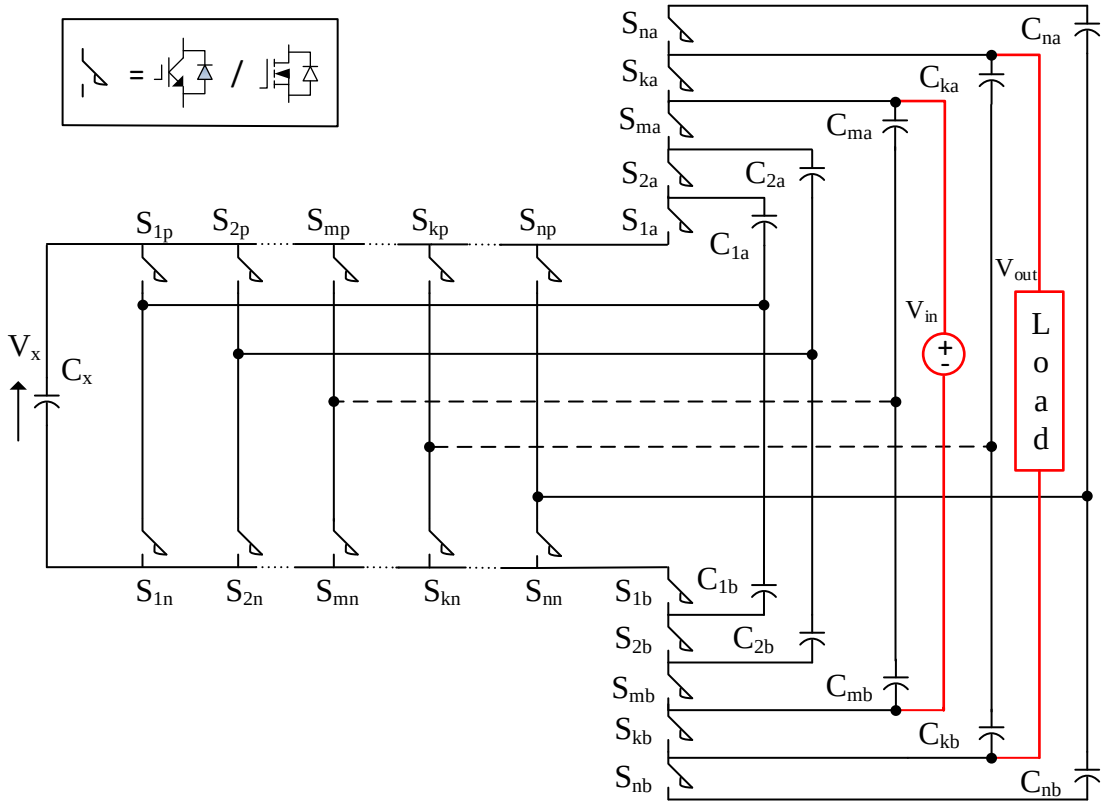
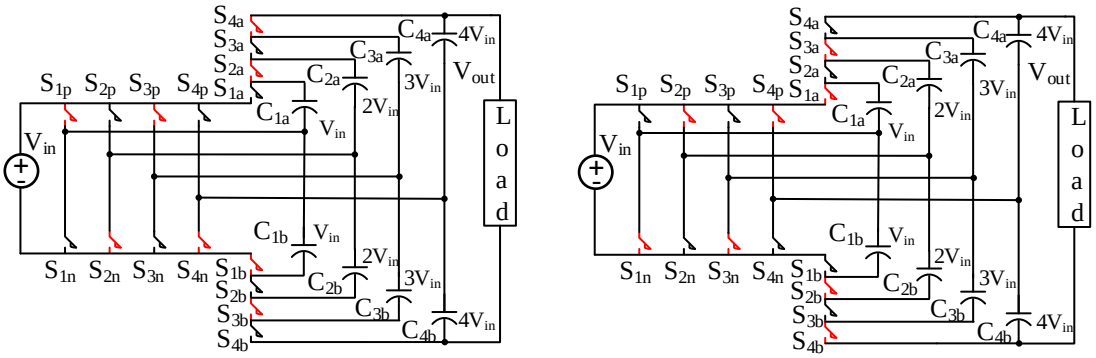


Figure 2.1: A generic (k/m)X converter.

For example, arm no. 1 comprises of capacitors C_{1a} and C_{1b} connected in series with switches S_{1a} and S_{1b}, arm 'm' comprises of capacitors C_{ma} and C_{mb} connected in series and so on. Each leg of the converter consists of a half-bridge cell with two switches switched in a complementary manner. Leg 1 consists of switches S_{1p} and S_{1n}, Leg 2 consists of switches S_{2p} and S_{2n} and so on. For the double wing structure proposed in [11], the relationship between input voltage and the voltage

across individual capacitors has already been established. Figure 2.2 illustrates this relationship along with the two operating states to achieve a gain of 8. Switches marked in red indicate switches that are ON and those marked in black indicate switches that are OFF.



(a) (b)

Figure 2.2: Operating states of an 8X converter.

In comparison to the structure of double wing nX converter in Figure 2.2, it can be observed that extra degrees of freedom with respect to the location of input voltage and load are introduced in the proposed structure. The input voltage V_{in} can now be connected across the capacitors of any of the 'n' arms of the converter. Similarly, the load (output voltage) can also be connected across the capacitors of any of the 'n' arms of the converter. Hereafter, the connection across the capacitors of an arm are simply referred to as connection across the corresponding arm. For a generic location of the input voltage, V_{in} across the m^{th} arm of the converter, the "effective input" voltage, V_X across C_X can be expressed as,

$$V_x = \frac{1}{m} * \frac{V_{in}}{2} \qquad (2.1)$$

Based on the voltage buildup across individual arm capacitors (Figure 2.2) in a double wing structure, for a generic location of the load across arm 'k', output voltage V_{out} can then be expressed as,

$$V_{out} = 2k * V_x = \frac{k}{m} * V_{in} \qquad (2.2)$$

Where, 'm' is the arm (capacitors of the arm) across which the input voltage is connected, k is the arm across which the load is connected and $k, m \leq n$.The converter is fully bidirectional. The relative magnitudes of k and m determine if the converter functions as a boost or buck converter. If k < m, the converter functions as a buck converter. On the other hand, if $k > m$, $V_{out} > V_{in}$ and the converter functions as a boost converter. From Figure 2.1, it can also be seen that, another degree of freedom can be obtained by connecting the source/load across the converter leg. This is achieved by placing the source or load across C_X. If the input voltage, V_{in} is placed across C_X and the load is connected across the generic arm, $'k'$ as described above, the output voltage,

$$V_{out} = \frac{k}{1/2} V_{in} = 2k * V_{in.} \qquad (2.3)$$

Comparing equations (2.2) and (2.3), it can be seen that for the input voltage being placed across, C_X, this presents a case of m=(1/2) for the generic (n/m)X converter. Similarly, if the load is placed across C_X (for buck functionality) and the input voltage is placed across the m^{th} arm as described before, the output voltage V_{out} can now be described as,

$$V_{out} = \frac{\frac{1}{2}}{m} V_{in} = \frac{1}{k} * \frac{V_{in}}{2} \qquad (2.4)$$

Comparing equations (2.2) and (2.4), it can be seen that placing the load across C_X presents a special case of the generic (k/m)X converter where, k=1/2. The acceptable values of k and m can now be listed as below,

$$k = \frac{1}{2} \; or \; k = 1,2 \ldots n. \qquad (2.5)$$

On similar lines,

$$m = \frac{1}{2} \; or \; m = 1,2, \ldots . n. \qquad (2.6)$$

The double wing based nX converter developed in [11]now becomes a special case of the (k/m)X converter. The 8X converter developed in [43] can be represented as a fixed (4/0.5)X converter. The boost nX converter is obtained using k=n and m=1/2. The buck nX converter is obtained by using k=1/2 and m=n. For a given application, say the required ratio of output to input voltage (gain) is 1/4. Based on the discussion above, several sets of (m,k) values can provide the required gain (k/m) of 1/4. For instance, (2,1/2); (4,1) and (8,2) are all valid solutions. But, in order to provide the required gain with the minimum number of semiconductor devices, ′k′ has to be minimized. Thus, for this case, (m,k) of (2,1/2) has the lowest overall device count. The overall system would only contain 2 arms. This implies 4 capacitors and each arm would necessitate four semiconductor switches leading to a total of 8. Hence, the design for a fixed output voltage gain is driven by the need to minimize 'k'. For a given boost converter configuration, the highest output voltage, V_{out} for a given input voltage, V_{in} can be achieved with k=n. Thus, k=n and m=1/2 provides the maximum possible gain. On the other hand, for a buck configuration, m=n and k=1/2 provides the minimum possible gain. Thus, the bounds for the maximum and minimum converter gains are determined by k=n and m=n respectively. This means that the (k/m)X converter functions as an (n/m)X boost converter or (k/n)X buck converter within the realms of the maximum and minimum output voltage requirements. The ability to vary the value of 'm' by varying the location of input voltage, V_{in} in a (n/m)X configuration is shown in Figure 2.3. Using this method, fractional voltage gain can be achieved. The location of the input voltage now becomes a design parameter and is fixed based on the required voltage gain. The location of input voltage cannot be varied during operation. Experimental results illustrating the different fractional gains using a variable (4/(1/2))X or (4/0.5)X converter are presented in Section 2.7. The various possible gains achievable by varying m from ½ to 4 are, (4/1), (4/2), (4/3) and (4/4) respectively.

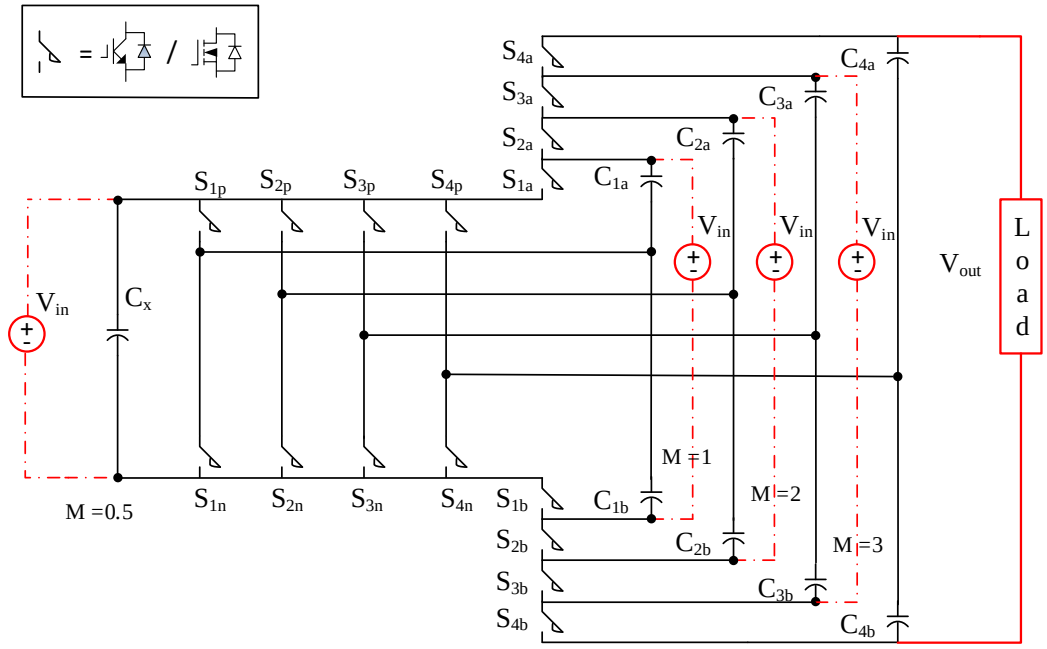


Figure 2.3: A (4/0.5)X converter with different locations of input voltage.

2.3 Gain Variation using the (n/m)X converter

As this method is independent of the type and magnitude of load, it is termed as "load independent" mode change.

2.3.1 Load independent "shift-down"

Figure 2.4 (a) through (c) illustrates the trajectory of the various stages during load independent "shift-down" and Figure 2.4 (c) through (a) illustrates the trajectory of various stages resulting in load independent "shift-up" operation. In any given operating state, the switches marked in red indicate switches that are ON. Grey is used to indicate switches and current paths that are OFF due to the switches being OFF. The purple colored arrow adjacent to the arm capacitors indicates that the capacitor is being discharged in the corresponding operating state. The teal colored arrow indicates that the capacitor is being charged during the operating state. This color code is followed through the rest of the dissertation. For the (4/0.5)X converter, transitioning from stage (a) to (c) results in a "shift-down" from an initial gain of 8 to a final gain of 4. Each stage comprises of two

alternating operating states within a switching cycle (50% duration each) which are represented by means of roman numerals within each stage.

Stage (a)

The operating states ((i) and (ii)) within this stage are identical to that of the fixed 8X converter in [43]. The converter continuously switches between these two operating states in order to achieve a gain of 8. This is illustrated in Figure 2.4 (a). Each operating state in this stage exists for 50% duration in a given switching cycle. In steady state, the average voltage across capacitors C_{1a}, C_{2a}, C_{3a} and C_{4a} equal V_{in}, $2V_{in}$, $3V_{in}$ and $4V_{in}$ respectively. Due to the symmetric structure, the voltages across individual capacitors in the lower wing, C_{1b}, C_{2b}, C_{3b} and C_{4b} are equal to the voltages across corresponding capacitors in the upper wing.

Stage (b)

Transition from stage (a) to (b) occurs when a gain "shift-down" operation from 8 to 6 is initiated. Stage (b) comprises of two alternating states (iii) and (iv), each lasting for 50% duration in a switching period. This is illustrated in Figure 2.4 (b). In operating states (iii) and (iv), the switching states in arm 4 and leg 4 are identical to switching states of switches in arm 3 and leg 3 respectively. In operating state (iii), capacitors C_{4b} and C_{3b} are essentially paralleled by means of switches S_{4b}, S_{3p} and S_{4p}. Analysis of transients present during mode change are described in future sections of this dissertation. Operating state (iv) essentially parallels capacitors C_{3a} and C_{4a} by means of switches S_{4a}, S_{3n} and S_{4n}. At the same time, a path for energy transfer between V_{in} and C_{4a} exists through S_{4a}, S_{3a}, C_{2a}, S_{2p} and S_{4n}. The trace impedance limits the transient over-shoot in current occurring during the paralleling interval in both these cases. By continuously switching between operating states (iii) and (iv) for a duration of 50% in each switching cycle, capacitors C_{4a} and C_{4b} are discharged until they reach a voltage close to that of capacitors C_{3a} and C_{3b}. If the converter is

set at stage (b) during steady state operation, a fixed voltage gain of 6 can be achieved. From the operating state (iii) in Figure 2.4 (b), it can be observed that in steady state, capacitors C_{3b} and C_{4b} undergo charging (teal colored arrow) from two parallel input paths enabled by switches S_{3p}, S_{4p}, S_{3b} and S_{4b}. During the transients, the individual capacitor voltages will undergo transitions from the steady state value. The colored arrow represents the charge/discharge states for the capacitors once the voltages have been established. Methods to determine the transient mode currents are described in future sections of the dissertation. On similar lines, the capacitors C_{3a} and C_{4a} are represented by purple colored arrows indicating that they undergo a net discharge. They essentially two parallel load discharge paths. The path for discharge for C_{3a} is through the body diode of switch S_{4a} into the load. The body diodes across switches S_{4b} and S_{4a} ensure that the voltages across capacitors in arms 3 and 4 are balanced by automatically clamping in the event of a voltage unbalance.

Stage (c)

Transition from stage (b) to (c) occurs when a gain "shift-down" operation from 6 to 4 is initiated. Stage (c) comprises of two alternating states (v) and (vi), each lasting for 50% duration in a switching period. These operating states are illustrated in Figure 2.4 (c). When Stage (v) commences, the switching states in arms 3 and 4 are identical to the switching states of the switches in arm 2. The switching states of switches in legs 3 and 4 are identical to those of the switches in leg 2. This essentially connects capacitors C_{2b}, C_{3b} and C_{4b} in parallel. In state (vi), capacitors C_{2a}, C_{3a} and C_{4a} are all essentially paralleled. By continuously switching between operating states (v) and (vi), the voltage across capacitors C_{4a}, $C_{4b,}$ C_{3a} and C_{3b} reach a value close to voltage across C_{2a} and C_{2b} ($2V_{in}$). Thus, at steady state, operating in stage (c) leads to a voltage gain of 4.

2.3.2 Load independent gain "shift-up"

Transitioning from stage (c) to (a) in Figure 2.4 results in a "shift-up" from a gain of 4 to a gain of 8. The sequence of stages is the reverse of the sequence used for "shift-down" described before. The operating states within each of the stages remains the same as that described for "shift-down".

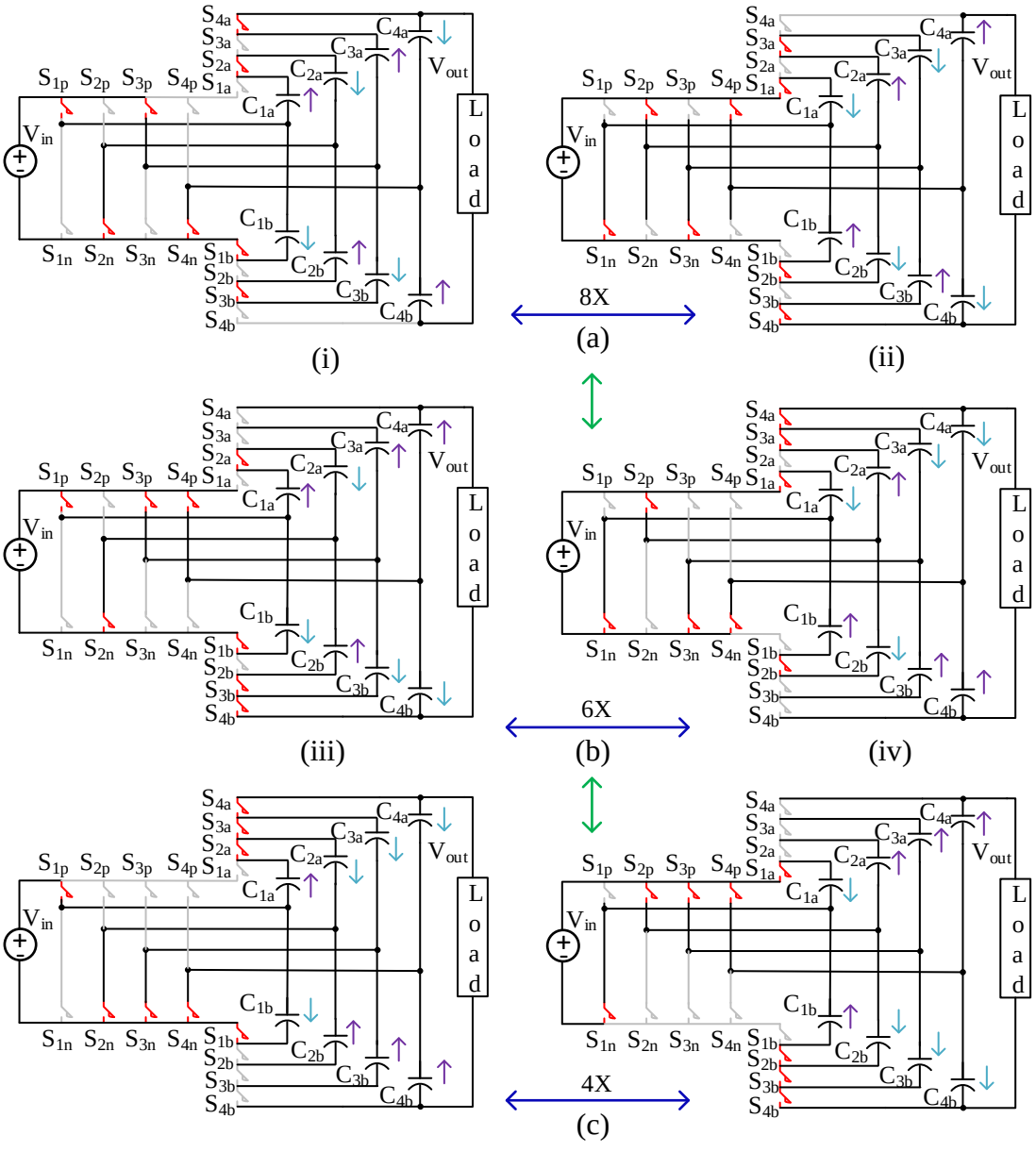


Figure 2.4: Operating states for load independent "shift-up" and "shift-down" in voltage gain.

This section describes the brief trajectory of all the operating states involved for the load-independent gain shift from 8 to 4 and back to 8. Detailed analysis of currents and voltage during transition along with equivalent circuits for each mode transition are described in future sections. While the energy loss during paralleling of capacitors with large voltage differences can affect the instantaneous efficiency, the converter can still be designed for high overall efficiency. The overall design of the converter to withstand transient conditions during mode change and achieve high overall efficiency forms an important aspect. This is described in Section 2.5. Experimental results for the load independent gain shift on a 1-kW prototype are presented in Section 2.7.

2.4 Equivalent Circuit and Transient Currents during Load- Independent Mode Change

In this dissertation, transient mode is defined as the time duration between initiation of mode change (from current gain level) and the time taken to reach the new steady state (to new gain level). Analysis of the circuit in transient mode is an important step in determining the transient voltage and currents through individual switches. In order to simplify the transient mode analysis, the simplified equivalent circuits for every such mode transition are first derived based on the operating states in Figure 2.4. Equations determining the transient current through the switches in each mode are then determined. The transient over-voltage across each switch is dependent on the transient current through each switch (described in Section 2.5). For this analysis, the steady state capacitor voltage ripple is ignored as it is much smaller than the capacitor voltage ripple in transient mode. The equivalent circuit also provides the charge/discharge paths for each of the capacitors involved.

2.4.1 8X to 6X Mode Transition

The different current loops present during this mode change are illustrated by means of simplified equivalent circuit in Figure 2.5 (a)-(h). This is based on the loops present in operating states (iii) and (iv) of Figure 2.4. The equivalent circuits in Figure 2.5 (a)-(d) represent operating state (iv) of Figure 2.5. The equivalent circuits in Figure 2.4 (e)-(h) represent operating state (iii) of Figure 2.5. As the converter alternates between operating states (iii) and (iv) with a duty cycle of 50% every switching cycle, the charge/discharge paths for individual capacitors also alternate. The initial conditions for the voltages across individual capacitors are determined by operating states (i) and (ii) of stage (a) in Figure 2.4. It is assumed that the converter is in steady state operating in 8X mode (stage (a)) before a mode change is initiated. The initial capacitor voltage (before start of transient mode) is marked in parenthesis on each of the capacitors. The inductance and resistance of the loop are labeled as R_{lj} and L_{lj} respectively, where $'j'$ represents the loop under consideration. R_{lj} and L_{lj} can be determined by summing the resistance and inductance along the length of the loop respectively. R_{lj} would typically include the ON state resistance of the conducting switch, R_{Sn}, resistance of the trace, R_{trace} and ESR of the capacitors. L_{lj} would typically include the inductance of the trace, L_{trace} and the ESL of the capacitors. The instantaneous capacitor voltages are determined by individual loop dynamics. In order to achieve a compact design at high efficiency, it is desired to select devices that ensure underdamped response in each loop of the switched capacitor converter **[**42]. Since, this is also the goal for the converter design in this chapter (discussed in future sections), the analysis in this section is performed considering underdamped response in each of the current loops. The expression for current for a second order under-damped system such as in Figure 2.5 (a), can be expressed as,

$$i_{lj}(t) = \frac{V_d}{L_{lj}} * \frac{1}{\omega_{lj}} e^{-\alpha_{lj}t}\, Sin\left(\omega_{lj}t\right). \qquad (2.7)$$

where, V_d is the initial voltage difference in the loop, $\alpha_{lj} = \frac{R_{lj}}{2L_{lj}}$;

ω_{lj} represents the resonant frequency of the j^{th} loop given by,

$\omega_{lj} = \sqrt{\frac{1}{L_{lj}C_{lj}} - \alpha_{lj}^2}$ and C_{lj} represents the overall loop capacitance.

It is assumed that the converter is in steady state prior to initiation of mode change. The steady state current in every loop is ignored for this analysis. So, for all the loops, a zero initial current condition is used.

For loop 1 illustrated in Figure 2.5 (a),

$$R_{l1} = R_{S1a} + R_{S1n} + R_{trace} + ESR_{C1a};\ L_{l1} = L_{trace} + ESL_{C1a};\ C_{l1} = C1a;\ V_d = V_{in};$$

Where, R_{Sn} represents the $R_{DS(ON)}$ of switch n.

On similar lines, the parameters for loops 2 and 3 can be determined by the following set of equations:

$$R_{l2} = R_{S2p} + R_{S3a} + R_{S3n} + R_{trace} + ESR_{C2a} + ESR_{C3a};\ C_{l2} = \frac{C_{2a}C_{3a}}{C_{2a} + C_{3a}};\ L_{l2}$$

$$= L_{trace} + ESL_{C2a} + ESL_{C3a};$$

$$R_{l3} = R_{S3n} + R_{4n} + R_{S4a} + R_{trace} + ESR_{C3a} + ESR_{C4a};\ L_{l3} = L_{trace} + ESL_{C3a} + ESL_{C4a};\ C_{l3} =$$

$$\frac{C_{3a}C_{4a}}{C_{3a}+C_{4a}};\ V_d = V_{in}.$$

This method is then extended to obtain the loop parameters for each of the ten loops presented in Figure 2.5 (a) through (h). In order to estimate the maximum transient current through the switches, the transient current in each of the loops is evaluated. By computing the current through loops i_{l1} through i_{l10}, it can be determined that i_{l3} and i_{l9} have the highest magnitude compared to the other loops present. This is primarily due to large initial voltage difference V_d when compared to other loops. In a modular design of the (n/m)X converter, all the capacitances ($C_{1a} \ldots . C_{4b} = C$) and the

trace impedances are identical. Hence, i_{l3} and i_{l9} are also identical. The maximum current through the switches can then be estimated by computing one of the two symmetrical branch currents. In the case of 8X to 6X mode transition, the maximum transient current is expected to be along i_{b2} and i_{b4} computed using the following expression, $i_{b2} = i_{b4} = i_{l3} + i_{l4} = i_{l9} + i_{l10}$.

The exact values for i_{b2} or i_{b4} can be derived using Equation (2.7) for a given set of device parameters. In Figure 2.5 (h), i_{b4} represents the current in the path between capacitors C_{4b} and C_{3b}. Mapping this current path to the operating state (iii) in Figure 2.4 (b), it can be observed i_{b4} represents the current through switches S_{4b}, S_{3p}, S_{4p}. On similar lines, by mapping current i_{b2} in Figure 2.5 (b), to the operating state (iv) in Figure 2.4 (b), it can be observed that i_{b2} is carried by switches S_{4a}, S_{3n}, S_{4n}. Thus, the above-mentioned switches are expected to have the highest current transient during the 8X to 6X mode change. In order to achieve a modular design, all the switches in the circuit must be designed to withstand the highest transient current across all mode changes. In order to determine the worst-case transient current across all mode changes, the current loops present during other mode changes are all determined. In order to simplify the analysis, only the loops where both conditions, $C_l \geq \frac{C}{2}$ and $V_d \geq V_{in}$ are considered in determining the transient current in other mode changes.

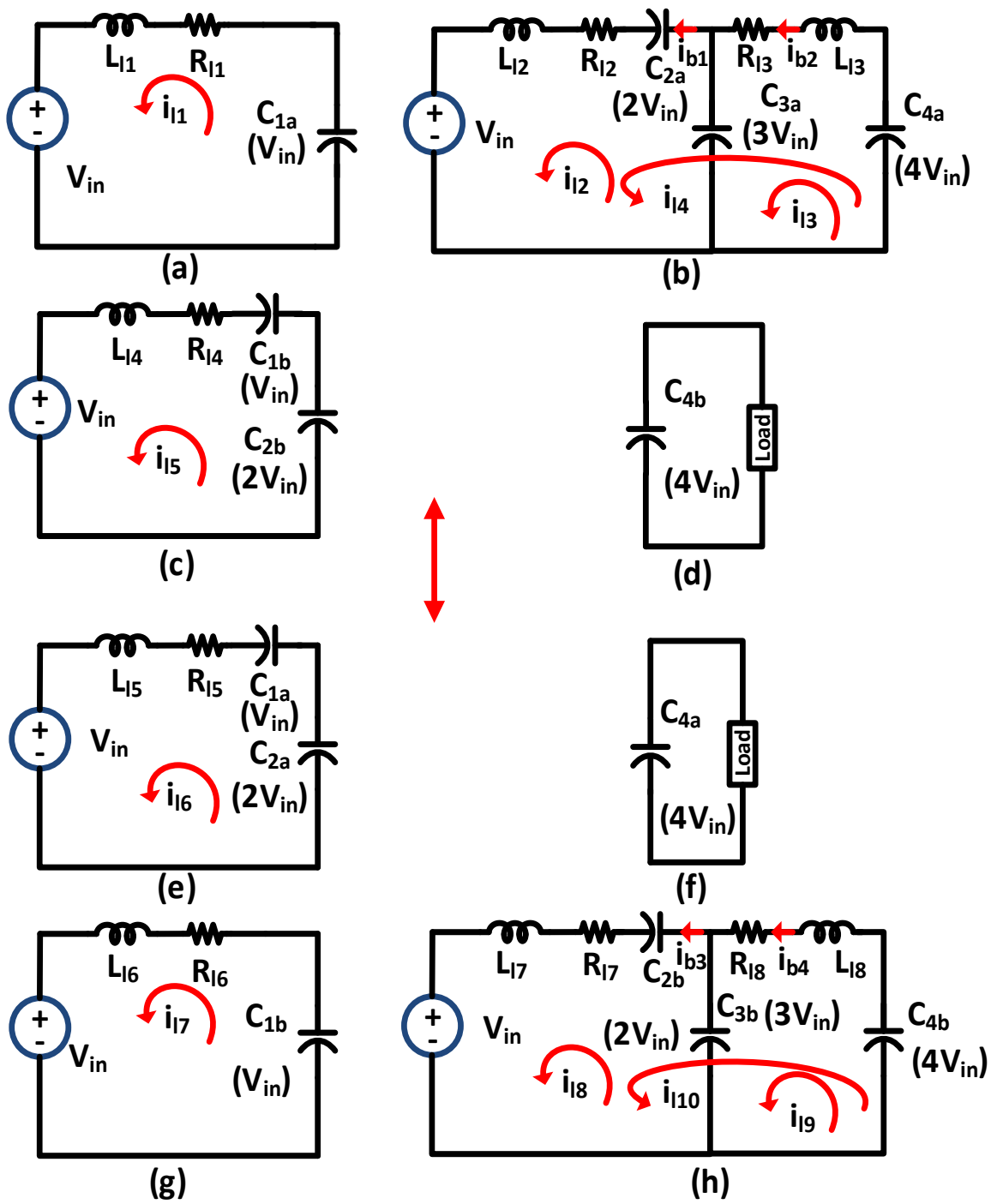


Figure 2.5: Transient current loops during 8X to 6X mode transition.

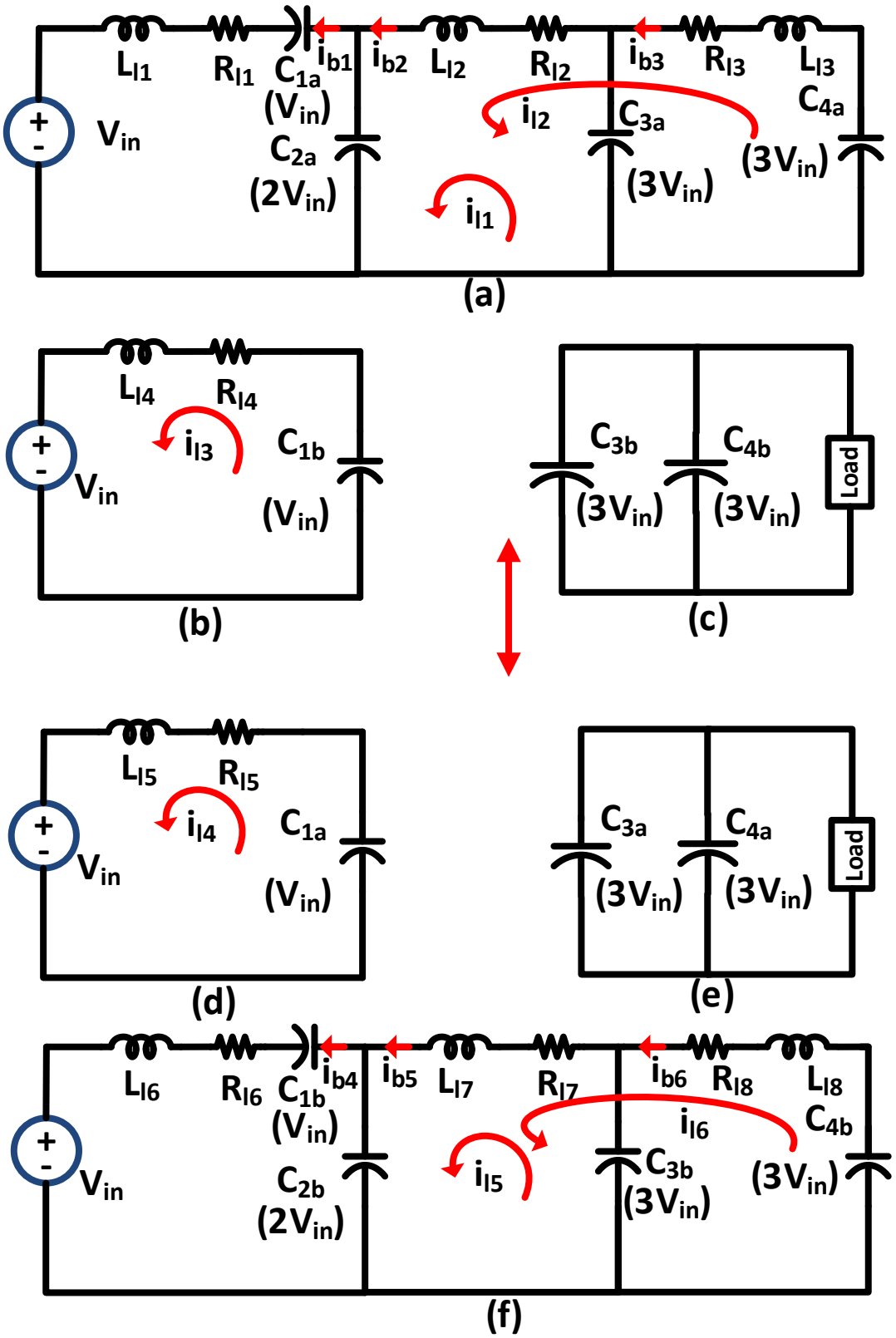


Figure 2.6: Transient current loops during 6X to 4X Transition.

2.4.2 6X to 4X Mode Transition

Figure 2.6 (a) through (f) illustrates the charging and discharging paths present for each of the capacitors during transition from 6X to 4X mode. These loops correspond to the operating states (v) and (vi) in Figure 2.4. The equivalent circuits in Figure 2.6 (a)-(c) represent operating state (v) in Figure 2.4 (c). The equivalent circuits in Figure 2.6 (d)-(f) represent operating state (vi) in Figure 2.4 (c). The initial conditions for the voltages across individual capacitors are determined by operating states (iii) and (iv) of stage (b) in Figure 2.4. As discussed above, loops with equivalent capacitance, $C_{eq} \geq \frac{C}{2}$ and $V_d \geq V_{in}$ have been marked. In loops 1, 2, 5 and 6, $C_l = \frac{C}{2}$ and $V_d = V_{in}$. This causes the estimate for the highest transient current to be along i_{b2} and i_{b5}. The expression for peak current transient in this mode can be obtained using the following expression, $i_{b2} = i_{l1} + i_{l2}$. Mapping individual branch currents, i_{b2} (Figure 2.6 a) and i_{b5} (Figure 2.6 f) to the operating states (v) and (vi) in Figure 2.4(c), it can be observed that i_{b2} is carried by switches S_{3a}, S_{3n} and S_{2n}. i_{b5} is carried by switches S_{3b}, S_{3p} and S_{2p}. Thus, the above-mentioned switches are expected to carry the largest transient current in this mode of operation. The overall expression for the transient current can then be determined using Equation (2.7).

2.4.3 4X to 6X Mode Transition

Figure 2.7 (a) through (h) illustrates the charging and discharging paths present for each of the capacitors during the 4X to 6X mode change. This translates to the various loops present in operating states (iii) and (iv) of stage (b) in Figure 2.4. The equivalent circuits in (a)-(d) represent the current paths in operating state (iv) of Figure 2.4 (b). The equivalent circuits in Figure 2.7 (e)-(h) represent the current paths in operating state (iii) of Figure 2.4(b). Since this is a case of "shift-

up" operation, the initial conditions for the voltages across individual capacitors are set by the operating states (v) and (vi) of stage (c) in Figure 2.4.

Using the same method of analysis used for "shift-down" operation, the branch/loop with the largest transient current is identified, considering loops with $C_l \geq \frac{C}{2}$ and $V_d \geq V_{in}$, $\mathrm{i_{b1}} = \mathrm{i_{l1}} + \mathrm{i_{l2}}$ and $\mathrm{i_{b2}} = \mathrm{i_{l3}} + \mathrm{i_{l4}}$ are expected to have the highest transient current magnitude for this mode change. The overall expression for maximum current transient in this mode can then be determined using Equation (2.7). From, operating state (iv) of Figure 2.4 (b) and Figure *2.7* (b), it can be seen that $\mathrm{i_{b1}}$ maps to current through switches $\mathrm{S_{2p}}, \mathrm{S_{3a}}, \mathrm{S_{3n}}$.

2.4.4 6X to 8X Mode Transition

Figure 2.8 (a) through (j) illustrates the several charging and discharging paths present for each of the capacitors during transition from 6X to 8X modes. This translates to the various loops present in operating states (i) and (ii) of stage (a) in Figure 2.4. The equivalent circuits in Figure 2.8 (a)-(e) represent the current paths in operating state (ii) of Figure 2.4. The equivalent circuits in Figure 2.8 (f)-(j) represent the current paths in operating state (i) of Figure 2.4. Since, this also represents a case of "shift-up" operation, the initial conditions for the voltages across individual capacitors are determined by the operating states (iii) and (iv) of stage (b) in Figure 2.4. It can be observed that $\mathrm{i_{l1}}$ and $\mathrm{i_{l2}}$ are the largest transient currents in this mode. From operating state (ii) of Figure 2.4(a) and Figure 2.8(e), it can be seen that $\mathrm{i_{l1}}$ maps to current through switches $\mathrm{S_{3n}}, \mathrm{S_{4b}}, \mathrm{S_{4p}}$. From operating state (i) of Figure 2.4 (a) and Figure 2.8(j), it can be seen that $\mathrm{i_{l2}}$ maps to current through switches $\mathrm{S_{3p}}, \mathrm{S_{4a}}, \mathrm{S_{4n}}$. Based on the equivalent circuit-based analysis this section, a script file is developed to compute the worst-case transients during all mode changes. This is used to estimate the worst-case transient current through the switches. In the next section, the relation between the

worst case transient current and the transient over-voltage rating of the switches will be derived. The results obtained using actual device parameters are presented in Section 2.6.

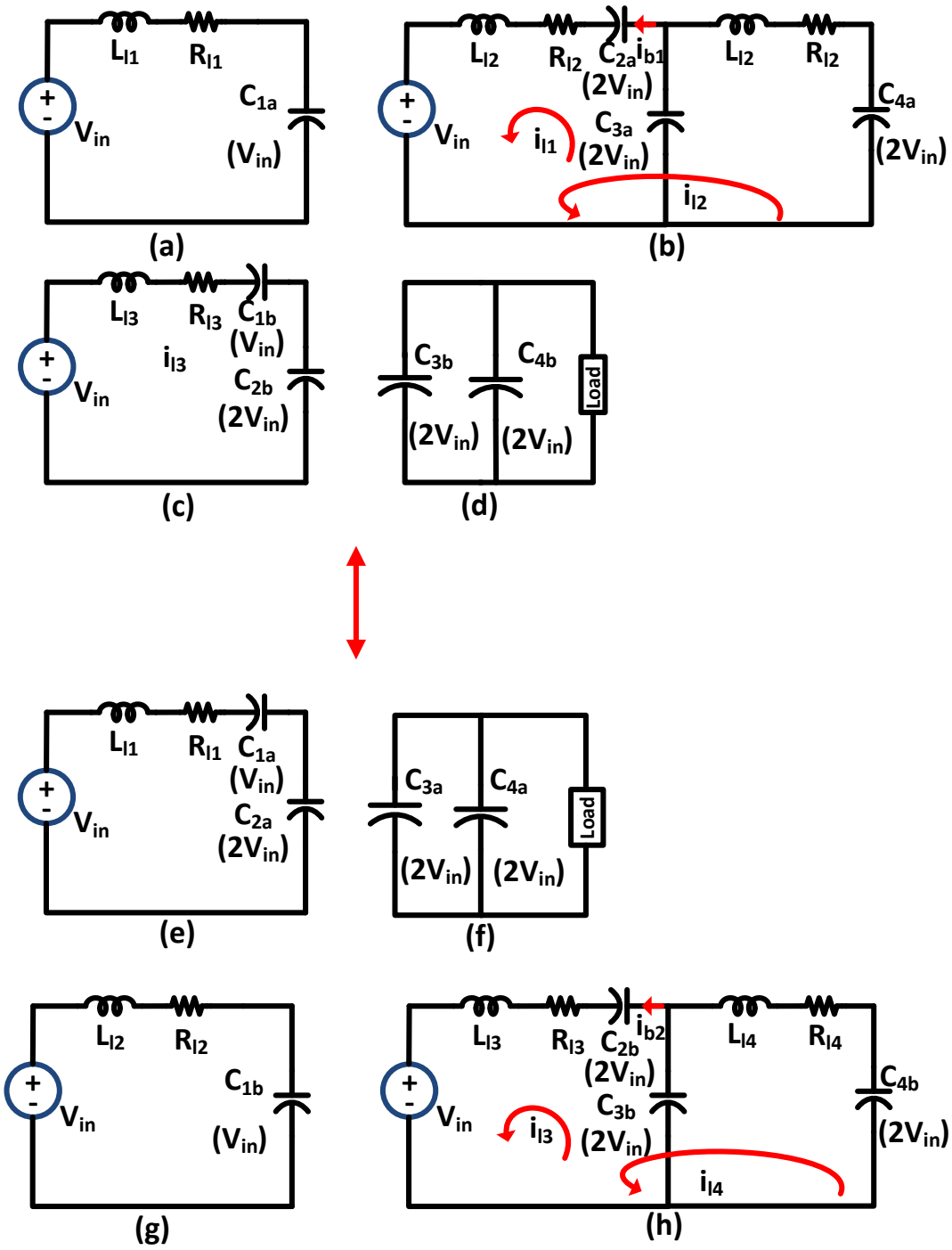


Figure 2.7: Transient current loops during 4X to 6X Transition.

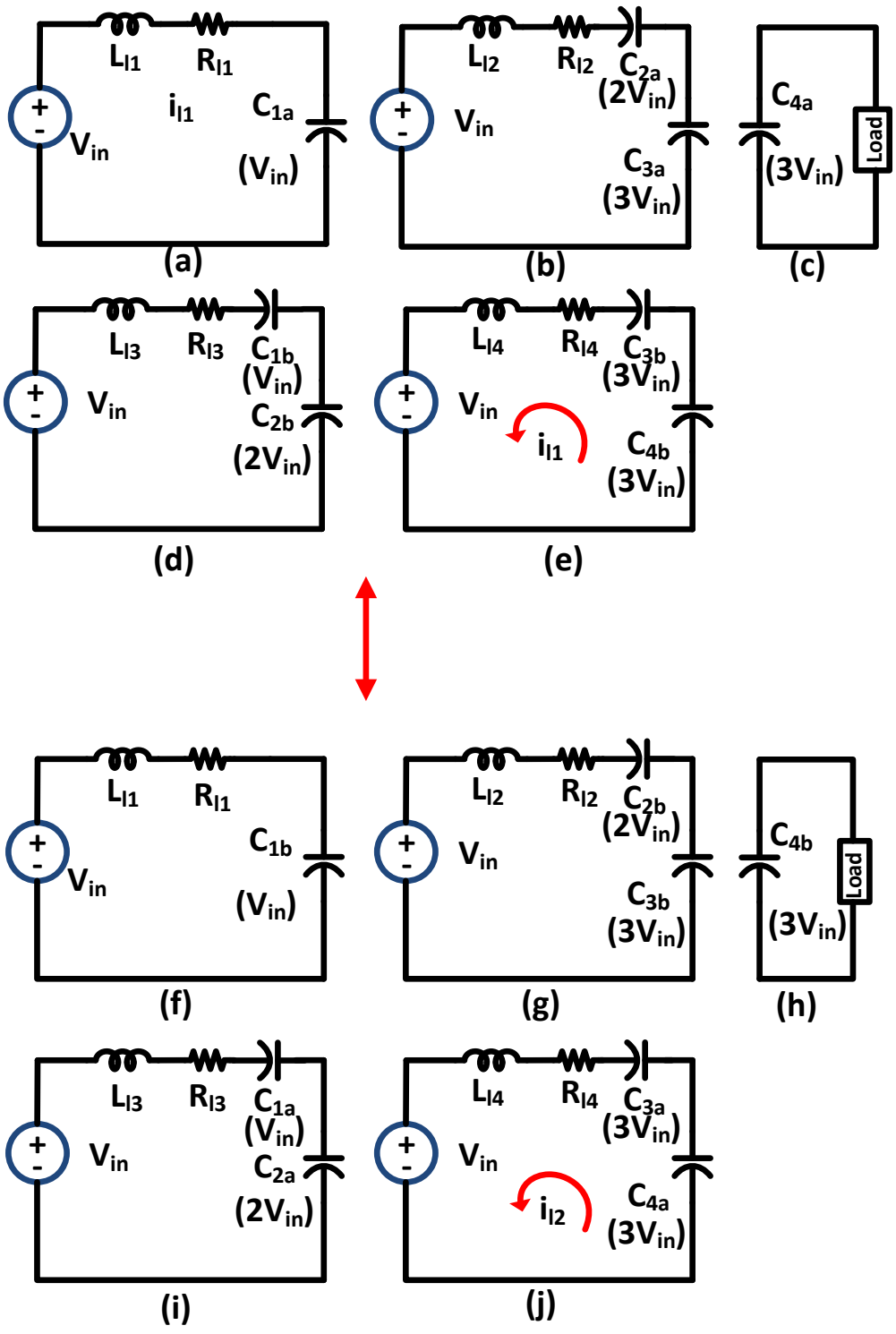


Figure 2.8: Transient current loops during 6X to 8X Transition.

2.5 Transient over-voltage analysis

In steady state operation of a modular nX converter, switches with two different voltage ratings of V_{in} and $2V_{in}$ are selected. This is described in [43]. For an (n/m)X converter with variable voltage gains, the peak voltage ratings of the switches are also influenced by the current transients. This section elaborates on this influence and expressions for peak voltage ratings of the switches are derived. Figure 2.9 illustrates the circuit schematics of the (4/0.5)X converter with the inductance in every path lumped into two different inductors, L_T (red) and L_M (blue). The switches are represented by means of IGBT and an anti-parallel diode as an example only. They can be replaced other switches depending on the application. In order to determine the peak voltage transient during a mode transition, the inductor current path during the dead-time of the switches needs to be considered. The dead-time interval is the period in which all the switches are OFF during transition from one operating state to another. Figure 2.10 (a) illustrates the inductor current path in arms 3 and 4 during operating state (iv) when it has just transitioned from stage (a) to (b) in Figure 2.4. Figure 2.10 (b) illustrates the inductor current path in arms 3 and 4 during transition from state (iv) to (iii) in Figure 2.4. During this interval, all the switches are OFF due to the dead-time necessary to prevent a shoot-through state. The diodes shown in red are conducting. As this analysis only concerns arms 3 and 4, the current paths in other arms are marked in grey. In Figure 2.10 (a), the initial conditions for the voltages across individual capacitors are determined by stage (a) (Figure 2.4). In this case, the current through L_{M3} is equal to the current through L_{M4}, L_{T4a} and L_{T3a} as all of them form one series path. It can also be seen that there is no current through L_{T3b} and L_{T4b}. In Figure 2.10 (b), all the switches are turned OFF. The diodes across S_{3p}, $S_{4n}$and S_{4b} conduct in order to provide a freewheeling path for the current through inductors L_{M3} and L_{M4}.

The current path is marked as shown in the Figure. This leads to a sudden voltage transient, V_{LT3b} and V_{LT4b} across inductors L_{T3b} and L_{T4b}, given by the following expression,

$$V_{LT3b} = V_{LT4b} = L_{T3b}\frac{i_{L_{T3}}}{t_{off}} = L_{T4b}\frac{i_{L_{T4}}}{t_{off}}. \qquad (2.8)$$

Here, t_{off} is the switch turn-off time, i_{LT3} and i_{LT4} are the currents through L_{T3} and L_{T4}, respectively prior to switch turn-off.

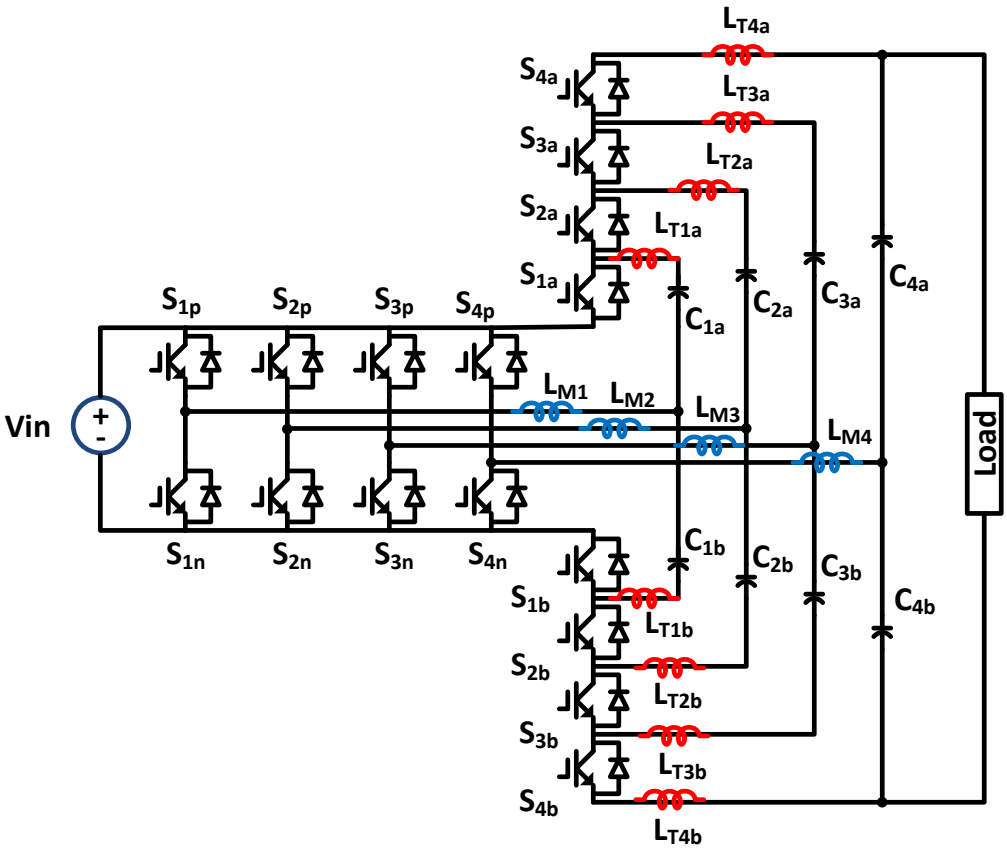


Figure 2.9: (4/0.5)X Converter with lumped trace inductances.

During the dead-time, current through inductor L_{T3a} ideally has a free-wheeling path through C_{3a}, C_{3b}, L_{T3b}, L_{T3a}, diode S_{3b}, C_{2b}, C_{2a} and diode S_{3a}. But, the current through L_{T3b} has already been established by inductors L_{M3} and L_{M4}. This would lead to a transient over-voltage, V_{LT3a} across L_{T3b} given by the following expression,

$$V_{LT3a} = L_{T3a}\frac{1}{t_{off}}(0 - i_{LM3}) \qquad (2.9)$$

On similar lines, transient over-voltage across L_{4a},

$$V_{LT4a} = L_{T4a}\frac{1}{t_{off}}(0 - i_{LM4}). \qquad (2.10)$$

The transient over-voltage across switch, S_{4a} (not considering the DC voltage across individual capacitors), V_{S4at}, can then be represented as,

$$V_{S4at} = V_{LT4a} + V_{LT4b} - V_{LT3a} - V_{LT3b}. \qquad (2.11)$$

In a modular design, $L_{T3a} = L_{T3b}$, $L_{T3b} = L_{T4b} = L_T$, equation (2.11) can be simplified to the following expression,

$$V_{S4at} = 2L_{T4a}\frac{i_{LT4}}{t_{off}} + 2L_{T3a}\frac{i_{LT3}}{t_{off}}. \qquad (2.12)$$

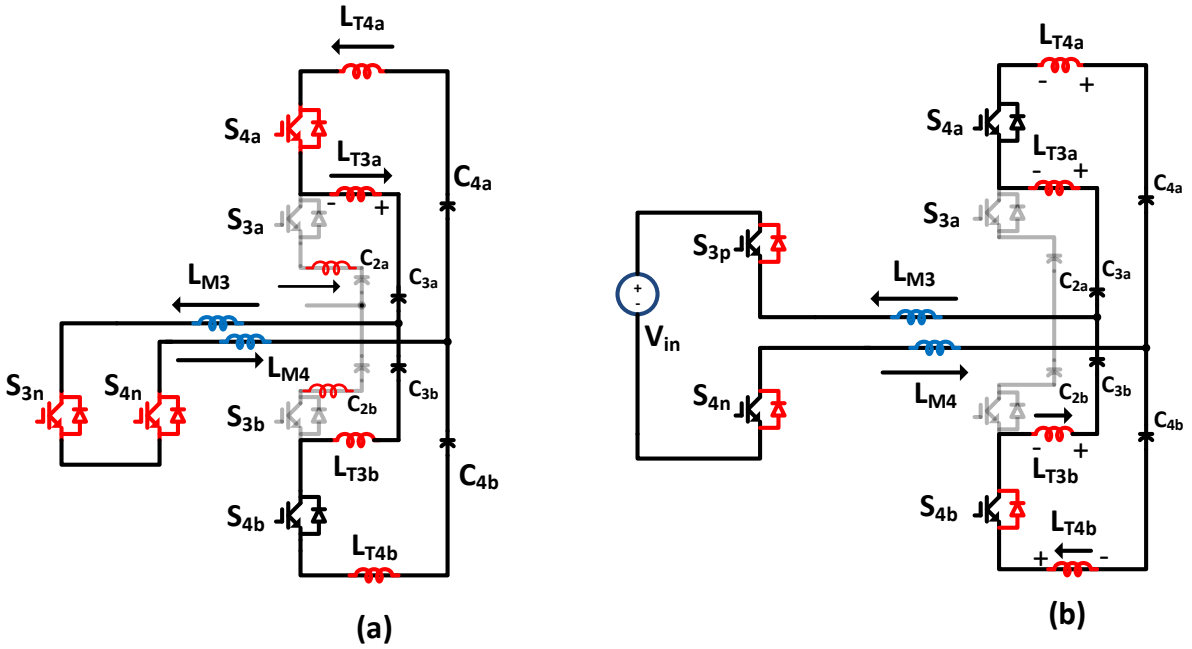


Figure 2.10: (a) Inductor Current path during load during operation in 6X mode (Load independent), (b) Inductor current path during dead-time interval of 6X mode (Load-independent).

From Equations (2.11) and (2.12), it can be seen that, the transient over-voltage across the switch depends on the current through L_T. The worst-case voltage transient across switch S_{4a} is expected

when the current i_{LT4} is the highest. So, for every operating state, the peak voltage across a switch can be determined this way as described in the equations below.

$$V_{S3at} = 2L_{T3a}\frac{i_{LT3}}{t_{off}} + 2L_{T2a}\frac{i_{LT2}}{t_{off}}$$

$$V_{S2at} = 2L_{T2a}\frac{i_{LT2}}{t_{off}} + 2L_{T1a}\frac{i_{LT1}}{t_{off}}$$

Here, i_{LT2} and i_{LT1} are the currents through L_{T1} and L_{T2} prior to dead-time respectively.

The worst-case transient voltage across a switch, V_{WT} can be determined by using the following approximation, $V_{WT} = 4L_T\frac{i_{LT}}{t_{off}}$ where, i_{LM} represents the worst-case transient current across all mode changes. The peak voltage rating of the arm switches, $\hat{S}_V$ can then be approximated by the following expression,

$$\hat{S_V} = 2V_{in} + 4L_T\frac{i_{LT}}{t_{off}}. \qquad (2.13)$$

The over-voltage transient can be minimized by distributing all the trace inductance along L_M and a minimum trace inductance along L_T. This forms an important design parameter for minimizing the voltage transient across individual switches of the (n/m)X converter.

2.6 Design and Specifications of an (N/M)X Converter Prototype

The block diagram of a typical low-voltage converter/inverter system is illustrated in Figure 2.11. The input voltage and load specifications of an example converter/inverter system are illustrated in Table 2.1. For such a system, using a variable gain (n/m)X converter in place of the nX converter [43] can result in significant reduction in the DC-voltage link of the inverter stage for the same input voltage and load specifications. To provide a fair comparison, the same specification as the PV converter/inverter system in [43] is used here. In order to achieve an AC output voltage of 120 V at the load in Figure 2.11, a minimum inverter DC link voltage of 170 V is required. For an nX based DC-DC converter, the fixed gain of the converter is selected based

on the minimum input voltage. For V_{imin} of 25 V, a minimum gain of 8 is necessary to achieve V_o =170 V. This leads to a maximum output voltage, $V_{out(max)}$ of 400 V for V_{imax} of 50 V.

Range of input voltage,Vin	25 to 50 V (V_{imin} to V_{imax})
Maximum load power (P_m)	1-kW
Load AC voltage, V_0	120 V AC single - phase

Table 2.1: Input and load specifications of an example converter/inverter system.

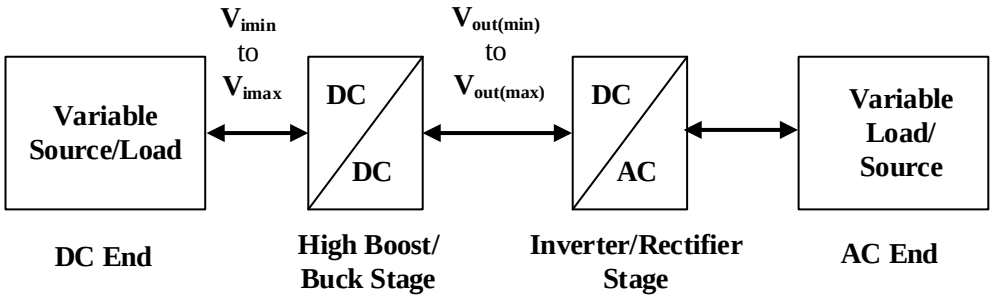


Figure 2.11: Block diagram of an example converter/inverter system.

The switches in the inverter stage following an nX converter have to then be rated for 400 V. In the proposed (n/m)X converter, the voltage gain can be shifted dynamically. If the gain is shifted depending on magnitude of input voltage, according to the example shown in Table 2.2, $V_{out(max)}$ is limited to 264 V for the same variation in input voltage. The output voltage variation for the whole range of input voltage is illustrated in Figure 2.12. Since the output voltage of the (4/0.5)X converter is about 35% lower than the maximum output voltage of the 8X converter, the voltage stress on the inverter switches are also reduced by the same margin. This is a key advantage of using (n/m)X converter in a converter/inverter system. By choosing a different (n/m)X converter with more available voltage gains and further optimizing the voltage at which mode changes occur, the inverter voltage stress can further be lowered.

V_{in}	Voltage gain	V_o
25 to 30 V	8	200 to 240
31 to 44 V	6	186 to 264
45 to 50 V	4	180 to 200

Table 2.2: Gain selection based on input voltage variation in a (n/m)X converter.

The proposed variable (n/m)X converter can be used for several different applications that have a wide varying input voltage/output voltage requirement such as power systems within a PV based converter/inverter system, more electric aircrafts, EV/HEV powertrains and other battery based systems that require a variable input/output voltage at high gains.

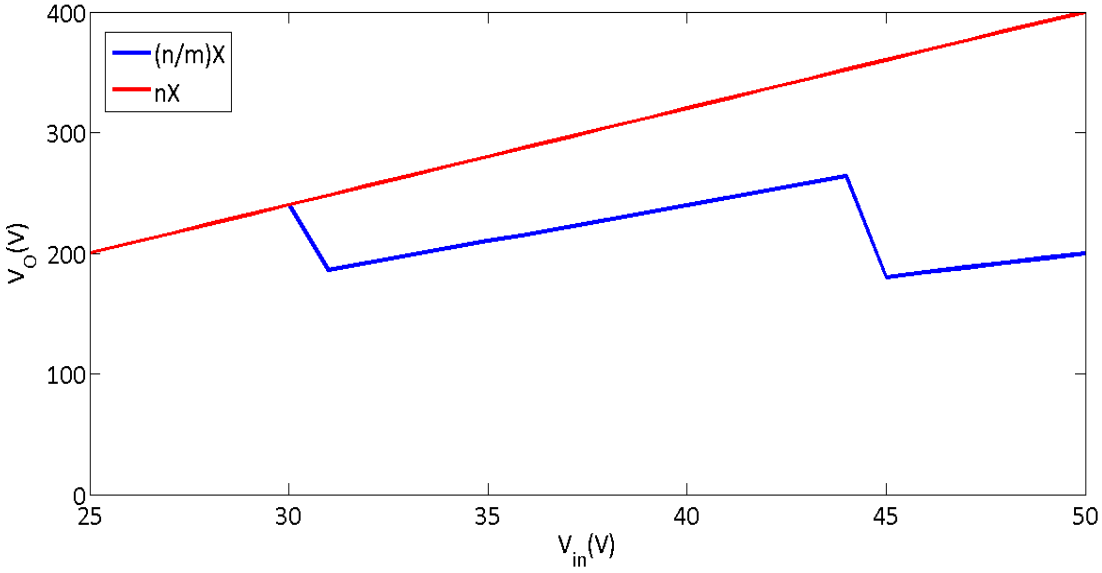


Figure 2.12: Output voltage of DC-DC converter stage, V_o for an input voltage of V_{in} in a nX and (n/m)X converter.

2.7 Experimental Prototype

In order to validate the proposed theory and configuration, a 1-kW prototype of the (4/0.5)X converter is developed for the specifications described in Table 2.1. Using the prototype, the ability to achieve different fixed fractional voltage gains by changing the location of the input voltage (offline) is first demonstrated. Next, the load-independent method to achieve both "shift-up" and "shift-down" are demonstrated by shifting the gains at voltage levels described in Table *2.2*. The

block diagram of the overall experimental setup is illustrated in Figure 2.13. A 3-phase variac based, V_{ac} is rectified and filtered to achieve the DC input voltage, V_{in}. The variac position is varied in order to achieve a variable DC input voltage to the converter. The load is a variable resistance bank rated for a maximum power of 1 kW.

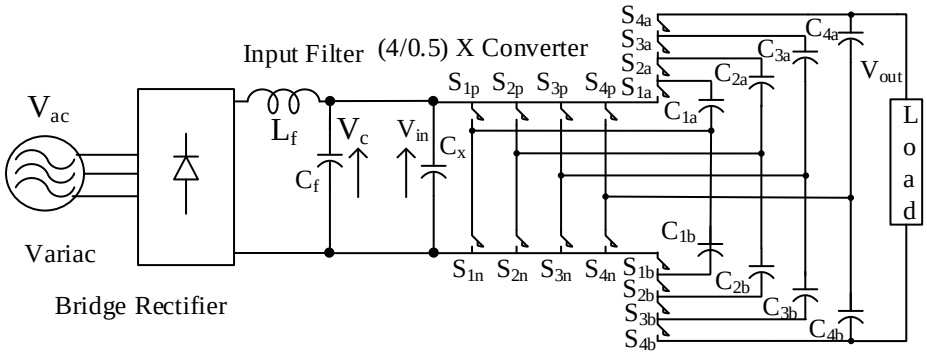


Figure 2.13: Block Diagram of the overall experimental setup.

In the experimental setup, there are a total of 16 switches. In order to simplify the gate drive requirement, the switches along the legs of the converter, S_{1p},S_{1n}….S_{4p},S_{4n} use a bootstrap half-bridge driver for each pair. The switches along the arms of the converter, S_{1a}, S_{1b} through S_{4a}, S_{4b} use individual isolated single channel gate drivers. So, overall 4-half bridge drivers and 8 isolated single channel gate drivers are used. The isolated power supply required for each individual switch is derived using individual isolated power supply ICs on the board. The gate drive structure used in this prototype is just one of the implementations possible for this structure. It can be replaced with other types of gate driver structures that suit the application. Figure 2.14 shows the photograph of the overall experimental prototype. The gate pulses from the DSP are transmitted onto the gate driver board by means of optical fibers. At the gate driver board, the optical signal is first converted to electrical pulse and fed to the individual gate driver ICs. The gate driver board is stacked directly below the power board. The other components of the overall setup are labeled in the figure.

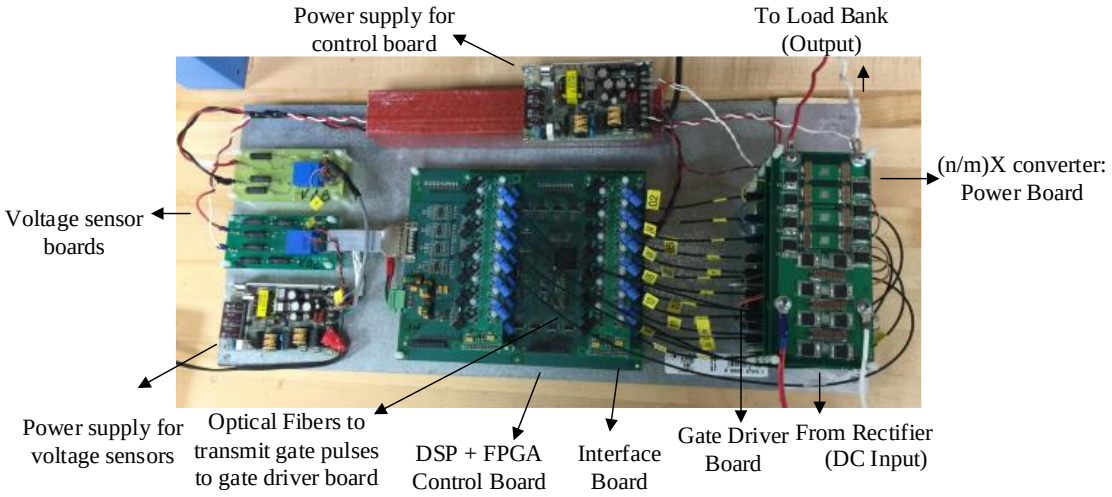


Figure 2.14: Photograph of the overall experimental setup.

2.8 Design of a variable (4/0.5)X converter

The need to achieve variable voltage gain using the (4/0.5)X converter imposes more constraints on the design (due to transients) when compared to the nX converter. In this chapter, the design is based on a two-step procedure. First, the converter is designed based on the steady state requirements. Next, the worst-case transient over-voltage, over-currents and transient energy pulse are computed using the parameters of selected devices. If the devices are able to handle the worst-case transients, no change is made to the device selection. If not, the trace inductance and the switching frequency are altered to achieve the required transient performance. This process is done iteratively until all transient specifications are satisfied. The important constraints in a modular design for steady state are listed below:

1. Low ripple voltage on individual capacitors to achieve high efficiency
2. High switching frequency to minimize size of capacitors and trace inductors
3. Loop inductance and resistance designed to ensure a resonant frequency close to switching frequency in every loop
4. Device parameter selection to ensure underdamped response for current in every loop.

Based on these constraints, the following choices are made for the switches and capacitors in the converter limbs.

Parameter	Type
Arm Capacitors	C5750X7T2E225K. (6 in parallel)
Arm Switches	IPB036N12N3G
Leg Switches	IPB017N06N3G
Switching Frequency	200 kHz
Loop inductance in V_{in}, C_{1a}/C_{1b} loop	180~200 nH

Table 2.3: Component/ Parameter selection based on steady state operation of (4/0.5)X converter.

Using these device parameters, the worst-case transient currents during mode changes occurring in accordance with Table 2.2 are computed. For the selected device parameters, a MATLAB script is developed to determine the worst-case transient current, over-voltage, duration of the transient and estimated worst-case energy delivered by the source. Based on the calculations, the worst-case transient current is found to occur during the mode transition from 4X to 6X mode. Figure 2.15 illustrates the calculated worst-case transient current (i_{b1}) based on the equivalent circuit in Figure 2.7(b). The peak current transient is 180 A. A dead-time of 250 ns is selected to ensure that the energy stored in L_M is dissipated before the start of the next switching cycle.

Beyond a duration of $60\mu s$, the current transient is close to the steady-state current rating of the device. So, the duration beyond $60\mu s$ can be neglected for transient analysis.

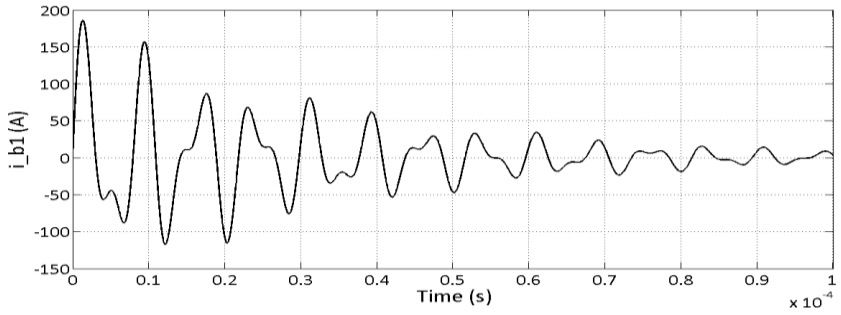


Figure 2.15: Worst- case transient current (Calculated) in (4/0.5)X converter.

Optimized layout to further reduce L_T has the potential to fully eliminate the transient over-voltage. Based on the analysis in Section 2.5, the inductance distribution and device parameters ($t_{off} = 100\ ns$), the worst-case voltage transient across individual switches is calculated to be 160 V (~3*V_{inmax}). As the switches and other components selected in Table 2.3 can handle all of the worst-case transient conditions, the component selection based on Table 2.3 is retained for this design.

2.9 Experimental Results

2.9.1 Fractional output using the (4/0.5)X converter

The experimental results that illustrate the generation of fractional gains (Section 2.3) using the (n/m)X converter are presented in this section. Table 2.4 illustrates the experimental results for input and output voltages for different fractional voltage gains of (4/0.5), (4/1), (4/2) and (4/3) achieved using the (4/0.5)X converter. These gains are obtained by changing the value of 'm' between 0.5 and 3 as illustrated in Figure 2.3. As described before, the location of the input voltage, V_{in} cannot be changed during operation of the converter. For this experiment, the location of the input voltage has been changed offline to demonstrate the possibility of obtaining different fixed

voltage gains using the converter by selecting different locations of the input voltage. The load resistance for all these cases is fixed at 40 Ohms. The average input voltage, V_{in} and average output voltage, V_{out} for each case is marked in each case. The achieved gains show a small drop when compared to the theoretical voltage gains due to the non-idealities in the devices used.

Location of input voltage (m)	V_{in} (V)	V_{out} (V)	Measured Gain (V_{out}/V_{in})	Expected Gain (n/m)
m=0.5, n=4	25.0	195.4	7.82	(4/0.5) = 8
m=0.5, n=4	30.4	238.2	7.83	(4/0.5) = 8
m=1, n=4	25.0	98.7	3.95	(4/1) = 4
m=1, n=4	30.2	118.5	3.92	(4/1) = 4
m=2, n=4	25.1	49.3	1.96	(4/2) = 2
m=2, n=4	30.2	59.5	1.97	(4/2) =2
m=3, n=4	25.3	32.2	1.27	(4/3) = 1.33
m=3, n=4	30.5	40.2	1.31	(4/3) = 1.33

Table 2.4: Experimentally Measured Gains for different location of the input voltage using an (n/m)X converter.

2.9.2 Controller implementation

A feed-forward based control is implemented to achieve dynamic gain shifts based on the magnitude of input voltage. The block diagram for the feed-forward control is illustrated in Figure 2.16. The input voltage, V_{in} and output voltage at load terminal, V_{out} are sensed using voltage sensors. Using the gain-shift specifications in Table 2.3, a look-up table is developed in the DSP controller. Depending on the input voltage, the required gain is determined and the switching sequence for the said gain is generated. If the input voltage V_{in} is rising and V_{in} =30 V, a transition from 8X to 6X is initiated. On the other hand, if the input voltage, V_{in} is falling and V_{in} =29 V, a mode transition from 6X to 8X is initiated. Similarly transition from 6X to 4X and vice-versa are initiated depending on the nature (rising or falling slope) of input voltage and it's magnitude now centered around 44 V (rising) and 43 V (falling). The pulse interface block then converts the switching sequence to gate pulses that are fed to individual gate drivers. A TMS280335 based DSP controller and ALTERA Cyclone III FPGA are used to generate the sequence of pulses necessary for all the switches. LV-25P Hall-effect voltage sensors are used to sense the input and output voltages. The input voltage is sampled every 6 ms and the output voltage is sampled every 10 μs by the ADC within the DSP controller.

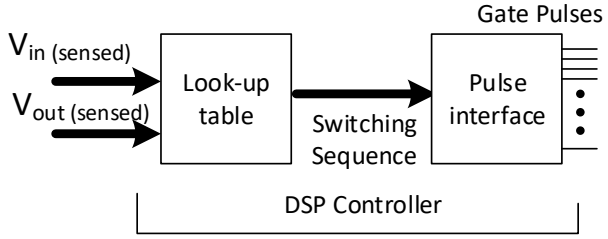


Figure 2.16: Block schematic of the feed forward-control implemented on the prototype converter.

2.9.3 Load independent dynamic mode change

Figure 2.17 (a)-(d) illustrate the waveforms for load independent gain transition from 8X to 6X, 6X to 8X, 6X to 4X and 4X to 6X respectively. All the gain transitions are initiated based on the specifications in Table *2.2* using input feed-forward control described in Figure 2.16. In Figure 2.17 (a), it can be observed that V_{out} (red trace) transitions from $8V_{in}$ to $6V_{in}$ in $25\mu s$ once initiated. The transition in mode change is initiated when the sampled input voltage is rising and V_{in} =30 V (blue trace) The beginning and end times of transition are marked in the waveform by means of red arrows. Once the transition is initiated, it can be seen that the gate-source voltages across switch S_{4a} (V_{GS4a}, orange trace) and the gate-source voltage across switch S_{3a} (V_{GS3a}, green trace) are identical in order to parallel capacitors C_{3a} and C_{4a} (as described in Section 2.3). In Figure 2.17 (b), the transition in output voltage, V_{out} (red trace) from $6V_{in}$ to $8V_{in}$ is initiated when the sampled input voltage V_{in} is decreasing and V_{in} = 29V (blue trace). From the traces representing V_{GS4a} and V_{GS3a}, , it can be observed that these individual gate-source voltages are identical before the mode change in initiated and are complementary, once the mode change is initiated. This verifies the control method proposed in Section 2.3. In Figure 2.17 (c)-(d), the experimental waveforms for transition from 6X to 4X and 4X to 6X are illustrated. The transition from 6X to 4X is initiated when the sampled input voltage, V_{in} is increasing and V_{in}=44V.

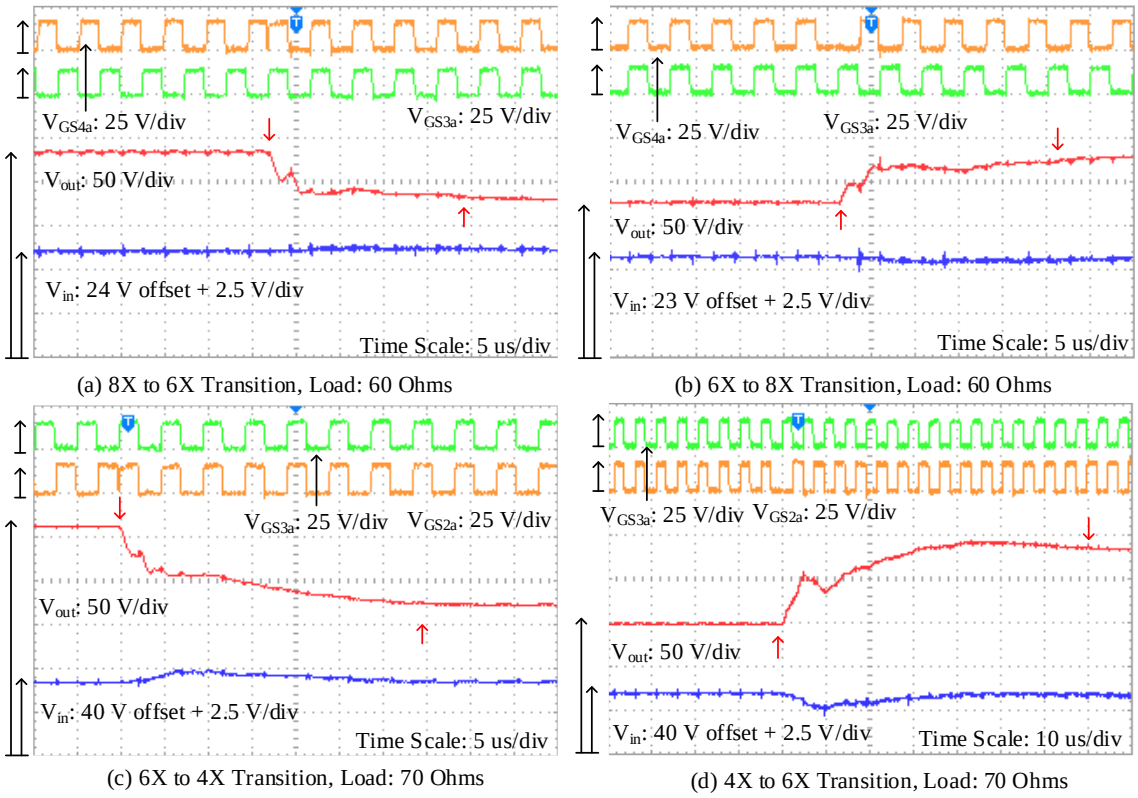


Figure 2.17: Load independent mode change using the (4/0.5)X converter.

The transition from 4X to 6X is initiated when V_{in} is decreasing and V_{in}=43V.The beginning and end times of the transition are marked in the waveform by means of red arrows. The transition times are much lower when compared to the load-assisted mode change for the same load levels. Figure 2.18 illustrates the steady state output voltage at different operating points for input voltage (from 27 to 50V) for three different load conditions. The resistance value is changed for each output voltage to ensure the load power remains the same as the input is varied. The load independent dynamic mode change has been used to achieve these operating points. The curve is an interpolation and does not represent the real slope of output voltage variation in between operating points. The worst-case error between the experimentally observed voltage output and the theoretical output voltage for each input voltage at different loads are shown in Table 2.5.

Figure 2.19 (a)-(d) illustrate the worst -case transient voltage across individual switches and the worst-case transient current through the switches during mode change. The results are obtained for a no-load case to eliminate damping due to load. The currents through inductors i_{LM1} through i_{LM4} are measured using the LEM HC6F300-S current transducer. The maximum switch transient current transient is measured to be 150 A. This occurs during 4X to 6X mode transition. The maximum transient voltage is measured to be 150 V across S_{2b}. This is achieved during 6X to 4X mode transition. The worst case over-current transient exists for close to 25 μs. The achieved transient performance is within the calculated limits in Section 2.8.

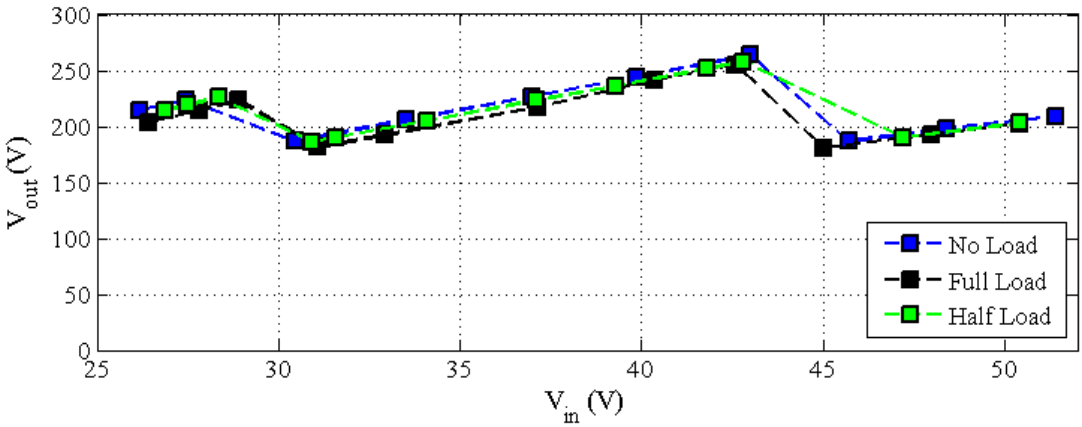
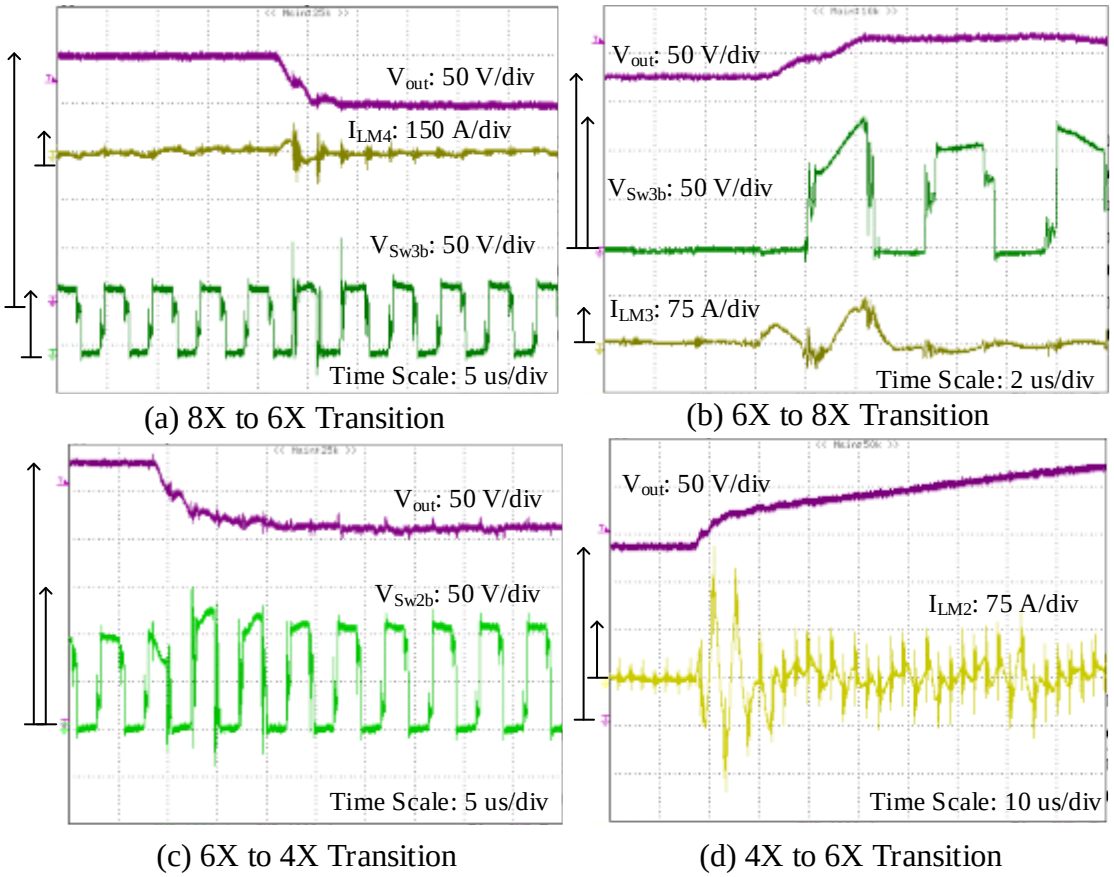


Figure 2.18: Measured output voltage regulation with different loads using load-independent mode change.

Load Level	Maximum Error: $\frac{1}{V_{theoretical}}(V_{theoretical} - V_{experiment})$
Full Load (1kW)	3.7 %
Half-load (500 W)	1.2%
No-Load	0.2%

Table 2.5: Worst-case error between theoretical and experimentally obtained gains for different loads in a (4/0.5)X converter.



(a) 8X to 6X Transition (b) 6X to 8X Transition

(c) 6X to 4X Transition (d) 4X to 6X Transition

Figure 2.19: Transient over-voltage and current during load independent mode change.

2.10 Efficiency analysis of (4/0.5)X Converter

In the load independent method of transition, the transition from 4X to 6X results in capacitors across arms 3 and 4 to undergo a transition in voltage. In the case of 6X to 8X transition, only the capacitors on the outermost arm undergo transition in voltage. So, in order to determine the worst-case energy supplied by the input during transient, the case of 4X to 6X transition has to be analyzed. Figure 2.20 illustrates the input current (measured flowing into the positive terminal of Vin) and input voltage waveforms for the case of 4X to 6X transition at no load. The duration of the input current transient represents the time needed to charge/discharge all the intermediate capacitors in the switched capacitor network. Based on the data obtained from Figure 2.20 , the

Energy supplied by the source, V_{in} during the transient, E_{tran} is calculated to be 170 mJ during the transient current interval of $80\mu s$. If a mode change from 4X to 6X occurred every T seconds, the average input power, P_{in} can be computed using the following expression:

$$P_{in} = \frac{1}{T}\{E_{tran} + P_{ss} * (T - T_r)\} \qquad (2.14)$$

Where, P_{ss} represents the steady state input power requirement, T_r represents the duration of transient Energy. As the time interval between successive mode changes reduces, the input power requirement increases leading to a reduced overall efficiency. So, for this prototype, in order to limit $\frac{P_{in}-P_{ss}}{P_{ss}} < 0.3\%$, the time between successive mode changes is limited to 100 ms. The interval between successive mode changes is expected to be well above 100 ms for most applications. In such cases, the loss in efficiency due to successive mode changes is almost negligible.

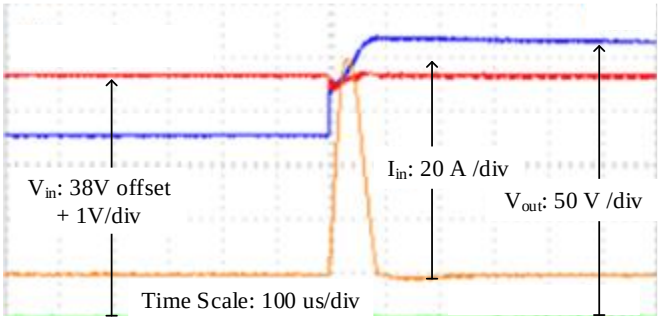
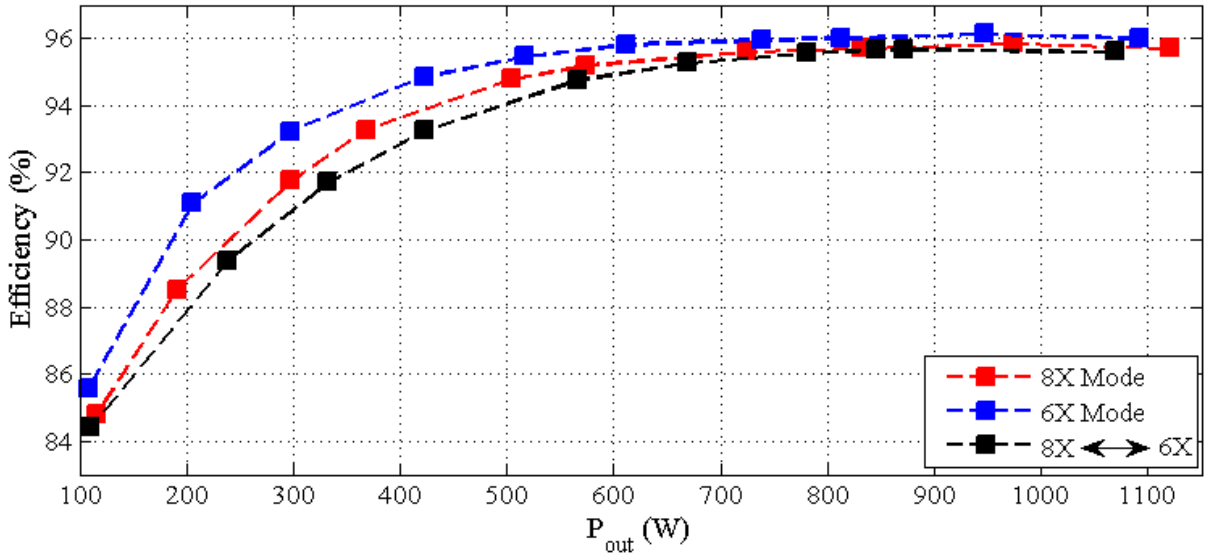


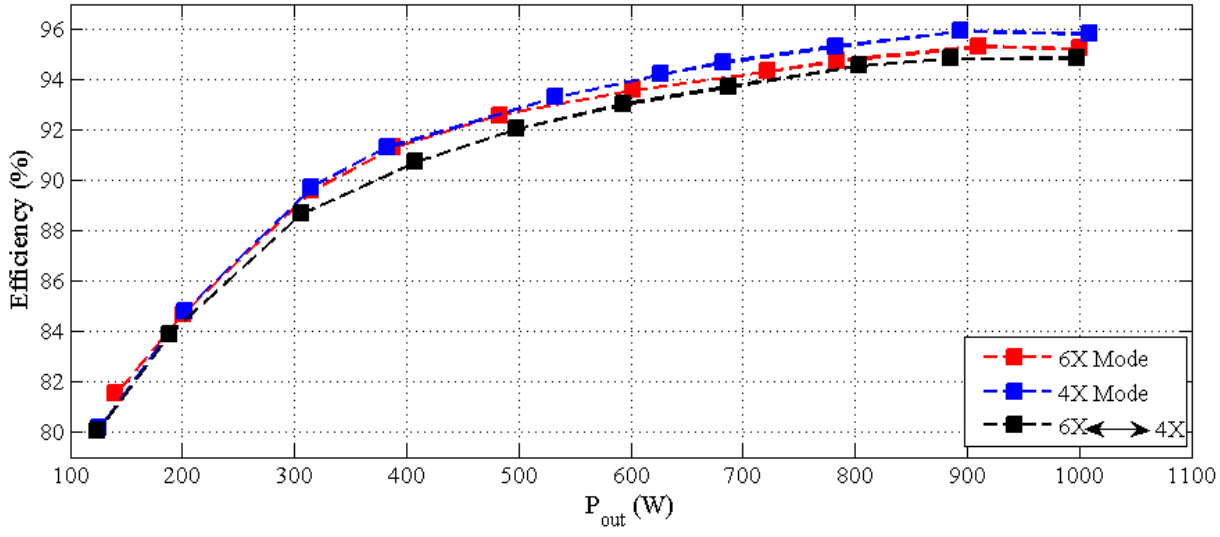
Figure 2.20: Input transient during 4X to 6X load-independent mode change.

Figure 2.21 (a) illustrates the efficiency curves measured during steady state operation of the converter for three different operating conditions, 8X mode, 6X mode and continuously transitioning between 8X and 6X modes once every 100 ms using the load independent method of mode change. Such continuously transitioning operating mode may not exist for most applications. But, experimental results for such a case further underscores the ability of the (n/m)X converter to provide dynamically varying voltage gains. The load is varied from about 150 W to 1000 W. The input voltage is fixed at 30 V as is the case described in Table *2.3* for 8X to 6X mode change. A maximum efficiency of 96.2% is achieved for this prototype during the 6X mode of operation. The maximum efficiency of the converter operating in 8X mode is measured to be 95.8%. The peak efficiency for the continuous transition mode (8X-6X-8X) is measured to be 95.7%. Figure 2.21 (b) describes the efficiency curves for three different operating conditions, 6X mode, 4X mode and continuous transition between 6X and 4X modes once every 100 ms using the load independent mode change method. As in the previous case, the load is varied from 150 W to 1000 W. The input voltage is fixed at 44 V as is the case described in Table 2.2 for 6X to 4X mode change. The measured peak efficiency in the 6X mode is 95.9% for the 6X and transition modes. The data for all the efficiency tests has been obtained using a Yokogawa WT1600 Digital Power Meter. From these results, it can be observed that the efficiency of the converter does not reduce

considerably in the continuously transitioning operating mode. It is within the estimated value based on input energy calculation. Based on the efficiency tests, it can be established that high values of efficiency (96%) can be achieved using the variable (4/0.5)X converter.



(a)



(b)

Figure 2.21: Efficiency curves for the prototype (4/0.5)X converter.

2.11 Conclusions

The main contributions of this chapter are summarized as follows:

1. A circuit configuration to achieve variable fractional voltage gains using a Dickson type converter.

2. Control and operation of the (n/m)X converter to achieve variable voltage gain.

3. Transition mode analysis and development of simplified equivalent circuit models for each mode.

4. Design methodology along with experimental results for a 1 kW, (4/0.5)X converter prototype.

Measured efficiency of over 95% is achieved during repeated transition in gain at regular intervals of 100 ms. The high efficiency capability along with the ability to achieve variable gains leads to useful advancements to the state of the art in Switched capacitor converters derived based on the Dickson converter. The design framework and analysis in this chapter are for a variable (4/0.5)X converter. But, the same methods can be extended for a generic (n/m)X converter or other variants of the Dickson converter.

CHAPTER 3 IMPROVED "SOFT" GAIN-TRANSITION METHODS FOR (N/M)X CONVERTER

3.1 Introduction

The (n/m)X converter proposed in Chapter 2 can provide fractional and variable voltage gains by retaining all the advantages of the nX converter. However, high input current transients are observed during transition for the methods proposed. Also, depending on the trace inductance distribution, the high input transient current can potentially translate to over-voltage stress on individual switches during mode transition. This could be a major limiting factor for the (n/m)X converter at higher power levels. The aim of this chapter is to introduce methods to achieve a soft-transition in gain for the (n/m)X converter. Here, the term "soft-transition" refers to reduction/elimination of input current transient during mode change (gain transition). This also enables the converter to operate without over-voltage stress across individual switches. Hence, the individual switches can now be rated for 2Vin (same as the fixed gain converter in [43]). The rest of the chapter is organized as follows: Section II introduces the schematic and trace inductance distribution in an (n/m)X converter. Section III introduces one method to achieve soft gain-transition for the (n/m)X converter. The method uses assistance form the load to achieve a soft-transition. Section IV introduces another method that can be used to achieve soft-gain transition without assistance from the load. In Section V, experimental results using a 1-kW (4/0.5)X converter undergoing soft gain-transition using the two proposed methods are presented. From these results, the improvement in transient input current and elimination of over-voltage stress across switches can be observed. This immensely improves the voltage regulation (gain hopping) capability for the Dickson type switched capacitor converters without compromising the individual device voltage stress.

3.2 The (n/m)X converter during transition between modes

The operating principle of the variable (4/0.5)X converter is described in Chapter 2. Figure 3.1 illustrates the structure of the (4/0.5)X converter with the trace inductance in every path lumped into two different locations, L_M and L_T. Figure 3.2 (a) and (b) illustrates one of the operating states for achieving 6X operation using the load-independent method proposed in Chapter 2. However, the direction of current through the individual switches at the instant of switch turn OFF (marked by red arrows in the figure) is determined by the relationship between switching frequency and the resonant frequency in a given loop for a given direction of power flow. For instance, if the direction of power flow is from V_{in} to load and the switching frequency is higher than the resonant frequency of the loop in question, the current direction is defined as positive and the case is represented by the illustration in Figure 2a. In this case, both the arm and leg switches of the converter are naturally clamped. However, should the direction of current (at the instant of turning OFF) be negative, the arm switches are not naturally clamped. This case is illustrated in Figure 3.2.

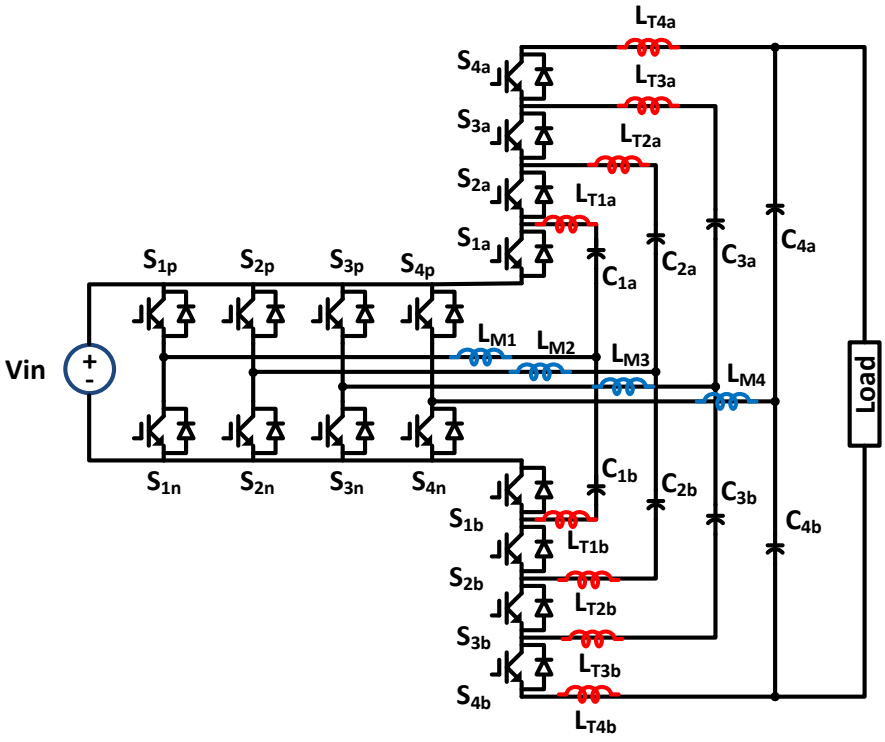


Figure 3.1: A (4/0.5)X converter with lumped inductances L_M and L_T.

Figure 3.3 (a)-(b) describes the latter case in more detail. The current paths (at the instant of turn-off) in the outermost loop of the case described in Figure 3.2 (b) are illustrated in Figure 3.3(a). Figure 3.3 (b) illustrates the current path during the dead-time (when all switches are OFF). The absence of a natural clamping for switches S_{4a} and S_{4b} can be observed from Figure 3.3 (b). As a result, when switches S_{4a} and S_{4b} are turned OFF, the worst-case peak voltage transient, V_T across each switch can be estimated by Equation (3.1).

$$V_T = 2V_{in} + 4*L_T*(i_T/T_{off}) \qquad (3.1)$$

Here, i_T is the current through inductor L_T prior to switch S_{4a} being turned OFF. T_{off} is the turn off time of the switch.

An optimum operating point for steady-state operation of the converter is close to the zero-current crossing point [42]. In such a case, i_T is minimized, and the resulting V_T is also minimized. However, this operating point cannot be met during the load-independent mode transition proposed in Chapter 2. The voltage across arms 3 and 4 are $6V_{in}$ and $8V_{in}$ respectively before the initiation of a mode change from 8X to 6X.

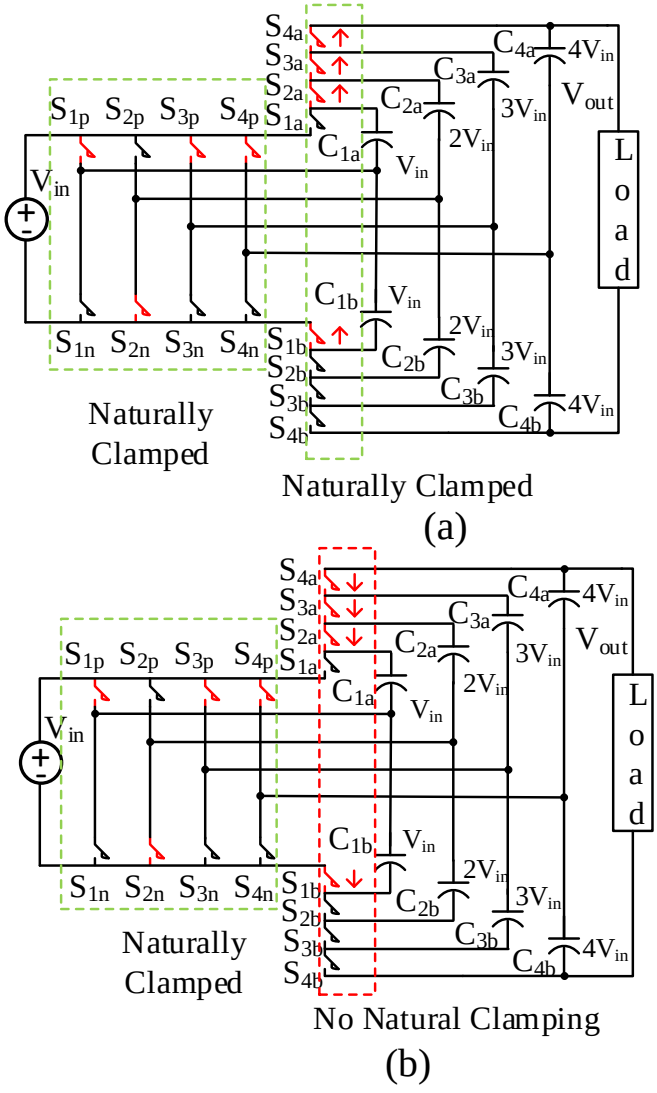


Figure 3.2: An operating state for the (n/m) X converter (a) Current direction resulting in natural clamping for all switches, (b): Current direction resulting in no natural clamping for the arm switches.

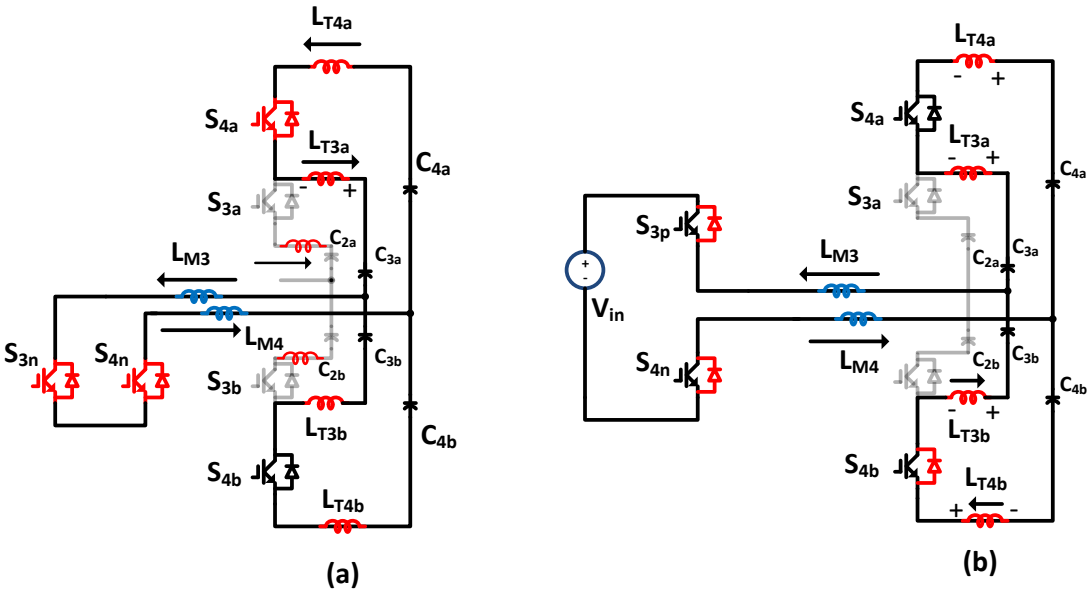


Figure 3.3: (a) Switching state during 8X to 6X transition, (b): dead-time interval during gain transition.

Once initiated, capacitors C_{4a} and C_{3a} are essentially paralleled to achieve a transition in voltage gain from 8 to 6 (output voltage transition from $8V_{in}$ to $6V_{in}$). However, at the instant of paralleling, C_{4a} has an initial voltage of $4V_{in}$. C_{3a} has an initial voltage of $3V_{in}$. Thus, a voltage difference of V_{in} drives the outer-most loop. This leads to a large inrush current from the input and also large arm currents in the converter. This leads to an increased i_T and leads to a large V_T as estimated by Equation (3.1). One method to minimize this transient over-voltage is to achieve optimal trace inductance distribution (larger inductance along L_M and smaller inductance along L_T). However, such methods are always not possible owing to constraints such as size and power density. Besides, as the arm current is large during mode transition, the inductance must be close to zero to ensure no over-voltage transient. In order to overcome this constraint, two different methods to achieve soft-transition in gain are proposed in the next few sections.

3.3 Load assisted soft-transition in Gain

The proposed method uses assistance from the load in order to transition from one gain to another. The case of a (4/0.5)X converter is used to describe the method to vary gain from one level to another. The method can then be extended to any (n/m)X converter. In order to explain the dynamic shift in gain during normal operation, the analysis is divided into two different modes viz., "shift-up" and "shift-down". The "shift-up" mode refers to a case where the gain is increased. The "shift-down" mode refers to a case where the gain is decreased. Using the (4/0.5)X converter, variable gains of 8, 6, 4 and 2 can be achieved.

3.3.1 Load assisted "Shift-down" mode using a dissipative load

In the case of a (4/0.5)X converter, shift-down from (4/0.5) to (3/0.5) or from 8 to 6 is achieved by following stages (a) through (c) illustrated in Figure 3.4. Every stage consists of two operating states, each lasting for 50% duration in a switching cycle. Figure 3.4 (a) shows the two operating states of a (4/0.5)X converter to achieve a steady state gain of 8 along with a timing diagram.

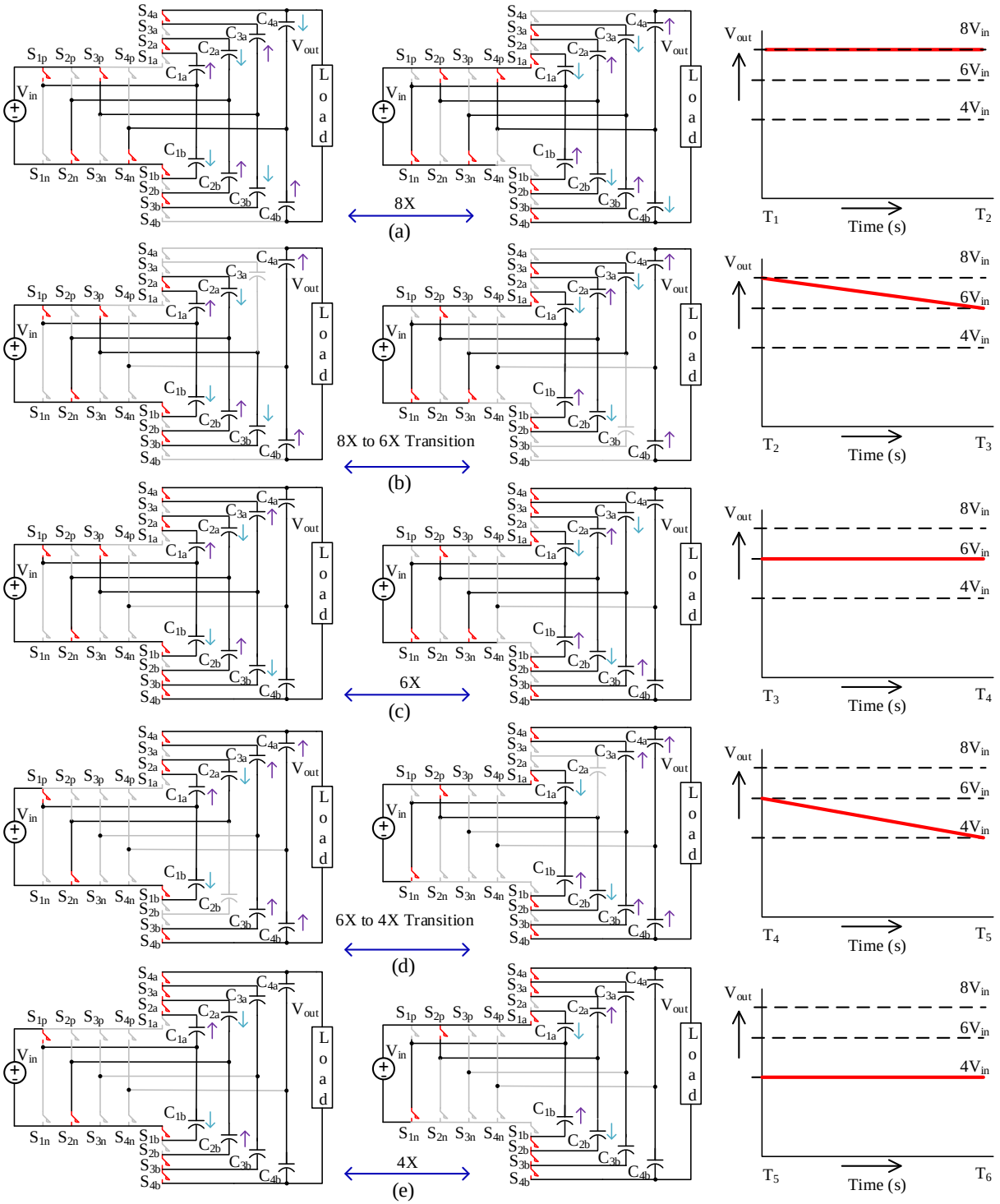


Figure 3.4: Operating states in load assisted "shift-down" and "shift-up" for a (4/0.5)X converter.

The duration for which the converter has a voltage gain of 8 is illustrated as T_1 to T_2 using the timing diagram in Figure 3.4(a). Since, the load is placed across arm 4, it continuously discharges

capacitors C_{4a} and C_{4b}. But, each of the capacitors on the outer arm receives energy from the input and inner capacitors every alternate operating state. So, for that operating state, the net energy received by the outer-most arm capacitor (difference between energy received from inner arms and the energy dissipated by the load) is positive. This is represented by means of the teal colored arrow on the outermost capacitors. In order to "shift-down" from a gain of 8 to a gain of 6, the switches S_{4a}, S_{4b}, S_{4p} and S_{4n} are all turned OFF as shown in Figure 3.4(b). The rest of the switches are continuously switching and alternating between the two operating states shown in Figure 3.4(b). This essentially disconnects the charging path to capacitors C_{4a} and C_{4b} on arm 4 of the converter. This is to ensure that the power flow path from the input to the arm capacitors undergoing transition is disconnected. During this time interval, as the load is dissipative in nature, it continuously discharges the capacitors C_{4a} and C_{4b} until the output voltage reaches a value close to the voltage across the third arm ($6V_{in}$). In this operating stage, the discharging path of capacitors C_{4a} and C_{4b} shown in Figure 3.4(b) are through the load. This is approximated by means of a linearly decaying slope (between T_2 and T_3) shown in the timing diagram of Figure 3.4(b). At the end of T_3, the anti-parallel diodes across switches S_{4a} and S_{4b} are clamped by the voltage difference between arms 3 and 4, essentially paralleling arms 3 and 4 of the converter. In order to maintain a voltage gain of 6 during steady state, switches S_{4a} and S_{4b} are turned ON permanently once the output voltage reaches $6V_{in}$ as shown in Figure 3.4(c). Once switches S_{4a} and S_{4b} are permanently ON, the voltage across the load and arm 4 are effectively controlled by arm 3 of the converter. Should an unbalance occur between the voltage across arms 3 and 4, a circulating current between the arms will automatically flow to balance the voltages on the individual arms. Should an unbalance occur between voltage across C_{3a} and C_{4a}, the body diode of switches S_{4p} or S_{4n} will automatically clamp to restore voltage balance. As the voltage across capacitors in arm 4

have the capability to self-balance, the individual charge, discharge states of these capacitors (teal and purple colored arrows) are not illustrated in Figure 3.4(c). Continuously alternating between the two states shown in Figure 3.4(c) will lead to a steady state gain of 6. The output voltage is maintained at $6V_{in}$ after time T_3 as shown in the timing diagram of Figure 3.4(c). In a manner similar to that described above, the gain "shift-down" from 6 to 4 with a dissipative load can be explained by means of additional stages shown in Figure 3.4 (d)-(e). The same method can then be further extended to transition to a voltage gain of 2. In the load assisted "shift-down" mode, capacitors (belonging to different arms) with a large initial voltage difference are not paralleled. The transient current and energy pulse across the switches are minimized by paralleling multiple arms only when their voltages are very close to each other (typically, determined by voltage drop across switch). Also, in this method, the power flow path from input to the arms undergoing transition is disconnected during mode transition. Hence, the excess energy stored in the arm capacitors are dissipated by the load.

3.3.2 Load assisted "Shift-up" mode using a regenerative load

In the load assisted "shift-down" mode, gain is shifted from a higher to lower level using a dissipative load. But, if the load in Figure 3.4 were replaced by a regenerative load, the gain can be moved up from a lower level to a higher level following the reverse sequence of all the stages described for the "step-down" mode. i.e. by moving from time T_5 to T_1 as described in the timing diagrams of Figure 3.4(e) to Figure 3.4(a), the gain can be shifted from 4 to 8. Much like the "shift-down" case, in the load assisted "shift-up" mode, the arm capacitors undergoing transition are disconnected from the original input during the transition. The excess energy needed to charge the capacitors during the "shift-up" transition is provided by the regenerative load (essentially

functioning as the source) and is not transferred from other capacitors/ the original input in the circuit. This eliminates the transient power loss during capacitive energy transfer that is determined by the magnitude of initial voltage difference between capacitors being paralleled. Capacitors belonging to different arms are paralleled only when their voltage difference is similar to the steady state voltage ripple of individual capacitors. This is key to ensuring a smooth transition without affecting the steady state efficiency of the system. During mode change, the power flow path from the input voltage is disconnected. The output arm capacitors (and any arm paralleled to it) are only discharged by the load until the new gain level has been reached.

At that point, power flow path from the input is restored. So, during the load assisted mode change, no power transfer takes place from the input to the arm capacitors undergoing transition. This leads to negligible input current transients. Based on the operating method for the "shift-down" and "shift-up" modes of a (4/0.5)X converter, it can be seen that the load-assisted method is dependent on the nature of the load to achieve a shift in gain. If the load is always dissipative, only "shift-down" operation can be achieved using this method. On the other hand, if the load is always regenerative, only "shift-up" operation can be achieved. In order to address these issues, a method to achieve soft transition in gain that is independent of the load is proposed in the next section. In the case of the (4/0.5)X converter, the different available gains are 8,6, 4 and 2. These are some of the limitations of the load-assisted method of mode change. For a generalized (n/m)X converter, the available steps of gain are, (n/m), {(n-1)/m}….{1/m}. Experimental results for a 1-kW converter with gain shift achieved using this method are illustrated in future sections.

3.4 Load Independent Soft-Transition in Gain

In Section 3.2, the inability of the converter arm switches to be naturally clamped in the event of negative current direction has been highlighted. This leads to over-voltage across the arm switches in Chapter 2. Using the method proposed in this section, natural clamping of individual switches can be achieved irrespective of the direction of arm current at the turn-off instant of the switch.

Figure 3.5(a)-(b) illustrates a case of input current transients due to loop voltage difference, V_d. Here, R and L represent stray inductance and resistance in the respective loops. S indicates a switch that can be controlled to be ON/OFF. The instantaneous currents in each loop are marked.

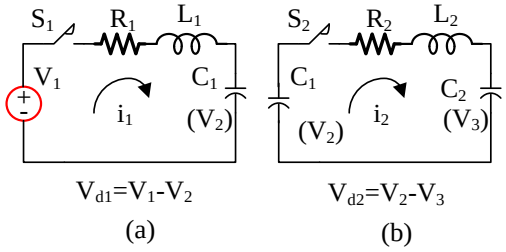


Figure 3.5: Illustration of loop and input current transients.

At steady state, assume that the voltages, V_1, V_2 and V_3 are identical to each other or have a very small voltage difference, V_d. In such a case, the transient current is well limited by the stray inductance and resistance in each path. Consider another case where V_3 is much larger than V_2. In such a case, when S_2 is closed, the large voltage difference V_{d2} drives a large transient current i_2. If the time duration for which switch S_2 is closed is larger than the resonant time period of the loop, it is possible for the final value of V_2 to be as high as the initial value of V_3. Next, when S_2 is opened and S_1 is closed, due to the modified voltage of V_2, large transient current will be drawn by the source. Hence, to avoid large input current transient to be drawn by the source, variation in

voltage V_2 has to be minimized. On similar lines, by controlling the variation in inner loop capacitor voltage during transition from one gain level to another, the input current transient of the (n/m)X converter can also controlled.

By ensuring that the arm switches are clamped and the transition mode voltage across individual capacitors are controlled, both the over-voltage transient across the switches and input current transient from the source can be controlled. Figure 3.6 (a)-(c) illustrates the trajectory of operating stages to achieve a load-independent soft gain-transition from 6 to 8.

3.4.1 Operating stage (a): 6X mode

Figure 3.6 (a) illustrates this operating stage. The two operating states in this stage are identical to the 6X operating states in the load-independent transition method proposed in [5]. Voltage across individual arm capacitors, C_{1a} through C_{4a} are V_{in}, $2V_{in}$, $3V_{in}$ and $3V_{in}$ respectively. By following identical switching states on arms 3 and 4, the capacitors on these arms are essentially paralleled.

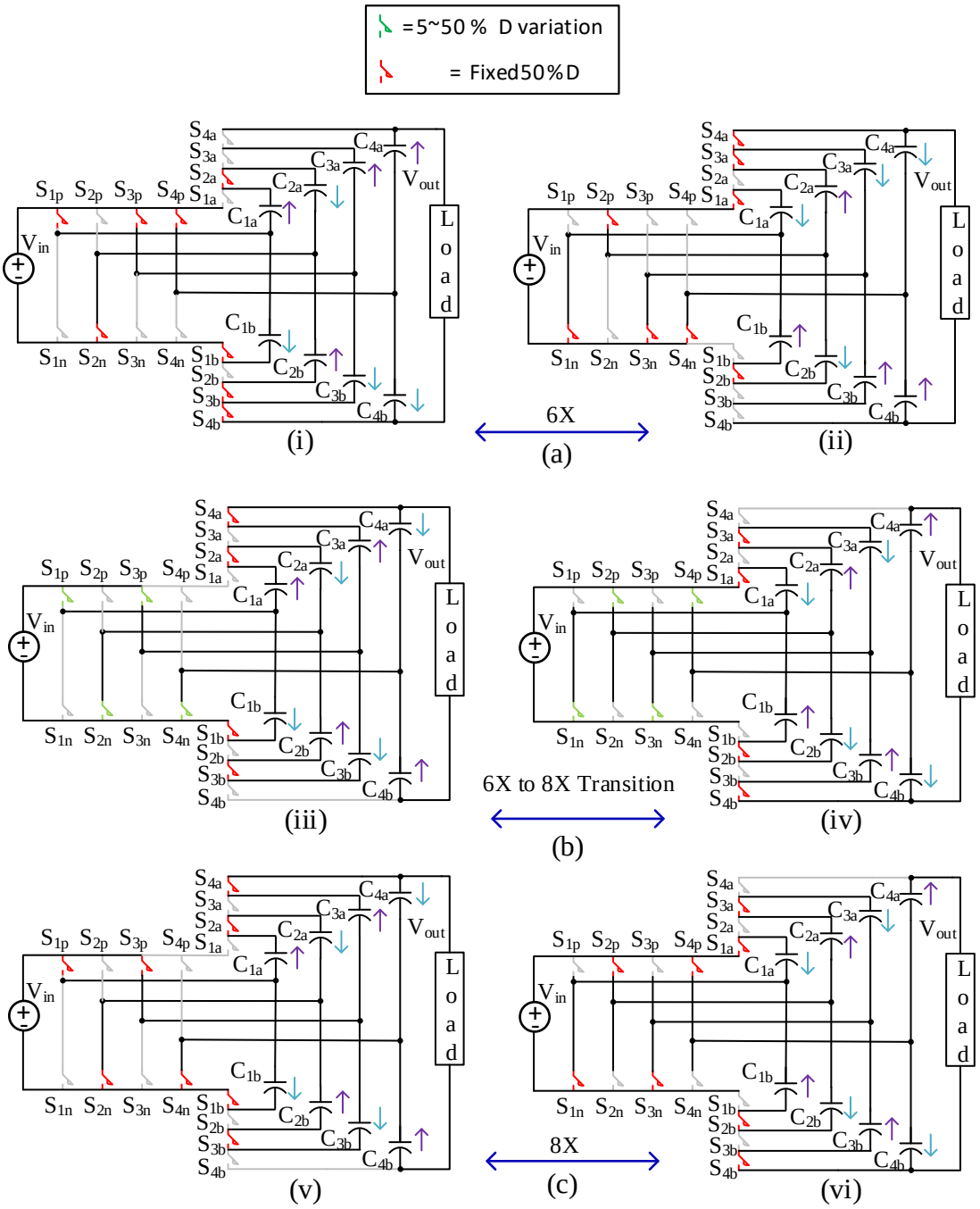


Figure 3.6: (a)-(c): Operating stages for load-independent soft transition from 6X to 8X in a (4/0.5) X converter.

3.4.2 Operating stage (b): 6X to 8X mode transition

Figure 3.6 (b) illustrates this operating stage. The (n/m)X converter shifts to this operating stage when a gain transition from 6X to 8X is initiated. A key difference in this stage compared to the other stages is the introduction of variable duty cycle control. The leg switches are controlled with

a variable duty cycle from 5% to 50% over several switching cycles. To distinguish this from the conventional 50% duty cycle operation, the leg switches are marked in green. The variable duty cycle control for the leg switches is illustrated in Figure 3.7. Duty cycle control for leg switches limits the arm currents. The fixed 50% duty cycle for the arm switches provides ample freewheeling interval for the trace inductors L_T (Figure 3.1) irrespective of the current direction and the arm switches can be switched OFF at zero current. Hence, the arm switches are naturally clamped. The duty cycle control also limits the variation in voltage across capacitor C_{3a} and C_{3b} in the transition mode. This is instrumental in limiting the input current transient from V_{in}.

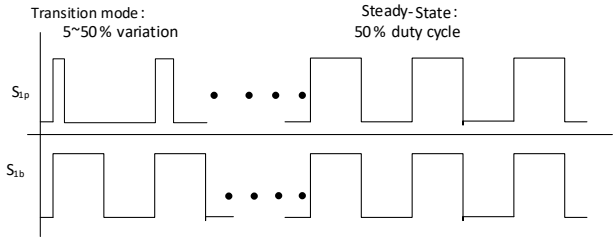


Figure 3.7: Illustration of duty cycle control for leg switches in a (n/m)X converter.

3.4.3 Operating stage (c): 8X mode

Figure 3.5 (c) illustrates this mode of operation. In this operating stage, the transition from 6X to 8X is complete and a steady state voltage of $8V_{in}$ is obtained at the load. The same technique can be extended to a gain transition from 4 to 6 using a (4/0.5)X converter. The operating stages for this case are illustrated in Figure 3.8 (a)- (c). The same method can be extended to any general (n/m)X converter and is completely load independent in sharp contrast to the load assisted soft-transition method.

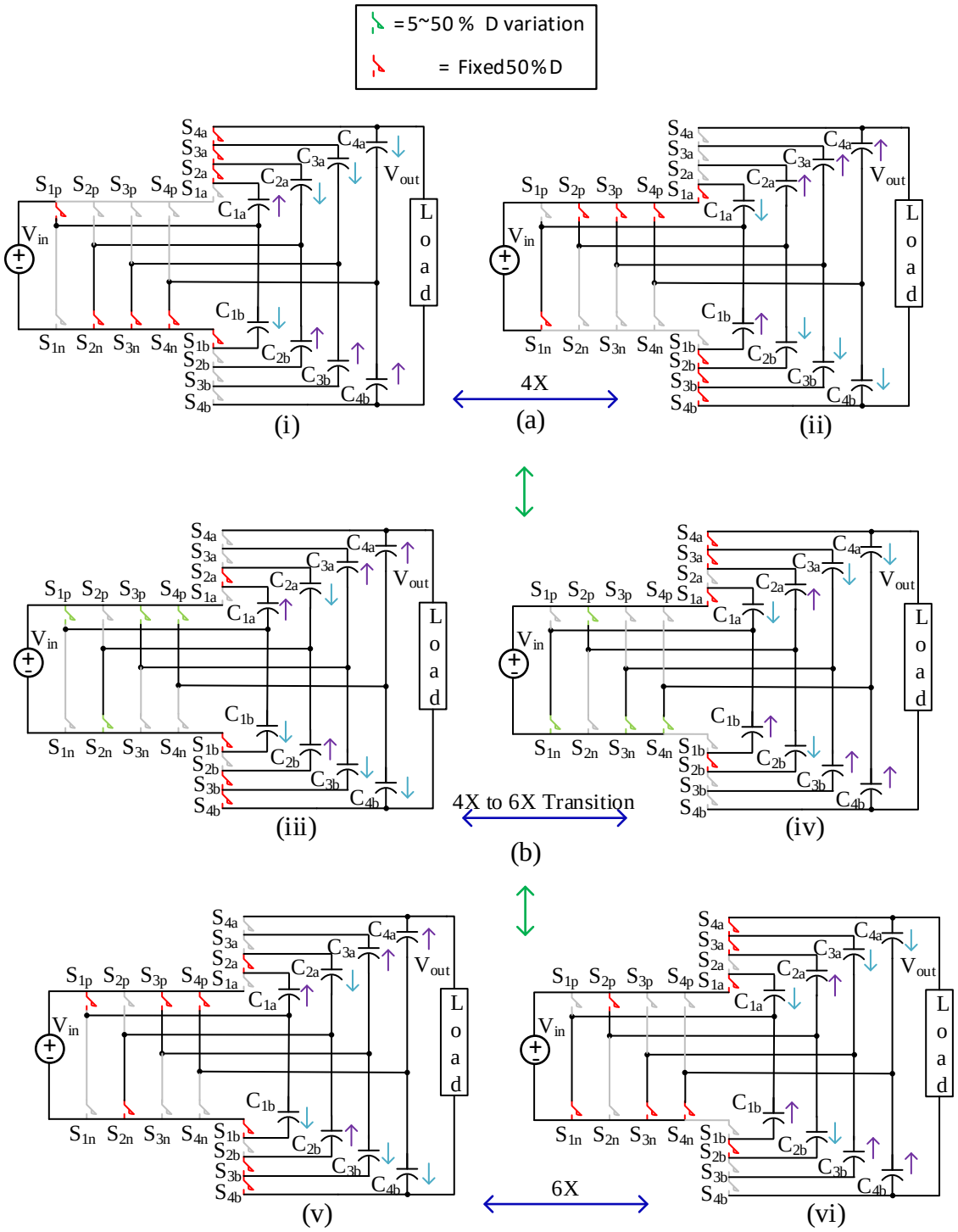


Figure 3.8: (a)-(c): Operating stages for load-independent soft transition from 4X to 6X in a (4/0.5) X converter.

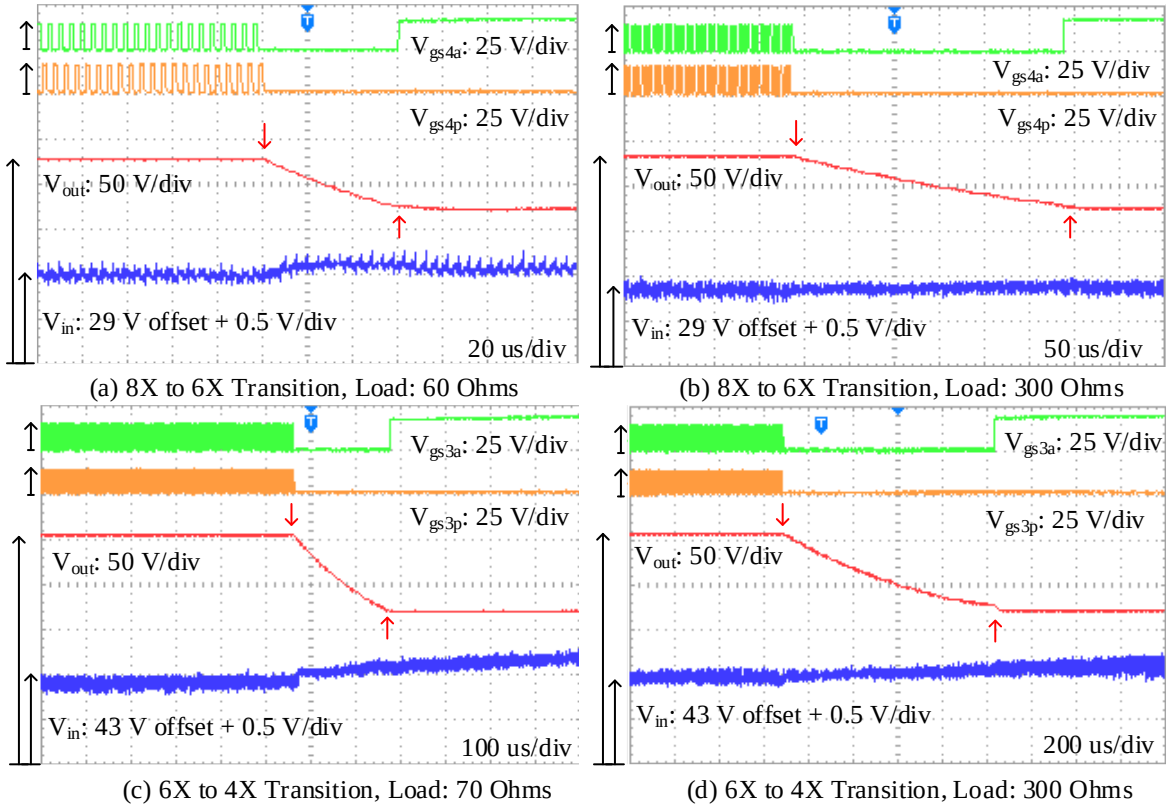
3.5 Experimental Results

A 1-kW prototype of a (4/0.5) X converter in a boost configuration has been developed to validate the proposed methods. The input voltage range for the converter is 25 V to 50V. The peak voltage rating of individual switches is 100 V. The switching frequency is 200 kHz. A variable resistance load is used for all the experimental results.

3.5.1 Load assisted soft-transition

In Figure 3.9 (a), when the sensed input voltage is rising and (input voltage is sensed every 6 ms) reaches 30 V, a gain transition from 8X to 6X is initiated. The rising input voltage is achieved by manually varying the position of variac in Figure 2.13.

As the rate of increase is much slower than the time scale of the waveform, the input voltage trace (blue) remains fairly constant over the entire waveform. This is true with all the mode change waveforms presented in the chapter. As the input voltage is represented by means of the trace V_{in} (blue). The waveform is shown here with a DC offset of 29V.



(a) 8X to 6X Transition, Load: 60 Ohms

(b) 8X to 6X Transition, Load: 300 Ohms

(c) 6X to 4X Transition, Load: 70 Ohms

(d) 6X to 4X Transition, Load: 300 Ohms

Figure 3.9: Experimental results for the load assisted soft-transition.

The transition in output voltage can be seen in the output voltage trace, V_{out}.(red). The beginning and end times for the transition are marked within the waveform by means of red arrows. The gate-source voltage across switch S_{4a}, V_{gs4a} is shown by means of the green trace. From the trace, it can be seen that switch S_{4a} is first turned OFF (at the beginning of mode transition) to disconnect the charging path to capacitor C_{4a}. Once the output voltage has finished transitioning from 8X to 6X, the switch is turned ON permanently. The gate-source voltage across switch S_{4p} during this mode transition is illustrated by means of the orange trace, V_{gs4p}. It can be seen that the switch is turned OFF as soon as the mode change is initiated. Figure 3.9 (b) illustrates the case of an 8X to 6X transition for a load of 300 Ohms. From the trace for V_{out}, it can be observed that the time taken to complete the mode transition is $320\,\mu s$ when compared to the $60\mu s$ taken in case of 60 Ohms load. Thus, the transition time is a linear function of the load as expected for the case of load-

assisted transition. The waveforms illustrating load assisted mode change from 6X to 4X at a rising input voltage, Vin = 44V are shown in Figure 3.9 (c)-(d).

Figure 3.10 (a)-(d) illustrates the experimental waveforms for load assisted soft-transition.

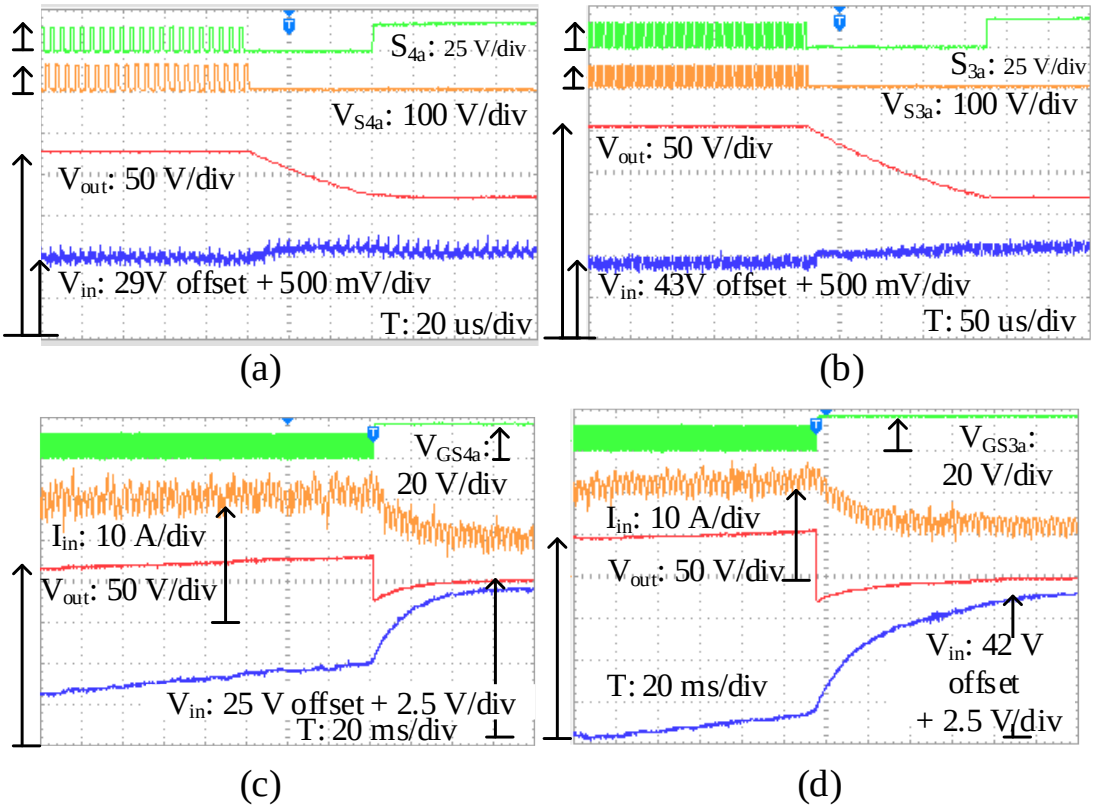


Figure 3.10: Experimental waveforms for load assisted soft-transition: (a),(c): 8X to 6X Transition at Vin=30 V, Load = 60 Ohms, (b), (d) 6X to 4X Transition, Vin = 44 V, load = 70 Ohms.

In Figure 3.10 (a) and (c), transition from 8X to 6X occurs at V_{in}= 30 V. The soft transition in output voltage, V_{out} can be observed. Since, the switched capacitor network is disconnected from V_{in} during gain transition, there is no transient inrush current, I_{in} from V_{in}. There is no over-voltage across individual switches. This is illustrated by voltage across S_{4a}, V_{S4a}. The peak voltage stress is within $2V_{in}$. Figure 3.10 (b) and (d) illustrate the case of load assisted transition from 6X to 4X.

3.5.2 Load independent soft-transition

Figure 3.11 (a) illustrates the experimental results for the conventional load independent transition method proposed in Chapter 2. The result is obtained at V_{in}=25 V and no load. Since there is no load, it can be assumed that the input energy is drawn to charge/discharge the arm capacitors. Figure 3.11 (b) illustrates the experimental results for the same input condition but replacing the conventional transition method with the soft-transition.

Here, the input current peak is reduced by 300% compared to the conventional case. The voltage deviation across capacitor C_{3a}, V_{C3a} is limited to within 10 V (< 0.5 Vin). Figure 3.11 (c) illustrates the experimental results for a 4X to 6X transition using the load-independent method in Chapter 2. In comparison to this, the peak current transient in the soft-transition method is about 300% lower.

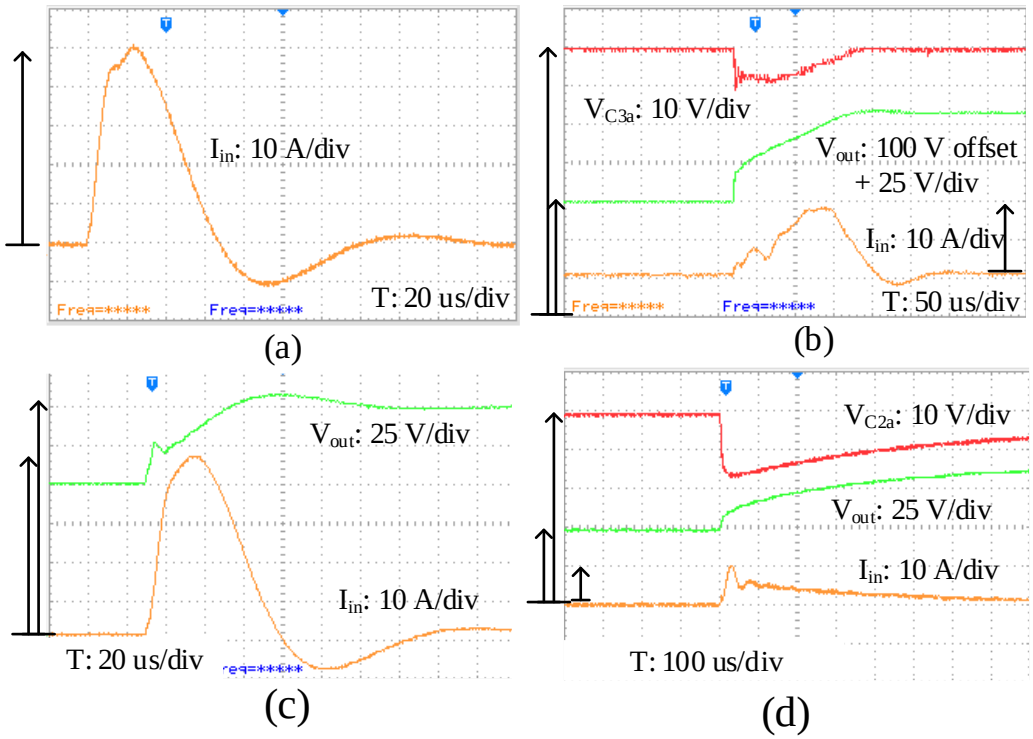


Figure 3.11: Experimental results for load independent soft-transition: (a),(b): 6X to 8X Transition at Vin=25 V, No load. (c), (d) 4X to 6X Transition, Vin = 25 V, No load.

Figure 3.12 (a)-(c) illustrate the input current transient with a load of 50 Ohms and voltage stress of switches S_{3a} and S_{2a} during a load independent soft- transition. In both cases, (6X to 8X) and (4X to 6X), the input transient is limited to 150% of the load current. Additionally, there is no over-voltage transient across any of the switches. This leads to superior performance when compared to the performance of the load independent gain transition method in Chapter 2.

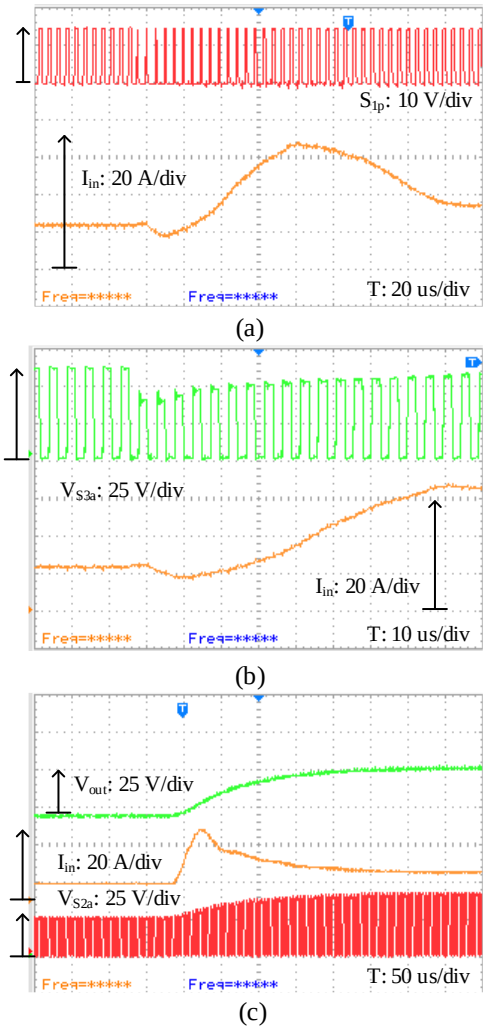


Figure 3.12: Experimental results for load independent soft-transition: (a)-(b): 6X to 8X Transition at Vin=25 V, Load =50 Ohms. (c): 4X to 6X Transition, Vin = 25 V, Load: 50 Ohms.

3.6 Conclusion

Two methods to reduce the input current transient and eliminate the over-voltage transient across switches during gain transition have been proposed. For each of these methods, the operating principle along with the different operating stages has been introduced. Experimantal results for a 1-kW prototype further illustrates the superior performance of the proposed methods. Using the proposed methods, the input transient current is limited to within 150% of the load demand. This is a 300% improvement over the methods proposed in Chapter 2. The over-voltage transients

across each of the switches are eliminated. The proposed methods can also be extended to buck configuration of the (n/m)X converter.

CHAPTER 4 ULTRA-HIGH EFFICIENCY AND POWER DENSITY RESONANT DICKSON CONVERTER

4.1 Introduction

The trend in aircraft power systems is to move towards “no-bleed” systems or more electrification [50], [51]. However, to reduce the weight of the conductors, one preferred method is to use a high-voltage DC (up to 540 V or +/- 270 V nominal) based power distribution system. This necessitates efficient power converters to step down +/-540 (or 0 to 270) down to the nominal 28 V required by existing low-voltage loads in the aircraft [51]. At steady state, the nominal 270 V DC bus has a range of 250 V to 280 V the nominal 28 V bus has a range of 22 to 29 V [52]. The commercial off-the shelf (COTS) power supplies are designed for this specification [53],[54]. Several blocks of 250 to 350 W rated such power supplies can then be used in parallel to achieve higher power output. Dickson type switched capacitor (DSCCs) converters offer a single-stage solution to achieve high voltage-gains. The main power stage in the Dickson type converter is derived from the original Dickson converter that offers a fixed gain/step-down ratio. A high-efficiency low-voltage buck regulator can be integrated or cascaded to achieve voltage regulation when needed. This enables DSCCs to offer numerous advantages such as ease of control, bidirectional operation, high power density and high efficiency. Overall, it is a suitable candidate in more-electric aircrafts to achieve large step-down at high-efficiency and power density. At the maximum input voltage of the 270 V DC bus (280 V), a Dickson type converter with a fixed step-down of 10 is required to achieve 28 V. However, there are several challenges in configuring and designing a Dickson type converter for use in such a system and other similar systems with a high step-down. In this chapter, a 300 W rated 280/28 V system is used an example for high-gain systems. However, it can be adopted for the power stage of any other system that requires a high-voltage gain.

A 280/28 V step-down converter for MEAs requires a nominal step-down ratio of 10. At such high

voltage gains, the number of individual switched capacitor (SC) cells in SCCs increases. This leads to an increase in the number of semiconductor devices and capacitors in the system. Figure 4.1 illustrates the Dickson type converter configured for a 4:1 step-down voltage gain. The number of switches and capacitors for a step-down, N (V_{in}/V_o) are N+4 and N respectively. For a step-down of 10, this results in 14 switches and 10 capacitors.

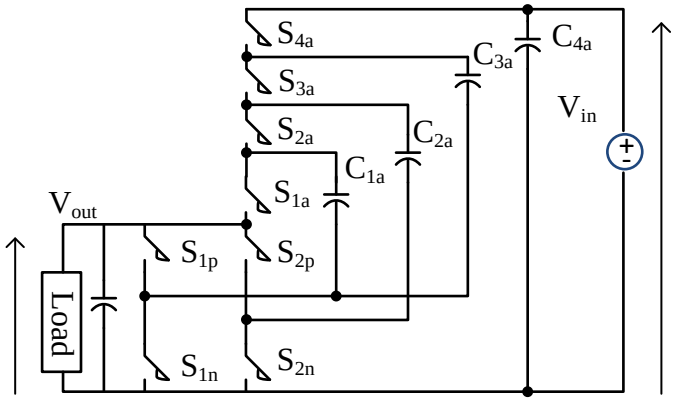


Figure 4.1: Conventional Dickson type converter with a voltage step-down ratio of 4 (V_{in}/V_o).

To achieve higher efficiency, traditional Dickson type converter requires low capacitor voltage ripple [15] and high switching frequency. While this limits transient charging currents, it contributes to increased switching losses. Split-phase control is proposed in [19] and [55], to relax the requirement of low ripple voltage on the arm capacitors. But, the method is load dependent and requires additional intermediate control stages. A modular multi-level capacitor clamped converter is proposed in [38]. Zero-current switching techniques for this configuration are proposed in [23] to reduce the cross-over switching losses. However, the configuration requires large number of switches to achieve a modular structure in terms of current sharing and ease of tuning individual resonant loops. Also, the usage of air-core/trace inductors in resonant loops can potentially lead to increased EMI. GaN HEMTs are widely recognized as an enabling technology to minimize losses in switched capacitor and other power electronics systems [25], [57]. Resonant

SCCs using GaN HEMTs for the power stage of data center applications (48 to 12 V) has been explored in [27], [28]. The configuration is based on the resonant type configuration in [23] with suitable optimization in arm capacitor and inductor selection. But, the switch network follows the same modular approach as in [23] resulting in increased number of switches. While, it may not be an issue for low step-down ratios, the large number of switches in the system is a cause of concern for scaling to higher voltage step-down. It also results in increased gate drive requirement and losses if not optimized. Also, as majority of the energy in each cell is still stored in arm capacitors, it renders a relatively large capacitive network.

In this chapter, a Dickson type resonant converter is designed for a 300 W, 280/28 V power stage in a MEA. A holistic design approach is used to optimizes loss, power density and system component count leading to a high-efficiency, high power density system. Using optimal switch selection techniques, the configuration achieves high-efficiency without the need for a large number of switches. By utilizing GaN switches in the main power conversion stage, the losses are further reduced. An ultra-efficient, low-profile custom gate drive for GaN HEMTs is designed. This allows the entire converter to function with a single 5 V auxiliary supply for the gate drive. This significantly reduces the component count of the system and improves power density. It also fully exploits the benefits of GaN switches in the system. The gate drive design can also be used for other GaN based fixed duty cycle power converters that require ultra-high efficiency gate drivers. During power transfer, energy in each switching cell is optimally (for power density) distributed between HV ceramic capacitors and flat-wire chip inductors without affecting the overall power density. This results in improved soft-charging and a high power-density switched "LC" network compared to traditional Dickson type converters. A 300 W resonant Dickson type converter prototype for a 280/28V more-electric aircraft power system is designed with a target

efficiency of 99+%. A peak efficiency of 99.1 % and a power density of 87 W/in^3 is achieved.

The rest of the chapter is organized as follows:

The GaN based resonant Dickson converter configuration is described in Section 4.2. Section 4.3 discusses the loss optimization techniques for the resonant Dickson converter. Section 4.4 presents the design of a high-efficiency and compact gate drive solution for GaN switches. Section 4.5 describes the physical converter prototype. Section 4.6 presents experimental waveforms other experimental results obtained with the prototype converter.

4.2 Resonant Dickson Converter

4.2.1 Configuration

Figure 4.2 illustrates the schematic of the 280 V / 28 V resonant Dickson converter designed in this manuscript. Generic switch symbol is used to represent the switches in the figure. The switches on load end of the converter are termed as 'leg' switches. They are represented with subscripts 'p' and 'n'. The switches on the source end of the converter are termed as 'arm' switches. They are represented with subscript 'a'. The design uses a hybrid, GaN and Si MOSFET solution. Si MOSFETs are used for the switches on converter leg and GaN HEMTs are used for the arm switches. Detailed loss analysis that underline the benefits of such a hybrid solution is described in Section 4.2 A. Individual arm capacitors in traditional Dickson-type converters are replaced by a series LC network. HV ceramic capacitors and flat-wire, low resistance magnetic chip inductors are used for the arm inductance. The optimal distribution of the overall arm energy between L and C is described in Section 4.3.2. This leads to numerous benefits such as high power- density, soft-charging in every switching cycle and the ability to allow larger capacitor voltage ripple. The use of magnetic chip inductors over air core or trace inductance has the potential to reduce radiated EMI. Identical to the traditional Dickson converter, for a load current of I_o, each leg switch in the

resonant Dickson converter carries an average current of 0.5* I_o. On the other hand, the arm switches carry an average input current, I_{in}. The converter operates with a fixed 50% duty cycle, the average currents are distributed over the ON time of the individual switches. The peak voltage stress across leg switches is the output voltage, V_o. Peak voltage stress across the arm switches is $2V_o$. The only exceptions in the arm switches are S_{1a} and S_{10a} (or generic S_{na}), which have a voltage stress of V_o.

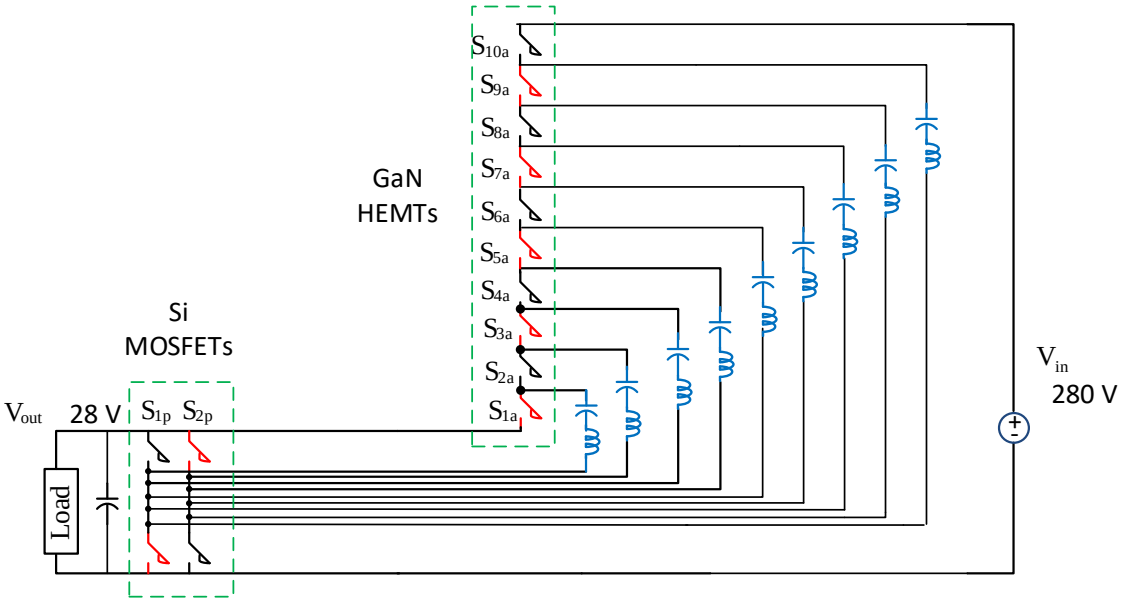


Figure 4.2: Schematic of 280 V/28 V resonant Dickson converter.

In contrast, the resonant SCC converters in [23]- [28] use 'N-1' number of half-bridges or '2N-2' number of leg switches on the load side, N being the voltage step-down ratio. Although having multiple half-bridge cells reduces the current stress on individual switches, having fewer switches with larger current stress leads to lower losses in the system. This is described in detail in Section 4.3.1.

4.2.2 Operating modes

As is the case with conventional Dickson type converters, the resonant Dickson converter has two operating modes. Each mode operating for a fixed 50% duty cycle. In Figure 4.2, the switches marked in red are ON during one mode and the switches marked in black are ON during the next mode. This leads to continuous switching between the following two sets of equivalent circuits as shown in Figure 4.3 and Figure 4.4. Here, C_o represents the capacitance at load terminal. For ease of analysis, the load has been removed from the individual loops.

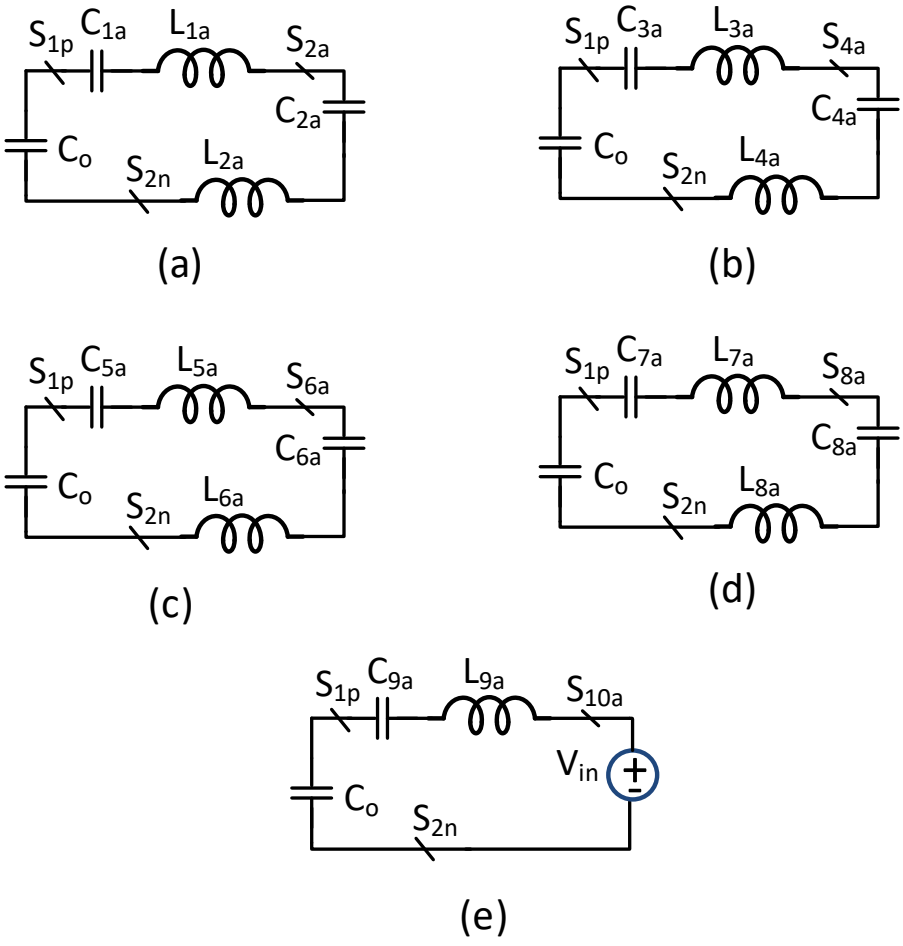


Figure 4.3: Equivalent loops in switching state I.

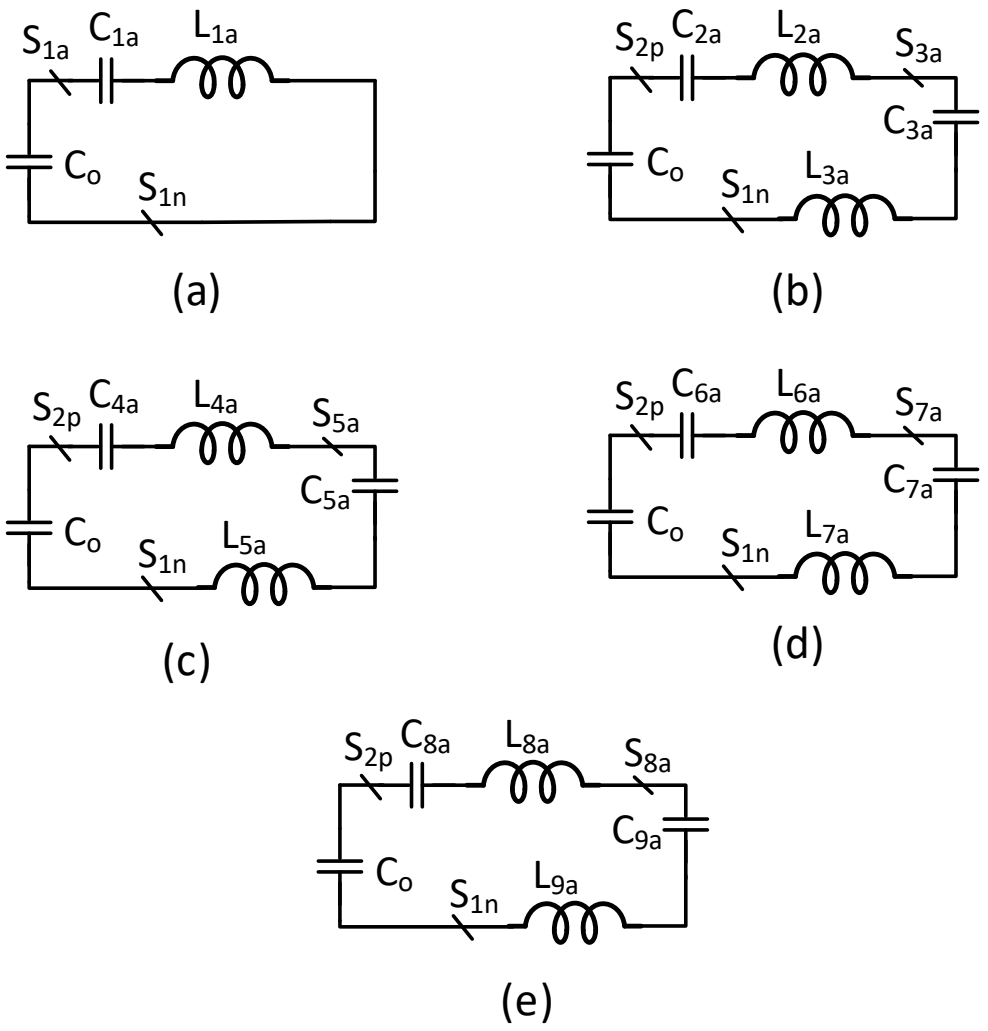


Figure 4.4: Equivalent loops in switching state II.

It can be observed that all, but two loops consist of three capacitors and two inductors. These loops have nearly matching resonant frequencies if the L and C are identical. The equivalent loop resistor is considered intrinsic to the L and C elements and has not been marked in the Figures. This implies that for modes (b) to (d), the overall loop inductance and capacitance can be equally divided between adjacent arms. But, for loops (a) and e, the loop L and C cannot be divided equally between adjacent arms. This is taken into consideration while designing individual converter modules in later sections.

As in the case of other resonant SCCs [23], to achieve zero-current switching at turn-off, the

resonant frequency (f_r) in each loop must be equal to or close to the switching frequency (f_s) and the loops must all show underdamped response. The key difference in the resonant Dickson converter is that the leg switches carry the arm currents from 5 different loops at any given time. If the switch selection is not optimal, this can lead to much larger losses in the leg switches and hence the overall converter. Optimal switch selection to avoid excessive losses in the system due to large currents is discussed in Section 4.3.1.

4.3 Loss Optimization

4.3.1 Optimal Switch selection

In a Dickson type SCC, the voltage stress of leg switches is the output voltage, V_o. The voltage stress of arm switches is twice the output voltage, $2V_o$. The only exceptions are the switches in the innermost and outermost arms of the converter that have a voltage stress of V_o. For a 280/28 V, 300 W buck specification, the peak voltage stress across arm switches is 56 V and the peak voltage stress across the leg switches is 28 V. For this specification, the nominal load (I_o) and input current (I_{in}) are 10.7 A and 1.07 A respectively. In the resonant Dickson converter, the individual arm switches undergo zero-current switching. If each loop is tuned for under-damped response, the current waveshape is close to a half-sine wave [42].

The RMS current through the arm switches can be represented using the following expression

$$I_{rms}^{a} = \frac{\pi}{2} I_{in} \qquad (4.1)$$

The RMS current through the leg switches can be represented using the following expression

$$I_{rms}^{l} = \frac{N\pi}{4} * I_{in} \qquad (4.2)$$

Where N represents the step-down ratio of the resonant Dickson converter.

The presence of two-half bridge cells on the converter leg results in an average current of $I_o/2$ through the leg switches. The average current along arm switches is I_{in}.

To minimize the overall losses in the system, the arm and leg switches are chosen carefully. Due to zero-current switching nature of the resonant Dickson converter and other SCCs, the switching losses are dominated by the losses due to charging and discharging of the switch output capacitor, C_{oss}.

The switching loss for an arm switch for a switching frequency, f_s is given by the following expression,

$$P_{sw}^{a} = (2V_o)^2 * C_{oss} * f_s \quad (4.3)$$

Conduction loss for the arm switch is determined by the following expression,

$$P_{con}^{a} = {I_{rms}^{a}}^2 R_{DS(ON)} \quad (4.4)$$

For the leg switches, these losses are represented by the following expressions:

$$P_{sw}^{l} = (V_o)^2 * C_{oss} * f_s \quad (4.5)$$

$$P_{con}^{l} = {I_{rms}^{l}}^2 R_{DS(ON)} \quad (4.6)$$

The timing between turning ON of leg switches and turning ON of arm switches is tuned in order to minimize or eliminate the switching loss component on the leg switches, P_{sw}^{l}. Figure 4.5 illustrates this method where the timing in the individual gate drivers of arm and leg switches are tuned to achieve a small delay, t_z in the gate-source voltage, V_{gs} of the leg switches with respect to the arm switches. When the arm switches are ON and the leg switches are off, the arm currents flow through the body diodes of the leg switch. This is illustrated in Figure 4.6 (a). Once the current starts to flow through the body diode, the switch is turned-on (marked in green) leading to zero-voltage turn ON of the leg switches. This is illustrated in Figure 4.6(b). The same procedure is repeated for the other set of complementary leg switches.

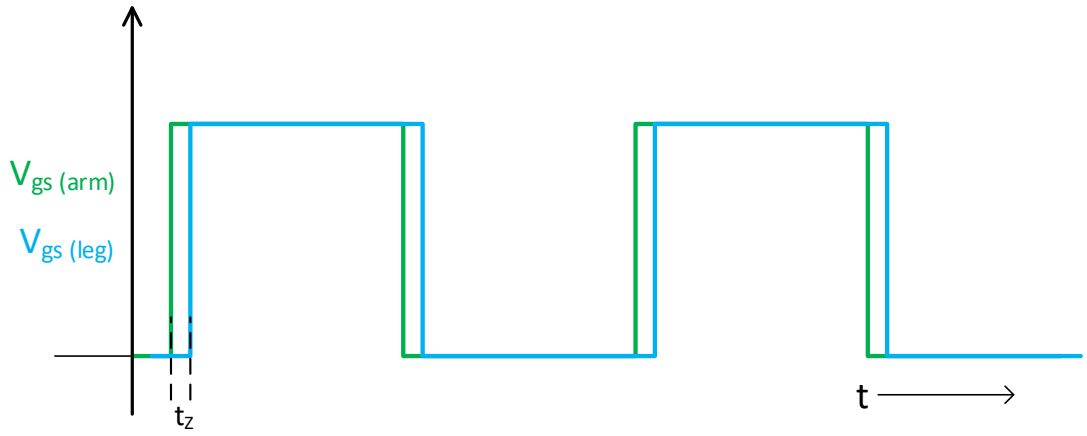


Figure 4.5: Tuning the turn-on time of arm and leg switches to minimize switching losses in leg switches.

In this chapter, this tuning is accomplished by altering the turn-on and turn-off dynamics of the gate driver. Other adaptive tuning techniques could also be adopted. For the purpose of loss estimation, the turn-on portion of the switching losses, P_{sw}^{l} in the leg-switches can hence be ignored. Low on-state drop across the body diode or it's equivalent can minimize the conduction losses incurred during t_z.

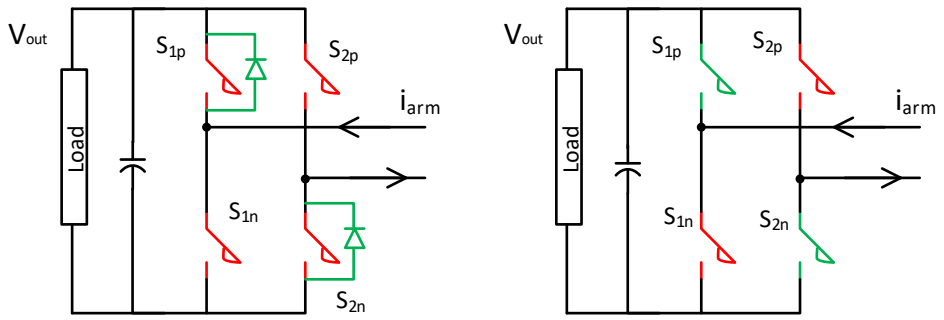


Figure 4.6: (a) arm currents flowing through body diodes of leg switches when OFF; (b) Arm currents flowing through the leg switches when ON.

As the voltage stress across arm switches is double that of the leg switches, higher emphasis is to optimize for low C_{oss} in arm switches. For a voltage step-down ratio of 10 (280/28 V), the leg

switches are required to carry approximately 5 times the current of the arm switches. This is also evident from the five loops connected to a single set of leg switches in Figure 4.3 and Figure 4.4. Higher emphasis is placed on minimizing $R_{DS(ON)}$. However, in doing so, the overall losses in the system should also be minimized. Additionally, to improve power density and overall stray inductance in the layout, a low-profile switch package is preferred.

Considering a factor of safety to account for voltage overshoot across switches, 100 V and 60 V are considered as suitable voltage ratings for the arm and leg switches respectively. The Figure of merit (FOM) commonly used for switch selection is $C_{oss} * R_{DS(ON)}$.

Table 4.1 compares the key parameters of switches with superior FOM and small footprints for 100 V peak voltage stress. The switches listed here are suitable for the arm switches. At this voltage range, GaN HEMTs feature heavily as they have superior FOM (lower FOM values) when compared to Si based MOSFETs. Additionally, the ability to use low gate drive voltages to drive the GaN switches results in increased benefits in terms of reducing gate drive losses and hence overall losses. To facilitate safe operation with a unipolar 5 V gate drive, only the switches that have a typical gate plateau at ≤ 3 V are considered in this design.

Table 4.2 compares the key parameters of the switches with superior FOM and small footprint for 60 V rated switches. These switches listed here are suitable for leg switches. Once again, only the switches that have a gate plateau ≤ 3 V are considered here to ensure safe operation with a 0-5 V gate drive. Since the leg switches carry current through the body diode for a tiny duration, it is essential to select switches with a low voltage drop in reverse conduction.

The selection of suitable switches for both arm and leg switches is based on the target efficiency

of the system. The loss equations described in equations (4.3)-(4.5) illustrate the dependence on switching frequency. The gate drive losses are also a function of the switching frequency. As the targeted efficiency is over 99% on a 300 W rated converter, the total allowable losses are 3 W. Loss estimation for each of the arm and leg switches listed in Table 4.1 and Table 4.2 are performed for different switching frequencies.

Device	C_{oss} @ V_{DS}=50V	$R_{DS(ON)}$ @ T_j =25 C, V_{gs}=5V	Qg(tot) @ V_{gs}=5V	Package dimensions
GaN Systems GS61008T	280 pF	10.5 mΩ	12 nC	7.0 x 4.0 x 0.54 mm
GaN Systems GS61004B	140 pF	15 mΩ	6.2 nC	4.6 x 4.4 x 0.51 mm
EPC2022	840 pF	2.4 mΩ	13 nC	6.05 x 2.3 x 0.78 mm
EPC8010	25 pF	120 mΩ	360 pC	2.05 x 0.85 x 0.81 mm
Nexperia PSMN015-100YL	200 pF	40 mOhm	50 nC	6.20 x 5.0 x 1.5 mm
Vishay SiR882DP	1210 pF	9.2 mΩ	18.3 nC	4.4 x 6.6 x 1.1 mm

Table 4.1: Switches with superior FOM considered for arm switches.

Device	C_{oss} @ V_{DS} =25 V	$R_{DS(ON)}$ @ T_j =25 C, V_{gs}= 5V	Qg(tot) @ V_{gs}= 5V	Package dimensions
On Semi NTMFS5H600NL	1230 pF	1.7 mΩ	40 nC	1.0 x 4.9 x 5.9 mm
EPC2031	900 pF	2.6 mΩ	20 nC	6.0 x 2.2 x 0.78 mm
EPC 2020	1020 pF	2.2 mΩ	16 nC	6.0 x 2.2 x 0.78 mm
On Semi NVMFS5C673NL	450 pF	11 mΩ	4.5 nC	1.0 x 4.9 x 5.9 mm

Table 4.2: Switches with superior FOM considered for leg switches.

A loss estimate in the region of 2.5 W at 100% rated load current is set as the objective in order to provide room for other parasitic losses in the final system. Any losses well below 2.5 W will result in higher efficiencies, but the lower switching frequency has a direct impact on the power density of the system. So, loss estimates in the region of 2.5 W is selected as the key objective.

Using this objective to determine the estimates (using an m-file) for each switch results in combination of GS61008T and NTMFS5H600NL providing the optimal losses in the system. This implies that using a combination of GaN switches (for the arm) and Si MOSFETs (for the leg) provides the desired loss estimates. The Si MOSFETs on the leg switches also provides a lower voltage drop during reverse conduction (or equivalent body diode) compared to the GaN switches. Figure 4.7 illustrates the estimated loss components for each of the arm switches (considering 10 such arm switches as needed in the system) listed in Table 4.1.

It can be observed that the GaN switches (Selection 1-3) have much lower losses than the Si

MOSFETs in the table (Selection 5-6). The plots are obtained for a switching frequency of 85 kHz

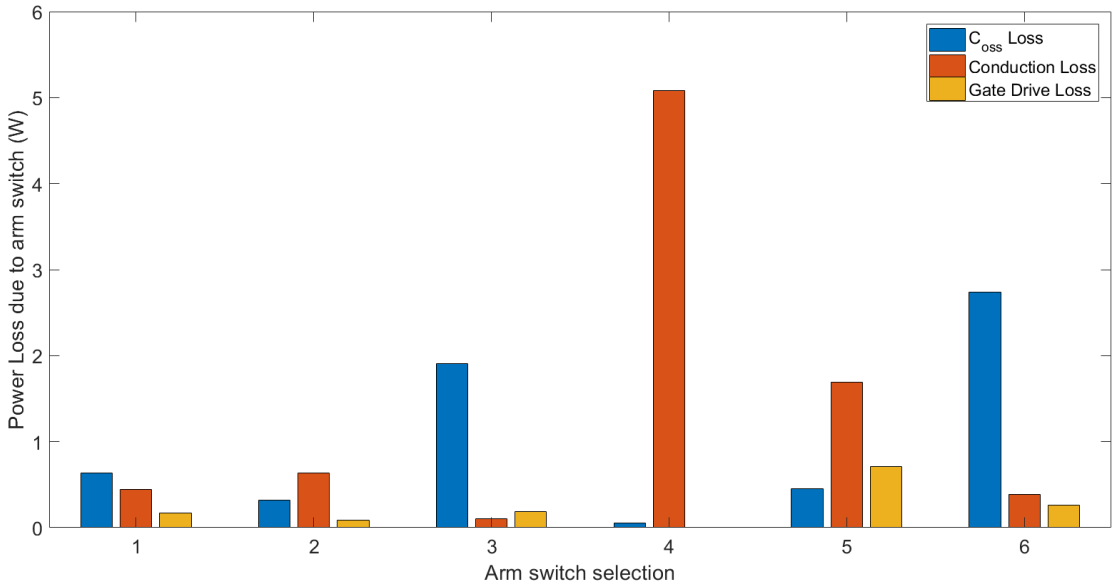


Figure 4.7: Estimated loss distribution for different arm switches in Table 4.1.

Using GS61004B over GS61008T can lead to better loss estimates for the arm switches (selection 1 over 2). However, the GS61008T (selection 2) is still preferred in terms of its superior ability to be top-cooled in a high power-density layout. In the loss estimate, a factor of 1.5 X is used to determine the $R_{DS(ON)}$ at a junction temperature of 100 C. A unipolar gate drive of 0 to 5 V is used for both arm and leg switches. An efficiency of 60% is assumed for the gate drive power supply source. Switching frequencies in the range of 85 to 100 kHz results in the estimated losses to be in the 2.5 W region. However, the exact choice of switching frequency is made at a system level that also includes losses in passive components and other stray traces that haven't been considered here. Figure 4.8 illustrates the estimated loss distribution for the leg switches (considering all 4 'leg' switches) listed in Table 4.2. the plots are obtained for a switching frequency of 85 kHz. It can be observed that the Si MOSFET (selection 1) has the lowest estimated losses. Table 4.3 illustrates the estimated individual switch losses and the overall losses in the system based on this.

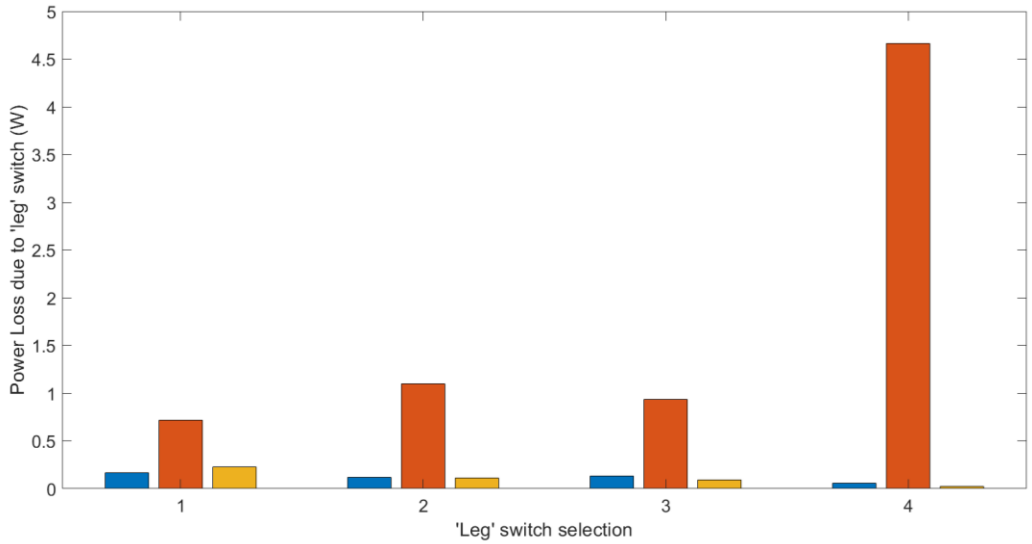


Figure 4.8: Estimated loss distribution for different ‘leg’ switches listed in Table 4.2.

Switch type	Loss per switch @ fs= 85 kHz	Loss per switch @ fs = 100 kHz	No. of switches	Total estimated loss @ 85 kHz	Total estimated loss @ 100 kHz
Arm (GS61008T)	128 mW	140 mW	10	1.3 W	1.4 W
Leg (NTMFS5H600NL)	250 mW	260 mW	4	1.0 W	1.04 W
Total Loss:				2.3 W	2.44 W

Table 4.3: Estimated loss for the overall converter considering conduction, switching and gate drive losses.

4.3.2 Design of Passives

The goal of the passive component design here is to minimize the overall volume of the combined LC network in each arm of the resonant Dickson converter. This is instrumental in driving up the power density of the overall system. The switching frequency and hence resonant frequency are

determined by the overall efficiency targets of the system (Section 4.2- A). For that given switching frequency, the arm inductor and capacitor are selected to provide the minimum volume. Unlike the SCCs in [23] arm inductance must be placed in series with the arm capacitors as shown in Figure 4.2. This is to provide the ability to independently tune loop individual loop inductors. Some resonant SCCs [23] utilize trace inductors to shape arm currents leading to zero current switching. But, the need for longer traces constrains power density of the overall converter. Air-core inductors are also used to eliminate the need for longer traces [28]. However, using air-core or trace inductors results in low inductances values which in-turn increases the required arm capacitance for a given resonant frequency. This may not necessarily provide the lowest passive component volume.

The relationship between damped resonant frequency (ω_d) and the magnitude of inductance (L), capacitance (C) and resistance (R) in each loop is determined using the second-order under-damped expression:

$$w_d = \sqrt{\left\{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2\right\}} \qquad (4.7)$$

From the discussion in Section 4.2, the 280/28 V resonant converter has a total of five different loops in each switching state. Each arm capacitor is part of two different loops over a switching period. All, but the inner and outer-most loops have identical loop capacitances. In this design, the overall loop inductance and capacitance are split between the two adjacent arms that form the loops. Arms 2 through 9 are designed to have identical arm R,L and Cs. The inner and outer-most arms have a different split.

Chip-scale MLCC ceramic capacitors are used for the arm capacitors and chip-scale low resistance inductors are used for the arm inductors. As the different arm capacitors have different voltage ratings, it is essential to achieve the required arm capacitance considering the variation in

capacitance of MLCC type capacitors with voltage. Based on commercially available MLCC capacitor specification [58], two different capacitor ratings are identified as suitable candidates to achieve low overall volume for arm capacitance. The magnitude along with individual capacitor volumes are illustrated in Table 4.4.

Capacitance (uF)	Rated Voltage (V)	Volume (mm^3)
2.2 uF	450 V	78 (2520 package)
4.7 uF	100 V	78 (2520 package)

Table 4.4: Suitable MLCC capacitors commercially available for selection of arm capacitance.

A combination of commercially available low-resistance chip inductors (that can safely carry arm currents) and MLCC ceramic capacitors in Table 4.4 is considered in determining optimum volume for the "LC" network in the converter arm. The chip inductors with a resistance over 2 mΩ are not considered in this design to limit the overall losses in the network. Several different commercially available LC combinations suitable for the converter arms were considered before narrowing down on seven key combinations suitable for a 85 kHz resonant frequency. Figure 4.9 illustrates these different combinations along with the overall volume of the LC network considering all arms of a 280 V/28 V resonant Dickson converter. Similar analysis can also be done for the different arms of the converter. The inductance and capacitance required for each of these combinations along with the overall component volume is described in Table 4.5. The capacitances in each of these combinations are achieved by a combination of the capacitors described in Table 4.4.

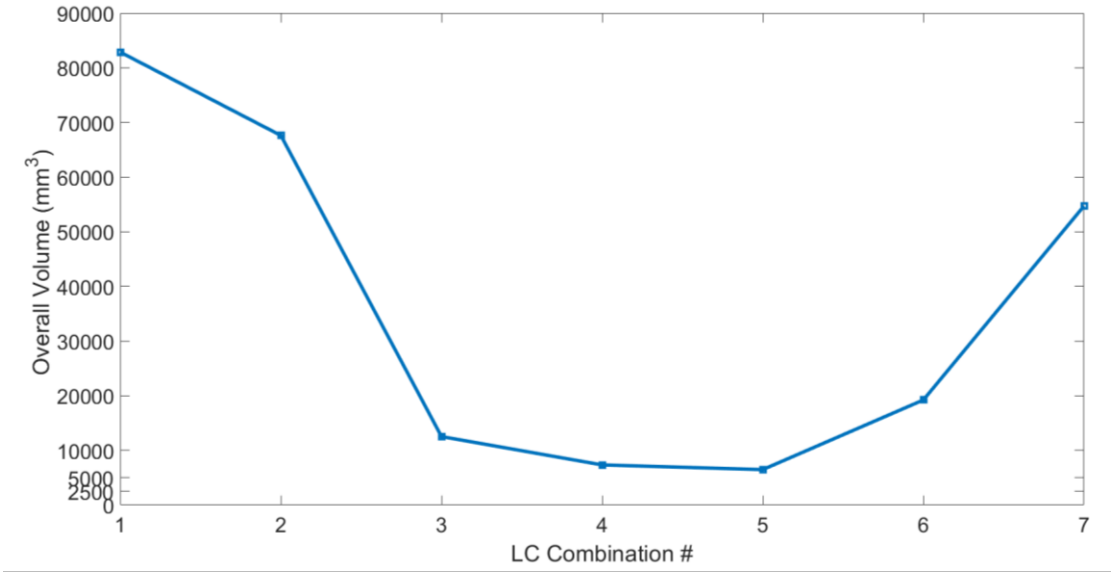


Figure 4.9: Overall volume of LC network for seven different LC combinations based on commercially available components for a resonant frequency of 85 kHz.

It can be observed that the minimum volume of about 6450 mm^3 is obtained for combination 5 which uses an arm capacitance of 2.7 uF and arm inductance of 1.2 uH. This solution has an overall volume, 12 x lower than an air-core solution (combination #1).

This combination is used in designing the prototype converter in this chapter. Selecting a 85 khz switching frequency also provides margin for the core losses associated with the selected inductor. The reported overall volume of the LC requirement is the sum of the physical volume of all the required components. It does not consider the tolerances and spacing requirements needed for mounting these components.

LC Combination #	Capacitance (uF)	Inductance	Resistance	Manufacturer (Inductor)	Overall Volume (mm^3)
1	100 uF	23.5 nH (Air core)	1.05 mΩ	Coilcraft	82,866
2	78 uF	79 nH (Air core)	2.11 mΩ	Wurth	67,620
3	15 uF	220 nH	1.2 mΩ	Wurth	12,525
4	4.0 uF	680 nH	1.65 mΩ	TDK	7,338
5	2.7 uF	1.2 uH	1.2 mΩ	Wurth	6,476
6	1.2 uF	2.2 uH	1.98 mΩ	Vishay	19,221
7	0.8 uF	3.3 uH	1.98 mΩ	Wurth	54,716

Table 4.5: Specifications of the LC network for a 280 V/ 28 V resonant Dickson converter for a resonant frequency of 85 kHz.

4.4 Efficient and Compact Gate Drive solution for GaN HEMTs.

For a 300 W rated system with a target efficiency of over 99%, the total allowable losses are < 3W. The proposed resonant Dickson converter configuration consists of a total of 14 switches. Therefore, optimizing gate drive efficiency forms an important part of loss optimization.

Additionally, the gate drive stage must be easily integrable into the overall system to achieve high power density.

In hard-switched converters, high-speed switching (fast edge rates/slew on drain-source voltages, 10 to 100 kV/us) is key to reducing switching losses. Suh fast-edge rates reduce the overlap time between falling drain-source voltages and rising currents and vice-versa. In the case of resonant converters, zero-current switching eliminates the losses due to overlap of current and voltage transitions. Due to this, the benefits of switching at high slew rates are negligible for resonant, zero-current switched converters such as the resonant Dickson converter presented here. This coupled with the sub-100 kHz switching frequency relaxes the requirement for ultra-fast rise and fall times on the drain to source voltage. This allows slower switching of the gate-source waveform as the voltage/current slew is controlled by the gate voltage profile. For a unipolar gate-source voltage (V_{gs}) of 0 to 5 V, the arm switches (GaN HEMTs) have a typical total gate charge requirement $Q_{g(tot)}$ of 12 nC. The leg switches, on the other hand have a total gate charge of 40 nC. To minimize the total gate drive losses, a unipolar 0 to 5 V drive is used to drive the individual Si MOSFETs and GaN HEMTs. Typically, GaN HEMTs have a low gate threshold voltage (1.7 V in the case of arm switches). In fast-switching GaN applications, a bipolar gate drive is normally used to protect against inadvertent turn-on due to miller injection [59]. However, the ability to switch the resonant Dickson converter slower without compromising on the efficiency or power density of the system enables a unipolar gate drive.

Gate drive losses due to a single GaN HEMT can be estimated using the following expression,

$$P_{gate} = Q_{g(tot)} * V_{gs} * f_s$$

Where, P_{gate} represents the gate driver loss and f_s represents the switching frequency.

At a switching frequency of 100 kHz, this leads to a gate drive loss of 6 mW per GaN. For the leg

switches that use Si MOSFETs, the gate drive loss per MOSFET is about 20 mW. Although, the 6 mW and 20 mW loss per switch numbers are only a small fraction of the 300 W base power of the system, it translates to a much bigger footprint due to a few key reasons discussed below.

In most SCCs, individual switches are all floating. The most common gate drive method is to use the following set of components: an isolated gate driver and an isolated power supply to power the secondary side of the gate driver IC [59]. At 100 kHz, these isolated drivers consume about 8 mW to power the internal circuitry [60]. So, the total power drawn from the isolated DC-DC converter is 14 mW. Commercially available 5 V isolated power supplies [61], [62] are rated for 100 mW to 250 mW. They have an estimated efficiency of 10 to 15 % when delivering a load of 14 mW. This implies a power draw of 93 mW by each isolated DC-DC converter powering the GaN gate driver. Considering all the ten GaN HEMTs in the system, the total gate drive power draw is about 1 W. The gate drive power needed to drive the Si MOSFETs in the system is about 500 mW considering a 25% power supply efficiency. So using an isolated gate driver IC along with an isolated DC-DC converter results in an estimated power consumption of 1.5 W for the gate drive stage alone. 1.5 W of losses on a 300 W base amounts to 0.5% loss and majorly constrains the ability to limit the overall losses to within 1% of the rated power in the entire system.

A bootstrap based gate drive solution is often considered as an alternative to isolated drivers. However, the presence of multiple floating switches would require a cascaded bootstrap configuration. Such cascaded schemes [63] rely heavily on the load current and dead-time of the switches. With GaN HEMTs, due to their large reverse conduction voltage (>2 V) it can also lead to overcharging of the bootstrap capacitors during dead-time. Individual bootstrap capacitors also have different voltage levels. LDO s are normally used to regulate voltage at the gate terminals. This leads to low-efficiency. As 4.5 to 6.0 V is the range of safe and efficient operation for the arm

switches [59], variation in individual bootstrap capacitor voltages can lead to potential risks. Modified bootstrap methods to include a high-voltage capacitor to achieve the required charge pump has also been explored [63]. However, the requirement for a new set of high-voltage capacitors apart from the arm capacitors leads to increased volume.

A pulse-transformer based gate drive solution [64] has not been explored much for GaNs. The size and slew rates of the pulse-transformer are often considered limitations for a fast-switching GaN application. However, in the resonant Dickson converter, there are a few aspects that are favored by the system. First, the converter operates at a fixed duty cycle. So, dynamic variation in duty cycle is not a requirement. Next, the zero-current switching nature and sub-100 kHz switching frequency of the converter relaxes the requirement for fast slew rates. These enable an optimized design of a pulse transformer stage for high efficiency.

A typical pulse transformer-based gate drive configuration for GaN is illustrated in Figure 4.10. The configuration eliminates the need for individual isolated power supplies in each gate drive stage.

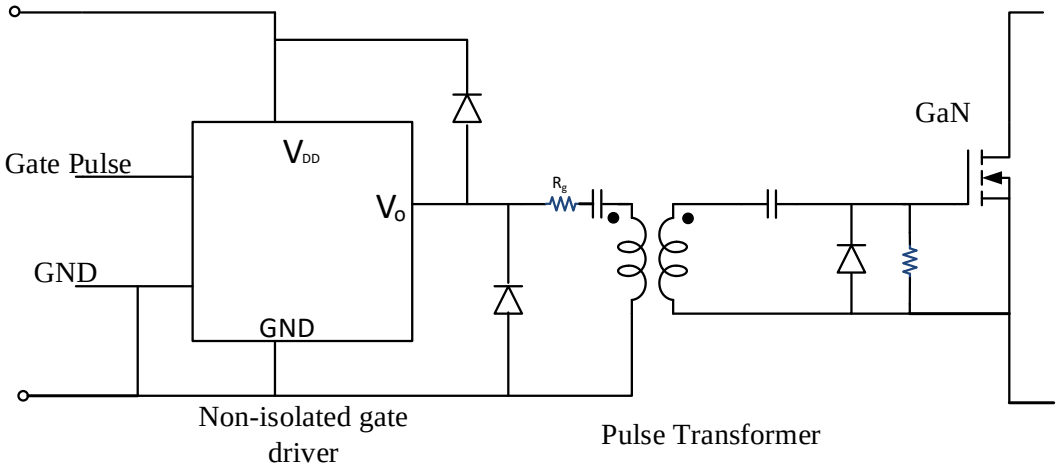


Figure 4.10: Basic block schematic of pulse-transformer gate drive stage.

To adopt the pulse-transformer based gate drive configuration for the resonant Dickson converter,

the overall size and efficiency of each individual gate driver stage is optimized. Table 4.6 lists some of the key features in individual gate drive components that enable high efficiency and power density at the gate drive stage.

Component of gate drive stage	Key feature (typical values at 25 deg. C)
Transformer: HM42-20002LFTR	Low-profile: 3mm height, low winding resistance of 0.6 ohms, 1.5 kV isolation
Gate driver IC: FAN 3122CMX	1 mA no-load current at 100 kHz, V_{DD} range: 4.5 to 8 V, UVLO at 4 V.
Primary and secondary side Schottky diodes: BAT60A	120 mV forward voltage drop, low reverse current 0.3 mA

Table 4.6: Key features of the pulse-transformer gate drive stage suitable for a GaN gate drive.

The same gate drive configuration is also used to drive the Si MOSFETs (leg switches) of the resonant Dickson converter. Figure 4.11 illustrates experimental waveforms showing the rise and fall times associated with driving both GaN and Si MOSFETs using the pulse-transformer based gate drive stage discussed above. Here, they are both driven with a gate resistor, R_g of 3.3 Ohms and a supply voltage, V_{dd} of 5.5 V. In the overall system, the individual gate resistances for the MOSFETs and GaNs are tuned to achieve suitable quality factor and appropriate delay sizing between the arm and leg switches to reduce switching loss of leg switches (Section 4.3.1).

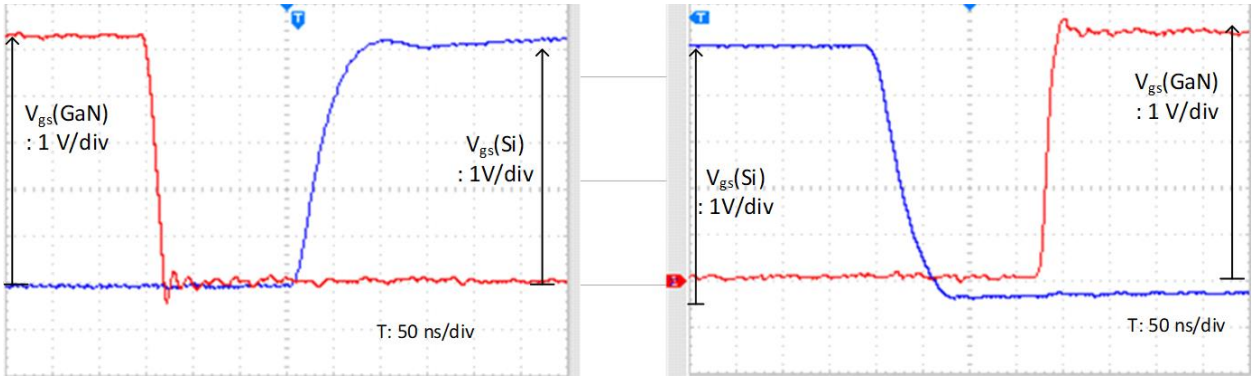


Figure 4.11: Gate-source (Vgs) voltage of GaN (red) and Si MOSFET (blue) when driven using pulse-transformer based drive (a) falling edge of GaN and rising edge of MOSFET, (b) falling edge of MOSFET and rising edge of GaN.

To compare the performance of different gate drive technology used for GaN HEMTs, the total gate drive loss is considered as the base power. The power drawn from the gate drive stage is then measured by measuring current draw on V_{dd} rail. A term "gate drive efficiency" is defined here. The gate drive efficiency is a ratio of the gate driver losses to the power drawn by the gate drive stage. A higher efficiency indicates a more efficient driver. Table 4.7 lists the measured power draw from the gate driver stage to drive the GaN HEMT. At 100 kHz (which is the region of interest for the operation of the converter), the typical efficiency of the entire pulse-transformer based gate drive for 100kHz switching is 47%.

Switching frequency	Power drawn	Gate drive Efficiency
100 kHz	12.8 mW	47%
200 kHz	30.0 mW	40%

Table 4.7: Measured power draw from pulse-transformer based gate drive stage for GaN.

However, the key benefit of using the pulse-transformer based gate drive stage comes from the overall configuration of the gate drive architecture. As discussed before, there are a total of 10 floating GaN HEMTs in the overall system. This would require a separate pulse transformer-based gate drive stage for each switch. However, the isolation here is provided by the pulse-transformer and a single DC-DC converter can now be used to power the primary side of all the gate drives.

Considering all 10 switches, the total power draw from the DC-DC converter is about 130 mW. Using a 250 mW power supply to power this load leads to a power supply efficiency of 75% [61]. The power draw from the primary of the DC-DC converter is then 175 mW. Comparing to the 1 W power draw in the case of the isolated gate driver configuration and individual DC-DC converter, the total power draw in the pulse-transformer case is about 5.4 times lower. The need for a single DC-DC converter in this case also leads to a compact gate drive structure that can easily be integrated into the rest of the system. This is crucial for the overall power density of the system. The total power draw considering drivers for all MOSFET and GaN HEMT gate drivers is 260 mW. Table 4.8 summarizes the different types of gate drivers discussed in this section. The high efficiency and compact nature of the pulse-transformer based gate drive stage makes it suitable for the current application.

Gate driver type	Power draw/Pros and cons
Isolated Gate driver + individual DC-DC converter	Low gate drive efficiency, estimated power draw of 930 mW for 10 GaN HEMTs
Pulse-transformer based driver + common DC-DC converter	Ultra-high gate drive efficiency, power draw of 175 mW for 10 GaN HEMTs (over 5X improvement over previous case)
Cascaded bootstrap	Potential over- charging issues, need for LDO reduces efficiency.

Table 4.8: Summary of different gate drive techniques for GaN HEMTs at 100 kHz switching.

4.5 Prototype Development

A modular approach (in volume and form-factor) is used to build the prototype. The 280 /28 V converter is split into ten individual modules. Each module essentially represents one arm of the converter and fully contains gate drive stage, GaN HEMTs and the passive components in each arm. Figure 4.12 (a) and (b) illustrate the top and bottom view of one such module respectively.

A US quarter is shown here for size reference only. The overall dimensions of individual module with all components and connectors mounted is: 41 x 11 x 8 mm.

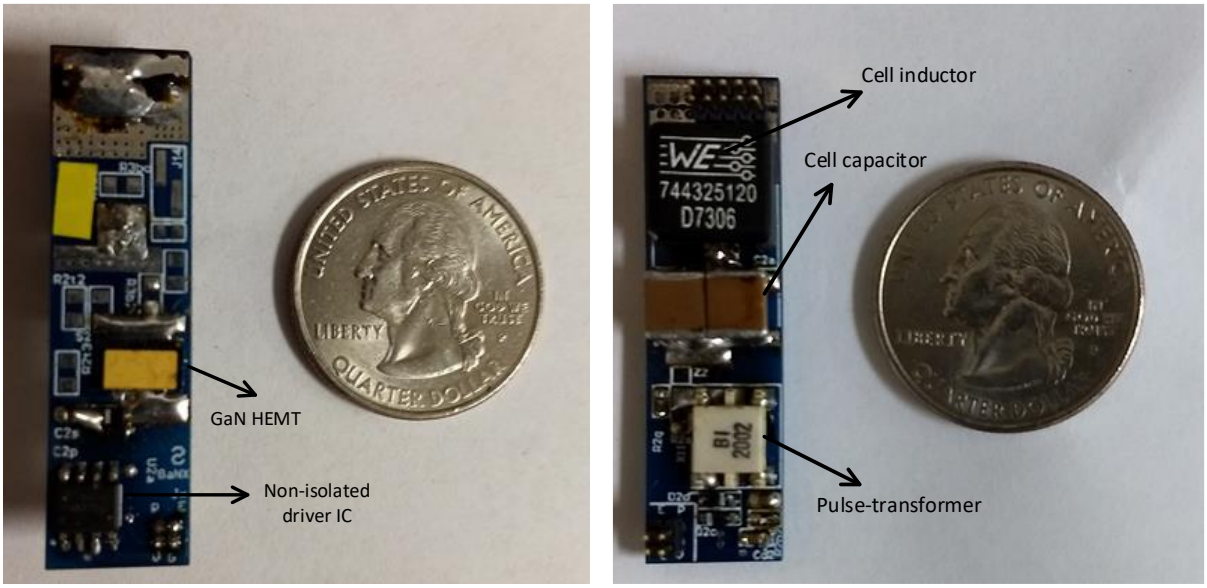


Figure 4.12: (a) Top view of one module of the overall converter; (b) Bottom view of one module of the overall converter.

Ten individual modules (identical to the one shown in Figure 4.12 are connected to achieve the 280 V/28 V resonant Dickson converter. As described in Section 4.2, the innermost and outermost modules require different inductance values to achieve identical resonant frequencies in every loop. However, the same physical package is selected for these inductors in order to retain the same structure for all the modules in the converter.

The leg switches (Si MOSFETs) and the analog PWM IC are placed on a separate interface board that interfaces to these modules by means of board-to-board connectors. The fully assembled resonant Dickson converter prototype consisting of all the 14 switches, passive components and connectors is shown in Figure 4.13.

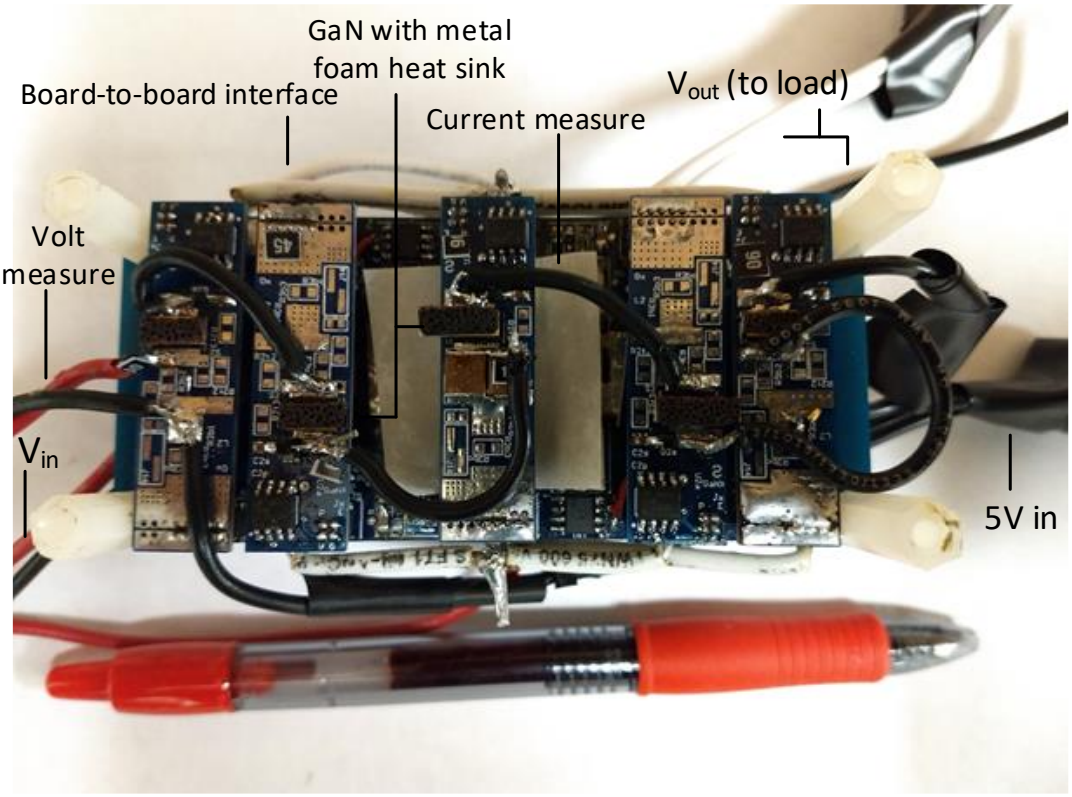


Figure 4.13: Top view of fully assembled 280/28 V 300 W resonant Dickson prototype.

The figure also shows key terminals along with wires used for probing currents and a low-profile metallic foam heat sink on the top cooled GaN switches. The spacing between boards and individual arms is part of thermal design of the system. This is to provide natural air convection and to eliminate the need for large external forced air cooling or cold plates. A resistive load bank is used to load the converter and perform efficiency tests at different operating points. The overall dimensions of the power converter are: 81 x 41 x 17 mm. The overall power density of the converter is 87 W/in^3 or 5.3 kW/L. The pie chart in Figure 4.14 illustrates the percentage volume distribution of the overall converter. It can be seen that the volume of the power components (passive, gate drive, switches) accounts for a much lower volume. The power density of the power stage alone results in about 270 W/in^3.

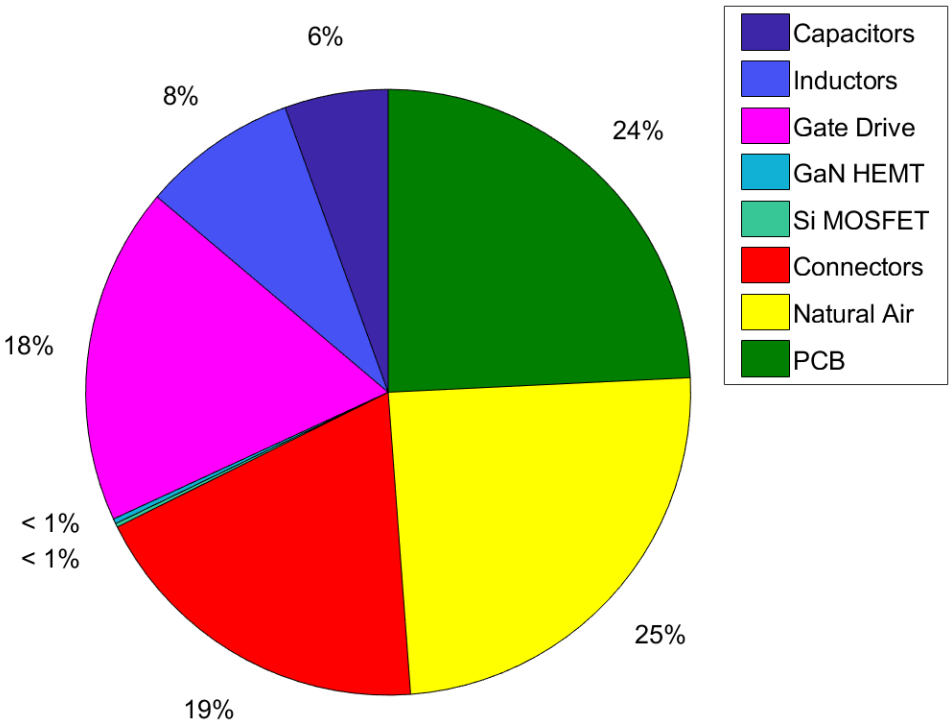


Figure 4.14: Volume distribution of the prototype converter.

If a 1MHz switching frequency were used (hypothetically), volume of passives (L and C) can be reduced 3x. Predicted total volume improvement: 13.5 %. But, losses increase by over 400%, almost certainly needing extra cooling. So, increasing switching frequency may not necessarily improve power density.

4.6 Experimental Results

The 280 V DC input to the converter is derived from a 240 V, 3-phase AC power supply using a standard variac, rectifier and LC filter configuration. A variable resistor load bank is used to load the converter. In accordance with the loss optimization in this chapter, the converter is operated at a switching frequency of 85 kHz. To achieve zero-current switching, the resonant frequency in each loop is designed to be 85 kHz. The design of passive components for this resonant frequency is described in Section 4.3.2.

The waveforms in this section are labeled using the following nomenclature : V_{Sx} represents voltage across the drain - source of switch S_x. I_x represents current through Switch S_x. Positive current is represented as flowing from drain to source of switch S_x. V_{Cx} represents AC voltage ripple across capacitor C_x.

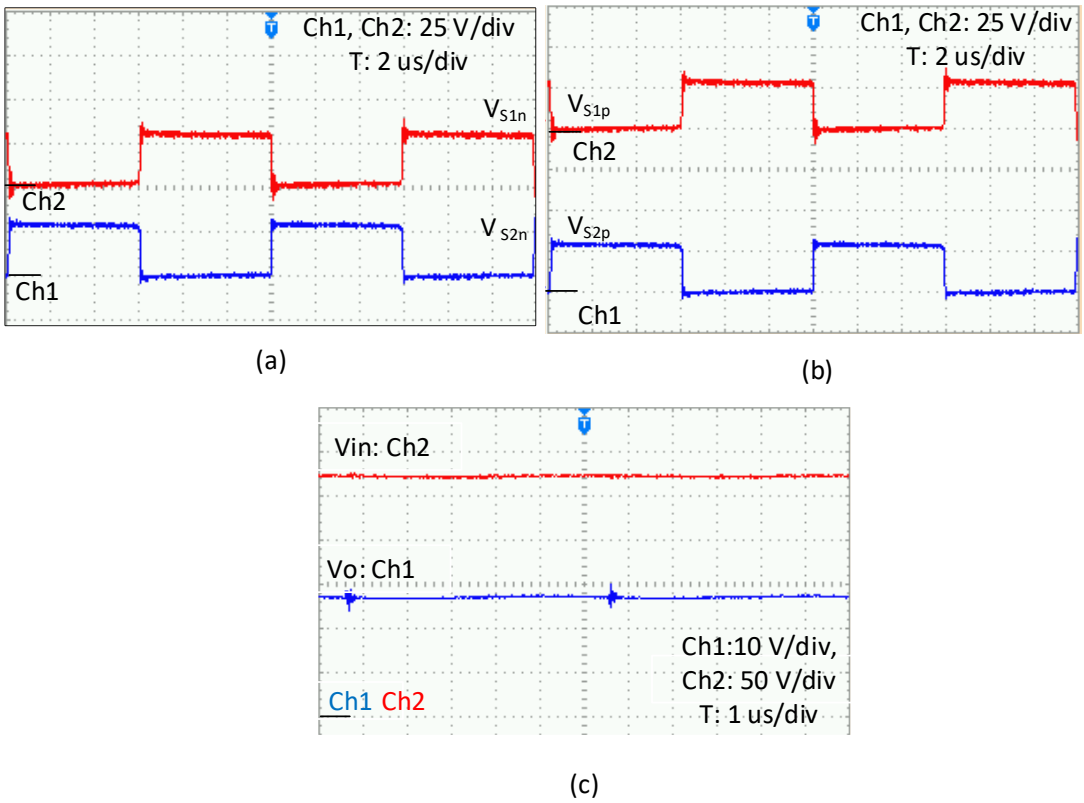
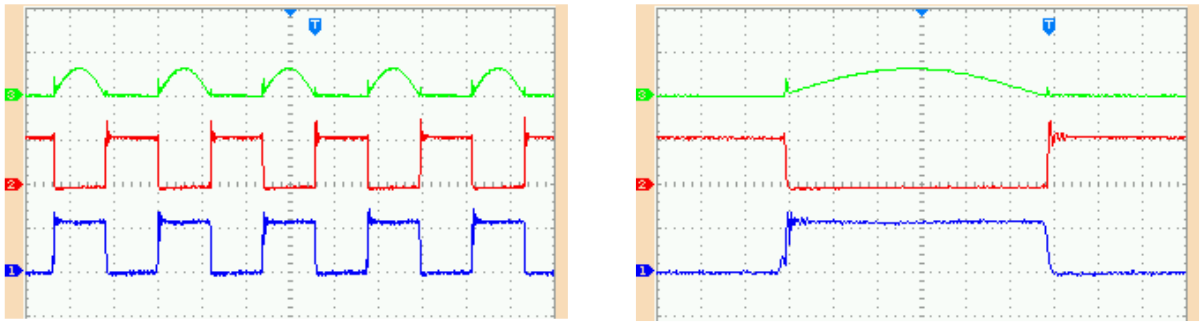


Figure 4.15: (a), (b) Leg switch waveforms at Vin=280 V and full load; (c): Input and output voltage waveforms at rated load and input voltages.

Figure 4.15 (a)-(b) illustrate the complementary nature of the leg switches (Si MOSFETs) while Vin =280 V and at full load (~10 A load current). The nominal voltage stress of the device is 28 V and the nominal output voltage is 28 V. The input and output voltage profile at this load is illustrated in (c).

Figure 4.16 (a) illustrates the complementary nature of voltage across GaN switches (arm-switches) S_{7a} (red) and S_{8a} (blue). Current through switch S_{7a} is illustrated in Ch 3 (green). The zero-current switching nature of the converter is evident in the half-sine current waveform. The resonant time period is about 5.8 µs. Zero-current switching is achieved at both turn-on and turn-

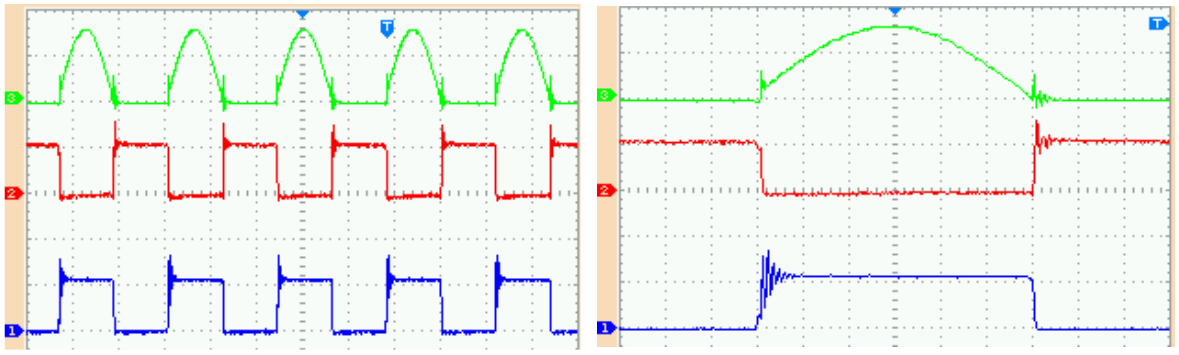
off of the switch. Figure 4.16 (b) illustrates a zoomed-in version of Figure 4.16 (a) at a 1 us time scale. The load current is 4 A which is about 2.5 x lower than full-load current.



(a) (b)

Figure 4.16: (a): GaN switch voltage waveform at 40% rated load. Ch1, V_{S8}: 50V/div, Ch2, V_{S7}: 50 V/div, Ch3, I_7: 2A/div, T: 5us/div; (b): Zoomed in version of (a), 1us/div.

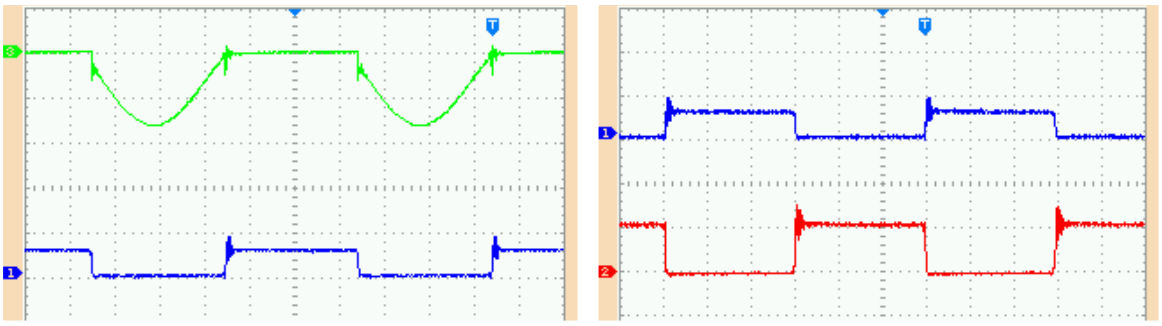
Figure 4.17(a) illustrates GaN switch voltage and current waveforms at 100% rated load of 10.5 A. Ch1 (blue) represents Switch S_{5a} and Ch2 (red) represents switch S_{4a}. Upon comparison with the current waveform in Figure 4.16, it can be observed that the resonant time-period is identical and that it doesn't vary with load and between different current loops in the converter. Ch3 (green) represents currents through switch S_{4a}. The peak switch current is 3.2 A at full-rated load.



(a) (b)

Figure 4.17: (a): GaN switch voltage waveform at 100% rated load. V_{S5}: 50V/div, Ch2, V_{S4}: 50 V/div, Ch3, I_4: 2A/div,: T: 5us/div; (b): Zoomed in version of (a), T: 1us/div.

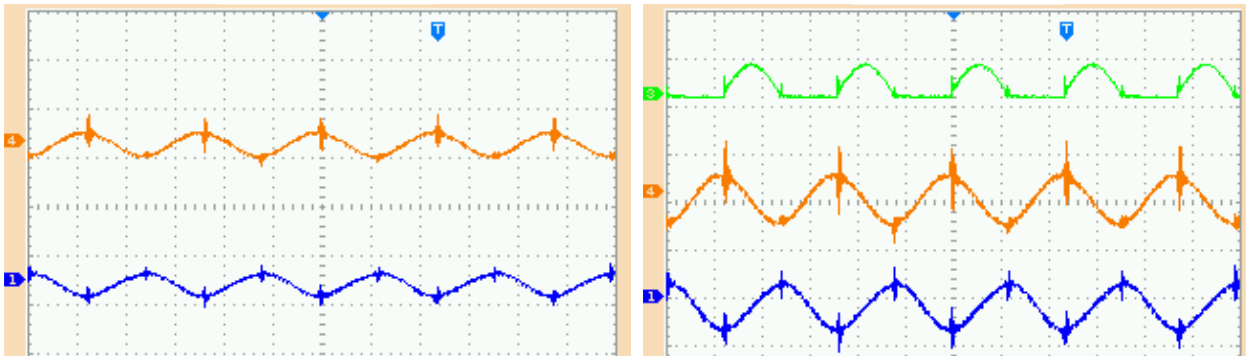
Figure 4.18(a) illustrates the voltage across inner-most arm switch S_{1a} on Ch1 (blue). The current through the switch (measured source to drain), -I1 is shown on Ch3 (green). It can be observed that the design ensures identical resonant frequency on the innermost arm and the outer arms. Figure 4.18 (b) compares the inner-most switch voltage stress (blue) with switch S_{2a} (red) The innermost switches have only ½ the voltage stress of the switches on the outer arms of the converter (28 V over 56 V for other arms).



(a) (b)

Figure 4.18: (a) Current and voltage waveforms for inner-most current loop at 100% rated load. Ch1, V_{S1}: 50 V/div, Ch2:-I_1: 2A/div; (b) Comparison to switches outside inner-most loop, Ch1, V_{S1}: 50 V/div, Ch2, V_{S2}: 50 V/div; ,T: 2us/div.

Figure 4.19(a) illustrates the AC capacitor ripple across two different arm capacitors, C_9 and C_6 at 100% rated load. The peak-to-peak ripple voltage is 6 V. As these capacitors are on different arms of the converter, this implies that the arms have equal capacitances. Figure 4.19 (b) illustrates the arm capacitor ripple across two more arm capacitors, C_5 (Ch1) and C_8 (Ch4). This is consistent with the ripple voltage seen on the other two arm capacitors illustrated in Figure 4.19(a). Ch3 super-imposes current through Switch S_{6a}. When the switch is ON, the switch current flows through capacitors C5 and C6. The voltage on C5 (Ch is seen to ramp up when current I_6 rises.



(a) (b)

Figure 4.19: (a) AC voltage ripple across different arm capacitors at 100% rated load. Ch1, V_{C9}: 10 V/div, Ch4, V_{C6}: 10/div; T: 5us/div (b) Ch1, V_{C5}: 5 V/div; Ch4, V_{C8}: 5 V/div, Ch3: I_6: 5A/div, T: 5us/div.

The variation in voltage step-down ratio with different load conditions is an indicator of the load regulation. Table 4.9 illustrates experimentally obtained data for voltage step-down ratios for different loads conditions at a nominal input voltage of 280 V. The maximum variation in gain from 9% rated load to 98% rated load is within 1.06% considering gain of 10 as the nominal or base gain. This implies good load regulation considering that the system does not use closed loop feed-back control.

Load Power	V_{in}/V_o
294.0 W	10.106
225.4 W	10.082
171.7 W	10.060
159.6 W	10.056
109.03 W	10.032
47.88 W	10.012

Table 4.9: Voltage step-down ratio vs load power at steady-state, V_{in}=280 V.

The overall efficiency of the converter is also measured with a nominal input voltage of 280 V. The load is varied by varying the load resistance bank to achieve different load currents. As the

prototype uses an external 5V supply for the gate driver power supply, an efficiency of 60% for the gate drive power is already factored into the individual data points. The converter is operated at a fixed switching frequency of 85 kHz. The data points are plotted in Figure 4.20. The peak efficiency of the converter is 99.07% at a load of 294 W.

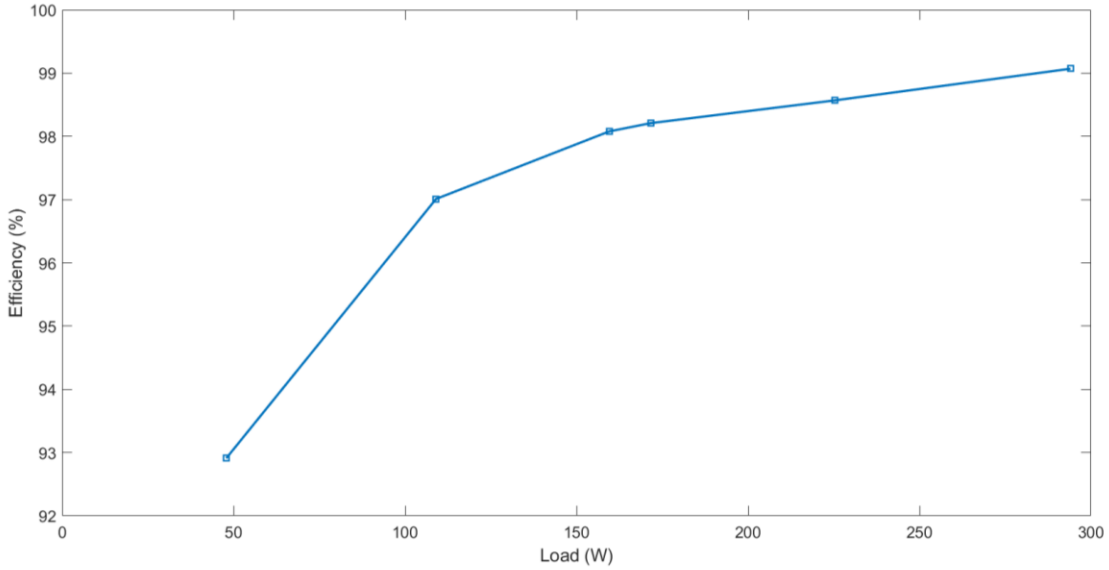


Figure 4.20: Efficiency plots for the 280 V/28 V resonant Dickson Converter.

4.7 Conclusion

This chapter presents the configuration and design of a GaN based resonant converter for large voltage step-down. A prototype with spec comparable to commercial off the shelf power supplies for More-electric aircrafts is designed here. To this effect, a 300 W 280 V/28 V resonant Dickson converter is designed, and results are presented. A peak efficiency of 99.08% and a power density of 87W/in^3 is achieved. The design relies on optimum switch selection, operating modes, high efficiency gate drive stage and optimal passive component sizing to achieve the high efficiency and power density. All these different aspects of design optimization are presented in detail within this chapter. Key benefits of GaN switches such as low C_{oss}, low $R_{DS(ON)}$, low Q_g(tot) and low

threshold voltage are fully exploited in the design. The design and configuration of the resonant Dickson converter presented in this chapter can be extended or provide useful guidelines for other similar wide bandgap-based power converter systems.

CHAPTER 5 CONCLUSION AND FUTURE WORK

The key contributions of this research that help advance the state of the art in Switched capacitor power conversion technology are summarized here. Recommendations for future work for each of the chapters are also described here.

5.1 Summary of Chapter 2

Traditionally, Dickson type converters have two fixed operating states. Operating the converter between these states leads to a fixed voltage gain in boost mode and fixed step-down ratio in buck mode operation. The concept of utilizing additional transition mode operating states for Dickson type converters introduced here breaks away from the norm and enables the possibility of achieving real-time gain variation using switched capacitor converters without adding additional stages down- stream. Detailed analysis, design and operation of a converter incorporating these new transition states is described by designing a prototype 1kW converter suitable for a solar PV application. By regulating the converter output voltage based on the input voltage variation, the overall voltage ratings of the output capacitor is reduced by over 30%. This can result in large savings in overall volume and cost of the system. Any downstream converter in the system would also benefit due to reduced voltage stress. Experimental results and efficiency tests for the converter show negligible loss in efficiency compared to a converter operating in it's traditional operating states. A peak efficiency of 96% is reported for the prototype.

In order to analyze the new operating states, the switched capacitor network is split into multiple equivalent second order circuits. However, as the voltage gain increases, this would result in additional loops making the analysis more cumbersome. In future, a generalized approach to model

the transients in a ‘N’ loop Dickson type converter can help model transients for a high-gain converter.

5.2 Summary of Chapter 3

The introduction of additional operating states in the Dickson type converters leads to several benefits. However, the transient current at the input side of the converter relies on the trace inductance present in individual switched capacitor cells. This may be a constraint for some applications that have a strict tolerance on input side transient current. Chapter 3 focuses on addressing this issue and enable a “smooth” transition in gain. An innovative energy distribution-based approach is used here to minimize the input current transitions seen by the source of the converter. The energy stored in capacitor cells undergoing transition in voltage are either distributed to the load or the immediate adjacent capacitor cell. By selecting optimum timing between the switching of individual switches, this energy re-distribution is well managed leading to a significant reduction in input side current transient and also minimizing the reliance on trace inductors present in individual cells. Experimental results on a 1 kW prototype using the proposed soft gain-transition methods illustrates the benefits of this method.

Chapters 2 and 3 propose two different approaches to achieving real-time gain variation of the converter. However, in the future, adopting a super-set of both these methods along with optimal placement of trace inductors in the converter circuit may lead to greater benefits in certain applications. By using adaptive control and selecting the optimal transition mode based on load and input conditions can lead to the most optimal results.

5.3 Summary of Chapter 4

So far, resonant switched capacitor converters at ultra-high efficiency and power density are possible for low voltage step-down ratio. At higher step-down ratios, the efficiency and number of components in the systems constrains the overall efficiency and power density. But, the configuration and design methodology proposed in this chapter enables switched capacitor-based converters with ultra-high efficiency and power density at high step-down ratios. Some of the key aspects of the proposed configuration are the ability to maintain minimum number of switches, a distributed inductive-capacitive approach to power transfer in each individual cell, a highly-efficient integrated gate drive stage and optimally designed passive components. Each of these aspects is described in great detail. A 270 V HVDC architecture is common in more-electric aircraft power systems. However, legacy loads on the aircraft still require a 28 V DC supply. This leads to a requirement of 270/28 V DC power supply in more-electric aircrafts. Additionally, airborne applications require a high-efficiency and high power-density. The proposed resonant Dickson configuration is a suitable candidate to achieve these targets. Designing for such a system would also demonstrate the tangible benefits of the configuration and design. In this chapter, the proposed configuration is designed to meet specifications of a 270 V/28 V power converter in a more-electric aircraft. A peak efficiency of 99.1% and a power density of over 5 kW/L is demonstrated for a 300 W converter prototype.

A modular approach is used here to design the converter prototype. Individual switched capacitor module boards are first designed. These are used as basic cells and the overall converter is built using these cells. This leads to some volume used for mounting and stacking the individual cells.

For future versions of the design, directly using one board with all the switched capacitor cells can further improve power density.

As the gate driver stage is of sub-100 kHz switching frequency, the magnetizing inductance (V-us requirement) in the pulse transformer stage leads to longer rise times. However, the zero-current switching operation ensures no additional switching losses due to slower rise times. In the future, designing a custom pulse-transformer with minimum inductance can lead to a suitable solution for high-speed GaN switching.

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