FABRICATION AND CHARACTERIZATION OF MOS_2 NEAR-INFRARED NANO-OPTOELECTRIC DEVICES

By

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ABSTRACT

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With the high-speed development of electronic device, structural miniaturization and integration are the essential elements for new technology creation. Because of the physical limits of silicon-based transistor, needed to develop alternative channel for minimum 5 nm gate length devices, a brand-new materials(2D) such as graphene and MoS_2 has be introduced in to the engineering study. To manufacture the ultrascaled electronic devices, the fabrication method and new material properties are the most important keys.

At present, MoS_2 has become to the most popular new semiconductor materials because of its own advantages in electricity, thermology and mechanics. These advantages make the MoS_2 have a great potential value in Nano-scale electronic device and photoelectric device development. However, most of the scientific research about MoS_2 devices were focused on the visible spectrum study, there is only few reports for MoS_2 in near infrared because people indicated that 2D materials have a weakness in photoelectric response when it reaches into the near-infrared band. This argument not only blocks the path for 2D materials study but also slows down the development in wireless communication, super charging and autopilot applications. In this article, by using different micro-fabrication methods, we set our final goal as improving the photoelectric induction intensity for 2D materials and study the related application.

To my family and friends, for their unconditional support.

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Chapter 1: Research Background and Purpose

1.1 Development Status of 2D Materials

2D materials, sometimes referred to as single lay materials, are crystalline materials consisting of a single layer of atoms. The fast development of research in 2D material can be traced back to 2004 England. The research group Geim, from University of Manchester physics department, posted the paper, Electric Field Effect in Atomically Thin Carbon Films, introduced the first 2D semiconductor material to the public. The research group used traditional mechanical exfoliation method to obtain the semi material substance with the single layer carbon atomic structure and named it as graphene (Figure 1.1.1). Graphene was considered as a new star in 2D material because it breaks the rule that 2D material will be easily collapsed under the high temperature tensions. Single layer graphene is constructed by sp^2 hybrid hexagon carbon atoms. The high mobility (under room temperature), high heat stability and extreme high thermal conductivity make the graphene an outstanding semiconductor material. With the great CVD technic development, graphene has already stepped into the new world industries. By the latest science report, graphene can be developed by using CVD technic into foot size large area [2]. However, the disadvantages of graphene are also obvious. It can be divided into 2 parts. First, by analyzing the structure of graphene people found out that the gap between the conduction band and valence band is approach to 0, which makes the graphene electronic devices on-off state hardly control. It creates a serious block in developing the new generation field effect transistor products [3]. Second, graphene has an ultra-high transparency. Single layer graphene will only absorb 2.3% light energy and the 0-gap structure causes the life time of charge carrier extremely short which can limit the application in new Nano-photoelectric devices.

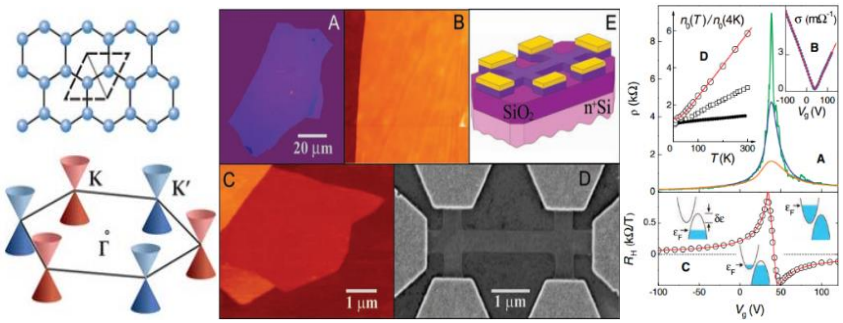


Figure 1.1. 1 The first metallic field-effect transistor based on monolayer graphene and the electrical characterization [1].

To exploit the new application in 2D materials, more and more 2D semiconductor material become to the focus in scientific research study. In 2010, transition metal dichalcogenides family of material (TMDs) break though the weakness in graphene applications. The structure of TMDs is usually presented as MX_2, M is the transition metal elements includes forth group (Ti, Zr and Hf) fifth group (V, Nb Ta) and sixth group (Mo, W). X is the chalcogens elements includes S, Se and Te. One layer of M atoms is sandwiched between two layers of X atoms. Multi-layer MX_2 materials have a great ionic covalent bond which can satisfied the stability inside the system, between each layers the Van der Waals' force (VDW) can keep the structure steadiness [4]. Unlike graphene, TMDs has a large range in energy band gap from ~0eV (TiS_2) to ~2eV (single layer WS_2) [5]. Another advantage of TMDs is that this material can be controlled by changing the number of layers, applied bias and multiple-material contact [6]. These advantages can be widely applied into high performance Nano-electronic devices. In the TMDs family, molybdenum disulfide (MoS_2) is a typical 2D semiconductor material which has been deeply studied. In Figure 1.2.1, it is the multiple-layers MoS_2 atom structure. The thickness of monolayer MoS_2 is ~6.5 Å. Because of the weak VDW force between each layer, MoS_2 flakes

can be exfoliated either in traditional machinal method or liquid stripping. There are 3 states in MoS_2 semiconductor material: 2H, 3R and 1T. The 2H has the most stable construction and appears the semiconductor properties. However, the 1T state has metal properties [7]. By learning the MoS_2 energy band, people found out the flakes MoS_2 has an indirect band gap (~1.2eV), however the monolayer MoS_2 has a direct band gap (~1.9eV) [8]. The energy band gap of MoS_2 makes it become to one of the great short tunnel effect applicators. The direct band gap and indirect band gap give MoS_2 a good property in photoelectric device applications such as monolayer MoS_2 can absorb ~10% incident light (with 615 nm or 650 nm wavelength) [9]. Also, the inside ionic covalent bonds allow the MoS_2 to bear a 25% mechanical deformation [10]. Another advantage of MoS_2 is thermal stability. The MoS_2 photoelectric device will still be functional under ~1100 °C condition [11].

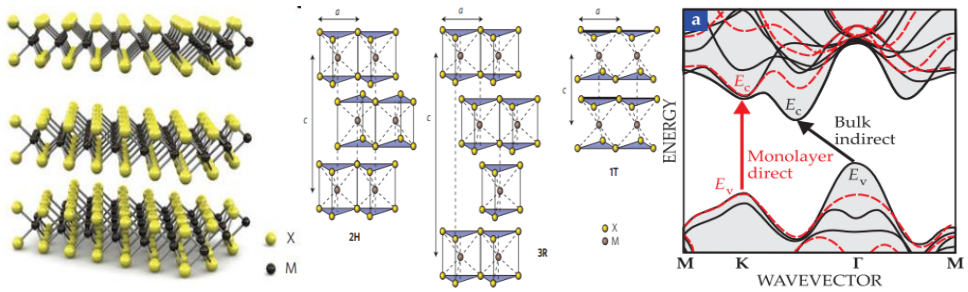


Figure 1.2. 1 The schematic illustration of MoS_2 nanoflakes' structure and band diagram [7].

1.2 2D Semiconductor Material Current Research Status

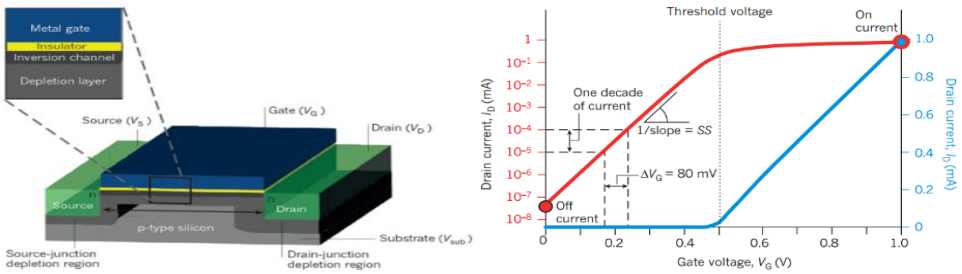
Multiple-functional Nano-devices are the key technic to the modern science. By researching the basic physical and chemical properties of the materials, people will be able to improve and adjust the current technic in device manufacturing. The modern science applications including biomedical, energy storage, logical circuit and photoelectric detections are all required a deep

study in the new material itself [12]. 2D semiconductor material is one of the most important steps in improving method. In this paper, it will focus on the Nano-fabrication and photoelectric device study to prove that 2D semiconductor material is the core part in modern science technology.

1.3 Introduction of Field Effect Transistor

Field effect transistor plays a key position in semiconductor device family. Also, it is one of the important components in large scale integrated circuit (LSI circuit). The very first silicon-based metal-oxidesemiconductor field-effect transistor (MOSFET) was invented in 1960 by Kahng and Atalla [13]. Today, there are 4 different type MOSFET because of their unique channel type and transporting mechanism: enhanced-Ntype MOSFET, depletion mode N-type MOSFET, enhanced-P-type MOSFET and depletion mode-P-ctype MOSFET. For the N-type MOSFET, the basic function is electron transportation. And for the P-type, it usually uses the hole transportation. For the traditional MOSFET structure, there are 3 ports (Figure 1.3.1a): Source, Drain and Gate. The source is defined as providing electrons and the drain is receiving electrons. For the gate usually located at the middle of the channel. The operating principle for a MOSFET is that the electrons will be passing through between source and drain. However, by changing voltage at the gate, people can control the magnitude of current inside the channel (Figure 1.3.1b). For the most 3D semiconductor transistor, there is a Dangling bond located on its surface which will create unavoidable phonon scattering and degrade the performance of electronic devices [14]. On the contrary, 2D semiconductor material is missing the Dangling bond on the surface, all the free carriers are constrained by the atomic layers, it will cause a great

narrow carrier structure and an excellent gate voltage control [14]. In this case, 2D semiconductor material will become to the future field effect transistor.



a. 3D MOSFET structure b. Drain current and voltage characterization

Figure 1.3. 1 The structure and electrical characterization of MOSFET devices.

1.4 Transition Metal Disulphide Field Effect Transistor

At first, researchers were focused on the 3D semiconductor material channel effect study. For example, in 2004 Rutgers University, Podzorov's group first time reported that transition metal disulphide has a high mobility in field effect transistor [15]. During their study, researchers were using the disulphide as channel material discussed the field effect on WSe_2(thickness ~10mm). the final report indicated that the mobility of this new field effect transistor can achieve ~500cm^2/Vs which is as good as the p type silicon-based transistor. Also, the report shows that under the low temperature environment, the device has a bipolar transportation and onoff characters. However, by using the crystal block structure as channel which will hard obtain a high on-off ratio (~10^4). With the development in 2D semiconductor study, people began to use the atomic TMDs to fabricate the transistor channel. In 2007, Ayari's group from University of Maryland used traditional mechanical exfoliation method and extracted the atomic MoS_2

monolayer structure [16]. This new transistor not only keep the advantage of high mobility character but also improve the on-off ratio (~10^5).

Besides the high mobility on MoS_2 device, p-n junction effect can be also applied in the fabrication steps. This method largely increased the application in field effect transistors. Choi' group from Sungkyunkway University first time used the different metals on electrodes fabrication in MoS_2 device. By using $AuCl_3$ solution and Au Nano-particles on the Pd side and using BN to protect the other side of the transistor successfully achieved the p-n junction structure (Figure 1.4.1) [17].

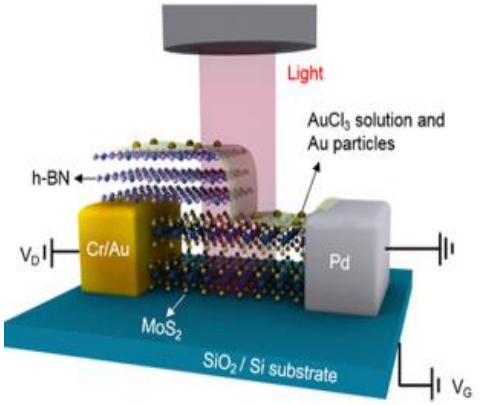


Figure 1.4. 1 The schematic of chemical doping p-n junction MoS_2 devices.

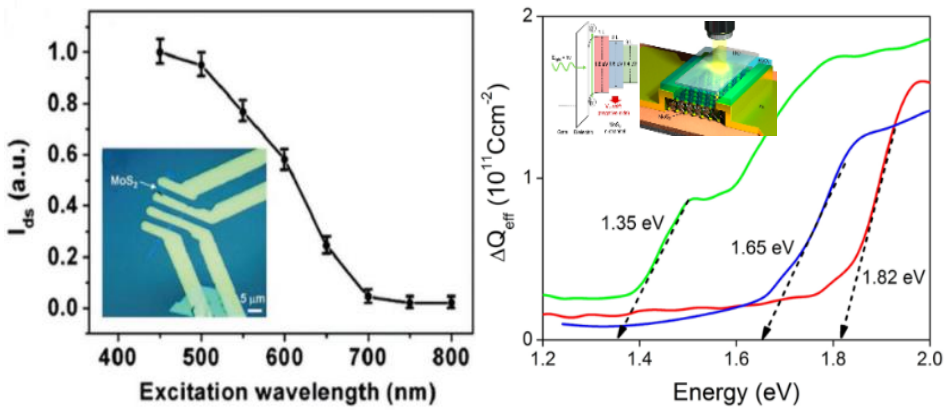
1.5 Current Status in 2D Semiconductor Photoelectric Devices

Today, 2D semiconductor materials can be not only applied on Nanoelectric device but also used in photoelectric devices. Because of the special structure, 2D semiconductor plays an important role in photoelectric devices such photoreactors, electrical imaging devices and solar cells. To be specific, there are 3 main reasons that make the 2D semiconductor material important: 1. 2D semiconductor material has a strong absorbing ability for light because of its

binding forces in vertical quantum scales. 2. 2D semiconductor such as MoS_2 has a symmetry structure in quantum level and the band gap will change while the stickiness varying. This will case the 2D material has a large wavelength response rang. For example, the silicon photoelectric device has a band gap as 1.12eV, however MoS_2 has a band gap from 1.2eV-1.9eV. 3. Monolayer 2D material has a direct band gap which is different to the traditional semiconductor materials. So, during the photon interaction process, the free carriers will be directly created, these devices will have a great progress in shorting response time. The advantages of 2D semiconductor material can highly improve the application area in civil uses and military uses.

1.6 Current MoS_2 Photoelectric Device Research Status

Since 2011 the research group from Nanyang Technological University (NTU) first tested the monolayer MoS_2 photoelectric device, people began to focus on this new material's study. In the research report, the response wave band was ~670 nm, the response rate was ~7.5mA/W and the response time was ~50ms (Figure 1.6.1a) [18]. Compare to the graphene devices (response rate~6.1mA/W), MoS_2 shows a great potential in photoelectric device applications. In 2012, Hee's group from Yonsei University tested the thickness varying MoS_2 photoelectric device. The result shows that with the increasing thickness varying the response band of MoS_2 can be extend to near-infrared range (Figure 1.6.1b) [19].



a. Single-layer MoS_2 photoelectric device.

b. Thickness effects of MoS_2 photoelectric devices.

Figure 1.6. 1 (a) The single-layer MoS_2 devices' drain current changes by different incident laser wavelength. (b) The thickness effects of MoS_2 energy gap. With the layers increasing, the energy gap inside MoS_2 becomes large.

1.7 Research Idea and Plan

By searching the current 2D material photoelectric device reports, there is an obvious point which will affect the performance. The energy band structure will change the electricity ability and photoelectricity ability. Therefore, combine the new fabrication method and device structure are the most efficient way to improve the device performances. In this report, the core idea is to modify the energy band level of 2D materials by using different device structures. Also, the improved devices should be able to adapt the near-infrared wave band.

Chapter 2: Photoelectric Device Theory and Manufacture Process

2.1 Photoelectric Device Theory

There are 3 steps between photons and semiconductor material during the photoelectric response. First photon absorption process, carrier transportation and carrier recombination or recapture process. Because of the different response theories, there are 2 groups in photoelectric devices: photodetector and heat detector. This paper will focus on the main theories in photodetector applications [20]. To improve the performance of photodetector devices 2 factors should be considered: photoconductive effect and photovoltaic effect.

2.1.1 Photoconductive Effect

Photoconductive effect means by having enough photons on the semiconductor surfaces, inside the material electrons and holes will be created. Semiconductors can use the free carriers to transport these 2 elements to improve the electric conductivity. In general, to achieve the separation between elections and holes, people usually use typical semiconductor material as channel and ohmic contact as source and drain. Therefore, photo-induced carrier will easily find the electrons and holes by using applied bias. Increasing the bias, the device will have a large benefit in electrons-holes separation and transportation to obtain a large light current. the equation for photoconductive gain factor is [21]:

$$G = \frac{\tau_{\text{lifetime}}}{\tau_{\text{transit}}}$$

τ_{lifetime}—— hole life time

$\tau_{transit}$—— electron transportation time

From the equation, to gain high photoconductive gain factor, it needs to reduce the electron transportation time and increase the hole life time. However, the response time of photoconductive effect is also related to the hole life time. So, over increase the G can also slow down the response time. In the real application, people need to balance the weight between gain factor and response time. Another equation is the photocurrent calculation. Under the photoconductive effect, the increased conductive rate of free carriers will increase the photocurrent [22].

$$I_{PC} = \left(\frac{W}{L}\right) V_D \Delta\sigma$$

W——device channel width

L——device channel length

V_D——Drain voltage

$\Delta\sigma$——Difference of conductive rate

2.1.2 Photovoltaic Effect

Photovoltaic effect is the creation of voltage and electric current in a material upon exposure to light and is a physical and chemical phenomenon. It usually uses the inside electrical field to

separate the electrons and holes. The photovoltaic effect is related to the photoelectric effect. In this case, light is absorbed, causing excitation of an electron or other charge carrier to a higher energy state. Under the light inject condition, the device will have 2 different operation modes. For bias ~0V, device works as photovoltaic effect. For reverse bias, the device will have photoconductive effect. The equation of photocurrent under photovoltaic effect is [22]:

$$I_{PV} = I_D\left(V_G - V_T + \Delta V_T\right) - I_D\left(V_G - V_T\right)$$

$$I_{PV} \approx g_m \Delta V_T$$

$$g_m = dI_D / dV_G$$

I_D——Source current

V_G——Gate voltage

V_T——Gate threshold voltage

ΔV_T——Gate threshold voltage offset

g_m——Device transconductance

2.1.3 Photoelectric Device Evaluation Criterion

Because the diversity of photoelectric device fabrications, there are lots of different methods and semiconductor material selections. Therefore, due to the different function of photoelectric devices, the requirement will change correspondingly. To compare the different photoelectric device, a stander and parameter need to be unified including the responsivity, internal quantum efficiency, external quantum efficiency and rise/fall time. The responsivity represents the rate

of output photocurrent or photovoltage to the incident power. In another word, when the input wavelength is fixed, under the unit incident power, the output photocurrent and voltage increase the responsivity will be larger. The responsivity R can be expressed by the following equation [21].

$$R = \frac{I_{ph} or V_{ph}}{P_{ab}}$$

I_{ph}——photocurrent

V_{ph}——photovoltage

P_{ab}——incident power

The external quantum efficiency means the rate between the electrons and holes (creating the photocurrent) and the number of injected photons.

The equation of EQE is showing below [21]

$$EQE = \frac{I_{ph} / q}{P_{in} / h\nu} = R\frac{hc}{q\lambda}$$

h——Kepler constant

v——light frequency

c——light speed

λ——wavelength

Through the equation, to obtain a high EQE rate, semiconductor materials need to have a high absorbance and the recombination rate of free carriers need to be reduce to the minimum.

The internal quantum efficiency is like the external quantum efficiency. It means the ratio between the electrons/holes and the absorbed photons. The absorbed photons can be attributed the refraction and reflection [21].

$$IQE = \frac{I_{ph} / q}{P_{ab} / h\nu}$$

Another important parameter to evaluate the photoelectric devices is the rise/fall time. This will directly represent the sensitivity to the inject light.

Chapter 3. 2D Semiconductor Photoelectric Device Fabrication

To achieve the high-quality photoelectric device, high efficiency, reliability and advanced micro-fabrication technic are the most important steps. In this chapter, it will focus on 3 main process in device fabrication: 2D material preparing (traditional mechanical exfoliation and monolayer material transfer). Second, 2D material device micro-fabrication (device structure design and electrode design). Third, after-treatment for fabricated device (anneal and storage).

3.1 2D Semiconductor Material Mechanical Exfoliation

In the 2D material preparing stage, because the device performance depends on the material surface quality, so the method to obtain the monolayer 2D material is very important.

In this paper, the traditional mechanical exfoliation with heat supported technic was elected to obtain the monolayer MoS_2 semiconductor material.

The detailed steps are shown below:

(1) Tape preparation: Using 3M Scotch tape cut into 10cm length, 2 cm width (Figure 3.1.1a).

(2) 2D material particle transfer: Using tweezer to collect the large 2D material chunk and put it to the center of the prepared tape (Figure 3.1.1b).

(3) Semiconductor exfoliation: Using hands to fold the tape 2-3 times and make sure 2/3 of the tape surface is full of 2D semiconductor materials (Figure 3.1.1c).

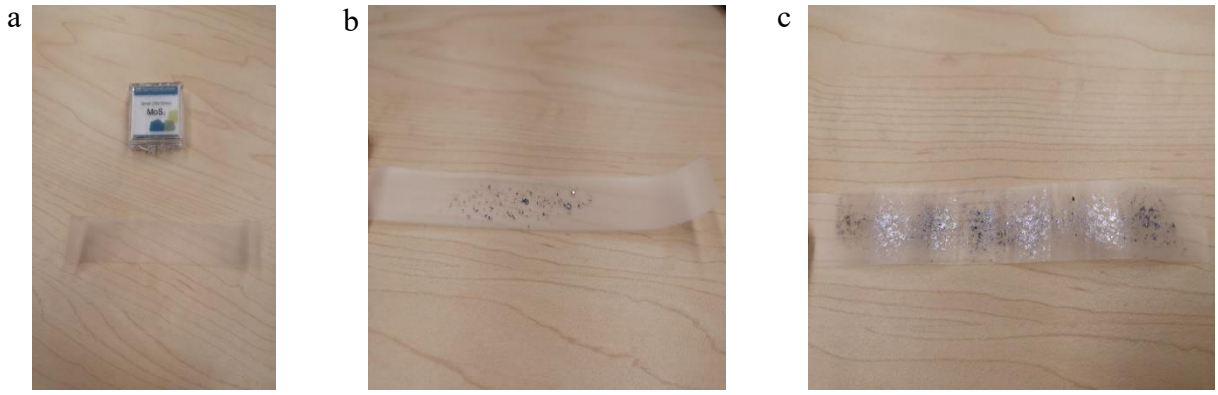


Figure 3.1. 1 The first 3 steps in single-layer MoS_2 sample preparation. (a) 3M tape was selected as primary traditional mechanical exfoliation tools. (b) Transfer the MoS_2 large particles on the tape. (c) Folded the tape to break the internal bonds inside the MoS_2 to obtain the single-layer MoS_2 samples.

(4) Flexible substrate preparation: flexible substrate will provide a reliable transfer condition to the later works if the VDW force between the semiconductor material and substrate is greater than semiconductor material and the device substrate. In this research experiment, Polydimethylsiloxane (PDMS) was selected as flexible substrate. PDMS is produced by SYLGARD184 silicone rubber in proportion 10:1 on an empty glass ware (Figure 3.1.2a). To achieve uniform mixing, using stirrer to mix for 3 mins. Drip the mixed solution to the microslide and standing 20 mins until the surface of the PDMS is smooth (Figure 3.1.2b).

(5) Baking: Leave the prepared microslide on the heater (100 ℃) for 10 mins until the PDMS solution is solidified (Figure 3.1.2c).

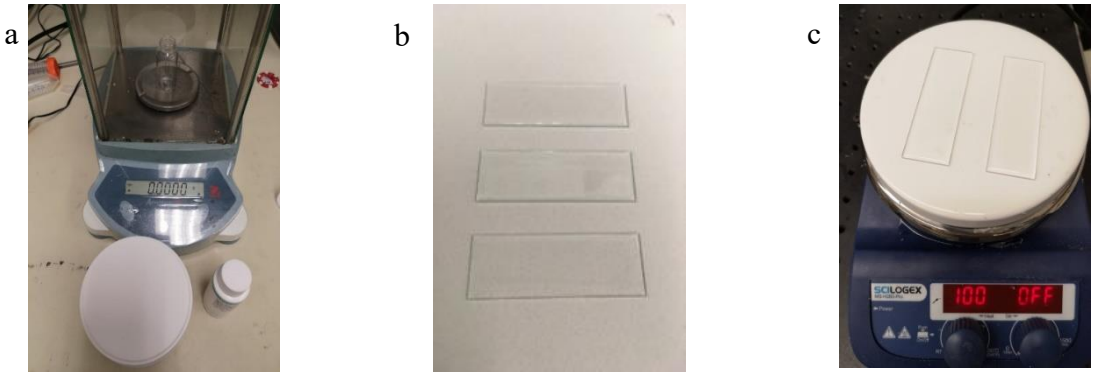


Figure 3.1. 2 (a) Prepared the Polydimethylsiloxane (PDMS) solution by using the electronic scales. (b) Applied the PDMS on the blank microslides. (c) Baked the PDMS on the hot plate under 100℃ conditions.

(6) 2D material transfer: Apply the sampled tape on the surface of the microslide (Figure 3.1.3a). Using swab press the contact surface until eject the air between 2 layers. Quickly pull away the tape from the microslide. The 2D semiconductor material will be remained on the substrate. Using blade to cut the PDMS into small grids. It will be easy to detect the position of MoS_2 samples under the microscope (Figure 3.1.3b).

(7) Microscope sample selection: Using the microscope to select the ideal monolayer 2D material (Figure 3.1.3c). After scanning, the ideal monolayer MoS_2 will appear special color because of the thickness. The monolayer MoS_2 is more likely in light grey color. Screenshot the shape of MoS_2 and record the position on the notebook for photoelectric device transfer (Figure 3.1.3d).

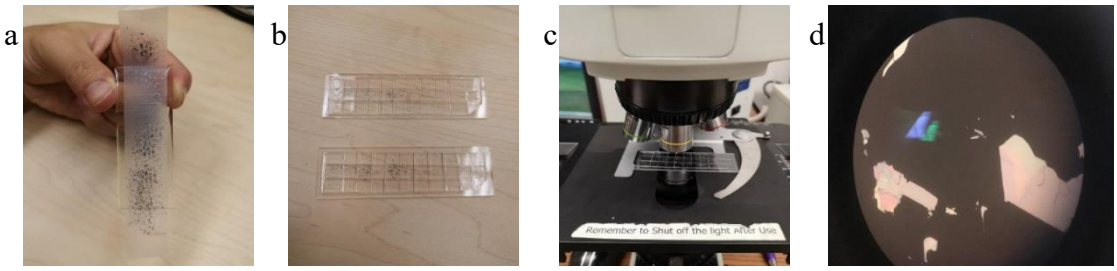


Figure 3.1. 3 (a) Applied the folded 3M tape on the PDMS and teared off quickly. The single-layer MoS_2 will remain on the PDMS microslides. (b) Using blade to cut the PDMS into small grids. (c) Using microscope to observe the thickness and size of MoS_2 nanoflakes. (d) Microscope image of single-layer MoS_2 nanoflakes.

3.2 2D Semiconductor Material All Dry Transfer Method

After the mechanical exfoliation, the selected monolayer sample needs to transfer to the silicon substrate for micro-fabrication. During this process, the selected sample will be transfer to the specific location on the base substrate under the digital microscope monitor (Figure 3.2.1a).

(1) Silicon-based substrate cleanse: To avoid the impurity particles' effect, silicon substrate needs to be cleaned by the transfer process proceed. The 0.5 x 0.5 inches substrate will be dipped into the acetone solution for 10 mins to remove the surface oil and grease. After the bath, using deionized water clean the surface and dry the substrate by nitrogen gas gun. To remove the organic matter on the substrate surface, oxygen plasma is applied. The substrates will be placed under 300W, pressure 70 mtorr and oxygen speed rate 60 sccm environment for 3 mins.

(2) Silicon-base and PDMS sample fixation: Put the selected sample microslide on the 3D movable-operating stage and applied the PDMS face down to the silicon substrate (Figure 3.2.1b). Keep the silicon-base substrate on the bottom of the microscope and parallel with the microslide. Increase the magnification times of the microscope until the shape of selected sample appears (Figure 3.2.1c). Move the sample position to the ideal area on the silicon-based substrate. Focused on the substrate and slow move down the microslide in z-axis approximate speed 1mm/s.

(3) Sample fixation: When the sampled microslide total contact to the silicon-based substrate, a yellow shadow will appear on the microscope screen (Figure 3.2.1d). Leave the substrate and sampled microslide for 30s and slowly rise the microslide. The selected 2D monolayer material will be remained on the substrate (Figure 3.2.1e).

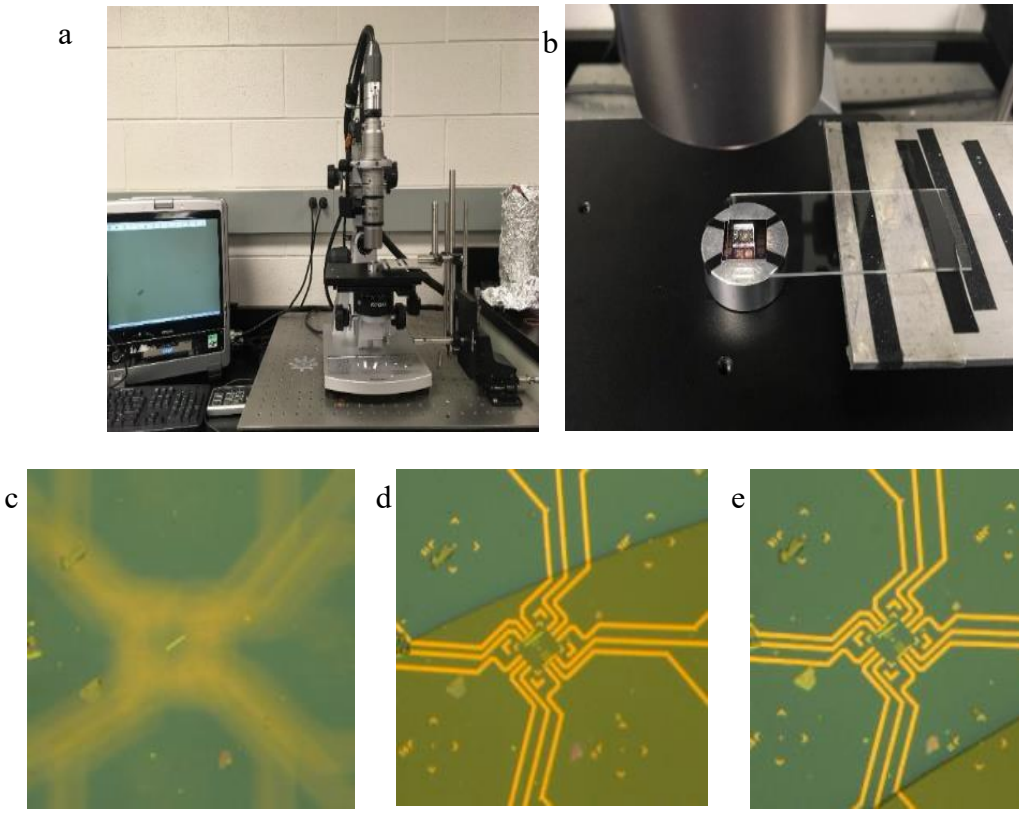


Figure 3.2. 1 (a) Digital microscope for all dry transfer process. (b) Movable-operating stage. (c) Focusing the digital microscope on the PDMS level and find the selected MoS_2 nanoflake. (d) The PDMS is fully contacted with silicon substrate when the yellow shadow appears. (e) By slowly rising the PDMS, the selected MoS_2 nanoflake will remain on the silicon substrate.

3.3 2D Semiconductor Material Photoelectric Device Fabrication

After obtaining the perfect monolayer 2D semiconductor material, the photoelectric device design can be divided into 2 steps: outside circuit design and the inside electrodes design. For the outside circuit design, it is proceeded on millimeter scale. The key for outside circuit design is quantity production. In this paper, research group was using the UV micro-fabrication technic to unify the stander outside circuit. By using the AuotCAD, the UV mask was designed and fabricated (Figure 3.3.1a). Inside the mask, there are 45 individual micro-circuits in size of 0.5 x 0.5 inches. For each microcircuit, there are 10 square electrodes pin in size of 2mm x 2mm

(Figure 3.3.1b). These electrodes are used to connect the photoelectric device to the semiconductor tester. At each micro-circuit center, there is a 100μm x 100μm space for 2D material transfer (Figure 3.3.1c).

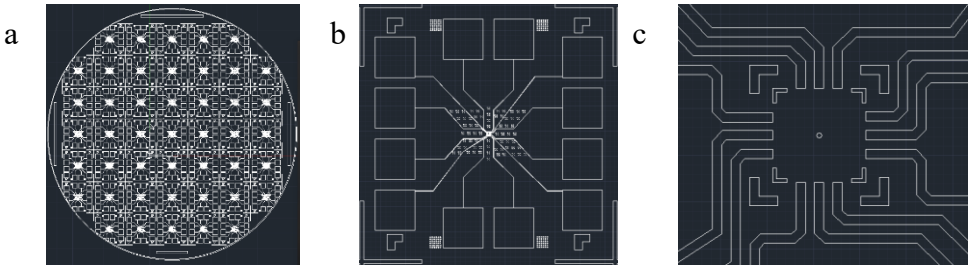


Figure 3.3. 1 (a). Using AutoCAD to design and fabricate the UV Lithography. Inside the mask, there are 45 individual micro-circuits. (b) The size of one micro-circuit is 0.5 x 0.5 inches. Each individual micro-circuit has 10 square electrodes in size of 2 mm x 2 mm. (c) The open space at the center of the individual micro-circuit is 100 x 100 μm.

3.3.1 External Circuit Micro-fabrication

(1) Clean silicon wafer: First put the 5 inches silicon wafer into the acetone solution for 10 min and removes the impurities. Using the deionized water to clean the remaining acetone and dry the surface by the nitrogen gas gun. To remove the organic matter on the substrate surface, oxygen plasma is applied. The substrates will be placed under 300W, pressure 70 mtorr and oxygen speed rate 60 sccm environment for 3 mins.

(2) Photoresist process: Applied the 5 inches silicon wafer at the center of the spinner, set the speed as 4000 rad/min and time 45 s. Applied the AZ5215E photoresist on the surface of the wafer until it spread equally.

(3) Pre-bake process: Put the wafer into the bake oven, set the temperature as 90 ℃ and time for 1 min. in this pre-bake process, it will remove the moisture from the photoresist to avoid the negative effects under the UV exposing.

(4) Set the baked wafer on the UV exposing device and put the mask on the top of the wafer. Using UV to expose the photoresist surface for 2 s.

(5) Second bake: After the first time exposing, re-bake the wafer in 115 ℃ for 45 s.

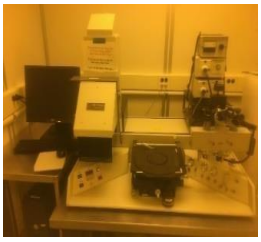
(6) Second UV exposing: Remove the mask from the UV exposing device and expose the wafer again for 12 s. In this step the remaining unexposed photoresist will be completely reaction with UV.

(7) Wafer development: Put the exposed wafer into the MIF300 solution to develop for 90 s. Using deionized water to remove unreacted solution and dry the wafer surface.

(8) Metal electrodes evaporation: Using the high vacuum evaporator to design the outside circuit on the developed silicon wafer. To improve the adhesive force between the Au and silicon, first applied the Ti as bonding layer. To evaporate Ti, the ideal voltage is 3 V, evaporation rate 1.2 nm/s and thickness 2 nm. To evaporate Au, the ideal voltage is 2.1 V, evaporation rate 1.2nm/s and thickness 45nm.

(9) Lift off: Put silicon wafer into the acetone solution for 30 mins with a heating support (75 ℃).

In Figure 3.3.2, all the external circuit process required devices are shown.

a  b  c 

d  e 

Figure 3.3. 2 (a) A plasmonic cleaning device is used to clean the silicon wafer before the external circuit fabrication. (b) A photoresist baking oven is used to bake the photoresist. (c) An UV Lithography device is used to fabricate the blank silicon wafer into the 45 individual external circuit chips. (d) Photoresist spinner. (e) A metal evaporator is used to steam the metal material on the surface of the silicon wafer.

3.3.2 Internal Circuit Micro-fabrication

After transferred the 2D semiconductor material MoS_2 onto the silicon-based substrate, the last micro-fabrication step is the inside circuit design.

In this process, the electron beam lithography (EBL) technic is applied. The difference between the UV lithography and the electron beam lithography is that EBL (Figure 3.3.3a) is using the electrons bombardment on the EBL photoresist, after that using the development solution the develop the design pattern.

(1) The first step in EBL is the same process as UV lithography.

(2) Apply the EBL photoresist MMA EL9 to the substrate under spinner speed as 4000rad/ min for 50s.

(3) Baking the prepared substrate in oven under180 ℃ for 5 mins

(4) Re-spinning the substrate with PMMA C2 photoresist for another 50s in 4000rad/ min speed. The reason to apply 2 layers photoresist is the during the EBL process, high speed electrons will create an under-cut effect on the substrate which will make the lift off process more efficient.

(5) Re-baking the substrate under 180 ℃ for 10 mins.

(6) Electrodes design: By using the NPGS system, the electrodes will be draw on the substrates (Figure 3.3.3b). The advantage of EBL design is that people can design different micro-circuit for each substrate, there is no mask needed during the process.

(7) EBL development: After the EBL lithography, put the substrates into the MIBK : IPA = 1:3 solution for 1min 30s. Using deionized water to remove unreacted solution and dry the wafer surface.

(8) Lift off: Put silicon wafer into the acetone solution for 90 mins with a heating support (75 ℃).

a b

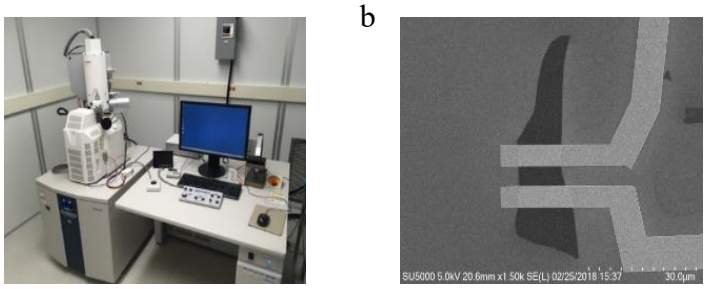
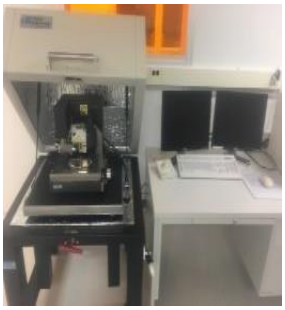


Figure 3.3. 3 The electron beam lithography (EBL) is used as the primary tools in internal circuit design and fabrication (a) The scanning electron microscope (SEM) can be used as observation tools during the EBL process. (b) Under the SEM observation, the internal circuit was designed to have a 5 μm gap between two electrodes. The MoS_2 was the transistor channel inside the device.

3.3.3 2D Semiconductor Photoelectric Device Electrical Characterization

For 2D semiconductor photoelectric device electrical characterization, there are a lot of equipment used to test the device performances such as Atomic Force Microscope (AFM), Raman Spectroscopy and Semiconductor Tester 4156B (Figure 3.3.4 a-c). The semiconductor Tester can test multiple tasks such as photoelectric device current/voltage curves, capacity test and transient current voltage curves. The range of testing current is ~0.1 fA-1A, voltage ~0.5 μV-200V. During the test, 3 ports SMU1-SMU3 are selected. SMU1 is the source, SMU2 is drain and SMU3 is gate. In general, the drain voltage range is ~ -5V to 5V, source will connect to the ground and gate voltage will be ~ -100V to 100V scanning.

a 
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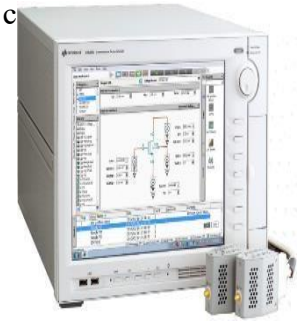
c 

Figure 3.3. 4 (a) An Atomic Force Microscope (AFM) is used to measure the sample thickness. (b) A Raman Spectroscopy is used to detect the molecular vibration mode inside the 2D materials. Also, there are 3 built in lasers (532nm, 785nm and 830nm) that can be used to test the device performance. (c) A semiconductor tester (Agilent 4156B) is used to find the performance of the photoelectric devices.

Chapter 4. Enhanced MoS_2 Photoelectric Device by Using Nano Antenna Structure

In these years, the development of nano-technology is growing fast. nano-optical antennas is applied for the most industries as a new energy absorption method.

Like the macro antenna structure, the major purpose of mano-optical antennas structure is to transfer the free radiant energy into regionalized energy. Because of the scale of nano-optical antennas in inside the nano level, therefore it has a great advantage in light focusing property. This special structure can break the limit for traditional optical diffraction, and easily control the free electrical field within the nano scale level [23]. Although, nano-optical antennas has already been developed in microfabrication, most of them are used within the visible light range. In this paper, the research group used MoS_2 as carrier and nano-optical antennas as enhanced method to improve the responsivity in near-infrared range.

4.1 Nano-optical Antennas Design

For nano-optical antennas structure, different shape and size of antennas can not only control the resonant frequency but also change the magnetic field intensity in nano-photoelectric device. Therefore, the reasonable structure design will achieve multiple bands corresponding to enhance light trapping ability. In this paper, the designed structure is to trap the light within the near-

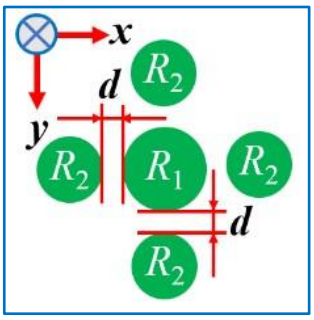


Figure 4.1. 1 Pentamer antenna structure has 4 metal disks (radius R_2 50 nm ） around the center metal disk (radius R_1 75 nm). Adjusting the radius (R_1 or R_2) and gaps (d) can trap different wavelength light.

infrared range, it will enhance the interaction between injecting light and the semiconductor material. During the experiment, the research group design the pentamer nano-optical antennas structure (Figure 4.1.1). From the figure, the pentamer shape is using 4 Nano disks with diameter R_2 surround the center Nano-disk with diameter R_1. The distance between the outside disks and center disk is *d*. By changing the diameter of disk and value *d*, the photoelectric device can response different optical wavelength.

4.2 Nano-optical Antennas Optical Field Distribution

To verify light trapping ability of pentamer shape structure, the research group used Three-Dimensional Finite Difference Time Domain (3D FDTD) to simulate the results. The simulation model for pentamer shape structure is shown in figure 4.2. In the simulation, assuming the injected laser are located on the semiconductor material equally. The laser polarization direction is alone the x-axis and the direction of the wave vector is alone z-axis, wavelength 830nm, wave function $E=E_x sin(2\pi ft)=sin(2\pi ft)$. For the antennas structure, outside disks' diameter is 100nm and center disk is 150nm, distance *d* ~15nm. The antennas are directly connected to the silicon dioxide substrate (200nm thickness). The bottom of Nano-disk sets to z=0nm. The material for

Nano-antennas is Au. To calculate the enhanced factor η using equation $\eta=E_{max}/E_{input}$ (E_{input} is injected laser electric field intensity) to find the best solution.

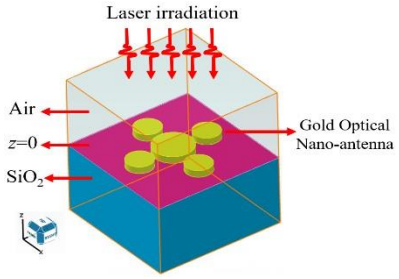


Figure 4.2. 1 Schematic illustration of simulation model of pentamers optical-antennas.

In Figure 4.3.1, the research group calculated the electric field intensity at y = 0nm and y = 110nm point. From the result, it shows that at y=100nm the largest enhanced factor located at the left and right edges, η~4.01. The electric field intensity begins to decrease at the edges of 50nm. For y=0nm, there are 2 different enhanced electric field appeared. The first point is the gap between 2 outside disks, η~5.72. the second location is the gap between the outside disk and the center disk. As a result, the electric field for second location can cover the whole gap (15nm), and the enhanced factor η are all above 20. The largest factor appears at the edge of disk, η~25.13.

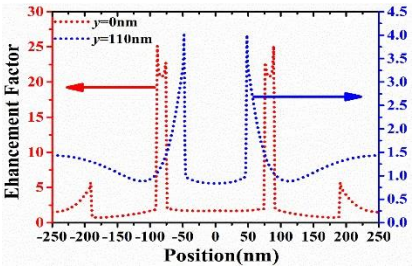


Figure 4.3. 1 At position y=100 nm and y=0 nm, the electric field has been enhanced.

To prove the distance d=15nm is the best design structure for wavelength 830nm, the group simulated the other laser with different wavelength (400nm, 600nm, 830nm,110nm) (Figure 4.4.1). For the visible light wavelength, all the enhanced factors are below 5, near-infrared SWL will achieve ~10, especially for 850nm η~29 (Figure 4.5.1). Therefore, Nano optical antennas structure can efficiently trap the light in near-infrared range.

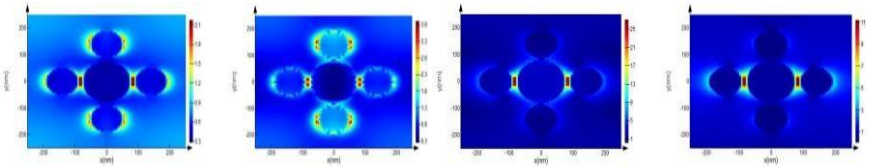


Figure 4.4. 1 The electric field distribution under different wavelength incident lasers. From the left to the right, the incident lasers' wavelength are 400 nm, 600 nm, 830 nm and 1100 nm.

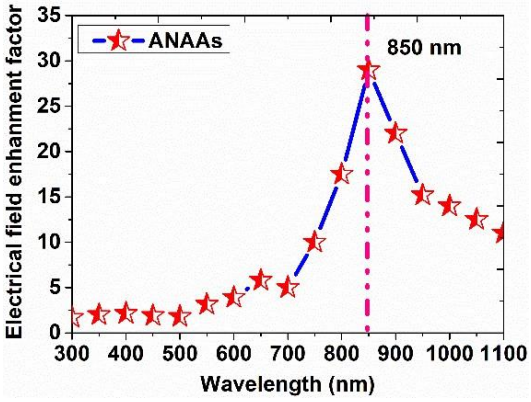


Figure 4.5. 1 Effect of the wave length λ on electric field enhancement factor of optical antenna.

4.3 Nano-optical Antennas Micro-fabrication

By using the FDTD, the result shows that the pentamer structure is the most efficient method to trap the near-infrared wavelength light. In this section, it will focus on the micro-fabrication process to create the antennas structure.

During the EBL micro-fabrication, first step is to adjust the electrical beam to the best state. The best state means the beam shape reaches to the smallest size. To estimate whether the beam is the smallest size, zoom in and focus the microscope until the SEM image can clearly format Nano size particles. To obtain the 15nm gap, the EBL experiment needs to test several times and optimize the beam parameters. Thus, to reduce the ejection damage of electrons to the photoresist.

The detail micro-fabrication process is:

(1) To avoid the defect during the photoresist development, the antenna fabrication uses single layer photoresist PMMA C2. Accelerate voltage 30kV, beam working distance 5mm,

magnification times 1200, center to center beam distance 2.54nm, step distance 2.54nm, beam current 68pA, EBL area 245nC/cm^2.

(2) After loading the silicon-base substrates into the SEM, move the beam gun to the desired design location. Focus the microscope until the Nano-size particles appear. Exposing the photoresist area follows the previous EBL fabrication process in the last chapter.

(3) Develop the substrate by using the MIBK: IPA=1:3 solution. To avoid the defect due to the small 15nm gaps, keep the substrate stable in the solution.

(4) Evaporate 30nm Au thin film.

(5) Lift off: Apply the substrate into acetone solution under 75 ℃ oven heating condition for 2 hours.

Figure 4.6.1 shows the SEM image of Nano-optical antenna structure. From the left figure, it shows that the single antennas structure unit has a good condition after micro-fabrication (Nano-disks appear regular circle shape and Nano-gap approach 15nm). The right figure shows the antenna array structure, the density approaches ~5 units/ μm^2, array length 100nm. From the figure, it shows all Nano-optical antenna structures have perfect shapes and qualities.

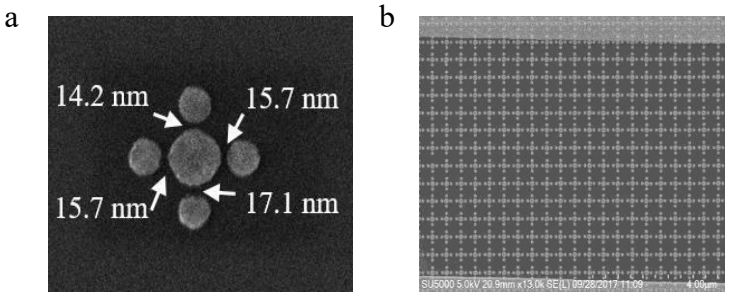


Figure 4.6. 1 The image obtained by using SEM. (a) The single pentamer optical antenna array. The gaps between each disk are 15 nm. (b) A large area with pentamer optical antenna arrays (300 pentamer groups).

4.4 Nano-optical Antennas Enhance MoS_2 Photoelectric Device

After the research in Nano-optical antennas structure study, this section will focus on the antenna applications in 2D semiconductor material photoelectric device study. The experiment selected MoS_2 as semiconductor base, the reasons are listed below:

(1) The energy band gap of MoS_2 is located at ~1.2eV-1.8eV, therefore the sensitive wavelength band is the visible light range [8]. The band gap directly limits the application

for MoS_2 in near-infrared wavelength range. If using the Nano-optical antennas structure can improve the sensitive of MoS_2 to a large range, this will be helpful for future photoelectric device applications.

(2) The previous experiment has already proved that under the light condition, the photons will motivate the thermions from the metal Nano-structure into the MoS_2 Schottky barrier [24]. The injected thermions can be treated as a new method to improve the density of free carriers.

(3) MoS_2 has a great stability during the room temperature compare to the black graphene.

4.5 Testing the Enhanced MoS_2 Photoelectric Device with Antenna Structure

From Figure 4.7.1, it shows a typical MoS_2 photoelectric device. To provide a reliable connection between the electrodes and the MoS_2, all electrodes were designed in width ~2 μm. Figure 4.7.1a is the device image under the electric-microscope obversion. From the figure, it shows that the channel length is 13.53 μm x 6.10 μm. It has enough space for antenna array fabrication. Figure 4.7.1b is the image under SEM obversion. From the figure, it shows the antenna array is located at the drain side. This means that the EBL technic can not only provide a Nano-scale fabrication skill but also make sure the fabrication precisely enough. Figure 4.7.1c is the device image under AFM obversion. From the figure, it shows the thickness of MoS_2

Figure 4.7. 1 The characteristic of one of representative few -layer MoS_2 photodetector with optical antenna arrays. (a) The device was observed under the electron microscope. The length of the select MoS_2 is 13.53 μm. (b) By using the SEM, the antenna arrays are placed close to the drain side. (c) By using the AFM, the result shows that the thickness of selected MoS_2 is 2.56 nm.

~2.56 nm. Base on the known knowledge, single layer MoS_2 thickness is ~0.618 nm, so the tested sample is about 5~6 layers.

To verify the enhanced effect for photoelectric device by using Nano-optical antenna structure, the contrast test for MoS_2 device with or without antenna array structure under near-infrared wavelength environment is needed. In Figure 4.8.1a, it shows the testing environment of MoS_2 device with antenna array structure under the near-infrared 830 nm incident laser. In Figure 4.8.1b, it shows the comparison (with or without antenna array) output current and voltage result for MoS_2 device under different laser power situations.

From the figure, the laser power was increased from 0mW to 64mW, the output current for non-antenna structure MoS_2 device was ~0.03 μA to ~0.05 μA. However, the output current for antenna structure MoS_2 device was ~0.04 μA to 0.20 μA. Therefore, the result shows that under laser 830 nm lighting condition. The Nano-optical antenna array structure enhanced the current for photoelectric devices.

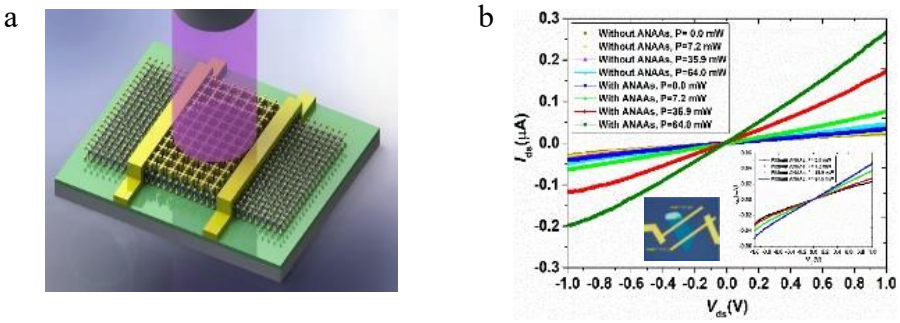


Figure 4.8. 1 The performance comparison of MoS_2 photodetectors with or without optical antennas. (a) The device testing schematic. (b) With the incident laser power increases, the output drain current range is 0.03 μA to 0.05 without optical antenna and 0.04 μA to 0.20 μA with optical antenna.

For further experiment, the research group need to compare the effect of Nano-optical antenna structure for MoS_2 device photocurrent. In general, the optical response mechanisms for MoS_2 device are conductive effect and photovoltaic effect [22]. In figure 4.9.1a, it shows the result of MoS_2 device under photovoltaic effect. The drain voltage V_{ds} = 0V, gate voltage V_{gs} = 0V. For non-antenna structure MoS_2 device, when the incident laser power P_{in}=7.2mW increased to

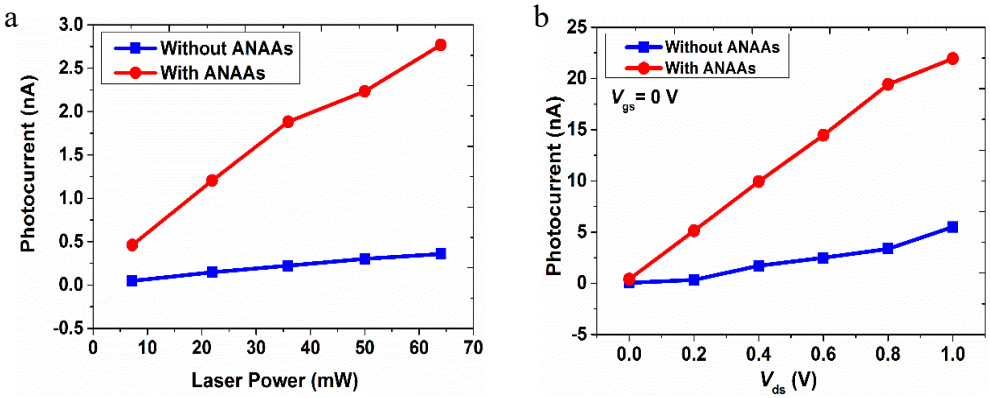


Figure 4.9. 1 The photocurrent comparison of MoS_2 photodetectors with or without optical antennas under different mechanisms. (a) The photocurrents under photovoltaic condition. (b) The photocurrent under photoconductive condition.

P_{in}=64.0mW, the range of output photocurrent is ~0.1-0.25nA. However, the antenna structure's output photocurrent range is 0.5-2.8nA. Especially the laser power is 64mW, the output photocurrent is increased 11.4 times. In figure 4.9.1b, it shows the result of MoS_2 device under the conductive effect condition. When the V_{ds} = 0V increased to 1V, the photocurrent for non-antenna structure device is ~0.15-5nA. And the antenna structure device can have a photocurrent ~5-17.5nA range. To sum up in conclusion, the pentamer Nano-optical antenna structure will improve the performance of photoelectric device obviously within the near-infrared wavelength range.

4.6 Position Effects to the Nano-optical Antenna structure

After verifying that pentamer Nano-optical antenna structure will improve the performance of photoelectric device in the near-infrared wavelength range, the research group suggest a new idea about the position affects to the antenna structure.

To prove this idea, there are 3 experiments were tested base on the antenna location dependence. First, the antenna array was applied between the source and drain. Second, the antenna array was fabricated close to the drain side and inside the channel range. Third, the antenna array was applied outside the channel but close to the drain side. In the Figure 4.10.1 (a-c) it shows the different antenna array positions on the MoS_2 photoelectric devices. To test the position affects, all 3 experiments were tested under same antenna coving rating condition ~ 40%. The coving rate is the ratio between the antenna array area and the channel area.

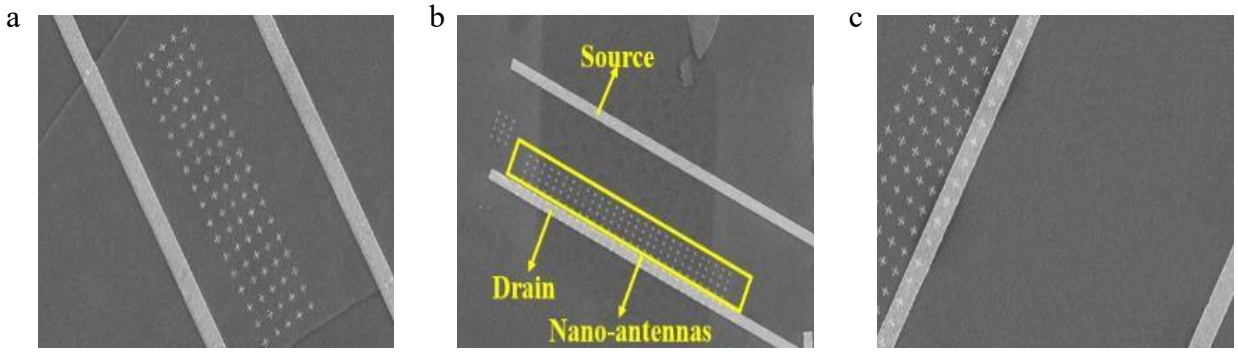


Figure 4.10. 1 The performance comparison of MoS_2 photodetectors with different optical antenna positions. (a) Antenna arrays placed at the channel center. (b) Antenna arrays placed close to the drain and inside the channel. (c) Antenna arrays placed close to the drain and outside the channel.

In Figure 4.11.1, it shows the output current and voltage under different laser power lighting. The result shows that when the antenna array structure located closer to the drain side, the output result for with/without antenna structure is significantly different. However, for the other antenna position, the compared results are not significant.

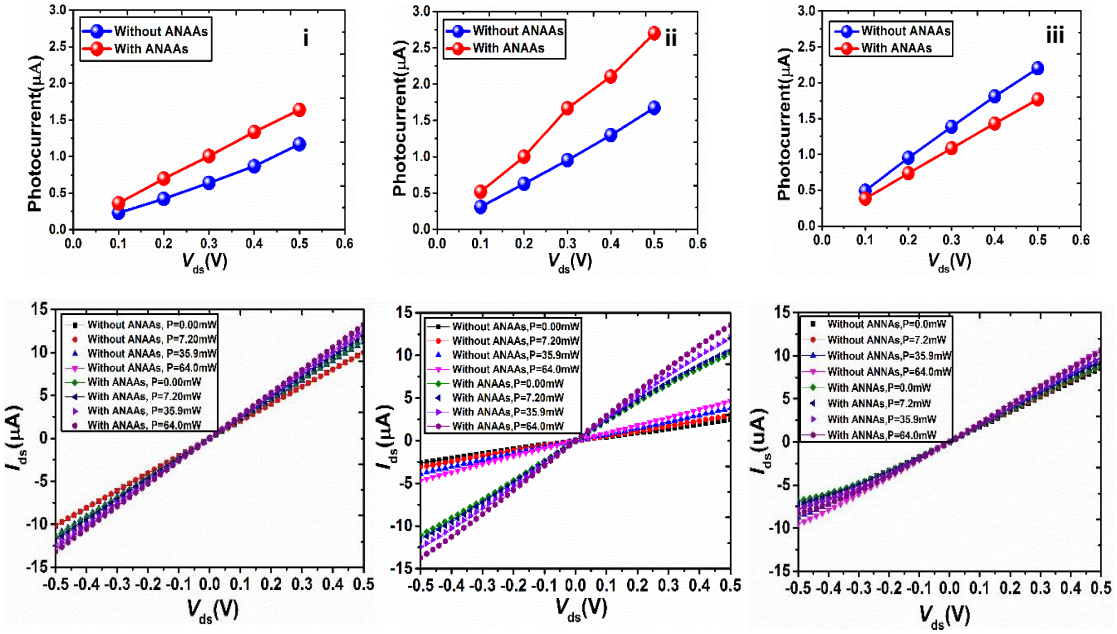


Figure 4.11. 1 The performance comparison of MoS_2 photodetectors with different optical antenna positions. The upper figures are the photocurrent comparison. The bottom figures are the drain current and bias voltage comparison.

Chapter 5 Structure Enhanced the MoS_2 Photoelectric Device

In semiconductor industries, changing the material structures to improve the devices' performance is the most common method [25]. However, the low strain rate of traditional semiconductor material plays an opposite effect to this application. In general, the limit tension of silicon-based semiconductor material is ~1.2% [25]. Recent years, with the rapid development of nanomaterials, 2D semiconductor materials have a great performance in mechanical deformation because of its unique bod characteristics. For example, the graphene can withstand elastic deformation about ~25% [26], and MoS_2 can bear elastic deformation ~11% [26]. This special characteristic will allow 2D semiconductor material have a bending and folding structures during the fabrications.

Thus, this chapter takes transition metal disulfide as the research object, a "sandwich" structure photoelectric device is proposed. This new fabrication structure will greatly enhance the performance of current Nano photoelectric device.

5.1 "Misaligned Sandwich" Structure MoS_2 Photoelectric Device Micro-fabrication

In Figure 5.1.1, it shows the schematic of "Misaligned Sandwich" structure fabrication. In Figure 5.2.1, it shows the fabrication process of "Misaligned Sandwich" structure under the electron microscope observation.

In general, the key fabrication steps can be summarized as the flowing points:

(1). Using traditional mechanical exfoliation method to prepare MoS_2 materials in thickness ~15nm-30nm. The multiple layers material is required because it take more degree of deformation.

(2). Preparing the silicon-based substrates. Using acetone and plasma cleaning obtain a clean surface.

(3). For the silicon substrates, using EBL and metal evaporating methods apply source electrodes in size of 2 μm width, 35 μm length and thickness 45 μm. In this experiment, the selected number of source electrodes are 4.

(4). Using dry 2D material transfer method, applied the selected multiple layers MoS_2 material on the prepared source electrodes. During the transfer process, because of the edges of PMDS completely contact with the electrodes, a high degree bending will occur.

(5). Using EBL and metal evaporating methods to complete the rest of circuit design. In this step, 5 new electrodes (thickness~100 μm) will be applied between the source electrodes. In the figure, it shows that after the fabrication, there are 8 repeated current channels and the gap between each channel is 1 μm. For each current channel we defined it as “single sandwich” structure because MoS_2 was mounted between the upper and lower electrodes (source and drain). Therefore, MoS_2 will have a large bending structure at the edge of drain side. At the source side, MoS_2 will still have a traditional Schottky contact.

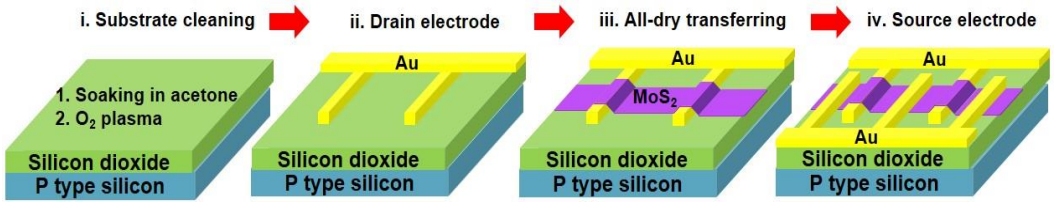


Figure 5.1. 1 Schematic illustration of fabrication procedure of a representative multilayered MoS_2 nano device with "Misaligned Sandwich" architecture.

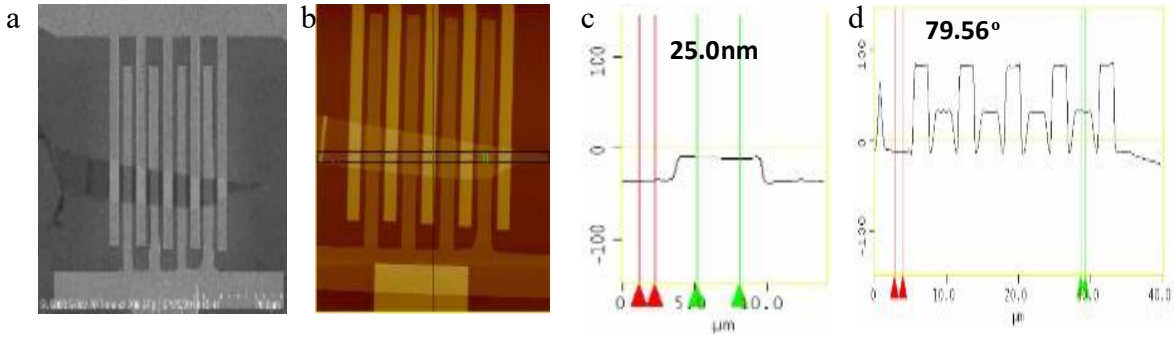


Figure 5.2. 1 Characterization of a representative multilayered MoS_2 nano device with "Misalinged Sandwich" architecture. (a) The device image under SEM observation. (b) The image under electron microscope, the width of MoS_2 is 5 μm. (c) By using the AFM, the MoS_2 nanoflake thickness is 25 nm. (d) By using the AFM, the bending angle of MoS_2 is 79.56°.

In Figure 5.3.1a, it is the AFM scanning image of fabricated device. From Figure 5.3.1b, the width of MoS_2 is 5 μm and it was mounted between the source and drain electrodes. From Figure 5.3.1c. the selected MoS_2 is 24.955 nm satisfy the requirement for bending structure. From Figure 5.3.1d, at the edge of MoS_2 a great bending degree was formed ~79.56°. Because of the bending degree, inside the atomic geometry a great structure changing is essential, this may cause a difference between the traditional MoS_2 properties and the modified one.

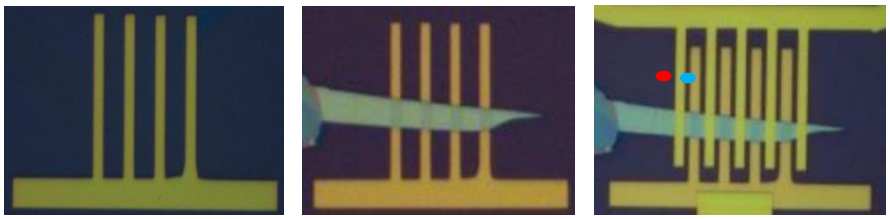


Figure 5.3. 1 Optical microscope images of fabrication procedure of a representative multilayer MoS_2 nano device with "Misaligned Sandwich" structure.

5.2 Energy Band Analysis of "Misaligned Sandwich" Structure MoS2 Photoelectric Device

The energy band structure is the key to determine material's electrical properties and current-illumination characteristic. This section will focus on the principle of band-gap modulation of the "Misaligned sandwich" structure device. The first important part of band-gap modulation is to determine the new Fermi level position. Kelvin probe force microcopy (KPFM) is the most common device to determine the Fermi level, it tests the voltage potential difference across the sample surface [27].

In this experiment, the research group used MFP-3D-AFM from Asylum Research Company to test the surface voltage potential. During the test, the probe will firstly stay in tapping mode to test the sample surface. Secondly the probe will rise 30nm and applied bias. The sample will be grounded to offset the electrostatic force. Therefore, the tested result is the voltage potential between the probe and the surface to reflect the material's work function difference. In this experiment, the voltage potential between the AFM probe and sample is called CPD and calculation equation is shown below:

$$CPD = \frac{\Phi_{\text{Tip}} - \Phi_{\text{Sample}}}{e}$$

Φ_{Tip}——probe work function

Φ_{sample}——sample work function

From the equation, when the KPFM probe work function is fixed, the sample work function will be inversely proportional to the CPD. Because of the Fermi level position is related to the material work function, so the new Fermi level can be calculated as a result.

5.2.1 Bending Effects to MoS_2 Fermi Level

To explore the bending effect of MoS_2 surface voltage potential, the research divided the sample surface into 6 different area to test the individual voltage potentials. In Figure 5.4.1, position 0 is the flat area on the MoS_2 bottom electrode, position 1 is the upper bending area, position 2 is the flat slope area, position 3 is the lower bending area, position 4 is the flat area and position 5 is the area that source electrode contact with MoS_2. The first tested group is 0 and 1, these positions are all located on the Au substrate. Groupe 3 and 4 are based on the silicon substrate.

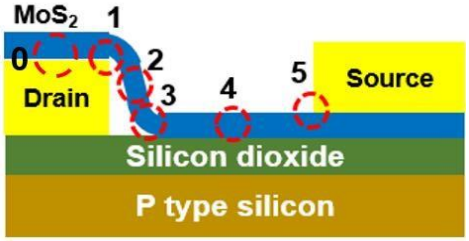


Figure 5.4. 1 The measurement results MoS_2 based field effect transistors with "Misaligned Sandwich" architecture under zero bias.

During the testing, the result shows that the voltage potential at position 0 is -20mV, however, at position 1 (bending area) the surface voltage potential decreased and approach -40mV. At position 4 (flat area), the voltage potential is -35mV and position 3(lower bending area) voltage potential drop to -45 mV. Therefore, the result shows that bending area will have an obvious voltage potential drop. Based on the CPD equation. The voltage difference between bending and flat area can be represented as:

$$\Delta CPD = CPD_{\text{bend}} - CPD_{\text{flat}} = \frac{\Phi_{\text{Tip}} - \Phi_{\text{bend}}}{e} - \frac{\Phi_{\text{Tip}} - \Phi_{\text{flat}}}{e} = \frac{\Phi_{\text{flat}} - \Phi_{\text{bend}}}{e}$$

CPD_{bent}——bending area surface voltage potential；

CPD_{flat}——flat area surface voltage potential;

Φ_{bent}——bending area work function；

Φ_{flat}——flat area work function;

From the equation: the MoS_2 work function for bending and flat area are the opposite changing with the surface voltage potential.

5.2.2 Bending Effect to MoS_2 Band-gap

After obtaining the Fermi level effect because of the bending structure, the research group focused on the band-gap changing result. According to the recent experiment report and simulation result, the mechanical bending will decrease the band-gap 100meV [28]. Also, to approve the report, the research group used Raman Spectrum Microscope found out that the bandgap at bending area is lower than the flat area (position 1and 3 E_{g1} are smaller than position 2 and 4 E_{g2}).

5.3 “Misaligned Sandwich” Structure MoS_2 Device Electrical Properties Test

Figure 5.5.1, it shows the “sandwich” structure MoS_2 field effect transistor electrical properties. In Figure 5.5.1 (left), it is field effect transistor the test diagram. MoS_2 device is under room temperature and no laser injection. The bottom electrode is selected as drain, bias voltage swipe from -1V to 1V. the upper electrodes are selected as source connected to the ground. Figure 5.5.1 (right) shows under different bias voltage condition, the generated current tendency changes (I_{ds}-V_{ds}). From the figure, the result shows that “sandwich” which will provide a great rectification characteristic. At the meantime, by changing the gate voltage, the electrical current will increase obviously. With the V_{gs} increases from 0 V to 20 V, MoS_2 devices field effect transistor current increased rapidly, when V_{ds}=1 V, the current increases from ~0.14 μA to ~47 μA. Under the negative bias condition, the devices are turned off completely. To prove the rectification characteristic can be repeatedly achieved, the research group tested the multiple samples by using the “sandwich” structure method. In figure 5.6.1, 4 different size MoS_2 devices were tested and all devices obtained large current at V_{ds}=1V V_{gs}=20V.

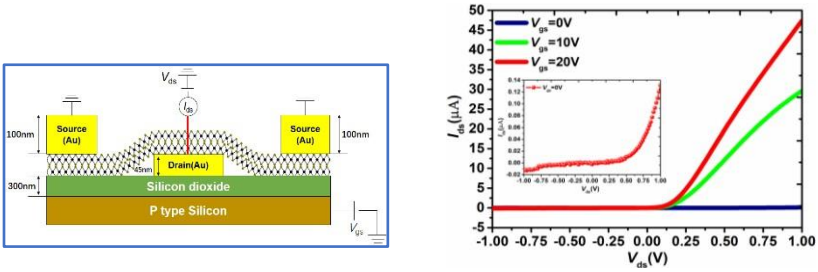


Figure 5.5. 1 Electronic transport properties of MoS_2 nano device with “Misaligned Sandwich” architecture. During the test, 4 different devices were measured by the semiconductor tester. And all the result showed rectification characteristic

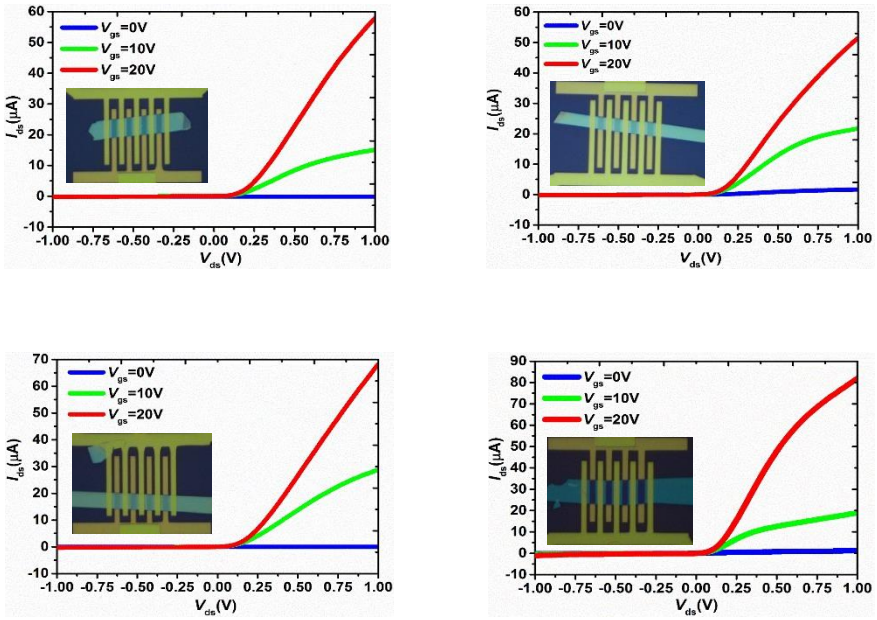


Figure 5.6. 1 Electronic transport properties of MoS_2 nano device with "Misaligned Sandwich" architecture. During the test, 4 different devices were measured by the semiconductor tester. And all the result showed rectification characteristic.

CONCLUSIONS

With the fast development of silicon semiconductor, new material (2D semiconductor materials) is becoming into a key part of advanced technology applications. MoS_2 using its unique electrical properties and physical properties shows a great potential prospect in future industries. Also, by applying different micro-fabrication method, the photoelectric devices are satisfied more wavelength range. The pentamer Nano-optical antennas achieved the near-infrared wavelength light capture. During the 2D material study, the main achievements are as follows:

(1) By having MoS_2 as transistor channel and Nano-optical antennas as enhanced method, the fabricated device successfully captures the incident laser (830nm) in near-infrared wavelength range.

(2) The Nano-optical antennas positions verified the photosensitivity of photoelectric devices. The best position for antennas is located at the drain side and it will increase the photocurrent ~60% to the pervious result.

(3) “Sandwich” structure will improve the rectification characteristic of existed photoelectric devices. The special structure will modify the material’s Fermi level. Thus, changing the band-gap to achieve the rectification characteristic.

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