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A Rapid Charge Pulse Polarizer for
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# A RAPID CHARGE PULSE POLARIZER FOR CONTROLLED-POTENTIAL ELECTROANALYSIS

By

Norman Earl Penix

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## ABSTRACT

## A RAPID CHARGE-PULSE POLARIZER FOR CONTROLLED-POTENTIAL ELECTROANALYSIS

**By**

**Norman Earl Penix**

A microcomputer-controlled charge-pulse polarizer has been developed for controlled-potential electroanalysis. In this polarizer, discreet charge packets are added as needed to achieve or maintain the desired potential. The polarizer consists of five modules in addition to the microcomputer. These are the potential comparison module, the potential step injector, the potential maintenance injector, the control module, and the potential measurement module. The advantages of charge pulse polarization over the conventional analog (continuous current) polarizer are the complete separation of the charging current from the Faradaic current, the elimination of potential control errors due to solution resistance, the digital acquisition of the Faradaic charge, and the integration of the Faradaic current.

A comparison of a conventional analog potentiostat and the charge-pulse polarizer has been performed. Staircase cyclic voltammograms obtained by the charge-pulse polarizer demonstrates it ability to completely eliminate errors due to ohmic drop from the voltammograms and the its ability to completely separate the charging current from the Faradaic current. The total Faradaic charge is obtained by counting the number of quantitative charge injections required to maintain the potential for the

duration of the step. The measured Faradaic charge obtained by the charge-pulse polarizer is shown to **increase** for **decreasing** scan rates. The linear dynamic range obtainable for by the polarizer for a constant injection capacitance was determined to be $2.5 \times 10^3$

To Susan, Brandon, and Liselotte

with all my love

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Special thanks go to Enke group members past and present for their friendship. Special thanks to Ronald Lopshire for editing this dissertation, to Dr. Peter Palmer who kept me sane in the middle of the night, to Dr. Adrian Wade for his compassion when my project was not working, and to Christine Evans for assistance with "simple" chemical problems.

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# CHAPTER 1
# INTRODUCTION

Conventional controlled potential electroanalysis is limited by errors caused by the presence of the electrode double layer capacitance and the resistance of the cell solution. It is the goal of this research to eliminate these errors through the use of the relatively new technique of charge pulse polarization.

Charge pulse polarization is a technique which may be used to control the potential of an electrochemical cell through the rate of injection of discreet charge packets into the cell. In this technique the electrode double layer serves to store the injected charge which may then be used by a Faradaic reaction. The charge is then replenished by another injection as required by to maintain the desired potential. By counting the number of injections required to maintain the cell, the charge consumed by the Faradaic reaction can be obtained. In addition, the potential of the cell is measured between charge pulses when the cell is at open circuit thereby eliminating errors in the measurement of the cell potential due to solution resistance.

The polarizer, which was designed as part of this research, has been used to perform charge-pulse staircase cyclic voltammetry. The resulting voltammograms prove that the polarizer completely eliminates the errors due to charging current and ohmic drop.

**Overview of the Dissertation**

Chapter two briefly introduces potentiostats. The causes of ohmic drops and charging currents and the problems that are discussed. In addition, the concept of potential control by charge pulse polarization is explained and the design goals for the polarizer are given.

Chapter three describes the charge-pulse polarizer. This includes the controlling microcomputer and the individual components of the polarizer. A description of the control language, polyFORTH, which is used with the microcomputer is given including a discussion of how the language works; the programming language used for data analysis, C, is also presented.

Chapter four details the steps required in the balancing of the analog circuitry and the adjustment and characterization of the charge injectors. The values obtained in the characterization of the injectors are reported along with a discussion of the analytical quality of the polarizer.

A comparison of the charge-pulse polarizer with analog potentiostatic control for cyclic voltammetry is presented in chapter five. The results of experiments which were designed to test the ability of the polarizer to eliminate charging current and ohmic drop errors from the voltammograms are given. These results are compared to the results from identical experiments performed using an analog potentiostat. The linear dynamic range obtainable with a given set of charging capacitors is presented along with a discussion of the effect of scan rate on the peak charge obtained. In addition, some closing comments about the polarizer are given.

## CHAPTER 2

## BACKGROUND AND HISTORICAL

The typical electrochemical apparatus used for controlled potential electroanalysis consists of a potentiostat with a three electrode cell in the electronic feedback loop of the control amplifier. The three electrode cell consists of a working electrode, an auxiliary electrode, and a reference electrode. The working electrode is the electrode at which the electrochemical reaction being investigated occurs. The reference electrode provides a constant potential with respect to the solution and thus provides a means of measuring the difference in potential between the working electrode and the solution. As a measuring device only, the reference electrode does not conduct an appreciable amount of current. The auxiliary electrode is added to complete the complete the feedback loop. Of necessity, an electrochemical reaction must occur at the auxiliary electrode which is opposite is sense, but equal in rate to that occurring at the working electrode.

Typically the working electrode and electrolytic solution are chosen such that the electrode behaves as an ideally polarizable electrode, IPE, over the voltage range of the electrochemical experiment (with no analyte present). An IPE is an electrode at which no charge transfer between the working-solution interface occurs regardless of the imposed potential. The difference in potential between the electrode and the solution occurs abruptly at the electrode-solution interface. This non-conducting contact between the solution and the electrode has the properties of an electrical capacitor. The

capacitance it exhibits, known as the double layer capacitance, is dependent upon the surface area of the electrode and the ionic strength of the solution in the cell. This double layer capacitance is different from a usual capacitor in that the double layer capacitance is potential dependent (1). When a redox couple is added to the electrochemical cell, the electrode double layer capacitance can be discharged by the Faradaic reaction. The current that is added to the cell to maintain the potential is equal to current due to the Faradaic reaction.

Another aspect of the electrochemical cell is that the solution has a finite resistance. This resistance can be separated into two categories. The resistance between the auxiliary and the reference electrode, $R_c$, and the resistance between the reference and working electrode, $R_u$. In addition, the resistance of the reference electrode is called $R_r$. The Faradaic reaction acts as a time and potential-dependent resistor capable of discharging the double layer capacitance and is denoted as $Z_f$. A cell equivalent circuit which illustrates these characteristics is shown in Figure 2.1.

Potential control of an electrochemical cell is predicated on the ability to measure accurately and precisely the potential difference between the working electrode and the solution. While it is impossible to measure the absolute potential of the working electrode with respect to the solution, it is possible to measure the potential difference between the working electrode and the reference electrode. The potential measured at the reference electrode with the working electrode at common, is equal to the negative of the potential of the working electrode-solution interface plus the constant potential of the reference electrode-solution interface. When a reaction is occurring in the cell, a finite current must be present. The product of this

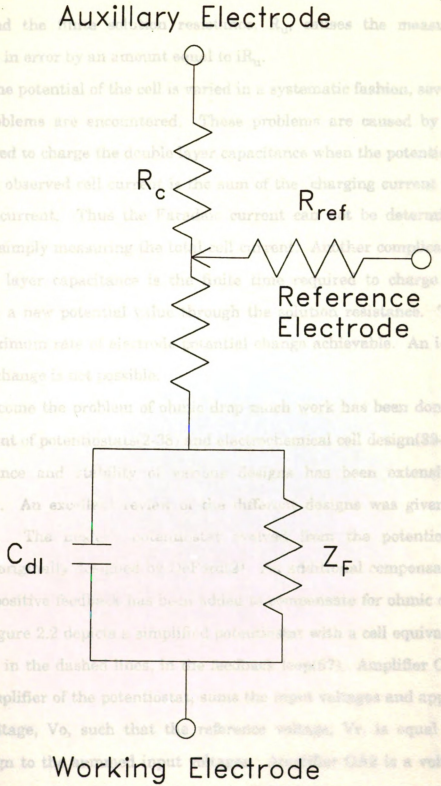


**Figure 2.1 Cell equivalent circuit for the three electrode cell.**

current, i, and the finite solution resistance, $R_u$, causes the measured potential to be in error by an amount equal to $iR_u$.

When the potential of the cell is varied in a systematic fashion, several additional problems are encountered. These problems are caused by the current required to charge the double layer capacitance when the potential is changed. The observed cell current is the sum of the charging current and the Faradaic current. Thus the Faradaic current can not be determined accurately by simply measuring the total cell current. Another complication of the double layer capacitance is the finite time required to charge the capacitance to a new potential value through the solution resistance. This limits the maximum rate of electrode potential change achievable. An ideal step function change is not possible.

To overcome the problem of ohmic drop much work has been done in the development of potentiostats(2-38) and electrochemical cell design(39-57). The performance and stability of various designs has been extensively studied(39-56). An excellent review of the different designs was given by Schroeder(37). The modern potentiostat evolved from the potentiostat configuration originally designed by DeFord(2). An additional compensation circuit using positive feedback has been added to compensate for ohmic drop errors(51). Figure 2.2 depicts a simplified potentiostat with a cell equivalent circuit, shown in the dashed lines, in the feedback loop(57). Amplifier OA1, the control amplifier of the potentiostat, sums the input voltages and applies an output voltage, Vo, such that the reference voltage, Vr, is equal but opposite in sign to the summed input voltages. Amplifier OA2 is a voltage follower which prevents the feedback circuit from drawing an appreciable amount of current from the reference electrode. Amplifier OA3 is a current

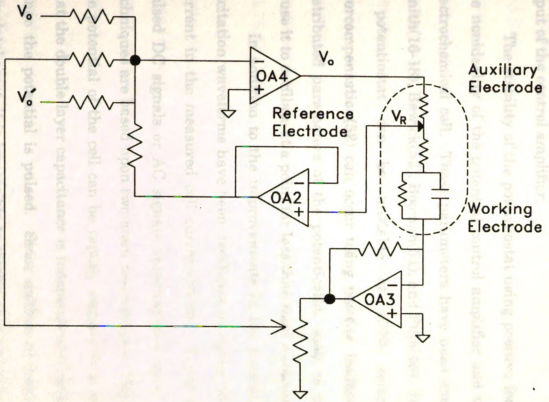


**Figure 2.2** Simplified schematic of a modern three potentiostat with a cell equivalent circuit shown in the feedback loop.

to voltage converter which converts the total cell current into a voltage for subsequent measurement. In addition, a potetnial proportional to the cell current is returned to OA1 as part of the feedback loop. This portion of the feedback loop is the positive feedback mentioned earlier. It is called positive feedback since the output potential is of the same sign as that applied to the input of the control amplifier.

The stability of the potentiostat using positive feedback is governed by the nonideality of the potential control amplifier and the phase shift in the electrochemical cell. These parameters have been extensively analyzed by Smith(16-18), Bewick(52), Booman(51), and Pilla(46). It has been shown that a potentiostat can be unstable at 100% compensation and that overcompensation(52) can occur using positive feedback. In addition, the distributed parameters of the potentiostat, such as stray capacitance can cause it to oscillate at a point far less than total compensation.

In addition to the improvements in the potentiostat, many different excitation waveforms have been developed to reduce the amount of charging current in the measured cell current(58-62). These waveforms are either pulsed DC signals or AC signals superimposed upon a DC signal. These techniques are based upon two main assumptions. The assumptions are that the potential of the cell can be rapidly stepped to a different potential and that the double layer capacitance is independent of potential over the voltage range the potential is pulsed. Since neither of these assumptions can be completely met, it is impossible to totally separate the charging current from the measured cell current.

**Charge Pulse Polarization**

Charge pulse polarization is a technique in which charge pulses are used to control an electrochemical cell. The control function achieved can implement most any of the typical electrochemical techniques employed in electrochemical analysis. The technique of charge pulse polarization was developed concurrently in independent laboratories by Delahay (63,66-70) and Reinmuth (64,65). The basis of the coulostatic technique is to step the potential of the electrochemical cell by the rapid injection of a known quantity of charge followed by returning the cell to open circuit and recording the potential decay. The resulting decay curves are extrapolated back to time zero using equations developed by Delahay (66), Reinmuth (65) and others (71-88). Several workers have used a compilation of the recorded decays to reconstruct voltammograms from a series of potential steps. The source of charge used in these experiments were from timed constant current sources (71,76,83,85,86-88) or capacitive discharge (78-82,84).

An alternative to conventional potentiostatic control of an electrochemical cell is potential control by charge pulse polarization. Potential control by charge pulse polarization is accomplished by injecting charge of appropriate polarity whenever the cell potential deviates from the desired control potential.

Five polarizers which use charge pulse polarization have been developed previously. The first polarizer developed for potential control was the "digiopotentiograter" of Goldsworthy and Clem (89). This polarizer was a hybrid of a constant current polarizer and a charge-pulse polarizer. Figure 2.3 is a block diagram of this digiopotentiograter. The potential control is through the addition of discreet charge pulses. A constant current source is also connected to the cell so that a significant number of counts would be

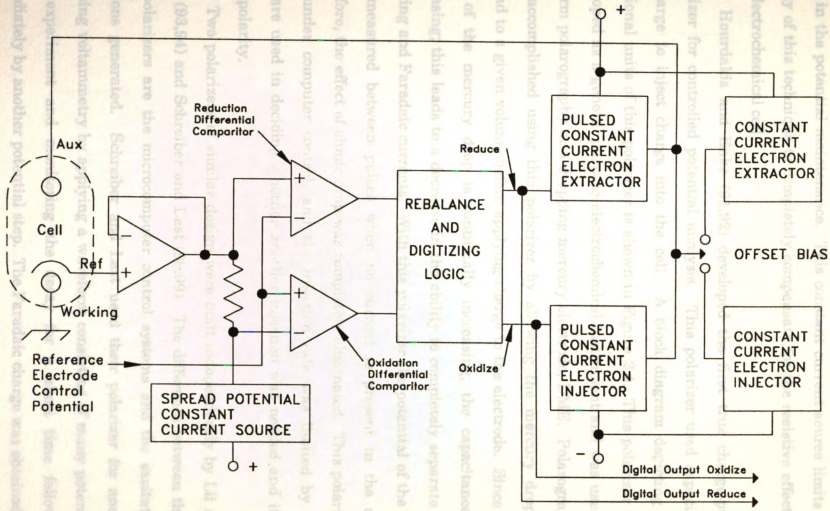


**Figure 2.3** A block diagram of Goldsworthy and Clem's "digiopotentiostat".

used in the potential maintenance. This constant current source limits the ability of this technique to completely compensate for the resistive effects of the electrochemical cell.

Hourdakis and Enke (91,92) developed the first true charge-pulse polarizer for controlled potential analysis. This polarizer used capacitive discharge to inject charge into the cell. A block diagram depicting the functional units of this polarizer is shown in Figure 2.4. This polarizer was developed as a general purpose electrochemical instrument and was used to perform polarography at a dropping mercury electrode, DME. Polarography was accomplished using this polarizer by allowing the mercury drop to expand to a given volume before applying charge to the electrode. Since the area of the mercury drop is continually increasing, the capacitance is increasing; this leads to a decrease in the ability to completely separate the charging and Faradaic currents. With this polarizer the potential of the cell was measured between pulses when no current is present in the cell; therefore, the effect of ohmic drop was completely eliminated. This polarizer was under computer control, and the injection rate was limited by the software used in deciding whether another injection was needed and if so what polarity.

Two polarizers of similar design were built independently by Lii and Enke (93,94) and Schreiber and Last (98,99). The difference between these two polarizers are the microcomputer control systems and the excitation functions generated. Schreiber and Last used their polarizer for anodic stripping voltammetry by applying a waveform consisting of many potential step experiment and monitoring the decay for a short time followed immediately by another potential step. The Faradaic charge was obtained by measuring the cell voltage six separate times on each pulse at three different

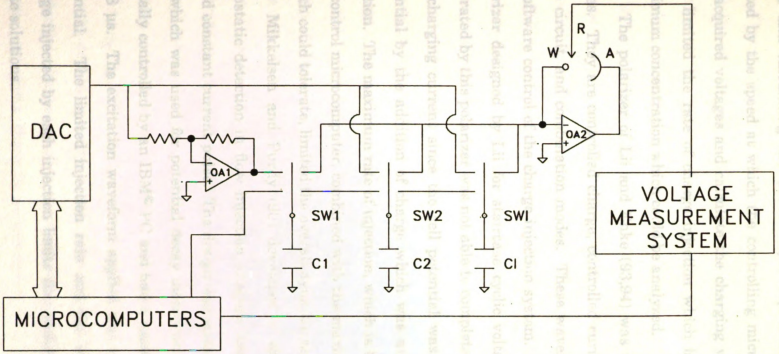


Figure 2.4 A block diagram of the charge pulse polarizer designed by Hourdakis and Enke.

gains and calculating the double layer capacitance. This polarizer was limited by the speed at which the controlling microcomputer could process the acquired voltages and calculate the charging voltages for the injectors. This limited the rate of charge injection which is directly related to the maximum concentration which could be analyzed.

The polarizer of Lii and Enke (93,94) was used in several different modes. They are controlled charge, controlled current, controlled potential, open circuit, and combination modes. These waveforms were accomplished by software control of the charge injection system. Engerer (95,96) used the polarizer designed by Lii for staircase cyclic voltammetry. The staircase generated by this polarizer was not able to completely eliminate the effects of the charging current since the cell potential was trimmed to the desired potential by the addition of charge which was attributed to the Faradaic reaction. The maximum rate of injection, which is limited by the response of the control microcomputer, combined with the maximum charge injection the switch could tolerate, limited the overall dynamic range of the polarizer.

Mikkelsen and Purdy (90) developed a charge-pulse polarizer for coulostatic detection in flow injection analysis based on the injection of a timed constant current pulse. The design was similar to that of Nieman (86-88) which was used for potential decay measurements. The polarizer was digitally controlled by an IBM© PC and had a maximum injection frequency of 38 μs. The excitation waveform applied was a charge pulse based DC potential. The limited injection rate and the relatively large minimum charge injected by each injection limits the usefulness of this polarizer for dilute solutions..

**General Method for Controlled Potential Electroanalysis**

Figure 2.5 illustrates a typical diffusion controlled experiment in which the cell potential is maintained by a charge-pulse polarizer. Since the injection of the charge pulses is a discrete process, a control window is defined in which the potential is maintained. In Figure 2.2, it is assumed that the cell potential has just been changed, is within the control window, and the cell is at open circuit. Further it is assumed that a diffusion-controlled Faradaic reaction can occur at this potential but no reaction has occurred as yet. Since the cell potential has become more negative, a corresponding decrease in the ratio of oxidized species to the reduced species at the electrode surface occurs. This change in the surface concentration ratio produces a net reaction current which is equal to the rate of diffusion of the oxidized species to the electrode surface. Since the cell is at open circuit between charge injections, the charge required by the reaction current comes from the electrode double layer which causes the cell potential to drift positive, toward the control window threshold. As the potential of the cell drifts more positive, the surface concentration ratio of oxidized species to reduced species increases, thereby decreasing the surface concentration gradient of the oxidized species and reducing the net reaction current. When the cell potential crosses the threshold, a charge injection is triggered. This injection occurs very rapidly causing a rapid change in the electrode potential equal to $q_s/C_{dl}$, where $q_s$ is the standardized amount of charge injected and $C_{dl}$ is the double layer capacitance. The magnitude of $q_s$ is chosen to provide a potential change smaller than the magnitude of the control window. Between injections there is no current through the cell; therefore, the

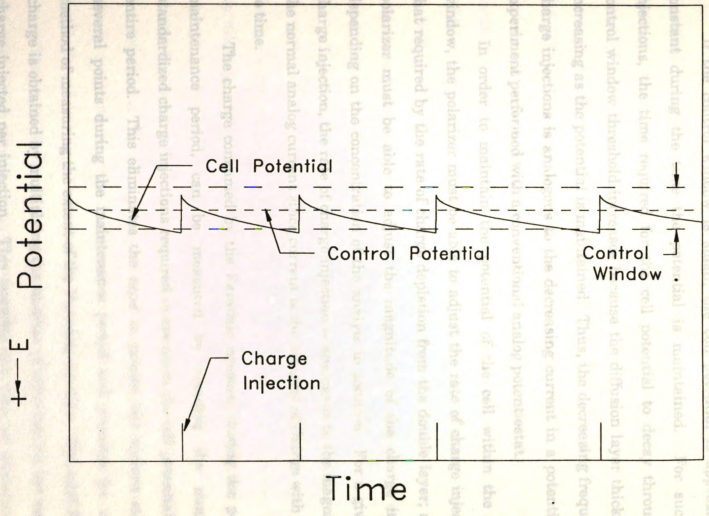


**Figure 2.5** **Potential control by charge pulse polarization.**

potential of reference electrode is an accurate measure of the working electrode potential and allows accurate potential control unaffected by the Faradaic current.

If the control window is small, the cell potential is approximately constant during the time the potential is maintained. For successive injections, the time required for the cell potential to decay through the control window threshold increases because the diffusion layer thickness is increasing as the potential is maintained. Thus, the decreasing frequency of charge injections is analogous to the decreasing current in a potential step experiment performed with a conventional analog potentiostat.

In order to maintain the potential of the cell within the control window, the polarizer must be able to adjust the rate of charge injection to that required by the rate of charge depletion from the double layer; and the polarizer must be able to adjust the magnitude of the charge injection depending on the concentration of the analyte in solution. For a given size charge injection, the rate of charge injection is analogous to the magnitude of the normal analog current since current is the integral of charge with respect to time.

The charge consumed by the Faradaic reaction, during the potential maintenance period, can be measured by counting the number of standardized charge injections required to maintain the cell potential for the entire period. This eliminates the need to sample the current at one or several points during the maintenance period and provides for a digital method of measuring the extent of the Faradaic reaction. The total Faradaic charge is obtained by multiplying the number of injections by the amount of charge injected per injection. This quantity can then be converted to the average Faradaic current by dividing the total charge injected by the time

over which the potential was maintained. This average Faradaic current is equivalent to the integrated Faradaic current over the entire time the potential was maintained.

To achieve a varying potential experiment (any of the voltammetries), a method is needed to change as well as maintain the set potential. Three distinct possibilities for changing the set potential are: (1) a linear potential ramp, (2) a non-uniform step ramp, or (3) a uniform step ramp.

In a linear potential ramp, the cell potential is constantly varied with time. This gives rise to the charging current which is a function of scan rate and double layer capacitance. Since the charging and Faradaic currents occur simultaneously, they cannot be distinguished experimentally. Additionally, since the double layer capacitance is not constant with respect to voltage, the Faradaic and charging currents cannot be separated mathematically. Using a linear ramp to change the potential would negate the polarizer's usefulness and therefore was not used.

The other possible choices for changing the desired control potential of the cell involve using step functions to approximate a potential ramp. Step functions are used with potentiostats to reduce the effects of charging current by allowing sufficient time to pass before sampling the current, since the charging current decays more rapidly than the Faradaic current. By using a charge impulse large enough to step the electrode to its new control potential, the potential of the cell is changed very quickly. If the number of standard charge injections required to maintain the potential are now counted, the separation of charging charge and Faradaic charge is perfectly achieved.

The magnitude of the potential step function generated by the polarizer can be either uniform or non-uniform. A non-uniform step function would result from the addition of a constant amount of charge for each step.

As the double layer capacitance changes with electrode potential, the size of the step will vary. Since the Faradaic current measured is a function of all previous step voltages and times, the voltammograms obtained will deviate from the theoretical shape and magnitude and thus will be more difficult to interpret.

A uniform potential step function can be obtained by adjusting the amount of charge injected at each step to compensate for the changing double layer capacitance. The size of the step injections can be varied by determining the amount of capacitance from the previous step and correcting the amount of charge injected by a correction factor. Another method by which the size of the step injection can be varied is to dynamically adjust the voltage which charges the injection capacitors. This can be accomplished by measuring the difference from the control potential after each injection, amplifying this difference and using the amplified difference as the charging voltage.

**Design Goals**

The design goals for the charge-pulse polarizer in this work are: (1) to be able to add rapidly a preset and known quantity of charge at an automatically controlled rate to maintain the cell potential, (2) to add a variable amount of charge at a predetermined times to step the potential, (3) to count the number of injections made during potential maintenance, (4) to monitor and control the cell potential without the need for an analog to digital conversion, and (5) to increase the speed of its control logic thereby increasing the dynamic range of the system. These goals were chosen such that the benefits of charge-pulse polarization are achieved and yet retain the flexibility to perform a variety of voltammetric techniques.

## CHAPTER 3

## THE CHARGE-PULSE POLARIZER

In this chapter, a complete description of the charge-pulse polarizer which was developed is presented. The goal of the instrument is to control the potential of an electrochemical cell without having to compensate for charging current or ohmic drop in the measured voltage. All major parts of the design are discussed: the microprocessor, the charge injection system, the voltage measurement system, and the software for the data acquisition and manipulation.

### The Microcomputer

Figure 3.1 is a detailed block diagram of the microcomputer system and the charge-pulse polarizer. The microcomputer designed by Bruce Newcome (15) is based on the Intel 8088 16 bit internal 8 bit external microprocessor. The same board contains 8 Kbytes of RAM and 8 Kbytes of PROM, two USARTS (Universal Synchronous Asynchronous Receiver TransmitterS), and an interrupt controller. The system is readily expandable through a mother board/backplane arrangement known locally as the "Bruce Bus" (1). This extension of the CPU bus allows user modules (interface circuits) access to the CPU bus and provides for connector space to remote devices. The microcomputer and polarizer consist of 4 mother boards.

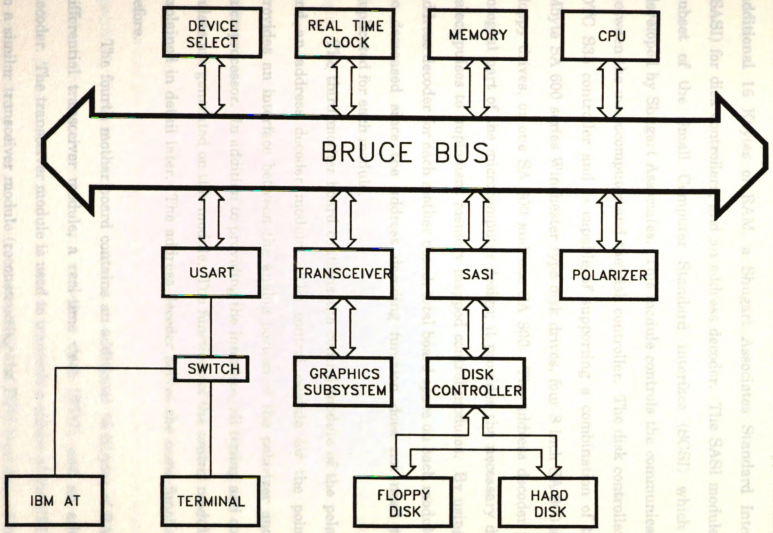


**Figure 3.1** Block diagram of the microcomputer-controlled charge-pulse polarizer

The first mother board is the microcomputer described above. The second mother board, an extension of the CPU bus only, contains an additional 16 Kbytes of RAM, a Shugart Associates Standard Interface (SASI) for disk controllers, and an address decoder. The SASI module is a subset of the Small Computer Standard Interface (SCSI) which was developed by Shugart Associates. This module controls the communications between the microcomputer and the disk controller. The disk controller is a DTC S35 controller and is capable of supporting a combination of two 5 Mbyte SA 600 series Winchester type disk drives, four 8 inch SA 800 series floppy drives, or one SA 600 and one SA 800. The address decoder is an integral part of the microcomputer design; it provides the necessary device select pulses to implement memory mapped control modules. By using one address decoder for each mother board, total board space on each module can be decreased since the address decoding function does not need to be duplicated for each module.

The third mother board contains the control module of the polarizer and an address decoder module. The control module for the polarizer provides an interface between the analog portion of the polarizer and the microprocessor. In addition to providing the interface, all timing and control pulses are generated on this module. The functions of the control module are explained in detail later. The address decoder serves the same function as before.

The fourth mother board contains an additional 16 Kbytes of RAM, a differential transceiver module, a real-time clock (RTC), and an address decoder. The transceiver module is used to transmit a subset of the CPU bus to a similar transceiver module (reconstructing the CPU bus) housed in the graphics subsystem. The graphics subsystem also includes a 9-inch Ball

monitor and a Matrox 256 X 256 graphics display board. This system provides a 256 by 256 dot display, each individually addressed. Timing of various components can be controlled by the real time clock which has a resolution of 0.1 millisecond. The RTC can be programmed to generate output pulses at ten-fold intervals from 1 ms to 1 day. This is not sufficient for the step timing but can provide accurate delays between repeated experiments and information on the time required for various processes.

## DESCRIPTION OF THE POLARIZER

The polarizer was designed in the same manner as the microcomputer in that each functional unit is a separate module. This facilitates modifications to the design of the polarizer. The individual modules which form the polarizer are shown in Figure 3.2. They are the comparison circuit, the potential maintenance injector, the potential step injector, the control logic, and the analog to digital converter. The comparison circuit is responsible for monitoring the potential of the electrochemical cell between charge injections and for returning the results to the control module. In addition, the Comparison circuit generates the reference voltage (setpoint potential) for the control window as well as the control window. The charge injection system is comprised of two separate injectors, the potential step injector and the potential maintenance injector. The potential step injector is specifically designed to change the potential rapidly from one setpoint to another. The maintenance injector is designed to maintain the cell potential within a given control window about the setpoint potential for the duration of the potential step. The control module generates all of the necessary timing and control signals used throughout the polarizer and serves as a remote bus

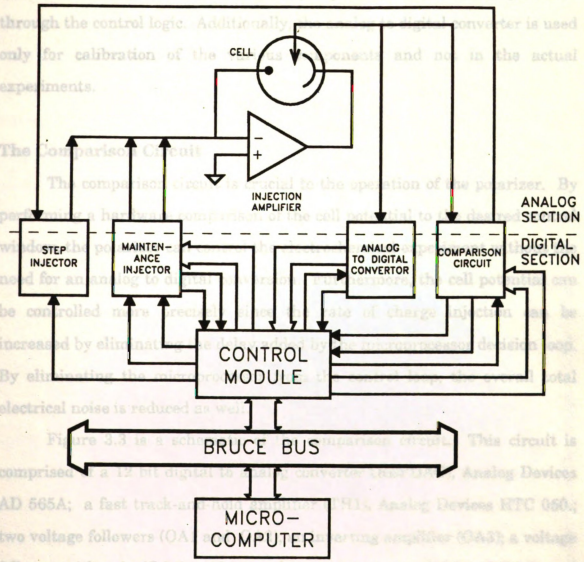


**Figure 3.2** Detailed block diagram of the charge-pulse polarizer.

for the exchange of information between modules. In addition, this module is the sole interface to the microcomputer system. Figure 3.2 indicates the flow of information through the polarizer. It is important to note that the analog functions of the polarizer are completely separated from the microprocessor through the control logic. Additionally, the analog to digital converter is used only for calibration of the various components and not in the actual experiments.

**The Comparison Circuit**

The comparison circuit is crucial to the operation of the polarizer. By performing a hardware comparison of the cell potential to the desired control window, the polarizer can control the electrochemical experiment without the need for an analog to digital conversion. Furthermore, the cell potential can be controlled more precisely since the rate of charge injection can be increased by eliminating the delay added by the microprocessor decision loop. By eliminating the microprocessor from the control loop, the overall total electrical noise is reduced as well.

Figure 3.3 is a schematic of the comparison circuit. This circuit is comprised of a 12 bit digital to analog converter (REFDAC), Analog Devices AD 565A; a fast track-and-hold amplifier (TH1), Analog Devices HTC 050.; two voltage followers (OA1 and OA2); an inverting amplifier (OA3); a voltage follower with gain (OA4); and two voltage comparators (OA5 and OA6); and resistors R1 - R14. Voltage follower OA1, an Analog Devices AD 380, is used to buffer the reference electrode potential. This device was chosen for its low input bias current and high full power bandwidth. The remaining operational amplifiers OA2, OA3, and OA4 are Precision Monolithics Inc. OP77 amplifiers and the comparators OA5 and OA6 are National

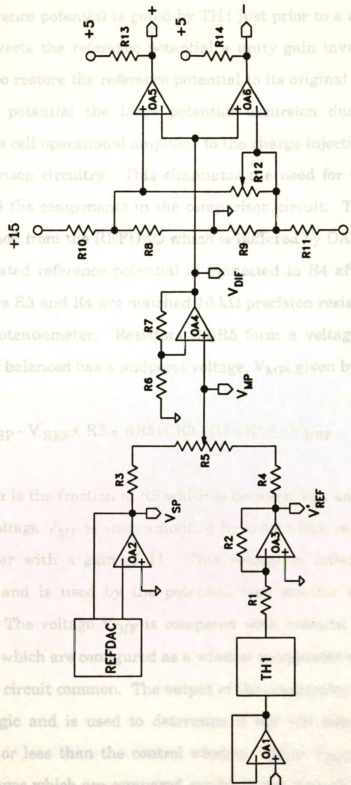


Figure 3.3 Comparison circuit of the charge-pulse polarizer.

Semiconductor LF311's. After input buffering of the reference electrode by OA1, the reference potential is gated by TH1 just prior to a charge injection. Since TH1 inverts the reference potential a unity gain inverting amplifier, OA3, is used to restore the reference potential to its original sign. By gating the reference potential the large potential excursion due to the initial response of the cell operational amplifier to the charge injection is not sensed by the comparison circuitry. This eliminates the need for wide bandwidth response of all the components in the comparison circuit. The set potential ($V_{SP}$) is obtained from the REFDAC which is buffered by OA2 and connected to R3. The gated reference potential is connected to R4 after inversion by OA3. Resistors R3 and R4 are matched 10 kΩ precision resistors and R5 is a 500 Ω trim potentiometer. Resistors R3-R5 form a voltage divider which when properly balanced has a midpoint voltage, $V_{MP}$, given by equation 1.

$$V_{MP} = [(V_{SP} - V'_{REF})( R3 + \alpha R5)/( R3 + R4 + R5)] - V'_{REF} \qquad (1)$$

The quantity $\alpha$ is the fraction of R5 which is between $V_{SP}$ and the center tap of R5. The voltage $V_{MP}$ is then amplified by OA4 which is configured as a voltage follower with a gain of 11. This voltage is called the difference voltage $V_{DIF}$ and is used by the potential step injector and the voltage comparators. The voltage $V_{DIF}$ is compared with common by comparators OA5 and OA6 which are configured as a window comparator with the window uniform about circuit common. The output of the comparators is connected to the control logic and is used to determine if the cell potential is within, greater than, or less than the control window. Since $V_{DIF}$ is amplified by OA4, the voltages which are compared can be larger than the desired control window. Comparators OA5 and OA6 can thus be used without hysteresis

which enables them to respond more rapidly to changes at their inputs and eliminates the error in potential control due to the additional voltage added by hysteresis.

From Equation 1, it can be seen that the output of the voltage divider will be zero only if the network is balanced under conditions where the two inputs are equal in magnitude and opposite in sign. Any deviations in this condition will cause the output to have a nonlinear gain as the input voltage increases.

The window threshold voltages are generated by a voltage divider network which consists of resistors R8 - R12. Resistor R12 is a 500 Ω ten-turn potentiometer which is used to adjust the size of the control window. The control window voltage, relative to the negative supply voltage, can be calculated using the equation for a voltage divider. Equations 2 and 3 are the equations for the positive threshold and the negative threshold respectively.

$$V_{+th} = [(V_+ - V_-)\,(R10 + R_e)/(R10 + R11 + R_e)] \quad (2)$$

$$V_{-th} = [(V_+ - V_-)\,R10\,/(R10 + R11 + R_e)] \quad (3)$$

The quantities $V_+$ and $V_-$ are provided by the power supply and $R_e$ is the equivalent resistance of R8, R9, and R12. The value of Re is given by equation 4, where αR12 is the fraction of R12 which is not shorted out by the center tap.

$$R_e = 1/(\,1/(R8 + R9) + 1/\alpha R12) \quad (4)$$

By adjusting the value of $R_e$ the operator can adjust the size of the control window. Using this configuration, the comparison voltage is always near common and the comparison window is nominally symmetric about common. By maintaining the control window near common, the need for amplifiers with extremely fast bandwidths is eliminated while still maintaining a very rapid response time to changes in the cell potential.

**The Maintenance Injector**

The maintenance injector is responsible for maintaining the cell potential within a given control window for the duration of the step. This is accomplished by the rapid injection of equally sized charge pulses at a variable rate which is governed by the rate of the Faradaic reaction at the working electrode. The schematic of this injector is shown in Figure 3.4. The injector consists of: a 12 bit digital to analog converter (INJDAC), Analog Devices AD 565A; three operational amplifiers (OA7, OA8 and OA9), National Semiconductor LF 411; four switches (S1 - 4), Harris HI 381, four resistors (R15 - 18), and two calibrated capacitors. In addition, the cell amplifier (OA10) is an Analog Devices AD 380. The charging voltage is obtained from INJDAC which is configured to provide a 0 to 5 volt unipolar output with an accuracy of 0.00061 volts. The output of INJDAC is then buffered by OA7 to provide a stable voltage source for OA8 and OA9 which generate the two charging voltages which are equal in magnitude but opposite in sign. The outputs of OA8 and OA9 are connected to the calibrated capacitors through S1 and S2 respectively. The outputs of OA8 and OA9 are isolated from the switches by R17 and R18, 100 Ω resistors, to prevent the amplifier output from being affected by the large change in the capacitive load due to the opening and closing of the switches The calibrated capacitors

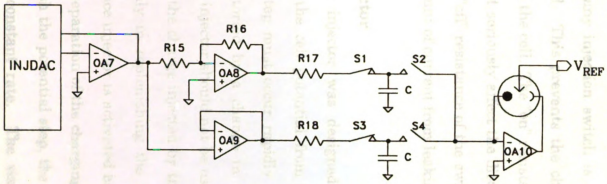


Figure 3.4 Maintenance injector schematic of the charge-pulse polarizer.

are then connected to the summing point of the cell amplifier, OA10, through S3 or S4, respectively. Having both a positively and negatively charged capacitor available to inject charge into the cell without delay increases the versatility and control of the maintenance injector. Timing of the switches is such that 400 ns before any injection switch is closed, the corresponding charging switch is opened. This prevents the charging voltage from ever being connected directly to the cell. The "on" resistance of the switches is less than 30 ohms and does not seriously affect the discharge or charging time of the capacitors. The large "off" resistance of the switches, greater than 3 GΩ, prevents a significant amount of current from leaking into the cell.

**The Potential Step Injector**

The potential step injector was designed to provide an efficient mechanism for changing the cell potential from one setpoint potential to another. The potential step must occur rapidly so that the shape of the voltammogram is not distorted by a change in the diffusion profile. In addition, the maintenance injector should not be used to trim the potential to the desired setpoint since the charge injected by the maintenance injector is considered to be used only in replenishing the charge consumed by the reaction. If the maintenance injector is activated before the desired potential is achieved, the complete separation of the charging and Faradaic currents is not possible. To accomplish the potential step, the injector injects a variably sized charge pulse at a constant rate. The size of the charge pulse is determined by the amplified difference between the cell potential and the setpoint potential which is then used as the charging voltage for the injection capacitor. By dynamically adjusting the charging voltage, the cell potential is stepped in a rapid yet controlled manner.

**Figure 3.5 Schematic of the potential step injector**

The schematic for this injector is shown in Figure 3.5. The circuitry consists of an 8 bit multiplying digital to analog converter (IDAC), National Semiconductor 0830; two operational amplifiers OA11 and OA12, two switches S5 and S6, and two resistors R17 and R18. The amplifiers and switches are the same as those used in the maintenance injector. The charging voltage is obtained from $V_{DIF}$ of the comparison circuit which is connected to the reference input of the IDAC. The output of the IDAC is amplified by OA11 and buffered by OA12. This buffered voltage is used to charge the step injection capacitor through S5. Switch S6 connects this capacitor to the cell amplifier. In this configuration, the IDAC is being used as a current switch which allows the operator to select the desired gain for the charging voltage before the experiment begins. The design of this injector allows the charging voltage to be dynamically adjusted as the double layer capacitance changes. This enables the cell to be charged in an efficient manner without intervention from the microprocessor or the use of repetitive runs to determine the exact charge needed.

**Analog To Digital Converter**

An analog to digital converter (ADC) was included in the design of the polarizer as a means to calibrate and verify proper operation of the polarizer. Figure 3.6 is the schematic of the ADC module. The converter is an Analog Devices HAS 1200 which has a conversion time of 2 μs. A fast conversion speed allows the operator to check the cell potential by software control at anytime along the potential curve. To insure that the input signal is stable and within the operating range of the ADC, two operational amplifiers (OA13 and OA14) and a track and hold amplifier (TH2) are incorporated. These components are of the same type described previously. The reference

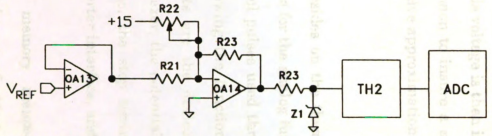


Figure 3.6 Schematic of the analog-to-digital converter.

potential is buffered by OA13 and connected to OA14, a summing amplifier with a gain of 2, through resistor R21. Trim potentiometer R22 is used to provide a constant offset of 5 volts to the summing point. This allows the ADC to be used in the unipolar mode on a zero to -10 volt scale. This is the scale which offers the greatest protection from an overload. In addition, the reference potential is amplified by a gain of 2. The output of OA14 is clipped to 13 volts by a zener diode (Z1). This voltage is then input to the TH2 where the signal is held prior to a conversion to insure a stable voltage. This is necessary since the ADC is a successive approximation type converter.

**The Control Module**

The control module which resides on the third mother board of the microcomputer provides the interface for the analog functions of the polarizer and generates all timing and control pulses used throughout the polarizer. Figure 3.7 is a block diagram showing the functional components of the control module. These components are the device select, the data bus demultiplexer, the data bus multiplexer, the potential step control logic, the potential maintenance control logic, the step timing logic, the injection counters, the analog to digital converter interface, and the PAR 303A control logic.

The control module is a memory mapped peripheral to the microcomputer and decodes a selected range of addresses to be used as device selects. This is similar to the manner in which the standard chip select module of the Bruce Bus functions (15,16), except that the decoding scheme is carried out such that sequential addresses can be used to trigger events with reproducible timing. The device select decodes an address field of 512 bytes into eight 64 byte segments. Whenever any address within a given 64-byte

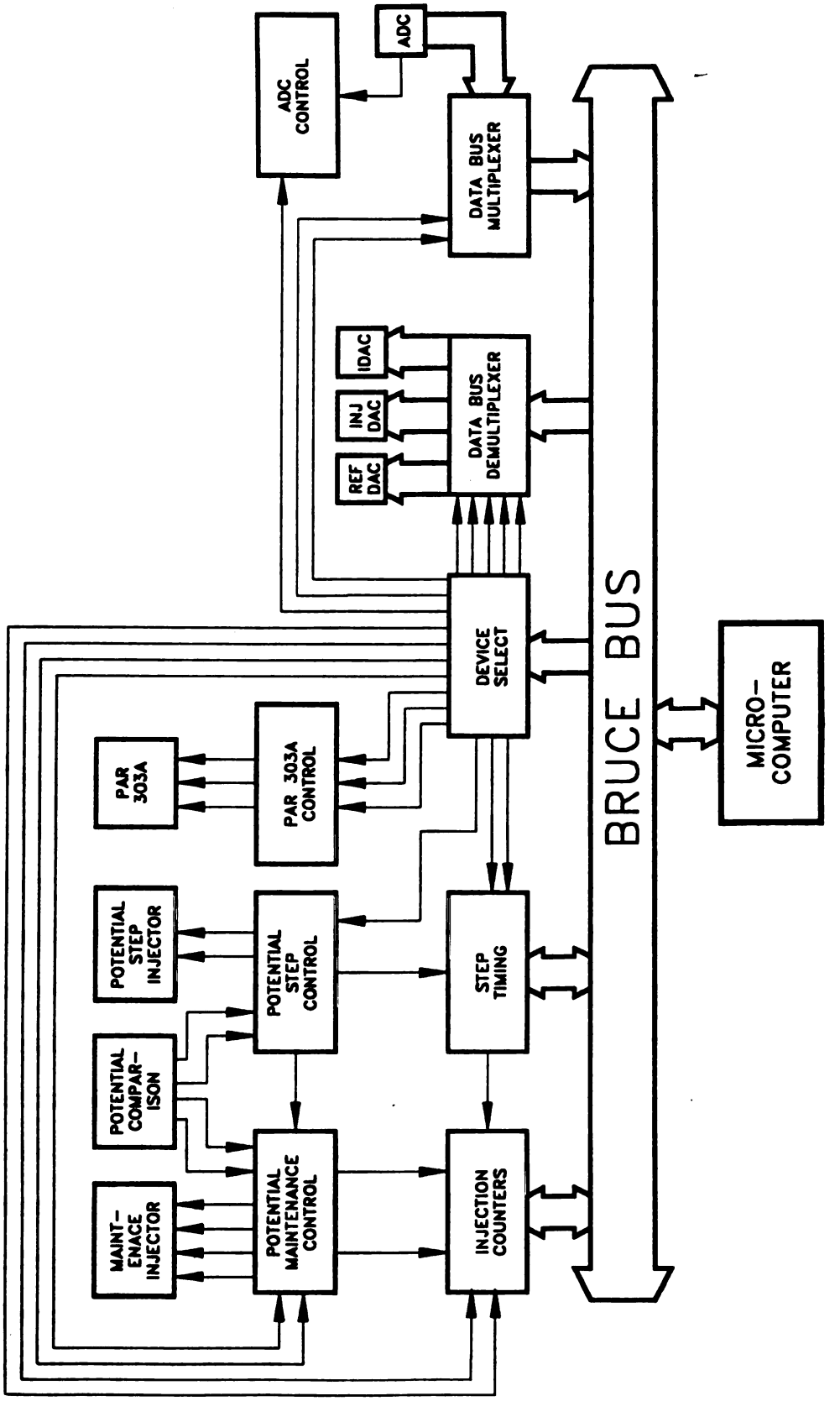


**Figure 3.7** Detailed block diagram of the charge-pulse polarizer control module.

segment is written on the address bus of the microprocessor an output pulse is generated. The eighth 64-byte segment is further decoded into eight 8-byte segments which are qualified by the read and write strobe from the microcomputer. By qualifying these eight 8-byte segments, an output pulse is only generated when a valid read or write operation is occurring. This prevents stray output pulses from being generated by the device select. The first two 8-byte segments are further decoded into sixteen 1-byte segments which are used to trigger individual devices on the control module. Figure 3.8 is a schematic of the device select function of the control module. Table 3.1 contains the description and address(s) of each functionality.

In addition to address decoding, the control module provides several types of data multiplexing and demultiplexing for the different analog modules. Data for the reference DAC is double buffered and demultiplexed from 8 to 12 bits and all 12 bits must be simultaneously written to the DAC. The schematic for this circuit is shown in Figure 3.9. By using double buffering, the reference value can be updated prior to issuing the command to start a new step. This allows the microcomputer to setup the next step during the interrupt which handles the data collection. The data for the maintenance injector DAC needs only to be demultiplexed and written simultaneously to the DAC. This method of demultiplexing allows the processor to change the value of any charge injection by simply writing new data to the control module. Since the microcomputer can change the charging voltage at any time during an experiment, a wide variety of different experimental waveforms are possible. The schematic for this type of demultiplexing is shown in Figure 3.10. The ADC generates 12 bits in parallel and the data must be multiplexed onto the eight bit CPU data bus.

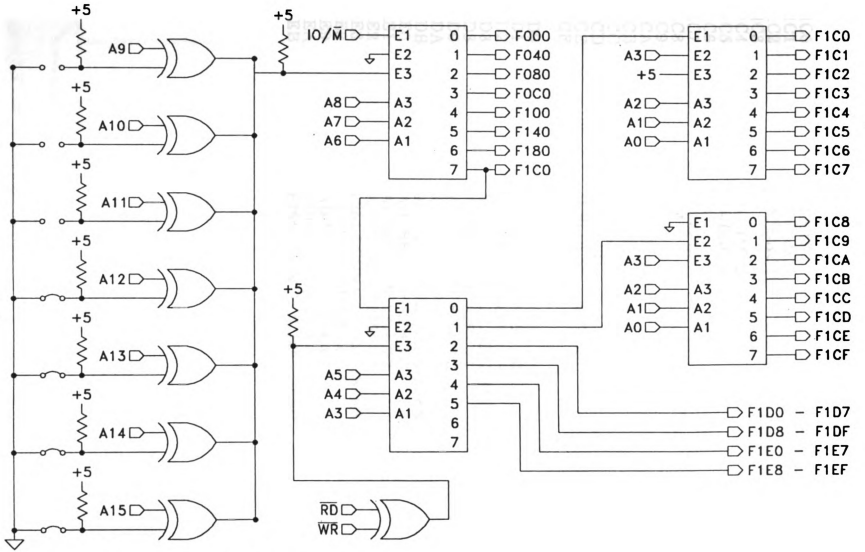


**Figure 3.8** Schematic of the device select logic.

TABLE 3.1. Hardware addresses of the polarizer interface.

| | |
|---|---|
| F1C0 | START |
| F1C1 | REFDAC L |
| F1C2 | REFDAC H |
| F1C3 | |
| F1C4 | INJDAC L |
| F1C5 | INJDAC H |
| F1C6 | IDAC |
| F1C7 | SAMPLE |
| F1C8 | ON |
| F1C9 | OFF |
| F1CA | LATCH DATA H |
| F1CB | LATCH DATA L |
| F1CC | PURGE |
| F1CD | STOP PURGE |
| F1CE | DISLODGE/DISPENSE |
| F1CF | |
| | |
| F1D0 | ADDRESS OF 8254-1-1 |
| F1D1 | ADDRESS OF 8254-1-2 |
| F1D2 | ADDRESS OF 8254-1-3 |
| F1D3 | 8254-1 CONTROL REGISTER |
| F1D8 | ADDRESS OF 8254-2-1 |
| F1D9 | ADDRESS OF 8254-2-2 |
| F1DA | ADDRESS OF 8254-2-3 |
| F1DB | 8254-2 CONTROL REGISTER |
| F1E0 | ADDRESS OF 8254-3-1 |
| F1E1 | ADDRESS OF 8254-3-2 |
| F1E2 | ADDRESS OF 8254-3-3 |
| F1E3 | 8254-3 CONTROL REGISTER |
| F1E8 | ADDRESS OF 8254-4-1 |
| F1E9 | ADDRESS OF 8254-4-2 |
| F1EA | ADDRESS OF 8254-4-3 |
| F1EB | 8254-4 CONTROL REGISTER |

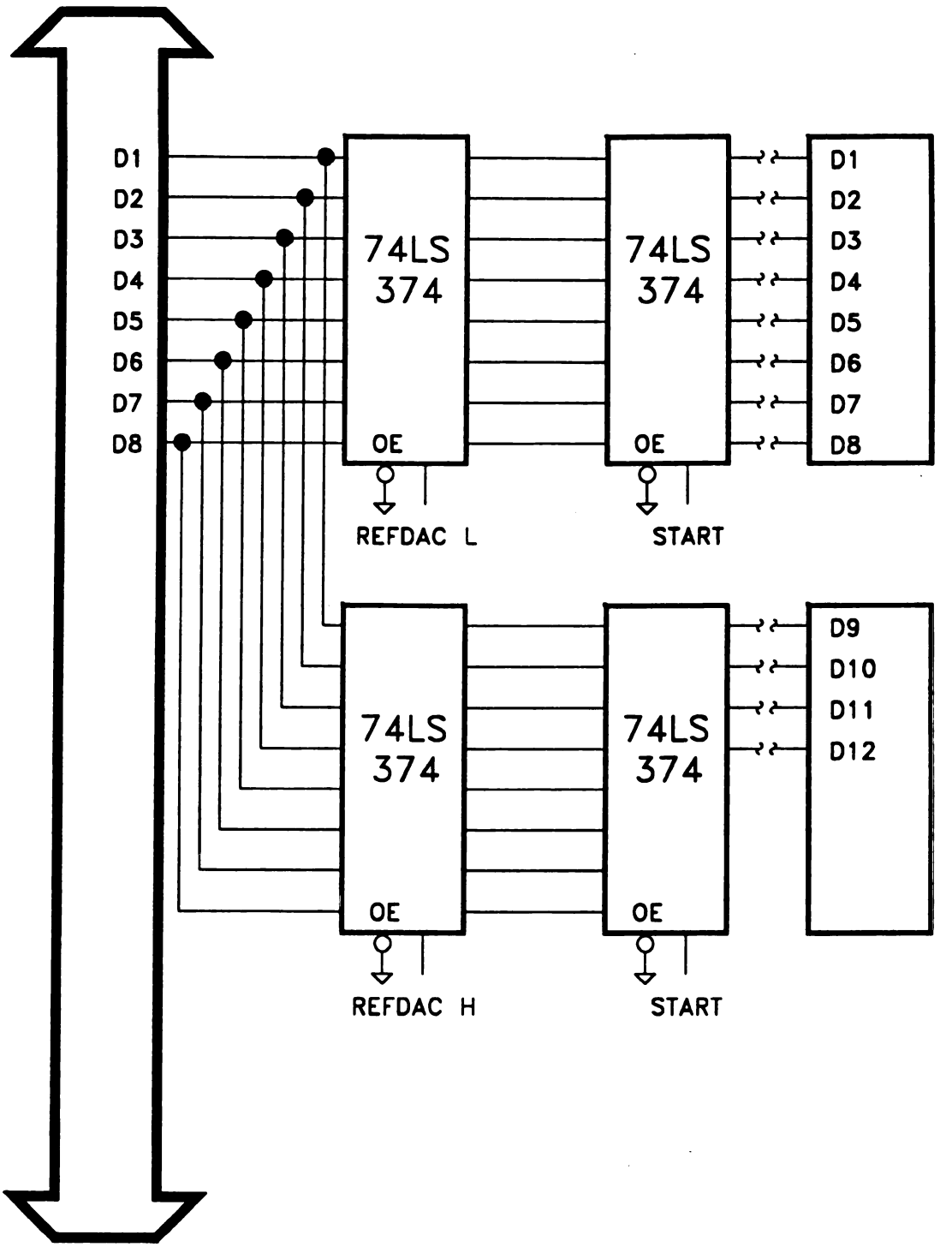


**Figure 3.9** Schematic of the double buffered demultiplexer for the reference DAC.

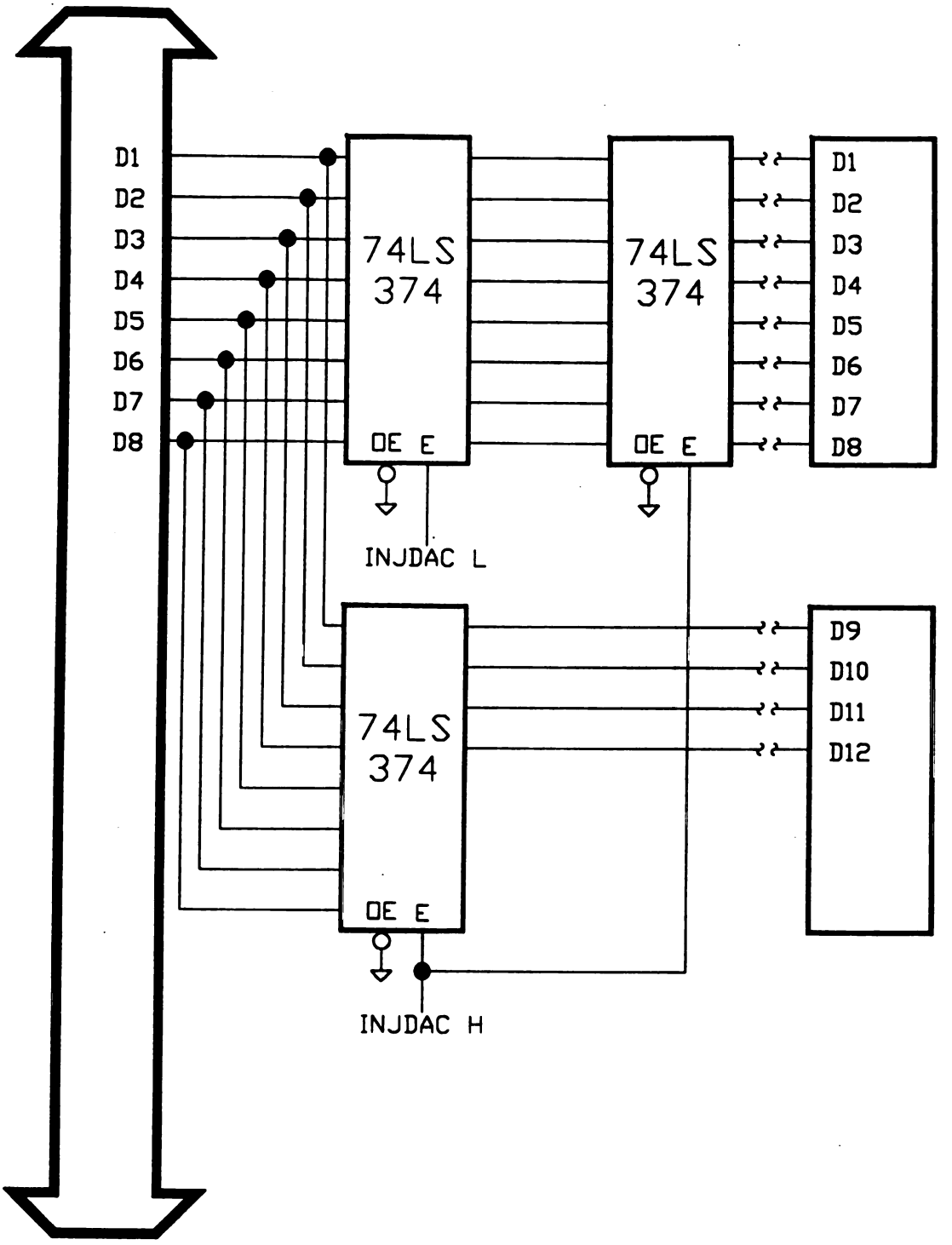


**Figure 3.10 Schematic of the demultiplexer for the maintenance injector DAC.**

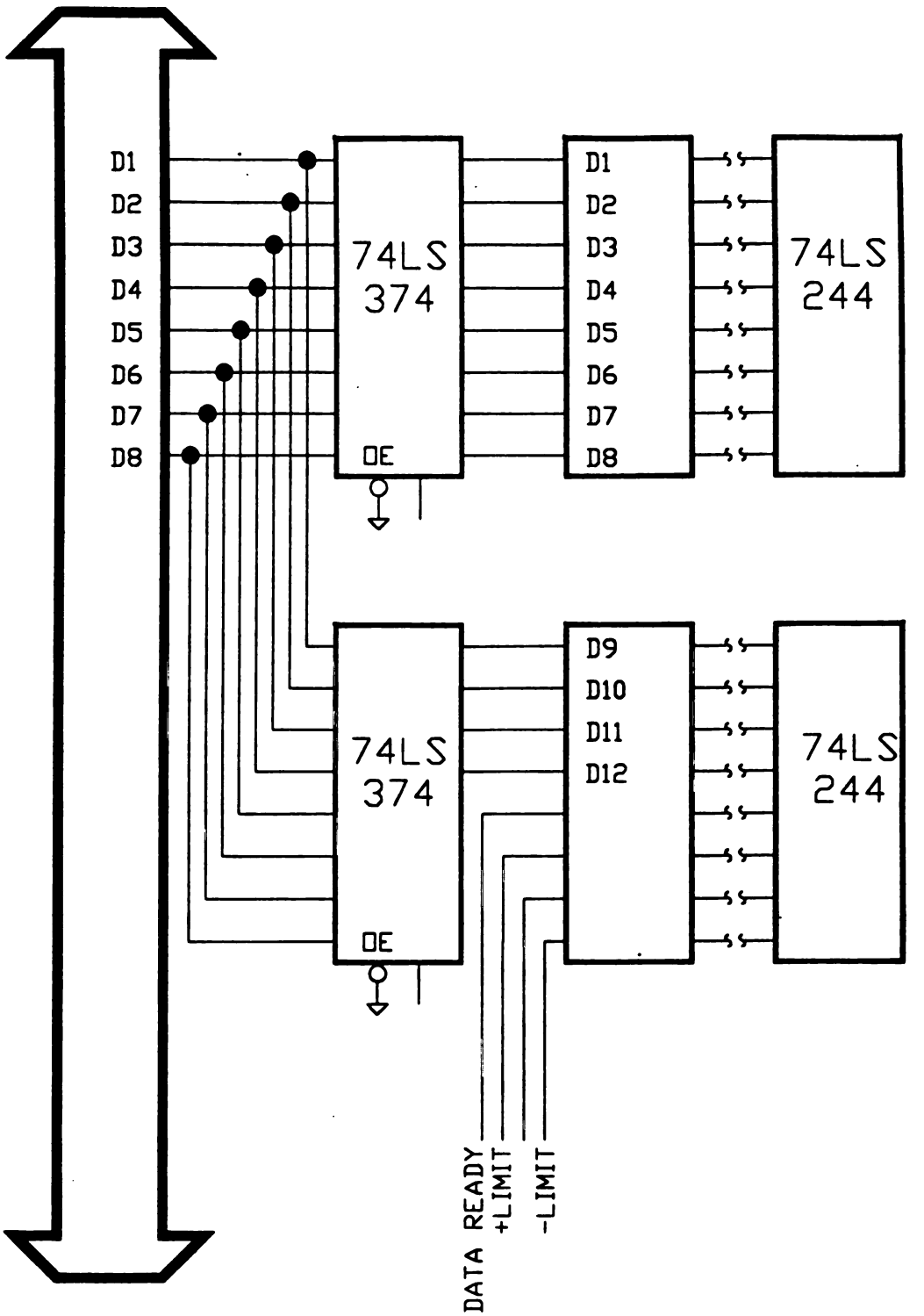


**Figure 3.11 Schematic of the twelve to eight bit multiplexer for the ADC.**

Furthermore, the data must be latched for later acquisition by the CPU. The schematic for this function is shown in Figure 3.11.

Timing for the potential step injector is generated by four counters on two Intel 8254 Programmable Interval Counter Timers and associated logic. The schematic for the timing and potential step control logic is shown in Figure 3.12 and the resulting timing diagram in Figure 3.13 A potential step is initiated by issuing the STEP command which writes the $F1C0_{16}$ onto the address bus. Counter 1 is programmed for mode 5, interrupt on terminal count, and delays the start of the step until the output of the REFDAC has settled to the desired voltage. A typical delay time for this counter is 4 μs which corresponds to a count of $14_{16}$. The STEP commands stops the maintenance injector and resets all other counters. After counter 1 generates an output pulse, counter 2 is triggered and generates a pulse which latches the output of the comparison circuit. One half clock cycle after the values are latched the control logic determines if a step injection pulse is needed. The determination is based on the value of the two control signal from the comparison circuit. If either signal is low, step charge injection is needed. This generates a pulse which sends the comparison circuit into hold mode and in turn triggers counter 3 to start counting. Counter three provides a delay while the charge is being injected into the cell by the potential step injector. When the counter reaches the end of count, counter 4 is started. The end of count from counter three also toggles a flip flop which reset counter 3 and prevents the charging voltage from being connected directly into the cell. Counter 4, provide the timing for the recharging of the step injector based on the difference voltage derived from the comparison circuit and a delay for the reference electrode to settle before the comparison circuit compares the cell with the reference DAC.

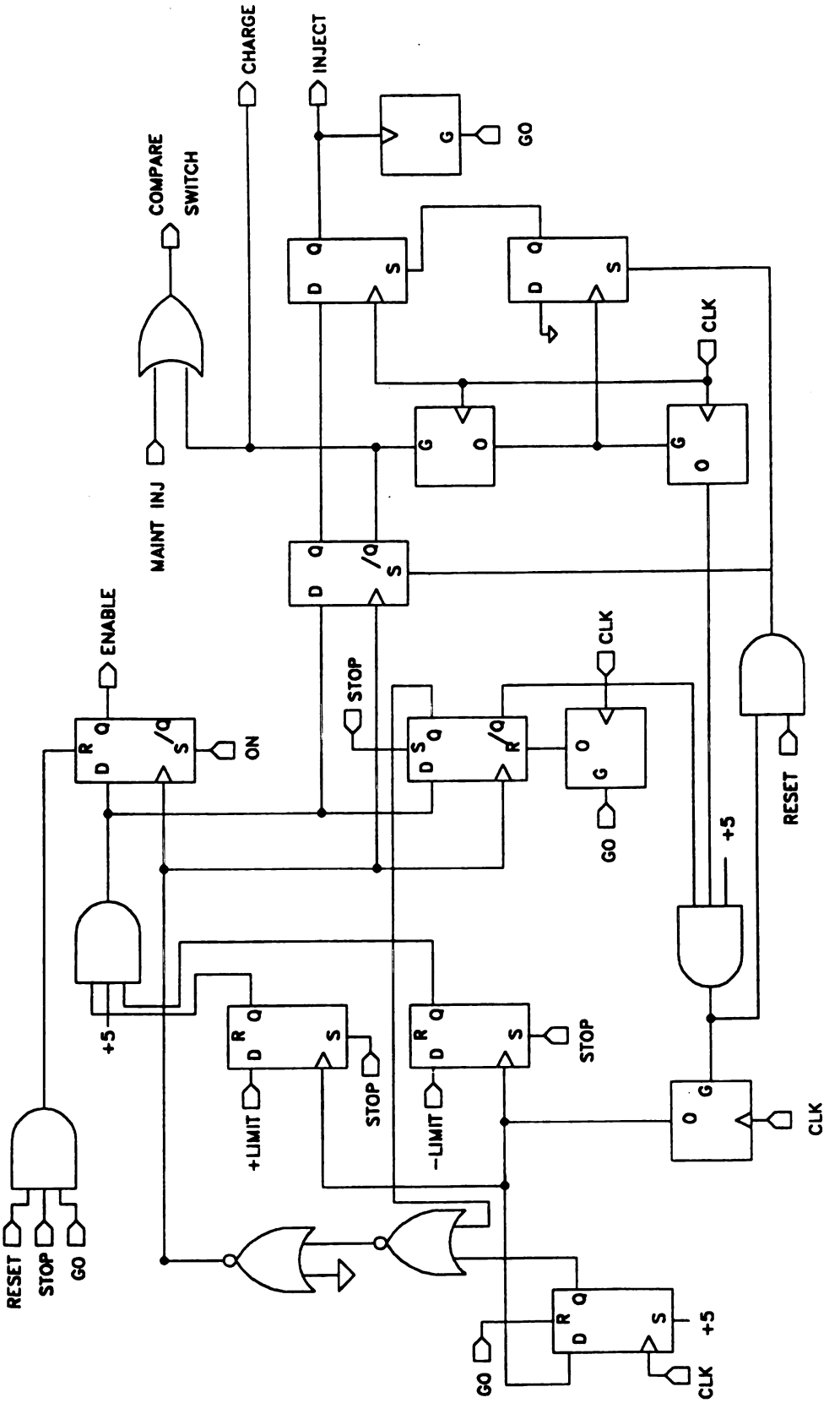


Figure 3.12 Schematic of the potential step injector control logic.

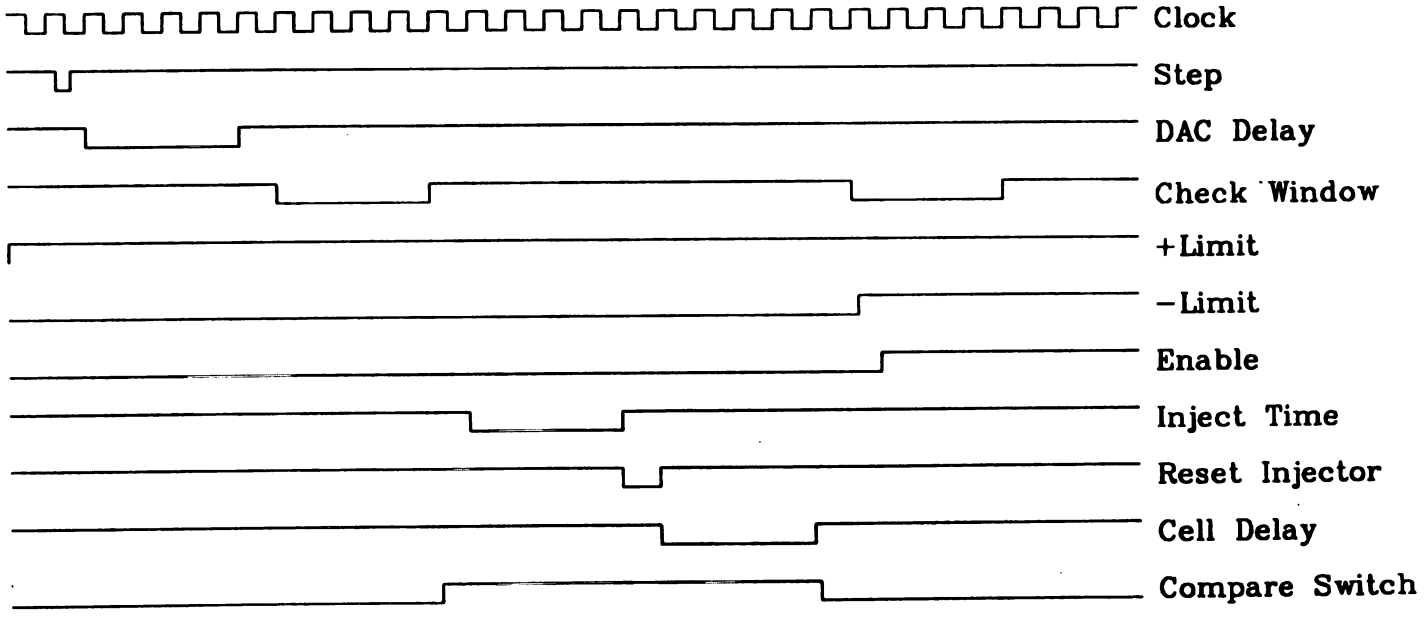


**Figure 3.13 Timing diagram of the potential step injector control logic.**

When both comparator outputs are true at the end of the delay time, ENABLE is generated. This signal stops the injection of charge by the potential step injector and activates the potential maintenance injector.

The timing of the maintenance injector is different from that of the step injector since smaller quantities of charge are injected thereby eliminating the need for a delay time between injection and comparison. The ENABLE signal also starts the timing of the potential step by counters 5 and 6. Counter 5 is programmed to be a divide by n counter, and its output is the clock input for counter 6. Counter 6 is programmed to be in mode 5 which generates an interrupt on terminal count. At terminal count the output of counter 6 goes LO which toggles a flip flop and generates the interrupt to the processor. This flip flop is necessary since the interrupt controller on the CPU is edge triggered but level sensitive. This means that the edge triggers the interrupt controller, but the level must be maintained until the computer acknowledges the interrupt. The interrupt is reset by the STEP command which starts the next step or by the end of the programmed waveform. The schematic for the maintenance injector control and timing logic is shown in Figure 3.14 and the timing diagram is shown in Figure 3.15. The logic for the injection counters is also shown in Figure 3.14.

The control of the analog to digital converter is designed to function under a variety of conditions. To achieve this flexibility the ADC control module is driven by a device select generated by the microcomputer. This limits the time during which an analog to digital conversion can occur, since the microcomputer has to be active. The schematic for this function is shown in Figure 3.16. The device select trigger a flip/flop which generates the hold pulse for the track and hold amplifier TH2. Additionally, the device select is inverted and used as the trigger for the ADC. The data ready signal

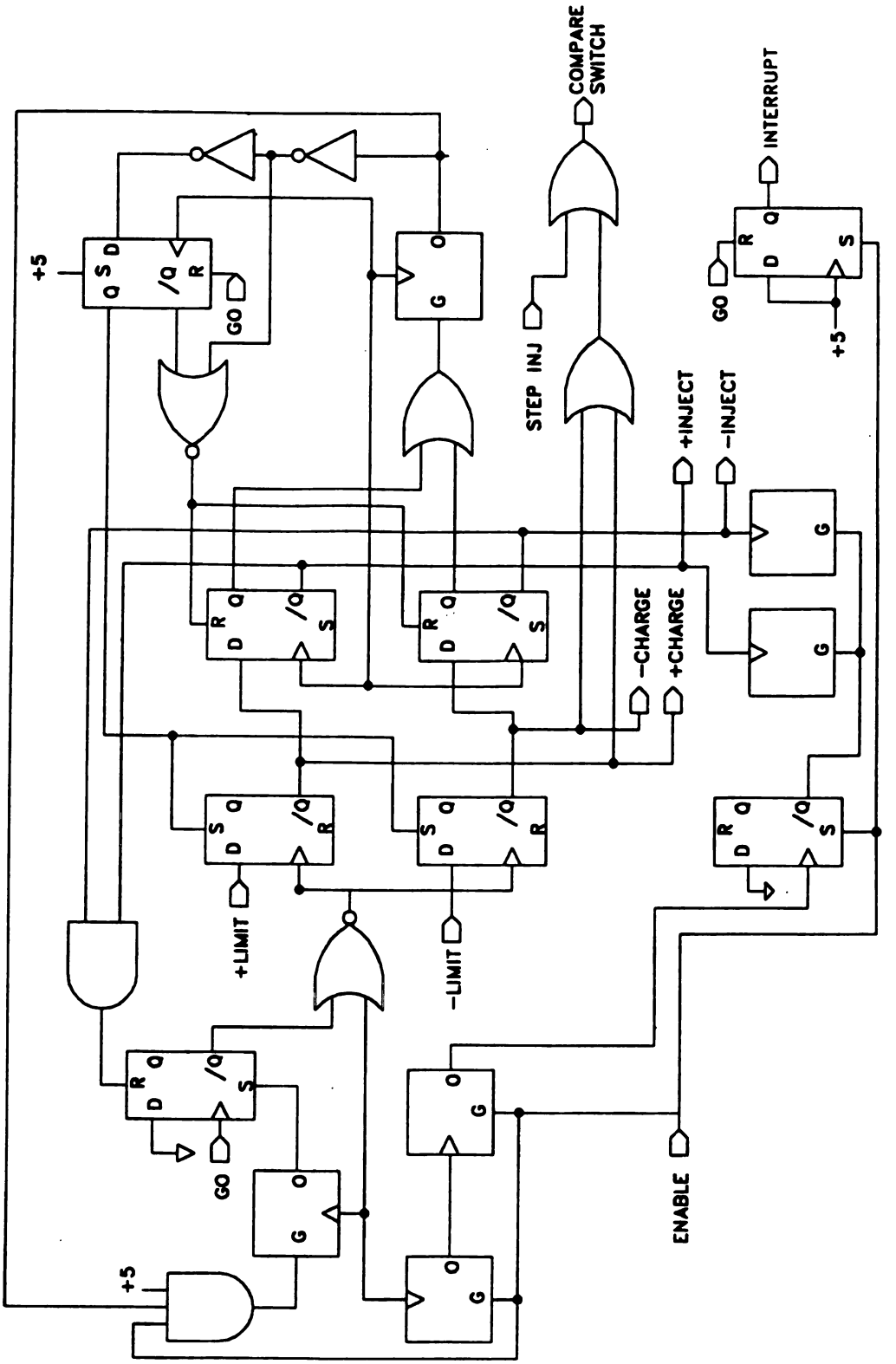


Figure 3.14 Schematic of the potential maintenance injector control logic, step timing logic, and the injection counters.

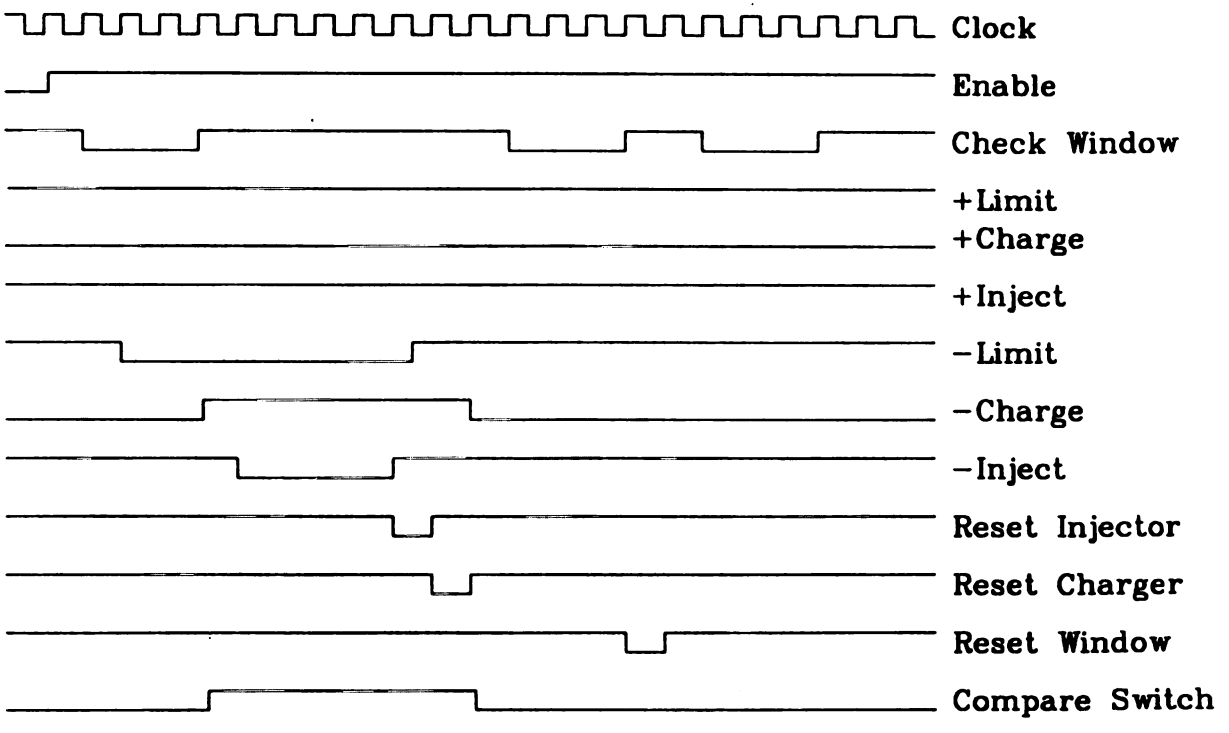


**Figure 3.15 Timing diagram of the potential maintenance injector control logic.**

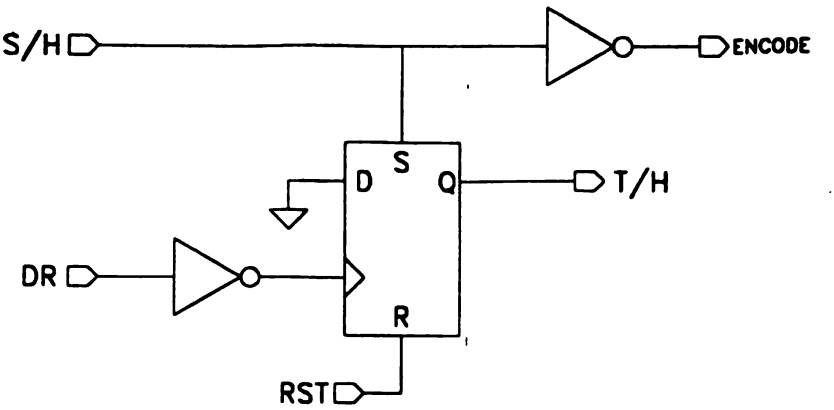


**Figure 3.16 Schematic of the ADC control logic.**

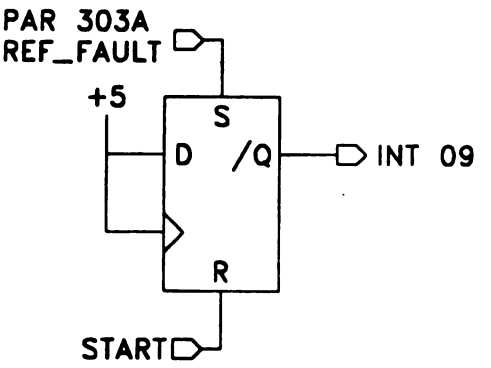


**Figure 3.17 Schematic of PAR 303A reference fault detection interface.**

generated by the ADC is used to latch the data into the data latches in the multiplexing function described earlier and also used to reset TH2 into the tracking mode. If the need arises for the ADC to function during a given experiment, the device select can be replaced by a hardware generated signal which would have the required timing. The only constraint is that only one conversion per step is allowed unless the microcomputer is capable of storing the data during the step.

Additional control circuitry is required when the polarizer is used with a PAR 303A. The additional functions which need to be controlled are the reference electrode fault sensing, the dislodge/dispense cycle for the mercury drop, and the nitrogen purge. Figures 3.17, 3.18, and 3.19 respectively are the schematics for these additional control functions. Fortunately, in cyclic voltammetry the only function which needs to be active during a voltammetric run is reference fault sensing, and this function serves as an error condition to the microprocessor. The reference fault signal occurs when the reference electrode potential exceeds ± 4.5 V. When the reference fault signal goes HI, a flip/flop is triggered which generates an interrupt to the processor. This interrupt stops the charge injectors and returns the system to go to open circuit. In addition, the processor activates a task which notifies the user that an error has occurred.

The dislodge/dispense and purge control functions can occur only when the microprocessor is active, thus eliminating additional timing logic. A dislodge/dispense sequence for the SMDE is initiated by writing an $F1CC_{16}$ on the CPU bus. This address is decoded and triggers a one-shot monostable multivibrator. The output pulse of the monostable is logic 0 for 50 μs. This pulse initiates the dislodge/dispense sequence which is part of the PAR 303A. To perform experiments which employ a DME the necessary software could

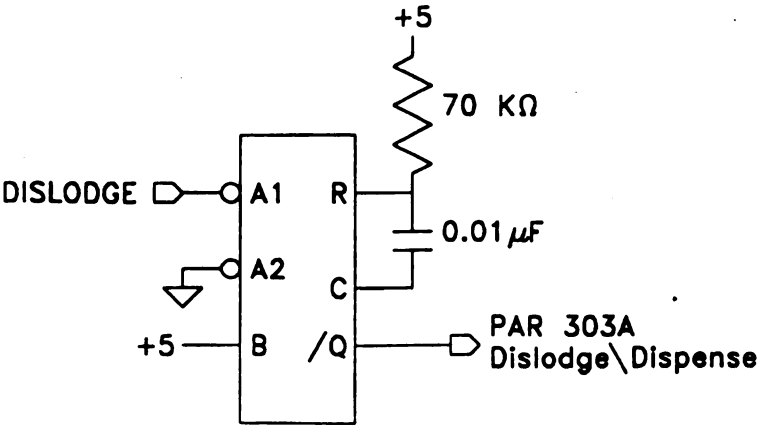


Figure 3.18 Schematic of Par 303A dislodge/dispense control interface.

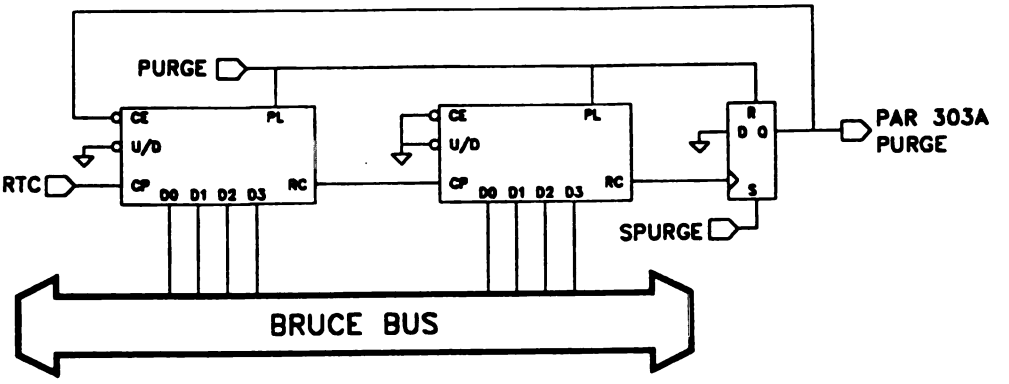


Figure 3.19 Schematic of PAR 303A $N_2$ purge interface.

be incorporated into the interrupt handler and a new drop A dislodge/dispense sequence for the SMDE is initiated by writing an $F1CC_{16}$ on the CPU bus. This address is decoded and triggers a one-shot monostable multivibrator. The output pulse of the monostable is logic 0 for 50 μs. This pulse initiates the dislodge/dispense sequence which is part of the PAR 303A. To perform experiments which employ a DME the necessary software could be incorporated into the interrupt handler and a new drop could be dispensed between steps. In addition, timing of other parameters would need to be adjusted to account for the drop growth since the PAR requires a maximum of 250 ms for a large drop to form.

Purging the cell with nitrogen is easily controlled by the microprocessor since this function can only occur between experiments when the processor is active. The purge valve is always either purging the solution by bubbling $N_2$ through the cell or providing a positive atmosphere of $N_2$ over the solution in the cell. Timing of the purge cycle is accomplished by using the Real Time Clock module on the CPU bus programmed to generate output pulses at 1 second intervals. These clock pulses are then counted by an asynchronous ripple counter constructed of two 74LS190 decade up/down counters. The ripple count output of the second counter provides a clock pulse to the D flip/flop, 74LS74 which disables the counter and stops bubbling $N_2$ through the solution. To purge the cell, a simple write to the appropriate hardware device select activates the solution purging cycle. The purging will continue until the counter reaches terminal count, and then the valve is switched such that a flow of $N_2$ is maintaining an inert atmosphere above the cell. The purge cycle can also be terminated by software. This is accomplished by writing the appropriate device select address on to the CPU bus.

**Software**

The software for the collection and subsequent analysis is divided into two distinct categories. The microprocessor acquires and controls the polarizer using programs written in the language polyFORTH (17). Data analysis and reduction occur in an IBM AT by programs written in C which runs under PC DOS.

FORTH is a multi-level language and operating system which is used exclusively on the microprocessor (17,18,19). FORTH is characterized by four major elements: the dictionary, the stack, the interpreter, and the assembler. The dictionary occupies most of the memory space. It is a list of 'words', each of which is a program which can include any other dictionary entry. New entries can easily be added to the dictionary which makes FORTH an extensible and versatile language. One minor fault with FORTH is that already defined words can be redefined thereby changing the effect of all subsequent words that include that word in their definition. For this reason extreme care must be used in naming new words.

Four separate dictionaries are maintained, and each can contain functions of the same name, but with drastically different meanings. Two push-down stacks are also maintained. The first, the parameter stack, provides an efficient mechanism for transferring numbers from one word to another. The second stack, the return stack, is used for internal flow from word to word. This stack can also be used as temporary storage; however, extreme caution must be used to restore this stack before another word is called.

If the return stack is changed, the system will crash and all data is lost. FORTH is fundamentally an interpretive language. Two interpreters

are available. One works in the usual manner, simply passing text strings and looking up each word in the dictionary; the other interprets strings of absolute memory addresses by executing words which contain addresses of the next word. This threading provides for a faster execution speed as each word does not have to be located as in a conventional interpreter. FORTH also includes an assembler, which allows the user to define words on the assembly language level for even greater execution speed. Such words are necessary for low level control and interrupt driven devices.

FORTH was chosen for this application for many reasons. It is a very compact language/operating system using only 8 Kbytes of memory for the kernel. FORTH is extensible, a great advantage when software modifications are required due to changing experiments or hardware modifications. FORTH is highly portable. FORTH is relatively fast and efficient. Well-written FORTH programs compare favorably with software written strictly in machine-language (about 85 %). Since FORTH is extensible, it can grow to a high-level language. Programming productivity is much greater than machine-language, and yet overall speed is not reduced as in other high-level languages such as FORTRAN or C.

In addition to the basic defining words supplied with FORTH, additional words have been added to the dictionary which control the polarizer and perform disk access. As an example, a listing of five words involved in storing data to the disk in a binary format follows:

```
VARIABLE !BLOCK
: SBUFFER 6 6 PREV DUP 2+ ROT SWAP ! ! ;
: N_BYTES ( -> # bytes) B000 @ 2 * 1 + 0D * 40 + ;
: N_BLKS ( - # blocks) N_BYTES 400 /MOD SWAP 0> IF DROP 1+ THEN ;
: STORE>DISK ( -> # blocks) N_BLKS DUP 4 SWAP - 0> IF DROP 0 DO
    SBUFFER I !BLOCK @ + I 2* 4 + PREV + ! LOOP !BLOCK @ +
    !BLOCK ! FLUSH THEN ;
```

The first word !BLOCK is a variable definition. When a variable definition is called the address of the variable is placed on the top of the stack. This allows any following word to read or alter the contents of !BLOCK directly. SBUFFER stores the value 6 at the memory location pointed to by the system variable PREV and again at the memory location of PREV + 2 using the FORTH definition "!". This word initializes the disk buffers so that the next available buffer starts at B000. N_BYTES reads the contents of $B000_{16}$ with the @ definition and multiplies the value by 2, adds 1, multiplies by $0D_{16}$, and adds $40_{16}$. N_BLKS executes N_BYTES which returns to the top of the stack the number of data points stored during the experiment. The number of bytes returned by N_BYTES is divided by 400 using the command /MOD which returns the integer divisor on the top of the stack with the remainder below it. SWAP changes the order of the stack such that the remainder is now on the top. The statement 0> IF performs a conditional jump to the THEN statement if the tested value is false. If the tested value is true, the number is removed from the stack by the FORTH definition DROP and 1 is added to the divisor. STORE>DISK is the only routine that would normally be typed by the operator. It uses N_BLKS to determine the number of blocks used and checks to see if less than four disk buffers were used. If the condition is true, a loop is entered which stores the

disk buffers to the disk block pointed to by the address in !BLOCK. This loop continues until the disk buffers which were used for the data acquisition are written to disk.

Since the time required to store a given buffer is considerably longer than the time required to perform the experiment, we are limited to the four disk buffers in which to store all acquired data. This has not been a problem since each buffer can contain 2 Kbytes of information. Table 3.2 is a listing of the most frequently used and highest level words written for the operation of the polarizer along with their functions. The most intricate word developed is the interrupt service routine which reactivates the processor and starts a new step. Appendix A.1 is a complete listing of all FORTH code required to run the polarizer.

Since FORTH is integer based and the use of the floating point kernel is extremely cumbersome, the data are uploaded to an IBM AT via a serial connection. A switch box is used to switch the serial line between the terminal and the IBM computer. The data are logged to the fixed disk of the IBM computer by using a terminal emulation package named EM, copyrighted by Diversified Computer Systems. The data are sent to the IBM computer in ASCII format.

Once the data have been transferred to the IBM computer, data reduction can occur. These routines are written in Microsoft© C and run on the IBM AT. The data reduction routines read the header, the first 64 bytes, to determine the various parameters of the experiment. The data are then read in, point by point, converted to real values and stored in a file with a name which is contained in the first word of the comment field of the header. Since each experiment has a unique data file, each method has a separate

TABLE 3.2. Table of FORTH words and their function.

| | |
|---|---|
| DISK_STATUS | Shows the status of the disk buffers. |
| NRAMP | Calculates the REFDAC values for a ramp which initially scans in the negative direction. |
| PRAMP | Calculates the REFDAC values for a ramp which initially scans in the positive direction. |
| SETUP_COUNTERS | Writes the control word to th counters. |
| LOAD_COUNTERS | Writes the timing data to the counters. |
| ARM_INT | Arms the interrupt controller. |
| SAVE-INT-MASK | Saves the interrupt controller status. |
| ADC_VOLTS | Converts the ADC value into a voltage using the math coprocessor. |
| INTR8 | Interrupt routine which reactivates the processor, stores the data, and updates REFDAC. |
| INTR9 | Interrupt routine which reactivates the processor, returns the cell to open circuit, and issues an error message to the operator. |
| CV | Highest level word which clears the buffers, writes the data header, sets up the scan, starts the first step, and upon completion of scan stores the data to disk. |

routine to read the data in and calculate the charge used to maintain the step and the control voltage for each step. The exact equations used to calculate the charge are given in later chapters. The reduced data are then passed to PLOT, a device independent plotting routine written by Drake Deidrich (20) and myself which plots the output on either the monitor, the plotter, or the Postscript© compatible printer. Appendix A.2 is a complete listing of all programs written in C for use with the polarizer. A brief explanation of the individual functions is included with the program listings.

# CHAPTER 4

## CALIBRATION OF THE CHARGE-PULSE POLARIZER

Careful calibration of the polarizer is essential to accurate performance of the instrument. However, once completed, the calibration need only be checked periodically to insure proper operation. The calibration of the polarizer includes balancing of the analog circuitry and the adjustment and characterization of the charge injectors. This chapter will detail the analog adjustments chronologically starting with the operational amplifiers, track and hold amplifiers, digital to analog convertors and the comparison circuitry. Once the analog circuitry is balanced the leakage current can be measured and the total charge injected by the maintenance charge injectors can be calibrated.

### ANALOG DEVICE CALIBRATION

Particularly crucial among the analog adjustments are those in the comparison circuit where the cell potential is being monitored and the reference potential and the control window are generated. The need for such precise calibration is that during a given experiment, the system never makes an analog to digital conversion; the control system accuracy is based on the assumption that the comparison circuit is accurately comparing the current cell potential with the desired setpoint potential. However, before the comparison circuit can be trimmed, several other analog devices must be

balanced. The current to voltage convertors OA2 and OA7 ( see Figures 3.4) at the outputs of the REFDAC and INJDAC, respectively, are the first devices to be balanced. The gain on the feedback loop of the amplifier is temporarily increased by placing a 1 MΩ resistor in the feedback loop and a 10 kΩ resistor at the inverting input. The inverting input of the operational amplifiers is disconnected from the DACs and grounded. The output of the amplifiers is then balanced by adjusting the balance potentiometers which are associated with the operational amplifiers. The cell amplifier OA10 was also balanced in this manner. The voltage followers OA1, OA9, OA12 and OA13 (see Figure 3.3, 3.4, 3.5, 3.6) are adjusted by disconnecting the non-inverting input and connecting it to circuit common. The gain of the voltage followers is then temporarily increased by putting a 1 MΩ resistor between the amplifier output and the inverting input and a 10 kΩ resistor from the inverting input to circuit common. As with the other amplifiers, the output is then balanced to 0.0000 V by adjusting the balance potentiometer. Once the operational amplifiers are balanced, the remainder of the analog devices can be trimmed.

The following order for calibration is important since it provides a means whereby the system is self-consistent. The first functionality to be trimmed is REFDAC. The digital inputs to REFDAC are set to all zeros by the microprocessor, and the zero adjust potentiometer is adjusted until the output is -2.500 V. The microcomputer then sets the digital inputs to all ones, and the gain adjust potentiometer is adjusted until the output voltage reads +2.4988 volts on a digital multimeter. This process is repeated until no further adjustments are needed. A linearity check may be made by incrementing the digital inputs from zero to full scale and recording the

output at each step. Once calibrated, REFDAC is used to generate all other calibration voltages used. INJDAC is adjusted by the same procedure.

The track and hold amplifiers TH1 and TH2 (see Figures 3.3 and 3.6), are balanced by disconnecting their analog inputs and connecting them to system common. In addition, the track/hold inputs are disconnected from the microcomputer and connected to a function generator. The function generator is set to generate a TTL square wave at a frequency of 200 KHz. While TH1 and TH2 are being gated by the frequency generator, the pedestal offset is adjusted to 0.000 V by the offset adjust potentiometers. By using this procedure, the pedestal offset can be trimmed while preventing the droop rate of 5 mV $sec^{-1}$ from affecting the results.

The output of REFDAC is then connected to the TH1 input, and the ADC encode signal is connected to the function generator (see Figure 3.6). As in the prior procedure, the function generator is set to generate a 200 KHz TTL square wave. The output from the ADC is displayed on a logic analyzer, and the offset adjust potentiometer is adjusted until the output flickered equally between 111111111111 and 111111111110 for a REFDAC input of +2.500 V. The output of REFDAC is then set to -2.500 V, and the full scale adjust potentiometer is adjusted until the display flickers between 000000000000 and 000000000001.

The next circuit to be balanced is the voltage divider network which is part of the comparison circuit (see Figure 3.3). This must be done very carefully. For this procedure an externally balanced summing amplifier with a gain of exactly -1.0000 is used to generate a voltage of equal magnitude but opposite sign of the REFDAC output. The REFDAC output is connected to the buffer amplifier OA4, and the inverted output is connected to the reference input buffer OA5. The network is then balanced by adjusting the

trim potentiometer, R5, so that the output of OA4 is 0.0000 V. The balance of the voltage divider network is then checked by changing the value of REFDAC and verifying that the output voltage remains 0.0000 V. This is an extremely accurate test of the balance since the output voltage will vary as a function of the input voltage if the two inputs are not equal in magnitude but opposite in sign. For example, if the divider is balanced with one input at 1.000 V and the other input at -0.995 V, the balance point for R5 will be at 224.3 Ω. If each input voltage is then increased by 1.000 V, the new balance point would be at 237.1 Ω. The voltage error caused by this difference would be -24.95 mV at the input to OA4.

The voltage comparators ( see Figure 3.3) are balanced by connecting the inverting and the non inverting inputs to the circuit common, and the balance potentiometers are adjusted until the comparators are on the verge of oscillation. Complete balancing of the comparators is not necessary since the circuit design uses the internal hysteresis as a means of stabilizing the response of the comparators.

Finally, the window voltage (see Figure 3.3) is adjusted to the desired value by using a digital multimeter to measure the output voltages of the window generating voltage divider as R18 is adjusted. For this work, the window voltage was adjusted to ±2.5 mV.

## CALIBRATION OF THE MAINTENANCE INJECTORS

In order to know accurately the amounts of charge injected, it is necessary to know the leakage current through the injection switches, the capacitance of the charge injectors, and the amount of charge injected each time the switches are activated. Precision capacitors could be used; however, they are very expensive and would still require calibration to insure the

capacitance from the circuitry would be accounted for in the total capacitance of the injector. To avoid buying several precision capacitors which would need recalibration, capacitors with relatively high tolerances which are stable with respect to changes in frequency and temperature can be standardized to the necessary precision.

Before the injection capacitance can be calibrated, the leakage current from the injection switches must be determined. This current is due to the finite off resistance of the analog switch and from the input offset current of the cell operational amplifier. To determine the overall leakage current of the injection system, it is necessary to insert a known capacitor in the feedback loop of the cell amplifier, as shown in Figure 4.1. In this configuration, the cell amplifier is configured as an integrator where the output voltage is related to the input voltage by equation 4.1.

$$V_{out} = \frac{-1}{C_f} \int i \, dt \qquad (4.1)$$

A jumper wire is used to short out the feedback loop, such that the initial voltage is 0.000 V. By measuring Vout as a function of time, the leakage current can be obtained. A linear regression of equation 4.1 should yield a line with an intercept through the origin if the integrator is started at 0.000 V.

Experimental data for four different known feedback capacitors are shown in Figures 4.2 through 4.5. The results from fitting the data to equation 4.1 yielded a leakage current of -12.2 ± 0.1 pA with a coefficient of correlation of 1.00 for each of the feedback capacitors. However, the data did not go through the origin as expected. The offset in the data was due to the

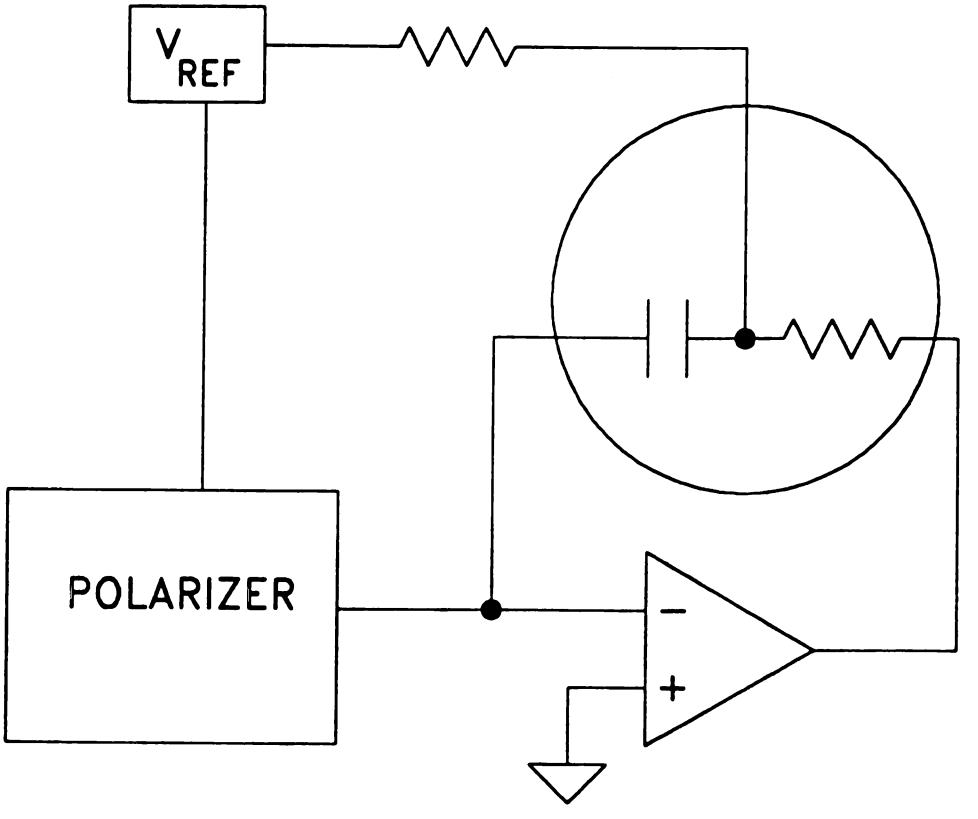


**Figure 4.1 Calibration circuit using a precision capacitor.**

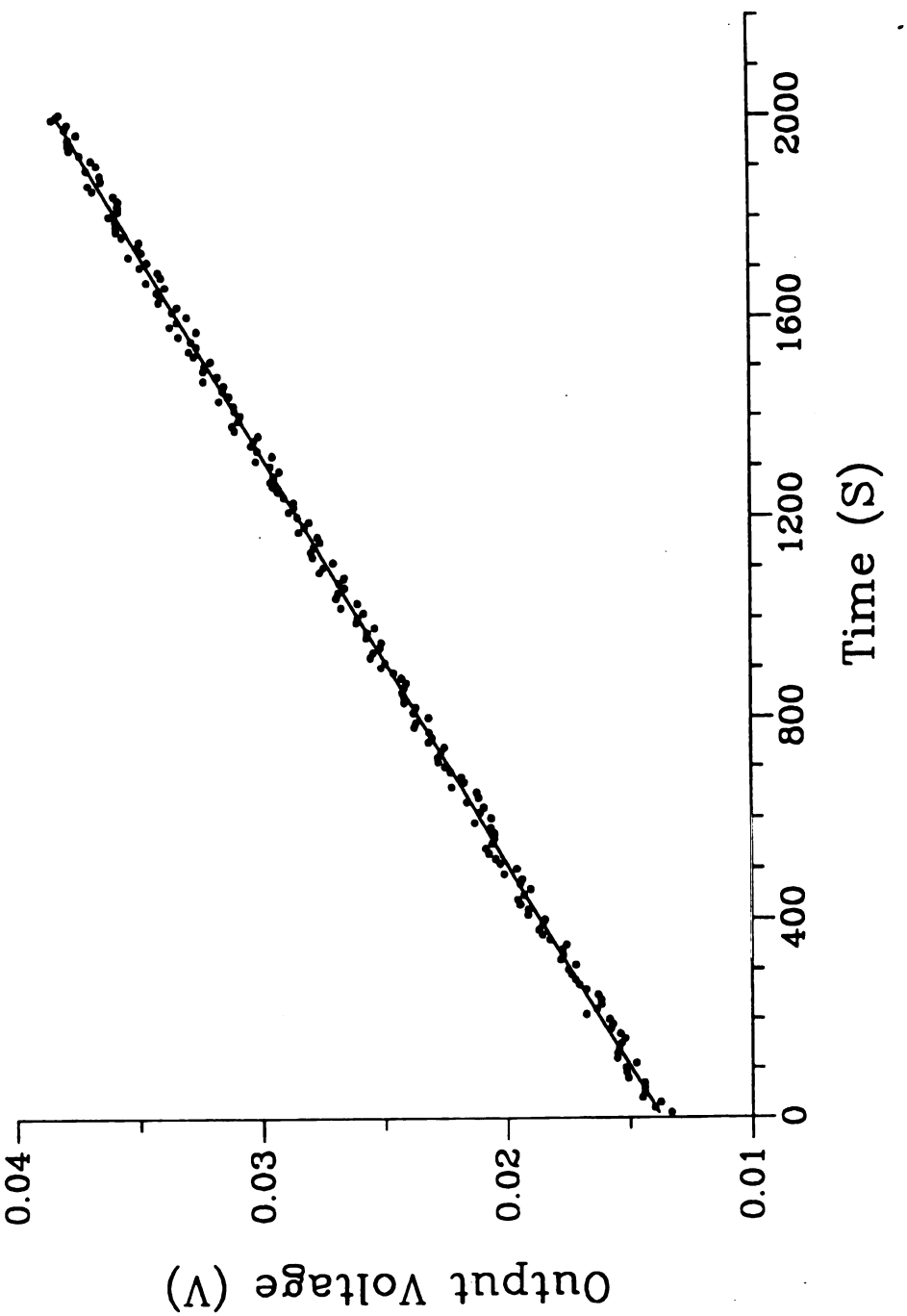


**Figure 4.2** Calibration of the leakage current represented by the slope of potential versus time for a 0.985 µF capacitor.

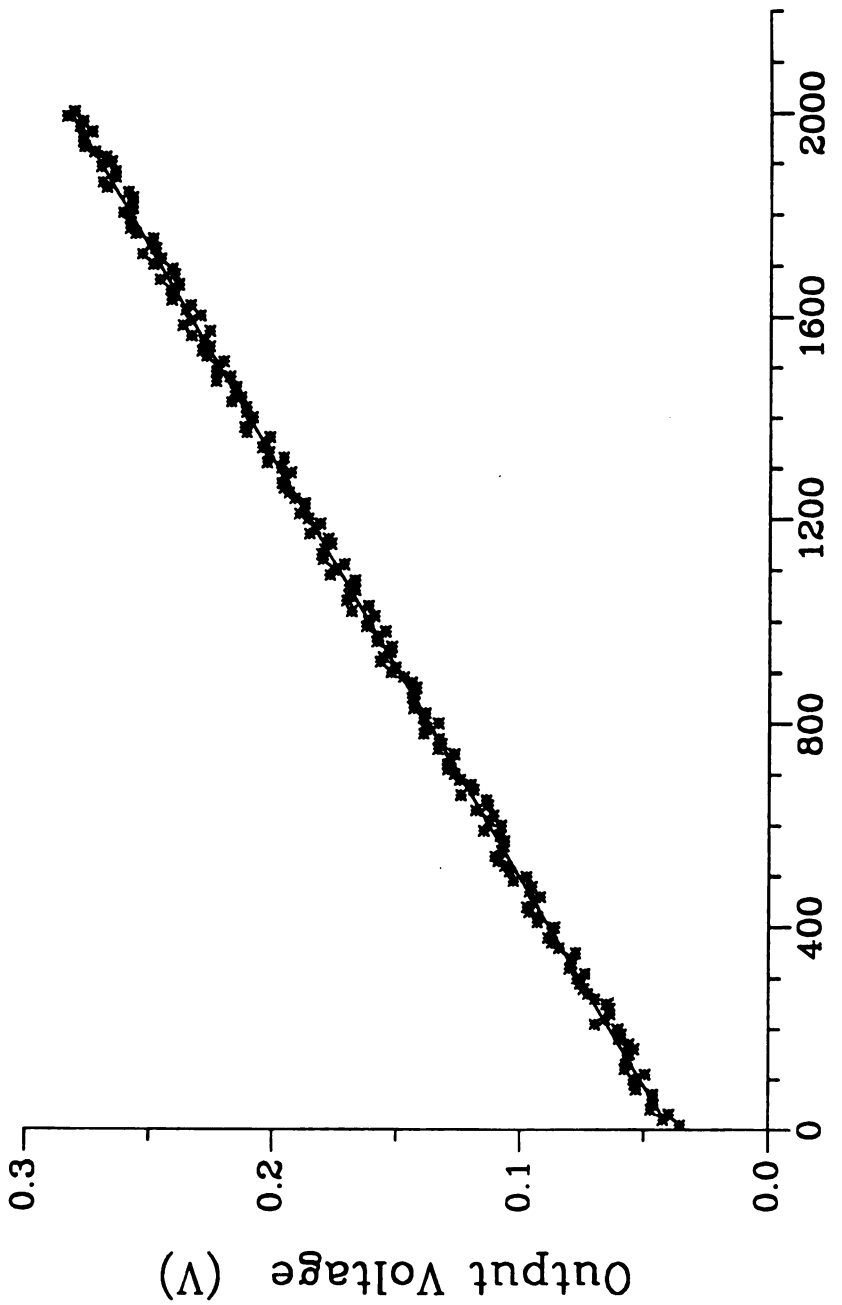


**Figure 4.3** Calibration of the leakage current represented by the slope of potential versus time for a 0.0997 μF capacitor.

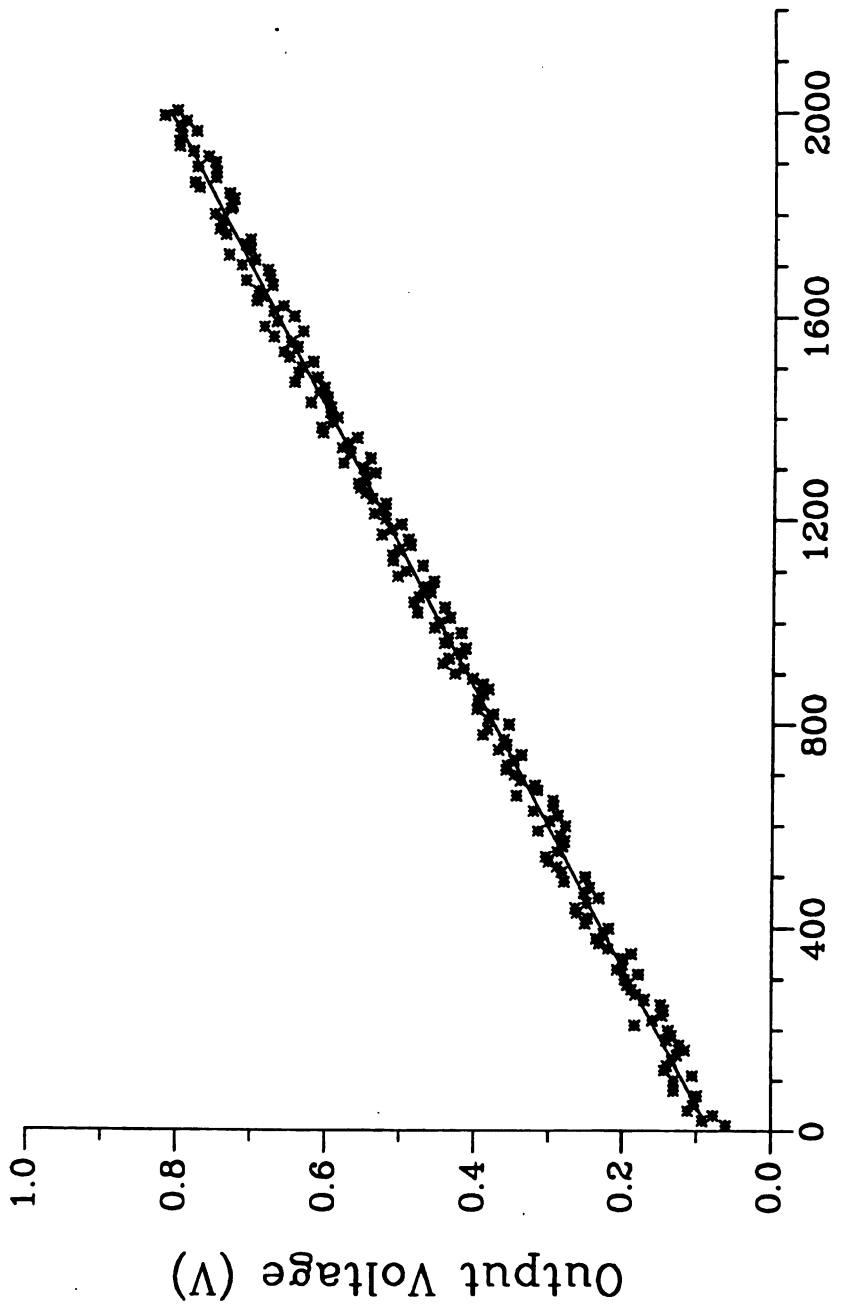


**Figure 4.4** Calibration of the leakage current represented by the slope of potential versus time for a 0.0332 μF capacitor.

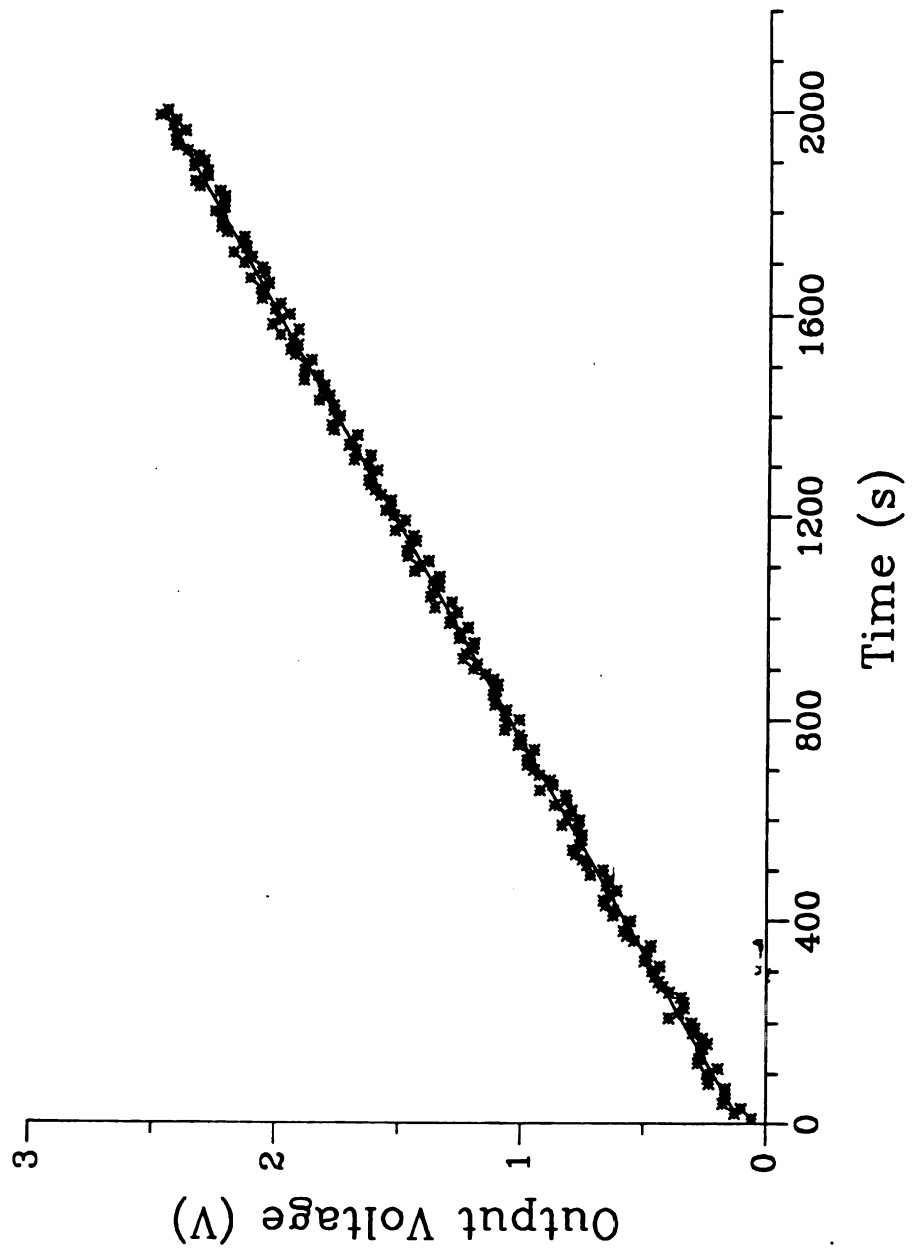


Figure 4.5 Calibration of the leakage current represented by the slope of potential versus time for a 0.0102 μF capacitor.

injection of stray charge caused by removing the jumper wire. An attempt to use a switch instead of a jumper wire failed since the switch increased the measured leakage current.

Once the leakage current has been measured, the calibration of the total injector capacitance and the charge injected by the switch can be performed. The same integrator configuration used for the leakage current measurement can be used to calibrate the maintenance charge injectors. The calibration procedure consists of using the maintenance injectors to step the voltage of the integrator capacitor a known amount. This is accomplished by setting the DAC_DELAY counter to a large value and issuing the STEP command followed immediately by STOP and MAINT_ON. Using this procedure, the setpoint potential is updated through the STEP command; however, the potential step injector is prevented from injecting charge. The maintenance injectors are then started and the potential is stepped to the setpoint potential by the maintenance injectors. The number of injections needed to step the potential a known amount is recorded. This procedure is repeated for a range of charging voltages for both the positive and negative injectors. The injector capacitance and charge injected by the switch are then calculated from equation 4.2.

$$Q_{out} = (V_{inj}\, C_{inj}\, N_{inj}) + (Q_{sw}\, N_{inj}) + (i_{leak}\, t) \qquad (4.2)$$

The quantity $V_{inj}$ is the voltage to which the injection capacitor is charged, $C_{inj}$ is the unknown capacitance of the charge injector, $N_{inj}$ is the number of injections needed to step $V_{out}$ from the initial voltage to the setpoint, $Q_{sw}$ is the charge injected by the switch when the charge driver changes state, and $i_{leak}$ is the value determine previously. The quantity $Q_{out}$ is obtained by

multiplying $V_{out}$ by the feedback capacitance $C_f$. Equation 4.2 is based on four assumptions: 1) the charge on the injection capacitors is transferred quantitatively to the feedback capacitor; 2) only one charge injector is used; 3) the leakage current is known; 4) the capacitance of the feedback capacitor is known precisely. A plot of $(Q_{out} - i_{leak}t)/N_{inj}$ versus $V_{inj}$ should yield calibration curves which are linear where the slope is equal to the $C_{inj}$ and the intercept is $Q_{sw}$.

The results of this calibration procedure where the charging voltage ranged from 1.250 to 0.400 V are shown in Figures 4.6 and 4.7. The integrator feedback capacitance was independently measured to be 0.985 μF and the injector capacitor had a nominal value of 1000 pF. Linear regression of these curves yielded injection capacitances of 1054 pF and 1056 pF and switch charges of -36.3 pC and 20.3 pC for the positive and negative injectors, respectively.

An alternative method of calibration which eliminates the need for a known capacitor in the feedback loop can be used. The feedback loop for this calibration procedure consists of a resistor and capacitor in series and a precision resistor in parallel with the capacitor as shown in Figure 4.8. This circuit forms the classical cell equivalent circuit for a three electrode cell (21). In this configuration, the precision resistor provides a constant load on the feedback capacitor. In order to maintain the potential, the polarizer must replace the charge which is depleted from the capacitor by the precision resistor. This is accomplished by using the maintenance injectors to inject equal sized charge injections at a variable rate so that the potential of the feedback capacitor is maintained to within ±1 mV of the setpoint potential. If the voltage on the feedback capacitor, $V_{out}$, is considered to be constant, the value for $Q_{out}$ is given by equation 4.3.

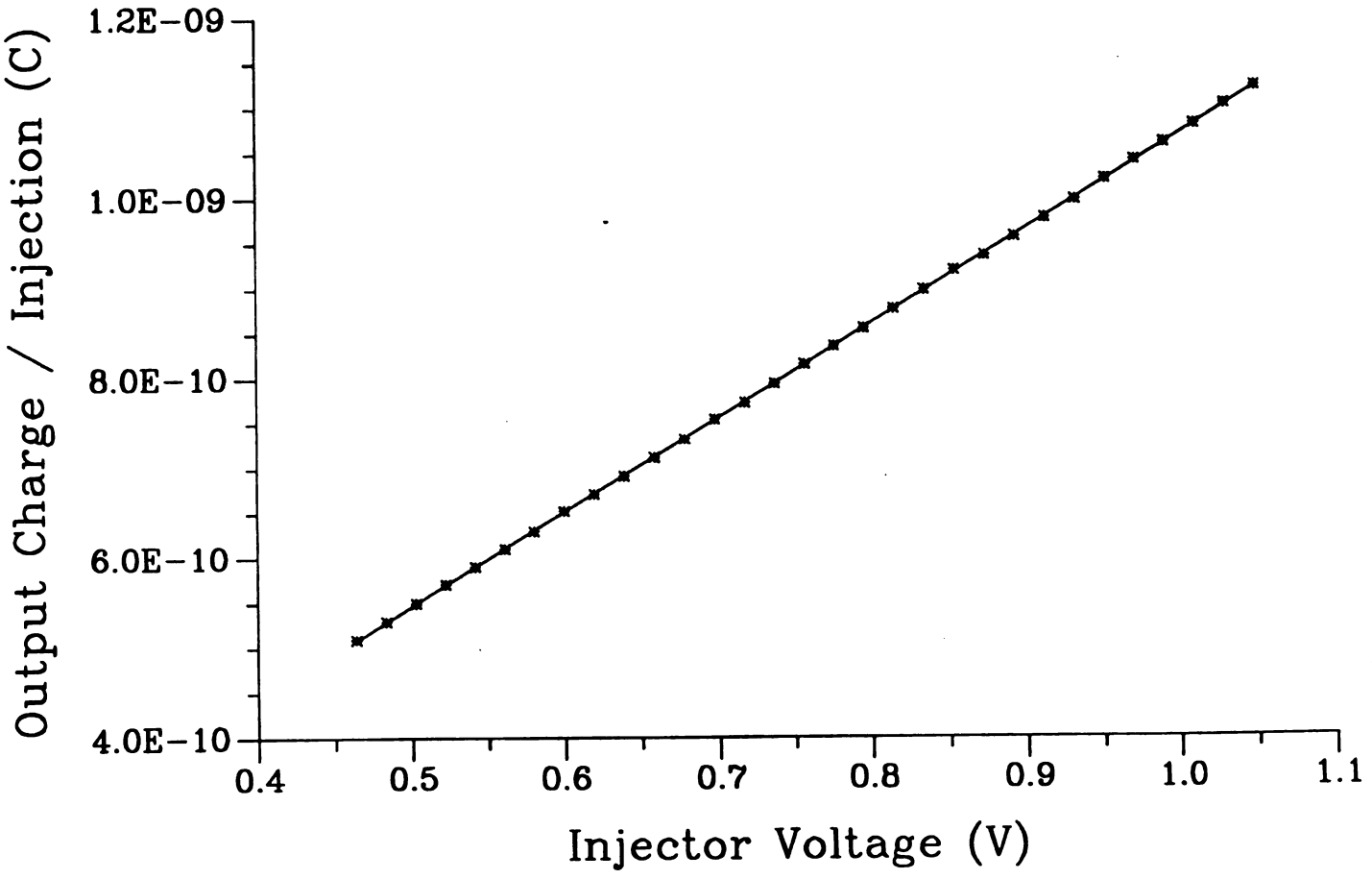


**Figure 4.6** **Calibration curve for the positive potential maintenance injector using the integrator feedback configuration with a 0.985 μF capacitor.**

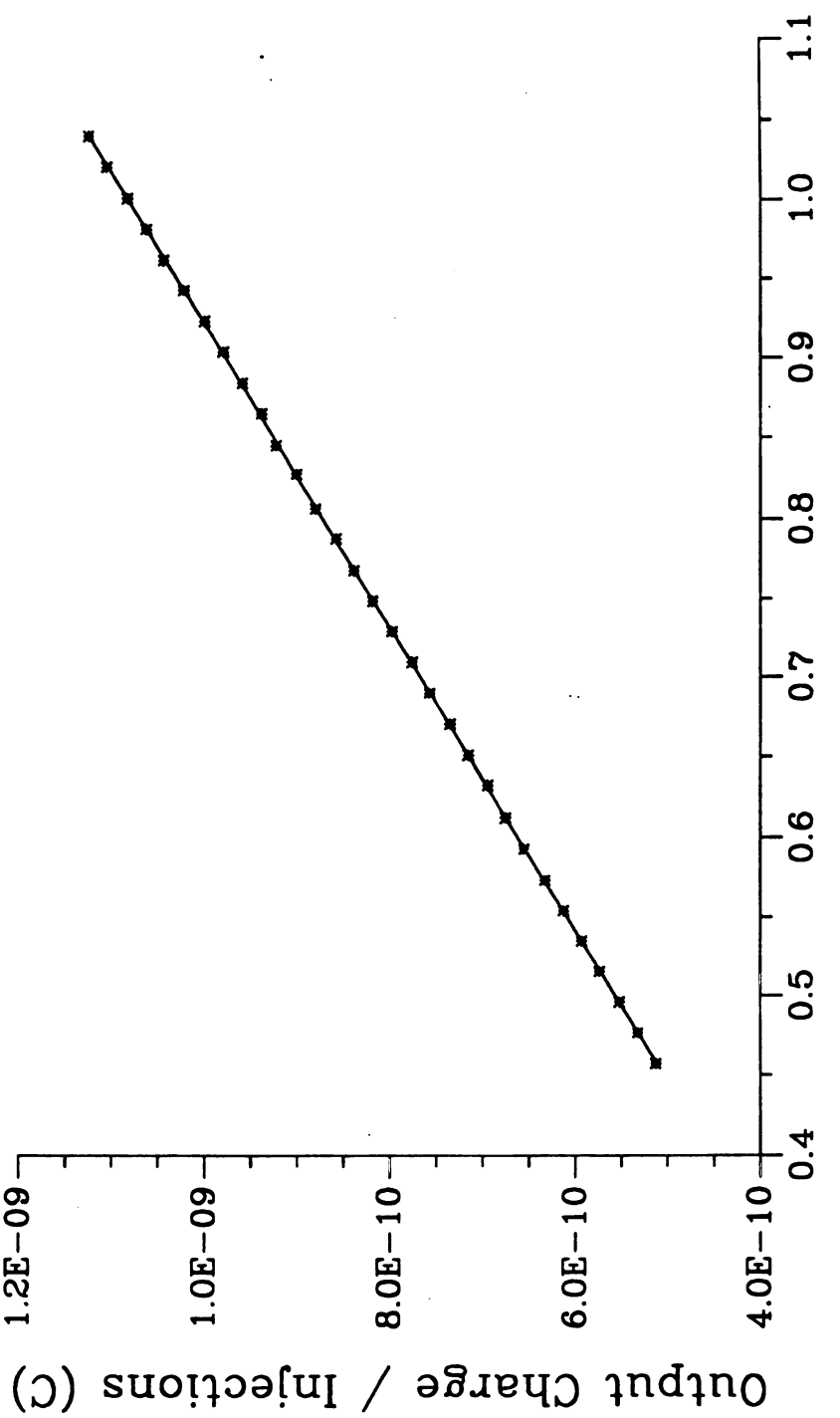


**Figure 4.7** Calibration curve for the negative potential maintenance injector using the integrator feedback configuration with a 0.985 µF capacitor.

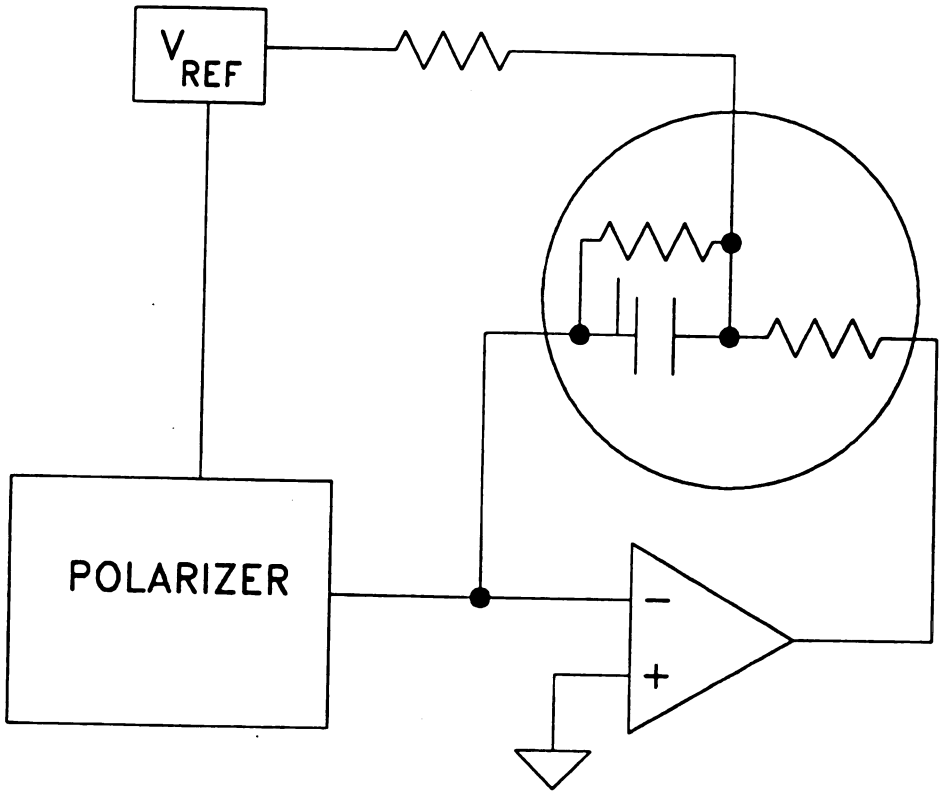


**Figure 4.8** Calibration circuit using a cell equivalent circuit with a precision resistor in the feedback loop of the control amplifier.

$$Q_{out} = V_{out}\, t_{step} / R_f \qquad (4.3)$$

The quantity $R_f$ is the precision resistor in the feedback loop, $t_{step}$ is the time duration of the potential step, and $V_{out}$ and $Q_{out}$ are the same as in the previous equations. The quantity $Q_{out}$ is then used in equation 4.2. This procedure is repeated for several charging voltages and the resulting data plotted. A linear least squares fit of the data provide the values of $C_{inj}$ and $Q_{sw}$ for the charge injectors..

Two benefits of this method are that the same control software used in a typical voltammetric experiment can be used in the calibration procedure, and the need of a precision capacitor is eliminated. Instead of a precision capacitor, a precision resistor which is less expensive and more readily available can be used for the calibration procedure. Since resistance is an more easily measured than capacitance, the result from this calibration procedure should provide a more accurate means of measuring the amount of charge per injection.

The calibration curves obtained by this procedure are shown in Figures 4.9 and 4.10 for the positive and negative injectors, respectively. The values for the feedback capacitor and load resistor were 0.985 μF and 464 kΩ, respectively. The setpoint potential was maintained for 65,536 μs. The results of the linear regression of equation 4.2 yielded values for $C_{inj}$ and $Q_{sw}$ of 1055 pF and -36.8 pC, and 1057 pF and 21.4 pC for the positive and negative injectors, respectively.

The results from the two calibration procedures for two sets of injection capacitors are shown in Table 4.1. The values obtained for the injection capacitance are consistent regardless of the method used for calibration. Moreover, the value obtained for the switch charge is consistent

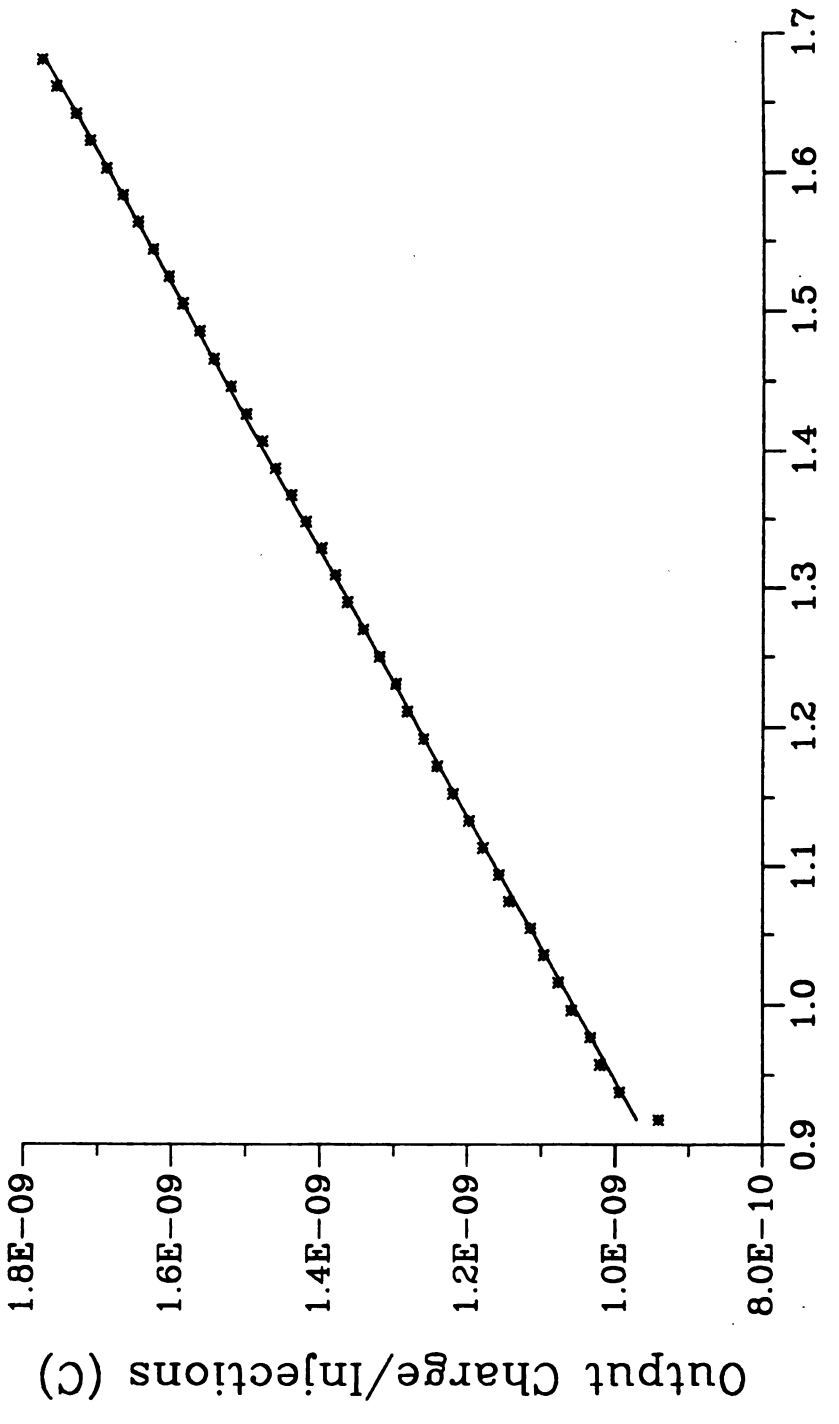


**Figure 4.9** Calibration curve for the positive potential maintenance injector using the cell equivalent circuit configuration with a 454.7 kΩ resistor.

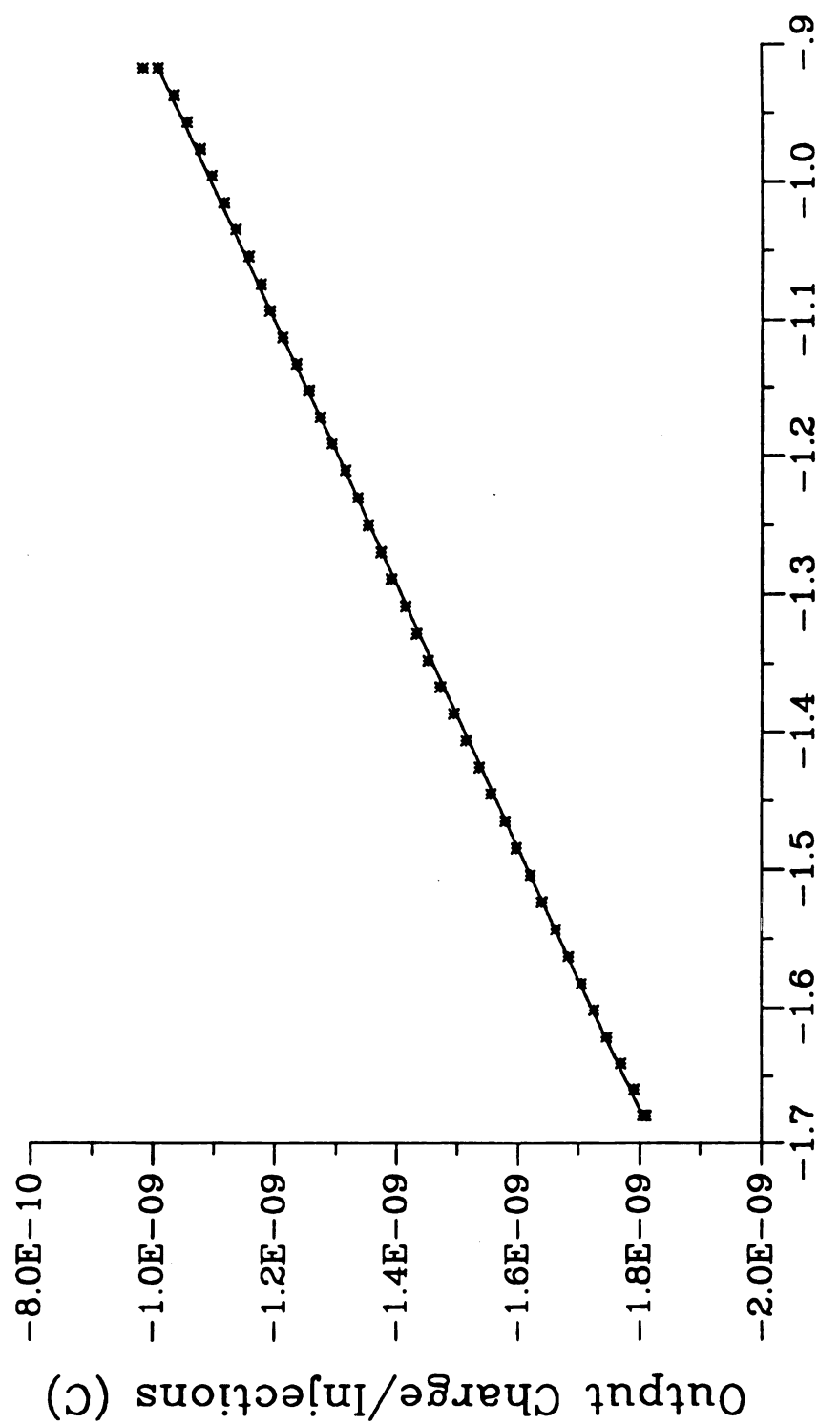


**Figure 4.10 Calibration curve for the negative potential maintenance injector using the integrator feedback configuration with a 454.7 kΩ resistor.**

TABLE 4.1 Comparison of the injection capacitance and switch charge per injection for the two methods of calibration.

| | INTEGRATOR | | CELL EQUIVALENT CIRCUIT | |
|---|---|---|---|---|
| | Injection Capacitance | Switch Charge | Injection Capacitance | Switch Charge |
| 1000 pF Injection Capacitor | | | | |
| Positive Injector | 1054 pF | -36.3 pC | 1055 pF | -36.8 pC |
| Negative Injector | 1056 pF | 20.3 pC | 1057 pF | 21.4 pC |
| 220 pF Injection Capacitor | | | | |
| Positive Injector | 287 pF | -35.8pC | 287 pF | -36.4 pC |
| Negative Injector | 293 pF | 20.7 pC | 294 pF | 21.5 pC |

even for the two different sets of injection capacitors used. Based on this information and the ease with which the second calibration procedure can be performed, the second method was used periodically to check the calibration of the polarizer.

**Error Assessment**

The analytical usefulness of an instrument is based upon the relative precision and accuracy with which the data can be acquired. In order to assess the accuracy of the polarizer, an estimation of the relative systematic error in the charge delivered to the cell by the charge injectors must be made. A propagation of the systematic error was performed for each of the calibration procedures previously described using the equations which define the output charge, $Q_{out}$ to the measured voltage. The resulting expression of the error are shown in equations 4.4 and 4.5 for the integrator and the cell equivalent circuit, respectively.

$$(\delta Q/Q) = (\delta V/V) + (\delta t/t) + (\delta C_f/C_f) \quad (4.4)$$

$$(\delta Q/Q) = (\delta V/V) + (\delta t/t) + (\delta R_f/R_f) \quad (4.5)$$

The systematic error in each of the components was estimated. The estimated error for the measurement of the output voltage of the control amplifier was ± 1/2 LSB. This corresponds to an error of 0.000612 V for a twelve bit ADC with a voltage span of 2.5 V. The estimated relative error was 0.1 % for both the standard resistor and the standard capacitor. These are the rated values of the components. The systematic error in the timing of the step is due to the delay between the end of the step and the acquisition of the voltage by the ADC. The worst case error based upon the known clock frequency of the timing device is one count for a step of 65,536 μs. This corresponds to a relative error $7.6 \times 10^{-7}$, which is negligible. The results of

the propagation of error, for an output voltage of 0.800 V, are given in Table 4.2. The results show that the most significant source of systematic error is the accuracy to which the standard capacitor or resistor is known.

Table 4.2 Table of error analysis for the charge-pulse polarizer obtained by propagation of error.

| Leakage Current | Integrator | Equivalent Circuit |
|---|---|---|
| 0.18 % | 0.18 % | 0.18 % |

The precision of the charge-pulse polarizer can be obtained experimentally by replicate calibrations and also by the propagation of the random errors. The relative standard deviation of 40 replicate scans for each calibration procedure was calculated. The calculated relative standard deviation is 0.1 % and is independent of the calibration procedure. This value agrees with the value obtained by a propagation of the random error, where the precision of the standard is assumed to be zero and the errors in the voltage and time are the same as those given previously. The value obtained by the propagation of error is 0.077 %. This value is governed by the quantization error of the ADC. Thus the charge-pulse polarizer is capable of injecting a known quantity of charge with a precision of 0.1 % and the potential can be measured and controlled to within 0.612 mV.

# CHAPTER 5

# A COMPARISON OF CHARGE-PULSE AND ANALOG POTENTIOSTATIC CONTROL FOR CYCLIC VOLTAMMETRY

## INTRODUCTION

Cyclic voltammetry is a controlled potential electroanalytical technique where the potential ramp is reversed at some predetermined value and proceeds back to the starting potential where it reverses again. This technique, typically the first experiment performed in an electrochemical analysis (23,24), was chosen to illustrate some of the important characteristic differences between charge-pulse polarization and conventional analog potentiostatic control. The characteristics examined and compared include charging current, iR drop, scan rate, and changes in concentration. Cyclic voltammetry was chosen since the effects of charging current and iR drop are easily seen and can be clearly distinguished.

## MATERIALS

The chemicals used for this study were ACS reagent grade $CdCl_2$ and $KNO_3$. These chemicals were used without further purification. The stock solution for the supporting electrolyte was 1 M $KNO_3$ and the cadmium stock solution was 0.1 M $CdCl_2$. All subsequent solutions were prepared by serial dilution in large volume flasks to minimize weighing and volumetric errors. The water used in the dilutions was deionized water from an "in-house" reverse osmosis type deionizer followed by distillation.

The mercury for the mercury electrode was triply distilled and was subjected to further chemical pretreatment. The chemical pretreatment was that suggested by the SMDE manufacturer, Princeton Applied Research (25). The pretreatment consists of placing equal volumes of mercury and 10% sodium hydroxide in a 1 liter flask. Tank oxygen is then passed into the mercury by a disposable Pasteur pipette for a period of 12 hours. Extreme caution must be used and no open flames are allowed. The mercury is rinsed with deionized water, and the procedure is repeated using 10% nitric acid. Again the mercury is rinsed with deionized water and the excess water removed. After the excess water is removed, the mercury is filtered through a paper filter which has a pinhole at the center into a clean polyethylene container. Any residual scum or water will remain on the filter paper.

To eliminate the reduction of oxygen and subsequent changes in pH of the analyte solution, the nitrogen used to purge the solution was passed through two gas scrubbing towers. The procedure used was adapted from the procedure suggested by PAR (26). The first tower contained a solution of vanadous chloride and amalgamated zinc, and the second tower contained 0.1 M potassium nitrate, the supporting electrolyte. The vanadous chloride solution is prepared by boiling 2 grams of ammonium metavanadate with 25 ml of concentrated hydrochloric acid and diluting the solution with 250 ml of water. The solution produced contains vanadium in several higher oxidation states and should be blue or green in color. The diluted solution is then transferred to a gas scrubbing tower, and 10 grams of amalgamated zinc is added. The solution will retain its original color until nitrogen is bubbled through it, at which point it will turn purple. The solution will revert back to a blue or green solution upon exhaustion but can easily be rejuvenated by the

addition of a few drops of concentrated hydrochloric acid. If the acidity is too low a precipitate will form. The precipitate can then be redissolved by the addition of 10% hydrochloric acid.

Glassware used in this study was cleaned by rinsing with tap water and soaking for 24 hours in a strong solution of Alconox followed by rinsing with deionized water. After a thorough rinsing, the glassware is then soaked in 6 M $HNO_3$ for 24 hours. After soaking, the glassware is again thoroughly rinsed with deionized water. All glassware is then dried in an oven for 24 hours at 70° C. The glassware is stored under aluminum foil to prevent dust from settling onto the surface of the glassware. The only exception to this procedure is for the glass capillary. It was cleaned according to the manufacturer's instructions by aspirating 6 M $HNO_3$ for 5 minutes followed by aspirating deionized water for 30 minutes. After cleaning, the capillary is dried by aspirating air for several hours.

The electrode used throughout this comparison study was a PAR 303A, Princeton Applied Research, Princeton, New Jersey. The PAR 303A is a Static Mercury Drop Electrode (SMDE) which delivers a known volume of mercury down the capillary by using a solenoid between the reservoir and the capillary to interrupt the flow of mercury. When the capillary is energized, by either the front panel push button or by remote control from the controlling instrument, the mercury is allowed to flow down the capillary until the desired drop size, selected by the front panel, is obtained.

The potentiostat used to obtain the conventional voltammograms, for comparison to those obtained by the charge-pulse polarizer, was a PAR 364, Princeton Applied Research. The internal waveform generator was modified by M. Raab (27), such that the polarographic analyzer was capable of generating a linear cyclic potential waveform. The scan rates of the PAR 364

are 500, 200, 100, 50, 20, 10, 5, 2, 1 mV $s^{-1}$. While these scan rates are not extremely fast, under certain conditions the effects of charging current and ohmic drop can be observed.

**EXPERIMENTAL PROCEDURE**

The procedure for operating the PAR 364 in the cyclic voltammetric mode is given below. The starting potential is set by selecting the sign of the of the starting voltage, the range (0,1, or 2 volts), and the appropriate value on the calibrated dial for millivolts. The operating mode is set to DC and the scan direction is negative. The cell switch is set to off. The turn-around potential is set by a 20 turn potentiometer which reduces the normal 1.5 V ramp generated by the PAR to the value selected by the potentiometer. This potentiometer is not calibrated and thus requires the use of several potential scans to adjust the turn around potential to the desired voltage. Once the turn-around point is set, the potentiostat is ready for use. The scan is initiated by setting the cell switch to "Init.", pushing the button labelled "Ready", and then changing the cell switch to "Scan". The range for the electrometer can be set by the "Current Range" switch. Immediately after a scan, the cell switch should be returned to the off position. This disconnects the potentiostat from the cell.

The operation of the polarizer requires the input of various parameters. These parameters include the starting potential, the turn-around potential, the number of steps to be used, the charging voltage for the maintenance injectors, and the timing parameters for the charge injectors. Careful selection of the timing parameters and the charging voltage for the injectors are needed to optimize the results of the polarizer. If the timing between pulses is too long or the charging voltage is not large enough, the polarizer will be unable to maintain the cell potential during the Faradaic

reaction. If, on the other hand, the voltage is too large or the timing between pulses is too short, quantitative transfer of the charge on the injection capacitors will not occur and the results will be meaningless. Once the proper values are entered, the parameters are loaded into the control logic of the polarizer; and the experiment is initiated by a START pulse from the microcomputer. The only intervention by the microcomputer occurs at the end of each step when an interrupt generated by the control logic signals the microcomputer to acquire the data.

The cyclic waveform generated by the polarizer is a staircase waveform as depicted in Figure 5.1. The potential scan starts at an initial potential where no Faradaic reaction is occurring. The potential is then stepped in a uniform manner until a predetermined turn-around potential is reached at which time the potential is then stepped back to the initial potential. The expanded view illustrates how the charge-pulse polarizer controls the cell potential. A specified small control window is generated in which the desired control potential exists. Whenever the cell potential crosses a window threshold, a uniform charge pulse of constant size and appropriate polarity is injected into the cell in order that the cell potential is restored to the control window. The rate of the maintenance charge injection is entirely determined by the rate at which the Faradaic reaction consumes charge from the double layer. The potential is then stepped by the potential step injector through the addition of variable sized charge pulses at a constant rate until the new desired control potential is achieved.

The experiments were performed by switching the SMDE between the PAR and the polarizer by means of a switchbox. This was easily accomplished since both instruments connect to the SMDE via a 25 pin D subminiature connector. The solution was purged with $N_2$ for 30 minutes

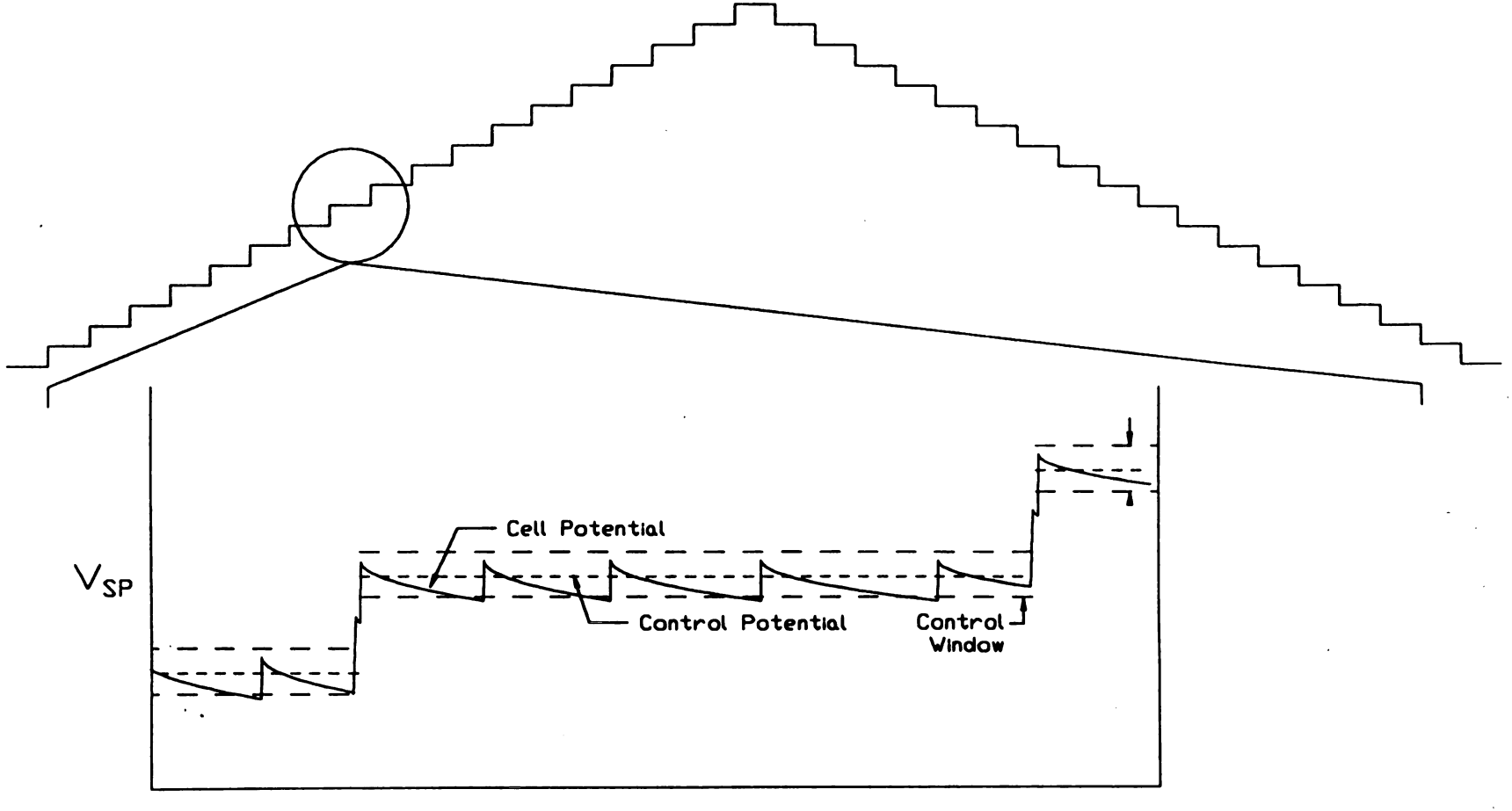


**Figure 5.1** **Description of charge-pulse staircase cyclic voltammetry with an expanded view of the potential control.**

between experiments. The order of the experiments was to purge the solution, obtain voltammogram with the PAR 364, dislodge and dispense a new drop, purge the solution for 30 minutes, and obtain a voltammogram with the polarizer. This method allowed the use of the same solution for each scan in the comparison study.

## PEAK HEIGHT VERSUS SCAN RATE

In conventional controlled potential electroanalysis the measured cell current, which is the summation of the charging and Faradaic currents, increases as the scan rate increases. This increase in the measured cell current is due to two factors. The first factor is the increased charging current needed to change the cell potential more rapidly. The second factor is the increase in the concentration ratio at the electrode surface due to a shorter time for depletion of the analyte from the electrode surface. In all cases, the charging current increases at a more rapid rate than does the Faradaic current thereby increasing the error in the measurement of the Faradaic current. In stark contrast to potentiostatic control, the measured charge **increases** with **decreasing** scan rate. The increase in the measured charge is due to the integration of the charge consumption by the Faradaic reaction during the entire potential maintenance period. Therefore, with charge pulse polarization, the longer the step is maintained the further the extent of the reaction causing a greater amount of charge to be consumed and increasing the measured charge. Figure 5.2 is a plot of cathodic peak charge versus $(\text{scan rate})^{-1/2}$ where the step height was held constant at 3.66 mV and the duration of the step was varied.

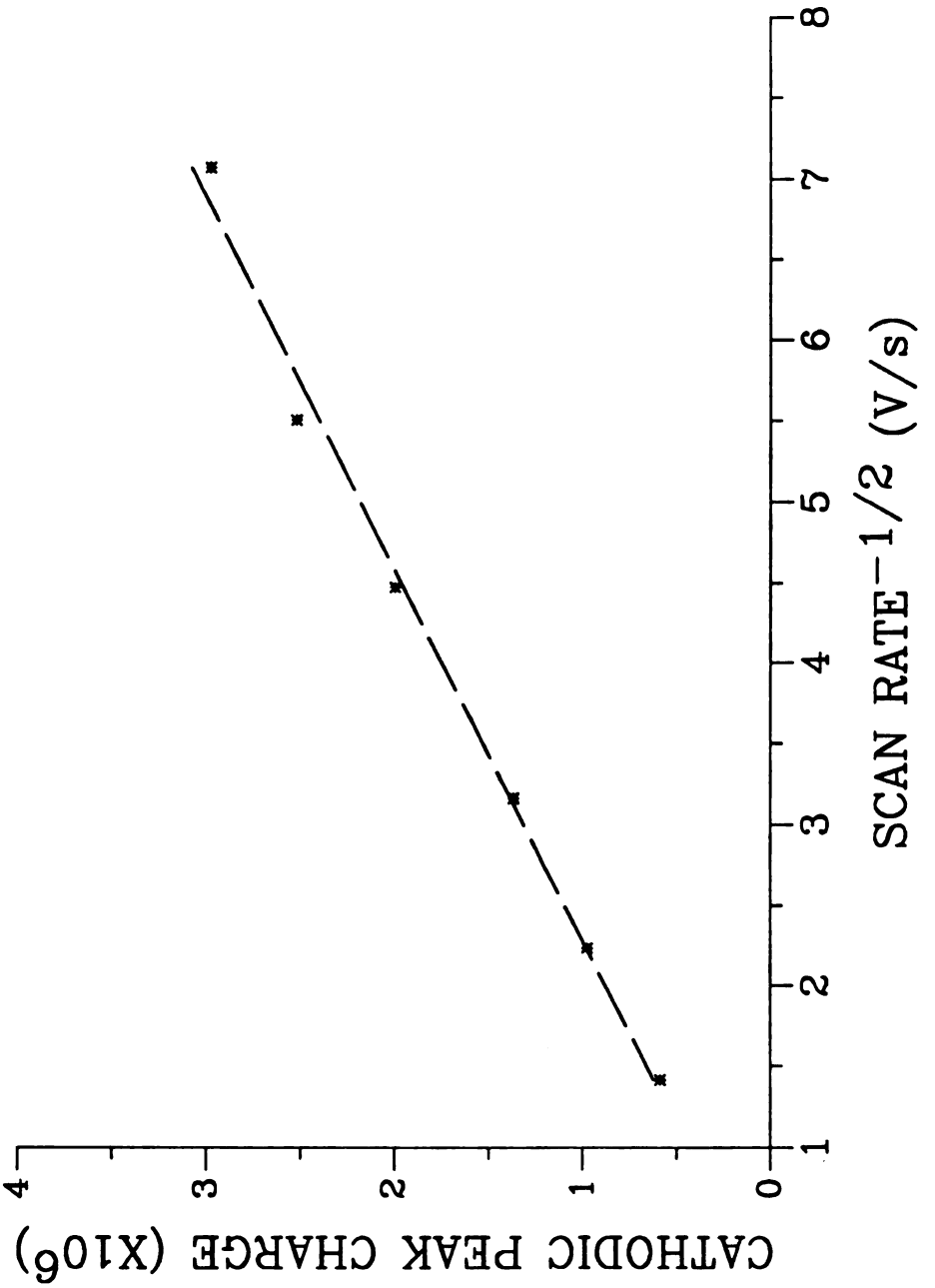


**Figure 5.2** Peak charge versus scan rate$^{-1/2}$ for a 5 mM $CdCl_2$ solution in 0.1 M $KNO_3$ supporting electrolyte.

## EFFECTS OF CHARGING CURRENT

Charging current arises from the need to change the extent of polarization of the working electrode. The charge which goes toward polarizing the working electrode is not related to the concentration of the analyte in solution and is therefore an error term when it is included in the measurement of the cell current. When a significant amount of charge is required to charge the double layer capacitance, the resulting voltammograms have a continually changing baseline and tend to take on an overall box shape. With charge pulse polarization the competition between the charging current and the Faradaic current is replaced by an equality of charging and Faradaic current since the Faradaic current occurs by the discharge of the double layer capacitance. To illustrate this, two series of voltammograms were obtained for a solution of 10 μM $CdCl_2$ in 0.1 M $KNO_3$. The first series was obtained using a PAR 364, in linear sweep mode, at scan rates of 500, 200, 100, 50, 20, and 10 millivolts per second. The resulting voltammograms are shown in Figure 5.3. Notice the non-zero baseline and the overall box shape to the voltammogram. The second series of voltammograms, shown in Figure 5.4, was obtained by the charge-pulse polarizer, using a staircase waveform, at the same scan rates as the previous series. This series of voltammograms does not have the characteristic box shape which was seen in the first series of voltammograms. In addition, the baseline for each of the scans in this series was zero. The comparison of these two series of voltammograms clearly demonstrates that the charge-pulse polarizer eliminates the effects of charging current in the resulting voltammograms.

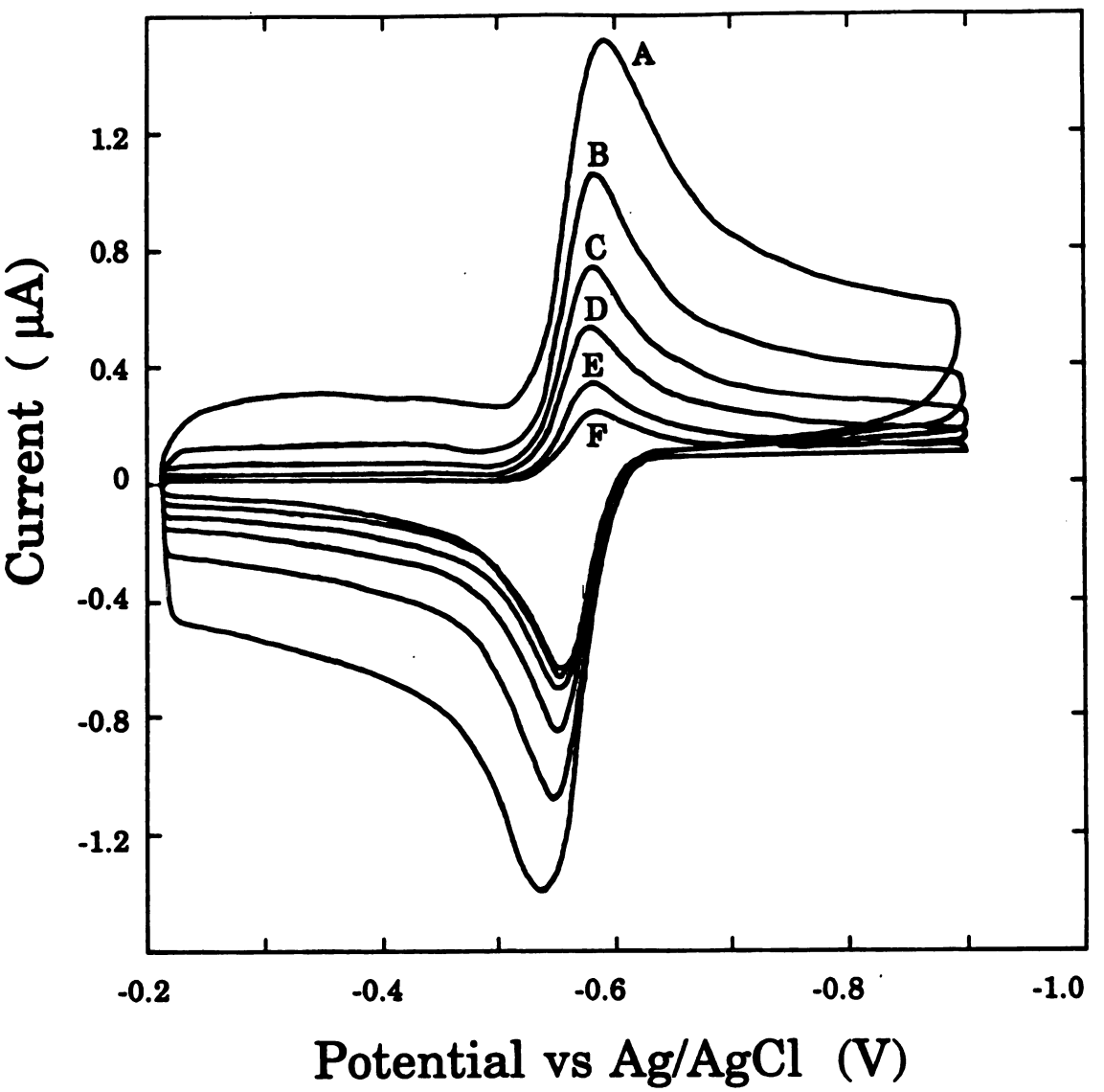


**Figure 5.3** The effect of charging current on conventional analog voltammograms at scan rates of: a) 20 $mVs^{-1}$; b) 50 $mVs^{-1}$; c) 100 $mVs^{-1}$; d) 200 $mVs^{-1}$; e) 500 $mVs^{-1}$.

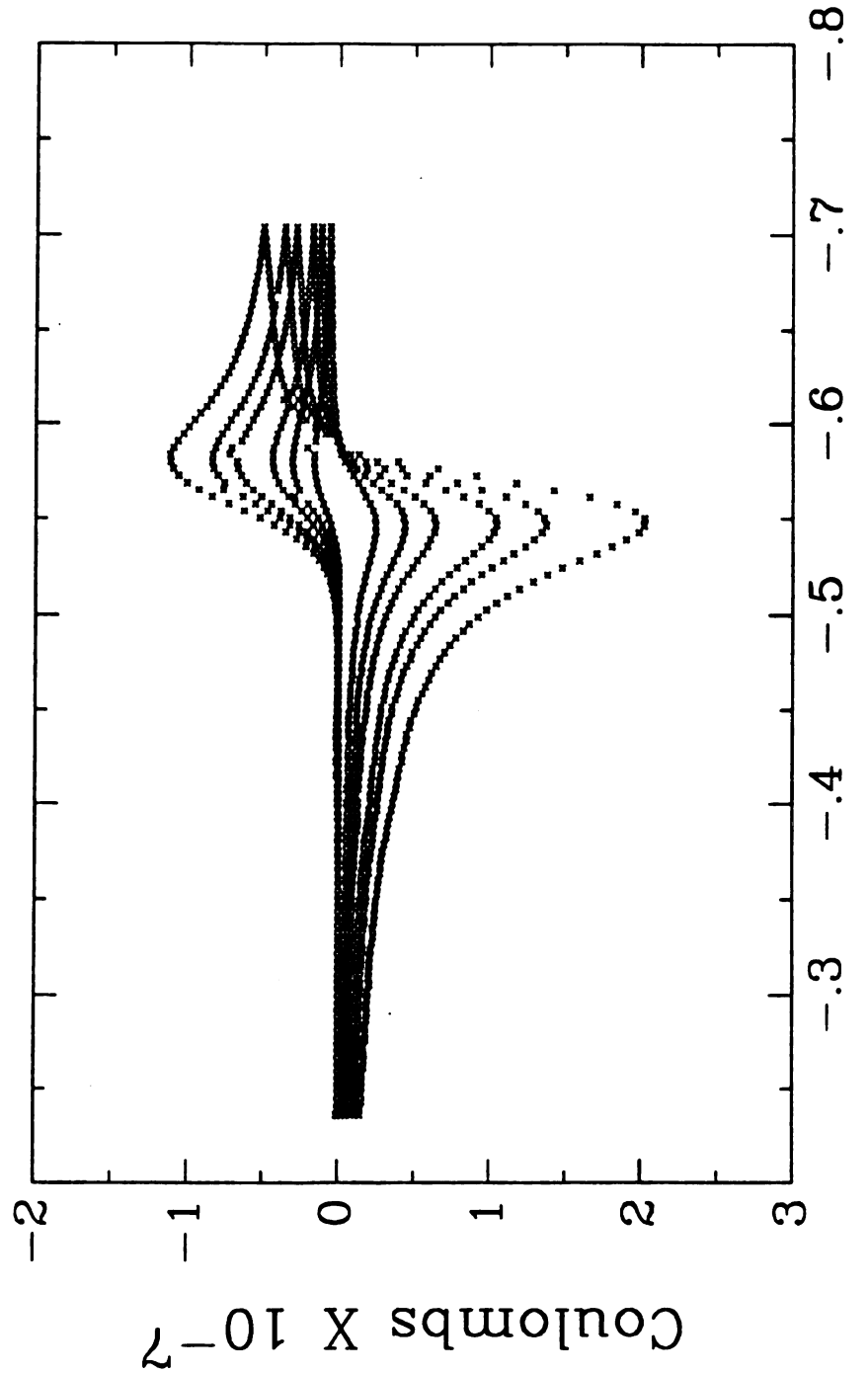


**Figure 5.4** The effect of charging current on charge-pulse voltammograms at scan rates of: a) 20 $mVs^{-1}$; b) 50 $mVs^{-1}$; c) 100 $mVs^{-1}$; d) 200 $mVs^{-1}$; e) 500 $mVs^{-1}$.

## EFFECT OF OHMIC DROP

The ohmic drop across the uncompensated resistance between the reference and working electrodes causes the peak potentials of a voltammogram to shift in the direction of the potential scan. For solutions where significant amounts of current is present in the cell, this potential shift can become quite large, i.e., several hundred millivolts. To illustrate this effect, two series of voltammograms were obtained for a solution of 5 mM $CdCl_2$ in 0.1 M $KNO_3$ with scan rates of 500, 200, 100, 50 mV/s.. The first series was obtained with the PAR 364 (see Figure 5.5) and the second series of voltammograms was obtained by the charge-pulse polarizer (see Figure 5.6). These conditions were chosen to accentuate the effects of ohmic drop on the voltammograms and are not typical of those used in an optimized analysis. Notice in Figure 5.5, the voltammograms acquired by the PAR, that the peak potentials for the cathodic reaction are shifted to more negative potentials as the scan rate increases and that the peak potentials for the anodic reaction are shifted to more positive potentials. From the shift in peak potentials obtained with the PAR, the uncompensated solution resistance was calculated to be approximately 300 Ω. For the voltammograms shown in Figure 5.6, the series obtained by the charge-pulse polarizer, the peak potentials are not shifted by increasing scan rate as in the first series of voltammograms. This is the expected result, since the cell potential is monitored between charge injections when the cell is at open circuit and no current, or charge, is being applied to the cell. The concentration of the supporting electrolyte can be reduced without error until the solution resistance prevents charging of the double layer capacitance in a time that is short compared to the step duration. Where very low supporting

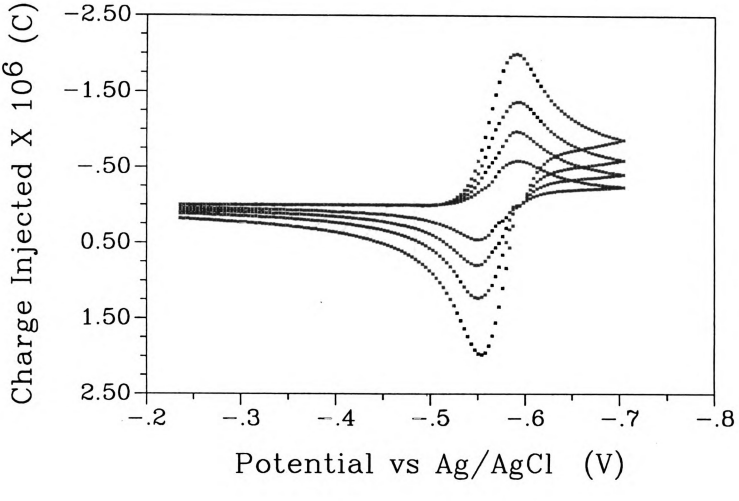


**Figure 5.6** **The effect of ohmic drop on charge-pulse voltammograms at scan rates of: a) 50 $mVs^{-1}$; b) 100 $mVs^{-1}$; c) 200 $mVs^{-1}$; d) 500 $mVs^{-1}$.**

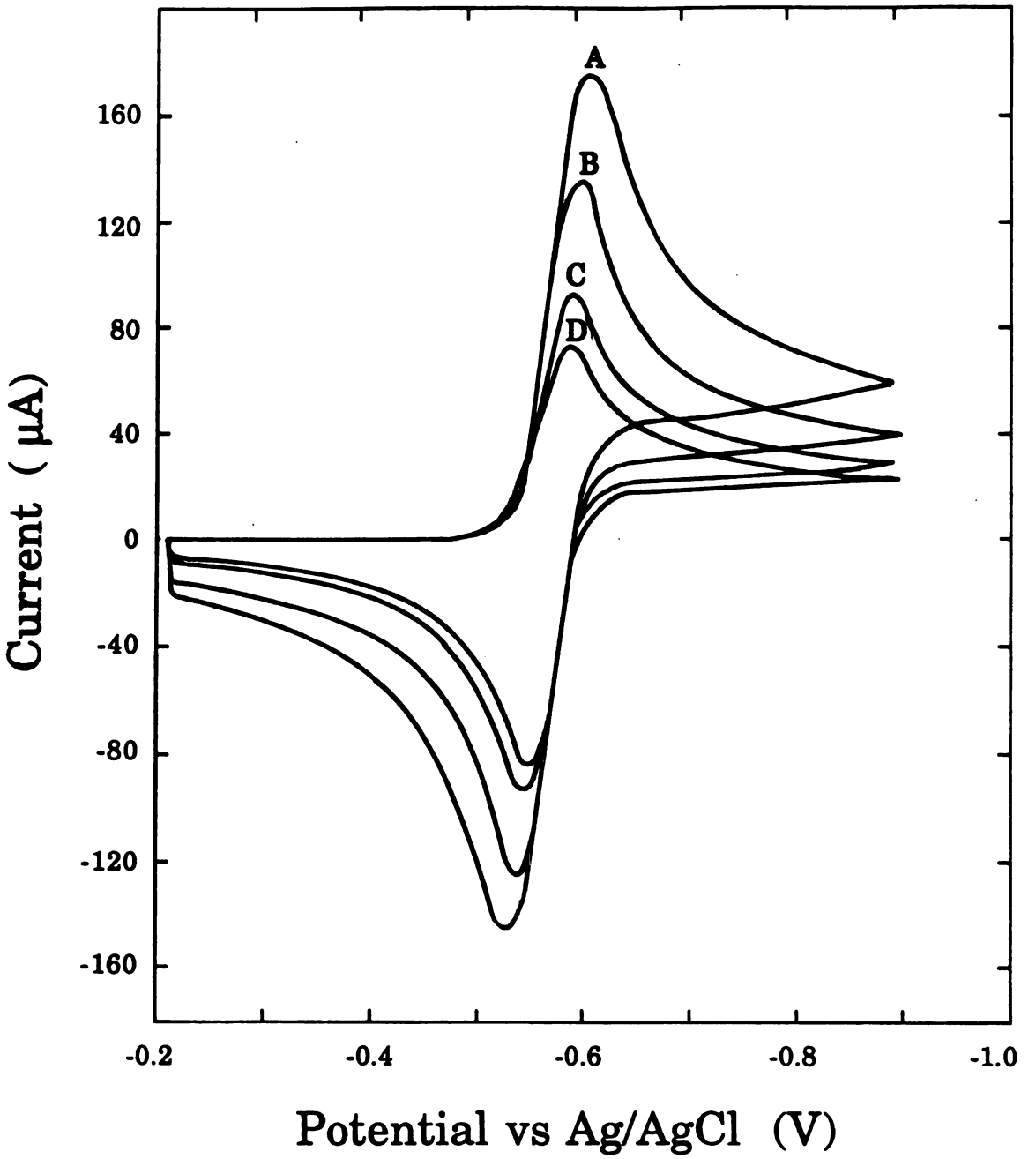


Figure 5.5 The effect of ohmic drop on conventional analog voltammograms at scan rates of: a) 50 $mVs^{-1}$; b) 100 $mVs^{-1}$; c) 200 $mVs^{-1}$; d) 500 $mVs^{-1}$.

electrolyte concentrations are used ($10^{-4}$ M or lower) a cell amplifier with high output voltage compliance should be used.

## CALIBRATION CURVE

To demonstrate the analytical usefulness of the charge-pulse polarizer a series of $CdCl_2$ solutions ranging from 1.0 μM to 2.0 mM with supporting electrolyte concentration of 0.01 M $KNO_3$ were analyzed using a constant value for the injection capacitance. The resulting cathodic peak charge was plotted versus analyte concentration and a linear regression performed. The regression yielded a regression coefficient of 1.000. Figure 5.7 illustrates the linear dynamic range of the polarizer for a constant capacitance by plotting the log of charge versus the log of concentration. This dynamic range is for a specific set timing parameters and injection capacitors. By changing these parameters, the linear dynamic range can be shifted from to higher or lower concentrations.

## CONCLUSIONS

The maximum rate at which the potential of an electrochemical cell can be stepped is governed by the maximum charge per injection and the maximum rate at which the charge-pulse polarizer can successively inject charge. The maximum charge per injection is given by $Q_{max} = (V_{max}/R_s)t_{inj}$ where $V_{max}$ is the maximum output voltage of the cell amplifier, $R_\sigma$ is the solution resistance between the working and auxiliary electrodes, and $t_{inj}$ is the time required for each injection. The maximum repetition rate for charge injections is 100 kHz. This includes the time required for the injection of the charge, the comparison of the reference electrode potential to the desired set point potential, and recharging the potential step injection capacitor. In this

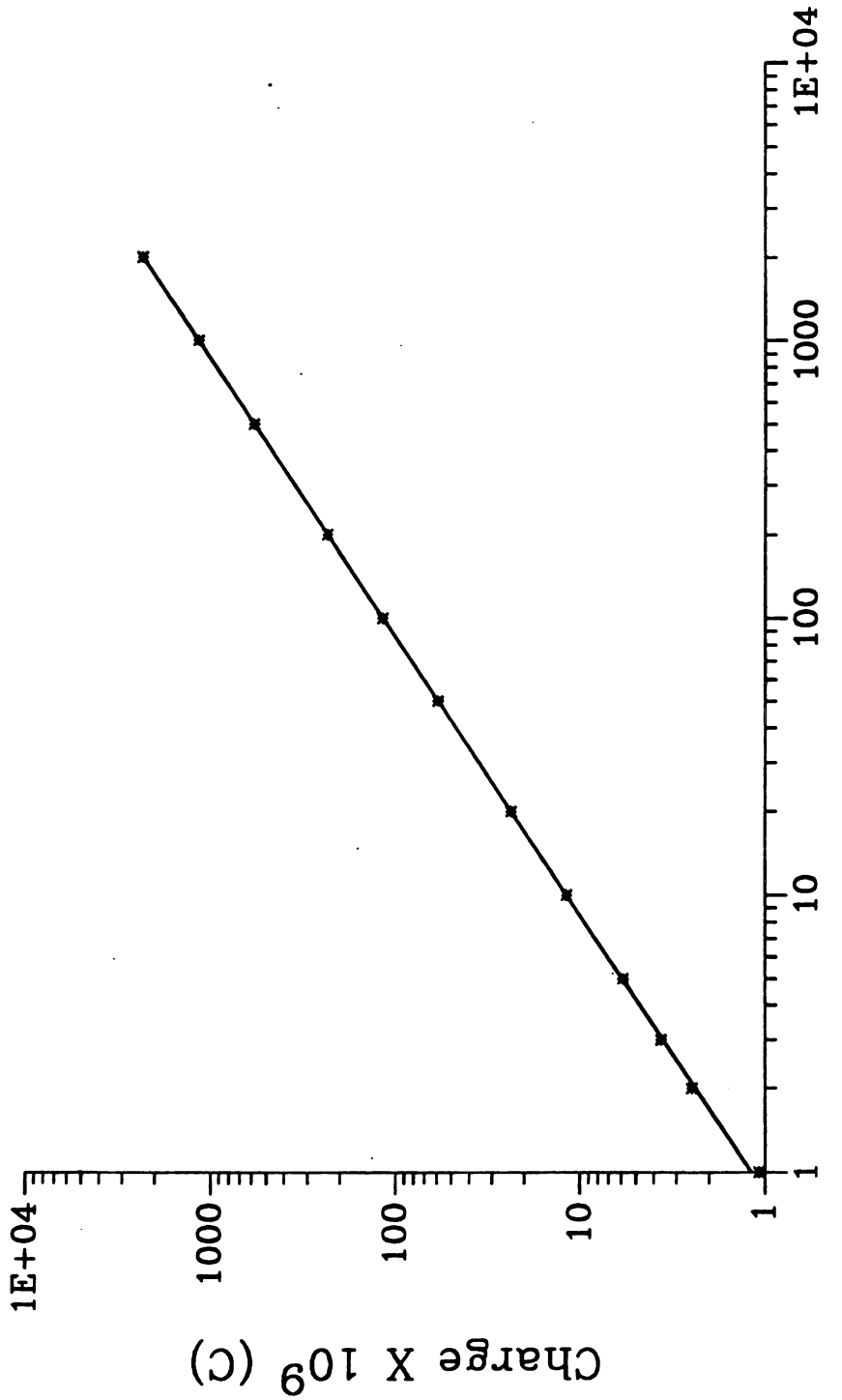


**Figure 5.7** Dynamic range of the polarizer for a 1054 pF maintenance injection capacitor represented as $\log_{10}$(charge) versus $\log_{10}$(concentration).

work, the 5 mV steps typically used were achieved in about 100 μs. At this time, integration of the Faradaic current begins.

The minimum charge which can be accurately measured by the charge-pulse polarizer is dependent upon the accuracy and precision to which the charge injection is known, the number of injections used, and the magnitude of the charging voltage. For quantitative measurements, at least 100 counts should be injected at the voltammetric peak and the charging voltage of the injection capacitor should be 0.1 V. These values correspond to an error of 1 %. With a 1054 pF injection capacitor, this corresponds to a Faradaic charge of 6.94 nC over the step interval. For a step duration of 50 ms (scan rate of 100 mV/s) this is an average Faradaic current of 0.139 μA. Of course the detection limit would be much lower. Use of a smaller injection capacitor could extend measurement of the system to still lower concentrations.

The Faradaic current measured in charge-pulse polarization has no exact parallel in analog voltammetry. In charge-pulse polarization the Faradaic charge is determined by the charge injection controller keeping track of the amount of charge injected rather than by independently measuring the current as in an analog potentiostat. With charge-pulse polarization the total accumulated charge over a step is determined rather than sampling the instantaneous current during the step. Since the accumulated charge is the integral of the Faradaic current over the entire step, an improvement in signal/noise is achieved. The measurement of the Faradaic charge begins immediately after the potential step is complete - much sooner than in an analog potentiostat. The average currents (total charge divided by step time) determined by the charge-pulse polarizer are generally greater than the instantaneous currents measured by an analog

potentiostat. Since the charge-pulse polarizer integrates the charge for the duration of the step, the sensitivity of the measurement increases with decreasing scan rate - opposite to the trend observed with analog potentiostats.

The resolution to which the charge-pulse polarizer can control the potential of an electrochemical cell is given by $\Delta V = Q_{inj}/C_{dl}$ where $Q_{inj}$ is the size of the maintenance injection. The accuracy to which the controlled potential is known is dependent upon the magnitude of the potential difference between the setpoint and the control window limits. For example in a cathodic scan, the potential of the electrochemical cell would be controlled about the negative limit of the control window but the recorded voltage would be the setpoint potential. If the value of $\Delta V$ is nearly equal to the difference in the control window limits, the control and setpoint potentials would be nearly identical. In our experiments potential control was maintained within 0.3 mV resolution.

## CLOSING COMMENT

From the data shown in this chapter, charge-pulse polarization is a superior alternative to conventional analog potentiostatic control for controlled potential electroanalysis. This is especially true when the cell conditions are such that charging current and/or ohmic drop cause errors in the resulting voltammograms. To increase the charge-pulse polarizer's ability to rapidly step the cell potential or to use very dilute supporting electrolyte, a cell amplifier with high output voltage compliance should be used. The development of a cybernetic control system, for the charge-pulse

polarizer, which is capable of optimizing the selection of the charging capacitor and the charging voltage could obviate the need for conventional potentiostats in all but a few cases.

# APPENDICES

## APPENDIX A.1

The software listed in this appendix is the instrument control code for the charge-pulse polarizer. The software is written in polyFORTH and assembly language.

```
BLOCK 1050
 0 1050 1061 THRU HEX 42A LOAD 42D LOAD 42B LOAD 42E LOAD
 1 HEX 42F LOAD 430 LOAD 431 LOAD
 2 12 IINJECT ! 20 DAC-DELAY !
 3 30 ISETTLE !
 4 20 DAC-SETTLE !
 5
 6
 7
 8
 9
10
11
12
13
14
15

BLOCK 1051
 0 ( SHOWS THE STATUS OF BLOCK BUFFERS AND UPDATE FLAG )
 1 MATH   0 DRIVE
 2 : ?BLK DUP 255 = IF DROP ."  ---" ELSE 5 U.R THEN ;
 3  ( SHOWS BLOCK NUMBER OR DASHES TO INDICATE EMPTY )
 4 : ?OFFSET DUP 127 AND DUP 127 = IF DROP 0 3 U.R ELSE 3 U.R
 5  THEN ;
 6
 7 : ?FLG ?OFFSET 128 AND 128 = IF ."   1" ELSE ."   0" THEN ;
 8   ( 1 INDICATES UPDATE FLAG SET )
 9
10
11 : DISK_STATUS CR ." INDEX " PREV @ 5 U.R PREV 2+ @ 5 U.R
12   CR ." BLOCK #   OFFSET FLAG " PREV 12 + PREV 4 + DO
13   CR I C@ ?BLK 8 SPACES I 1+ C@ ?FLG 2 +LOOP ;
14   ( SHOWS WHAT PREV IS SET TO )
15
```

```
BLOCK 1052
 0 ( SYSTEM CONSTANTS AND INTERRUPT VARIABLES ) HEX
 1 ( Constants which are addresses of counters are lower case )
 2 F1C0 CONSTANT GO          F1C9 CONSTANT OFF
 3 F1C8 CONSTANT ON          F1C7 CONSTANT Convert
 4 F1D2 CONSTANT Idelay      F1C4 CONSTANT Vinj
 5 F1C6 CONSTANT Idac        F1CA CONSTANT LATCH
 6 B040 CONSTANT WRD         F1E3 CONSTANT Get-counts
 7 F1D0 CONSTANT Dac_delay   F1D1 CONSTANT Dac_settle
 8 F1D2 CONSTANT Isettle     F1D8 CONSTANT Iinject
 9 F1D9 CONSTANT Qinject     F1DA CONSTANT Qcharge
10 F1E0 CONSTANT -Counts     F1E2 CONSTANT +Counts
11 F1E8 CONSTANT HSteptime   F1E9 CONSTANT LSteptime
12 F1C1 CONSTANT RDAC        F1C3 CONSTANT RDAC2
13 VARIABLE VADC 0 VADC !
14 VARIABLE DPTR  0 DPTR !
15  DECIMAL

BLOCK 1053
 0 ( INITIALIZE VARIABLES  ) HEX
 1 VARIABLE VINIT     VARIABLE VFINAL   VARIABLE #_STEPS
 2 VARIABLE ISETTLE   CVARIABLE IDAC   CVARIABLE CFLG 0 CFLG C!
 3 VARIABLE VINJ      VARIABLE STEP-SIZE  VARIABLE SWEEPRATE
 4 VARIABLE LSTEPTIME     VARIABLE VSTAT  VARIABLE STEP_#
 5 VARIABLE STEPDAC 3EC ALLOT  STEPDAC 3EC ERASE   0 STEP_# !
 6 VARIABLE HSTEPTIME    VARIABLE DAC_DELAY VARIABLE QINJECT
 7 VARIABLE QCHARGE   VARIABLE IINJECT   VARIABLE DAC_SETTLE
 8 VARIABLE +COUNTS   VARIABLE -COUNTS  CVARIABLE +STAT
 9 CVARIABLE -STAT
10 VARIABLE NAME      B000 CONSTANT HEADBUF
11 CVARIABLE #BLK     CVARIABLE BLKOFF  VARIABLE #_CNTS
12 VARIABLE N-FREE    VARIABLE K-FREE
13 VARIABLE 'FRE-BLK   VARIABLE #_BLKS
14
15 FE81 CONSTANT INT-MSK   VARIABLE SAV-MSK

BLOCK 1054
 0 ( THIS BLOCK WRITES DATA FOR THE EXPERIMENTS ) HEX
 1
 2 ( : WRITE-DATA 400 0 DO I B000 + 0FFF SWAP ! 2 +LOOP  ;
 3 : WRITE-EOF 3FE B000 + 1388 SWAP ! ; )
 4 : NORM'S-FILE 504E NAME ! ; : KAT'S-FIL  464B NAME ! ;
 5  DECIMAL
 6 : KATHY K-FREE  ;
 7 : Norman N-FREE  ;
 8
 9 : FRE-BLK  'FRE-BLK @ EXECUTE ;
10 : WHO ." NORM =1 / KAT =2 " 1KEY DUP 49 - 0= IF [']  Norman
11   'FRE-BLK ! DROP NORM'S-FILE ELSE 50 - 0= IF [] KATHY
12   'FRE-BLK ! KAT'S-FIL  THEN THEN ;
13 : GET-FREE 0 BLOCK DUP 10 + @ N-FREE ! 20 + @ K-FREE !  ;
14 : FREE-BLOCK 0 BLOCK 10 + N-FREE @ SWAP ! 0 BLOCK 20 + K-FREE @
15   SWAP ! UPDATE FLUSH ;
```

```
BLOCK 1055
 0 ( THIS BLOCK WRITES THE DATA FROM THE DISK BUFFERS TO HDISK )
 1 DECIMAL
 2
 3 : BLK# ( --BLOCK OFFSET) FRE-BLK @ 256 /MOD 128 + SWAP ;
 4 : NBLKS  #_CNTS @ 120 /MOD SWAP 0= NOT IF 1+ #_BLKS ! ELSE
 5  #_BLKS ! THEN ;
 6 : STORE-IT #_BLKS @ 0 DO BLK# PREV 4 2 I * + + C! PREV 5 2 I
 7  * + + C! FRE-BLK @ 1+ FRE-BLK ! FLUSH  LOOP ;
 8
 9
10 HEX
11 : ?VSTATIC F1C7 C@ DROP 10 0 DO LOOP F1CA @
12  0FFF AND VSTAT ! ; DECIMAL
13
14
15

BLOCK 1056
 0 ( EXPERIMENTAL SET-UP ROUTINES )
 1 : Y/N ."  ENTER Y OR N " KEY   ;
 2 : CHECK-IT Y/N 89 = IF ." ENTER CORRECT VALUES " ELSE THEN ;
 3 : "INPUT ." ENTER THE VALUE OF " ;
 4 : INPUT-PARAMETERS PAGE "INPUT ." STEP SIZE " INPUT STEP-SIZE !
 5    CR "INPUT ." HIGH WORD OF STEP TIME " INPUT HSTEPTIME !
 6   CR "INPUT ." LOW WORD OF STEP TIME " INPUT LSTEPTIME !
 7            CR "INPUT ." CHARGING DAC " INPUT VINJ !
 8            CR "INPUT ." CURRENT CONTROL " INPUT IDAC C!
 9            CR "INPUT ." FINAL VOLTAGE " INPUT VFINAL !
10         CR "INPUT ." LARGE INJ. DELAY " INPUT ISETTLE C! CR
11 ." INITIAL VOLTAGE "  VSTAT @ 6 U.R CR ." IS INITIAL VOLTAGE OK
12  " Y/N 89 =  NOT IF CR ." ENTER INITIAL VOLTAGE " INPUT VINIT !
13 ELSE  THEN ;
14
15

BLOCK 1057
 0 (
 1 : SWEEP-RATE STEP-SIZE @ STEPTIME @ 12207 SWAP M*/ SWEEPRATE ! ;
 2 )  : ?#STEPS VFINAL @ VINIT @ - STEP-SIZE @ /MOD SWAP 0= NOT IF
 3  ." VFINAL WILL BE OFF BY 1 STEP SIZE " THEN #_STEPS ! ;
 4
 5 : CHECK-PARAMS ." INITIAL VOLTAGE " VINIT @ 6 U.R CR
 6  ." FINAL VOLTAGE " VFINAL @ 6 U.R CR
 7 ." STEP SIZE IN DAC UNITS " STEP-SIZE @ 6 U.R
 8 CR  ." STEP TIME IN COUNTS " HSTEPTIME @ 6 U.R
 9 CR ." STEP TIME IN COUNTS " LSTEPTIME @ 6 U.R
10 CR  ." LARGE INJECTOR DELAY " ISETTLE C@ 6 U.R
11 CR  ." CURRENT INJECTOR CONTROL DAC " IDAC C@ 6 U.R
12 CR  ." CHARGING DAC " VINJ @ 6 U.R CR  ;
13
14
15
```

```
BLOCK 1058
 0 ( STEP CALCULATION ROUTINES )
 1
 2 : UP-RAMP STEP-SIZE @ STEP_# @ * VINIT @ + ;
 3 : DOWN-RAMP STEP-SIZE @ #_STEPS @ 2* STEP_# @ - * VINIT @ + ;
 4
 5 : !STEP STEP_# @ 2*  STEPDAC + ! ;
 6
 7 : RAMP #_STEPS @ 2* 2+ 0 DO I #_STEPS @ - DUP 0< IF UP-RAMP
 8  !STEP  I STEP_# ! DROP ELSE 0= IF UP-RAMP !STEP I STEP_# !
 9   ELSE DOWN-RAMP !STEP I STEP_# ! THEN THEN LOOP 0 STEP_# !
10 100 #_STEPS @ 4 * 2+  DO I STEPDAC + 0 SWAP ! 2 +LOOP ;
11 : DRAMP #_STEPS @ 2 * 2+ 0 DO I #_STEPS @ - DUP 0< IF DOWN-RAMP
12 !STEP I STEP_# ! DROP ELSE 0= IF DOWN-RAMP !STEP I STEP_# !
13 ELSE UP-RAMP !STEP I STEP_# ! THEN THEN LOOP 0 STEP_# ! ;
14 : LIST-STEPDAC #_STEPS @ 2* 1+ 0 DO I 2* STEPDAC + @ U. CR LOOP
15  ; DECIMAL

BLOCK 1059
 0 ( TEST2 BLOCK )  DECIMAL
 1 : ?WHO WHO GET-FREE ;
 2 : ?INPUT BEGIN INPUT-PARAMETERS PAGE CHECK-PARAMS Y/N 89 = END ;
 3  : ?READY ." HIT ENTER WHEN YOU ARE READY TO RUN "
 4   BEGIN 1KEY 13 = END ;
 5
 6
 7
 8 : SAV-INT-MSK INT-MSK C@ SAV-MSK C! 01 INT-MSK C! ;
 9
10
11
12
13
14
15

BLOCK 1060
 0 : INPUT_PARAMETERS ." INPUT STEP SIZE " INPUT STEP-SIZE !
 1 ." INPUT CHARGING VOLTAGE " INPUT VINJ ! CR ." INPUT
 2 FINAL VOLTAGE " INPUT VFINAL ! CR ." INPUT HIGH WORD OF STEP
 3 TIME " INPUT HSTEPTIME ! CR ." INPUT LOW WORD OF STEP TIME "
 4 INPUT LSTEPTIME ! CR ." INPUT DAC DELAY TIME " INPUT DAC_DELAY
 5 ! CR ." INPUT DAC SETTLING TIME " INPUT DAC_SETTLE !
 6  CR ." INPUT I INJECT TIME " INPUT IINJECT ! CR
 7 ." INPUT CELL SETTLING TIME " INPUT ISETTLE ! CR ." INPUT CHARG
 8 ING TIME " INPUT QCHARGE ! CR ." INPUT Q INJECT TIME " INPUT
 9 QINJECT ! CR ;
10
11
12
13
14
15
```

```
BLOCK 1061
 0 HEX
 1 : SETUP_COUNTERS 3A F1D3 C! 72 F1D3 C! B2 F1D3 C!
 2            3A F1DB C! 7A F1DB C! BA F1DB C!
 3            30 F1E3 C! B0 F1E3 C!
 4            3A F1EB C! 7A F1EB C! ;
 5
 6 CODE W>B 0 0 SUB 1 1 SUB 0 POP 0 HI 1 MOV B 1 PUSH 0 1 MOV B
 7 1 PUSH NEXT   : LC! @ W>B ROT DUP ROT SWAP C! C! ;
 8
 9 ASSEMBLER   F4 OPC HLT     FORTH
10
11 ' HLT CONSTANT HALT
12
13 FFFF HSTEPTIME ! FFFF LSTEPTIME ! FFFF +COUNTS ! FFFF -COUNTS !
14 20 DAC_DELAY ! 20 QCHARGE ! 20 QINJECT ! 10 DAC_SETTLE !
15 10 ISETTLE ! 40 IINJECT !

BLOCK 1062
 0 HEX
 1 : LOAD_COUNTERS Dac_delay DAC_DELAY LC!
 2            Dac_settle DAC_SETTLE LC!
 3            Isettle   ISETTLE LC!
 4            Iinject    IINJECT LC!
 5            Qinject    QINJECT LC!
 6            Qcharge    QCHARGE LC!
 7            -Counts      -COUNTS LC!
 8            +Counts      +COUNTS LC!
 9            HSteptime  HSTEPTIME LC!
10            LSteptime  LSTEPTIME LC! ;
11
12 : FILL EMPTY-BUFFERS B3FE B000 DO 00 I ! 2 +LOOP ;
13
14 FORTH DECIMAL
15

BLOCK 1063
 0 ( THIS IS RETURNING 2 * THE ADC VALUE) HEX ASSEMBLER
 1 CREATE <ICOUNTER>
 2 0 PUSH 1 PUSH 2 PUSH W PUSH
 3 CE #B Get-counts MOV
 4 +Counts 2 MOV B    +Counts 0 MOV B    +Counts  0 HI MOV B
 5 -Counts 2 HI MOV B    -Counts 1 MOV B    -Counts  1 HI MOV B
 6 DPTR W MOV    0 WRD W) MOV      2 # W ADD   2 WRD W) MOV B
 7 W INC    1 WRD W) MOV     2  # W ADD    2 HI WRD W) MOV B
 8 W INC OFF 0 MOV B 0 0 SUB    Convert  0 MOV B 1 1 SUB 1 1 SUB
 9 LATCH 0 MOV   0FFF # 0 AND ON 1 MOV B
10  0 WRD W) MOV 2 # W ADD VINJ 0 MOV 0 WRD W) MOV  8 # W ADD
11 W DPTR MOV 90 #B HALT MOV  W POP  2 POP  1 POP   0 POP   STI
12 IRET
13  <ICOUNTER> 08 INTERRUPT
14
15
```

```
BLOCK 1064
 0 ( CALIBRATION CODE USING INTERRUPT HANDLER FOR LINEAR RAMP )
 1 HEX
 2 CODE SLEEP HLT NEXT
 3 : RUN 1 STEP_# ! STEPDAC @ RDAC ! RDAC2 C@ DROP #_STEPS 0 DO
 4 GO C@ DROP  SLEEP F4 HALT C! #_STEPS @ STEP_# @ - 0= IF
 5 01 INT-MSK C! THEN LOOP B000 100 DUMP ;
 6
 7
 8
 9
10
11
12
13
14
15

BLOCK 1065
 0   HEX
 1
 2 : LIST-DATA CR 6 PREV ! 6 PREV 2+ ! BLOCK B3F6 AFF6 DO 3 1 DO I
 3 0A * J + DUP @ 5 U.R 2+ DUP @ 5 U.R 2+ 7 1 DO DUP C@  5 U.R 1+
 4 LOOP DROP LOOP CR 14  +LOOP ;
 5
 6 CODE BFLIP 0 POP 1 1 SUB 0 1 HI MOV B 0 HI 1 MOV B FFFF #
 7 0 MOV 1 0 SUB 0 PUSH NEXT
 8 FORTH
 9 : LIST-COUNTS CR 6 PREV ! 6 PREV 2+ ! BLOCK B400 B000 DO
10  I  DUP @ 5 U.R 2+ DUP C@ 5 U.R 1+
11 DUP @ 5 U.R 2+ DUP C@ 5 U.R
12 1+ DUP  @  5 U.R 2+ @ 5 U.R   CR 10 +LOOP ;
13
14 : LIST-ALL CR 820 800 DO I U. CR I LIST-COUNTS CR LOOP ;
15

BLOCK 1066
 0 HEX ASSEMBLER
 1 CREATE <ICOUNTER> 0 PUSH 1 PUSH 2 PUSH
 2 W PUSH CE #B Get-counts MOV
 3 +Counts 2 MOV B    +Counts 0 MOV B    +Counts  0 HI MOV B
 4 -Counts 2 HI MOV B    -Counts 1 MOV B    -Counts  1 HI MOV B
 5 DPTR W MOV    0 WRD W) MOV      2 # W ADD   2 WRD W) MOV B
 6 W INC    1 WRD W) MOV     2  # W ADD    2 HI WRD W) MOV B
 7 W INC STEP_# 0 MOV 0 WRD W) MOV 2 # W ADD
 8  W DPTR MOV STEP_# W MOV W W ADD STEPDAC W) 0
 9 MOV  1 # STEP_# ADD   0 RDAC  MOV 0  RDAC2 MOV B
10  90 #B HALT MOV  W POP  2 POP  1 POP   0 POP   STI
11 IRET
12
13  <ICOUNTER> 08 INTERRUPT
14
15
```

```
BLOCK 1067
 0 CODE SLEEP HLT NEXT ' SLEEP CONSTANT HALT
 1 : RDAC! F1C1 ! F1C3 C@ DROP ; : GO F1C0 C@ DROP ;
 2 : 1STEP ( OFFSET ) STEPDAC + @ RDAC!
 3 GO 10 0 DO I DROP LOOP SLEEP F4 HALT C! ;
 4 : STAIRCASE #_STEPS @ 2* 1+ 0 DO OFF C@ DROP I U. I 2 * 1STEP
 5 LOOP OFF C@ DROP 01 INT-MSK C! ; : ARM-INT 00 INT-MSK C! ;
 6 HEX ASSEMBLER  CREATE <ICOUNTER>
 7 0 PUSH 1 PUSH 2 PUSH W PUSH CE #B Get-counts MOV
 8 +Counts 2 MOV B   +Counts 0 MOV B   +Counts  0 HI MOV B
 9 -Counts 2 HI MOV B   -Counts 1 MOV B   -Counts  1 HI MOV B
10 DPTR W MOV   0 WRD W) MOV     2 # W ADD   2 WRD W) MOV B
11 W INC   1 WRD W) MOV     2  # W ADD   2 HI WRD W) MOV B
12 W INC W 1 MOV  STEP_# W MOV W W ADD STEPDAC W) 0 MOV 1 W MOV
13 0 WRD W) MOV 2 # W ADD W DPTR MOV STEP_# INC 90 #B HALT MOV
14  W POP  2 POP  1 POP   0 POP   STI IRET
15  <ICOUNTER> 08 INTERRUPT FORTH

BLOCK 1068
 0 CODE SLEEP HLT NEXT ' SLEEP CONSTANT HALT VARIABLE CADC
 1 0 CADC ! VARIABLE ADCVAL 100 ALLOT
 2 ( TEST HANDLER 4-26-88 ) HEX ASSEMBLER
 3 CREATE <ICOUNTER> 0 PUSH 1 PUSH 2 PUSH
 4 W PUSH CE #B Get-counts MOV
 5 +Counts 2 MOV B   +Counts 0 MOV B   +Counts  0 HI MOV B
 6 -Counts 2 HI MOV B   -Counts 1 MOV B   -Counts  1 HI MOV B
 7 DPTR W MOV   0 WRD W) MOV     2 # W ADD   2 WRD W) MOV B
 8 W INC   1 WRD W) MOV     2  # W ADD   2 HI WRD W) MOV B
 9 W INC W 1 MOV +COUNTS 0 MOV 0 +Counts MOV B 0 HI +Counts MOV B
10 -COUNTS 0 MOV 0 -Counts MOV B 0 HI -Counts MOV B
11 STEP_# W MOV  W W ADD  STEPDAC W) 0 MOV  1 W MOV
12 0 WRD W) MOV 2 # W ADD W DPTR MOV STEP_# INC 90 #B HALT MOV
13 F1CA  0 MOV  CADC W MOV 0 ADCVAL W) MOV 2 # CADC ADD
14  W POP  2 POP  1 POP   0 POP   STI IRET
15  <ICOUNTER> 08 INTERRUPT FORTH

BLOCK 1069
 0 ( TEST HANDLER 4-26-88 ) HEX ASSEMBLER
 1 CREATE <ICOUNTER> 0 PUSH 1 PUSH 2 PUSH
 2 W PUSH CE #B Get-counts MOV
 3 +Counts 2 MOV B   +Counts 0 MOV B   +Counts  0 HI MOV B
 4 -Counts 2 HI MOV B   -Counts 1 MOV B   -Counts  1 HI MOV B
 5 DPTR W MOV   0 WRD W) MOV     2 # W ADD   2 WRD W) MOV B
 6 W INC   1 WRD W) MOV     2  # W ADD   2 HI WRD W) MOV B
 7 W INC STEP_# 0 MOV 0 WRD W) MOV 2 # W ADD
 8  W DPTR MOV STEP_# INC 90 #B HALT MOV
 9  W POP  2 POP  1 POP   0 POP   STI IRET
10  <ICOUNTER> 08 INTERRUPT FORTH
11 CODE SLEEP HLT NEXT ' SLEEP CONSTANT HALT
12 : RDAC! F1C1 ! F1C3 C@ DROP ;
13 : 1STEP ( OFFSET ) STEPDAC + @ RDAC! SLEEP F4 HALT C! ;
14 : STAIRCASE #_STEPS 0 DO OFF C@ DROP I 1STEP LOOP 01 INT-MSK C!
15 ; : ARM-INT 00 INT-MSK C! ;
```

```
BLOCK 1070
 0 HEX
 1
 2 VARIABLE KNT 0 KNT !
 3 : RDAC! F1C1 ! F1C3 C@ DROP ; : GO F1C0 C@ DROP ;
 4 : 1STEP ( OFFSET ) STEPDAC + @ F1C1 ! F1C0 C@ F1C3 C!
 5  1 KNT +! SLEEP F4 HALT C! ;
 6 : STAIRCASE #_STEPS @ 2* 1+ 0 DO  I 2 * 1STEP
 7 LOOP  ;
 8 : ARM-INT 00 INT-MSK C! ;
 9 : CSTAT F1EB F1D0 DO CE 3 I + ! 8 +LOOP ;
10 : LCSTAT 4 0 DO I 8 * F1D0 + 3 0 DO DUP I + 3 0 DO DUP C@ U.
11 LOOP DROP CR LOOP DROP LOOP ;
12
13
14
15

BLOCK 1071
 0 : GETDATA B250 B048 DO I 3 + @ I 8 - 3 + @ - U. 8 +LOOP ;
 1 20 QCHARGE ! 8 QINJECT ! 50 IINJECT !  10 DAC_SETTLE !
 2 10 ISETTLE ! 8 DAC_DELAY !
 3 18 ISETTLE ! 28 IINJECT ! 8 DAC-SETTLE !
 4 60 QCHARGE ! 10 QINJECT ! 20  DAC-DELAY !
 5 : SHT 0 DPTR ! 0 STEP_# ! FILL ARM-INT ;
 6 : ONE SHT STAIRCASE B040 210 DUMP ;
 7 610 VINIT ! 20 #_STEPS ! 20 STEP-SIZE ! RAMP LIST-STEPDAC
 8 : FILADC 0 CADC ! 100 0 DO 0 I ADCVAL + ! 2 +LOOP ;
 9 : 1S SHT FILADC 1STEP ADCVAL @ U. B040 20 DUMP  ;
10 : GETADCVAL F1CA @ 0FFF AND ; DECIMAL SVARIABLE CONADC
11 0.00125 CONADC S! 0.0 2.5 F- SCONSTANT TEMP
12 2.0 SCONSTANT TWO  5.0 SCONSTANT FIVE
13 : VOLTS_ADC GETADCVAL >N CONADC S@ F* TEMP  FSWAP F+
14 TWO F* FIVE F+ 5 F. ; : VOLTS GETADCVAL >N CONADC S@ F*
15 TEMP FSWAP F+ TWO F* 5 F. ;

BLOCK 1072
 0 HEX ( CODE TO VIEW CALIBRATION DATA 6-2-88 )
 1 VARIABLE K
 2 : SBUFFER 6 6 PREV DUP 2+ ROT SWAP ! ! ;
 3 : SBLOCK EMPTY-BUFFERS SBUFFER BLOCK ;
 4 : CST K !  K @ 2+ C@ 70 = IF FFFF K @ ! THEN  K @ 5 + C@ 70 =
 5 IF FFFF K @ 3 + ! THEN  K @ 2+ C@ 30 = IF K @ @ 1+ K @ ! THEN
 6 K @ 5 + C@ 30 =  IF K @ 3 + @ 1+ K @ 3  + ! THEN  ;
 7 : -MAX FFFF SWAP - ;
 8 : READ-DATA B000 @ ." VINJ = " U. CR  B400 B040 DO I CST
 9  I @ -MAX 7 U.R  I 2+ C@ 7 U.R I 3 + @ -MAX 7 U.R I 5 + C@
10  7 U.R  I 6 + @ 7 U.R ( B260 I B040 - 8 / 2* + @ 0FFF AND 5 U.R
11  ) CR 8 +LOOP  ;
12 : 20READ 20 0 DO I 800 + SBLOCK READ-DATA CR CR LOOP ;
13
14
15
```

```
BLOCK 1073
 0 : VOLTS GETADCVAL >N CONADC S@ F* TEMP FSWAP F+ 5 F. ;
 1 : >VOLTS CR CR 82 0 DO 8 0 DO J I + ADCVAL + @ 0FFF AND >N
 2 CONADC S@ F* TEMP F+ 5 F. 2 +LOOP CR 8 +LOOP ;
 3
 4 DAC-DELAY = 20
 5         ISETTLE = 2C
 6         DAC_SETTLE = 28
 7 IINJECT = 12          QCHARGE = 60          QINJECT = 10
 8
 9
10
11
12
13
14
15

BLOCK 1074
 0 ( START AT VINIT AND GO DOWN THEN UP STEP CALCULATIONS )
 1
 2 : DRAMP STEP_SIZE @ STEP_# @ * VINIT @ SWAP - ;
 3 : URAMP STEP_SIZE @ #_STEPS @ 2* STEP_# @ - * VINIT @ SWAP - ;
 4
 5 : !STEP STEP_# @ 2* STEPDAC + ! ;
 6
 7 : NRAMP #_STEPS @ 2* 2+ 0 DO I #_STEPS @ - DUP 0< IF DRAMP
 8 !STEP I STEP_# ! DROP ELSE 0= IF DRAMP !STEP I STEP_# !
 9 ELSE URAMP !STEP I STEP_# ! THEN THEN LOOP 0 STEP_# !
10 100 #_STEPS @ 4 * 2+ DO STEPDAC I + 0 SWAP ! 2 +LOOP ;
11
12
13
14
15

BLOCK 1075
 0 HEX
 1 : WRITE_ADC CADC @ 0 DO ADCVAL I + @ B260 I + ! 2+ LOOP ;
 2 : INC_VINJ VINJ @ 10 + DUP DUP F1C4 ! 10 - B000 ! VINJ ! ;
 3 : 20_RUNS 20 0 DO ONE INC_VINJ WRITE_ADC 8800 I + PREV 4 + !
 4 DISK-STATUS INPUT DROP FLUSH LOOP ;
 5
 6
 7
 8
 9
10
11
12
13
14
15
```

```
VARIABLE ZZ 2 ZZ ! HEX ASSEMBLER

 CREATE <INT8>
0 PUSH
1 PUSH
2 PUSH
3 0 MOV
W PUSH
CE #B Get-Counts MOV
F1E0 # 3 MOV
2 # ZZ MOV
BEGIN
>R
2 # 2 MOV
 BEGIN 3 ) 0 MOV B
0 WRD W) MOV B
W INC
2 DEC
0< END
R>
3 INC
ZZ DEC
0< END
F1EA # I MOV
2 # 1 MOV
BEGIN I ) 0 MOV B
0 WRD W) MOV B
W INC
1 DEC
0< END
STEP_# I MOV
2 # I ADD
STEPDAC I) 0 MOV
 0 WRD W)  MOV
2 # W ADD
W DPTR MOV
0 F1C1 MOV
MAX_STEP DEC
 0< IF
90 #B HALT MOV
THEN
W POP
I POP
2 POP
1 POP
0 POP
 1 F1C0 MOV B
IRET
 <INT8> 08 INTERRUPT  FORTH
```

## APPENDIX A.2

The software written for data analysis and elementry plotting are given. The source code is written entirely in the C programming language.

```
*/ CV.C /*
#include    <stdio.h>
#include    <stdlib.h>
#include    <math.h>

#define     n_steps      var[0]
#define     vinj         var[1]
#define     capsize      var[2]
#define     i_inj        var[3]
#define     i_settle     var[4]
#define     dac_settle   var[5]
#define     dac_delay    var[6]
#define     q_inj        var[7]
#define     q_charge     var[8]
#define     h_step       var[9]
#define     l_step       var[10]
#define     com_len      var[11]
#define     BELL         printf("\007");

main ()
{

/*
  counts which cause a negative voltage are
  negative counts, these are the first set of
  numbers to be read from the file.
*/


  int    var[11 * sizeof(int)];
  int  i, pos_cnts, neg_cnts, vdac, stat_pos, stat_neg;
  int  l_cnts, l_time, l_stat ;
  float qout, volts, vinj_pos, vinj_neg, cappos, capneg,\
  posoffset, negoffset;
  char string[80], instring[80], outstring[80], comments[60];

  FILE *finstream, *fout1 *fout2;

  printf(" \nEnter the input filename >> ");
  gets( string);
  finstream = fopen(string, "r");
  printf(" \nEnter the output filename >> ");
  gets( string);
  finstream = fopen(string, "w");


/*
```

```
  Read the header information in the data file
*/
  for (i = 0; i <= 11; ++i)
    fscanf(finstream, "%6x", &var[i]);

 /*
  Read the comment field and determine if there is a comment.
  If a comment exists use the first word in the comment field
  as the output file name.
 */
  if (com_len)
  {
    fscanf(finstream, "%s", string);
/*          strcpy(instring, string);
    strcat(string, ".dat");
    foutstream = fopen(string, "w+a");      */
    fgets(comments, com_len, finstream);
  }
/*
  If no comment is present, then prompt user for filename.
*/
  else
  {
    fgets(comments, 61, finstream);
 /*         BELL
    printf(" \nEnter the output filename >> ");
    gets( string);
    strcpy(instring, string);
    strcat(string, ".dat");
    foutstream = fopen(string, "w+a");      */
  }


/*
  Read the data from the input file and manipulate it.
*/
  n=m=0;
  for(i = 0; i <= (n_steps * 2); ++i)
  {
    fgets(string, 81, finstream);
    sscanf(string, "%4x %4x %2x %4x %2x %4x %2x %4x",\
      &vdac, &pos_cnts, &stat_pos, &l_time,\
      &l_stat,& neg_cnts, &stat_neg, &l_cnts );
/*
  change the vinj to real numbers
*/
  vinj_neg = ((float) vinj * 5.00 / 4096.0) + 2.5 ;
  vinj_pos = ((float) vinj * 5.00 / 4096.0) + 2.5;
/*
  increment the count values by one since the counter represents
  ( count - 1 )
*/

    pos_cnts += 1;
```

```
    neg_cnts += 1;
    l_time  += 1;
    l_cnts  += 1;

/*
  Check the count values for a zero count by looking at the status byte
*/
    if( stat_pos == 0x70 && neg_cnts < 0xb00)
    {
      pos_cnts = 0;
      qout_neg += ( vdac * (5.00/4096.0) - 2.5) * time) / ( ohms * neg_cnts);
      ++n;
    }
    if( stat_neg == 0x70 && neg_cnts < 0xb00)
    {
      neg_cnts = 0;
      qout_pos += ( vdac * ( 5.00/4096.0) - 2.5) * time) / ( ohms * pos_cnts);
      ++m;
    }
  }
    qout_neg = qout_neg / n;
    qout_pos = qout_pos / m;

    fprintf( fout1, "%g,%g\n", qout_neg, vinj_neg);
    fprintf( fout2, "%g,%g\n", qout_pos, vinj_pos);
/*
  Print the output file without header information
*/



/*
  Plot the output data files
*/
  plot1(foutstream);
/*
  Close all files and end.
*/
  fclose(finstream);
  fclose(foutstream);
}
```

```
*/ LSQUARE.C /*
#include      <stdio.h>
#include      <stdlib.h>
#include      <math.h>
#define       ARRAY_SIZE  100

main(argc, argv)
intargc;
char*argv[ ];
{
/*  Define variable for the program                 */
  char fname[80], fname2[15], string[80];
  float x[ARRAY_SIZE + 1], y[ARRAY_SIZE +1], avex, avey;
  double xysum, xres2, sumx, sumy, a, b, xsum, ysum, Syx;
  double  yline, yres, xsqr, Sintercept, Sslope;
  double sqrt();
  double pow();
  int count, i, j;

/*  Set up file pointers for optional output devices    */
  FILE *instream, *outstream;

/*  printf("\n Enter the input filename ? => ");
  instream = fopen(gets(fname), "ra");               */
  instream = fopen(argv[1], "ra");
  outstream = fopen(argv[2], "a");
/*  printf("%s\n", fname);        */
  xsum = 0.0;
  ysum = 0.0;
  xsqr = 0.0;
  i = 0;

/*  Read in the data an calculate the x[i] square, xsum and ysum   */

  for(count = 0; count <= ARRAY_SIZE; ++count)
  {
    if ((fscanf(instream, "%e, %e", &x[count], &y[count])) == 2)
            {
          xsum = xsum + x[count];
          ysum = ysum + y[count];
          xsqr = xsqr + (x[count] * x[count]);
          ++i;
                }
              else
              break;
  }

/*  Calculate the average value of x and y                  */

  avex = (xsum / i);
  avey = (ysum / i);

  xres2 = 0.0;
  xysum = 0.0;
```

```
/*  Calculate the the variances in x and y and the x residuals
  and the sum(variance in x * variance in y)                */

  for(j = 0; j < i; ++j)
    {
    sumx = x[j] - avex;
    sumy = y[j] - avey;
    xres2 = xres2 + (sumx * sumx);
    xysum = xysum + (sumx * sumy);
       }

/* Calculate the slope and the intercept for the regression line */

      b = xysum / xres2;
      a = avey - (b * avex);

/* Calculate the deviations from the regression line       */

  yres = 0.0;
  for (count = 0; count < i; ++count)
    {
    yline = (b * x[count]) + a;
    yres = yres + pow((y[count] -yline), 2);
    }

/*  Calculate the statistic Sy/x                          */

  Syx = sqrt(yres / (i - 2));

/*  Calculate the error in the intercept and the slope        */

  Sslope = Syx / sqrt(xres2);
  Sintercept = Syx * sqrt(( xsqr / (i * xres2)));

/*  Print the Slope and error, and the intercept and error     */

  fprintf(outstream, " %s\n\
    \nSlope..... %6.4G\
    \nSlope error..... %6.4G\
    \nIntercept..... %6.4G\
    \nIntercept error... %6.4g"\
    , argv[1], b, Sslope, a, Sintercept);
  fcloseall();

}
```

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