This is to certify that the

thesis entitled

Test Generation and Concurrent Error Detection
for Current-mode A/D Converters

presented by

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has been accepted towards fulfillment
of the requirements for

Master of Science degree in Electrical Engineering

Carl Jay Way

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Date Sept 15, '92

TEST GENERATION AND CONCURRENT ERROR DETECTION IN CURRENT-MODE A/D CONVERTERS

By

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A THESIS

Submitted to
Michigan State University
in partial fulfillment of the requirements
for the degree of

MASTER OF SCIENCE

Department of Electrical Engineering

1992

ABSTRACT

TEST GENERATION AND CONCURRENT ERROR DETECTION IN CURRENT-MODE A/D CONVERTERS

By

Sondes Sahli

Analog MOS circuits are becoming increasingly sophisticated in terms of checking and correcting themselves. Self-correcting, self-compensating, or self-calibrating techniques have been employed in Analog-to-Digital (A/D) converters to eliminate errors caused by offset and low frequency noise, and to cancel switching error effects and non-linearities. For real-time applications, however, it is rather difficult to achieve validation of the converted data in the presence of faulty switching element(s). In this thesis, the effects of stuck-at-ON/OFF faults on the switching elements of a current-mode A/D converter are demonstrated, and the generation of test patterns for such a circuit is also addressed. Results show that the converter achieves full testability with two test currents. In addition, the A/D converter can be enhanced with concurrent error detection capability for real time applications.

To my parents

Habiba Boumaiza and *Mohamed Cherif Sahli,*

my brothers *Montassar*, *Nizar* and *Ahmed*

and my sister *Sonia*.

ACKNOWLEDGEMENTS

First I would like to thank Allah (SWT) for providing me with the ability to complete this work. I would like to thank Professor Chin-Long Wey, my thesis advisor, for his valuable inspiration and guidance. I would like to thank my friend Shoba for her continual support and help.

I am in debt towards my country, Tunisia, for providing me with the necessary support to get both my Bachelor and Master degrees.

I am very grateful for my parents for their years of concern and patience and to my sister and brothers for their encouragement.

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CHAPTER ONE

INTRODUCTION

After the recent progress in digital signal processing, there has been a trend towards an "all-digital" realization of devices and systems. Historically, the field of data conversion emerged from two sources: the interest in coding and decoding techniques primarily for telephone communication and the development of low cost digital computing power [1]. Today, conversion systems include circuits and systems that interface between the analog world and the digital world of communication, processing, storage and display.

The field of signal conversion encompasses a broad range of disciplines including sampled data theory, communication theory, noise theory, probability theory, numerical analysis, process manufacturing, instrumentation testing, etc. A conversion system involves numerous components such as sensors, operational amplifiers, isolators, sample and hold circuits, comparators, power supplies, analog-to-digital (A/D) converters, digital-to-analog (D/A) converters, etc. Among the critical properties to be considered when designing a data conversion system are resolution, accuracy, sampling rate, throughput, signal conditioning, intended disposition of the converted data, level of the system user, cost, dynamic range, environment conditions, tolerated level of complexity and required fault tolerance. Accordingly, the designer must carefully choose the system architecture that meets the requirements pertaining to his/her specific application. Typical configurations include direct conversion, sample and hold then conversion, preamplification, filtering, multiplexing, post processing, pipelining, buffering, error detection, etc. Commercially available

data conversion systems range from basic analog to digital converter on a single monolithic chip to a completely integrated system that includes even a digital processor.

Mixed mode analog/digital circuit represent a new fast growing trend in electronic systems. Circuits combine the properties of both analog and digital units ideally fabricated on the same chip to increase speed and area efficiency. Hence there is a need for a unified fabrication technology for both analog and digital circuits. Due to the present dominance of digital technologies, the architecture of analog circuits must be compatible with these technologies. Typical mixed mode circuits include digital processing units and analog-to-digital converters that link the analog signals to the digital processing power. The fabrication of A/Ds should use the available digital fabrication technologies. The widespread use of MOS technology, with its ability to accurately store and transfer voltages or charge packets, led to the development of analog-integrated circuit techniques in which voltage was used as the active circuit parameter [2].

1.1 MOTIVATION

Analog MOS circuits are becoming increasingly sophisticated in terms of checking and correcting themselves [3]. Self-correcting, self-compensating, or self-calibrating techniques eliminate errors traditionally associated with analog circuits. They eliminate offset and low frequency noise and cancel the error effect [4]. Self-compensating techniques can be used to cancel nonlinearities [5,6]. For real-time applications, however, it is rather difficult to achieve validation of the data generated from A/D converters in the presence of faulty element(s). In general, the validation is accomplished by using an extra D/A converter and an analog window comparator, as shown in Figure 1.1, where a high resolution and accuracy digital-to-analog (D/A) converter is needed [7] and the comparison is performed in an analog manner. Therefore, the validation must highly depend upon the reliability of both the D/A converter and the window comparator. Although their reliability may be im-

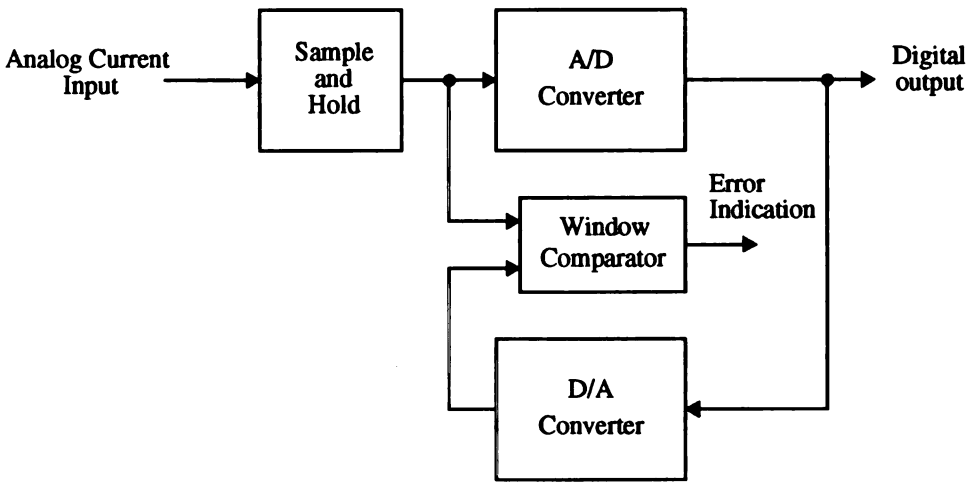


Figure 1.1 Testing of the A/D Converter.

proved by using sophisticated testing schemes to weed out faulty components [8], such off-line or static tests cannot identify the transient faults that occur during on-line operation. It would be preferable for the circuits to be designed such that they will indicate malfunction during normal operation and will not produce an erroneous result without an error indication.

As pressures increase on VLSI designers to use a lower supply voltage of 3.3 V rather than the present 5V, current-mode signal processing techniques will surely become increasingly important and attractive [9]. Current-mode circuits offer two potential advantages: improved dynamic range and improved operating speed [2]. Recently, an algorithmic A/D converter that combines current-mode and dynamic techniques has been presented [10] and some alternative current-mode A/D and D/A converters and their array structures have been studied [11]. These architectures represent an answer to the increasing proliferation of applications requiring larger signal bandwidth such as medical imaging where small differences in image density obtained from digitizing data collected at the scanning receptors are important for diagnosis. The converter does not rely on high gain amplifiers or well-matched components to achieve high resolution and is inherently insensitive to the amplifier's offset voltage. However, the converter is susceptible to faulty switching elements even though mismatched components are allowed.

1.2 PROBLEM STATEMENT

In order to enhance the reliability of data processing systems during real-time operation, a *concurrent error detection* (CED) mechanism is added to the design of a current-mode A/D converter. During manufacturers testing, it is necessary to generate test vectors which when applied to the device under test (DUT) reveal faults. The first question that naturally arises concerns the types of faults that a test experiment is to detect. The fault model considered in this study is the stuck-at-ON/OFF fault at the switching elements of a current-

mode A/D converter. Based on this fault model, the objectives of this thesis are (1) to explore the fault effects of a single faulty switching element, (2) to develop a concurrent error detecting structure for real-time applications and (3) to find a finite set of test patterns that detects all single stuck-at faults at the switching elements during the manufacturing test.

1.3 THESIS ORGANIZATION

This thesis is organized as follows. The next chapter presents necessary background information. The first section deals with the design of A/D converters by introducing some conversion algorithms and their circuit implementation. A distinction is made between voltage-mode and current-mode converters. Section two is concerned with the issue of testing. General definitions and description of testing strategies are included. In particular, concurrent error detection theory is detailed.

In chapter three, current-mode devices where the processed signal is current instead of voltage are described. The basic building cells used in current-mode devices are introduced. The design and operation of an algorithmic current-mode A/D [10] is presented.

Chapter four focuses on the testing of the current-mode converter. First the fault effects are analyzed assuming a single stuck-at fault model at the switching elements. This lead to the generation of a finite set of test vectors that detect these faults. In order to enhance the reliability of the current-mode converter for real-time operation, an alternative converter architecture with concurrent error detection capability is proposed. An analysis of this new converter is carried out.

Finally, the last chapter summarizes the work of this thesis and presents suggestions for future related research.

CHAPTER TWO

BACKGROUND

This chapter introduces two important issues concerning A/D converters: design and test. The design issue is presented as an overview of the conversion algorithms, and their circuit implementation. A distinction is made between voltage-mode and current-mode A/D converters. The subject of testing is first described as a general philosophy. Next, standard and novel test techniques applied to A/D converters are presented.

2.1 DESIGN

There is a vast number of conceivable approaches for A/D conversion. The most popular of these are: successive-approximation, integration, counter and servo, parallel and modified parallel. Each approach has characteristics that make it most useful for a specific class of applications based on speed, accuracy, cost, size and versatility. Because A/D converters have been developed for different applications in various disciplines with little relationship to each other it is rather difficult to establish a unified classification of all known kinds of conversion techniques.

Converters have been manufactured using first discrete components; then hybrid and monolithic technologies. In this section, the circuit techniques used in building A/Ds will be presented with emphasis put on the monolithic processes. Even though designers of monolithic converters have been successful in employing ingenious circuit techniques to achieve a high level of performance, they are still faced with performance limitations im-

posed by the inherent properties of monolithic technologies [12]. These limits will be discussed.

Most of the currently available A/D converters are called voltage-mode A/D converters since the converted data is a voltage signal. A general discussion of voltage-mode converters is included. Recently, a new class of A/D converters, namely current-mode A/D converters, is being developed as an answer to the new challenges faced by the designer of A/D converters. Current-mode A/D converters process current signals instead of voltages.

2.1.1 Conversion Principle

Functionally, a linear electronic A/D converter is a device that accepts an input signal, X_{in}, voltage or current and yields at its output a set of electronic signals representing a numeric code whose magnitude is in proportion to an internal or external reference signal, X_r and the input signal. An ideal A/D converter can be described by a transfer function as shown in Figure 2.1. If the range of input signals is either positive or negative then the converter is described as *unipolar*; otherwise it is labeled as a *bipolar* A/D converter. Since an N-bit binary code can produce only 2^N distinct digital numbers, an N-bit converter also has 2^N quantization levels. In a fixed point digital representation these levels are equidistant and the distance q, denoted by 1 LSB (Least Significant Bit), is referred to as a *quantization step* or *interval.* The smallest quantization step is equal to the full-scale (FS) signal divided by the number of quantization increments, i.e., $FS/2^N$. Hence, even an ideal A/D converter introduces a quantization error bounded between 1/2 LSB, i.e. one half of the smallest quantization interval. The quantization error can be reduced to any desired level by increasing the number of output bits. The quantization error is often referred to as *quantization noise* because for analog signals with sufficient amplitude variation it has a noise-like character. The smallest quantization step, $FS/2^N$, is also referred to as the *resolution* of the converter. The resolution is generally specified assuming an ideal converter; therefore, it does

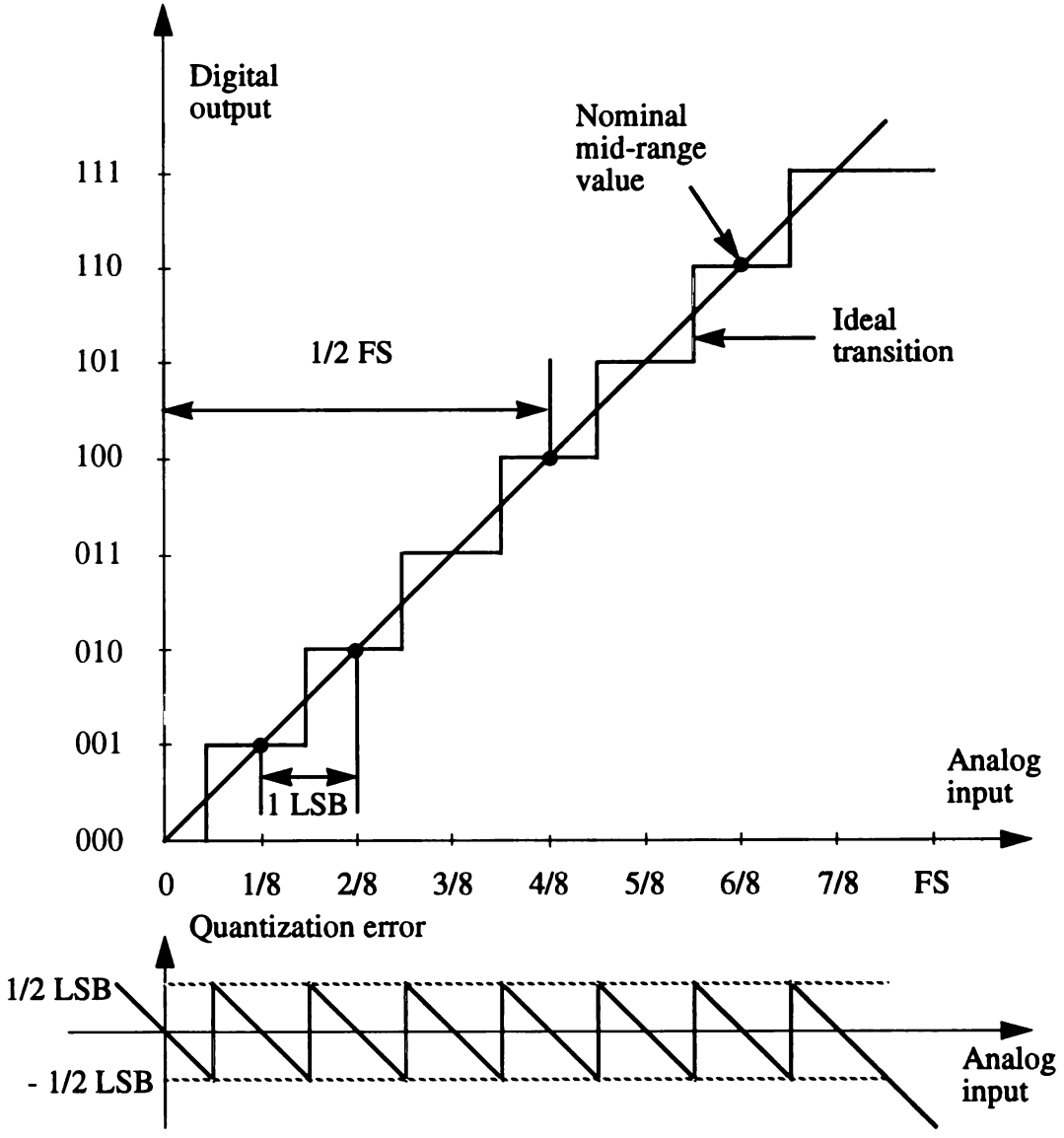


Figure 2.1 Ideal Transfer Characteristic in a 3-bit A/D Converter.

not reflect the actual performance of the converter which may be different due to some parasitic phenomena; e.g. internal noise exceeding the quantization error. Thus the performance of a practical A/D converter should be measured by an "effective-bits" resolution.

The transfer characteristic of an ideal A/D, would be invariant with variations in time, temperature and power supply. It would also be insensitive to interfering electronic and magnetic fields and power supply noise. Thus the ideal A/D converter would have perfect absolute or relative accuracy, linearity, differential linearity, degree of precision, no variance or noise in its output, ultimate stability, total monotonicity, zero offset, no transients, zero settling time, no missing code and would be capable of being updated to accommodate inputs of every frequency range or bandwidth. In practice such an ideal behavior is unattainable and quantitative measures must be introduced to describe practical behavior and assess the different A/D conversion circuits.

2.1.2 Conversion Techniques

Depending upon the speed of conversion, A/D converters are classified under three large groups: high-speed, medium-speed and slow-speed [11].Typical conversion algorithms pertaining to each group are described. It has not been always easy to implement these conversion techniques for a reasonable degree of resolution and accuracy in parts because the processed variables involve a continuum of voltage or current rather than a 0-1 logic.

2.1.2.1 High-Speed A/D Converters

High speed A/D converters are sometimes called video A/Ds since such converters find application in the encoding of composite video signals as required for example in digital television receivers [11]. Parallel or flash converters are the fastest and largest of this

group. Both subranging, pipelined and time interleaved array converters offer a fast conversion rate and a smaller circuit.

Parallel or Flash A/D Converters: A simplified block diagram of a flash A/D is shown in Figure 2.2. Two reference signals can be used thus allowing for greater input range flexibility. The difference between the reference signals, X_{r1} - X_{r2}, is divided into 2^N nominally equal segments thus generating all possible signal quantization levels. Simultaneously, during the same cycle, each of these levels is compared with the input signal X_{in}. If the input signal is higher than the quantization level under consideration, an output bit of 1 is generated; otherwise an output bit of 0 is produced. This "thermometer" like digital code is converted to the desired binary code by an encoder circuit. The main advantage of flash A/D converters is their high conversion rate. However the exponential increase in the number of comparators as a function of resolution limits the practicality of such converters.

Time Interleaved Array A/D Converters: In this structure n identical N-bit A/D converters with S/H stages are connected in n parallel channels Figure 2.3. In each channel, the input signal is sampled and held then converted at a rate of 1/nT. By staggering the S/H stages in time such that the sampling in the second channel is T seconds behind that in the first channel and so on, the input signal can be sampled and held each T seconds by a different A/D converter in the structure. Hence, the overall system achieves a conversion rate n times higher than that of the building A/D subconverter. A buffer and a digital multiplexer stage is used at the output to service the conversion channels one at a time. For high-speed input signals very stable and regular sampling intervals are required. Even a small, deviation from the nominal sampling frequency of 1/nT may cause considerable error since it leads to overlapping the input signals. A high-speed analog demultiplexer can be used to relax the sampling accuracy requirement by converting the analog input signal into n lower-speed sampled and held data signals which are fed into the appropriate sample and hold stage.

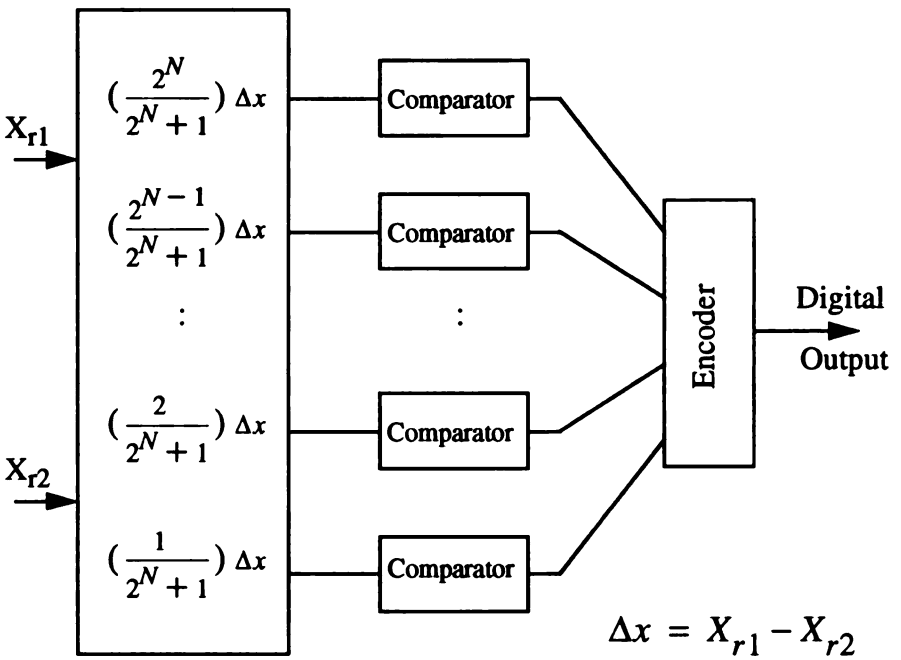


Figure 2.2 Block Diagram of a Flash A/D Converter.

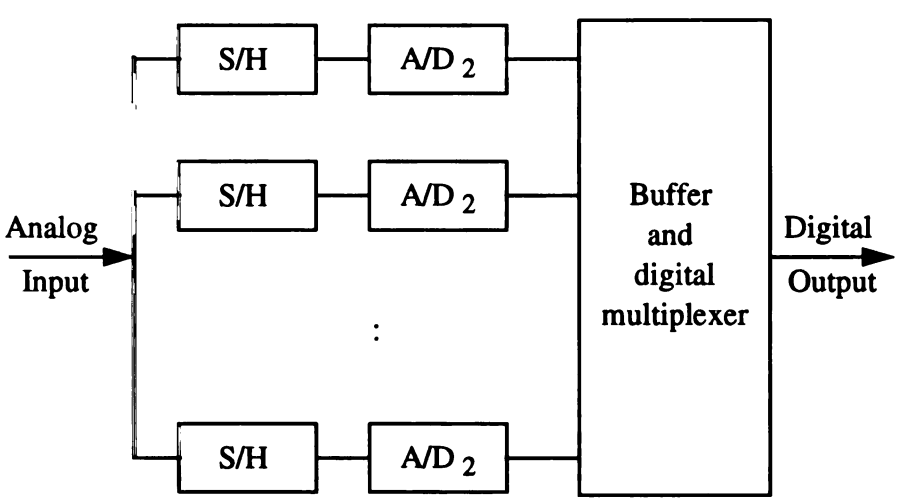


Figure 2.3 Block Diagram of a Time Interleaved A/D Converter.

Subranging and Pipelined A/D Converters: One possible approach to increase the resolution capability and/or to reduce the size and the cost of fast A/D converters is to implement two or more stages of flash converters. Such techniques usually have cascaded structures i.e. the input signal is processed sequentially in consecutive stages.

In a subranging converter, there is no S/H device between the stages and the signal must propagate through all the stages before a new conversion can be started. Figure 2.4 depicts a two-stage subranging A/D converter. The operation consists of two steps. During the first step, a coarse M-bit flash converter gives an approximation of the M most significant bits. In the second step, the fine flash converter gives the least significant bits. The input S/H stage is used to reduce the aperture effect and to optimize the performance.

A general structure of the pipelined A/D converter architecture is shown in Figure 2.5. The pipe consists of m basic stages where each stage consists of a S/H circuit and a low resolution low speed A/D converter. The input signal flows sequentially through successive stages, so the converter produces an N-bit digital word over several sampling periods rather than over one period. The main idea of a pipelined A/D converter is to insert S/H structures between the subconverter stages in order to operate all the stages concurrently thus achieving a high conversion rate which is almost independent of the number of stages. The principal disadvantage of pipelining is the requirement of high speed and high precision S/H structures.

2.1.2.2 Medium-Speed A/D Converters

A slower class in common use is the successive-approximation converter. Cyclic or algorithmic [13] converters are also employed. Both techniques offer a relatively good speed-size performance.

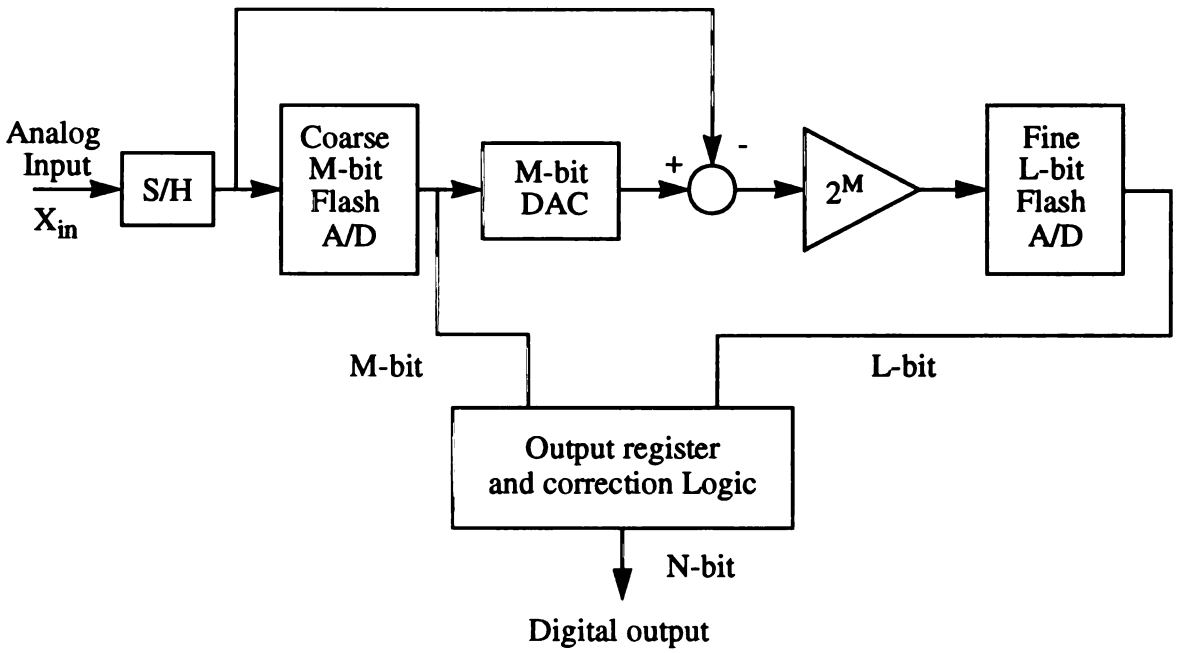


Figure 2.4 Block Diagram of Subranging A/D Converter.

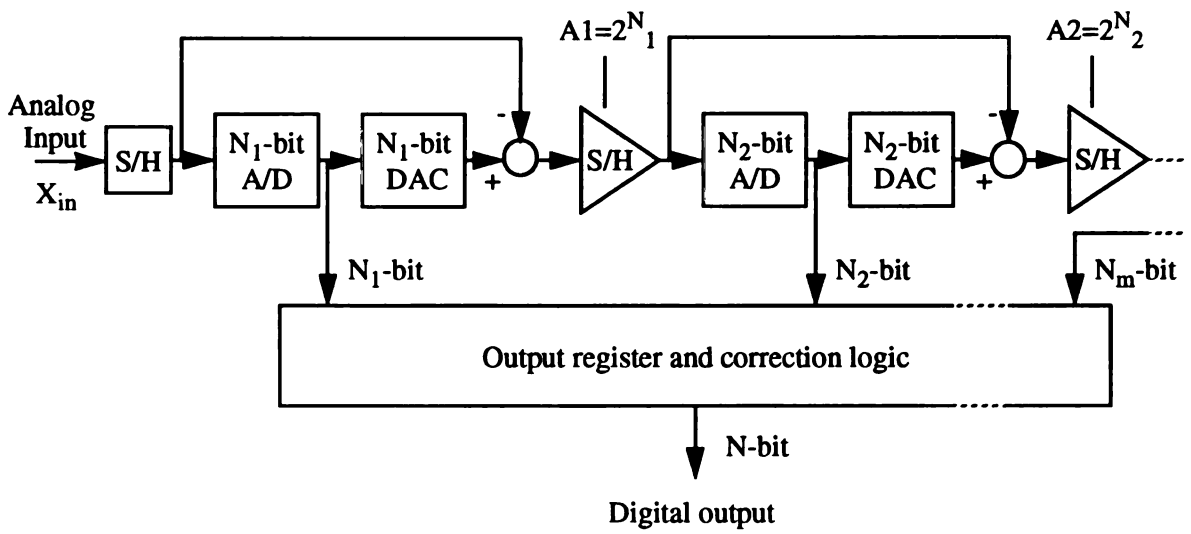


Figure 2.5 Block Diagram of a Pipelined A/D Converter.

Successive-approximation A/D Converters: The successive-approximation A/D converters belong to the class of medium speed converters. Their implementation requires the use of the following building blocks: a S/H stage, a signal comparator, a DAC and a digital control logic often called a successive approximation register (SAR). These building blocks are connected in a feedback arrangement as shown in Figure 2.6. The input S/H stage is used to hold the analog input signal constant during the conversion process.

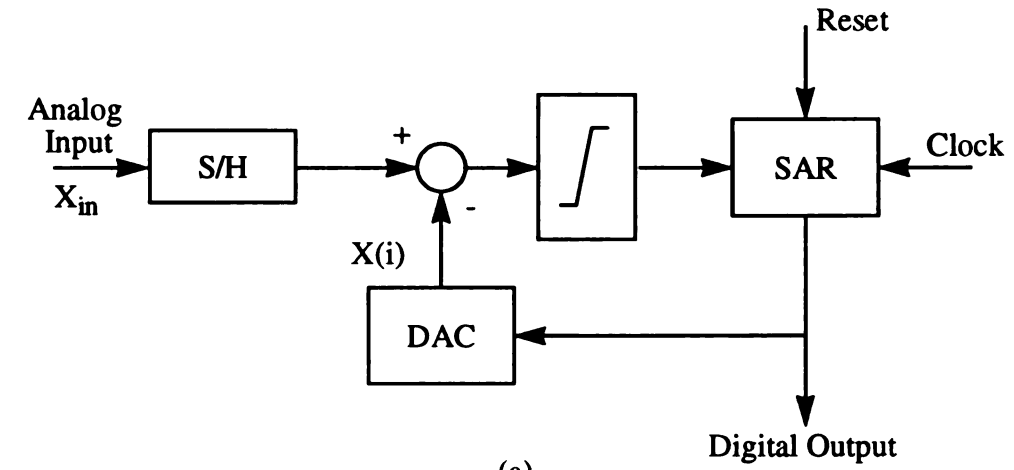
The converter operates on the following principle: after the reset in the first conversion step, the SAR sets the DAC output to $X_r/2$. Hence, the MSB, d_1, is assumed to be one whereas all other bits are set to zero. If the input is higher than $X_r/2$, the MSB is left at one; otherwise, it is reset to zero. In the next step, the DAC output is set to $X_r/2 \pm X_r/4$ where the plus sign is taken if $d_1 = 1$ and the minus sign if $d_1 = 0$. This signal is again compared with the input and the second most significant bit is determined depending on the result of comparison. In the following step, the output of the DAC is to be incremented or decremented by $X_r/8$ and a third comparison is performed leading to d_3. The process continues until all bits of the output word have been determined. Such a converter requires only N clock cycles to complete an N-bit conversion. Mathematically, the algorithm which describes the operation of the successive approximation A/D can be represented as follows:

$$X(k) = X(k-1) - \frac{(-1)^{d_{k-1}}}{2^k} X_r \qquad (2.1)$$

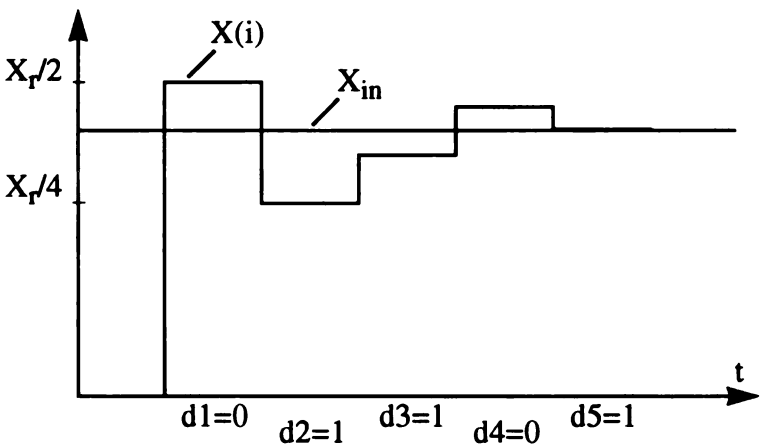
$$d_k = 1 \text{ if } X_{in} > X(k) \text{ and } d_k = 0 \text{ otherwise,}$$

$$X(0) = X_r \text{ and } k = 1, 2,...,N.$$

A bipolar A/D conversion can be achieved by introducing a sign bit d_0 to select either $+X_r$ or $-X_r$.



(a)



(b)

Figure 2.6 (a) Block Diagram of a Successive- Approximation A/D Converter.
(b) Exemplary Voltage Waveform Illustrating the Operation Principle.

Cyclic or Algorithmic A/D converters: The key operations in the cyclic A/D converter are S/H, multiplication by two, subtraction and comparison. Conversion is based on holding the reference signal constant and multiplying the signal to be converted by two during each conversion cycle.

Conversion begins with sampling the input signal, X_{in}, doubling it, then comparing it with X_r in order to generate the MSB d_1. If $2X_{in} \geq X_r$ then d_1 is set to 1, X_r is subtracted from $2X_{in}$ and the difference is multiplied by two. Otherwise, d_1 is set to 0 and X_{in} is multiplied by two. This procedure continues according to the algorithm described by the next set of equations until the desired resolution is achieved.

$$X(k) = 2X(k-1) + (-1)^{d_{k-1}} X_r \qquad (2.2)$$

$$d_k = 1 \text{ if } X(k) \geq 0 \text{ and } d_k = 0 \text{ otherwise,}$$

$$X(0) = X_{in},\ d_0 = 0 \text{ and } k = 1, 2,\ldots,N.$$

2.1.2.3 Low-Speed A/D Converters

High resolution converters can be obtained using one of the described conversion techniques at the expense of costly fabrication technology and/or complicated circuitry. Two alternative techniques achieve high resolution without these burdens. However, the conversion speed is negatively affected.

Integrating Type A/D: Usually the conversion cycle consists of two separate integration intervals. In the first interval the analog input signal is integrated up for a fixed and known period of time T_1. Typically T_1 equals $2^N/f_c$ where f_c is the clock frequency and N is the desired resolution. In the second interval T_2 the reference signal $-X_r$ is integrated down until the integration output returns to zero. The time period T_2 is proportional to the input signal

X_{in}. At the start of conversion, the integrator and the counter are both zeroed. From the above considerations it follows that

$$\frac{1}{T_i}\int_0^{T_1} X_{in}dt - \frac{1}{T_i}\int_0^{T_2} X_r dt = 0 \tag{2.3}$$

where T_i is the integration time constant. Thus we can write

$$\overline{X}_{in}T_1 - X_r T_2 = 0 \tag{2.4}$$

where $\overline{X}_{in}$ is the average value of the input signal. Taking into account that

$$T_1 = \frac{2^N}{f_c} \text{ and } T_2 = \frac{D}{f_c} \tag{2.5}$$

where D is the number of counts in the second interval T_2 we get

$$D = 2^N \frac{\overline{X}_{in}}{X_r} \tag{2.6}$$

The important feature of this result is that the digital number D is independent of the integration time constant T_i and of the clock frequency f_c since these parameters affect both the first and the second interval in the same ratio.

Oversampling A/D Converters: In oversampling A/D converters, the input signal is sampled at a rate much higher than the Nyquist rate; then it is converted to a digital stream in an interpolative modulator. A block diagram of an interpolative A/D converter, a typical class of oversampling A/Ds, is depicted in Figure 2.7. The quantized approximation of the input signal is subtracted from it and the difference is integrated. The integrator in the loop tends to minimize the average difference of the sampled analog input and the quantized approximation. The output of the estimator goes to a digital-low-pass filter which averages and decimates this coarse estimate to get a finer approximation at a lower sampling rate.

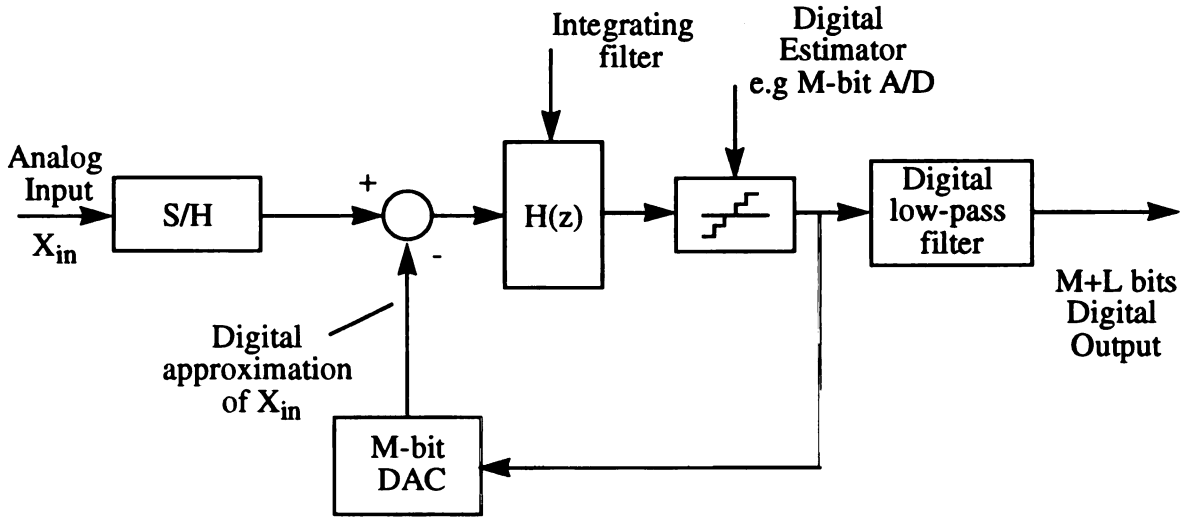


Figure 2.7 Block Diagram of a Interpolative A/D Converter.

2.1.3 Converter Technologies / Converters Microcircuits

This section provides an overview of the circuit technologies used in building A/D converters. Early A/Ds have been of the discrete component type. Later, hybrid and monolithic converters have been developed. Advances in integrated circuit fabrication along with the development of new circuit techniques still contribute to the improvement of monolithic converters.

2.1.3.1 Discrete Component Converters

Early A/D converters were made of discrete components. It was possible to individually select and provide a set of optimal components such that high speed comparators and low temperature coefficient resistors to be used in building the A/D converter. The result was high performance fast and stable converters.

2.1.3.2 Hybrid Converters

One may think of hybrid processing as reducing a printed circuit to the level of a single component producible in large economical quantities. Hybrid circuit design is almost as flexible as proto-boarding except for two limitations. The first limitation is a result of the fact that not all components used in building the converter are available in chip form. The second limitation concerns the number of chips which must be minimized for economical production. Hybrid design is particularly useful when the components to be used are available in technologies that are normally incompatible and can not be integrated in a single chip. Several factors such as availability of low cost chips, development of efficient A/D designs which minimize the used circuitry and production of high precision components contributed to improving hybrid A/Ds.

2.1.3.3 Monolithic Converters

Monolithic converters are generally below discrete and hybrid ones in performance due to the impossibility of fabricating high performance components such as matched capacitors, stable resistors, etc. However, these converters currently dominate the A/D converter field due to their economical production and mostly to the possibility of integrating them as part of the integrated data systems. In general monolithic converters have been fabricated with either bipolar, CMOS or BiCMOS technology.

The bipolar technology is used to fabricate many popular logic families such as TTL and its derivatives. However, there are significant differences in the processes used for linear bipolar circuits and digital bipolar circuits. For example, bipolar digital circuits are generally designed for relatively low breakdowns and high speed. Linear circuits on the other hand, need a wider supply spread in order to accommodate larger signal swings. Achieving an acceptable dynamic range requires higher breakdowns thus dictating larger geometries and leading to lower speeds. Therefore, it is difficult to produce both high precision linear circuits and digital functions on the same chip using either the standard linear bipolar process or digital bipolar process.

An approach that has been successful is the addition of the logic functions to a predominantly linear circuit using the integrated-injection logic (I^2L) process. This allows including reasonably dense logic on the same chip along with high breakdown linear circuitry.

The CMOS technology is superior to other processes in power requirements and packing density. Hence larger conversion systems including a microprocessor are possible. In addition, CMOS offers the A/D designer with a simple and efficient switching subcircuit. Unfortunately, the lack of CMOS low-noise reference sources and gain stages (operational amplifiers and comparators) handicaps this technology. In fact, most CMOS

converters are designed for use with an external reference, since high performance bipolar Zener and bandgap references are available with low drift and noise.

BiCMOS, a generic name applying to several manufacturing processes combines bipolar and MOS transistors on one chip. This process is considered to be the most promising technology for future data converters. It benefits from the advantages of both processes and avoids both of their short coming.

Independent of the particular conversion technique being used, properties of the technology in which the analog to digital converter is implemented place limits on the circuit performance [12]. For example, implementation in CMOS puts limits on the voltage dynamic range and speed of A/Ds. Specifically, the process of sampling and holding (S/H) the converted signal also stores the thermal noise on the S/H circuitry on the holding capacitor. The noise appears as a random variable with a variance equal to $\frac{kT}{C}$, where k is Boltzman's constant, T is the temperature in degree Kelvin and C is the value of the sampling capacitor [12]. As the technologies is scaled down, the capacitance value shrinks and the thermal noise phenomenon represents a limit on the achievable dynamic range per sample. Speed is ultimately limited by the use of a comparator, an essential element in voltage-mode A/Ds. The conversion time is limited by many factors but cannot be shorter than some multiple of the comparator delay.

Monolithic analog to digital converters are at the present time far from the fundamental limits imposed by comparator delay and S/H noise. Presently, performance levels are dictated by practical circuit, technology and packing limitations. Examples include undesired coupling between the analog and digital portions of the circuitry within the converter, charge injection from the switches, offsets in operational amplifiers and comparators, component mismatch and so forth. Perhaps the single most important factor limiting the linearity of those A/D converters which are based on conversion algorithms requiring either a divide or multiply by two scheme is the component mismatch problem. As the converter

resolution increases the effect of mismatching becomes more pronounce. The comparator and/or the operational amplifier's offset is more important in high resolution converters where the per-sample signal is low.

2.1.4 Solutions to Some Limitations on the Performance of A/Ds

During the last few years monolithic A/Ds have improved dramatically in speed and accuracy. These improvements in performance are made possible by new converter architectures and improved semiconductor processes. To obtain matching in components their geometrical size and therefore the area of the circuit has to increase. To overcome this drawback, component adjustment techniques such as laser trimming or thin-film resistor networks have been introduced. Although these methods yield components matched to extremely high precision, they have the disadvantage that extra area is needed for placement of the components to be trimmed or a different substrate has to be used for the passive components [14].

A common way of handling the component matching problem is to develop circuit techniques which eliminate the matching requirement. Two main approaches have emerged. The first consists of improving the currently available voltage-mode converters while the second proposes a novel class of A/Ds i.e. current-mode converters.

2.1.4.1 Voltage-Mode A/Ds

The development of A/D converter circuits was dominated by voltage-mode devices because of the availability of voltage-mode supporting circuitry such as reference generating units, switching circuits, sample and hold circuits, comparators and operational amplifiers, etc. Voltage-mode A/D converters evolved from vacuum tube and resistive ladder implementations to transistor and switched capacitor systems. When faced with perfor-

mance limitations due to mismatching monolithic converter designers have been quite successful in employing circuit techniques such that self-calibration [15], reference refreshing [16], charge balancing, dynamic element matching, ratio-independent converters [17] and digital error correction [18]. Each technique is appropriate for a specific conversion algorithm and a specific implementation of this algorithm. It is worth noticing that most of these techniques pertain to either successive approximation or cyclic A/D converters. As a matter of fact, most of the monolithic A/Ds implement these two algorithms since they represent one of the best approaches to achieving a minimum area A/D which in turn is easily integrated as part of a single chip data processing systems [7].

The self-calibration technique applies to both successive-approximation and cyclic A/D conversion methods. Correction terms are properly added during the normal conversion cycles to cancel the nonlinear effects due to capacitor mismatch. Relatively high resolution is achieved at the expense of increasing the complexity of the control logic for an extra calibration cycle.

In the reference refreshing technique the error is reduced by circulating both the reference voltage and the signal being converted around the loop. This method is not only capacitor ratio independent, it also compensates the error due to non-ideal operational amplifier gain. However, it tends to increase the circuit complexity and the number of tasks to be carried out during each conversion cycle.

Charge balancing and dynamic element matching apply to successive approximation converters by improving the accuracy of the digital to analog converter used as part of the circuit.

The error due to capacitor mismatch can also be improved by using a ratio-independent algorithmic conversion technique. The exact integral multiplication of the signal required by the conversion is realized through an algorithmic circuit method which involves charge summing with an MOS integrator and exchange of the sampling and the integrating

capacitors. A first-order cancellation of the charge injection effect from MOS transistor switches is attained with a combination of differential circuit implementation and optimum timing scheme [14].

Error-compensation A/Ds belong to two general classes. The first class comprises those A/Ds that achieve data accuracy via digital error correction. An example is given in [18] where the concept of variable conversion rate has been used by only allocating longer conversion cycles for the least significant bits and hence minimizing the time overhead introduced for error compensation. The use of both analog and digital circuitry and the extra compensation time are the main disadvantages of these A/Ds. The second class consists of those A/D that use analog circuit schemes and a modified converting sequence where special cycles are allocated for charge redistribution for the purpose of error compensation [19]. Hence compensation involves almost no change to the A/D circuit; however the conversion speed is affected.

2.1.4.2 Current-Mode A/Ds

An alternative approach to the design of A/Ds is to use the current instead of voltage to represent the signal. This approach offers a number of advantages such as improved accuracy, higher sampling rates and reduced chip area. Improvements in accuracy are achieved because the usual problem of switch induced charge injection encountered in voltage based systems has no effect on the signal in current based systems. Improvements in speed can be achieved by reducing the time required for the voltage to settle on the capacitors at the various circuit nodes. The settling time can also be reduced by minimizing the voltage swing required for a given signal dynamic range. This can be done by using CMOS devices always operating in the saturation region where a doubling of the transistor's gate voltage is all that is required to provide a four fold increase in the signal or current level. Since the signal is represented by current, there is no need for a large capacitor array with

its significant charge and discharge times. As a result, the concept of using current to represent the signal in an A/D leads to higher sampling rates as well as reduced chip area. Chapter three expands on the concept of current-mode analog-to-digital conversion.

2.2 TESTING AND VERIFICATION

During the last few years the theory and practice of testing electronic products have changed considerably. The continuing revolution in electronic circuitry in terms of size and speed have increased the problems of testing. In fact, in the field of electronics methods of testing and measurement have always had complex relationship with the products being tested. The technology of testing is bound to exploiting the available technologies of the day to their limits in order to answer the increasing demands for reliability. The philosophy of testing has evolved from merely measuring electrical parameters at many points in the device under test to integrating testing in every step of the device design and development. A whole field of testing has emerged. The following section presents a brief introduction to some important testing concepts.

2.2.1 Testing Techniques

A test is a means by which the existence and quality of certain attributes within a system are determined [20]. The testing of any system or device is vital to achieving high reliability, safety, maintainability, cost effectiveness, fault tolerance, or other design requirements. The testing process attempts to determine if the *device under test* (DUT) works and if it possesses its complete capability. There exists various testing techniques that can be used to achieve this goal. In general testing techniques use two major approaches: *built-in* test and *external* test [20]. External test techniques are typically performed with the DUT removed from its operating environment and various tests applied to it using external equipment. Built-in test techniques usually incorporate testing as part of the design

of the device; thus no external testing equipment is needed. Built-in techniques can follow either a *concurrent* or a *nonconcurrent* approach [20]. Nonconcurrent test techniques require that the operation of the DUT be halted before beginning the test. Concurrent test techniques allow a device to be tested while in normal operating mode.

Whether the test mechanism is built-in or external, three major types of tests are possible: *functional*, *parametric* and *fault* testing. The purpose of functional testing is to verify the functional specifications that the DUT was designed to achieve assuming error free components and proper usage. Parametric testing checks if certain parameters of the DUT are within a required range. Fault testing determines if the DUT suffers from any faults.

Each of these three tests can be performed in either a *static* or a *dynamic* manner [20]. A static test only investigates the steady-state or D.C. characteristics of the device's response. The time response of the DUT overlooked in static tests is used during dynamic testing to evaluate the DUT. A subset of dynamic testing is the at-speed testing where a device is tested at, or above, its normal operating speed.

2.2.2 Test Generation

The test generation process includes fault modeling and reduction, test pattern generation, fault simulation, fault coverage evaluation, and the production of fault dictionary. The first step consists of developing a fault dictionary for the circuit, i.e. modeling the faults that are assumed. Next test vectors and/or test patterns are generated to test for the set of faults being considered. The test patterns are then simulated against the faulted circuit and the fault coverage is evaluated. If the fault coverage is inadequate, the process of test pattern generation and fault simulation are repeated. To be practical and cost effective for large scale integrated circuits, the test generation process should be automated.

Fault modeling is very important in developing cost effective test strategies for electronic circuits. A fault is a physical defect imperfection, weakness, or flaw that occurs with-

in some hardware or software component [20]. A Fault manifest itself as an error(s) i.e. deviation(s) from accuracy or correctness. Many different physical defects can occur in a circuit. A fault model maps this relatively large number of defects into a small number of modeled faults. The selection of adequate fault models is crucial to achieving high quality testing because the efficiency of a test scheme is limited accuracy of the chosen fault model. If the model fails to capture the important characteristics of the actual fault, the test based on this model will fail to detect the actual fault.

For circuits containing switching elements the logical stuck-at model is appropriate, effective and simple to work with. This model is based on two assumptions [20]. The first states that a stuck-at fault results in the circuit responding as if the faulty node is physically connected to 0 or 1. The second assumption is that the basic functionality of the circuit is not affected by the fault. This implies that the circuit continues to behave as expected of it given the existence of the fault.

2.3 TESTING OF A/D CONVERTERS

The revolution in circuit fabrication technology and architectures led to a shift from analog design of electronic systems to all-digital implementations. The decreasing cost of implementing digital solutions and algorithms for data processing, system monitoring and control resulted in rich variety of digital systems. A/D and D/A converters are the answer to linking the analog world of signals to this digital processing power. Applications using converters are found whenever a digital system is used in conjunction with analog data, that is almost everywhere. The properties of the converter to be used for each system are important. Reliability is crucial for some of the converter applications, such as power plant monitoring, medical diagnosis and industrial automation. For example, an erroneous digital data generated by an A/D converter reading the radioactivity level near a nuclear reactor may fail to flag some equipment failure and result in a nuclear catastrophe. Hence, spending

fortunes improving the monitoring processor and the sensing devices will not be enough for a secure plant if the bridge between the controlling tools and the sensors output is defective. Both less dramatic consequences of converter failure and worse ones exists. They all stress the importance of converter reliability and the reliability of any electronic circuit in general. Different strategies can be taken to achieve different level of reliability depending on the device's objective.

2.3.1 Functional and Parametric Testing

Functional and parametric tests check the design and specifications of the DUT. In the case of A/D converters, these tests answer the following questions: does the DUT provide good A/D characteristics and what are the restrictions and properties of the used components that are detrimental to the performance of the A/D converter? The first step in performance evaluation consists of generating the transfer function of the A/D converter i.e. for an N-bit resolution A/D converter finding 2^N transition points. Next, the transfer function of the A/D converter is tested for offset error, gain error, differential linearity and integral non-linearity. These errors reflect either a bad design, too many non-idealities, or a wide tolerance in the fabrication process. Several test methods such as Crossplot and ATE are known for voltage-mode converters [7]. Current-mode converter represent a relatively novel architecture without any well known functional and/ or parametric test procedures.

Functional and parametric tests are crucial for the designer in proving the merit of a given A/D conversion architecture. An A/D converter passing such test(s) is expected to operate within its intended specifications. In fact, the investigated specifications determine the converter's usefulness for specific applications.

2.3.2 Fault Testing

Proving the correctness of an A/D converter can be achieved by functional and parametric test types. However, in general, the success of these tests does not guarantee that the A/D will operate correctly thereafter. In fact, faults may occur only after the device has been used for a period of time. Also the effect of some faults may only appear during device operation. In addition the device may be fault free and still fails to function correctly due to misuse. Parametric and functional tests perform design verification; however, fault testing aims at fault immunization i.e. monitoring device reliability. This work approaches reliability at the level of data validation. Hence its objective is to achieve an A/D conversion circuit that does not produce erroneous output data without indicating that it is erroneous. The error flag does not give any information about the occurring fault and no mechanism has been devised to retrieve the correct data. There exist several techniques for designing and or modifying electronic circuits providing them with data validation capabilities i.e. with fault tolerance properties. On-line *concurrent error detection* (CED) methods achieve such a goal. *Built-in concurrent error detection* avoids several difficulties involved with external testing of analog circuits, such as loading by the test equipment. Moreover, this strategy solves the problem of existing disparity between the testing equipment and the DUT. Concurrent error detection is implemented by slightly modifying the topology of the current-mode A/D. The new A/D architecture possesses a built-in concurrent data validation mechanism.

2.3.3 Concurrent Error Detection

All CED schemes detect errors through conflicting results generated from operations on the same operands. CED can be achieved through space or time redundancy, or space/time hybrid redundancy [21-27]. Time redundancy employs only one single set of hardware to carry out the repeated operations. Since the same hardware is used, the repeated opera-

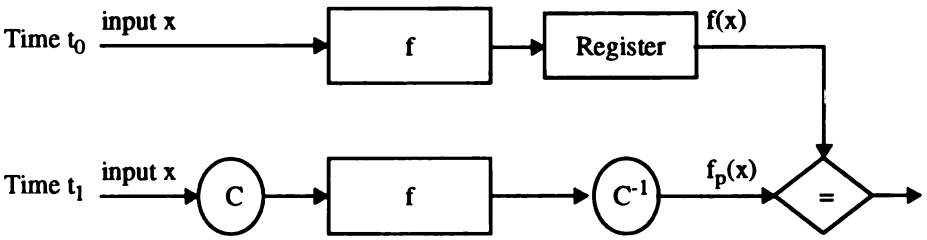


Figure 2.8 The Concept of Time Redundancy.

tion, in the presence of faults, is liable to produce the same erroneous result as that of the first step. To avoid this problem, the operand must be coded in the repeated cycle. The result thus obtained must be decoded back to the appropriate form for meaningful comparison. Two simple time redundancy techniques have been reported: RESO (*REcomputing with Shifted Operands*) [21,24,25] and AL (*Alternating Logic*) [26,27]. Among existing CED techniques, both RESO and AL have unique features of transient fault detection and require only a moderate increase in hardware.

Consider a time redundancy technique shown in Figure 2.8 [21]. Let x be the input of the computation unit f and let $f_p(x)$ and f(x) be the outputs with and without encoding-decoding operations, respectively. Two fundamental requirements must be satisfied in these operations. First, the coding function c must not interfere with the original function f. In other words, for a selected coding function c, there must exist a decoding function c^{-1} such that

$$f_p(x) = c^{-1}(f(c(x))) = f(x) \tag{2.7}$$

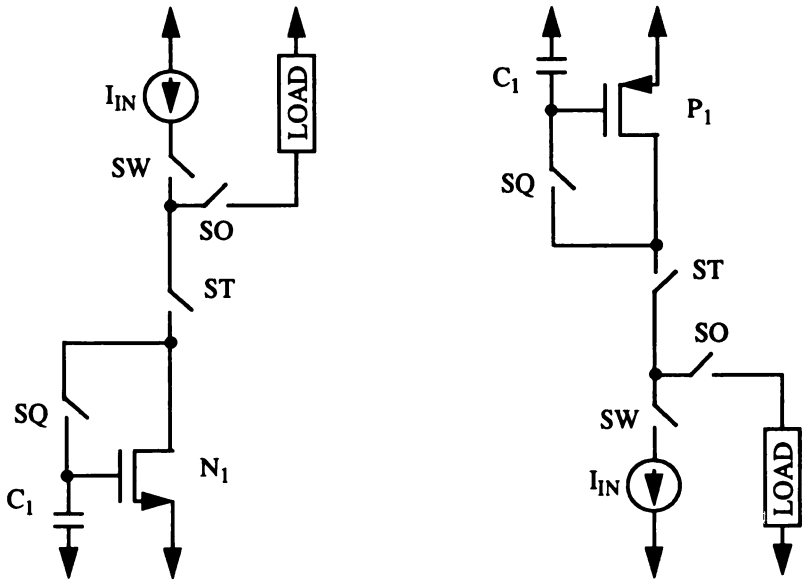
in the absence of faults. This is the concept of *mappable correct output* [24]. Secondly, for the purpose of fault detection, the coding operation c must transform the input operand(s) x in such a way that when subjected to the same faulty conditions, the output in the repeated step, though still erroneous will be different from the first step. This is the concept of *disjoint error sets* [24]. AL implementation uses the complementation operator as the encoding function, i.e., the application of an input x followed by the complemented input $\bar{x}$, produces outputs that are bitwise complements. Any noncomplemented bit indicates an error. If the produced outputs are N-bits then, even when assuming a fault probability of one, the probability of a fault going undetected is equal to $1/2^N$.

CHAPTER THREE

CURRENT-MODE A/D CONVERTERS

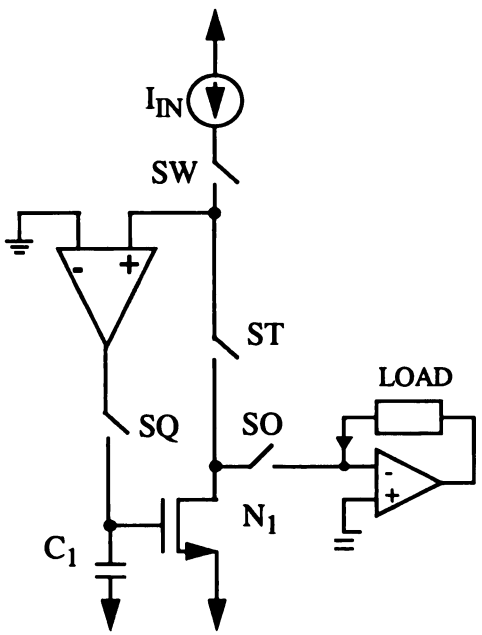
Current-mode techniques in which circuits use current as the processed signal offer two main advantages: improved dynamic range and improved speed. Due to the non-linear I-V relationship characteristic of most transistors, a small change in the controlling voltage results in a much larger change in the output current. Consequently, for a process with a narrow voltage range, the corresponding current range is much larger. Since a change in current level flowing through any node is not necessarily accompanied by a change of voltage at that node, or at least by a smaller change of voltage at that node, the circuit's speed will not be degraded by the need of charging or discharging the parasitic and/or actual capacitances present in the circuit. In addition to these two inherent advantages, current-mode devices offer auxiliary benefits such as simpler circuitry and lower power consumption [2]. These properties made current-mode techniques appealing for usage in a wide variety of signal processing circuits.

This chapter describes the detailed design and operation of a current-mode A/D converter with dynamic current techniques [10], where the basic building blocks of such a circuit are NMOS and PMOS current copiers. In general NMOS and PMOS current copiers are each used to precisely memorize unidirectional currents. In this study, a new CMOS bipolar current copier is introduced.



(a)

(b)



(c)

Figure 3.1 Current Copiers .
(a) NMOS Copier. (b) PMOS Copier. (c) NMOS Copier with Op. Amp.

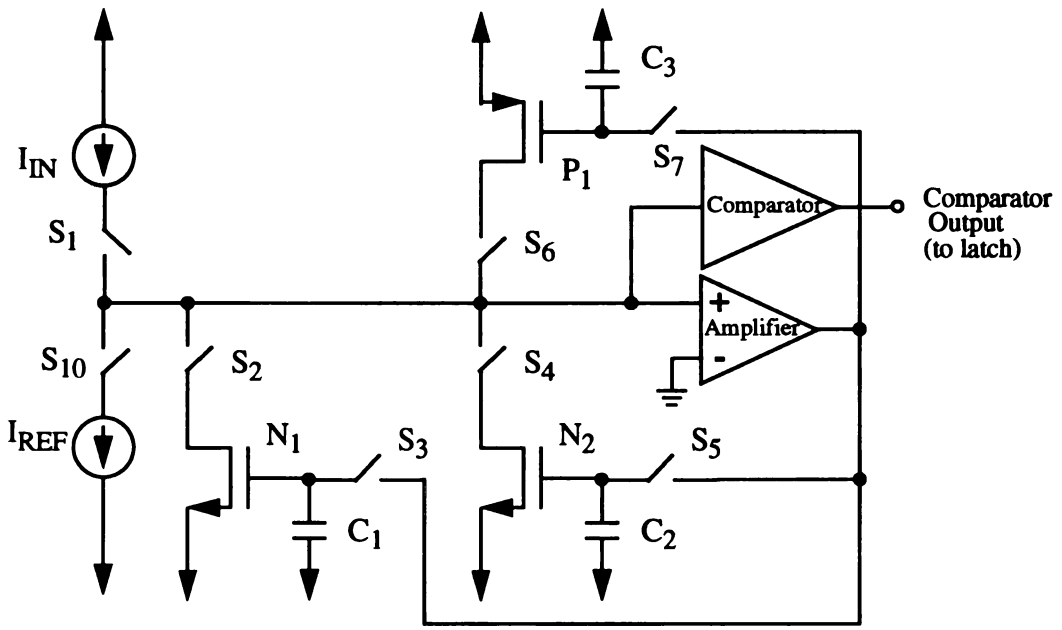
3.1 CURRENT COPIERS

The basic current copier cell, as shown in Figure 3.1(a) [28,29], referred to as a *simple NMOS current copier*, consists of three non-critical components: a switch, an enhancement-mode NMOS transistor and a capacitor.To copy the current I_{IN} into the NMOS current copier, as shown in Figure 3.1(a), switches S_Q, S_T and S_W are turned on; the capacitor will charge up to the gate voltage needed by the transistor to achieve a drain current equal to I_{IN}. S_W is then turned off to disconnect the cell from the current source; thereafter, the cell is capable of sinking a current I_{IN} when connected to a load [28,29]. For currents in the reverse direction, the simple PMOS current copier shown in Figure 3.1(b) is operated in the same manner.

Clock feedthrough, leakage and channel length modulation limit the accuracy of the copied current [28,29]. Thus, the stored current will differ from the original source current and will in general have some dependency on the component matching. For example, due to channel modulation, the simple current copier will not work properly if the drain to source voltage V_{DS} of the transistor during current copying is not the same as that during use of the cell's copy. An op-amp can be used to fix the drain voltage during both copying and read out as illustrated in Figure 3.1(c) [28,29]. S_Q, S_T and S_W are switched on during copying; while S_O is switched on during read out.

3.2 CURRENT MATCHING A/D CONVERTER DESIGN AND OPERATION

The current-mode digital signal processing techniques have surely become increasingly important and attractive as pressures increase on VLSI designers to use a lower supply voltage of 3.3 V rather than the present 5V [9]. Recently, both NMOS and PMOS current copiers have been implemented in the design of current-mode A/D converters [10] which do not rely on high gain amplifiers or well-matched components to achieve high res-



(a)

	MSB	previous bit = 1	previous bit = 0
S_1			
S_2			
S_3			
S_4			
S_5			
S_6			
S_7			
S_8			
Latch			
Reset			

(b)

Figure 3.2 Current-Mode A/D Converter.
(a) Schematic Diagram. (b) Switching Sequence.

olution and are inherently insensitive to the amplifier's offset voltage. In order to speed up the conversion time, while still keeping the converter circuit simple, a current-mode A/D converter has been proposed [10] in which the following recursive conversion algorithm was employed,

$$I_{k+1} = I_k - q_k I_{REF}/2^{k+1};\ k=0,1,...,N-1 \tag{3.1}$$

where $I_0=I_{IN}$, $d_0=1$, $q_0=1$, and

$$q_k = \begin{cases} 1 & \text{if } d_k=1, \text{ i.e., } I_{k+1} \geq 0, \\ -1 & \text{if } d_k=0, \text{ i.e., } I_{k+1} < 0. \end{cases} \tag{3.2}$$

The bit values of d_k and q_k are determined by the polarity of the current I_{k+1}

Figure 3.2 shows the schematic circuit diagram of the current-mode A/D converter [10]. The converter is comprised of two NMOS current copiers, one PMOS copier, an op-amp, and a current comparator. The converter starts converting for the *most significant bit* (MSB) of an input current I_{IN} by first switching on S_1, S_2, and S_3 to cause the current in N_1 to be set to I_{IN}. Once N_1 is set, S_2 and S_3 are switched off while S_4 and S_5 are on to copy I_{IN} to N_2. Once the input signal has been stored in N_1 and N_2, twice the input signal is loaded into P_1 by turning off S_1 and S_5 while switching on S_2, S_6, and S_7. After P_1 is set, S_2, S_4 and S_7 are turned off while S_{10} is turned on, thus allowing the comparator to sense the current imbalance and hence determine if the signal, $2I_{IN}$, is greater than I_{REF}. If the signal exceeds the reference, the MSB will be a "1" otherwise it will be a "0." This completes the conversion for the MSB. The current comparator, Figure 3.3, operates as follows: the current imbalance flows through the large equivalent gate to source input impedance presented by the CMOS structure, the resulting drain voltage reflects the current direction.

The remaining (N-1) bits are then converted in the same manner. The signal held in P_1 is loaded to N_1 by turning on S_6, S_2 and S_3. If the preceding bit was a "1," S_{10} is also turned on to subtract the reference from the signal in P_1. On the other hand, if it was a "0,"

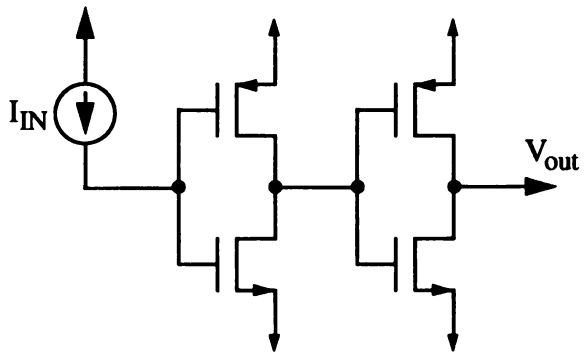


Figure 3.3 A Simple Current Comparator.

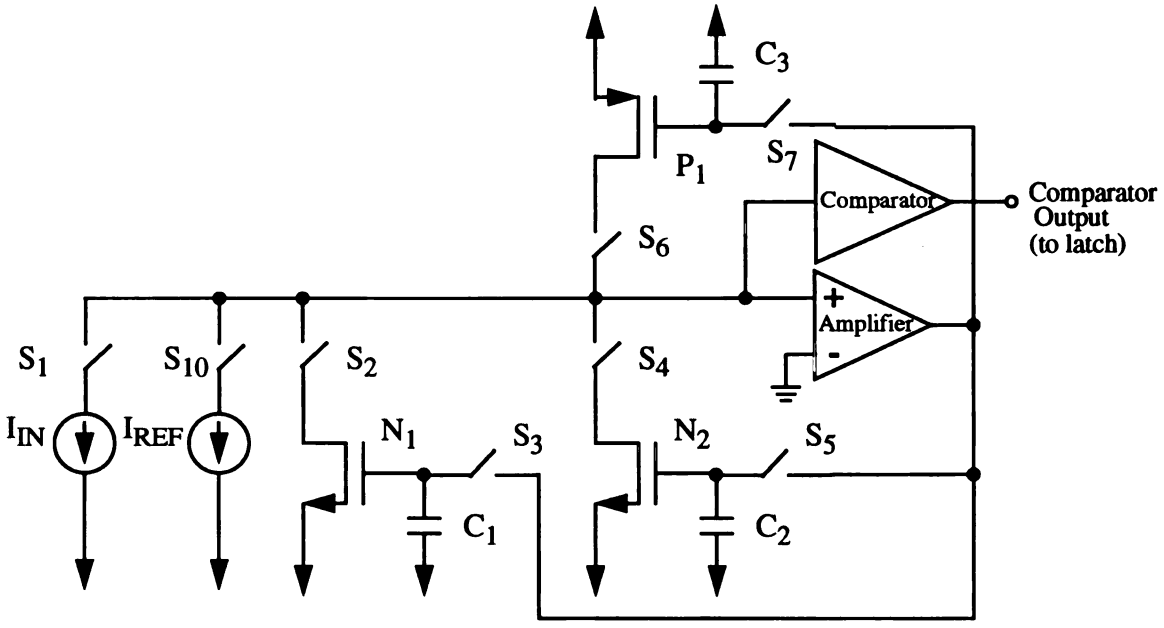


Figure 3.4 Modified Current-Mode A/D Converter.

S_{10} is off so that the signal remains unchanged. Once N_1 is set, N_2 is set by the same procedure. The signal is then doubled and stored on the gate of P_1. Finally, it is compared with the reference. This sequence is repeated until the desired resolution has been achieved; an end of conversion pulse is then generated to signal the end of conversion. The converter needs 4N clock cycles for an N-bit data conversion.

An extensive discussion of the limitations and the practical design issues involved in implementing the described current matching A/D converter is presented in [30]. The prototype circuit has been fabricated using a 3-μm CMOS technology. It achieved a resolution of 10 bits with a maximal sampling rate of 25 KHz, or 40 μsec conversion time, a power consumption of only 3.5 mW and an area of $0.32mm^2$. The power supply was +5V and the reference current was 100μA. The gain error at full scale was -2.29 LSB and the offset error was equal to 0.03 LSB. The integral nonlinearity varied between ± 0.92LSB, while the differential nonlinearity was bound between 0.10LSB and -0.87LSB.

It should be mentioned that, since the input current is needed during the first two clock cycles for converting the MSB, a sample-and-hold (S/H) circuit is required for the input current [10]. However, the S/H circuit can be omitted by holding the input I_{IN} in P_1, where the polarity of the input current is changed as shown in Figure 3.4.

3.3 CMOS CURRENT COPIER

Consider the current-mode A/D converter in either Figure 3.2 or Figure 3.4. In the presence of a stuck-at-ON fault at S3 (S5) and during the copying of the current held in N_1 (N_2) to P_1, the CMOS structure N_2-P_1 (N_1-P_1) act as the copier.

Conventional NMOS and PMOS copiers can be used for memorizing only input currents that flow in the same direction as the drain current. To accommodate applications where currents in both directions are present a CMOS current copier is designed. Experi-

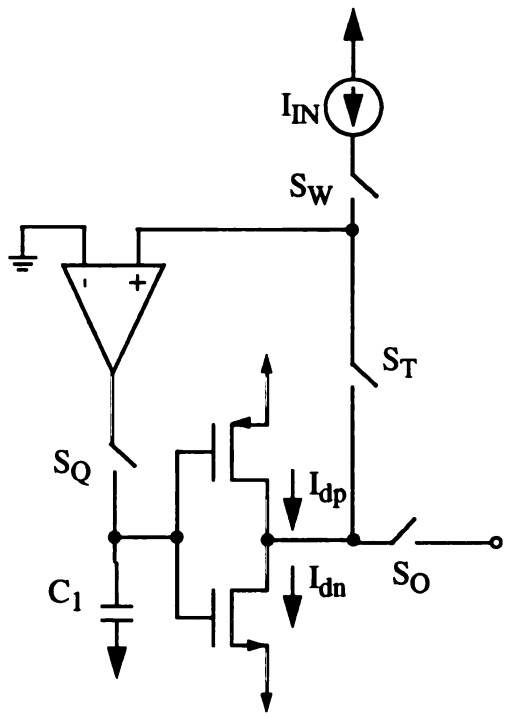


Figure 3.5 CMOS Copier Where $I_{IN} = I_{dn} - I_{dp}$.

mental and simulation results show that the proposed copier can precisely memorize bipolar input currents within a specific range

Figure 3.5 shows the proposed CMOS current copier with op-amp, where the dual power supplies ±2.5V are employed. During the copying, both switches SW and SQ are turned on; the capacitor will charge up to the gate voltage needed by both NMOS and PMOS transistors to achieve a current equal to the input current $I_{IN}=I_{dn}-I_{dp}$, where I_{dn} and I_{dp} are the drain currents of the NMOS and PMOS transistors, respectively. If the polarity of the current I_{IN} is positive, then $I_{dp} < I_{dn}$, otherwise $I_{dp} > I_{dn}$. Note that $I_{dp}=I_{dn}$ if $I_{IN}=0$. The op-amp is used to force the drain voltages of both transistors to be zero so that they are operating at the saturation region. After the copying, switches SW and SQ are turned off to disconnect the cell from the input current source and then the cell is ready to source or sink current when connected to a load. When switch ST is turned on, the op-amp again forces the drain voltages of both transistors to be zero and ensures that both transistors are operating at the saturation region and thus the proper current can be extracted.

A prototype CMOS current copier, which is comprised of a CD4007 dual complementary pair chip and a μA741 op-amp, has been implemented. The experimental results are plotted in Figure 3.6(a), where the capacitance C=46.035pF and the applied input currents range from -2.2mA and +2.2mA. Both drain currents I_{dn} and I_{dp} are measured by two current meters. Since both PMOS and NMOS transistors in the CD4007 chip have virtually the same device transconductance parameters k=k'(W/L), the plot is nearly symmetrical. Results show that I_d=2.0mA and I_{dn}=0mA if I_{IN}=-2.0mA; I_{dp}=1.18mA and I_{dn}=0.08mA if I_{IN}=-1.10mA; $I_{dp}=I_{dn}$=0.49mA if I_{IN}=0mA; I_{dp}=0.06mA and I_{dn}=1.15mA if I_{IN}=+1.09-mA; and I_{dp}=0mA and I_{dn}=2.0mA if I_{IN}=2.0mA.

For reliable operation of the copier it is necessary that the PMOS and NMOS transistors be operating either at the saturation region or at the cutoff region depending upon the relationship between the power supplies and the threshold voltage difference (V_{tn}-V_{tp}), the

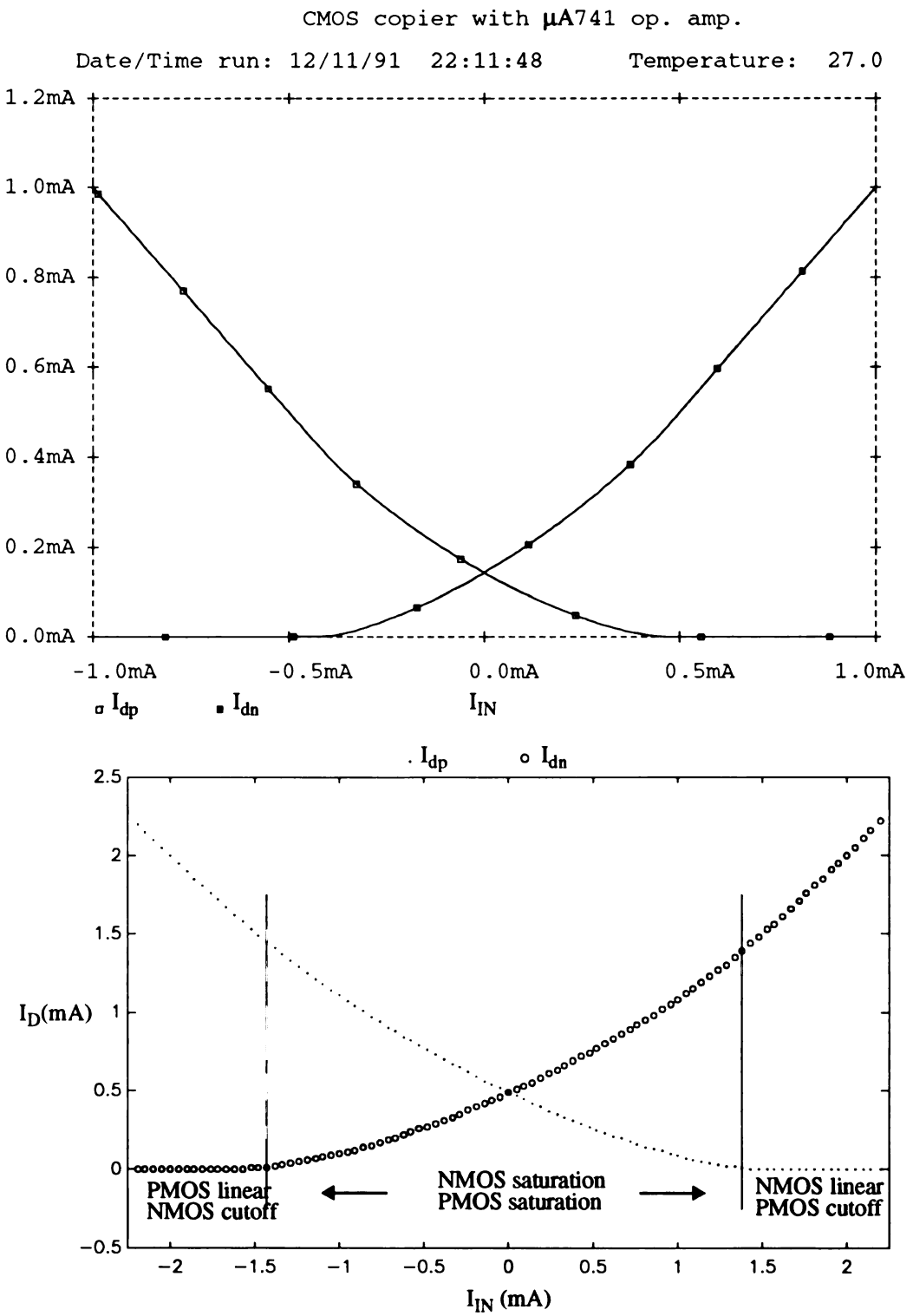


Figure 3.6 (a) Pspice Output. (b) Experimental Output.

input currents can be improved by increasing the aspect ratios $(W/L)_n$ and $(W/L)_p$, as shown in (2) and (3), but at the cost of larger chip area.

3.4 SUMMARY

The presented current-mode A/D has a number of features that make it attractive for designers of VLSI systems. Its favorable speed/area trade-off makes it well suited for use in large signal processing systems. Further circuit refinements should allow better performance. For example, speed can be quadrupled by using a pipelined architecture. Special attention should be given to minimize errors inherent to the current copier cell. Inevitable circuit nonidealities will cause the current retrieved from the cell to differ from the copied current. Mechanisms of error include switch charge feedthrough, limiting the initial accuracy of the current sample; channel length modulation, producing a change in the retrieved current as the voltage VDS changes; junction leakage, associated with the resistance of the switch in the off state causing a steady discharge of the storage capacitor; and 1/f and thermal noise, limiting the accuracy of the current sample and varying the current during retrieval [31]. Circuit techniques for reducing these errors range from proper choice of the parameters of the circuit components to altering the circuit's topology as in the case of adding an operational amplifier.

CHAPTER FOUR

TEST GENERATION AND CONCURRENT ERROR DETECTION

The objective of this chapter is first to address the fault effects and test generation of the current-mode A/D converter proposed in [10], where the single stuck-at fault model is assumed for switching elements. Further, in order to enhance the reliability of A/D converters for real-time operations, an alternative current-mode A/D converter with CED capability is proposed to detect transient and permanent faults.

4.1 FAULT MODEL AND FAULT EFFECTS

Although mismatched components are allowed in the converter of Figure 3.4, the converter is still susceptible to faulty switching elements. Any faulty switching element may result in an incorrect converted data. The single stuck-at fault model, commonly employed for digital test generation, will be used. In this implementation, it is assumed that only one faulty switch occurs at a time and the faulty switch is permanently stuck-at ON state (*S/ON*) or OFF state (*S/OFF*). In general, the faults may be caused by either a malfunctioning clock generator, i.e., one bit may be permanently stuck-at-1 (or 0) causing the controlled switch to be *S/ON* (or *S/OFF*), or by malfunctioning transistor switches.

The analysis of the faulty switches in the converter of Figure 3.4 revealed that the fault effects can be classified into three types: Type 1 fault effect occurs when the faulty switch results in the same conversion output regardless of the values of the input current.

Switches S_1, S_2, S_4, S_7, and S_{10} being *S/ON* and S_1, S_2, S_4, S_6, and S_{10} being *S/OFF* illustrate this fault behavior; Type 2 occurs when the faulty switch renders the conversion output dependent on the initial condition of the active capacitors. Switches S_3, S_5, S_7 lead to this condition when *S/OFF*; and Type 3 faults make the result of the conversion process dependent on the CMOS structure P_1/N_1 (or P_1/N_2) when S_3 (or S_5) is being *S/ON*. Throughout the next analysis, I_{P1} (I_{N1}, or I_{N2}) will denote the current held in P_1 (N_1, or N_2)

4.1.1 Type 1 Fault Effect

Consider the case when S_1 or S_6 is *S/OFF*, the input current will not be copied into P_1; this is effectively equivalent to an input current of zero. Consequently, the conversion process results in a string of zeros. When S_2 (S_4) is *S/OFF*, the input current in P_1 will never be doubled. In fact, S_2 (S_4) being open circuited results in N_1 (N_2) contributing zero current to P_1 during the copying of the sum current $I_{N1}+I_{N2}$. Hence the comparison of current in P_1, i.e., I_{IN}, and I_{REF} always results in a zero bit. S_{10} being *S/OFF* leads to the current in P_1 being compared to zero instead of I_{REF}. Hence conversion results in a string of ones. When S_1 is *S/ON*, P_1 gets the input current; however when P_1 is being copied into N_1 (N_2), N_1 (N_2) gets the difference current $(I_{P1}-I_{IN})=0$. The comparison of I_{P1} $(=I_{N1}+I_{N2}+I_{IN})$ and I_{REF} produces a zero MSB. Next, instead of P_1 being copied into N_1, the zero current difference $(I_{P1}-I_{IN})$ is copied into N_1. Hence conversion results in a string of zeros.

At the end of every conversion, the capacitors are left charged. This charge represents the last current that has been copied into the corresponding transistor. Since N_1 and N_2 copy either the current I_{P1}, when $I_{P1} < I_{REF}$, or the current difference $(I_{P1}-I_{REF})$, when $I_{P1} > I_{REF}$, the current in the corresponding NMOS, at any instant, is bounded between zero and I_{REF}. If S_2 is *S/ON*, both the initial current I_{N1} and the input current I_{IN} will be copied to P_1, i.e., P_1 gets $I_{IN}+I_{N1}$. Then P_1 is successfully copied into N_1. However, when P_1 is being copied into N_2, the current in N_1 is subtracted from it resulting in copying zero current into

N_2. Hence the current in P_1, will not be doubled. During the comparison phase, the comparator senses the unbalanced current, $-I_{REF}$, from P_1, N_1, and I_{REF}. Thus, a zero bit always results. Similarly, when S_4 is *S/ON*, a string of zeros is generated.

While comparing P_1 and I_{REF} with S_7 being *S/ON*, P_1 will first copy I_{REF} due to S_7 being ON. At the end of the comparison cycle, the difference between $I_{P1}=I_{REF}$ and I_{REF} will be compared leading to a conversion bit of 1. This scenario is repeated for all conversion bits. Thus, a string of ones results.

4.1.2 Type 2 Fault Effect

When S_3 is *S/OFF*, the transistor N_1 cannot copy any current because the capacitor C_1 has no charging path. Thus, N_1 will retain the current it has copied prior to the occurrence of the fault. This current will be held constant since the capacitor can only leak its charge through the gate to source impedance. In the presence of such a fault, conversion proceeds as follows: I_{IN} is copied into P_1; P_1 copy to N_1, but N_1 still holds the constant current I_x; P_1 is copied to N_2; P_1 gets $I_{N1}+I_{N2}$, or I_x+I_{IN}; finally, the current held in P_1 is compared to I_{REF} and the proper conversion bit results. Similarly, the *S/OFF* faulty switch S_5 has the same fault effect. When S_7 is *S/OFF*, the transistor P_1 cannot copy any current. Thus, the constant current in P_1 is compared to I_{REF} for the output.

4.1.3 Type 3 Fault Effect

In the presence of *S/ON* faulty switch S_3, conversion starts off with successfully copying I_{IN} into P_1; P_1 into N_1, and P_1 into N_2. Then, instead of copying $I_{N1}+I_{N2}$ into P_1, N_2 will source its current I_{IN} to the CMOS structure, comprised of P_1 and N_1, due to S_3 being *S/ON*. Since the current copied in the CMOS structure is positive P_1 ends up with a positive current greater than or equal to the current supplied by N_2 ($=I_{IN}$). The conversion proceeds

such that at the end of the k^{th} cycle the currents in the transistors P_1 and N_1 are given by the following recursive formula:

$$I_{P1}(k) - I_{N1}(k) = I_{P1}(k-1) - d(k-1) * I_{REF} \quad (4.1)$$

$$I_{P1}(k) = K'_p (1/2) (W/L)_p (V_G(k) - V_{DD} - V_{tp})^2 \quad (4.2)$$

$$I_{N1}(k) = K'_n (1/2) (W/L)_n (V_G(k) - V_{ss} - V_{tn})^2 \quad (4.3)$$

$$d(k) = 1 \text{ if } I_{P1}-I_{REF} \geq 0 \text{ and } 0 \text{ if } I_{P1}-I_{REF} < 0. \quad (4.4)$$

where $k = 1, 2,...,N$, $I_{P1}(0) = I_{IN}$, $d(0) = 0$, $d(k)$ is the k^{th} conversion bit, $V_G(k)$ is the common node voltage at the gate of P_1 and N_1 during the k^{th} cycle and K'_p, V_{tp}, $(W/L)_p$, K'_n, V_{tn} and $(W/L)_n$ are the parameters of the respective P and N transistors. Similarly, the *S/ON* faulty switch S_5 has the same fault effect.

4.2 TEST GENERATION AND FAULT COVERAGE

According to the fault effects discussed previously, in the presence of a Type 1 fault, i.e., *S/ON* faulty switch S_1, S_2, or S_4, or *S/OFF* faulty switch S_1, S_2, S_4, or S_6, conversion results in a string of zeros. Thus, any nonzero input current can detect such a fault. Similarly, in the presence of *S/ON* faulty switch S_{10} or *S/OFF* faulty switches S_7 or S_{10}, conversion results in a string of ones. Thus, a zero test current can detect the fault.

For Type 2 fault effect, in the presence of *S/OFF* faulty switch S_3, transistor N_1 cannot copy any current because there is no charging path to the capacitor C_1. In fact, N_1 retains the current it has copied prior to the occurrence of the fault. This current referred to as I_x remains almost constant since C_1 can only leak its charge through the high gate to source impedance of the transistor N_1. Consequently, the current held in P_1 in the step is equal to $I_{IN}+I_x$. Two test currents, $I_{IN}=0$ and I_{REF}, can detect such a fault for any value of I_x. Specifically, for $I_{IN}=0$, during the MSB conversion, the comparison of I_{P1} $(=I_{IN}+I_x=I_x)$

and I_{REF} generates a zero MSB except when $I_x=I_{REF}$. During the k-th bit conversion, $I_{P1}=-kI_x$ generates a zero bit except for $I_x \geq I_{REF}/k$. Hence the conversion of $I_{IN}=0$ generates at least one nonzero bit in the k-th bit position. The result of conversion follows the general pattern of 0...1xxx, and the first nonzero bit detects the fault. On the other hand, for $I_{IN}=I_{REF}$, the comparison of I_{P1} ($=I_{IN}+I_x=I_{REF}+I_x$) and I_{REF} leads to an MSB of 1. The k-th comparison involving $I_{P1}=kI_x$ and I_{REF} produces a one bit except $I_x \leq I_{REF}/k$. Hence the result of conversion follows the pattern 1...0xxx i. e. the result contains at least k zero bits after MSB where k is the smallest integer such that $kI_x < I_{REF}$. The first occurrence of a zero bit detects the fault. This concludes that these two test currents can detect the fault regardless of the value of I_x. Similarly, these two test currents can detect the *S/OFF* fault on switch S5. Consider the presence of *S/OFF* faulty switch S_7, the fault effect shows that the current, I_y, copied in prior to the fault will not change. During normal non-faulty conversion P_1 copies either $I_{IN} \leq I_{REF}$, $2I_{IN} \leq 2I_{REF}$, or $2I_z \leq 2I_{REF}$ where $I_z = I_{P1}$ if $I_{P1} < I_{REF}$ and $I_z = I_{P1}-I_{REF}$ if $I_{P1} \geq I_{REF}$. Thus the constant current I_y held in P_1 is bounded between 0 and $2I_{REF}$. Thus, the above two test currents, namely 0 and I_{REF}, can also detect the fault. More specifically, $I_{IN}=0$ and $I_{IN}=I_{REF}$ detect the fault in cases $I_y < I_{REF}$ and $I_y \geq I_{REF}$, respectively.

For Type 3 fault effect, in the presence of *S/ON* faulty switch S_3, the transistor N_2 will source its current I_{IN} to the (P_1/N_1) CMOS structure. This results in $I_{P1}-I_{N1}=I_{N2}=I_{IN}$, where the values of I_{P1} and I_{N1} depend on the characteristics of the CMOS structure. For example, based on the parameters given in the MOSIS 2um CMOS technology, when the aspect ratios of P_1 and N_1 are 10μm/2μm and 4μm/2μm, respectively, *Pspice* simulation results show that, for $I_{IN}=0$, the currents $I_{P1}=I_{N1}=0.1483$mA, and the current I_{P1} increases as the positive current I_{IN} increases. Thus, the converted data will definitely include at least a 1 in the presence of such a fault and the test current $I_{IN}=0$ detects the fault. The number of conversion cycles needed to detect the fault depend on the transistor parameters and con-

sequently on the fabrication technology. Similarly, the test current also detects the *S/ON* fault on switch S_5.

In summary, two test current I_{IN}=0 and I_{IN}= I_{REF} can detect all *S/ON* and *S/OFF* switches in the converter of Figure 3.4. Thus, the converter achieves full testability. Not only is the test set finite and easily generated; the testing sequence is also simple and cheap. In fact, testing consists of merely converting zero and I_{REF} then checking the output. It can be seen that it is not always possible to locate the erroneous element from examining the output resulting from the conversion of the test vectors.

4.3 CONCURRENT ERROR DETECTION

In order to enhance the reliability of A/D converters for real-time applications, an alternative current-mode A/D converter which possesses the CED capability to detect transient faults and permanent faults, is proposed.

4.3.1 Proposed Concurrent Error Detectable A/D Converter Design and Operation

Figure 4.1 illustrates a CED scheme with the AL implementation. First, the input current I_{t1}=I_{IN} is converted during the first time step (or, normal operation phase) and the resulting digital data is stored in a digital shift register. Then, the complemented current I_{t2}=I_{REF} -I_{IN} is converted during the second time step (or, recomputing phase). The digital data resulting from both phases are compared to identify an error, if it exists. If the converter is fault-free, the converted data resulting from both phases must be bitwise complements of each other. For example, with the reference current suggested in [10], i.e., I_{REF}=100μA, the input current 27μA and its complement 73μA are converted to the 10-bit data D_1=(0100010100) and D_2=(1011101011), respectively, where both D_1 and D_2 are bitwise complements. Since the comparison is in a digital manner, a *totally self-checking (TSC)*

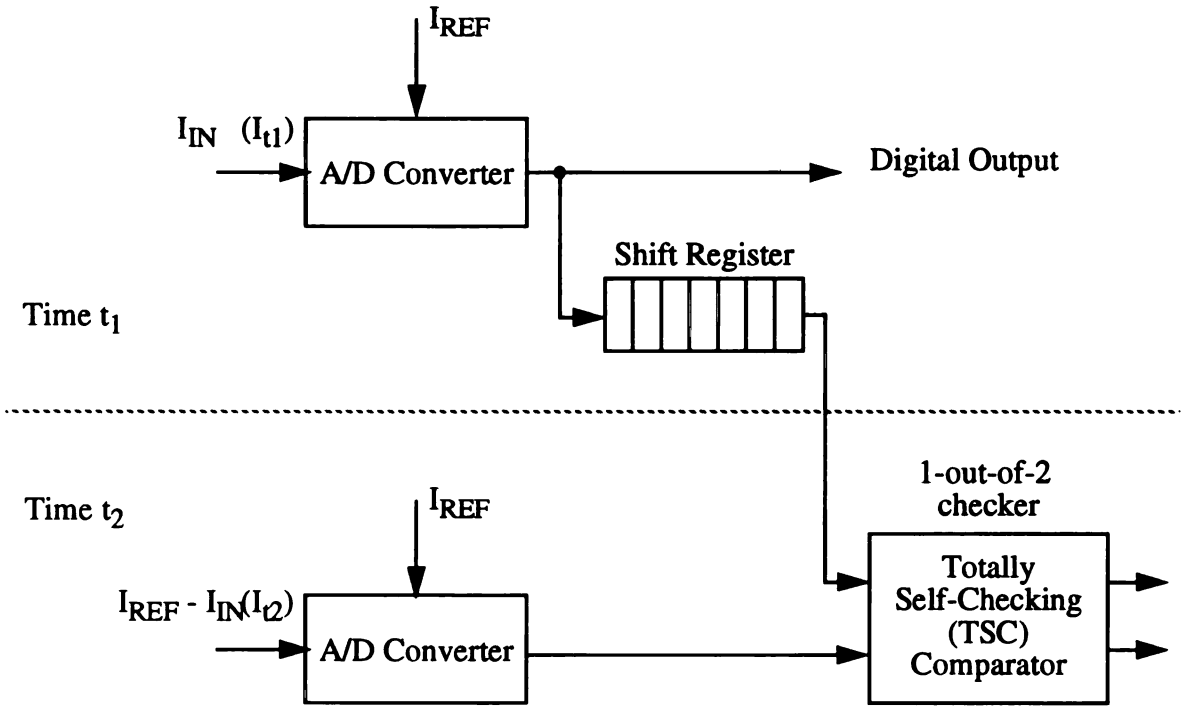


Figure 4.1 CED Structure With AL Implementation.

checker can be used to identify the error and also to ensure the correctness of the checker circuit. Therefore, a reliably converted data can be attained.

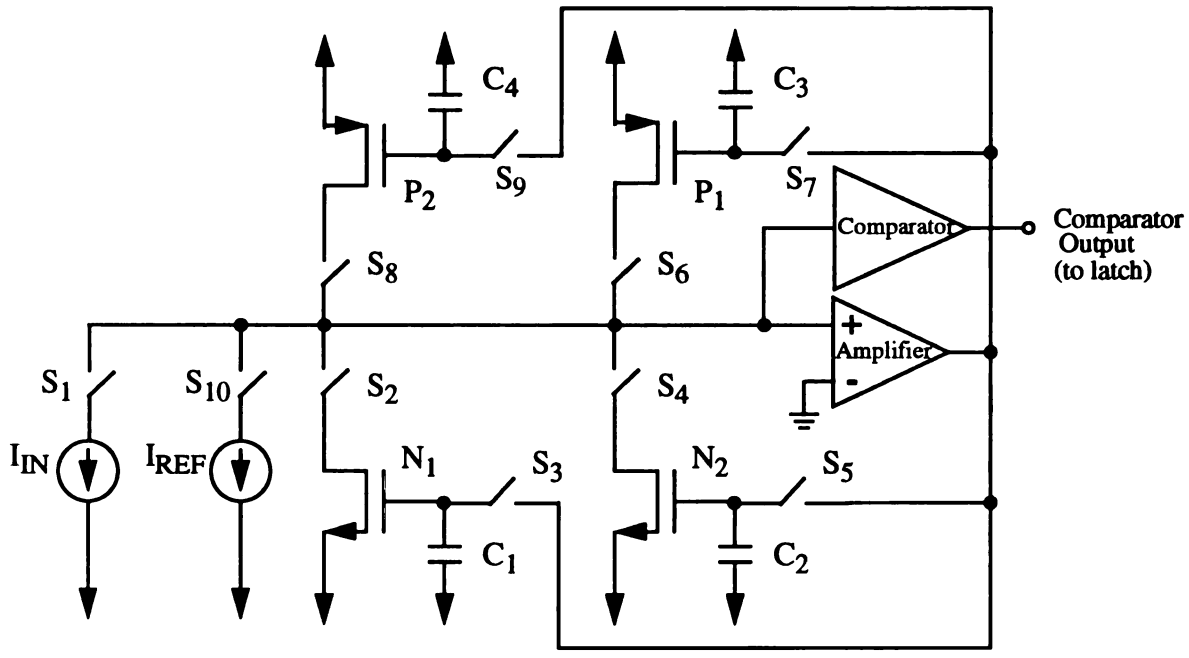
Figure 4.2(a) shows the proposed current-mode A/D converter with the CED capability. The input current I_{IN} is sampled only once and the current is stored in P_1. In order to store the current (I_{REF}-I_{IN}), an additional PMOS current copier is needed to hold the current at the beginning of the data conversion. The input current I_{IN} is copied and stored in P_1 by turning on Switches S_1, S_6, and S_7, while the current difference (I_{REF}-I_{IN}) is loaded to P_2 by turning off S_1 and S_7 and turning on S_8, S_9, and S_{10}. Once both currents are stored, the current held in P_1 and the current held in P_2 are converted. The results from both conversions are compared to identify an error, if it exists. The data conversion process is exactly the same as presented previously. Figure 4.2(b) illustrates the switching sequence.

In the next section fault diagnosis of the proposed converter is performed to determine the effectiveness of the CED scheme. The fault model underlying this analysis is presented. In this case transient characteristics of the faults are considered.

4.3.2 Fault Model and Fault Effects

Similar to the fault model and fault effects discussed previously, a single stuck-at fault model is also considered. Only one faulty switch occurs at a time and a faulty switch may be permanently or temporarily *S/ON* or *S/OFF*. By temporary faults, or transient faults, we mean that the duration of fault behavior is sufficiently short. Transient faults have been very common in today's digital VLSI design. Since all switches in the A/D converter are controlled by the digital clock signals, a signal may temporarily change its value from 0 to 1 or from 1 to 0 and cause the switching elements to temporarily malfunction. By permanent faults we mean the duration of the fault behavior is sufficiently long.

In general, the duration of a transient fault is sufficiently short. It is most likely shorter than the conversion time for the converter, i.e., 4N clock cycles. Here, a fault may occur



(a)

	Current S/H	NORMAL OPERATION PHASE			RECOMPUTATION PHASE		
		MSB	Previous bit = 1	Previous bit = 0	MSB	Previous bit = 1	Previous bit = 0
S_1							
S_2							
S_3							
S_4							
S_5							
S_6							
S_7							
S_8							
S_9							
S_{10}							

(b)

Figure 4.2 Proposed Current-Mode A/D Converter With CED Design.
(a) Schematic Diagram. (b) Switching Sequence.

during the first time step, or during the second time step, or overlap in both time steps (but the duration is shorter than 4N). If the fault occurs only during the first time step, i.e., the fault disappears during the second time step, then the converted data D_2 is reliable and can be used to check D_1 for identifying an error, if it exists. Thus, the fault is detectable. Similarly, the fault that occurs only during the second time step is also detectable. Now, if the fault occurs after the r-th bit of D_1 is being converted and disappears after the (r-1)-th of the D_2, for any integer r, then at least the first (r-1) bits of D_1 are reliable and can be used to identify the fault. Thus, the fault is detectable and the proposed design can detect all transient faults.

If the duration of fault behavior is longer than the time required to complete the first time step and the second time step, all time redundancy CED schemes will no longer possess the property of disjoint error sets, and the errors, thus, cannot be detected. This implies that not all permanent faults are detectable. It would be preferable for the circuits to be designed such that they will indicate malfunction during normal operation and will not produce an erroneous result without an error indication. In these circuits, any failures will cause a detectable erroneous output during normal operation, and each fault must not cause an erroneous output without also producing an error signal. The circuits that possess this property are referred to as *fault secure* circuits.

In the presence of single stuck-at faults at the switching elements in the proposed A/D converter design, four types of errors may be identified. Tables 4.1-4.4 illustrate these error types and their fault effects.

The errors that can be definitely detected by the CED scheme are referred to as *Type 1 errors*, i.e., a Type 1 error causes $D_1 \neq \overline{D}_2$ for all possible input currents. The errors that cannot be detected are referred to as *Type 2 errors*, i.e., a Type 2 error causes $D_1 = \overline{D}_2$ for all possible input currents. In some cases $D_1 \neq \overline{D}_2$ for all possible input currents except a few. For these few where $D_1 = \overline{D}_2$, if the resulting data D_1 is reliable even in the presence of

fault(s), then the circuit is fault secure and such an error is referred to as *Type 3 error*. On the other hand, if the resulting data D_1 is not reliable in the presence of fault(s), then the fault cannot be detected for the application of such input and this error is referred to as *Type 4 error*.

4.3.2.1 Type 1 Errors

Type 1 errors occur due to S/ON faults at S_2, S_3, S_4 and S_5 and S/OFF faults at S_2 and S_4. Consider a *S/OFF* faulty switch S_2, the first time step results in D_1=(00...0) regardless of the value of the input current being converted. Similarly, during the second time step, the conversion of the complemented current I_{REF}-I_{IN} results in an output data D_2=(00...0), i.e., $D_1 \neq \overline{D}_2$ for all possible input currents. Thus, this is a Type 1 error. Similarly, the *S/OFF* fault of switch S_4 and the *S/ON* faults of switches S_2 and S_4 have the same fault effect.

Consider the *S/ON* faulty switch S_3. During the first time step, the fault leads to constructing a P_1/N_1 CMOS structure, as discussed in Section 2.2. Experimental results have shown that D_1=(00...0) and D_2=(10...0) for a sufficiently low input I_{IN}; D_1=(10...0) and D_2=(00...0) for a sufficiently high input I_{IN}; and D_1=(00...010...0) and D_2=(00...010...0) for the others. Obviously, the error can be detected for either case. Thus, it is a Type 1 errors. Similarly, the *S/ON* fault of S_5 has the same fault effect.

Table 4.1: Type 1 Errors - $D_1 \neq \overline{D}_2 \; \forall \; I_{IN} \Rightarrow$Definitely detectable

Fault	Analysis	Fault Effects
S_2 (S_4) S/OFF	Zero current held in N_1 (N_2). Current not doubled.	$D_1=D_2=(00...00)$
S_2 (S_4) S/ON	N_1 (N_2) cancels current from P_1 or P_2. N_2 (N_1) holds zero current. Current not doubled.	$D_1=D_2=(00...00)$
S_3 (S_5) S/ON	Output depends on the CMOS structure P_1/ N_1 (P_1/N_2).	One bit of D_1 equals the respective of D_2.

4.3.2.2 Type 2 Errors

Type 2 errors include S/ON fault at S_{10} and S/OFF faults at S_1, S_6 and S_{10}. These errors are caused by either not reading the input current (*S/OFF* fault at S_1), or not reading the reference current (*S/OFF* fault at S_{10}), or the equivalent fault effects. For example, a *S/OFF* fault at S_1 implies that a zero current is copied into P_1 and thus I_{REF} is copied into P_2. Thus, $D_1=(00...0)$ and $D_2=(11...1)$, i.e., $D_1=\overline{D}_2$ for all possible input currents. Such a Type 2 error is definitely undetectable. Similarly, the *S/OFF* faults of switch S_6 has the same fault effect.

Consider a *S/OFF* fault at S_{10}. The fault is equivalent to the A/D converter using a zero reference current. First, the input current I_{IN} is copied into P_1. Then, P_2 was expected to copy a current equal to (I_{REF}-I_{IN}). However, the zero reference current results in a negative current, -I_{IN}, being forced into P_2. The operational amplifier saturates, P_2 cuts off, and its corresponding storage capacitor charges to the amplifier's negative saturation voltage. During the first conversion step this capacitor gradually discharges to ground. At the start of the second conversion step, the current in P_2 is supposed to be copied into N1; however the new feedback connection presented to the operational amplifier results in a different drain to source voltage for P_2. This voltage depends on the charge of the storage capacitor of P_2 and of the parameters of both P_2 and N_1 i.e. of the equivalent impedance of the P_2-

N_1 connection. The current to be converted in the second time step depends on the circuit parameters. Hence it may be effectively regarded as random. Since, during the first time step, P_1 holds the current I_{IN} and the reference current I_{REF}=0, the resultant data is D_1=(11...1). Since the second conversion step may result in D_2=(00...0). D_1 may equal $\overline{D}_2$ for all possible input currents and the error is of Type 2. A *S/ON* fault at S_{10} has the same fault effect. In fact, the first conversion step resolves the current $I_{IN}+I_{REF}$ resulting in D_1=(11...1). The current held in P_2 to be converted in the next step is equal to I_{REF}-($I_{IN}+I_{REF}$) i.e. $-I_{IN}$.

Table 4.2: Type 2 Errors - $D_1=\overline{D}_2 \; \forall \; I_{IN} \Rightarrow$ Definitely undetectable

Fault	Analysis	Fault Effects
S_1 S/OFF	Equivalent to I_{IN}=0. P_1 holds zero and P_2 holds I_{REF}.	$D_1=\overline{D}_2$=(00...00)
S_6 S/OFF	P_1 never copies current. P_2 holds I_{REF}.	$D_1=\overline{D}_2$=(00...00)
S_{10} S/OFF	Equivalent to I_{REF}=0. $-I_{IN}$ forced into P_2	$D_1=\overline{D}_2$=(11...11.)
S_{10} S/ON	I_{REF} always added to the current copied into P_1. $-I_{IN}$ forced into P_2	$D_1=\overline{D}_2$=(11...11.)

4.3.2.3 Type 3 Errors

This set includes S/ON faults at S_6, S_7, S_8 and S_9 and S/OFF faults at $S_8$and S_9. Consider a S/ON fault at S_6. According to switching sequence shown in Figure 4.2(b), S_6 is on for the entire conversion cycle during the first time step. Thus, the resultant data is still correct even in the presence of such a fault. On the other hand, at the end of the first time step, the current held in P_1 is I_x, where I_x is less than 1 LSB if the last bit of D_1 is 1; otherwise I_x is greater than 1 LSB. Due to the faulty switch S_6, the current, I_x, held in P_1 is always available during the second time step. This is equivalent to converting the sum of I_x and the current held in P_2 for each bit conversion. If $D_1 \neq \overline{D}_2$, then the checker will indicate an error.

On the other hand, if $D_1=\overline{D}_2$, the converted data D_1 is reliable. Thus, the circuit is fault secure and the error is of Type 3.

Similarly, a *S/OFF* fault that occurs at S_8 or S_9 and a *S/ON* fault at S_9 do not affect the conversion in the first time step, i.e., D_1 is reliable. However, the *S/OFF* faulty switches S_8 and S_9 results in D_2=(00...0), while the *S/ON* faulty switches S_9 may cause P_2 to source a random current. In fact, P2 stores the last current copied into P1. Thus, the circuit is fault secure in the presence of such fault(s) and the error is of Type 3. In the same manner, a *S/ON* faulty switch S_8 results in D_1=(11...1) for all possible input currents, but provides a reliable data D_2. If there exists, at least, one 1-bit in D_2, the comparison will identify an error. On the other hand, if D_2=(00...0), then D_1 provides a reliable result. Thus, the circuit is also fault secure in the presence of such a fault.

Consider the *S/ON* faulty switch S_7. The fault causes the current held in P_1 to be changed whenever the op-amp is in use. For example, after the input current I_{IN} is loaded into P_1, the current (I_{ref}-I_{IN}) is copied into P_2. The faulty switch S_7 will cause the gate-source voltage of P_1 to equal that of P_2. Thus, I_{ref} will be approximately divided between P_1 and P_2, reflecting any mismatch between the two transistors. During the normal operation phase, when the current held in P_1 is compared to the reference current I_{ref} to determine the converted bit value, the faulty switch S_7 causes the current held in P_1 to be I_{ref} and thus a "1" results. This implies that D_1=(11..11). Since the fault does not affect the conversion of the current held in P_2,the converted data D_2 corresponds to approximately $I_{ref}/2$. This would have been a Type 1 error if it were not for the case of I_{IN} equal to approximately $I_{ref}/2$.

Table 4.3: Type 3 Errors - D_1 correct or $D_1 \neq \overline{D}_2 \Rightarrow$ Fault secure.

Fault	Analysis	Fault Effects
S_6 S/ON	Normal operation phase not altered. Residual current in P_1 always sourced during recomputation phase.	D_1 correct. D_2 random.
S_7 S/ON	During comparison P_1 initially copies I_{ref} and then gets compared. Recomputation phase converts a current equal to approximately $I_{ref}/2$.	D_1=(11...11). D_2= code for approximately $I_{ref}/2$.
S_8 S/ON	Residual current in P_2 always sourced during normal operation phase. Recomputation phase not altered.	D_1 random. D_2 correct.
S_9 S/ON	Normal operation phase not altered. During comparison P_2 initially copies I_{ref} and then gets compared.	D_1 correct. D_2=(11...11).
S_8 S/OFF	Normal operation phase not altered. P_2 never copies current.	D_1 correct. D_2=(00...00).
S_9 S/OFF	Normal operation phase not altered. Residual current in P_2 always compared with I_{ref}.	D_1 correct. D_2 random.

4.3.2.4 Type 4 Errors

Type 4 errors include S/ON fault at S_1 and /OFF faults at S_3, S_5 and S_7. Consider the S/ON faulty switch S_1. It is assumed that the input current will be varying for real-time applications. The fault implies that the data is converted in the environment where the noise is equivalent to the varied input currents. Thus, D_1 and D_2 can be any random results. Statistically speaking, the probability of having two random data D_1 and D_2 as complements to each other is very low. Thus, this is a Type 4 error.

Due to the *S/OFF* faulty switch S_7, the current copier with P_1 cannot copy any current. Thus, the current, I_x, held in P_1 is the one remained in the previous operation. This results in D_1=(00...0) if $I_x < I_{REF}$, or D_1=(11...1) otherwise. Since P_1 can still source the

current I_x, the current held in P_2 is (I_{REF}-I_x) and the resultant data D_2 is reliable. Therefore, $D_1=\overline{D}_2$ only if *either* I_x or (I_{REF}-I_x) is less than 1 LSB, $D_1\neq\overline{D}_2$ otherwise. This is a Type 4 error. Similarly, due to *S/OFF* faulty switch S_3 the current copier with N_1 cannot copy any current. Assume that the current held in N_1 is I_x. then the conditions for D_1 to be complementary to D_2 can be determined. First, an input current I_{IN} is assumed. Next, two inequalities involving I_{IN}, I_x and I_{REF} are derived based on the assumption that I_{IN} and (I_{IN}-I_{REF}) result in complementary MSBs. If the inequality does not contradict any initial assumptions, it is kept. The derivation continues for the next bit, and a new set of inequalities are determined and checked for contradictions against the assumptions and the previous inequalities. The result, is summarized as follows:

MSB=0 so that $I_{IN} \leq I_x < I_{REF}-I_{IN}$

Bit 1 = 1 so that $(I_{REF}-I_{IN})/2 \leq I_x < (I_{REF}+I_{IN})/2$

...

Bit k = 1 so that $(kI_{REF}-I_{IN})/(k+1) \leq I_x < (I_{REF}+I_{IN})/(k+1)$

where k=0,1,...,N-1, and N is the converter's resolution. Hence $D_1=\overline{D}_2$ only if I_x is very close to $I_{REF}/2$, and $D_1\neq\overline{D}_2$, otherwise. For a reliable design, the chance that the fault occurs when the current held in N_1 is $I_{REF}/2$ is rare. Due to the analog nature, this error is of Type 4. Similarly, the fault of *S/OFF* switch S_5 has the same fault effect.

Table 4.4: Type 4 Errors - Random data $\Rightarrow$ Most likely detectable

Fault	Analysis	Fault Effects
S_1 S/ON	Varying I_{IN} always sourced to the circuit.	D_1 and D_2 random
S_3 (S_5) S/OFF	N_1 (N_2) do not copy any current but its residual current is sourced.	D_1 and D_2 random
S_7 S/OFF	Residual current in P_1 always compared with I_{REF}. Recomputation phase converts the complement of this residual current.	D_1 and D_2 random

4.3.3 Fault Coverage

Table 4.5 summarizes the status of error detection for all possible stuck-at faults that may occur at the switching elements in the proposed A/D converter design.

There exist eight Type 1 errors, four Type 2 errors, five Type 3 errors, and three Type 4 errors. If the fault coverage is defined as the total number of Types 1, 3, and 4 errors over all possible errors, the fault coverage of permanent faults is 80%.

A novel current-mode A/D converter design with CED capability, where a time redundant CED scheme is implemented. The original A/D converter [10] is modified by adding an extra PMOS current copier to provide the CED capability, thus making the validation of the converted data more reliable. Results have shown that the proposed design can detect all transient faults that occur at the switching elements and most of the permanent faults. Some permanent faults cannot be detected due to the unavailability of test patterns for real-time applications. However, as discussed previously, two test patterns can be employed to detect the permanent faults. Therefore, it is suggested to randomly apply the two test patterns to the proposed A/D converter detecting the permanent faults.

The drawback of the proposed design with CED capability is approximately 100% overhead in time which is inherent in all time redundancy schemes. Judging from the VLSI performance measure of AT^2 (where A is the chip area and T is the operation cycle time),

this is rather a high price to pay. However, the performance penalty associated with time redundancy can be absorbed by the inherent idleness of the processing element [25]. The proposed design is perfectly applied to those systems or subsystems in which the time to process the converted data is as much as twice of the conversion time. The other salient feature is that the proposed design allows users to easily switch between an A/D converter with and without CED capability by simply changing the switching sequence without causing any performance degradation.

Table 4.5: Concurrent Error Detection

Switches	S/ON	S/OFF
S_1	Type 4	Type 2
S_2	1	1
S_3	1	4
S_4	1	1
S_5	1	4
S_6	3	2
S_7	3	4
S_8	3	3
S_9	3	3
S_{10}	2	2

CHAPTER FIVE

CONCLUSIONS

This chapter summarizes the major contributions of this thesis and outlines the directions for future developments.

5.1 SUMMARY OF MAJOR CONTRIBUTIONS

This thesis achieves test pattern generation for the current-mode A/D converter proposed in [10]. Results show that during the manufacturing test, the converter circuit can be tested for all single stuck-at faulty switching elements by applying two test currents at the input. In addition a novel current-mode A/D converter design with CED capability, where a time redundant CED scheme is implemented. The original A/D converter [10] is modified by adding an extra PMOS current copier to provide the CED capability, thus insuring the validation or rejection of the converted data in the presence of any stuck-at-fault model at the switching elements during real-time operation. Results have shown that the proposed design can detect all transient faults and most of the permanent faults. The other salient feature of the proposed design is its versatility. The user can easily switch between an A/D converter with and without CED capability without causing any performance degradation by simply changing the switching sequence.

5.2 DIRECTIONS FOR FUTURE DEVOLOPMENTS

In the process of fault effect analysis, a new current copier cell has been established. The CMOS current copier has the advantage of handling bipolar currents making it attractive for circuit application where the direction of the current(s) is not known a priori. A new successive-approximation current-mode converter is being developed where the CMOS copier represents the core of the reference generation circuit [32].

This work has focused on fault diagnosis pertaining to a specific fault model at specific elements of the converter circuit. By applying the concept of fault equivalence, any fault whose effect is equivalent to a stuck-at fault at the switching element(s) will also be flagged by the proposed converter. The possibility of reducing faults in other parts of the circuit to a stuck-at fault at the switching elements can be investigated. To further improve the data validation capability of the proposed converter, the effects of those faults that cannot be modeled as stuck-at can also be analyzed. Different fault models can be applied and diagnosed.

The CED strategy can be applied to other current-mode A/D and D/A conversion circuits as well as voltage mode converters in the quest for data validation; thus improving the reliability of data processing systems.

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