This is to certify that the

dissertation entitled

An Investigation of Hot Electron Induced Degradation for Silicon Bipolar Transistors

presented by

Chi-Jung Huang

has been accepted towards fulfillment of the requirements for

PhD degree in Electrical Engineering

Timothy Gutgiln
Major professor

Date 2/17/1992

AN INVESTIGATION OF HOT ELECTRON INDUCED DEGRADATION FOR SILICON BIPOLAR TRANSISTORS

By

Chi-Jung Huang

A DISSERTATION

Submitted to
Michigan State University
in partial fulfillment of the requirement
for the degree of

DOCTOR OF PHILOSOPHY

Department of Electrical Engineering

1992

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ABSTRACT

AN INVESTIGATION OF HOT ELECTRON INDUCED DEGRADATION FOR SILICON BIPOLAR TRANSISTORS

By

Chi-Jung Huang

Bipolar transistors were electrically stressed at -75, 23, 175, and 240 C for up to 1000 hours with a constant reverse bias of 4 volts applied to the emitter-base junction. Additionally, electrical stress experiments were performed for reverse biases of 3.5, 4.0, 4.5, and 5.0 volts for 200 hours at 23 C. The rate of degradation was observed to be dependent on the stress voltage and the ambient temperature. For larger reverse bias voltages, the rate of degradation was larger, and for higher temperatures, the rate of degradation was generally smaller. However the 23 C degradation was greater than the -75 C degradation for the first few hours of stress.

An investigation of the degradation was done by developing an electron energy simulation program. The electron energy simulation program was used to solve for the electron energy under experimental stress conditions. The simulator had a band-to-band tunneling model implemented to solve for the reverse-bias stress current. For the experimental stress conditions, the number of hot electrons above a threshold damage energy was seen to be primarily controlled by the tunneling process with a larger number of hot electrons at higher temperatures. The simulations explain the increasing degradation rate when the ambient temperature changes from -75 to 23 C.

The decreasing degradation rate from 23 to 240 C was studied by using post-degradation annealing experiments. A simultaneous annealing effect was found to repassivate some of the hot electron produced states at higher ambient temperatures. A

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degradation/annealing model is proposed to include both degradation and annealing effects. The simultaneous annealing effect explains the decreasing degradation rate for ambient temperatures from 23 to 240 C. The degradation/annealing model predicts the saturation of the degradation phenomena at higher stress temperatures.

A degradation model which relates the surface recombination velocity to the number of interface states was implemented into a device simulation program. The device simulation program which includes the energy simulation technique can be applied to predict the rate and magnitude of the hot electron induced damage when the device geometry, doping level, or stressing/operating conditions are varied.

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ACKNOWLEDGMENTS

I would like to thank my academic advisor, Dr. Timothy A. Grotjohn. This dissertation would not have been produced without the many valuable suggestions and inspiring discussions from Dr. Grotjohn.

I would also like to acknowledge my appreciation to C. J. Sun and Professor D. K. Reinhard for their assistance during this investigation.

This work was performed as part of a research contract from IBM Corporation, East Fishkill, NY. The suggestions and comments of C.-C. W. Yu (IBM Corporation, Kingston, NY) are acknowledged and appreciated.

Finally, I am grateful to my wife, Su-Yun, for her support and encouragement.

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Chapter 1

Introduction

1.1 Motivation

With each advancement in the technology of semiconductor device design and fabrication, the associated reliability problem has always been an important issue. In particular, an understanding of the degradation mechanisms and the establish of a degradation model are essential for the prediction and improvement of device lifetime.

For silicon bipolar transistors, current gain (β) degradation as a result of avalanching the emitter-base junction was observed before 1970 [1-3]. The cause of the avalanche induced degradation was first thought to be related to ionic contamination existing within the device oxide [2]. Collins [3] and McDonald [1] were able to show that the avalanche induced degradation for low current gain was in fact due to hot carriers creating surface states within a transistor's depletion region. Several later improvements were made to avoid operating BJT's at avalanching biases, an example is the termination of input lines by clamping diodes in integrated logic systems.

Recently, the trends in bipolar transistor scaling have resulted in highly energetic carriers at the reverse biased emitter-base junction for below-avalanche voltages. A schematic diagram of the BJT geometry and the local high field region where damage is most likely to occur is shown in Figure 1.1 [4]. Hot carriers were reported to cause degradation in advanced technology transistors operated at biases which were less than avalanche bias conditions in several studies [5-17]. The reported mechanisms include hot carrier created interface states formed by breaking bonds at the interface and/or injected carriers trapped in the oxide producing oxide fixed charges as shown in Figure 1.2.

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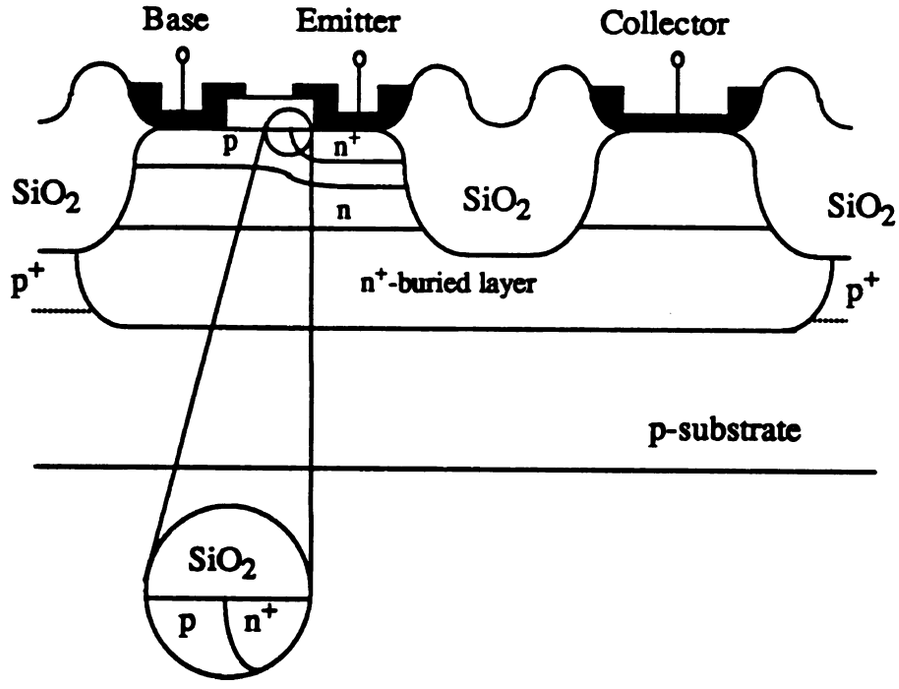
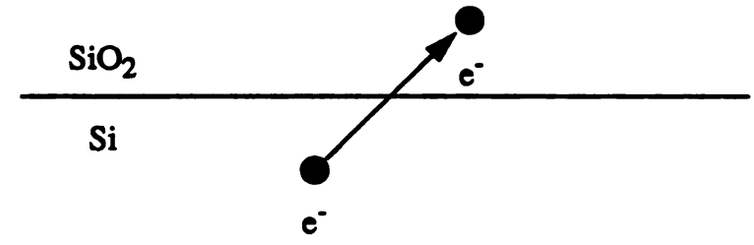


Figure 1.1: A schematic diagram of the bipolar transistor geometry. Emphasized region is the local high field region where hot electron induced damage is most likely to occur.



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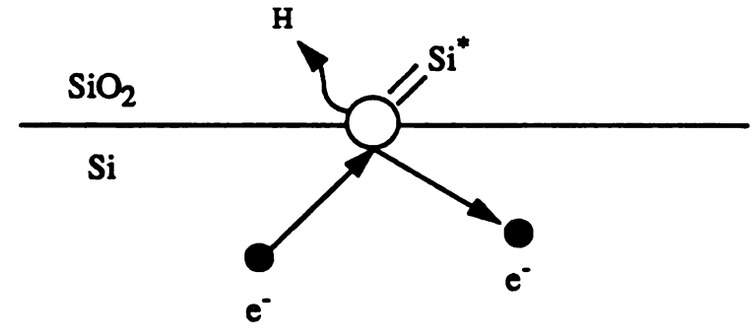

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Figure 1.2: Hot electron induced degradation mechanisms: (a) Injected electron trapped in the oxide. (b) Hot electron breaks the Si-H bond.

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Based on their experimental results, several researchers developed degradation models that predict the degradation rate as a function of the stress conditions. These works were either based on simplified approximations for the hot electron energies or were empirical and modeled the macroscopic quantities. The exact amount of hot carriers responsible for the degradation was not solved by these works and a device level model suitable for the prediction of device degradation when a device design changes is yet to be established.

The purpose of this study is to analyze the hot electron induced degradation mechanism produced by degradation conditions and to provide a relationship, at a device level, between the degradation and the hot electrons produced. This will be done by first using hot electron induced degradation experiments from which the actual degradation process is recorded. Second, by using an electron energy simulation technique which solves for the hot electron current along the surface high field region for bipolar transistor structures. By correlating these two results, an understanding of the mechanism and process of hot electron induced degradation can be improved. Additionally, a device degradation model that predicts device degradation based on the device operating conditions is established so that the reliability problem can be evaluated at the time of device design by simulation techniques.

1.2. Review of Previous Work

1.2.1 Hot Electron Induced Degradation Experiments and h_{FE} or Base Current Degradation Modeling

Experimental degradation and reliability studies for the bipolar transistor can be traced back several years. The degradation process and mechanism vary depending on the device design and the technology of fabrication. This study will focus only on the hot electron induced degradation in advanced bipolar transistor structures.

Hot electron induced degradation in advanced self-aligned sidewall spacer NPN bipolar transistors was observed by Petersen et. al. [6]. The transistors were operated

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with their emitter-base junctions reverse biased and collectors opened. The carriers were injected by illumination near the edge of the emitter-base depletion region with a 5 mW He-Ne laser source. After the application of the reverse-bias produced hot electrons, the forward base current was measured as a Gummel plot (I_B, I_C vs. V_{BE} for V_{BC} = 0) to determine the amount of current change ΔI_B. The measured characteristics taken before and after the constant current stress showed that the increase of the low level base current after stress was accompanied by a shift in the ideality factor from near 1 to almost 2. This indicated the probable cause for the higher base leakage current to be an increase of interface state density in the sidewall oxide between the emitter and base. The plot of ΔI_B versus stress charge Q(=i·t) through the emitter base junction for various applied stress voltages showed that the ΔI_B increased nonlinearly with Q for stress voltages above a critical value.

The work done by Joshi [8] showed hot carrier induced degradation in a poly-emitter bipolar transistor fabricated by a BiCMOS process. Transistor gain degradation was studied by reverse biasing the emitter base junction under DC, pulsed, and AC conditions. For the ceramic packaged devices, extended temperature (-55 C to 175 C) tests were performed. The β degradation was seen at both low emitter-base forward bias current levels (I_C =10 μA) and high current levels (I_C = 1 mA). From the Gummel plot, the emitter-base ideality factor first increased from 1 to 2 for low current levels and subsequently for the entire range of I_B up to the Gummel knee current. Constant current stressing of the reverse biased E-B junctions revealed that β degradation depends on the stress current I_R and the stress duration t. An excellent correlation was observed between the stress charge defined as I_R·t and β degradation. Joshi thus proposed the model

$$\frac{\Delta\beta}{\beta_o} = K_1 \log Q + K_2 \qquad ; Q > Q_C \qquad (1.1)$$

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where $\Delta\beta$ is the change in the current gain after stress, β_o is the initial current gain, K_1 and K_2 are fitting constants, and Q_C is the critical charge beyond which the degradation cannot be recovered by annealing at elevated temperatures.

Burnett et. al. [9] investigated Joshi's model over a range of reverse bias currents and device sizes for self-aligned polysilicon emitter transistors. Unlike the result of Joshi's model, $\Delta\beta/\beta_o$ for different values of I_R did not fall on the same curve and the individual curves were not straight lines. Burnett, instead, plotted the logarithm of ΔI_B versus logarithm of Q and found that the plots are straight lines with approximately the same slope for various I_R. Burnett proposed the empirical model

$$\Delta I_B = C \cdot I_R^{m+n} \cdot t^n \tag{1.2}$$

where m, n, and C are fitting parameters.

Li et. al. [7] and Hackbarth et. al [10] investigated the current components for both the inherent and stressed induced leakage currents for heavily doped emitter-base junctions of polysilicon self-aligned bipolar transistors. By using devices with various perimeter dimensions and by investigating the temperature dependence of bipolar transistor I-V characteristics for both forward and reverse bias voltages over a temperature range of 90 to 390 K, a band-to-band tunneling current and a trap-assisted tunneling component were found to be the inherent reverse leakage component in [7] or [10], respectively. Reverse-bias stress was found to produce interface states which induced a Poole-Frenkel electric field enhanced generation/recombination leakage current [10] or to cause an increase in trap densities and subsequently a trap-assisted tunneling nonideal current [10]. The induced ΔI_B was observed to eventually saturate at some maximum level [11]. A first order relation between ΔI_B and stress charge Q was found as

$$\Delta I_B = \Delta I_{B,sat}(1 - \exp(-Q/\alpha)) \tag{1.3}$$

where $\Delta I_{B,sat}$ indicates the maximum current degradation the device will be subjected to, and α indicates at what accumulated charge the device degradation will become

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significant. An empirical rate model was also proposed by Tang et. al. [11] which considered two time constants: the surface state generation time constant τ_g and the healing time constant τ_h,

$$\frac{d\Delta N_{ss}}{dt} = \frac{(N - \Delta N_{ss})}{\tau_g} - \frac{\Delta N_{ss}}{\tau_h} \tag{1.4}$$

where N is the total number of interface states that can be created, and ΔN_{ss} is the newly created surface states. The stress induced leakage current is proportional to ΔN_{ss} and rises according to (1.3).

A temperature dependence study on the emitter-base reverse bias stress degradation was done by Momose et. al. [13] for npn bipolar transistors fabricated by a ion-implanted emitter BiCMOS process. They found that the reverse-bias stress-induced degradation is largest around 50 C. By applying a MOSFET structure simulation, they modeled both trapped electrons and interface state creation for the degraded characteristics. The interface state creation in the oxide near the emitter-base junction was modeled using an increase in the recombination velocity at the surface and was found to be in agreement with experimental results. They concluded that interface state creation is the dominant degradation mechanism.

In 1990, Burnett et. al. [15] reported the reverse bias induced degradation at 110 and 300 K for BJT's fabricated by BiCMOS technology. The rate of degradation was observed to be four times larger at 110 K than at 300K for the same reverse voltage and ten times larger for the same stress current. The increased degradation at lower temperature is consistent with the increase severity of hot carrier damage in MOSFET's at lower temperatures [18,19]. The BJT degradation was modeled as

$$\Delta I_B = D J_c^a I_R^b t^c \tag{1.6}$$

where J_C is the collector current density. D, a, b, and c are fitting parameters.

Although the empirical models developed can be used for lifetime prediction, they provide little insight in the degradation for different device designs. An

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experimental procedure must be performed for individual devices in order to determine the fitting parameters.

1.2.2 Hot Electron Induced Degradation Mechanism Modeling

One of the earlier works of modeling the avalanche induced degradation mechanism was done by McDonald [1]. He was able to explain the degradation current by an increase in the surface recombination velocity S_o as a result of avalanche induced surface state formation within the surface depletion region. By summing the uniform, nonavalanche associated surface recombination velocity S_o and the localized avalanche-induced surface recombination velocities S_{oA}, a total surface recombination velocity was obtained. To obtain the degradation current, a summation of the surface recombination current in each of n intervals along the surface depletion region was calculated where in each interval the surface recombination rate U_{sj} was calculated. The total degradation current was expressed as

$$I_{rec,s}(V_G) = q\sum_{j=1}^{n} U_{sj}(V_G)A_{sj} \qquad (1.7)$$

where V_G is the applied gate voltage and A_{sj} is the area associated with interval j. An agreement between the experiment and the model was found by assuming an avalanche induced surface recombination velocity of 100 cm/s localized within 0.1 μm on either side of the emitter-base metallurgical junction. Experimental evidence was also presented for localized charge trapping within the oxide over the emitter-base junction as a result of avalanching condition.

Bulucea [20] developed a theory to calculate the injection probability defined as the fraction of the avalanching electrons which acquire sufficient energy to surmount the Si-SiO_2 energy barrier. The number of these high energy electrons actually entering the oxide is determined by a scattering function which allows some high energy electrons to

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enter the oxide while the rest are reflected. By assuming a Maxwellian distribution of electron energy in the avalanche current, the injection probability is derived to be

$$P_I = a\exp(-E_B / kT_e) \qquad \text{for } E_B / kT_e \geq 4 \tag{1.8}$$

where a = 1.874, b = 0.926, E_B is the energy barrier, and T_e is the electron temperature.

Bergeron et. al. [5] proposed a model for the failure of lateral bipolar transistors caused by oxide trapped charge forming a short-circuiting inversion layer between the collector and emitter. The trapped charge in the model was due to the electrons being injected and then trapped in the oxide. Once enough electrons were trapped, an inversion layer formed leading to the transistor failure. By assuming a Schottky emission process, the probability of electrons entering the oxide is given by

$$P = A^*(kT_e)^2 \exp\left(-\frac{\phi_B}{kT_e}\right) \tag{1.9}$$

where A^* is the Richardson constant, and ϕ_B is the energy barrier. The electron density injected into the oxide at any time t is given by

$$N = \frac{1}{q}\int_0^t P j_e d\tau \tag{1.10}$$

where j_e is the junction leakage current. By examining the inversion layer between the emitter and collector, the time of failure is defined to be the time to reach the onset of inversion produced by the trapping of hot electrons in the dielectric region. The electron temperature in this model was calculated based on the given electric field as

$$T_e \cong T\frac{\mu E}{c}\sqrt{\frac{3\pi}{32}} \tag{1.11}$$

where μ is the mobility, c is the velocity of sound, and E is the electric field [21].

So far in the literature, the device level modeling of the hot electron degradation for bipolar transistor has not been discussed in detail due to (1) the complexity of extracting the electron energy when operating at hot electron induced conditions and (2) the much more difficult task of simulating an advance technology transistor. On the other

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hand, the modeling of MOSFET degradation has been very active, the following lists only a few of the studies that represent this approach for MOSFET degradation.

Roblin et. al. [22] modeled the hot electron trapping rate by considering the electron density in the channel, the frequency of ballistic launching of electrons, and the trapping probability. The probability P_{12} of a hot electron overcome the barrier height at the interface is

$$P_{12} \equiv \frac{1}{4}\frac{E\lambda}{\phi_B}e^{-\phi_B/E\lambda} \tag{1.12}$$

where λ is the mean free path (assumed constant) of hot electrons between collisions, and E and ϕ_B are the electric field and the energy barrier at the interface. Experimental studies [14] have reported λ to be a function of electron energy and is between 72 to 135 $\mathring{A}$. The probability P_3 of an electron scattered at a distance y from the interface traveling to the interface without further collision is given by

$$P_3 = e^{-y/\lambda}. \tag{1.13}$$

And the probability P_4 of an electron injected in the SiO_2 being captured by empty traps is given by

$$P_4 = \left(N_{max} - N_{trap}(t)\right)\sigma_{trap} \tag{1.14}$$

where N_{max} is the initial density of empty traps per unit area, $N_{trap}(t)$ is the density of traps filled per unit area, and σ_{trap} is the trapping cross section that depends on the fabrication technology. The product $P_{12}P_3P_4$ represents the probability for a ballistic electron located in the channel at a distance y from the oxide interface becoming trapped in the oxide. Finally, the rate for hot-electron trapping in the oxide was expressed as

$$\frac{dN_{trap}}{dt} = P_4(t)\int_0^{\infty} R_b(E)\cdot P_{12}(E)\cdot P_3(y)n(y)dy \tag{1.15}$$

where R_b is the launching frequency [23] and n is the carrier density. (1.15) as well as the two dimensional simulation program PISCES [24] was then used for the MOSFET structure by iteratively solving (1.15) and simulating a PISCES solution.

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Many works closely parallel Roblin's work, they are [25] which did AC hot electron stress, and [26] which incorporated the degradation of the surface mobility by using surface scattering due to interfacial charges.

These works were based on the classical drift-diffusion model which determined the carrier energy by using semiempirical relationships between the carrier temperature and the electric field. For nonequilibrium hot carrier energy calculations, the accuracy of these semiempirical relationships becomes questionable.

Horiuchi et. al. [27] included the carrier energy transport physics in a two dimensional simulation for the MOSFET structure. Their purpose was to establish a model that related the device lifetime with hot electron substrate current produced.

1.2.3 Hydrodynamic Transport Model

Numerical simulations have been widely used to provide insight into the physics of semiconductor devices. Two numerical models for the solution of semiconductor devices include (1) the Drift-Diffusion (DD) model, which solves for the Poisson, electron continuity, and hole continuity equations, and (2) the Hydrodynamic Transport Model (HTM), which solves for the Poisson, electron continuity, hole continuity, and electron and hole energy conservation equations. The classical DD simulation assumes that the carrier energies are in equilibrium with the lattice temperature, whereas the HTM simulation also solves for the carrier energies.

The method of including the carrier energy in the device simulation is to solve the energy conservation equation in addition to the continuity equation and Poisson equation [28,29]. The HTM models the carrier mobility as a function of the average carrier energy instead of the local electric field. Thus, the carrier energy can be different from the lattice temperature. Particularly in submicron GaAs devices where carriers exhibit strong nonstationary behavior, many researchers found the HTM model more accurate since it includes the momentum and energy relaxation effects [30,31]. Only a few papers have

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applied the HTM simulation method to silicon bipolar transistors. In 1983, Cook [28] first applied the HTM to simulate simplified one-dimensional bipolar transistors for the active mode of operation. The same device structure was simulated using the classical DD and the HTM simulation methods to compare the effects of including the hot-carrier transport. For an npn bipolar transistor with a base width of 150 nm and a collector to emitter voltage of 2.5 V, carrier heating was seen to occur in the collector-base depletion region where the potential drop accelerates the electrons. An electron temperature exceeding 2000 K was observed for a collector current density of 0.086 $mA/\mu m^2$. It was found that the classical DD assumption, which assumes that the carriers are in thermal equilibrium with the lattice, is invalid for the BJT device electron energy simulated, although this does not greatly affect the terminal I-V characteristics. The work by Ou et. al. [29] paralleled that of Cook's work, but differed in that the carrier transport coefficients were introduced in a more general form and that the effects of various model parameters on the hot carrier phenomena were examined. With proper choice of parameters, the carrier temperature results were similar to Cook's work. Forghieri et. al. [32] simulated an npn bipolar transistor in a two dimensional structure. For a BJT of base-width 100 nm, V_{BE} of 0.67 V and V_{CE} of 1.67 V, the peak electron temperature was about 900 K. The temperature maximum occurred near the collector-base junction under the emitter contact where the current density is nearly parallel to the electric field.

So far in the literature, there has been no modeling study devoted to the emitter-base reverse bias condition of bipolar transistors. In order to explore the energies of reverse bias induced hot electrons and to relate the hot electrons with BJT performance degradation, this study developed an electron energy simulation technique based on the HTM to extract the number of hot electrons in reverse biased conditions. The HTM model and the electron energy simulation technique are described in Chapter 3.

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1.3 Statement of Purpose

The purpose of this work is to improve the understanding of the hot electron degradation phenomena in silicon bipolar transistors. In particular, this work quantifies the hot electron induced degradation in silicon bipolar transistors using hot electron induced degradation experiments and electron energy simulations. Another objective for this research is to develop a model that is suitable for the prediction of device lifetime based on device designs and device operating conditions.

1.4 Thesis Preview

Chapter 2 describes the bipolar transistors used in this study. The stressing and measurement procedures are explained. The results of several BJT degradation experiments are described in this Chapter.

The numerical models for BJT's are described in Chapter 3. A classical DD simulation program is used both to extract the reverse bias stress conditions and the forward bias degraded characteristics. An electron energy simulation technique based on the HTM is developed to extract the hot electron current during BJT reverse bias stress conditions. The implementation of the band-to-band tunneling mechanism for the reverse stress condition is also shown in this chapter. Finally, the use of a single particle Monte Carlo simulation program to extract energy related parameters for the HTM model is presented.

Chapter 4 analyzes the unstressed BJT characteristics in both the emitter-base forward- and reverse-bias current regions. Measurement results are compared to simulation results for unstressed BJT characteristics.

Chapter 5 develops the hot electron degradation model by using the electron energy simulation technique and a surface state creation model. The subsequent prediction of degraded transistor characteristics and their comparison to experimental degradation results are also shown in this chapter.

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Chapter 6 applies the electron energy simulations to extract the amount of hot electrons at four different temperatures. At higher temperatures, a simultaneous annealing effect is found to be important in describing the degraded characteristics. An empirical degradation/annealing lifetime model is formulated to describe the degradation and annealing behavior for BJT's stressed in ambient temperatures other than room temperature.

Finally, conclusions and contributions are summarized in Chapter 7.

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Chapter 2

Experimental Bipolar Transistor Degradation Studies

2.1 Device Description

Over 200 wire bonded chips were provided to Michigan State University by IBM. Each chip contained three test devices (named TIN3, TOUT, and TD4) which were fabricated by conventional oxide isolation methods and had a base width of 0.35 μm [36]. These devices did not include emitter or base polysilicon structures. The chips were traceable as to location on the wafer, wafer number, and job number. TOUT and TD4 had Schottky diode clamps and TIN3 did not. The device used most extensively in this study was TIN3 which had an emitter area of 4.3 μm× 2.5 μm. TOUT devices were used only in the experiments of studying voltage dependence of reverse bias induced degradation as described in Section 2.4.2 and had the same emitter area as TIN3. The layouts for TIN3 and TOUT transistors are shown in Figures 2.1 and 2.2 respectively. All I-V characteristics measured for different TIN3 and TOUT devices show only slight device to device variations. The fact that the TIN3 and TOUT devices had the same doping profile and emitter region layout resulted in almost identical I-V characteristics except for the collector-base junction. TOUT devices showed higher collector base current due to the Schottky diode clamp between the collector-base junction. All three devices were provided with double collector contacts, double emitter contacts, and a single base contact as shown in Figure 2.3. The chips were wired bond by IBM in 28 pin ceramic packages. For TIN3, the pin-to-pin resistance between the two collector contacts was approximately 21 Ω whereas for TOUT, the resistance was approximately 5.2 Ω. For the two common emitter contacts, the pin-to-pin resistance was approximately 8.5 Ω.

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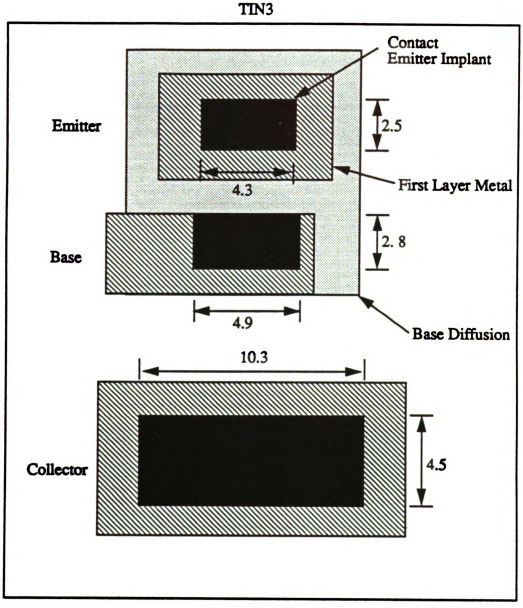

Figure 2.1: Top view of TIN3 device layout showing the contact regions, the base diffusion region, and the first level metals. The dimensions are in units of μm. Actual metal regions exceed the plotted metal regions.

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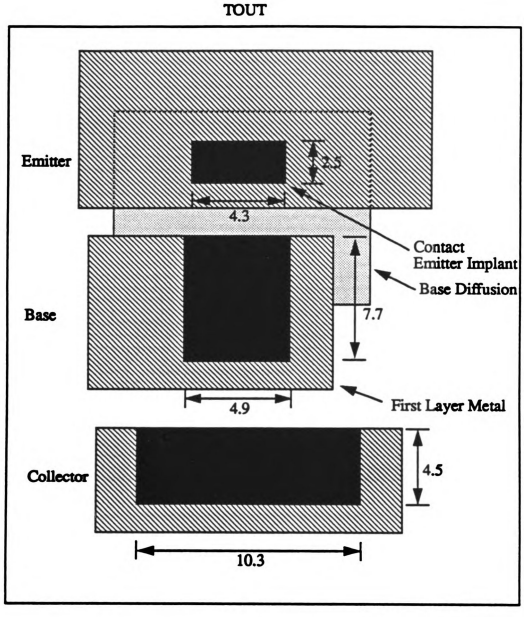

Figure 2.2: Top view of TOUT device layout showing the contact regions, the base diffusion region, and the first level metals. The dimensions are in units of μm. Actual metal regions exceed the plotted metal regions.

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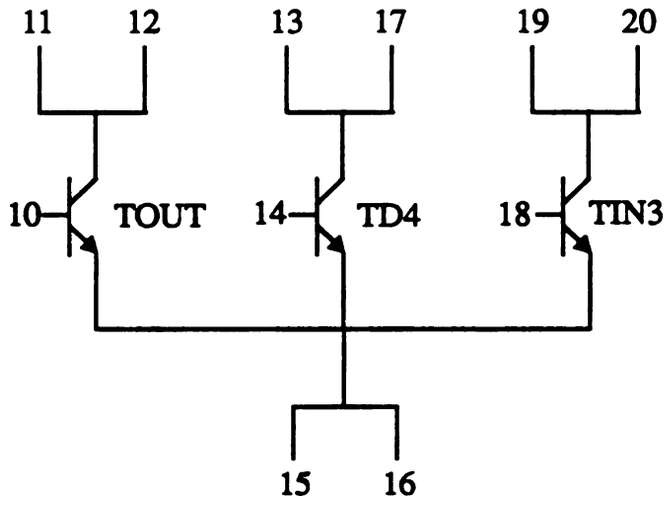

Figure 2.3: Pin out configuration of the transistors. The three transistors have two common emitter pins.

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Both collector contacts and both emitter contacts were used during stressing to reduce parasitic resistance effects. The doping profile for these devices is shown in Figure 2.4 [36].

2.2 Device Characterization

The I-V characteristics of the transistor being stressed were measured before any stressing began and at cumulative stress times of 1, 4, 24, 100, 200, 500, and 1000 hours during the stress. The I-V characteristics measured consisted of the following set of six I-V measurements:

(1) I_{EBO} forward, $0 \leq V_{BE} \leq 0.8$ V and $I \leq$ 1mA.

(2) I_{EBO} reverse, $-2 \leq V_{BE} \leq 0$ V.

(3) I_{CBO} forward, $0 \leq V_{BC} \leq 0.8$ V and $I \leq$ 1mA.

(4) I_{CBO} reverse, $-5 \leq V_{BC} \leq 0$ V.

(5) I_C, I_B with $V_{BC} = 0$ and $0 \leq V_{BE} \leq 0.8$ V, $I \leq$ 1 mA. (Gummel plot)

(6) Family of curves, I_C versus V_{CE} and I_B.

Figure 2.5 shows the circuit configuration for each of the tests. Double contacts were used for the emitter and collector during device testing. Measurements were performed on a Hewlett-Packard 4145B Semiconductor Parameter Analyzer in the long integration time mode, except for the family of curves for which the medium integration time mode was used. The medium integration time mode takes 16.7 msec for each current measurement while the long integration time mode takes 270 msec. The minimum resolution of the HP 4145 is 1 mV for the source voltage and 1 pA for the current measurement. The voltage accuracy is $\pm$(0.1% measured values + 10 mV + 0.4 Ω * I_o) and the current accuracy is $\pm$(1% measured values + 6 pA + 20 fA * V_o). I_o and V_o are the output current and output voltage, respectively.

The measurements were performed at T= 23 C $\pm$ 1 C in a Thermotron S1.2 environmental chamber. The data collected was then transferred to a Unix computer

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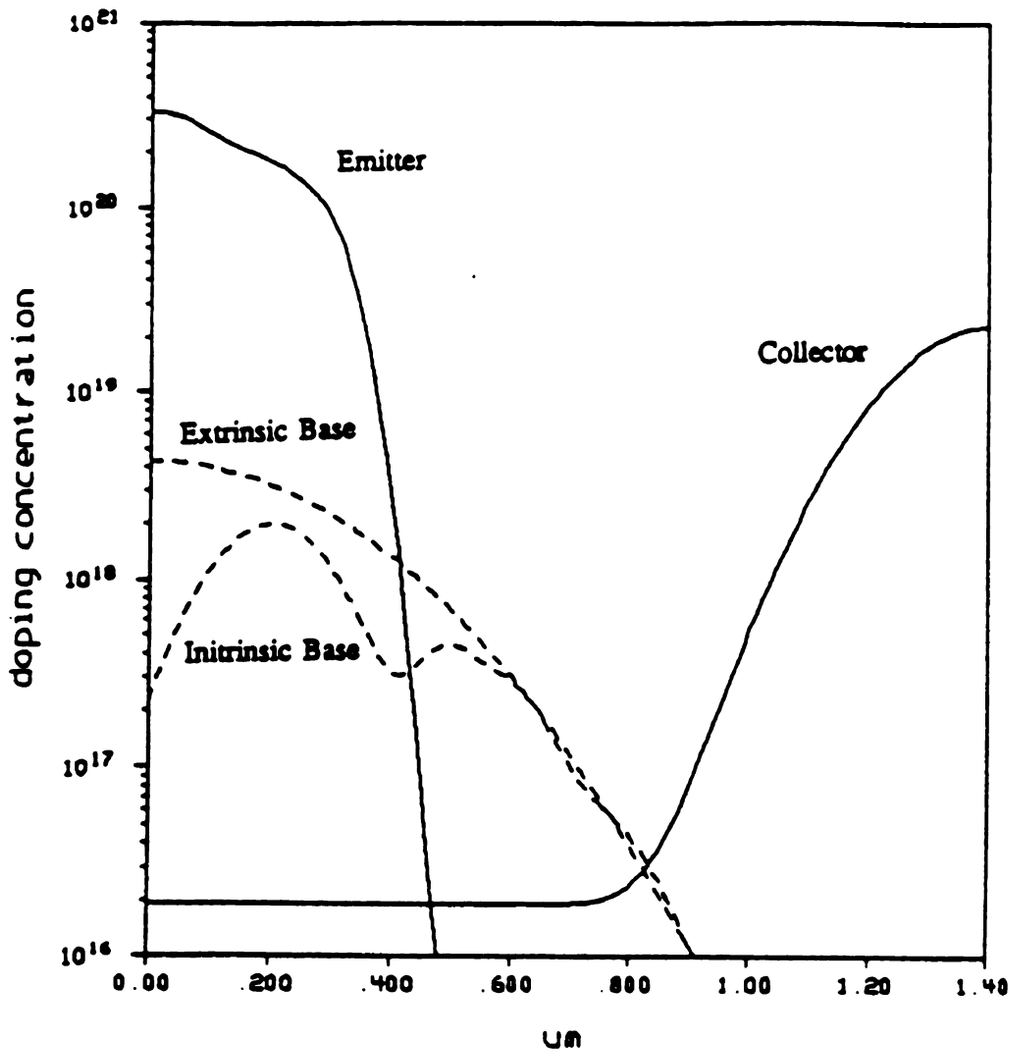

Figure 2.4: Doping profile for the devices used in this study. The impurity concentrations are in units of cm^{-3}.

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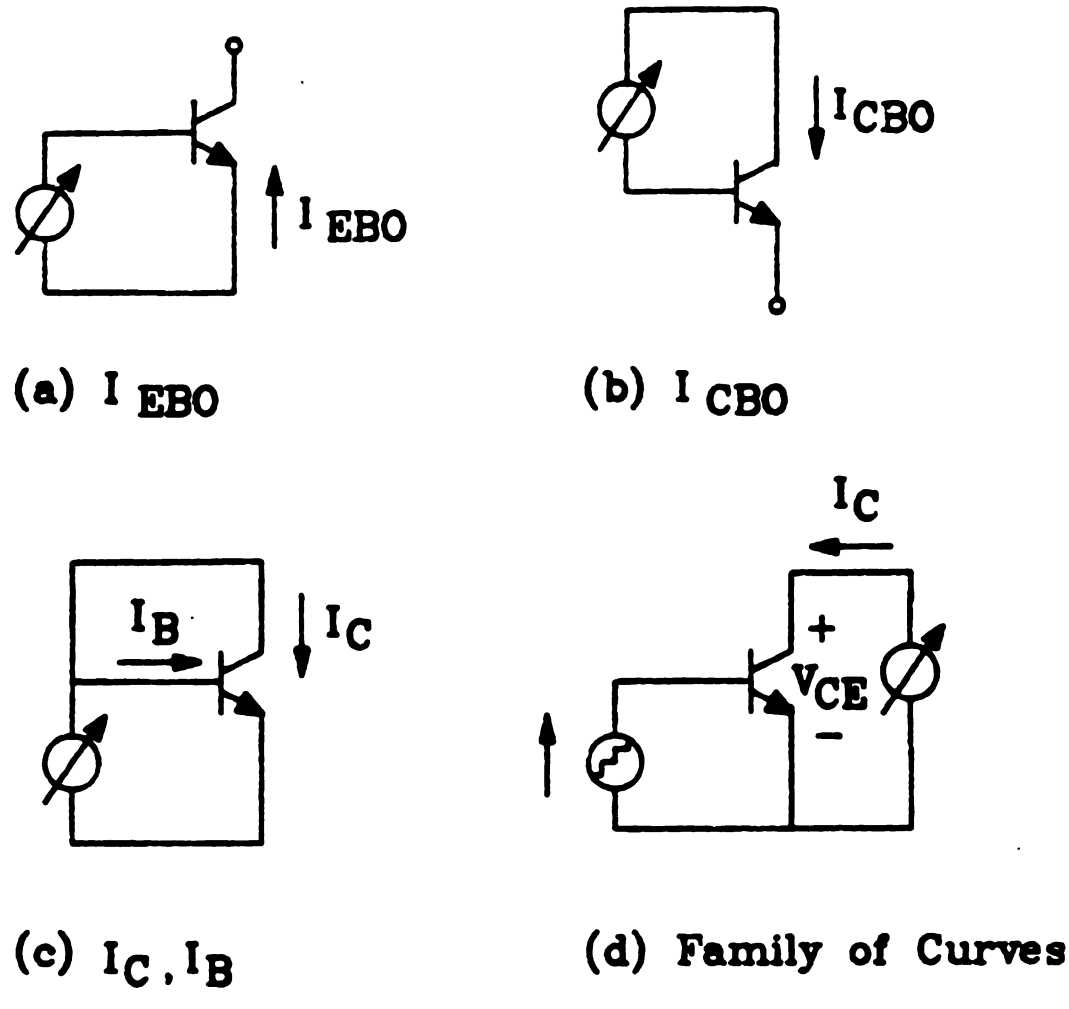

Figure 2.5: Circuit configuration for the measurements: (a) I_{EBO} forward and reverse, (b) I_{CBO} forward and reverse, (c) Gummel plot, and (d) family of curves.

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2.3 Unstressed BJT Characteristics

Typical unstressed BJT characteristics are plotted in Figures 2.7 to 2.12 showing the device to device variation for TIN3 and TOUT. Figures 2.7 and 2.8 show I_{EBO} versus V_{BE} for forward and reverse bias of a population of six TIN3 transistors and six TOUT transistors. Figures 2.9 and 2.10 show I_{CBO} for forward and reverse bias V_{BC} voltages. The TOUT device shows larger collector base current due to the presence of Schottky diode clamps. The characteristics studied most extensively were the current gain and Gummel plot curves. The unstressed characteristics measurements for these devices are shown in Figures 2.11 and 2.12. Figure 2.11 shows that in a total population of 12 devices, the maximum and minimum gain are 71 and 57 for V_{BE} = 0.6 V, respectively. Figure 2.12 shows the Gummel plots for the 12 devices.

2.4 DC Reverse Bias Stressing Experiments

2.4.1 Temperature Dependence of Reverse Bias Induced Degradation Experiment

At a variety of temperatures from -75 C to 240 C, transistors were stressed with the circuit shown in Figure 2.13 which reverse bias stressed the TIN3 transistors with a base-emitter voltage of -4 volts. The transistors during stressing were placed in an environmental chamber or oven as shown in Figure 2.14 in order to provide the desired ambient temperature. The Thermotron S1.2 environmental chamber was used to provide ambient temperatures of -75, 23, and 175 C. The temperature of the Thermotron S1.2 is automatically controlled by the built-in thermocouple sensor and a heater/refrigerator unit. The accuracy of the temperature is ± 1 C. A Blue M model OV-18SA oven was used to provide ambient temperatures of 175 and 240 C. The temperature of the Blue M

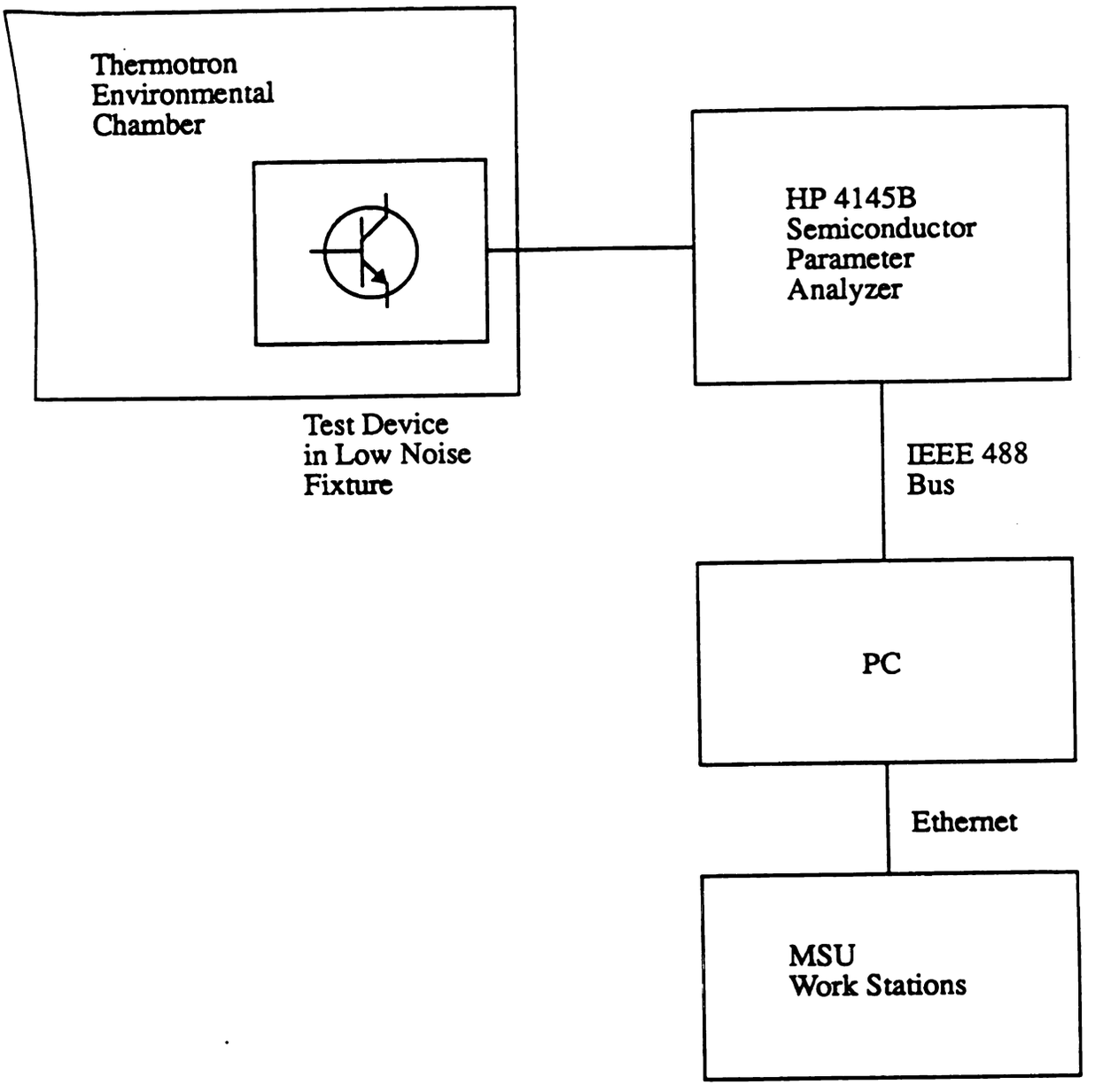

Figure 2.6: Diagram for the measurement setup.

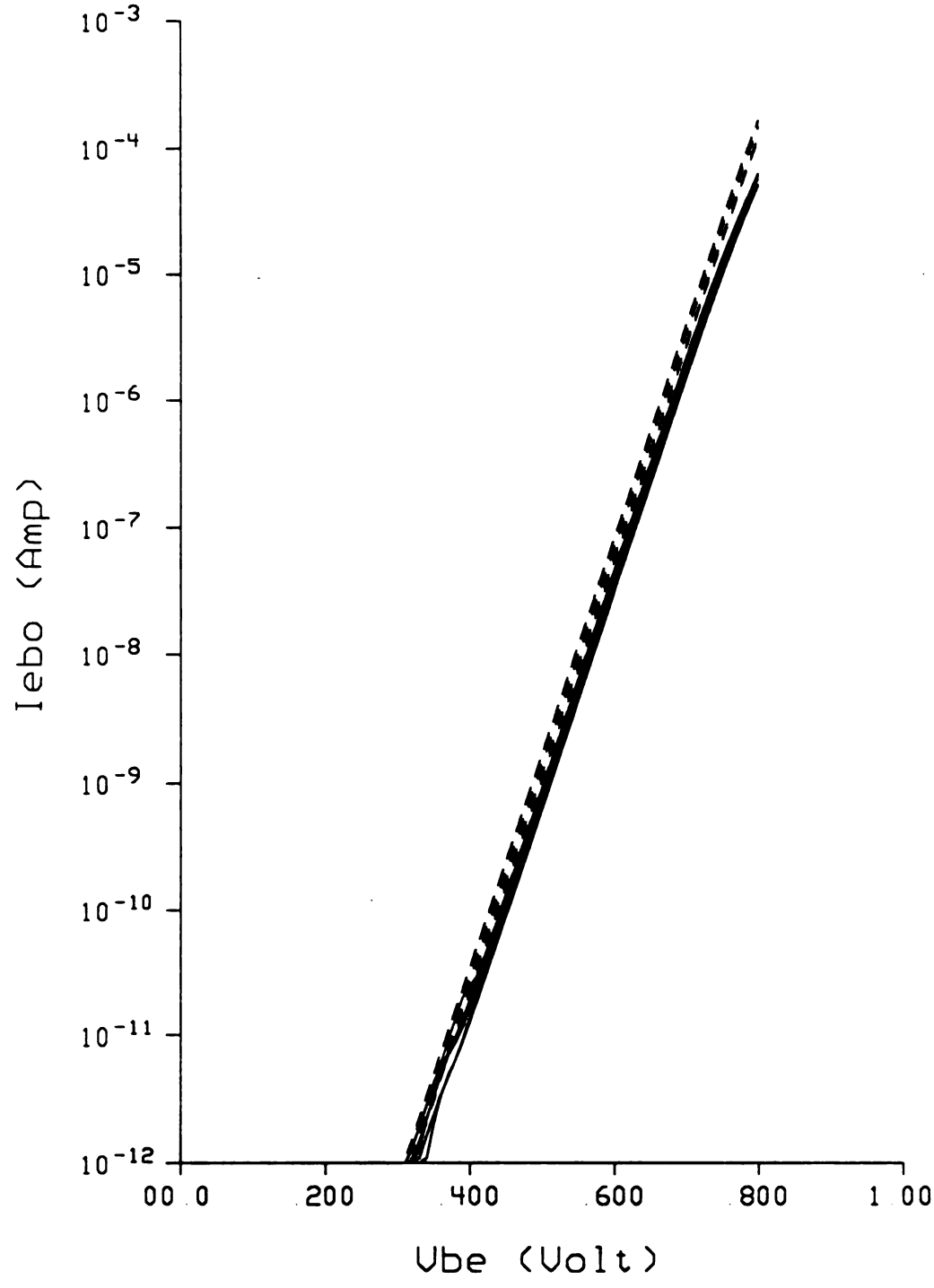

Figure 2.7: Forward biased I_{EBO} versus V_{BE} characteristics of a population of six TIN3 transistors (solid lines) and six TOUT transistors (dashed lines).

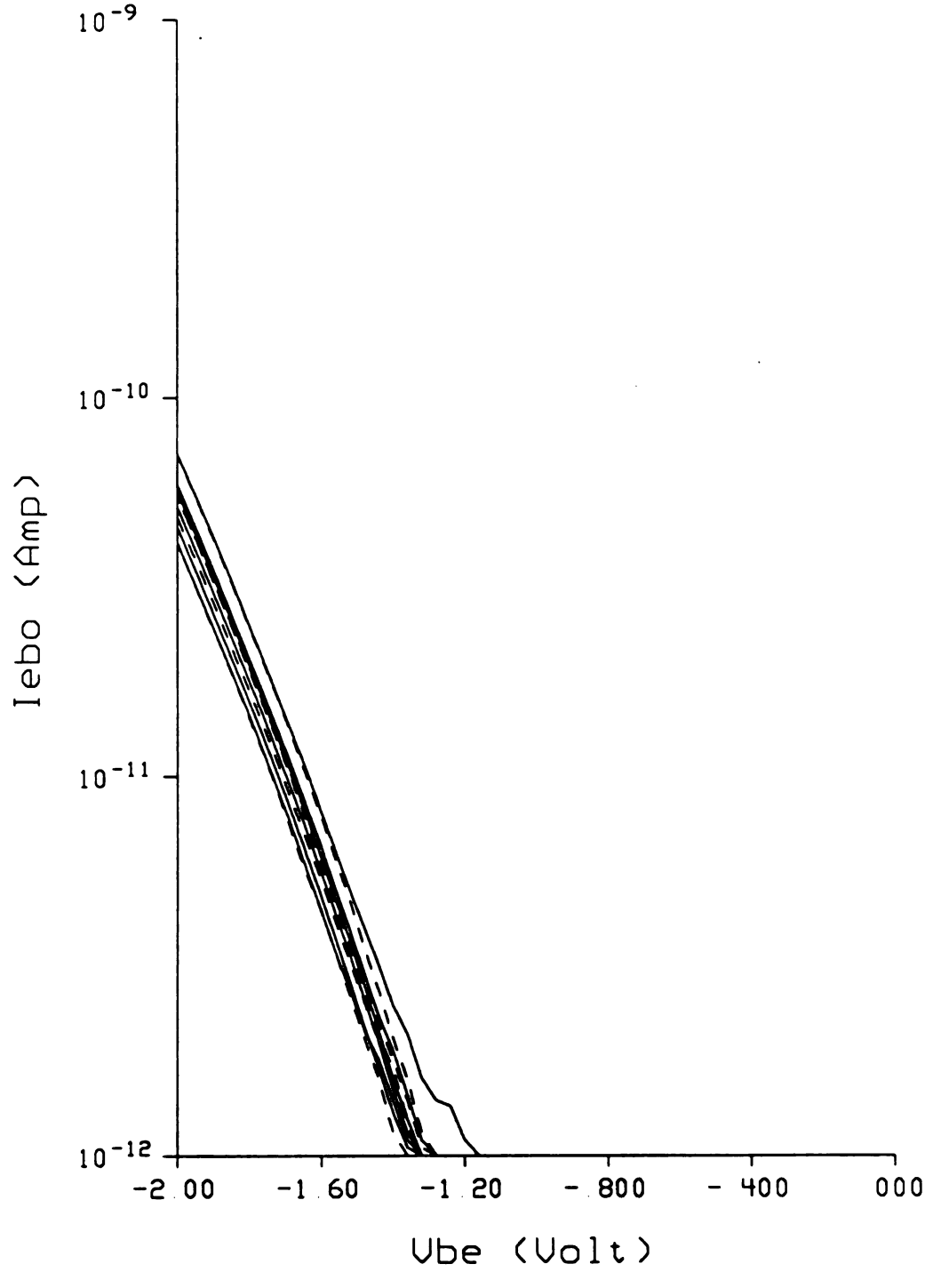

Figure 2.8: Reverse biased I_{EBO} versus V_{BE} characteristics of a population of six TIN3 transistors (solid lines) and six TOUT transistors (dashed lines).

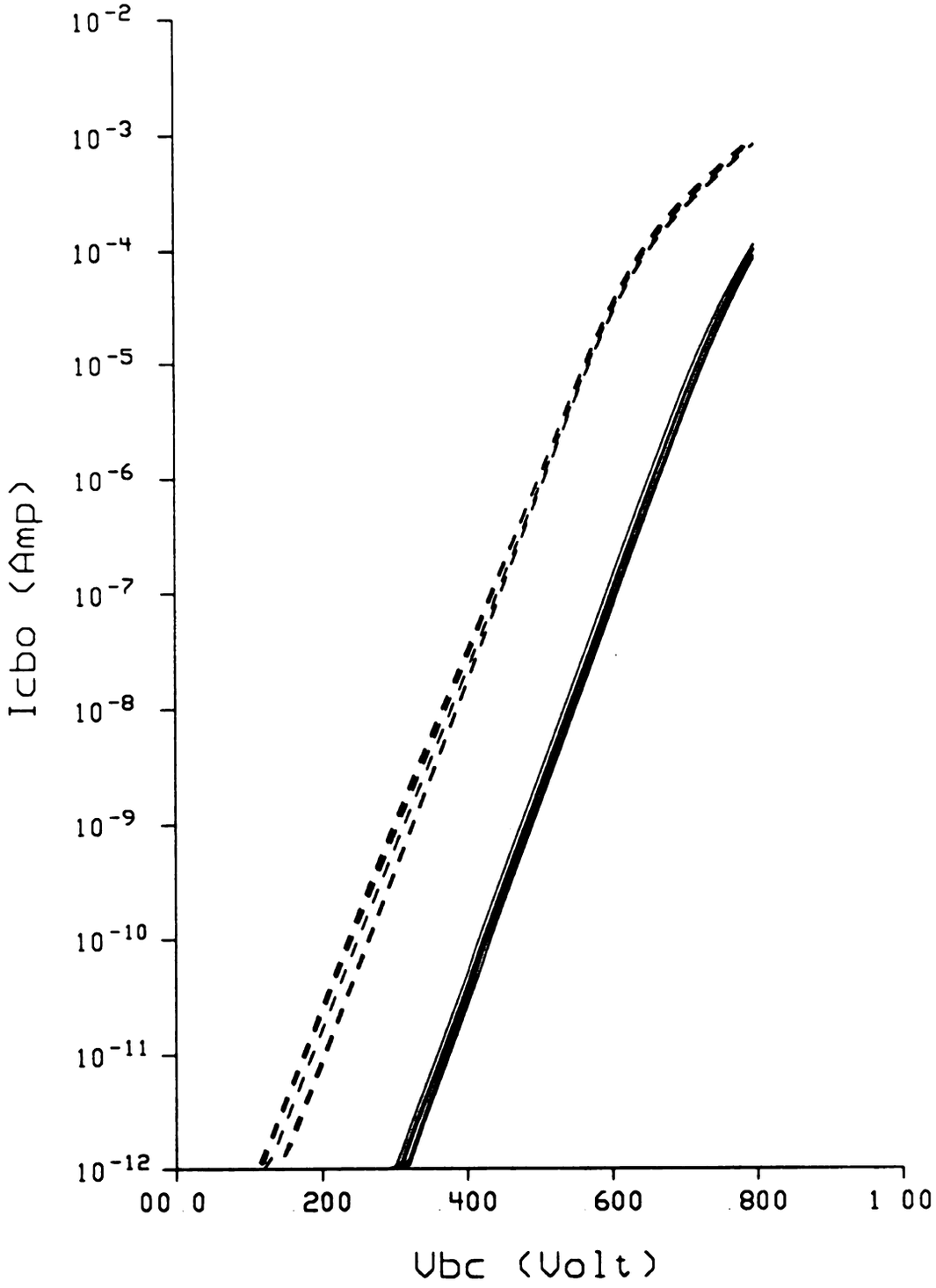

Figure 2.9: Forward biased I_{CBO} versus V_{BC} characteristics of a population of six TIN3 transistors (solid lines) and six TOUT transistors (dashed lines).

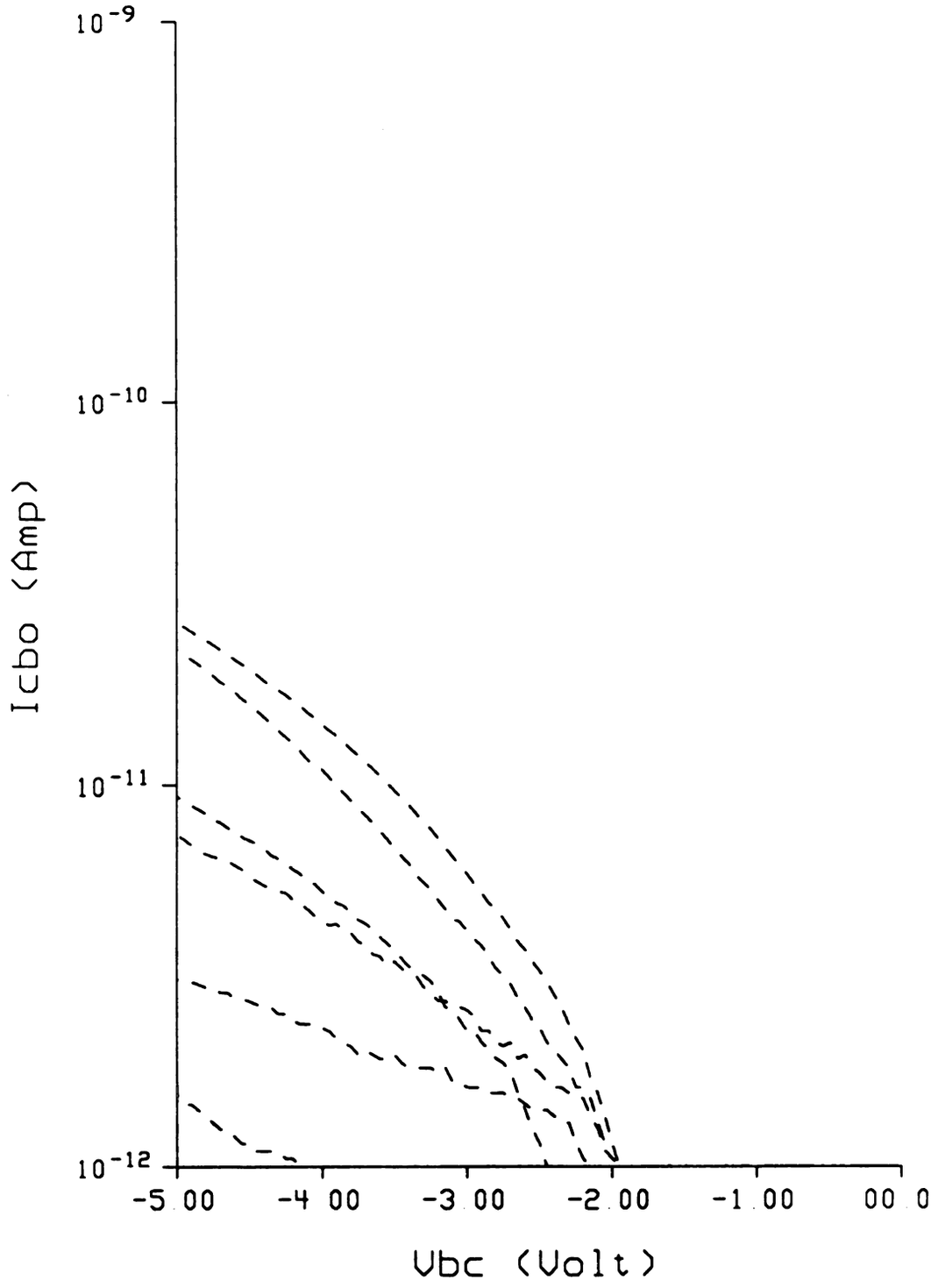

Figure 2.10: Reverse biased I_{CBO} versus V_{BC} characteristics of a population of six TIN3 transistors (solid lines) and six TOUT transistors (dashed lines). All six TIN3 transistors had currents of less than 1 pA.

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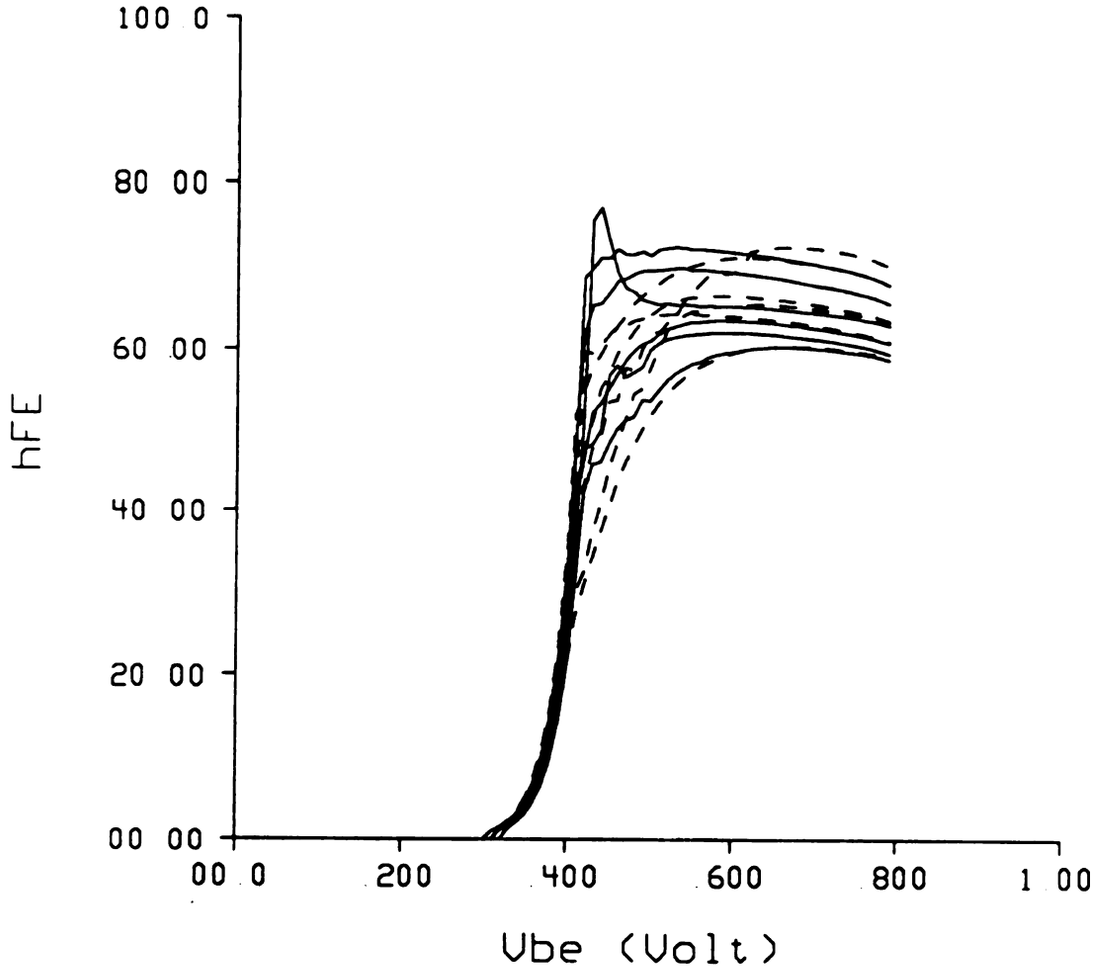

Figure 2.11: Current gain characteristics of a population of six TIN3 transistors (solid lines) and six TOUT transistors (dashed lines).

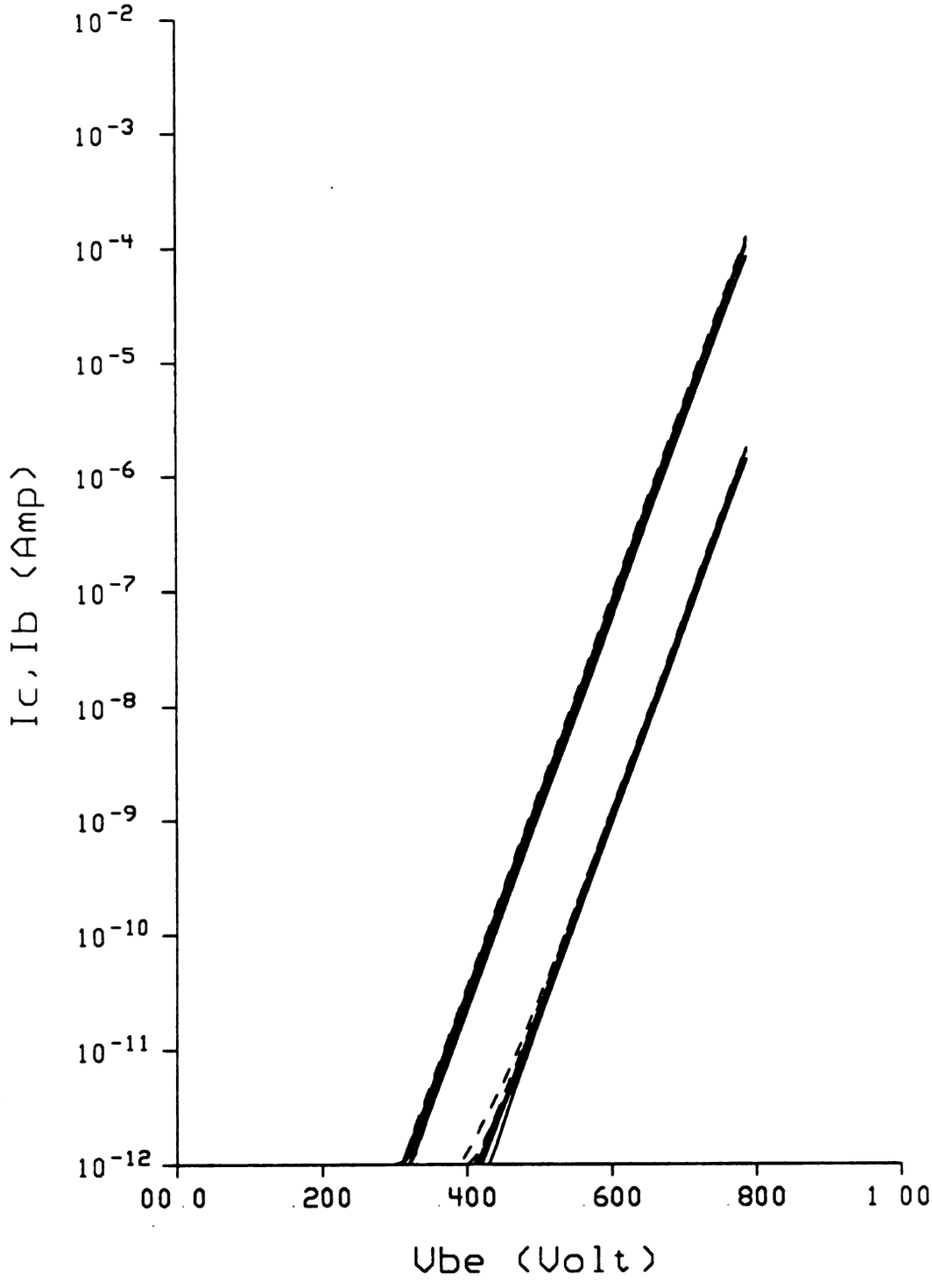

Figure 2.12: Gummel characteristics of a population of six TIN3 transistors (solid lines) and six TOUT transistors (dashed lines).

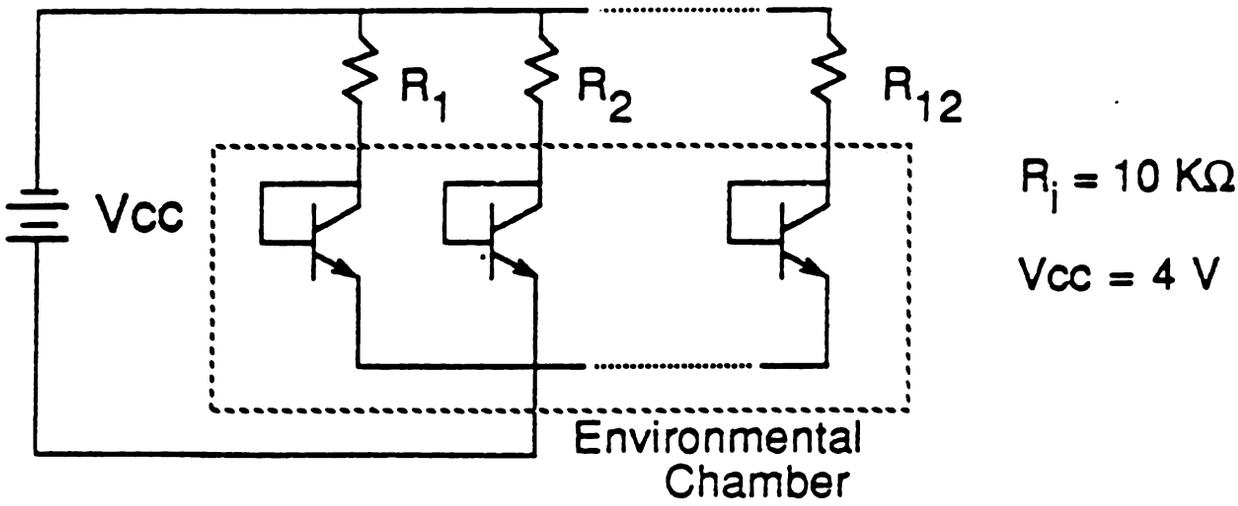

Figure 2.13: Circuit for stressing the transistors.

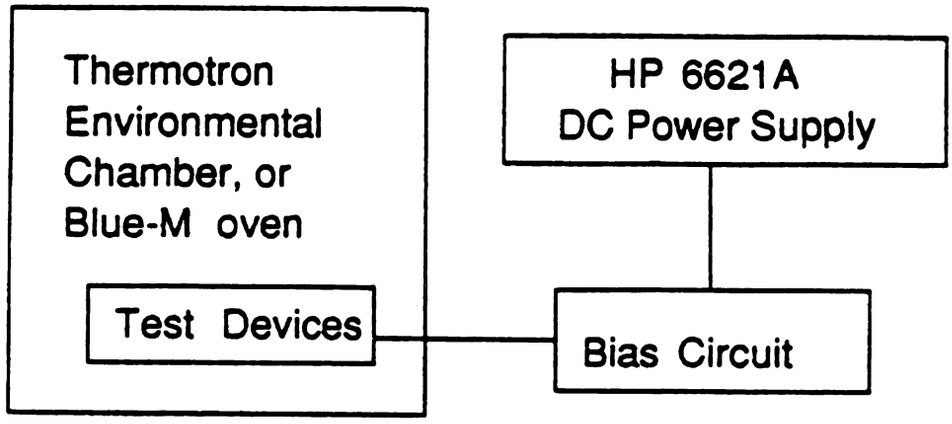

Figure 2.14: The transistors were placed in an environmental chamber or oven to provide the desired ambient temperature.

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oven was monitored by using a mercury thermometer of resolution 1 degree Celsius and adjusted by turning the analog dial on the front panel. The temperature provided by Blue M was controlled within ±5 C. The detailed stress conditions used in this experiment were:

- -75 C for 1000 hours (12 TIN3 devices)
- +23 C for 500 hours (12 TIN3 devices)
- +175 C for 1000 hours (12 TIN3 devices)
- +240 C for 1000 hours (12 TIN3 devices)

For the above listed stress experiments, each group of 12 devices were equally divided between two job numbers and each subgroup of 6 devices contained one chip from each of the 6 possible wafer locations. This mixing of job numbers and chip locations was done to reduce the influence of job number and chip location on the final results. Missing devices and bad devices caused some minor deviations from this overall strategy. In addition to the devices being stressed, for each temperature stress condition two chips were used as control devices which were exposed to the same temperature as the stressed devices, but not the electrical stress. The control devices were seen to exhibit no change in the electrical characteristics measured.

A reverse bias stress of -4 volts caused a degradation in the current gain versus V_{BE} as shown in Figure 2.15 for stressing at -75 C. The largest change in the current gain occurred at base-emitter voltages less than 0.9 volts. Gain degradation is due to the increase in the base current as shown in Figure 2.16. The base current changes are the changes most expected since the base current is most susceptible to non-ideal transistor effects. And it is at lower biases that the changes in the base current are most significant percentage-wise. The collector current is unaffected by the reverse bias stress condition. The gain degradation versus time at V_{BE} = 0.6 volts for several individual devices is shown in Figure 2.17 where it can be noted that the gain degradation occurred with a similar behavior in all devices. A comparison of the normalized current gain [stressed

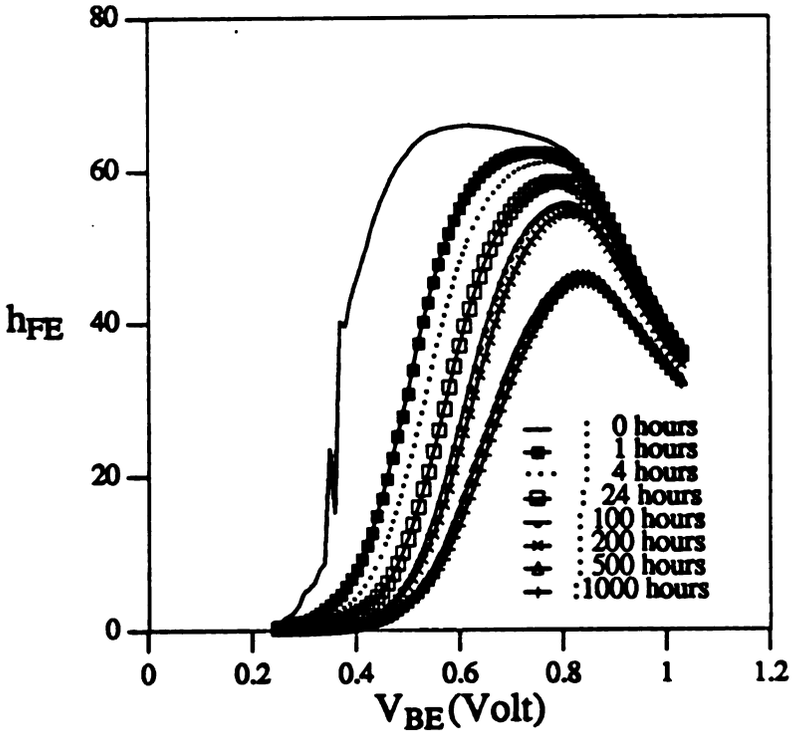

Figure 2.15: Current gain versus V_{BE} for stressing at -75 C for various stress times up to 1000 hours.

Figure 2.1

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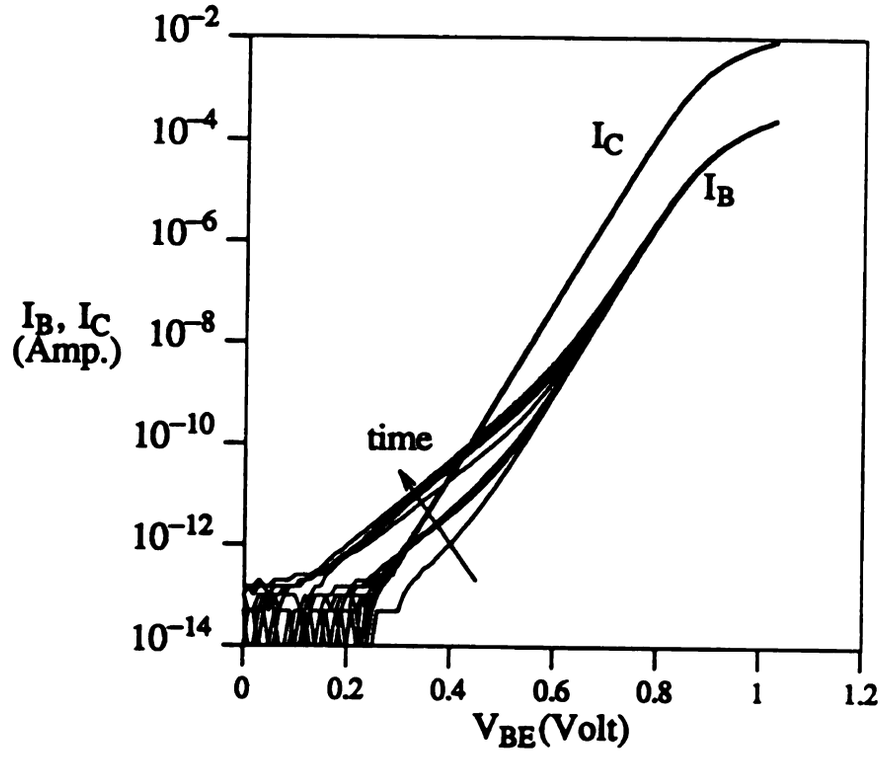

Figure 2.16: Gummel plots for stressing at -75 C for various stress times up to 1000 hours.

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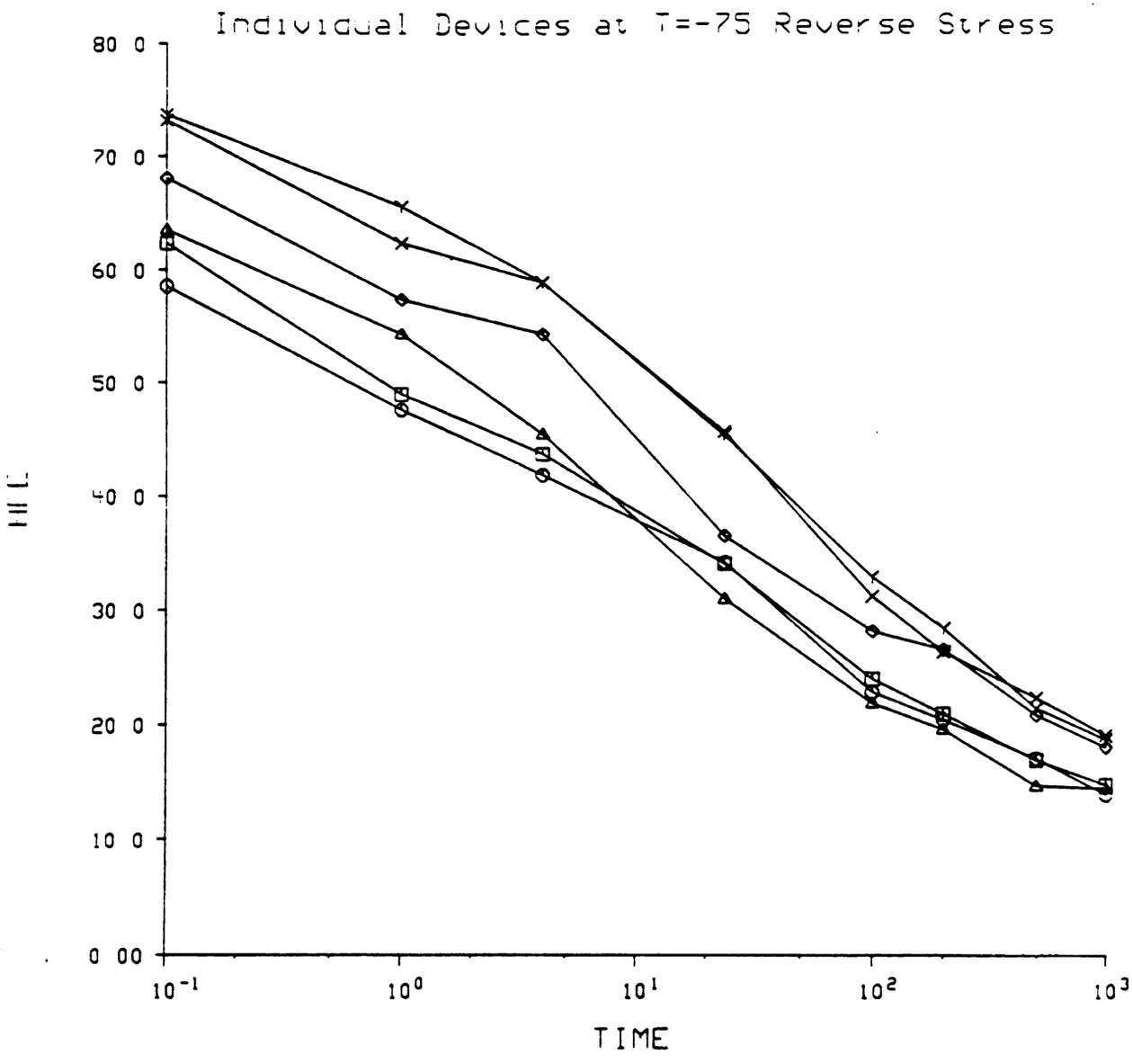

Figure 2.17: Gain degradation versus time at V_{BE} = 0.6 V for several individual devices stressed at -75 C.

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current gain / prestressed current gain] for the four stress temperatures (-75 C, 23 C, 175 C, 240 C) is shown in Figure 2.18. The largest degradation occurred at the lower ambient temperature. Additional examination of the experimental degradation results revealed no wafer location or job number variation in the degradation.

The base current change can be plotted as a function of the stress charge which is defined as the product of stress time and stress current. The stress current increases as the ambient temperature increases. The currents for typical devices were 28.3 nA, 54.3 nA, 0.329 μA, and 1.94 μA for ambient temperatures of -75, 23, 175, and 240 C, respectively. Figure 2.19 shows the base current change versus stress charge for the four stress temperatures.

After reverse stressing, the forward and reverse characteristics of the collector-base junction were seen to be unchanged and the emitter-base junction exhibited higher leakage current in both forward and reverse characteristics. The pre-stress and post-stress I_{EBO} verses V_{BE} characteristics is shown in Figure 2.20 for stressing at -75 C for 1000 hours.

2.4.2 Voltage Dependence of Reverse Bias Induced Degradation Experiment

The voltage dependence of the degradation rate was investigated by stressing TOUT transistors with a range of reverse bias voltages. The bipolar transistors were stressed at room temperature with reverse biases of 3.5, 4.0, 4.5, and 5.0 volts. The circuit diagram of the stress setup is shown in Figure 2.21 where a voltage divider is used for the circuit to provide the four voltages simultaneously. The detailed stress conditions were

- -3.5 volts for 200 hours (3 TOUT devices)
- -4.0 volts for 200 hours (3 TOUT devices)
- -4.5 volts for 200 hours (3 TOUT devices)
- -5.0 volts for 200 hours (3 TOUT devices)

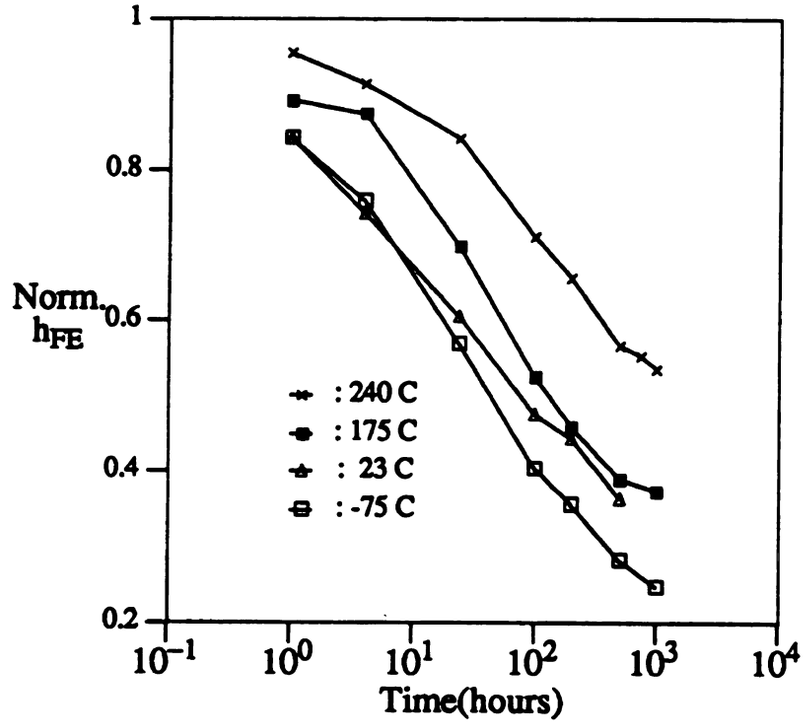

Figure 2.18: Normalized current gain [stressed current gain / prestressed current gain] for stress temperatures of -75, 23, 175, and 240 C.

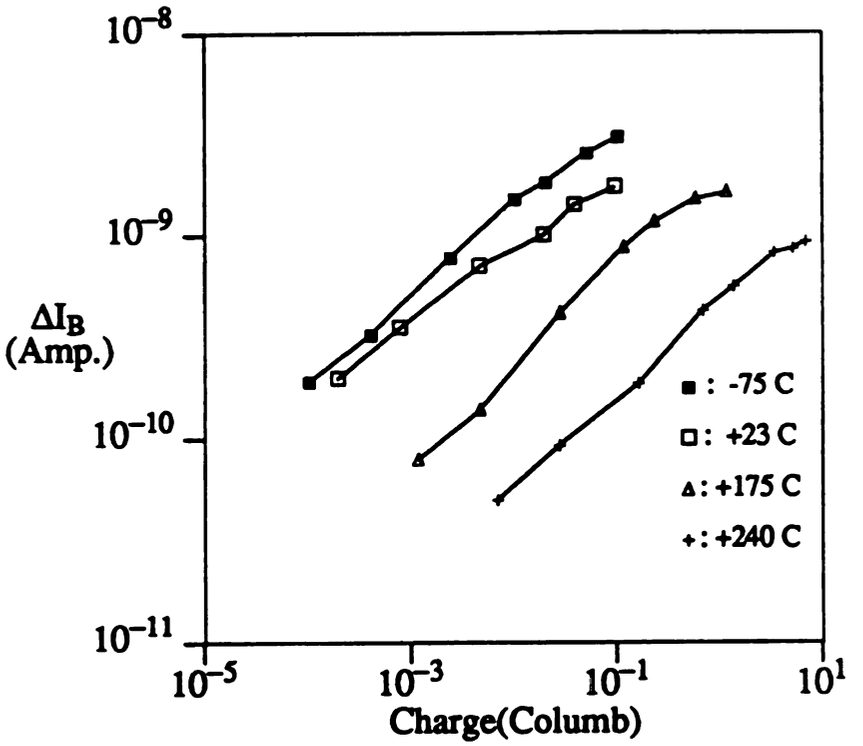

Figure 2.19: Base current change versus stress charge for stress temperatures at -75, 23, 175, and 240 C.

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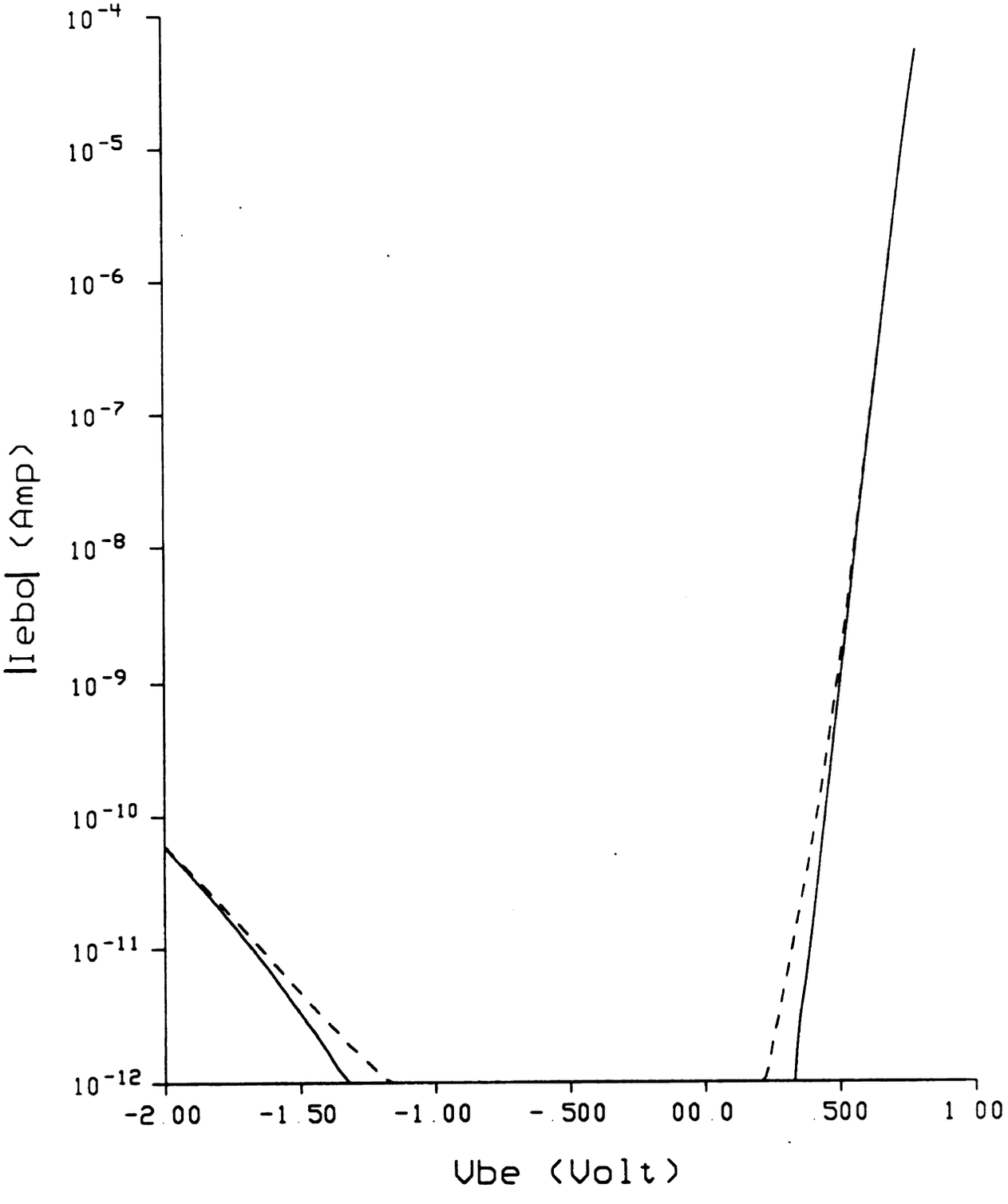
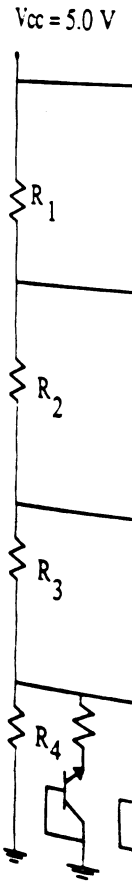


Figure 2.20: Pre-stress (solid line) and post-stress (dashed line) $|I_{EBO}|$ versus V_{BE} for a device stressed at -75 C for 1000 hours.



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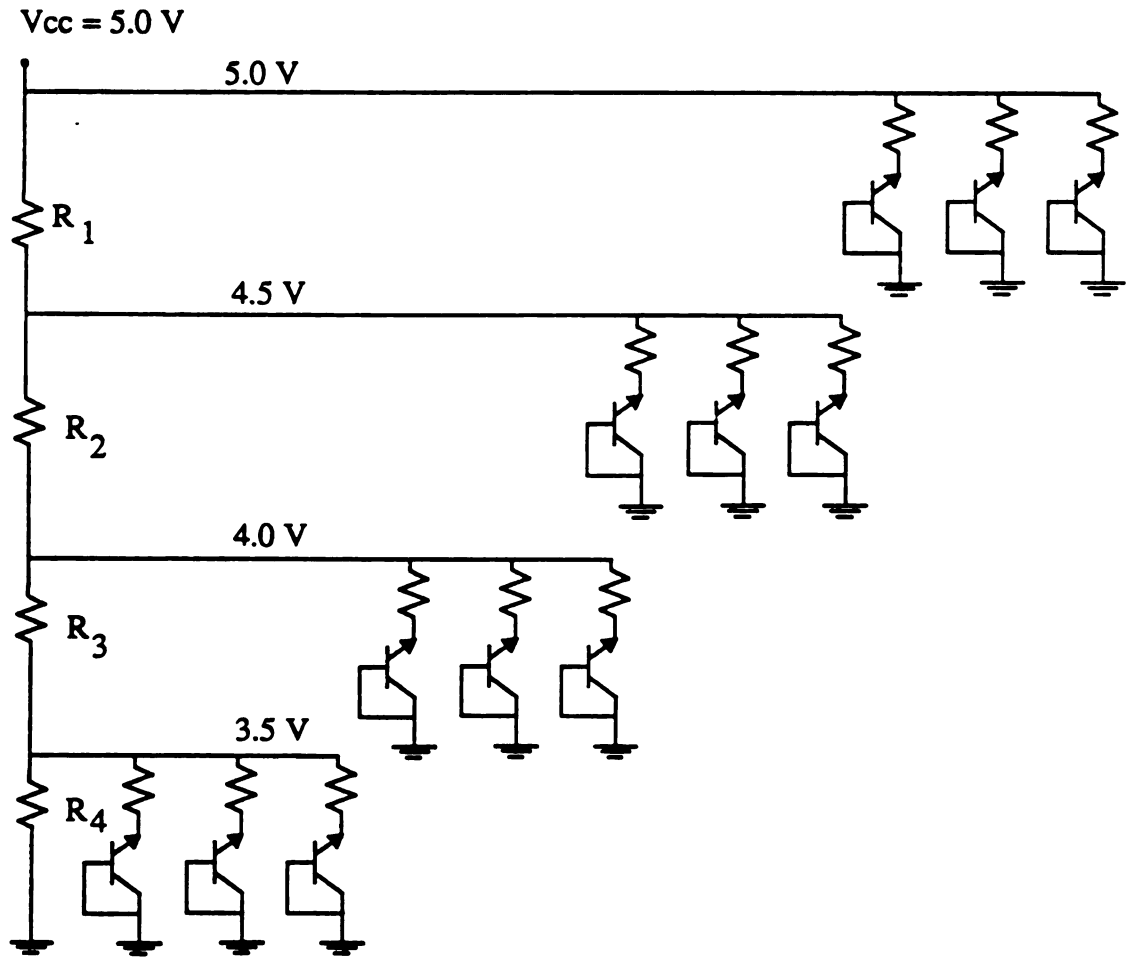

Figure 2.21: Circuit diagram for stressing TOUT transistors. The resistors used are: $R_1 = R_2 = R_3 = 47$ ohm, $R_4 = 317$ ohm, and all other resistors are 100 kohm.

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In addition to the 12 stressed devices, two control device went through the same measurement procedure but had no electrical bias applied during stressing. The control devices showed no change in the characteristics measured.

The stressing were interrupted at cumulative stress times of 1, 4, 24, 100, and 200 hours for the characterization of the changes in the BJT characteristics. The measurement setup was the same as that described earlier in Figure 2.6, i.e., 23 C in a temperature controlled chamber and I-V characteristics measured with the HP 4145B. The I-V measurements taken for this experiment were

(1) I_{EBO} forward, $0 \leq V_{BE} \leq 0.6$ V and $I \leq$ 1mA.

(2) I_R (Reverse stress current), $V_B = 0$, $V_C = 0$ and $0 \leq V_E \leq V_{STRESS}$.

(3) I_C, I_B with $V_{BC} = 0$ and $0 \leq V_{BE} \leq 0.8$ V (Gummel plot).

The Gummel plots showing the base and collector currents versus V_{BE} for the unstressed and stressed characteristics are shown in Figure 2.22. The degradation increased substantially as the base-emitter reverse bias voltage increased. Figure 2.23 shows the amount of the base current degradation increase at $V_{BE} = 0.6$ volts versus the total stress charge which flowed across the base emitter junction. The amount of degradation depends on the stress charge and the stress voltage. The reverse bias stress current was measured versus time for the transistors at all four different stress voltages as shown in Figure 2.24. It shows that for a given stress voltage, the stress current did not differ significantly between devices. For example, devices 62, 35, and 73 were all stressed with $V_{BE} = -4.5$ volts and they all showed about the same leakage current at this voltage. It can also be noted in this figure that the stress current changed little as the experiment proceeded out to 200 hours. Figure 2.25 shows the degradation for each of the devices stressed at -4.5 volts. By comparing this figure with Figure 2.24, it can be seen that the device with a slightly higher leakage current shows a slightly larger degradation.

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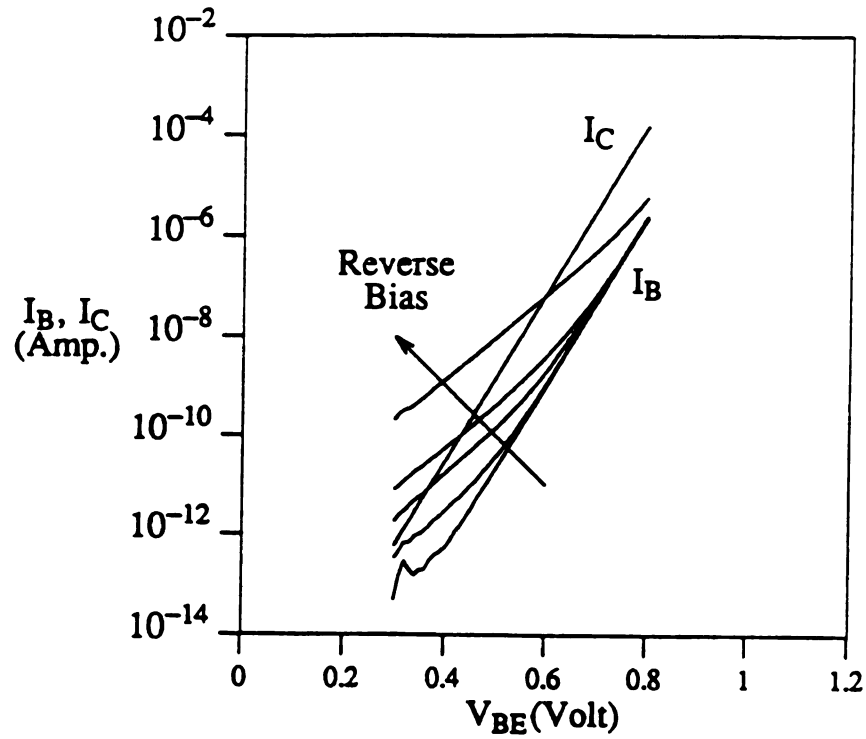

Figure 2.22: Gummel plots for the unstressed and the four stressed characteristics. TOUT devices were stressed for 200 hours at -3.5, -4.0, -4.5, and -5.0 volts.

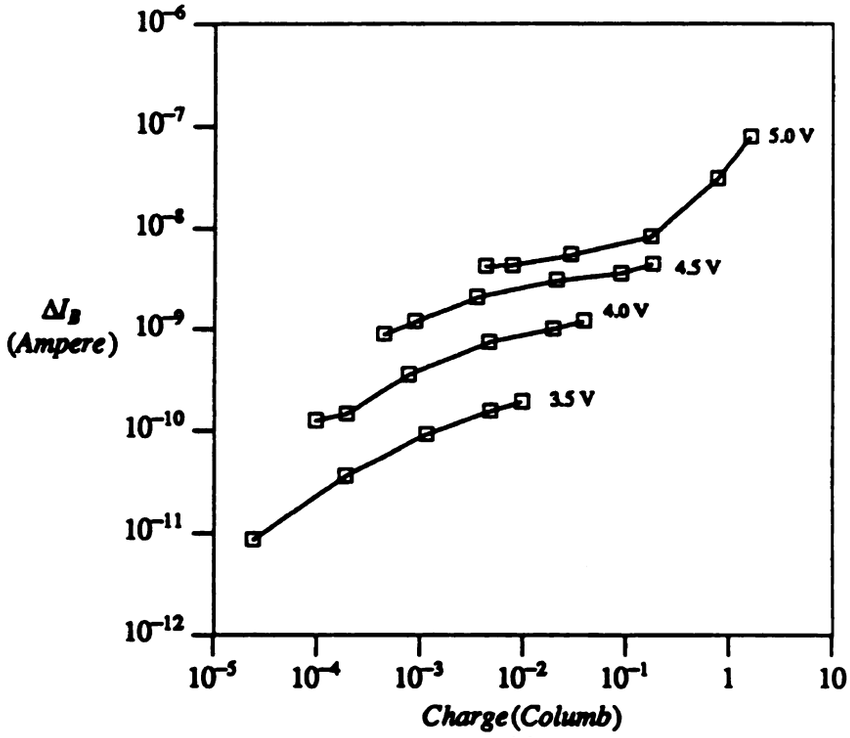

Figure 2.23: Base current change versus stress charge at V_{BE} = 0.6 volts. TOUT devices were stressed for 200 hours at -3.5, -4.0, -4.5, and -5.0 volts.

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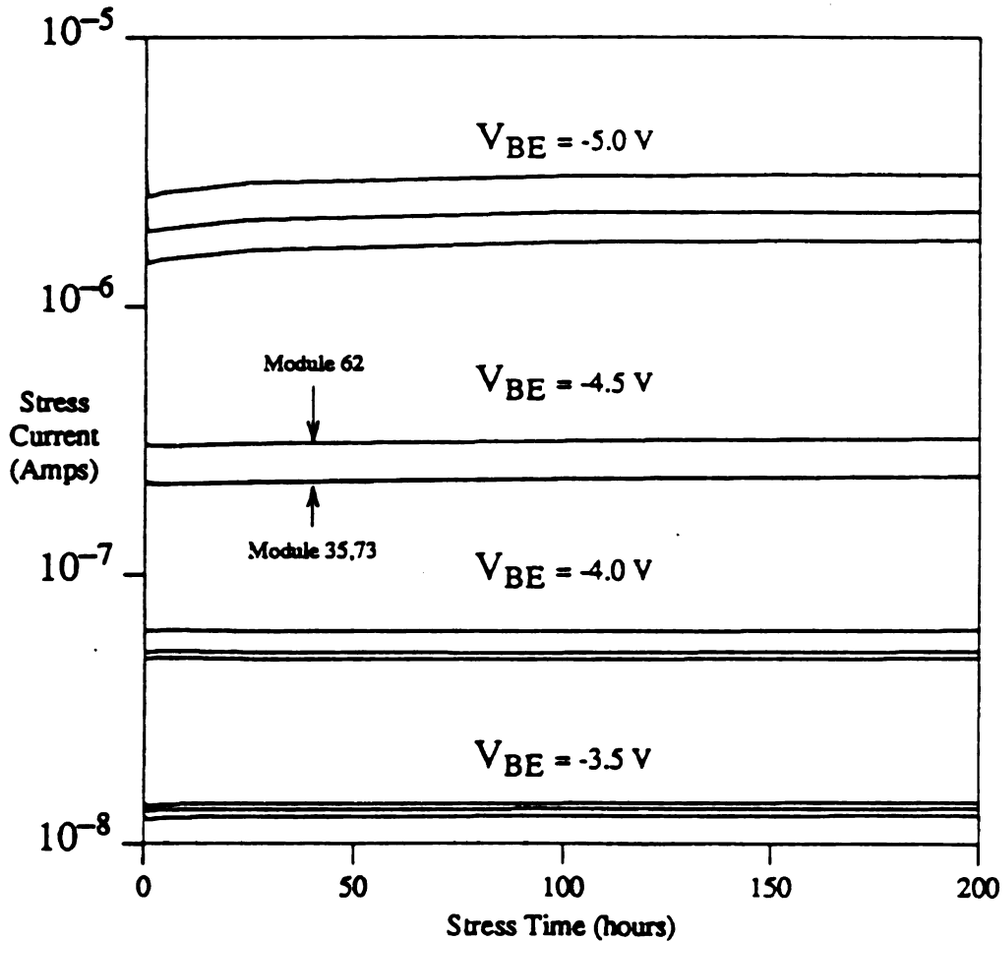

Figure 2.24: Reverse bias stress current versus time for the transistors stressed at the four stress voltages.

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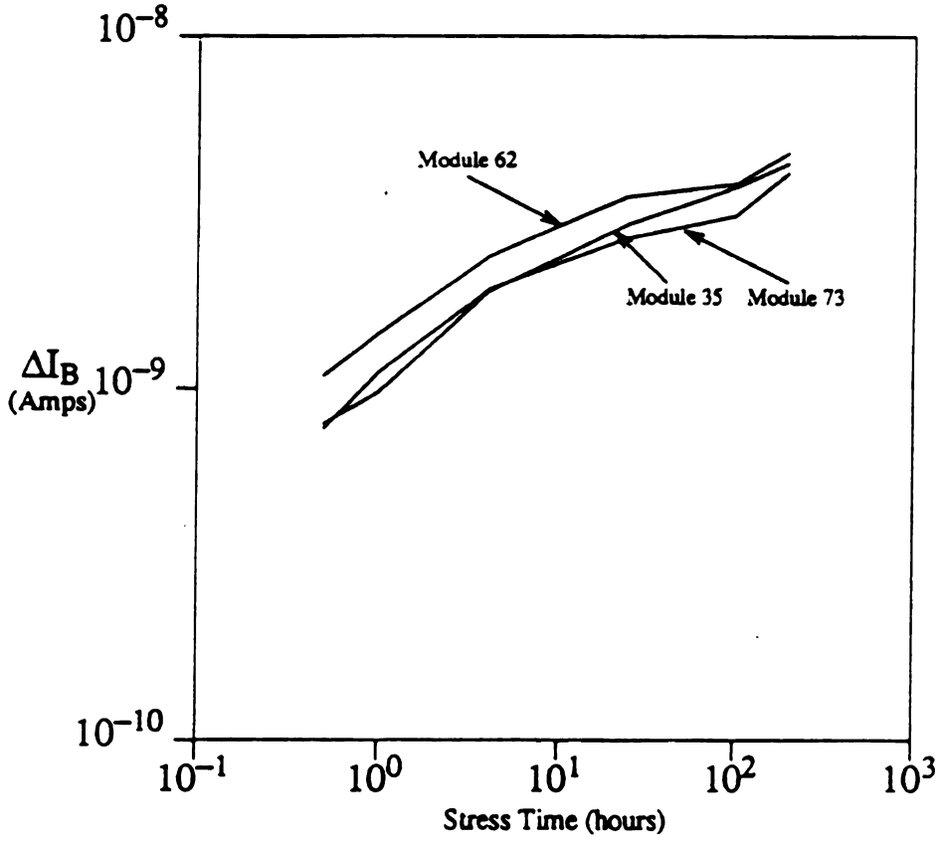

Figure 2.25: Base current change versus time for TOUT devices stressed at -4.5 volts.

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2.4.3 Short Time Scale Stress

The hot electron degradation phenomena was also investigated on a short time scale where the Gummel plot was measured after fixed stress times that were selected in the range from 1/60th of a second to 10 seconds. In order to obtain precise timing of the stress/measurement procedure, the HP 4145B was used for both stressing and measurement. By using the IEEE 488 interface bus, the HP 4145B was automatically controlled by a personal computer on which a stressing and measurement C program was executed. A TIN3 transistor was placed in the low noise test fixture for the stressing and measurement at T = 23 C.

These short stress-time degradation experiments showed that fluctuations of the base current occur as the degradation proceeds. The fluctuation is demonstrated in Figure 2.26 which shows the current gain of a transistor after being subjected to short stress periods of 10 seconds. The current gain changes are caused by fluctuations in the base current as shown in Figure 2.27. The data shows that over an extended period of time, there is a net decrease in the current gain over many stress periods. On a shorter time scale, the base current may either increase or decrease from one stress period to another. These fluctuation increases in the base current are caused by hot electrons which increase the number of degradation produced states. The fluctuation decreases in the base current are caused by a repassivation or simultaneous annealing process. This observation is consistent with measurements performed by Wachnik et. al. [17] who saw fluctuations attributed to forward stress created hot electrons via the Auger recombination process. To evaluate the possibility of the gain recovery being caused by the forward bias measurement of the current gain, an experiment was performed where after each short time interval of reverse bias stress, the transistor was forward biased for 60 seconds before the current was measured. This experiment still showed significant fluctuations of the base current with both increases and decreases in the base current observed, although to a reduced extent as shown in Figure 2.28. Figure 2.26 demonstrates that the hot

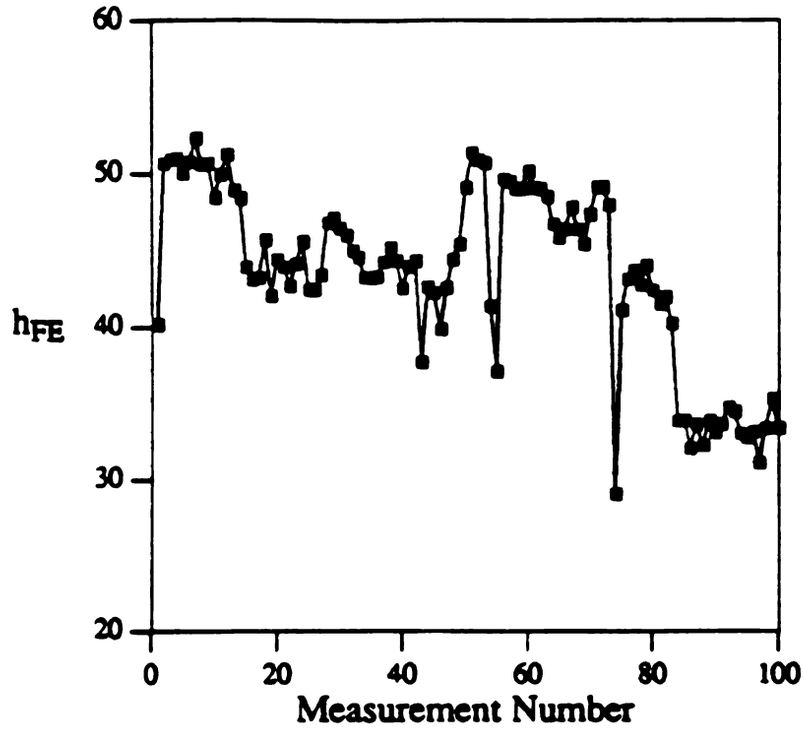

Figure 2.26: Fluctuations of the current gain at V_{BE} = 0.45 volts for transistors being subjected to short stress periods of 10 seconds. A control device subjected to the same measurement procedure with no reverse-bias stress showed current gain values changing over the range from 55 to 58 only.

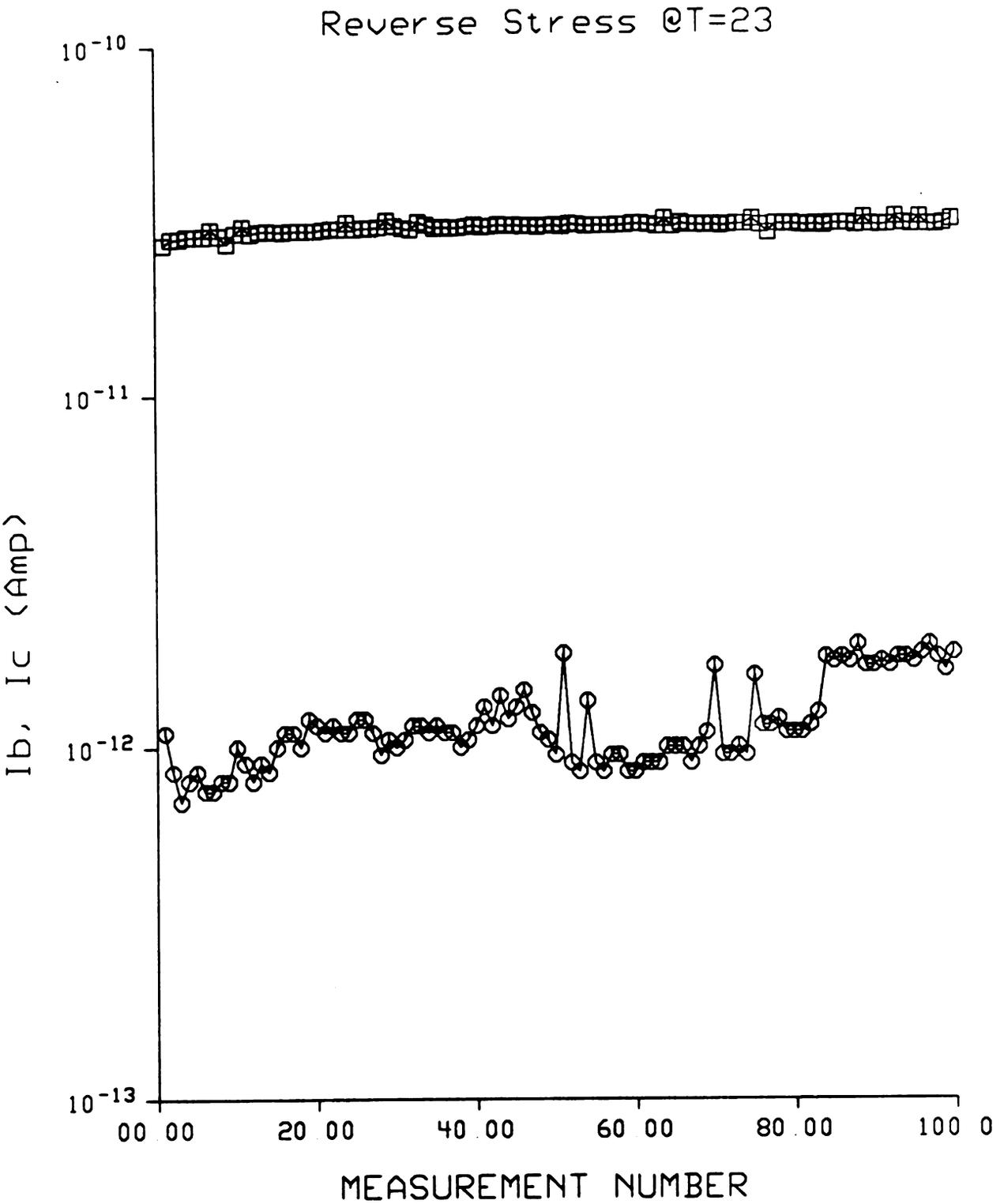

Figure 2.27: Base and collector current fluctuations for a transistors being subjected to short stress periods of 10 seconds.

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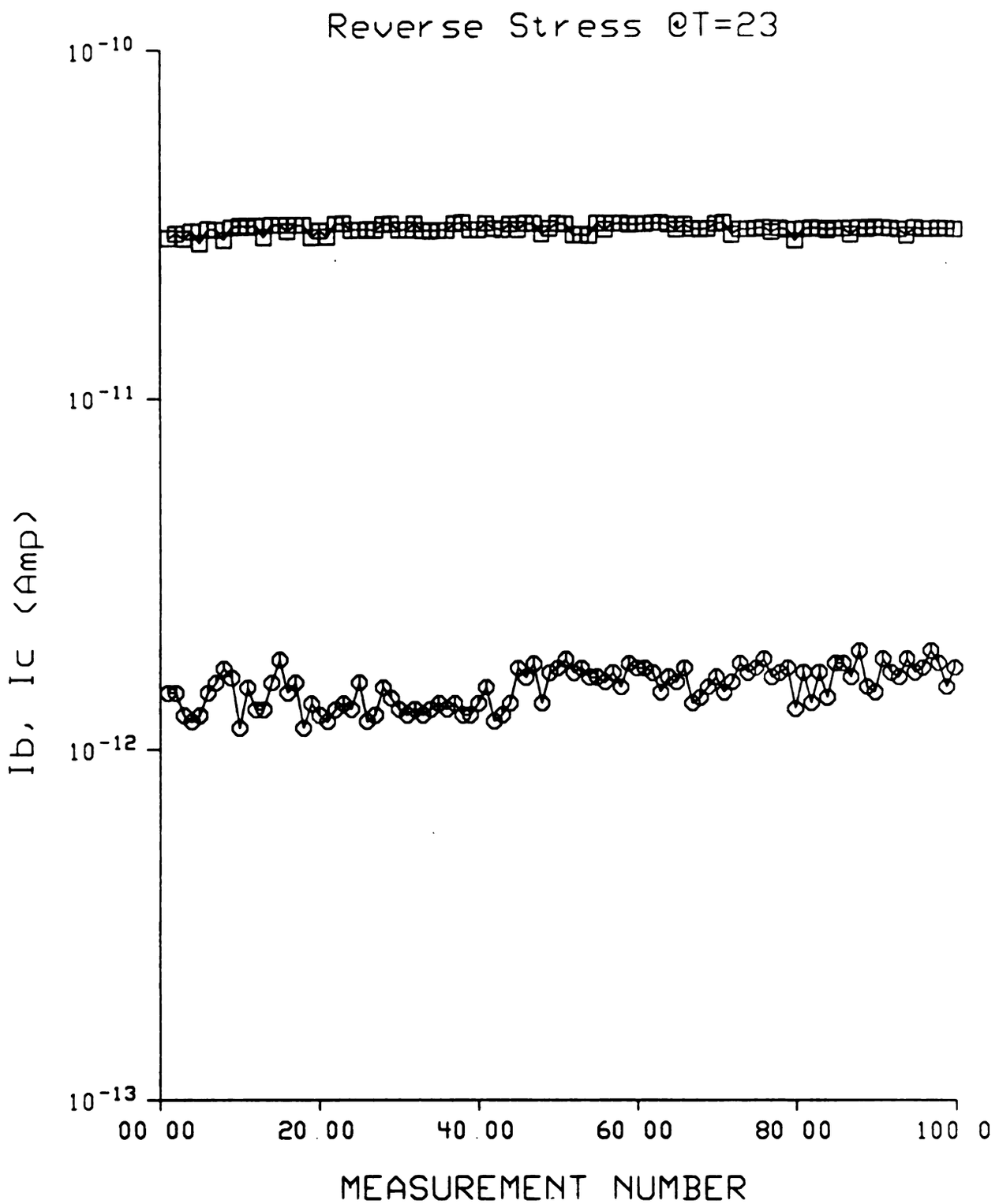

Figure 2.28: Base and collector current fluctuations for a transistor being subjected to short stress periods of 1 second followed by a subsequent forward bias of 0.6 volt for 60 seconds.

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2.4.4 Temperature Dependency of the Pre-stress and Post-stress Base Current

I-V characteristics were measured at various temperatures in order to determine the type of leakage current caused by the reverse bias stress conditions. The Gummel plots of a TIN3 transistor were measured for temperatures ranging from T = -60 C to T = 120 C in 30 C increments at a pre-stress time and at a 1000 hours post-stress time. For the temperature range of -60 C to 60 C, the measurements were performed by using the low noise test fixture provided with the HP 4145B. The test fixture was placed in the Thermotron S1.2 environmental chamber. For the temperatures of 90 and 120 C, a circuit board that could withstand high temperatures was built and placed in the environmental chamber for measurements. Figure 2.29 shows the prestress characteristics for the collector and base currents. The nonideality factor n [which gives the base current dependence on voltage $I_B \propto \exp(V_{BE}/nkT)$] is found to be n = 1.03 at T = -60 C and n = 1.01 at T = 120 C. These low non-ideality values demonstrate that the base current in a prestress device is primarily the ideal diffusion current. The post-stress characteristics are shown in Figure 2.30. The non-ideality factors for low current values are n = 2.44 at T = -60 C and n = 1.26 at T = 120 C.

The technical literature has attributed increases in the base current to three possible mechanisms [7,10,11,37] which include Schockly-Reed-Hall (SRH) recombination current, Poole-Frenkel electrical field enhanced recombination current, and trap-assisted tunneling current (or excess current). Assuming the trap level is in the middle of energy gap, the SRH recombination R_S for a surface can be expressed as

$$R_S = \frac{np - n_i^2}{\frac{1}{S_{op}}(n + n_i) + \frac{1}{S_{on}}(p + n_i)} \qquad (2.1)$$

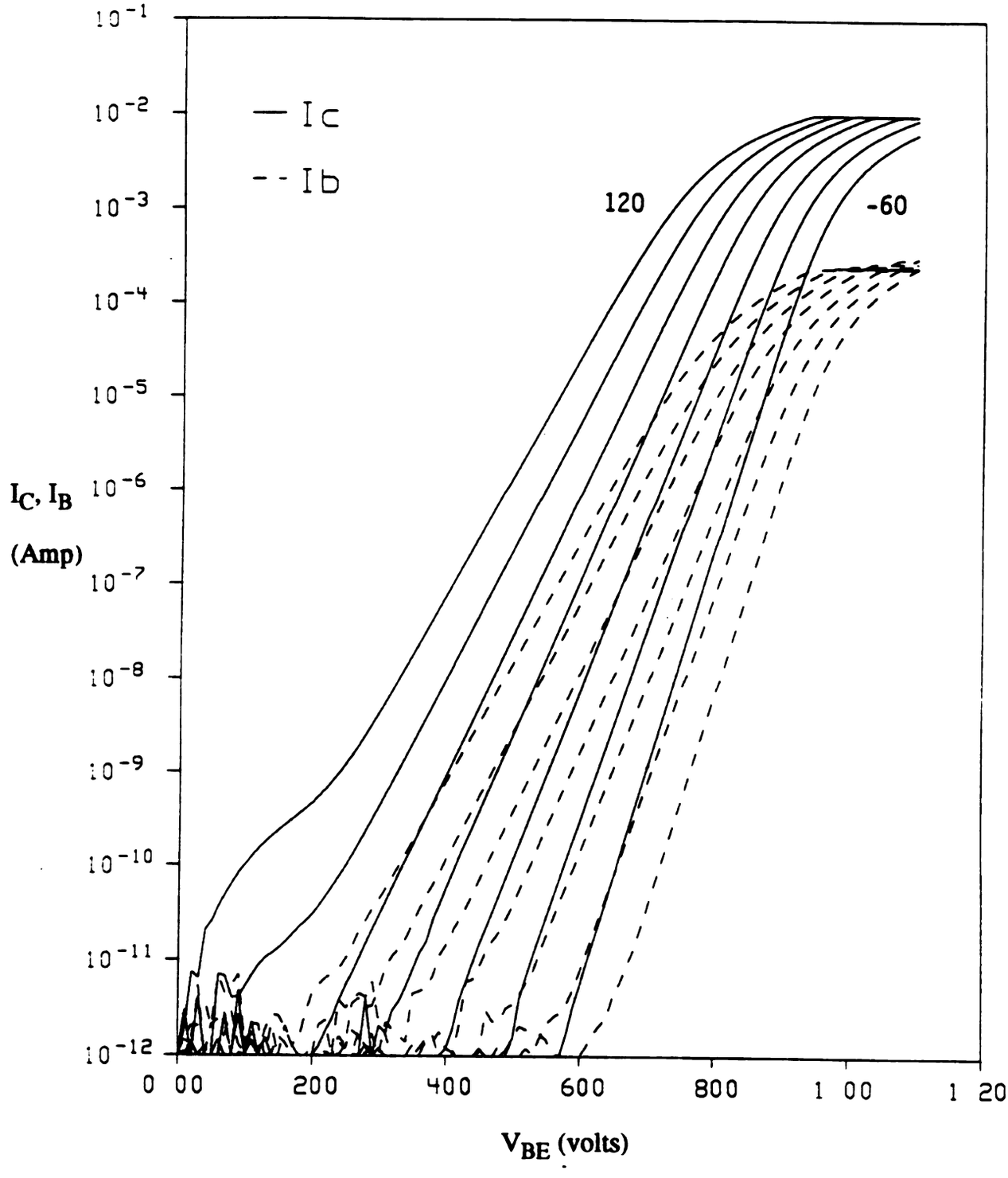

Figure 2.29: Gummel characteristics for a pre-stress TIN3 transistor at temperatures of -60, -30, 0, 30, 60, 90, and 120 C.

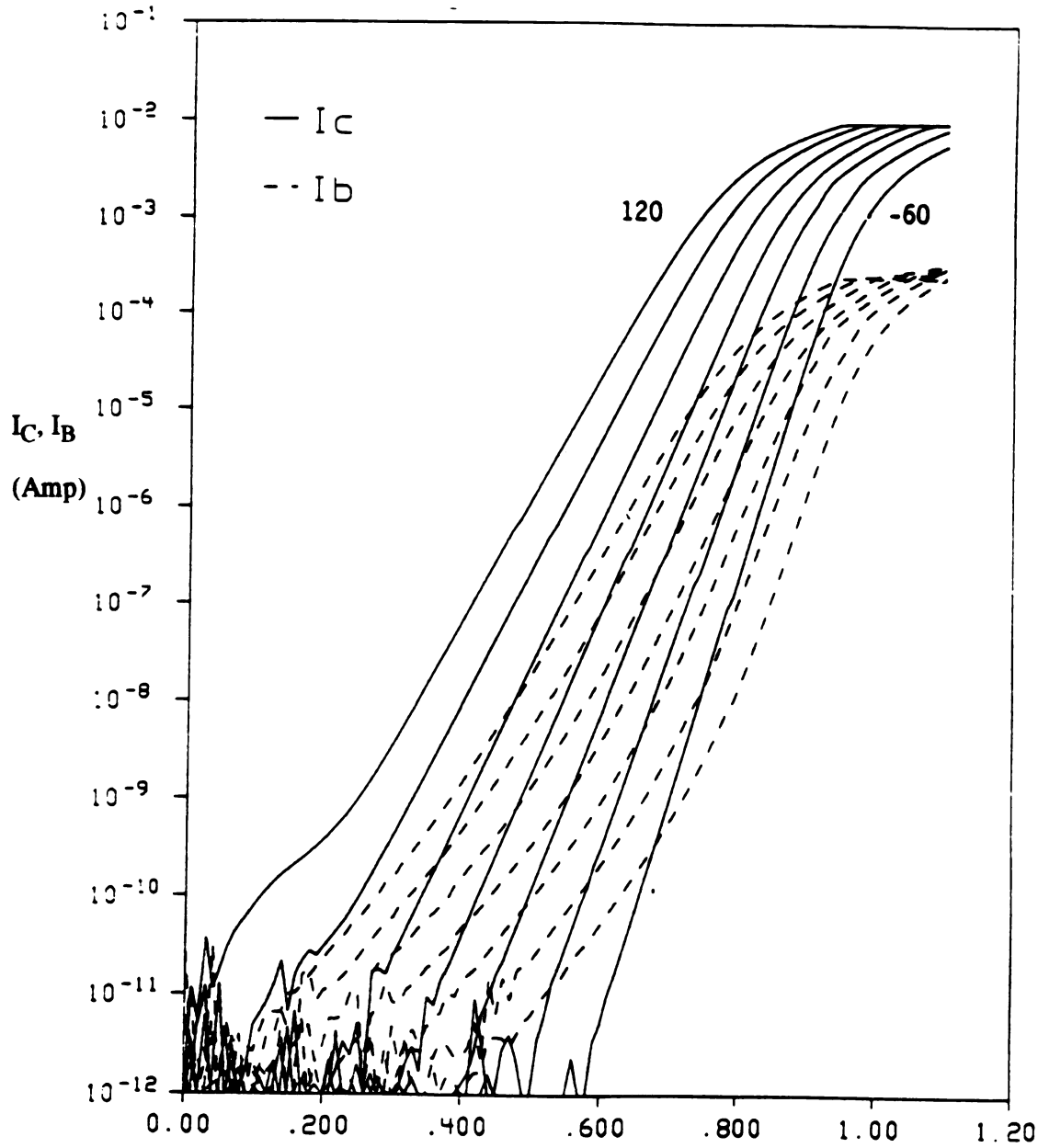

Figure 2.30: Gummel characteristics for a stressed TIN3 transistors at temperatures of -60, -30, 0, 30, 60, 90, and 120 C. The transistor was stressed at -75 C for 1000 hours.

where the hole and electron surface recombination velocities can be expressed as

$$S_{op} = \sigma_p v_{th} N_t \tag{2.2}$$

$$S_{on} = \sigma_n v_{th} N_t \tag{2.3}$$

σ_p, σ_n, v_{th}, and N_t are the hole capture cross section, electron capture cross section, thermal velocity of the carriers, and trap density respectively. Assuming the hole and electron surface recombination velocities are the same, assuming maximum recombination rate throughout the depletion region, i.e., n, p >> n_i, and using $np = n_i^2 e^{qV/kT}$, allows R_S to be simplified giving

$$R_S = \frac{S_o}{2} n_i e^{\frac{qV}{2kT}} \tag{2.4}$$

where $S_o = S_{op} = S_{on}$. The SRH current can be approximated by integrating the recombination rate over the depletion area A giving

$$I_{SRH} \approx qA\frac{S_o}{2} n_i e^{\frac{qV}{2kT}} \tag{2.5}$$

Taking into account the temperature dependence of n_i, the SRH current can be arranged in the following form which shows the temperature dependence and voltage dependence relationship to be

$$I_{SRH} \approx k' \cdot T^{3/2} \cdot \exp\left(-\frac{E_g}{2kT}\right) \cdot \exp\left(\frac{qV}{2kT}\right) \tag{2.6}$$

where k′ is a temperature and voltage independent constant.

The SRH current has a nonideality factor of 2. The larger non-ideality factor at lower temperatures in the experimental data indicates the presence of additional contributions to the base current [38]. The second mechanism possible is the Poole-Frenkel enhanced surface SRH recombination current reported by Woo et. al. [37] and Hackbarth et. al. [10,11]. The carrier emission coefficient is enhanced due to the Pool-Frenkel effect when a high electric field is present. The capture rate for electrons and holes are enhanced by the following

$$C_n = \sigma v_{th} = C_n^o \exp(\frac{q\beta^{1/2}E^{1/2}}{kT}) \tag{2.7}$$

$$C_p = \sigma v_{th} = C_p^o \exp(\frac{q\beta^{1/2}E^{1/2}}{kT}) \tag{2.8}$$

where

$$\beta = \frac{q}{\pi\varepsilon} \tag{2.9}$$

E is electric field, and ε is the high frequency dielectric constant which has a value between free space dielectric constant and the static dielectric constant. Similar to the derivation of (2.6), the Poole-Frenkel recombination current can be expressed as

$$I_{P-F} \approx k_2' \cdot T^{3/2} \cdot \exp\left(\frac{q\beta^{1/2}E^{1/2}}{2kT}\right) \cdot \exp\left(-\frac{E_g}{2kT}\right) \cdot \exp\left(\frac{qV}{2kT}\right) \tag{2.10}$$

where the temperature and voltage dependencies are shown.

The Poole-Frenkel effect can have a nonideality factor greater than two only at very low temperatures (< -150 C) [7,10,11]. Attempts of fitting (2.10) to the degraded characteristics in the temperature range of -60 to 120 C were unsucessful. A third possible degradation current, i.e., the tunneling current, is examined below.

By examining the temperature and voltage dependence of each of these leakage currents, the best fit of the experimental data to the calculated model is obtained by assuming a trap-assisted tunneling current. The forward-bias tunneling model adopted is that developed by Del Alamo and Swanson [39]. This model gives the total forward current as the sum of the trap-assisted tunneling current and the ideal diffusion current. The trap-assisted tunneling current, I_T, is given by

$$I_T = I_{OT} \exp(V/V_T) \tag{2.11}$$

where I_{OT} is the tunneling saturation current and V_T is the characteristic tunneling voltage. The tunneling saturation current has the form

$$I_{OT} = C \exp(-\beta E_G(T)) \tag{2.12}$$

where C and β are constants and $E_G(T)$ is the temperature dependent bandgap.

The fitting of (2.11) to the degraded characteristics produces the plot shown in Figure 2.31 where experimental and calculated base currents are compared for temperatures of -60, -30, 0, 30, 60, 90, and 120 C. The parameters used are β = 146, V_T = 0.053, C = 3×10^{57}, and $E_G(T)$ is [4]

$$E_G(T) = 1.170 - \frac{4.73\times10^{-4}T^2}{T+636} \qquad (2.13)$$

Degradation current due to the excess tunneling mechanism is also reported by Li et. al. [7]. They showed an exponential dependence of the base current on the energy gap and identified the degraded characteristics as the excess tunneling current. So far in the literatures, however, excess tunneling mechanism has not been implemented in a device level simulation program. In addition to its complex quantum mechanical treatment, lack of a detailed knowledge of the surface state energy distribution created by hot electrons makes the device level implementation most difficult. On the other hand, it had been shown that at room temperature the degraded characteristics can be modeled by an increase of surface recombination rate due to an increase in the surface state density created by the hot electrons [1]. The implementation of the surface state creation to model the base current degradation will be used in this work and described in Chapter 3.

2.5 AC Stressing

To investigate the effect of non-DC stressing, transistors were stressed under two conditions:

- V_{BE} switching from -4 to 1 volts for 1950 hours (6 TIN3 devices).
- V_{BE} switching from -4 to 0 volts for 1800 hours (6 TIN3 devices).

In the first group of six transistors, a 1KHz alternating reverse-bias to forward-bias (-4 to +1 V) pulse train was applied to the base-emitter junction with the collector-base junction shorted. The duty cycle was 50% so that the devices were in forward bias for half the time and reverse bias for half the time. In the second group, an alternating

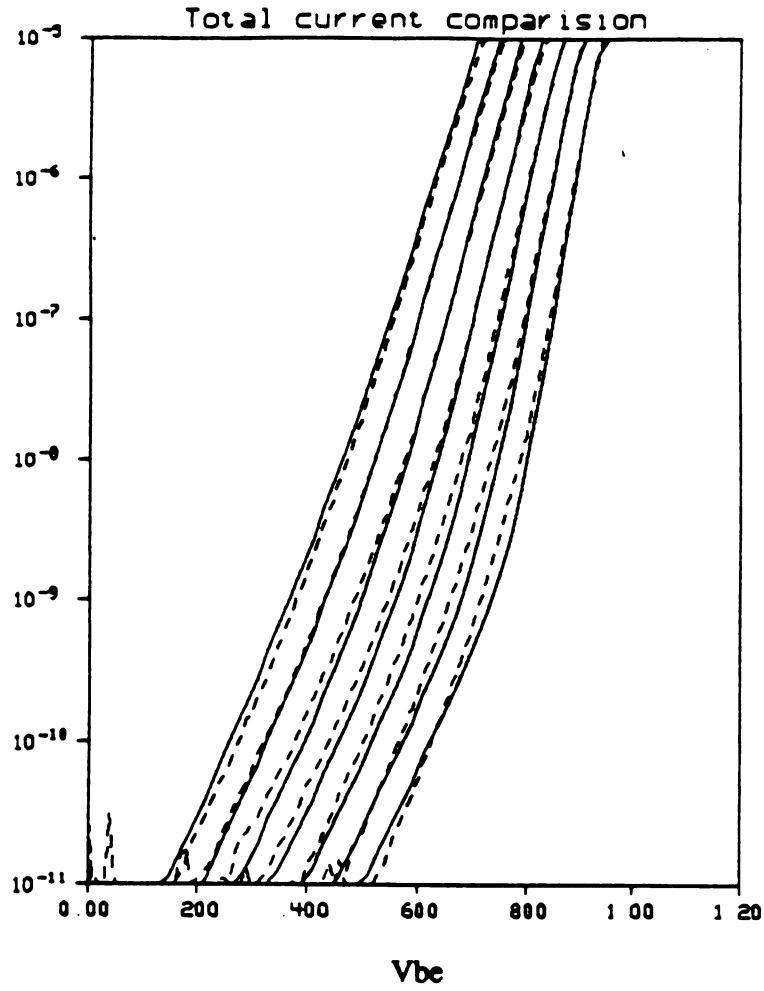

Figure 2.31: Comparison of nonideal tunneling current model (solid lines) to the experimental (dashed lines) base current for temperatures of -60, -30, 0, 30, 60, 90, and 120 C.

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reverse bias-to-zero (-4 to 0 V) pulse train was applied so that the devices were unbiased for half the time and reverse biased for half the time. Self heating of the devices is in both cases not sufficient to cause thermal annealing effects because with a 1 V forward bias on the base-emitter junction, the base current measured is less than 10 mA and the device power dissipation is a maximum of 10 mW. The thermal resistance of a rectangular emitter on a wafer surface is $R_{th} = g / k$ [40,41], where k is the thermal conductivity of the silicon (1.45 W/cm °C at 300 K) and g is the geometrical factor defined as $\frac{\sinh^{-1}(b/c)}{\pi b} + \frac{\sinh^{-1}(c/b)}{\pi c}$ where b and c are the width and length of the emitter. For the emitter dimensions of the transistors used in this study, g is 0.17 μm^{-1} and the thermal resistance is 1.2 C/mW. The resulting temperature rise of 12 C is below the temperature required for thermal annealing effects.

Previous reports on AC stressing have indicated various results. In one report, a significant difference in degradation between stress cycles which included a forward-bias cycle and a stress cycle without forward-bias was reported [8]. In that work, at a stress charge of 6×10^{-5} Columb (about 10 minutes stress time), the 0 to -5 V cycles resulted in a decrease of gain of 14 % whereas the +1 to -5 V cycles resulted in a decrease of gain of 6 %. However, a second study did not report any difference between the two stressing modes for less than one hour of reverse-bias-on time [42]. Our results for AC stressing for up to 1950 hours are shown in Figure 2.32. For the first 100 hours, no apparent distinction is observed between the two stressing conditions. However, with longer stress times, a decrease in degradation rate is observed for the devices receiving forward-bias pulses. After 1800 hours, h_{FE} has degraded to 26% of the original value for reverse bias only stressing, and has degraded to 45% of the original value for stressing which included forward-bias pulses.

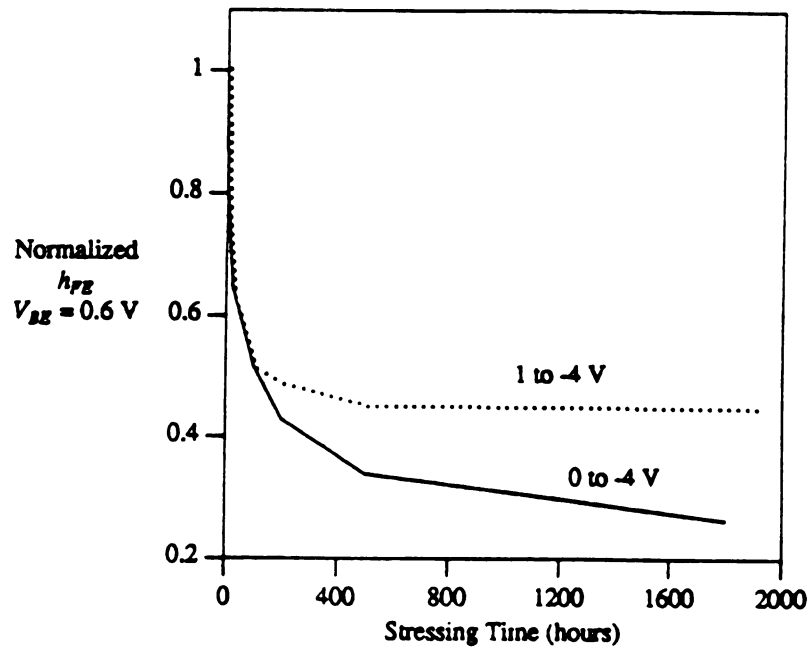


Figure 2.32: AC stressing results for stressing with and without a forward bias cycle.

2.6 Thermal Annealing Experiments

The temperature dependence of the reverse bias degradation as shown earlier in Figure 2.19 can be attributed to two phenomena. One is the temperature dependence of the number of hot electrons. At higher temperatures, a reduced mean-free path between electron scattering events leads to a decrease in the average electron energy. On the other hand, an increase in the stress current (the number of electrons passing through the space charge region) at higher temperatures could still result in an overall larger number of hot electrons. Another phenomena is the simultaneous repassivation of degraded states which occurs significantly more often at the higher ambient temperatures. This repassivation of degraded states was investigated with two annealing experiments.

In the first experiment, transistors degraded at 23C for 500 hours were annealed by placing the transistors in an ambient temperature (50 C to 240 C) without electrical connections. At preselected times the annealing was stopped and the transistor characteristics were measured at 23 C to assess the annealing rate and magnitude. In the second experiment, annealing at 240 C of transistors previously degraded at 240 C for 1000 hours was done in order to compare the annealing characteristics between devices degraded at different temperatures. A detailed description of the two experiments includes:

- degradation at 240 C with V_{BE} = -4 V for 1000 hours, annealing at 240 C for 200 hours (3 TIN3 devices), and
- degradation at 23 C with V_{BE} = -4 V for 500 hours, anneal at 23, 50, 100, 150, 175 and 240 C for up to 500 hours (3 TIN3 devices).

Post degradation gain recovery by annealing at elevated temperatures was observed at temperatures of 150, 175 and 240 C for devices which received previous reverse bias stressing at 4 volts for 500 hours in an ambient temperature of 23C. The degree of post-degradation recovery is highly temperature dependent. Annealing for one hour recovered about 50% of the current gain drop which occurred during the 500 hour

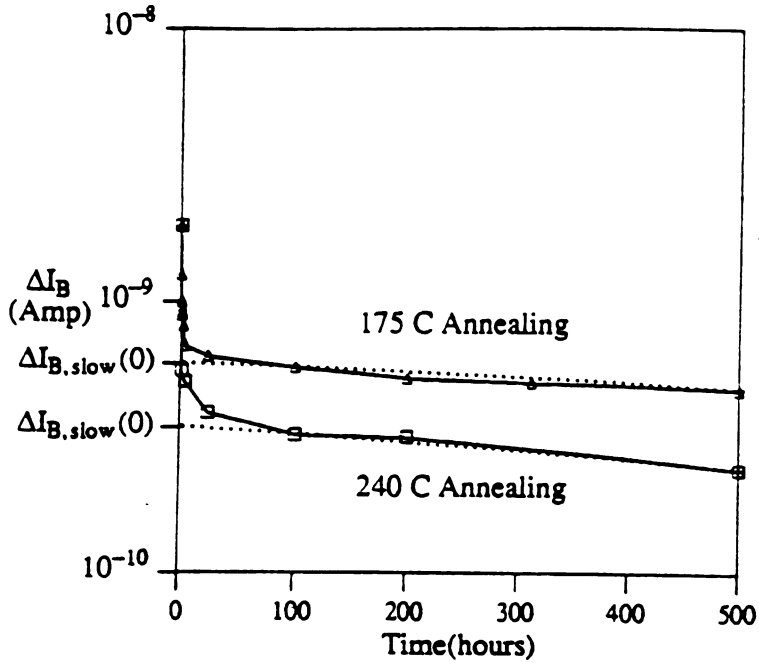


Figure 2.33: Base current change versus annealing time for annealing at 175 and 240 C. Transistors were originally degraded at 23 C for 500 hours.

degradation when the annealing temperature was 240 C. At annealing temperatures of 175 C and 150 C the gain recovery was 30% and 20%, respectively. Figure 2.33 shows the change in base current at V_{BE} = 0.6 V versus annealing time at 175 and 240 C. The zero hour time point on this plot indicates the degradation amount after a 500 hour stress at 23 C. The annealing data shows two distinct regions. For the first few hours of the annealing process the recovery is rapid and for the longer times (greater than 24 hours) the recover continues but at a slower rate. Figure 2.34 shows another annealing experiment in which transistors degraded at 240 C for 1000 hours are annealed at 240 C. The Figure 2.34 result for annealing of 240 C degraded devices shows a smaller recovery for the first few hours of annealing time when compared to the result of Figure 2.33 which shows annealing results for 23 C degraded devices. This difference is attributed to a simultaneous repassivation of a portion of the degradation-produced states during the higher 240 C degradation condition. In particular, the portion of the states which repassivated during the higher temperature degradation are believed to be the same states which show very rapid annealing in Figure 2.33. Once the easily annealed out states have been removed, the longer annealing time data of Figures 2.33 and 2.34 show similar behavior. These two different repassivation rates will be referred to as the slow repassivation and the fast repassivation components. The portion of the total repassivation attributed to the fast and the slow components is temperature dependent. At higher temperatures the fast component is larger as indicated by the larger rapid recovery at 240 C as compared to 175 C in Figure 2.33.

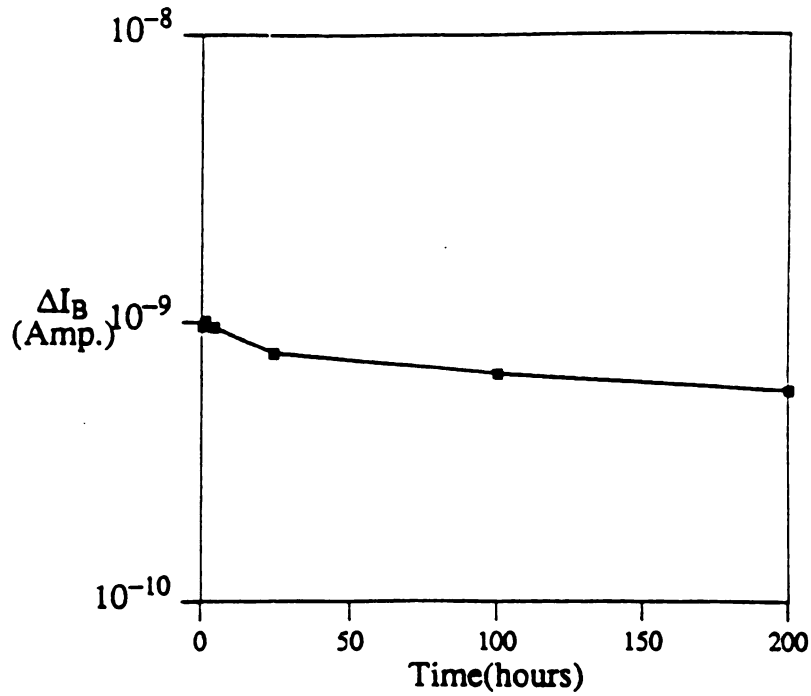


Figure 2.34: Base current change versus annealing time for annealing at 240 C. Transistors were originally degraded at 240 C for 1000 hours.

Chapter 3

Numerical Models of Bipolar Junction Transistors

In this chapter, numerical models are presented and developed to investigate the physical phenomena of bipolar transistor operation including hot electron induced degradation. Section 3.1 introduces the model history and explains the formulation of the Drift-Diffusion Model (DD) model and the Hydrodynamic Transport Model (HTM). Section 3.2 discusses the implementation of numerical solutions for semiconductor devices utilizing these models. Section 3.3 presents physical effects included in the simulation program, e.g., bandgap narrowing, Auger and SRH recombination/generation, and band-to-band tunneling. Section 3.4 develops the model used for extracting the number of hot electrons, namely, the simplified Hydrodynamic Transport Model. The use of the Monte Carlo simulation technique for determination of energy dependent parameters is presented in Section 3.5. Finally, all parameters used in the device simulations of this study are listed in Section 3.6.

3.1 Model History

The behavior of charge carriers can be described by the Boltzmann transport equation (BTE). The unknown to be solved for is the distribution function, $f(\mathbf{r},\mathbf{k},t)$, in the seven dimensional space (the phase space) consisting of spatial coordinate $\mathbf{r}$, momentum coordinate $\mathbf{k}$, and time t. The distribution function determines the carrier density per unit volume of the phase space. The BTE can be written as

$$\frac{\partial f}{\partial t} + \mathbf{v}\cdot\frac{\partial f}{\partial \mathbf{r}} + \frac{\mathbf{F}}{m^*}\cdot\frac{\partial f}{\partial \mathbf{v}} = \left(\frac{\partial f}{\partial t}\right)_c \qquad (3.1)$$

where F represents external forces, m^* is particle effective mass, and $\mathbf{v}$ is group velocity of the carriers. The right hand side includes the randomly-timed scattering events that the

particles experience. The density of particles n(**r**, t) can be determined by integrating the distribution function over all momentum volume as

$$n(\mathbf{r},t) = \int f(\mathbf{k},\mathbf{r},t)d\mathbf{k} \tag{3.2}$$

To directly solve the BTE for a semiconductor device would be formidable, an alternative is to make a series of simplifying assumptions to obtain the semiconductor equations. The final form of these equations may depart significantly from the original form of the BTE. In the following, the DD and HTM models are constructed by obtaining the moment equations for the BTE .

3.1.1 Moment Equations

The moment equations are obtained from (3.1) by multiplying it by various functions of velocity, $\Phi(\mathbf{v})$, and integrating over velocity space. Various $\Phi(\mathbf{v})$ functions include 1, **v**, and **vv**, etc. which give rise to the zero-order, first-order, and second order, etc. moment equations. The procedure is straightforward, though tedious for higher orders. It replaces an equation for the distribution function, f(**r**,**v**,t), by equations that are functions of **r** and t only.

The average over velocity space of an arbitrary function ϕ is defined by

$$\langle\phi\rangle = \frac{1}{n(\mathbf{r},t)}\int \phi(\mathbf{r},\mathbf{v},t)f(\mathbf{r},\mathbf{v},t)d\mathbf{v} \tag{3.3}$$

where n(**r**, t) is defined in (3.2). Hence, multiplying (3.1) by $\Phi(\mathbf{v})$ and integrating over velocity space, the general moment equation may be written as

$$\frac{\partial(n\langle\Phi\rangle)}{\partial t} + \frac{\partial}{\partial \mathbf{r}}\cdot(n\langle \mathbf{v}\Phi\rangle) - \frac{ne}{m^*}\mathbf{E}\cdot\langle\frac{\partial\Phi}{\partial \mathbf{v}}\rangle = \left[\frac{\partial}{\partial t}(n\langle\Phi\rangle)\right]_c \tag{3.4}$$

where **F** is replaced by e**E** where E is the electric field.

Thus the BTE for the distribution function f is replaced by a set of equations containing averaged quantities. By using the following functions of $\Phi(\mathbf{v})$, the first three moment equations are derived to be [43,44]:

Zero-order: $\Phi(\mathbf{v}) = 1$

$$\frac{\partial n}{\partial t} + \nabla \cdot (n\langle \mathbf{v} \rangle) = -R \tag{3.5a}$$

First-order: $\Phi(\mathbf{v}) = m^* \mathbf{v}$

$$\frac{\partial \mathbf{v}}{\partial t} + \mathbf{v} \cdot \nabla \mathbf{v} + \frac{q\mathbf{E}}{m^*} + \frac{1}{m^* n} \nabla (nkT_n) = -\frac{\mathbf{v}}{\tau_p} \tag{3.5b}$$

Second-order: $\Phi(\mathbf{v}) = \frac{1}{2} m^* \mathbf{v}\mathbf{v}$

$$\frac{\partial \xi}{\partial t} + \nabla \cdot \mathbf{S} - \mathbf{J} \cdot \mathbf{E} = -\frac{\xi - \xi_o}{\tau_e} \tag{3.5c}$$

where R is the recombination rate, τ_p and τ_e are momentum and energy relaxation times, T_n is the electron temperature, and $\mathbf{S}$ is the energy flow flux given by

$$\mathbf{S} = -\kappa(T)\frac{dT}{dx} - J\delta(T)\frac{k_B T}{q} \tag{3.6}$$

where $\delta(T)k_B T$ is the average kinetic energy transported per charged carrier arising from the current flow and $\kappa(T)$ is thermal conductivity of the carrier where the Wiedemann-Franz relationship can be used [29,45] to give

$$\frac{\kappa(T)}{\delta(T)} = \left(\frac{k_B}{q}\right)^2 \Delta(T) T \tag{3.7}$$

$\delta(T)$ and $\Delta(T)$ are dimensionless transport coefficients given by [45,46]

$$\delta(T) = \frac{\langle \tau \xi^2 \rangle}{\langle \tau \xi \rangle} \tag{3.8}$$

$$\Delta(T) = \left[\frac{\langle \tau \xi^3 \rangle}{\langle \tau \xi \rangle} - \left(\frac{\langle \tau \xi^2 \rangle}{\langle \tau \xi \rangle} \right)^2 \right] \Big/ (k_B T)^2 \tag{3.9}$$

where ξ is the total carrier energy given by

$$\xi = \tfrac{3}{2} n k_B T_n + \tfrac{1}{2} m^* n \langle \mathbf{v} \rangle^2. \tag{3.10}$$

Equation (3.5a) is the particle conservation equation, Equation (3.5b) is the momentum conservation equation and Equation (3.5c) is the energy conservation equation. Each moment equation introduces the next higher-order velocity moment due to the second term in (3.4). If it is assumed that the distribution function is symmetric about the average velocity in momentum space, as it is for a displaced Maxwellian distribution,

then third and higher order moments of the distribution function vanish [44]. This approximation uses the first three moments of BTE to calculate carrier transport.

3.1.2 Drift-Diffusion Model

The Drift-Diffusion (DD) Model consists of solving the Poisson equation and the continuity equation (3.5a). This model makes a simplified approximation for the momentum equation (3.5b) and neglects the energy conservation equation. The DD model assumes that the carriers are at thermal equilibrium with the lattice and that the carrier temperature gradient is zero. These two assumptions resulted in equation (3.5c) not being used. The simplified approximation for the momentum conservation equation leads to the expression for the current density. This is done by assuming that a quasi-steady-state model is adequate, i.e., $\partial \mathbf{v} / \partial t = 0$, and that $\mathbf{v} \cdot \nabla \mathbf{v}$ is negligible compare to other terms. With these assumptions, the momentum conservation equation (3.5b) becomes

$$\mathbf{v}_n = -\frac{q\tau_p}{m^*}\mathbf{E} - \frac{kT}{m^*}\tau_p \frac{\nabla n}{n} \quad . \tag{3.11}$$

If the mobility and diffusion parameters μ_n, D_n are defined as

$$\mu_n = \frac{q\tau_p}{m^*} \tag{3.12}$$

and

$$D_n = \frac{kT}{q}\mu_n \quad , \tag{3.13}$$

then the expression for the carrier velocity can be written as

$$\mathbf{v}_n = -(\mu_n \mathbf{E} + \frac{D_n}{n}\nabla n) \tag{3.14}$$

and the electron current density becomes

$$\mathbf{J}_n = -qn\mathbf{v}_n = qn\mu_n \mathbf{E} + qD_n \nabla n. \tag{3.15}$$

This representation of carrier transport is referred to as the 'Drift-Diffusion' model and can be extended similarly for holes in semiconductor devices involving both holes

and electrons. The semiconductor equations in the DD model for two carriers are the Poisson equation, the electron continuity equation, and the hole continuity equation. One such Drift-Diffusion simulation program is PISCES-II [24].The equations it solves are

$$\nabla^2\psi = -\frac{q}{\varepsilon}(p - n + N_D - N_A) \tag{3.16a}$$

$$\nabla \cdot \mathbf{J}_n - q \cdot \frac{\partial n}{\partial t} = q \cdot R \tag{3.16b}$$

$$\nabla \cdot \mathbf{J}_p + q \cdot \frac{\partial p}{\partial t} = -q \cdot R \tag{3.16c}$$

where the electron and hole current density $\mathbf{J}_n$ and $\mathbf{J}_p$ can be expressed as

$$\mathbf{J}_n = qn\mu_n\mathbf{E} + qD_n\nabla n \tag{3.16d}$$

and

$$\mathbf{J}_p = qp\mu_p\mathbf{E} - qD_p\nabla p. \tag{3.16e}$$

3.1.3 Hydrodynamic Transport Model

The DD transport model derived above assumes that the carrier velocities are instantaneous functions of the local electric field and that the mobility and diffusion coefficients are functions of local electric field alone. In reality, the carriers do not respond instantaneously to a change of the electric field. A more complete model requires inclusion of the momentum and energy relaxation effects included in the HTM model presented in this section.

The HTM model consists of solving self-consistently the Poisson equation and the first three moment equations, i.e., continuity equation (3.5a), momentum conservation equation (3.5b), and energy conservation equation (3.5c). In a similar manner as the derivation of the velocity equation in the DD Model, the momentum conservation equation leads to the expression for the velocity equation as

$$\mathbf{v}_n = -\mu(T_n)\mathbf{E} - \frac{1}{n}\nabla(D(T_n)n) \tag{3.17}$$

where the mobility and diffusion coefficients are functions of the carrier temperature. They are

$$\mu(T_n) = \frac{q\tau_p(T_n)}{m^*} \tag{3.18}$$

and

$$D(T_n) = \frac{k_B T_n \mu(T_n)}{q} \tag{3.19}$$

Thus for the HTM model, the electron current density is

$$\mathbf{J}_n = qn\mu_n(T_n)\mathbf{E} + q\nabla(nD_n(T_n)) \tag{3.20}$$

For steady state, the energy conservation equation becomes

$$\nabla \cdot \mathbf{S} = \mathbf{J} \cdot \mathbf{E} - \frac{\xi - \xi_o}{\tau_e} \tag{3.21}$$

The energy conservation equation states that the rate of change of energy flow is given by the balance of the Joule heating rate and the energy absorption rate. The energy absorption rate due to carrier phonon collisions and recombination can be expressed in a different way as nC_n+w_nR, where C_n is the energy absorption rate function and w_n is the average electron energy taken to be $\frac{3}{2}kT_n$. Following Cook [28], the expression for the energy absorption rate C_n is

$$C_n(T_n, T_p) = \frac{3}{2}\frac{k_B(T_n - T_o)}{\tau_{wn}} + \frac{3}{2}\frac{k_B(T_n - T_p)}{\tau_{wn}}\frac{p}{p_o} \tag{3.22}$$

where τ_{wn} is the energy relaxation time for electrons and p_O is reference hole density. Finally the energy conservation equation used in this study is

$$\nabla \cdot \mathbf{S}_n = \mathbf{J}_n \cdot \mathbf{E} - nC_n(T_n, T_p) - \frac{3}{2}kT_nR \tag{3.23}$$

The p_o value is 10^{18} cm^{-3} [28].

The derivation for the momentum conservation and the energy conservation equations can be extended to describe the holes. The HTM method for semiconductor devices involving both electrons and holes solves self-consistently the Poisson equation, the continuity equation for electrons, the continuity equation for holes, the energy conservation equation for holes, and the energy conservation equation for electrons. These equations for the steady state case are

$$\nabla^2\psi = \frac{q}{\varepsilon}(p - n + N_D - N_A) \tag{3.24a}$$

$$\nabla \cdot \mathbf{J}_n = qR \tag{3.24b}$$

$$\nabla \cdot \mathbf{J}_p = -qR \tag{3.24c}$$

$$\nabla \cdot \mathbf{S}_n = \mathbf{J}_n \cdot \mathbf{E} - nC_n(T_n, T_p) - \tfrac{3}{2}kT_nR \tag{3.24d}$$

$$\nabla \cdot \mathbf{S}_p = \mathbf{J}_p \cdot \mathbf{E} - pC_p(T_n, T_p) - \tfrac{3}{2}kT_pR \tag{3.24e}$$

where the electron and hole energy fluxes are

$$\mathbf{S}_n = -\kappa(T_n)\nabla T_n - \mathbf{J}_n\delta(T_n)k_BT_n/q \tag{3.24f}$$

$$\mathbf{S}_p = -\kappa(T_p)\nabla T_p + \mathbf{J}_p\delta(T_p)k_BT_p/q \tag{3.24g}$$

and the electron and hole current densities are

$$\mathbf{J}_n = qn\mu_n(T_n)\mathbf{E} + q\nabla(nD_n(T_n)) \tag{3.24h}$$

$$\mathbf{J}_p = qp\mu_p(T_p)\mathbf{E} - q\nabla(pD_p(T_p)) \tag{3.24i}$$

3.2 Numerical Solution Implementation

In this section, the implementation of numerical solutions for the models discussed in the last section will be presented. To solve the semiconductor device model numerically involves discretization of the equations at a set of grid points. Setting up the discretized equations for the grid points constructs a nonlinear matrix problem which typically needs to be solved iteratively. If the iterations result in a convergent solution, the unknowns on the grid points are solved. The details of the scheme are presented below.

3.2.1 Discretization

The numerical solution of the semiconductor equations requires the discretization of these equations (3.24a - 3.24e) for an appropriate grid structure superimposed on the simulated device geometry. For the discussion of the discretization schemes, the notation for the mesh points is shown in Figure 3.1.

The discretization of the Poisson equation is done using a 5-point finite difference approximation which gives

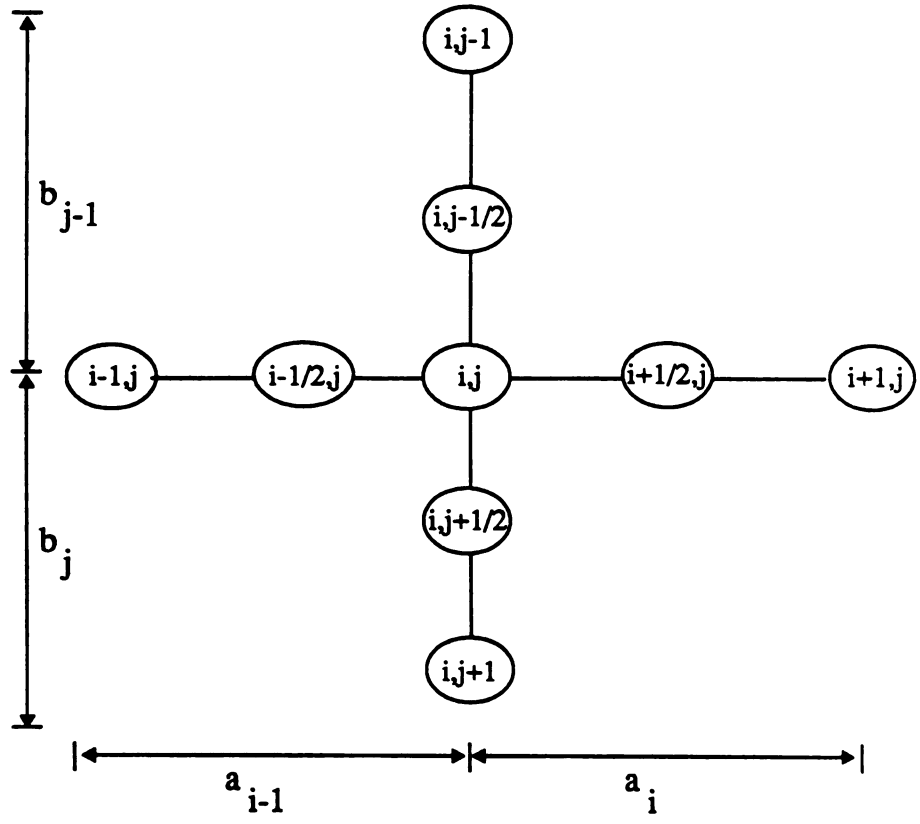


Figure 3.1: The notation for the mesh points used in the discretization of semiconductor equations.

$$\frac{\dfrac{\psi_{i+1,j}-\psi_{i,j}}{a_i}-\dfrac{\psi_{i,j}-\psi_{i-1,j}}{a_{i-1}}}{\dfrac{a_i+a_{i-1}}{2}}+\frac{\dfrac{\psi_{i,j+1}-\psi_{i,j}}{b_j}-\dfrac{\psi_{i,j}-\psi_{i,j-1}}{b_{j-1}}}{\dfrac{b_j+b_{j-1}}{2}}$$

$$=-\frac{q}{\varepsilon}\left(p_{i,j}-n_{i,j}+N_{D_{i,j}}+N_{A_{i,j}}\right) \tag{3.25}$$

For the electron current continuity equation, (3.24b) can be written as

$$\frac{\partial}{\partial x}J_{nx}+\frac{\partial}{\partial y}J_{ny}=qR \tag{3.26}$$

where J_{nx} and J_{ny} are the x and y components of the electron current density vector $\mathbf{J}_n$. Using a 5-point finite difference approximation, the discretized current continuity equation can be expressed as

$$\frac{J_{nx_{i+\frac{1}{2},j}}-J_{nx_{i-\frac{1}{2},j}}}{\dfrac{a_i+a_{i-1}}{2}}+\frac{J_{ny_{i,j+\frac{1}{2}}}-J_{ny_{i,j-\frac{1}{2}}}}{\dfrac{b_j+b_{j-1}}{2}}=qR_{i,j} \tag{3.27}$$

where the electron current densities are evaluated at the mid points shown in Figure 3.1. The hole current continuity equation is discretized as

$$\frac{J_{px_{i+\frac{1}{2},j}}-J_{px_{i-\frac{1}{2},j}}}{\dfrac{a_i+a_{i-1}}{2}}+\frac{J_{py_{i,j+\frac{1}{2}}}-J_{py_{i,j-\frac{1}{2}}}}{\dfrac{b_j+b_{j-1}}{2}}=-qR_{i,j}. \tag{3.28}$$

The derivation of the discretized forms of J_n and J_p follows the work of Tang [46] which is closely related to the Scharfetter-Gummel expression [47] in the DD approximation. The classical Scharfetter-Gummel expression involves the use of the Bernoulli function to include the exponentially varying electron and hole concentration as a function of position and is numerically more accurate. The electron current density has been discretized as

$$J_{nx_{i+\frac{1}{2}}}=\left[-\frac{q(\psi_{i+1}-\psi_i)}{x_{i+1}-x_i}+\frac{k_B(T_{i+1}-T_i)}{x_{i+1}-x_i}\right]\cdot\frac{[n\mu_n(T)]_i B(-\theta)-[n\mu_n(T)]_{i+1}B(\theta)}{\theta} \tag{3.29}$$

where B(x) is the Bernoulli function defined by

$$B(x) = \frac{x}{e^x - 1} \quad . \tag{3.30}$$

θ represents

$$\theta = -(\alpha_m + 1)\ln(T_{i+1} / T_i) \tag{3.31}$$

and α_m is given by

$$\alpha_m = -\frac{q(\psi_{i+1} - \psi_i)}{k_B(T_{i+1} - T_i)} \quad . \tag{3.32}$$

Similarly, the hole current density can be expressed as

$$J_{px_{i+\frac{1}{2}}} = \left[-\frac{q(\psi_{i+1} - \psi_i)}{x_{i+1} - x_i} - \frac{k_B(T_{i+1} - T_i)}{x_{i+1} - x_i} \right] \cdot \frac{[p\mu_p(T)]_i B(-\theta') - [p\mu_p(T)]_{i+1} B(\theta')}{\theta'} \tag{3.33}$$

where

$$\theta' = -(\alpha'_m + 1)\ln(T_{i+1} / T_i) \tag{3.34}$$

and

$$\alpha'_m = \frac{q(\psi_{i+1} - \psi_i)}{k_B(T_{i+1} - T_i)} \quad . \tag{3.35}$$

The detail derivation for the discretization of the electron and hole current density is documented in Appendix A.

For the discretization of the energy conservation equation, the $\nabla \cdot \mathbf{S}$ term is discretized similar to the $\nabla \cdot \mathbf{J}$ term of the continuity equation. The $\mathbf{J} \cdot \mathbf{E}$ term is taken as the average between the mid points as

$$\mathbf{J}_n \cdot \mathbf{E} = J_{nx}E_x + J_{ny}E_y \tag{3.36}$$

where

$$\begin{aligned} J_{nx}E_x &= \frac{1}{2}\left(J_{n_{i+\frac{1}{2},j}} E_{i+\frac{1}{2},j} + J_{n_{i-\frac{1}{2},j}} E_{i-\frac{1}{2},j} \right) \\ &= -\frac{1}{2} J_{n_{i+\frac{1}{2},j}} \frac{\psi_{i+1,j} - \psi_{i,j}}{a_i} - \frac{1}{2} J_{n_{i-\frac{1}{2},j}} \frac{\psi_{i,j} - \psi_{i-1,j}}{a_{i-1}} \end{aligned} \tag{3.37}$$

The energy conservation equation for electrons is discretized as

$$\frac{S_{n_{i-\frac{1}{2},j}} - S_{n_{i-\frac{1}{2},j}}}{\frac{1}{2}(a_i + a_{i-1})} + \frac{S_{n_{i,j-\frac{1}{2}}} - S_{n_{i,j-\frac{1}{2}}}}{\frac{1}{2}(b_j + b_{j-1})} =$$

$$-\frac{1}{2}J_{n_{i+\frac{1}{2},j}}\frac{\psi_{i+1,j} - \psi_{i,j}}{a_i} - \frac{1}{2}J_{n_{i-\frac{1}{2},j}}\frac{\psi_{i,j} - \psi_{i-1,j}}{a_{i-1}}$$

$$-\frac{1}{2}J_{n_{i,j+\frac{1}{2}}}\frac{\psi_{i,j+1} - \psi_{i,j}}{b_j} - \frac{1}{2}J_{n_{i,j-\frac{1}{2}}}\frac{\psi_{i,j} - \psi_{i,j-1}}{b_{j-1}}$$

$$-n_{i,j}C_{i,j} - \frac{3}{2}kT_{n_{i,j}}R_{i,j} \qquad (3.38)$$

The energy conservation equation of holes is similar to that of the electrons and is simply the substitute of p for n in (3.38). The details of the discretization of electron and hole energy flux densities S_n and S_p is shown in Appendix A.

3.2.2 Box Integration Method

The general form of the semiconductor equation, e.g., the Poisson equation, the continuity equation, or the energy conservation equation, can be expressed as

$$\nabla \cdot \mathbf{F}(u, \dot{u}) = c(u, \dot{u}) \qquad (3.39)$$

where **F** represents the electric flux density **D** for the Poisson equation, the current flux density **J** for the continuity equation, and the energy flux density **S** for the energy conservation equation. u represents the unknown state variables which are being solved, e.g., ψ, n, p, T_n, and T_p. The divergence theorem states that for a generalized function **F**, the volume integral can be transformed into the surface integral by the relationship

$$\int_v \nabla \cdot \mathbf{F} dv = \int_s \mathbf{F} \cdot \mathbf{n} dA \qquad (3.40)$$

where **n** is the outgoing unit vector normal to surface dA. Applying (3.40) to (3.39) gives

$$\int_s \mathbf{F} \cdot \mathbf{n} dA = \int_v c dv \qquad (3.41)$$

For the two dimensional case, (3.41) becomes

$$\int_l \mathbf{F} \cdot \mathbf{n} d\ell = \int_A c dx dy \qquad (3.42)$$

where **n** is the outgoing unit vector normal to the perimeter dl of the rectangular around the grid point as shown in Figure 3.2. By taking the line integral of the left hand side and assuming the value c is constant in the area dxdy, (3.42) becomes

$$(F_{35} - F_{13})dy + (F_{34} - F_{23})dx = c(dx)(dy) \tag{3.43}$$

where F_{13} is the physical quantity from point 1 to 3, F_{35} is the physical quantity from point 3 to 5, etc. The box integration method numerically solves for the semiconductor equations of the form of (3.43), i.e., for the Poisson equation,

$$(D_{35} - D_{13})dy + (D_{34} - D_{23})dx = q(p - n + N_D - N_A)(dx)(dy) \tag{3.44}$$

for the continuity equation,

$$(J_{35} - J_{13})dy + (J_{34} - J_{23})dx = qR(dx)(dy) \tag{3.45}$$

and for the energy conservation equation,

$$(S_{35} - S_{13})dy + (S_{34} - S_{23})dx = (\mathbf{J}\cdot\mathbf{E} - nC_n - \frac{3}{2}kTR)(dx)(dy) \tag{3.46}$$

The box-integration method, which can be understood as a finite-difference on a rectangular elements, has been proven to work satisfactorily in semiconductor device applications [48]. Similar as above, the box integration method can be applied to triangular elements [24]. This research uses the box integration method on a rectangular mesh structure to set up the matrix elements for iterative solutions. The box integration method was chosen to facilitate the use of a terminating line mesh structure as discussed in the next section.

3.2.3 Grid Structure

For semiconductor device simulations, three types of grid structure are commonly used: (1) non-uniform rectangular mesh, (2) triangular mesh, and (3) terminating line rectangular mesh structures as shown in Figure 3.3. The non-uniform rectangular mesh is easiest to implement and its numerical properties are well known. The disadvantage of the non-uniform rectangular mesh is that it would take the most mesh points among the three grid structures. The triangular mesh structure has a similar form to the

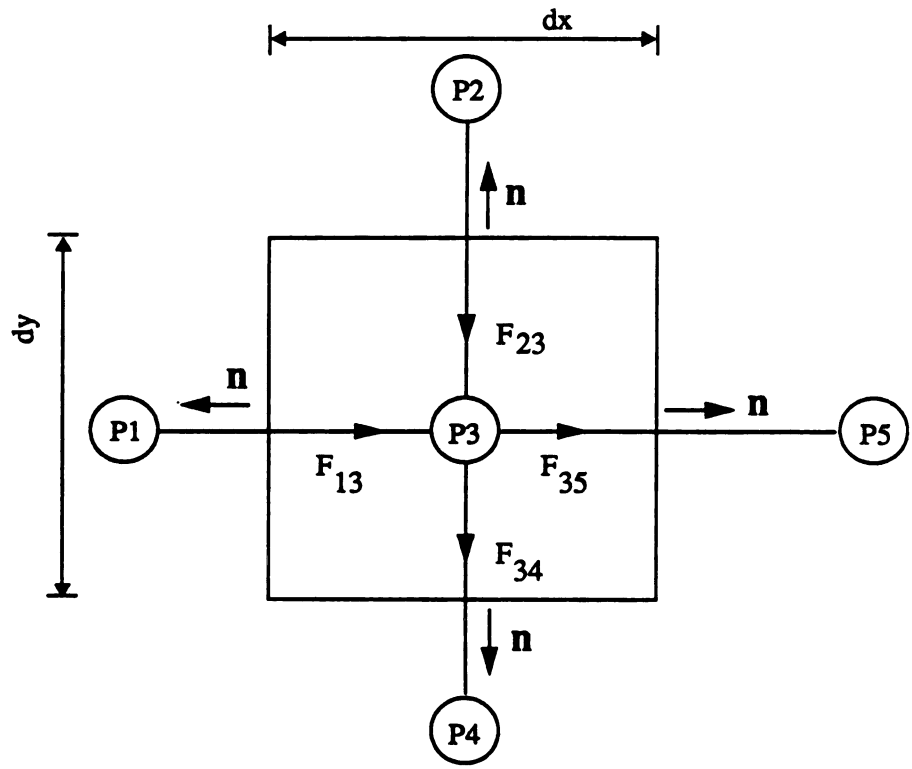
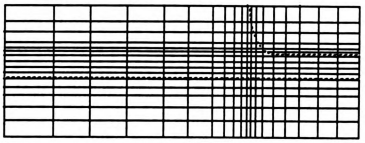
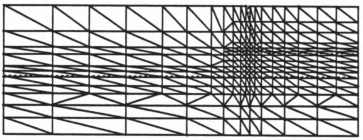


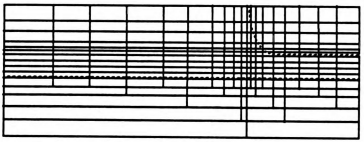
Figure 3.2:The physical quantities and the unit normal vectors for the box integration method.



(a)



(b)



(c)

Figure 3.3: Three commonly used grid structure: (a) non-uniform rectangular mesh, (b) triangular mesh, and (3) terminating line mesh. Dashed lines indicate pn junctions.

finite-element method and is more flexible when applied to irregular boundary conditions but is more difficult to implement. The third kind of mesh structure is the terminating line mesh structure which improves the non-uniform rectangular mesh structure by (1) not extending the mesh lines to where physical changes are slow and by (2) reducing the number of mesh points. The structure of the grids employed by this work is the terminating line mesh structure [49].

The mesh and point assigning scheme for an example grid is illustrated in Figure 3.4. The use of the terminating line mesh structure requires that a "book-keeping" be done to record and use the grid. For each point, a list of its right and left neighbors are kept. The number of the first point in each column is stored in an array NLOC. To locate a point from its column and row number, the following equation can be used

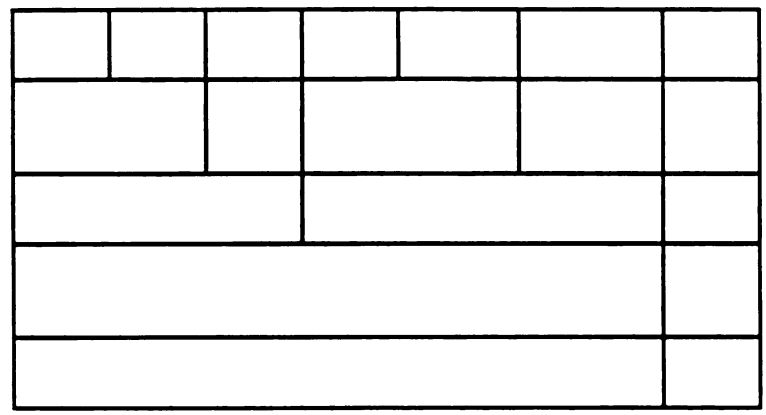
$$N = NLOC(i) + j \tag{3.47}$$

where i and j are the column and row number.

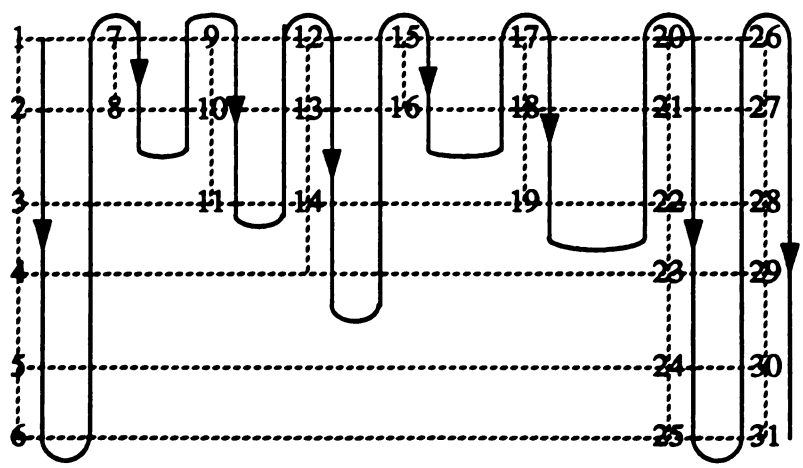
The location for each column and row are kept in two arrays, XLOC and YLOC. The position of each grid point can be identified from its row and column number by x = XLOC(i) and y = YLOC(j). Layout of the mesh structure as specified in the user's input file includes the location of a specific mesh line and the distance ratio between the mesh lines. The mesh lines in the y direction can be specified to be shorter than the device depth, giving rise to a terminated mesh line. If, in the y direction, all mesh lines are specified to be equal to the device depth, all lines are nonterminated and the mesh structure reduces to the nonuniform rectangular mesh structure. The details for describing the layout of a mesh in the input file are explained in Appendix B.

3.2.4 Numerical Solution

The solution of the discretized semiconductor equations on a grid of N nodes involves a total of 5N unknowns for the HTM since at each point the unknowns are ψ, n, p, T_n, and T_p. The system of 5N discretized equations including the Poisson equation, the



(a)



(b)

Figure 3.4: (a) An example mesh and (b) its point assigning scheme for terminating line mesh.

continuity equations for electrons and holes, and the energy conservation equations for electrons and holes are

$$F(\psi,n,p,T_n,T_p)=\begin{bmatrix} F_\psi(\psi,n,p,T_n,T_p) \\ F_{cn}(\psi,n,p,T_n,T_p) \\ F_{cp}(\psi,n,p,T_n,T_p) \\ F_{tn}(\psi,n,p,T_n,T_p) \\ F_{tp}(\psi,n,p,T_n,T_p) \end{bmatrix}=0 \tag{3.48}$$

where F_ψ denotes the system of the N Poisson equations, F_{cn} and F_{cp} denote the system of the 2N continuity equations for electrons and holes, and F_{tn} and F_{tp} denote the system of the 2N energy conservation equations for electrons and holes. Two principle methods of solving (3.48) are the Newton method and the decoupled method or Gummel method.

The Newton's method linearizes the system of partial differential equations and, by starting from an initial guess, the solution of the nonlinear equations is obtained by iterating the matrix equation

$$\begin{bmatrix} \frac{\partial F_\psi}{\partial\psi} & \frac{\partial F_\psi}{\partial n} & \frac{\partial F_\psi}{\partial p} & \frac{\partial F_\psi}{\partial T_n} & \frac{\partial F_\psi}{\partial T_p} \\ \frac{\partial F_{cn}}{\partial\psi} & \frac{\partial F_{cn}}{\partial n} & \frac{\partial F_{cn}}{\partial p} & \frac{\partial F_{cn}}{\partial T_n} & \frac{\partial F_{cn}}{\partial T_p} \\ \frac{\partial F_{cp}}{\partial\psi} & \frac{\partial F_{cp}}{\partial n} & \frac{\partial F_{cp}}{\partial p} & \frac{\partial F_{cp}}{\partial T_n} & \frac{\partial F_{cp}}{\partial T_p} \\ \frac{\partial F_{tn}}{\partial\psi} & \frac{\partial F_{tn}}{\partial n} & \frac{\partial F_{tn}}{\partial p} & \frac{\partial F_{tn}}{\partial T_n} & \frac{\partial F_{tn}}{\partial T_p} \\ \frac{\partial F_{tp}}{\partial\psi} & \frac{\partial F_{tp}}{\partial n} & \frac{\partial F_{tp}}{\partial p} & \frac{\partial F_{tp}}{\partial T_n} & \frac{\partial F_{tp}}{\partial T_p} \end{bmatrix}^k \begin{bmatrix} \Delta\psi^k \\ \Delta n^k \\ \Delta p^k \\ \Delta T_n^k \\ \Delta T_p^k \end{bmatrix}$$

$$= -\begin{bmatrix} F_\psi(\psi^k,n^k,p^k,T_n^k,T_p^k) \\ F_{cn}(\psi^k,n^k,p^k,T_n^k,T_p^k) \\ F_{cp}(\psi^k,n^k,p^k,T_n^k,T_p^k) \\ F_{tn}(\psi^k,n^k,p^k,T_n^k,T_p^k) \\ F_{tp}(\psi^k,n^k,p^k,T_n^k,T_p^k) \end{bmatrix} \tag{3.49}$$

where k denotes the iteration count. The correction vector for the k-th iteration is given by

$$\Delta\psi^k = \psi^{k+1} - \psi^k \tag{3.50a}$$

$$\Delta n^k = n^{k+1} - n^k \tag{3.50b}$$

$$\Delta p^k = p^{k+1} - p^k \tag{3.50c}$$

$$\Delta T_n^k = T_n^{k+1} - T_n^k \tag{3.50d}$$

$$\Delta T_p^k = T_p^{k+1} - T_p^k \tag{3.50e}$$

The Gummel method decouples the equations such that each system of equations can be treated independently for each iteration cycle. Each system of equations are solved sequentially and the variables are updated along each solutions. When all the updates are less than a set of criterion for an iteration, the convergence is reached. The Gummel method can be written as

$$\left[\frac{\partial F_\psi(\psi^k, n^k, p^k, T_n^k, T_p^k)}{\partial\psi}\right]\cdot\Delta\psi^k = -F_\psi(\psi^k, n^k, p^k, T_n^k, T_p^k) \tag{3.51a}$$

$$\left[\frac{\partial F_{cn}(\psi^{k+1}, n^k, p^k, T_n^k, T_p^k)}{\partial n}\right]\cdot\Delta n^k = -F_{cn}(\psi^{k+1}, n^k, p^k, T_n^k, T_p^k) \tag{3.51b}$$

$$\left[\frac{\partial F_{cp}(\psi^{k+1}, n^{k+1}, p^k, T_n^k, T_p^k)}{\partial p}\right]\cdot\Delta p^k = -F_{cp}(\psi^{k+1}, n^{k+1}, p^k, T_n^k, T_p^k) \tag{3.51c}$$

$$\left[\frac{\partial F_{tn}(\psi^{k+1}, n^{k+1}, p^{k+1}, T_n^k, T_p^k)}{\partial T_n}\right]\cdot\Delta T_n^k = -F_{tn}(\psi^{k+1}, n^{k+1}, p^{k+1}, T_n^k, T_p^k) \tag{3.51d}$$

$$\left[\frac{\partial F_{tp}(\psi^{k+1}, n^{k+1}, p^{k+1}, T_n^{k+1}, T_p^k)}{\partial T_p}\right]\cdot\Delta T_p^k = -F_{tp}(\psi^{k+1}, n^{k+1}, p^{k+1}, T_n^{k+1}, T_p^k) \tag{3.51e}$$

where (3.51a) to (3.51e) are solved sequentially. At each stage only one semiconductor equation is being linearized and solved by the Newton method, so the matrix being solved has N rows by N columns regardless of the number of coupled equations being solved. Whereas in the full Newton's method, all of the coupling between variables are taken into account and the matrix size will be 5N× 5N.

Because of the tight-coupling, the full Newton's method requires a smaller number of iterations for convergence, however, since the matrix size is larger, it takes more time to solve for each iteration. The Gummel method usually takes considerably more iterations to reach the convergence while the time for each iterations is often less than the Full Newton method because of the smaller matrix size. Depending on the numerical technique and the exact device structure to be solved, the least time for a solution to converge could be achieved either by a full Newton method or a Gummel method [24]. However, when the limiting factor is the load of the computer memory, the Gummel method is preferred because of the smaller matrix size.

Another technique to further alleviate the memory load and the computation time required is the sparse matrix solution technique which has the following general features [50]:

1. Only nonzero elements with necessary indexing information are stored.
2. Operations involving zeros are not performed.

The procedure of the sparse matrix solution Ax=B typically involves the following steps:

(1) Symbolic LU Decomposition: First, the nonzero elements of A are setup and the location of the nonzero elements are recorded. Second, a symbolic LU decomposition is performed which does not actually perform a numerical value computation but merely determines the new nonzeros (fill-in) that will appear after an actual LU decomposition. The locations of these fill-ins are than used to adjust the new data structure to include the location of the fill-ins.

(2) Numerical LU Decomposition: This LU decomposition performs the numerical calculations. The scheme used for LU decomposition is the Dolittle scheme [50]. After the LU decomposition, the A matrix is now decompose into a L matrix and a U matrix which is expressed as

$$A = LU \tag{3.52}$$

where the L and U are upper and lower triangular matrices respectively.

(3) Solving for y from Ly = B followed by x from Ux = y gives the x solution vector.

Special care is taken throughout the steps not to stored any zero elements and to index the nonzero elements such that only nonzero element operations are involved.

3.2.5 Boundary Conditions

The set of semiconductor equations are solved on the device grid points by the methods described above. The grid point values located on the device electrodes are predetermined by the boundary conditions. The boundary conditions used for the simulation program are ohmic contact conditions which assume that the contact is perfectly conducting. The potential on the electrode grid points are predetermined to be

$$\psi = \psi_b + \psi_a \tag{3.53}$$

where ψ_b represents the built-in potential between the electrodes, and ψ_a is the applied bias to the electrode. The carrier concentration is determined by assuming thermal equilibrium and vanishing space charge at the ohmic contacts,i.e.,

$$n \cdot p - n_i^2 = 0 \tag{3.54}$$

and

$$p - n + N_D - N_A = 0 \tag{3.55}$$

Finally for the HTM device simulations, carriers at the electrode are assume to be in thermal equilibrium with the contacts

$$T_n = T_p = T_o \tag{3.56}$$

where T_o is the ambient temperature of the device.

The boundary conditions along non-electrode boundaries are

$$\frac{\partial \psi}{\partial \mathbf{n}} = 0$$
$$\frac{\partial n}{\partial \mathbf{n}} = 0$$
$$\frac{\partial p}{\partial \mathbf{n}} = 0$$
$$\frac{\partial T_n}{\partial \mathbf{n}} = 0 \qquad (3.57)$$
$$\frac{\partial T_p}{\partial \mathbf{n}} = 0$$

Throughout the simulation, it is assumed that physical quantities have no variation in the direction normal to the domain boundary, thus, no energy flux or current can flow through non-electrode boundaries.

3.3 Physical Effects

3.3.1 Bandgap Narrowing and Auger/SRH Recombination

The recombination term implemented in this study includes both Schockley-Reed-Hall and Auger recombination, i.e.,

$$R = R_{SRH} + R_{Aug} \qquad (3.58a)$$

where

$$R_{SRH} = \frac{np - n_{ie}^2}{\tau_p\left[n + n_{ie}\exp\left(\frac{E_t - E_i}{k_B T}\right)\right] + \tau_n\left[p + n_{ie}\exp\left(\frac{E_i - E_t}{k_B T}\right)\right]} \qquad (3.58b)$$

and

$$R_{Aug} = c_n(pn^2 - nn_{ie}^2) + c_p(np^2 - pn_{ie}^2) \qquad (3.58c)$$

In the above, E_i is the intrinsic Fermi energy, E_t is the trap energy level, τ_n and τ_p are electron and hole lifetimes, c_n and c_p are Auger coefficients, and n_{ie} is the effective intrinsic concentration. The electron and hole concentrations using a Fermi-Dirac distribution and a parabolic distribution of the density of states are given by

$$n = N_C F_{1/2}\left\{\frac{1}{kT}[E_{Fn} - E_C]\right\} \qquad (3.59a)$$

$$p = N_V F_{1/2}\left\{\frac{1}{kT}\left[E_V - E_{Fp}\right]\right\} \tag{3.59b}$$

where N_C and N_V are the effective density of states in the conduction and valence bands, E_C and E_V are the conduction and valence band energies, E_{Fn} and E_{Fp} are the electron and hole Fermi energies, and $F_{1/2}$ is the Fermi-Dirac integral. For the range of operation of most semiconductor devices, Boltzmann statistics is a good approximation to the Fermi-Dirac distribution and n and p can be simplified to

$$n = N_C \exp\left\{\frac{1}{kT}\left[E_{Fn} - E_C\right]\right\} = n_{ie} \exp\left[\frac{q}{kT}(\psi - \phi_n)\right] \tag{3.60a}$$

$$p = N_V \exp\left\{\frac{1}{kT}\left[E_V - E_{Fp}\right]\right\} = n_{ie} \exp\left[\frac{q}{kT}(\phi_p - \psi)\right] \tag{3.60b}$$

where n_{ie} can be expressed as the following by neglecting the band gap narrowing effects:

$$n_{ie}(T) = \sqrt{N_C N_V}\exp(-E_g / 2kT) \tag{3.61}$$

In heavily doped semiconductor devices where the band gap narrowing effect can not be ignored, n_{ie} is modeled as

$$n_{ie}(x,y) = n_i \exp\left\{\frac{9\times 10^{-3} q}{2k_B T}\left[\ln\frac{N(x,y)}{10^{17}} + \sqrt{\left[\ln\frac{N(x,y)}{10^{17}}\right]^2 + \frac{1}{2}}\right]\right\} \tag{3.62}$$

where N(x,y) is the local (total) impurity concentration. The band gap narrowing effect also requires adjustment of the electric field terms in (3.24) as the following

$$E_n = -\nabla\left[\psi + \frac{kT}{q}\ln n_{ie}\right] \tag{3.63a}$$

$$E_p = -\nabla\left[\psi - \frac{kT}{q}\ln n_{ie}\right] \tag{3.63b}$$

Energy gap and density of states are temperature dependent, their temperature dependence can be expressed as

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \tag{3.64}$$

$$N_C(T) = \left(\frac{T}{300}\right)^{3/2} N_C(300) \tag{3.65a}$$

$$N_V(T) = \left(\frac{T}{300}\right)^{3/2} N_V(300) \tag{3.65b}$$

By assuming Boltzmann statistics, the diffusivities and mobilities can be related by

$$D_n = \frac{kT}{q}\mu_n \tag{3.66a}$$

$$D_p = \frac{kT}{q}\mu_p \tag{3.66b}$$

The low field mobility model adopted by this study included the ionized impurity scattering in silicon and is temperature dependent as [54]

$$\mu_n = 88\frac{cm^2}{Vs}\left(\frac{T}{300K}\right)^{-0.57} + \frac{1252\frac{cm^2}{Vs}\left(\frac{T}{300K}\right)^{-2.33}}{1+\frac{CI}{1.432\cdot 10^{17}cm^{-3}\left(\frac{T}{300K}\right)^{2.546}}} \tag{3.67a}$$

for electrons and

$$\mu_p = 54.3\frac{cm^2}{Vs}\left(\frac{T}{300K}\right)^{-0.57} + \frac{407\frac{cm^2}{Vs}\left(\frac{T}{300K}\right)^{-2.33}}{1+\frac{CI}{2.67\cdot 10^{17}cm^{-3}\left(\frac{T}{300K}\right)^{2.546}}} \tag{3.67b}$$

for holes. T is the ambient temperature and CI is the sum of all ionized impurity species times the magnitude of their charge state. In this work, CI is assumed to be the total impurity concentration N(x,y). Equations (3.67) are supposed to be accurate to within a maximum error of 13% in a temperature range of 250 to 500 K for a total ionized impurity concentration range of 10^{13} to 10^{15} cm^{-3} [54]. (3.67) is the mobility model suitable for DD simulations, for the HTM model, however, an energy dependent mobility model is required. The use of Monte Carlo simulations to extract the energy dependent mobility model will be discussed in Section 3.5.

3.3.2 Band-to-Band Tunneling Mechanism

The emitter and extrinsic base regions are close enough together in advanced technology transistors that when the emitter-base junction is reverse biased, the stress current is mainly a band-to-band tunneling current [33]. In most device simulation programs, the tunneling mechanism is not included due to the complexities of treating the quantum mechanical effects. The reverse bias stressing condition, therefore, can not be solved in these device simulators. Recent work by Endoh et. al. [52] has included the calculation of tunneling current for MOSFET structures. In this study, Endoh's work has been extended to BJT device level simulations and applied to the experimentally stressed BJT structure.

When transistors are operated at large enough base-emitter reverse bias conditions the electrons in the valence band on the base side can tunnel to the conduction band on the emitter side as shown in Figure 3.5. Following Kane's work, the band-to-band tunneling rate can be described as a function of electric field as [51-53]

$$P(E) = \frac{q^2 m^{1/2} E^2}{2\pi\hbar^2 E_{gap}^{1/2}} \exp\left(-\frac{\pi m^{1/2} E_{gap}^{3/2}}{2\hbar q E}\right) \tag{3.68}$$

where P is the tunneling rate per second per cubic centimeter, E is the electric field, E_{gap} is the semiconductor band gap, and m is the reduced mass defined as

$$m = \frac{m_c^* \cdot m_v^*}{m_c^* + m_v^*} \tag{3.69}$$

where m_c^* and m_v^* are the effective mass for electrons in conduction band and valence band respectively. Note that, (3.68) is numerically a factor of 9 times larger than the original expression of Kane's as suggested by Chakraborty et. al. [53].

Although this model is valid only when the electric field is uniform along the tunneling path, the local average electric field over the distance of the tunneling path is used for the tunneling rate calculation. Endoh et. al. [52] has shown this approximation

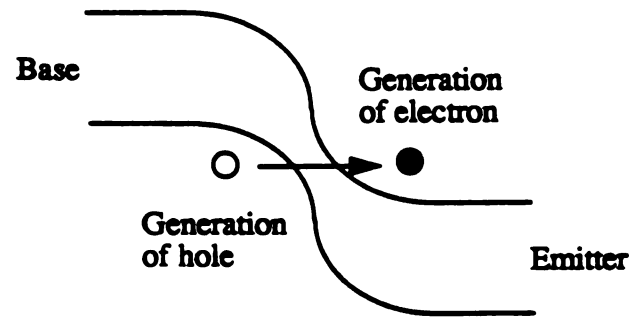


Figure 3.5: The band-to-band tunneling mechanism showing the electron tunneling from the valence band of the base to the conduction band of the emitter.

to be valid even when the electric field in the silicon is strong enough for band-to-band tunneling.

The band-to-band tunneling has been implemented into the device simulation program by treating the tunneling process as the generation of holes on the base side and a simultaneously generation of electrons on the emitter side at values given by

$$G^{e}_{tun} = P(E) \qquad \text{(tunneling end point)} \qquad (3.70a)$$

$$G^{h}_{tun} = P(E) \qquad \text{(tunneling initiation point)} \qquad (3.70b)$$

where G^{e}_{tun} and G^{h}_{tun} are the generation terms to be included in the electron and hole continuity equations for the device simulation program. The device simulation program calculates tunneling (generation) at each point after each potential solution. By solving current continuity equations along with appropriate generation terms the tunneling current mechanism can be accounted for satisfactorily.

The tunneling current calculation is implemented by considering each grid point in the simulation to be the beginning location for a tunneling event. All other grid points in an extended neighborhood are then checked as possible termination locations for the tunneling process. The neighboring point having the largest tunneling rate is chosen as the tunneling termination point. The tunneling termination point must be spatially close enough to the tunneling beginning point and at a potential that permits tunneling to occur. If both of these conditions are met then a generation rate for electrons and holes is calculated according to (3.68). The comparison of the reverse stress current predicted by the band-to-band tunneling model with the experimentally measured values will be done in Chapter 4.

3.4 Simplified Hydrodynamic Transport Model

When the emitter-base junction is reverse biased, the electrons, as minority carriers, in the base region (p-type) move into the emitter region (n-type) due to the electric field in the depletion region. The HTM solves for the average electron

temperature (or energy) for the electron population. The averaging of the energies of hot electrons which originate in the base region with the much larger population of electrons in the emitter region causes the electron energy information to often be inaccurate due to numerical accuracy limitation. In order to examine the behavior of only the hot electrons, a simplified Hydrodynamic Transport Model (SHTM) based on the energy conservation equation is developed in this section.

Equation (3.24f) gives the electron energy flux as

$$\mathbf{S}_n = -\kappa(T_n)\nabla T_n - \mathbf{J}_n \delta(T_n) k_B T_n / q. \tag{3.71}$$

The first term on the left hand side is neglected because the thermal conductivity is small in the depletion region due to the small electron concentration (see (3.7), the Wiedemann-Franz relationship). Due to a very strong electric field in the depletion region, the dominant current is the drift current. This allows the electron current density $\mathbf{J}_n$ to be approximated by

$$\mathbf{J}_n \approx qn\mu_n(T_n)\mathbf{E}. \tag{3.72}$$

Since the SHTM will be applied to the surface portion of the depletion region, (3.71) can be reduced to a scalar equation as

$$S_n \approx n\mu_n E \delta k_B T_n \tag{3.73}$$

Note that when reducing to a scalar quantity, the electric field is in the opposite direction of the energy flux and was substituted by a -E term.

Neglecting the recombination term and using $\frac{\xi - \xi_o}{\tau_e}$ as the energy absorption rate, the energy conservation equation (3.24d) is expressed as

$$\frac{dS_n}{dx} = J_n E - n\frac{3}{2}k_B \frac{T_n - T_o}{\tau_e} \tag{3.74}$$

Substitute (3.73) into (3.74) and assume that the dominant change in the energy flux is due to the energy (electron temperature) change, the energy conservation equation can be reduced to be

$$\frac{dT_n}{dx} = \frac{qE}{\delta k_B} - \frac{3}{2}\frac{T_n - T_o}{\mu(T_n)\delta E \tau_e}. \tag{3.75}$$

The use of (3.75) to solve for the electron temperature with the electric field extracted from a DD device simulation will be referred to as the 'Simplified Hydrodynamic Transport Model' (SHTM). SHTM can be treated as an extension of the DD model by solving an additional simplified energy conservation equation. The consistency of the scheme adopted by SHTM can be verified by examining the electric field intensity and the electron population solved by full HTM device simulations and DD device simulations. If the number of hot electrons is small compared to the overall population, most of the macroscopic quantities are unchanged by this subpopulation of electrons. Figure 3.6 shows the comparison of the electric field and electron concentration for a pn junction doped with 10^{18} cm^{-3} (p-type) and 10^{20} cm^{-3} (n-type) operated at -4 V of reverse bias. This comparison shows that the SHTM is valid in the reverse bias stress conditions.

Another way of deriving (3.75) is to consider the rate of gaining and losing energy for electrons as

$$\frac{d\xi}{dx} = qE \qquad \text{(Energy Increase)} \tag{3.76}$$

$$\frac{d\xi}{dt} = -\frac{\xi - \xi_o}{\tau_e} \qquad \text{(Energy Decrease)} \tag{3.77}$$

The total energy increase of the electrons traveling a distance dx can thus be written as

$$\frac{d\xi}{dx} = qE - \frac{\xi - \xi_o}{\tau_e}\frac{dt}{dx}. \tag{3.78}$$

Assuming $dx/dt = v = \mu E$ and $\xi = 3k_B T_n/2$, (3.78) can be expressed as

$$\frac{dT_n}{dx} = \frac{qE}{\frac{3}{2}k_B} - \frac{T_n - T_o}{\tau_e \mu(T_n)E}. \tag{3.79}$$

The similarity between (3.79) and (3.75) indicates that the SHTM can be correlated to classical mechanics by suitably choosing the parameters δ, μ, and τ_e. The

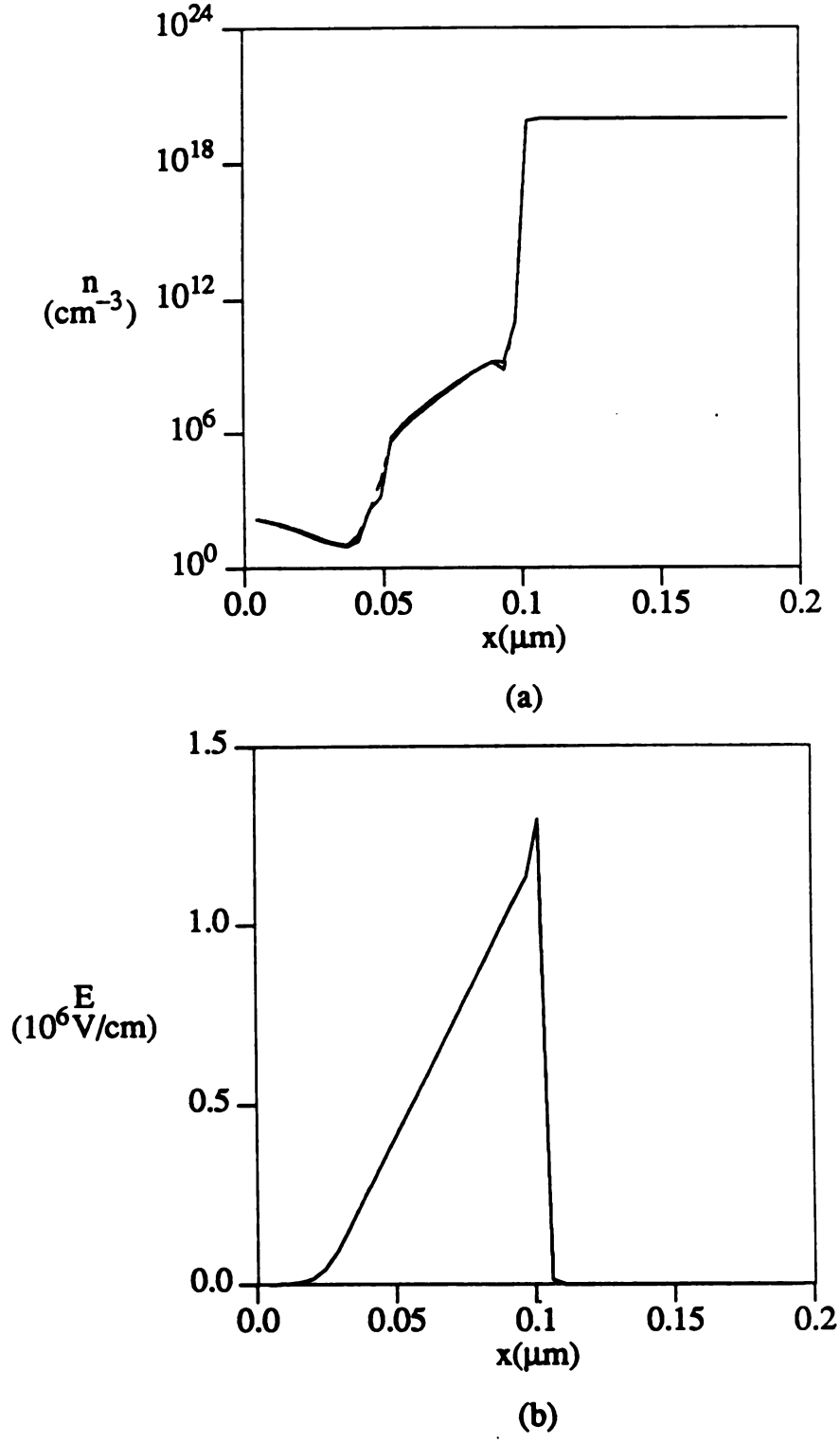


Figure 3.6: Comparison for (a) the electron concentration and (b) the electric field for a pn junction at -4 V reverse bias. Solid line is from DD model and dashed line is from HTM model.

use of the Monte Carlo particle simulation technique to extract these material parameters is explained in the next section.

It is assumed in the simplified HTM model that the interface states are created by hot electrons and not hot holes. This approximation is made because the hot electrons occurred spatially at positions where the depletion region is present during forward bias. The hot holes occur more towards the base side of the depletion region and under forward bias conditions this region is not in the depletion region. Any interface states created by hot holes, therefore, do not expect to alter the forward bias electrical characteristics.

3.5 Monte Carlo Method for HTM Parameter Extraction

To use the simplified HTM model requires the material parameters δ, μ, and τ_e as functions of energy or electron temperature. The Monte Carlo method is a particle simulation which records the state of simulated particles before and after each scattering event. The physical quantities such as the velocity, the location, and the energy at a specific time can be derived from the information provided by the recorded states. The scattering mechanisms included in this Monte Carlo method are ionized impurity scattering, acoustic phonon scattering, and intervalley optical phonon scattering. The band structure used was a nonparabolic band structure. In this section, the use of single particle steady state and transient Monte Carlo simulations to extract the material parameters will be explained.

The mobility μ versus electron temperature is determined by using steady state Monte Carlo simulations on an uniformly doped region for electric field intensities ranging from 5×10^4 V/cm to 1×10^6 V/cm. From Monte Carlo simulation, the average velocity and energy at a specific electric field is obtained. The electron temperature is derived from the average energy ξ as

$$\xi = \frac{3}{2} k_B T_n . \tag{3.80}$$

The mobility is derived by using the average velocity v and electric field E as

$$\mu(T_n) = \frac{v(T_n)}{E} . \tag{3.81}$$

The Monte Carlo simulations have been done to obtain the mobilities at lattice temperatures of -75, 23, 175, and 240 C. Combining the energy independent mobility model as described in (3.67) for the low energy limit with the Monte Carlo simulated mobility versus electron temperature for impurity concentrations of 10^{15} cm^{-3} and 10^{18} cm^{-3} , the results shown in Figure 3.7 are obtained.

The material parameter δ determines the rate of energy increase versus position due to the external electric field and τ_e determines the saturation value of energy once μ and δ are fixed. These two parameters are determined by fitting the simplified HTM to a transient Monte Carlo simulation. By using the electric field extracted from DD simulations for the transistor operating at -4 V reverse bias (see Figure 3.8a), the transient Monte Carlo simulations were used to record the energy versus position as shown in Figure 3.8(b). The simplified HTM was solved for the same electric field profile. By adjusting the values of δ and τ_e, a best fit was achieved. The same procedure was used for extracting these two parameters at lattice temperatures of -75, 23, 175, and 240 C. The electric field profile and the fit of simplified HTM to Monte Carlo simulation at 23 C are shown in Figure 3.8(a) and 3.8(b) respectively. δ and τ_e determined by this method are listed in Table 3.1 for the four lattice temperatures.

3.6 List of Parameters for Device Simulations

For all the device simulations done throughout this research, the numerical values of the material parameters and their corresponding equation numbers are listed in Table 3.2.

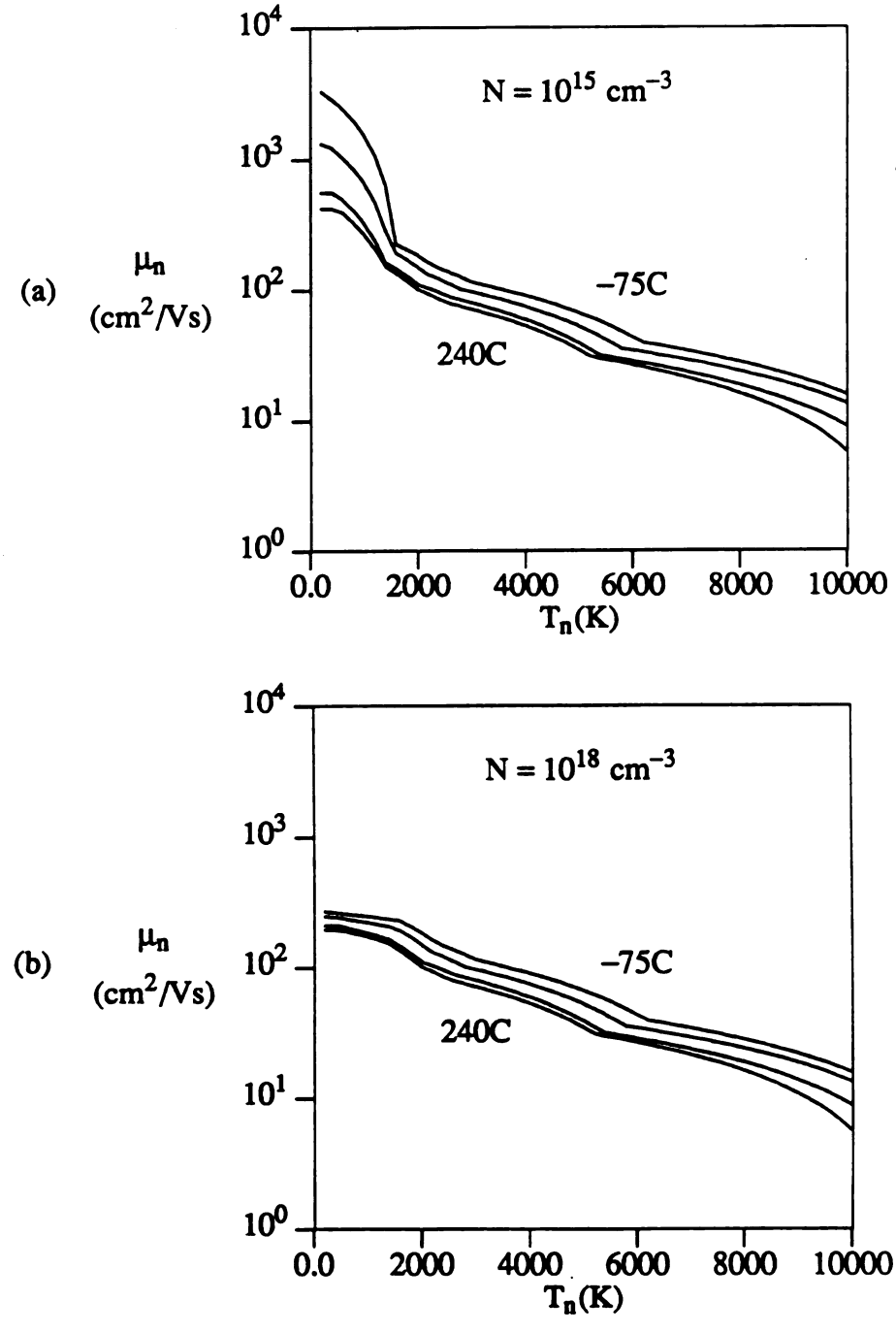


Figure 3.7: The electron mobility versus electron temperature at lattice temperatures of -75, 23, 175, and 240 C for doping concentrations of (a) 10^{15} cm^{-3} and (b) 10^{18} cm^{-3}.

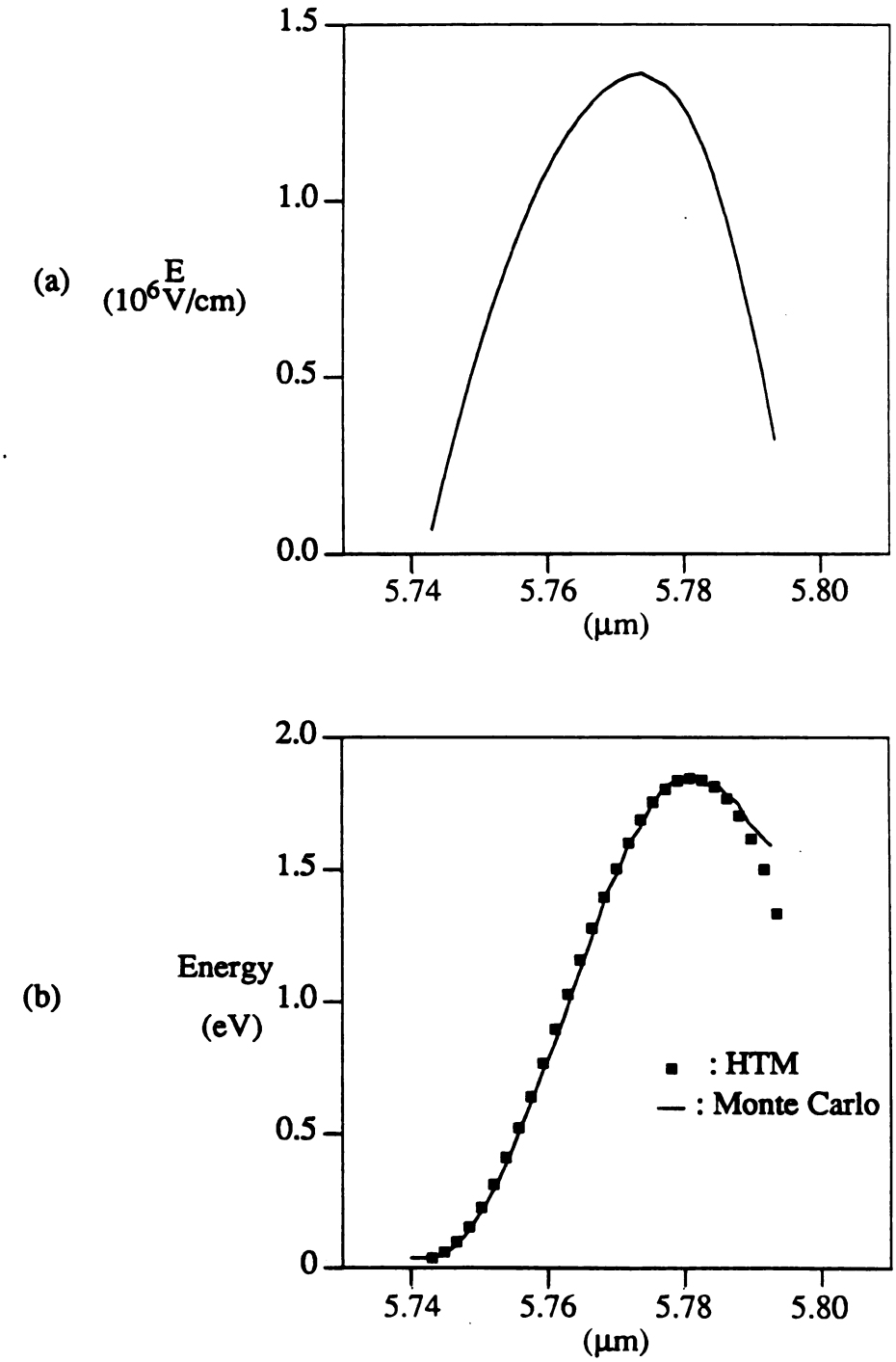


Figure 3.8: (a) The electric field profile and (b) the fit of simplified HTM with the Monte Carlo simulation results at 23 C.

	δ (dimensionless)	τ_e (psecond)
-75 C	2.0	0.13
23 C	2.0	0.15
175 C	2.0	0.17
240 C	2.0	0.17

Table 3.1: δ and τ_e at four temperatures determined by fitting the SHTM with the Monte Carlo simulation.

Parameter	Equation Number	Value	Unit
τ_p	(3.58b)	$1.0 \cdot 10^{-7}$	second
τ_n	(3.58b)	$1.0 \cdot 10^{-7}$	second
c_n	(3.58c)	$2.8 \cdot 10^{-43}$	m^6/s
c_p	(3.58c)	$0.99 \cdot 10^{-43}$	m^6/s
E_t	(3.58b)	E_i	eV
$N_C(300K)$	(3.65a)	$2.8 \cdot 10^{25}$	m^{-3}
$N_V(300K)$	(3.65b)	$1.04 \cdot 10^{25}$	m^{-3}
$E_G(0K)$	(3.64)	1.17	eV
α	(3.64)	$4.73 \cdot 10^{-4}$	$eV/^oK$
β	(3.64)	636	^oK
m_r	(3.71)	$0.14m_o$	kg

Table 3.2: Parameters for device simulation program.

Chapter 4

Analysis and Simulation of Unstressed Bipolar Transistor Characteristics

Before simulating the amount of hot electron produced degradation, the unstressed characteristics must first be simulated in order to establish an accurate simulation model for the bipolar transistor. In this chapter, the unstressed bipolar transistor characteristics will be analyzed and simulated for both the reverse bias stress conditions and the forward bias Gummel measurement conditions. By first obtaining a good match between measurements and simulations for these unstressed conditions, a more accurate simulation of the hot electron current and the degradation rate can be achieved.

4.1 Reverse Bias Stress Conditions

The reverse bias stress condition will first be analyzed by using PISCES-II [24] simulations followed by using the device simulator developed in this work. Simulation studies using the PISCES-II simulator were conducted for TIN3 and TOUT devices using the BJT structure as shown in Figure 4.1(a) in order to match the experimental characteristics of the unstressed transistors. The bipolar structure simulated has a length of 9 μm and a depth of 1.4 μm. The structure includes an oxide interface in the region of the base-emitter junction. Figures 4.1(b) and 4.1(c) show the actual and enlarged grid structure used in the PISCES-II program for the BJT structure. The doping profile includes the intrinsic and extrinsic base regions, the emitter region, and the collector region [36] as shown previously in Figure 2.4.

The PISCES-II simulator has been used to investigate the electric fields present in the bipolar structure. The reverse bias stress conditions produced significant hot electron

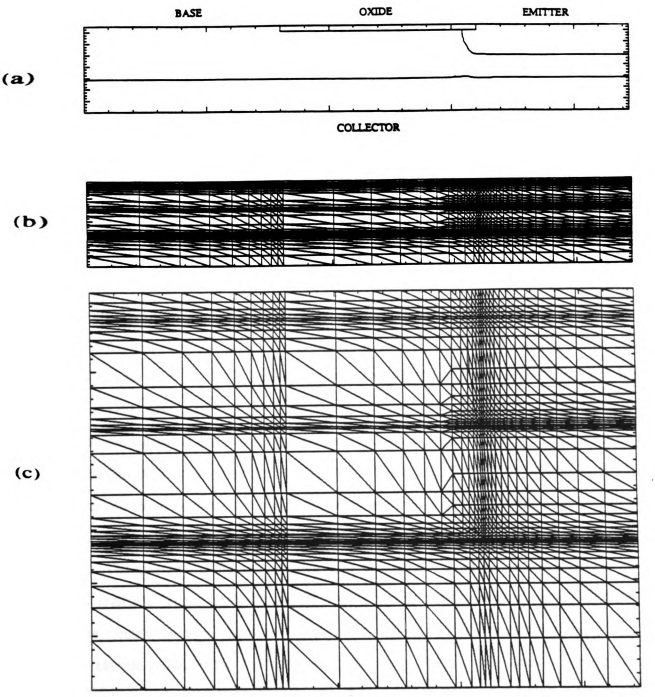
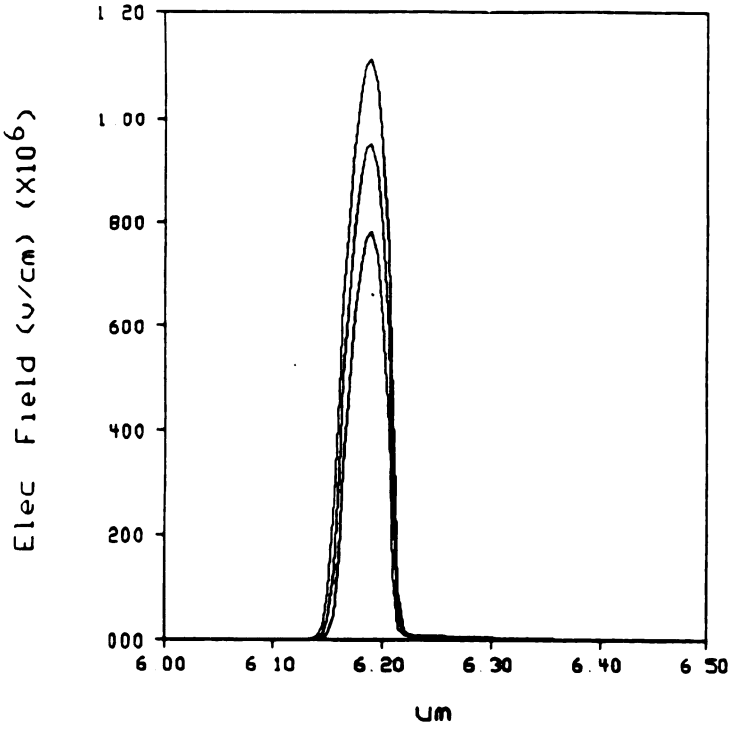


Figure 4.1: (a) The BJT structure with 0.1 μm thickness of oxide simulated by the PISCES-II device simulator. (b) The actual grid structure for device simulation. (c) The enlarged grid structure of (b).

degradation (see Chapter 2) which occurs at the oxide interface of the base and emitter junction. Figure 4.2 shows the electric field in the lateral direction at the emitter-base junction just below the oxide interface for simulation bias values of -2, -3, and -4 volts. The figure shows the electric fields calculated assuming two different lateral doping profiles. The calculated electric field assuming a spacing between the extrinsic base and the emitter region of 0.4 μm and lateral doping diffusions having the same form as the vertical doping diffusions but shrunk by 60% are in the range of 0.7×10^6 to 1.1×10^6 V/cm. Alternatively, the calculated electric field assuming a spacing between the extrinsic base and the emitter region of 1.0 μm are in the range of 4×10^5 to 6×10^5 V/cm. These electric fields are sufficiently large to produce hot electrons. The presence of large electric fields at the emitter-base junction is also indicated by the reverse bias emitter-base junction current characteristics as shown in Figure 4.3. This reverse bias characteristic shows a large leakage component which is likely a tunneling leakage current [16]. Also present in the reverse bias characteristics is a more rapid increase in the reverse current in the voltage range of 4.5 to 5 volts which corresponds to the start of junction breakdown. Reverse bias breakdown voltages in this range are usually attributed to breakdown by tunneling which requires an electric field of approximately 1×10^6 V/cm [4].

The reverse bias electric field was also simulated with a fixed charge placed at the oxide interface. These simulations were done to assess the influence of oxide fix charge on the electric fields in the bipolar transistor, in particular, the vertical component of these electric fields. In the simulator, the oxide fixed charge concentration is varied by the PISCES-II parameter Q_f. The effect of this parameter is to provide a boundary condition for the Poisson equation which determines the surface band bending at a given bias voltage. With a relatively large reverse bias, however, band bending will be determined by the bias voltage. For example, a large oxide fixed charge concentration of 1×10^{12} cm^{-2} produced only a minimal change in the electric field for stress condition

(a)



(b)

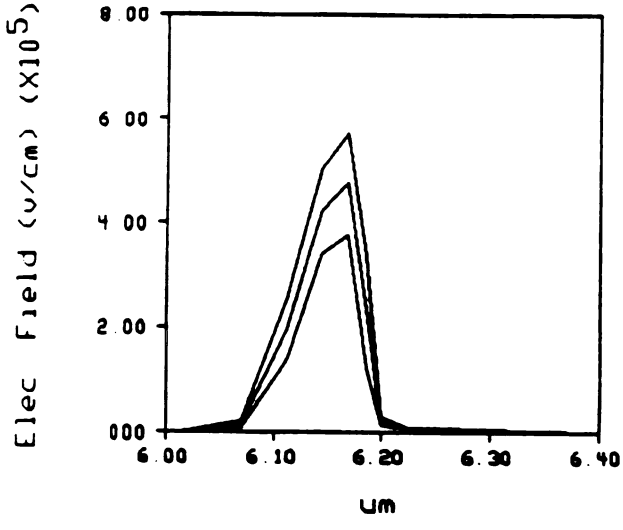


Figure 4.2: The lateral electric field below the oxide interface with reverse bias voltages of -2, -3, -4 volts for assumed spacings between the extrinsic base and emitter region of (a) 0.4 μm and (b) 1.0 μm.

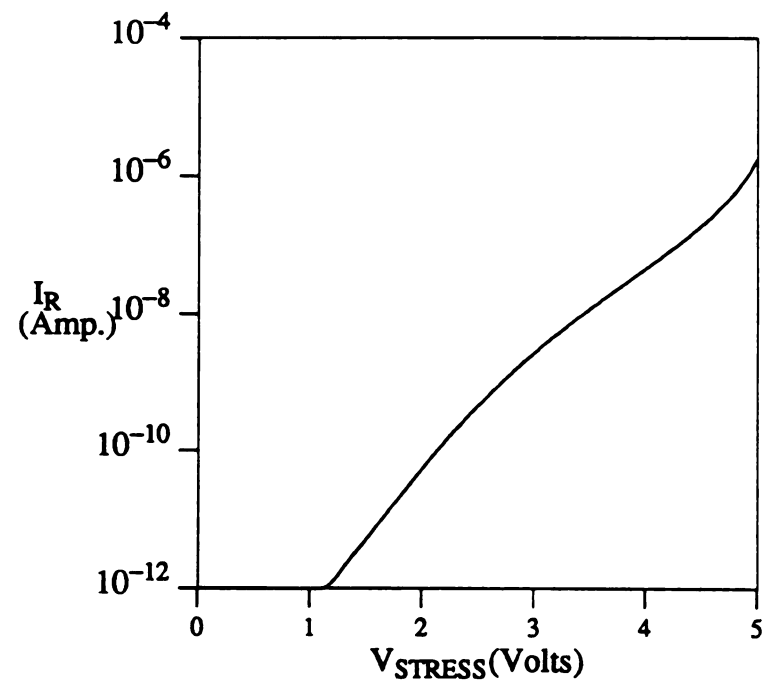


Figure 4.3: The measured data of reverse bias stress current versus V_{BE} at room temperature.

reverse bias voltages. This change was observed as a small vertical electric field component as shown by the potential plots in Figure 4.4. This vertical field component is significantly smaller than the lateral electric field component. An absence of strong vertical electric fields would suggest that the hot electron process proceeds as an acceleration of the electrons in the lateral direction followed by an elastic or inelastic (with only a small change in the electron energy) collision event which changes the direction of the electron so that it interacts with the oxide interface breaking bonds or becoming trapped in the oxide.

Since PISCES-II simulations do not include the band-to-band tunneling current calculation, the predicted reverse bias stress current can not be compared to the measured data. In the rest of this section, the reverse bias stress condition is simulated by using the device simulator developed in this study. The bipolar simulations were done using both the HTM and DD models. For the emitter-base reverse bias conditions, no difference was observed in the currents and electric fields calculated by the two models.

The bipolar transistor simulated has the same emitter area as the one used in PISCES-II simulations. The lateral doping profile has been examined by fitting the reverse bias stress current to the measurement data. Figure 4.5 shows the reverse bias stress currents for three different base doping levels with corresponding surface base doping of 1.1×10^{18}, 5.6×10^{17}, and 2.2×10^{17} cm^{-3}. Since Figure 4.5 indicates that the surface base doping of 5.6×10^{17} cm^{-3} gives the best fit to the experimental data, this profile was used for the extraction of the hot electron quantities as will be explained in Chapter 5. The emitter doping profile in the lateral direction is the same as the vertical doping profile but is shrunk by 60%.

The electric field for the 5.6×10^{17} cm^{-3} surface base doping BJT structure operating at -4 V reverse bias has a peak value of 1.3×10^{6} V/cm comparing to the 1.1×10^{6} V/cm predicted by PISCES-II simulation mentioned earlier. The temperature dependence of the reverse bias stress current exhibits tunneling type characteristics.

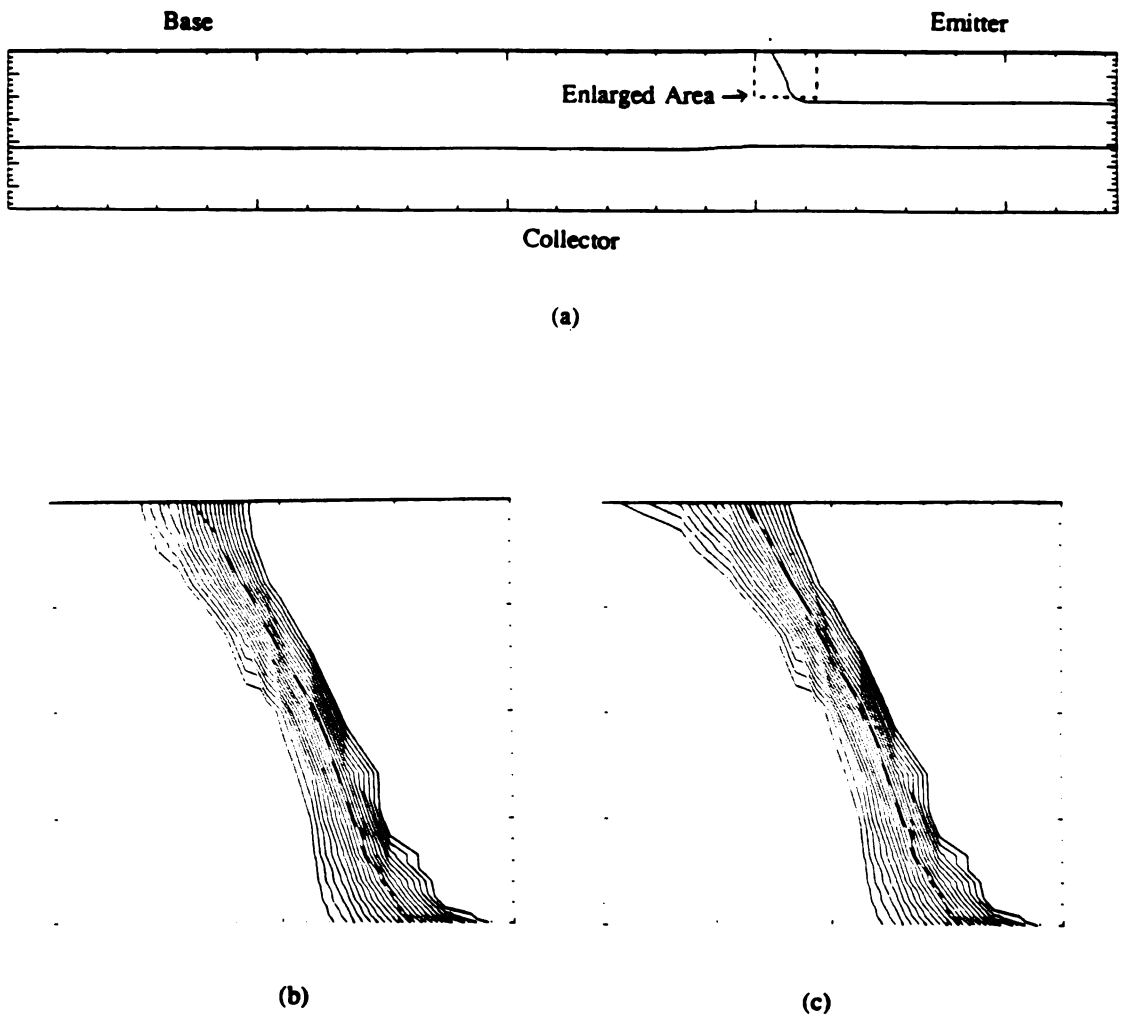


Figure 4.4: The potential plots for reverse biasing the transistor showing (a) the transistor structure indicating the enlarged region, (b) the potential plot without oxide fixed charge, and (c) the potential plot with the oxide fixed charge.

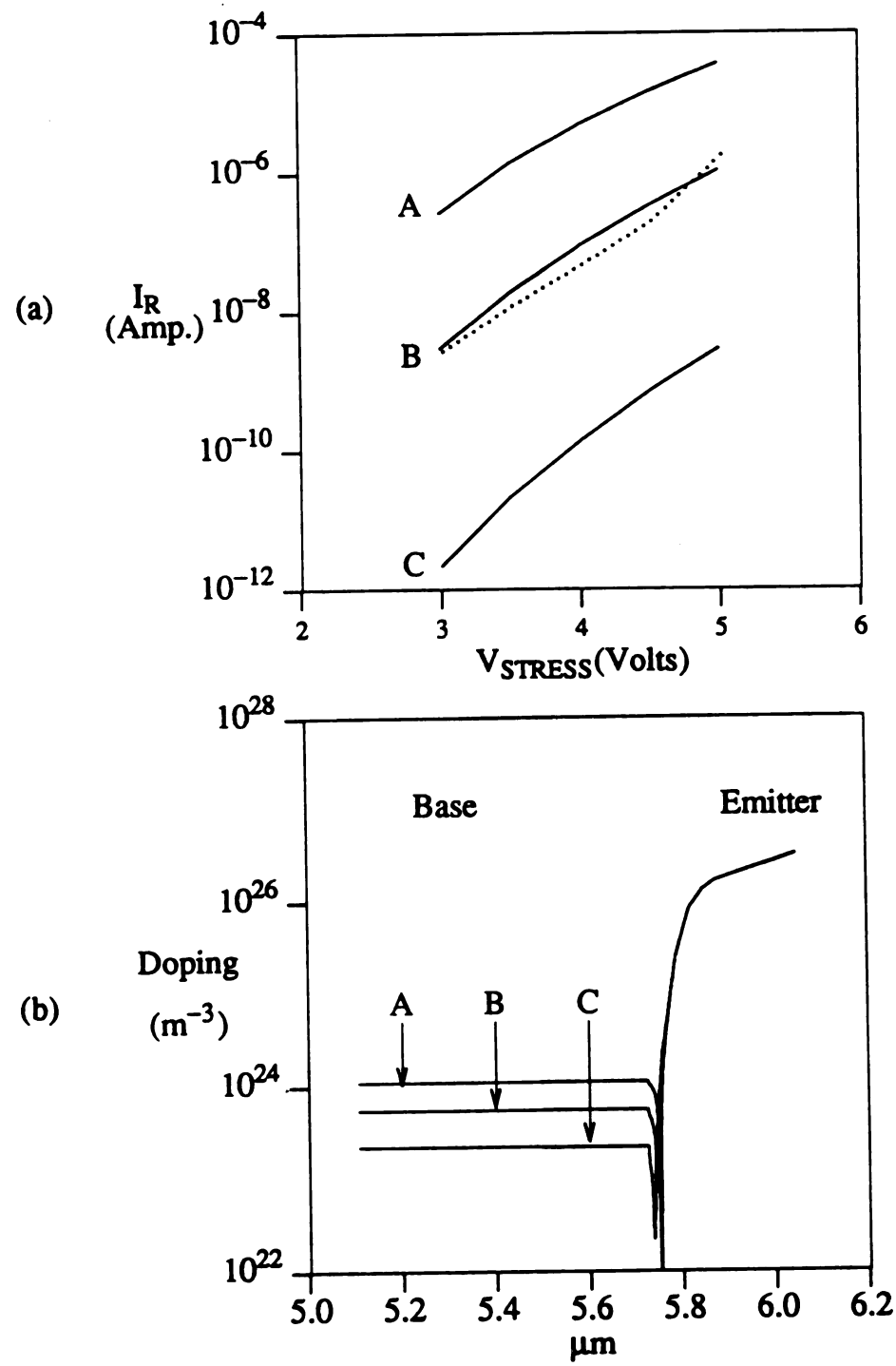


Figure 4.5: The reverse bias stress currents and their respective lateral doping profiles showing: (a) The simulated reverse bias stress current and the measured current versus V_{BE}. The dashed line is the measured data. (b) The lateral doping profiles of different base doping level.

Table 4.1 lists the reverse bias stress current at V_{BE} = -4V for the measured data and the simulated data for temperatures of -75, 23, 175, and 240 C.

4.2 Gummel Characteristics

Simulations of the forward Gummel characteristics were also performed by using both the PISCES-II simulator and the simulator developed in this study. By using the same doping structure found in the previous section, PISCES-II produces the unstressed current gain characteristics of the transistors at room temperature as shown in Figure 4.6. The phenomena included in the simulations were bandgap narrowing, incomplete ionization of donors and acceptors, Fermi-Dirac statistics, Auger recombination, and Schockley-Reed-Hall (SRH) recombination. This figure shows the simulated values of current gain, h_{FE}, with all effects included (curve IFSBA), with Auger recombination not considered (curve IFSB), and with Auger and SRH recombination not considered (curve IFB).

The simulated transistor gain characteristics including all the above mentioned phenomena are compared to the minimum and maximum measured gain characteristics for the transistors in Figure 4.7. The midrange V_{BE} values from V_{BE} = 0.4 to V_{BE} = 0.8 volts show good agreement. The low voltage region (V_{BE} < 0.4 volts) of the experimental data is undeterminable because the current is less than 1 picoampere (the limit of the measurement equipment). The high voltage region (V_{BE} > 0.8 volts) shows discrepancies which may be attributed to parasitic effects not included in the simulation such as lateral device resistance and metalization voltage drops.

The forward-active bias conditions were also simulated to determine the electric field. Figure 4.8 shows the electric field in the vertical direction along a line which passes through the emitter, base, and collector. The collector-base voltage was 2 volts and the base-emitter voltages were 0.6, 0.7, 0.8, 0.9, 1.0, and 1.1. The electric field at the base-emitter junction was found by the simulation to be less than 0.5×10^5 V/cm. This

	I_R (Measurement) (Amp)	I_R (Simulated) (Amp)
-75 C	$2.83 \cdot 10^{-8}$	$4.69 \cdot 10^{-8}$
23 C	$5.43 \cdot 10^{-8}$	$6.88 \cdot 10^{-8}$
175 C	$3.29 \cdot 10^{-7}$	$1.39 \cdot 10^{-7}$
240 C	$1.94 \cdot 10^{-6}$	$1.98 \cdot 10^{-7}$

Table 4.1: The reverse bias stress current at -4 V reverse bias for temperatures of -75, 23, 175, and 240 C.

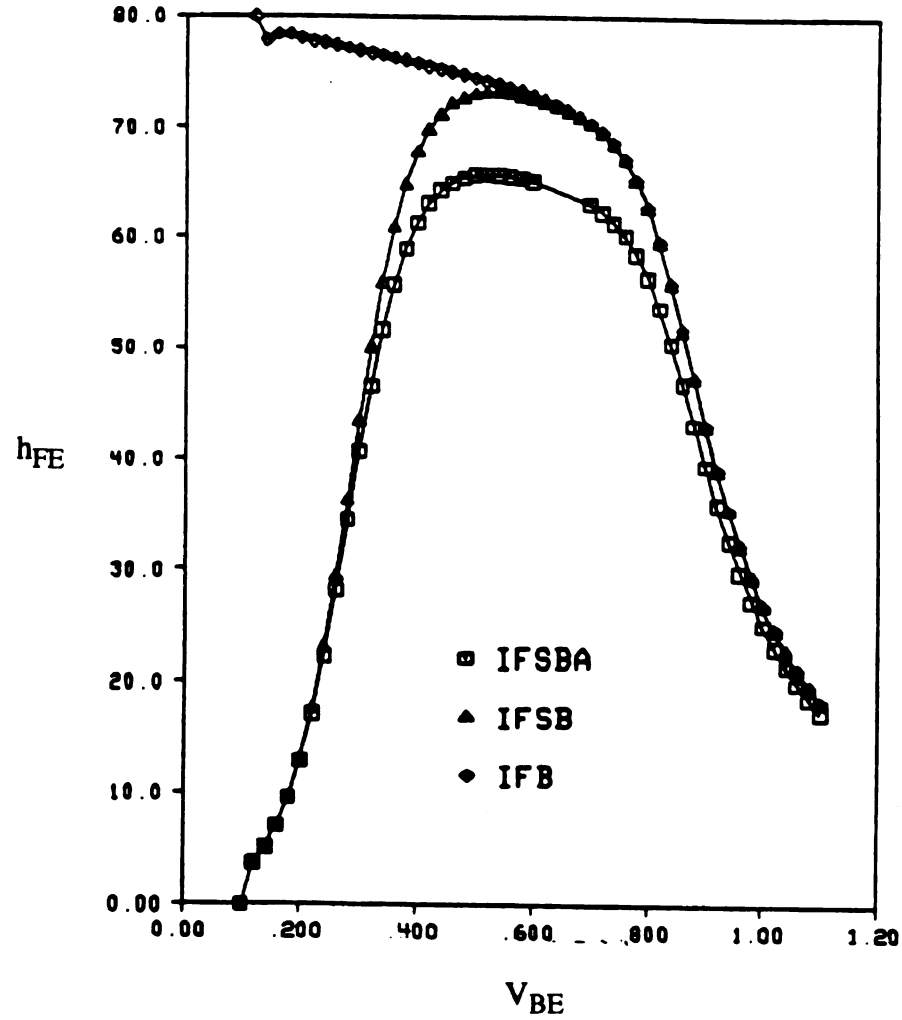


Figure 4.6: Unstressed current gain characteristics at room temperature. IFSBA curve included incomplete ionization, Fermi-Dirac statistics, SRH recombination, bandgap narrowing, Auger recombination. IFSB curve does not include Auger recombination. IFB curve does not include Auger and SRH recombination.

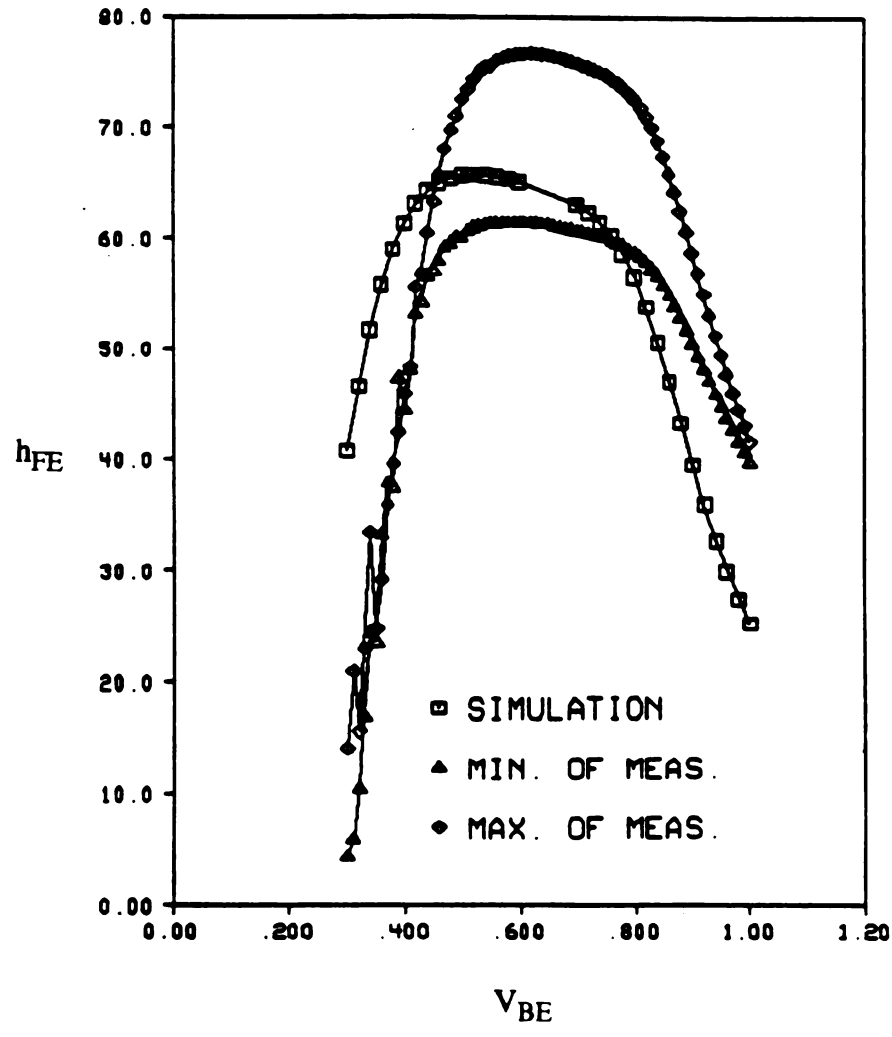


Figure 4.7: Simulated current gain compared to the minimum and maximum measured current gain characteristics.

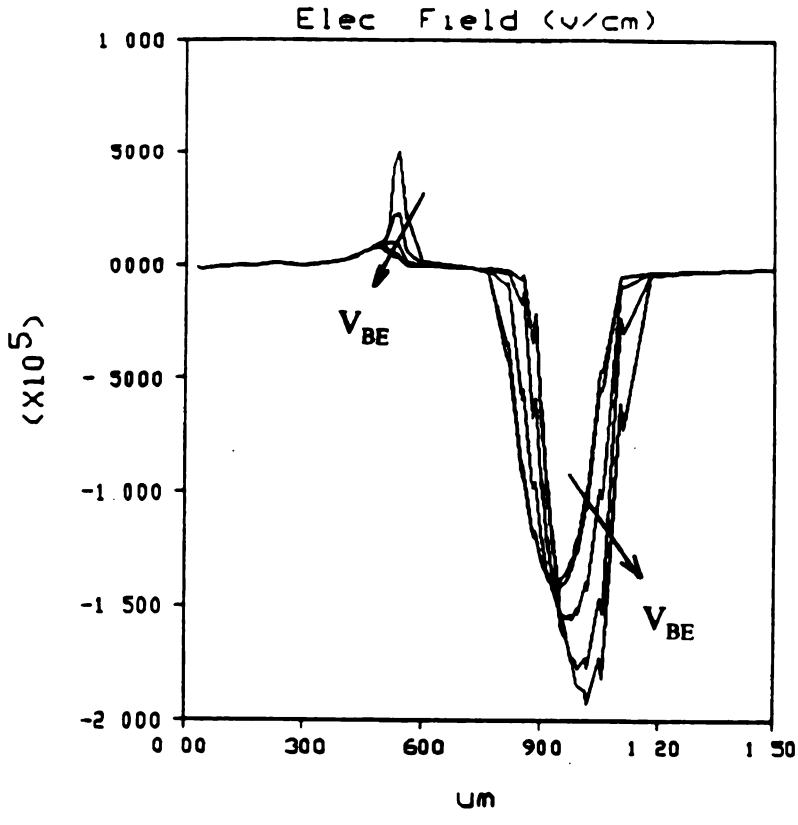


Figure 4.8: Electric field simulated in the vertical direction along the emitter, base, and collector for V_{CB} = 2 V and V_{BE} = 0.6, 0.7, 0.8, 0.9, 1.0, and 1.1 volts.

magnitude of electric field is not suggestive of the creation of hot electrons. The electric fields at the collector-base junction in Figure 4.8 show that there is only a minimal movement of the peak electric field into the collector region as the current increases. This occurs because the collector doping is large enough to minimize the Kirk effect. The electric field for these forward bias conditions was also checked at the emitter-base junction close to the oxide interface. For forward bias conditions, the electric field in this region was again less than 0.5×10^5 V/cm for $V_{BE} > 0.5$ volts.

The device simulation program developed in this study was also used to simulate the unstressed characteristics. The simulated Gummel plot including bandgap narrowing, SRH recombination, and Auger recombination effects is compared in Figure 4.9 with the room temperature experimental value. The simulated Gummel characteristic shows a smaller collector current but gives a good fit to the base current. The discrepancy for the collector current is acceptable since (1) the goal of this simulation is to best match the unstressed base current and (2) the degradation model to be developed will be based on the changes in the unstressed and stressed base currents. The use and the development of the degradation model will be described in Chapter 5 and 6.

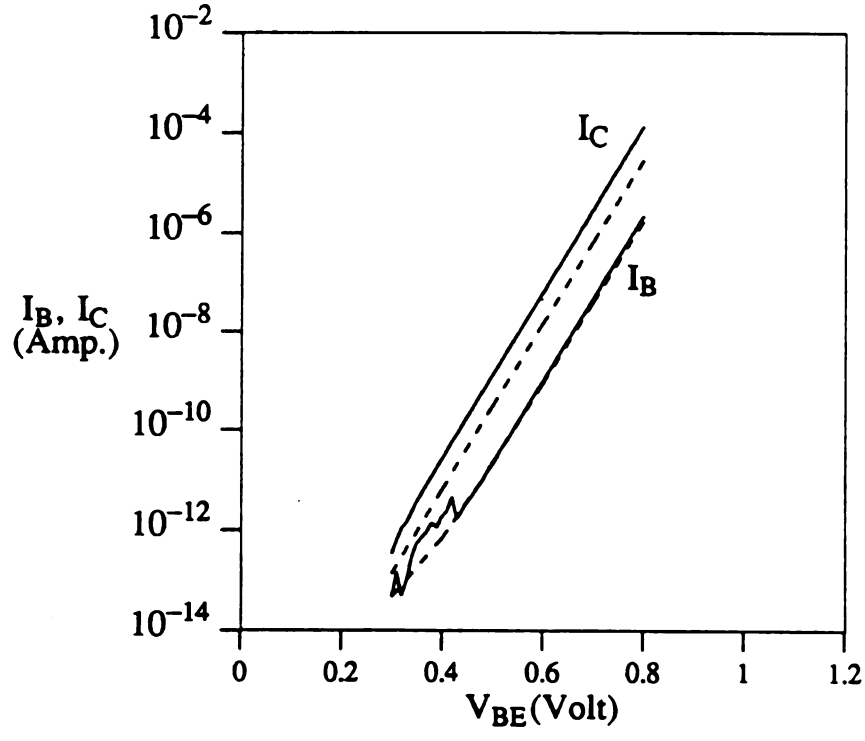


Figure 4.9: Simulated unstressed Gummel characteristics (solid line) compared to the measured unstressed Gummel characteristics (dashed line).

Chapter 5

Simulation of Hot Electron Induced Degradation for Bipolar Transistors

With appropriate degradation models, a device level simulation program can provide a microscopic view of the degradation giving more insight for device lifetime improvements. A complete analysis for the degradation of bipolar transistors must consider both calculations of the number and energy of the carriers producing the damage and the significant tunneling currents at device degradation voltages.

This chapter presents the results of device level simulations that: (1) extract the reverse bias stress currents including the band-to-band tunneling current mechanism, (2) use the simplified Hydrodynamic Transport Model (SHTM) to solve for the number of hot electrons per unit time adjacent to the Si-SiO_2 interface where the damage occurs, (3) predict the increase of surface recombination velocity based on an interface state creation model calculated from the quantity of hot electrons, and (4) predict the voltage dependence and time progression of the hot electron induced degradation. The procedures are detailed in the following sections.

5.1 Hot Electron Current Simulations

The simulation of hot electron degradation at the reverse-biased base-emitter junction in bipolar transistors begins by simulating the number of electrons passing adjacent to the Si-SiO_2 interface per unit time with enough energy to cause damage. This quantity is best represented as the hot electron current density, J_{hot}.

As described earlier in Chapter 3, the electron energy solutions for reverse bias junctions can be decoupled from the Poisson and the two continuity equations. By using

DD device simulations, the electric field and the electron current density for reverse bias stress conditions were extracted. The simulated BJT structure is shown in Figure 5.1. The vertical doping profile used was shown earlier in Figure 2.4. The simplified HTM model is then used for the calculation of the average electron energy. To include the tunneling generated electrons, the depletion region is divided into small intervals where in each interval an SHTM energy calculation was applied to the subpopulation of electrons generated due to tunneling in this interval. An average of electron energy is then calculated to obtain the electron temperature T_n. J_{hot} is determined from the reverse bias current density J_{dep} and from the electron temperature T_n of the electrons originating in the depletion-region according to the expression

$$J_{hot} = J_{dep} \cdot \exp(-\phi / k_B T_n) \tag{5.1}$$

where ϕ is the energy threshold (2.0 eV) capable of producing hot electron damage [17]. Figure 5.2 (a) shows the hot electron current versus position for reverse biasing the emitter-base junction of the bipolar transistors at room temperature for voltages of 3.5, 4.0, 4.5, and 5.0 volts. At higher reverse bias voltages, the hot electron current is higher due to a higher electric field. At higher electric fields, both the tunneling rate and the electron temperature are increased leading to a larger J_{hot}. Figure 5.2(b) shows the electron tunneling rate versus position for the corresponding reverse bias voltages. By comparing Figure 5.2(a) and 5.2(b) it can be seen that the hot electron current originates mostly from the band-to-band tunneling process. The magnitude of the hot electron current originating from the base side is about 4 orders of magnitude smaller than that originating from the tunneling process as seen by comparing J_{hot} at 5.75 μm to J_{hot} at locations > 5.77 μm where tunneling is significant.

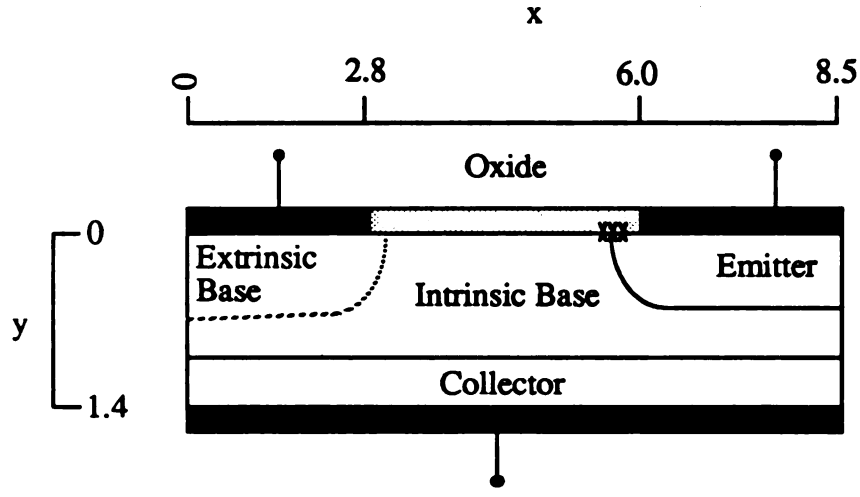


Figure 5.1: Bipolar structure simulated. The dimensions are in micrometers.

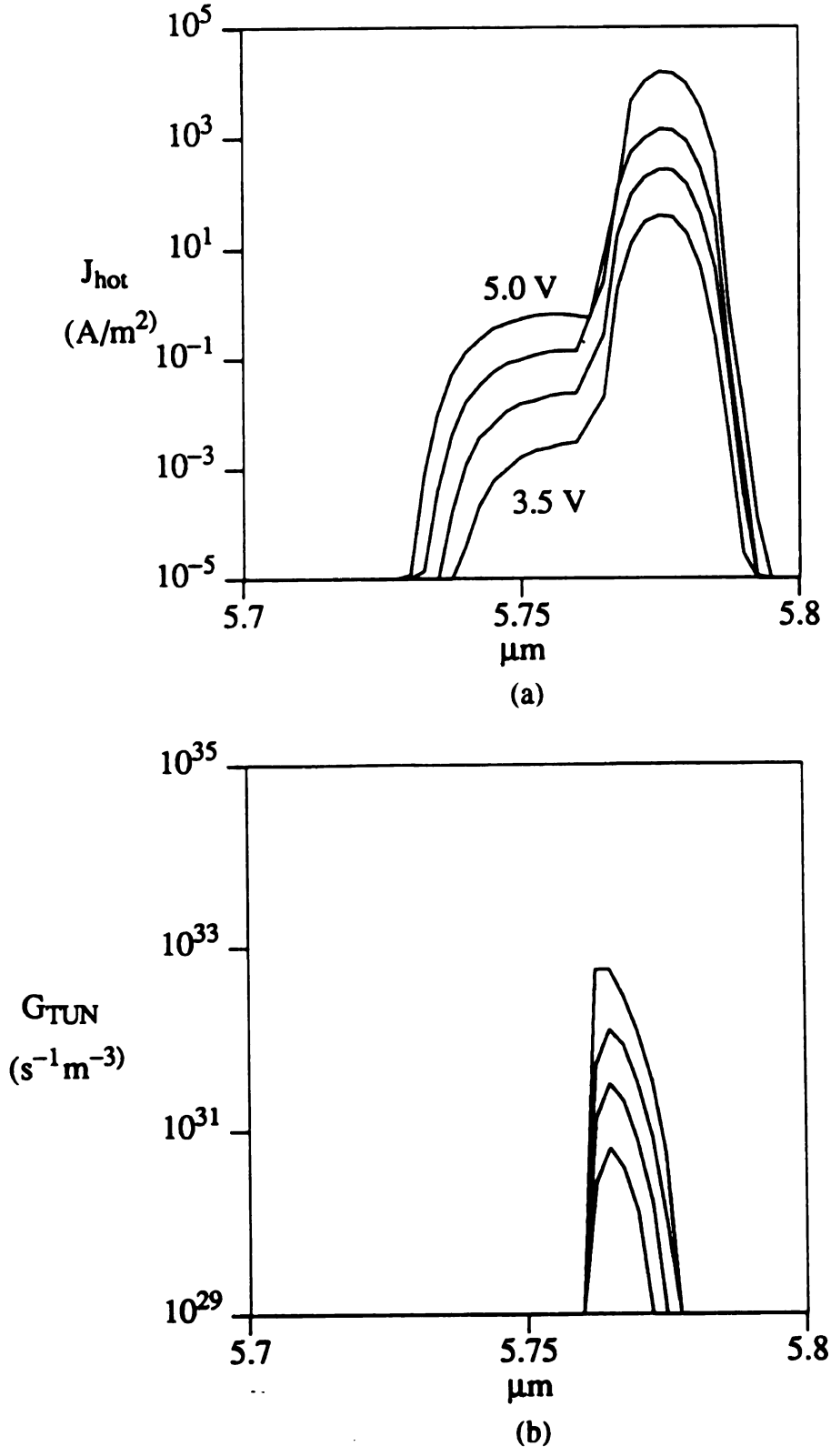


Figure 5.2: (a) Hot electron current densities versus position for reverse bias voltages of 3.5, 4.0, 4.5, and 5.0 volts. (b) The corresponding electron tunneling rate versus position.

5.2 Degradation Model

In this section, the hot electron induced degradation is modeled by an increase in the density of interface states resulting from hot electron damage of the Si-SiO_2 interface. The interface states give rise to an increase of the surface recombination velocity and thus, the base leakage current.

From earlier MOSFET work [14-16], the interface state creation from a current with energetic hot electrons can be written as

$$N_{it} \propto (t\frac{I_d}{W}e^{-\phi/k_B T_n})^n \tag{5.2}$$

assuming the energy distribution of the hot electrons is Maxwellian. I_d is the drain current, W is the channel length, t is the stress time, T_n is the electron temperature, k_B is the Boltzmann constant, ϕ is the critical energy for the breaking of a Si-H bond, and n is the fitting parameter for the relationship between the number of hot electrons present and the number of interface states created. For BJT simulation, it is found that the rate of creation of interface states has a different time dependence [7,8]. Equation (5.2) is modified to become

$$N_{it} \propto (t)^{n_1} (J_{hot})^{n_2} \tag{5.3}$$

where n_1 and n_2 are parameters which are adjusted to achieved a best fit for the dependence on the stress time and the hot electron current density.

After the hot electron current is solved along the Si-SiO_2 interface, the number of reverse bias induced interface states in the base-emitter depletion region is imported into the forward bias Gummel characteristics calculations. The increase of the interface state density results in an increase of the surface recombination velocity which is expressed as

$$S_o = \sigma v_{th} N_{it} \tag{5.4}$$

where σ is the scattering cross section and v_{th} is the electron thermal velocity. Equation (5.3) and (5.4) can be combined to formulate an expression suitable for device simulation programs. The combined equation for the surface recombination velocity is

$$S_o = c \cdot (t)^{n_1} \cdot (J_{hot})^{n_2} \tag{5.5}$$

where c is a fitting parameter which includes the effects of scattering cross section and the thermal velocity for electrons in silicon. In the forward Gummel measurement where the electric field is weak, the thermal velocity and scattering cross section can be assumed to be constants for a given ambient temperature. Therefore, c is a constant for a given device fabrication technology and ambient temperature.

The surface recombination velocity increases the surface recombination rate which is implemented in the device simulation program by using an equivalent surface recombination life time given as [24]

$$\tau_{SUR} = \frac{A_i}{S_o d_i} \tag{5.6}$$

where A_i and d_i are the area and length of the interface associated with grid point i. The total effective recombination lifetime can be written as

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{SUR}} + \frac{1}{\tau_{SRH}} . \tag{5.7}$$

This effective lifetime is used for recombination rate calculations in the device simulation program in order to model the increase of base leakage current due to the increase of the surface recombination velocity. The simulated degraded characteristics are presented in the next section.

5.3 Simulation of Degraded Characteristics

To calculate the forward degraded characteristics, the surface recombination velocity along the interface is first calculated based on the stress time and the appropriate J_{hot}. The surface recombination velocity values along the oxide interface for reverse biasing the emitter-base junction at -4 V for stress times of 1, 24, and 500 hours are shown in Figure 5.3. The parameters used for Equation (5.5) is c = 3.8, n_1 = 0.35, and n_2 = 0.8. The surface recombination velocities for a stress time of 200 hours at reverse bias voltages of 3.5, 4.0, 4.5, and 5.0 volts are shown in Figure 5.4.

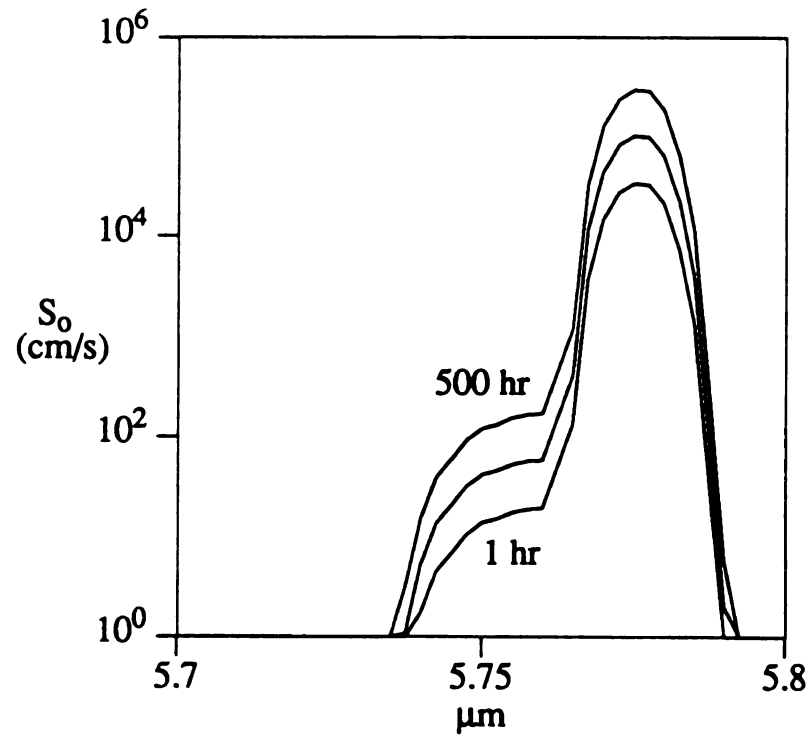


Figure 5.3: The simulated surface recombination velocities for a reverse bias of -4 V after stress times of 1, 24, and 500 hours.

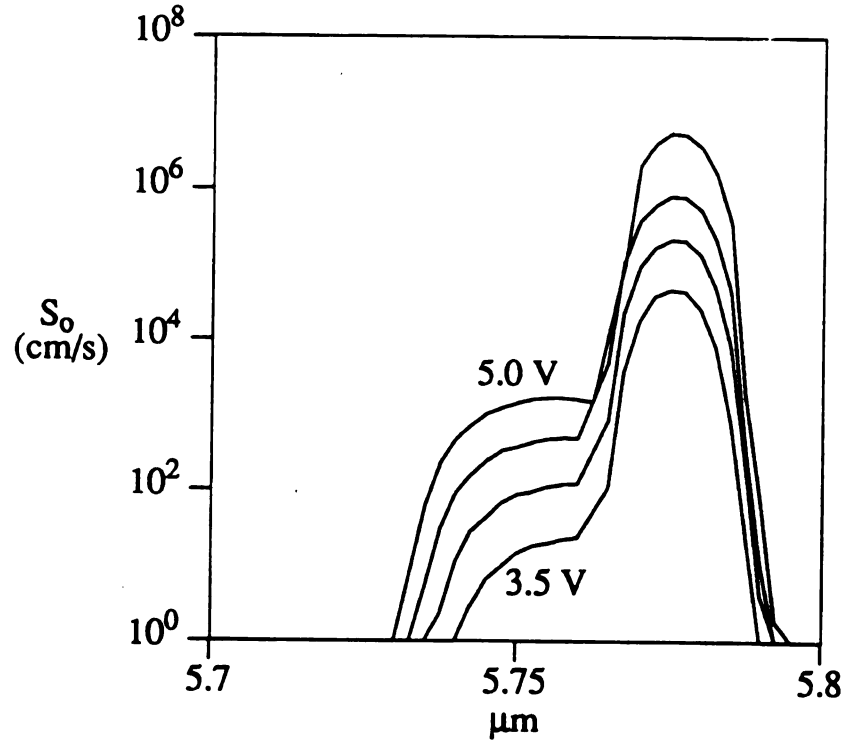


Figure 5.4: The simulated surface recombination velocities for reverse bias voltages of 3.5, 4.0, 4.5, and 5.0 volts after 200 hours stress time.

Since the Gummel characteristics measurement has a zero collector-base voltage while the emitter-base voltage is forward biased, the electron temperature throughout the device is not high. Therefore, the forward Gummel characteristics resulting from the calculated surface recombination velocity profile is simulated by the Drift-Diffusion model to obtain the degraded characteristics. By using the degradation model described above, the degraded characteristics are simulated and compared to the experimental studies as described in Chapter 2. For an example of the modeling of the rate of hot electron induced degradation, Figure 5.5 compares the simulated and measured base currents for stress times of 0, 1, 24, and 500 hours at -4 volts 23 C. For the modeling of the voltage dependence of hot electron induced degradation, Figure 5.6 compares the simulated and measured base current at reverse biases of 3.5, 4.0, 4.5, and 5.0 volts for a stress time of 200 hours. The parameters c, n_1, and n_2 were obtained by fitting the measured and simulated data in Figures 5.5 and 5.6. Figures 5.5 and 5.6 show an excellent fit to the measured results except for stressing the BJT at 5 volts for 200 hours. The discrepancy is understandable since the 5 volts reverse bias is near breakdown voltage and the hot electron degradation process could be altered.

The good agreement for the predicted results for the voltage dependence and time evolution of the degraded characteristics indicates that the degradation model is suitable for implementation into a device level simulation program to predict the change of device degradation when the device design changes. For operating the transistors at temperatures other than room temperature, temperature effects must be carefully evaluated. The next chapter presents a model that includes the temperature effects.

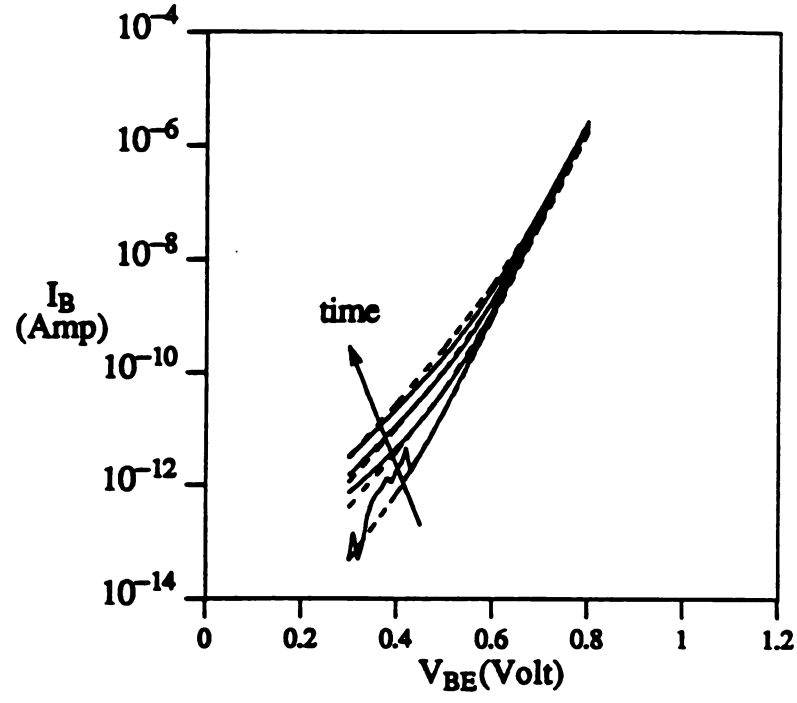


Figure 5.5: Comparison of experimental (solid lines) and simulated (dashed lines) base currents versus V_{BE} for stress times of 0, 1, 24, and 500 hours at a stress voltage of -4 volts.

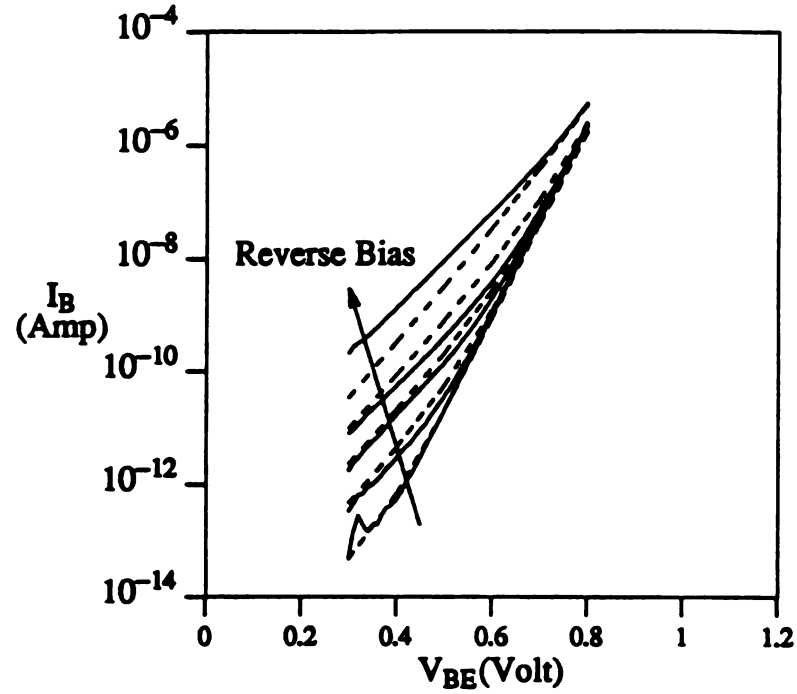


Figure 5.6: Comparison of experimental (solid lines) and simulated (dashed lines) base currents versus V_{BE} for stress times of 200 hours at stress voltages of -3.5, -4.0, -4.5, and -5.0 volts. Also shown is the initial base current characteristic.

Chapter 6

Degradation/Annealing Model for Bipolar Transistors

The study of the temperature dependence of the rate of hot electron induced degradation is presented in this chapter. The temperature dependence is discussed in view of the hot electron current densities simulated and the experimental data on degradation and post-degradation annealing. A model is developed to describe the temperature dependence of degradation and post-degradation annealing.

6.1 Hot Electron Current Simulations

The simulation of hot electron currents for different temperatures at 4 volts reverse-biased on the base-emitter junction follows the same procedure as that described in Section 5.1. The hot electron current density, J_{hot}, along the base-emitter oxide interface for the bipolar transistor is solved by using the simplified HTM model at temperatures of -75, 23, 175, and 240 C. The simulated BJT structure is the same as that described in Chapter 5.

Figure 6.1 shows the hot electron current densities versus position for temperatures of -75, 23, 175, and 240 C. The magnitude of the hot electron current density originating from the base side (hot electrons at positions less than 5.76 μm) is seen to be smaller than that from the tunneling process. In particular, at -75 C, J_{hot} is about 4 orders of magnitude smaller, while at 240 C, J_{hot} is only about 2 orders of magnitude smaller for the hot electron current originating from the base. This occurs because the minority carrier concentration is more temperature sensitive than the tunneling process. At a specific location, J_{hot} is seen to increase with increasing

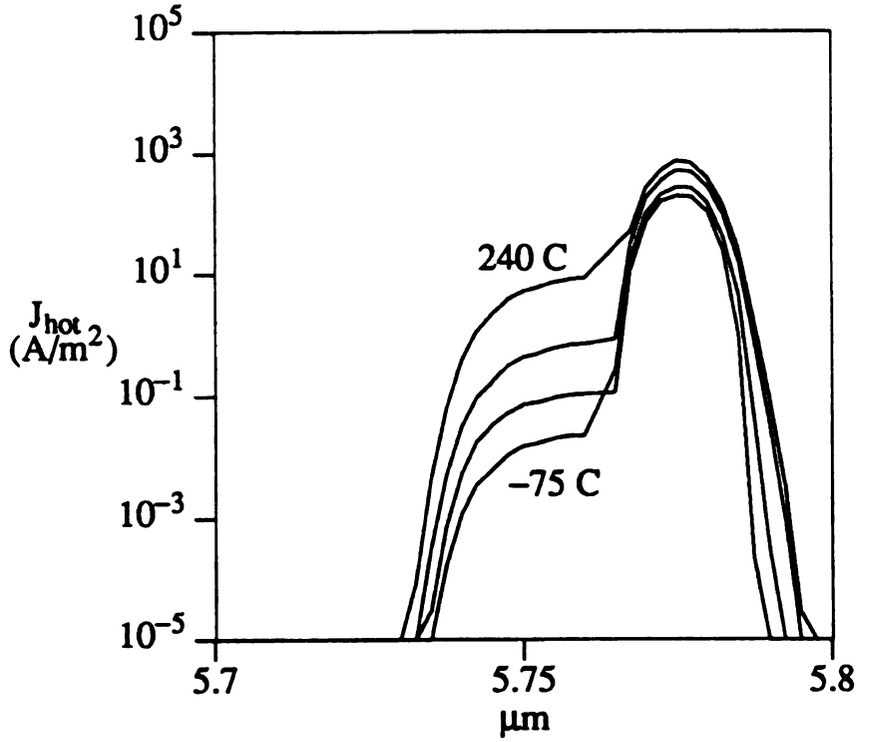


Figure 6.1: Hot electron current densities versus position for the bipolar transistors operated at -4 volts reverse bias for temperatures of -75, 23, 175, and 240 C.

temperatures. The temperature dependence of J_{hot} can be explained by examining the expression defined earlier in Chapter 5, namely,

$$J_{hot} = J_{dep} \cdot \exp(-\phi / k_B T_n) \tag{6.1}$$

where J_{dep} is the reverse bias current density and T_n is the electron temperature. The dominant reverse bias current is the band-to-band tunneling current and since the energy gap monotonically decreases with increasing temperature, the reverse bias current increases with increasing temperature resulting in the value of J_{hot} increasing. On the other hand, the electron temperature decreases with increasing ambient temperature due to the increased phonon scattering rate. This reduces the value of J_{hot}. Depending on whether the dominant change comes from the increasing reverse bias stress current or the decreasing electron temperature, the number of hot electrons capable of device damage could either increase or decrease with increasing temperature. For the TIN3 devices operated at constant reverse bias, the simulation study shows that the electron temperature has a weak dependence on the ambient temperature due to the very short depletion width and high electric fields at the emitter-base junction. For this case, the electric field plays a dominant role in determining the electron energy as shown in (3.75). Since the electric field for a constant voltage biased emitter-base junction is weakly temperature sensitive, the increase of the reverse bias current dominates over the electron temperature change and is responsible for the increase of the J_{hot} value.

In general, for advanced technology transistors where the depletion width is narrow and the electric field is strong, it is more likely that the tunneling current dominates and a larger number of hot electrons is expected at higher temperature whereas for transistors with lower doping levels (e.g. no extrinsic base region) a smaller number of hot electrons is expected at higher temperatures. In Burnett's work [15] where transistors with base doping level of 10^{14} cm^{-3} were used, a larger degradation was found for transistors stressed at 110 K than at 300 K. In Momose's work [13] which did not report the doping level of the transistors, for a temperature range of -10 to 200 C, the

degradation at 50 C was found to be larger than at -10 C. It is speculated that in [13], a higher doping level for the base diffusion was used resulting in larger degradation at 50 C. The degradation at 200 C was also seen in [13] to be smaller than at 50 C. This occurs because an additional annealing effect at higher temperatures takes place. This effect is also consistent with the degradation data in this work to be described below and previously in Chapter 2.

6.2 Degradation and Annealing Model

The hot electron current density increases with increasing ambient temperature for the transistors reverse biased at -4 volts on the emitter-base junction. The rate of degradation as described earlier in the experimental study of Chapter 2, however, is generally smaller at higher temperatures. This occurs because at higher temperatures a simultaneous annealing effects can happen such as shown in Figure 2.33 where a portion of the degraded base current can be annealed out within a very short time. The fact that the hot electron produced states are not all permanent is also indicated by the fluctuation of the base current in the short time scale stress experiment as described earlier in Section 2.4.3. Therefore, at high temperatures, even though the hot electron current creates more leakage states, more states are simultaneously removed. The overall effect is less degradation.

In order to include the phenomenon of simultaneous annealing or repassivation in a BJT degradation lifetime model, the degradation model of Burnett and Hu [9] has been extended. The model is developed by writing the degradation/annealing rate as

$$\frac{d\Delta I_B}{dt} = C_1 I_R \exp(\frac{-\phi}{k_B T_n}) g(\Delta I_B) - C_2 \Delta I_B \qquad (6.2)$$

where ΔI_B is the change in base current, $g(\Delta I_B)$ is the dependence of the degradation rate on the previous degradation, I_R is the reverse bias stress current, ϕ is the electron energy needed to produce damage, T_e is the electron temperature, and C_1 and C_2 are coefficients

that are temperature dependent. The term $g(\Delta I_B)$ is given a form $(\Delta I_B)^{-h}$ following the work of Burnett and Hu. The first term on the right side of (6.2) models the degradation process caused by hot electrons where the exponential function gives the number of hot electrons available at a given electron temperature. In this work, this corresponds to the hot electron current, $J_{hot}L_pZ_p$, where L_p is the emitter perimeter and Z_p is the maximum effective distance from the oxide-silicon interface that hot electrons can be created and still reach and damage the interface. The $C_2\Delta I_B$ term in (6.2) models the repassivation component, and it is an addition to [9]. The solution for ΔI_B is

$$\Delta I_B = \left[\frac{C_1 J_{hot}}{C_2}(1-\exp(-C_2(1+h)t))\right]^n \tag{6.3}$$

where n=1/(1+h). The L_p and Z_p quantities have been incorporated into the C_1 quantity. The role of the C_2 term is to cause a reduction in the net degradation rate as ΔI_B increases and an eventual saturation of the degradation in base current. This saturation value, $(\Delta I_B)_{sat}$, according to (6.3) is

$$(\Delta I_B)_{sat} = \left[\frac{C_1 J_{hot}}{C_2}\right]^n. \tag{6.4}$$

The application of this model to the experimental stress results is shown in Figure 6.2 which plots the base current change ΔI_B versus stress time for degradation and subsequent annealing at 240 C. Equation (6.3) contains four parameters including J_{hot}, n or h, C_1, and C_2. Of these four parameters, two of them (C_1 and n) are obtained by fitting to the degradation data shown in Figure 6.2(a). The value of J_{hot} used is the peak value of the hot electron current density obtained previously in Section 6.1. The C_2 value is obtained from the annealing data of Figure 6.2(b) by fitting the annealing data to Equation (6.2) after setting the stress current I_R to zero giving

$$\frac{d\Delta I_B}{dt} = -C_2\Delta I_B \tag{6.5}$$

Solving (6.5) gives

$$\Delta I_B = \Delta I_B(0)\exp(-C_2 t) \tag{6.6}$$

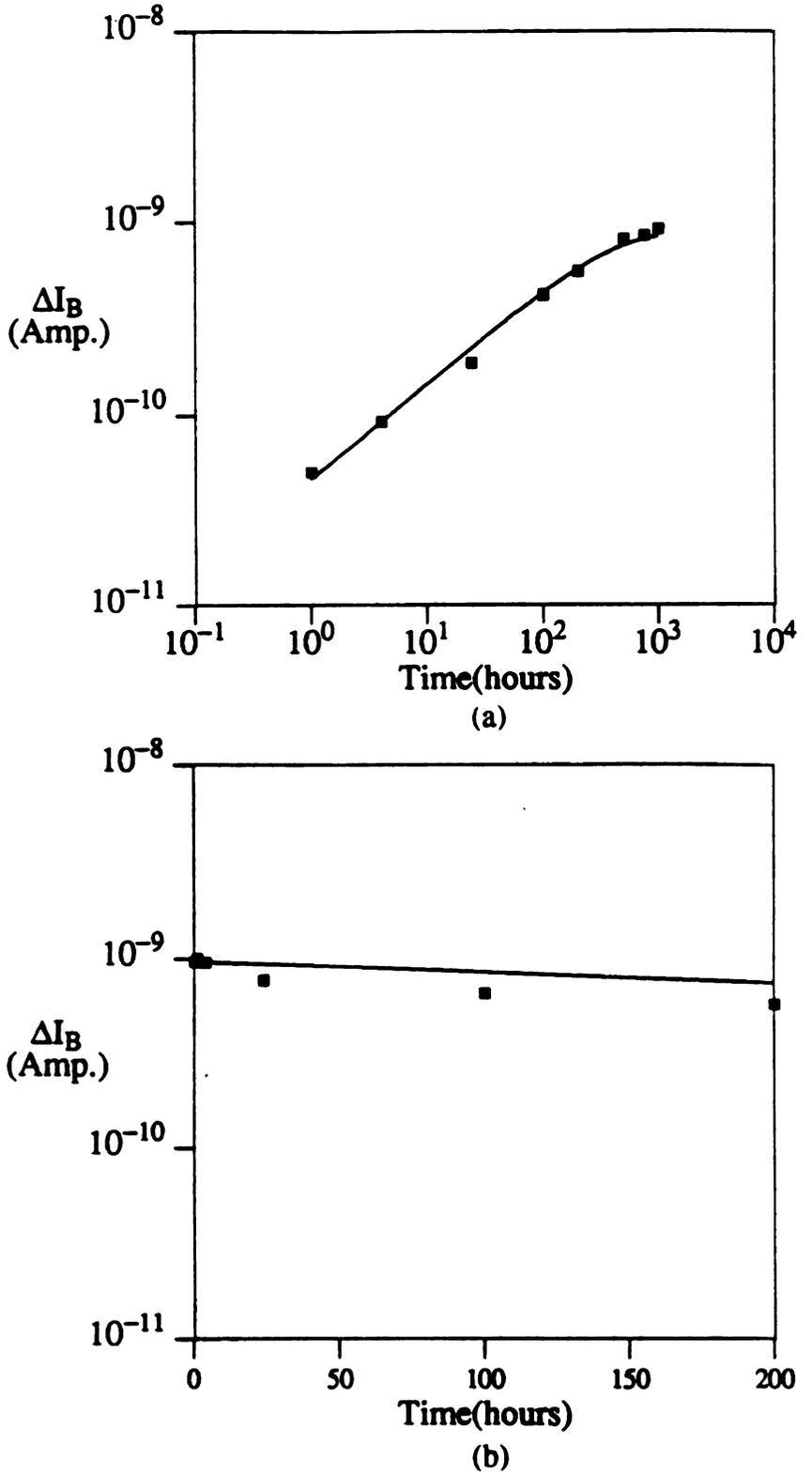


Figure 6.2: Experimental (squares) and modeled (solid line) degradation and annealing data. (a) Degradation at 240 C. (b) Annealing at 240 C.

where $\Delta I_B(0)$ is the post-degradation value of ΔI_B. The annealing data from Figure 6.2(b) gives a value of C_2=0.0014.

The fit of Equation (6.3) to the experimental data for degradation at T=240 C using the already determined J_{hot} and C_2 values gives n=0.5 and $C_1=1.4\times10^{-24}$. Specifically, when the degradation of base current versus time is plotted on a log-log scale, the data for times less than 100 hours forms a line of slope n.

6.3 Temperature Dependence

The temperature dependence of the degradation is determined by the number of hot electrons and the repassivation rate of hot electron created states. The values of n, J_{hot}, C_1, and C_2 for temperatures of -75, 23, 175, and 240 C are given in Table 6.1 with the fit of the model to the experimental data given in Figure 6.3.

J_{hot} is determined by simulating the current flow and electron energy at the various temperatures. It is significant to note that for constant voltage stressing the number of electrons with an energy above ϕ increases as the temperature is increased due to the increase in reverse bias current.

The determination of C_1 and C_2 as a function of ambient temperature requires a closer look at the annealing behavior of the degraded bipolar transistors. The annealing rate at a given annealing temperature depends on the degradation conditions used. This is illustrated in Figure 6.4 where two groups of devices were degraded at 23 C and 240 C respectively. The degradation was stopped when the base leakage current at V_{BE} = 0.6 volts had increased by 1 nanoamp. To produce this equal level of degradation the 240 C degradation took 1000 hours and the 23 C degradation took about 100 hours. The subsequent annealing of these two groups of devices at 240 C for 200 hours showed two different annealing behaviors. The 240 C degraded devices showed only a slight recovery, whereas, the 23 C degraded devices showed a substantial recovery with the largest recovery occurring almost immediately (within 1 hour) upon the initiation of the

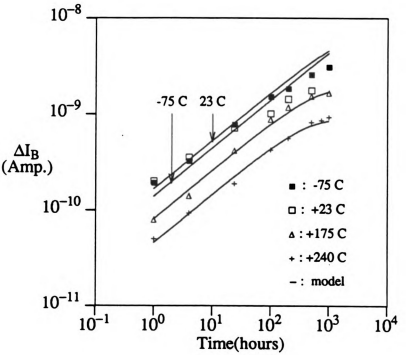


Figure 6.3: Change in base current at V_{BE} = 0.6 V versus time. The solid lines are calculated values from (6.3). The symbols are experimentally measured values.

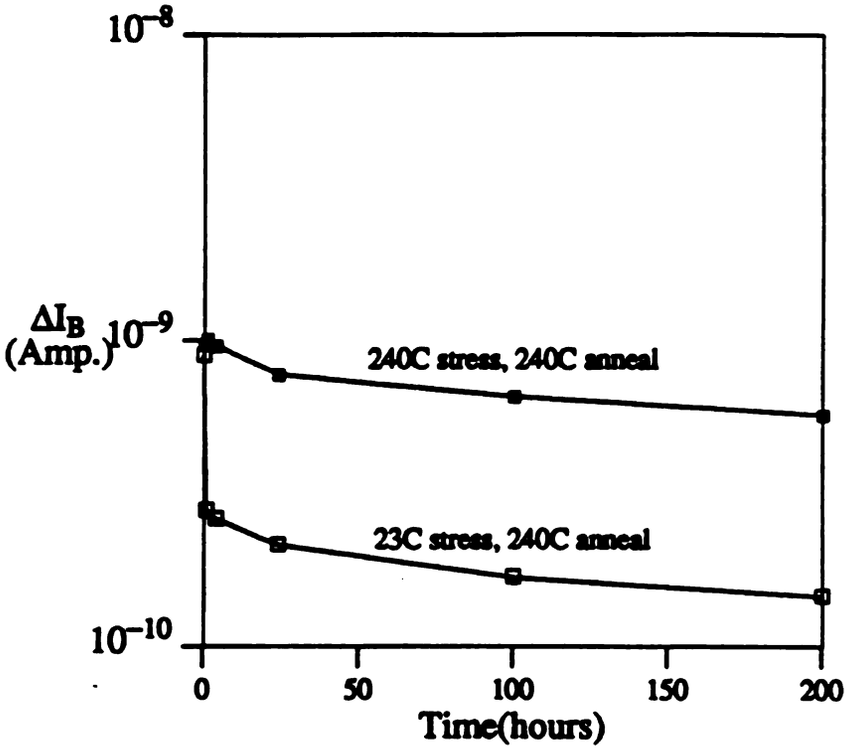


Figure 6.4: Annealing data for two groups of devices. Group 1 was degraded at 240 C for 1000 hours and group 2 was degraded at 23 C for 100 hours. ΔI_B values are for V_{BE} = 0.6 volts.

annealing process. The physical process of degradation believed to be occurring is that hot electrons are creating surface states at the silicon-silicon dioxide interface. A portion of these surface states are repassivated as seen earlier in Figure 2.26 which showed spontaneous gain recovery during the stress. It is further believed that the size of this repassivation increases as the temperature increases. Hence, net degradation at a high temperature is much slower because a large portion of the surface states are annealed out shortly after their creation. This portion of the repassivation that occurs quickly will be referred to as rapid repassivation. In Equation (6.2), the C_1 term has a temperature dependence due to the number of hot electrons given by J_{hot} and by the amount of rapid repassivation which is included by reducing C_1 as the temperature increases.

Another feature of Figure 6.4 is that after the first few hours of annealing, the annealing rate as indicated by the slope of logarithm ΔI_B versus time is similar for both the 23 C and the 240 C degraded devices. This indicates that once the rapid repassivation portion of the states have been annealed out, the annealing process proceeds in a similar manner regardless of the degradation temperature. These long time annealing observations are used to determine the value of C_2 as a function of temperature. Figure 6.5 shows the results of annealing devices at T=175 C and 240 C which were originally degraded at 23 C for 500 hours. The values of C_2 are determined by fitting the annealing data for long annealing times to

$$\Delta I_B = \Delta I_{B,slow}(0)\exp(-C_2 t) \tag{6.7}$$

which is a modification of (6.6) where $\Delta I_{B,slow}(0)$ is the post-degradation value of the slow repassivation portion of ΔI_B. The temperature dependent C_2 values are given in Table 6.1. Since no annealing is observed at -75 and 23 C, the C_2 value is negligible. An alternative model for C_2 is an activation energy relationship where $C_2 = C_{20}\exp(\frac{-E_A}{kT})$. A fit of the two measured C_2 values gives $C_{20} = 0.0134$ and $E_A = 0.10$ eV. The C_2 value is

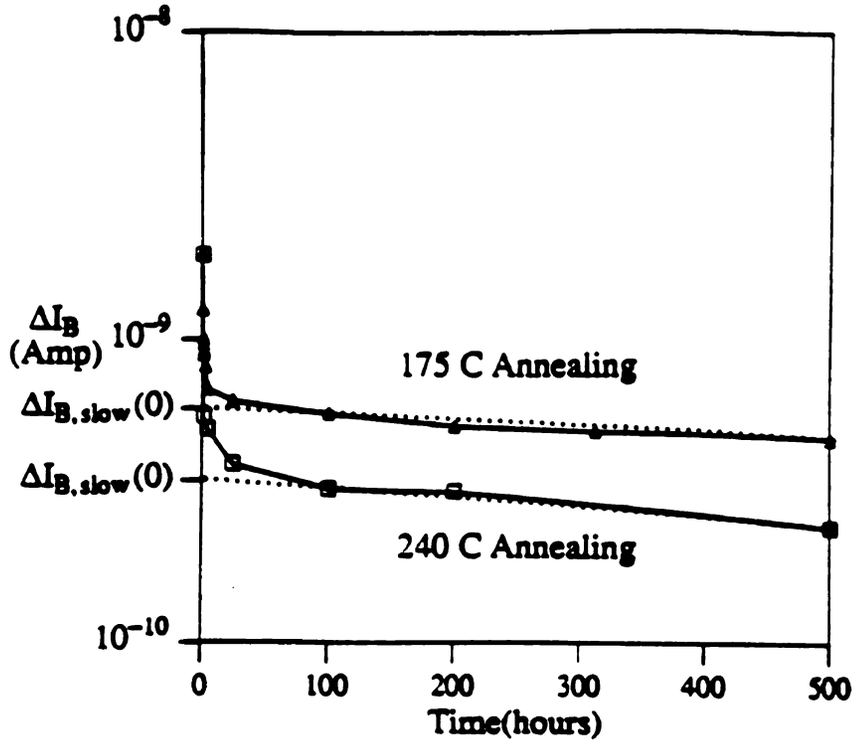


Figure 6.5: Annealing of the base current at V_{BE} = 0.6 volts versus time for the two annealing temperatures of 175 and 240 C. The symbols indicate experimental data and the dotted line is the fit of the data to (6.7). The transistors were first degraded for 500 hours at V_{BE} = -4 volts at room temperature.

T (^{o} C)	J_{hot} (A/m^{-2})	C_1 ($A.hr^{-1}$)	C_2 (hr^{-1})
-75	193.6	5.0×10^{-23}	(small)
23 C	274.5	5.0×10^{-23}	(small)
175	519.9	6.4×10^{-24}	1.0×10^{-3}
240	758.4	1.4×10^{-24}	1.4×10^{-3}

Table 6.1: Parameter values for the fitting of Equation (6.3) to the experimental data as shown in Figure 6.3.

also used to model the data in Figure 6.3. C_2 is important in determining the saturation value of the degradation as indicated by Equation (6.4). The fit at the higher temperatures of 175 C and 240 C is good, at -75 and 23 C no saturating effect is predicted by simultaneous annealing. After stressing for longer than 100 hours, both -75 and 23 C degradation rates are lower than that predicted by Equation (6.3) possibly attributed to a limit being reached at higher degradation levels in the number of interface states formed. This limiting effect was found in earlier work by Hackbarth and Tang[10].

Without the simultaneous annealing effect, the degradation rate is expected to be larger at higher ambient temperatures for transistors dominated by band-to-band tunneling in reverse bias as found in many advanced technology transistors. Including the simultaneous annealing effect, the degradation rate decreases with increasing temperatures once the annealing takes place. The overall result can then be an increasing degradation rate with temperature at lower temperatures followed by a decreasing degradation rate at higher temperatures with the maximum degradation rate corresponding approximately to the onset of simultaneous annealing. This temperature dependence is seen for the first few (time < 10 hours) data points of Figure 6.3 with the 23 C data exhibiting the largest degradation rate. In Momose's work [13], the same phenomena was measured with the peak degradation rate at a ambient temperature of 50 C.

Chapter 7

Conclusions

The degradation of bipolar transistors caused by hot electrons was investigated at room temperature for emitter-base junction reverse biases of 3.5, 4.0, 4.5, and 5.0 volts for up to 1000 hours. The degradation was also investigated at a constant reverse bias of 4 volts for temperatures of -75, 23, 175 and 240 C. The interface states created by the hot electrons provide sites for surface recombination-generation to occur leading to base surface leakage currents and a reduced current gain. For constant temperature stresses, larger voltages of reverse bias were seen to create more degradation. At a constant voltage, reverse bias stressing at higher temperatures was seen to generally cause less degradation.

The temperature dependence of the annealing of the states created was studied by using post-degradation thermal annealing experiments at a temperature range of 50 to 240 C for transistors stressed at room temperature and at 240 C. The states removed by the thermal annealing were found to be distinguishable into fast and slow repassivation components with the fast component being easily annealed out and the slow component being resistive to annealing. The ratio of these two components was found to be very temperature sensitive, i.e., a larger portion of the interface states for the fast repassivation component at a higher temperature.

Short time scale stress experiments were conducted to examine the lifetime of the states created by hot electrons. The results showed fluctuations of the base current indicating the hot electron created states were not all permanent. AC experiments for 50% reverse bias stress cycling time only and for 50% reverse and 50% forward cycling time were performed. The transistors stressed with forward bias cycles showed less

degradation indicating the removal of hot electrons created states by the forward bias applied voltage.

In order to solve for the reverse bias stress conditions, a band-to-band tunneling model was implemented into a device simulation program developed for this study. The hot electron current density was calculated by a simplified Hydrodynamic Transport Model (HTM) and related to the interface states created in a spatially dependent, microscopic fashion. The increase of the surface recombination velocity due to the increase of interface states was taken into account by a two-dimensional device simulation program to predict the base leakage current.

The device level band-to-band tunneling was implemented by an electron and hole generation rate model calculated based on the band bending and electric field information. The reverse bias stress current predicted by the band-to-band tunneling model was in good agreement with the measured data. The band-to-band tunneling mechanism provides a microscopic view for the behavior of the tunneling electrons under reverse bias stress conditions.

HTM and the drift-diffusion (DD) model simulations were done for the reverse bias stress conditions. The results were compared and no significant difference was observed in the I-V characteristics. The conclusion is that the energy conservation equation can be decoupled from the full HTM model for reverse-biased junctions with sufficiently low current densities. A simplified HTM model is proposed which is based on a decoupled solution of the DD model and the energy conservation equation. This model predicts the electron energy under various reverse bias stress conditions.

In order to analyze the magnitude and location of hot electron generation, a hot electron current density, J_{hot}, was proposed which conveniently represents the number of hot electrons passing a local region per unit time above a threshold damage energy. J_{hot} is the portion of the total electron current density that is responsible for the device interface state creation. The hot electron current densities were solved for these stress conditions,

namely, for reverse biases of 3.5, 4.0, 4.5, and 5.0 volts at 23 C, and for a 4 volt reverse bias at temperatures of -75, 23, 175, and 240 C. Comparisons were made for the magnitude of the hot electron current densities originating from the base side and from the tunneling process. The results showed that the majority of the hot electrons originate from the tunneling process indicating the importance of including band-to-band tunneling process into the reverse bias calculations. For the constant voltage-different temperature stresses, the hot electron current densities were found to be increasing with increasing ambient temperatures. This phenomena was caused by the more rapid increase of the tunneling rate as compared to the decrease of the electron temperature as the ambient temperature increases.

For higher temperatures of reverse bias stressing, an additional annealing effect was found to take place which removes some of the interface states created by hot electrons. This phenomena was studied by using the hot electron current density simulations and the post-degradation annealing experiments. Despite the larger hot electron current density at higher temperatures, a simultaneous annealing removed many states created by the hot electrons resulting in a smaller degradation rate at higher temperatures. The degradation/annealing model developed in this study extends the degradation model developed by Burnett and Hu and includes the saturation of the degradation and the simultaneous degradation/annealing effect not accounted for in previous models.

By using the hot electron current density simulated and a surface recombination velocity model, the degraded characteristics and subsequent device lifetime of bipolar transistors can be determined. The model can be applied in the prediction of the device lifetime due to hot electron induced degradation as the geometry, doping profile, temperature, and stressing/operating conditions are varied.

Appendix A

Discretization of J and S in Scharfetter-Gummel Form

Discretization of J:

The discretization of the electron and hole current densities starts with the expression for electron current density [46],

$$J = qn\mu(T)E + k_B n\mu(T)\frac{dT}{dx} + k_B T\frac{d(n\mu(T))}{dx} \quad (A1)$$

Or, (A1) can be rearranged as

$$k_B T(x)\frac{d(n\mu(T))}{dx} + \left[n\mu(T)(qE + k_B\frac{dT}{dx}\right] = J \quad (A2)$$

Assuming E, $\frac{dT}{dx}$, and J are all constants across the spacing between grid points, (A2) can be written as

$$\frac{d(n\mu(T))}{dx} + \frac{n\mu(T)(qE + k_B\frac{dT}{dx})}{k_B T(x)} = \frac{J}{k_B T(x)} \quad (A3)$$

From a general mathematical handbook [55], the solution of (A3) is

$$n\mu(T)\exp(\int_{x_i}^{x_{i+1}} \frac{qE + \frac{k_B dT}{dx}}{k_B T(x)}dx)$$

$$= \int_{x_i}^{x_{i+1}} \frac{J}{k_B T}\exp(\int_{x_i}^{x_{i+1}} \frac{qE + \frac{k_B dT}{dx}}{k_B T(x)}dx)dx + C \quad (A4)$$

The left hand and right hand sides of (A4) can be solved to become

$$\text{LHS} = n\mu(T)e^{(qE+k_B\frac{dT}{dx})\int_{x_i}^{x_{i+1}}\frac{\frac{1}{T}\frac{dT}{dx}}{k_B\frac{dT}{dx}}}$$

$$= n\mu(T)e^{(qE+k_B\frac{dT}{dx})\ln(T)\frac{1}{k_B dT/dx}}$$

$$= n\mu(T)\left[e^{\ln(T)}\right]^{(qE+k_B\frac{dT}{dx})\frac{1}{k_B dT/dx}}$$

$$= n\mu(T)T^{\alpha+1} \qquad \text{(A5)}$$

where

$$\alpha = \frac{qE}{k_B dT/dx} \qquad \text{(A6)}$$

and

$$\text{RHS} = \frac{J}{k_B}\int_{x_i}^{x_{i+1}}\frac{1}{T}T^{\alpha+1}dx$$

$$= \frac{J}{k_B}\int_{x_i}^{x_{i+1}}T^{\alpha}\frac{dT/dx}{dT/dx}dx$$

$$= \frac{J}{k_B dT/dx}\frac{T^{\alpha+1}}{\alpha+1}\Bigg|_{x_i}^{x_{i+1}} . \qquad \text{(A7)}$$

Hence, (A4) is now expressed as

$$n\mu(T)T^{\alpha+1}\Big|_{x_i}^{x_{i+1}} = \frac{J}{k_B dT/dx}\frac{T^{\alpha+1}}{\alpha+1}\Bigg|_{x_i}^{x_{i+1}} \qquad \text{(A8)}$$

Rearranging (A8) yields

$$J = k_B\frac{dT}{dx}(\alpha+1)\frac{[n\mu(T)]_{i+1}T_{i+1}^{\alpha+1} - [n\mu(T)]_i T_i^{\alpha+1}}{T_{i+1}^{\alpha+1} - T_i^{\alpha+1}} \qquad \text{(A9)}$$

In the expression of (A6), α is discretized to be

$$\alpha_m = -\frac{q(\psi_{i+1} - \psi_i)}{k_B(T_{i+1} - T_i)} . \qquad \text{(A10)}$$

Using (A10), (A9) can be written as

$$J_m = \left[-\frac{q(\psi_{i+1} - \psi_i)}{x_{i+1} - x_i} + \frac{k_B(T_{i+1} - T_i)}{x_{i+1} - x_i} \right] \cdot \frac{[n\mu(T)]_{i+1} e^{(\alpha_m+1)\ln(T_{i+1}/T_i)} - [n\mu(T)]_i}{e^{(\alpha_m+1)\ln(T_{i+1}/T_i)} - 1} \quad \text{(A11)}$$

(A11) can be simplified by the use of Bernoulli functions given by

$$\frac{e^{-x}}{e^{-x} - 1} = -\frac{1}{x} B(x) \quad \text{(A12)}$$

$$\frac{1}{e^{-x} - 1} = -\frac{1}{x} B(-x) \quad \text{(A13)}$$

where B(x) is defined as

$$B(x) = \frac{x}{e^x - 1} \quad \text{(A14)}$$

Using (A12) to (A14), (A11) can then be expressed as

$$J_m = \left[-\frac{q(\psi_{i+1} - \psi_i)}{x_{i+1} - x_i} + \frac{k_B(T_{i+1} - T_i)}{x_{i+1} - x_i} \right] \cdot \frac{[n\mu(T)]_i B(-\theta) - [n\mu(T)]_{i+1} B(\theta)}{\theta} \quad \text{(A15)}$$

where θ represents

$$\theta = -(\alpha_m + 1)\ln(T_{i+1} / T_i) \quad \text{(A16)}$$

and α_m is given by

$$\alpha_m = -\frac{q(\psi_{i+1} - \psi_i)}{k_B(T_{i+1} - T_i)} \quad \text{(A17)}$$

(A15) is the discretized expression for the electron current density. For the hole current density, similar expression can be derived following the same procedures. Note, however, that if one substitutes E by -E, multiplies J by -1, and changes the electron mobility to hole mobility the electron current density expression (A11) transforms to that of the hole current density expression.

Discretization of S:

The discretization of electron and hole energy density flux starts with the expression for electron energy density flux [46]

$$S = -k(T)\frac{dT}{dx} - J\delta(T)k_B\frac{T}{q} \quad (A18)$$

By using the Wiedemann-Franz relation,

$$\frac{k(T)}{qn\mu(T)} = \left(\frac{k_B}{q}\right)^2 \Delta(T)T \quad (A19)$$

and substituting (A1), (A18) can be expressed as

$$\begin{aligned} S = &-\left(\frac{k_B}{q}\right)^2 \Delta(T)qn\mu(T)T\frac{dT}{dx} \\ &- qn\mu(T)E\delta(T)k_B\frac{T}{q} \\ &- k_BT\frac{d(n\mu(T))}{dx}\delta(T)k_B\frac{T}{q} \\ &- k_Bn\mu(T)\frac{dT}{dx}\delta(T)k_B\frac{T}{q} \end{aligned} \quad (A20)$$

Or, after rearranging terms, (A20) is written as

$$\begin{aligned} &\frac{k_B^2T^2}{q}\delta(T)\frac{d[n\mu(T)]}{dx} + \\ &\left[k_B\delta(T)E + \frac{k_B^2}{q}(\Delta(T) + \delta(T))\frac{dT}{dx}\right]n\mu(T)T = -S \end{aligned} \quad (A21)$$

(A21) can be further rearranged to be

$$\frac{d[n\mu(T)T]}{dx} + [n\mu(T)T]\left(\frac{qE + \frac{k_B\Delta(T)}{\delta(T)}\frac{dT}{dx}}{k_BT}\right) = -\frac{S}{\frac{k_B^2\delta(T)T}{q}} \quad (A22)$$

(A22) and (A3) are in similar forms. Equation (A22) can be developed parallel to that of the discretization of J described in the above section, i.e., let

$$\alpha_m = -\frac{q(\psi_{i+1} - \psi_i)}{T_{i+1} - T_i} \quad (A23)$$

and one obtains the discretized electron energy density flux as

$$S_m = -\frac{k_B\delta(T)}{q}\left[-\frac{q(\psi_{i+1}-\psi_i)}{x_{i+1}-x_i}+\frac{\frac{\Delta}{\delta}k_B(T_{i+1}-T_i)}{x_{i+1}-x_i}\right]\cdot$$
$$\left[\frac{[n\mu(T)T]_{i+1}\exp[(\alpha_m+\frac{\Delta}{\delta})\ln(T_{i+1}/T_i)]-[n\mu(T)T]_i}{\exp[(\alpha_m+\frac{\Delta}{\delta})\ln(T_{i+1}/T_i)]-1}\right] \quad \text{(A24)}$$

Similarly, for holes, the energy flow can be written as

$$S_p = -k(T)\frac{dT_p}{dx}+J_p\delta(T)\frac{k_BT_p}{q} \quad \text{(A25)}$$

Parallel to that of developing electron energy flow discretization equation, i.e. substitute the Wiedemann-Franz relation and the expression of J_p,

$$J_p = qp\mu E - k_BT\frac{d(p\mu)}{dx} - k_Bp\mu\frac{dT}{dx} \quad \text{(A26)}$$

S_p can be expressed as

$$S_p = -\left(\frac{k_B}{q}\right)^2\Delta(T)qp\mu(T)T\frac{dT}{dx}$$
$$+qp\mu(T)E\delta(T)k_B\frac{T}{q}$$
$$-k_BT\frac{d(p\mu(T))}{dx}\delta(T)k_B\frac{T}{q}$$
$$-k_Bp\mu(T)\frac{dT}{dx}\delta(T)k_B\frac{T}{q} \quad \text{(A27)}$$

Comparing (A27) to (A20), it is seen that the discretized form of hole energy flux can be obtained by a simple substitution of E by -E, n by p, and electron mobility by hole mobility in the expression for electron energy flux.

Appendix B

Input File Description for Device Simulation Program

The input file specification for this device simulation program is described in this appendix. The input file must be saved as the file name 'input' and within the input file, the entries are case-sensitive, i.e., upper case and lower case should be distinguished. The simulation program first executes various data input subroutines to provide necessary information before it can performed the simulation. The program reads one 80 character line at a time, analyzes the first three letter, decides what information is contained in the next few lines and reads the appropriate informations. Typically, the first three letters are in upper case and acts like a command to the program. The program then appropriately reads the next few lines which have the information data to be loaded or executed. Empty lines are allowed in the input file to separate the commands and information data. The empty lines are simply ignored. The following lists the allowed commands and the appropriate information data:

COM

syntax COM<arbitrary user input characters>

description The comment line is used to let the user put some comments in the line. The program does nothing with the line.

example COMMENT : This is the structure used in the research.

COM The extrinsic base doping profile:

GRD

syntax GRD<arbitrary user input>

<yline number> <ylocation> <yratio>

<yline number> <ylocation> <yratio>

....

999 0.0 0.0

<xline number> <xlocation> <ylength>

<xline number> <xlocation> <ylength>

....

999 0.0 0.0

description The GRD command first reads y meshes specifications (horizontal mesh line) then reads x meshes (vertical mesh line). The simulation program reads in the line number and than the location. The ratio is the ratio between the distances between the adjacent lines. The program will automatically determine the distance between the lines to satisfy the ratio specification. Horizontal mesh lines are layout from boundary to boundary; while vertical mesh lines can be terminated according to the specified ylength value. The program will automatically determine the suitable terminating point (i.e. not violating the rules of having two termination point in one segment of line).

example The grid layout in Figure B.1 is done by the following input entries:

GRD this grid will produce Figure B.1

10 1.0 1.0

999 0.0 0.0

15 1.0 0.8 0.5

30 2.0 1.2 1.0

999 0.0 0.0

CON

syntax CON<arbitrary user input>

<contact number> <contact type> <xmin> <xmax> <ymin> <ymax>

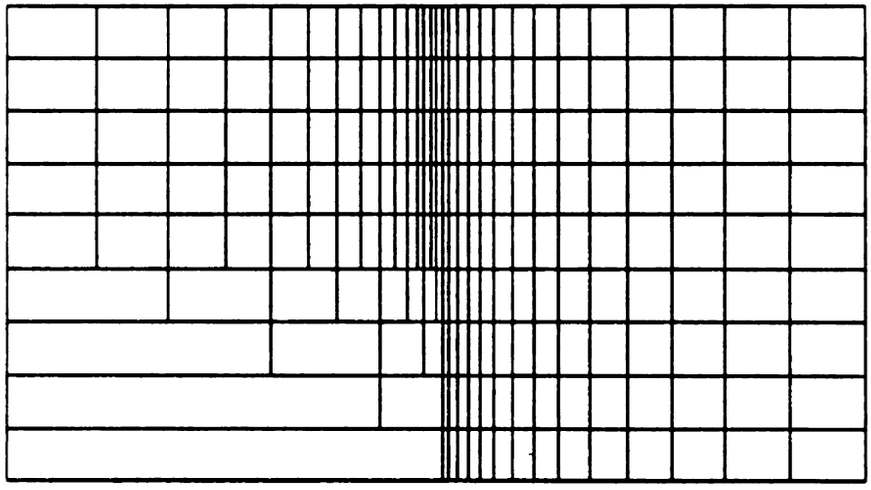


Figure B.1: An example layout of grid structure.

description The contact is specified by the contact number and its locations. So far, the only contact type supported is 'ohm', the ohmic contact.

example The following contact specification put contacts 1 and 2 on top and bottom surfaces of Figure B.1:

CON

1 ohm 0.0 2.0e-6 0.0 0.0

2 ohm 0.0 2.0e-6 1.0e-6 1.0e-6

UNI

syntax UNI<arbitrary user input characters>

<impurity type> <concentration> <xmin> <xmax> <ymin> <ymax>

description The uniform doping concentration are specify by this entry for its impurity type (either 'nd' or 'na'), concentration magnitude (in m^{-3}), and the region enclosed by xmin, xmax, ymin, ymax.

example UNI

nd 1.9e22 0.0 1.0e-6 0.0 0.1e-6

GAX

syntax GAX

<impurity type> <peak location> <peak concentration> <xchar> <ychar> <ymin> <ymax>

description GAX specifies the Gaussian profile along the x direction according to the following relationship

$$\text{ymin} < y < \text{ymax} \qquad N(x,y) = N_o e^{-\left(\frac{x-x_o}{x_c}\right)^2} \qquad \text{(B1)}$$

$$y < \text{ymin} \qquad N(x,y) = N_o e^{-\left(\frac{x-x_o}{x_c}\right)^2\left(\frac{y-y\min}{y_c}\right)^2} \qquad \text{(B2)}$$

$$y > \text{ymax} \qquad N(x,y) = N_o e^{-\left(\frac{x-x_o}{x_c}\right)^2\left(\frac{y-y\max}{y_c}\right)^2} \qquad \text{(B3)}$$

where N_o is the peak concentration, x_o is the location of the peak concentration, and x_c and y_c are the characteristic lengths in the x and y directions.

example GAX

nd 0.0 2.0e24 0.1e-6 0.1e-6 0.1e-6 0.2e-6

GAY

syntax GAY

<impurity type> <peak location> <peak concentration> <xchar> <ychar> <xmin> <xmax>

description GAY specifies the Gaussian profile along the y direction according to the following relationship

$$xmin < x < xmax \qquad N(x,y) = N_o e^{-(\frac{y-y_o}{y_c})^2} \qquad (B4)$$

$$x < xmin \qquad N(x,y) = N_o e^{-(\frac{y-y_o}{y_c})^2(\frac{x-xmin}{x_c})^2} \qquad (B5)$$

$$x > xmax \qquad N(x,y) = N_o e^{-(\frac{y-y_o}{y_c})^2(\frac{x-xmax}{x_c})^2} \qquad (B6)$$

where N_o is the peak concentration, y_o is the location of the peak concentration, and x_c and y_c are the characteristic lengths in the x and y directions.

example GAY

nd 0.0 2.0e24 0.1e-6 0.1e-6 0.1e-6 0.2e-6

FIY

syntax FIY<arbitrary user input characteristics>

<Impurity type> <xmin> <xmax> <ymin> <ymax> <lateral diffusion> <C_1> <C_2> <C_3> <C_4> <C_5> <C_6> <C_7> <C_8> <C_9> <C_{10}>

description FIY specifies an arbitrary shape doping profile along the y direction. The doping profile is specified by interconnecting the C_i values along equal

spacing points in the y direction from ymin to ymax. A lateral diffusion specifies the lateral diffusion length as reference to the vertical diffusion length (e.g. 0.6 for 60% lateral diffusion length of the vertical diffusion length). Figure B.2 shows an example of the use of FIY. The vertical and lateral diffusion profile are also shown.

example The following generates the extrinsic base doping of Figure 2.4:

FIY

na 0.0 5.575e-6 0.0 0.9e06 0.6

4.3e24 4.0e24 3.21e24 2.23e24 1.34e24 6.92e23 3.1e23 1.2e23 4.01e22 1.16e22

MET

syntax MET<arbitrary user input characters>

<imax> <iinfo> <infile> <imeshonly> <ibgn> <inter> <stress time> <itun> <tunrange> <temperature> <C> <n_1> <n_2>

description MET specifies the solution parameters that can be controlled in the input file. These parameters are described below:

<imax> : the maximum iteration count that can be performed by the program. The value is set to limit the iteration when the solution is diverging. When the iteration count of the solution exceeds the <imax> number and no convergence is reached, the solution at that point will be saved into a file 'diverg.dat', and the whole simulation is aborted for the user to examine the problem of divergence.

<iinfo> : = 0 or 1. If iinfo is one, load the information file 'devinfo'. 'devinfo' stores the necessary information about the device such that the simulation can simply load the file and start the solution. 'devinfo' includes the doping profile, the data structure of the point assignment scheme, the location of the rows and columns, the

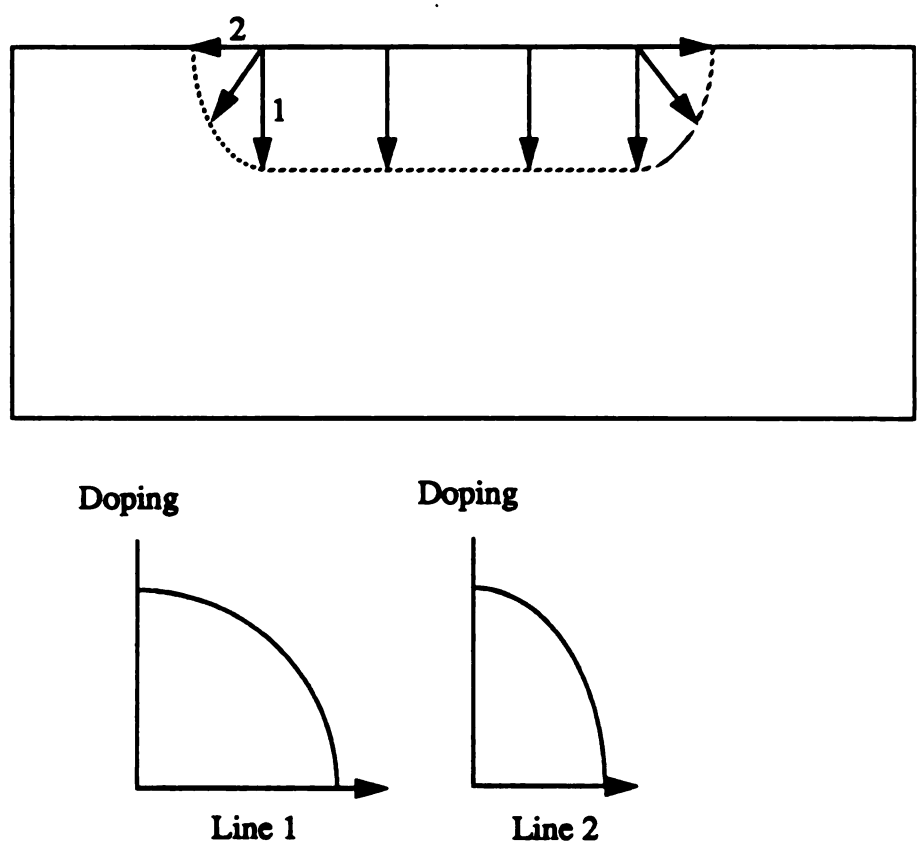


Figure B.2: The doping profile specified by the use of FIY command.

results of the L/U matrix after symbolic LU decomposition etc. If iinfo = 0, the device simulation program first reads the necessary informations (doping, mesh, etc.) and then saves the information into 'devinfo' and starts the solution iteration.

<infile> : The device simulation program can import previous solutions as the initial condition. If <infile> is 'no', no importing of previous solutions; otherwise, the device simulator reads the file name specified in <infile>.

<imeshonly> : If <imeshonly> = 1, the device simulator only reads the doping information and saves it to file 'meshndop'. This option is used when the user only wishes to repeatedly check the doping profile and not solving any symbolic LU decomposition. If <imeshonly> = 0, this option is disabled.

<ibgn> : use 1 to include bandgap narrowing effect; otherwise, use 0.

<inter> : This option is used for the easy extraction of top surface properties. <inter> = 0, this option is disabled. <inter> = 2, the simulator will import the file 'hot.d' into the device simulation and calculate the corresponding surface recombination velocity.

<stress time> : The value of stress time described in Equation (5.5).

<itun> : <itun> = 1, the tunneling mechanism is turned on.

<tunrange> : Typically for two grid points having a long distance between them, the tunneling current can be negligibly small. The simulator checks the distance between any two points, if they are larger than tunrange, the calculation for tunneling current is skipped.

<temperature> : The ambient temperature (lattice temperature) for the simulation.

<C> : is used when calculating corresponding surface recombination velocity calculation as describe in Equation (5.5).

<n_1> : is the fitting parameter adjusting the time dependence of surface recombination velocity used in Equation (5.5).

<n_2> : is the fitting parameter adjusting the voltage dependence of surface recombination velocity used in Equation (5.5).

example The entries below specify that the maximum iteration can be no more than 200, don't load from 'devinfo', don't import an initial solution, mesh-only option is turned off, include bandgap narrowing effect, disable interface property extraction, tunneling current mechanism is turn on with the range set at 0.1 μm, the lattice temperature is 296 K, C=3.8, n_1=0.35, and n_2=0.8:

MET imax;info;infile;imesh;bgn;int;time;tun;tunr;temp;C;n1;n2

200 0 'no' 0 1 0 0.0 1 0.1 296.0 3.8 0.35 0.8

SOL

syntax SOL<arbitrary user input characters>

<solution number> <model> <V1> <V2> (<V3>) <error> <output file>

<solution number> <model> <V1> <V2> (<V3>) <error> <output file>

...

999 pois 0.0 0.0 1.0e-6 no (Or, 999 pois 0.0 0.0 0.0 1.0e-6 no)

description The entries below SOL specify the solutions to be performed. <solution number> specifies the number of the solution, and is began from 1. <model> is either 'pois' for Poisson solution, 'drdi' for Drift-Diffusion solution, or 'entr' for Hydrodynamic Transport Model solution. The details for the algorithm of these solution methods will be described in Appendix C. <V1>, <V2>, and <V3> specify the voltage on the contacts. Typically

<V1> is the reference potential and must be zero. If the input file specifies 3 contacts in the CON block, V3 must be specified. If the input file specifies only 2 contacts, no V3 can present. <error> specifies the error criterion of the solution iteration; when the updates of the solution results in a value smaller than the criterion, a convergence is considered reached. Finally, if the solution is to be saved in a file, specify the file name in <output>. If <output> = 0, no solution is saved. When all solutions are performed and 999 is reached, the simulation process is considered successful and the program completed.

example The following entries solve for a Poisson solution as the initial condition and then solves for V1 = 0 and V2 = 0.1 volts by using Drift-Diffusion model. The results are saved in a file called 'dr01':

```
SOL
1 pois 0.0 0.0 1.0e-6 no
2 drdi 0.0 0.1 1.0e-6 dr01
999 pois 0.0 0.1 1.0e-6 no
```

END

syntax END

description END specifies the end point that the simulator will be examining, i.e., any input pass this point will simply be ignored by the simulator.

example

```
END
one can store anything here since
anything here will never be seen by the device simulator.
```

In the following, two example input files are listed. The first file was used in the reverse bias simulation that extracted the solution at 4 volts of reverse bias at an ambient

temperature of -75 C. The second file was used in the forward degraded characteristic calculation for a stress time of 1 hour.

Example input files:

```
COMMENT ::: The first input file
COMMENT ::: This is a doping profile for a TIN3 bjt
COMMENT ::: used for reverse bias study

GRD :::
10 0.4 1.0
999 0.0 0.0
15 5.5 1.0 1.4
20 5.625 1.0 1.4
120 5.875 1.0 1.4
135 8.5 1.0 1.4
999 0.0 0.0 0.0

COMMENT ::: Contact spec:

CON
1 ohm 0.0 2.8d-6 0.0 0.0

CON
2 ohm 6.0d-6 8.5d-6 0.0 0.0

COMMENT ::: Extrinsic Base doping:

FIY
na 0.00e-6 5.575e-6 0.0 0.9e-6 0.6
4.30e24 4.0e24 3.21e24 2.23e24 1.34e24 6.92e23 3.1e23 1.2e23 4.01e22 1.16e22

COMMENT ::: Intrinsic Base doping:

GAY
na 0.2e-6 2.0e24 1e-6 0.135e-6 0.0 8.5e-6

GAY
na 0.49e-6 4.0e23 1e-6 0.076e-6 0.0 8.5e-6

GAY
na 0.60e-6 2.0e23 1e-6 0.075e-6 0.0 8.5e-6
```

```
GAY
na 0.7e-6 8.0e22 1e-6 0.14e-6 0.0 8.5e-6

COMMENT ::: Emitter doping:

FIY
nd 6.0e-6 8.5e-6 0.0 0.45e-6 0.6
3.31e26 3.1e26 2.52e26 2.07e26 1.77e26 1.37e26 8.44e25 2.58e25 2.61e24 8.55e22


MET :::Imax,iinfo,infile,imesh,ibgn,inter,stt,itun,tunr,temp,c,n1,n2
200 0 'no' 0 1 0 0.0 1 0.1 198.0 3.8 0.35 0.8

SOL ::: No. : model : V1 : V2 : (V3) : erri : outfile
1 pois 0.0 0.0 1.0e-6 no
2 drdi 0.0 0.2 1.0e-6 no
3 drdi 0.0 0.4 1.0e-6 no
4 drdi 0.0 0.6 1.0e-6 no
5 drdi 0.0 0.8 1.0e-6 no
6 drdi 0.0 1.0 1.0e-6 no
7 drdi 0.0 1.2 1.0e-6 no
8 drdi 0.0 1.4 1.0e-6 no
9 drdi 0.0 1.6 1.0e-6 no
10 drdi 0.0 1.8 1.0e-6 no
11 drdi 0.0 2.0 1.0e-6 no
12 drdi 0.0 2.2 1.0e-6 no
13 drdi 0.0 2.4 1.0e-6 no
14 drdi 0.0 2.6 1.0e-6 no
15 drdi 0.0 2.8 1.0e-6 no
16 drdi 0.0 3.0 1.0e-6 no
17 drdi 0.0 3.2 1.0e-6 no
18 drdi 0.0 3.4 1.0e-6 no
19 drdi 0.0 3.5 1.0e-6 no
20 drdi 0.0 3.8 1.0e-6 no
21 drdi 0.0 4.0 1.0e-6 dr_40
999 pois 0.0 0.0 1.0e-3 no

END


COMMENT ::: The second input file.
COMMENT ::: This is a doping profile for a TIN3 bjt
COMMENT ::: used in forward degraded char. simulation

GRD :::
20 1.4 1.0
```

```
999 0.0 0.0
16 2.625 1.0 1.4
116 2.875 1.0 1.4
121 3.0 1.0 1.4
135 8.5 1.0 1.4
999 0.0 0.0 0.0

COMMENT ::: Contact spec:

CON
1 ohm 0.0d-6 2.8d-6 0.0 0.0

CON
2 ohm 6.0d-6 8.5d-6 0.0 0.0

CON
3 ohm 0.0 8.5d-6 1.4d-6 1.4d-6

COMMENT ::: Collector doping:

UNI
nd 1.9e22 0.0 8.5e-6 0.0 1.4e-6

GAY
nd 1.4e-6 2.3e25 1e-6 0.206e-6 0.0 8.5e-6

COMMENT ::: Extrinsic Base doping:

FIY
na 0.00e-6 5.575e-6 0.0 0.9e-6 0.6
4.30e24 4.0e24 3.21e24 2.23e24 1.34e24 6.92e23 3.1e23 1.2e23 4.01e22 1.16e22

COMMENT ::: Intrinsic Base doping:

GAY
na 0.2e-6 2.0e24 1e-6 0.135e-6 0.0 8.5e-6

GAY
na 0.49e-6 4.0e23 1e-6 0.076e-6 0.0 8.5e-6

GAY
na 0.60e-6 2.0e23 1e-6 0.075e-6 0.0 8.5e-6

GAY
na 0.7e-6 8.0e22 1e-6 0.14e-6 0.0 8.5e-6
```

```
COMMENT ::: Emitter doping:

FIY
nd 6.0e-6 8.5e-6 0.0 0.45e-6 0.6
3.31e26 3.1e26 2.52e26 2.07e26 1.77e26 1.37e26 8.44e25 2.58e25 2.61e24 8.55e22

MET :::Imax,iinfo,infile,imesh,ibgn,inter,stt,itun,tunr,temp,c,n1,n2
200 0 'no' 0 1 0 1.0 0 0.1 300.0 3.8 0.35 0.8

SOL ::: No. : model : V1 : V2 : (V3) : erri : outfile
1 pois 0.0 0.0 0.0 1.0e-6 no
2 drdi 0.0 0.0 0.0 1.0e-6 no
3 drdi 0.0 0.1 0.1 1.0e-6 no
4 drdi 0.0 0.2 0.2 1.0e-6 no
5 drdi 0.0 0.3 0.3 1.0e-6 no
6 drdi 0.0 0.4 0.4 1.0e-6 no
7 drdi 0.0 0.5 0.5 1.0e-6 no
8 drdi 0.0 0.6 0.6 1.0e-6 no
9 drdi 0.0 0.7 0.7 1.0e-6 no
10 drdi 0.0 0.8 0.8 1.0e-6 no
999 pois 0.0 0.0 0.0 1.0e-3 no

END
```

Appendix C

Device Simulation Program Structure Outline

The device simulation program consisted of about 60 subroutines in about 6,000 lines of FORTRAN language and is structured into the algorithm shown in Figure C.1. The program starts by reading the input file to decide important options such as whether to read an initial solution, whether only to layout the mesh, whether to read the preprocessed informations, etc.

If the input files specifies 'do the preprocess step', the procedure does the symbolic LU decomposition and saves the result in 'devinfo', etc. Otherwise, this step can be skipped by simply loading from the file 'devinfo'.

The next step is to read from the input file the contact voltages. The program then proceeds to solving the Poisson, electron continuity, hole continuity, electron energy conservation, and hole energy conservation equations. The Poisson solution only involves iteratively solving the Poisson equation, whereas the Drift-Diffusion solution iteratively solves the Poisson, electron continuity, and hole continuity equations, and the HTM solution solves the Poisson, electron continuity, hole continuity, electron energy conservation, and hole energy conservation equations.

After each iteration, all the updates in the solution are examined. If all updates are smaller than the error criterion specified, the solution is considered to be converged. The program than proceeds to the output handling (saving output), and deciding whether to go to the next solution. If any of the updates are larger than the error criterion, the solution is iterated with the new solution as the initial condition.

The following lists the main subroutines for each of the function blocks:

Read Input File: readdop.f, readmesh.f, readcon.f, param.f

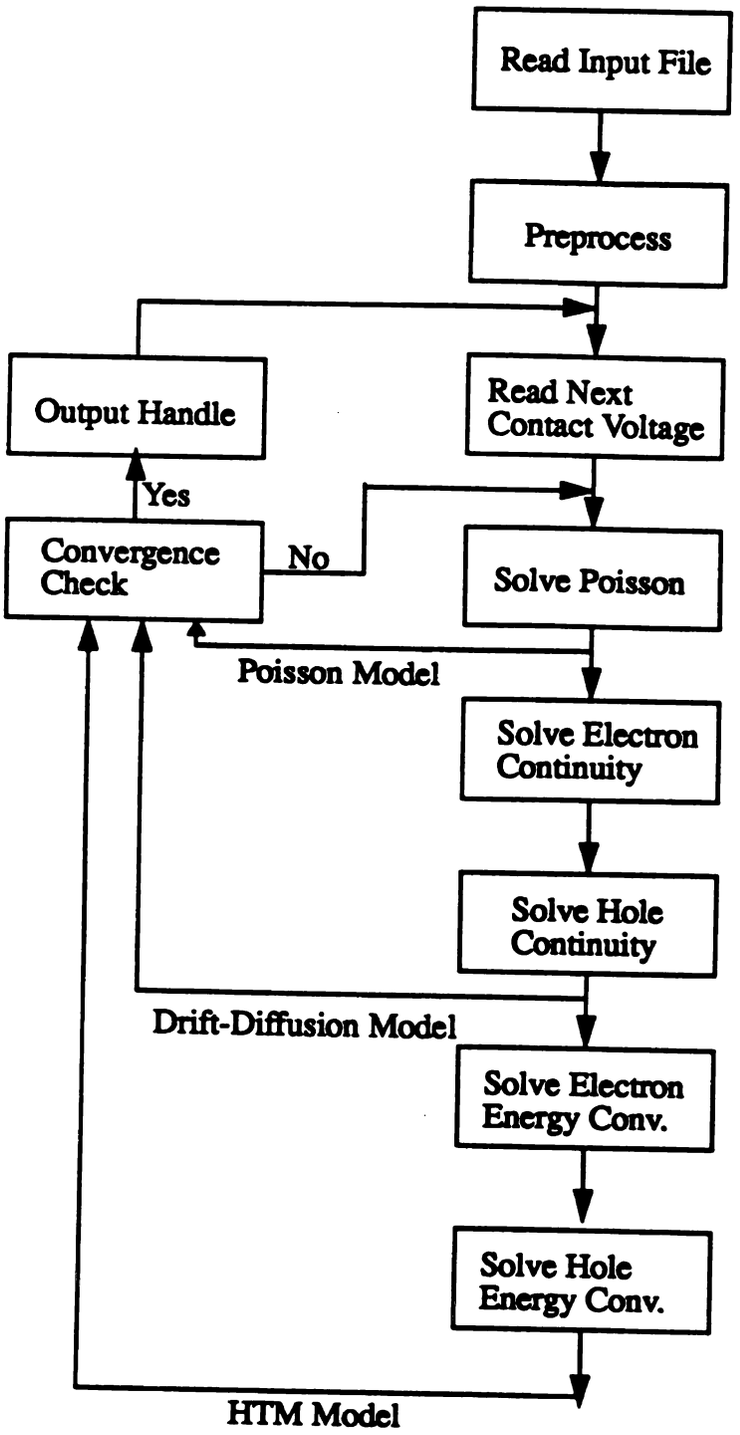


Figure C.1: The algorithm of the device simulation program.

Preprocess: readmet.f, loadhot.f, loadinfo.f, loadini.f, makeitype.f, symlu.f, scale.f, init.f, saveinfo.f, savemesh.f

Read Next Solution: readsol.f, bound.f, loadv.f, loadnp.f, loadt.f

Poisson solution: sparsep.f, funtp.f, solve.f, numlu.f

Electron continuity solution: sparsecn.f, funtcn.f, solve.f, numlu.f

Hole continuity solution: sparsecp.f, funtcp.f, solve.f, numlu.f

Electron energy conservation solution: sparseen.f, funten.f, solve.f numlu.f

Hole energy conservation solution: sparseep.f, funtep.f, solve.f, numlu.f

Convergence check: convchk.f

Output handle: saveout.f, printout.f, currcon.f

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