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MACROMODELING OF IC VOLTAGE REGULATORS

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KENNETH VINCENT NOREN

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MACROMODELING OF IC VOLTAGE REGULATORS

By

Kenneth Vincent Noren

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ABSTRACT

MACROMODELING OF IC VOLTAGE REGULATORS

By

Kenneth Vincent Noren

When computer simulators are used in the design and analysis of electronic systems, it is necessary that the IC's and discrete components being used are well modeled. The modeling of IC's presents a special problem, and one solution to that problem is to develop a *macromodel* for the IC. A macromodel is an equivalent circuit, which is composed of simulator components, that can predict the linear and non-linear behavior of the IC. This macromodel can then be used in simulations of electronic systems which use the IC.

In developing macromodels, it is necessary to choose device characteristics which will adequately describe the chip. Once the characteristics are chosen, and measured in lab, these characteristics become the device phenomenon to be modeled and provide guidelines in model development. This dissertation will describe the development of macromodels for several voltage regulator IC's for use in PSpice.

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CHAPTER 1

INTRODUCTION AND BACKGROUND

1.1 INTRODUCTION

Computers play an important role in all branches of science. Analog electronic circuit design has seen its share of development due to the advancement of computer technology. In the past a designer would sit down and design a circuit based on past experience, intuition and knowledge. The circuit would then be breadboarded. If need be - again based on past experience, intuition, knowledge and now measurements and analysis - the design would be altered. The process would repeat itself until an acceptable breadboarded circuit was obtained. Computer-Aided Design (CAD) is nowadays a part of this procedure. CAD simulations play an important role in the design and analysis phase of electronic circuit design. Circuit simulators, such as SPICE, have grown out of this.

There are misconceptions of the role of circuit simulators in electronic design. Human nature sometimes allows oneself to rely heavily on computer simulations as a substitution for intuition and breadboarding. This is not a correct use of the tool. This is precisely the argument opponents of circuit simulators in electronic design use to justify their non-use. Non-use is also an incorrect use of the tool. The nature of this tool is such that when used properly, it can enhance both intuition and breadboarding. For these reasons, it is necessary that CAD in electronic circuits be further developed from it's present immature state. One area which needs attention is the modeling of devices and IC's for use in the circuit simulators.

1.1.1 Electronic System Design Involving IC's

It is rare today that analog electronic systems are built without at least one analog IC in them. This presents a problem when the designer wants to do a computer simulation. This problem is how to model the IC in order to use it in the simulation package. A brute force method is to use a computer model for the IC which is based on the individual components of the IC. This is called a *device level model*. The device level model can have at least two problems. First, an analog IC, may be composed of several, sometimes thousands of components. This gives rise to very large circuits and can translate into large computer time cost and memory problems, especially due to non-linear components. Secondly, the user seldom has the correct transistor and diode parameters necessary to model the individual components correctly. This translates into an accuracy problem.

One proposed solution is to develop a *macromodel* for the IC. A macromodel by definition is a model for an IC which would predict ac, dc, and transient phenomenon, both linear and non-linear, of that IC. It is usually built out of the ideal components which are available to most circuit simulators. Normally a macromodel is much simpler and contains fewer components than the device level model. This solves the component size problem. Also because the model is normally simpler, the designer has better control over the macromodel characteristics than the design-level model. This means the designer can better fit the characteristics of the actual IC. This solves the accuracy problem. The designer can then use the macromodel for the IC in the computer simulation of the analog electronic system.

1.2 BACKGROUND

The goal of a macromodel is then to obtain a circuit model of an IC which is of much less complexity than that IC itself, using the components available to the circuit simulator. One standard for this is SPICE [1] because many other simulators have elements which are compatible with SPICE, in part because most of simulators are variants of SPICE. The simulator discussed hereafter is PSpice. PSpice has some elements and element definitions which are not compatible with the original SPICE. However all of the elements in SPICE can be used in PSpice. The use of PSpice is justified because it is probably the most widely used simulator in the academic arena. This is because an excellent, also very powerful, student version is available as freeware.

Macromodels are typically built with two techniques. These are *build up* and *simplification*. In simplification, elements or subcircuits of the IC being used are modeled by simpler configurations of ideal elements which provide the same function of that subcircuit. Consider, for instance, that a differential pair can sometimes be modeled as a voltage-controlled voltage source in which the nodes of the differential input become the controlling nodes of the controlled voltage source. This procedure gives rise to macromodels which in terms of functionality, can look very similar to the original circuit. The build up technique, on the other hand, is used when circuit elements are used to build a subcircuit to provide the macromodel with specific characteristics. This subcircuit may bear little resemblance to the elements or subcircuits actually contributing to the phenomenon.

As stated before, one goal of the macromodel is to predict ac, dc, and transient, as well as linear and non-linear phenomenon. In general, the principle of increased

accuracy meaning increased complexity and numbers of components holds true. This fact can provide for different levels of macromodeling. If a user, for example is mainly interested in the small signal gain vs frequency response of an op-amp, so a macromodel developed for this use may not need to model *higher order effects* such as slew rate, voltage clamping, etc, and a simpler model than one modeling all of these effects can be used. In general, when designing macromodels, it is probably best to develop as high an order model as possible, and let the user make any simplifications.

Credit is normally given for the first macromodel to Boyle, et al, in [2]. In [2] a macromodel was developed for integrated circuit op-amps which provides an excellent pin-for-pin representation. The driving force in it's development was to have a model which provided circuit simulations which were much less time costly and used less memory. The full chip model for the 741 and it's corresponding Boyle macromodel are shown in Fig. (1). The model predicted very good results, but as CAD evolved, weaknesses were exposed.

1.2.1 Op-amp Macromodels

The macromodel developed by Boyle was actually more geared toward bipolar op-amps. From the Boyle model, macromodels were derived for MOSFET-bipolar and JFET-bipolar op-amps [3] and all MOS op-amps [4]. The model in [4] pays special attention to the simulation of settling time of the MOS op-amp. All of these can be considered deviations of the Boyle model.

In more recent times, due to the maturing of CAD and computing in general, other macromodels for op-amps were developed by Precision Monolithics [5] and Linear Technology [7]. Both are alternative topologies to the Boyle model which attempt to improve the accuracy of characteristics to that beyond those of the Boyle

model.

Presently, MicroSim uses a modified Boyle model in their circuit simulator PSpice. In their library, they claim to have macromodels for many of the most popular op-amps. There are actually a few topologies. Bipolar input op-amps, for example, all share the same topologies, but may have different component values in those macromodels, in order to produce different device characteristics.

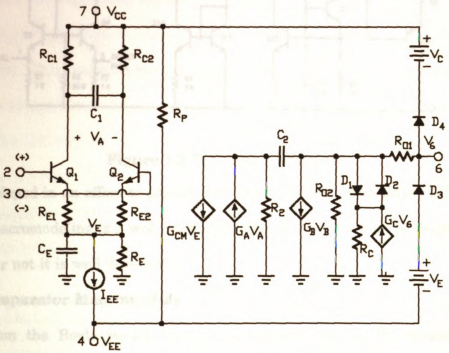

Figure 1.1 Boyle macromodel for the bipolar op-amp

In an attempt to get people to design with their op-amps, many op-amp vendors also provide macromodels of their op-amps. Some of these are Burr-Brown, Comlinear, Harris Semiconductor, Linear Technology, Precision Monolithics, and Texas Instruments [8]. Texas Instruments publishes a data book, compatible with their other product data books, with listings of their op-amp models [9].

Some rather interesting macromodels for op-amps, more application specific,

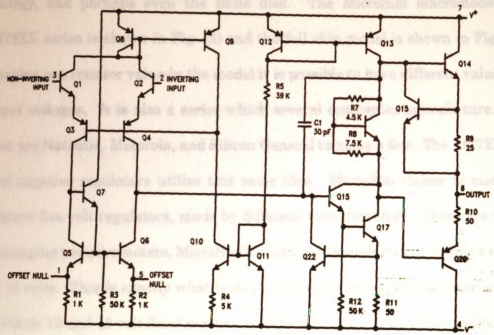

Figure 1.2 741 op-amp schematic

were developed in an effort to predict EMI effects in bipolar op-amps [10] [11]. The op-amp macromodeling is a well worked in area, although it may be debatable as to whether or not it is well developed.

1.2.2 Comparator Macromodels

From the Boyle model, came a macromodel for an IC comparator [12]. MicroSim also provides macromodels for several commercial comparators, again each with the same topology, and based on that found in [2].

Comparator macromodeling is not well developed.

1.2.3 Voltage Regulator Macromodels

MicroSim provides macromodels for several commercial voltage regulator IC's. These are a LM78XX series fixed positive voltage regulator, the LM79XX series fixed negative voltage regulator, and the LM723 adjustable positive voltage regulator. The LM78XX series is a series of positive regulators which all share the same basic

topology, and perhaps even the same dies. The MicroSim macromodel for the LM78XX series is shown in Fig. (3) and the full chip model is shown in Fig. (4). By changing one resistor value in the model it is possible to have different values for the output voltages. It is also a series which several companies manufacture. Some of these are National, Motorola, and Silicon General to name a few. The LM79XX series fixed negative regulators utilize this same idea. MicroSim claims to model many different five volt regulators, made by different manufacturers. These are identical. By changing two parameters, MicroSim's model can provide output voltages of 12 volts and 15 volts. This is exactly what is done to provide corresponding macromodels for all of their 12 and 15 volt fixed positive voltage regulators. The same topology is used to model the LM140 series and LM340 series, of 5, 12, and 15 volt regulators as well.

The topology of the negative regulator macromodel is derived, in part, from that of the positive regulator. The same philosophy in modeling all of the -5, -12, and -15 volt regulators hold true for the negative regulator series as it did for the positive regulators.

Several different companies also manufacture a 723 like chip. These are again Motorola, Fairchild, and Silicon General for example. Microsim has one 723 macromodel which is used to model all of these.

MicroSim provides for variation in certain chip characteristics with ambient temperature. Specifically these are changes in quiescent current and regulated output voltage.

Microsim provides no design formulas. Also, information of what phenomenon is modeled is provided.

Microsim does not provide for variation in macromodels for regulators which

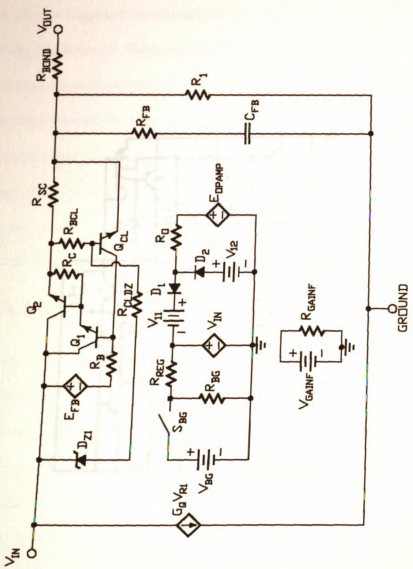

Figure 1.3 *LM78XX series* macromodel by MicroSim

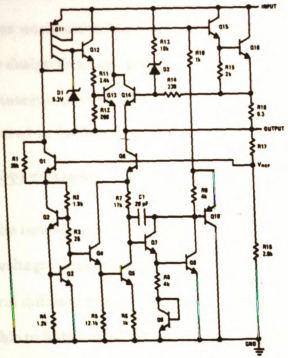

Figure 1.4 LM78XX series device level model

may occur from manufacturer to manufacturer.

Wierzba has a macromodel for an LM117 adjustable positive voltage regulator [13]. Design formulas are given and information on what phenomenon is model is provided. Variation with ambient temperature is not included.

The voltage regulator macromodels are not well developed.

1.2.4 Voltage Reference Macromodels

There is one voltage reference macromodel based on a REF02 topology. The macromodel was created by Analog Devices (formerly Precision Monolithics).

The model has weaknesses based on laboratory measurements here.

There are no design formulas given.

The above statements show both interest in the macromodeling of voltage references and the need to further develop this area.

1.3 PROBLEM STATEMENT

Because of the lack of work done in the area of voltage regulator macromodels, the motivation for voltage regulator macromodeling is clear. Macromodels need to be developed for several different types of regulators. Design formulas need to be given so that users are able to fully utilize the macromodels. This dissertation will focus on the macromodeling of voltage regulator IC's.

Because of the heuristic nature of the problem, special techniques are required to present the work in document format. Consider the problem of building of a pc computer system, for example. An infinite number of solutions existed for this problem. One of these solutions solved the problem. As a result, we have an endless number of solutions to that problem and a wealth of knowledge arising from it. This

situation comes up time and time again in everyday life. This is the nature of the macromodel problem.

The format of this dissertation to first explain some basic regulator terminology. This is done in Chapter 2. Chapters 3-7 explains the developed voltage regulator macromodels for the following voltage regulators: SG7805, SG7812, SG7915, CA3085, UA723, and the SG137. This will provide adequate insight into the understanding of the macromodels. It is at this point, *after* having read about how the models function, and questions have arisen, that the reader is now in a much better position to understand the development. Then, some design issues are discussed in Chapter 8. Finally, conclusions are presented in Chapter 9.

CHAPTER 2

TERMINOLOGY AND LAB APPARATUS

2.1 INTRODUCTION

The voltage regulators which are being modeled are the CA3085, UA723, SG7805, SG7812, SG7915, and the SG137 voltages regulators. These regulators all fall under the category of series-pass voltage regulators. The SG7805, SG7812, and the SG7915 are three-terminal fixed regulators, providing regulated voltages of 5, 12, and -15 volts respectively. The SG137 is a three-terminal, adjustable, negative regulator. The CA3085 is an 8-pin, programmable positive regulator. The UA723 is a 10-pin programmable, positive regulator.

In the development of these models, certain chip characteristics and behavior are chosen as critical. These characteristics not only become the characteristics which are modeled, but also become ways of evaluating regulator performance. Before the models are developed, this short chapter will describe some the performance characteristics which the models are based on. This includes both terminology and laboratory techniques. If the reader has little background with voltage regulators, this chapter should be read before any of the individual chapters on any one of the models is read. Temperature considerations will be discussed first.

2.2 TEMPERATURE CONSIDERATIONS

The temperature effects of the chip are of interest. Chip characteristics are subject to variations with temperature. Models will be provided for the following

temperatures: -55°C, 25°C, and 125°C. This means that all of the measurements performed will be at one of these temperatures. When referring to chip temperature, junction temperature of the device is being referred to. Junction temperature is a function of ambient temperature and power dissipation. A standard, textbook, formula is

$$T_J = T_a + \theta_{jc} \times PD + \theta_{ca} \times PD, \qquad (2.1)$$

where T_j is the junction temperature of the device in degrees celsius,

T_a is the ambient temperature in degrees celsius,

θ_{jc} is the junction to case thermal resistance with units of °C/Watt,

θ_{ca} is the case to ambient thermal resistance with units of °C/Watt,

and PD is the average power dissipation of the chip in Watts.

Note that the product θ_{jc} x PD represents the difference in temperature between the case and the junction and that the product θ_{ca} x PD represents the difference in temperature between the case and the ambient. θ_{jc} is normally given by the manufacturers in the data sheets. This figure depends primarily on the case style that the particular chip uses. θ_{ca} can be determined by using a temperature probe to measure case and ambient temperatures and using the fact that $\Delta T_{ca} = \theta_{jc}$ x PD, where ΔT_{ca} is the difference between the case and ambient temperatures. A heat sink is always used in these measurements, so θ_{ca} is an indication of the thermal properties of the external case and the heat sink.

The method described above is the standard textbook method of estimating the junction temperature. An alternative method was used based on these findings. Several loads were hooked up to the regulator. For each load, the case and ambient

temperatures were measured and θ_{ca} was determined. A problem which occurred was that for different loads, θ_{ca} was significantly different. This is not in accordance with theory. This lead to the following procedure. For each different load, a ΔT_{ca} figure was calculated. This product was then substituted into Eqn. (2.1) to give

$$T_j = T_a + \theta_{jc} \times PD + \Delta T_{ca'} \tag{2.2}$$

Evidently ΔT_{ca} holds fairly constant for different ambient temperatures for a given load. This was verified by measurement. The junction temperature for each load and ambient temperature is then calculated based on Eqn. (2.2). θ_{jc} is assumed to be correct.

Because the models are developed based on junction temperatures, when desiring measurements at -55°C, 25°C, or 125°C, it may be necessary to set the ambient differently from these temperatures in order to compensate for changes in junction temperature due to power dissipation. The ambient temperature is usually lowered by an amount determined from Eqn. (2.2) to produce the desired junction temperatures of -55°C, 25°C, or 125°C.

Several measurements are taken in a pulsed mode. This is when the input to the regulator is a pulsed input. When the regulator is pulsed, it has the effect of turning the regulator off and on. If a duty cycle of say roughly 5% is used, the regulator is off much more than it is on and the average power dissipation is negligible. Then, the junction temperature given by Eqn. (2.1) is roughly the ambient temperature. The ambient temperature of the chip is *always* set by putting the chip inside a temperature chamber with the specified ambient programmed into the chamber's temperature controller. Non-pulsed measurements have a non-zero average

power dissipation. This means that in order to produce the desired junction temperatures, this ambient must be changed in order to compensate for the change in junction temperature which arises from power dissipation.

2.3 PARAMETERS

In this section, parameters which are used to describe the regulators behavior and the circuits used to measure these parameters are discussed.

2.3.1 Line Regulation, Ripple Rejection, and Line Transient Response

An ideal voltage regulator provides a constant, stable, and temperature insensitive output voltage under all possible conditions. IC regulators are very non-ideal. Line regulation, ripple rejection and line transient response reflect the non-ideal behavior of a varying output voltage caused by a varying input voltage.

Line regulation is a measure of how the dc output voltage varies for a varying dc input voltage. It can be defined as

$$LR = \frac{\Delta V_{OUT}}{\Delta V_{IN}}. \tag{2.3}$$

The test circuit used to measure this is shown in Fig. (2.1). The box described as regulator circuit contains the regulator and any external components necessary for the regulator to regulate. This is done in order to view all regulators as a two-port, even the multi-terminal and adjustable regulators. Then, the measurements only deal with input and output terminal characteristics of the entire "regulating circuit". It is also a convenient way to generically look at all test circuits for all of the regulators without having to redefine test circuits. In the case of the three-terminal, adjustable regulators for example, the regulator circuit consists of the regulator and 2 external

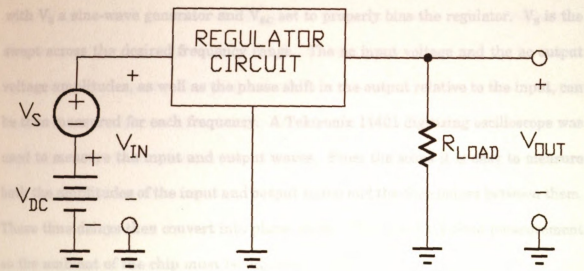

Figure 2.1 Test circuit No. 1

resistors needed to produce the regulated voltage. In the case of a three terminal, fixed regulator, the regulator circuit is simply the regulator circuit itself. In the case of the negative regulators, V_{DC} becomes a negative voltage.

Line regulation is a pulsed measurement. This means that in Fig. (2.1), $V_{DC} = 0$ and V_S is a pulse generator. The change in magnitude of the output voltage pulse is compared to the change in the magnitude of the applied pulse and LR is computed.

Ripple rejection is a measure of how much ac signal can pass through the regulator circuit, as a function of frequency. A formal, mathematical definition is

$$RR(s) \triangleq -20 \log\left(\frac{|Vout(s)|}{|Vin(s)|}\right). \qquad (2.4)$$

Note that the definition is set up so that when the ratio of the output voltage

to the input voltage magnitude is small, the value for RR given by Eqn. (2.4) is large, indicating "good" ripple rejection. The measurement circuit for this is again Fig. (2.1) with V_S a sine-wave generator and V_{DC} set to properly bias the regulator. V_S is the swept across the desired frequency range. The ac input voltage and the ac output voltage amplitudes, as well as the phase shift in the output relative to the input, can be then measured for each frequency. A Tektronix 11401 digitizing oscilloscope was used to measure the input and output waves. From the scope it is easy to measure both the amplitudes of the input and output signal and the time delays between them. These time delays then convert into phase shifts. This is not a pulsed measurement so the ambient of the chip must be adjusted.

Note that the low frequency ripple rejection is a measure of line regulation. This is because the lower frequencies for ripple rejection can be interpreted as being dc, providing the first pole or zero is not near by. Low frequency ripple rejection is then dc ripple rejection. Dc ripple rejection reflects the changes in output voltage due to changing input voltage for dc, which is simply line regulation.

Line transient response is a measure of how the output voltage changes due to a sudden change in the input voltage. This sudden change can be either positive or negative. The test circuit is Fig. (2.1) with V_S a pulse generator and V_{DC} set at a proper biasing level. The average power dissipation due to the pulsed voltage, for small duty cycles, is negligible. The average power dissipation due to the dc bias voltage must be taken into consideration and the ambient compensated accordingly. On the positive edge of the input pulse, effects on the output due to positive changes in input voltage are observed, and on the negative edge of the input voltage the effects on the output voltage due to negative changes in the input voltage are observed.

Ideally during the positive and negative slopes of an applied pulse voltage, any capacitors are can be treated as short circuits and any inductors can be treated as open circuits, which is the exact behavior of these components at high frequencies. This means the ratio of the amplitudes of the change in output voltage to the change in input voltage during the positive and negative edges are a measure of high frequency voltage gain. This ratio is related to high frequency ripple rejection as seen from Eqn. (2.3). Thus, there is a relationship with the line transient response during the positive and negative edges of the input transient peak to ripple rejection.

Theoretically, if the ripple rejection characteristics are known, line regulation and line transient response should match up with ripple rejection. When this was done with lab results, they are close, but not exact. It is up to the modeler to decide which of the parameters above should be used for the model. For example, in the model, low frequency ripple rejection and line regulation will be exact. In lab, they may not be. When modeling, it must be decided which one is most important, either the low frequency ripple rejection or the line regulation. Then, the chosen parameter will be used in determining the model and become both low frequency ripple rejection and line regulation.

2.3.2 Load Regulation, Output Impedance vs Frequency, and Load Transient Response

Another ideal characteristic of a voltage regulator is that for changing loads, the output voltage should remain constant. This is to say that the regulator should have a zero value for it's Thevenin output resistance. In practice, this does not happen. There are three parameters which reflect this type of non-ideal behavior and they are load regulation, output impedance vs frequency, and load transient response.

Load regulation can be defined as

$$LDREG \triangleq -\frac{\Delta V_{OUT}}{\Delta I_{LOAD}}. \tag{2.5}$$

This definition is just the definition of dc output resistance. This is a pulsed measurement. The test circuit is Fig. (2.1) with V_S a pulse generator and $V_{DC} = 0$. The resulting regulated voltages are then compared for each load, or more frequently, under a loaded and non-loaded condition.

Output impedance vs frequency is a measure of how the output impedance of the regulator varies with frequency. Low frequency output impedance is just the load regulation. This is not a pulsed measurement. The test circuit is Fig. (2.1) with $V_S = 0$ and V_{DC} properly biased. The output impedance is then measured with an HP 4192A LF impedance analyzer set up in a four-wire probe configuration across the load.

Load transient response is an indication of how the output voltage responds to either the sudden application of a load, or the sudden removal of a load. In computer simulations, this can be handled with a current source in which the current is pulsed on and off. Practically, this cannot be done. The test circuit to look at these effects is shown in Fig. (2.2). Here, a load is electronically switched on and off at the output of the regulator. The electronic switching is done by the bjt transistor being pulsed. Note that V_S is a pulse generator with a duty cycle of roughly 5%. This means that the load is ungrounded, or the load is "switched off" 95% of the time, and therefore power dissipation of the chip is negligible.

Because when sudden changes in output current occur the reactive elements

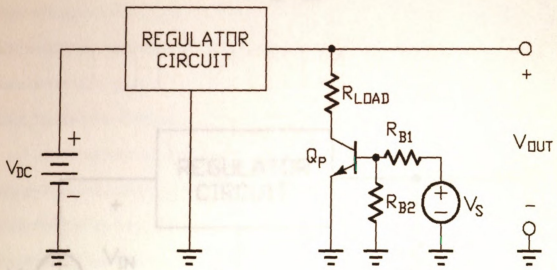

Figure 2.2 Test circuit No. 2

behave as either open or shorts, the peak of the load transient response is a measure of the high frequency change in output voltage for a change in load current. This is just high frequency output impedance.

Similar to ripple rejection, when the macromodel is used, the low frequency output impedance is equal to the load regulation and the high frequency output impedance is equal to the peak of the change in output voltage divided by the change in the output current. In lab, however, these results will be close, but not identical. Again, some trade-offs as to which measurements will be used in the models must be made.

2.3.3 Quiescent Current

Quiescent current is the amount of current which is required to properly bias

the regulator. A standard definition is

$$IQ \triangleq I_{IN} - I_{OUT}, \tag{2.6}$$

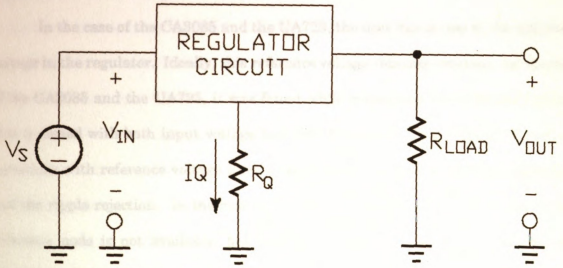

Figure 2.3 Test circuit No. 3

where I_{IN} is the current supplied to the regulator and circuit by the voltage source and I_{OUT} is the current supplied to the load, in the case of the three terminal, fixed, regulators. I_{OUT} is the current supplied the load plus any current required for any external resistors added, such as feedback resistors for the adjustable regulators. For the three terminal regulators, this is conveniently the current coming out of the third terminal. The test circuit is in Fig. (2.3). This is a pulsed measurement so V_S is a pulse generator. The measured voltage across R_Q is used to determine the value of the quiescent current. For the adjustable regulators, the circuits for measuring

quiescent current are slightly different and will be treated in their particular sections.

Quiescent current is not constant. It typically varies with two parameters and these are input voltage and load current. The variations with input voltage are more severe than the variations with load current, so normally, modeling variations with load current is neglected.

2.3.4 Reference Voltage

In the case of the CA3085 and the UA723, the user has access to the reference voltage in the regulator. Ideally, this reference voltage remains constant. In the case of the CA3085 and the UA723, it was found while measuring the reference voltage, that it varied with both input voltage and with frequency. It is believed that these variations with reference voltage have a significant influence on the line regulation and the ripple rejection. In the case of the three terminal references, access to the reference node is not available, but it is assumed, based on the findings for the CA3085 and the UA723, that the reference voltage varies with input voltage and frequency. These variations influence ripple rejection. The measurement circuits for these will be described in the appropriate sections for the CA3085 and the UA723, if they are made.

2.3.5 Dropout Voltage, Dropout Characteristics

Voltage regulators require a minimum input voltage in order to produce the desired output voltage. This is mainly because the circuit needs to be properly biased in order for the regulator to be functioning as a linear device. The difference between the input voltage and the output voltage, just at the point the output voltage begins to regulate, will be termed the dropout voltage.

The dc transfer function between the input voltage and the output voltage will

be termed either the dropout characteristics or V_{OUT} vs V_{IN} characteristics. The input voltage should be swept through some reasonable range, like zero to several volts above the point where the regulator regulates. The dropout characteristics, then, include the dropout voltage in their characteristics.

The dropout voltage and the dropout characteristics vary with load. This is because the load current directly influences the region in which the output pass transistors must operate for proper regulator biasing.

The test circuit for these is Fig. (2.1) with $V_{DC} = 0$ and V_S a pulse generator, and it is a pulsed measurement.

2.3.6. Short Circuit Current Limiting, Foldback Current Limiting

All of the regulators above offer short circuit current limiting, to protect against, for example, the possibility of accidently shorting the output. Short Circuit Current can also be defined as the maximum available output current. In the case of the three terminal regulators, the short circuit current limiting is done internally in the regulator, and cannot be changed. In the case of the CA3085 and the UA723, it is achieved by adding an external resistor. The value of the resistor can vary, giving rise to a user programmed value for short circuit current.

Power dissipation of the regulators, in all cases, is a function of the voltage differential across the chip, and the load current. The voltage differential across the chip is the difference between the input and output voltages of the regulator. As input voltage rises, power dissipation increases, and the potential for exceeding the chip's maximum power dissipation limit and potential for destroying the chip increases. In order to ensure that the power dissipation does not exceed some maximum value, as the differential voltage increases, the maximum output current should decrease. This

is the case for the three terminal regulators, and this effect is known as foldback current limiting. In the case of the CA3085 and the UA723, there is no foldback limiting, although the user may choose to implement this through the use of external device connections.

The test circuit is Fig. (2.1). These are pulsed measurements so $V_{DC} = 0$ and V_S is a pulse generator. R_{LOAD} is chosen to be a value low enough so that at the regulated voltage the resistor needs more current than the amount of current allowed in either the short-circuit current region or the foldback region. This of course cannot happen so the output voltage decreases to an amount equal to the maximum current multiplied by the load resistance. The voltage across R_{LOAD} is measured and since the value of R_{LOAD} is known, the maximum output current can be deduced.

2.3.7 Power Up and Down with Square Wave and Triangle Wave Inputs

These characteristics are the response of the output waveform when the input of the regulator is powered up and down with either a square wave or a triangle wave. A characteristic found in data sheets which is an indication of how the chip responds to power up is the "turn on" time of the regulator. For the triangle wave, the results normally depend upon the slope of the wave. If the rate of change in voltage with time is not significant enough, then non-steady-state characteristics of the output may be lost. What results is just a dc transfer function. The dc function implemented with a triangle wave still provides enough information to include.

Power up and down with square wave is done with Fig. (2.1). This is a pulsed measurement so $V_{DC} = 0$ and V_S is a pulse generator. For power up and down with triangle wave, $V_{DC} = 0$ and V_S is a triangle wave. The triangle wave causes a non-zero average power dissipation, so the ambient temperature must be set.

2

This concludes the introduction to terminology and measurements.

2.4 TEST EQUIPMENT

The following is list of the equipment used:

1) Tektronix 11401 Digitizing Oscilloscope, used to measure and observe waveforms.

2) PM 5193 programmable synthesizer/function generator, used for sine wave generation.

3) HP 214A pulse generator, used for square wave and pulse generation.

4) Wavetek model 186 function generator, used for triangle wave generation.

5) Fluke 8506A digital multimeter, used for measuring resistances and voltages.

6) Fluke 8840A digital multimeter, used for measuring resistances and voltages.

7) HP 4192A LF Impedance Analyzer, used for measuring output impedances and capacitances.

8) Trygon model HR40-750 power supply, used to generate DC voltages between 0 and 20 volts.

9) HP 6634A DC power supply, used to generate DC voltages between 0 and 20 volts.

10) NJE model QRP-160-3 dc power supply, used to generate voltages greater that 50 volts.

11) Thermatron S1.2 temperature chamber, used to control the ambient temperature of the chip.

12) Thermatron 2800 programmer/controller, used to control the temperature chamber. This is built right into the chamber.

3.1

CHAPTER 3

SG7805 / SG7812 MACROMODEL DEVELOPMENT

3.1 INTRODUCTION

The SG7805 and the SG7812 macromodels are done together. In the actual chips for these regulators, the SG7800 series shares the same topology, with the exception of one value for one of the resistors in the circuit. This resistor is such that changing its value results in changing the output voltage of the regulator. Hence, it is possible to have a basic topology provide for many different desired regulated output voltages. Of course, the more common output voltages of 5, 12, and 15 Volts, as well as less common values are manufactured. Because of this fact, it seems reasonable that the macromodel for the SG7805 and SG7812 are nearly identical. Thus, the macromdel for these are nearly identical.

The SG7805 is developed first, at room temperature and then at -55°C and 125°C, then this model is adapted to the SG7812. The macromodel under development is referred to as the SG78XX model until adapted to one of the specific chips to be modeled.

The functional block diagram for the SG78XX is shown in Fig. (3.1). Note that the feedback resistors are R_{23} and R_{24}. It is R_{23} that is changed in the chip and

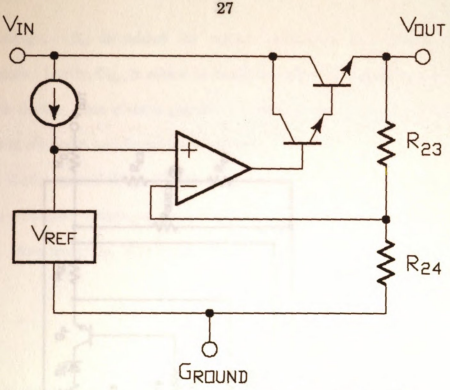

Figure 3.1 Functional block diagram for the SG78XX

macromodel to produce the different regulated output voltages.

3.2 DEVELOPMENT

The macromodel for the regulator is shown in Fig. (3.2). The voltage reference generator and bias current source shown in Fig. (3.1) are replaced by D_{Z1}, R_{ZR}, R_Q, R_R, D_{ZR}, and L_1. The error amplifier has been replaced by E_A, R_{OUT}, R_P, C_P, E_B, D_+, D_-, V_+ and E_+. The resistors R_{24} and R_{23} are the feedback resistors. Finally the Darlington pair pass transistor has been replaced by one pass transistor and a small base resistance and these are Q_P and R_B, respectively. Additions not shown in the functional block diagram follow. D_{BL}, D_{CL}, R_{BCL}, R_{SC}, R_{FB}, Q_{CL}, and D_{ZFB} are added to model the behavior of short circuit current limiting and foldback current limiting. G_B and R_{QUIES} are added to model the quiescent current. R_C and D_C are added to model

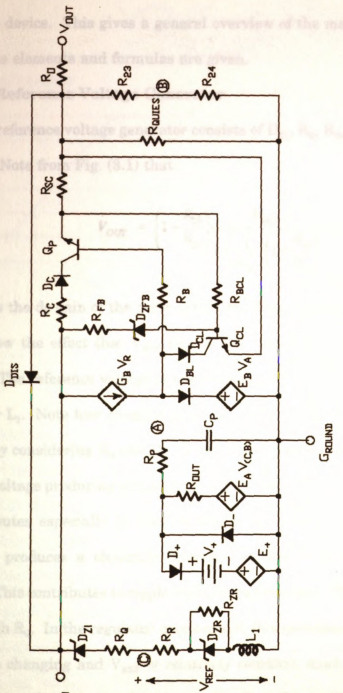

Figure 3.2 Full macromodel for the SG78XX

dropout voltage. R_O is added for output resistance and output impedance characteristics. Lastly, D_{DIS} is added to model the effect of capacitive load discharge through the device. This gives a general overview of the macromodel, and now the details of the elements and formulas are given.

3.2.1 The Reference Voltage Generator

The reference voltage generator consists of D_{Z1}, R_Q, R_R, D_{ZR}, R_{ZR}, and L_1 shown in Fig. (2). Note from Fig. (3.1) that

$$V_{OUT} = \left(1 + \frac{R_{23}}{R_{24}}\right) \frac{V_{REF}}{1 + \frac{1}{A_{DC}}\left(1 + \frac{R_{23}}{R_{24}}\right)}, \qquad (3.1)$$

where A_{DC} is the dc gain of the error amplifier. This equation for the output voltage helps to show the effect that V_{REF} has on the output if it varies with voltage and frequency. The reference voltage is taken across the resistor R_R, the diode D_{ZR}, and the inductor L_1. Note how changes in the dc input voltage for a grounded regulator effect V_{REF} by considering R_Q and R_R. This means that the reference voltage changes with input voltage producing a change in output voltage in accordance with Eqn. (3.1). This contributes especially to line regulation and ripple rejection. Likewise, the inductor L_1 produces a changing reference voltage with changing input voltage frequency. This contributes to ripple rejection vs frequency. Finally, note that current flows through R_Q. In the regulator macromodel, this contributes to quiescent current. When V_{IN} is changing and V_{REF} is relatively constant, most of the change in input voltage is dropped across R_Q, since in practice $R_Q > R_R$. In the modeling, this means that the current through R_Q is changing and hence quiescent current is changing. In the macromodel, R_Q is almost entirely responsible for changes in quiescent current due

to changes in the input voltage.

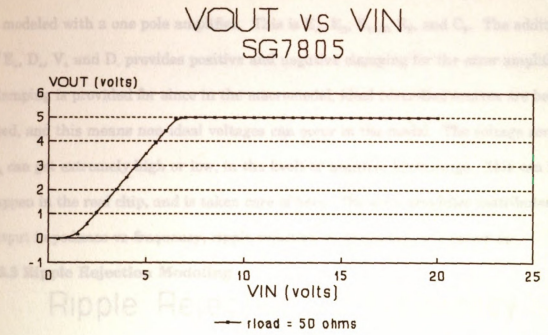

Figure 3.3 V_{OUT} vs V_{IN}, measured

In the actual chip measurements, it is determined that there is no activity and the output of the regulator for an input voltage from zero to anywhere between .75V and 1.5V. This is because overcoming one or more diode drops is necessary to begin to turn the chip "on". Note this in Fig. (3.3), which shows V_{OUT} vs V_{IN} for the SG7805 regulator. This effect is modeled by the zener diode D_{Z1}. V_{REF} cannot begin to develop any voltage drop until the breakdown voltage of D_{Z1} is overcome. This means the circuit shows no activity, since the circuit is dependent upon V_{REF} for functioning. Labeling the "on" voltage as V_{ON} means

$$BV_{DZ1} = V_{ON} \tag{3.2}$$

3.2.2 The Error Amplifier

The SG78XX series contains a frequency compensated error amplifier and this is modeled with a one pole amplifier. This is E_A, E_B, R_{OUT}, R_P, and C_P. The addition of E_+, D_+, V_+ and D_- provides positive and negative clamping for the error amplifier. Clamping is provided for since in the macromodel, ideal controlled sources are being used, and this means non-ideal voltages can occur in the model. The voltage across E_A can get extremely high or low, in the kvolt or negative kvolt range. This can not happen in the real chip, and is taken care of here. The error amplifier contributes to output impedance vs frequency, ripple rejection vs frequency, and power up.

3.2.3 Ripple Rejection Modeling

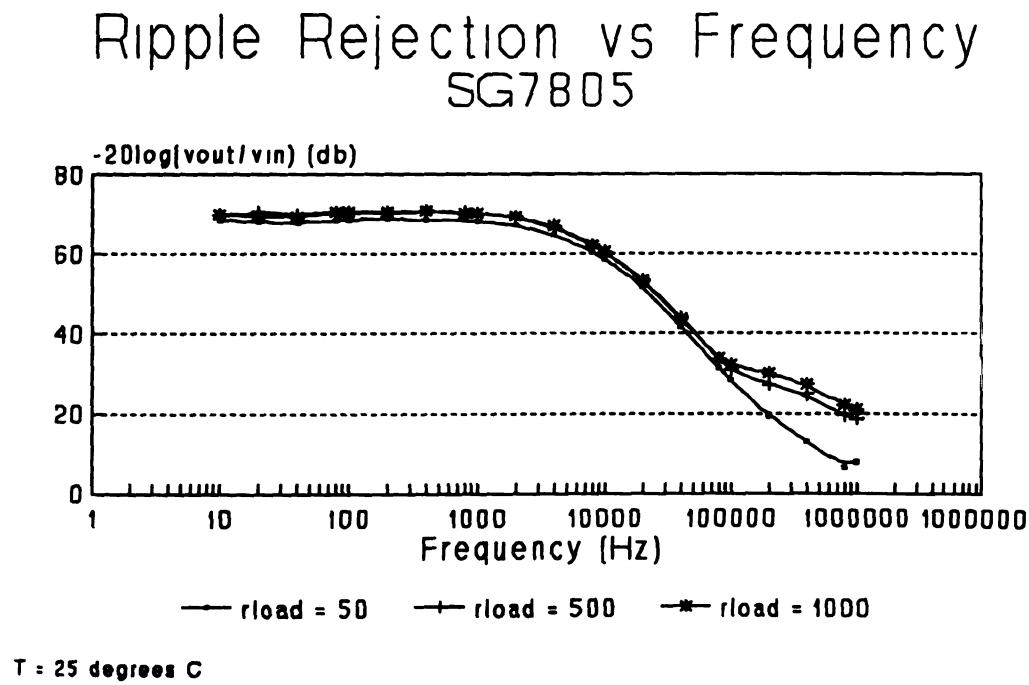

Figure 3.4 Ripple rejection vs frequency, measured

Fig. (3.4) gives an example of ripple rejection vs frequency of the SG7805 for different loads. In modeling the ripple rejection, the following approximations are made. First, it is be assumed that low frequency ripple rejection for all three loads

is be nearly equal. Secondly it is assumed that the first pole for ripple rejection vs frequency is almost equal for all three loads.

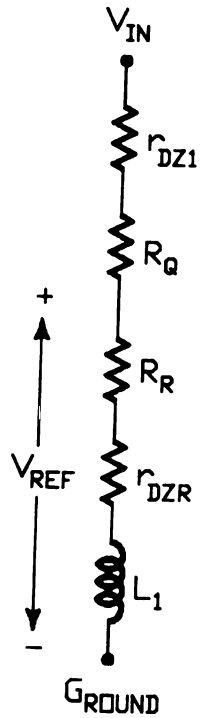

Figure 3.5 AC equivalent circuit for the reference circuitry

From the definition of ripple rejection, a zero in the transfer function, Eqn. (1), is a pole in the ripple rejection response. Note that because V_{REF} is actually a function of V_{IN}, Eqn. (3.1) becomes a transfer function relating V_{OUT} to V_{IN}. A zero of V_{REF} is a pole of ripple rejection. It is necessary to find the zero in V_{REF}. Fig. (3.5) gives the ac equivalent circuit for V_{REF}, neglecting R_{ZR} since $R_{ZR} \gg r_{DZR}$. From this circuit, it is determined that

$$v_{ref} = \frac{R_R + r_{DZR} + sL_1}{R_R + r_{DZR} + R_Q + r_{DZ1} + sL_1} v_{in}. \tag{3.3}$$

This shows that the first pole in the ripple rejection is,

$$Pl_{RR} = \frac{(R_R + r_{DZR})}{L_1}. \tag{3.4}$$

The formula for dc ripple rejection is also needed. This again comes from Eqn. (3.1). It is necessary to find the small signal, dc relationship for V_{REF} with V_{IN}. From, Fig. (3.5) this is

$$v_{ref} = \frac{R_R + r_{DZR}}{R_R + r_{DZR} + R_Q + r_{DZ1}} v_{in}, \tag{3.5}$$

or

$$v_{ref} \approx \frac{R_R + r_{DZR}}{R_Q} v_{in}, \tag{3.6}$$

since in practice R_Q is much larger than R_R, r_{DZR} and r_{Z1}. This can be used with Eqn. (3.1) to solve for the formula for low frequency ripple rejection and it is

$$RR_{LF} = \left(\frac{V_{OUT}}{V_{IN}}\right)_{DC} = \frac{\left(1 + \frac{R_{23}}{R_{24}}\right)\left(\frac{R_R + r_{DZR}}{R_Q}\right)}{1 + \frac{1}{A_{DC}}\left(1 + \frac{R_{23}}{R_{24}}\right)}. \tag{3.7}$$

It can be seen from Fig. (3.4) that there is also a zero in the ripple rejection response. This is modeled in the macromodel, and will not be determined by the ripple rejection response, but will be determined by the power up response, since both are due to the capacitor C_P.

3.2.4 Output Impedance Modeling

Output impedance vs frequency is shown in Fig. (3.6). Low frequency output impedance is determined primarily by R_O. For changes in load, low frequency output impedance also changes due to the small signal parameters for Q_P changing. To select R_O, the simple relationship

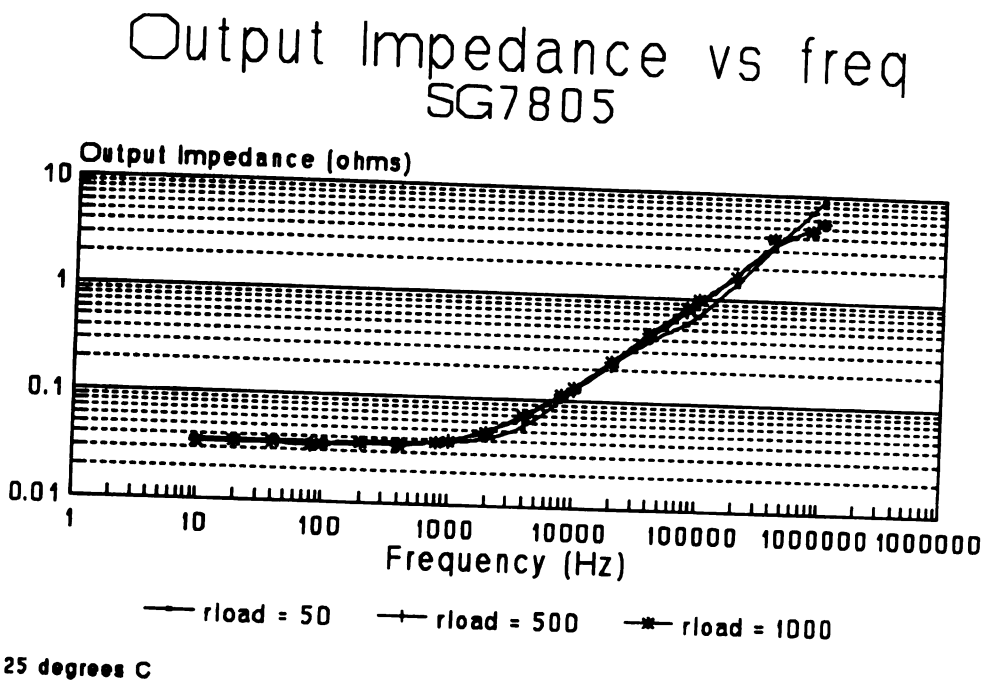

Figure 3.6 Output impedance vs frequency, measured

$$Z_{OUT,LF} \approx R_O \tag{3.8}$$

is used. The frequency characteristics of $Z_{OUT}(s)$ are determined primarily by C_P. As stated with ripple rejection, this parameter is selected based on the power up response. When this is done, this gives adequate results for the first zero in the output impedance vs frequency response. Variations in output impedance with load are modeled because of a correct choice in the topology, however these are not modeled with strict accuracy.

3.2.5 Quiescent Current Modeling

In Fig. (3.2) the elements which contribute to quiescent current are G_B, R_{QUIES}, R_Q and R_{24}. Fig. (3.7) shows the measured quiescent current vs input voltage. The quiescent current modeling works in the following way. G_B is a voltage dependent

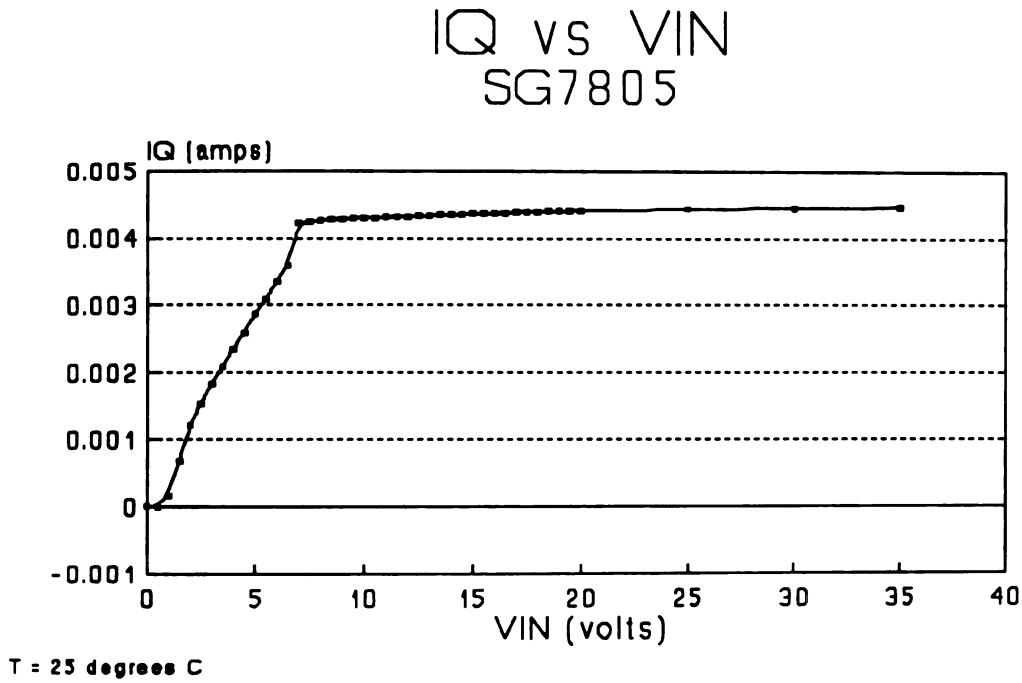

Figure 3.7 Quiescent current vs input voltage, measured

current source which depends upon the voltage V_{REF}. This simulates the realistic behavior of a current source gradually turning on until reaching it's maximum value when the correct regulator biasing is achieved. Initially, IQ is zero, and no voltages appear in the macromodel as there is not enough voltage to overcome the breakdown voltage of D_{Z1}. As V_{IN} increases, V_{REF} increases and thus G_B increases. However, all of the current supplied by G_B is drawn by Q_P. This means that the quiescent current consists of only the current flowing through R_{QUIES} and R_{24}. At the point where V_{OUT} achieves regulation, Q_P enters into the active region. Since Q_P has a very large BF, during this transistion it goes from drawing most of the current available from G_B to little of the current available from G_B. This causes the 'jump' in quiescent current seen in the transfer function. The current from G_B now contributes to quiescent current. This means

$$\Delta IQ_{JUMP} = g_B V_{REF} \tag{3.9}$$

Once regulation is achieved, there is little significant change in the quiescent current due to G_B, R_{QUIES}, and R_{24}. The changes in quiescent current with input voltage seen beyond this point are modeled by R_Q. Large changes in input voltage effect the reference voltage circuitry mainly as changes in the voltage drop across R_Q, since V_{REF} and the voltage across D_{Z1} are nearly constant. This means in this region

$$\frac{\Delta IQ}{\Delta V_{IN}} = \frac{1}{R_Q}. \tag{3.10}$$

Finally, just at the point where the regulated voltage occurs at the output of the regulator, the point right after the jump occurs in the quiescent current

$$IQ = \frac{V_{OUT}}{R_{QUIES}} + \frac{V_{REF}}{R_{24}} + g_B V_{REF} \tag{3.11}$$

3.2.6 Short Circuit Current Limiting and Foldback Current Limiting

An example of measured short circuit current and foldback current limiting is shown in Fig. (3.8).

The addition of short circuit current and foldback current are given by D_{CL}, Q_{CL}, R_{BCL}, R_{FB}, D_{ZFB}, and R_{SC}. The short circuit current works in the following way.

Note that D_{BL} prevents the controlled source E_B from supplying any current to the base of Q_P. This means that G_B supplies all of the current to Q_P. This is an important point. As current flows out of the emitter of Q_P through R_{SC} and to the load, a voltage is generated across the base emitter junction of Q_{CL}, due to the voltage drop across R_{SC}. If this voltage is large enough to turn Q_{CL} on, most of the current supplied by G_B is drawn by the collector of Q_{CL}, since it's needs are large compared to the current supplied by G_B. The remaining current is suppied to the base of Q_P in

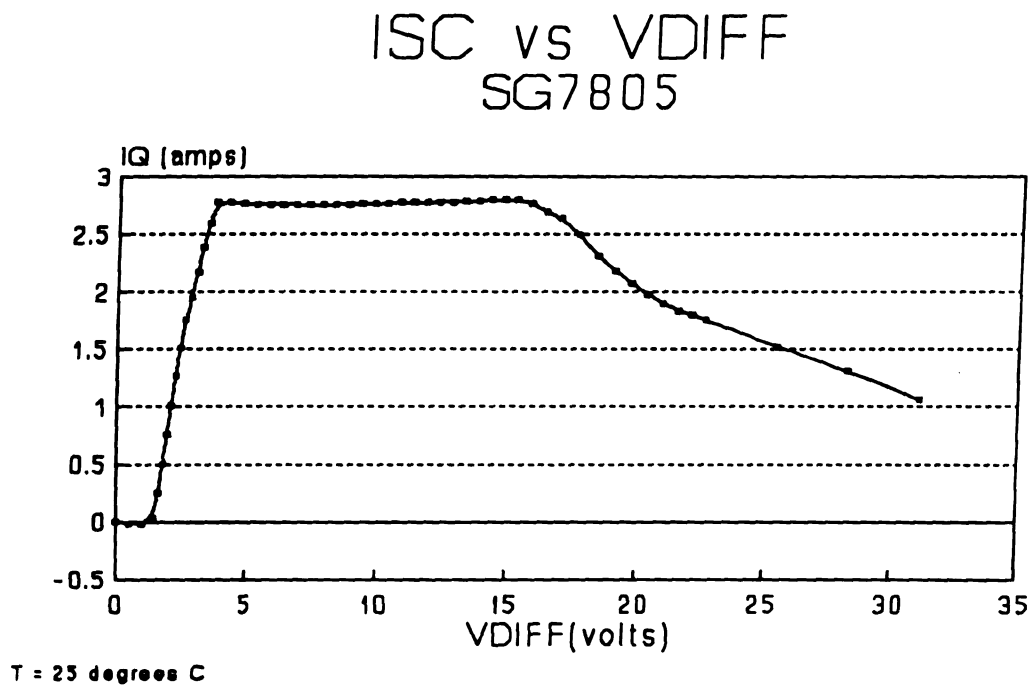

Figure 3.8 Maximum output current vs V_{DIFF}, measured

order to produce the voltage across R_{SC}. If the base emitter voltage of Q_{CL} is not large enough to turn on Q_{CL}, it remains off and draws no current. The maximum output current is then just the current required to turn Q_{CL} on. This is

$$I_{MAX} = I_{SC} = \frac{V_{BE,ON,CL}}{R_{SC}}. \tag{3.12}$$

This is a very simplified explanation of how short circuit current works, however it serves to explain the fundamental operation. Under the short circuit mode, the base of Q_P still draws only a small amount of current. The collector of Q_{CL} draws most of the current available from G_B. This means that in Eqn. (3.10), $V_{BE,ON,CL}$ can be estimated since the collector current of Q_{CL} can be estimated as approximately the total current supplied by G_B, which is $g_B V_{REF}$. Using an approximation for the relationship between collector current and base emitter voltage and inserting into

Eqn. (3.10) gives

$$I_{SC} \approx \frac{V_T \ln\left(\frac{g_B V_{REF}}{IS_{CL}}\right)}{R_{SC}}. \tag{3.13}$$

Note the addition of D_{CL}. This diode was added in order to prevent current from coming in through the output pin and eventually flowing through the collector of Q_{CL}. This was witnessed in the computer simulations with the macromodel.

Finally, foldback current limiting is provided with the addition of D_{ZFB} and R_{FB}. An explanation follows.

Foldback current is normally given as a function of differential voltage. This is roughly the voltage drop across R_{FB}, D_{ZFB}, R_{BCL}, and R_{SC}. When the differential voltage is less than the breakdown voltage of D_{ZFB}, there is no drop across R_{FB} and very little drop across R_{BCL}, due to little base current of Q_{CL}, and also R_{SC}, due to this having a small resistance.

Once the differential voltage exceeds the breakdown voltage of D_{ZFB}, the device enters into the foldback region. Now the difference between the chip's differential voltage and the breakdown voltage of D_{ZFB}, is largely dropped across R_{FB} and R_{BCL}. The voltage drop across the base emitter junction of Q_{CL} is

$$V_{BE,CL} = V_{RBCL} + V_{RSC} \tag{3.14}$$

The turn on voltage of Q_{CL} is fixed, as well as the voltage drop across R_{BCL}, for a given V_{DIFF}. Since R_{BCL} is no longer equal to zero in the foldback region, from Eqn. (3.14), it is seen that a smaller voltage drop across R_{SC} is necessary to turn on Q_{CL}. Hence a smaller output current will turn on Q_{CL} and so a smaller maximum current is available to the output. As the differential voltage across the chip increases, the

voltage drop across R_{BCL} increases, and maximum available output current decreases. This is how foldback current limiting is achieved.

Since the foldback region begins at the point where the differential voltage across the chip, V_{DIFF}, is equal to the breakdown voltage of D_{ZFB},

$$BV_{DZFB} \approx V_{FB} \tag{3.15}$$

where V_{FB} is the differential voltage required to put the regulator into the foldback region. The values for R_{BCL} and R_{FB} can be selected by selecting a point in the foldback region which gives the maximum output current for a given differential voltage. Then, from Fig. (3.2) and Eqn. (3.14), it can be determined that

$$V_{BE,CL,ON} = (V_{DIFF} - BV_{DZFB}) \left(\frac{R_{BCL}}{R_{BCL} + R_{FB}} \right) + I_{MAX} R_{SC} \tag{3.16}$$

The first term in Eqn (3.16) is V_{RBCL} and the second term is V_{RSC}.

3.2.7 Power Up and Down, Square Wave

Fig. (3.9) gives the measured power up square wave response. There are two main contributions to the power up square wave phenomenon. The first is the turn-on time. As seen in Fig. (3.9), there is a period of time it takes for the output voltage required to reach it's steady state regulated output value. This time is mainly the time required to charge up the capacitor in the error amplifier, C_p. This time is proportional to the time constant due to R_p and C_p. Presently, there is no formula for determining these values. They are adjusted empirically.

Secondly, when the input makes the transistion from on to off and the load is capacitive, the load must discharge. This is normally the case for the SG7805 where a capacitor is always required at the output for stability. The path for this discharge

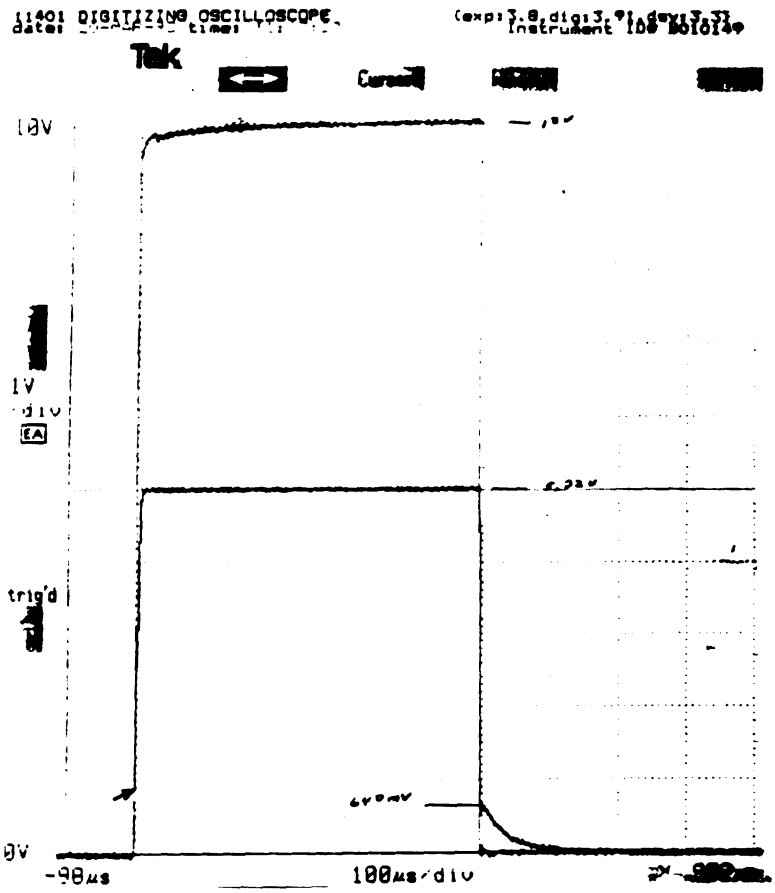

Figure 3.9 Power up and down, square wave, measured

is through D_{DIS} and R_O and back into the power supply. This effect was verified by measurements. Note in Fig. (3.9), the difference between the input and output voltage is roughly one diode drop. This is further justification for use of this D_{DIS}. Finally, if D_{DIS} is not used, the capacitor must discharge through the parallel combination of the load resistance, the feedback resistor R_{23}, and R_{QUIES}. The simulations where D_{DIS} is not present show that this discharge path is inadequate for the rapid discharge which is shown in Fig. (3.9). It is possible to model the voltage difference between the input and output voltages by varying the parameter N in D_{DIS}. This again is done empirically.

3.2.8 Dropout Characteristics

The dropout characteristics are controlled primarily by R_C, D_C and Q_P. The dropout voltage is the voltage drop across these elements when Q_P is on the edge of saturation. Then

$$VDO \approx I_{LOAD}R_C + V_{DC} + V_{SAT,QP}(I_{LOAD}), \tag{3.17}$$

where it should be noted that $V_{SAT,QP}$ is a function of the load current. Then N_{DC} can be chosen to realize a dropout voltage for a given load with

$$VDO \approx I_{LOAD}R_C + N_{DC}\,VT \ln\left(\frac{I_{LOAD}}{IS_{DC}}\right) + V_{SAT,QP}(I_{LOAD}) \tag{3.18}$$

3.2.9 Other Modeled Characteristics

The characteristics presented are sufficient to produce the macromodel of the SG7805. These characteristics give the guidelines in choosing components and parameters. Because of a correct choice of components and parameters, the macromodel can accurately predict other responses. These are: power up and down

with triangle wave, line transient response, load transient response, line regulation and load regulation. These responses are shown in a later section.

3.3 DESIGN PROCEDURE FOR A SG7805

Based on the equations and procedures shown in the last section, a design procedure will be developed in this section.

Basic to the design procedure is a list of measurements required to base the design on. The following measurements should be taken in the basic regulator circuit:

1) Measure V_{OUT} vs V_{IN} with no load.
2) Measure IQ vs V_{IN} with no load.
3) Measure V_{OUT} for V_{IN} = 10V, no load.
4) Measure ripple rejection vs frequency, $R_{LOAD} = 50\Omega$.
5) Measure maximum output current vs voltage differential.
6) Measure output impedance vs frequency.
7) Measure dropout voltage with $R_{LOAD} = 50\Omega$.
8) Measure R_{LOAD}.

The component selection procedure is:

1) Select E_A and E_B. This determines A_{DC}.
2) Select $R_{23} = 1800\Omega$ and $R_{24} = 600\Omega$. These selections are based on the actual chip component values.
3) Select the amplifier clamping circuitry parameters, these are: R_{OUT}, V_+, the gain of E_+, and the diode parameters for D_+ and D_-.
4) Based on the V_{OUT} vs V_{IN} measurement, determine the input voltage required to begin to turn the circuit on, V_{ON}, then

$$BV_{DZ1} = V_{ON} \tag{3.19}$$

Select NBV_{DZ1} and R_{ZR}.

5) From the measured value of V_{OUT} at V_{IN} = 10V, and utilizing Eqn. (3.1),

$$BV_{ZR} = V_{REF} = \frac{V_{OUT}}{\left(1+\frac{R_{23}}{R_{24}}\right)}\left(1+\frac{1}{A_{DC}}\left(1+\frac{R_{23}}{R_{24}}\right)\right). \tag{3.20}$$

Select NBV_{DZR} and R_{ZR} = 1MEGΩ.

6) Measure the slope of IQ vs V_{IN} for the quiescent current measurement. Then from Eqn. (3.10),

$$R_Q = \frac{\Delta V_{IN}}{\Delta IQ}. \tag{3.21}$$

7) From the ripple rejection measurement, determine RR_{LF}. Then determine the small signal resistance of D_{ZR}. This is determined from a trial macromodel run with PSpice. Then from Eqn. (3.7),

$$R_R = \left(\frac{\left(1+\frac{1}{A_{DC}}\left(1+\frac{R_{23}}{R_{24}}\right)\right)RR_{LF}}{1+\frac{R_{23}}{R_{24}}}\right)R_Q - r_{DZR} \tag{3.22}$$

8) From the ripple rejection measurement, determine $P1_{RR}$. Then from Eqn. (3.4),

$$L_1 = \frac{R_R + r_{ZR}}{P1_{RR}}. \tag{3.23}$$

9) Select R_P.

10) From the power up measurement, measure the turn-on delay and from

this measurement, determine C_P empirically.

11) Also from the power up measurement, and measuring the difference in the input and output voltage waveforms directly after power down, select and appropriate value for N_{DDIS}.

12) From the IQ vs V_{IN} measurement, determine the value of the jump in quiescent current just after regulation is achieved. Then from Eqn. (3.9),

$$g_B = \frac{\Delta IQ_{JUMP}}{V_{REF}}. \tag{3.24}$$

13) From the IQ vs V_{IN} measurement, determine the value of quiescent current at the point where regulation is achieved. Then from the value of V_{OUT} at V_{IN} = 10V, and from Eqn. (3.11),

$$R_{QUIES} = \frac{V_{OUT}}{IQ - \frac{V_{REF}}{R_{24}} - g_B V_{REF}}. \tag{3.25}$$

14) Select the parameters for the output transistor Q_P. These are: BF, VAF, NF, and IS.

15) Select R_B.

16) Select the parameters for the transistor Q_{CL}, these are: BF_{CL} and IS_{CL}.

17) Select R_{BCL}.

18) From the maximum output current vs voltage differential, select the value of I_{CL} when the device is not in the foldback region. Then from Eqn. (3.13),

$$R_{SC} = VT \ln \frac{\left(\frac{g_B V_{REF}}{IS_{CL}}\right)}{I_{SC}}. \tag{3.26}$$

19) From the maximum output current vs voltage differential, select the value where the curve enters into the foldback region and call this voltage V_{FB}. Then

$$BV_{DZFB} = V_{FB}. \tag{3.27}$$

Select NBV_{DZFB}.

20) From the maximum output current vs voltage differential, select a value for the maximum output current and it's corresponding output voltage. Then from Eqn. (3.15),

$$R_{FB} = \left(\left(\frac{V_{DIFF} - BV_{DZFB}}{VT \ln\left(\frac{g_B V_{REF}}{IS_{CL}}\right) - I_{MAX} R_{SC}}\right) - 1\right) R_{BCL}. \tag{3.28}$$

21) From a trial run with the macromodel, determine the value for $V_{SAT,QP}$. Select R_C. Select IS_{DC}. Determine the value of the load current. From the measured dropout voltage, VDO, and Eqn. (3.18),

$$N_{DC} = \frac{VDO - I_{LOAD} R_C - V_{SAT,QP}}{VT \ln\left(\frac{I_{LOAD}}{IS_{DC}}\right)}. \tag{3.29}$$

22) From the output impedance vs frequency measurement, determine low frequency output impedance for the no load condition. Then

$$R_O = ZOUT_{LF}. \tag{3.30}$$

23) Select the parameters for the diodes D_{BCL} and D_{CL}, IS and N. These may be important for convergence reasons.

This concludes the design procedure. All of the parameters for the macromodel have been selected.

3.4 DESIGN PROCEDURE EXAMPLE

In this section, an example based on actual laboratory measurements will be presented, and a comparison of the predictions of the macromodel with lab results will be given.

The design procedure is based on measurements in lab. The data, unless otherwise specified, is taken directly off from the plots which are were shown previously in the document.

1) Set $E_A = 300$, $E_B = 2$, so $A_{DC} = 600$.

2) Set $R_{23} = 1800\Omega$, $R_{24} = 600\Omega$.

3) Set $R_{OUT} = 25\Omega$, $V_+ = -1V$ and $E_+ = 1$. Let the diodes D_+ and D_- have the PSpice default parameters. This means that $V_{MAX} = (V_{IN} - 0.3)V$ and $V_{MIN} = -0.7V$ if the voltage drops across the diodes are taken as 0.7V.

4) Based on the V_{OUT} vs V_{IN} measurement, $BV_{DZ1} = 1.5V$.
Select $NBV_{DZ1} = 0.01$. This helps the voltage drop across D_{Z1} be close to BV_{DZ1}. In fact, all of the diodes being used as zener diodes should have the parameter NBV set to 0.01 or 01.

5) $V_{OUT} = 5.027V$, then $BV_{DZR} = 1.2651V$.
Set $NBV_{DZR} = 0.1$.

6) Based on the IQ vs V_{IN} measurement, R_Q = 112090Ω.

7) RR_{LF} = 70db = .316228m and r_{DZR} = 4.22Ω,
then R_R = 4.7Ω.

8) $P1_{RR}$ = 1785Hz, so L_1 = .796mH.

9) Set R_P = 50Ω.

10) By iteration, C_P = .5uF.

11) By iteration, N_{DDIS} = 0.7.

12) The jump in the IQ vs V_{IN} measurement is .6328mA, then g_B = .5002m.

13) The value of the quiescent current at the point where regulation is achieved is 4.2215mA. This gives R_{QUIES} = 3396Ω.

14) Set IS_{QP} = 1e-12A, BF_{QP} = 70k, and VAF_{QP} = 150.

15) Set R_B = 100Ω.

16) Set BF_{CL} = 100Ω.

17) Set R_{BCL} = 1600Ω.

18) From the short circuit current measurement, ISC = 2.7688A,
then R_{SC} = .275Ω.

19) From the short circuit current measurement, the point at which foldback occurs is 15.26V, then BV_{DZFB} = 15.26V.
Set NBV_{DZFB} = 0.01.

20) From the short circuit current measurement, the point V_{DIFF} = 31.08V and I_{MAX} = 1.06A was selected, then R_{FB} = 62196Ω.

21) In lab, the dropout voltage for a 50 resistor was determined to be 1.59V, then N_{DC} = 1.1617.

22) Based on the low frequency, no load, output impedance vs frequency

```
SUBROUTINE MODEL
*
*
DIMENSION MODEL(1)
COMMON /BLOCK1/ MODEL
EQUIVALENCE (MODEL(1),
1 MODEL(2),
2 MODEL(3),
3 MODEL(4),
4 MODEL(5),
5 MODEL(6),
6 MODEL(7),
7 MODEL(8),
8 MODEL(9),
9 MODEL(10),
A MODEL(11),
B MODEL(12),
C MODEL(13),
D MODEL(14),
E MODEL(15),
F MODEL(16),
G MODEL(17),
H MODEL(18),
I MODEL(19),
J MODEL(20),
K MODEL(21),
L MODEL(22),
M MODEL(23),
N MODEL(24),
O MODEL(25),
P MODEL(26),
Q MODEL(27),
R MODEL(28),
S MODEL(29),
T MODEL(30),
U MODEL(31),
V MODEL(32),
W MODEL(33),
X MODEL(34),
Y MODEL(35),
Z MODEL(36),
$ MODEL(37),
= MODEL(38),
- MODEL(39),
+ MODEL(40),
* MODEL(41),
/ MODEL(42),
( MODEL(43),
) MODEL(44),
, MODEL(45),
. MODEL(46),
' MODEL(47),
0 MODEL(48),
1 MODEL(49),
2 MODEL(50),
3 MODEL(51),
4 MODEL(52),
5 MODEL(53),
6 MODEL(54),
7 MODEL(55),
8 MODEL(56),
9 MODEL(57))
RETURN
END
```

measurement, R_O = 0.025Ω.

23) Set IS_{DCL} = IS_{DBL} = 1e-4A.

Set N_{DCL} = 2.

This concludes the design procedure for the room temperature macromodel for the SG7805. The PSpice macromodel description is:

```
.SUBCKT SG7805  1       2       3
*               in      out     gnd
*
DZ1     4 1 DZ1
.MODEL DZ1 D (BV=1.5 NBV=0.01)
RQ      4 17 112090
RR      17 18 4.7
DZR     16 18 DZR
.MODEL DZR D (BV=1.2651 NBV=0.01)
RZR     16 18 1MEG
L1      16 3 .796M
EP      22 3 17 15 300
RO      22 6 25
DC-     3 6 DCLAMP
DC+     6 19 DCLAMP
.MODEL DCLAMP D
V+      19 23 DC -1
E+      23 3 1 3 1
RP      6 7 50
CP      7 3 .5U
GB      1 9 17 3 .5002M
DBL     9 8 DBL
.MODEL DBL D (IS=1E-4 EG=0 XTI=0)
EB      8 3 7 3 2
RC      1 14 .2
DC      14 13 DC
.MODEL DC D(N=1.617)
RB      9 11 100
QP      13 11 5 QP
.MODEL QP NPN (BF=70K VAF=150 IS=1E-12)
DCL     9 10 DCL
.MODEL DCL D (N=2 IS=1E-4)
QCL     10 20 12 QLIMIT
.MODEL QLIMIT NPN (BF=100)
RSC     5 12 .275
RBCL    20 5 1600
```

```
RFBCL   1 21 62.196K
DZFB    20 21 DZFB
.MODEL DZFB D (BV=15.26 NBV=.01)
RQUIES  12 3 3396
R23     15 3 600
R24     12 15 1800
ROUT    12 2 0.036
DDIS    2 1 DMOD
.MODEL DMOD D (N=0.7)
.ENDS SG7805
```

3.5 MODELING THE SG7805 AT -55 AND 125 DEGREES

It is desired to produce models which work at -55 degrees and 125 degrees. These will be ambient models. It would be most desirable to have a model which predicted behavior throughout the entire range of temperatures, however this is not possible yet at this time. Instead, the extremes of -55°C and 125°C are used. These temperatures, along with room temperature, provide an adequate range of temperatures which the device can be swept through. Of course, the chip does not always work at ambient temperature. The model is set up so that the user must figure out the junction temperature of the chip, and add the .TEMP statement into the PSpice input file for the circuit which will be simulated.

3.5.1 Strategy in Modeling the SG7805 Temperature Variations

The problem in modeling for different ambient temperatures is that certain parameters in PSpice have an automatic and preset dependance on temperature. One value is IS. Note also that VT exhibits a change with temperature since

$$VT \triangleq \frac{kT}{q}, \tag{3.31}$$

where q is the charge of the electron and k is Boltzman's constant. Using a value of

1.60218e-19 for q and a value of 1.38066e-23 for k gives values for VT of 0.0188V and 0.0343V at temperatures of -55°C and 125°C, respectively. Then parameters NBV, VAF, BF, and N for the diodes and transistors can not be made temperature dependent in PSpice. Finally, it is of importance to note that IS for the diodes and transistors exhibits the following temperature dependance

$$IS(T) = IS e^{\left(\frac{T}{T_{nom}} - 1\right)\frac{EG}{NVT}} \left(\frac{T}{T_{nom}}\right)^{\frac{XTI}{N}}. \tag{3.32}$$

Fortunately BV for the diodes can show second order temperature dependance by specifying the parameters TBV1 and TBV2. This gives BV a temperature dependance in accordance with the following equation,

$$BV(T) = BV_{NOM}(1 + TBV1(\Delta T) + TBV2(\Delta T)^2), \tag{3.33}$$

where BV_{NOM} is the value of BV at the nominal temperature which is 27° by default in PSpice.

Other temperature dependent elements are the resistors, capacitors, and diodes. These follow a temperature dependance much like the parameter BV, and these are

$$R(T) = R_{NOM}(1 + TC1(\Delta T) + TC2(\Delta T)^2), \tag{3.34}$$

$$C(T) = C_{NOM}(1 + TC1(\Delta T) + TC2(\Delta T)^2), \tag{3.35}$$

$$\text{and } L(T) = L_{NOM}(1 + TC1(\Delta T) + TC2(\Delta T)^2). \tag{3.36}$$

for the resistors, capacitors and inductors.

The following strategy is used in developing temperature dependent models. The room temperature model is developed first. The design procedure for an ambient temperature is almost identical to that of the room temperature model. The steps which need modifications are steps 4, 5, 6, 7, 8, 10, 13, 18, 19, 20, and 22. These will give rise to new values for BV_{DZ1}, BV_{DZR}, R_Q, R_R, L_1, C_P, R_{QUIES}, R_{SC}, BV_{DZFB}, R_{FB}, and R_O. Selection of these values gives remarkable temperature predictions for the lab results of interest. Lab data is taken and the above parameters are selected. Most generally, there are three values, one for each temperature, for each of the parameters. Next, the temperature coefficients of these parameters must be determined from these values. Consider BV(T) in Eqn. (3.33). Note from Eqn. (3.33) that

$$\frac{BV(T)}{BV_{NOM}} = (1 + TBV1\,(\Delta T) + TBV2\,(\Delta T)^2). \tag{3.37}$$

This leads to the following system of equations with two unknowns, setting TNOM = 25°C:

$$\begin{pmatrix} \frac{BV(-55)}{BV_{NOM}} \\ \frac{BV(125)}{BV_{NOM}} \end{pmatrix} = \begin{pmatrix} -80 & 6400 \\ 100 & 10000 \end{pmatrix} \begin{pmatrix} TBV1 \\ TBV2 \end{pmatrix}. \tag{3.38}$$

This can be solved to find the values of TBV1 and TBV2. The passive component temperature coefficients can be solved in this same manner. Once these coefficients have been determined, they can be inserted into the room temperature macromodel which then becomes a model which is accurate between the temperatures of -55°C and 125°C.

3.5.2 Design Example to Include Temperature Dependance

In this section the parameters for the model for -55°C and 125°C are developed. The temperature coefficients will be determined and then inserted into the room temperature model. This represents the fully developed, macromodel for the SG7805.

Following the format of the first example for the -55 degree portion:

4) Based on the V_{OUT} vs V_{IN} measurement, BV_{DZ1} = 1.5V.

5) V_{OUT} = 4.875V, then BV_{DZR} = 1.2269V.

6) Based on the IQ vs V_{IN} measurement, R_Q = 77320Ω.

7) RR_{LF} = 71.283db = .272793m and r_{DZR} = 2.07Ω,
then R_R = 3.2382Ω.

8) $P1_{RR}$ = 1192Hz so L_1 = .70875mH.

10) By iteration, C_P = .5uF.

13) The value of the quiescent current at the point where regulation is achieved is 4.58mA. This gives R_{QUIES} = 2537Ω.

18) From the short circuit current measurement, ISC = 3.5A,
then R_{SC} = .2499Ω.

19) From the short circuit current measurement, the point at which foldback occurs is 17.87V, then BV_{DZFB} = 17.87V.

20) From the short circuit current measurement, the point V_{DIFF} = 32.5V and I_{MAX} = 1A was selected, then R_{FB} = 35855.93Ω.

22) Based on the low frequency, no load, output impedance vs frequency measurement, R_O = 0.025Ω.

This concludes the design procedure for the -55 degree temperature macromodel for the SG7805.

Doing the same for the 125 degree model:

4) Based on the V_{OUT} vs V_{IN} measurement, BV_{DZ1} = 1V.

5) V_{OUT} = 4.994V, then BV_{DZR} = 1.2568V.

6) Based on the IQ vs V_{IN} measurement, R_Q = 145596.6Ω.

7) RR_{LF} = 69.06db = .3524m and r_{DZR} = 6.85Ω,

then R_R = 6.0626Ω.

8) $P1_{RR}$ = 1900Hz, so L_1 = 1.0816mH.

10) By iteration, C_P = .5uF.

13) The value of the quiescent current at the point where regulation is achieved is 3.406mA. This gives R_{QUIES} = 7315.27Ω.

18) From the short circuit current measurement, ISC = 1.762A,

then R_{SC} = .3526Ω.

19) From the short circuit current measurement, the point at which foldback occurs is 16.06V, then BV_{DZFB} = 16.06V.

20) From the short circuit current measurement, the point V_{DIFF} = 31.79V and I_{MAX} = .53A was selected, then R_{FB} = 56346.548Ω.

22) Based on the low frequency, no load, output impedance vs frequency measurement, R_O = 0.04Ω.

23) Set EG_{DBL} = 0eV.

Set XTI_{DBL} = 0.

These are set to zero because it was determined by PSpice simulation that the dependance of IS_{DBL} on temperature was causing problems in the 125 degree simulations. Specifically, IS_{DBL} gets very high when the nominal value is set at 1e-4A. This allows E_B to supply currents equal

to this saturation current, which were unacceptable. Setting these parameters to 0 renders IS_{DBL} nearly temperature independent.

A final summary of the temperature dependent parameters and elements follows.

element or parameter	value at 25 degrees	value at -55 degrees	value at 125 degrees
BV_{DZ1}	1.5	1.5	1
BV_{DZR}	1.2651	1.2269	1.2568
R_Q	112090	77320	145596.6
R_R	4.7	3.238	6.0626
L_1	.796m	.708753m	1.086m
R_{QUIES}	3396	2537.12	7315.27
R_{SC}	.275	.25	.3526
BV_{DZFB}	15.26	17.87	16.06
R_{FB}	62196	35855.03	56346.55
R_O	0.036	0.025	0.04

Table 3.1 Temperature dependent components and parameters

Sc

El

pa

B

B

R

R

L

R

R

B

R

Solving for the linear and quadratic coefficients gives Table (3.2).

element or **parameter**	**TC1** or **TBV1** (linear coeff.)	**TC2** or **TBV2** (quadratic coeff.)
BV_{DZ1}	-0.001481	-1.85167e-5
BV_{DZR}	1.805303e-4	-2.4614e-6
R_Q	0.003483	-4.9343e-6
R_R	.003449	-5.4953e-6
L_1	0.00238	1.26281e-5
R_{QUIES}	0.006886	4.655264e-5
R_{SC}	0.001885	9.3636e-6
BV_{DZFB}	-9.547473e-4	1.478994e-5
R_{FB}	0.002523	-3.4635e-5
R_O	0.002616	-1.50463e-5

Table 3.2 Temperature coefficients

The final SG7805 macromodel is:

```
.SUBCKT SG7805  1       2       3
*               in      out     gnd
*
DZ1     4 1 DZ1
.MODEL DZ1 D (BV=1.5 NBV=0.01)
RQ      4 17 112090 TC=.003483,-4.9343E-6
RR      17 18 4.7 TC=.003449,-5.495E-6
DR      16 18 DR
.MODEL DR D (BV=1.2651 NBV=0.01 TBV1=1.805303E-4 TBV2=-2.461378E-6)
L1      16 3 IND1 .796M
.MODEL IND1 IND (TC1=.00238 TC2=1.262851E-5)
EP      22 3 17 15 300
RO      22 6 25
DC-     3 6 DCLAMP
DC+     6 19 DCLAMP
.MODEL DCLAMP D
```

W
E
R
C
G
D
M
EB
RC
DC
MC
RB
QP
MC
DC
MC
QC
MC
RSC
REC
RFB
DLF
MOD
RQU
R23
R24
ROU
DIS
MOD
END

```
V+    19 23 DC -1
E+    23 3 1 3 1
RP     6 7 50
CP    7 3 .5U
GB     1 9 17 3 .5002M
DBL    9 8 DBL
.MODEL DBL D (IS=1E-4 EG=0 XTI=0)
EB     8 3 7 3 2
RC     1 14 .2
DC    14 13 DC
.MODEL DC D(N=1.617)
RB     9 11 100
QP     13 11 5 QP
.MODEL QP NPN (BF=70K VAF=150 IS=1E-12)
DCL    9 10 DCL
.MODEL DCL D (N=2 IS=1E-4)
QCL    10 20 12 QLIMIT
.MODEL QLIMIT NPN (BF=100)
RSC    5 12 .275 TC=.001885,9.363636E-6
RBCL   20 5 1600
RFBCL  1 21 62.196K TC=.002523,-3.4635E-5
DZFB   20 21 DZFB
.MODEL DZFB D (BV=15.26 TBV1=-9.5474743E-4 TBV2=1.478994E-5 NBV=.01)
RQUIES  12 3 3396 TC=.006886,4.655264E-5
R23    15 3 600
R24    12 15 1800
ROUT   12 2 0.036 TC,=.002616,-1.50463E-5
DDIS   2 1 DMOD
.MODEL DMOD D (N=0.7)
.ENDS SG7805
```

3.5.3 Comparison of Macromodel Predictions with Lab Results

A comparison of macromodel predictions with lab results are presented for the SG7805 in this section.

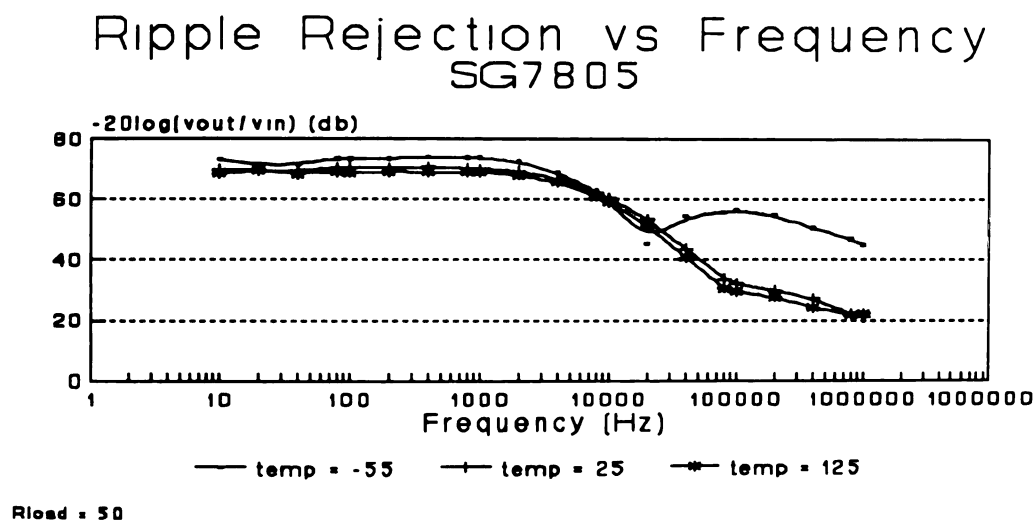

Figure 3.10 Ripple rejection vs frequency, measured

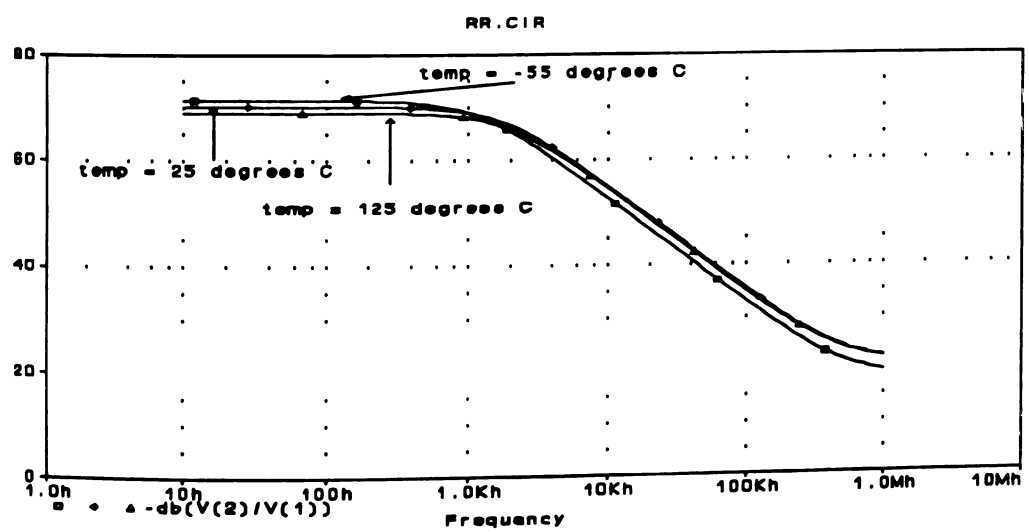

Figure 3.11 Ripple rejection vs frequency, macromodel

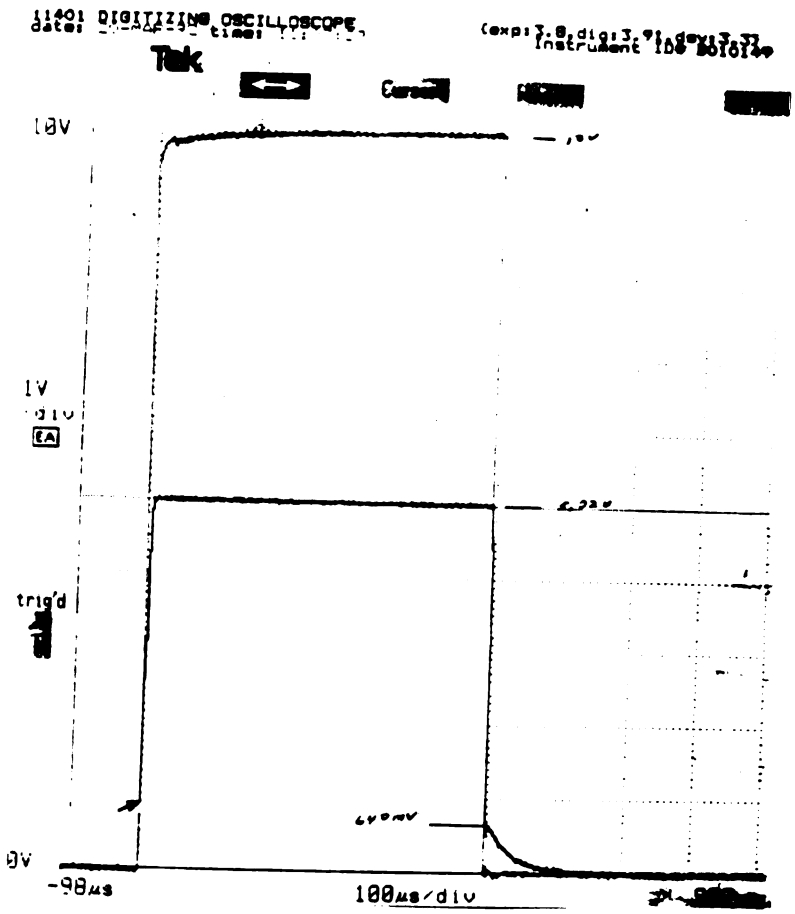

Figure 3.12 Power up and down, square wave, measured

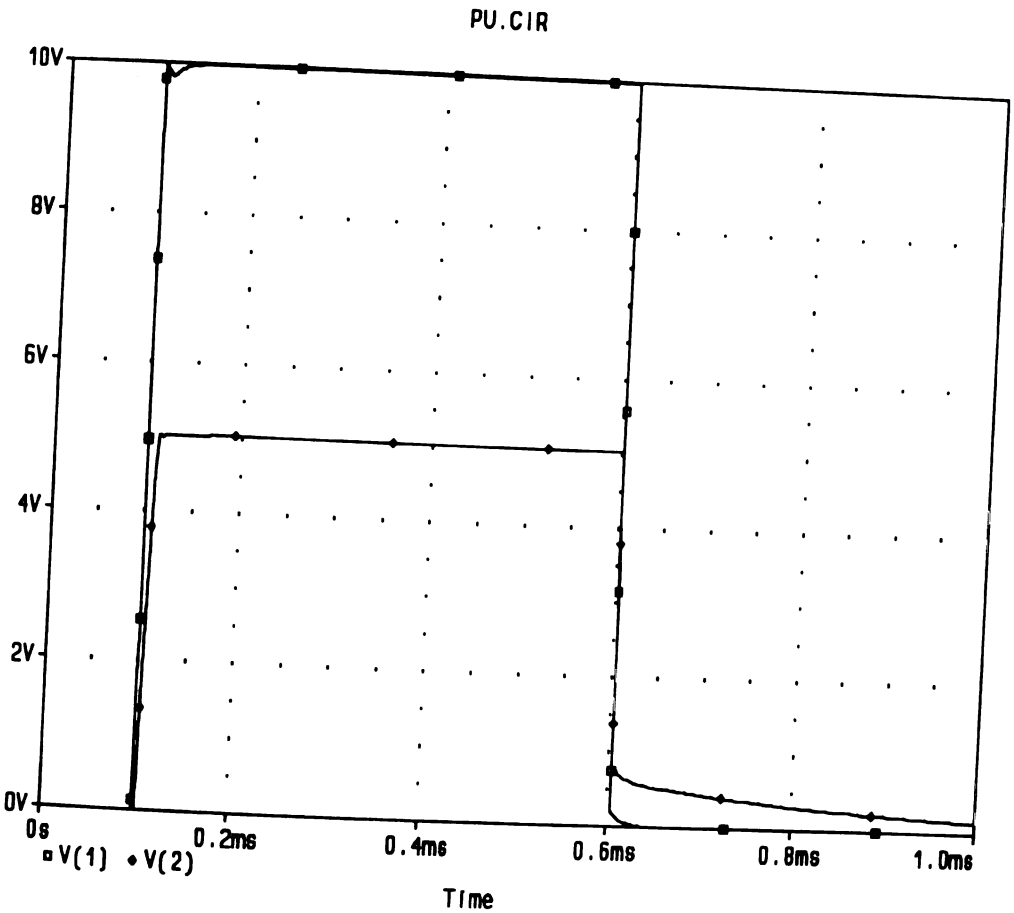

Figure 3.13 Power up and down, square wave, macromodel

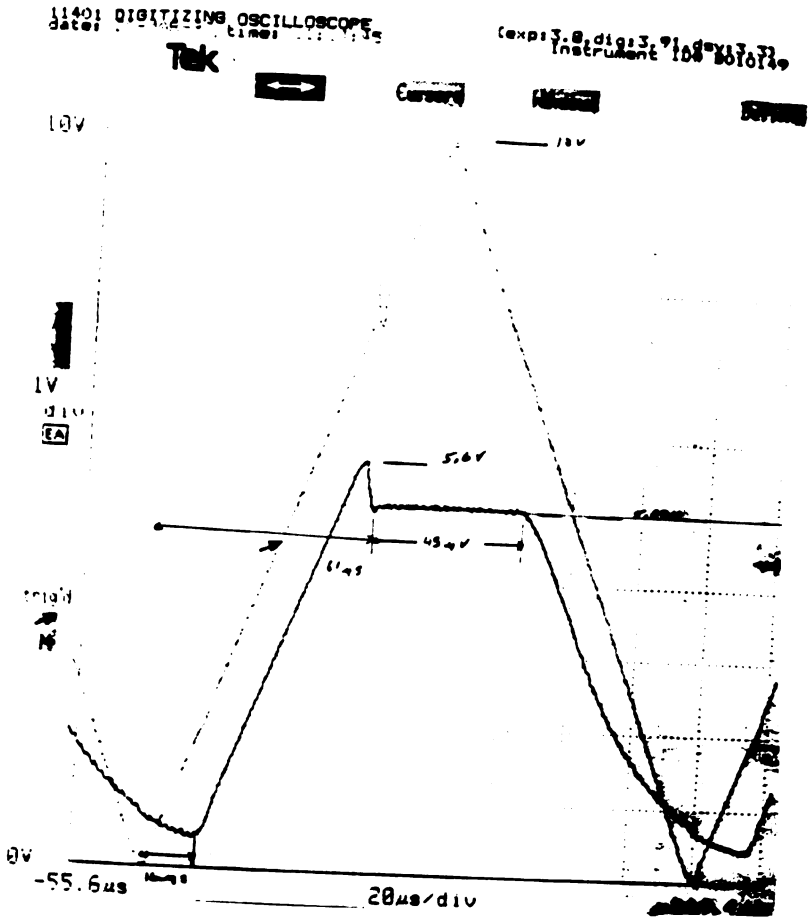

Figure 3.14 Power up and down, triangle wave, measured

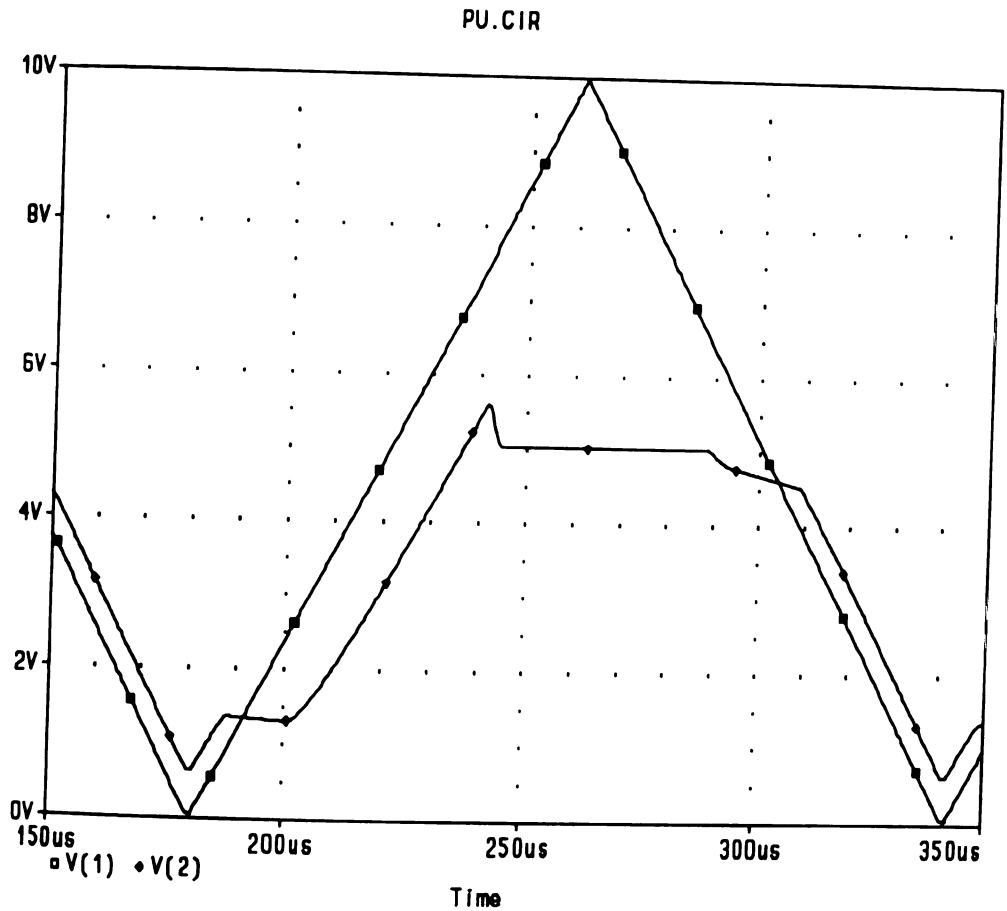

Figure 3.15 Power up and down, triangle wave, macromodel

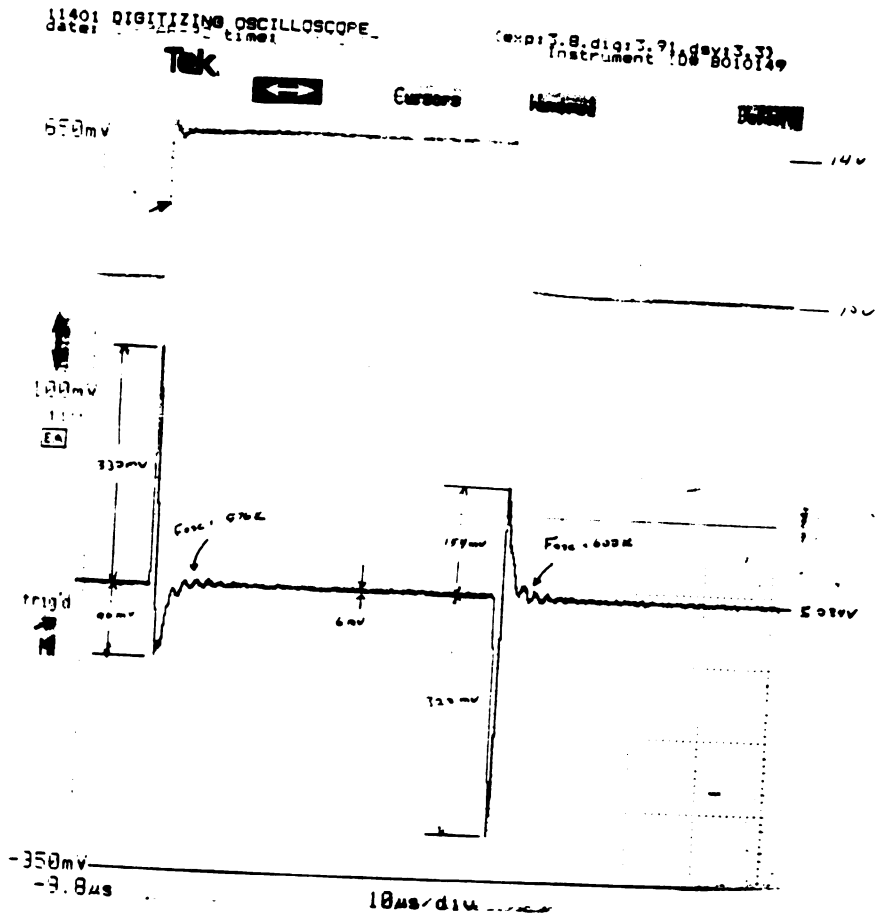

Figure 3.16 Line transient response, measured

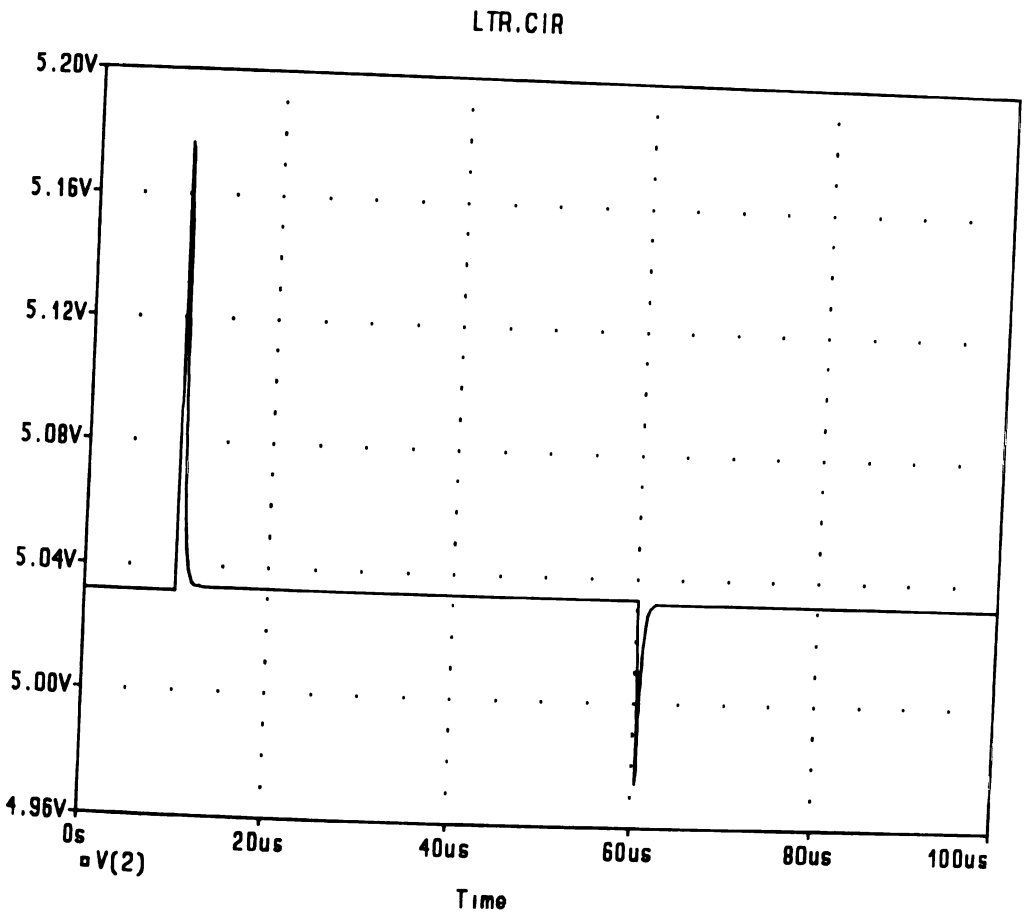

Figure 3.17 Line transient response, macromodel

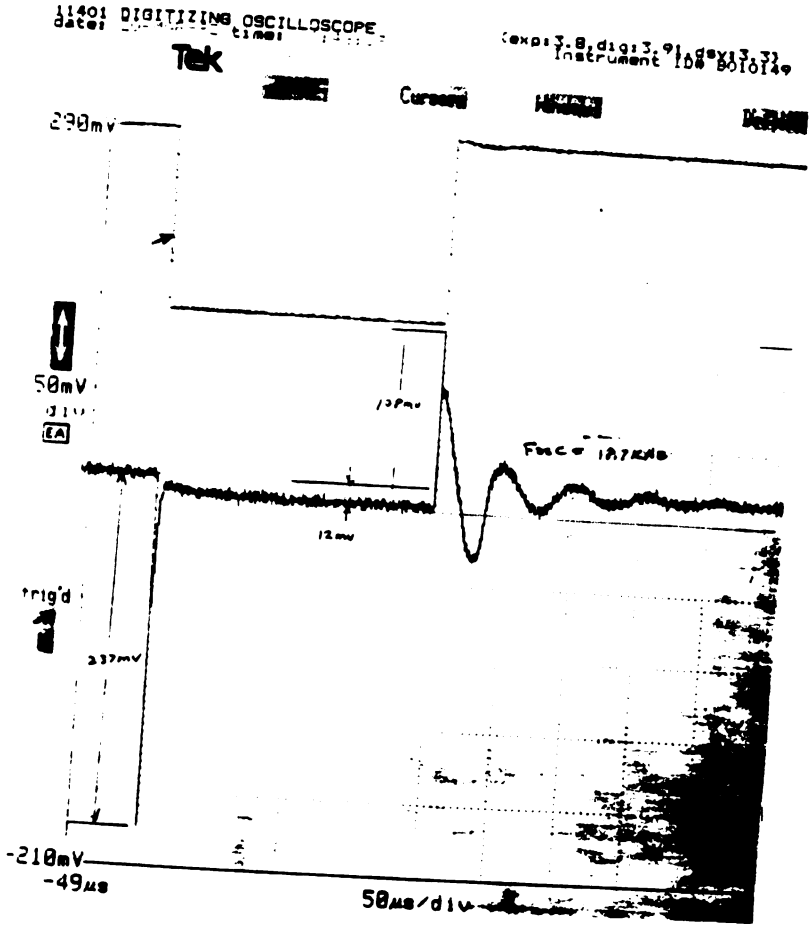

Figure 3.18 Load transient response, measured

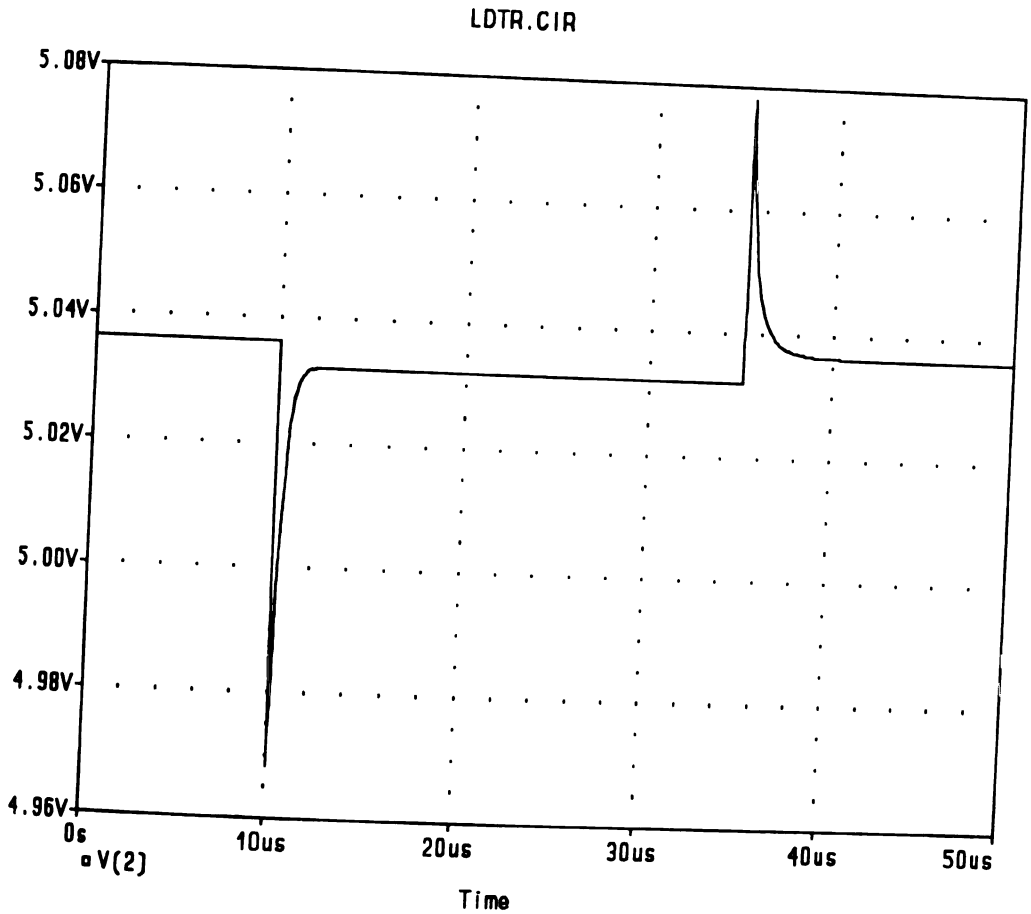

Figure 3.19 Load transient response, macromodel

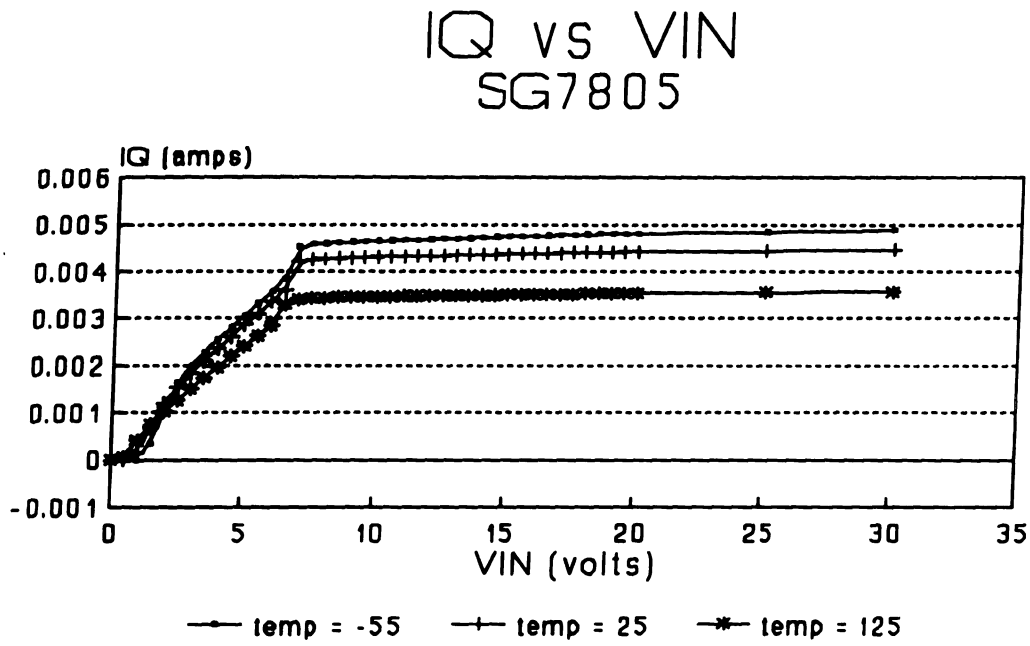

Figure 3.20 Quiescent current vs input voltage, measured

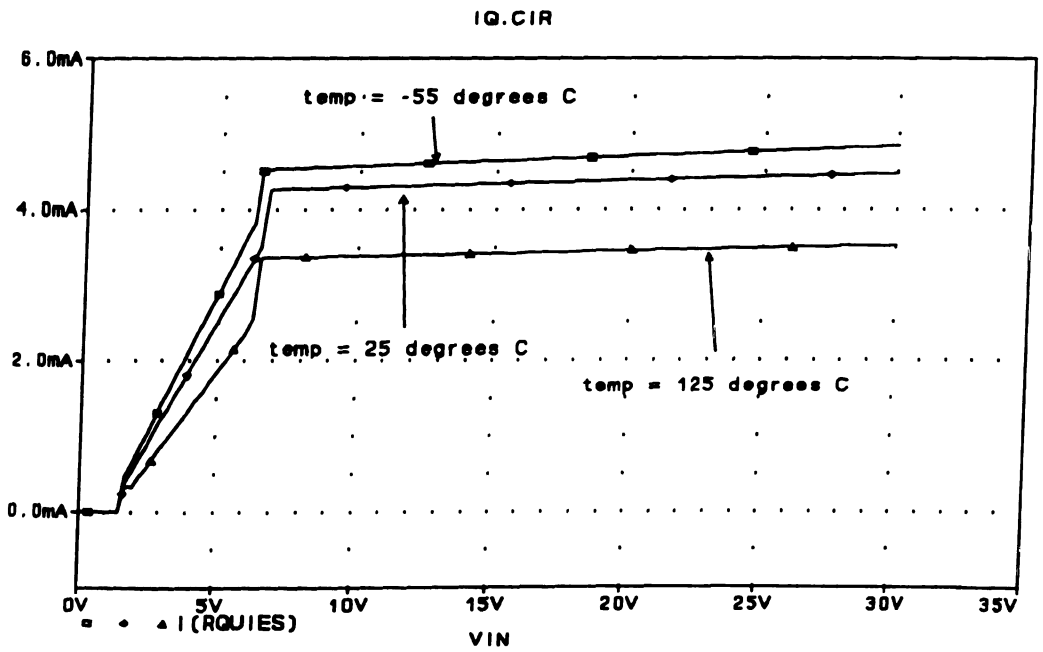

Figure 3.21 Quiescent current vs input voltage, macromodel

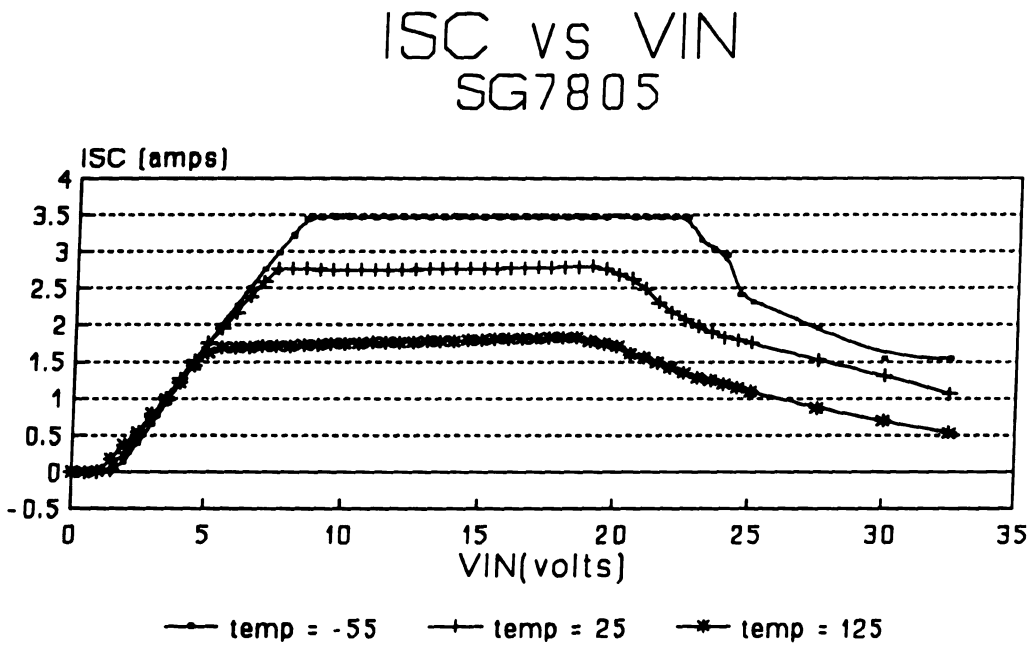

Figure 3.22 Maximum output current vs input voltage, measured

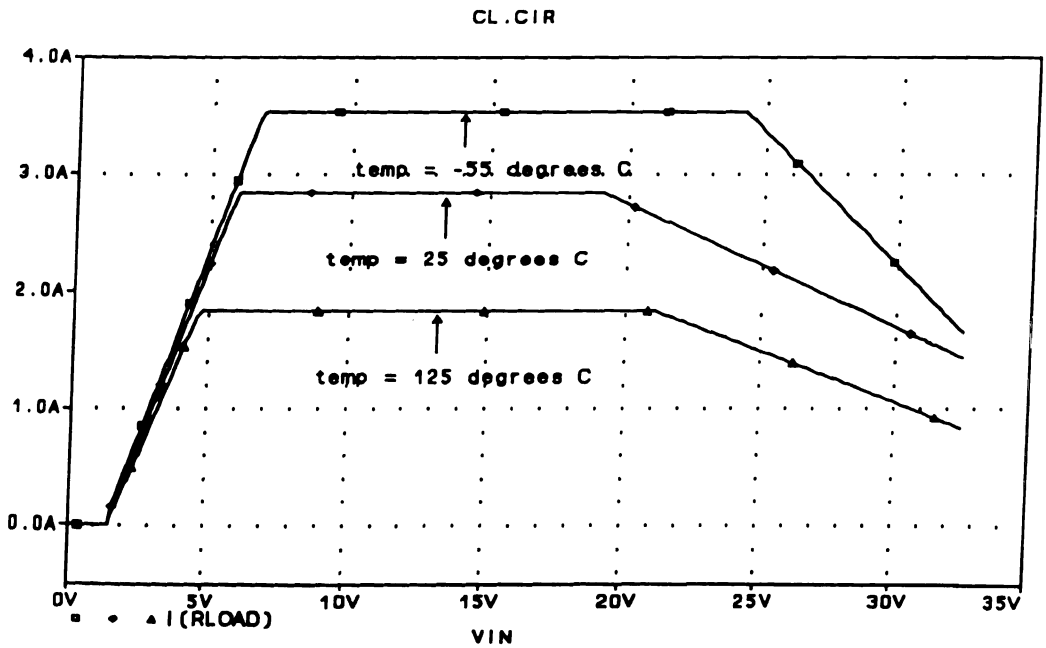

Figure 3.23 Maximum output current vs input voltage, macromodel

Comparison of Macromodel parameters and Measured Parameters				
QUANTITY		**-55°C**	**25°C**	**125°C**
RR_{LF}	lab	71.3db	70.0db	69.1db
	model	71.4db	70.3b	69.0db
$P1_{RR}$	lab	1.192kHz	1.785kHz	1.900kHz
	model	1.176kHz	1.760kHz	1.941kHz
IQ	lab	4.58mA	4.22mA	3.41mA
	model	4.53mA	4.27mA	3.36mA
$\Delta IQ/\Delta V_{IN}$	lab	12.93u	8.92u	6.87u
	model	13.29u	9.19u	7.08u
max output current	lab	3.50A	2.84A	1.76A
	model	3.53A	2.84A	1.84A
dropout voltage	lab	1.88V	1.59V	1.16V
	model	1.40V	1.46V	1.50V
R_{OUT}	lab	0.0250Ω	0.036Ω	0.04Ω
	model	0.0275Ω	0.0392Ω	0.0446Ω

Table 3.3 Macromodel comparisons with lab data, SG7805

3.6 DEVELOPMENT OF THE SG7812 VOLTAGE REGULATOR MACROMODEL

In the actual chip, the topology of the SG7812 voltage regulator is identical to the SG7805 voltage regulator, with the exception of one value of one of the feedback resistors, R_{23}, being changed to produce an output voltage of 12V instead of 5V. It makes sense if the same feedback resistor R_{23} is varied in the macromodel to produce a 12V output, that this can now be used for the macromodel for the SG7812. This is the case, and in fact helps verify the correctness of the macromodeling methodologies which were used in developing the SG7805. It is only necessary to change the feedback resistor R_{23} and use the procedure developed in section 3.4.1 to create the macromodel for the SG7812. Section 3.5.2 is then be duplicated to include the effects of ambient temperature. Finally, lab results are be compared against the macromodel predictions.

3.6.1 Development of the Room Temperature Macromodel for the SG7812

As stated before, the procedure used in section 3.4.1 is used to develop the macromodel for the SG7812. The design procedure for the room temperature model follows.

1) Set $E_A = 300$, $E_B = 2$, then $A_{DC} = 600$.

2) Set $R_{23} = 5160\Omega$ and $R_{24} = 600\Omega$.

3) Set $R_{OUT} = 10\Omega$, $V_+ = -1V$ and $E_+ = 1$. Let the diodes D_+ and D_- have the PSpice default values for their parameters. This means that $V_{MAX} = (V_{VIN} - 0.3)V$ and $V_{MIN} = -0.7V$ if the voltage drops across the diodes are taken as 0.7V.

4) Based on the V_{OUT} vs V_{IN} measurement, BV_{DZ1} = .75V.

Select NBV_{DZ1} = 0.01 and R_{ZR} = 1MEGΩ.

5) V_{OUT} = 11.894V, then BV_{DZR} = 1.2588V.

Set NBV_{DZR} = 0.01.

6) Based on the IQ vs V_{IN} measurement, R_Q = 86343.84Ω.

7) RR_{LF} = 62.8464db = .7206m and r_{DZR} = 1.34Ω,

then R_R = 5.2447Ω.

8) $P1_{RR}$ = 2933Hz so L_1 = .3573mH

9) Set R_P = 500Ω.

10) By iteration, C_P = .1uF.

11) By iteration, N_{DIS} = 0.7.

12) The jump in the IQ vs V_{IN} measurement is .6223mA, then g_B = .4944m.

13) The value of the quiescent current at the point where regulation is achieved is 3.8945mA. This gives R_{QUIES} = 10572.61Ω.

14) Set IS_{QP} = 1e-12A, BF_{QP} = 70k, and VAF_{QP} = 150.

15) Set R_B = 100Ω.

16) Set BF_{CL} = 100.

17) Set R_{BCL} = 200Ω.

18) From the short circuit current measurement, ISC = 1.32A,

then R_{SC} = .578Ω.

19) From the short circuit current measurement, the point at which foldback occurs is 14.79V, then BV_{DZFB} = 14.79V.

Set NBV_{DZFB} = 0.01.

20) From the short circuit current measurement, the point V_{DIFF} = 33.89V

and I_{MAX} = .2826A was selected, then R_{FB} = 6170.43Ω.

21) Set R_C = 0.2Ω. In lab, the dropout voltage for a 50Ω resistor was determined to be 1.59V, then N_{DC} = 1.6339.

22) Based on the low frequency, no load, output impedance vs frequency measurement, R_O = 0.02Ω.

23) Set IS_{DBL} = IS_{DCL} = 1e-4A.

Set N_{DBL} = 2.

3.6.2 Development of the Model for -55°C and 125°C.

The following gives the model for -55°C:

4) Based on the V_{OUT} vs V_{IN} measurement, BV_{DZ1} = 1.3V.

5) V_{OUT} = 11.7926V, then BV_{DZR} = 1.2481V.

6) Based on the IQ vs V_{IN} measurement, R_Q = 110497Ω.

7) RR_{LF} = 65.715db = .5179m and r_{DZR} = 1.15Ω,

then R_R = 4.9065Ω.

8) $P1_{RR}$ = 2 kHz so L_1 = .4820mH.

10) By iteration, C_P = .08uF.

13) The value of the quiescent current at the point where regulation is achieved is 4.276mA. This gives R_{QUIES} = 7469.5Ω.

18) From the short circuit current measurement, ISC = 1.553A,

then R_{SC} = .5634Ω.

19) From the short circuit current measurement, the point at which foldback occurs is 15.4V, then NBV_{DZFB} = 15.4V.

20) From the short circuit current measurement, the point V_{DIFF} = 33.06V and I_{MAX} = .5634A was selected, then R_{FB} = 5719.35Ω.

22) Based on the low frequency, no load, output impedance vs frequency measurement, $R_O = 0.016\Omega$.

The following gives the model for 125°C:

4) Based on the V_{OUT} vs V_{IN} measurement, $BV_{DZ1} = 1V$.

5) $V_{OUT} = 11.838V$, then $BV_{DZR} = 1.2529V$.

6) Based on the IQ vs V_{IN} measurement, $R_Q = 134495.64\Omega$.

7) $RR_{LF} = 60.0650db = .9925m$ and $r_{DZR} = 2.6\Omega$, then $R_R = 11.5274\Omega$.

8) $P1_{RR} = 3.5kHz$ so $L_1 = .6424mH$.

10) By iteration, $C_P = .08uF$.

13) The value of the quiescent current at the point where regulation is achieved is 3.0112mA. This gives $R_{QUIES} = 38992.15\Omega$.

18) From the short circuit current measurement, ISC = .8529A, then $R_{SC} = .7256\Omega$.

19) From the short circuit current measurement, the point at which foldback occurs is 15.15V, then $NBV_{DZFB} = 15.15V$.

20) From the short circuit current measurement, the point $V_{DIFF} = 34.98V$ and $I_{MAX} = 0A$ was selected, then $R_{FB} = 6208.17\Omega$.

22) Based on the low frequency, no load, output impedance vs frequency measurement, $R_O = 0.01\Omega$.

23) Set $EG_{DBL} = 0eV$ and $XTI_{DBL} = 0$.

A final summary of the temperature dependent parameters and elements follows.

elem para

element or **parameter**	**value** at **25 degrees**	**value** at **-55 degrees**	**value** at **125 degrees**
BV_{DZ1}	.75	1.3	1
BV_{DZR}	1.2588	1.2481	1.2529
R_Q	86343.84	7469.5	134495.64
R_R	5.2447	4.9065	11.5274
L_1	.3573m	.482m	.6424m
C_P	.1u	.08u	.08u
R_{QUIES}	10572.61	7469.5	38992.15
R_{SC}	.5780	.5634	.7256
BV_{DZFB}	14.79	15.4	15.15
R_{FB}	6170.43	5179.35	6208.17
R_O	0.02	0.016	0.01

Table 3.4 Temperature components and parameters

element or **parameter**	**TC1** or **TBV1** (linear coeff.)	**TC2** or **TBV2** (quadratic coeff.)
BV_{DZ1}	-0.001481	-1.85167e-5
BV_{DZR}	1.805303e-4	-2.4614e-6
R_Q	0.003483	-4.9343e-6
R_R	.003449	-5.4953e-6
L_1	0.00238	1.26281e-5
C_P	-0.002	1e-4
R_{QUIES}	0.006886	4.655264e-5
R_{SC}	0.001885	9.3636e-6
BV_{DZFB}	-9.547473e-4	1.478994e-5
R_{FB}	0.001143	-1.081421e-5
R_O	0.002616	-1.50463e-5

Table 3.5 Temperature coefficients

The full temperature dependent macromodel for the SG7812 is:

```
.SUBCKT SG7812  1       2       3
*                       in      out     gnd
DZ1     4 1 DZ1
.MODEL DZ1 D (BV=.75 NBV=0.01 TBV1=-0.003611 TBV2=6.9444E-5)
RQ      4 17 86343.84 TC=5.3597E-4,5.0408E-5
RR      17 18 5.2447 TC=0.005772,6.2073E-5
DZR     16 18 DZR
.MODEL DZR D (BV=1.2588 NBV=0.01 TBV1=3.820E-5 TBV2=-8.5068E-7)
RZR     16 18 1MEG
L1      16 3 IND1 .3573M
.MODEL IND1 IND (TC1=0.001123 TC2=6.8566E-5)
EA      22 3 17 15 300
ROUT    22 6 10
D-      3 6 DCLAMP
D+      6 19 DCLAMP
.MODEL DCLAMP D
V+      19 23 DC -1
E+      23 3 1 3 1
RP      6 7 500
CP      7 3 CAP1 .1U
.MODEL CAP1 CAP (TC1=-0.002 TC2=1E-4)
GB      1 9 17 3 .4944M
DBL     9 8 DBL
.MODEL DBL D(IS=1E-4 EG=0 XTI=0)
EB      8 3 7 3 2
RC      1 14 .2
DC      14 13 DC
.MODEL DC D(N=1.6339)
RB      9 11 100
QP      13 11 5 QP
.MODEL QP NPN (BF=70K VAF=150 IS=1E-12)
DCL     9 10 DCL
.MODEL DCL D (N=2 IS=1E-4)
QCL     10 20 12 QCL
.MODEL QCL NPN (BF=100)
RSC     5 12 .5780 TC=0.00131,1.2433E-5
RBCL    20 5 200
RFB     1 21 6.17043K TC=0.001143,-1.081421e-5
DZFB    20 21 DZFB
.MODEL DZFB D (BV=14.79 NBV=.01 TBV1=-1.78236E-4 TBV2=4.2164E-6)
RQUIES  12 3 10572.61 TC=0.013985,1.28953E-4
R24     15 3 600
R23     12 15 5160
RO      12 2 0.02 TC=-8.3333E-4,-4.1667E-5
DDIS    2 1 DMOD
.MODEL DMOD D (N=0.7)
.ENDS SG7812
```

3.6.3 Comparison of Macromodel Predictions with Lab Results

A comparison of macromodel predictions with lab results are presented in this section.

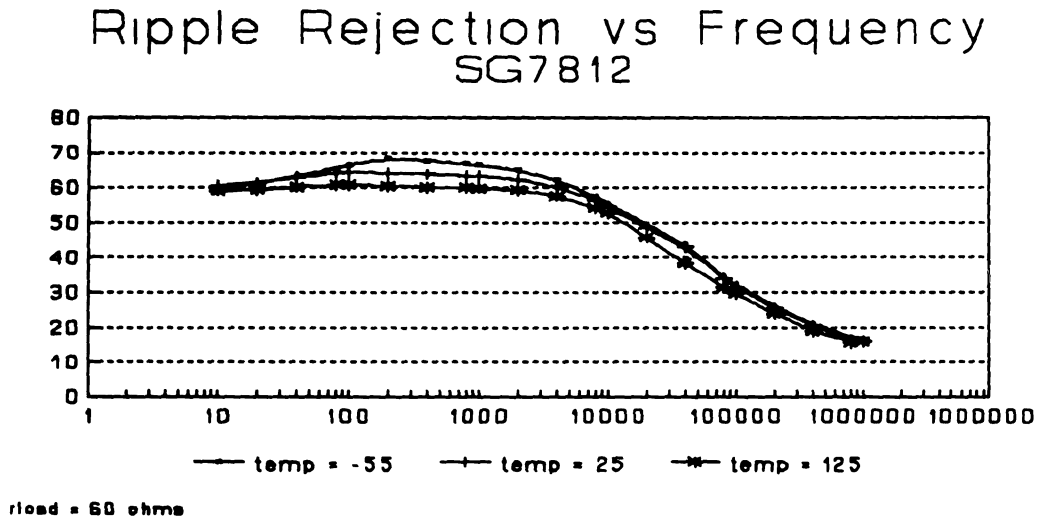

Figure 3.24 Ripple rejection vs frequency, measured

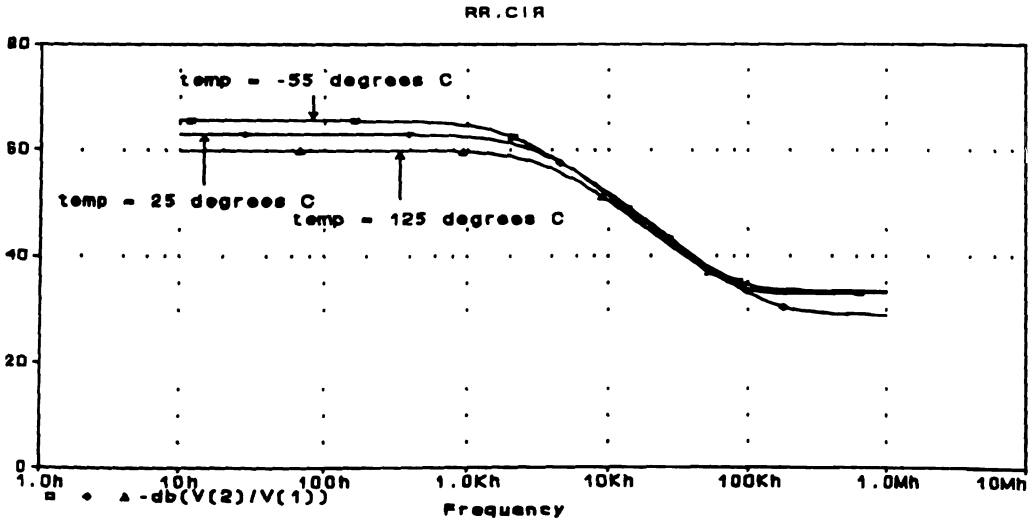

Figure 3.25 Ripple rejection vs frequency, macromodel

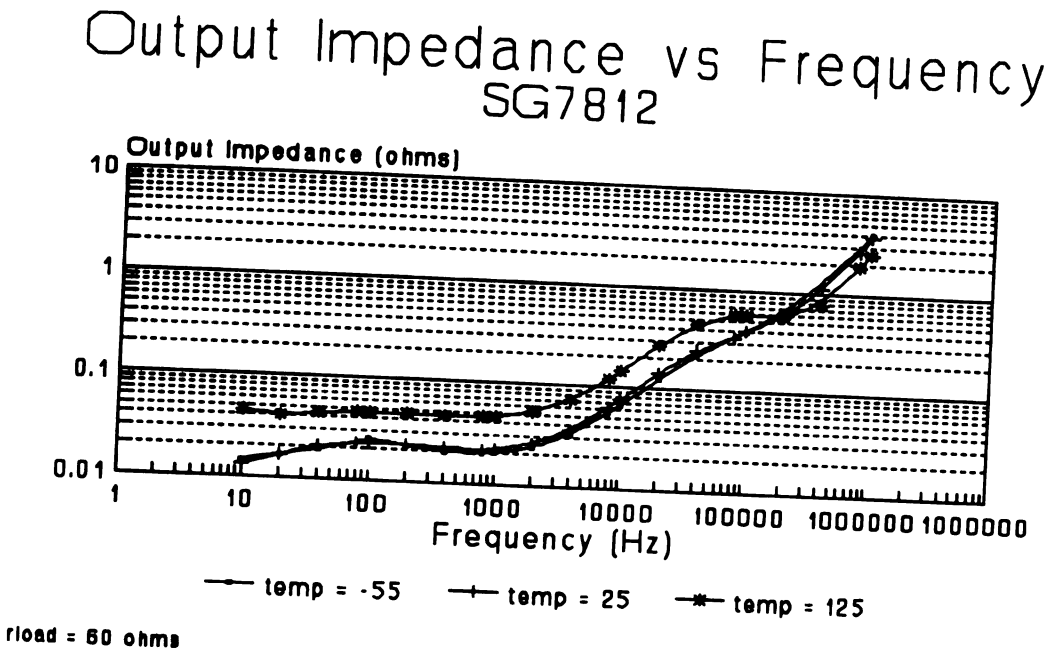

Figure 3.26 Output impedance vs frequency, measured

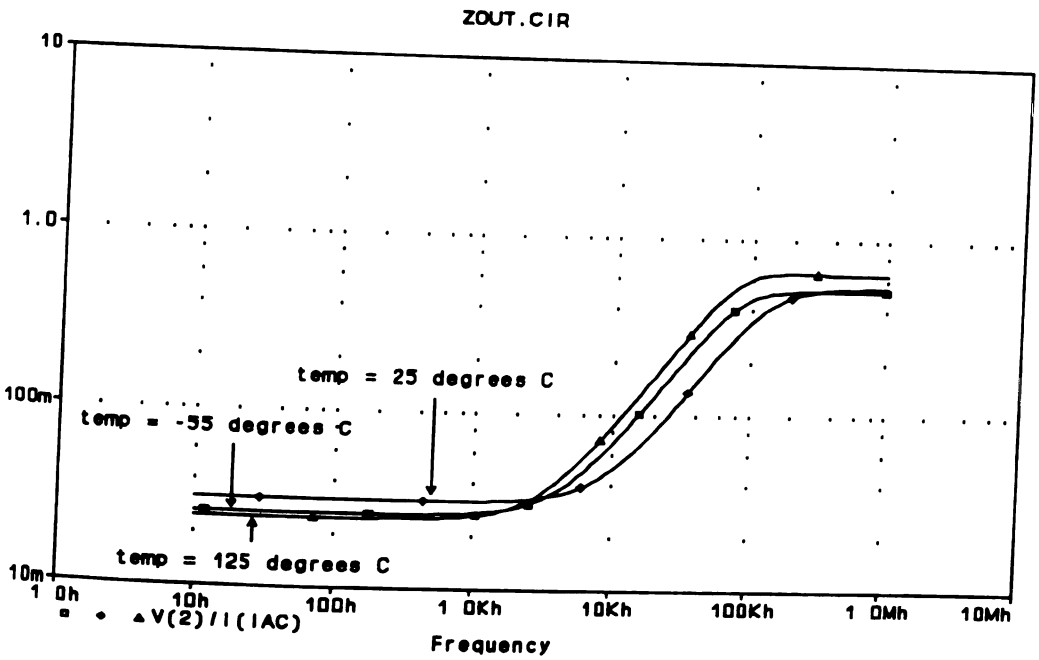

Figure 3.27 Output impedance vs frequency, macromodel

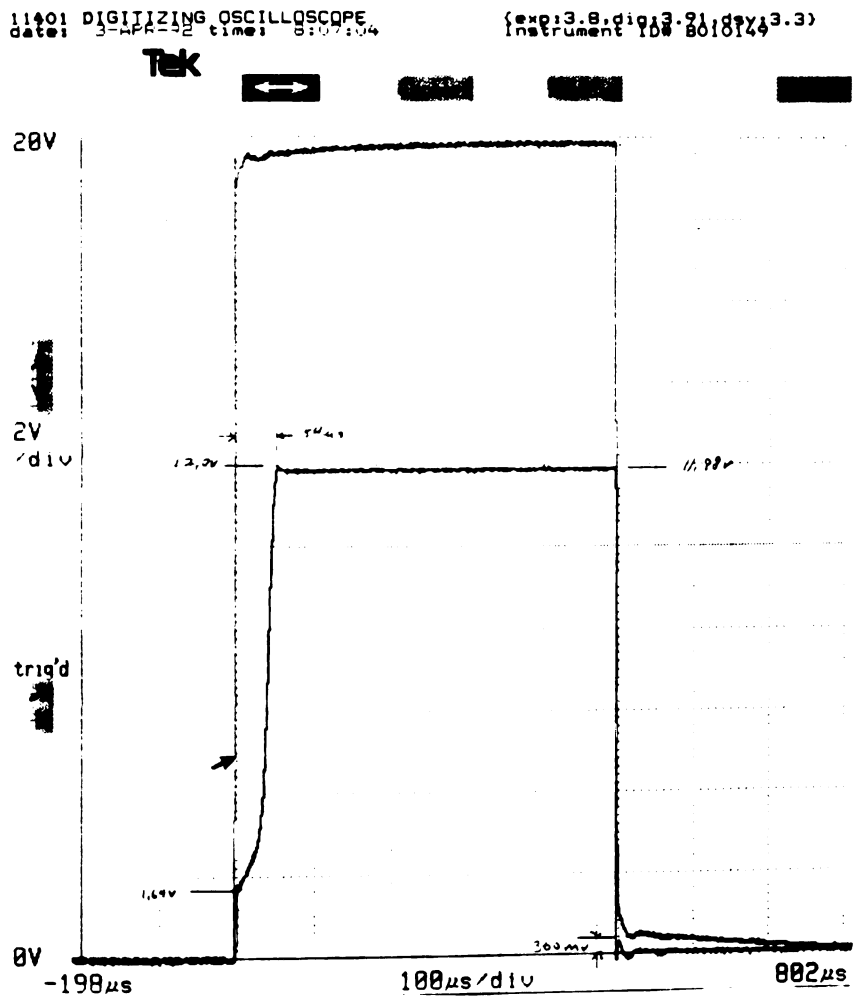

Figure 3.28 Power up and down, square wave, measured

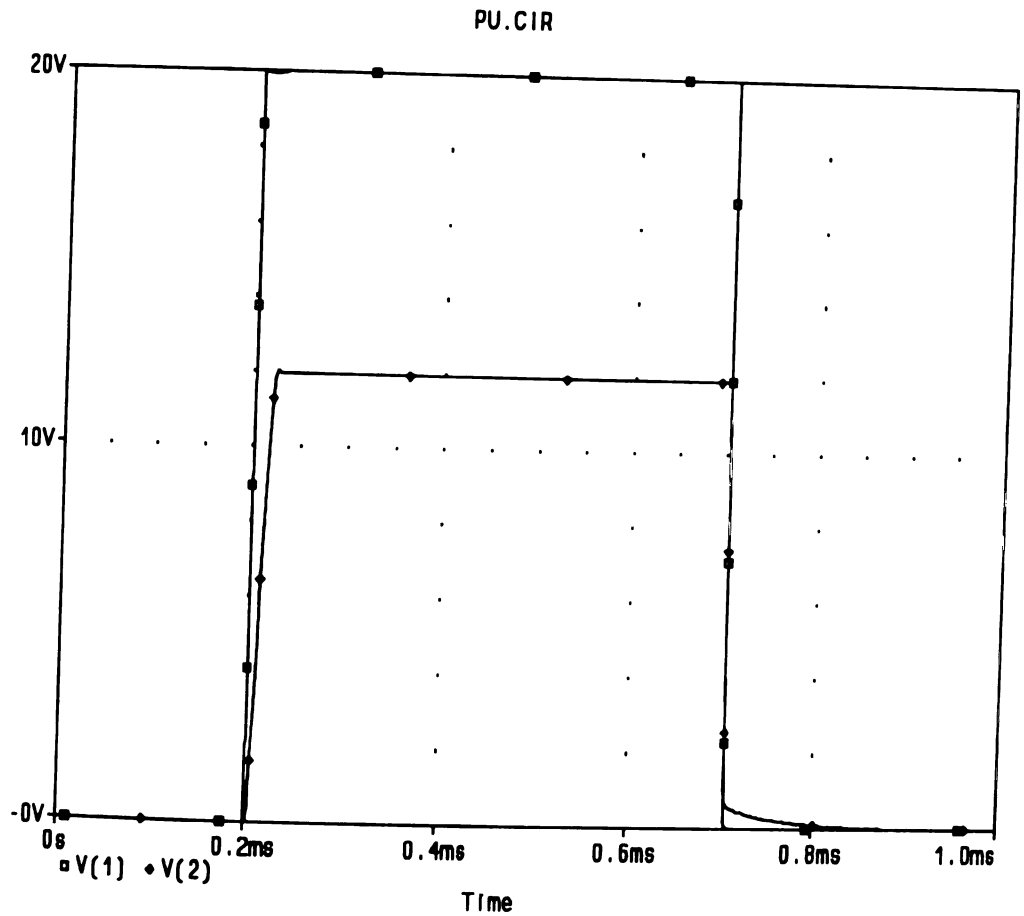

Figure 3.29 Power up and down, square wave, macromodel

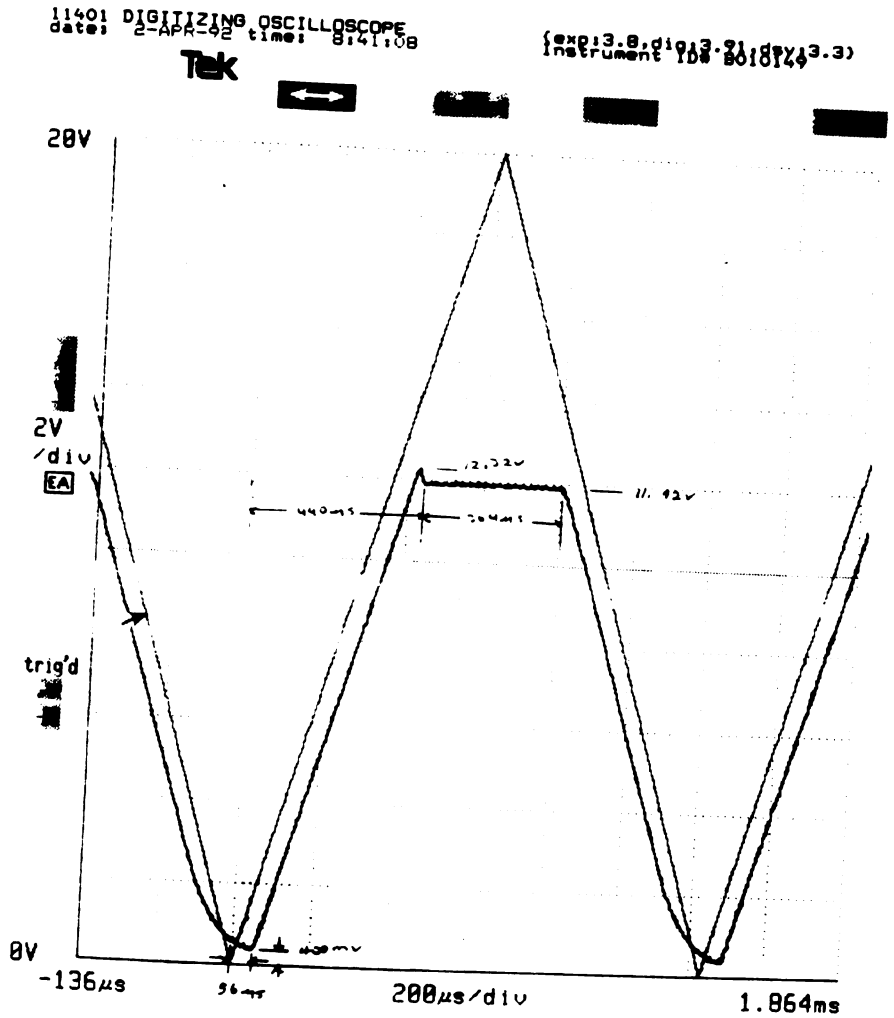

Figure 3.30 Power up and down, triangle wave, measured

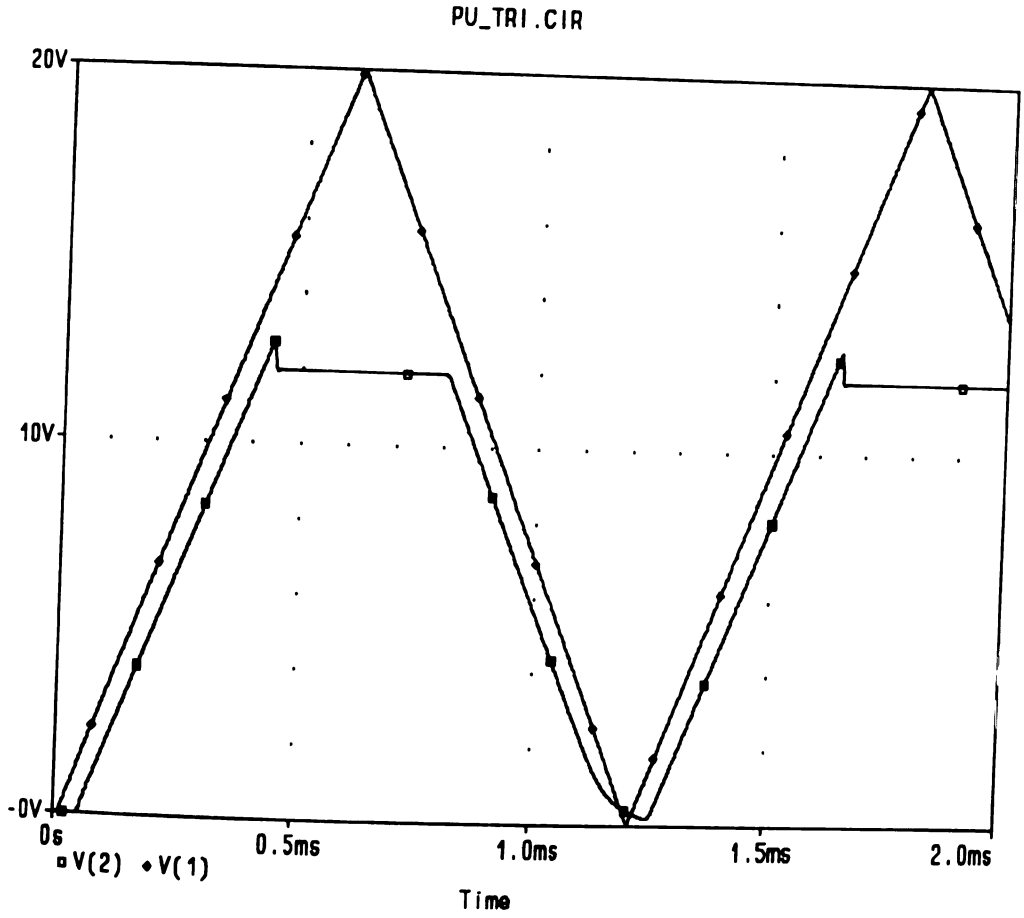

Figure 3.31 Power up and down, triangle wave, macromodel

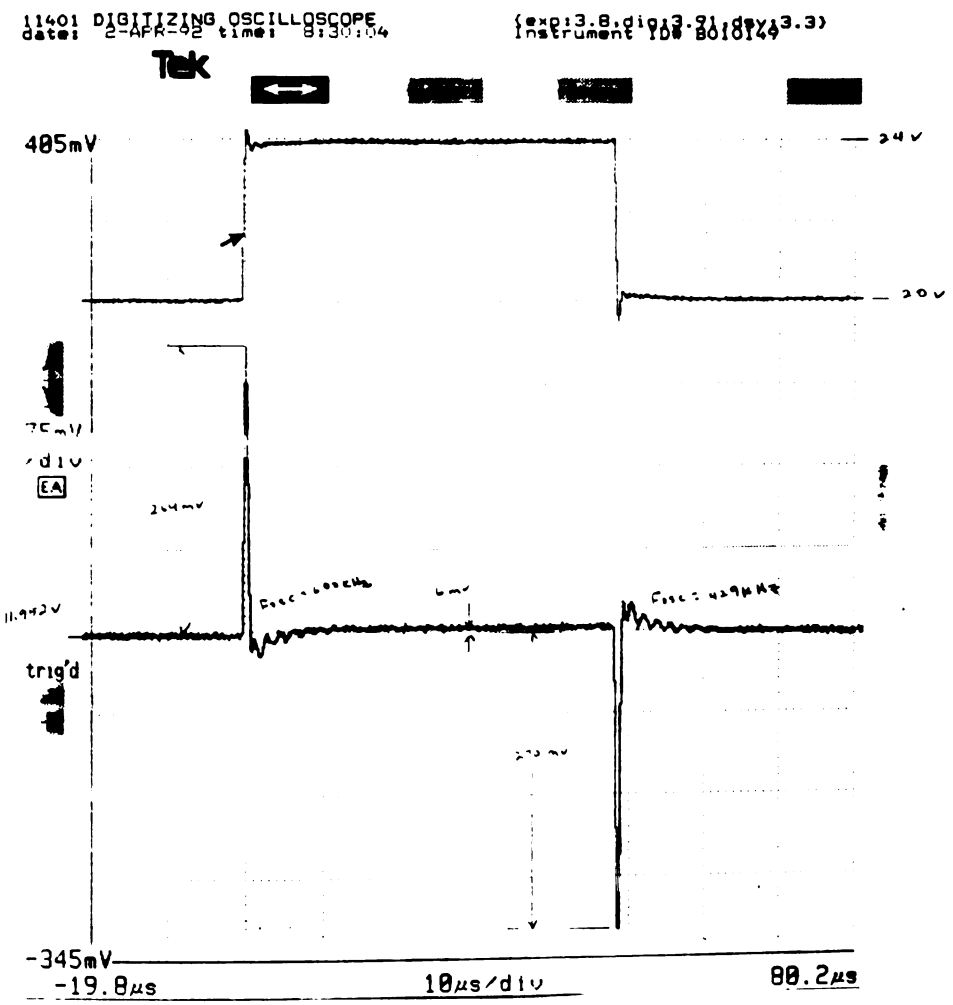

Figure 3.32 Line transient response, measured

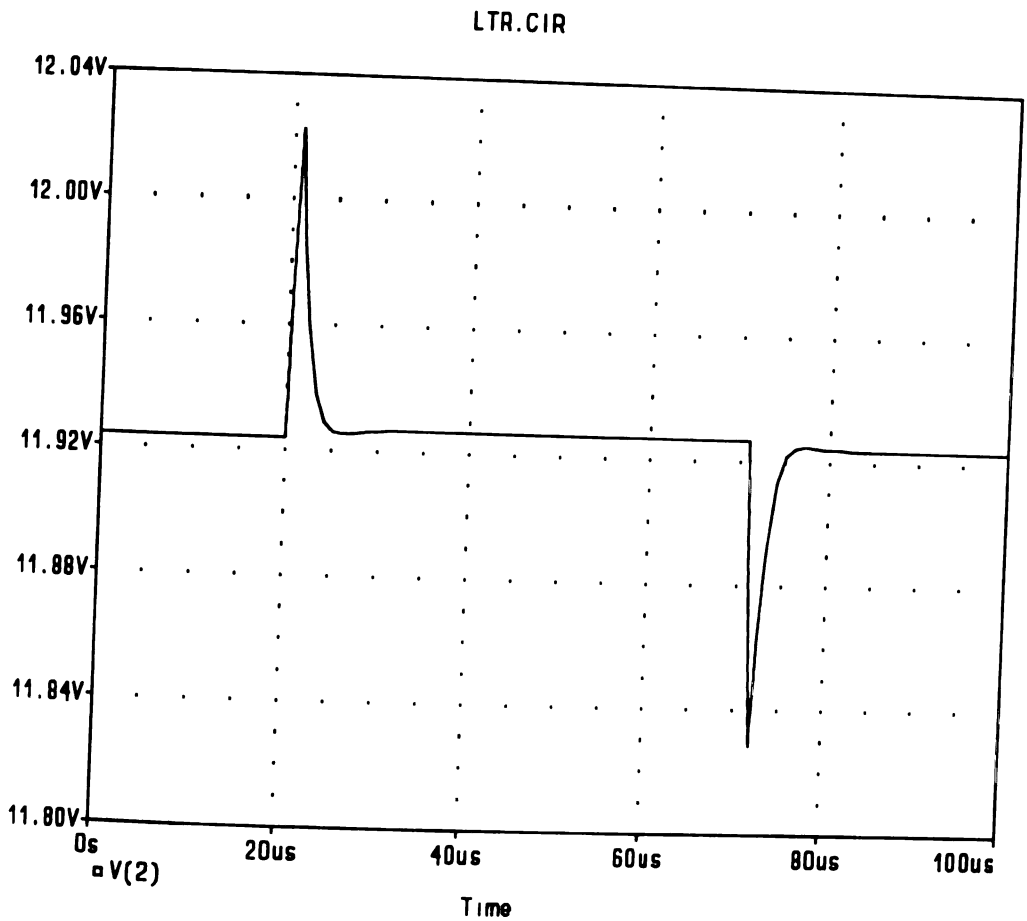

Figure 3.33 Line transient response, macromodel

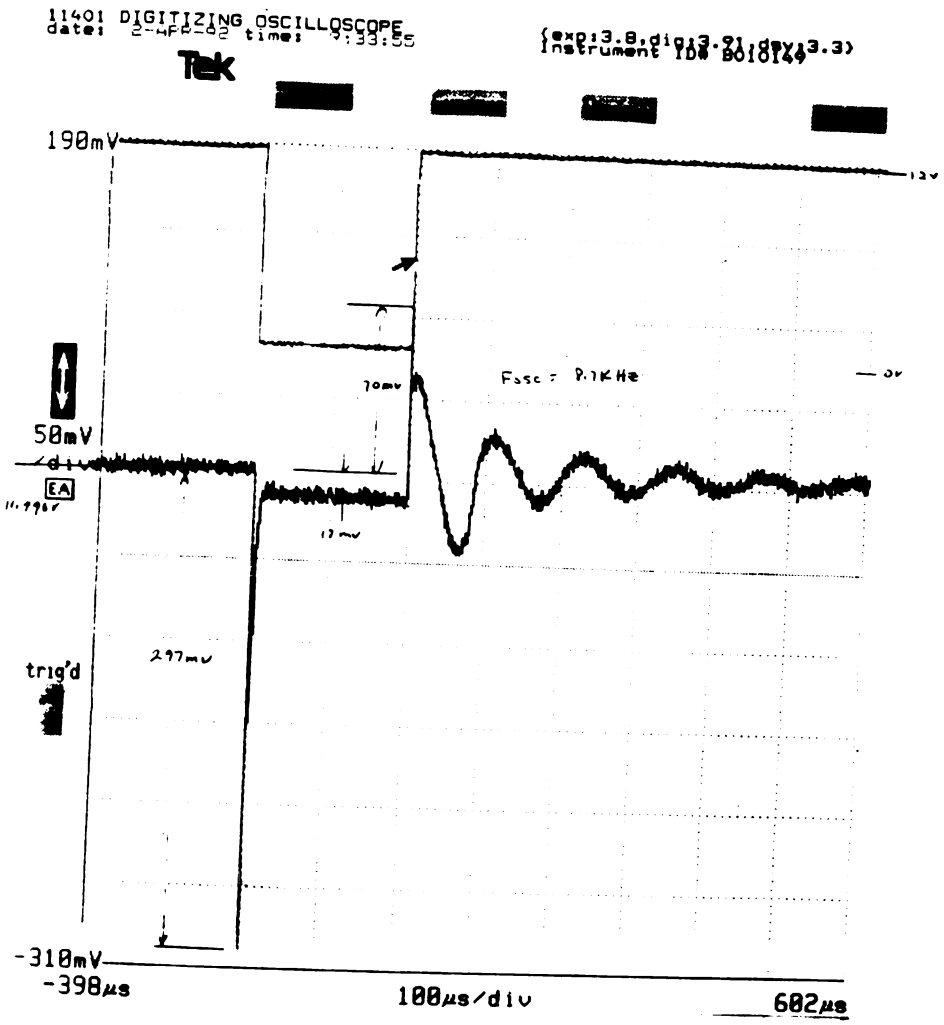

Figure 3.34 Load transient response, measured

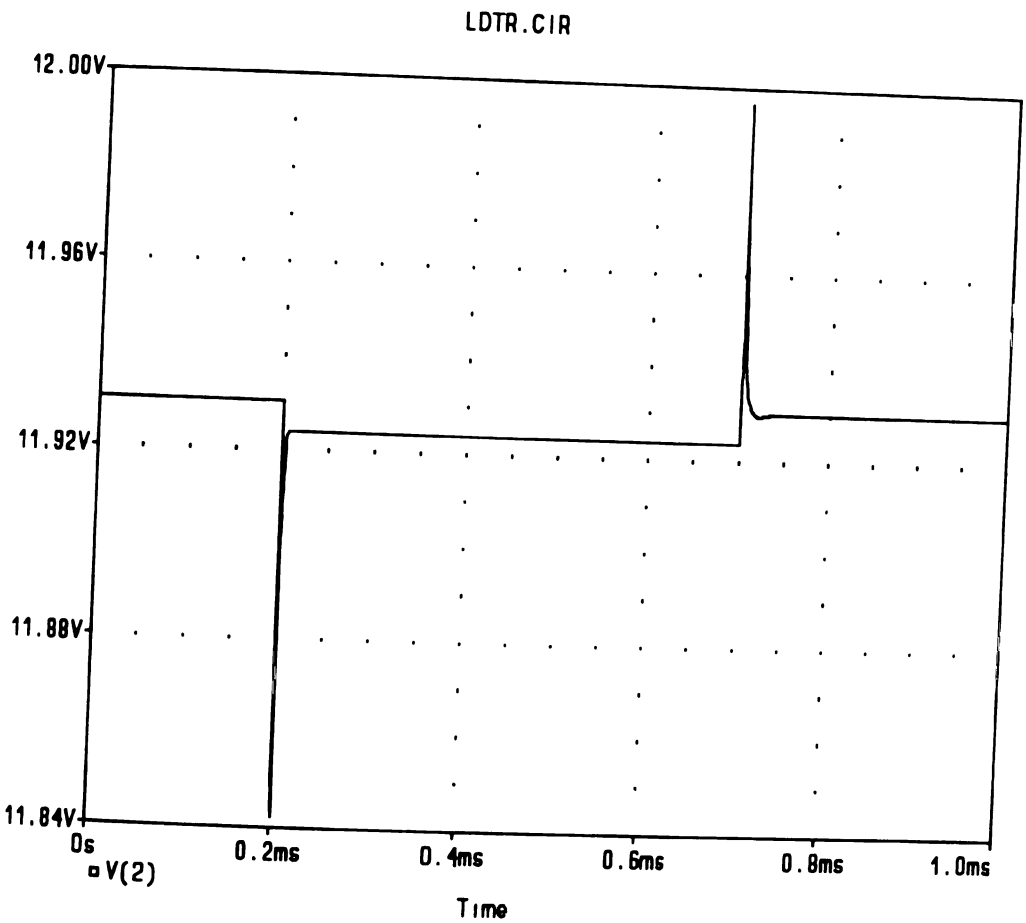

Figure 3.35 Load transient response, macromodel

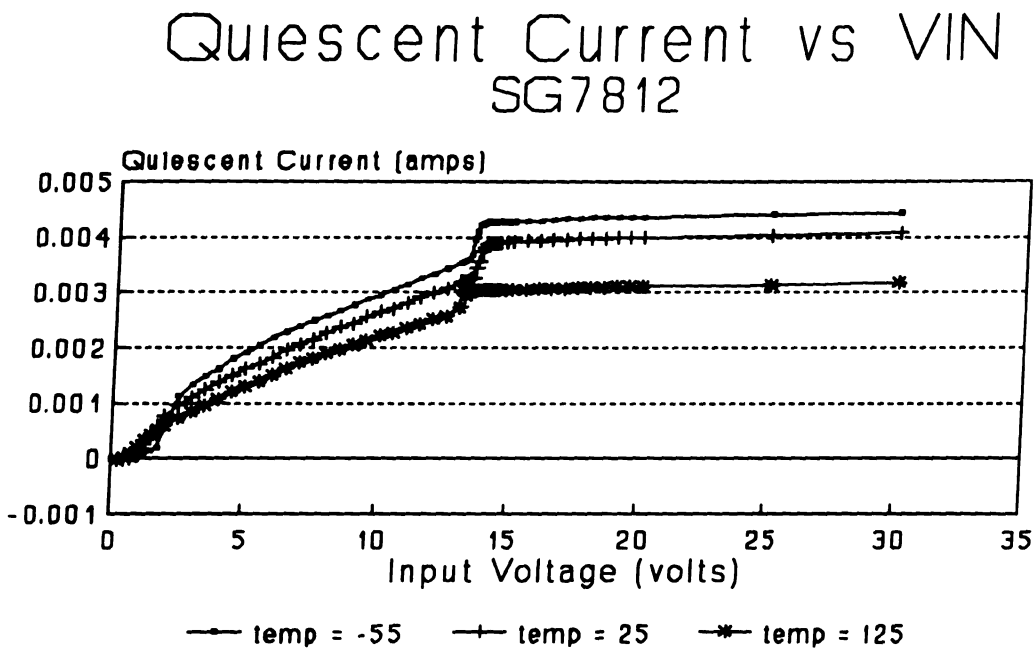

Figure 3.36 Quiescent current vs input voltage, measured

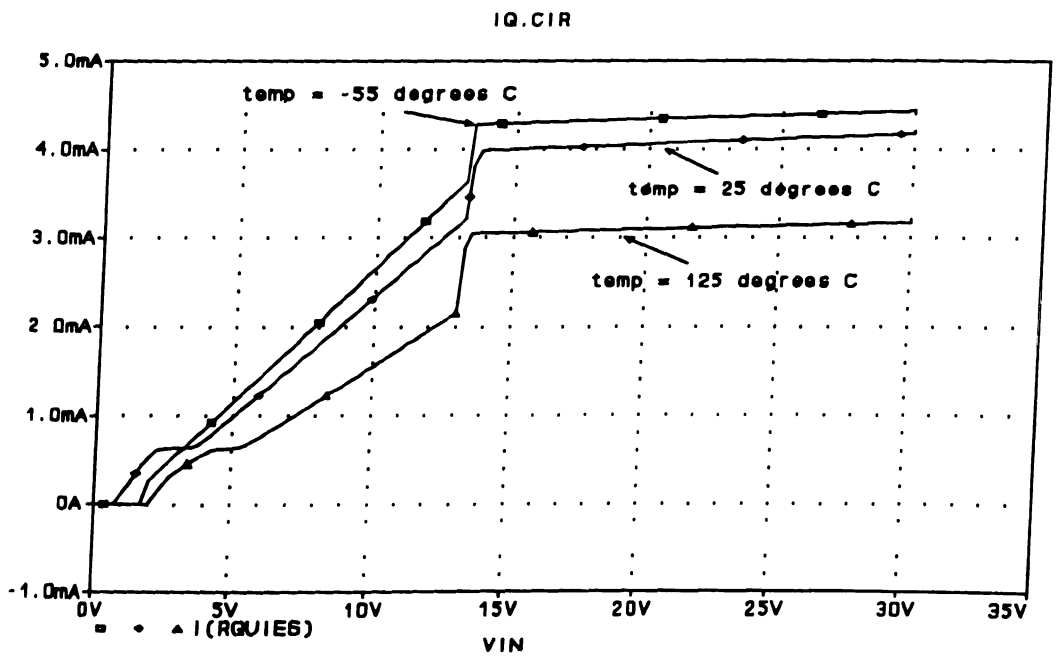

Figure 3.37 Quiescent current vs input voltage, macromodel

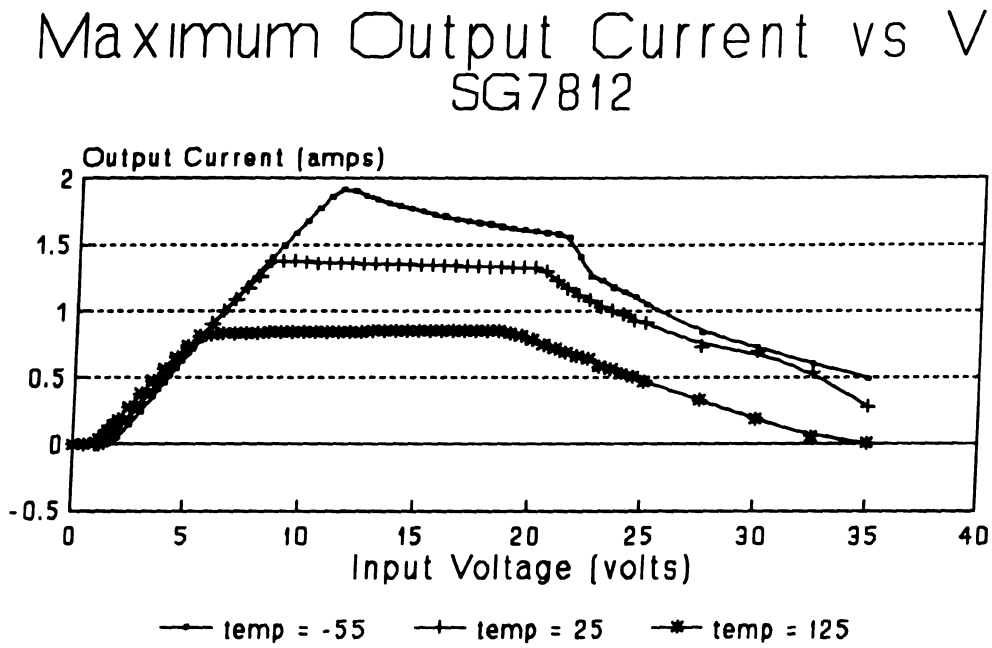

Figure 3.38 Maximum output current vs input voltage, measured

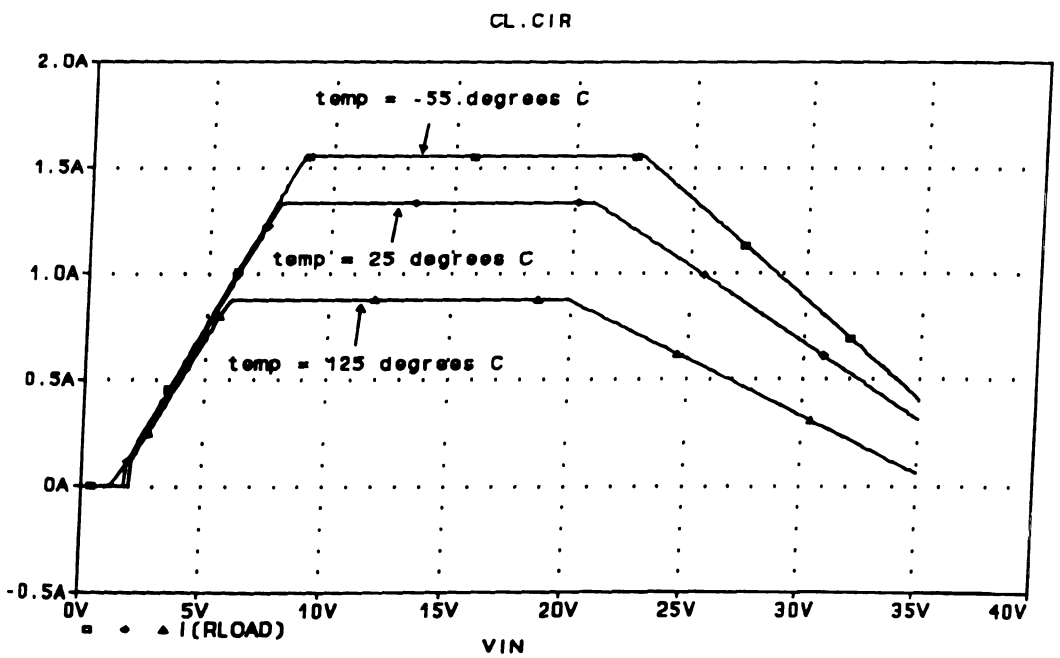

Figure 3.39 Maximum output current vs input voltage, macromodel

Comparison of Macromodel Parameters and Measured Parameters				
QUANTITY		**-55°C**	**25°C**	**125°C**
RR_{LF}	lab	65.7db	62.9db	60.1db
	model	65.5db	62.9b	60.0db
$P1_{RR}$	lab	2.000kHz	2.933kHz	3.500kHz
	model	2.113kHz	2.996kHz	3.788kHz
IQ	lab	4.28mA	3.89mA	3.01mA
	model	4.43mA	3.99mA	3.05mA
$\Delta IQ/\Delta V_{IN}$	lab	9.05u	11.58u	7.43u
	model	9.12u	11.81u	7.78u
max output current	lab	1.55A	1.32A	0.853A
	model	1.55A	1.33A	0.877A
dropout voltage	lab	1.86V	1.59V	1.36V
	model	1.56V	1.58V	1.66V
R_{OUT}	lab	0.016Ω	0.02Ω	0.01Ω
	model	0.0263Ω	0.0314Ω	0.0248Ω

Table 3.6 Macromodel comparisons with lab data, SG7812

3.7 TEST CIRCUITS

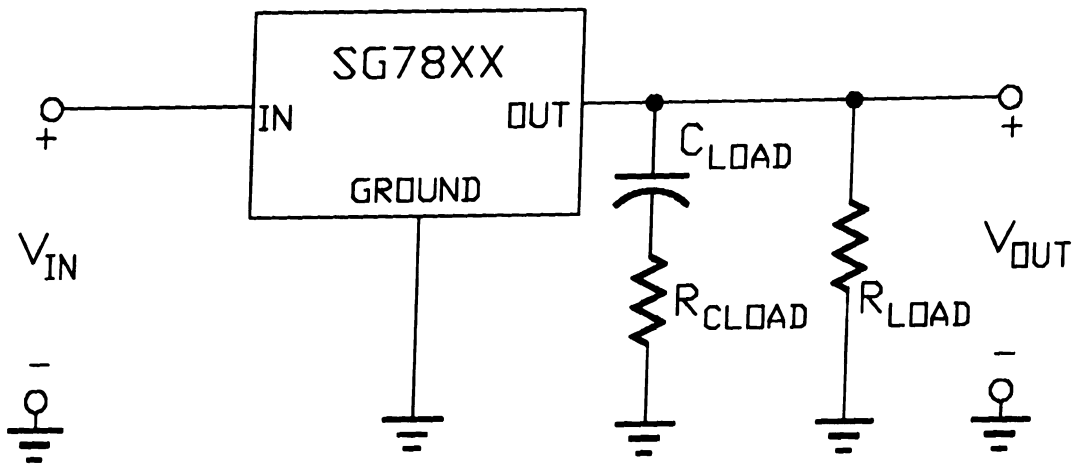

Figure 3.40 Basic Pspice test circuit for the SG7805 and SG7812

A. SG7805 Pspice Test Circuits

```
RR.CIR
*
*ripple rejection for the SG7805
*
VDC    3 0 DC 10
VAC    1 3 AC 1
RLOAD  2 0 51.081
CLOAD  2 10 5.478u
RCLOAD 10 0 1.8934
XREG   1 2 0 SG7805
.OP
.LIB SG7805.LIB
.AC DEC 20 10 1MEG
.TEMP -55 25 125
.PROBE
.END
```

```
ZOUT.CIR
*
*output impedance for the SG7805
*
VDC     1 0 DC 10
RLOAD   2 0 51.081
CLOAD   2 10 5.478u
RCLOAD  10 0 1.8934
XREG    1 2 0 SG7805
IAC     0 2 AC 1
.OP
.LIB SG7805.LIB
.AC DEC 20 10 1MEG
.PROBE
.TEMP -55 25 125
.OPTIONS NOPAGE
.END
```

```
PU.CIR
*
*power up and down, square wave, response for the SG7805
*
VPULSE  100 0 PULSE (0 10 100u 0 0 500u)
ROUT    100 1 .1
XREG    1 2 0 SG7805
RLOAD   2 0 51.081
CLOAD   2 10 5.478u
RCLOAD  10 0 1.8934
.OP
.OPTION ITL5=0 ITL1=300 ITL2=300
.LIB SG7805.LIB
.TRAN 2.5u 1000u 0 2.5u
.TEMP -55 25 125
.PROBE
.END
```

```
PU_TRI.CIR
*
*power up and down, triangle wave, response for the sg7805
*
VPULSE  100 0 PULSE (0 10 20u 80u 80u 0.001u 161u)
ROUT    100 1 .1
XREG    1 2 0 SG7805
RLOAD   2 0 51.081
CLOAD   2 10 5.478u
RCLOAD  10 0 1.8934
.OP
.OPTION ITL5=0 ITL1=300 ITL2=300
.LIB SG7805.LIB
.TRAN .5u 600u 0 .5u
.TEMP -55 25 125
.PROBE
.END
```

```
LTR.CIR
*
*line transient response for the SG7805
*
VIN     1 3 DC 10
VPULSE  3 0 PULSE (0 4 10u 0 0 50u)
XREG    1 2 0 SG7805
RLOAD   2 0 51.081
CLOAD   2 10 5.478u
RCLOAD  10 0 1.8934
.OP
.OPTION ITL5=0
.LIB SG7805.LIB
.TEMP -55 25 125
.TRAN .25u 100u 0 .25u
.PROBE
.END
```

```
LDTR.CIR
*
*load transient response for the SG7805
*
VIN     1 0 DC 10
XREG    1 2 0 SG7805
VPULSE  20 0 PULSE (4.97 0 10u 0 0 25u 40u)
RLOAD   2 20 51.081
CLOAD   2 10 5.478u
RCLOAD  10 0 1.8934
.OP
.LIB SG7805.LIB
.OPTIONS ITL5=0
.TRAN .1u 50u 0 .1u
.TEMP = -55 25 125
.PROBE
.END
```

```
IQ.CIR
*
*quiescent current for the SG7805
*
VIN     1 0 DC 10
RLOAD   2 0 100MEG
CLOAD   2 10 5.478u
RCLOAD  10 0 1.8934
RQUIES  3 0 99.65
XREG    1 2 3 SG7805
.LIB SG7805.LIB
.OPTIONS ITL1=200 ITL2=200
.DC VIN 0 30 0.25
.TEMP -55 25 125
.PROBE
.END
```

C
*
*
VT
RE
CL
RC
XF
LI
DC
IT
PR
EN

B.S

RR
*
*
VDC
VAC
RLO
CLO
RCL
FEC
OP
LB
IEN
AC
PRO
ZD

```
CL.CIR
*
*current limiting for the SG7805
*
VIN     1 0 DC 20
RLOAD   2 0 1.02
CLOAD   2 10 5.478u
RCLOAD  10 0 1.8934
XREG    1 2 0 SG7805
.LIB SG7805.LIB
.DC VIN 0 32.5 0.1
.TEMP -55 25 125
.PROBE
.END
```

B. SG7812 Pspice Test Circuits

```
RR.CIR
*
*ripple rejection for the SG7812
*
VDC     3 0 DC 20
VAC     1 3 AC 1
RLOAD   2 0 67.449
CLOAD   2 10 .784U
RCLOAD  10 0 2.138
XREG    1 2 0 SG7812
.OP
.LIB SG7812.LIB
.TEMP -55 25 125
.AC DEC 20 10 1MEG
.PROBE
.END
```

```
ZOUT.CIR
*
*output impedance for the SG7812
*
VDC     1 0 DC 20
RLOAD   2 0 67.449
CLOAD   2 10 .784U
RCLOAD  10 0 2.138
XREG    1 2 0 SG7812
IAC     0 2 AC 1
.OP
.LIB SG7812.LIB
.TEMP -55 25 125
.AC DEC 20 10 1MEG
.PROBE
.END
```

```
PU.CIR
*
*power up and down, square wave, response for the SG7812
*
VPULSE  100 0 PULSE (0 20 200U 0 0 500U)
ROUT    100 1 0.1
RLOAD   2 0 67.449
CLOAD   2 10 .784U
RCLOAD  10 0 2.138
XREG    1 2 0 SG7812
.OP
.OPTION ITL5=0 ITL1=500 ITL2=500
.LIB SG7812.LIB
.TRAN 2.5U 1000U 0 2.5U
.TEMP 25
.PROBE
.END
```

```
PU_TRI.CIR
*
*power up response, triangle wave, for the SG7812
*
VPULSE  100 0 PULSE (0 20 10U 600U 600U .0001U 1201U)
ROUT    100 1 .1
XREG    1 2 0 SG7812
CLOAD   2 10 .784U
RCLOAD  10 0 2.138
RLOAD   2 0 67.449
.OP
.OPTION ITL5=0 ITL1=300 ITL2=300
.LIB SG7812.LIB
.TEMP=25
.TRAN 1U 2000U 0 1U
.PROBE
.END
```

```
LTR.CIR
*
*line transient response for the SG7812
*
VIN     1 3 DC 20
VPULSE  3 0 PULSE (0 4 20U 0 0 50U)
XREG    1 2 0 SG7812
CLOAD   2 10 .784U
RCLOAD  10 0 2.138
RLOAD   2 0 67.449
.OPTION ITL5=0
.LIB SG7812.LIB
.TRAN 1U 100U 0 1U
.TEMP 25
.PROBE
.END
```

```
LDTR.CIR
*
*load transient response for the SG7812
*
VIN     1 0 DC 20
XREG    1 2 0 SG7812
RLOAD   2 20 67.449
CLOAD   2 10 .784u
RCLOAD   10 0 2.138
VPULSE  20 0 PULSE (11.8 0 200U 0 0 500U)
.OP
.LIB SG7812.LIB
.OPTIONS ITL5=0
.PARAM VALUE = 1
.TRAN 1U 1000U 0 1U
.TEMP = 25
.PROBE
.END
```

```
IQ.CIR
*
*quiescent current for the SG7812
*
VIN     1 0 DC 20
RLOAD   2 0 100MEG
CLOAD   2 10 .784U
RCLOAD  10 0 2.138
RQUIES  3 0 99.650
XREG    1 2 3 SG7812
.LIB SG7812.LIB
.OPTIONS ITL1=200 ITL2=200
.DC VIN 0 30 0.25
.TEMP = -55 25 125
.PROBE
.END
```

```
CL.CIR
*
*current limiting for the SG7812
*
VIN     1 0 DC 20
RLOAD   2 0 3.9295
CLOAD   2 10 .784U
RCLOAD  10 0 2.138
XREG    1 2 0 SG7812
.LIB SG7812.LIB
.TEMP -55 25 125
.DC VIN 0 35 0.1
.PROBE
.END
```

3.7.3 Measurement Test Circuits

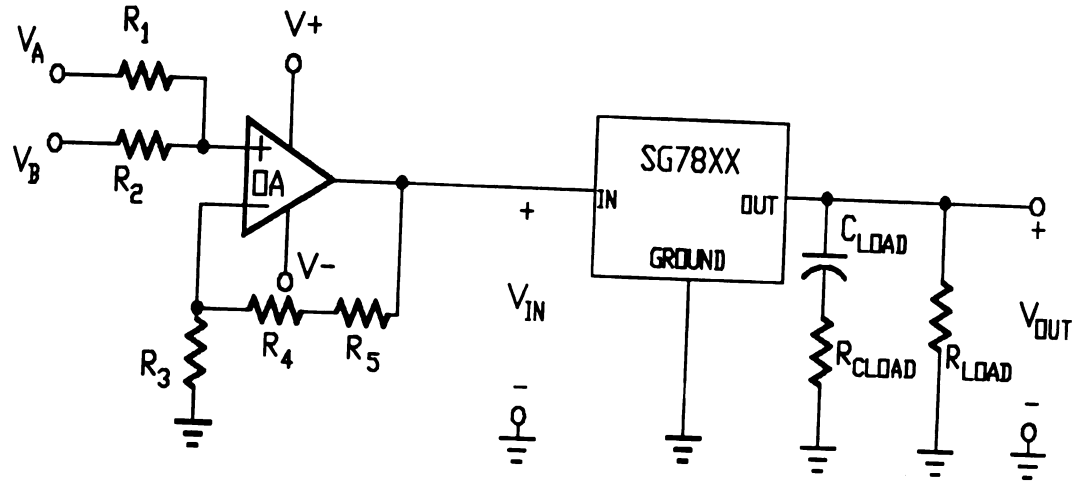

Figure 3.41 Test circuit No. 1

The conditions of test circuit No. 1 are stated.

C_{LOAD} measured 5.478uF at 100kHz for the SG7805
C_{LOAD} measured .784uF at 100kHz for the SG7812
R_{CLOAD} represents the series resistance of C_{LOAD} and measured 1.8934Ω at 100kHz for the SG7805.
R_{CLOAD} measured 2.138Ω at 100kHz for the SG7812.
R_1, R_2, R_3, R_4, and R_5 have nominal values of 1kΩ.
V+ is a positive 50 volt dc power supply.
V- is a negative 10 volt dc power supply.
OA is a Burr-Brown OPA541 Op-Amp.
The SG7805 and SG7812 reside inside a temperature chamber. Wires are connected at the terminals of the SG7805 and SG7812 to allow them to be connected outside the chamber to the test circuit.

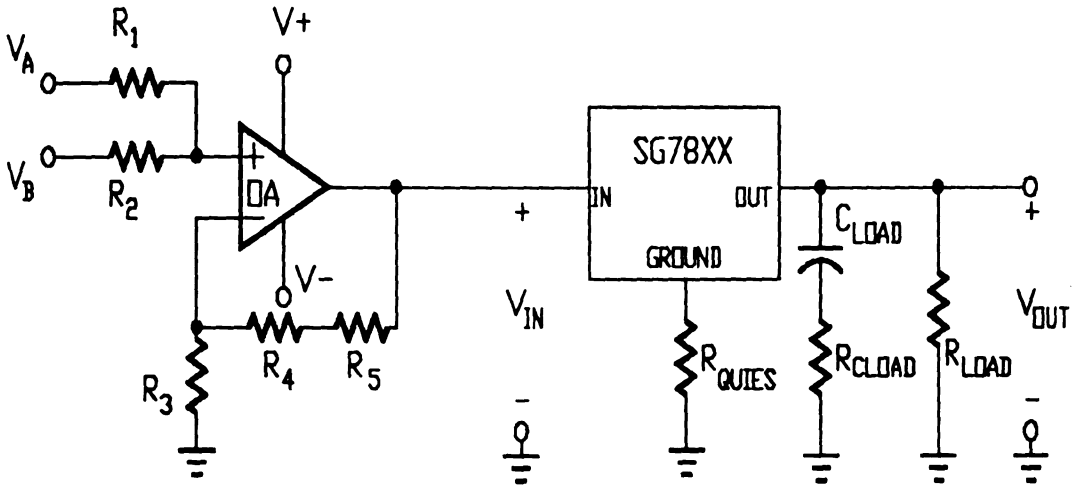

Figure 3.42 Test circuit No. 2

The conditions of test circuit No. 2 are stated.

C_{LOAD} measured 5.478uF at 100kHz for the SG7805

C_{LOAD} measured .784uF at 100kHz for the SG7812

R_{CLOAD} represents the series resistance of C_{LOAD} and measured 1.8934Ω at 100kHz for the SG7805.

R_{CLOAD} measured 2.138Ω at 100kHz for the SG7812.

R_1, R_2, R_3, R_4, and R_5 have nominal values of 1kΩ.

V+ is a positive 50V dc power supply.

V- is a negative 10V dc power supply.

OA is a Burr-Brown OPA541 Op-Amp.

The SG7805 and SG7812 reside inside a temperature chamber. Wires are connected at the terminals of the SG7805 and SG7812 to allow them to be connected outside the chamber to the test circuit.

R_{QUIES} has a nominal value of 100Ω

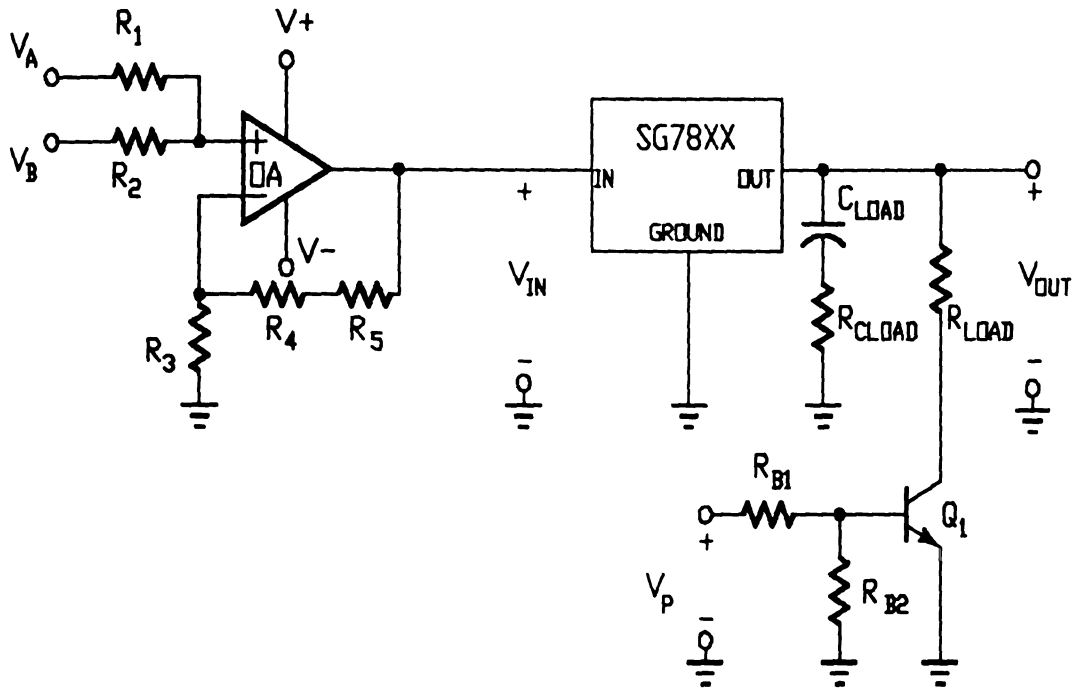

Figure 3.43 Test circuit No. 3

The conditions of test circuit No. 3 are stated.

C_{LOAD} measured 5.478uF at 100kHz for the SG7805

C_{LOAD} measured .784uF at 100kHz for the SG7812

R_{CLOAD} represents the series resistance of C_{LOAD} and measured 1.8934Ω at 100kHz for the SG7805.

R_{CLOAD} measured 2.138Ω at 100kHz for the SG7812.

R_1, R_2, R_3, R_4, and R_5 have nominal values of 1kΩ.

V+ is a positive 50V dc power supply.

V- is a negative 10V dc power supply.

OA is a Burr-Brown OPA541 Op-Amp.

The SG7805 and SG7812 reside inside a temperature chamber. Wires are connected at the terminals of the SG7805 and SG7812 to allow them to be connected outside the chamber to the test circuit.

Q_1 is a 2N4401 npn transistor.

R_{B1} has a nominal value of 10kΩ.

R_{B2} has a nominal value of 1kΩ.

1) Ripple rejection was done using test circuit 1. V_A was connected to an ac function generator. V_B was connected to a positive dc power supply. These were set to produce a 10V dc voltage at V_{IN} for the SG7805 and a 20V dc voltage at V_{IN} for the SG7812, with a sine wave superimposed for both. R_{LOAD} measured 51.081Ω for the SG7805 and 67.449Ω for the SG7812. Voltages and phases were measured with a Tektronix 11401 scope.

2) The V_{IN} vs V_{OUT} for both chips, V_{OUT} at V_{IN} = 10V for the SG7805, and the V_{OUT} at V_{IN} = 20V for the SG7812 measurements were done using test circuit 1. V_A was connected to an pulse generator and pulsed at 100Hz, with a duty cycle of 5%. V_B was grounded. These were set to produce the necessary voltage at V_{IN}. R_{LOAD}, when used, measured 51.081Ω for the SG7805 and 67.449Ω for the SG7812. Voltages were measured with a Tektronix 11401 scope.

3) The power up and down square wave measurements were done using test circuit 1. V_A was connected to an pulse generator. V_B was grounded. R_{LOAD} measured 51.081Ω for the SG7812 and 67.449Ω for the SG7812. Voltages were measured with a Tektronix 11401 scope.

4) The power up and down triangle measurements was done using test circuit 1. V_A was connected to an ac function generator, generating a triangle wave. V_B was connected to a positive dc power supply. These were set to produce a triangle wave at V_{IN} which has a maximum value of 10V for the SG7805 and 20V for the SG7812, and a minimum value of 0V for both. R_{LOAD} measured 51.081Ω for the SG7812 and 67.449Ω for the SG7812. Voltages were measured with a Tektronix 11401 scope.

5) The quiescent current measurements were done using test circuit 2. V_A was connected to an pulse generator and pulsed at 100Hz, with a duty cycle of 5%. V_B was grounded. These were set to produce the necessary voltage at V_{IN}. R_{QUIES} measured 99.65Ω for both the SG7805 and SG7812. Voltages were measured with a Tektronix 11401 scope. The voltage was measured across R_{QUIES} and divided by R_{QUIES} to give the quiescent current.

6) The load transient response measurements was done with test circuit 3. V_A was grounded. V_B was connected to a positive dc power supply to produce a dc voltage of 10V at V_{IN} for the SG7805 and 20V at V_{IN} for the SG7812. V_P was pulsed to allow Q1 to function as a switch, connecting R_{LOAD} on and off to ground to simulate the switching on and off of a load. R_{LOAD} measured 51.081Ω for the SG7812 and 67.449Ω for the SG7812.

7) The maximum output current vs V_{IN} measurements were done using test circuit 1. V_A was connected to an pulse generator and pulsed at 100Hz, with a duty cycle of 5%. V_B was grounded. These were set to produce the necessary voltage at V_{IN}. R_{LOAD} measured 3.9295Ω for both the SG7805 and SG7812. Voltages were measured with a Tektronix 11401 scope. The voltage was measured at R_{LOAD} was then converted to a current.

8) The line transient response measurements was done with test circuit 1. V_A was connected to a pulse generator. V_B was connected to a positive dc power supply. These were set to produce a 10V dc voltage at V_{IN} for the SG7805 and a 20V dc voltage at V_{IN} for the SG7812, with a pulse superimposed. R_{LOAD} measured 51.081Ω for the SG7812 and 67.449Ω for the SG7812. Voltages were measured with a Tektronix 11401 scope.

CHAPTER 4

SG7915 MACROMODEL DEVELOPMENT

4.1 INTRODUCTION

This chapter describes the development of the SG7915 voltage regulator macromodel. The SG7915 is a three terminal, fixed, negative, voltage regulator.

The format for this chapter is to develop the macromodel for the SG7915 for room temperature, then to adapt this macromodel to produce a model for the temperatures of -55°C to 125°C. Finally, lab results are shown.

4.2 DEVELOPMENT OF THE SG7915 MACROMODEL

The functional block diagram for the SG7915 macromodel is shown in Fig. (4.1). This gives the starting point for the macromodel development. The macromodel for the SG7915 is shown in Fig. (4.2). The voltage reference and bias current source have been replaced by E_{REF} (the controlled source labeled V_{REF} in Fig. (4.2)) and F_Q. The voltage controlled voltage source E_{REF} has V_{REF} as it's controlling voltage, and has a gain of 1. The error amplifier is replaced by E_A, E_B, R_O, R_P, C_P, D_+, D_-, E_+, V_+ and V_-. R_{22} and R_{23} are the same as depicted in the functional block diagram, replacing R_1 and R_2. The Darlington output pair has been replaced by one output transistor, Q_P. Additions not shown in the functional block diagram will follow. $E_{Q1\text{-}Q3}$, $V_{Q1\text{-}Q3}$, and the

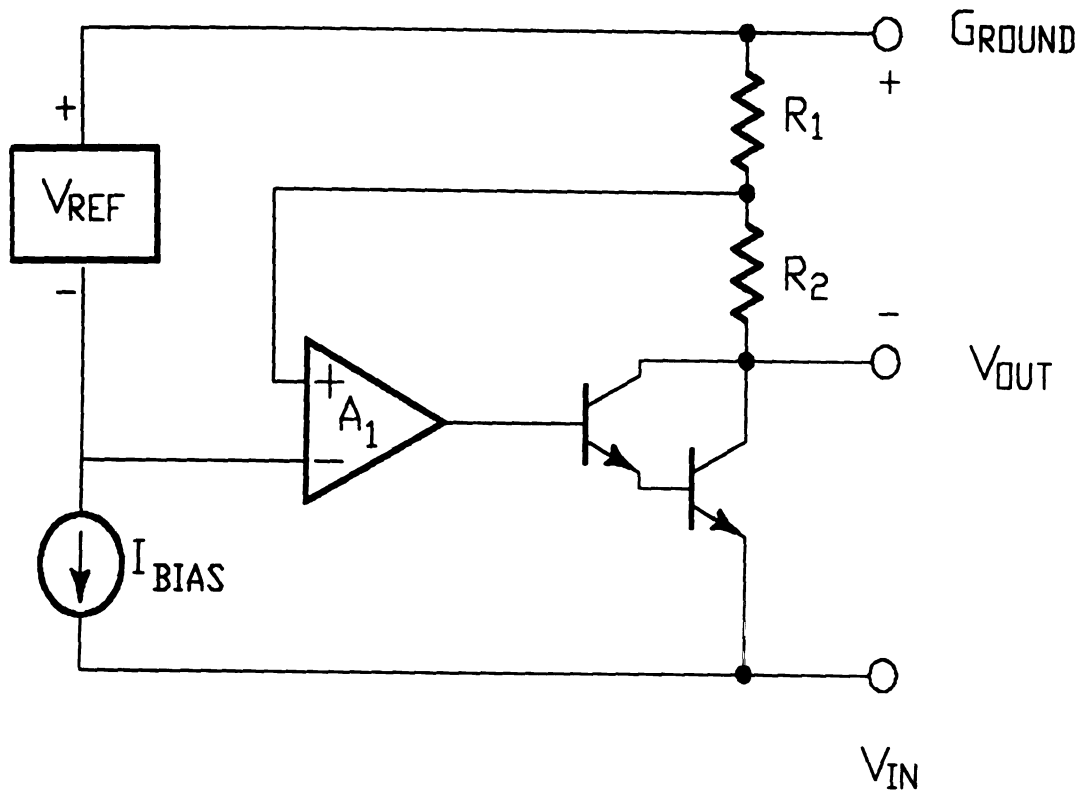

Figure 4.1 SG7915 functional block diagram

resistors R_{Q1-Q3}, provide for quiescent current shaping as well as variations in quiescent current with temperature. L_1, D_{ZR}, R_{ZR}, R_R, R_Q, and D_{Z1} provide the voltage reference, V_{REF}, upon which E_{REF} depends. R_B provides some output resistance for E_B as well as base resistance for Q_P. D_{DIS} provides for capacitive load discharge through the device when the SG7915 is driving a capacitive load. R_{BC} and C_{BC} provide for frequency compensation for Q_P. D_{DO} and R_{DO} provide for dropout characteristics. Finally, Q_L, R_{FB}, D_{ZFB}, Q_{CL}, R_{BCL}, and R_{CL} provide for maximum output current limiting and foldback current limiting. This gives a general overview of the macromodel. The details of the elements and formulas follow.

4.2.1 The Reference Voltage Generator

The voltage reference generator consists of L_1, D_{ZR}, R_{ZR}, R_R, R_Q, D_{Z1}, and E_{REF}

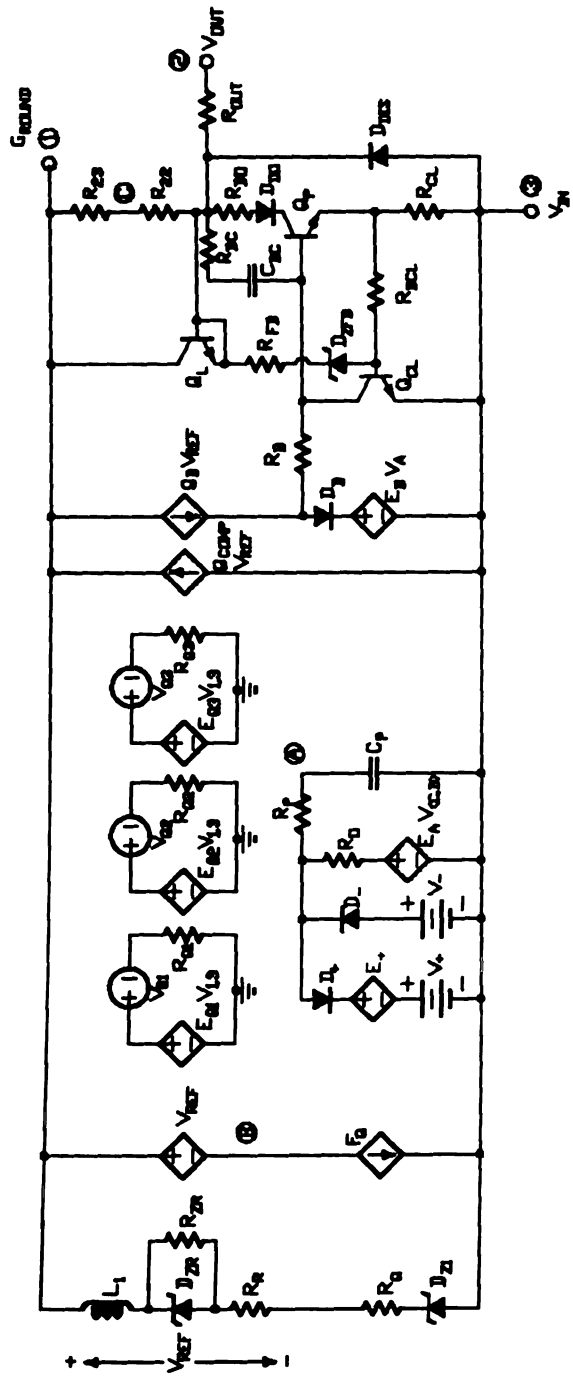

Figure 4.2 SG7915 macromodel

shown in Fig (4.2). The controlled source E_{REF} depends upon V_{REF} and has a gain of one, so the entire reference voltage is determined by the voltage across the components L_1, R_R, and D_{ZR}. E_{REF} provides a voltage buffer between the reference and the rest of the circuit. It was determined that the SG7915 has an internal reference voltage of roughly 2.65V. This information was gathered from the data sheets. Note from Fig (4.1),

$$V_{OUT} = \left(1 + \frac{R_{22}}{R_{23}}\right) \frac{V_{REF}}{1 + \frac{1}{A_{DC}}\left(1 + \frac{R_{22}}{R_{23}}\right)}, \tag{4.1}$$

where A_{DC} is the dc gain of the amplifier. This equation shows the effect that changes in V_{REF} have on V_{OUT}. Note from the structure of the reference voltage generator, that V_{REF} changes with both frequency and input voltage. The dc changes contribute to line regulation. The ac changes contribute to ripple rejection. Note the chip schematic for the SG7915 indicates a reference contains frequency dependent components.

R_Q provides variation in quiescent current with respect to input voltage while the regulator is at the regulated output voltage. For all practical purposes, during regulation, the voltage V_{REF} and the voltage drop across D_{Z1} are constant. This means if the G_{ROUND} pin is grounded, the changes in input voltage result in identical changes in voltage drop across R_Q. This results in the current in R_Q changing. This current then flows through the ground terminal of the regulator which is the quiescent current.

In the actual chip measurements, the output voltage remained zero for input voltages from 0 to anywhere between -1.5V to -2V. As with the SG78XX chips, there is an "on" voltage which the regulator is required to overcome. Note this behavior in

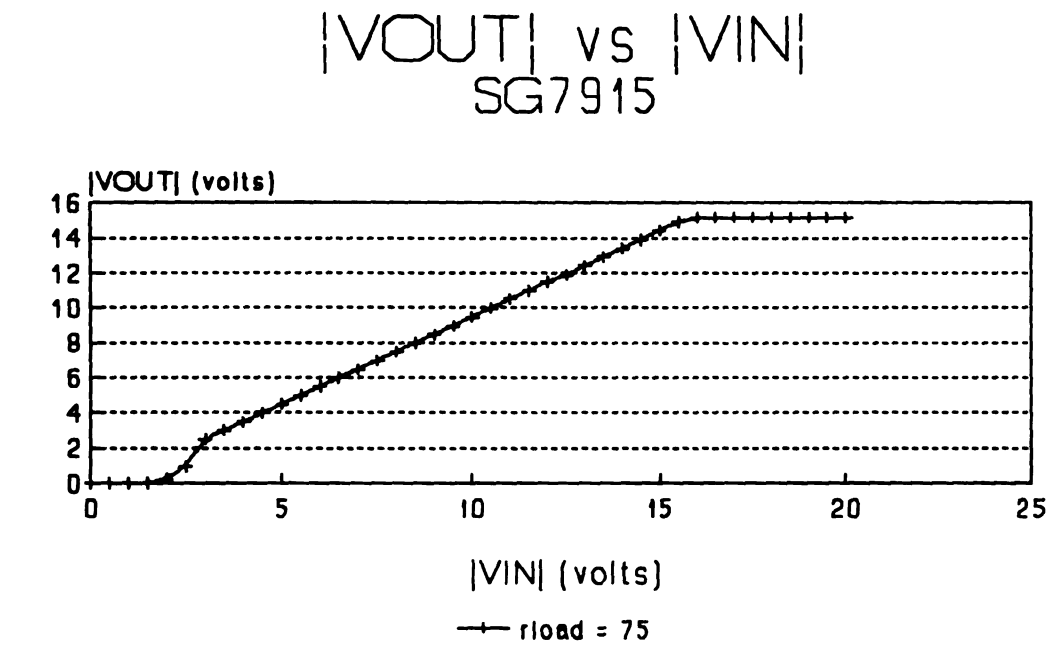

Figure 4.3 $|V_{OUT}|$ vs $|V_{IN}|$, measured

Fig. (4.3) which shows measured $|V_{OUT}|$ vs $|V_{IN}|$ characteristics for the SG7915. This effect is modeled by BV_{DZ1}. If the voltage at which activity in Fig. (4.3) begins to turn on is call V_{ON}, then this can be reproduced by setting

$$BV_{Z1} = |V_{ON}|. \tag{4.2}$$

Note that for all $|V_{IN}|$ less than $|V_{ON}|$ the reference voltage $V_{REF} = 0$ and the regulator shows no activity.

4.2.2 The Error Amplifier

The error amplifier consists of E_A, E_B, R_O, R_P, C_P, D_+, D_-, E_+, V_+ and V_-. E_A and E_B are voltage controlled voltage sources whose product has a dc gain of A_{DC}. This with C_P, R_P, and R_O, provide for a one pole error amplifier. D_+, D_-, E_+, V_+, and V_- provide for maximum and minimum clamping of the error amplifier.

4.2.3 Ripple Rejection Modeling

Fig. (4.4) gives an example of measured ripple rejection vs frequency for the SG7915 for several loads. In modeling ripple rejection, a couple of approximations are made. The first is that low frequency ripple rejection is assumed equal for all loads. The second is that the first pole in ripple rejection for all loads is assumed equal. Fig.

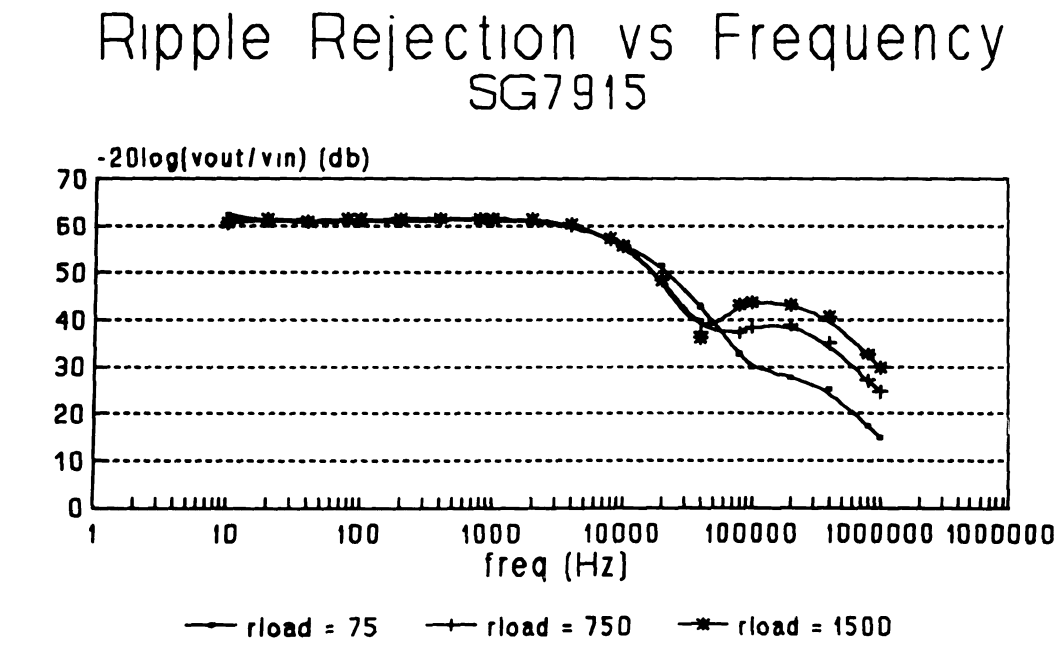

Figure 4.4 Ripple rejection vs frequency, measured

(4.4) shows that these are reasonable approximations.

The zero of V_{REF} is the pole of ripple rejection which is seen from Eqn. (4.1). The zero generated by V_{REF} is normally at a frequency much lower than any poles or zeros generated by any of the other reactive elements. It is necessary to find this pole. To find this, find the small signal relationship of V_{REF} to V_{IN}. It is

where r_{DZR} and r_{DZ1} are the small signal resistances of the diodes. Eqn. (4.3) describes

$$v_{ref} = \frac{R_R + r_{DZR} + sL_1}{R_R + r_{DZR} + R_Q + r_{DZI} + sL_1} v_{in}, \tag{4.3}$$

a simple voltage divider. Then, since the first zero of Eqn. (4.3) is the first pole of the ripple rejection,

$$PI_{RR} = \frac{R_R + r_{DZR}}{L_1}. \tag{4.4}$$

Next it is necessary to find the dc changes in output voltage, since this gives rise to low frequency ripple rejection. The dc changes in output voltage are modeled by allowing the reference voltage to vary with dc input voltage. At low frequencies Eqn. (4.3) reduces to

$$v_{ref} = \frac{R_R + r_{DZR}}{R_R + r_{DZR} + R_Q + r_{DZI}} v_{in}, \tag{4.5}$$

or

$$v_{ref} = \frac{R_R + r_{DZR}}{R_R + r_{DZR} + R_Q} v_{in}. \tag{4.6}$$

Inserting Eqn. (4.6) into Eqn. (4.1) gives

$$RR_{lf} = \left(\frac{\Delta V_{OUT}}{\Delta V_{IN}}\right)_{DC} = \frac{\left(1 + \frac{R_{23}}{R_{22}}\right)\left(\frac{R_R + r_{DZR}}{R_Q}\right)}{1 + \frac{1}{A_{DC}}\left(1 + \frac{R_{23}}{R_{22}}\right)}. \tag{4.7}$$

The high frequency ripple rejection cannot be measured, but is of interest because of it's relationship with line transient response. The symbolic solution for the high frequency ripple rejection is determined from a symbolic circuit simulator, Sspice. The result is

$$RR_{HF} = \frac{1}{1+\frac{R_{CL}}{R_{SCL}}\left(1+\frac{R_{BC}}{R_B}\right)\left(\frac{R_{23}}{R_{22}+R_{23}}\right)}. \qquad (4.8)$$

Note that R_{SCL} is the series resistance of the load capacitor. This series resistance must always be included for correct simulations. The SG7915 requires a load capacitor for stability.

There are other poles and zeros in the ripple rejection. Most of these are beyond the range of our measurements. The reactive components which contribute to these are C_{BC}, C_P, and C_L. C_L is the load capacitor, used for stability, and is not part of the actual macromodel, but must be used in the development. C_P is determined empirically by power up measurements. C_{BC} is determined empirically by trying to match a zero in the macromodel ripple rejection response to the zero seen around 100kHz in Fig. (4.4).

4.2.4 Output Impedance Modeling

We were not able to measure the output impedance of the SG7915. This is because the dc voltage of the SG7915 was out of range of the HP4192A impedance analyzer. Low frequency output impedance, can however be deduced from load transient response measurements and load regulation measurements. The low frequency output impedance is just the output resistance of the SG7915, and this is determined in the macromodel by the relationship

$$R_{OUT,\,SG7915} = R_{OUT} \qquad (4.9)$$

4.2.5 Quiescent Current Modeling

In Fig. (4.2), the elements which contribute to quiescent current are F_Q, $E_{Q1\text{-}Q3}$, $V_{Q1\text{-}Q3}$, and the resistors $R_{Q1\text{-}Q3}$. Due to the reference voltage drop across R_{23}, it too

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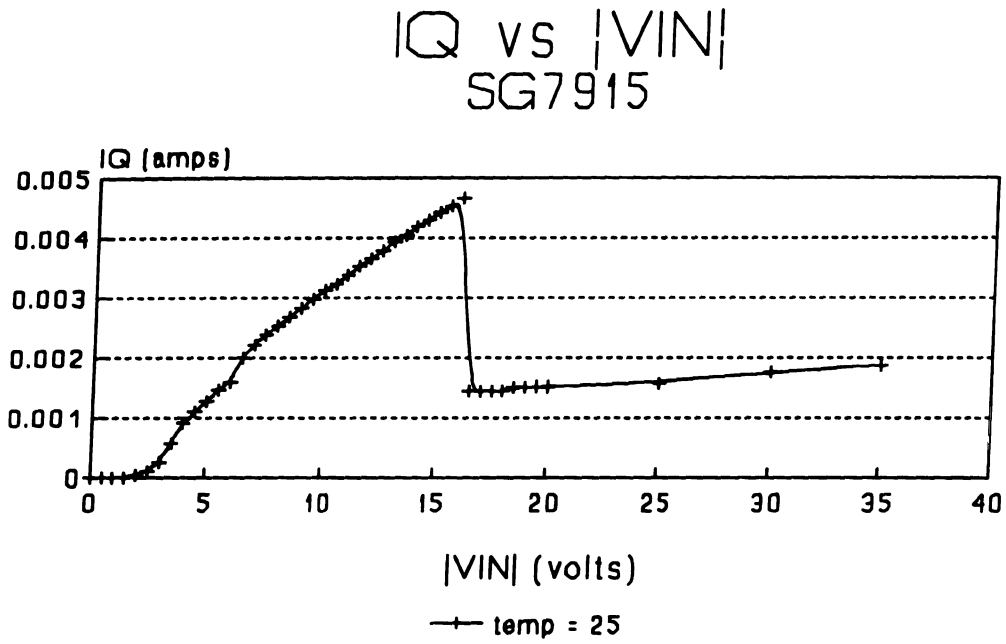

Figure 4.5 Quiescent current vs $|V_{IN}|$, measured

contributes to quiescent current. This is deduced from Fig. (4.1). The measured quiescent current vs input voltage is shown in Fig. (4.5). The most interesting phenomenon here is the very sharp jump at roughly the point at which the chip goes into regulation. Because this is a complicated phenomenon to model, and gets even more complicated to model with temperature, there are many elements used to model this behavior. Quiescent current is modeled in the macromodel in the following way. For the analysis, it is convenient to label certain critical voltages and currents as well as slopes of curves. All voltages discussed will be taken in the positive sense. Using Fig. (4.5) as a reference, let the point at which the quiescent current just begins to flow be labeled V_{ON}. Let the point at which the first discontinuity occurs be labeled V_1 and I_1. This is roughly at V_{IN} = 6V in Fig. (4.5). Let the point at which the jump occurs be V_2 and I_2 and this occurs at roughly 16V. Let the point directly after the

jump be labeled V_3 and I_3, and note this occurs at approximately 16.5V. Finally, the let the slope of the Quiescent current vs $|V_{IN}|$ curve after this point be called $(\Delta IQ/\Delta V_{IN})_{REG}$. The analysis follows. The current controlled current source F_Q has the currents through the independent voltage sources $V_{Q1\text{-}Q3}$ as its controlling currents. F_Q has the PSpice definition

FQ 4 3 POLY (3) VQ1 VQ2 VQ3 0 1 1 -1

which means that

$$I_{FQ} = I_{BQ1} + I_{BQ2} - I_{BQ3}, \tag{4.10}$$

since the voltage sources $V_{Q1\text{-}Q3}$ are dc sources of 0V. The voltage controlled voltage sources $E_{Q1\text{-}Q3}$ all have the voltage drop between the ground and input terminals as their controlling voltage, and this is just V(1,3). Instead of the normal gain relationship between the controlled sources and V(1,3), the table look-up option of PSpice is used. This is done for convenience.

The voltage controlled voltage sources are defined in the following manner:

E_{Q1} 1000 0 TABLE {V(1,3)} (V_{ON}, 0) (V_1, V_1 - V_{ON})

E_{Q2} 2000 0 TABLE {V(1,3)} (V_1, 0) (V_1, V_2 - V_1)

E_{Q3} 3000 0 TABLE {V(1,3)} (V_2, 0) (V_3, V_3 - V_2).

Describing E_{Q1}, for example, note that there is zero voltage until V(1,3) attains V_{ON}. When V(1,3) attains V_1, the voltage across the voltage source is V_1 - V_{ON}, and the voltage source retains this value for increasing V(1,3). Note that V_1 - V_{ON} is the change in voltage that V(1,3) undergoes during it's transistion from V_{ON} to V_1. E_{Q2} and E_{Q3} follow the same pattern.

Now for V(1,3) = V_{IN} from zero to V_{ON}, all of the controlled sources, as well as approximately V_{REF}, are off in the macromodel, so IQ = 0A.

When $V_{IN} = V_{ON}$, E_{Q1} begins to turn on, but IQ is still equal to 0A.

For $V_{IN} = V_{ON}$ to $V_{IN} = V_1$, $E_{Q2\text{-}Q3}$ are off, E_{Q1} is on, and current flows though V_{Q1} and hence F_Q. This is the main contribution to quiescent current in this region. At $V_{IN} = V_1$, the current through F_Q is I_1 = IQ and this current is the current through V_{Q1}, or

$$I_1 = \frac{V_1 - V_{ON}}{R_{Q1}}. \tag{4.11}$$

At $V_{IN} = V_1$, E_{Q2} begins to turn on and hence I_{RQ2} begins to contribute current. This occurs until $V_{IN} = V_2$. The current IQ now consists of current contributed from I_{RQ1}, I_{RQ2}, and R_{23}, since at this point the voltage across R_{23} is V_{REF}. Then

$$I_2 = I_1 + \frac{V_{REF}}{R_{23}} + \frac{V_2 - V_1}{R_{Q2}}, \tag{4.12}$$

since the voltage across R_{Q2} at this point is $V_2 - V_1$.

Finally at V_2, E_{Q3} begins to turn on and I_{RQ3} now contributes current to the quiescent current. This current, however, is subtracted from F_Q which causes the "jump" seen in Fig. (4.5). At V_3, E_{Q3} has reached its maximum value and

$$I_3 = I_2 - \frac{V_3 - V_2}{R_{Q3}}. \tag{4.13}$$

At this point, $E_{Q1\text{-}Q3}$ are no longer changing with input voltage, so there is no longer any variation in the current through the dependent source F_Q. Note however, there is a slight increase in quiescent current with increasing $|V_{IN}|$. This change comes from R_Q. Since V_{REF} and V_{DZ1} have little change in voltage with changes in

$|V_{IN}|$, all of the change in input voltage is dropped across R_Q in the reference circuit. This means

$$\frac{|\Delta V_{IN}|}{\Delta IQ} = R_Q \tag{4.14}$$

4.2.6 Short Circuit Current Limiting and Foldback Current Limiting

An example of measured short circuit current limiting and foldback current

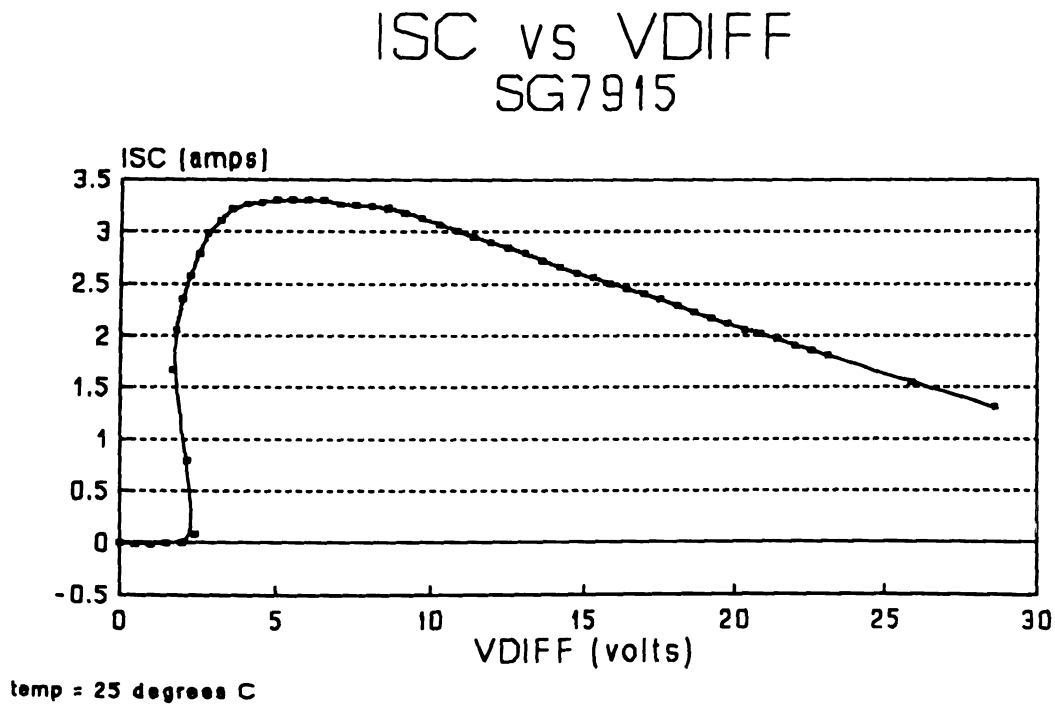

Figure 4.6 Maximum output current vs V_{DIFF}, measured

limiting is shown in Fig. (4.6).

The elements in the macromodel that contribute to short circuit current limiting and foldback current limiting are G_{COMP}, G_B, D_B, Q_{CL}, R_{BCL}, R_{CL}, D_{ZFB}, R_{FB}, and Q_L. The short circuit current works in the following way. Note the similarities with in the short circuit current limiting with the SG78XX and SG7915 voltage regulators.

D_B prevents the controlled source E_B from supplying any current to the base of Q_P. This means that G_B is the only supplier of base current to Q_P. Since the output voltage is negative, all of the load current must flow out of the load and through the collector of Q_P. This is approximately equal to the current flowing out of the emitter of Q_P. As current flows out of the emitter of Q_P through R_{CL}, a voltage is generated across the base emitter junction of Q_{CL}. If this voltage is large enough to turn Q_{CL} on, the current supplied by G_B is drawn by the collector of Q_{CL}, since its needs are large compared to the current supplied by G_B. This means that Q_P begins to turn off. If the voltage is not large enough, Q_{CL} remains off, drawing no current and Q_P is active. The maximum output current is just the current necessary to turn Q_{CL} on. This is

$$I_{MAX} = I_{ESC} = \frac{V_{BE,ON,CL}}{R_{CL}}. \tag{4.15}$$

This is a very simplified explanation of how short circuit current works, however it serves to explain the fundamental operation. Under the short circuit mode, the base of Q_P actually draws a little current, but this is negligible. The collector of Q_{CL} draws most of the current available from G_B. Then, $V_{BE,ON,CL}$ can be estimated since the collector current of Q_{CL} can be estimated as approximately the current supplied from G_B, which is $g_B V_{REF}$. Using an approximation for the relationship between collector current and base emitter voltage and inserting into Eqn. (4.15) gives

$$I_{MAX} = \frac{V_T \ln\left(\frac{g_B V_{REF}}{IS_{CL}}\right)}{R_{CL}}. \tag{4.16}$$

The voltage controlled current source G_B has V_{REF} as its controlling voltage. The transconductance of G_B, g_B, is set so that the total current flowing out of G_B is

roughly 10mA when V_{REF} attains its steady state value. The value of 10mA was selected based on the needs of C_{BC} during the line transient response. During line transient response C_{BC} needs to draw several milliamps of current and this is supplied by G_B. If G_B was added, and G_{COMP} was not added, this 10mA of current would add to the total quiescent current. This is undesirable as in the regulated state because the quiescent current is only about 1-2mA. To compensate for this, G_{COMP} was added. G_{COMP} is defined identically to G_B, except that it supplies current to pin 1, whereas G_B draws current out of pin 1, and the net effect on pin 1, and the net effect on quiescent current, is now 0A.

Finally, foldback current limiting is provided with the addition of D_{ZFB}, R_{FB}, and R_{BCL}. Note the addition of Q_L as well. Q_L was added because it was noticed that quiescent current, upon the power up and down response, was inaccurate due to current flowing through D_{ZFB}. Placing Q_L here prevents this. Note that the placement of a transistor here is *identical* to what is found in the SG7915 schematic. An explanation of foldback current follows.

The voltage differential is roughly the voltage drop across R_{FB}, D_{ZFB}, R_{BCL}, and R_{CL}. When the differential voltage is not large enough to place D_{ZFB} in the breakdown region, there is no drop across R_{FB} and very little drop across R_{BCL}, since the base current of Q_{CL} is small.

Once the differential voltage is large enough to place D_{ZFB} in the breakdown region, the macromodel enters into the foldback region. Let this voltage be referred to as V_{FB}. Any further increase in the differential voltage is mainly dropped across R_{FB} and R_{BCL}. The voltage drop across the base emitter junction of Q_{CL} is

$$V_{BE,CL} = V_{RBCL} + V_{RCL} \qquad (4.17)$$

The turn on voltage of Q_{CL} is fixed, as well as the voltage across V_{RBCL}. This is means

that, in the foldback region, a smaller voltage drop across R_{CL} is needed to turn on Q_{CL}, and hence a smaller maximum current is available to be supplied by the output. As the differential voltage across the chip increases, the voltage drop across R_{BCL} increases, and the maximum available output current decreases. This is how foldback current limiting is achieved.

Since the foldback region begins at the point where the differential voltage across the chip, V_{DIFF}, is equal to V_{FB} and the voltage drop across R_{CL},

$$BV_{DIFB} \approx V_{FB} - I_{SC}R_{CL}. \tag{4.18}$$

The components R_{BCL} and R_{FB} can be selected by selecting a point in the foldback region which gives the maximum output current for a given differential voltage. Then it can be determined that

$$V_{BE,CL,ON} = (V_{DIFF} - V_{FB})\left(\frac{R_{BCL}}{R_{BCL}+R_{FB}}\right) + I_{DIFF}R_{CL}. \tag{4.19}$$

Where V_{DIFF} and I_{DIFF} represent the voltage and current at the selected point.

4.2.7 Power Up and Down, Square Wave

Fig. (4.7) gives the measured power up and down response. There are two main contributions to the square wave input phenomenon. The first is the phenomenon which occurs as the input is powered up. As seen in Fig. (4.7), initially the output voltage peaks at a voltage slightly less than the input voltage, then oscillates before settling down to the regulated value. This is mainly due to the capacitor in the error amplifier, C_P. This effect is proportional to the time constant determined from R_O and C_P, since it should be noted that R_P is set very low.

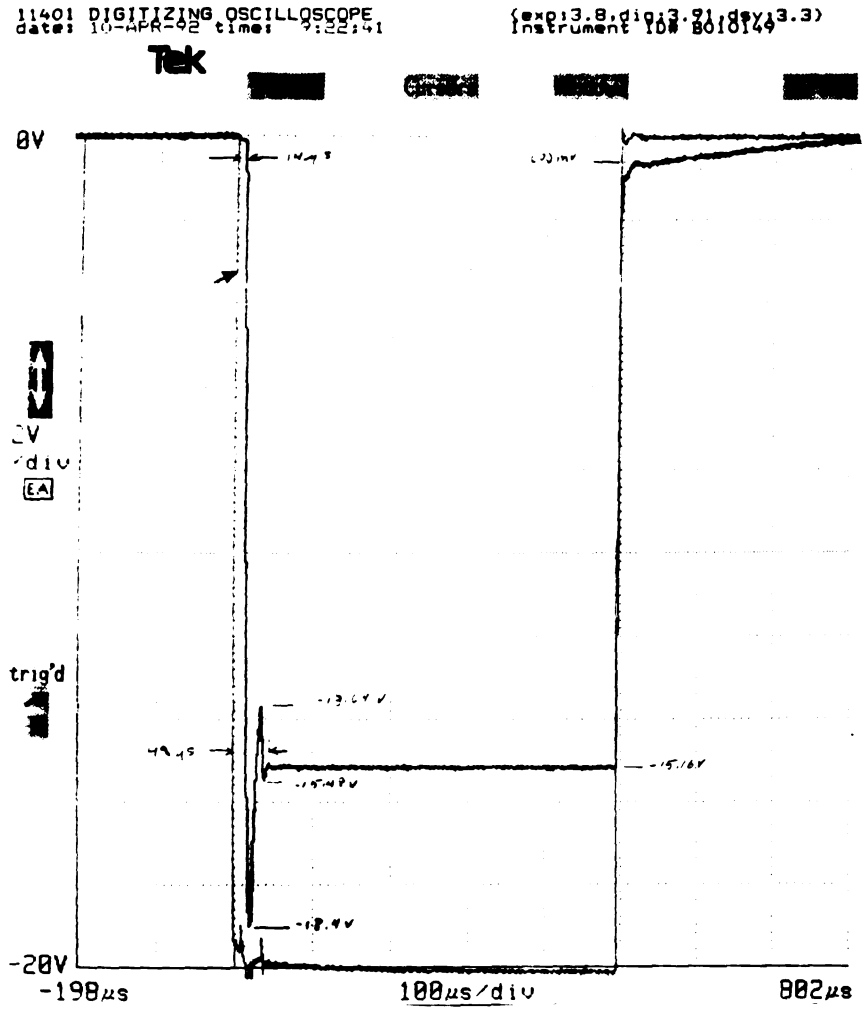

Figure 4.7 Power up and down, square wave, measured

Presently, there is no formula for determining these values. They have been adjusted empirically.

Secondly, when the chip is powered down, and the load is capacitive, the load must discharge. This will normally be the case for the SG7915 as a capacitor was always required on the output for stability. The path for this discharge is through ground, however this forces the need for a current to be supplied at the output pin. By measurement it is determined that the source supplies this current. Note that in Fig. (4.7) the difference between the input and output voltage at power down is roughly one diode drop, as with the SG78XX. This is further justification for use of this D_{DIS}. The parameters for D_{DIS} can be selected empirically, although the default diode works well.

4.2.8 Dropout Characteristics

The dropout characteristics are done primarily by D_{DO} and Q_P. The dropout voltage is then the voltage drop across these elements when Q_P is on the edge of saturation. Then

$$VDO \approx V_{DDO} + V_{SAT,QP}(I_{LOAD}) + I_{LOAD}R_{DO}, \tag{4.20}$$

where it should be noted that $V_{SAT,QP}$ is a function of the load current. Then N_{DC} can be chosen to realize a dropout voltage for a given load with

$$VDO \approx N_{DDO}\, VT \ln\left(\frac{I_{LOAD}}{IS_{DC}}\right) + V_{SAT,QP}(I_{LOAD}) + I_{LOAD}R_{LOAD} \tag{4.21}$$

4.2.9 Other Modeled Characteristics

The prior characteristics gives the characteristics modeled which are used to determine the proper choice of values for the components and the parameters of the

components for the SG7915 voltage regulator macromodel. Because of a correct choice of parameters, the macromodel can accurately predict other responses. These are: power up and down with triangle wave, line transient response, load transient response, line regulation and load regulation.

4.3 DESIGN PROCEDURE FOR A SG7915

Based on the equations and procedures shown in the last section, a design procedure will be developed in this section.

Basic to the design procedure is a list of measurements required to base the design on. The following measurements should be taken in the basic regulator circuit:

1) Measure V_{OUT} vs V_{IN} with no load.
2) Measure IQ vs V_{IN} with no load.
3) Measure V_{OUT} for V_{IN} = -20V.
4) Measure ripple rejection vs frequency with a 75Ω load.
5) Take a line transient response measurement with a 75Ω load, determine the ratio of the first peak to the change in input voltage, call this RR_{HF}.
6) Measure maximum output current vs voltage differential.
7) Take a load transient response measurement, determine the value of the difference in the steady state output voltages with and without R_{LOAD} = 75Ω.
8) Measure dropout voltage with R_{LOAD} = 75Ω.
9) Take a power up measurement with R_{LOAD} = 75Ω.
10) Measure R_{LOAD}, this value gets used in all of the equations. Also

measure C_{OUT}, the output capacitor, and R_{COUT} the effective series resistance of the capacitor.

The component selection procedure is:

1) Select E_A and E_B , this will determine A_{DC}.

2) Select R_{22} = 12.5kΩ, R_{23} = 2.69kΩ, these selections are based on the actual chip component values.

3) Select the amplifier clamping circuitry, these values are:

V_+, V_-, E_+, E_-, and the diode parameters for D_+ and D_-.

4) Based on the V_{OUT} vs V_{IN} measurement, determine the input voltage required to begin to turn the circuit on, V_{ON}, then

$$BV_{DZ1} = |V_{ON}|. \tag{4.22}$$

Select NBV_{DZ1}.

5) From the measured value of V_{OUT} at V_{IN} = -20V, and utilizing Eqn. (4.1),

$$BV_{DZR} = V_{REF} = \frac{V_{OUT}}{\left(1+\frac{R_{22}}{R_{23}}\right)}\left(1+\frac{1}{A}\left(1+\frac{R_{22}}{R_{23}}\right)\right). \tag{4.23}$$

Select NBV_{DZR} and R_{ZR}.

6) Measure the slope of IQ vs V_{IN} for the quiescent current measurement. Then from Eqn. (4.14),

$$R_Q = \frac{|\Delta V_{IN}|}{\Delta IQ}. \tag{4.24}$$

7) From the ripple rejection measurement, determine RR_{LF}. Then determine the small signal resistance of D_{ZR}. This is determined from

a trial macromodel run with PSpice. Then from Eqn. (4.7),

$$R_R = \left(\frac{\left(1 + \frac{1}{A_{DC}} \left(1 + \frac{R_{22}}{R_{23}} \right) \right) RR_{ff}}{1 + \frac{R_{22}}{R_{23}}} \right) R_Q - r_{DZR} \qquad (4.25)$$

8) From the ripple rejection measurement, determine $P1_{RR}$, then from Eqn. (4.4), then

$$L_1 = \frac{R_R + r_{DZR}}{p1_{RR}}. \qquad (4.26)$$

9) Select R_p.

10) From the power up measurement determine C_p empirically.

11) Also from the power up measurement, and measuring the difference in the input and output voltage waveforms directly after power down, select and appropriate value for N_{DDIS}.

12) From the quiescent current vs input voltage measurements determine V1, V2, V3, and I1, I2, and I3, then the table definitions for E_1, E_2, and E_3 become

(V_{ON}, 0) (V_1, V_1 - V_{ON})

(V_1, 0) (V_1, V_2 - V_1)

and (V_2, 0) (V_3, V_3 - V_1).

13) From the quiescent current vs input voltage measurements and Eqns. (4.11), (4.12), (4.13),

$$R_{QI} = \frac{V_1 - V_{ON}}{I_1}, \qquad (4.27)$$

$$R_{Q2} = \frac{V_2 - V_1}{I_2 - I_1 - \frac{V_R}{R_{23}}}, \tag{4.28}$$

$$\text{and} \quad R_{Q3} = -\frac{V_3 - V_2}{I_3 - I_2}. \tag{4.29}$$

14) Select the parameters for the output transistor Q_P. These are: BF, VAF, NF, and IS.

15) Select R_B.

16) Select the parameters for the transistor Q_{CL}. Q_{CL} can normally be the default transistor specified in PSpice.

17) Select the parameters for the transistor Q_L. Q_L can normally be the default transistor specified in PSpice.

19) Select R_{BCL}.

20) From the maximum output current vs voltage differential, select the of I_{CL} when not in the foldback region. Then from Eqn. (4.16),

$$R_{CL} = VT \ln \frac{\left(\frac{g_B V_{REF}}{IS_{CL}}\right)}{I_{SC}}. \tag{4.30}$$

21) From the maximum output current vs voltage differential, select the value where the curve enters into the foldback region and call this voltage V_{FB}. Then from Eqn. (4.18),

$$BV_{DZFB} \approx V_{FB} - I_{MAX} R_{CL}. \tag{4.31}$$

Select NBV_{DZFB}.

22) From the maximum output current vs voltage differential, select a value

for the maximum output current and its corresponding output voltage, in the foldback region, call this V_{DIFF} and I_{DIFF}. Then from Eqn. (4.19),

$$R_{FB} = \left(\left(\frac{V_{DIFF} - V_{FB}}{VT \ln\left(\frac{g_B V_R}{IS_{CL}}\right) - I_{DIFF} R_{CL}}\right) - 1\right) R_{BCL}. \tag{4.32}$$

23) From the line transient response, determine RR_{HF}, then from Eqn. (4.8),

$$R_{BC} = \left(\left(\frac{1}{RR_{HF}} - 1\right)\left(1 + \frac{R_{22}}{R_{23}}\right)\left(\frac{R_{SCL}}{R_{CL}}\right) - 1\right) R_B. \tag{4.33}$$

24) For the ripple rejection vs frequency measurement, determine approximately where the third pole should lie. This is difficult, but it should be in the area of slightly greater than 100kHz. From Sspice, the result is,

$$C_{BC} = \frac{\left(\frac{1}{P3_{RR}} - C_L R_{SCL}\right) L_R A_{DC}}{C_P R_O R_P R_B}. \tag{4.34}$$

24) From a trial run with the macromodel, determine the value for $V_{SAT,QP}$. Select IS_{DC}. Determine the value of the load current. From the measured dropout voltage, VDO, and Eqn. (4.21),

$$N_{DDO} = \frac{VDO - V_{SAT,QP} - I_{LOAD} R_{DO}}{VT \ln\left(\frac{I_{LOAD}}{IS_{DDO}}\right)}. \tag{4.35}$$

25) From the load transient response measurement, measure the jump in the voltage when the 75Ω load is switched on and off. Then from Eqn. (4.9),

$$R_O = \frac{\Delta V_{OUT}}{V_{OUT,\ RL=75\Omega}} R_{LOAD} \qquad (4.36)$$

26) Select the parameters for the diodes D_{BL} and D_{CL}, IS and N. These may be important for convergence reasons.

This concludes the design procedure. All of the parameters for the macromodel have been selected.

4.4 DESIGN EXAMPLE FOR A SG7915

An example of the design of the SG7915 will be shown in this section. The design is based on actual laboratory measurements. The data, unless otherwise specified, will be taken off the data shown previously. The load resistor was measured at 74.96Ω. An output capacitor was required for stability. The capacitor had a series capacitance of .7561uF and a series resistance of .6156Ω at 100kHz. Based on the procedure for parameter and component selection given in section 4.3, the component and parameter selection is:

1) Set $E_A = 600$, $E_B = 1$, then $A_{DC} = 600$.

2) Set $R_{22} = 12.5k\Omega$ and $R_{23} = 2.69k\Omega$.

3) Set $V_+ = -1V$, $V_- = 1V$, and the gain of E_+ to 1. This gives $V_{MAX} = 0.3V$ and $V_{MIN} = (V(3,1) + 0.3)V$, assuming diode drops of roughly 0.7V. Select the parameters of the diodes D_+ and D_- as N = 0.1, EG = 0eV, XTI = 0, and CJO = 0F. Throughout the design example, several diodes will have the parameters EG and XTI set as above. This is done for convenience and renders IS for the diodes less temperature sensitive. Also, CJO will frequently be set to 1pF. This is done because it helps

diodes converge better in PSpice.

4) $|V_{ON}| = 2V$, so $BV_{DZ1} = 2V$. Set NBV = 0.01, EG = 0, and XTI = 0.

5) $V_{OUT} = -15.17V$, so $BV_{DZR} = 2.7117V$ set NBV = 0.01, $R_{ZR} = 1MEG\Omega$.

6) $R_Q = 42072.4191\Omega$.

7) $RR_{LF} = 61.1117db = 0.8799m$ and $r_{DZR} = .77\Omega$, so $R_R = 5.8475\Omega$.

8) The first pole of ripple rejection, $P1_{RR}$, is 5.0667kHz. Then $L_1 = .2079mH$.

9) Set $R_P = 1\Omega$.

10) Based on the power up measurements, $C_P = 1uF$.

11) Based on the power up measurements, $N_{DDIS} = 1$.

12) From the Quiescent Current vs $|V_{IN}|$ measurements, the following voltage and currents are found:

$I_1 = 1.9999mA$ $V_1 = 6.5V$

$I_2 = 4.6570mA$ $V_2 = 16V$

$I_3 = 1.4391mA$ $V_3 = 16.5V$.

Also $|V_{ON}| = 2V$. The voltage definitions give rise to the following definitions for the voltage controlled voltage sources E_{Q1-Q3}:

EQ1 30 0 table {V(1,3)} (2,0) (6.5,4.5)

EQ2 32 0 table {V(1,3)} (6.5,0) (16,9.5)

EQ3 34 0 table {V(1,3)} (16,0) (16.5,.5).

13) From the information in 12),

$R_{Q1} = 2251.1256\Omega$

$R_{Q2} = 5757.8093\Omega$

$R_{Q3} = 155.38\Omega$

14) Select the parameters for Q_P:

BF = 70k

VAF = 150V

IS = 1e-14A.

The rest of the parameters are the PSpice default parameters.

15) Set R_B = 5.

16) Let Q_{CL} be the default transistor in PSpice.

17) Let Q_L be the default transistor in PSpice.

18) Set R_{BCL} = 1000.

19) From the maximum output current vs voltage differential measurement, I_{MAX} = 3.3A, then R_{CL} = .2175Ω.

20) From the maximum output current vs voltage differential measurement, V_{FB} = 8.57V, then BV_{DZFB} = 7.8523V.

21) From the maximum output current vs voltage differential measurement, V_{DIFF} = 28.61V and I_{DIFF} = 1.3064A, then R_{FB} = 46866.3Ω.

22) From the measured line transient response, R_{BC} = 1762.01Ω.

23) Set C_{BC} = 1nF.

24) Set R_{DO} = .1Ω. $V_{SAT,QP}$ = 0.077V and V_{DO} = 0.94V for a 75Ω load, then N_{DDO} = 1.0627.

25) From the Load Transient Response Measurement, $|\Delta V_{OUT}|$ = 18mV, with a 75Ω load, then R_O = 0.0891Ω.

The room temperature macromodel parameters have been selected.

4.5 MODELING THE SG7915 AT -55 AND 125 DEGREES

The strategy for model the SG7915 is done the same way as the SG78XX for modeling at -55 degrees and 125 degrees.

4.5.1 Strategy in Modeling the SG7915 Temperature Variations

The room temperature model is developed first. The steps which need modifications are steps 4, 5, 6, 7, 8, 10, 12, 13, 19, 20, 21, and 25. These will give rise to new values for BV_{DZ1}, BV_{DZR}, R_Q, R_R, L_1, C_P, $R_{Q1\text{-}Q3}$, R_{SC}, BV_{DZFB}, R_{FB}, and R_O. Lab data will be taken and the above parameters will be selected. Temperature coefficients are then selected base on the variation of the above parameters with temperature.

4.5.2 Design Example to Include Temperature Dependance

In this section the parameters for the model for -55°C and 125°C will be developed. The temperature coefficients will be determined and then inserted into the room temperature model. This will represent the fully developed, macromodel for the SG7915.

Based on the design example given in section 4.4, the design for the -55 degree temperature model is:

4) $|V_{ON}| = 3V$, so $BV_{DZ1} = 3V$.

5) $V_{OUT} = -15.23V$, so $BV_{DZR} = 2.7225V$.

6) $R_Q = 54201.22\Omega$.

7) $RR_{LF} = 61.7733db = 0.8153m$ and $r_{DZR} = .714\Omega$, so $R_R = 7.1854\Omega$.

8) The first pole of ripple rejection, $P1_{RR}$, is 7.2333kHz. Then $L_1 = .1738mH$.

10) Based on the power up measurements, $C_P = 1uF$.

12) From the Quiescent Current vs $|V_{IN}|$ measurements, the following voltage and currents are found:

$I_1 = 2.6898mA$ $V_1 = 6.5V$

$I_2 = 6.4858mA$ $V_2 = 16V$

$I_3 = 1.60897mA$ $V_3 = 16.5V.$

At -55 degrees $V_{1\text{-}3}$ are not exact, as the controlled sources $E_{Q1\text{-}Q3}$ have not been made temperature dependent.

13) From the information in 12),

$R_{Q1} = 1681.98\Omega$

$R_{Q2} = 3654.34\Omega$

$R_{Q3} = 102\Omega$

19) From the maximum output current vs voltage differential measurement, $I_{SC} = 3.9A$, then $R_{SC} = .2161\Omega$.

20) From the maximum output current vs voltage differential measurement, $V_{FB} = 9.47V$, then $BV_{DZFB} = 9.1635V$.

21) From the maximum output current vs voltage differential measurement, $V_{DIFF} = 32.99V$ and $I_{DIFF} = .88A$, then $R_{FB} = 32846\Omega$.

25) From the Load Transient Response Measurement, $|\Delta V_{OUT}| = 9mV$, with a 75Ω load, then $R_O = 0.0443\Omega$.

The design for the 125 degree temperature is:

4) $|V_{ON}| = 1.5V$, so $BV_{DZ1} = 1.5V$.

5) $V_{OUT} = -15.18V$, so $BV_{DZR} = 2.7135V$.

6) $R_Q = 132226.92\Omega$.

7) $RR_{LF} = 58.2383db = 1.2249m$ and $r_{DZR} = 2.88\Omega$, so $R_R = 26.0725\Omega$.

8) The first pole of ripple rejection, $P1_{RR}$, is 3.1333kHz. Then L_1 = 1.4706mH.

10) Based on the power up measurements, C_P = 1uF.

12) From the Quiescent Current vs $|V_{IN}|$ measurements, the following voltage and currents are found:

I_1 = 1.3192mA V_1 = 6.5V

I_2 = 3.0980mA V_2 = 16V

I_3 = 1.1593mA V_3 = 16.5V.

At 125 degrees $V_{1\text{-}3}$ are not exact, as the controlled sources $E_{Q1\text{-}Q3}$ have not been made temperature dependent.

13) From the information in 12),

R_{Q1} = 3411.158Ω

R_{Q2} = 13951.6Ω

R_{Q3} = 257.9Ω

19) From the maximum output current vs voltage differential measurement, I_{SC} = 2.2556A, then R_{SC} = .2479Ω.

20) From the maximum output current vs voltage differential measurement, V_{FB} = 8.1001V, then BV_{DZFB} = 7.5408V.

21) From the maximum output current vs voltage differential measurement, V_{DIFF} = 29.06V and I_{DIFF} = .8834A, then R_{FB} = 61609.9Ω.

25) From the load transient response measurement, $|\Delta V_{OUT}|$ = 20mV, with a 75Ω load, then R_O = 0.0988Ω.

A final summary of the temperature dependent parameters and elements follows in Table 4.1.

element or parameter	value at 25 degrees	value at -55 degrees	value at 125 degrees
BV_{DZ1}	2	3	1.5
BV_{DZR}	2.7117	2.7225	2.7135
R_Q	42072.4191	54201.22	132226.92
R_R	5.8475	7.1854	26.0725
L_1	0.2079m	.1738m	1.4706m
C_P	1u	1u	1u
R_{Q1}	2251.1256	1681.98	3411.158
R_{Q2}	5757.8093	3654.34	13951.6
R_{Q3}	155.38	102	257.9
R_{SC}	.2175	.2161	.2479
BV_{DZFB}	7.8523	9.1635	7.5408
R_{FB}	46866.3	32846.0	61609.88
R_O	0.0891	0.0443	0.0988

Table 4.1 Temperature dependent parameters and elements

Solving for the linear and quadratic coefficients for each of these components and parameters leads to the following results for Table 4.2

element or parameter	TC1 or TBV1 (linear coeff.)	TC2 or TBV2 (quadratic coeff.)
BV_{DZ1}	-0.004583	2.08333e-5
BV_{DZR}	-2.4708e-5	3.1346e-7
R_Q	0.007522	1.3907e-4
R_R	.01378	2.0804e-4
L_1	0.02119	3.9548e-4
C_P	0	0
R_{Q1}	0.004046	1.1071e-5
R_{Q2}	0.008862	5.3689e-5
R_{Q3}	0.005318	1.2798e-5
R_{SC}	6.659e-4	7.318e-6
BV_{DZFB}	-0.001336	9.3921e-6
R_{FB}	0.003476	-3.2975e-6
R_O	0.003976	-2.8869e-5

Table 4.2 Temperature coefficients

The final macromodel for the SG7915 follows. The macromodel includes the effects of temperature.

```
.SUBCKT SG7915  1       2       3
*                   GND   OUT    IN
*
L1     4 1 IND1 .2079m
.MODEL IND1 IND (TC1=0.021188 TC2=3.9548E-4)
DZR    29 4 DZR
.MODEL DZR D (BV=2.7117 TBV1=-2.4708E-5 TBV2=3.1346E-7 NBV=0.01 EG=0
XTI=0 CJO=1P)
RR     29 15 5.8475 TC=0.013783,2.0804E-4
RQ     15 22 42072.4191 TC=0.007522,1.3907E-4
D1     3 22 D1
.MODEL D1 D (BV=2 TBV1=-0.004583 TBV2=2.08333E-5 NBV=0.01 EG=0 XTI=0
CJO=1P)
FQ     1 3 POLY (3) VQ1 VQ2 VQ3 0 1 1 -1
EA     9 3 5 15 600
RO     6 9 200
D+     6 20 DC
E+     20 21 1 3 1
V+     21 3 -1
D-     19 6 DC
.MODEL DC D (EG=0 XTI=0 CJO=1P)
V-     19 3 DC 1
RP     6 7 1
CP     7 3 1U
EQ1    23 0 TABLE {V(1,3)} (2,0) (6.5,4.5)
VQ1    23 24 DC 0
RQ1    24 0 2300.0318 TC=0.004046,1.1071E-5
EQ2    25 0 TABLE {V(1,3)} (6.5,0) (16,9.5)
VQ2    25 26 DC 0
RQ2    26 0 6670.73 TC=0.008862,5.369E-5
EQ3    27 0 TABLE {V(1,3)} (16,0) (16.5,.5)
VQ3    27 28 DC 0
RQ3    28 0 155.4 TC=0.005318,1.2798E-5
GB     1 8 1 15 4M
GCOMP  3 1 1 15 4M
DB     8 18 DB
.MODEL DB D (N=.1 EG=0 XTI=0 CJO=1P RS=.1)
EB     18 3 7 3 1
RB     8 10 10
QL     1 14 14 QTEMP
.MODEL QTEMP NPN
RFB    12 14 46.8663K TC=.003476,-3.2976E-6
DZFB   13 12 DZFB
```

```
.MODEL DZFB D (BV=7.8523 TBV1=-0.001336 TBV2=9.3921E-6 NBV=0.1)
QCL     10 13 3 QMOD
RBCL    13 17 1000
RCL     17 3 .2175 TC=6.659E-4,7.318E-6
RBC     11 14 1762
CBC     10 11 1N
QP      16 10 17 QMOD
.MODEL QMOD NPN (IS=1E-14 BF=70000 VAF=150)
DDO     14 30 DDO
.MODEL DDO D (N=1.0627)
RDO     30 16 .1
R23     1 5 2.69K
R22     5 14 12.5K
ROUT    14 2 0.0891 TC=.003976,-2.8869E-5
DDIS    3 14 DDIS
.MODEL DDIS D(IS=1E-12)
.ENDS SG7915
```

4.5.3 Comparison of Macromodel Predictions with Lab Results

A comparison of macromodel predictions with lab results is presented in this section.

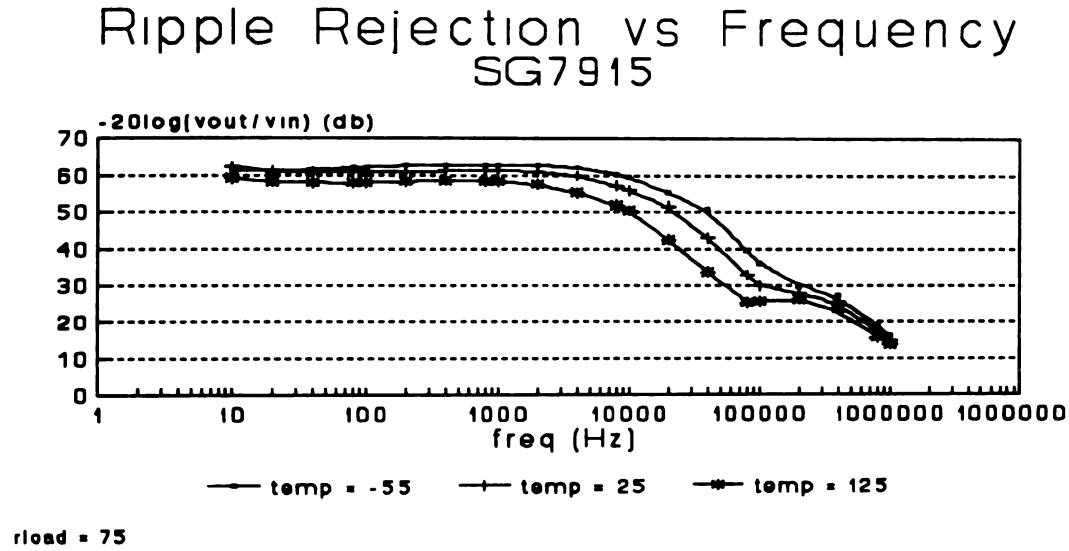

Figure 4.8 Ripple rejection vs frequency, measured

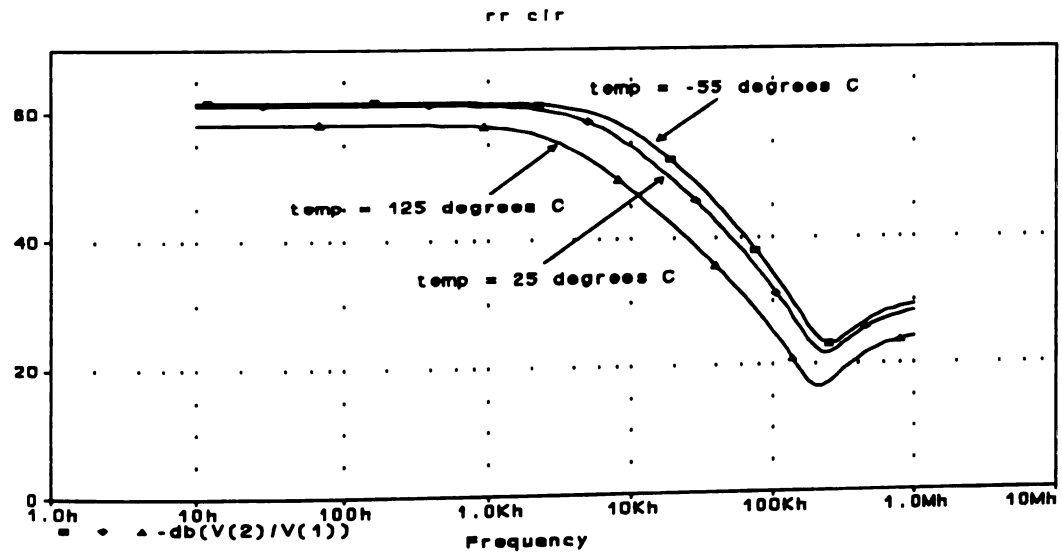

Figure 4.9 Ripple rejection vs frequency, macromodel

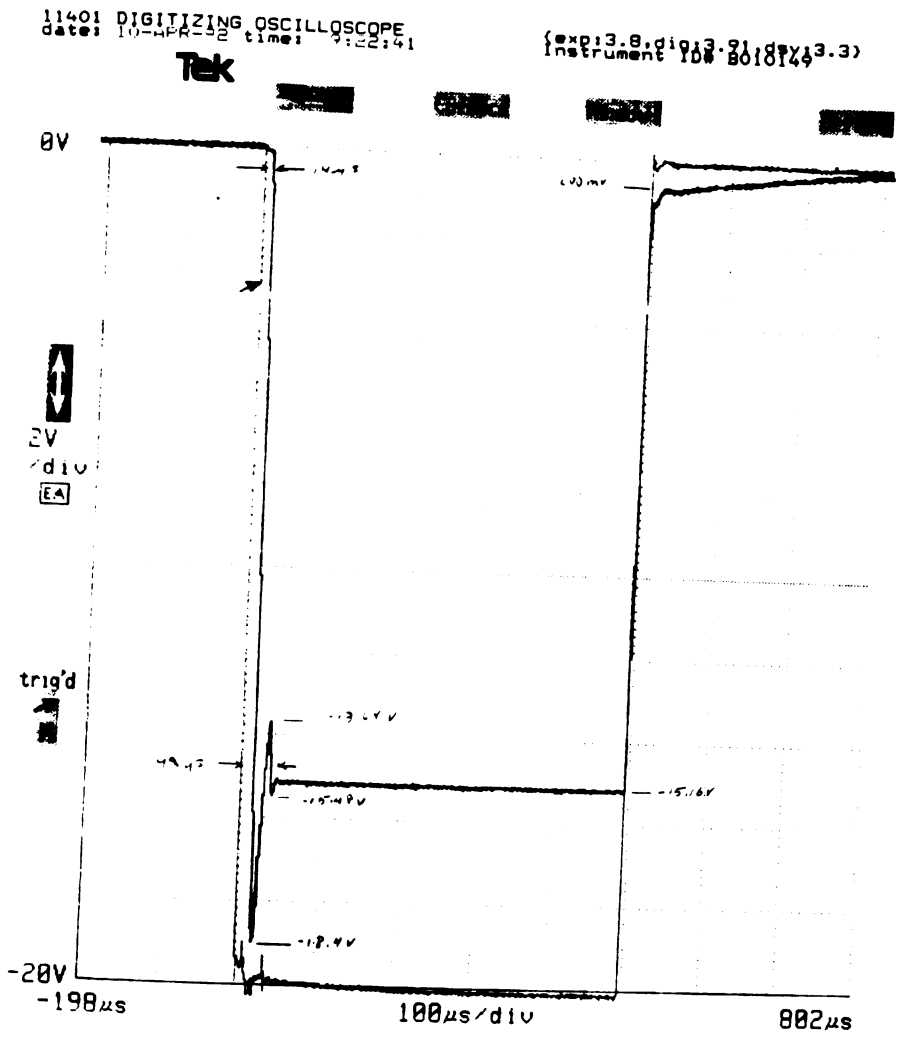

Figure 4.10 Power up and down, square wave, measured

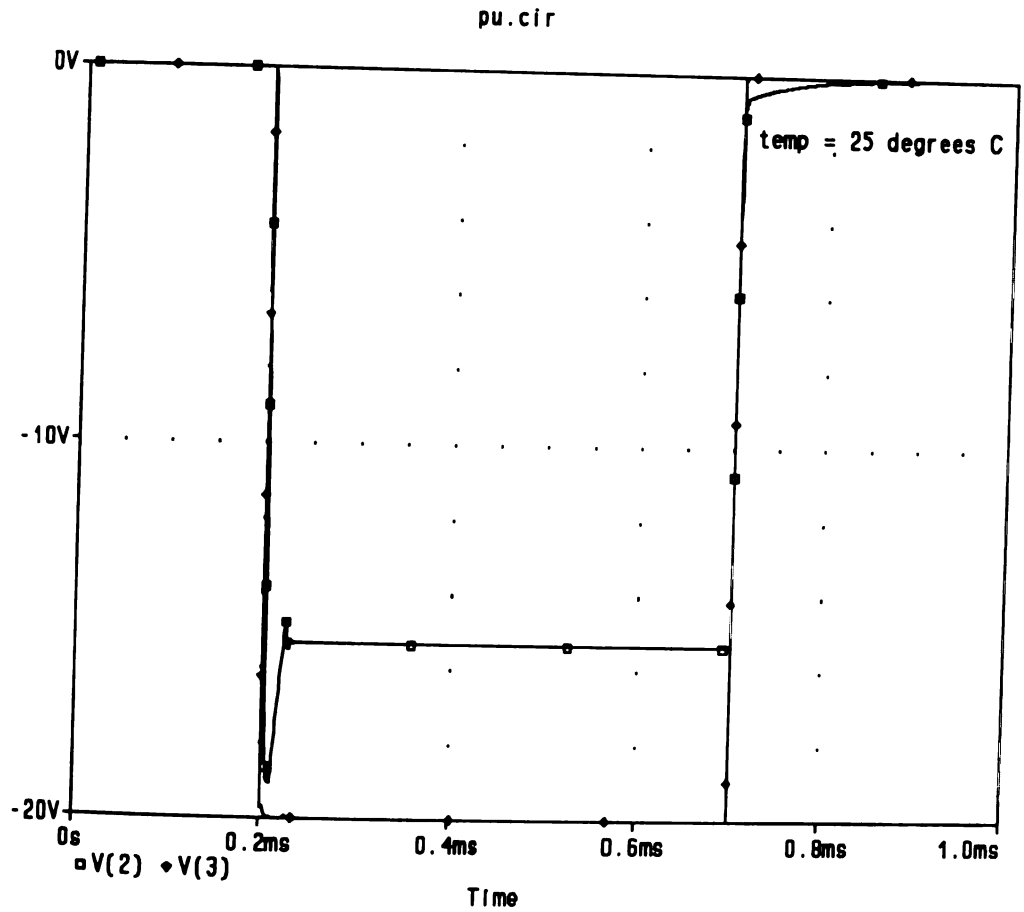

Figure 4.11 Power up and down, square wave, macromodel

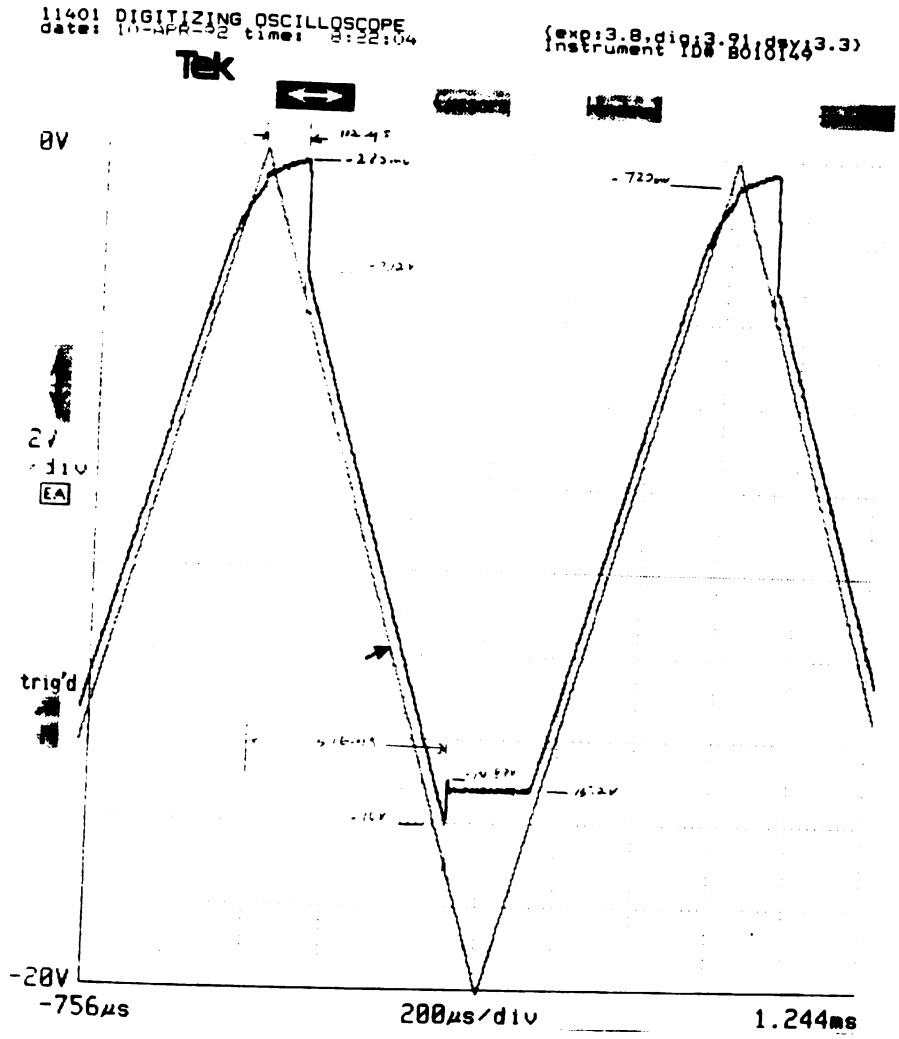

Figure 4.12 Power up and down, triangle wave, measured

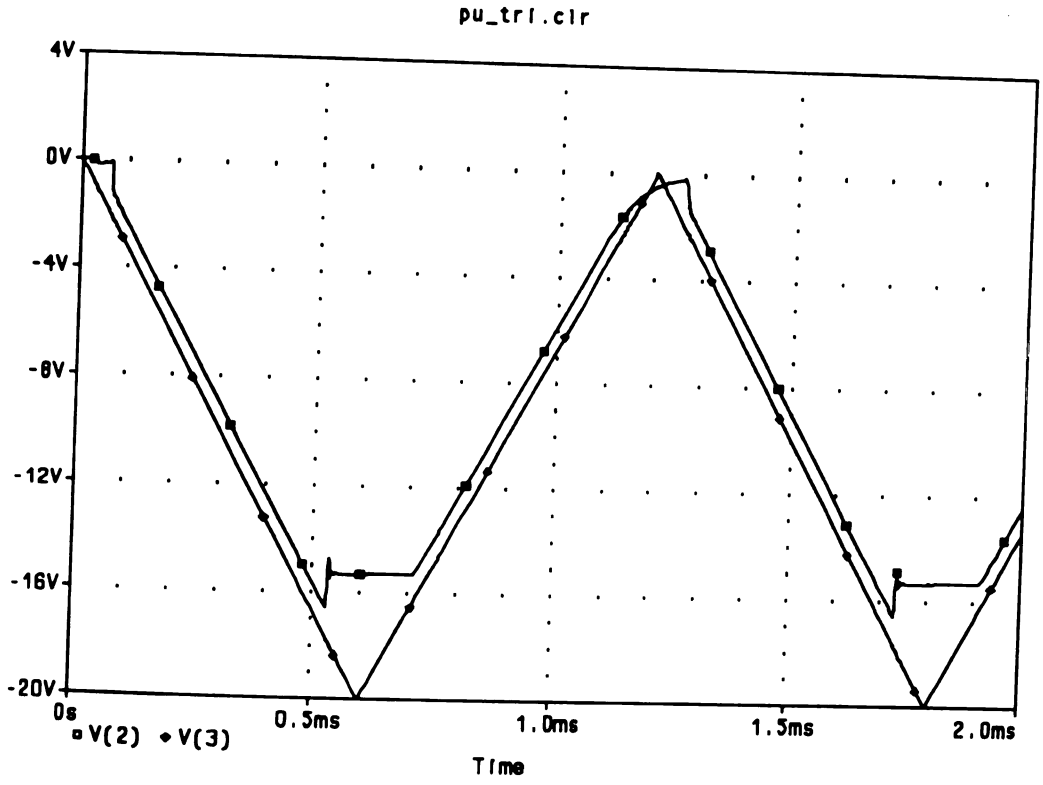

Figure 4.13 Power up and down, triangle wave, macromodel

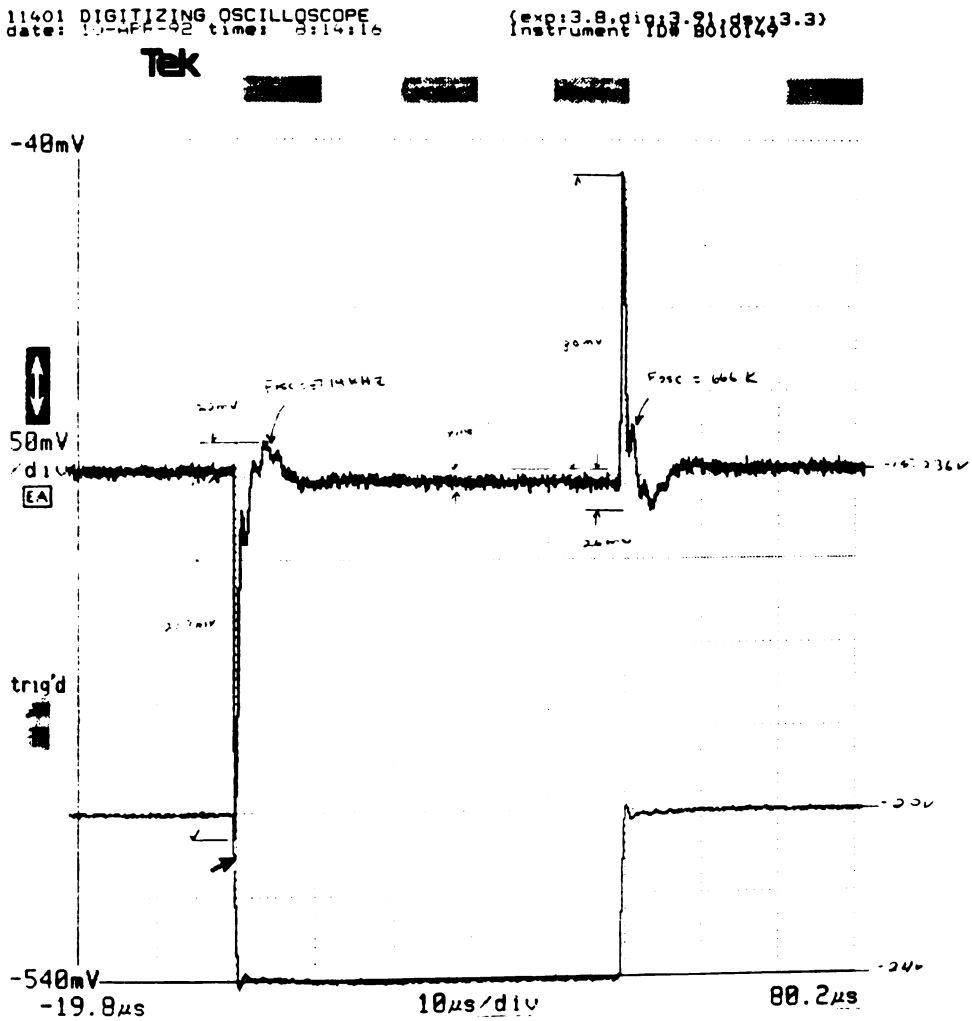

Figure 4.14 Line transient response, measured

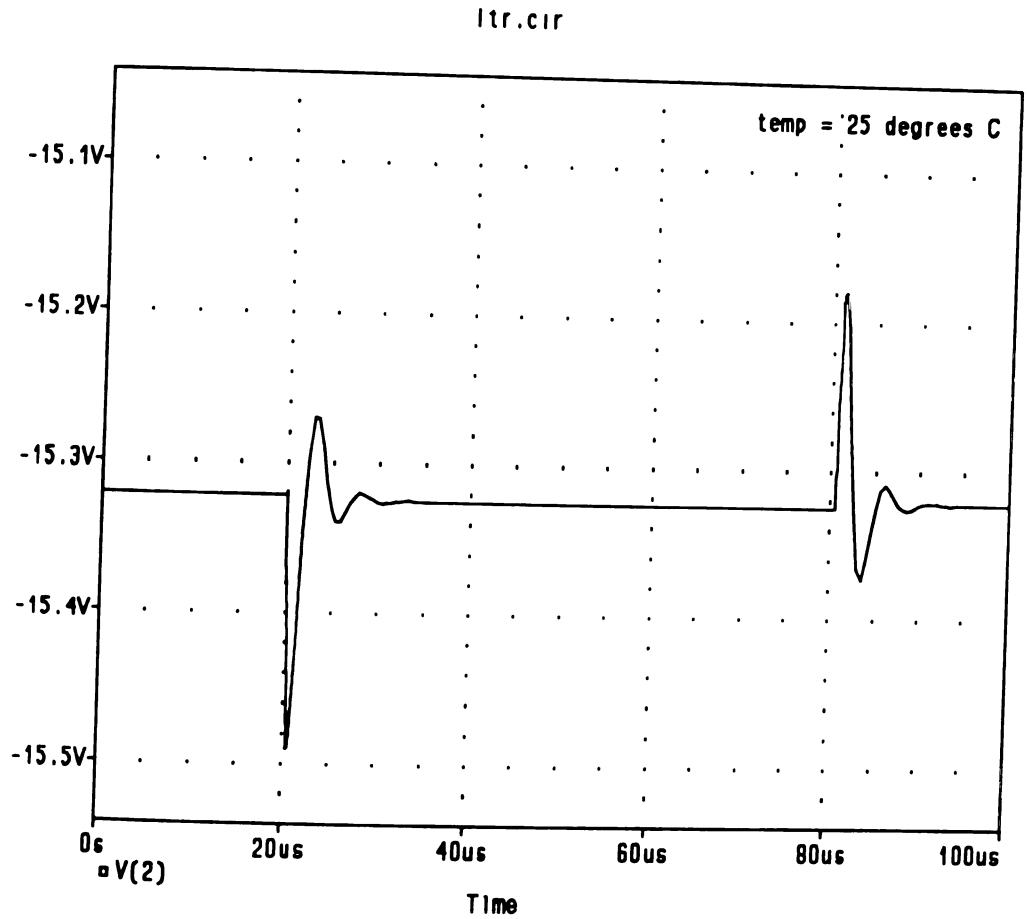

Figure 4.15 Line transient response, macromodel

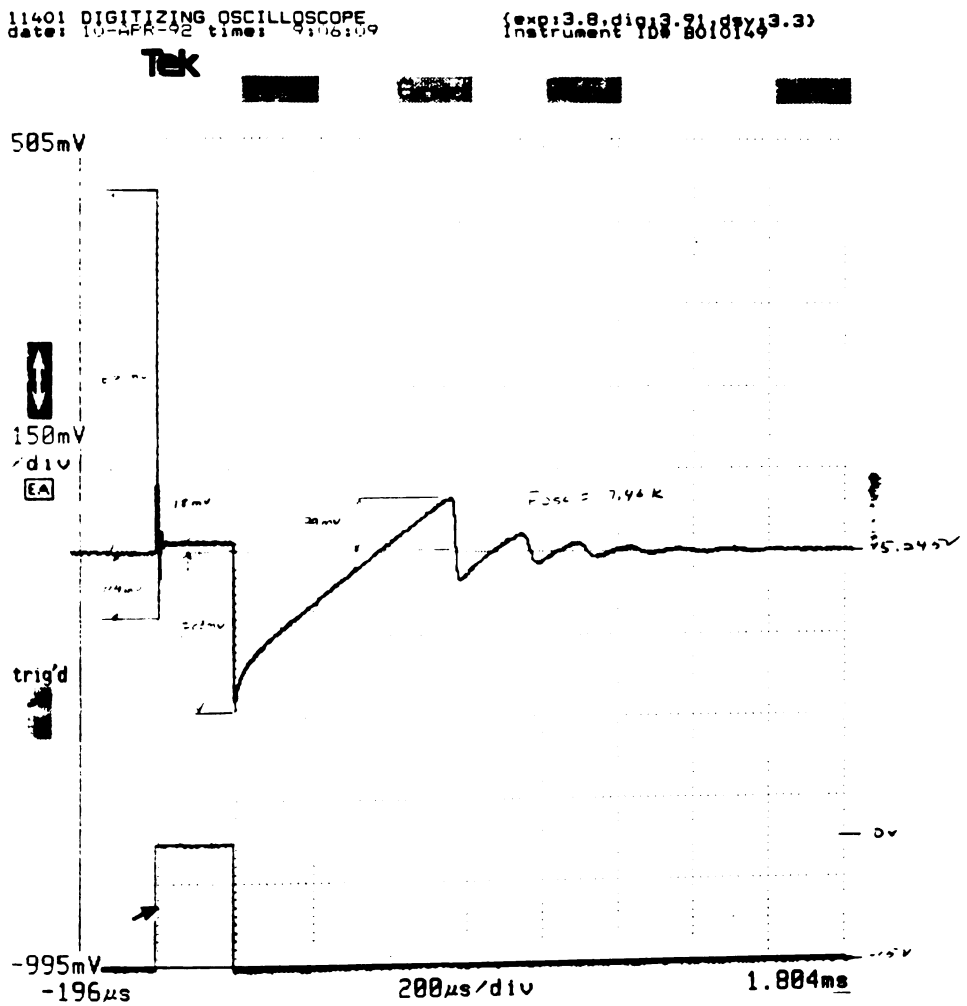

Figure 4.16 Load transient response, measured

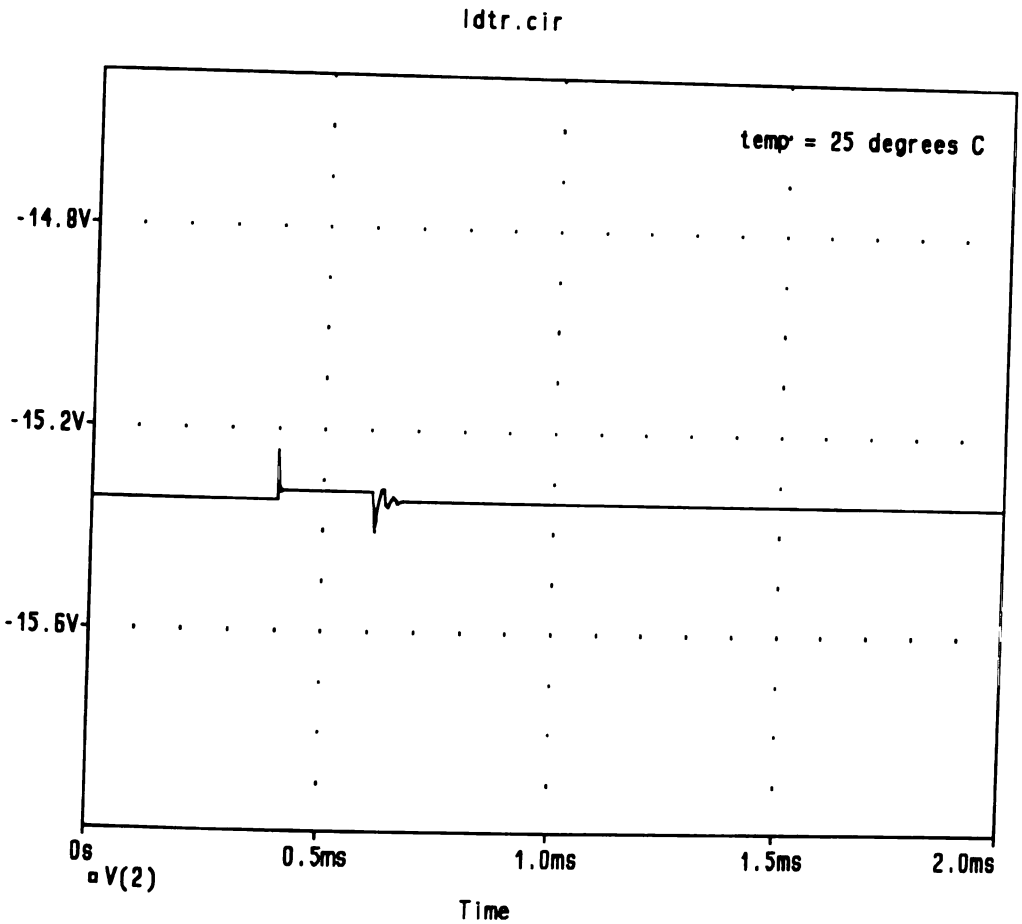

Figure 4.17 Load transient response, macromodel

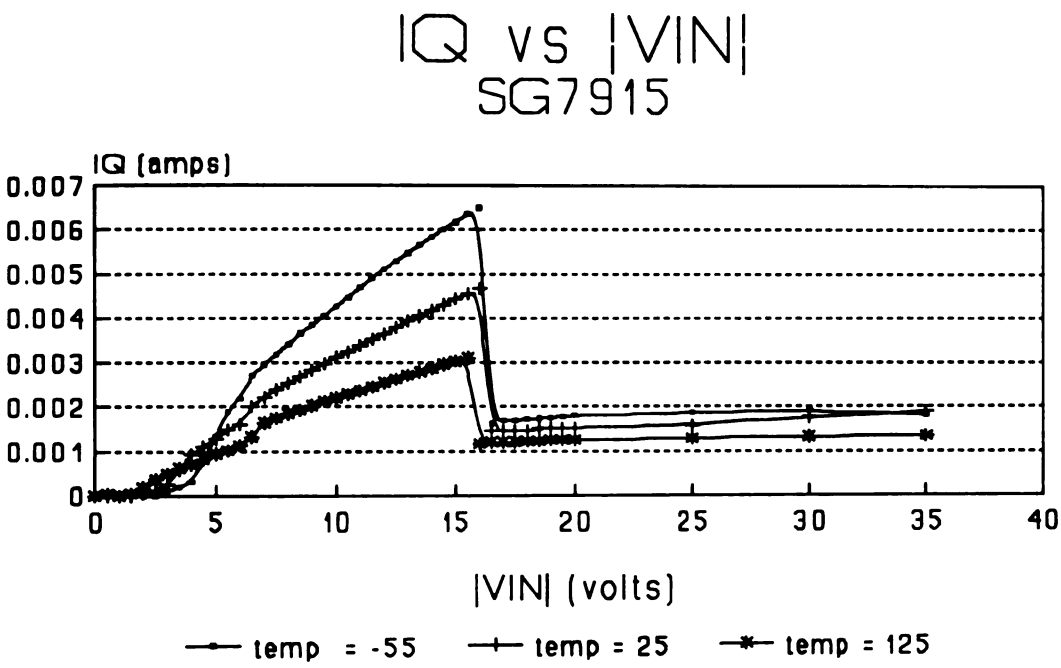

Figure 4.18 Quiescent current vs $|V_{IN}|$, measured

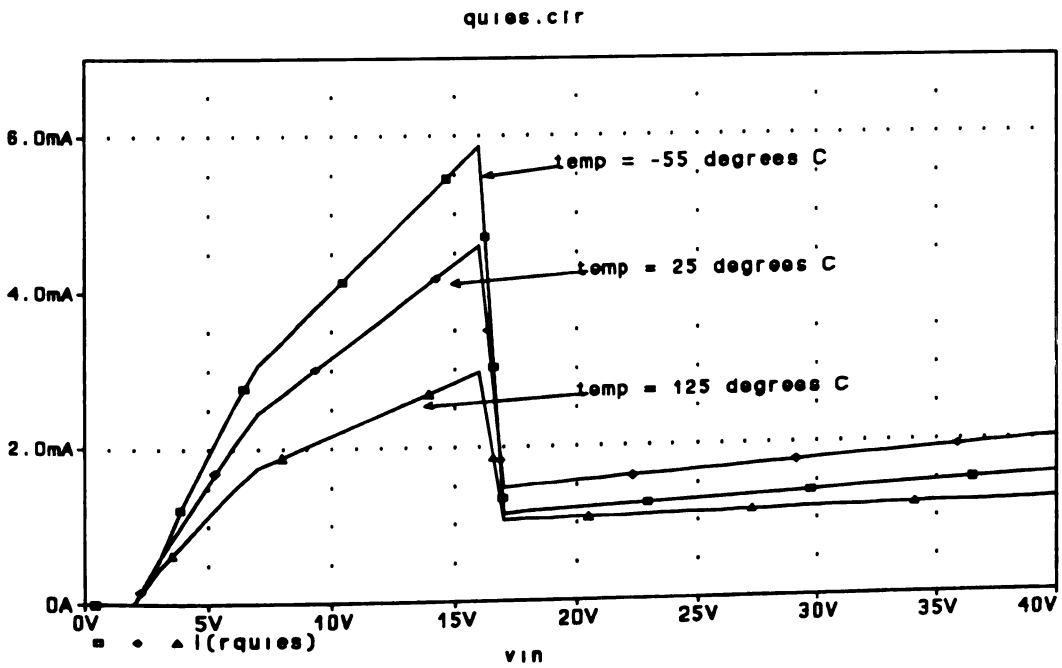

Figure 4.19 Quiescent current vs $|V_{IN}|$, macromodel

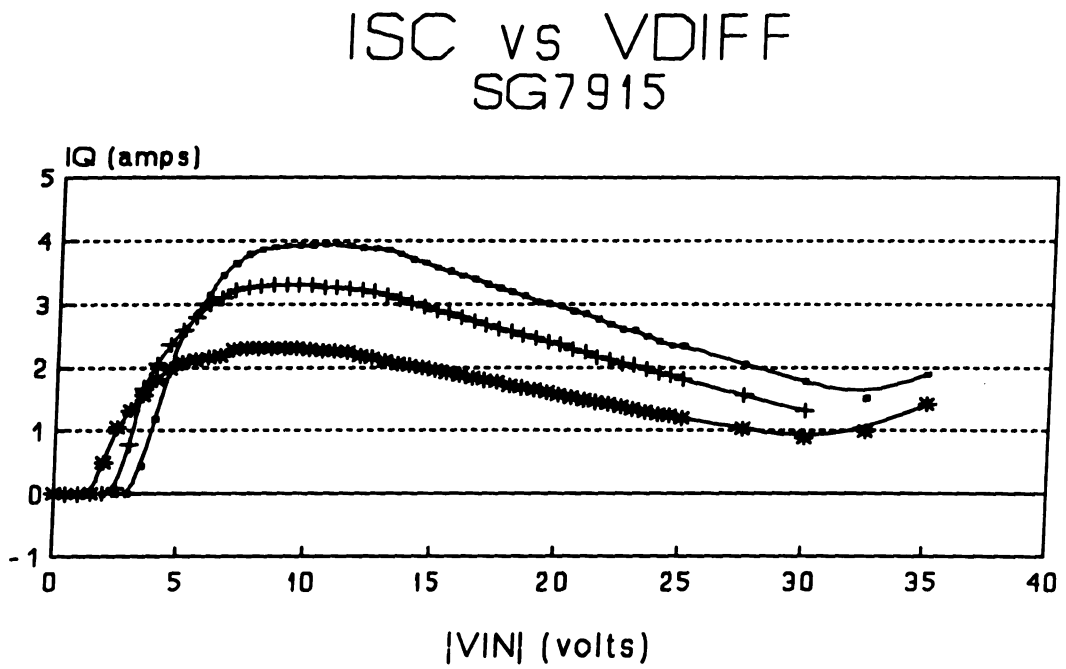

Figure 4.20 Maximum output current vs $|V_{IN}|$, measured

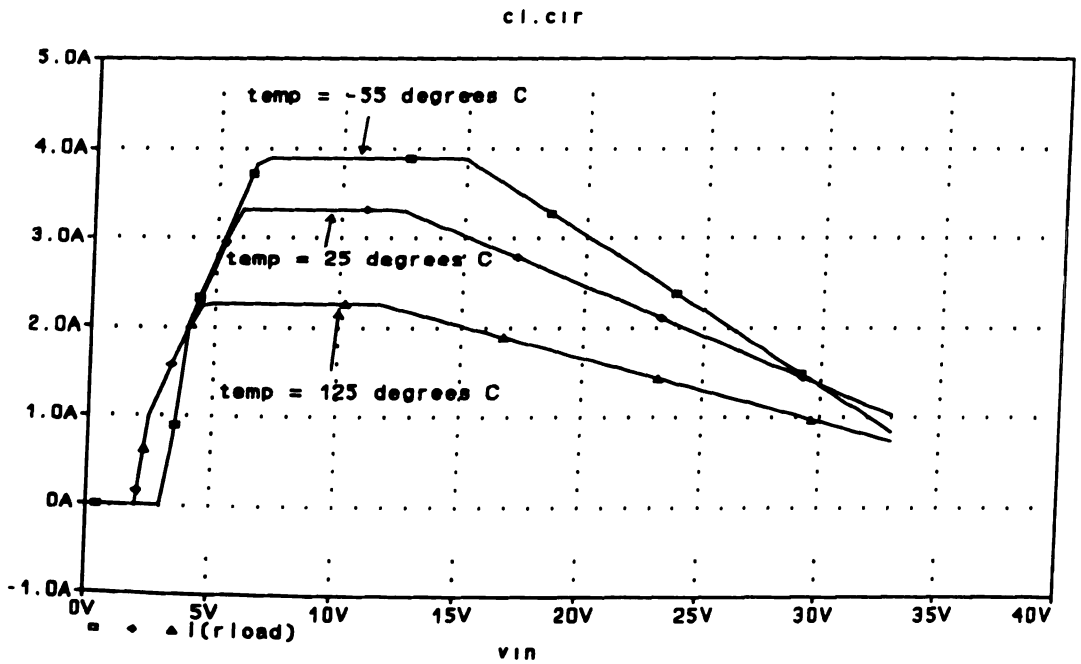

Figure 4.21 Maximum output current vs $|V_{IN}|$, macromodel

Comparison of Macromodel parameters and Measured Parameters				
QUANTITY		**-55°C**	**25°C**	**125°C**
RR_{LF}	lab	61.8db	61.1db	58.2db
	model	61.7db	61.2db	58.2db
$P1_{RR}$	lab	7.233kHz	5.067kHz	3.133kHz
	model	6.558kHz	4.9506kHz	3.074kHz
IQ_{MAX}	lab	6.486mA	4.657mA	3.098mA
	model	5.874mA	4.595mA	2.971mA
$IQ_{@VIN=-20V}$	lab	1.789mA	1.519mA	1.239mA
	model	1.194mA	1.542mA	1.073mA
$\Delta IQ/\Delta Vin$	lab	18.45u	23.76u	7.56u
	model	18.045u	24.11u	7.807u
maximum output current	lab	3.947A	3.299A	2.303A
	model	3.893A	3.314A	2.265A
dropout voltage	lab	.8V	.94V	.78V
	model	1.088V	1.0622V	.924V
output resistance	lab	0.0443Ω	0.0891Ω	0.0988Ω
	model	0.046Ω	0.091Ω	.103Ω

Table 4.3 Macromodel comparisons with lab data

This concludes the comparison of the macromodel with lab results as well as the description of the development of the SG7915 macromodel.

4.6 TEST CIRCUITS

4.6.1 Pspice Test Circuits

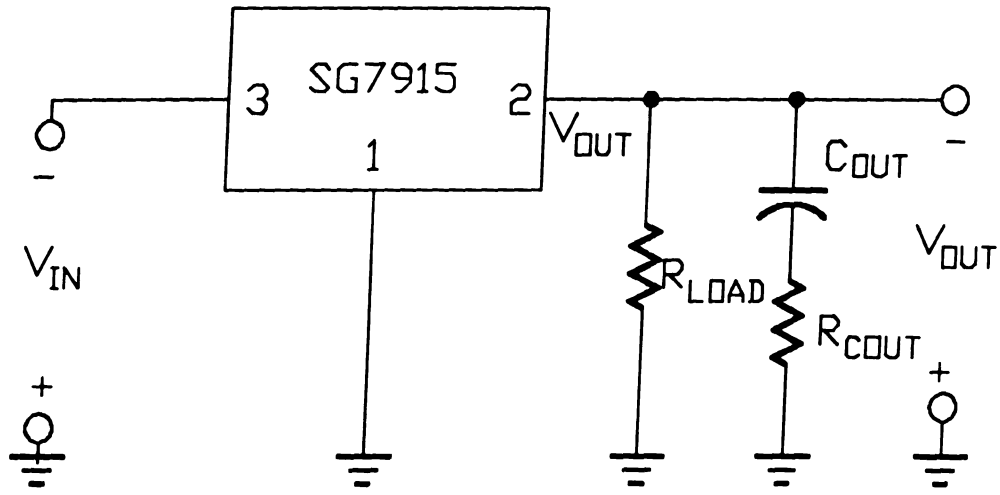

Figure 4.22 Basic PSpice test circuit

```
RI
*
*T
*
VI
VA
RL
CO
RC
XR
.OP
.LI
.OP
.AC
.TE
.PR
.EN
```

```
PU.C
*
*pow
*
ROU
COU
RCO
XI
VP
RP
.OPTI
.LIB S
.TEMP
.TRAN
.PROB
.END
```

```
RR.CIR
*
*ripple rejection for the sg7915
*
VIN     3 0 DC -20
VAC     1 3 AC 1
RLOAD   2 0 74.96
COUT    2 4 .7561u
RCOUT   4 0 .6156
XREG    0 2 1 sg7915
.OP
.LIB SG7915.LIB
.OPTIONS NUMDGT=10 ITL5=0 ITL1=300 ITL2=300
.AC DEC 20 10 1MEG
.TEMP -55 25 125
.PROBE
.END
```

```
PU.CIR
*
*power up for the SG7915
*
ROUT    2 0 74.96
COUT    2 4 .7561u
RCOUT   4 0 .6156
X1      0 2 3 SG7915
VP      5 0 PULSE (0 -20 200u 0 0 500u)
RP      5 3 0.1
.OPTIONS NUMDGT=10 ITL5=0 ITL1=300 ITL2=300
.LIB SG7915.LIB
.TEMP -55 25 125
.TRAN 1u 1000u 0 1u
.PROBE
.END
```

```
PU_TRI.CIR
*
*power up, with triangle wave, for the sg7915
*
ROUT    2 0 74.96
COUT    2 4 .7561u
RCOUT   4 0 .6156
X1      0 2 3 sg7915
VP      5 0 PULSE (0 -20 0 600u 600u 1u 1202u)
RP      5 3 0.0001
.OPTIONS NUMDGT=10 ITL5=0
.LIB SG7915.LIB
.TRAN 2.5u 2000u 2.5u
.TEMP -55 25 125
.PROBE
.END
```

```
LTR.CIR
*
*line transient response for the sg7915
*
ROUT    2 0 74.96
COUT    2 10 .7561u
RCOUT   10 0 .6156
X1      0 2 3 sg7915
VIN     11 0 DC -20
VP      3 11 PULSE (0 -4 20u 0u 0u 60u)
.OPTIONS NUMDGT=10 ITL5=0 ITL1=300 ITL2=300
.LIB SG7915.LIB
.TEMP -55 25 125
.TRAN .5u 100u 0 .5u
.PROBE
.END
```

```
LDTR.CIR
*
*load transient response for the sg7815
*
VP      10 0 PULSE (-15 0 400u 0 0 200u)
RLOAD   2 10 75
COUT    2 11 1u
RCOUT   11 0 1.5
X1      0 2 3 SG7915
VIN     3 0 DC -20
.OPTIONS NUMDGT=10 ITL5=0 ITL1=300 ITL2=300
.TRAN 5u 2000u 0 5u
.LIB SG7915.LIB
.TEMP -55 25 125
.PROBE
.END
```

```
QUIES.CIR
*
*quiescent current for the sg7915
*
RQUIES  0 1 100.06
VIN     0 3 dc 20
RLOAD   2 0 1e8
COUT    2 10 7.561e-6
RCOUT   10 0 0.6156
XREG    1 2 3 SG7915
.OPTIONS NUMDGT=10 ITL1=300 ITL2=300
.LIB SG7915.LIB
.DC VIN  0 40 1
.TEMP -55 25 125
.PROBE
.END
```

```
CL.CIR
*
*short circuit current for the sg7915
*
VIN     0 3 DC -10
RLOAD   0 2 1.0532
COUT    2 4 .7561u
RCOUT   4 0 .6156
XREG    0 2 3 SG7915
.OPTIONS NUMDGT=10 ITL5=0 ITL1=300 ITL2=300
.LIB SG7915.LIB
.TEMP -55 25 125
.DC VIN 0 33 0.5
.PROBE
.END
```

```
VDO.CIR
*
*dropout characteristics for the sg7915
*
VIN     0 3 DC -10
RLOAD   0 2 74.96
COUT    2 10 .7561u
RCOUT   10 0 .6156
XREG    0 2 3 sg7915
.OPTIONS NUMDGT=10 ITL5=0 ITL1=300 ITL2=300
.LIB SG7915.LIB
.DC VIN 0 20 0.1
.PARAM RES=75
.TEMP -55 25 125
.PROBE
.END
```

4.6.2 Measurement Test Circuits

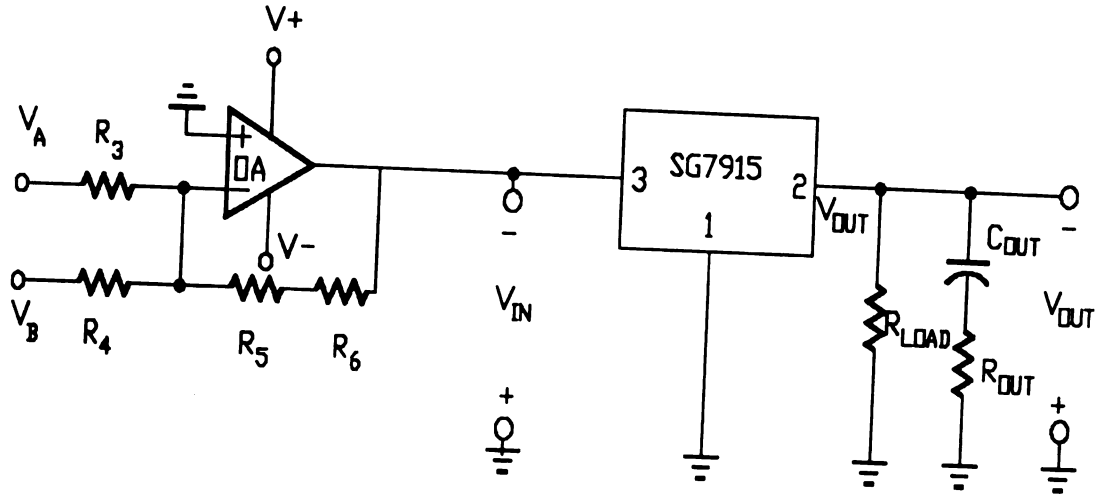

Figure 4.23 Test circuit No. 1

The conditions of test circuit No. 1 are stated.

C_{OUT} measured .7561uF at 100kHz.

R_{COUT} represents the series resistance of C_{OUT} and measured .6156Ω at 100kHz.

R_3, R_4, R_5, and R_6 have nominal values of 1kΩ.

V+ is a positive 10V dc power supply.

V- is a negative 50V dc power supply.

OA is a Burr-Brown OPA541 Op-Amp.

The SG7915 resides inside a temperature chamber. Wires are connected at the terminals of the SG7915 to allow it to be connected outside the chamber to the test circuit.

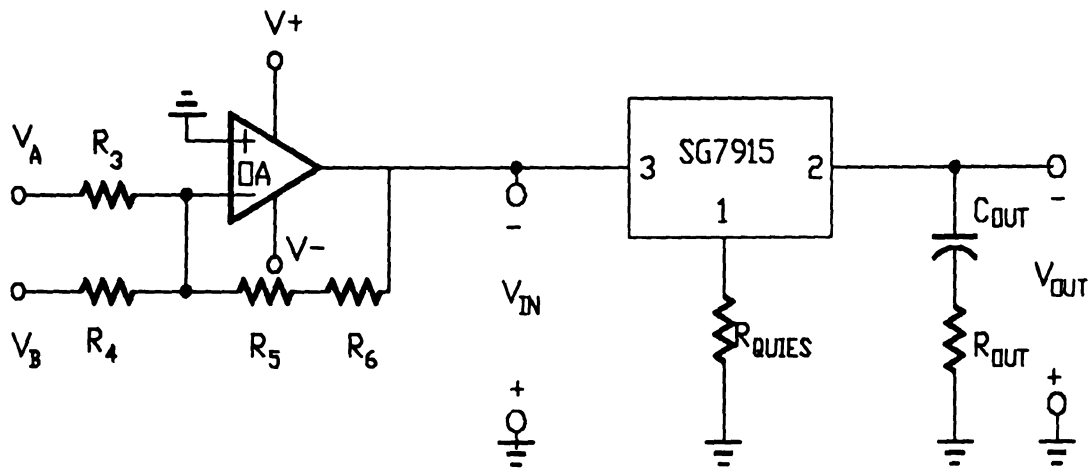

Figure 4.24 Test circuit No. 2

The conditions of test circuit No. 2 are stated.

C_{OUT} measured .7561uF at 100kHz.

R_{COUT} represents the series resistance of C_{OUT} and measured .6156Ω at 100kHz.

R_3, R_4, R_5, and R_6 have nominal values of 1kΩ.

V+ is a positive 10V dc power supply.

V- is a negative 50V dc power supply.

OA is a Burr-Brown OPA541 Op-Amp.

The SG7915 resides inside a temperature chamber. Wires are connected at the terminals of the SG7915 to allow it to be connected outside the chamber to the test circuit.

R_{QUIES} has a nominal value of 100Ω, and measured 100.06Ω.

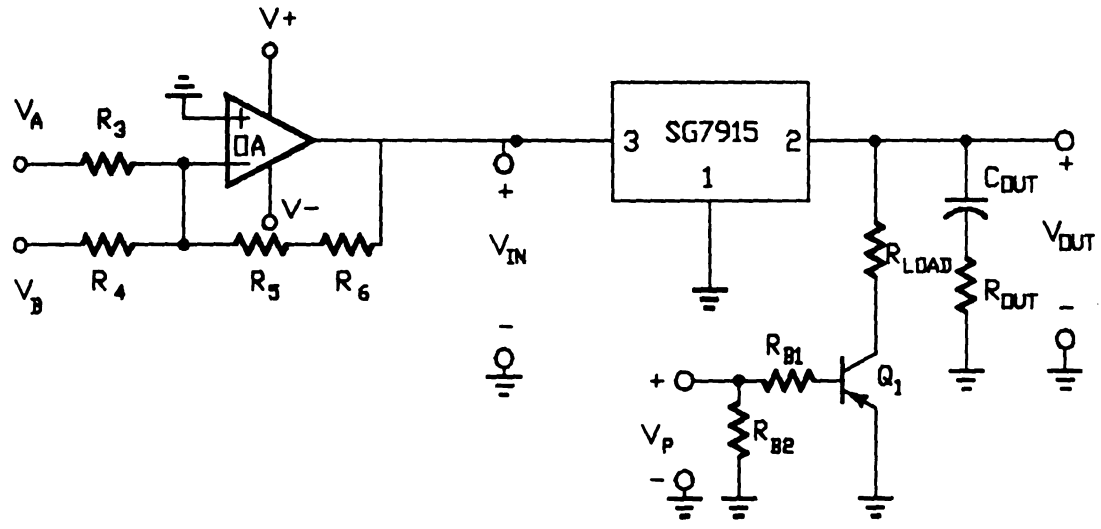

Figure 4.25 Test circuit No. 3

The conditions of test circuit No. 3 are stated.

C_{OUT} measured .7561uF at 100kHz.

R_{COUT} represents the series resistance of C_{OUT} and measured .6156Ω at 100kHz.

R_3, R_4, R_5, and R_6 have nominal values of 1kΩ.

V+ is a positive 10V supply.

V- is a negative 50V supply.

OA is a Burr-Brown OPA541 Op-Amp.

The SG7915 resides inside a temperature chamber. Wires are connected at the terminals of the SG7915 to allow it to be connected outside the chamber to the test circuit.

Q_1 is a 2N4403 pnp transistor.

R_{B1} has a measured value of 5.526kΩ.

R_{B2} has a measured value of 62.430Ω.

1) Ripple rejection was done using test circuit 1. V_A was connected to an ac function generator. V_B was connected to a negative dc power supply. These were set to produce a -20V dc voltage at V_{IN}, with a sine wave superimposed. R_{LOAD} measured 74.96Ω. Voltages and phases were measured with a Tektronix 11401 scope.

2) The V_{IN} vs V_{OUT} and V_{OUT} at V_{IN} = -20V measurements were done using test circuit 1. V_A was connected to an pulse generator and pulsed at 100Hz, with a duty cycle of 5%. V_B was grounded. These were set to produce the necessary voltage at V_{IN}. R_{LOAD}, when used, measured 74.96Ω. Voltages were measured with a Tektronix 11401 scope.

3) The power up and down square wave measurements were done using test circuit 1. V_A was connected to an pulse generator. V_B was grounded. R_{LOAD} measured 74.96Ω. Voltages were measured with a Tektronix 11401 scope.

4) The power up and down triangle measurement was done using test circuit 1. V_A was connected to an ac function generator, generating a triangle wave. V_B was connected to a negative dc power supply. These were set to produce a triangle wave at V_{IN} which has a maximum value of 0V, and a minimum value of -20V. R_{LOAD} measured 74.96Ω. Voltages were measured with a Tektronix 11401 scope.

5) The quiescent current measurements were done using test circuit 2. V_A was connected to an pulse generator and pulsed at 100Hz, with a duty cycle of 5%. V_B was grounded. These were set to produce the necessary voltage at V_{IN}. R_{QUIES} measured 100.06Ω. Voltages were measured with a Tektronix 11401 scope. The voltage was measured across R_{QUIES} and divided by R_{QUIES} to give the quiescent current.

6) The load transient response measurement was done with test circuit 3. V_A was grounded. V_B was connected to a negative power supply to produce a dc voltage of -20V at V_{IN}. V_P was pulsed to allow Q1 to function as a switch, connecting R_{LOAD} on and off to ground to simulate the switching on and off of a load.

7) The maximum output current vs V_{IN} measurements were done using test circuit 1. V_A was connected to an pulse generator and pulsed at 100Hz, with a duty cycle of 5%. V_B was grounded. These were set to produce the necessary voltage at V_{IN}. R_{LOAD} measured 1.0530Ω. Voltages were measured with a Tektronix 11401 scope. The voltage measured at R_{LOAD} was then converted to a current.

8) The line transient response measurement was done with test circuit 1. V_A was connected to a pulse generator. V_B was connected to a negative dc power supply. These were set to produce a -20V dc voltage at V_{IN}, with a square wave superimposed. R_{LOAD} measured 74.96Ω. Voltages and phases were measured with a Tektronix 11401 scope.

CHAPTER 5

CA3085 MACROMODEL DEVELOPMENT

5.1 INTRODUCTION

This chapter describes the development of the CA3085 voltage regulator macromodel. The CA3085 is a 10-pin, programmable, positive voltage regulator.

5.2 DEVELOPMENT

The CA3085 functional block diagram is shown in Fig. (5.1). Fig. (5.2) shows the

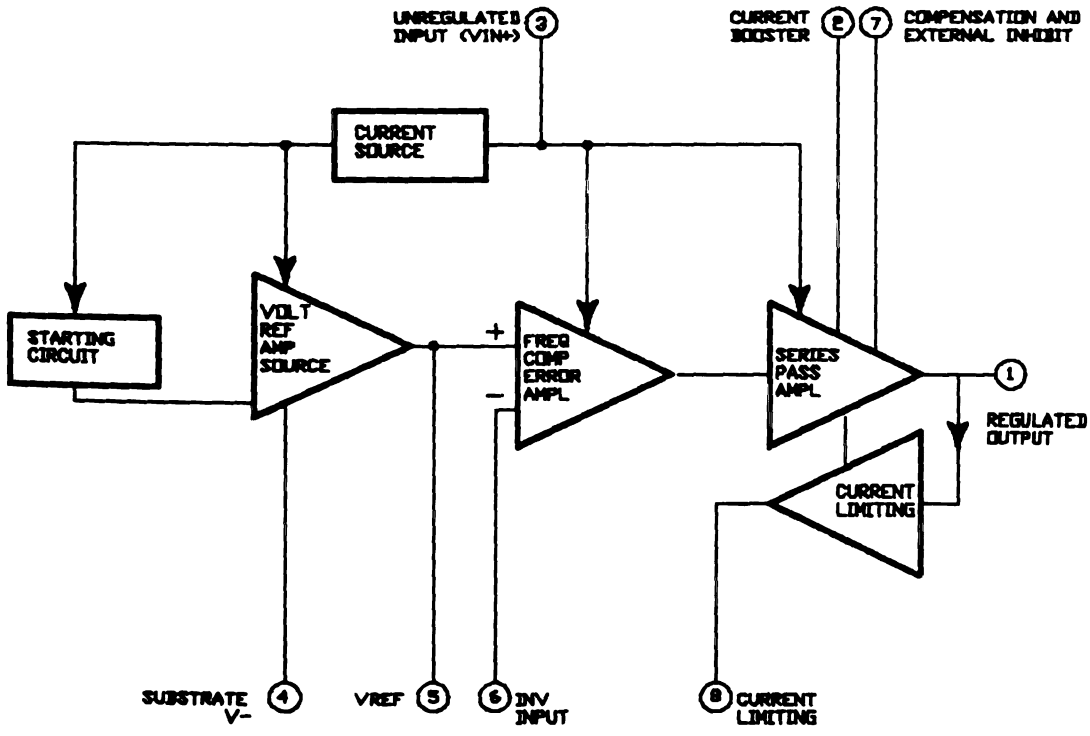

Figure 5.1 Functional block diagram for the CA3085

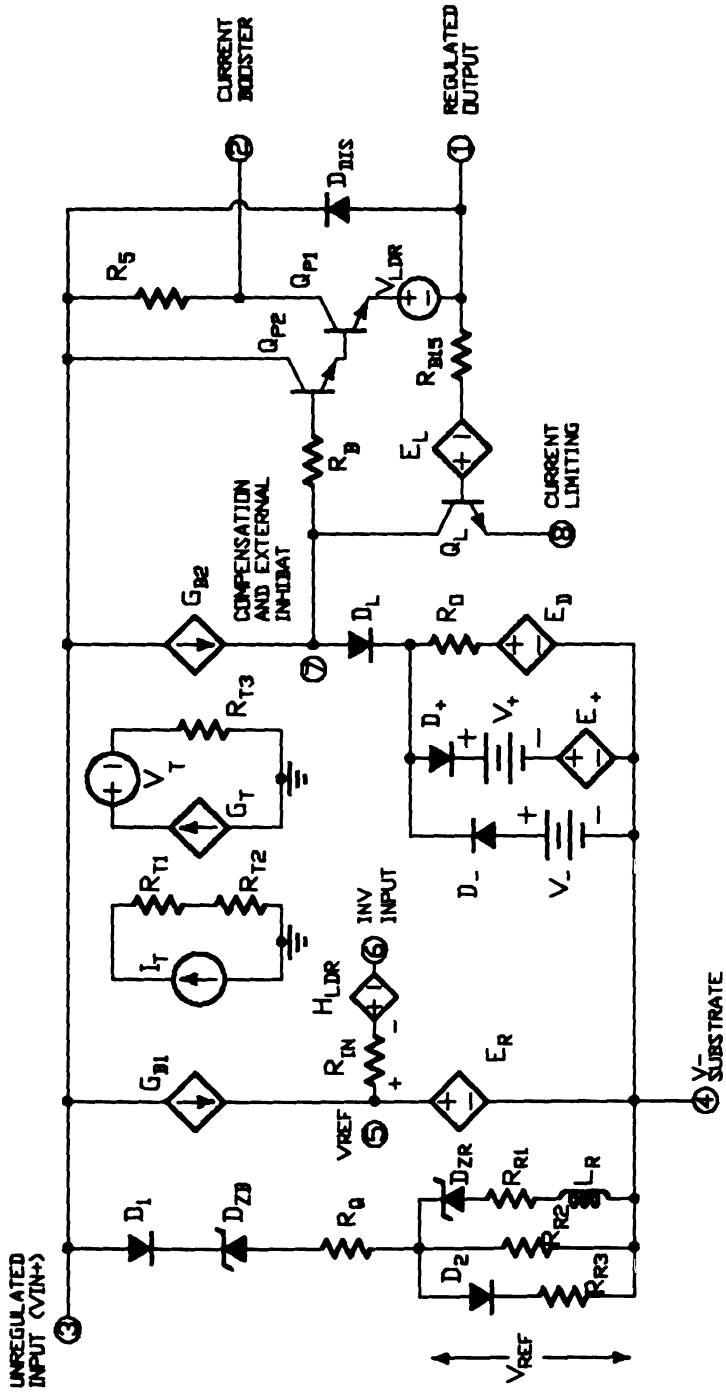

Figure 5.2 Macromodel for the CA3085

macromodel for the CA3085. The voltage reference amplifier source is replaced by D_1, D_{ZR}, D_{ZB}, D_2, R_{R1}, R_{R2}, R_{R3}, R_Q, L_R, and E_R. The current source is replaced by G_{B1} and G_{B2}. The Frequency Compensated Error Amplifier is replaced by E_D, R_{IN}, D_L, D_+, D_-, E_+, V_+, V_-, and R_O. The Series Pass Amplifier is replaced by R_B, Q_{P1}, Q_{P2}, and R_5. The Current Limiting block is replaced by Q_L, E_L, and R_{B15}. V_{LDR} and H_{LDR} are added to provide load regulation characteristics. I_T, G_T, V_T, R_{T1}, R_{T2}, and R_{T3} provide circuitry which detects the change in ambient temperature from a nominal value. Finally, D_{DIS} provides capacitive discharge characteristics. This gives an overview of the macromodel.

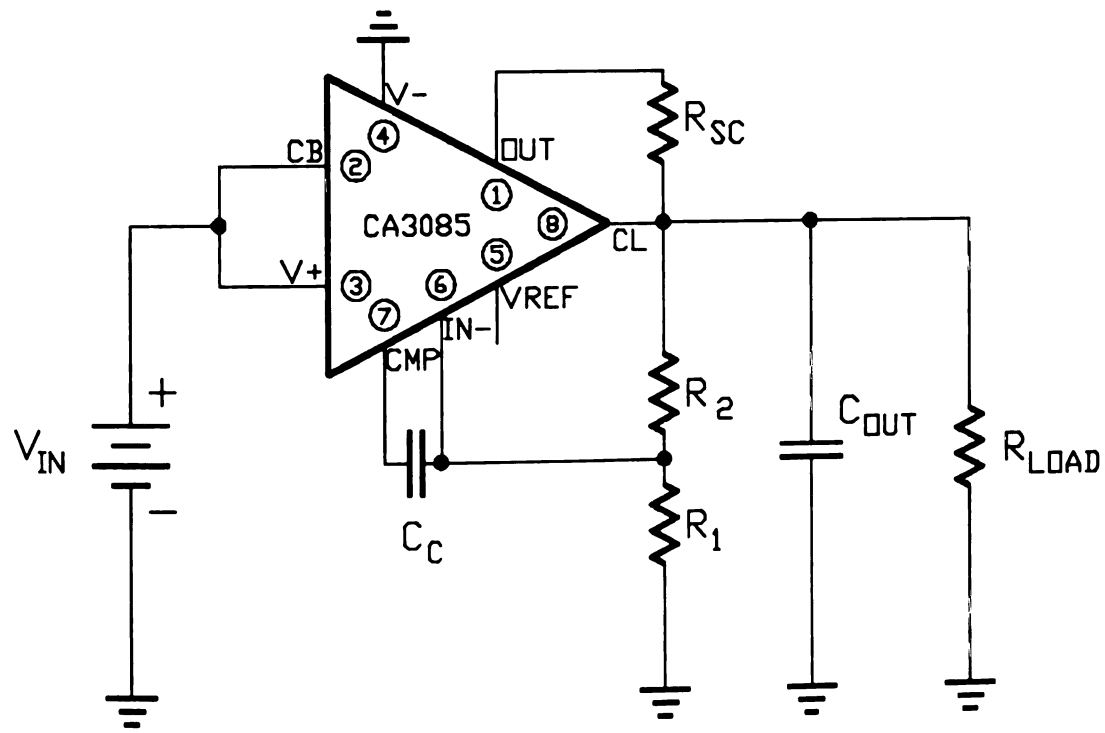

Figure 5.3 Basic application circuit for the CA3085

The basic application circuit for the CA3085 is shown in Fig. (5.3). Under normal operating conditions, $V(6) \approx V_{REF}$, V_{REF} being the internal voltage reference. This gives the output voltage as

$$V_{OUT} = V_{REF}\left(1 + \frac{R_2}{R_1}\right). \tag{5.1}$$

5.2.1 The Voltage Reference Amplifier Source

The voltage reference amplifier source consists of D_1, D_{ZR}, D_{ZB}, D_2, R_{R1}, R_{R2}, R_{R3}, R_Q, L_R, and E_R. The diodes, resistors and inductors provide both ac and dc characteristics. E_R is used to deliver the voltage generated by the reference to the rest of the circuit, acting as a buffer between the circuit and the reference generator.

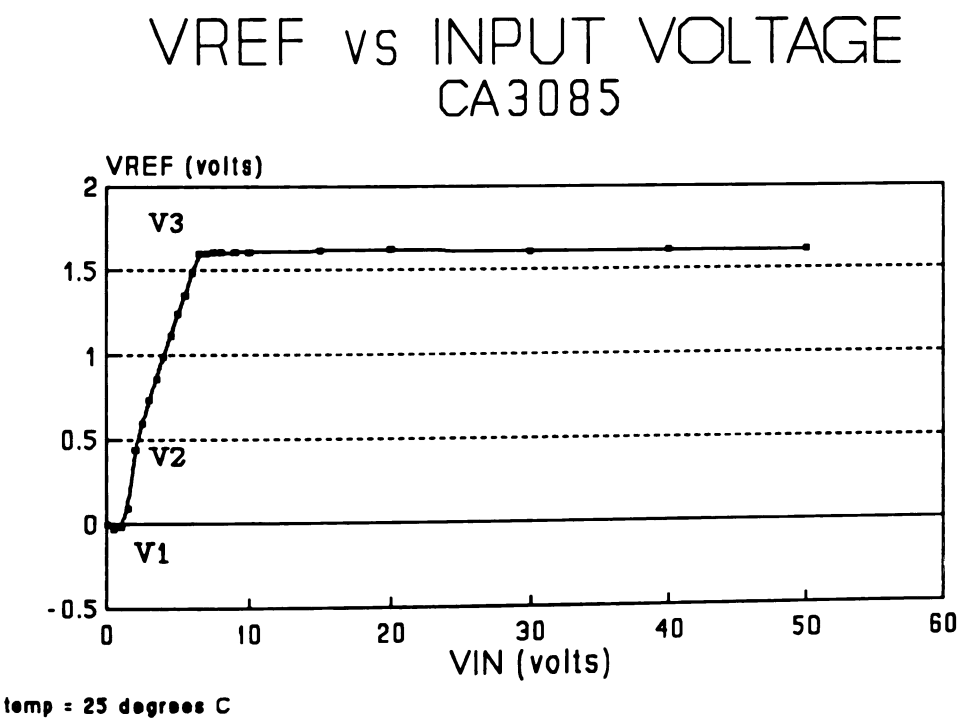

Figure 5.4 DC characteristics of the reference voltage, measured

Fig. (5.4) gives the dc characteristics of the voltage reference, and Fig. (5.5) gives the ac characteristics of the voltage reference. In Fig. (5.4), note the labeling of $V_{1\text{-}3}$. The slope of the curve between V_1 and V_2 will be called $(\Delta V_{REF}/\Delta V_{IN})_1$, the slope of the curve between V_2 and V_3 will be called $(\Delta V_{REF}/\Delta V_{IN})_2$, and the slope of the curve

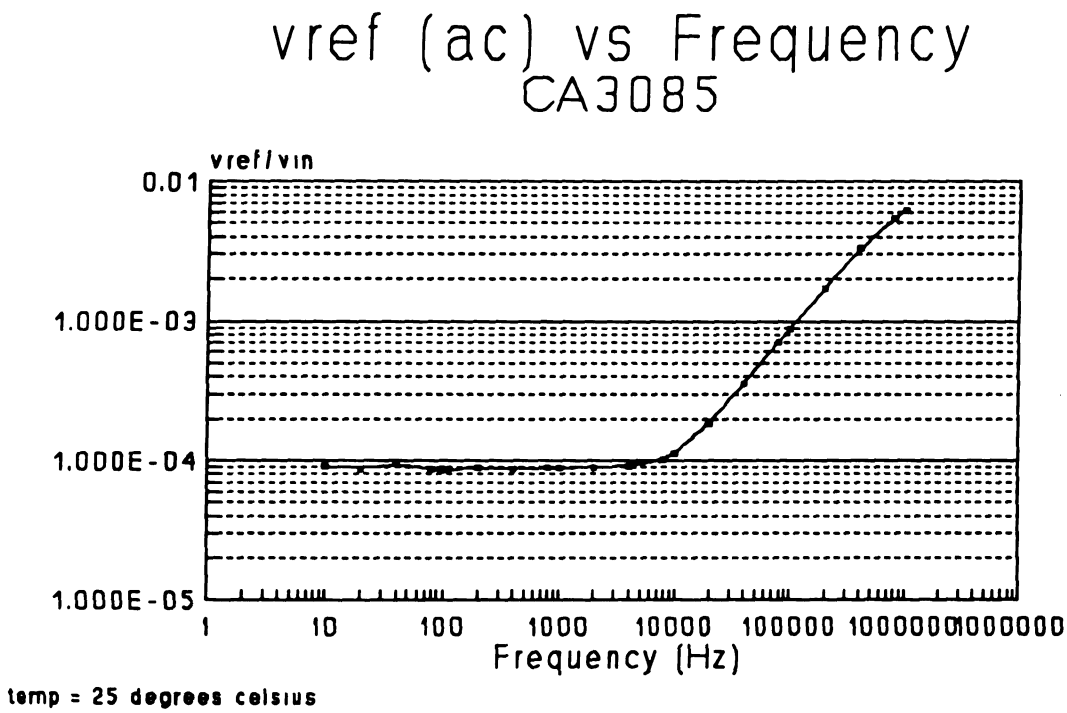

Figure 5.5 AC characteristics of the voltage reference, measured

to the right of V_3 will be called $(\Delta V_{REF}/\Delta V_{IN})$.

The dc operation of the circuit works in the following manner.

For $0 \leq V_{IN} \leq V_1$: using Fig. (5.4) as a reference, the drop across the circuit is not large enough to turn on D_1 and overcome the breakdown voltage of D_{ZB}. Thus, no current flows in the reference circuit and $V_{REF} = 0$.

For $V_1 \leq V_{IN} \leq V_2$: At $V_{IN} = V_1$, the diodes D_1 and D_{ZB} begin to conduct and current begins to flow through the reference circuit, resulting in the reference beginning to turn on. The diodes D_2 and D_{ZR} still remain off. Thus

$$V_1 = V_{D1} + BV_{DZB} \tag{5.2}$$

Once the voltage drop across the reference is great enough to allow D_1 and D_{ZB} to conduct, the slope $(\Delta V_{REF}/\Delta V_{IN})_1$ results from the resistive voltage divider

combination of R_Q and R_{R2}. Thus,

$$\left(\frac{\Delta V_{REF}}{\Delta V_{IN}}\right)_1 = \frac{R_{R2}}{R_Q + R_{R2}}. \tag{5.3}$$

For $V_2 \leq V_{IN} \leq V_3$: The voltage V_2 is approximately a diode drop greater than V_1, which suggests another diode turning on. This is modeled at the voltage in which D_2 turns on. The slope $(\Delta V_{REF}/V_{IN})_2$ is determined by the parallel combination of R_{R2} and R_{R3} in series with R_Q, and

$$\left(\frac{\Delta V_{REF}}{\Delta V_{IN}}\right)_2 = \frac{R_{R2} | R_{R3}}{R_{R2} | R_{R3} + R_Q}. \tag{5.4}$$

For $V_3 \leq V_{IN}$: At V_3, the breakdown voltage of D_{ZR} is reached. The reference has now achieved its nominal value. This is approximately 1.6V. V_{REF} is now the voltage drop across D_{ZR} and the small resistor R_{R1}. The slope $(\Delta V_{REF}/\Delta V_{IN})$ is due to the small signal voltage divider produced by r_{D1}, r_{DZB}, R_Q, r_{DZR}, and R_{R1}. In practice, the series combination of r_{DZR} and R_{R3} is much smaller than R_{R2} and the series combination of r_{D2} and R_3, so the equivalent resistance produced by these series combinations being in parallel is simply the series combination of r_{DZR} and R_{R1}. The slope $(\Delta V_{REF}/\Delta V_{IN})$ can then be described by

$$\left(\frac{\Delta V_{REF}}{\Delta V_{IN}}\right) = \frac{r_{DZR} + R_{R1}}{r_{DZR} + R_{R1} + R_Q + r_{DZB} + r_{D1}}. \tag{5.5}$$

The slope $(\Delta V_{REF}/V_{IN})$ represents the change in reference voltage which occurs with input voltage after the reference has achieved its nominal value. This has an effect on the output voltage which can be deduced by observing Eqn. (5.1). These changes in reference voltage with input voltage contribute to low frequency ripple rejection and

line regulation, as with the SG78XX and the SG7915.

As seen in Fig. (5.5), the voltage reference has ac characteristics which are inductive. These characteristics are introduced in the model by the inductor L_R. This adds a zero to the reference voltage, which adds a zero to the output voltage frequency response, and in turn gives the ripple rejection a pole.

Finally, E_R is added to provide a buffer between the voltage reference and the rest of the circuit so that any chance of the rest of the circuit effecting the voltage reference characteristics are minimized.

5.2.2 The Frequency Compensated Error Amplifier

The frequency compensated error amplifier is modeled by E_D, R_{IN}, D_L, D_+, D_-, E_+, V_+, V_-, and R_O. E_D is a voltage controlled voltage source which has as its controlling voltage the voltage across R_{IN}. This amplifies the voltage difference between V_{REF} and the Inverting Input terminal. In the actual chip, this is just a differential pair. The voltage controlled voltage source provides an adequate model for the amplifying action seen by the differential pair.

Although the functional block diagram states that this is a frequency compensated error amplifier, there is no indication that the amplifier is actually compensated in the chip. Compensation for the amplifier is normally provided for by an external capacitor. In Fig (5.3), this capacitor is C_C.

D_+, D_-, E_+, V_+, V_-, and R_O provide maximum and minimum clamping for the amplifier. The controlled source, E_+, has as its controlling voltage the voltage across nodes 3 and 0, with a gain of 1. This means the voltage across E_+ is simply V_{IN}. The voltage at the terminal of the resistor R_O which is not connected to V_D has a maximum and minimum value, with the clamping circuitry added. The maximum value is

$$V_{MAX} = V_{D+} + V_{+} + V_{IN} \tag{5.6}$$

The minimum value is

$$V_{MIN} = V_{-} - V_{D-}. \tag{5.7}$$

5.2.3 Series Pass Amplifier

The series pass amplifier consists of Q_{P1}, Q_{P2}, R_5 and R_B. This is identical to what is found in the real chip, with the exception of the addition of R_B which provides some base resistance for Q_{P2}.

5.2.4 Ripple Rejection Modeling

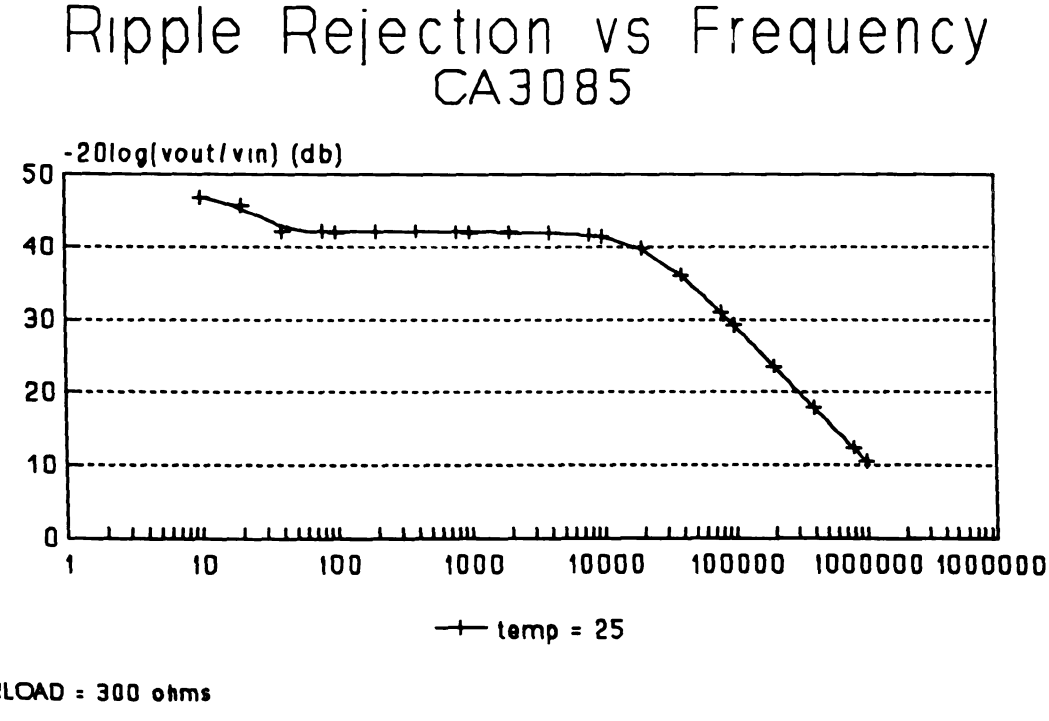

Figure 5.6 Ripple rejection vs frequency, measured

Fig. (5.6) gives the measured ripple rejection vs frequency response. This was measured as a one pole response.

The low frequency ripple rejection can be derived from Eqn. (5.1). From Eqn.

(5.1),

$$\Delta V_{OUT} = \Delta V_{REF}\left(1+\frac{R_2}{R_1}\right). \tag{5.8}$$

From Eqn. (5.5),

$$\Delta V_{REF} \approx \frac{R_{R1}}{R_{R1}+R_Q}\Delta V_{IN}, \tag{5.9}$$

neglecting r_{DZR}, r_{DZB}, and r_{D1}. Inserting this into Eqn. (5.8) gives

$$RR_{LF} = \left(\frac{\Delta V_{OUT}}{\Delta V_{IN}}\right)_{DC} = \frac{R_{R1}}{R_{R1}+R_Q}\left(1+\frac{R_2}{R_1}\right), \tag{5.10}$$

with some slight manipulation.

The pole of the ripple rejection response can also be derived from Eqn. (5.1). The pole of ripple rejection is the zero of V_{REF}. This is the zero formed by the inductor L_1 and R_{R1}, neglecting r_{DZR}, so

$$Pl_{RR} = \frac{R_{R1}}{L_R}. \tag{5.11}$$

5.2.5 Load Regulation

H_{LDR} and V_{LDR} are added to provide load regulation effects. H_{LDR} is a current controlled voltage source which has the current through V_{LDR} as its controlling current. In the application circuit in Fig. (5.3), note that the voltage reference is not connected to the external circuitry. Because the amplifier is configured in a feedback system, the effective voltage between the controlling nodes, the voltage across R_{IN}, of the high gain amplifier E_D, is nearly zero. This gives the voltage at the Inverting Input terminal a voltage almost equal to V_{REF}. The voltage at this terminal is used in the external circuitry as the 1.6V reference. H_{LDR} then provides the Inverting Input

terminal with a slight difference in voltage from that of V_{REF}. Since H_{LDR} depends on the current through V_{LDR}, which consists mainly of the load current, the voltage across H_{LDR} changes with load current. This means the voltage at the Inverting Input terminal changes, so V_{OUT}, in accordance with Eqn. (5.1), varies with load current. Changes in V_{OUT} with load current are just a load regulation characteristics. Note that

$$R_{OUT} = -\frac{\Delta V_{OUT}}{\Delta I_{OUT}}. \tag{5.12}$$

Using Eqn. (5.1), and the fact that variations in reference voltage with load current are given by

$$\Delta V_{REF} = -h_{LDR}\Delta I_{OUT}, \tag{5.13}$$

gives

$$R_{OUT} = h_{LDR}\left(1+\frac{R_2}{R_1}\right). \tag{5.14}$$

To include variations with temperature, the general PSpice description of the controlled source, HLDR, is

HLDR +n -n poly (2) V_{LDR} V_T 0 a_1 0 0 a_4 0 0 0 a_8

Since $I_{VLDR} \approx I_{OUT}$ and it is shown in section 5.2.10 that $I_{VT} = \Delta T$, where ΔT = TEMP - TNOM, the current through H_{LDR} is equal to

$$I_{HLDR} = I_{OUT}\left(a_1 + a_4\Delta T + a_8\Delta T^2\right), \tag{5.15}$$

which allows the controlled source quadratic temperature sensitivity. This allows for a new definition for h_{LDR}, and that is

$$h_{LDR} \triangleq (a_1 + a_4\Delta T + a_5\Delta T^2). \tag{5.16}$$

At room temperature,

$$R_{OUT} = a_{1,HLDR}\left(1 + \frac{R_1}{R_2}\right). \tag{5.17}$$

5.2.6. Quiescent Current Modeling

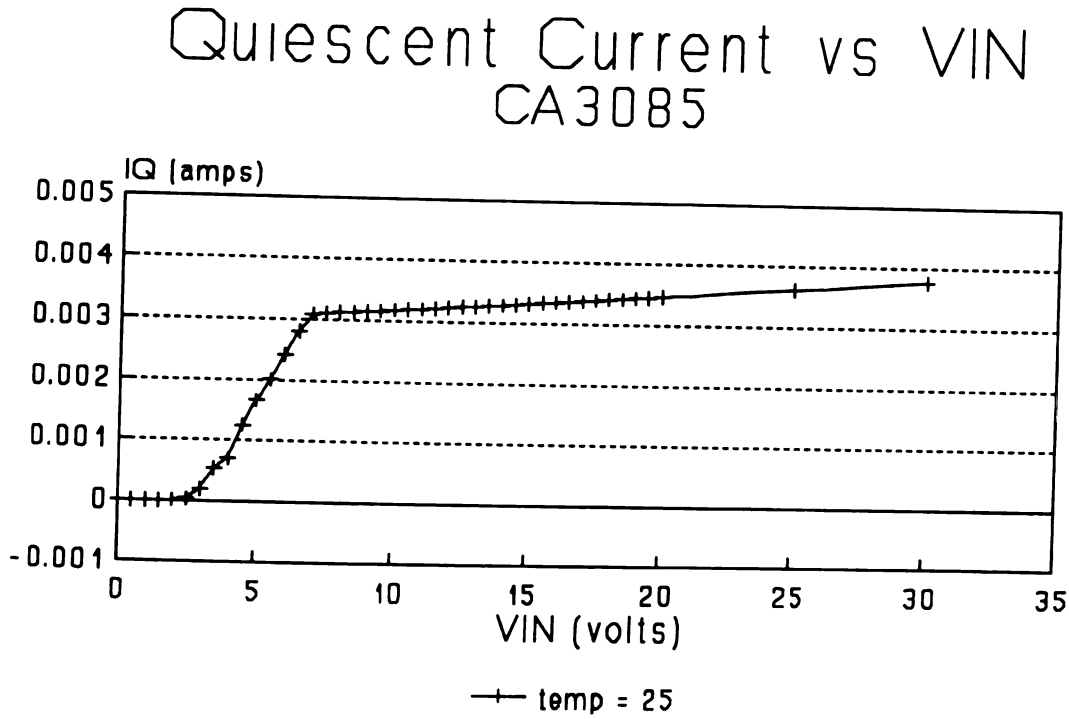

Figure 5.7 Quiescent current vs input voltage, measured

Fig. (5.7) shows the measured quiescent current vs input voltage characteristics. The quiescent current characteristics are modeled by G_{B1}, G_{B2}, and R_Q.

G_{B1} and G_{B2} are voltage controlled current sources which have the voltage across R_{R3} as their controlling voltage. The voltage controlled current source G_{B1} is slightly different from G_{B2}. It is defined generically in the macromodel as

G_{B1} n+ n- poly(2) V(12,4) V(10000) 0 a_1 0 0 a_4 0 0 0 a_8.

The voltage V(12,4) is the voltage across R_{R3}, still one of the controlling voltages, but another voltage, V(10000), is introduced as one of the controlling voltages. V(10000) has a voltage which is equal to ΔT. Again, this will be explain in more detail in section 5.2.10. From the PSpice definition for a two variable polynomial, the current produced by G_{B1} is

$$I_{GB1} = a_1 V(12,4) + a_4 V(12,4)\Delta T + a_8 V(12,4)\Delta T^2. \quad (5.18)$$

or

$$I_{GB1} = V(12,4)\left(a_1 + a_4\Delta T + a_8\Delta T^2\right). \quad (5.19)$$

A new definition can be introduced for g_{B1}, and that is

$$g_{B1} \triangleq a_1 + a_4\Delta T + a_8\Delta T^2. \quad (5.20)$$

This allows G_{B1} to show quadratic temperature effects, as the passive devices do, and allows it to remain off if V_{REF} is zero. G_{B1} is the main contributor to quiescent current, and provides much of the changes in quiescent current with temperature. For the room temperature model, ΔT = 0, and

$$I_{GB1} = a_1 V(12,4). \quad (5.21)$$

After the reference voltage has achieved its nominal value, the current through G_{B1} and G_{B2} no longer changes.

Note that the voltage across R_{R3} was selected as a controlling voltage because it best fit the characteristics in Fig. (5.7) to the second break point, or discontinuity in the plot. From 0V to this second break point, at approximately V_{IN} = 8.5V, the

contribution to quiescent current is primarily G_{B1} and G_{B2}. This point will be labeled V_{Q1} and I_{Q1}. At this point, the reference voltage has achieved its nominal value, and so R_{R3} has achieved its maximum value, so the currents through G_{B1} and G_{B2} are constant. However, at this point

$$(g_{B1}+g_{B2})(BV_{DZB}-V_{D2})+\frac{(V_{Q1}-BV_{DZB}-V_{D1}-BV_{DZR})}{R_Q}=I_{Q1}. \tag{5.22}$$

After this point, the changes in quiescent current with input voltage come from R_Q. Since the voltage V_{REF} and the voltage drops across D_1 and D_{ZB} are constant, any change in the input voltage across the reference voltage structure is dropped across R_Q. This contributes to a change in current through R_Q, and hence a change in quiescent current in accordance with,

$$\Delta IQ = \frac{\Delta V_{IN}}{R_Q}, \tag{5.23}$$

and

$$R_Q = \frac{\Delta V_{IN}}{\Delta IQ}. \tag{5.24}$$

5.2.7 Short Circuit Current Limiting

The short circuit current circuitry is D_L, Q_L, R_{B15} and E_L. The short circuit current circuitry work in the following way.

For short circuit current limiting the CA3085 requires an external resistor, R_{SC} in Fig. (5.3), to be attached the OUT and CL pins. All of the load current and current which biases R_1 and R_2, pass though R_{SC}.

E_L has the following PSpice definition,

E_L n+ n- POLY(1) V(10000) a_1 a_2,

From the Pspice definition of a one variable polynomial and using the fact that V(10000) = ΔT, the voltage across E_L can be described by the relationship

$$V_{EL} = a_1 \Delta T + a_2 (\Delta T)^2. \tag{5.25}$$

This gives the voltage source a quadratic variation with temperature, with a value of 0 and the nominal temperature (room temperature, usually). E_L does not come into the design procedure until the section on temperature modeling, so more information will be given in another section.

D_L prevents the controlled source E_D from supplying any current to the base of Q_{P2}. This means that G_{B2} supplies all of the drive current to Q_{P2}, which in turn supplies the drive current to Q_{P1}, which supplies the load current. If Q_{P2} shuts off, Q_{P1} shuts off and no load current can be supplied. As current flows out of the emitter of Q_{P1} through R_{CL} and to the load, a voltage is generated across the base emitter junction of Q_L. If this voltage is large enough to turn Q_L on, most of the current supplied by G_{B2} is drawn by the collector of Q_L, since its needs are large compared to the current needed by the base of Q_{P2} and the maximum available current from G_{B2}. Q_{P2} begins to shut off. A very small amount of current can be suppied to the base of Q_{P2} in order to supply the current to produce the voltage across R_{CL}. If the voltage across R_{CL} is not large enough, Q_L remains off and draws no current. The maximum output current is the current necessary to turn on Q_L. This gives

$$I_{MAX} = \frac{V_{BE,ON,QL}}{R_{SC}}. \tag{5.26}$$

Under the short circuit mode, because the base of Q_{P2} draws a small amount

of current, the collector of Q_L draws most of the current available from G_{B2}. This means that in Eqn. (5.26), $V_{BE,ON,QL}$ can be estimated since the collector current of Q_L can be estimated as approximately the total current supplied from G_{B2}, which is $g_{Q2}(V_{REF} - V_{D2})$. Using an approximation for the relationship between collector current and base emitter voltage and inserting into Eqn. (5.26) gives

$$I_{MAX}R_{SC} \approx V_{BEQL} \approx NF\,V_T \ln\left(\frac{g_{B2}(V_{REF} - V_{D2})}{IS_{QL}}\right). \tag{5.27}$$

When using Eqn. (5.27), note that I_{MAX} is the sum of the maximum available current supplied to the load, plus the current required to bias R_1 and R_2 under the maximum output current condition. Then, since $I_{R1} = I_{R2}$,

$$I_{MAX} = I_{R1@MAX.COND.} + I_{MAX,LOAD}. \tag{5.28}$$

5.2.8 Dropout Characteristics

For the macromodel, dropout voltage is a function of IS, NF, BF, and VAF for the transistors Q_{P1} and Q_{P2}.

No closed form solution, or even an approximation exists for the determination of the relationship between these parameters and the dropout voltage. An empirical method was used with good results. Given that NF, VAF, and BF are set for Q_{P1} and Q_{P2}, vary IS for the transistors until the correct dropout voltage is attained. The method was done for $R_{LOAD} = 300\Omega$, and trends were matched nicely for different loads and different temperatures.

5.2.9 Power Up and Down, Square Wave and Triangle Wave

The measured power up and down with square wave is shown is Fig. (5.8). This is primarily a function of an external output capacitor charging up to its needed

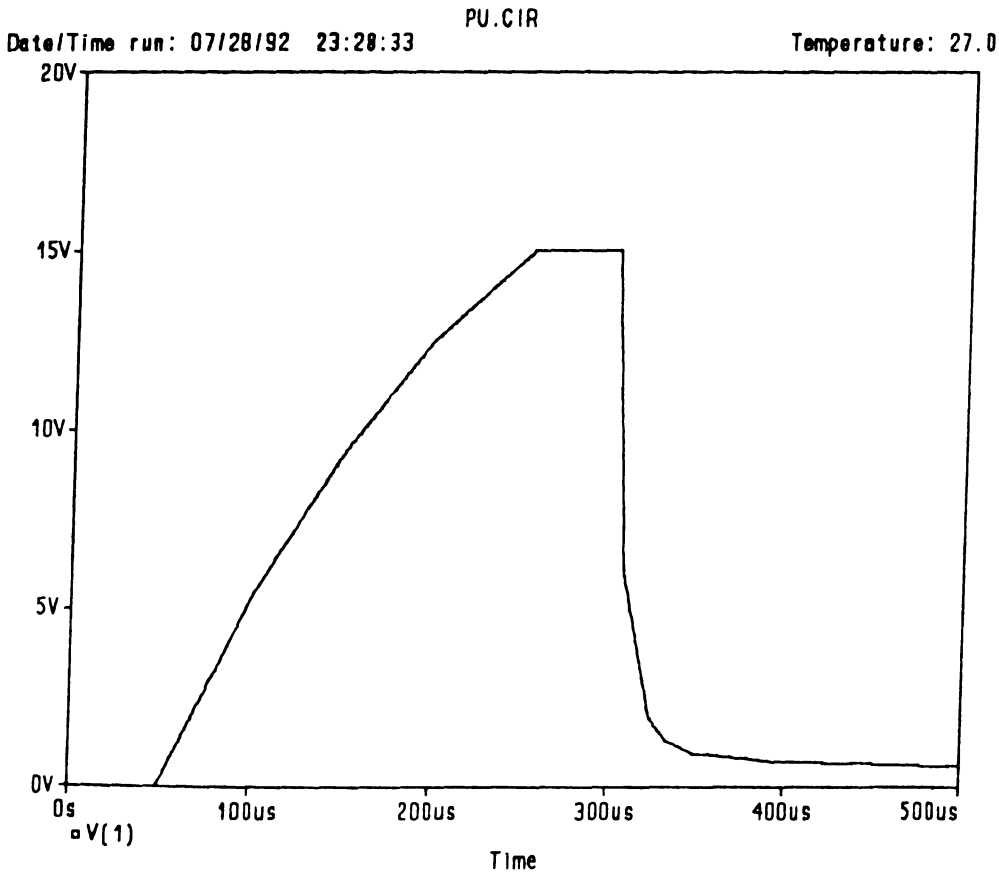

Figure 5.8 Power up and down, square wave, measured

voltage. Although the output capacitor was not needed for stability for this regulator, it was used solely on the power up and down with square wave to provide modeling insight. This charging is limited since the capacitor has a finite amount of current available due to the limited amount of current available from the regulator, since R_{SC} limits the output current.

D_{DIS} is added to the model for capacitive discharge which can be noted in Fig. (5.8), upon powering down.

The measured power up and down with triangle wave is shown in Fig. (5.9). The controllable response is the slight delay seen at the base of the triangle wave output. This is due to the fact that C_C in Fig. (5.3) must charge up, but has a limited amount of current available to it which results in slewing. The maximum current it has available is approximately I_{GB2}. The parameter g_{B2} is set empirically based on this response.

5.2.10 Ambient Temperature Sensing Circuitry

I_T, R_{T1}, R_{T2} are used to generate a voltage at node 10000 which is equal to the change in ambient temperature from the nominal temperature , ΔT. The description of the circuitry is

```
IT     0 10000 dc 1
RT1    10000 10001 100.00001 TC=0.01
RT2    10001 0 -100.00001
```

This means that the total resistance seen by I_T is $R_{T1} + R_{T2}$, or

$$R = 100.00001(1 + (T - TNOM).01) + 100. \qquad (5.29)$$

Simplifying (5.29) and setting T - TNOM = ΔT gives

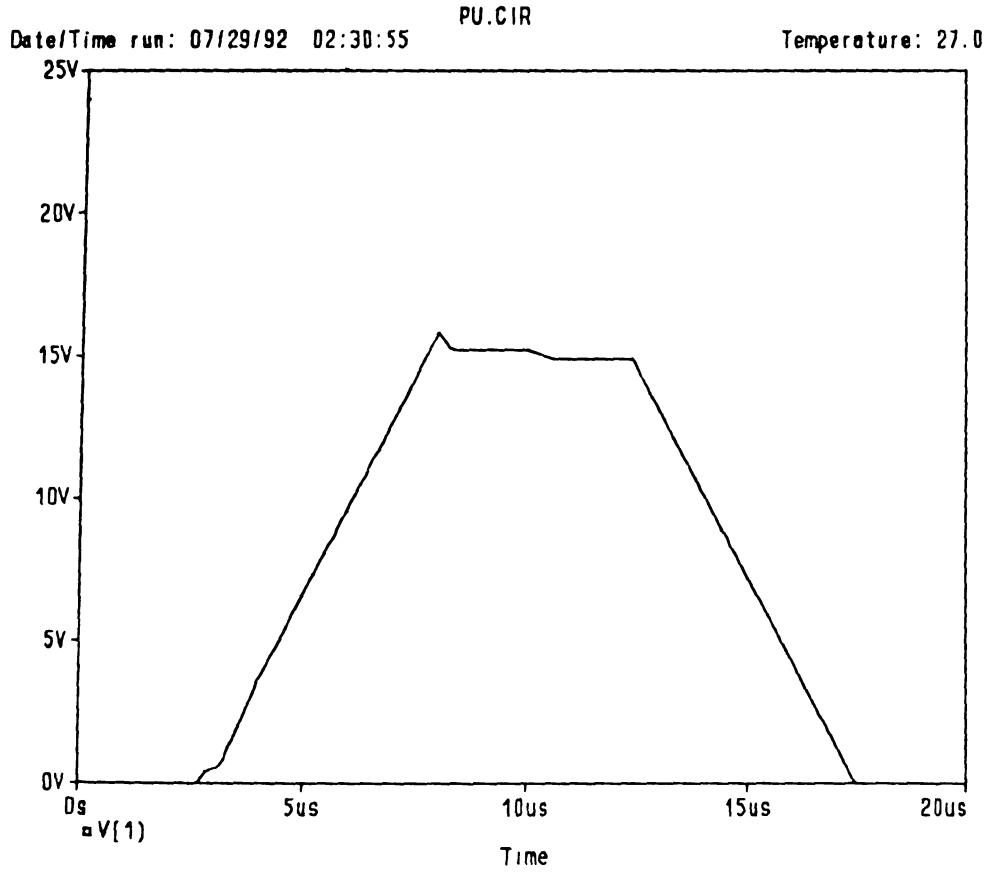

Figure 5.9 Power up and down, triangle wave, measured

$$R = \Delta T. \tag{5.30}$$

Since I_T has a dc value of 1A, the voltage at node 10000 is equal to ΔT. Controlled sources can now use this voltage as one of the controlling voltages which not only provide temperature dependent controlled sources, but provide conceptually easy to understand temperature dependent controlled sources.

It is of interest to know why the values of the resistors were set to 100Ω and -100Ω instead of 1Ω and -1Ω and TC to 0.01 instead of 1, which provides the same result as (5.30), but in a much more straight forward manner. The description of the resistor with TC1 specified is

$$R = R_{NOM}(1 + TC1\,\Delta T). \tag{5.31}$$

Although Pspice allows for R and R_{NOM} to become negative, it does not allow for the quantity in brackets to become negative. This is a subtle point which must be taken into consideration when temperature work is being done.

The circuitry above generates a voltage which is equal to ΔT. It is desirable, with current controlled dependent sources for instance, to have a current which is equal to ΔT as well. This is provided for by G_T, V_T and R_{T3}. G_T is a voltage controlled current source with a gain of one which has as its dependent voltage the voltage at node 10000, which has a value of ΔT. This current then flows through V_T and R_{T3}, and V_T acts as the sensing device for temperature dependent controlled sources.

5.2.11 Other Modeled Characteristics

The prior characteristics shown are used to determine the values of the components and parameters. Other characteristics are modeled as well, because of a correct choice of parameters, and these are: line transient response, load transient

response and line regulation.

5.3 DESIGN PROCEDURE FOR A CA3085

Based on the equations and procedures shown in the last section, a design procedure will be developed in this section.

Fundamental to the design procedure is a list of measurements required to base the design on. The following measurements should be taken in the basic regulator circuit:

1) Measure V_{REF} vs V_{IN}.

2) Measure IQ vs V_{IN}.

3) Measure V_{OUT} for V_{IN} = 25V, with no load.

4) Measure ripple rejection vs frequency with R_{LOAD} = 300Ω.

5) Measure R_{OUT}, with R_{LOAD} = 300Ω.

6) Select R_{SC} = 5.2Ω. Measure maximum output current at V_{IN} = 25V.

7) Measure dropout voltage with R_{LOAD} = 300Ω.

8) Take a power up and down with square wave and triangle wave input with R_{LOAD} = 300Ω.

9) Measure R_{LOAD}, the external resistors R_1, R_2, R_{SC}, C_{OUT}, and the compensation capacitor C_C. These measured values get used in all of the equations. Measure as well the capacitances of all capacitors and the series resistance of all capacitors at some representative frequency.

The component selection procedure is:

1) Select E_D and E_R.

2) Select the amplifier clamping circuitry, these are the values and

parameters for:

V_+, V_-, E_+, R_O, and the diode parameters for D_+ and D_-.

3) Select the parameters for the diodes D_1 and D_2.

4) Based on the V_{REF} vs V_{IN} measurement, determine the input voltage required to begin to turn the reference on, V_{ON}, then, from Eqn. (5.2),

$$BV_{DZB} = V_{ON} - V_{D1}. \tag{5.32}$$

Select NBV_{DZB}.

5) From the measured value of V_{OUT} at V_{IN} = 25V, and utilizing Eqn. (5.1),

$$BV_{DZR} = V_{REF} \approx \frac{V_{OUT}}{\left(1 + \frac{R_2}{R_1}\right)}. \tag{5.33}$$

Select NBV_{DZR}.

6) Measure the slope of IQ vs V_{IN} for the quiescent current measurement. Then from Eqn. (5.24),

$$R_Q = \frac{\Delta V_{IN}}{\Delta I_Q}. \tag{5.34}$$

7) From the measured V_{REF} vs V_{IN} plots, and Eqn. (5.3),

$$R_{R2} = \left(\frac{1}{\left(\frac{\Delta V_{REF}}{\Delta V_{IN}} \right)_1} - 1 \right) R_Q \tag{5.35}$$

8) From the measured V_{REF} vs V_{IN} plots, and Eqn. (5.4),

$$R_{B3} = \left(\frac{1}{\left(\frac{\Delta V_{REF}}{\Delta V_{IN}} \right)_2} - 1 \right)^{-1} \frac{R_Q}{} - \frac{1}{R_{B2}} \qquad (5.36)$$

9) From the ripple rejection measurement, determine RR_{LF}. Then from Eqn. (5.10),

$$R_{B1} = \left(\frac{1 + \frac{R_2}{R_1}}{RR_{LF}} - 1 \right)^{-1} R_Q \qquad (5.37)$$

10) From the ripple rejection measurement, determine $P1_{RR}$, then from Eqn. (5.11),

$$L_R = \frac{R_{B1}}{P1_{RR}}. \qquad (5.38)$$

11) From the power up and down triangle wave measurement, empirically determine g_{B2}.

12) From the quiescent current vs input voltage measurement, determine the value of the quiescent current at the point where a steady value is achieved call this V_{Q1} and I_{Q1}. The total quiescent current is the sum of the currents from G_{B1}, G_{B2}, and R_Q. Using this fact and Eqn. (5.22),

$$g_{B1} = \frac{I_{Q1} - \frac{(V_{Q1} - BV_{DZB} - V_{D1} - V_{REF})}{R_Q}}{BV_{DZR} - V_{D2}} - g_{B2}. \qquad (5.39)$$

13) Select R_{B15}.

14) Select R_B.

15) Select the parameters BF, VAF, and NF for Q_{P2} and Q_{P1}. Let the

transistors be identical.

16) Based on the dropout voltage measurement, empirically determine IS for the transistors.

17) Select IS and BF for Q_L. From the short circuit current measurement, find I_{MAX}. Then, from Eqn. (5.27) and Eqn. (5.28),

$$NF_{QL} = \frac{I_{MAX}R_{SC}}{VT\ln\left(\frac{\beta_{R2}(V_{REF}-V_{D2})}{IS_{QL}}\right)}. \tag{5.40}$$

18) Determine R_{OUT} from the Load Regulation measurement or Load Transient Response, from Eqn. (5.14),

$$h_{LDR} = \frac{R_{OUT}}{\left(1+\frac{R_1}{R_2}\right)}. \tag{5.41}$$

19) Select the parameters for the diode D_{DIS}.

This concludes the design procedure. All of the parameters for the macromodel have been selected.

5.4 DESIGN PROCEDURE EXAMPLE

In this section, a design example will be given. The following components were measured and used for the modeling: R_1 = 100.1Ω, R_2 = 818.98Ω, C_C measured 113.01pF and negligible series resistance at 100kHz, C_{OUT} measured .9602uF and had a series resistance of 1.034Ω at 100kHz, R_{SC} = 5.602Ω, and R_{LOAD} = 300.617Ω. For the room temperature modeling, set $V_{D1} = V_{D2} = 0.6V$.

1) Set E_D = 10000 and E_R = 1.

2) Set V_+ = -1V, V_- = 1V. Set the gain of E_+ = 1. Let the diodes be the Pspice default diodes. Set R_O = 5Ω. This means that the maximum amplifier voltage is about (V_{IN} - .4)V and the minimum amplifier voltage is .4V, if the diode drops are taken to be 0.6V.

3) Let the diodes D_1 and D_2 be the Pspice default diodes.

4) V_{ON} = 2.5V then BV_{DZB} = 1.9V. Set NBV_{DZB} = 0.01.

5) V_{OUT} = 15.03V then BV_{DZR} = 1.637V. Set NBV_{DZR} = 0.01.

6) From the measured slope of IQ vs V_{IN} for the quiescent current measurement, R_Q = 34034.65Ω.

7) From the measured V_{REF} vs V_{IN} plots, R_{R2} = 43316.83Ω

8) From the measured V_{REF} vs V_{IN} plots, R_{R3} = 15853.64Ω

9) From the ripple rejection measurement, determine RR_{LF} = 42.08db = 0.0079, then R_{R1} = 29.3092Ω.

10) From the ripple rejection measurement, $P1_{RR}$ = 23kHz, then L_R = .2028mH.

11) From the power up and down triangle wave measurement, g_{B2} was set to 2m.

12) From the quiescent current vs input voltage measurement, V_{Q1} = 7.5V and I_{Q1} = 3.106mA, then g_{B1} = .8999m.

13) Set R_{B15} = 1.5kΩ.

14) Set R_B = 10Ω.

15) Set BF, VAF, and NF for Q_{P2} and Q_{P1} to be 50, 150V, and 1.25.

16) Based on the dropout voltage measurement, IS for Q_{P1} and Q_{P2} was set to 1e-16A.

17) Set IS = 1e-14A and BF = 100 for Q_L. $I_{MAX,LOAD}$ = 115mA and I_{MAX} = 128.5mA, then NF_{QL} = 1.0667.

18) From the load transient response measurement R_{OUT} = -0.4Ω, then h_{LDR} = -0.0436.

19) Let the diode D_{DIS} be the Pspice default diode.

This concludes the design of the room temperature macromodel. The parameters for the room temperature macromodel have been selected.

5.5 MODELING THE CA3085 AT -55 AND 125 DEGREES

5.5.1 Strategy in Modeling the CA3085 Temperature Variations

From the room temperature model, steps which need modifications are steps 4, 5, 6, 9, 10, 12, 17, and 18. These will give rise to new values for BV_{DZB}, BV_{DZR}, R_Q, R_{R1}, and L_R. R_{R2} and R_{R3} will not be varied with temperature. This will also be used to find the coefficients of the polynomials which describe h_{LDR}, E_L, and g_{B1}.

Since the controlled sources have the same format as the Pspice defined temperature coefficients, they are solved in a similar way.

The strategy for the temperature dependent sources G_{B1}, and H_{LDR} is to first solve for the first coefficient a_1, which is g_{B1}(TNOM), since $\Delta T = 0$. Then let $g_{B1}(T) = (a_1 + a_4\Delta T + a_8\Delta T^2)$, as in Eqn. (5.20). Writing out $g_{B1}(T)$ at -55°C and 125°C gives two equations and 2 unknowns since a_1 will be known from the room temperature design. This solution will yield a_4 and a_8.

The coefficients of H_{LDR} are handled identically to this.

E_L only depends on the temperature and $V_{EL}(T) = a_1\Delta T + a_2\Delta T^2$. At temperatures other than the nominal temperatures Eqn. (5.27) becomes

$$I_{MAX}R_{SC} \approx V_{BEQL} \approx V_{EL} + NF\,V_T \ln\left(\frac{g_{Q1}V_{REF}}{IS_{QL}}\right), \qquad (5.42)$$

which allow the maximum output current to vary with temperature. Solving for $V_{EL}(T)$ at -55°C and 125°C again yields two equations and two unknowns and this is easily solved for.

5.5.2 Design Example to Include Temperature Dependance

In this section the parameters for the model for -55°C and 125°C are developed. The temperature coefficients are determined and then inserted into the room temperature model. This will represent the fully developed, macromodel for the CA3085.

Following the example in Sec. (5.4) for -55 degrees:

Let $V_{D1} = V_{D2} = 0.45V$.

4) $V_{ON} = 3.5V$ then $BV_{DZB} = 3.05V$.

5) $V_{OUT} = 15.052V$ then $BV_{DZR} = 1.6394V$.

6) From the measured slope of IQ vs V_{IN} for the quiescent current measurement, $R_Q = 29858.85\Omega$.

9) From the ripple rejection measurement, determine $RR_{LF} = 47.63db = 0.00415$, then $R_{R1} = 13.516\Omega$.

10) From the ripple rejection measurement, $P1_{RR} = 12kHz$, then $L_R = .1793mH$.

12) From the quiescent current vs input voltage measurement, $V_{Q1} = 7.5V$ and $I_{Q1} = 2.942mA$, then $g_{B1} = .4014m$.

17) $I_{MAX,LOAD} = 136.3mA$ and $I_{MAX} = 150.07mA$, then $E_L = .0861$.

18) From the load transient response measurement $R_{OUT} = -3.7563\Omega$, then

h_{LDR} = -0.4091.

19) Let all of the diodes in the model have the parameters EG = 0eV and XTI = 0 set.

Following the example in Sec. (5.4) for 125 degrees:

Let $V_{D1} = V_{D2} = 0.75V$.

4) V_{ON} = 1.5V then BV_{DZB} = .75V.

5) V_{OUT} = 15.112V then BV_{DZR} = 1.6459V.

9) From the measured slope of IQ vs V_{IN} for the quiescent current measurement, R_Q = 40923.71Ω.

9) From the ripple rejection measurement, determine RR_{LF} = 52.81db = 0.002287, then R_{R1} = 10.1936Ω.

10) From the ripple rejection measurement, $P1_{RR}$ = 6kHz, then L_R = .2704mH.

12) From the quiescent current vs input voltage measurement, V_{Q1} = 7V and I_{Q1} = 2.738mA. Then g_{B1} = .9510m.

17) $I_{MAX,LOAD}$ = 82.717mA and I_{MAX} = 91.7263mA, then E_L = -.0165V.

18) From the load transient response measurement, R_{OUT} = .4834mΩ, then h_{LDR} = .5268.

A final summary of the temperature dependent parameters and elements follows in Table 5.1.

element or **parameter**	**value** at **25 degrees**	**value at -55 degrees**	**value** at **125 degrees**
BV_{DZB}	1.9	3.05	0.75
BV_{DZR}	1.637	1.6394	1.6459
R_Q	34.03465k	29.85885k	40.92371k
R_{R1}	29.3092	13.516	10.1936
L_R	.2028m	.1793m	.2704m
g_{B1}	.8999m	.4014m	.9510m
H_{LDR}	-0.0436	-.4091	.5268
E_L	0	.0861	-.0165

Table 5.1 Temperature dependent components and parameters

Solving for the linear and quadratic coefficients for these parameters results in Table 5.2.

element or **parameter**	**TC1** or **TBV1** (linear coeff.)	**TC2** or **TBV2** (quadratic coeff.)
BV_{DZB}	-6.8933e-3	8.4064e-6
BV_{DZR}	1.3982e-5	4.0386e-7
R_Q	1.7516e-3	2.7248e-06
R_{R1}	8.4331e-4	-7.3654e-05
L_R	2.2862e-3	1.0471e-05
g_{B1}	3.6889e-6	-3.1779e-08
h_{LDR}	2.734e-3	-2.293e-05
E_L	-6.7125e-3	5.0625e-6

Table 5.2 Temperature coefficients

The macromodel for the CA3085 follows:

```
.SUBCKT 3085  1   2   3   4   5   6   7   8
*             VOUT |   |   |   |   |   |   |
*                  CB |   |   |   |   |   |
*                    VIN |   |   |   |   |
*                        V-  |   |   |   |
*                        VREF|   |   |   |
*                            IN- |   |
*                             COMP|
*                                 CLIMIT
*
*
D1      3 9 DMOD
DZB     10 9 DZB
.MODEL DZB D (BV=1.9 TBV1=-6.8933E-3 TBV2=8.4064E-6 NBV=.01 EG=0 XTI=0)
RQ      10 11 34.034K TC=1.7516E-3,2.7249E-6
DZR     13 11  DZR
.MODEL DZR D (BV=1.6370 TBV1=1.3982E-5 TBV2=4.0386E-7 NBV=.01 EG=0
XTI=0)
LR      14 4 IND1 .2028M
.MODEL IND1 IND (TC1=2.2862E-3 TC2=1.0471E-5)
RR1     13 14 29.3092 TC=8.4331E-4,-7.3654E-5
D2      11 12 DMOD
.MODEL DMOD D (EG=0 XTI=0)
RR2     11 4 43.316K
RR3     12 4 15.853K
ER      5 4 11 4 1
RIN     5 15 1000000
HLDR    15 6 POLY (2) VLDR VT 0 -.0436 0 0 0.002734 0 0 0 -2.2930E-5
GB2     3 7 12 4 2M
DL      7 17 DL
.MODEL DL D (N=0.1 EG=0 XTI=0)
ED      18 4 5 15 10000
GB1     3 5 POLY (2) (12,4) (10000,0) 0 .8999M 0 0 3.6889E-6 0 0 0 -3.1779E-8
RT1     10000 10001 100.00001 tc=0.01
RT2     10001 0 -100
IT      0 10000 DC 1
GT      0 30000 10000 0 1
VT      30000 30001 DC 0
RT3     30001 0 1
RO      17 18 5
E+      16 4 9 4 1
D+      17 160 DMOD
V+      160 16 DC -1
DC-     40 17 DMOD
V-      40 4 DC 1
RB      7 20 10
QP2     3 20 21 QMOD1
QP1     2 21 22 QMOD1
```

```
VLDR    22 1 DC 0
.MODEL QMOD1 NPN (BF=50 VAF=150 IS=1E-16 NF=1.25)
R5      3 2 500
RB15    200 1 1.5K
QL      7 19 8 QLIMIT
EL      19 200 POLY (1) (10000,0) 0 -6.7125E-4 5.0625E-6
.MODEL QLIMIT NPN (IS=1E-14 BF=100 NF=1.0666)
DDIS    1 3 DDIS
.MODEL DDIS D (EG=0 XTI=0)
.ENDS 3085
```

5.5.3 Comparison of Macromodel Predictions with Lab Results

A comparison of macromodel predictions with lab results are presented in this section.

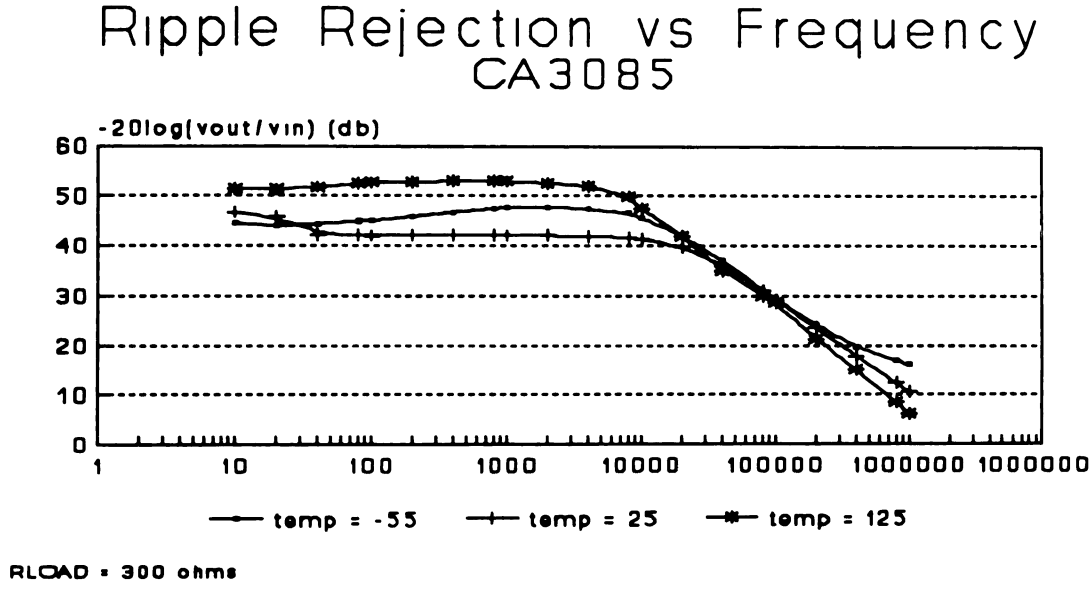

Figure 5.10 Ripple rejection vs frequency, measured

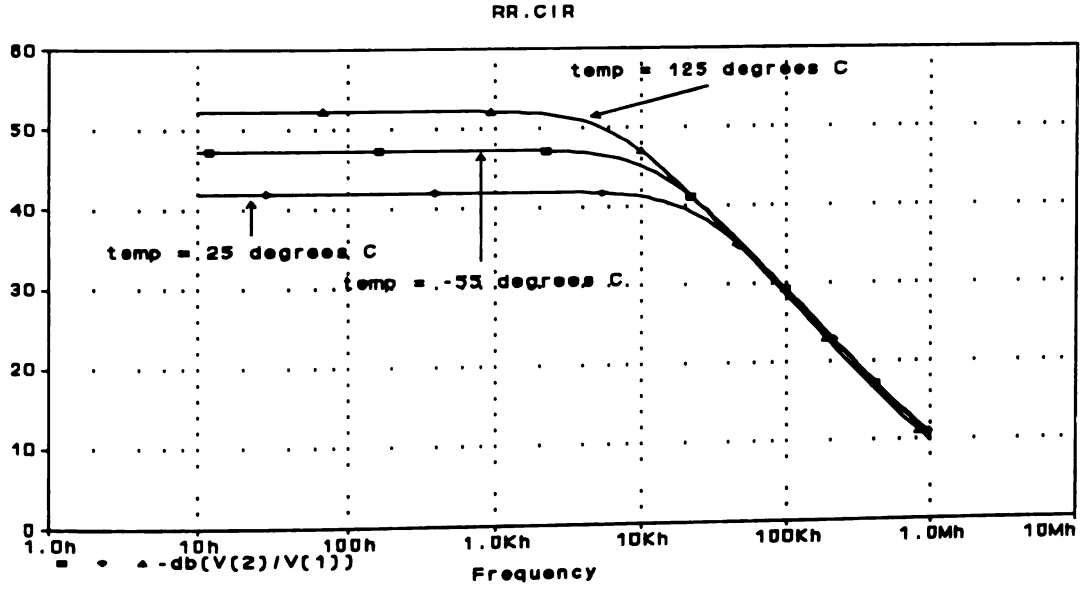

Figure 5.11 Ripple rejection vs frequency, macromodel

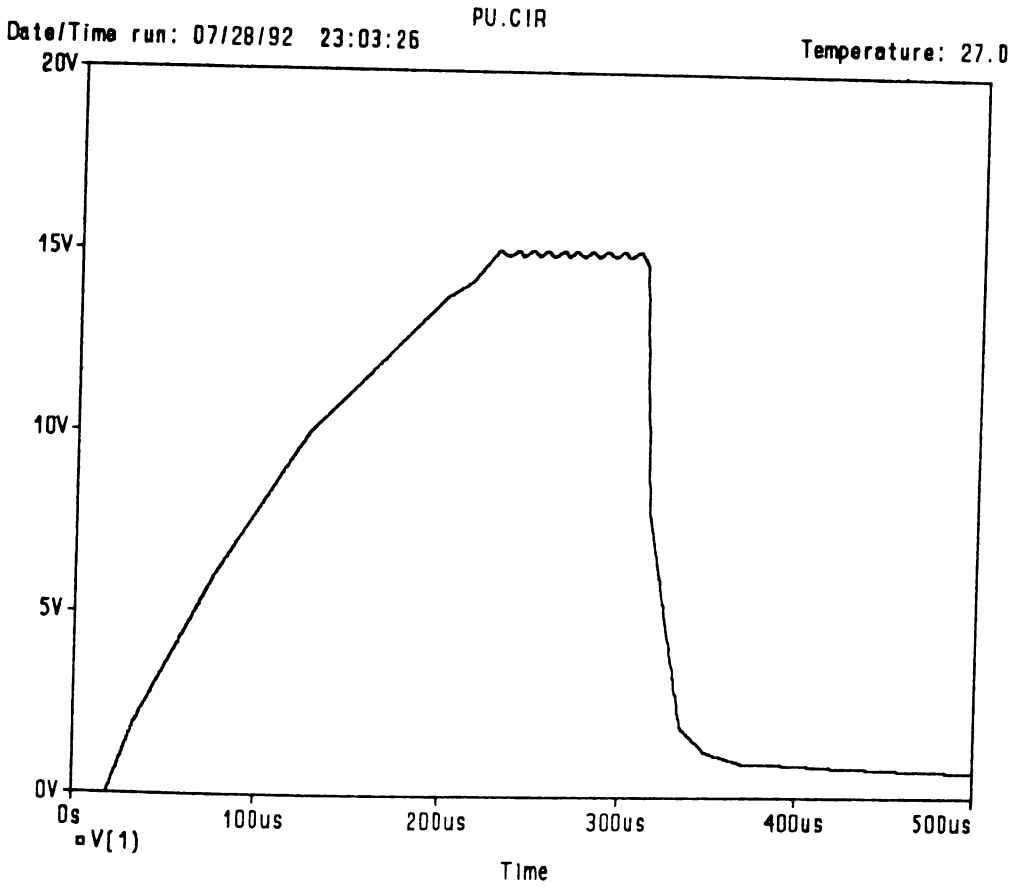

Figure 5.12 Power up and down, square wave, T = -55, measured

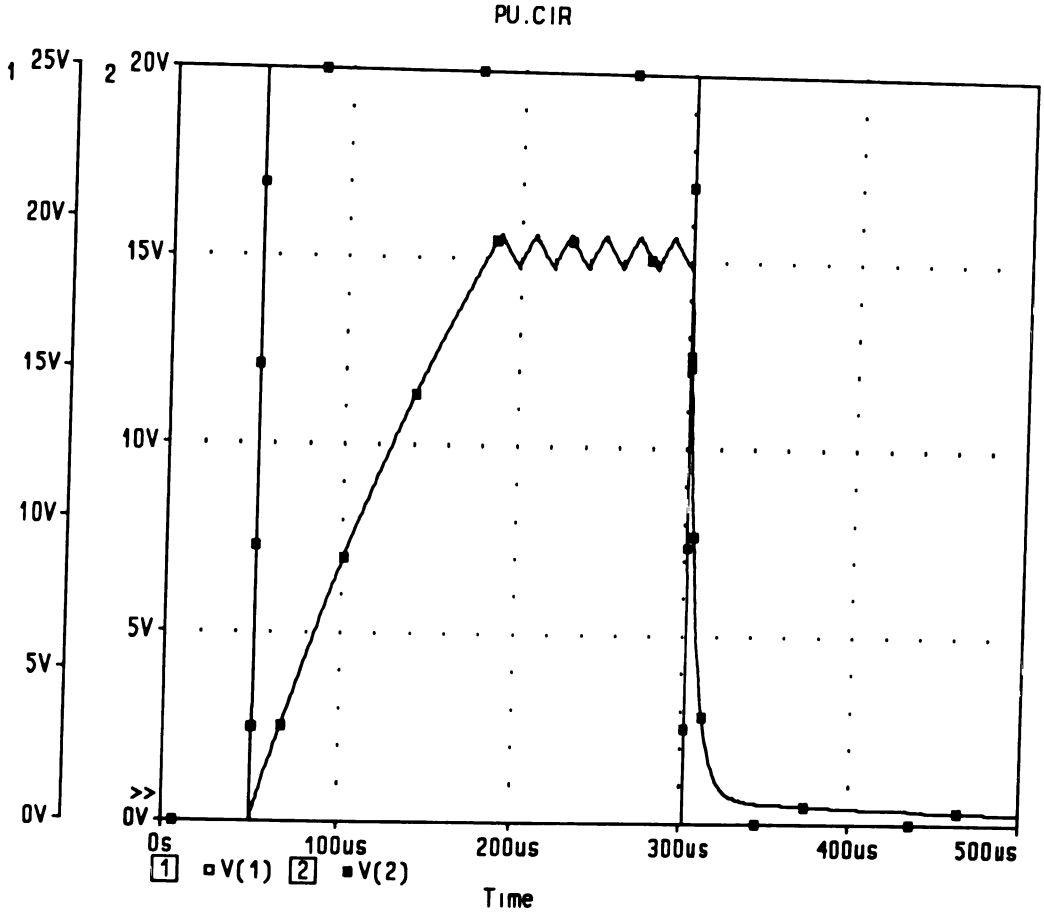

Figure 5.13 Power up and down, square wave, T = -55, macromodel

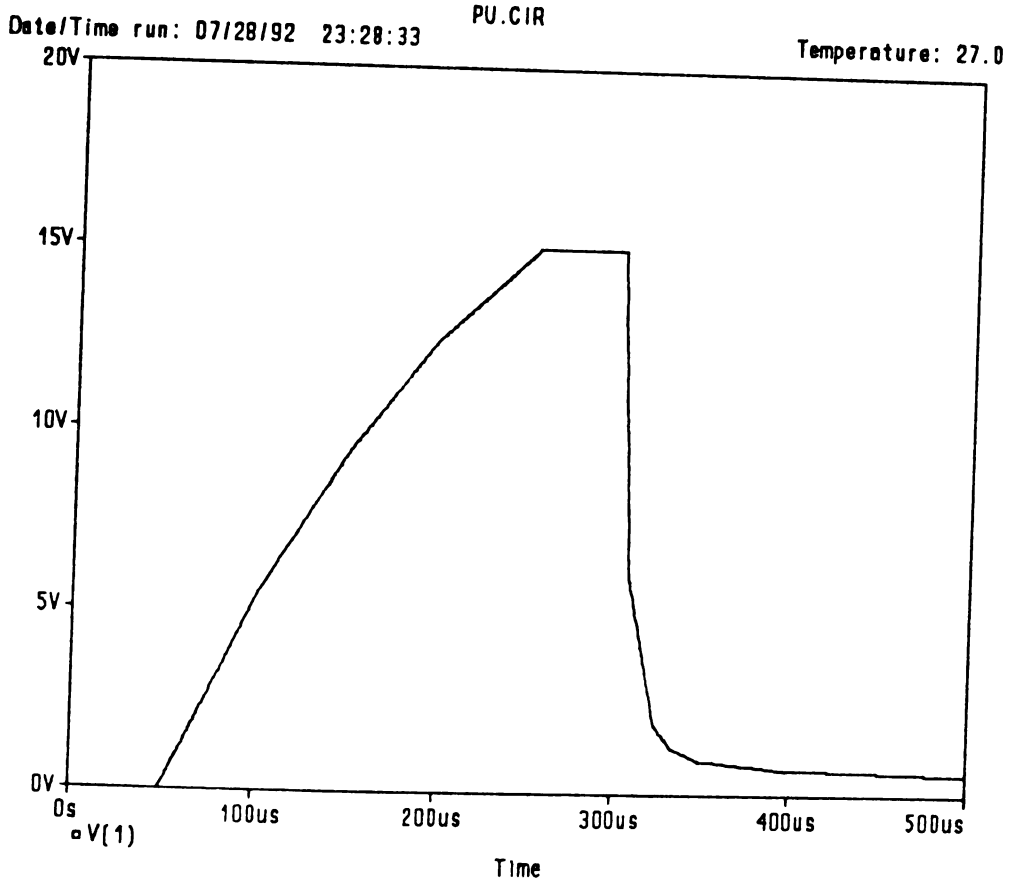

Figure 5.14 Power up and down, square wave, T = 25, measured

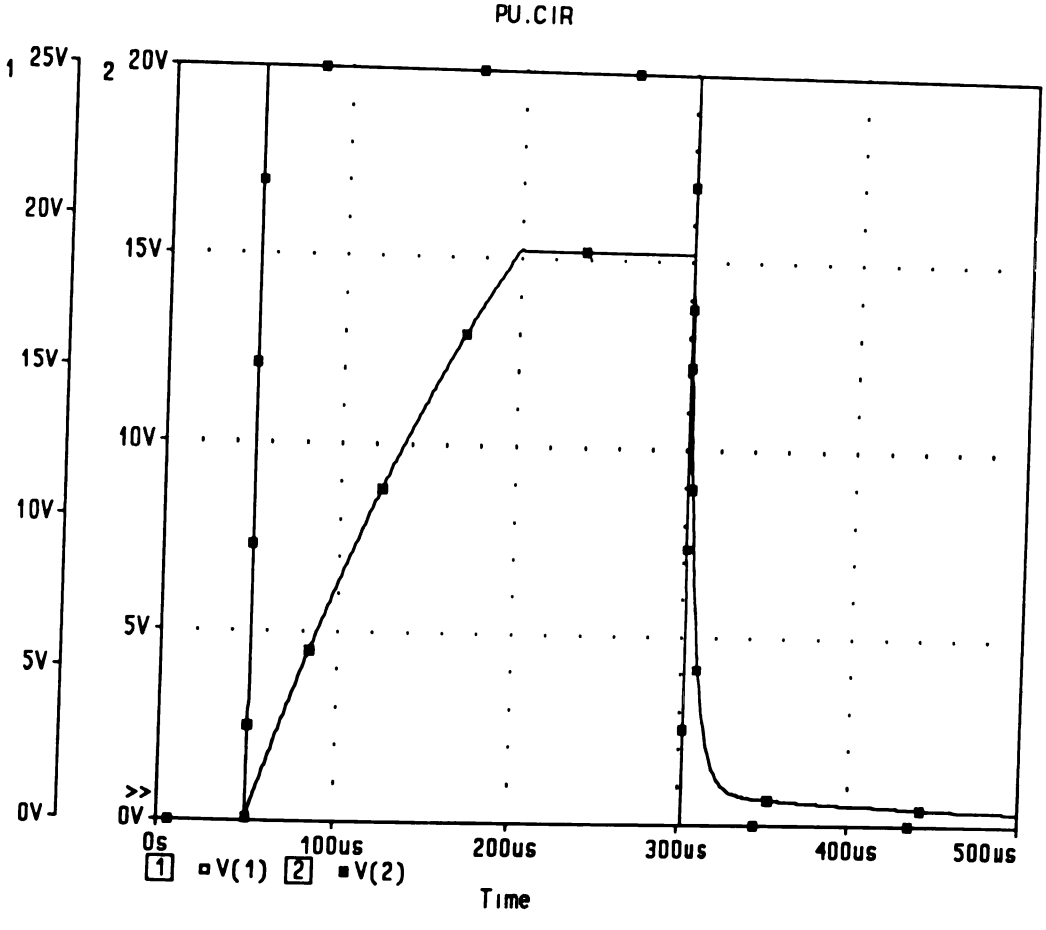

Figure 5.15 Power up and down, square wave, T = 25, macromodel

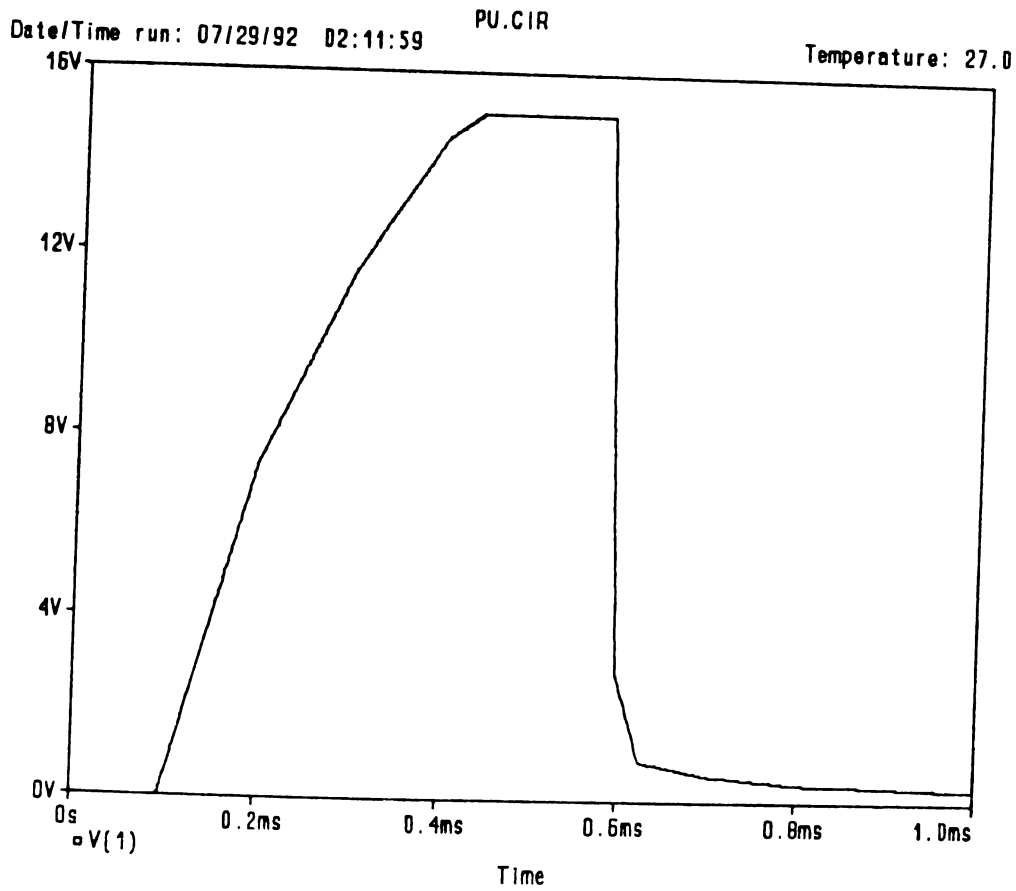

Figure 5.16 Power up and down, square wave, T = 125, measured

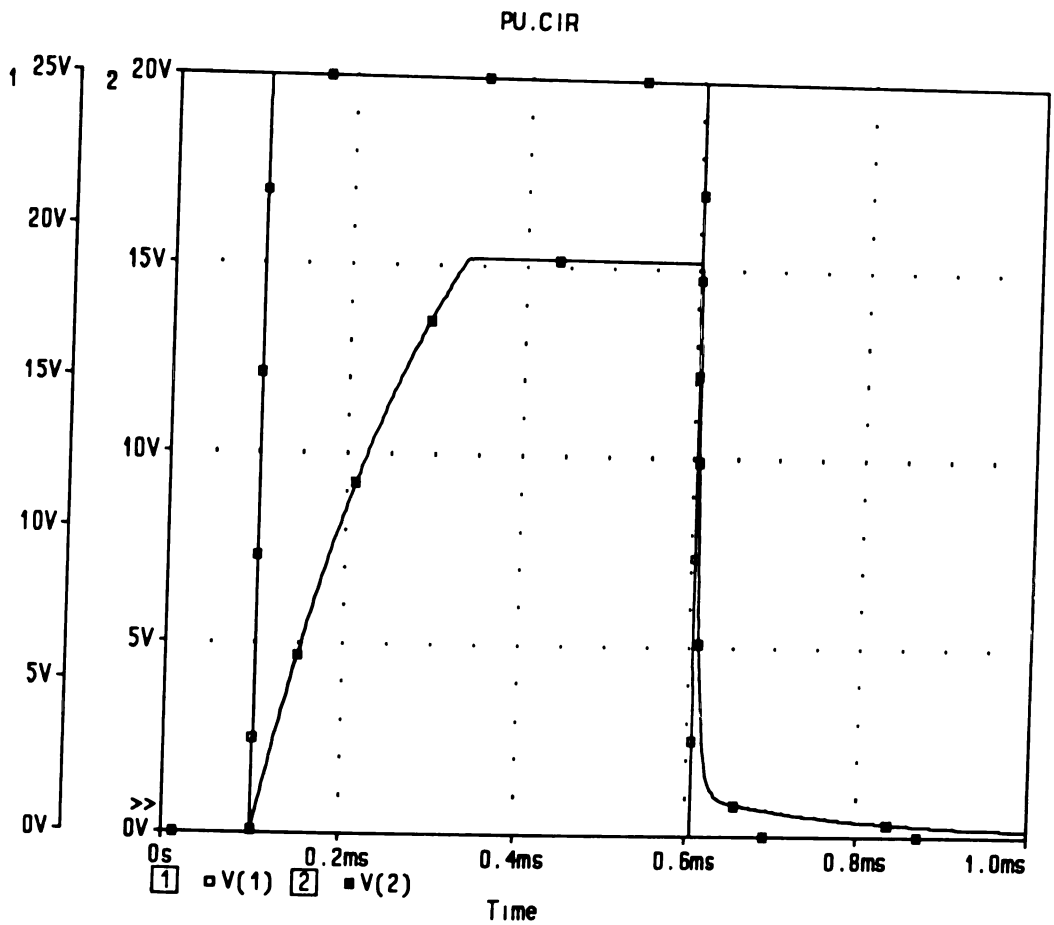

Figure 5.17 Power up and down, square wave, T = 125, macromodel

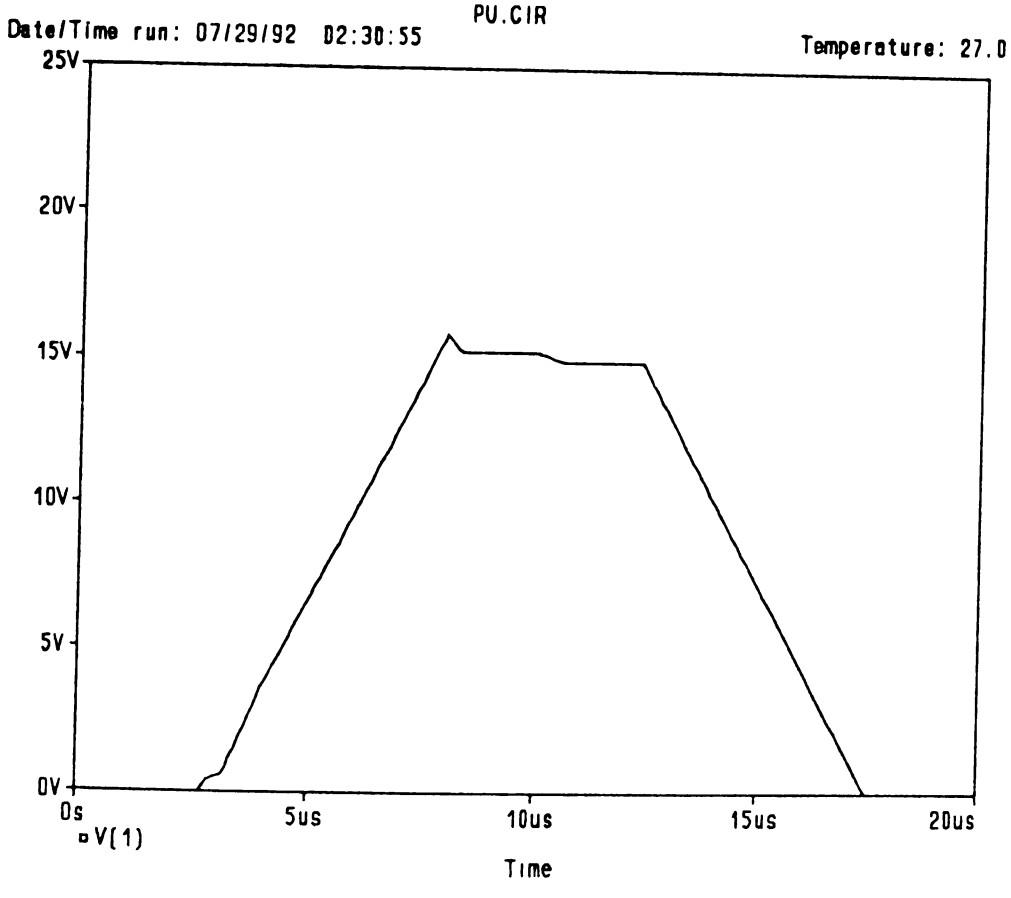

Figure 5.18 Power up and down, triangle wave, measured

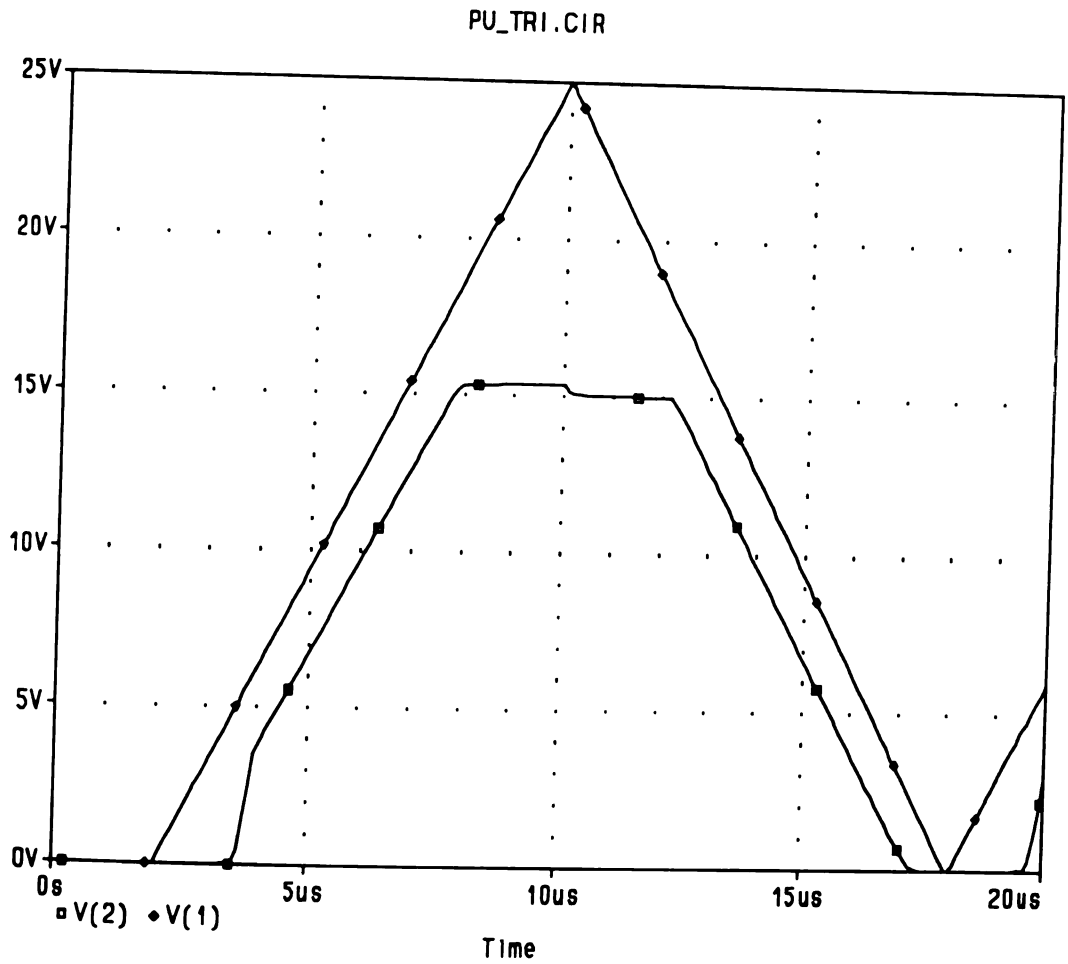

Figure 5.19 Power up and down, triangle wave, macromodel

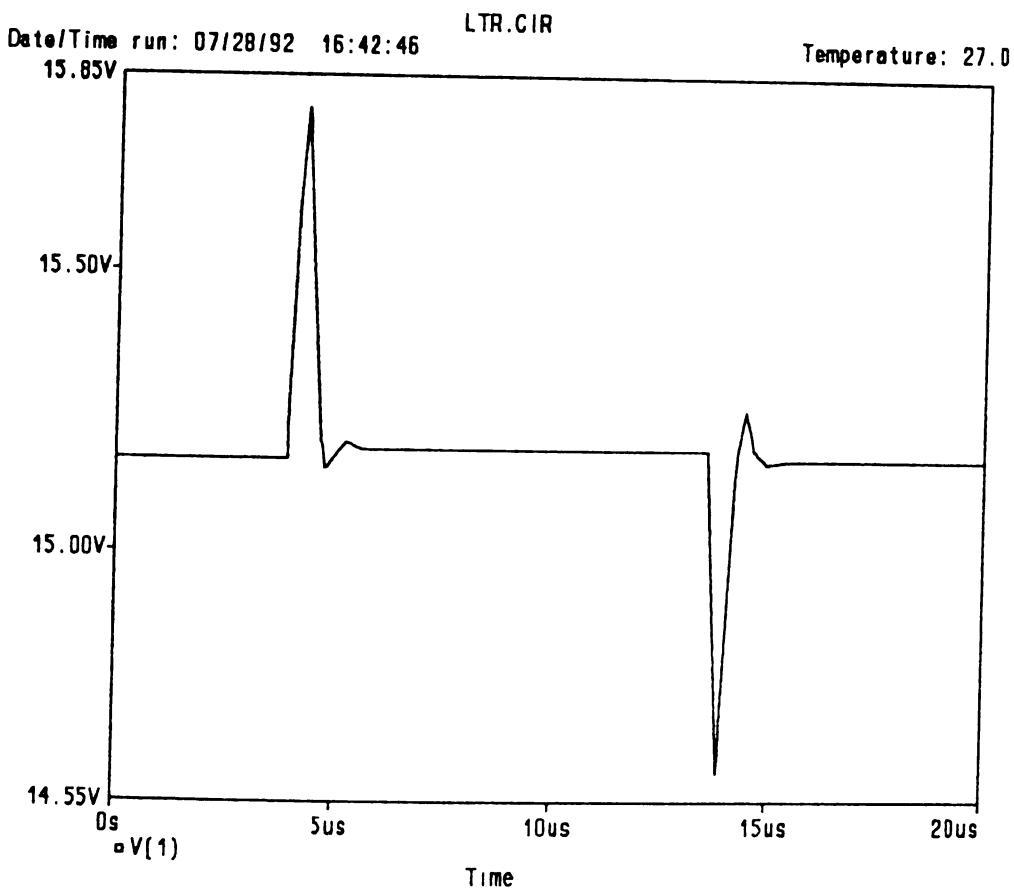

Figure 5.20 Line transient response, measured

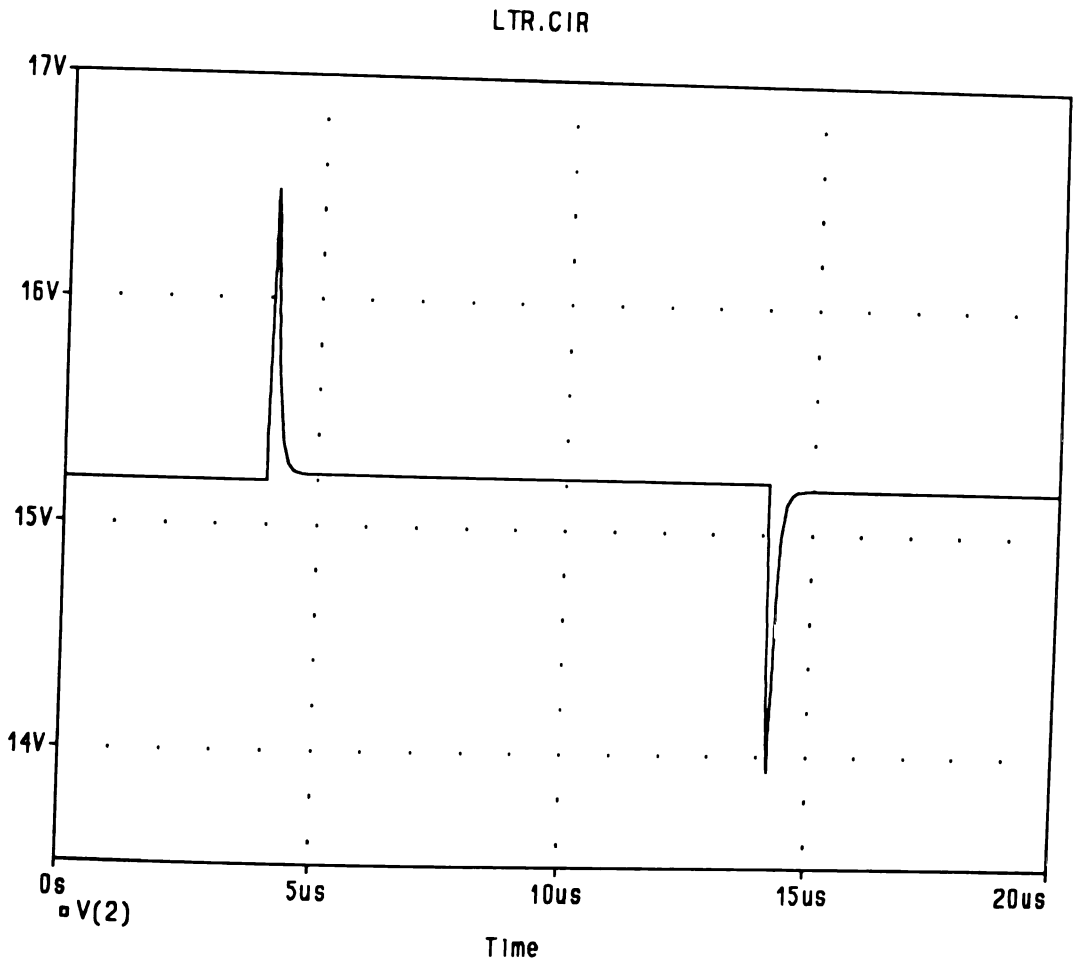

Figure 5.21 Line transient response, macromodel

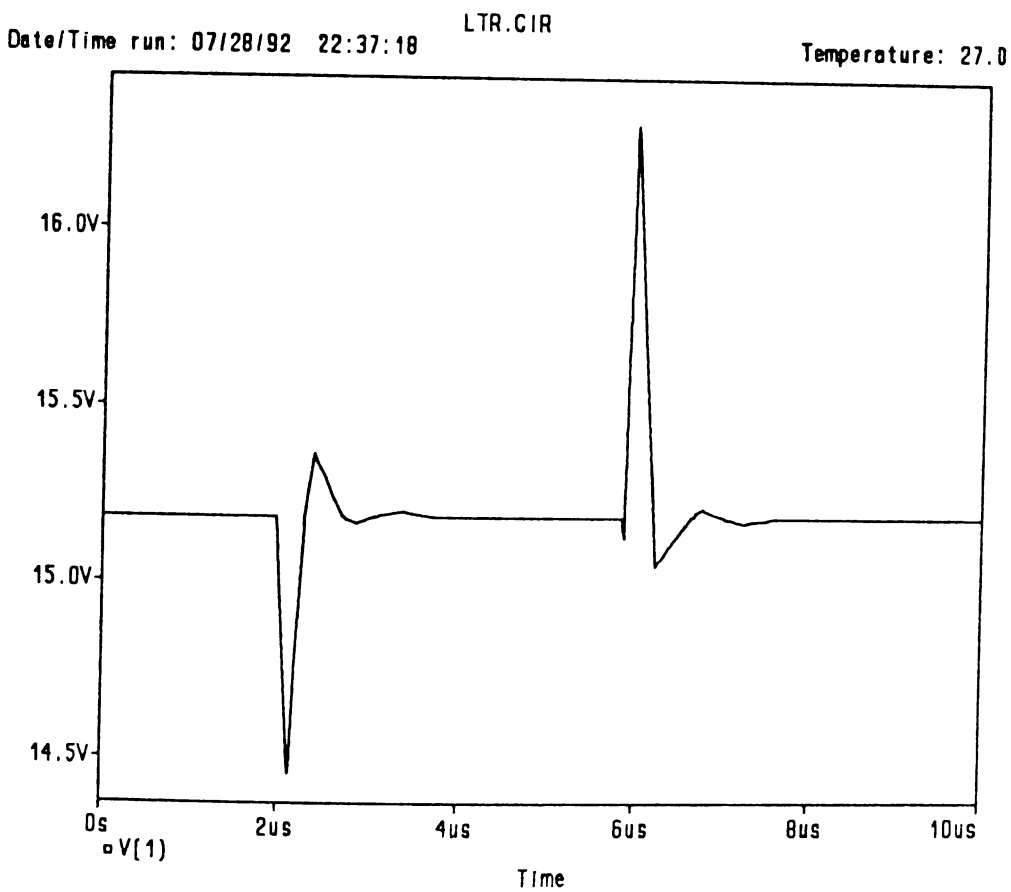

Figure 5.22 Load transient response, measured

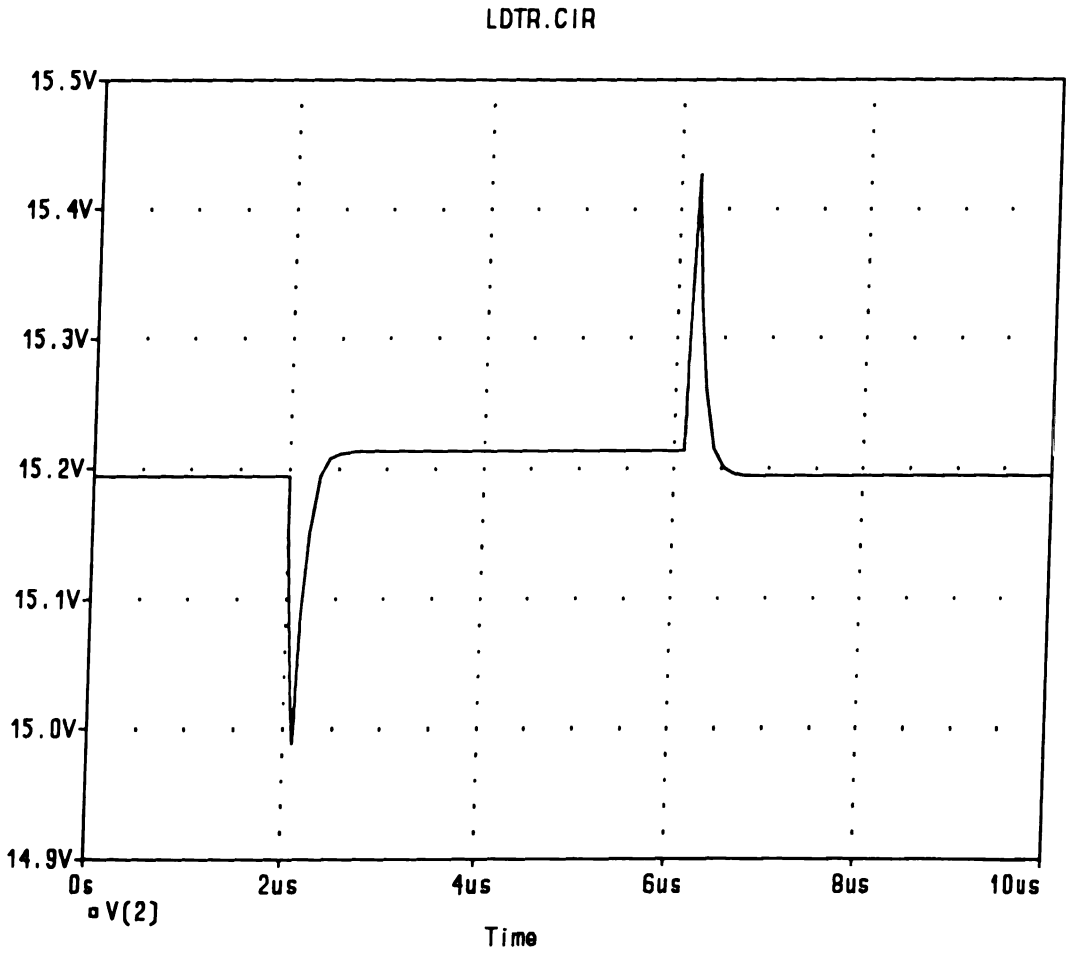

Figure 5.23 Load transient response, macromodel

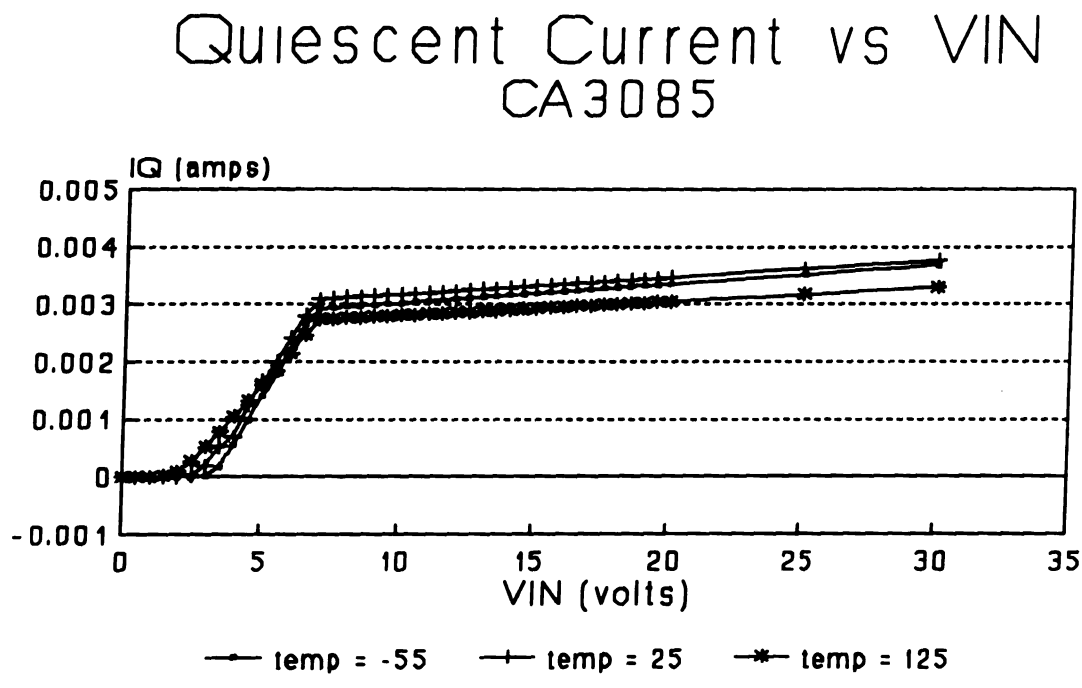

Figure 5.24 Quiescent current vs input voltage, measured

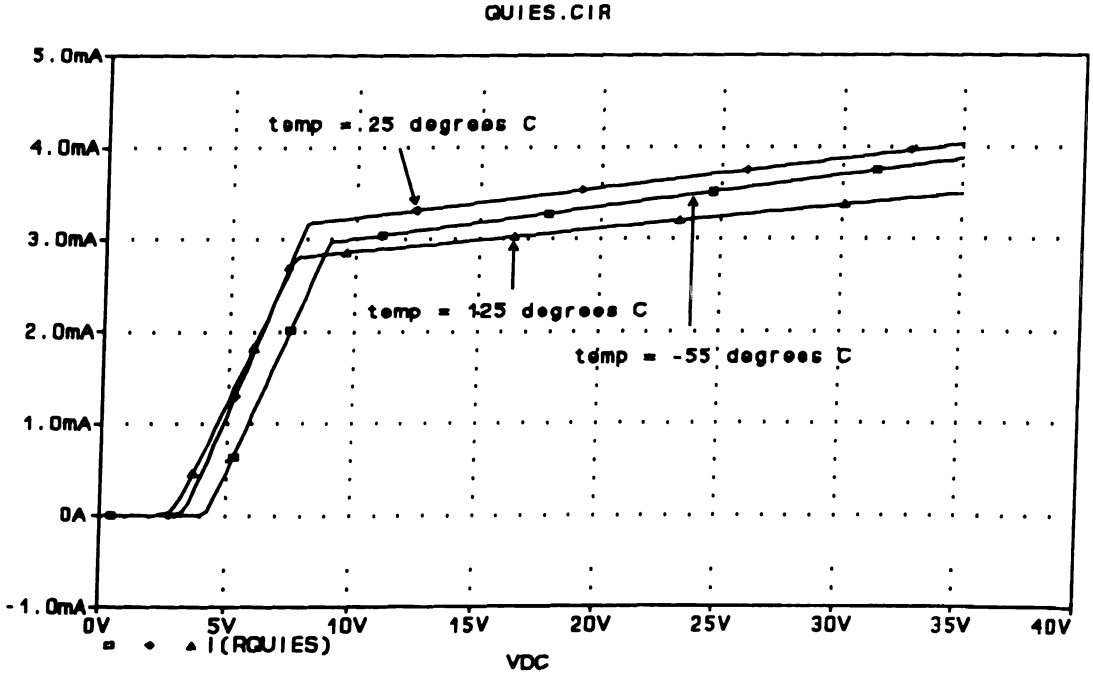

Figure 5.25 Quiescent current vs input voltage, macromodel

Comparison of Macromodel parameters and Measured Parameters				
QUANTITY		**-55°C**	**25°C**	**125°C**
RR_{LF}	lab	47.63db	42.08db	52.81db
	model	47.29db	41.93db	52.20db
$P1_{RR}$	lab	12kHz	23kHz	6kHz
	model	12.4kHz	23.3kHz	6.5kHz
IQ	lab	2.942mA	3.106mA	2.738mA
	model	2.987mA	3.172mA	2.810mA
ΔIQ/ΔVin	lab	33.49u	29.38u	24.44u
	model	34.42u	31.17u	25.11u
max load current	lab	139.5mA	115.88mA	82.72mA
	model	132.5mA	121.88mA	92.31mA
dropout voltage	lab	6.28V	2.84V	2.46V
	model	3.13V	2.82V	2.44V
$\Delta V_{OUT}/\Delta I_{LOAD}$	lab	-3.75Ω	-.4091Ω	.483mΩ
	model	-3.71Ω	-.388Ω	0.0117Ω

Table 5.3 Macromodel comparisons with lab data

5.7 TEST CIRCUITS

5.7.1 Pspice Test Circuits

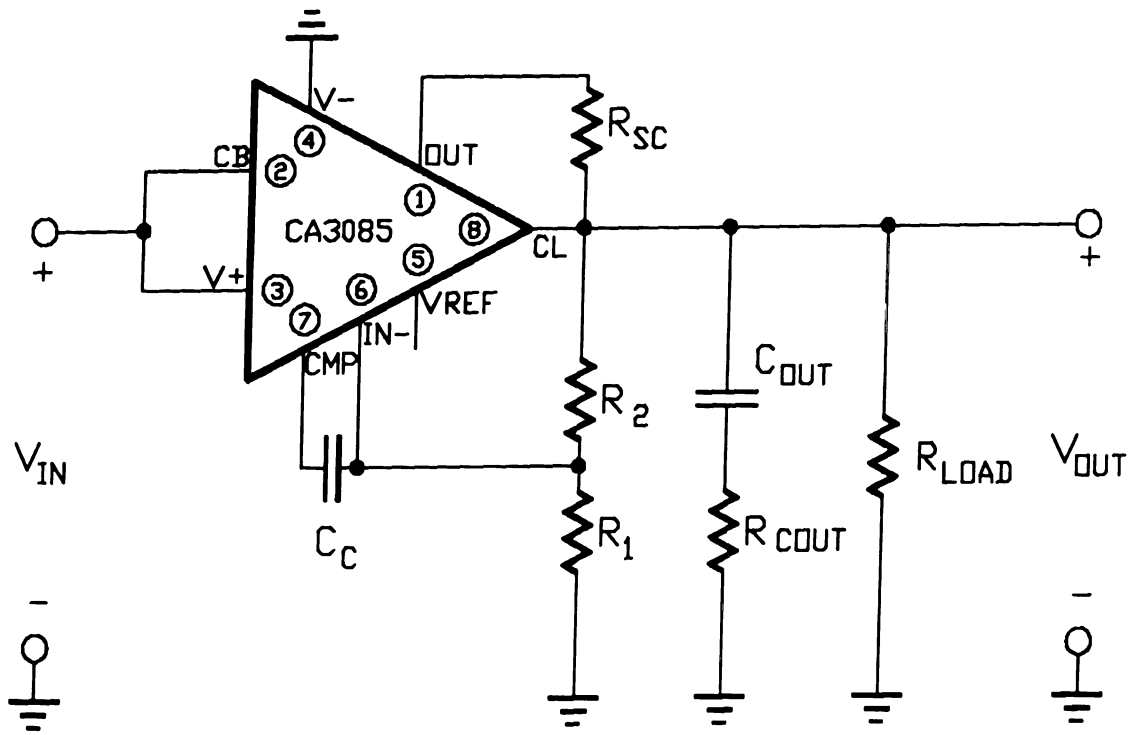

Figure 5.26 Basic PSpice test circuit

```
RR.CIR
*
*RIPPLE REJECTION FOR THE CA3085
*
VDC     7 0 DC 25
VAC     1 7 AC 1
RSC     6 2 5.602
CC      3 4 113.01P
R2      2 4 818.98
R1      4 0 100.1
RLOAD   2 0 300.617
*PIN NO*1*2*3*4*5*6*7*8*****
XREG    6 1 1 0 5 4 3 2 3085
.OP
.OPTIONS ITL5=0 ITL1=300 ITL2=300 NOPAGE
.LIB CA3085.LIB
.OP
.TEMP -55 25 125
.OPTIONS TNOM=25
.AC DEC 20 10 1MEG
.PROBE
.END
```

```
PU.CIR
*
*POWER UP WITH SQUARE WAVE FOR THE CA3085
*
VPULSE  1 0 PULSE (0 25 50U 0 0 250U)
RSC     6 2 5.602
CC      3 4 113.01P
R2      2 4 818.98
R1      4 0 100.1
RLOAD   2 0 300.617
COUT    2 100 .9602U
ROUT    100 0 1.034
*PIN NO*1*2*3*4*5*6*7*8*****
XREG    6 1 1 0 5 4 3 2 3085
.OP
.OPTIONS ITL5=0 ITL1=300 ITL2=300 TNOM=25
.TRAN 1U 500U 0 1U
.TEMP = -55 25 125
.LIB CA3085.LIB
.PROBE
.END
```

```
PU_TRI.CIR
*
*POWER UP, WITH TRIANGLE WAVE, FOR THE CA3085
*
VPULSE  1 0 PULSE (0 25 2U 8U 8U .01U 16.1U)
RSC     6 2 5.602
CC      3 4 113.01P
R2      2 4 818.98
R1      4 0 100.1
RLOAD   2 0 300.617
*PIN NO*1*2*3*4*5*6*7*8*****
XREG    6 1 1 0 5 4 3 2 3085
.OP
.OPTIONS ITL5=0 ITL1=300 ITL2=300 TNOM=25
.TRAN .1U 20U 0 .1U
.LIB CA3085.LIB
.TEMP 25
.PROBE
.END
```

```
LTR.CIR
*
*LINE TRANSIENT RESPONSE FOR THE CA3085
*
VDC     7 0 DC 25
VPULSE  100 7 PULSE (0 4 4U 0 0 10U)
ROUT    100 1 0.1
RSC     6 2 5.602
CC      3 4 113.01P
R2      2 4 818.98
R1      4 0 100.1
RLOAD   2 0 300.617
*PIN NO*1*2*3*4*5*6*7*8*****
XREG    6 1 1 0 5 4 3 2 3085
.OP
.OPTIONS ITL5=0 TNOM=25
.TEMP = 25
.TRAN .1U 20U 0 .1U
.LIB CA3085.LIB
.PROBE
.END
```

```
LDTR.CIR
*
*LOAD TRANSIENT RESPONSE FOR THE CA3085
*
VDC     1 0 DC 25
VPULSE  7 0 PULSE (14.98 0 2U 0 0 4U 10U)
RSC     6 2 5.602
CC      3 4 113.01P
R2      2 4 818.98
R1      4 0 100.1
RL      2 7 300.617
*PIN NO*1*2*3*4*5*6*7*8*****
XREG    6 1 1 0 5 4 3 2 3085
.OP
.OPTIONS ITL5=0 TNOM=25
.LIB CA3085.LIB
.TRAN .1U 10U 0 .1U
.TEMP -55 25 125
.PROBE
.END
```

```
QUIES.CIR
*
*QUIESCENT CURRENT FOR THE CA3085
*
VDC     3 0 DC 40
ROPEN1  1 0 1000MEG
ROPEN2  2 0 1000MEG
RQUIES  4 0 100.383
ROPEN3  5 0 1000MEG
ROPEN4  8 0 1000MEG
CC      7 0  113P
*PIN NO*1*2*3*4*5*6*7*8*****
XREG    1 2 3 4 5 0 7 8 3085
.OP
.DC VDC 0 35 .25
.OPTIONS ITL5=0 ITL1=300 ITL2=300 TNOM=25
.LIB CA3085.LIB
.TEMP = -55 25 125
.PROBE
.END
```

```
DROPOUT.CIR
*
*DROPOUT CHARS FOR THE CA3085
*
VDC     100 0 DC 20
ROUT    100 1 0.1
RSC     6 2 0.00001
CC      3 4 113.01P
R2      2 4 818.98
R1      4 0 100.1
RLOAD   2 0 300.617
*PIN NO*1*2*3*4*5*6*7*8*****
XREG    6 1 1 0 5 4 3 2 3085
.OP
.OPTIONS ITL5=0 ITL1=300 ITL2=300 TNOM=25
.TEMP -55 25 125
.DC VDC 0 30 .25
.LIB CA3085.LIB
.PROBE
.END
```

5.7.2 Measurement Test Circuits

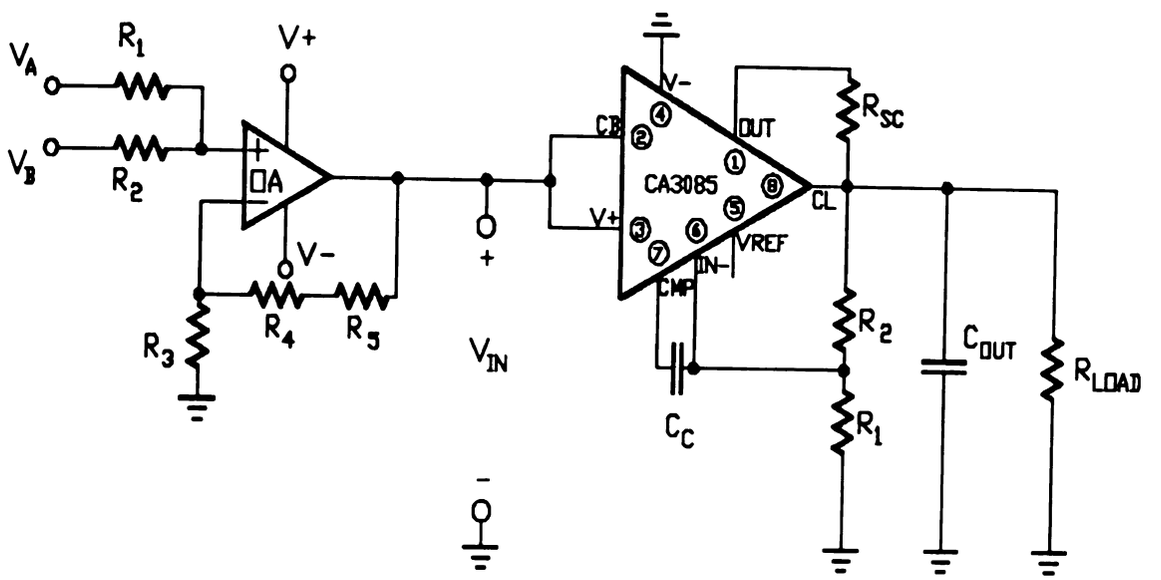

Figure 5.27 Test circuit No. 1

The conditions of Test circuit No. 1 are stated.

R_1 measured 100.1Ω.
R_2 measured 818.8Ω.
R_{SC} measured 5.602Ω.
R_{LOAD} measured 300.617Ω.
C_{OUT} measured .9602uF and had a series resistance of 1.034 at 100kHz
C_C measured 113.01pF at 100kHz and had a neglible series resistance.
R_1, R_2, R_3, R_4, and R_5 have nominal values of 1kΩ.
V+ is a positive 50V dc power supply.
V- is a negative 10V dc power supply.
OA is a Burr-Brown OPA541 Op-Amp.
The CA3805 resides inside a temperature chamber. Wires are connected at the terminals of the CA3085 to allow it to be connected outside the chamber to the test circuit.

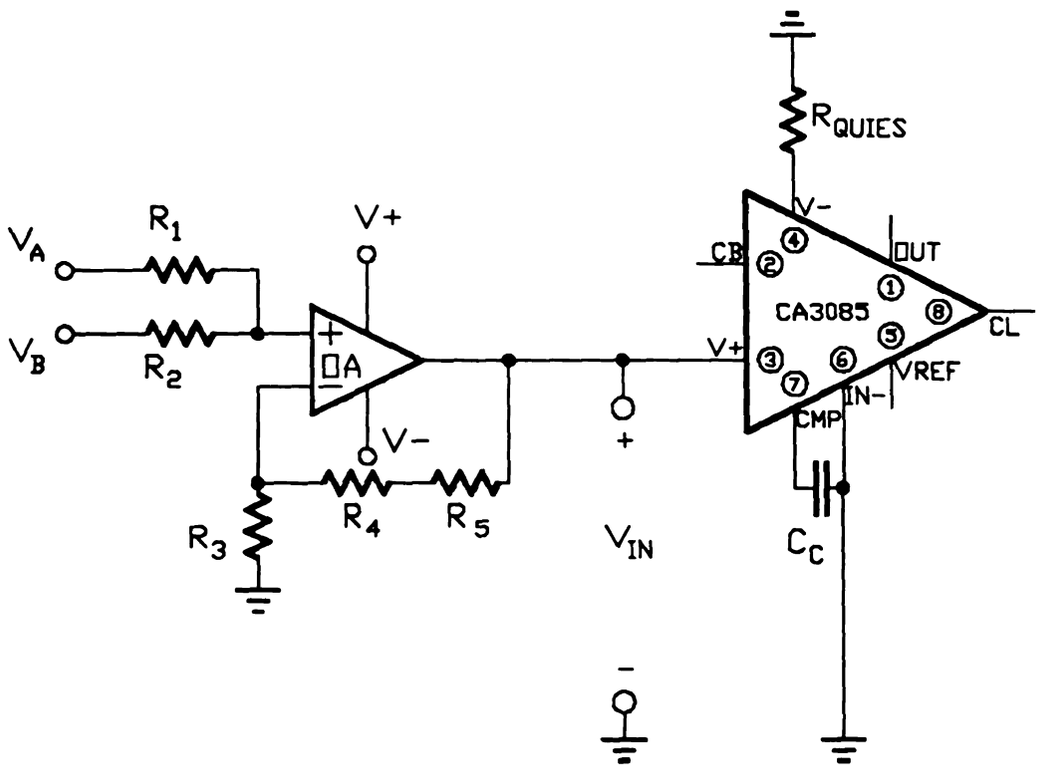

Figure 5.28 Test circuit No. 2

The conditions of Test circuit No. 2 are stated.

R_{QUIES} measured 100.383Ω.

C_C measured 113.01pF at 100kHz and had a neglible series resistance.

R_1, R_2, R_3, R_4, and R_5 have nominal values of 1kΩ.

V+ is a positive 50V dc power supply.

V- is a negative 10V dc power supply.

OA is a Burr-Brown OPA541 Op-Amp.

The CA3805 resides inside a temperature chamber. Wires are connected at the terminals of the CA3085 to allow it to be connected outside the chamber to the test circuit.

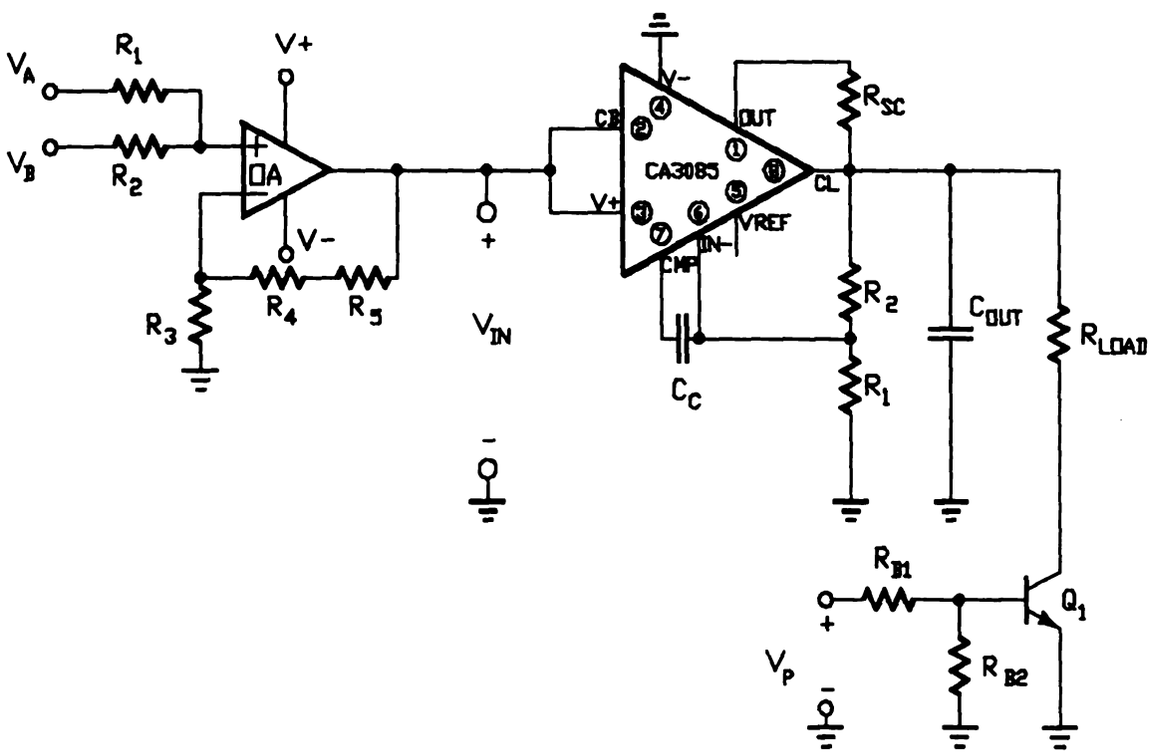

Figure 5.29 Test circuit No. 3

The conditions of Test circuit No. 3 are stated.

R_1 measured 100.1Ω.
R_2 measured 818.8Ω.
R_{SC} measured 5.602Ω.
R_{LOAD} measured 300.617Ω.
C_{OUT} measured .9602uF and had a series resistance of 1.034 at 100kHz.
C_C measured 113.01pF at 100kHz and had a neglible series resistance.
R_1, R_2, R_3, R_4, and R_5 have nominal values of 1kΩ.
V+ is a positive 50V dc power supply.
V- is a negative 10V dc power supply.
OA is a Burr-Brown OPA541 Op-Amp.
The CA3805 resides inside a temperature chamber. Wires are connected at the terminals of the CA3085 to allow it to be connected outside the chamber to the test circuit.
Q_1 is a 2N4401 npn transistor.
R_{B1} has a nominal value of 10kΩ.
R_{B2} has a nominal value of 1kΩ.

1) Ripple Rejection was done using test circuit 1. V_A was connected to an ac function generator. V_B was connected to a positive dc power supply. These were set to produce a 25V dc voltage at V_{IN} with a sine wave superimposed for both. C_{OUT} was not connected. Voltages and phases were measured with a Tektronix 11401 scope.

2) The V_{IN} vs V_{OUT} for both chips, V_{OUT} at V_{IN} = 25V for the CA3085 was done using test circuit 1. V_A was connected to an pulse generator and pulsed at 100Hz, with a duty cycle of 5%. V_B was grounded. These were set to produce the necessary voltage at V_{IN}. C_{OUT} was not connected. Voltages were measured with a Tektronix 11401 scope.

3) The power up and down square wave measurements were done using test circuit 1. V_A was connected to an pulse generator. V_B was grounded. Voltages were measured with a Tektronix 11401 scope.

4) The power up and down triangle measurements was done using test circuit 1. V_A was connected to an ac function generator, generating a triangle wave. V_B was connected to a positive dc power supply. These were set to produce a triangle wave at V_{IN} which has a maximum value of 25V and a minimum value of 0V. C_{OUT} was not connected. Voltages were measured with a Tektronix 11401 scope.

5) The quiescent current measurements were done using test circuit 2. V_A was connected to an pulse generator and pulsed at 100Hz, with a duty cycle of 5%. V_B was grounded. These were set to produce the necessary voltage at V_{IN}. R_{QUIES} measured 100.383Ω. Voltages were measured with a Tektronix 11401 scope. The voltage was measured across R_{QUIES} and divided by R_{QUIES} to give the quiescent current.

6) The load transient response measurements was done with test circuit 3. V_A was grounded. V_B was connected to a positive power supply to produce a dc voltage of 25V at V_{IN}. V_P was pulsed to allow Q1 to function as a switch, connecting R_{LOAD} on and off to ground to simulate the switching on and off of a load.

7) The maximum output current vs V_{IN} measurements were done using test circuit 1. V_A was connected to an pulse generator and pulsed at 100Hz, with a duty cycle of 5%. V_B was grounded. These were set to produce the necessary voltage at V_{IN}. R_{LOAD} measured 100.383Ω. Voltages were measured with a Tektronix 11401 scope. The voltage across R_{LOAD} was measured and then converted to a current.

8) The line transient response measurements was done with test circuit 1. V_A was connected to a pulse generator. V_B was connected to a positive dc power supply. These were set to produce a 25V dc voltage at V_{IN} with a pulse superimposed. Voltages were measured with a Tektronix 11401 scope.

CHAPTER 6

UA723 MACROMODEL DEVELOPMENT

6.1 INTRODUCTION

This chapter describes the development of the UA723 voltage regulator macromodel. The UA723 is a ten pin, programmable, positive, voltage regulator.

6.2 DEVELOPMENT OF THE UA723 MACROMODEL

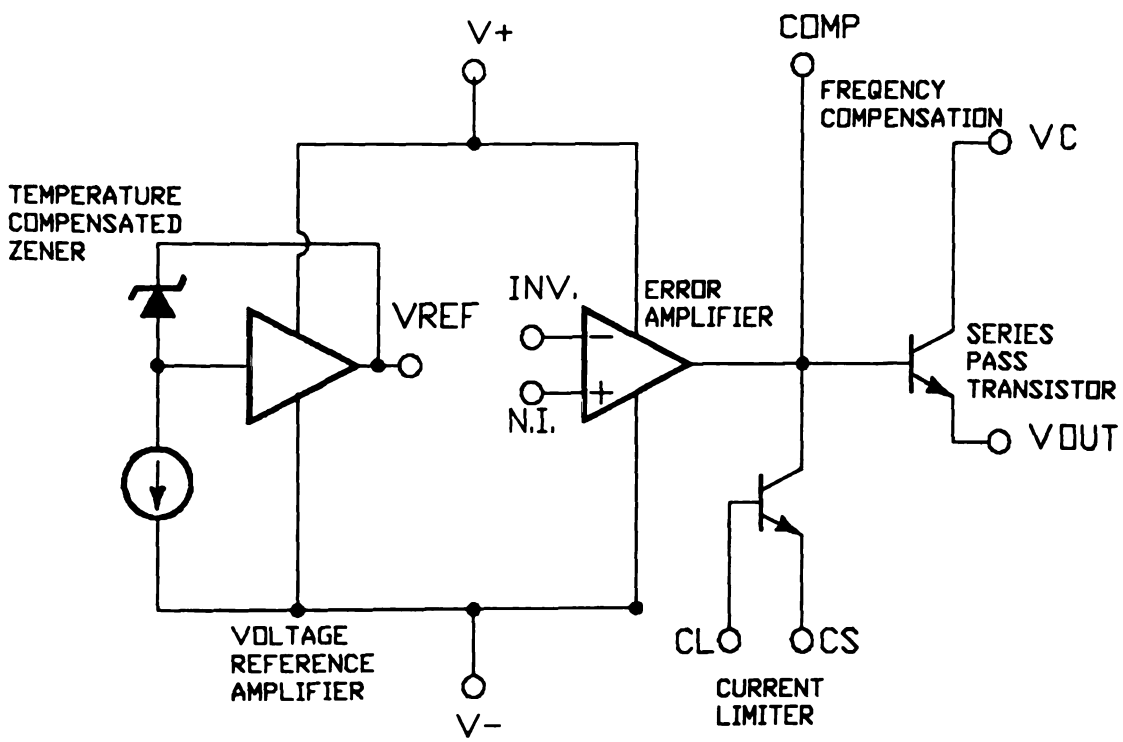

Figure 6.1 Functional block diagram for the UA723

The functional block of the UA723 is shown in Fig. (6.1). This gives the

starting point for the macromodel development. The macromodel for the UA723 is shown in Fig. (6.2). The voltage reference amplifier, the temperature compensated zener, and the associated biasing current source have been replaced by D_{Z1}, D_{ZR}, R_Q, R_{R1}, R_{R2}, E_R, L_R, C_R, and R_{CR}. These elements provide the necessary reference for pin 5, labeled V_{REF} in Figures (6.1) and (6.2). The error amplifier is replaced by E_A, R_{IN}, R_O, D_L, D_+, D_-, V_+, V_-, and E_+. The series pass transistor is replaced by two transistors, Q_{P1} and Q_{P2}. These transistors and R_E are configured exactly as they are in the actual UA723 chip. Associated with the transistors are a slight base resistance, R_{B1} and R_{B2}, some frequency response adding by C_{B1}, C_{B2}, R_{CB1} and R_{CB2}. Q_L and E_L provide the current limiting, replacing the current limiter in the functional block diagram. V_{LDR} is a dc voltage source set to zero to sense output current and is used in the load regulation, along with H_{LDR}. G_{Q1} and G_{Q2} provide the UA723 with quiescent current. Temperature sensing circuitry is provided for by I_T, R_{T1}, and R_{T2} as well as G_T, R_{T3} and V_{GT}. Finally, D_{DIS} is provided to add the capacitive discharge characteristics. This provides the necessary overview of the UA723 macromodel.

The UA723 needs to be configured in a circuit to provide regulation, as did the CA3085. The test circuit chosen comes from the data sheets and is shown in Fig. (6.3). This is termed the high voltage application for the UA723. In this circuit, $V_{INV} \approx V_{REF}$ so this circuit provides a regulated output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R_1}{R_2}\right). \qquad (6.1)$$

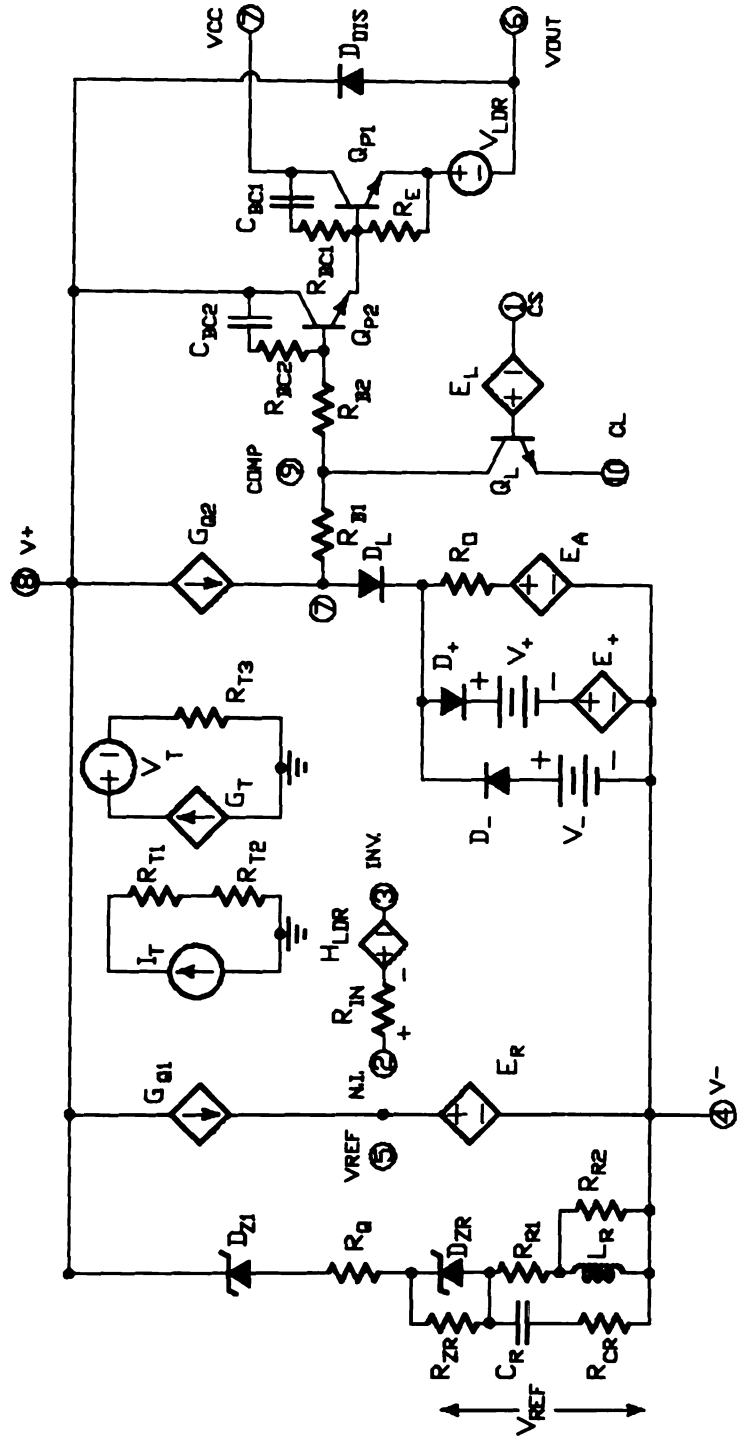

Figure 6.2 Macromodel for the UA723

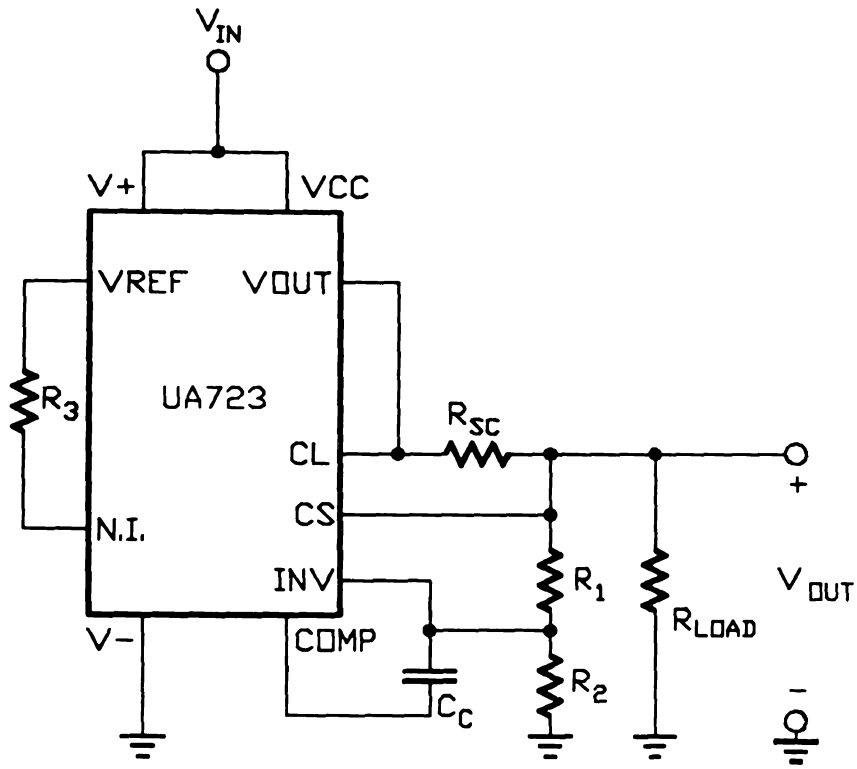

Figure 6.3 Application circuit for the UA723

6.2.1 The V_{REF} Pin

The reference voltage generator for pin 4 consists of D_{Z1}, D_{ZR}, R_{ZR}, R_Q, R_{R1}, R_{R2}, L_R, C_R, and R_{CR}. The UA723 provides a reference voltage of approximately 7V. This 7V is provided for mainly by D_{ZR} operating in the breakdown region, but the reference voltage is the total dc voltage across D_{ZR} and R_{R1}. R_{R1} is selected so that it does not contribute much to the overall 7V, but does provide for enough voltage variation with input voltage so that it is the main contributor to low frequency ripple rejection and line regulation. This comes directly from Eqn. (6.1).

E_R provides a buffer for the actual generated voltage reference characteristics to the rest of the circuit.

L_R, C_R, R_{CR}, R_{R1}, and R_{R2} provide the reference with frequency response characteristics. This contributes to the ripple rejection vs frequency and line transient

response. Under dc operation, these elements do not effect the circuit.

R_Q provides for changes in quiescent current with changes in input voltage. It is much larger than the differential resistance of the diodes and R_{R1} and it functions identically to R_Q in the circuits developed prior to the UA723.

Note in Fig. (6.4), the V_{OUT} vs V_{IN} characteristics, there is an associated "on" voltage with the circuit. This effect is modeled by the diode D_{Z1}. This gives

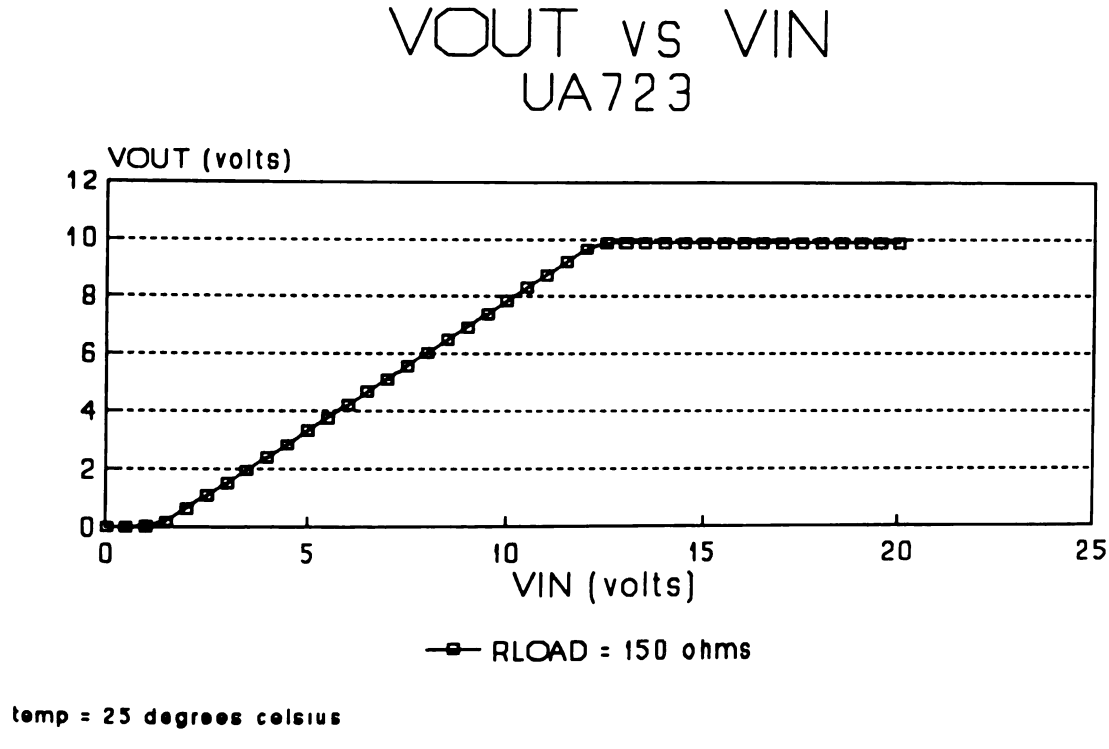

Figure 6.4 V_{OUT} vs V_{IN} characteristics for the UA723

$$BV_{DZ1} = V_{ON} \tag{6.2}$$

6.2.2 The Error Amplifier

The error amplifier is modeled as a simple voltage controlled voltage source with a dc gain. The controlling voltage is the voltage across R_{IN}, which represents some input

resistance for the amplifier. R_O, D_+, D_-, V_+, V_-, and E_+ provide for maximum and minimum clamping for the amplifier.

6.2.3 Ripple Rejection Modeling

Fig. (6.5) gives an example of ripple rejection vs frequency for the UA723. It is the usual one pole response which means a one-zero transfer function. In modeling

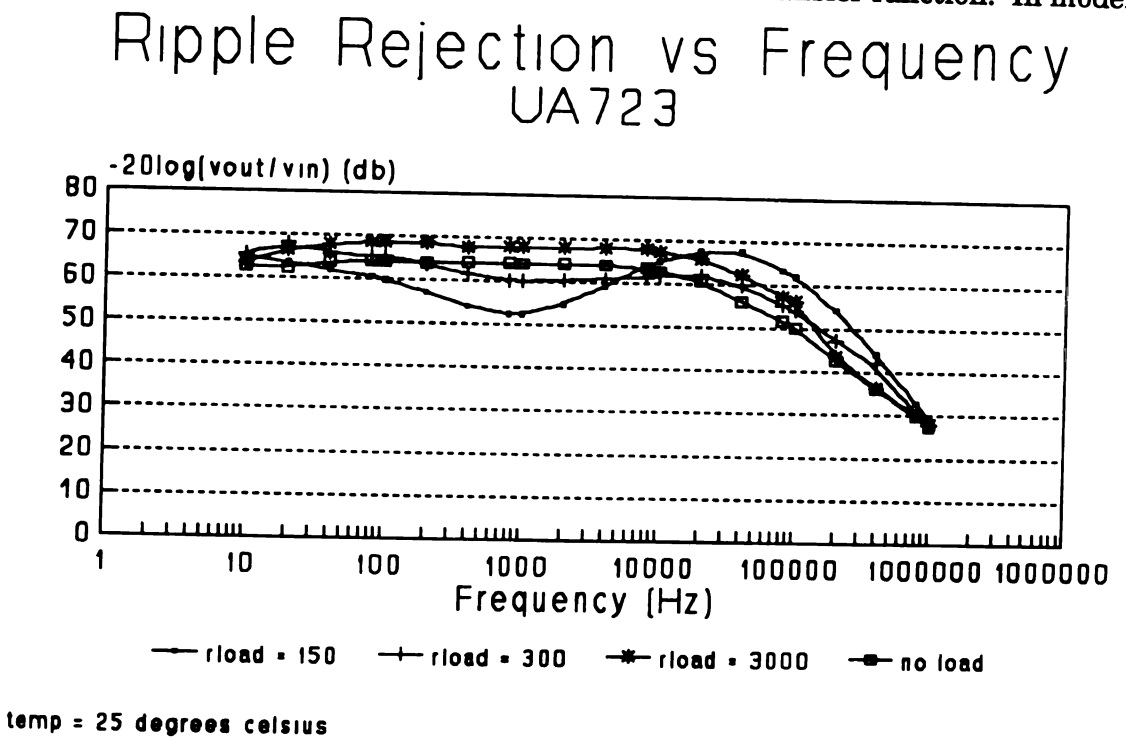

Figure 6.5 Ripple rejection vs frequency, measured

ripple rejection vs frequency, the following approximations are made. The first approximation is that the low frequency ripple rejection for all the loads are the same. The second approximation is that the first pole in ripple rejection is the same for all loads. As seen in Fig. (6.5), the approximations are fair. It should be pointed out that for the UA723 ripple rejection vs frequency was very difficult to measure. The above assumptions are made in part because they held true in the full chip simulations. Note that the "no load" ripple rejection in Fig. (6.5) will be used for modeling. The low frequency ripple rejection is due primarily to dc changes in the reference voltage. Dc

changes in reference voltage with input voltage are given by, with $R_{ZR} \gg r_{DZR}$,

$$\Delta V_{REF} = \Delta V_{IN}\left(\frac{r_{DZR}+R_{R1}}{r_{DZR}+R_{R1}+r_{DZ1}+R_Q}\right), \tag{6.3}$$

and with a few approximations,

$$\Delta V_{REF} \approx \Delta V_{IN}\left(\frac{r_{DZR}+R_{R1}}{R_Q}\right). \tag{6.4}$$

Low frequency ripple rejection can be determined from Eqn. (6.1) as

$$RR_{LF} \approx \frac{\Delta V_{OUT}}{\Delta V_{IN}} \approx \frac{\Delta V_{REF}\left(1+\frac{R_2}{R_1}\right)}{\Delta V_{IN}}, \tag{6.5}$$

and substituting Eqn. (6.4) into (5) gives

$$RR_{LF} \approx \left(\frac{r_{DZR}+R_{R1}}{R_Q}\right)\left(1+\frac{R_2}{R_1}\right). \tag{6.6}$$

The first pole of the ripple rejection is due to first zero of the voltage reference. This is

$$Pl_{RR} \approx \frac{R_{R1}}{L_R}, \tag{6.7}$$

if R_Q and R_{R2} are large in comparison to R_{R1} and C_R is very small.

The capacitor C_R, as well as R_{CR}, and R_{R2} also contribute to the frequency response, but their effects show up mainly in the line transient response.

6.2.4 Quiescent Current Modeling

Quiescent current vs input voltage is shown in Fig. (6.6). The elements which contribute to quiescent current are R_Q, G_{Q1}, and G_{Q2}. G_{Q2} is voltage controlled current

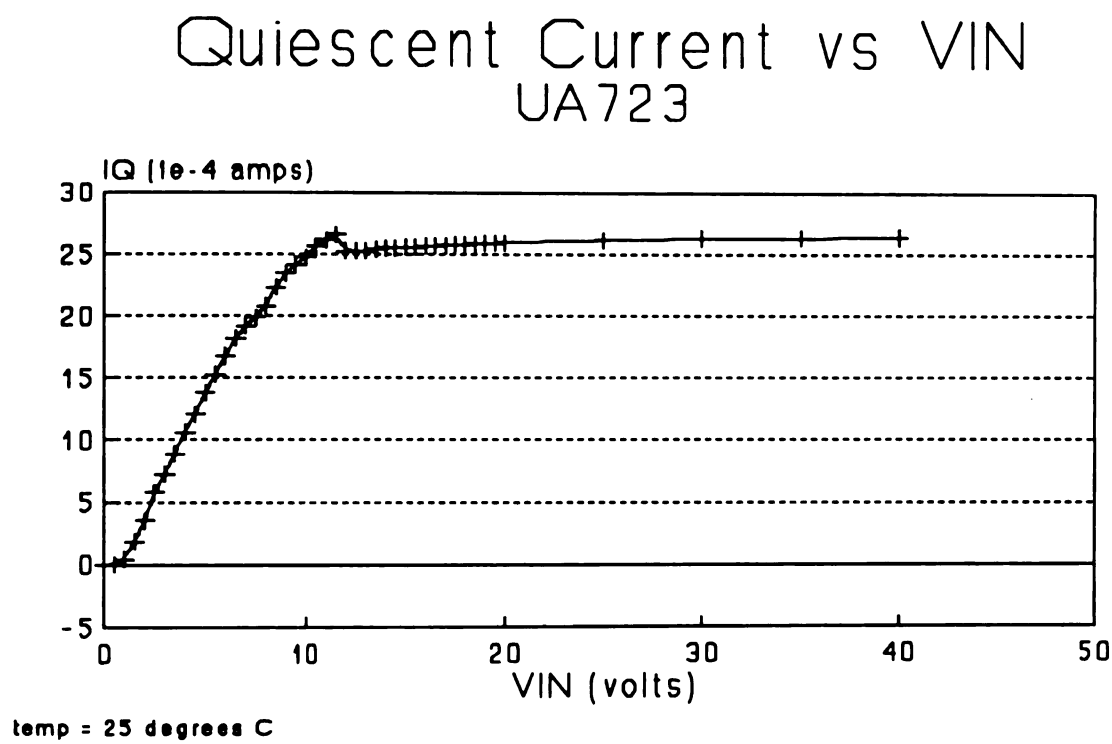

Figure 6.6 Quiescent current vs input voltage, measured

source which senses the voltage across the reference voltage. This provides it with the characteristics seen in Fig. (6.6). The voltage controlled current is defined generically in the macromodel as

$$G_{Q1}\ n+\ n-\ poly(2)\ V_{REF}\ V(100000)\ 0\ a_1\ 0\ 0\ a_4\ 0\ 0\ 0\ a_8.$$

V_{REF} is one of the controlling voltages and V(10000) is equal to ΔT. This is identical to what is found with the CA3085 temperature sensing circuit, and ΔT is generated from an identical circuit. G_{Q1} is identical to G_{B1} for the CA3085, so

$$I_{GQ1} = a_1 V_{REF} + a_4 V_{REF} \Delta T + a_8 V_{REF} \Delta T^2, \tag{6.8}$$

or

$$I_{GQ1} = V_{REF}\left(a_1 + a_4\Delta T + a_5\Delta T^2\right). \tag{6.9}$$

The quantity in brackets is the new g_{B1}. G_{Q1} is the main contributor to quiescent current, and provides much of the changes in quiescent current variations with temperature. Note that for the room temperature model, $\Delta T = 0$ and

$$I_{GQ1} = a_1 V_{REF} \tag{6.10}$$

After the reference voltage has achieved it's nominal value, the current through G_{Q1} and G_{Q2} no longer changes. The changes in IQ with V_{IN} are due to R_Q, then,

$$R_Q = \frac{\Delta V_{IN}}{\Delta I_Q}. \tag{6.11}$$

6.2.5 Output Impedance Modeling

Output impedance vs frequency is not modeled, however output resistance is modeled.

H_{LDR} and V_{LDR} are added to provide output resistance effects. H_{LDR} is a current controlled voltage source which has the current through V_{LDR} as its controlling current. This functions exactly like in the CA3085 development. As with the CA3085,

$$R_{OUT} = -\frac{\Delta V_{OUT}}{\Delta I_{LOAD}}. \tag{6.12}$$

Using Eqn. (6.1), and the fact that variations in reference voltage with load current are given by

$$\Delta V_{REF} = -h_{LDR} I_{OUT}, \tag{6.13}$$

gives

$$R_{OUT} = h_{LDR}\left(1 + \frac{R_2}{R_1}\right). \tag{6.14}$$

The general PSpice description of the controlled source, HLDR, is

HLDR +n -n poly (2) V_{LDR} V_T 0 a_1 0 0 a_4 0 0 0 a_8,

for temperature variations. Since $I_{VLDR} \approx I_{OUT}$ and $I_{VT} = \Delta T$, the current through H_{LDR} is equal to

$$I_{HLDR} = I_{LOAD}\left(a_1 + a_4\Delta T + a_8\Delta T^2\right). \tag{6.15}$$

which allows the controlled source quadratic temperature sensitivity. This allows for a new definition for h_{LDR}, and that is

$$h_{LDR} \triangleq \left(a_1 + a_4\Delta T + a_8\Delta T^2\right). \tag{6.16}$$

At room temperature,

$$\frac{\Delta V_{OUT}}{\Delta I_{OUT}} = R_{OUT} = a_{1,HLDR}\left(1 + \frac{R_1}{R_2}\right). \tag{6.17}$$

6.2.6 Short Circuit Current Limiting

The short circuit current circuitry is D_B, Q_L and E_L. The short circuit current circuitry functions identically to that of the CA3085.

E_L carries the same PSpice definition

E_L n+ n- POLY(1) V(10000) a_1 a_2,

where V(10000) = ΔT, and the voltage across E_L the following value

For short circuit current limiting the UA723 requires an external resistor, R_{SC}

$$V_{EL} = a_1\Delta T + a_2(\Delta T)^2. \tag{6.18}$$

in Fig. (6.3) to be attached between 1 and 10, also in Fig. (6.3). All of the load current and current which biases R_1 and R_2 must pass though R_{SC}. The maximum output current is

$$I_{MAX} = I_{SC} = \frac{V_{BE,ON,CL}}{R_{SC}}. \tag{6.19}$$

$V_{BE,ON,QL}$ can be estimated as

$$I_{MAX}R_{SC} \approx V_{BEQL} \approx NF\,V_T \ln\left(\frac{g_{Q1}V_{REF}}{IS_{QL}}\right). \tag{6.20}$$

As with the CA3085, I_{MAX} is the sum of the maximum load current and the current biasing the external resistors at this point. For the UA723, it is sufficient to neglect the biasing current.

6.2.7 Power Up and Down, Square Wave

Fig. (6.7) gives the power up and power down for the square wave. The delay time in achieving regulation is due the slewing of the external compensation capacitor C_C. The slewing occurs because the capacitor must charge to a set value, but does not have enough current available to it to produce the change either nearly "instantaneously" or anywhere near several time constants of C_C. C_C has available to it a maximum current which is determined by G_{Q1}. It must charge to a voltage which is the difference between pins 9 and 2. From Fig. (6.7), V(9) is approximately the output voltage plus two diode drops. From Fig (6.9), V(2) is approximately the reference voltage V_{REF}. From the definition of slew rate

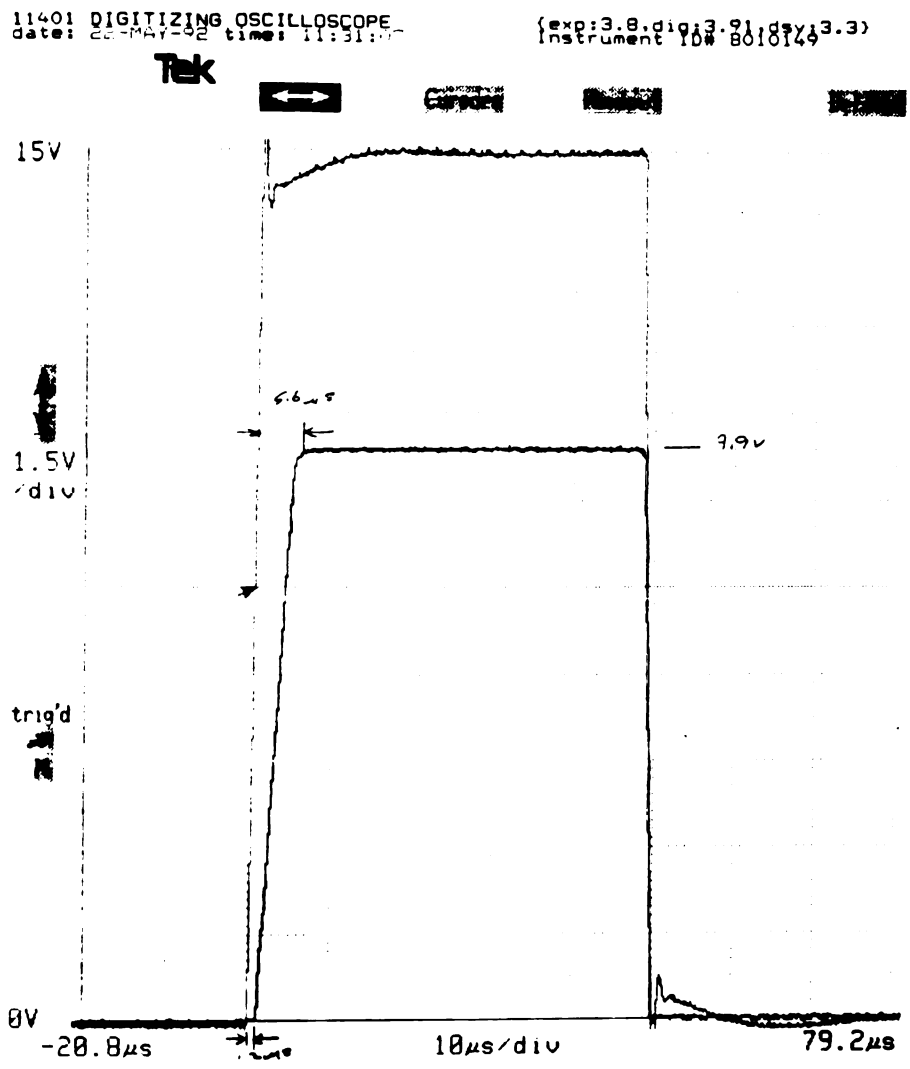

Figure 6.7 Power up and down, square wave, measured

$$\Delta t = C_C \frac{\Delta V}{I_{MAX}}, \tag{6.21}$$

and inserting the proper values gives

$$\Delta t = C_C \frac{V_{OUT} + 1.4 - V_{REF}}{g_{Q1} V_{REF}}. \tag{6.22}$$

The time delay seen can be estimated by Eqn. (6.22). It is desirable to determine an approximate value for g_{Q2} with this formula, but tweek g_{Q2} to match both power up and down square wave and power up an down triangle wave.

D_{DIS} is added for capacitive discharge behavior, and the default diode works well.

6.2.8 Power Up and Down, Triangle Wave

Fig. (6.8) gives the measured power up and down with triangle wave. The main component of power up and down which is modeled, and controlled by the user, is the slewing seen in the transistion from 0V to 3V. This, as with power up and down square wave, is due to the slewing of C_C.

6.2.9 Dropout Characteristics

The dropout characteristics are contributed by primarily by Q_{P1} and Q_{P2}. The dropout voltage is the difference between the input voltage and the output voltage when the regulator begins functioning as a linear device, and regulated voltage is produced. When the regulator is not functioning as a linear device, the amplifier is saturated. This means that the voltage at the cathode and anode of D_L is clamped, positive. By choosing E^+ to be equal to V(8,1) = V_{IN} for this circuit, and by correct choice of V+, the voltage at the anode of D_L can be set approximately equal to V_{IN} during op-amp saturation. If $I_{RB1} \approx I_{LOAD}/BF$, $IC_{QP1} \approx I_{LOAD}/BF$ and $IC_{QP2} \approx I_{LOAD}$, which

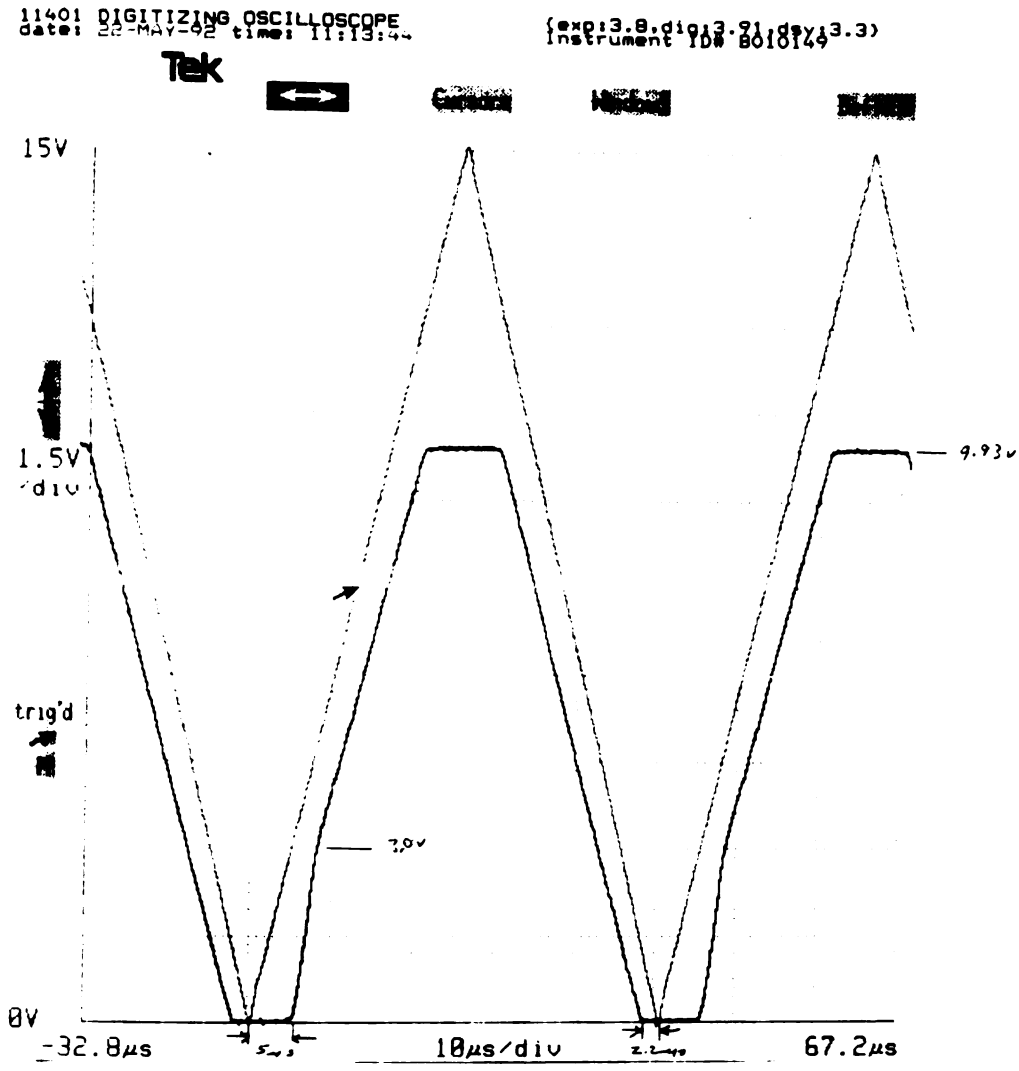

Figure 6.8 Power up and down, triangle wave, measured

neglects the current which biases R_1 and R_2, and Q_{P1} and Q_{P2} have equal BF, IS, and NF, then

$$VDO = \frac{I_{LOAD}}{BF^2}(R_{B1} + R_{B2}) + NF\,VT\ln\left(\frac{I_{LOAD}}{IS\,BF}\right) + NF\,VT\ln\left(\frac{I_{LOAD}}{IS}\right). \qquad (6.23)$$

The first term in Eqn. (6.23) can be neglected for small R_{B1} and R_{B2}, and Eqn. (6.23) can be simplified to

$$VDO \approx NF\,VT\ln\left(\frac{I_{LOAD}^2}{IS^2\,BF}\right). \qquad (6.24)$$

6.2.10 Line Transient Response

Line transient response is shown in Fig. (6.9). This is controlled primarily by the frequency dependent components in the voltage reference, especially C_R, R_{CR}, and R_{R2}. No closed form solution exists, so these components are chosen empirically to provide an adequate fit to the line transient response.

6.2.11 Ambient Temperature Sensing Circuitry

I_T, R_{T1}, R_{T2} are used to generate a voltage at node 10000 which is equal to the change in ambient temperature from the nominal temperature , ΔT. G_T, V_T and R_{T3}. provide the means to sense a current which has the value ΔT. This is identical to the temperature sensing circuitry inside the CA3085.

6.2.12 Other Modeled Characteristics

The prior characteristics are used in determining component selection. As a result of correct choice of parameters and topology the macromodel predicts other responses. These are: line and load regulation, and load transient response.

Figure 6.9 Line transient response, measured

6.3 DESIGN PROCEDURE FOR A UA723

Based on the equations and procedures shown in the last section, and design procedure will be developed in this section.

Basic to the design procedure is a list of measurements required to base the design on. The following measurements should be taken in the basic regulator circuit:

1) Measure V_{OUT} vs V_{IN} with no load.

2) Measure IQ vs V_{IN} with no load.

3) Measure V_{OUT} for V_{IN} = -15V, with no load.

4) Measure ripple rejection vs frequency with no load.

5) Take a load transient response measurement with a 150Ω load, to determine the ratio of the change in output voltage for no load and load steady state conditions. This determines R_{OUT}.

6) Select R_{SC} = 5.2Ω. Measure maximum output current at V_{IN} = 15V.

7) Measure dropout voltage with R_{LOAD} = 150Ω.

8) Take a power up and down with both triangle wave input and square wave input with R_{LOAD} = 150Ω.

9) Take a power up and down with both triangle wave input and square wave input with R_{LOAD} = 150Ω.

10) Measure R_{LOAD}, the external resistors R_1, R_2, R_3, and the compensation capacitor C_C. These measured values get used in all of the equations. Measure as well the capacitances of all capacitors and the series resistance of all capacitors at some representative frequency.

The component selection procedure is:

1) Select E_A.

2) Select the amplifier clamping circuitry, these values are:

V_+, V_-, E_+, R_O, and the diode parameters for D_+ and D_-.

3) Based on the V_{OUT} vs V_{IN} measurement, determine the input voltage required to begin to turn the circuit on, V_{ON}, then

$$BV_{DZ1} = V_{ON} \tag{6.25}$$

Select NBV_{DZ1}.

4) From the measured value of V_{OUT} at V_{IN} = 15V, and utilizing Eqn. (6.1),

$$V_{REF} = \frac{V_{OUT}}{\left(1 + \frac{R_2}{R_1}\right)}. \tag{6.26}$$

Select NBV_{DZR} and R_{ZR}.

5) Measure the slope of IQ vs V_{IN} for the quiescent current measurement. Then from Eqn. (6.11),

$$R_Q = \frac{\Delta V_{IN}}{\Delta I_Q}. \tag{6.27}$$

6) From the ripple rejection measurement, determine RR_{LF}. Then determine the small signal resistance of D_{ZR}, r_{DZR}. This is determined from a trial macromodel run with PSpice. Then from Eqn. (6.6),

$$R_{R1} = \left(RR_{LF}\frac{R_2}{R_1 + R_2}\right)R_Q - r_{DZR} \tag{6.28}$$

7) From the ripple rejection measurement, determine $P1_{RR}$, then from Eqn. (6.7),

$$L_R = \frac{R_{R1}}{Pl_{RR}}. \tag{6.29}$$

8) Based on the line transient response measurement, select C_R, R_{CR}, and R_{R2} empirically.

9) From the power up and down square wave measurement, measuring the response time and from Eqn. (6.22),

$$g_{q2} = C_C \frac{V_{OUT} + 1.4 - V_{REF}}{\Delta t\, V_{REF}}. \tag{6.30}$$

This will produce a close value. This value should then be iterated to produce a value based on both the power up and down triangle and square waves.

10) From the quiescent current vs input voltage measurement, determine the value of the quiescent current at the point where a steady value is achieved. The total quiescent current is the sum of the currents from G_{Q1} and G_{Q2}, using this fact and Eqn. (6.10),

$$a_1 = \frac{I_Q - I_{GB2}}{V_{REF}}. \tag{6.31}$$

11.) Set $C_{B1} = C_{B2}$ and $R_{B1} = R_{B2}$ and determine values for both of them.

12.) Select R_{B1} and R_{B2}.

13.) From the load regulation measurement, determine the value of R_{OUT}. Then, from Eqn. (6.17)

$$h_{LDR} = \frac{R_{OUT}}{1 + \frac{R_1}{R_2}}. \tag{6.32}$$

14) From the short circuit current measurement, find I_{MAX}. Select IS_{QL}. Then, from Eqn. (6.19)

$$NF_{QL} = \frac{I_{MAX} R_{SC}}{VT \ln\left(\frac{\beta_{Q2} V_{REF}}{IS_{QL}}\right)}. \tag{6.33}$$

15.) Select IS and BF for Q_{P1} and Q_{P2}. From the dropout voltage measurement and from Eqn. (6.23)

$$NF_{QP1,QP2} = \frac{VDO}{VT \ln\left(\frac{I_{LOAD}^2}{IS^2 \beta}\right)}. \tag{6.34}$$

16) Select the parameters for the diode D_{DIS}.

This concludes the design procedure. All of the parameters for the macromodel have been selected.

6.4 DESIGN EXAMPLE FOR A UA723

The design example is based on laboratory measurements is presented. The data, unless otherwise specified, is taken directly off from the plots which were shown previously in the document.

The nominal 150Ω load resistor was measured at 150.94Ω. R_1 was measured at 2.4184Ω, R_2 at 5.7375kΩ and R_3 at 1616Ω. The compensation capacitor had a measured value of 153.98pF and a negligible series resistance. Finally R_{SC} was

measured at 5.2062Ω.

1) Set $E_1 = 600$.

2) Let the diodes D^+ and D_- be the Pspice default diodes. Set $V_+ = -1.6V$, $V^- = 1V$. Set the gain of $E_+ = 1$ and let V(8,1) be the controlling voltage. If the diode voltage drops are approximated at 0.8V, the maximum voltage at node 17, for node 5 grounded, is approximately V_{IN}. The minimum voltage for the amplifier is 0.2V.

3) Based on the V_{OUT} vs V_{IN} measurement, set $BV_{DZ1} = 1V$. Set $NBV_{DZ1} = 0.001$.

4) From the measured value of V_{OUT} at $V_{IN} = 15V$, set $BV_{DZR} = 6.904V$. Set $NBV_{DZR} = 0.001$ and $R_{ZR} = 1MEG\Omega$.

5) From the IQ vs V_{IN} measurement, $R_Q = 237.273k\Omega$.

6) From the ripple rejection measurement, $RR_{LF} = 63.694db = 0.6536m$. r_{DZR} was determined to be 8.9Ω, as was r_{DZ1}. This gives $R_R = 100.1936\Omega$.

7) $P1_{RR}$ was determined to be 14kHz, then $L_R = 1.1390mH$.

8) Based on the line transient response measurements, the following components were selected: $R_{CR} = 10\Omega$, $R_{R2} = 15000\Omega$, and $C_R = 3pF$.

9) Base on the power up and down square wave measurement, Δt as 4.4us. This gave a value of 0.0224m for g_{Q2}, however the value 0.08m worked much better for the power up and down responses.

10) IQ was measured at 2.5244mA, then $a_1 = 0.28325m$.

11) Set $C_{B1} = C_{B2} = 1pF$. Set $R_{BC1} = R_{BC2} = 10\Omega$.

12) Set $R_{B1} = 10\Omega$ and $R_{B2} = 10\Omega$.

13) From the load regulation measurements, $R_{OUT} = 50m\Omega$. Then $h_{LDR} =$

35.2m.

14) I_{MAX} at 15V was determined to be 258.3mA. Set IS_{QL} = 1e-20A. Then NF_{QL} = 1.3466.

15) Set $IS_{QP1, QP2}$ = 1e-20. Set $BF_{QP1, QP2}$ = 50. VDO = 2.08V, then $N_{QP1, QP2}$ = 1.0188.

16) Let the diode D_{DIS} be the Pspice default diode.

17) Set R_{IN} = 100kΩ.

This concludes the design example. All of the parameters for the macromodel have been selected.

6.5 MODELING THE UA723 AT -55 AND 125 DEGREES

6.5.1 Strategy in Modeling the UA723 Temperature Variations

The room temperature model is developed first. The steps which need modifications are steps 3, 4, 5, 6, 7, 10, 11, 13, and 14. These will give rise to new values for BV_{DZ1}, BV_{DZR}, R_Q, R_{R1}, and L_R. This will also be used to find the coefficients of the polynomials which describe h_{LDR}, E_L, and g_{Q1}. For further ease, the parameters XTI = 0 and EG = 0eV have been set for Q_L. This makes the value of IS for Q_L relatively constant over the temperature range of interest.

To solve for the value of E_L, Eqn. (6.20) is modified for temperatures other than the nominal temperature as

$$I_{MAX}R_{SC} + V_{EL} \approx NF\,V_T \ln\left(\frac{g_{Q1}V_{REF}}{IS_{QL}}\right). \qquad (6.35)$$

6.5.2 Design Example to Include Temperature Dependance

In this section the parameters for the model for -55°C and 125°C are developed.

The temperature coefficients are determined and then inserted into the room temperature model. This will represent the fully developed, macromodel for the UA723.

Following the example in section 4 for -55 degrees:

3) Based on the V_{OUT} vs V_{IN} measurement, set BV_{Z1} = 1V.

4) From the measured value of V_{OUT} at V_{IN} = 9.823V, set BV_{ZR} = 6.9103V.

5) From the IQ vs V_{IN} measurement, R_Q = 196.569kΩ.

6) From the ripple rejection measurement, RR_{LF} = 68.7967db = 0.3632m. r_{DZR} was determined to be 5.24Ω. This gives R_R = 44.9840Ω.

7) $P1_{RR}$ was determined to be 14khz, then L_R = .5507mH.

10) I_Q was measured at 2.6283mA, then g_{Q1}(-55°C) = 0.3003m.

13) From the load regulation measurements, R_{OUT} = 137.6mΩ. Then h_{LDR} = 0.0968.

14) I_{MAX} at 15V was determined to be 152.4mA. Solving Eqn. (6.35) for E_L yields E_L(-55°C) = -.1825V.

Following the example in section 4 for 125 degrees:

3) Based on the V_{OUT} vs V_{IN}, set BV_{DZ1} = 1V.

4) From the measured value of V_{OUT} at V_{IN} = 9.92V, set BV_{DZR} = 6.9785V.

5) From the IQ vs V_{IN} measurement, R_Q = 318.543kΩ.

6) From the ripple rejection measurement, RR_{LF} = 62.11db = 0.7843m. r_{DZR} was determined to be 15.7Ω. This gives R_R = 160.0533Ω

7) $P1_{RR}$ was determined to be 11kHz, then L_R = 2.3158mH.

10) I_Q was measured at 2.3625mA, then g_{Q1}(125°C) = 0.2585m.

13) From the load regulation measurements, R_{OUT} = 171.9mΩ. Then h_{LDR}

= 0.1209.

14) I_{SC} at 15V was determined to be 169mA. Solving Eqn. (6.35) for E_L yields $E_L(125°C)$ = -.9012V.

A final summary of the temperature dependent parameters and elements follows.

element or **parameter**	**value** at **25 degrees**	**value** at **-55 degrees**	**value** at **125 degrees**
BV_{DZ1}	1	1	1
BV_{DZR}	6.9504	6.9103	6.9785
R_Q	237.273k	196.569k	318.543k
R_{R1}	100.1936	44.9840	160.0533
L_R	1.1390m	.5507m	2.3158m
g_{Q1}	.2832m	.3003m	.2585m
h_{LDR}	35.2m	0.0968	.1209
E_L	0	-.1825	-.9012

Table 6.1 Temperature dependent components and parameters

Solving for the linear and quadratic coefficients for each of these components and parameters to the following results for Table 6.2

element or **parameter**	**TC1** or **TBV1** (linear coeff.)	**TC2** or **TBV2** (quadratic coeff.)
BV_{DZ1}	0	0
BV_{DZR}	5.8034e-05	-1.7605e-07
R_Q	2.7132e-03	6.8655e-06
R_{R1}	6.4819e-03	-5.0748e-06
L_R	8.1788e-03	2.1531e-05
g_{Q1}	-2.2853e-07	-1.8472e-10
h_{LDR}	-4.6889e-05	9.0389e-06
E_L	-2.7380e-3	-6.2740e-5

Table 6.2 Temperature coefficients

The final macromodel is shown in follows. The macromodel includes the effects of temperature.

```
.SUBCKT UA723   1   2   3   4   5   6   7   8   9   10
*               |   |   |   |   |   |   |   |   |   |
*              CS   |   |   |   |   |   |   |   |   |
*                  IN-  |   |   |   |   |   |   |   |
*                      IN-  |   |   |   |   |   |   |
*                         VREF  |   |   |   |   |   |
*                               V-  |   |   |   |   |
*                                  VOUT |   |   |   |
*                                      VC   |   |   |
*                                           V+  |   |
*                                               FC  |
*                                                   CL
*
DZ1     13 8 DZ1
.MODEL DZ1 D (BV=1 NBV=0.001)
RQ      40 13 237.273K TC=2.7132E-3, 6.8655E-6
DZR     11 40 DZR
.MODEL DZR D (BV=6.9504 TBV1=5.8034E-5 TBV2=-1.7605E-7 NBV=0.01 CJO=1P)
RZR     11 40 1MEG
RR1     11 500 100.1936 TC=6.4819E-3,-5.0748E-6
LR      500 5 LR 1.1390M
.MODEL LR IND (TC1=8.1788E-3 TC2=2.1531E-5)
```

```
RR2     500 5 15000
CR      11 1000 3P
RCR     1000 5 10
GQ1     8 4 POLY (2) (4,5) (10000,0) 0 .2832M 0 0 -2.2853E-7 0 0 0 -1.8472E-10
ER      4 5 40 5 1
RIN     2 3000 100K
HLDR    3 3000 POLY (2) VLDR VT  0 35.2M 0 0 -4.6889E-5 0 0 0 9.03892E-6
GQ2     8 17 4 5 .08M
DB      17 19 DB
.MODEL DB D
RO      19 14 500
EA      14 5 3000 2 600
D-      22 19 DC
V-      22 5 DC 1
E+      23 5 8 5 1
D+      19 20 DC
V+      20 23 DC -1.6
.MODEL DC D
RT1     10000 10001 100.00001 TC=0.01
RT2     10001 0 -100
IT      0 10000 DC 1
GT      0 30000 10000 0 1
VT      30000 30001 DC 0
RT3     30001 0 1
RB1     17 9 10
RB2     9 21 10
QP1     8 21 16 QPASS1
QP2     7 16 15 QPASS2
.MODEL QPASS1 NPN (BF=50 VAF=50 NF=1.0188 IS=1E-20)
.MODEL QPASS2 NPN (BF=50 VAF=50 NF=1.0188 IS=1E-20)
CBC1    21 800 1P
RCBC1   800 8 10
CBC2    7 160 1P
RCBC2   160 16 10
VLDR    15 6 DC 0
QL      9 125 1 QLIMIT
.MODEL QLIMIT NPN (IS=1E-20 EG=0 XTI=0 NF=1.3466)
ESC     10 125 POLY (1) (10000,0) 0 -0.002738 -6.274E-5
DDIS1   15 8 DDIS
.MODEL DDIS D
.ENDS UA723
```

6.5.3 Comparison of Macromodel Predictions with Lab Results

A comparison of macromodel predictions with lab results are presented in this section.

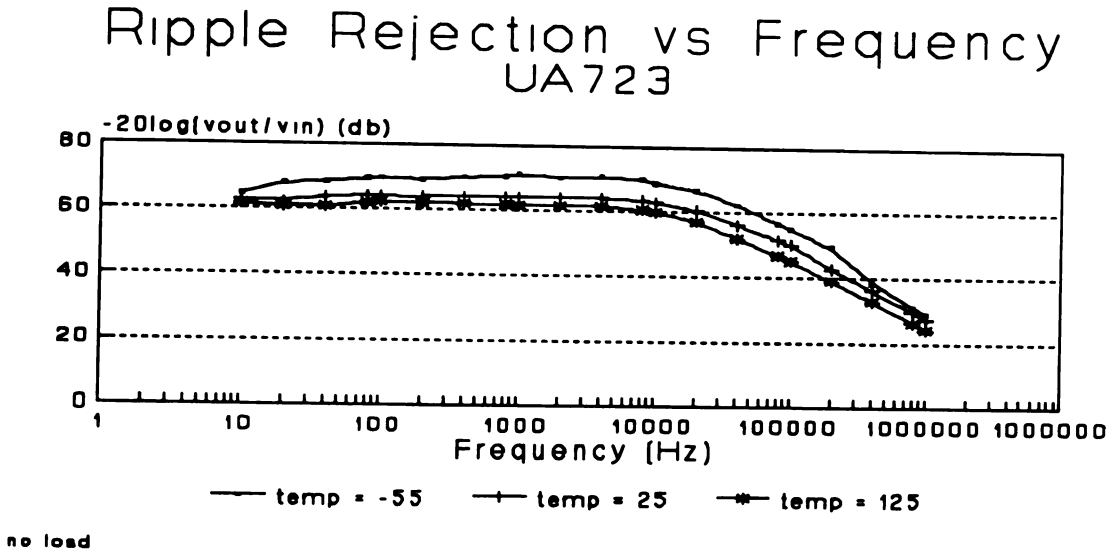

Figure 6.10 Ripple rejection vs frequency, measured

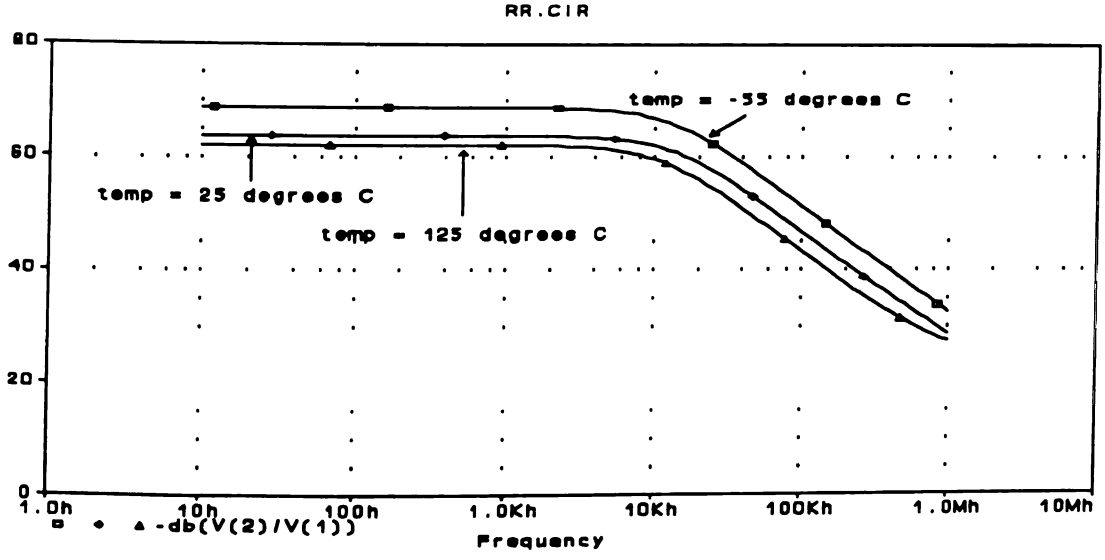

Figure 6.11 Ripple rejection vs frequency, macromodel

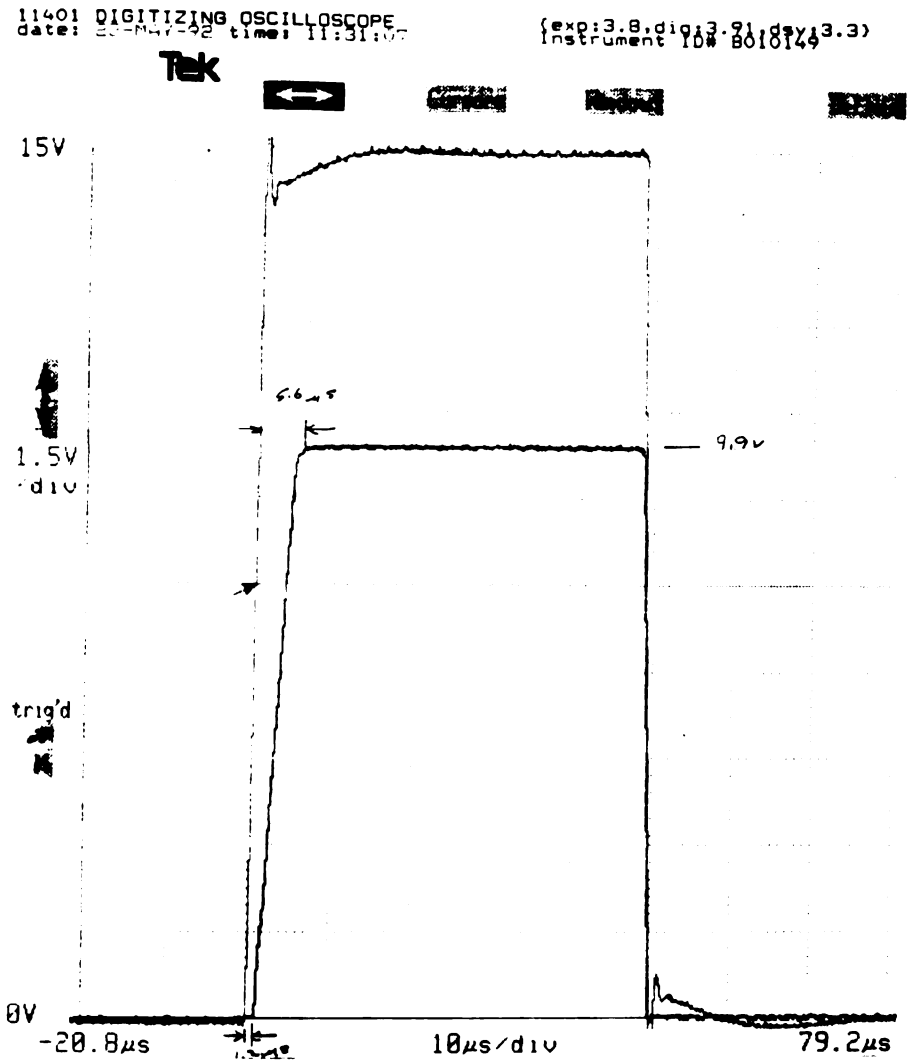

Figure 6.12 Power up and down, square wave, measured

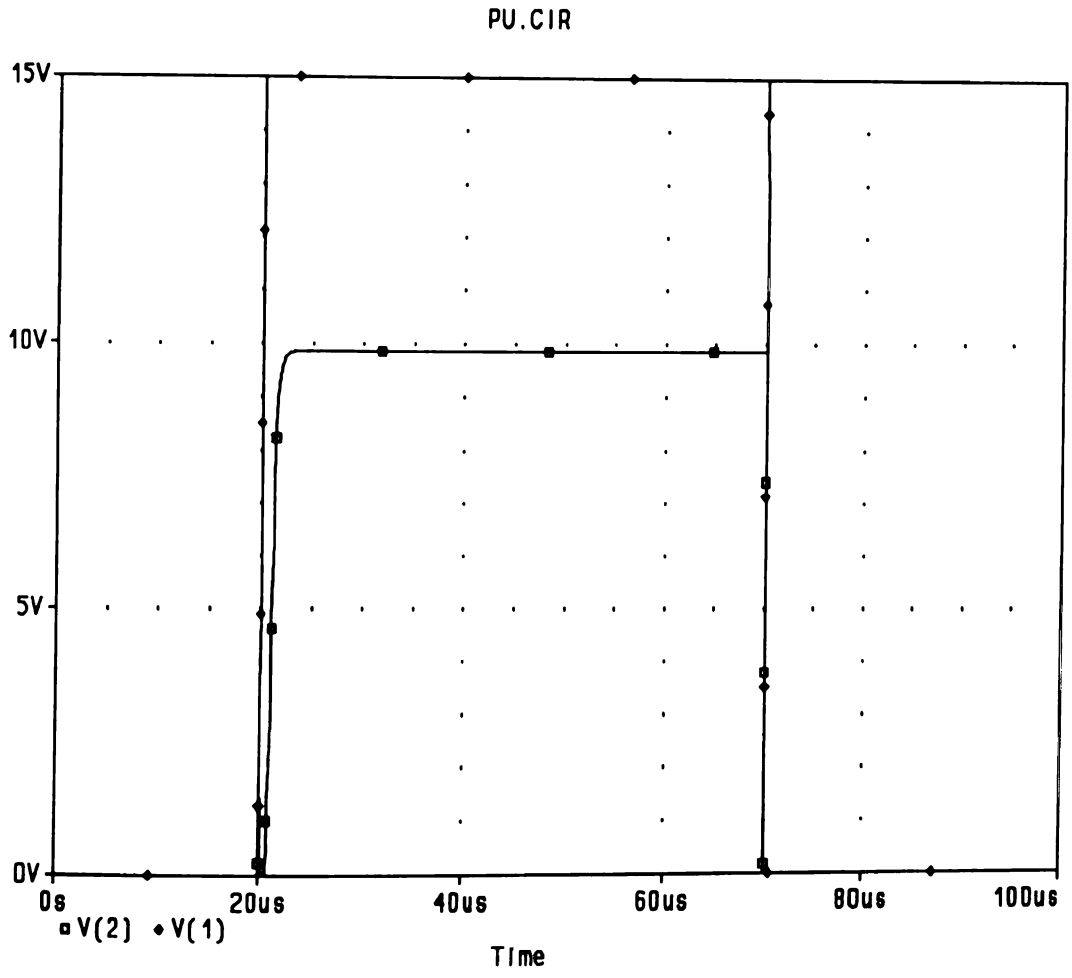

Figure 6.13 Power up and down, square wave, macromodel

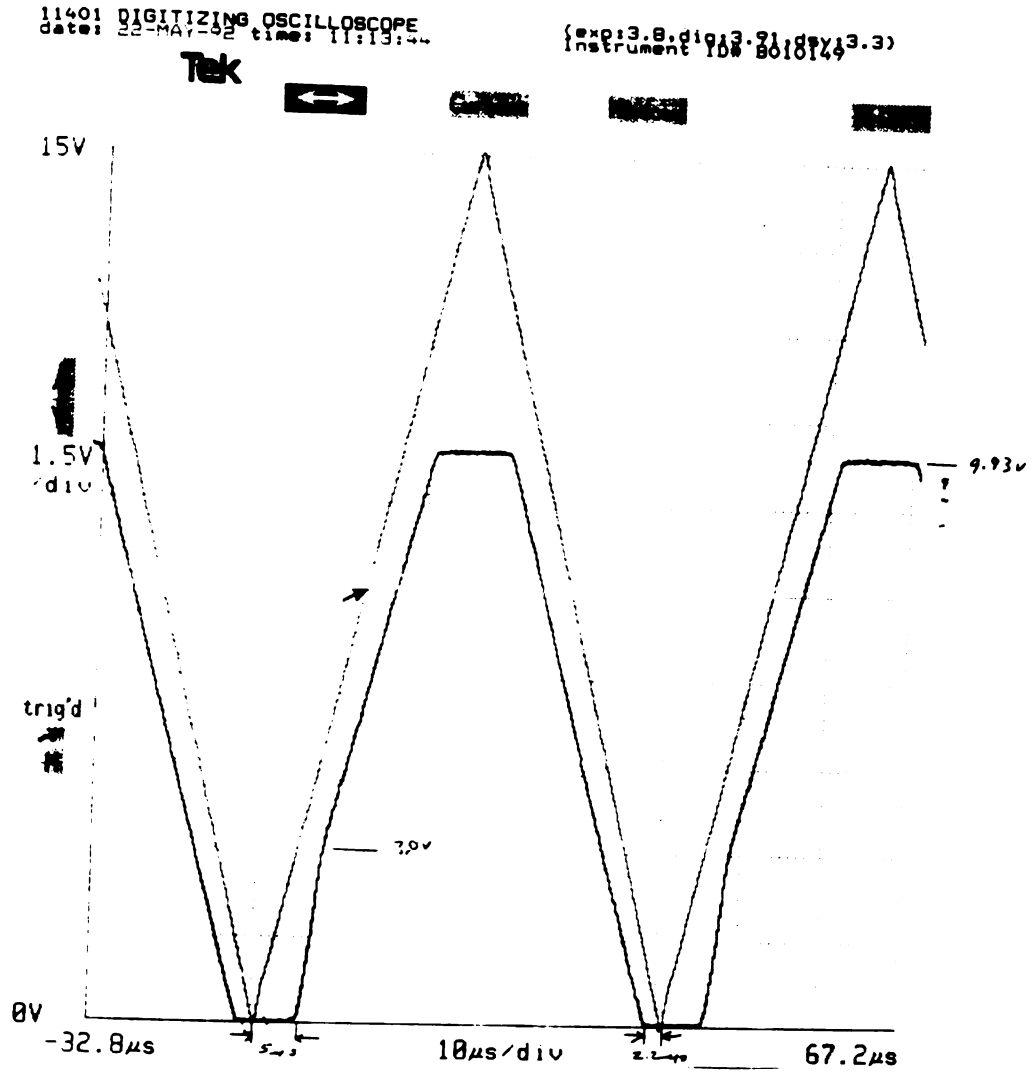

Figure 6.14 Power up and down, triangle wave, measured

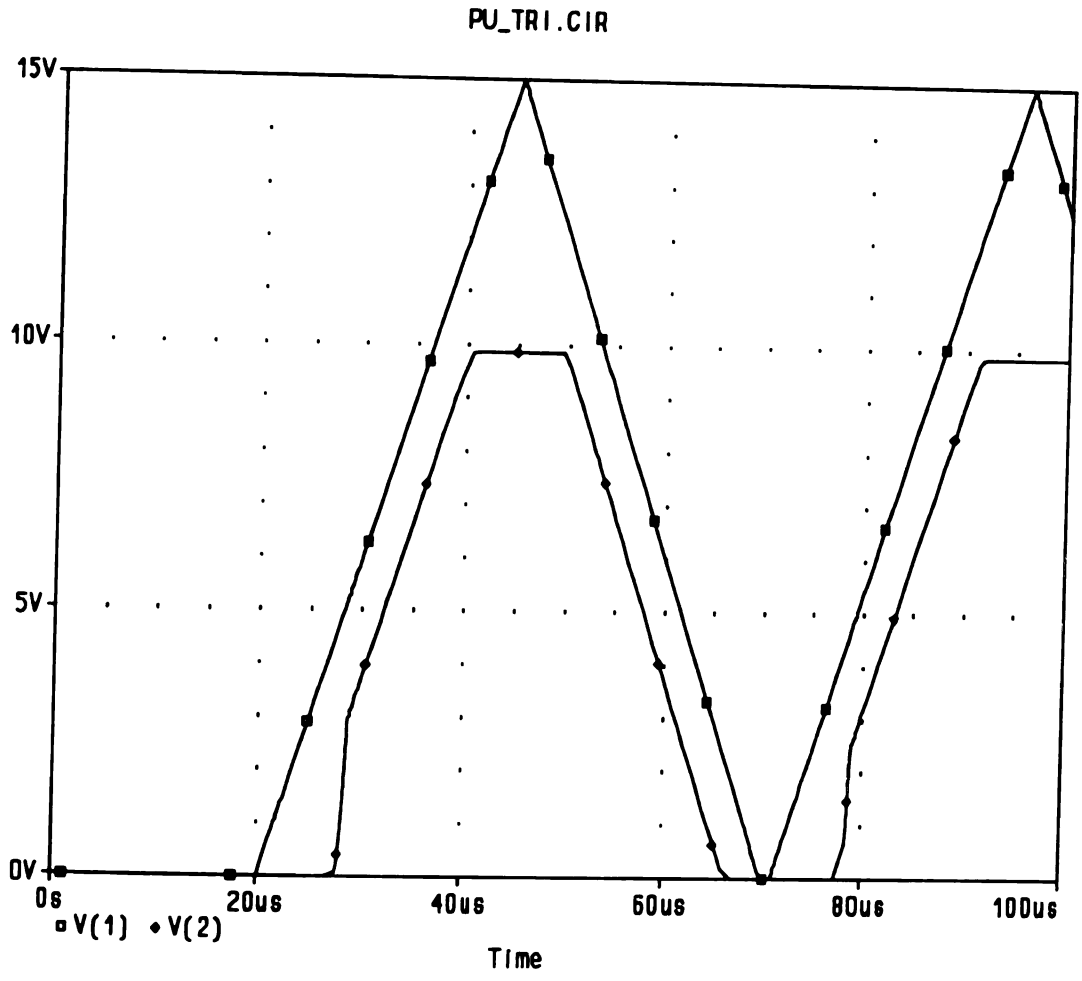

Figure 6.15 Power up and down, triangle wave, macromodel

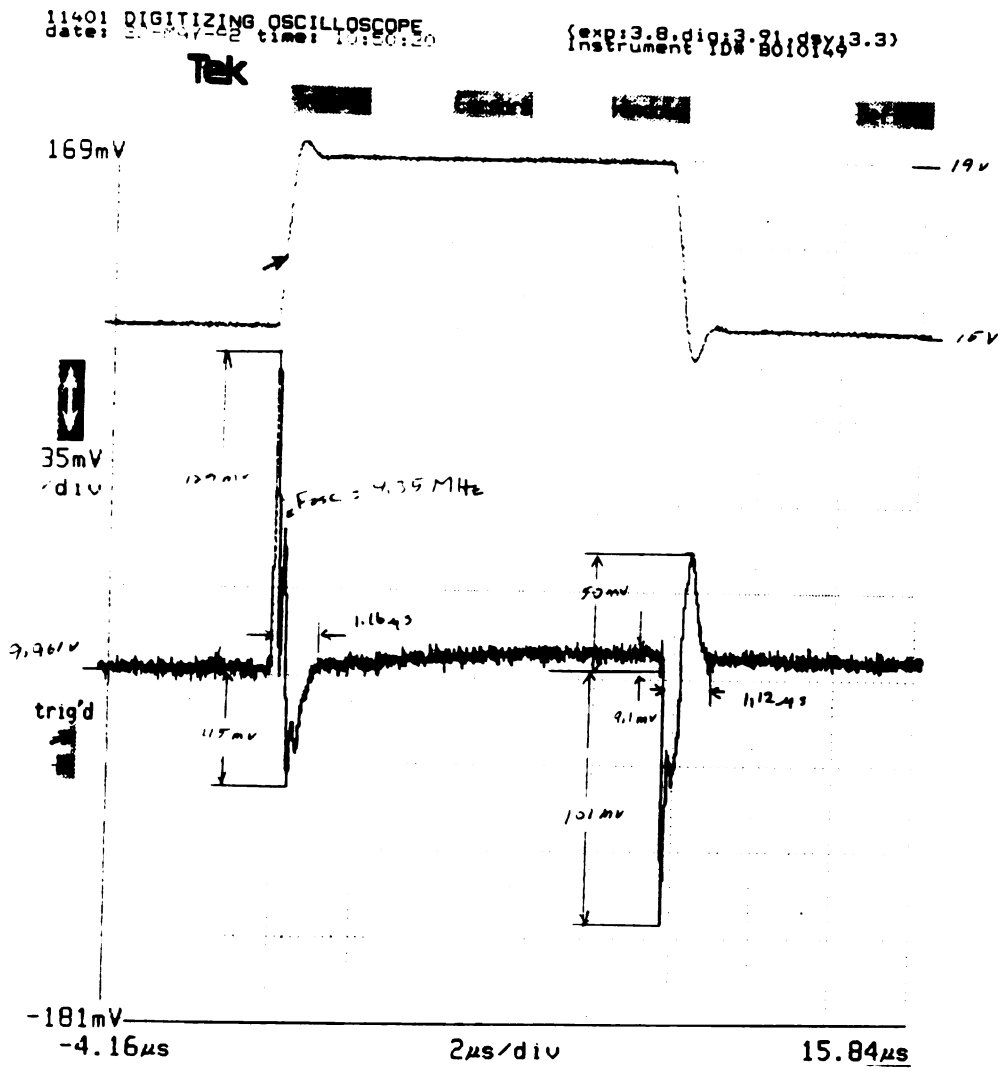

Figure 6.16 Line transient response, measured

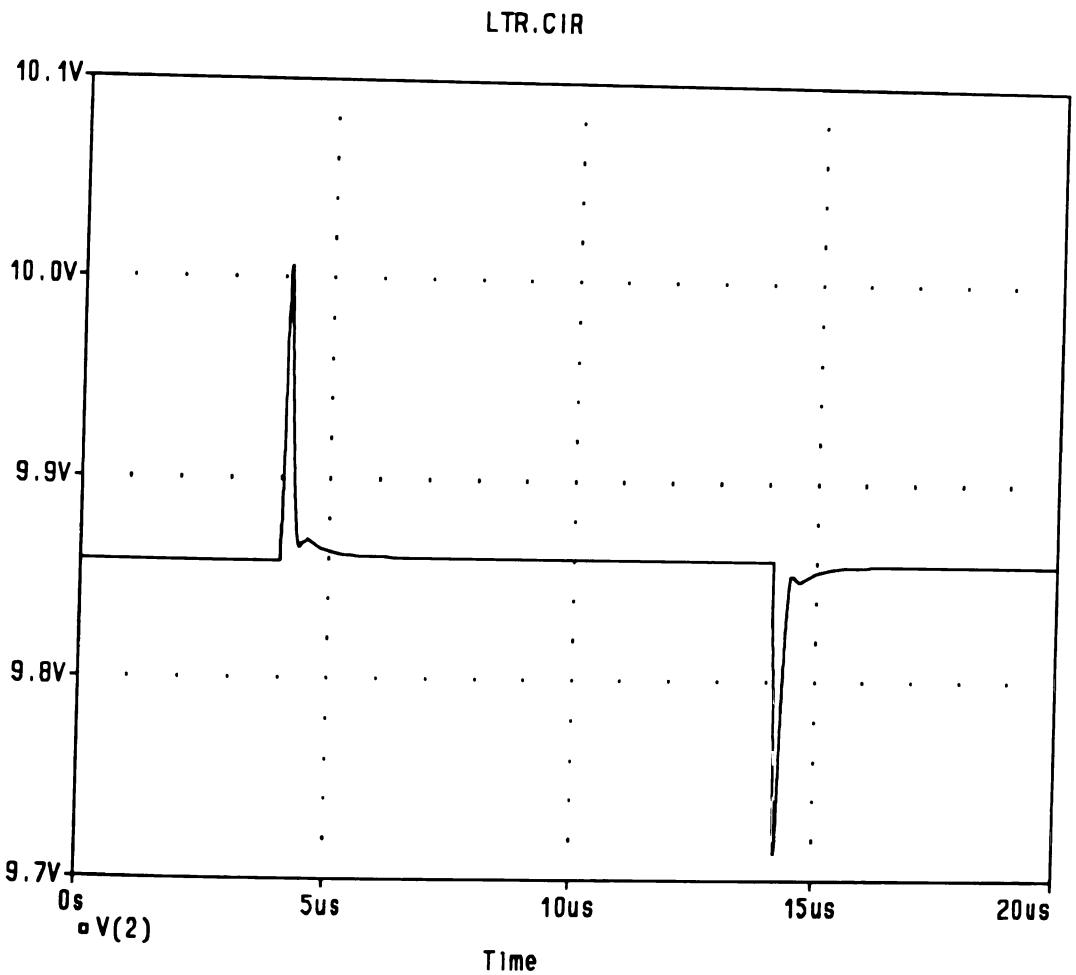

Figure 6.17 Line transient response, macromodel

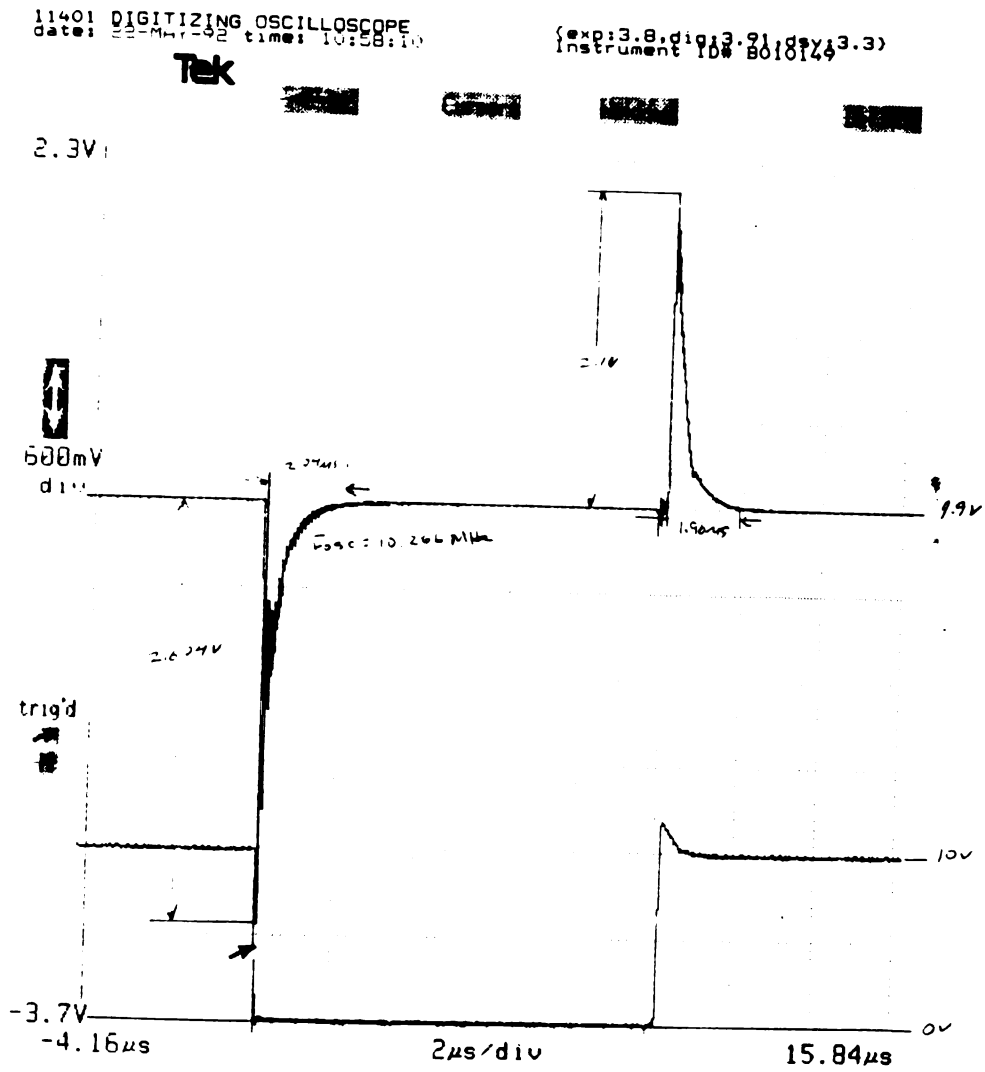

Figure 6.18 Load transient response, measured

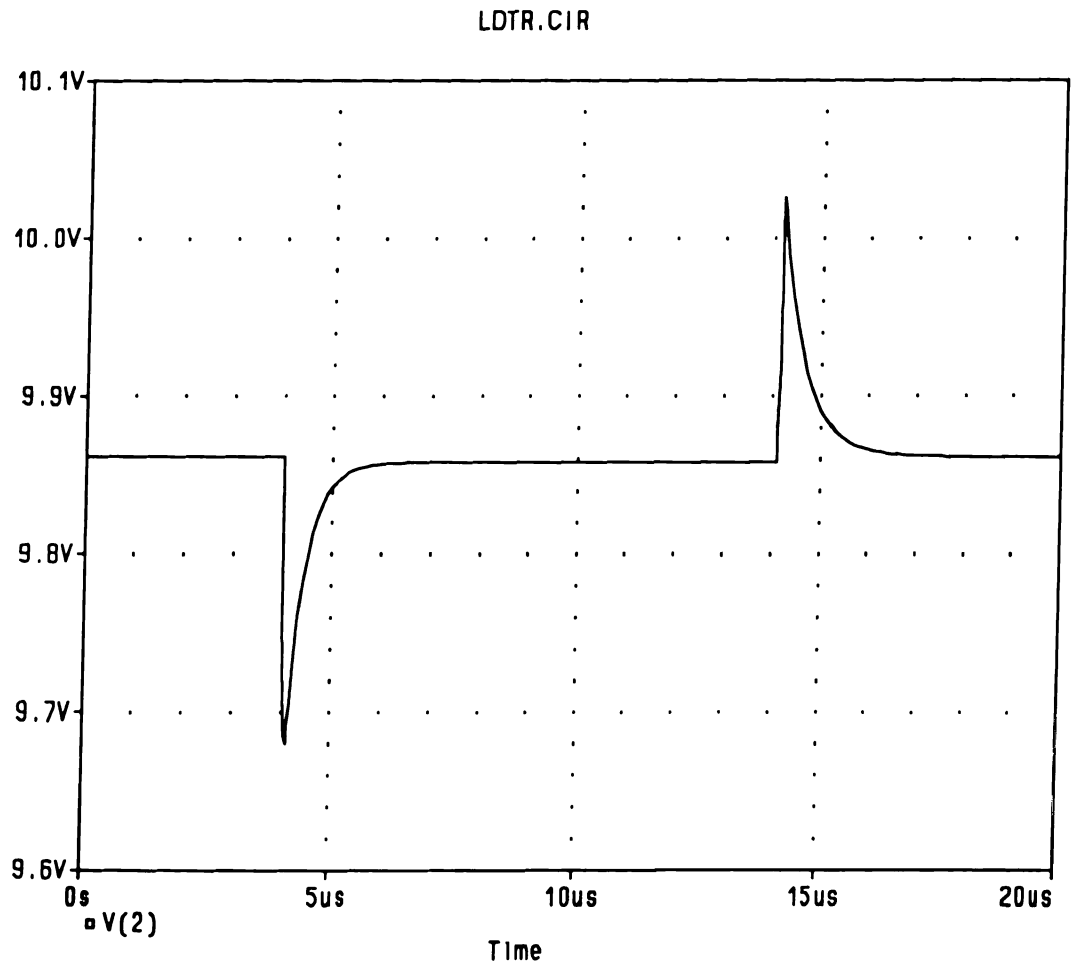

Figure 6.19 Load transient response, macromodel

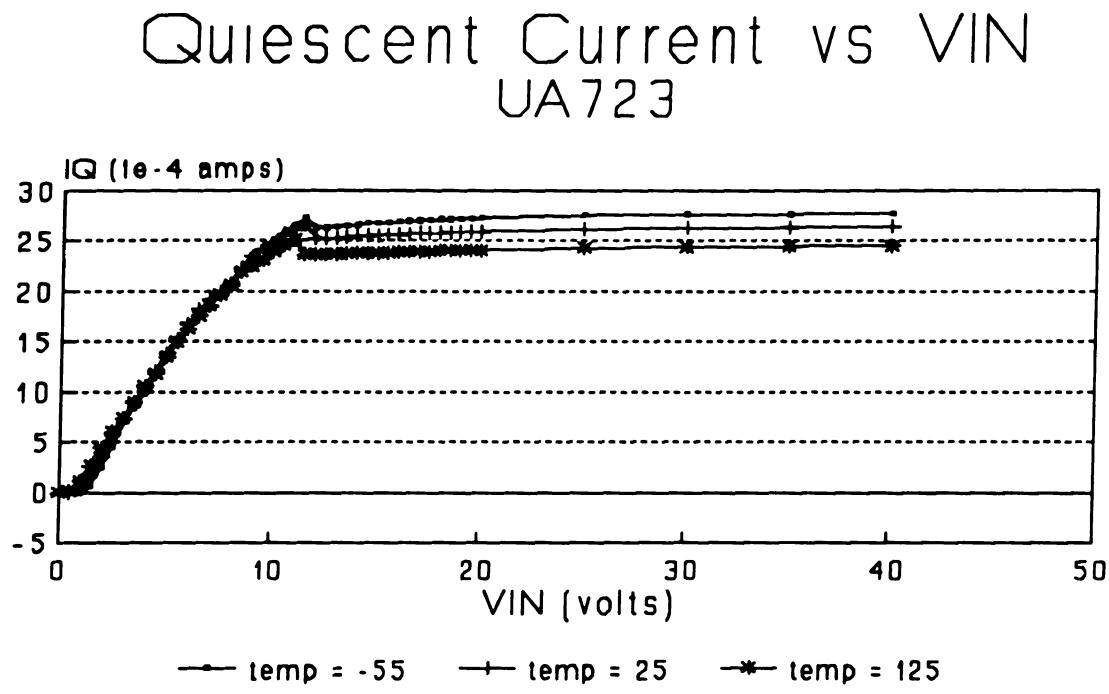

Figure 6.20 Quiescent current vs input voltage, measured

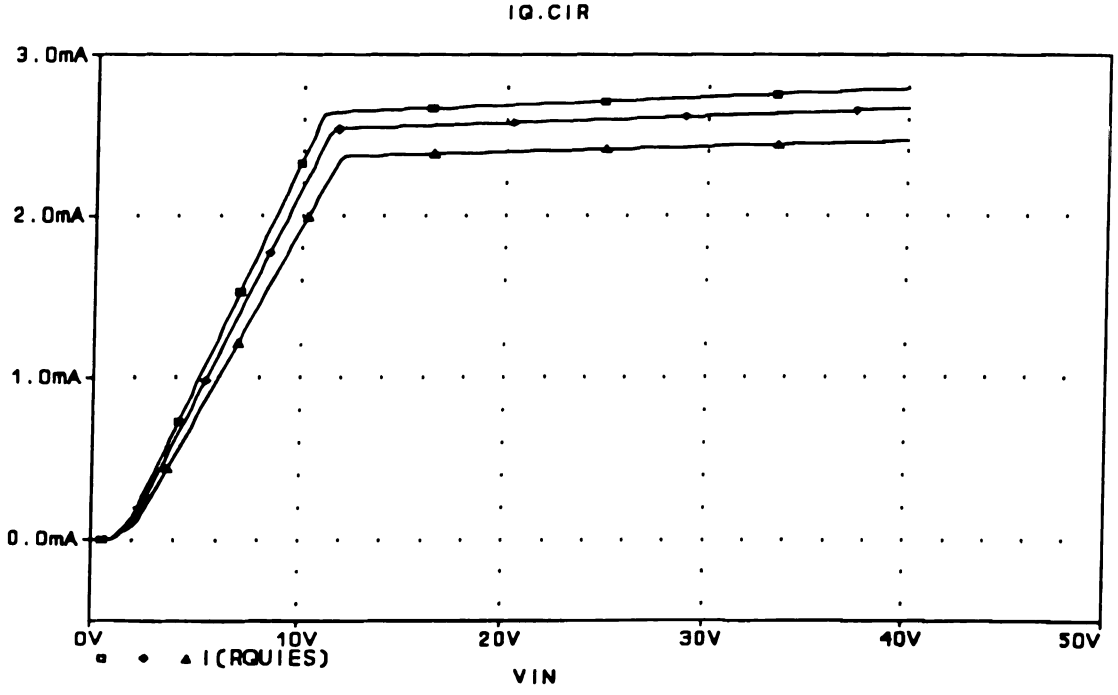

Figure 6.21 Quiescent current vs input voltage, macromodel

Comparison of Macromodel parameters and Measured Parameters				
QUANTITY		**-55°C**	**25°C**	**125°C**
RR_{LF}	lab	68.767db	63.694db	62.110db
	model	68.744db	63.687db	62.069db
$P1_{RR}$	lab	14kHz	14kHz	11kHz
	model	13.55kHz	14.16kHz	11.38kz
IQ	lab	2.628mA	2.524mA	2.363mA
	model	2.628mA	2.526mA	2.360mA
ΔIQ/ΔVin	lab	5.087u	4.215u	3.139u
	model	5.195u	4.381u	3.331u
max load current	lab	152.4mA	252.9mA	169mA
	model	157.8mA	258.3mA	154.3mA
dropout voltage	lab	2.68V	2.08V	2.36V
	model	2.20V	2.37V	2.56V
$\Delta V_{OUT}/\Delta I_{LOAD}$	lab	.138Ω	.05Ω	.172mΩ
	model	.146Ω	.059Ω	.182Ω

Table 6.3 Macromodel comparisons with lab data

6.6 TEST CIRCUITS

6.6.1 Basic Pspice Test Circuits

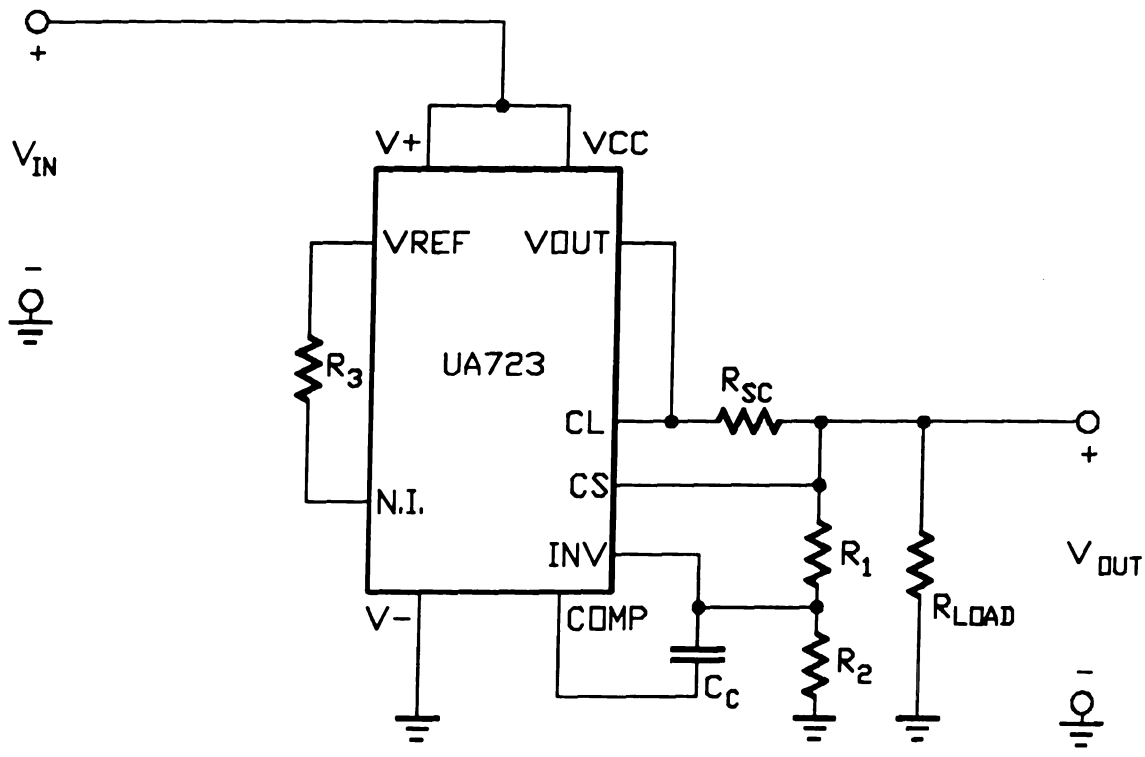

Figure 6.22 Basic pspice test circuit

```
RR.CIR
*
*RIPPLE REJECTION CHARACTERISTICS FOR THE UA723, HIGH VOLTAGE
*APPLICATION
VIN     8 0 DC 15
VAC     1 8 AC 1
R1      2 3 2.4184K
R2      3 0 5.7375K
R3      4 5 1616
CC      6 3 153.98P
*pins   1 2 3 4 5 6 7 8 9 10
XREG    2 3 5 4 0 2 1 1 6 2 UA723
.OPTIONS ITL1=300 ITL2=300 TNOM=25
.TEMP -55 25 125
.OP
.LIB UA723.LIB
.PROBE
.AC DEC 20 10 1MEG
.END
```

```
PU.CIR
*
*POWER UP, SQUARE WAVE, FOR THE UA723, HIGH VOLTAGE APPLICATION
*
VP      1 0 PULSE (0 15 20U 0 0 50U)
R1      2 3 2.4184K
R2      3 0 5.7375K
R3      4 5 1616
CC      6 3 153.98P
RLOAD   2 0 150.94
*pins   1 2 3 4 5 6 7 8 9 10
XREG    2 3 5 4 0 2 1 1 6 2 UA723
.OPTIONS ITL1=300 ITL2=300 TNOM = 25
.OP
.TEMP 25
.LIB UA723.LIB
.PROBE
.TRAN .1U 100U 0 .1U
.END
```

```
LTR.CIR
*
*LINE TRANSIENT RESPONSE FOR THE UA723, HIGH VOLTAGE APPLICATION
*
VIN     8 0 DC 15
VP      1 8 PULSE (0 4 4U 0 0 10U)
R1      2 3 2.4184K
R2      3 0 5.7375K
R3      4 5 1616
CC      6 3 153.98P
RLOAD   2 0 150.94
*pin    1 2 3 4 5 6 7 8 9 10
XREG    2 3 5 4 0 2 1 1 6 2 UA723
.OPTIONS ITL1=300 ITL2=300 TNOM=25
.OP
.TEMP 25
.LIB UA723.LIB
.PROBE
.TRAN .1U 20U 0 .1U
.END
```

```
LDTR.CIR
*
*LOAD TRANSIENT RESPONSE FOR THE UA723, HIGH VOLTAGE
APPLICATION
*
VIN     1 0 DC 15
R1      2 3 2.4184K
R2      3 0 5.7375K
R3      4 5 1616
CC      6 3 153.98P
RLOAD   2 10 150.94
VP      10 0 PULSE (9.9 0 4U 0 0 10U)
*pin    1 2 3 4 5 6 7 8 9 10
XREG    2 3 5 4 0 2 1 1 6 2 UA723
.OPTIONS ITL1=300 ITL2=300 TNOM=25
.OP
.LIB UA723.LIB
.TEMP = 25
.PROBE
.TRAN .1U 20U 0 .1U
.END
```

```
IQ.CIR
*
*QUIESCENT CURRENT CHARACTERISTICS FOR THE UA723, HIGH VOLTAGE
APPLICATION
*
VIN     1 0 DC 15
R1      2 3 2.4184K
R2      3 0 5.7375K
R3      4 5 1616
CC      6 3 153.98P
RQUIES  7 0 100.072
*pin    1 2 3 4 5 6 7 8 9 10
XREG    2 3 5 4 7 2 1 1 6 2 UA723
.OPTIONS ITL1=300 ITL2=300 TNOM=25
.TEMP -55 25 125
.OP
.LIB UA723.LIB
.PROBE
.DC VIN 0 40 0.25
.END
```

```
DROPOUT.CIR
*
*DROPOUT CHARACTERISTICS FOR THE UA723, HIGH VOLTAGE
APPLICATION
*
VIN     1 0 DC 15
R1      2 3 2.4184K
R2      3 0 5.7375K
R3      4 5 1616
CC      6 3 153.98P
RLOAD   2 0 150.94
*pins   1 2 3 4 5 6 7 8 9 10
XREG    2 3 5 4 0 2 1 1 6 2 UA723
.OPTIONS ITL1=300 ITL2=300 TNOM=25
.TEMP -55 25 125
.OP
.LIB UA723.LIB
.PROBE
.DC VIN 0 20 0.1
.END
```

```
CL.CIR
*
*CURRENT LIMITING CHARACTERISTICS FOR THE UA723, HIGH VOLTAGE
APPLICATION
*
VIN     1 0 DC 15
R1      2 3 2.4184K
R2      3 0 5.7375K
R3      4 5 1616
CC      6 3 153.98P
RSC     8 2 5.2062
RLOAD   2 0 5.5762
*pin    1 2 3 4 5 6 7 8 9 10
XREG    2 3 5 4 0  8 1 1 6 8 UA723
.OPTIONS ITL1=300 ITL2=300 TNOM=25
.OP
.LIB UA723.LIB
.PROBE
.TEMP -55 25 125
.DC VIN 0 40 0.25
.END
```

6.6.2 Measurement Test Circuits

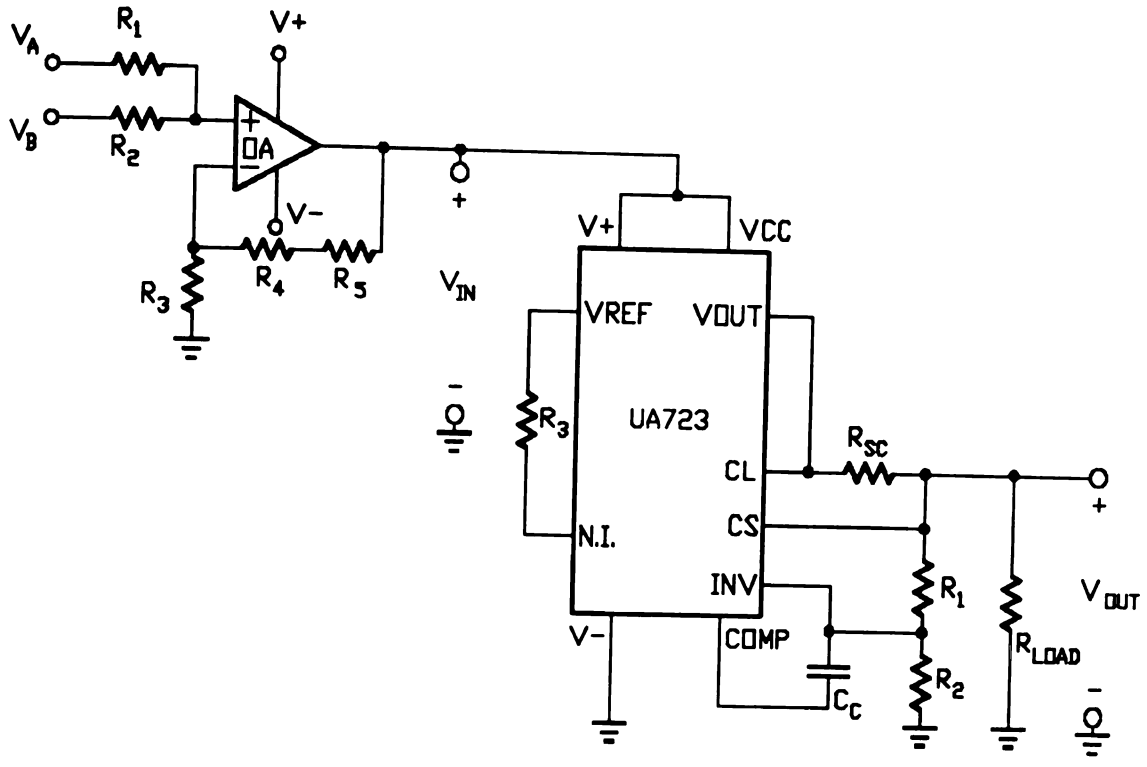

Figure 6.23 Test circuit No. 1

The conditions of test circuit No. 1 are stated.

R_1 measured 2.4184kΩ.
R_2 measured 5.7375kΩ.
R_3 measured 1.616kΩ
R_{SC} measured 5.2062Ω.
R_{LOAD} measured 150.94Ω.
C_C measured 153.98pF at 100kHz and had a negligible series resistance.
R_1, R_2, R_3, R_4, and R_5 have nominal values of 1kΩ.
V+ is a positive 50V dc power supply.
V- is a negative 10V dc power supply.
OA is a Burr-Brown OPA541 Op-Amp.
The UA723 resides inside a temperature chamber. Wires are connected at the terminals of the UA723 to allow it to be connected outside the chamber to the test circuit.

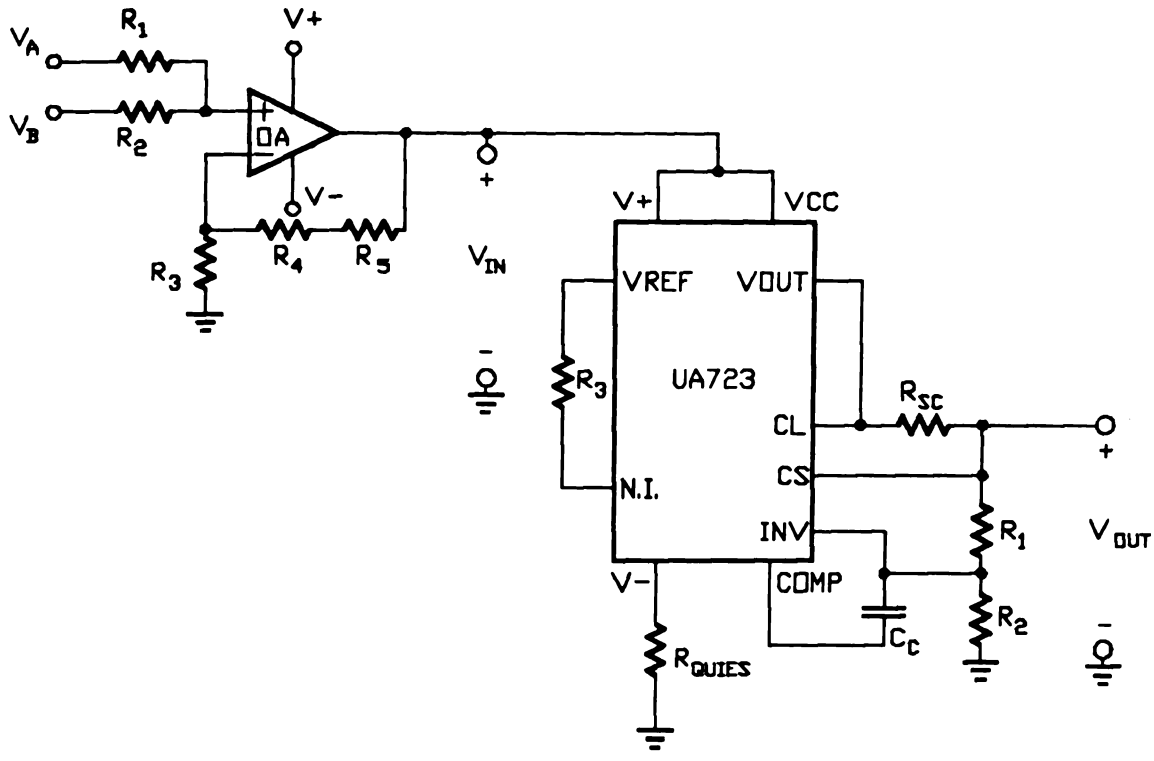

Figure 6.24 Test circuit No. 2

The conditions of test circuit No. 2 are stated.

R_1 measured 2.4184kΩ.
R_2 measured 5.7375kΩ.
R_3 measured 1.616kΩ
R_{SC} measured 5.2062Ω.
R_{QUIES} measured 100.072Ω.
C_C measured 153.98pF at 100kHz and had a negligible series resistance.
R_1, R_2, R_3, R_4, and R_5 have nominal values of 1kΩ.
V+ is a positive 50V dc power supply.
V- is a negative 10V dc power supply.
OA is a Burr-Brown OPA541 Op-Amp.
The UA723 resides inside a temperature chamber. Wires are connected at the terminals of the UA723 to allow it to be connected outside the chamber to the test circuit.

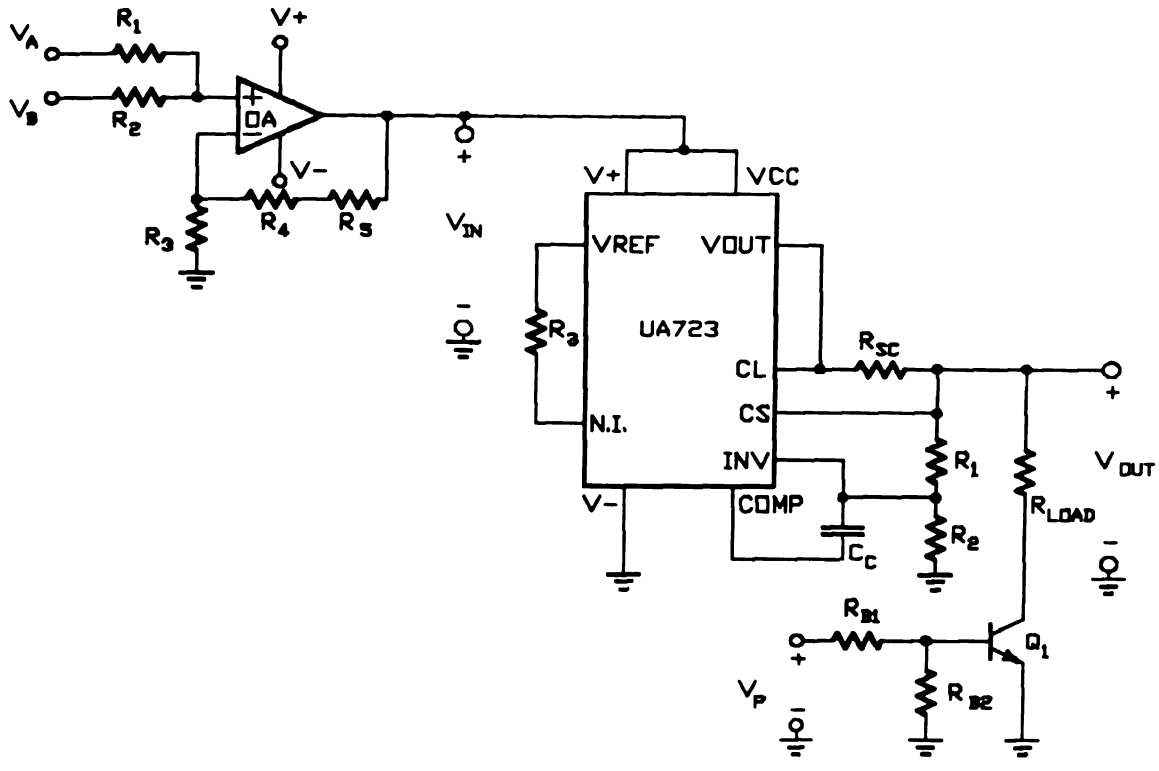

Figure 6.25 Test circuit No. 3

The conditions of test circuit No. 3 are stated.

R_1 measured 2.4184kΩ.
R_2 measured 5.7375kΩ.
R_3 measured 1.616kΩ
R_{SC} measured 5.2062Ω.
R_{LOAD} measured 150.94Ω.
C_C measured 150.94pF at 100kHz and had a negligible series resistance.
R_1, R_2, R_3, R_4, and R_5 have nominal values of 1kΩ.
V+ is a positive 50V dc power supply.
V- is a negative 10V dc power supply.
OA is a Burr-Brown OPA541 Op-Amp.
The UA723 resides inside a temperature chamber. Wires are connected at the terminals of the UA723 to allow it to be connected outside the chamber to the test circuit.
Q_1 is a 2N4401 npn transistor.
R_{B1} has a nominal value of 10kΩ.
R_{B2} has a nominal value of 1kΩ.

1) Ripple Rejection was done using test circuit 1. V_A was connected to an ac function generator. V_B was connected to a positive dc power supply. These were set to produce a 15V dc voltage at V_{IN} with a sine wave superimposed for both. Voltages and phases were measured with a Tektronix 11401 scope.

2) The V_{IN} vs V_{OUT} and V_{OUT} at V_{IN} = 15V for the UA723 was done using test circuit 1. V_A was connected to an pulse generator and pulsed at 100Hz, with a duty cycle of 5%. V_B was grounded. These were set to produce the necessary voltage at V_{IN}. Voltages were measured with a Tektronix 11401 scope.

3) The power up and down square wave measurements were done using test circuit 1. V_A was connected to an pulse generator. V_B was grounded. Voltages were measured with a Tektronix 11401 scope.

4) The power up and down triangle measurements was done using test circuit 1. V_A was connected to an ac function generator, generating a triangle wave. V_B was connected to a positive dc power supply. These were set to produce a triangle wave at V_{IN} which has a maximum value of 15V and a minimum value of 0V. Voltages were measured with a Tektronix 11401 scope.

5) The quiescent current measurements were done using test circuit 2. V_A was connected to an pulse generator and pulsed at 100Hz, with a duty cycle of 5%. V_B was grounded. These were set to produce the necessary voltage at V_{IN}. R_{QUIES} measured 100.072Ω. Voltages were measured with a Tektronix 11401 scope. The voltage was measured across R_{QUIES} and divided by R_{QUIES} to give the quiescent current.

6) The load transient response measurements was done with test circuit 3. V_A was grounded. V_B was connected to a positive power supply to produce a dc voltage of 15V at V_{IN}. V_P was pulsed to allow Q1 to function as a switch, connecting R_{LOAD} on and off to ground to simulate the switching on and off of a load.

7) The maximum output current vs V_{IN} measurements were done using test circuit 1. V_A was connected to an pulse generator and pulsed at 100Hz, with a duty cycle of 5%. V_B was grounded. These were set to produce the necessary voltage at V_{IN}. R_{LOAD} measured 5.2Ω. Voltages were measured with a Tektronix 11401 scope. The voltage was measured at R_{LOAD} was then converted to a current.

8) The line transient response measurements was done with test circuit 1. V_A was connected to a pulse generator. V_B was connected to a positive dc power supply. These were set to produce a 15 volt dc voltage at V_{IN} with a pulse superimposed. Voltages were measured with a Tektronix 11401 scope.

CHAPTER 7

SG137 MACROMODEL DEVELOPMENT

7.1 INTRODUCTION

This chapter describes the development of the SG137 voltage regulator macromodel. The SG137 is a three terminal, adjustable, negative, voltage regulator.

7.2 DEVELOPMENT OF THE SG137 MACROMODEL

The functional block diagram for the SG137 macromodel is shown in Fig. (7.1). The macromodel for the SG137 is shown in Fig. (7.2). The voltage reference is been replaced by D_{ZR}, R_{ZR}, D_{Z1}, R_R, L_1, C_R, and R_{CR}. The bias current source is been replaced by R_Q. The error amplifier is replaced by E_1, E_2, R_{OE1}, C_P, R_P, R_{IN}, D_+, D_-, V_+, V_-, and E_+. The pass transistors are replaced by Q_P and some base resistance is provided for by R_{B1} and R_{B2}. Some additional circuitry has been added to the SG137 functional block diagram. F_Q, E_{Q1}, V_{Q1}, and R_{Q1} provide for quiescent current characteristics. R_{DO}, D_{DO1}, and D_{DO2} provide dropout characteristics for the SG137. D_L, E_L, D_{FB}, and E_{FB} provide the model with short circuit current and foldback current limiting. D_{DIS} provides for capacitive load discharge through the device. Finally, R_O provides for output resistance. This gives an overview of the macromodel.

Finally, the SG137 needs external resistors to provide for the variable output voltage. The basic application circuit for the SG137 is shown in Fig. (7.3). The

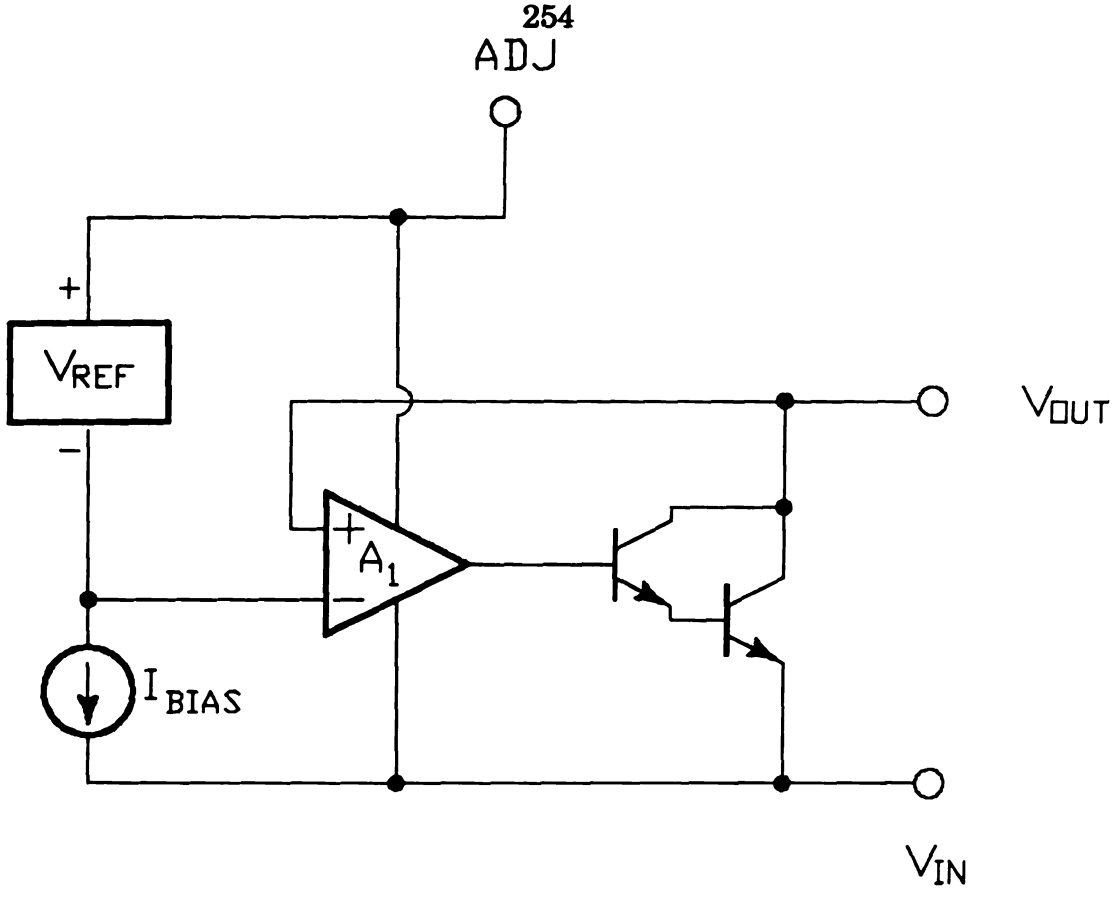

Figure 7.1 Functional block diagram for the SG137

regulated output voltage is then

$$V_{OUT} = V_{REF}\left(1 + \frac{R_2}{R_1}\right), \tag{7.1}$$

assuming the current out of the third terminal is 0A.

7.2.1 The Voltage Reference

The reference voltage generator consists of D_{ZR}, R_{ZR} D_{Z1}, R_R, R_Q, L_R, C_R, and R_{CR}. When a sufficient voltage is applied across pins 1 and 3, the diode D_{ZR} operates in the breakdown region. When set with a breakdown voltage of 1.25V, this provides the macromodel with the basic 1.25V reference which is seen in the actual chip. R_R and R_Q help to provide some dc changes for V_{REF} with changes in input voltage. These changes are the main contribution to line regulation and low frequency ripple

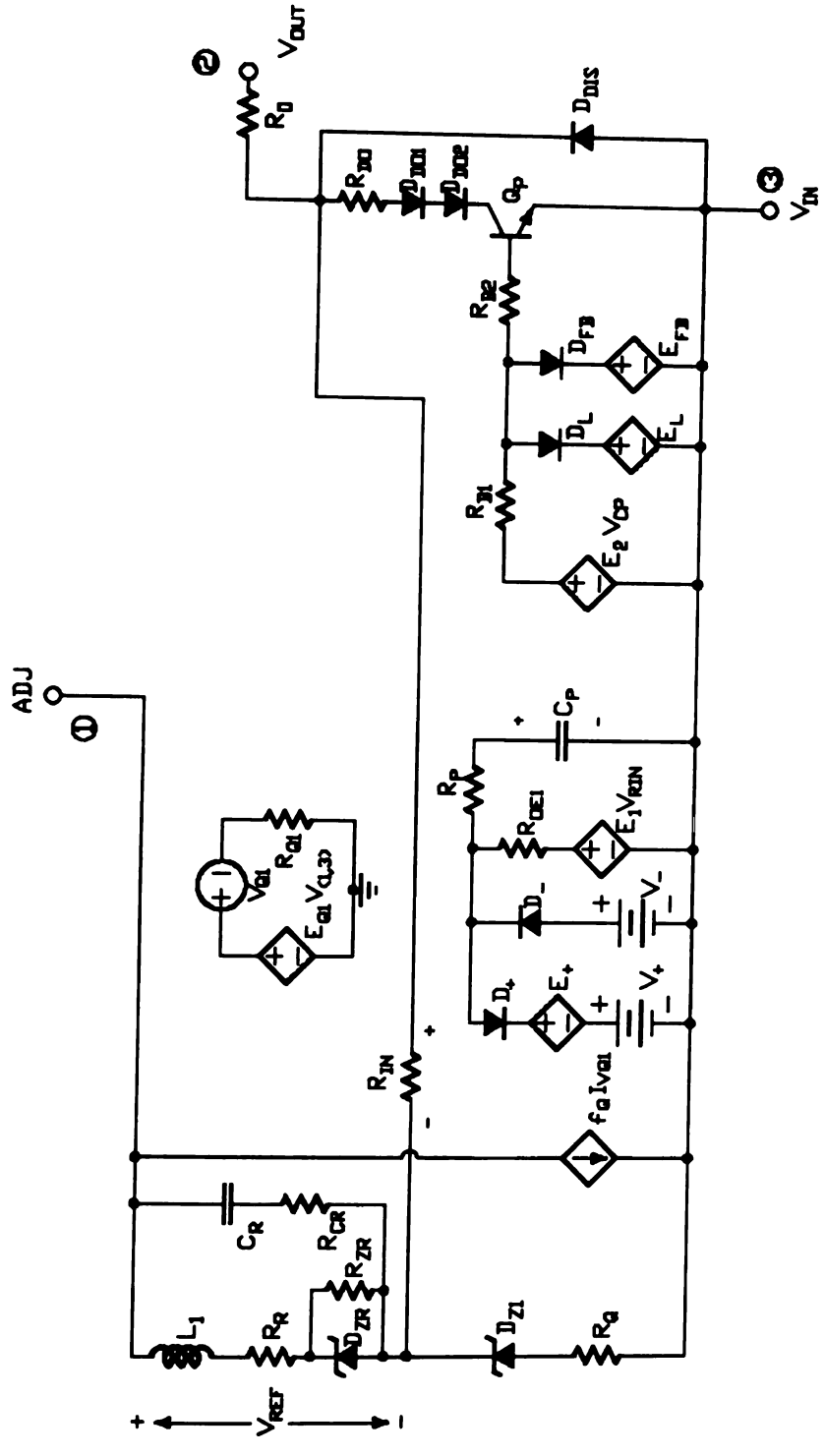

Figure 7.2 Macromodel for the SG137

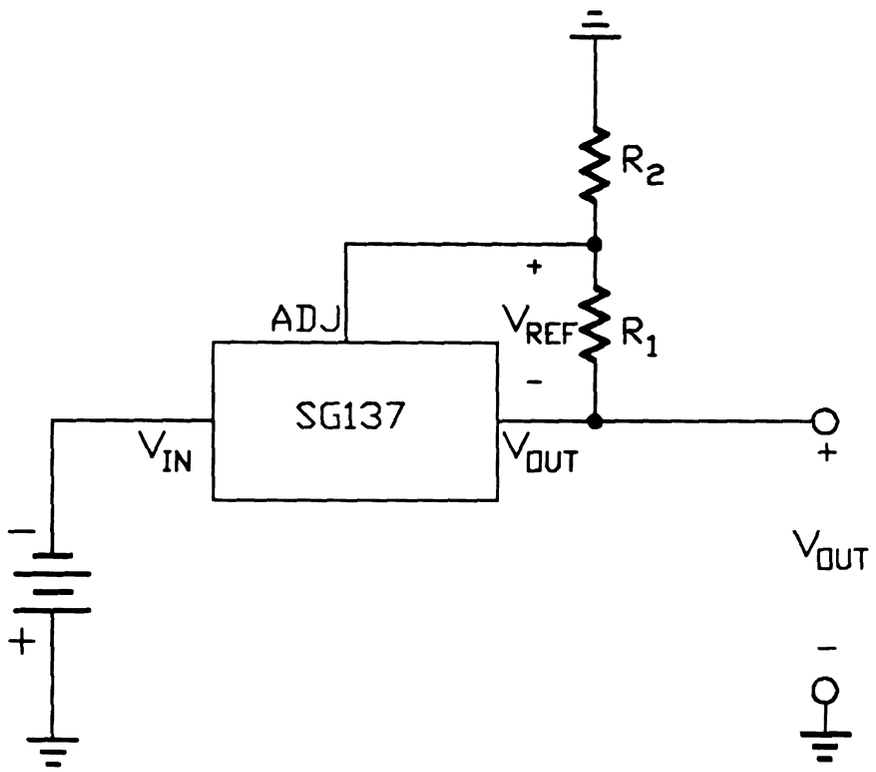

Figure 7.3 Basic application circuit for the SG137

rejection. The inductor L_R, the capacitor C_R and the resistor R_{CR} provide for the reference to have some frequency response. This provides the reference voltage with two poles and two zeros in it's ac response. This contributes significantly to the ripple rejection response.

R_Q is set to be much larger than the combination of the differential resistance of D_{ZR} and R_R so that under dc conditions, changes in input voltage which occur across the reference structure are dropped mainly across it. This contributes to quiescent current variations with input voltage.

The usual "on" voltage for the device. This is modeled by the diode D_{Z1}. Before the reference voltage can begin to turn on, the voltage between pins 1 and 3 must overcome BV_{DZ1}. This gives

$$BV_{DZ1} = V_{ON} \tag{7.2}$$

7.2.2 The Error Amplifier

The error amplifier is modeled as a one pole amplifier to model the effects of a frequency compensated amplifier which exists in the SG137. This effect is modeled by R_{IN} which represents the input resistance for the amplifier, E_1 which provides all of the dc gain, R_P and C_P which provide the pole, and E_2 which has a gain of one and senses the voltage across C_P. E_2 is used as a buffer. The amplifier senses the difference between a sample of the output and the reference voltage. R_O, D_+, D_-, V_+, V_-, and E_+ provide for maximum and minimum clamping for the amplifier.

7.2.3 Ripple Rejection Modeling

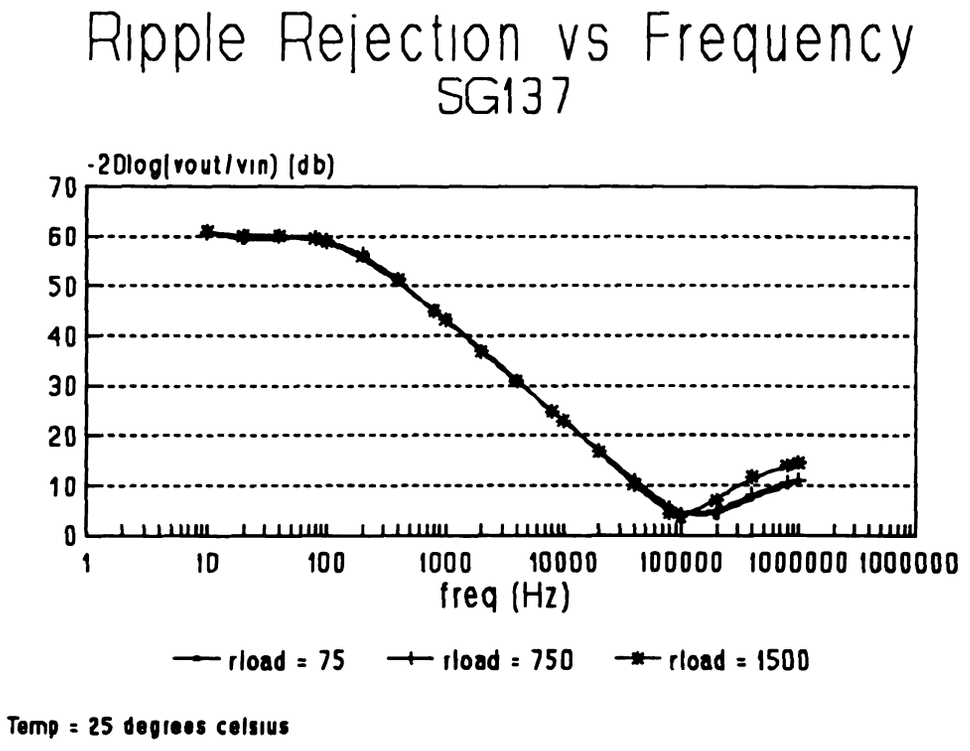

Figure 7.4 Ripple rejection vs frequency, measured

Fig. (7.4) gives an example of ripple rejection vs frequency for the SG137. In

modeling ripple rejection vs frequency, the following approximations are made. The first approximation is that the low frequency ripple rejection for all the loads are the same. The second approximation is that the first pole in ripple rejection is the same for all loads. As seen in Fig. (7.4), the approximations are reasonable.

In order to evaluate the ripple rejection for the macromodel, the program Sspice is used to get an approximate symbolic solution. The symbolic solution for the macromodel is quite complicated, and using this symbolic solution in designing the macromodel is quite involved. The useful formulas which can be used are given here without proof or derivation. These formulas provide the necessary information to correctly choose the low frequency ripple rejection and the first pole. These two parameters dominate the ripple rejection response as seen in Fig. (7.4). The formula for low frequency ripple rejection is

$$RR_{LF} = \frac{R_2}{R_Q + r_{DZ1}} + \frac{R_1 + R_2}{R_1}\frac{R_R + r_{DZR}}{R_Q + r_{DZ1}}, \tag{7.3}$$

where r_{DZ1} and r_{DZR} are the small signal resistances of the diodes D_{Z1} and D_{ZR}. The formula for the first pole in ripple rejection, which is the first zero in the transfer function is

$$Pl_{RR} = \frac{R_1 \| R_2 + R_R + r_{DZR}}{L_R}. \tag{7.4}$$

The capacitor C_R, R_{CR}, C_P, R_P, the load capacitor and it's series resistance contribute to the frequency response as well. The load capacitor and series resistance are fixed, but the other capacitors and resistors mentioned can be varied to produce the desired ripple rejection.

7.2.4 Output Impedance Modeling

Output impedance vs frequency is not modeled, however output resistance is modeled. The formula for output resistance has been determined from Sspice and is

$$R_{OUT} \approx \left(\frac{R_{B1} + R_{B2}}{A_{DC} BF_{QP}} + R_O \right) \frac{R_2}{R_1}, \tag{7.5}$$

where A_{DC} is taken to be the product of the dc gains of E_A and E_B.

The output resistance of the SG137 is taken from either the load transient response or load regulation measurement. For a given load, the Thevenin output resistance can be deduced from the change in output voltage when the load is connected from the output voltage under no load conditions.

7.2.5 Quiescent Current Modeling

Quiescent current vs input voltage is shown in Fig. (7.5). The elements which contribute to quiescent current are R_Q, F_Q, E_{Q1}, V_{Q1}, and R_{Q1}. E_{Q1} is a voltage controlled voltage source which depends upon the reference voltage. F_Q is a current controlled current source which senses the current through V_{Q1} and has a gain of 1. From the transistion from V_{IN} = 0V to the point where V_{REF} achieves its reference voltage, it is F_Q which contributes most of the quiescent current to the third terminal. At this point

$$I_Q = I_{FQ} = \frac{V_{REF}}{R_{Q1}} f_{QP} \tag{7.6}$$

or

$$f_Q = I_Q \frac{R_{Q1}}{V_{REF}}. \tag{7.7}$$

Then, R_{Q1} can be varied with temperature to produce a change in quiescent current with temperature.

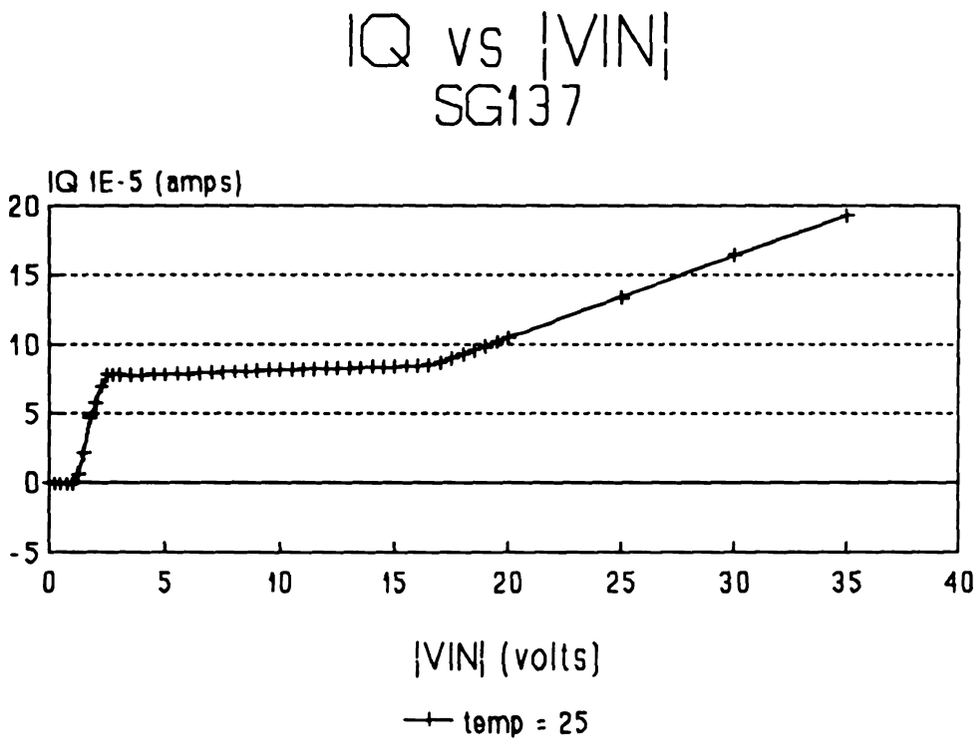

Figure 7.5 Quiescent current vs $|V_{IN}|$, measured

After the reference voltage has achieved it's nominal value, the current through F_Q no longer changes. The variations in quiescent current now come from R_Q. Thus

$$R_Q = \frac{\Delta V_{IN}}{\Delta I_Q}. \tag{7.8}$$

In the quiescent current measurement, the lab data plot shows that a severe change in quiescent current occurs at approximately V_{IN} = 16V. This slope is not modeled. It is felt that this slope is a function of the test circuit, and does not occur under normal operation. If it did, quiescent current on the order of .2mA, which occurs at $|V_{IN}|$ = 35V, would have a significant effect on the output voltage, as it flows through R_2. This was checked in lab, and no effect on output voltage was noted. Therefore, it probably does not exist, and is not modeled.

7.2.6 Short Circuit Current and Foldback Current Limiting

A plot of measured short circuit current and foldback current limiting is shown

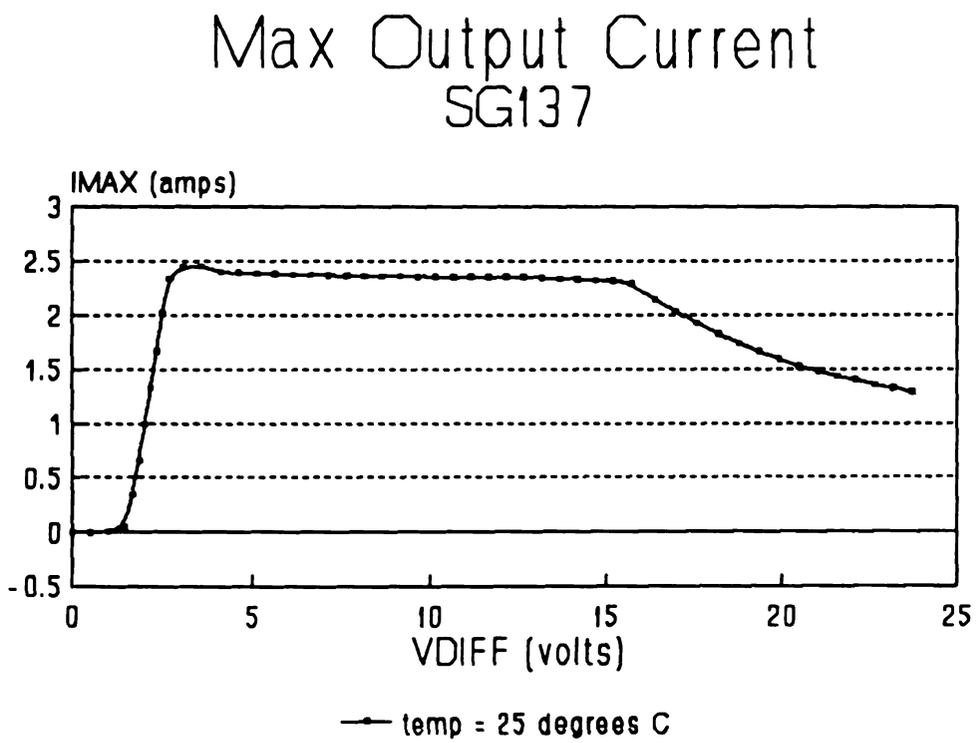

Figure 7.6 Maximum output current vs V_{DIFF}, measured

in Fig. (7.6).

The short circuit current circuitry consists of D_L and E_L and the foldback current circuitry consists of D_{FB} and E_{FB}. These additional circuitry work in the following way.

The load current flows through the collector of Q_P. Then, a current, approximately equal to IC/BF must flow through the base of Q_P as well. If the base current is limited, the collector current is limited, and hence the output current is limited. The base current of Q_P is limited by limiting the voltage across R_{B2}. The voltage drop across the series combination of D_L and E_L is equal to the voltage drop

across $R_{B2} + V_{BEQP}$. If $V_{RB2} + V_{BEQP}$ becomes larger than $V_{ON,DL} + V_{EL}$, then the diode D_L will turn on. If the voltage drop across the diode is taken to be nearly equal to V_{BEQP}, then $V_{RB2} = V_{EL}$. V_{EL} depends upon the differential voltage, V(2,3), so under short circuit current conditions, and for a given V(2,3) it is constant and constrained, meaning that V_{RB2} cannot become larger than V_{EL}. The voltage R_{B2} then becomes clamped at this maximum voltage, and hence the load current becomes clamped at some maximum value. The equation, then relating maximum output current to the model parameters is

$$I_{MAX} = BF_{QP}\frac{V_{EL}(V(2,3))}{R_{B2}}, \tag{7.9}$$

where the voltage V_{EL} is a function of the differential voltage V(2,3). This formula does not take into account the current necessary to bias R_1 and R_2 which is small in comparison to the maximum allowable output current. To select the coefficients of the polynomial which describes the voltage across E_L, two points are picked in the current limiting region, which are not in the foldback current region. These points are the point in Fig. (7.6) where the maximum output current is achieved after device turn on, and the edge of the foldback region. In practice, E_L is modeled with a constant term and one first order term. The constant slope of the maximum output current in this region should strongly suggest this relationship.

The foldback current works identically to the short circuit current limiting circuitry. In the foldback region, the voltage drop across E_{FB} is selected so that it is less than the voltage drop across E_L in the foldback region. This means that the voltage E_{FB} is the main controller of the maximum output current. Then

$$I_{MAX} = BF_{QP}\frac{V_{EFB}(V(2,3))}{R_{B2}} \tag{7.10}$$

and E_{FB} also depends on the differential voltage. The behavior of the maximum output current in this region, suggests a higher order relationship between E_{FB} and V(2,3). In practice, a fourth order relationship is used.

7.2.7 Power Up and Down, Square Wave

Fig. (7.7) gives the power up and power down for a square wave input. The peaking which occurs in power up is a result of the natural frequencies of the circuit. These are mainly determined by ripple rejection, but it is advised to use ripple rejection to get a feel for the approximate placement of the poles and zeros, and to tweak components to get the correct power up transient response. The delay seen just before the peaking occurs results from the output capacitor slewing, which occurs because the regulator can only supply a maximum amount of current due to current limiting. This, of course, is set by the current limiting itself.

Upon power down, the capacitor must discharge itself through the regulator. D_{DIS} is used to model these effects.

7.2.8 Power Up and Down, Triangle Wave

Fig. (7.8) gives the measured power up and down with triangle wave. The main component of power up and down which is modeled, and controlled by the user, is the peaking which occurs just prior to the regulation of the chip. This occurs primarily as a result of the time required to charge up C_P. Presently, there is no formula for this, it is done with an empirical fit.

7.2.9 Dropout Characteristics

The dropout characteristics are contributed by R_{DO}, D_{DO1}, D_{DO2} and Q_P. This is

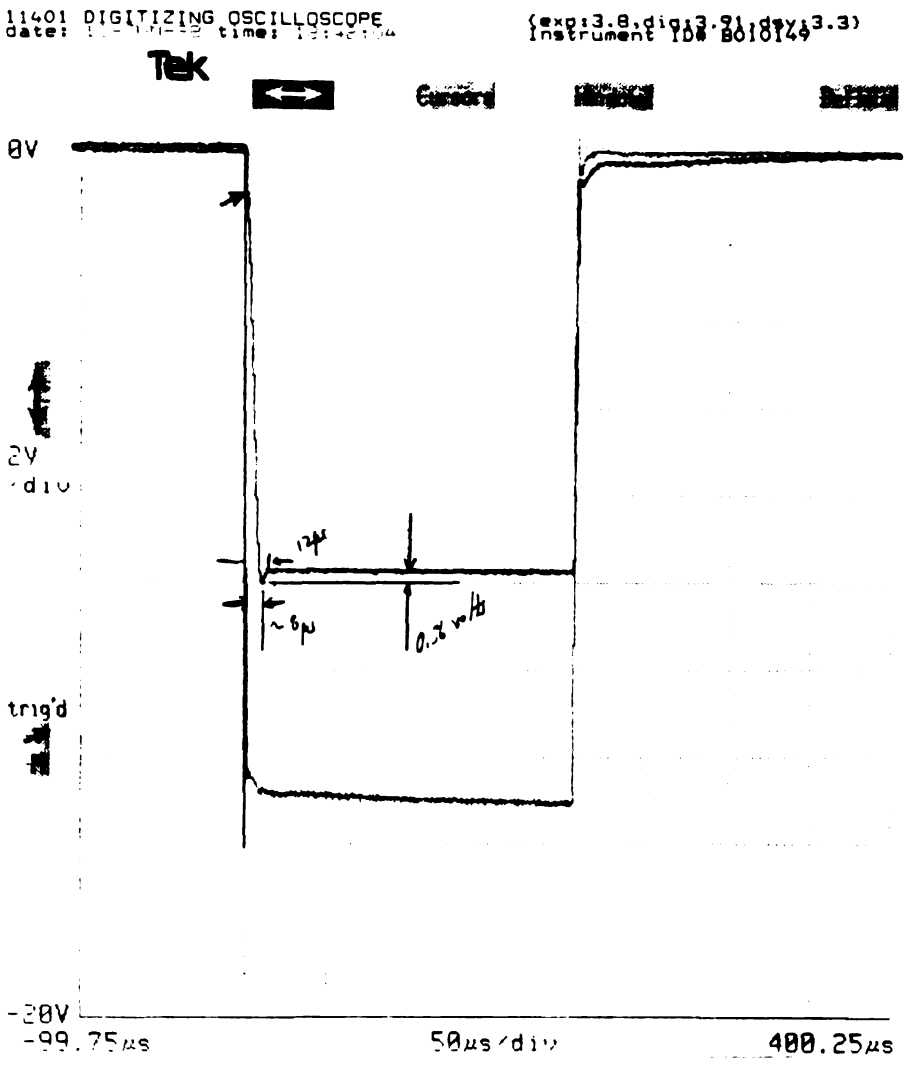

Figure 7.7 Power up and down, square wave, measured

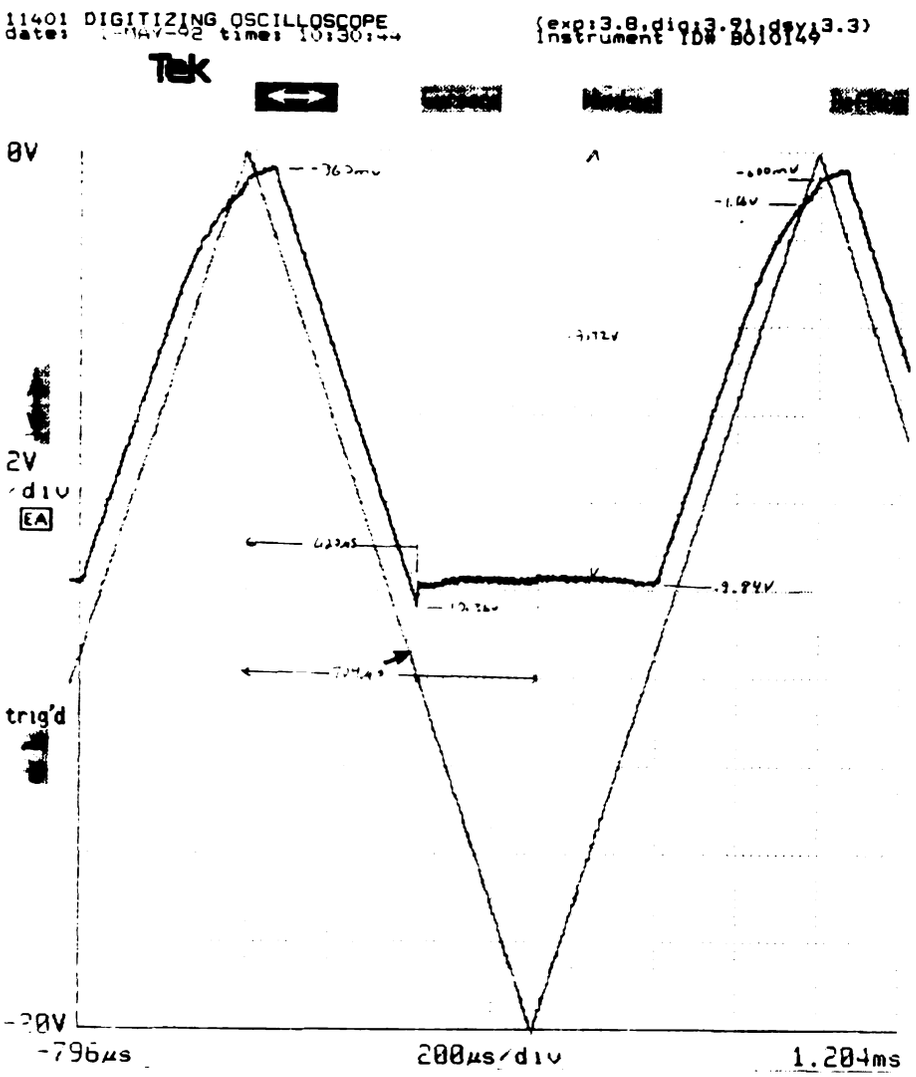

Figure 7.8 Power up and down, triangle wave, measured

approximately the voltage required to put Q_P at the edge of saturation. Then

$$VDO = I_{LOAD}R_{DO} + 2NVT\ln\left(\frac{I_{LOAD}}{IS_{DDO1}}\right) + V_{SAT,QP}(I_{LOAD}), \qquad (7.11)$$

if the diodes D_{DO1} and D_{DO2} are taken to be equivalent. Eqn. (7.11) does takes into account the fact that the saturation voltage of Q_P is a function of load current.

7.2.10 Other Modeled Characteristics

The prior characteristics are used in determining component selection. As a result of correct choice of parameters and topology the macromodel predicts other responses. These are: line and load regulation, line transient response and load transient response.

7.3 DESIGN PROCEDURE FOR A SG137

Based on the equations and procedures shown in the last section, a design procedure will be developed in this section.

Basic to the design procedure is a list of measurements required to base the design on. The following measurements should be taken in the basic regulator circuit:

1) Measure V_{OUT} vs V_{IN} with no load.

2) Measure IQ vs V_{IN} with no load.

3) Measure V_{OUT} for V_{IN} = -15V, with no load.

4) Measure ripple rejection vs frequency with a 100Ω load.

5) Take a load transient response measurement with a 100Ω load, and from this determine R_{OUT}.

6) Measure maximum output current vs voltage differential.

7) Measure dropout voltage with R_{LOAD} = 100Ω.

8) Take a power up and down with both triangle wave input and square wave input with $R_{LOAD} = 100\Omega$.

9) Measure R_{LOAD}, and the external resistors R_1 and R_2. These measured values get used in all of the equations. Measure as well the capacitances of all capacitors and the series resistance of all capacitors at some representative frequency.

The component selection procedure is:

1) Select E_1 and E_2.

2) Select the amplifier clamping circuitry, these are the values for: V_+, V_-, E_+, E_-, and the diode parameters for D_+ and D_-.

3) Based on the V_{OUT} vs V_{IN} measurement, determine the input voltage required to begin to turn the circuit on, V_{ON}, then

$$BV_{DZ1} = |V_{ON}|. \tag{7.12}$$

Select NBV_{DZ1}.

4) From the measured value of V_{OUT} at $V_{IN} = -15V$, and utilizing Eqn. (7.1),

$$BV_{DZR} = V_{REF} = \frac{|V_{OUT}|}{\left(1 + \frac{R_2}{R_1}\right)}. \tag{7.13}$$

Select NBV_{DZR} and R_{ZR}.

5) Measure the slope of IQ vs V_{IN} for the quiescent current measurement. Then from Eqn. (7.8),

$$R_Q = \frac{\Delta IQ}{|\Delta V_{IN}|}. \tag{7.14}$$

6) From the ripple rejection measurement, determine RR_{LF}. Then

determine the small signal resistance of D_{ZR}, r_{DZR} and of D_{Z1}, r_{DZ1}. This is determined from a trial macromodel run with PSpice. Then from Eqn. (7.3),

$$R_R = \left(RR_{LF} - \frac{R_2}{R_Q + r_{DZ1}}\right)\left(\frac{R_1}{R_1 + R_2}\right)(R_Q - r_{DZ1}) - r_{DZR} \tag{7.15}$$

7) From the ripple rejection measurement, determine $P1_{RR}$, then from Eqn. (7.4),

$$L_R = \frac{R_1 \| R_2 + R_R + r_{DZR}}{P1_{RR}}. \tag{7.16}$$

8) Select R_{CR}

9) From the ripple rejection vs frequency measurement, determine C_R empirically.

10) Select R_Q and R_P

11) From the power up and down triangle measurement, as well as ripple rejection vs frequency, determine C_P empirically.

12) From the power up and down square wave measurement, measuring the difference in the input and output voltage waveforms directly after power down, select an appropriate value for N_{DDIS}.

13) Select R_{Q1}. Then from the IQ vs V_{IN} measurements and from Eqn. (7.7),

$$f_Q = I_Q \frac{R_{Q1}}{V_{REF}}. \tag{7.17}$$

14) Select the parameters for the output transistor Q_P. These are BF and IS.

15) Select R_{B1} and R_{B2}.

16) Select the parameters for the diodes D_L and D_{FB}.

17) From the maximum output current vs differential voltage measurement, in the short circuit current region, select I1 and V1, the point where maximum output current is achieved. Select I2 and V2 as the point where the device enters into the foldback region. Then the coefficients of E_L need to be solved for. E_L is described as

$$E_L = a_0 + a_1 V_{DIFF} \tag{7.18}$$

Then from Eqn. (7.9), let

$$a_0 = \frac{I1}{BF_{QP}} R_{B2}. \tag{7.19}$$

Then a_1 can be determined and is

$$a_1 = \frac{\frac{R_{B2} I1}{BF_{QP}} - a_0}{V2}. \tag{7.20}$$

18) Select a maximum of 4 points in the foldback limiting region, (I1,V1) (I2,V2) (I3,V3) and (I4,V4). The first point should be the point on the curve where the device enters into the foldback region, the last should be the last point in the measurement, and the other two placed where the rate of change in the curve is greatest. The coefficients of E_{FB} need to be solved for and these are b_0, b_1, b_2, and b_3. E_{FB} can now be described as

$$E_{FB} = b_0 + b_1 V_{DIFF} + b_2 V_{DIFF}^2 + b_3 V_{DIFF}^3. \tag{7.21}$$

The coefficients can be solved for by solving the system of equations

$$\begin{pmatrix} 1 & V1 & V1^2 & V1^3 \\ 1 & V2 & V2^2 & V2^3 \\ 1 & V3 & V3^2 & V3^3 \\ 1 & V4 & V4^2 & V4^3 \end{pmatrix} \begin{pmatrix} b_0 \\ b_1 \\ b_2 \\ b_3 \end{pmatrix} = \begin{pmatrix} \frac{I1}{BF_{QP}} R_{B2} \\ \frac{I2}{BF_{QP}} R_{B2} \\ \frac{I3}{BF_{QP}} R_{B2} \\ \frac{I4}{BF_{QP}} R_{B2} \end{pmatrix}. \tag{7.22}$$

19) From a trial run with the macromodel, determine the value for $V_{SAT,QP}$. Select $IS_{DDO1,DDO2}$. Determine the value of the load current. From the measured dropout voltage, VDO, and Eqn. (7.11),

$$N_{DDO} = \frac{VDO - V_{SAT,QP} - I_{LOAD} R_C}{2VT \ln\left(\frac{I_{LOAD}}{IS_{DDO}}\right)}. \tag{7.23}$$

20) From the load regulation measurement, measure the change in output voltage when the 100Ω load is connected from no load conditions. Then from Eqn. (7.5)

$$R_{OUT} = \frac{\Delta V_{OUT}}{V_{OUT,\,RL=100\Omega}} R_{LOAD}. \tag{7.24}$$

From Eqn. (7.5)

$$R_O = R_{OUT} \frac{R_1}{R_2} - \frac{R_{B1} + R_{B2}}{A\, BF_{QP}}. \tag{7.25}$$

21) Select R_{IN}. At times, a capacitive load may need to partially discharge through this resistance, so it should be selected large, but finite.

22) Several diodes will have very small values selected for their series resistance, RS, and junction capacitance, CJO. This helps the

macromodel converge, especially at the temperatures of -55 degrees and 125 degrees.

This concludes the design procedure. All of the parameters for the macromodel have been selected.

7.4 DESIGN EXAMPLE FOR A SG137

The design example is based on laboratory measurements is presented. The data, unless otherwise specified, is taken directly off from the plots which were shown previously in the document.

The nominal 100Ω load resistor was measured at 100.214Ω. R_1 was measured at 119.93Ω and R_2 was measured at 820.13Ω. An output capacitor was used with a series capacitance value of .9396uF and a series resistance of 1.0953Ω at 100kHz. The output capacitor was necessary. An adjustment capacitor was also necessary. This is a capacitor which is connected between the adjustment pin and ground. This had a series capacitance of 158.04pF and a negligible series resistance at 100kHz.

1) Set $E_1 = 600$ and $E_2 = 1$.

2) Let the diodes D^+ and D_- be the Pspice default diodes. Set $V_+ = -1V$, $V^- = 1V$. Set the gain of $E_+ = 1$ and let V(3,1) be the controlling voltage. This means the maximum voltage for the amplifier is (V(3) + 0.3)V and the minimum voltage for the amplifier is (0.3 + V(1))V which falls between the rail voltages of the chip.

3) Based on the V_{OUT} vs V_{IN} measurement, set $BV_{Z1} = 1V$. Set $NBV_{Z1} = 0.001$.

4) From the measured value of V_{OUT} at $V_{IN} = -15V$, set $BV_{DZR} = 1.25V$. Set

NBV_{DZR} = 0.001 and R_{ZR} = 1MEGΩ.

5) From the IQ vs V_{IN} measurement, R_Q = 1.7546MegΩ.

6) From the ripple rejection measurement, RR_{LF} = 60.8db = 0.9120m. Then r_{DZR} was determined to be 1.3Ω, as was r_{DZ1}. This gives R_R = 98.2994Ω.

7) $P1_{RR}$ was determined to be 120Hz, then L_1 = .2709H.

8) Set R_{CR} = 150kΩ.

9) By iteration, C_R = 3pF.

10) Set R_O = 10Ω and R_P = 151Ω.

11) By empirical methods, C_P = 0.01uF.

12) From the power up and down square wave measurement, set N_{DDIS} = 1.

13) IQ was measured at 78.09uA. Set R_{Q1} = 1Ω. Then f_Q = 0.0625m.

14) Set BF_{QP} = 500 and IS_{QP} = 1e-14A.

15) Set R_{B1} = 10Ω and R_{B2} = 500Ω.

16) Let the diode parameters for D_L and D_{FB} be the Pspice default diodes.

17) From the maximum output current vs differential voltage measurement, I1 = 2.447A, then a_o = 2.447. Then I2 = 2.29A and V2 = 15.724V gives a_1 = -0.01.

18) 4 points were selected in the foldback limiting region, (2.29A, 15.724V) (1.8233A, 18.188V) (1.5878A, 19.922V) and (1.2880A, 23.72V). Solving (7.22) yields the following values for the coefficients a_0, a_1, a_2, and a_3, 12.5955, -1.2275, 0.0457, -5.9169e-4.

19) Set $IS_{DDO1, DDO2}$ = 1e-14A. From a trial run with the macromodel, $V_{SAT,QP}$ = 0.1292V. Then from $N_{DDO1,DDO2}$ = 0.9687.

20) From the load regulation measurement, ΔV_{OUT} = 1.9mV for the 100Ω load, then R_{OUT} = 0.0193Ω and R_O = 1.1556mΩ.

21) Set R_{IN} = 100kΩ.

This concludes the design example. All of the parameters for the room temperature macromodel have been selected.

7.5 MODELING THE SG137 AT -55 AND 125 DEGREES

7.5.1 Strategy in Modeling the SG137 Temperature Variations

The room temperature model is developed. The steps which need modifications are steps 3, 4, 5, 6, 7, 8, 11, 13, and 15. These will give rise to new values for BV_{DZ1}, BV_{DZR}, R_Q, R_R, L_R, R_{CR}, C_P, and R_{B2}. Lab data will be taken and the above parameters will be selected.

In step number 13, R_{Q1} was set, then the determination of f_Q followed. For simplicity, f_Q remains constant throughout temperature, and R_{Q1} is varied to produce variation in quiescent current with temperature.

For the temperature dependence of the maximum current and foldback current limiting, R_{B2} is varied. This results in shifting the maximum output current curve up or down, depending on the temperature. This does not give exact results, but gives good results.

7.5.2 Design Example to Include Temperature Dependance

In this section the parameters for the model for -55°C and 125°C are developed. The temperature coefficients are determined and then inserted into the room temperature model. This represents the fully developed, macromodel for the SG137.

Following the format of the first example and applying it to the -55°C model:

3) Based on the V_{OUT} vs V_{IN}, set BV_{DZ1} = 1.25V.

4) From the measured value of V_{OUT} at V_{IN} = -15V, set BV_{DZR} = 1.2503 V.

5) From the IQ vs V_{IN} measurement, R_Q = 1.7546MegΩ.

6) From the ripple rejection measurement, RR_{LF} = 57.6db = 1.9120m. Then r_{DZR} was determined to be .851Ω as was r_{DZ1}. This will then give R_R = 189.6Ω.

7) $P1_{RR}$ was determined to be 170Hz, then L_R = .2755H.

8) Set R_{CR} = 150kΩ.

9) By iteration, C_R = 3pF.

11) By empirical methods, C_P = 0.01uF.

13) IQ was measured to be 81.6uA. Then R_{Q1} = .9574Ω.

15) I_{MAX} = 2.36A. From Eqn. (7.19), R_{B2} = 518.43Ω.

20) From the load transient response measurement, ΔV_{OUT} = 4mV for the 100Ω load, then R_{OUT} = 0.0410Ω and R_O = 4.2674mΩ.

Following the format of the first example for the and applying it to the 125°C model:

3) Based on the V_{OUT} vs V_{IN}, set BV_{DZ1} = .75V.

4) From the measured value of V_{OUT} at V_{IN} = -15V, set BV_{DZR} = 1.2511V.

5) From the IQ vs V_{IN} measurement, R_Q = 1.9331MegΩ.

6) From the ripple rejection measurement, RR_{LF} = 61.8db = .81283m. Then r_{DZR} was determined to be 1.51Ω as was r_{DZ1}. This will then give R_R = 94.3197Ω.

7) $P1_{RR}$ was determined to be 110Hz, then L_R = .29H.

8) Set R_{CR} = 150kΩ.

9) By iteration, C_R = 3pF.

11) By empirical methods, C_P = 0.01uF.

13) IQ was measured to be 81.6uA. Then R_{Q1} = .8445Ω.

15) I_{MAX} = 2.413A. From Eqn. (7.19), R_{B2} = 507.0536Ω.

20) From the load regulation measurement, ΔV_{OUT} = 1mV for the 100Ω load, then R_{OUT} = 0.0102Ω and R_O = -.2mΩ, therefore let it be approximately 1e-8Ω.

A final summary of the temperature dependent parameters and elements follows in Table 7.1.

element or **parameter**	**value** at **25 degrees**	**value** at **-55 degrees**	**value** at **125 degrees**
BV_{DZ1}	1	1.25	.75
BV_{DZR}	1.25	1.2503	1.2511
R_Q	1.7546Meg	1.7546Meg	1.9331Meg
R_R	98.2994	189.6	94.3197
L_R	.2709m	.2755	.29
R_{Q1}	1	.9574	.8445
R_{B2}	500	518.43	507.0536
R_O	1.1556m	4.2674m	1e-8

Table 7.1 Temperature dependent components and parameters

Solving for the linear and quadratic coefficients for each of these components and

parameters leads to the following results in Table 7.2

element or **parameter**	**TC1** or **TBV1** (linear coeff.)	**TC2** or **TBV2** (quadratic coeff.)
BV_{DZ1}	-0.002847	3.4722e-6
BV_{DZR}	2.2444e-6	6.5556e-8
R_Q	4.5212e-4	5.6515e-6
R_R	-0.00663	6.2251e-5
L_R	1.9544e-4	5.0962e-6
R_{Q1}	-3.9528e-4	-1.1597e-5
R_{B2}	-1.9327e-4	3.3434e-6
R_O	-.007894e-4	0.001136

Table 7.2 Temperature coefficients

The macromodel for the SG137 follows. The macromodel includes the effects of temperature.

```
.SUBCKT SG137    1  2  3
*pin out        adj  |  |
*                   out |
                        in
LR      1 4 IND1 .2709
.MODEL IND1 IND (TC1=7.8864E-4 TC2=-2.8391E-5)
RR      4 5 98.2994 TC=-0.0063,6.2251E-5
CR      1 6 3p
RCR     6 7 150k
DZR     7 5 DZR
.MODEL DZR D (BV=1.25 TBV1=2.2444E-6 TBV2=6.5556E-8 NBV=0.0001 CJO=.1P)
RZR     7 5 1MEG
DZ1     8 7 DZ1
.MODEL DZ1 D (BV=1 TBV1=-0.002847 TBV2=3.4722E-6 NBV=0.0001 CJO=1P
RS=1)
RQ      8 3 1.7546MEG TC=4.5212E-4,5.6515E-6
FQ      1 3 VQ1 0.0625m
EQ1     24 0 1 7 1
VQ1     24 25 dc 0
RQ1     25 0 1 TC=-3.9528E-4,-1.1597E-5
```

```
RIN     7 23 100k
E1      11 3 23 7 600
ROE1    9 11 10
D+      9 13 dc
V+      14 3 -1
E+      13 14 1 3 1
D-      12 9 DC
V-      12 3 DC 1
.MODEL DC D (CJO=10P)
RP      9 10 151
CP      10 3 .01U
E2      15 3 10 3 1
RB1     15 16 50
RB2     16 19 500 TC=-1.9327E-4,3.3434E-6
DSC     16 17 DMOD
ESC     17 3 POLY (1) (2,3) 2.447  -.01
DFB     16 18 DMOD
EFB     18 3 POLY(1) (2,3) 12.5955 -1.2275 0.0457 -5.9169E-4
QP      20 19 3 QMOD
.MODEL QMOD NPN (BF=500 IS=1E-14)
RDO     23 22 0.1
DDO1    22 21 DDO
DDO2    21 20 DDO
.MODEL DDO D (N=.9687 IS=1E-14)
RO      23 2 0.0017 TC=-0.07894,0.001136
DDIS    3 23 DDIS
.MODEL DDIS D (CJO = 1P)
.MODEL DMOD D (IS=1E-14)
.ENDS SG137
```

7.5.3 Comparison of Macromodel Predictions with Lab Results

A comparison of macromodel predictions with lab results is presented in this section.

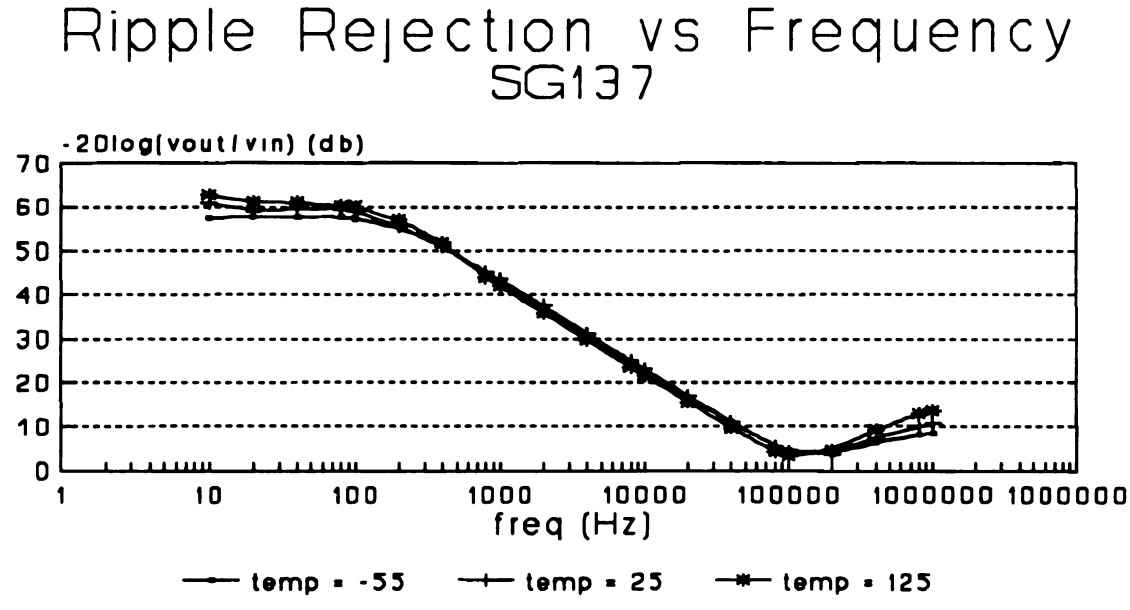

Figure 7.9 Ripple rejection vs frequency, measured

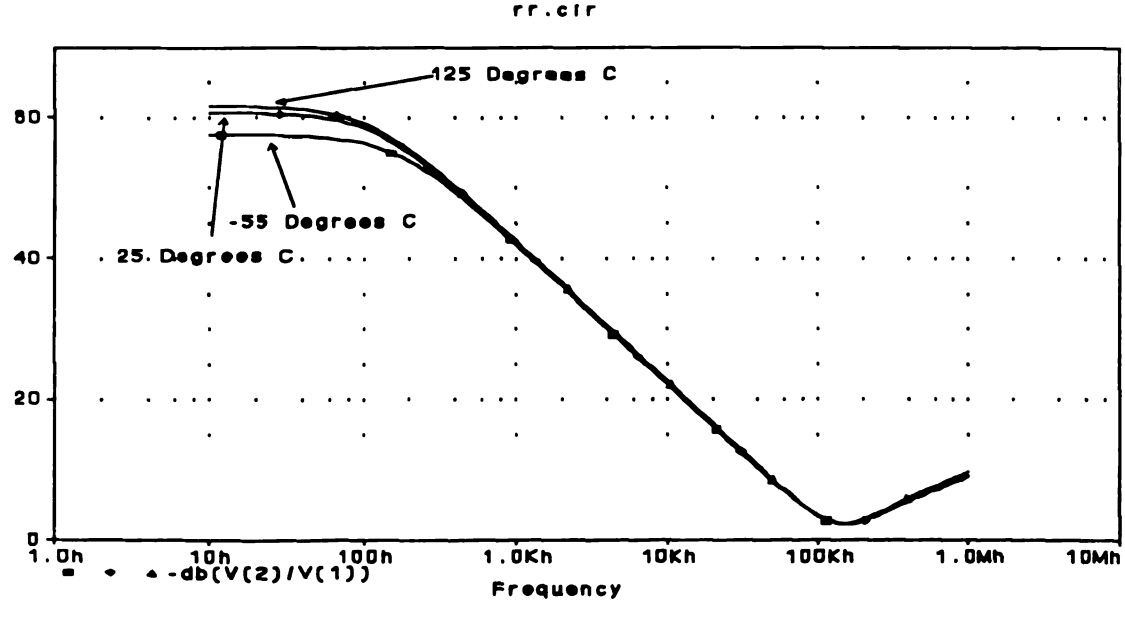

Figure 7.10 Ripple rejection vs frequency, macromodel

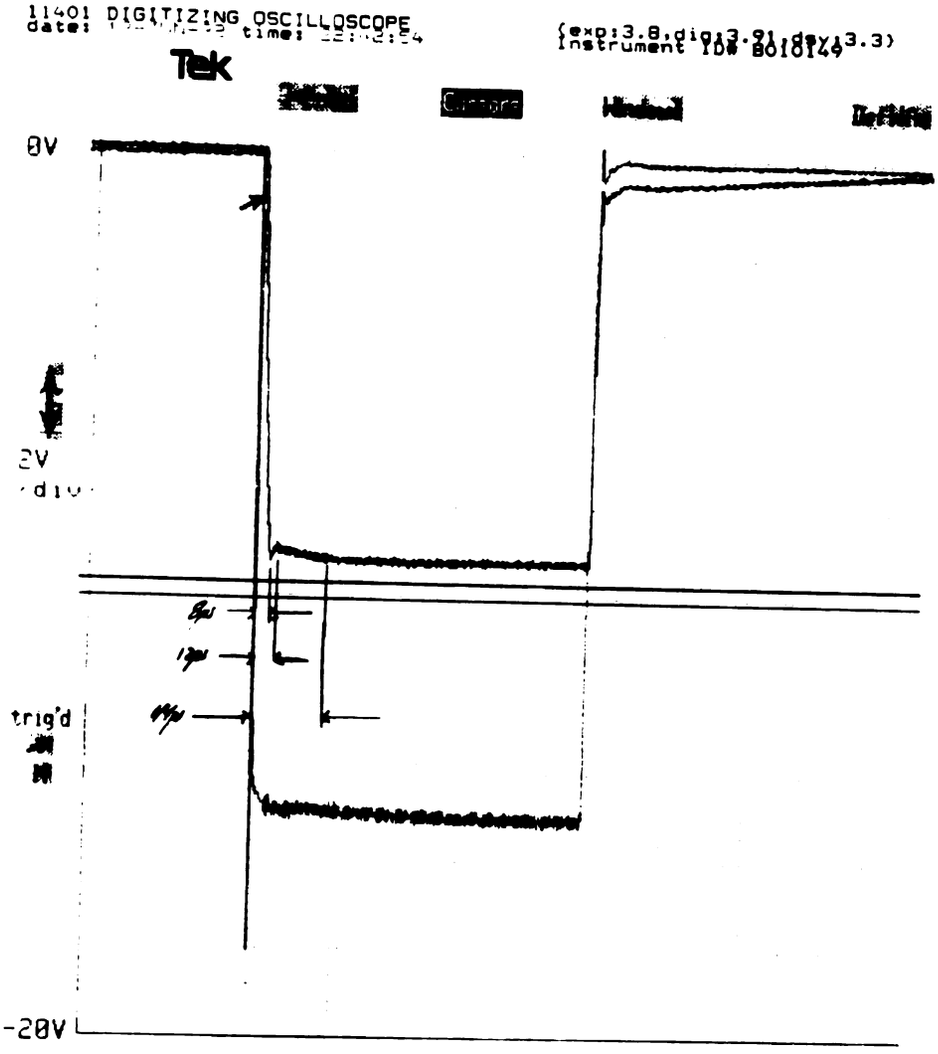

Figure 7.11 Power up and down, square wave, T = -55, measured

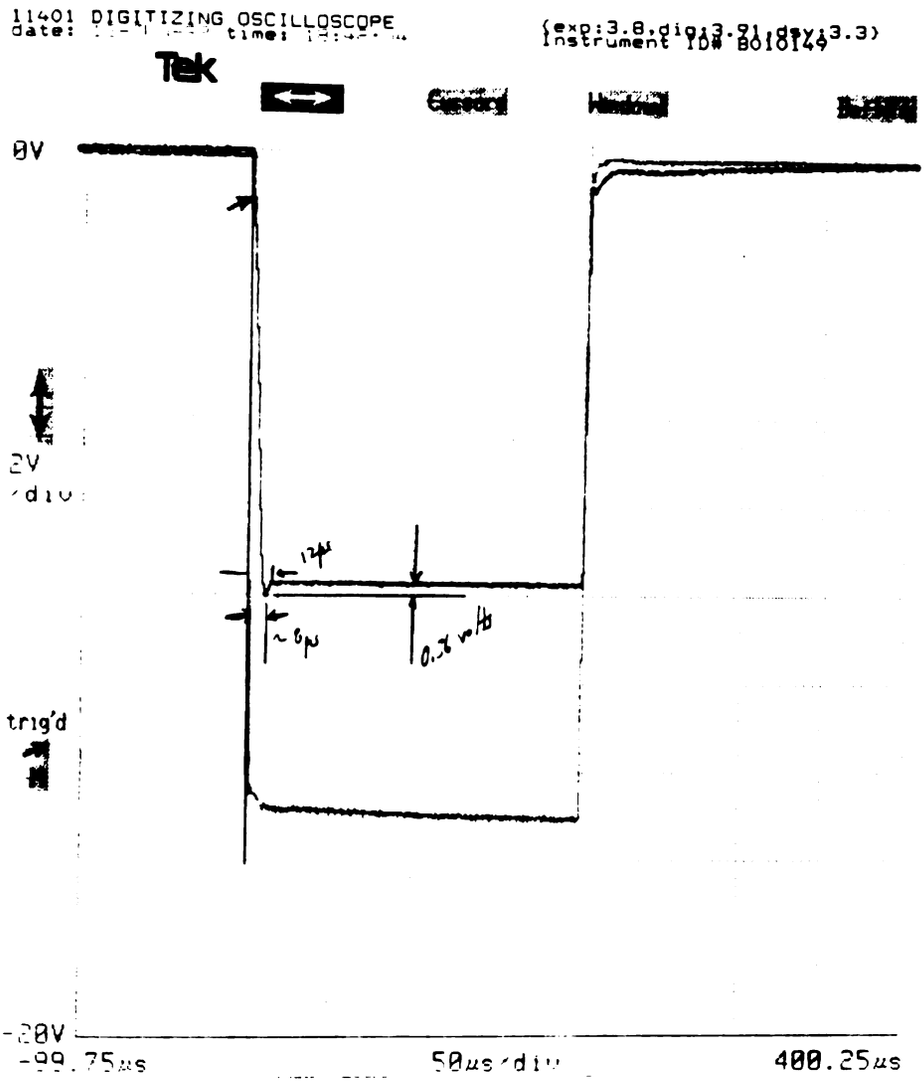

Figure 7.12 Power up and down, square wave, T = 25, measured

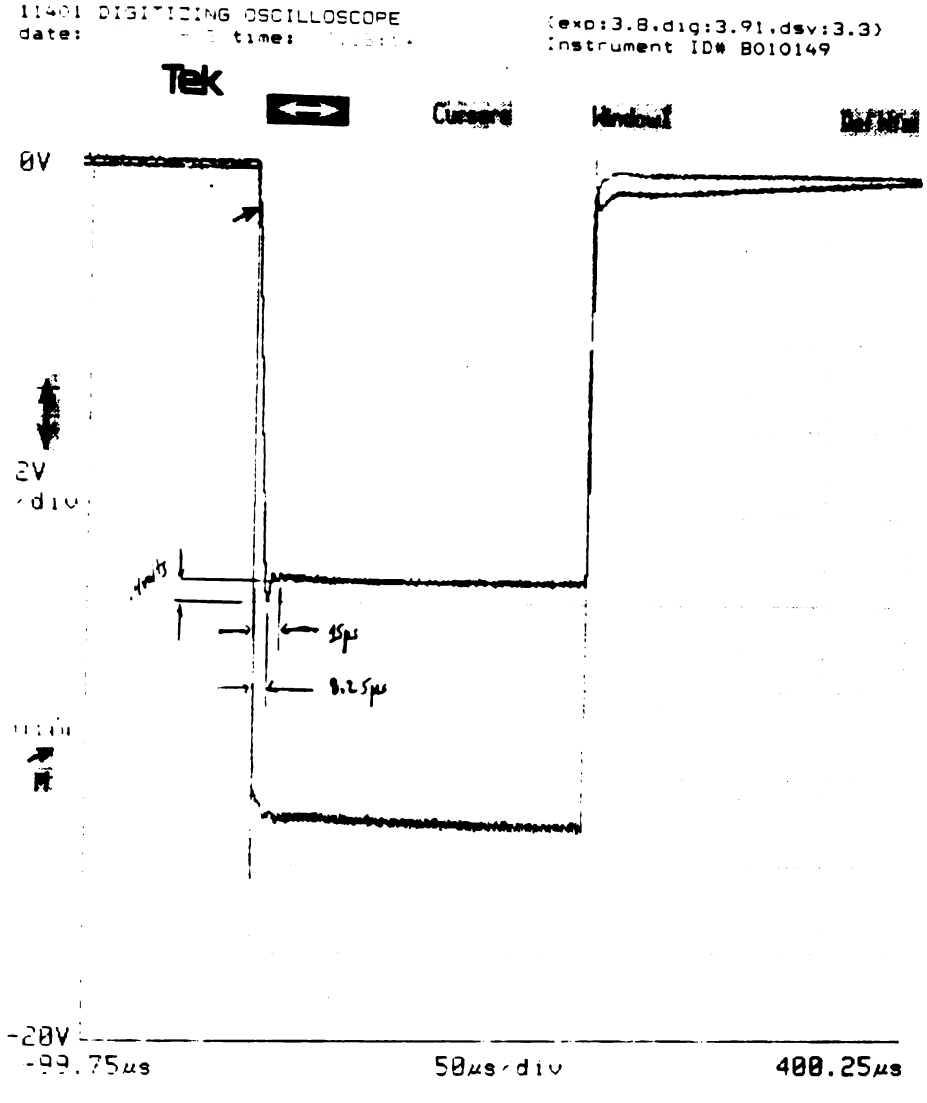

Figure 7.13 Power up and down, square wave, T = 125, measured

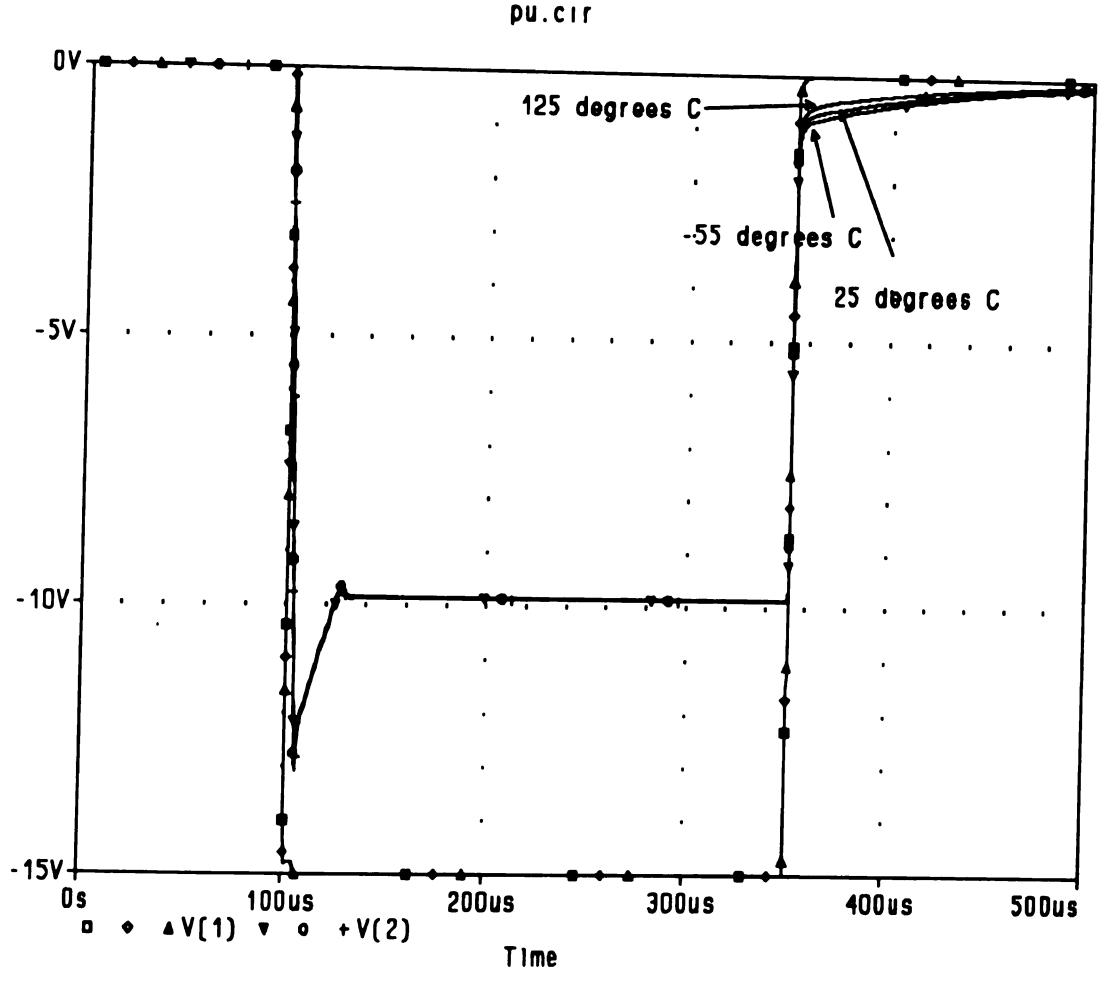

Figure 7.14 Power up and down, square wave, macromodel

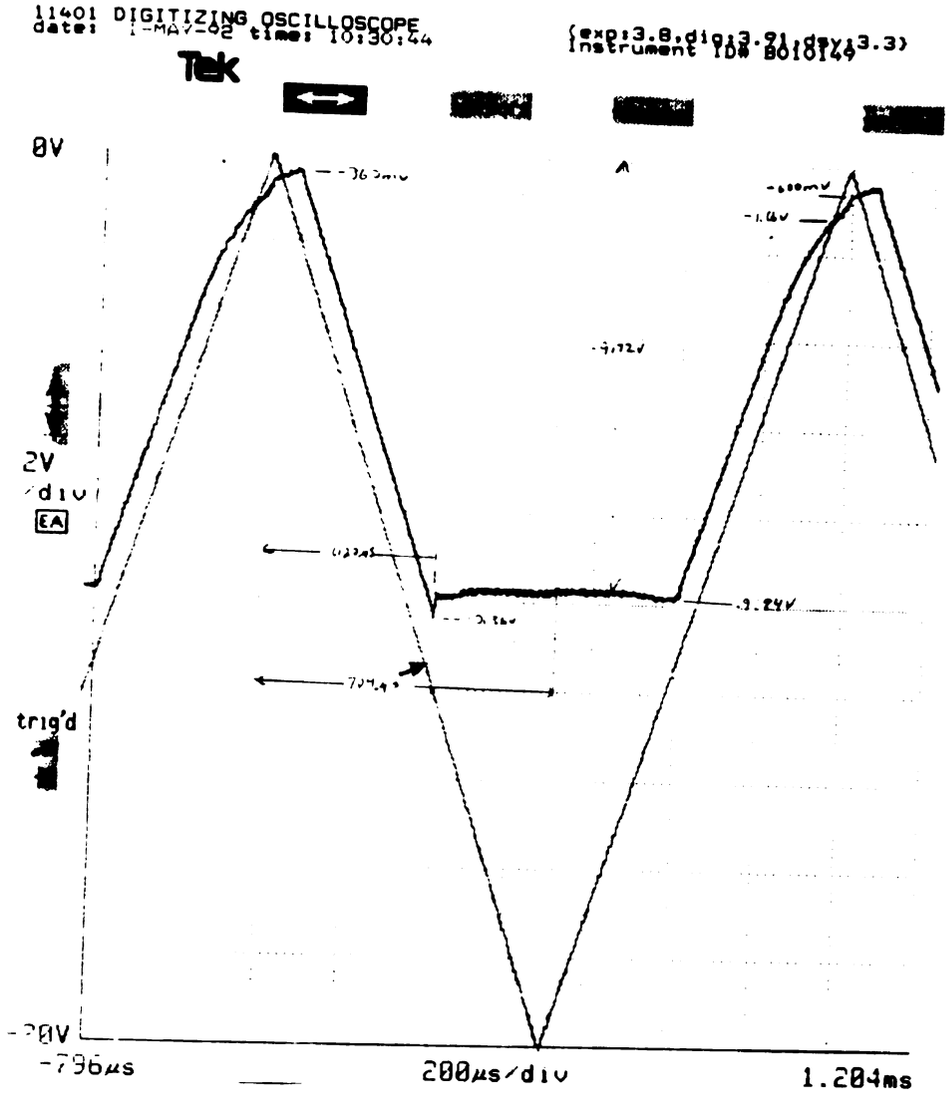

Figure 7.15 Power up and down, triangle wave, measured

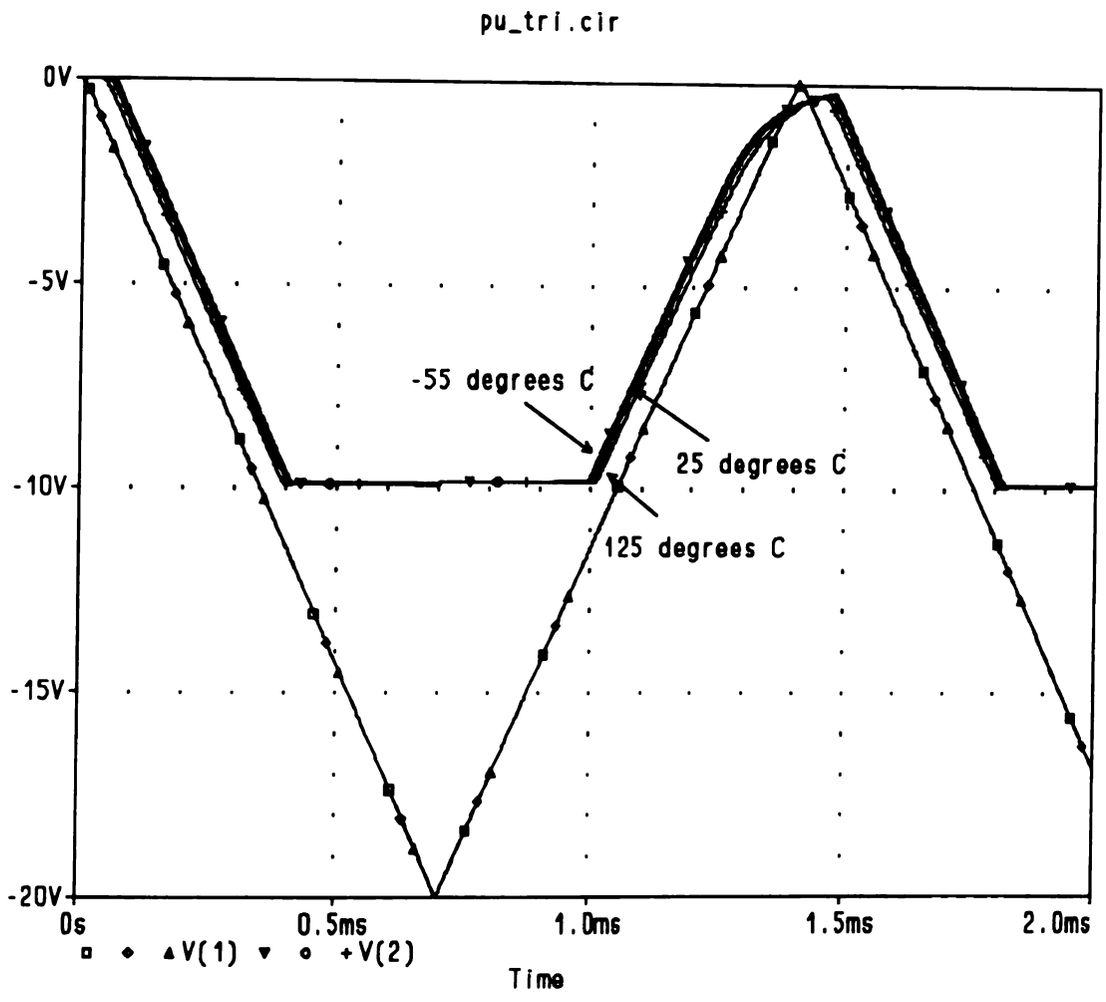

Figure 7.16 Power up and down, triangle wave, macromodel

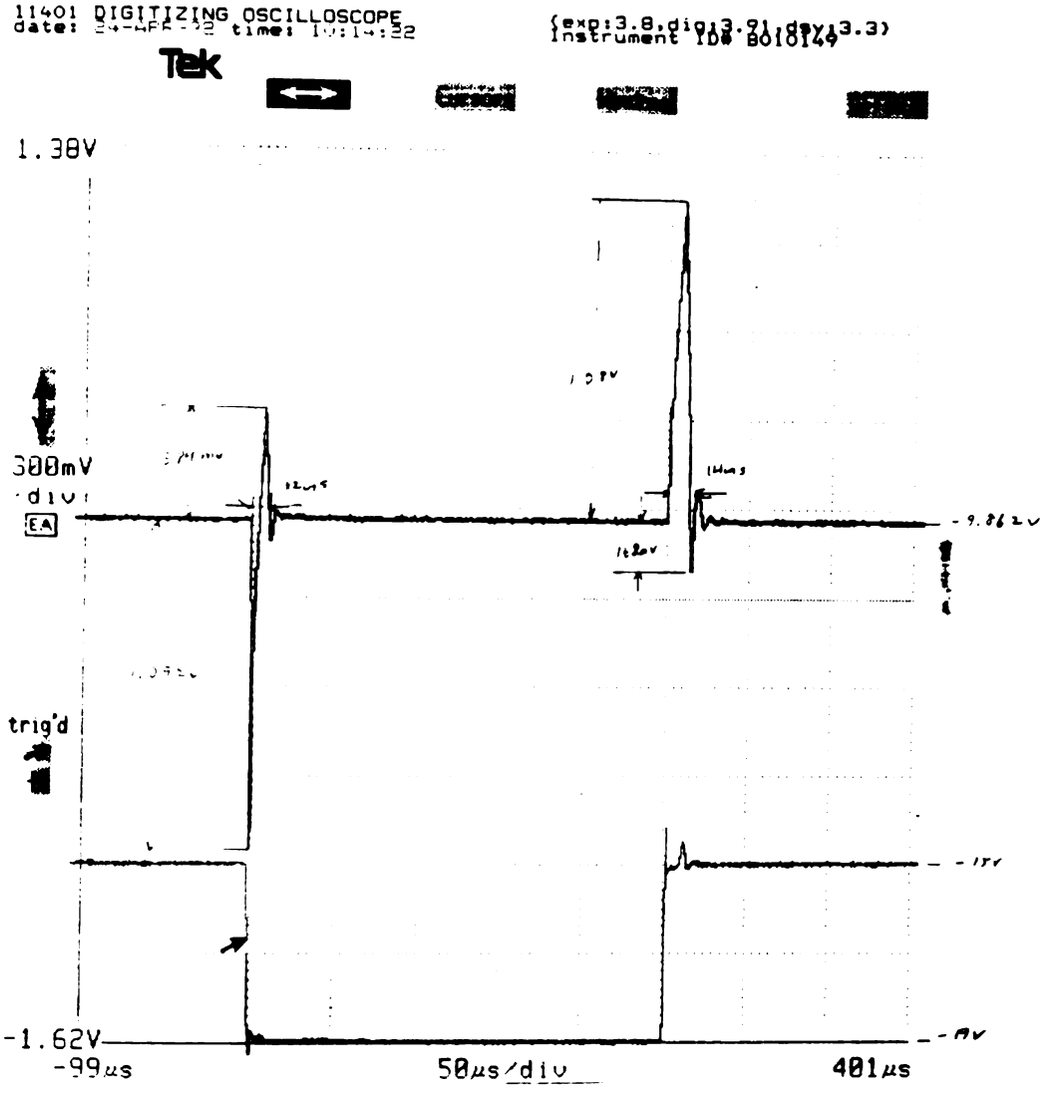

Figure 7.17 Line transient response, measured

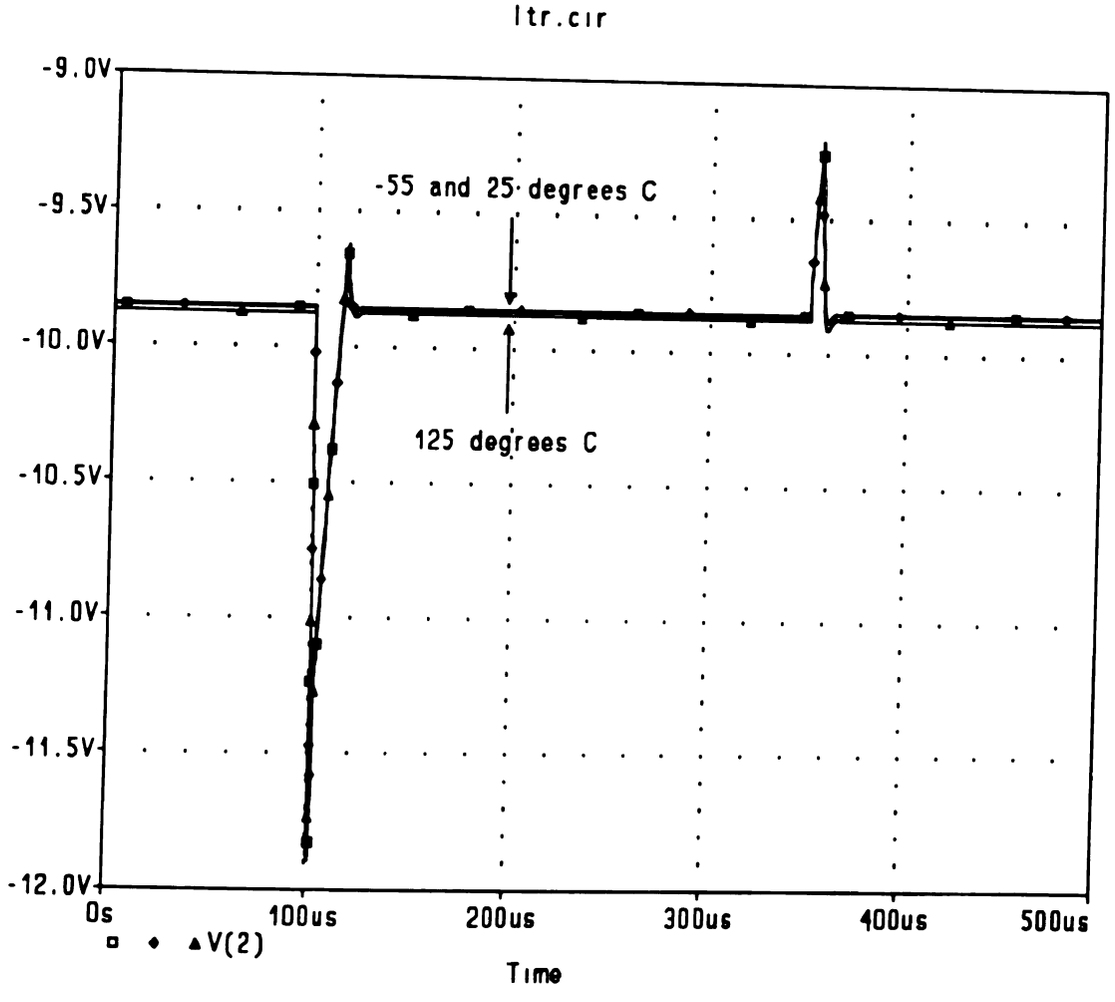

Figure 7.18 Line transient response, macromodel

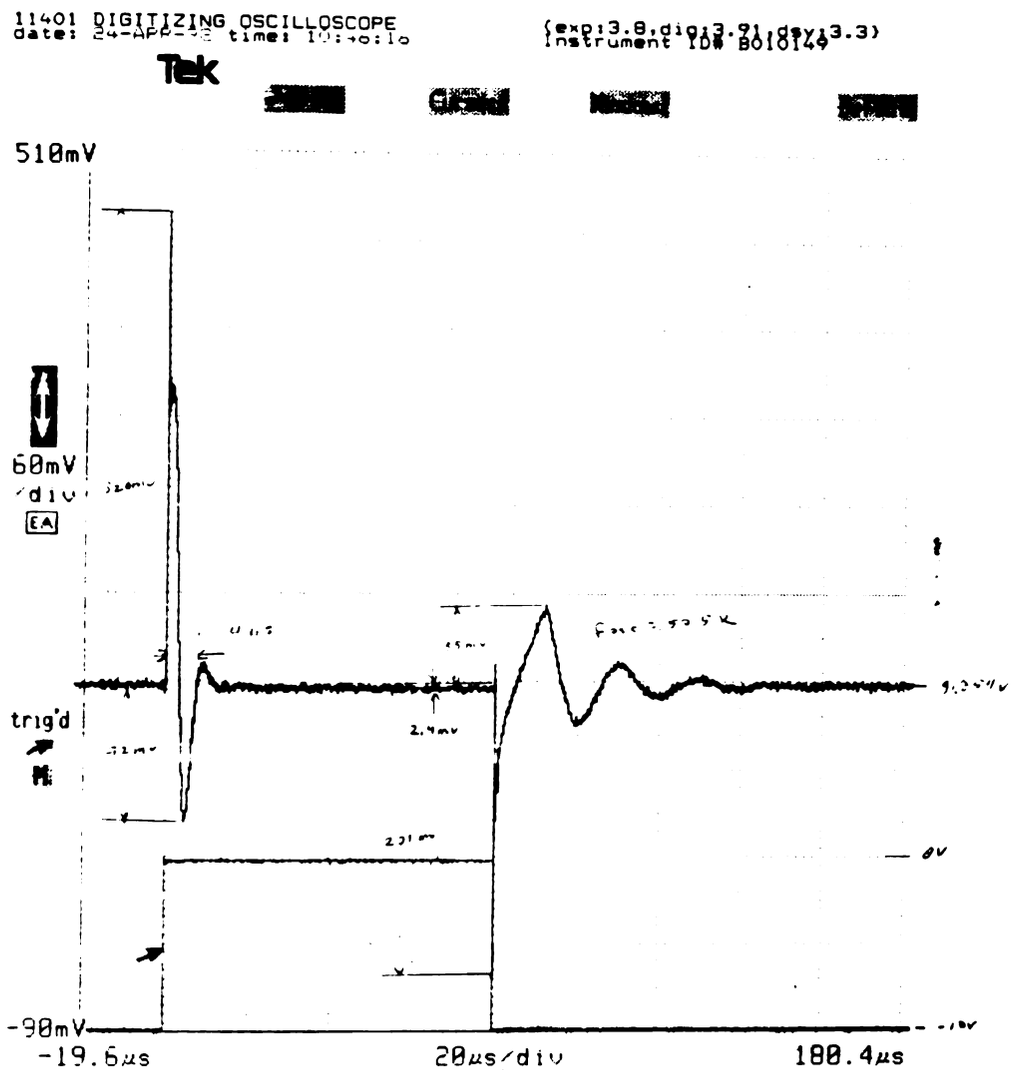

Figure 7.19 Load transient response, measured

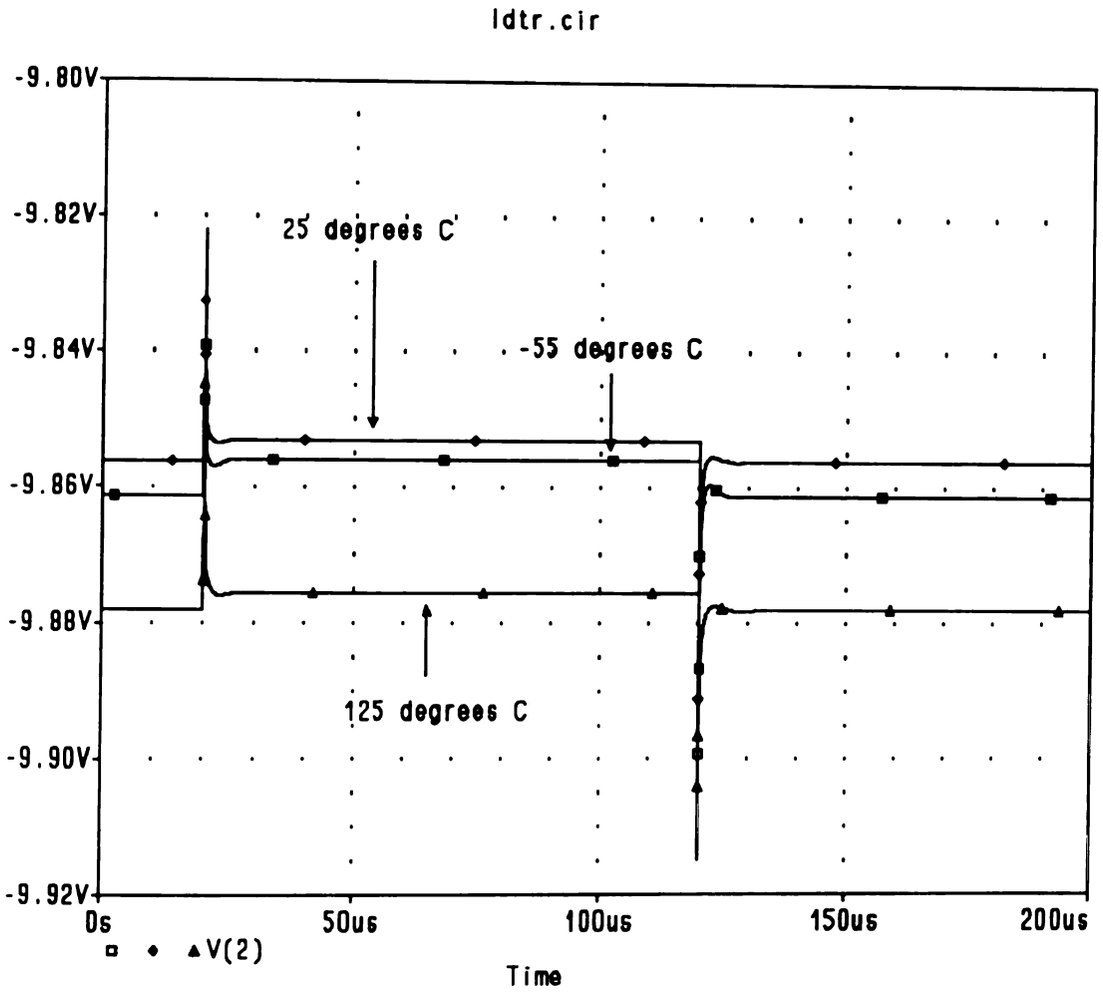

Figure 7.20 Load transient response, macromodel

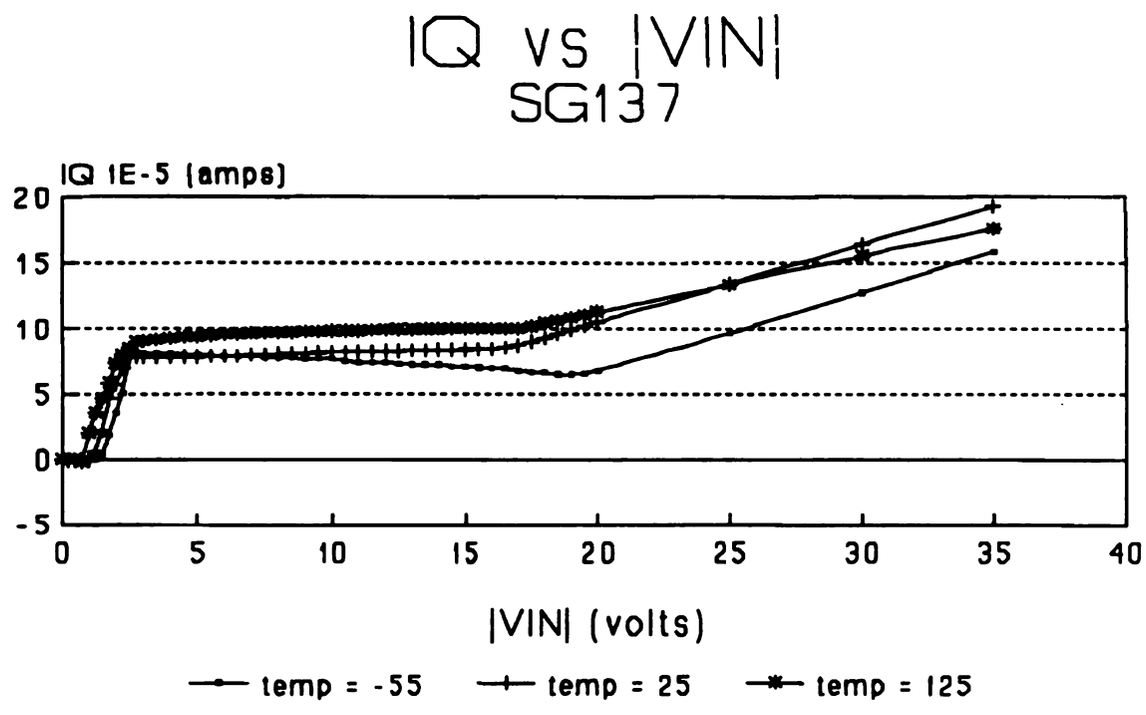

Figure 7.21 Quiescent current vs $|V_{IN}|$, measured

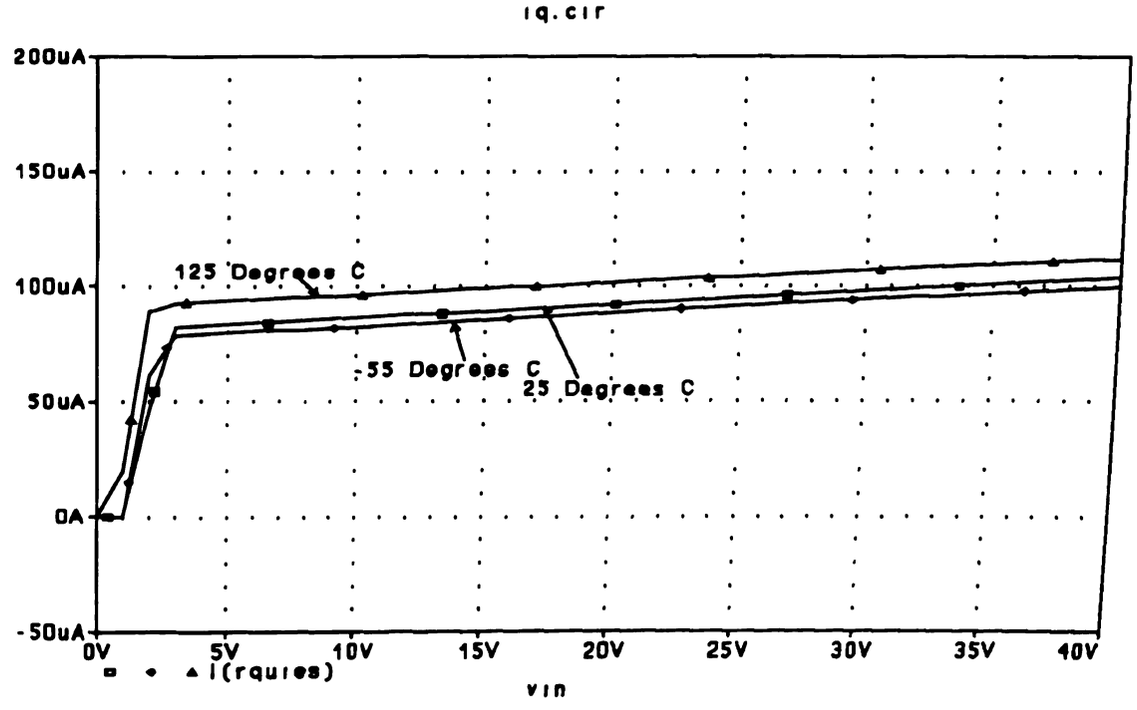

Figure 7.22 Quiescent Current vs $|V_{IN}|$, macromodel

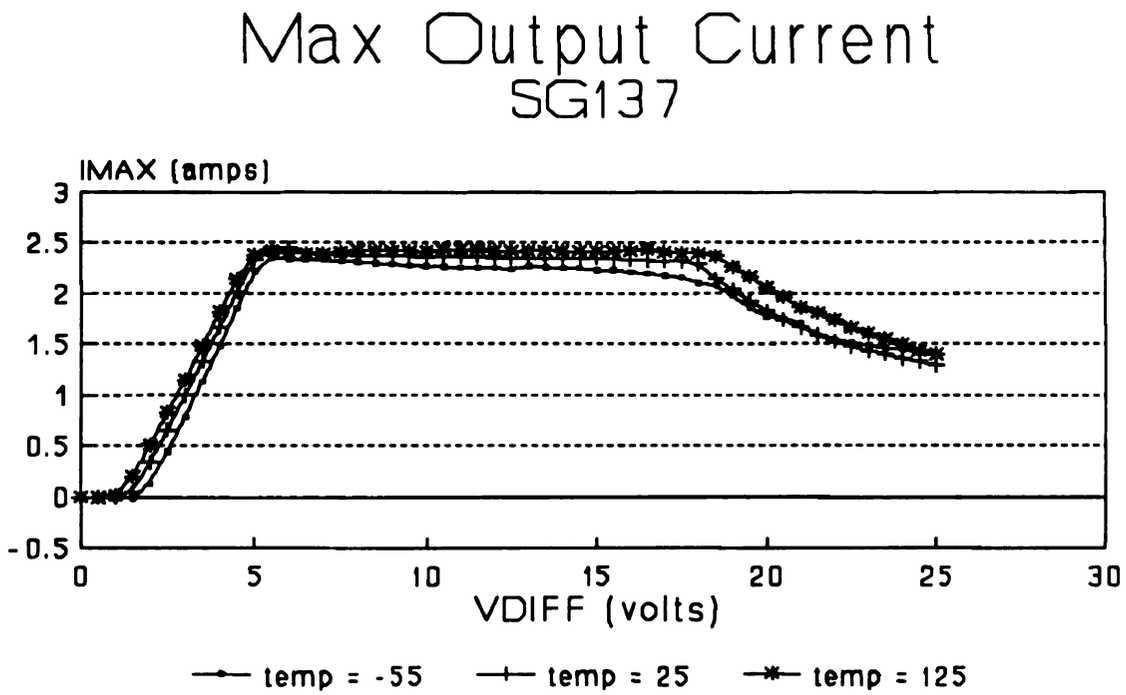

Figure 7.23 Maximum load current vs $|V_{IN}|$, measured

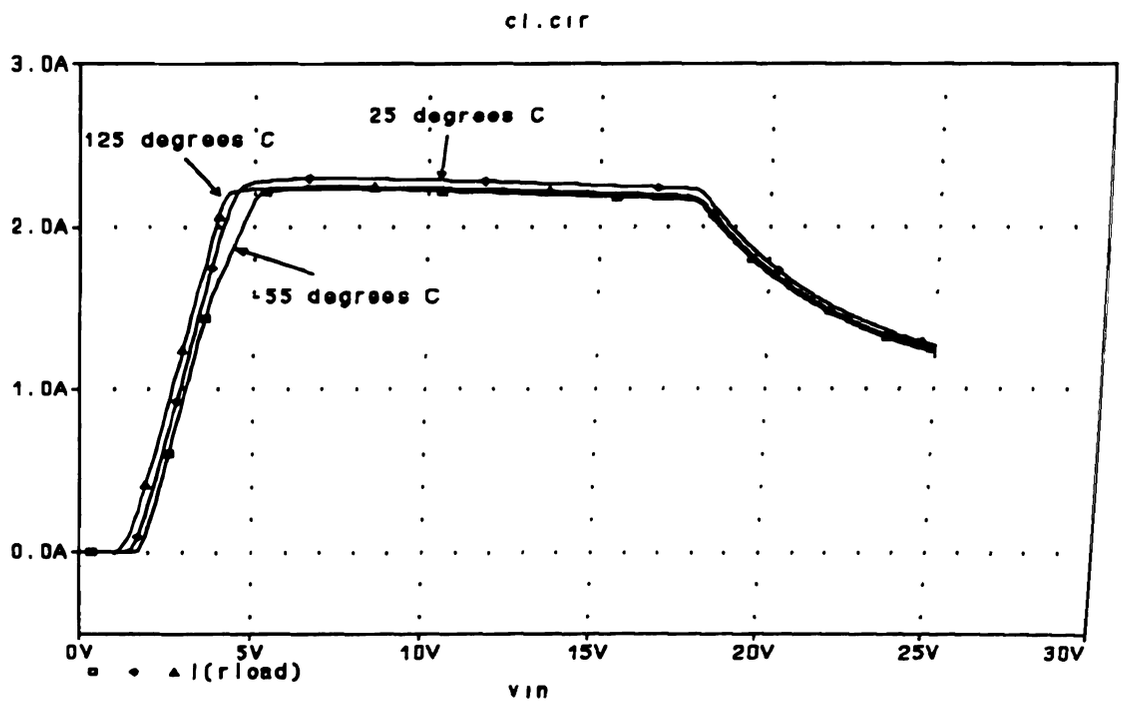

Figure 7.24 Maximum load current vs $|V_{IN}|$, macromodel

Comparison of Macromodel parameters and Measured Parameters				
QUANTITY		**-55°C**	**25°C**	**125°C**
RR_{LF}	lab	57.6db	60.8db	61.8db
	model	57.5db	60.8b	61.6db
$P1_{RR}$	lab	170Hz	120Hz	110Hz
	model	170.5Hz	120.4Hz	110.0Hz
IQ	lab	81.6uA	79.1uA	92.5uA
	model	82.2uA	78.5uA	92.6uA
$\Delta IQ/\Delta V_{IN}$	lab	.5699u	.5699u	.5173u
	model	.5765u	.5740u	.5225u
maximum load current	lab	2.36A	2.45A	2.41A
	model	2.24A	2.30A	2.25A
dropout voltage	lab	1.83V	1.16V	1.35V
	model	1.86V	1.64V	1.20V
R_{OUT}	lab	0.0410Ω	0.0193Ω	0.0102Ω
	model	0.0545Ω	0.0316Ω	0.0255Ω

Table 7.3 Macromodel comparisons with lab data

This concludes the comparison of the macromodel with lab results as well as the report for the development of the SG137 macromodel.

7.5 TEST CIRCUITS

7.5.1 Pspice Test Circuits

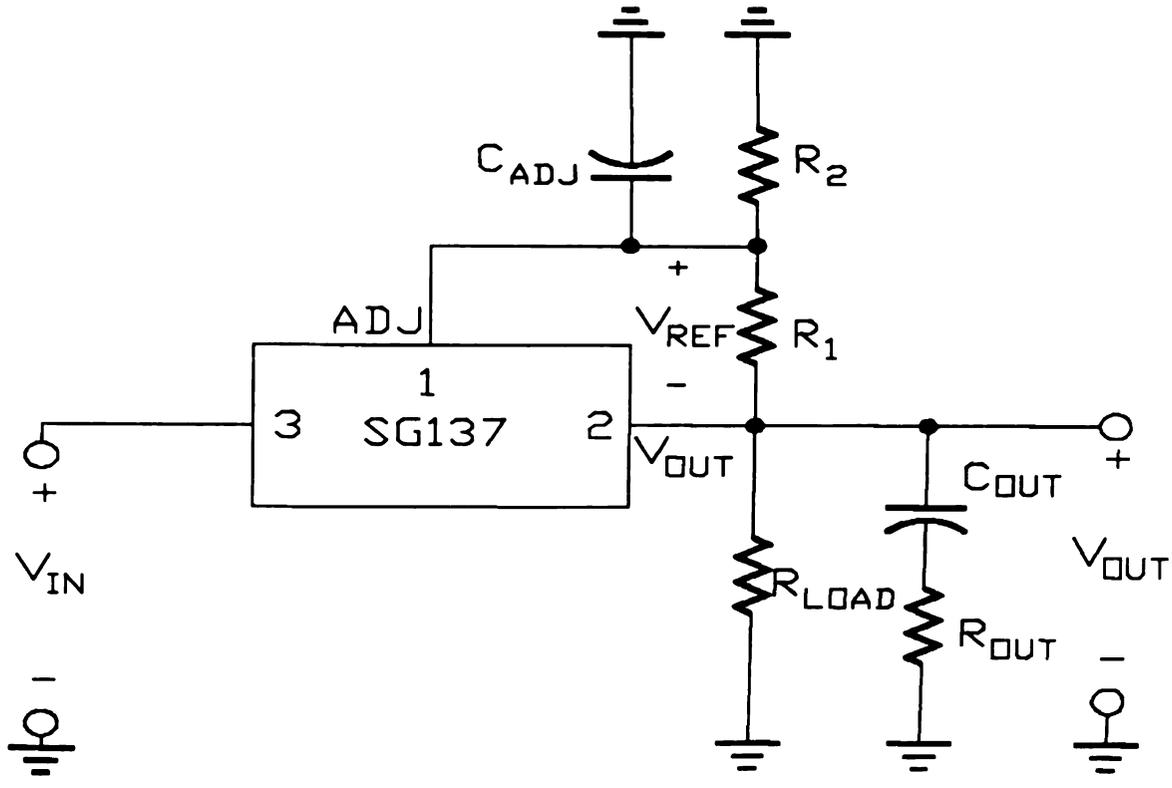

Figure 7.25 Basic PSpice test circuit

```
RR.CIR
*
*RIPPLE REJECTION FOR THE SG137
*
VIN     4 0 DC -15
VAC     1 4 AC 1
RLOAD   2 0 100.214
COUT    2 10 .9396u
ROUT    10 0 1.0953
R1      2 3 119.93
R2      3 0 820.13
CADJ    3 0 158.04p
XREG    3 2 1 sg137
.OP
.LIB SG137.LIB
.AC DEC 20 10 1MEG
.PROBE
.TEMP -55 25 125
.END


PU.CIR
*
*POWER UP AND DOWN, SQUARE WAVE FOR THE SG137
*
RLOAD   2 0 100.214
CLOAD   2 10 .9396u
RCLOAD  10 0 1.0953
R1      2 3 119.93
R2      3 0 820.13
CADJ    3 0 158.04p
X1      3 2 1 SG137
VP      100 0 PULSE (0 -15 100u 0 0 250u)
RVP     100 1 .1
.LIB SG137.LIB
.TRAN 1u 500u 0 1u
.TEMP -55 25 125
.PROBE
.END
```

```
PU_TRI.CIR
*
*POWER UP AND DOWN, TRIANGLE WAVE FOR THE SG137
*
ROUT    2 0 100.214
COUT    2 20 .9396u
RCOUT   20 0 1.0953
X1      3 2 1 SG137
R1      2 3 119.93
R2      3 0 820.13
CADJ    3 0 158.04p
VP  1 0 PULSE (0 -20 0u 700u 700u 1u 1410u)
.LIB SG137.LIB
.TRAN 2.5u 2000u 0 2.5u
.TEMP -55 25 125
.PROBE
.END


LTR.CIR
*
*LINE TRANSIENT RESPONSE FOR THE SG137
*
ROUT    2 0 100.214
COUT    2 10 .9396u
RCOUT   10 0 1.0953
X1      3 2 1 sg137
R1      2 3 119.93
R2      3 0 820.13
CADJ    3 0 158.04p
VIN     11 0 dc -15
VP      1 11 PULSE (0 -4 100u 0u 0u 250u)
.LIB SG137.LIB
.TRAN 1u 500u 0 1u
.TEMP -55 25 125
.PROBE
.END
```

```
LDTR.CIR
*
*LOAD TRANSIENT RESPONSE FOR THE SG137
*
VP      10 0 pulse (-9.8 0 20u 0 0 100u)
RLOAD   2 10 100.214
*RLOAD NOT GROUNDED, ONE PIN CONNECTED TO OUTPUT, THE OTHER TO
*VP
COUT    2 100 .9396u
RCOUT   100 0 1.0953
R1      2 3 119.93
R2      3 0 820.13
CADJ    3 0 158.04p
X1      3 2 1 sg137
VIN     1 0 dc -15
.TRAN .1u 200u 0 .1u
.TEMP -55
.LIB SG137.LIB
.PROBE
.END


IQ.CIR
*
*QUIESCENT CURRENT CHARACTERISTICS FOR THE SG137
*
VIN     0 1 DC 10
RQUIES  0 3 0.00001
RLOAD   0 2 100MEG
X1      3 2 1 SG137
.LIB SG137.LIB
.TEMP -55 25 125
.PROBE
.END
```

```
CL.CIR
*
*CURRENT LIMITING FOR THE SG137
*
VIN     0 1 DC -15
RLOAD   0 2 .9938
R1      2 3 119.93
R2      3 0 820.13
CADJ    3 0 158.04p
COUT    3 10 .9396u
RCOUT   10 0 1.0953
XREG    3 2 1 sg137
.DC VIN  0 25 0.1
.PROBE
.LIB SG137.LIB
.TEMP -55 25 125
.END


VDO.CIR
*
DROPOUT VOLTAGE FOR THE SG137
*
VIN     0 1 DC -15
RLOAD   2 10 100.214
R1      2 3 119.93
R2      3 0 820.13
CADJ    3 0 158.04p
COUT    3 10 .9396u
RCOUT   10 0 1.0953
XREG    3 2 1 sg137
.DC VIN  0 25 0.1
.LIB SG137.LIB
.PROBE
.TEMP -55 25 125
.END
```

7.6.2 Measurement Test Circuits

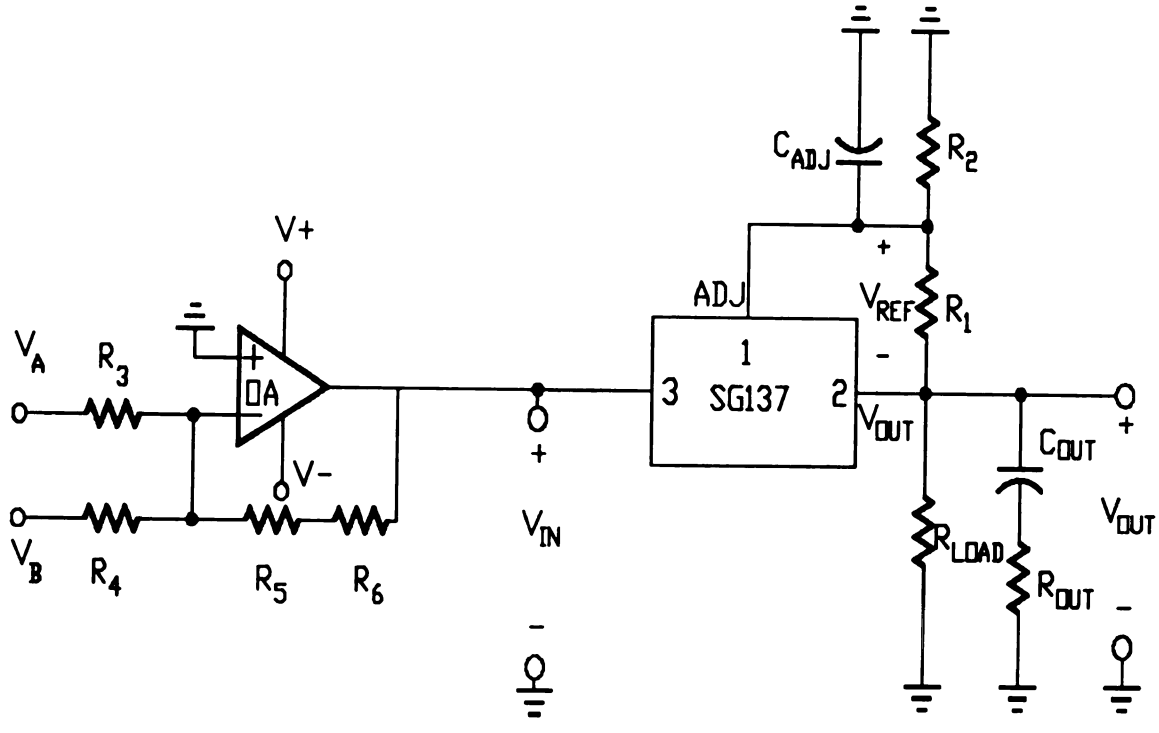

Figure 7.26 Test circuit No. 1

The conditions of test circuit No. 1 are stated.

R_1 measured 119.93Ω.
R_2 measured 820.13Ω.
C_{OUT} measured .9396uF at 100kHz.
R_{COUT} represents the series resistance of C_{OUT} and measured 1.0953Ω.
C_{ADJ} measured 158.04pF at 100kHz.
R_3, R_4, R_5, and R_6 have nominal values of 1kΩ.
V+ is a positive 10V dc power supply.
V- is a negative 50V dc power supply.
OA is a Burr-Brown OPA541 Op-Amp.
The SG137, R_1, R_2 reside inside a temperature chamber. Wires are connected at the terminals of the SG137 to allow it to be connected outside the chamber to the test circuit.

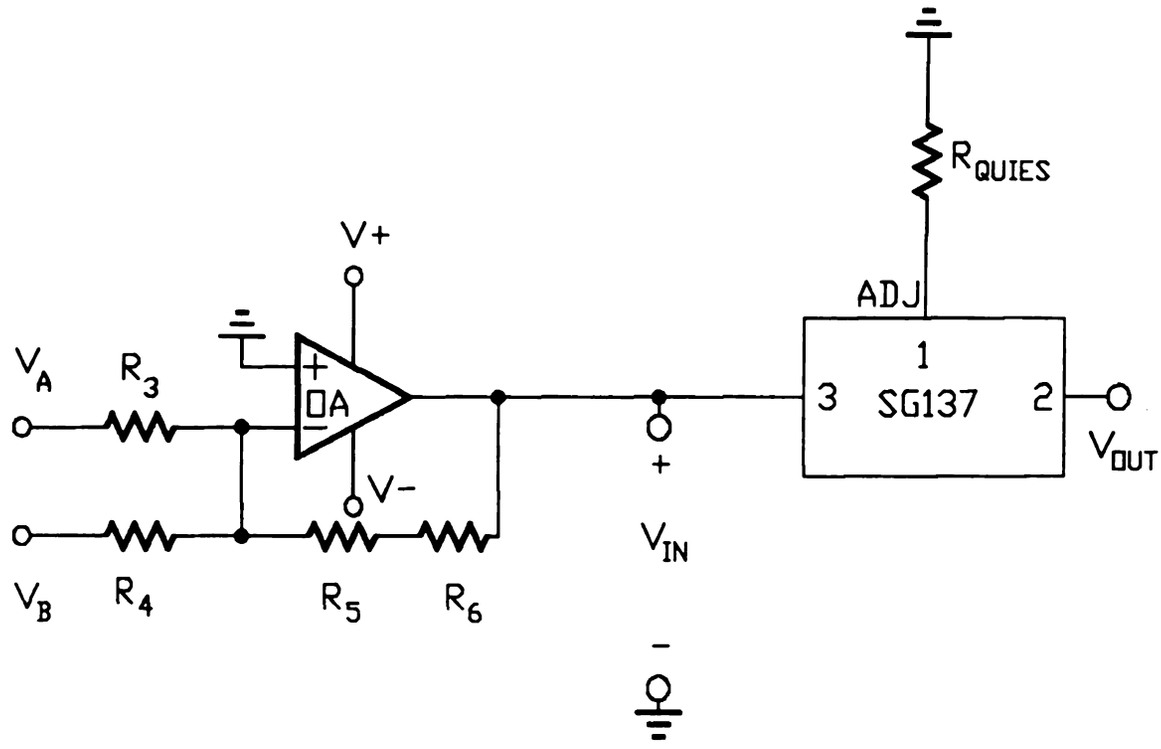

Figure 7.27 Test circuit No. 2

The conditions of test circuit No. 2 are stated.

R_3, R_4, R_5, and R_6 have nominal values of 1kΩ.
V+ is a positive 10V dc power supply.
V- is a negative 50V dc power supply.
OA is a Burr-Brown OPA541 Op-Amp.
The SG137 resides inside a temperature chamber. Wires are connected at the terminals of the SG137 to allow it to be connected outside the chamber to the test circuit.
R_{QUIES} has a nominal value of 100Ω.

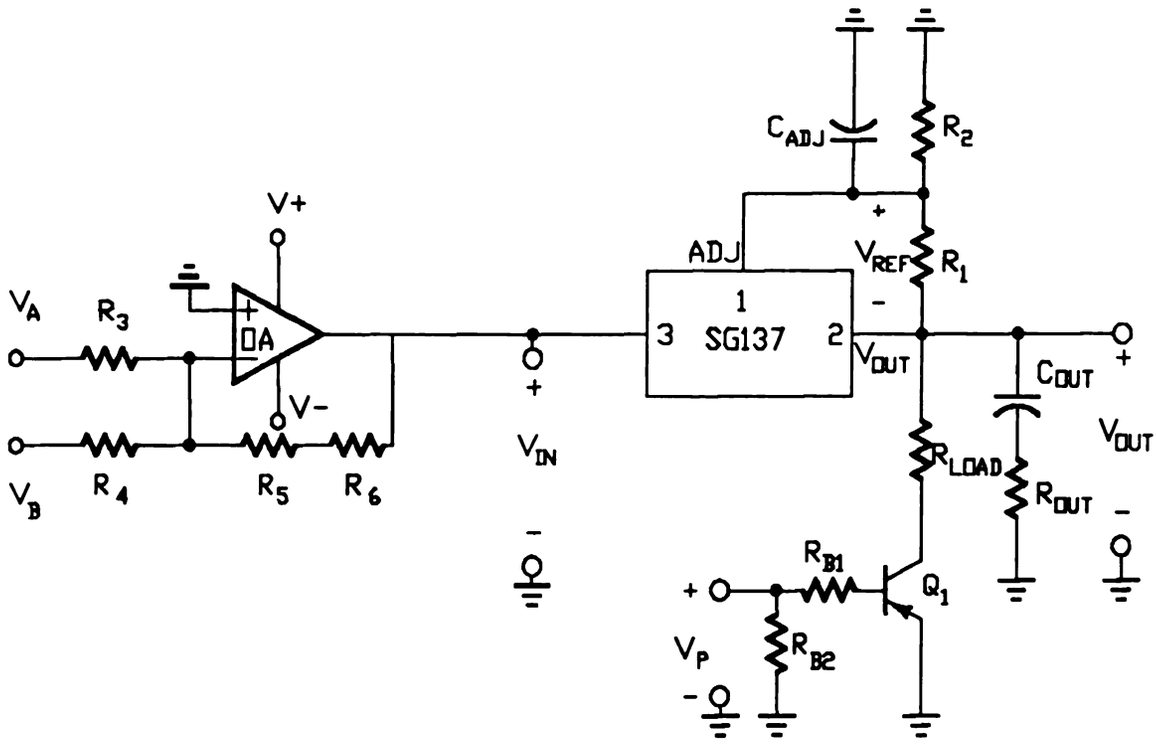

Figure 7.28 Test circuit No. 3

The conditions of test circuit No. 3 are stated.

R_1 measured 119.93Ω.
R_2 measured 820.13Ω.
C_{OUT} measured .9396uF at 100kHz.
R_{COUT} represents the series resistance of C_{OUT} and measured 1.0953Ω.
C_{ADJ} measured 158.04pF at 100kHz.
R_3, R_4, R_5, and R_6 have nominal values of 1kΩ.
V+ is a positive 10V supply.
V- is a negative 50V supply.
OA is a Burr-Brown OPA541 Op-Amp.
The SG137, R_1, R_2 reside inside a temperature chamber. Wires are connected at the terminals of the SG137 to allow it to be connected outside the chamber to the test circuit.
Q_1 is a 2N4403 pnp transistor.
R_{B1} has a nominal value of 10kΩ.
R_{B2} has a nominal value of 1kΩ.

1) Ripple rejection was done using test circuit 1. V_A was connected to an ac function generator. V_B was connected to a negative dc power supply. These were set to produce a -15V dc voltage at V_{IN}, with a sine wave superimposed. R_{LOAD} measured 100.214Ω. Voltages and phases were measured with a Tektronix 11401 scope.

2) The V_{IN} vs V_{OUT} and V_{OUT} at V_{IN} = -15V measurements were done using test circuit 1. V_A was connected to an pulse generator and pulsed at 100Hz, with a duty cycle of 5%. V_B was grounded. These were set to produce the necessary voltage at V_{IN}. R_{LOAD}, when used, measured 100.214Ω. Voltages were measured with a Tektronix 11401 scope.

3) The power up and down square wave measurements were done using test circuit 1. V_A was connected to an pulse generator. V_B was grounded. R_{LOAD} measured 100.214Ω. Voltages were measured with a Tektronix 11401 scope.

4) The power up and down triangle measurement was done using test circuit 1. V_A was connected to an ac function generator, generating a triangle wave. V_B was connected to a negative dc power supply. These were set to produce a triangle wave at V_{IN} which has a maximum value of 0V, and a minimum value of -20V. R_{LOAD} measured 100.214Ω. Voltages were measured with a Tektronix 11401 scope.

5) The quiescent current measurements were done using test circuit 2. V_A was connected to an pulse generator and pulsed at 100Hz, with a duty cycle of 5%. V_B was grounded. These were set to produce the necessary voltage at V_{IN}. R_{QUIES} measured 99.876Ω. Voltages were measured with a Tektronix 11401 scope. The voltage was measured across R_{QUIES} and divided by R_{QUIES} to give the quiescent current.

6) The load transient response measurement was done with test circuit 3. V_A was grounded. V_B was connected to a negative power supply to produce a dc voltage of -15V at V_{IN}. V_P was pulsed to allow Q1 to function as a switch, connecting R_{LOAD} on and off to ground to simulate the switching on and off of a load.

7) The maximum output current vs V_{IN} measurements were done using test circuit 1. V_A was connected to an pulse generator and pulsed at 100Hz, with a duty cycle of 5%. V_B was grounded. These were set to produce the necessary voltage at V_{IN}. R_{LOAD} .9938Ω. Voltages were measured with a Tektronix 11401 scope. The voltage measured at R_{LOAD} was then converted to a current.

8) The line transient response measurement was done with test circuit 1. V_A was connected to a pulse generator. V_B was connected to a negative dc power supply. These were set to produce a -15V dc voltage at V_{IN}, with a sine wave superimposed. R_{LOAD} measured 100.214Ω. Voltages were measured with a Tektronix 11401 scope.

CHAPTER 8

DESIGN ISSUES

8.1 INTRODUCTION

In this chapter, some of the issues which go into the macromodeling of voltage regulators are discussed. The issues are general issues of macromodeling, and can be applied macromodels of other IC's as well.

8.2 DESIGN ISSUES

The macromodeling problem can be broken up into three parts. They are:

1) starting point

2) modeled specifications

3) development to meet specifications

Although 1 and 2 seem simple, they are not. Many current macromodels violate good choices for 1 and 2. Part 3 is where the problem becomes most open ended, with numerous solutions.

8.2.1 Starting Point

The thesis shows that good macromodels are developed from a good choice of a starting point. The most reasonable choice is the functional block diagram [13]. It makes sense that if a model is functionally the same as the actual chip, that it behaves like the real chip. If the model is not functionally the same, it is unreasonable to assume that the model will perform like the actual chip. This is only common sense. An example of a chip which violates this idea is the MicroSim's

LM78XX macromodel. The chip assumes a grounded voltage reference, instead of the voltage reference existing between two internal nodes in the chip.

8.2.2 Modeled Specifications

This is another seemingly easy, but difficult task. Obviously, when a correct starting point has been chosen, a goal must be set. The goal is the choice of parameters to be modeled. In the case of the op-amp, a well known chip and widely used chip, it is easy. There are enough designers with enough op-amp experience so that it is relatively clear which parameters need to be modeled. An example of a chip in which it is not clear what to model is the voltage reference.

The chosen parameters should be suitable to define the chip. This helps guarantee that the model will work even when implemented in a topology which may be different from any topology that the model underwent during development. It is not clear how many parameters or characteristics can completely define the chip being modeled. It would be ideal, that if given a number of parameters, one could completely characterize the chip. Consider the linear 1-port network. Fundamental theory states that two measurements are necessary to completely characterize the linear one-port. These measurements are open circuit voltage measurement and short circuit current measurement. The equivalent circuit which results can be used in place of the linear 1-port. With a linear 2-port, four measurements are necessary, etc. Unfortunately IC's are non-linear devices with non-linear phenomenon, a problem that cannot be solved as easily as the linear networks, if at all. It is easy to choose 1 or 2 characteristics and have the macromodel mimic these characteristics with great accuracy. It is difficult to choose many parameters and have the model reflect all of them accurately.

Most importantly, the most critical characteristics of the devices should be modeled. For the voltage regulator, power up and down, and output resistance are the important parameters which must be modeled. In general, the modeled characteristics can come from several sources. These are data sheets, customer applications, personal experience, and personal curiosity. It was curiosity which lead to the measurement of the frequency response of the voltage reference inside the UA723. This lead to a great deal of insight. The other chosen characteristics came from the first three sources. When a decision has been made on what characteristics are to be modeled, the characteristics should be measured. The model is then based on measurement. Relying on data sheets is not good practice - as data sheets may be incorrect.

Finally, the user must select some tolerance for the characteristics. Even maturely developed macromodels can not completely meet specifications. There is a trade-off to be made on how much tolerance is realistic for the model to be useful and time invested in the model. Trade-offs will also occur between characteristics. Low frequency ripple rejection in the SG78XX was favored over line regulation, for example. Any of the macromodels presented here can model almost any parameter with almost zero percent tolerance, but at the cost of reducing the accuracy of other modeled characteristics. At some point, the user must decide when all of the parameters are modeled with reasonable accuracy.

8.2.3 Developing the Macromodel

Once the starting point and ending goal have been defined, the starting point is developed to meet the desired specifications. Ideally, it is desirable to replace each functional block with an equivalent circuit for that actual functional block which

behaves like that functional block for all linear and non-linear behavior. The voltage reference in the CA3085 is an example of this. Because we were able to measure the reference, the reference which replaced it had almost identical ac and dc response to the actual reference. Instead of a differential amplifier, or some other type of error amplifier, a voltage controlled voltage source with some gain and clamping is seen to work well with all of the macromodels. Darlington output pair transistors can frequently be replaced by one pass transistor. Most of the maximum output current structures are also identical to what may be found in the actual chip. Optimally, the functional blocks are replaced with circuits which are less complicated, easier to understand, and have fewer components.

At times, it may be necessary to model phenomenon by adding in components which have actually no physical meaning inside the chip. The maximum output current of the SG137 is an example of this. Perhaps, to a degree, adding an output resistor to model output resistance is also an example of this. Caution must be exercised when using this technique. This technique deviates the model from a functional block approach. It works well in the SG137 because the short circuit current circuitry is normally off and does not affect the circuit under normal operating conditions.

Once the structure has been developed, choosing component values presents yet another problem. Techniques in choosing component values range from empirical to symbolic. The symbolic techniques are beyond the scope of this dissertation. Ideally, each component would be chosen by formula. These formulas would be derived from the measured characteristics.

The guidelines presented are some fundamental guidelines which can bring a

macromodeling problem to a manageable technique.

CHAPTER 9

CONLUSIONS

This dissertation presents the development of five voltage regulator macromodels. The macromodels are developed for use in the circuit simulator PSpice. The models developed are for five representitive topologies in the voltage regulator family.

Chapter 3 gives the development the macromodels for the SG7805 and SG7812 voltage regulators. This represents a model for a fixed, three terminal, positive voltage regulator. Chapter 4 gives the development of the SG7915 voltage regulator macromodel. This represents a model for a fixed, three terminal, negative voltage regulator. Chapter 5 and 6 gives the development of the UA723 and CA3085 voltage regulators. These are programmable, positive, 8 and 10 terminal devices. Finally, Chapter 7 gives an example of an adjustable, three terminal, negative voltage regulator. These regulators can easily be adapted to other models of voltage regulators sharing the same functional blocks.

For each model, the room temperature model is developed, as well as models for -55°C and 125°C. This represents the range of military temperature specifications. For a much stronger temperature dependent model, data would be gathered for more temperatures. The parameters of the macromodels would then be fitted to this set of temperature data. The temperature set used in this dissertation represented a set of three data points. Three points were chosen because of many of the PSpice defined temperature variable parameters had a built in quadratic dependence. Also, the three

points represented a complete range of temperatures. However, in many circumstances the temperature dependent phenomenon is well behaved, and not much more than a "three-point" curve fit is required. The temperature work presented lays the basis for much stronger temperature modeling.

Chapter 8 provides some useful ideas and guidelines that were used in designing the macromodels.

The future of macromodelling lies in the ability to systematically generate accurate macromodels which reflect ambient as well as self-heating effects. The macromodels must be conceptually easy to understand as well. Macromodeling needs for its advancement the following.

Continued advancement in the area of computer-aided design of electronic circuits. It is stated in the first chapter, that computer simulations are not a replacement for breadboarding. Development must proceed along the path of bridging the gap between breadboarding and computer simulation. This is an enormous task, however the path is clear. When this happens, more circuit designers can use a macromodel for an IC or a number of IC's in a computer simulation and make confident decisions based on the simulation results.

Computer simulators, in particular, PSpice needs more development. In macromodeling, more flexibilty is desirable. Consider for example the limitation of the quadratic temperature dependence of the passive components. If an unlimited order were available, more accurate temperature models could be generated. Complex user defined devices should also be available, although this is somewhat available with the device equations options in PSpice.

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