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thesis entitled

OP AMP MACROMODELS

presented by

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has been accepted towards fulfillment
of the requirements for

Master's degree in Electrical Engineering

Major professor

Date July 17, 1992

OP AMP MACROMODELS

By

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A THESIS

Submitted to
Michigan State University
in partial fulfillment of the requirements
for the degree of

MASTER OF SCIENCE

Department of Electrical Engineering

1992

ABSTRACT

OP AMP MACROMODELS

BY

Raoudha Hamza

In this thesis, the circuit analysis and basic operations of two different op amp macromodels are described. One is called microsim model and the other one is called linear technology model. Some macromodel design procedures are presented, that enables the macromodel parameters to be found from typical data sheet or easily measured characteristics. Numerical examples are included using the μA741, LM124, LF411, LF355 and LTC1050. Some inaccuracies of the two models are explained followed by the device level performance. Finally some improvements of these models are proposed. The improvements include supply current, power supply rejection ratio, clipping voltage and common mode rejection ratio.

To my parents and my dear husband.

ACKNOWLEDGMENTS

My gratitude to professor G.M. Wierzba for his guidance and assistance in completing this thesis.

My appreciation to Shoba Krishnan for her help in drawing the diagrams.

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CHAPTER 1

Introduction

1.1 Introduction

Electronic circuit simulators have certain limitations, such as the maximum number of nodes, devices, elements, etc. These limitations are established either by memory limitations or convergence problems. Even if adequate simulaters and computers are available, nowadays the required simulation time makes the analysis impractical for the design engineer. Therefore, the idea and use of macromodels in electronic design arose since 1970's. The purpose of the op amp macromodel is to provide an adequate pin for pin representation of op amp and to represent the electrical characteristics of the operational amplifier. Since the macromodel components are selected based on data sheet specifications, this allows the designer to accurately model a specific IC based on laboratory measurements.

A macromodel for all bipolar operational amplifier was developed by G.R Boyle, B.M cohn, D.O. Pederson and J.E Solomon [1]. This macromodel is referred to it as the Boyle model. Since this paper was published, the area of op amp macromodeling has been of interest to many SPICE users [6], [9], [2]. Later on the MOS bipolar and JFET

bipolar op amps were presented based on the original Boyle model [3] and others have worked on improving the Boyle model such as in [11], [9], [4], [2]. In all the work, the design procedures were not developed and sometimes even the design formulas were not derived such as in [9], [2]. The main focus of this thesis is to present a complete analysis of two macromodels one called the microsim model [9] and the other one is called the linear technology model [2]. These two models were published with no design formulas or design procedure. This thesis includes all the necessary design formulas of these two macromodels. A design procedure is established so that given the op amp specifications one can determine its macromodel parameters in a systematic way.

1.2 Boyle Model

The circuit diagram of the op amp Boyle macromodel is shown in Fig. 1.1. This model is divided into three stages. The input stage consists of two ideal transistors, sources and some passive elements. This stage produces the necessary linear and non-linear differential mode (DM) and common mode (CM) input characteristics. In addition, this stage is designed to have a unity voltage gain to reduce the complexity of the design equations. The intermediate stage produces the DM and CM voltage gain. Also a capacitance c_2 is used at this stage to control the frequency and slew rate performances. The output stage provides a dc and ac output resistance for the op amp, the desired output voltage swing limits and is responsible for limiting short circuit output current. Since then, this strategy has been adapted by most of the op amp macromodels with of course

some improvements.

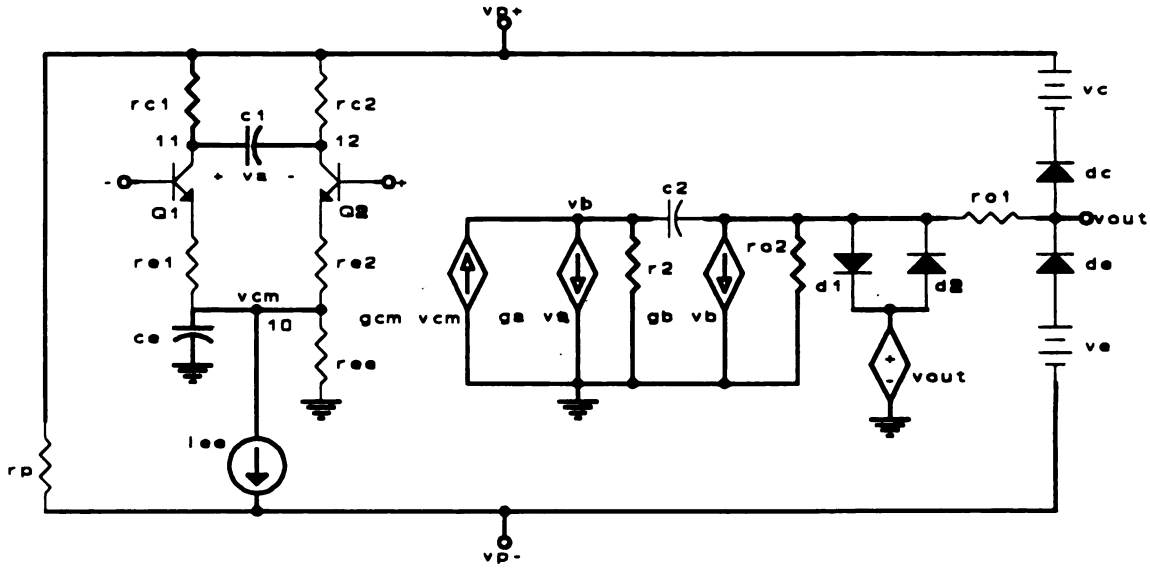

Figure 1.1 Boyle macromodel

1.3 Thesis Summary

This thesis concentrates on the analysis of two different designs of op amp macromodel: one called the microsim model, in chapter 2 and the other one called the linear technology model, in chapter 3.

Chapter 2 itself includes three different types of op amp macromodels: npn input stage macromodel (μA741), pnp input stage macromodel (LM124), n-channel JFET input stage marcomodel (LF411).

Chapter 3 also includes two different types of op amp macromodels: p-channel

JFET input stage macromodel (LF355), PMOS bipolar input stage macromodel (LTC1050).

In each of these chapters, the schematic diagram and its corresponding SPICE file of each op amp macromodel are provided followed by a set of SPICE test circuits to measure some of the typical op amp macromodel characteristics. Then, the design equations of each macromodel are derived with details which allows us to develop a systematic general design procedure for each type. Finally, a numerical example is used to verify the accuracy of the derived design equations by comparing the calculated measurements with the simulated ones.

Chapter 4 includes some models inaccuracies and some improvements to the two models.

Chapter 5 includes the conclusion and further research.

CHAPTER 2

Microsim Model

2.1 Introduction

In this chapter, the structure and basic operations of an op amp macromodel called the microsim model are described. The schematic diagram of an npn bipolar input stage macromodel (μA741) is shown in Fig. 2.1 as well as its SPICE file in Table. 2.1 [9]. The choice of the macromodel parameters are determined and explained later in other sections. This macromodel is designed by using elements inherent to SPICE such as ideal controlled source stages instead of transistors, and generally minimizes the number of pn junctions [1]. Two basic controlled sources dominate the microsim model: the voltage controlled voltage source (VCVS) and the voltage controlled current source (VCCS). This macromodel should represent the circuit behavior of an IC op amp for nonlinear dc, ac, and large signal transient responses.

The microsim model is fundamentally similar to the Boyle model [1] but with further adaptation such as the intermediate stage and the short circuit current limiter. However, the input stage and the voltage limiting circuit remain almost the same.

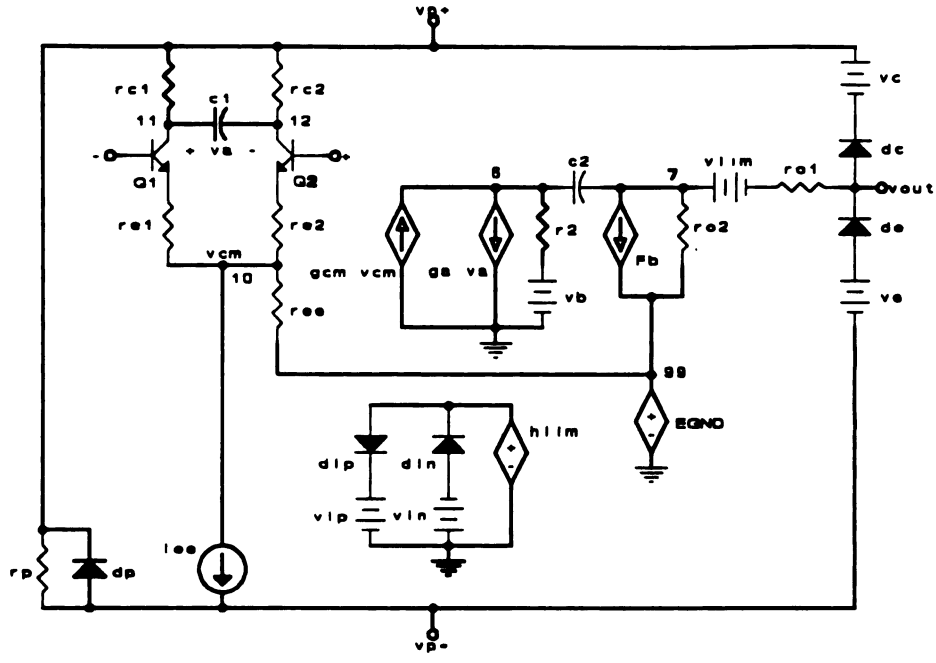

Figure 2.1 Microsim macromodel of the μA741

Table 2.1 SPICE file of the μA741 macromodel

```
*CONNECTIONS: + - VP+ VP- VOUT
.SUBCKT UA741 1 2 3 4 5
C1 11 12 8.661E-12
C2 6 7 30.00E-12
DC 5 53 DX
DE 54 5 DX
DLP 90 91 DX
DLN 92 90 DX
DP 4 3 DX
EGND 99 0 POLY(2) (3,0) (4,0) 0 .5 .5
FB 7 99 POLY(5) VB VC VE VLP
+ VLN
+ 0 10.61E6 -10E6 10E6 10E6 -10E6
GA 6 0 11 12 188.5E-6
GCM 0 6 10 99 5.961E-9
IEE 10 4 DC 15.16E-6
HLIM 90 0 VLIM 1K
Q1 11 2 13 QX
Q2 12 1 14 QX
R2 6 9 100.0E3
RC1 3 11 5.305E3
RC2 3 12 5.305E3
RE1 13 10 1.836E3
RE2 14 10 1.836E3
REE 10 99 13.19E6
RO1 8 5 50
RO2 7 99 100
RP 3 4 18.16E3
VB 9 0 DC 0
VC 3 53 DC 1
VE 54 4 DC 1
VLIM 7 8 DC 0
VLP 91 0 DC 40
VLN 0 92 DC 40
.MODEL DX D(IS=800.0E-18 RS=1)
.MODEL QX NPN(IS=800.0E-18
BF=93.75)
.ENDS
```

2.2 Circuit Component and Operation

The microsim model can be divided into three basic building blocks: input stage, intermediate stage and output stage which includes the short circuit current and voltage limiting. Each stage provides a certain characteristic.

2.2.1 Input stage

The input stage consists of two ideal transistors Q_1, Q_2, resistances, a capacitance c_1 and a current source noted I_{ee} or I_{ss}. This stage produces the necessary linear and nonlinear differential mode (DM) and common-mode (CM) input characteristics and it is isolated from the rest of the stages to simplify the modeling of the slew rate and frequency response [3]. For simplicity and design flexibility, the input stage gain was chosen to be unity [1]. This normalization step increases the utility of the model by simplifying design expressions for gain bandwidth product as shown in the model formulas section. In addition, this unity gain enables other structures to be implemented such as pnp and JFET input stages without changing the basic design equations [2]. Also the two transistors are modeled in the SPICE with their simplest models which does not include internal capacitances or resistances.

2.2.2 Intermediate stage

The elements g_a, g_{cm}, F_b, r_2, r_{o2} and c_2 provide the DM and CM op amp gain and vary the frequency response characteristics. The capacitance c_2 is used to provide the necessary ac output resistance change with frequency [1].

2.2.3 Output stage

The output stage provides a dc and ac output resistance of the op amp by the two resistances r_{o2} and r_{o1}.

The short circuit current limiting which provides the desired maximum short circuit current, I_{sc}, consists of two diodes d_{lp}, d_{ln}, two dc voltage souces v_{lp}, v_{ln} and a controlled voltage source h_{lim} which is controlled by the current flowing through r_{o1}. The elements d_{lp}, v_{lp} provide the positive short circuit current I_{sc+}, while d_{ln}, v_{ln} provide the negative short circuit current I_{sc-}.

The elements d_c, v_c and d_e, v_e provide voltage clamp circuits where the pair d_c, v_c is for the positive voltage clamp and d_e, v_e is for the negative voltage clamp.

2.3 Preview

The focus of the rest of the chapter is on developing expressions for the values of the elements in the macromodel. This is done because the design formulas for this model have not been published. The starting point is to use SPICE simulations of a given

macromodel to establish the basic design equations. Then, a general procedure is developed for the prameter and element values in the macromodel. Finally, the last step is to check the design procedure by using a numerical example. This analysis is done for a three different input stage macromodels: npn input stage macromodel (μA741), pnp input stage macromodel (LM324) and n-channel JFET input stage macromodel (LF411).

2.4 The NPN Bipolar Input Stage Macromodel

One of the npn bipolar input stage macromodels is the μA741. The schematic diagram is shown in Fig. 2.1 and the corresponding SPICE file is shown in Table 2.1. Also, the schematic diagram shown in Fig. 2.2 is of the μA741 full device op amp and its corresponding SPICE file is in Table 2.2.

2.4.1 SPICE test circuits

The SPICE test circuits are established using the μA741 macromodel. Since, the μA741 full device is available, then there are additional SPICE test circuits to compare the full device with its macromodel. The SPICE test circuits include transfer characteristics, input bias and offset currents, open loop gain, output impedance, common mode gain, short circuit current and slew rate.

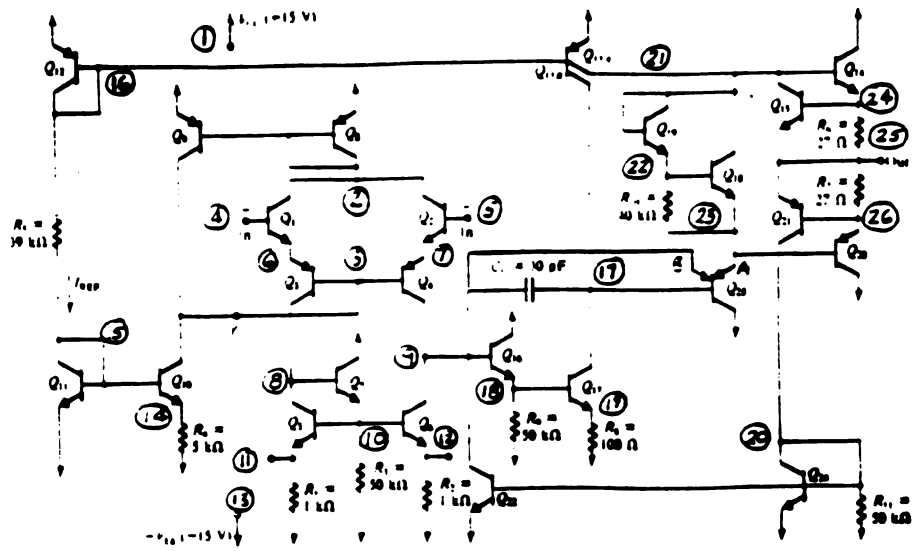

Figure 2.2 μA741 full device

Table 2.2 SPICE file of the μA741 full device

```
.SUBCKT UA741 4 5  1  13  25
*             + - Vp+ Vp- Vout
Q1 2 4 6 13 M1
Q2 2 5 7 13 M1
Q3 8 3 6 13 M2
Q4 9 3 7 13 M2
Q5 8 10 11 13 M1
Q6 9 10 12 13 M1
Q7 1 8 10 13 M1
Q8 2 2 1 13 M2
Q9 3 2 1 13 M2
Q10 3 15 14 13 M1
Q11 15 15 13 13 M1
Q12 16 16 1 13 M2
Q13A 21 16 1 13 M2 .25
Q13B 17 16 1 13 M2 .75
Q14 1 21 24 13 M1  3
Q15 21 24 25 13 M1
Q16 1 9 18 13 M1
Q17 17 18 19 13 M1
Q18 21 22 23 13 M1
Q19 21 21 22 13 M1
Q20 13 23 26 13 M2 3
Q21 20 26 25 13 M2
Q22 9 20 13 13 M1
Q23A 13 17 23 13 M2
Q23B 13 17 9 13 M2
Q24 20 20 13 13 M2
R1 11 13 1K
R2 12 13 1K
R3 10 13 50K
R4 14 13 5K
R5 16 15 39K
R6 24 25 27
R7 25 26 22
R8 19 13 100
R9 18 13 50K
R10 22 23 40K
R11 0 13 50K
CC 17 9 30P
.MODEL M1 NPN (BF=200 IS=1E-14
+ VAF=125 VJS=.75 RB=185 RC=15
+ CJE=.65P CJC=.36P TF=1.15N
+ TR=405N CJS=3.2P MJS=.5)
.MODEL M2 LPNP (BF=50 IS=1E-14
+ VAF=50 VJS=.75 RB=500 RC=150
+ CJE=.1P CJC=1.05P TF=27.4N
+ TR=2540N CJS=5.1P MJS=.5)
. ENDS
```

2.4.1.1 Transfer characteristics

The circuit used for the transfer characteristics test is shown in Fig. 2.3a. Using the cursor in SPICE, one can determine the input offset voltage, v_{io} by reading the input when the output is zero. Fig. 2.3b shows the transfer curve for the macromodel where the input offset is measured to be -19.17 μV and the saturation voltages are v_{out+} = 14.45 V and v_{out-} = -14.46 V. Also Fig. 2.3b shows the full device response where the input offset voltage is measured to be 327 μV, v_{out+} = 14.3 V and v_{out-} = -12.77 V.

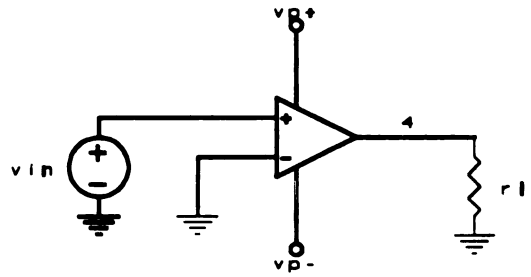

Figure 2.3a Test circuit for dc transfer curve

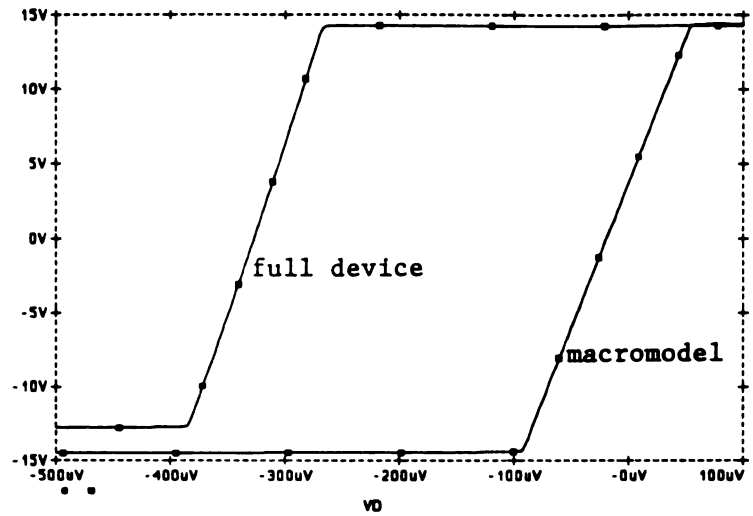

Figure 2.3b dc transfer curve

2.4.1.2 Input bias and offset currents

Consider the circuit test of Fig. 2.3a. The input offset current, I_{io} is the difference between the current at the positive and negative input of the op amp. In other words, it is the difference between the base currents of the two bipolar transistors Q_1, Q_2 at the input stage [7]. The bias current, I_B is the average of the two input currents [7]. Fig. 2.4a shows the base currents for the macromodel where I_{B+} = 79.66 nA, I_{B-} = 79.82 nA. I_{B+} is the current at the positive input and I_{B-} is the one at the negative input of the op amp. Then, I_{io} = 0.16 nA. Fig. 2.4b shows the full device response where I_{B+} = 33.89 nA and I_{B-} = 34.12 nA, then, I_{io} = 0.23 nA and I_B = 34.005 nA.

2.4.1.

the *gain*

full devi

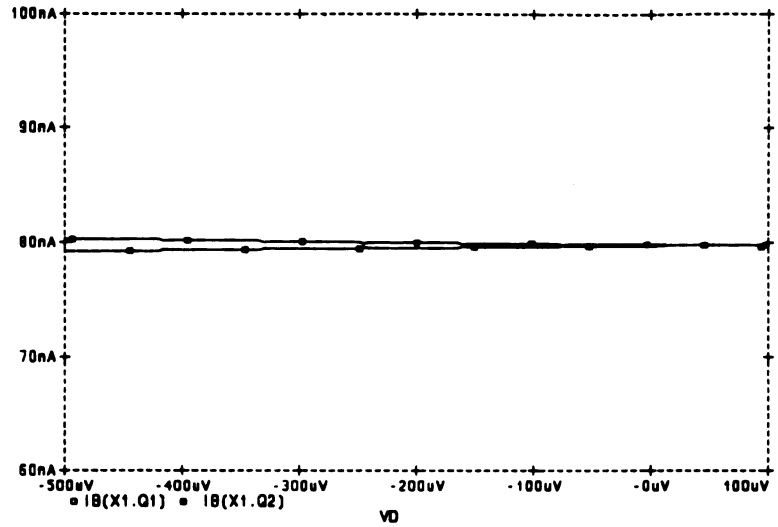

Figure 2.4a Input bias current (macromodel)

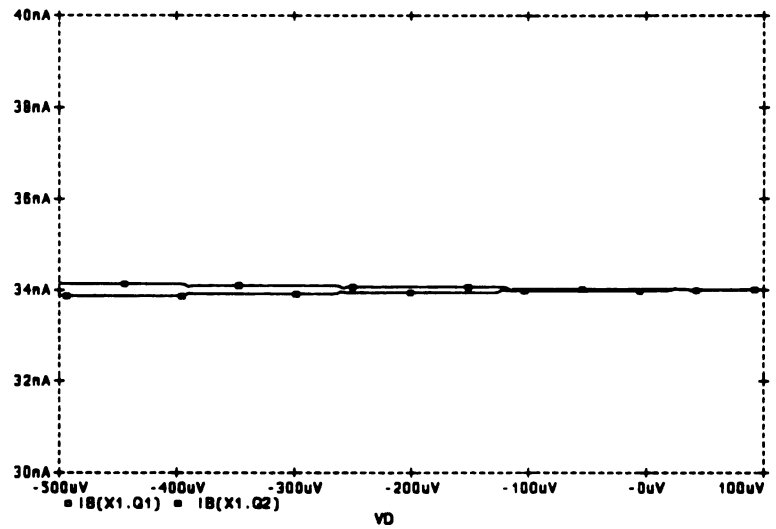

Figure 2.4b Input bias current (full device)

2.4.1.3 Open loop gain

The circuit used for the open loop gain test is shown in Fig. 2.5a. Fig. 2.5b shows the gain versus frequency and the phase versus frequency for both cases macromodel and full device. The dc gain A_{dmo} is equal to 105.9 dB, the 3dB frequency f_0 is found to be

5.012 Hz. Therefore, the gain bandwidth product GBP which is defined as the product of A_{dmo} and f_0 and is approximately equal to 988.57 KHz [7]. Also, the unity gain frequency, f_μ, is located at 891.3 KHz and the phase margin, ϕ_{pm}, is 63.1°. For the full device response A_{dmo} = 107.2 dB, the 3dB frequency f_0 is 3.286 Hz and the unity gain frequency f_μ = 825.4 KHz. Therefore, the GBP = 752.77 KHz. Also, the unity frequency f_μ = 825.4 KHz and the phase margin ϕ_{pm} = 64.4°.

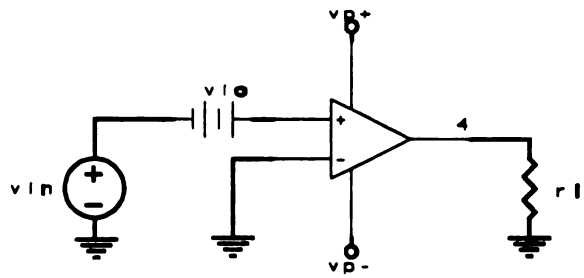

Figure 2.5a Open loop test circuit

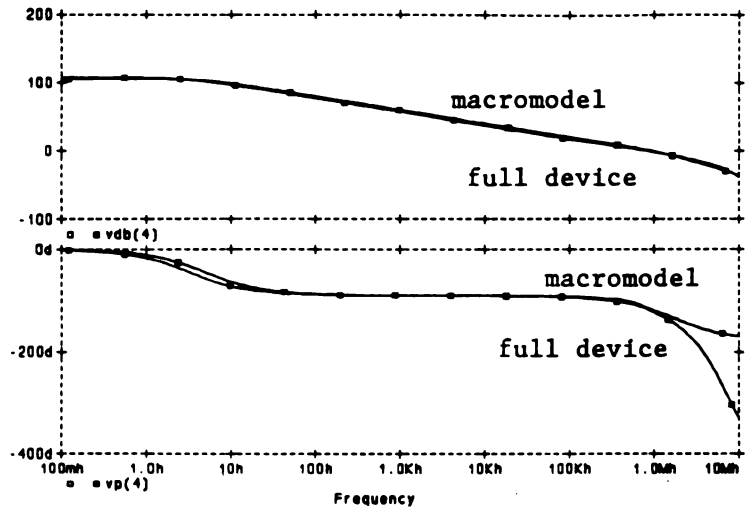

Figure 2.5b Open loop gain and phase margin

2.4.1.4 Output impedance

The output impedance is measured by using the circuit shown in Fig. 2.6a where the input is grounded and a test current I_T is applied at the output. The variation of the output impedance versus frequency is shown in Fig. 2.6b for both macromodel and full device of the μA741.

At low frequencies, the output impedance for the macromodel is measured to be 151.7 Ω and is called the dc output resistance $r_{o\text{-}dc}$. At high frequencies it becomes constant and is called ac output resistance, $r_{o\text{-}ac}$ and is equal to 50.4 Ω. For the full device case, $r_{o\text{-}dc}$ = 98.32 Ω and $r_{o\text{-}ac}$ = 87.17 Ω.

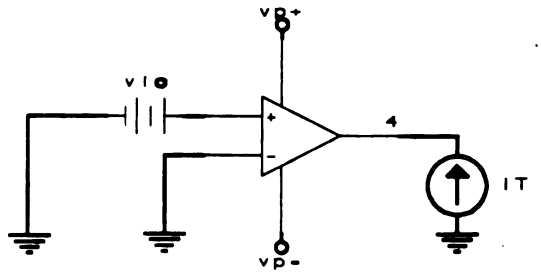

Figure 2.6a Output impedance test circuit

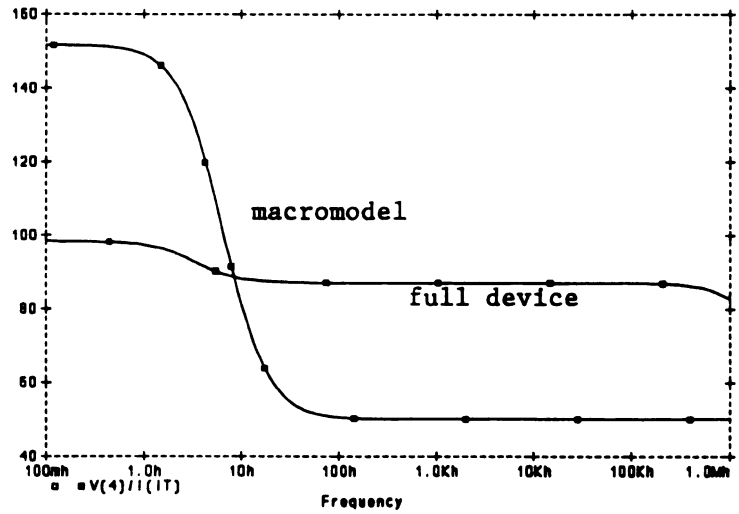

Figure 2.6b Output impedance versus frequencies

2.4.1.5 Common mode gain

The common mode gain test circuit is shown in Fig. 2.7a. The corresponding simulation curves for both macromodel and full device are shown in Fig. 2.7b (gain versus frequency and phase versus frequency). Obviously, the dc common mode gain is not modelled at frequecies higher than 10 Khz. The common mode gain is measured to be 15.89 dB = 6.23 for the macromodel and is 2.059 dB = 1.267 for the full device.

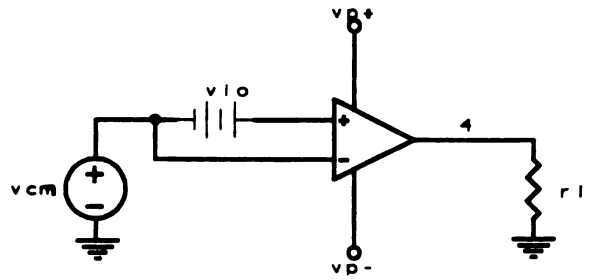

Figure 2.7a Common mode test circuit

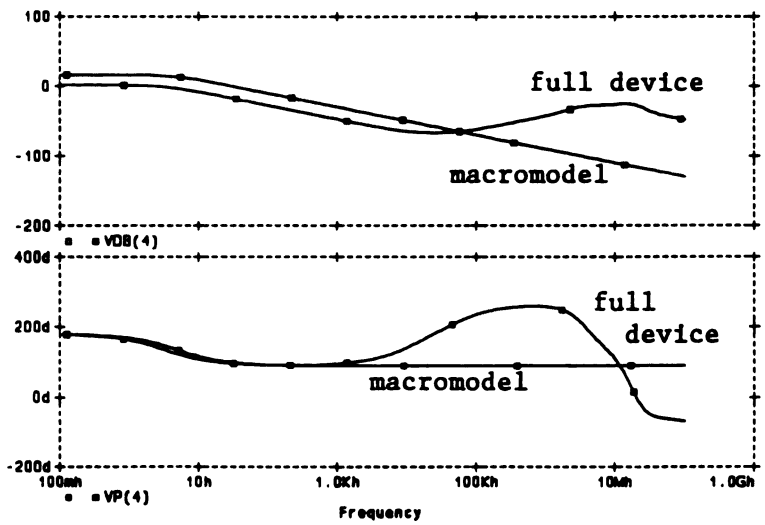

Figure 2.7b Common mode gain of the μA741

2.4.1.6 Short circuit current

The short circuit current test is shown in Fig. 2.8a. A very small resistance (1 Ω) is connected to the output so the output is almost shorted. Fig. 2.8b shows the SPICE response of the macromodel where the positive short circuit current is measured to be I_{sc+} = 40.61 mA and the negative short circuit current is I_{sc-} = -40.61 mA.

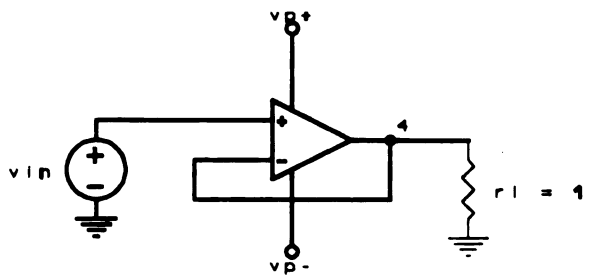

Figure 2.8a Short current test circuit

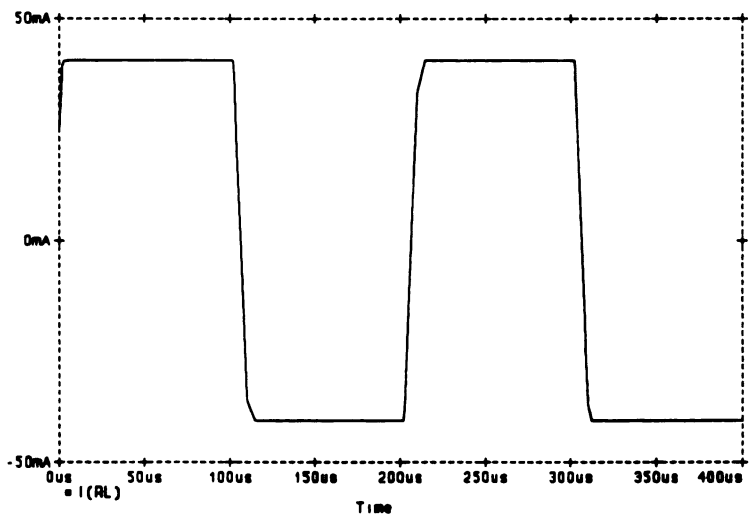

Figure 2.8b Short current of the μA741 macromodel

2.4.1.7 Slew rate

The slew rate is an important large signal characteristic of the operational amplifier and it is usually measured for the unity gain buffer amplifier as shown in Fig. 2.9a. The corresponding response is shown in Fig. 2.9b for both devices. As we can see the full device has a jump at the rising edge, which is not modeled correctly by the macromodel.

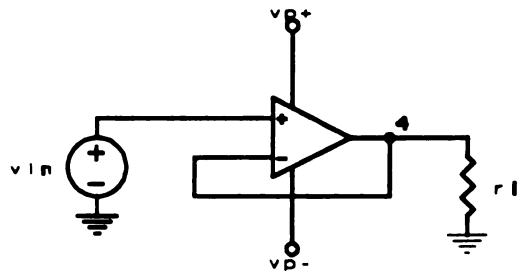

Figure 2.9a Slew rate test circuit

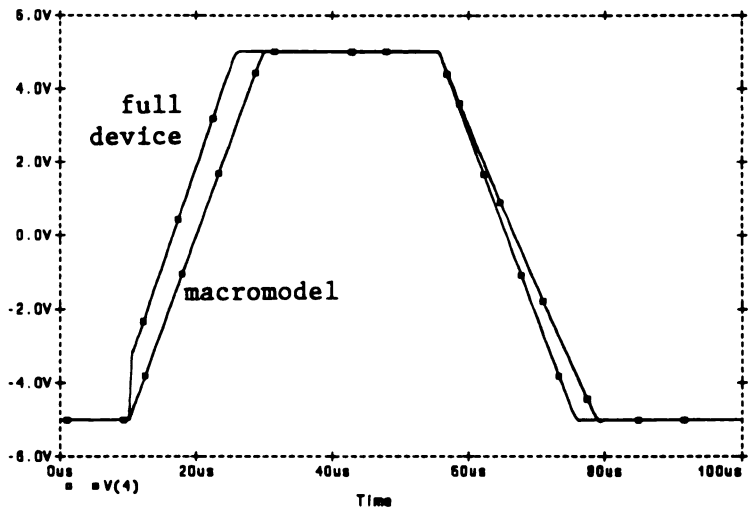

Figure 2.9b Slew rate of the μA741

2.4.2 Model formulas

2.4.2.1 Slew rate

Consider the unity gain buffer amplifier configuration as shown in Fig. 2.9a, the op amp input stage passes through several states. Fig. 2.10 shows the collector currents of the two transistors Q_1, Q_2. From these SPICE simulations, we see that at the rising

edge of the input, Q_1 is cutoff and Q_2 is active, while at the falling edge of the input Q_1 is active and Q_2 is cutoff. Also, Fig. 2.11 shows that the voltage at the node 6, v_6 is almost equal to zero and the voltage at node 7, v_7 is almost equal to the output voltage, V_{out}.

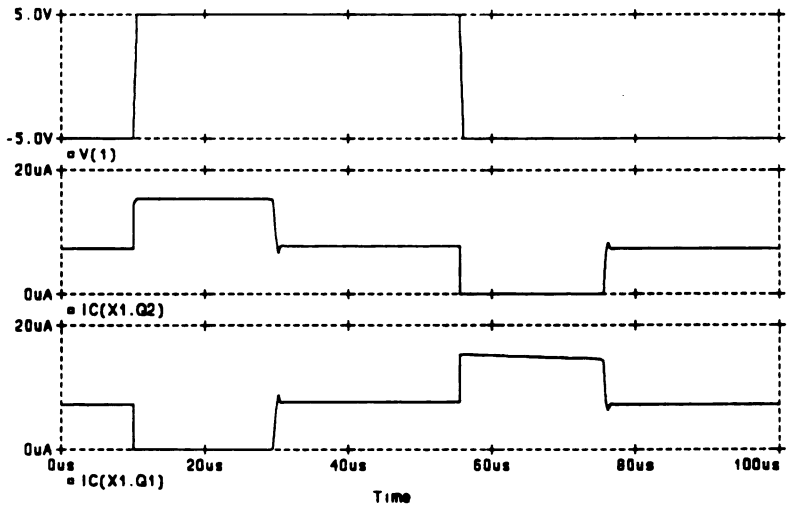

Figure 2.10 Collector currents of Q_1 and Q_2

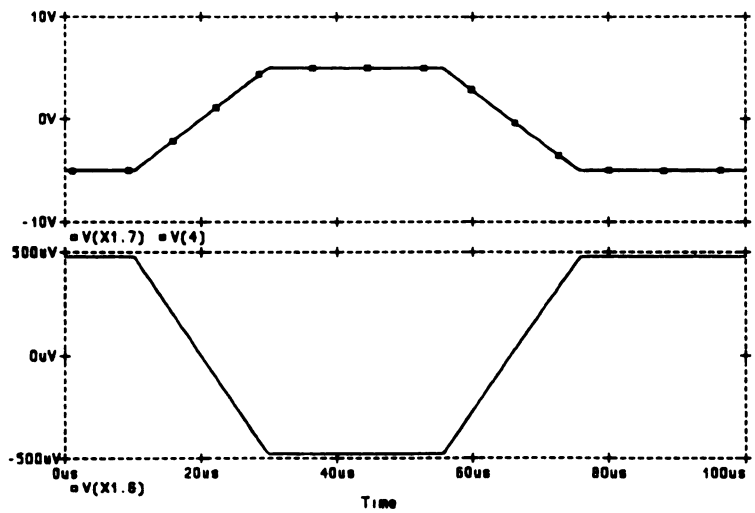

Figure 2.11 Voltages at node 6 and 7

a) Positive slew rate, SR^+

At the rising edge of the input when Q_1 is cutoff anf Q_2 is active, the current through the resistance r_{c2}, I_{rc2} is almost equal to I_{ee} and $I_{rc1} \approx 0$.

Also $v_a = v_{11} - v_{12} = r_{c2} \times I_{ee}$. To simplify the design, the VCCS g_a is chosen to be equal to

$$g_a = \frac{1}{r_{c2}} = \frac{1}{r_{c1}}$$

then, the current flowing in the VCCS g_a is equal to I_{ee}, that is

$$g_a v_a = I_{ee}$$

Since v_6 is a very small voltage and r_2 is a large resistance, then most of the current I_{ee} flows through c_2. The voltage across c_2, v_{c2} is equal to

$$v_{c2} = v_6 - v_7 \approx -v_7 \approx -v_{out}$$

then

$$v_{c2} = -\frac{I_{ee}}{c_2} t = -v_{out}$$

and

$$SR^+ = \frac{\Delta v_{out}}{\Delta t} = \frac{I_{ee}}{c_2} \qquad (2.1)$$

b) Negative slew rate, SR^-

At the falling edge of the input when Q_1 is active and Q_2 is cutoff, Q_1 is operating as a source follower tracking the variation of the output voltage. r_{e1} is a small resistance, therefore the output is across r_{ee} which is a very large resistance. Then the current flowing through r_{e1} is almost equal to I_{ee} and

$$I_{re1} \approx I_{ee} \approx I_{rc1}$$

hence

$$v_a = v_{11} - v_{12} = I_{ee} r_{c1}$$

Since v_6 is a very small voltage, then most of I_{ee} flows out of c_2, thus

$$v_{c2} = \frac{I_{ee}}{c_2} t = -v_{out}$$

and

$$SR = -\frac{I_{ee}}{c_2} \qquad (2.2)$$

2.4.2.2 Transistor parameters

The two transistors used at the input stage, Q_1 and Q_2 are identical, therefore I_{io} is zero and I_B is equal to the base current

$$I_B = I_{B1} = I_{B2}$$

The saturation current IS_1, IS_2 of the transistors Q_1, Q_2 are also the same. The value of β_1 and β_2 for the two ideal transistors is obtained from the values of the base currents I_{B1} and I_{B2} and the collector current I_{C1} and I_{C2} where

$$I_{C1} = I_{C2} = \frac{I_{ee}}{2}$$

Hence

$$\beta_1=\beta_2=\frac{I_{ee}}{2I_B} \tag{2.3}$$

2.4.2.3 Input stage: r_{ei}, r_{ci}

The circuit of the input stage differential mode is shown in Fig. 2.12. The dc voltage sources are grounded while the dc current source are open circuit. Using Bartlett's Bisection theorem [8], the common nodes are left grounded. Then, the circuit of Fig. 2.12 becomes that shown in Fig. 2.13.

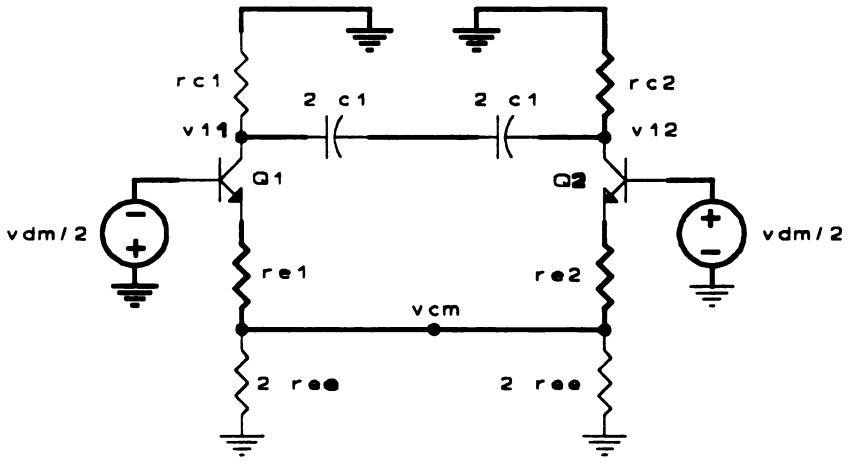

Figure 2.12 Input stage differential mode

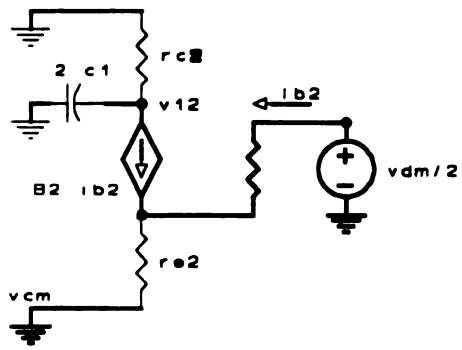

Figure 2.13 More simplified input stage DM

At low frequencies, c_1 is an open circuit then, the voltage v_{12} is equal to

$$v_{12}=-\beta_2 r_{c2} I_{B2}=-\beta_2 r_{c2}\frac{v_{dm}}{2(r_{\pi 2}+r_{e2}(\beta_2+1))}$$

where $r_{\pi 2}$ is the small signal input resistance between base and emitter, looking into the base [7]. Since $v_{12} = -v_{11}$ then $v_a = -2\ v_{12}$. The input stage gain A_{v1} is chosen to be one as was explained previously, then

$$A_{v1}=\frac{\beta_i r_{ci}}{(r_{\pi i}+r_{ei}(\beta_i+1))}=1 \qquad (2.4)$$

Through all the analysis, the subscript i could be 1 or 2 because the input stage is perfectly symmetric. Using the above equation r_{ei} is equal to

$$r_{ei}=r_{ci}-\frac{1}{g_{mi}} \qquad (2.5)$$

where

$$\frac{\beta_i+1}{\beta_i}\approx 1$$

and g_{mi} is the transconductance defined as follows

$$g_{mi}=\frac{v_T}{I_{Ci}}=\frac{r_{\pi i}}{\beta_i} \tag{2.6}$$

$I_{Ci}= I_{ee}/2$ is the collector current, v_T = K T/q = .02583 V at T = 300K [7].

The current controlled current source F_b is a polynominal set of currents flowing through th dc voltages v_b, v_c, v_e, v_{ip} and v_{in} with a_1, a_2, a_3, a_4 and a_5 are respectively the real coefficients.

$$F_b=a_1I_{vb}+a_2I_{vc}+a_3I_{ve}+a_4I_{vip}+a_5I_{vin} \tag{2.7}$$

When the op amp macromodel is operating in the linear region, the current flowing through F_b becomes equal to

$$F_b=a_1I_{vb} \tag{2.8}$$

Equation 2.8 is also verified by using SPICE. The test circuit used is the same as in Fig. 2.9a where the input does not exceed the saturation voltage (v_{in} = 1 V). Fig. 2.14 shows that the current in F_b is almost equal to equation 2.8.

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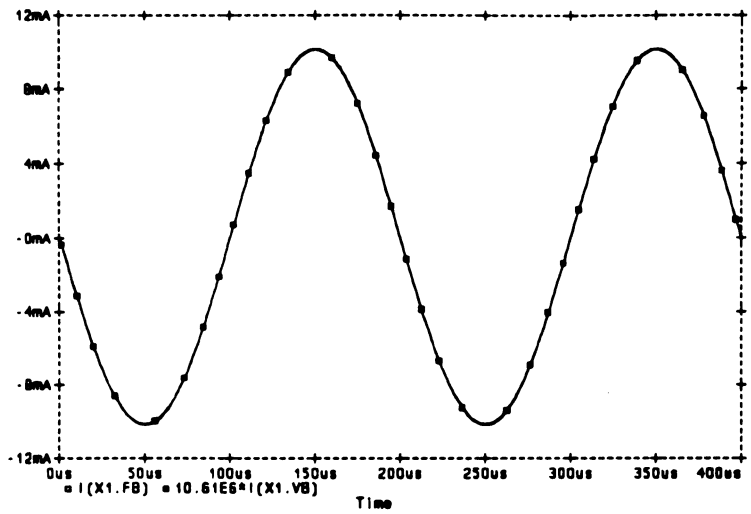

Figure 2.14 Currents in F_b and v_b

At dc, c_2 is an open circuit, then v_6 becomes equal to

$$v_6=-g_a v_a r_2=-I_{vb} r_2$$

and

$$v_7=-F_b r_{o2}=v_{out} \tag{2.9}$$

using equation 2.8, v_7 becomes

$$v_7=a_1 I_{vb} r_{o2}=a_1 g_a v_a r_{o2} \tag{2.10}$$

Since the input stage gain $A_{v1} = 1$ then $v_a = v_{dm}$, and from equation 2.9 and 2.10

$$v_{out}=a_1 g_a r_{o2} v_{dm}$$

Hence, the dc gain A_{dmo} is

$$A_{dmo}=a_1 g_a r_{o2} \tag{2.11}$$

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higher frequencies c_2 becomes short and a pole occurs. The pole is found by using the one capacitor method [8]. To solve for the resistance seen by c_2, a test current source is applied in parallel with the capacitance c_2 creating a voltage drop called v_x (see Fig. 2.15). Also, v_{dm} is set to zero, then $v_a = 0$,

$$v_x = I_x r_2 + r_{o2}(F_b + I_x)$$

From equation 2.8

$$v_x = I_x r_2 + r_{o2}(a_1 I_x + I_x)$$

a_1 is usually much larger than 1, then

$$v_x \approx I_x(r_2 + a_1 r_{o2})$$

and the above equation could be also approximated

$$v_x \approx I_x a_1 r_{o2}$$

because $a_1 \times r_{o2}$ is much larger than r_2, hence the resistance seen by c_2 is $a_1 \times r_{o2}$, then

$$f_0 = \frac{1}{(2\pi c_2 a_1 r_{o2})} \tag{2.14}$$

where f_0 is the frequency at which the dominant pole occurs and it is also the 3dB cutoff frequency. Thus, the gain bandwidth product is

$$GBP = \frac{g_a}{2\pi c_2} \tag{2.15}$$

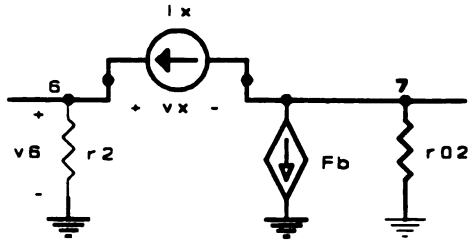

Figure 2.15 The resistance seen by c_2

2.4.2.4 Input offset voltage: v_{io}

Even though the input offset is meant to be zero in this type of op amp macromodel the value is measured to be -19.17 μV. This offset is due to the voltage across r_{ee} which is fedback to the VCCS g_{cm} at the intermediate stage. In order to find an expression of the input offset, the positive and negative inputs of the macromodel are grounded, then an expression of v_{out} is established where

$$v_{io} = -\frac{v_{out}}{A_{dmo}} \tag{2.16}$$

Since the input stage is perfectly symmetric, then the voltage at the node 10, v_{10}, is equal to

$$v_{10} = -\frac{I_{ee}}{2} r_{ei} - v_{bei}$$

v_{bei} is the base emitter voltage of the forward bias transistors Q_1 or Q_2 and is defined as follows

$$v_{bei}=v_T\ln(\frac{I_{ee}}{2IS})$$

IS is the saturation current of the transistor Q_1 and Q_2. Since v_{in} = 0 V then v_a = 0 V and the output voltage is found to be

$$v_{out}=-g_{cm}v_{cm}r_{o2}a_1+v_{99}$$

v_{99} is the voltage at the node 99 and if the power supply are equal in magnitude then v_{99} = 0 V because E_{GND} is averaging the power supplies. v_{cm} is the voltage drop across r_{ee}, thus it is the difference between v_{10} and v_{99}, using equation 2.16, the expression of v_{io} is as follows,

$$v_{io}=-\frac{g_{cm}}{g_a}[\frac{I_{ee}}{2}r_{ei}+v_T\ln(\frac{I_{ee}}{2IS})+v_{99}]-\frac{v_{99}}{r_{o2}a_1g_a}$$

2.4.2.5 Input stage: I_{ee} and r_{ee}

The value of the dc current source at the input stage for equal collector current is

$$I_{ee}=2(\frac{\beta+1}{\beta})I_C\approx 2I_C$$

The resistance r_{ee} is added to provide a finite CM input resistance. Because the current source I_{ee} is often realized with an npn transistor, the resistance r_{ee} is taken as its output resistance,

$$r_{ee}=\frac{V_A}{I_{ee}}$$

where V_A is the early voltage of the device [1]. V_A for a small npn is typically 200 V.

2.4.2.6 Input stage: c_1

From Fig. 2.5b and Fig. 2.12, a second pole occurs at f_2. Using the one capacitor method

$$f_2=\frac{1}{4\pi r_{c2}c_1} \tag{2.17}$$

c_1 is added at the input stage to introduce the excess phase effects in the DM amplifier response [1]. The excess at f_2 due to the non-dominant second pole is $\Delta\phi$ defined as follows

$$\Delta\phi=90°-\phi_{pm}$$

where ϕ_{pm} is the phase margin of the DM open-loop response.

$$\tan|\Delta\phi|=\frac{f_\mu}{f_2}$$

Substituting equation 2.17 into the above equation [8]

$$\tan|\Delta\phi|=4\pi r_{c2}c_1 f_\mu$$

Then, the necessary value of c_1 to produce the second pole is

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$$c_1 = \frac{\tan|90° - \phi_{pm}|}{4\pi f_\mu r_{c2}} \tag{2.18}$$

2.4.2.7 Interstage: g_{cm}

For CM response and after using the Bartlett's theorem, becomes that shown in Fig. 2.16 where the common nodes are left open, the dc voltage sources are grounded and dc current source becomes open circuit.

At low frequencies c_2 is an open circuit and

$$v_{10} = 2r_{ee}(\beta_i + 1)i_{bi} \tag{2.19}$$

where

$$i_{bi} = \frac{v_{cm}}{r_{\pi i} + (\beta_i + 1)(r_{ei} + 2r_{ee})}$$

Since r_{ee} is a very large resistance, then i_{bi} could be approximated to

$$i_{bi} \approx \frac{v_{cm}}{(\beta_i + 1)2r_{ei}} \tag{2.20}$$

Substituting equation 2.20 into 2.19

$$v_{10} \approx v_{cm}$$

The current flowing through r_2 is equal to

$$I_{vb} = -g_{cm}v_{cm}$$

Substituting the above equation into equation 2.9

$$v_{out}=a_1 g_{cm} r_{o2} v_{cm}$$

Hence, the common mode gain, A_{cm} is

$$A_{cm}=a_1 g_{cm} r_{o2} \tag{2.21}$$

The common mode rejection ratio (CMMR) is defined as the ratio of the DM gain to the CM gain [7], that is

$$CMMR=\frac{1}{r_{ci} g_{cm}} \tag{2.22}$$

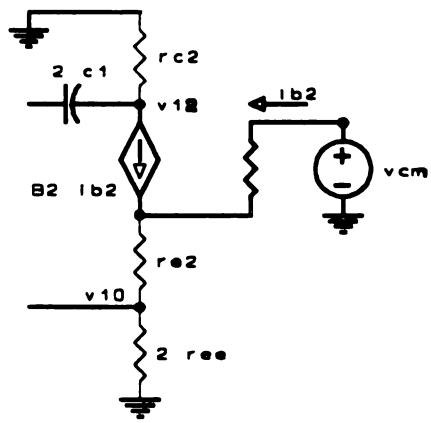

Figure 2.16 A simplified common mode input stage

2.4.2.8 DC power drain

To model the actual dc power dissipation of an op amp, a resistance r_p is added into the macromodel [1]. The power dissipation is

$$p_d=(v_{p+}-v_{p-})I_{ee}+\frac{(v_{p+}-v_{p-})^2}{r_p}$$

The necessary value of r_p to produce this dissipation is

$$r_p = \frac{(v_{p+} - v_{p-})^2}{p_d - (v_{p+} - v_{p-})I_{ee}} \tag{2.23}$$

The diode d_p is used across r_p for modeling the case of possible conduction. This can occur with incorrect power supply polarities. Also the diode d_p has an ohmic resitance noted as r_s and chosen to be 1 Ω to avoid the convergence problem.

2.4.2.9 Output stage: r_{o1} and r_{o2}

The output stage provides the dc and ac output resistances. From Fig. 2.6b, the output resistance at low frequencies (dc output impedance) is

$$r_{o-dc} = r_{o1} + r_{o2} \tag{2.24}$$

At high frequencies, c_2 is short and the ac output impedance is

$$r_{o-ac} = r_{o1} + (r_2 \| \frac{1}{a_1} \| r_{o2}) \tag{2.25}$$

Since a_1 is very large, then

$$r_{o-ac} \approx r_{o1}$$

2.4.2.10 Output stage: current limiting

a) Sourcing current: I_{sc+}

The positive short circuit current, I_{sc+} is a sourcing current that occurs for positive output voltages. When the input and output do not exceed the saturation voltage of the op amp, the expression of the CCCS F_b becomes as follows

$$F_b = a_1 I_{vb} + a_4 I_{vlp} \tag{2.26}$$

The current I_{vlp} is used to absorbs the current flowing in F_b. The current flowing in r_{o1} is I_{sc+} and from the SPICE simulation (see Fig 2.17) the current flowing through c_2 is almost zero, that is

$$g_a v_a = -I_{vb} = I_{ee} \tag{2.27}$$

and

$$F_b = -(1 + \frac{r_{o1}}{r_{o2}}) I_{sc}. \tag{2.28}$$

Since I_{ee} and I_{sc+} are positive currents, then the two above equations show that, I_{vb} and F_b are negative currents. From equation 2.11, the coefficient a_1 is found to be a very large positive number. Thus the product of a_1 and I_{vb} is a large negative current. Also I_{vlp} is defined to be a positive current. In order to make F_b a small internal current, the product of a_4 and I_{vlp} has to be positive. Thus a_4 has to be positive coefficient and close to but smaller than a_1 so that F_b is still negative current and satisfies equation 2.28.

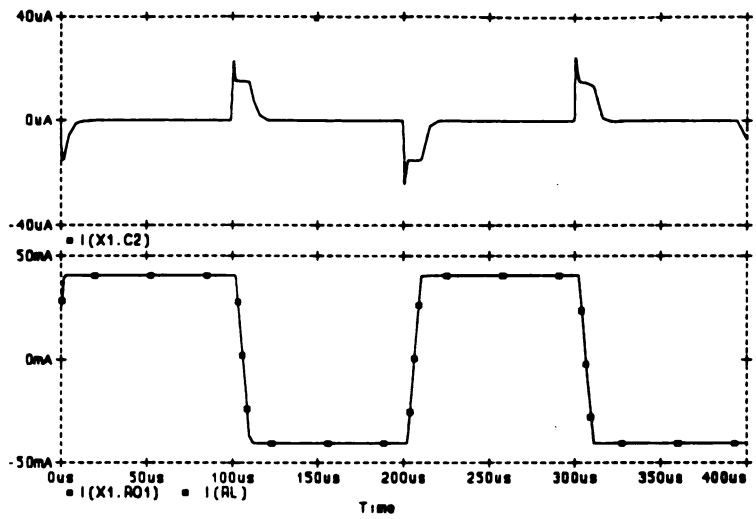

Figure 2.17 Currents through c_2 and r_{o2}

The CCVS h_{lim} is defined as

$$h_{lim}=\alpha I_{vlim}=\alpha I_{sc}.$$

α is a constant coefficient and usually selected to be equal to 1 K. On the other hand, h_{lim} is the summation of the voltage drop v_{dlp} across the diode d_{lp} and the dc voltage source v_{lp}. Therefore

$$v_{lp}=\alpha I_{sc}.-v_{dlp} \tag{2.29}$$

The voltage v_{lp} could be solved once v_{dlp} is determined and I_{sc+} is specified. The voltage v_{dlp} is related to the current flowing through the diode d_{lp} which is equal to I_{vlp}, that is

$$v_{dlp}=v_T\ln(\frac{I_{vlp}}{IS_{dlp}})$$

where IS_{dlp} is the diode saturation current of the diode, d_{lp} specified in SPICE program as IS and is arbitrarily chosen to be 8E-16 A. The value of I_{vlp} is determined by equating equation 2.26 and 2.28, that is

$$I_{vlp}=-\frac{1}{a_4}(1+\frac{r_{o1}}{r_{o2}})I_{sc+}+\frac{a_1}{a_4}I_{ee}$$

Since a_4 is usually a large coefficient, then the above equation is approximated as follows,

$$I_{vlp}\cong\frac{a_1}{a_4}I_{ee}$$

Hence

$$v_{dlp}=v_T\ln(\frac{a_1 I_{ee}}{a_4 IS_{dlp}}) \tag{2.30}$$

Finally, by substituting equation 2.30 into 2.29, the expression of v_{lp} is established

$$v_{lp}=\alpha I_{sc}.-v_T\ln(\frac{a_1 I_{ee}}{a_4 IS_{dlp}}) \tag{2.31}$$

All this analysis is checked by using SPICE (see Fig. 2.18).

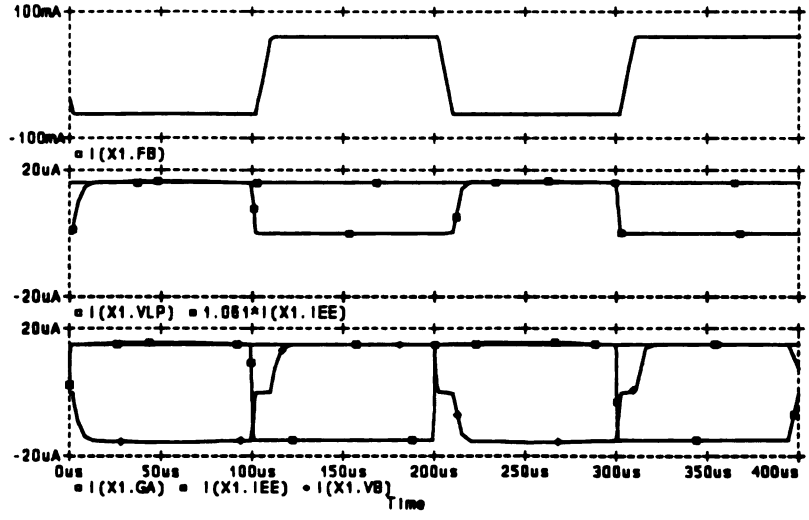

Figure 2.18 Currents through F_b, g_a, v_{lp} and v_b

b) Sinking current: I_{sc-}

The negative short circuit I_{sc-} is a sinking current that occurs at negative output

voltages. When the input and output do not exceed the saturation voltage of the op-amp, the expression of the CCCS F_b becomes as follows

$$F_b = a_1 I_{vb} + a_5 I_{v_{in}} \tag{2.32}$$

Now, the current flowing through r_{o1} is I_{sc-} and from the SPICE simulation (see Fig. 2.17), the current flowing through c_2 is almost zero, that is

$$g_a v_a = -I_{vb} = -I_{ee} \tag{2.33}$$

and

$$F_b = -(1 + \frac{r_{o1}}{r_{o2}}) I_{sc-} \tag{2.34}$$

Since I_{sc-} is a negative current then, the two above equation show that, I_{vb} and F_b are positive currents. The product of a_1 and I_{vb} is a large positive current. Also the current I_{vin} is defined to be a negative current. In order to make F_b a small positive internal current, the product of a_5 and I_{vin} has to be negative. Thus a_5 is a negative coefficient and close to but smaller than a_1. If the negative short circuit current is equal in magnitude to the positive short circuit current, the a_4 is equal to the absolute value of a_5.

The CCVS h_{lim} is now defined as

$$h_{lim} = \alpha I_{sc-}$$

Also

$$h_{lim} = -v_{in} - v_{din}$$

then

$$v_{in} = -\alpha I_{sc-} - v_{din} \tag{2.35}$$

The voltage v_{in} could be solved once v_{din} is determined and I_{sc-} is specified. Following the same methodology done previously for the case of I_{sc+}, the expression of v_{in} is found to be

$$v_{in} = -\alpha I_{sc-} - v_T \ln\left(-\frac{a_1 I_{ee}}{a_5 IS_{din}}\right) \tag{2.37}$$

where IS_{din} is the saturation current of the diode d_{in}. It should be noted that I_{sc-} is a negative quantity.

2.4.2.11 Output stage: voltage limiting

a) Positive voltage limiting

The positive output voltage is limited by the voltage by the voltage source diode clamp combinations v_c, d_c. When the output clamps positively such as to forward bias d_c, a current flows in the diode d_c, I_{dc} to absorbs the current flowing in CCCs F_b, thus

$$F_b = a_1 I_{vb} - a_2 I_{dc} \tag{2.38}$$

where $I_{dc} = - I_{vc}$ because in SPICE the current is defined to flow from the positive node to the negative node. Also from the SPICE simulation (see Fig. 2.19), the current flowing in the VCCS g_a is

$$g_a v_a = I_{ee}$$

and the current I_{vb} is approximately equal to $-I_{ee}$, then equation 2.38 becomes now

$$F_b=-a_1I_{ee}-a_2I_{dc}$$

Since I_{dc} is a positive quantity, then a_2 must be a negative coefficient to make F_b a small internal current and is close to but smaller than a_1 in magnitude so that F_b is still negative small current as seen in Fig. 2.19. Therefore I_{dc} is approximately equal to

$$I_{dc}\approx-\frac{a_1}{a_2}I_{ee}$$

Since positive output voltage is limited by the voltage source diode clamp combinations v_c, d_c, the clipping voltage is equal to

$$v_{sat+}=v_{p+}-v_c+v_{dc} \tag{2.39}$$

where v_{dc} is the voltage drop across diode d_c. Since v_{sat+} is specified (for the μA741 is measured to be ±14.61 V), then the value of v_c could be determined once v_{dc} is determined. This voltage is related to the current I_{dc} as follows

$$v_{dc}=v_T\ln(-\frac{a_1I_{ee}}{a_2IS_{dc}})$$

IS_{dc} is the diode saturation current of the diode d_c and is set arbitrarily equal to 8E-16 A. Finally using equation 2.39 and the above equation, the value of v_c is defined as below

$$v_c=v_{p+}-v_{sat+}+v_T\ln(-\frac{a_1I_{ee}}{a_2IS_{dc}}) \tag{2.40}$$

b) Negative voltage limiting

The negative output voltage is limited by the voltage source diode clamp combination v_e, d_e. When the output clamps negatively such as to forward bias d_e, v_{sat-} is defined as follows

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$$v_{sat-}=v_{p-}+v_e-v_{de}$$

Following the same methodology done in the case of the positive output clamp, v_e is found to be

$$v_e=-v_{p-}+v_{sat-}+v_T\ln\left(\frac{a_1 I_{ee}}{a_3 IS_{de}}\right) \tag{2.41}$$

where $IS_{de} = IS_{dc}$ and a_3 is a positive coefficient close to but smaller than a_1.

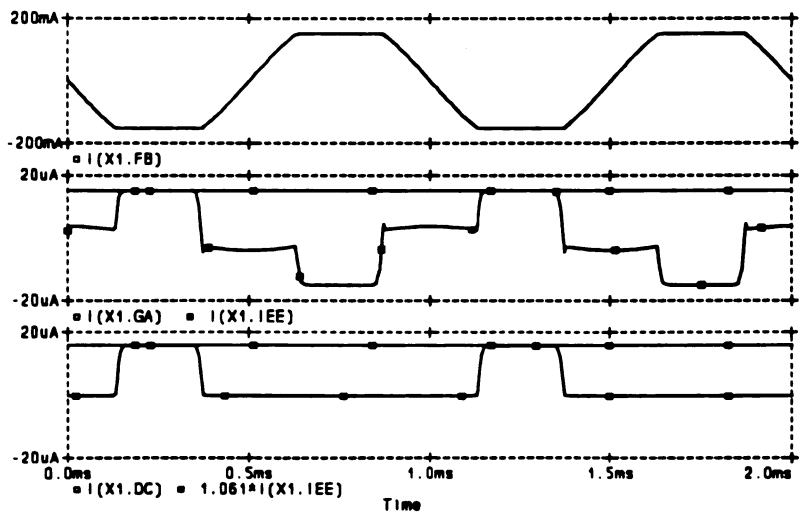


Figure 2.19 The current through F_b, g_a and d_c

2.4.3 Design procedure

A summary of the design equations for the macromodel parameters is developed in this section. The following design procedure could be used for any op amp microsim model with npn bipolar transistor at the input stage. The starting point of the design is to have values of the typical response characteristics of the corresponding op amp, that

is, the following specifications are assumed available : SR^+, SR^-, I_B, A_{dmo}, f_μ, GBP, ϕ_{pm}, CMRR, $r_{o\text{-}ac}$, $r_{o\text{-}dc}$, I_{sc+}, I_{sc-}, v_{sat+}, v_{sat-}, and p_d.

Step 1: Choose $c_2 = c_c$ where c_c is used in the chip as a compensation capacitance.

Step 2: $$I_{ee}=c_2 SR^+$$

Step 3: $$\beta=\frac{I_{ee}}{2I_B}$$

Step 4: Choose the saturation current IS for the two transistors Q_1 and Q_2 to be equal to 8E-16 A.

Step 5: $$r_{c1}=r_{c2}=\frac{1}{2\pi GBPc_2}$$

Step 6: $$g_{mi}=\frac{I_{ee}}{2v_T}$$

Step 7: $$r_{e1}=r_{e2}=r_{ci}-\frac{1}{g_{mi}}$$

Step 8: Choose V_A = 200 V, then $$r_e=\frac{V_A}{I_{ee}}$$

Step 9: $$c_1=\frac{\tan|90°-\phi_{pm}|}{4\pi f_\mu r_{c1}}$$

Step 10: $$g_a = \frac{1}{r_{c2}}$$

Step 11: $$g_{cm} = \frac{1}{CMMR r_{c1}}$$

Step 12: Choose r_2 = 100 kΩ.

Step 13: $$r_{o2} = r_{o-dc} - r_{o-ac}$$

$$r_{o1} = r_{o-ac}$$

Step 14: $$a_1 = \frac{A_{dmo} r_{c1}}{r_{o2}}$$

Step 15: Pick $-a_2 = a_3 = a_4 = -a_5 = a_1$, and then round them off.

Step 16: Choose the diode saturation current for all the diodes used in the model to be equal to 8E-16 A and the diode ohmic resistance r_s to be 1 Ω.

Step 17: Choose α = 1 K.

Step 18: $$v_{lp} = \alpha I_{sc+} - v_T \ln \frac{a_1 I_{ee}}{a_4 IS_{dlp}}$$

Step 19: $$v_{ln} = -\alpha I_{sc-} - v_T \ln - \frac{a_1 I_{ee}}{a_5 IS_{dln}}$$

Step 20: $$v_c = v_{p+} - v_{sat+} + v_T \ln - \frac{a_1 I_{ee}}{a_2 IS_{dc}}$$

Step 21: $$v_e = v_{p-} + v_{sat-} + v_T \ln \frac{a_1 I_{ee}}{a_3 I S_{de}}$$

Step 22: $$r_p = \frac{(v_{p+} - v_{p-})^2}{p_d - (v_{p+} - v_{p-}) I_{ee}}$$

Step 23: $$E_{GND} = \frac{v_{p+} + v_{p-}}{2}$$

2.4.4 Numerical example

A numerical example is used to illustrate the development of the parameters of the op amp macromodel and to verify the design formulas and procedure. This verification is done by finding the specifications of the model using the model formulas derived in the previous section and the macromodel parameter's values given in Table 2.1. Table 2.3 includes the calculated and the SPICE simulated measurements using the μA741 microsim macromodel as an example. A list of the equations used to find the calculated measurements are listed below.

1) $$SR^+ = \frac{I_{ee}}{C_2}$$

2) $$SR^- = -\frac{I_{ee}}{C_2}$$

3) $$I_B=\frac{I_{B1}+I_{B2}}{2}=\frac{I_{ee}}{2\beta}$$

4) $$v_{io}=-\frac{g_{cm}}{g_a}\left[\frac{I_{ee}}{2}r_{ei}+v_T\ln\left(\frac{I_{ee}}{2IS}\right)+v_{99}\right]-\frac{v_{99}}{r_{o2}a_1g_a}$$

5) $$f_0=\frac{1}{2\pi c_2 a_1 r_{o2}}$$

6) $$A_{dmo}=a_1 g_a r_{o2}$$

7) $$GBP=\frac{g_a}{2\pi c_2}$$

8) $$f_\mu=\sqrt{\frac{-f_2^{\,2}+\sqrt{f_2^{\,4}+4A_{dmo}^{\,2}f_0^{\,2}f_2^{\,2}}}{2}}$$

where $$f_2\frac{1}{4\pi r_{c2}c_1}$$

9) $$\phi_{pm}=90^\circ-\arctan\frac{f_\mu}{f_2}$$

10) $$CMMR=\frac{1}{r_{ci}g_{cm}}$$

11) $$r_{o-ac}=r_{o1}$$

12) $$r_{o-dc}=r_{o1}+r_{o2}$$

13) $$I_{sc+}=\frac{1}{\alpha}(v_{lp}+v_T\ln\frac{a_1 I_{ee}}{a_4 IS_{dlp}})$$

14) $$I_{sc-}=-\frac{1}{\alpha}(v_{ln}+v_T\ln-\frac{a_1 I_{ee}}{a_5 IS_{dln}})$$

15) $$v_{sat+}=v_{p+}-v_c+v_T\ln-\frac{a_1 I_{ee}}{a_2 IS_{dc}}$$

16) $$v_{sat-}=v_{p-}+v_e-v_T\ln\frac{a_1 I_{ee}}{a_3 IS_{de}}$$

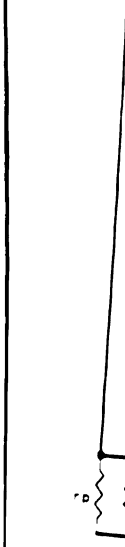
17) $$p_d=(v_{p+}-v_{p-})I_{ee}+\frac{(v_{p+}-v_{p-})^2}{r_p}$$

Table 2.3 Parameters of the μA741

Parameter	Calculated	Simulated
SR^+	0.5053 v/μs	0.5074 v/μs
SR^-	-0.5053 v/μs	-0.4957 v/μs
v_{io}	-19.24 μV	-19.17 μV
I_B	80.853 nA	79.742 nA
f_0	5.000 Hz	5.012 Hz
A_{dmo}	106.02 dB	105.9 dB
GBP	1 MHz	988.57 KHz
f_μ	889.53 KHz	891.3 KHz
ϕ_{pm}	62.81°	63.1°
CMRR	90 dB	90.01 dB
$r_{o\text{-}ac}$	50 Ω	50.4 Ω
$r_{o\text{-}dc}$	150 Ω	151.7 Ω
I_{sc+}	40.614 mA	40.61 mA
I_{sc-}	-40.614 mA	-40.61 mA
v_{sat+}	14.614 V	14.61 V
v_{sat-}	-14.614 V	14.61 V
p_d	50 mW	50 mW

2.5 PNP Bipolar Input Stage Macromodel

The pnp input stage microsim macromodel schematic is the same as the npn input stage macromodel with of course pnp transistors replacing the npn transistors. This causes the input stage to be flipped over as it is seen in Fig. 2.20. This type of macromodel has been adapted to many op amps such as: LT1013, LM324, LM124,



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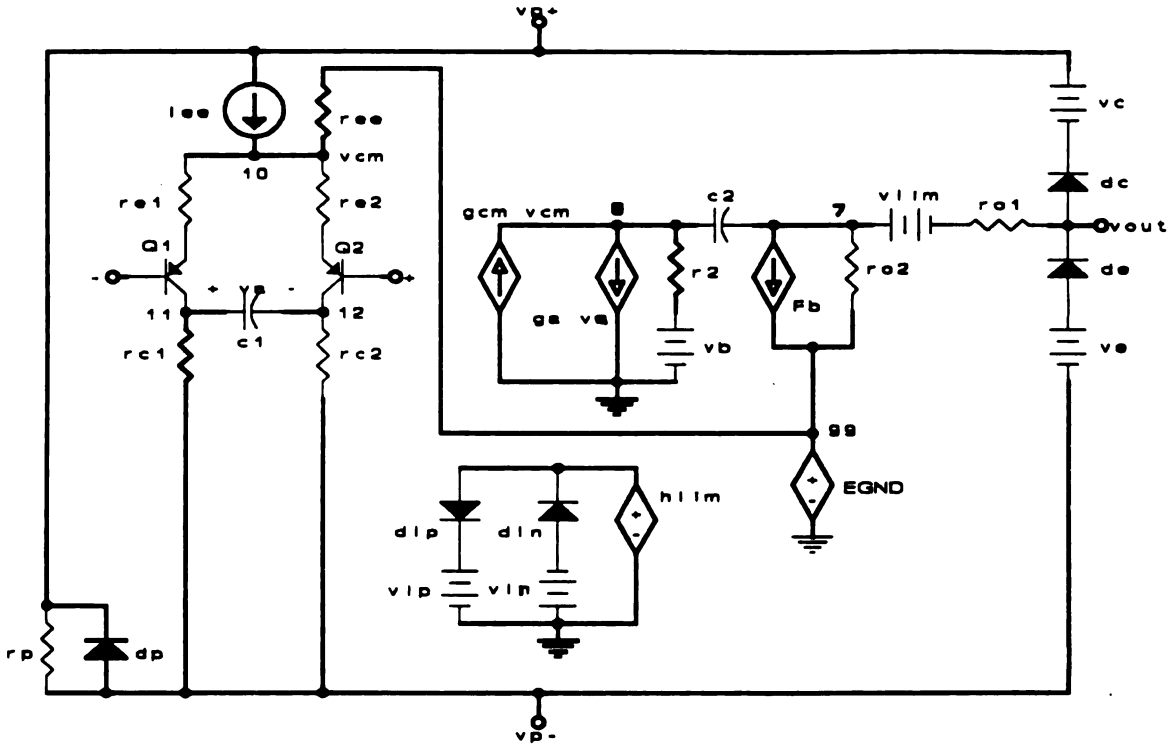

Figure 2.20 Microsim macromodel of the LM124

Table 2.4 SPICE file of the LM124 macromodel

```
.subckt LM124    1 2 3 4    5
*                + - vp+ vp- vout
* for the rest of the file see SPICE library version 4.02 July 1989
```

2.5.1 SPICE test circuits

The same SPICE test circuits established previously using the npn input stage macromodel, now will be defined using the pnp input stage macromodel. The LM124 op amp is used as the example. The summarized data of the SPICE test circuit

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Step 1: Ch

Step 2:

measurements are included in Table 2.5.

2.5.2 Model formulas

The only difference between the npn and pnp input stage macromodel is the input stage. Even though all the previous analysis was done for the npn input stage, including the design equations, the same formulas hold exactly for the pnp macromodel except for the bias current and input offset voltage. The bias current is defined as a negative current since it is flowing out of the base. The input stage is also symmetric, but due to the voltage across r_{ee} the input offset is not zero and is defined as follows

$$v_{io}=\frac{g_{cm}}{g_a}\left[\frac{I_{ee}}{2}r_{ei}+v_T\ln\left(\frac{I_{ee}}{2IS}\right)-v_{99}\right]-\frac{v_{99}}{r_{o2}a_1g_a}$$

2.5.3 Design procedure

A summary of the design equations for the macromodel parameters is developed in this section. The following design procedure could be used for any op amp microsim model with pnp bipolar transistor at the input stage. The starting point of the design is to have the following specifications of the corresponding op amp: SR^+, SR^-, I_B, A_{dmo}, GBP, f_μ, ϕ_{pm}, CMRR, $r_{o\text{-}ac}$, $r_{o\text{-}dc}$, I_{sc+}, I_{sc-}, v_{sat+}, v_{sat-}, and p_d.

Step 1: Choose $c_2 = c_c$ where c_c is used in the chip as a compensation capacitance.

Step 2: $I_{ee}=c_2SR^+$

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Step 7:

Step 8: C

Step 9:

Step 10:

Step 11:

Step 12: CH

Step 3: $$\beta=\frac{I_{ee}}{-2I_B}$$

Step 4: Choose the saturation current for the two transistors Q_1 and Q_2 to be equal to 8E-16 A.

Step 5: $$r_{c1}=r_{c2}=\frac{1}{2\pi GBPc_2}$$

Step 6: $$g_{mi}=\frac{I_{ee}}{2v_T}$$

Step 7: $$r_{e1}=r_{e2}=r_{ci}-\frac{1}{g_{mi}}$$

Step 8: Choose V_A = 200 V, then $$r_{ee}=\frac{V_A}{I_{ee}}$$

Step 9: $$c_1=\frac{\tan|90°-\phi_{pm}|}{4\pi f_\mu r_{c1}}$$

Step 10: $$g_a=\frac{1}{r_{c2}}$$

Step 11: $$g_{cm}=\frac{1}{CMMRr_{c1}}$$

Step 12: Choose r_2 = 100 kΩ.

St

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Step

Step

Step 19

Step 20

Step 21:

Step 22:

Step 13: $$r_{o2}=r_{o-dc}-r_{o-ac}$$

$$r_{o1}=r_{o-ac}$$

Step 14: $$a_1=\frac{A_{dmo}r_{c1}}{r_{o2}}$$

Step 15: Pick $-a_2 = a_3 = a_4 = -a_5 = a_1$, and then round them off.

Step 16: Choose the diode saturation current for all the diodes used in the model to be equal to 8E-16 A and the diode ohmic resistance r_s to be 1 Ω.

Step 17: Choose α = 1 K.

Step 18: $$v_{lp}=\alpha I_{sc+}-v_T\ln\frac{a_1 I_{ee}}{a_4 IS_{dlp}}$$

Step 19: $$v_{ln}=-\alpha I_{sc-}-v_T\ln-\frac{a_1 I_{ee}}{a_5 IS_{dln}}$$

Step 20: $$v_c=v_{p+}-v_{sat+}+v_T\ln-\frac{a_1 I_{ee}}{a_2 IS_{dc}}$$

Step 21: $$v_e=v_{p-}+v_{sat-}+v_T\ln\frac{a_1 I_{ee}}{a_3 IS_{de}}$$

Step 22: $$r_p=\frac{(v_{p+}-v_{p-})^2}{p_d-(v_{p+}-v_{p-})I_{ee}}$$

Step 23: $$E_{GND}=\frac{V_{p+}+V_{p-}}{2}$$

2.5.4 Numerical example

This verification is done by finding the specifications of the model using the model formulas derived in the previous section and the macromodel parameter's values given in Table 2.4. Table 2.5 includes the calculated and the SPICE simulated measurements using the LM124 microsim macromodel as an example. A list of the equations used to find the calculated measurements are listed below.

1) $$SR^{+}=\frac{I_{ee}}{C_2}$$

2) $$SR^{-}=-\frac{I_{ee}}{C_2}$$

3) $$I_B=-\frac{I_{B1}+I_{B2}}{2}=-\frac{I_{ee}}{2\beta}$$

4) $$v_{io}=\frac{g_{cm}}{g_a}\left[\frac{I_{ee}}{2}r_{ei}+v_T\ln\left(\frac{I_{ee}}{2IS}\right)-v_{99}\right]-\frac{v_{99}}{r_{o2}a_1g_a}$$

5) $$f_0=\frac{1}{2\pi C_2a_1r_{o2}}$$

6) $$A_{dmo}=a_1 g_a r_{o2}$$

7) $$GBP=\frac{g_a}{2\pi c_2}$$

8) $$f_\mu=\sqrt{\frac{-f_2^2+\sqrt{f_2^4+4A_{dmo}^2 f_0^2 f_2^2}}{2}}$$

where $$f_2\frac{1}{4\pi r_{c2}c_1}$$

9) $$\phi_{pm}=90^\circ-\arctan\frac{f_\mu}{f_2}$$

10) $$CMMR=\frac{1}{r_{ci}g_{cm}}$$

11) $$r_{o-ac}=r_{o1}$$

12) $$r_{o-dc}=r_{o1}+r_{o2}$$

13) $$I_{sc+}=\frac{1}{\alpha}(v_{ip}+v_T\ln\frac{a_1 I_{ee}}{a_4 IS_{dip}})$$

14) $$I_{sc-}=-\frac{1}{\alpha}(v_{in}+v_T\ln-\frac{a_1 I_{ee}}{a_5 IS_{din}})$$

15) $$v_{sat+}=v_{p+}-v_c+v_T\ln-\frac{a_1 I_{ee}}{a_2 IS_{dc}}$$

16) $$v_{sat-}=v_{p-}+v_e-v_T\ln\frac{a_1 I_{ee}}{a_3 IS_{de}}$$

17) $$p_d=(v_{p+}-v_{p-})I_{ee}+\frac{(v_{p+}-v_{p-})^2}{r_p}$$

Table 2.5 Parameters of the LM124

Parameter	Calculated	Simulated
SR^+	0.503 V/μs	0.4942 V/μs
SR^-	-0.503 V/μs	-0.506 V/μs
I_B	-45.26 nA	-44.83 nA
f_0	10.00 Hz	10.00 Hz
A_{dmo}	100 dB	99.91 dB
GBP	1 MHz	989.691 KHz
f_μ	982.577 KHz	962.4 KHz
ϕ_{pm}	79.29°	79.5°
CMRR	85.43 dB	84.97 dB
$r_{o\text{-}ac}$	50 Ω	50 Ω
$r_{o\text{-}dc}$	75 Ω	75.92 Ω
I_{sc+}	40.613 mA	40.61 mA
I_{sc-}	-40.613 mA	-40.61 mA
v_{sat+}	14.113 V	14.11 V
v_{sat-}	-15.613 V	-15.61 V
p_d	99.55 mW	99.5 mW

2.6 JFET Input Stage

An other op amp macromodel designed by microsim is the n-channel JFET input stage macromodel (see Fig. 2.21). Its schematic is very similar to the bipolar transistor input stage macromodel with of course JFETs j_1, j_2 replacing the transistors Q_1, Q_2. This macromodel has been adapted to several op amps such as: LF411, LF412, TLO82 and TLO84 ..... The only difference between these two macromodels is the input stage. The intermediate and output stages remain exactly the same as was described previously. The input stage now has a two n-channel JFETs j_1, j_2 instead of the two transistors Q_1, Q_2. A capacitance c_{ss} is added to produce the asymmetric slew rate. Since the input stage has a unity dc gain, then the basic design equations remain the same.

Table 2.6 SPICE file of the LF411 macromodel

```
.subckt LF411    1  2  3  4  5
*                +  -  vp+ vp- vout
* (for the rest of the SPICE file see SPICE library version 4.02 July 1989)
```

2.6.1 SPICE test circuits

The same SPICE test cicuits established using bipolar input stage macromodel, now will be established using the n-channel JFET input stage macromodel such as the LF411. Table 2.7 provides the summarized data of the SPICE test circuits for the LF411.

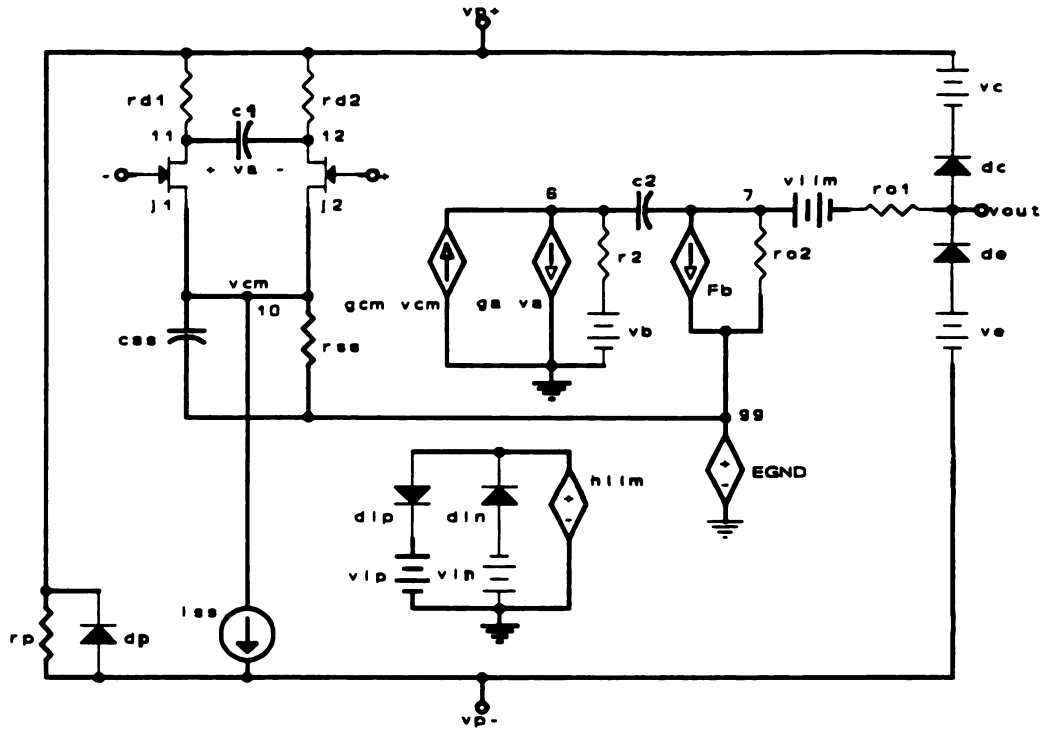

Figure 2.21 Microsim model of the LF411

2.6.2 Model formulas

The basic operations and design formulas of a n-channel JFET input stage macromodel are described in this section.

2.6.2.1 Slew rate

Consider the op amp (LF411) in a closed loop circuit as in Fig. 2.9a with a pulse at the input, the op amp passes through several states. Fig. 2.22 shows the input voltage, and the drain current of j_1 and j_2.

a) Positive slew rate: SR^+

The SPICE simulation (Fig. 2.22), shows that on the rising edge of the input, j_2 is active and j_1 is cutoff. The current flowing in the VCCS g_a is equal to I_{ss} . Then, the current I_{ss} flows out of c_2 because r_2 is usually a large resistance. The voltage across c_2 is almost equal to the output voltage. Thus, the positive slew rate is found to be

$$SR^{+}=\frac{I_{ss}}{c_2}$$

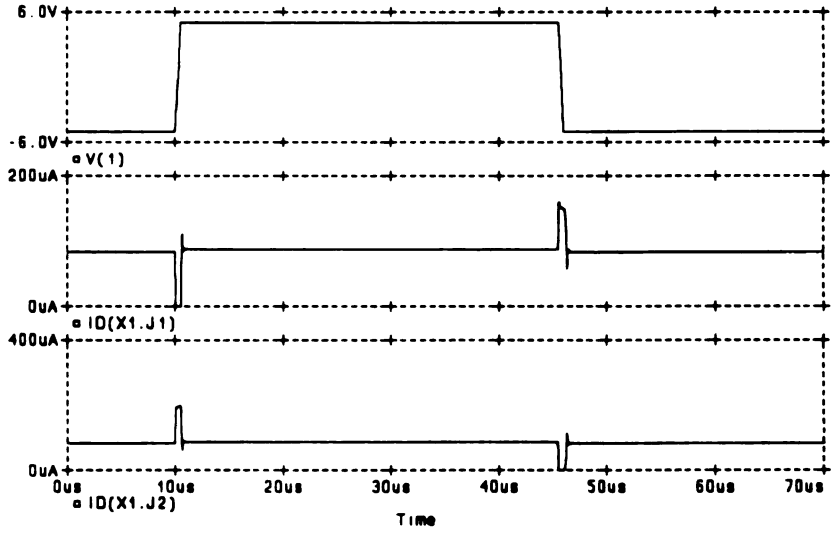

Figure 2.22 Drain current of j_1 and j_2

b) Negative slew rate: SR^-

At the falling edge of the input, the SPICE simulation (Fig. 2.22) shows that j_1 is active and j_2 is cutoff. At this case j_1 is operating as a source follower tracking the variation of the output voltage. The output voltage is all across the capacitor c_{ss}, then

$$SR^{-}=\frac{\Delta v_{out}}{\Delta t}=\frac{\Delta v_{css}}{\Delta t}=\frac{I_{css}}{c_{ss}}$$

where I_{css} is the current flowing in c_{ss}. Since the slope is negative, then I_{css} is negative quantity and it is pumped out of c_{ss}. The current flowing in r_{d1}, I_{rd1} is equal to the summation of I_{ss} and I_{css}, then

$$I_{rd1}=I_{ss}+SR^{-}c_{ss} \tag{2.43}$$

From equation 2.42

$$SR^{+}=\frac{I_{rd2}}{c_2}$$

but in this case

$$v_a=-r_{d1}I_{c2}$$

Therefore

$$SR^{-}=\frac{I_{rd1}}{c_2}$$

Then, using equation 2.43

$$-c_2SR^{-}=I_{ss}+SR^{-}c_{ss}$$

that is

$$SR^{-}=-\frac{I_{ss}}{c_2+c_{ss}}$$

The capacitance c_{ss} makes the slew rate asymmetric. That is SR^{+} is larger than SR^{-} in magnitude.

2.6.2.2 JFET parameters

The JFET used at the input stage are presented in SPICE program by the simplest models which does not include internal capacitance and resistances.

The input currents flowing in the gate of j_1, j_2 are due to the saturation currents of both pn junctions. The required value of the saturation current specified in SPICE program as IS could be established once the input offset and bias current are given. The SPICE JFET model has two diodes connected to the gate. Thus the gate current, I_{Bi}, is twice the saturation current,IS_i, of the corresponding JFET, that is

$$I_{Bi}=-2IS_i$$

The input offset current, I_{io} is the difference between the two base currents,

$$I_{io}=I_{B2}-I_{B1}$$

The bias current, I_B is defined as follows

$$I_B=\frac{I_{B1}+I_{B2}}{2}$$

then, the saturation current IS_i for each JFET is found to be

$$IS_i=\frac{1}{2}(-I_B\pm\frac{I_{io}}{2})$$

In the case of the microsim model, the JFETs at the input stage are identical, therefore $I_{io} = 0$, and $IS_1 = IS_2 = IS$.

As it was mentioned previously, the input stage gain has a unity dc gain, that is

$$A_{v1}=g_m r_{di}=1 \tag{2.44}$$

where g_m is the transconductance defined as follows

$$g_m=2\sqrt{\beta\frac{I_{ss}}{2}}$$

using equation 2.44,

$$g_m=\frac{1}{r_{di}} \tag{2.50}$$

So obviously, the value of β could be established once the value of r_{di} is determined, where

$$\beta=\frac{1}{2I_{ss}r_{di}^{2}} \tag{2.45}$$

The input offset voltage, v_{io} could be modelled as the difference in the threshold voltages of the two JFETs used at the input. This threshold voltage in noted in SPICE program as VTO, that is v_{io} is equal to

$$v_{io}=VTO_1-VTO_2$$

where VTO_1 and VTO_2 are respectively the threshold voltage of j_1, j_1. Since j_1 and j_2 have the same VTO, then v_{io} = 0 V. So the microsim did not model the input offset current and the input offset voltage fot this type of op amp macromodel. However from SPICE measurement, it shows that vio is different from zero and that is because of the voltage drop across r_{ss}. v_{io} is found to be equal to

$$v_{io}=-\frac{g_{cm}}{\sqrt{2\beta I_{ss}}}\left[\sqrt{\frac{I_{ss}}{2\beta}}-VTO+v_{99}\right]-\frac{v_{99}}{r_{o2}a_1\sqrt{2\beta I_{ss}}}$$

2.6.2.3 Input stage gain: r_{di}

The intermediate and output stage design equations of the JFET input stage macromodel are the same as the bipolar input stage macromodel except for some minor changes due to the notation.

2.6.2.4 Input stage: r_{ss}

The resistance r_{ss} is added for the same purpose as r_{ee} in case of bipolar input stage macromodel and is defined as

$$r_{ss}=\frac{V_A}{I_{ss}}$$

where V_A is the early voltage of the device.

2.6.2.5 Intermediate and output stage

Since, the intermediate stage and output stage are exactly the same as the bipolar op amp macromodel, the previous analysis holds for this op amp macromodel. Therefore, the other design equation are the same as the bipolar input stage.

2.6.3 Design procedure

A summary of the design equations for the macromodel parameters is developed in this section. The following design procedure could be used for any op amp microsim model with a n-channel JFETs at the input stage. Given the following specifications: SR^+, SR^-, I_B, A_{dmo}, GBP, f_μ, ϕ_{pm}, CMRR, $r_{o\text{-}ac}$, $r_{o\text{-}dc}$, I_{sc+}, I_{sc-}, v_{sat+}, v_{sat-} and p_d, then the design procedure is

Step 1: Choose $c_2 = c_c$ where c_c is used in the chip as a compensation capacitance.

Step 2: $$I_{ss} = c_2 SR^+$$

Step 3: $$c_{ss} = \frac{I_{ss}}{-SR^-} - c_2$$ Assuming $SR^+ > -SR^-$.

Step 4: Choose the saturation current of the two JFETs to be equal to 12.5 pA and VTO = -1 V.

Step 5: $$r_{di} = \frac{1}{2\pi c_2 GBP}$$

Step 6: $$\beta = \frac{1}{2 I_{ss} r_{di}^2}$$

Step 7: Choose $V_A = 200$ V, then $$r_{ss} = \frac{V_A}{I_{ss}}$$

Step 8: $$c_1 = \frac{\tan|90° - \phi_{pm}|}{4\pi f_\mu r_{di}}$$

Step 9: $$g_a = \frac{1}{r_{di}}$$

Step 10: $$g_{cm} = \frac{1}{CMMR r_{di}}$$

Step 11: Choose r_2 = 100 kΩ.

Step 12: $$r_{o2} = r_{o-dc} - r_{o-ac}$$

$$r_{o1} = r_{o-ac}$$

Step 13: $$a_1 = \frac{A_{dmo} r_{di}}{r_{o2}}$$

Step 14: Pick $-a_2 = a_3 = a_4 = -a_5 = a_1$, and then round them off.

Step 15: Choose the diode saturation current for all the diodes used in the model to be equal to 8E-16 A and the diode ohmic resistance r_s to be 1 Ω.

Step 16: Choose α = 1 K

Step 17: $$v_{lp} = \alpha I_{sc+} - v_T \ln \frac{a_1 I_{ee}}{a_4 IS_{dlp}}$$

Step 18: $$v_{ln} = -\alpha I_{sc-} - v_T \ln - \frac{a_1 I_{ee}}{a_5 IS_{dln}}$$

Step 19: $$v_c = v_{p+} - v_{sat+} + v_T \ln - \frac{a_1 I_{ee}}{a_2 IS_{dc}}$$

Step 20: $$v_e = v_{p-} + v_{sat-} + v_T \ln \frac{a_1 I_{ee}}{a_3 IS_{de}}$$

Step 21: $$r_p = \frac{(v_{p+} - v_{p-})^2}{p_d - (v_{p+} - v_{p-}) I_{ee}}$$

Step 22: $$E_{GND} = \frac{v_{p+} + v_{p-}}{2}$$

2.6.4 Numerical example

This verification is done by finding the specifications of the model using the model formulas derived in the previous section and the macromodel parameter's values given in Table 2.6. Table 2.7 includes the calculated and the SPICE simulated measurements using the LF411 microsim macromodel as an example. A list of the equations used to find the calculated measurements are listed below.

1) $$SR^+ = \frac{I_{ss}}{c_2}$$

2) $$SR^- = -\frac{I_{ss}}{c_2 + c_{ss}}$$

3) $$I_B = -2IS$$

4) $$v_{io}=-\frac{g_{cm}}{\sqrt{2\beta I_{ss}}}\left[\sqrt{\frac{I_{ss}}{2\beta}}-VTO+v_{99}\right]-\frac{v_{99}}{r_{o2}a_1\sqrt{2\beta I_{ss}}}$$

5) $$f_0=\frac{1}{2\pi c_2 a_1 r_{o2}}$$

6) $$A_{dmo}=a_1 g_a r_{o2}$$

7) $$GBP=\frac{g_a}{2\pi c_2}$$

8) $$f_\mu=\sqrt{\frac{-f_2^2+\sqrt{f_2^4+4A_{dmo}^2 f_0^2 f_2^2}}{2}}$$

where $$f_2\frac{1}{4\pi r_{di} c_1}$$

9) $$\phi_{pm}=90^\circ-\arctan\frac{f_\mu}{f_2}$$

10) $$CMMR=\frac{1}{r_{di}g_{cm}}$$

11) $$r_{o-ac}=r_{o1}$$

12) $$r_{o\text{-}dc}=r_{o1}+r_{o2}$$

13) $$I_{sc+}=\frac{1}{\alpha}(v_{lp}+v_T\ln\frac{a_1 I_{ee}}{a_4 IS_{dlp}})$$

14) $$I_{sc-}=-\frac{1}{\alpha}(v_{ln}+v_T\ln-\frac{a_1 I_{ee}}{a_5 IS_{dln}})$$

15) $$v_{sat+}=v_{p+}-v_c+v_T\ln-\frac{a_1 I_{ee}}{a_2 IS_{dc}}$$

16) $$v_{sat-}=v_{p-}+v_e-v_T\ln\frac{a_1 I_{ee}}{a_3 IS_{de}}$$

17) $$p_d=(v_{p+}-v_{p-})I_{ee}+\frac{(v_{p+}-v_{p-})^2}{r_p}$$

Table 2.7 Parameters of the LF411

Parameter	Calculated	Simulated
SR^+	17 V/μs	19.6 V/μs
SR^-	-11.975 V/μs	-15.07V/μs
v_{io}	-6.691 μV	-3.25 μV
I_B	-25 pA	-40.32 pA
f_0	20.000 Hz	19.95 Hz
A_{dmo}	106.02 dB	112 dB
GBP	4 MHz	7.942 MHz
f_μ	3.292 MHz	5.412 MHz
ϕ_{pm}	55.37°	41.4°
CMRR	100 dB	106.07 dB
r_{o-ac}	50 Ω	50 Ω
r_{o-dc}	75 Ω	76.38 Ω
I_{sc+}	25.675 mA	25.68 mA
I_{sc-}	-25.675 mA	-25.68 mA
v_{sat+}	14.175 V	14.17 V
v_{sat-}	-14.175 V	-14.17 V
p_d	65.1 mW	65.1 mW

Lots of the simulated measurements obtained in the above table do not match the calculated measurements such as A_{dmo}, GBP, f_μ, ϕ_{pm} amd CMRR due to the wrong definition of β used by the microsim in Table 2.6. While using the β definition given in equation 2.45 and the same values of I_{ss} and r_{di} given in Table 2.6, the value of β reduces by a factor of 4.

Also the bias current is off because SPICE program models the open circuit by

a large resistance of 1E12 Ω value between the gate and the channels this causes a leakage current flowing out of the gate. Therefore the base cuurent calculated in the above table does not match the simulated one. In order to avoid the effect of these resistances we connect other resistances between the gate and the channels with a -1E12 Ω value. Table 2.8 shows the simulated measurements of the revised model. Thus, the two measurements are comparable.

Table 2.8 Revised parameters of the LF411

Parameter	Calculated	Simulated
SR^+	17 V/μs	19.6 V/μs
SR^-	-11.975 V/μs	-14.9 V/μs
v_{io}	-3.237 μV	-3.2 μV
I_B	-25 pA	-25 pA
f_0	20.000 Hz	19.95 Hz
A_{dmo}	106.02 dB	106 dB
GBP	4 MHz	3.98 MHz
f_μ	3.292 MHz	3.286 MHz
ϕ_{pm}	55.37°	55.4°
CMRR	100 dB	100 dB
$r_{o\text{-}ac}$	50 Ω	50 Ω
$r_{o\text{-}dc}$	75 Ω	76.38 Ω
I_{sc+}	25.675 mA	25.68 mA
I_{sc-}	-25.675 mA	-25.68 mA
v_{sat+}	14.175 V	14.17 V
v_{sat-}	-14.175 V	-14.17 V
p_d	65.1 mW	65.1 mW

CHAPTER 3

Linear Technology Model (LTC)

3.1 Introduction

In this chapter, the structure and basic operations of another op amp macromodel called linear technology model (LTC), are described [2]. Fig. 3.1 shows a schematic circuit of a JFET p-channel input stage macromodel. The LTC macromodel is designed by using elements inherent to SPICE such as using ideal controlled source stages instead of transistors, and generally minimizes the number of pn junctions [2]. Like the microsim model, two basic controlled sources dominate this op amp macromodel: the VCVS and the VCCS.

As mentioned in the first chapter a good macromodel design is one that shows a useful reduction in simulation time and memory usage. If improving a macromodel results in a very complex circuit, then we maybe better off to model the op amp at the electronic device level.

The LTC model is called a modified Boyle model [2], and can model virtually any input differential transconductance stage [2]. Therefore, it can be adapted to any op amp

with an npn, pnp, JFET or MOSFET input stage [2]. Obviously the LTC model is a more complex macromodel.

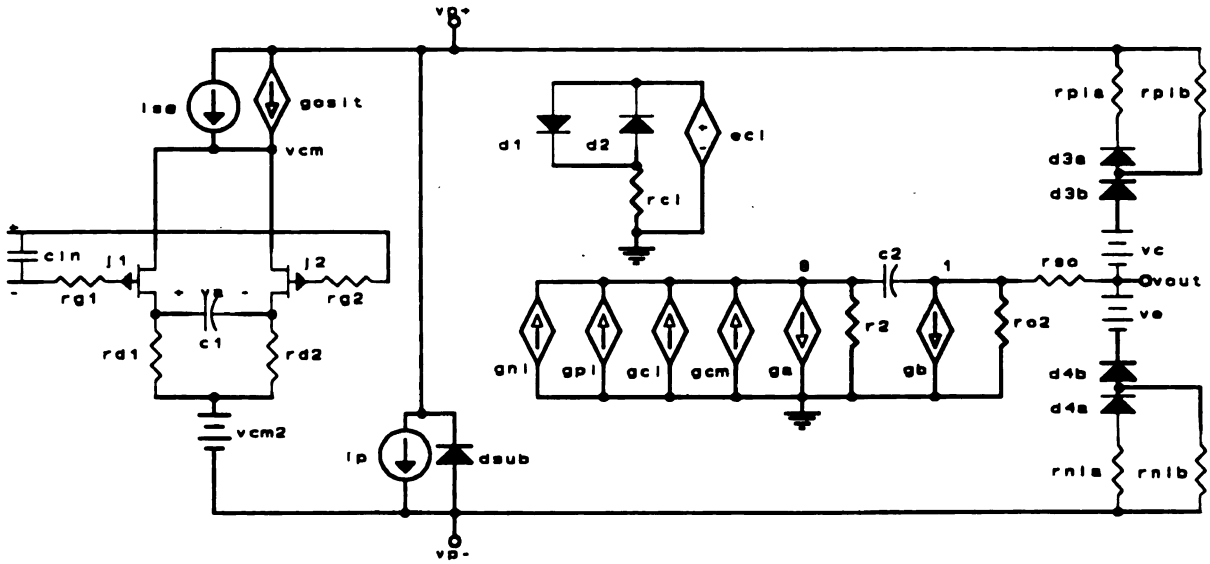

Figure 3.1 LTC macromodel of the LF355

Table 3.1 SPICE file of the LF355 macromodel

```
* Linear Technology LF355
* Connections: +   -  V+ V- O
.SUBCKT LF355  3  2  7  4  6
* INPUT
VCM2 40 4 2.0000E+00
RD1 40 80 2.1221E+03
RD2 40 90 2.1221E+03
J1 80 102 12 JM1
J2 90 103 12 JM2
CIN 2 3 4.0000E-12
RG1 2 102 2.0000E+00
RG2 3 103 2.0000E+00
C1 80 90 1.5000E-11
ISS 7 12 2.4000E-04
GOSIT 7 12 90 80 1.2000E-04
* INTERMEDIATE
GCM 0 8 12 0 4.7124E-09
GA 8 0 80 90 4.7124E-04
R2 8 0 1.0000E+05
C2 1 8 3.0000E-11
GB 1 0 8 0 4.2768E+01
RO2 1 0 9.9000E+01
* OUTPUT
RSO 1 6 1.0000E+00
ECL 18 0 1 6 1.9963E+01
GCL 0 8 20 0 1.0000E+00
RCL 20 0 1.0000E+03
D1 18 20 DM1
D2 20 18 DM1
D3A 131 70 DM3
D3B 13 131 DM3
GPL 0 8 70 7 1.0000E+00
VC 13 6 3.1360E+00
RPLA 7 70 1.0000E+04
RPLB 7 131 1.0000E+05
D4A 60 141 DM3
D4B 141 14 DM3
GNL 0 8 60 4 1.0000E+00
VE 6 14 3.1360E+00
RNLA 60 4 1.0000E+04
RNLB 141 4 1.0000E+05
*
IP 7 4 1.7600E-03
DSUB 4 7 DM2
* MODELS
.MODEL JM1 PJF (IS=3.1500E-11
+ BETA=4.6264E-04 VTO=-1)
.MODEL JM2 PJF (IS=2.8500E-11
+ BETA=4.6264E-4 VTO=-9.97E-1)
.MODEL DM1 D (IS=1.0000E-15)
.MODEL DM2 D (IS=8.0000E-16
+ BV=4.3200E+01)
.MODEL DM3 D (IS=1.0000E-16)
.MODEL DM4 D (IS=1.0000E-09)
.ENDS LF355
```

3.2 Circuit Component and Operation

The LTC op amp macromodel can be divided into three basic building blocks: input stage, intermediate stage and output stage which includes the short circuit current and voltage limiting.

3.2.1 Input stage

The input stage is very similar to the microsim model input stage and is, also isolated from the rest of the stages to simplify the modeling of the slew rate and frequency response. The two transistors used at the input are represented in the SPICE program by the simplest models which does not include internal capacitances or resistances. They are at the input to model the linear and nonlinear differential mode and common mode input characteristics and provide the desired input offsets [2]. The input stage gain is chosen to be unity for the same reasons mentioned in chapter 2.

3.2.2 Intermediate stage

The element g_a, g_b, r_2, r_{o2} and c_2 provide the op amp gain and vary the frequency response characteristics. For a more simplified LTC model, the basic modeling equations follow exactly the original Boyle model [2]. The capacitance c_2, c_1 are used for the same reasons used in the microsim model.

3.2.3 Output stage

The output stage provides a dc and ac output resistance of the op amp by the two resistance r_{o2} and r_{so}.

The short current limiting which provides the desired maximum short circuit

current I_{sc}, consists of two back to back diodes d_1, d_2, a resistance r_{c1} and a VCVS e_{cl}, where v_{ecl} is the voltage across r_{so}. The diode d_1 provides current limiting for positive short circuit I_{sc+}, while d_2 is for negative short circuit current I_{sc-}.

The voltage limiting circuit is more complex than the microsim model voltage limiting circuit. The diodes d_{3a}, d_{3b} and VCCS g_{pl} form a positive voltage limiter, while d_{4a}, d_{4b} and VCCS g_{nl} form the negative voltage limiter.

3.3 Preview

The focus of the rest of the chapter is to develop expressions for the values of the elements of the macromodel. The starting point is to use SPICE simulations of a given macromodel to establish the basic design equations. Then, a general procedure will be developed for the parameter and element values of the linear technology macromodel. Finally, the last step is to check the design procedure by using a numerical example. This analysis will be done for a three different input stage macromodels: JFET p-channel input stage macromodel (LF355) and PMOS input stage macomodel (LTC1050).

3.4 JFET Input Stage Macromodel

One of the JFET p-channel input stage macromodel is the LF355. Its schematic diagram is shown in Fig. 3.1 and its corresponding SPICE file is shown in Table 3.1. Also, a schematic diagram of the LF355 full device is shown in Fig. 3.2 and its

corresponding SPICE file in Table 3.2 [3].

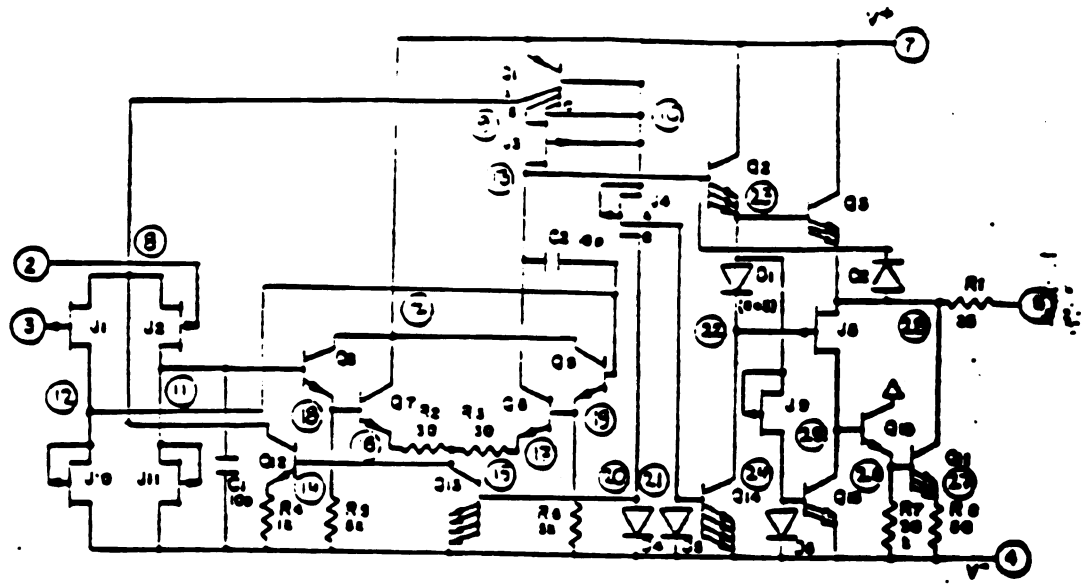

Figure 3.2 LF355 full device

Table 3.2 SPICE file of the LF355 full device [3]

```
*OP AMP LF355 DEVICE LEVEL
*CONNECTIONS   +  -  V+  V-  0
.SUBCKT LF355D 3  2  7   4   6
QD4 20 20 4 6 MOD3
QD5 21 21 4 6 MOD3
Q1C 10 10 7 6 MOD2 1
J4A 21 10 10  MOD4 4
J4B 20 10 10  MOD4 4
R2 16 15 30
R3 15 17 30
R4 14 4 1K
R5 18 4 5K
R6 19 4 5K
C1 11 4 10E-12
C2 13 12 10E-12
Q1A 8 10 7 6 MOD2 1
Q1B 9 10 7 6 MOD2 1
Q5 4 13 12 6 MOD2 1
Q6 7 11 18 6 MOD3
Q7 7 18 16 6 MOD3
Q8 13 19 17 6 MOD3
Q9 7 12 19 6 MOD3
Q12 8 15 14 6 MOD3 2
Q13 15 20 4 6 MOD3 4
J3 13 10 9 MOD4 10
J10 4 12 12 MOD4 3
J11 4 11 11 MOD4 3
R7 26 4 3K
R8 27 4 50
QD1 23 23 22 6 MOD3 3
QD6 24 24 4 6 MOD3
Q2 7 13 23 6 MOD3 3
Q3 7 23 28 6 MOD3 3
Q10 7 25 26 6 MOD3
Q11 28 26 27 6 MOD3 3
Q15 25 24 4 6 MOD3 2
J5 25 22 28 MOD4 2
J9 24 23 23 MOD4 1
R1 28 6 25
Q14 22 21 4 6 MOD3 4
J1 12 3 8 MOD4 5
J2 11 2 8 MOD4 5
.MODEL MOD2 PNP (BF=40 BR=.1
+ RB=500 RC=500 CJS=.21E-12
+ TF=25N TR=2.5U CJE=.5E-12
+ CJC=.21E-12 IS=3.5E-15 VAF=50)
.MODEL MOD3 NPN (BF=100 BR=.1
+ RB=500 RC=500 CJS=.21E-12
+ TF=1N TR=.5U CJE=.5E-12
+ CJC=.21E-12 IS=1E-15 VAF=250)
.MODEL MOD4 PJF (VTO=-1.0
+ BETA=.25E-4 LAMBDA=.01 RD=90
+ RS=90 CGS=2E-12 CGD=2E-12
+ PB=.6 IS = 1E-15)
.ENDS LF355D
```

3.4.1 SPICE test circuits

The same test circuits established using the npn input stage microsim macromodel, now will be established using the p-channel JFET input stage LTC macromodel such as the LF355. Table 3.3 provides the summarized data of the SPICE test circuits for the LF355 macromodel and full device.

3.4.2 Model formulas

3.4.2.1 Slew rate

The LTC models asymmetric slew rate for some chips by adding a VCCS designated g_{osit} (instead of using c_{ss} or c_e) which has no effect on the frequency response [2]. This VCCS modifies the total current available to j_1 and j_2. This source is driven by the differential output of j_1, j_2 and produces a current which adds to or substracts from the fixed current I_{ss}. Then, the current flowing to charge or discharge the compensation capacitance c_2 increases for one slewing slope and decreases for the opposite. Consider the unity gain buffer amplifier configuration, the op amp input stage passes through several states. Fig. 3.3 shows the drain current of the two JFET j_1, j_2.

a) Negative slew rate: SR^-

Fig. 3.3 shows that at the falling edge of the input j_2 is active and j_1 is cutoff. The current flowing in r_{d2}, I_{rd2} is equal to

$$I_{rd2}=I_{ss}-g_{osit}v_a$$

and $I_{rd1} = 0$, therefore

$$v_a=-(I_{ss}-g_{osit}v_a)r_{d2}$$

then

$$v_a = -\frac{I_{ss} r_{d2}}{1 - g_{osit} r_{d2}} \tag{3.1}$$

Since g_a is chosen to be equal to $1/r_{di}$, then the current flowing in the VCCS g_a is

$$g_a v_a = -\frac{I_{ss}}{1 - g_{osit} r_{d2}}$$

Since the voltage at node 8 noted, v_{gb}, is very small voltage and r_2 is a large resistance then most of the current (g_a v_a) flows out of c_2 then,

$$v_{c2} = \frac{I_{ss}}{1 - g_{osit} r_{d2}} \frac{1}{c_2} t$$

where v_{c2} is the voltage across c_2 (see Fig.3.4).

$$v_{c2} = -v_{out}$$

Hence

$$SR^- = -\frac{I_{ss}}{c_2} \frac{1}{1 - g_{osit} r_{d2}} \tag{3.2}$$

b) Positive slew rate: SR^+

Fig.3.3 shows that at the rising edge of the input j_1 is active and j_2 is cutoff. At this case j_1 is operating as a source follower tracking the variation of the output voltage. The current flowing in r_{d1}, I_{rd1} is equal to

$$I_{rd1} = I_{ss} - g_{osit} v_a$$

and now $I_{rd2} = 0$. Also

$$v_a=(I_{ss}-g_{osit}v_a)r_{d1}$$

then

$$g_a v_a=\frac{I_{ss}}{1+g_{osit}r_{d1}}$$

Since v_{gb} is very small voltage and r_2 is a very large resistance, then most of the current $g_a v_a$ flows through c_2, then

$$SR^{+}=\frac{I_{ss}}{c_2}\frac{1}{1+g_{osit}r_{d2}} \tag{3.3}$$

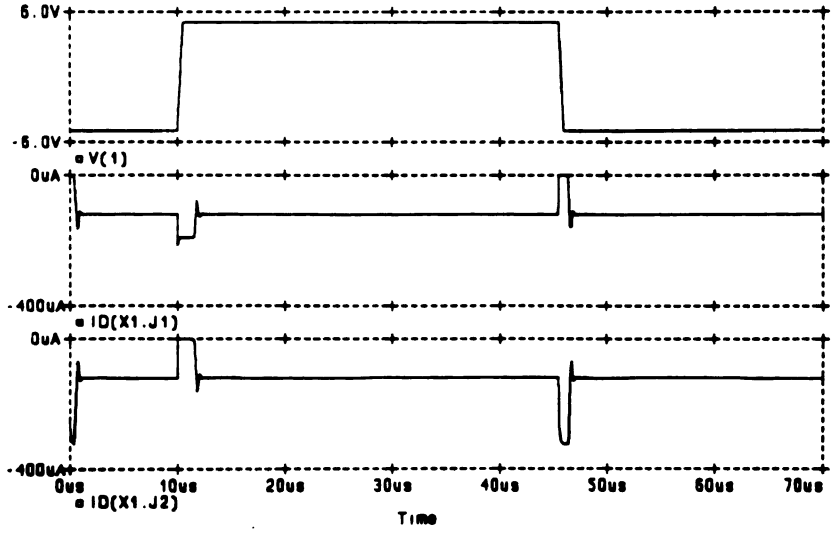

Figure 3.3 The drain current of j_1 and j_2

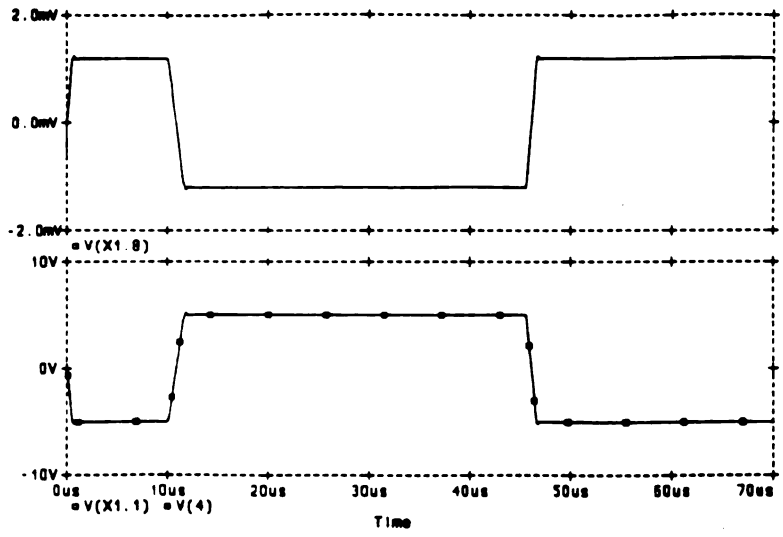

Figure 3.4 The voltage v_{gb} and v_{c2}

3.4.2.2 JFETs parameters

The JFETs parameters can be derived the same way done in chapter 2. These two JFETs used at the input stage have different threshold voltages and saturation currents so that the input offset current and the input offset voltage are different from zero.

3.4.2.3 Input stage: r_{di}

When the op amp macromodel is operating in the linear region, the current flowing through the VCCS g_{cl}, g_{pl} and g_{nl} are zero. For the differential mode and using Barlett's theorem [8], v_{cm} is shorted, therefore the current flowing in the VCCS g_{cm} is zero. Thus, the schematic circuit of the intermediate stage for the differential mode case

is shown in Fig.3.5. The resistance r_{so} is usually very small, thus the output voltage v_{out} is approximately equal to that at node voltage 1, v_1.

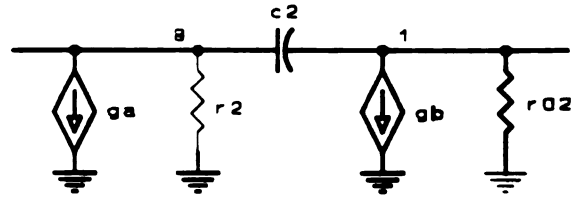

Figure 3.5 Intermediate stage at DM input

Since at dc, c_2 is an open circuit, then v_1 is equal to

$$v_1 = -g_b v_{g_b} r_{o2} = v_{out} \tag{3.9}$$

and

$$v_{gb} = -g_a v_a r_2 \tag{3.10}$$

Substituting equation 3.10 into 3.9 then

$$v_{out} = g_b g_a r_2 r_{o2} v_a \tag{3.11}$$

Since $v_a = v_d$, then the dc gain A_{dmo} is

$$A_{dmo} = g_b g_a r_2 r_{o2} \tag{3.12}$$

The previous analysis holds for very low frequencies where c_2 is an open circuit, but at higher frequencies c_2 becomes short and

$$v_{out} = -g_a v_a (r_{o2} \| \frac{1}{g_b} \| r_2) \tag{3.13}$$

$1/g_b << r_{o2} << r_2$ thus,

$$\frac{1}{g_b} \| r_{o2} \| r_2 = \frac{1}{g_b}$$

and from equation 3.13

$$v_{out} = -\frac{g_a v_a}{g_b}$$

which is very small, therefore a system pole must occur at low frequencies. The pole is found by using the one capacitor method [8]. To solve for the resistance seen by c_2, a test current source I_x is applied in parallel with the capacitance c_2 creating a voltage drop called v_x. v_{dm} is set to zero, thus $v_a = 0$, (see Fig. 3.6)

$$v_x = I_x r_2 + r_{o2}(g_b v_{gb} + I_x) \tag{3.14}$$

then

$$\frac{v_x}{I_x} = r_2 + r_{o2} g_b r_2 + r_{o2} \tag{3.15}$$

The above equation can be approximated as

$$\frac{v_x}{I_x} = r_{o2} g_b r_2$$

Hence, the resistance seen by c_2 is $r_{o2} \times g_b \times r_2$ and the frequency f_0 at which the pole occurs is

$$f_0 = \frac{1}{2\pi r_{o2} r_2 g_b c_2} \tag{3.16}$$

Using equation 3.12 and 3.16

$$GBP = \frac{1}{2\pi c_2 r_{di}} \tag{3.17}$$

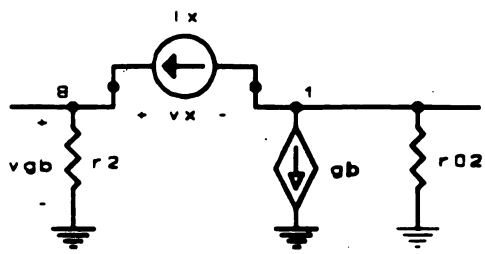

Figure 3.6 Resistance seen by c_2

3.4.2.4 Input stage: c_1

The second pole occurs at f_2 which is found to be equal to

$$f_2 = \frac{1}{4\pi c_1 r_{di}} \tag{3.18}$$

Following the same analysis done in chapter 2, the necessary value of c_1 to produce the second pole is

$$c_1 \frac{\tan|90° - \phi_{pm}|}{4\pi f_\mu r_{di}} \tag{3.19}$$

3.4.2.5 Interstage: g_{cm}

At low frequencies c_2 is an open circuit and

$$v_{gb}=g_{cm}r_2 \tag{3.20}$$

and

$$v_{out}=-g_b v_{gb} r_{o2} \tag{3.21}$$

Substituting equation 3.20 into equation 3.21

$$v_{out}=-g_{cm}g_b r_2 r_{o2} v_{cm} \tag{3.22}$$

then, the common mode gain A_{cm} is

$$|A_{cm}|=g_{cm}g_b r_2 r_{o2} \tag{3.23}$$

Using equation 3.12 and 3.23, the common mode rejection ratio is found to be

$$\text{CMMR}=\frac{1}{g_{cm}r_{di}} \tag{3.24}$$

3.4.2.6 DC power drain

To model the actual dc power dissipation of an op amp, a current source i_p is added into the macromodel. The power dissipation is

$$p_d=(v_{p.}-v_{p-})I_{ss}+(v_{p.}-v_{p-})i_p$$

Then, the necessary value of i_p to produce this dissipation is

$$i_p=\frac{p_d}{(v_{p.}-v_{p-})}-I_{ss} \tag{3.25}$$

A diode d_{sub} is used across i_p for the same reason as microsim model and it has a breakdown voltage which is equal to the maximum total supply voltage of the corresponding op amp.

3.4.2.7 Output stage: r_{so} and r_{o2}

The output stage provides the dc and ac output resistances. The output resistance usually depends on r_{so} and r_{o2} as was described in chapter 2. But for this type of macromodel this assumption is not valid anymore due to the short circuit current design. The test circuit used to find the output impedance is shown in Fig. 2.6a. At low frequencies, c_2 is open. When the current I_T flows through r_{so}, it creates a voltage drop which is fedback through a VCVS, e_{cl}. Thus the resistance r_{cl} also has a very small voltage drop across it. In SPICE program, when the diode is in the cutoff mode it is represented by a large resistance r = 1E12 Ω. Thus the voltage across r_{cl}, v_{cl} is

$$v_{cl}=I_T\frac{r_{so}r_{cl}e_{cl}}{r_{cl}+\frac{1}{2}r}$$

This voltage is fedback through the VCCS, g_{cl} and creates a voltage drop across r_2, noted

v_b. Since the current through c_2 is almost zero, then the current through VCCS g_b is

$$v_b g_b = I_T \frac{r_{so} r_{cl} r_2 g_{cl} g_b e_{cl}}{r_{cl} + \frac{1}{2} r}$$

The output voltage, v_{out} is found to be

$$v_{out} = I_T r_{so} + I_T \left(1 + \frac{r_{so} r_2 r_{cl} g_{cl} g_b e_{cl}}{r_{cl} + \frac{1}{2} r}\right) r_{o2}$$

Hence the dc output impedance is

$$r_{o-dc} = \frac{v_{out}}{I_T} = r_{so} + r_{o2} \left(1 + \frac{r_2 r_{so} r_{cl} g_{cl} g_b e_{cl}}{r_{cl} + \frac{1}{2} r}\right)$$

At higher frequencies, c_2 is shorted and the ac output impedance is

$$r_{o-ac} = r_{so} + \left(r_2 \| \frac{1}{g_b} \| r_{o2}\right) \approx r_{so} \qquad (3.27)$$

3.4.2.8 Output stage: current limiting

When the output is shorted and current limiting occurs, a predetermined voltage appears across r_{cl} which controls the current in VCCS g_{cl} to absorb the current from the main signal path through the VCCS g_a [2]. The voltage across the diode is used to adjust the desired sinking and sourcing current limits.

a) Sourcing current: I_{sc+}

The short circuit, I_{sc+}, flows through r_{so} creating a voltage drop, v_{ecl} across r_{so}, so

$$v_{ecl}=r_{so}I_{sc}. \tag{3.28}$$

The voltage v_{ecl} controls the VCVS e_{cl}, where

$$v_{ecl}e_{cl}=v_{dl}+v_{gcl}$$

v_{dl} is the diode voltage drop across d_1 and v_{gcl} is the voltage across the resistance r_{cl}. Substituting equation 3.28 into the above equation, e_{cl} is found to be,

$$e_{cl}=\frac{v_{dl}+v_{gcl}}{r_{so}I_{sc}} \tag{3.29}$$

The current flowing in the VCCS g_a is equal to the current (I_{ss} - g_{osit} v_a), as well as the VCCS g_{cl}. This is verified by using SPICE program (see Fig. 3.7), that is

$$g_a v_a=g_{cl}v_{gcl}=I_{ss}-g_{osit}v_a \tag{3.30}$$

For a simpler design procedure, g_{cl} is usually picked to be 1 Ω^{-1}, then the value of v_{gcl} is determined by using equation 3.30

$$v_{gcl}=\frac{I_{ss}}{g_{cl}}\left(\frac{g_a}{g_a+g_{osit}}\right) \tag{3.31}$$

The current flowing in the diode d_1, I_{dl}, is the same current flowing in r_{cl}, thus

$$I_{dl}=\frac{v_{gcl}}{r_{cl}} \tag{3.32}$$

Substituting equation 3.31 into 3.32 then

$$I_{dl}=\frac{I_{ss}}{g_{cl}r_{cl}}\left(\frac{g_a}{g_a+g_{osit}}\right) \tag{3.33}$$

So now, the current I_{d1} is determined once the value of r_{c1} is determined. For the p-channel JFET op amp macromodel, r_{c1} is chosen to have the value of 1 kΩ . The voltage across the diode d_1, v_{d1}, is established from the diode equation,

$$v_{d1}=v_T \ln\frac{I_{d1}}{IS_{d1}} \tag{3.34}$$

The diode saturation current IS_{d1}, specified in SPICE program as IS, is chosen to have the value 1E-15 A. Then, substituting equation 3.33 into 3.34

$$v_{d1}=v_T \ln\frac{I_{ss}g_a}{g_{c1}r_{c1}IS_{d1}(g_a+g_{osit})} \tag{3.35}$$

So now, the value of e_{c1} could be established by substituting equation 3.35 and 3.31 into 3.29

$$e_{c1}=\frac{1}{r_{so}I_{sc+}}\left[v_T \ln\left(\frac{I_{ss}g_a}{g_{c1}r_{c1}IS_{d1}(g_a+g_{osit})}\right)+\frac{I_{ss}g_a}{g_{c1}(g_a+g_{osit})}\right] \tag{3.36}$$

b) Sinking current: I_{sc-}

The negative short circuit current, I_{sc-}, flows through r_{so} creating a voltage drop, v_{ec1}, across r_{so}

$$v_{ec1}=r_{so}I_{sc-} \tag{3.37}$$

The voltage v_{ec1} controls the VCVS e_{c1}, where

$$V_{ec1}e_{c1}=v_{gc1}-v_{d2}$$

v_{d2} is the diode voltage drop across d_2. Substituting equation 3.37 into the above equation, e_{c1} is found to be

$$e_{cl}=\frac{v_{gcl}-v_{d2}}{r_{so}I_{sc-}}$$

The current flowing in VCCS g_a is now equal to the $-(I_{ss} - g_{osit}\, v_a)$ as well as the VCCS g_{cl}. That is

$$-g_a v_a=-g_{cl}g_{gcl}=I_{ss}-g_{osit}v_a$$

Then

$$v_{gcl}=-\frac{I_{ss}}{g_{cl}}\left(\frac{g_a}{g_a-g_{osit}}\right)$$

Therefore

$$I_{d2}=-\frac{v_{gcl}}{r_{cl}}$$

Hence

$$v_{d2}=v_T\ln\left(\frac{I_{ss}}{g_{cl}r_{cl}IS_{d2}}\left(\frac{g_a}{g_a-g_{osit}}\right)\right)$$

So the value of e_{cl} in terms of I_{sc-} is found to be

$$e_{cl}=-\frac{1}{r_{so}I_{sc-}}\left[v_T\ln\left(\frac{I_{ss}}{g_{cl}r_{cl}IS_{d2}}\left(\frac{g_a}{g_a-g_{osit}}\right)+\frac{I_{ss}g_a}{g_{cl}(g_a-g_{osit})}\right]\right.$$

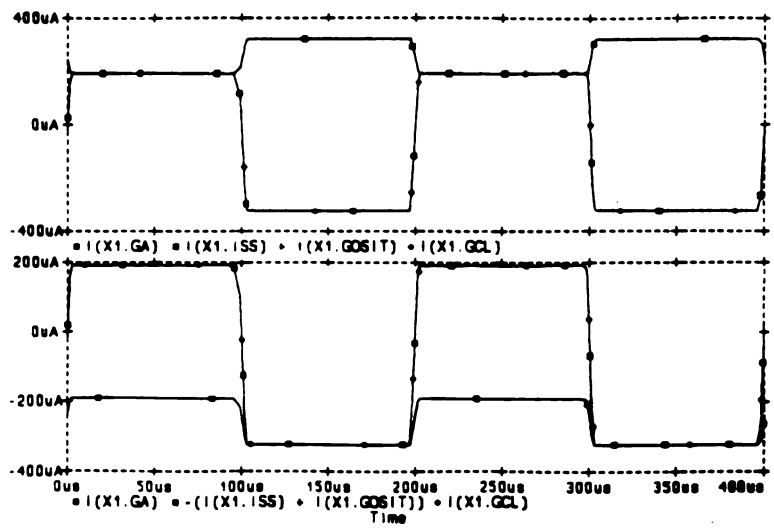

Figure 3.7 The current flowing through g_a and g_{cl}

3.4.2.9 Output stage: voltage limiting

a) Positive output voltage

When the output is clamped positive, a predetermined voltage drop occurs across r_{pla} which controls the VCCS g_{pl} to absorb the main current flowing in g_a, then

$$g_a v_a = v_{gpl} g_{pl} = I_{ss} - g_{osit} v_a \tag{3.37}$$

For a simpler design procedure, g_{pl} is chosen to have the value 1 Ω^{-1}. From equation 3.37

$$v_{gpl} = \frac{I_{ss}}{g_{pl}} \left(\frac{g_a}{g_a + g_{osit}} \right) \tag{3.38}$$

The voltage v_c is equal to

$$v_c = v_{p+} - v_{sat+} + v_{d3a} + v_{d3b} \tag{3.39}$$

where v_{d3a} and v_{d3b} are respectively the voltage drop across d_{3a} and d_{3b}. These two diodes are identical and have the same saturation current specified in SPICE as IS and is chosen to be equal to 1E-16 A. The current in the diode d_{3a}, I_{d3a} is the same current flowing in r_{pla}, thus

$$I_{d3a} = \frac{v_{gpl}}{r_{pla}} \tag{3.40}$$

Therefore, by selecting the value of r_{pla} one can determine the value of v_{d3a} by substituting equation 3.38 and 3.40 into the diode equation,

$$v_{d3a} = v_T \ln\left(\frac{I_{ss}}{g_{pl} r_{pla} IS_{d3}} \left(\frac{g_a}{g_a + g_{osit}}\right)\right) \tag{3.41}$$

The voltage across r_{plb} is the summation of v_{d3a} and v_{gpl}, then, the current flowing through r_{plb}, I_{rplb} is

$$I_{rplb} = \frac{v_{d3a} + v_{gpl}}{r_{plb}} \tag{3.42}$$

In order to determine the voltage v_{d3b}, one needs to find the current I_{d3b} flowing through it which is defined by the following equation,

$$I_{d3b} = I_{rplb} + I_{d3a} \tag{3.43}$$

Substituting equation 3.40 and 3.42 into 3.43

$$I_{d3b}=\frac{v_{d3a}}{r_{p1b}}+v_{gp}\left(\frac{1}{r_{p1a}}+\frac{1}{r_{p1b}}\right) \tag{3.44}$$

Since the voltage v_{gp} is much smaller than v_{d3a}, then equation 3.44 becomes as follows,

$$I_{d3b}\approx\frac{v_{d3a}}{r_{p1b}} \tag{3.45}$$

Substituting equations 3.41 and 3.38 into 3.45

$$I_{d3b}=\frac{v_T}{r_{p1b}}\ln\left(\frac{I_{ss}}{g_{p1}r_{p1a}IS_{d3a}}\left(\frac{g_a}{g_a+g_{osit}}\right)\right) \tag{3.46}$$

Hence

$$v_{d3b}=v_T\ln\left[\frac{1}{IS_{d3b}}\frac{v_T}{r_{p1b}}\ln\left(\frac{I_{ss}}{g_{p1}r_{p1a}IS_{d3a}}\left(\frac{g_a}{g_a+g_{osit}}\right)\right)\right] \tag{3.47}$$

Finally, the expression for v_c is established after selecting a value for r_{p1b} and substituting equations 3.41 and 3.47 into 3.39

$$v_c\approx v_{p+}-v_{out+}+v_T\left[\ln\left(\frac{I_{ss}\left(\frac{g_a}{g_a+g_{osit}}\right)}{g_{p1}r_{p1a}IS_{d3a}}\right)+\ln\left(\frac{v_T}{r_{p1b}IS_{d3b}}\ln\frac{I_{ss}\left(\frac{g_a}{g_a+g_{osit}}\right)}{g_{p1}r_{p1a}IS_{d3a}}\right)\right]$$

b) Negative output voltage

When the output is clamped negative, a predetermined voltage drop occurs across r_{n1a} which will control the VCCS g_{n1} to absorbs the main current flowing through g_a

$$-g_a v_a=-v_{gp1}g_{p1}=I_{ss}-g_{osit}v_a \tag{3.48}$$

For a simpler design procedure, g_{n1} is chosen to have the value 1 Ω^{-1}. Using equation 3.48

$$v_{gnl} = -\frac{I_{ss}}{g_{nl}}\left(\frac{g_a}{g_a - g_{osit}}\right)$$

The voltage v_e is equal to

$$v_e = -v_{p-} + v_{sat-} + v_{d4a} + v_{d4b} \tag{3.48}$$

where v_{d4a} and v_{d4b} are respectively the voltage drop across the diodes d_{4a} and d_{4b}. These two diodes are identical to d_{3a} and d_{3b} and have the same saturation current. The expression of v_e can be established by following the same procedure done previously. Also $r_{nla} = r_{pla}$ and $r_{nlb} = r_{plb}$, then

$$v_e = -v_{p-} + v_{sat-} + v_T\left[\ln\left(\frac{I_{ss}\left(\frac{g_a}{g_a - g_{osit}}\right)}{g_{nl} r_{nla} IS_{d4a}}\right) + \ln\left(\frac{v_T}{r_{nlb} IS_{d4b}} \ln \frac{I_{ss}\left(\frac{g_a}{g_a - g_{osit}}\right)}{g_{nl} r_{nla} IS_{d4a}}\right)\right]$$

3.4.3 Design procedure

A summary of the design equations for the p channel JFET linear technology macromodel is developed in this section. The starting point of the design is to have the corresponding op amp characteristics such as SR^+, SR^-, I_B, I_{io}, v_{io}, A_{dmo}, GBP, f_p, ϕ_{pm}, CMRR, r_{o-ac}, r_{o-dc}, I_{sc+}, I_{sc-}, v_{sat+}, v_{sat-} and p_d.

Step 1: Choose $c_2 = c_c$ where c_c is used in the chip as a compensation capacitance.

Step 2: $$r_{di} = \frac{1}{2\pi GBP c_2}$$

Step 3: $$g_a = \frac{1}{r_{di}}$$

Step 4: $$I_{ss} = \frac{2c_2}{\frac{1}{SR^+} - \frac{1}{SR^-}}$$

Step 5: $$g_{osit} = g_a\left(\frac{I_{ss}}{SR^+ c_2} - 1\right)$$

Step 6: $$\beta = \frac{g_a^2}{2I_{ss}}$$

Step 7: $$IS_1 = \frac{1}{2}\left(I_B + \frac{I_{io}}{2}\right)$$

$$IS_2 = \frac{1}{2}\left(I_B - \frac{I_{io}}{2}\right)$$

where IS_1, IS_2 are respectively the saturation currents of j_1, j_2.

Step 8: Choose $VTO_1 = -1$ V, and $VTO_2 = -1 - v_{io}$, where VTO_1, VTO_2 are respectively the threshold voltages of j_1, j_2.

Step 9: $$c_1 = \frac{\tan|90° - \phi_{pm}|}{4\pi f_\mu r_{di}}$$

Step 10: $$g_{cm}=\frac{1}{r_{di}CMRR}$$

Step 11: Choose $r_2 = 100\ k\Omega$

Step 12: $$g_b=\frac{A_{dmo}}{g_a r_2 r_{o2}}$$

Step 13: Choose $g_{cl} = 1\ \Omega^{-1}$, $r_{cl} = 1\ k\Omega$

Step 14: Choose the saturation current of the diode d_1 and d_2 to be equal to 1E-15 A.

Step 15: $$e_{cl}=\frac{1}{r_{so}I_{sc}+}\left[v_T \ln\left(\frac{I_{ss}\left(\frac{g_a}{g_a+g_{osit}}\right)}{g_{cl}r_{cl}IS_{d1}}\right)+\frac{I_{ss}\left(\frac{g_a}{g_a+g_{osit}}\right)}{g_{cl}}\right]$$

Step 16: Choose $r_{pla} = r_{nla} = 10\ k\Omega$

$$r_{plb} = r_{nlb} = 100\ k\Omega$$

$$g_{pl} = g_{nl} = 1\ \Omega^{-1}$$

Step 17: $$r_{so}=r_{o-ac}$$

$$r_{o2}=\frac{(r_{o-dc}-r_{o-ac})(r_{cl}+\frac{1}{2}r)}{r_{cl}+\frac{1}{2}r+r_2 r_{so} r_{cl} g_{cl} g_b e_{cl}}$$

Step 18: Choose the saturation currents of the diodes d_{3a}, d_{3b}, d_{4a} and d_{4b} to be equal

1E-16 A.

Step 19:

$$v_c = v_{p+} - v_{sat+} + v_T\left[\ln\left(\frac{\frac{I_{ss}\left(\frac{g_a}{g_a+g_{osit}}\right)}{g_{pl}r_{pla}IS_{d3a}}}{}\right) + \ln\left(\frac{v_T}{r_{plb}IS_{d3b}}\ln\left(\frac{\frac{I_{ss}\left(\frac{g_a}{g_a+g_{osit}}\right)}{g_{pl}r_{pla}IS_{d3a}}}{}\right)\right)\right]$$

Step 20:

$$v_e = -v_{p-} + v_{sat-} + v_T\left[\ln\left(\frac{\frac{I_{ss}\left(\frac{g_a}{g_a-g_{osit}}\right)}{g_{nl}r_{nla}IS_{d4a}}}{}\right) + \ln\left(\frac{v_T}{r_{nlb}IS_{d4b}}\ln\left(\frac{\frac{I_{ss}\left(\frac{g_a}{g_a-g_{osit}}\right)}{g_{nl}r_{nla}IS_{d4a}}}{}\right)\right)\right]$$

Step 21: Choose the saturation current of the diode d_{sub} to be equal to 8E-16 A.

Step 22: Set the breakdown voltage of the diode d_{sub} to be equal to the maximum supply voltage of the op amp.

Step 23:
$$i_p = \frac{p_d}{(v_{p+} - v_{p-})} - I_{ss}$$

Step 24: Choose c_{in} = input capacitance of the op amp.

Step 25: The voltage source v_{cm2} is picked such that it will simulates the negative common mode characteristics of some JFET amplifiers. In most of the cases is set to 2 V.

Step 26: Choose $r_{g1} = r_{g2} = 2\ \Omega$.

3.4.4 Numerical example

A numerical example is used to illustrate the development of the parameters of the op amp macromodel and to verify the design formulas and procedure. This verification is done by finding the specifications of the model using the model formulas derived in the previous section and the macromodel parameter's values given in Table 3.1. Table 3.3 includes the calculated and the SPICE simulated measurements using the LF355 macromodel as an example. A list of the equations used to find the calculated measurements are given below.

1) $$GBP=\frac{1}{2\pi c_2 r_{di}}$$

2) $$SR^{+}=\frac{I_{ss}}{c_2}\frac{1}{1+g_{osix}r_{d2}}$$

3) $$SR^{-}=-\frac{I_{ss}}{c_2}\frac{1}{1-g_{osix}r_{d2}}$$

4) $$v_{io}=VTO_1-VTO_2$$

5) $$I_B=IS_1+IS_2$$

6) $$I_{io}=2(IS_1-IS_2)$$

7) $$f_0=\frac{1}{2\pi r_{o2}r_2 g_b c_2}$$

8) $$A_{dmo}=g_b g_a r_2 r_{o2}$$

9) $$f_2=\frac{1}{4\pi c_1 r_{di}}$$

10) $$f_\mu=\sqrt{\frac{-f_2^2+\sqrt{f_2^4+4A_{dmo}^2 f_0^2 f_2^2}}{2}}$$

11) $$\phi_{pm}=90^\circ-\arctan\frac{f_\mu}{f_2}$$

12) $$CMRR=\frac{1}{g_{cm} r_{di}}$$

13) $$r_{o-ac}=r_{so}$$

$$r_{o-dc}=r_{so}+r_{o2}\left(1+\frac{r_{so} r_2 r_{cl} g_{cl} g_b e_{cl}}{r_{cl}+\frac{1}{2}r}\right)$$

14) $$I_{sc+}=\frac{1}{r_{so} e_{cl}}\left[v_T \ln\left(\frac{I_{ss}\left(\frac{g_a}{g_a+g_{osit}}\right)}{g_{cl} r_{cl} IS_{d1}}\right)+\frac{I_{ss}\left(\frac{g_a}{g_a+g_{osit}}\right)}{g_{cl}}\right]$$

15) $$I_{sc-}=-\frac{1}{r_{so}e_{cl}}\left[v_T\ln\left(\frac{I_{ss}\left(\frac{g_a}{g_a-g_{osit}}\right)}{g_{cl}r_{cl}IS_{d2}}\right)+\frac{I_{ss}\left(\frac{g_a}{g_a-g_{osit}}\right)}{g_{cl}}\right]$$

16) $$v_{sat+}=v_{p+}-v_c+v_T\left[\ln\left(\frac{I_{ss}\left(\frac{g_a}{g_a+g_{osit}}\right)}{g_{pl}r_{pla}IS_{d3a}}\right)+\ln\left(\frac{v_T}{r_{plb}IS_{d3b}}\ln\left(\frac{I_{ss}\left(\frac{g_a}{g_a+g_{osit}}\right)}{g_{pl}r_{pla}IS_{d3a}}\right)\right)\right]$$

17) $$v_{sat-}=v_{p-}+v_e-v_T\left[\ln\left(\frac{I_{ss}\left(\frac{g_a}{g_a-g_{osit}}\right)}{g_{nl}r_{nla}IS_{d4a}}\right)+\ln\left(\frac{v_T}{r_{nlb}IS_{d4b}}\ln\left(\frac{I_{ss}\left(\frac{g_a}{g_a-g_{osit}}\right)}{g_{nl}r_{nla}IS_{d4a}}\right)\right)\right]$$

18) $$p_d=(i_p+I_{ss})(v_{p+}-v_{p-})$$

Table 3.3 Parameters of the LF355

Parameter	Calculated	Simulated
SR^-	-10.733 V/μs	-10.70 V/μs
SR^+	6.376 V/μs	6.364 V/μs
v_{io}	-3 mV	-3.005 mV
I_{io}	6 pA	6.01 pA
I_B	60 pA	73.47 pA
f_0	12.5298 Hz	12.59 Hz
A_{dmo}	105.99 dB	105.9 dB
GBP	2.5 MHz	2.5 MHz
f_μ	1.965 MHz	1.979 MHz
ϕ_{pm}	51.82°	51.4°
CMRR	100 dB	100 dB
$r_{o\text{-}ac}$	1 Ω	1.023 Ω
$r_{o\text{-}dc}$	116.9 Ω	117.4 Ω
I_{sc+}	24.70 mA	24.72 mA
I_{sc-}	-25.383 mA	-25.40 mA
v_{sat+}	12.99 V	12.99 V
v_{sat-}	-13.01 V	-13.01 V
p_d	60.0 mW	59.5 mW

3.5 MOSFET Input Stage Macromodel

Some of the LTC macromodels have a PMOS input stage such as the LTC1050. Its design is very similar to the JFET input stage macromodel with of course a PMOS M_1,

M_2 replacing the JFETs j_1, j_2. This macromodel has been adapted to several op amps such as: LTC1051, LTC1049, LTC1052.... The schematic circuit of the LTC1050 is shown in Fig. 3.8 and its corresponding SPICE file in Table 3.4. The only differences between these two macromodels are the input stage and the short circuit current. The intermediate stage, the output stage including the voltage limiting remain exactly the same as was described for the JFET input stage LTC macromodel.

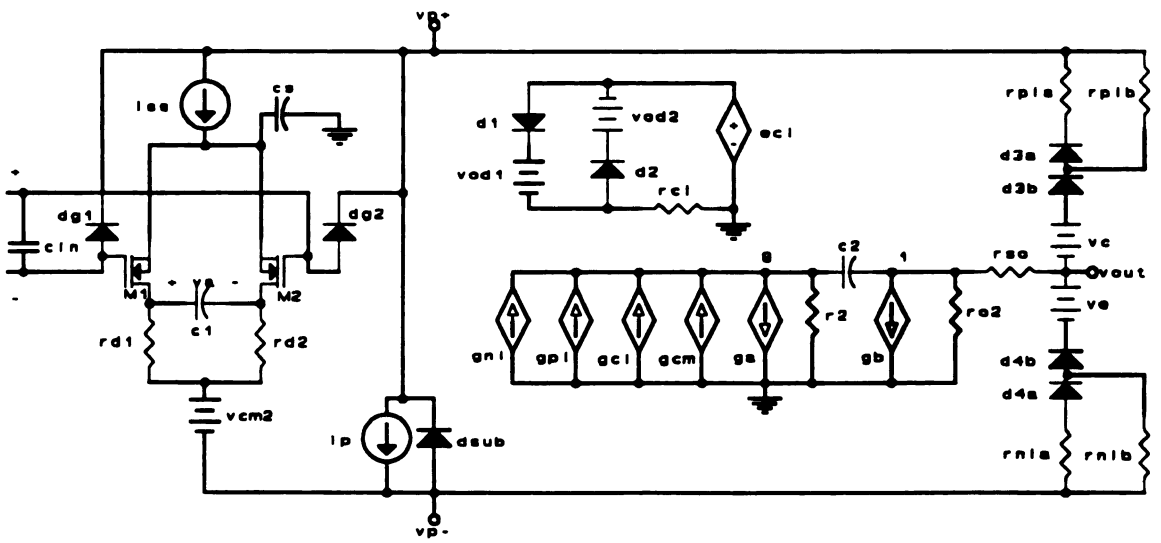

Figure 3.8 LTC macromodel of the LTC1050

Table 3.4 SPICE file of the LTC1050 macromodel

```
* Linear Technology LTC1050
* Connections:  + - V+ V- O
.SUBCKT LTC1050 3 2 7  4  6
* INPUT
RD1 4 80 2.1221E+03
RD2 4 90 2.1221E+03
M1 80 2 12 12 PM1
M2 90 3 12 12 PM2
CIN 2 3 5.0000E-12
DG1 2 7 DMG1
DG2 3 7 DMG2
C1 80 90 1.5000E-11
ISS 7 12 1.2000E-04
CS 12 0 1.2857E-11
* INTERMEDIATE
GCM 0 8 12 0 1.4902E-10
GA 8 0 80 90 4.7124E-04
R2 8 0 1.0000E+05
C2 1 8 3.0000E-11
GB 1 0 8 0 1.0664E+04
RO2 1 0 1.9900E+02
* OUTPUT
RSO 1 6 1.0000E+00
ECL 18 0 1 6 1.7955E+02
GCL 0 8 20 0 1.0000E+00
RCL 20 0 1.0000E+01
D1 18 19 DM1
VOD1 19 20 0.0000E+00
D2 20 21 DM1
VOD2 21 18 2.6932E+00
D3A 131 70 DM3
D3B 13 131 DM3
GPL 0 8 70 7 1.0000E+00
VC 13 6 1.4332E+00
RPLA 7 70 1.0000E+01
RPLB 7 131 1.0000E+03
D4A 60 141 DM3
D4B 141 14 DM3
GNL 0 8 60 4 1.0000E+00
VE 6 14 1.4332E+00
RNLA 60 4 1.0000E+01
RNLB 141 4 1.0000E+03
IP 7 4 8.8000E-04
DSUB 4 7 DM2
.MODEL PM1 PMOS (KP=1.8506E-3
+ VTO=-1.1000000E+00)
.MODEL PM2 PMOS (KP=1.8506E-3
+ VTO=-1.1000005E+00)
.MODEL DM1 D (IS=1.0000E-20)
.MODEL DM2 D (IS=8.0000E-16
+ BV=1.9800E+01)
.MODEL DM3 D (IS=1.0000E-16)
.MODEL DMG1 D (IS=2.0010E-11)
.MODEL DMG2 D (IS=9.9998E-15)
.ENDS LTC1050
```

3.5.1 SPICE test circuits

The same SPICE test circuits used for the JFET input stage macromodel, now may be used for the PMOS input stage macromodel such as the LTC1050. Table 3.5 provides the summarized measurements of the SPICE test circuits for the LTC1050. For this type of op amp, the maximum total supply voltage has to be less than or equal to 18 V.

3.5.2 Model formulas

The basic operation and design formulas of the PMOS input stage macromodel are described in this section.

3.5.2.1 Slew rate

This version of the macromodel, models the asymmetric slew rate by adding a capacitance c_s at the input stage. Consider the unity gain buffer amplifier configuration, the op amp input stage passes through several states. the two PMOS M_1, M_2.

a) Negative slew rate: SR^-

Using a SPICE simulation, we conclude that on the falling edge of the input M_2 is active and M_1 is cutoff. The current flowing in the VCCS g_s is equal to I_{ss} which flows out of c_2, since r_2 is usually a large resistance, the voltage across c_2 is almost equal to the output voltage. Then SR^- is found to be

$$SR^- = -\frac{I_{ss}}{c_2} \tag{3.49}$$

b) Positive slew rate: SR^+

Also on the rising edge of the input, M_2 is cutoff and M_1 is active. For this case M_1 is operating as a source follower tracking the variation of the output. The output voltage is all across the capacitor c_s. Then SR^+ is equal to

$$SR^{+}=\frac{dv_{out}}{dt}=\frac{dv_{cs}}{dt}=\frac{I_{cs}}{c_s} \tag{3.50}$$

where v_{cs} is the voltage across c_s and I_{cs} is the current flowing through it. Since the slope is positive then I_{cs} is positive and it is pumped through c_s.

The current flowing through r_{d1} is the difference between I_{ss} and I_{cs} that is

$$I_{rd1}=I_{ss}-I_{cs} \tag{3.51}$$

substituting equation 3.52 into 3.53

$$I_{rd1}=I_{ss}-SR^{+}c_s \tag{3.52}$$

Since on the rising edge of the input

$$v_a=I_{rd1}r_{d1}$$

then

$$SR^{+}=\frac{I_{rd1}}{c_2} \tag{3.53}$$

Using equation 3.53 in 3.52, then

$$SR^{+}c_2=I_{ss}-SR^{+}c_s \tag{3.54}$$

Finally, equation 3.54 gives,

$$SR^{+}=\frac{I_{ss}}{c_s+c_2} \tag{3.55}$$

3.5.2.2 MOSFET parameters

The input offset voltage v_{io} is modeled as a difference in the threshold voltages of the input MOSFETs specified in SPICE program as V_{TO}, so

$$v_{io}=VTO_1-VTO_2$$

where VTO_1 and VTO_2 are respectively the threshold voltages of M_1, M_2. The value of Kp can determined from the following equation

$$g_m=\sqrt{2K_p\frac{I_{ss}}{2}}$$

where g_m is the transconductance of the MOSFET and its value can be determined from the unity input stage gain A_{v1}, that is

$$A_{v1}=g_m r_{di}=1$$

Hence

$$g_m=\frac{1}{r_{di}} \qquad (3.56)$$

3.5.2.3 Intermediate stage

All the design equations developed for the intermediate stage of the JFET input LTC macromodel remain the same for the MOSFET input stage LTC macromodel.

3.5.2.4 Output stage: current limiting

Two voltage sources v_{od1}, v_{od2} have been added to the short circuit current used in the case of JFET input stage LTC macromodel as shown in Fig. 3.8a. These two souces are added because the positive and negative short circuit current are not equal in magnitude. This is one of the typical specs for the PMOS input stage LTC macromodel. While for the JFET input stage case I_{sc+} and I_{sc-} are almost equal in magnitude.

a) Sourcing current: I_{sc+}

The short circuit I_{sc+} flows through r_{so} creating a voltage drop v_{ecl} across r_{so}, so

$$v_{ecl}=r_{so}I_{sc}. \tag{3.57}$$

The voltage v_{ecl} controlls the vcvs e_{cl}, where

$$v_{ecl}e_{cl}=v_{d1}+v_{gcl}+v_{od1} \tag{3.58}$$

substituting equation 3.57 into 3.58, e_{cl} is found to be

$$e_{cl}=\frac{v_{d1}+v_{gcl}+v_{od1}}{r_{so}I_{sc+}} \tag{3.59}$$

The current flowing in the VCCS g_a is equal to the current I_{ss}, as well as the VCCS g_{cl}. This is verified using SPICE program, then

$$g_a v_a=g_{cl}v_{gcl}=I_{ss} \tag{3.60}$$

The value of g_{cl} is usually selected to be 1 Ω^{-1}. Then using equation 3.60

$$v_{gc1}=\frac{I_{ss}}{g_{c1}} \tag{3.61}$$

The current flowing in the diode d_1, I_{d1} is the same current flowing in r_{c1}, thus

$$I_{d1}=\frac{v_{gc1}}{r_{c1}} \tag{3.62}$$

Substituting equation 3.61 into 3.62,

$$I_{d1}=\frac{I_{ss}}{g_{c1}r_{c1}} \tag{3.63}$$

So now, the current I_{d1}, is determined once the value of r_{c1} is determined. For this type of op amp (PMOS input stage macromodel) r_{c1} is chosen to have the value of 10 Ω. The voltage across the diode d_1, v_{d1} is established from the diode equation once the saturation current of the diode d_1, IS_{d1} specified in SPICE as IS, is selected. Usually, for the PMOS input stage macromodel, IS_{d1} is equal to 1E-20 A. Then substituting equation 3.63 into the diode equation

$$v_{d1}=v_T\ln\frac{I_{ss}}{g_{c1}r_{c1}IS_{d1}} \tag{3.64}$$

Finally substituting equations 3.64 and 3.61 into 3.59

$$e_{c1}=\frac{1}{r_{so}I_{sc+}}\left[v_T\ln\left(\frac{I_{ss}}{g_{c1}r_{c1}IS_{d1}}\right)+\frac{I_{ss}}{g_{c1}}+v_{od1}\right] \tag{3.65}$$

The value of e_{c1} could be determined once the value of v_{od1} is solved.

b) Sinking current: I_{sc-}

Following the same procedure done for the positive short circuit, the expression

of e_{cl} could be established also from the following equation

$$e_{cl}=-\frac{1}{r_{so}I_{sc-}}[v_T\ln(\frac{I_{ss}}{g_{cl}r_{cl}IS_{d2}})+\frac{I_{ss}}{g_{cl}}+v_{od2}] \qquad (3.66)$$

where IS_{d2} is the saturation current of d_2 and is selected to be equal to IS_{d1}. So, we obtain two equations 3.65 and 3.66 but with three unknows. There are two cases to discuss.

Case 1: If $|I_{sc+}| < |I_{sc-}|$ then set $v_{od1} = 0$. Using equation 3.65, e_{cl} can be determined and then substituting its value into equation 3.66, then v_{od2} can be solved using the following equation

$$vo_{d2}=-e_{cl}I_{sc-}r_{so}+v_T\ln(\frac{I_{ss}}{g_{cl}r_{cl}IS_{d2}})+\frac{I_{ss}}{g_{cl}}$$

Case 2: If $|I_{sc+}| > |I_{sc-}|$ then set v_{od2} to zero. Using equation 3.66, e_{cl} can be determined. Substituting its value into equation 3.65 v_{od1} can be solved using the following equation

$$v_{od1}=e_{cl}I_{sc+}r_{so}-v_T\ln(\frac{I_{ss}}{g_{cl}r_{cl}IS_{d1}})-\frac{I_{ss}}{g_{cl}}$$

3.5.2.5 Intermediate stage and output stage

The PMOS input stage macromodel has the same intermediate and output stage including the voltage limiting as the JFET input stage macromodel. Therefore the design equations for this part remain the same as was done in the previous section for the JFET input stage macromodel.

3.5.3 Design procedure

The following design procedure could be used for any op amp linear technology macromodel with PMOS at the input stage. The starting point of the design are the corresponding op amp measurements such as: SR^+, SR^-, v_{io}, A_{dmo}, GBP, f_μ, ϕ_{pm}, CMRR, $r_{o\text{-}ac}$, $r_{o\text{-}dc}$, I_{sc+}, I_{sc-}, v_{sat+}, v_{sat-} and p_d

Step 1: Choose $c_2 = c_c$ where c_c is used in the chip as a compensation capacitance.

Step 2: $$I_{ss} = -SR^- c_2$$

Step 3: $$c_s = \frac{I_{ss}}{SR^+} - c_2$$

Step 4: $$r_{di} = \frac{1}{2\pi GBP c_2}$$

Step 5: $$g_a = \frac{1}{r_{di}}$$

Step 6: $$K_p = \frac{g_a^2}{I_{ss}}$$

Step 7: Choose $VTO_1 = -1$ V, and $VTO_2 = -1 - v_{io}$, where VTO_1, VTO_2 are respectively the threshold voltages of M_1, M_2.

Step 8: $$c_1 = \frac{\tan|90° - \phi_{pm}|}{4\pi f_\mu r_{di}}$$

Step 9: $$g_{cm}=\frac{1}{r_{di}CMRR}$$

Step 10: Choose $r_2 = 100\ k\Omega$

Step 11: $$g_b=\frac{A_{dmo}}{g_a r_2 r_{o2}}$$

Step 12: Choose $g_{c1} = 1\ \Omega^{-1}$, $r_{c1} = 10\ \Omega$

Step 13: Choose the saturation current of the diode d_1 and d_2 to be equal to 1E-20 A.

Step 14: If $|\ I_{sc+}\ | < |\ I_{sc-}\ |$ then, set $v_{od1} = 0$ V.

$$e_{c1}=\frac{1}{r_{so}I_{sc+}}[v_T\ln(\frac{I_{ss}}{g_{c1}r_{c1}IS_{d1}})+\frac{I_{ss}}{g_{c1}}]$$

and

$$v_{od2}=-e_{c1}r_{so}I_{sc-}+v_T\ln(\frac{I_{ss}}{g_{c1}r_{c1}IS_{d2}})+\frac{I_{ss}}{g_{c1}}$$

Step 15: If $|\ I_{sc+}\ | > |\ I_{sc-}\ |$ then, set $v_{od2} = 0$ V.

$$e_{c1}=-\frac{1}{r_{so}I_{sc-}}[v_T\ln(\frac{I_{ss}}{g_{c1}r_{c1}IS_{d1}})+\frac{I_{ss}}{g_{c1}}]$$

and

$$v_{od1}=e_{c1}r_{so}I_{sc+}-v_T\ln(\frac{I_{ss}}{g_{c1}r_{c1}IS_{d1}})-\frac{I_{ss}}{g_{c1}}$$

Step 16: $$r_{so}=r_{o-ac}$$

$$r_{o2}=\frac{(r_{o-dc}-r_{o-ac})(r_{cl}+\frac{1}{2}r)}{r_{cl}+\frac{1}{2}r+r_2 r_{so} r_{cl} g_{cl} g_b e_{cl}}$$

Step 17: Choose $r_{pla} = r_{nla} = 10\ \Omega$

$$r_{plb} = r_{nlb} = 1\ k\Omega$$

$$g_{pl} = g_{nl} = 1\ \Omega^{-1}$$

Step 18: Choose the saturation currents of the diodes d_{3a}, d_{3b}, d_{4a} and d_{4b} to be equal 1E-16 A.

Step 19:

$$v_c=v_{p+}-v_{sat+}+v_T[\ln(\frac{I_{ss}}{g_{pl}r_{pla}IS_{d3a}})+\ln(\frac{v_T}{r_{plb}IS_{d3b}}\ln(\frac{I_{ss}}{g_{pl}r_{pla}IS_{d3a}}))]$$

Step 20:

$$v_e=-v_{p-}+v_{sat-}+v_T[\ln(\frac{I_{ss}}{g_{nl}r_{nla}IS_{d4a}})+\ln(\frac{v_T}{r_{nlb}IS_{d4b}}\ln(\frac{I_{ss}}{g_{nl}r_{nla}IS_{d4a}}))]$$

Step 21: Choose the saturation current of the diode d_{sub} to be equal to 8E-16 A.

Step 22: Set the breakdown voltage of the diode d_{sub} to be equal to the maximum supply voltage of the op amp.

Step 23: $$i_p = \frac{p_d}{(v_{p+} - v_{p-})} - I_{ss}$$

Step 24: Choose c_{in} = input capacitance of the op amp.

3.5.4 Numerical example

A numerical example is used to illustrate the development of the parameters of the op amp macromodel and to verify the design formulas and procedure. This verification is done by finding the specifications of the model using the model formulas derived in the previous section and the macromodel parameter's values given in Table 3.4. Table 3.5 includes the calculated and the SPICE simulated measurments using the LTC1050 as an example. A list of the equations used to find the calculated measurements are listed below.

1) $$SR^- = -\frac{I_{ss}}{c_2}$$

2) $$SR^+ = \frac{I_{ss}}{c_2 + c_s}$$

3) $$GBP = \frac{1}{2\pi c_2 r_{di}}$$

4) $$v_{io} = VTO_2 - VTO_1$$

5) $$f_0=\frac{1}{2\pi r_{o2}r_2g_bc_2}$$

6) $$A_{dmo}=g_bg_ar_2r_{o2}$$

7) $$f_2=\frac{1}{4\pi c_1r_{di}}$$

8) $$f_\mu=\sqrt{\frac{-f_2^2+\sqrt{f_2^4+4A_{dmo}^2f_0^2f_2^2}}{2}}$$

9) $$\phi_{pm}=90^\circ-\arctan\frac{f_\mu}{f_2}$$

10) $$CMRR=\frac{1}{g_{cm}r_{di}}$$

11) $$r_{o-ac}=r_{so}$$

$$r_{o-dc}=r_{so}+r_{o2}\left(1+\frac{r_{so}r_2r_{cl}g_{cl}g_be_{cl}}{r_{cl}+\frac{1}{2}r}\right)$$

12) $$I_{sc+}=\frac{1}{r_{so}e_{cl}}\left[v_T\ln\left(\frac{I_{ss}}{g_{cl}r_{cl}IS_{d1}}\right)+\frac{I_{ss}}{g_{cl}}+v_{od1}\right]$$

13) $$I_{sc-}=-\frac{1}{r_{so}e_{cl}}\left[v_T\ln\left(\frac{I_{ss}}{g_{cl}r_{cl}IS_{d2}}\right)+\frac{I_{ss}}{g_{cl}}+v_{od2}\right]$$

14) $$v_{sat+}=v_{p+}-v_c+v_T\left[\ln\left(\frac{I_{ss}}{g_{pl}r_{pla}IS_{d3a}}\right)+\ln\left(\frac{v_T}{r_{plb}IS_{d3b}}\ln\left(\frac{I_{ss}}{g_{pl}r_{pla}IS_{d3a}}\right)\right)\right]$$

15) $$v_{sat-}=v_{p-}+v_e-v_T\left[\ln\left(\frac{I_{ss}}{g_{nl}r_{nla}IS_{d4a}}\right)+\ln\left(\frac{v_T}{r_{nlb}IS_{d4b}}\ln\left(\frac{I_{ss}}{g_{nl}r_{nla}IS_{d4a}}\right)\right)\right]$$

16) $$p_d=(i_p+I_{ss})(v_{p+}-v_{p-})$$

Table 3.5 Parameters of the LTC1050

Parameter	Calculated	Simulated
SR^+	2.8 V/μs	2.8 V/μs
SR^-	-4 V/μs	-4.12 V/μs
v_{io}	0.5 μV	0.0087 μV
f_0	25 mHz	27 mHz
A_{dmo}	160 dB	159.2 dB
GBP	2.5 MHz	2.46 MHz
f_μ	1.965 MHz	1.995 MHz
ϕ_{pm}	51.82°	51.5°
CMRR	130 dB	130 dB
$r_{o\text{-}ac}$	1 Ω	1 Ω
$r_{o\text{-}dc}$	962.05 Ω	961.3Ω
I_{sc+}	4.995 mA	5.002 mA
I_{sc-}	-20 mA	-20 mA
v_{sat+}	4.989 V	4.991 V
v_{sat-}	-4.989 V	-4.991 V
p_d	10 mW	10 mW

CHAPTER 4

Inaccuracies and Improvements of the Model

4.1 Introduction

In this chapter, some of the additional SPICE test circuits that were not performed in the previous chapters are introduced here. These tests do not contribute in determining the macromodel parameters, but they show some of the model inaccuracies and its failure to mimic the actual behavior of the corresponding full device. These consist of the supply current, asymmetric power supplies and finally the power supply rejection ratio (PSRR). In order to fix some of these failures, some elements are added to the macromodel as will be described in this chapter. These changes do not effect any of the original macromodel formulas.

4.2 Supply Current Test

The supply current SPICE test circuit consist of the op amp connected as a noninverting amplifier with a 10 KΩ load resistance. Then measure the curent

flowing through the positive and negative power supply pins.

4.2.1 Microsim model

The following test was performed on the μA741 macromodel and the full device. Fig. 4.1a shows the SPICE response of the μA741 full device. The current flowing in the positive power supply is coming into the chip, while the current flowing in the negative power supply is pumped out of the chip. Also as the output voltage increases, the load current increases, therefore the supply current increases through the positive and negative power supplies. If the output decreases, then the load current also decreases, thus the supply current decreases. In the case where the output is constant (clamped), the supply current is also constant (clamped). So the load current flows from the power supplies.

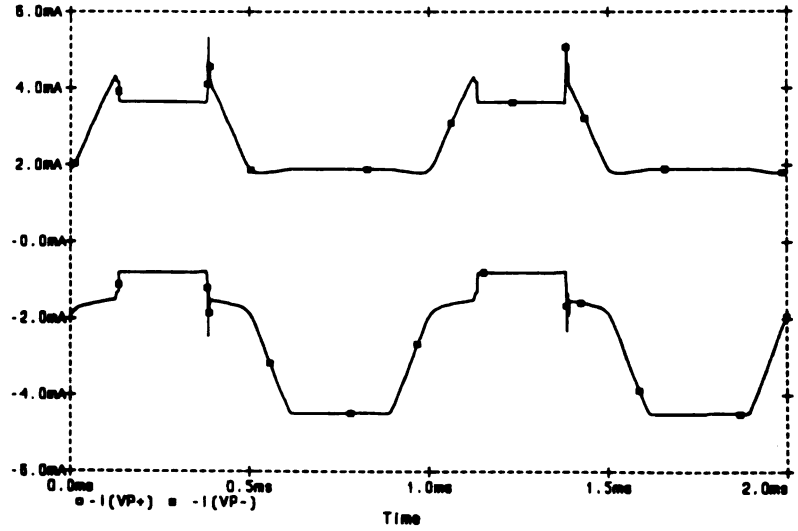

Figure 4.1a The supply current of the μA741 (full device)

Fig. 4.1b shows the supply current test response of the μA741 macromodel. The supply

current has the same direction as in the case of full device, but it remains constant as the output voltage increases or decreases. Thus the load current is not modeled as flowing from the power supplies. In order to fix such a porblem, the output current is fedback into the power supplies through a CCCS [8]. Hence the current flowing through the power supplies have the same variation as the load current. The diode d_{x1} and the CCCS f_{x1} are used for the positive load current while d_{x2} and f_{x2} are used for the negative load current. Fig. 4.2a shows the new output stage circuit, and Fig. 4.2b shows the corresponding response of the supply current test.

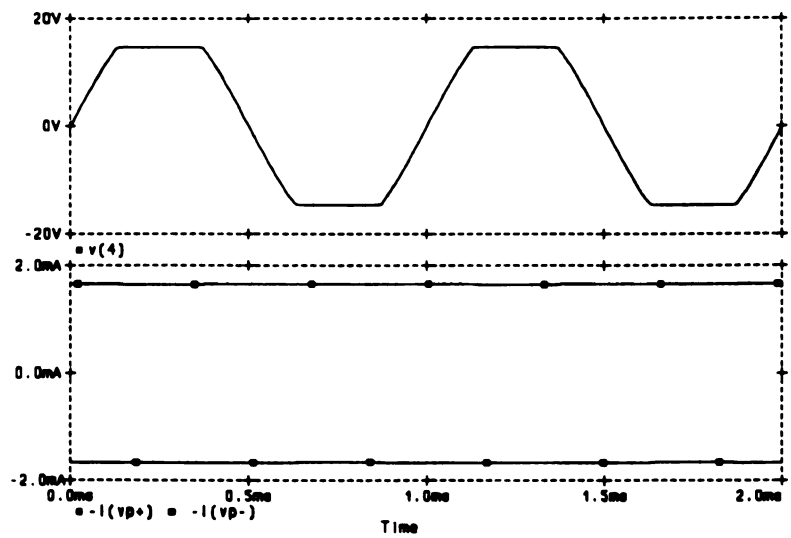

Figure 4.1b The supply current of the μA741 (macromodel)

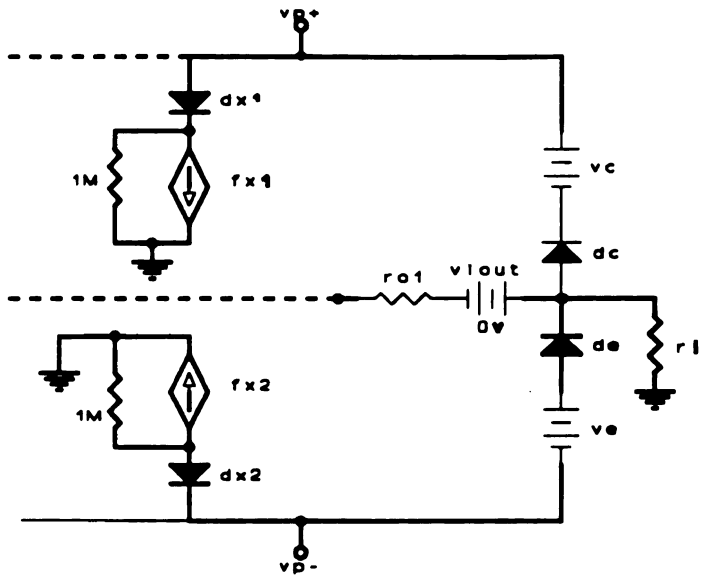

Figure 4.2a The new output stage circuit

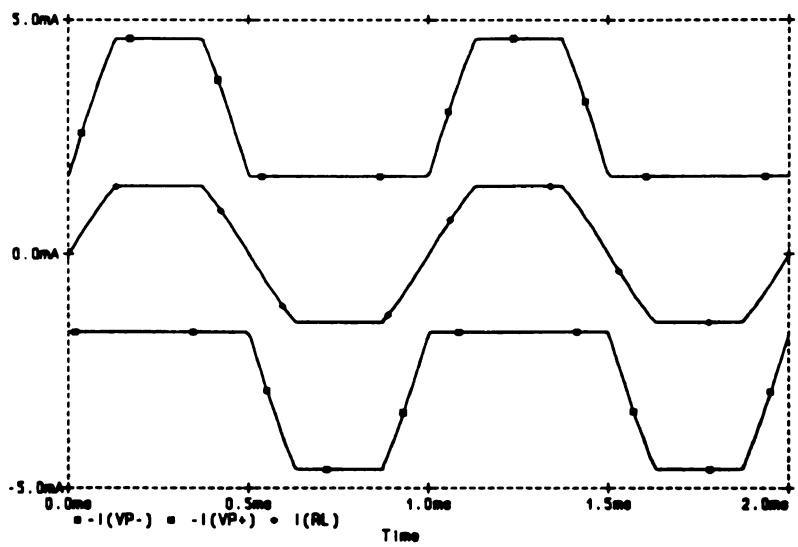

Figure 4.2b The supply current of the modified macromodel

4.2.2 LTC model

The following tests are performed on the LF355. The supply current test response of the LF355 full device looks the same as the μA741 full device. Also, for the

macromodel the load current is still not modeled as flowing from the power supplies. This problem can be fixed in the same way. Fig. 4.3 shows the supply current test response of the improved LF355 macromodel where the load current is modeled correctly.

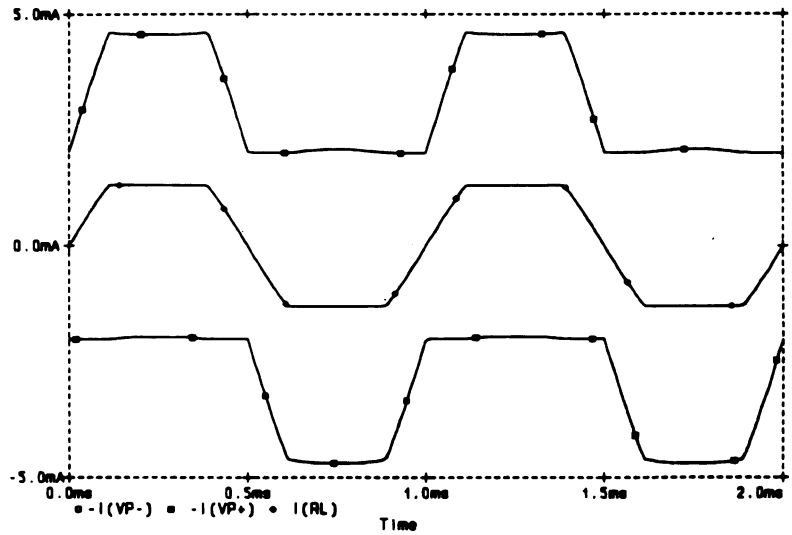

Figure 4.3 Supply current of the modified LF355 macromodel

4.3 The effect of E_{GND} in the microsim model

The EGND is added in the microsim model to average the power supplies, but in [8] it was shown that this VCVS has no effect on improving the macromodel behavior in case of asymmetric supplies. However the input offset of the macromodel depends on E_{GND}, thus in the case of asymmetric supplies this input offset voltage becomes large. Therefore as was suggested in [8], it is better to remove this VCVS, E_{GND}, to eliminate further error.

4.4 Power Supply Rejection Ratio (PSRR)

The power supply rejection ratio SPICE test circuit is shown in Fig. 4.4. The test consist of sweeping the dc input voltage for different values of positive and negative power supplies. The PSRR is the ratio of the change in the voltage input offset over the change in the power supplies

$$PSRR=\frac{\Delta v_{io}}{\Delta v_{p}}$$

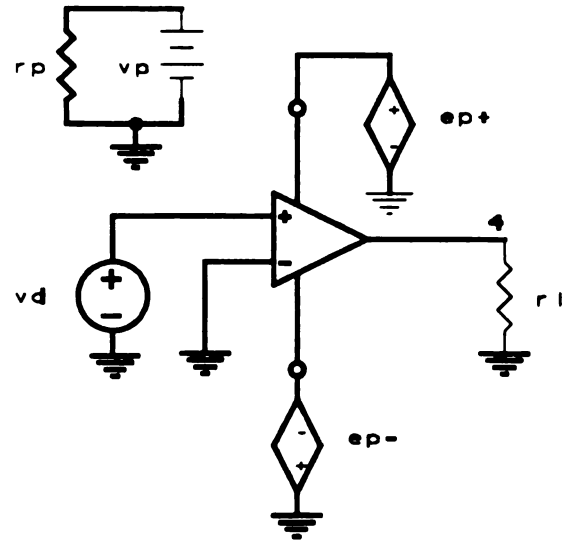

Figure 4.4 PSRR test circuit

4.4.1 Microsim model

Fig. 4.4a shows the SPICE response of the μA741 full device, where the input offset varies as the power supplies changes. Fig. 4.4b shows the SPICE response of the

μA741 macromodel. The input offset remains the same as the power supplies vary. So, the microsim model does not model the PSRR.

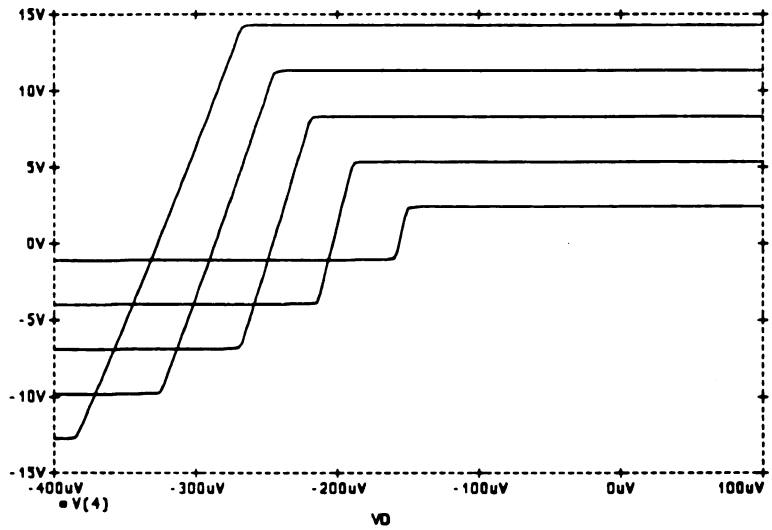

Figure 4.4a PSRR of the μA741 full device

The PSRR problem can be fixed by adding two controlled voltage sources at the input stage of the macromodel. These two controlled sources are described by a look-up tables. One table is for the positive power supply case and the other one is for the negative power supply. Each table consists of pairs of values. The first value in each pair is the value of the power supply and the second is the corresponding additional input offset voltage. The table's input values must be in order from lowest to highest.

For the positive power supply case the table's values are found by using the following formula

$$y=PSRR(v_{p+}-15)$$

where y is the additional input offset voltage added to the positive input for the corresponding value of v_{p+}. The PSRR is about -7.104 μV/V for $v_{p+} \leq 6$ V and is about

-6.85 μV/V for $v_{p+} \geq 6$ V. Table 4.1 includes the values used in the look-up table for the case of the positive power supply. For the negative power supply, the following formula is used to find the additional input offset voltage, y, added to the negative input

$$y=PSRR(|v_{p-}|-15)$$

where PSRR is about -7.85 μV/V for $|v_{p-}| \leq 6$ V and is about -6.66 μV/V for $|v_{p-}| \geq 6$ V. Table 4.1 also includes the values used in the table look-up for the case of the negative power supply.

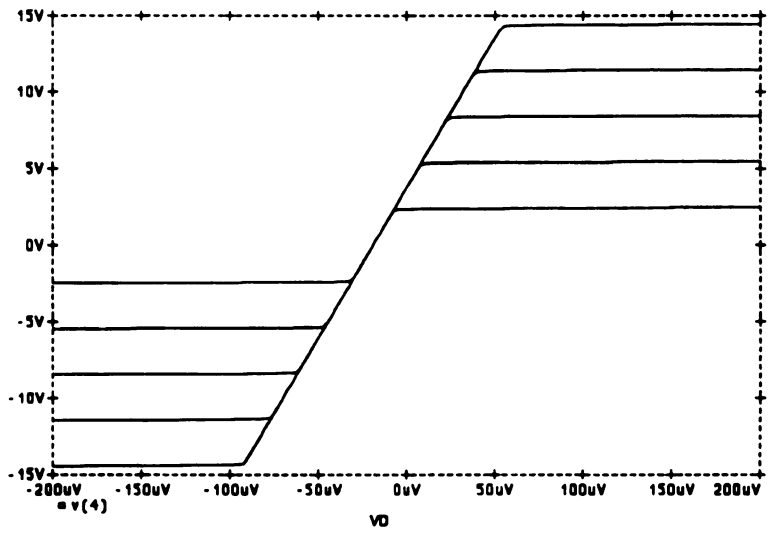

Figure 4.4b PSRR of the μA741 macromodel

The PSRR test SPICE response of the modified microsim model is shown in Fig. 4.4c where now the PSRR is modeled correctly.

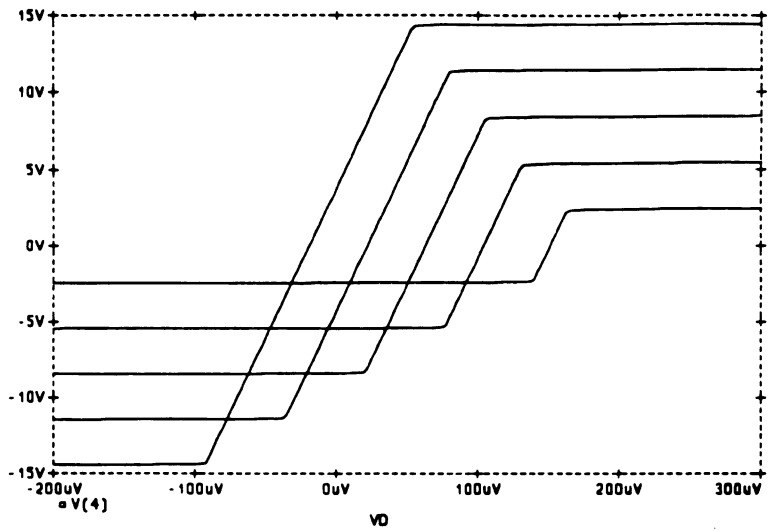

Figure 4.4c PSRR of the modified μA741 macromodel

Table 4.1 Values of the additional offset (μA741)

vp- (V)	vp+ (V)	y (μV)
-3	3	85.25
-6	6	61.7
-15	15	0
-20	20	-34.27

4.4.2 LTC model

The LTC model does not also model the PSRR. Fig. 4.5a shows the SPICE response of the LF355 full device to the PSRR test circuit. Then Fig. 4.5b shows the SPICE response of the modified LF355 macromodel where the same method used for the μA741 now is used for the LF355. Table 4.2 includes the values of the additional

input offset voltage for both negative and positive power supplies.

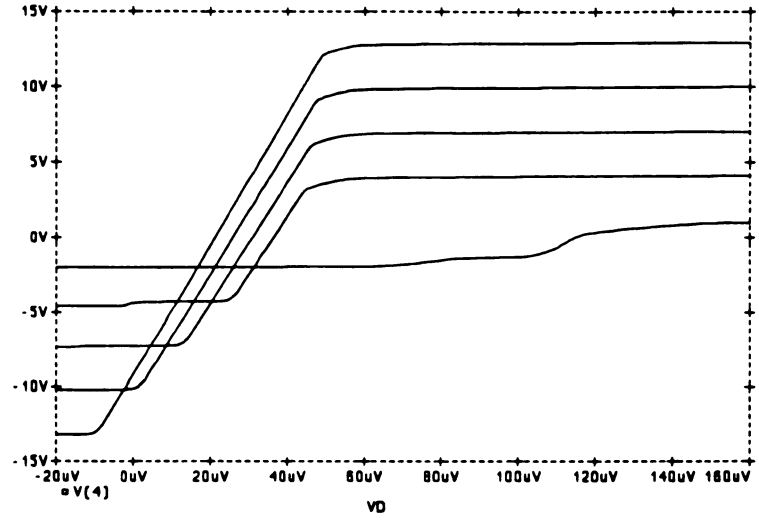

Figure 4.5a PSRR of the LF355 full device

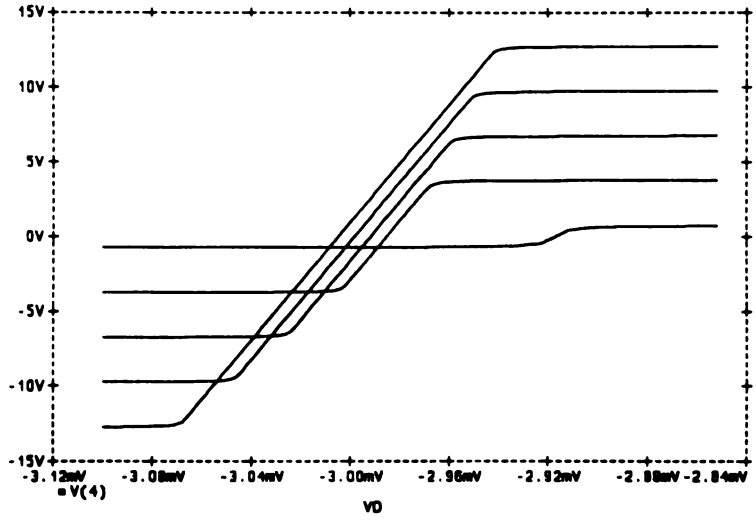

Figure 4.5b PSRR of the modified LF355 macromodel

Table 4.2 Values of the additional offset (LF355)

vp- (V)	vp+ (V)	y (μV)
-3	3	46.61
-6	6	9.745
-15	15	0
-20	20	-5.414

4.5 Clipping Voltage

For some op amps the clipping voltage changes linearly as the positive power supply changes even around the 0 V such as the LF355. But some other op amps like the μA741, the clipping voltage changes linearly as the positive power supply except at the value of 0 V for the positive power supply (see Fig. 4.6a). For both macromodels (LTC and microsim), the clipping voltage changes linearly even around the 0 V power supply because of the voltage source used at the output stage usually noted as v_c. The nonlinearity of the clipping voltage around the 0 V power supply such as the μA741 can be easily solved by introducing a controlled voltage source instead of vc [8]. This controlled voltage source is described by a look-up table which consists of pair of values. The first value in the pair is the value of the power supply and the second is the corresponding value of the controlled voltage source at the output. The values used in the look-up table are determined by using equation 2.40 and are included in Table 4.3. Fig. 4.6b shows the modified macromodel response where the clipping voltage does not change linearly around 0 V.

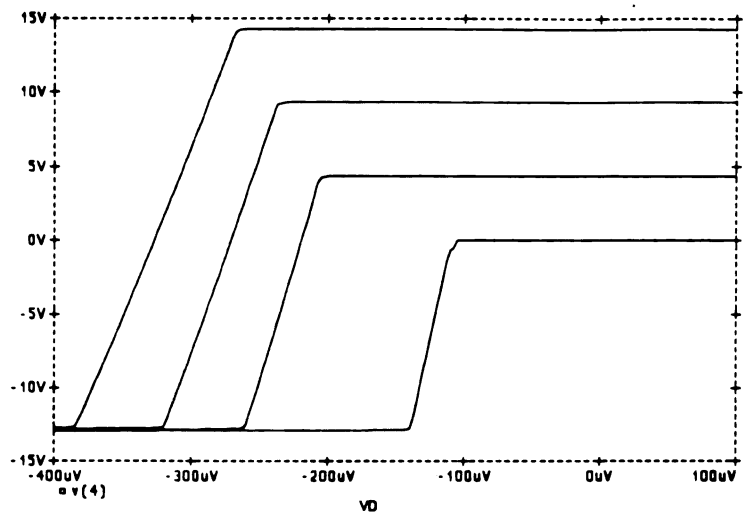

Figure 4.6a Clipping voltage of the μA741 full device

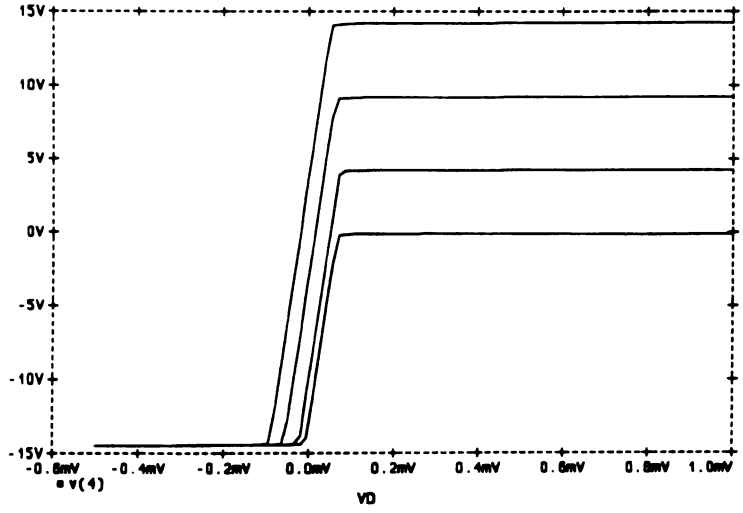

Figure 4.6b Clipping voltage of the modified macromodel (μA741)

Table 4.3 Values of the clipping voltage (μA741)

V_{p+}	V_c
0 V	0.6128 V
5 V	1.253 V
20 V	1.253 V

4.6 Common Mode Rejection Ratio (CMRR)

Since the CMRR is the ratio of the differential mode gain and the common mode gain, then the CMRR SPICE test circuit could be done in two steps: differential mode gain test and a common mode gain test. These two tests were already described previously in Fig. 2.5a and 2.7a.

4.6.1 Microsim model

The microsim model fails to model correctly the common mode gain even for a range of frequency lower than 10 MHz, while it succeeds to mimic the differentail mode behavior of the full device up to 10 MHz. Thus, the CMRR versus frequency is not modeled correctly even for a range of frequency less than 10 MHz. So, the CMRR is improved by improving the common mode gain. The common mode SPICE response of the full device μA741 (see Fig. 2.7b) shows that a pole occurs at a frequency less than 10 Hz, a zero occurs at approximately 10 KHz and another one at 100 KHz. While the

macromodel SPICE response (Fig. 2.7b) shows that only a pole occurs at $f_0 = 5$ Hz. In order to fix the common mode response, a circuit of two zeros needs to be added to the common mode response, one at 10 KHz and the other one at 100 KHz. These zeros are added by using inductors in series with resistances, where at low frequencies these inductors are short circuits [8]. The additional components needed to add these zeros are shown in Fig. 4.7. The two CCCS are used to feed back the signal into the intermediate stage. At low frequencies c_2 is open and the two inductors added l_{cm1}, l_{cm2} are shorted, therefore A_{cm} is now found to be equal to

$$|A_{cm}| = a_1 g_{cm} r_{o2} r_{cm1} r_{cm2} g_{cm1} g_{cm2}$$

Comparing the above equation to equation 2.21, the low frequency common mode gain is not the same, but by selecting the product $r_{cm1}\ r_{cm2}\ g_{cm1}\ g_{cm2}$ to be equal to one, the above equation becomes the same as equation 2.21.

At higher frequencies, c_2 is not open anymore and the common mode transfer function has the following form

$$\frac{v_{out}}{v_{cm}} = A_{cm} \frac{(1+\frac{s}{z_1})(1+\frac{s}{z_2})}{(1+\frac{s}{p_1})}$$

where z_1, z_2 are the two zeros added to the common mode response, and

$$|z_1| = \frac{r_{cm1}}{l_{cm1}}$$

and

$$|z_2| = \frac{r_{cm2}}{l_{cm2}}$$

p_1 is the existing pole that occurs at f_0 defined by equation 2.14 due to c_2.

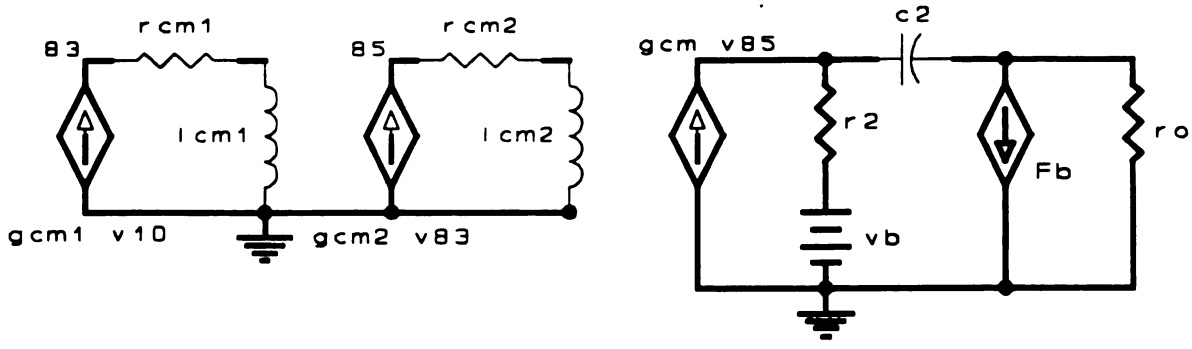

Figure 4.7 Additional components used for CM response

Fig. 4.8a shows the SPICE response of the modified microsim macromodel (μA741) and its full device response. So clearly with these additional components the common mode gain now modeled correctly for frequencies lower than 10 MHz. However for frequencies higher than 10 MHz, the macromodel common mode gain keeps increasing while the full device common mode levels off and then starts to deacrease. In order, to level off the common mode gain at frequencies higher than 10 MHz a resistance, r_x is added in parallel with l_{cm2}. Fig. 4.8b shows the final modified macromodel response where: $g_{cm1} = g_{cm2} = 1E\text{-}2\ \Omega^{-1}$ $r_{cm1} = r_{cm2} = 100\ \Omega$, $l_{cm1} = 1.592$ mH, $l_{cm2} = 0.1592$ mH , $r_x = 1$ KΩ.

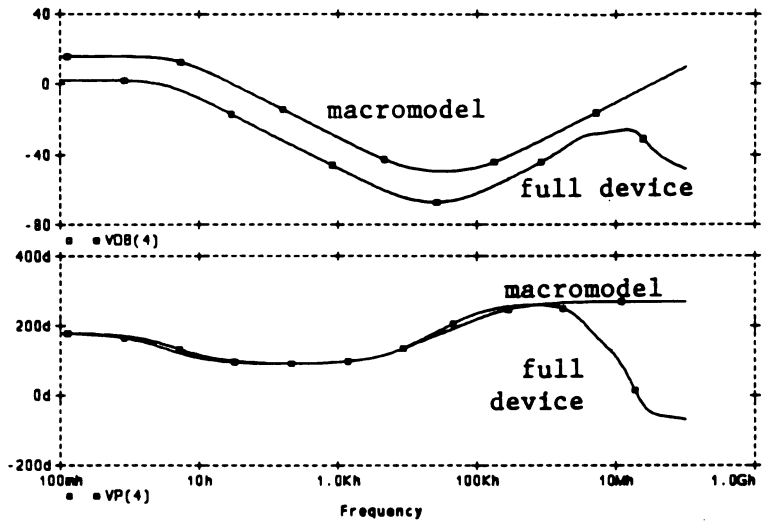

Figure 4.8a CM response of the modified macromodel

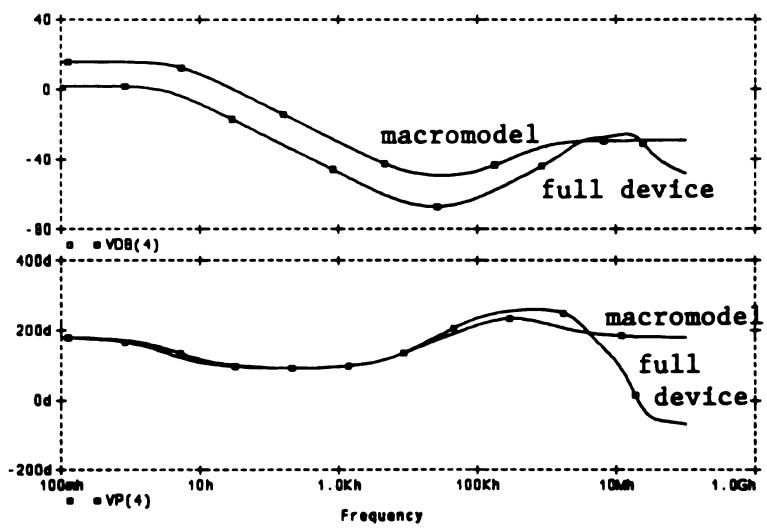

Figure 4.8b A more improved CM response

4.6.2 LTC model

Also the LTC model fails to model correctly the common mode gain for the same range of frequencies as the microsim model, while it succeeds to mimic the differential

mode behavior of the full device. Thus adding the same additional components described in the above section to the LF355, the common mode gain is now modeled correctly except that the phase versus frequency is off by 180° (see Fig. 4.9a). To fix this phenomena we just need to reverse the direction of the current in the CCVS g_{cm} (see Fig. 4.9b).

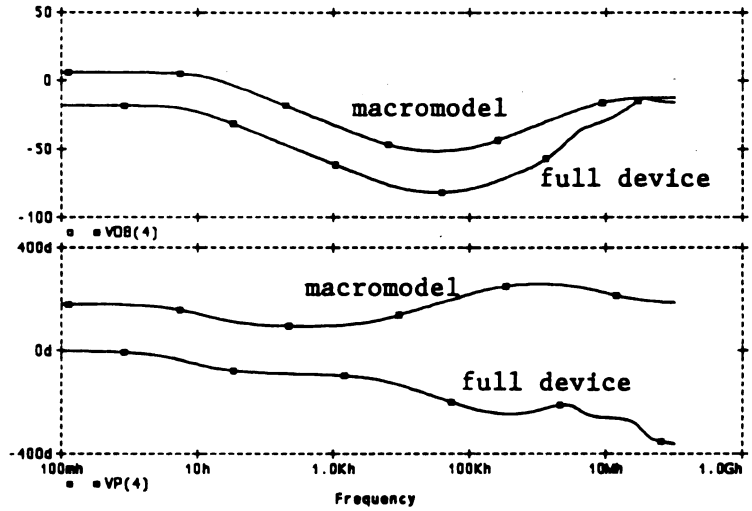

Figure 4.9a CM response of the modified LF355 macromodel

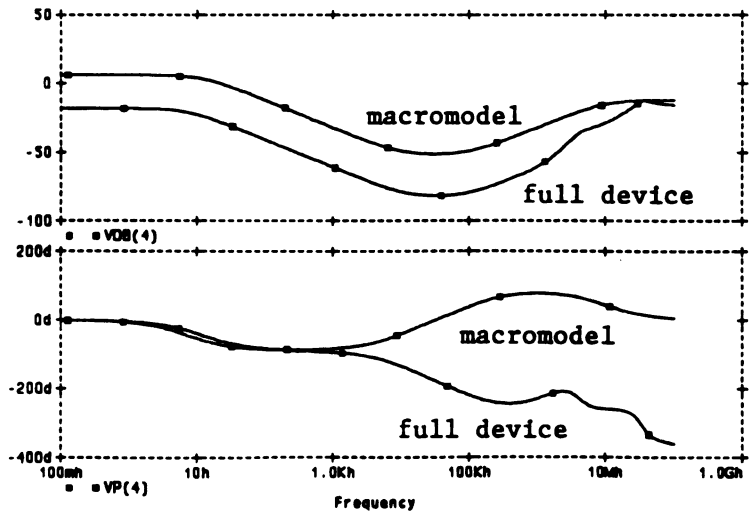

Figure 4.9b More improved CM response

4.7 Numerical example

A numerical example is used to verify that the changes added to the original macromodel do not affect any of the original macromodel formulas. This verification is done by comparing the SPICE simulated measurements of the original μA741 microsim macromodel and the modified μA741 macromodel.

Table 4.4 Parameters of the original and modified μA741 macromodel

Parameter	Original macromodel	Modified macomodel
SR^-	-0.4957 V/μs	-0.4957 V/μs
SR^+	0.5074 V/μs	0.5074 V/μs
v_{io}	-19.17 μV	-19.17 μV
I_B	79.742 nA	79.742 nA
f_0	5.012 Hz	5.012 Hz
A_{dmo}	105.9 dB	105.9 dB
GBP	988.57 KHz	988.57KHz
f_μ	891.3 KHz	891.3 KHz
ϕ_{pm}	63.1°	63.1°
CMRR	90.01 dB	90.01 dB
$r_{o\text{-}ac}$	50.4 Ω	50.1 Ω
$r_{o\text{-}dc}$	151.7 Ω	151.7 Ω
I_{sc+}	40.61 mA	40.61 mA
I_{sc-}	-40.61 mA	-40.61 mA
v_{sat+}	14.61 V	14.36 V
v_{sat-}	-14.61 V	-14.61 V
p_d	50.0 mW	50.4 mW

CHAPTER 5

Conclusion and Future Research

5.1 Conclusion

The design procedures developed in this thesis allows the designer to determine the corresponding op amp characteristics. Also these equations shows how the different components effect the op amp characteristics. Most of the macromodels mimic some of the behaviors of the real device while it fails to mimic some other behaviors. Therefore, the designer has to select the most suitable macromodel that provides a close approximation to the certain response of interest.

5.2 Future Research

Since a large number of macromodels are published without design procedure, one may continue on testing some other macromodels and develop their model formulas. In this way the designer will have more macromodels to choose from. Two macromodels published in [14] and [15] could be an area of future research using the same ideas

presented in this thesis.

1.) One of these macromodel is called the advanced linear devices (ALD) in [13]. The ALD op amp macromodel is built based on the microsim model but it has MOSFET input stage. This kind of macromodel is very useful for CMOS IC's since the microsim don't have a MOSFET input stage macromodel in their library.

2.) The other macromodel is called the PMI model (Precision Monolithics Incorporation) in [14]. This model is built trying to improve on the Boyle model so that it operates better versus frequency. This macromodel mimics the behavior of op amps with multiple poles and zeros. Also this model has no ground reference while all the previous macromodels have a ground reference. This is more complex than the other macromodels and thus requires more time for simulation but it has improved accuracy.

APPENDIX

APPENDIX A

List of SPICE files

Table A.1 SPICE file of Fig. 2.3a

```
DC TRANSFER FUNCTION
* MACROMODEL UA741
VD 1 0
VP+ 2 0 15
VP- 3 0 -15
RL 4 0 10K
X1 1 0 2 3 4 UA741
.DC VD -500U 100U 2.5U
.LIB MICROSIM.LIB
.PROBE
.END
DEVICE LEVEL
VD 1 0
VP+ 2 0 15
VP- 3 0 -15
RL 4 0 10K
X1 1 0 2 3 4 UA741A
.DC VD -500U 100U 2.5U
.LIB UA741D.LIB
.PROBE
.END
```

Table A.2 SPICE file of Fig. 2.5a

```
OPEN LOOP GAIN MACROMODEL
VD 1 0 AC 1
VP+ 2 0 15
VP- 3 0 -15
RL 4 0 10K
VIO 1 5 .01923m
X1 5 0 2 3 4 UA741
.AC DEC 30 .1 10MEG
.LIB 741M.LIB
.PROBE
.END
DEVICE LEVEL
VD 1 0 AC 1
VP+ 2 0 15
VP- 3 0 -15
RL 4 0 10K
VIO 1 5 .327m
X1 5 0 2 3 4 UA741A
.AC DEC 30 .1 10MEG
.LIB  UA741D.LIB
.PROBE
.END
```

Table A.3 SPICE file of Fig. 2.6a

```
OUTPUT IMPEDANCE
* MACROMODEL
VP+ 2 0 15
VP- 3 0 -15
IT 0 4 AC 1
VIO 0 5 19.17U
X1 5 0 2 3 4 UA741
.AC DEC 30 .1 1MEG
.LIB 741M.LIB
.PROBE
.END
DEVICE LEVEL
VP+ 2 0 15
VP- 3 0 -15
IT 0 4 AC 1
VIO 0 5 327U
X1 5 0 2 3 4 UA741A
.AC DEC 30 .1 1MEG
.LIB UA741D.LIB
.PROBE
.END
```

Table A.4 SPICE file of Fig. 2.7a

```
COMMON-MODE GAIN
* MACROMODEL
VCM 1 0 AC 1
VP+ 2 0 15
VP- 3 0 -15
RL 4 0 10K
VIO 1 5 .01923m
X1 5 1 2 3 4 UA741
.AC DEC 30 .1 100MEG
.LIB 741M.LIB
.PROBE
.END
DEVICE LEVEL
VCM 1 0 AC 1
VP+ 2 0 15
VP- 3 0 -15
RL 4 0 10K
VIO 1 5 .327m
X1 5 1 2 3 4 UA741A
.AC DEC 30 .1 100MEG
.LIB UA741D.LIB
.PROBE
.END
```

Table A.5 SPICE file of Fig. 2.8a

```
SHORT CIRCUIT CURRENT
* MACROMODEL
VIN 1 0 SIN (0 .01 1K)
VP+ 2 0 15
VP- 3 0 -15
RL 4 0 10k
X1 1 0 2 3 4 UA741
.TRAN 10U 2m 0 10U
.LIB 741M.LIB
.PROBE
.END
```

Table A.6 SPICE file of Fig. 2.9a

```
SLEW RATE MACROMODEL
VIN 1 0 PULSE (-5 5 10U .5U .5U
+ 45U)
VP+ 2 0 15
VP- 3 0 -15
RL 4 0 10K
X1 1 4 2 3 4 UA741
.TRAN .5U 100U 0U .5U
.LIB 741M.LIB
.PROBE
.END
DEVICE LEVEL
VIN 1 0 PULSE (-5 5 10U .5U .5U
+ 45U)
VP+ 2 0 15
VP- 3 0 -15
RL 4 0 10K
X1 1 4 2 3 4 UA741A
.TRAN .5U 100U 0U .5U
.LIB UA741D.LIB
.PROBE
.END
```

Table A.7 SPICE file of Fig. 2.14

```
CURRENT IN FB AND VB
VIN 1 0 SIN(0 1 5K)
VP+ 2 0 15
VP- 3 0 -15
RL 4 0 10K
X1 1 4 2 3 4 UA741
.TRAN 5U 400U 0U 5U
.LIB 741M.LIB
.PROBE
.END
```

Table A.8 SPICE file of Fig. 2.19

```
OUTPUT VOLTAGE CLAMP
VCM 1 0 SIN(0 2 1K)
VP+ 2 0 15
VP- 3 0 -15
RL 4 0 10k
R1 5 0 1K
R2 5 4 9K
X1 1 5 2 3 4 UA741
.TRAN 10U 2m 0 10U
.LIB 741m.LIB
.PROBE
.END
```

Table A.9 SPICE file of Fig. 2.22

```
SLEW RATE MACROMODEL LF411
VIN 1 0 PULSE (-5 5 10U .5U .5U
+ 35U)
VP+ 2 0 15
VP- 3 0 -15
RL 4 0 10K
X1 1 4 2 3 4 LF411
.TRAN .5U 70U 0U .5U
.LIB LF411.LIB
.PROBE
.END
```

Table A.10 SPICE file of Fig. 3.3 & 3.4

```
SLEW RATE MACROMODEL LF355
VIN 1 0 PULSE (-5 5 10U .5U .5U
+ 35U)
VP+ 2 0 15
VP- 3 0 -15
RL 4 0 10K
X1 1 4 2 3 4 LF355
.TRAN 5U 70U 0U 5U UIC
.LIB LF355.LIB
.PROBE
.END
```

Table A.11 SPICE file of Fig. 3.7

```
SCHORT CIRCUIT CURRENT
* MACROMODEL LF355
VIN 1 0 SIN (0 10 5K)
VP+ 2 0 15
VP- 3 0 -15
RL 4 0 1
X1 1 4 2 3 4 LF355
.TRAN 100U .4m 0 100U
.LIB LF355.LIB
.PROBE
.END
```

Table A.12 SPICE file of Fig. 4.1a

```
NONINVERTING AMPLIFIER
* DEVICE LEVEL UA741
VIN 1 0 SIN (0 2 1K)
VP+ 2 0 15
VP- 3 0 -15
RL 4 0 10K
R2 5 4 9K
R1 5 0 1K
X1 1 5 2 3 4 UA741A
.TRAN 10U 2M 0 10U
.LIB UA741D.LIB
.PROBE
.END
```

Table A.13 SPICE file of Fig. 4.1b

```
MACROMODEL UA741
VIN 1 0 SIN (0 2 1K)
VP+ 2 0 15
VP- 3 0 -15
RL 4 0 10K
R2 5 4 9K
R1 5 0 1K
X1 1 5 2 3 4 UA741
.TRAN 10U 2M 0 10U
.LIB 741M.LIB
.PROBE
.END
```

Table A.14 SPICE file of Fig. 4.2b

```
NONINVERTING AMPLIFIER
* MODIFIED MACROMODEL UA741
VIN 1 0 SIN (0 2 1K)
VP+ 2 0 15
VP- 3 0 -15
RL 4 0 10K
R2 5 4 9K
R1 5 0 1K
X1 1 5 2 3 4 UA741
.TRAN 10U 2M 0 10U
.LIB MICROSIM.LIB
.PROBE
.END
```

Table A.15 SPICE file of Fig. 4.4a

```
DC PSRR DEVICE LEVEL UA741
VD 1 0
EP+ 2 0 6 0 1
EP- 0 3 6 0 1
VP 6 0
RP 6 0 1K
RL 4 0 10K
X1 1 0 2 3 4 UA741A
.DC VD -400U 100U 2.5U VP 3 15 3
.LIB UA741D.LIB
.PROBE
.END
```

Table A.16 SPICE file of Fig. 4.4b

```
DC PSRR OF UA741 MACROMODEL
VD 1 0
EP+ 2 0 6 0 1
EP- 0 3 6 0 1
VP 6 0
RP 6 0 1K
RL 4 0 10K
X1 1 0 2 3 4 UA741A
.DC VD -200U 200U 2U VP 3 15 3
.LIB 741M.LIB
.PROBE
.END
```

Table A.17 SPICE file of Fig. 4.4c

```
DC PSRR OF MODIFIED UA741
* MACROMODEL
VD 1 0
EP+ 2 0 6 0 1
EP- 0 3 6 0 1
VP 6 0
RP 6 0 1K
RL 4 0 10K
X1 1 0 2 3 4 UA741A
.DC VD -200U 200U 2U VP 3 15 3
.LIB MICROSIM.LIB
.PROBE
.END
```

Table A.18 SPICE file of Fig. 4.6a

```
CLIPPING VOLTAGE DEVICE LEVEL
VD 1 0
VP+ 2 0
VP- 3 0  -15
RL 4 0 10K
X1 1 0 2 3 4 UA741A
.DC VD -400U 100U 2.5U VP+ 0 15 5
.LIB UA741D.LIB
.PROBE
.END
```

Table A.19 SPICE file of Fig. 4.6b

```
CLIPPING VOLTAGE OF THE
* MODIFIED MACROMODEL UA741
VD 1 0
VP+ 2 0
VP- 3 0  -15
RL 4 0 10K
X1 1 0 2 3 4 UA741A
.DC VD -0.4m 1m 5U VP+ 0 15 5
.LIB UA741D.LIB
.PROBE
.END
```

Table A.20 SPICE file of the modified microsim macromodel

```
*CONNECTIONS: + -  VP+ VP- VOUT
.SUBCKT UA741 301  302  3    4    5
C1 11 12  8.661E-12
C2 6 7 30.00E-12
DC 5 53 DX
DE 54 5 DX
DLP 90 91 DX
DLN 92 90 DX
DP 4 3 DX
EVP+ 301 1 TABLE {V(3)} =
+ (3,85.25E-6) (6,61.7E-6) (15,0)
+ (20,-34.27E-6)
EVP- 2 302 TABLE {-V(4)} =
+ (3,85.25E-6) (6,61.7E-6) (15,0)
+ (20,-34.27E-6)
FB 7 0 POLY(5) VB VC VE VLP VLN
+ 0 10.61E6 -10E6 10E6 10E6 -10E6
GA 6 0 11 12 188.5E-6
IEE 10 4 DC 15.16E-6
HLIM 90 0 VLIM 1K
Q1 11 2 13 QX
Q2 12 1 14 QX
R2 6 9 100.0E3
RC1 3 11 5.305E3
RC2 3 12 5.305E3
RE1 13 10 1.836E3
RE2 14 10 1.836E3
REE 10 0 13.19E6
RO1 8 201  50
RO2 7 0 100
*CMRR FIX
GCM  0 6 85 0 5.961E-9
GCM1 0 83 10 0 1e-2
RCM1 83 84 100
LCM1 84 0 1.592mH
GCM2 0 85 83 0  1e-2
RCM2 85 86 100
LCM2 86 0 .1592mH
Rx 86 0 1000
* IVP FIX
VIOUT 201 5 0
D5 3 207 DX
R5 207 0 1MEG
F5 207 0 VIOUT 1
D6 204 4 DX
R6 204  0 1MEG
F6 204 0 VIOUT 1
RP 3 4 18.16E3
VB 9 0 DC 0
*
* CLIPPING FIX
*
EVC 3 530 TABLE {V(3)} = (0,0.6128)
+ (5, 1.253) (20,1.253)
*
VC 530 53 DC 0
VE 54 4 DC 1
VLIM 7 8 DC 0
VLP 91 0 DC 40
VLN 0 92 DC 40
.MODEL DX D(IS=800.0E-18 RS=1)
.MODEL QX NPN(IS=800.0E-18
+ BF=93.75)
.ENDS
```

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