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ABSTRACT

Design and Test of Current-mode Signal Processing Circuits

By

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The shrinking feature sizes of devices and their increasing density make it necessary that a reduced supply of 3.3V and lower operating voltages be used in order to enhance performance and reliability. The effects of this reduction are especially impressive for battery-operated systems, as this reduces power drain, which extends battery life and allows for smaller and lighter portable equipment. As pressures increase on VLSI designers to use lower power, voltage-mode techniques will deteriorate in performance due to reduced dynamic range and operating speeds. Analog design has historically been viewed as a voltage-dominated form of signal processing and, all too often, the electronics engineer will think in voltage terms rather than current simply because of the unavailability of current-mode signal processing circuits. Current-mode circuits, circuits in which signals are processed mainly in the current domain, will become increasingly important and attractive as they improve dynamic range and operating speed and have simpler circuitry and lower power consumption. In this study, these inherent advantages of current-mode techniques are applied to the design of data-acquisition and conversion circuits.

To decrease costs and increase performance of electronic circuits, it has become increasingly necessary to integrate both analog and digital circuits on-chip, thus making the

fabrication process very complicated. Current-mode circuits generally do not require high precision resistors or capacitors and can be designed almost exclusively with transistors making them fully compatible with most standard digital CMOS processes. Matched currents are typically generated using current mirrors which depend on good component device matching. Although the use of laser-trimming technology may result in good component device matching, the fabrication process is costly. This work develops and analyzes current-mode signal processing circuits in MOS technology that achieve their functionality without the need for well-matched components.

In real-time applications, it is important to achieve validation of the data generated from data-acquisition and conversion elements. Even though analog MOS circuits are becoming increasingly sophisticated in terms of checking and correcting themselves, the techniques used may not be appropriate when a fatal fault occurs during real-time operation. It would be preferable for the circuits to be designed such that they will indicate malfunction during normal operation and will not produce an erroneous result without an error indication. This dissertation implements time redundancy techniques in analog circuit design for reliability enhancement. In addition, current-mode Built-In Self-Test (BIST) structures are developed to increase the number of test points in a circuit, while still keeping low pin overhead.

Sensor arrays, in which signal processing is integrated with the sensor, are being employed in many applications. The requirement on speed of the data-acquisition and conversion circuits in such implementations is not very high, but the reduction of the size and power consumption is the most important. Thus, the developed current-mode signal processing circuits and diagnosable design methodologies are well suited for the design of reliable integrated sensor arrays.

To my parents

Alamelu and Kalyana Krishnan

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Chapter 1

Introduction

The present trend in digital integrated circuits (ICs) towards submicron technologies with 3.3 V power supplies is increasing. The shrinking feature sizes of devices and their increasing density makes it necessary to have reduced supply and operating voltages to help enhance their performance and reliability [1]. The widespread use of MOS technology, with its unique ability to accurately store and transfer voltages or charge packets, led to the development of analog IC techniques in which voltage was used as the signal. These techniques, though quite successful in many applications, have deteriorated in performance due to reductions in the available supply voltage and the move to ever smaller geometries [2]. Thus, there is difficulty in designing high-linearity, wide-dynamic-range and high-speed voltage-mode analog circuits.

Analog circuit design has historically been viewed as a voltage-dominated form of signal processing. This has been apparent in analog IC design where generally current signals are readily transferred into the voltage domain before any analog signal processing takes place. All too often, transistors are assembled into voltage-oriented circuits and systems, and this form of processing is assumed to be most appropriate for the task, although BJTs and FETS are both current-output devices. The electronics engineer will think in voltage terms rather than current simply because of the unavailability of current-mode signal processing circuits such as data-acquisition and data-conversion systems [3].

Sample-and-hold circuits (S/H), analog-to-digital (A/D) converters and digital-to-analog (D/A) converters form an integral part of real-time systems. Validation of the data

generated from these elements for real-time applications is very important. Analog MOS circuits are becoming increasingly sophisticated in terms of checking and correcting themselves [4]. They use self-correcting, self-compensating, or self-calibrating techniques to eliminate errors traditionally associated with analog circuits such as offset, low frequency noise, and non-linearities [5,6,7]. However, these techniques may not be appropriate when a fatal fault occurs during real-time operation. It would be preferable for the circuits to be designed such that they will indicate malfunction during normal operation and will not produce an erroneous result without an error indication.

This study addresses the potential of current-mode circuits for signal processing, and presents their applications and reliability issues for real-time systems.

1.1 Potential of Current-mode Signal Processing Circuits

A current-mode circuit may be taken to mean any circuit in which current is used as the active variable in preference to voltage. Current-mode circuits have emerged over the last decade as an important class of analog circuits with properties that enable them to rival their voltage-mode counterparts in a wide range of applications [8]. Recently, a number of novel circuit functions and topologies have been explored on the broader front of current-mode analog circuits, opening up wider areas of interest. Current conveyors and related current-mode circuits such as current converters, amplifiers and current rectifiers are only a few of the circuits that have been successfully constructed using Bipolar, MOS, BiCMOS, GaAs, and optical technologies [8].

There are many advantages to be gained by signal processing embracing current-mode techniques. Due to the nonlinear I-V relationship exhibited by most transistor structures, a small change in input voltage results in a much larger change in the output current [9]. Consequently, for a process with a fixed voltage supply, the usable dynamic range of current-mode signals is significantly larger than that of their voltage-mode counterparts. It has long been recognized that current manipulation is inherently faster than voltage manipulation, since the effects of stray inductances are less severe than those

of stray capacitances [10]. Thus, there is potential for higher operating frequencies in current-mode circuits.

To decrease the costs and increase the performance of electronic circuits, it has become increasingly necessary to integrate both analog and digital circuits on the same IC [11]. The problem is that the most commonly available process, the standard digital CMOS process, does not offer the linear components with which analog design is usually implemented. Until recently the only solution to this problem was to develop more complicated processes that can provide such linear components. Thus, there is a need for circuitry that is compatible with the standard digital CMOS process. Current-mode signal processing circuits generally do not require high precision resistors or capacitors. When capacitors are used to store the signal, they need not display good ratio matching or good linearity. Consequently, these circuits can be designed almost exclusively with transistors making them fully compatible with most digital processes. Generally, current-mode circuits do not require amplifiers with high voltage gains thereby reducing the need for high performance amplifiers [12].

When current is used as the active parameter, the need for matched signals implies a need for matched currents [13]. Matched currents are generally generated using current mirrors which depend on good component device matching. Although the use of laser-trimming technology may result in good component device matching, the fabrication process is costly. Therefore, it is necessary to develop current-mode circuits which achieve their functionality without the need of well-matched components.

The continued growth of mixed analog/digital VLSI systems will ensure the need for small size, high speed analog-to-digital and digital-to-analog converters fabricated using commonly available digital processes. Mixed signal VLSI design is essential to analog and digital interfacing, and the immunity of current-mode circuits to supply noise is an important property in a mixed-mode environment. Also, in large data-acquisition systems there is a preference for the use of current to represent the measurand as it is fairly interference-resistant [14]. This is because of the low probability that DC currents would be induced in data-transmission lines.

The complexity of current-mode circuits is generally less than their voltage-mode counterparts for the same function, as currents may be manipulated to yield more effective and efficient circuit realizations. They have also been found to be a cheaper alternative to voltage-mode circuits for many applications. Another significant advantage rests in the immunity of current signals to deleterious influences such as ground and power supply noise, debiasing, and signal line impedance [15]. These technological reasons form the basis of many commonly used current-mode circuits.

One of the important applications of current-mode signal processing circuits is in the design of integrated sensors. Integrated sensors have the inherent advantages of small size, light weight, high performance, low cost, and high reliability. They provide a better signal-to-noise ratio, improved sensitivity, and a digital output which is less prone to noise. Smart sensor arrays improve overall system performance by changing the system architecture to take advantage of signal processing that is integrated with the sensor [16]. A sensor array chip must include *data-acquisition and conversion circuits* as well as an *array of sensing elements*, as shown in the block diagram of Figure 1.1. Each sensing element may include a signal conditioning circuit and/or a simple analog signal processor. When a scan has been completed, each cell in the array will be holding the raw sensing data as either voltages or currents which are read out and converted by either a high-speed current-mode A/D converter, or an array of medium-speed converters. The requirement on speed of the acquisition and conversion circuits is not very high in many such implementations, but the reduction of the size and power consumption is of utmost importance [17].

This dissertation develops a current-mode shift register that can be wound through the array and simultaneously load the data which can then be serially read out to be converted. This dissertation also presents the design of current-mode A/D converter arrays in which each subconverter does not rely on high gain amplifiers or well-matched components to achieve high resolution. Incorporating parallel signal processors into an IC sensor array will increase the overall computation rate significantly.

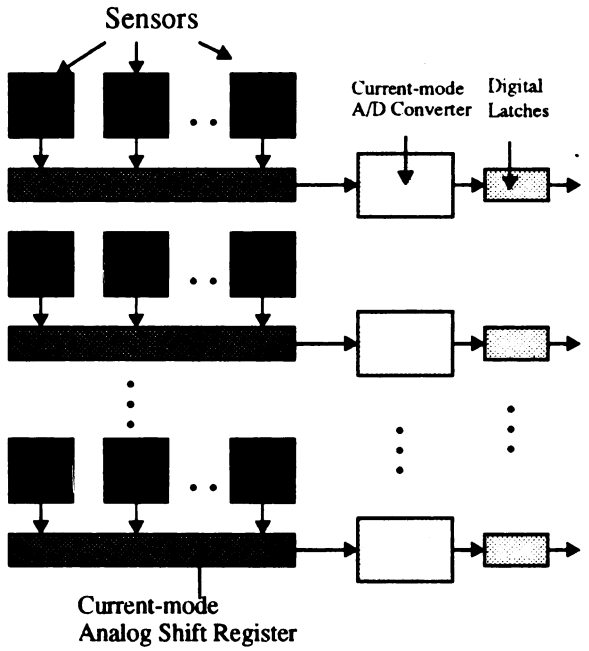


Figure 1.1 A Sensor Array Implementation

One of the primary motivations of this work, therefore, is to apply the inherent advantages of current-mode techniques to the design of data-acquisition and conversion circuits. The goal of this dissertation is to develop, analyze and construct these current-mode signal processing circuits in MOS technology and to explore the limits of their applications.

1.2 Importance of Reliability

For real-time applications, in general, the validation of data from A/D converters is accomplished by using an extra D/A converter and an analog window comparator [18], as shown in Figure 1.2, where a high-resolution and high-accuracy D/A converter is needed and the comparison is performed in an analog manner. Therefore, the validation must highly depend upon the reliability of both the D/A converter and the window comparator. Although their reliability may be improved by using sophisticated testing schemes to weed out faulty components [19], such off-line or static tests cannot identify the transient faults that occur during on-line operation. Therefore, it is obvious that a mechanism for *concurrent error detection* (CED) [20-22] must be installed to detect such faults before they cause undesirable results.

One of the objectives of this dissertation is to implement time-redundancy techniques in analog circuit design for reliability enhancement of real-time systems. In this study, an alternative current-mode A/D converter with CED capability is presented in which the Alternating Logic technique [22] is implemented. The fault model considered here is the single stuck-at fault at the switching elements. The A/D converter is capable of detecting all transient faults and most permanent faults.

For more than two decades, the subjects of automatic testing and fault diagnosis of electronic circuits have been of interest to researchers in the area of circuits and systems [23-28]. Recently, with rapidly increasing complexity and size of modern electronic systems, these subjects have become more important and critical. Due to the difficulty of current measurement in an analog circuit, most of the fault diagnosis algorithms have been

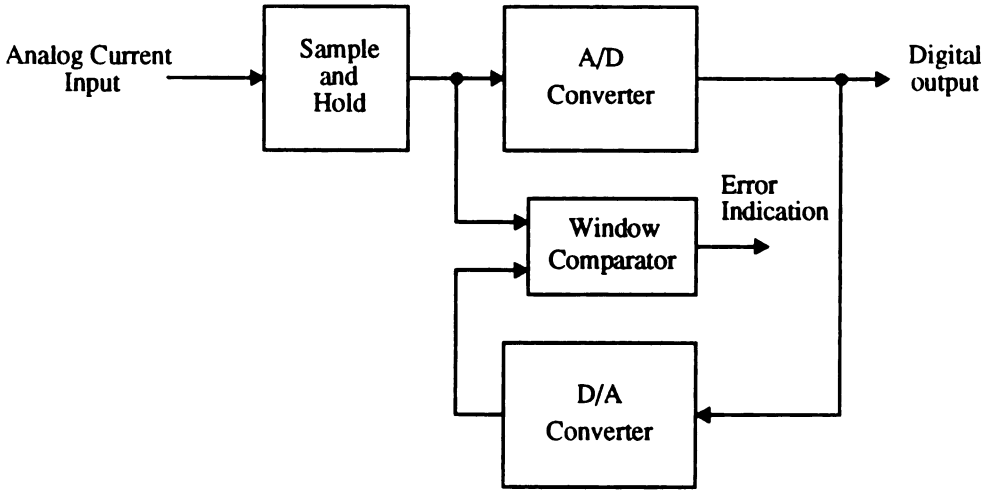


Figure 1.2 Testing of the A/D Converter

developed requiring only node voltage measurement [23-26]. However, it has been shown that the use of both current and voltage measurement can simplify the diagnosis process significantly [27,28]. This dissertation presents alternative Built-In Self-Test (BIST) structures in order to allow the voltage and current test data measured at various test points to be shifted out for fault diagnosis.

1.3 Dissertation Organization

This dissertation is organized as follows. Chapter 2 presents background knowledge of data-acquisition and conversion circuits in general and existing current-mode signal processing methods specifically. The concepts of reliability and fault testing applied in diagnosable design are also touched upon.

Chapter 3 describes in detail several basic elements developed, followed by descriptions of data-acquisition and conversion systems in which they are used. A bipolar current copier that forms a sample-and-hold building block is first presented. A current-mode shift register used as a data-acquisition system is also discussed. An accurate current-mode divider circuit which does not rely on well-matched components is later described. A successive-approximation A/D converter that can be adapted into a parallel array structure with a common reference unit is finally illustrated. Several design issues are addressed, and simulation results give a thorough understanding of the functioning and performance of these current-mode signal processing circuits.

Chapter 4 describes the incorporation of reliability into these circuits and presents the diagnosable current-mode circuit design methodology. Finally, Chapter 5 summarizes this dissertation and contributions of this study as well as future research topics.

Chapter 2

Background

This chapter briefly reviews the background knowledge of data-acquisition and conversion circuits in general and existing current-mode signal processing methods. In addition, the concepts of reliability and testability are also discussed.

2.1 Data-acquisition and Conversion Techniques

Sample-and-hold circuits are the essential elements in data-acquisition systems and contribute significantly to their performance. Analog-to-digital (A/D) and Digital-to-analog (D/A) converters are the primary components of data-conversion, and they have been implemented using several techniques. The operation principles and characteristics of different sample-and-hold elements and A/D converters are described in this section.

2.1.1 Sample-and-hold (S/H) Circuits

A sample-and-hold (S/H) circuit is an essential building block of sampled data systems and its operation and properties are described in this section. The function of a S/H circuit in its simplest configuration is to take samples from an input signal during the sample mode and then to hold the last value of the input signal for a certain time interval, called the hold mode [29]. An elementary S/H circuit is shown in Figure 2.1. The switch

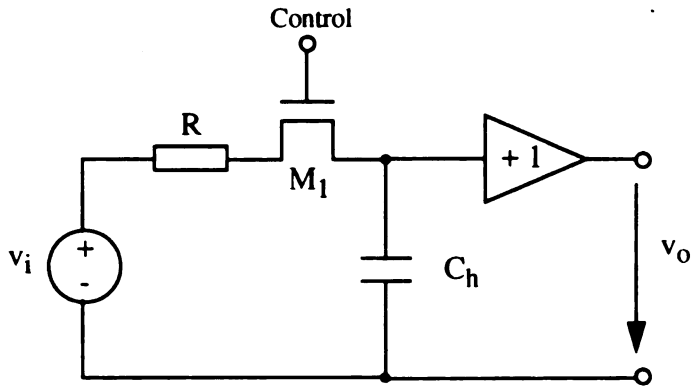


Figure 2.1 A Sample-and-hold Circuit

M_1 is implemented by a single or complementary MOS transistor. During the sample mode the input voltage source $v_i(t)$, which has an internal resistance R, is connected to the hold capacitor C_h via the MOS switch M_1. The capacitor voltage follows (tracks) the input voltage assuming that the time constant RC_h is small enough. When the 'hold' mode is selected and the switch is opened, the capacitor voltage remains fixed at the input signal level. To avoid the discharging of the hold capacitor C_h by an output circuit, a buffer amplifier (voltage follower) is usually used. If necessary, a second voltage follower is used at the input of the S/H stage to avoid loading the input signal source.

In the ideal S/H circuit, tracking is error-free; i.e. the capacitor is immediately charged and the change from the sampling to the hold mode and vice-versa occurs instantaneously. However, there are several factors that determine the performance of practical S/H elements. For example, in the switched capacitor implementation of the elementary S/H circuit, noise and unbalanced charge injection are the major sources of error of the sampled voltage.

The most important S/H circuit parameters are defined as follows [29]:

(1) Acquisition Time: The time required after receipt of the sample command for the hold capacitor to charge to a specified voltage change and remain within a specified error band.

(2) Slew-Rate: The maximum rate of change of the output voltage after receipt of the sample command and for a voltage step applied to the input.

(3) Aperture Uncertainty Time: The time variation or jitter in the opening of the sampling switch.

(4) Hold-Mode Droop Rate: The output voltage change per unit of time during the hold mode.

(5) Offset: The extent to which the output deviates from zero for zero input.

(6) Feedthrough Offset: The step error occurring at the initiation of the hold mode caused by the clock voltage feedthrough through the gate-source or gate-drain overlap capacitances and the unbalanced channel charge stored in the MOS switch.

2.1.2 Analog-to-Digital (A/D) Converters

A/D converters are used to transform continuous-time or discrete-time analog signals (typically voltages) to digital data which can then be easily processed, stored, and/ or transmitted digitally. An A/D converter connected between some analog sensors and a digital computer, must be able to accept the outputs from these sensors as its inputs. It should provide its digital outputs to the computer and its complete operation and performance must be tailored to that of the overall system. For example, there is no need for a converter to have 12-bit accuracy if the signals from the sensor are accurate only to 8-bits.

When the input signals to the converter change as a function of time, which is most often the case, it is important to consider all the factors that determine the dynamic behavior of a converter [29]. A/D conversion is ideally considered to take place instantly but in real converters this process takes a finite amount of time for completion during which the output cannot be updated. The dynamic parameters of the converter primarily characterize the speed of converter operation. The most important of these parameters are conversion time, conversion rate (often called throughput rate) and aperture effects (delay, jitter). Conversion time is the amount of time required for an A/D converter to perform one complete conversion under the least favorable conditions. Alternatively, to determine the conversion speed one uses the conversion rate (throughput rate) defined as the maximal number of repetitive analog-to-digital conversions per second. It is calculated as the reciprocal of the total time required for one successful conversion.

Depending upon the structure and the principle of operation, A/D converters can be divided into several different categories such as parallel (direct), serial (or sequential), and serial/parallel. Based on the speed of conversion, A/D converters can be divided into three groups: high-speed, medium-speed, and slow-speed [29]. This categorization is based on the conversion time which is 50nsec for a high-speed converter while the medium-speed and low-speed types convert at 50μsec and 100msec, respectively.

High-Speed A/D Converters

High-speed A/D converters find application in the encoding of composite video signals. Parallel or flash converters are the fastest and largest of this group. Both pipelined and time-interleaved array converters offer a fast conversion rate and a smaller circuit.

In a *parallel or flash A/D converter*, the reference is divided into 2^N nominally equal segments, thus generating all possible signal quantization levels. It employs the most straightforward approach to achieve high-speed analog-to-digital conversion by performing 2^{N-1} simultaneous voltage comparisons with the 2^{N-1} equally spaced reference sources, where N is the number of bits. If the input signal is higher than the quantization level under consideration, an output bit of 1 is generated; otherwise an output bit of 0 is produced. This digital code is then converted to the desired binary code by an encoder circuit. The main advantage of flash A/D converters is their high conversion rate. However the exponential increase in the number of comparators as a function of resolution limits the practicality of such converters.

In *time interleaved array A/D converters*, n identical N-bit A/D converters with S/H stages are connected in n parallel channels as shown in Figure 2.2. In each channel, the input signal is sampled and held and then converted at a rate of 1/nT. By staggering the S/H stages in time such that the sampling in the second channel is T seconds behind that in the first channel and so on, the input signal can be sampled and held each T seconds by a different A/D converter in the structure. Hence, the overall system achieves a conversion rate n times higher than that of the building A/D subconverter. A buffer and a digital multiplexer stage is used at the output to service the conversion channels one at a time. For high-speed input signals very stable and regular sampling intervals are required. Even a small, deviation from the nominal sampling frequency of 1/nT may cause considerable error since it leads to overlapping the input signals. A high-speed analog demultiplexer can be used to relax the sampling accuracy requirement by converting the analog input signal into n lower-speed sampled and held data signals which are fed into the appropriate sample-and-hold stage.

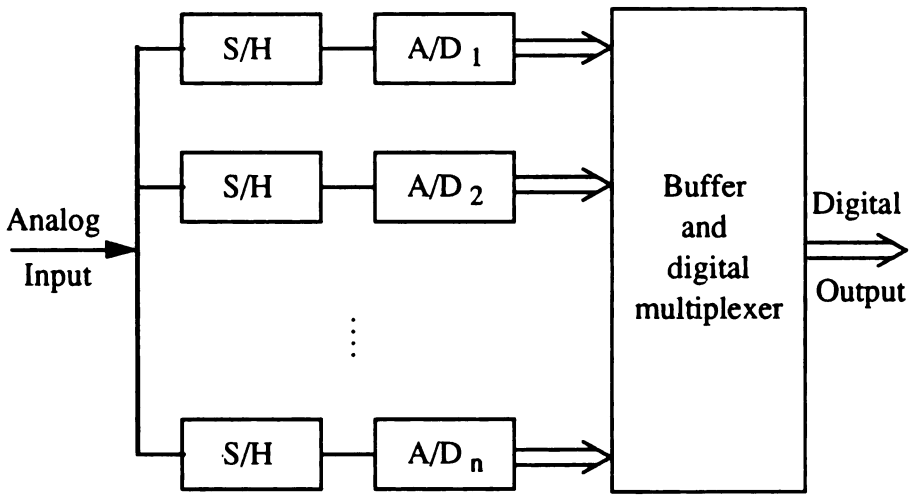


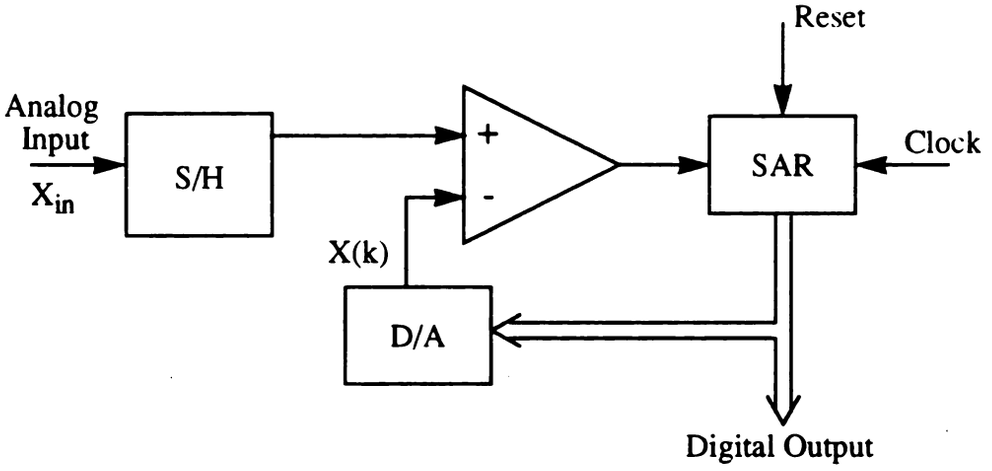
Figure 2.2 Block Diagram of a Time Interleaved A/D Converter

The *pipelined A/D converter* architecture is such that the pipe consists of m basic stages, each stage consisting of a S/H circuit and a low-resolution low-speed A/D converter. The input signal flows sequentially through successive stages, so the converter produces an N-bit digital word over several sampling periods rather than one period. The main idea of a pipelined A/D converter is to insert S/H structures between the subconverter stages in order to operate all the stages concurrently thus achieving a high conversion rate which is almost independent of the number of stages. The principal disadvantage of pipelining is the requirement of high-speed and high-precision S/H structures.

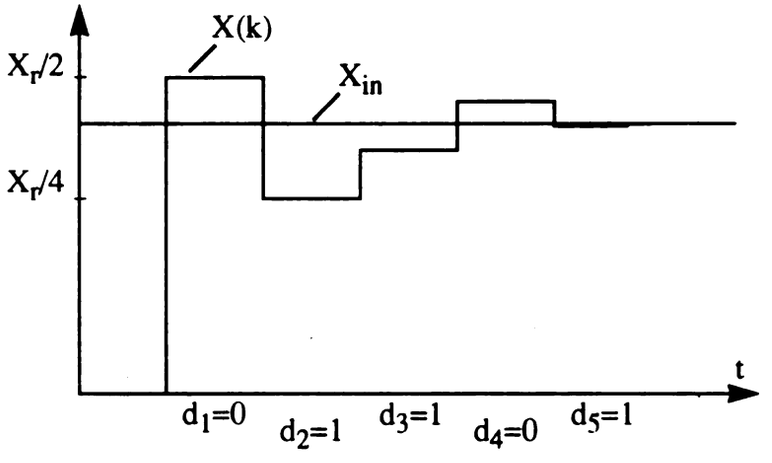
Medium-Speed A/D Converters

This class of A/D converters commonly employ successive-approximation and cyclic or algorithmic conversion techniques. Both techniques offer a relatively good speed-size performance.

Successive-approximation A/D converters require the use of a S/H stage, a signal comparator, a D/A converter and a successive-approximation register (SAR) as shown in Figure 2.3 (a). The input S/H stage is used to hold the analog input signal constant during the conversion process. The converter operates on the following principle: after the reset in the first conversion step, the SAR sets the D/A output to $X_r/2$. Hence, the most significant bit or MSB, d_1, is assumed to be one whereas all other bits are set to zero. If the input is higher than $X_r/2$, the MSB is left at one; otherwise, it is reset to zero. In the next step, the D/A converter output is set to $X_r/2 \pm X_r/4$ where the plus sign is taken if $d_1 = 1$ and the minus sign if $d_1 = 0$. This signal is again compared with the input and the second most significant bit is determined depending on the result of comparison as seen in Figure 2.3(b). In the following step, the output of the D/A is to be incremented or decremented by $X_r/8$ and a third comparison is performed leading to d_3. The process continues until all bits of the output word have been determined. Such a converter requires only N clock cycles to complete an N-bit conversion. Mathematically, the algorithm which describes the operation of the successive-approximation A/D can be represented as follows:



(a)



(b)

Figure 2.3 Successive- Approximation A/D Converter :
(a) Block Diagram; and (b) Voltage Waveform

$$X(k) = X(k-1) - \frac{(-1)^{a_{k-1}}}{2^k} X_r \qquad (2.1)$$

with $d_k = 1$ if $X_{in} > X(k)$ and $d_k = 0$ otherwise

for $k = 1, 2, ...,$N where $X(0) = X_r$.

A bipolar A/D conversion can be achieved by introducing a sign bit d_0 to select either $+X_r$ or $-X_r$.

The *cyclic or algorithmic A/D converter* involves the basic operations of comparison, subtraction and multiplication by two. Conversion is based on holding the reference signal constant and multiplying the signal to be converted by two during each conversion cycle. Conversion begins with sampling the input signal, X_{in}, doubling it, then comparing it with X_r in order to generate the MSB d_1. If $2X_{in} \geq X_r$ then d_1 is set to 1, X_r is subtracted from $2X_{in}$ and the difference is multiplied by two. Otherwise, d_1 is set to 0 and X_{in} is multiplied by two. This procedure continues according to the algorithm described by the next set of equations until the desired resolution is achieved.

$$X(k) = 2X(k-1) + (-1)^{a_{k-1}} X_r \qquad (2.2)$$

with $d_k = 1$ if $X(k) \geq 0$ and $d_k = 0$ otherwise

for $k = 1, 2, ...,$N where $X(0) = X_{in}$, $d_0 = 1$.

Low-Speed A/D Converters

High resolution converters can be obtained using one of the described conversion techniques at the expense of costly fabrication technology and/or complicated circuitry. Two alternative techniques achieve high resolution without these burdens but their conversion speed is negatively affected.

The *integrating type A/D converter* operates with a conversion cycle consisting of two separate integration intervals. In the first interval the analog input signal is integrated up for a fixed and known period of time. In the second interval the negative reference signal is integrated down until the output voltage of the integrator returns to zero. This time period

is then proportional to the input signal. At the start of conversion, the integrator and the counter are both zeroed to guarantee stable timing. The important feature of this result is that the digital output is independent of the integration time constant and of the clock frequency since these parameters affect both the first and the second interval in the same ratio.

In *oversampling A/D converters*, the input signal is sampled at a rate much higher than the Nyquist rate, then converted to a digital stream in an interpolative modulator. The quantized approximation of the input signal is subtracted from it and the difference is integrated. The integrator in the loop tends to minimize the average difference of the sampled analog input and the quantized approximation. The output of the estimator goes to a digital-low-pass filter which averages and decimates this coarse estimate to get a finer approximation at a lower sampling rate.

2.2 Current-mode Circuits

This section reviews some traditional concepts of current-mode circuits. Current-mode signal processing circuits using dynamic techniques and challenges in their design are also described.

2.2.1 Current Mirrors

The current mirror is a very useful and familiar building block in CMOS analog circuit design. Current mirrors use the principle of matched devices such that if the gate-to-source potential of two identical MOSFETS are equal, their currents are equal [30]. Figure 2.4 shows the implementation of a simple n-channel current mirror. The current i_I is assumed to be defined by a current source or some other means and i_O is the output or "mirrored" current. M_1 is in saturation because $V_{DS1}=V_{GS1}$. In the most general case, the ratio of i_O to i_I, is then

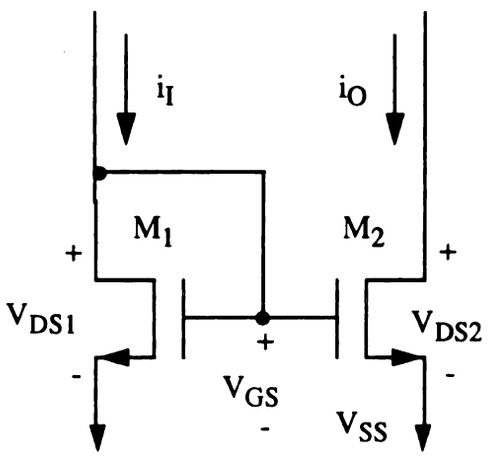


Figure 2.4 A Simple N-Channel Current Mirror

$$\frac{i_O}{i_I} = \left(\frac{L_1 W_2}{W_1 L_2}\right)\left(\frac{V_{GS} - V_{T2}}{V_{GS} - V_{T1}}\right)^2 \left(\frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}\right)\left(\frac{\mu_{o2} C_{ox2}}{\mu_{o1} C_{ox1}}\right) \tag{2.3}$$

where $(W/L)_i$ are the aspect ratios, V_{Ti} is the threshold voltage of the MOSFETs. Normally, the components of a current mirror are processed on the same integrated circuit and thus all of the physical parameters such as V_T, μ_O, C_{ox}, etc., are identical for both devices. As a result, (2.3) simplifies to

$$\frac{i_O}{i_I} = \left(\frac{L_1 W_2}{W_1 L_2}\right)\left(\frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}\right) \tag{2.4}$$

If $V_{DS2} = V_{DS1}$ (not always a good assumption) then the ratio of i_O/i_I becomes

$$\frac{i_O}{i_I} = \left(\frac{L_1 W_2}{W_1 L_2}\right) \tag{2.5}$$

Consequently, i_O/i_I is a function of the aspect ratios that are under the control of the designer. However, there are three main factors that cause the current mirror to be different than the ideal situation of (2.5). These factors are: (1) channel-length modulation, (2) threshold offset between the two transistors, and (3) imperfect geometrical matching.

Consider the channel-length modulation effect. Assuming all other aspects of the transistor are ideal and the aspect ratios of the two transistors are both unity, then (2.4) simplifies to

$$\frac{i_O}{i_I} = \left(\frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}\right) \tag{2.6}$$

with the assumption that the modulation parameter λ is the same for both transistors. This equation shows that differences in drain-source voltages of the two transistors can cause a deviation for the ideal unity current gain or current mirroring.

Consider two transistors in a mirror configuration where both have the same drain-source voltage and all other aspects of the transistors are identical except V_T. In this case, (2.3) simplifies to

$$\frac{i_O}{i_I} = \left(\frac{V_{GS} - V_{T2}}{V_{GS} - V_{T1}}\right)^2 \tag{2.7}$$

It is also possible that the transconductance gain K' of the current mirror is also mismatched. Assume that the W/L ratios of the two mirror devices are exactly equal but that K' and V_T may be mismatched. (2.3) is then written as

$$\frac{i_O}{i_I} = \frac{K'_2 (V_{GS} - V_{T2})^2}{K'_1 (V_{GS} - V_{T1})^2} \tag{2.8}$$

The third nonideal effect of current mirrors is the error in the aspect ratio of the two devices. These are due to mask, photolithographic, etch, and out-diffusion variations. These variations can be different even for two transistors placed side by side. One way to avoid the effects of these variations is to make the dimensions of the transistors much larger than the typical variation one might see. For transistors of identical size with W and L large in value, the errors due to geometrical mismatch will generally be insignificant compared to offset-voltage and V_{DS} induced errors.

In most current mirror realizations, ideal mirroring is true only for a range of voltages, and there is a minimum voltage, V_{MIN}, below which the realization will not be a good approximation of the input current. This is because the MOS transistor in the nonsaturation region is not a good current source. Even in the region where it is a good approximation, it deviates due to the resistance r_{out} which is ideally infinite. Thus, the small signal output resistance of a current mirror is important in determining its performance. Therefore, V_{MIN} and r_{out} are the two major aspects by which these mirrors can be characterized.

The advantage of this current mirror is its simple structure. Higher performance current mirrors will attempt to increase the value of r_{out} and reduce V_{MIN} further. Several

improvements such as bootstrapped structures or cascode structures have also been implemented. Table 2.1 summarizes the performance of the different types of MOS current mirrors having unity gain from the viewpoint of accuracy (linearity), output resistance, and V_{MIN} [31]. Additional considerations include the size of devices where ratio accuracy will be obtained for larger size devices.

Table 2.1 Comparison of Current Mirror Structures

MOS Current Mirror	Accuracy ($i_O = i_I$)	r_{out}	V_{MIN}
Simple	Poor	$r_o=1/(\lambda i_O)$	$V_{DS}(sat)$
Cascode	Good	$g_m r_o^2$	$2V_{DS}(sat)$
Wilson	Good	$g_m r_o^2/2$	$V_{GS} + V_{DS}(sat)$
Regulated Cascode	Good	$g_m^2 r_o^3$	$V_{DS}(sat)$

2.2.2 Current Copiers

The *current mirror* uses the principle that if the gate-source potential of two identical MOS transistors are equal, the channel currents should be equal. However, the most important limits of conventional current mirror techniques with respect to their use in high-precision analog circuits are the current errors due to mismatch and the low-frequency 1/f flicker noise. Both of these can be reduced by increasing the gate area WL and the saturation voltage V_{Dsat}, but this classical approach cannot eliminate flicker noise or reduce the error much below 1% [1].

Unlike bipolar transistors, MOSFETs do not need any gate current to control their drain current. This property has been recently used to build current copiers or dynamic current mirrors that do not require well-matched components [32-34]. The analog storage capability is exploited to sequentially use the same transistor for copying and read-out. Thus, the very notion of mismatch disappears since there is only one transistor. These

current copiers make practically identical copies of a given current without the need for accurately matched componentsand are implemented as sampled-current circuits [1].

Figure 2.5(a) shows a simple current copier that consists of switches, a non-critical enhancement-mode MOS transistor, and a non-critical capacitor. I_{in} is copied into the current storage cell by turning on the switches SW, ST and SQ, the capacitor will charge up to the gate voltage needed by the transistor to achieve a drain current equal to I_{in}. The switches SW and SQ are then turned off to disconnect the cell from the current source; thereafter, the cell is capable of sinking a current I_{in} when connected to a load. Note that the input current to the NMOS copier cell must be positive. Figure 2.5(b) illustrates a simple PMOS copier which memorizes negative input current.

Many current-mode circuits that utilize dynamic techniques are constructed using current copiers. The error effects of the current copiers will also affect these current-mode circuits. Inevitable circuit non-idealities will cause the current retrieved from a cell to differ from its original copied current. Some of the mechanisms of original-to-copy error include clock feedthrough, leakage and channel length modulation [33,34].

The first important limitation to the precision of the above scheme is *charge injection or switch charge feedthrough.* The various switches are realized by means of transistors. To close the switch, the switching transistor is made conductive by mobile carriers that are attracted into the channel by the gate voltage. When the switch is opened, these carriers are released from the channel in order to block the transistor, and most of them flow to the source or to the drain [32]. Thus, when the switch opens, a fraction Δq of q flows onto the capacitor C_1, which causes an error $\Delta V = \frac{\Delta q}{C_1}$ in the stored voltage. This voltage error in turn creates a relative error in the output current equal to $\frac{\Delta I}{I_o} = \frac{g_m \Delta V}{I_o}$.

An estimate of the magnitude of this effect for the basic cell of Figure 2.5(a) can be derived as follows. Assume a single n-channel transistor acting as switch SQ. If half of the charge Q_{SQ} on the switch inversion layer is dumped onto C_1, then

$$\Delta V = \frac{1}{2}\left(\frac{Q_{SQ}}{C_1}\right) = \frac{1}{2}\left(\frac{(WL)_{SQ} C'_{ox} (V_{GS} - V_T)_{SQ}}{C_1}\right) \qquad (2.9)$$

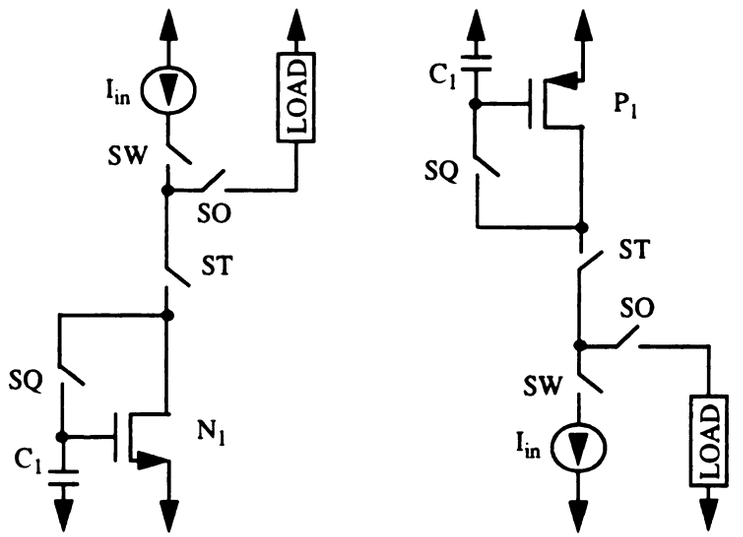


Figure 2.5 Simple Current Copier: (a) NMOS Copier; and (b) PMOS Copier

where the assumption that the switch is operated in the linear region and N_1 in the saturation region is taken. W_{SQ} and L_{SQ} represent the width and length of switch SQ. C_{ox} is the gate oxide capacitance per unit area $(V_{GS}-V_T)_{SQ}$ is the 'on voltage' of the switch and μ, W_{N1} and L_{N1} represent the electron mobility, width and length of N_1, respectively. The resulting relative change in the copier current is

$$\frac{\Delta I}{I_o} = \frac{g_m \Delta V}{I_o} = \left(\frac{\mu C_{ox}' \left(\frac{W}{L}\right)_{N1}}{2I_o}\right)^{\frac{1}{2}} \left(\frac{(WL)_{SQ} C_{ox}' (V_{GS} - V_T)_{SQ}}{C_1}\right) \qquad (2.10)$$

Simple alternations to the basic current copier cell can help reduce some of the errors. The use of CMOS switches may eliminate the error caused by switch charge feedthrough. ΔV can also be decreased by increasing C_1, with one limit given by the area of the capacitor. It can also be decreased by reducing the total charge q in the channel in order to reduce the fraction Δq that flows onto C_1. This can be achieved by minimizing the gate area WL and/or by controlling the gate control voltage of the switch in order to adjust its on-conductance to the minimum required value. External gate capacitors can be used to reduce the effects of the charge injection from switches and to allow the transistor and capacitor geometries to be determined independently.

The various approaches to reduce the effect of charge injection on the precision of the dynamic mirror may be combined. It may be pointed out that most of them tend to increase the time needed to achieve equilibrium in the circuit and therefore decrease the maximum frequency of switching. Since the input current is sampled, the bandwidth of the mirror is in turn reduced. Thus, there exists a trade-off between speed and precision.

Another contribution to the error is due to *channel length modulation* which is represented by the drain-to-source conductance g_{ds}. As shown in Figure 2.5(a), the drain of N_1 is connected to its gate during the storage phase, thus the two nodes are at the same voltage potential. During the read-out phase, the drain potential will be different and be equal to a value imposed by the load of the mirror. This difference in drain voltage during the two phases produces important additional contributions to the inaccuracy of the mirror.

Because of the change in the effective channel length as V_{DS} of N_1 changes, the basic current copying circuit of Figure 2.5(a) will supply a slightly different current during retrieval.

These considerations show that an accurate implementation must include some means to keep the drain voltage of N_1 as constant as possible in spite of the difference. An operational amplifier could be used for this purpose, in which case the circuit becomes an active current copier shown in Figure 2.6. Another solution which is more compact is obtained by adding a common gate transistor in series with the main transistor to build a cascode structure, a technique commonly used in current mirrors.

Junction leakage is another error effect to be considered. Even with the switch SQ turned off, a small current will flow through the reversed biased source-substrate junction, drawing charge from C_1. Over a time interval Δt this leakage current I_{leak} will create a change in voltage $\Delta V = I_{leak}\frac{\Delta t}{C_1}$ across C_1 with a resulting change in current $\Delta I = g_m \Delta V$. However, as is also true for switched capacitor circuits, with usual junction leakage currents and reasonable clock rates, this does not create a severe constraint on circuit operation.

Since both the transconductance element and the switches consist of MOS transistors, the copier inherently contains both *thermal and 1/f internal noise* sources. As with other sampled data circuits, the resulting output noise current can be separated into two types. Sampled noise, occurring during the period when the current is sampled, resulting in an error in the voltage held across the capacitor C_1 and nonsampled or direct noise, occurring when the copier is sinking current from a load.

Junction leakage and noise can be limited by a careful choice of switch dimensions, capacitor sizes, and loop bandwidth. Note that larger capacitors may reduce the effects of the thermal noises and charge injection from the switches, thus increasing the resolution. However, larger capacitors result in slower settling time. This leads to a significant area/ resolution/speed trade-off.

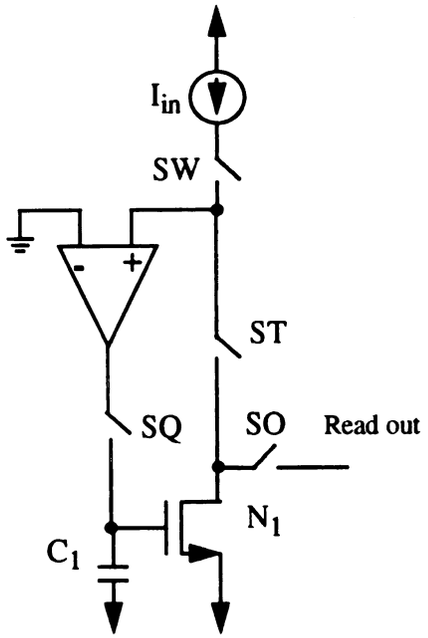


Figure 2.6 Active NMOS Copier

2.2.3 Dynamic Current-mode Signal Processing Circuits

Several circuits that use dynamic current-mode techniques are reviewed in this section. These circuits form an essential part of current-mode data converters and utilize current copiers.

2.2.3.1 Current-mode Multiplier

One obvious application of current copiers is the integer current multiplier where if the input current I_{in} is constant, then an output current equal to an integer multiple of I_{in} can be obtained. Figure 2.7 shows a current-mode multiply-by-two circuit which achieves accurate signal multiplication without the need for well-matched components [9].

Initially, switches S_1, S_2 and S_3 are turned on. After the amplifier has settled, I_1 will equal I_{in}. When switch S_3 is turned off, the gate capacitance will cause transistor N_1 to "memorize" the current level. The procedure is then repeated for transistor N_2 by turning on S_1, S_4 and S_5. Once N_2 has been "programmed", an output current of $2I_{in}$ is produced by turning on S_2, S_4 and S_6 and providing an appropriate V_{out} such that I_{out} is equal to (I_1+I_2) or $2I_{in}$. Ideally, the sum of the outputs of the cells is therefore an integer multiple of I_{in} achieved without relying on element matching.

2.2.3.2 Current-mode Divider

Current dividers are usually implemented by using resistor networks or weighted transistors. The division accuracy of such solutions is limited by device mismatch. An algorithmic method for dividing a given current I_{in} by an integer factor without depending on device matching or even linearity is depicted in Figure 2.8, for the specific case of division by a factor of 2. The circuit does not require laser trimming, external adjustment, or matched components [35].

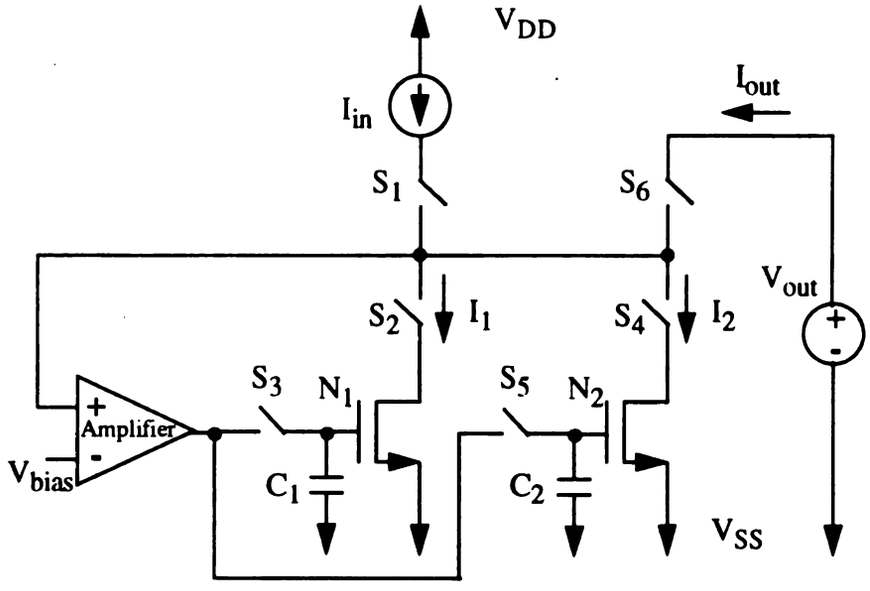


Figure 2.7 Current-mode Multiplier

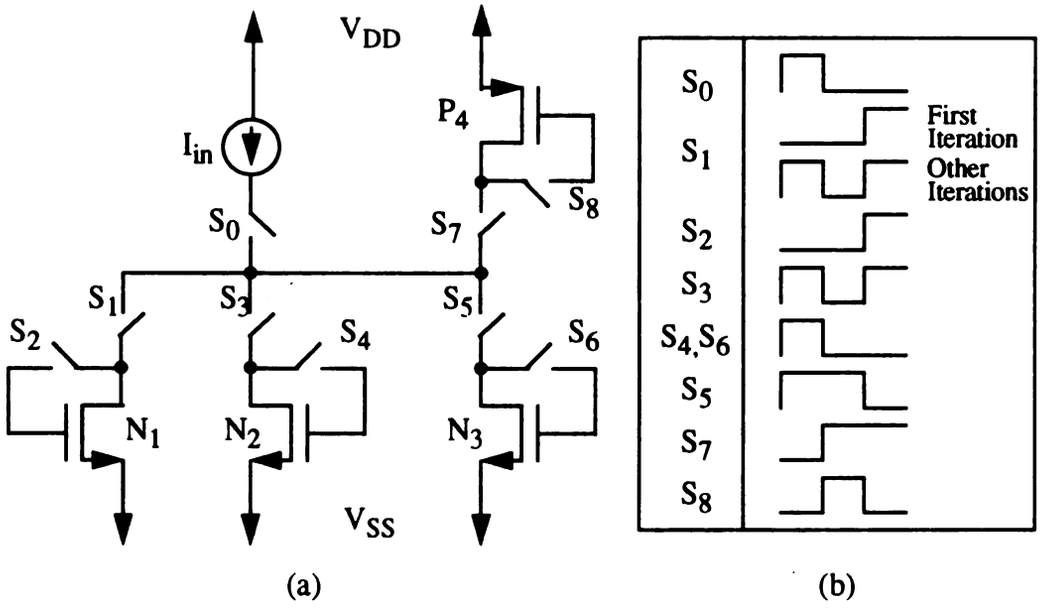


Figure 2.8 A Highly Accurate Current Divider: (a) Schematic Diagram; and (b) Switching Sequence

The basic operation of the current divider is described as follows. (For simplicity of the discussion, I_i, i=1, 2, or 3, is the memorized current in transistor N_i and I_4 is the current held in P_4.) First, the current difference (I_{in}-I_1) is fed to both transistors N_2 and N_3 by turning on switches S_0, S_1, S_3, S_4, S_5, and S_6, and turning off the others. The currents copied into N_2 and N_3 are determined by the mismatch between them. In order to obtain the difference in their currents, N_3 sources its copied current to P_4, during the second cycle, by turning on S_7, S_8, and S_5, and turning off the others. Once the current held in P_4 is set, turning on S_3, S_7, S_1, and S_2, and turning off the others, during the third cycle, will copy the current difference (I_4-I_2) into N_1, i.e., I_1=I_4-I_2. Thus, N_1 holds the current difference between I_2 and I_3. This completes an iteration of the division process and thus each iteration takes three clock cycles. During the next iteration, this current difference is removed from I_{in} and is sourced to N_2 and N_3. Therefore, through subsequent iterations, the error reduces to a minimal value and the current in N_3 converges to $I_{in}/2$. Note that, in order to zero the current remaining in N_1, only the input current I_{in} is copied into N_2 and N_3 during the first iteration. The number of iterations necessary to obtain half of the current with certain accuracy depends on the mismatch in N_2 and N_3. Figure 2.8(b) illustrates the switching sequence of the divider circuit. Let α_2 and α_3 be the mismatch factors of the transistors N_2 and N_3, respectively, then I_2=$\alpha_2 I_{in}$, I_3=$\alpha_3 I_{in}$, where

$$\alpha_2 = \frac{k_2 (V_{GS}-V_{T2})^2}{k_2 (V_{GS}-V_{T2})^2 + k_3 (V_{GS}-V_{T3})^2} \tag{2.11}$$

$$\alpha_3 = \frac{k_3 (V_{GS}-V_{T3})^2}{k_2 (V_{GS}-V_{T2})^2 + k_3 (V_{GS}-V_{T3})^2} \tag{2.12}$$

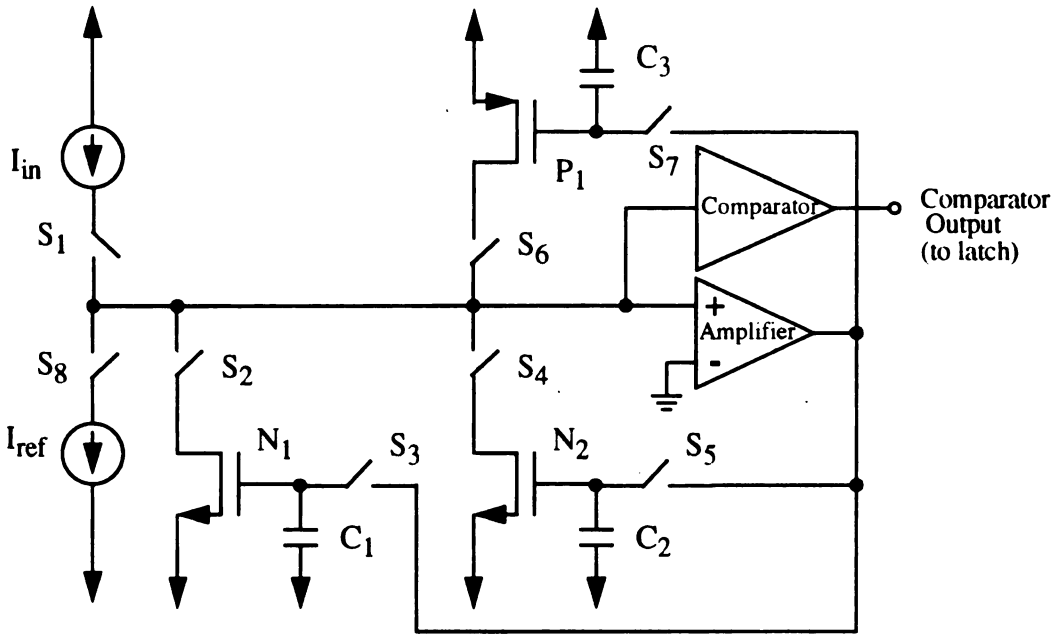
Note that V_{T2} and V_{T3} are the threshold voltages of the transistors N_2 and N_3, respectively, and the device transconductance $k_i = k'_i (\frac{W}{L})_i$ where $(W/L)_i$, i=1 or 2, is the aspect ratio of the transistor N_i. Since the sensitivity of α_2 and α_3 to V_{GS} is small, the values of α_2 and α_3 are considered constant [35].

2.2.3.3 Current-mode A/D Converter

As discussed in (2.2), algorithmic (cyclic) current-mode A/D converters convert an input current to an N-bit digital data word D using a multiply-by-two scheme . The accuracy of these converters is often limited by the mismatching of passive components of the circuits. An algorithmic A/D converter that combines current-mode and dynamic techniques achieves high resolution without the need for high gain amplifiers or well-matched components [13]. The converter, shown in Figure 2.9, starts converting for the most significant bit (MSB) of an input current I_{in} by turning on switches S_1, S_2, and S_3 to cause the current in N_1 to be set to I_{in}. Once N_1 is set, S_2 and S_3 are switched off while S_4 and S_5 are on to set N_2 to be I_{in}. Once the input signal has been stored on N_1 and N_2, twice the input signal is loaded into P_1 by turning off S_1 and S_5 while switching on S_2, S_6, and S_7. After P_1 is set, S_2, S_4, and S_7 are turned off while S_8 is turned on, thus allowing the comparator to sense the current imbalance, and hence, determine if the signal, $2I_{in}$, is greater than I_{ref}. If the signal exceeds the reference, the MSB will be a "1" otherwise it will be a "0." This completes the conversion for the MSB.

2.3 Fault-tolerant and Testable Circuit Design

During the last few years the theory and practice of testing electronic products have changed considerably. The continuing revolution in electronic circuitry in terms of size and speed has increased the problems of testing. The philosophy of testing has evolved from merely measuring electrical parameters at many points in the device under test to integrating testing in every step of the device design and development. A whole field of testing has emerged. The following section presents a brief introduction to some important testing concepts.



(a)

	MSB	previous bit = 1	previous bit = 0
S_1			
S_2			
S_3			
S_4			
S_5			
S_6			
S_7			
S_8			
Latch			
Reset			

(b)

Figure 2.9 Current-mode A/D Converter: (a) Schematic Diagram; and (b) Switching Sequence

2.3.1 Fault Tolerance

There are two fundamentally different approaches that can be taken to increase the reliability of computing systems [36]. The first approach is called *fault prevention* (also known as fault intolerance) and the second *fault tolerance*. In the traditional fault prevention approach the objective is to increase the reliability by *a priori* elimination of all faults. Since this is almost impossible to achieve in practice, the goal of fault prevention is to reduce the probability of system failure to an acceptably low value. Fault tolerance is an attribute that is designed into a system to achieve some design goal. A design must meet many functional and performance goals, it must satisfy numerous other requirements as well. The most prominent of the additional requirements are reliability, availability, safety, performability, dependability, maintainability, and testability. Fault tolerance is one system attribute capable of fulfilling such requirements. Fault tolerance is not a replacement but rather a supplement to the most important principles of reliable system design: (a) use the most reliable components; and (b) keep the system as simple as possible, consistent with achieving the design objectives.

Three fundamental terms in fault-tolerant design are fault, error, and failure [20]. There is a cause-and-effect relationship between faults, errors, and failures. Specifically, faults are the cause of error, and errors are the cause of failures. A fault is a physical defect, imperfection, or flaw that occurs within some hardware or software component. An error is the manifestation of a fault, and it is a deviation from accuracy or correctness. Finally, if the error results in the system performing one of its functions incorrectly, a system failure has occurred. Essentially, a failure or malfunction is the non-performance of some action that is due or expected.

Fault duration specifies the length of time for which a fault is active. A permanent fault remains in existence indefinitely if no corrective action is taken, while a temporary fault occurs for short period of time. Temporary faults have been referred to as "intermittent" or "transient" faults with the same meaning. Transient faults are non-recurring temporary faults. Intermittent faults are recurring faults that reappear on a

regular basis. A major portion of digital system malfunctions are caused by temporary faults. Such faults can occur due to loose connections, partially defective components or poor designs.

In the fault tolerance approach, faults are expected to occur during computation, but their effects are automatically counteracted by incorporating redundancy, i.e. additional facilities, into a system, so that valid computation can continue even in the presence of faults. They are redundant in the sense that they could be omitted from a fault -free system without affecting its operation. Redundancy is achieved simply by the addition of information, resources, or time beyond what is needed for normal system operation [20]. The redundancy can take one of several forms: hardware redundancy, software redundancy, information redundancy and time redundancy. Note that time redundancy uses additional time to perform the functions of a system such that fault detection and often fault tolerance can be achieved.

2.3.2 Testability Techniques

The testing of an integrated circuit is extremely vital to the ultimate goal of achieving high reliability, availability, safety, maintainability, fault tolerance or other design requirements [20]. Integrated systems, even when designed with highly reliable components, do not operate forever without developing some faults. When a system ultimately does develop a fault it has to be detected and located so that its effect can be removed. *Fault detection* means the discovery of something erroneous in a system or circuit. *Fault location* means the identification of the faults with components, functional modules or subsystems, depending on the requirements. *Fault diagnosis* includes both fault detection and fault location.

Fault detection in a logic circuit is carried out by applying a sequence of test inputs and observing the resulting outputs. Therefore, the cost of testing includes the generation of test sequences and their application. The test generation process includes fault modeling, test pattern generation, fault simulation and fault coverage evaluation. The first

step consists of developing a fault dictionary for the circuit, i.e. modeling the faults that are assumed. Next, test vectors and/or test patterns are generated to test for the set of faults being considered. One of the main objectives in testing is to minimize the length of the test sequence. The test patterns are then simulated against the faulted circuit, and the fault coverage is evaluated. If the fault coverage is inadequate, the process of test pattern generation and fault simulation is repeated. To be practical and cost effective for large scale integrated circuits, the test generation process should be automated. A test is a means by which the existence and quality of certain attributes within a system are determined.

The testing process attempts to determine if the *unit under test* (UUT) works and if it possesses its complete capability [20]. There are two key concepts in having a testable design: controllability and observability. Controllability refers to the ability to apply test patterns to the inputs of a sub-circuit via the primary inputs of the circuit. Observability refers to the ability to observe the response of a sub-circuit via the primary outputs of the circuit or at some other output point. In general, the easiest way to increase controllability/ observability is to add some control gates and control terminals (controllability) or to add some output terminals (observability) for testing purposes.

Fault Model

Fault modeling is very important in developing cost effective test strategies for electronic circuits. In general the effect of a fault is represented by means of a model, which represents the change the fault produces in circuit signals. The selection of adequate fault models is crucial to achieving high quality testing because the efficiency of a test scheme is limited by the accuracy of the chosen fault model. If the model fails to capture the important characteristics of the actual fault, the test based on this model will fail to detect the actual fault [36].

The fault models in use today are Stuck-at faults, Bridging faults and Stuck-open faults. The most common model used for logical faults is the "single-stuck-at fault". It assumes that a fault in a logic gate results in one of its inputs or the output being fixed to either a logic 0 (Stuck-at-0) or a logic 1 (stuck-at-1). Stuck-at-0 and stuck-at-1 faults are

often abbreviated to s-a-0 and s-a-1, respectively. The stuck-at fault model, often referred to as the "classical" fault model, offers good representation for the most common types of failures, e.g. short-circuits ("shorts") and open-circuits ("open") in many technologies.

For circuits containing switching elements, the logical stuck-at model is appropriate, effective and simple to work with. This model is based on the assumption that the basic functionality of the circuit is not affected by the fault. This implies that the circuit continues to behave as expected of it given the existence of the fault.

There exist various testing techniques that can be used to achieve this goal. In general testing techniques use two major approaches: *built-in* test and *external* test [20]. External test techniques are typically performed with the UUT removed from its operating environment and various tests applied to it using external equipment. Built-in test techniques usually incorporate testing as part of the design of the device; thus no external testing equipment is needed.

Built-In Test

As digital circuits grow more complex and difficult to test, it becomes increasingly attractive to build some self-testing ability into the circuits under test. Built-in test may be conveniently used to detect and isolate a faulty component in a circuit and thus facilitate its replacement. An important added feature of properly designed built-in test is the ability to simplify off-line testing by taking advantage of the increased controllability and observability made possible by the incorporation of the self-testing capability.

The built-in test strategy can be used to enhance testability of VLSI chips. It is based on the following principles: (1) Test patterns are generated on-chip; (2) Responses to the test patterns are also evaluated on-chip; (3) External operations are required only to initialize the built-in tests and to check the go/no-go tests results from a chip; and (4) Additional pins and silicon area are kept to a minimum.

As the internal complexity of the integrated circuit chip increases, the idea of built-in test becomes more and more attractive as it has many advantages: (1) Test patterns are generated automatically inside chips; (2) Responses to test patterns need not be stored;

and (3) Use of expensive test equipment is not necessary. Built-in techniques can follow either a *concurrent* (on-line) or a *nonconcurrent* (off-line) approach. Nonconcurrent test techniques require that the operation of the UUT be halted before beginning the test. Concurrent test techniques allow a device to be tested while in normal operating mode. The off-line test techniques suffer from the disadvantage of not being able to detect temporary faults, which are likely to be more important in VLSI systems.

Concurrent Error Detection (CED)

Although reliability of circuits may be improved by using sophisticated testing schemes to weed out faulty components, off-line or static tests cannot identify the transient faults that occur during on-line operation. Therefore, a mechanism for concurrent error detection must be installed to detect such faults before they cause undesirable results [22]. All CED schemes detect errors through conflicting results generated from operations on the same operands. CED can be achieved through space or time redundancy, or space/time hybrid redundancy. Time redundancy employs only one single set of hardware to carry out the repeated operations and can be effectively used in the detection and correction or errors caused by temporary faults. Since the same hardware is used, the repeated operation, in the presence of faults, is liable to produce the same erroneous result as that of the first step. To avoid this problem, the operand must be coded in the repeated cycle, and the result thus obtained must be decoded back to the appropriate form for meaningful comparison.

Consider a time redundancy technique shown in Figure 2.10 [21,22]. Let x be the input of the computation unit f, and let $f_p(x)$ and f(x) be the outputs with and without encoding-decoding operations, respectively. Two fundamental requirements must be satisfied in these operations. First, the coding function c must not interfere with the original function f. In other words, for a selected coding function c, there must exist a decoding function c^{-1} such that $f_p(x) = c^{-1}(f(c(x))) = f(x)$ in the absence of faults. This is the concept of *mappable correct output* [37]. Secondly, for the purpose of fault detection, the coding operation c must transform the input operand(s) x in such a way that when subjected to the same faulty conditions, the output in the repeated step, though still erroneous will be

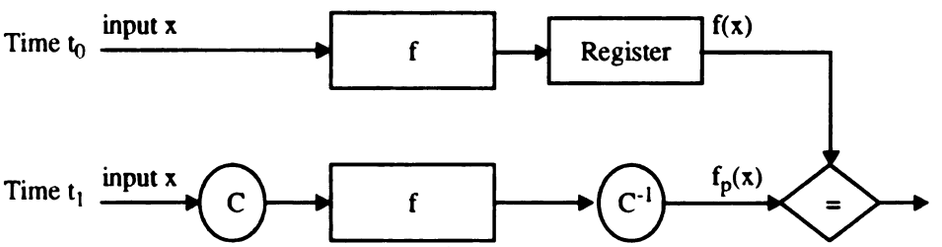


Figure 2.10 The Concept of Time Redundancy

different from the first step. This is the concept of *disjoint error sets*. Two simple time redundancy techniques have been reported: RESO (*REcomputing with Shifted Operands*) [21,37] and AL (*Alternating Logic*) [22,38]. Among existing CED techniques, both RESO and AL have unique features of transient fault detection and require only a moderate increase in hardware. AL implementation uses the complementation operator as the encoding function while RESO uses the arithmetic shift.

The "alternating logic design" technique achieves its fault detection capability by utilizing a redundancy in time based on the successive execution of a required function and its self-dual [22]. A function for which the normal output is the complement of the output, when complemented inputs are applied, is known as a self-dual function, e.g. a function f(x), where $x=(x_1, x_2, ..., x_n)$, is a self-dual if for all x, $f(\bar{x}_1, \bar{x}_2, ..., \overline{x_n}) = \bar{f}(x_1, x_2, ..., x_n)$. Thus, the principal characteristic of alternating logic is that it provides a true output in one time period and the complementary output in the next time period. The main disadvantage of the technique is that it requires twice as much time to obtain the verified output.

Chapter 3

Current-mode Data-acquisition and Data-conversion Circuits

All too often the electronics engineer will think in voltage terms rather than current simply due to the unavailability of current-mode signal processing circuits, thus not taking advantage of the many gains of current-mode techniques [3]. The goal is thus to develop, analyze and construct current-mode data-acquisition and conversion circuits in MOS technology for signal processing and to explore the limits of their applications.

This chapter presents several current-mode circuits and their design and operation. Section 3.1 describes the bipolar current copier, which is a fundamental building block for several current-mode signal processing circuits. A data-acquisition system in the form of a current-mode shift register is discussed in Section 3.2. In Section 3.3 a current-mode divider is described that will form an integral part of a current-mode A/D converter as its reference-generating unit. And, finally, Section 3.4 presents a successive-approximation A/D converter that operates in the current domain.

3.1 Bipolar Current Copier

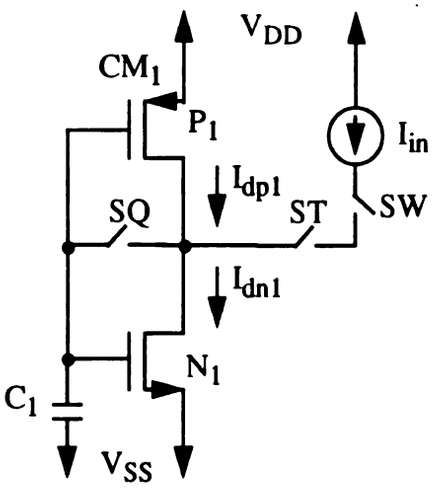
A simple *NMOS current copier*, consisting of three non-critical components: a switch, an enhancement-mode NMOS transistor, and a capacitor, is generally used to copy a positive current into its cell [39]. It has also been implemented to memorize the current difference $I_3=I_1-I_2$, where the current difference I_3 must be positive, i.e., I_1 is greater than

I_2. However, the copier cannot precisely memorize a negative current difference. Moreover, the problem of memorizing negative currents can be resolved simply by either switching the polarities of the current sources I_1 and I_2, or using a simple *PMOS current copier* with a PMOS transistor. In instances when the polarity of the current may be either positive or negative neither PMOS nor NMOS copier can be implemented. Thus, in anticipation of a time varying bidirectional input current (can be either positive or negative), as would be encountered in a general purpose multiplier or divider, a bidirectional copier is necessary. This section presents a current copier which can precisely memorize bipolar input currents.

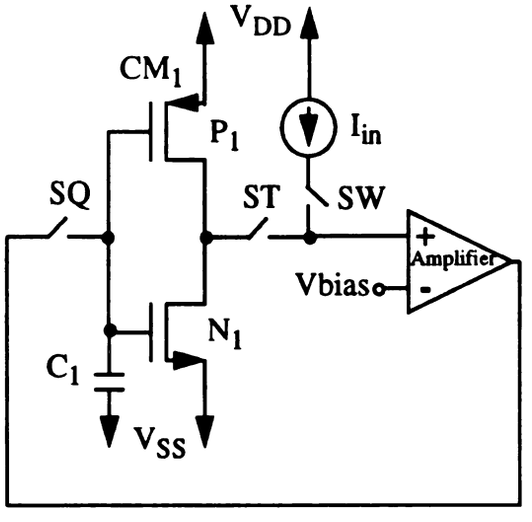
3.1.1 Circuit Design and Operation

Figure 3.1(a) shows a bipolar current copier that employs a CMOS structure CM_1 and one gate capacitance C_1 for both the NMOS and PMOS transistors. During the copying, the switches SW, ST and SQ are turned on and the capacitor will charge up to the gate voltage needed by both NMOS and PMOS transistors to achieve a current equal to the input current $I_{in}=I_{dn1}-I_{dp1}$, where I_{dn1} and I_{dp1} are the drain currents of the NMOS and PMOS transistors, respectively. If the polarity of the current I_{in} is positive, then $I_{dp1} < I_{dn1}$, otherwise $I_{dp1} > I_{dn1}$. Note that $I_{dp1}=I_{dn1}$ if $I_{in}=0$. After the copying, switches SW and SQ are turned off to disconnect the cell from the input current source, and then the cell is ready to source or sink current when connected to a load with ST turned on.

The bipolar copier suffers from the same limitations of switch charge feedthrough, channel length modulation, noise and junction leakage similar to those of a simple copier. The appropriate circuit techniques discussed earlier can also be applied to the bipolar copier to reduce the error effects. For example, the effects of channel length modulation can be reduced by implementing an active copier with the addition of an opamp to fix the drain voltage as shown in Figure 3.1 (b). The opamp forces the drain voltages of both transistors to a bias voltage so that they operate in the saturation region during copy. The correct current can then be extracted by ensuring the same drain voltage at the time of retrieval.



(a)



(b)

Figure 3.1 Bipolar Current Copier: (a) Simple Copier; and (b) Active Copier

3.1.2 Analysis

The performance of the bipolar copier for a range of currents has to be analyzed. For reliable operation of the copier it is necessary that the PMOS and NMOS transistors either both be operating in the saturation region or at most one in cutoff. Thus, there is a finite range over which the copier will perform accurately.

For dual power supplies of $+V_{DD}$ and $-V_{SS}$ for the PMOS and NMOS transistors and a bias voltage, V_{bias}, of zero, one can obtain an approximate estimate of the input current range available for the active bipolar copier. One end of the range is when the NMOS transistor is operating in the saturation region while the PMOS is at pinch-off. The drain voltage being at zero and the PMOS being in pinch-off implies that the gate voltage is equal to its threshold voltage. Thus, the minimum negative current is the sum of the saturation currents of the two transistors and is given by

$$I_{min} = \frac{1}{2}\left[(k'\frac{W}{L})_p V_{DD}^2 - (k'\frac{W}{L})_n (V_{tp} - V_{SS} - V_{tn})^2 \right] \tag{3.1}$$

where $(k'\frac{W}{L})_p$ and $(k'\frac{W}{L})_n$ are the device transconductance parameters of the PMOS and NMOS transistors, respectively and V_{tn} and V_{tp} are their threshold voltages. The second term of (3.1) is zero when the NMOS transistor is in the cutoff region. Similarly, for the PMOS and NMOS transistors operating in the saturation region and pinch-off, respectively, the maximum positive current is determined by

$$I_{max} = \frac{1}{2}\left[(k'\frac{W}{L})_n V_{SS}^2 - (k'\frac{W}{L})_p (V_{tn} - V_{DD} - V_{tp})^2 \right] \tag{3.2}$$

and the second term vanishes when the PMOS transistor is in cutoff.

3.1.3 Experimental Results

In order to verify the performance and analysis of the bipolar copier design, both simulations and experimental tests were carried out.

A prototype active bipolar copier, which is comprised of a CD4007 dual complementary pair chip and a μA741 opamp, has been implemented where the dual power supplies of ±2.5V were employed [40]. The experimental results are plotted in Figure 3.2, where the capacitance C_1=46.035pF and the applied input currents range from -2.2mA and +2.2mA. Both drain currents I_{dn1} and I_{dp1} are measured by two ammeters. Since both PMOS and NMOS transistors in the CD4007 chip have virtually the same device transconductance parameters $k = k'(\frac{W}{L})$ the plot is nearly symmetrical. Results show that I_{dp1}=2.0mA and I_{dn1}=0mA if I_{in}=-2.0mA; I_{dp1}=1.18mA and I_{dn1}=0.08mA if I_{in}=-1.10mA; I_{dp1}=I_{dn1}=0.49mA if I_{in}=0mA; I_{dp1}=0.06mA and I_{dn1}=1.15mA if I_{in}=+1.09mA; and I_{dp1}=0mA and I_{dn1}=2.0mA if I_{in}=+2.0mA. The experimental results show that I_{min}= -1.4350mA and I_{max}=+1.4370mA, i.e., the prototype bipolar current copier can reliably memorize the input currents within this range.

PSpice, a circuit simulator of the SPICE (Simulation Program with Integrated Circuit Emphasis) family, was used to verify the bipolar copier operation. The simulations assume the transistor parameters of the MOSIS 2μm CMOS technology, i.e., k'_n=56.06μA/V^2 and k'_p=22.3μA/V^2, V_{tn}=0.771327V, and V_{tp}=-0.78821V. The simulations were carried out to further verify the operation of the copier circuit. The switches were modeled as ideal switches and were operated at a cycle time of 1μsec. In order to keep the symmetry of the drain currents for both NMOS and PMOS, the aspect ratios of the NMOS and PMOS transistors were chosen as 2μm/2μm and 5μm/2μm, respectively. This implies that $(k'\frac{W}{L})_n = 56.06\mu\frac{A}{V^2}$ and $(k'\frac{W}{L})_p = 55.75\mu\frac{A}{V^2}$. The power supplies were a V_{DD} of 5 volts and V_{SS} at ground. Note that *PSpice* represents the drain current in a MOSFET m1 as Id(m1). Also, *PSpice* shows the opposite polarity of current in the PMOSFETs. Thus, all graphs and plots from *PSpice* have a negative sign for Id(mp), the drain current in the PMOSFET mp.

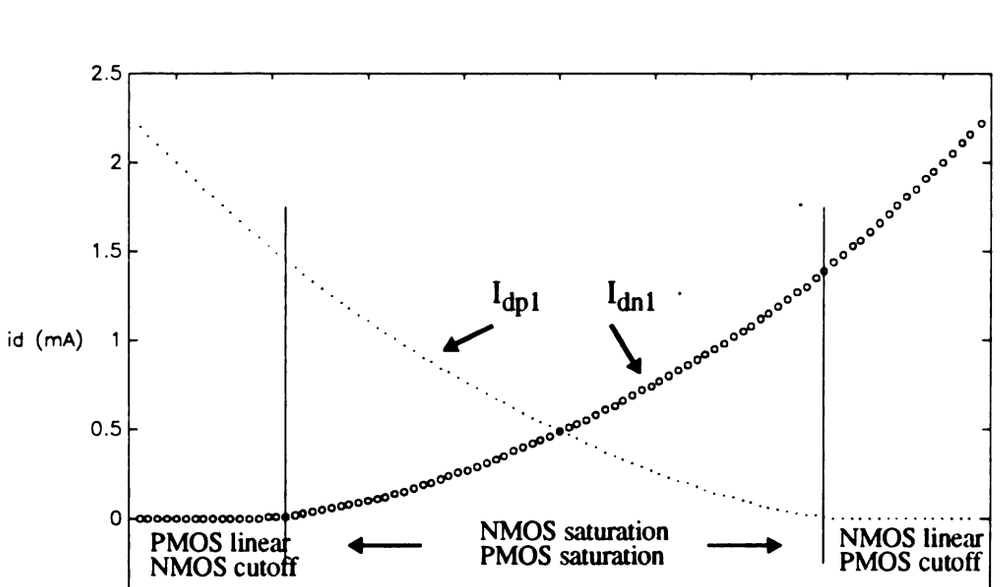
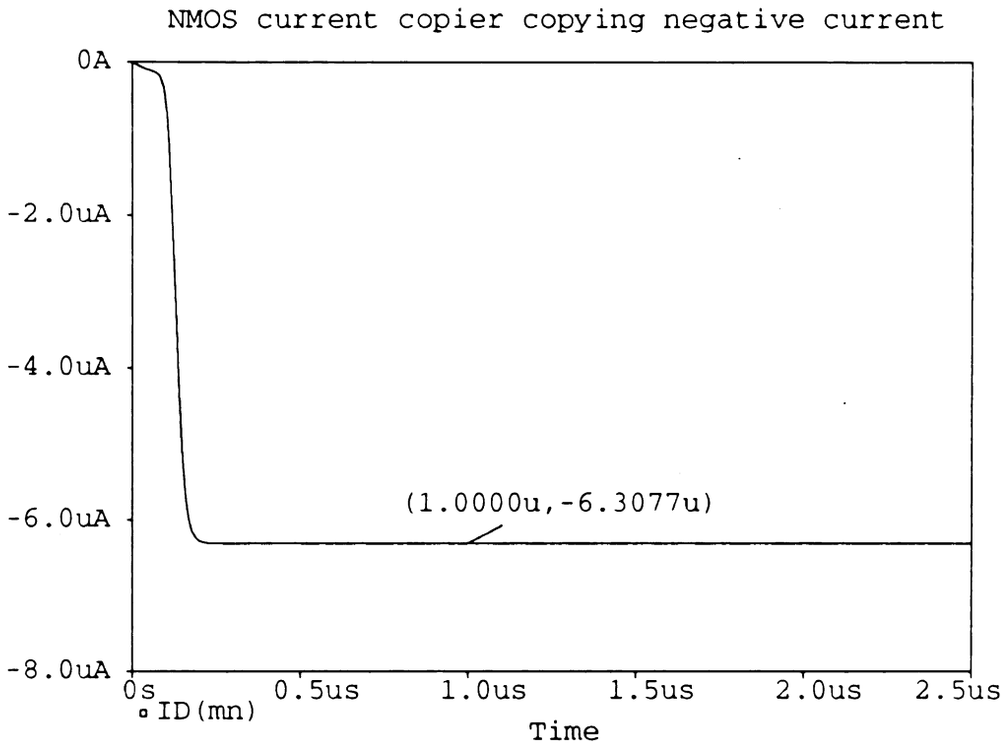


Figure 3.2 Experimental Results of a Bipolar Current Copier



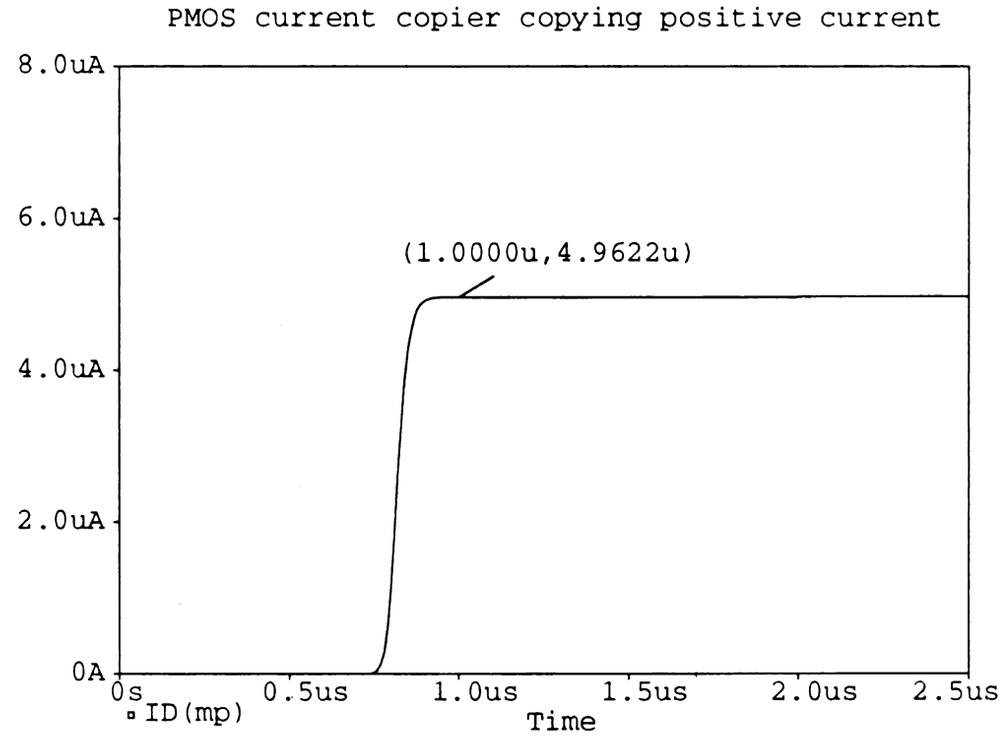


Figure 3.3 Unidirectional Limitation of NMOS and PMOS Copiers

Figure 3.3 illustrates that an NMOS copier cannot copy negative current while a PMOS copier cannot copy positive ones. When a negative current of -50μA is copied into an NMOS copier the NMOS device is forced to copy -6.3109μA as it cannot source current. Similarly as the PMOSFET in a PMOS copier cannot sink current, a positive current of 50μA is copied as 4.9679μA. However, the bipolar current copier is capable of copying both positive and negative polarity currents as seen in the simulations of Figure 3.4. For I_{in}= 50.039μA, the current copied to the NMOS was Id(mn1) = 98.606μA and to the PMOS, Id(mp1) =-48.553μA. The positive input current then read out to a PMOS copier as load was equal to 49.900μA thus having a percentage error of 0.277%. On the other hand, a negative input current of I_{in} = -50.023μA resulted in Id(mp1) =-98.198μA and Id(mn1) = 48.155μA. This current on retrieval to an NMOS copier, as illustrated in Figure 3.4, produced an error of 0.527%.

It should be mentioned that, based on the *PSpice* parameters and (3.1) and (3.2), the range that can be accurately obtained from this copier results in I_{min}= -0.298mA and I_{max}=0.3mA. In practice, the range of the input currents can be improved by increasing the aspect ratios $(W/L)_n$ and $(W/L)_p$ but at the cost of larger chip area. In order to study the effects of channel length modulation, the functioning of the active copier of Figure 3.1(a), was also simulated, where a two-stage CMOS opamp and a V_{bias} of 2.5 volts were employed. Figure 3.5 illustrates the performance of this active copier. The percentage error in copying +50μA was 0.091% and the accuracy for -50μA was 0.039%. The results show that the active copiers significantly reduce the effects caused by channel length modulation.

3.2 Current-mode Shift Register

A current-mode shift register can sample the data in parallel and then serially read it out to be converted by either a high-speed current-mode A/D converter, or an array of medium-speed converters [41]. Thus, the shift registers can be used where the data is transmitted serially over a single pair of wires, instead of as parallel bits over many wires.

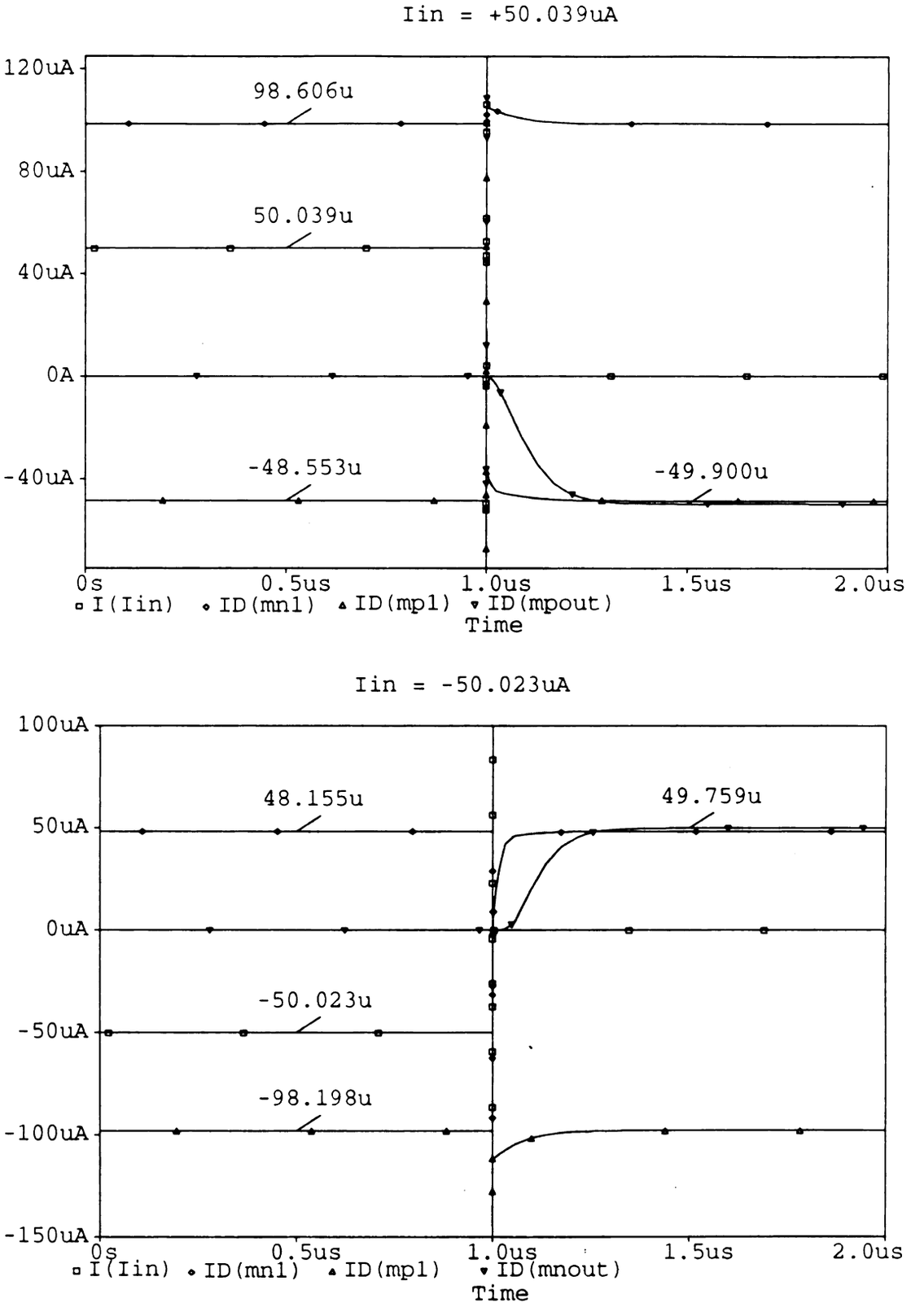


Figure 3.4 *PSpice* Simulation of a Bipolar Current Copier

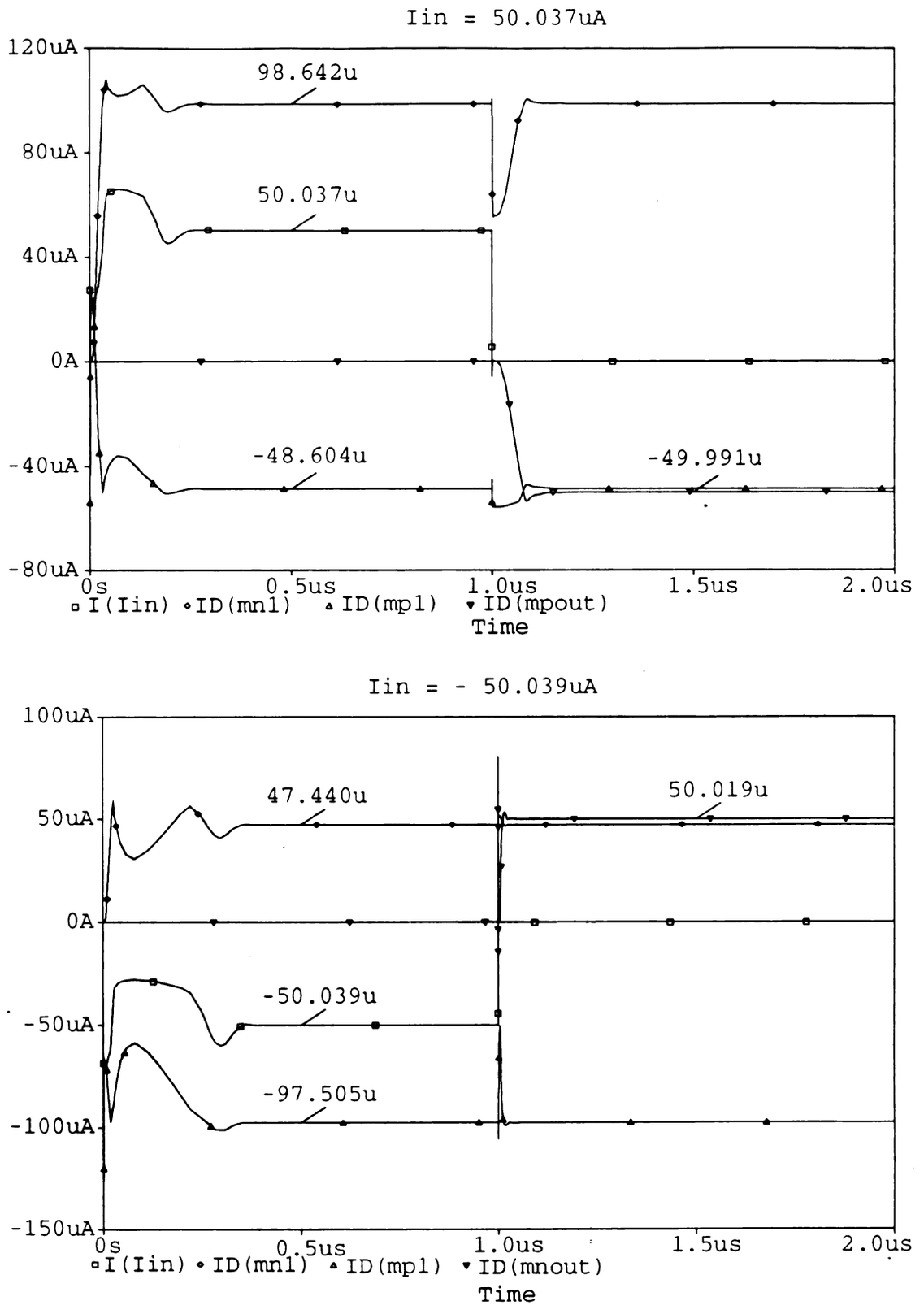


Figure 3.5 *PSpice* Simulation of a Bipolar Active Copier

In this section, current-mode shift register structures for sampling and holding current data are discussed.

3.2.1 Operation Principle

Figure 3.6 shows a shift register using simple current copiers, where four sampling nodes, m_i, i= 1 to 4, are assumed from the sensors and a 4-stage current-mode shift register is considered. Each current copier is defined as a Current Storage Cell, *CSC#i*. The timing diagram, as shown in Figure 3.7, shows the switching sequence of the current-mode shift register for its operation which proceeds in two stages: load and shift.

Figure 3.8 illustrates a part of the load/shift operation. First, the switches SW_i, ST_i, and SQ_i are all turned ON, as shown in Figure 3.8 (a), loading data into the current storage cells. Once the data is held in the *CSC#i*, the switches SW_i, ST_i, and SQ_i are turned off. This cycle is referred to as the *load process*. The *shift process* proceeds in a *last stage first out* fashion. More specifically, the datum held in the last stage (or the fourth stage in Figure 3.6) is first shifted out by turning on the switches SP_4 and ST_4, where the switches ST_1, ST_2, and ST_3 remain OFF, as shown in Figure 3.8(b); thereafter, the load will source a current I_4 which is the same as the stored current in *CSC#4*. This is followed by switching on SP_3, and ST_3 and turning off ST_4, as shown in Figure 3.8(c), and the load will copy a current I_3 that is stored in *CSC#3*. The subsequent data are processed in a similar manner and the operation is carried out continually until the current held in *CSC#1* is finally processed. It should be noted that switches ST_i help disconnect those storage cells which are not being processed. For instance, when data held in *CSC#3* is being processed, the load may source current to both *CSC#3* and *CSC#4* in the absence of ST_4 and copy an incorrect datum. The accuracy of the current-mode shift register suffers due to the same non-ideal effects that limit the performance of the basic current copier. For example, during readout the drain voltage varies due to the load, a PMOS copier, and the channel length modulation parameter causes an original-to-copy error. This limitation can be overcome with the use of active current copiers as illustrated in the alternative structure in Figure 3.9.

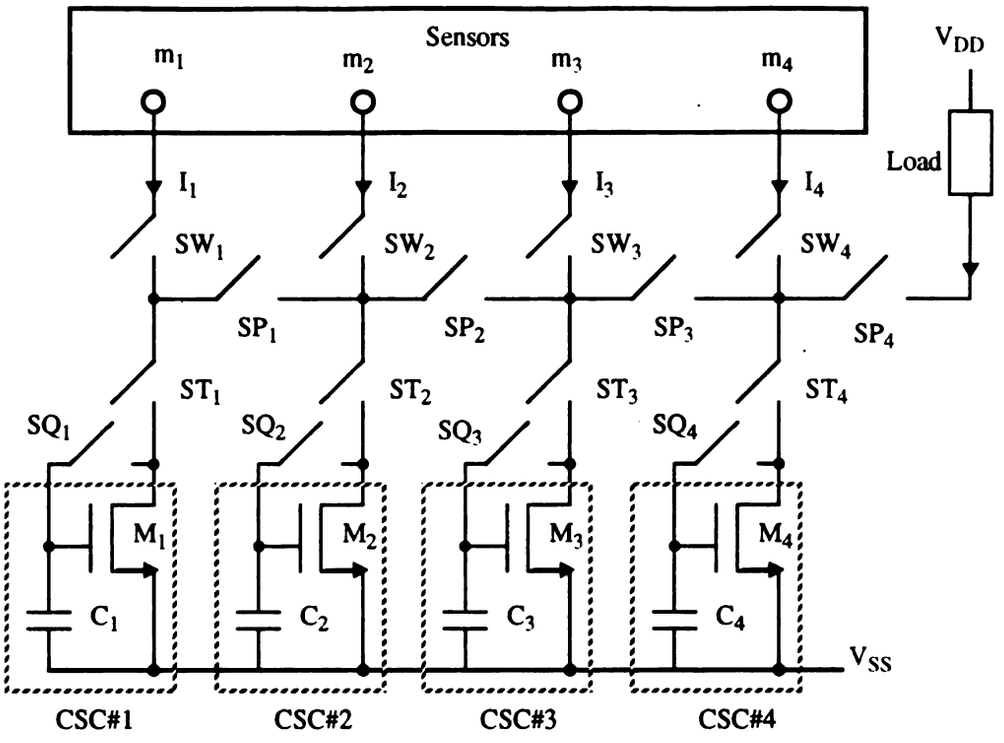


Figure 3.6 Current-mode Shift Register Using Simple Current Copiers

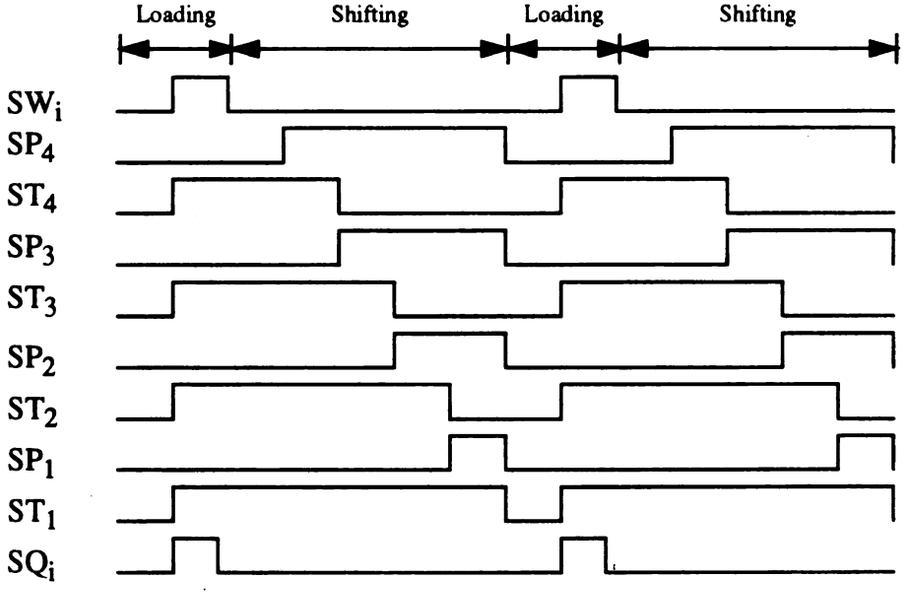


Figure 3.7 Switching Sequence for Load/Shift Operation

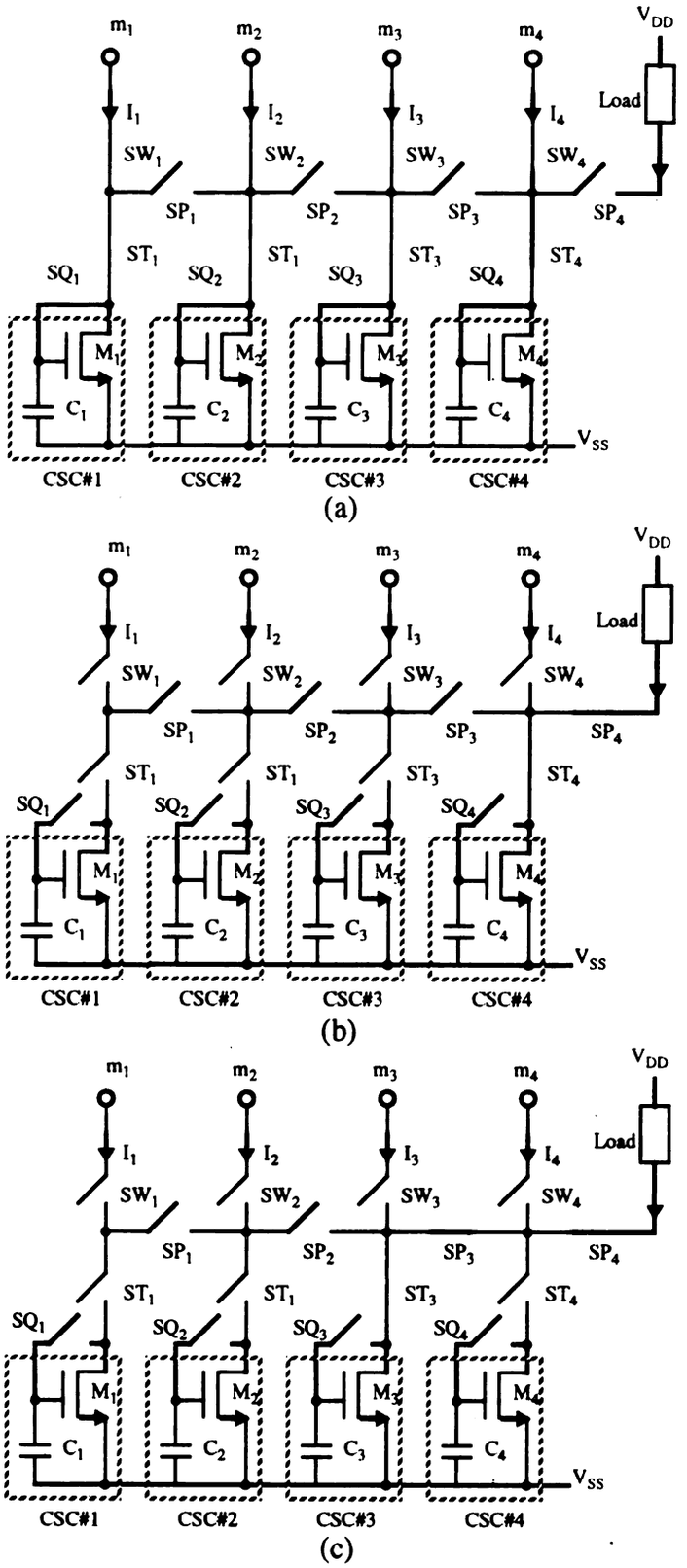


Figure 3.8 Operation Sequence during Load/Shift: (a) Parallel Loading; and (b) & (c) Serial Shifting

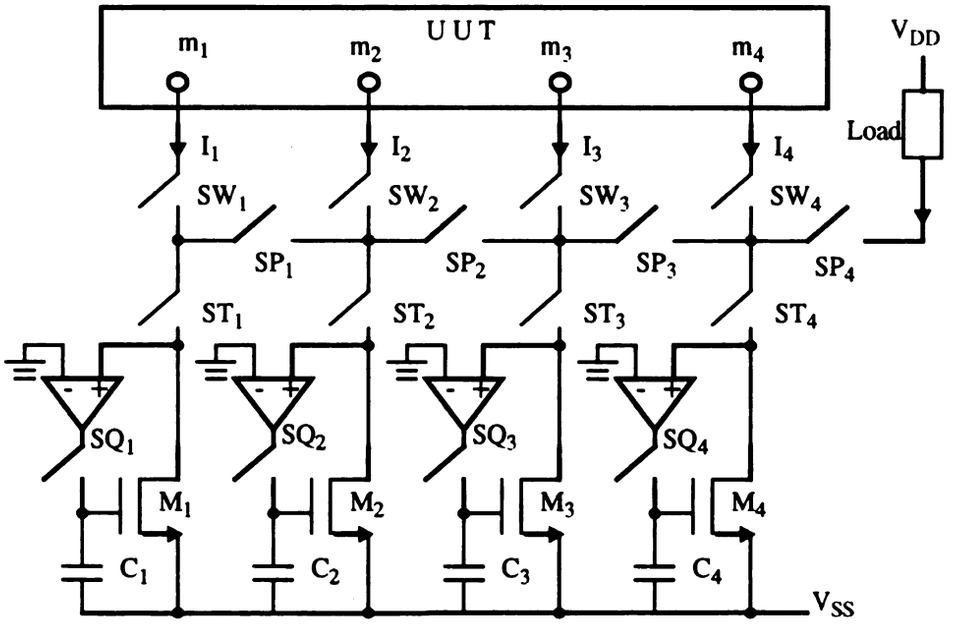


Figure 3.9 A Current-mode Shift Register Using Active Current Copiers

3.2.2 Design Considerations

The current-mode shift register being a set of sample-and-hold elements suffers from problems faced by many data-acquisition systems. The various practical issues that must be investigated are (1) determination of the acceptable change and the effect of the change in the gate voltage held in the capacitor during the read-out stage; (2) the relationship between the clock rate and the highest allowed signal frequency; and (3) accumulation of errors due to charge injection from the series switches.

The acceptable change in the sampled voltages during the shifting process is limited due to charge leakage from the holding capacitor through the switch wherein there is a constant drift of the gate voltage. The effect of the leakage current is given by

$$I_{leakage} = C\frac{\Delta V}{\Delta t} \tag{3.3}$$

where C is the net capacitance of the holding capacitor and the gate to source capacitance of the MOS transistor. The effect of the change in the gate voltage brings about a relative change in the copier current given by

$$\frac{\Delta I}{I_o} = g_m\frac{\Delta V}{I_o} \tag{3.4}$$

where g_m is the transconductance and I_o is the drain current.

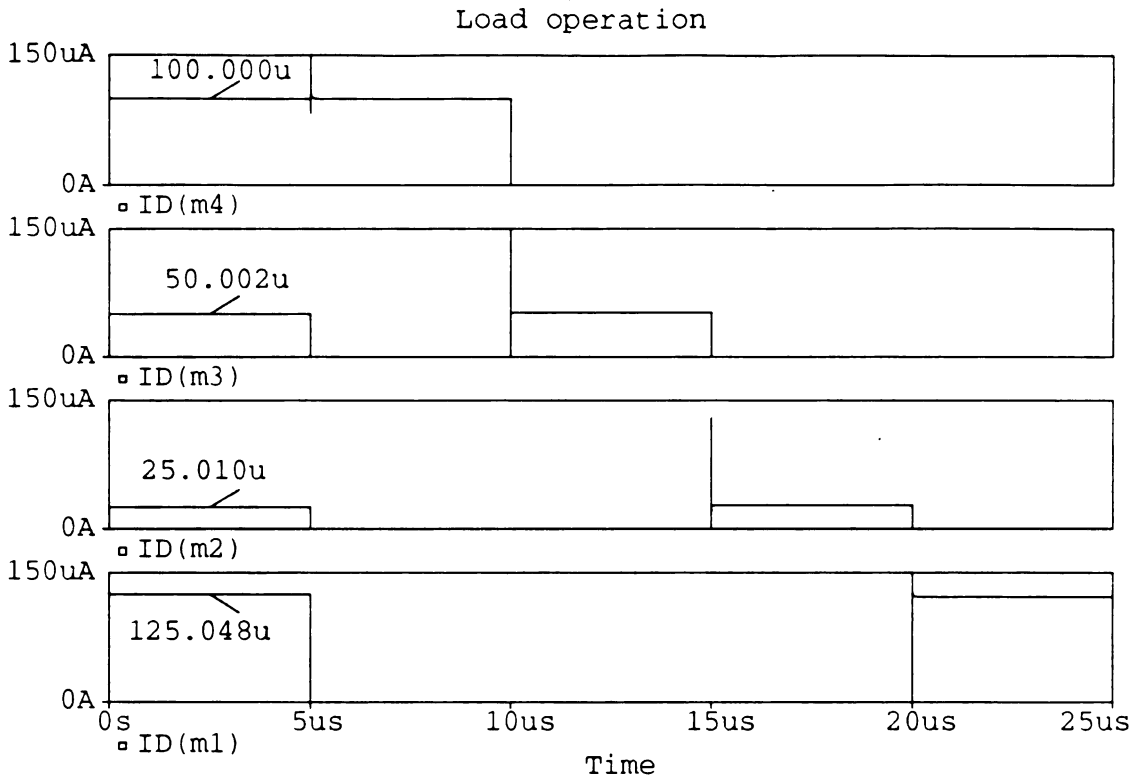
The accuracy of the gate voltage can be improved by either increasing the capacitance or decreasing the leakage current. Though holding accuracy can be improved by capacitors of larger size, this is at the cost of acquisition time. A better methodology would be to carefully allocate the test points so that smaller voltage values sampled at the register cell are closer to the output terminal while larger values that can be held longer are further down. Thus, given a percentage accuracy or allowable original-to-copy error, (3.3) and (3.4) can be used to attain the acceptable change in gate voltage.

In general, the maximum sample rate of the BIST structure is determined by the time intervals spent in the sample and hold mode. The minimum time in the sample mode is established by the sample-and-hold acquisition time, i.e., the time for which the SW_i switches are on. The time interval in the hold mode is determined by the sequence in which the data stored in register cells is read out. According to the structure, the further the register cell is from the output terminal, the longer the holding time. Wide BIST structures are thus not encouraged, and, if more test points are to be sampled, more output terminals may be used.

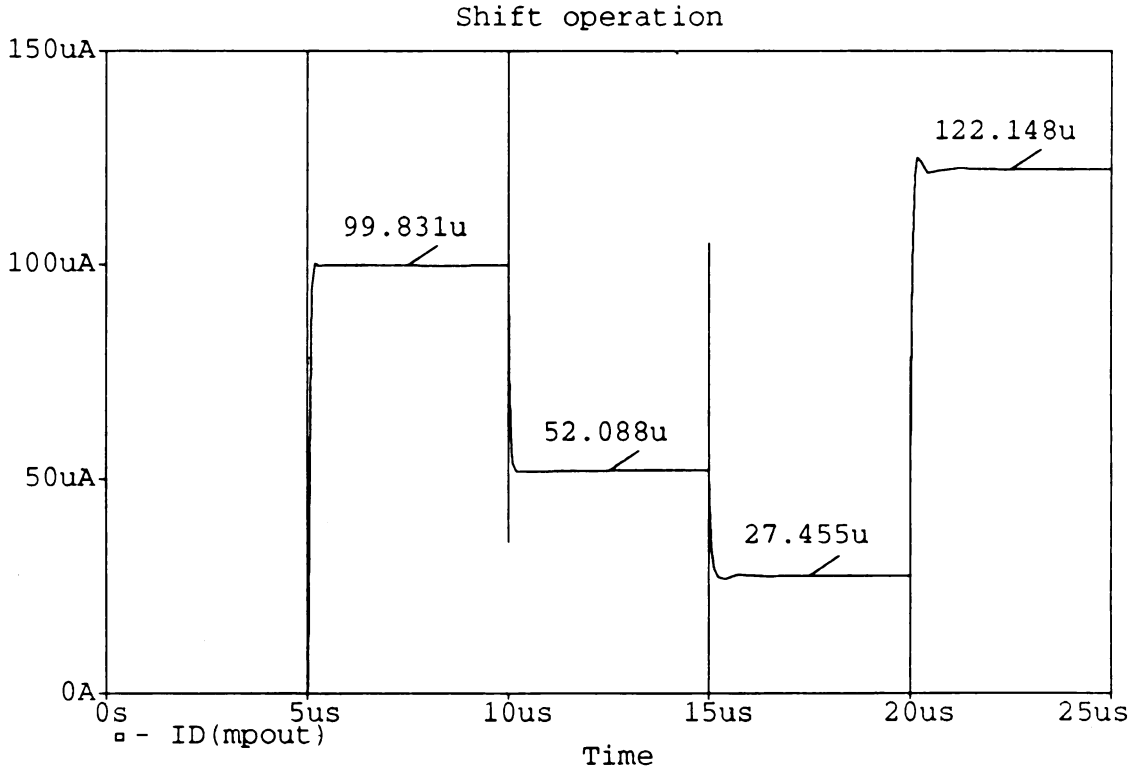
3.2.3 Simulation Results

The operation of a four-stage current-mode shift register has been verified using *PSpice* where the transistor parameters of the MOSIS 2μm CMOS technology and ideal switches were assumed. During the load cycle, the currents loaded into the current storage cells were such that Id(m4)=100μA, Id(m3)=50.002μA,Id(m2)=25.010μA and Id(m1)= 125.048μA as seen in Figure 3.10(a). During the first shift at the time step of 5μsec, the PMOS copier load reads out 99.831μA from CSC#4 with an error of 0.169%, and the second shift yields an output current of 50.088μA at -4.171% error. The shift operation proceeds as seen in the plot with the data in CSC#2, 27.455μA and CSC#1, 122.148μA shifting out during the third and fourth cycle at -9.776% and 2.319% errors, respectively.

As seen from Figure 3.10 (b) the circuit performance when the varied currents of 125μA, 25μA, 50μA and 100μA are sampled into the shift register is not adequate. The read-out to a PMOS copier load causes changes in the drain voltage during every cycle of the shift stage giving rise to considerable errors. For a similar sampling operation the shift register with active copiers provides a more accurate output, as shown in Figure 3.11, since the opamp fixes the drain. 100μA is read out as 99.908μA with 0.092% error while 50μA is obtained within -0.129% error. 25μA and 125μA can be shifted out with percentage accuracy of 0.006% and 0.012%, respectively. The improved current-mode shift registers provide more accurate data than those using the simple copier, but they require more chip



(a)



(b)

Figure 3.10 Simulation of the Current-mode Shift Register: (a) Varied Inputs; and (b) Output of the PMOS Copier Load

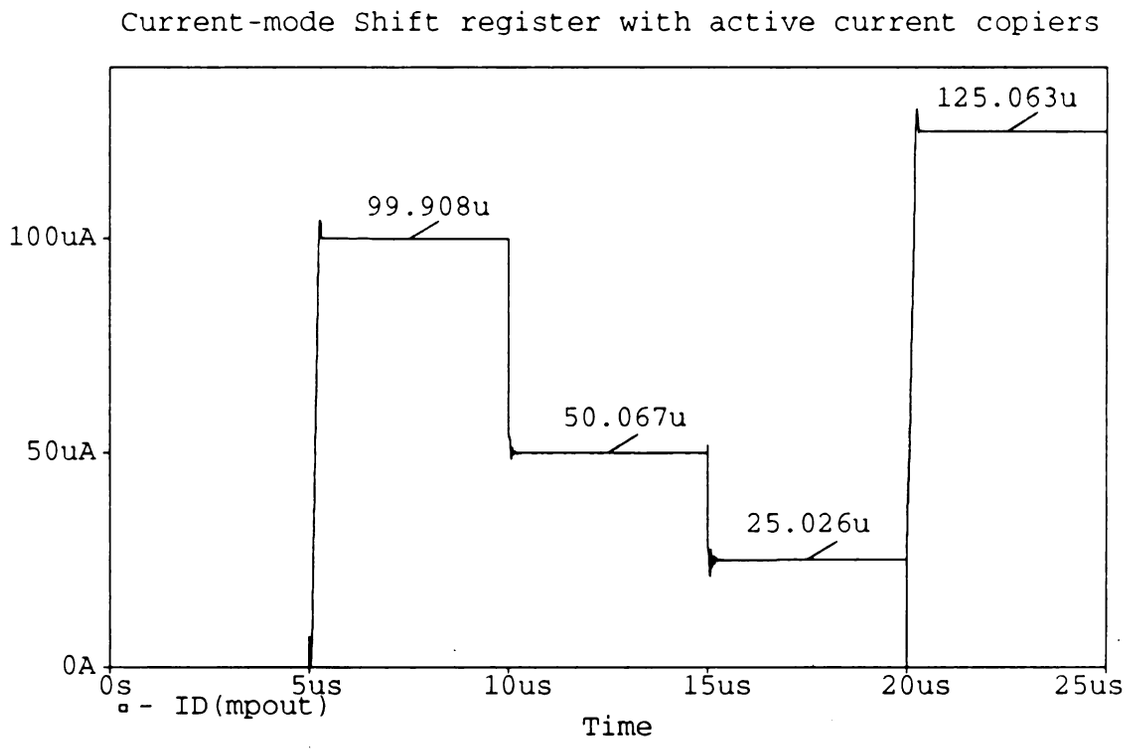


Figure 3.11 Simulation of the Shift Register with Active Copiers

area to implement them. The improved structure may be used in cases where the original and copied currents must be matched precisely.

Other error effects that have to be analyzed are those of the sample-and-hold procedure. According to (3.3) and (3.4), the performance of the copier deteriorates due to the drop in holding voltage and, as observed in Figure 3.6, the further the register cell is from the output terminal, the longer the holding time and thereby the greatest error. Consider the case when an input of 125.057μA is copied into all the four cells. The read-out current from each stage is plotted in Figure 3.12. The error in current read out from the last stage, CSC#1, due to junction leakage can be seen from Figure 3.12 where the leakage current in the holding capacitor C_1, I(c1), is approximately -30.483nA. Thus, for a gate capacitance of 40pF and a hold time of 15 μsec, i.e. from the instant the switches are shut off after load to the time the data in the cell are shifted out, the change in voltage from (3.3) is approximately -11.43mV and a value of -11.35mV is read off the plot. A few methods by which the holding accuracy can be improved are by capacitors of larger size or by employing faster clock rates. Figure 3.13 shows simulations in which both these alternatives were tried out to verify these design options. With the same leakage current and hold time as before and a hold capacitance two times larger of 80pF, an error of 6.1mV was obtained while the theoretical prediction from (3.3) was 5.715mV. Thus, the accuracy was improved, but at the cost of acquisition time, as seen in the plot. With the hold capacitance of 40pF, data was acquired in 2.075μsec, while double the capacitance took almost twice as long, i.e., 3.95μsec.

Figure 3.13 shows simulations run at a faster sampling rate of 1 MHz. Sampling faster implies that the capacitor discharges for a shorter time and so the accuracy does not deteriorate too much. With Δt of only 3μsec, (3.3) predicts a fifth of the previous error, and the plot indicates an error of only 2.4mV.

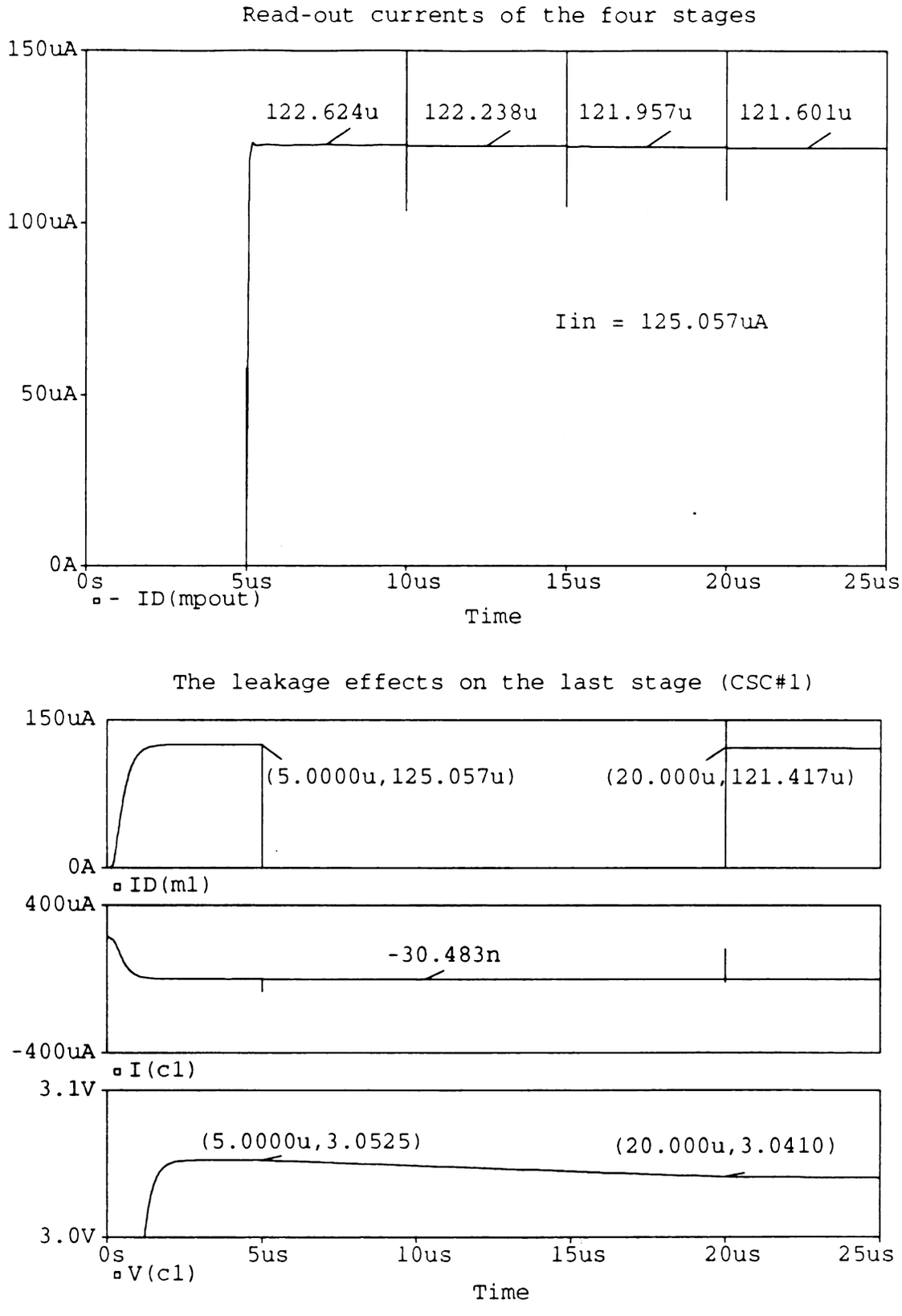


Figure 3.12 Error Effects of the Sample-and-hold Procedure

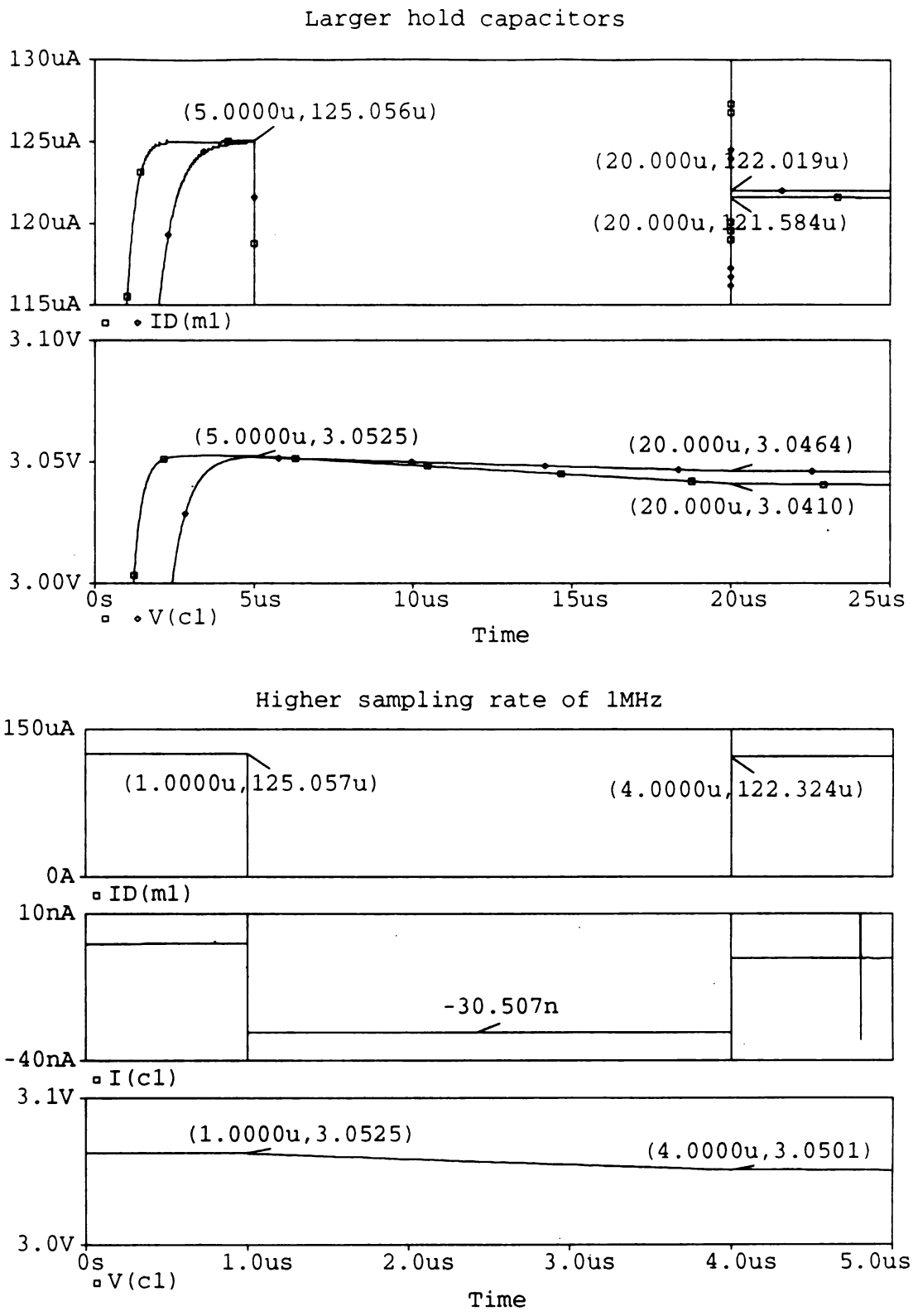


Figure 3.13 Improvements to the Acquisition Procedure

3.3 Current-mode Divider Circuit

Current division has traditionally been carried out using resistive networks or weighted transistors. However the precision of such schemes are limited by device mismatch. The highly accurate current divider in Section 2.2. overcomes this limitation by using dynamic techniques, and the system converges to give an accurately divided current [35]. Note that an NMOS current copier is generally used to store the positive input currents. Results have shown that the copier cannot precisely memorize any negative input currents. Since the NMOS transistor N_1 is used to hold the current difference between I_2 and I_3 in the circuit of Figure 2.8, where $I_1=I_3-I_2$, the current difference must be positive, i.e., I_3 must be greater than or equal to I_2.

When the mismatch factor α is such that $0 < \alpha < 0.5$, then the system response is overdamped and all copier currents are unidirectional [1]. But if α is in the range such that $0.5 < \alpha < 1$, then the system will become underdamped, and some currents may change sign while the system is converging. In this case the roles of N_3 and N_2 would have to be reversed, which is possible only if switch programming can be implemented. In practice, the mismatch of transistors is unknown in advance and thus the divider circuit functions properly only when the mismatch between the transistors N_3 and N_2 makes $Idn_3 > Idn_2$. Another solution to the problem which would be less complex is the use of a bidirectional copier. Therefore, an alternative current-mode divide-by-two circuit which allows any mismatch in N_3 and N_2, utilizing a bipolar copier is discussed in this section. This circuit can then be used if I_{in} is allowed to be bidirectional thus becoming an important general purpose analog current-mode divider.

3.3.1 Method of Operation

Figure 3.14 illustrates the schematic diagram of the alternative current-mode divide-by-two circuit. The divider operation and its switching sequence are exactly the same as those described in Figure 2.8 and are illustrated in Figure 3.15. However, the

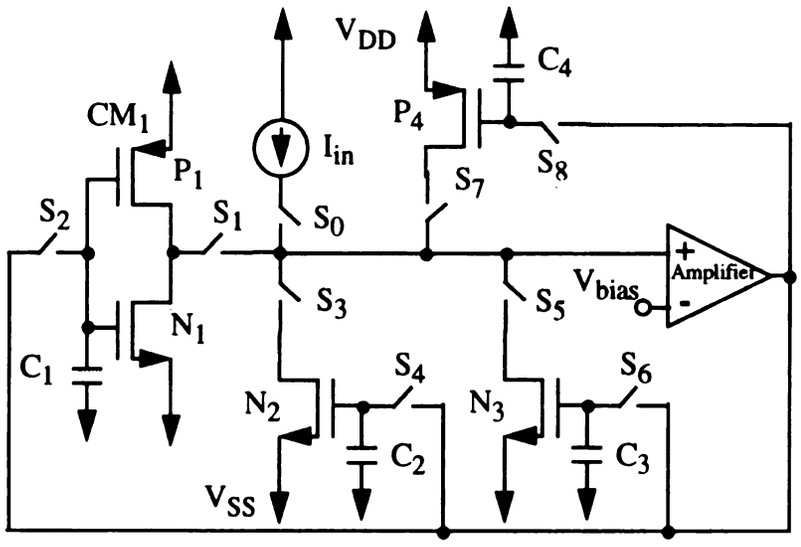


Figure 3.14 The Alternative Current-mode Divider

Clock	Copying Sequence
1	$I_{in} \rightarrow N_2$& N_3
2	$N_3 \rightarrow P_4$
3	P_4- $N_2 \rightarrow N_1$
4	I_{in}–$CM_1 \rightarrow N_2$& N_3
5	$N_3 \rightarrow P_4$
6	P_4- $N_2 \rightarrow N_1$
7	I_{in}–$CM_1 \rightarrow N_2$& N_3

Figure 3.15 Operational Sequence of Divider

NMOS current copier with N_1 used to store the current difference in Figure 2.8 is replaced by a bipolar CMOS copier CM_1 [42]. Since the bipolar copier can memorize both positive and negative input currents, where the memorized current = Idn_1-Idp_1, this divider circuit will function properly for any mismatch between N_2 and N_3. With the mismatch factor α_2 greater than α_3, less current is copied to N_3. Thus, $Idn_3 < Idn_2$ and the bipolar copier stores the negative current difference (Idn_3-Idn_2), where $Idp_1 > Idn_1$. On the other hand, $\alpha_2 < \alpha_3$ implies the positive current difference (Idn_3-Idn_2) of the division is stored in the bipolar copier structure, with $Idp_1 < Idn_1$. The error due to channel length modulation can be reduced by the use of an opamp to fix the drain to source voltage. The gate capacitors, C_i, are used to reduce the effects of the charge injection from switches and to allow the transistor and capacitor geometries to be determined independently. The circuit accurately divides the input current I_{in} by two, irrespective of the mismatch between the two transistors, and stores the result in N_3. Note that the divider circuit does not rely on any well-matched components or a high gain opamp.

3.3.2 Performance Estimation

The structure of the divider indicates that current division can be carried out effectively. However, the number of iterations necessary to obtain $I_{in}/2$ with a certain accuracy depends on the mismatch of the transistors N_2 and N_3 in the divide-by-two circuit. The performance and accuracy of the divider considering its dependence on several parameters is analyzed. Let γ be defined as the mismatch ratio of the transistors N_2 and N_3, where $\gamma=(\alpha_3/\alpha_2)-1$. Therefore, γ is positive if the mismatch factor α_3 is greater than α_2, otherwise γ is negative.The relationship between the number of iterations required for the division process and the desired accuracy for a given mismatch has now to be addressed.

According to the current copying sequence listed in Figure 3.15, at the end of the first cycle of the first iteration, N_2 copies $I_2 = \alpha_2 I_{in}$, and N_3 obtains the current $I_3 = \alpha_3 I_{in}$. Thus, the currents copied to these transistors in terms of γ are

$$I_2 = I_{in}\left(\frac{1}{2+\gamma}\right) \quad \text{and} \quad I_3 = I_{in}\left(\frac{1+\gamma}{2+\gamma}\right) \tag{3.5}$$

The current difference, I_3-I_2, held in CM_1 at the end of the third cycle is approximately

$$I_1 = I_{in}\left(\frac{\gamma}{2+\gamma}\right) \tag{3.6}$$

As a result, at the end of the first cycle of the second iteration, I_{in} - I_1 is now sourced and so the current held in N_3 becomes

$$I_3 = (I_{in} - I_1)\left(\frac{1+\gamma}{2+\gamma}\right) = I_{in}\left(1 - \frac{\gamma}{2+\gamma}\right)\left(\frac{1+\gamma}{2+\gamma}\right) \tag{3.7}$$

Similarly, at the end of the first cycle of the kth iteration, the current held in N_3 can be expressed as

$$I_3 = I_{in}\left[1 - \frac{\gamma}{2+\gamma} + \left(\frac{\gamma}{2+\gamma}\right)^2 - \ldots + (-1)^{k-1}\left(\frac{\gamma}{2+\gamma}\right)^{k-1}\right]\left(\frac{1+\gamma}{2+\gamma}\right) \tag{3.8}$$

Let I_{3k} denote the current held in N_3 at the end of the first cycle of the kth iteration. The term in brackets is a geometric progression, and since $1 + \frac{\gamma}{2+\gamma} = 2\left(\frac{1+\gamma}{2+\gamma}\right)$ (3.8) can now be re-written as

$$I_{3k} = \frac{I_{in}}{2}\left[1 + (-1)^{k-1}\left(\frac{\gamma}{2+\gamma}\right)^k\right] \tag{3.9}$$

For a reasonably uniform technology, the mismatch ratio γ generally lies between 0 and ±50%. The error term $\left(\frac{\gamma}{2+\gamma}\right)^k$ diminishes rapidly as k increases, i.e., $I_{3k} \approx I_{in}/2$. Therefore, the error term can be used to determine the number of iterations necessary to obtain $I_{in}/2$ with certain accuracy [43]. Table 3.1 illustrates the relationship among the

Table 3.1 Relationship among γ, k and the Corresponding Error Terms

k	γ=20%	γ=10%	γ=5%	γ=2%	γ=1%
1	9.09e-02	4.76e-02	2.44e-02	9.90e-03	4.97e-03
2	8.26e-03	2.26e-03	5.95e-04	9.80e-05	2.47e-05
3	7.51e-04	1.07e-04	1.45e-05	9.70e-07	1.23e-07
4	6.83e-05	5.14e-06	3.53e-07	9.60e-09	6.12e-10
5	6.21e-06	2.45e-07	8.63e-09	9.51e-11	3.04e-12
k	γ=-20%	γ=-10%	γ=-5%	γ=-2%	γ=-1%
1	1.11e-01	5.26e-02	2.56e-02	1.01e-02	5.02e-03
2	1.23e-02	2.77e-03	6.57e-04	1.02e-04	2.52e-05
3	1.37e-03	1.45e-04	1.68e-05	1.03e-06	1.26e-07
4	1.52e-04	7.67e-06	4.32e-07	1.04e-08	6.37e-10
5	1.69e-05	4.03e-07	1.11e-08	1.05e-10	3.20e-12

mismatch ratio, γ, and the iteration index, k, and tabulates the corresponding error terms. Results show that the divider circuit can achieve an accuracy within 6.21e-06 by taking 5 iterations for γ=20%. On the other hand, for a practical 1% transistor mismatching, the circuit takes only 2 iterations to achieve an accuracy within 2.47e-05 and 5 iterations for an accuracy within 3.04e-12.

3.3.3 Experimental Verification

PSpice simulations were run to test the operation of the divider assuming parameters of the MOSIS 2μm CMOS technology. The aspect ratios of the NMOS and PMOS transistors were chosen as 2μm/2μm and 5μm/2μm, respectively. This preserved the symmetry of the drain currents in the bipolar copier and kept a minimal area for the divider structure. The circuit had V_{DD} at 5 Volts, V_{SS} at ground and a V_{bias} of 2.5 Volts was picked to keep the devices in saturation. The ideal switches were operated at a cycle time of 3μsec. Figure 3.16 shows one iteration of the division process for an input current of approximately 100μA through switch S_0, I(sw0), with no mismatch between transistors N_2 and N_3. The current difference between Idn_3 and Idn_2 is very low and the divider settles down in one iteration within a duration of 9μsec. The value of the divided current in N_3 is equal to 50.018μA, and thus an error of only 0.045% exists.

The operation of the divider for several mismatch ratios between the transistors is then tested. This was established by considering all the mismatch between the two copiers to be in the aspect ratios of the transistors N_2 and N_3. For example, for a γ of 5%, $(W/L)_3$ was equal to 2.1μm/2μm while $(W/L)_2$ was 2μm/2μm. Figure 3.17 shows the currents as the iterations of the divider are carried out when a mismatch factor γ of 5% exists between N_2 and N_3. The current in N_3 is initially at 51.263μA, thus starting the division process with an error of -2.535%. The bipolar copier stores the positive error difference between N_2 and N_3 of 2.425μA and sources it for the next cycle. After two iterations, the current in N_3 settles to 50.041μA with only -0.091% error. For γ= -5%, Idn_3 is a lower value of 48.755μA with the initial error of 2.487%. The negative current difference of -2.5828μA stored in

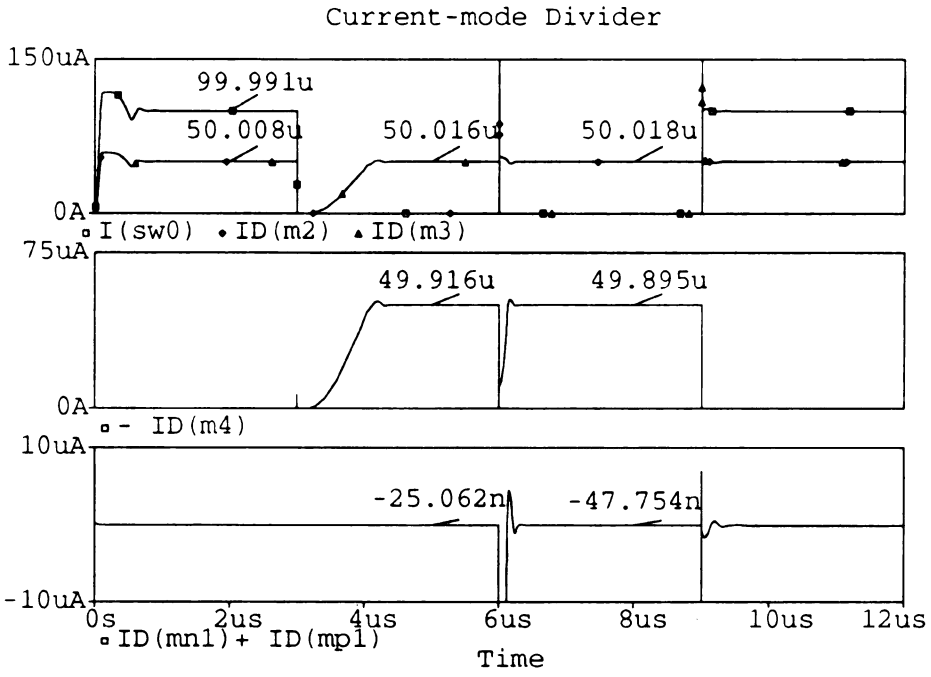


Figure 3.16 *PSpice* Simulations of the Current-mode Divider

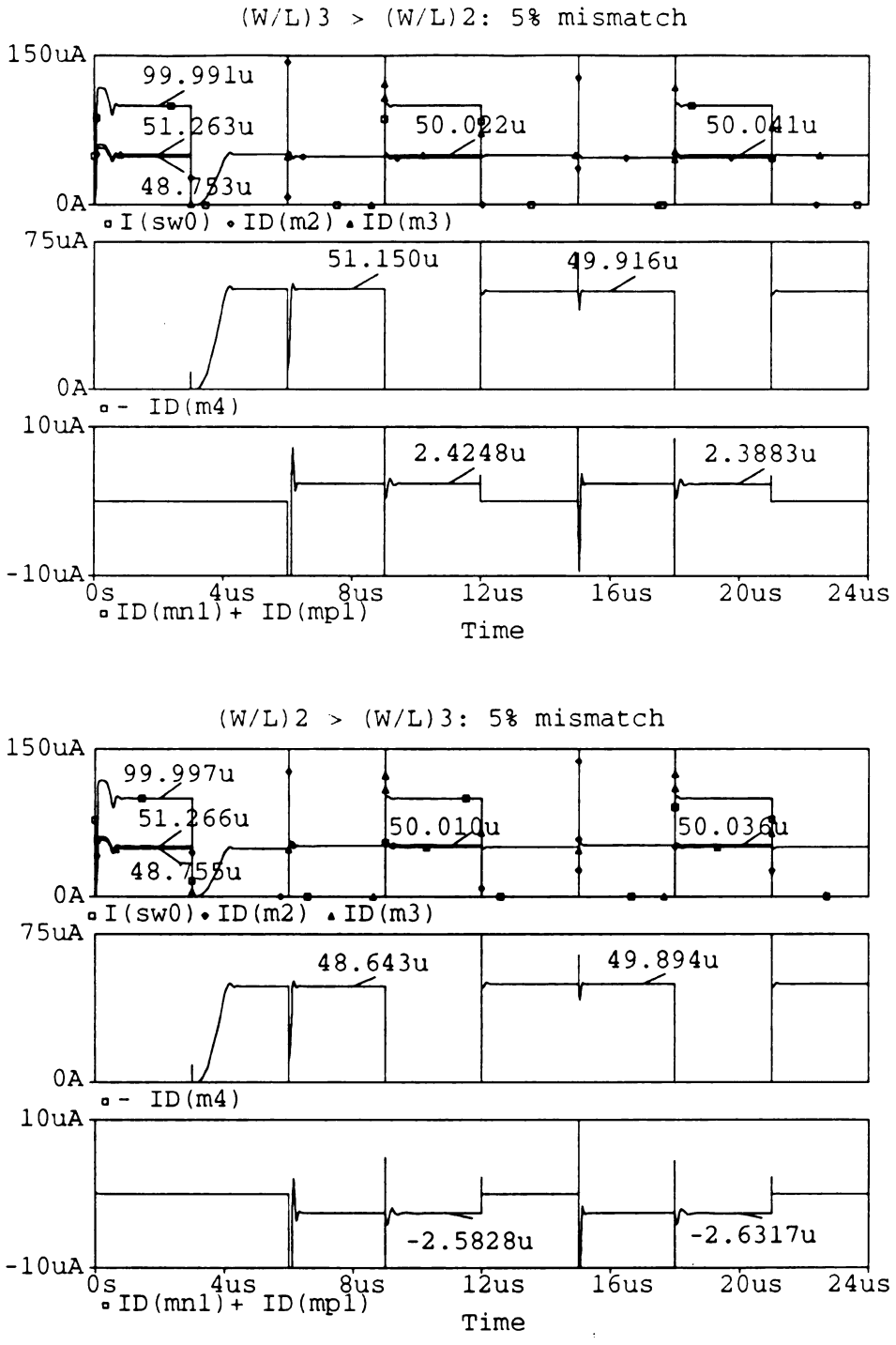


Figure 3.17 Divider Operation with 5% Mismatch

CM_1 is sourced in subsequent iterations to make the divided current be 50.036μA. Thus, the resultant error is only -0.075%.

The relationship between accuracy of the divided current and the number of iterations has been theoretically derived and is then to be verified through simulations. Figure 3.18 shows how with a mismatch γ =10% more iterations are necessary to get a required accuracy. The error begins with the value of 4.925% and reduces to 0.121%, 0.097% and 0.087% at the start of the second, third and fourth iterations, respectively. The current in N_3 varies at every iteration as CM_1 holds more of the error current to allow N_3 to obtain a more accurate value. For γ=-10%, the error starts at 4.881% and settles, at the beginning of the fourth iteration to -0.077% . To study the convergence of the error several simulations were run on the divider for an input current of approximately 100μA for various mismatch ratios. The results of these runs are tabulated in Table 3.2 in the same fashion as Table 3.1. As seen in the graph of Figure 3.19, the error converges to a finite value of approximately 0.0026, unlike the theoretical prediction of close to zero error, and the error term remains at this value for subsequent iterations. This finite error even when there is a mismatch of zero is due to the limitations in the performance of the active copiers and the functioning of the switches. A comparison run between the error for 20% mismatch and its theoretical prediction is plotted in Figure 3.20, and the finite difference in their converged values can be clearly observed.

3.4 Successive-approximation A/D Converter

The continuous progress of VLSI technology has provided the possibility of integrating a large sensor array and parallel digital processors on a single chip. The requirement on speed of the A/D converter array is not necessarily very high. However, the reduction of the size and power consumption is more important. Cyclic (algorithmic) and successive-approximation current-mode A/D converters convert an input current to an N-bit digital data word D using a *multiply-by-two scheme* and a *divide-by-two scheme*, respectively. The former scheme converts for the MSB of an input current by comparing

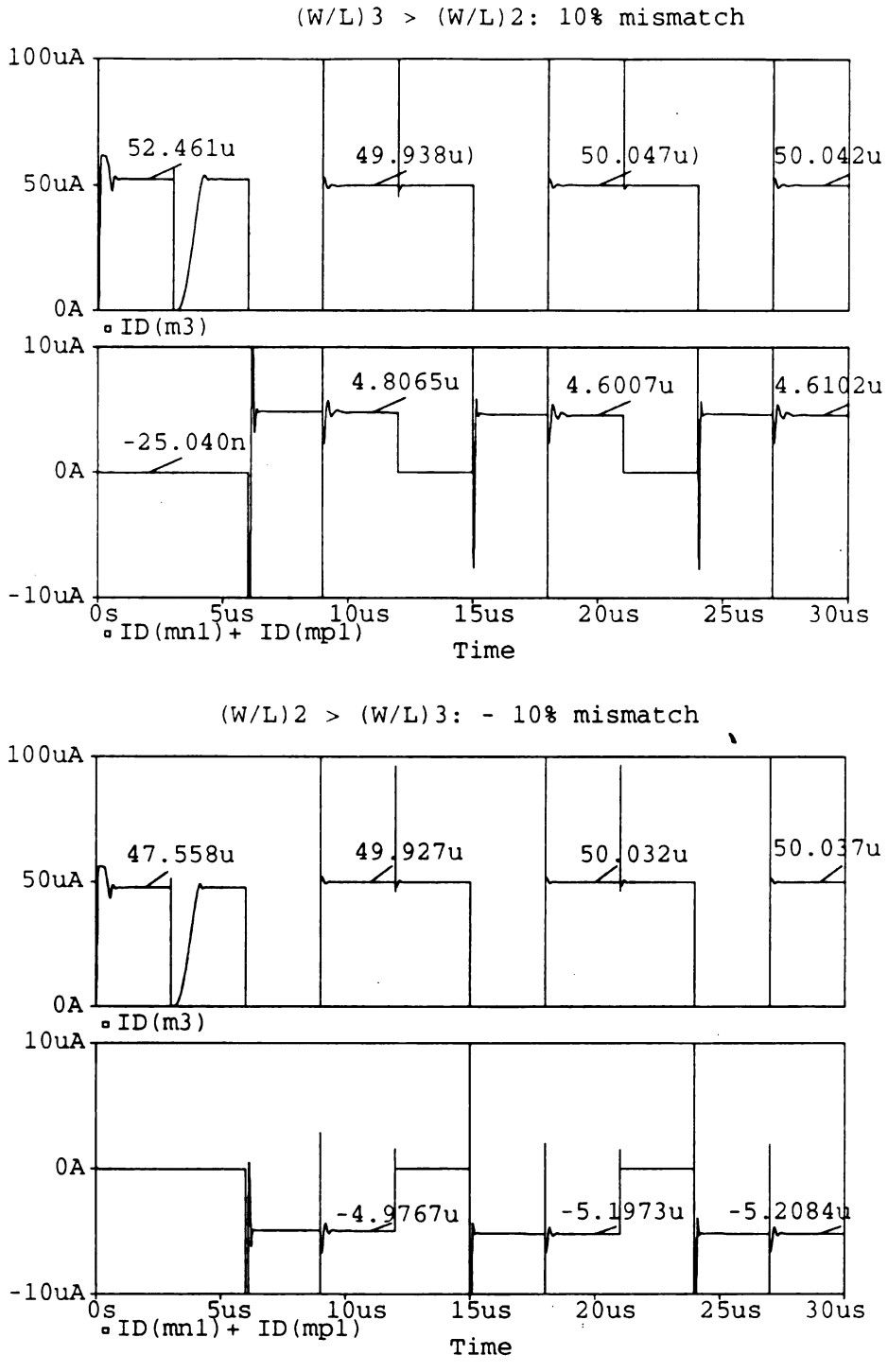


Figure 3.18 Divider Operation with 10% Mismatch

Table 3.2 Error Terms Obtained from Simulations

k	γ=20%	γ=10%	γ=5%	γ=2%	γ=1%
1	9.37e-02	4.93e-02	2.54e-02	1.04e-02	5.39e-03
2	4.47e-03	1.68e-03	2.32e-03	2.66e-03	2.72e-03
3	4.47e-03	3.51e-03	2.68e-03	2.36e-03	2.44e-03
4	3.95e-03	3.43e-03	2.69e-03	2.44e-03	2.42e-03
5	3.51e-03	3.33e-03	2.79e-03	2.48e-03	2.38e-03
k	γ=-20%	γ=-10%	γ=-5%	γ=-2%	γ=-1%
1	9.32e-02	4.87e-02	2.49e-02	9.96e-03	4.91e-03
2	6.29e-03	7.99e-05	1.74e-03	2.42e-03	2.59e-03
3	1.66e-03	2.06e-03	2.29e-03	2.32e-03	2.12e-03
4	2.04e-03	2.29e-03	2.04e-03	2.34e-03	2.42e-03
5	2.14e-03	2.18e-03	2.19e-03	2.18e-03	2.28e-03

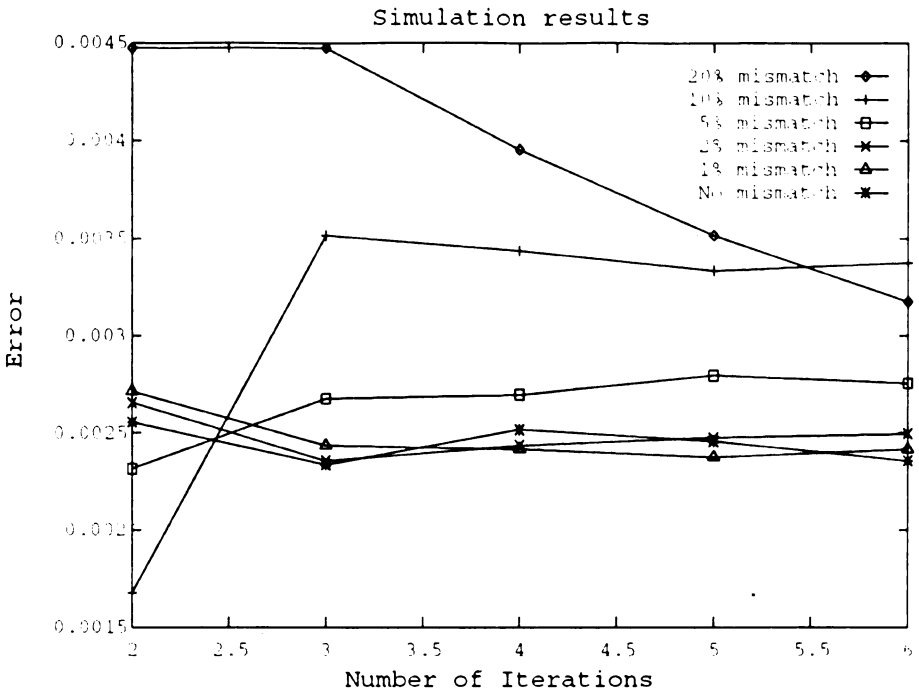


Figure 3.19 Experimental Error Terms

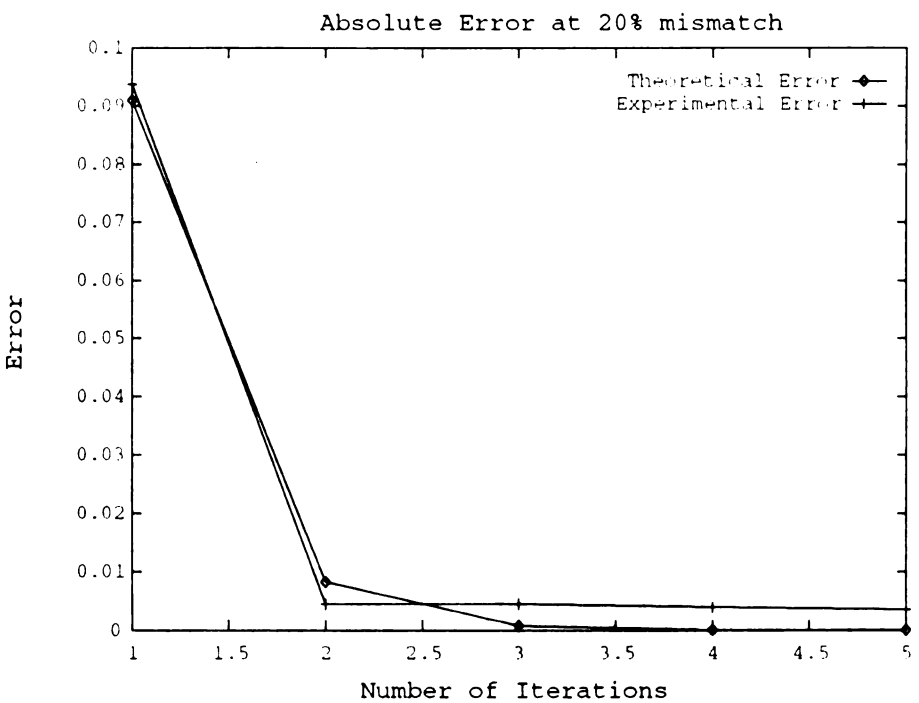


Figure 3.20 Comparison of Error Terms

twice the input current to the reference current, while the latter scheme compares the input current to half the reference current.

The multiplier approach requires simpler cells, but errors are progressively accumulated from cell to cell, and the largest current (MSB) has the worst relative precision [29]. A more severe limitation is due to noise. The accumulation of noise culminates at the MSB and can by no means be compensated. Consequently, the first cells of the multiplying cascade generate large values of noise and error, which are propagated to the MSB current. These limitations can be avoided by using the dividing scheme, which confines the larger error and noise to the least significant bits. This advantage is probably worth the increased complexity of the cells.

Since the reference current in the divide-by-two scheme is reduced constantly by half during each bit conversion, the division can be done in parallel with the bit conversion process. In the multiply-by-two scheme, however, the multiplication cannot be performed until the end of each bit conversion. Thus, A/D converters implemented with the divide-by-two scheme achieve higher conversion rates than those with the multiply-by-two scheme.

This section describes the conversion principle of a successive-approximation current-mode A/D converter implemented with the divide-by-two scheme and its detailed design and operation. The converter is comprised of a *reference-generating (RG)* circuit and a *converting (CV)* circuit as seen in Figure 3.21. The RG circuit generates the reference levels 1/2, 1/4, 1/8,..., $1/2^N$ of the reference current, while the CV circuit along with a comparator determines the converted digital bit value and the current to be converted for the next bit.

This section also describes a converter array which employs a common RG circuit that is shared by many CV circuits that process many input signals simultaneously. Due to the small number of components needed and simplicity of the current-mode circuit realization, the converter array is well suited for sensor array implementation. Results of this study will show that the converter array achieves high resolution and high conversion rate at low hardware cost

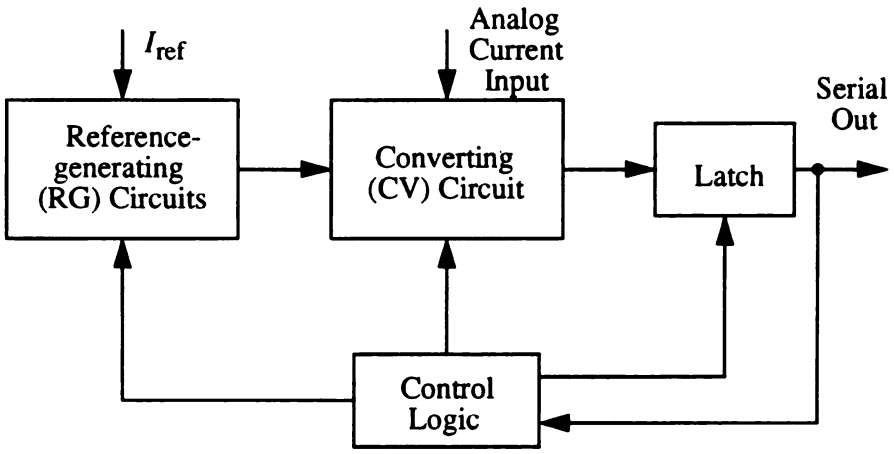


Figure 3.21 Block Diagram of a Current-mode Successive-approximation A/D Converter

3.4.1 Circuit Description

The successive-approximation current-mode A/D converter implemented with the divide-by-two scheme converts an input current I_{in} to an N-bit digital data word D, where $D = (d_1 d_2 .. d_N)$ and d_1 and d_N are the *most significant bit (MSB)* and the *least significant bit (LSB)*, respectively. The converter starts converting for the MSB by comparing the input current I_{in} to the reference current $I_{ref}/2$. If I_{in} exceeds $I_{ref}/2$, the MSB will be a "1", i.e., $d_1=1$, otherwise it will be a "0". The current to be converted for the bit d_2 depends on the preceding bit value. If $d_1=0$, then the current remains unchanged, otherwise it equals the current difference $(I_{in}-I_{ref}/2)$. Bit d_2 is determined by comparing this current to the reference current $I_{ref}/4$. The remaining (N-2) bits are obtained using the same principle.

Figure 3.22(a) shows the schematic circuit diagram of the current-mode A/D converter, where latches and control logic circuitry are not shown. The CV circuit consists of a PMOS current copier, an NMOS current copier, and an opamp. It receives the input current I_{in} and the current reference levels via switches S_I and S_R, respectively. Figure 3.22(b) illustrates the sequence of operations of the circuit. For the MSB conversion, the input current I_{in} is first copied into N_a, denoted by "$I_{in} \rightarrow N_a$". Then, the current held in N_a is compared to $I_{ref}/2$ to determine the bit value of the MSB, or d_1, denoted by "$C(N_a, I_{ref}/2)$". A comparator outputs a "1" if the current difference between the current held in N_a and a reference current level is positive or zero, otherwise an output of "0" is obtained. Once the bit value is determined, either the current difference $(I_{in}-I_{ref}/2)$, for $d_1=1$, or the current I_{in}, for $d_1=0$, is copied into P_a, denoted by "$N_a \& d_1(I_{ref}/2) \rightarrow P_a$". Finally, P_a sinks its copied current to N_a which holds the current to be converted for the next bit, or d_2. The remaining bits are converted in the same manner. Figure 3.22(c) shows the timing sequence for the switches necessary to implement the copying sequence listed in Figure 3.22(b). Results show that the circuit takes three clock cycles for each bit conversion. Note that the switch S_I, the NMOS copier, and the opamp form a S/H circuit. Thus, the input current is sampled and held in N_a during the first cycle of operation.

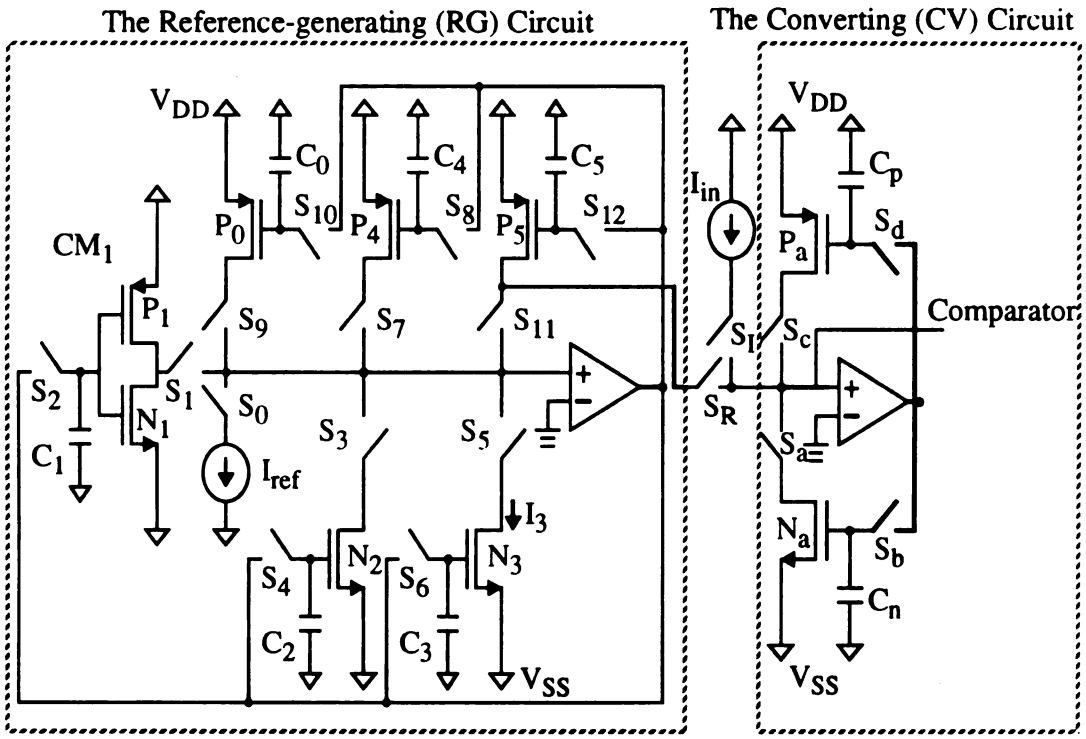
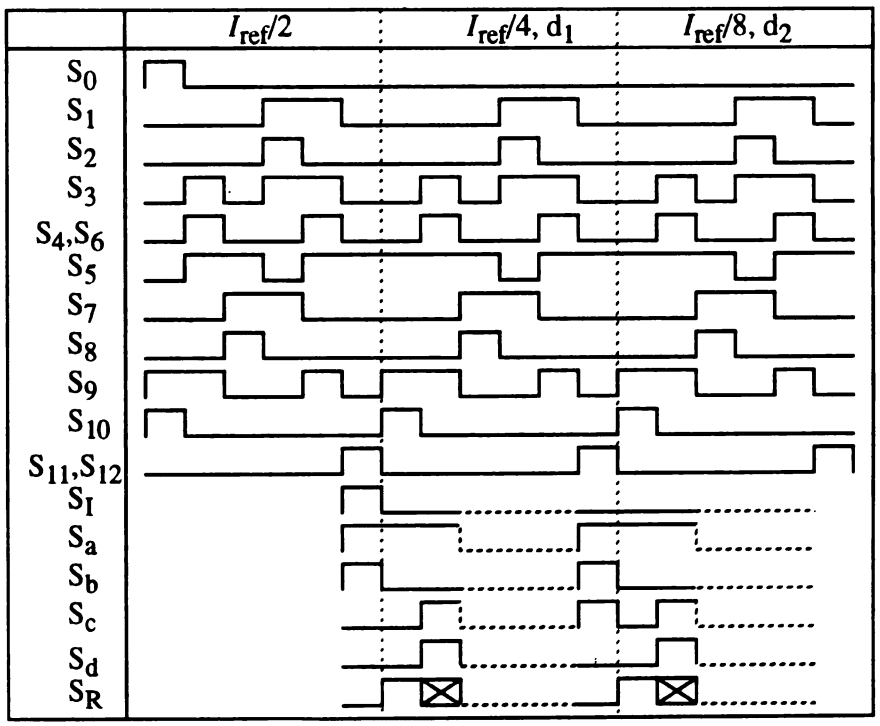


Figure 3.22 Proposed Current-mode A/D Converter: (a) Schematic Diagram; (b) Current Copying Sequence; and (c) Switching Sequence

Clock	RG Circuit	CV Circuit	P_5
1	$I_{ref} \rightarrow P_0$		
2	$P_0 \rightarrow N_2\&N_3$		
3	$N_3 \rightarrow P_4$		
4	$N_2\&P_4 \rightarrow CM_1$		
5	$P_0\&CM_1 \rightarrow N_2\&N_3$		
6	$N_3 \rightarrow P_5$	$I_{in} \rightarrow N_a$	
7	$N_3 \rightarrow P_0$	$C(N_a, I_{ref}/2)$	x
8	$P_0 \rightarrow N_2\&N_3$	$N_a\&d_1(I_{ref}/2) \rightarrow P_a$	x
9	$N_3 \rightarrow P_4$		x
10	$N_2\&P_4 \rightarrow CM_1$		x
11	$P_0\&CM_1 \rightarrow N_2\&N_3$		x
12	$N_3 \rightarrow P_5$	$P_a \rightarrow N_a$	
13	$N_3 \rightarrow P_0$	$C(N_a, I_{ref}/4)$	x
14	$P_0 \rightarrow N_2\&N_3$	$N_a\&d_1(I_{ref}/4) \rightarrow P_a$	x
15	$N_3 \rightarrow P_4$		x
16	$N_2\&P_4 \rightarrow CM_1$		x
17	$P_0\&CM_1 \rightarrow N_2\&N_3$		x
18	$N_3 \rightarrow P_5$	$P_a \rightarrow N_a$	

(b)



(c)

Figure 3.22 (Continued)

The RG circuit implements the current-mode divide-by-two circuit using the improved version of the current divider described in Section 3.3 [43]. The PMOS copiers with P_0 and P_5 are used to store each reference current level $I_{ref}/2^t$. P_0 is used as a current source for the next reference level generation, while P_5 provides the CV circuit with the current reference. The reference current is first applied to the circuit for generating $I_{ref}/2$. Then, the generated reference $I_{ref}/2$ is applied to the circuit again for generating $I_{ref}/4$, and the process is repeated to obtain the remaining reference levels.

The basic operation of the RG circuit is described as follow. First, the reference current I_{ref} is copied into P_0. The divide-by-two circuit divides it by two, where the number of iterations required for this circuit depends on the desired accuracy. At the end of the first cycle of the kth iteration, the current level $I_{ref}/2$ is generated and held in N_3. The next current level $I_{ref}/4$ is generated by copying the current held in N_3, i.e., $I_{ref}/2$, into P_0 and applying the same division process. The resultant current level is also held in N_3. The remaining current levels $I_{ref}/2^t$ are generated in the same manner.

Figure 3.22(b) illustrates the operation of the RG circuit which is as follows. First, the current reference I_{ref} is copied into P_0. The divide-by-two circuit divides the current held in P_0 by two. During the first iteration, the circuit is operated as follows: "$P_0 \rightarrow N_2 \& N_3$", "$N_3 \rightarrow P_4$", and "$N_2 \& P_4 \rightarrow CM_1$". Then, at the end of the first cycle of the second iteration, the currents held in P_0 and the bipolar copier CM_1 are copied into N_2 and N_3, where N_3 holds the desired reference current level $I_{ref}/2$. Once the current in N_3 is set, it is copied into P_5 so that the reference current level is available for the CV circuit. This completes the generation of $I_{ref}/2$. The generation of $I_{ref}/4$ is achieved by first copying the current held in N_3, i.e., $I_{ref}/2$, into P_0 and dividing the current held in P_0 by two, where the division process is the same as described above. Then, the resultant reference current level $I_{ref}/4$ held in N_3 is copied into P_5. The remaining reference current levels are generated in the same manner. Figure 3.22(b) shows that the RG circuit takes 6 cycles for generating each reference current level. Results show that the RG circuit implemented with such a divider requires two iterations for achieving an N=10 bit resolution, with a practical 1% mismatch between transistors N_2 and N_3 being assumed.

3.4.2 Analysis

Since the same circuit and its divided current are used repeatedly, the errors resulting from the reference generations may add up. The accumulated error has been formulated and used to develop the relationship among the mismatch ratio γ, the resolution bits N, and the number of iterations k [43]. The relationship of the accumulated error in terms of k is now examined . As shown in (3.9), the current held in N_3 at the end of the first cycle of the kth iteration is

$$I_{R1} = \frac{I_{ref}}{2}\left[1 + (-1)^{k-1}\left(\frac{\gamma}{2+\gamma}\right)^{k}\right] = \frac{1}{2}\left[1 + (-1)^{k-1}\left(\frac{\gamma}{2+\gamma}\right)^{k}\right] I_{ref} \qquad (3.10)$$

When the current I_{R1} is applied to the divider circuit again, the current held in N_3 becomes

$$I_{R2} = \frac{I_{R1}}{2}\left[1 + (-1)^{k-1}\left(\frac{\gamma}{2+\gamma}\right)^{k}\right] = \frac{1}{2^2}\left[1 + (-1)^{k-1}\left(\frac{\gamma}{2+\gamma}\right)^{k}\right]^{2} I_{ref} \qquad (3.11)$$

Therefore, for generating the current level $I_{ref}/2^m$, m=1, 2,.., N, the current held in N_3 can be generally expressed as follows,

$$I_{Rm} = \frac{I_{R.m-1}}{2}\left[1 + (-1)^{k-1}\left(\frac{\gamma}{2+\gamma}\right)^{k}\right] = \frac{1}{2^m}\left[1 + (-1)^{k-1}\left(\frac{\gamma}{2+\gamma}\right)^{k}\right]^{m} I_{ref} \qquad (3.12)$$

The accumulated error is estimated by considering the worst case where a string of 1's results. The input current to be converted as a string of 1's should be the sum of all reference currents $I_{ref}/2^t$ and it is expressed as

$$I_{\Sigma} = \left(\frac{I_y}{2}\right) I_{ref} + \left(\frac{I_y}{2}\right)^{2} I_{ref} + \ldots + \left(\frac{I_y}{2}\right)^{N} I_{ref} \qquad (3.13)$$

where

$$I_y = 1 + (-1)^{k-1}\left(\frac{\gamma}{2+\gamma}\right)^{k} \qquad (3.14)$$

and the accumulated error is

$$E_{\Sigma} = I_{ref}\left(\frac{I_y - 1}{2} + \frac{I_y^2 - 1}{2^2} + \ldots + \frac{I_y^N - 1}{2^N}\right) \tag{3.15}$$

For an N-bit converter, the accumulated error term E_{Σ} must be less than $1/2^{N+1}$. According to (3.15), Table 3.3 lists the relationship among γ, N, and k.

Table 3.3 Relationship among γ, k and N

γ \ k	Resolution (bits)						
	4	6	8	10	12	14	16
1%	1	2	2	2	2	3	3
2%	1	2	2	2	3	3	3
5%	2	2	2	3	3	3	3
10%	2	2	3	3	4	4	5
20%	2	3	3	4	5	5	6

For example, with 20% mismatching of transistors N_2 and N_3, the divide-by-two circuit can be used to achieve a 10-bit resolution by taking 4 iterations for generating each reference level. For the practical 1% mismatching, the circuit takes only two iterations to achieve a 10-bit resolution. Note that the operation with k iterations in this implementation includes 1 clock cycle of loading input data and 3(k-1)+1 cycles of generating half of the input currents, i.e., the operation requires (3k-1) clock cycles. Thus, the RG circuit of Figure 3.22(a) requires 5 cycles for generating the reference levels for a 10-bit conversion with 1% mismatch in N_2 and N_3.

3.4.3 Design Evaluation

The CV circuit in Figure 3.22 requires 3 clock cycles while the RG circuit requires 6 cycles for each bit conversion, and both are operated in parallel. Thus, for repetitive conversions of continuously changing inputs, the converter requires 6N clock cycles for an N-bit conversion. However, for a single conversion, the converter may need (6N+1) cycles.

In practice, however, the conversion rate can be improved by sharing the slower RG circuit. More specifically, each reference current level is available in P_5 for 5 cycles, as indicated by the "x" in Figure 3.22(b). Since the CV circuit uses the I_{ref} for only two cycles, the RG circuit is capable of driving one more CV circuit to improve the conversion rate as shown in Figure 3.23. Thus, a converter with a common RG circuit and two CV circuits requires 6N cycles to convert two input currents. Thus, for the repetitive conversions of continuously changing inputs, the average conversion time is 3N cycles.

For the general case where the divide-by-two circuit requires k iterations to achieve an N-bit resolution, the RG circuit needs 3k cycles to generate each reference current level. Since the current held on P_5 is available for (3k-1) cycles, it can provide $v = \left\lfloor \frac{3k-1}{2} \right\rfloor$ CV circuits, where $\lfloor\ \rfloor$ stands for the floor function. Thus, such a converter array requires 3kN cycles for converting v consecutive input currents, i.e., the average conversion time is 3kN/v cycles. Each conversion is done every two consecutive cycles when $I_{ref}/2^t$ is made available to the corresponding CV_i circuit. Therefore, for the 10% mismatch, the divide-by-two circuit requires 3 iterations for N=10. The converter achieves an average conversion time of 2.25N cycles. On the other hand, for a mismatch of 20%, the divide-by-two circuit requires 4 iterations for N=10. The average conversion time is 2.4N, or 24 cycles. This demonstrates that the mismatch of transistors N_2 and N_3 will not affect the average conversion time.

Note that current divider achieves a more accurate result if more iterations are taken. A larger transistor mismatch may require more cycles to achieve the desired accuracy. As a result, P_5 will hold the reference current level for more cycles and connect more CV circuits. The conversion time can be improved, but the improvement is limited by the CV circuit operation. In the next section, a parallel array structure is presented to achieve higher conversion rate.

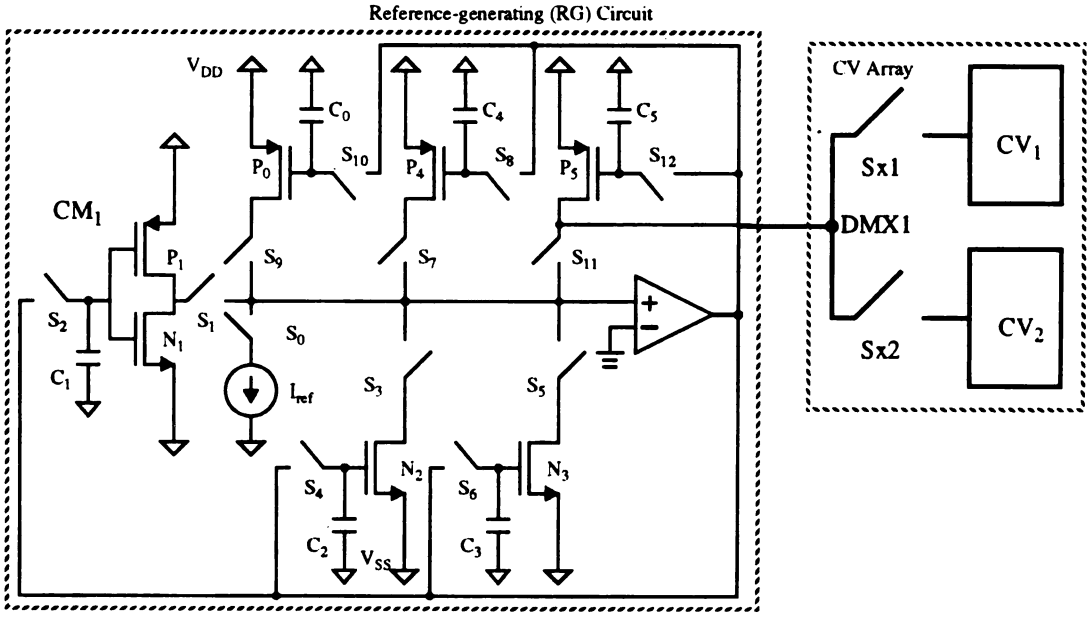


Figure 3.23 A Converter Array with two CV Circuits

3.4.4 Array Structures

In general, the CV circuit of a successive-approximation A/D converter may require only two or three cycles. Thus, the slower RG circuit may degrade the conversion rate. In practice, however, a common RG may be shared by several CVs to simultaneously convert several analog data. The implementation of the RG in an A/D converter array to achieve a higher conversion rate is discussed.

High conversion rate can be achieved by using a parallel array structure with a common RG circuit. Figure 3.24 shows an alternative RG circuit which is comprised of a current-mode divide-by-two circuit and two PMOS copiers with P_{Hi}, i=1 and 2. Similar to P_5 in Figure 3.22, P_{Hi} are used to hold the generated reference current levels for the use of the CV circuits. For the case of 1% mismatch, the divide-by-two circuit takes 5 cycles to generate the reference current level which is held in N_3. Together with two cycles for copying the current in N_3 into P_{H1} and P_{H2}, the RG circuit requires 7 cycles for each reference current generation. Since each P_{Hi} holds the current for 6 cycles, it can provide 3 CV circuits, as shown in Figure 3.24(b). Thus, the RG circuit connects to 6 CV circuits via the two analog demultiplexers (each has three switches).

Consider a general RG(m) circuit which is comprised of a current-mode divide-by-two circuit and m pairs of PMOS copiers, i.e., 2m PMOS copiers with P_{Hi}, i=1,2,..,2m. Thus, the RG circuit in Figure 3.24(a) is a RG(1) circuit. In general, a RG(m) circuit requires 5 cycles for generating each reference current level and 2m cycles for copying it to all P_{Hi}, i.e., (2m+5) cycles in total. Each P_{Hi} holds the reference current level for (2m+4) cycles and connects to (m+2) CV circuits via an analog demultiplexer. Thus, a converter consisting of a RG(m) circuit, 2m(m+2) CV circuits, and 2m demultiplexers, requires (2m+5)N cycles to convert ($2m^2$+4m) input currents. Figure 3.24(c) illustrates a converter array with a RG(2) circuit.

Since a RG(m) circuit is comprised of a divide-by-two circuit and 2m PMOS copiers, its hardware includes a bipolar copier, an opamp, two NMOS copiers, and (2m+2) PMOS copiers in total. Thus, the converter array with a RG(m) requires ($2m^2$+4m+1)

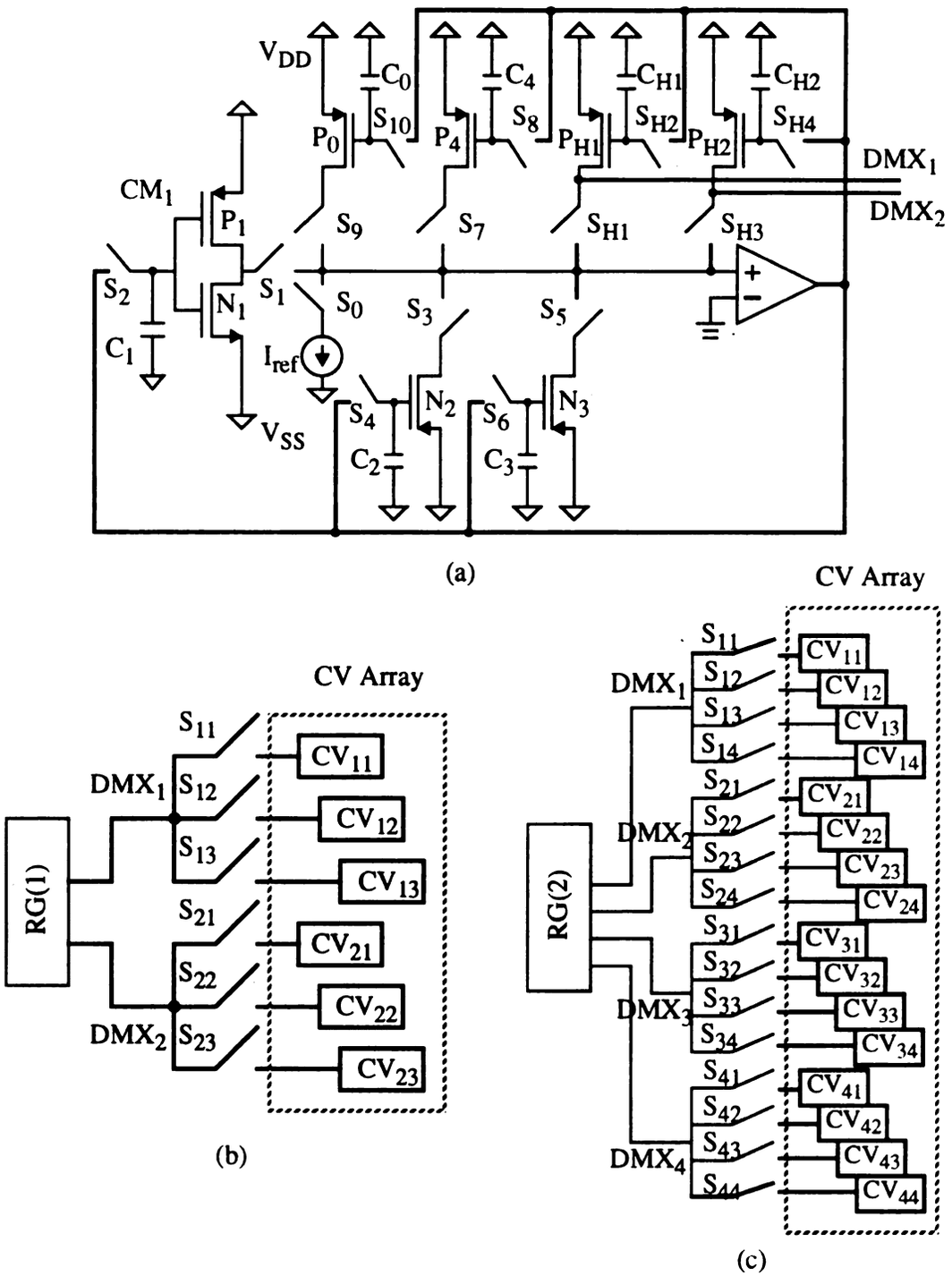


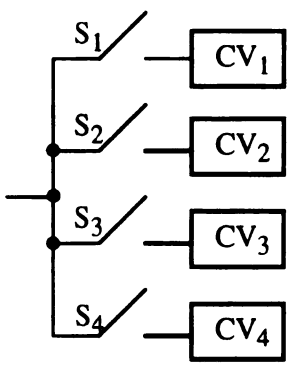
Figure 3.24 Converter Arrays (a) RG(1) Circuit; (b) RG(1) Circuit with 2-by-3 CV Array; and (c) RG(2) with 4-by-4 CV Array

opamps, $(2m^2+4m+2)$ NMOS copiers, $(2m^2+6m+2)$ PMOS copiers, $(2m^2+4m)$ comparators, $(2m^2+4m)$ switches (for demultiplexer circuits), and one bipolar copier. As, a result, the number of each type of components, except the bipolar copier, is quadratically increased with m.

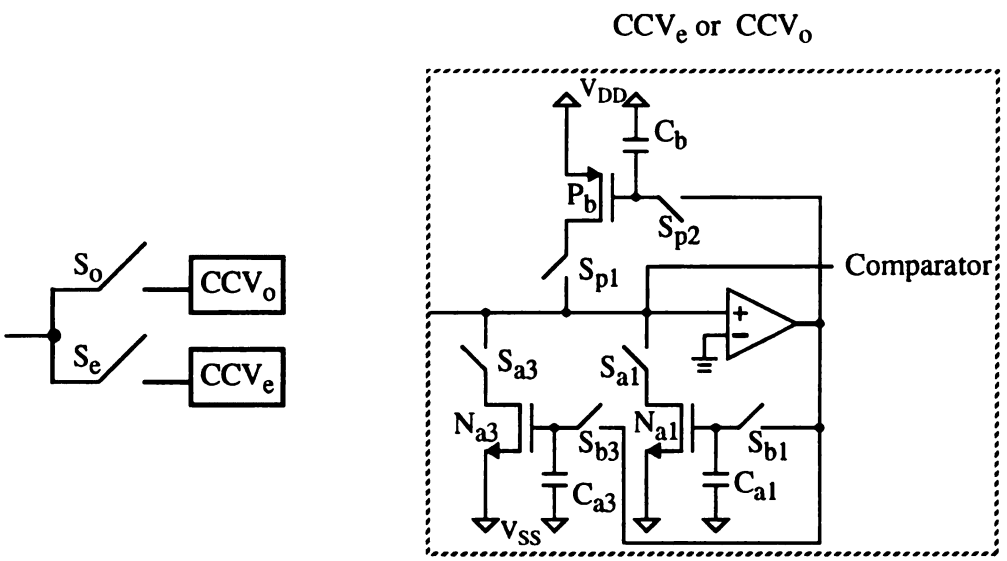
3.4.5 Hardware Reduction

Since the CV circuits are dominant in the hardware of the converter circuit with a RG(m) circuit, the hardware cost can be reduced considerably if some components in those CV circuits can be shared. Figure 3.25(a) shows a structure with four CV circuits, CV_i, i=1,2,3,4, which are connected to the P_{H1} of the RG(2) circuit via the switches S_i of the demultiplexer. The P_{H1} holds the reference current level for eight cycles, and it sinks its current to the CV_1 circuit during the first and second cycles, to the CV_2 during the third and forth cycles, to the CV_3 circuit during the fifth and sixth cycles, and to the CV_4 during the seventh and eighth cycles. Note that each CV requires only three cycles to complete its operation. This means that the CV_1 circuit completes its operation and becomes idle when the CV_3 circuit starts off its operation. Thus, the opamp and comparator in the CV_1 circuit can be shared by the CV_3 circuit. In addition, since the PMOS copier in each CV circuit is used as temporary storage while the NMOS copier stores the current to be converted, the PMOS transistor in the CV_1 circuit can also be shared by the CV_3 circuits. As a result, a circuit that combines the CV_1 and CV_3 circuits, referred to as the *combined CV circuit*, or denoted as CCV_o, is shown in Figure 3.25(b). Similarly, a circuit combining the CV_2 and CV_4 circuits, referred to as CCV_e, has the same structure.

For a converter array with a RG(m) circuit, each P_{Hi} connects to a CCV_o circuit and a CCV_e circuit, where the CCV_o circuit combines $\lceil (m+2)/2 \rceil$ CV circuits and the CCV_e circuit includes the remaining $\lfloor (m+2)/2 \rfloor$ circuits, where $\lceil\ \rceil$ stands for the ceiling function and $\lfloor\ \rfloor$ stands for the floor function. The CCV_o (CCV_e) circuit is comprised of $\lceil (m+2)/2 \rceil$ ($\lfloor (m+2)/2 \rfloor$) NMOS copiers, one PMOS copier, one opamp, and one comparator. In addition, the CCV_o and CCV_e circuits are connected to the RG(m) circuit via switches S_o



(a)



(b)

Figure 3.25 Hardware Reduction (a) An Array with 4 CV Circuits; and (b) Combined CV (CCV) Circuits: CCV_o and CCV_e

and S_e, respectively. Thus, the array structure requires a RG(m) circuit, 2m CCV_0 circuits, 2m CCV_e circuits, and 4m switches, i.e., it requires (4m+1) opamps, (6m+2) PMOS copiers, 4m comparators, 4m switches, ($2m^2$+4m+2) NMOS copiers, and one bipolar copier in total. Consequently, the numbers of opamps, PMOS copiers, comparators, and switches are linearly proportional to m, instead of m^2. Thus, the chip area is reduced considerably.

3.4.6 Implementation

Since the basic circuit components of the converter array structures and their operations are similar to the successive-approximation current-mode A/D converter reported in [13] in which its prototype circuit has been fabricated using 3μm CMOS technology. The circuit achieves a resolution of 10 bits with a maximal sample rate of 25 KHz, or 40 μsec conversion time. Since the converter requires 4N clock cycles for an N-bit data word, this implies that a cycle of 1 μsec is sufficient to stabilize the circuit operation. The fabrication data reported in [13] may be used to assess the performance of the converter array structures. Based on the experimental data in [13], the converter with RG(m), where m=10, for example, requires (2m+5)N, or 250 cycles, or 250 μsec, or 4 Kframes/sec, for a 12-by-20 sensor array with a 10-bit resolution. Its hardware includes 41 opamps, 62 PMOS copiers, 40 comparators, 40 switches, one bipolar copier, and 242 NMOS copiers. Note that the converter in [13], consisting of 3 MOS copiers, an opamp, two switches, and a comparator, takes only 0.6x0.2mm, or $0.18mm^2$. Thus, it is predictable that the converter requires a reasonably small chip area which is well suited for use in smart sensor array designs.

It is obvious that the sample rate of the converter array can be increased as m is increased. However, it should be mentioned that the reference current in each P_{Hi} of the RG(m) circuit must be held for (2m+4) cycles. As m increases, larger capacitors may be needed so that the copier can accurately hold the reference current level. Although larger capacitors may reduce the effects of the thermal noise and charge injection from the switches, they lead to slower settling time. The dilemma is that, as m increases, the

conversion rate increases, but the settling time may decrease. Thus, a point will eventually be reached where an optimal conversion rate, i.e., an optimal value of m, is obtained.

3.5 Summary

In this chapter, several new current-mode signal processing circuits have been presented. A bipolar copier with its bidirectional copying capability is an essential element in general purpose multipliers and dividers. In analog fault diagnosis with current data, a malfunction in a circuit may cause currents to be of any polarity. The CMOS bipolar copier can be an important part of fault diagnosis systems and can be used to load current test data.

The current-mode shift register can be used to load sensory information for signal processing of sensor arrays and arranged to exploit the parallelism of an array structure. The study of the shift-register structure also indicates that it can be easily adapted to obtain an analog BIST design for current test data. A highly accurate current divider that does not require matched components or external adjustments has also been developed and successfully implemented as a reference-generating unit of a successive-approximation A/D converter. Section 3.4 presents a successive-approximation A/D converter that uses a divide-by-two scheme, thus avoiding the accumulation of error and noise that can be associated with the multiply-by-two methods. In order to improve the conversion rate that can be degraded due to a slow reference generation, array structures have been described. These current-mode A/D converter arrays contain subconverters that do not rely on high gain amplifiers or well-matched components to achieve high resolution and are inherently insensitive to the amplifier's offset voltage. These arrays utilize the inherent idleness of several operational blocks to execute the conversions in parallel at very low hardware cost.

Even though these structures are successful in function, during real-time operations it is difficult to achieve data validation of these circuits. Thus, the reliability of the current-mode signal processing circuits and their data has to be ensured and so the diagnosable design of current-mode data-acquisition and data-conversion circuits has to be addressed.

Chapter 4

Testable Current-mode Circuits

A/D and D/A converters are the main link between the analog world of signals and digital systems that control and monitor electronic applications. The properties of the converters used for such systems are important and reliability is one of the crucial elements in their make-up. During real-time operations, a system failure could have fatal results. Consequences of such failures stress the importance of converter reliability and reliability of electronic circuits in general.

The objective of this chapter is to present schemes to improve the testability and reliability of current-mode data-acquisition and conversion circuits. In order to enhance the reliability of A/D converters for real-time operations, an alternative current-mode A/D converter with CED capability is described in Section 4.1 to detect transient and permanent faults [44-46]. Further, the fault effects and test generation of the current-mode A/D converter proposed in [13] is presented. Based on the single stuck-at fault model for the switching elements, the converter can achieve full testability with the application of two test currents. In the past, analog circuit fault diagnosis algorithms that have been developed are restricted for use only on small-scale networks due to the limited number of available test points. Section 4.2 presents analog BIST structures using voltage test data and current test data which can be used to make fault diagnosis and testing of analog circuits much simpler.

4.1 Testable Current-mode A/D Converter

In this section, a diagnosable current-mode A/D converter with CED capability is presented and thus it can achieve data validation for real-time applications [44]. Due to the continuum nature of analog circuits, it is extremely difficult to generate a finite and complete set of test vectors. Exhaustive tests are impossible even though the number of inputs of an analog circuit may be reasonably small, and so analog circuits become very difficult to test. This section addresses the fault effects and test generation of an algorithmic current-mode A/D converter, and the design achieves full testability with the application of only two test currents [44]. Thus, a test set of only two vectors is all that is necessary for 100% fault detection.

4.1.1 Concurrent Error Detection

Figure 4.1 illustrates a CED scheme with the AL implementation. First, the input current $I_{t1}=I_{in}$ is converted during the first time step (or, normal operation phase) and the resulting digital data word is stored in a digital shift register. Then, the complemented current $I_{t2}=I_{ref}-I_{in}$ is converted during the second time step (or, recomputing phase). The digital data words resulting from both phases are compared to identify an error, if it exists. If the converter is fault-free, the converted data resulting from both phases must be bitwise complements of each other. For example, with the reference current of I_{ref}=100μA, the input current 27μA and its complement 73μA are converted to the 10-bit data word D_1=(0100010100) and D_2=(1011101011), respectively, where both D_1 and D_2 are bitwise complements. Since the comparison is in a digital manner, a *totally self-checking (TSC) checker* can be used to identify the error and also to ensure the correctness of the checker circuit. Therefore, a reliably converted data word can be attained.

Figure 4.2 shows the current-mode A/D converter with the CED capability. The input current I_{in} is sampled only once and the current is stored in P_1. In order to store the current $(I_{ref}-I_{in})$, an additional PMOS current copier is needed to hold the current at the

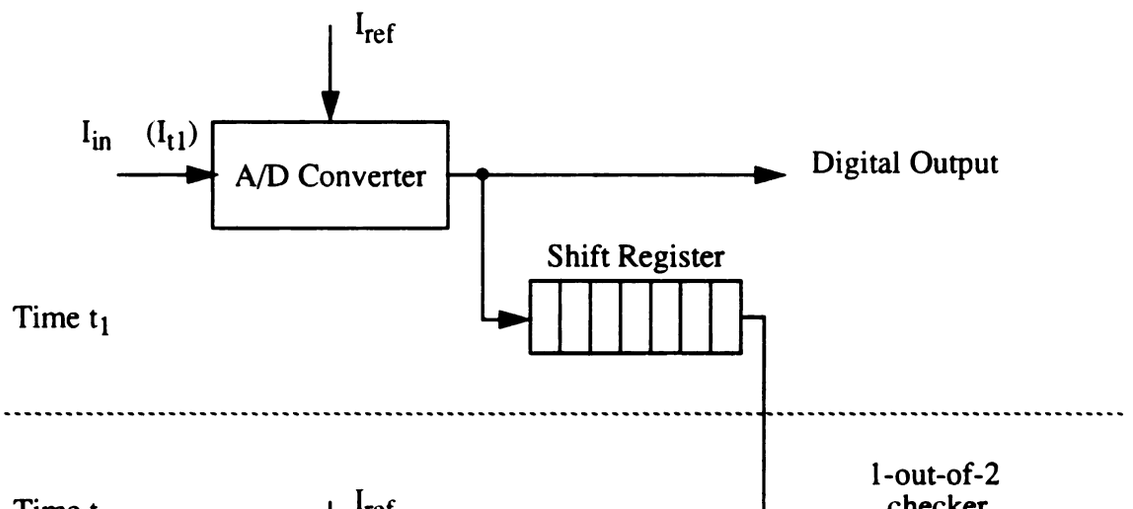
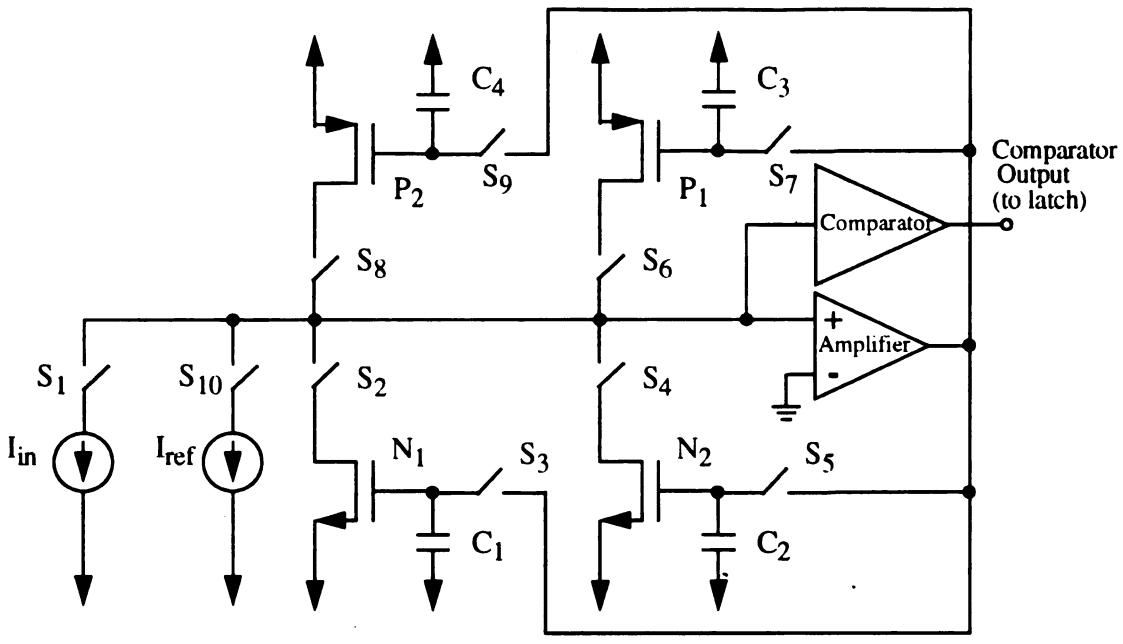


Figure 4.1 CED Structure with AL Implementation



(a)

	Current S/H	NORMAL OPERATION PHASE			RECOMPUTATION PHASE		
		MSB	Previous bit = 1	Previous bit = 0	MSB	Previous bit = 1	Previous bit = 0
S_1							
S_2							
S_3							
S_4							
S_5							
S_6							
S_7							
S_8							
S_9							
S_{10}							

(b)

Figure 4.2 Proposed Current-mode A/D converter with CED Design:
(a) Schematic Diagram; and (b) Switching Sequence

beginning of the data-conversion. The input current I_{in} is copied and stored in P_1 by turning on Switches S_1, S_6, and S_7, while the current difference (I_{ref}-I_{in}) is loaded to P_2 by turning off S_1 and S_7 and turning on S_8, S_9, and S_{10}. Once both currents are stored, the current held in P_1 and the current held in P_2 are converted. The results from both conversions are compared to identify an error, if it exists. The data-conversion process is exactly the same as presented previously. Figure 4.2 (b) illustrates the switching sequence.

4.1.1.1 Fault Models

Since the current-mode A/D converter implements a ratio-independent algorithm for conversion, any mismatched components do not affect the converted data. However, any faulty switching element may result in incorrect operation and thereby erroneously converted data. The single stuck-at fault model has been commonly employed for digital test generation. In this implementation, it is assumed that only one faulty switch occurs at a time and the faulty switch is permanently or temporarily stuck-at ON state (*S/ON*) or OFF state (*S/OFF*). In general, the faults may be caused by either an erroneous clock generator where the timing control signal may be permanently stuck-at-1 (or 0) causing the controlled switch to be *S/ON* (or *S/OFF*). These faults can also be the result of malfunctioning transistor switches.

Temporary faults, or transient faults are such that the duration of fault behavior is sufficiently short. Transient faults have been very common in today's digital VLSI design. Since all switches in the A/D converter are controlled by the digital clock signals, a signal may temporarily change its value from 0 to 1 or from 1 to 0 and cause the switching elements to temporarily malfunction. For permanent faults, the duration of the fault behavior is sufficiently long. In general, the permanent faults may be caused by either an erroneous clock generator where the timing control signal may be permanently stuck-at-1 (or 0) causing the controlled switch to be S/ON (or S/OFF), or by malfunctioning transistor switches. For a reliable circuit design, the permanently faulty switches can be tested by an

off-line test process. The chance that permanent faults occur during the normal operation is rare. However, the design can still detect most of the permanently faulty switches.

4.1.1.2 Fault Coverage

In general, the duration of a transient fault is sufficiently short. It is most likely shorter than the conversion time for the converter, i.e., 4N clock cycles. Here, a fault may occur during the first time step, or during the second time step, or overlap in both time steps (but the duration is shorter than 4N). If the fault occurs only during the first time step, i.e., the fault disappears during the second time step, then the converted data word D_2 is reliable and can be used to check D_1 for identifying an error, if it exists. Thus, the fault is detectable. Similarly, the fault that occurs only during the second time step is also detectable. Now, if the fault occurs after the rth bit of D_1 is being converted and disappears after the (r-1)th of the D_2, for any integer r, then at least the first (r-1) bits of D_1 are reliable and can be used to identify the fault. Thus, the fault is detectable and the design can detect all transient faults.

If the duration of fault behavior is longer than the time required to complete the first time step and the second time step, all time redundancy CED schemes will no longer possess the property of disjoint error sets, and the errors, thus, cannot be detected. This implies that not all permanent faults are detectable. It would be preferable for the circuits to be designed so that they will indicate malfunction during normal operation and will not produce an erroneous result without an error indication. In these circuits, any failures will cause a detectable erroneous output during normal operation, and each fault must not cause an erroneous output without also producing an error signal. The circuits that possess this property are referred to as *fault secure* circuits.

The errors resulting from these faulty switches can be categorized into four types. The errors that can be definitely detected by the CED scheme are referred to as *Type 1 errors*, i.e., a Type 1 error causes $D_1 \neq \overline{D}_2$ for all possible input currents. The errors that cannot be detected are referred to as *Type 2 errors*, i.e., a Type 2 error causes $D_1 = \overline{D}_2$ for all possible input currents. In some cases $D_1 \neq \overline{D}_2$ for all possible input currents except a

few. For these few where $D_1=\overline{D}_2$, if the resulting data word D_1 is reliable even in the presence of fault(s), then the circuit is fault secure and such an error is referred to as *Type 3 error*. On the other hand, if the resulting data word D_1 is not reliable in the presence of fault(s), then the fault cannot be detected for the application of such input currents and this error is referred to as *Type 4 error*.

A. Type 1 Errors

Type 1 error causes $D_1\neq\overline{D}_2$ for all possible input currents. These errors are definitely detected by the CED scheme. Such errors are the results of S/ON faults at S_2, S_3, S_4, and S_5 and S/OFF faults at S_2 and S_4. Table 4.1 lists the faults and fault effects of Type 1 errors.

Consider a S/OFF faulty switch S_2. During the first time step, for the fault-free circuit, the input current I_{in} held in P_1 is copied to both N_1 and N_2, and then the sum current $2I_{in}$ is copied back to P_1. However, because of the faulty switch N_1 cannot sink any current held in P_1. This is equivalent to a zero current being held in N_1. Thus, only the I_{in} held in N_2 is copied back to P_1, i.e., P_1 holds I_{in} in each bit conversion. This results in D_1=(00..0) regardless of converting any input current. During the second time step, the conversion of the complemented current I_{ref}-I_{in}, the resulting data word D_2=(00..0), i.e., $D_1\neq\overline{D}_2$ for all possible input currents. Thus, this is a Type 1 error. Since the S/OFF fault of switch S_4 and the S/ON faults of switches S_2 and S_4 have the same fault effect, thus these faults are all detectable, i.e., the errors are all Type 1 errors.

For the S/ON faulty switch S_3, during the first time step, the currents I_{in} and (I_{ref}-I_{in}) are respectively held in P_1 and P_2. When the current held in P_1 is converted, the current is first copied to N_1 and then to N_2. Now, when the current is copied to N_2, the fault causes the gate-source voltages of both N_1 and N_2 to be the same. If both N_1 and N_2 are well-matched, the currents held in both N_1 and N_2 will be the same. However, if both N_1 and N_2 are mismatched, the current held in N_1 is overwritten. When the currents held in N_1 and N_2 are copied back to P1, due to the S/ON faulty switch S_3, the operation is equivalent to copying the current held in N_2 to a CMOS current copier consisting of PMOS P_1 and

NMOS N_1. The experimental results have shown that D_1=(00..0) and D_2=(10..0) for a sufficiently low input I_{in}; D_1=(10..0) and D_2=(00..0) for a sufficiently high input I_{in}; and D_1=(00..010..0) and D_2=(00..010..0) for the others. Obviously, the error can be detected for either case. Thus, it is a Type 1 errors. Similarly, the S/ON fault of S_5 has the same fault effect as that of S_3.

Table 4.1: Type 1 Errors

Fault	Analysis	Fault Effects
S_2 (S_4) S/OFF	Zero current held in N_1 (N_2). Current not doubled.	D_1=D_2=(00...00)
S_2 (S_4) S/ON	N_1 (N_2) cancels current from P_1 or P_2. N_2 (N_1) holds zero current. Current not doubled.	D_1=D_2=(00...00)
S_3 (S_5) S/ON	Output depends on the CMOS structure P_1/N_1 (P_1/N_2).	One bit of D_1 equals the respective of D_2.

B. Type 2 Errors

Type 2 errors cause $D_1=\overline{D}_2$ for all possible input currents. These errors are caused by either not reading the input current (S/OFF fault at S_1), or not reading the reference current (S/OFF fault at S_{10}), or the equivalent fault effects (S/OFF fault at S_6 and S/ON fault at S_{10}), as shown in Table 4.2. In general, these errors are not detectable by the CED scheme.

For example, a S/OFF fault at S_1 implies that a zero current is copied to P_1 and thus I_{ref} is copied to P_2. Thus, D_1=(00..0) and D_2=(11..1), i.e., $D_1=\overline{D}_2$ for all possible input currents. Such a Type 2 error is definitely undetectable. Similarly, the S/OFF faults of switch S_6 has the same fault effect as above and the errors are also of Type 2.

Consider a S/OFF fault at S_{10}. The fault is equivalent to the A/D converter using a zero reference current. First, the input current I_{in} is copied to P_1. Then, P_2 was expected to source a current equal to (I_{ref}-I_{in}). However, the zero reference current results in a negative current, -I_{in}, being copied to P_2 and causes a breakdown in transistor P_2. Since, during the

first time step, P_1 holds the current I_{in} and the reference current I_{ref}=0, the resultant data word D_1=(11..1). On the other hand, the breakdown of transistor P_2 may result in D_2=(00..0). Thus, $D_1=\overline{D}_2$ for all possible input currents and it is a Type 2 error. Similarly, a S/ON fault at S_{10} has the same fault effect. Thus, it is also a Type 2 error.

Table 4.2: Type 2 Errors

Fault	Analysis	Fault Effects
S_1 S/OFF	Equivalent to I_{in}=0. P_1 holds zero and P_2 holds I_{ref}.	$D_1=\overline{D}_2$=(00...00)
S_6 S/OFF	P_1 never copies current. P_2 holds I_{ref}.	$D_1=\overline{D}_2$=(00...00)
S_{10} S/OFF	Equivalent to I_{ref}=0. $-I_{in}$ forced into P_2	$D_1=\overline{D}_2$=(11...11.)
S_{10} S/ON	I_{ref} always added to the current copied into P_1. $-I_{in}$ forced into P_2	$D_1=\overline{D}_2$=(11...11.)

C. Type 3 Errors

In some cases $D_1\neq\overline{D}_2$ for all possible input currents except a few. For these few where $D_1=\overline{D}_2$, if the resulting data word D_1 is reliable even in the presence of fault(s), then the circuit is *fault secure* and such an error is referred to as *Type 3 error*. Table 4.3 illustrates the fault effects of Type 3 errors. The faults include S/ON faults at S_6, S_7, S_8, and S_9; S/OFF faults at S_8 and S_9.

Consider a S/ON fault at S_6. According to the switching sequence shown in Figure 6(b), S_6 is on for the entire conversion cycle during the first time step. Thus, the resultant data word is still correct even in the presence of such a fault. On the other hand, at the end of the first time step, the current held in P_1 is I_x, where I_x is less than 1 LSB if the last bit of D_1 is 1; otherwise I_x is greater than 1 LSB. Due to the faulty switch S_6, the current, I_x, held in P_1 is always available during the second time step. This is equivalent to converting the sum of I_x and the current held in P_2 for each bit conversion. If $D_1\neq\overline{D}_2$, then the checker

will indicate an error. On the other hand, if $D_1=\overline{D}_2$, the converted data word D_1 is reliable. Thus, the circuit is fault secure and the error is of Type 3.

Similarly, a S/OFF fault that occurs at S_8 or S_9 and a S/ON fault at S_9 does not affect the conversion in the first time step, i.e., D_1 is reliable. However, the S/OFF faulty switches S_8 and S_9 results in D_2=(00..0), while the S/ON faulty switches S_9 may cause P_2 to source a random current. Thus, the circuit is fault secure in the presence of such fault(s) and the error is of Type 3. In the same manner, a S/ON faulty switch S_8 results in D_1=(11..1) for all possible input currents, but provides a reliable data word D_2. If there exists, at least, one 1-bit in D_2, the comparison will identify an error. On the other hand, if D_2=(00..0), then D_1 provides a reliable result. Thus, the circuit is also fault secure in the presence of such a fault.

Table 4.3: Type 3 Errors

Fault	Analysis	Fault Effects
S_6 S/ON	Normal operation phase not altered. Residual current in P_1 always sourced during recomputation phase.	D_1: correct D_2: random
S_7 S/ON	During comparison P_1 initially copies I_{ref} and then gets compared. Recomputation phase always converts approximately $I_{ref}/2$.	D_1=(11...11) D_2: approximately the digital output of $I_{ref}/2$
S_8 S/ON	Residual current in P_2 always sourced during normal operation phase. Recomputation phase not altered.	D_1: random D_2: correct
S_9 S/ON	Normal operation phase not altered. During comparison P_2 initially copies I_{ref} and then gets compared.	D_1: correct D_2=(11...11)
S_8 S/OFF	Normal operation phase not altered. P_2 never copies current.	D_1: correct D_2=(00...00)
S_9 S/OFF	Normal operation phase not altered. Residual current in P_2 always compared with I_{ref}.	D_1: correct D_2: random

Consider the S/ON faulty switch S_7. The fault causes the current held in P_1 to be changed whenever the opamp is in use. For example, after the input current I_{in} is loaded to P_1, the current (I_{ref}-I_{in}) is copied to P_2. The faulty switch S_7 will cause the gate-source voltage of P_1 to be changed as the same as that of P_2 and, thus, changing the current held in P_1. In addition, when the current held in P_1 is compared to the reference current I_{ref} to determine the converted bit value, the faulty switch S_7 causes the current held in P_1 to be I_{ref} and, thus, a "1" results. This implies that D_1=(11..11). Since the fault does not affect the conversion of the current held in P_2, hence, the converted data word D_2 is reliable. Similar to the above discussion, this is a Type 3 error.

D. Type 4 Errors

If the resulting data word D_1 is not reliable in the presence of fault(s), then the fault cannot be detected for the application of such input currents and this error is referred to as *Type 4 error*. The fault effects of such error types are listed in Table 4.4. The faults include S/ON fault at S_1; S/OFF faults at S_3, S_5, and S_7.

Consider the S/ON faulty switch S_1. It is assumed that the input current will be varying for real-time applications. The fault implies that the data is converted in the environment where the noise is equivalent to the varied input currents. Thus, D_1 and D_2 can be any random results. Statistically speaking, the probability of having two random data words D_1 and D_2 as complements to each other is very low. Thus, this is a Type 4 error.

Due to the S/OFF faulty switch S_7, the current copier with P_1 cannot copy any current. Thus, the current, I_x, held in P_1 is the one remaining from the previous operation. This results in D_1=(00..0) if $I_x < I_{ref}$, or D_1=(11..1) otherwise. Since P_1 can still source the current I_x, the current held in P_2 is (I_{ref}-I_x) and the resultant data word D_2 is reliable. Therefore, $D_1=\overline{D}_2$ only if *either* I_x or (I_{ref}-I_x) is less than 1 LSB, $D_1 \neq \overline{D}_2$ otherwise. This is a Type 4 error. Similarly, the S/OFF faulty switch S_3 causes the current copier with N_1 not to copy any current. Assume that the current held in N_1 is I_x. Experimental results have shown that $D_1=\overline{D}_2$ only if I_x is very close to $I_{ref}/2$, and $D_1 \neq \overline{D}_2$, otherwise. For a reliable design, the chance that the fault occurs when the current held in N_1 is $I_{ref}/2$ is rare. Due to

the analog nature, this error is of Type 4. Since the fault of S/OFF switch S_5 has the same fault effect as S_3, the error is also a Type 4.

Table 4.4: Type 4 Errors

Fault	Analysis	Fault Effects
S_1 S/ON	Varying I_{in} always sourced to the circuit.	D_1 & D_2: random
S_3 (S_5) S/OFF	N_1 (N_2) do not copy any current but its residual current is sourced.	D_1 & D_2: random
S_7 S/OFF	Residual current in P_1 always compared with I_{ref}. Recomputation phase converts the complement of this residual current.	D_1 & D_2: random

Based on the above discussion, Table 4.5 summarizes the status of error detection of the A/D converter with CED capability. There exist eight Type 1 errors, four Type 2 errors, five Type 3 errors, and three Type 4 errors. If the fault coverage is defined as the total number of Types 1, 3, and 4 errors over all possible errors, the fault coverage of permanent faults is 80%.

Table 4.5: Error Detection

Switches	S/ON	S/OFF
	Type	Type
S_1	4	2
S_2	1	1
S_3	1	4
S_4	1	1
S_5	1	4
S_6	3	2
S_7	3	4
S_8	3	3
S_9	3	3
S_{10}	2	2

4.1.2 Test Generation

For the A/D converter in [13], the input current is needed during the first two clock periods of the conversion cycle, a sample-and-hold (S/H) circuit is, thus, required for the input current. In practice however, the S/H circuit may be omitted by holding the input I_{in} in P_1, where the polarity of the input current is changed as shown in Figure 4.3. The sampled current is held in P_1 by turning on switches S_1, S_6, and S_7 to cause the current in P_1 to be set to I_{in}. Once P_1 is set, the remaining switching sequences are the same as those in Figure 2.9. In other words, the converter needs 5 cycles to determine the MSB. Therefore, there exists a trade-off between hardware (a sample-and-hold circuit) and speed (an additional cycle).

4.1.2.1 Fault Model and Fault Effects

Although mismatched components are allowed in the converter of Figure 2.9, the converter is still susceptible to faulty switching elements which cause incorrect operation of the converter. A single stuck-at fault model is assumed where only one switch is faulty at a time and it is permanently stuck-at ON state (*S/ON*) or OFF state (*S/OFF*). The cause of these faults could be malfunctioning clock generators or transistor switches.

The analysis of the faulty switches in the converter of Figure 4.3 revealed that the fault effects can be classified into three types: Type 1 fault effect occurs when the faulty switch results in the same conversion output regardless of the values of the input current. Switches S_1, S_2, S_4, S_7, and S_{10} being *S/ON* and S_1, S_2, S_4, S_6, and S_{10} being *S/OFF* illustrate this fault behavior; Type 2 occurs when the faulty switch renders the conversion output dependent on the initial condition of the active capacitors. Switches S_3, S_5, S_7 lead to this condition when *S/OFF*; and Type 3 faults make the result of the conversion process dependent on the CMOS structure P_1/N_1 (or P_1/N_2) when S_3 (or S_5) is being *S/ON*. Throughout the next analysis, I_{P1} (I_{N1}, or I_{N2}) will denote the current held in P_1 (N_1, or N_2).

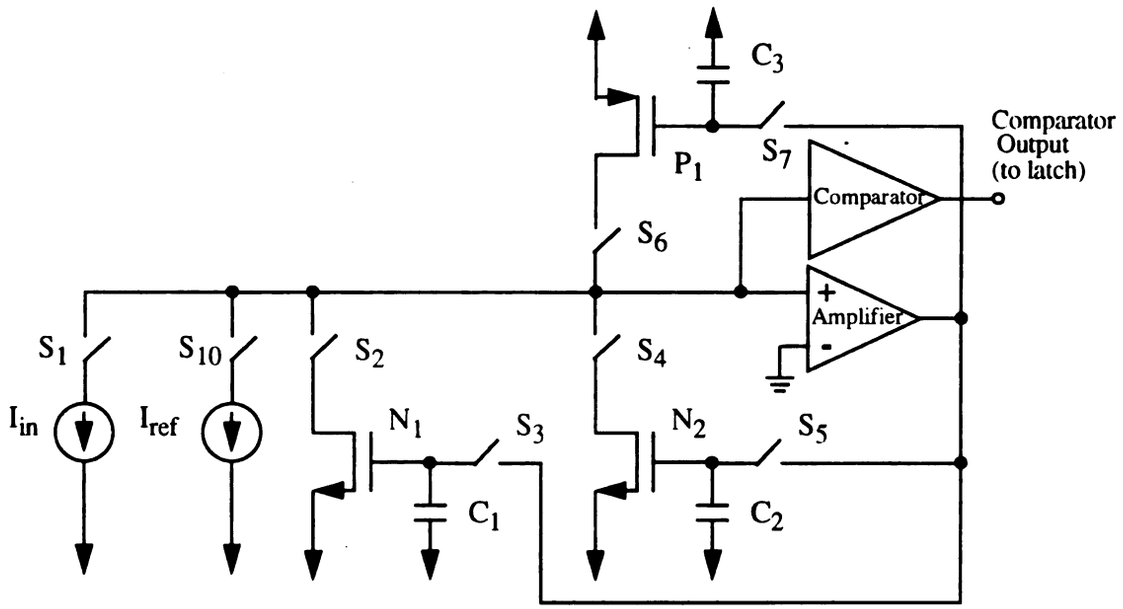


Figure 4.3 Modified Current-mode A/D Converter

A. Type 1 Fault Effect

Consider the case when S_1 or S_6 is *S/OFF*, the input current will not be copied into P_1; this is effectively equivalent to an input current of zero. Consequently, the conversion process results in a string of zeros. When S_2 (S_4) is *S/OFF*, the input current in P_1 will never be doubled. In fact, S_2 (S_4) being open circuited results in N_1 (N_2) contributing zero current to P_1 during the copying of the sum current $I_{N1}+I_{N2}$. Hence the comparison of current in P_1, i.e., I_{in}, and I_{ref} always results in a zero bit. S_{10} being *S/OFF* leads to the current in P_1 being compared to zero instead of I_{ref}. Hence conversion results in a string of ones. When S_1 is *S/ON*, P_1 gets the input current; however when P_1 is being copied into N_1 (N_2), N_1 (N_2) gets the difference current $(I_{P1}-I_{in})=0$. The comparison of I_{P1} $(=I_{N1}+I_{N2}+I_{in})$ and I_{ref} produces a zero MSB. Next, instead of P_1 being copied into N_1, the zero current difference $(I_{P1}-I_{in})$ is copied into N_1. Hence conversion results in a string of zeros.

At the end of every conversion, the capacitors are left charged. This charge represents the last current that has been copied into the corresponding transistor. Since N_1 and N_2 copy either the current I_{P1}, when $I_{P1} < I_{ref}$, or the current difference $(I_{P1}-I_{ref})$, when $I_{P1} > I_{ref}$, the current in the corresponding NMOS, at any instant, is bounded between zero and I_{ref}. If S_2 is *S/ON*, both the initial current I_{N1} and the input current I_{in} will be copied to P_1, i.e., P_1 gets $I_{in}+I_{N1}$. Then P_1 is successfully copied into N_1. However, when P_1 is being copied into N_2, the current in N_1 is subtracted from it resulting in copying zero current into N_2. Hence the current in P_1, will not be doubled. During the comparison phase, the comparator senses the current imbalance, $-I_{ref}$, from P_1, N_1, and I_{ref}. Thus, a zero bit always results. Similarly, when S_4 is *S/ON*, a string of zeros is resulted.

While comparing P_1 and I_{ref} with S_7 being *S/ON*, P_1 will first copy I_{ref} due to S_7 being ON. At the end of the comparison cycle, the difference between $I_{P1}=I_{ref}$ and I_{ref} will be compared leading to a conversion bit of 1. This scenario is repeated for all conversion bits. Thus, a string of ones results.

B. Type 2 Fault Effect

When S_3 is *S/OFF*, the transistor N_1 cannot copy any current because the capacitor C_1 has no charging path. Thus, N_1 will retain the current it has copied prior to the

occurrence of the fault. This current will be held constant since the capacitor can only leak its charge through the gate to source impedance. In the presence of such a fault, conversion proceeds as follows: I_{in} is copied into P_1; P_1 copy to N_1, but N_1 still holds the constant current I_x; P_1 is copied to N_2; P_1 gets $I_{N1}+I_{N2}$, or I_x+I_{in}; finally, the current held in P_1 is compared to I_{ref} and the proper conversion bit results. Similarly, the *S/OFF* faulty switch S_5 has the same fault effect. When S_7 is *S/OFF*, the transistor P_1 cannot copy any current. Thus, the constant current in P_1 is compared to I_{ref} for the output.

C. Type 3 Fault Effect

In the presence of *S/ON* faulty switch S_3, conversion starts off with successfully copying I_{in} into P_1; P_1 into N_1, and P_1 into N_2. Then, instead of copying $I_{N1}+I_{N2}$ into P_1, N_2 will source its current I_{in} to the CMOS structure, comprised of P_1 and N_1, due to S_3 being *S/ON*. Similarly, the *S/ON* faulty switch S_5 has the same fault effect.

4.1.2.2 Test Generation and Fault Coverage

According to the fault effects discussed previously, in the presence of a Type 1 fault, i.e., *S/ON* faulty switch S_1, S_2, or S_4, or *S/OFF* faulty switch S_1, S_2, S_4, or S_6, conversion results in a string of zeros. Thus, any nonzero input current can detect such a fault. Similarly, in the presence of *S/ON* faulty switch S_{10} or *S/OFF* faulty switches S_7 or S_{10}, conversion results in a string of ones. Thus, a zero test current can detect the fault.

For Type 2 fault effect, in the presence of *S/OFF* faulty switch S_3, the current held in P_1 is equal to $I_{in}+I_x$, where I_x is a constant current held in N_1. Thus, two test currents, $I_{in}=0$ and I_{ref}, can detect such a fault. More specifically, for $I_{in}=0$, during the MSB conversion, the comparison of I_{P1} ($=I_{in}+I_x=I_x$) and I_{ref} generates a zero MSB except when $I_x=I_{ref}$. During the kth bit conversion, $I_{P1}=kI_x$ generates a zero bit except for $I_x \geq I_{ref}/k$. Hence the conversion of $I_{in}=0$ generates at least one nonzero bit in the kth bit position. The result of conversion follows the general patterns of 0...1xxx, and the first nonzero bit detects the fault. On the other hand, for $I_{in}= I_{ref}$, the comparison of I_{P1} ($=I_{in}+I_x= I_{ref}+I_x$)

and I_{ref} leads to an MSB of 1. The kth comparison involving $I_{P1}=kI_x$ and I_{ref} produces a one bit except $I_x \leq I_{ref}/k$. Hence the result of conversion follows the patterns 1..0xxx and the first occurrence of a zero bit detects the fault. This concludes that these two test currents can detect the fault regardless of the value of I_x. Similarly, these two test currents can detect the *S/OFF* fault on switch S5. Consider the presence of *S/OFF* faulty switch S_7, the fault effect shows that the constant current I_y held in P_1 is bounded between 0 and 2 I_{ref}. Thus, the above two test currents can also detect the fault. More specifically, $I_{in}=0$ and $I_{in}= I_{ref}$ detect the fault in cases $I_y < I_{ref}$ and $I_y \geq I_{ref}$, respectively.

For Type 3 fault effect, in the presence of *S/ON* faulty switch S_3, the transistor N_2 will source its current I_{in} to the (P_1/N_1) CMOS structure. This results in I_{P1}-I_{N1}=I_{N2}=I_{in}, where the values of I_{P1} and I_{N1} depend on the characteristics of the CMOS structure. For example, based on the parameters given in the MOSIS 2um CMOS technology, when the aspect ratios of P_1 and N_1 are 10μm/2μm and 4μm/2μm, respectively, *PSpice* simulation results show that, for $I_{in}=0$, the currents $I_{P1}=I_{N1}=0.1483$mA, and the current I_{P1} increases as the positive current I_{in} increases. Thus, the converted data will definitely include at least a 1 in the presence of such a fault and the test current $I_{in}=0$ detects the fault. Similarly, the test current also detects the *S/ON* fault on switch S_5.

In summary, two test current $I_{in}=0$ and $I_{in}= I_{ref}$ can detect all *S/ON* and *S/OFF* switches in the converter of Figure 4.3. Thus, the converter achieves full testability.

4.2 Testable Data-acquisition Circuits

Recently, with rapidly increasing complexity and size of modern electronic systems, automatic testing and fault diagnosis of electronic circuits have become more important and critical. Historically, analog circuits have been tested with the aid of a *bed of nails* tester that allows one to make use of test data which is not accessible via the input and output terminals of the circuit board, or chip. However, this is only pertinent to printed circuit boards with discrete circuit design including some replaceable units, and it does not apply to analog integrated circuits because only primary inputs and primary outputs are

accessible. Modern electronic systems are often multi-layered and/or coated, thereby limiting the applicability of the *bed of nails* concept. As the number of components in a unit increases, it is impractical to provide proportionately more I/O terminals. As a result, various existing analog circuit test algorithms have suffered from the restriction of the number and location of test points that must be externally accessible.

One approach to increasing the number of accessible nodes and thereby test points, while still keeping low pin overhead, is to incorporate *Built-In Self-Test* (BIST) circuitry into the *unit under test* (UUT) during the initial design. The BIST design has been successfully applied to the test of digital sequential circuits. With the BIST structure, circuits that generate test patterns and analyze the output responses of the functional circuitry are included on the same chip or elsewhere on the same board. In order to ensure the reliability of the copied test data, it is necessary to check whether or not the BIST structure is functioning properly before the structure is used. Thus, full testability of the BIST structure is one of the most important issues in the BIST design. Due to the difficulty of current measurement in an analog circuit, most of the fault diagnosis algorithms have been developed requiring only node voltage measurement. However, it has been shown that the use of both current and voltage measurement can simplify the diagnosis process significantly. In order to allow the current test data measured at various test points to be shifted out for fault diagnosis, a BIST structure has been implemented [41].

4.2.1 Built-In Self-Test Structures

The current-mode shift register described earlier can be used to sample and hold current test data. Results show that the shift register circuit is *self-testable* and allows the measured test data to be simultaneously loaded into the register cells and serially read out. The study of the structure initially attempts to simplify the fault analysis process and provides a possible BIST analog circuit design.

Scan-in and scan-out terminals are added to the current-mode shift register to form the BIST structure and make it testable as seen in Figure 4.4. Four test points, m_i, are

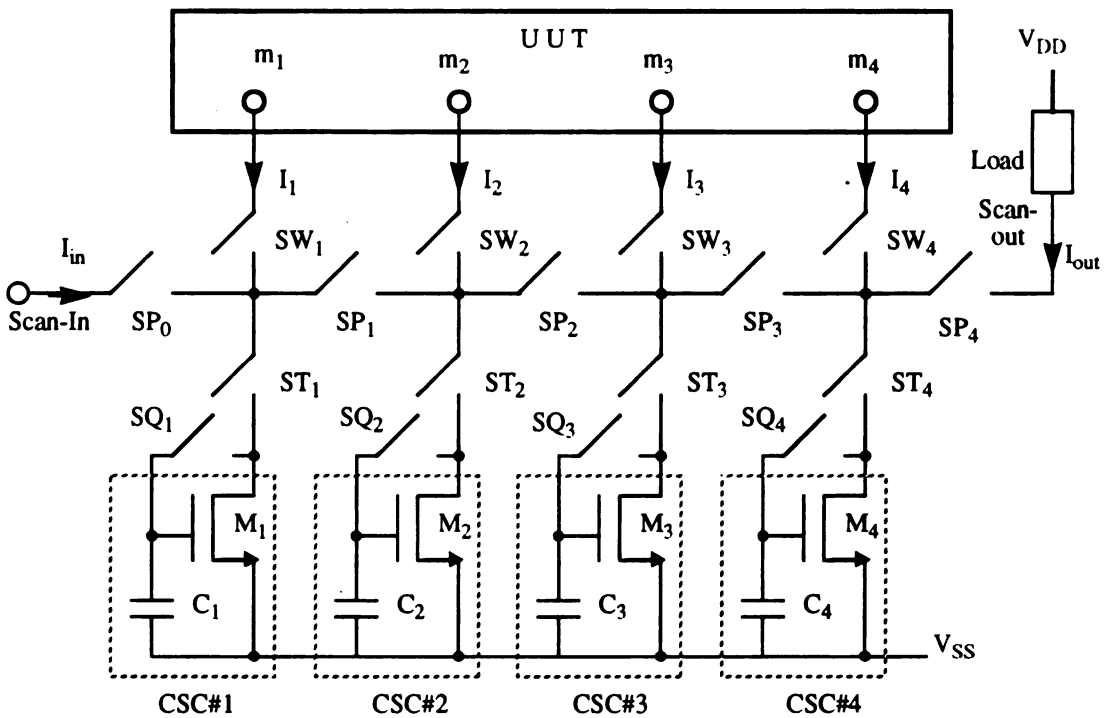


Figure 4.4 An BIST Structure Using Simple Current Copiers

assumed in the UUT and a 4-stage BIST structure is considered. The structure is operated in two modes: *the normal operation mode* and *the test mode*. During the normal operation mode, all switches SW_i are OFF, disconnecting the current storage cells from the test points. Thus, the BIST does not effect the functioning of the UUT. However, during the test mode, the BIST comes into play and is utilized to carry out fault diagnosis. In this mode, two operations can be identified. They are: *the load/shift operation* and *the scan test operation*. The scan test operation is to ensure the reliability of the BIST structure while the load/shift operation samples the current test data from the UUT. Since the BIST structure is non-redundant, any fault is considered fatal and no further testing of the UUT is needed.

In order to ensure the reliability of the copied test data, it is necessary to check whether or not the BIST structure is functioning properly before the structure is used for the load/shift operation. The BIST structure is tested by the scan test operation which includes the testing of switches SW_i, SP_i, ST_i, and SQ_i, and the storage cells.

The fault models considered in the BIST structure are *the stuck-at fault* for switches and *the functional fault* for the storage cells. The stuck-at fault model assume that a switch is either *stuck-at-ON state* or *stuck-at-OFF state*. The former, referred to as *stuck-at-ON fault*, implies that a switch is always ON regardless of the application of controlled clock signals, while the latter, referred to as *stuck-at-OFF fault*, indicates a switch is always OFF. The ability of storing correct test data in the storage cell determines whether the cell is functioning properly.

In order to ensure full testability of the BIST structure, the scan test operation proceeds by first checking the switches SP_i, ST_i, and SW_i, and then testing the storage cells and switches SQ_i. First, the switches SW_i and ST_i are all OFF, and SP_i are all ON, expecting a current copied at the load to be exactly the same as the current sunk into the scan-in portion if the switches are all fault-free. If any of the SW_i are stuck-at-ON, the corresponding input current, I_i, will also be sourced and the output current will be the summation of this current and the scanned in current, I_{in}. SP_i being open or stuck-at-OFF implies an open circuit in the scan path and I_{out} will be zero. With any ST_i stuck-at-ON, the respective NMOS copier will sink some current thus causing I_{out} to be the difference of I_{in}

and the sunk current. Thus, passing this test implies that neither stuck-at-ON faults occur in switches SW_i and ST_i, nor stuck-at-OFF faults in SP_i.

The storage cells, in general, can be tested by first loading test data from the scan-in portion to each storage cell and comparing the copied and stored currents. More specifically, turning on ST_4 and switching off SP_4 will load the test datum from the scan-in portion into the storage cell *CSC#4*. Then, with SP_3 and SQ_4 OFF and SP_4 ON, the copied current is expected to be identical to the stored current. Passing this test implies that the storage cell *CSC#4* and switch SQ_4 are functioning properly. Also, neither ST_4 nor SP_4 has a stuck-at-OFF fault implying that both the switches ST_4 and SP_4 are also functioning properly. Once the components in the fourth stage are tested to be all reliable, they can be used to test the third stage. The same test procedure can be carried out for the remaining stages. In summary, passing the above tests will ensure that all components, except switches SW_i, are fault-free. However, it has been checked that no stuck-at-ON fault occurs in SW_i. So, there is only the need to test whether or not the switches have stuck-at-OFF faults.

If a switch SW_i has a stuck-at-OFF fault, no current will flow through the switch and the current stored in *CSC#i* will be zero. On the other hand, if the current stored in *CSC#i* is zero, three cases can be identified: (1) the current I_i is actually zero (or nearly zero); (2) A faulty UUT induces I_i=0; and (3) the switch SW_i is stuck-at-OFF. Since cases 2 and 3 have already indicated the existence of fault, the remaining task is to distinguish case 1 from others. This can be done by applying appropriate inputs to the UUT during the test mode, (where the *appropriate* inputs are the ones which should generate a sufficiently large current I_i if the UUT is fault-free). Since the current I_i will not be zero with the appropriate inputs to the UUT, a zero current stored in *CSC#i* will indicate the existence of a fault in case 2 or case 3.

Thus, the BIST structure is concluded to be fully testable. The load-shift operation can then be carried out with this assurance. The sequence of steps for this mode is similar to the current-mode shift register and is carried out in the same manner.

As mentioned previously, there are several error effects that limit the accuracy of the simple current-copiers and thereby that of the current retrieved. In order to avoid the accumulation of offset errors and charge injection from the series switches SP_i in Figure 4.4, an improved version of BIST structure is shown in Figure 4.5, where switches SP_i are the scan switches which form a demultiplexer circuit, while switches ST_i form a multiplexer circuit for reading out the current test data. Both opamp and cascode current copiers can reduce the errors due to the channel length modulation. The improved BIST structures using such copiers may provide more accurate test data than that using the simple copier, but they require more chip area to implement them. The improved copiers may be used in cases where the original and copied currents must be matched precisely. In analog circuit fault diagnosis, however, a "good" component value may deviate from its nominal value within a predefined component tolerance. Thus, the test data obtained at various test points may also deviate from the expected "nominal" values within a certain tolerance even though the components are all good. Due to the inherent tolerance in analog circuits, precise matching of the original and copied current is desirable, but not necessary. The trade-off lies between precision and chip area. In principle, in cases where chip area is insignificant, such as board testing, the improved BIST structures may be employed. However, for chip testing, the BIST structure using the simple copier may be sufficient for fault diagnosis if the copied current deviates from the original current within 5 to 10 percent.

4.2.2 Experimental Results

Simulated verification of the design and operation of the BIST structure was done using *PSpice*. Various switching faults were induced in a 4-stage BIST made up of active copiers. Constant currents, I_i, were applied at the different test points as data from the UUT. A scan-in current of 75μA was used and the tests were run at a cycle time of 4μsec.

As the effect of a fault could cause bidirectional currents at the scan-out terminal, a bipolar copier was implemented as the load. The scanned out current I_{out} is thus given by

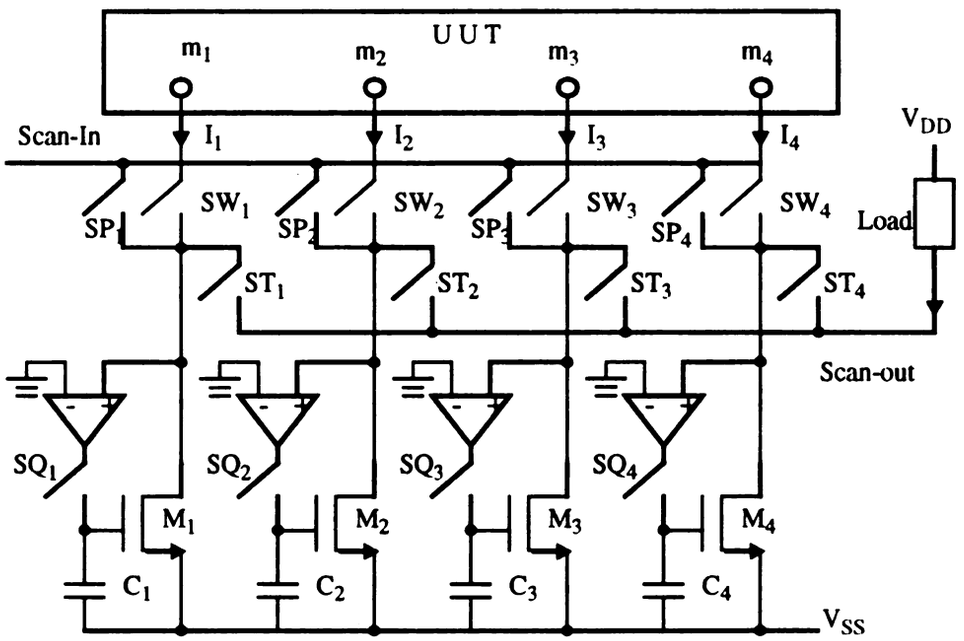


Figure 4.5 An Improved BIST Structure with Active Current Copiers

Id(mnout)-Id(mpout). The current through SP_0 is the current scanned in, I_{in} and through SW_i flow the currents, I_i.

Figure 4.6 shows the results of some of the tests performed on this BIST structure. Initially, a check is to be done for switches SP_i, ST_i, and SW_i. With SW_i and ST_i open and only SP_i on, the output current must equal the current scanned in. This step is verified in the first cycle of Figure 4.6, where there were no faults in the BIST and thus I_{out} is approximately 75μA. For a second test run, SP_i have to be verified to be not stuck-at-OFF. For example, when one of the pass switches SP_2 is stuck-at-OFF, it causes an open circuit and so $I_{out} = 0 \neq I_{in}$ and the BIST output during the second cycle of Figure 4.6 indicates that a fault has occurred. The next check is to verify that all the SW_i are open. SW_3 stuck-at-ON implies that I_3 will also combine with the scan-in current. As seen in the third cycle Figure 4.6, the current through switch SW_3 which is equal to 50μA adds with I_{in} =75μA and results in output of 125μA. Again the BIST successfully detected the fault. To check the stuck-at-ON faults on the ST_i, a charge of approximately 2.75Volts on the capacitor C_4 will cause the NMOS transistor in CSC#4 to sink 100μA of current. Consequently with ST_4 stuck-at-ON, $I_{out} = I_{in}$ - I(st4) and a negative current of -25μA is read out as seen in the last cycle of Figure 4.6. The bipolar copier load thus helps check the reliability of the BIST structure.

4.3 Summary

This chapter has presented a novel current-mode A/D converter design with time redundant CED capability. A slight addition in hardware of a PMOS copier is all that is required to make the validation of the converted data more reliable. The design can detect all transient faults that occur at the switching elements and most of the permanent faults. Some permanent faults cannot be detected due to the unavailability of test patterns for real-time applications. However, the same structure can be tested off-line with only two test patterns and this is described in the test generation process of the current-mode A/D

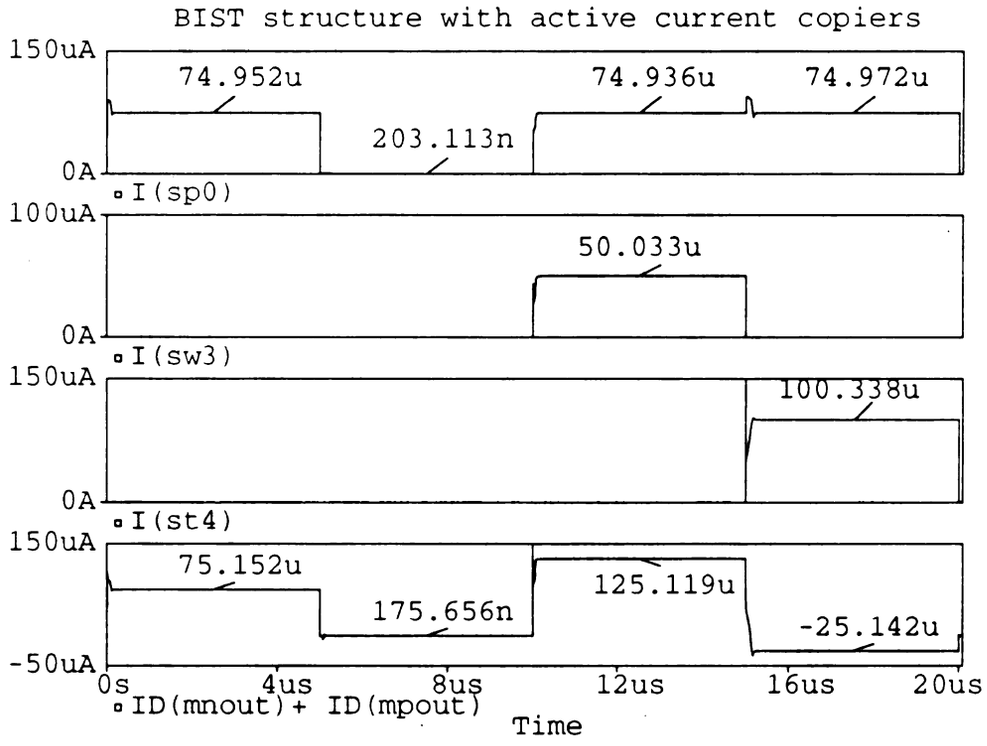


Figure 4.6 BIST Tests for Various Faults

converter. With the application of only two test signals, the converter achieves full testability of single stuck-at faults at the switching elements.

In the past, analog circuit fault diagnosis algorithms that have been developed were restricted for use only on small-scale networks due to the limited number of available test points and have strictly used voltage test samples. The analog BIST structure presented in this chapter increases the accessible nodes through scan terminals and utilizes current test data thus making fault diagnosis and testing much simpler. The BIST structure can be perfectly employed for testing mixed analog/digital circuits and can be incorporated into an analog function or module design.

Chapter 5

Conclusions

As pressure increases on VLSI designers to use a lower supply voltage, analog circuits operating in the voltage domain will suffer and circuits designed to exploit current-mode techniques will surely become increasingly important and attractive [8]. All too often the electronics engineer will think in voltage terms rather than current simply because of the unavailability of current-mode signal processing circuits [3]. The primary goal of this dissertation has been to develop a gamut of current-mode data-acquisition and conversion circuits. This chapter describes the major contributions of this research and addresses some potential problems for further investigation.

5.1 Summary

In this research, a set of new circuits, such as bipolar copiers, current-mode shift registers and current-mode dividers have been presented for the design of current-mode A/D converters and their array structures.

The bipolar copier which is a very useful building block in the design of current-mode data-acquisition and conversion circuits has been presented. This copier can precisely memorize input current which is either positive or negative. Its bidirectional capability makes it an important element in general purpose multipliers and dividers. It forms an integral part of a current divider that generates reference current levels for a successive-approximation A/D converter. In analog fault diagnosis with current data, a

malfunction in a circuit may cause currents to be of any polarity. Thus, the need for a circuit that can sense bidirectional current arises. This necessity can be satisfied by the bipolar copier which can then be used as a load to sense the current test data. The use of this copier in these applications has also been demonstrated.

A current-mode shift register has been developed to copy currents. This shift register can be used to load sensory information for signal processing and can be arranged to exploit the parallelism of array structures. Although the shift-register is similar to an analog multiplexer circuit, its structure indicates that it can be easily adapted to obtain a possible analog BIST circuit design for current test data. This was possible by the use of an additional scan-in terminal for self-testability which allows the structure to detect any faults, either stuck-at faults at switching elements, or functional faults in the storage cells. Both the shift register and its BIST implementation have been simulated to verify their operation principle.

According to the switching operation of the current-mode shift register circuit the data held at the first stage will be read out last. For this reason, the criterion to determine the optimal number of stages for the shift register structure given the precision of the measurement has been developed. The reduction in the number of stages can be achieved by increasing the number of scan paths and forming a parallel structure in which several shift registers can be arranged in rows. Thus, instead of having a long sequential chain, several short serial segments can be operated in parallel.

Current dividers are important signal processing elements but have been limited in their accuracy by device mismatch. This dissertation has presented a highly accurate current-mode divide-by-two circuit that does not require well-matched components or a high gain opamp. The circuit allows any mismatch factors between the divider transistors through its use of the bipolar copier. The current-mode divider circuit has been implemented as the reference-generating (RG) circuit of the current-mode A/D converter. The number of iterations required for the divide-by-two circuit to obtain the desired accuracy has been formulated and its performance has been assessed through simulations.

This dissertation has also presented a successive-approximation current-mode A/D converter that functions through a divide-by-two scheme. The circuit does not rely on high gain amplifiers or well-matched components to achieve high resolution and is inherently insensitive to the amplifier's offset voltage. For the practical 1% mismatch between the divider transistors of the RG circuit, 5 clock cycles are required to generate each reference level. In general, the converting (CV) circuit of the A/D converter may require only two or three cycles. Thus, the slower RG circuit may degrade the conversion rate. In practice, however, a common RG unit may be shared by several CVs to simultaneously convert several analog data. Based on this idea, the converter design has been modified to obtain a parallel A/D converter with a common RG circuit to achieve a higher conversion rate. The array structure has been designed such that several functional units are time shared thus utilizing minimum hardware. Results show that the array structure achieves high resolution and high conversion rate at a very low hardware cost.

In order to improve the reliability of data validation for real-time operations, this paper presents a novel current-mode A/D converter design with CED capability, where a time redundant scheme is implemented. The original A/D converter with the addition of only a PMOS current copier provides CED capability improving its reliability. The design can detect all transient faults that occur at the switching elements and most of the permanent faults. Some permanent faults cannot be detected due to the unavailability of test patterns for real-time applications. To satisfy this need and to enable off-line testing, test generation of the current-mode A/D converter has also been demonstrated. With the application of only two test signals, the converter achieves full testability of single faults at the switching elements. Therefore, as permanent faults can be fully testable by these two test patterns it is suggested to randomly apply the two test signals to the A/D converter detecting the permanent faults during real-time operation.

The drawback of this design with CED capability is approximately 100% overhead in time which is inherent in all time redundancy schemes. Judging from the VLSI performance measure of AT^k (where A is the chip area, T is the operation cycle time, and k is a parameter determined by the applications), this is rather a high price to pay

particularly when k is increased. However, the performance penalty associated with time redundancy can be absorbed by the inherent idleness of the processing element. This design can be effectively applied to those systems or subsystems in which the time to process the converted data is as much as twice of the conversion time. The other salient feature is that the design allows users to easily switch between an A/D converter with and one without CED capability without causing any performance degradation.

To alleviate the problem of limited number of available test points for fault diagnosis of analog circuits, analog Built-In Self-Test (BIST) structures have been implemented in this dissertation. These structures provide more test points, while still keeping low pin overhead, for analog fault diagnosis with current test data and voltage test data. With both BIST structures, fault diagnosis and testing of analog circuits will become simpler. In addition, these structures also provide an innovative feature that allows designers to use one channel of an oscilloscope to simultaneously monitor multiple output waveforms of analog circuits or systems. The BIST structures are perfectly employed for fault diagnosis and testing of mixed analog/digital circuits and can be incorporated into an analog function or module design. In addition, it is better off to include an A/D converter into the analog module so that the test outputs of the analog module are in digital form. The digital data obtained from the digital modules and the analog modules are then processed by a simple microprocessor for fault diagnosis and testing.

5.2 Contributions

The major contributions of this research are described as follows.

(1) This dissertation has successfully developed, analyzed and constructed current-mode signal processing circuits that include bipolar copiers, current-mode shift registers, current-mode dividers, A/D converters and converter arrays.

(2) In this study, diagnosable circuit design methodologies have been applied to current-mode data-acquisition and conversion circuits in order to enhance their reliability.

(3) The investigation of some practical design issues through simulations, to assess the performance of the architectures presented has also been carried out.

(4) This research has also investigated the design trade-offs and developed a design strategy to provide an optimal solution for the integration of the current-mode circuits with IC sensor arrays.

5.3 Future Research

For the design of these analog signal processing circuits, it is essential to apply MOS technology to the single chip implementation of analog and digital circuits. As both the digital control units and the analog interface systems such as the A/D converters, sample-and-hold elements have to be implemented on the same chip, there has to be an automated design tool to cope with the complexity of building such large scale mixed mode circuits. The performance specifications for the analog building blocks are more complicated that the digital ones. Thus, a topology and layout for the A/D converter for the given specifications has to be chosen. The device sizes and currents have to be adjusted to satisfy performance criteria such as power dissipation, bandwidth, sampling rate, settling time, area, etc. It is the future intent of this research, to develop a methodology for a design and layout tool that optimizes the design and performance of these current-mode signal processing circuits.

Current copier cells are controlled by digital clock signals. The potential crosstalk problem of digital noise finds its way into sensitive analog circuitry [47]. Although the problem can be handled effectively by judicious use of multiple power bussing and desensitized analog circuitry, the noise problem will worsen in the future as digital speeds will increase, additional analog circuitry will be included, chips will become more densely packed, interconnect layers will be added, and analog resolution will be increased. A number of possible sources of performance degradation in mixed analog/digital ICs have been identified: signal coupling through the substrate, coupling through parasitic wiring capacitance, and coupling the IR drops in the power distribution network [47]. However,

quantitatively modeling and simulating these effects is extremely difficult. Therefore, these dominant error sources and the limitations they impose on the performance of the various current-mode signal processing circuits have to be assessed. Therefore, it is also necessary to develop in the automated tool a method for designing such mixed analog/digital current-mode circuits so that alternative circuit structures for various design variations can be investigated.

Integration of sensing and processing on chip yields a qualitative improvement in performance. Thus, the shift registers and the converter array can be integrated along with an array of sensors. Recently, a smart sensor array has been implemented for a *light-stripe rangefinding system*, where each pixel contains a photodiode to detect the light stripe and an analog signal processor to determine and store the time at which the light stripe crosses that photodiode [48]. For the current-mode data-acquisition and conversion circuits developed and analyzed, the demonstration of integrating these circuits with an IC sensor array can be conducted. Figure 5.1 illustrates a possible implementation of the current-mode A/D converter array in a sensor array [49]. The architecture is comprised of a sensor array, current-mode analog shift registers, a current-mode A/D converter array with a common RG circuit, and a set of high speed digital shift registers. The sensory information is sampled row-wise into a set of current-mode shift registers and is then shifted out serially to a channel of the current-mode A/D converter array. These independent signals sources are processed through the same converter or communications channel and so a multiplexer is usually introduced to couple the input signals into A/ D converter in some sequence. Additional switching logic can keep track of which data source is coupled to the converter at any instant. After the conversion, multiplexers can then output, one at a time, the converted data from the array, to common digital shift registers. The current-mode shift registers can be arranged more efficiently to exploit the parallelism in the array structure and to have more accurate sampling. To reduce the hardware cost, the array structure shares resources and alternately processes data in the CCV_o and CCV_e circuits. Apparently, the hardware reduction is achieved at the cost of performance of the sensory structure. Future study can explore the advantages and

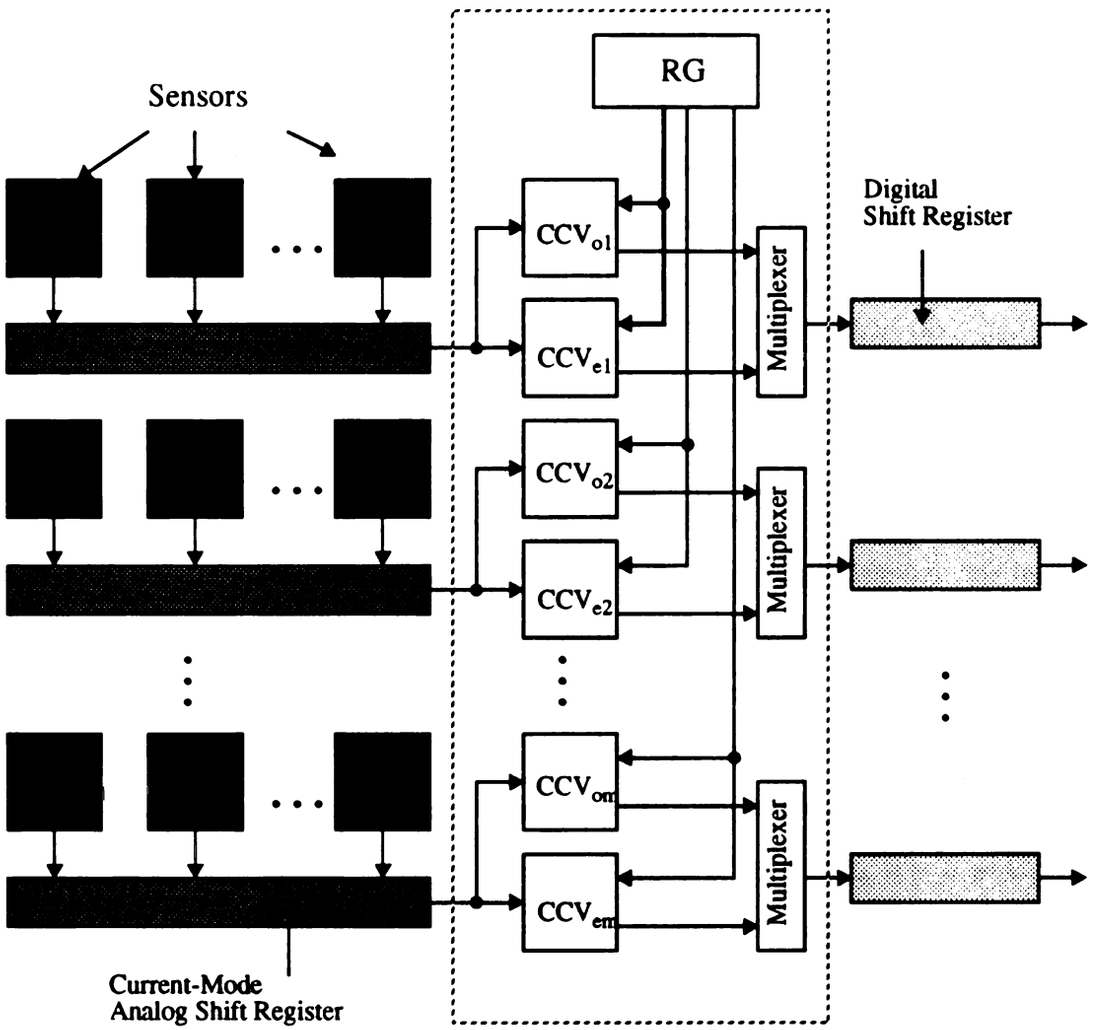


Figure 5.1 A Sensor Array Implementation

disadvantage of implementing such structures and identify their best applications. An arbitrary IC sensor array may be used to demonstrate the practicality and resulting improvement in using these current-mode circuits.

As the copiers may be used as sample-and-hold elements to read data from sensors, their operation under changing sensory conditions should be investigated. As temperature sensing is an important application, *PSpice* simulations were run at different temperatures on the simple bipolar copier copying positive current of 50μA. Results show that the copier functions correctly, but its accuracy varies with temperature as shown in Figure 5.2. This variation is mainly due to the dependence of certain parameters, such as transconductance (k'), bulk p-n saturation current (*IS*), junction capacitances, and several others on temperature. One primary error source of the copier, leakage current, thus varies with temperature. Other sources of error and factors that come into play at different temperatures are also to be investigated.

For the diagnosable design of the current-mode circuits, the fault model considered in this study was the single-stuck at fault in the switching elements. Although this fault was focussed on, the faults that occur in other elements can be modeled as the equivalent faults of the switching elements. This leads to an interesting area for future study. Also the concurrent error detection time redundancy scheme was Alternating Logic. Some interesting prospects of better fault coverage may be obtained by the use of the RESO (REcomputing with Shifted Operands) scheme. Shifting in the analog world would mean multiply or divide the signal by two. As both the multiplier and the divider circuits are available in current-mode, this method could also be implemented in the future.

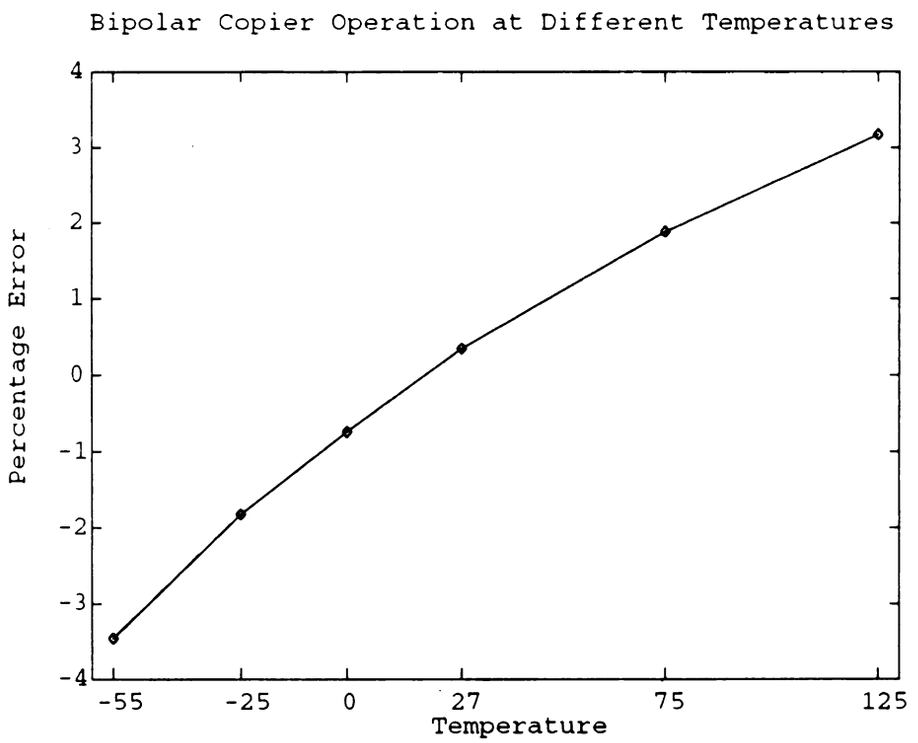


Figure 5.2 Temperature Dependence of Bipolar Copier Operation

APPENDICES

Appendix A

A CMOS Opamp

The operational amplifier used for the simulations is a two-stage, N-channel input, unbuffered CMOS opamp, as shown in Figure A.1, where compensation is achieved through resistor, rz, and capacitor, cc. The simulated characteristics of the operational amplifier are given in Table A.1.

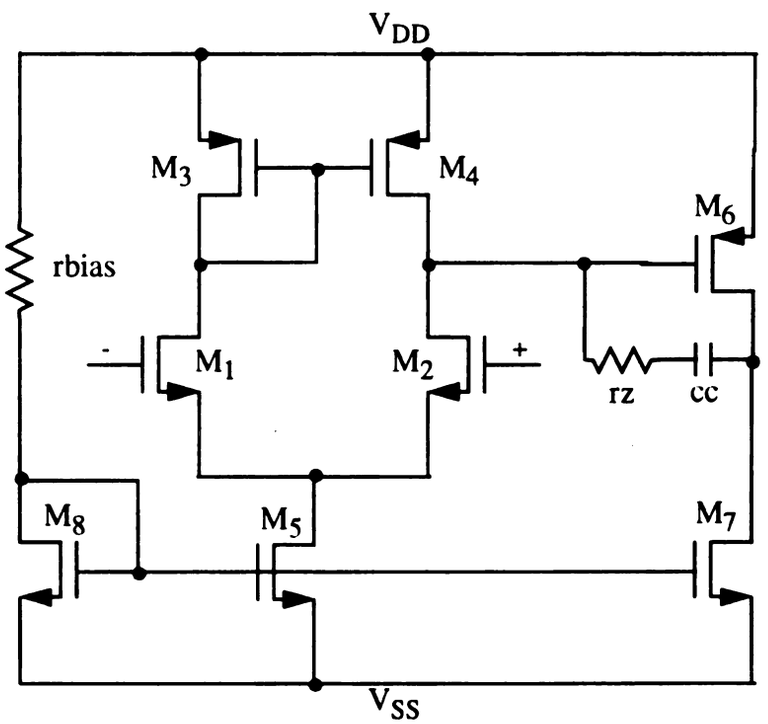


Figure A.1 A Two-stage CMOS Opamp

Table A.1 Simulated Characteristics of Opamp

Design Specification	Simulation Result
Supply Voltage	5 V olts
Open Loop Gain	44.18 dB
Phase Margin (Load Capacitance=10pF)	94°
Gain Bandwidth Product (Load Capacitance=10pF)	3.58 MHz
Output Resistance	5.77KΩ
Input Resistance	$1E^{20}\Omega$
Slew Rate (Load Capacitance=10pF)	9.556 (+) V/μsec 7.567 (-) V/μsec
Input Offset Voltage	1.46mV
Input CMR	+4.47V, -5V
Output Voltage Range	+4.924V, -5V
Power Dissipation	1.91 mW

Appendix B

PSpice Files

mos.lib

```
* parameters: MOSIS 2 micron CMOS process on Oct.3, 1990
.model nmos nmos level=2 ld=0.25u vto=.771327 kp=56.06u gamma=.53 phi=.6
+ lambda=.030894 rsh=29.6 cj=113.65u cjsw=531.87p mj=.6862 mjsw=.2651
+ cgso=322.9249p cgdo=322.9249p cgbo=672.6429p nsub=6.257042e+15
+ nss=10.0e+9 nfs=4.834708e+12 tox=40.1n xj=0.25u uo=650.996
+ ucrit=41.9315e+3 uexp=.153507 vmax=67.6608e+3 delta=.472546
.model pmos pmos level=2 tpg=-1 ld=0.20961u vto=-.78821 kp=22.3u gamma=.5486
+ phi=.6 lambda=.049817 rsh=90.7 cj=251.36u cjsw=294.47p mj=.5471
+ mjsw=.3188 cgso=270.7532p cgdo=270.7532p cgbo=583.9625p
+ nsub=6.722092e+15 nss=10.0e+9 nfs=0.1e+12 tox=40.1n xj=0.25u uo=259
+ ucrit=12.5945e+3 uexp=.182346 vmax=41.2226e+3 neff=1.001 delta=.844423
```

CMOS opamp with lead compensation

```
.subckt opamp 1 2 6 100 101
*              + - o  +p  -p
m1 4 2 3 3 nmos w=10u l= 2u
m2 5 1 3 3 nmos w=10u l= 2u
m3 4 4 100 100 pmos w=20u l= 2u
m4 5 4 100 100 pmos w=20u l= 2u
m5 3 7 101 101 nmos w=2u l= 2u
m6 6 5 100 100 pmos w=76u l= 2u
m7 6 7 101 101 nmos w=4u l= 2u
m8 8 7 101 101 nmos w=2u l= 2u
rz 5 9 7.28K
cc 9 6 5p
rbias 100 8 158K
rsc 7 8 1
.LIB mos.lib
.ends
```

A CMOS switch

```
.subckt msw 210 212 213
*             In   Out Ctrl
vdd 25 0 5
vss 24 0 0
m1 210 211 212 25 pmos w=5u l=2u
m2 210 213 212 24 nmos w=2u l=2u
m3 211 213 25 25 pmos w=2u l=2u
m4 211 213 24 24 nmos w=2u l=2u
.LIB mos.lib
.ends
```

Bipolar current copier

```
* Copying positive current

* The power supplies
vdd 10 0 5
vss 9 0 0
*The input
m11 101 101 10 10 pmos w=5u l=2u
m12 102 101 10 10 pmos w=5u l=2u
i1 101 0 50u
xsw 102 11 1w msw
vsc 11 1 0
* The bipolar copier
mp1 3 4 10 10 pmos w=5u l=2u
mn1 3 4 9 9 nmos w=2u l=2u
cp1 4 9 10p
st 1 3 1t 0 sw
sq 3 4 1q 0 sw
* The output stage
mpout 7 8 10 10 pmos w=5u l=2u
cpout 8 10 4p
stout 1 7 2t 0 sw
sqout 7 8 2q 0 sw

*Digital waveforms for switching

U1 STIM(3, 111) $G_DPWR $G_DGND 1w 1t 1q
+ IO_STM TIMESTEP = 0.2us
+Label = start1
+ 0c 111
+ 4c 110
+ 5c 010
+ 10c 000
+ +5c GOTO start1 5 times

Uout STIM(2, 11) $G_DPWR $G_DGND 2t 2q
+ IO_STM TIMESTEP = 0.2us
+Label = start1
+ 0c 00
+ 5c 11
+ 9c 10
+ 10c 00
+ +5c GOTO start1 5 times

.model sw vswitch(ron=10 roff=100e+6 von=5
voff=0)
.LIB mos.lib
.LIB sw.lib
.LIB digital.lib
.tran 0.01u 2u 0u 0.01u UIC
.IC v(4)=0.0 v(8)=0.0
.probe
.end
```

Bipolar current copier

```
* Copying negative current

* The power supplies
vdd 10 0 5
vss 9 0 0
*The input
m11 101 101 9 9 nmos w=5u l=2u
m12 102 101 9 9 nmos w=5u l=2u
i1 10 101 50u
xsw 102 11 1w msw
vsc 11 1 0
* The bipolar copier
mp1 3 4 10 10 pmos w=5u l=2u
mn1 3 4 9 9 nmos w=2u l=2u
cp1 4 9 10p
st 1 3 1t 0 sw
sq 3 4 1q 0 sw
* The output stage
mnout 7 8 9 9 nmos w=5u l=2u
cnout 8 9 4p
stout 1 7 2t 0 sw
sqout 7 8 2q 0 sw

*Digital waveforms for switching

U1 STIM(3, 111) $G_DPWR $G_DGND 1w 1t 1q
+ IO_STM TIMESTEP = 0.2us
+Label = start1
+ 0c 111
+ 4c 110
+ 5c 010
+ 10c 000
+ +5c GOTO start1 5 times

Uout STIM(2, 11) $G_DPWR $G_DGND 2t 2q
+ IO_STM TIMESTEP = 0.2us
+Label = start1
+ 0c 00
+ 5c 11
+ 9c 10
+ 10c 00
+ +5c GOTO start1 5 times

.model sw vswitch(ron=10 roff=100e+6 von= 5
voff=0)
.LIB mos.lib
.LIB sw.lib
.LIB digital.lib
.tran 0.01u 2u 0u 0.01u UIC
.IC v(4)=0.0 v(8)=0.0
.probe
.end
```

Current-mode Shift register

```
* Four stages with active current copiers

* The power supplies
vp+ 110 0 5
vp- 90 0 -5
vdd 100 0 5
vss 9 0 0
vbias 108 0 2.5

* The first cell
i1 0 10 150u
r1 0 10 100K
sw1 10 11 1w 0 sw
m1 12 13 9 9 nmos w=2u l=2u
c1 13 9 100p
st1 11 12 1t 0 sw
sq1 14 13 1q 0 sw
sp1 11 21 1p 0 sw
x1 11 108 14 110 90 opamp

*The second cell
i2 0 20 50u
r2 0 20 100K
sw2 20 21 2w 0 sw
m2 22 23 9 9 nmos w=2u l=2u
c2 23 9 100p
st2 21 22 2t 0 sw
sq2 24 23 2q 0 sw
sp2 21 31 2p 0 sw
x2 21 108 24 110 90 opamp

* The third cell
i3 0 30 75u
r3 0 30 100K
sw3 30 31 3w 0 sw
m3 32 33 9 9 nmos w=2u l=2u
c3 33 9 100p
st3 31 32 3t 0 sw
sq3 34 33 3q 0 sw
sp3 31 41 3p 0 sw
x3 31 108 34 110 90 opamp

* The fourth cell
i4 0 40 125u
r4 0 40 100K
sw4 40 41 4w 0 sw
m4 42 43 9 9 nmos w=2u l=2u
c4 43 9 100p
st4 41 42 4t 0 sw
sq4 44 43 4q 0 sw
sp4 41 51 4p 0 sw
x4 41 108 44 110 90 opamp

* The output stage
mpout 51 53 100 100 pmos w=5u l=2u
cout 53 100 10p
sqout 54 53 5q 0 sw
x5 51 108 54 110 90 opamp

*Digital waveforms for switching

U1 STIM(4, 1111) $G_DPWR $G_DGND 1w 1t 1q 1p
+ IO_STM TIMESTEP = 1us
+Label = start1
+ 0c 1110
+ 4c 1100
+ 5c 0000
+ 20c 0101
+ 25c 0001
+ +5c GOTO start1 5 times

U2 STIM(4, 1111) $G_DPWR $G_DGND 2w 2t 2q 2p
+ IO_STM TIMESTEP = 1us
+Label = start2
+ 0c 1110
+ 4c 1100
+ 5c 0000
+ 15c 0101
+ 20c 0001
+ +10c GOTO start2 5 times

U3 STIM(4, 1111) $G_DPWR $G_DGND 3w 3t 3q 3p
+ IO_STM TIMESTEP = 1us
+Label = start3
+ 0c 1110
+ 4c 1100
+ 5c 0000
+ 10c 0101
+ 15c 0001
+ +15c GOTO start3 5 times

U4 STIM(4, 1111) $G_DPWR $G_DGND 4w 4t 4q 4p
+ IO_STM TIMESTEP = 1us
+Label = start4
+ 0c 1110
+ 4c 1100
+ 5c 0101
+ 10c 0001
+ +20c GOTO start4 5 times

U5 STIM(1, 1) $G_DPWR $G_DGND 5q
+ IO_STM TIMESTEP = 1us
+Label = start5
+ 0c 0
+ 5c 1
+ 9c 0
```

```
+ 14c 0
+ 15c 1
+ 19c 0
+ 20c 1
+ 24c 0
+ +6c GOTO start5 5 times

.model sw vswitch(ron=10 roff=100e+6
+von=5 voff=0)
.LIB mos.lib
.LIB opamp.lib
.LIB digital.lib
.tran 0.005u 25u 0u 0.005u UIC
.IC v(13)=0 v(23)=0 v(33)=0 v(43)=0
.probe
.end
```

Current-mode Divider

*(W/L)2 > (W/L)3 : 5% mismatch

```
* The power supplies
vp+ 100 0 5
vp- 90 0 -5
vdd 110 0 5
vss 109 0 0

* The input stage
iin 0 101 125u
rin 0 101 100K
sw0 101 10 1v 0 sw

* The error corrector stage - mp1 and mn1
sw1 10 1 11 0 sw
sw2 107 2 12 0 sw
mn1 1 2 109 109 nmos w=2u l=2u
mp1 1 2 110 110 pmos w=5u l=2u
c1 2 109 40p

* The divider stage

* The nmos stage - m2
sw3 10 3 13 0 sw
sw4 107 4 14 0 sw
m2 3 4 109 109 nmos w=2.2u l=2u
c2 4 109 40p

* The nmos stage - m3
sw5 10 5 15 0 sw
sw6 107 6 16 0 sw
m3 5 6 109 109 nmos w=2u l=2u
c3 6 109 40p

* The pmos stage - m4
sw7 10 7 17 0 sw
sw8 107 8 18 0 sw
m4 7 8 110 110 pmos w=5u l=5u
c4 8 110 40p
* The opamp stage
x100 10 108 107 100 90 opamp
vbias 108 0 2.5

* Digital waveforms for switching

Uin STIM(1, 1) $G_DPWR $G_DGND 1v
+ IO_STM TIMESTEP = 0.6us
+Label = instart
+ 0c 1
+ 5c 0
+ +10c GOTO instart 5 times

Ucmos STIM(2, 11) $G_DPWR $G_DGND 11 12
+ IO_STM TIMESTEP = 0.6us
+ 0c 00
+Label = cstart
+ 10c 11
+ 14c 10
+ 20c 00
+ +5c GOTO cstart 5 times

Unmos STIM(4, 1111) $G_DPWR $G_DGND 13 14 15 16
+ IO_STM TIMESTEP = 0.6us
+Label = nstart
+ 0c 1111
+ 4c 1010
+ 5c 0010
+ 10c 1000
+ +5c GOTO nstart 5 times

Upmos STIM(2, 11) $G_DPWR $G_DGND 17 18
+ IO_STM TIMESTEP = 0.6us
+ 0c 00
+Label = refstart
+ 5c 11
+ 9c 10
+ 15c 00
+ +5c GOTO refstart 5 times

.model sw vswitch(ron=10 roff=100e+6 von=5 voff=0)
.LIB mos.lib
.LIB opamp.lib
.LIB digital.lib
.tran 0.01u 72u 0u 0.01u UIC
.IC v(2)=0.0 v(4)=0.0 v(6)=0.0 v(8)=0.0
.probe
.end
```

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