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AN INVESTIGATION OF ANISOTROPIC ETCHING OF SILICON IN AN ELECTRON CYCLOTRON RESONANCE PLASMA

By

Brian David Musson

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ABSTRACT

AN INVESTIGATION OF ANISOTROPIC ETCHING OF SILICON IN AN ELECTRON CYCLOTRON RESONANCE PLASMA

By

Brian David Musson

The increasing density of integrated circuits has lead to a need for novel chemical techniques to produce silicon chips. Acids and other wet chemistries cannot be used to anisotropically etch small (<5μm) features. Plasma techniques for etching experienced rapid growth in the 1970's and 1980's but traditional plasma etchers may be eclipsed by new technologies due to the inherent problems in older plasma systems. ECR plasma reactors, capable of operating at very low pressures (<1mTorr), producing low ion energies, and low sheath potentials show great promise for achieving low damage, highly selective anisotropic silicon etching.

A new ECR plasma source is investigated for anisotropically etching silicon over large (>125 mm) diameters. Low pressure (<1mTorr) experiments in an SF_6/Ar gas mixture have shown anisotropic profiles with etch rates of 80 nm/min and uniformities of 5% (3σ values) over 125 mm wafers. Etch profiles at various ρ, ϕ positions are also investigated and shown to be uniform.

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Chapter 1

Introduction

New techniques for etching silicon, along with a number of other scientific advances, have allowed the integrated circuit (IC) industry to produce highly reliable, extremely small, low cost chips for use in practically all electronic devices. Older methods employing liquid or vapor phase chemistry suffer from uniformity and wetability problems in the sub-ten micron size range. Plasma processing, introduced in the late 1960's and used extensively in the 1970's and 1980's, has allowed the industry to uniformly and anisotropically pattern silicon wafers. Plasma techniques are currently the most widespread method used for etching silicon and insulating (SiO_2 and Si_3N_4) layers on ICs. Interest in reducing or eliminating some of the drawbacks of conventional plasma systems has provided the impetus for investigation into new plasma sources. The electron cyclotron resonance (ECR) microwave plasma disk reactor (MPDR) utilized in this research is one such example of a new source.

ECR reactors have generated considerable interest recently due to the many advantages they hold over conventional plasma systems. Low, controllable sheath potentials, high degrees of ionization, and low pressure operation coupled with the electrodeless design of the reactor constitute promising system features that may provide the necessary characteristics for widespread acceptance of MPDR ECR systems. This work has specifically

investigated silicon etching as a function of chamber pressure and working gas composition and is an extension of earlier work at Michigan State University [1] which studied the use of ECR etching systems for feature sizes with dimensions of several micrometers.

A principal hypothesis of this research was that the MPDR ECR system would also be effective at etching submicron features. A second hypothesis was that as compared to divergent field ECR systems, the MPDR ECR system would show less spatial variation in etch profiles across the wafer surface. The results of the research support both of these hypotheses.

Chapter 2 presents a background of IC etching and demonstrates a need for plasma processes. Fluorine etching is reviewed along with currently used industrial plasma systems. Currently investigated microwave plasma generators are reviewed and previous MPDR results are presented.

Sample preparation techniques are presented in chapter 3. A process for sub-micron pattern definition in a positive and negative tone is detailed along with an aluminum lift-off recipe to provide submicron aluminum lines without aluminum etching. Aluminum is used as a robust mask to study etching profiles in chapter 5.

The MPDR and vacuum system used in the etching experiments are diagrammed in chapter 4. Etching gas selection and pattern and uniformity evaluation techniques are also described.

Chapter 5 presents uniformity, profile, and etch rates on multiple 75 mm diameter and single 125 mm diameter wafers. Orientation and positional

effects are investigated and found to be uniform across a 150 mm diameter. *Preliminary* damage assessment studies using depletion layer capacitance techniques are shown to exhibit a dopant compensation layer extending 1.5μm into the silicon.

Chapter 2

Background

2.1 Introduction

In the early 1960's Texas Instruments produced the first integrated circuit (IC). Thirty years later, this technology has become the backbone of the electronics industry, currently larger than the aerospace, automobile, and steel industries combined. Phenomenal growth rates (sometimes over 25 percent per year) have fueled the most rapid sustained expansion of any industry in history [2] [3]. Minimum feature sizes, such as gate widths, have decreased two orders of magnitude to as small as 0.5μm. An estimated 3,500 technical papers are published each year presenting new and informative work in the field of integrated circuits [4]. The silicon transistor has permeated our lives and transformed the way we work and think.

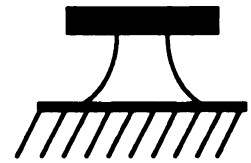
One of the most important processes in modern silicon IC fabrication lines is plasma processing. Plasma processes have replaced many of the typical chemical processes and are used in fields such as; silicon and polysilicon etching, oxide and nitride etching and deposition, aluminum etching, wafer cleaning, photoresist stripping, and planarization. This chapter briefly describes some of the industry standard plasma systems and presents the rational for ECR plasmas. Also presented are plasma systems based upon the ECR phenomena.

2.2 Role of Etching in IC Technology

An early MOS process in 1974 typically incorporated only 35 processes with wet chemistry compromising fully one third of all steps. Acids such as hydrofluoric (HF), phosphoric (H_3PO_4), and nitric (HNO_3) were commonly used for etching oxides and metals [5]. In the wet etch process, a patterned layer of photoresist is initially deposited on the surface of the silicon wafer (see Figure 2.1). The resist is hardened to form a polymerized surface and the entire wafer is immersed in or sprayed with an etchant to remove the underlying layer. Wet chemistry, by its very nature, is generally an isotropic process. In an isotropic process, the underlying layer is removed in both the horizontal and vertical direction (Figure 2.1a). When horizontal dimensions were on the order of several microns an engineer could design a mask with undercutting in mind to achieve the desired feature dimension (Figure 2.1b). As feature sizes began to decrease, mask compensation was unable to overcome the drawbacks of isotropic etching. Anisotropic pattern transfer (no horizontal layer removed) is required for small features and densely packed circuits (Figure 2.1c).

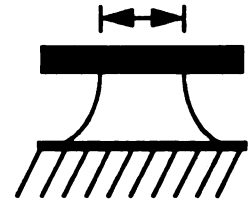
2.3 Applications for Anisotropic Silicon Etching

Two common applications for anisotropic silicon etching are trench isolation and trench capacitors. Trench isolation refers to etching deep, narrow trenches between devices to electrically isolate individual transistors [6]. Trench capacitors are capacitors formed on the surface layer of trenches etched into a material. Also of issue is highly selective, low damage etching



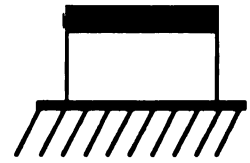
Photoresist
Resultant Feature
Bottom Layer

(a)



Required Feature Size

(b)



Anisotropic Transfer

(c)

Figure 2.1 Pattern Transfer showing a) isotropic mask undercutting, b) mask compensation, and c) anisotropic transfer (after Sze, Reference 52)

of polysilicon gates in MOS devices [7] [8]. In each of these three applications, ECR etching offers the potential for improved processing as will be discussed in section 2.7.

2.3.1 Trench Isolation

CMOS circuits present potential dangers by exhibiting parasitic BJT-type behavior with the transistor body acting as a base. This problem can be overcome by a deep implantation (buried layer) of an opposite dopant (p-type into an n-body, or n-type into a p-body) and reverse biasing the resulting junction [9].

Latch-up, a significant problem seen in early CMOS circuit designs, occurs when the substrate acts as a conducting path between the NMOS and PMOS regions. The CMOS device can then behave as a silicon controlled rectifier (SCR). Diffusing deep rings of opposing dopant around both the NMOS and PMOS regions and reverse biasing the diodes effectively eliminates this problem [10]. Both procedures (buried layers and dopant rings) require extra high temperature steps which result in increased carrier diffusion. As scaling of CMOS circuits is reduced, tighter control over junction depths and profiles is necessary. The available time at a given temperature for thermal processing decreases as MOS technology sizes decrease (Figure 2.2). Ion implantation, although done at a lower temperature, requires a significant post-implant anneal and therefore will also carry a thermal budget. As can be seen in Figure 2.2, very small devices have a very limited high temperature processing time. Clearly, extra diffusion or annealing

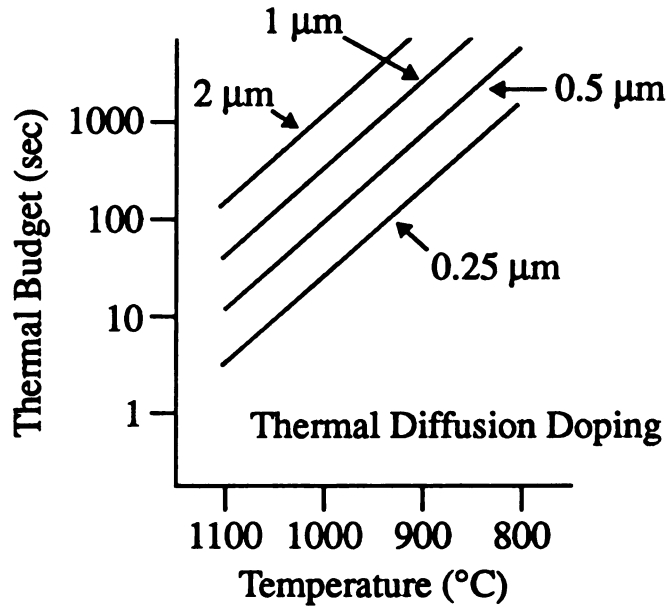


Figure 2.2 Thermal Budgets. Time available at a given temperature to produce scaled junction depths (after Fair, Reference 11)

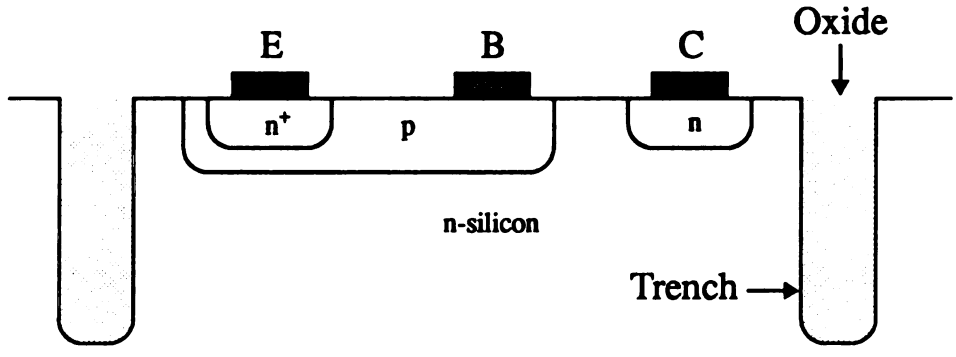


Figure 2.3 BJT cell with trench isolation

steps must be avoided.

An alternative to diffusing (or implanting) rings around transistors is electrical isolation by deep trenches. BJT inter-transistor parasitic capacitances and resistances may also be improved by tench isolation. Current work in both CMOS and BJT research employs trench isolation in a wide variety of applications [12]-[13]. Trenches are typically three to four times as deep as the deepest junction and are filled with a low temperature chemical-vapor-deposition (CVD) oxide. Figure 2.3 shows a representative BJT cell with trench isolation.

2.3.2 Trench Capacitors

Another benefit of trenched silicon is the possibility of creating vertical capacitors. DRAM cells require capacitors to hold a charge between refresh cycles and should ideally be very small (occupy a small planar chip area) and have a high capacitance. Trench walls may be coated with a thin layer of a CVD oxide to serve as a dielectric and the remaining volume filled with a conductor such as polysilicon (Figure 2.4). This geometry can create a capacitor with a surface area approximately $4z/d+1$ times larger than a planar (surface) capacitor. A 1μm diameter, 4μm deep trench capacitor has a surface area seventeen times larger than a planar capacitor. This is turn yields a sixteen times higher capacitance. Super high density (64Mbit and higher) DRAMs, however, may be required to use CROWN, stacked trench or similar technologies to achieve usable circuits [14]. CROWN-type DRAM cells employ vertically stacked, convex capacitors in multiple conductor/dielectric

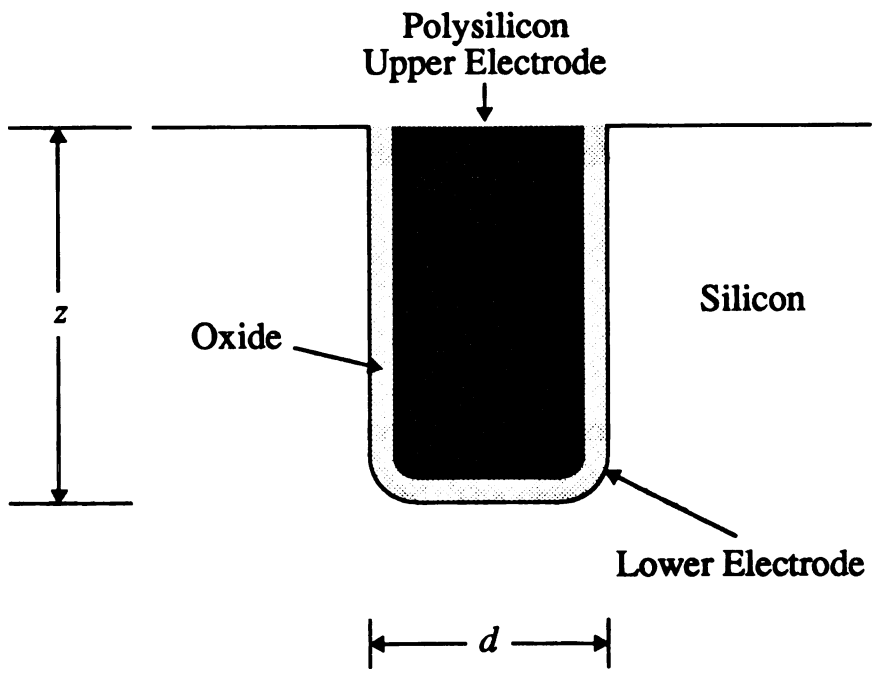


Figure 2.4 Trench Capacitor

layers. Stacked trench designs use multiple, thick dielectric layers with capacitors formulated in trenches in the *dielectric* layers [15].

2.3.3 Polysilicon Gate Definition

In ULSI polysilicon gate structures etching, selectivities of poly over SiO2 (as thin as 100Å) and photoresist should be greater than 60:1 and 3:1, respectively [8]. Near perfect anisotropy, high degrees of uniformity, and low damage must also be achieved. Low pressure, ion-enhanced chemistries found in ECR discharges provide the necessary conditions to meet these requirements. Low energy ions produced in ECR discharges also enhance the prospects for using ECR etching in poly gate definition as damage to the substrate will be lower.

2.4 Plasma Etching

A plasma is defined as a neutrally ionized gas with an equal number of positive and negative charges [16]. The chemical processes taking place in a plasma are used to create species for processing environments. Simple plasma reactors are typically composed of a set of conducting parallel plates in a chamber pumped down to low pressures (Figure 2.5). A high frequency voltage applied across the plates in the system accelerates electrons in the gas between the plates. If such an electron suffers an inelastic collision a number of reactions can occur that produce ions, radicals, and more electrons. The radicals and ions may then be used for a variety of purposes. Plasma etching processes have been grouped into 4 basic phenomena: 1) sputtering, 2) chemical, 3) ion-enhanced energetic, and 4) ion-enhanced protective

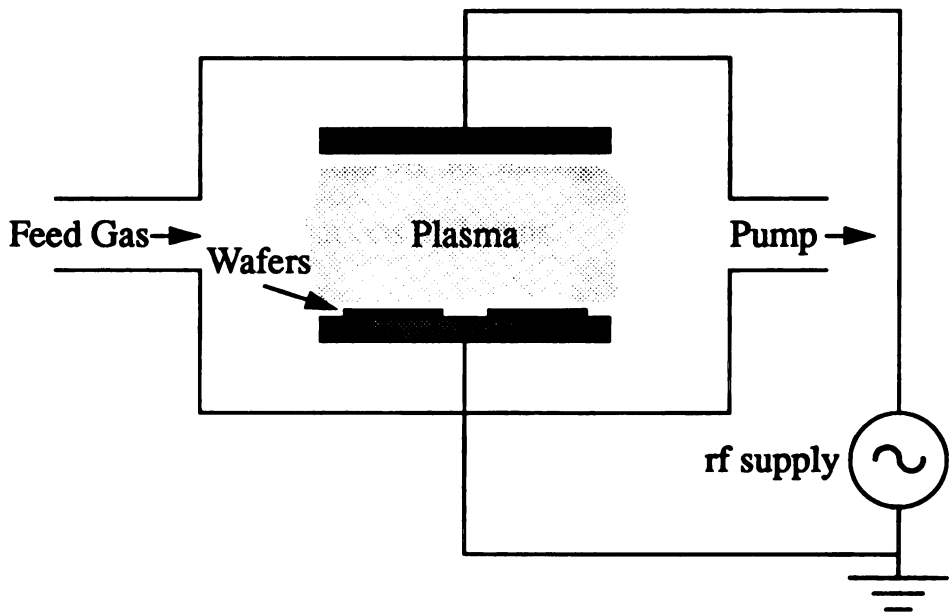


Figure 2.5 Generic rf Plasma Source

(Figure 2.6) [5].

2.4.1 Sputtering

In sputtering (Figure 2.6a), ions are accelerated through a potential drop and strike the surface of a substrate. Material is removed in a mechanical fashion. Bonds are broken and substrate atoms or molecules are liberated from the surface. At low pressures where the mean free path of liberated molecules is long enough, this ejected material will not be re-deposited on the surface. Sputtering is non selective and suffers from the need to have high energy (>75 eV) ions. These are known to damage the surface and introduce imperfections such as dislocations and traps.

2.4.2 Chemical Etching

Chemical (or spontaneous) etching (Figure 2.6b) is simply the chemical reaction of a neutral species with substrate material. If a volatile, high vapor pressure product forms, atoms can be removed from the surface of the substrate. Random thermal motion provides a flux of neutral free radicals from the plasma to the surface so the reaction rate will be somewhat temperature sensitive. A free radical is any species containing a single electron, rather than a pair, available for bonding. They typically exist only as short-lived intermediates in chemical reactions but can be produced in a plasma and sustained long enough to react with a substrate [17].

2.4.3 Ion-Enhanced Etching

Ion-enhanced *energetic* (Figure 2.6c) and *protective* (Figure 2.6d)

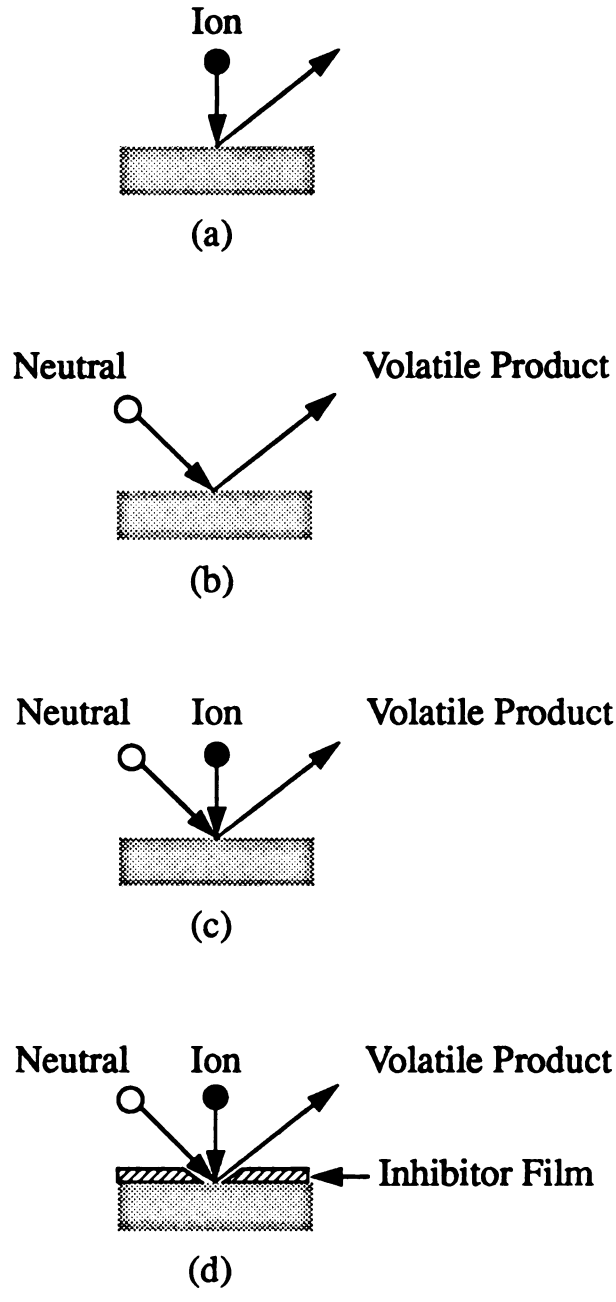


Figure 2.6 Plasma Etching Processes
a) sputtering, b) chemical, c) ion-enhanced energetic,
and d) ion-enhanced protective (after Flamm, reference 5)

plasma etching processes are somewhat similar in that they both require a flux of ions, in association with neutral radicals to remove substrate material. In the *energetic* model, ions alter the substrate to allow neutrals to form volatile products thus gasifying the material. Without the ion flux the neutrals alone cannot cause etching. The *protective* scenario assumes an inhibitor film coates the surface thus protecting it from the neutral radicals. The ion flux here weakens the inhibitor and allows free radicals to spontaneously combine and therefore gasify the material.

2.5 Fluorine Atom Silicon Etching

Fluorine atoms are known to spontaneously etch silicon and have been shown to produce SiF_4 and SiF_2 [18]. Flamm, et al have proposed two models for the liberation of silicon atoms from a <100> surface by fluorine atoms [19]. The first assumes a repetitive fluorine adsorption at the silicon surface until a high vapor pressure SiF_4 molecule is produced:

$$\text{Si(surface)} + \text{F(gas)} \rightarrow \text{SiF(adsorbed)} \qquad (2.1)$$

$$\text{SiF(ads)} + \text{F(g)} \rightarrow \text{SiF}_2\,\text{(ads)} \qquad (2.2)$$

$$\text{SiF}_2\,\text{(ads)} + \text{F(g)} \rightarrow \text{SiF}_3\,\text{(ads)} \qquad (2.3)$$

$$\text{SiF}_3\,\text{(ads)} + \text{F(g)} \rightarrow \text{SiF}_4\,\text{(g)} \qquad (2.4)$$

The second model proposes that SiF_2(ads) and SiF_3(ads) molecules may associatively desorb from the surface and produce SiF_4(gas).

Anisotropic etching of silicon has been observed in an SF_6 plasma at relatively low concentrations [20]-[23] and low temperatures [24]. Petit and Pelletier [25] have proposed a model to describe this anisotropic etching behavior. The model supposes that each of the two dangling bonds on a <100> silicon surface is filled by a fluorine atom but repulsive forces between fluorine atoms prevent them from occupying nearest neighbor positions. Accelerated ions destroy the ordered nature of the silicon surface and then SiF_2(ads) species may combine with other SiF_2(ads) species to form an SiF_4(gas) product according to the reaction:

$$SiF_2(ads) + SiF_2(ads) \rightarrow SiF_4(g) + Si \qquad (2.5)$$

The remaining Si atom in equation (2.5) may bond with other Si atoms or undergo successive fluorination and be liberated via equations 2.1-2.4. This phenomena may be grouped in the ion-enhanced energetic category (see section 2.4.3).

Since ions accelerated through a sheath potential or an applied dc-bias will have little or no horizontal energy, sidewall etching would be minimal. At higher pressures, lateral etching may be expected due to ion-ion, or ion-neutral elastic collisions yielding lateral ion velocities. Low temperature work performed by Tachi et al [24] has demonstrated purely anisotropic silicon etching in 100% SF_6 plasmas at -110°C. By controlling the temperature of the substrate, the reaction rate of spontaneous silicon etching on the sidewalls may be greatly reduced. The bottom surface etch rate is only slightly affected since

this is controlled mainly by ion enhanced chemistries. Etching selectivity of silicon over photoresist was also improved.

2.6 Etching Systems

Commercial plasma etching systems are typically classified according to pressure, geometry, generator frequency, and material position and load capacity [26]. Early etching systems were typically designed for high throughput, automated processes. Small 50 and 75 mm wafers did not present serious uniformity concerns so reactors were generally designed with mass production in mind. Barrel, parallel plate, and hexode reactors were the backbone of the industry in the 1970's and 1980's. Figure 2.7 is a diagram of two generic batch reactors.

2.6.1 Barrel Reactors and "Plasma Etchers"

Barrel reactors (2.7a) use an rf supply to generate radicals which thermally diffuse to the surface of the wafers and isotropically etch the substrate. These typically have a high capacity but uniformity is often quite poor and are mainly suited for applications such as photoresist ashing. Plasma etchers, are similar in design to Figure 2.5. The wafers are placed on the grounded electrode and the second, parallel electrode is rf-driven at 13.56 MHz. Operating pressures for both the barrel reactors and plasma reactors are typically around 1 Torr. At these pressures, sheath potentials on the wafers are low (<20 V) and they are typically isotropic etching devices.

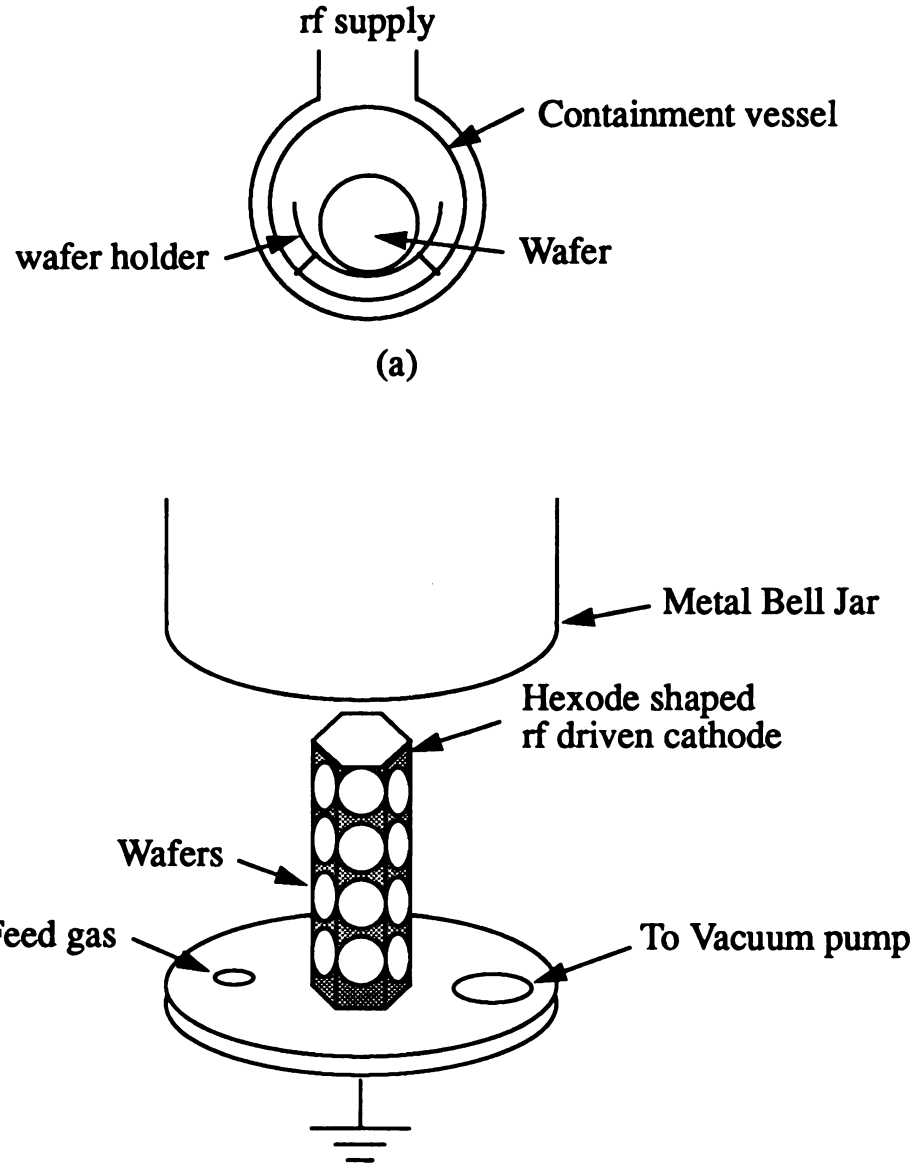


Figure 2.7 Generic batch reactors, a) barrel and b) hexode etcher (after Flamm, reference 26)

2.6.2 Reactive Ion Etchers

Reactive ion etching (RIE) designs are similar to parallel plate plasma etching systems except that the rf-driven electrode holds the wafers. The chamber may then be used as the grounded electrode. The large area of the chamber in conjunction with the smaller wafer holding platform yields much higher sheath potentials (20-500 V) than plasma, or barrel-type systems [27]. This design provides a better method for directing ion energies perpendicular to the substrate and can provide high levels of anisotropy. Drawbacks to this design are that it requires a large area to concurrently etch multiple wafers and it is likely to contaminate or damage wafers. High rf power levels are needed to sustain high plasma densities at operating pressures (from 5 mTorr to 100 mTorr) used in these reactors. This in turn imparts large amounts of energy to ions which can physically damage substrate surfaces. Sputtering from the walls of the reactor can also contaminate the substrates although this is minimized by making the anode (containment vessel) very large with respect to the cathode (wafer holder) and completely covering the cathode with wafers.

2.6.3 Hexode Reactors

Extending the design described in 2.6.2 vertically in the third dimension yields the hexode type reactor (Figure 2.7b). Wafers are vacuum or mechanically mounted to a hexagonal shaped cathode inside a metal bell jar. An rf bias is applied to the hexode and charged particles drift toward the wafers. This design also suffers similar drawbacks as the parallel plate etcher

but can achieve higher throughput due to its larger processing area and has a smaller footprint thereby reducing space. Hexode reactors and those described in 2.6.2 are typically referred to as Reactive Ion Etching (RIE) systems. This term is somewhat of a misnomer as it implies that ions are doing the etching when in fact they are only assisting the process.

2.6.4 Downstream Reactors

For chemical etching only, a plasma may be generated in a discharge region and allowed to flow through a transport region to a reaction region. If wafers are placed in the reaction region they will be exposed to a very limited number of high energy charged particles and may be isotropically etched or stripped. This design is called a downstream etcher [28]. Fine-featured semiconductor devices which are sometimes damaged by high energy particles are separated from the plasma generation. Microwave assisted plasma etching, as discussed in the following section is an expansion of this idea. By separating the discharge and processing region, many of the drawbacks of typical plasma etching systems can be avoided.

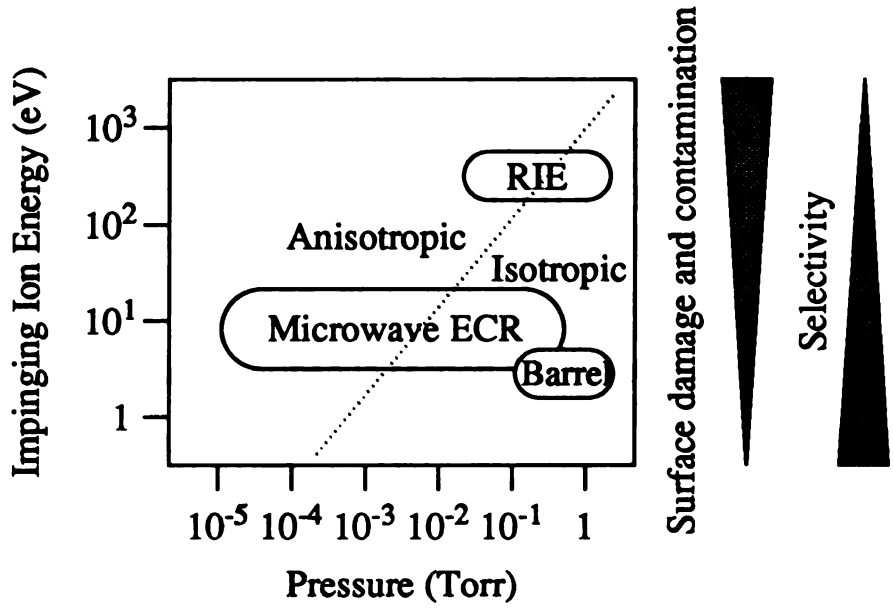
2.7 Microwave Plasma Assisted Etching

Microwaves are capable of accelerating electrons and, through collisions, producing plasmas. An important benefit of a microwave plasma is the separation of the discharge and processing region. This section will present some of the basic microwave plasma designs and give a summary of some of the etching work performed with systems similar to those used in this study.

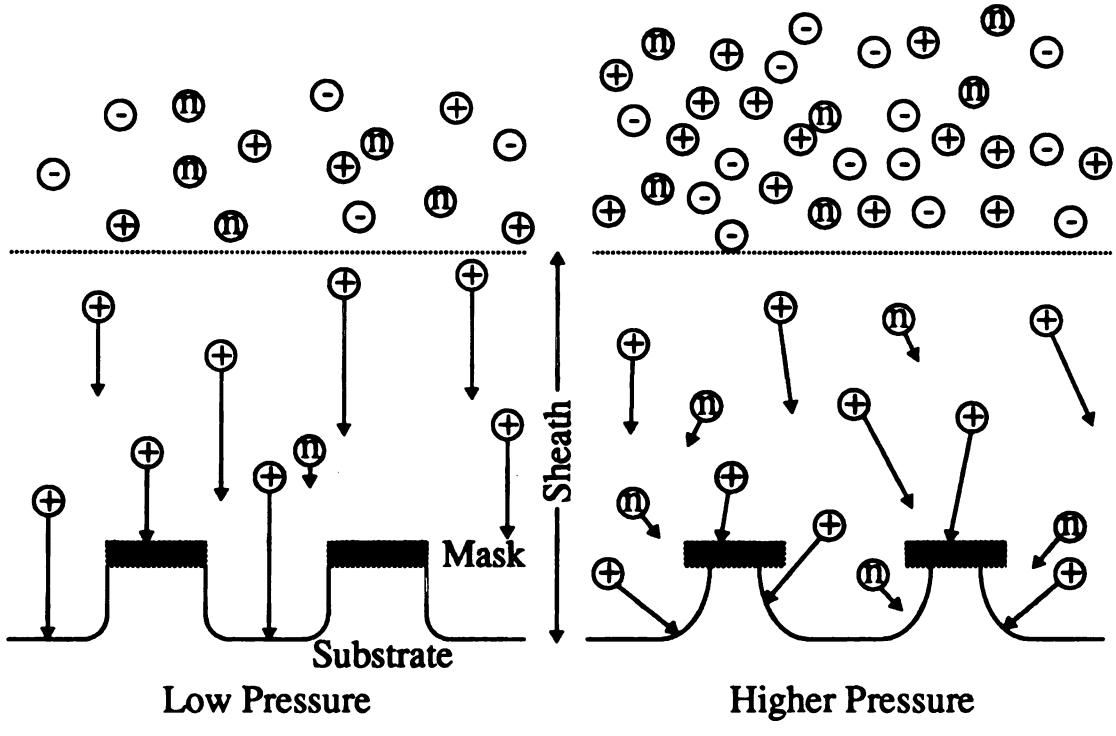
2.7.1 Rationale for Microwave Plasmas

As mentioned in section 2.6, early plasma etching systems suffer from drawbacks that, unless reconciled, will preclude their use in ultra small geometries. These geometries will require a combination of high anisotropy, high selectivity, low substrate damage, and high throughput. Microwave plasmas are uniquely positioned to offer these features by virtue of their ability to achieve high plasma densities at low pressures. Figure 2.8a shows that one may achieve high degrees of anisotropy by operating with high sheath potentials, as is the case for RIE. However, this causes a loss in selectivity and increase in substrate damage. Figure 2.8b shows that one may also achieve high degrees of anisotropy by operating a very low pressures. For rf plasmas, however, plasma densities decrease significantly at low pressures. Consequently, etch rates are low and throughput is reduced. Microwave plasmas combine high plasma densities at low pressures with low sheath voltages, thereby offering the ability to achieve high etch rates under highly anisotropic, low sheath voltage conditions. Additionally, since microwave plasmas do not use internal electrodes, contamination concerns are reduced.

An ideal reactor would produce cold (low eV), controllable, monoenergetic, and highly directional ions, operate at low pressures, and have a high uniformity over large (>200 mm diameter) areas. It should also have a high ratio of ions to neutrals to reduce the effect of spontaneous chemical reactions. Microwave plasmas offer a plasma generation means that is closer to this ideal than are current rf plasma etching systems.



(a)



(b)

Figure 2.8 a) Operation parameters and characteristics of conventional and microwave plasma etching, and b) simple model for etching profiles as a function of pressure (after Suzuki, Reference 29)

2.7.2 Microwave Plasma Sources

There are three different microwave plasma sources that have generated the most interest in the recent past. They are the Microwave Plasma Disk Reactor (MPDR), Distributed ECR Reactor (DECR), and the Divergent Field Reactor (DFR).

The MPDR, as described in section 4.2, is a resonant cavity surrounding a quartz dish in which a multi-cusp magnetic field provides the proper conditions for electron cyclotron resonance. The reader is referred to section 4.2 for a more detailed description.

The DECR is a design where long, thin antennae are arranged in parallel rows next to ECR strength magnets along the outer circumference of a cylindrical vacuum chamber. The plasma is generated in the ECR regions next to the antennae/magnet pairs and diffuses into the processing region [30]. This design can produce a uniform plasma over large areas but magnets are placed inside the discharge (which can cause contamination) and the system is reportedly hard to tune to reduce reflected power.

Perhaps the earliest developed ECR source is the DFR [31]. In the divergent field source, a waveguide is terminated in a transparent window (such as quartz) and surrounded by large solenoidal magnetic coils. The plasma is generated in this discharge region and diffuses out to the processing region. A downstream magnetic confinement structure, or *bucket*, is often used to increase the plasma uniformity in the processing region. The divergent field source is the oldest and perhaps the most well understood. Issues that

remain to be solved are the considerable problems associated with scaling up to large diameters and reducing the horizontal, or diverging ion velocities.

2.7.3 Previous MPDR Results.

A sample of previous etching studies using the MPDR has demonstrated anisotropic, low ion energy results. Hopwood, without using additional confinement magnets, has presented SF_6/Ar mixture (15% SF_6, 85% Ar) results with near perfect anisotropy at etch rates of 280 nm/min. A higher fraction (25%) of SF_6 is shown to increase the etch rate but anisotropy is concurrently reduced [1] [20] [21]

Constantine, et al [32], also without downstream confinement magnets, have demonstrated etching of III-V semiconductors in CH_4/H_2/Ar discharges. Etching of InP and InGaAs (15 cm downstream) was shown to increase linearly with increasing rf-bias but with low etch rates (12nm/min at 50v rf-bias, 1 mTorr, 250 Watts microwave power). Damage was measured with Schottky barrier diodes and found to be quite shallow (~20Å).

Issues that remain to be investigated include extensions to large diameter substrates, investigations of sub-micron feature etching, and ρ, ϕ dependant profiles and etch rates.

2.8 Summary

High fidelity anisotropic pattern transfer is a necessary requirement for VLSI and ULSI circuits. Trenches in silicon have been shown to be useful, and perhaps necessary, for a number of different applications. Also mentioned are

requirements for polysilicon gate etching. Currently, plasma chemistry is the only tool available for high density, anisotropic silicon etching. Etching in the 1970's and 1980's utilized rf-plasma systems where the processing region is inherently part of the generation region. In order to reduce damage and provide a more controllable system, downstream reactors may be necessary. The rational for microwave plasma etching and various microwave plasma systems were introduced and previously published results using the MPDR were summarized.

Chapter 3

Sample Preparation

3.1 Introduction

Integral to any etching investigation is the establishment of a masking pattern on the substrate which defines the regions to be etched. This chapter describes the methods used in this study to establish aluminum and photoresist patterns on silicon wafers prior to plasma etching. Lithography, the transfer of a pattern from an original to a copy, is one of the dominant and controlling factors in state-of-the-art high density integrated circuits [27]. Dynamic Random Access Memory (DRAM) chips are projected to reach the 1 Gbit milestone by the year 2001. To reach this goal, many believe that minimum feature sizes will reach 0.1μm with x-ray, ion, and electron beam exposure tools eclipsing today's step and repeat projection aligners [33]. In addition to using shorter wavelength exposure methods, new paradigms including self-aligned sidewalls and phase shifting masks may also play a significant role [34]. Companies wishing to compete in this market must spend hundred of millions of dollars developing these technologies. This is clearly out of the reach of most university research programs. Fortunately, engineering advances in contact lithography (a system the silicon industry abandoned in the 1970's) have made sub-micron exposure tools available at relatively low cost. A recently acquired mask aligner (Karl Suss MJB3) with state-of-the-art features was used in this study to pattern silicon with sub-micron lines. This establishes the silicon region to be exposed to the plasma etchant. Photoresist selection and resist process development are discussed in sections 3.2, 3.3, and

3.5 through 3.7. Sections 3.6 and 3.7 describe the aluminum lift-off technique necessary to generate sub-micron aluminum lines for anisotropy studies.

3.2 Resist Selection

The primary development tool was a Karl Suss MJB3 contact mask aligner. The MJB3 is fitted with UV300 class optics. A mercury vapor light source integral to the aligner provides deep UV light (λ=280-350nm) with primary peaks at 313nm and 334nm. The majority of industrial optical step and repeat aligners use I, H, and G-line sources (365, 405, and 436nm) [35]. As a consequence, very few deep UV photoresist are readily available.

Four brands of photoresist were investigated to determine the greatest flexibility and process latitude; AZ 5200 from Hoechst Celanese [36], PR 1024 from MacDermid[37], S1800 and 1450J from Shipley [38] [39]. Process latitude refers to the ability to achieve high quality, repeatable results without strict control over all of the input parameters (bake times and temperatures, ambient temperature and humidity, and exposure energy.) Typical development times and equipment requirements were also evaluated to ensure a viable photoresist process. Based upon these considerations, the AZ 5200 series was selected as best suited for our laboratory and equipment.

AZ 5200 is a novalak resin based photoresist which can be used in a positive or negative tone providing a high level of flexibility from a single mask. Although not specifically tailored for deep UV processing, the AZ5200/ deep UV combination has been used at other universities with favorable results[40]. Three solubilities are available and the 5209-E was chosen. The

"09" refers to a final film thickness (0.9μm) after a 4000 rpm/30 second spin and a 90°C/30 minute softbake.

3.3 Wafer Preparation

For multiple and single 75 mm silicon wafer experiments the substrates were initially rinsed in a 50:1 Deionized water(DI):HF solution to remove a native oxide. Processing continued with a boiling trichloroethylene clean, followed by a degrease and a demetal etch [41]. An acetone, methanol, DI water rinse with a vapor phase isopropyl alcohol (IPA) final rinse assured maximum particle removal [42]. Any remaining water on the hydrophobic silicon surface is pulled down into the IPA/water mixture by the sheeting action of the condensing IPA (see Figure 3.1). When removed from the beaker, the IPA quickly evaporates leaving a dry silicon surface. In addition to helping remove surface particles, the IPA rinse has the advantage of not requiring a nitrogen gun drying procedure. Wafers are dehydrated for 45 minutes at 200°C to remove any remaining adsorbed surface water.

After a cooldown period of 15 minutes, a liquid phase hexamethyldisilazane (HMDS) wafer prime was used to ensure high photoresist adhesion rates. HMDS chemically reacts with surface water vapor to form an ammonia gas and leaves behind a monolayer of HMDS. AZ5209-E is then spun on at 4000 RPM for 30 seconds. A short softbake (30 minutes) at 85°C facilitates solvent removal while leaving the photoresist susceptible to future UV light and thermal processing.

Two very different procedures are described in sections 3.5 and 3.6 to

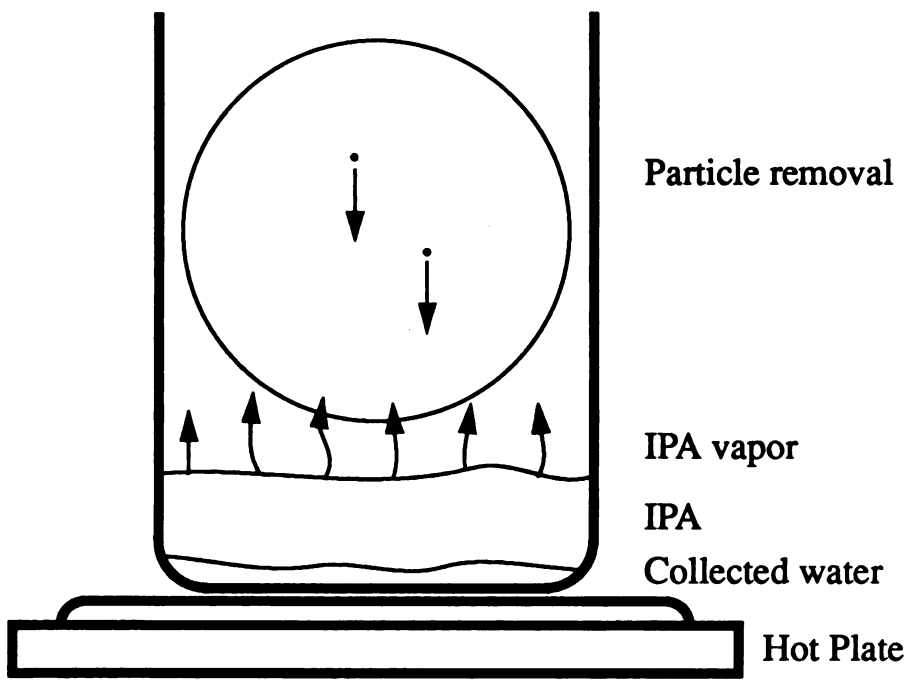


Figure 3.1 Vapor Phase IPA water and particle removal. The IPA is heated to near boiling. Its vapor condenses on the wafer and removes water droplets and particles.

transfer the mask pattern to the photoresist in a negative and positive tone process.

3.4 Mask Description

The mask used for the majority of the studies herein was purchased from Microtronics, Inc. Being a test mask, it employs many features for evaluating PR procedures, etching uniformity, and anisotropy. It is made from anti-reflective chrome on a synthetic quartz substrate. Low expansion and white crown glass are considerably cheaper, but both have transmittances of less than 35% at 314nm. Synthetic quartz has a transmittance of over 90% well below 200nm.

The primary features for use in evaluating anisotropy and uniformity are the chevrons that dominate the middle of each die (Figure 3.2). The smallest set of chevrons have four lines with equal spaces at a width of 0.6 μm. This pattern is repeated for 1.0 μm, 2.0 μm, 3.0 μm, 4.0 μm, and 5.0 μm lines. The circles to the right of the chevrons represent via or contact cuts. A "dagger" structure, not shown in Figure 3.2, at the top of the die begins at 5 μm wide and tapers down, in 0.5 μm steps, to 1.0 μm, then to 0.6 μm. The dagger is visible in Figure 3.5. A "comb" pattern at the bottom left is useful for evaluating sharp corners and positive/negative features. Stigmatisms in the UV light source are readily observable due to the orthogonal nature of the chevrons. Precise tuning mechanisms on the MJB3 allowed us to minimize any such aberrations.

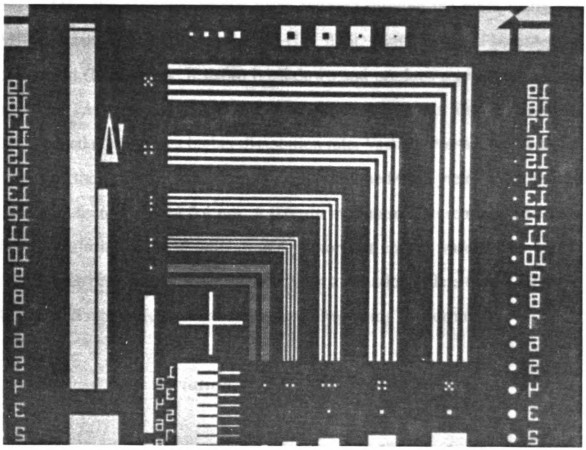


Figure 3.2 Photomask used in etching studies

3.5 Positive Tone Process

Positive tone processing refers to the ability to create a copy of the mask on the wafer where photoresist lines represent opaque areas on the mask (Figure 3.3a).

After the softbake, wafers were exposed through the mask using the MJB3 mask aligner. Exposure to UV light stimulates a PhototActive compound (PAC) in the resist to breakdown and produce a relatively strong acid. The PAC originally acted as a dissolution inhibitor but after breakdown, the exposed areas have a higher dissolution rate. Vacuum contact between the mask and the wafer with the deep UV optics on the MJB3 yields a theoretical minimum feature size of 0.4 μm. A 0.6 μm minimum feature mask was used for the majority of the aluminum and photoresist coated wafers. The MJB3 light source provides 14.8 mWatts/cm^2 with a variation of less than 2.5% over 45 cm^2 (75 mm wafers). Variation is measured using the formula

$$Variation = \frac{High - Low}{High + Low} \times 100\%$$

Exposure times were 45 seconds followed immediately by development in a 1:1 solution of AZ312 Metal Ion Free Developer and DI water [36]. Development times varied from 30-45 seconds and were followed by a DI water quench and a 3 minute DI water rinse.

Plasma processing is a fairly hostile environment which requires a very robust masking material. Surface temperatures of the wafers on the non-

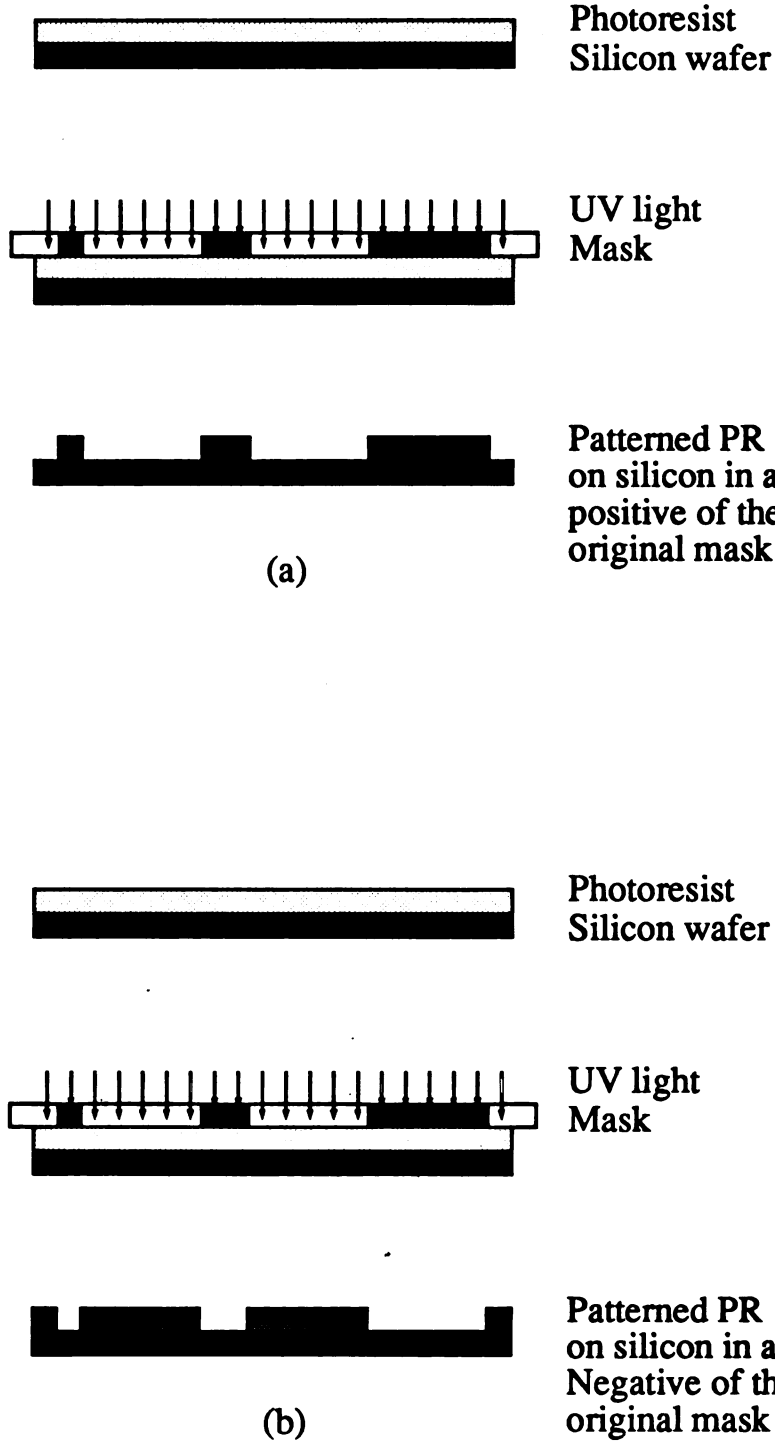


Figure 3.3 Positive tone (a) and Negative tone (b) photoresist processing

cooled platter in our ECR reactor are estimated to rise above 350°C. In order to achieve etching selectivities high enough to use photoresist as a viable mask, a deep UV curing procedure was implemented.

The finished wafers were blanket exposed to deep UV light for 15 minutes (0.22 J/cm^2). The deep UV light is absorbed by the novalak resin in the outer shell only. This forms a hard, polymerized surface which can withstand a high temperature bake. The wafers were baked for 40 minutes at 200°C. The high temperature bake is the final curing step which yields an extremely hard PR pattern [43]. No noticeable spreading or critical dimension (CD) loss was observed after this process.

3.6 Negative Tone Process

Negative tone processing refers to the ability to create a copy of the mask on the wafer where photoresist lines represent transparent areas on the mask (Figure 3.3b).

After the process outlined in section 3.2 (wafer preparation), the wafers underwent an image-wise (through the mask) exposure using the MJB3. This activated the PhototActive Compound (PAC) in the resist in such a fashion as to provide a "solubility gradient" in the PR. The wafers were then given a post-exposure, reversal bake followed by a cooldown and a blanket UV exposure.

Upon initial exposure, the PAC breaks down and produces an acid similar to the positive tone process. The high temperature post-exposure bake encourages the acid to diffuse into the resin system of the thin film. The high

temperature also causes acid catalyzed cross-linking. This cross-linking acts as an inhibitor and reduces the solubility in exposed areas. The short image-wise exposure produces acid mainly at the top of the resist surface and therefore the solubility increases with increasing depth into the PR. The temperature and time of the post-exposure bake control how much of the photogenerated acid is cross-linked. This controls the generation and profiles of submicron features [44] [45]. A flood exposure after the PEB increases the solubility of the unexposed resist by breaking down the PAC thereby reducing the development time. Since this is not followed by any baking steps, no cross-linking occurs in the unexposed regions and this area has a much higher development rate [35]. A 1:1 solution of AZ312-MIF Developer and DI water followed by a DI quench and rinse was similarly used.

At this point, as a result of the solubility gradient, the photoresist exhibited a "negative sidewall", or re-entrant profile as shown in Figure 3.4. The sharp rise at the edges of the photoresist is a result of cleaving the silicon to view the profile. Table 3.1 shows the orthogonal chart used to determine the optimum process parameters. Early flood exposure times were gauged by measuring the dissolution rate of the photoresist. Wafers were coated with photoresist and exposed to varying amounts of light. The dissolution rate was determined by measuring the time taken to remove the entire layer of photoresist in a 1:1 developer solution. Wafer #6 proved to have the best combination of adhesion and undercutting in the resist sidewall. Adhesion proved to be the major determining factor as well as the easiest to observe. This recipe was used throughout the study to pattern wafers in a negative tone.

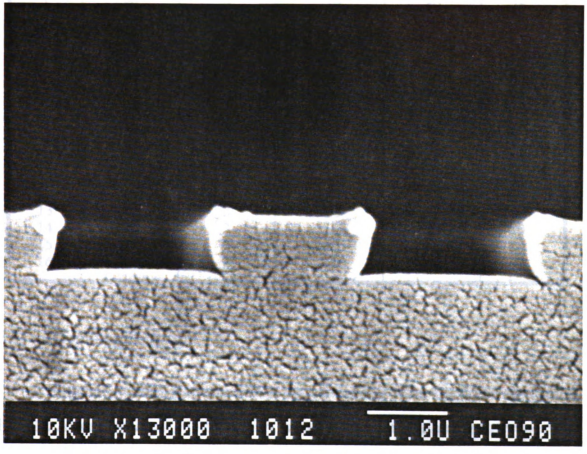


Figure 3.4 2μm PR lines on silicon exhibiting the negative profile

Table 3.1 AZ5209 Orthogonal chart

Wafer #	Softbake Temp (°C)	Image Exp. Time (sec)	Reversal bake Temp (°C)	Time (min)	Flood Exp. Time (sec)
1	80	2	95	40	75
2	80	2	100	40	75
3	80	2	105	40	75
4	80	2	110	40	75
5	85	2	95	45	75
6	85	2	100	45	75
7	85	2	105	45	75
8	85	2	110	45	75
9	85	3	95	45	80
10	85	3	100	45	80
11	85	3	105	45	80
12	85	3	110	45	80
13	90	2	95	40	80
14	90	2	100	40	80
15	90	2	105	40	80
16	90	2	110	40	80

3.7 Aluminum Lift-off

Finished wafers patterned in a negative-tone were used for aluminum lift-off. After development the wafers were placed in the aluminum evaporator which was pumped down to pressures of 10^{-8} Torr for 8 hours to assure removal of any water vapor on the silicon surface. Approximately 4200Å of aluminum were evaporated on the wafers. The negative sidewall profile was highly desired as it allowed us to evaporate aluminum over the entire surface of the wafer leaving substantial gaps in the aluminum film. Wafers were emerged in an ultrasonic bath of AZ327 Photoresist Stripper to dissolve the underlying layer of photoresist. This procedure proved quite reliable for

producing aluminum patterns on silicon wafers. Figure 3.5 is an SEM photograph of a single die on a 75 mm wafer. Aluminum line features as small as 0.6 μm in a positive tone image of the original mask can be seen. Figure 3.6 is a conceptual diagram showing the aluminum lift-off technique employed for this study.

3.8 Substrates from Delco Electronics

Delco Electronics, of Kokomo Indiana, supported this research by providing patterned 125 mm wafers for uniformity and anisotropy studies. Twelve wafers were donated with 8000Å thick RIE patterned oxides. Figure 3.7 shows an SEM photograph of a portion of the surface of the wafer where anisotropy studies were performed. These wafers were used in addition to the 75 mm diameter patterned wafers described earlier in this chapter.

3.9 Summary

This chapter has described the procedure for fabrication of the substrates used in the etching anisotropy and etching uniformity studies of chapter 5. Photoresist selection, processing, and evaluation was detailed with the goal of achieving a wide process latitude. Sub-micron patterns were consistently achieved with a negative-tone aluminum lift-off recipe. A sub-micron photomask used for defining features was also described.

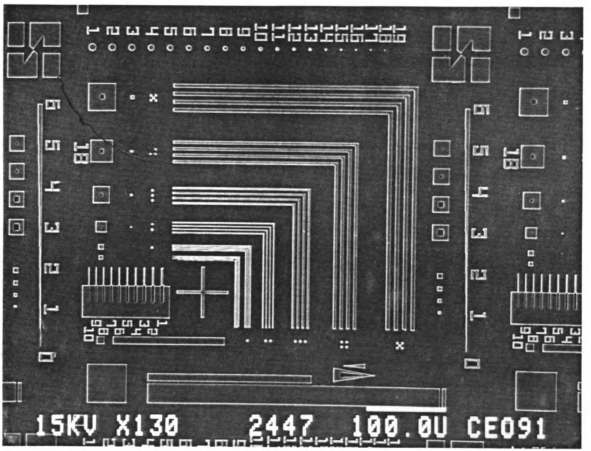
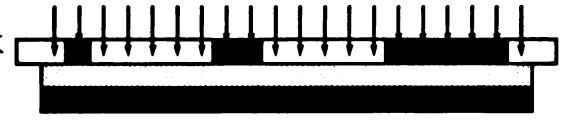


Figure 3.5 SEM photograph of aluminum on silicon

1) Clean a silicon wafer and spin on a thin layer of photoresist.

2) Shine ultra-violet light through a mask into the photoresist (2 seconds).



3) Bake the wafer in an oven at 100°C for 45 minutes.

4) Flood expose the wafer to ultra-violet light for 75 seconds.

5) Develop the wafer. This selectively removes soluble photoresist.

6) Evaporate aluminum onto the wafer.

7) Strip the underlying photoresist to selectively remove the aluminum.

8) Finished wafer has 0.6μm aluminum lines.

Figure 3.6 Aluminum lift-off process using an image reversal bake

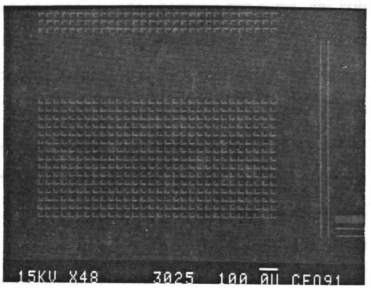


Figure 3.7 SEM Photograph of
Delco Supplied Wafer

Chapter 4

Etching Procedures

4.1 Introduction

Microwave Plasma Disk Reactor (MPDR) ECR plasma sources similar to those used in this study have been described extensively by Sze, Root, Asmussen, and Hopwood [23] [46] -[48]. The reader is referred to these for operational and characterization studies. Measurements used to quantify and compare plasma sources include operating pressures, gas compositions and flow rates, ion and electron densities and energy distributions, and application-specific performance issues. It is with the latter, performance of the ECR source as an etching tool, that this focuses upon. Although not fully understood, systems similar to those used in these experiments have been described elsewhere and a general relationship between input power, gas compositions, and substrate conditions have been established [1]. The MPDR ECR sources used herein are specifically treated as tools to study silicon etching uniformity and anisotropy.

4.2 Etching system

The MPDR is a versatile plasma source that may quickly and conveniently be adapted to a variety of host systems. Any processing chamber with a large enough entrance hole may be adapted to the MPDR with relative ease. The system used in these experiments is schematically diagramed in Figure 4.1.

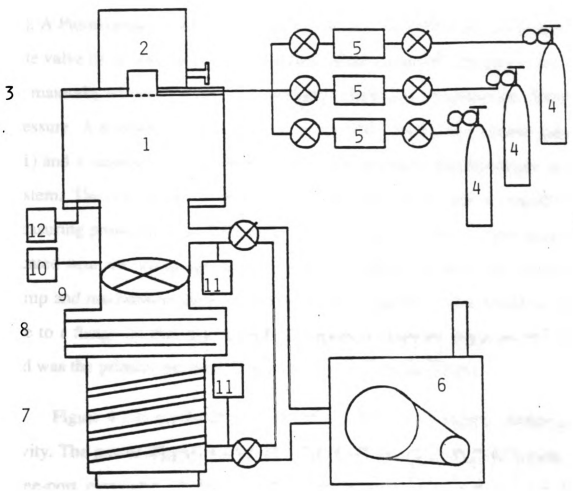


Figure 4.1 Vacuum and Gas Handling Components of the MPDR Plasma Processing System
(After Hopwood, Reference 1)

A 21h x 18d inch Pyrex cylinder serves as the processing chamber (1). The MPDR (2) rests on top of an aluminum baseplate (3) with a 37 cm diameter hole. Feed gasses (4) are mixed and introduced to the MPDR baseplate via a 3-channel mass flow controller (5). A mechanical pump (6) is used to pump the chamber from atmospheric pressure to approximately 50 mTorr, after which it is switched over to service the output of a diffusion pump (7). A Freon cooled baffle (8) is installed between the diffusion pump and the gate valve (9) to minimize back streaming of the pump oil. The gate valve can be manually adjusted to alter the pumping speed, and therefore the chamber pressure. A miniature ion gauge (10), along with two thermal couple gauges (11) and a capacitance manometer (12) supply pressure measurements in the system. The ion gauge is located near the gate valve and is capable of measuring pressures from 10^{-2} to 10^{-8} Torr. The first thermal couple gauge is located near the ion gauge and the second is placed between the diffusion pump and mechanical pump. The manometer, connected via a stainless steel line to a flange on the bottom of the chamber, is accurate down to 10^{-5} Torr and was the primary pressure gauge used in these experiments.

Figure 4.2 is a schematic of the microwave power source, circuit, and cavity. The power supply (1) is a 1200 Watt Micronow 2.45 GHz source. A three-port circulator (2) directs power from the supply to the cavity (3). Reflected power is absorbed into a dummy load (4). A dual-directional coupler (5) samples the forward and reflected power. Twenty dB attenuators (6) are placed in-line on the coupler and power is displayed on two Hewlett-Packard HP432A (7) microwave power meters. Rectangular waveguides (8) are used

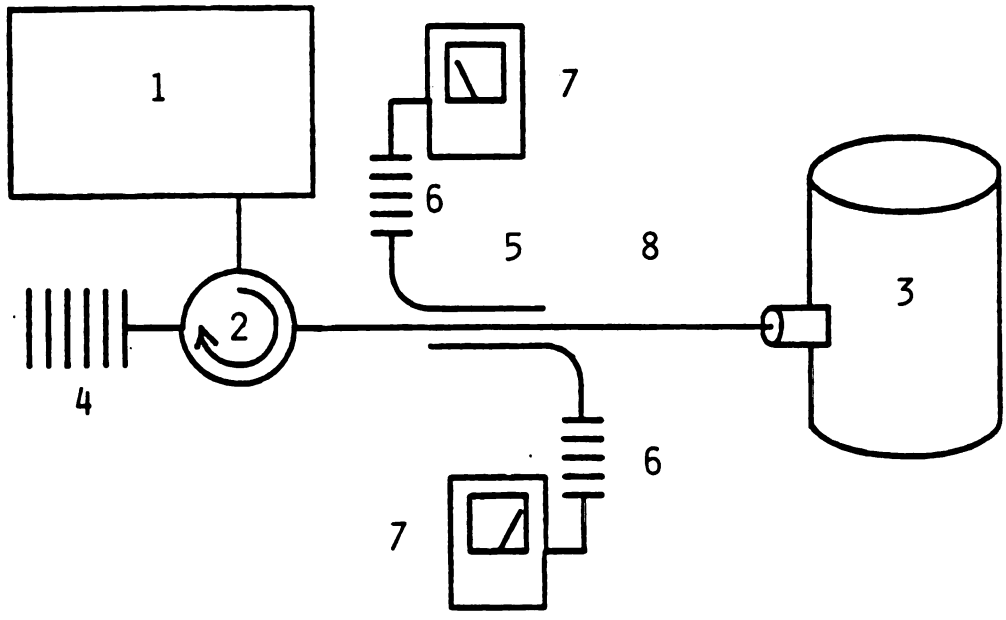


Figure 4.2 Microwave Power Supply, Circuit, and Cavity
(after Hopwood, Reference 1)

for the transmission circuit to allow high power operation.

4.3 Wavemat MPDR 325 Description

As substrate diameters in silicon integrated circuits continue to grow, the need for larger processing tools grows as well. The primary plasma source used in this work is the Wavemat model MPDR 325. Figure 4.3 is a profile view of the 325 and related equipment.

The resonating cavity (1) is a 37cm ID aluminum tube. A 3/4" OD input probe (3) couples microwave energy from a rectangular waveguide into the cavity. The position of this probe (*Lp*) may be altered by an external tuning screw. The top of the cavity (2), or sliding short, may also be adjusted to tune the cavity. This measurement is diagrammed as *Ls*. When properly adjusted, the input probe and the sliding short can tune the cavity to match impedances between the waveguide and the plasma. The baseplate (4) holds twelve magnets (8) which provide the magnetic fields necessary for ECR. The alternating magnets are water cooled (11) to prevent thermal degradation and have pole face fields in excess of 3 kG. For microwave excitation at 2.45 GHz, electron cyclotron resonance occurs at

$$B = \frac{m\omega}{e} = 875 \ Gauss$$

The resonating cavity is at atmospheric pressure and a quartz dish, transparent to microwaves, is the barrier to the vacuum system and processing environment. Beneath the 25 cm diameter quartz dish (6) the working gasses

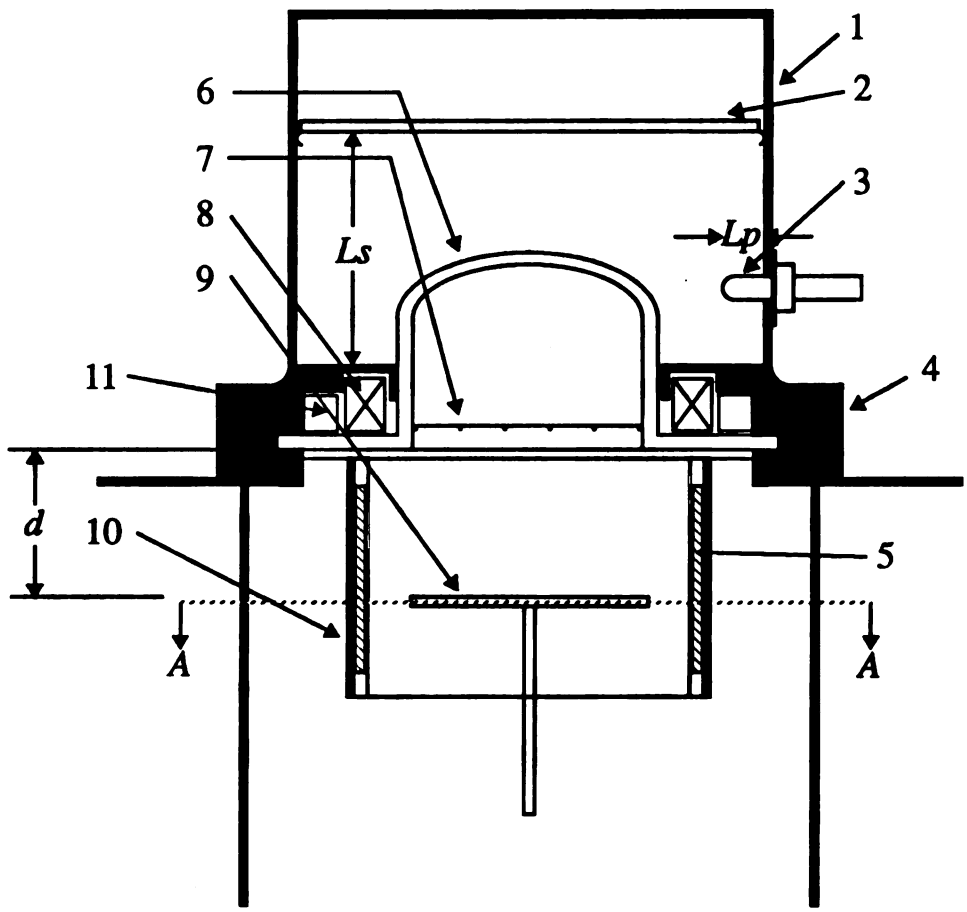


Figure 4.3 Experimental Setup for Silicon Etching

are introduced through 12 equally spaced pinholes (7).

Additional confinement magnets (10) are suspended beneath the baseplate. The structure is a 28cm OD, 22cm long aluminum tube. Twelve six inch long Alnico bar magnets (5) are symmetrically placed around the outside of the tube. Magnetic fields are 1 kG on the pole faces, 100 G 2 cm radially from the inner surface of the structure, and are virtually zero 4 cm inward. Magnets in both the additional confinement structure and the baseplate are oriented in such a fashion that one of the poles is always facing in toward the axis of the system. Adjacent magnets, either horizontally or vertically, are opposite to each other in terms of polarity. In the discharge region this creates multiple zones in which the electron cyclotron resonance conditions are satisfied. Downstream, in the confinement structure, the magnetic field configurations serve to limit species diffusion, and therefore surface recombination, on the walls. Plasma density and etching uniformity is higher with the downstream magnets in place.

The wafer holder (9), a 18.54 cm diameter aluminum disk, can be mounted at any position downstream (*d*). The platform is negatively biased with respect to the processing chamber (baseplate, MPDR, etc.). A cross-sectional view (*A-A*, see Figure 4.3) of the downstream confinement structure and wafer holder is shown in Figure 4.4. This figure shows a multiple 75 mm wafer (12) experiment. The bar magnets (5) can be water or air cooled through cooling channels (14) that run the length of the structure.

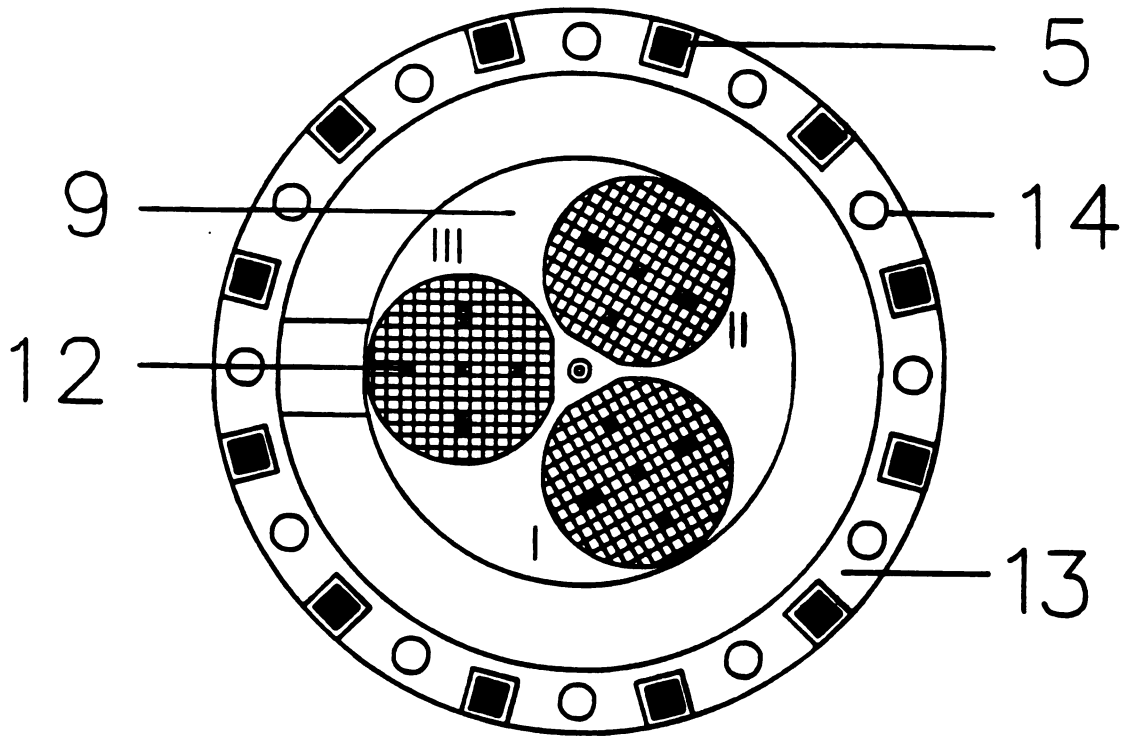


Figure 4.4 Top View of Section *A-A* in Figure 4.3
(After Sze, et al, Reference 23)

4.4 Seven Inch Cavity Description

A cavity previously investigated by Hopwood [1] is an earlier design that was used in our preliminary etching studies. This cavity is a 17.8 cm (7 inch) diameter brass cylinder with a 9 cm ID quartz cup. Eight water cooled magnets with pole face strengths of approximately 3 kG surround the discharge region. The baseplate has eight pinholes to supply gas to the chamber.

The discharge region of the Hopwood cavity is much smaller than that of the MPDR 325. It is therefore not suitable for uniformity studies over large areas. The smaller cavity has the advantage of being much lighter than the 325 and as such, it was used for preliminary measurements on segments of wafers to estimate etch rates and anisotropy.

4.5 Choice of Etching Gasses

Although Freons (CF_4, CHF_3, CF_3Cl, etc.) are often used as an etchant in wafer production, the gasses used in this study were SF_6 and argon. Any chlorine based gasses will attack many of the aluminum components in the etching system and are therefore avoided. Previous studies by Hopwood [1] have investigated silicon etching with CF_4 and SF_6 and found higher etch rates using SF_6. This may be due to a larger number of neutral Fluorine atoms available in the plasma. Throughout our work, small fractions SF_6 (5%-10%) were used in conjunction with argon.

4.6 Procedures

For a given resonant cavity mode, a proper match will reduce reflected power and maximize the power transfer to the cavity. For the 7 inch cavity, the TE_{211} excitation mode was used based on previous experience. Reflected power could generally be reduced to less than 5% of incident power. With the MPDR 325, because of the larger cavity diameter, cavity modes at 2.45 GHz are separated by only very small variations of the sliding short position *Ls* and probe position *Lp*. Under processing conditions, the 325 is likely operating in a multimode fashion. Care was taken to properly record the position of the sliding short and the input probe in order to properly repeat operating conditions for etching comparisons. With the 325, reflected power levels were typically in the range of 10-20% of the incident power at *Ls*=21.5 cm, *Lp*=1.4 cm. All power measurements given in the performance studies are incident minus reflected.

The backside of the wafers were painted with a conducting paint to ensure good electrical contact. After placing wafers on the platform, the system was pumped down to approximately $5x10^{-6}$ Torr. Argon was then introduced and the gate valve closed to increase the pressure in the chamber. The required bias is then applied to the substrate and the microwave power is turned on to start a plasma. The gate valve was immediately opened to reduce chamber pressure to the operating conditions. The wafer bias was turned on and SF_6 was slowly introduced. The impedance of the plasma is a function of the pressure so the MPDR must be concurrently tuned as the SF_6 flow increases.

When the etching was completed, the microwave power and SF_6 flow are halted. The argon was allowed to flow for approximately one minute to help remove any residual sulfur or fluorine gasses. Next, the argon and bias are shut off, the gate valve closed, and the system was vented with dry nitrogen.

Throughout the experiments latex gloves were worn to prevent contamination of the processing chamber and to protect the operator. Acetone was used to clean the wafer holder after processing was complete. The graphite paint on the backside of the wafers was easily removed in an ultrasonic bath of acetone.

4.7 Pattern Evaluation

A surface profileometer (Dektak IIA) and scanning electron microscope (SEM) were the two primary evaluation tools used. The profileometer has a 12.5μm wide stylus that can be used to record etch depths over an entire wafer provided the features are large enough. Samples are then carefully cleaved and mounted perpendicularly on aluminum stubs to observe profiles in the SEM). Both instruments have very high degrees of accuracy but care must be taken to interpret the results correctly. The SEM, for example, can appear to show etch depths that are more or less than actual if the sample is not mounted perpendicular or cleaved properly. Also of issue is SEM calibration.

4.8 Summary

This chapter has presented the experimental techniques and systems

used in our silicon etching study. The processing chamber, gas delivery system, MPDR, and wafer handling system were diagrammed and described. Also presented was the method used to etch samples. Chapter 5 presents results obtained from the system described herein.

Chapter 5

Etching Results

5.1 Introduction

Early investigations of new equipment such as the MPDR ECR etching tools generally consist of trying to establish patterns between the input parameters (power levels, etching gasses, etc.) and observed results (profiles, etch rates, etc.). In this section we present profiles, etch rates, loading effects, and positional effects obtained in our research using 2.45 GHz microwave excitation. Also included is preliminary information on surface contamination using depletion layer capacitance studies.

5.2 Etching with Aluminum Masks

Aluminum was used as a masking material due to its robust character in a fluorine plasma. The silicon substrate may then be etched with a very high selectivity over the aluminum. Initially, wafers were evaluated using a small cavity. The 325 source was subsequently employed for large diameter studies.

5.2.1 Seven Inch Cavity Aluminum Mask Results

The smaller cavity has been previously characterized by Hopwood for large features (>10 μm) and small wafer diameters (up to 75 mm). In our current work, small patterns (0.6 μm - 5 μm) were etched on full 75 mm wafers as an initial investigation. The large wafer holding platform (18.54cm diameter) was placed 32 mm below the d=0 position as defined by Hopwood [1]. Microwave power levels of 250 Watts, 10% SF_6, 90% Ar, gas mixtures,

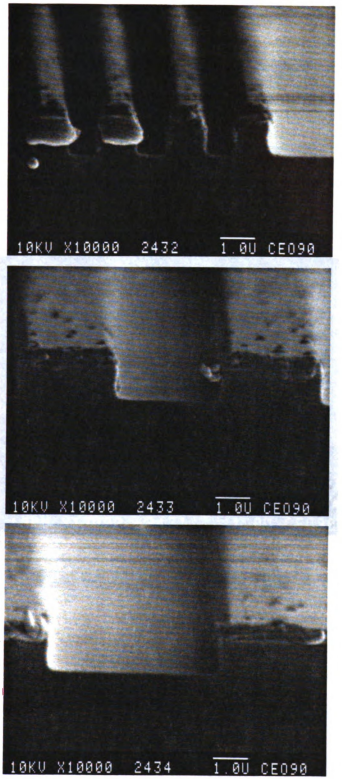
with a -50 volt d.c. bias yielded etch rates of 150 nm/min. Uniformity over a 75 mm diameter was poor ($\sigma > 20\%$) but expected with the small diameter discharge and short source to substrate distance.

5.2.2 MPDR 325 Aluminum Mask Results

Large diameter studies were completed using three 75 mm wafers uniformly placed on the 18.54 cm diameter platter as shown in Figure 4.4. A representative set of pictures for sub-micron, 3 μm, and 5 μm wide trenches, etched at 2.45 GHz, is shown in Figure 5.1.

Figures 5.1b and 5.1c clearly show some damage to the aluminum surface which is believed to be caused by minute amounts of liquid trapped between the silicon and aluminum. As the wafer is heated in the etching process, the liquid forces its way out through the aluminum. The small bubbles seen on the aluminum surface are where the liquid expanded and the vapor broke through. The ragged front edge of the aluminum is a result of cleaving the wafer while the side edges are representative of a slightly ragged photoresist pattern. This is attributed to an early problem achieving good vacuum contact between the mask and wafer in the MJB3.

Figure 5.1a shows some evidence of the so called "keyholing" effect. Keyhole-type etching is diagrammatically shown in Figure 5.2a where, as the etching progresses, the trench is slightly widened or bowed. A number of causes have been suggested and are outlined as follows; 1) an increasing temperature of the wafer as time progresses causes more random thermal motion of ions and neutrals in the trench, 2) electric field effects in trenches



(a)

(b)

(c)

Figure 5.1 a) sub-micron, b) 3μm, and
c) 5μm wide trenches etched in silicon
(0.7 mTorr, 600 Watts Microwave Power, -50 volts, *Ls*=21.5cm, *Lp*=1.4cm)

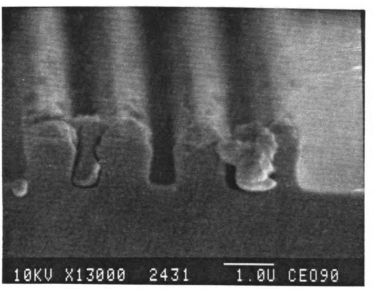


Figure 5.1 d) 0.5 micron trenches

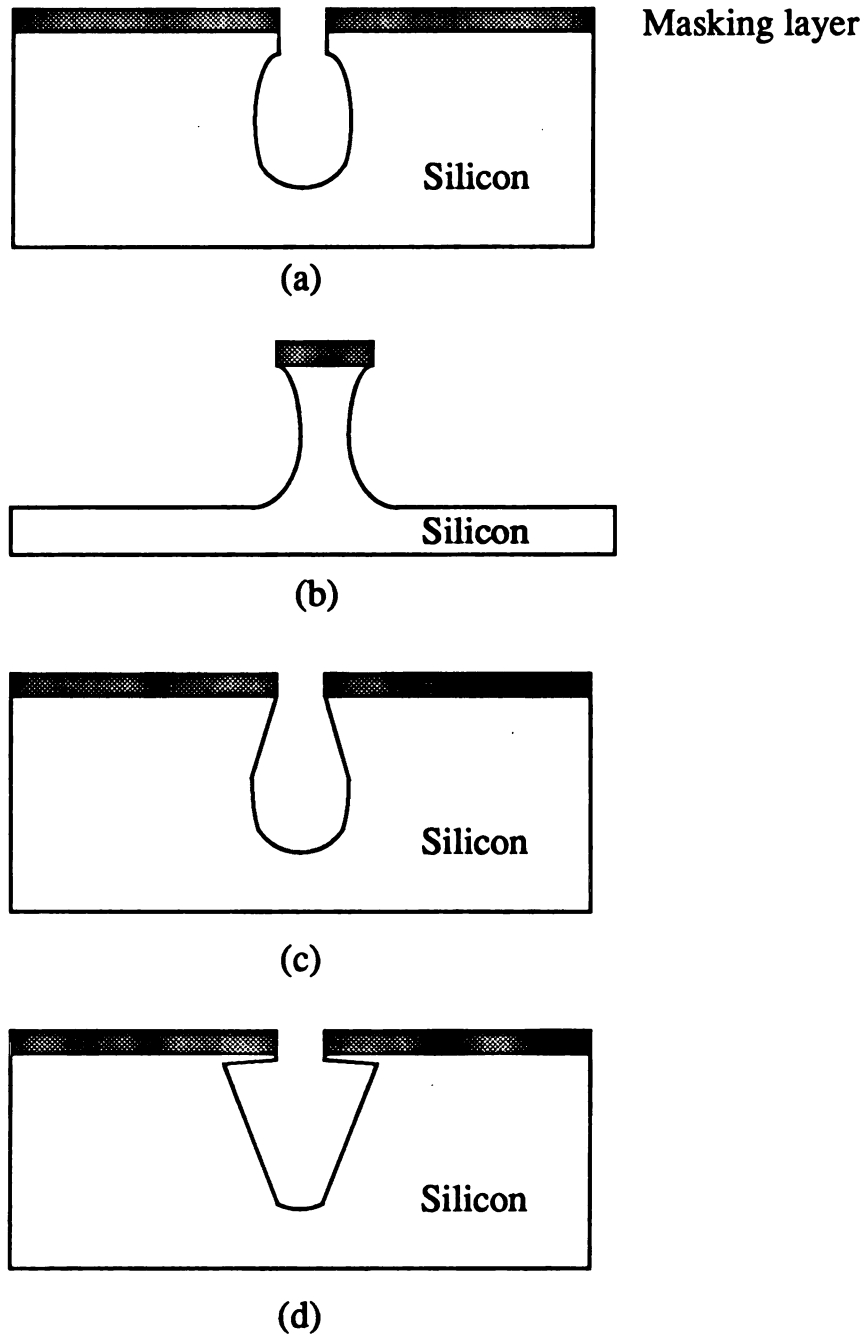


Figure 5.2 Non-Anisotropic Etching Profiles
a) Keyholing, b) Bowing, c) Angled wall,
and d) Arrow-head Type Features.

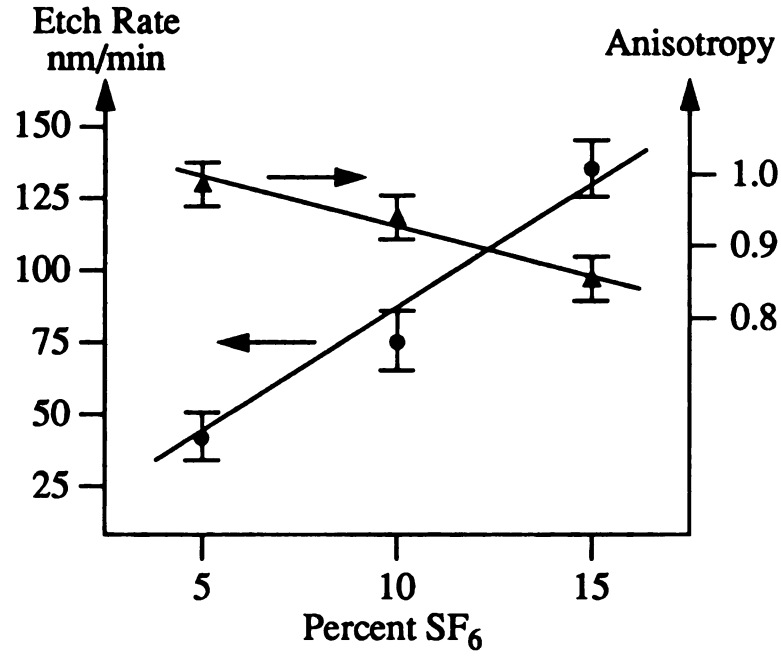
alter the path of ions as they pass through the trench opening, and 3) the increasing temperature of the substrate allows the fluorine radicals to spontaneously etch the silicon without the need for ion bombardment. Non-anisotropic profiles, however, were only observed between very *small* (< 2μm) features. Small amounts of "bowing" (Figure 5.2b) (a 1-sided keyhole) was observed on *small*, stand-alone features and the edges of multiple, closely spaced small features. *Large* lines, such as those shown in Figure 5.1b do not appear to exhibit similar profiles. Figure 5.1d is a photograph of sub-micron trenches etched in silicon. Etch rates are seen to be slightly lower than Figures 5.1a - 5.1c and a small amount of keyholing is apparent.

The phenomena where small trenches are etched at a different rate than the bulk silicon is often called "microloading." In Figure 5.1a it appears as though some evidence of this exists. Between the lines, the etch depth measures about 5-10 percent less than outside of the lines. No evidence of microloading could be found on larger (3 μm, 5 μm) lines.

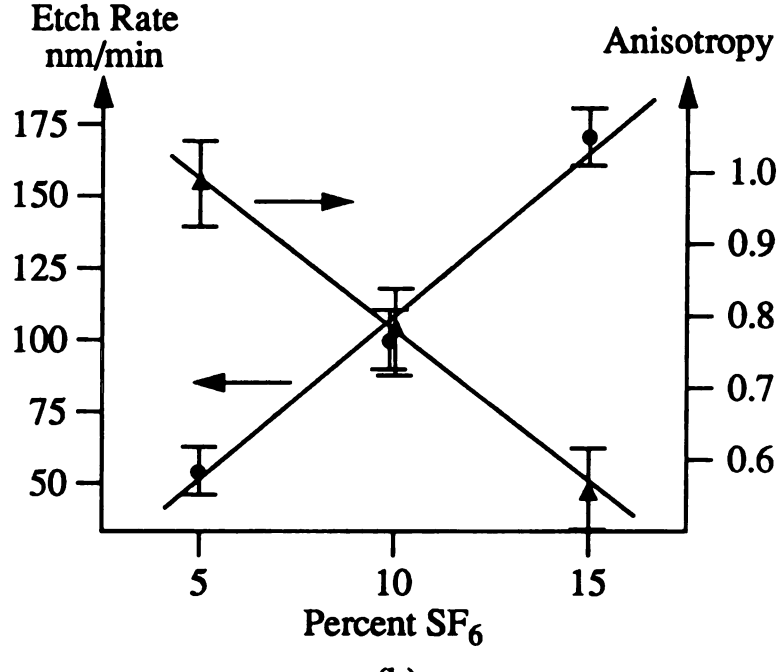
Etch rate and anisotropy were measured with the platter at d=15 cm below the discharge and are shown in Figure 5.3a. Anisotropy is defined as

$$A = 1 - \frac{h}{v}$$

where h is the horizontal etch depth and v is the vertical etch depth. *Undercutting*, as diagrammed in Figure 2.1a, was only seen in oxide mask etching. More commonly, keyholing (Figure 5.2a), bowing (Figure 5.2b), angled wall (Figure 5.2c), and arrowhead (Figure 5.2d) type features were



(a)



(b)

Figure 5.3 325 Silicon Etch Rate (•) and Anisotropy (▲)
with a) an Aluminum Mask, and b) a Resist Mask
(0.7 mTorr, 600 Watts Microwave Power, -50 volt, *Ls*=21.5cm, *Lp*=1.4cm)

seen. The horizontal etch depth in all anisotropy studies presented herein is defined as the point where horizontal etching was maximum.

5.3 MPDR 325 Etching with Photoresist Masks

Photoresist masks were also used to define etching patterns although as previously discussed it is less robust than aluminum. The selectivity of silicon over deep UV cured AZ5209 is approximately 15:1 for 5% SF_6, 95% Ar and 3:1 for 15% SF_6, 85% Ar mixtures. These numbers are for pressures of 0.7 mTorr, d=15 cm below the discharge with a -50 volt d.c. bias and 600 Watts of microwave power. Any remaining resist is extremely hard after plasma etching and must be stripped via an oxide plasma "ashing" procedure.

An interesting feature of resist masks is that the resist appears to somehow aid in the etching process. Etch rates are significantly higher on wafers with resist masks than on those with aluminum masks. The etch rates also exhibit non-linearity with the higher percentages of SF_6 yielding a much higher etch rate. If the resist somehow increases the etch rate, as it is attacked by the plasma, one would expect higher etch rates.

Anisotropy is difficult to guage as the edges of the resist lines decay before the center. The same method was used to measure anisotropy, but since the resist degrades there is less certainty in the numerical values. A graph similar to 5.3a is shown in Figure 5.3b for resist masks.

5.4 Etching with Oxide Masks

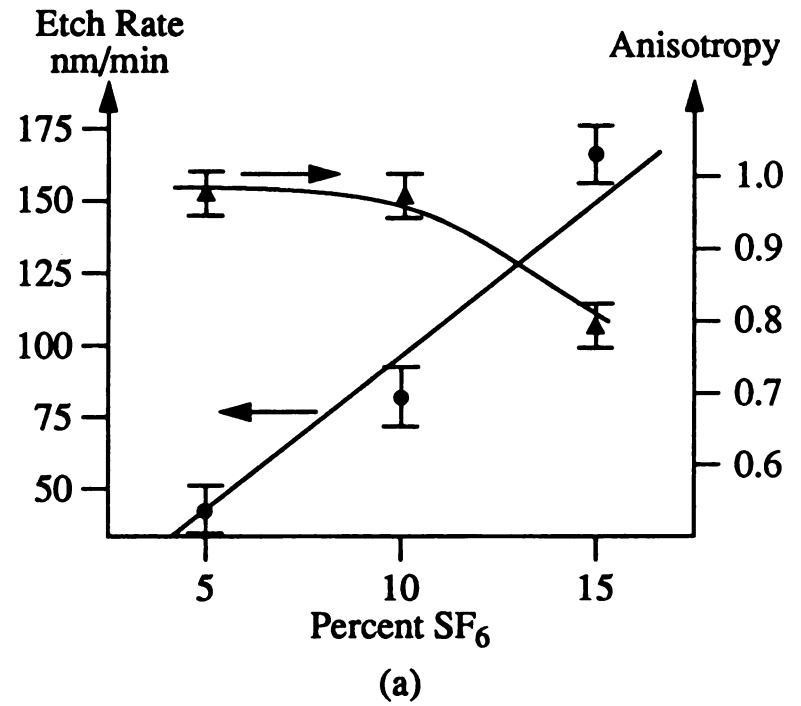
As described in section 3.8, Delco Electronics supplied twelve oxide

patterned wafers to assist in uniformity studies. Initially, the oxide layer was removed from the backside using an HF/DI mixture so that a d.c. bias could be applied to the wafer. One wafer was cut up into small pieces for preliminary tests using the Hopwood designed cavity. Whole remaining wafers were etched in the 325.

5.4.1 Seven Inch Cavity Oxide Mask Results

Six experiments were performed using the seven inch cavity with varying pressures, SF_6 concentrations, and d.c. biases. Low SF_6 ratios (5%) appeared not to etch the underlying silicon at all, while high ratios showed significant undercutting similar to Figure 5.2d. In six trials, only one combination (10% SF_6, -20 v) showed anisotropic etching. Theoretical studies by Ingram [49] have suggested that with an insulating mask, such as SiO_2, a higher d.c. bias might lead to larger undercutting. Figure 5.4a presents the results from the small cavity etching as a function of percent SF_6 at d=32 mm (see Hopwood, Reference 1) below the discharge. This position, however, may not be optimal for oxide mask experiments. Pressure was kept at a constant 0.8 mTorr with 260 Watts microwave power and -20 volt d.c. bias. The SEM photographs in Figure 5.5 suggest that as the bias voltage is increased, the increased negative charging of the oxide layer produces very strong fields at trench openings thereby imparting lateral energy to positive ions, resulting in horizontal etching.

Ingram, [49] through numerical solutions to LaPlace's equation, has shown that at 0 volts applied d.c. bias, the electrostatic potential distribution



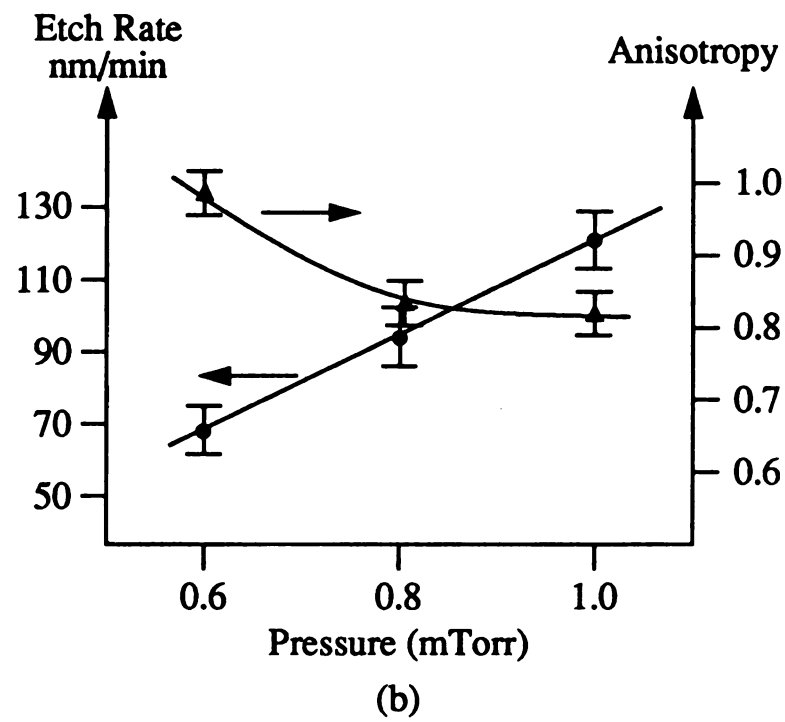
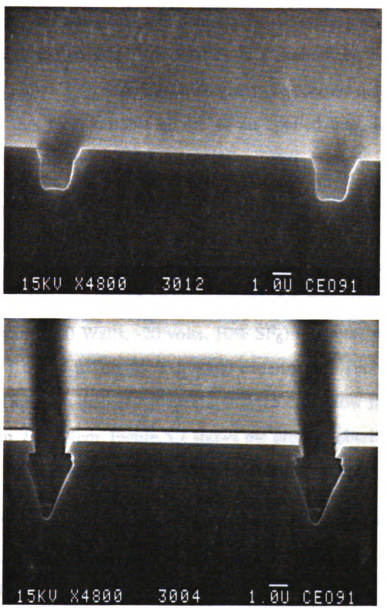


Figure 5.4 Etch Rate (•) and Anisotropy (▲) for oxide masks as a function of a) Percent SF_6 in the Seven Inch Cavity, and b) Pressure in the MPDR 325 (at 10% SF_6).



(a)

(b)

Figure 5.5 Seven Inch Cavity Etching Profiles a) -20 volts, b) -30 volts for Oxide Masks. The outward slanting profile is the patterned oxide before etching.

attracts positive ions to sidewall surfaces. As a negative wafer bias is increased, ion trajectories are directed more toward the sidewall with increasing angles. For very large negative biases, ions that would normally strike the mask are directed away from this upper layer and strike the silicon at varying angles. Assuming a sheath potential of -10 volts, a set of plots for ion trajectories is shown in Figure 5.6 (Vs is a normalized potential, i.e. $Vs=V_{applied}/V_{sheath}$). V_{sheath} is defined by Ingram as a positive quantity. These results suggest that by a suitable choice of an applied bias, ions may be directed away from the trench sidewalls.

5.4.2 MPDR 325 Oxide Mask Results

Whole 125 mm wafer etching results as a function of pressure using the 325 are shown in Figure 5.4b. Microwave power, d.c. bias, and percent SF_6 were held constant (600 Watts, -20 volts, 10% SF_6) while the pressure was regulated from 0.6 to 1 mTorr for individual experiments. The wafers were etched on the 18.54 cm diameter platform at d=15 cm below the discharge with Ls=21.5cm, Lp=1.4cm. Figure 5.7 shows the profiles obtained from the lowest (0.6 mTorr) and highest (1.0 mTorr) pressure experiments.

Near perfect anisotropy is achieved at 0.6 mTorr with an etch rate of 70 nm/min and a selectivity greater that 25:1 (Figure 5.7a). As pressure is increased to 1.0 mTorr, angled sidewalls begin to appear (Figure 5.7b).

Ingram's theoretical results indicate that with insulating masks, profiles can be selectively controlled with an applied d.c. bias. The results obtained here are in qualitative agreement with theoretical modelling.

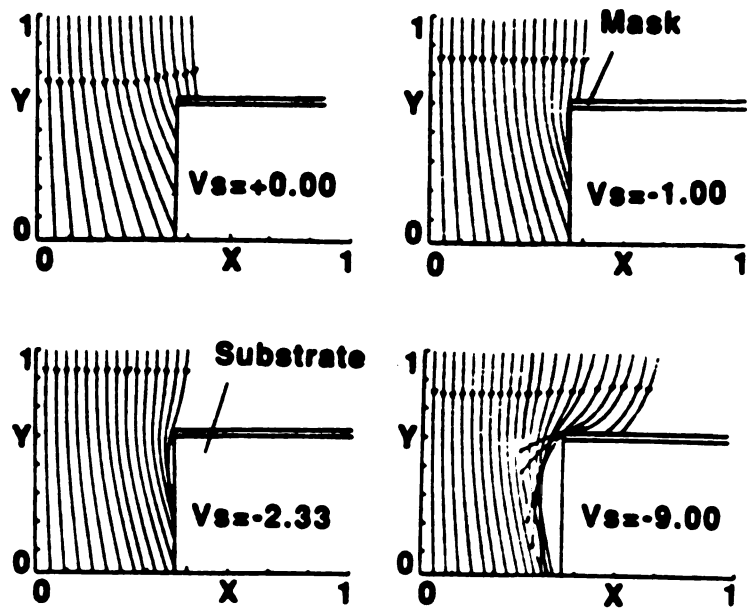
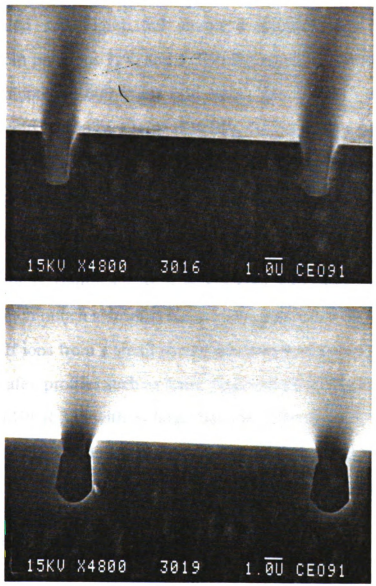


Figure 5.6 Trajectories of Positive Ions Near an Insulating Mask
(after Ingram, Reference 5.1)



(a)

(b)

Figure 5.7 MPDR 325 Etching Profiles, a) 0.6 mTorr, b) 1.0 mTorr.

5.5 Orientation and Position Effects.

Multiple 75 mm wafer experiments were conducted to determine if etching profiles vary with wafer position. Etched wafers on the 18.54 cm diameter platter were cleaved along the lines in Figure 5.8. All areas (1-12) were investigated and Figure 5.9 shows a representative set of SEM photographs from positions 1, 4, and 5. Etching conditions using the MPDR 325 were 30 minutes at 600 Watts microwave power, d=15 cm below the discharge, -30 volts, 0.8 mTorr, with 10% SF_6. No noticeable profile changes are observed in any of the positions. Slightly smaller etch depths were noticed at the outer edges (1-2 cm) but this is to be expected as plasma density is also lower at the edges.

This result is significant as it is assumed that ions with horizontal velocities will etch trench sidewalls but no diverging ion trench wall etching was observed. If ions from a small source are forced to diverge to uniformly cover a large wafer, profiles such as those diagrammed in Figure 5.10 may be expected. The MPDR 325 with its large diameter (25cm) discharge region, in conjunction with the additional confinement magnets appear to produce monoenergetic (no horizontal velocity) ions over the entire wafer.

5.6 Uniformity

Uniformity of etching using the MPDR 325 was gauged by measuring the etch depth over single 125 mm wafers and multiple 75 mm wafers. Single 125 mm wafers etched 15 cm below the discharge with 600 Watts microwave power, -20 volt d.c. bias at 0.6 mTorr showed 3σ (3 x std. dev.) values of

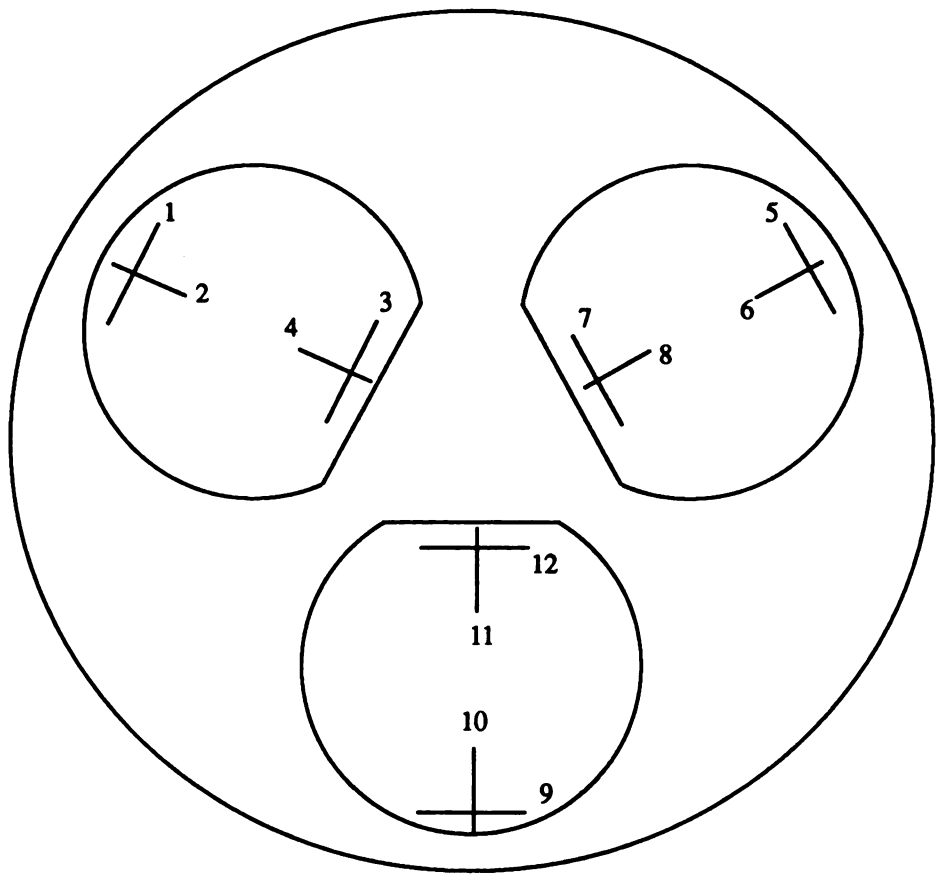
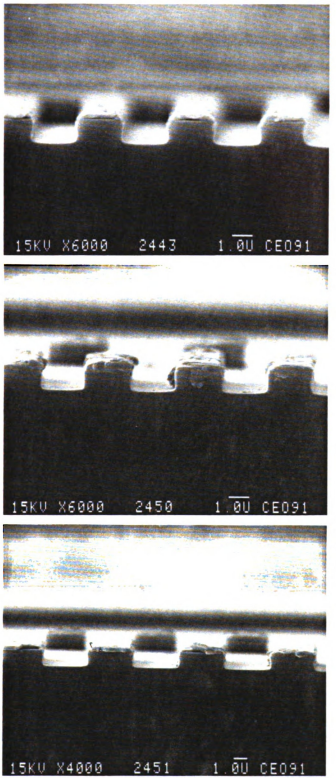


Figure 5.8 Cleave Lines for Orientation and Positional Studies



(a)

(b)

(c)

Figure 5.9 SEM Profile Photographs of Positions
a) 1, b) 4, and c) 5 (see Figure 5.8)

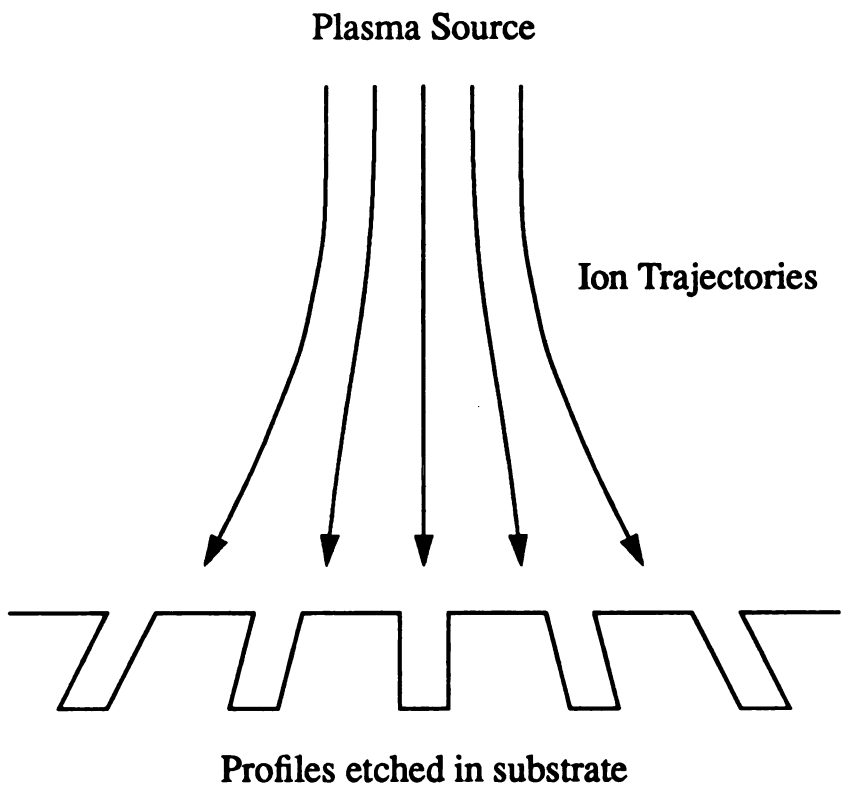


Figure 5.10 Diverging ions and the resultant etch profiles

2.31% of the etch depth. Higher pressures (0.8 mTorr) exhibited a slightly larger 3σ variations of 3.6% of the etch depth. It should be noted, however, that these numbers represent measurements taken on approximately 70% of the area as measurements on the right third of the wafer were unavailable due to masking problems. It is believed that since only nine measurements were available on the entire wafer, the actual 3σ value *might* be more than 3.6%.

Multiple 75 mm wafer experiments may better represent the actual etch uniformity but suffer slightly from the fact that there are areas inside the observation diameter where no numbers are available (see Figure 4.4). With 550 Watts microwave power, 8% SF_6, and a -30 volt d.c. bias, 3σ uniformity within a 15cm diameter using a resist mask measures 8.1% of the etch depth. The majority of variation is seen in the outer one or two centimeters. Within a 12.5 cm diameter, the 3σ uniformity is 5.1% of the etch depth. In order to minimize any measurement induced error, approximately 40 measurements were taken on each wafer to accurately reflect the etch depth.

Another uniformity figure of merit often used in industry [50] is the so called "max-min" uniformity.

$$U = \frac{Max - Min}{2 \times Avg}$$

This number inherently produces rather large values if anomalies are found in the etch depth or an error in measurement occurs. Inside a 15.2 cm diameter for the previously mentioned resist mask experiments, U=7.13%. After removing a single number from the data which is believed to be in error,

U=5.6%. Inside a 12.7 cm diameter, U=4.8%. For the single 125 mm oxide patterned wafers, U varied from 1.3% to 1.8%.

5.7 Damage Assessment

Depletion layer capacitors were formed by evaporating aluminum on the surface of bare silicon. Initially, wafers were cleaned with boiling TCE followed by a Degrease and Demetal etch. A 2000Å thick oxide layer was grown and stripped off the backside to allow for a Boron diffusion (p^+ layer) necessary for an ohmic contact. The residual Boron-glass was stripped away and a 4500Å thick layer of aluminum was evaporated then annealed on the back. This provided an ohmic contact for the anode of the capacitor. Subsequently, the oxide layer was stripped from the front with a buffered oxide etch and half the samples were selected for plasma etching. Immediately prior to plasma etching, samples were dipped in a 9:1 DI:HF solution to remove any native oxide layers. They were rinsed for one minute in DI water then dried with a vapor phase IPA rinse (see section 3.3).

After etching, both control and etched samples were rinsed in DI water, dipped in a 9:1 DI:HF solution and cleaned with boiling TCE followed by an acetone, methanol, and two-minute DI rinse. Drying was similarly accomplished with a vapor phase IPA rinse. Control and etched samples were immediately placed in the electron beam aluminum evaporator and pumped down to 10^{-7} Torr. A shadow mask with 1.8 and 2.6 mm diameter holes was used to evaporate 2400Å thick aluminum dots on the substrates.

Preliminary studies by Gopinath [51] on samples etched with the

MPDR 325 at 0.8 mTorr, -20 volt d.c. bias, 600 Watts microwave power, 15 cm downstream, with 10% SF_6 are shown in Figure 5.11. From C-V curves, one can obtain information on dopant concentration near the surface and shallow impurities. Figure 5.11a shows the C-V characteristics of the control sample. A straight line indicates a uniform dopant concentration and very little surface contamination. Figure 5.11b is a similar plot of etched sample C-V characteristics. N_a, the acceptor concentration in the silicon can be evaluated by [52]

$$N_a = \frac{2}{q\varepsilon_s}\left[-\frac{1}{\frac{d}{dV}(1/C^2)}\right]$$

and is plotted in Figure 5.11c. A damage (or contaminated) layer appears to extend approximately 1.5 μm into the silicon surface.

This is a relatively deep carrier compensation layer given the fact that the temperature of the wafer was generally kept under 350°C. Further studies on these samples (such as Schottky barrier diode I-V characteristics) may reveal interesting new information and also may explain the apparent deep depletion layer.

5.8 Summary

This chapter has detailed etching experiments on small features using the Hopwood designed cavity and the MPDR 325. Specifically, etch profiles and etch uniformity were evaluated while varying system pressure and SF_6 partial pressures.

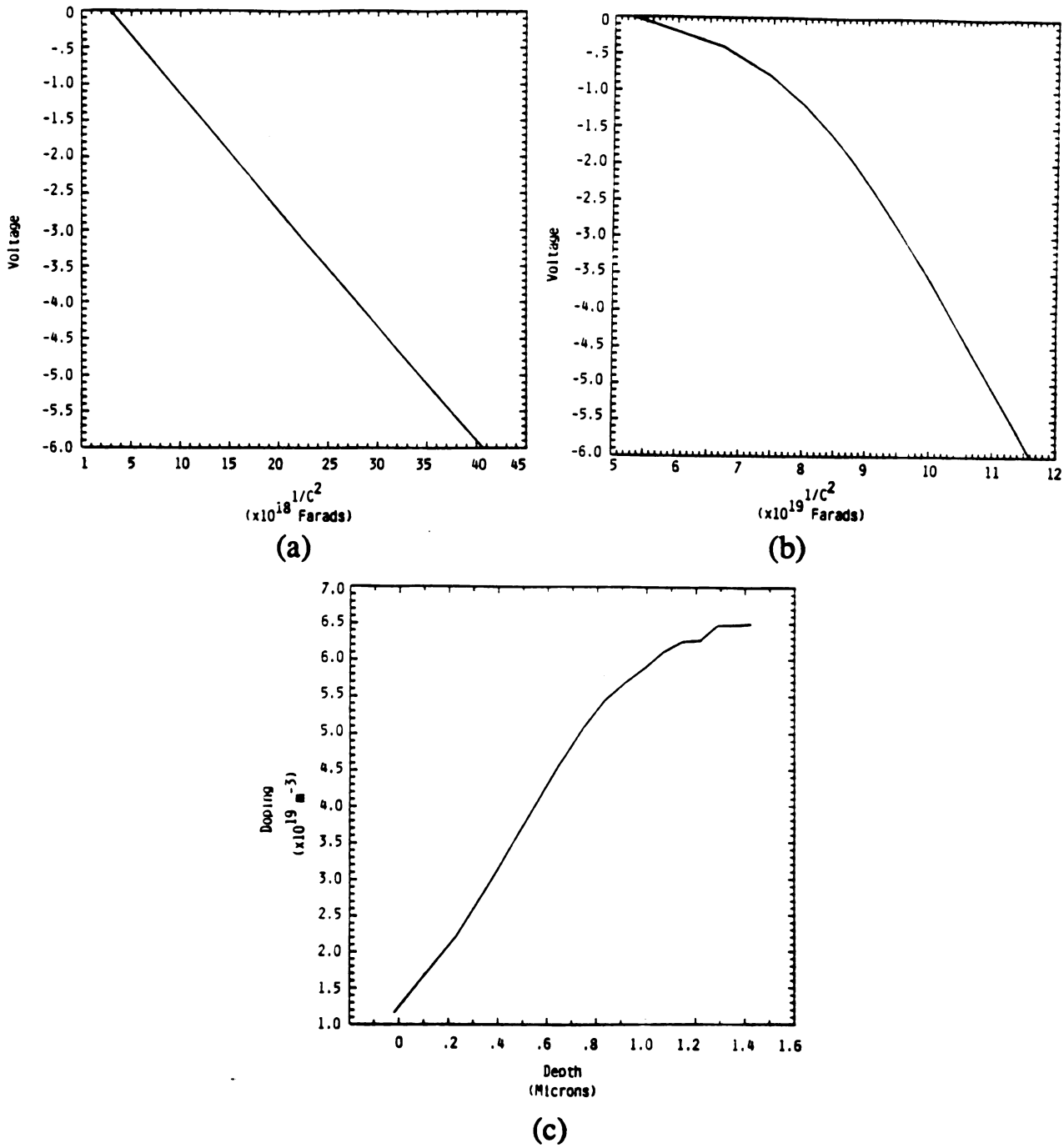


Figure 5.11 C-V plots for a) unetched, and b) plasma etched samples, and c) doping concentrations in etched samples.

Aluminum masks were employed to anisotropically etch sub-micron features with an early design Wavemat MPDR 325 reactor excited at 2.45 GHz with relatively low input power (600 Watts). Etch rates of 40 nm/min were observed with a 5% SF_6, 95% Argon mixture. Higher SF_6 concentrations (15%) yielded higher etch rates (140 nm/min) but at a loss of anisotropy (A=0.85). Similar experiments were performed using photoresist masks and show etch rates varying from 55 nm/min (5% SF_6) to 175 nm/min (15% SF_6).

Oxide patterned wafers were used to study etching with insulating masks and a variety of different trench profiles were obtained. Low pressure (0.6 mTorr, 5% SF_6) experiments in the MPDR 325 at 2.45 GHz show silicon etch rates of 65 nm/min with near perfect anisotropy. By increasing pressure and SF_6 concentrations, arrow-head profiles are seen. Increasing d.c. biases on the wafer are also seen to alter the trench profiles. Etch results are quantitatively compared to theoretical studies modeling ion trajectories.

Large wafer studies show high degrees uniformity over 125 and 150 mm diameters. Multiple (3) 75 mm wafers have 3σ values of 8.1% over 150 mm and 5.1% over 125 mm. Single 125 mm wafers show 3σ values as low as 2.3%. No etch profile or depth variations were found at twelve selected ρ, ϕ positions.

Preliminary damage studies using Schottky barrier diode depletion layer capacitors indicate an apparent dopant compensation layer extending approximately 1.5 μm into the silicon. These results are for wafers etched at 0.8 mTorr, -20 volts, 600 Watts microwave power in the MPDR 325 at d=15cm downstream.

Chapter 6
Summary and Conclusions

6.1 Summary

A new ECR plasma source has been evaluated for silicon etching in a fluorine plasma. Also, a sub-micron lithography procedure was developed to pattern silicon wafers with aluminum using lift-off techniques. In this exploratory study, processing conditions, including partial pressures of SF_6 in an argon gas and total system pressures, were varied and corresponding etching performance information including profiles and uniformity were obtained and evaluated. With appropriate operating conditions, anisotropic etching of submicron silicon features was obtained for oxide masks, resist masks, and aluminum masks. Uniform etching was observed over single 125 mm wafers and multiple (3) 75 mm wafers both in regard to etch rate and etch profile.

Two reactors were investigated. Initial experiments were performed on a 7 inch diameter cavity with a 9 cm diameter discharge which was used in an earlier study by Hopwood [1]. However, the majority of the experiments were performed on a 14 inch diameter cavity with a 25 cm diameter discharge. In both cases the microwave excitation was at 2.45 GHz. For the larger reactor, additional confinement magnets were used to improve plasma uniformity. The percentage of SF_6 ranged from 5 to 15% and pressures were varied from 0.5 to 2 mTorr. Relatively low input powers were used with a maximum of 250 W

for the small reactor and 600 W for the large reactor. For the large reactor, etching experiments were performed with the wafers approximately 15 cm below the ECR production region on uncooled substrates which were provided with a dc bias.

Etch rates and profiles were evaluated at different ρ, ϕ values on the wafer holder and no substantial positional/orientation effects could be found on etch *rates* or *profiles*. For single 125 mm wafers with oxide masks the 3σ variation of silicon etch rate uniformity was 2.3% and for multiple 75 mm wafers with aluminum masks the 3σ variation was 8.1% for a 150 mm radius. Because of the low power inputs and low SF_6 concentrations, etch rates were relatively low, ranging from 40 to 140 nm/min as the SF_6 ratio ranged from 5 to 15%. In contrast to reports for divergent field ECR reactors, no ρ or ϕ dependence was observed in the etch profiles. Vertical, anisotropic etching was obtained both at the center of the wafers and at the peripheries.

Anisotropic etching is achieved with an appropriate set of operating conditions which depend in part on the masking material. For example, anisotropic etching of silicon with an oxide mask was observed with a -20 V bias and 10% SF_6 at 0.6 mTorr. For higher biases with oxide masks, and for higher pressures, an arrow head shaped etching profile was observed for the power and pressure conditions investigated in this work. When etching with aluminum masks, anisotropic values of unity were obtained with 5% SF_6 at 0.7 mTorr when the substrate bias was -50 V. Higher values of SF_6 and higher total pressures produced measurable deviations from perfect anisotropy with keyhole and bowing observed. In this exploratory research, other substrate

biases were not investigated for the case of aluminum masks. Microloading effects appear to be small for both oxide and aluminum masks. Sub-micron (0.6μm) trenches and holes were anisotropically etched in silicon and show approximately a 5% lower etch rate than large (>5μm) features. After forming Schottky barrier diodes on etched silicon surfaces, preliminary C-V measurements indicate a dopant compensation layer extending into the silicon. This may however be caused by handling or other contamination during processing. The etching system was not located in a cleanroom environment and utilizes oil based diffusion pumps and roughing pumps. High energy UV light may also contribute to the damage at the surface.

6.2 Suggestions for Further Research

There are a number of possibilities for improving the etching performance. These include operating at higher microwave input power to achieve higher rates, as well as improvements in the reactor and system design. Further research remains on the optimum number and location of ECR magnets and the specific mode of excitation as well as the location of the confinement magnets relative to the ECR magnets. Also it would appear desirable to reduce the cavity diameter from 14 inches to 12 inches and to reduce the base plate thickness.

To better understand the performance of the ECR reactor, full 125 and 150 mm wafers should be more thoroughly investigated. Complete 150 mm wafers experiments may provide better information on any orientation or positional effects as well as being a more robust technique for evaluating

uniformity over large diameters. Also of interest is a temperature controlled wafer holding platform. In this work, it is estimated that the surface temperature of the wafer can exceed 300°C. Other investigators [24] have demonstrated steadily improving anisotropy and etch rates by cooling the wafer to as low as -130°C.

For etching insulating substrates such as SiO_2 and Si_3N_4, an rf-bias, capacitively coupled to the wafers, should be investigated. Contamination and damage should be more thoroughly investigated via Schottky barrier diodes, metal oxide semiconductor capacitors, and other analytical techniques such as Auger electron spectroscopy, XPS, and SIMS. This may provide a better understanding of the results presented in section 5.7. Investigations into UV light produced by the reactor may also help to define the source of the recorded damage.

A deeper understanding of the relation between trench profiles and substrate bias with an insulating mask should also be obtained. Theoretical modeling of charge buildup and the resulting potential distributions along with further experimental studies using multiple biases may help to define optimum processing conditions.

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