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AN INVESTIGATION OF METHODS OF EVALUATING PLASMA ETCH DAMAGE ON SILICON

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ABSTRACT

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Plasma etching is widely used in the industry to achieve low damage and smaller line widths. The major forms of damage due to etching can be in the form of shallow and deep surface disruptions leading to anomalous device behavior of the devices subsequently formed. Energetic ions can cause substrate damage in the form of interface states and dopant compensation. UV and X-ray radiation can lead to the formation of electron-hole pairs which can lead to non ideal C-V characteristic and shift in threshold voltage in MOS devices. Some of these effects are reversible by annealing, however, these effects are still harmful when high temperature annealing cannot be done on the wafer.

The particular etch procedure used in this investigation was SF_6/Ar plasma etching of silicon in which plasma was formed by a microwave electron cyclotron resonance (ECR) source. However the emphasis was on a comparison of evaluation methods rather than on the etching process. The etching parameters were not varied.

This thesis applies five different methods to evaluate damage to silicon substrate that occurs due to plasma etching. Of these methods, three (current vs. voltage, capacitance vs. voltage and Deep Level Transient Spectroscopy) were applied to compare the characteristics of Schottky Barrier diodes formed on the surface of etched and unetched silicon. In addition preliminary results of two chemical spectroscopy methods (Auger and XPS) are briefly reported.

The most significant insight into the effects of plasma etching for the particular etching condition used here was provided by the C-V measurements which pointed to a sig-

nificant dopant compensation beneath the surface of the wafer.

The method perhaps most mentioned in the literature, I-V evaluation of Schottky barrier diodes, did not show significant changes in etched vs. unetched samples. This may indicate small surface effects for the etching process evaluated.

The etched samples showed a measurable change in the transient capacitance measurements used for the DLTS method, indicating up to about 10^{13} states /cm^3 after etching, but the results were not interpretable as a single energy trap level.

XPS and Auger measurements were conducted in order to determine the concentration of impurities.It was noticed that fluorine is present in large quantities in the wafer even after surface sputter. Fluorine has been previously known to cause carrier reduction under ion implantation in semiconductors and may be the reason for the C-V results on Schottky diodes. However, hydrogen, which is not detectable by either of the above methods, is also known to cause a similar effect in semiconductors. The obvious source of fluorine is the etching gas SF_6. A source of hydrogen is less apparent but may be acetone which is a constituent in the conducting graphite paint applied on the back of the wafer during etching.

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Chapter 1

Introduction

1.1 Problem statement and objectives

The present trend in integrated circuit fabrication is toward higher circuit densities leading to requirements of smaller line widths. In this regard, most conventional wet etching methods stand at a disadvantage due to their inherent lack of directionality. This has led to the increasing use of dry etching methods in which plasmas provide the reactive chemical species required for etching. Plasma etching techniques allow precise process control and with appropriate operating conditions are highly directional thus leading to higher circuit densities. However dry etching techniques are not altogether without drawbacks. Amongst the possible deleterious effects of plasma etching are carrier reduction, introduction of deep states and electrostatic damage of thin insulating films [1].

This thesis compares several different experimental methods for determining damage associated with plasma etching. The particular etch procedure used in this investigation was SF_6/ Ar plasma etching of silicon in which the plasma was formed by a microwave electron cyclotron resonance (ECR) plasma source [2]. There exist a number of methods which allow one to check for the occurrence of plasma etch related damage, contamination, or defects. In this thesis five different methods were chosen and applied to the same etching processes. The emphasis therefore is on a comparison of evaluation methods rather than on the etching process. The etching parameters were not appreciably varied.

Three of the evaluation methods involved the formation of Schottky barrier diodes. These diodes were chosen in particular for this experiment because of their simplicity and

ease of fabrication. Most of the electrical characteristics of the SBDs can be directly correlated to the structure of the underlying silicon wafer. The chief evaluation methods associated with the Schottky barrier diodes were the current vs. voltage (I-V), capacitance vs. voltage (C-V) and Deep Level Transient Spectroscopy (DLTS). The bulk of the thesis is concerned with these three evaluation methods. In addition, two preliminary experiments with chemical spectroscopy methods, X- ray Photoelectron Spectroscopy (XPS) and Auger Electron Spectroscopy (AES), were used to determine the chemical composition of the wafer after etching. Each of the first three methods associated with Schottky barrier diode is sensitive to a different form of defect. A type of defect which causes a major change in the characteristic of one of the measurements may hardly effect the other two.The chemical spectroscopy methods were used to explore explanations for the results of the first three methods in terms of the wafer's chemical composition, thus obtaining additional insight into the electrical behavior of the devices formed on it. The thesis compares the nature and amount of information provided by each method in terms of the analysis of etching damage. A PISCES simulation was also conducted to confirm some of the unexpected I-V results.

1.2 Thesis Organization

This thesis presents insight into some of the commonly applied methods used to study effects of etching on semiconductors.

Chapter 2 provides the background details of plasma etching and associated etching damage. The underlying concepts of DLTS, XPS and Auger methods and a short overview of the Schottky Barrier Diode are also presented.

Chapter 3 describes the different experimental methods conducted on the samples. Sections 3.2 and 3.3 describe the fabrication and etching details of the Schottky Barrier diodes. Section 3.4 describes in detail the experimental setup and procedure of the DLTS

measurements. Finally, Section 3.5 describes the electrical measurement conducted on diodes.

The results of the afore mentioned experiments are detailed in Chapter 4. The chapter offers speculation on the results of the measurements in terms of chemical composition, using information from the results of XPS and Auger methods.

Finally Chapter 5 summarizes the work of this thesis and points out areas where further work can be done.

Chapter 2

Background

2.1 Introduction

This chapter provides a brief overview of the various experimental methods conducted during this thesis. Sections 2.2 and 2.3 introduce the concepts of plasma etching and associated damage. Section 2.4 provides a detailed introduction to the concepts of DLTS. A brief overview of the Schottky barrier diode and its electrical characteristics is provided in Section 2.5. Concepts of the chemical spectroscopy methods like XPS and Auger are introduced in Section 2.6.

2.2 Plasma etching

Etching can be broadly classified into two categories, wet and dry. Wet etching (purely chemical), with some exceptions, has no preferred direction, leading to isotropic properties and undercutting of the mask. Higher circuit densities require low defect densities and precise process control, both of which are lacking in wet etching. Ideal ion enhanced plasma etching (dry) produces an anisotropic profile[1]. Therefore as device sizes continued to shrink, dry anisotropic etching methods became preferable to wet isotropic ones. This, however, led to new variables and new types of defects associated with ion bombardment and other plasma effects. This chapter will briefly introduce plasma etching and its related effects [1].

The simplest form of plasma reactor consists of two parallel plates in a chamber filled with a gas at pressures of approximately 0.01 to 1 Torr. When a voltage of sufficient magnitude is applied to the plates, ionization occurs forming a plasma which emits a characteristic glow. The applied voltage may be AC or DC. Most typically in parallel plate reactors, an RF frequency is applied. Reactive species including ions and radicals are formed

due to this electrical discharge. Semiconductor wafers exposed to this environment combine with the reactive species and form volatile products thus leading to etching. The plasma chemistry can be chosen such that the reactive species do not react with the masks and the substrate holder. Plasma etching is similar to wet etching in that both of them react selectively with the desired material thus removing it. A major advantage of plasma etching, as will be seen, lies in the capability to control the direction of etching.

In plasmas used for etching the extent of ionization of the gas is small. Usually less than 1% of the species are ionized. The plasma contains equal numbers of positive and negative species. The positive species are generally positive ions and the negative species include electrons and in some cases negative ions. The flow of current however is dominated by electrons because among all the charged particles present in the plasma they are the lightest and hence the most mobile. Since the transfer of energy between two particles is most efficient when the masses of the interacting species are comparable, the electrons in motion lose very little energy to the surrounding matter. Thus it can be considered that the effective temperature of the electrons is much higher than that of the surrounding gas. The elevated electron temperature allows formation of high temperature type reactions in a low temperature neutral gas leading to formation of free radicals. In the absence of plasma the formation of radicals would require temperatures of thousands of degrees kelvin.

Although the amount of positive and negative charge is the same, charge imbalance will occur due to charge diffusion into the walls and recombination at boundary surfaces. This tends to deplete the charge in the adjacent gas forming a thin boundary layer or *sheath*. The electrons being the lightest diffuse the fastest leading to a charge separation and the development of a plasma potential relative to the walls. The plasma can now be considered as a series combination of an extremely conductive central glow and a less conducting sheath. Therefore most of the potential drop appears across the sheath. This voltage accelerates the positive ions towards the surface leading to near normal incidence.The magnitude of this voltage plays a critical role in the degree of anisotropy and to substrate damage.

Although current etching procedures used in integrated circuit fabrication are predominantly RF reactors, there is appreciable interest in microwave ECR plasma reactors

such as the one used in this research. The theory and practice of ECR reactors has been reviewed by Asmussen and only brief features will be described here [3]. Because of the resonant coupling of electromagnetic energy to the plasma electrons, and because of magnetic confinement, these discharges are highly efficient. Consequently, high plasma densities (on the order of 10^{12} /cm^3) are obtainable at low pressures (less than or equal to 1 mTorr) with relatively low electric fields and therefore low sheath potentials (on the order of 10 V). This combination of properties results in the ability to achieve anisotropic etching with low damage and high selectivity. Examples of current interest in ECR etching include the etching of gate polysilicon in which high selectivity and low damage is crucial [4] and the etching of III-V and II-VI compounds whose surfaces are highly sensitive to damage by energetic ions [5,6].

Plasma etching can be divided into four distinct methods as described below.

1) *Sputtering* involves the process where the ion strike the surface of the semiconductor with enough energy to cause the ejection of surface atoms, much like a high pressure water drill. This process lacks selectivity and is generally associated with significant substrate damage.

2) *Chemical etching* occurs where the gas species reacts spontaneously with the surface. The gas is chosen such that the components of the gas selectively react with the surface forming a volatile product. Here plasma assists the etching by forming the reactive etchant from the gas. For example NF_3 in plasma leads to the formation of F atoms which reacts selectively with silicon. Selectivity is inherent in this process since fluorine reacts strongly with silicon forming SiF_4. However this process is similar to wet etching in directionality.

3) *Ion enhanced energetic etching* occurs when the high energy ions act as catalysts during the etching. A gas is chosen such that neutral radicals on their own cannot react with the surface to form a volatile product. However when the surface is exposed to high energy ions, the reactivity of the surface to the gas increases, leading to ion assisted etching. This process is directional since the ions which hit the surface perpendicularly enhance the reactivity of only those surface atoms. At room temperature chlorine does not react with silicon but when the surface is exposed to high energy ions, silicon chloride is formed rapidly.

4) *Inhibitor ion enhanced etching* consists of inhibitors and etchants. The etchant used in this case reacts spontaneously with the substrate. The role of the inhibitor lies in enhancing selectivity by forming a thin film on the side walls thus preventing undercutting.

2.3 Damage due to Plasma etching

Wafers placed in plasma environment are exposed to particle bombardment. If the particle energies are sufficiently high, this may cause both shallow and deep surface disruption, altering the electrical characteristics and thereby the behavior of the devices formed on this surface. Damage can be in the form of atomic displacements due to ion impact or formation of electron-hole pairs due to UV or X-ray radiation. The effects of this damage can manifest itself in a number of ways including, for example, a change in the C-V characteristic of the device or as a shift in threshold voltage in MOS transistors. Damage due to plasma etching can be broadly classified into reversible and irreversible effects. Reversible effects are those which can be removed by some form of post processing, normally in the form of thermal annealing. Annealing as a form of damage control will be effective only as long as other wafer properties are unaffected. This technique is less useful when applied to technologies where shallow junctions are critical because the temperatures involved in annealing cause impurity motion and permanently change the characteristics of the wafer. Difficulties also arise when extremely good surface characteristics are desired as in the formation of thin oxide gates. Irreversible effects are seen when contamination occurs due to the deposition of sputtered reactor material onto the surface of the semiconductor. Electrostatic damage of thin insulating films is another irreversible effect of plasma etching. The gate insulator may not be able to withstand the voltage developed across it during etching.

Compensation of dopants is also reported as a type of plasma etch damage. Studies conducted on Schottky barrier diodes formed on etched surfaces by Constantine et al [4] indicate a reduction in carrier concentration in the near-surface region of n-type GaAs after etching. This effect was ascribed to the indiffusion of atomic hydrogen from the plasma

resulting in the deactivation of Si dopants in GaAs. Studies conducted by Heddelson et al [7] also showed dopant deactivation in both n-type and p-type silicon when hydrogen was present in the bombarding species. It was also noticed that this effect was more pronounced in p-type material. In the case of p-type material dopant deactivation was noticed even when hydrogen was not introduced intentionally.

2.4 Overview of DLTS

Deep Level Transient Spectroscopy (DLTS) is a high frequency capacitance thermal scanning method first introduced by D.V. Lang [8]. The technique displays the presence of traps in differential capacitance as negative or positive peaks as a function of temperature. The peak reflects the thermal emission properties of traps, activation energy, concentration profile etc. The theory behind this technique assumes exponential capacitance vs. time transients. An alternative method, luminescence, can be used with considerable success in the study of shallow centers but is not very successful in characterizing deep traps.

Some definitions are in order before the theory behind DLTS can be explained.

Deep traps: Traps found to occur nearer to the center of the band gap.

Electron traps: Traps present in the upper half of the band gap i.e. closer to the conduction band. In steady state these traps tend to be empty of electrons and thus capable of capturing them.

Hole traps: Traps present in the lower half of the band gap i.e. closer to the valence band. In steady state these traps tend to be full of electrons and thus are capable of capturing holes.

Pulsed bias capacitance transients: The capacitance vs. time transient that occurs after a short width bias pulse has been applied to a steady state capacitor.

Intrinsic lattice defects or impurity atoms can introduce trap states in the middle of the gap. The presence of deep traps makes the junction capacitance a complicated function

of bias voltage and measurement frequency. If the time constant of the trap is low enough to follow the bias variation and the small AC signal used to measure capacitance, then the background doping concentration N_b can be replaced by $(N_b + N_t)$ where N_t is the concentration of deep traps.However if the time constant of the trap is so large that it cannot follow the changes in either bias voltage or measuring signal, no effect on capacitance is observed.

If the depletion region of a Schottky barrier diode contains deep traps and the capacitance is changed rapidly, the traps, because of their finite response time, will not be able to respond to this change instantaneously. Information about trap energy and response time can be obtained from the capacitance transient resulting from the bias pulse. Consider a SBD fabricated on n-type silicon with donor type traps below the Fermi energy level and therefore unionized. If the diode is suddenly reverse biased, the capacitance will decrease abruptly because of the increase in the depletion layer width. Initially the depletion region will expand, incorporating an increased number of the donor traps. However as time passes since the donor traps are now above the Fermi level, they will be emptied out resulting in an increased density of positive charge and thus reducing depletion region widths. The resulting change in capacitance, measured as a function of time can be used to characterize traps present in the semiconductor. A short review of Schottky barrier diodes and their C-V and I-V characteristics is given in Section 2.5.

In this DLTS discussion we will consider the transients occurring after a reverse biased junction capacitance is momentarily forward biased. The sample, a Schottky barrier diode or a p^+n junction diode, is reverse biased long enough to bring the traps present in the depletion region to the steady state conditions. For example, electron traps, if any, are now emptied by the reverse bias. The sample is then given a biasing pulse, the value of which depends on the type of the trap being examined. The return of the capacitance to its reverse biased value at various instances of time forms the basis of Deep Level Transient Spectroscopy. The value of the reverse biased junction capacitance is labelled as C_∞. The DLTS theory consists of plotting the values of $(C(t_1)- C(t_2))/C_\infty$ versus temperature. The sign of the capacitance change depends upon the nature of the trap.

The theory of DLTS as presented by Lang is explained in terms of a heavily doped

p^+n junction. The theory assumes that in such a junction under reverse bias most of the depletion region will be in the lesser doped area, i.e. the n region, and the capacitance transients will be mainly due to the characteristics of the lightly doped region. However a Schottky barrier diode is also well suited for such an explanation because all of the depletion region is formed in the semiconductor. Let the thermal capture and emission rates for electrons be c_1 and e_1 respectively and the same for the holes be c_2 and e_2. In the quiescent reverse bias state all of the observable states are in the depletion region, therefore the capture rates are zero. The occupation level is determined by the thermal emission rates e_1 and e_2. The steady state occupation of a trap is given by

$$n_1 = [e_2/(e_1+e_2)]N \qquad (1)$$

where n_1 is number of electrons present in the trap and N is the concentration of the trap. Therefore electron traps have a value of n_1 close to zero and hole traps have n_1 nearly equal to N. Thus according to Eq. (1), an electron trap has $e_1 >> e_2$ while the contrary is true for a hole trap. The emission rates depend exponentially on the energy difference between the trap level and the corresponding band, conduction band for electrons and valence band for holes. A bias pulse causes a change in capacitance by changing the steady state occupation of the trap i.e. the trap concentration is no longer given by Eq. (1). As the trap concentration returns back to the value given by Eq. (1) the capacitance returns to its equilibrium value.

The actual change in capacitance would depend upon the way the bias pulse effects the trap i.e. if the concentration of the trap decreases as a result of this pulse, as it does for a hole trap, the value of the capacitance shows an increasing transient. The change in capacitance due to electron traps is quite the contrary since the occupancy of the trap is increased by the bias pulse. This leads to two types of bias pulses, one for electron traps and the other for hole traps. The bias pulse for electron traps forward biases the junction to the maximum possible extent so as to saturate the traps present in the depletion region and is hence called an injection pulse. The pulse used to observe hole traps momentarily reduces the bias across the diode and injects only minority carriers i.e. tends to empty the traps of all electrons. The two pulses and their effect on device capacitance is shown in Figure 2.1. The rate constant of the curve for electron traps will be nearly equal to e_1 and that of hole traps is e_2. Assum-

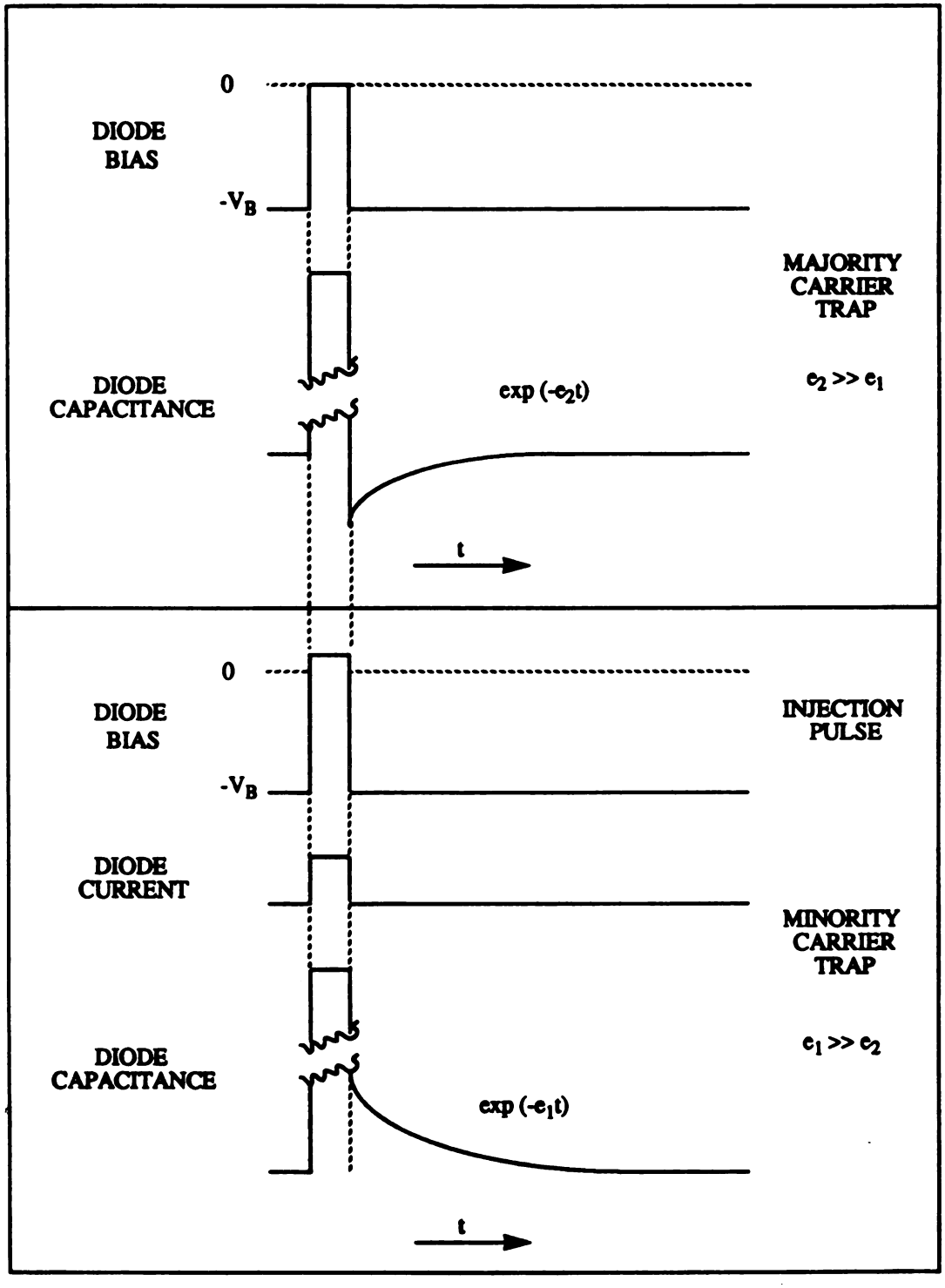


Figure 2.1. Capacitance transients for majority- and minority-carrier traps in p-type Schottky barrier diodes.

ing that the capture (recombination) rates of the traps are much larger than their emission rates, the steady state electron occupation of the same trap during the bias pulse can now be written as

$$n_1 = [c_2/(c_1+c_2)]N \qquad (2)$$

where c_1 and c_2 are the electron and hole capture rates respectively. The effect of an injection pulse is to introduce a large enough number of electrons, overwhelming the trap emptying process and thus making $c_1 >> c_2$. The effect of a majority (in this case, holes) carrier pulse is to do the opposite. The concentration of a trap can be obtained directly from the capacitance caused by the bias pulse. The relationship for a diode would be

$$N = 2(\Delta C/C)(N_B) \qquad (3)$$

where N is the trap concentration, ΔC is the capacitance change at time $t = 0$ due to the bias pulse and N_B is the background doping of the Schottky diode or the lesser doped side of a pn junction diode as the case may be.

The main feature of DLTS is the ability to set a rate window such that the measurement apparatus shows maximum sensitivity for transients with rates that fall in this window. The emission rate is related to the temperature by the following equation

$$e_x = (\sigma \langle v_1 \rangle N_{d1}/g_1) / \exp(-\Delta E/kT) \qquad (4)$$

where σ is the carrier capture cross section, N_{d1} is the effective density of states in the carrier band, $\langle v_1 \rangle$ is the mean thermal velocity of the carrier, g_1 is the degeneracy of the trap level, ΔE is the trap activation energy and $x = 1$ (2) for an electron (hole) trap. The above equation can be drawn as a straight line plot of $\ln e_x$ vs. $1/T$ whose slope would be $\Delta E/k$. The main assumption behind this is that all other factors in Eq. (4) are independent of temperature. In fact, however, these parameters do vary with temperatures and so the value of activation energy is not a very accurate one.

A plot of $C(t_1) - C(t_2)$ vs. temperature goes through a peak when τ, the inverse of the transient rate constant, is of the order of $t_1 - t_2$. The value τ_{max}, the rate at which maximum $C(t_1) - C(t_2)$ is experimentally observed, and for exponential transients with infinitesimally short gate widths is given by

$$\tau_{max} = (t_1 - t_2)/[\ln(t_1/t_2)]. \qquad (5)$$

The emission rate (inverse of τ_{max}) at the peak of $C(t_1) - C(t_2)$ can be used along with temperature to get one point on the ln e_x vs. T plot. Other points are obtained similarly from other scans with different values of t_1 and t_2. This value of peak maximum can be used to measure trap concentrations from Eq. (3). The rate at which the thermal scan is done and the direction in which it is done does not effect the shape or position of the DLTS peaks as long as the temperature measurement device reads the true device temperature and the sampling does not distort the signal.

In order to get some points on the ln e_x vs. 1/T plot one will have to do a number of DLTS scans with different values of t_1 and t_2. The values of t_1 and t_2 can be varied in three different ways:

(1) t_1 is fixed while t_2 is varied

(2) t_2 is fixed while t_1 is varied

(3) Both t_1 and t_2 are varied with t_1/t_2 fixed.

The easiest of these methods is (3) since t_1/t_2 remains constant making it easier to calculate τ_{max}.

It should always be kept in mind that the above theory is valid for traps with exponential transients. This can however be used for relative comparisons of samples with non-exponential transients but the formulae listed earlier no longer apply. Concentration profiling of majority (hole) carrier traps are straight forward. A number of DLTS scans are done with majority carrier pulses of varying height up to a maximum value just below injection. A plot of signal height vs. majority carrier pulse height is plotted and this data is used to calculate carrier concentrations. The procedure for a minority, in this case an electron trap, is a little more complicated. It involves two pulses, the first of which is the normal saturation injection pulse and the second a majority carrier pulse of variable amplitude which empties the trap. A series of scans is made with progressively larger majority carrier pulses but unlike before, the signal destruction is plotted vs. pulse voltage and the concentration is given by

$$N(t+t_c) = N(t) \exp[-(1/T_1+e_1)t_c) \qquad (6)$$

where t_c is the width of the second majority carrier pulse, T_1 is the hole recombination rate

of a filled trap and N(t) is the concentration of filled traps at time t after the start of the injection pulse. This method of using two pulses to profile minority carrier traps is detailed in [9].

DLTS scans can be made sensitive to different type of traps by adjusting the width of the bias pulse to suit the capture rate of the trap. If the trap under scrutiny is a fast recombination center, the width of the bias pulse can be made very small such that only the faster traps get filled and the slower will not be appreciably filled. The resulting DLTS signal can be safely assumed as being due to the faster traps and thus can be profiled.

The DLTS method while being an extremely versatile one is not without its inherent drawbacks. It is incapable of detecting minority (electron traps on a p-type background) carrier traps in Schottky barrier diodes. The method behind profiling the minority trap is to have a sufficiently large and wide injection pulse that injects electrons into the depletion region. In the case of metal-semiconductor contacts, forward currents do not inject any carriers and hence the technique fails. The method also fails when the capture rate c_2 is so large that the trap empties itself before the measurements can be taken. Such cases can be profiled using a combination of DLTS and other methods.

2.5 Schottky Barrier Diode overview

2.5.1 Introduction

Schottky barrier diodes are usually fabricated by depositing metal layers on chemically cleaned semiconductor surfaces. When a metal and a semiconductor are brought in contact such that charge can flow between them, the Fermi levels line up and depending upon the doping of the semiconductor, the nature of the interface states and the work function of the metal, a rectifying contact can be formed [10]. An example band diagram of an ideal metal- p-type semiconductor interface is as shown in Figure 2.2. Figure 2.2 (a) shows the vacuum levels and Figure 2.2 (b) shows the actual interface. The quantity Φ_B is called

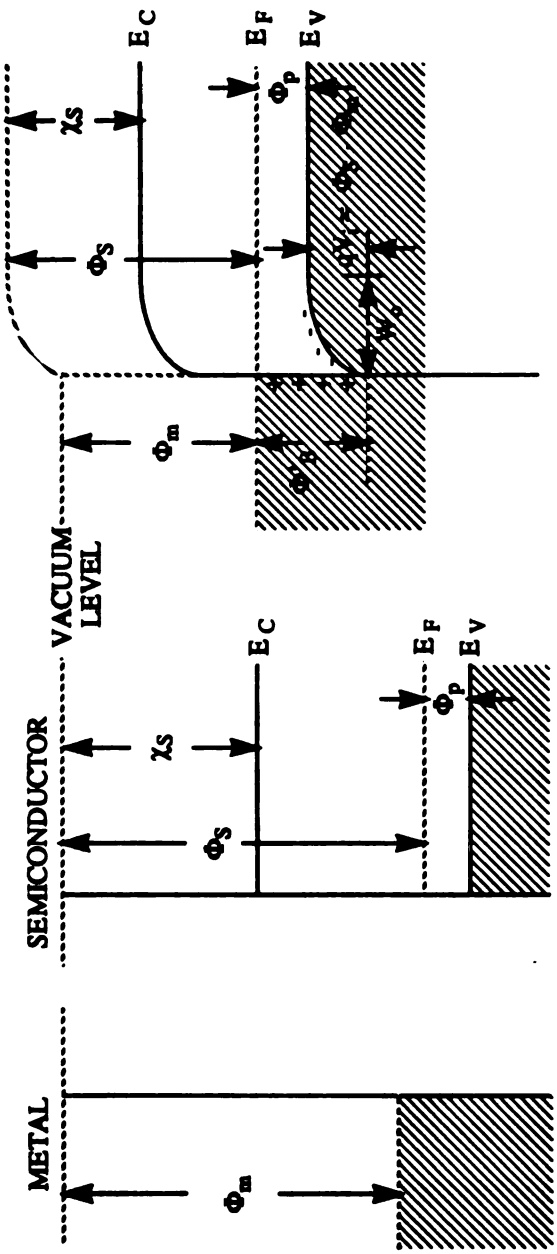


Figure 2.2. Electron energy band diagrams of metal contact on p-type semiconductor with $\Phi_m < \Phi_S$

the barrier height and under ideal conditions depends only upon the doping of the semiconductor and the metal work function. In real interfaces however, localized surface states may lead to pinning of the Fermi level and the barrier height would no longer be a simple function of the metal and semiconductor work functions. The fabrication of SBDs is fairly simple in terms of the number of fabrication steps, though care should be taken to ensure that clean surfaces are maintained. This allows one to study the effects of various processing steps on the semiconductor by examining the I-V, C-V and DLTS measurements of a SBD formed on that surface.

2.5.2 Capacitance - Voltage measurement

The change of capacitance of a reverse biased Schottky barrier diode with voltage can be used to determine the junction height of the metal-semiconductor contact. The basic assumption is that the semiconductor has uniform background doping and that all of the impurities are ionized. This method is used only in reverse bias because when a diode is forward biased the capacitance is shunted with a large conductance.

The depletion region capacitance of a diode can be considered equal to that of a parallel plate capacitor separated by the width of the depletion region and having the semiconductor as dielectric.This capacitance is given by

$$C = S\,[\varepsilon_s q N_b/(2(V_i + V_R - kT/q))]^{1/2} \qquad (7)$$

where N_b is the background doping, ε_s is the permittivity of the semiconductor, V_i is the contact potential, V_R is the reverse voltage and S is the area of cross section of the diode [10]. In this equation it has been assumed that an appreciable oxide interface layer does not exist and that the semiconductor is uniformly doped. If in the above equation $1/C^2$ is plotted vs. V_R, the result is a straight line with a slope of $2/(S^2\varepsilon_s q N_B)$ and an intercept on the voltage axis of $V_0 = (V_i - kt/q)$. The slope can be used to calculate the dopant concentration and the intercept to calculate barrier height. The barrier height is given by

$$\Phi_{Bn} = (qV_0 + \Phi_n + kT) \qquad (8)$$

$$\Phi_{Bp} = (E_g - \Phi_{Bn}) \qquad (9)$$

where E_g is the energy gap and Φ_{Bp} is the barrier height as seen by the holes. The kT factor comes due to the contribution of majority carriers to the space charge. Eq. (8) does not include effects due to image force barrier lowering.

In the case where background doping varies with distance into the semiconductor, the plot of $1/C^2$ vs. Voltage is not a straight line. The slope at any point in the characteristic can be used to calculate $N_b(W)$, where W is the distance into the semiconductor and is given by

$$W = (2\varepsilon_s|V_i - V_R|/qN_b)^{1/2} \qquad (10)$$

where V_i is the built in voltage and is calculated from the intercept of the slope with the V axis.

2.5.3 Current - Voltage measurement

The current in a SBD formed on high mobility semiconductors like Si or GaAs is due to emission of electrons over the barrier and is given by the relation

$$I = I_0 [\exp (qV/nkT) - 1] \qquad (11)$$

where

$$I_0 = SA^*T^2 \exp(-\Phi_B/kT) \qquad (12)$$

and n is the diode ideality factor, A^* is the modified Richardson constant, V is the applied bias and all other symbols are as defined earlier. For forward biases in excess of approximately $3kT/q$, a plot of ln I vs. V gives a straight line. The value of I_0 is the intercept of this line on the I axis. If all other values in Eq. (12) are known, the value of Φ_B can then be calculated. The value obtained this way is the zero bias barrier height and includes the image force effect on the barrier. The value of n is one for an ideal Schottky barrier diode, where the barrier height is independent of bias and the current flow is only due to thermionic emission. Factors that make n greater than one are the bias dependence of barrier height, electron tunneling through the barrier and carrier recombination in the depletion

region. Carrier recombination causing an increase in n is an important factor in Si diodes with doping concentrations less the 10^{15} cm^{-3} because of relatively large depletion layer widths. In devices operating under high injection conditions an increase in n is due to the enhanced minority carrier drift in the quasineutral region caused by the drift field. The value of n also increases from unity due to the field dependence of barrier height. This field dependence arises either due to the presence of the insulating interfacial layer or due to image force lowering of the barrier. Since a part of the applied voltage appears across the interfacial layer, the barrier height becomes voltage dependent. The interfacial layer also causes the zero bias barrier height to be lower than it would be in the absence of this layer.

The thermionic emission theory predicts that under reverse bias, the reverse current should saturate to the value I_0 given in Eq (12). This saturation is not observed in practical diodes, rather the reverse current is seen to increase with reverse voltage. This is caused in part due to the dependence of barrier height on bias. Other phenomena that cause this are the tunneling of electrons from the metal into the semiconductor conduction band and the electron-hole pair generation inside the depletion region. For large barrier heights and low dopant concentrations, the injection of minority carriers from the semiconductor into the metal may also be important.

2.6 Chemical Spectroscopy methods

2.6.1 Introduction

Chemical spectroscopy techniques are often used to explain the effects of processing on the electrical characteristics of a device in terms of changes in chemical composition. It is known that even traces of contaminants like sodium can cause a very large change in the electrical behavior of the fabricated device. The spectroscopy methods provide a way of detecting contaminants which may have been introduced during fabrication.

2.6.2 XPS overview

X-ray Photoelectron Spectroscopy (XPS) [11] involves the adsorption of photons resulting in the prompt emission of photoelectrons from the excited atom. All electrons with a binding energy below the X-ray photon energy may be emitted.The resulting photoelectron spectrum has characteristic peaks corresponding to chemical elements and their associated compounds, which may be compared with available charts. Shifts in the peak shapes and positions can be used to yield bonding information. These shifts can be used to distinguish between, say, silicon bonded to silicon and silicon bonded to oxygen. The photoelectrons have an escape depth of 5-30 ^{0} A for most conducting materials thus allowing for surface sensitive analysis. It is the combined advantages of high surface sensitivity, chemical bonding determination and non-destructive analysis capability that makes this technique so attractive for surface analysis. XPS is also less susceptible to sample charging than other ion and electron based techniques used for analyzing nonconducting polymers. This allows for analysis of polymers used in lithography of semiconductor and organic residues picked up during processing or packaging. Unlike other ion-beam techniques, XPS is non-destructive and has no inherent depth profiling capability. Even angle resolved XPS is limited to near surface region. Sequential ion beam sputtering can be used to remove layers of the material and then XPS measurements can be done to obtain a qualitative depth profile. It should be kept in mind that data obtained by this means may not be very accurate due to the distortion of the true chemical bonding environment caused by the energetic ion beam used for sputtering. Recent developments in XPS have allowed analysis of small areas with computer controlled analysis. Small spot size is achieved by collimating the X-ray beam to a region of approximately 150 μmeters. However this causes low flux rates leading to increased counting time. To avoid surface contamination most XPS equipment operate in an ultrahigh vacuum environment.

Surface analysis by XPS is often done by irradiating the sample with mono-energetic photons and examining the electrons emitted. Mg K α (1253.6 ev) or Al K α (1486.6 ev) are commonly used X-ray sources. These irradiated photons cause photoionization of

the atoms in the surface region of the sample, resulting in emission of two types of electrons, photoelectrons and auger electrons. The probability of interaction of these emitted electrons with matter far exceeds those of the photons. Therefore even though the photons can penetrate up to tens of microns, the emitted electrons can escape out of only tens of angstroms. The electrons leaving the surface region are detected by an electron spectrometer according to their kinetic energy. The analyzer is operated within a fixed narrow range referred to as "pass energy". Therefore, the narrower the region, the higher the resolution of the energy scan. Scanning for different energies is accomplished by electrostatically retarding the electrons before they reach the detectors. This retardation voltage may be varied between zero and the incident photon energy. For a typical surface where the surface composition is unknown, a wide scan "survey spectrum" of the surface is obtained and then a narrower detailed scan for selected peaks is done.

2.6.3 Auger Electron Spectroscopy

A focussed electron beam impinging on a specimen causes numerous beam specimen interactions to take place. This results in electron signals and X-rays being produced. Auger Electron Spectroscopy (AES) [11] measures the energy of the Auger electrons emitted from the first few atomic layers of the material. The AES technique for chemical surfaces is based on the Auger radiationless process. In practice, a specimen is bombarded with a focused beam of electrons in ultrahigh vacuum. Incident electrons ionize atoms in the material, creating vacancies in their inner electron shells. As the ionized atoms relax to a lower energy state, these vacancies are filled by electrons from a lower energy shell. The transition to a lower energy state is accompanied by the emission of energy in the form of an x-ray photon or an "Auger electron". This phenomenon was first described by Pierre Auger who noticed this transition while working with x-rays.

The emitted Auger electrons are detected by an electron spectrometer and their energies are measured. The distribution of Auger electron energies are recorded as Auger

spectra. These spectra consist of peaks denoting specific Auger electron energies in the total energy distribution produced by the incident beam. The energies of Auger electrons are characteristic of the emitting elements. Thus peak identification leads to determination of a sample's surface elemental composition. Unlike XPS, AES allows the use of a very small probing beam, on the order of 1 μmeter in size. However, XPS is better suited for obtaining bonding information.The two methods are often used in a complementary fashion.

Chapter 3

Experimental Methods

3.1 Introduction

This chapter describes the methods used to fabricate Schottky barrier diodes as well as the methods for performing DLTS, C-V and I-V measurements on these diodes for etched and unetched specimens. In addition, the etching procedure and etching conditions are described.

3.2 Description of SBD fabrication

For this research, 3 inch diameter p-type silicon wafers, with resistivities between 6 to 18 Ω-cm, corresponding to a background doping of approximately 7×10^{14} cm^{-3} to 2×10^{15} cm^{-3}, were selected. Each wafer was initially cleaned with boiling TCE, followed by a degrease etch and a demetal etch to remove organic and metallic contaminants. The wafer was then oxidized at 1000 ^{o} C temperature to grow a 2000^{o}A thick oxide layer on both sides. The oxide on the back was stripped using a buffered oxide etch. The sample was then placed in a diffusion furnace with a boron source for 20 minutes so as to allow a shallow but high concentration boron doping on the entire back of the wafer, thus forming a p^{+} layer. The residual boron glass on the surface was stripped using a borosilicate etch. The sample was then metallized in an electron beam aluminum evaporator forming a 4500^{o}A thick layer of aluminum on the back. Good ohmic contact was ensured by annealing the sample for 20 minutes at 400^{o}C in an annealing furnace. Next, the oxide layer on the front surface of the wafer was stripped using a buffered oxide etch and half the sample, obtained after cleaving the wafer along a (100) crystallographic axis, was selected for plasma etching.

Immediately before the plasma etching, the samples were dipped in 9:1 DI:HF

solution to remove any native oxide. This was done because silicon tends to react spontaneously with the oxygen in the air to form a "native" oxide. Then the samples were rinsed for one minute in running DI water and subsequently dried with a vapor phase IPA rinse. After etching one half of the wafer, both the unetched and etched samples were rinsed in running de-ionized water and dipped in 9:1 DI:HF solution to remove any native oxide growth. The samples were then cleaned with boiling TCE followed by an acetone, methanol and two minute DI rinse. The samples were dried using vapor phase IPA. The unetched and etched samples were then immediately placed in the electron beam evaporator and the setup was pumped down to 10^{-7} torr. Aluminum was evaporated using a shadow mask with holes of 1.8 and 2.6 mm diameter, to form Schottky barrier diodes. The aluminum evaporated onto the surface was approximately 2400 ^{o}A thick.

It should be particularly noted that extreme care was taken to avoid any external contamination and to ensure that the two Schottky diode samples (etched and unetched) were identical except for the damage/effects of the plasma etching. This was done to ensure that the results of subsequent measurements on the Schottky diodes fabricated on the two surfaces can be subject to reliable relative comparisons. The characteristics of these different types of diodes are discussed in chapter 4. It will be seen that the extra clean control samples, henceforth labelled type A, show remarkable uniformity and near ideal C-V characteristics.

The flow chart in Figure 3.1 shows the various fabrication steps involved in the fabrication of the diodes. Detailed explanation of the various processes and chemicals used in the above fabrication can be obtained from Reinhard [12]. Another set of diodes was fabricated for which the degrease and demetal etch steps as well as the native oxide removal step prior to metallizing was omitted. These diodes, labelled type B, showed non-uniform electrical characteristics. The electrical characteristics of these diodes are included in Section 4.2 to emphasize upon the importance of the omitted steps.

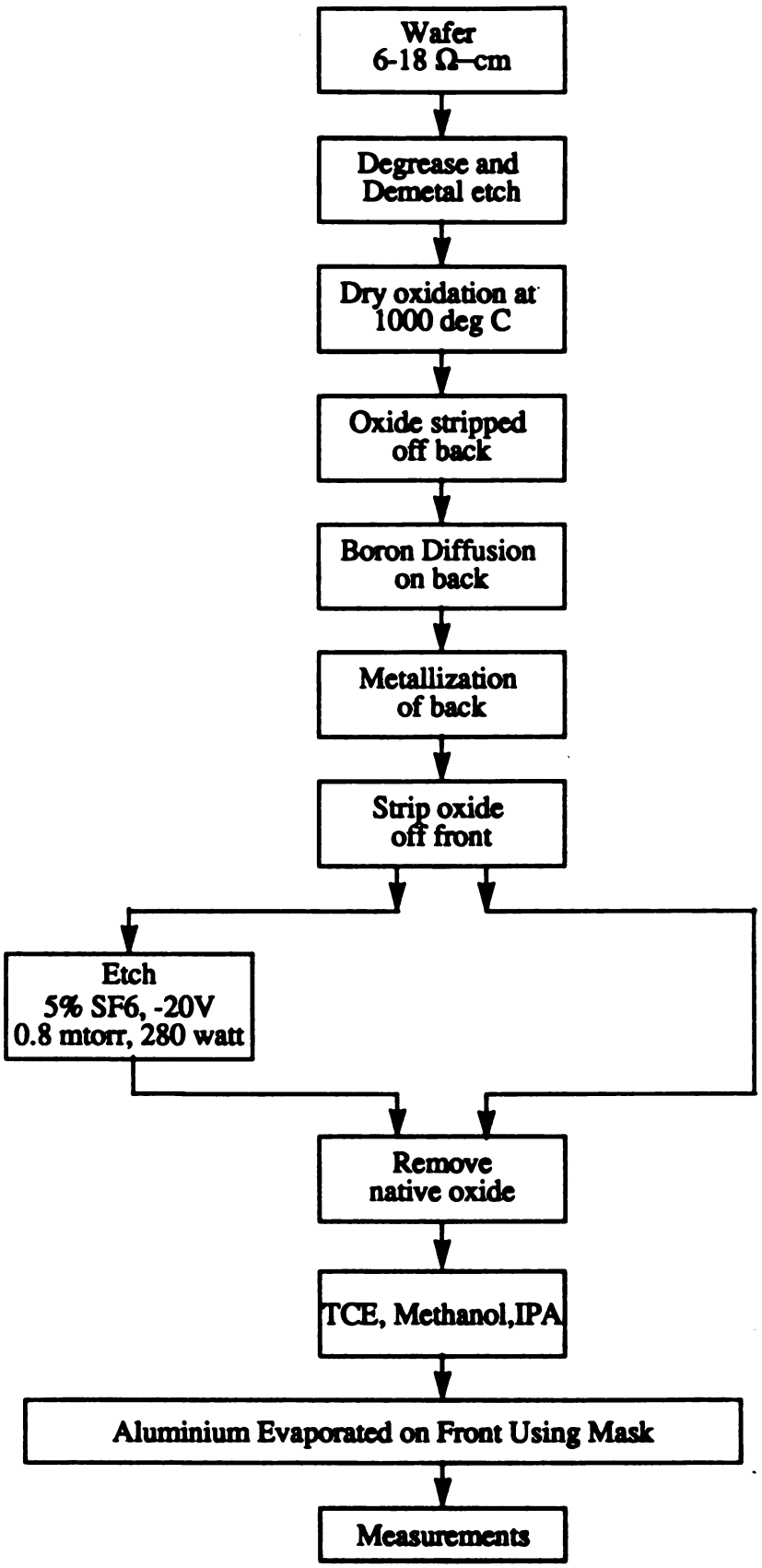


Figure 3.1 Steps involved in the fabrication of the etched and unetched diodes

3.3 Etching Procedure

The particular MPDR 325 plasma source used for this study has been described in some detail by Musson [13]. The etching gas used in the experiment, SF_6, has been shown by Hopwood [14] to have a higher etch rate than CF_4. This has been speculated to be because of the availability of higher number of neutral fluorine atoms in the plasma. The gases used in this experiment typically consisted of small fractions of SF_6 mixed with Argon. In order to provide a DC bias, the back of the wafer was coated with a graphite based conducting paint to ensure good electrical contact to the aluminum wafer holder which was uncooled. For most of the reported results, three 3 inch diameter wafers were simultaneously etched in the MPDR 325 at 0.8 mTorr, biased at -20 volts DC, and was placed 15 cm downstream with 5% SF_6 for approximately 15 minutes. Since the thrust of this research was a comparison of analysis methods, emphasis was not placed on systematically varying the etching conditions. When the etching was completed, microwave power and SF_6 flow were halted but the argon was allowed to flow for approximately one minute to help remove residual sulfur or fluorine. A more detailed description of the etching setup and procedure can be obtained in Musson [13]. The graphite paint on the back of the wafers could be easily removed using an ultrasonic bath of acetone. A type B sample was also etched in the same plasma source but under different conditions.

3.4 DLTS experiment

3.4.1 DLTS setup

The DLTS setup used in order to conduct the experiment is interconnected as shown in Figure 3.2. The whole setup has been programmed and controlled via the Hewlett-Packard Interface Bus (HPIB). A brief description of the various components and their interconnection is given as follows.

1) Displex refrigeration system: This is a closed cycle refrigeration system employing

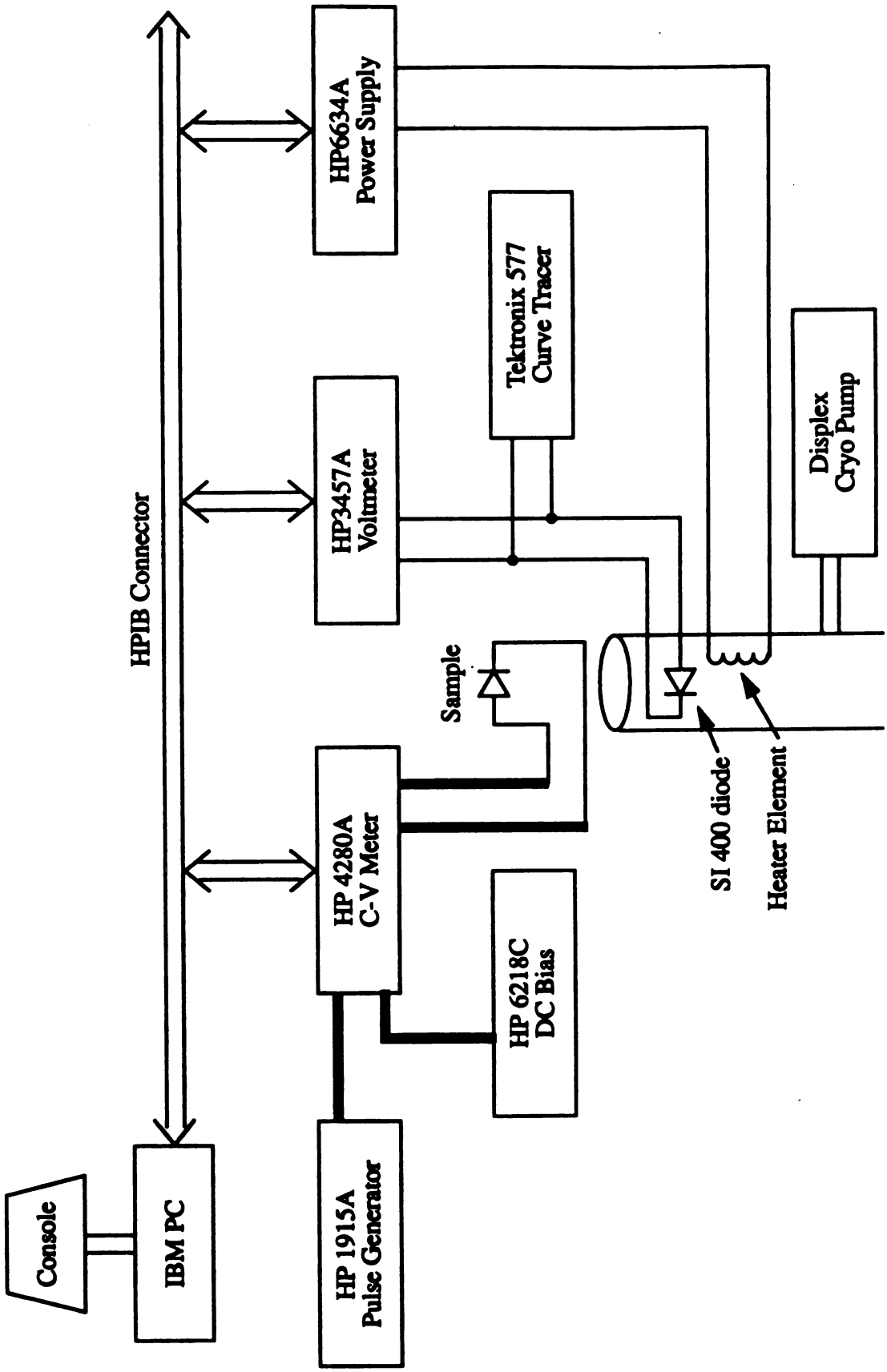


Figure 3.2 Block diagram of the DLTS interconnections

helium as a working medium. The system is capable of variable refrigeration between room temperature and 10 ^{0}K. The system consists of

a) The compressor module which includes a one cylinder, hermetic, oil cooled compressor designed for use in commercial air conditioning systems. Heat developed by during compression is rejected by a heat exchanger wrapped around the case and secured with high thermal conductivity epoxy.

b) The expander module which is the refrigeration producing mechanism in the system. It has a reciprocating expander which is gas actuated and gas loaded.

c) A calibrated SI 400 diode (manufactured by Scientific Instruments) whose voltage vs. temperature characteristics are accurately known for a biasing current of 100 μamperes.

d) A 50 ohm heater coil to heat the sample to the required temperature.

2) Vacuum pump: The vacuum pump is required to form a good working vacuum below 5 mTorr to reduce thermal heat transfer from the sample to the case and allow efficient functioning of the Displex system.

3) HP 4280A 1 Mhz C-V meter: This instrument is capable of capacitance, capacitance vs. voltage and capacitance vs. time measurements. In this case it is used in the C-t mode wherein it is capable of sampling rates up to 10 μseconds using an external pulse generator and up to 10 ms using its internal pulse generator. In the "fast" transient measurement mode the instrument is capable of measurements with up to 10 femtofarad resolution. The instrument offers up to 14 combinations of grounded or floating connection modes and a choice of internal or external pulse bias sources.

4) HP 6634A DC power supply: This single output power source is capable of an output up to 100 volts at 1 ampere current. This is used to control the voltage across the heater unit to arrive at the desired temperature.

5) HP 3457A programmable multimeter: This is used to measure the voltage across the calibrated SI diode. The software running on the PC converts this voltage to its equivalent temperature and programs the power source accordingly.

6) Tektronix 577 curve tracer: The curve tracer is operated in the DC mode and supplies a bias current of 100 μamperes required for correct functioning of the SI 400 diode.

7) HP 6218C DC bias source: This source sets up the quiescent conditions of the sample by supplying a reverse bias voltage of 6 volts across the sample. Further details are given in Section 3.4.3 under measurement details.

8) HP 1915A variable transient time output: The pulse generator is used in those measurements requiring the sampling rate to be faster than 10 ms. The pulse generator forms part of the "connection mode 14" circuit detailed later. The pulse source is used in the external width mode after setting its output voltage to 6 v pp and 0 v offset. The output of this source is terminated in a 50 ohm feed through load so as to prevent any changes in the impedance the HP 4280A sees.

9) IBM PC with 640 K RAM, is used as the control and programming center of this setup. The PC is equipped with a HPIB control card. The software requirements are a Microsoft C compiler version 5.1 and a HPIB command library version 1.1 or higher. The software is written in C and a commented listing of the program forms Appendix B. The software has been compiled using the above compiler and linked with the command library.The details of the measurement setup is given in the Section 3.4.3 and detailed instructions to repeat the experiment are given in Appendix A.

3.4.2 Measurement procedure

The cryogenic unit has no temperature control as such. The temperature measurement and control is in the form of a calibrated diode and a heater element present inside the cryogenic unit. In view of this, the cryogenic unit is allowed to cool down to its lowest temperature, reaching approximately 40 ^{0}K for the vacuum pump used in this study. The SI 400 calibrated diode has an operating current of 100 μamperes which is supplied by the curve tracer. The voltage across the diode is measured and converted to its temperature equivalent by the controlling software. Temperature control is achieved by changing the voltage across the internal heater element from the programmable voltage source and continuously monitoring the voltage across the diode. The software is capable of maintaining the sample at a

temperature within a margin of 2 ^{0}K of the desired value. When the desired temperature is reached, the C-t meter is programmed to take six readings in intervals of t_1.

The software written for the purposes of this research requires an input file containing the number of readings to be taken and the respective temperatures at which these measurements are to be made. The minimum difference between successive readings has to be at least 2 ^{0}K. In order that the readings be taken most efficiently, the required temperatures should be in an increasing order of magnitude. The software goes through five iterations before taking a reading thus ensuring that the temperature is within the allowed margin. The readout is automatically written into a file and the filename of which is in increasing numerical order, the readout at the first temperature being written into filename "0". A typical run of the software for a set of 46 readings between 65 ^{0}K and 280 ^{0}K takes approximately 6 hours. The software has been made efficient in the sense that it "remembers" the previous heater voltage requirements to reach the earlier temperature and increments this value to efficiently reach the next higher temperature. This is the main reason why it is most efficient to take readings in an increasing order of magnitude. Detailed setup and measurement procedures are listed in the appendix A and the source code is presented in Appendix B.

3.4.3 Measurement details

The main aim of the DLTS experiment was to compare the spectra of a device fabricated on silicon before and after etching and hence study the effects of ECR etching on device fabrication in terms of deep trap generation. The device chosen for this experiment was the Schottky Barrier diode. Since the SBD has a one sided junction, all of the depletion region is present in the semiconductor being studied. Theoretically this makes the sample relatively easy to analyze, however, a major drawback in this approach is that DLTS on SBDs is incapable of detecting minority carrier traps. In this case, since the background doping made the wafer p-type, only hole traps could be detected.

A wafer was cut up into four quarters and Schottky barrier diodes were formed on

one quarter by following the steps detailed in Section 3.2. DLTS thermal scans were done on the sample with "t_1" values being 1ms, 5ms, 11ms, 16ms and 20ms. At each of these values six readings were taken i.e. at t_1, $2t_1$, $3t_1$ etc. This led to a rich combination of $t_1$and t_2 which was manipulated on the "UNIX" system using the "NCAR" graphics plotting routine. The HP 4280A is capable of 10 fF resolution in the "fast C-t" mode of operation. The values of $(C(t_2) - C(t_1))/ C_\infty$ were plotted as a function of temperature. A variation of less than 2 femtofarad was ignored allowing for the last digit fluctuation of data in digital instruments. It can be seen here that of the three DLTS measurement modes detailed in Section 2.4, option 2 was chosen. This was partly because of simplicity of calculation and also due to HP 4280A measurement characteristics. However all three measurement modes can be obtained in software by simply manipulating the readings t_1 through t_6 to get the best result. For example, if the values at t_1 and $4t_1$ are considered as the first and the second value for DLTS measurement, the difference would be $3t_1$ and ratio would be 4, leading to a value of τ_{max} of 1.386. This methodology leads to the large combinations of t_1/t_2 mentioned earlier.

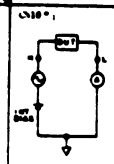
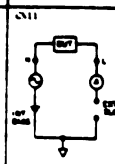
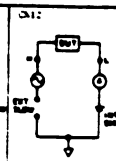
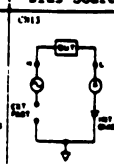
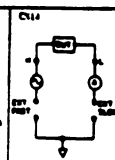
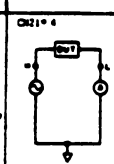
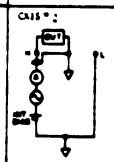
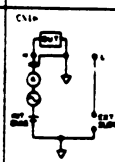
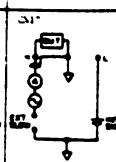
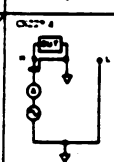
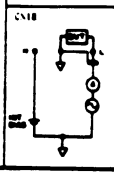
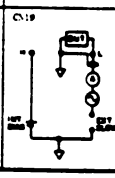
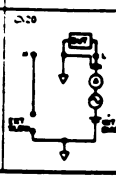
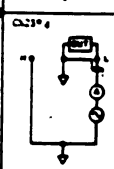
The second quarter was then etched following the etching procedure detailed in Section 3.3 and SBD was formed on the top surface following the same steps used to fabricate the unetched diodes. These were mounted on the DLTS setup and the same scan was done on these. A detailed discussion of the results is done in Section 4.5.

The selection of the time "t_1" was done with a lot of deliberation. The decay of the diode junction capacitance due to a pulsed bias can be considered as being made up of two components; a fast natural RC type decay of the junction capacitance and a factor due to the slow decay of charge due to traps. It was the latter which was investigated for the DLTS purposes. This leads to a search for a "t_1" which is slow enough to allow the decay of the fast transient and fast enough to catch the effects of the slow transient. A test with t_1 of 1 μsecond (the fastest the HP 4280A can measure) showed the effects of the fast transient. After several trial and error measurements, the values of "t_1" listed above were chosen. The value of 11ms was seen to highlight the desired effects.

The HP 4280A C meter is capable of a number of different circuit connections to suit various needs. This experiment connected the sample to the meter and to other instru-

Table 1 Connection modes of the HP4280A CV meter

(excerpted from "4280A, 1Mhz C meter / C-V plotter," HP 1987)

DC Bias / Sample	Internal DC Bias Source	Internal and External DC Bias Sources		External Fast Pulse Generator*3 and Internal or External DC Bias Source		None
FLOATING						
GROUNDED						
						

*1: Set when the FLOATING key is pressed.

*2: Set when the GROUNDED key is pressed.

*3: Used when delay time, td, for a high speed C-t measurement is less than 200 μs.

*4: L-R measurement. Used when test lead impedance is to be measured for error correction.

ments in two connection modes. The measurements which required readings for times less than 10ms, i.e., the readings at 1ms and 5ms, needed the HP 1915A to supply the biasing pulses.This setup used the connection mode 14 shown in Table 1. The readings at 11ms, 16ms and 20 ms can be done using the internal pulse generator of HP 4280A. Connection mode 11, also shown in Table 1, was used for these readings. When the external pulse generator is used, care should be taken to terminate the generator in a 50 ohm load so as not to introduce additional impedance into the circuit. Another precaution is to make sure the pulse generator does not supply a DC offset in the external width mode. Please refer to appendix A for details about this problem.

3.5 Description of I-V and C-V measurements

3.5.1 Introduction

The I-V and C-V measurements can be used to obtain details of the SBDs as described in Section 2.5. The C-V capability of the HP 4280A capacitance meter was used to measure the C-V characteristics and a semiconductor parameter analyzer, HP 4145B, was used for the I-V measurements.The various samples used were of two sizes, the small one of 1.8 mm diameter and the large one of 2.6 mm diameter. In each of these sizes four types of diodes were used; etched and unetched of types A and B. In each of these categories four diodes were used leading to a total number of 32 readings. This was done to measure the effect of etching on various locations of the surface and the effects of post and preprocessing on the quality of the final diode. The fabrication and etching details are given in Sections 3.2 and 3.3 respectively.

3.5.2 I-V measurement details

The HP 4145B semiconductor parameter analyzer used for this experiment is designed to measure, analyze and graphically display the DC characteristics of a wide range of semiconductor devices like diodes, bipolar transistors, field effect transistors, ICs, etc. Amongst other accessories, it is equipped with four Source/Monitor units (SMUs), two programmable voltage source units (Vs), two programmable voltage monitor units (Vm) and a removable floppy-disc storage unit. In order to connect the instrument with user furnished test fixtures like wafer probing stations, the instrument can be interfaced with a rectangular connector plate equipped with four BNC connectors and four triaxial connectors which can be used to provide the necessary electrical contacts to the sample.

For I-V measurements the analyzer was used in the "diode VF-IF" mode of operation. The analyzer was interfaced to a wafer probing station through the connector plate. The base plate of the probing station was used as the bottom contact while a probe was used for the top contact. Since the forward bias characteristics of the Schottky barrier diode were of interest, 100 readings were taken between 0.01V and 1V in steps of 0.01 volts. The measured values were stored in the local floppy drive and later transferred to the "UNIX" system to be plotted using "gnuplot". These measurements were done in a light proof enclosure because the diodes possessed photovoltaic properties. The theory behind this experiment is discussed in Section 2.5.3.

3.5.3 C-V measurement details

For these measurements the C-V mode of the HP 4280A was used. In this mode the meter can generate a single or double staircase voltage sweep from its internal bias source. The start, stop and step voltages for the staircase sweep are user selectable. In addition, the "hold" time and the "step delay" time are also user selectable. The "hold" time sets the bias stabilization time at the beginning and end of the bias sweeps made with the internal bias

source and the "step delay" time sets the bias stabilization period for each step of the internal source. The instrument measures the capacitance after these two times.

The capacitance meter was programmed over the HPIB bus to have a "step delay" time and "hold" time of 30 ms each. It was noticed that times less than this caused bus time-out errors on the HPIB. The instrument was set in connection mode 10 for these measurements. The start voltage was set at -6 v, the stop voltage at 0 v and the step at 0.4 v leading to a total of 16 readings. It was noticed that light increased the steady state capacitance of the device, hence all measurements were done by placing the sample in a light proof black box. The resulting data was transferred to the "UNIX" system and used to calculate $1/C^2$ and background doping by methods detailed in Section 2.5.2. The results of this experiment are discussed in Section 4.2.

Chapter 4

Results

4.1 Introduction

This chapter describes the results of the electrical measurements conducted on the Schottky barrier diodes formed on etched and unetched silicon. In addition this chapter also discusses the results of preliminary XPS and Auger studies of etched silicon samples.

4.2 C-V characteristics before and after etching

Ideal $1/C^2$ vs. V characteristics of Schottky barrier diodes, as discussed in Section 2.5, are straight lines and information about background doping and barrier height can be obtained from these plots. The characteristics of diodes formed on unetched silicon with pre-evaporation cleaning are in fact are seen to be very close to ideal as shown in Figures 4.1 and 4.2. The characteristics of the eight samples, four large ones of 2.6 mm diameter and four small ones of 1.8 mm diameter, were all similar. This is an indication of the isotropy of the surface with regard to carrier concentration and surface states as would be expected for an unprocessed wafer. Figure 4.1 and Figure 4.2 show the characteristics of the large and the small diode respectively.

The carrier concentration was calculated from the slope of the line and was found to be in the range of 6.41×10^{14} /cm^3 to 6.72×10^{14} /cm^3 for the large diode and for the small diode, between 5.87×10^{14} /cm^3 and 6.32×10^{14} /cm^3. This difference in the carrier concentrations as calculated from the two lines can be attributed to the error in measuring the diameter of the two samples. It should be kept in mind that in the formula used to calculate the doping, the diameter of the diode is raised to the fourth power and hence small errors in diameter measurement tend to be magnified. The value of the background doping calculated from the C-V plot is in agreement with the background doping of the chosen

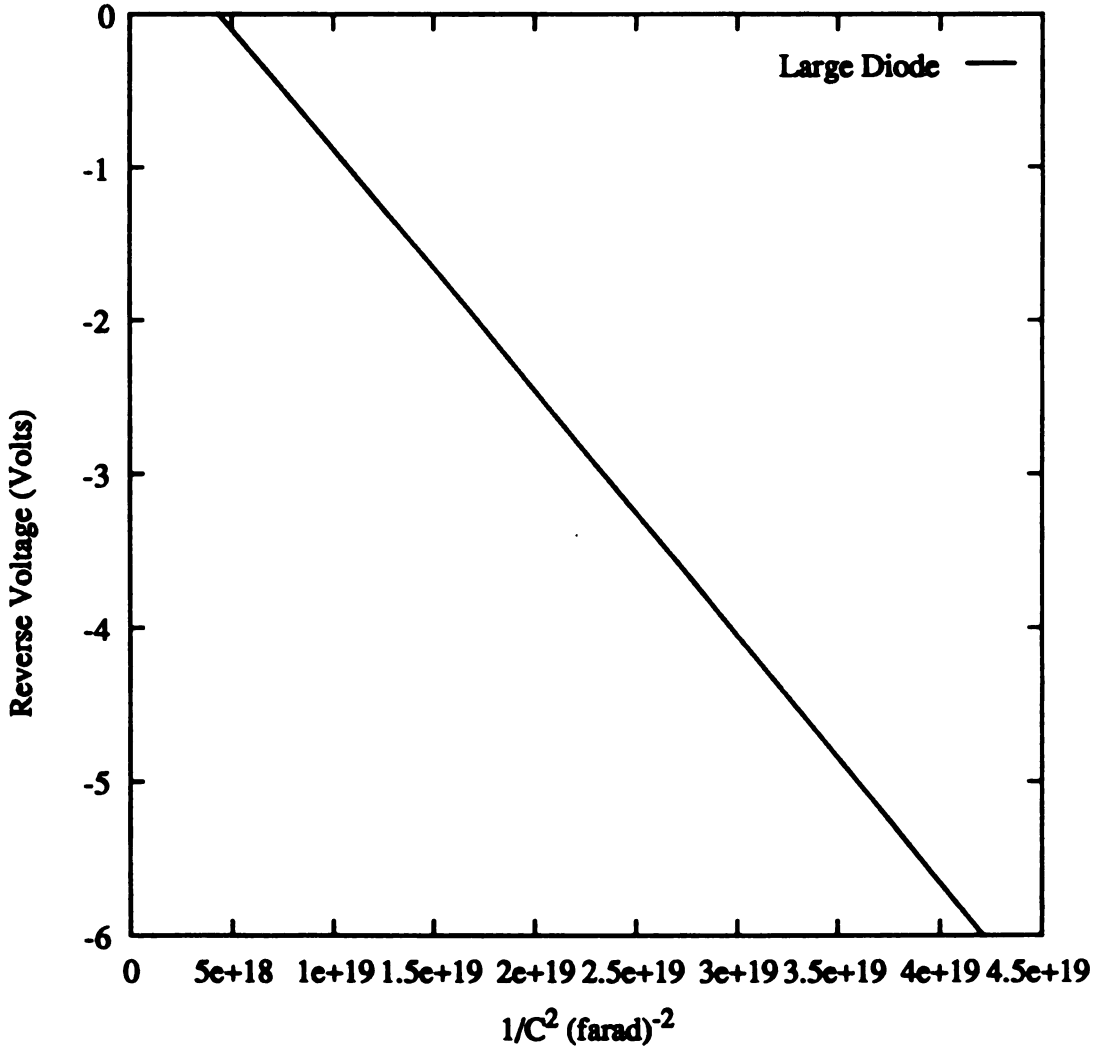


Figure 4.1 Plot of $1/C^2$ vs. V for the large diode formed on unetched silicon

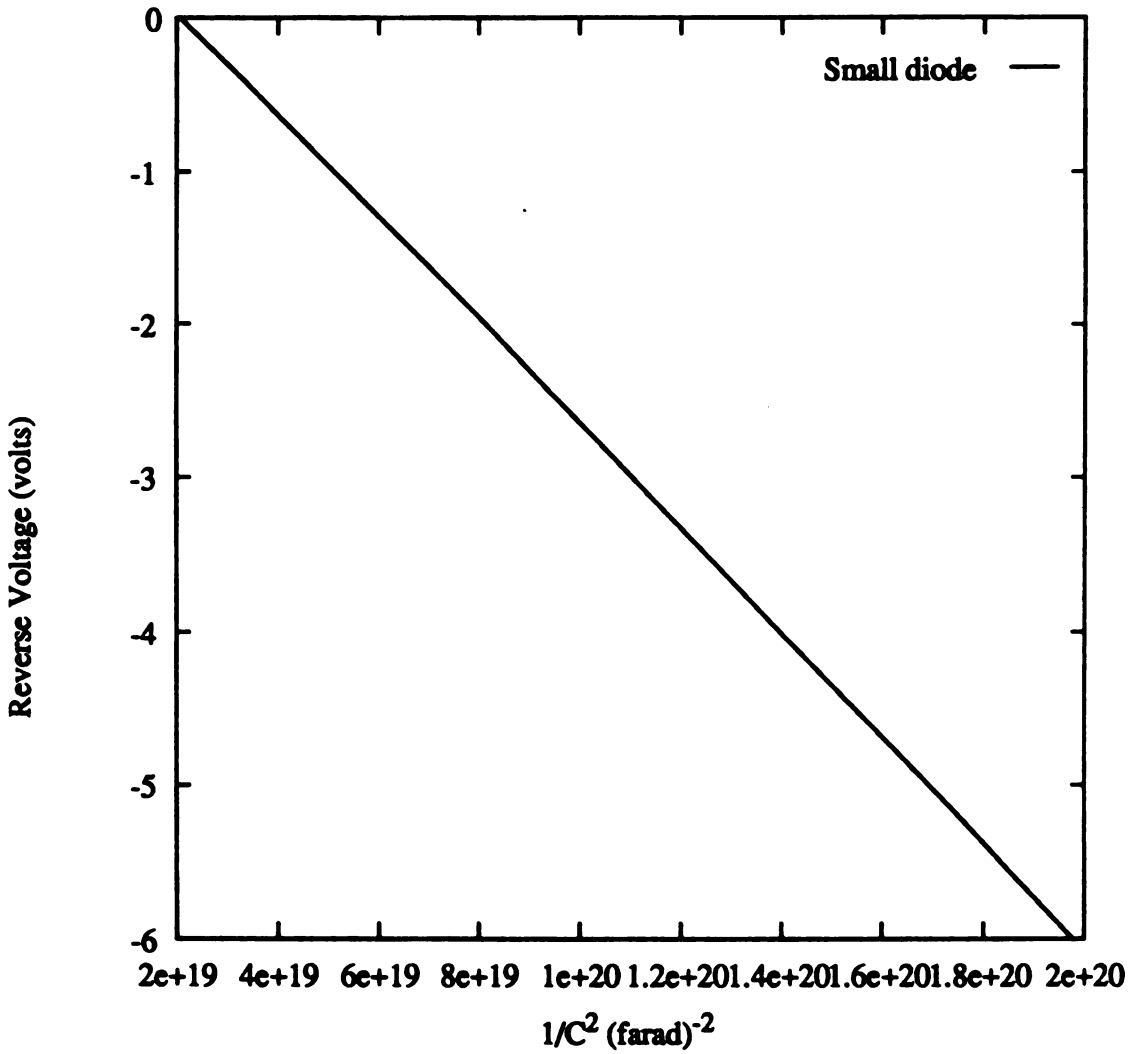


Figure 4.2 Plot of $1/C^2$ vs. V for the small diode formed on unetched silicon

wafers. The variation of doping with distance into the wafer for the small and large diode is plotted on the same scale and shown in Fig 4.3. The worst case variation in the calculated doping is about 5% for the large diode and 7% for the small one. The value of the intercept of the $1/C^2$ plot with the voltage axis, V_0, is the same for both the large and small diodes and is equal to 0.7 volts. The value of Φ_{Bn}, assuming an average value of 6.5×10^{14} /cm^3 for the background doping, can then be calculated from Eq. (8), Section 2.5.2 and is equal to 0.98 volts.

The importance of native oxide and other impurity removal from the surface before aluminum metallizing the surface is illustrated by the C-V plots shown in Figure 4.4 of other SBDs fabricated without this step being taken. It can be seen that even though the plots are straight lines the values vary from sample to sample. This points to the non-uniform nature of an uncleaned surface which leads to unpredictable results.

The C-V plots of diodes formed on the etched surface are shown in Figure 4.5 and Figure 4.6 for the large and the small SBDs respectively. The most noticeable aspect of the plots are that they are no longer straight lines in spite of cleaning prior to etching and prior to SBD formation. This leads to the conclusion that the background doping is no longer a constant with respect to distance in the semiconductor. The plot can be considered to be piecewise linear and the slope and hence the carrier concentration can be calculated at each point. Figure 4.7 and Figure 4.8 show the variation of doping vs. distance for the large and the small SBDs respectively. It is seen that there is a significant reduction of effective dopant concentration at the surface and there is a gradual rise in the effective dopant concentration with distance into the semiconductor. It can be seen in Figures 4.8 and 4.9 that for both diodes, etching has somehow caused dopant compensation to a distance of nearly 6 μmeters. Specifically for the small diode, the doping varies from a value of 1.5×10^{14} / cm^3 at 5.2 μmeters to a value of 6×10^{14} /cm^3 at 6.6 μmeters.

Etching produced dopant compensation has been previously reported. For example, hydrogen has been claimed to cause carrier passivation in silicon and GaAs. Hydrogen present in etching gases has been shown to cause carrier reduction up to a distance of nearly 6 microns in the case of p-type silicon [7] similar to the results shown in Figures 4.7 and

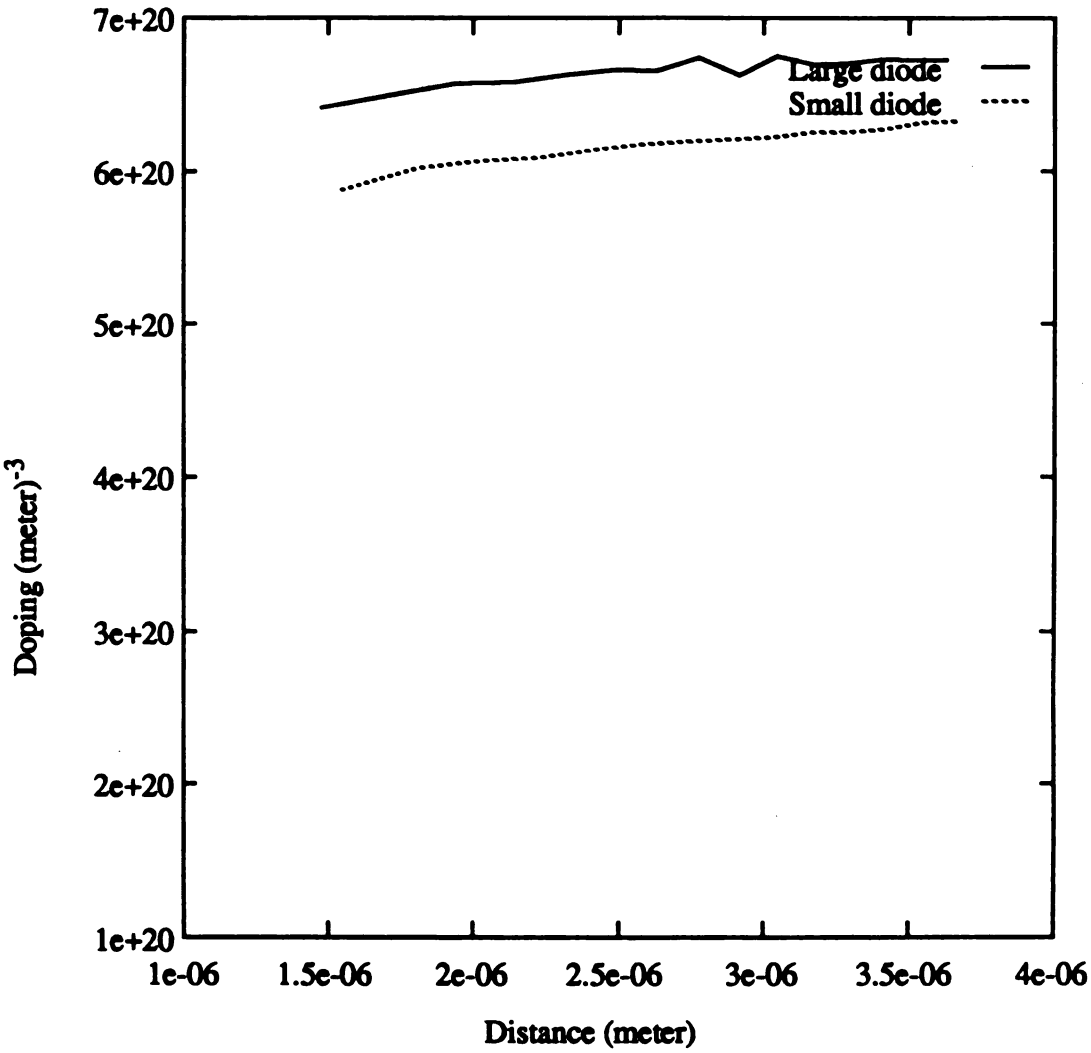


Figure 4.3 Variation of doping vs. distance in the unetched diodes

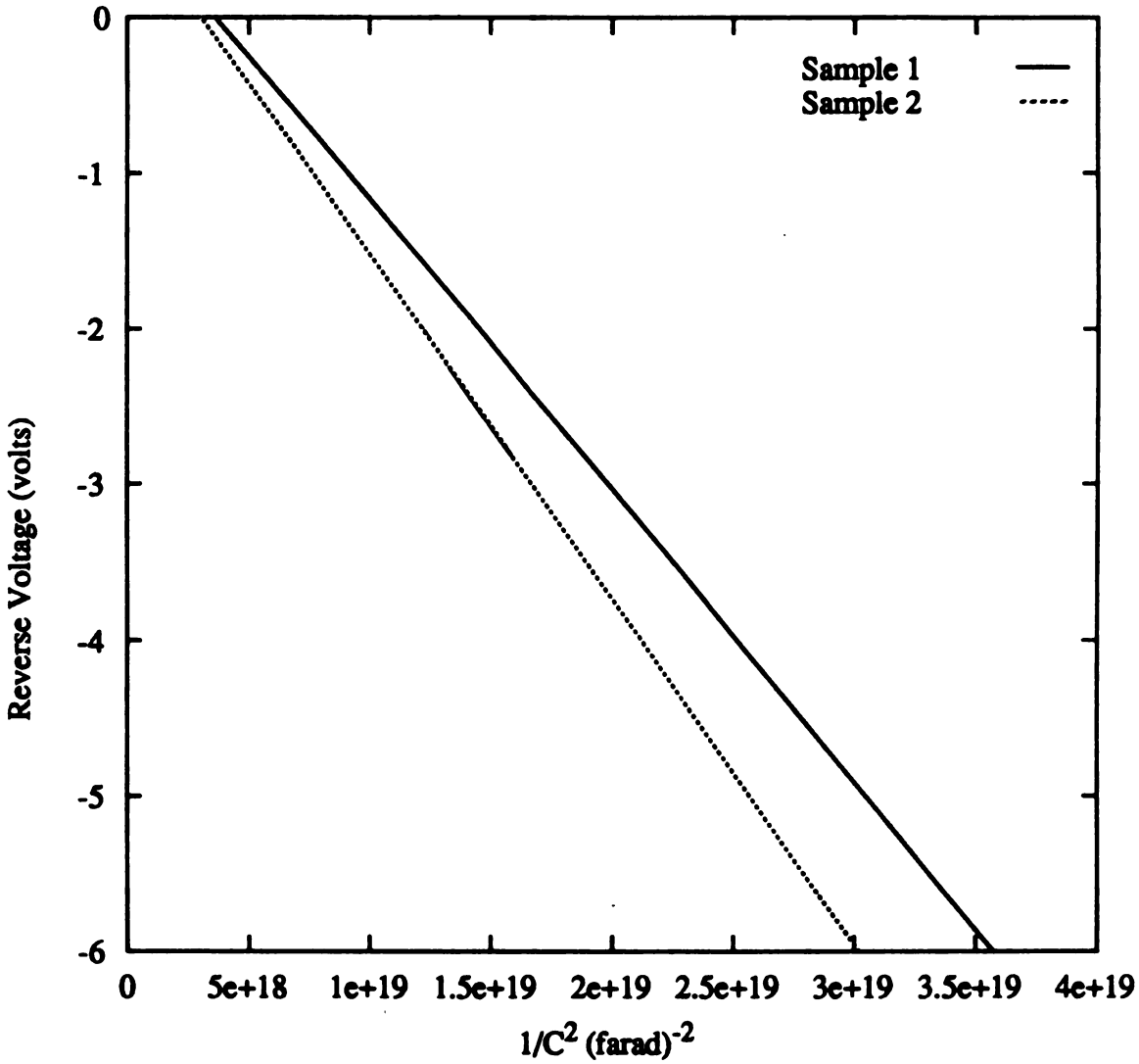


Figure 4.4 Variation of capacitance on unclean surface for two different samples

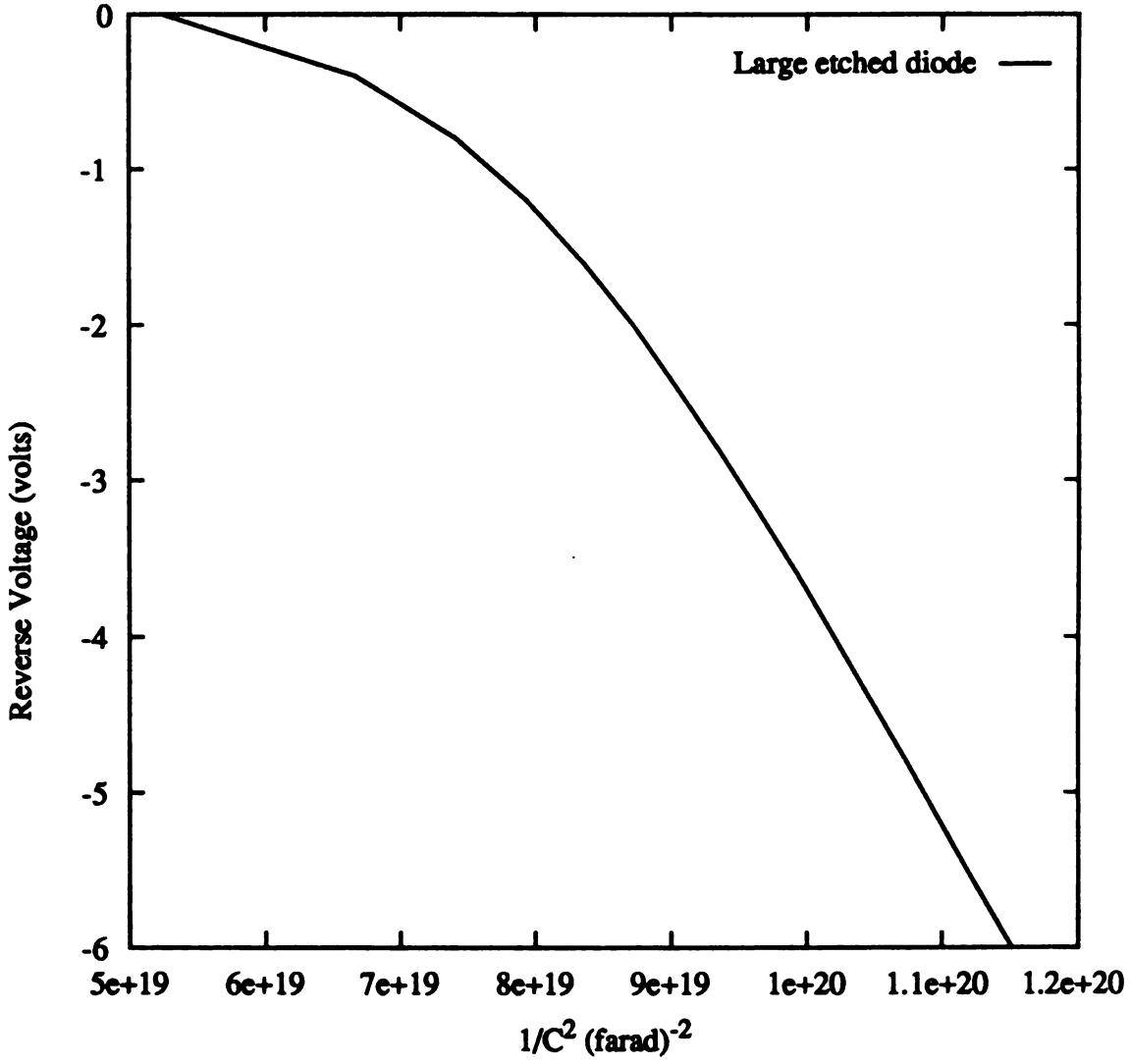


Figure 4.5 Plot of $1/C^2$ vs. V for the large etched diode

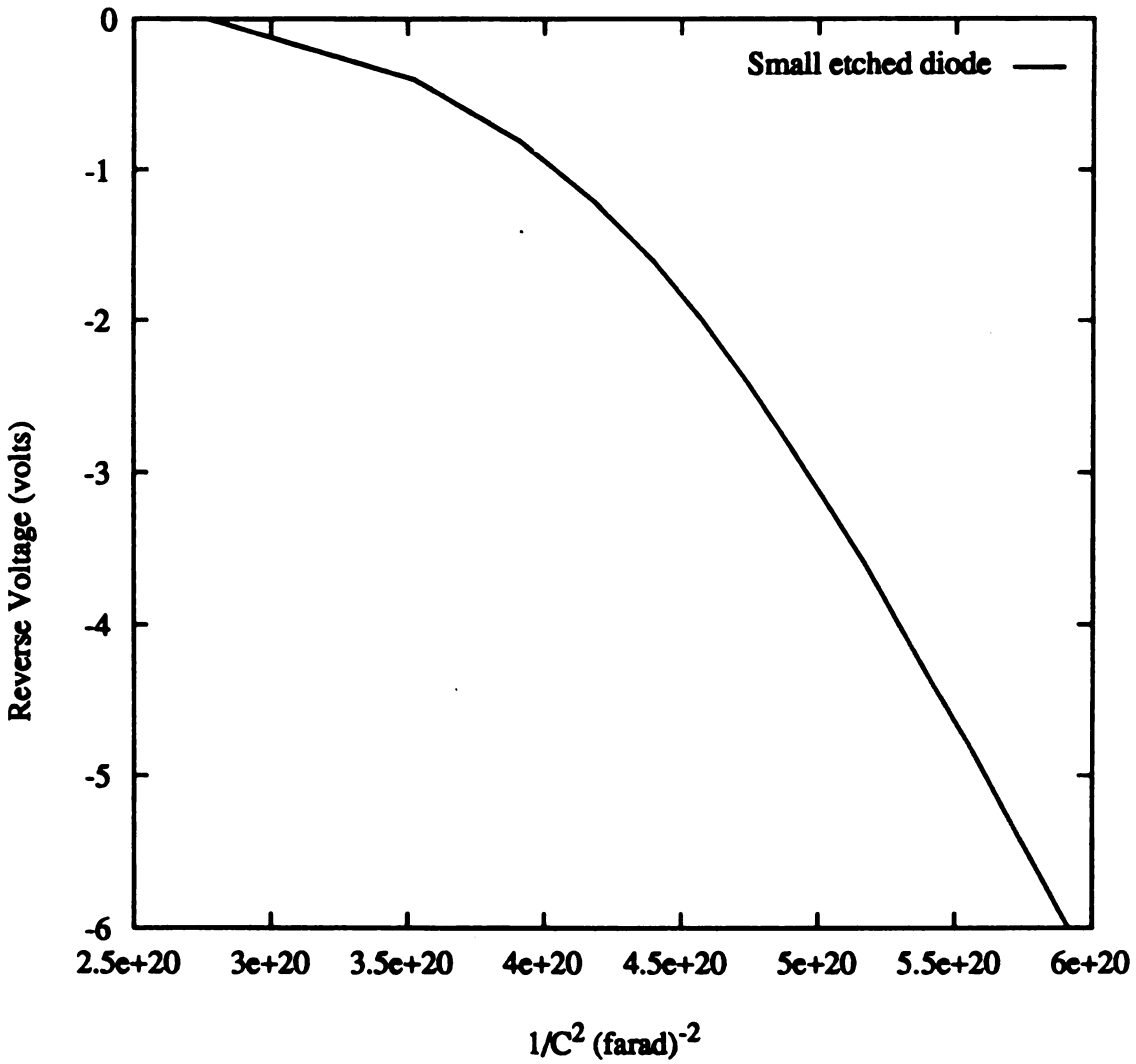


Figure 4.6 Plot of $1/C^2$ vs. V for the small etched diode

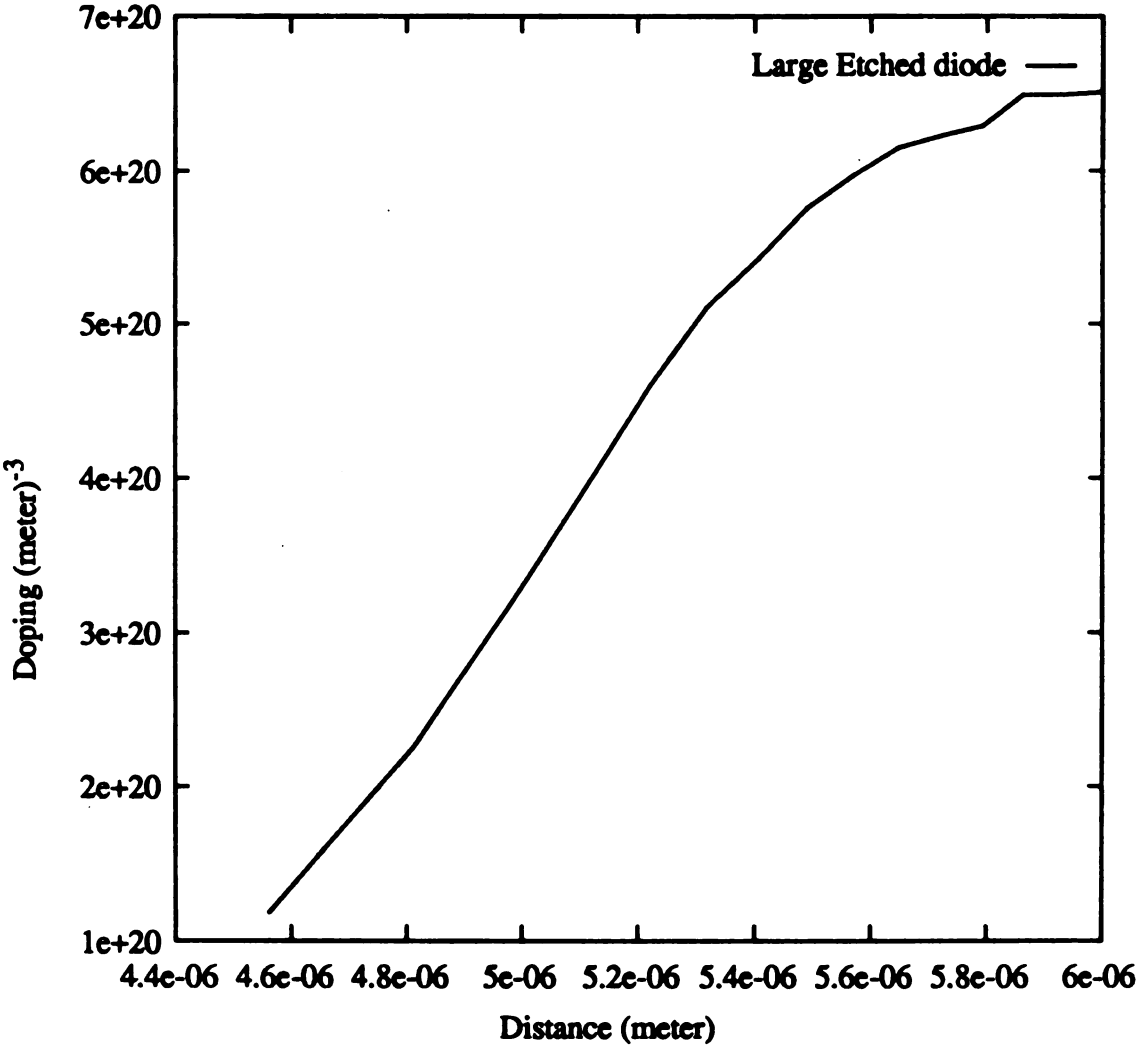


Figure 4.7 Variation of doping vs. distance in the large etched diode

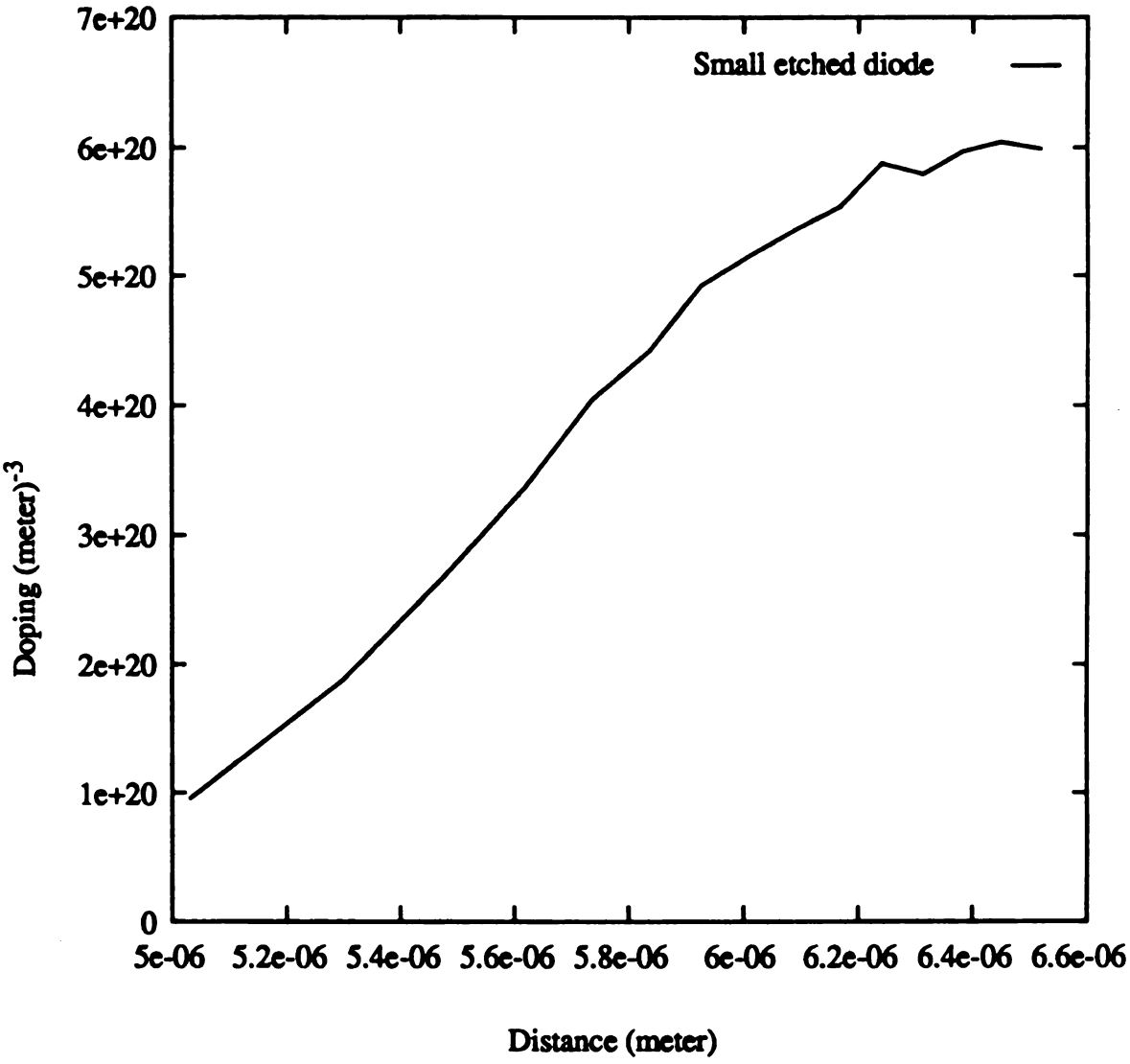


Figure 4.8 Variation of doping vs. distance in the small etched diode

4.8. It was noticed [7] that p-type, 10 Ω-cm <100> silicon samples subjected to plasma etching using a barrel type plasma system with 700 W of power at 500 mTorr for five minutes and to reactive ion etching (RIE) using a commercial parallel plate system at 1300 W of power at 20 mTorr for 5.2 minutes, exhibited dopant compensation effects up to a depth of nearly 6 μmeters. The RIE reactor used 75 sccm CHF_3/9 sccm O_2 while the plasma reactor used 60 sccm C_2F_6/60 sccm CHF_3. It was also noticed that effects on n-type silicon is less than those on p-type. The samples were seen to recover after ten minutes of annealing at 230 ^{0}C. Similar effects have been seen in the etching of GaAs and AlGaAs [4,15] where hydrogen appears as a component of the etching gases. ECR etching of GaAs [4] using CH_4/H_2/Ar as the etchant produced dopant deactivation in n-type GaAs up to a distance of 0.3 microns. However in the present case, hydrogen has not been intentionally introduced and the etching gas is a combination of SF_6 and argon. It should also be noted that in the etching conducted during this thesis, the bias voltage was much lower than that in the referenced material for silicon.

In terms of speculating on the possible role of hydrogen compensation in this case, the ECR plasma etch system used in this experiment uses an oil based diffusion pump to maintain low pressure. The oil used in the pump is separated from the plasma chamber by a series of baffles preventing a straight path from the oil pump to the chamber. However some molecules of oil will manage to reach the chamber and the plasma present there may break the oil into its constituents. But in this case the oil is not a hydrocarbon and hence contains no hydrogen to cause the effect seen. Another source of hydrogen could be from the conducting paint applied on the back of the SBD in order to form a proper contact. The conducting paint is made up of graphite dissolved in acetone. The wafer substrate holder was uncooled in this work, and although the temperature was not documented, it was observed to become quite hot. It may be possible that the heat caused the paint solvents to be driven from the film, contributing hydrogen. In that case, this could well be a major cause of the effect noticed.

Alternatively, fluorine is present in relatively large quantities as compared to hydrogen and has also been known to cause carrier reduction in highly n-type silicon. Stud-

ies have shown that ion implanted fluorine [16] causes carrier reduction in highly doped n-type silicon by bonding with arsenic or phosphorous as the case may be and thus reducing the amount of donors available. Since fluorine belongs to group VII of the periodic table it is still the most electronegative material in the setup. Using the same argument as in the case of fluorine and arsenic, it can be argued that since both boron and silicon are relatively electropositive with respect to fluorine, the carrier reduction may be due to either a fluorine - silicon bond or a fluorine - boron bond. Both these bonds are known to occur in nature [17] and have bonding strengths of 116 ± 12 and 180 ± 3 k cal/mole respectively. Since the fluorine - boron bond has higher bond strength this may be the one being formed.

In order to resolve this one has to test for the chemical composition of the wafer. It is in this context that XPS and Auger introduced earlier are used. The results of these experiments are discussed in Section 4.4.

4.3 I-V characteristics before and after etching

The I-V characteristics of the diodes can be used to get additional understanding of the interface and the ideality factor of the diodes. The current across a Schottky barrier diode is mainly controlled by the barrier height at the metal semiconductor interface. Changes in current can often be directly correlated to changes in barrier height. The theory of the I-V characteristics and the associated non-idealities is discussed in Section 2.5.3. Ideally with I on a log scale, the I-V plot is a straight line. The plots of the large etched and unetched diode are drawn on the same scale and shown in Figure 4.9. It can be immediately seen that the etched diode actually has a better I-V characteristic than the unetched one. The characteristics of the interface seems to improve after etching. The etched diode conducts less current at lower voltages than the unetched one indicating a higher barrier height. The value of I_0, as calculated from the intercept of the straight line portion of the I-V characteristic of the large etched diode with the current axis, is 4×10^{-8} amperes. The value of Φ_B can then be calculated using Eq. (12), Section 2.5.3 and is equal to 0.78 volts. The value of the

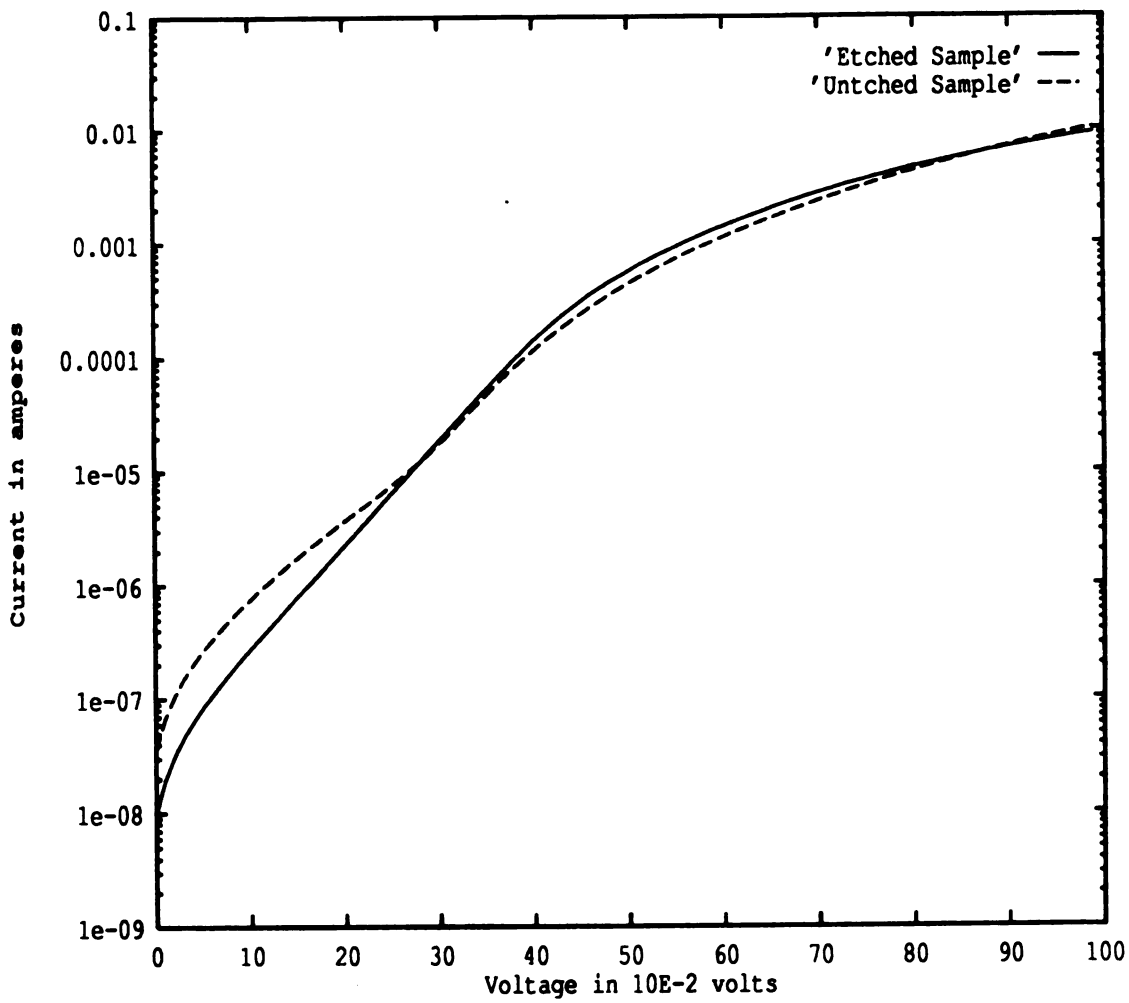


Figure 4.9 I-V plots of etched and unetched diodes

ideality factor, n, calculated using the slope of the same straight line is found to be 1.52. Similar calculations could not be conducted for the unetched diodes due to the absence of a straight line portion in their I-V characteristics. The etched and unetched samples are however very similar in all other regions. This means that the strong dopant deactivation effect noticed in the C-V plot does not seem to translate into a strong corresponding effect in the I-V plot. In order to investigate this further, a PISCES simulation of the I-V characteristics was run for a SBD with uniform background doping and on another diode with a non-uniform doping profile as calculated from the C-V plot for an etched structure. The results are shown in Figure 4.10. The PISCES plot of the two cases seems to justify the above experimental observation that a large C-V change does not necessarily correspond to a large I-V change. It is noted that since the doping as calculated from the C-V plot does not yield a complete doping vs. distance profile, i.e., the first estimate of the doping is available at 4.6 microns for the large diode, this profile had to be extrapolated to the surface. The PISCES input file is listed in Appendix C.

The PISCES plot indicates that at lower voltages, the non-uniformly doped diode conducts slightly more than the uniformly doped one but their characteristics are practically identical in all other regions. This is as expected since a lightly doped junction has a larger depletion region and hence a larger contribution to the total current because of generation - recombination contribution to current in that region. The experiment results however indicated that the unetched samples had a slightly higher current which is opposite to the simulation. In contrast to the C-V results, the I-V results of the unetched diodes show significant non-idealities. There may be due to surface phenomena which may have a large effect on the I-V characteristics but not on the C-V behavior, since the latter probe more deeply into the wafer.

Earlier experiments conducted by Hopwood [14] on the I-V characteristic of Schottky barrier diodes indicated that the ideality factors of the etched diodes were better than those of the unetched ones but that the etched diodes conducted higher currents at lower voltages as compared to the unetched ones due to reduced barrier heights. These experiments were conducted on diodes etched in a similar ECR plasma source but at much higher

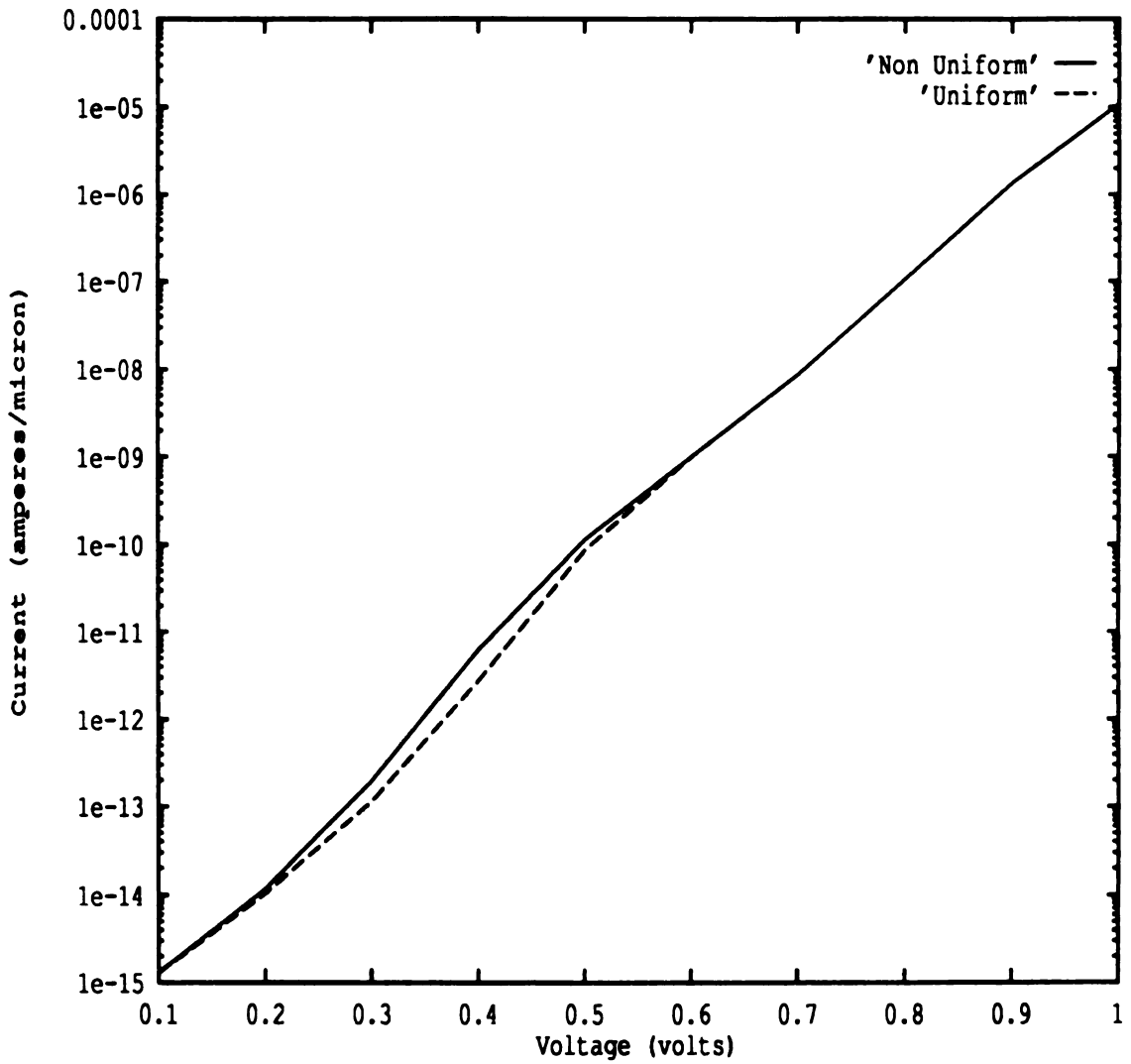


Figure 4.10 PISCES simulation plot of uniform and non-uniformly doped diodes

voltages (-30,-60 and -70 v). It is noted that at lower bias voltages plasma etching improved the ideality factor but did not effect the barrier heights. This observation should indicate that at higher bias voltages etching is deleterious to the surface leading to reduced barrier heights and hence higher currents.

The results of this study show that damage assessment with SBDs should include both C-V and I-V measurements since they yield complementary information. Specifically, the I-V measurements did not indicate, either by simulation or by experiment, the deep dopant compensation that was apparent from the C-V measurements. However they are more sensitive to surface phenomena. It is noted that the I-V calculated barrier height for etched diodes is less than the C-V calculated barrier height for unetched diodes. This direction of barrier height change is consistent with Hopwood's results.

4.4 XPS and AES measurement results

Multiple XPS measurements were done but with varying results. In the first study, XPS was done on one of the diodes fabricated on etched silicon. This experiment was conducted over a large range of binding energies (0 -1100 ev) in order to get a complete picture of all the impurities present on the surface. The initial measurement was done without any pre-measurement sputter of the surface. The XPS spectrum for the surface is given in Figure 4.11 and the composition of the surface in atomic percentage is given in Table 2. It can be seen that the single largest component on the surface is oxygen. This is from the native oxide formed on the surface of the exposed silicon and possibly on the exposed aluminum. The other major component of the surface is carbon and it is generally present in samples that are not analyzed in-situ. Another unwelcome constituent of the surface is sodium which is present in concentrations of nearly 1 atomic percent. The major source of this contamination could be from human handling. Peaks corresponding to aluminum were seen near 100 ev. These correspond to the aluminum on the surface contact of the diode. All the afore mentioned constituents can be reasonably explained except for the peaks correspond-

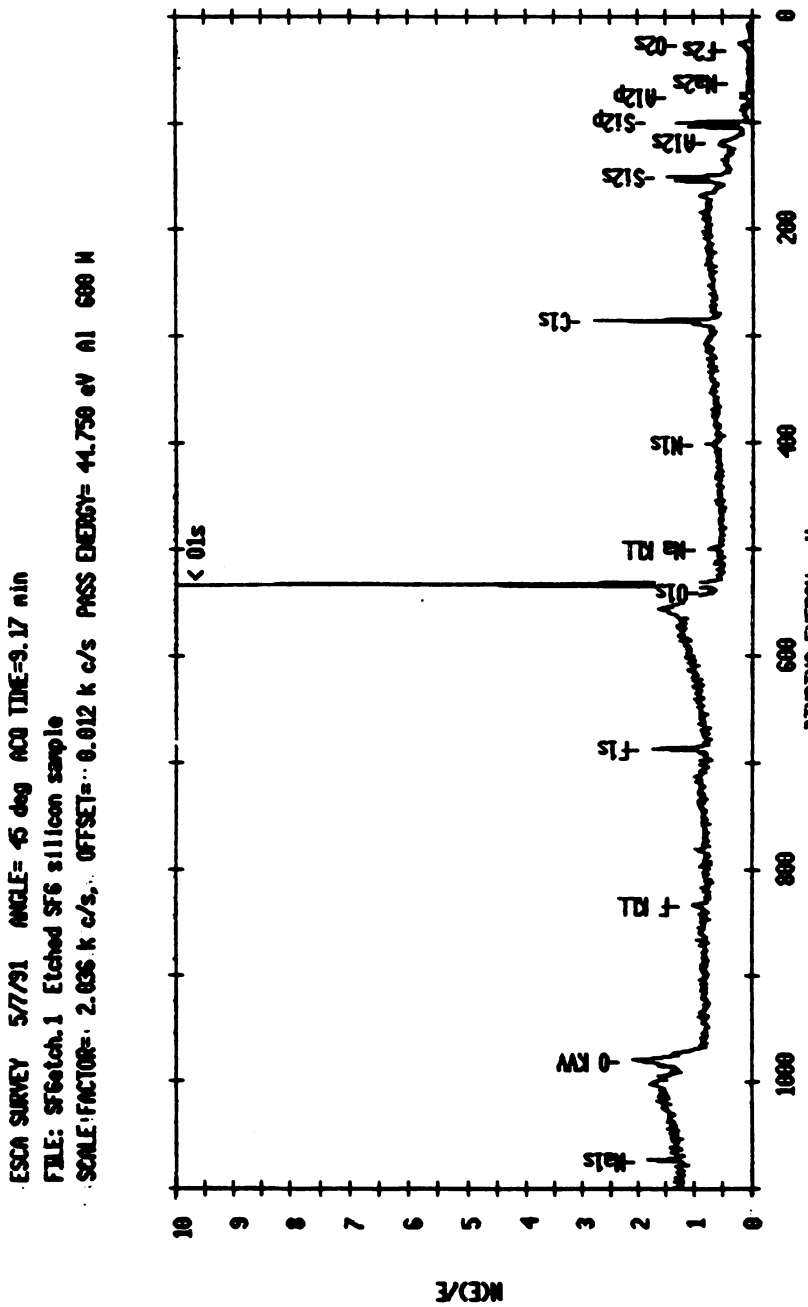


Figure 4.11 XPS plot of the surface of the etched semiconductor

Table 2 XPS results of Silicon surface

[redacted] New [redacted] Element Name [redacted]
Mode [redacted] Height [redacted] Baseline [redacted] Integrated
Regions C1 N1 O1 F1 Na1 Al2 [redacted]

[redacted]
[redacted] SF6etch.1 Etched SF6 silicon sample
[redacted] Small Area Omni-Focus [redacted] Monochromated

Element	Area (cts-eV/s)	Sensitivity Factor	Concentration (%)
C1s	7394	0.296	25.66
N1s	860	0.477	1.85
O1s	28431	0.711	41.08
F1s	3996	1.000	4.11
Na1s	1536	1.685	0.94
Al2s	1829	0.288	6.52
Si2p	5466	0.283	19.84

ing to fluorine. Fluorine peaks are seen near 700 ev and 10 ev and this corresponds to a surprisingly large amount of 4.11 atomic percent. The only logical source of fluorine could be the etching gas made up of SF_6. However no traces of sulfur was found on the surface. This could be because post - etch cleaning of the surface of the wafer may have washed away any sulfur deposited on it. It is also possible that the level of sulfur present is too low to be measured by XPS. Either of these is a valid reason because even though it is known that the wafer is nominally p-type, no boron peak was detected. Assuming the surface to be silicon containing 5×10^{22} atoms/cm^3 with a boron doping of 5×10^{14}/cm^3, leads a value of 10^{-6} atomic percent. This is well below the measurement limit of XPS.

The sample was then sputtered by argon ions in vacuum for one minute corresponding roughly to a depth of 50^0A. The XPS spectra is plotted in Figure 4.12 and the composition of the surface is given in Table 3. It was seen that the amount of carbon detected dropped from a value of more than 25% at the surface to a value of 5.15% after sputtering. It was however seen that the amount of oxygen had increased in percentage. It is known that the "native" oxide formed on the surface has a maximum thickness of 15-20 ^{0}A. Therefore the oxygen detected after a one minute sputter could not be from SiO_2. It could however have been from the Al_2O_3 formed on the surface of the aluminum contact since the X-ray spot size seemed to include the some part of the contact. A previously unseen element which showed up this time is copper. The source of this is the copper wafer holder used to fasten the sample in place. The sputtering process seems to have sputtered some copper off the wafer holder. Sodium concentration remains more or less unchanged whereas the concentration of fluorine actually seems to increase. The quantity of silicon shows some increase. This is logical since we are progressing into the surface of the silicon wafer. It seems, based on these results, that fluorine has diffused into the wafer and is present in large quantities.

In order to further examine the extent of fluorine diffusion, sputtering was continued for a further two minutes. The XPS spectra and the corresponding element concentrations are given in Figure 4.13 and Table 4 respectively. The major component was still oxygen.The percentage of silicon present had nearly doubled and fluorine was still present

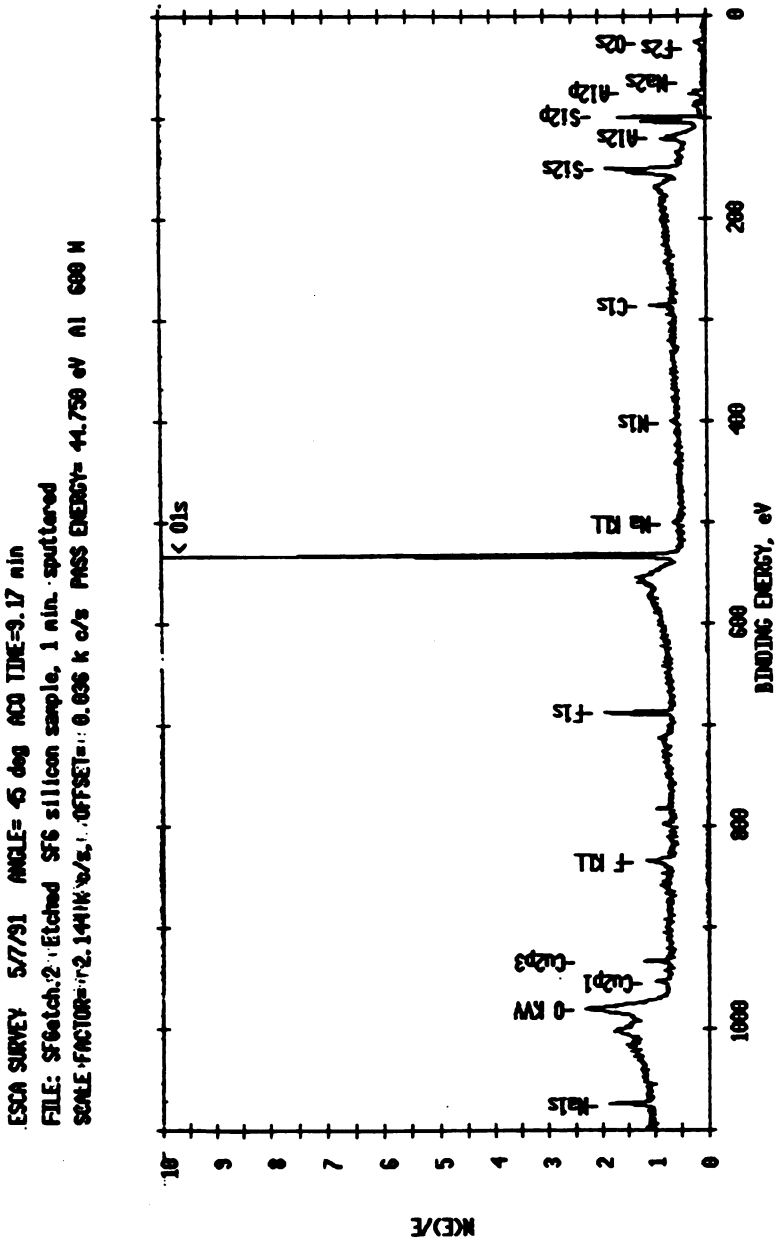


Figure 4.12 XPS plot of the surface after 1 minute of sputtering

Table 3 XPS results after 1 minute sputter

[redacted] New [redacted] Element Name [redacted]
[redacted] Mode [redacted] Height [redacted] Baseline [redacted] Integrated
[redacted] Regions C1 N1 O1 F1 Na1 Al2 [redacted]

[redacted] SF6etch.2 Etched SF6 silicon sample, 1 min. sputtered
[redacted] Small Area Omni-Focus [redacted] Monochromated

Element	Area (cts-eV/s)	Sensitivity Factor	Concentration (%)
C1s	1398	0.296	5.15
N1s	420	0.477	0.96
O1s	30229	0.711	46.37
F1s	5325	1.000	5.81
Na1s	2652	1.685	1.72
Al2s	2934	0.288	11.11
Si2p	7492	0.283	28.88

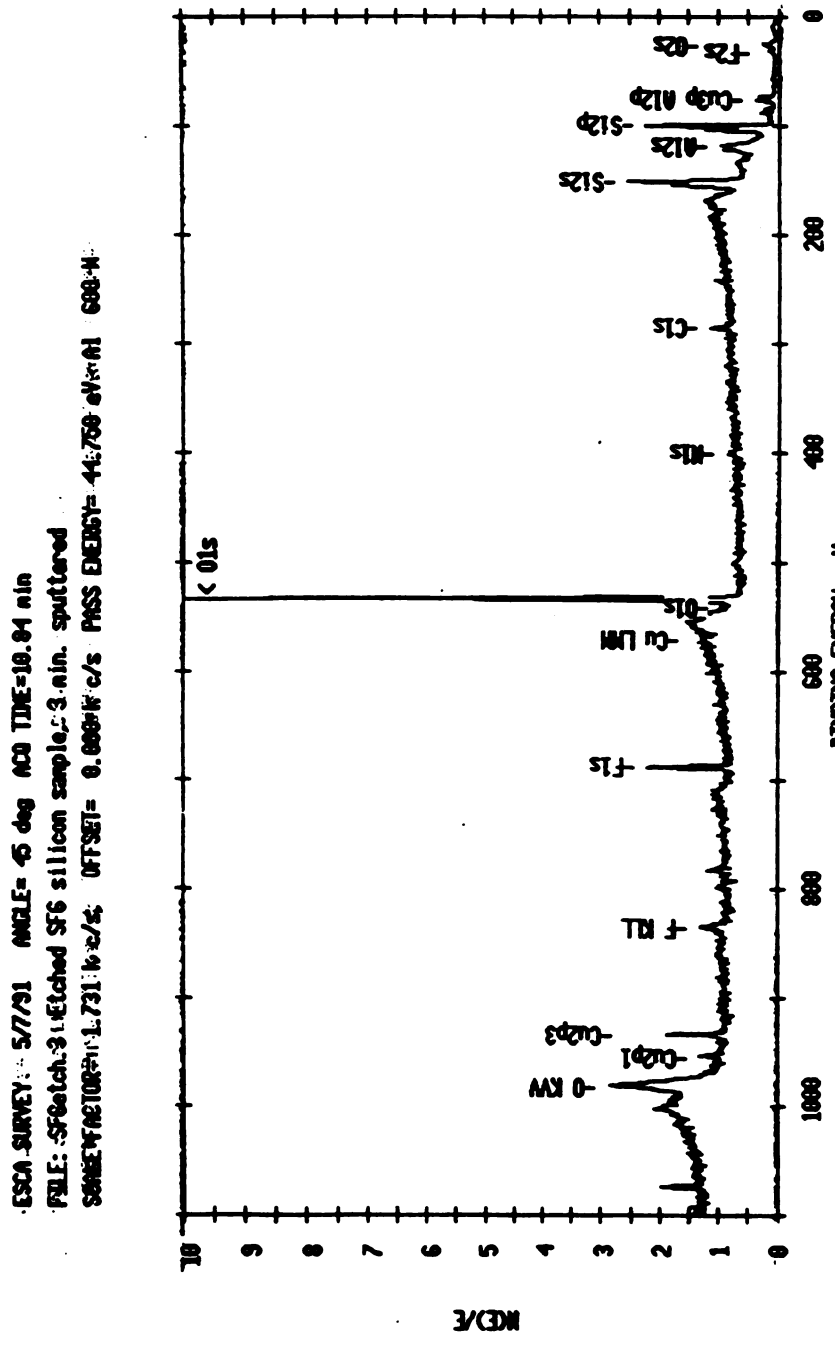


Figure 4.13 XPS plot of the surface after 3 minutes of sputtering

Table 4 XPS results after 3 minute sputter

[redacted] New

Mode [redacted] Height [redacted] Baseline [redacted] Integrated

Regions C1 N1 O1 F1 Na1 Al2 [redacted]

[redacted] Element Name [redacted]

[redacted]

[redacted] SF6etch.3. Etched SF6 silicon sample, 3 min. sputtered

Small Area Omni-Focus [redacted] Monochromated

Element	Area (cts-eV/s)	Sensitivity Factor	Concentration (%)
C1s	933	0.296	3.07
N1s	307	0.477	0.63
O1s	30959	0.711	42.35
F1s	6005	1.000	5.84
Na1s	2147	1.685	1.24
Al2s	3997	0.288	13.50
Si2p	9712	0.283	33.38

in large quantities. Since sputtering away 6 microns at the rate of 50 ^{0}A per minute would take a long time, Auger spectroscopy of the wafer's edge was used to obtain a depth profiling of impurities in silicon. The Auger results are described later in this section. These experiments were conducted at the Composites Center, Michigan State University and will be collectively referred to as Experiment A.

In order to verify the above results another set of XPS scans was conducted using the Chemistry department's XPS equipment and this will be referred to as Experiment B. Since this equipment required samples of relatively larger size, three quarters of a wafer which was etched simultaneously with the quarter upon which SBDs were fabricated was selected for this experiment. However this sample did not have SBD's formed upon it and had not been subjected to any form of post etch cleaning. XPS results of the surface showed measurable amounts of fluorine in addition to large amounts of carbon, oxygen and silicon. However, the amount was fluorine detected here was less than that detected by Experiment A. This could be due to the relative position of the different quarters in the etching cavity. Since the sputter gun associated with this equipments was not designed for depth profiling, sputtering had to be conducted for a very long time in order to obtain some idea of the concentration profile. It is noted that measurable quantities of fluorine was still present after 24 hours of sputtering with helium ions.

A attempt was then made to obtain a depth profile of the various elements present in the Experiment A sample using Auger Electron Spectroscopy. The sample was mounted on its edge and a "line scan" i.e., a small spot size Auger scan of the sample perpendicular to the surface and parallel to the edge, was performed on it. Initial results seemed to indicate the presence of fluorine in large quantities with a depth profile as shown in Figure 4.14. However further tests on the same sample did not yield similar results. One speculation offered by the Experiment A XPS operator was that the electron beam used in this technique could have heated the sample resulting in fluorine (molecular or non-bonded) escaping out. It is noted that the C-V characteristics of these diodes measured after the Auger process were essentially identical to the pre-Auger characteristics. This could mean that either fluorine is not the cause of dopant compensation, or that fluorine could not escape

from underneath the aluminum dot contact and hence the diode behavior is unchanged, or that the fluorine that escaped was not the same as fluorine causing compensation, or that the AES effected volume is a negligible part of the total sample. It should however be kept in mind that even though the element is undetectable by AES, it could still be present in concentrations enough to cause a change in electrical characteristics. Further research should be conducted in this area. It is further noted that subsequent XPS scans, using the same equipment as Experiment A, on the same samples failed to detect any fluorine. Further more AES scans conducted on the samples subjected to Experiment B did not detect any fluorine.

Earlier experiments conducted by Hopwood [14] used Auger spectroscopy to obtain the surface composition of etched silicon. Scans done on an unsputtered surface showed 0.5% fluorine as well as silicon, oxygen, carbon and sulfur. The fluorine was no longer present after a 3 minute argon ion sputter. It was concluded in that case that fluorine was present only on the surface and had been removed by the sputtering. Clearly XPS and Auger analysis of fluorine is a matter requiring further study.

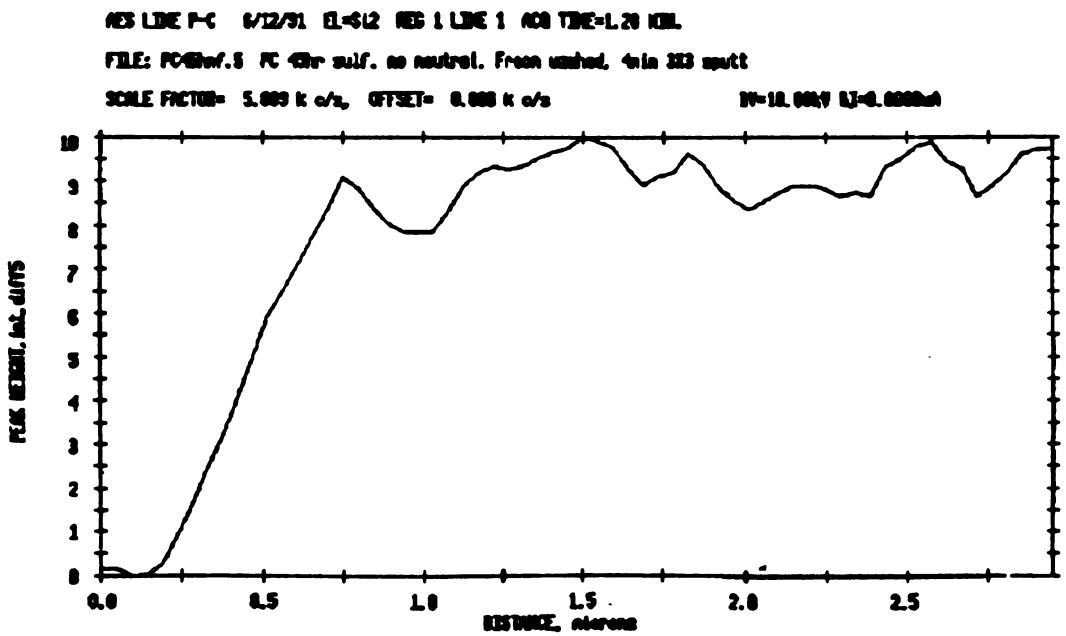


Figure 4.14 Auger "line scan" of sample

4.5 DLTS measurement results

DLTS scans were done at five different t_1 values as described in Section 3.4. Figure 4.15 and Figure 4.16 show typical C-t plots at different temperatures for unetched and etched diodes respectively. The plot of $(C(t_2)-C(t_1))/C_\infty$ was plotted for each of the two cases and is shown in Figures 4.17 and 4.18. It is seen that the maximum value of this ratio in the case of the unetched diode is about -0.0005, approximately 0.05%. This could be due to noise or due to the LSB fluctuation error present in digital instruments. The same calculation in the case of the etched diode yields a maximum value of 0.03 or 3%. It should be noted in Figure 4.16 that the absolute value of the capacitance has decreased and so a similar change in capacitance in the case of the etched diode will lead to larger value of the ratio due to a smaller value of C_∞.

Consequently etching produced a measurable change in transient capacitance characteristics. The detectable trap density in terms of background concentration and differential capacitance is given by Eq. (3), Section 2.4 and has been reproduced below for convenience.

$$N = 2(\Delta C/C)(N_B)$$

The 3% change in $\Delta C/C$ for the etched sample would correspond to an N value of approximately 3×10^{13} /cm^3. From the post etch data, the various values of e, t_{max} and t_1/t_2 corresponding to the plots in Figure 4.18 are calculated and tabulated in Table 5. It can be seen that in spite of the change in the DLTS signal between the etched and unetched diodes, the tabulated values do not provide insight about trap energy levels when evaluated by standard DLTS analysis. Ideally a plot of ln e vs. 1000/T is a straight line, the slope of which gives the activation energy. In this case the values do not form a straight line. The DLTS experiments conducted on the samples failed to yield any results leading to quantitative information about trap energies. These could be due to the following reasons:

(1) The transient capacitance change is not due to deep states, but rather due to some other phenomenon which overwhelms the number of deep states. The minimum detectable change in capacitance for the experimental setup was 0.02 pf and the background doping

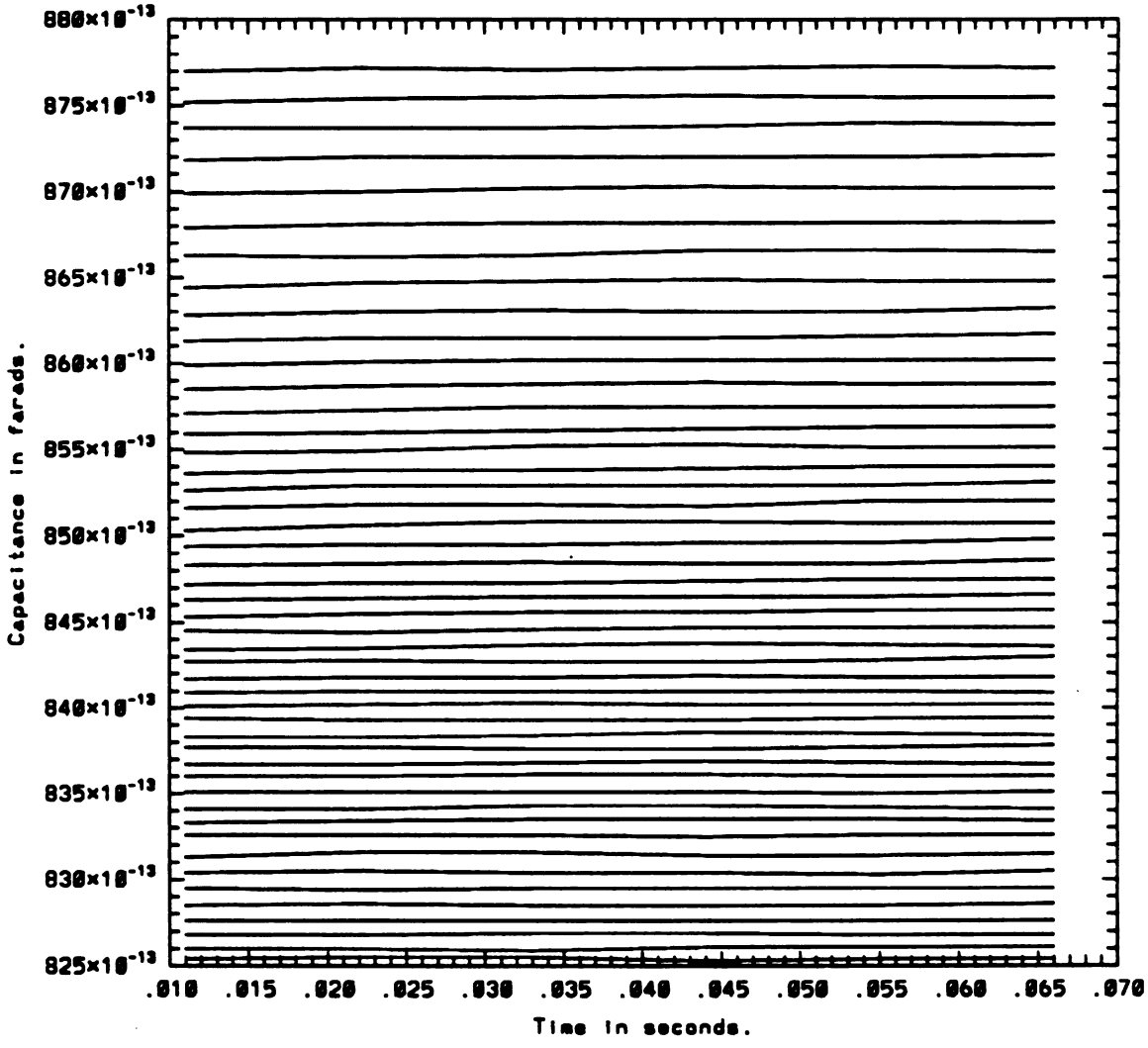


Figure 4.15 Capacitance transients of an unetched diode between 47 ^{0}K and 285 ^{0}K

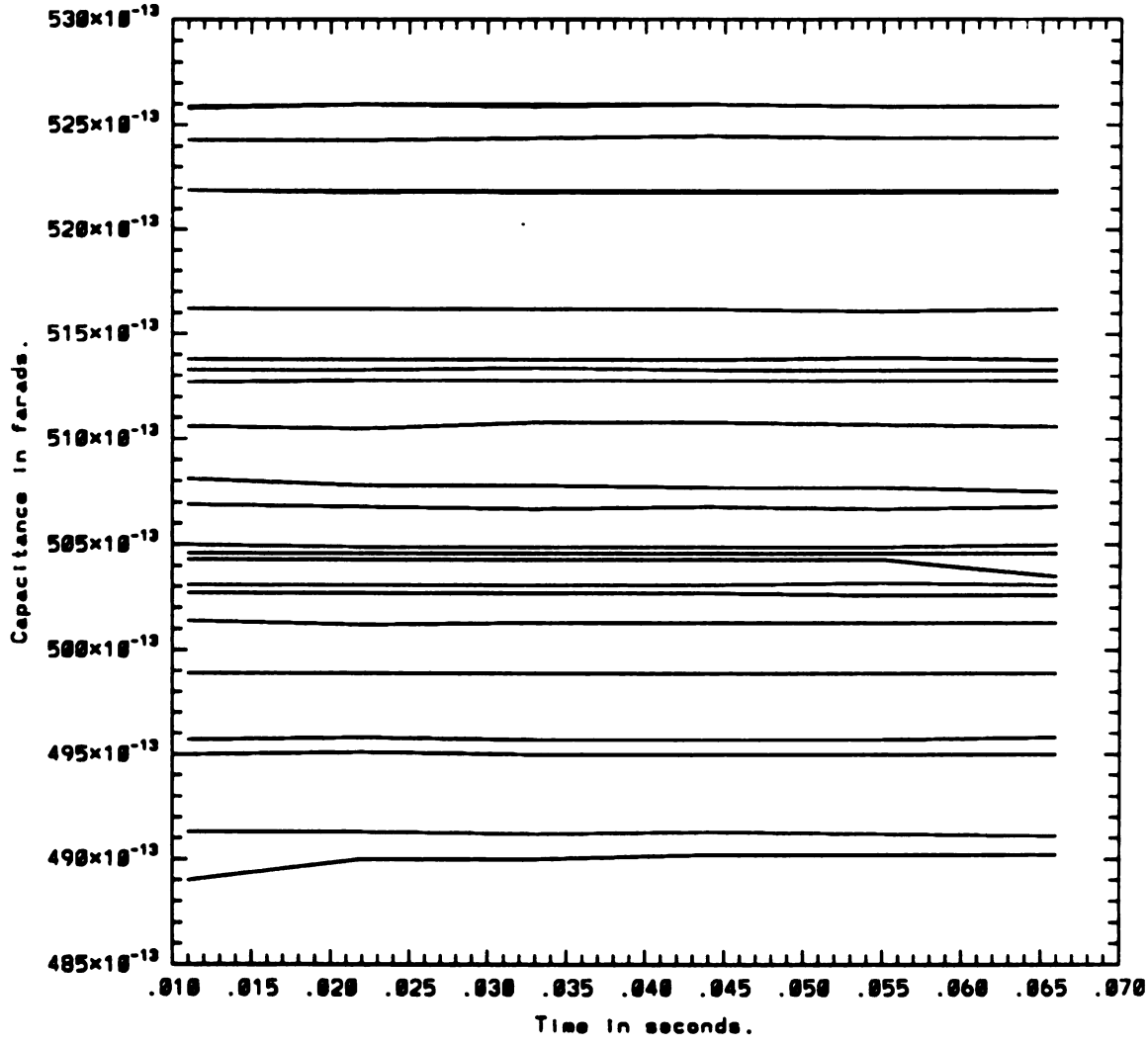


Figure 4.16 Capacitance transients of an etched diode between 43 ^{0}K and 175 ^{0}K

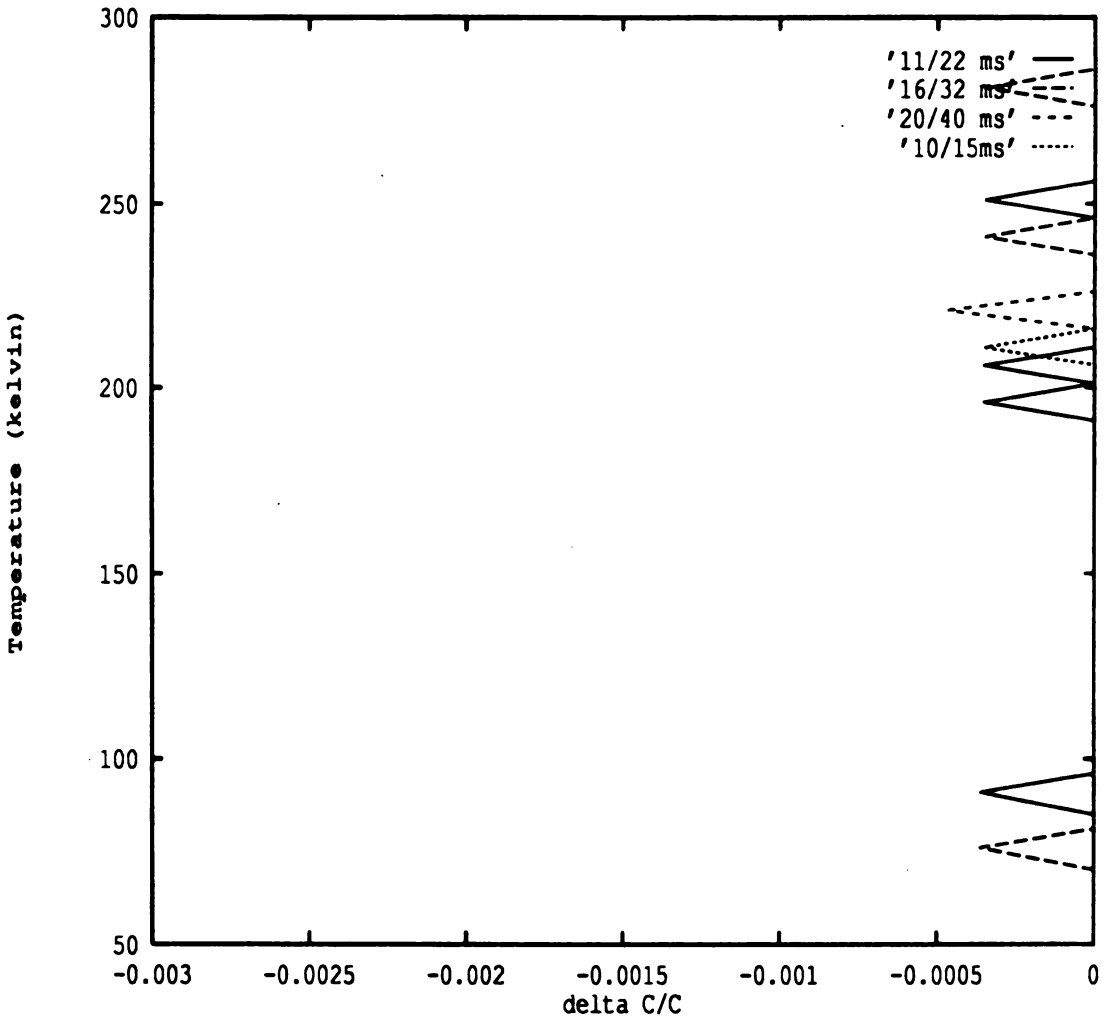


Figure 4.17 DLTS plots for various t_1/t_2 conducted on unetched diodes

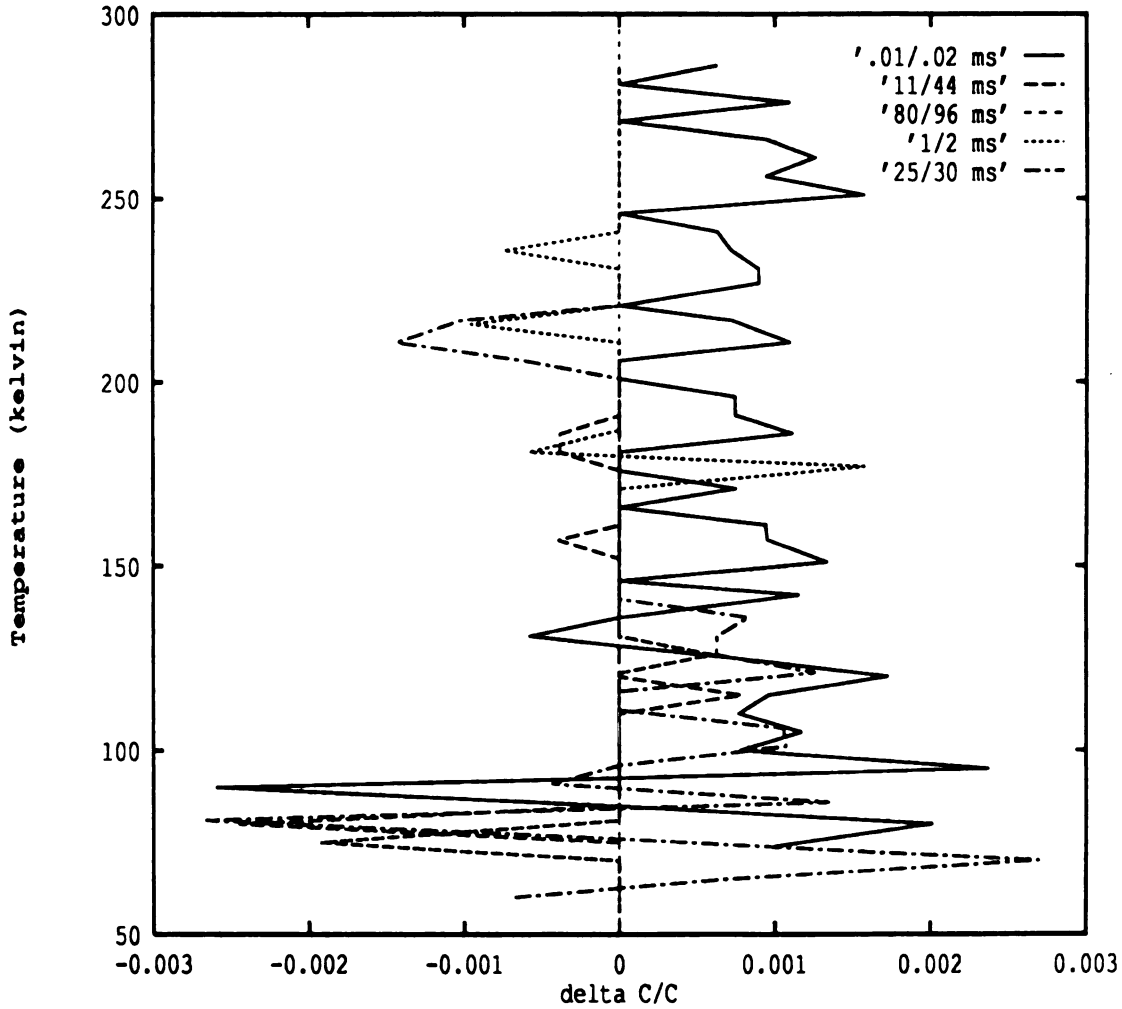


Figure 4.18 DLTS plots for various t_1/t_2 conducted on etched diodes

Table 5. DLTS experimental results.

t_1 / t_2	$\Delta C / C_\infty$	τ_{max} (ms)	e (ms^{-1})	1000 / T (K^{-1})
0.01/0.02	- 0.0026	0.01443	69.314	11.11
11/44	- 0.0025	23.8	0.04	12.5
80/96	- 0.0020	87.75	0.0114	13.33
1/2	- 0.0018	1.443	0.69	14.2857
25/30	- 0.0027	13.712	0.073	12.5

was approximately 5×10^{14} /cm^3. The quiescent reverse bias capacitance of the large etched diode is nearly 100 pf at -6v bias. This leads to a value of 4×10^{10} states/cm^3 as the lowest detectable trap density. Earlier work done by Indusekhar et al. [18] on Nickel introduced deep states in p-type silicon, indicated a lowest reported value of 10^{11} states/cm^3. In that case large quantities of Ni were intentionally added to silicon to examine and profile the electrically active deep states.

(2) DLTS conducted on Schottky barrier diodes is inherently incapable of detecting minority carrier traps. In the present case, since the diode was p-type, n-type traps were not detectable. It is conceivable that plasma etching may be introducing deep states in the upper half of the band gap. These would need to be detected by fabricating SBDs on n-type silicon and subjecting them to the same steps.

(3) The states are not characterizable by a single activation energy, but are spread over a significant energy range within the gap.

In summary, this DLTS study did not produce any quantifiable information on activation energies of deep state production on silicon due to plasma etching. DLTS, however is more useful in profiling deep traps in iii-v and ii-vi semiconductors which inherently have a higher density of traps.Future studies on ECR etching of iii-v materials may find the DLTS method to be of value as a complementary tool for studying etch damage.

Chapter 5

Conclusions

5.1 Introduction

This chapter summarizes the major results of this study and outlines directions for future research.

5.2 Summary of Major Results

This study applied several different methods to evaluate and quantify the effects of plasma etching on silicon. A method often reported for this purpose in the literature is the measurement of I-V characteristics of Schottky barrier diodes. This study shows that the I-V characteristics are a poor measure of one possible etching effect, namely dopant compensation. For this effect, a preferred method is an evaluation of C-V characteristics. The results of this research indicate an appreciable compensation effect, up to several μmeters depth, that is readily observable both experimentally and via simulation in C-V evaluations but not in I-V evaluations. It is recommended that etching evaluation via Schottky diodes include both I-V and C-V measurement since they provide complementary information. The I-V characteristics are particularly sensitive to surface phenomena which effect the barrier height. The C-V characteristics reflect the effect of damage at depths within the semiconductor. For this work, with relatively low (20 V) substrate biases, the I-V characteristics of the etched and unetched diodes did not vary appreciably.

Transient capacitance variations were observed on etched surfaces, but not on unetched surfaces, which indicates that etching did cause production of a small (on the order of 10^{13}) number of states which can be filled and emptied by varying the applied

diode bias. However results were not interpretable in terms of standard DLTS analysis of single activation states.

The XPS and Auger analysis indicates the presence of fluorine both on the surface of the etched samples, and at depths of up to 150 ^{0}A. However it was not possible within the scope of this study to unambiguously confirm the presence of fluorine at several μmeter depths indicated for dopant compensation. It is possible that fluorine is responsible for this effect. Alternatively, hydrogen introduced inadvertently by the sample mounting procedure may also be playing a role.

The results indicate clear differences between etched and unetched samples. The various methods produced complementary results. For this study, the electrical method which provided the most information about etching effects was the C-V methods on Schottky diodes.

5.3 Directions for future research

This thesis did not attempt to find the effect of post-processing steps, e.g. annealing, on the characteristics of the etched device. Further research could be done in this area. Studies done in similar cases have shown that the device characteristics return back to normal after a thermal anneal. A comparison of C-V characteristics of the device after annealing with those before and after etching will be sufficient.

A major point of contention is the cause of carrier reduction. Even though fluorine has been known to cause carrier reduction in certain cases, the experiments conducted so far do not conclusively prove that this is the sole cause. Even though fluorine has been detected in large quantities, the presence of hydrogen in the acetone used in the conductive paint makes this evidence inconclusive.

Two major approaches to resolve this issue can be suggested. The first one would

be to conduct the etching step without conducting paint by using an RF bias rather than DC. Extra care should be taken to ensure that no source of hydrogen is inadvertently introduced into the chamber. Also substrate temperature should be varied to investigate the diffusion of the element causing compensation. A second alternative would be to conduct other chemical spectroscopy methods like SIMS which are sensitive to minute quantities of hydrogen on the etched samples to resolve this issue.

DLTS measurements conducted on the p-type SBDs did not yield any quantitative results on trap energy levels due to the possible causes listed in Section 4.5. However it is necessary that the same approach be used on n-type diodes to determine whether any electron deep traps were introduced as a result of plasma etching. Finally, the XPS and Auger results, while interesting, were quite preliminary. The correlation of defect effects with their chemical and physical origins will benefit greatly by a more concerted surface science study.

APPENDICES

Appendix A

Instrumentation required

Displex closed-cycle refrigeration system: This is a closed cycle cryogenic refrigeration system employing helium as a working medium. The system is capable of refrigeration between room temperature (300 ^{0}K) and 10 ^{0}K. The system consists of a compressor module with electrical controls, flexible interconnecting gas lines and an expander module. As the system is water cooled, it is imperative that running water be used all the time the system is in use. Failure to do so will cause the compressor to trip due to overheating.

Vacuum pump: The pump is used to start and maintain a working vacuum for the cryogenic unit to operate efficiently. The cryogenic unit requires pressure below at least 5 mTorr. Note that incorrect vacuum can damage the cryogenic unit.

HP 4280A 1 MHz capacitance meter: This is designed for C-V and C-t measurements of semiconductor devices. The meter is equipped with an internal pulse generator for pulse bias measurement.The HPIB address of this instrument was set to 2.

HP 3457A multimeter: The HPIB address of this instrument was set to 22. It was used to measure the DC voltage across the calibrated SI 400 diode.

HP 6634A DC power supply: The HPIB address of this instrument was set to 5. The overload current protection of this device was enabled so as to prevent run away heating in the software loop.

HP 1915A variable transient time output: This is a pulse shaper and output amplifier housed in the HP 1900A pulse generator mainframe. This instrument was terminated in a 50 ohm feed-through resistance for two reasons. The first was to ensure that the circuitry "saw" the impedance of the pulse source as 50 ohms. The second was to convert the current output of the HP 1915A to a voltage pulse of 6 V pp upon being triggered.

Note: Some pulse generators have non zero outputs even when disabled. These should either be calibrated to zero or as was done in this case, using the offset capability of the instrument.

Tektronix 577 curve tracer: The curve tracer was used in the "DC" mode to supply a 100 μampere biasing current to the SI 400 diode. Even though the curve tracer maintains the current output quite correctly, the output should be frequently checked and manually readjusted.

HP 6218C bias source: This DC power supply was used to supply the 6 V reverse bias across the device under test. The current demand on this power source is minimal since very little current flows through a reverse biased diode.

Pirani vacuum gauge: The vacuum gauge is used to measure the vacuum inside the cryogenic unit. The compressor of the cryogenic unit is started up when the instrument reads below 5 mTorr.

IBM PC with 640 K RAM, 5.1 Microsoft C compiler, HPIB command library version 1.1 and a HPIB interface control board. To repeat the experiment the source code listed in appendix B will have to be compiled using Microsoft c compiler version 5.1 and linked with the HPIB command library version 1.1 or higher.

Note: Read through the source code for details of the programming of the HP 4280A, HP 3457A and HP 6634A.

Procedure:

1) Start up the vacuum pump and wait until the vacuum gauge reads at least 5 mTorr.

2) Start cooling water for the cryogenic unit and then start up the compressor.

3) Use the curve tracer in DC mode to supply 100 μamperes of current to the SI 400 diode and measure the voltage across the diode using the voltmeter. The voltage readout at room temperature is approximately 1.5 volts.

4) Allow cryogenic unit to cool the sample down to a value below the lowest desired temperature.

5) On the PC change to the directory where the data files need to be stored. Ensure that the file "calib.dat" containing the SI 400 diode calibration details and the file containing the required measurement details are present.

7) Start up the program on the PC.

8) The program will automatically take all the readings desired. Upon exiting from the pro-

gram reset all instruments to their power on state.

Note: If the readings are to be taken such that the first value has to be measured below 10 ms then an external pulse generator will be required. This will entail some changes in the software as detailed in the source code. Please refer to the HP 4280A programming part of the software for further details.

Device mounting: The device was fabricated such the whole back of the wafer was metallized. This was done to ensure good ohmic contact on the mount. The front of the device was metallized through a mask leading to SBD of two different diameters. Refer to device fabrication for further details. This section details the actual mounting of the device inside the cryogenic unit and solutions to the problems which arose thereof.

The device holder was fabricated out of copper and one contact of the holder was the bottom metal and the other, a spring controlled blunt pin. The spring led to the device being firmly held in the mount thus ensuring proper contact. Since the bottom of the device holder is metal, care has to be taken to prevent the chuck from coming in electrical contact with the device holder and yet have the device in thermal contact with the cold chuck tip. An electrical contact leads to undesirable stray capacitances being present in the circuit. Lack of thermal contact will lead to different temperatures of the sample and cold tip. This problem can be resolved by mounting the device holder on some plaster of paris stuck on to the top of the chuck in a circular fashion. The empty space between the bottom of the device holder and the cold surface of the chuck was filled with "cryocon" conductive grease thus ensuring the two above requirements. Though the readings are taken with the samples "floating", it is best to connect the body of the cryogenic unit to the ground of HP 4280A.

Appendix B

Source code

```
/* This is the source code of the software used to take DLTS measurements*/
#include <stdio.h>
#include <ctype.h>
#include <c_hpib.h>
#include <stdlib.h>

short error;
long isc = 7;   /* address of the HPIB board on the PC */
long C4280a = 702; /* address of the C meter on the HPIB bus */
long C3457a = 722; /* address of the Multimeter on the HPIB bus */
long C6634a = 705; /* address of the Power supply on the HPIB bus */
FILE *inputfile;
FILE *outputfile;
char buf[1024];
char dumm [20];
int temp [50];
int iteration;
double I_am;                    /* Present reading of the voltmeter */
double I_wannabe; /* Volt equivalent of the desired reading */
int n_ofr;
float volts [400]; /* Internal buffer containing SI 400 calibration */
int limit , nofr;

#define                 SRQLINE                 1
#define TRUE 1
#define FALSE 0

/*****************************************************************/
void reverse (s)
char s[];
{
        int c,i,j;

        for (i = 0, j = strlen(s) - 1; i < j; i++, j--) {
        c = s[i];
        s[i] = s[j];
        s[j] = c;
        }
}
/*****************************************************************/

void mitoa(n, s)
```

```
int n;
char s[];
{
        int i, sign;

        if (( sign = n) < 0 )
                n = -n;
        i = 0;
        do {
                s[i++] = n % 10 + '0' ;
        } while (( n /= 10 ) > 0 );

        if ( sign < 0 )
                s[i++] = '-';
        s[i] = '\0';
        reverse (s);
}
/*****************************************************************/
read_temp (tempfile)

char tempfile[20];
/* reads the file containing the temperatures at which measurements are needed*/

{
int i;
 inputfile = fopen (tempfile,"r");

 fscanf (inputfile,"%d\n",&nofr);
        for ( i = 0 ; i< nofr ; i++ )
 fscanf (inputfile,"%d\n",&temp[i]);

 fclose(inputfile);

}

/*****************************************************************/
initialize ()

/* set all the instruments on the bus to thier default values */
{
 error = ioreset (isc);
 error_handler (error, "IORESET");
 error = iotimeout (isc, 5.0);
 error_handler (error, "IOTIMEOUT");
 error = ioclear (isc);
 error_handler (error, "IOCLEAR");
```

```
error = ioclear (C4280a);
error_handler (error, "IOCLEAR");
error = ioclear (C3457a);
error_handler (error, "IOCLEAR");
error = ioclear (C6634a);
error_handler (error, "IOCLEAR");
}
/*****************************************************************/
HP4280a_setup (tm)
int tm;

{
char                    *codes;

/* Program the HP 4280 to the proper connection mode etc
 Un comment the lines below if connection mode 11 is needed */

 if (tm ==0)
/* codes = "CN11,LE2,CE1,MS1,CH1,CS"; */
 codes = "CN14,LE2,CE1,MS1,CH1,CS";

 if (tm ==1)
/* codes = "TR3,BC,FN5,IB2,PU+6.0,VO1,RA1,BL1,PN6,PH20E-3,PT20E-
3,MD1,SW1";*/
 codes = "TR3,BC,FN5,IB0,PC+0.0,VO1,RA1,BL1,PN6,PH20E-3,PT05E-3,MD1,SW1";

 error = iooutputs (C4280a, codes, strlen(codes));
 error_handler (error, "IOOUTPUTS");

}

/*****************************************************************/
wait_for_srq ()
/* wait for SRQ from the device before taking readings */

{
 int                    response;

 do
 {
 do
 {
 error = iostatus (isc, SRQLINE, &response);
 error_handler (error, "IOSTATUS");
 }
 while (response == 0);
```

```
error = iospoll (C4280a, &response);
error_handler (error, "IOSPOLL");
}
while ((response & 1) != 1);
printf("response is %d \n",response);
}

/*********************************************************************/
/* program the HP 4280 A to output the buffered readings */
readout (iter)

int iter;

{
char                    *codes;
char *info;
char *bsinfo;
int                     numvalues;
int i;
char outname[20];

mitoa (iter,outname);
outputfile = fopen (outname,"w");
printf("filename is %s ptr is%s\n",outname,outputfile);

volt_read ();
fprintf (outputfile,"%s",dumm);

error = ioeoi (isc, 1);
error_handler (error, "IOEOI");

codes = "BS?";
error = iooutputs (C4280a, codes, strlen(codes));
error_handler (error, "IOOUTPUTS");
numvalues = 1500;
error = ioenters (C4280a, bsinfo, &numvalues);
error_handler (error, "IOENTERS");

codes = "MF?";
error = iooutputs (C4280a, codes, strlen(codes));
error_handler (error, "IOOUTPUTS");
numvalues = 1500;
error = ioenters (C4280a, bsinfo, &numvalues);
error_handler (error, "IOENTERS");

codes = "BD";
```

```
error = iooutputs (C4280a, codes, strlen(codes));
error_handler (error, "IOOUTPUTS");



fprintf (outputfile,"%d\n",iteration);
delay(30);

for ( i = 1; i < ( iteration + 1 ); i++)
{
numvalues = 1500;
error = ioenters (C4280a, info, &numvalues);
error_handler (error, "IOENTERS");
fprintf (outputfile,"%s\n", info);
printf ("%s\n", info);
}

fclose(outputfile);

}

/*********************************************************************/

double search ( itemp )
int itemp;
{
return ( volts [ itemp - 1 ] );
}

*********************************************************************/

error_handler (error, routine)
/* report any HPIB programming errors */

int                     error;
char                    *routine;

{
char                    *estring;
char                    ch;

if (error != NOERR)
{
printf ("Error in call to %s \n", routine);
printf (" Error = %d : %s \n", error, errstr(error));
printf ("Press <RETURN> to continue: ");
```

```
scanf ("%c", &ch);
 }
}

/*****************************************************************/

read_calibdata ()

/* read the file containing SI 400 calibration data */

{
int i;

 inputfile = fopen ("calib.dat","r");

 fscanf (inputfile,"%d\n",&n_ofr);
 for ( i = 0 ; i < n_ofr ; i++ )
 {
 fscanf (inputfile,"%f\n",&volts [i]);
 }
 fclose(inputfile);

}

/*****************************************************************/

delay(i)
int i;
{
int j,k,l;
 for ( j = 0 ; j < i ; j ++)
 {
 k=l;
 l=k;
 printf (".\r");
 }

}

/*****************************************************************/
/* maintains a loop continuosly monitors the voltmeter reading and changes
 the power source output to match the requirement that "I_wannabe- I_am"
 be equal to 4 mv (approx 2 centrigrade) */

maintain (itr)
int itr;
```

```
{
int count;
double diff;

 count = 0;
 I_wannabe = search (temp[itr]) ;
 volt_read ();
 I_am = atof (dumm);

 printf (" I AM %f I WANT %f ", I_am , I_wannabe);
 if ( (I_am - I_wannabe) > 0.4) limit = limit + 1500;
 if ( (I_am - I_wannabe) > 0.7) limit = limit + 4000;
 set_volt();
 delay (3000);

 volt_read();
 I_am = atof (dumm);

 do {
 printf (" I AM %f I WANT %f count %d ", I_am , I_wannabe,count);

 diff = I_am - I_wannabe ;
 if (diff < 0.0 ) diff = I_wannabe - I_am;

 printf (" %f ", diff );
 set_volt();
 volt_read();
 I_am = atof (dumm);

 if ( diff < 0.004 ) count++ ;

 } while (count < 5 ) ;


}

/*****************************************************************/
set_volt ()
/* continuosly vary the voltage across the heater unit depending upon the status */
{
char code [20];
char tmp [50];
char *codes;

 if (limit > 0 )
 {
```

```
sprintf (code ,"%s" , "VSET ");

if ( I_am > I_wannabe ) limit = limit + 50;

if ( I_am < I_wannabe ) limit = limit - 75;

mitoa (limit , tmp);
strcat (code , tmp );
strcat (code , "E-3" );
printf ("%s ", code);

error = iooutputs (C6634a, code, strlen(code));
error_handler (error, "IOOUTPUTS");
delay(3000);

}

}

/*********************************************************************/
power_setup()
/* program the powe supply for a maximum current ouput and set the overload protection*/
{
char *codes;

codes = "ISET .6 ; OCP 1" ;
error = iooutputs (C6634a, codes, strlen(codes));
error_handler (error, "IOOUTPUTS");
}

/*********************************************************************/
close_up ()
{

error = ioclear (isc);
error_handler (error, "IOCLEAR");
error = ioclear (C4280a);
error_handler (error, "IOCLEAR");
error = ioclear (C3457a);
error_handler (error, "IOCLEAR");
error = ioclear (C6634a);
error_handler (error, "IOCLEAR");
}

/*********************************************************************/
```

```
volt_read()
/* called by the subroutines to read the DC voltage of the SI 400 calibrated diode */

{
 char info [20];
 char                    *codes;

 codes = "PRESET";

 error = iooutputs (C3457a, codes, strlen(codes));
 error_handler (error, "IOOUTPUTS");

 delay(20);

 codes = "CSB;TRIG SYN;DCV";

 error = iooutputs (C3457a, codes, strlen(codes));
 error_handler (error, "IOOUTPUTS");

 delay(80);

error = ioenters (C3457a, info, 1);
 error_handler (error, "IOENTERS");
 if ( info[0] != 45 ) info[0] = 43 ;

 sprintf(dumm,"%s",info);

}


/*****************************************************************/
/* This the main program, it in invoked in the form "source filename". The program will be
in a loop for the number of readings required as mentioned in the firet line of filename. The
software rests all instruments to their power on state upon exiting
*/

main (argc,argv)
int argc;
char *argv[];

{
int iter;
char                    ch;

 initialize ();
 read_temp(argv[1]);
```

```
power_setup();
read_calibdata();

limit = 5500;
iteration = 6;

for ( iter = 0 ; iter < nofr ; iter++ )
{
HP4280a_setup (0);
maintain (iter);
delay(30);
HP4280a_setup (1);
printf("HP4280A SETUP COMPLETE \n");
wait_for_srq ();
delay(20);
readout (iter);
printf("exiting loop %d \n",iter);
}
close_up();

}

/*****************************************************************/
```

```
Title Schottky barrier
$ The wafer is non - uniformly doped with input being result of experiment
option tek
mesh rect nx=4 ny= 60 outf = sbd.mesh
x.m n=1 l=0 r=1
x.m n=4 l=0.1 r=1
y.m n=1 l=0 r=1
y.m n=60 l=10 r=1
region num=1 ix.l=1 ix.h=4 iy.l=1 iy.h=50 silicon
region num=2 ix.l=1 ix.h=4 iy.l=50 iy.h=60 silicon
elec num=1 ix.l=1 ix.h=4 iy.l=1 iy.h=1
elec num=2 ix.l=1 ix.h=4 iy.l=60 iy.h=60
doping reg=1 ascii inf=dope.dat
doping reg=2 p.type conc=1e19 uniform
contac num=1 alum
symb newton carr=2
method rhsnorm xnorm autonr
models temp=300 srh auger conmob fldmob print
solve init outf=pn2a0-r.slv
log outf=IV-r.log
solve vstep=-0.1 nsteps=10 elect=1
plot.1d inf=IV-r.log x.ax=v1 y.ax=i2 points min=0 outf=nunif.tr
end
```

BIBLIOGRAPHY

Bibliography

1) Manos and Flamm, "Plasma etching, An introduction," (Academic press, San Diego, CA, 1989).

2) Wavemat inc., "Microwave Plasma Disk Reactor 325 Instruction Manual," 1990.

3) J. Asmussen, J. Vac. Sci. Technol., A 7, 883, (1989).

4) C. Constantine, D. Johnson, S. J. Pearton, U. K. Chakrabarti, A.B. Emerson, W. S. Hobson and A. P. Kinsella, "Plasma etching of III - V semiconductors in $CH_4/H_2/Ar$ electron cyclotron resonance discharges," J. Vac. Sci. Technol., B 8 (4), pp 596-605, Jul/ Aug 1990.

5) T. Matsura et al., "Directional etching of Si with perfect selectivity to SiO_2 using ultra clean electron cyclotron resonance plasma," Appl. Phys. Lett. 56 (14), Apr 1990.

6) T. Saitoh, T. Yokogawa and T. Narusawa, "Reactive ion beam etching of ZnSe and ZnS epitaxial films using Cl_2 electron cyclotron resonance plasma," Appl. Phys. Lett. 56 (9), Feb 1990.

7) J. M. Heddleson, M. W. Horn, S. J. Fonash and D. C. Nguyen, "Effect of dry etching on the properties of Silicon," J. Vac. Sci. Technol., B 6 (1), pp 280-283, Jan/Feb 1988.

8) D. V. Lang, "Deep Level Transient Spectroscopy: A new method to characterize traps in semiconductors," J. Appl. Phys., Vol. 45, No. 7, pp 3023-3032, July 1974.

9) D. V. Lang, "Fast capacitance transient apparatus: Application to ZnO and O centers in GaP p-n junctions," J. Appl. Phys., Vol 45, No 7, 3014, July 1974.

10) L. Sharma, "Metal-Semiconductor Schottky Barrier Junctions and Their Applications," (Plenum press, NY,1984).

11) Edward B. Hakim, "Microelectronic Reliability," (Vol. 1, Artech house, MA, 1988).

12) D. K. Reinhard, "Introduction to Integrated circuit fabrication," (Houghton Mifflin, NY, 1987).

13) Brian Musson, "An investigation of Anisotropic etching of silicon in an Electron Cyclotron Resonance Plasma", Master's thesis, Michigan State University (1991).

14) J. A. Hopwood, "Macroscopic properties of a multipolar electron cyclotron resonance microwave - cavity plasma source for anisotropic silicon etching," Dissertation for Ph. D.,

Michigan State University (1990).

15) R. Cheung, S. Thomas, I. McIntyre, C. D. W. Wilkinson and S. P. Beaumont, "Passivation of donors in electron beam lithography defined nanostructures after methane/hydrogen reactive ion etching," J. Vac. Sci. Technol., B, Vol. 6, No. 6, pp 1911-1915, Nov/ Dec 1988.

16) Juri Kato, "The effect of Fluorine atoms in high dose Arsenic or Phosphorous ion implanted Silicon," J Electrochem. Soc., Vol. 137, No. 6, pp 1918-1924, June 1990.

17) Weast, "Handbook of Chemistry and Physics," (56^{th} edition, 1975-76, CRC press).

18) H. Induskhar and Vikram Kumar, "Electrical properties of nickel-related deep levels in silicon," J. appl. Phys. 61 (4), pp 1449-1455, Feb 1987.

19) Karl Hess, "Advanced theory of semiconductor devices," (Prentice Hall, NJ, 1988).

20) A. G. Milnes and D. L. Feucht, "Heterojunctions and Metal Semiconductor Junctions," (Academic press, NY, 1972).

21) Jian H. Zhao, "Effect of Carrier Confinement by InGaAs/ GaAs Heterointerface Barrier on Deep Trap Concentration Profiling," IEEE Transactions on Electron devices, Vol. 37., No. 10, pp 2158-2164, October 1990.

22) S. M. Sze, "Physics of Semiconductor Devices," (2nd edition, John Wiley and Sons, NY, 1981).

23) U. S. Kim, C. H. Wolowodiuk, and R. J. Jaccodine, "The effect of Fluorine additions to the oxidation of silicon," J. Electrochem. Soc Vol. 137, No. 6, pp 2291-2296, July 1990.

24) Le Xu, D. K. Reinhard and M. G. Thompson, "RF sputtered Gold-Amorphous Silicon Schottky barrier diodes," IEEE Transactions on Electron Devices, Vol. ED-29, No. 6, pp 1004-1008, June 1982.

25) J. S. Wang, S. J. Fonash and S. Ashok, "Passivation of Dry-Etching Damage Using Low-Energy Hydrogen Implants," IEEE Electron Device letters, Vol. Edl-4, No. 12, pp 432-435, Dec 1983.

26) Jian H. Zhao, Jyh-Chwen Lee, Z. Q. Fang, T. E. Schlesinger and A. G. Milnes, "Theoretical and experimental determination of deep trap profiles in semiconductors", J. Appl. Phys., 61(3), pp 1063-1067, Feb 1987.