This is to certify that the

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AN UPGRADED INTERFACE FOR

AN ICP-DIRECT READING SPECTROMETER

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AN UPGRADED INTERFACE FOR AN ICP-DIRECT READING SPECTROMETER

By

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Abstract

The computer interface for a Jarrell Ash AtomComp 750 direct reading spectrometer has been upgraded. The original interface involved integration of the photocurrent followed by an analog to digital conversion of the resulting voltage. This system was controlled by a DEC PDP8/M minicomputer. The upgraded interface involves amplification of the photocurrent using a current to voltage converter and conversion of this voltage to a frequency. The frequency is then counted by a counter/timer board mounted in an IBM PC/AT clone. Four channels of data can be collected simultaneously by the upgraded system. Results obtained with the new instrument are presented.

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Chapter 1

INTRODUCTION

1.1 Development of the ICP

The introduction of the inductively coupled plasma (ICP) as an excitation source for spectrochemical analysis revolutionized optical emission spectroscopy. Following the description of an ICP by Reed[1,2] in 1961, two independent groups of spectroscopists began research in the area. Their objective was to modify the ICP such that it would be suitable for optical emission spectroscopy (OES). Greenfield[3] *et al* in 1964 and Fassel and Wendt[4] in 1965 published results obtained with the first ICP-OES systems. Although their instruments were quite different and neither was optimized, their results were competitive with those obtained using the more established flame methods. In a critical paper, Fassel *et al*[5] describe an ICP-OES system incorporating impedance matching of the plasma and power supply. They found that this improved detection limits over those previously obtained with ICPs and over those obtained using flame atomic emission (AES) or flame atomic absorption (AAS). This particular work gave credence to predictions that the ICP would become a primary source for atomic emission spectroscopy.

Up until this time, the most widely used methods for spectroscopic analysis of solutions were flame AES and AAS. In their favour, flame AES and AAS are instrumentally relatively simple techniques which can be implemented at low cost. The flame, however, has several inherent disadvantages with respect to its use as an excitation source for AES. Flames typically display high background levels, poor sensitivity, narrow linear dynamic range and high susceptibility to chemical and spectral interferences. Flame AES in particular has a limited number of elements

to which it may be applied because the flame does not provide enough thermal energy to excite many elements. Flame AAS compensates for some of these disadvantages since an external excitation source is used, but a hollow cathode lamp for the element of interest must be available.

The ICP suffers to a much lesser extent from these inherent disadvantages and is nearer to an ideal atomization and excitation source. Table 1 lists some of the ICP's characteristics[6]. The higher temperature of the plasma alleviates many of the disadvantages typical of flames. The plasma's higher temperatures and near inert environment make it relatively free of chemical interferences resulting from the formation of molecular species or refractory compounds. A higher temperature also increases the number of elements that can be successfully determined using ICP-OES and improves detection limits since more of the analyte is atomized.

Table I: Characteristics of the Inductively Coupled Plasma

1. High temperature
2. Long residence times
3. High electron number densities
4. Free atoms formed in nearly inert environment
5. Molecular species absent or present at very low levels
6. Optically thin
7. No electrodes
8. No explosive gases

Low background emission in the analytical observation zone and the optical thinness of the plasma give it a wide linear dynamic range. Freedom from many chemical interferences and its ability to excite most samples make the ICP well suited to simultaneous multielement analysis (SMEA). SMEA would be feasible for flame AES if more elements could be excited at flame temperatures, but it is not

feasible for flame AAS in part because of geometric restrictions and the loss of sensitivity accompanying the use of multielement hollow cathode lamps. In an overall comparison of analytical figures of merit, the plasma is certainly superior to flames for atomic spectroscopy.

The ICP also offers some advantages over other plasma sources. As discussed in an extensive review by Greenfield *et al*[7,8,9], the ICP, in the majority of cases, gives better detection limits and has higher sensitivity than both dc plasma jets and microwave plasma torches. For many analytes, the limit of detection is some two to three orders of magnitude lower with the ICP than with other plasma sources examined. To a lesser extent, the ICP also gives higher precision than the other plasma sources. Boumans[10,11] evaluated the ICP, high temperature flames, current free and current carrying DC plasmas and microwave plasmas for their applicability to simultaneous multielement analysis. Boumans concluded, based on his criteria, that the ICP gave the best analytical performance of the excitation sources examined.

1.2 History of ICP Measurement Systems

When the first ICP-OES systems were developed, they were generally applied to single element or sequential multielement analyses. The typical detection system consisted of a monochromator, spectrometer or spectrograph, phototransducer, amplifier and readout device. Certainly one of the more popular early systems incorporates a scanning monochromator and a photomultiplier tube (PMT). This provides the high resolution spectral information obtainable from monochromators with the high sensitivity of a PMT. A block diagram of such a system is given in Fig. 1. One disadvantage is that the time required for acquisition of a single spectrum is often on the order of tens of minutes.

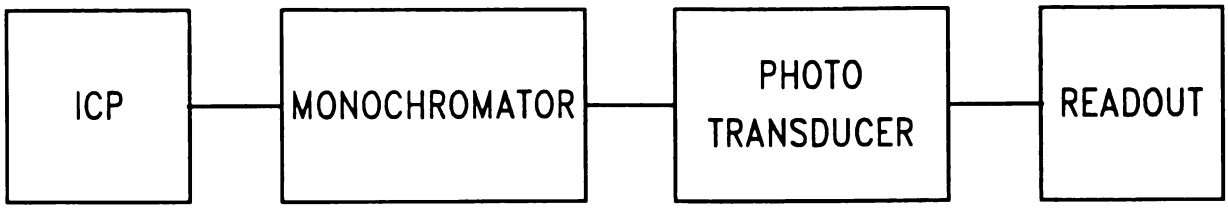


Figure 1: Block diagram of a typical ICP emission system.

The approach described above was taken by Barnett *et al*[12] for ICP-AAS, Scott *et al*[13,14,15] and Kirkbright *et al*[16,17,18] for ICP-OES analysis of real samples including rock, soil and plants. Boumans *et al*[19,20,21] describe an interesting dual channel-dual monochromator system. A commercial ICP-OES system based on an instrument developed by Boumans and de Boer employs a 1.5 m concave grating spectrometer and a roving slit assembly that enables measurement of any spectral line within the wavelength range of the instrument. As indicated above, a large number of early detection systems for ICPs have involved a scanning monochromator and single photomultiplier tube. This approach has the advantage of providing spectral information and flexibility of line choice, but, because it involves some means of scanning, it is also time intensive and consumes much sample.

It was quickly recognised that ICP-OES was fundamentally well suited to simultaneous multielement analysis. An initial study by Boumans and de Boer[22] revealed that conditions for SMEA favoring few interferences were the same conditions that gave relatively good detection limits for most analytes. By the mid 1970s many researchers were taking advantage of this capability of the ICP by using polychromators or spectrometers with multiple fixed exit slits and detectors. An optical diagram of a polychromator is shown in Fig. 2. These systems in most cases could accommodate more than twenty channels. Greenfield *et al*[23], since the early 1970s, have used a thirty channel polychromator. Watson *et al*[24] used a 3.4 m Ebert spectrograph and 24 channel spectrometer. The popularity of multichannel systems extended to instrument manufacturers and by the late 1970s several companies offered ICP detectors capable of determining as many as 64 elements simultaneously. Among these is the 50 channel Jarrell Ash AtomComp 750. In contrast to monochromator based systems, the polychromator or direct reading

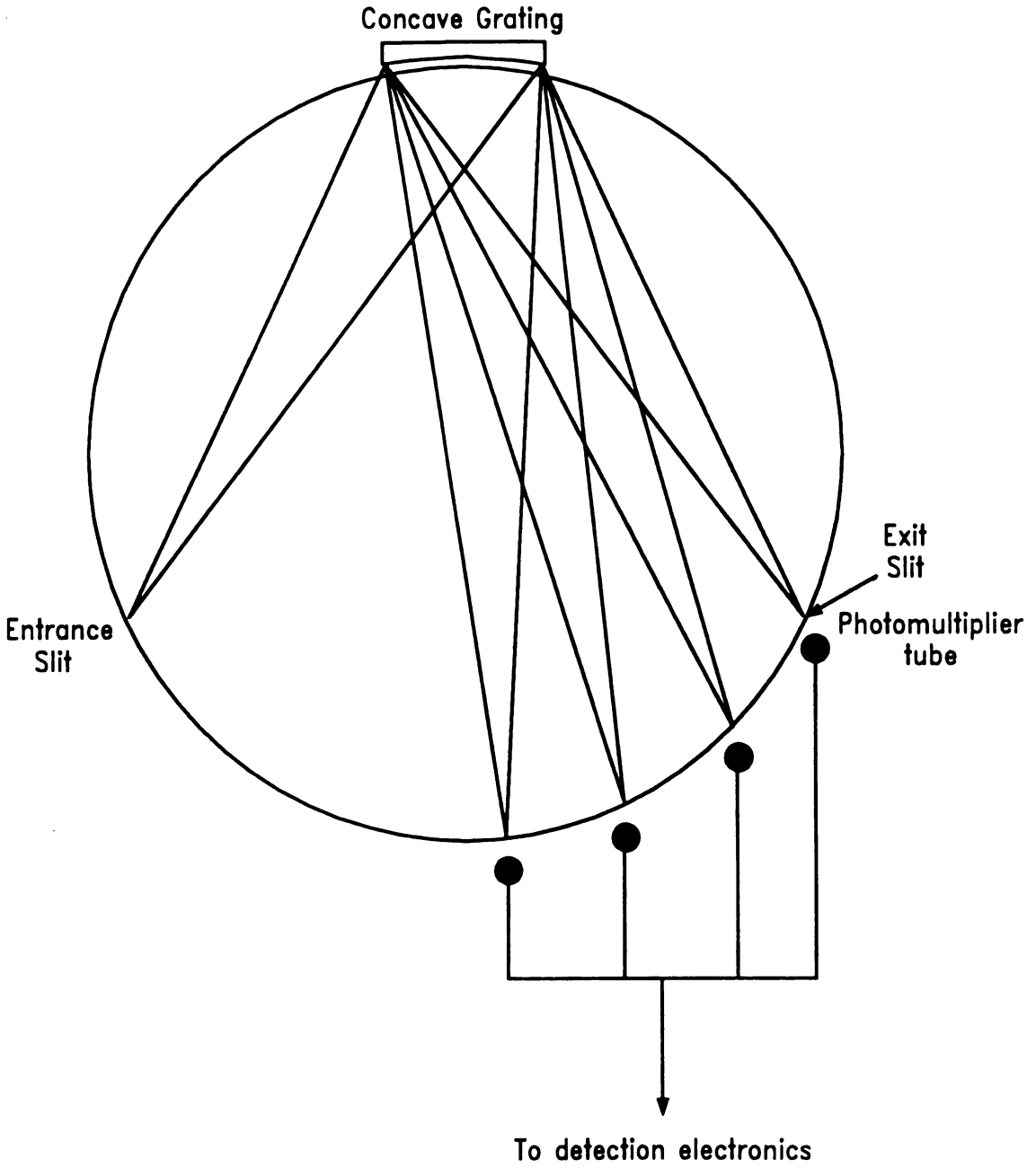


Figure 2: Optical configuration of a Paschen–Runge type direct reading Spectrometer.

instrument gives only intensity information at a fixed set of wavelengths within a specified range. This range, however, is typically greater than 300 nm. Furthermore, polychromator systems take less time than monochromator systems for analysis of a fixed number of analytes (greater than one) and, hence, generally consume less sample.

A compromise between the two detection systems discussed above is the photodiode array (PDA). A number of researchers have chosen this detector in the recent past for a variety of applications of the ICP[25,26,27]. The PDA in conjunction with a mono- or polychromator can provide spectral information in a very small amount of time. The disadvantages associated with the PDA may, however, make it inappropriate for some applications. The wavelength range available at one time is reduced relative to the polychromator/fixed detector system. Furthermore, the PDA is less sensitive than a PMT. The problem of sensitivity has been somewhat alleviated by the development of intensified diode arrays, but the restricted wavelength range remains an inconvenience if the ICP system is to be used for SMEA.

In the very recent past, the ICP has been introduced to a new detection system - charge coupled and charge injection devices[28,29]. As yet, this innovative and promising measurement technique is used primarily in the research environment. Charge coupled and charge injection devices are more sensitive than diode arrays and have higher resolution but are still relatively expensive.

Evaluation of all options for detection systems for ICPs indicates that some are fundamentally better suited to SMEA than others. The photodiode array has many desirable features but lacks the breadth of wavelength range necessary for SMEA. The CCD and CID may in time become more popular for this type of work

but at present are out of the price range of many potential users. Thus, for many analytical applications the direct reader remains the most viable option.

1.3 Objective

The goal of this work was to modernize the computer interface for the ICP/polychromator system. The ICP unit is the PlasmaTherm ICP 2500 with a radio frequency generator and AMNS Automatic Matching Network. The direct reader is an automated Fisher Jarrell Ash AtomComp 750 (equipped with up to 50 PMTs) interfaced to a Digital Equipment Corporation PDP8/M minicomputer. This original system is described in Chapter 2. The intent is to re-interface the polychromator to a IBM PC, XT, or AT clone. Various approaches will be proposed and evaluated. The upgraded system is detailed in Chapter 3. Results that have been obtained with the revised system are presented and discussed in Chapter 4. Conclusions and possible methods for improving the revised system are given in Chapter 5.

Chapter 2

ORIGINAL SYSTEM

This chapter gives a description of the ICP/Direct reader system as it was received from NASA. A brief description of the instrument as a whole is given in the first section. The Jarrell Ash Direct Reader can be divided into three subsystems, each performing a unique function. The second section of this chapter describes the excitation source; the inductively coupled plasma. Section three deals with the detection system and optics; the PMTs and polychromator. The final section is devoted to the data acquisition and control system consisting of the channel modules and PDP8/M minicomputer.

2.1 The ICP Direct Reader

The ICP direct reader system as received from NASA consisted of the following components: the PlasmaTherm 2500 ICP unit (PlasmaTherm, Kresson NJ) with 27.12 MHz radio frequency generator (PlasmaTherm, Kresson NJ) and AMNS automatic matching network (PlasmaTherm, Kresson NJ); imaging optics, AtomComp 750 polychromator (Fisher Jarrell Ash, Waltham, MA) with PMTs and sockets (Hamamatsu, Bridgewater, NJ), Model 1307A High Voltage power supply (Bertan, Syosset, NY) channel module boards and module motherboard (Fisher Jarrell Ash, Waltham, MA), PDP8/M minicomputer (Digital Equipment Corporation), background correcter (wobulator) and controller. A diagram of the instrument is given in Fig. 3. Each component is described in further detail in the proceeding sections[30].

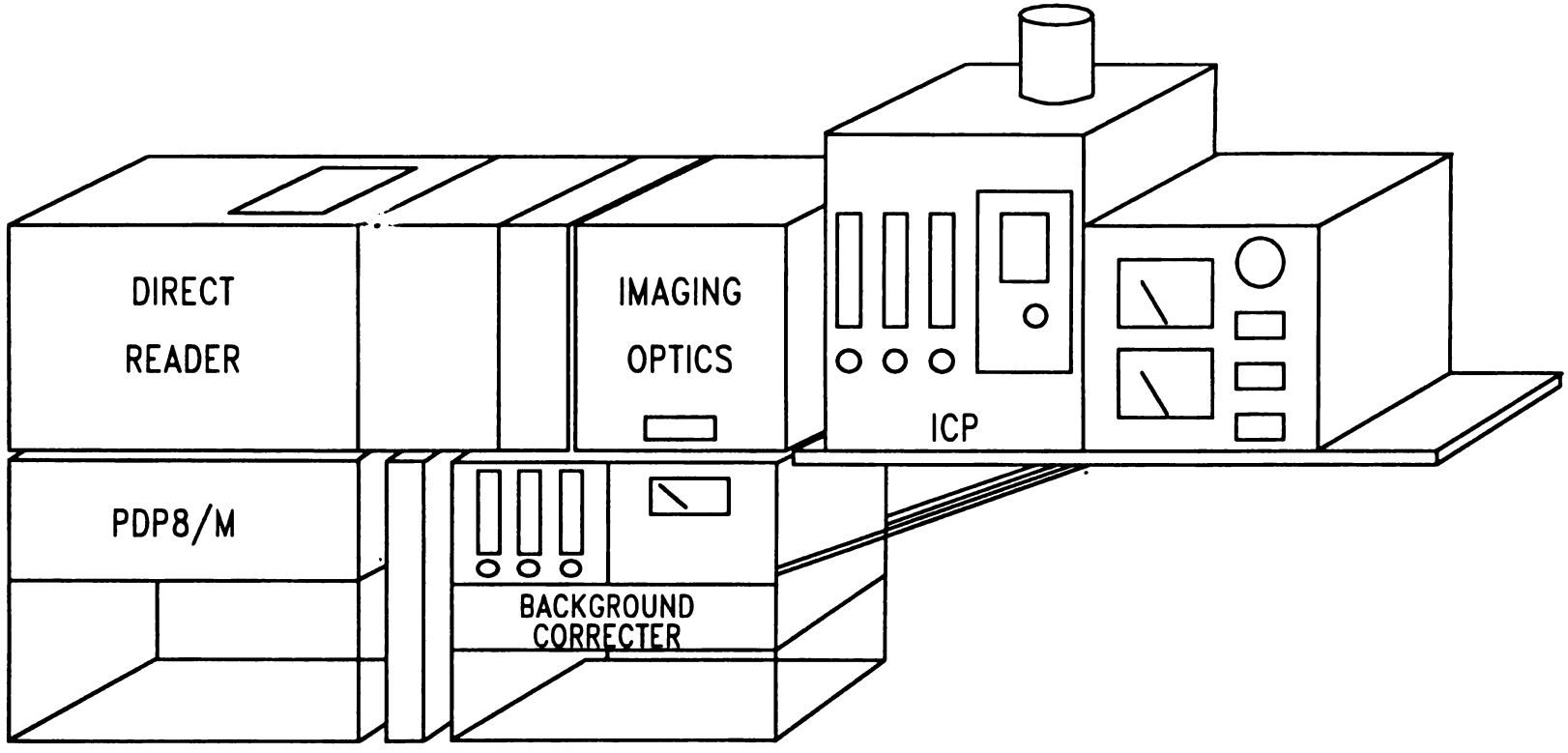


Figure 3: Diagram of ICP Direct Reader as received from the National Aeronautics and Space Association

2.2 ICP unit

2.2.1 Inductively Coupled Plasma.

The plasma unit itself is composed of a sample introduction system (consisting of a concentric glass nebulizer and spray chamber), the torch assembly, Tesla coil and load coil. A diagram of the sample introduction system and torch assembly is given in Fig. 4.

The plasma is ignited by a quick discharge of the Tesla coil across a gap at the base of the torch. The discharge provides the seed Argon ions and electrons required for generating the plasma. The seeded plasma is maintained by supply of alternating current (27.12 MHz) through the load coil at roughly 1 kW of power. RF power is coupled to the plasma via argon ions and electrons. Two features of modern instruments give rise to a stable plasma. The first is an automatic matching network which continually matches the output impedance of the RF generator to the impedance of the plasma and load coil. The second stabilizing feature is a continuous flow of coolant gas introduced tangentially between the plasma tube and the outer barrel of the torch. The torch is thus kept at a much lower temperature than the plasma.

2.2.2 Sample Introduction.

Samples are introduced into the plasma in solution form through a concentric nebulizer (Precision Glassblowing, Denver, CO) at a rate between 2 and 3 mL/min. The sample is aspirated from the spray chamber up through the innermost tube of the torch (Precision Glassblowing, Denver, CO). As the nebulizer gas flow rate is increased, a hole is formed in the centre of the plasma so that the plasma takes on a torroidal shape. The formation of this hole allows

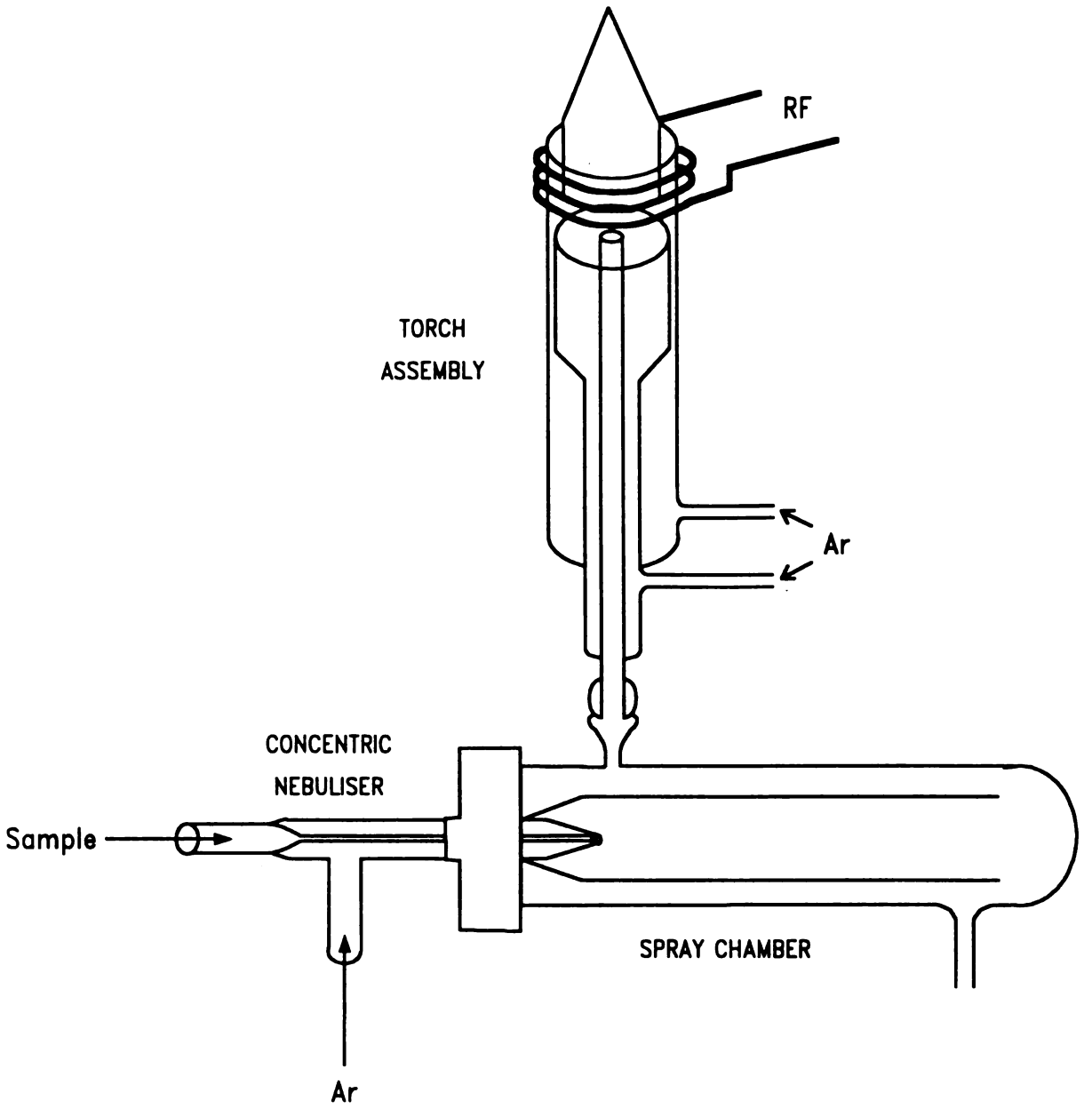


Figure 4: Diagram of the ICP sample introduction system

sample to reach the core of the discharge. This increases both the atomization efficiency and the residence time of atoms and ions in the plasma.

2.3 Detection System and Optics

2.3.1 Imaging Optics.

Two optical elements are used to focus a 1:1 image of the plasma onto the entrance slit of the polychromator. This is shown diagrammatically in Fig. 5. Focal lengths and relevant distances are given in the diagram. The optical elements are mounted in a cabinet which formerly housed a spark source.

2.3.2 Polychromator.

The image of the plasma is centred on a 25 μm x 2 cm bayonet type entrance slit. The entrance can be accurately translated using a micrometer so that optimal alignment of the spectrum onto the exit slits can be obtained. Radiation passing through the slit travels down a light pipe onto a 0.75 m focal length concave holographic grating (1509 grooves/mm). The grating is mounted on a rigid cast iron stand but can be adjusted in both vertical and horizontal directions and can be rotated with respect to the focal curve of the polychromator if necessary. The position of the grating is optimized at the factory[30].

Dispersed radiation is passed through a mask before reaching the exit slits on the focal curve. The focal curve has positions for 70 exit slit assemblies, up to fifty of which can be occupied at any one time. Each assembly is composed of a slit body that serves as a mount for the exit slit and refractor plate, as well as alignment pins, hold down screw and clamp, the refractor plate, the exit slit, PMT socket and PMT.

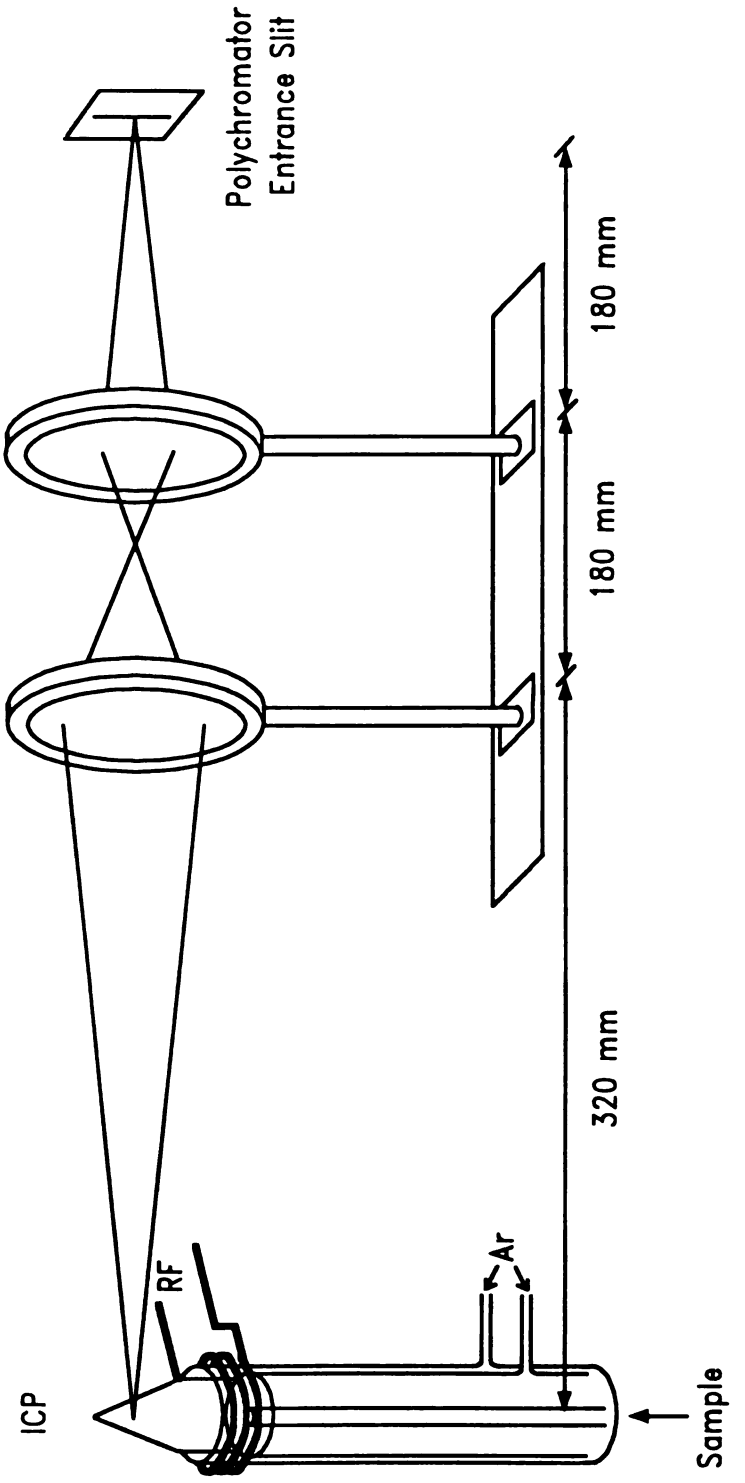


Figure 5: Plasma imaging optics

2.3.3 Slit Assemblies.

Exit slits are available in three widths: 10, 35 and 50 μm. The 50 μm slit is used for typical applications. The slit can be mounted in a right hand or left hand fashion and will have one of four radii of curvature depending on its position along the focal curve.

A refractor plate, mounted in front of each exit slit, allows fine adjustment of the wavelength passing through the exit slit. This procedure[30] is diagrammed in Fig. 6. The refractor plate is constructed either of quartz, corex or glass which is 1 or 3 mm thick. Plates that are one millimetre thick allow a 0.2 nm variation of first order radiation on either side of the centre wavelength of the exit slit. Three millimetre plates allow a 1.0 nm sweep on either side of the centre wavelength. The refractor plate also reduces other order stray radiation for a given region of the spectrum.

2.3.4 Photomultiplier Tubes.

Three types of PMTs are available for use in various regions of the spectrum. All are side on mount Hamamatsu (Bridgewater, NJ) photomultiplier tubes which are most sensitive either to red, visible or ultraviolet radiation. The R427 has a useful wavelength range between 160 and 320 nm with a maximum response at 200 nm; its window is quartz and the photocathode material is Cs-Te. The R300 has a useful wavelength range between 185 and 650 nm and has its maximum response at 340 nm. The photocathode for this PMT is Sb-Cs and its window is constructed of UV glass. The R889 is used between 185 and 850 nm with a maximum response at 530 nm. Its photocathode is a multialkali material; its window is also UV glass. All are low dark current models which can produce photocurrents of up to 10 μA.

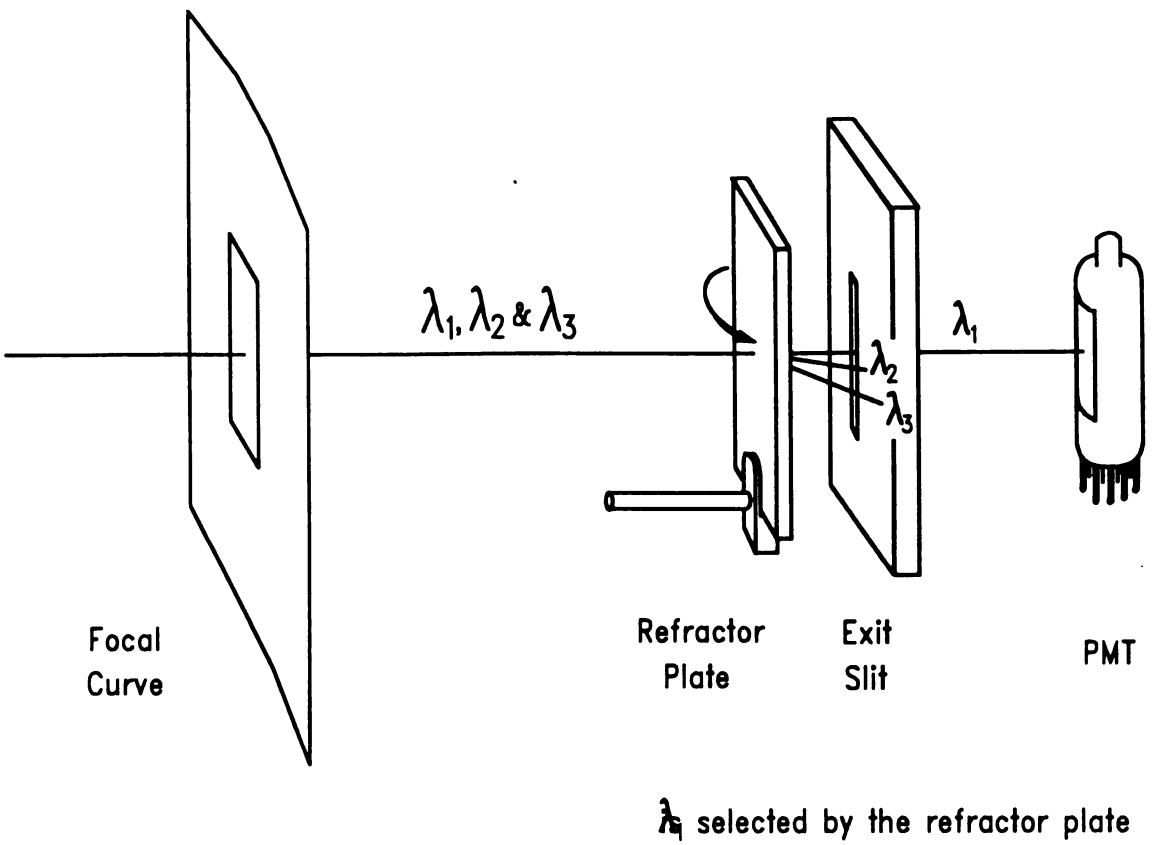


Figure 6: Ray trace through refractor plate and slit assembly.

PMT sockets are constructed with a total dynode chain resistance of about 10 MΩ , (about 1 MΩ between each pair of dynodes). The sockets and PMTs are mounted by the manufacturer. Each socket is connected to a power distribution or 'mother' board which supplies a maximum of 950 V. All channels are tested at this voltage. If the count rate is too high, resistors are inserted in the J board for the individual channel to reduce the total PMT gain.

2.3.5 PMT Housings.

The photomultiplier tubes and sockets can be mounted in one of two types of housings. The first holds the PMT in an upright position about 5 cm directly behind the exit slit. A diagram of this housing is shown in Fig. 7[30]. When space constraints prevent this for a particular channel, an overhead mount is used. In this case the PMT is held perpendicular to the plane of the exit slit as shown in Fig. 8[30]. A mirror mounted at a 45° angle with respect to the PMT and exit slit is used to direct radiation to the photocathode. In both cases a reflective sleeve fits around the PMT which extends to the exit slit. This increases the amount of radiation at the centre wavelength and reduces the amount of stray radiation reaching the photocathode.

2.4 Data Processing System

2.4.1 Channel Module Boards.

The channel module board performs integration of the photocurrent and decodes I/O instructions from the CPU. Each channel module is specific for a single element. The PMT is connected to its channel module board by a removable anode clip attached to an insulated solid wire fixed to the board. The photocurrent from the PMT passes along the lead directly to an operational amplifier configured as an integrating charge to voltage converter. A simplified circuit diagram is shown in Fig. 9[30]. The capacitance in the feedback loop is selected for the channel

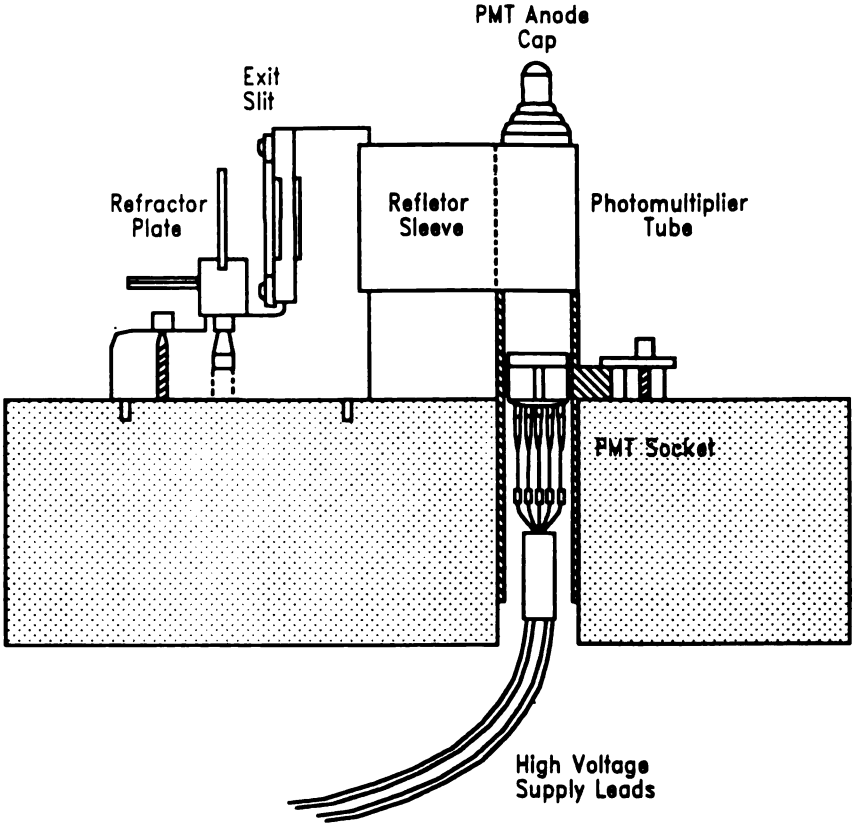


Figure 7: Cross section of a direct mount slit assembly with photomultiplier

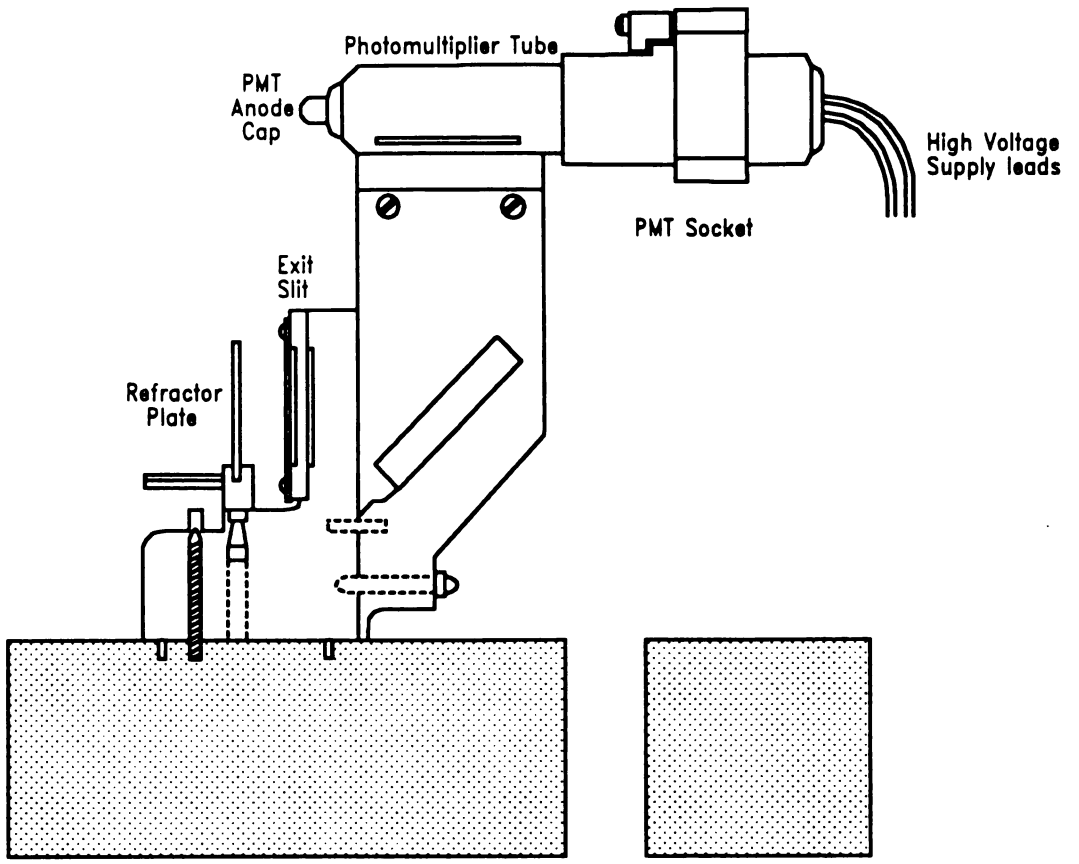


Figure 8: Cross section of an overhead photomultiplier tube holder

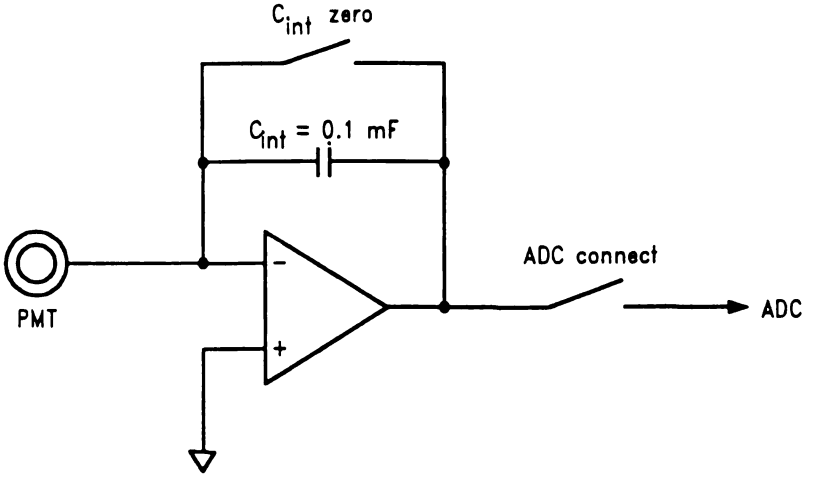


Figure 9: Simplified circuit diagram of the channel module as supplied by NASA.

(element) based on the relative intensity of its spectral line. This is typically 0.1 μF, but, for unusually weak lines, is 0.01 μF.

The operational amplifier is switched between integrate and zero modes by a field effect transistor (FET 2). In the Zero Mode, the capacitor is shorted and the operational amplifier output is converted to the input (summing point). When the FET switch opens, the capacitor is allowed to charge and the integrator is in Integrate Mode.

2.4.2 The PDP8/M Minicomputer.

Each channel module occupies one edge connector on the channel control board. The minicomputer communicates with the channel via this edge connector. Both control functions, (e.g. switch the capacitor from integrate mode to zero mode); and data acquisition functions, (e.g. send the output voltage from the integrator to the analog to digital converter (ADC)); are carried out through this edge connector. These functions are described in more detail below.

The central processing unit of the PDP8/M performs four main functions for the channel modules through the channel control board. These are listed below.

1. The CPU addresses and instructs any one of the 50 channel modules with one of the following commands:
    a.) Connect the integrating capacitor to the ADC.
    b.) Disconnect the capacitor from the ADC.
    c.) Zero the integrating capacitor by shorting it, which connects the operational amplifier to the inverting input (summing point).
    d.) Clear the capacitor's ground connection for integrate mode.

2. Requests the analog to digital conversion and transfer the count to the accumulator.

3. Transfer the contents of the accumulator to memory.

4. Select low or high gain mode for the analog to digital conversion. This allows two modes of acquisition:
   a.) Integrate using the integrating capacitor or
   b.) Profile by reading instantaneous intensities.

All user I/O is expressed in octal numbers and all operations of the computer can be synchronized to a real time clock.

Control of the Integrator.

The PMT is physically connected at all times to the integrating capacitor. Two field effect transistors control the status of the integrator and connection of the operational amplifier output to the analog to digital converter. The specific functions of each FET are given in Table 2 along with the octal codes which request the function.

Table II: Functions of Integrator-Controlling Field Effect Transistors

FET 1	Octal Code	Status of Integrator
open	202_8	Clear mode: A 100 kΩ resistor is placed across the terminals of the integrating capacitor. C_{int} will build up a voltage as a result of the photocurrent.
closed	201_8	Zero mode: C_{int} is shorted through a few hundred Ωs to the summing point of the operational amplifier.

FET 2	Octal Code	ADC Status
open	002_8	Disconnect: The ADC is not connected to the output of the integrator.
closed	001_8	Connect: Integrator output is connected to the ADC.

Control commands can be issued by the current program or typed directly into the teletype. These are three or four digit octal codes. Instructions are transferred to the decoders by I/O instruction 6164_8. The capacitor is connected to the ADC directly if 401_8 is specified or through a 300 fold amplifier if 402_8 is specified. The analog to digital conversion is initiated by I/O instruction 6161_8. The count is loaded into memory when the CPU receives I/O instruction 6162_8.

Integration Mode.

An example of the interrogation of channel one is given below. The procedure includes connecting channel one to the ADC, performing a conversion, transferring the count to the accumulator, and determining whether or not to zero the integrator. This cycle repeats every 16.67 ms.

1. A 6164_8 I/O instruction followed by the channel select code 001_8 are sent to connect channel one to the ADC. This closes FET 2.

2. A 6161_8 I/O instruction is sent which requests that an analog to digital conversion be performed.

3. The count is compared to 3777_8.
   a.) If the count is less than 3777_8, a 002_8 is sent to disconnect channel one from the ADC. This opens FET 2, allowing the capacitor to continue integrating.

b.) If the count is greater than 3777_8, the CPU transfers the count to the accumulator and then to memory with a 6162_8 I/O instruction. A 002_8 signal is sent disconnecting channel one from the ADC. The integrating capacitor is then zeroed by sending 201_8 and cleared for integration by sending 202_8 to FET 1.

Once the counts for all channels of interest have been stored in memory, they are available for readout as absolute intensities, relative intensities with or without background correction and can be converted into concentrations.

This implies that computer data acquisition is not initiated simultaneously for all channels; but all channels can be acquiring data within 16.67 ms.

Profiling Mode.

A channel that is being profiled can be monitored on a real time basis at a current meter mounted on the front left side of the cabinet below the polychromator. The analog voltage at the output of the operational amplifier is converted to a digital signal and then sent to a digital-to-analog converter (DAC) and finally displayed on the microammeter.

2.4.3 Additional Features.

Background Correction.

Background correction can be achieved by a computer controlled rotatable refractor plate system, called a wobulator mounted in the bottom left corner of the cabinet below the polychromator . A quartz refractor plate is mounted on a rotatable stage between the entrance slit and the grating. When the angle between the plate and the entrance slit is varied, the spectrum is shifted with respect to the

exit slits such that the spectral lines are not centred on the slits. The intensity measured by the PMT is then background intensity. This automated background correction procedure is shown in Fig. 10.

Slave Relays.

Also mounted behind the ammeter in the top left corner of the cabinet below the polychromator is a slave relay board. This houses a set of six power relays whose functions are described in Table 3. The power relays are operated by reed relays on the G board. All relays in the system were intended for the control and actuation of a spark source which was mounted in the space now occupied by the collection optics. A +12 V power supply is included to power the relays. This is intended for use with the spark source originally accompanying the polychromator.

Table III: Functions of Power Relays

Relay	Function
1	Fatigue lamp relay: Turns fatigue lamp on at the end of the exposure, turns lamp off on request.
2	Unused: Turns on an optional accessory with 113_8, off with 114_8.
3	Exposure relay: Turns on power to the source unit and to the EXP panel light during the exposure and preburn cycles. Computer software determines the duration of the preburn cycle.
4	Blank relay socket: Turns on a second optional accessory with 111_8, off with 112_8.
5	Standby relay: Turns on the SB panel light when the source is turned off. Turns SB off when source is on.
6	Flush relay: Opens the solenoid of the gas system mounted beside the microammeter in the upper left corner of the cabinet on user request. This relay is actuated by the controlling computer after relay 3.

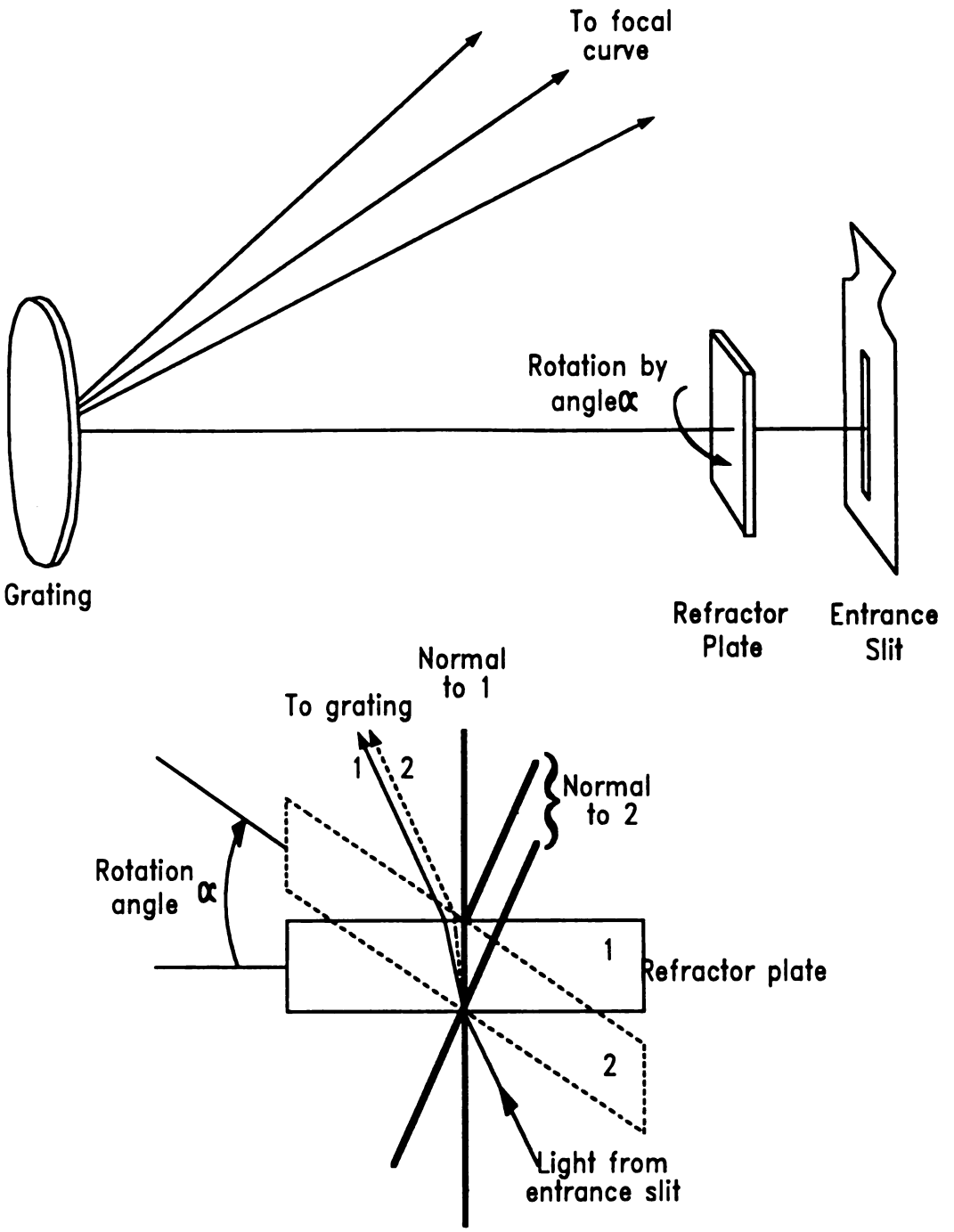


Figure 10: Diagram of the wobulator: method of background correction used with the Jarrell Ash Atomcomp 750.

2.5 Summary

The original data acquisition and control system, including the integrators and the DEC PDP8/M, has several advantages. Most importantly, it was constructed to accommodate up to 50 channels. Furthermore, the system provides options such as automated background correction, some data manipulation, and control of the excitation procedure if the spark source is used. The original system has virtually full automation of control of the instrument and data acquisition.

The data acquisition and control system also has some disadvantages. Most obviously it is outdated. The advances made in both digital and analog electronics over the past fifteen years warrant updating the instrument. For example, the operational amplifiers used as integrators could be replaced with the more stable, lower bias current models available today. The PDP8/M minicomputer could be replaced by a faster, higher capability IBM compatible (or MacIntosh type) microcomputer. The DEC PDP8/M has only 64K of random access memory and uses paper tape drives for long term storage. The user interface consists of a teletype or paper tape reader. Instructions must be given in the form of octal number sequences or primitive basic code. Data presentation facilities are minimal. Today's computers are faster, smaller and have more capabilities than the PDP8/M. Thus, an upgraded interface would greatly enhance the viability of the ICP/direct reader system as a research quality instrument.

Chapter 3

UPGRADED SYSTEM

As discussed in the introduction, it was the goal of this work to design and construct an interface for the ICP polychromator system described in chapter 2. In the first section of this chapter the desired features of the upgraded system are outlined. Two design approaches are evaluated in the second section. The third section discusses the modifications made to the original instrument. A detailed description of the upgraded system is presented in the final section of this chapter.

3.1 Desired Features

The most obvious requirement for the upgraded system is replacement of the PDP8/M minicomputer by an IBM compatible microcomputer. This will increase the speed and performance of the system and also improve its user interface.

Another important feature of the upgraded system is the capability for simultaneous multielement analysis. The original system allows simultaneous measurement of up to 50 channels. These are gated independently, however, so that a channel begins and ends integration in a sequential fashion. This allows unique integration times (i.e. variable gain) for all channels. It might be more convenient to have all channels gated by the same signal and provide some other means of gain selection. Finally, the upgraded interface should give detection limits, signal to noise ratios and sensitivities competitive with state-of-the-art systems.

3.2 Design Approaches

There are two unique options for the design of a system with the characteristics discussed above. These are techniques involving integration of

analog signals or those involving integration of digital signals. In this section these two options will be presented and compared.

3.2.1 Evaluation of Options

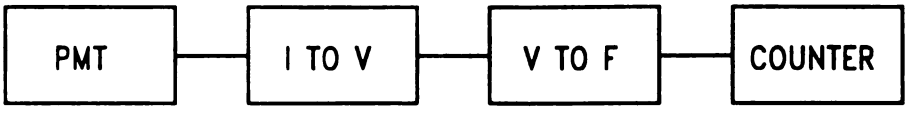
Analog Integration.

A block diagram of an interface based on analog integration is given in Fig. 11a. Like the present system, this option involves integrating the current from the photomultiplier tube using an operational amplifier with a capacitor as its feedback element. Inherent in this option is the necessity to address each channel module individually (for integrator SET and RESET) which requires decoding logic. For this option, the simplest approach would be to replace the outdated components on the existing boards with new ones and to use a PC/XT or PC/AT clone equipped with an ADC board for data acquisition. This would provide four or five independent channels.

Digital Integration.

A block diagram of an interface based on digital integration is given in Fig. 11b. In this option, the photocurrent is first converted to a voltage using an operational amplifier equipped with an appropriate feedback resistor. The voltage is then converted to a frequency using a single, commercially available voltage to frequency converter (VFC). This performs an analog to time domain conversion. The final step would be to count the frequency using a counter/timer chip which completes the analog to digital conversion process. This option involves essentially reconstructing the majority of the existing system rather than replacing key components.

a) Option 1: Integration of charge



b) Option 2: Integration of frequency

Figure 11: Outline of options for PMT interface

3.2.2 Comparison of Options.

In order to determine which of the two methods is the more appropriate, they were compared based on construction time, cost, and analytical figures of merit.

Time.

The first option maintains much of the existing system as it is. The integrator boards would be modified and the computer replaced. The second option requires full reconstruction of the channel modules as well as replacement of the computer system. Furthermore, software already exists for data acquisition with two ADC boards; the Analog Devices RTI/850 and the IBM data acquisition and control adapter. A counter/timer chip has been used in the laboratory but for applications other than the one of interest. On the basis of time required for construction, then, the first option seems more attractive.

Cost.

Again, the first option requires only the purchase of replacement components for the channel module integrator boards, whereas the second option would require supplies for their complete reconstruction. However, the cost of an ADC board when compared to the cost of a counter/timer greatly favors the second option. This has become true only in the recent past with the lack of availability of the IBM data acquisition and control adapter. A second option, Analog Devices' RTI/850, is priced at 1100$ versus 325$ for the Metrabyte Counter/Timer Module. When considering cost, the second option appears to be more favorable.

Analytical Figures of Merit.

This is perhaps the most important basis for comparison of the two methods. Several analytical figures of merit will be discussed which are relevant to the choice of the better method for modernizing the polychromator interface.

Resolution

Since both results would be 16 bits, technically neither method gives an advantage over the other with respect to resolution. The second option, however, could accomodate a 32 bit result.

Flexibility

The first option has a variable integration time in the sense that the integrator can be set and cleared as many times as the user wishes up to a total time of 10 seconds. For uninterrupted integration, the time is fixed by the capacitance value and the magnitude of the signal. One advantage of this method is that each channel's integrator can be set and cleared an independent number of times so that the total integration time could be different for each channel.

The second option allows the integration time to be any value from 1 μs to 3276.7 s, a span of roughly nine orders of magnitude. Clearly the useful range of integration times is dictated by the frequency values produced by the voltage to frequency conversion, but still the capability exists to use any integration time within the given range. In a truly simultaneous application, however, it must be noted that all channels would have the same integration time unless an independent source gated each of the counters.

The second option could easily incorporate a switchable current amplification factor so that any board could be used for any element. The first option dedicates each channel module board to a specific element.

Linear Dynamic Range

It is somewhat difficult to compare the linear dynamic ranges of the two methods. According to the AtomComp 750 manual[30], the maximum number of counts per second obtainable with the present system is about 250 000. This value for the second option will vary depending on the clock frequency used to drive the VFC. Assuming a 1 MHz oscillator is used, the maximum frequency output would be 500 kHz, and thus the maximum obtainable number of counts per second is 500 000. These values are comparable.

Sensitivity

In both cases the real sensitivity depends on the input bias current of the operational amplifier used either for integration or for current to voltage conversion. In both cases the bias current results in a small voltage output. For option one, however, the magnitude of the output voltage due to the bias current varies with time since V_{out} is charge and time dependent. The voltage output of a current to voltage converter does not vary inherently with time and can be calculated by:

$$V_{out} = -i_b R_f$$

Detection Limit

The susceptibility of a signal to variation or loss as it is passed between various elements of a system is an important consideration if the signal is small.

Analog signals are more susceptible to electrical noise manifested as amplitude fluctuations. Time domain signals or digital signals are much less sinsitive to these amplitude fluctuations since only HI and LO logic levels need to be distinguished; this type of noise does not change the frequency which encodes the signal. It is therefore likely that the frequency passed from the VFC to the counter will be better maintained than will be the voltage passed from the integrator to the ADC. Since the detection limit is three times the signal to noise ratio (expressed as the concentration of the analyte) it is possible that, all other things being equal, the second option will have associated with it a lower limit of detection than does the first.

Simplicity of System

Although this is somewhat an esoteric factor, the simplicity of a system often contributes to its user friendliness as well as to its functional lifetime. The second system proposed is probably simpler to construct and use because it involves no communication between the computer's CPU and individual channel module boards. The counter timer used with the second option serves as the integrator and the analog to digital converter and provides the gate signal for the integration process. The integrators of the first option are set and cleared by mechanical switches which must be controlled by a remote CPU.

3.2.3 Conclusions.

Based on the criteria discussed above the second option was chosen for the modernization of the polychromator interface. Specifically, reduced cost, wide linear dynamic range, good sensitivity, flexibility and simplicity make the second option the more attractive overall. The system which was constructed is described in detail in the next section.

3.3 Previous Approaches

The VFC and counter approach to data acquisition from photomultiplier tubes has been used by several workers. Blades and Horlick reported in 1981[31] a wide dynamic range data acquisition system for a single PMT using a VFC and an 8080 based single board computer. The key subsystem of the computer was an onboard 8253 counter/timer chip.

The 8253 counter timer has three 16 bit counters that can be programmed by the user. Both the frequency measurement and the integration time carried 32 bit resolution by cascading two counters on two separate 8253 counter timers. This afforded the wide dynamic range deemed necessary for spectrochemical measurements.

In the same publication by Blades and Horlick, a second wide dynamic range, microprocessor controlled data acquisition scheme was described. A current to voltage conversion is carried out as well, but in this case the voltage was immediately applied to a 10 bit successive approximation ADC which was interfaced to the single board computer. In a comparison of the two methods, the authors suggest that the VFC/counter approach may be better suited to multichannel measurements.

Horlick and Karannassios propose a method for interfacing the direct reader involving a current to frequency conversion followed by counting. They suggest that the system could be controlled by a single board computer[32].

Judith Auping's PhD thesis[33] describes a 48 channel upgraded interface for the Jarrell Ash direct reader. In this system each channel module was equipped with a current to voltage converter, a voltage to frequency converter, cascaded 4 and

12 bit counters, a 16 bit latch and chip select logic. This method allowed all 48 channels to be easily interfaced but requires communication between the central processing unit and individual channel modules. In this system all channels cannot be addressed simultaneously; as with the original system each integrator is independently gated.

3.4 Description of Upgraded System

In two of the systems described above a VFC and counter approach is used to interface a PMT to a computer. In both cases, however, the resulting instrument lacks one of the two features desired of this system; multiple channels in the first case and simultaneity in the second case. These shortcomings are addressed in the discussion of this system. Each aspect of the signal processing is described below.

3.4.1 Current to Voltage Conversion.

The current-to-voltage conversion is carried out by an operational amplifier (OA) equipped with a resistor in the feedback loop; that is a resistor between the output and inverting input of the operational amplifier. The choice of which operational amplifier to use involved a compromise between the relative magnitudes of the input bias current and the offset voltage. Operational amplifiers are typically constructed with either a low bias current or a low offset voltage. For a current to voltage converter, the bias current is amplified by the same factor as the signal. The offset voltage, however, remains constant regardless of the amplification factor. Furthermore, it is possible, with some operational amplifiers, to trim the offset voltage with a potentiometer. For these reasons, an operational amplifier with a very low input bias current was chosen. The Analog Devices 549LH satisfied the requirements with an ultra low input bias current and a fairly low offset voltage. A diagram of the AD549LH based current to voltage converter[34] is given in Fig. 12.

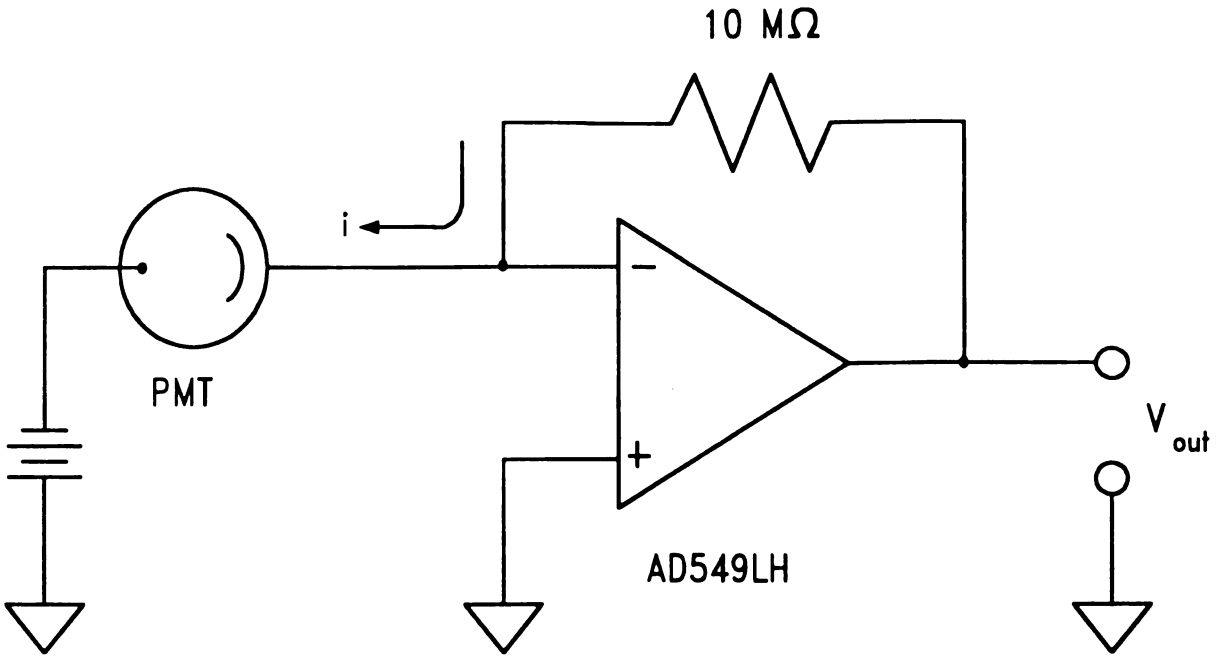


Figure 12: Circuit diagram of the current to voltage converter.

The feedback element for the current to voltage converter was chosen based on the expected magnitude of the photocurrent. The largest expected current should be amplified such that it produces a voltage no larger than the maximum voltage input of the voltage-to-frequency converter. The Hamamatsu photomultiplier tubes generally give no higher than 10 μA signals[35]; typical values of photocurrents listed in the literature are between 1 nA and 1 μA. The largest voltage for which the voltage-to-frequency converter will give a linear response is 10 V. A 10 MΩ feedback resistor gives 10 V for an input current of 1 μA

Two decoupling capacitors are used to filter the power supply; a 0.01 μF ceramic capacitor for low frequencies and a 1 μF Tantalum capacitor for high frequencies. These are placed between the supply voltage input pins and digital ground. The offset voltage was left untrimmed since its maximum value (0.4 mV) is small compared to the expected signals. Furthermore, the output voltage due to the dark current of the photomultiplier tube is an order of magnitude larger than the offset voltage (5 mV).

3.4.2 Voltage to Frequency Conversion.

The voltage-to-frequency conversion is performed by a single integrated circuit. The particular package was selected because it had low gain and linearity errors, a wide range of oscillator frequencies and high sensitivity. The AD652BQ specifies a 0.25 % gain error, a 0.002% linearity error, and a clock input of up to 5 MHz[36]. Finally the frequency output of the AD652BQ is synchronized to its clock input. A circuit diagram of the AD652BQ synchronous voltage-to-frequency converter (SVFC) is given in Fig. 13.

A synchronous voltage-to-frequency converter, like other VFCs, uses an integrator to carry out a charge balance of the input signal with an internal

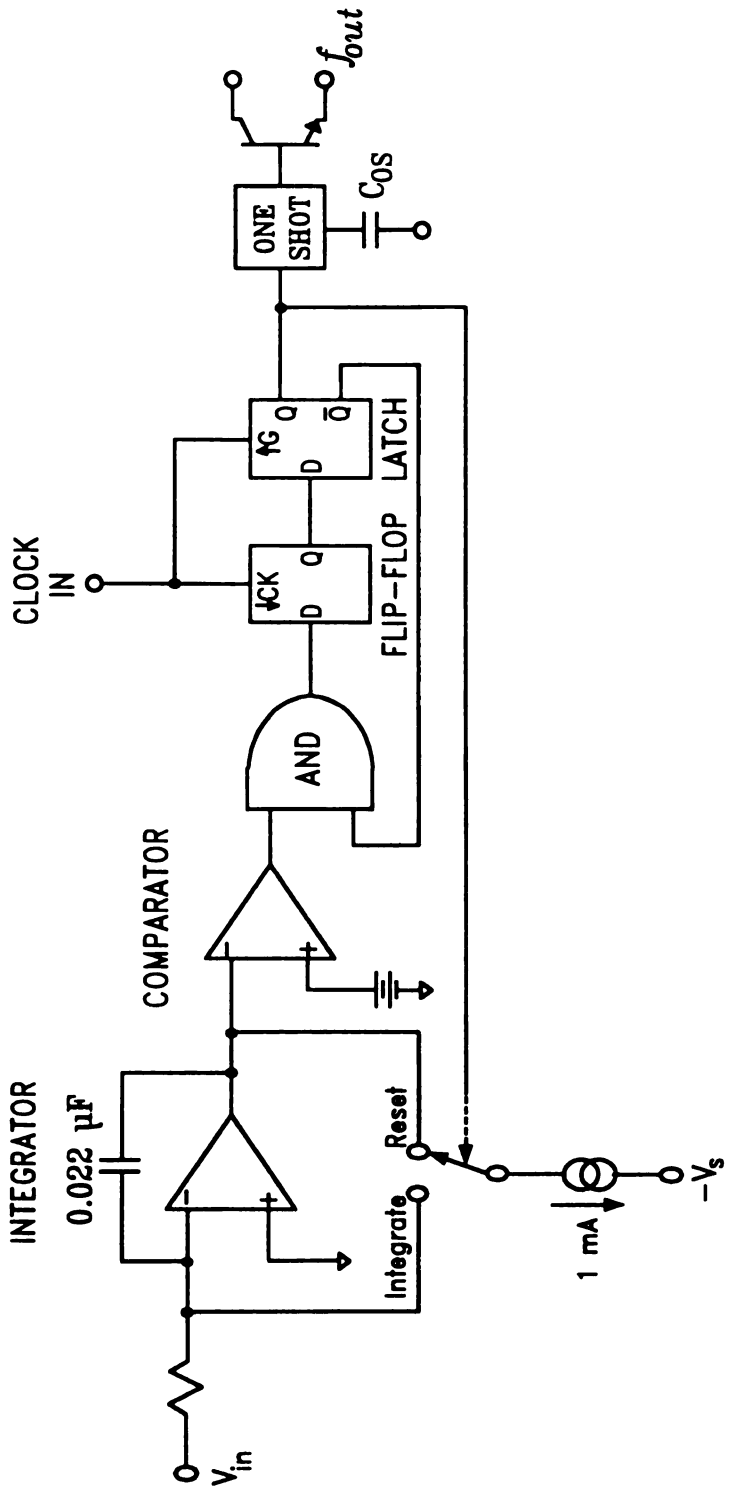


Figure 13: Schematic diagram of the AD652BQ synchronous voltage-to-frequency converter

reference current. However, for the SVFC, the primary timing element is an external clock rather than a one shot monostable multivibrator. This method removes the requirement for a high quality low drift capacitor and allows the user to determine the system stability and drift based on the performance of the external clock or oscillator.

The voltage-to-frequency conversion involves several key steps. Assuming the input signal is DC, the charge balancing integrator produces an up and down ramp output. After the integrator output has crossed below the comparator threshold the output of the AND gate goes HI. The next negative edge of the clock transfers the information to the output of the flip-flop. At this point, the clock level is LO so the latch does not change state. When the clock returns HI, the latch output goes HI. This simultaneously drives the switch to reset the integrator and returns the AND gate to a LO output state. On the next negative edge of the clock, the LO AND output is transferred to the output of the D-flop. When the clock goes HI the latch output goes LO, driving the switch back into integrate mode. At the same time, since not Q of the latch is HI, the AND gate is put into a state where its output will truthfully represent the output of the comparator.

An external oscillator frequency of 1 MHz was chosen for the system. This value gives reasonable frequency outputs seven at low output voltages and corresponds to a useful range of integration times between 1 and 1000 ms. A 0.022 μF mylar integrating capacitor was chosen. This was the component recommended in the data sheets for use with the device operated at frequencies greater that 500 kHz. A 1 kΩ resistor is inserted between the frequency out pin of the package and 5 V. This sinks any excess current from the VFC. Two decoupling capacitors of the same values and composition as those used for the operational amplifier are mounted near the supply voltage pin of the device to reduce AC noise from the

power supply. A 39 pF ceramic capacitor is chosen for the one shot giving a pulse width of about 200 ns. The one shot is actuated by connecting the capacitor to 15 V ($+V_s$). The voltage to frequency converter is configured for positive input voltages in the 0 to 10 V range. An input greater than or equal to 10 V gives an output frequency of one half of the clock frequency (500 kHz).

The synchronous VFC can be used in a number of creative applications. If the output frequency is gated by a signal derived from its clock, the clock stability is not important. In this configuration, the SVFC acts as a voltage controlled frequency divider giving a high resolution analog to digital converter. Also, if the clock signal for a SVFC is supplied by a VFC, the output frequency of the SVFC is related to the product of the two input frequencies. In this situation, multiplication and analog to digital conversion of two signals can be performed simultaneously.

Note also that the Q output of the latch goes HI for exactly one clock cycle. As long as the external clock is stable, the reset pulses applied to the integrator are always of the same duration. This reduces the linearity error and produces a very linear voltage to frequency transfer relationship.

One slight disadvantage of using a synchronous VFC is that the output is constrained to be an exact fraction of the clock frequency. For example, if the input current is exactly one quarter of the reference current then the output frequency will be one quarter of f_{clock}. This corresponds to one clock cycle for reset and three cycles for integration. Increasing the input current very slightly should produce an instantaneous, slight increase in the output frequency. This, however, is not what occurs. Initially, no change in the output frequency is observed. The output frequency remains at one quarter of f_{clock} so that an average of 250 μA is delivered to the summing point of the integrator. Because the input current is slightly greater

that 250 μA (corresponding to an input voltage of V_{IN} > {250 μA }{20 kΩ} > 5 V) the integrator accumulates charge. This causes the sawtooth signal that is the integrator output to drift downward, and the comparator threshold is crossed earlier with each integrator/reset cycle. Finally, a full clock cycle is lost and the integration time period lasts two clock cycles rather than three. Thus, the average output frequency of the SVFC is proportional (linearly related) to the input voltage but the instantaneous may not be.

3.4.3 Channel Module Boards.

The current-to-voltage converter, voltage to frequency converter, crystal oscillator, anode clip and BNC f_{out} jack are mounted on a 3" x 5" dual inline pin type vector board. Each board is equipped with two busses and two 30 position IC mount lanes. Each position is a 3 hole per pad strip on either side of a bus. The edge of the vector board has 30 copper strips with the same spacing as the edge connectors mounted on the channel module motherboard.

The vector boards were modified slightly for use with the system. The boards were first cut to fit the guides on the motherboard edge connectors. The connections between solder strip busses and copper fingers were severed. The centre arm of the outer bus was isolated. These modifications generated three floating busses which could be dedicated to $+V_s$, $-V_s$ and ground by connection to the appropriate copper fingers as dictated by the configuration of the motherboard. The three busses were then connected to the appropriate positions along the edge corresponding to those used in the original system. Positions 1 and 15 are at ground potential, position 2 is at $+V_s$ and position 3 is at $-V_s$. Position 12 is used for a 5 V supply voltage but is not connected to a bus on the vector board.

The ICs are mounted in 3M™ teflon crimp sockets. Wire wrap (22 gauge) wire is used to make connections between two sockets and to passive components. Photocurrent is passed from the PMT to the current to voltage converter via the anode clip which is connected to a 12" piece of stranded, flexible wire soldered to the vector board. The output of the SVFC is removed from the channel module board via a PC mount female BNC jack.

3.4.4 Channel Module Motherboard.

A motherboard for the five channel modules was constructed from existing components; a printed circuit board manufactured at NASA and edge connectors from a spare motherboard supplied by Jarrell Ash. The printed circuit board has positions for 50 edge connectors with busses connecting pins 1, 2, 3, and 15. Five of the edge connectors were removed from the original motherboard and mounted onto the printed circuit board. The +5 V bus at pin 12 was constructed by connecting jumper wires between adjacent edge connectors at that position. A four terminal barrier strip was mounted on the motherboard for connection of the power supply. The power supply for the channel module boards provides +15 V, -15 V, and 5 V regulated outputs and was constructed in house.

The output frequencies from the channel modules are sent to a BUD™ box via coaxial cable. Here the frequencies are transferred from the coaxial cable to the SOURCE input pins of the Metrabyte™ board (via 37 conductor ribbon cable).

3.4.5 Metrabyte Counter Timer Module.

The final step in signal processing is counting of the frequencies from each of the four channel module boards. This is achieved by the software control of a MetraByte counter/timer module, the CTM05. The key subsystem of the board is

the Advanced Microdevices AMD9513 counter/timer. Other components on the board include the system oscillator, base address selector and address decoding logic, and an interrupt line[37].

ADVANCED MICRODEVICES AMD9513 SYSTEM TIMING CONTROLLER.

This subsection gives a description of the AMD9513 system timing controller. Some of the general details of its operation are given[38] along with its specific uses in this system. A general block diagram of the AMD9513 is given in Fig. 14; a pinout is shown in Fig. 15.

The AMD9513 can be addressed through two I/O ports. The control port, which directly accesses the command and status registers and the data port which communicates with all remaining registers including the mode, load and hold registers for all five counter groups. The communication processes that occur within the AMD9513 are shown in Fig. 16.

Control Port Registers

The control port addresses the command register when writing and the status register when reading the hexadecimal (base 16) address 301. Both registers are 8 bits wide.

Command Register.

Several groups of functions can be performed by writing 8 bit command codes to the command register. These are: Data Pointer Register updating, Counter control, single bit Counter functions, and single bit Master Mode Register functions. Each group of functions is described below.

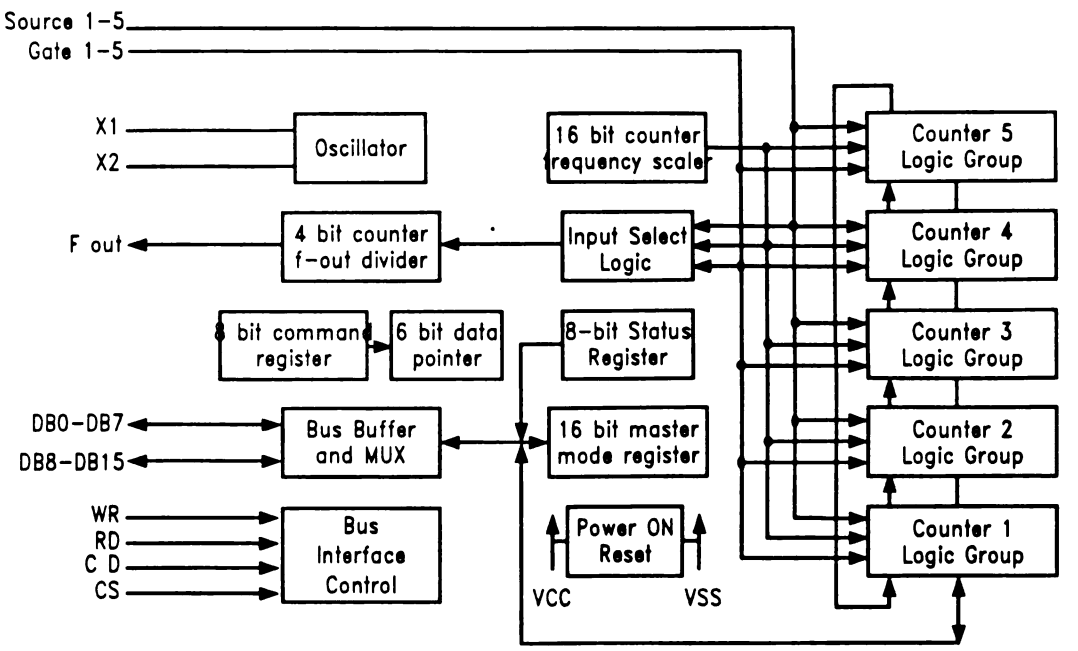


Figure 14: General block diagram of the Advanced MicroDevices 9513 Counter Timer.

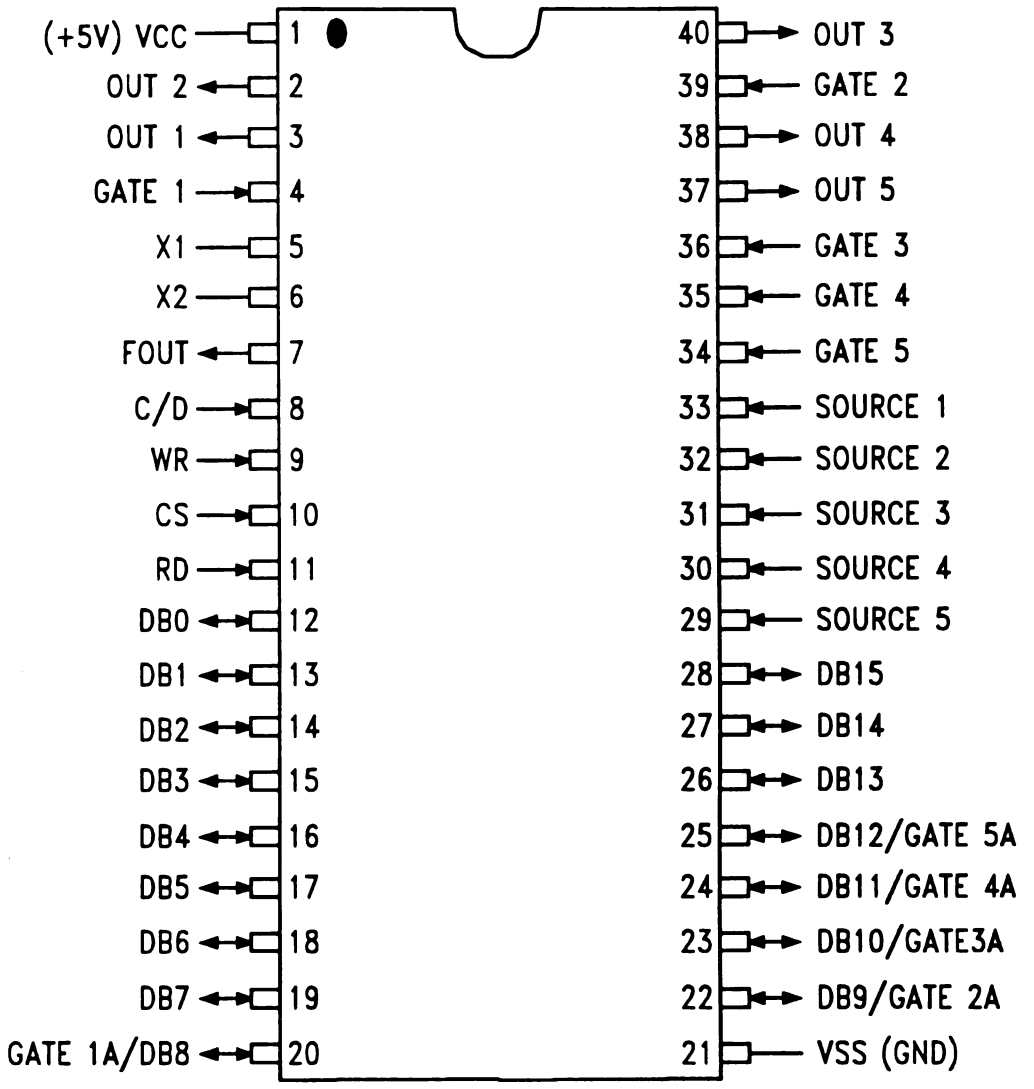


Figure 15: Pin out of the Advanced MicroDevices 9513 Counter Timer.

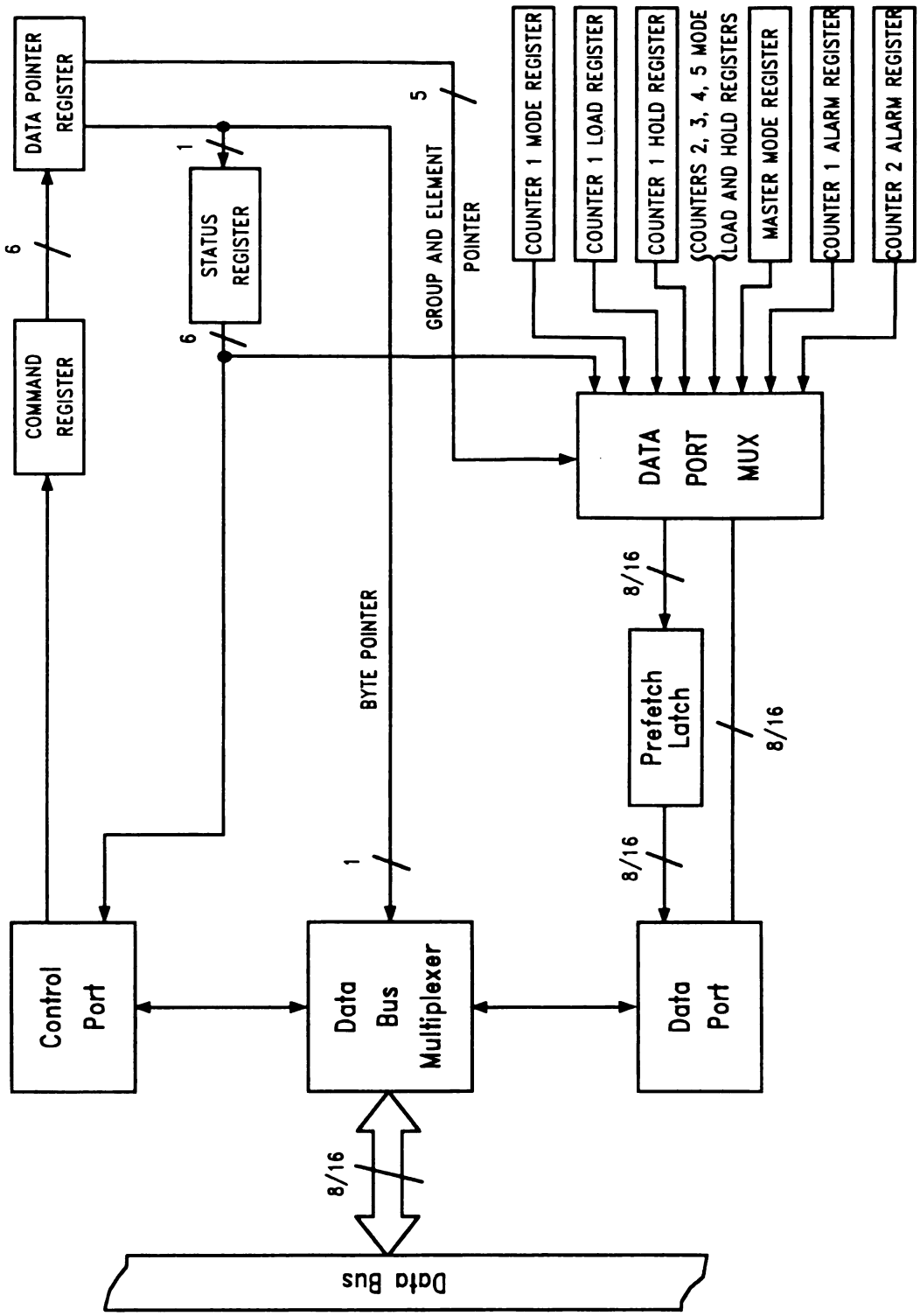


Figure 16: Communication within the Advanced Microdevices 9513 Counter Timer.

1. Data Pointer Register Updating.

All data pointer register (DPR) updates are requested by command codes having the three most significant bits set to 000. The location to which the DPR will point is specified by a three bit group pointer and a two bit element pointer. The group pointer selects either the control group or one of the counter groups. The element pointer specifies one of the available registers in the given group. The contents of the DPR specify the location for the next word sent through the data port. The bit sequences for accessible registers are given below.

The three bit sequence for each of the counter groups and the two bit element sequences available with each of the counter groups are listed in Table 4.

Table IV: Counter Group and Element Fields

Sequence	Group	Sequence	Element
000	illegal		
001	counter group 1	00	Mode register
010	counter group 2	01	Load register
011	counter group 3	10	Hold register
100	counter group 4	11	Hold register/hold
101	counter group 5		cycle increment
110	illegal		

To select the control group, a three bit group field of 111 must be specified. The elements of the control group are given in Table 5.

Table V: Element Fields for Control Group

Sequence	Element
00	Alarm register 1
01	Alarm register 2
10	Master mode register
11	Status register/no increment.

The data pointer register itself is 6 bits wide. Five of the six are the element and group fields; E2 E1/G4 G2 G1. The least significant bit of the data pointer register is the byte pointer which indicates whether the least or most significant byte of the data word is to be transferred on the next access through the data port.

2. Counter Control Functions.

All counter control function command codes begin with 001 through 110 and end with a five bit counter select field. Thus the function indicated by the first three bits is performed on the counter N if bit (N-1) of the command register is set.

3. Single Bit Counter Functions.

Single bit counter functions begin with 111 and end with 001 to 101 corresponding to the binary equivalent of counter 1 to 5.

4. Master Mode Register Single Bit Switching Codes.

These codes also begin with 111 but end with either 000, 110, or 111. Master mode bits 12, 13 and 14 can be set or cleared by selecting the appropriate command code. This is an alternative to using the data pointer register and the data port.

Status Register

The status register is an 8 bit read only register typically accessed by reading the control port, but can also be accessed via the data port as part of the control group.

The least significant bit of the status register (SR0) is a byte pointer which indicates which byte of a 16 bit word is to be transferred next (0=LSB, 1=MSB). This is functional only if an 8 bit external bus is specified since the Metrabyte board has a 16 bit internal bus. For a 16 bit external bus, this bit is always 0. Bits SR1 through SR5 reflect the internal outputs of counters 1 through 5 after the polarity select logic and just before the interface buffer circuit. The two most significant bits may be 0 or 1 and have no apparent purpose.

Data Port Registers.

Once the DPR has been loaded with the desired location, the next data transfer through the data port delivers its contents. Each of the registers described below is loaded through the data port in this fashion.

Counter Logic Groups.

Each of the five counter logic groups includes a 16 bit general counter with associated control and output logic, a 16 bit mode register, a 16 bit load register and a 16 bit hold register. Counter groups 1 and 2 also have a 16 bit alarm register and a 16 bit comparator. All registers are read/writeable through the data port, but the counter itself is never directly accessed. Comparator and alarm functions for counters 1 and 2 are controlled by the master mode register. A block diagram of the control of counter logic groups is shown in Fig. 17.

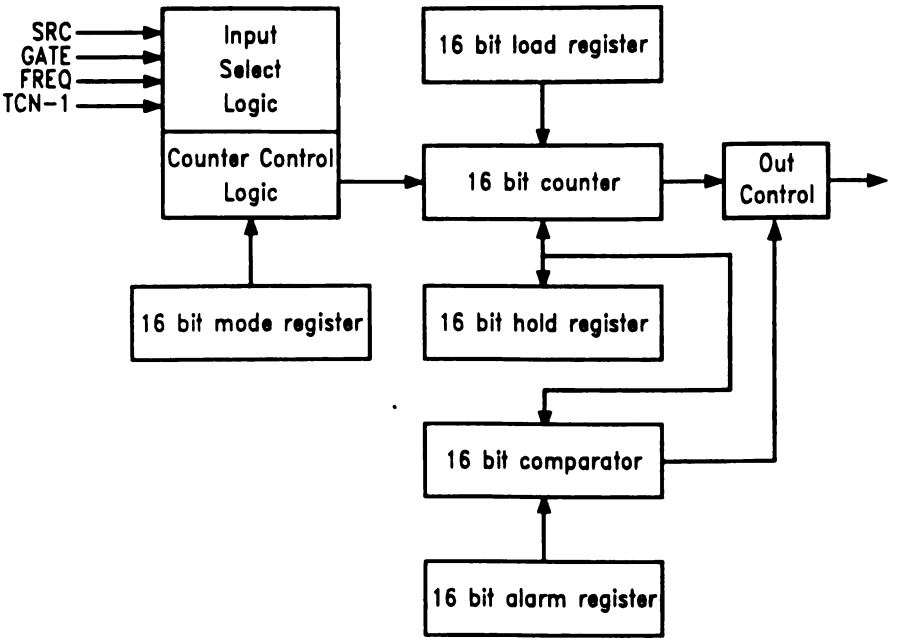


Figure 17a: Counter Logic Groups 1 and 2

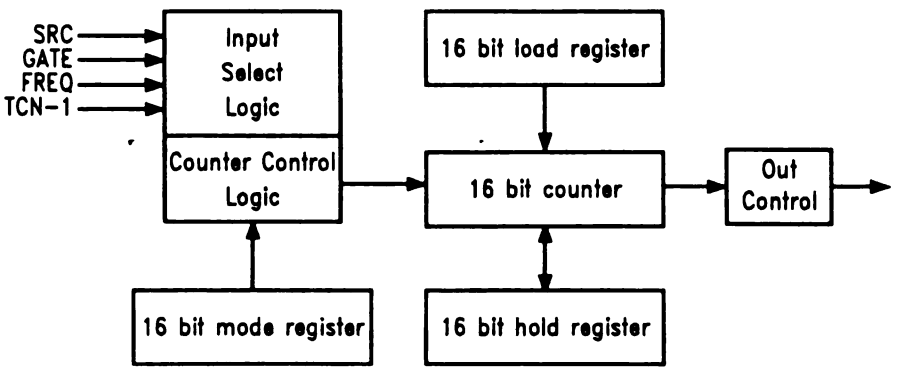


Figure 17b: Counter Logic Groups 3,4 and 5

The general counter is reloaded from either the load or hold register on each occurrence of a terminal count. The value in the load register is transferred to the counter after each terminal count. The terminal count is the point in time when the contents of the counter would have been zero if an external value had not been transferred into the counter. Regardless of the mode selected, the contents of either the load or the hold register are transferred to the counter on terminal count. Issuing a LOAD command or combinations of commands including the LOAD command is considered equivalent to a terminal count occurring.

1. Counter Mode Register.

The 16 bit counter mode register allows the user to specify the counting, gating, source select and output functions for its respective counter. A wide variety of mode options are available. A list is given in Table 6.

Table VI: Counter Mode Options

Mode	Description
A	Software triggered strobe with no hardware gating
B	Software triggered strobe with level gating
C	Hardware triggered strobe
D	Rate generator with no hardware gating
E	Rate generator with level gating
F	Non retriggerable one shot
G	Software triggered delayed pulse one shot
H	Software triggered delayed pulse one shot with hardware gating
I	Hardware triggered delayed pulse strobe
J	Variable duty cycle rate generator with no hardware gating
K	Variable duty cycle rate generator with level gating
L	Hardware triggered delayed pulse one shot
M	RESERVED
N	Software triggered strobe with level gating and hardware retriggering

Table VI Continued: Counter Mode Options

Mode	Description
O	Software triggered strobe with edge gating and hardware retriggering
P	RESERVED
Q	Rate generator with synchronization
R	Retriggerable one shot
S	Gate controllable delay/pulse width delayed pulse one shot
T	RESERVED
U	RESERVED
V	Gate controlled variable duty cycle rate generator
W	RESERVED
X	Hardware save

2. Load Register.

The 16 bit read/write load register can be used to specify the contents of its corresponding counter. The conditions for driving a counter to terminal count can be selected when the mode is specified, but issuing a LOAD command always drives the counter to terminal count. The action of the load register can be disabled by giving it a value of hexadecimal 0000.

3. Hold register.

The 16 bit read/write hold register can be used for two purposes. The first, as mentioned above, is the same as the load register; that is its contents can be transferred to the counter on terminal count. The hold register can also be used to store the instantaneous count value accumulated in the corresponding counter. Sampling the counter by transferring its contents to the hold register does not disturb the counting process. The STORE function can be executed by sending the appropriate command code to the command register at any time during the

counting process.

4. Alarm Registers and Comparators.

These elements and their functions are available only for counters 1 and 2. The comparator's output will be TRUE when the counters contents are the same as those of the alarm register. When the comparators are activated, the outputs of counters 1 and 2 will follow the state of the comparator; out = TRUE when the comparison is TRUE. The active level is specified in the counter mode register output control field. The comparators are activated individually by enabling the appropriate bits of the master mode register. The alarm registers can be loaded by issuing the appropriate command code through the control port such that the data pointer register points to the register, and then sending the desired value through the data port.

Master Mode Register.

The master mode register controls internal functions which pertain to the system as a whole or which are not controlled by the individual counter mode registers. Setting the master mode register requires sending two commands. A hex 17 command code is sent through the control port, which sets the data pointer to point to the MMR. The 2 byte master mode word is then sent through the data port. Master mode bits 12, 13, and 14 can be set individually by issuing master mode register single bit switching command codes to the command register through the control port.

Fig. 18 gives assignments for the 16 bits of the master mode word. The following is a brief description of system options that are controlled by the master mode register.

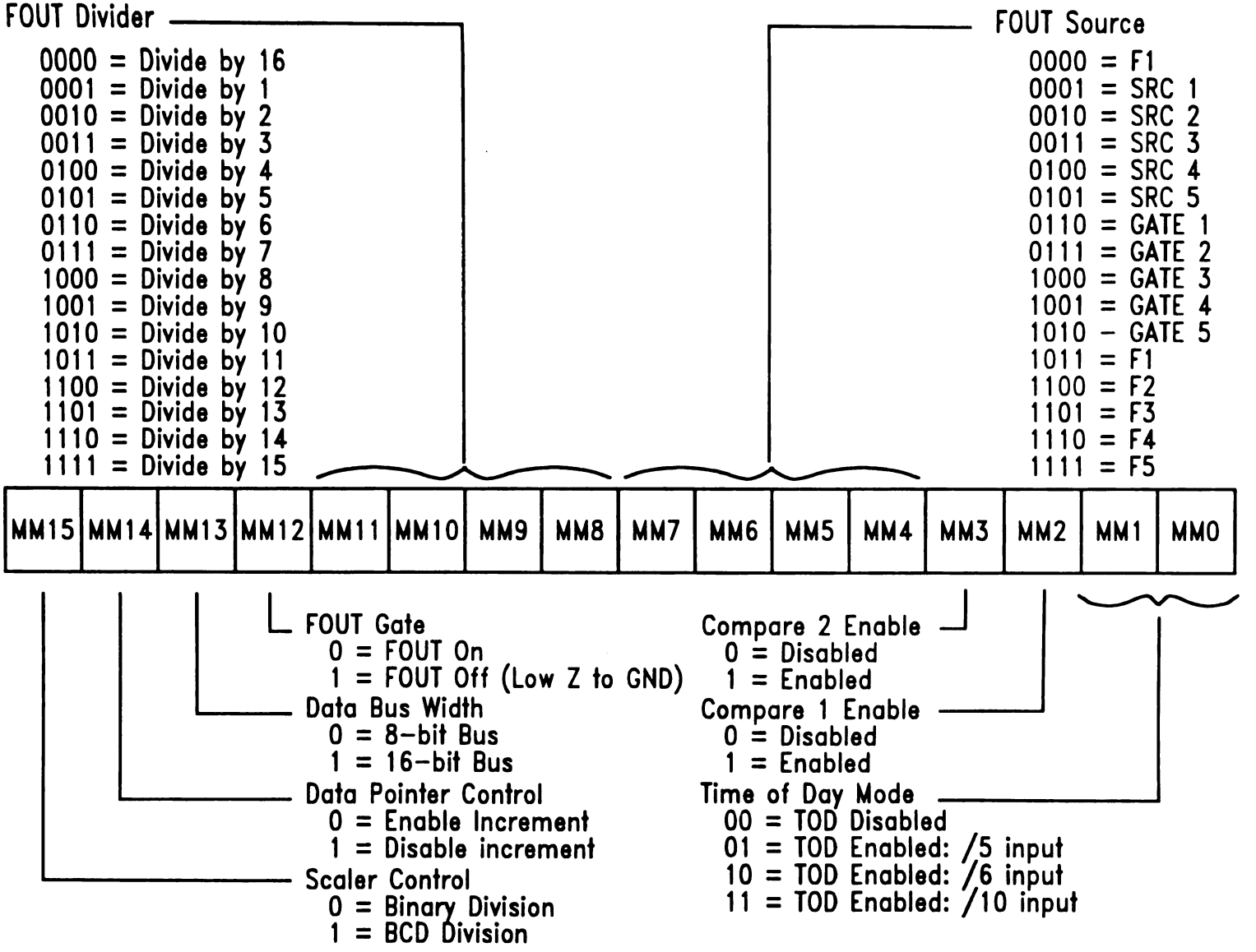


Figure 18: Master Mode Register Bit Assignments

1. Time of Day Mode.

This function is controlled by master mode bits 0 and 1. Bit assignments and their operations are given below.

00 - disabled
01 - enabled; 5 input
10 - enabled; 6 input
11 - enabled; 10 input

If MM0 or MM1 is 1 additional counter decoding and control logic is enabled for counters 1 and 2 which causes their decades to turn over at counts which generate 24 hour accumulations.

2. Comparator Enable.

The comparator functions for counters 1 and 2 are controlled by master mode bits 2 and 3.

MM2 = 1: Counter 1 comparator is enabled
MM3 = 1: Counter 2 comparator is enabled

If MM2/MM3 is 0, the corresponding comparator is disabled.

3. f_{out} Source.

The frequency input for the f_{out} divider is specified by the next 4 bits of the master mode word, MM4-MM7. The options include BCD or binary scaled oscillator frequencies, source inputs, and gate inputs.

4. f_{out} divider.

Master mode bits 8-11 specify the four bit value by which the f_{out} source is divided before being presented to the f_{out} pin.

5. f_{out} Gate.

Master mode bit 12 toggles the gate for f_{out} on (MM12=0) and off (MM12=1). When f_{out} off is chosen, the output is sent through a low impedance to ground.

6. Data Bus Width.

Master mode bit 13 toggles the data bus width between 8 (MM13=0) and 16 bits (MM13=1) wide. When an 8 bit external bus width is chosen the 8 lowest order bits of the internal bus contents are used for input/output.

7. Data Pointer Sequencing.

Master mode bit enables (MM14=0) or disables (MM14=1) the automatic data pointer sequencing functions. These are sequences through which the location specified by the DPR will progress on request. When MM14=0, any of the data pointer sequences can be specified or the data pointer register can be set manually using the appropriate command codes. When MM14=,1 the data pointer register can only be set manually. The automatic data pointer sequences that are available are described below.

Element Cycle

This cycle is selected by setting either bit in the element field (E1 or E2) to 0 and the group field (G4 G2 G1) to counter group N. In this configuration, the DPR points first to the mode register then to the load register and finally to the hold register of counter N. The completion of the first element cycle causes the group pointer to be incremented by 1; the element cycle is then repeated for group (N+1) and so on.

Hold Cycle

The hold cycle is enabled by setting the element field (E2 E1) to 11 and the group field (G4 G2 G1) to some counter group N. This selection cycles the data pointer register through the group fields N, (N+1), (N+2) and so on with the element fixed at the hold register.

Control Cycle

This sequence is activated by setting the element field (E2 E1) to anything but 11 and the group field (G4 G2 G1) to 111. In this configuration, the data pointer cycles through the elements of the control group only.

Status Cycle

This sequence is selected by setting the element field to 11 and the group field to 111 and involves no incrementing of the data pointer register. The DPR points to the status register all of the time.

8. Scaler Ratios.

Master mode bit 15 specifies the base by which scaled oscillator frequencies F2-F5 are derived. If MM15 is set to 0, the oscillator frequency is divided in binary fashion, by successive powers of 16; if MM15 is set to 1 the oscillator is divided in binary coded decimal fashion; by successive powers of ten.

3.4.6 Software.

An elementary program was written for simple data acquisition from the Metrabyte CTM05 board. The original program was written in Microsoft QuickBasic 4.00B. This was then translated into assembly code by Eric Hemenway

of the C. G. Enke research group. The assembler routines were written in the Turbo Assembler (TASM) environment. This was intended to increase the speed of execution. The final program uses a library of assembler routines callable from the main QuickBasic program. The library, CTMLIB, includes subroutines for setting the AMD9513 master mode register, configuring counters 1-5, starting the gate signal, checking the status of the gate signal, and storing the counts in counters 2-5 in an array. Each of the subroutines is described in detail in the following sections. The QuickBasic calling code and library of assembler routines is listed in Appendix 1.

CTMLIB.

This is the calling code for the library of routines described below. The system is first initialized by CTMLIB, relevant constants are defined, and then each routine is called in succession.

Setting the Master Mode Register: SETMMR.

This subroutine is called first from the QuickBasic program and serves to configure the master mode register of the 9513 for the desired system functions. This is typically if not always the first task to be performed when programming the AMD9513 counter timer. The data pointer register is loaded with the address of the MMR by writing the appropriate command code to the command register through the control port (17 Hex). Two bytes are then sent through the data port, D1D0 Hex, corresponding to the MMR bit assignments given in Table 7.

Table VII: Master Mode Register Bit Assignments

Bits	Function	Value	Result
0,1	Time of Day Mode	00	TOD disabled
2	Compare 1 enable	0	Disabled
3	Compare 2 enable	0	Disabled
4-7	F_{out} source	1101	F1
8-11	F_{out} divider	0001	Divide by 1
12	F_{out} gate	1	F_{out} off
13	Data bus width	0	8 bit bus
14	Data pointer control	1	Disable increment
15	Scaler control	1	BCD division

The time of day mode and comparator functions are disabled since they are not used. The f_{out} source, divider and scaler control were assigned arbitrary values since bit 12 turns off the f_{out} gate. The data pointer control bit is set to 1 to disable automatic data pointer sequencing functions. This restricts the programmer to changing the contents of the data pointer only by loading the command register with the appropriate byte. An 8 bit bus width is specified to allow flexibility in the choice of the controlling microprocessor.

Generating the Gate Signal.

Choosing the Gate Signal.

The next subroutine will set up a gate signal for the data counters. As mentioned in the section describing the capabilities of the AMD9513, there are many gating options available to the user. Thus, it is advantageous for the user to define a set of requirements for the gate signal that form a basis for choice of a specific option. Three points seemed essential in this particular application. First, the frequency of the gate signal must be sufficiently adjustable to generate a wide

range of integration times. Second, the level of the gate signal must be readable so that the status of the data acquiring counters (integrating or ready for reading) can be quickly determined without disruption of the integration cycle. Third, the gate signal must be available as output on the 37 pin D connector so that it can be connected to the external gate inputs of the integrating counters.

These constraints leave two more obvious options for generating the gate signal. Both methods involve hardware triggering of the data counters; only the source of the gate signal differs.

1. Gate = f_{out}

The frequency output available to the user at the f_{out} pin is derived from the internal frequency source of the AMD9513. Two software specified parameters determine the magnitude of the frequency at the f_{out} pin. Any one of 15 internal sources can be divided by up to 16, in unit increments, providing a reasonably large number of gate periods. Sources which can be sent to the divider are chosen from the following options; any one of the five counter sources (SRC1-SRC5) or gate inputs (GATE1-GATE5), or one of five frequencies derived from the on board oscillator (F1-F5). The base frequency, F1, is the external oscillator frequency (1 MHz). The remaining four frequencies, F2-F5, are integral fractions of the oscillator frequency. If the scale for division is binary coded decimal (BCD), then F2-F5 are, respectively; 100 kHz, 10 kHz, 1 kHz, and 100 Hz. If the scale for division is binary, then F2-F5 are F1/16...F1/16^4.

The f_{out} pin is accessible at the D connector and can thus be used as input for the gate pins of the five counters but its output level cannot be determined directly by software inquiry. It could, however, be read through the digital input port available at the D connector.

All possible sources available to be sent to the f_{out} divider cannot be used with this application. The sources for the five counters (SRC1-SRC5) must be the frequencies produced by the VFCs; the gate signals GATE1-GATE5 also must be used, leaving only F1-F5. This is still a reasonable selection of frequencies since each element of the two sets of F1-F5 can be divided by any integer between 1 and 16. This gives a total of 136 unique output frequencies that can be used for gate signals. The calculation of periods for each frequency (and hence integration times) depends on the duty cycle of f_{out}. This is not, in general, 50% and varies depending on which of the five frequencies is used and what f_{out} divider ratio is chosen. Thus, f_{out} may not be the ideal source for a gate signal. Furthermore, in order to adjust the value of f_{out} and the state of the f_{out} gate, the master mode register must be reconfigured.

2. Gate = Counter 1.

As an alternative, one of the counter outputs could be used as a gate input for the remaining four counters. This counter can be configured to use an internal or external time base as its source. Given that the time base is chosen, the counter can be set to count (down) from any value between 1 and 2^{16}-1 (65535). The output of each of the five counters available on the D connector and is software accessible. Finally, the counter's output can be set to give a short pulse or to toggle its output state on each occurrence of a terminal count source pulse.

This option unfortunately requires the sacrifice of one of the data channels since one counter serves as a gate for the others. Thus only four channels of data may be acquired simultaneously as opposed to the five available with the first option. However, using one of the counters as a gate signal for the others produces a set of integration times spanning nine orders of magnitude in unit increments of

the smallest period (1 μs). Also, all functions of the gate counter can be controlled by issuing commands to the appropriate counter mode register or to the command register.

Based on flexibility and predictability of integration times, and simplicity of implementation, the second gating option was chosen for this system. The details of configuring counter 1 as the gate signal are given below.

Configuring Counter 1 as Gate: SETCNTR1.

In this subroutine, counter 1 is configured as the gate signal for the remaining counters. Before implementing this routine, the output pin of counter 1 (pin 35 on the D connector) is connected to the gate input pins of counters 2-5.

The counter mode register of counter 1 is loaded with the 2 byte word that corresponds to the desired actions; 0E02 Hexadecimal. The individual bit assignments are listed in Table 8.

Table VIII: Counter 1 Mode Register Bit Assignments

CMR Bits	Value	Function
0-2	010	Counter 1 output TC toggled
3	0	Count down
4	0	Binary count
5	0	Count once
6	0	Reload from load
7	0	Disable special gate
8-11	1110	Source = F4; 1 kHz
12	0	Count on rising edge
13-15	000	No gating

This selection enables single point data acquisition on user request. The integration is specified in ms since 1 kHz is selected for a time base.

Counters 2-5 will begin counting when their gate inputs are LO (this is defined in the CNTSEUP routine). To ensure that the gate is not opened before the user requests acquisition of data, the output of counter 1 is set HI.

Setting up the data counters: CNTSETUP.

This subroutine sets up the data acquiring counters. The mode register for each counter is set with the desired options. All other registers are loaded with zero to start. At the end of the subroutine, the counters are LOADed, ARMed and are waiting for the gate to open; that is for the output of counter 1 to go LO.

Each counter mode register is loaded individually in a loop. The number of counters being used is obtained as input from the user. The mode register for the current counter is loaded by sending the appropriate word through the data port. The bit sequence for the necessary functions is detailed in Table 9.

Table IX: Counters 2-5 Mode Register Bit Assignments

CMR Bits	Value	Function
0-2	000	Counter N output is inactive
3	1	Count up
4	0	Binary count
5	0	Count once
6	0	Reload from load
7	0	Disable special gate
8-11	N	Count source = SRC N
12	0	Count on rising edge
13-15	101	Gate = Active LO level GATE N

After the counter mode register has been set up, the load register of counter N is sent a value of zero. When the loop is terminated, counters 2-5 are LOADed and ARMed at the same time by sending a single command code (7E Hex) to the command register.

Starting the Gate Signal: STRTCNT1.

This subroutine loads counter 1 with the integration time, opens the gate by setting counter 1 output LO, and starts counter 1 counting down from the integration time.

The integration time is sent to the load register of the gate counter. The output of counter 1 is then cleared (set LO). Immediately after this command, the counter is issued a LOAD and ARM command, which begins its counting period.

Because loading and arming counter 1 does not toggle its output, the output of counter 1 following this command is still HI. Thus a LOAD and ARM command is not sufficient to provide the gate signal for counters 2-5. In order for counters 2-5 to begin counting, a LO must be presented to their gate inputs. This is achieved by CLEARing the output of counter 1 (setting it LO) immediately before this counter is given a LOAD and ARM command. Using this sequence of commands, the gate counter's output is LO and will stay LO for the duration of the integration time.

The disadvantage to this approach is that as soon as the gate inputs for counters 2-5 go LO, the counters are counting. This occurs before the gate counter starts counting through the integration period. The integration time then must be calculated to include the time delay for execution of the LOAD and ARM command. Since the software is written in assembly language, this delay is relatively short compared to typical integration times; perhaps a few microseconds added to at

least one millisecond.

Integration Cycle Status Check: CHKSTAT.

This subroutine determines whether or not integration is completed. This task is not trivial since operations which may interrupt the integration process must not be executed during the integration cycle. Thus, a non-invasive method for determining whether or not the cycle is complete is essential. Several conditions would indicate that the integration period had concluded. These are listed below.

1. The values in counters 2-5 are constant.
2. The output of counter 1 and the gate inputs of counters 2-5 are LO.
3. The gate counter has reached its terminal count (TC) value.

The first option requires making successive comparisons over time of the counts in each data counter. Since the source frequency could be any value between 0 and 500 kHz, this method is not feasible. Furthermore, whether or not a signal is being collected, the data counters are recording background and thus their values are always increasing.

The second choice requires reading the least significant bit of the status register (OUT1) until it goes HI. The options for determining the contents of the status register were discussed earlier in this chapter.

The final possibility involves reading the contents of counter 1 until they are equal to TC. Either of the latter two options is acceptable; the third was chosen. The conditions for driving to TC a counter operating as a software triggered strobe are described below.

When any software triggered down counter receives an ARM command, it begins counting down from some value N (the integration time) until it reaches a value of one. The count remains one for one cycle of the source at which point the counter is reloaded with the contents of a preselected register. The mode register was configured such that counter 1 is reloaded from the load register, so that the contents of the counter are again N. Counter 1 continues counting down to (N-1), the terminal count value. Thus, the TC condition is met for counter 1 when a source edge drives its count to (N-1) for the second time.

As mentioned above, the integration period is complete when the contents of counter 1 are (N-1) where N is the integration time. This event, however, will occur twice; once during the integration period, and again at TC. The first occurrence clearly must be ignored so two check status routines were written. CSTAT1 determines whether or not the gate counter has reached a count of (N-1) for the first time. This is accomplished by repeatedly comparing the contents of counter 1 to (N-1). The comparison is false while the count is greater than or equal to (N-1); true if the count is less than (N-1). When the comparison is true, the second check status routine is called. CSTAT2 also compares the contents of counter 1 to (N-1). The comparison is false in this case while count 1 is not equal to (N-1). When the count is (N-1), the comparison is true and the subroutine is exited.

Both check status routines perform the same function; that is to compare the contents of counter 1 with (N-1) without disturbing the counting process. The contents of the counter are sent to the hold register by issuing a SAVE command. By pointing to the hold register of counter 1, its contents can be taken through the data port as input. The value in the hold register is thus read into one of the microprocessor's internal registers, and the comparison is made. The process is repeated until the individual conditions for termination given above are met.

Save the data: STORECNT.

This final library routine stores the contents of the integrating counters in an array called CNTR. Each counter's contents are transferred to its hold register. The data pointer is set to point to appropriate location, the data word is read as input and finally stored in the array.

Calling Code: CTM05B

The main program, CTM05B.BAS, serves to obtain various pieces of information from the user and to call the library of assembler routines.

A filename and key data collection parameters are obtained from the user. The number of channels of data being examined and the integration time are then requested. With this information, the quicklibrary CTMLIB is called. When data have been acquired, the user is prompted to either save or reject the points. He/she may then collect another data point or exit the program.

Chapter 4

RESULTS AND DISCUSSION

In this chapter the results obtained with the revised system are presented and discussed. The experimental section gives the details of instrumental parameters used for data acquisition. The results section deals with the two goals of this work; the first being selection of four appropriate elements for simultaneous multielement analysis; the second being construction of calibration curves. Analytical figures of merit and SMEA capabilities of the ICP/direct reader are evaluated in the discussion.

4.1 Experimental

4.1.1 Instrumentation

The ICP-OES system used for this work is a PlasmaTherm 2500 inductively coupled plasma. This consists of an RF Plasma quartz torch and a Meinhard concentric glass nebulizer. The ICP is powered by a PlasmaTherm 27.12 MHz RF generator equipped with a PlasmaTherm AMNS automatic matching network. Radiation from the ICP is focussed onto the entrance of the polychromator with two optical elements; both are fused silica biconvex lenses with focal lengths of 60 mm and 90 mm. Focussed radiation is passed to a 0.75 m holographic concave grating (1509 grooves/mm). Dispersed radiation is passed through 25 μm exit slits onto $1^1/_8$ inch diameter side-on mount Hamamatsu photomultiplier tubes. Photocurrent from the PMTs is amplified, and then converted to a frequency. This frequency is then counted using a Metrabyte CTM-05 Counter Timer Module mounted in a Zenith IBM PC/AT compatible computer. The computer is equipped with a Zenith flatscreen color monitor, VGA card and Keytronix keyboard.

4.1.2 Parameters

For most experiments, the instrumental parameters used are listed in Table 10.

Table X: Instrument Parameters

Nebulizer OFF.

Plasma gas flow rate.....12.0 l/min
Auxiliary gas flow rate..... 1.0 l/min
Nebulizer gas flow rate..... 0.0 l/min
RF power..... 1.0 kW
PMT voltage..... 950 V
Integration time.....1000 ms

Nebulizer ON.

Plasma gas flow rate..... 14.0 l/min
Auxiliary gas flow rate..... 0.85 l/min
Nebulizer gas flow rate..... 0.65 l/min
RF power..... 1.50 kW
PMT voltage..... 950 V
Integration time..... 1000 ms

4.1.3 Solutions

Stock solutions were prepared by diluting the appropriate mass of a chloride or nitrate salt of the metal in 1 litre of distilled-deionized water (Millipore). Standard solutions of 0, 5, 10, 15, 20, 25, 40, 60, 80, and 100 ppm were prepared by dilution of the appropriate stock solution.

4.2 Results

Four calibration curves were obtained for Ca, Cd, Mg, and Ni. For all but calcium, concentrations of 0, 20, 40, 60, 80, and 100 ppm were used. Standards of 5, 10, 15, and 25 ppm were added for the Ca calibration. In addition to the single element calibration curves, data were collected from two, three and all four channels simultaneously for various concentrations of each element.

Initial experiments were carried out for measurement of the background. Electronic, thermal, stray light, and dark current contributions to this were determined independently. The conditions for each experiment are summarized in Table 11.

Table XI: Experimental Conditions for Determinations of Various Sources of Noise and Background.

	Digital Power	PMT Power	Anode Connect	Ent. Slit
Electronic Noise	on	off	no	block
Thermal Noise	on	off	yes	block
Dark Current	on	on	yes	block
Stray Light	on	on	yes	open

Average values of each type of noise are given in Table 12. These results indicate that the largest contribution to the background is stray light.

Table XII: Typical Counts for Various Sources of Noise and Background

Channel	Electronic Noise	Thermal Noise	Dark Current	Stray Light
1	25	29	30	330
2	6	7	14	153
3	21	21	28	687
4	33	33	66	574

Photomultiplier tubes and sockets were installed only at positions along the focal curve corresponding to elements of interest. All PMTs were aged for about 48 hours to allow stabilization of the dark current before being used for data collection. Optical alignment of the exit slits was verified in the following fashion. With the plasma off, hollow cathode lamps were mounted behind the ICP enclosure such that their radiation passed through the housing and was focussed onto the entrance slit of the polychromator by the collection optics. The position of the HCL was optimized to obtain maximum throughput of light through the polychromator. HCLs were powered with nominal currents of 5-10 mA and in most cases were single element lamps. Once the position of the lamp was optimized, the refractor plate for the relevant element was rotated to maximize the signal.

Four elements were chosen for initial studies. These were Na, Fe, K, and Ca. Typical count values (obtained from hollow cathode lamps) for each element are listed in Table 13.

Table XIII: Typical Counts for Initial Four Elements

Channel	Element	Wavelength	Counts
1	Fe	259.9 nm	30
2	Ca	393.7 nm	27750
3	K	799.4 nm	1388
4	Na	589.5 nm	59300

Although the intensity observed for iron at channel 1 was small, spectral interferences of much higher magnitude were seen at every other channel. For these reasons the PMT at channel 1 was moved from the Fe line at 259.9 nm to a Co line at 345.3 nm. Alignment of the Co slit was ensured. The plasma background intensity at all channels was then evaluated at the minimum PMT voltage.

With no solution being nebulized, three of the four channels gave the maximum number of counts. Since the PMT voltage was at its minimum value, the only means of further reducing the gain of the system was to reduce the amplification factor of the current-to-voltage converter.

The amount by which the amplification should be reduced was determined as follows. Neutral density filters were placed back to back in front of the entrance slit until the counts obtained at all four counters were on scale. Four 10% ND filters were required, implying that a reduction of three to four orders of magnitude of the I/V amplification factor would be sufficient.

The feedback element for a single board, the calcium at channel three, was switched to a 10 kΩ resistor from 10 MΩ. The plasma background was remeasured and found to be an acceptable value of about 2000 counts·s^{-1}. A 5 ppm Ca^{2+} solution was then aspirated into the plasma to estimate the sensitivity of the lower gain system. Approximately 52000 counts·s^{-1} were collected.

At the same time a second method was employed to reduce the measured background intensity of the plasma. The entrance slit to the polychromator was blocked such that only radiation at more than 12 mm above the load coil (ALC) passed through the slit. The plasma is hottest below about 10 mm ALC where most ion-electron recombinations and brehmsstralung (free electron continuum) occur. This results in extremely intense UV radiation. Masking the slit proved very effective in reducing observed background intensity. Average background counts are given in Table 14.

Table XIV: Background Intensities

Channel	Integration Time (ms)	Background Counts	Relative Std. Dev.
Ca	100	14400	1.3%
Ni	1000	615	1.0%
Cd	1000	700	1.0%
Mg	1000	185	1.0%

With the slit masked below 10 mm ALC and the gain of the channel at 10 V/mA, a 10 ppm Ca^{2+} solution was aspirated into the plasma. This gave a signal of approximately 2000 counts s^{-1} with a background of 500 counts s^{-1}. Solutions of 10 ppm Na^{+}, K^{+}, and Co^{2+} were then aspirated, again with the slit masked below 10 mm ALC but with a gain of 10 kV/mA. The signals for all elements were indistinguishable from the background.

Feedback resistances for the remaining three channels (Na^{+}, K^{+}, and Co^{2+}) were changed to 10 kΩ so that all channels have a gain of 10 V/mA. At the same time new elements were selected for these channels. Channel one collects Ni emission at 231.6 nm, channel two collects Cr emission at 425.4 nm and channel four collects Mg emission at 285.2 nm. The photomultiplier tubes at channels one and four were replaced with UV sensitive PMTs (Hamamatsu R427s). The electronic noise level was remeasured and the new PMTs were aged again for 48 hours prior to redetermination of dark current. The dark current was determined at both the highest and the lowest possible values of the PMT voltage. These values are given in Table 15.

Table XV: Dark Current at Various PMT Voltages

Ch.	Electronic Noise (cnts)	Dark Current (cnts) 580 V	950 V
1	9	2	10
2	35	1	10
3	27	900	32200
4	23	0	1

Aspirating 100 ppm solutions of each of the three new elements into the plasma and collecting emissions above 7 mm ALC gave the representative signals shown in Table 16.

Table XVI: Signals Obtained Above a 7 mm Height Above the Load Coil

Channel	Blank	Ni	Mg	Cr
1	30	160	30	33
2	510	510	510	515
3	2150	2170	2150	2150
4	25	25	35	35

The combination of masking the entrance slit and reducing the amplification factor of the current to voltage converter by three orders of magnitude gave a sensitivity far below that which could be expected. In order to increase sensitivity, the amplification factor was raised to 100 V/mA using a 100 kΩ feedback resistor for all four channels.

With the revised channel module boards in place, the entrance slit masked below approximately 12 mm ALC and the PMT voltage raised to 950 V, the following representative signal intensities were obtained:

Table XVII: Representative Signal Intensities Obtained at Reduced Gain

Channel	Blank	10 ppm Ca	100 ppm Mg
1 (Ni)	70	90	90
2 (Cr)	1250	1750	1750
3 (Ca)	3000	24000	4500
4 (Mg)	40	40	70

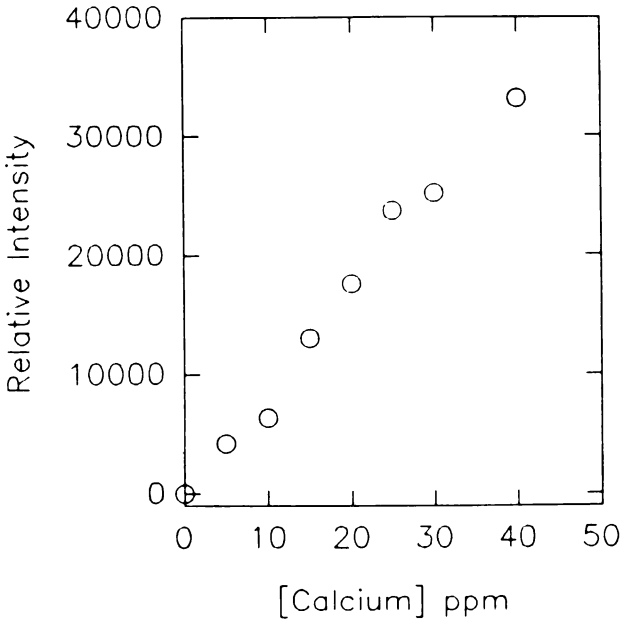
Following various unsuccessful attempts to improve the sensitivity of the chromium channel, and in light of its susceptibility to spectral interferences, again a new set of elements was chosen. The final positions of the PMTs are as follows: Channel one collects second order Ni emission at 231.6 nm, channel two collects second order Cd emission at 228.8 nm, channel three measures Ca emission at 393.7 nm and channel four measures Mg emission at 285.2 nm.

After selecting four elements for which simultaneous multielement analysis gives minimum spectral interference and acceptable sensitivity on all channels, the data acquisition software was improved so that runs could be made quickly in succession. Data for each element alone were collected on all four channels such that single element calibration curves could be constructed. These are shown in Fig. 19. Finally, emission studies of two, three and all four elements were conducted simultaneously. These results are given in Table 18.

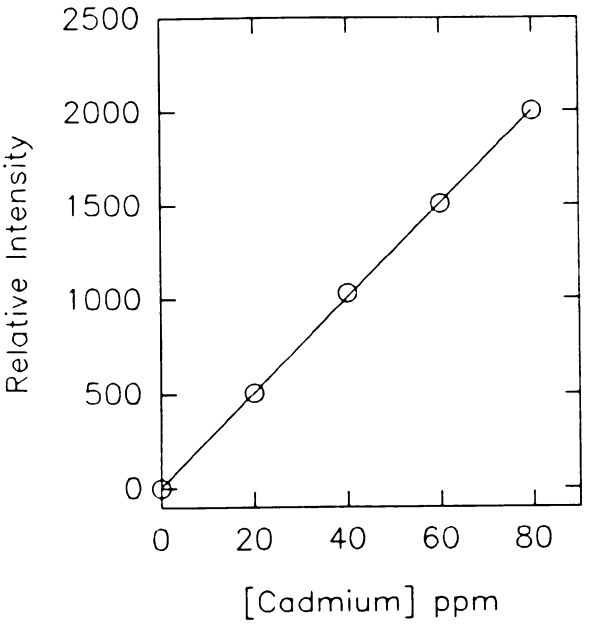
Table XVIII: Simultaneous Multielement Analysis with Upgraded ICP-OES System

Element	Concentration Measured	Actual	%Difference
Ca	6.45± 0.07	6.0	9
Ni	9.8± 0.1	10.0	2

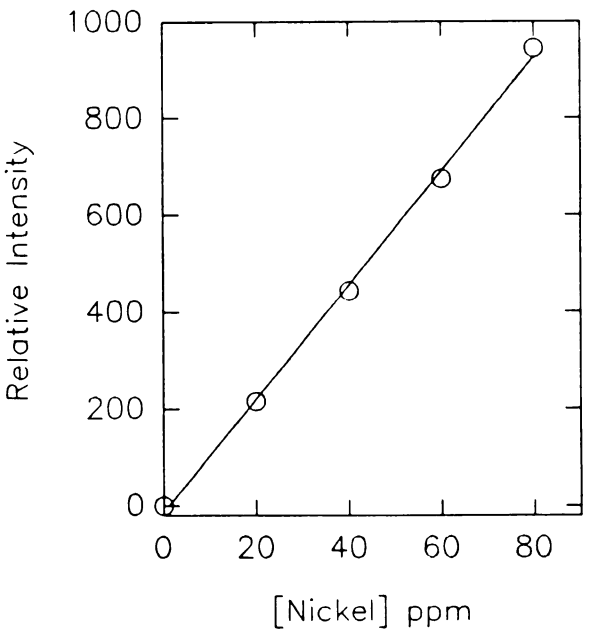
Calcium Calibration Curve



Cadmium Calibration Curve



Nickel Calibration Curve



Magnesium Calibraiton Curve

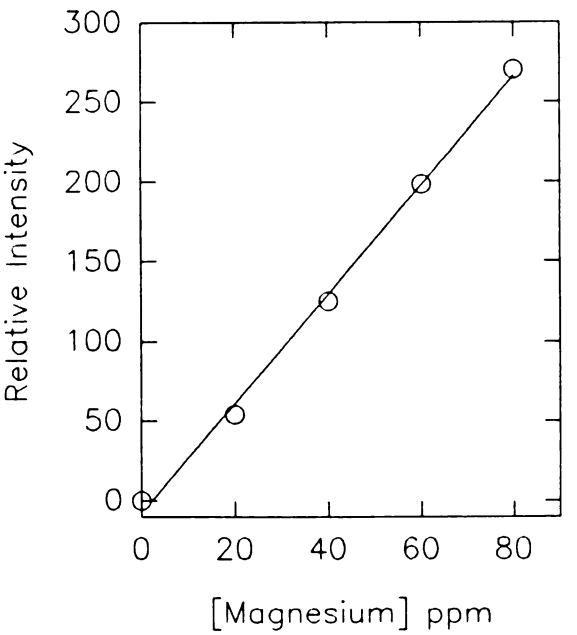


Table XVIII continued: Simultaneous Multielement Analysis with Upgraded ICP-OES System

Element	Concentration Measured	Actual	%Difference
Ca	6.36± 0.06	7.0	6
Ni	15.8± 0.2	15.0	5
Cd	9.8± 0.1	10.0	2
Ca	3.97± 0.04	4.0	1
Ni	11.8± 0.1	10.0	18
Cd	14.7± 0.2	15.0	2
Mg	16.1± 0.2	20.0	20

4.3 Discussion

The four channel, voltage-to-frequency conversion based data acquisition system was shown to be effective for simultaneous multielement analysis. The results presented above prove the feasibility of the system, but by no means reflect its full potential since data were collected under less than optimal conditions. In this section, analytical figures of merit of the ICP polychromator detection system are evaluated and discussed. Methods for improvement of these features are proposed with a focus on optimization of instrumental parameters.

4.3.1 Analytical Figures of Merit.

Sensitivity.

The revised system is capable of distinguishing between two photocurrents differing by a minimum of only 0.2 nA out of a total possible 100 μA. This is a function of the hardware based on the sensitivity of the voltage-to-frequency converter and the amplification factor of the current to voltage converter. With switchable gain, this value could be reduced.

Detection Limit.

Experimental (3σ) detection limits for the four elements studied are between 0.5 and 1 ppm. The values given for σ are standard deviations in the 0 ppm signal on the line of interest. Specific detection limits for each element are as follows: Ca: 0.7 ppm, Cd: 0.7 ppm, Ni: 1.1 ppm, Mg: 0.9 ppm. The Cd and Ni channels collect second order radiation, so their detection limits might be expected to be slightly higher than those collecting first order radiation (Ca and Mg).

Linear Dynamic Range.

The theoretical linear dynamic range is six orders of magnitude. This corresponds to the linear range of the voltage to frequency converter. The plasma can be expected to give a linear range of five orders of magnitude. The observed LDR is roughly three orders of magnitude.

Precision.

Typical relative standard deviation values are on the order of 1%. This figure is inherently highly dependent on the stability of the plasma.

4.3.2 Simultaneous Multielement Analysis.

In order for a system to be amenable to simultaneous multielement analysis, instrumental parameters must be similar for a large number of analytes. Excitation sources should be free of chemical and other types of interelement interferences, and matrix effects for a wide selection of analytes[10,11]. Spectroscopic tools in particular should be free from spectral interferences over a large wavelength range. The ICP itself satisfies all of these requirements to a very reasonable extent. The detection system, however, is less ideal. Several parameters including appropriate

individual channel gain, background intensity in the analytical window, spectral line intensity, etc. vary quite a bit depending on the element being studied. These problems could be removed with further optimization of the instrument.

When choosing a set of elements to be determined simultaneously, it was necessary, then, to select four whose signals are all on scale and roughly the same for a single integration time. This was somewhat difficult since individual channels are not all fully optimized. The single most important parameter to be optimized is the position of the refractor plates in front of each exit slit. If each spectral line were aligned, individual channel sensitivities would improve and perhaps be more similar.

Chapter 5

CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

The upgraded instrument maintains all of the capabilities of the original ICP direct reader system, and makes it competitive with state-of-the-art systems. The sensitivity and linear dynamic range are not reduced by the new interface; values for detection limits do not increase. The system's performance could be improved by optimization of optical alignment as discussed in chapter 4. Some modifications to the interface, however, might also enhance the instrument's overall performance.

5.2 Future Work

In the remaining paragraphs of this chapter, possible improvements of the direct reader interface are discussed. These are switchable gain, expansion to more channels, independent channel gating, larger number of counters per channel, and finally aesthetic improvements to the software.

5.2.1 Switchable Gain.

The addition of switchable gain for individual current to voltage converters (I/V) might aid in optimizing the sensitivity of each channel. As it stands, all PMTs receive the same dynode voltage (since all PMT sockets have the same total dynode resistance) and all signals are integrated for the same amount of time. With switchable gain I/Vs, one source of amplification is selectable by the user. The disadvantage of including switchable gain is that the system is somewhat more complicated with respect to the user. The benefits afforded by such a modification, however, outweigh this disadvantage. A simplified circuit diagram of a four option switchable gain current to voltage converter is given in Fig. 20.

5.2.2 Expansion to More Channels.

The expansion to more channels increases overall sample throughput since more analytes can be determined at one time. The likelihood of chemical and spectral interferences in such a system increases, but in many cases these can be corrected for. There are two methods by which more channels could be included. The first is to multiplex the inputs of each counter; the second is to use more counters.

Multiplexing of data channels is perhaps the more inexpensive method of expanding the system. Four counters could be used to count as many as sixty four frequencies. A block diagram of a 16 channel (multiplexed) interface for the direct reader is given in Fig. 21. The multiplex approach, however, inherently involves sequential analysis. Thus, the capability for simultaneous multielement analysis of all channels is lost.

A second option would be to use more counters. In this case there is one counter for each frequency (channel module board). A 50 channel system would then require eleven AMD9513 counter timers (assuming all channels use the same gate signal). A block diagram of a 19 channel interface using this approach for the direct reader is shown in Fig. 22. This approach retains the simultaneous multielement analysis capability of an ICP.

5.2.3 Independent Gating.

Independently gating each channel provides an alternative means of gain selection since each channel would have a unique integration time. Addition of this

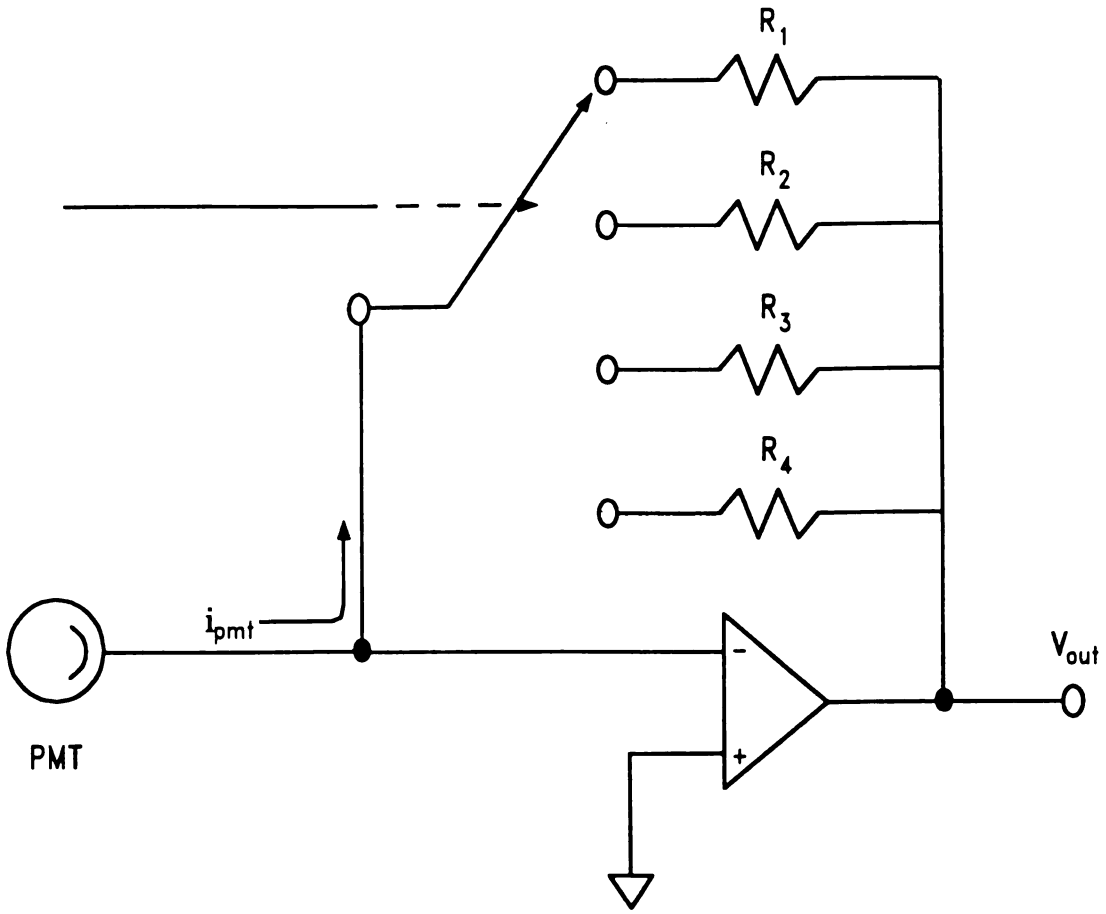


Figure 20: Diagram of a switchable gain current to voltage converter.

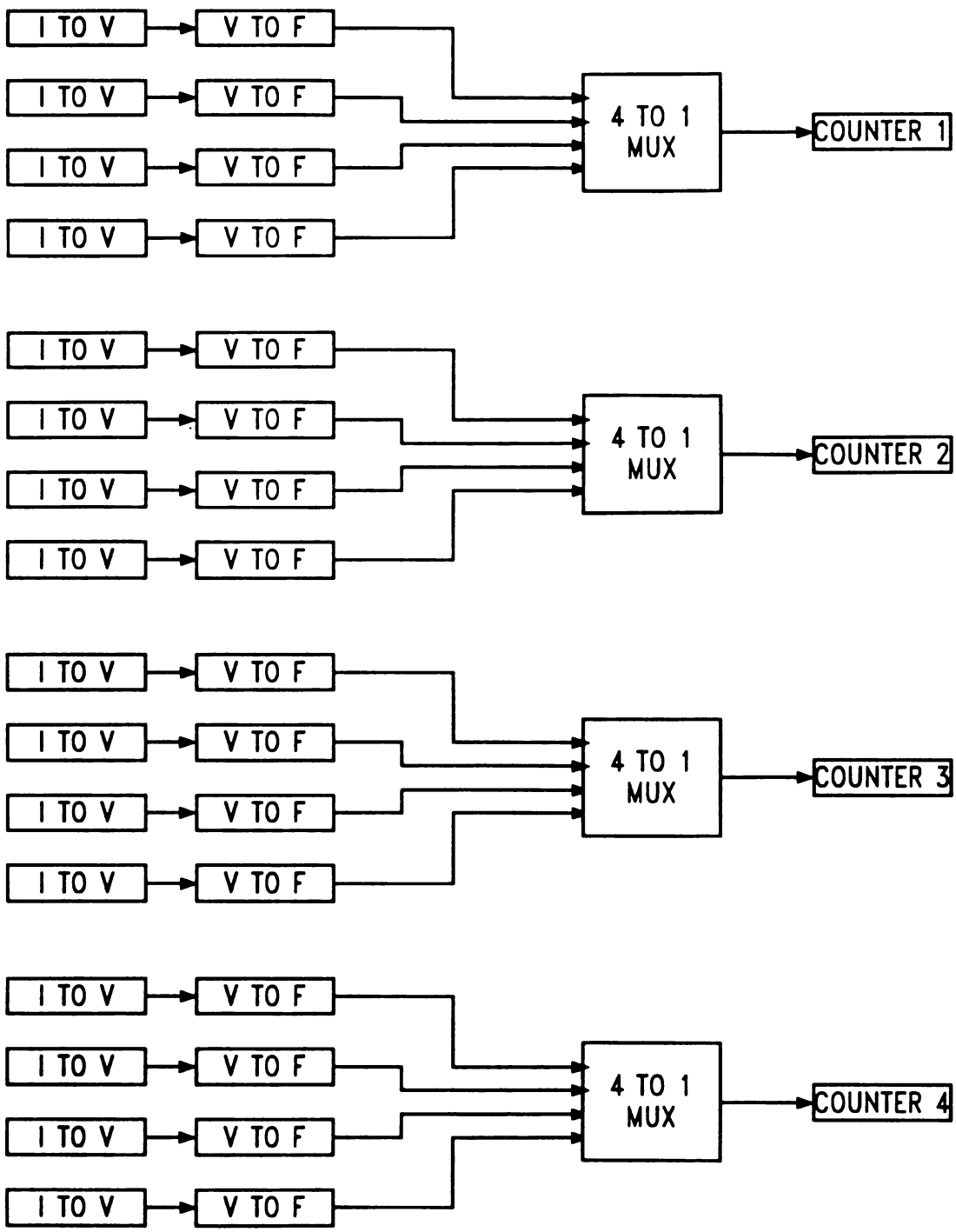


Figure 21: Diagram of a four-fold expansion of the Direct Reader interface using 4 to 1 multiplexers.

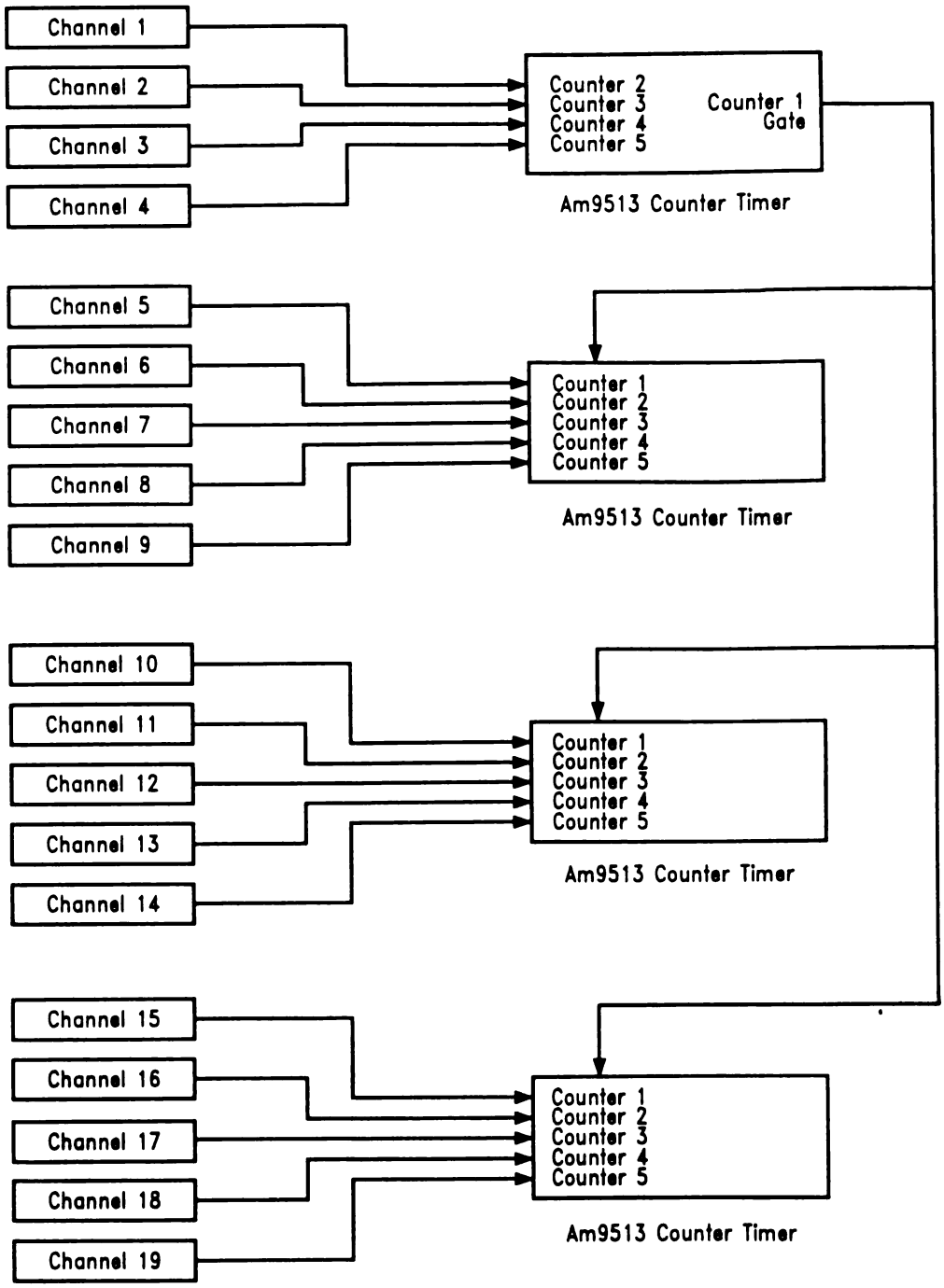


Figure 22: Expansion to 19 channel using four Analog MicroDevices 9513 Counter/Timers

feature, however, necessitates the use of at least two counters for each channel in the system. This is shown in a block diagram (Fig. 23). Expansion to many channels using this approach may be more difficult and would be more costly than using one gate for all channels; however, independent gating of channels results in a much more flexible system.

5.2.4 Channel Resolution.

The use of two cascaded counters for each data channel would double the present resolution and (logarithmic) linear dynamic range of the system. Currently, each channel has 16 bit resolution. The useful linear dynamic range (LDR) of the system is roughly 5 orders of magnitude. With two cascaded counters per channel, a 32 bit resolution and, hence, a linear dynamic range of 10 orders of magnitude are theoretically possible. The limitation to the LDR, in this case, would be the inductively coupled plasma itself which operates linearly over about 6 orders of magnitude. Thus, increasing the resolution to 32 bits may not afford much of an advantage.

5.2.5 Software Improvements.

Two modifications could be made to the existing software which would improve both its user interface and capabilities.

First, the option to collect flowing stream data at a fixed rate should be incorporated. Flow injection (FIA) is now widely used for sample introduction into a plasma and offers many advantages over conventional methods. Less sample is consumed and larger sample throughput can be achieved with an FIA-ICP-OES system[39]. Furthermore, combining SMEA with FIA-ICP would result in a highly modernized system.

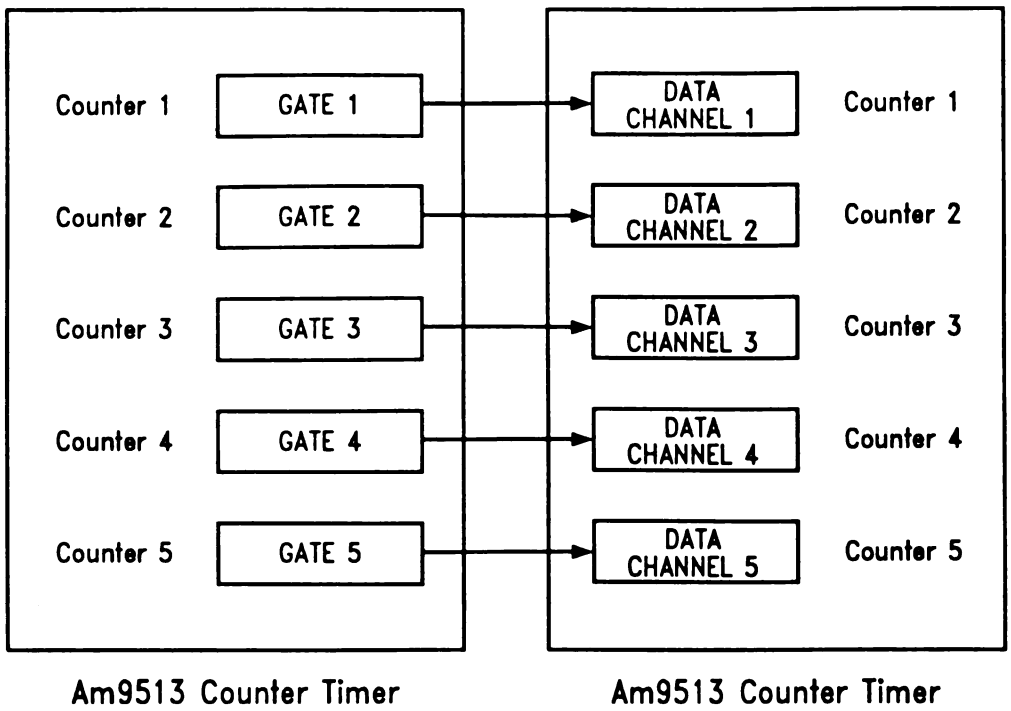


Figure 23: Independently Gated, Five Channel Interface for the Direct Reader using two AMD9513 Counter/Timers

Second, the package could be menu driven to increase ease and speed of its use. Potential options for the user might be choice of mode, time base, integration time, and number of data channels for data acquisition. This could be considered a somewhat esoteric improvement to the system, but would broaden its scope of potential users.

The upgraded system may well be improved by the modifications mentioned above, but is presently a research quality instrument capable of computer assisted simultaneous multielement analysis.

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APPENDIX I

Basic and Assembler Source Code Listings

```
; Name: CTMLIB
;
; Function: To initialize and control the CTM-05 board.
;
; Caller: MS-QuickBasic
;
; Declaration:
;
;   DECLARE SUB CTMLIB( BYVAL CNTR%, BYVAL INTTIM%,
;                 BYVAL SEGADDR%, BYVAL ADDRPTR% )
;
;   CALL CTMLIB(CNTR%, INTTIM%, VARGSEG(CNT&(1)),
;           VARPTR(CNT&(1)))
;
;    where CNTR% is number of used counters and INTTIM% is
;    the integration time (ms). The array must be a long
;    integer array.
;
;
.MODEL MEDIUM

.DATA

datptr EQU  word ptr [bp+06]     ; Array offset.
datseg EQU  word ptr [bp+08]     ; Array segment.
inttim EQU  word ptr [bp+10]     ; Integration time.
cntr   EQU  word ptr [bp+12]     ; Counter used.

dat  EQU  300h                   ; Define address of data register
cmd  EQU  301h                   ; Define address of command register

.CODE

PUBLIC CTMLIB

CTMLIB PROC

    push bp                      ; Store base pointer
    mov  bp,sp                   ; Setup own pointer
    push es                      ; Store extended seg. reg.
    push di                      ; Store data index.
;
    call far ptr[setmmr]
    call far ptr[setcntr1]
    call far ptr[cntsetup]
    call far ptr[strtcnt1]
    call far ptr[chkstat]
    call far ptr[storecnt]
;
    pop  di                      ; Restore data index.
    pop  es                      ; Restore extended segment.
    mov  sp,bp                   ; Restore stack pointer.
    pop  bp                      ; Restore base pointer.
    retf 8                       ; Return with 8 byte offset.
```

```
;
CTMLIB ENDP



; Routine: SETMMR
;
; Function: To set the Master Mode Register (MMR).
;
SETMMR PROC
;
; Call routine to set the Master Mode Register (MMR).
;
;
; Point to the Master Mode Register (MMR) through the
; command register (at &h301).
;
    mov  dx, cmd
    mov  ax,17h                 ; Set ptr to MMR
    jmp  $+2
    OUT  dx, al
;
; Set the MMR.
;
    mov  dx, dat
    mov  al,0d0h                ; Send lo byte first
    jmp  $+2
    OUT  dx, al
    mov  al,0d1h                ; then send hi byte.
    jmp  $+2
    OUT  dx, al
;
    retf
;
SETMMR ENDP



; Routine: SETCNTR1
;
; Function: To set counter 1.
;
SETCNTR1 PROC
;
; Point to counter 1 mode register through command register.
; Set the command mode register (CMR).
;
```

```
    mov dx, cmd
    mov al,1h
    jmp $+2
    out dx,al                   ; Set ptr to counter 1.
;
    mov dx, dat
    mov ax,2h
    jmp $+2
    out dx,al                   ; Send lo byte.
;
    mov al,0eh
    jmp $+2
    out dx,al                   ; Send hi byte.
;
    mov dx, cmd
    mov al,0e9h
    jmp $+2
    out dx,al                   ; To start, SET cntr 1 out (HI)
;
    retf
;
SETCNTR1 ENDP



; Routine: CNTSETUP
;
; Function: To setup the used counters.
;
CNTSETUP PROC
;
; Get the counting counters ready to go with the input
; parameters. On completion of the loop, counters are ready
; to go and are awaiting the gate signal. Also, load and
; arm counters 2-5.
;
    mov bx,cntr                 ; Move counters into bx.
    inc bl                      ; Offset due to counter 1.
;
    mov cx,2                    ; First counter used.
S1:
    mov dx, cmd
    mov al, cl
    jmp $+2
    out dx,al                   ; Point to mode register of counter.
;
    mov dx, dat
    mov al,8h
    jmp $+2
    out dx,al                   ; Config. mode reg. of counter.
;
```

```
    mov al, cl
    or  al,0a0h
    jmp $+2
    out dx,al                   ; Set for active LO gate level.
;
    mov dx, cmd
    mov al, cl
    or  al,8h
    jmp $+2
    out dx,al                   ; Point to load reg. of counter.
;
    mov dx, dat
    mov al, 0
    jmp $+2
    out dx,al                   ; Load with zero.
;
    inc cl                      ; Next counter.
    cmp cl, bl
    jng SHORT S1                ; Test if done.
;
;
    mov dx, cmd
    mov al,7eh
    jmp $+2
    out dx,al                   ; Load and arm counters.
;
    retf
;
CNTSETUP ENDP



; Routine: STRTCNT1
;
; Function: To start counter 1 counting.
;
STRTCNT1 PROC
;
    mov dx, cmd
    mov al,9h
    jmp $+2
    out dx,al                   ; Point to load reg. of cntr 1
;
    mov ax, inttim
    mov dx,dat                  ; Load with integration time.
    jmp $+2
    out dx,al                   ; Lo byte.
    xchg ah, al
    jmp $+2
    out dx,al                   ; Hi byte.
;
```

```
    mov dx, cmd
    mov al,0e1h
    jmp $+2
    out dx,al                   ; Now clear cntr 1 out (LO)
;
    mov al,61h
    jmp $+2
    out dx,al                   ; Begin read gate signal
;
    retf
;
STRTCNT1 ENDP



; Routine: CHKSTAT
;
; Function: To check if counter 1 is finished counting.
;
CHKSTAT PROC
;
; Check to see if we have passed the looped count.
; For a full explanation, see Julie Horner.
;
    mov bx,inttim               ; Move integration time to bx.
    dec bx                      ; Offset for counter overcount.
;
CSTAT1:
    mov dx, cmd
    mov al,0a1h
    jmp $+2
    out dx,al                   ; Hold counter 1.
    mov al,11h
    jmp $+2
    out dx,al                   ; Point to hold reg. of counter 1.
;
    mov dx, dat
    jmp $+2
    in  al,dx                   ; Read lo byte.
    xchg al, ah
    jmp $+2
    in  al,dx                   ; Read hi byte.
    xchg ah,al                  ; Put bytes in right order.
;
    cmp ax, bx
    jge SHORT CSTAT1            ; Check if counter now lower.
;
; Now, we check to see if finished counting.
;
```

```
CSTAT2:
    mov dx, cmd
    mov al,0a1h
    jmp $+2
    out dx,al                   ; Hold counter 1.
    mov al,11h
    jmp $+2
    out dx,al                   ; Point to hold reg. of counter 1.
;
    mov dx, dat
    jmp $+2
    in  al,dx                   ; Read lo byte.
    xchg al, ah
    jmp $+2
    in  al,dx                   ; Read hi byte.
    xchg ah,al                  ; Put bytes in right order.
;
    cmp ax, bx
    jne SHORT CSTAT2            ; Check if finished counting.
;
    retf
;
CHKSTAT ENDP



; Routine: STORECNT
;
; Function: To store the counter values in an array.
;
STORECNT PROC
;
; Save contents of counters 2-5 in hold registers. Return
; contents to caller via passed array.
;
    cld                         ; Clear direction flag.
    mov ax,datseg               ; Set ES to array segment.
    mov es, ax
    mov di,datptr               ; Set DI to array offset.
;
    mov cx,1                    ; First counter + 1.
;
S2:
    mov dx,cmd                  ; Command reg.
;
    mov al, 1
    shl al,cl                   ; Mask for selected counter.
    or  al,0a0h
    jmp $+2
    out dx,al                   ; Move count to hold.
;
```

```
    mov al,cl                   ; Reload counter number.
    inc al                      ; Increase by one for counter 1 offset.
    or  al,10h
    jmp $+2
    out dx,al                   ; Point to indiv. counter hold.
;
    mov dx, dat
    jmp $+2
    in  al,dx                   ; low byte
    mov ah, al
    jmp $+2
    in  al,dx                   ; high byte
    xchg ah,al                  ; Put them in the right order.
;
    stosw                       ; Store the value.
    mov ax, 0
    stosw                       ; Clear out high 16 bits just to be safe.
;
    inc cl                      ; Next counter.
    cmp cx, cntr
    jng SHORT S2                ; Check if done.
;
    retf
;
STORECNT ENDP

END
```