Reliability of Power Electronic Systems in HEV and HVDC Systems

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ABSTRACT

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With wide-spread application of power electronic systems across many different industries, their reliability is being studied extensively. In the dissertation, a mission profile based reliability analysis framework is proposed to quantitatively predict the reliability of power electronic systems. Based on the framework, the reliability of power converters in hybrid electric vehicle (HEV) and voltage source converter (VSC) high voltage direct current (HVDC) power transmission systems is evaluated and the reliability improvement strategies are proposed and verified by simulation and experiment.

Firstly, a general framework of reliability analysis of power electronic systems is presented. The framework is applied to quantitative reliability prediction of key power components, and standard and fault-tolerant power electronic systems in terms of probabilistic or deterministic performance metrics. The reliability evaluation is based on mission profiles for various applications so that the inaccuracy due to the uncertainty of operating conditions of systems can be minimized at the earliest design stage. The strategies to improve the reliability of power electronic system at three possible levels are also systematically analyzed.

Based on the framework of reliability analysis, a mission-profile-dependent simulation model based on MATLAB for quantitatively assessing the reliability of HEVs electric drivetrain is developed. This model takes into consideration the variable driving scenarios, dormant mode, electrical stresses, and thermal stresses. Therefore, more reliable and accurate prediction of system reliability has been achieved. The model is explained in detail and the results of reliability assessment based on a series hybrid electric vehicle (SHEV) are presented.

Reliability analysis results of SHEV provides guidance on improving reliability, two control strategies are proposed to increase the mean time to failure (MTTF) of HEV powertrains: 1) variable dc-link voltage control; 2) hybrid discontinuous pulse-width modulation scheme. These novel

control schemes reduce the power losses and thermal stresses of power converters, and consequently enhance system reliability. Numerical simulation and experimental results verify the benefits of two proposed control strategies in terms of power losses and reliability.

As a safety-critical system, the fault-tolerant operation is desirable for HEVs' power electronic systems. A fault-tolerant power electronic system for series hybrid electric vehicles (SHEVs) is proposed. The introduction of a redundant phase-leg that is shared by three converters in a standard SHEV powertrain allows to maximize the reliability improvement with minimal part-count increase. The new topology features fast response in fault detection and isolation, and post-fault operation at rated power throughput. A scaled-down laboratory prototype has been built and the experimental results further validate the robust fault detection/isolation scheme and uncompromized post-fault performance.

Due to aggregation of thousands of power electronic components, failures of power converters in VSC HVDC systems dominate faults of overall systems. Therefore, the accurate prediction of the reliability of HVDC converters is of great importance for design, reliability improvement, and maintenance management of HVDC systems. The failure rates and MTTF of three types of HVDC converters that are used in commissioned VSC HVDC systems have been comparatively evaluated by use of a mission-profile-dependent reliability simulation model.

As a mission-critical system, the unplanned stoppage of HVDC systems would result in a significant economic loss, therefore the fault-tolerant operation is necessary for HVDC converters. The fault-tolerant designs of the HVDC converters also have been presented and the reliability of the fault-tolerant designs has been assessed by use of Markov reliability model.

My wife, Hong Chen
My son, Ruien Song

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Introduction

1.1 Background

The ever-increasing demand for energy, the shortage of fossil fuels, and concerns over the greenhouse gas emission render energy saving and energy efficiency more important. Power electronics has been widely recognized as an enabling technology for efficient control and conversion of electrical power. By use of switching of solid-state semiconductor devices, power electronic equipment converts raw electrical energy into desired electrical power of various frequencies, voltages, currents and powers [5]. Power electronics plays a critical role in various applications, such as transportation, utility, consumer electronics and lighting, telecommunication, industrial drives, aerospace, and so forth. The important applications of power electronics are reviewed in the following paragraphs.

Power electronics is an enabling technology for the development of electrical, hybrid electrical and plug-in hybrid electrical vehicles (EVs, HEVs, and PHEVs) and their integration into grid. Power converters are crucial part of vehicles' battery management system and drive train. The combination of the internal combustion engine and power converters enables HEVs more energy efficient, potentially achieving almost twice fuel-mileage in comparison with conventional vehicles [6], and substantially reducing tailpipe emission. Although the global production number of

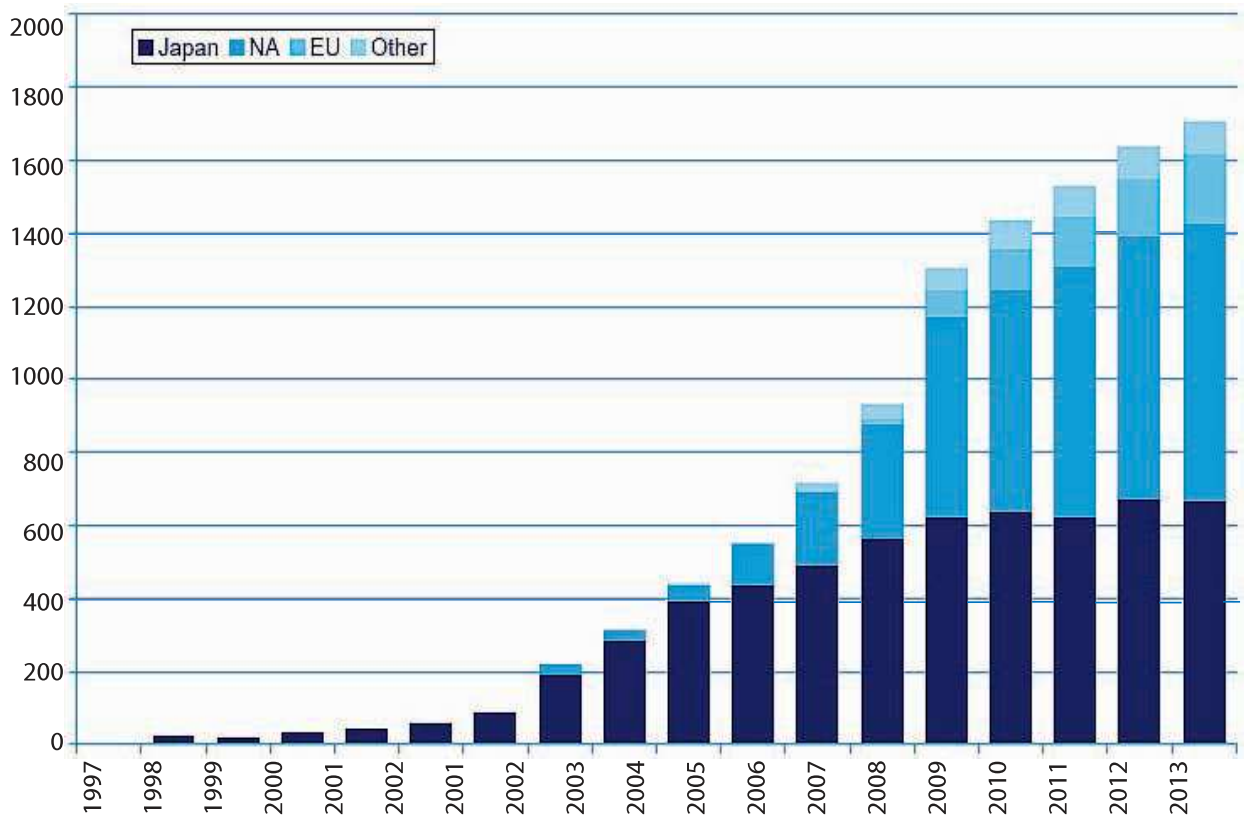
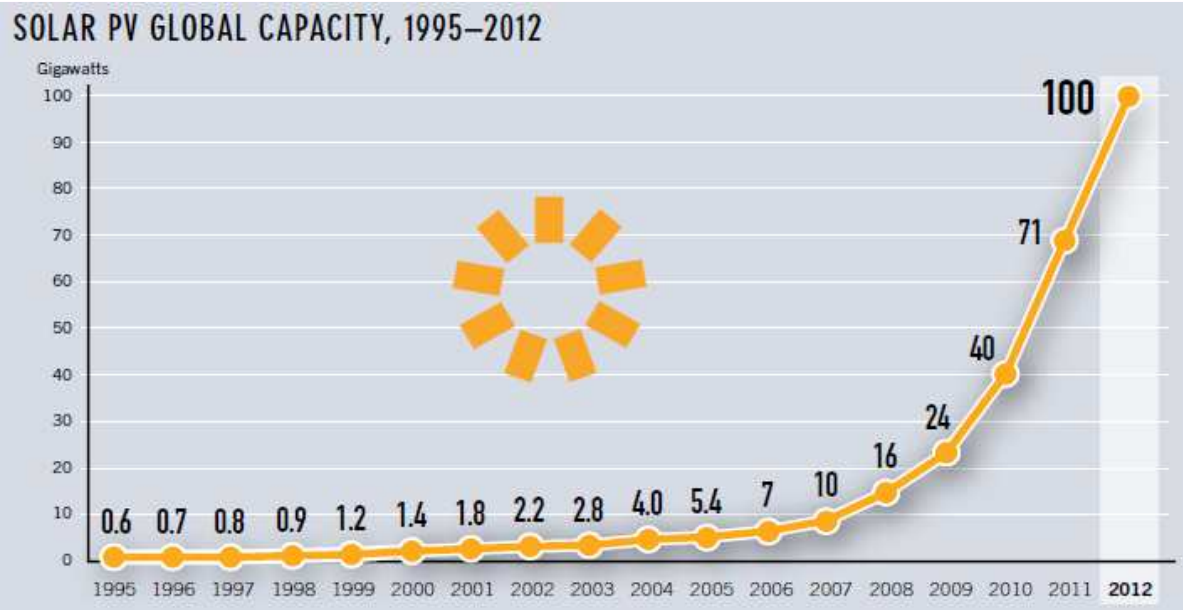


Figure 1.1 Global HEV Assembly During 1997-2014 (Unit: thousand) (Data from UNEP).

HEVs is relatively small when compared to overall fleet, it has been increasing since the first HEV, Toyota Prius, was launched on Japanese market in 1997. According to the 2007 Pricewaterhouse-Coopers outlook, HEV production number is expected to increase to 1.7 million by 2014 [6], as shown in Fig. 1.1.

In addition to hybrid electrical vehicles, the renewable energy generation, such as photovoltaic (PV) generation and wind power, is also an important solution to the energy crisis and environmental pollution. Total global operating capacity of PV systems have reached the 100 GW milestone in 2012 [7], as shown in Figure 1.2. Figure 1.3 illustrates the global wind power capacity during 1996-2012. It can be observed that averaged annual growth rate of the cumulative wind power capacity between 2007 and 2012 is approximately 25%, and by 2012 wind power systems of total 283 GW have been installed.

Rapid development of PV and wind power generation creates a great application field for power



Source: REN21 Renewables 2013 Global Status Report

Figure 1.2 PV global capacity during 1995-2012 (Data sourece: REN21 Renewables 2013 Global Status Report).

electronics technology since power electronics plays a significant role in these renewable generation systems. For wind power generation system, power electronic converters are essential for interfacing wind turbine with the power system by converting raw power generated by wind turbines to stable power compatible with the grid. Power electronic systems also perform power quality regulation, active and reactive power control, and maximum power harvest. In the case of PV systems, power electronics is also the core part that converts the dc power to ac power that is required by the grid and maximize energy capture by PV panels.

Solar farms and wind farms usually are located in remote regions that are rich in solar resource or wind resource and feature low-priced land. Therefore, the renewable-energy power plant are far from the load centers. The long-distance bulk power transmission is necessary. High voltage direct current (HVDC) power transfer possesses noticeable advantages over high voltage alternate current (HVAC) for long-distance or underwater cable power transmission. Voltage source converter (VSC) HVDC systems are developed to link offshore wind farms to onshore power grid. In fact, VSC HVDC is also applied to many fields, such as oil & gas offshore platforms, linkage between

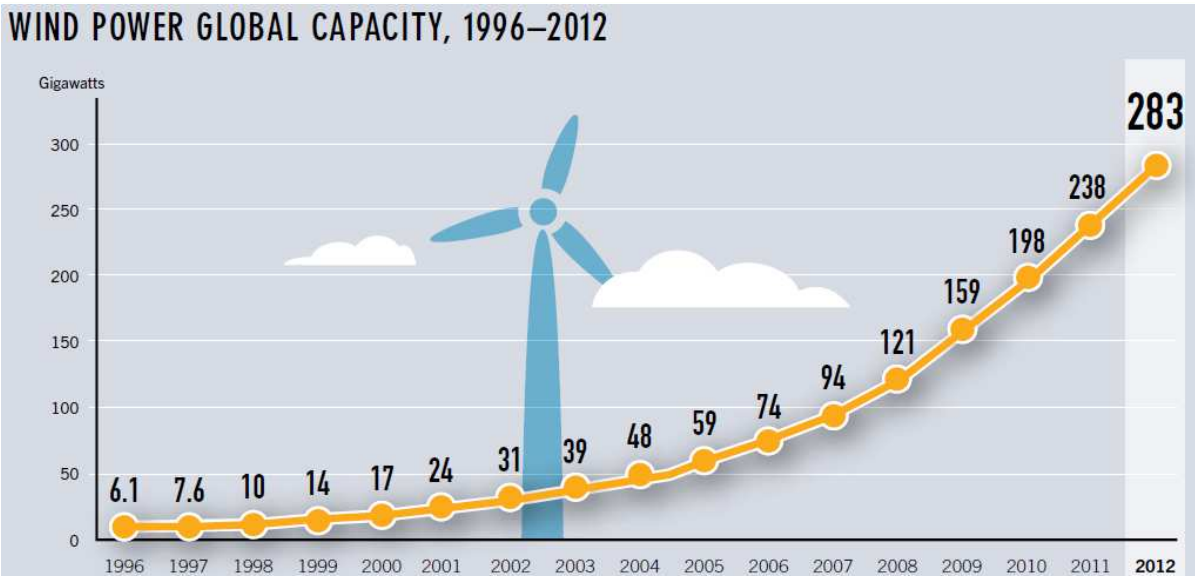


Figure 1.3 Wind power global capacity During 1996-2012 (Data source: REN21 Renewables 2013 Global Status Report).

asynchronous grids, and power delivery to large urban area through underground cables. Power electronics is also core technology of HVDC.

In fact, in addition to the aforementioned significant applications, power electronics gains widespread use in industrial and residential applications. It was forecast that by 2015 power electronics will play a significant role in all sectors of industry [8]. According to estimate of the technology consulting film, Authur D Little, in 2006 power electronics core components market volume would rise to $ 17 billion, and products containing power electronics subsystems would achieve the sales of $ 3 billion, as shown in Figure 1.4.

1.2 Motivation for the Work

The technology based on power electronics provides a compact and efficient solution to power conversion. However, with the increasing applications of power electronics, the issue about the reliability of power electronic systems arises. Introduction of power electronics techniques into these application fields challenges reliability of overall systems. One of the concerns related to

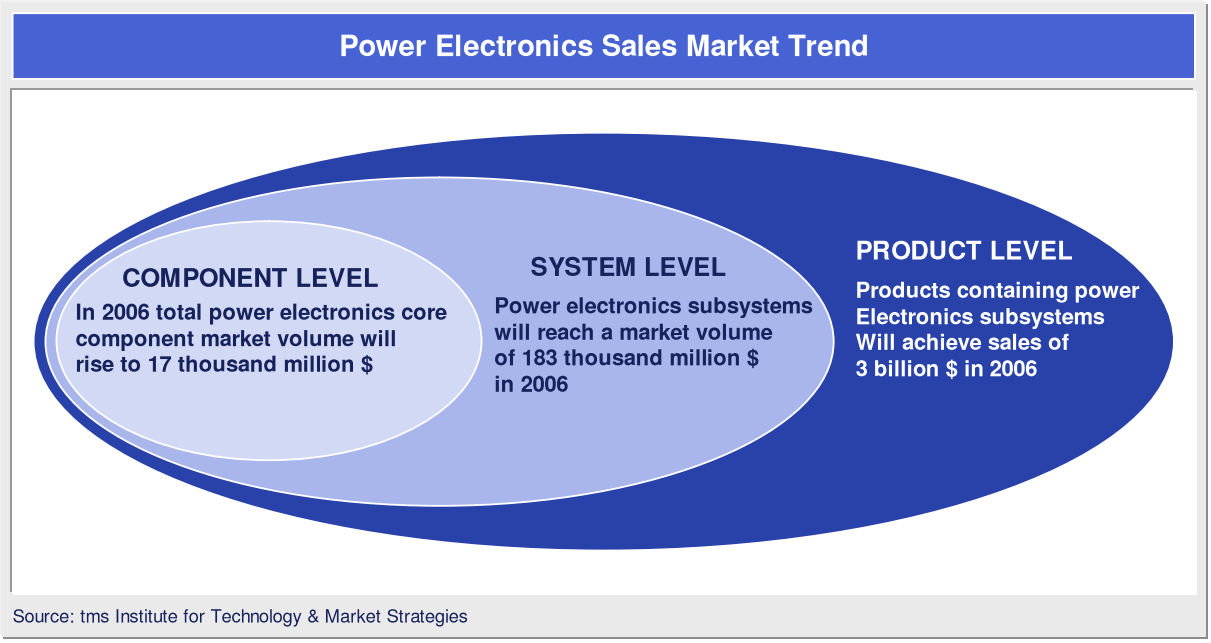


Figure 1.4 Power electronics sales market trend.

reliability lies in the fact that power semiconductor devices are the most vulnerable links [9, 10]. For instance, in photovoltaic (PV) generation systems, the converters are the least reliable components [9]. Field experiences show that PV inverters need to be replaced every 5-10 years while PV modules and other components have the lifetime of over 25 years [9]. According to field statistics of 35,000 downtime events associated with 350 offshore wind turbines, frequency converters contribute to 13% of failure rates and 18% of the downtime [11]. In the case of VSC based HVDC power transmission, an HVDC converter consists of several thousand semiconductor devices that are connected in parallel and/or series [12]. The aggregation of such large number of power devices results in much increased failure rates of the overall system. The field experiences show that the failure rate of the HVDC converters in Corss Sound Cable HVDC system during 2003-2009 is between 7 and 34 failures per year [12]. Therefore, the reliability of power electronic systems are of paramount importance to the reliable operation of overall systems.

Since most of power electronic converters are not equipped with redundancy, any fault that occurs to the components will lead to shut-down of the system. These unscheduled interruptions not only cast significant safety concerns, but also increase system operating cost and offsets the

benefits of introducing power electronic systems. For HEVs, faults that occur in electric drives as propulsion systems of HEVs can be critical since an uncontrolled output torque exerts much risk on the vehicles stability, which could ultimately endanger passengers' safety. Failures of the power electronic system in HEVs not only discounts fuel-saving premium, but also increases repair time and repair cost. In the case of PV and wind power systems, the cost of failure amounts to the value of the energy that would have been generated while the system is down plus the cost of repairing and replacing parts [13]. In particular for solar farms and wind farms that are located in the remote regions, the maintenance is typically time-consuming and expensive. For wind power and HVDC systems, unscheduled outages lead to a tremendous economic loss and even compromise the grid stability.

From above analysis, it can be observed that the reliability of power electronic systems is closely related to the operation and maintenance cost of the overall systems. In fact, the reliability is one of the most important performance metrics of power electronic systems. The reliability analysis includes reliability prediction and reliability improvement with the former being the basis of the latter. The accurate reliability evaluation is a key to reliability analysis. The reliability evaluation can be used for quality management, maintenance management, and engineering design. Maintenance is an effective way of reducing unplanned shutdowns of a system. However, the over-frequent maintenance will lead to high cost while insufficient maintenance will result in lower reliability and increasing forced outages of a system. The accurate quantitative reliability evaluation can be used to optimize maintenance schedule and to strike a balance between maintenance cost and unscheduled stoppages. From the perspective of engineering design, the reliability prediction can be utilized as a provision for comparison and contrast of various candidate configurations, topologies, and control strategies. The reliability evaluation also can pinpoint the least reliable link in the design and provide a guidance for subsequent reliability improvement.

Despite the paramount significance of the accurate reliability evaluation, disproportional research effort has been devoted to reliability analysis of power electronic systems in comparison with the study on topologies, modulation, and control of converters. One of the main reasons is

that accurate reliability prediction is challenged by the lack of accurate reliability data for key power components and uncertainty associated with operating conditions of power electronic systems. Although the reliability prediction of power converters for certain applications has been reported [11, 13–16], a systematic methodology of the reliability evaluation of power electronic system is still unavailable. This thesis proposes a general framework of the reliability evaluation and improvement of the power electronic systems. Therefore, the objective of the thesis is to present a systematic framework for the reliability analysis of power electronics systems and to apply the framework to investigation of the reliability of power electronic systems in HEVs and HVDC systems.

1.3 Reliability Basics

The first step in evaluating and improving system reliability is to determine what metrics to analyze. Because the metrics reflect the design goals, any information that is utilized to determine the metrics shall be based on requirements from customers and careful consideration of intended applications. The commonly adopted metrics for the evaluation of power electronic systems encompass reliability, failure rate, mean time to failure (MTTF), mean time to repair (MTTR), and availability.

1.3.1 Reliability

Reliability is defined as the probability that an item (component, subsystem, or system) performs required functions for an intended period of time under given environmental and operational conditions [17]. The reliability function $R(t)$ represents the probability that the system will operate without failures over a time interval $[0, t]$. The reliability of a system is dependent on the time in consideration. The reliability typically decreases as the time in consideration progresses. For commercial products, the time should cover the warranty time.

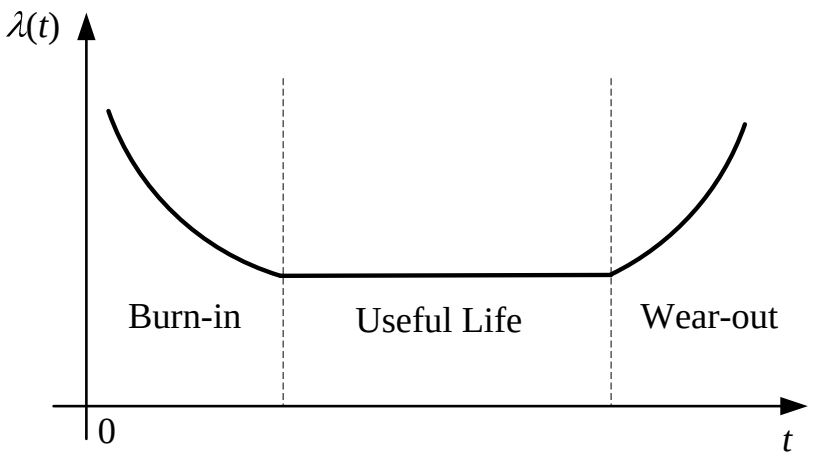


Figure 1.5 A typical failure rate curve as a function of time.

1.3.2 Failure Rate

The failure rate of an item is an indication of the "proneness to failure" of the item after time t has elapsed. Fig. 1.5 shows a typical failure rate curve as a function of time, which is commonly known as the bathtub curve. The shape of the bathtub curve in Fig. 1 suggests that the lifecycle of an item be divided into three different periods: the burn-in period, the useful life period, and the wear-out period. Although an item is subjected to quite extensive test procedure and much of the infant mortality is removed before they are put into use, undiscovered defects in an item during the process of design or production leads to the high failure rate in the burn-in period. When the item survives the initial burn-in period, the failure rate tends to stabilize at a level where it remains relatively constant for a certain period of time before the item begins to wear out. While in wear-out period, systems have finished their required missions. Therefore, the failure rate in useful life time is important for reliability analysis.

The failure rate $\lambda(t)$ is related to the reliability function $R(t)$ by

$$\lambda(t) = \lim_{\Delta t \to 0} \frac{R(t) - R(t + \Delta t)}{R(t) * \Delta t} = -\frac{1}{R(t)} \frac{dR(t)}{dt} \tag{1.1}$$

where Δt is a time interval. The reliability $R(t)$ is determined from the failure rate $\lambda(t)$ with the

consideration of $R(0) = 1$, i.e. the item is fully functional at the initial state,

$$R(t) = e^{-\int_0^t \lambda(\tau)d(\tau)} \tag{1.2}$$

In many reliability models, the failure rates of components and subsystems are assumed independent of time, although this assumption has limitations [17]. With the assumption of $\lambda(t) = \lambda$, (1.2) is simplied to

$$R(t) = e^{-\lambda t} \tag{1.3}$$

The failure rate is then estimated from the mean number of failures per unit time, which is expressed in failures in time(FIT).

$$1\ FIT = 10^{-9}\ failure/hour \tag{1.4}$$

1.3.3 Mean Time to Failure

The MTTF is the expected time before a failure occurs. Unlike reliability, MTTF does not depend on a particular period of time. It gives the average time in which an item operates without failing. MTTF is a widely quoted performance metric for comparison of various system designs. This indicator reflects life distribution of an item. Nonetheless, it does not convey the information that a longer MTTF than the mission time means that the system is highly reliable within mission time. The relationship between MTTF and reliability function is described by

$$MTTF = \int_0^{+\infty} R(t)dt \tag{1.5}$$

where $R(t)$ is the reliability function. When the failure rate $\lambda(t)$ is constant λ, the expression for MTTF is simplified to

$$MTTF = \frac{1}{\lambda} \tag{1.6}$$

1.3.4 Mean Time to Repair

The MTTR is the mean repair time that it takes to eliminate a failure and to restore the system to a specified state. The repair time depends on maintainability, such as effective diagnosis of faults, replaceable components at hand, and so on.

1.3.5 Availability and Average Availability

The availability is the probability that a system will be functioning at a given time. The average availability denotes the mean portion of the time the system is operating over a given period of time. For a repairable system, if it is repaired to an as good as new condition every time it fails, the average availability is

$$Aavg = \frac{MTTF}{MTTF + MTTR} \tag{1.7}$$

Therefore, availability improvement entails increasing MTTF and decreasing MTTR. The main limitation associated with the metric of average availability lies in the fact that it cannot reflect frequency of failures or maintenances required. Hence it is only utilized to assess the repairable systems where the primary concern is availability rather than reliability.

1.4 Scope of the Thesis

The goal of the thesis is to present a methodology for quantitatively predicting the reliability of power electronics systems and to investigate the associated strategies for enhancing the reliability of power electronics systems for some HEVs and HVDC systems. Based on the objective, a lot of research effort has been expanded. The rest of the thesis is organized as follows.

In chapter 2, a framework for reliability analysis of power electronics system is proposed and the associated details of the framework are illustrated.

Chapter 3 assesses the reliability of a series hybrid electrical vehicle (SHEV) powertrain by

use of the model that is presented in Chapter 2, and the detailed analyses are also presented.

Chapter 4 presents two reliability-oriented control strategies for SHEV powertrain based on the reliability analysis and investigation of characteristics of SHEV powertrain.

In Chapter 5 a fault-tolerant design for SHEV powertrain and the associated experimental verification are presented.

In Chapter 6, the failure rates and MTTFs of three types of VSC HVDC converters are evaluated by use of the model that is presented in Chapter 2.

Chapter 7 presents the fault-tolerant designs of the VSC HVDC converters and analyzes the associated reliability of the fault-tolerant HVDC converters.

Chapter 8 concludes the thesis with a summary and discussion on future works.

Chapter 2

A Framework for Reliability Analysis of Power Electronic Systems

In this chapter, a methodology of reliability prediction and improvement of power electronic systems is presented.

2.1 Reliability Evalution of Power Electronic Systems

In this section, a framework for reliability prediction of power electronic systems is presented. The framework constitutes a systematic procedure for quantitatively predicting the reliability performances of various power electronic systems based on specific application requirements.

The proposed framework is illustrated in Fig. 2.1. The reliability evaluation model that is suitable for specific application, such as HEV, PV or wind power generation system, and HVDC converters, can be obtained through slight modifications.

The mission profile that simulates the operating conditions of the power electronic systems is the input data to the general model, and the various reliability measures including failure rate, reliability, lifetime, ans so on, can be obtained from the model. The details of the framework are presented as follows.

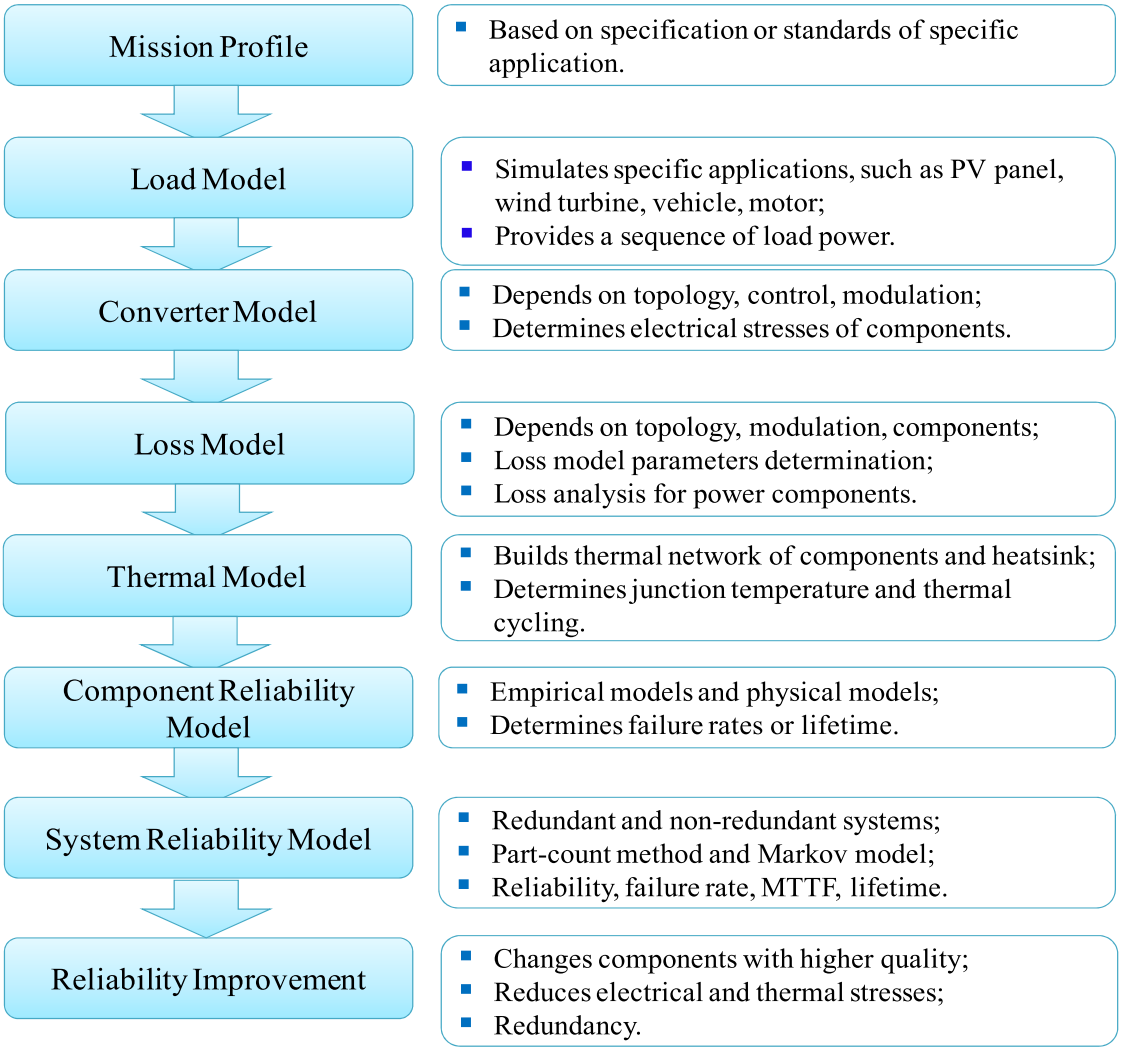


Figure 2.1 A framework of reliability analysis of power electronic systems.

2.1.1 Mission Profile

A mission profile represents the operating conditions of the system from the start to the end of the mission. In the context of power electronics, the mission profile models the typical load variation versus time, and finally determines the electrical stresses of the power electronic system.

The reliability of power electronic systems strongly depends on the electrical and thermal stresses of key power components of the systems, which can be observed from the reliability models to be presented in the following sections. The stresses of components are related to the output requirements of the converter that in turn are determined by the operating conditions of the overall system. For example, the stresses of power components in an HEV's powertrain are dependent upon the traction motor's stator voltages and currents that are further determined by the driver's driving behaviors and road conditions. Uncertainty of driving patterns challenges the prediction of HEVs' operating conditions. Fortunately, various standard driving cycles that are temporal sequences of vehicle speed, such as NEDC, FTP-72, FTP-75, and US06, have been developed in different countries to provide test benchmarks for evaluating efficiency and emission of vehicles. Since these driving cycles have been accepted by the industry and widely used to assess performance of vehicles, they can be employed to emulate the operating patterns of HEVs.

Likewise, for other applications, there are statistical models to simulate the typical load variation within a specific interval, such as solar insolation in a day or wind speed variations in a given interval. These temporal sequences of solar insolation and wind speed can be used as mission profiles of PV and wind power generation systems, respectively, and further used as the benchmarks for the reliability prediction of power electronic systems in PV and wind power applications.

2.1.2 Load Model

Mission profiles would not exclusively determine the electrical stresses of power electronics systems. The electrical stresses of power electronic systems are determined by the load model in conjunction with the mission profile. Herein, the load model is employed to describe the load characteristics of power converters.

For instance, the power electronic system in an HEV's powertrain is utilized to drive a traction motor that directly provides driving torque for the vehicle. Therefore, the motor is the load of the power converters in the drive train. As the driving cycles from the mission profile provide the instantaneous speed and acceleration of the vehicle, they can not exclusively determine the electrical stresses of the power electronic system. In fact, the electrical stresses of power converters are determined by the stator voltages and currents that depend on the torque, speed, and salient characteristics of the motor. The traction torque command is determined by the parameters of the vehicle and the road conditions, such as wind speed, gradient and roughness of the road surface. Therefore, in the case of HEVs, the load model simulates the characteristics of the vehicles and traction motor. The load model determines the instantaneous electrical stresses of power converters in HEV's drive train based on the speed and acceleration obtained from the driving cycle.

For the case of PV generation systems, the load model represents the output characteristics of PV panels. The solar insolation is the input of the load model. The load model can provide terminal voltage and current of the PV panel based on the instantaneous solar insolation obtained from the solar insolation profile. Likewise, for wind power generation systems, the load model represents the characteristics of the wind turbine if the grid voltage remains constant regardless of the variable power injection at the point of common coupling. Therefore, with the input of instantaneous wind speed, the load model outputs the voltage and current profiles for the power converters.

Based on the aforementioned analyses, the function of the load model is to provide voltage and current stresses profiles of power electronic systems by use of the mission profiles.

2.1.3 Converter Model

The electrical stresses of power electronic systems can be obtained from the load model. In order to assess the reliability of power electronics components, the electrical stresses of these components have to be first determined since the reliability depends on the electrical stresses and thermal stresses that are related to components' losses. The converter model is used to compute the power losses of components according to converters' electrical stresses.

The converter model depends on the topology, control strategy, and modulation scheme. An HVDC converter is taken as an example. In the case of same output power and grid voltage, semiconductor devices of the two-level converter have different voltage and current stresses from devices of the three-level converter. In the case of the inverter in the HEV's powertrain, the semiconductor devices experience different voltage stresses for the carrier-based sinusoidal pulse-width modulation and space vector pulse-width modulation.

The converter model provides voltage and current stresses of components in power electronic systems to the following loss model by use of the stresses of converters obtained from the load model.

2.1.4 Loss Model

The loss model is utilized to compute the losses of semiconductor devices based on the current and voltage stresses of the devices that are provided by the converter model. The model parameters of IGBTs and diodes are based on their respective data-sheet values. The calculations are carried out by use of a linear approximation of the device forward voltage drop and switch energy loss [18].

IGBT losses mainly include conduction loss and switching loss since the loss associated with gate drive is much lower and is dissipated in driver circuit. According to [18], the forward voltage drop of IGBT is modeled by a constant component plus a variable component that is the product of the resistance and actual current. The switching energy loss is the sum of all turn-on and turn off energies at the switching events.

The losses of diodes include the conduction loss and reverse recovery loss. Diodes have the similar conduction loss model formula as IGBTs. The reverse recovery loss model of diodes is similar to the switching loss model of IGBTs.

For a specific application, such as the two-level converter or three-level converter, the parameters of devices can be obtained from the data sheets, and the commutation voltage and current can be determined by the dc-link voltages and ac currents. The power losses obtained from the loss model can be used by the thermal model to estimate the junction temperatures of IGBTs and

diodes.

2.1.5 Thermal Model

The thermal model performs two functions: predicting junction temperatures of semiconductor devices and core temperatures of batteries and capacitors, and detecting thermal cycling. The junction temperature and temperature variation of power devices are key factors that affect reliable operation and lifetimes of components, which can be observed from the failure rate models of the devices.

The essence of thermal model is to mathematically describe the thermal transfer system of devices based on various basic heat transfer mechanisms. The simplified dynamic thermal equivalent model of IGBT modules and a cooling system is shown in Fig. 2.2, where P_{IGBT} and P_{diode} represent power losses of the IGBT and diode in a switch, Z_{thJC} denotes the junction-to-case thermal impedance of the IGBT and diode, R_{thCH} is the thermal resistance of the module case to the heatsink, and Z_{thHA} is the thermal impedance of the heatsink to ambient. Herein, in order to take the transient thermal analysis into consideration, the thermal impedance that includes thermal resistance and thermal capacitor rather than only thermal resistance is used. A thin film of silicon compound should be applied to the contact surfaces between heatsink and the case of semiconductor device modules to reduce the contact thermal impedance. Since the thermal capacity of the film of silicon compound is very small and can be neglected, the thermal resistance from the case to heatsink is used.

The device's juction-to-case thermal impedance can be represented by an equivalent partial fraction circuit, as shown in Fig. 2.3. In the thermal circuit, the thermal resistances and capacitances do not represent the physical layer sequences of the IGBT module. The network nodes also do not have any physical significance. The thermal parameters that can be extracted from the measured cooling curve are illustrated as pairs of thermal resistance r and thermal time constant τ in the data sheet of the corresponding device.

The devices' junction temperatures are obtained by use of the analysis of the equivalent ther-

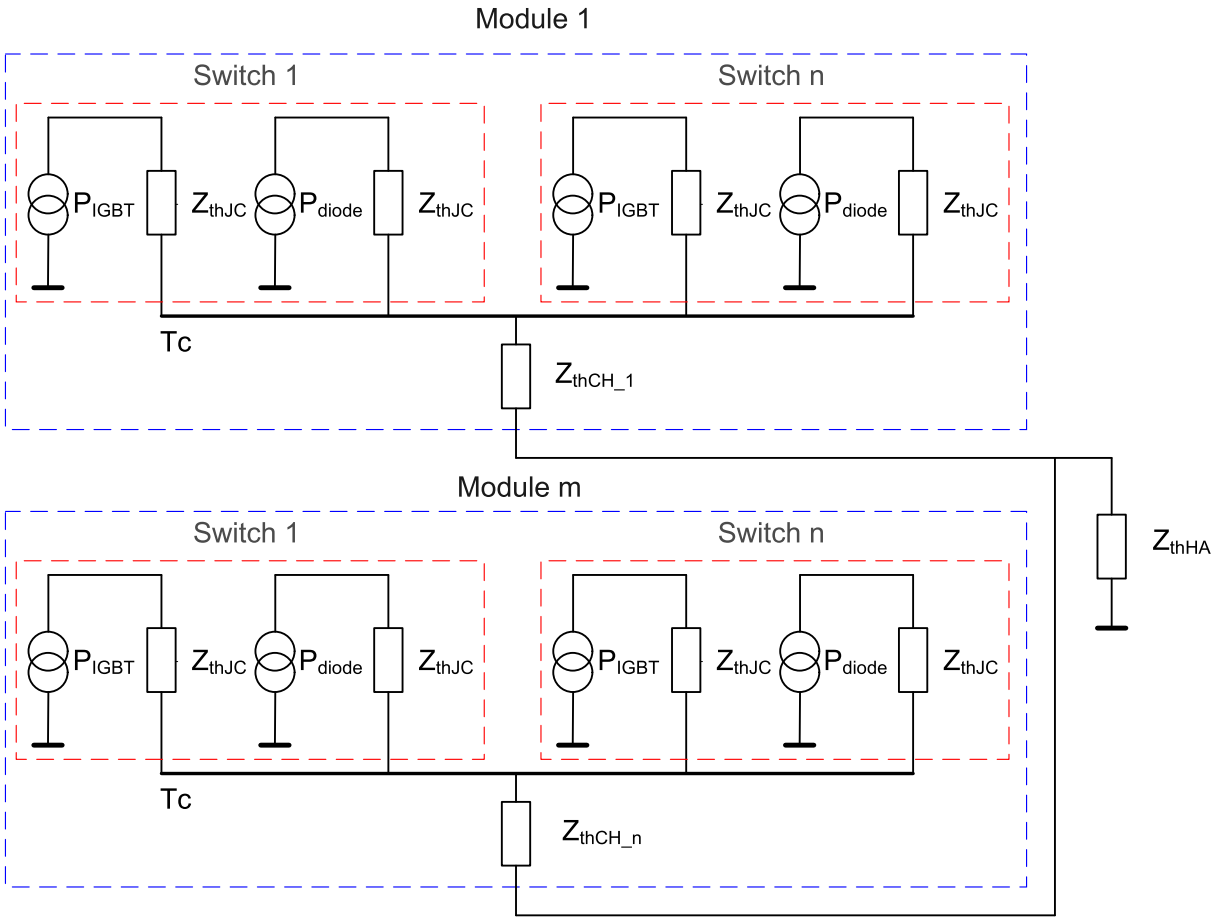


Figure 2.2 Thermal equivalent block diagram of semicondcutor devices and the heatsink.

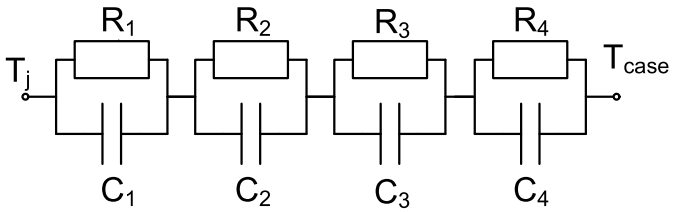


Figure 2.3 The thermal equivalent circuit of a IGBT or diode.

mal circuit, and the temperature cycling also can be calculated. The junction temperature and its variation are fed to the reliability model to evaluate the reliability indices of IGBTs and diodes.

2.1.6 Component Reliability Model

The functional block of the component reliability model is employed to calculate various reliability metrics of power devices by use of the electrical and thermal stresses obtained from the converter model and the thermal model. The reliability models can determine the failure numbers, mean time to failure (MTTF), lifetime and other reliability indices.

There exist two categories of reliability models: empirical models and physical models. These two types of reliability models of IGBTs are presented and analyzed as follows.

Empirical-based reliability models rely on a large amount of field data to quantify model parameters. Based on the empirical-based reliability models, the failure of the devices has the stochastic characteristic. These models can be used to evaluate failure rates and MTTF of power devices.

There are many empirical-based reliability models of power semiconductor devices. The military handbook for the reliability prediction of electronic equipment (Military-Handbook-217F) [2] is well known and widely accepted in military and industrial applications. The failure models that are provided in this handbook represent the relationship between the failure rates of components and various factors, such as types of components, quality, thermal stress, application environments, and so on, as shown in (2.1), which is the failure rate model of MOSFETs.

$$\lambda_{MOSFET} = \lambda_b * \pi_T * \pi_A * \pi_E * \pi_Q \tag{2.1}$$

where λ_b that is determined by the type of MOSFETs is the base failure rate, π_T is determined by the junction temperature, π_A depends on power rating of MOSFETs, π_E is determined by the application environment, and π_Q is the quality factor.

The limitation of the handbook MIL-217F is that it does not contain necessary data to assess

the influence of dormant modes on components, nor the data that reflect effects of thermal cycles. Furthermore, MIL-217F does not contain the failure rate model of IGBT that is the most commonly-used power electronics device. Although the failure model of MOSFETs can be utilized to estimate the failure rates of IGBTs due to the similarity between their internal structures, the accuracy of the result will be challenged. Another important limitation is that the handbook has not been updated since 1995.

The reliability handbook RDF 2000 [19] that was adopted on July 3, 2000 by the UTE (Union Techniques) is another important data source of empirical-based failure rate models. It considers dormant modes, effects of the temperature cycles and data of IGBTs. Herein the component failure rate models provided by RDF 2000 are detailed as follows. The IGBT failure rate can be determined by

$$\begin{cases} \lambda_{IGBT} = \lambda_{die} + \lambda_{package} + \lambda_{overstress} \\ \lambda_{die} = \pi_s * \lambda_0 * \frac{\sum_{i=1}^{y} (\pi_t)_i * \tau_i}{\tau_{on} + \tau_{off}} \\ \lambda_{package} = 2.75 * 10^{-3} * \lambda_b * \sum_{i=1}^{z} (\pi_n)_i * (\triangle T)^{0.68} \\ \lambda_{overstress} = \pi_I * \lambda_{EOS} \end{cases} \tag{2.2}$$

where, λ_{die} that is mainly determined by the junction temperature in the mission profile represents the partial failure rate related to the die of IGBTs, $\lambda_{package}$ denotes IGBT package-related failure rate that is caused by the number and magnitudes of thermal cycles that devices undergo, and $\lambda_{overstress}$, which reflects contribution of the over-current and over-voltage stresses to the total component failure rate, can be neglected since in practical applications the over-stress operating conditions should not occur in normal operating conditions. The unit of the failure rate in the above equation is the number of failures per 10^9 hours.

Failure rate models of diodes have the same form as that of IGBTs. RDF2000 provides the statistical reliability models for other power components, MOSFET, capacitor, battery, and so on.

However, RDF2000 also lags behind the advancement of the technology. For example, the base failure rate λ_b of IGBTs' package depends on the packaging technology. The handbook does not

contain the package base failure data of high power semiconductor modules, such as press-pack IGBT modules. The failure rate models that are provided in RDF2000 also do not include the effects of devices' quality levels on the failures.

Physical reliability models are proposed based on the analysis of component failure mechanisms. In order to use physical models, the model parameters have to be first determined by use of the testing reliability data. The thermal cycles to failure of devices are evaluated. The various analytic lifetime models for IGBTs are explained as follows.

The following analytical lifetime models of IGBTs do not consider the order in which thermal cycles occur. It is assumed that a small thermal cycle has a small effect on the failure of IGBTs no matter whether it occurs before or after a large cycle.

Arrhenius model is one of the commonly used lifetime model to estimate the lifetime of power devices, which is also called power law [20]. According to Arrhenius model, the higher the temperature is, the higher the reaction rate is with an exponential factor. The model can be mathematically expressed as

$$N_f = A * \exp^{(\frac{Q}{R*T})} \tag{2.3}$$

where A is a curve fitting constant, R is the universal gas constant with the value of $8.31 J/(K * mol)$, T is the absolute temperature with the unit K, and Q is the activation energy with the unit J/mol. The activation energy is the minimum energy that is required to start the reaction. In the evaluation of the lifetime of devices, the temperature T is replaced by the mean junction temperature T_m.

The Arrhenius model does not include the effect of the thermal variations on the failure of IGBTs. In order to take the thermal cycling into consideration, a term that describes the effect of the temperature swing with an exponent α is added to Arrhenius model [21], and the modified lifetime model is

$$N_f = A * (\Delta T_j)^{\alpha} * \exp^{(\frac{Q}{R*T})} \tag{2.4}$$

where A is curve fitting constant. The coefficients A and α can be obtained by use of curve

fitting from the data points of the experimental lifetime tests or lifetime curves that manufacturers provide.

The modified model is relatively simple and accurate since it includes the effects of the junction temperature and its variations. However, it does not consider the cycle duration. The relaxation time constant of the solder is in the range of minutes, while the time constant of the bond wire lift-off and the aluminum reconstruction is in the range of seconds [22]. Cycles of certain duration may have an effect on the bond wire lift-off but not on the solder degradation. Longer-duration cycles also have an effect on the solder degradation. Therefore, the cycle time, or the on-time should be considered to accurately assessing the lifetime of devices.

Norris and Landzberg proposed a model that includes the thermal cycle frequency [23], and the model is expressed as

$$N_f = A * f^{\beta} * (\Delta T_j)^{\alpha} * \exp^{(\frac{Q}{R*T})} \tag{2.5}$$

where f is the frequency of the thermal cycles and β is a curve fitting constant.

An extended model based on the analysis of a great number of tests is presented in [24], and the model is described by the following.

$$N_f = A * (\Delta T_j)^{\beta 1} * \exp^{(\frac{\beta_2}{T_{jmax}})} * t_{on}^{\beta 3} * I^{\beta 4} * V_c^{\beta 5} * D^{\beta 6} \tag{2.6}$$

where T_{jmax} is the maximum junction temperature in Kelvin degrees, t_{on} is the pulse duration of the thermal cycles, I is the current per bond foot, V_c is the voltage class, and D is the diameter of the bond wire. A, β_1, β_2, β_3, β_4, β_5, and β_5 are curve fitting constants. The parameters, validity limits and coefficients are listed in Table 2.1. The model is relatively accurate, but the large number of parameters that are needed may limit its applicability.

It should be noted that these lifetime models are analyzed based on wire-bonding IGBT modules. The press-pack IGBT utilizes a different mounting technique, and therefore the failure mech-

Table 2.1 Parameters and Limits for the Calculation of Power Cycles Using the Extended Model [1]

Parameters	Symbol	Unit	Limits	Coefficient	Value	Comment
Technology Factor	A				2.03E+14	Standard
Technology Factor	A				9.34E+14	IGBT4
Temperature difference	ΔT	K	45…150	$\beta 1$	-4.416	
Min. chip temperature	$T_{j(min)}$	°C	20…120	$\beta 2$	1285	
Pulse duration	t_{on}	s	1…15	$\beta 3$	-0.463	
Current per bond foot	I_B	A	3…23	$\beta 4$	-0.716	
Voltage class/100	V_C	V	6…33	$\beta 5$	-0.761	
Bond wire diameter	D	µm	75…500	$\beta 6$	-0.5	

anisms are different from those of wire-bonding IGBTs.

2.1.7 System Reliability Model

In the case that the reliability of components are determined, the reliability of power electronic systems can be evaluated. A system-level reliability model presents a clear picture of functional interdependence amongst components or subsystems and provides a framework of developing quantitative reliability estimates of systems to guide the design trade-off process. There are three types of system-level reliability models, part-count methods, combinatorial models, and state-space models. These are analyzed as follows.

Part-count method is suitable for non-redundant systems that feature: i) any fault that occurs to each of the components or subsystems will cause the overall systems to fail; ii) at component level, the failure rates of individual components are assumed constant during their useful life time; iii) the system is functionally treated as a series-connected structure of all components or subsystems.

For a series structure with n subsystems as shown in Fig. 2.4, the i^{th} subsystem has failure rate λ_i, and the failure rate λ of the overall system is determined by

$$\lambda = \sum_{i=1}^{n} \lambda_i \tag{2.7}$$

The main advantage of part-count method lies in its simplicity. A part-count model can provide

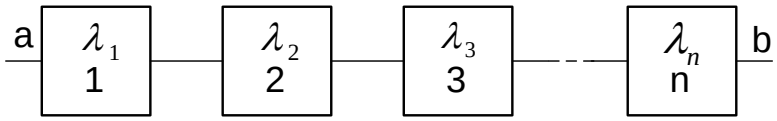


Figure 2.4 An illustration of a series conguration with n subsystems.

adequate reliability estimation for small systems. The part-count method is often adopted to power electronic converters that are not equipped with redundancy. It is also an effective approach to reliability comparison among different power electronic system architectures at the every early design stage. However, for the systems that can tolerate some failures or that can be repaired, this approach leads to over conservative results.

Combinatorial models are extensions to part-count models and are categorized into fault trees, success trees and reliability blocks diagrams. These methods can be used to analyze reliability of simple redundant systems with perfect coverage. Unfortunately, combinatorial models cannot reflect the details of fault-tolerant systems, such as repair process, imperfect coverage, state-dependent failure rates, order of component failures, and reconfiguration.

Markov model is based on graphical representation of system states that correspond to system configurations, which are reached after a unique sequence of component failures and transitions among these states. The system is said in failure-free state when all components are non-faulted. The system can evolve from a failure-free state to other states when faults occur to corresponding components. There are two types of states in Markov models: i) absorbing states that are associated with failed system configurations, and ii) non-absorbing states that correspond to configurations in which the system can deliver full or partial functionalities.

At the system level, Markov chain is an effective approach to evaluating the reliability of fault-tolerant systems. This approach can cover many features of redundant systems, such as sequence of failures, failure coverage, and state-dependent failure rates. Markov model can be utilized to estimate various reliability metrics such as failure rate, $MTTF$, reliability, and availability among others. Firstly, a stochastic state variable $\{X(t),\ t > 0\}$ is defined, which represents state of the

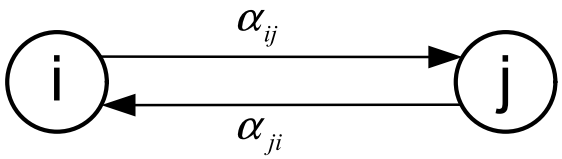


Figure 2.5 State transition diagram.

system. At time t, the probability $P_i(t)$ of the system being in the i^{th} state is expressed as

$$P_i(t) = P\{X(t) = i\} \tag{2.8}$$

If the system is in the i^{th} state at time t, the probability that the system transitions to the j^{th} state after an interval Δt is

$$P_{ij}(t) = P\{X(t + \Delta t) = j | X(t) = i\} \tag{2.9}$$

The transition rate α_{ij} that denotes the probability of system transitioning from state i to state j during the interval Δt is determined by

$$\alpha_{ij} = \lim_{\Delta t \to 0} \frac{P_{ij}(t)}{\Delta t} \tag{2.10}$$

Transition rates of the fault-tolerant system are analogous to the failure rates and repair rates of non-redundant systems. The transition amongst different states of a system is caused by failure and repair events of components. Fig. 2.5 illustrates the state transition diagram for a simple two-state case. If a system has k states, then the state equation is given by (2.11) [17].

$$\frac{d}{dt}\begin{bmatrix} P_0(t) \\ P_1(t) \\ \vdots \\ P_k(t) \end{bmatrix} = \begin{bmatrix} -\alpha_{00} & \alpha_{1,0} & \cdots & \alpha_{k,0} \\ \alpha_{01} & -\alpha_{11} & \cdots & \alpha_{k1} \\ \vdots & \vdots & \cdots & \vdots \\ \alpha_{0k} & \alpha_{1k} & \cdots & -\alpha_{kk} \end{bmatrix} \begin{bmatrix} P_0(t) \\ P_1(t) \\ \vdots \\ P_k(t) \end{bmatrix} \tag{2.11}$$

where the diagonal elements are

$$\alpha_{ii} = \sum_{j=0, j\neq i}^{k} \alpha_{ij} \tag{2.12}$$

The probabilities that the system is in each state at time t is then obtained by solving (2.11). Probabilities $P_0(t)$, $P_1(t)$, ..., $P_m(t)$, correspond to normal or degraded states 0, 1, ..., m, while probabilities $P_{m+1}(t)$, $P_{m+2}(t)$, ..., $P_k(t)$ correspond to failed states $m+1$, $m+2$, ..., k. The reliability function of the system is the sum of the probability functions of all functional (non-failed) states.

$$R(t) = \sum_{i=0}^{m} P_i(t) \tag{2.13}$$

The various reliability measures, such as reliability, MTTF, failure rate, for power electronics systems can be determined by use of the system-level reliability model.

2.2 Reliability Improvement of Power Electronic Systems

A framework of reliability evaluation of power electronic systems has been presented in Section 2.1. As a significant performance metric, reliability has to be improved if the initial design cannot meet the requirement. Therefore, the reliability evaluation and design of power electronic systems is a recursive process. Reliability evaluation also facilitates the identification of the dominant components or mechanisms that result in failures of a system. In this section, three common methods of improving reliability of power electronic systems are presented.

2.2.1 Changing Component Quality Level

The component quality level exerts a significant influence on the reliability of components. The failure rate models that are provided in MIL-217F take the component quality into accountant by the factor π_Q in (2.1). Table 2.2 lists the quality factor of MOSFETs with various quality levels. It can be observed that π_Q of components with the quality level $Lower$ is ten times as much as that of components with the quality level $JANTXV$. Therefore, replacing the components with

Table 2.2 Quality Factor of MOSFETs [2]

Quality Level	Quality Factor π_Q
JANTXV	0.5
JANTX	1.0
JAN	2.0
Lower	5.0

ones of higher quality levels is an effective way of improving the reliability of power electronic systems.

However, JAN, $JANTX$, and $JANTXV$ are military component standards. Components for military applications are much more expensive than components for commercial applications. In addition to the cost, some components with the quality levels of three military standards are unavailable. Therefore, the reliability improvement by use of components with higher quality levels are limited by the cost and availability of components.

2.2.2 Reducing Electrical and Thermal Stresses

The failure rates of semiconductor devices also depend on the electrical stresses and thermal stresses. For example, according to the reliability model of IGBTs that is provided in RDF2000, the failure rate of IGBTs' dies is determined by the voltage stress factor π_S and temperature factor π_t, as shown in (2.2).

The failure rate of IGBTs depends on the collector and gate voltage stresses. The collector voltage stress $S1$ is defined as the ratio between the maximum repetitively applied collector voltage V_C and the rated collector voltage V_{Cr}, as shown in (2.14).

$$S1 = \frac{V_C}{V_{Cr}} \tag{2.14}$$

The gate voltage stress $S2$ is defined as the ratio between the maximum repetitively applied gate

voltage V_{ge} and the maximum rated gate voltage V_{ger}, as shown in (2.15).

$$S1 = \frac{Vge}{Vger} \tag{2.15}$$

The corresponding voltage stresses factor are shown in Fig. 2.6 [19]. The total voltage stress factor π_S is equal to the product of π_{S1} and π_{S2}.

$$\pi_S = \pi_{S1} * \pi_{S2} \tag{2.16}$$

It can be observed that the voltage stress factors can be reduced by decreasing the voltage stresses. However, since the too low gate voltage results in much higher voltage drop across IGBTs, the freedom of reducing the gate voltage stress is very limited. Reduction in the collector voltage stress leads to increase in the equivalent silicon area that is related to the cost, and too low collector voltage stress also reduces electrical performance of converters. Therefore, improving the reliability of power electronic systems by reducing the electrical stresses is constrained by the cost and performances of systems.

Thermal stresses also influence failures of components. As shown in (2.2), the failure rate of IGBT's die is in proportion with the temperature factor π_t that is determined by the temperature of the IGBT junction. From Fig. 2.7(a), it can be observed that the temperature factor π_t can be reduced by two thirds as the junction temperature decreases to 50 $^{\circ}$C from 150 $^{\circ}$C and consequently the failure rate of the IGBT' die also can be greatly reduced. The junction temperature is determined by the power loss of a device and the associated cooling system. Therefore, enhancing thermal management and reducing power losses of semiconductor devices are effective solutions to improving reliability of power electronic systems [25].

Failures of chips inside power semiconductor devices depend on the junction temperature while failures of semiconductor devices' packages depend on the temperature variations that devices' junctions experience in a given period of time of interest. From (2.2), it is evident that the failure rate of IGBTs' packages is closely related with ΔT, the amplitude of thermal cycles and the

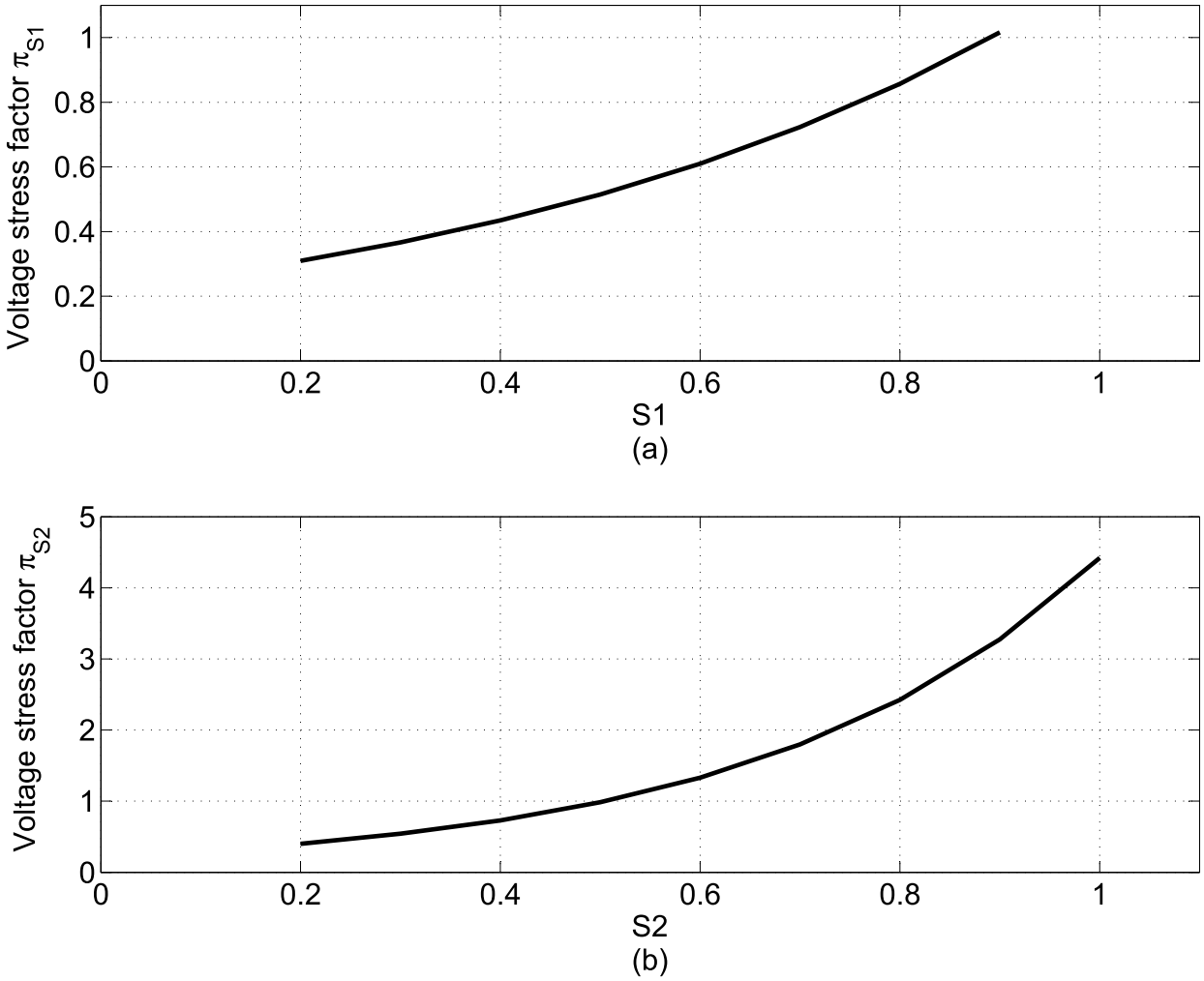


Figure 2.6 Voltage stress factors for IGBTs: (a) collector voltage stress factor π_{S1}; (b) gate voltage stress factor π_{S2}.

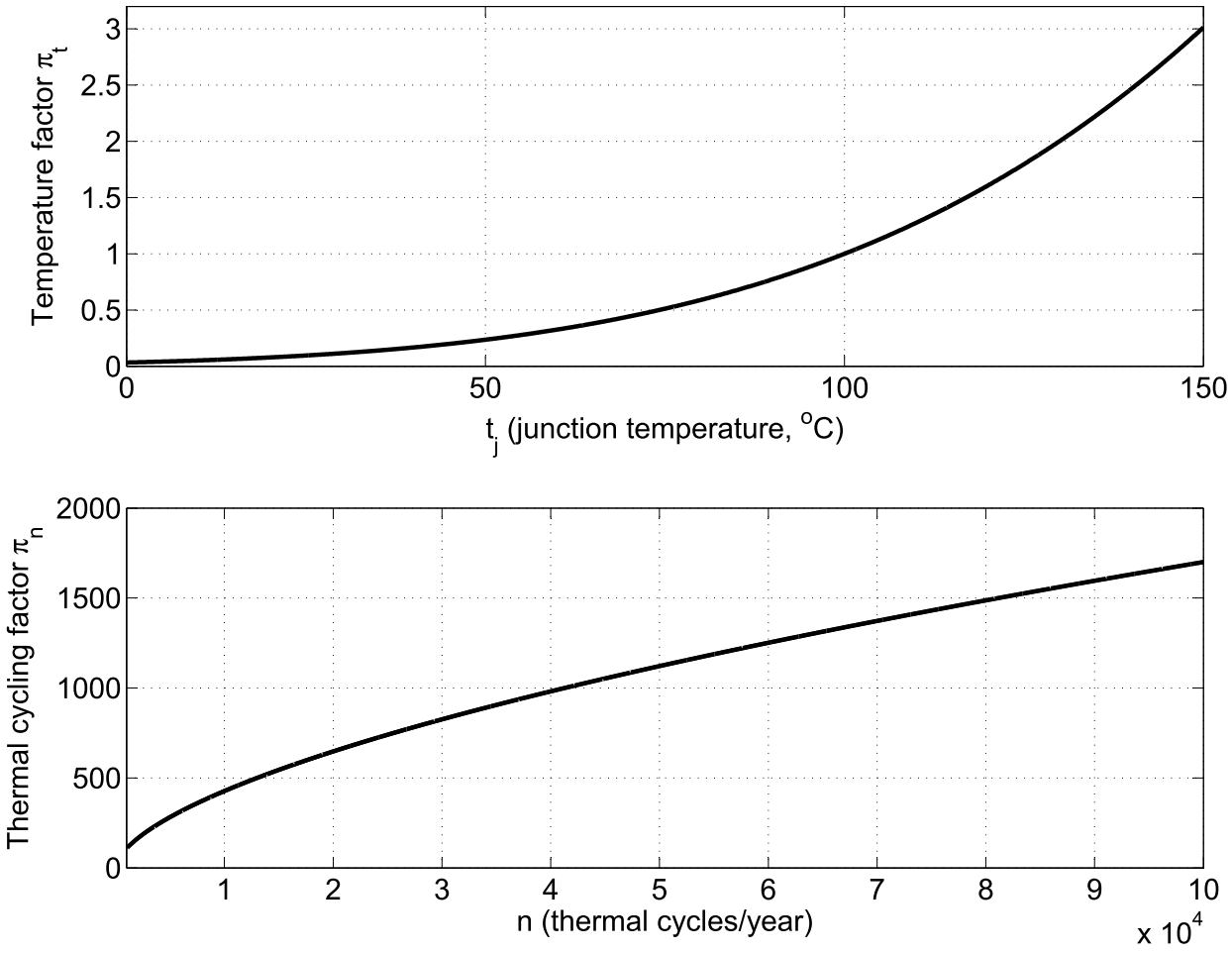


Figure 2.7 Factors in reliability model of IGBTs: (a) temperature factor π_t; (b) thermal cycling factor π_n.

influence factor π_n that is determined by the annual number of thermal cycles with the amplitude ΔT. Fig. 2.7(b) shows the profile of the influence factor π_n versus the annual number n of thermal cycles. It can be observed that the influence factor π_n can be greatly reduced when the number of thermal cycles decreases. Therefore, failure rates of semiconductor devices and converters can be reduced by lowering the number of thermal cycles or decreasing amplitudes of thermal cycles [26].

2.2.3 Redundancy

In addition to replacing components with high-quality ones and reducing the electrical and thermal stresses of components, equipping the design with redundancy is an effective method of improving reliability of systems, in particular for mission-critical systems. The significant benefit of the redundancy is to enable the fault-tolerant capability of a system and improve MTTFs and availability of a system. The realization of the fault-tolerance requires four important elements: redundancy, fault detection, fault isolation, and on-line repair [27]. For power electronic systems, the redundancy can be implemented by use of software and/or hardware approaches. The details of redundant power electronic systems are elaborated in the following paragraphs.

2.2.3.1 Software-Based Redundancy

The prerequisite of the software-level redundancy is availability of systems' inherent hardware redundancy. The redundancy can be realized by changing software-based control algorithms to utilize the inherent redundant states of systems without modification of hardware. For instance, for the open-switch fault of the two-level three-phase inverter that is applied as motor drives, by changing the software-based control strategies, the inverter can be reconfigured into a two-phase inverter and the electromagnetic torque of the motor remains unchanged [28]. The three-phase three-level converter has inherent redundant switching states and consequently for faults of some switches, the balanced post-fault output voltages can be maintained by use of the redundant switching states [29]. For other instance, an H-bridge multilevel converter may consist of a large number of H-bridge cells while a modular multilevel converter consists of a series of half-bridge cells. Their redundancy is feasible to be implemented by use of the software-based method. As a fault occurs to a cell, the faulted cell is bypassed, and the balanced output voltages can be maintained by raising the dc-link voltage of cells or by injecting zero-sequence components [30].

The paramount advantage of the software-based redundancy is that the fault-tolerant capability of systems can be realized and the reliability can be improved without incurring the cost associated with additional components. The drawback lies in the fact that the post-fault performances

of power converters are typically degraded, such as reduced achievable output voltage and output power, increased harmonic distortion, and increased components' electrical and thermal stresses. The application of the software-based redundancy is also limited by availability of power converters' inherent redundant states. The software-based redundancy generally cannot be applied to switching mode power supplies due to unavailability of inherent redundancy.

2.2.3.2 Hardware-Based Redundancy

In comparison to the software-based redundancy, the hardware-based redundancy is more flexible and can be applied to various power electronic systems since it can be implemented at the system level, subsystem level, and component level. The $N + m$ design rule is utilized in the hardware-based redundancy. Herein, N denotes the number of systems, subsystems or components are necessary to perform normal operation. m denotes the number of extra systems, subsystems, or components that are added to realize the redundancy of power electronic systems. Therefore, until $m + 1$ systems, subsystems or components fail, will the overall system continue functioning. The selection of N depends on the electrical requirements of power electronic systems while the selection of m is determined by the reliability requirements.

In the field of power electronics, the system-level redundant design has been applied to switching mode power supplies to power mission-critical equipment [31]. The redundant power system can increase availability by several orders of magnitude over a non-redundant system [27]. A power supply with MTTF of 500,000 hours and MTTR of 4 hours is taken as an example. In the case of non redundant design as shown in Fig. 2.8(a), the unavailability is 252.5 ms/year. When the power supply is designed as $1 + 1$ redundant system as shown in Fig. 2.8(b), the unavailability of the system is reduced to 2.02 ms/year. The unavailability of the system is greatly reduced by adding system redundancy with the price of doubled cost. The system-level redundancy is easy to be implemented since simple fault identification and isolation circuit can be used.

Although the system-level reliability greatly improves the reliability of power electronic systems, the cost of the overall system has to be doubled. As the power level increases, the benefits

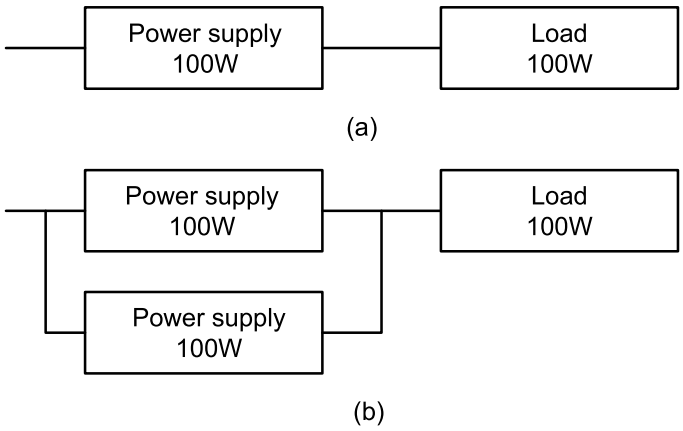


Figure 2.8 (a) non-redundant power system; (b) $1 + 1$ redundant power system.

that the system redundancy brings in may be offset by the extra cost of the redundant system and therefore system-level redundancy becomes unacceptable. The subsystem-level redundancy is more attractive in high-power applications. For example, a redundant leg and associated auxiliary components can be added to the H-bridge converter to provide redundancy [32]. Fault-tolerant capability of all phase legs can be obtained by minimal cost increase. For H-bridge multilevel and modular multilevel converters, the redundancy can be implemented at the cell (subsystem) level. Insertion of extra cell into each phase leg or arm can realize the redundancy of the converters [30]. In comparison with the system-level redundancy, the subsystem-level redundancy involves lighter cost burden and less reliability improvement. It is worth noting that implementation of subsystem-level redundancy involves complex or costly fault identification and isolation components.

The press-pack packaging technology enables the component-level redundant design of power electronic systems since press-pack devices are certain to fail in short-circuit mode and the failed devices still conduct the rated current with an acceptable voltage drop. For high-voltage high-power applications, such as HVDC and flexible ac transmission system (FACTS), high voltage drives, wind-power generation systems, and so on, in each switch position of the two-level or three-level converter, the series connection of IGBT modules is necessary to deliver high voltage blocking capability [12]. The $N + m$ rule can be applied to the converter design at the component level. Herein, the requirement of the low failure rate of each switch position drives the choice of N

to the smallest possible number. The degree of redundancy m is chosen according to requirement of reliability. Large m improves the reliability of converters but increases cost and complexity of the converters. In the field of power electronics, the component-level redundancy is suitable for press-pack device based converters since auxiliary fault-isolation components are unnecessary. Otherwise, a large number of additional fault isolation components will result in a costly and complicated system.

2.3 Summary

In this chapter, a general framework of quantitative reliability prediction of power electronic systems for various applications has been proposed. In this framework, the mission profile for a certain application is used to determine the operating conditions of power converters and further to determine electrical and thermal stresses of power components. By choosing appropriate reliability models, the probabilistic or deterministic reliability metrics for power components can be predicted. At the system level, part-count method and Markov model are applied to the reliability evaluation of standard and fault-tolerant power electronic systems, respectively. The reliability evaluation results can be utilized as a performance metric for the selection of various designs, and provide a guidance on reliability improvement. Three commonly-used methods of improving reliability of power electronic systems are analyzed. According to specific application, these three strategies can be used to improve the reliability of converters.

Chapter 3

Reliability Evaluation for HEV's Powertrain

In Chapter 2, a framework for reliability prediction of power electronics systems has been proposed. Based on the framework, in this chapter, the reliability of the power electronics system for a series hybrid electrical vehicle (SHEV) powertrain is evaluated.

3.1 Introduction

Hybrid electric vehicles (HEVs) with their superior fuel economy have been considered as a pivotal technology to mitigate concerns over the rapid rising of petroleum cost, increasingly worsening air pollution and global warming associated with greenhouse gas emission [33]. However, integration of a great number of power electronic devices into drive systems of vehicles could adversely impact reliability of the overall system [34]. The reduced reliability of HEVs not only discounts fuel-saving premium, but also increases operating cost. Therefore, the reliability of HEVs powertrain has increasingly attracted research attention from both academia and industry. Research activities on the reliability of components, power electronic converters and the whole drivetrain for HEVs from the probabilistic and deterministic perspectives have been reported in literature [35]. From the component point of view, battery is the most important and also the least reliable component

in HEVs, which has a crucial effect on the reliability and cost of HEVs. The authors of [36] study the influence of the operating temperature on the cycle life of lead-acid, lithium-ion and nickel-metal hydride (NiMH) batteries for HEVs based on simulation. The reliability of power electronic converters in HEVs is also widely investigated. The reliability of a bidirectional dc/dc converter for the energy storage system of HEVs is assessed in [37]. In this chapter the driving behaviors are taken into account and the failure rate models of the components are obtained by use of Monte Carlo simulation. But the reliability models introduced by the authors do not include effects of thermal cycling on component failures, which will lead to the results that may substantially deviate from reality. A test bench implemented with various driving cycles to verify the reliability of new prototypes of inverters for electric motors in hybrid vehicles is presented in [38]. Authors of [39] presents a simulation concept that is used to assess the lifetime of the inverter for HEVs in terms of the speed of crack propagation for bond and solder joint connections. Hirschmann, et al. present a simulation model to predict the reliability of inverters in HEVs [40]. This reliability model focuses on the effects of temperature and thermal cycle on the failure rates of key power components of inverters. A reliability model based on a sequence tree is adopted to analyze various reliability indices and related maintenance cost of the powertrain within a fuel cell car [41]. The authors of [42] evaluate and compare the availability of pure electric vehicles, hybrid electric vehicles, and conventional vehicles based on part-count reliability model. This method does not consider the practical driving scenarios and operating conditions of vehicles.

In order to overcome the limitations of the existing methods, a reliability model based on the framework proposed in Chapter 2 is presented to predict the reliability of power electronic system of hybrid electric vehicles. The practical scenarios, thermal stresses and electrical stresses are considered in the model.

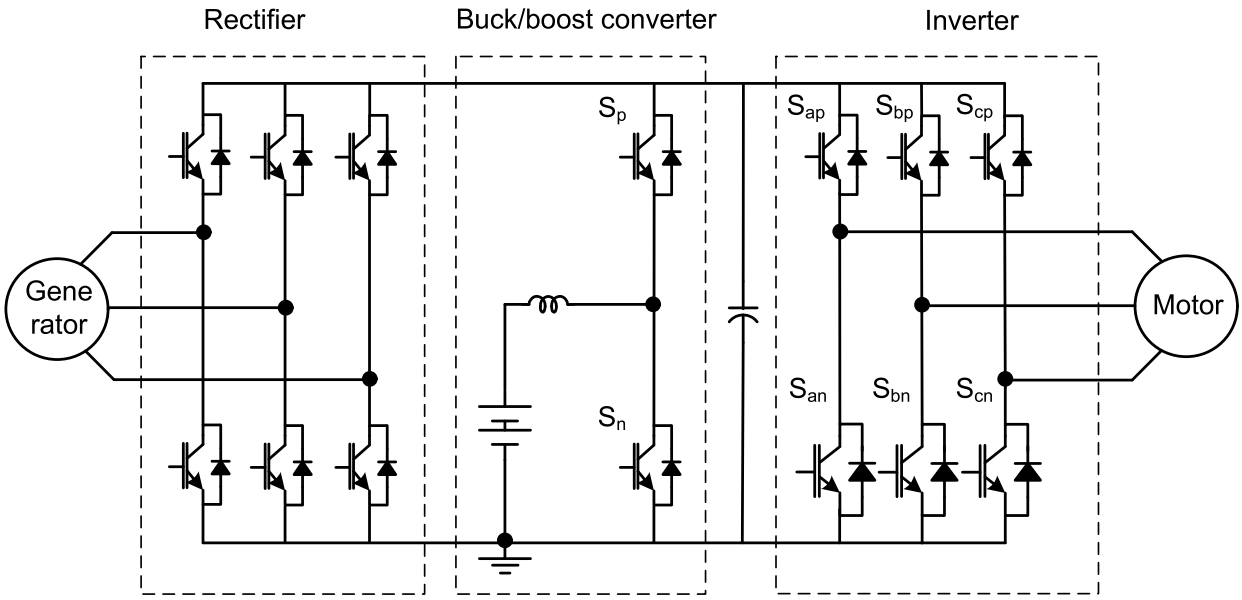


Figure 3.1 Schematic of the SHEV powertrain.

3.2 Series Hybrid Electric Vehicle Powertrain

Prior to evaluating the reliability of the SHEV's power electronic system, the SHEV's powertrain is briefly introduced. As shown in Fig. 3.1, an SHEV power system consists of three power converters, a three-phase pulse width modulated (PWM) rectifier, a three-phase inverter and a bidirectional dc/dc converter, and energy storage unit that is composed of battery cells connected in parallel and series manners. Since there are two energy sources, the traction power will be divided between the engine and the battery bank in accordance with the specific energy management strategy, driving conditions, and state of charge of the battery pack. Correspondingly there are five operating modes for SHEVs, and the operating conditions of the power converters and the battery bank are different from each mode to others. As a result, the electrical and thermal stresses of components in SHEVs greatly vary during a driving cycle, which will be considered in the reliability analysis model presented in the next section.

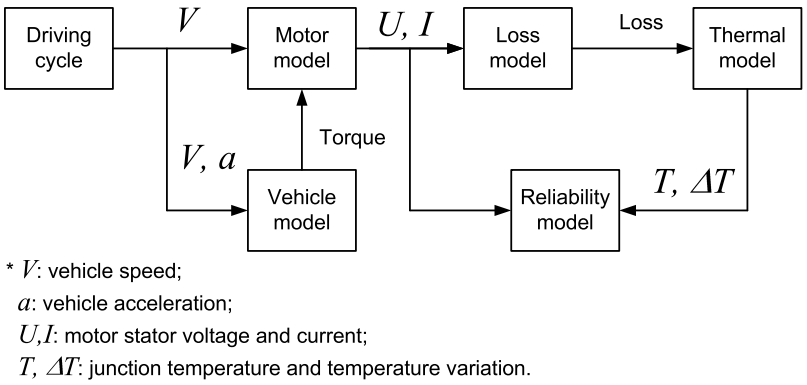


Figure 3.2 The diagram of the reliability simulation model.

3.3 Reliability Simulation Model of SHEVs

In this section, a reliability simulation model that is based on the framework for reliability evaluation of power electronic systems presented in Chapter 2 is built to evaluate various reliability metrics of SHEVs. The model takes various operating conditions of SHEVs into consideration. The structure of the reliability simulation model is shown in Fig. 3.2. In this model, the input data are the operating conditions of vehicles. Herein, various standard driving cycles are used to simulate the driving scenarios. The failure rates and mean time to failure (MTTF), lifetime and other reliability indices of the components, converters and the whole system can be obtained from the model. Each functional block will be introduced as follows.

3.3.1 Driving cycle

The first function block "Driving cycle" is used to simulate various driving cycles that represent standard temporal sequences of vehicle speeds and finally determine load profiles of HEVs. Herein, the various diving cycles are employed to model the mission profile of HEVs. The torque-speed characteristics of vehicles versus time determine the operating conditions of the power electronic converters in the drive system, which finally affect the electrical and thermal stresses of the key power components. However, the torque-speed profiles of vehicles depend on the behaviors of drivers and the road conditions. Uncertainty of driving patterns challenges the reliability predic-

tion of HEVs. Fortunately, various driving cycles that are temporal sequences of speeds, such as NEDC, FTP-72, FTP-75, US06, and so on, have been developed in different countries to provide a test benchmark for evaluating efficiency and emission of vehicles. Since these driving cycles have been accepted by the industry and widely used to assess performance of vehicles, herein they are employed to emulate the operating patterns of HEVs. The driving cycle provides the instantaneous speed V and acceleration a to motor model and vehicle model, as shown in Fig. 3.2.

3.3.2 Vehicle Model

In the function block of vehicle model, the vehicle speed and acceleration that are obtained from the driving cycle model are utilized to calculate the instantaneous traction torque and mechanical speed of the traction motor. The instantaneous speed and acceleration will not be able to exclusively determine the instantaneous electrical stresses of vehicles' powertrain. The specific electrical stresses also depend on the parameters of vehicles and the road conditions, such as wind speed, gradient and roughness of the road surface. The parameters of HEV and assumed road conditions not only determine the power ratings of energy sources and power electronic converters, but also determine their instantaneous powers [33]. The parameters of the vehicle, such as vehicle weight, front area, and diameter of wheels, are obtained from the commercial vehicle Toyota Prius. Rolling resistance coefficient, aerodynamic drag coefficient and transmission efficiency that are indispensable parameters for traction force analysis are obtained from literature [33]. These parameters have been tabulated in Table 3.1. The traction torque and the motor speed that are obtained from this vehicle model are served as inputs of the motor model.

3.3.3 Motor Model

The motor model simulates the steady-state operation of the traction motor and is used to compute the stator voltage and current by use of the traction torque and the rotor speed that are obtained from the vehicle model.The sizing of the traction motor in SHEVs is based on performance requirements of vehicle that mainly include maximum speed, acceleration and gradiability, vehicle's parameters

Table 3.1 Parameters Assumed of Vehicle

Parameter	Value
Vehicle weight	1243 kg
Front area	1.746 m^2
Rolling resistance coefficient	0.01
Aerodynamic drag coefficient	0.26
Diameter of tire	0.62 m
Transmission efficiency	0.9

Table 3.2 Power Ratings of the SHEV Powertrain

Parameter	Value
Traction motor	67 kW, base speed 1200 RPM, maximum speed 6000 RPM
Engine/generator power rating	33 kW
Inverter power rating	$V_{ll} = 400$ V, $I = 162$ A
Rectifier power rating	32 kW
Dc/dc convertere	49 kW
Battery pack	49 kW, 4.9 kWh

and the road conditions. The specific design process and methodology is detailed in [33]. The motor's power rating is illustrated in Table 3.2. Herein the interior permanent magnet motor (IPM) is utilized as the traction motor and its model is developed to calculate the instantaneous stator current and voltage by using known torque and speed. The simulation model is based on the steady-state model of IPMs [43]. The IPM's operating modes, such as maximum torque per ampere, fluxing weakening, are also considered in this model to simulate practical operating conditions. The stator voltage and current from the motor model directly determine the operating conditions of power converters in HEV's drive system.

3.3.4 Loss Model

The stator voltage and current obtained from the motor model determine the power losses of converters. The loss model is utilized to compute the losses of components in the power converters of SHEV's powertrain. The loss model depends on the operation principles and parameters of components that are determined by ratings of power converters. Therefore, the first step of building the loss model is to determine power ratings of converters in SHEV's powertrain.

The basic rules of sizing three power converters are explained as the following. The inverter is utilized to control the traction motor. Therefore, voltage and current ratings of the inverter are designed to meet requirements of the motor. The output voltage of the inverter should match the stator voltage of the motor, while the maximum output current is determined by the maximum achievable torque of the motor. Therefore, the voltage and current ratings rather than power rating are listed in Table 3.2. In the drive system of the HEVs, the engine/generator provides the total energy, while the battery pack only works as a power buffer that provides or absorbs peak power for the acceleration or deceleration of the vehicle. Therefore, the power rating of the engine/generator system should be equal to the average power of the traction motor in a standard driving cycle. Herein, FTP-75 is used as the benchmark to determine the ratings of the engine/generator system and the rectifier. It is apparent that the available peak power of the rectifier is much lower than that of the motor. During acceleration, the engine/rectifier system only provides fraction of the power that the motor requires, while the remaining has to be provided by the battery pack. Correspondingly, the power ratings of the battery pack and the dc/dc converter should be equal to the motor's power rating minus that of the rectifier if the power losses are neglected. The power ratings of the three power converters are listed in Table 3.2. Based on the power ratings, the components used in these converters have been selected and listed in Table 3.3.

In power electronic systems, power components such as IGBTs, MOSFETs, diodes, capacitors, inductors and transformers are key components that produce most of power losses. Since the magnetic components are much reliable, they are excluded from the reliability assessment of SHEV. The power loss calculation is the basis of thermal design and instantaneous thermal analy-

Table 3.3 Components for Power Converters of SHEV's Powertrain

Component	Part Number
Inverter IGBT (with freewheeling diode)	CM300DY-24A, Powerex.
Dc/dc converter IGBT	CM600DY-24A, Powerex.
Dc-link capacitor	B25655, EPCOS.
Battery	ANR26650M1-B, A123 Systems.

sis. The losses of semiconductor devices include conduction loss and switching loss. For capacitor and battery, the resistive losses dissipated in the equivalent series resistance (internal resistance for battery) are dominant. In order to reduce computational burden of simulation, analytic loss models are built, which are based on the behavioral device models [18]. Thus, the power losses of semiconductor devices and dc-link capacitors in the inverter and dc/dc converter can be obtained. The losses of components are further used as inputs to the thermal model to estimate the junction temperature.

3.3.5 Thermal Model

The thermal model is utilized to estimate junction temperatures of power semiconductors and core temperatures of batteries and capacitors, and detect thermal cycling by use of the power losses of key power component. The junction temperature and temperature variation of power devices are key factors that affect reliable operation and lifespans of components. The thermal impedance network for the semiconductor devices can be built based on the method presented in Chapter 2. The thermal parameters of devices can be obtained from the data sheets, while the thermal parameters of the heatsink are determined by the specific design of the cooling system.

3.3.6 Failure Rate Model

The function block of the reliability model is employed to determine various reliability metrics of power devices by use of the electrical and thermal stresses obtained from the loss model and the

thermal model. The reliability models can determine the failure numbers, MTTF, lifetime and other reliability indices of power components and power electronic systems. Herein, the empirical-based failure rate models obtained from RDF2000 [19] are used.

3.4 Reliability Assessment and Discussion

The reliability of SHEVs powertrain is evaluated based on the presented simulation model. The driving cycles FTP-75 and US06 are utilized, which represent the urban and highway driving conditions, respectively. In practical vehicles, the closed-loop liquid cooling system is typically utilized to dissipate the heat that is generated by the power converters. In the simulation model, such closed-loop cooling method is assumed. The proper regulation of inlet coolant temperature makes it a valid assumption that the heatsink temperature is constant and set to 60 $^{\circ}$C . The average total running time of a vehicle is about 500 hours per year [40]. The thermal cycles of the magnitude lower than 3 $^{\circ}$C have little influence on failure of components and therefore have been neglected.

The reliability of the powertrain depends on the type of driving cycles, the energy management strategy and initial conditions of the battery pack. In order to evaluate the effects of the various driving cycles on the reliability of SHEVs' powertrain, the simulations based on FTP-75 and US06 are implemented and analyzed. The energy management strategy determines the power distributions between two energy sources, the battery pack and the engine, and further determines electrical and thermal stresses of the rectifier and the dc/dc converter.

Herein, the engine on/off control that is suitable for urban driving is utilized. In this strategy, the battery pack is used as the main energy source and it provides total drive power to the inverter/motor while the engine is turned off if the state of charge (SoC) of the battery pack is within a set range. Once the SoC of the battery pack drops to its lower threshold, the engine is turned on and charges the battery pack with the full power. The benefit of the engine on/off control is that the engine always works in the high-efficiency range. However, the battery pack has to undergo deep

charge/discharge cycles and the dc/dc converter consequently has to experience higher electrical and thermal stresses. In order to minimize the influence of the initial condition of the battery pack, simulations have been conducted on four consecutive US06 cycles and four consecutive FTP-75 cycles, in which the battery pack experiences a full charge/discharge cycle.

Fig. 3.3, 3.4 and 3.5 illustrate the junction temperature profiles of IGBTs and diodes in the inverter and dc/dc converter in the first half of four consecutive FTP-75 driving cycles. It can be observed that the junction temperatures of devices fluctuate dramatically in a driving cycle although the absolute temperatures are not excessive. Fig. 3.6, 3.7 and 3.8 show the numbers and corresponding amplitudes of thermal cycles that the semiconductor devices in the inverter and dc/dc converter undergo in four consecutive FTP-75 cycles. It is observed that the amplitudes of the thermal cycles are mainly under 15 $^{\circ}$C, and that the IGBTs of the inverter and dc/dc converter experience more thermal cycles with higher amplitudes since the IGBTs have higher losses and correspondingly experience higher junction temperatures. The failure rates of components are related to the temperature cycles.

The failure rates and MTTFs of the power semiconductors, dc-link capacitors and battery cells, are listed in Table 3.4 and 3.5 for the FTP-75 driving cycle and US06 driving cycle, respectively. It should be noted that the failure rate of a component in these two tables is for a single device. Table 3.4 shows that the IGBTs of the converters have higher failure rates and therefore are less reliable. It is because the power losses dissipated in the switches are much higher than the losses of the diodes and correspondingly the thermal stresses are much higher, as shown in Fig. 3.3-3.5. Another worth noting observation is that the failure rate of the dc-link capacitors is lower than those of semiconductor devices by four orders of magnitude. Since there is no redundancy in the SHEV's power electronic system, the reliability of the overall system can be assessed by use of the part-count method. The failure rate of the whole system can be obtained by summing the failure rates of all power components, and the results are tabulated in Table 3.6.

The failure rate model of the battery that is presented in the reliability handbook RDF2000 is utilized for reliability analysis. This model is independent of its operating conditions and only de-

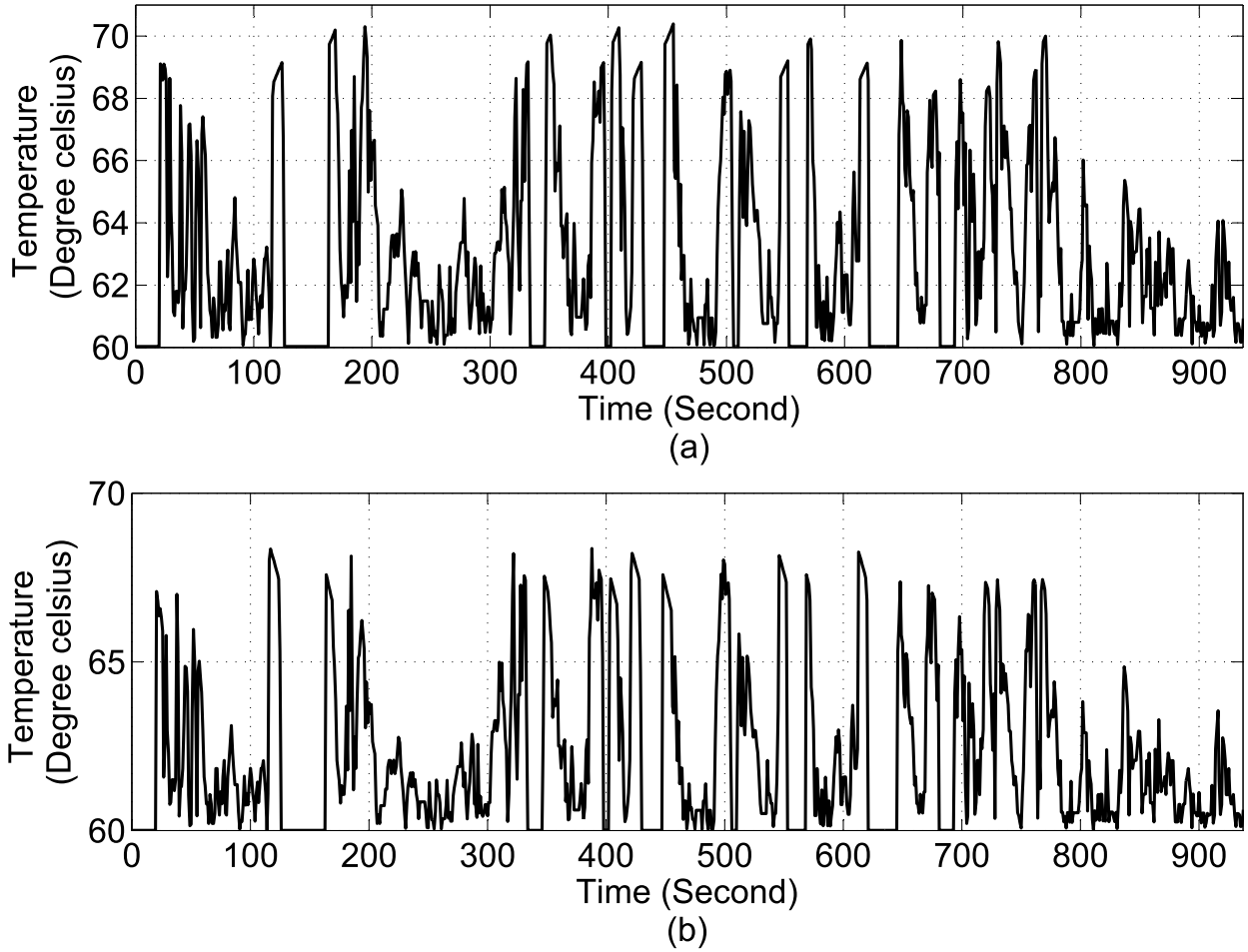


Figure 3.3 The junction temperatures of semiconductor devices in the inverter for the first half of four consecutive FTP-75 driving cycles : (a) IGBT; (b) diode.

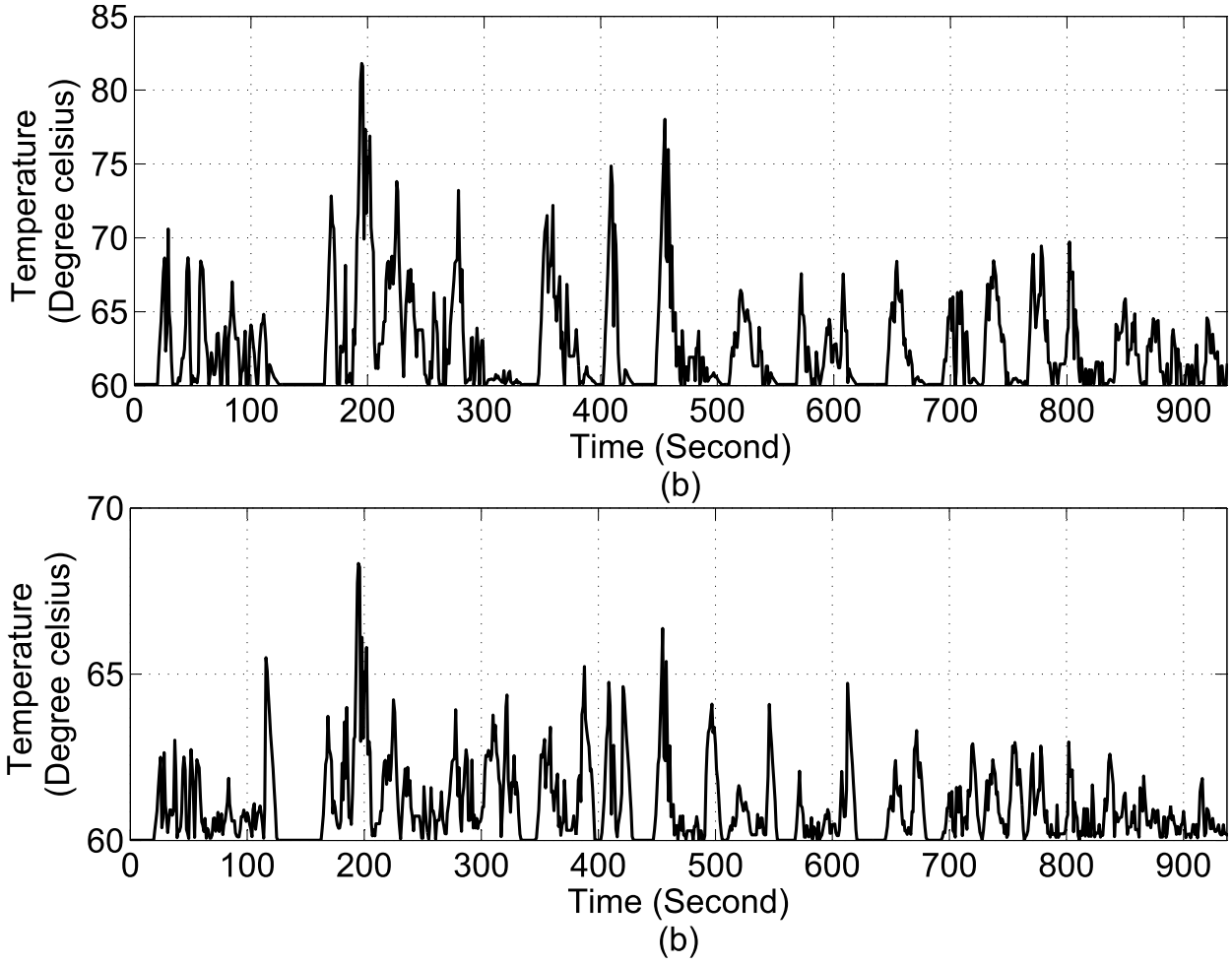


Figure 3.4 The junction temperatures of lower IGBT and upper diode (for boost mode) in the dc/dc converter for the first half of four consecutive FTP-75 driving cycles: (a) IGBT; (b) diode.

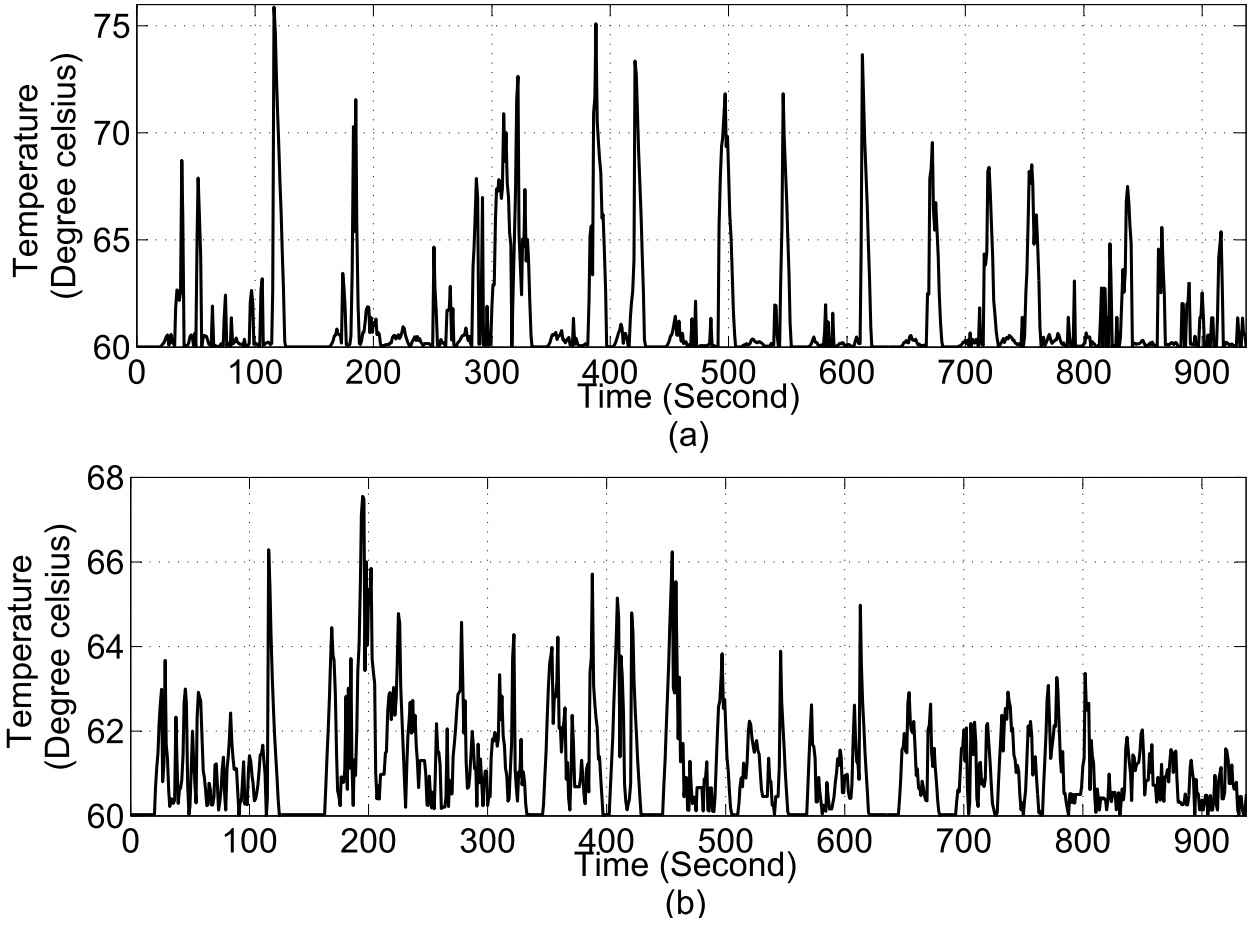


Figure 3.5 The junction temperatures of upper IGBT and lower diode (for buck mode) in the dc/dc converter for the first half of four consecutive FTP-75 driving cycles: (a) IGBT; (b) diode.

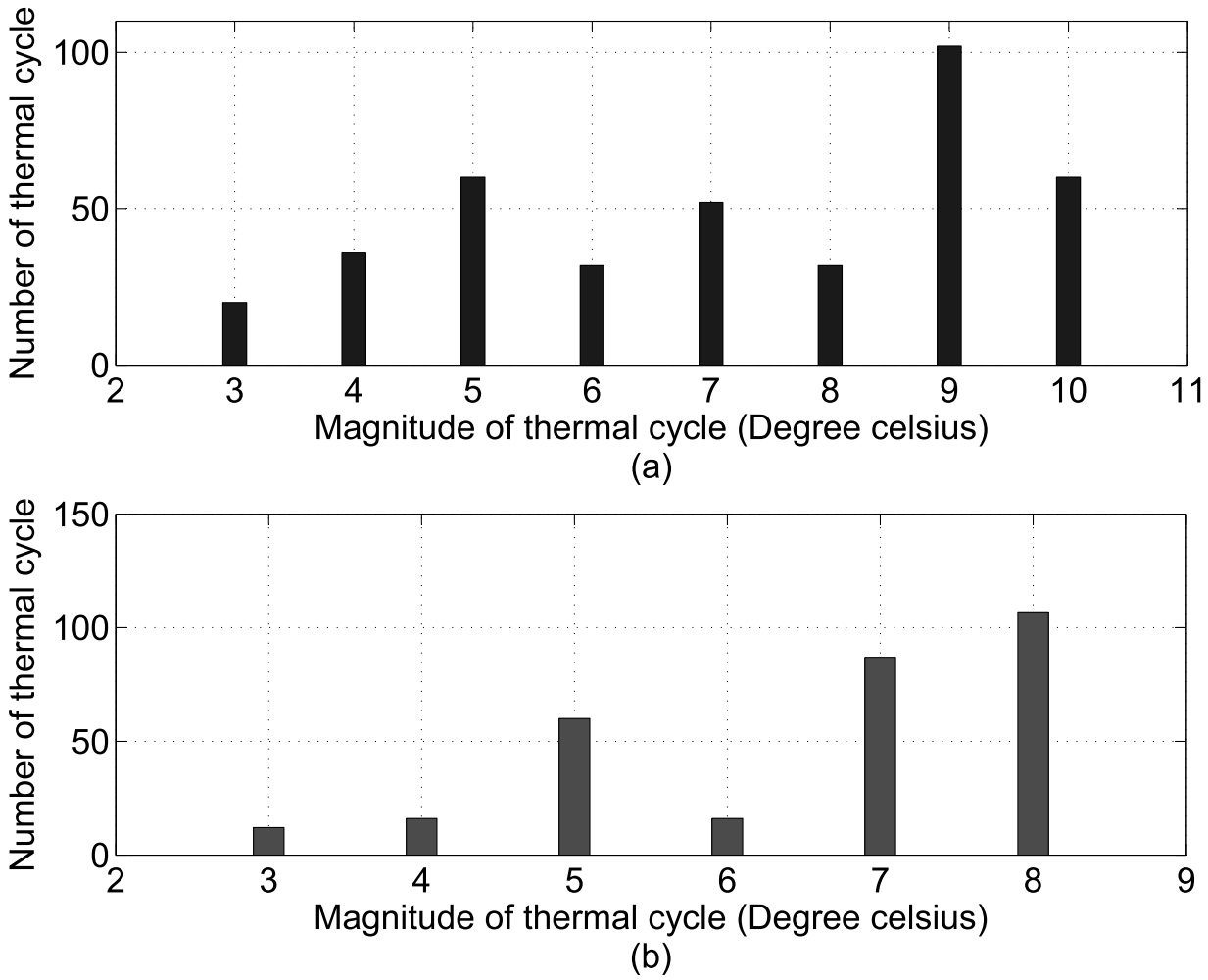


Figure 3.6 The numbers and amplitudes of semiconductor device thermal cycles in the inverter over four consecutive FTP-75 driving cycles: (a) IGBT; (b) diode.

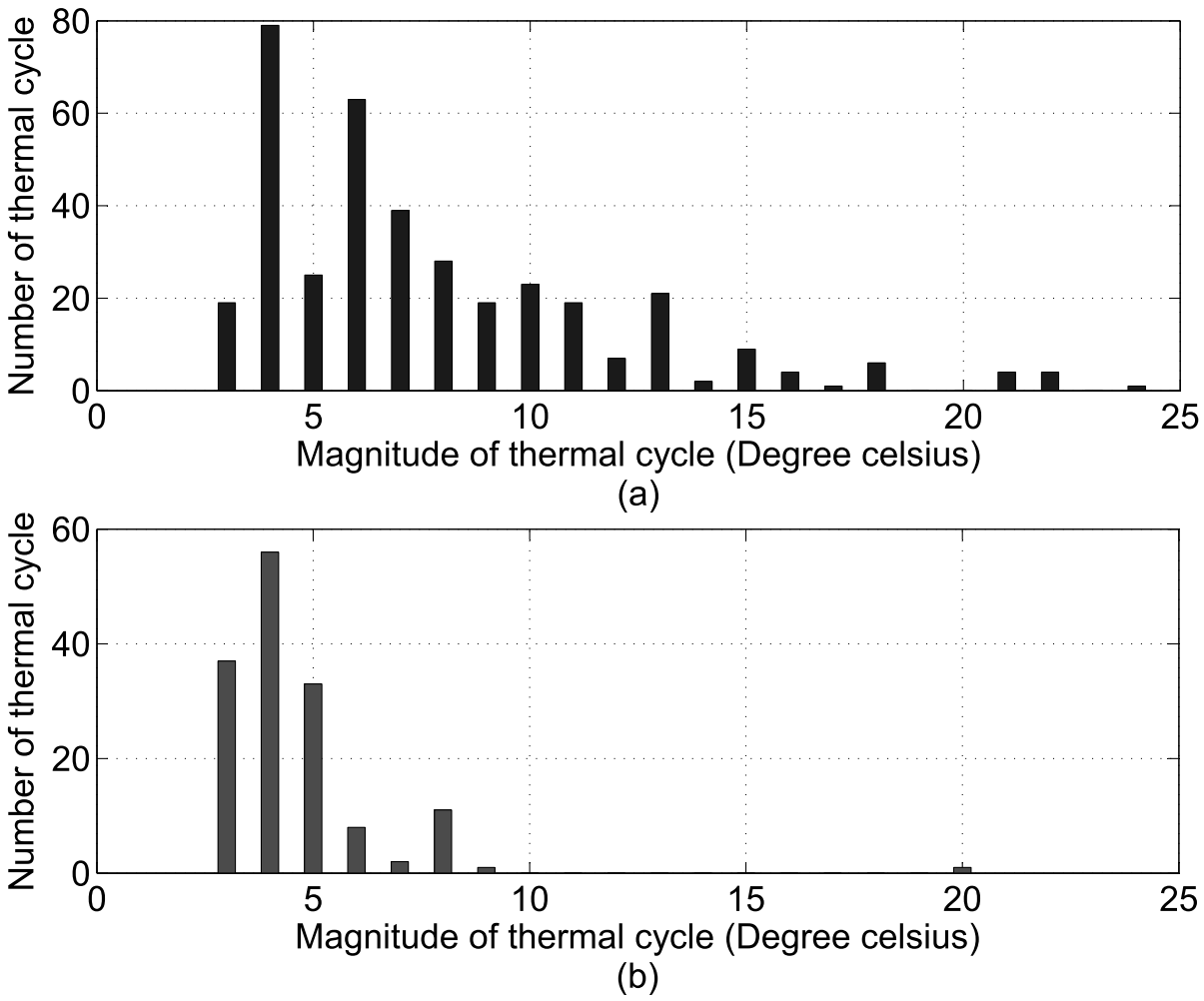


Figure 3.7 The thermal-cycle numbers and amplitudes of lower IGBT and upper diode (for boost mode) in the dc/dc converter over four consecutive FTP-75 driving cycles: (a) IGBT; (b) diode.

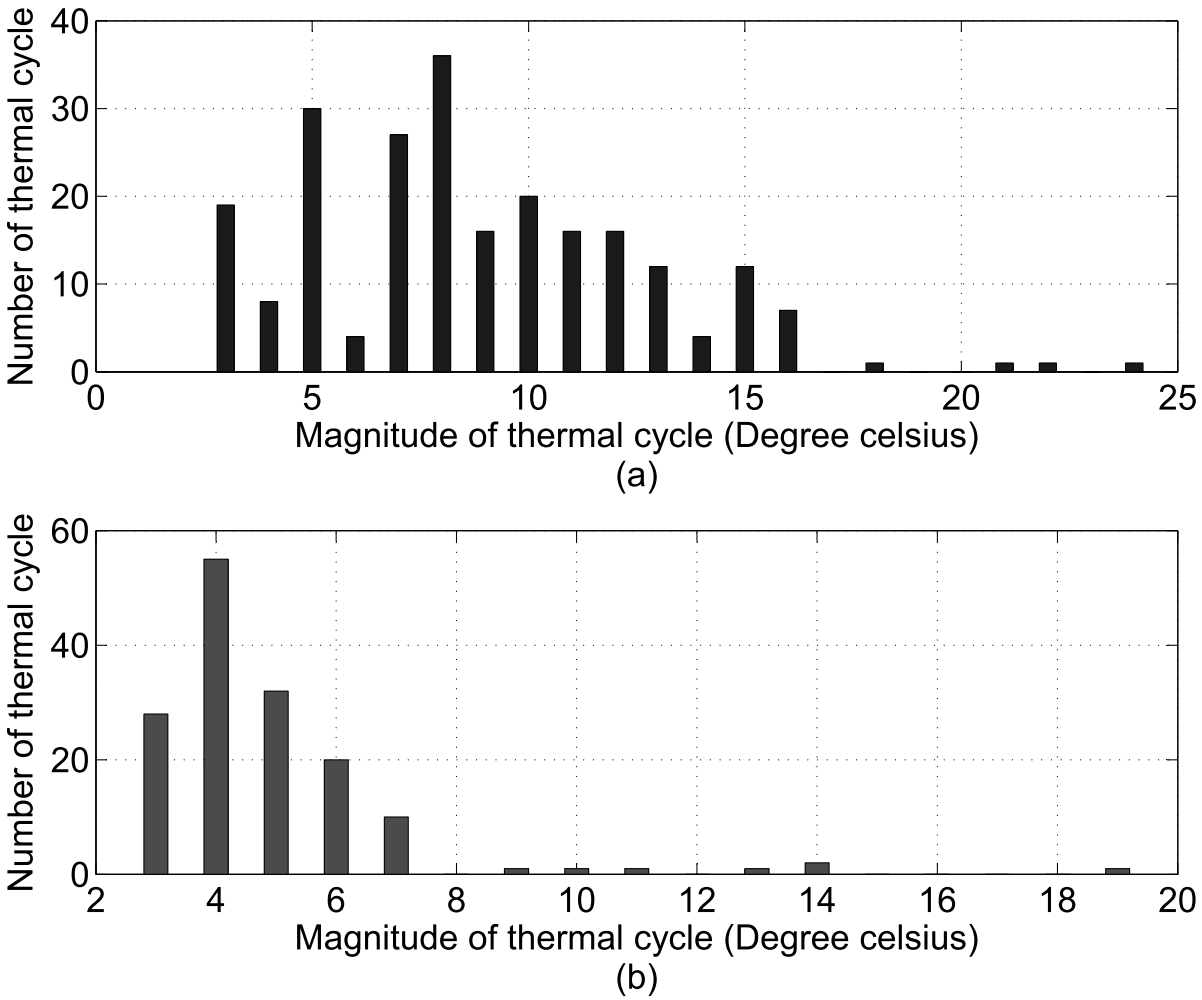


Figure 3.8 The thermal-cycle numbers and amplitudes of upper IGBT and lower diode (for buck mode) in the dc/dc converter over four consecutive FTP-75 driving cycles: (a) IGBT; (b) diode.

pends on the type and number of the battery cells. In the simulation model, 640 lithium-ion battery cells are used to form the battery bank in series and parallel manners. The failure rate of a single cell is listed in Table 3.4. Although the failure rate of each cell does not appear very high, the failure rate of the whole battery pack is as high as 96 failures per 10^6 hours, which is four times of the total failure rate of the semiconductor devices and capacitors. Correspondingly, the MTTF of the overall system is reduced to 8180 hours from 38030 hours by taking the battery bank into consideration, as shown in Table 3.4. The failure rate of the battery pack is dominant in the overall system. However, the failure rate model that is provided in Bellcore reliability handbook [44] is independent of the operating conditions of batter cells, such as battery core temperature, charge/discharge current, and depth of charge/discharge. As a result, any improvement of design and control strategies has a little effect on the failure rate and MTTF of the SHEV powertrain, which does not match practical observations and suggests more accurate battery reliability model needs to be developed. In fact, some lifetime models of battery based on electro-chemical theories that include effects of some operating conditions have been developed [45,46]. Nonetheless, these models depend on detailed battery design parameters that are unavailable in public domain, which renders it difficult for these models to be applied to the reliability analysis of battery systems. Therefore, in view of lack of the accurate applicable battery reliability model, the battery bank is excluded in the reliability analysis of the SHEV's power electronic system in the next two sections that two control strategies are presented to improve the reliability of the system.

Since US06 emulates the highway driving behaviors and features higher speeds and accelerations than the driving cycle FTP-75, the electrical and thermal stresses of the power converters in US06 cycles are much worse and correspondingly much higher failure rates and lower reliability have been predicted, as shown in Table 3.5 and 3.6.

Table 3.4 Failure Rates and MTTFs of Components in Power Electronic System of SHEV for FTP-75 Driving Cycle

Reliability index	Inverter IGBT	Inverter diode	Dc/dc lower IGBT	Dc/dc upper diode	Dc/dc upper IGBT	Dc/dc lower diode	Dc-link capacitor	Battery cell
Failure rate (/10^6 hours)	2.0298	1.3955	2.4523	0.6766	1.8345	0.7612	0.000839	0.15
MTTF (10^5 hours)	4.9266	7.1659	4.0778	14.780	5.4510	13.137	15300	6.667

Table 3.5 Failure Rates and MTTFs of Components in Power Electronic System of SHEV for US06 Driving Cycle

Reliability index	Inverter IGBT	Inverter diode	Dc/dc lower IGBT	Dc/dc upper diode	Dc/dc upper IGBT	Dc/dc lower diode	Dc-link capacitor	Battery cell
Failure rate (/10^6 hours)	4.7890	3.2056	9.2883	4.0930	6.8689	4.5617	0.00084	0.15
MTTF (10^5 hours)	2.0881	3.1196	1.0766	2.4432	1.4558	2.1922	11900	6.667

Table 3.6 Failure Rates and MTTFs of Power Electronic System of SHEV

Driving cycle / Reliability index	FTP-75		US06	
	System without battery	System with battery	System without battery	System with battery
Failure rate (/10^5 hours)	2.6294	12.229	7.2797	16.88
MTTF (10^4 hours)	3.803	0.818	1.374	0.592

3.5 Summary

In this chapter, based on the reliability evaluation framework proposed in Chapter 2, a reliability simulation model for the power converters in SHEVs' powertrain is presented. And then the reliability of an SHEV's power electronic system is evaluated in terms of failure rate and MTTF.

The reliability analysis results show that the semiconductor devices, in particular the IGBTs, are the least reliable components, and that the failure rates of the components strongly depend on the thermal stresses that the components experience. Therefore, alleviating the thermal stresses of semiconductor devices is an effective solution to reducing the failure rates of these power devices and further improving the reliability of SHEV's powertrain.

Chapter 4

Strategies for Improving Reliability of HEV's Powertrain

4.1 Introduction

The accurate reliability analysis not only provides an important guideline for planning, design and operation management of HEVs, it also allows designers to pinpoint the dominant causes of failure of systems and correspondingly make further design changes for improved system reliability. Based on the reliability analysis, two control strategies that are aimed to reduce the power losses of converters and consequently to improve the reliability of HEV's powertain have been proposed. The control methods are introduced as follows.

The first control scheme to improve reliability of HEV's powertrain is to allow the dc-link voltage of the inverter to vary according to the required output voltage. The reliability analysis shows that the thermal stresses of the semiconductor devices in power converters have a significant influence on the failure rates of the devices. The thermal stresses are determined by the power losses of components. Therefore, reducing power losses of power components is an effective solution to improving the reliability of an HEV powertrain. In fact, power losses of power components not only determine the reliability of power converters, but also influence the size of power converters

and fuel economy of HEVs. Therefore, a considerable amount of research effort has been focused on reducing power losses of HEVs' drive train. The authors of [47] investigate a motor-control method based on the direct self-control technique. This method applies the six-step modulation scheme to the inverter to reduce its switching loss in the constant-power region of motors. The loss of the auxiliary dc/dc converter for automotive application is investigated in [48]. Some alternative topologies of the dc/dc converter that interfaces the battery pack and the high-voltage dc bus are investigated to achieve higher efficiency of the powertrain [49–51]. This chapter presents a variable dc-link voltage control scheme for the power conversion unit of electric vehicles. Based on this control scheme, switching losses of the inverter and the dc/dc converter are greatly reduced. In particular, the inverter always operates at its optimal point with the highest efficiency.

In addition to the optimized dc-link voltage, the switching losses of the inverter can be further reduced through a proposed hybrid PWM scheme. For a two-level three-phase inverter, switching loss of semiconductors is dominant, and much effort is devoted to various techniques to reducing the switching loss, such as soft-switching technology and various modulation schemes. Different PWM schemes significantly influence performances of the three-phase inverter, in particular the harmonic distortion and switching losses. Continuous carrier-based PWM or space vector PWM schemes are extensively investigated and widely applied [4, 52]. By changing the positions of active voltage vectors or zero-sequence components in modulation signals, various discontinuous PWM schemes are formed to optimize switching losses or total harmonic distortion [53–56]. In comparison with continuous PWM schemes, the paramount benefit of discontinuous PWM schemes is that the number of the switching transitions during one carrier cycle is reduced to 4 from 6 and correspondingly the switching loss of the converter is reduced [4]. However, the harmonic distortion for discontinuous PWM schemes is worse than that for continuous PWM schemes, which impedes the wide application of the discontinuous PWM schemes. In the chapter, based on the variable dc-link voltage control, the discontinuous PWM schemes can be applied to the inverter to reduce the switching loss without compromising the harmonic distortion. And a hybrid discontinuous PWM scheme with the minimal switching loss is proposed to further

reduce the inverter losses and improve the reliability of the overall system.

4.2 Variable Dc-Link Voltage Control

Improving the reliability of HEV's drive train is as important as obtaining the reliability indices. Reliability evaluation is an effective approach to pinpointing the weakest link of the system and main causes of failure of HEV's power electronic system. From the aforementioned reliability analyses, the semiconductor devices is much less reliable than capacitors. Therefore, reducing the failure rates of these semiconductor devices can effectively enhance the reliability of HEV's powertrain. The failure models of IGBT and diode indicate that the junction temperature and thermal cycling of devices dominate their failure rates. Except for the cooling system and the environment that the system operates in, the thermal stresses of the components in the system are exclusively dependent upon power losses of the components. Therefore, reducing losses of components is the efficient way of reducing the failure rates of a power electronic system. In this section, variable dc-link voltage control is presented to improve the reliability of HEV's power converters.

4.2.1 Stator Voltage Profile of the Traction Motor

In the SHEV's drive system, the engine/generator and the battery unit can separately or jointly supply traction power to the inverter that directly controls the traction motor. By employing PWM scheme, the inverter operates from the dc-link voltage to achieve the required variable-frequency and variable-magnitude stator voltage for the traction motor. The relationship between the root-mean-square (RMS) value of the line-to-line stator voltage and the dc-link voltage for space vector PWM scheme can be mathematically expressed as

$$V_s = 0.612 * MI * V_{dc} \tag{4.1}$$

where MI that ranges between 0 and 1.15 is the modulation index of the inverter [57]. It can be observed that there are two freedoms to control stator voltage, modulation index and dc-link voltage. In practical scenarios, the required stator voltage of the motor depends on its operating modes, such as maximum-torque-per-ampere (MTPA) mode, and flux-weakening mode for permanent magnet machines, and load conditions. Fig. 4.1 illustrates the dramatic fluctuation of the peak stator voltage of the traction motor in an FTP-75 driving cycle. Correspondingly, the dc-link voltage or the modulation index has to be regulated so that the output voltage of the inverter produces certain torque at a given speed of the motor. The conventional control scheme is to maintain a constant dc-link voltage and regulate the output voltage of the inverter to track the required stator voltage by change of the modulation index.

Fig. 4.1(a) shows that the stator voltage is much lower than its maximum value during a large fraction of one driving cycle. Correspondingly, the modulation index deviates from its maximum value that is the operating point of the inverter with higher efficiency, since the switching loss of the semiconductors in the inverter is approximately proportional to the dc-link voltage [18], as shown in the following equation,

$$P_{sw} = \frac{6}{\pi} * f_s * (E_{on} + E_{off} + E_{rr}) * \frac{V_{dc} * I_{pk}}{V_{ref} * I_{ref}} \tag{4.2}$$

where f_s is the switching frequency, E_{on}, E_{off} and E_{rr} denote the turn-on and turn-off energy losses of the IGBT, and reverse recovery energy loss of the anti-parallel freewheeling diode, respectively, for the given reference commutation voltage V_{ref} and current I_{ref}, V_{dc} is the dc-link voltage, and I_{pk} is the peak value of the inverter output current. For a specific stator voltage, if the dc-link voltage can be regulated to follow the desired stator voltage while the modulation index of the inverter is kept constant and equal to its maximum value, the dc-link voltage can be reduced during a large fraction of a driving cycle and therefore the switching loss of the inverter would be greatly reduced.

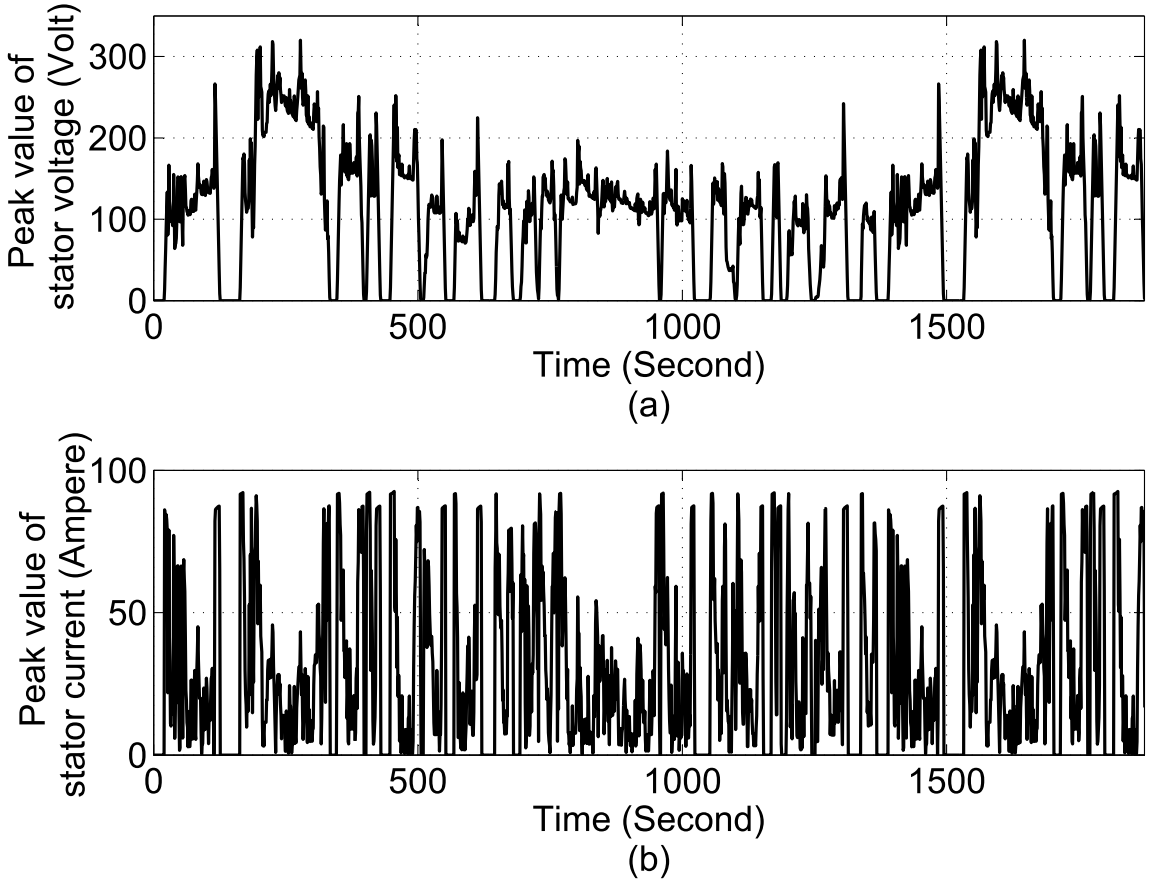


Figure 4.1 The peak values of the traction motor's line-to-neutral stator voltage and stator current in an FTP-75 driving cycle: (a) peak value of the stator voltage; (b) peak value of stator current.

4.2.2 Variable Dc-Link Voltage Control

In view of the aforementioned analysis, the variable dc-link voltage control strategy is proposed in the section. The principle is that the modulation index is kept constant and set to its maximum value, while the dc-link voltage is regulated by the dc/dc converter to follow the desired stator voltage of the traction motor. If the desired dc-link voltage decreases to be lower than the terminal voltage of the battery pack, the upper diode of the dc/dc converter is constantly forced on and correspondingly the battery pack is directly tied to the dc bus. In this case, the dc-link voltage is clamped by the terminal voltage of the battery pack that cannot be freely regulated to follow the profile of the required stator voltage. In order to supply the required stator voltage of the motor, the modulation index is regulated by the controller. The engine/generator and rectifier system is controlled by SoC and the upper-level energy management strategy of vehicles. Fig. 4.2 illustrates the control block diagram of the variable dc-link voltage drive system utilized in HEVs. Feasibility of this control strategy has been verified by the dynamic simulation based on MATLAB Simulink model, but the details are not presented in the section. It is worth mentioning that the variable dc-link voltage control can be implemented through modification of the original software-based control method, and hardware change is unnecessary. Therefore, the control strategy does not incur additional components, nor associated cost and unreliability.

Fig. 4.3 shows the dc-link voltage profiles for the variable dc-link voltage control as compared to the conventional variable modulation index control. Since the output voltage of the bidirectional dc/dc converter cannot be lower than its input voltage, when the required dc-link voltage is lower than the input voltage of the dc/dc converter, the practical dc-link voltage is equal to the input voltage, which is also the terminal voltage of the battery bank. The maximum dc-link voltage is determined by the maximum stator voltage. Herein, the nominal terminal voltage of the battery pack and the nominal line-to-line stator voltage of the traction motor are 264 V and 400 V, respectively, and the resultant maximum dc-link voltage is 568 V. It can be observed that during an FTP-75 driving cycle, the dc-link voltage for variable dc-link voltage control is much lower than that for variable modulation index control.

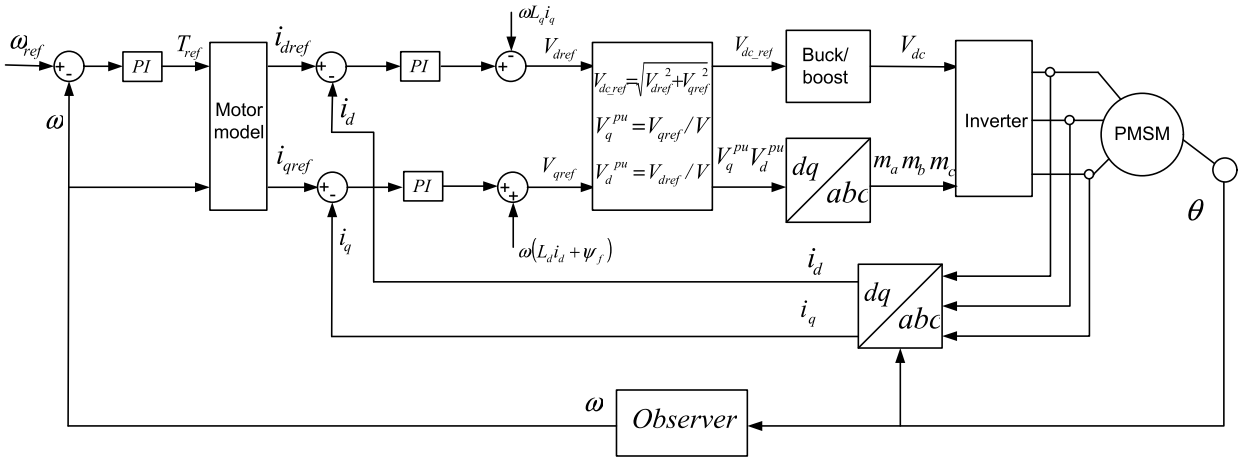


Figure 4.2 The control block diagram of the motor drive system with the variable dc-link voltage control.

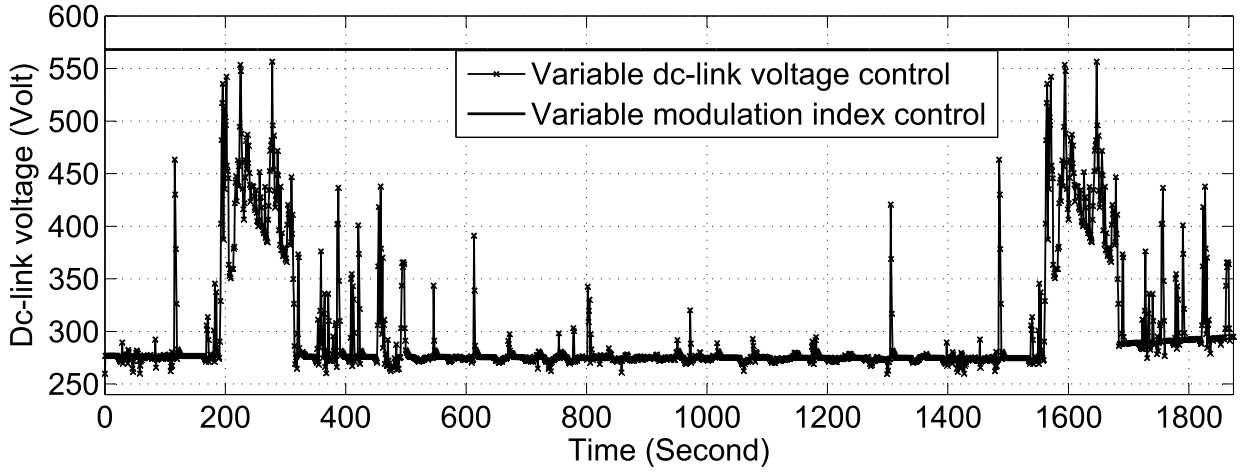


Figure 4.3 The dc-link voltage for variable dc-link voltage control and variable modulation index control in an FTP-75 driving cycle.

4.2.3 Verification of Benefits

The lower dc-link voltage will result in lower switching loss for the inverter. In comparison with the variable modulation index control, the modulation index for the variable dc-link control is higher. Although the modulation index affects the conduction loss of the inverter [18], the total power loss is still greatly reduced since the switching loss is dominant. The loss of the dc/dc converter also decreases. The benefit of the reduction in the overall loss can be verified by the simulation, as shown in Fig. 4.4. In order to clearly demonstrate the loss reduction of the proposed over conventional control schemes, the losses of the inverter, the dc/dc converter and the overall system in a half FTP-75 driving cycle are evaluated. The losses include conduction and switching losses of dc/dc converter and inverter semiconductor devices, core and winding losses of inductor in dc/dc converter, and the equivalent-series-resistance loss of dc-link capacitors and input filter capacitors of the dc/dc converter. It can be observed from the Fig. 4.4 that the losses of the inverter is greatly reduced, and and the loss of dc/dc converter also reduced.

Since the HEV powertrain experiences manifold operating conditions in terms of voltage stress, current stress and power stress in a driving cycle, it is unfair to evaluate the overall efficiency of converters in a whole driving cycle by use of efficiencies of converters in several operating points. Therefore, the energy that is consumed in one or several driving cycles is utilized to evaluate efficiency of HEV powertrain. Herein, the energy consumption and energy loss in several driving cycles are defined to quantitatively evaluate the efficiency of power converters for variable modulation index control and variable dc-link voltage control. The energy loss is defined by

$$E_{loss} = \int_{T_d} P_{loss}\, dt \tag{4.3}$$

where P_{loss} is the total loss of the inverter and dc/dc converter, and T_d is the time span of the driving cycles. The energy consumption is defined as total energy input in driving cycles, and it

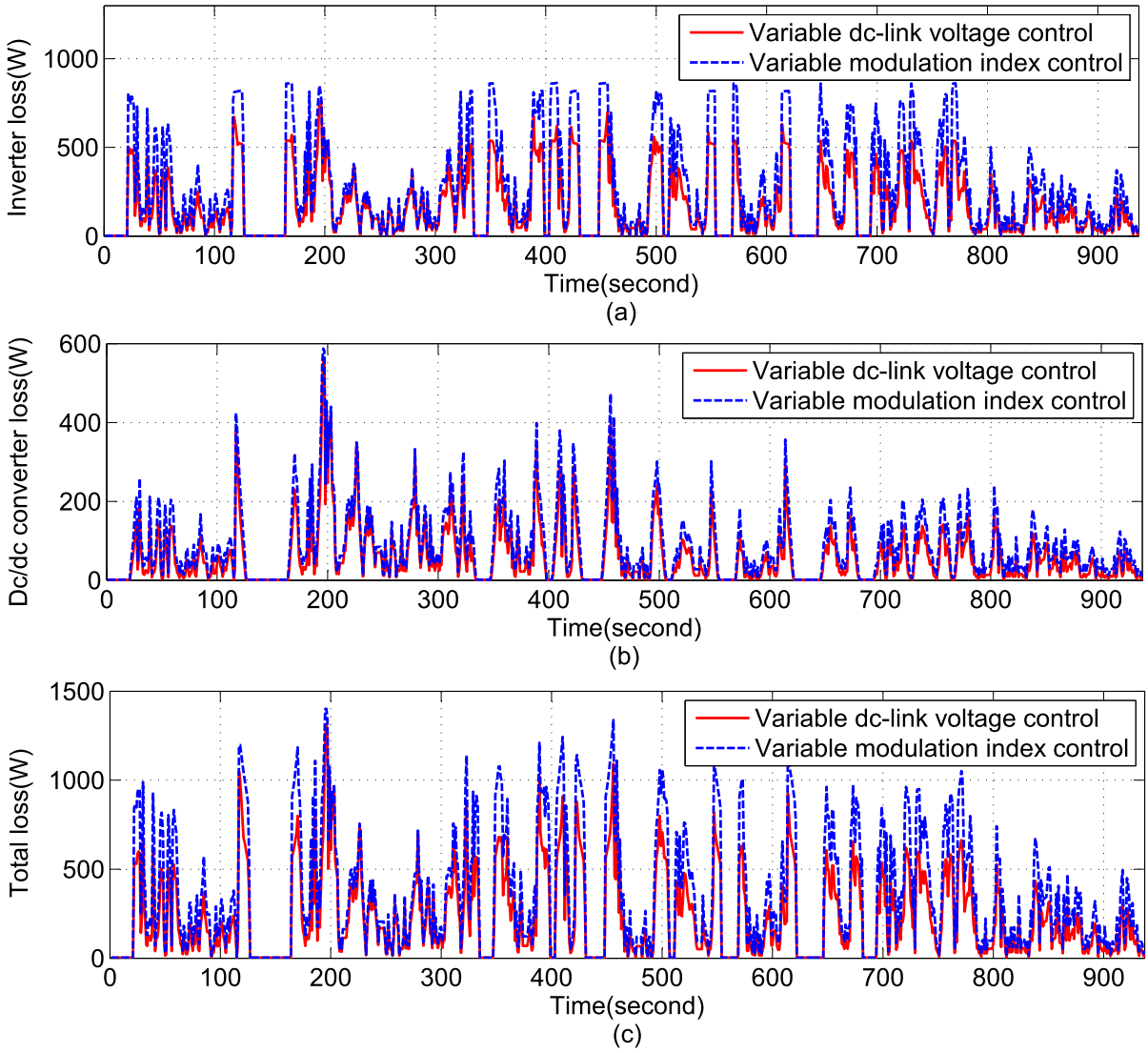


Figure 4.4 The losses profiles for variable dc-link voltage control and variable modulation index control in the first half of four consecutive FTP-75 driving cycles: (a) inverter loss; (b) dc/dc converter loss; (c) total loss.

Table 4.1 Energy Consumption and Loss for Variable Modulation Index Control and Variable Dc-link Voltage Control in Four Consecutive FTP-75 Driving Cycles

Control Strategy	Energy consumption (10^7 Joule)	Energy loss (10^6 Joule)
Variable modulation index	1.2745	2.87
Variable dc-link voltage	1.1829	1.9294

can be expressed mathematically as

$$E_{consum} = \int_{T_d} (P_{rectifier} + P_{battery})\, dt \tag{4.4}$$

where $P_{rectifier}$ and $P_{battery}$ are the output powers of the rectifier and the battery pack, respectively. Numeric simulations based on four consecutive FTP-75 driving cycles and four consecutive US06 driving cycles have been conducted. The energy consumption and loss for both types of driving cycles are tabulated in Table 4.1 and 4.2. In comparison with the commonly used control scheme of variable modulation index, with variable dc-link voltage control the energy loss of the power converters is reduced by 33% in four FTP-75 driving cycles, while in four US06 driving cycles the energy loss decreases by 11%. The energy consumption for two types of driving cycle is reduced by 7.2% and 1.4%, respectively. US06 driving cycle represents highway driving behaviors, and the required stator voltage and corresponding dc-link voltage are closer to their upper limits. In contrast, FTP-75 models the frequent stop-going urban driving behaviors that feature low speeds and low torque, and the corresponding stator voltage and dc-link voltage are much lower than their upper limits. As a result, the variable dc-link voltage control strategy brings forth greater reduction of energy loss for urban driving, which makes variable dc-link voltage control particularly suitable for urban driving.

The decreased switching losses also reduce the temperature of semiconductor junctions and capacitors, as illustrated by the junction temperature profiles of semiconductor devices in the first half of the four consecutive FTP-75 driving cycles in Fig. 4.5, 4.6 and 4.7. It can be observed

Table 4.2 Energy Consumption and Loss for Variable Modulation Index Control and Variable Dc-link Voltage Control in Four Consecutive US06 Driving Cycles

Control Strategy	Energy consumption (10^7 Joule)	Energy loss (10^6 Joule)
Variable modulation index	1.3954	1.6892
Variable dc-link voltage	1.3764	1.5061

that under variable dc-link voltage control, the junction temperatures of IGBT and diode in the inverter, and IGBT and lower diode in dc/dc converter are much lower since the losses of the semiconductors are reduced. One exception is the upper diode in the dc/dc converter. In some operating conditions, the thermal stress of the diode is elevated in the case of the variable dc-link voltage control. It is because in the case of the variable dc-link voltage control, the conduction loss of the dc/dc convert's upper diode increases while its switching loss decreases, and the resultant total loss may increase in some operation conditions.

The reliability data are obtained from the simulation model presented in the section. The failure rates and MTTFs in the case of FTP-75 driving cycle are tabulated in Table 4.3. When the proposed variable dc-link voltage control is utilized, the failure rates of the inverter IGBT and diode are reduced by approximate 32% and 20%, respectively, for the FTP-75 driving cycles. And the failure rates of the lower and upper IGBTs in dc/dc converter decrease by approximate 47% and 22%, respectively. The failure rate of the overall system is reduced by 27%, and its MTTF is improved by 37%. However, the failure rate and MTTF of dc-link capacitors almost remain unchanged. The upper diode of dc/dc converter becomes less reliable. For US06 driving cycles, the reliability of main components and the system is improved with various degrees, as shown in Table 4.4. Therefore, in comparison with conventional variable modulation index control, the proposed variable dc-link voltage control greatly improve the reliability of key power components and power electronic system of HEV powertrain.

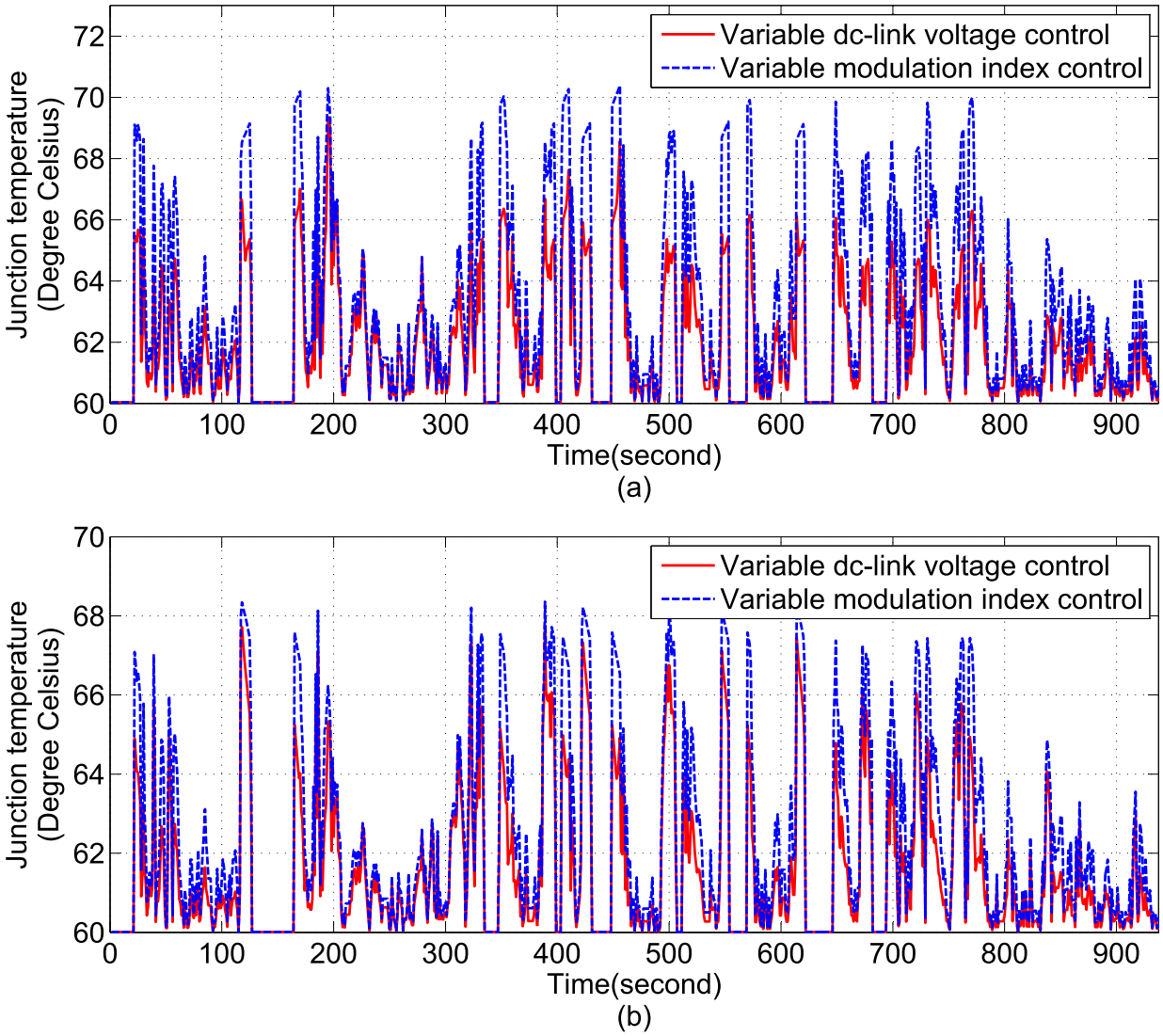


Figure 4.5 The junction temperatures of the inverter IGBT and diode for variable dc-link voltage control and variable modulation index control in the first half of four consecutive FTP-75 driving cycles: (a) IGBT; (b) diode.

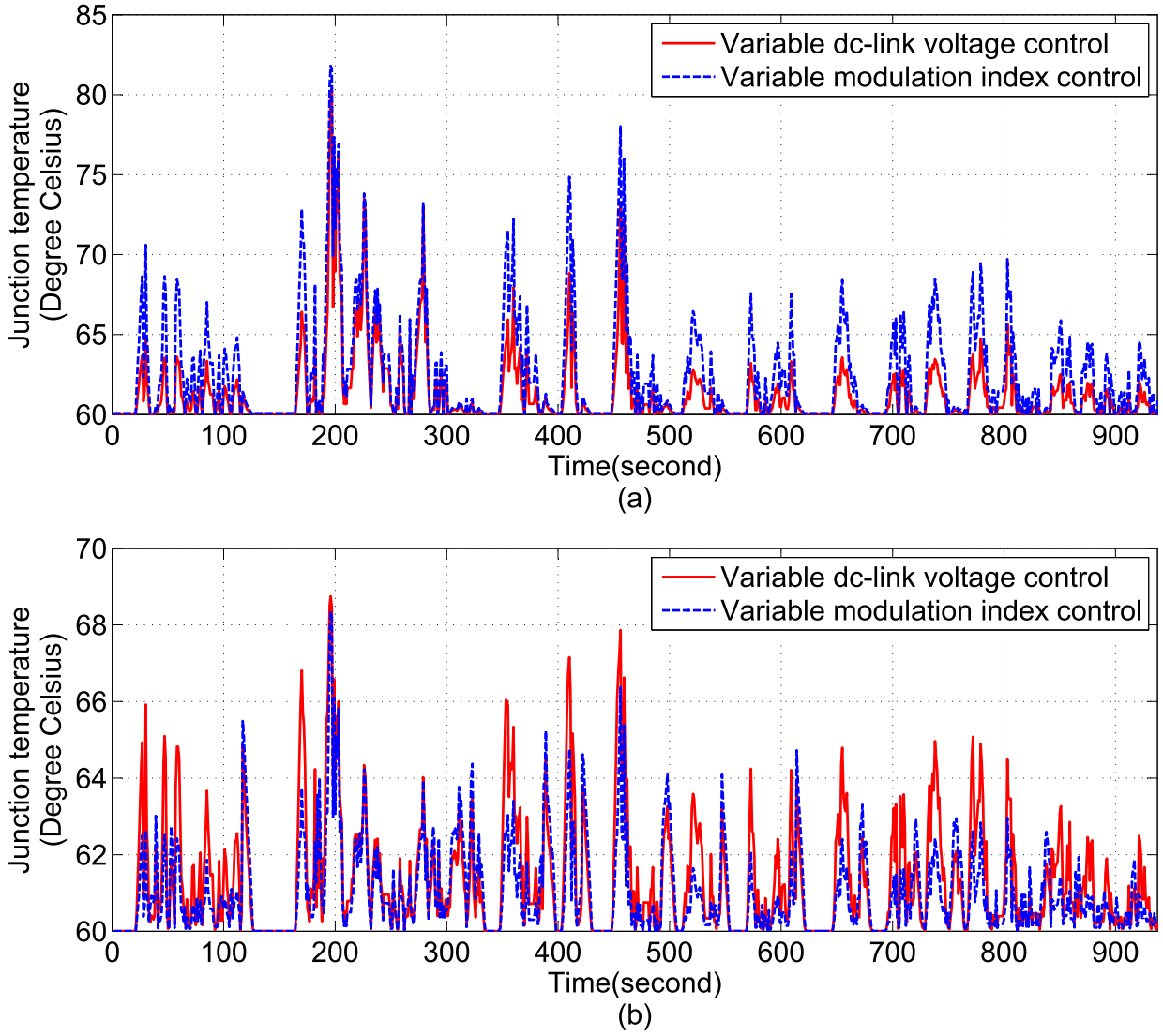


Figure 4.6 The junction temperatures of dc/dc converter lower IGBT and upper diode (for boost mode) for variable dc-link voltage control and variable modulation index control in the first half of four consecutive FTP-75 driving cycles: (a) IGBT; (b) diode.

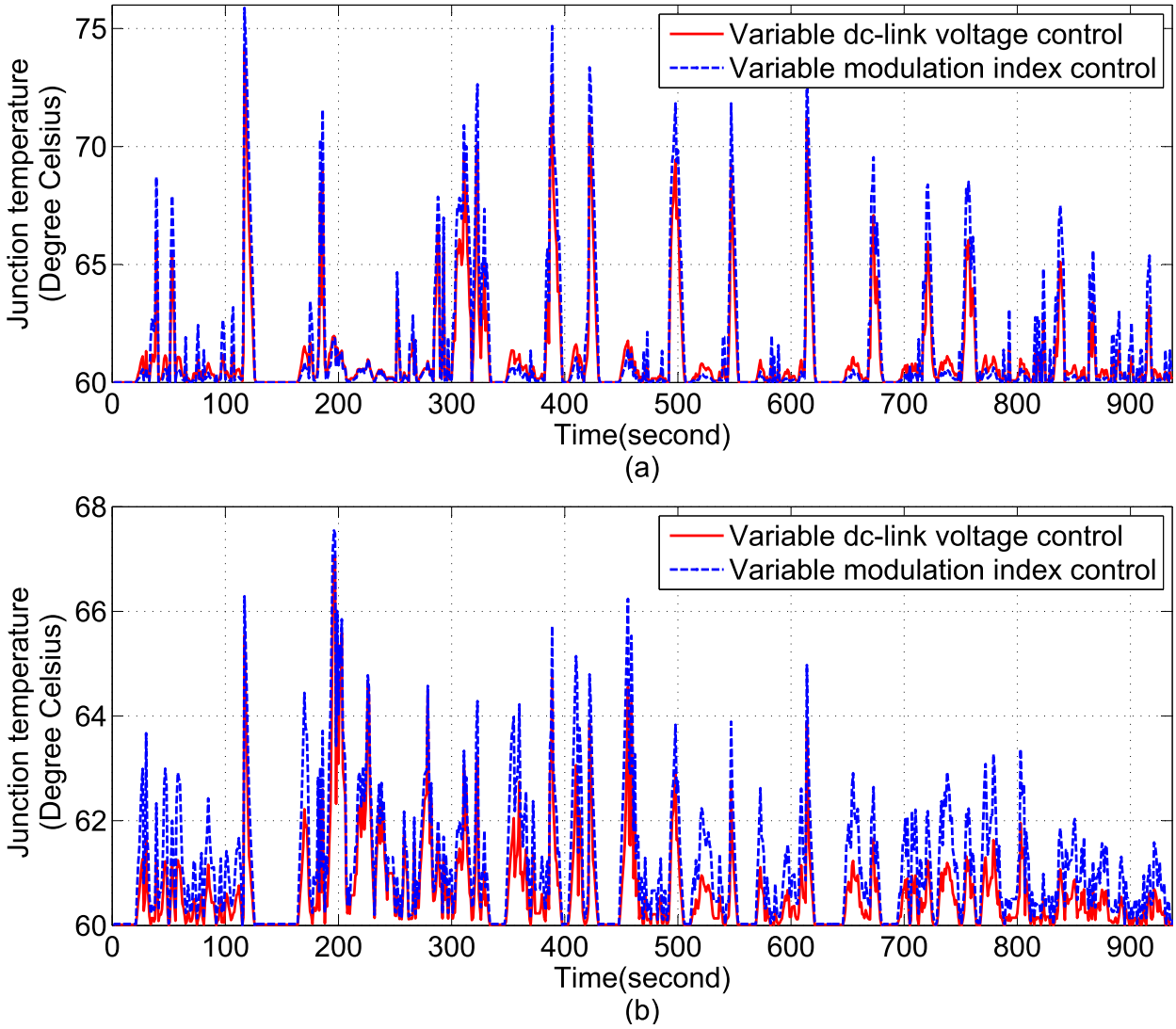


Figure 4.7 The junction temperatures of dc/dc converter upper IGBT and lower diode (for buck mode) for variable dc-link voltage control and variable modulation index control in the first half of four consecutive FTP-75 driving cycles: (a) IGBT; (b) diode.

Table 4.3 Failure Rates and MTTFs OF SHEV's Power Electronic System for Variable Dc-Link Voltage Control in the Case of FTP-75 Driving Cycle

Reliability index	Inverter IGBT	Inverter diode	Dc/dc lower IGBT	Dc/dc upper diode	Dc/dc upper IGBT	Dc/dc lower diode	Dc-link capacitor	System without battery
Failure rate (/10^6 hours)	1.3804	1.1101	1.3023	0.9982	1.4311	0.4827	0.000839	19.175
MTTF (10^5 hours)	7.2441	9.0084	7.679	10.019	6.9874	20.716	11917	0.5215

Table 4.4 Failure Rates and MTTFs OF SHEV's Power Electronic System for Variable Dc-Link Voltage Control in the Case of US06 Driving Cycle

Reliability index	Inverter IGBT	Inverter diode	Dc/dc lower IGBT	Dc/dc upper diode	Dc/dc upper IGBT	Dc/dc lower diode	Dc-link capacitor	System without battery
Failure rate (/10^6 hours)	4.4076	2.9565	9.1932	4.0352	6.3167	4.4480	0.00084	68.195
MTTF (10^5 hours)	2.2688	3.3824	1.0878	2.4782	1.5831	2.2482	11900	0.1466

4.3 Hybrid Discontinuous PWM Scheme with Minimal Switching Loss

The proposed variable dc-link voltage control improves the efficiency of power converters and reliability of SHEV powertrain. The variable dc-link voltage control features constant modulation index that is set to its maximum value. Discontinuous modulation schemes are particular suitable for the inverter under variable dc-link voltage control, since at the maximum modulation index, discontinuous PWM (DPWM) schemes have the same harmonic performance as continuous PWM. In comparison with continuous modulation schemes, discontinuous PWM schemes can further reduce the switching loss of the inverter. In this section, the application of discontinuous modulation to HEVs is investigated in terms of switching loss and harmonic distortion.

4.3.1 Hybrid Discontinuous PWM

PWM shcemes exert a significant influence on performances of the inverters, in particular switching loss and harmonic distortion. Although continuous PWM schemes are commonly applied to the inverter, various discontinuous PWM schemes are investigated to reduce switching loss of the inverter [3, 4]. Several discontinuous PWM strategies that are termed as 60° DPWM, 30°-lagging 60° DPWM, 30°-leading 60° DPWM and 30° DPWM, have been analyzed in [4]. The common feature of these discontinuous modulation schemes is that one of three phase legs of the inverter is clamped to the negative or positive side of the dc bus and does not switch in one sixth of a fundamental cycle. Therefore, the paramount advantage of the discontinuous PWM schemes over continuous modulation is that the number of the switching transitions during a carrier cycle is reduced to 4 from 6. Correspondingly, the switching loss of the inverter is reduced.

Fig. 4.8 shows the normalized switching losses of the inverter for various discontinuous modulation schemes [3]. Herein, the normalized switching losses are obtained by dividing the switching losses for various PWM schemes with that for the continuous space vector PWM. It can be observed that for discontinuous modulation, the averaged switching loss of the inverter over one

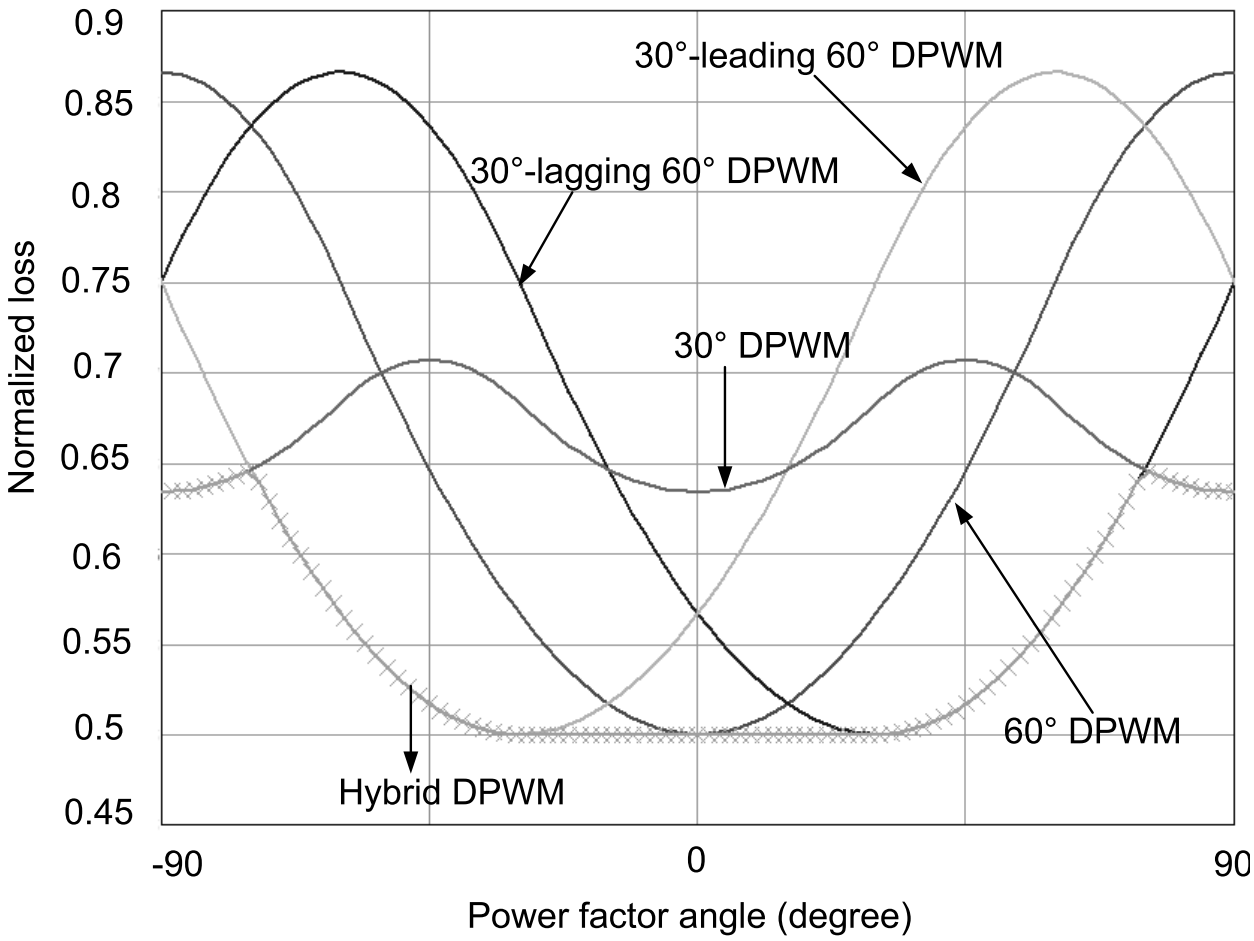


Figure 4.8 Normalized switching losses for various discontinuous PWM schemes with same carrier frequency [3].

fundamental cycle depends on the power factor angle of the load. The 60° DPWM results in half switching loss of continuous PWM at unity power factor. The reduction of switching losses peaks at a unity power factor, since the peak of the load current flows through the non-switching leg. In comparison with 60° DPWM, the switching-loss curve of the 30°-lagging 60° DPWM is only shifted by 30° in phase angle, while the loss curve of 30°-leading 60° DPWM is shifted by -30° in phase angle. In fact, the switching loss for various DPWM schemes is a periodic function of power factor angle, and the periods for 60° DPWM and 30° DPWM are 180° and 90°, respectively. The switching loss for discontinuous modulation is lower than that for continuous PWM schemes in the full range of power factor angle.

If the switching loss curves in Fig. 4.8 are further scrutinized, an optimal discontinuous modu-

Table 4.5 Hybrid Discontinuous PWM Scheme

Power factor angle ϕ	Hybrid discontinuous PWM
$-75^\circ \geqslant \phi \geqslant -90^\circ$ & $90^\circ \geqslant \phi \geqslant 75^\circ$	30° DPWM
$-30^\circ \geqslant \phi \geqslant -75^\circ$	30°-leading 60° DPWM
$30^\circ \geqslant \phi \geqslant -30^\circ$	60° DPWM with ϕ phase shift
$75^\circ \geqslant \phi \geqslant 30^\circ$	30°-lagging 60° DPWM

lation scheme with minimal switching loss can be constructed by following the lower envelope of multiple modulation schemes. In the range of -30° to 30° power factor angle, the minimal loss can be obtained by use of 60° DPWM with phase shift of the power factor angle. While the power factor angle is between 30° and 75°, 30°-lagging 60° DPWM corresponds to the lowest switching loss. In the range of power factor angle of -30° to -75°, 30°-leading 60° DPWM results in the lowest switching loss. In other range, the optimized switching loss can be obtained when 30° DPWM is utilized. Therefore, a hybrid PWM scheme with minimized switching loss is obtained if the appropriate discontinuous PWM schemes are employed for various power factor angles. The choices of DPWM schemes in the proposed hybrid DPWM are tabulated in Table 4.5. The switching loss for the hybrid PWM with minimized loss is also a periodic function of the power factor angle with the period of 180°, as illustrated in Fig. 4.8.

In comparison with continuous PWM, discontinuous modulation schemes reduce the number of switching transitions per phase leg over each fundamental cycle, but lead to suboptimal harmonic performance. The increased voltage harmonics would result in higher harmonic current and corresponding harmonic loss of loads. In order to properly evaluate harmonic losses, harmonic distortion factor (HDF) is defined, which is a function of the modulation index and independent of dc-link voltage and load inductance [4]. According to [4], the RMS value of the harmonic current for the three-phase inverter with delta-connected load is related to HDF(M) by

$$I_h = (\frac{V_{dc}}{24 f_s L_\sigma})^2 * HDF(M) \tag{4.5}$$

where V_{dc} is dc-link voltage, f_s is carrier frequency, and L_σ is load inductance. The harmonic distortion factors for continuous and discontinuous modulation schemes are shown in Fig. 4.9. It is evident that the harmonic distortion of the inverter for discontinuous modulation schemes is higher as compared to continuous SVPWM scheme for lower modulation index. However, the harmonic distortion factors for discontinuous PWM schemes are comparable to that for continuous modulation in the vicinity of maximal modulation index. Herein, the variable dc-link voltage control is utilized, and the corresponding modulation index is set to its maximal value, at which discontinuous modulation schemes have comparable harmonic performance of continuous modulation scheme. Therefore, the combination of variable dc-link voltage control and discontinuous PWM schemes achieves the minimized switching loss of the inverter without compromising the harmonic performance.

4.3.2 Verification of Benefits

The improved performance of the hybrid discontinuous PWM scheme in terms of the loss has been verified by simulation. From the system point of view, the hybrid DPWM only reduces the loss of the inverter, while has little influence on the dc/dc converter. The losses of the inverter and the system for variable dc-link voltage control in conjunction with continuous SVPWM scheme and the hybrid DPWM scheme are illustrated in Fig. 4.10. It can be observed that the losses of both the inverter and the system are reduced by employing the hybrid DPWM strategy. The quantitative evaluations of the loss reduction are illustrated in Table 4.6 and 4.7. For four FTP-75 driving cycles, the energy consumption and energy loss are reduced by 3.4% and 22%, respectively. In case of four US06 driving cycles, the energy consumption and energy loss decrease by 2.9% and 19%, respectively.

Likewise, the temperatures of the inverter IGBT and diode junctions are reduced, as shown in Fig. 4.11, since the hybrid DPWM strategy reduces the switching loss. Table 4.8 lists failure rates and MTTFs of semiconductors and capacitors in the power converters. In comparison with Table 4.3, the failure rates of the inverter IGBT and diode are further reduced, while other compo-

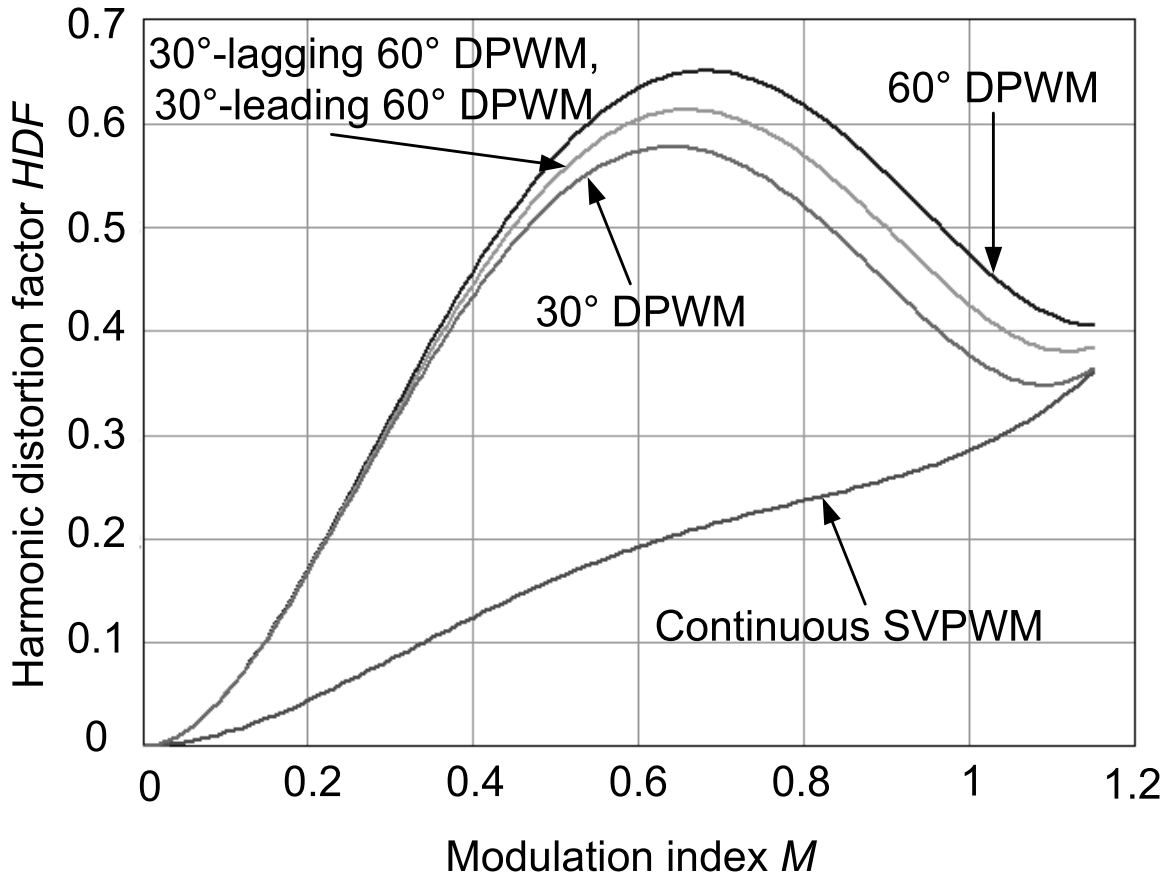


Figure 4.9 Harmonic distortion factors HDF for various modulation schemes as a function of modulation index [4].

nents' failure rates remain unchanged. The failure rate of the overall system is also greatly reduced by use of the hybrid DPWM scheme. Therefore, the proposed hybrid discontinuous modulation in conjunction with the variable dc-link voltage control greatly reduces the loss of the inverter and improves the reliability of HEV Powertrain without compromising harmonic performance of the inverter.

4.4 Summary

On the basis of accurate reliability analysis, the variable dc-link voltage control and hybrid discontinuous modulation scheme are presented in SHEV's drive train. It has been verified that the

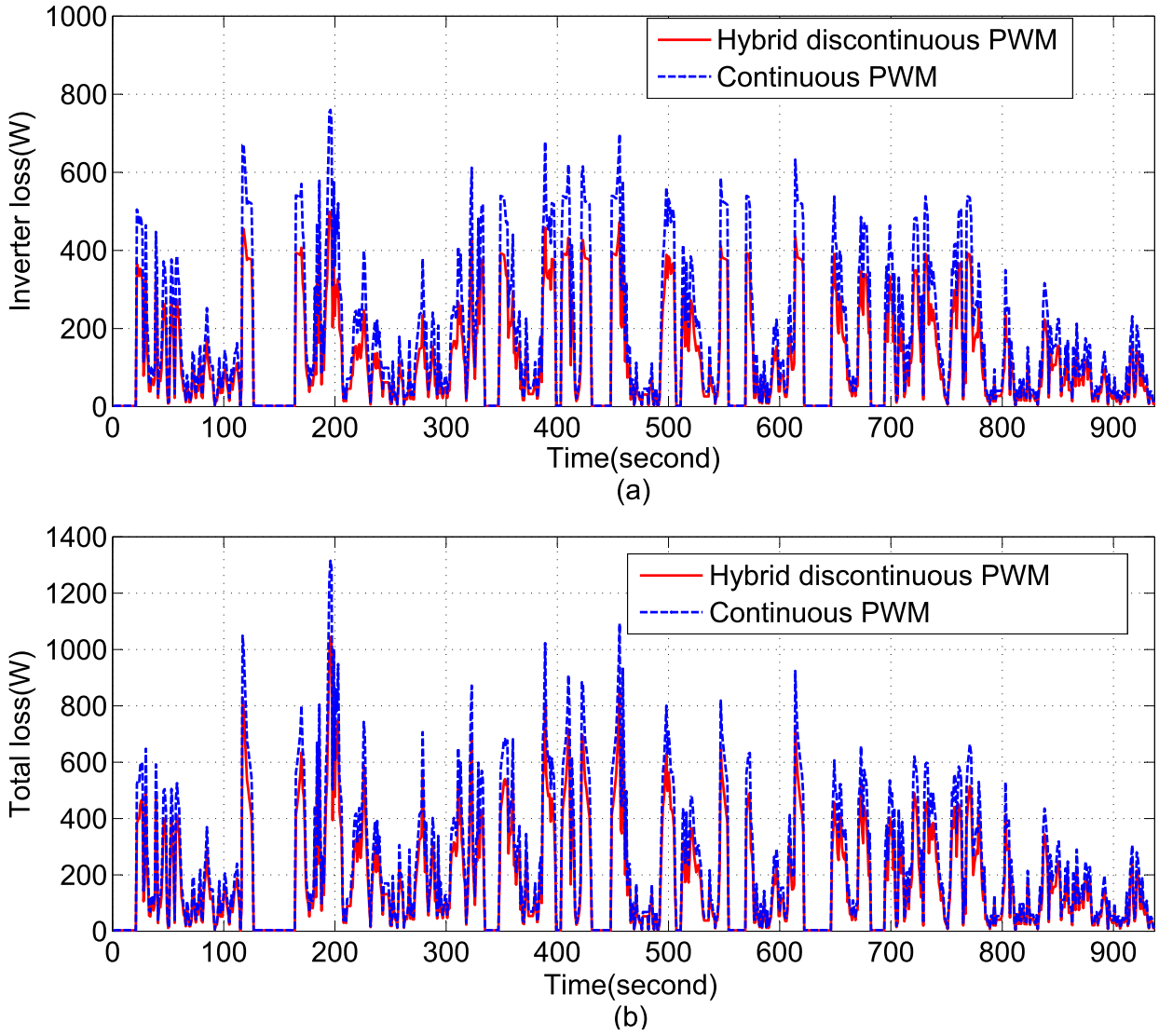


Figure 4.10 The losses profiles for hybrid discontinuous PWM and continuous PWM in the first half of four consecutive FTP-75 driving cycles: (a) inverter loss; (b) total loss.

Table 4.6 Energy Consumption and Loss for Continuous PWM and Hybrid discontinuous PWM in Four Consecutive FTP-75 Driving Cycles

Control Strategy	Energy consumption (10^7 Joule)	Energy loss (10^6 Joule)
Continuous PWM	1.1829	1.9294
Hybrid DPWM	1.1422	1.5138

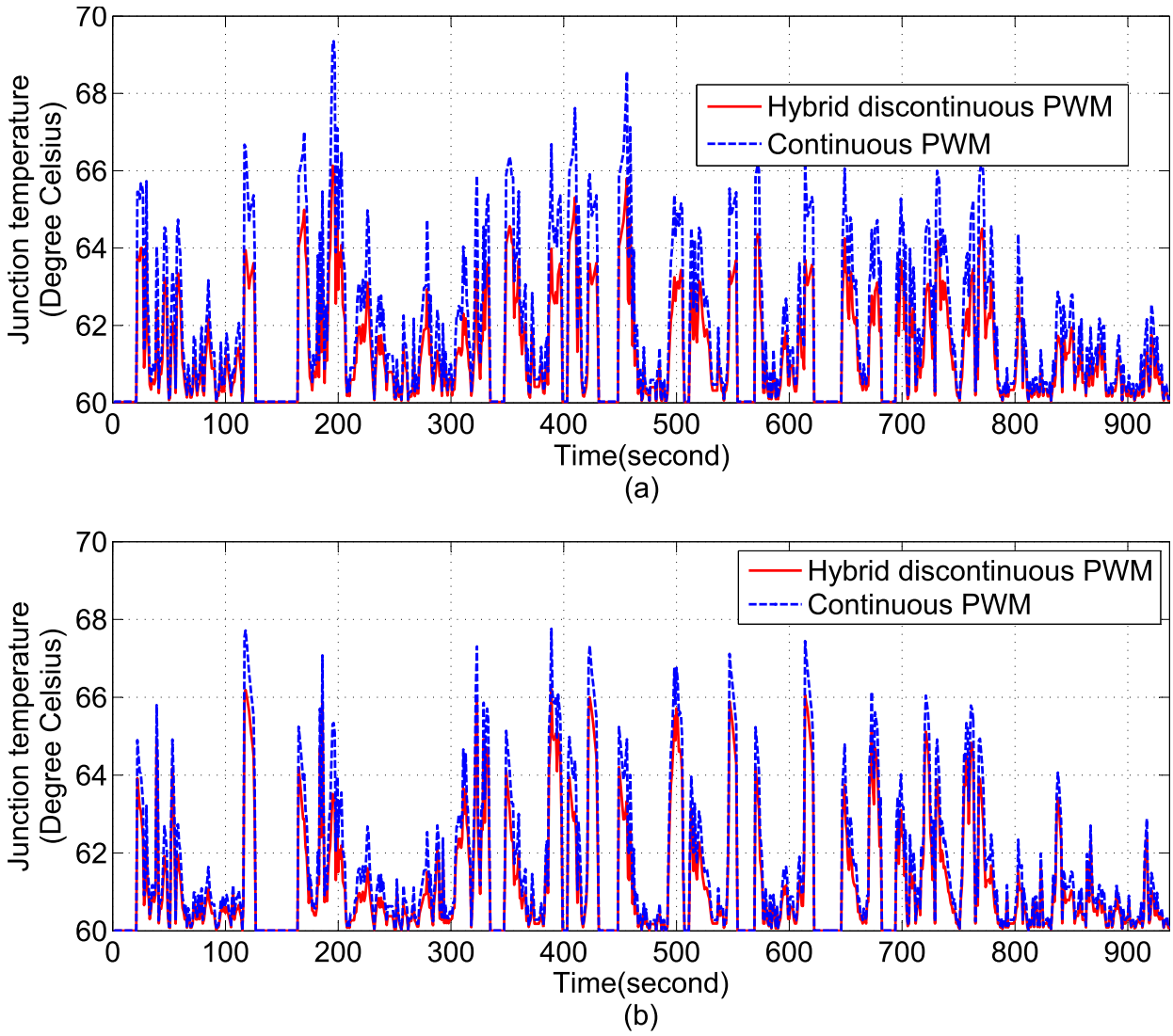


Figure 4.11 The junction temperatures of the inverter IGBT and diode for hybrid discontinuous PWM and continuous PWM in the first half of four consecutive FTP-75 driving cycles: (a) IGBT; (b) diode.

Table 4.7 Energy Consumption and Loss for Continuous PWM and Hybrid Discontinuous PWM in Four Consecutive US06 Driving cycles

Control Strategy	Energy consumption (10^7 Joule)	Energy loss (10^6 Joule)
Continuous PWM	1.3764	1.5061
Hybrid DPWM	1.3495	1.2165

Table 4.8 Failure Rates and MTTFs of SHEV's Power Electronic System for Variable Dc-Link Voltage Control in conjunction with Hybrid Discontinuous PWM in the Case of FTP-75

Reliability index	Inverter IGBT	Inverter diode	Dc/dc lower IGBT	Dc/dc upper diode	Dc/dc upper IGBT	Dc/dc lower diode	Dc-link capacitor	System
Failure rate (/10^6 hours)	0.7061	0.8656	1.2932	0.9840	1.4449	0.4756	0.000839	13.645
MTTF (10^5 hours)	14.163	11.553	7.7329	10.162	6.9207	21.026	11917	0.7329

Table 4.9 Failure Rates and MTTFs of SHEV's Power Electronic System for Variable Dc-Link Voltage Control in conjunction with Hybrid Discontinuous PWM in the Case of US06

Reliability index	Inverter IGBT	Inverter diode	Dc/dc lower IGBT	Dc/dc upper diode	Dc/dc upper IGBT	Dc/dc lower diode	Dc-link capacitor	System
Failure rate (/10^6 hours)	2.5140	2.1261	9.2238	4.0092	6.3845	4.4498	0.00084	51.925
MTTF (10^5 hours)	3.9777	4.7035	1.0842	2.4943	1.5663	2.2473	11900	0.1926

proposed methods are effective in reducing the losses of the SHEV's power electronic system and improving the reliability of the system.

Chapter 5

Fault-Tolerant Design of HEV's Powertrain

In the previous chapter, two control strategies have been presented to enhance the reliability of an SHEV's powertrain. Although reliability such as MTTF or availability can be enhanced by many solutions and failure rates can be minimized as low as possible, failure is inevitable during the mission time of systems. In some critical applications, malfunction either is unacceptable or would causes serious damages. Therefore, fault-tolerance is necessary in many power electronic systems. For electric drives utilized for EVs and HEVs, faults can be critical since an uncontrolled output torque may have an adverse impact on the vehicle stability, which ultimately can risk the passenger safety. Hence, a limping-home function is desirable [28]. In this chapter, a fault-tolerant design for SHEVs' powertrain is proposed and investigated.

5.1 Introduction

Hybrid electric vehicles (HEVs) with their competitive fuel economy have been considered as a pivotal technology to address concerns over the rapid rising of petroleum cost, increasingly worsening air pollution, and global warming associated with greenhouse gas emission [33]. A literature survey suggests that major research effort has been focused on power electronic converter topologies [49–51, 58–60], design and control of traction motors related to HEVs [61], energy storage unit and energy management [62–65], and control in the system level [66–68], while significantly

less attention has been devoted to the reliability and fault mitigation of HEVs' powertrains. In fact, aggregation of many power electronic devices into drive systems of vehicles may adversely affect reliability of the overall system [34, 35]. The reduced reliability of HEVs not only discounts fuel-saving premium, but also increases repair time and repair cost. In light of safety concerns, faults that occur in electric drives that are utilized as propulsion systems of HEVs can be critical since an uncontrolled output torque exerts much risk on the vehicle's stability, which can ultimately endanger the passengers' safety. Therefore, a fault-tolerant operation even with partial functionality that is commonly known as limping-home function is desirable [28].

The short-switch failure and the open-switch failure are the most common types of failure modes that compromise reliable operation of motor drive systems [19, 69]. This chapter compares and contrasts several existing alternative designs with short-switch and open-switch fault-tolerant capability employed in HEVs electrical machine driving systems in terms of performance and cost. In [70, 71], three-leg three-phase fault-tolerant inverter for motors with accessible neutral point are investigated. In this type of fault-tolerant inverter, the post-fault operation is implemented by reconfiguring the standard topology and regulating the currents in the remaining healthy legs in order to maintain the magnetomotive force (MMF) generated by the stator current unchanged. The limitation of this topology is that it requires access to the neutral point of the stator windings. A modified three-leg three-phase fault-tolerant inverter is developed for three-phase motors with three terminals [72–74]. Such three-leg fault-tolerant motor drive inverter features low part count. However, the dc-link capacitors have to be oversized in order to absorb large current at fundamental frequency of the load under faulted conditions. The post-fault power throughput is reduced to such an extent that it renders a long-term operation unfeasible. Four-leg three-phase fault-tolerant inverter topologies do not require available midpoint of dc-link or oversized dc-link capacitors [28, 72, 75–78]. A slight modification enables these four-leg inverter topologies to be applied to both three-terminal and four-terminal three-phase motors. Without oversizing the inverter, some of four-leg inverters can provide the same post-fault power throughput as the one under the healthy operating condition. The main drawback lies in the high component count of auxiliary devices

and the associated higher cost. The multi-phase motor drive inverter has inherent redundancy that can be utilized. But such a configuration is only suitable for motors with a particular design structure, which will exclude its applicability to general motor drive systems [79]. The authors of [80] present a cascaded inverter topology that have inherent fault-tolerant capability due to the redundancy of the switching states. However, similar to multi-phase inverter, this fault-tolerant topology is also only suitable for motors with special structure. Some modified matrix converter and multilevel converters feature superior fault-tolerant capability [29,81,82]. However, these high power converters are not suitable for application of HEVs.

Two implementations of a fault-tolerant topology of electric drive system for series hybrid electric vehicles (SHEVs) are proposed in this chapter to overcome the limitations that are associated with the existing topologies. Based on performance metrics proposed in [83], the new topology can obtain the post-fault operation at rated power throughput with the silicon-cost increase by 64% percent and seven fuses or relays compared with the standard topology.

5.2 Operating Principles of the Fault-tolerant Powertrain Topology

A standard SHEV drive system consists of a three-phase rectifier, a three-phase inverter and a bidirectional buck/boost dc/dc converter. Due to the lack of redundancy, any fault on any power device can cause the system to shut down. A fault-tolerant drive system for SHEVs is proposed to reduce unexpected stoppages caused by faults of semiconductor devices. As shown in Fig. 5.1, the newly proposed system is composed of a standard SHEV powertrain, a redundant phase leg, connecting devices, and fault-isolating components. The backup phase leg formed by S_{rp} and S_{rn} provides redundancy not only to the motor-drive inverter, but also to the rectifier and the buck/boost converter. Under the condition of open-switch or short-switch failure of any switch in these three converters, the system can maintain an uninterruptible and long-term post-fault operation without compromising the power throughput. Since these three converters share the same single redun-

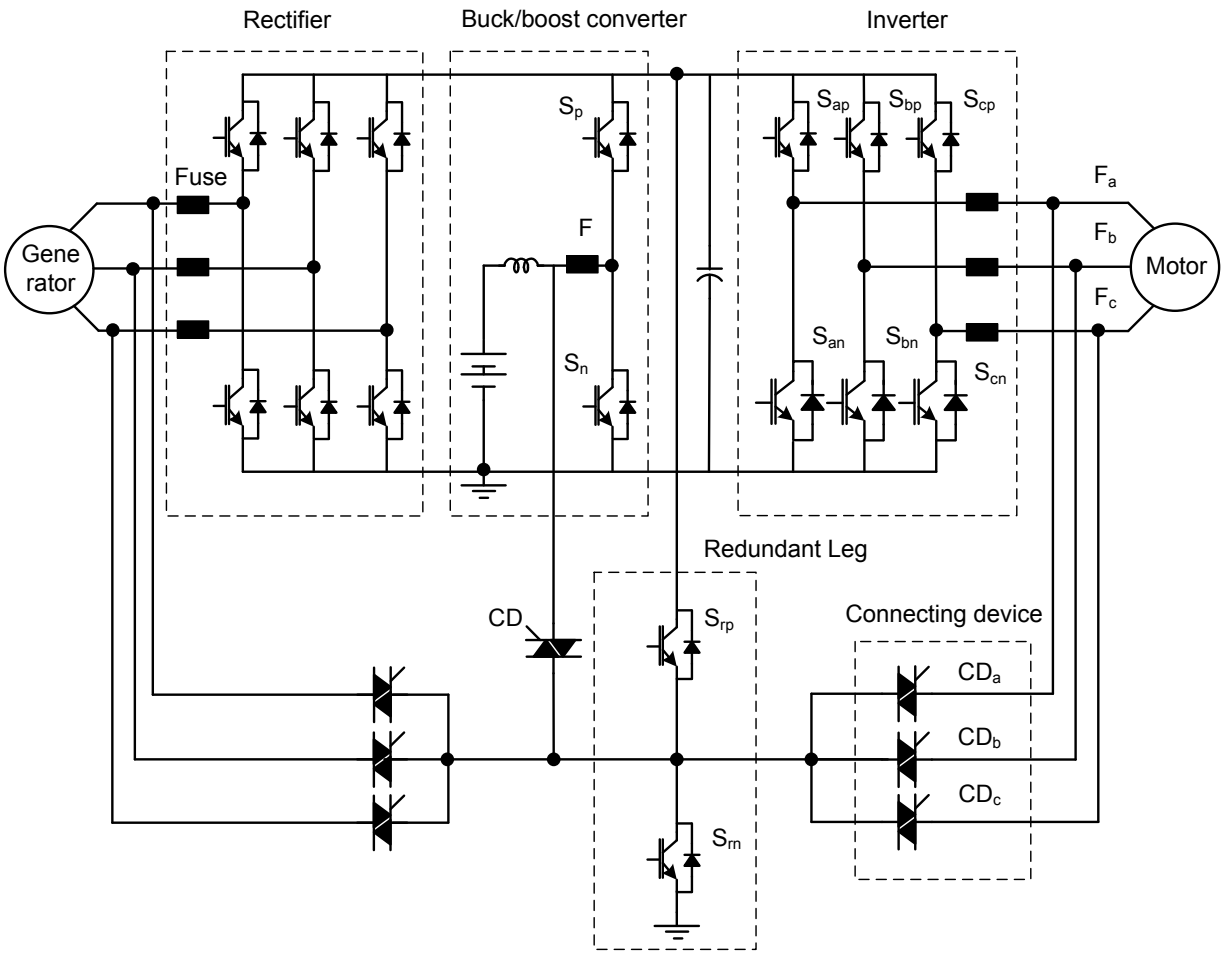


Figure 5.1 Schematic of the proposed fault-tolerant SHEV powertrain.

dant leg, the cost of the system is relatively lower in comparison to other four-leg fault-tolerant inverters that have been reported in literature for motor drives. The detailed operation principle and reliability performance are presented as follows.

5.2.1 Isolating and Connecting Devices

The short-switch fault is one of the most common types of motor drive inverter faults. In the case of a short-circuit failure of any switch, one phase of the stator windings will be directly connected to the positive or negative rail of the dc bus, which results in the pulsating electromagnetic torque. A device is needed to isolate the faulted switch from the rest of the overall system. Herein, a fast-acting fuse is utilized to fulfill this function. For instance, upon a short-circuit failure of the upper

switch S_{ap} of the a-phase leg, the a-phase of the stator windings will be directly connected to the positive rail of the dc bus, as shown in Fig. 5.1. The resultant a-phase current will be unable to regulate. Further remedial measures cannot be employed to restore the system to normal operation until this fault is successfully isolated by the fuse F_a.

Since the inverter, the rectifier and the buck/boost converter share the same backup leg, connecting devices are necessary to connect the redundant leg to the output terminals. These connecting devices need to block bidirectional voltage and conduct alternate current. Under post-fault operating conditions, the connecting devices for the inverter and the rectifier commutate at fundamental frequency. Therefore, low-speed low-cost ac switches will suffice to handle this task. Although the buck/boost converter may operate in discontinuous mode and consequently the connecting device has to commutate at higher switching frequency, the same low-speed ac switch can still be applied, due to the inherent zero-current turn-off characteristic of the discontinuous-mode buck/boost converter. Herein, TRIACs or anti-paralleled double-thyristors are used to connect the backup leg to the poles of the three converters in the standard SHEV powertrain.

5.2.2 Open-Switch Fault and Control Strategy

The new SHEV drive system can squarely handle open-circuit or misfiring faults in one or two IGBTs in the same leg of the three converters. When only one power device fails, the key to achieving the fault-tolerant operation is to isolate the faulted component and then reconfigure the structure and control strategy of the drive system. The specific control scheme is elaborated as the following for the failure in the switch S_{ap} of the inverter.

Fault isolation is implemented by disabling the gating signals to both the faulted and the non-faulted switches S_{ap} and S_{an} in the a-phase leg with reference to Fig. 5.1. Then the connecting ac switch CD_a is activated, and the gating signals of the faulted leg are subsequently routed to the two corresponding redundant switches S_{rp} and S_{rn}. As a result, the load current i_a that originally flowed through the faulty leg is diverted to the redundant one. Since this actuation does not fundamentally change the topology of the converters (rectifier, inverter or buck/boost

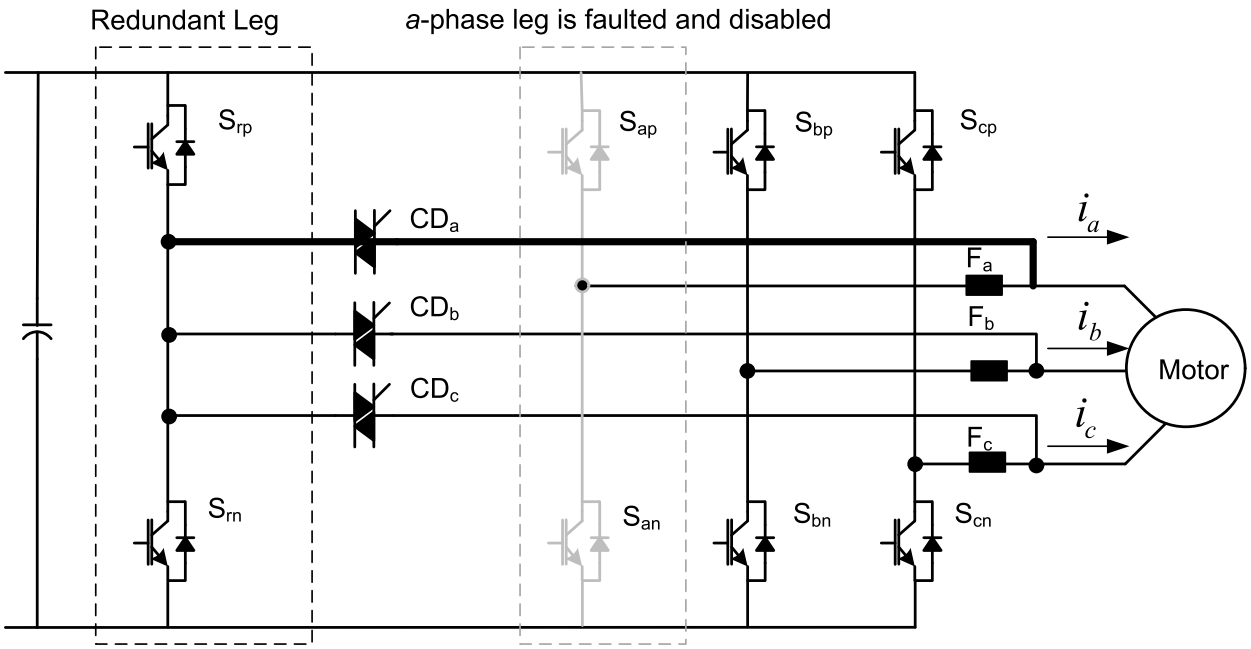


Figure 5.2 Power circuit of the dc/ac part after its a-phase leg is faulted.

converter), pulse width modulation (PWM) techniques and control algorithms remain unchanged. The only operational alternation amounts to the additional conduction loss of an ac switch. Fig. 5.2 shows the reconfigured power circuit of the dc/ac inverter after one switch of its a-phase leg fails in open-circuit mode. After the redundant leg replaces the faulty a-phase leg, the post-fault topology is identical to the standard three-phase inverter bridge except for the addition of the connecting device CD_a. The same control strategy can be applied to open-circuit failures with other switches.

5.2.3 Short-Switch Fault and Control Strategy

Unlike the open-circuit faults, it is relatively more involved to handle short-circuit faults in general due to additional provision of fault isolation. Different schemes are employed depending on the fault location.

If a short-circuit fault happens to an upper or lower switch of the inverter or the rectifier, the complementary switch in the same leg is blocked by a constant turn-off gating signal. The time delay between the detection of the fault and the blockage of switching devices are minimal since the logic is implemented through hardware. Then the corresponding connecting TRIAC and the

lower or upper switch in the backup leg are activated if the short-circuit fault occurs to the upper or lower switch, respectively, in the faulted phase leg. Thus a shoot-through loop is formed, which consists of one switch in the redundant phase leg, the faulted switch and the dc-link capacitors. Fig. 5.3 illustrates the shoot-through loop marked by the bold line in the case of a short-switch fault in a-phase upper switch S_{ap}. The resultant large inrush current in the shoot-through loop will clear the fuse F_a of the faulted phase. After the fuse F_a successfully isolates the faulted phase leg from the rest of the system, the original gating signals for S_{ap} and S_{an} are applied to S_{rp} and S_{rn} in the backup leg. The control strategy for the post-fault operation is the same as the case of the open-switch faults.

If a short circuit happens to the upper switch S_p of the buck/boost converter during buck-mode operation, the battery pack is connected to the positive rail of the dc bus through the inductor. As a result, the large battery charging current will clear the fuse F. In the case of a short-circuit fault in the lower switch S_n during boost-mode operation, the battery is shorted to the negative rail of the dc bus through the inductor. The resultant larger-than-normal discharge current clears the fuse F. Once the faulted switch is isolated, the connecting device CD is activated, and the control signals are applied to the backup leg. No further change is needed.

5.2.4 Design Rule for Power Devices

The selection and sizing of the power devices in the three standard converters is based on electrical and thermal stresses under normal operating conditions, which are the same as the methodology used for design of other power electronic converters. The current, voltage, and i^2t ratings of the fuses should be designed according to normal operating conditions. For the connecting devices TRIACs and the switches in the redundant leg, these semiconductor devices not only should meet electrical and thermal requirements, but also have to have i^2t that is higher than the fuse.

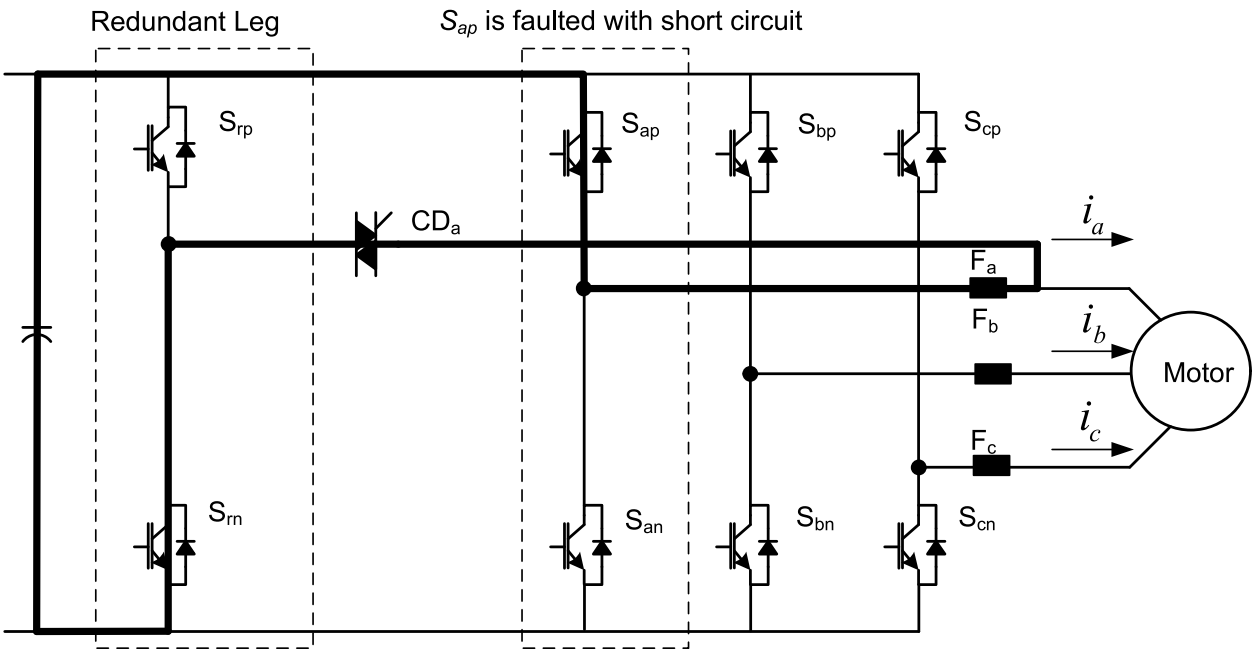


Figure 5.3 The shoot-through path to blow out the fuse F_a after the a-phase top switch S_{ap} of the inverter fails in short-circuit mode.

5.2.5 Alternative Implementation of the Fault-Tolerant Powertrain

The limitation of the aforementioned fault-tolerant design lies in the fact that the IGBTs in the backup leg and the TRIACs need to be oversized since their i^2t has to be higher than that of the fast-acting fuses. An alternative implementation of the proposed fault-tolerant design of SHEV powertrain is derived to overcome the aforementioned disadvantage. The alternative implementation is almost identical to the first one except that the fault-isolating fuses are replaced by seven ac switches, as shown in Fig. 5.4. These ac switches can be relays, TRIACs or other types of solid-state switches.

The fault-tolerant solution shown in Fig. 4 features the unified fault isolation scheme for both short-circuit and open-circuit faults. The control strategy is briefly explained as follows. Once a fault in a switch is detected, the gating signals of the faulted and the healthy switches in the faulted leg are immediately disabled to prevent fault propagation. Then the corresponding ac switch is turned off to isolate the faulted leg from the rest of the system. Upon successful isolation of the fault, the corresponding connecting device is permanently triggered and the original gating signals

of the faulted leg are routed to the corresponding switches in the redundant leg. Therefore, the redundant leg fully replaces the faulted leg and the system transits to post-fault operation that has the normal performance. The transition process of the system in the case of a fault is further illustrated with a short-switch failure to the top switch S_{ap} in the a-phase leg. When the short-circuit failure of the switch S_{ap} is detected, the controller immediately disables the gating signals of both switches S_{ap} and S_{an}. In the meantime, the ac switch S_a is turned off and the connecting device CD_a is turned on. Then the original gating signals of S_{ap} and S_{an} are utilized to control the switches S_{rp} and S_{rn} in the redundant phase leg. The normal operation of the drive system is resumed. The same transition steps can be applied to open-circuit faults of switches and faults of switches in other phase legs and other converters.

5.3 Fault Diagnosis

Fault detection and identification are two important steps to prevent fault propagation and to maintain proper post-fault operation of the system. Various solutions to fault diagnosis of the inverters in motor drives have been proposed [84–86]. These methods can be classified into two categories. The first category is mainly based on the analysis of the inverter output currents, which features low cost and low speed. Another category involves gate drive signals, voltage and current across/through the switches for fault diagnosis. The latter can accomplish fault detection within one to several switching cycles. The former ac-based detection methods are not suitable for diagnosis of short-switch faults since over one fundamental cycle is needed to identify a fault or the location of the faulted device. These methods are not suitable for the buck/boost converter either. Nowadays, the smart drivers of IGBTs often have embedded voltage-sensing and current-sensing circuits, which reduce complexity and cost.

Herein the second solution is adopted for fault identification. However, the proposed method in this thesis differs from the existing methods that are based on the gating signals and collector-to-emitter voltages of IGBTs [87]. In practical applications, it is a non-trivial and even challenging

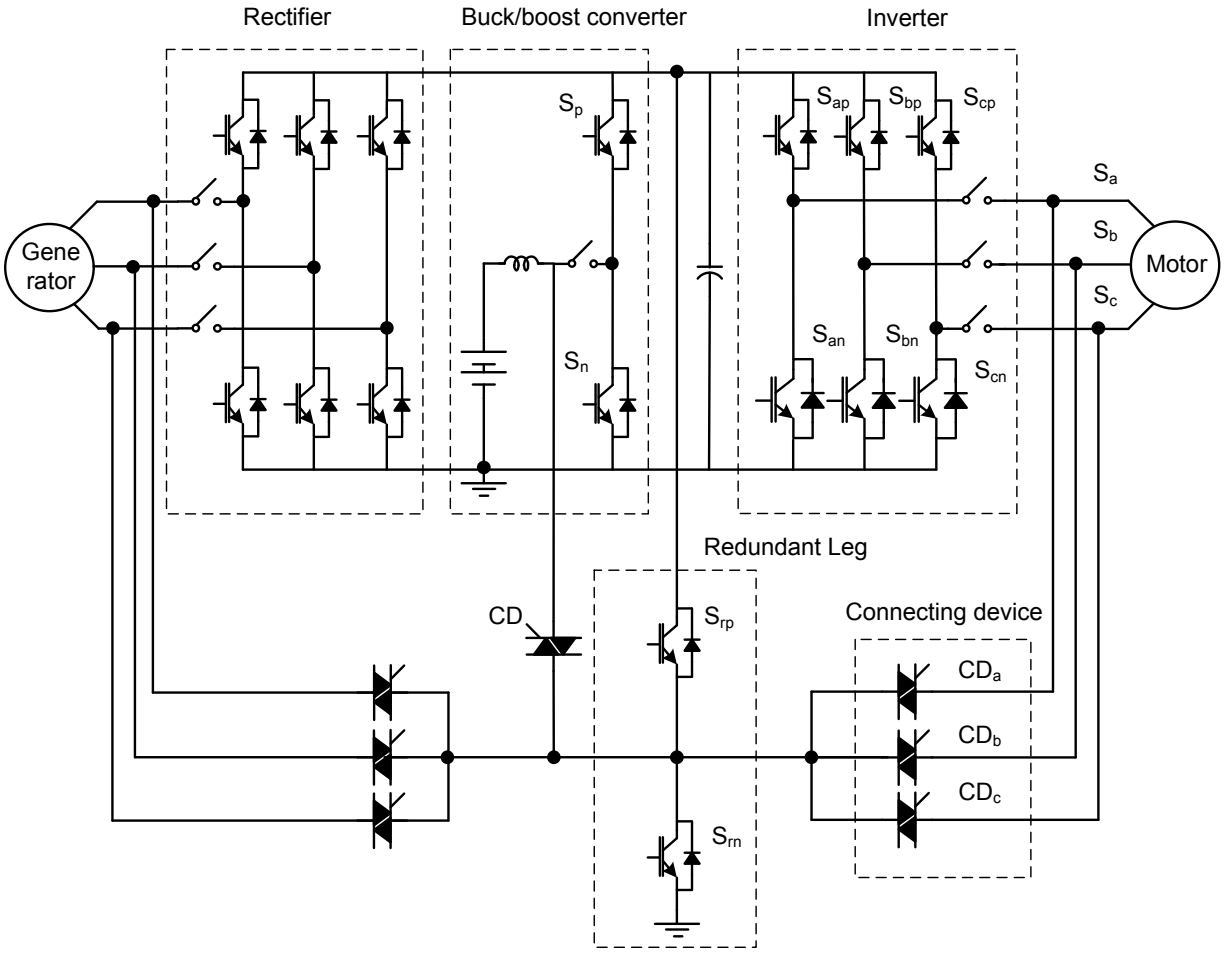


Figure 5.4 Illustration of the alternative implementation of the proposed fault-tolerant topology by replacing fuses in Fig. 5.1 with switches.

task to distinguish a short-switch fault from normal operating state of switches for two reasons. The first one is that the collector-to-emitter voltage V_{ce} of the faulted IGBT depends on its short-circuit resistance and the on-state resistance of the non-faulted switch in the faulted leg. Therefore, the voltage V_{ce} is not a reliable indicator of short-switch fault due to uncertainty associated with the short-circuit resistance of IGBTs. The other difficulty is that the collector-to-emitter voltages of some switches may not be constant in certain application. Hence, it is difficult to set a threshold to distinguish between low-level and high-level voltages of a switch. An example of such application is an inverter with variable dc-link voltage. Therefore, a current-based diagnosis method for short-switch fault that is reliable and simple to implement has been proposed and verified in experiments. Its principle will be illustrated as follows.

Table 5.1 shows the logic of fault diagnosis for the upper switch S_{ap} in the a-phase leg of the inverter. Herein IGBTs are assumed switches. It is worth noting that in Table 5.1, the fault diagnosis is based on the current through the IGBT that excludes the current of the anti-parallel diode. The principles of the diagnosis method are elaborated as follows. If the gating signal to a switch is at low level, while the sensed current through the switch is at high level, a short-circuit failure is thus asserted. In order to avoid false detection caused by the turn-off delay of IGBTs, the gating signal of the lower switch S_{an}, which is complementary to that of the upper switch S_{ap}, is utilized to detect short-switch faults. For conventional short-circuit protection, the design of the threshold of the current is a challenging task. A lower threshold for short-circuit detection logic will increase sensitivity of detection circuit but may lead to high possibility of misjudgment. On the contrary, while raising the threshold enhances the reliability of the fault diagnosis, the fault detection circuit is less sensitive to faults and a large inrush current may be generated before the short-circuit protection actuates.

The proposed diagnosis method for short-switch fault will function properly within a wide threshold range as explained in the following. The proposed diagnosis logic for short-circuit faults is based on the fact that the current through a switch (IGBT) should be zero when the gating signal of the switch is at low level and that a short-circuit fault is certain if the switch current is non-

Table 5.1 Fault Detection Logic of S_{ap}

Gating signal of S_{ap}	/	High
Gating signal of S_{an}	High	/
Collector-to-emitter voltage of S_{ap}	/	High
Collector current of S_{ap}	High	/
Fault detection	Short-switch fault	Open-switch fault

zero given a low-level gating signal. Therefore, the current threshold can be much lower than the maximum operating current under normal operating condition. The effectiveness of the method is not affected by load conditions. For instance, in light-load condition or the neighborhood of the load current's zero-crossing point, the current flowing through the switch will still increase to the threshold of short-circuit fault diagnosis circuit in the case of short-switch fault. Since the switches are identical, the scheme of fault diagnosis can be applied to other switches as well.

The diagnosis logic for open-switch fault is based on the gating signal and the collector-to-emitter voltage V_{ce} of a switch (IGBT). The open-circuit fault that occurs to the upper switch S_{ap} of the a-phase leg is taken as an illustrative case. Under the normal operating condition, when the gating signal to S_{ap} is high, the voltage V_{ce} across the switch S_{ap} must be at low level. Otherwise, if the voltage V_{ce} of the switch S_{ap} is at high level when its gating signal is at high level, an open-circuit fault is certain to occur to S_{ap}. An open-switch fault is asserted.

5.4 Reliability Analysis of the Fault-Tolerant SHEV Powertrain

The reliability of the system is closely related to the repair cost and repair time since higher reliability of the system will amount to less maintenance. This section quantitatively assesses the reliability of the proposed and the standard SHEV drive systems. In the assessment of the new drive system's reliability improvement, only semiconductor devices IGBTs and TRIACs are con-

sidered to demonstrate the methodology although inclusion of other passive components is rather straightforward.

5.4.1 Components Failure Rates

The reliability handbook MIL-217F [2] provides an extensive database of various types of parts. Therefore it is widely accepted and frequently utilized to determine reliability of various electronic equipment. In order to make use of the failure rate models of components from the handbook, the following operating conditions have been assumed:

1. The power ratings are 100 kW for the inverter, 70 kW for the rectifier, and 30 kW for the buck/boost converter.

2. The dc-link voltage is 250-600 V, and therefore devices with the rating of 1200 V/600 A are selected.

3. The junction temperature of devices is 150 $^{\circ}$C.

4. Reliability of IGBTs and TRIACs are considered.

5. Failure rates of components in inactive mode equal zero.

The reliability model of TRIAC is determined by

$$\lambda_{SCR} = \lambda_b \pi_T \pi_R \pi_S \pi_Q \pi_E \tag{5.1}$$

where

λ_b: Base failure rate;

π_T: Temperature factor;

π_R: Current rating factor;

π_S: Voltage stress factor;

Table 5.2 Failure Rates OF Components

Component	Failure rate	Unit
IGBT	7.236	Failures per 10^6 hours
TRIAC	0.8735	

π_Q: Quality factor;

π_E: Environmental factor.

The MIL-HDBK-217F contains no reliability data about IGBTs. In consideration of the similarity between the internal structures of IGBTs and MOSFETs, the failure rate model of MOSFTs is chosen to estimate failure rates of IGBTs. Hence, the failure rate of IGBTs can be expressed as

$$\lambda_{IGBT} = \lambda_b \pi_T \pi_A \pi_E \pi_Q \tag{5.2}$$

where π_A is application factor while the other parameters have been explained in equation (5.1).

Based on the assumed operating conditions, known environmental and application conditions, the failure rates of IGBT and TRIAC are evaluated and listed in Table 5.2.

5.4.2 Reliability Evaluation of the SHEV Driving System

Markov reliability model is adopted to assess the reliability of the fault-tolerant SHEV drive system. In order to reduce the order of the state equation, all devices with the same operating states and transition processes are treated as one subsystem. The system can be divided into two subsystems: one including all IGBTs and the other including all TRIACs. Repair processes have not been considered in this study. The system has three states:

State 0: All devices in the three converters of the standard drive work normally, and the redundant and connecting devices are in inactive mode;

State 1: One IGBT fails, and the redundant leg and correspondent connecting device TRIAC are activated;

State 2: Two components (IGBTs or the combination of a TRIAC and an IGBT) fail, and the system shuts down.

The state transition diagram of the system is illustrated in Fig. 5.5. A short-switch or open-switch failure of any one of the IGBTs in the rectifier, the inverter or the buck/boost leads to transition of the system to State 1 from State 0. Since all IGBTs are assumed to have the same junction temperature, the transition rate α_{01} is the sum of failure rates of all operating IGBTs. Transition between State 1 and State 2 are triggered by a failure of one IGBT in remaining healthy and the redundant legs or the TRIAC that is in active mode. The transition rate α_{12} comprises the failure rates of operating IGBTs and TRIAC. It is worth noting that only one TRIAC operates in State 1.

From (2.11), the state equation of the SHEV system can be obtained as

$$\frac{d}{dt}\begin{bmatrix} P_0(t) \\ P_1(t) \\ P_2(t) \end{bmatrix} = \begin{bmatrix} -\alpha_{01} & 0 & 0 \\ \alpha_{01} & -\alpha_{12} & 0 \\ 0 & \alpha_{12} & 0 \end{bmatrix} \begin{bmatrix} P_0(t) \\ P_1(t) \\ P_2(t) \end{bmatrix} \tag{5.3}$$

With the assumption that the probabilities that the system is in the functional states at time t, the reliability of the system can be obtained as

$$R(t) = P_0(t) + P_1(t) \tag{5.4}$$

Fig. 5.6 illustrates the reliability functions of the proposed fault-tolerant powertrain and the standard SHEV powertrain. It is evident that the reliability of the proposed drive system is substantially higher than that of the standard one due to the presence of the redundant phase leg.

The mean time to failure ($MTTF$) is another important index indicating the reliability of a system, which is related to the reliability function by the following.

$$MTTF = \int_0^{+\infty} R(t)dt \tag{5.5}$$

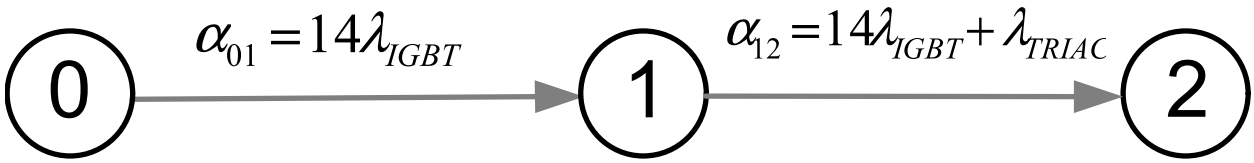


Figure 5.5 State transition diagram of the proposed SHEV powertrain.

Table 5.3 MTTF OF the Proposed and Standard SHEV Powertrains

Topology	MTTF
Standard powertrain	9.871×10^3 hours
Proposed powertrain	1.966×10^4 hours

In Table 5.3, $MTTF$s of the new fault-tolerant and the standard SHEV drive trains are listed. The significantly improved $MTTF$ demonstrates the superior reliability performance of the new topology. The operating time of the proposed fault-tolerant topology has been improved twice as much as that of the standard SHEV drive system.

5.5 Simulation Results

The post-fault operating performance of the proposed SHEV driving system is verified by time-domain simulation by use of Saber^{TM}. The simulation is based on the fault-tolerant design of SHEV powertrain as shown in Fig. 5.4. Because the fault diagnosis scheme and post-fault remedial strategy are identical for the inverter, the rectifier and the buck/boost converter, only the faults on the dc/ac inverter that directly drives the motor and the corresponding post-fault performance are investigated. The simulated system model consists of the proposed fault-tolerant three-phase inverter and an resistance-inductance load. The detailed specification and parameters of the system are tabulated in Table 5.4. Fig. 5.7 shows the transition process of the system from the normal operating condition to short-switch fault condition of the inverter. At the instant of 0.05 s, a short-

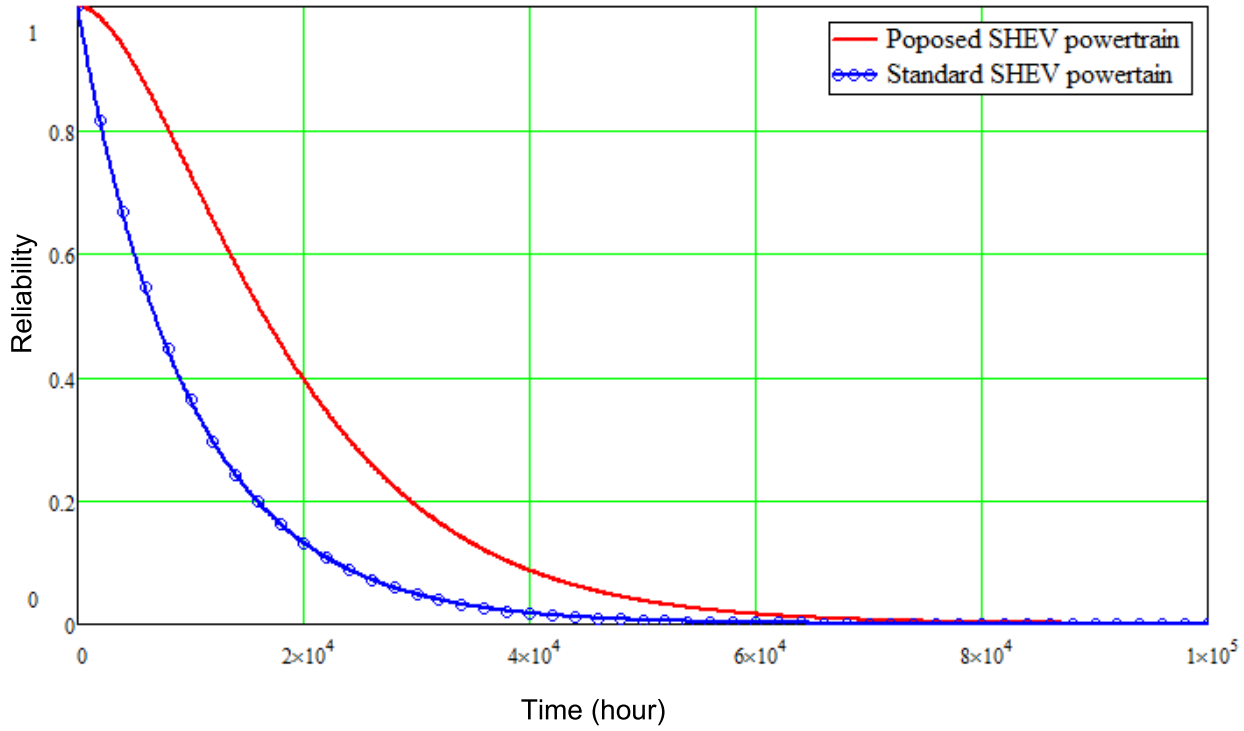


Figure 5.6 Reliability functions of the proposed and standard SHEV powertrains.

switch fault occurs to the top switch S_{ap} of the a-phase leg. A much-larger-than-normal current through the faulted device substantially results. The immediate remedial action should be taken to avoid fault propagation. It further verifies that the slow-acting fault-diagnosis methods based on the output current or voltage of the inverter are not suitable for identifying short-switch fault.

The fault-detection method presented in this section features a very short delay of approximate 1 μs that is caused by the analog components and a low-pass filer in the fault-detection circuit. At

Table 5.4 Specification and Parameters of Simulation Model

Parameter	Value
DC-link voltage	55 V
Fundamental frequency	60 Hz
Switching frequency	5 kHz
Modulation index	0.8
Load resistance	5 Ω
Load inductance	9 mH

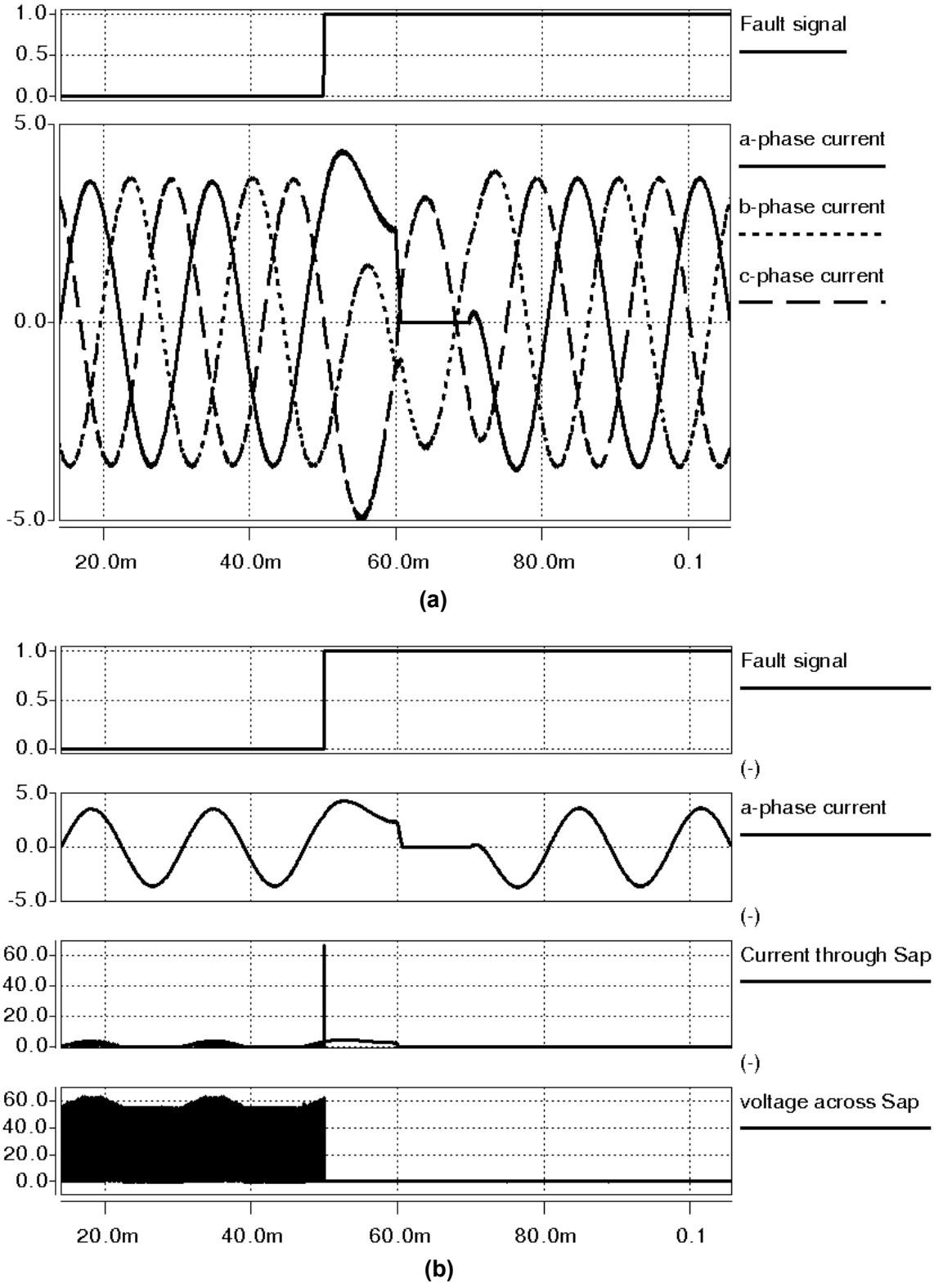


Figure 5.7 Simulation results based on the second fault-tolerant topology in case of short-switch fault of S_{ap}: (a) the fault signal and the three-phase load currents; (b) the fault signal, the load current of the faulted phase, the current through the faulted switch, and the voltage across the faulted switch.

time instant t = 50 ms, a short circuit occurs to S_{ap}. Once the fault is detected, the gating signal of the bottom switch S_{an} in the a-phase leg is disabled and the large current flowing through the faulted leg during the interval of fault is immediately terminated, as shown in Fig. 5.7. Then the isolating device S_a is controlled to be open, and the connecting device CD_a is triggered. At time instant t = 60 ms, the relay S_a is fully disconnected. And in another delay of about 10 ms, the original gating signals to both switches of the faulted leg are routed to the corresponding switches of the backup leg at t = 70 ms. Herein, the delay between time instants t = 60 ms and t = 70 ms is inserted to guarantee that the relay is fully disconnected before the redundant leg participates in operation of the system. Otherwise, the bottom switch S_{rp} in the redundant leg and the faulted switch S_{ap} will form a shoot-through path. The post-fault operation starts and normal system performance is resumed from t = 70 ms.

The transition process of the open-switch fault is illustrated in Fig. 5.8. The fault isolation actions taken by the controller are the same as the ones for the case of the short-switch fault except that the fault-detection logic is different, which has been explained in Section 5.3.

5.6 Experimental Results

A prototype of a three-phase inverter based on the fault-tolerant topology as shown in Fig. 5.4 has been built. The parameters of power circuit are the same as those of simulation model, as shown in Table 5.4. IGBTs and relays are used as main switches and fault-isolating devices, respectively.

The process of the detection and isolation of the short-switch fault and the reconfiguration of the inverter is illustrated in Fig. 5.9. At the rising edge of the fault signal, the gate-to-emitter voltage of the top switch S_{ap} in the a-phase leg is forced to be constantly high, so that the short-switch fault occurs. After a turn-on delay of 400 ns, the switch S_{ap} is completely turned on and a short-circuit path consisting of dc-link capacitors, the two switches in the a-phase leg forms. As a result, the current through S_{ap} rises dramatically. After a delay of 1 μs that is mainly caused by the response times of a comparator and a low-pass filter in the fault-detection circuit, the fault is

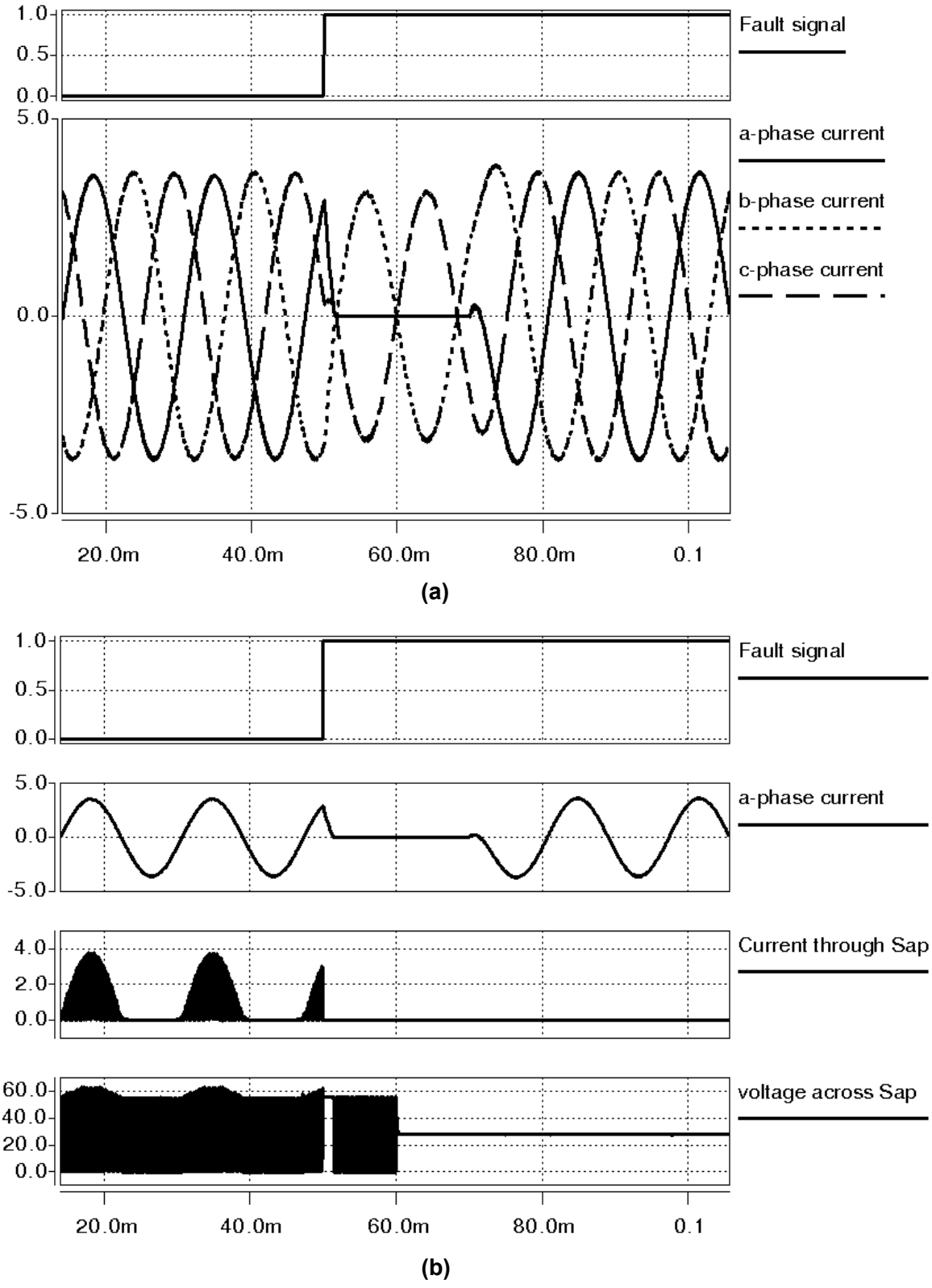


Figure 5.8 Simulation results based on the second fault-tolerant topology in case of open-switch fault of S_{ap}: (a) the fault signal and the three-phase load currents; (b) the fault signal, the load current of the faulted phase, the current through the faulted switch, and the voltage across the faulted switch.

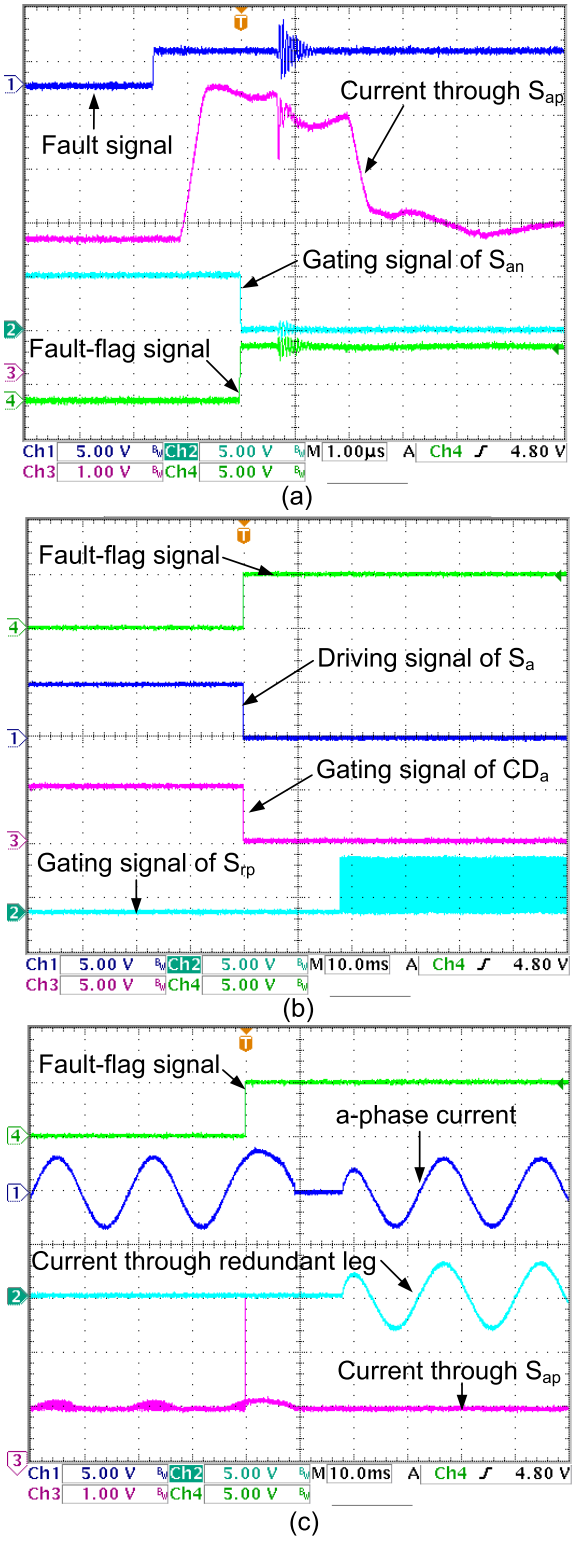
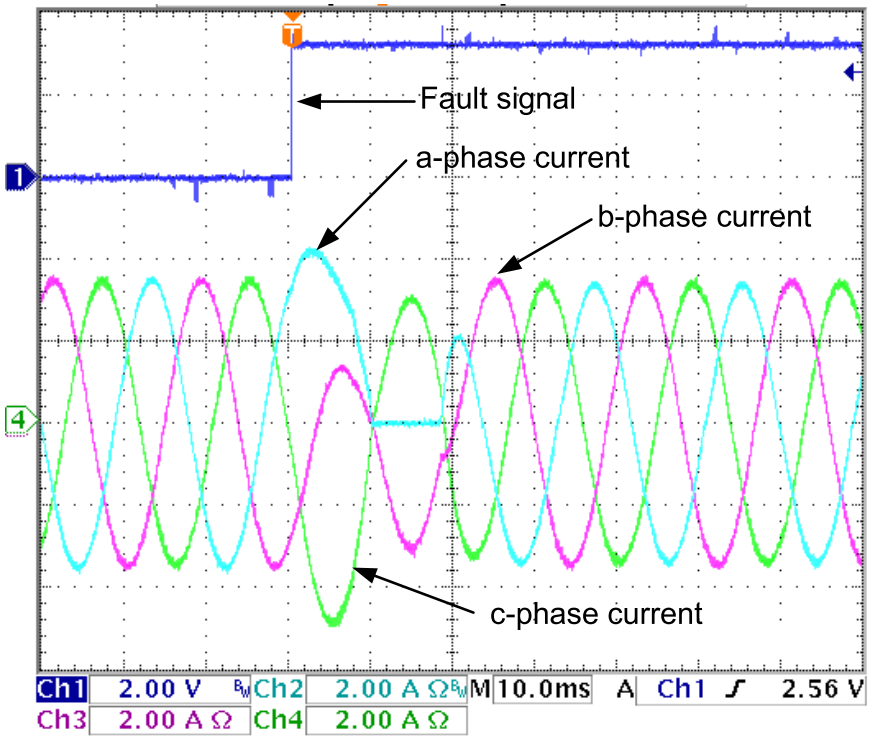


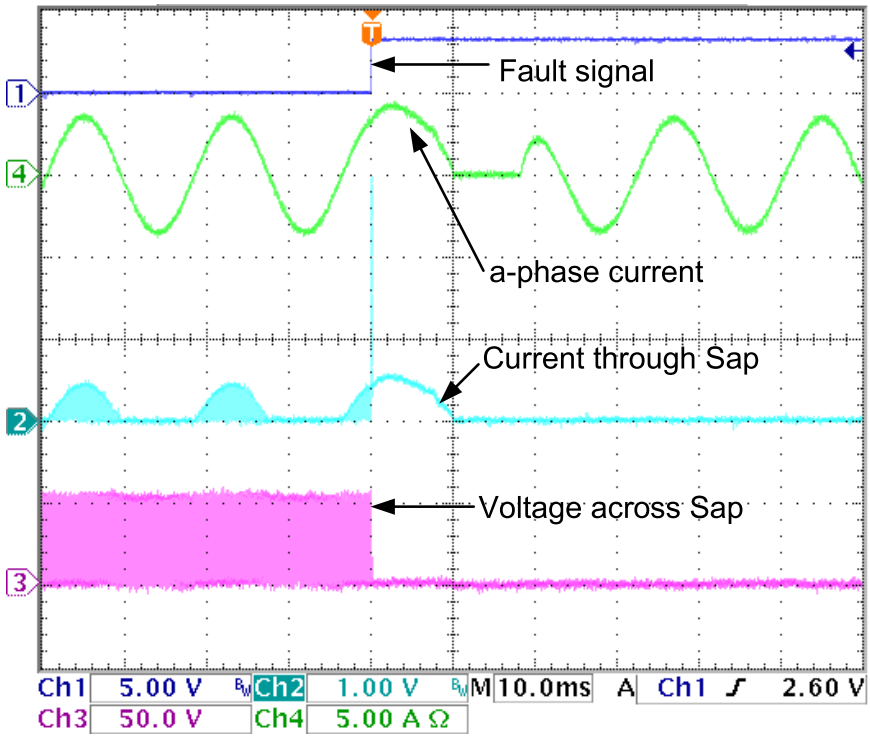
Figure 5.9 Fault detection and isolation based on the second fault-tolerant topology in case of short-switch fault of S_{ap}: (a) fault signal, sensed current through S_{ap}, gating signal of S_{an}, and fault-flag signal; (b) fault-flag signal, driving signal of the relay S_a, gating signal of the TRIAC CD_a, and gating signal of the upper switch S_{rp} in the redundant leg; (c) fault-flag signal, a-phase current, current through the redundant leg, and sensed current through S_{ap}.

detected by the controller and a fault flag is signaled. At the same time, the gating signals to the switches in the faulted leg are immediately disabled in order to avoid fault propagation, as shown in Fig. 5.9(a). Once the fault is detected, the controller starts reconfiguring the inverter. Firstly, the fault isolating component S_a and the connecting device CD_a are triggered. It should be noted that the connecting device has to be turned on before the isolating component is fully disconnected; otherwise an overvoltage generated by the inductive load current will damage the isolating component or other components. A solution to this problem is to insert a sufficient delay time between triggering the connecting device and energizing the isolating component. In the prototype, relays with the release time in the scale of several milliseconds and TRIACs with the turn-on time in the scale of one hundred microseconds are used as isolating components and connecting devices, respectively, therefore the delay time is not required. In order to avoid the shoot-through fault formed by the faulted switch S_{ap} and the switch S_{rn} in the redundant leg, the relay should be firstly disconnected before the redundant leg is activated. Since it takes several milliseconds for the relay to fully disconnect, a delay time of about 20 ms is inserted between energizing the relay and engaging the redundant leg. Then, after the delay time, the original gating signals to the switches in the a-phase leg are routed to both corresponding switches in the redundant leg. The process is clearly demonstrated in Fig. 5.9(b). Once the inverter successfully reconfigures, the normal system operation resumes. As shown in Fig. 5.9(c), the a-phase current flows through the redundant leg after the fault and the faulted leg is isolated from the remaining system.

The other salient waveforms during the period of a short-switch fault are illustrated in Fig. 5.10. The waveforms of the fault signal and three-phase load currents are shown in Fig. 5.10(a). It can be observed that the a-phase current increases and has a quasi-sinusoidal waveform after the fault. This is caused by the turn-off delay of the relay S_a. After the fault, the bottom switch S_{an} is turned off, and the top switch S_{ap} is shorted. As a result, the a-phase load is directly connected to the positive rail of the dc bus and the a-phase load current increases. When the relay S_a is completely disconnected, the faulted leg is isolated from the system, and the a-phase load current decreases to zero, as shown in Fig. 5.10(a). After a delay of approximate 10 ms, the original gating



(a)



(b)

Figure 5.10 Experiment results based on the second fault-tolerant topology in case of short-switch fault of S_{ap}: (a) fault signal, a-phase current, b-phase current, and c-phase current; (b) fault signal, a-phase current, sensed current through S_{ap}, and voltage across S_{ap}.

signals to the switches S_{ap} and S_{an} in the faulted leg are routed to the switches S_{rp} and S_{rn} in the redundant leg, respectively. Subsequently the post-fault operation starts. It can be observed that the inverter experiences a disturbance for 20 ms in the case of a short-switch fault, which has no significantly negative effect on the traction system of SHEVs since the mechanical system has much slower response than the electrical system. Fig. 5.10(b) shows the waveforms of the collector current and collector-to-emitter voltage of the faulted switch S_{ap}. Although at the instant of the short-switch fault the current flowing through the switch S_{ap} is much larger than that under normal operating condition, the short-circuit fault only lasts less than 4 μs.

The fault detection process for the open-switch fault is shown in Fig. 5.11. The strategy of the fault detection, isolation and system reconfiguration for the open-switch fault is the same as the one applied to the short-switch fault except that the fault detection logic is based on the gating signal and the collector-to-emitter voltage of the IGBTs. Fig. 5.12 illustrates the transition process of the system in the case of the open-switch fault in the switch S_{ap}. It can be observed that the inverter also only experiences a disturbance for approximate 20 ms during the interval when the system transits to the post-fault state. In fact, for open-switch fault, the transition period can be greatly reduced by optimizing the control strategy. The improved control strategy is that regardless of the fault isolating device the original gating signals of both switches in the faulted leg are immediately routed to two switches of the redundant leg once the gating signals of the switches in the faulted leg are disabled. Therefore the delay time caused by turning off the relay is substantially shortened.

5.7 Summary

A fault-tolerant powertrain for SHEVs with two different implementations has been proposed. The operating principles and performance have been analyzed in detail. The new drive system features nearly disturbance-free operation of the HEVs in case of open-switch and short-switch faults. Therefore, the vehicle safety has been improved. Moreover, the superior post-fault operating performance allows the vehicle to operate over a sustained long period of time after faults. The

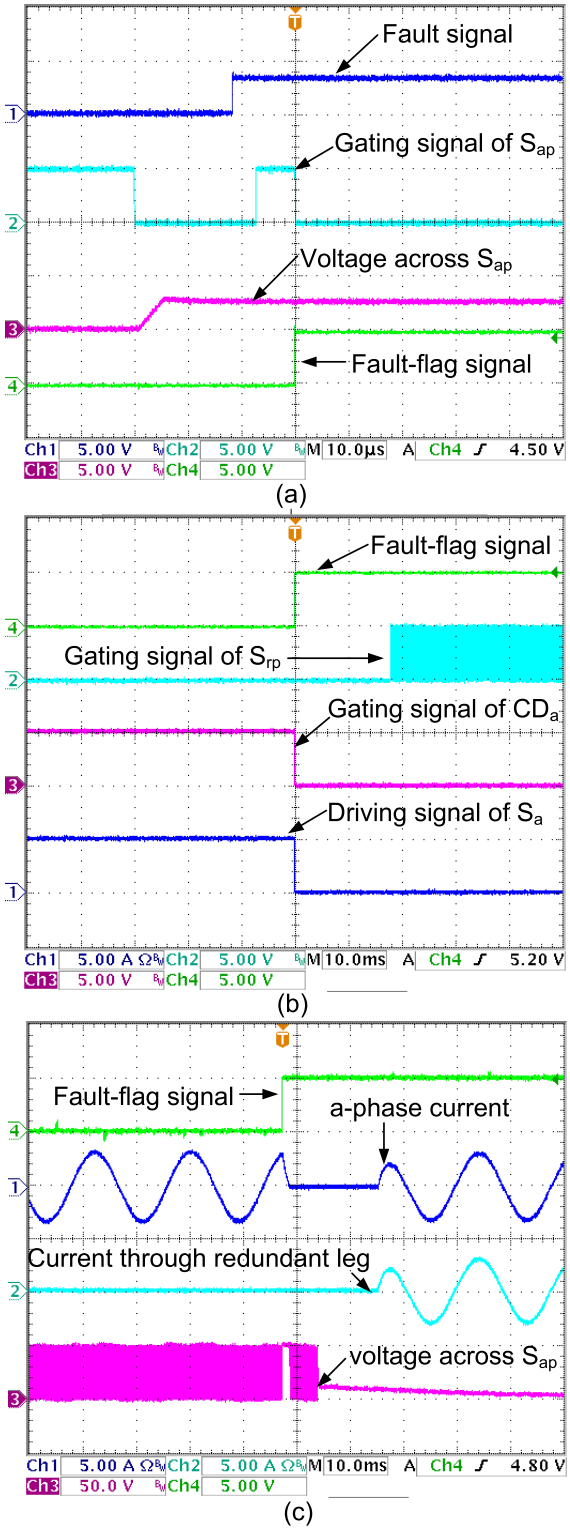
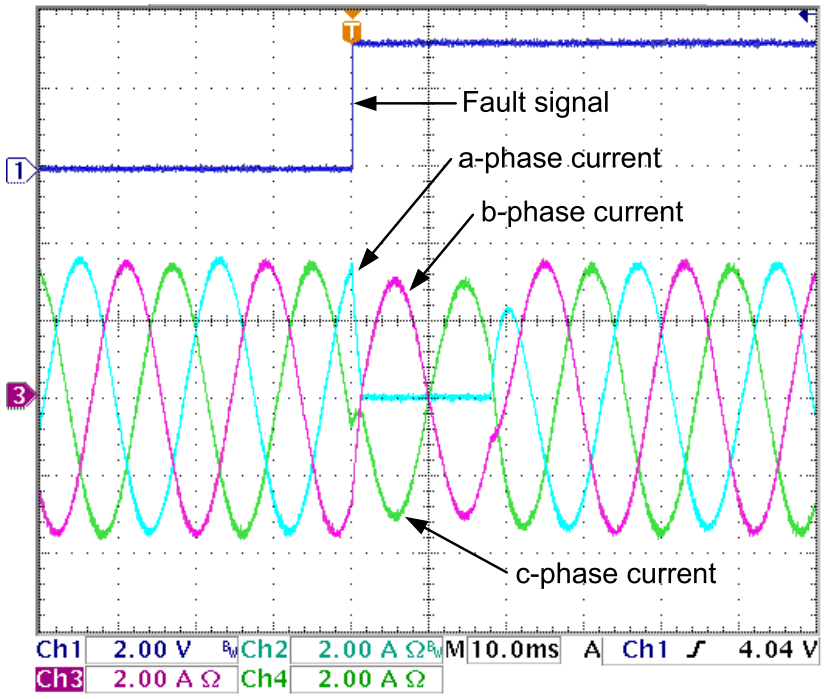
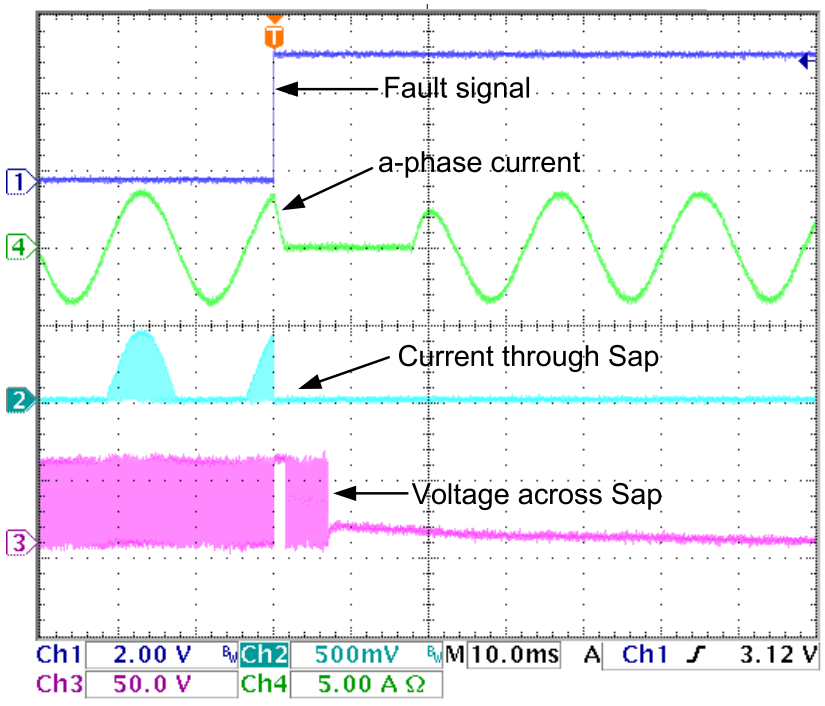


Figure 5.11 Fault detection and isolation based on the second fault-tolerant topology in case of open-switch fault of S_{ap}: (a) fault signal, gating signal of S_{ap}, sensed voltage across S_{ap}, and fault-flag signal; (b) fault-flag signal, gating signal of the upper switch S_{rp} in the redundant leg, gating signal of the TRIAC CD_a, and driving signal of the relay S_a; (c) fault-flag signal, a-phase current, current through the redundant leg, voltage across S_{ap}.



(a)



(b)

Figure 5.12 Experiment results based on the second fault-tolerant topology in case of open-switch fault of S_{ap}: (a) fault signal, a-phase current, b-phase current, and c-phase current; (b) fault signal, a-phase current, sensed current through S_{ap}, and voltage across S_{ap}.

full power operation distinguishes the limping-home capability of this proposed solution from the existing art. The excellent reliability of the new topology is verified by the quantitative assessment based on Markov reliability model. The doubled $MTTF$ of the proposed topology over the standard topology greatly reduces unscheduled maintenance, repair time and repair cost, which could offset the initial cost penalty for auxiliary devices. In addition, the time-domain simulation and experiment results evidently indicate that the normal operation of the drive system can be resumed after a short disturbance for both short-switch and open-switch faults.

Chapter 6

Reliability Evaluation of HVDC Converters

The reliability framework presented in Chapter 2 has been applied to evaluate the reliability of HEV systems. The focus of this chapter is to evaluate the reliability of different types of converters that are employed in HVDC systems.

6.1 Introduction

Voltage source converter (VSC)-based high voltage direct current (HVDC) technology has gained widespread applications in offshore power transmission, and long-distance underground and submarine cable crossings due to flexible power control capability, black-start capability, superior harmonic performance, and compact footprint [88, 89]. As a high-power high-voltage system, an HVDC system could adversely affect power quality and lead to significant economic losses to customers due to abnormal operation or unscheduled stoppage. Therefore, amongst the various system specifications, reliability bears substantial significance. The reliability analysis of HVDC power transmission systems has been reported in literature with emphasis on methods from the perspective of the power system [90–93]. An HVDC system is considered as a power supply, and the reliability research is focused on the indices that measure the capability that the HVDC system supply sufficient power to loads, such as the probability of failure (Q) that represents the probability that an HVDC system cannot supply sufficient power to loads, the expected energy not served

(EENS) that represents the energy that an HVDC system cannot supply to loads in a year, and so on.

In the reported studies, an HVDC converter is treated as a component with a fixed failure rate that is obtained from field experiences [94]. However, the failure rate of an HVDC converter strongly depends on the electrical and thermal stresses of components, which is particularly true for semiconductor devices. The oversimplified field-experience based reliability model does not accurately assess the reliability of the HVDC converters. The reliability of HVDC converters exerts a significant influence on the reliable operation of the overall HVDC system. An HVDC converter typically consists of several thousand semiconductor devices that are connected in parallel or in series [12]. The aggregation of such large number of power devices could result in high failure rates of the overall system. The field experiences show that the number of IGBT failures in Cross Sound Cable HVDC system during 2003-2009 ranges between 7 and 34 per year [12]. Therefore, the accurate prediction of the reliability of HVDC converters should be investigated to provide a guidance on the reliability improvement and maintenance management.

A few of investigations of the reliability of HVDC converters have been reported. The general concept and methodology for the prediction of the reliability of classic HVDC converter valves are introduced in [95]. The authors of [96] apply a k-out-of-n model to the reliability analysis of HVDC converter valves. The drawback to this reliability model is that the failure rates of semiconductor devices are independent of actual electrical stresses during operation.

In view of the significance of the reliability of HVDC converter and the lack of the detailed investigation, in this chapter the reliability of three commonly-used VSC HVDC converters (two-level, three-level, and modular multilevel converter (MMC)) is investigated by use of a mission profile-dependent model in terms of failure rate and mean time to failure (MTTF).

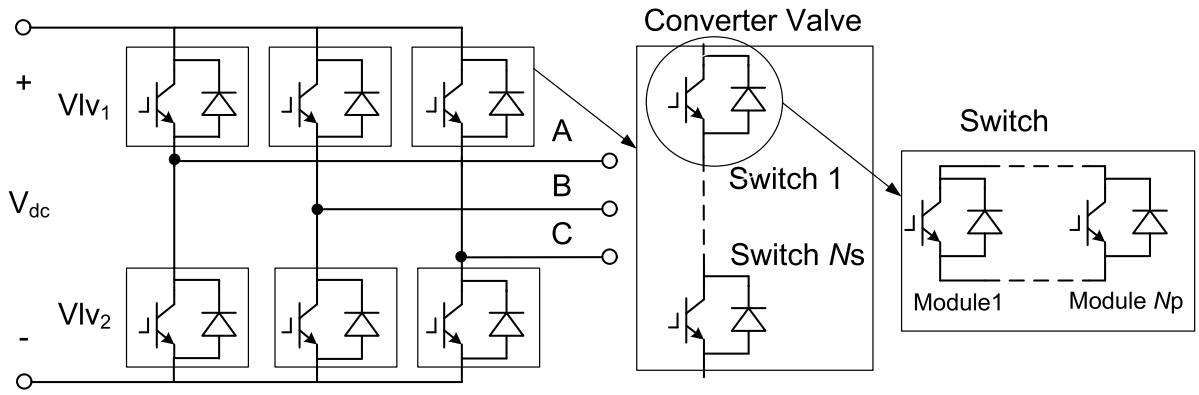


Figure 6.1 Schematics of a two-level converter, converter valve, and switch.

6.2 VSC-Based HVDC Converters

Since the first VSC HVDC transmission system was commissioned in 1997, three types of VSCs (two-level, three-level, and modular multilevel converters) have been utilized in HVDC systems [89]. The schematics of theses converters are shown in Fig. 6.1, 6.2, and 6.3, respectively. A two-level or modular multilevel converter consists of six switch positions, while a three-level converter consists of 18 switch positions.

For a two-level or three-level HVDC converter, a switch position is a converter valve that consists of N_S switches connected in series to deliver high voltage blocking capability. A switch consists of N_p insulated-gate bipolar transistor (IGBT) modules or diode modules connected in parallel to obtain high current capability. In a three-level converter, each phase leg consists of six converter valves with two clamping diodes, as shown in Fig. 6.2.

In a modular multilevel converter, each switch position that is also named as arm consists of n half-bridge cells with each cell consisting of two converter valves, as shown in Fig. 6.3. Likewise, the converter valve consists of IGBT modules that are connected in series and in parallel.

In the following sections, the reliability of these three types of HVDC converters are quantitatively evaluated in terms of failure rate and MTTF.

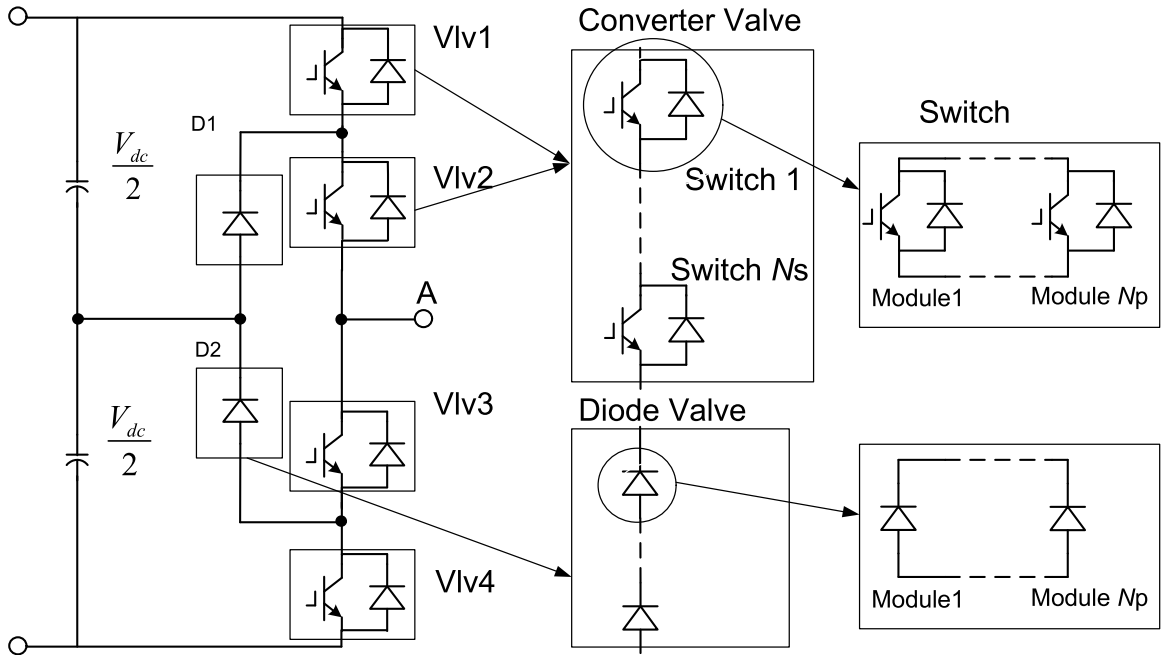


Figure 6.2 Schematics of a three-level converter, converter valve, diode valve, and switch.

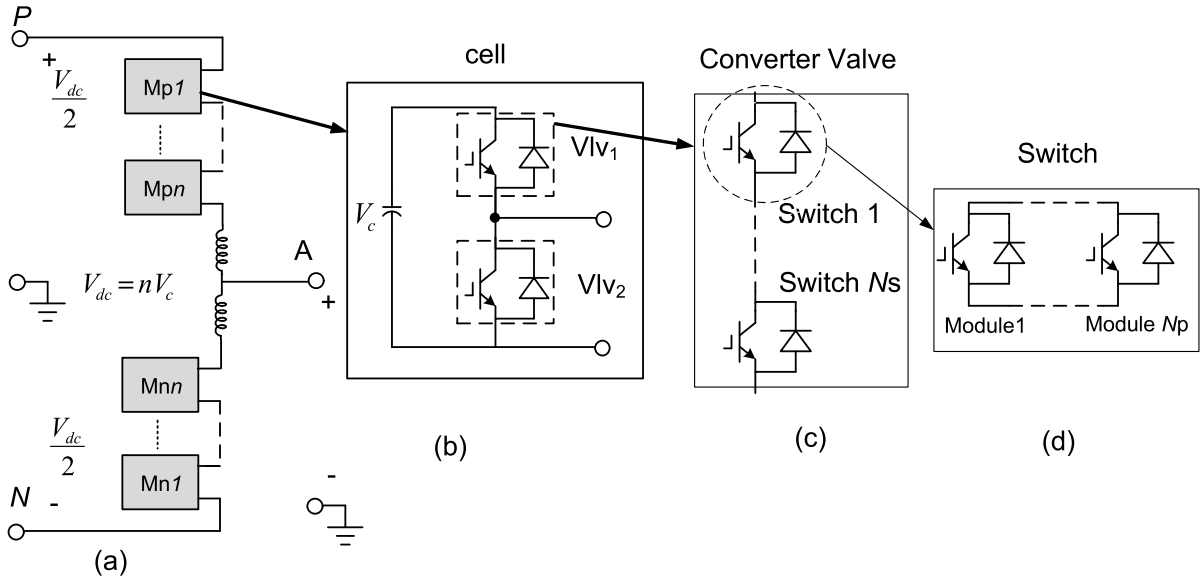
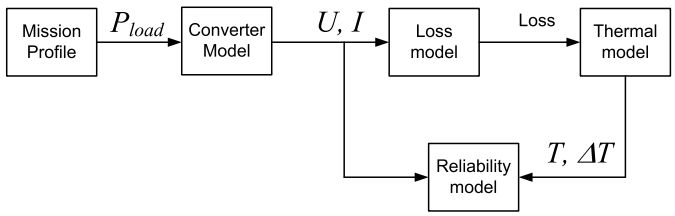


Figure 6.3 Schematics of a modular multilevel converter, cell, converter valve, and switch.



* P_{load}: load power;
U,I: converter voltage and current;
T, ΔT: junction temperature and temperature variation.

Figure 6.4 The diagram of the reliability simulation model for a VSC HVDC converter.

6.3 Reliability Model for HVDC Converters

Prior to the evaluation of the reliability of the HVDC converters, the reliability model is first introduced. This model is mainly focused on the reliability prediction of power semiconductor devices that include IGBTs and diodes, since these semiconductor devices are the key components of VSC HVDC converters. The structure of the reliability simulation model for VSC HVDC converters is shown in Fig. 6.4. In this model, the input data is the mission profile of the HVDC system that represents operating conditions of the converters. The failure rates and MTTFs of the components and converters can be obtained from the model. Each functional block will be introduced in the forthcoming paragraph.

The mission profile represents a sequence of load points versus time for an HVDC system. The mission profile provides instantaneous loading condition of the HVDC system to the converter model. By use of the load power from the mission profile, the electrical stresses of components in the HVDC converter are computed in the converter model. Based on the current and voltage stresses of the semiconductor devices that are provided by the converter model, the loss model is utilized to estimate the losses of the devices. The power loss calculation of the IGBT and diode is based on the averaged conduction and switching losses over each fundamental period of the output [97]. Based on the power losses that are obtained from the loss model, the thermal model is used to determine the junction temperature of the semiconductor devices and to detect the thermal cycling that the devices experience. Then, the electrical and thermal stresses are utilized by the

Table 6.1 Specification of the VSC HVDC System

Parameter	Value
Power rating	900 MW
Dc voltage	$\pm$320 kV
Configuration	Symmetric monopole

reliability model to calculate various reliability indices of power devices and converters. Herein, the failure rate models of IGBT and diode provided by the reliability handbook RDF2000 [19] is used to calculate the failure rates of semiconductor devices, and part-count method and Markov model are utilized to evaluate the reliability of the non-fault-tolerant and fault-tolerant designs of HVDC converters, respectively [35].

The reliability simulation model is utilized to evaluate the failure rates and MTTFs of three types of HVDC converters based on a simple HVDC system that is introduced in the following section.

6.4 System Specification and Component Selection

The reliability simulation model shown in Fig. 6.4 shows that the reliability of HVDC converters strongly depends on the electrical and thermal stresses of semiconductor devices. In order to determine these stresses, the converters should be firstly sized and the devices are then selected.

6.4.1 Specification of the HVDC System

In order to size the HVDC converters, the specification of the HVDC system and basic design rules should be first defined. Since the symmetric monopole configuration is used in the most of commercial VSC HVDC systems, it is applied to the simple VSC HVDC system. The basic specification of the VSC HVDC system in this study is shown in Table 6.1.

Some key operating parameters are needed to determine the electrical stresses of the three types

Table 6.2 Assumed Operating Parameters for the VSC HVDC Converters

Parameter	Value
Modulation index range for full-power operation	$0.8 \sim 1.0$
Minimal power factor for full-power operation	0.9
Switching frequency	Two-level converter 2340 Hz
	Three-level converter 1620 Hz
	Multilevel converter 60 Hz

of VSC HVDC converters. It is assumed that the sinusoidal PWM scheme with the maximum modulation index of 1.0 is used. In the case of fluctuations in the grid or generator voltage, the modulation index should be regulated so that the ac-side voltage of HVDC converters can follow the grid voltage. Therefore, it is assumed that the HVDC converter can transfer full power when the modulation index is in the range of 0.8 to 1.0. It is further assumed that the minimal power factor under full-power operating condition is 0.9. The modulation index and power factor in conjunction with power rating and dc voltage rating can determine the converters' maximum operating current.

Based on the operating experiences of commissioned or planned VSC HVDC systems, the switching frequencies for the two-level, three-level, and modular multilevel converter (MMC) are 2340 Hz, 1620 Hz and 60 Hz, respectively [98, 99]. The assumed operating parameters for the three types of VSC HVDC converters are listed in Table 6.2.

6.4.2 Electrical Stresses of the Converter Valves

The voltage and current stresses of the converter valves determine the selection of the components. Therefore, the electrical stresses of the converter valves for three types of converters are first determined.

For the two-level converter as shown in Fig. 6.1, each valve needs to block the total dc-link voltage when the complementary valve in the same phase leg conducts the load current. Therefore, the voltage stress of each valve is equal to the total dc voltage that is 640 kV. The current stress

can be determined by the following equation

$$I_{rms} = \frac{P_{dc}}{\sqrt{3} * pf * V_{ll}} \tag{6.1}$$

where P_{dc} is the power rating of the HVDC system, pf is power factor, V_{ll} is the RMS value of line-to-line voltage on the ac side, and is determined by

$$V_{ll} = 0.612 * M * V_{dc} \tag{6.2}$$

where M is the modulation index, and V_{dc} is the dc-link voltage. According to Table 6.2, pf is 0.9, and M for the worst case is 0.8. With these parameters (6.1) will determine the current stress of the converter valves. The voltage and current stresses of the two-level converter valves are tabulated in Table 6.3.

For the three-level converter, each phase leg consists of four switch valves $Vlv_1 \sim Vlv_4$ and two clamping-diode valves D_1 and D_2. These six valves are subject to the same voltage stress that is equal to half the dc-link voltage. The six valves have the same current stress as the valves of the two-level converter. The electrical stresses for the converter valves of the three-level converter are listed in Table 6.3.

In the case of the modular multilevel converter, the number of cells in each switch position should be first determined. If each cell is switched at the fundamental frequency, the number of cells determines the equivalent switching frequency of each phase leg. According to the implementation of MMC in [99], 38 cells per arm are selected. The nominal capacitor voltage V_c of the half-bridge cells as shown in Fig. 6.3 is accordingly determined [100]. The arms of the MMC have the same current stress as the valves of the two-level converter. The voltage and current stresses of the converter valves in the MMC are listed in Table 6.3.

Table 6.3 Electrical Stresses for the Converter Valves

Converter	Two-level	Three-level	Multilevel level
Voltage stress	640 kV	320 kV	16.85 kV
Current stress	1843 A(rms), 2605 A(peak)	1843 A(rms), 2605 A(peak)	1843 A(rms), 2605 A(peak)

6.4.3 Selection of Components

Based on the stresses of the converter valves, the components can be selected. In order for reliable operation, the applied voltage and current of devices should be less than their rated voltage and current. Herein, the voltage and current stresses of semiconductor devices are set to be the half of the corresponding current and voltage ratings. The ABB Stakpack IGBT module 5SNA 2000K451300 [101] is selected, whose voltage and current ratings are 4500 V and 2000 A, respectively. The parallel and series connection of IGBT modules are needed to obtain required voltage and current ratings. According to the electrical stresses listed in Table 6.3 and the design rule of 50% derating, the selection of semiconductor devices for the three types of HVDC converters is tabulated in Table 6.4.

6.5 Reliability Evaluation of HVDC Converters

In this section, the failure rates and MTTF of semiconductor devices of the three types of VSC HVDC converters are evaluated based on the reliability simulation model presented in Section 6.3.

Since the mission profile for the HVDC system is unavailable, the reliability of the devices under four typical loading conditions, 25%, 50%, 75% and 100% of the rated load, is analyzed. In the practical HVDC converter, the closed-loop liquid cooling system is utilized, and the heatsink temperature can be controlled by regulating the coolant temperature at the inlet. Therefore, the heatsink temperature is assumed constant at 60 °C. Since the thermal cycling at the fundamental frequency has an insignificant impact upon the failure of IGBTs and diodes, the average power loss

Table 6.4 Semiconductor Devices for the Three Types of HVDC Converters

Converter	Devices for non-redundant design
Two-level converter	6 converter valves, each valve includes 286 IGBT switches connected in series, each switch consists of two IGBT modules 5SNA 2000K451300 connected in parallel, and total 3432 IGBT modules 5SNA 2000K451300 are used.
Three-level converter	18 converter valves (only diodes in 6 valves are used), each valve consists of 143 IGBT switches connected in series, each switch consists of two IGBT modules connected in the parallel manner, and total 5148 IGBT modules 5SNA 2000K451300 are used.
Modular multilevel converter	6 arms, each arm consists of 38 half-bridge cells, each cell has two converter valves, each valve consists of 8 IGBT switches connected in series, each switch consists of two IGBT modules connected in parallel, and total 7296 IGBT modules 5SNA 2000K451300 are used.

model over one fundamental cycle is utilized. Based on the average loss model, the power losses of the IGBTs and diodes are constant in a fundamental cycle. The resultant temperatures of these semiconductor devices' junctions are also constant in a fundamental cycle.

6.5.1 Reliability Evaluation of the Devices in the Two-Level HVDC Converter

For the two-level converter, all IGBTs generate the same amount of power loss and consequently experience the same junction temperature. Likewise, all diodes experience the same junction temperature as well. The junction temperatures of the IGBTs and diodes can be obtained by use of the thermal model as shown in Fig. 6.4. The obtained junction temperatures of the IGBTs and the diodes under the four loading conditions are tabulated in Table 6.5. The profiles of junction temperatures versus the converter load are shown in Fig. 6.5. It can be observed that the temperature rise of IGBTs and diodes at rated load are 37.6 $^{\circ}$C and 20 $^{\circ}$C, respectively. Since the power loss

Table 6.5 Junction Temperatures of the IGBT and Diode in the Two-level Converter

Load	25%	50%	75%	100%
IGBT (°C)	69.1	78.3	87.9	97.6
Diode (°C)	64.9	69.9	74.9	80

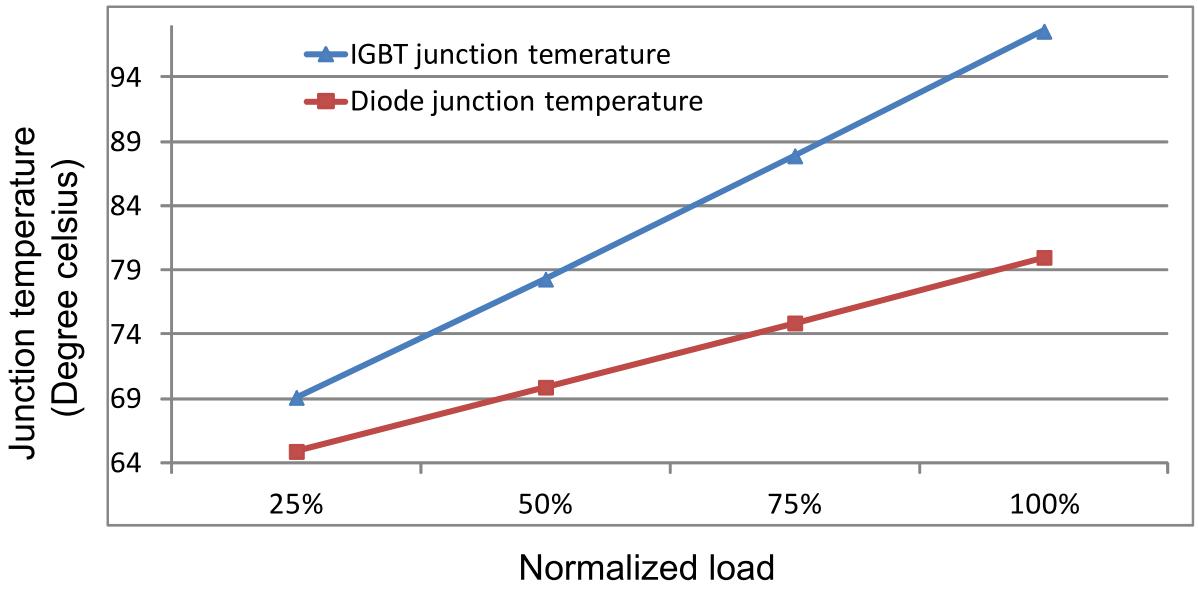


Figure 6.5 Junction temperatures of the IGBT and diode in the two-level converter.

of the IGBTs is higher than that of the diodes, the IGBTs experience higher thermal stress.

Based on the obtained voltage stress and thermal stress, the failure rates of the semiconductor devices can be evaluated by use of the reliability model from RDF2000. The failure rates of the IGBTs and diodes are listed in Table 6.6. It can be observed that the failure rates of the IGBT and diode in a module at rated load are 2.022 and 3.756 per 10^9 hours, respectively. The profiles of the failure rates versus the converter load are shown in Fig. 6.6. As the load power decreases, the junction temperatures of devices decrease and consequently the failure rates also decrease. Although the IGBTs experience higher junction temperature than the diodes, the failure rate of the IGBTs is lower than that of the diodes since the failure of the diodes are more sensitive to the junction temperature than the IGBTs.

Table 6.6 Failure Rates of the IGBT an Diode in the Two-level Converter

Load	25%	50%	75%	100%
IGBT (/10^9 hours)	0.924	1.209	1.569	2.022
Diode (/10^9 hours)	2.087	2.546	3.097	3.756

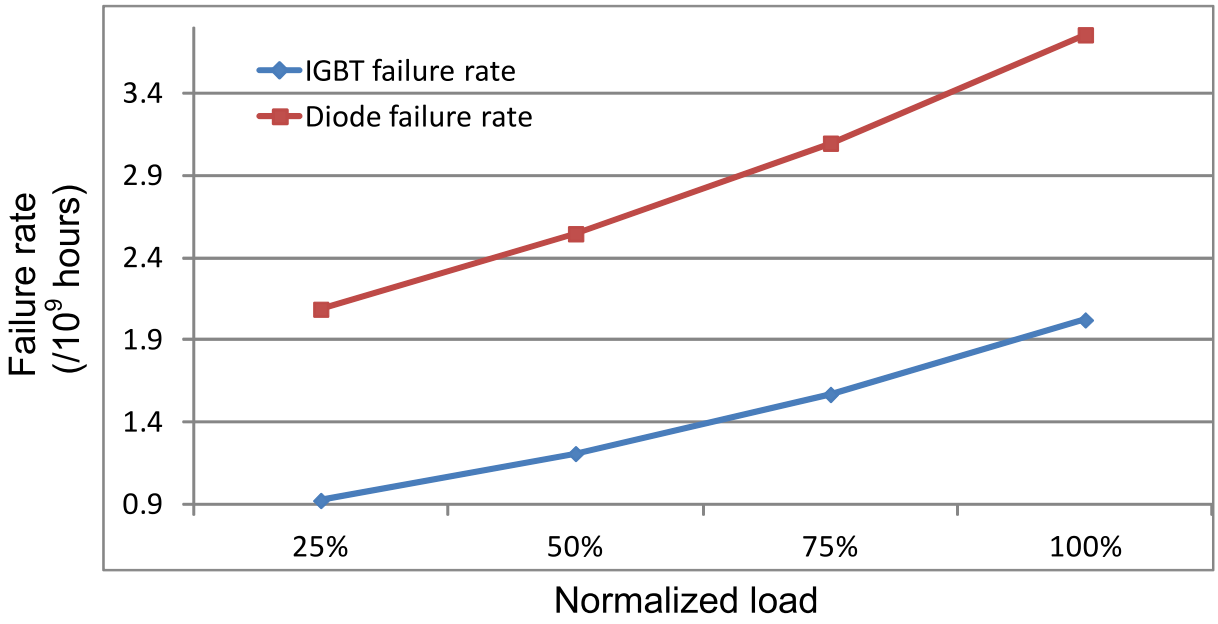


Figure 6.6 Failure rates for the IGBT and diode of the two-level converter.

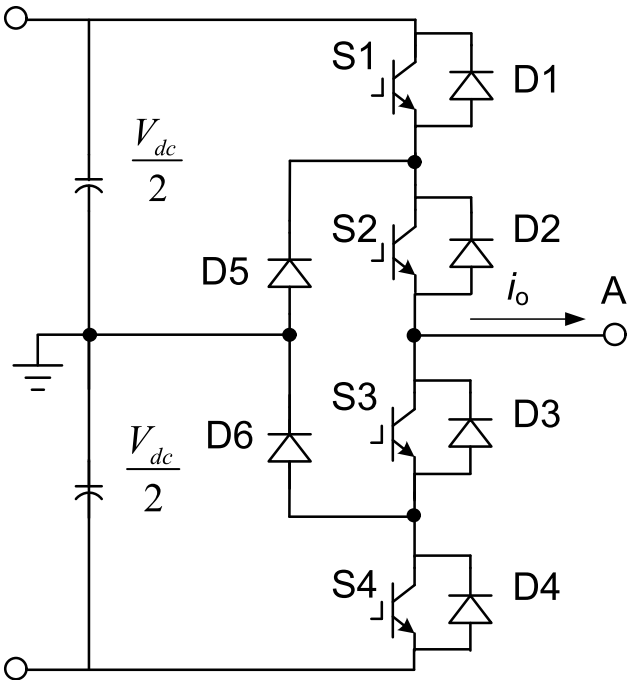


Figure 6.7 A phase leg of a three-level NPC converter.

6.5.2 Reliability Evaluation of the Devices in the Three-Level HVDC Converter

The same reliability simulation model as the one presented in Section 6.3 can be applied to the reliability assessment of the three-level HVDC converter.

The loss model for the three-level HVDC converter is deduced based on the carrier-based three-level PWM, and detailed loss model is not presented in the thesis. In comparison with the two-level converter, the IGBTs and diodes in different switch positions of the three-level converter have different power loss models. The IGBTs or diodes in one converter valve have the same loss model. Fig. 6.7 shows a phase leg of the three-level converter. In this phase leg, the IGBTs S1 and S4 generate the same average power loss while S2 and S3 generate the same power loss. For the diodes, D1 and D4 generate the same loss, D2 and D3 generate the same loss, and D5 and D6 generate the same loss. The devices in the same position of the three legs generate the same loss. Therefore, the losses of the five devices, S1, S2, D1, D2, and D5, are analyzed. Correspondingly, the junction temperatures of these five devices are analyzed.

Table 6.7 Junction Temperatures of the IGBTs and Diodes in the Three-level Converter

Load	25%	50%	75%	100%
IGBT S1 (°C)	66.4	72.9	79.7	86.7
IGBT S2 (°C)	60.7	61.6	62.8	64.2
Diode D1 (°C)	61.2	62.5	63.8	65.2
Diode D2 (°C)	60.1	60.3	60.5	60.8
Diode D5 (°C)	63.4	67.6	71.5	75.5

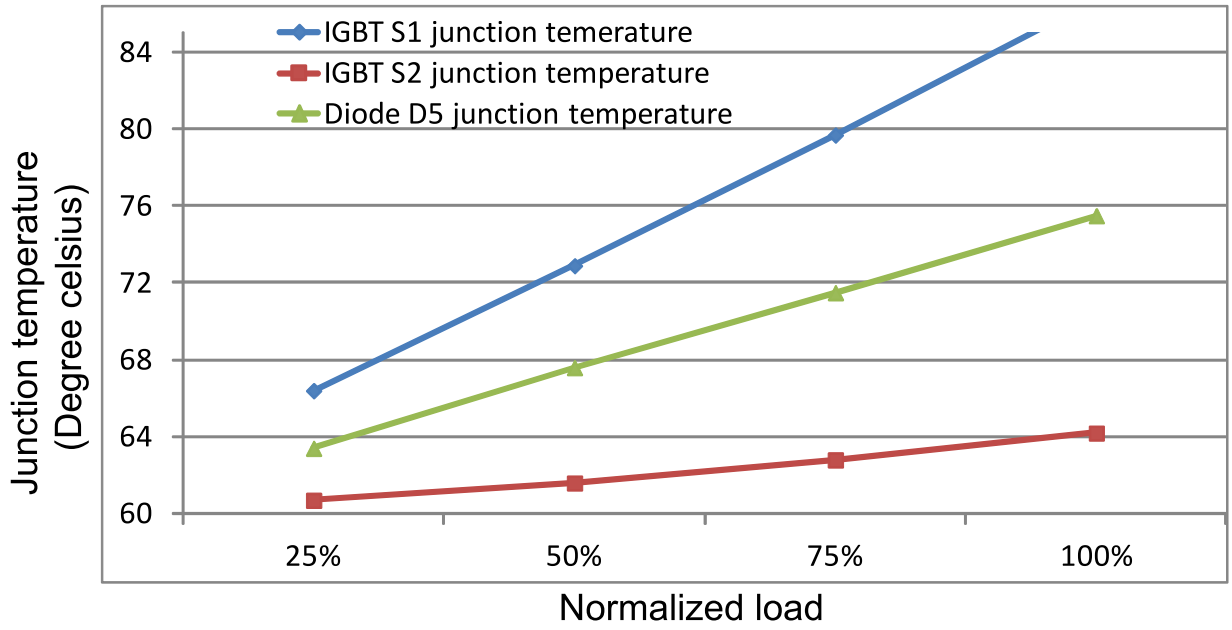


Figure 6.8 The Junction temperatures of the IGBTs and diodes in the three-level converter.

The obtained junction temperatures of the devices are listed in Table 6.7. Since the diodes $D1$ and $D2$ do not conduct the load current in the case of the unity power factor, they do not have power losses. Therefore, their junction temperatures are equal to the corresponding IGBT modules' case temperatures that are slightly higher than the heatsink temperature. The junction temperature variations of the IGBTs $S1$ and $S2$, and the diode $D5$ versus the changes in the normalized load are illustrated in Fig. 6.8.

By use of the voltage stresses and junction temperatures, the reliability model can be applied to the evaluation of the failure rates of the semiconductor devices. The calculated failure rates of the devices are listed in Table 6.8. The variations in the failure rates of the IGBTs and diodes are

Table 6.8 Failure Rates of the IGBTs and Diodes in the Three-Level Converter

Load	25%	50%	75%	100%
IGBT S1 (/10^9 hours)	0.852	1.036	1.257	1.522
IGBT S2 (/10^9 hours)	0.725	0.737	0.764	0.799
Diode D1 (/10^9 hours)	1.795	1.893	1.999	2.112
Diode D2 (/10^9 hours)	1.714	1.727	1.744	1.765
Diode D5 (/10^9 hours)	1.993	2.328	2.718	3.172

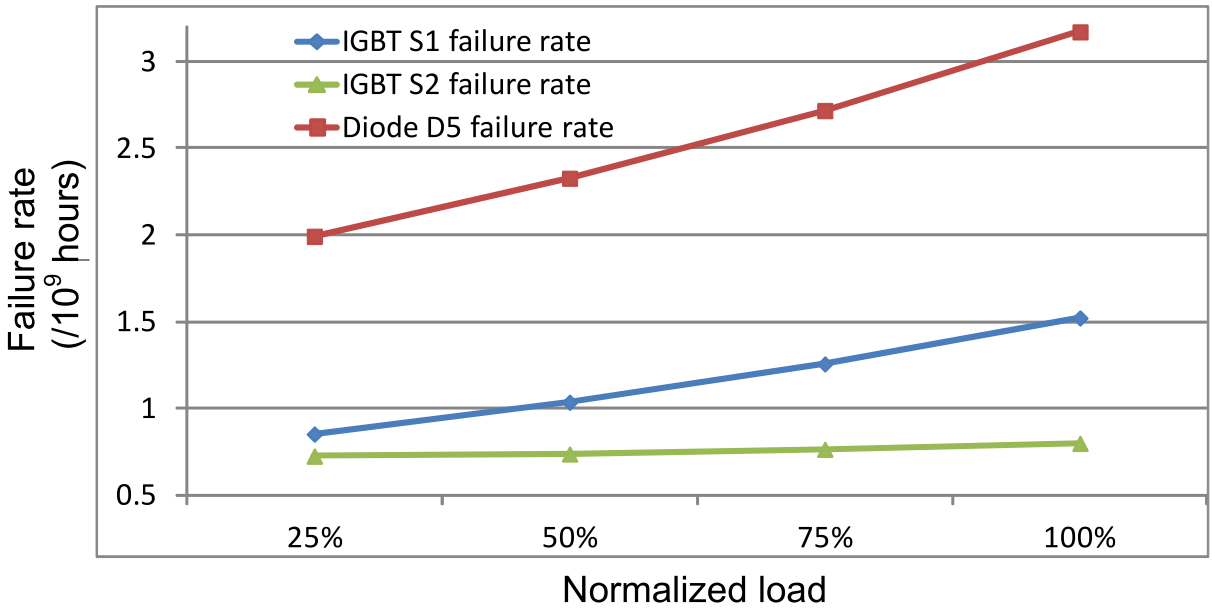


Figure 6.9 Failure rates of the devices in the three-level converter.

illustrated in Fig. 6.9. It can be observed that the failure rates of the diodes are higher than those of the IGBTs since the failure rate of the diode more strongly depends on the junction temperature.

6.5.3 Reliability Evaluation of the Devices in the Modular Multilevel HVDC Converter

The losses of the semiconductor devices in the MMC depend on the modulation scheme. Since each arm of the modular multilevel HVDC converter consists of 38 half-bridge cells, the nearest-level modulation scheme is utilized so that the cells operate at the fundamental frequency with

Table 6.9 Junction Temperatures of the IGBTs and Diodes in the Modular Multilevel Converter

Load	25%	50%	75%	100%
IGBT with the highest junction temperature ($^{\circ}$C)	60.72	61.7	62.7	63.98
IGBT with the lowest junction temperature ($^{\circ}$C)	60	60	60	60
Diode with the highest junction temperature ($^{\circ}$C)	61.1	62.5	64.1	65.8
Diode with the lowest junction temperature ($^{\circ}$C)	60	60	60	60

minimized switching losses [102]. The detailed loss analysis is not included in the thesis.

The power losses obtained from the loss model can be used for thermal analysis to obtain the junction temperatures of the devices. Since the half-bridge cells of the MMC is switched at the fundamental frequency, the switching losses of the devices in the MMC are significantly lower than the conduction losses. Therefore, the conduction losses of the devices in the MMC are dominant. In each arm of the MMC, the half-bridge cells conduct for different intervals. The uneven utilization of the half-bridge cells results in uneven distributions of the conduction losses of the semiconductor devices. The uneven loss distributions further lead to the fact that the devices in different cells experience different junction temperatures. Herein, only the junction temperatures of the IGBTs and diodes with the highest and lowest junction temperatures are listed in Table 6.9. It can be observed that the highest junction temperatures for the IGBTs and diodes are 63.98 and 65.8 $^{\circ}$C, respectively, and the lowest junction temperatures for IGBTs and diodes are 60 $^{\circ}$C, respectively. Therefore, the maximum junction temperature difference between IGBTs is only 4 $^{\circ}$C, and the maximum junction temperature difference between diodes is approximate 6 $^{\circ}$C.

The junction temperatures of the devices in the MMC also depend on the load power. Fig. 6.10 illustrates variations in devices' junction temperatures as load power varies from 25% to 100% of the rated load.

The junction temperatures can be further used for the reliability analysis of the semiconductor

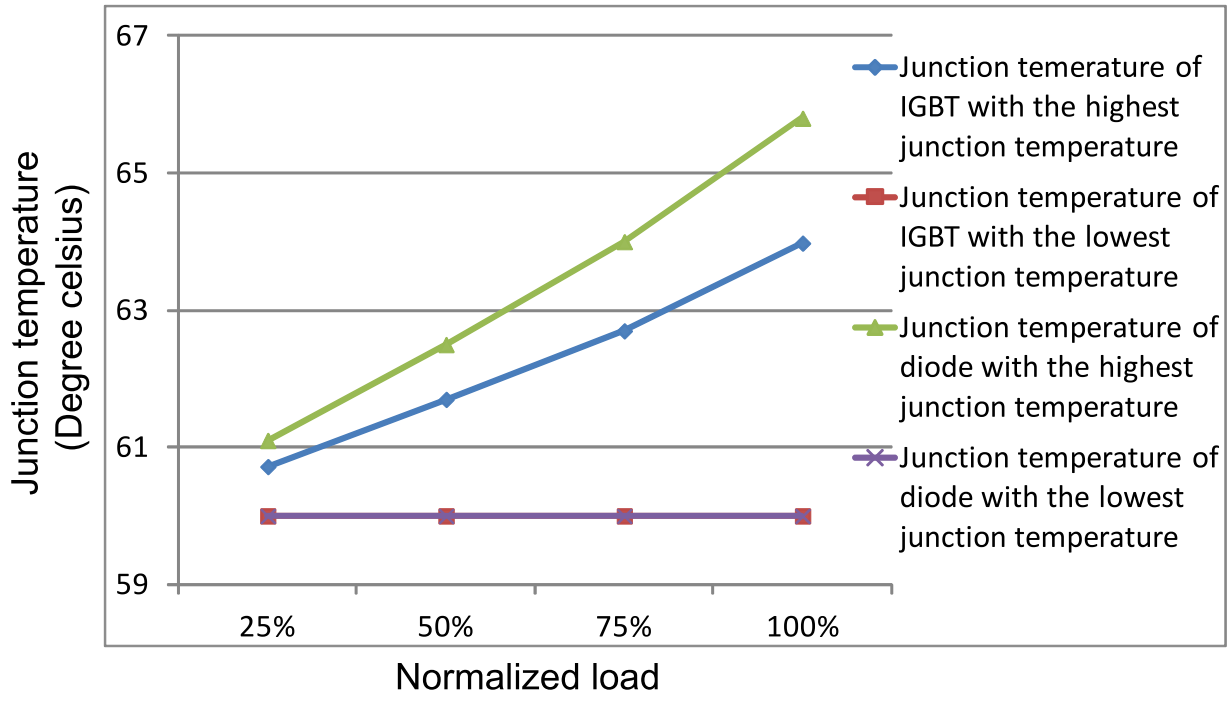


Figure 6.10 The junction temperatures of the IGBTs and diodes with the highest or the lowest junction temperature in the modular multilevel converter.

devices. The calculated failure rates of the devices with the highest or the lowest failure rate are listed in Table 6.10. The variations in the failure rates of the devices with the changes in the normalized load power are shown in Fig. 6.11.

6.5.4 Comparative Study of the Reliability of Three Types of HVDC Converters

As a non-redundant system, an HVDC converter's failure rate can be obtained by summing the failure rates of the IGBTs and diodes of the converters. Herein, the failure rates of the converters only include the failures of the semiconductor devices. The failures of the other components, such as the magnetic device and capacitors, are excluded from this study since they would only account for a very small percentage of the failures.

The annual failure rates for the three converters are listed in Table 6.11, and the failure rate variations versus the load power are shown in Fig. 6.12. The annual failure rates for the two-

Table 6.10 Failure Rates for the Devices and Modular Multilevel Converter

Load	25%	50%	75%	100%
IGBT with the highest failure rate (/10^9 hours)	0.716	0.736	0.763	0.792
IGBT with the lowest failure rate (/10^9 hours)	0.7	0.7	0.7	0.7
Diode with the highest failure rate (/10^9 hours)	1.788	1.891	2.015	2.165
Diode with the lowest failure rate (/10^9 hours)	1.705	1.705	1.705	1.705

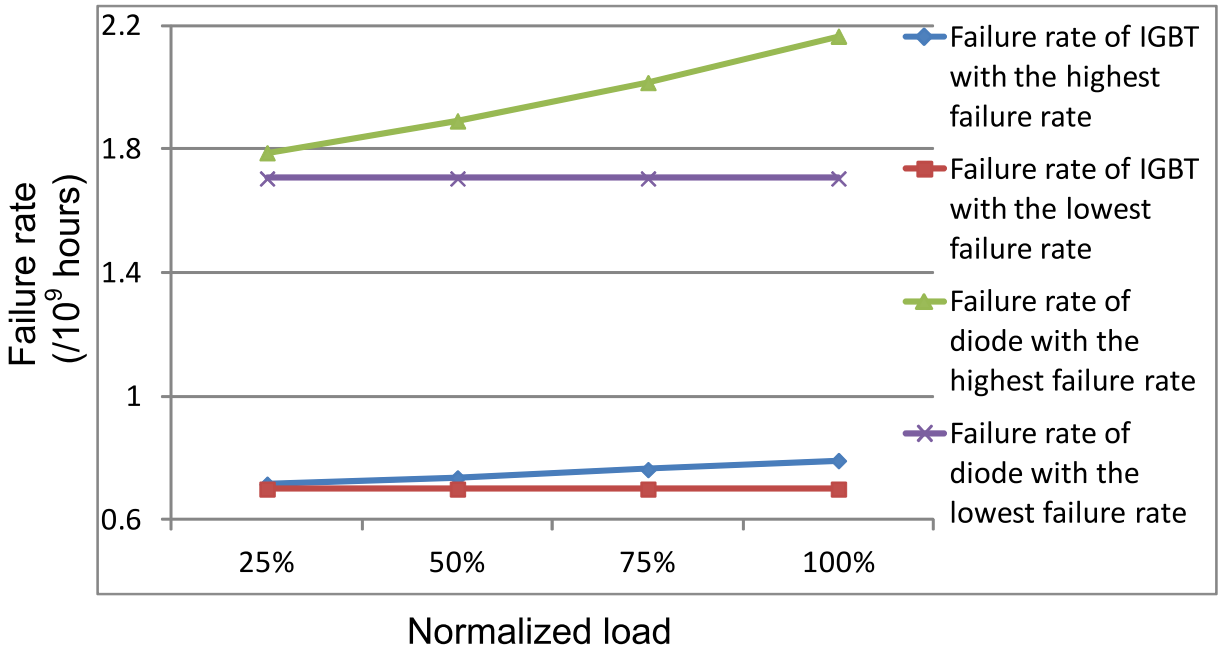


Figure 6.11 The failure rates of IGBTs and diodes with the highest or the lowest failure rates.

Table 6.11 Annual Failure Rates of the Three Types of VSC HVDC Converters

Load	25%	50%	75%	100%
Two-level converter (failures per year)	0.091	0.113	0.140	0.174
Three-level converter (failures per year)	0.106	0.116	0.128	0.141
Modular multilevel converter (failures per year)	0.155	0.157	0.159	0.162

level, three-level, and modular multilevel converter at the rated load are 0.174, 0.141 and 0.162 failures per year, respectively. It can be observed that under light-load operating condition, the modular multilevel converter has the highest annual failure rate, while the two-level converter has the lowest failure rate. On the contrary, under the full-load operating condition, the two-level converter experiences the highest failure rate, while the three-level converter has the lowest failure rate. The reason is that under the light-load condition, the contribution of the number of devices to the failures of the converters is dominant, while under the full-load operating condition, the thermal stress dominates the failures of the converters. Therefore, although the IGBTs and diodes in the MMC generate the lower losses, experience the lower thermal stresses and consequently the lower failure rates, the modular multilevel converter experiences the highest failure rate in the light-load condition since much more devices than the two-level and three-level converters are needed. Since the three-level converter needs few devices than the MMC and experienced less thermal stress than the two-level converter, in the full-load condition, the three-level converter is the most reliable topology.

The failure rates of the three converters are influenced by the load power. Under the condition of the full load, the converters are subject to the highest failure rates and are the least reliable since the converters experience the worst electrical and thermal stresses. The failure rates of the converters decrease as the load power decreases. Since the MMC has much lower switching loss, each device generates much lower loss and consequently experiences lower thermal stresses. Consequently, the contribution of thermal stresses to the failure rates of the MMC is less significant. Therefore, the minimal variations in the failure rate of the MMC can be observed when the con-

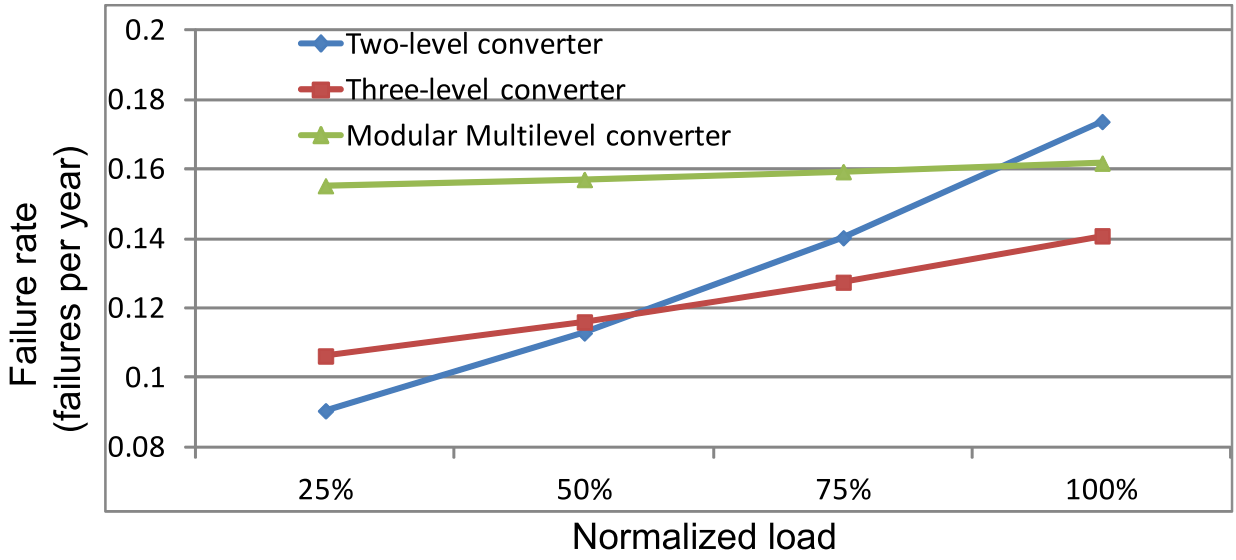


Figure 6.12 Annual failure rates of the three types of VSC HVDC converters.

Table 6.12 MTTFs of the Three Types of VSC HVDC Converters

Load	25%	50%	75%	100%
Two-level converter (years)	11.05	8.86	7.13	5.76
Three-level converter (years)	9.41	8.62	7.84	7.10
Modular multilevel converter (years)	6.44	6.37	6.28	6.18

verter's load power decreases to 25% of the rated load.

Another reliability metric, mean time to failure (MTTF) is also evaluated for the three types of converters. MTTFs of the three converters are listed in Table 6.12. MTTFs of the two-level, three-level, and modular multilevel converter under the full-load operating condition are 5.76, 7.10 and 6.18 years, respectively. The three-level converter has the longest MTTF and consequently is the most reliable under the full-load condition.

MTTF also depends on the load power. When the load power decreases, MTTFs of converters will increase, as shown in Fig. 6.13. In the case that the load power is reduced to 25% of the rated load, the MTTF of the two-level converter increases to 11.05 years from 5.76 years. It can be observed that the load variations have less impact on MTTF of the MMC.

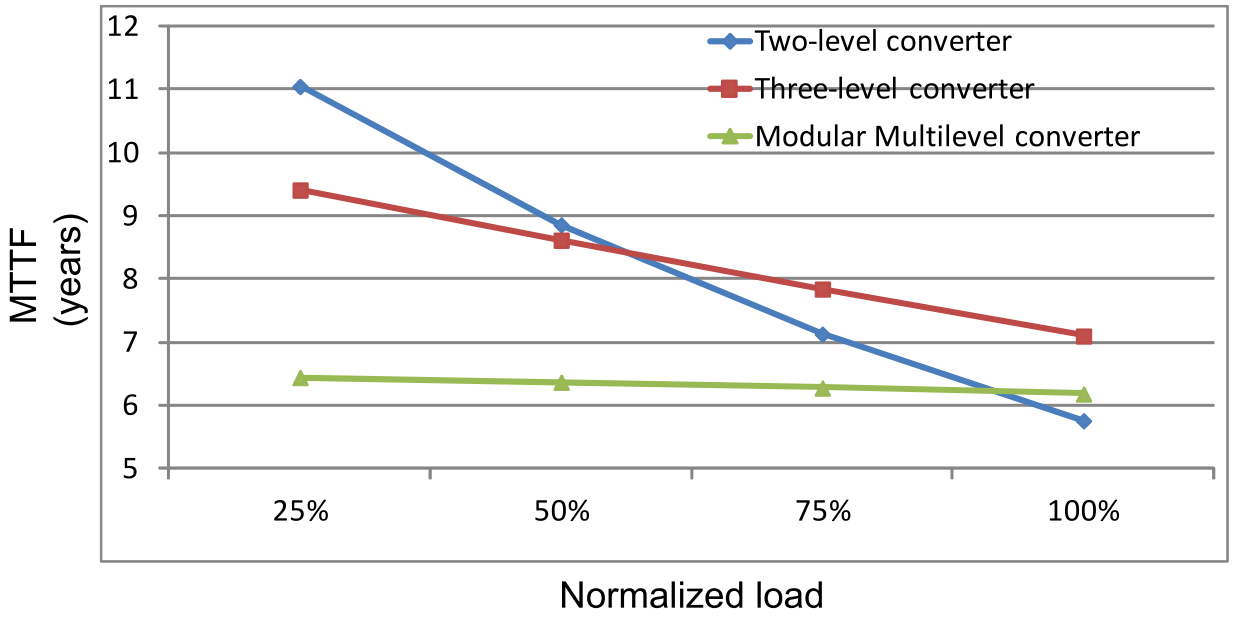


Figure 6.13 MTTFs of the three types of VSC HVDC converters.

6.6 Summary

In this chapter, the failure rates and MTTFs of the three types of commonly-used HVDC converter topologies, two-level, three-level, and modular multilevel converters, have been evaluated based on the load-dependent reliability model. The reliability evaluation results show that the reliability of the converters and semiconductor devices strongly depends on the thermal stresses that are related to the load conditions. When the load power decreases, the failure rates of the HVDC converters increase. At the rated load, the MTTFs of the two-level, three-level, and modular multilevel converters are 5.76, 7.10, and 6.18 years, respectively, while as the load power decreases to 25% of the rated load, the respective MTTFs of the three converters increase to 11.05, 9.41, and 6.44 years. It can be observed that the reliability of the two-level converter is most impacted by the load variations while the reliability of the modular multilevel converter is least impacted by the load variations.

In comparison to the two-level converter, the three-level converter consists of fewer devices and more reliable at heavy load. The modular multilevel converter needs much more components and is the least reliable topoloy. Therefore, the three-level converter has better reliability performance

with the reasonable part count.

Chapter 7

Fault-Tolerant Design and Reliability Analyaisi of HVDC Converters

7.1 Introduction

The failure rates and MTTFs of the three types of commonly-used VSC HVDC converters have been assessed in Chapter 6. Although the three-level converter has the best reliability performance and the failure rate can be minimized, the fault of the converter is possible in the life time. Since there is no redundancy, any failure of an HVDC converter will cause an unscheduled shutdown of the HVDC system. An unplanned stoppage of the HVDC system may lead to serious economic losses. Therefore, the fault-tolerant capability is worth investigation. The fault-tolerant design and corresponding reliability evaluation of the three types of VSC HVDC converters are presented in this chapter.

7.2 Fundamentals of Redundant Design of the VSC HVDC Converters

Fault-tolerant operation means that a fault in a component or subsystem does not cause the overall system to malfunction [27]. The fault-tolerant capability avoids the system from significant losses or unexpected interruptions and consequently improves the availability. Fault-tolerant operation can be realized by use of redundant design of systems. Redundancy can be implemented at the component level or at the system level. Since the HVDC converters involve a large number of devices, the converter-level redundant design can lead to significantly higher cost. On the other hand, the redundant components can potentially increase the cost and footprint with relatively low percentage. Therefore, the component-level redundant design is a suitable option for the VSC HVDC converters.

The failure mechanism of the press-pack IGBT module enables the component-level redundant design of VSC HVDC converters. The press-pack semiconductor devices certainly fail in short-circuit mode, and the faulted devices can conduct rated load current with acceptable voltage drop. A converter valve of the VSC HVDC converters consists of many IGBT switches that are connected in series to deliver the high blocking voltage. When a switch fails in the short-circuit mode, if the remaining healthy devices can deliver the full dc-link voltage, the converter still can transfer the full-capacity power. Consequently, the fault-tolerant operation of the HVDC converters can be maintained. The design rule is explained as follows.

The $N + m$ design rule is utilized. Herein, N denotes the number of semiconductor switches that are connected in series are necessary under normal operating condition while m denotes the number of extra switches that are added to each converter valve to realize redundancy. The HVDC converter can continue to work without stoppage until $m + 1$ devices have failed in a converter valve. Herein, m is chosen to be 1. Therefore, if one of $N + 1$ switches fails, the converter still continues to operate.

Table 7.1 Semiconductor Devices for Fault-Tolerant Design of the Three Types of HVDC Converters

Converter	Devices for redundant design
Two-level converter	6 converter valves, each valve includes 287 IGBT switches connected in series, each switch consists of two IGBT modules connected in parallel, and total 3444 IGBT modules 5SNA 2000K451300 are used.
Three-level converter	18 converter valves (only diodes in 6 valves are used), each valve includes 144 IGBT switches connected in series, each switch consists of two IGBT modules, and total 5454 IGBT modules 5SNA 2000K451300 are used.
Modular multilevel converter	6 arms, each arm consists of $38 + 1$ half-bridge cells, each cell has two converter valves, each valve consists of 8 switches connected in series, each switch consists of two IGBT modules connected in parallel, and total 7488 IGBT modules are used.

7.3 Redundant Design and Reliability Evaluation of the Two-Level HVDC Converter

As listed in Table 6.4, for normal operation, each converter valve consists of 286 switches that are connected in series. For the fault-tolerant design based on the design rule of $N + 1$, each converter valve should consist of $286 + 1$ switches. Each switch still consists of two IGBT modules in parallel. The total numbers of IGBT modules for the fault-tolerant two-level converter are shown in Table 7.1. It can be observed that 12 extra IGBT modules are needed to realize the fault-tolerant design of the two-level converter.

Markov chain is an effective approach to evaluating the reliability of fault-tolerant systems. This approach can cover many features of redundant systems, such as sequence of failures, failure coverage and state-dependent failure rates. Therefore, Markov model is adopted to assess the reliability of the fault-tolerant HVDC converters. The fundamentals of Markov model has been

explained in [103].

In order to reduce the order of the state equation, all devices with the same operating states and transition processes are treated as one subsystem. In the two-level converter, there are six converter valves. According to the design rule of the fault tolerance, the converter will fail and stop working if and only if any two series connected IGBT switches in the same converter valve fail. However, if two failed components reside in different converter valves, the system still works as a functional state and can deliver full power.

Based on the aforementioned analysis, for the fault-tolerant two-level converter, there are 13 states that include seven functional states and six failed states, as shown in Fig. 7.1, where $\alpha_{j,k}$ ($j = 0, 1, 2, 4, 6, 8, 10, k = 1, 2, ..., 12$) represents the transition rate of the converter from the state j to the state k. The 13 states and calculation of the corresponding transition rates are explained as follows:

1. State 0: It is a fault-free state, in which all components are healthy.

2. State 1: Only one IGBT switch fails in short-circuit mode, and the converter can perform normal functions. The transition of the converter from State 0 to State 1 can be caused by the failure of any one IGBT switch in the six converter valves. Consequently, the transition rate $\alpha_{0,1}$ can be obtained by summing the failure rates of all IGBT switches, and can be mathematically expressed as

$$\alpha_{0,1} = (\lambda_{IGBT,f} + \lambda_{diode,f}) * (N_s + 1) * N_p * 6 \tag{7.1}$$

   where $\lambda_{IGBT,f}$ and $\lambda_{diode,f}$ are failure rates of the IGBT and diode of the fault-tolerant two-level HVDC converter, respectively, and N_s is the number of the switches connected in series in a converter valve without fault-tolerant capability, and N_p is the number of the IGBT modules connected in parallel in a switch.

3. States 2 and 3: In both states, two IGBT switches fail in short-circuit mode. The difference lies in the fact that in State 2, the two faulted IGBT switches are in two different converter

valves, and consequently the converter will continue to properly function, while in State 3, the two faulted IGBT switches are in the same valve and consequently the converter is in a failed state and has to stop working. The transition rates $\alpha_{1,2}$ and $\alpha_{1,3}$ are determined by

$$\alpha_{1,2} = (\lambda_{IGBT,f} + \lambda_{diode,f}) * (N_s + 1) * N_p * 5 \tag{7.2}$$

and

$$\alpha_{1,3} = (\lambda_{IGBT,nf} + \lambda_{diode,nf}) * N_s * N_p \tag{7.3}$$

respectively, where $\lambda_{IGBT,nf}$ and $\lambda_{diode,nf}$ are failure rates of the IGBT and the diode for the non-fault-tolerant two-level HVDC converter, respectively.

4. States 4 and 5: In these two states, three IGBT switches are faulted. State 4 corresponds to a functional state in which the three faulted IGBT switches are located in three different valves, and the converter can continue to work. The transition rate $\alpha_{2,4}$ is

$$\alpha_{2,4} = (\lambda_{IGBT,f} + \lambda_{diode,f}) * (N_s + 1) * N_p * 4 \tag{7.4}$$

On the contrary, in State 5, two of the three faulted IGBT switches are in the same converter valve. Therefore, State 5 is a failed state. The corresponding transition rate from State 2 to State 5 $\alpha_{2,5}$ is

$$\alpha_{2,5} = (\lambda_{IGBT,nf} + \lambda_{diode,nf}) * N_s * N_p * 2 \tag{7.5}$$

5. States 6 and 7: Four IGBT switches fail in these two states. State 6 is a functional state, in which the four failed IGBT switches are in four different converter valves. In State 7, two of the four faulted IGBT switches are in the same converter valve and consequently the converter fails. The corresponding transition rates $\alpha_{4,6}$ and $\alpha_{4,7}$ are

$$\alpha_{4,6} = (\lambda_{IGBT,f} + \lambda_{diode,f}) * (N_s + 1) * N_p * 3 \tag{7.6}$$

and

$$\alpha_{4,7} = (\lambda_{IGBT,nf} + \lambda_{diode,nf}) * N_s * N_p * 3 \tag{7.7}$$

respectively.

6. States 8 and 9: These two states correspond to the condition of five faulted IGBT switches. In State 8, the five faulted IGBT switches are in five different converter valves. By contrast, in State 9, two of the five faulted IGBT switches are located in the same converter valve and consequently the converter fails and has to stop to work. The failure rates $\alpha_{6,8}$ and $\alpha_{6,9}$ are

$$\alpha_{6,8} = (\lambda_{IGBT,f} + \lambda_{diode,f}) * (N_s + 1) * N_p * 2 \tag{7.8}$$

and

$$\alpha_{6,9} = (\lambda_{IGBT,nf} + \lambda_{diode,nf}) * N_s * N_p * 4 \tag{7.9}$$

respectively.

7. States 10 and 11: In these two states, six IGBT switches fail. State 10 is a functional state and the converter can deliver full power since the six faulted IGBT switches are located in six different converter valves. In State 11, two of the six faulted switches are in the same converter valve. Therefore, State 11 is a failed state. The corresponding transition rates $\alpha_{8,10}$ and $\alpha_{8,11}$ are

$$\alpha_{8,10} = (\lambda_{IGBT,f} + \lambda_{diode,f}) * (N_s + 1) * N_p \tag{7.10}$$

and

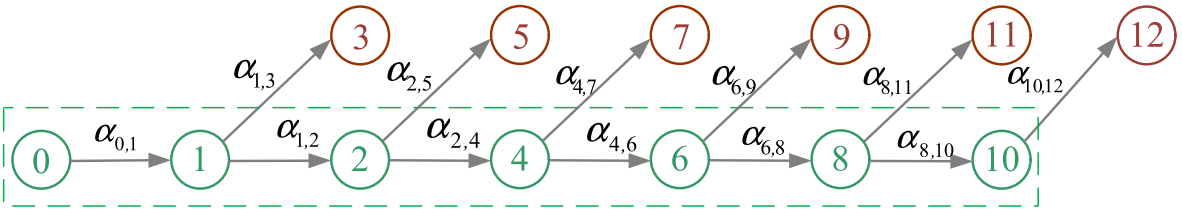
$$\alpha_{8,11} = (\lambda_{IGBT,nf} + \lambda_{diode,nf}) * N_s * N_p * 5 \tag{7.11}$$

respectively.

8. State 12: In State 12, there are seven faulted IGBT switches. Since there are six converter

Table 7.2 Component Failure Rates for the Fault-Tolerant and Non-Fault-Tolerant Two-Level VSC HVDC Converters

Design	Component	Failure rate ($/10^9$ hours)
Non fault-tolerant design	IGBT	2.022
	Diode	3.756
Fault-tolerant design	IGBT	2.016
	Diode	3.747



Functional states: 0, 1, 2, 4, 6, 8, 10, Failed states: 3, 5, 7, 9, 11, 12

State 0: fault free

State 1: one component fails

State 2 and 3: two components fail

State 4 and 5: three components fail

State 6 and 7: four components fail

State 8 and 9: five components fail

State 10 and 11: six components fail

State 12: seven components fail

Figure 7.1 The state transition diagram for the fault-tolerant two-level HVDC converter.

valves in the two-level converter, two of the seven faulted IGBT switches are certain to be located in the same converter valve. Therefore, State 12 is a failed state. The transition rate $\alpha_{10,12}$ from State 10 to State 12 is expressed as

$$\alpha_{10,12} = (\lambda_{IGBT,nf} + \lambda_{diode,nf}) * N_s * N_p * 6 \tag{7.12}$$

The transition rate is zero if there is no possible transition between two states. All non-zero transition rates obtained from the above equations are listed in Table 7.3.

Given the transition rates, the state equation of the fault-tolerant two-level converter can be

Table 7.3 Non-Zero Transition Rates of the Fault-Tolerant Two-Level VSC HVDC Converter

Transition rates	$\alpha_{0,1}$	$\alpha_{1,2}$	$\alpha_{2,4}$	$\alpha_{4,6}$	$\alpha_{6,8}$	$\alpha_{8,10}$
Value (/10^5 hours)	1.9848	1.6540	1.3232	0.9924	0.6616	0.3308
Transition rates	$\alpha_{1,3}$	$\alpha_{2,5}$	$\alpha_{4,7}$	$\alpha_{6,9}$	$\alpha_{8,11}$	$\alpha_{10,12}$
Value (/10^5 hours)	0.3305	0.6610	0.9915	1.3220	1.6525	1.9830

built as

$$\frac{d}{dt}\begin{bmatrix} P_0(t) \\ P_1(t) \\ \vdots \\ P_{12}(t) \end{bmatrix} = \begin{bmatrix} -\alpha_{0,0} & \alpha_{1,0} & \cdots & \alpha_{12,0} \\ \alpha_{0,1} & -\alpha_{1,1} & \cdots & \alpha_{12,1} \\ \vdots & \vdots & \cdots & \vdots \\ \alpha_{0,12} & \alpha_{1,12} & \cdots & -\alpha_{12,12} \end{bmatrix} \begin{bmatrix} P_0(t) \\ P_1(t) \\ \vdots \\ P_{12}(t) \end{bmatrix} \tag{7.13}$$

where the k^{th} diagonal element in the transition matrix can be obtained by summing all elements in the k^{th} column.

The probability $P_k(t)$ of the converter being in the k^{th} state at time t can be obtained by solving the state equation (7.13). Then, the reliability function can be obtained by summing the probabilities of all functional states.

$$R(t) = P_0(t) + P_1(t) + P_2(t) + P_4(t) + P_6(t) + P_8(t) + P_{10}(t) \tag{7.14}$$

The reliability functions for the fault-tolerant and non-fault-tolerant designs of the two-level HVDC converter are shown in Fig. 7.2(a). The MTTF can be obtained by integrating the reliability function over time, and the results are shown in Table 7.4. It can be observed that the MTTF for the fault-tolerant design is 21.7 years, which is greatly improved in comparison with the non-fault-tolerant design.

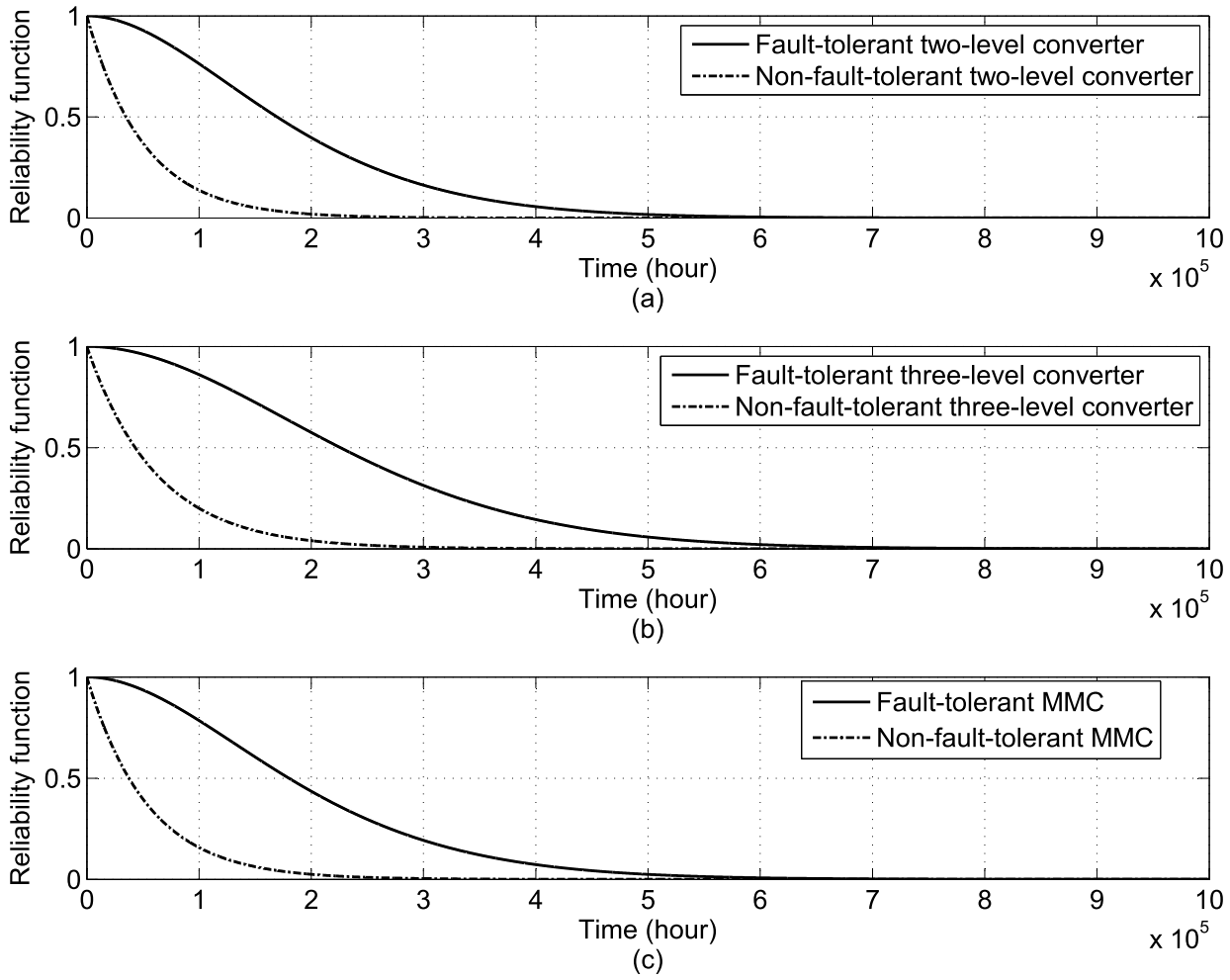


Figure 7.2 Reliability functions of the fault-tolerant and non-fault-tolerant designs of the three types of HVDC converters: (a) two-level converter; (b) three-level converter; (c) modular multi-level converter.

Table 7.4 MTTFs of the Fault-Tolerant and Non-Fault-Tolerant Designs of the Three Types of VSC HVDC Converters

Design	MTTF		
	Two-level	Three-level	MMC
Non fault-tolerant design	50426 hours (5.76 years)	62193 hours (7.10 years)	54148 hours (6.18 years)
Fault-tolerant design	190270 hours (21.72 years)	248200 hours (28.33 years)	202100 hours (23.07 years)

Table 7.5 Component Failure Rates of Fault-Tolerant and Non-Fault-Tolerant Three-Level VSC HVDC Converters

Design	Component	Failure rate ($/10^9$ hours)
Non fault-tolerant design	IGBT S1	1.522
	IGBT S2	0.799
	Diode D1	2.112
	Diode D2	1.765
	Diode D5	3.172
Fault-tolerant design	IGBT S1	1.515
	IGBT S2	0.799
	Diode D1	2.110
	Diode D2	1.765
	Diode D5	3.161

7.4 Redundant Design and Reliability Evaluation of the Three-Level HVDC Converter

The same redundant design rule can be applied to the three-level converter. As listed in Table 6.4, for normal operation, each converter valve consists of 143 switches that are connected in series. For the fault-tolerant design based on the design rule of $N + 1$, each converter valve would consist of $143 + 1$ switches. Each switch still consists of two IGBT modules that are connected in parallel. The components for the fault-tolerant three-level converter are listed in Table 7.1. By comparing Table 7.1 with Table 6.4, it can be observed that 36 extra IGBT modules (only diodes are used in 12 of 36 modules) are needed for the fault-tolerant design of the three-level converter.

The corresponding failure rates of the single IGBT and diode at different positions in each phase leg of the fault-tolerant and non-fault-tolerant designs under the full-load condition are tabulated in Table 7.5.

The state transition diagram of the fault-tolerant three-level converter is much more complicated than that of the fault-tolerant two-level converter. In the two-level converter, there are six converter valves and all valves are identical. However, in the three-level converters, there are 12

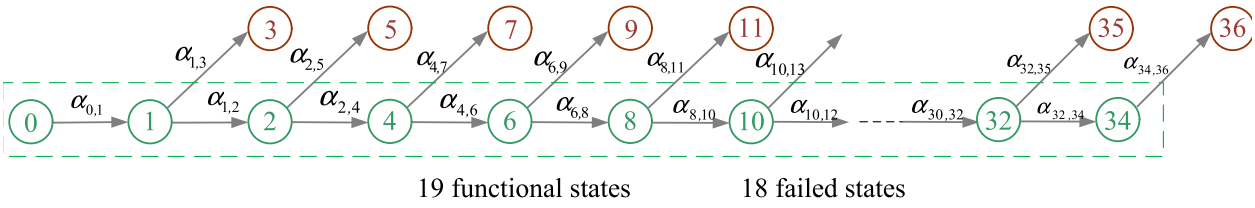


Figure 7.3 The state transition diagram for the fault-tolerant three-level HVDC converter.

switch valves and 6 diode valves. Six of these 12 switch valves are identical and have the same failure rate while the other six valves have a different failure rate. In order to reduce the number of states and simplify the state transition diagram, it is assumed that all 18 valves have the same failure rate that is equal to the highest one. The resultant state transition diagram is shown in Fig. 7.3. It can be observed that for the fault-tolerant three-level converter there are 37 states (19 functional states and 18 faulted states). The transition process can be analyzed and the transition rates can be calculated in a manner similar to the two-level converter. The detailed descriptions of these states and calculation of the transition rates is spared due to its similarity to the two-level converter.

Similar to the two-level converter, the state equation of the thee-level converter can be built. The probability of the converter being in each state at time t can be obtained by solving the state equation. The reliability function can be obtained by summing the probabilities of all functional states. The reliability functions for the fault-tolerant and non-fault-tolerant designs of the three-level HVDC converter are shown in Fig. 7.2(b). The MTTF can be obtained by integrating the reliability function over the time, and the results are shown in Table 7.4. It can be observed that the MTTF of the fault-tolerant design is 28.3 years and much higher than the MTTF of the non-fault-tolerant design.

Table 7.6 The Arm Failure Rates of the Non-Fault-Tolerant and Fault-Tolerant Modular Multilevel VSC HVDC Converters

Design	Arm failure rate ($/10^6$ hours)
Non fault-tolerant design	3.0732
Fault-tolerant design	3.1534

7.5 Redundant Design and Reliability Evaluation of the Modular Multilevel HVDC Converter

For the two-level and three-level converters, the redundant design is implemented at the component level. However, the fault-tolerant design for the modular multilevel converter can be implemented either at the component level or at the cell level. In the case of the component-based fault-tolerant design, the post-fault voltage stresses of components in cells without a faulted switch are different from the voltage stresses of components in cells with a faulted switch. Consequently, the power losses of the cells become unbalanced during post-fault operation. In contrast, for the cell-based fault-tolerant design, if a device in a cell fails, the failed cell will be bypassed and the remaining healthy cells in the arm with the faulted cell are still identical. Therefore, the cell-level fault-tolerant design has been selected in the study.

As analyzed in Section 6.4, each arm of MMC consists of 38 half-bridge cells. Based on the $N + 1$ fault-tolerant design rule, each arm of the MMC consists of $38 + 1$ cells. Since the MMC is composed of six arms, six extra half-bridge cells are needed to realize $N + 1$ fault-tolerant design. Consequently, the component selections for the fault-tolerant design of the MMC are shown in Table 7.1.

Once the fault-tolerant modular multilevel converter has been designed, the failure rates of each arm for the non-fault-tolerant and fault-tolerant designs can be evaluated. The calculated arm failure rates of the modular multilevel converter are listed in Table 7.6.

Markov model is also applied to the reliability analysis of the fault-tolerant modular multilevel

converter. According to the $N + 1$ design rule, the MMC can continue to function if less than two cells fail in each arm. When two cells in any arm simultaneously fail, the converter fails and has to stop working. The fault-tolerant MMC has the same state transition diagram as the fault-tolerant two-level converter except for transition rates. There are 13 states (seven functional states and six failed states) for the fault-tolerant MMC, as shown in Fig. 7.1. The detailed transition process and calculation of the transition rates will not presented.

The state equation of the MMC can be built, and the probability of the converter being in each state at time t can be obtained by solving the state equation. Then, the reliability function can be obtained by summing the probabilities of all functional states. The reliability functions of the fault-tolerant and non-fault-tolerant designs of the modular multilevel HVDC converter are shown in Fig. 7.2(c). The MTTF can be obtained by integrating the reliability function over the time, and the results are show in Table 7.4. It can be observed that the MTTF of the fault-tolerant design is 23.07 years and greatly improved over the non-fault-tolerant design.

7.6 Summary

The fault-tolerant design is an effective approach to reducing unscheduled shutdowns and improving the reliability of a system. The fault-tolerant designs of three types of HVDC converters have been presented and their associated reliability have been analyzed by use of a Markov reliability model in this chapter. In comparison with the standard designs, the fault-tolerant designs increase MTTFs of the HVDC converters by approximate 300%.

Chapter 8

Conlusions and Future Work

8.1 Conclusions

The reliability of key power semiconductor devices and power electronic systems is investigated in terms of the failure rate and MTTF in this thesis. A framework of reliability prediction of power electronic systems is proposed and the reliability improvement strategies for power electronic systems are also proposed. The proposed methodology of reliability evaluation and improvement has been applied to power converters in HEV and HVDC systems. The main research works and contributions are summarized as follows:

1. A framework of mission-profile-dependent reliability evaluation of power electronic systems is presented. In the framework, the effects of the thermal and electrical stresses on failure rates or lifetimes of power devices are taken into consideration. With slight modifications, the framework can be utilized to build reliability analysis model for power electronic systems in various applications. The methods of improving reliability of power electronic systems, component quality, electrical and thermal stresses, and redundancy, are also analyzed.

2. Based on the reliability assessment framework, the reliability simulation model for SHEVs' powertrain is built. The model utilizes various standard driving cycles as the mission profiles for the reliability analysis. The failure rates and MTTFs of the key components and the

overall power electronic system of an SHEV are assessed based on the urban driving cycle FTP-75 and the highway driving cycle US06, respectively. Although the simulation model is built for SHEVs, it can be applied to other types of HEVs with slight modification.

3. The reliability analysis can help designers pinpoint the least reliable link of the design and the dominant failure mechanism of key components, and then the designer can figure out reliability-oriented design to improve the reliability of systems. Based on the reliability analysis results, the variable dc-link control and the hybrid discontinuous modulation are proposed to reduce the loss and failure rate of SHEV's powertrain without any extra components.

4. Fault-tolerant operation is important for some critical applications. A fault-tolerant design of SHEV's powertrain is proposed, and its superior reliability performance have been quantitatively evaluated. The smoother transition process in the case of short-switch and open-switch faults have been experimentally verified.

5. As a critical application of power electronic technology, VSC HVDC converters' reliability is also evaluated based on the framework presented in Chapter 2. The mission-profile-dependent reliability evaluation model for VSC HVDC converters has been built, and the reliability of three commonly-used VSC HVDC converters has been evaluated in terms of the failure rates and MTTF.

6. Since the unscheduled shutdown of HVDC systems will lead to a tremendous economic loss, the fault-tolerant capability is indispensable for HVDC systems. The fault-tolerant designs of the VSC HVDC converters at the component level or the cell level have been investigated. The reliability of the fault-tolerant VSC HVDC converters is evaluated and the results show that the redundant designs greatly improve the MTTFs of the HVDC converters.

8.2 Future Work

The following topics are recommended for future research:

1. Verification of reliability of power electronic systems;

2. The reliability models of electrolytic capacitors and battery;

3. The load profile of HVDC systems;

4. The fault identification and transition of fault-tolerant VSC HVDC converters;

5. The reliability analysis and improvement of the inverters for photovoltaic application.

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