HIGH POWER, REFLECTION TOLERANT RF SOLID STATE AMPLIFIER DESIGN

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ABSTRACT

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RF amplifiers have been developed for use in the Facility for Rare Isotope Beams (FRIB) linear accelerator facility, which is currently under construction at Michigan State University. The development process has included the design, building, and testing of individual components, which together make a full-scale prototype suitable for testing purposes. These full-scale prototypes can be used in Superconducting Radio Frequency (SRF) resonator cavity conditioning, low energy linear accelerators such as the ReA3 re-accelerator, or simply bench tested.

The design of an amplifier suited for driving a linear accelerator cavity is different from an amplifier designed for more conventional applications such as FM or UHF broadcasting in several ways. Most importantly, amplifiers used in linear accelerator cavity applications are repetitively subject to full reflection load conditions which can destroy the amplifier in seconds. This necessitates the use of a circulator in every amplifier. Accelerator cavities also require power levels in the 2 – 8 kW range, which is significantly above what a single solid state power transistor can handle.

Amplifier components discussed include pallet amplifiers, along with low pass filter circuits, circulators, and power combiner blocks. Together, these four components can be used to create an amplifier system which reaches the power levels required, can tolerate a full reflection load through all phases, and meets the longevity and cost requirements set forth by the FRIB project.

To my parents Tom and Susan.

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CHAPTER 1

INTRODUCTION

On December 11th, 2008, Michigan State University was selected over Argonne National Laboratory to construct the Facility for Rare Isotope Beams (FRIB) [1]. The 550 million dollar facility was proposed almost 10 years ago, and will take another 10 years to construct, but will significantly advance the field of rare isotope research. Michigan State University has been a leader in this field since the 1960s with the construction and continued growth of the National Superconducting Cyclotron Laboratory (NSCL); however, the accelerator technology used in this facility is reaching its limits. When FRIB is finished near the end of this decade, it will completely replace the front end of the current NSCL facility, while reusing much of the experimental space. To understand the need for a new accelerator, a brief overview of a few nuclear physics concepts is necessary.

Figure 1.1 shows the expected isotope production of the FRIB facility in a format referred to as a “chart of the nuclides” [5]. The y-axis lists the number of protons in an atom, while the x-axis lists the number of neutrons. The number of protons determines the element; for example 6 protons results in the element carbon, while adding another proton results in the element nitrogen. Changing the number of neutrons in an atom does not change the element, but does change the atomic weight. Atoms with the same number of protons but different numbers of neutrons are called isotopes, and are of great interest to nuclear physicists. Referring back to the chart of the nuclides, the atoms near the x = y line are the stable isotopes that occur in nature and have lifetimes

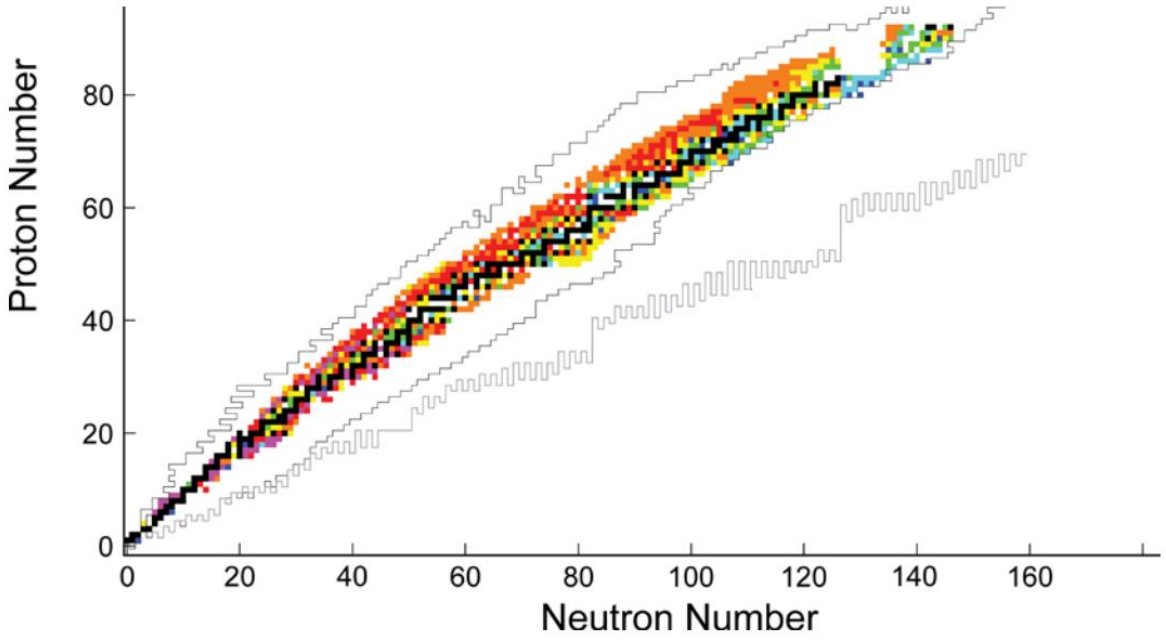

Figure 1.1: Chart of the Nuclides showing expected isotope production of FRIB. [5] For interpretation of the references to color in this and all other figures, the reader is referred to the electronic version of this thesis.

on the order of hundreds of years. Isotopes become harder to produce the farther one gets from the line of stable isotopes. The method that FRIB employs to create isotopes is to take a moderately stable heavy element such as uranium, accelerate it to about half the speed of light, and smash it into a much lighter element (liquid lithium in the case of FRIB). This is referred to as projectile fragmentation. The collision can break up the uranium into several lighter elements, as well as add or subtract neutrons to create different isotopes. Accelerating an element such as uranium up to half the speed of light is not easy, and takes about 400 kW of beam power. The isotopes that are farther away from the stable elements also have incredibly short lifetimes, on the order of microseconds, making them extremely difficult to study. The chances of creating one of these rare isotopes with a brute force approach like smashing atoms together is very rare. The existing NSCL facility at MSU has run 24 hours a day for a week in certain

experiments just to create one single copy of a rare isotope that would decay back to a more stable isotope in a matter of milliseconds. The result of this situation is that isotopes closer to the stable elements are easy to produce in larger quantities, and thus have been studied extensively. Rare isotopes on the fringe of nuclear existence are very difficult to produce in larger quantities, and thus very little is known about their properties. The main goal of FRIB is to study these rare isotopes.

The accelerator used in the existing NSCL facility uses two superconducting cyclotrons connected in series to reach about half the speed of light [3]. These cyclotrons are fairly compact and can fit in a 20 foot x 20 foot room, but their combined power usage is over a megawatt. The approach here is to use a small number of very high power accelerators to reach the desired power level. The current NSCL facility can reach power levels close to what is being proposed in FRIB, however there is a fundamental limit of cyclotrons that prevents them from creating large numbers of rare isotopes. A cyclotron works by injecting an atom into the center of three copper electrodes (called dees) that are fed with an RF source that is 120 degrees apart on each dee [4]. The injected atom will rotate in a circle around the interior of the cyclotron in sync with the applied electric filed. With each trip around the cyclotron the injected atom will gain energy, increasing the radius of the circle in which it spins, and moving it towards the outer edge. The atom will have gained full power once it reaches this edge,

Figure 1.2: Internal view of the K1200 cyclotron at MSU [5].

and it is then extracted and sent down the beamline towards the target. While the atom is in the cyclotron it makes a few thousand closely spaced rotations as it gains energy. The limitation of a cyclotron is in the number of atoms that can be packed into it at the same time. This limits the so called beam current of the cyclotron, and means that there are less rare isotopes available for study.

FRIB will employ the use of a linear accelerator, which has a different set of tradeoffs when compared to a cyclotron accelerator. While a cyclotron is a compact device that only requires one or two units to reach the desired power levels, a linear accelerator uses hundreds of lower power accelerators that are connected in series to reach the desired power levels. Refer to figure 1.3 to get an idea of the scale of the

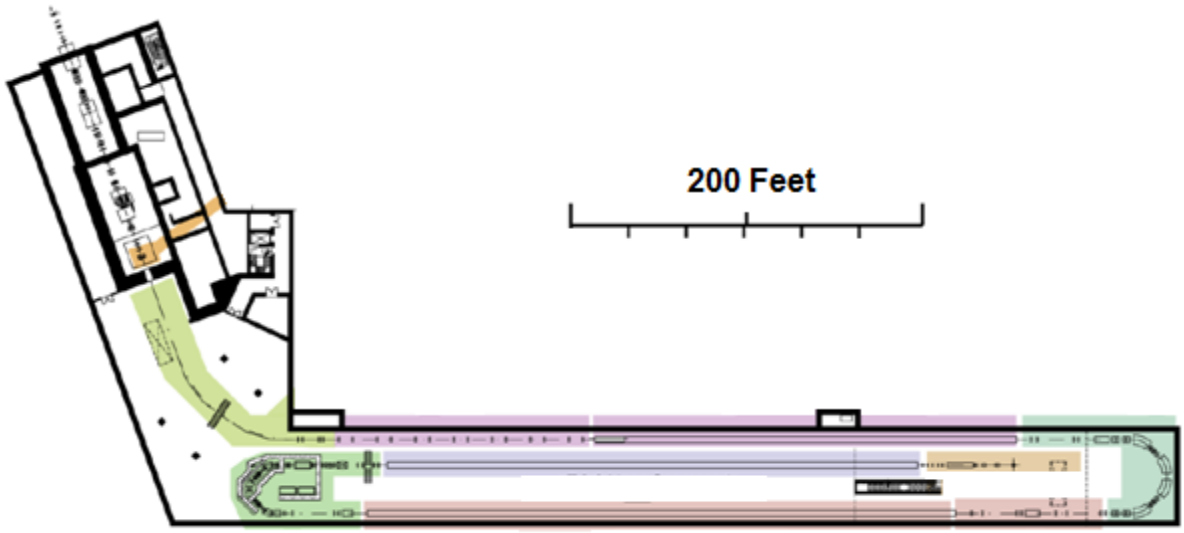

Figure 1.3: Folded arrangement of the FRIB linear accelerator [5].

FRIB linear accelerator [5]. The original plan had the entire facility running in a straight line of over 1000 feet, crossing Bogue St and starting out at McDonnell Hall. This approach was abandoned in favor of the paperclip arrangement shown above, not only because of simpler construction costs, but also because the two folding segments at either end provide an opportunity to separate out different elements produced by the ion source in relation to their weight. This configuration also allows closer spacing of the support facilities above ground.

The challenge from an electrical engineer's point of view is going from the 6 amplifiers (3 per cyclotron, and 1 per dee) of the NSCL accelerator, to the hundreds of amplifiers required for the FRIB accelerator. The amplifiers used in the cyclotron are varied between 10 MHz and 20 MHz based on the element being accelerated, and have power levels in the 100 to 200 kW range. These amplifiers are very similar to what is used in over-the-air broadcasting (FM and VHF bands), and use multiple vacuum tube

Figure 1.4: 200 kW vacuum tube amplifier final stage [5].

stages in cascade to reach the desired power levels. The final stage in a 200 kW vacuum tube amplifier is almost always water cooled, and the inlet to outlet water temperature difference can be as high as 60 °F with a flow rate of 30 gallons per minute. The amount of heat that these amplifiers must endure is enormous.

While a vacuum tube based amplifier is good for reaching very high power levels above 100 kW while maintaining an acceptable efficiency of 50 – 60%, these systems are very expensive to maintain, requiring frequent and costly tube replacement. With NSCL, the solution was to keep replacement tubes in stock, and swap them out during scheduled downtime to prevent an amplifier from going offline while an experiment was

being run. This is very costly, but the alternative is several days of downtime for an unexpected repair on a facility that costs $20 million each year to run. FRIB will require several hundred amplifiers in the 2 - 8 kW range at 80.5 MHz and 322 MHz [5]. While vacuum tube amplifiers exist in these power and frequency ranges, the downtime in a facility such as FRIB would be unacceptable. NSCL currently employs 2-3 full time technicians to maintain the cyclotron vacuum tube amplifier systems. Multiply the number of amplifiers used by 100, and it is clear that not only cost, but also labor would be prohibitive.

The lifetime of a solid state amplifier is measured in hundreds of thousands of hours, compared to the lifetime of a vacuum tube amplifier which is measured in thousands of hours. The only problem with solid state amplifiers is that presently available RF transistors are only capable of output power levels around 1 kW [6], while FRIB requires amplifiers in the power range of 2 – 8 kW.

1.1 Power and Frequency

Solid state transistors with cutoff frequencies approaching the THz band have been demonstrated [7] [8], but the power levels obtained are very small, on the order of 1 mW. On the other extreme, single solid state transistors used for conversion of 60 Hz power are available with power levels on the order of 10 kW [9]. The challenge is in creating a device that is capable of both high power and high frequency. The fundamental limits in play here are capacitance and thermodynamics.

In order to create higher frequency devices, the dimensions must shrink to reduce the capacitance between the three terminals of the transistor. The impedance of

a capacitor decreases as the frequency is raised, so above a certain frequency the effective capacitance between the gate and the source of a transistor looks like a short circuit [10]. Larger transistors have more surface area between the gate and the source, and thus more capacitance, which lowers the maximum operational frequency of the device.

Creating a high power device is based on two factors: efficiency and thermodynamics. Any input power from the DC source that is not converted to RF power at the output is converted to heat which is dissipated in the transistor. For example, a 1 kW transistor that is 67 % efficient will dissipate 500 W of heat in the transistor. The present limit on how much heat can be removed from a power transistor package while staying within safe operating temperatures is about 200 W/cm^2. The easiest way to get more power out of a transistor then is to increase the efficiency. Taking the previous example of a transistor that is 67 % efficient and somehow increasing that to slightly above 80 % would result in only 250 W dissipated in the same area, and could technically double the output power of the transistor if cooling was the only barrier to higher power. The other options for getting more power out of a transistor are to increase the thermal conductivity of the heatsink, or even the material that the device itself is made of. Different transistor materials can also have higher temperature safe operating limits. Above about 200 °C in silicon, thermal runaway and breakdown occur which will melt the device [11].

1.2 Device Technology

Solid state devices are mainly constructed from silicon, but other materials such as GaN and SiC can also be used [9]. Likewise, there is a standard vacuum tube based amplifier, along with other variants that have different power and frequency specifications, such as klystrons and gyrotrons. New device structures such as the Laterally Diffused Metal Oxide Semiconductor (LDMOS) have been used to push the power levels that can be obtained with silicon from the 10-20 W as shown in figure 1.5 to around 1 kW. This has been achieved even with the thermal conductivity and safe operating temperature limits of silicon. Switching to another device technology could theoretically enable even higher power levels than this in a single transistor. The ideal transistor material would be crystalline diamond, which has a thermal conductivity at

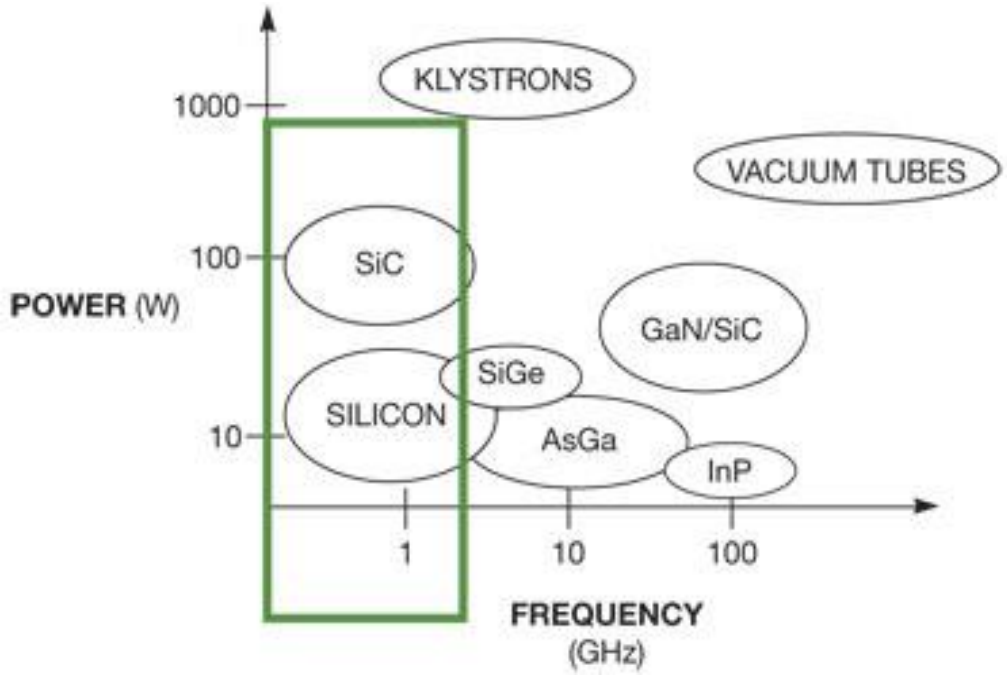

Figure 1.5: Power vs. Frequency for solid state and vacuum based devices [9].

room temperature higher than that of copper, and a safe operating temperature several hundred degrees above that of silicon [12]. Up until this point though, no one has managed to successfully create a commercially viable transistor based on diamond due to cost and manufacturing complexity. Silicon Carbide (SiC) devices are currently available, and offer operating temperatures significantly above that of silicon. These devices are capable of 10s of kW, but are targeted towards 60 Hz power conversion applications [9]. GaN based devices are available for high frequencies approaching the

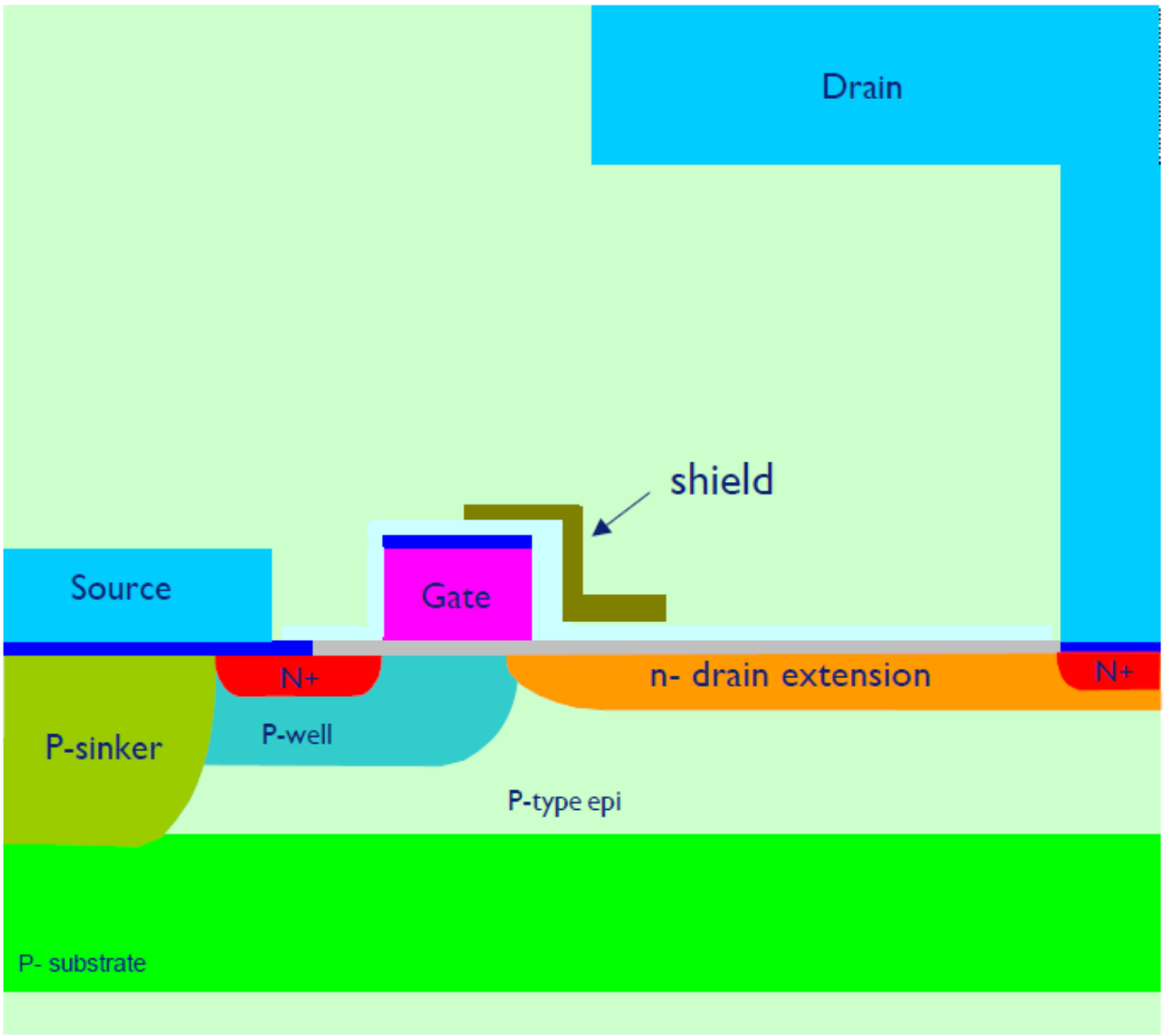

Figure 1.6: Cross section of an LDMOS transistor [13].

THz frequency range, but output power is limited [9]. When comparing the high power, high frequency landscape, vacuum tube based amplifiers still dominate.

Figure 1.6 shows the cross sectional area of an LDMOS transistor [13]. The key detail to notice here is the separation between the drain and the source. This enables higher voltage operation, which reduces the I^2R losses that heat up the device and reduce maximum power output. LDMOS technology has gone from 32 V devices, to the present 50 V devices, and 100V devices from ST Microelectronics are just starting to hit the market.

The other technique used in LDMOS transistors to increase the maximum power output is shown in figure 1.7 [13]. Several device fingers are put in parallel to increase the surface area available for cooling, and reduce the heat load on any one transistor. In a present state of the art silicon LDMOS transistor, the device area is about 1 cm by 3 cm [6]. At a power level of 1 kW and an efficiency of 67%, this translates to a heat load of about 500W, which is just under the thermodynamic cooling limit of 200 W/cm^2.

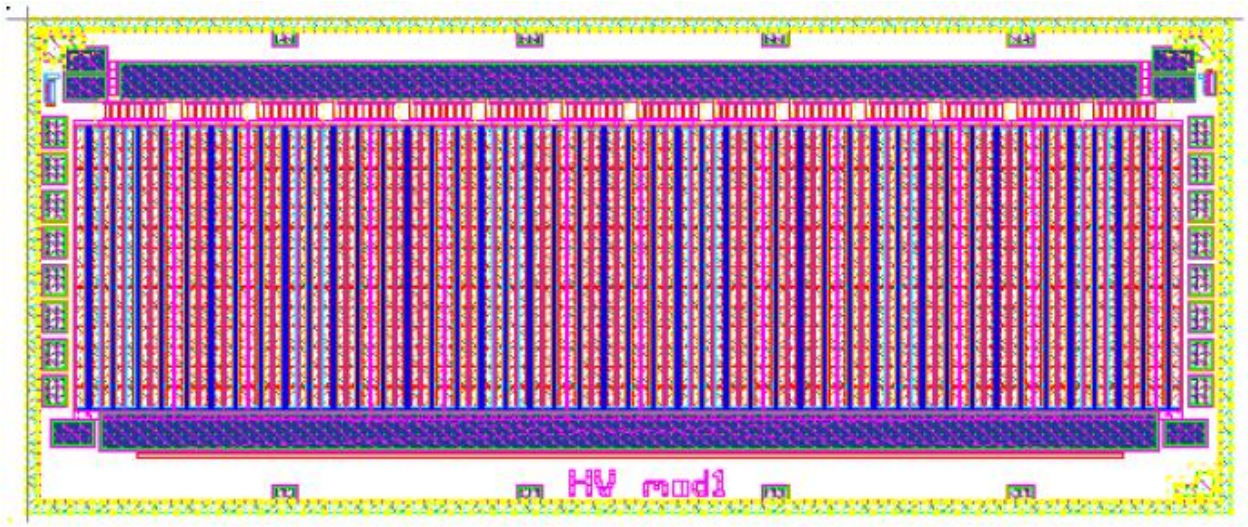

Figure 1.7: Layout of a 1 kW LDMOS device [13].

1.3 FRIB Specifications

The amplifier requirements for the FRIB project are shown in table 1.1 [5]. The amplifiers designed were for the β = 0.041 through β = 0.530 cryomodules, along with the matching cryomodules. This means the total number of high power RF solid state amplifiers needed is 344. The 6 buncher amplifiers at the front end of the beamline will be implemented used readily available 100 W solid state amplifiers, and the 200 kW Radio Frequency Quadrapole (RFQ) amplifier will use a vacuum tube based design similar to what was shown in figure 1.4.

The β of a cryomodule refers to the speed of an incoming particle with respect to the speed of light [14]. A cryomodule is simply a group of superconducting accelerator cavities that are connected to the same cryogenic cooling system, typically 6 to 8. A β value of 0.530 at the end of the linear accelerator means that the particles are traveling at about half the speed of light, while a β of 0.041 means the incoming particles are traveling at about 4.1% of the speed of light. The general operation of a linear accelerator is as follows: an ion source at the front end of the accelerator creates a

Component	Qty	# Cavities each	kW each	# Amplifiers
Multi-Harmonic Buncher	1	3	0.1	3
Energy Equalizer	1	1	0.1	1
Rebuncher	2	1	0.1	2
RFQ	1	1	200	1
β = 0.041 Cryomodule	4	4	2	16
β = 0.085 Cryomodule	12	8	4	96
β = 0.285 Cryomodule	13	6	4	78
β = 0.530 Cryomodule	18	8	8	144
Matching Cryomodules	5	2	4	10
Total	57			351

Table 1.1: RF amplifier requirements for the FRIB project [5].

charged beam of particles that can be manipulated by EM fields. This is a DC beam that is then formed into packets to be accelerated using the buncher cavities. The spacing is dependent on the design frequency of the accelerating cavities and amplifiers. This is 80.5 MHz for the β = 0.041 and β = 0.085 cavities, and 322 MHz for the β = 0.285 and β = 0.530 cavities [5]. At this point the particles are traveling very slowly. The RFQ is the first stage that imparts a significant amount of energy into the beam. It also aids in focusing the beam for the upcoming accelerator stages. Defocusing of the beam is more of a problem in the initial stages, while it becomes less of an issue at higher speeds [15]. After the RFQ, each of the 344 accelerating cavities gives a kick to the beam of particles, gradually increasing its speed from 4.1% of the speed of light at the start, to 53% of the speed of light at the finish. The change in speed is gradual, so a β = 0.285 cavity for example can accept particles with a β +/- 50%. It is most efficient at the designed β value, but having four standardized cavity designs reduces the manufacturing complexity [16]. After the last accelerating cavity, the beam of particles is sent towards the target where it is smashed against a film of liquid lithium. The hundreds of isotopes that result are then sorted by charge and mass and sent to the experimental area for study.

The design considerations for a solid state amplifier are the frequency: 80.5 MHz or 322 MHz, the power levels required, and the load conditions that will be seen by the amplifier. Frequency and power requirements are relatively straight forward, but the load conditions can be a challenge. Figure 1.8 shows the basic design of an 80.5 MHz Superconducting Radio Frequency (SRF) cavity, and a 322 MHz SRF cavity [2]. These cavities can be thought of as a basic EM resonator that holds energy in the form of

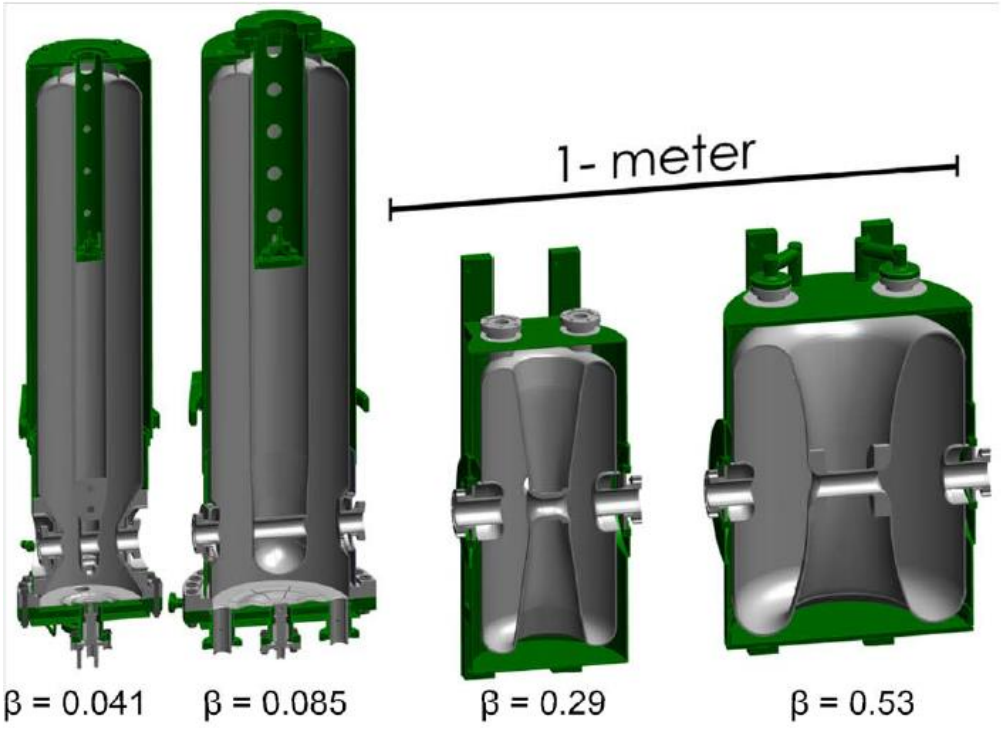

Figure 1.8: 80.5 MHz (β = 0.041/0.085) and 322 MHz (β = 0.041/0.085) cavities [2].

alternating electric and magnetic fields. By making the cavities superconducting, the losses in the walls of the cavities are reduced to almost zero, and the cavity can store a very large amount of energy. When a bunch of particles comes along, most of this energy is transferred to the beam, and the stored energy in the cavity is emptied. When more energy is being put into the cavity, this is an ideal load condition from the point of view of the RF amplifier. Most of the power coming from the amplifier is being transferred to the cavity, and very little is being reflected back. However, when the cavity is full of energy, most of the power from the amplifier is reflected back. So a power transistor that was designed to handle 500W of heat could now see up to 1.5 kW of heat. This is a major issue that must be accounted for in the design of these RF solid state amplifiers.

1.4 Thesis Layout

The design of an FRIB spec amplifier will be covered from start to finish. The main requirements are frequency (80.5 MHz or 322 MHz), power level (2 kW, 4 kW, or 8 kW), and reflection tolerance (able to tolerate full reflection under any condition).

Chapter 2 discusses the basic building block for any solid state amplifier: the pallet amplifier. This is simply a circuit board with input and output matching networks, along with gate and drain biasing circuitry built in. Two stages of amplifiers will be used: a pre-amp and a power-amp. The input signal level is a standard 10 dBm, with an output of between 63 dBm and 69 dBm. Since the 1 kW power transistors selected are only capable of 20-30 dB of gain, a second stage before the power stage with a gain of 30-40 dB is required.

Chapter 3 will cover the Low Pass Filter (LPF) used after the pallet amplifier stage. To get the highest efficiency out of a power transistor, it is necessary to drive it into class C operation, which has a side effect of producing significant harmonics. In this case the added cost and complexity of an LPF is worth the price due to the increase in efficiency from running in class C. The design used is a 7th order Butterworth LPF with a harmonic absorbing stage built in.

Chapter 4 covers circulators, which are three terminal devices used to redirect reflected power away from the transistor and towards a dummy load. Circulators are frequency dependent devices, so the design of an 80.5 MHz circulator is different and significantly more challenging than the design of a 322 MHz circulator. The mechanism in play here is the temperature dependence of the ferrite material used in the circulator.

As power is applied to the device the ferrite heats up, changing the operating frequency band of the device, and potentially pushing it out of range.

Chapter 5 covers the design of power combiners optimized for high power. Since a single power transistor can only reach power levels of 1 kW, a new approach must be taken to reach the 2 – 8 kW power levels required by FRIB. Of interest is the power handing of each type of combiner, but also the mismatch tolerance in case one amplifier is producing more or less power, or the phase is off by a certain amount. The power combiner types tested include a basic TEE combiner, a Wilkinson combiner, and a Hybrid combiner.

Chapter 6 covers the integration of an entire amplifier system using all of the components mentioned above, along with testing procedures to verify performance. In addition to the high power components mentioned above, low power control circuitry on the input side is required to keep signals in phase and to match amplitudes. Feedback and EMI can also be a significant issue in an amplifier system with 60 dB of gain.

Chapter 7 concludes with an overview of what was accomplished, and the potential for improvement before construction of the FRIB project. Future work is also discussed, including a class H amplifier topology that can be used to increase efficiency at lower power levels, a reflection tolerant amplifier design that eliminates the need for costly and complex circulators, and finally the potential for using future diamond based transistors in an FRIB spec amplifier.

CHAPTER 2

PALLET AMPLIFIERS

A pallet amplifier is simply a circuit board built around a single transistor. Pallet amplifiers are meant to be inexpensive, modular, and easy to tune for a specific application. True wideband transistors are rare, and in most cases, both input and output matching networks need to be designed around the desired frequency of operation. This means that the same transistor can be used in multiple different pallet amplifier configurations to reach different frequency bands of operation. Most popular is the 88 MHz – 108 MHz frequency band used for FM radio broadcasting in the US, and amateur radio broadcasting in other countries. This usage has facilitated the design and construction of several pallet amplifiers in this frequency range [17]. UHF broadcasting in the hundreds of MHz range is another source of standardized pallet amplifier designs. Pallet amplifiers also include biasing circuits in the form of filtered power supply connections to the gate and drain terminals of the transistor. A basic block diagram of a pallet amplifier setup is given in figure 2.1.

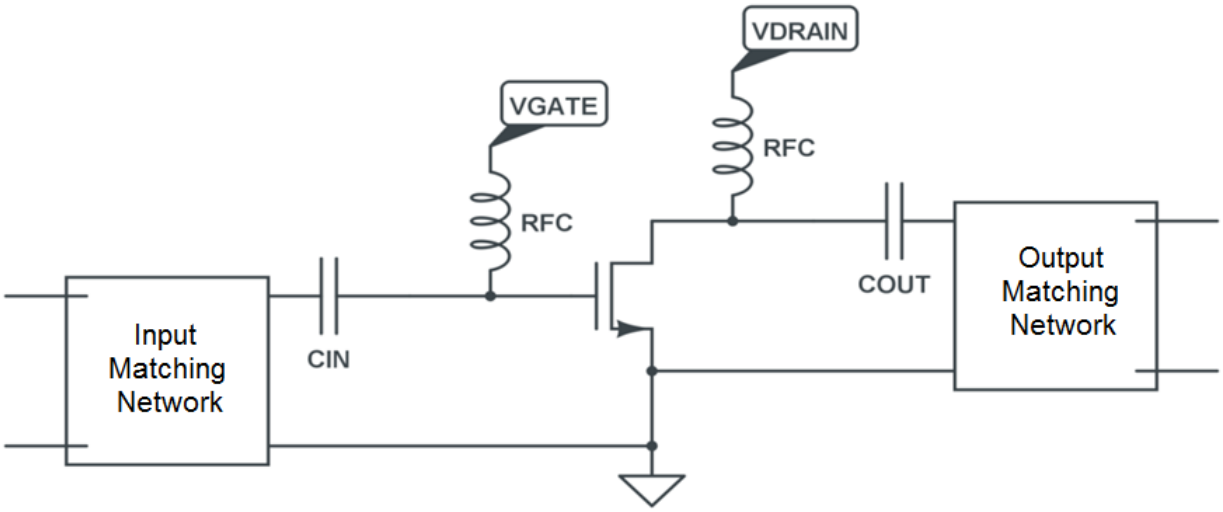

Figure 2.1: Impedance matching and biasing in an RF pallet amplifier.

2.1 Impedance Matching and Biasing

Matching networks below 100 MHz are usually implemented with lumped element components and transmission line transformers. Above 100 MHz, the shorter effective wavelength in the dielectric materials enables the use of microstrip based matching circuits [18]. These are lower cost and require less labor intensive manufacturing techniques. The result of this divide is that the 80.5 MHz pallet amplifier was designed using lumped elements and transmission line transformers in the matching networks, while the 322 MHz amplifier uses microstrip based matching networks. Pallet amplifiers in between these two frequency ranges often employ the use of both techniques.

In addition to impedance matching networks, a pallet amplifier also includes biasing circuits for the gate voltage and drain voltage. These can be varied to adjust the class of operation of the pallet amplifier, to hit goals of high efficiency or low harmonic distortion, just by changing a power supply voltage. Finally, a pallet amplifier will have input and output RF connections in the form of SMA, N-type, or 7/16 connectors, depending on the power levels required and frequency of operation.

Figure 2.2 shows a complete schematic of a 1 kW 80.5 MHz pallet amplifier designed around the NXP BLF578 transistor [6], [18]. The 50 ohm input is first balanced, after which the impedance is lowered using a 4:1 transmission line transformer. The output of the transistor is high current and low voltage, so the impedance must be raised by a 1:4 transmission line transformer, before it is converted back to an unbalanced signal. Biasing connections for a 43 V drain voltage and a 1.35 V gate voltage are provided. .

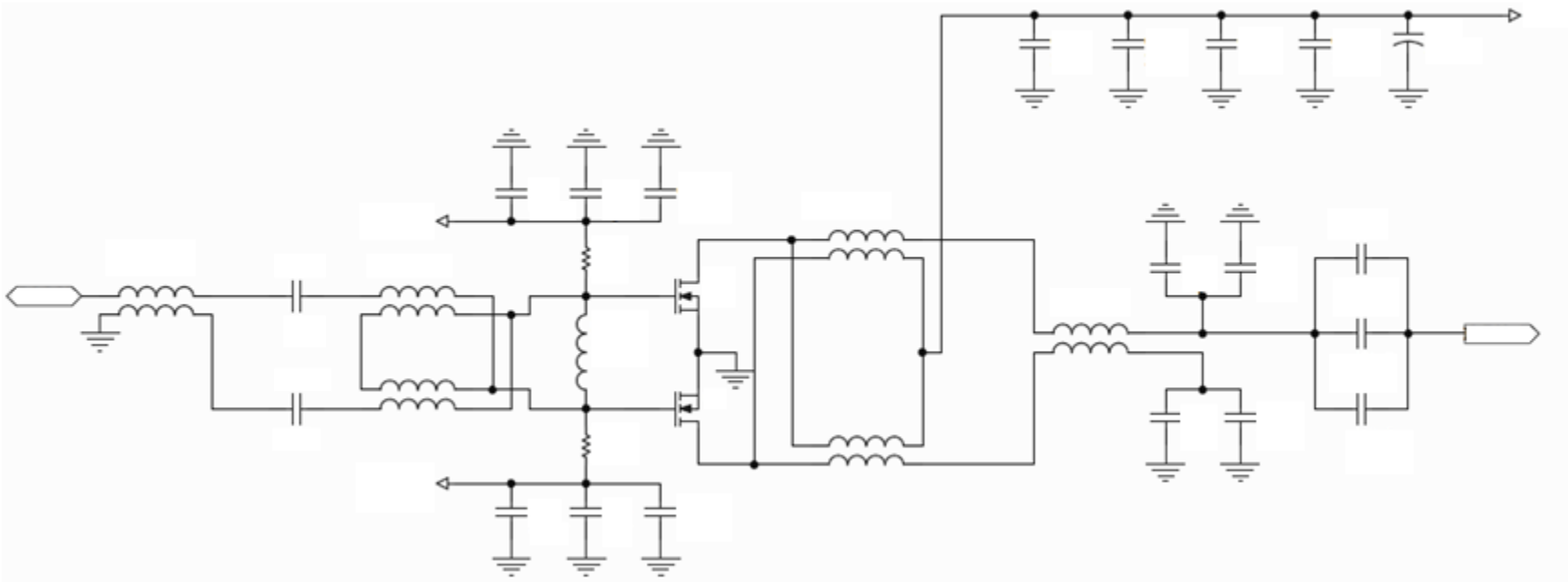

Figure 2.2: Schematic of a 1 kW solid state amplifier using an NXP BLF578 transistor.

2.2 Circuit Design

Three different types of transistors are available for use in solid state amplifiers: Bipolar Junction Transistors (BJTs), Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), and Insulated Gate Bipolar Transistors (IGBTs) [18]. A BJT is a current controlled current source; a small input current at the base controls a large output current between the collector and emitter. A MOSFET is a voltage controlled current source; a small applied voltage at the gate controls a large output current between the drain and source. Finally, an IGBT is a combination of these two devices; a small voltage is applied to the gate, which controls the current flow though a bipolar junction. IGBTs offer high power, but not high frequency, while BJTs offer high frequency, but not high power [9]. MOSFETs offer both high power and high frequency.

The next consideration is the amplifier topology; for a MOSFET either common gate, common drain, or common source [11]. A common gate amplifier provides voltage gain, but no current gain. A common drain amplifier, also known as a buffer, provides current gain, but no voltage gain. A common source amplifier provides both voltage and current gain, and thus is ideal for a power amplifier application.

The final circuit design consideration is the interconnection of multiple transistors used to achieve higher power levels. In an amplifier cascode, a common source amplifier is used as a driver for a common gate amplifier, providing both power and voltage gain. In an amplifier cascade, two common source amplifiers are connected input to output to achieve higher power gain than a single stage can provide. Another option is the balanced amplifier, in which two transistors are used to achieve double the voltage swing, and four times the power output [11].

2.3 Pre-amp Pallets and Power-amp Pallets

FRIB amplifiers require a maximum power output of 8 kW, which is equivalent to 69 dBm. The input source driving the amplifiers can vary between 0 dBm and 10 dBm, meaning a total gain of up to 70 dB is required. The only way to achieve this is with two separate gain stages cascaded, referred to as a pre-amp stage and a power-amp stage. The standard pallet amplifier block used will be designed for 1 kW of output power, or 60 dBm. The required gain and power output values for the pre-amp pallet can be determined by working backwards. The power-amp stage is capable of a maximum of 25 dB of gain at full power output, meaning that the pre-amp stage must be able to output at least 35 dBm of power. This is slightly under 4 W, and the minimum input power limit of 0 dBm dictates that the gain must be at least 35 dB.

The final design uses a 10 W preamp stage with 40 dB of gain, and a 1 kW power-amp stage with 25 dB of gain. With a full 10 dBm input signal, the output power would be 10 dBm + (40 + 25) dB = 75 dBm, which is more than enough to melt the output stage. The solution is to use the input signal level to control the final output signal level. If the gain levels were ideal, this would require an input of -5 dBm. If the gain of the pallet amplifier varies due to manufacturing tolerances, cable losses, or even temperature changes, the input signal level can be varied to maintain a stable output power.

Figure 2.3 shows the selected pre-amp pallet amplifier [17]. There is plenty of gain and power available in this pallet amplifier, so it is run in Class A operation, limiting the amount of harmonics generated while sacrificing maximum efficiency. This is a worthwhile tradeoff due to the small power levels of the pre-amp stage.

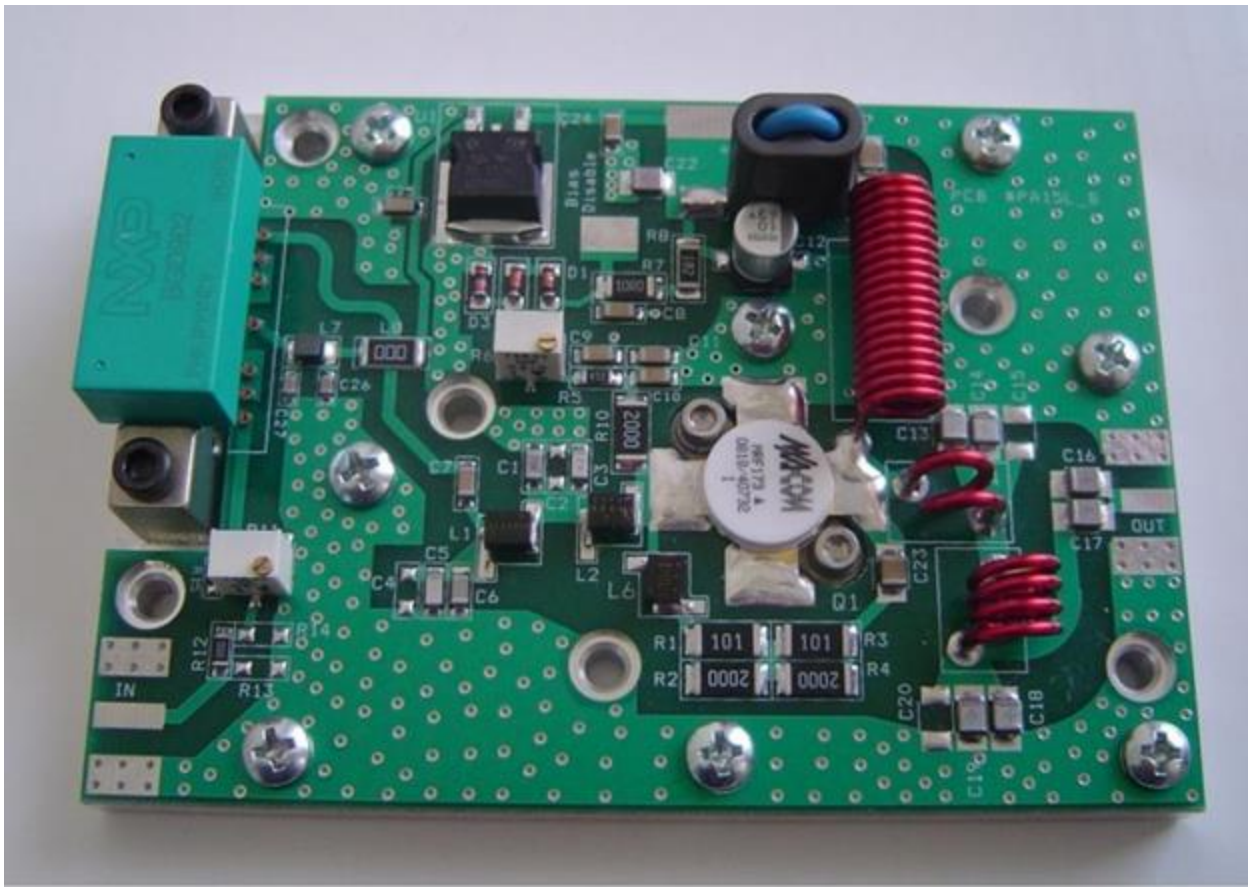

Figure 2.3: 10 W 80.5 MHz pallet amplifier [17].

Reducing harmonics before the input to a high power amplifier is significantly more efficient than trying to remove them after the power-amp stage. With a clean input signal, the harmonics generated in the final stage will be due exclusively to the power-amp pallet.

The selected power-amp pallet amplifier is shown in figure 2.4 [17]. This pallet uses two transistors capable of 1 kW each, but is operated at 1 kW total output to reduce the heat load on each transistor. There are two identical pallet amplifier stages used in this module, each running at around 500 W. A hybrid coupler is used on the input (right) as a two way power splitter, while a hybrid coupler is used on the output

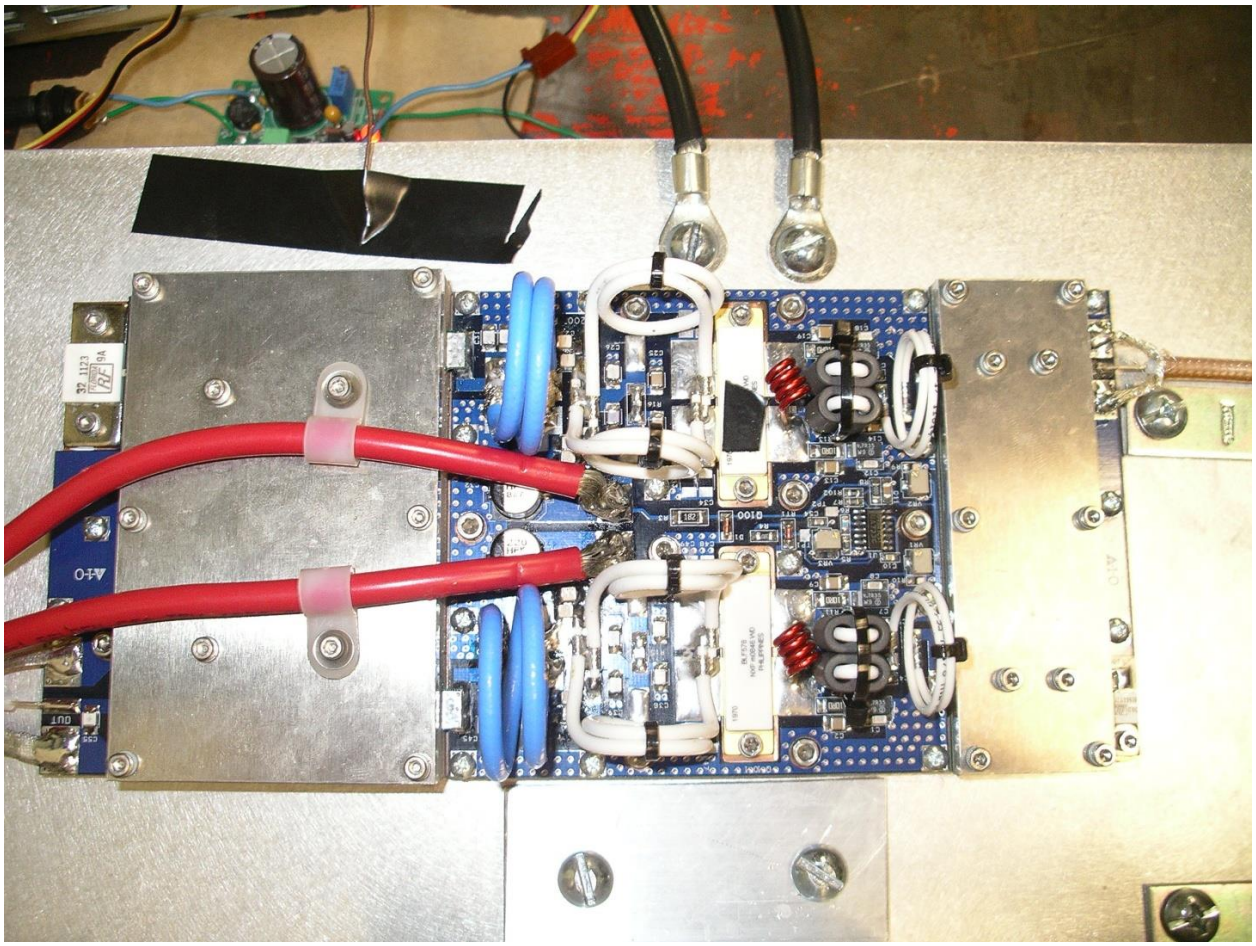

Figure 2.4: 1 kW 80.5 MHz pallet amplifier [17].

(left) as a two way power combiner. Input and output RF connectors on the pre-amp are SMA, while the output RF connector on the power-amp is a 7/16 DIN connector, due to the high power levels obtained.

2.4 Amplifier Classes and Efficiency

The standard classes of operation for an amplifier are Class A, Class AB, and Class C [11]. Different classes of operation can be achieved through the design of the amplifier, and by changing the gate and drain bias voltages.

Class A amplifiers have the lowest distortion, but are also the least efficient of the three classes of operation. This is because the transistor is biased on even when no input signal is applied. When the transistor is always on, distortion effects due to the process of switching the transistor on and off are reduced. Low distortion is the reason for running the pre-amplifier in Class A operation.

Class AB is possible in a balanced amplifier configuration, and employs the use of two transistors. While the output signal is high, the top transistor is biased on and the bottom transistor is biased off. When the output signal is low, the bottom transistor is biased on and the top transistor is biased off. This saves a significant amount of power when compared to class A, since one of the two transistors is always biased off. The downside is crossover distortion that occurs when the output is switched from a high to a low state. This can be reduced, but never completely eliminated, meaning that the distortion performance of a Class A amplifier will always be better than Class AB.

Class C operation is the most efficient, but also has the highest amount of distortion. This is because the transistor is biased off by default, and only the addition of an input signal can bias the transistor on. Class C amplifiers are also run very close to saturation, which maximizes the efficient use of the available DC input power, but creates significant harmonic distortion that must be removed before sending the output signal to an accelerating cavity.

2.5 Effects of Gate and Drain Biasing Voltages

Many of the effects of biasing on an amplifier can be understood simply by measuring the performance characteristics of the amplifier while changing the gate and drain voltages and plotting the results. This is shown in figures 2.5 – 2.12. All of these measurements were carried out by the author by hand, using a 2 kW amplifier module. Input power and output power were measured using a vector voltmeter, while harmonic content was measured using a directional coupler and a spectrum analyzer. Efficiency was calculated after measuring the drain current using a high current clamp meter, and temperature was measured with a thermocouple attached to the amplifier heatsink. Measurement values were allowed to stabilize for 5 minutes before moving on to the next measurement.

Figure 2.5 and figure 2.6 show the effects of changing the drain voltage and the gate voltage of the transistor on the gain with respect to the output power. Two trends can be observed. First, the gain starts out lower at small output power levels, raises as the output power increases, and lowers as the power output reaches maximum. This lowering of the gain is due to saturation of the transistor as the output voltage swing nears the drain to source voltage. The second trend is the difference in effect between changing the gate voltage and changing the drain voltage on the gain. When the drain voltage is varied, the gain values converge at low power output levels and diverge at high power output levels. When the gate voltage is varied, the gain values diverge at low power output levels and converge at high power output levels. This shows that the gate voltage controls the gain at low power output levels, while the drain voltage controls the gain at high power output levels.

Figures 2.7 and 2.8 show the effects of changing the drain voltage and the gate voltage of the transistor in relation to the input and output power levels of the final gain stage of the amplifier. This is the same data used in figures 2.5 and 2.6, but presented in a different way. These plots further exemplify the effect of the gate voltage on power output at low power and the effect of the drain voltage on the power output at high power, while also showing the saturation effect in more detail.

Figures 2.9 and 2.10 show the effects of changing the drain voltage and the gate voltage of the transistor in relation to harmonic distortion on the output. In this case, the third harmonic is shown plotted vs. a changing drain voltage and a changing gate voltage. It can be seen again that the gate voltage controls the output performance at low power levels, and the drain voltage controls the output performance at high power.

Figure 2.11 shows the effect of changing the drain voltage on the efficiency of the amplifier. The general trend observed here is that efficiency increases as the power output is raised, and decreasing the drain voltage results in a higher efficiency, but lower maximum power output before saturation is reached. Maximum efficiency is always reached when the amplifier is as close to saturation as possible. This can either be achieved by increasing the output power, or keeping the output power constant and lowering the drain voltage.

Finally, figure 2.12 shows the effect of changing the drain voltage on the temperature rise of the amplifier. It makes sense that a more efficient amplifier would have a lower operating temperature, and this is confirmed by the plotted results. Also notice that the temperature rise from minimum power output to full power output is only 10 °C. This shows the effectiveness of the water cooling system employed.

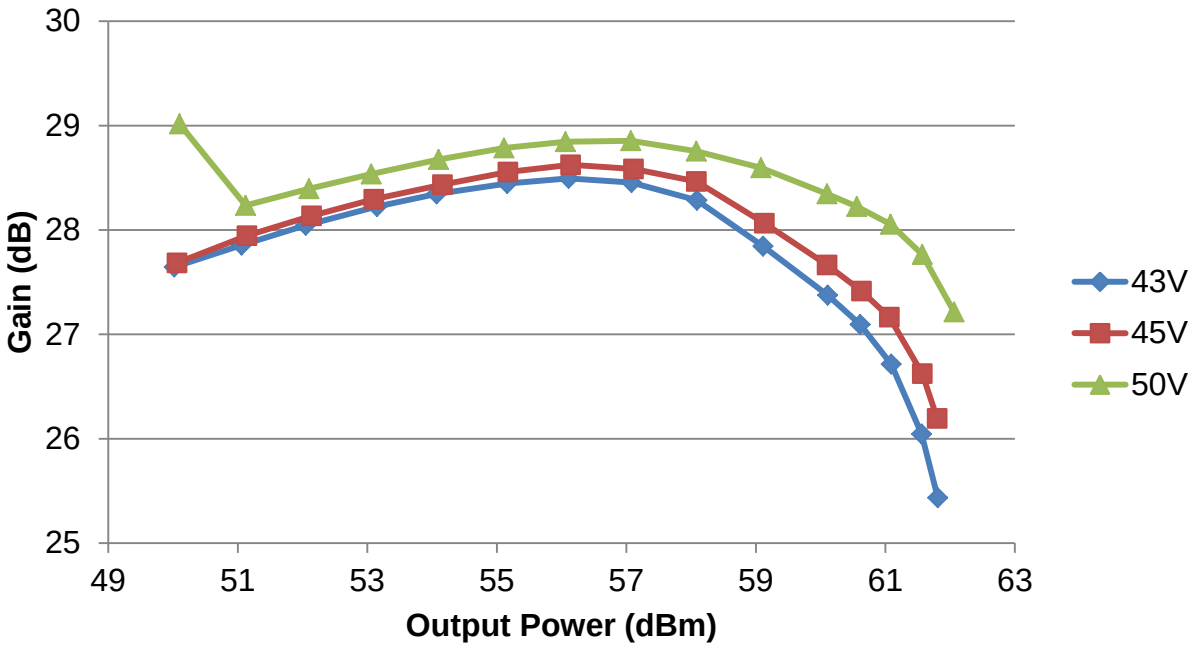

Figure 2.5: Gain vs. output power with a varying drain voltage.

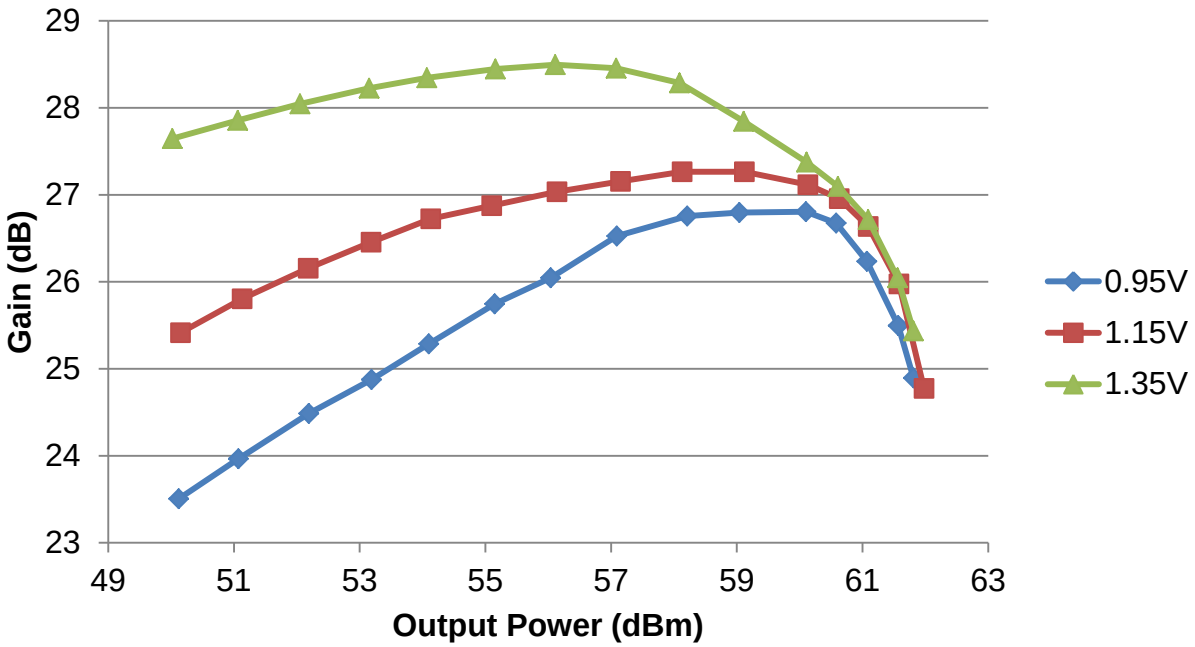

Figure 2.6: Gain vs. output power with a varying gate voltage.

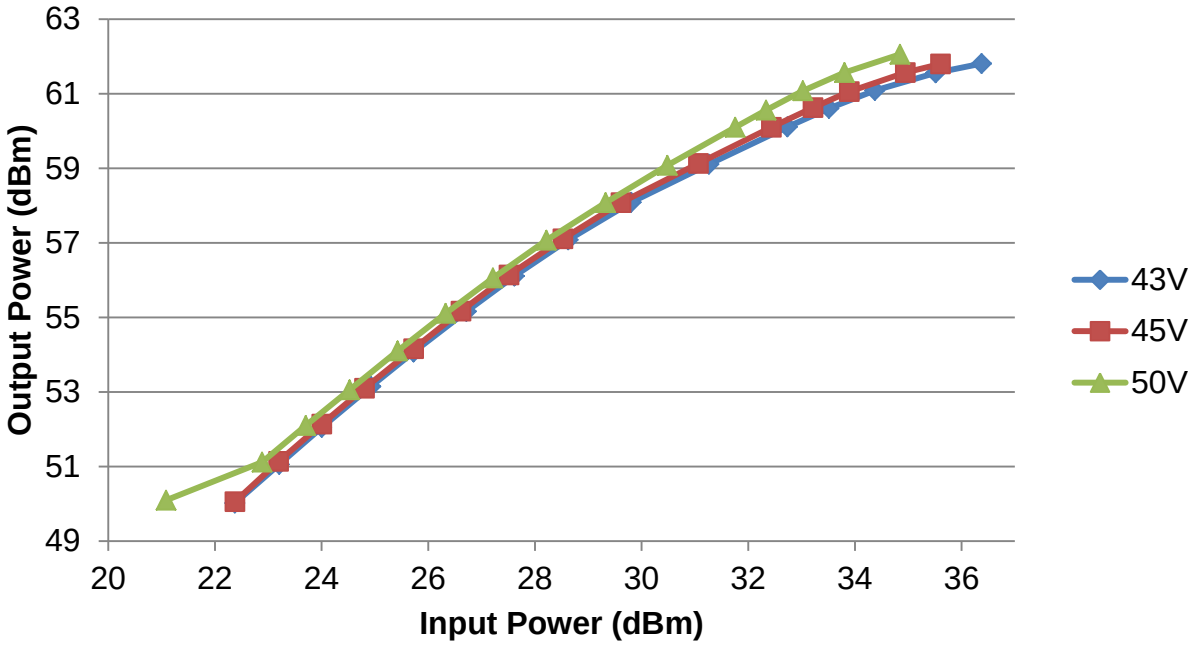

Figure 2.7: Output power vs. input power with a varying drain voltage.

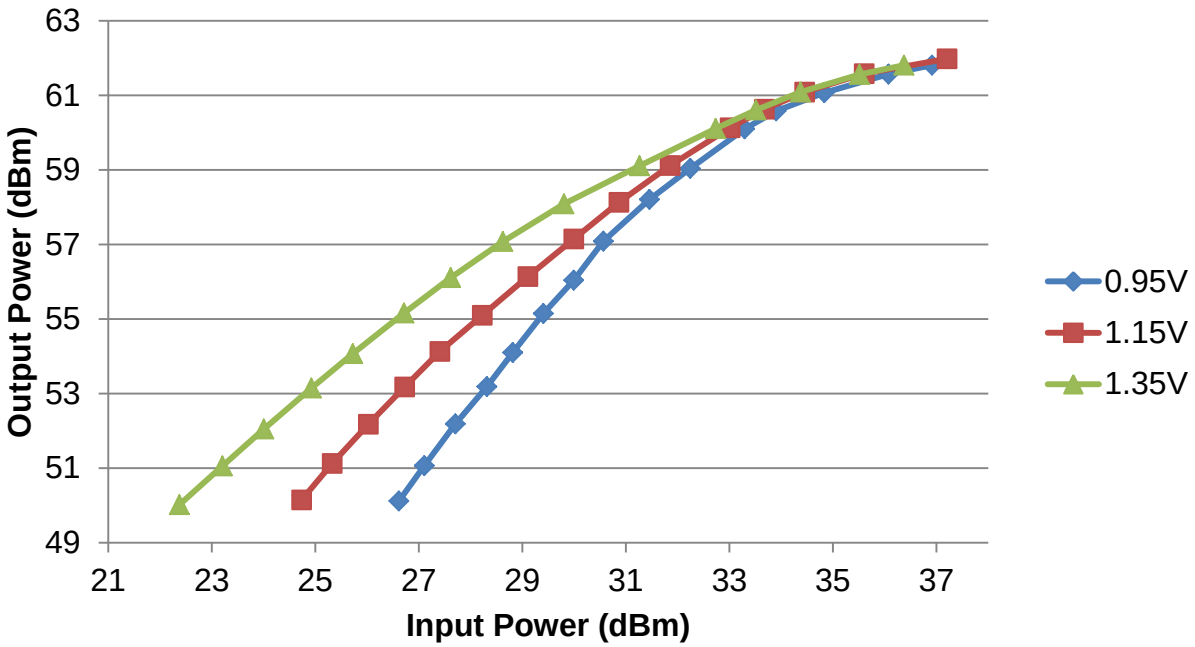

Figure 2.8: Output power vs. input power with a varying gate voltage.

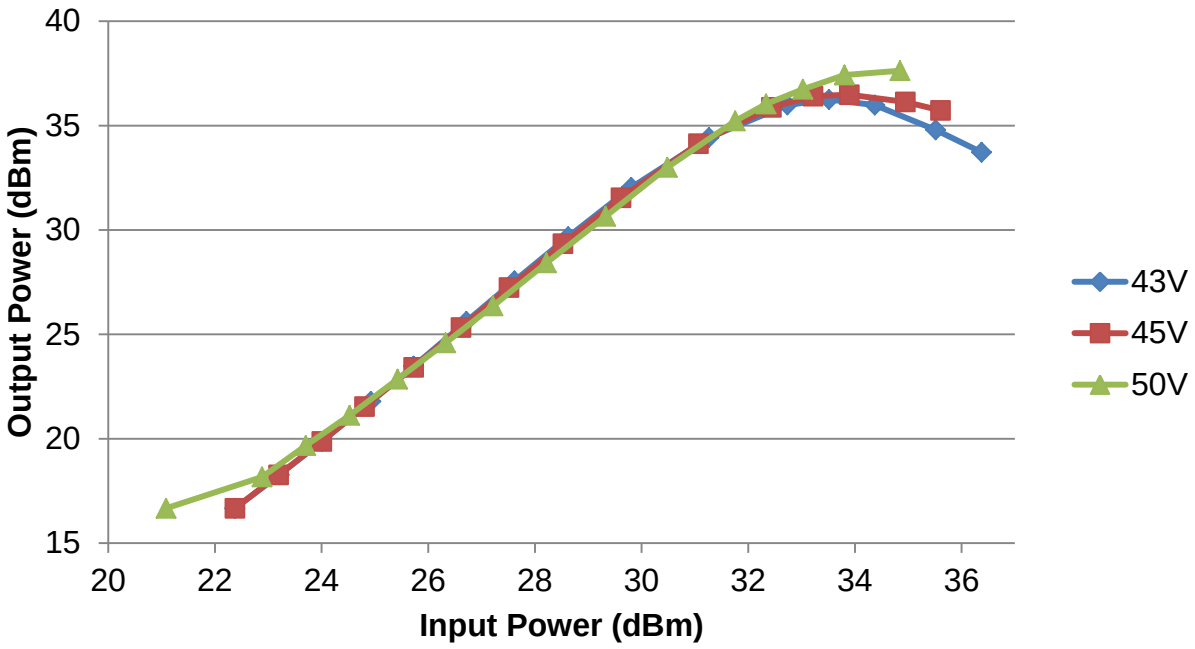

Figure 2.9: Third harmonic distortion vs. input power with a varying drain voltage.

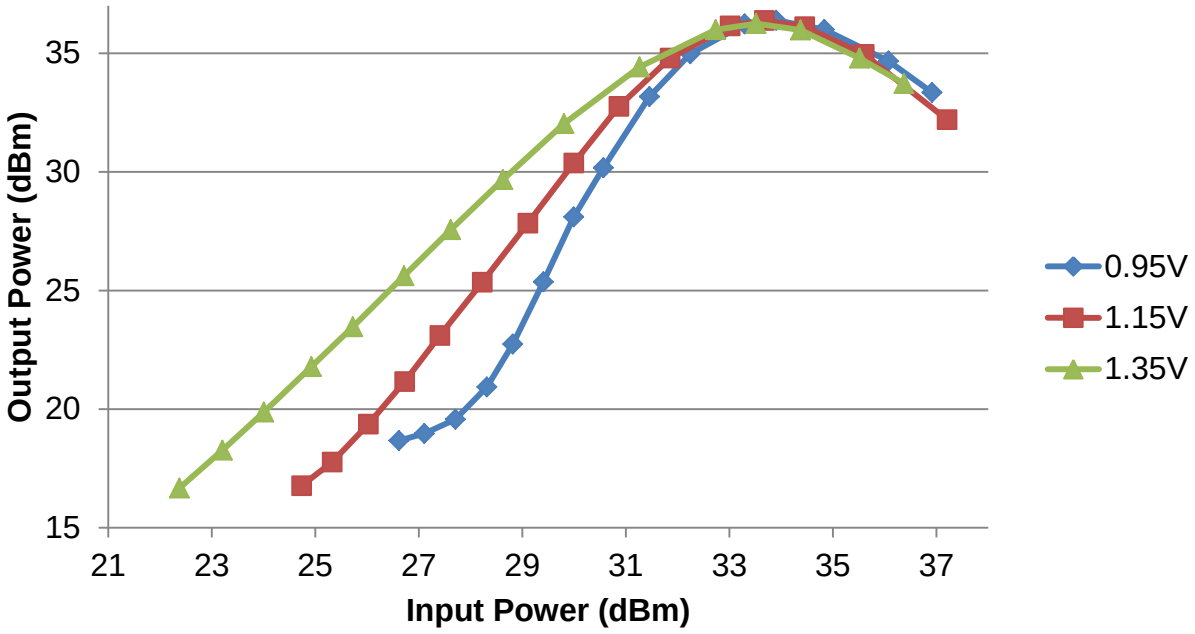

Figure 2.10: Third harmonic distortion vs. input power with a varying gate voltage.

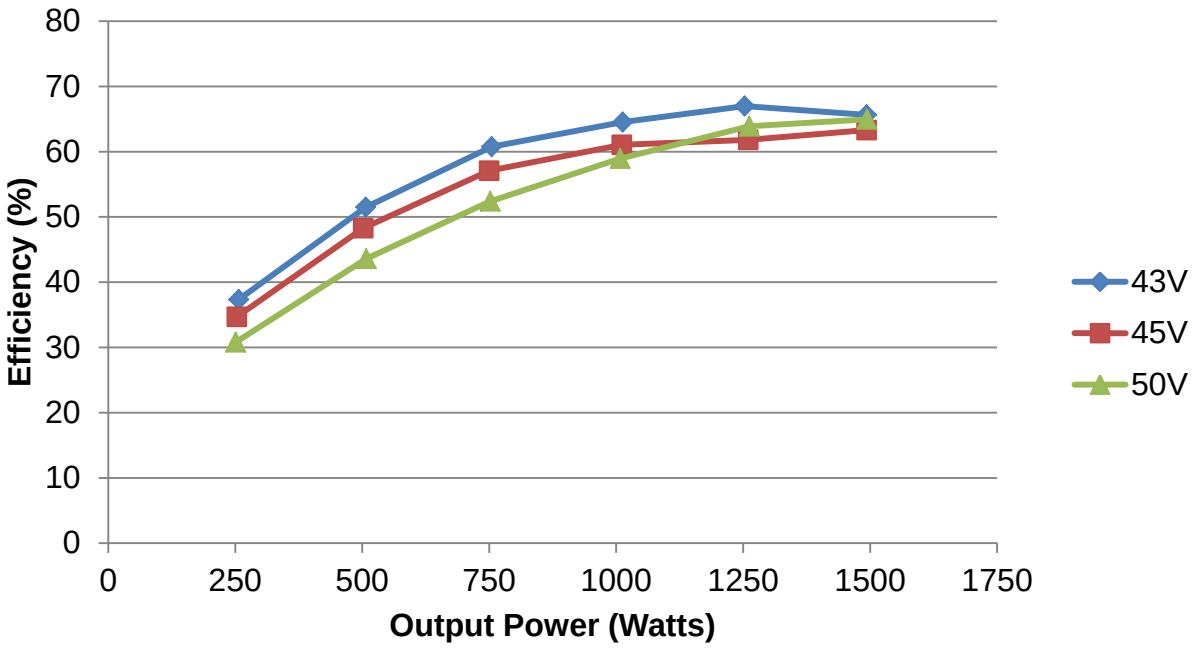

Figure 2.11: Efficiency vs. output power with a varying drain voltage.

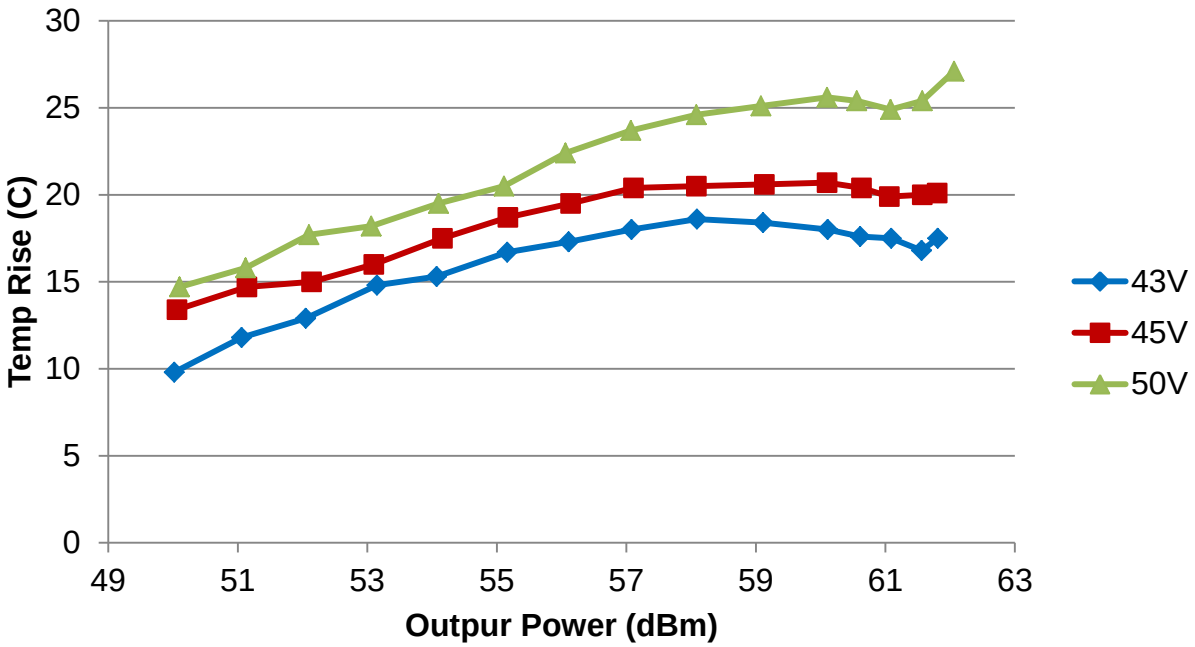

Figure 2.12: Temperature rise vs. output power with a varying drain voltage.

CHAPTER 3

LOW PASS FILTERS

Running an amplifier in Class C has the benefit of producing high efficiencies approaching 70%, but also creates significant harmonic content that must be removed for a linear accelerator cavity application. The input signal is kept clean by using a Class A pre-amp, but significant distortion is still present at the output of the power-amp. The FRIB linear accelerator cavities require a drive signal with harmonics that are -70 dBc, or 70 dB less than the carrier signal level of 63-69 dBm [5]. This requires a 7th order filter [10], which is shown in figure 3.1 [17]. The inductors are wound from 10 gauge wire, and the capacitors are implemented on the circuit board with a parallel plate capacitor supplemented with high power chip capacitors in parallel. A Butterworth response was selected to eliminate ripple in the pass band, since 3 dB of loss in the

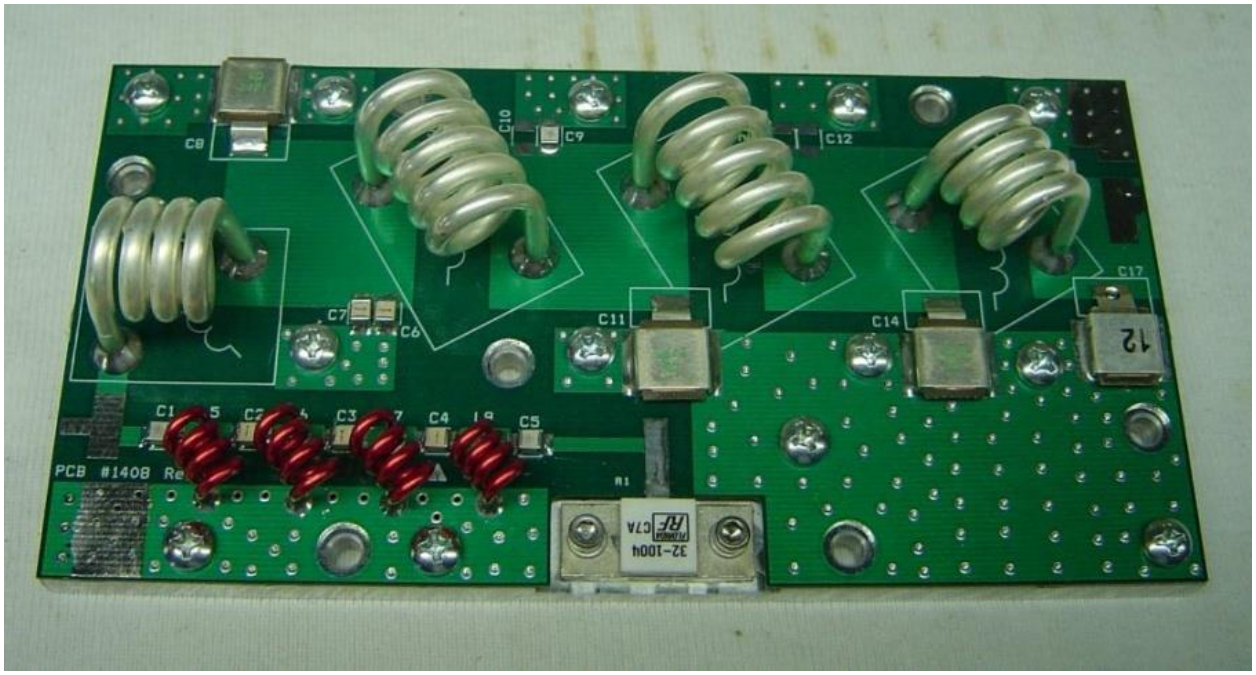

Figure 3.1: 7th order low pass filter, with a harmonic absorbing high pass filter [17].

passband of a 1 kW low pass filter would equate to 500 W of lost power. Finally, a harmonic absorbing high pass filter is included on the input to terminate most of the harmonics into a 50 ohm load, rather than reflect them back towards the transistor.

3.1 Measured Performance

The response characteristics of the filter are shown in figures 3.2 and 3.3 in the form of network analyzer screen captures. These figures and all subsequent figures including network analyzer screen captures will be presented in landscape format to make the small print of the standard Agilent files as easy to read as possible. In the case that information such as frequency markers cannot be read directly from the screen captures, important performance metrics will be included in the caption. The insertion loss presented in figure 3.2 is what would be expected for a 7th order filter, and shows a sharp drop off at the cutoff frequency of 400 MHz. The fundamental at 322 MHz is passed with 0.1 dB of insertion loss, and the second harmonic at 644 MHz is reduced by 75 dB.

Figure 3.3 shows the return loss of the 7th order low pass filter. While a plot of insertion loss shows attenuation of a signal as it passes though a two terminal network, return loss shows a drop in the level of the reflected signal compared to the incident signal in a two terminal network. The desired result is a large negative value of return loss in the pass band, and a value close to zero in the stop band. An insertion loss near zero means almost all of the incident power is reflected. These parameters show similar information in inverted form, but insertion loss of a low pass filter shows more detail in the stop band, while return loss shows more detail in the pass band.

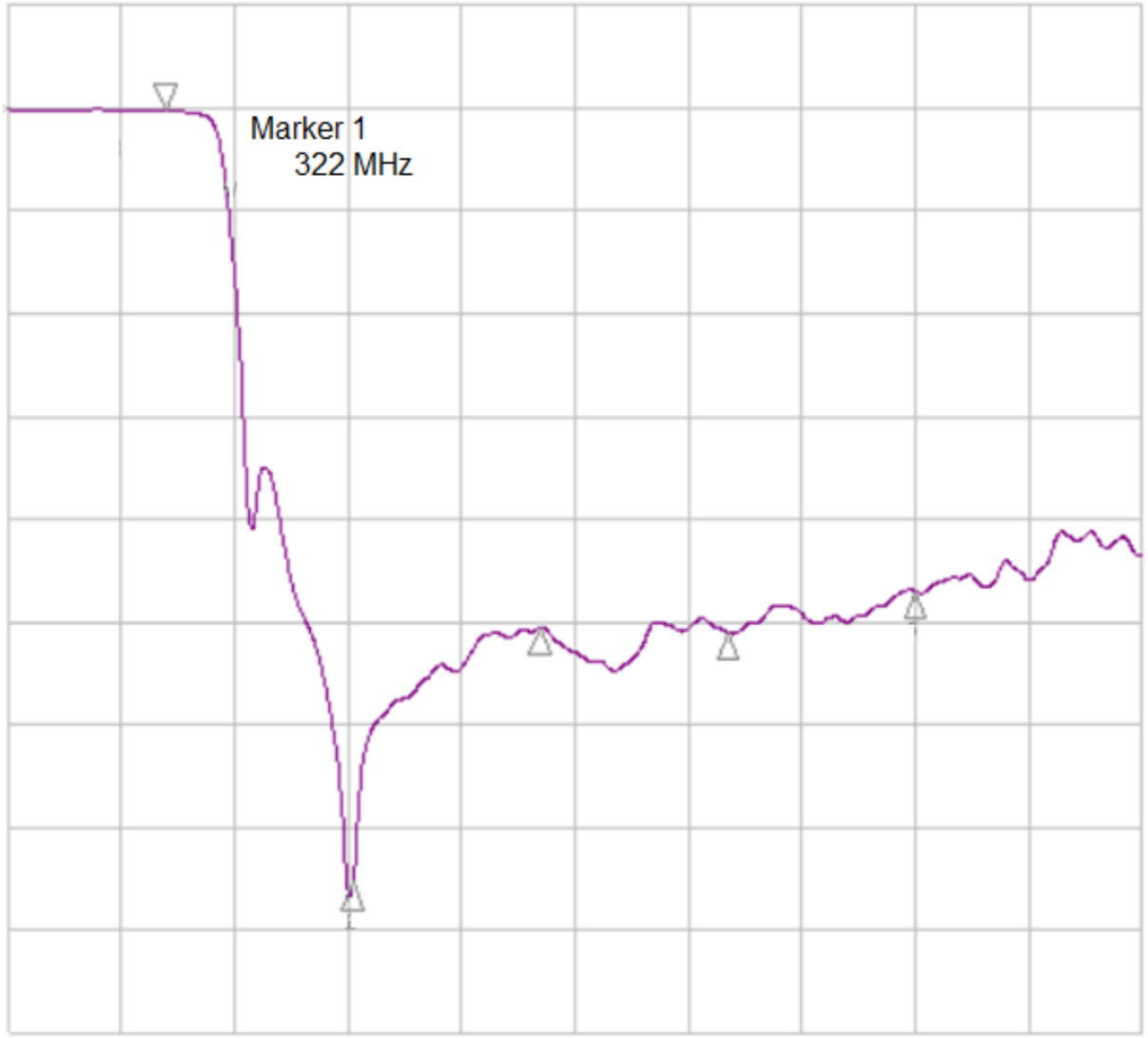

Figure 3.2: Insertion loss of a high power low pass filter. S21 = -0.1 dB at 322 MHz, and S21 = -70 dB at 644 MHz.

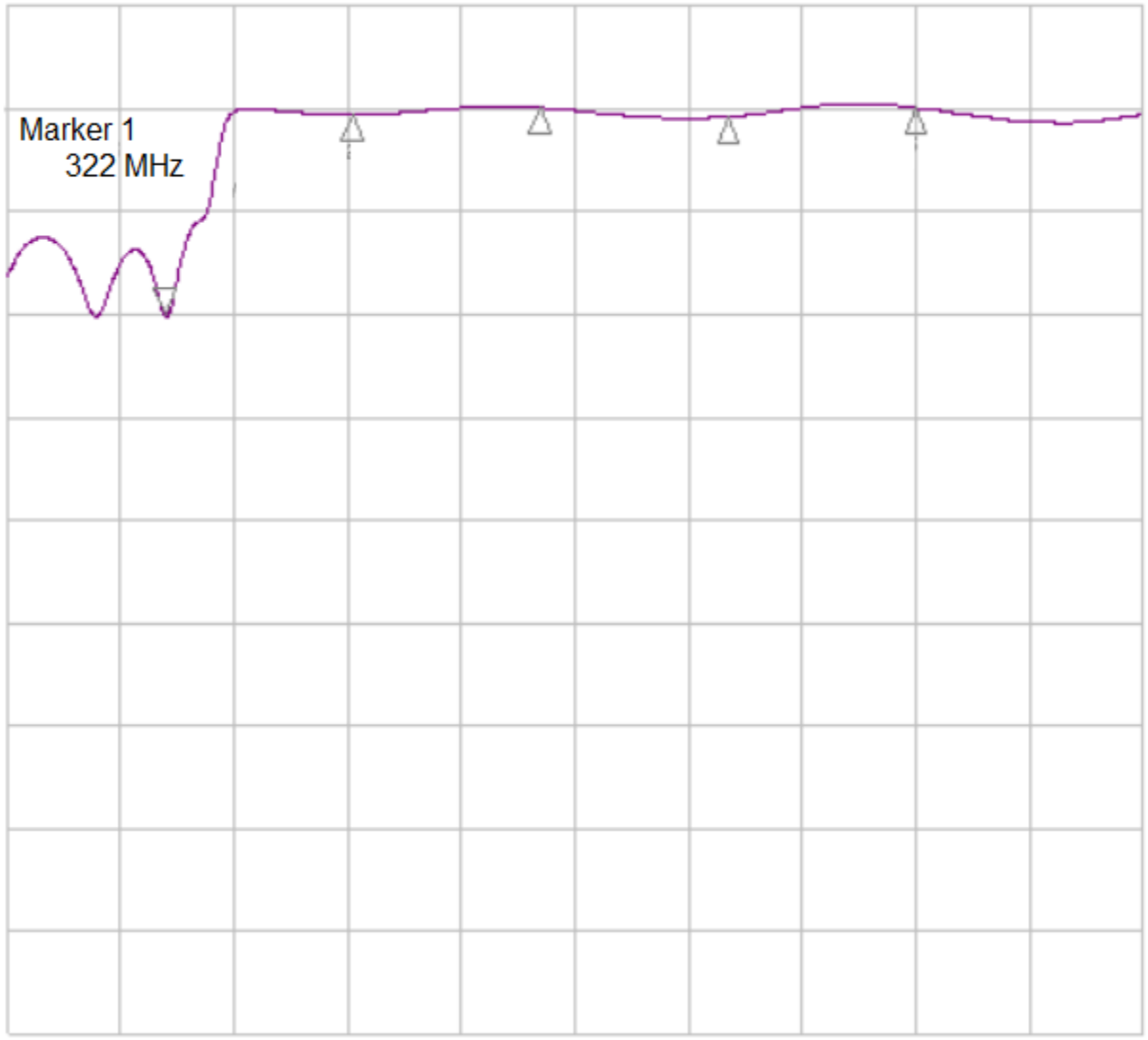

Figure 3.3: Return loss of a high power low pass filter. S11 = -20 dB at 322 MHz, and S11 = -0.5 dB at 644 MHz.

Figure 3.4 shows the harmonic content of a typical 1 kW amplifier running in class C operation. This is a 322 MHz amplifier, and the 2nd harmonic of 644 MHz and 3rd harmonic of 966 MHz are shown. Notice that the 3rd harmonic is actually greater than the 2nd harmonic in this example. This is due to the push-pull operation of the power-amp pallet amplifier [11]. This cancels out the even harmonics, leaving the odd harmonics at a more prominent level, creating a sine wave with a flattened top and bottom. Considering the requirement of -70 dBc distortion levels, the filter performance at the 3rd harmonic is actually more crucial than at the 2nd harmonic. S11 = -50 dB at 966 MHz in the previous example, so at the peak of the third harmonic at about 60 dBm of output power, the filter will reduce the third harmonic from 35 dBm to -15 dBm, which is -75 dBc, and within the desired specification.

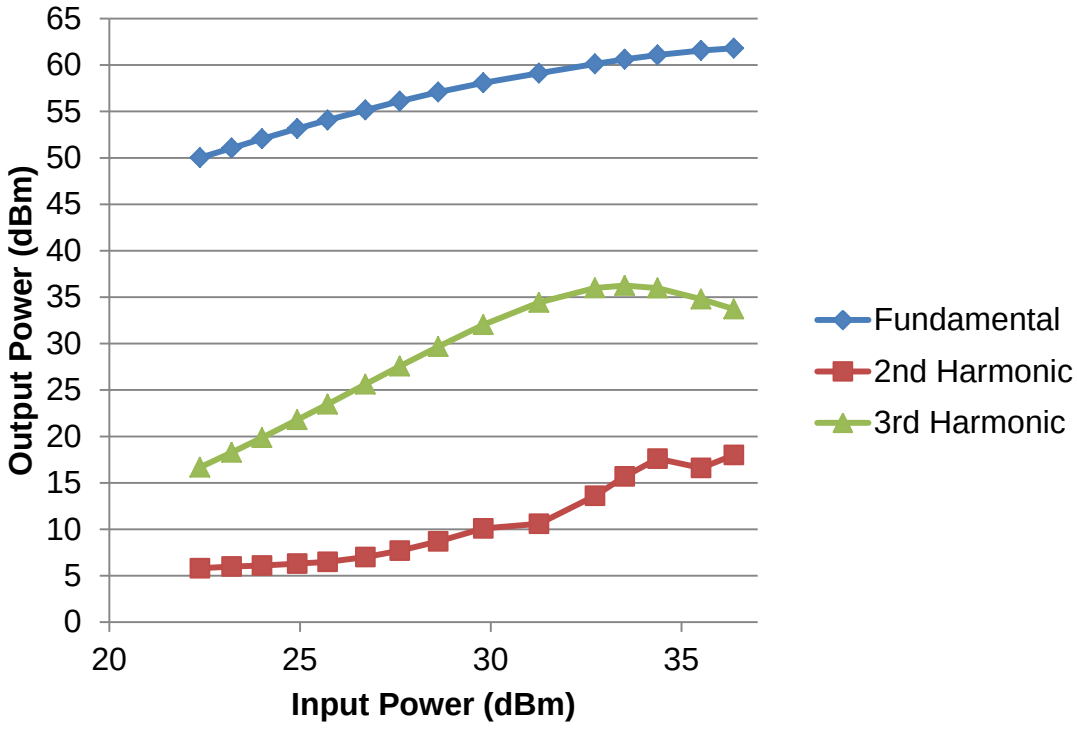

Figure 3.4: Harmonic content of a typical 1 kW Class C power amplifier.

CHAPTER 4

CIRCULATORS

A circulator is a three port device that is designed to allow power to flow from port 1 to port 2 and port 2 to port 3, but prevent it from flowing from port 2 to port 1, or port 3 to port 2 [18]. The applications for a device with these performance characteristics is either a transmit and receive system in which the transmitted power is sent to an antenna and the received power from the same antenna is sent to another amplifier, or an amplifier protection system in which reflected power is directed away from the amplifier and towards a dummy load. A circulator with a dummy load built in to the third port is called an isolator, but a circulator can perform the same function with greater flexibility in the power handling capability of the dummy load attached to port 3. An example of an 80.5 MHz circulator designed to operate at 2 kW is shown in figure 4.1 [19]. The dummy load is a custom built water cooled load resistor capable of 3 kW.

Figure 4.1: 2 kW 80.5 MHz circulator. Input (left), output (right), isolation (top) [19].

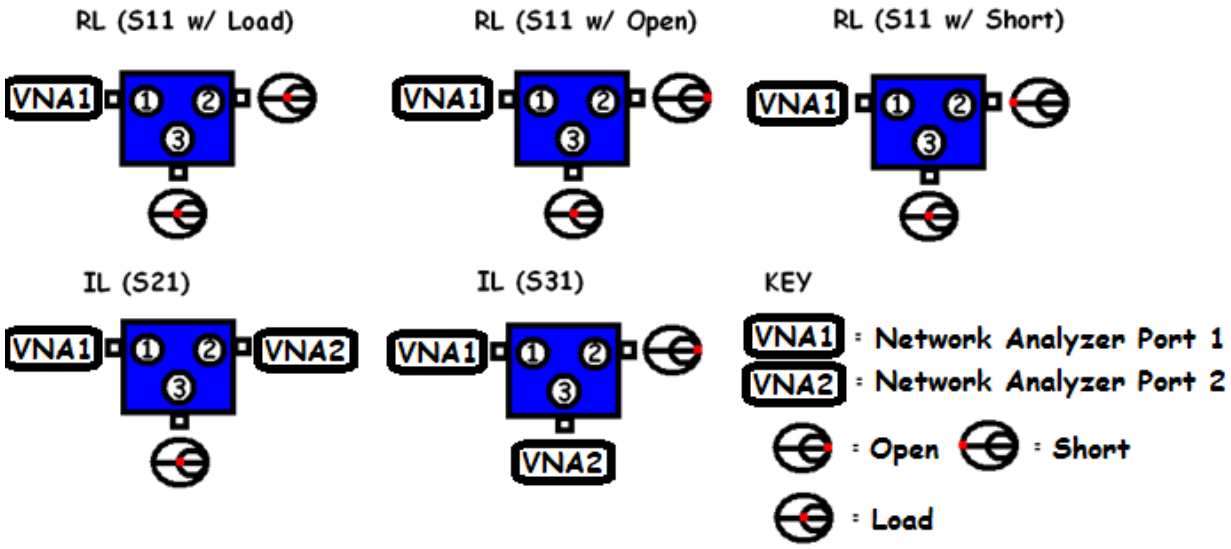

Figure 4.2: Characterizing circulator performance with a network analyzer.

Testing of a circulator requires measurement of the insertion loss with a load on the output, and measurement of the return loss from the output port to the input port with varying load conditions. Three standards that can be used are the open circuit, short circuit, and 50 ohm load. There are also an infinite number of full reflection load conditions surrounding the perimeter of the smith chart that have been found to create small changes in the insertion loss of the circulator, but the three standard loads give a good idea of the performance of the circulator.

Figure 4.2 shows the measurement setup for a circulator at low power levels using a network analyzer. Since the only input in this case is the network analyzer itself and the circulator is a passive device, network analyzer calibration standards can be used. Measuring circulators at high power levels requires the use of a directional coupler, and specially made open and short conditions. Short circuiting or open circuiting a 2 kW amplifier is not a common practice, and as such, specialized high

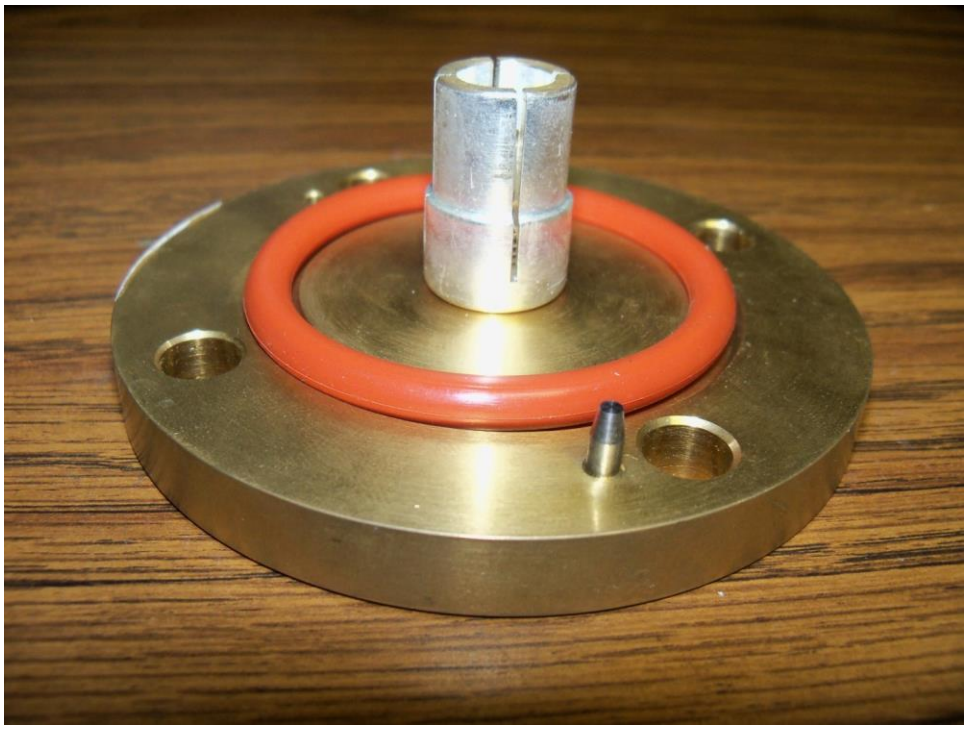

Figure 4.3: Custom made 1 5/8” EIA short circuit used for testing circulators.

Figure 4.4: 1 5/8” EIA open circuit used for testing circulators.

power short circuit and open circuit terminations had to be manufactured. These are shown in figures 4.3 and 4.4, and were constructed at the machine shop on site at NSCL.

4.1 Measured Performance

A three terminal device such as a circulator has 9 s-parameters total, but several of these are redundant due to symmetry, and only a few are necessary to judge the performance characteristics of a circulator. The first is insertion loss (S21) with a load on the output port, and is shown in figure 4.5. In this case the desired result is to have the input power pass though the circulator unaffected. The measured insertion loss of 0.7 dB at the center frequency of 80.5 MHz confirms this aspect of the circulators performance. Also of note is the bandwidth of the acceptable insertion loss. In this example it is about 30 MHz. This will become a very important consideration later on.

Figure 4.6 shows the case of return loss (S11) at the input with a matched load on the output. This is observed to be -23 dB at 80.5 MHz, which means that the reflected signal is 200 times smaller than the incident signal. This is acceptable, but a standard RF cable could provide return loss of greater than 60 dB in the same setup. The real reason for using a circulator is when the output load is not a matched load.

The case of return loss (S11) with an open circuit on the output is shown in figure 4.7. The return loss is 35 dB at 80.5 MHz, which means that the reflected signal is over 2000 times smaller than the incident signal. This means that the reflected power is being directed towards the dummy load instead of the amplifier, which is the desired result. Also notice a bandwidth of 30 MHz in which return loss is better than 20 dB.

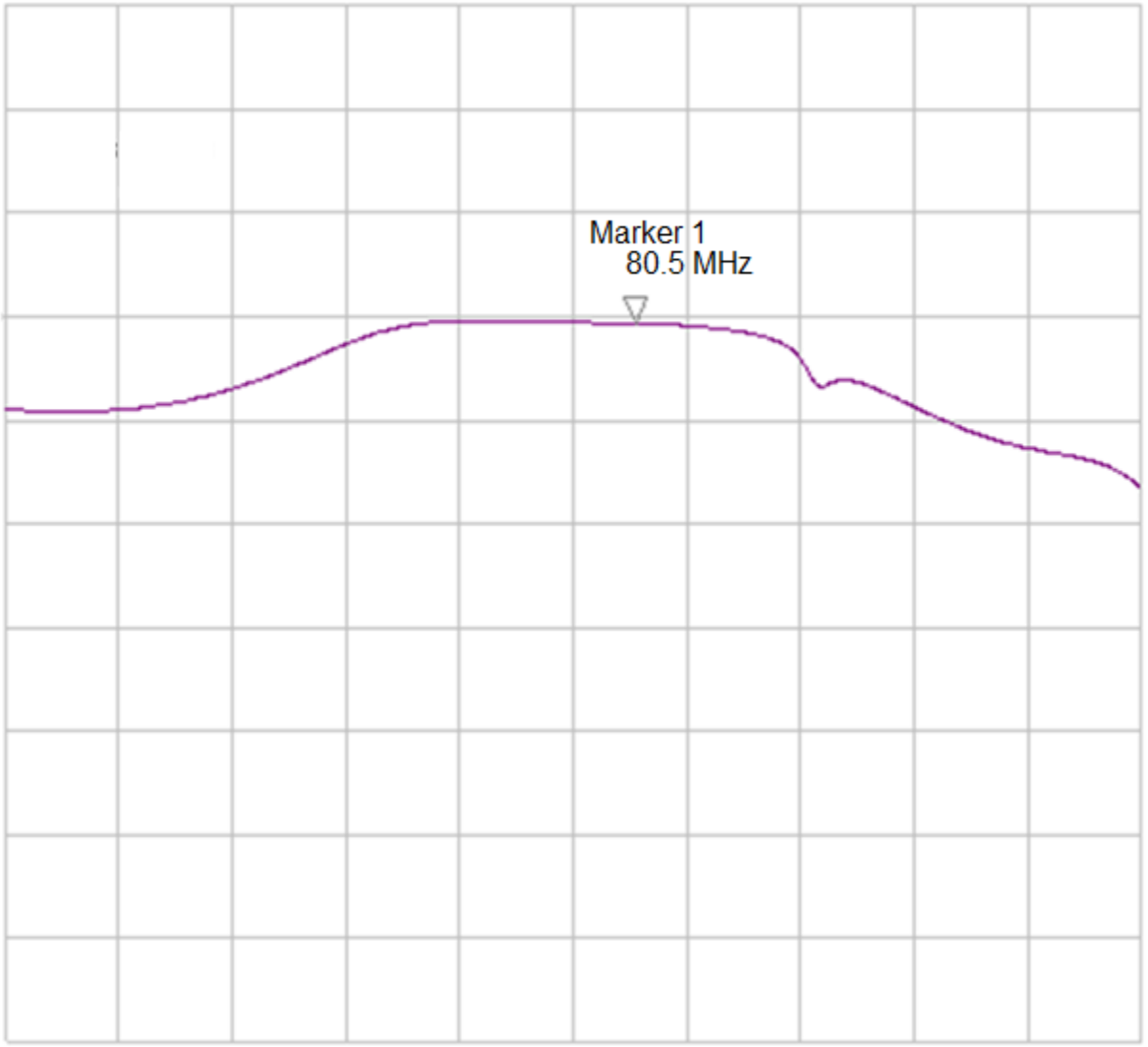

Figure 4.5: Circulator insertion loss with a matched load on the output. S21 = -0.7 dB at 80.5 MHz.

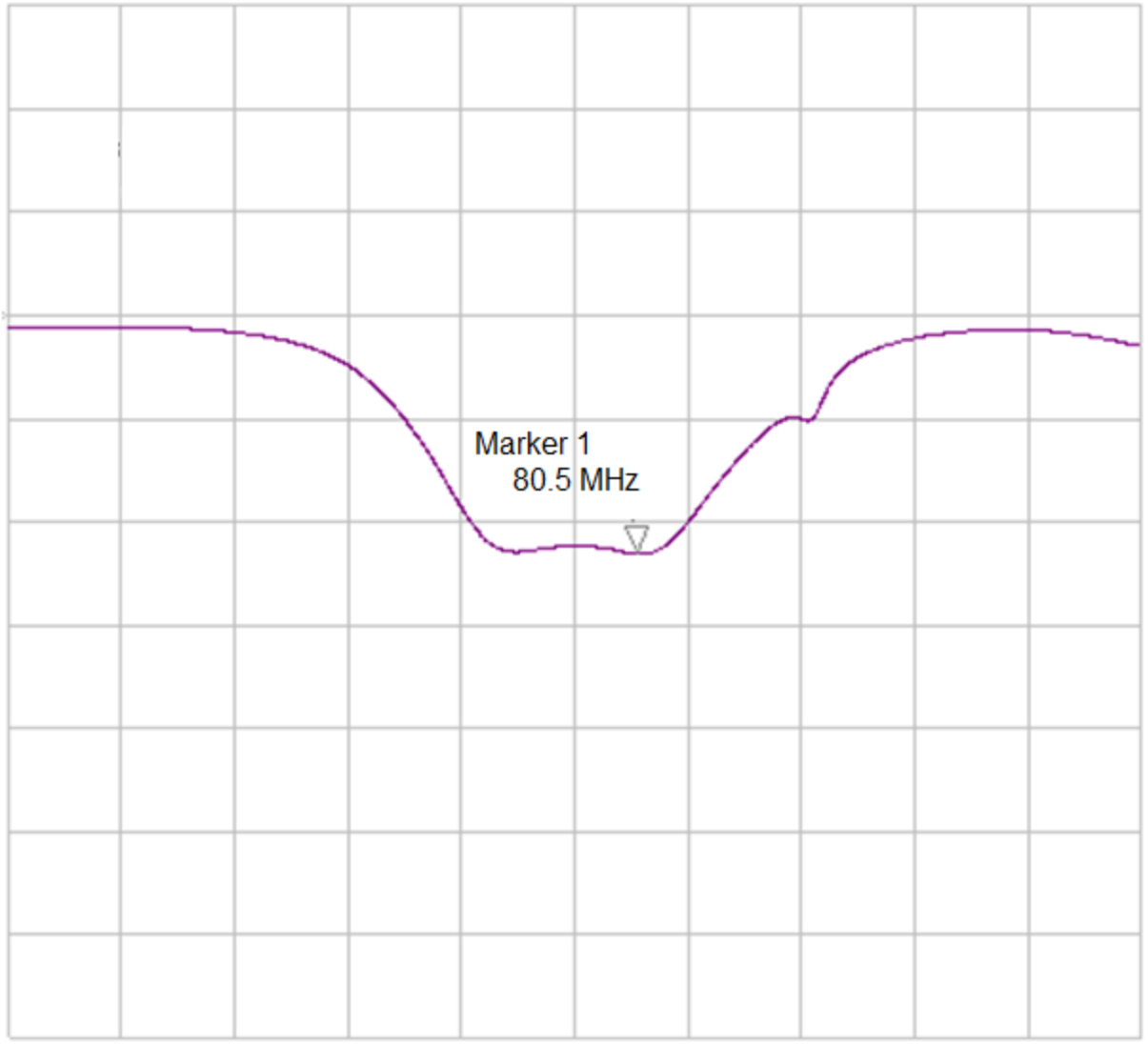

Figure 4.6: Circulator return loss with a matched load on the output. S11 = -23 dB at 80.5 MHz.

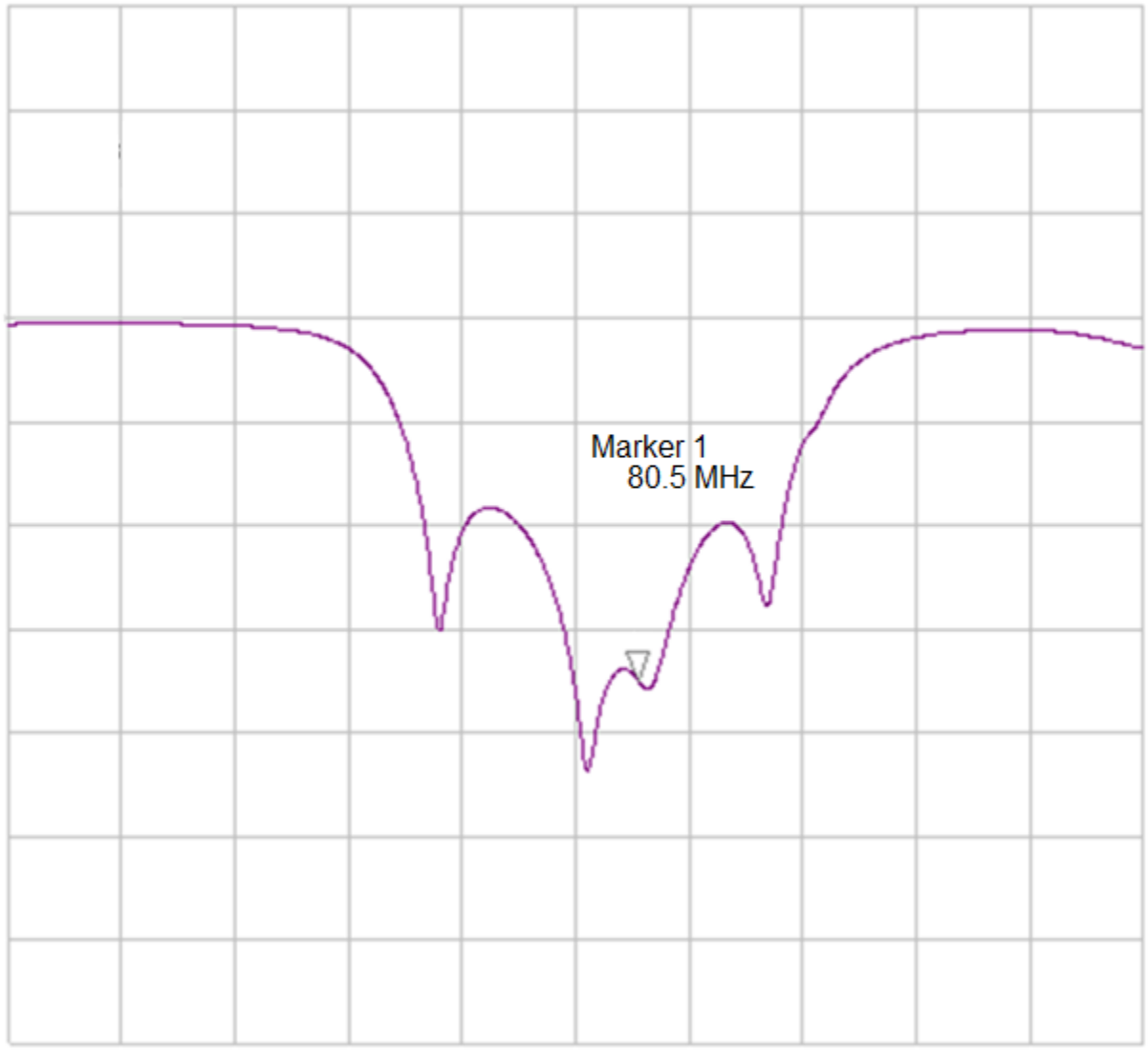

Figure 4.7: Circulator return loss with an open circuit load on the output. S11 = -35 dB at 80.5 MHz.

Low power measurements are relatively simple to take; cooling water is attached to get the circulator up to normal operating temperature, the readings are given time to settle, and measurements are taken for all the different load conditions. The challenge comes when taking high power measurements. The cooling water can still be turned on well in advance to stabilize the temperature of the circulator, but applying power to the device will heat up the ferrite material and alter its response. This means that rather than staying constant right in the sweet spot of the return loss plot, this value will shift. A value that was within specification could be pushed out of range as the power output is increased, but also a value that is out or range at low power could slowly drift into specification as power is applied and the device is heated. This is a potential problem when pulsing the output power. An amplifier and circulator that were designed to operate at high power could be out of range at low power. Pulsing the output of an amplifier to full power could destroy it in this case, since the ferrite material has a lag time when heating up. This temperature dependence will be discussed further in the next section.

Figure 4.8 shows the measured performance from zero power to full power with open, short, and load terminations. It can be seen that the short circuit return loss is very close to 10 dB at low power, while the open circuit return loss is nearing 10 dB at 2.2 kW output power as well. This is a very risky situation to operate an amplifier in, as any slight change in the cooling water temperature could push the circulator out of specification at either end causing thermal runaway, destroying both the circulator and the amplifier.

Figure 4.9 shows another high power test of an 80.5 MHz circulator that did not

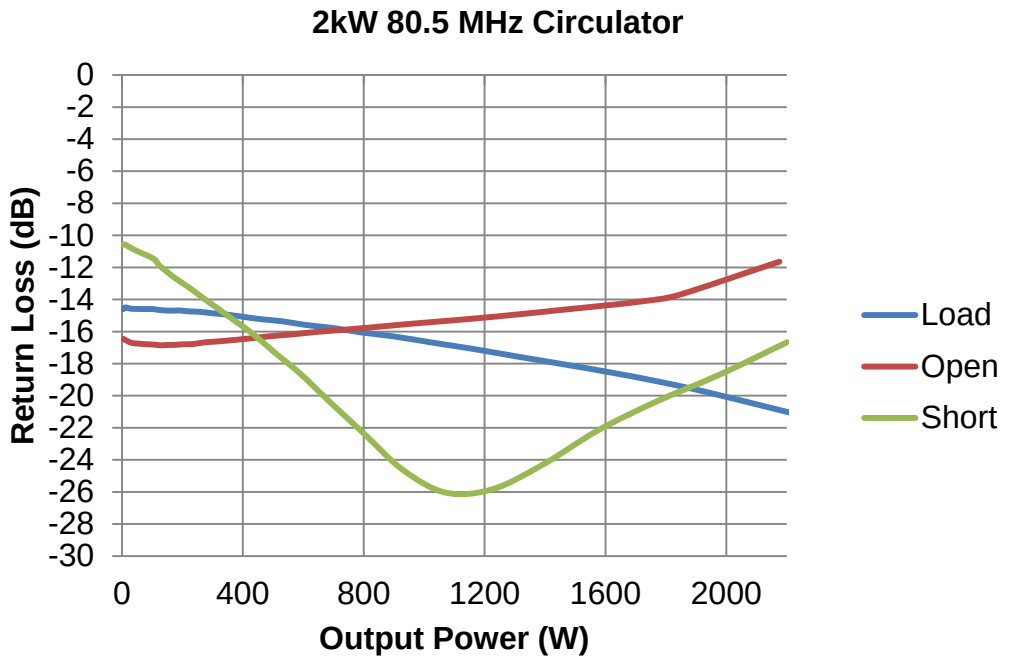

Figure 4.8: Return loss vs. output power for an in spec 80.5 MHz circulator.

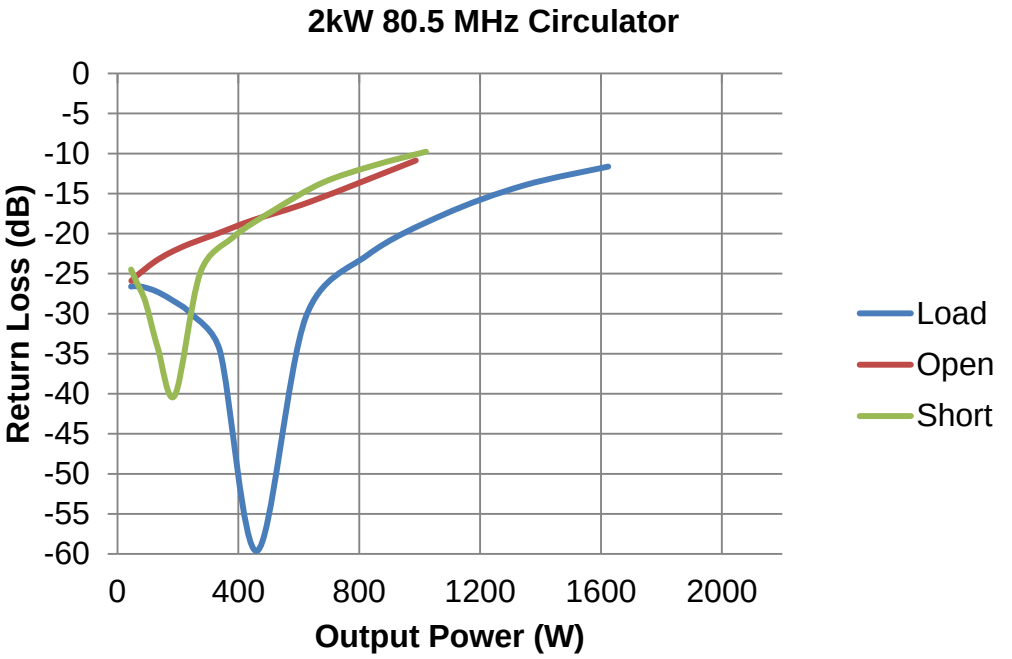

Figure 4.9: Return loss vs. output power for an out of spec 80.5 MHz circulator.

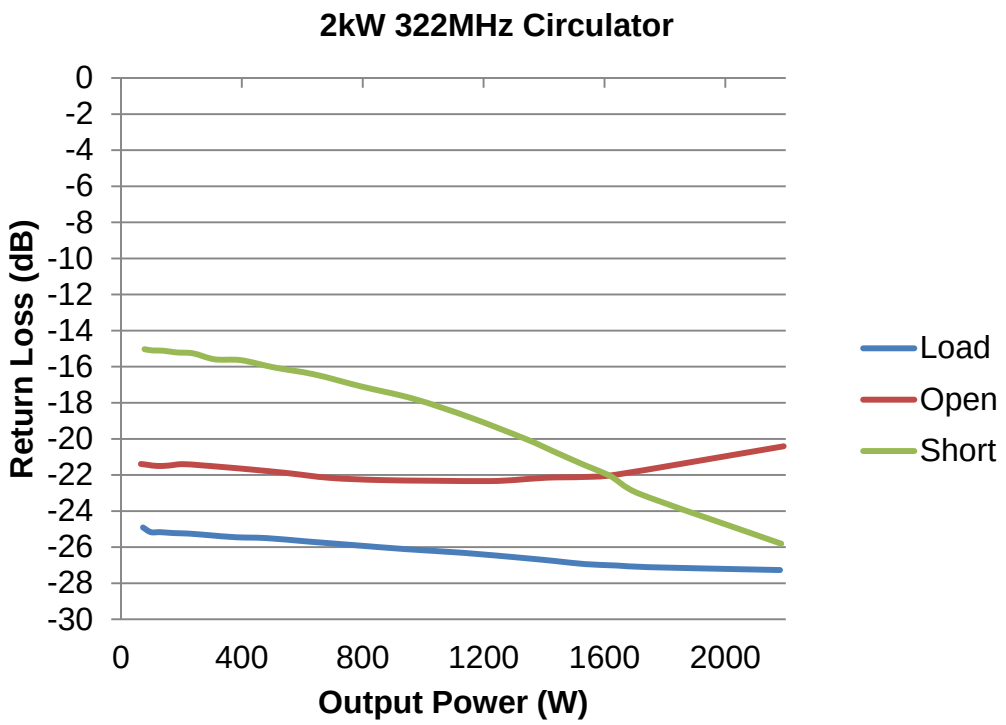

Figure 4.10: Return loss vs. output power for an in spec 322 MHz circulator.

meet the required specifications. An output power of only 1.6 kW was reached by the time the return loss had drifted to 10 dB. With open and short circuit terminations, a return loss of 10 dB was reached at 1 kW of output power. Increasing the power any further in each of these cases would cause thermal runaway and destroy the amplifier.

Figure 4.10 shows the high power testing results of a 322 MHz circulator. As can be seen from the data, the changes in return loss are gradual, and there is no danger of thermal runaway occurring. These higher frequency circulators are easier to design due to the larger bandwidths obtainable. Both 80.5 MHz and 322 MHz circulators are provided with tuning screws that can be used to adjust the performance. With an 80.5 MHz device this is crucial, but most 322 MHz circulators can be designed without the need for onsite adjustment, which would be time consuming with 344 amplifiers.

4.2 Temperature Dependence

The effect of temperature on circulator performance is significant at lower frequencies, and must be both understood and compensated for in order to prevent damage to amplifiers. In the absence of a time-lapse video, figure 4.11 shows an overview of what happens to the return loss response characteristics when the temperature of a circulator is either raised or lowered. The black line in the center of the plot marks the center frequency of 80.5 MHz. The return loss with all three loads is within specification at this point. When the device is heated, all three return loss response curves will maintain their general shape, but shift to the right of the centerline.

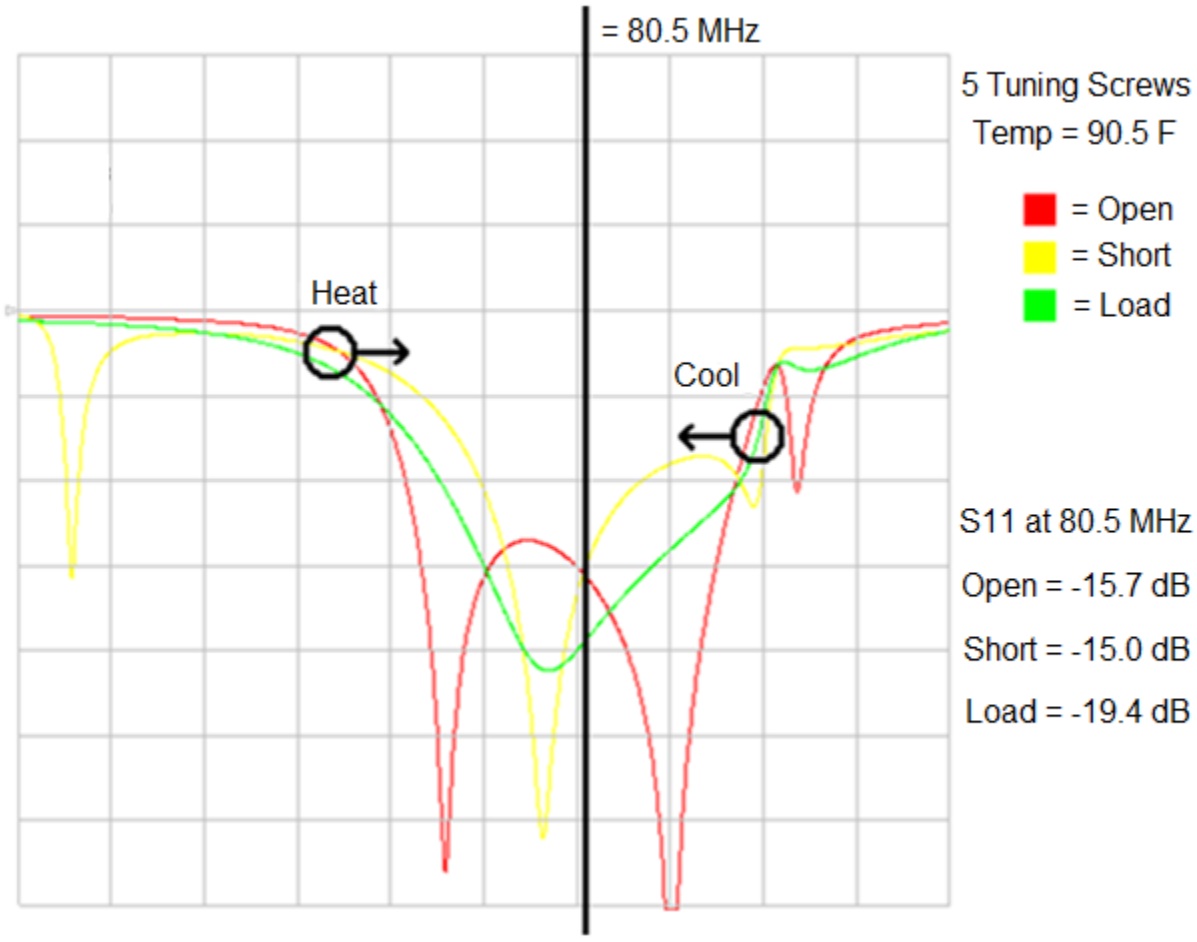

Figure 4.11: Temperature dependence of a circulator with an open, short, and load.

Likewise, when the device is cooled, all three return loss response curves are shifted to the left. With a limited amount of bandwidth available, the best design practice is to tune the circulator such that the black line is at the far left edge of all three response curves at the lowest temperature that the device would ever see. Return loss should be better than 10 dB for all three terminations. This will result in the maximum amount of bandwidth available as the device is heated due to the applied power. If a circulator is still not able to meet the full power requirements with this procedure, then no amount of tuning will get it to work. The response could be tuned for good performance at high power, but turning the device on quickly from a low power state would present a high reflection case to the amplifier for a short amount of time, which is enough to destroy it.

Another factor to consider is the magnetic properties of circulators. A basic circulator is constructed with a circular microstrip with three ports connected to it, and a large ferrite material placed on top of this microstrip to control the direction of power flow [18]. Exposing this ferrite material to other metallic materials can alter the response enough to push it out of specification. Figure 4.12 shows the effect of placing a circulator on a metal shelf as opposed to a plastic shelf. This has the effect of re-tuning the circulator from a center frequency of 80.5 MHz to a center frequency of 110 MHz. This is similar to the effect that tuning screws have on the response of a circulator, but is much more drastic. For this reason, all case material in a completed amplifier system containing a circulator needs to be constructed from a non-ferrous material such as aluminum, and the case must be kept away from other metallic materials.

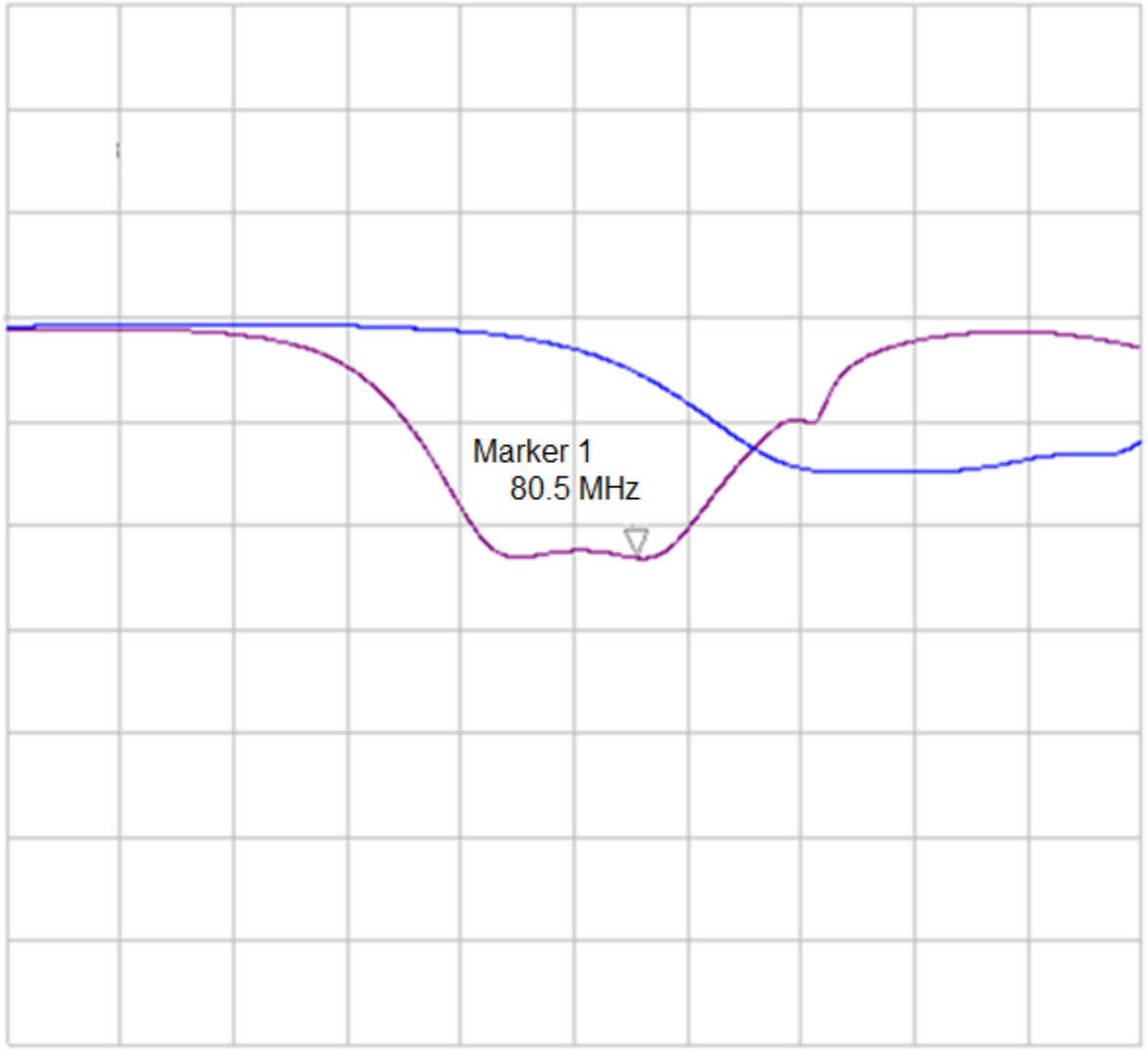

Figure 4.12: Shift in return loss: circulator on metal stand (blue) vs. circulator on plastic stand (purple).

CHAPTER 5

POWER COMBINERS

A power combiner is a passive circuit that is used to combine two or more inputs that are well matched in both frequency and phase, and relatively well matched in amplitude as well. Figure 5.1 shows examples of power combiners that are useful in the 2 kW – 8 kW power range. The line sections that look like copper pipe are high power rigid transmission lines, and are required for power levels above 2 kW. Variations in input power levels of +/- 0.5 dB do not cause much trouble,

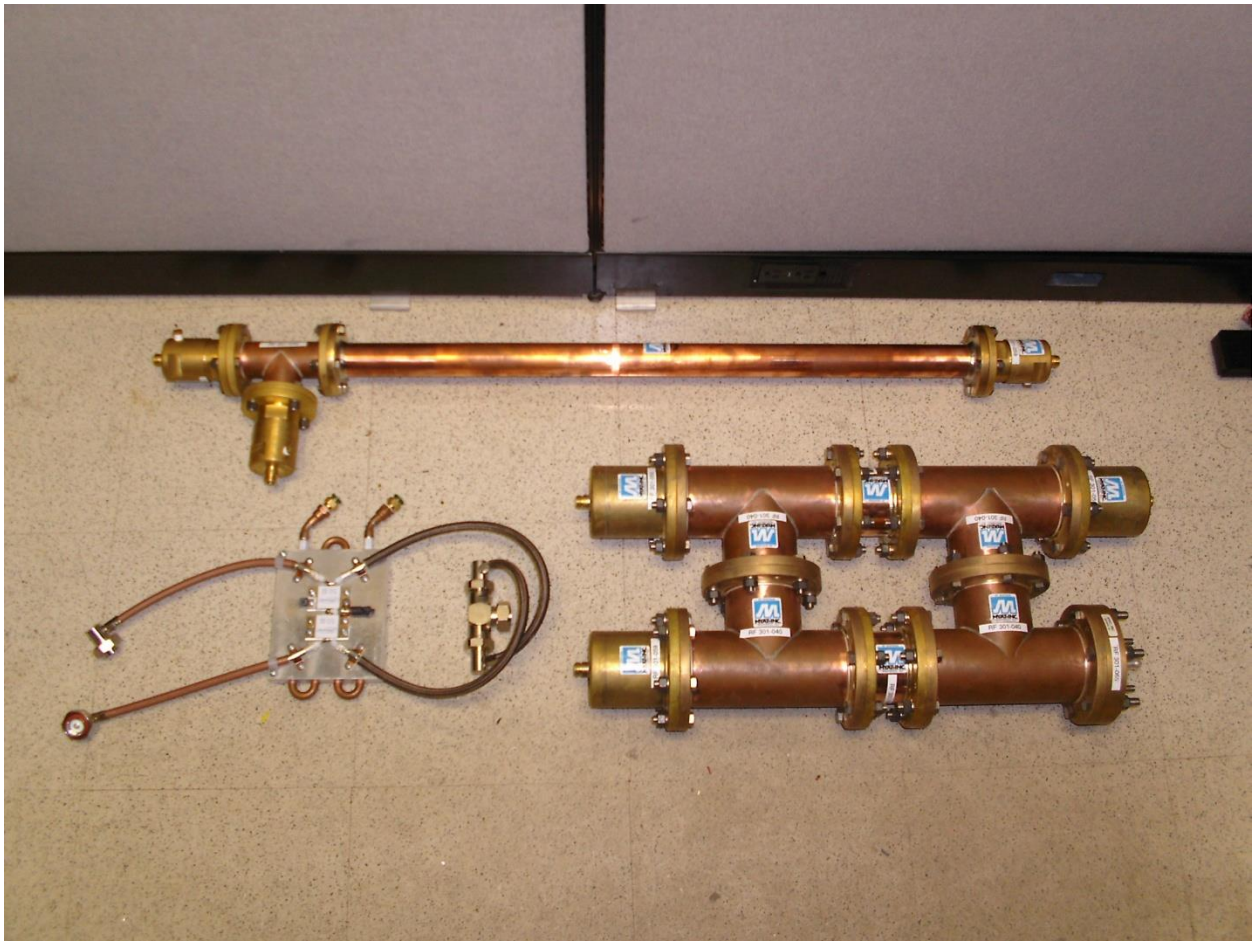

Figure 5.1: 4 kW TEE (top), 2 kW Wilkinson (bottom left), 8 kW hybrid (bottom right).

but slight variations in phase can cause problems for power combiners. As an extreme example, attempting to combine two sine waves that are 90 degrees apart without using a phase shifter will result in zero net power gain. This means that 1 kW + 1 kW = 1 kW, which is not a very worthwhile use of a power combiner designed to increase power levels. If these two sine waves were 180 degrees apart, the resulting power output would be zero. Figure 5.2 shows simulated and measured results for a TEE combiner circuit. The simulations were done using Ansoft Designer [20], and the measurements were carried out using a network analyzer to measure phase mismatch. As can be seen from the graph, the simulated results are much more optimistic than the measured results. Even a 20 degree phase mismatch, which is a fraction of a nanosecond at 322 MHz, is enough to cause an additional 0.5 dB of power loss.

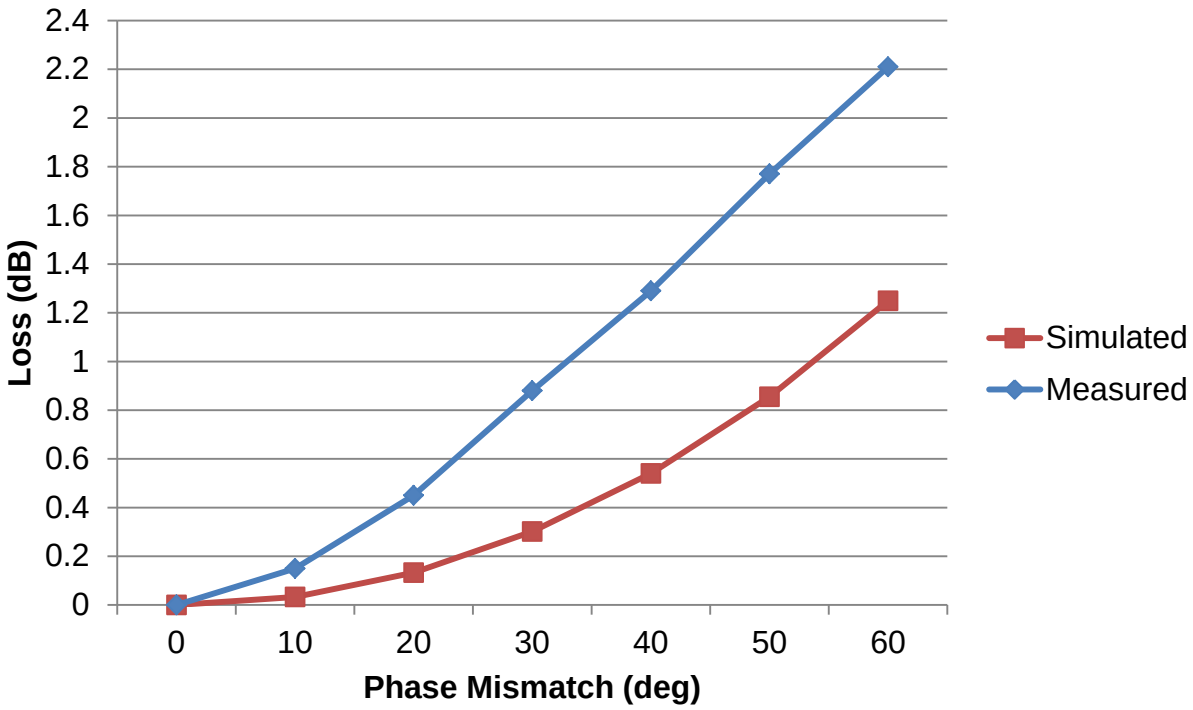

Figure 5.2: Loss vs. phase mismatch in a TEE combiner.

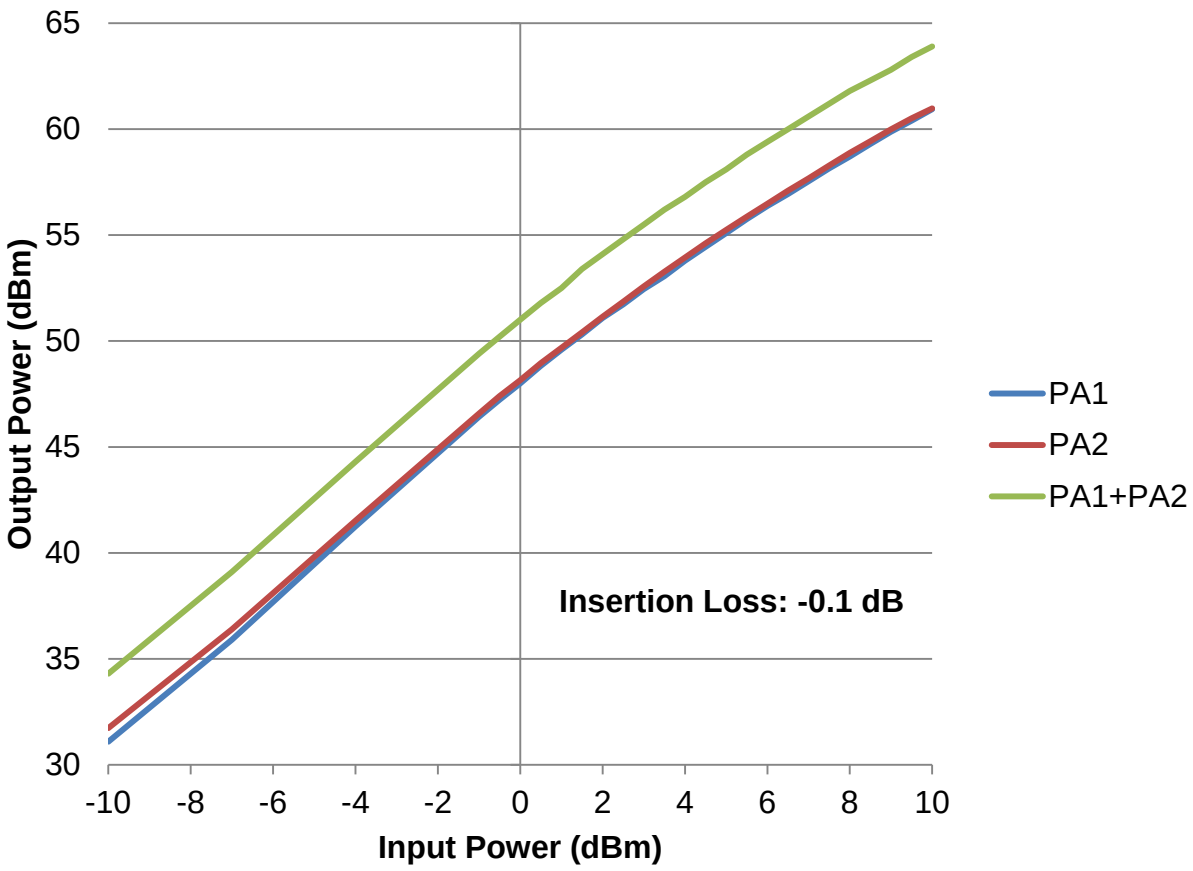

Figure 5.3: Results of a 2 kW Wilkinson combiner test.

The results of a high power combiner test are shown in figure 5.3. These measurements were taken using a directional coupler on both inputs and the output to measure power levels, but also to fine tune the phase of each input. With currently available equipment, the best phase match that can be achieved is +/- 1 degree at 322 MHz. With these conditions, the insertion loss at full power is measured to be 0.1 dB.

High power tests are good for measuring the absolute performance characteristics of a power combiner, but more sensitive measurements at low powers using a network analyzer are required to compare the performance characteristics of different combiner circuits. Figure 5.4 shows a test bench with a 4 kW Hybrid combiner

being measured. The isolation port is terminated with a 50 ohm water cooled dummy load, as it would be in actual operation, and the output is terminated with standard

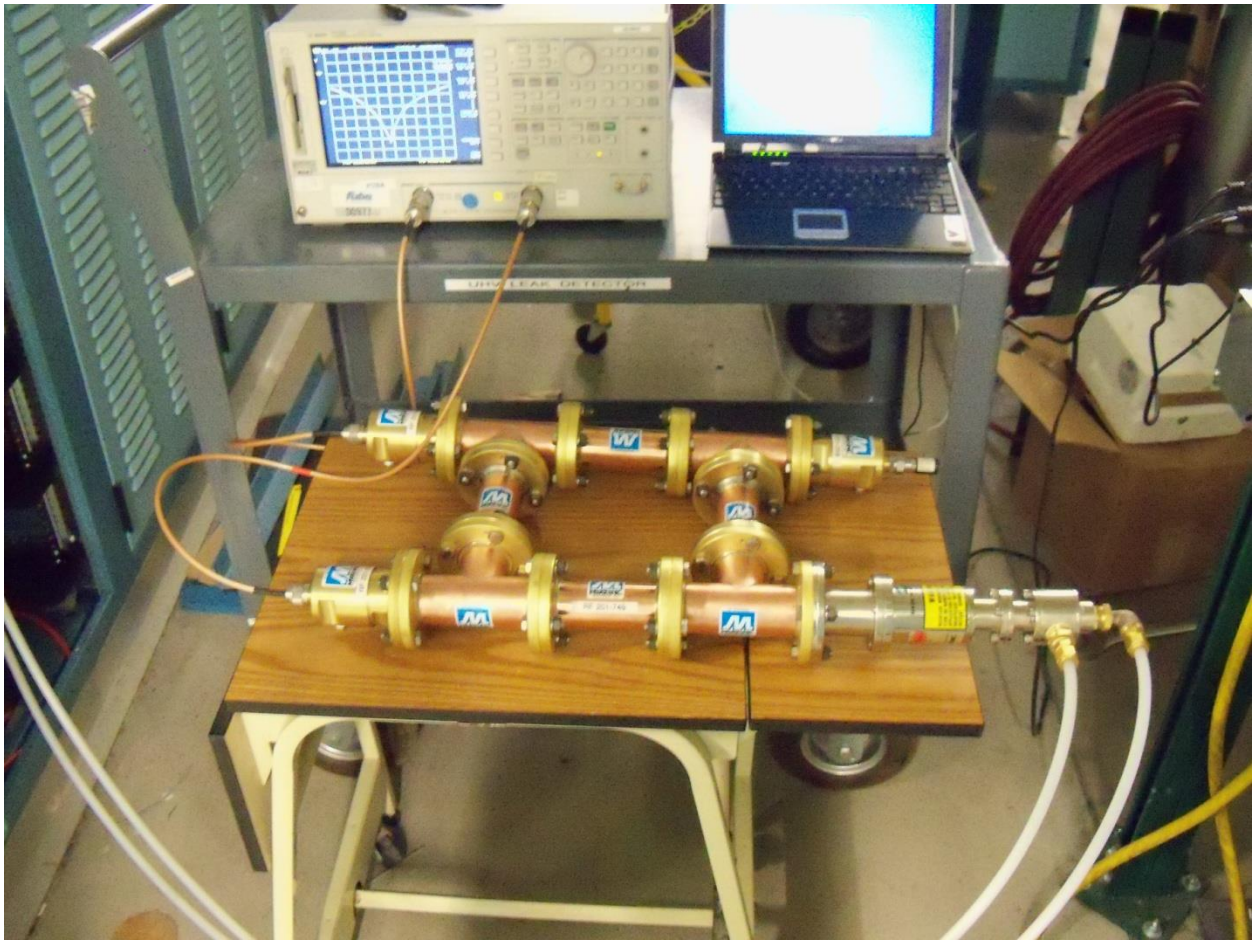

Figure 5.4: Low power test setup for measuring a 4 kW 322 MHz hybrid combiner.

network analyzer calibration loads. A four port device such as a hybrid combiner will have 16 S-parameters, but again only a few are required to judge the performance characteristics of the device. The following section will present three different measurements; return loss at an input port, insertion loss from an input port to the output port, and isolation between the two input ports. All measurements are taken with a matched load on the output; performance changes when either a short or an open is attached to the output. The following combiner circuits will be compared; a 4 kW 322

MHz TEE combiner, a 2 kW 322 MHz Wilkinson combiner, and finally an 8 kW 322 MHz hybrid combiner.

5.1 TEE Combiner

A TEE combiner is the most basic combiner circuit available, and simply consists of a T shaped three terminal connector, followed by a quarter wavelength line section designed to transform the resulting 25 ohm impedance back to 50 ohm. This circuit has the benefit of not requiring any resistor or load elements in the design, but as with most power combiner circuits, has a narrow frequency range. This is because the quarter wavelength transformer is only a quarter wavelength exactly at the design frequency. Above or below the center frequency, the output impedance is transformed to something other than 50 ohms, and the output power is reduced. A TEE combiner has several flaws, including very little isolation between the input ports, and poor return loss at the inputs. Despite these factors, a TEE combiner is a good option when the input signal and load conditions are predictable. Its main strong point is being one of the least expensive options available. Figure 5.5 shows that the return loss of the TEE combiner is about 6 dB at 322 MHz. Figure 5.6 shows the insertion loss from an input to the output with the unused input terminated. This is about 3 dB at 322 MHz. With a more accurate measurement setup, this information can be used to estimate the insertion loss at high power. Finally, figure 5.7 shows the isolation between the input ports. This is only about 6 dB, and can cause issues when both inputs are not perfectly matched.

5.2 Wilkinson Combiner

A Wilkinson combiner is constructed using a 100 ohm power resistor between the two inputs, and two 70.7 ohm 1/4 wavelength sections leading to a standard T shaped three terminal connector [18]. This design provides significantly better return loss performance and isolation between the inputs when compared to a TEE connector. The return loss in an 80.5 MHz Wilkinson combiner is shown in figure 5.8. It is 26 dB at 80.5 MHz, which is 20 dB better than the TEE combiner example. Figure 5.9 shows the insertion loss from input to output of the combiner. This is 3.3 dB at 80.5 MHz with one input terminated, so the insertion loss at high power can be estimated to be about 0.3 dB. Figure 5.10 shows the isolation between the two input ports of the Wilkinson combiner. This is 29 dB at 80.5 MHz, which is also significantly better than the TEE combiner example. The main benefit of a Wilkinson combiner is that if one input fails, part of the reflected power from the other input will be dissipated in the 100 ohm resistor. This reduces the stress on the amplifier due to high reflection.

5.3 Hybrid Combiner

The most complex, but also highest performing combiner circuit is the hybrid combiner. The hybrid combiner is typically implemented using microstrip lines at low power levels and high frequency [18]. The same concepts are applied here, with the exception of changing out microstrip lines for high power rigid transmission lines. The horizontal line sections in figure 5.1 are designed for a characteristic impedance of 35.3 ohms, and the vertical line sections have a characteristic impedance of 50 ohms. Each arm of the combiner is a quarter wavelength in air at 322 MHz. The two ports on the left

are the inputs, the port on the top right is the output, and the port on the bottom right is the isolation port. Figure 5.11 shows the return loss of an 8 kW 322 MHz hybrid combiner is 32 dB. This is better than both the TEE and Wilkinson examples. Figure 5.12 shows the return loss at 322 MHz. Again, this measurement was taken with the other input port terminated, making the true insertion loss at high power difficult to determine. Finally, Figure 5.13 shows the isolation performance of the Hybrid combiner to be 33 dB at 322 MHz. Again, this is better than both the TEE and Wilkinson examples. A high power hybrid combiner would be the ideal circuit for this application if it weren't for the cost and complexity of assembling these types of combiners. There are also issues with fitting a rigid connector such as this in the rack space between two amplifier modules. If size and cost are issues, than the Wilkinson combiner is the best solution.

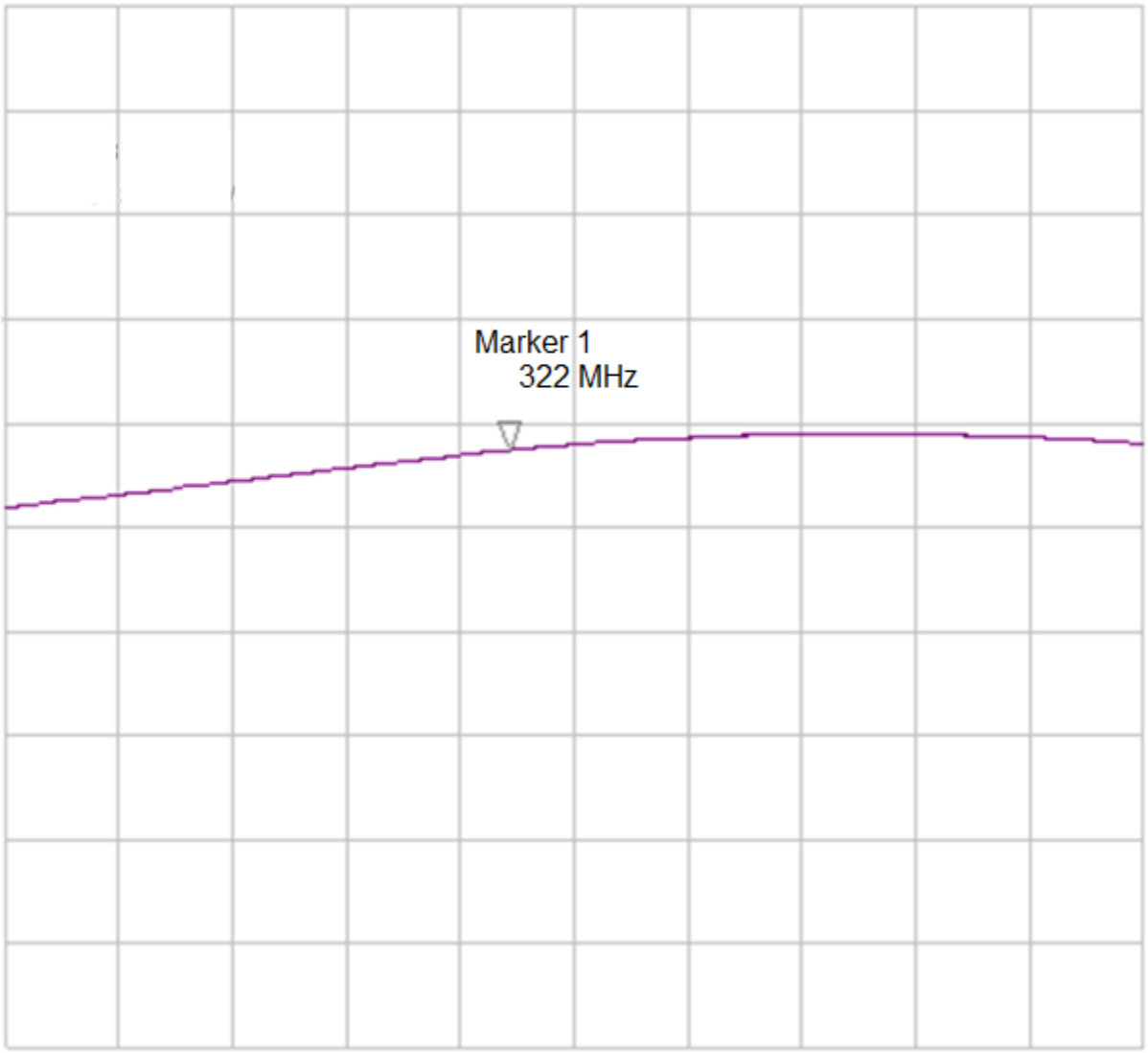

Figure 5.5: TEE combiner return loss. S11 = -6.3 dB at 322 MHz.

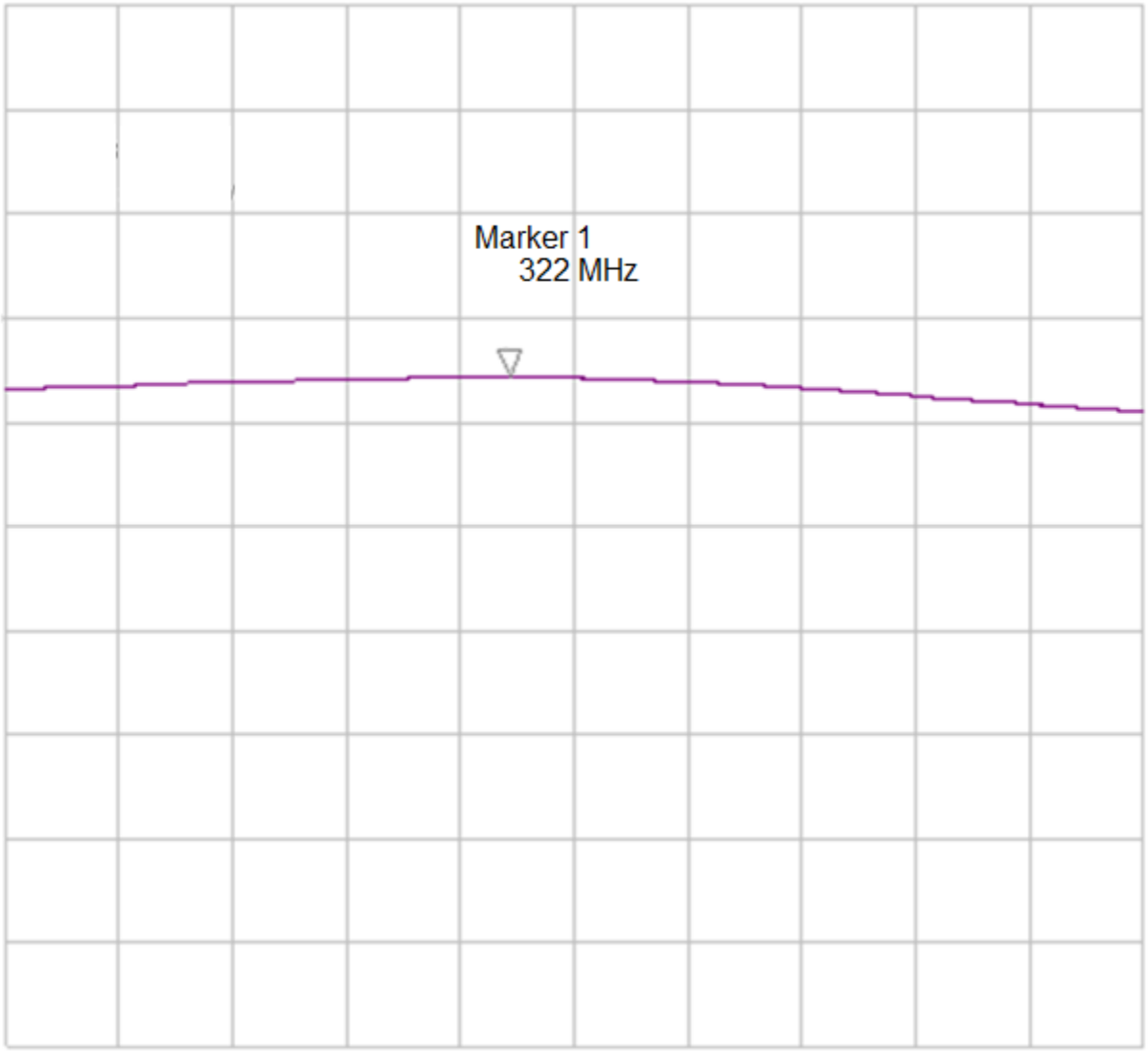

Figure 5.6: TEE combiner insertion loss. S31 = -2.8 dB at 322 MHz.

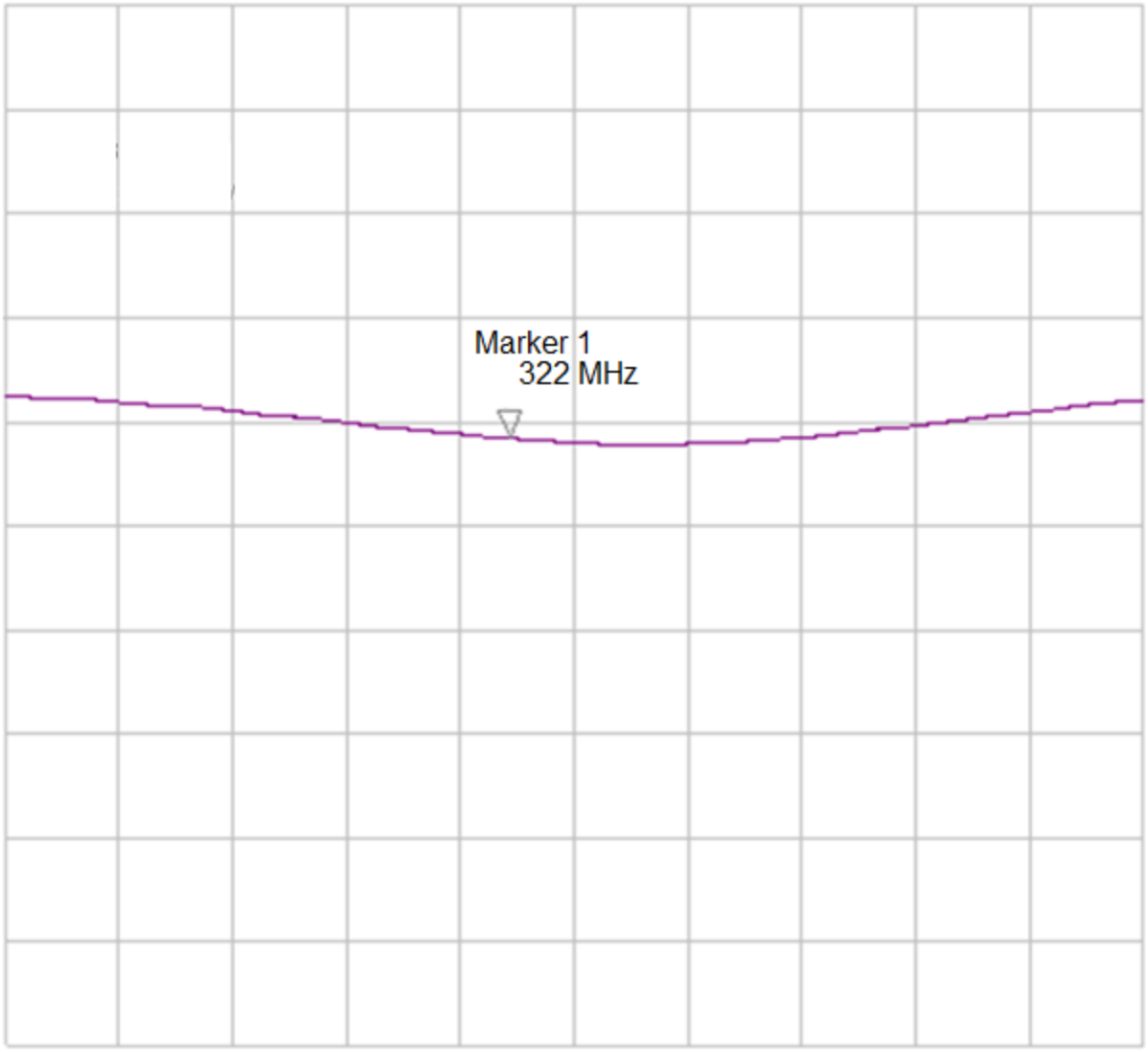

Figure 5.7: TEE combiner isolation. S21 = -5.8 dB at 322 MHz.

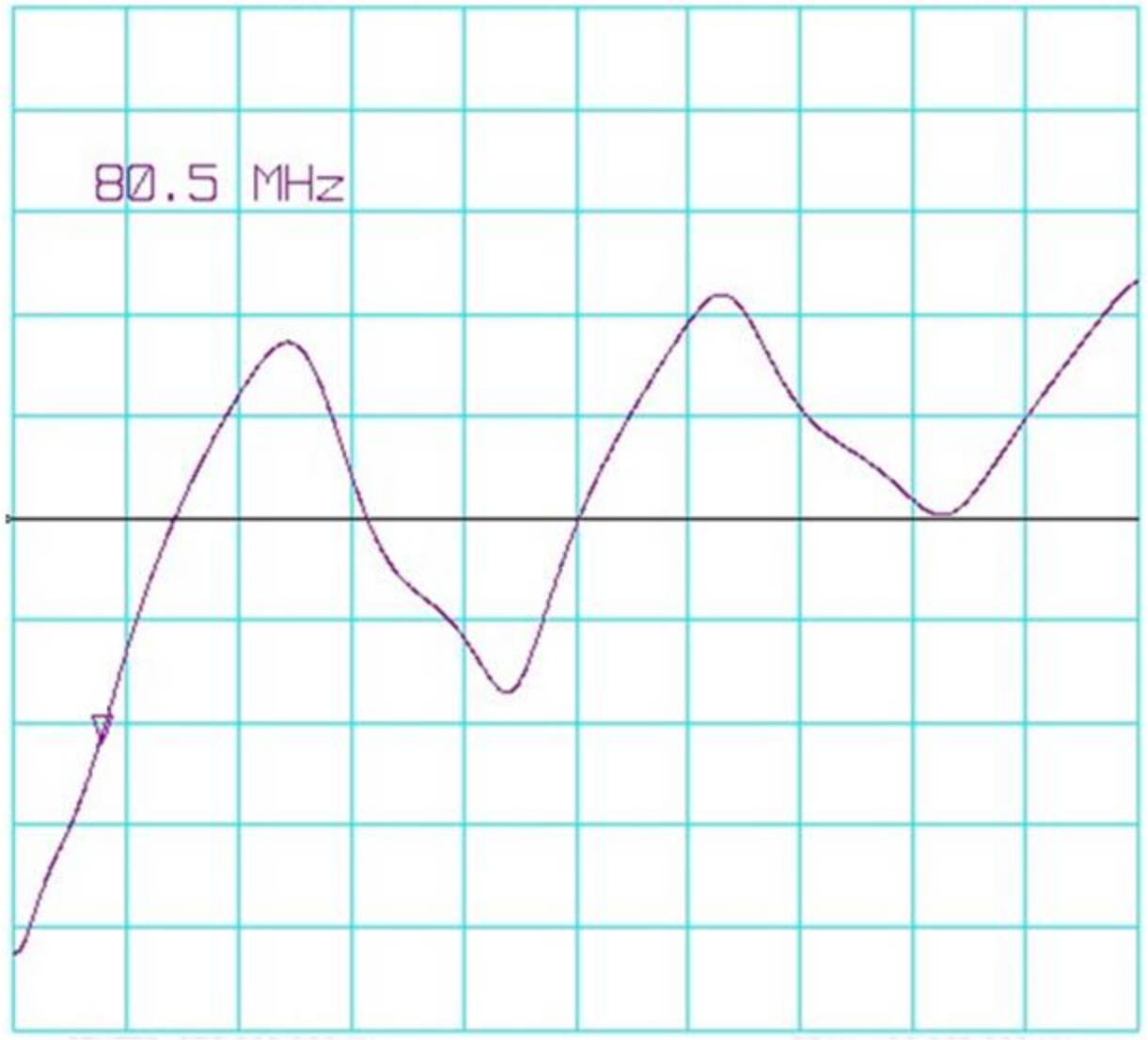

Figure 5.8: Wilkinson combiner return loss. S11 = -26 dB at 80.5 MHz.

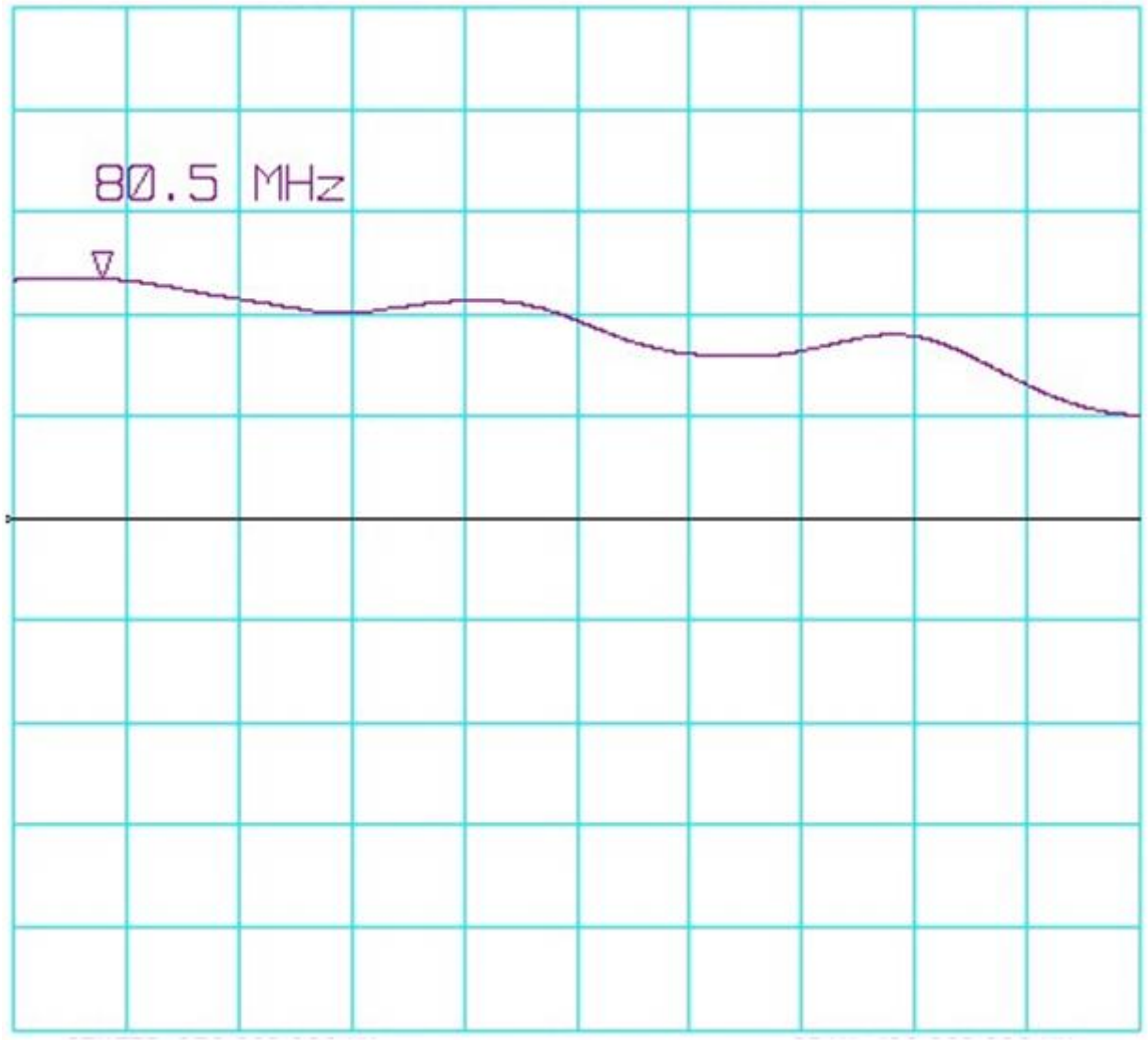

Figure 5.9: Wilkinson combiner insertion loss. S31 = -3.3 dB at 80.5 MHz.

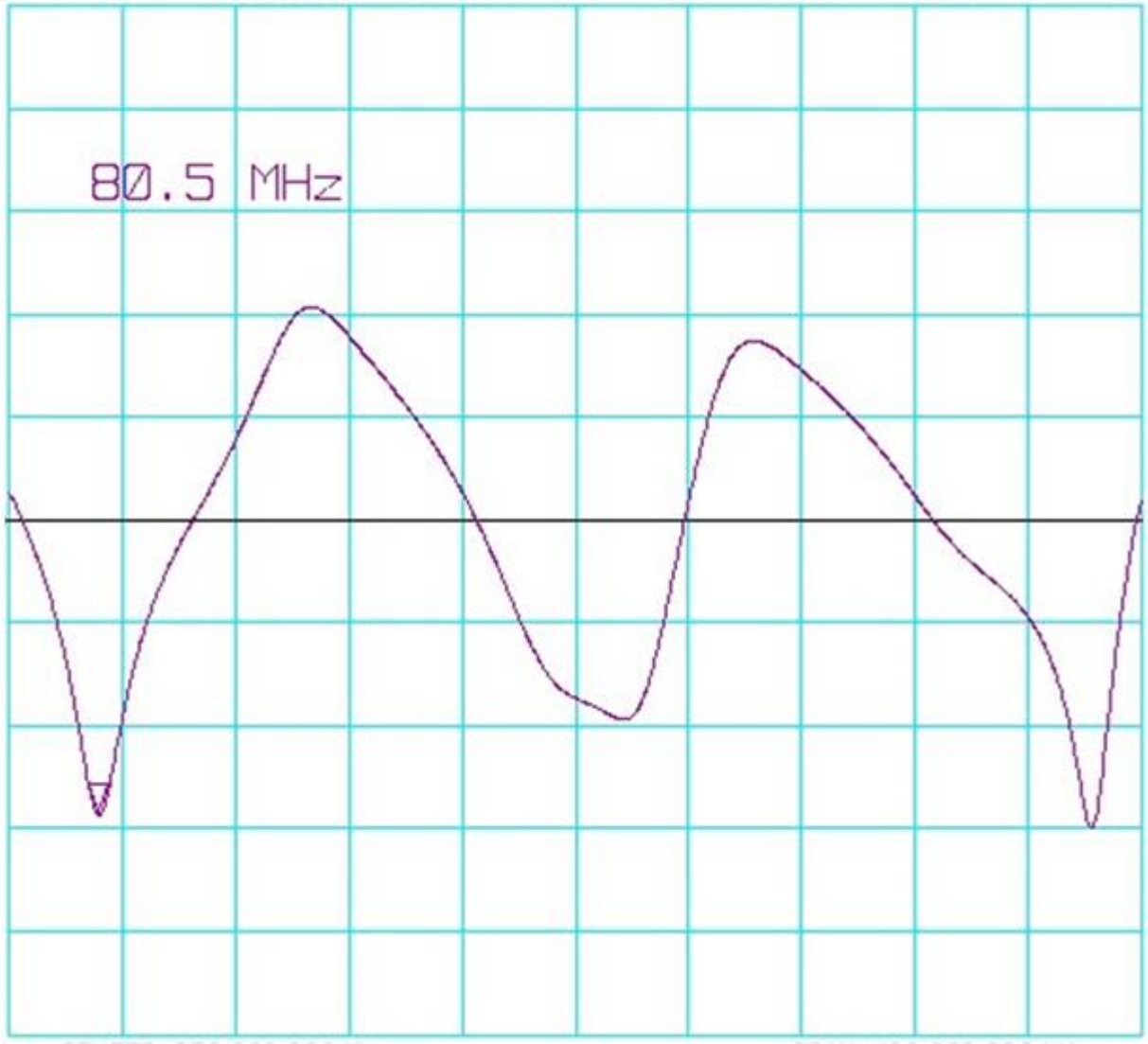

Figure 5.10: Wilkinson combiner isolation. S21 = -29 dB at 80.5 MHz.

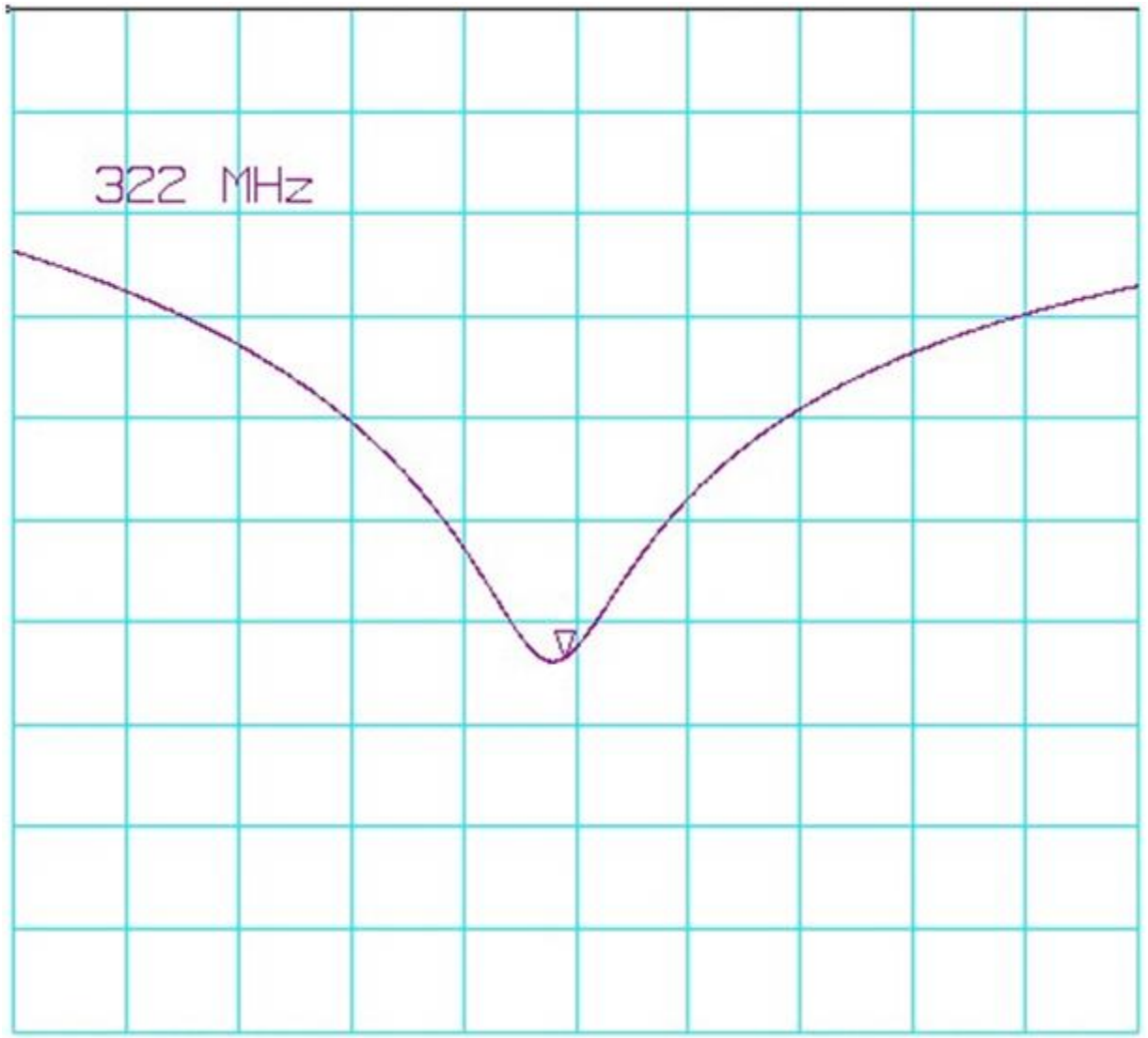

Figure 5.11: Hybrid combiner return loss. S11 -32 dB at 322 MHz

Figure 5.12: Hybrid combiner insertion loss. S31 = -2.8 dB at 322 MHz.

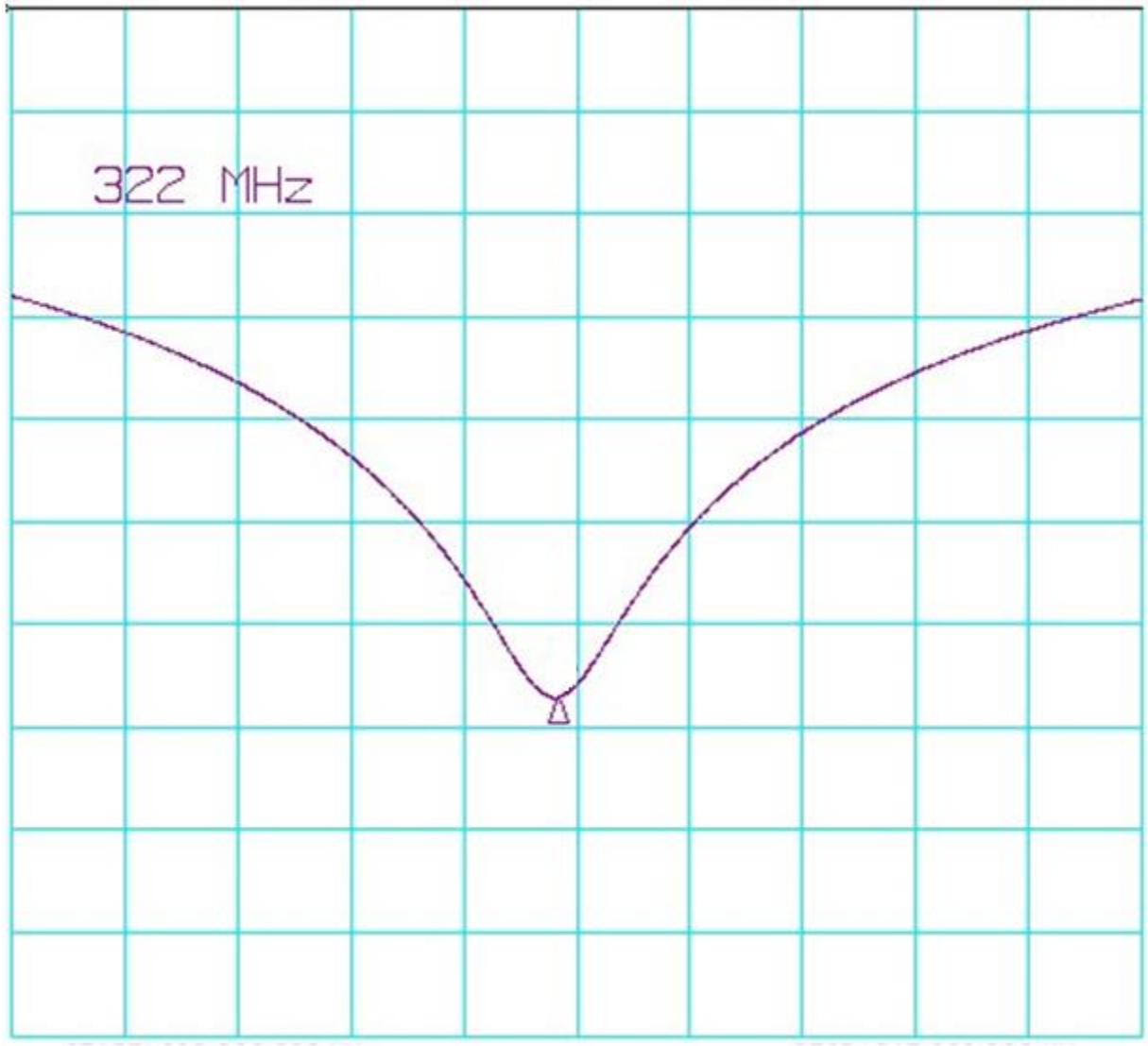

Figure 5.13: Hybrid combiner isolation. S21 = -33 dB at 322 MHz.

CHAPTER 6

SYSTEM TESTING

With all four amplifier components designed and tested independently, a complete amplifier system can be assembled to achieve the power output levels required for FRIB. The first method of testing is the bench test, in which amplifier components are assembled in a temporary location solely for the purpose of testing. An example of a test bench for a 1 kW amplifier system is shown in figure 6.1. The pallet amplifier and biasing power supply are on the top shelf, along with a collection of

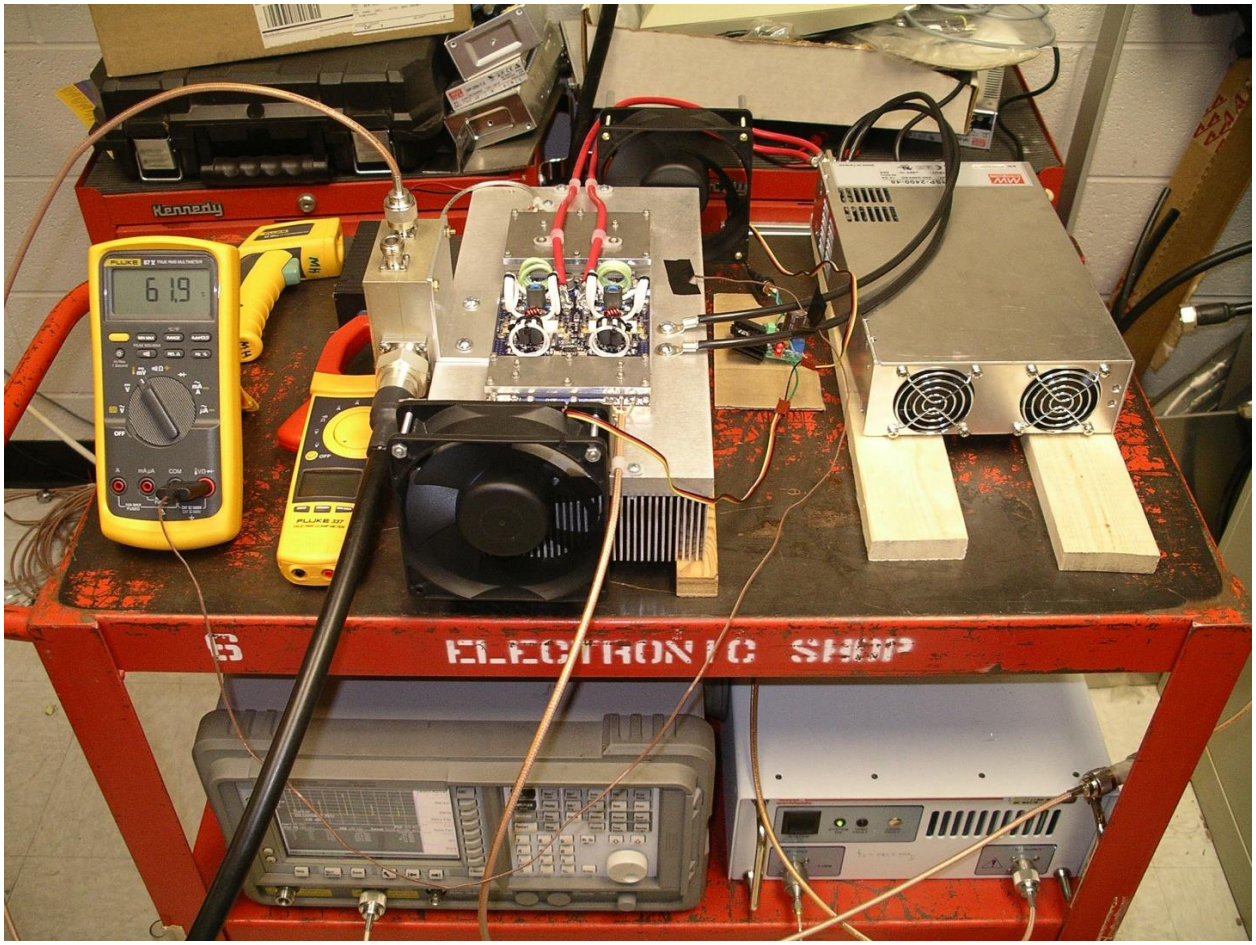

Figure 6.1: Test bench setup for measuring an amplifier using a directional coupler.

measurement tools: a thermocouple and an infrared thermometer for monitoring temperature, a multimeter for measuring voltage, and a clamp meter used for measuring high levels of current. The output of the pallet amplifier is run through a directional coupler, which is then sent to a dummy load. Figure 6.2 shows a frontal view of the same test bench setup. The output cable runs to an air cooled dummy load shown on the bottom right of the picture. The signal generator is followed by a LPF, sent to a 40 dB pre-amp, and filtered again by a second LPF. All of this filtering ensured that any harmonics measured at the output of the amplifier were generated by the power-amp stage alone, and are not a result of a distorted input signal. Measurement tools

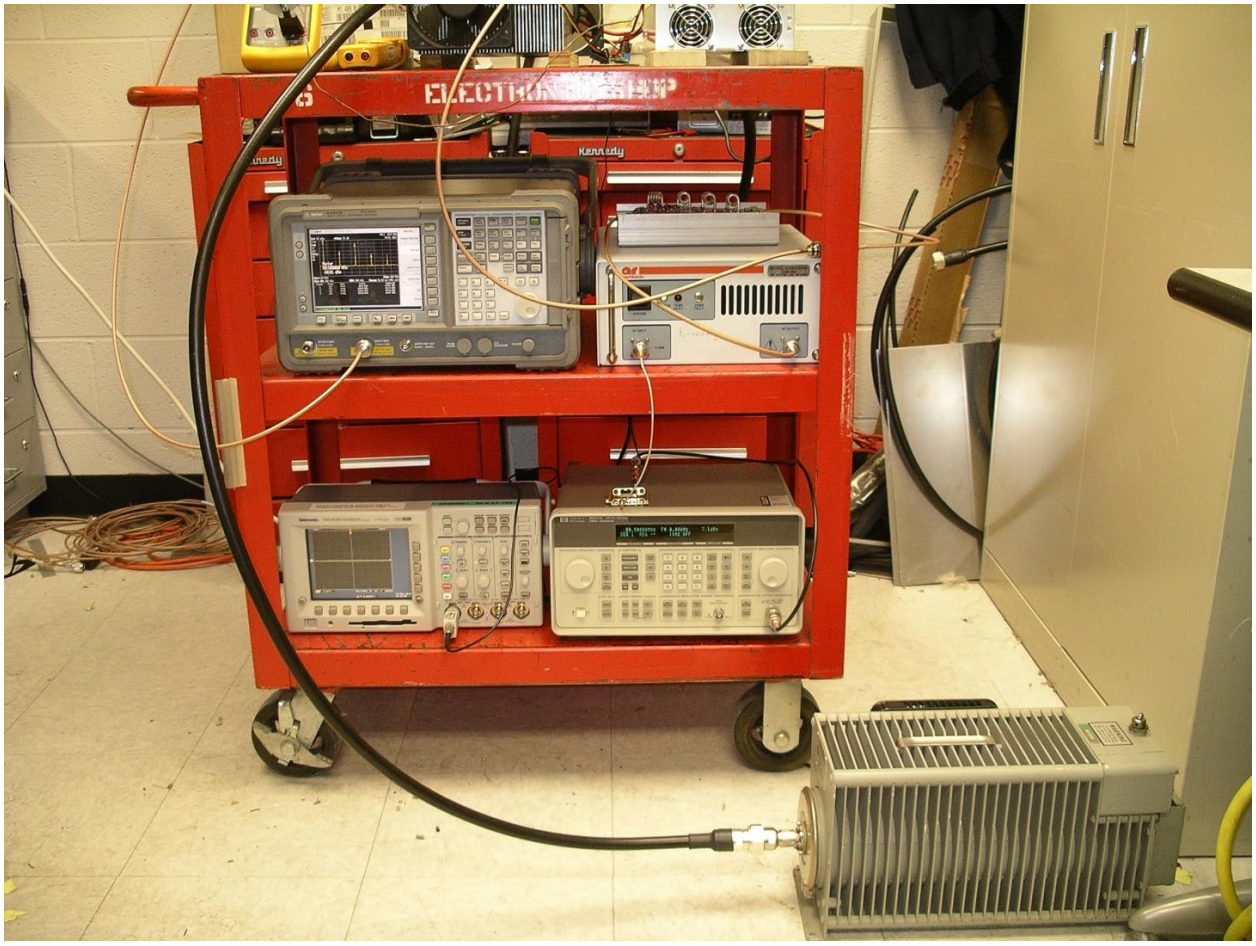

Figure 6.2: Test bench setup for measuring an amplifier using a directional coupler (2).

shown on the left side of the cart include a spectrum analyzer and an oscilloscope. The outputs of the directional coupler can be run to these measurement tools to get the frequency domain response and time domain response of the complete amplifier system. The amplitude and frequency of the signal generator can be swept to determine performance with different input conditions.

6.1 Measurement Examples

More complete amplifier systems have been tested, however these systems require hundreds of hours of work in the form of circuit board layouts, CAD design, and mechanical fabrication. The knowledge gained from testing an amplifier system in a bench test configuration can be just as valuable as the results from testing a complete amplifier chassis during the prototype phase. Moving on to mass production requires testing and debugging issues that are present in an enclosed chassis and not in a bench test. For example, placing input and output cables in close proximity in a system that has 60-70 dB of gain can cause feedback issues. Power supply brownouts causing distortion in the pre-amplifier stage, and EMI issues in the input power splitter are two more issues that appeared while testing a complete amplifier chassis.

Figure 6.3 shows a 2 kW 80.5 MHz amplifier module designed for use in the ReA3 reaccelerator. Ten copies of this amplifier were assembled in the summer of 2011 by the author to satisfy the amplifier requirements of the ReA3 project. These amplifiers will power the 8 accelerating cavities in the third cryomodule of the system, with 2 spares, and will provide useful testing results for the design of FRIB amplifiers.

Figure 6.3: 80.5 MHz 2 kW amplifier testing for the ReA3 reaccelerator.

Figure 6.4 shows a 4 kW prototype assembled by the author for testing the FRIB amplifier designs. These amplifiers have been tested extensively to determine reliability and performance under all different conditions. They can also be used in a process known as SRF cavity conditioning. The construction of an extremely high Q accelerating cavity requires that the surfaces of the cavities be extremely clean. The assembly is done in a class 100 clean room to achieve this goal [5]. Any impurities that remain can be burned off by running the cavity at a high power level for extended periods of time. This is an extreme condition for the amplifier, since full reflection is guaranteed, and is useful in testing the ruggedness of an amplifier system.

Figure 6.4: 80.5 MHz 4 kW amplifier testing.

6.2 Directional Couplers for High Power Measurements

One last detail that can't be ignored is the use of directional couplers for high power measurements. A directional coupler is a four terminal device that is placed in line with the output of a high power amplifier. The signal going though the directional coupler is barely affected, and the two additional ports are used to isolate and measure the forward and reflected signals [18]. These outputs are 30 to 40 dB down from the high power output, which is why there is very little loss through the directional coupler. The coupler outputs can be padded down further if necessary, and sent to a spectrum analyzer or a vector voltmeter for measurement. Figure 6.6 shows a test setup used to measure the high power circulator test data shown in figure 4.8 – figure 4.10.

Figure 6.7 shows the frequency response of a directional coupler designed for 80.5 MHz. The coupling factor is designed to be 40 dB at 80.5 MHz, but drops to 34 dB at the second harmonic of 161 MHz, and 30 dB at the third harmonic of 241.5 MHz.

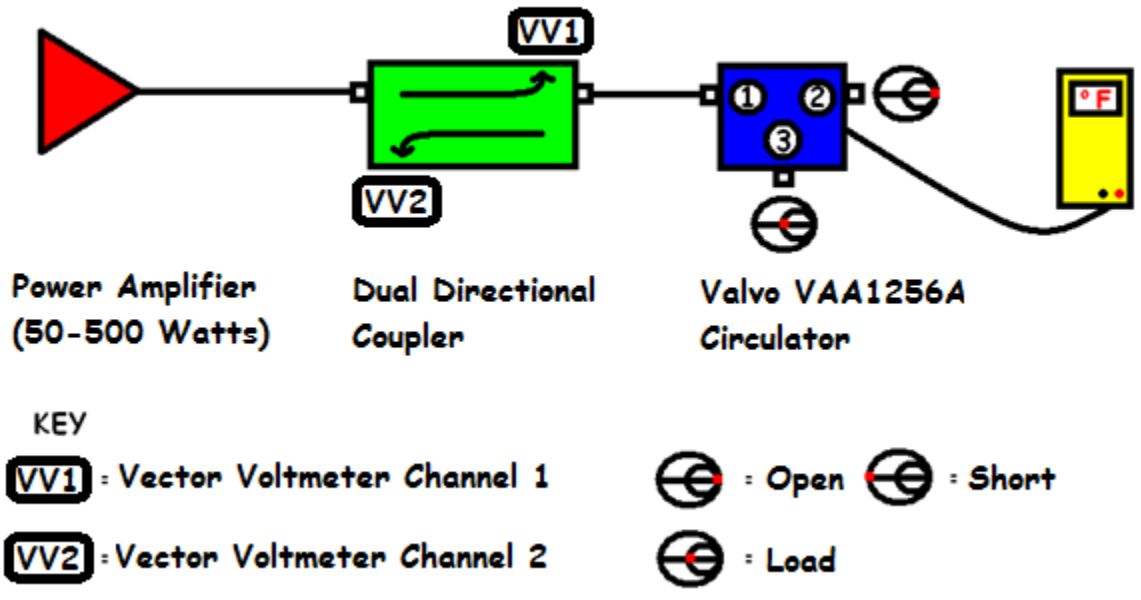

Figure 6.5: Amplifier test setup using a dual directional coupler and vector voltmeter.

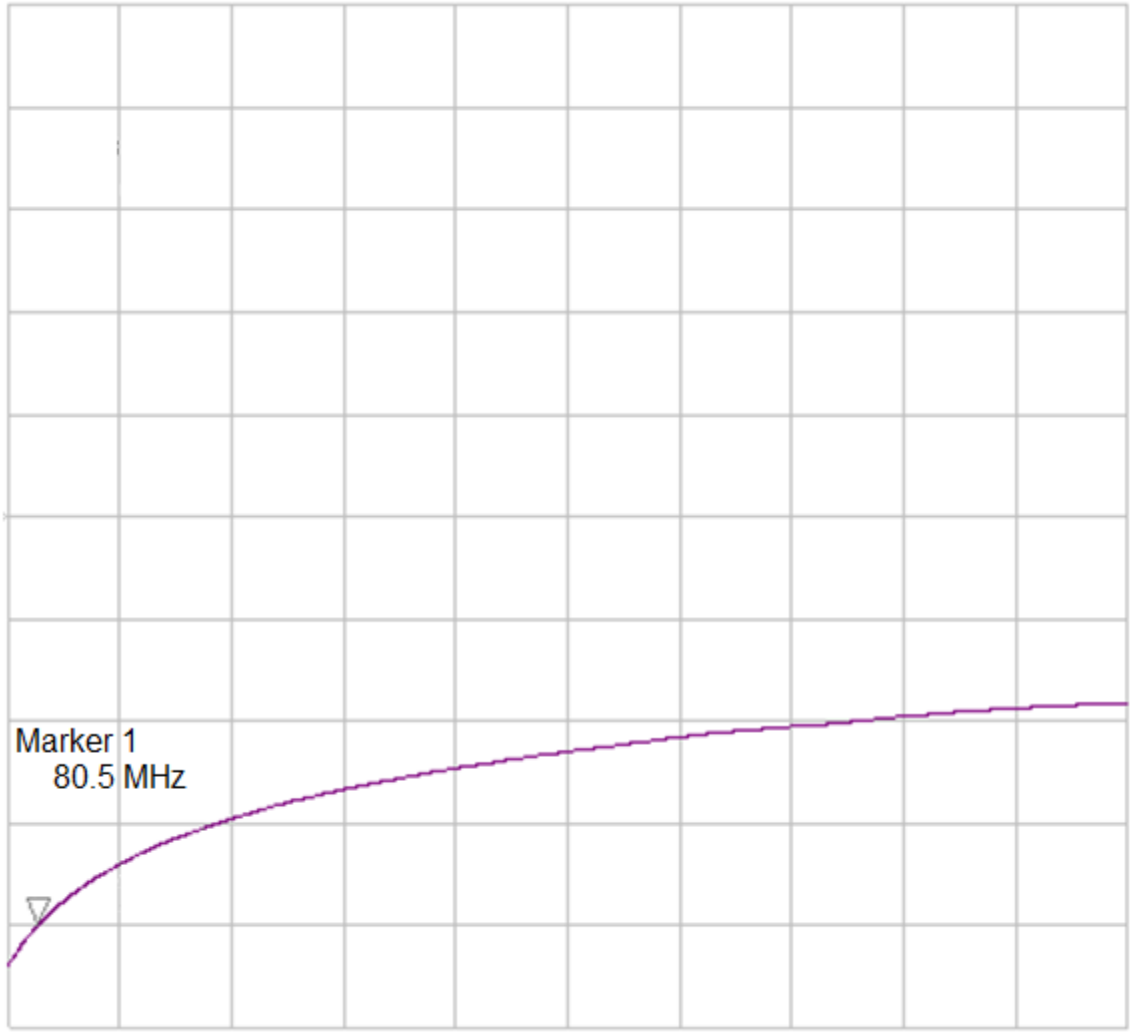

Figure 6.6: Frequency response of an 80.5 MHz dual directional coupler. S21 = -39.9 dB.

This means that the measured outputs of a directional coupler must be calibrated based on frequency, and cannot be taken directly from the measurement equipment. Figure 6.8 shows the spectral content of a 1 kW pallet amplifier measured directly at the output of a directional coupler. After accounting for the decrease in coupling as the frequency is raised, the harmonic distortion is not as severe as it first seems.

Another option that does not suffer from this problem is using a high power attenuator in line with the output of the amplifier. The attenuated output can then be measured directly, since the insertion loss of an attenuator has a wider frequency range. The risk is the damage that will occur if the attenuator fails as a short circuit.

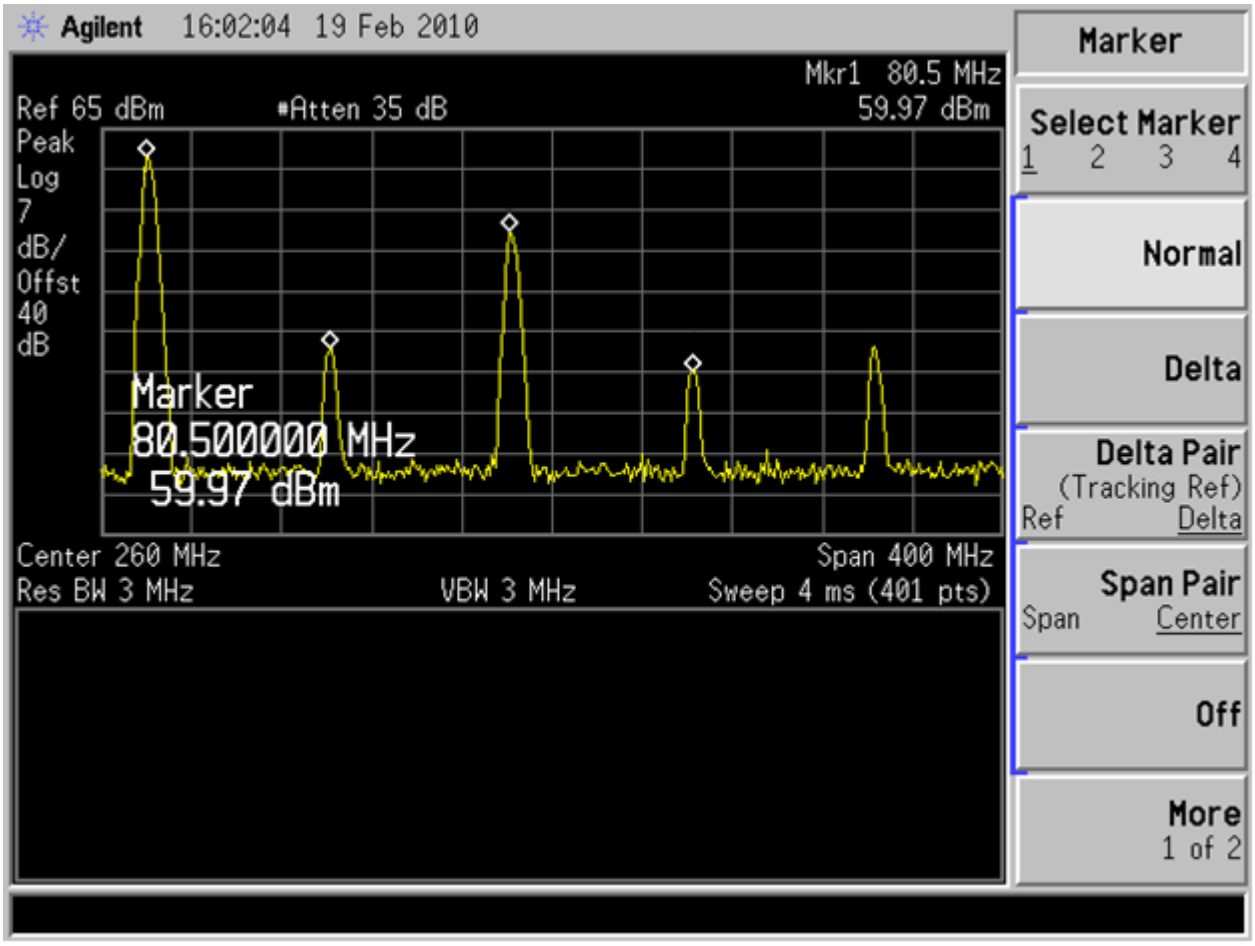

Figure 6.7: Spectral output of a directional coupler before accounting for response.

CHAPTER 7

CONCLUSION AND FUTURE WORK

The development of high power reflection tolerant RF solid state amplifiers has been covered from the specification phase, through designing, prototyping, building, and finally testing a complete amplifier system. The amplifiers were designed to be used in the FRIB linear accelerator, which is currently under construction, and set to replace the NSCL cyclotron accelerator by the end of the decade. A total of 344 amplifiers are needed to drive the linear accelerator cavities that make up the FRIB driver linac. The frequency of operation is either 80.5 MHz or 322 MHz, and the power levels range between 2 kW and 8 kW. Most importantly, the amplifiers need to be able to handle the unpredictable load that an accelerator cavity presents, including the case of full reflection.

The design of the amplifier system is built around 1 kW pallet amplifier blocks, which provide about 27 dB of gain at full power output. These pallet amplifiers are driven into class C operation to achieve the highest efficiency possible, around 70%. The input to the amplifier is limited to 10 dBm, so a pre-amp stage with at least 30 dB of gain is required. The gain of the pre-amp stage and power-amp stage is held constant, while the input signal level is varied to achieve the desired output power.

Driving an amplifier into class C has the benefit of higher efficiency, but produces harmonics that must be removed before the signal is sent to an accelerating cavity. Harmonic levels of -70 dBc are required. This is accomplished with a 7th order Butterworth low pass filter designed for high power operation. A harmonic absorbing high pass filter is also included, such that harmonics are captured and dissipated in a 50

ohm load, rather than being reflected back towards the amplifier. The result is an output signal that is free from harmonics, while maintaining a high efficiency.

A superconducting accelerating cavity is a difficult load to drive, and often presents full reflection to the amplifier. Without a protection system in place, a transistor that was designed to dissipate 500 W of heat could now see 1.5 kW. The solution is to use a circulator in each amplifier. A circulator is a three terminal device which allows power to pass through unaffected in the forward direction, but redirects reflected power towards a 50 ohm dummy load. Circulators are frequency and temperature dependent devices, so care must be taken that acceptable operating conditions are maintained throughout the entire power range. A circulator that is in band at low power could be pushed out of band at higher power. This is more of a challenge for the 80.5 MHz circulators due to the lower inherent bandwidth of these larger devices.

Power combiners are used as a tool to achieve the desired power output levels of 2 - 8 kW using 1 kW amplifier blocks. The most basic power combiner circuit is a TEE combiner, which places two output signals in parallel cutting the impedance in half, and then uses a quarter wave transformer to raise the output impedance back to 50 ohms. These combiners suffer with mismatched loads, and provide very little isolation between the two inputs. A better option is the Wilkinson combiner, which uses a 100 ohm resistor between both inputs, and two 70.7 ohm lines connected to a tee. This configuration has better performance in the case of mismatch, and provides isolation between the two input signals. A third option is the hybrid combiner, which provides the best amount of mismatch tolerance and input isolation, but is costly and complex to assemble for high power applications.

The final chapter discussed testing setup and procedures for high power amplifiers. Two methods of measuring the output of a high power amplifier were presented. The first case was a directional coupler placed in line with the output signal. The directional coupler outputs can be padded down even further, such that they are below the maximum input level for measurement tools such as a spectrum analyzer or an oscilloscope. Knowing the frequency response of the directional coupler and working backwards will then provide the desired high power measurements. The second option is to use a high power attenuator directly in line with the output of the amplifier to reduce the output down to an acceptable level for measurement. Attenuators have the benefit of a more consistent response over frequency when compared to directional couplers, but failure of a high power attenuator could be a catastrophic problem for sensitive electronic measurement equipment.

7.1 Class H Amplifiers

A possible area of study for future work is the investigation of different classes of amplifier operation. The three most common classes of amplifier operation seen in practice are Class A, Class AB, and Class C [11]. Class A provides the lowest distortion at the expense of operating efficiency. Class AB is used in push-pull amplifiers, and provides higher efficiency at the expense of increased crossover distortion. Class C has the highest efficiency of all three classes, but suffers from large amounts of odd-order harmonic distortion. There are several other classes of operation that are useful in specific applications. Class C works very well when the output power of the amplifier is constant, and close to saturation. When the output power is reduced

though, the efficiency is also reduced. This could be a problem in the FRIB amplifiers, since different beams of particles being accelerated require different amounts of power. A class C amplifier is designed for maximum efficiency at maximum power output.

Class C operation works by swinging the output voltage very close to the power supply voltage, which provides maximum use of the available power. Reducing the output power means that the output voltage swing is farther away from the power supply voltage, resulting in less efficient use of the available power. Another option is Class H operation, which uses an adjustable power supply to dynamically adjust the voltage with changing output power levels [21]. This allows higher efficiency operation over a wider range of output powers.

Considering that the total power usage of the completed FRIB facility is over 10 megawatts, even a few percent increase in the efficiency of the amplifier systems would result in millions of dollars of savings in electricity bills over the lifetime of the project.

7.2 Reflection Tolerant Transistors

The most common solution for protecting a solid state amplifier from reflected power is to use a circulator behind every power transistor, but this approach presents many challenges, especially at lower frequency operation. Lower frequency circulators require large amounts of ferrite material, making them expensive, heavy, and very sensitive to changes in temperature and power level. For an 80.5 MHz amplifier, the cost of a 2 kW circulator is more than the pallet amplifier, low pass filters, and power combiners put together. The final 80.5 MHz circulator used for the ReA3 project after 3 revisions was also just barely within specification. Even a slight change in the temperature of the cooling water or the power output requirements could push it out of

range, and destroy thousands of dollars worth of amplifier components. It would be ideal if there was a way to remove circulators from the amplifier system while still maintaining full reflection performance.

Recently, manufacturers have started releasing LDMOS transistor products that can withstand full reflection loads without damage to the device. There are both 300 W products and 1 kW products available on the market [22]. The thermodynamic cooling limit of 200 W/cm^2 still remains though, which means that the 1 kW transistor can only handle full reflection for a short period of time before being destroyed. The 300 W transistor on the other hand can withstand full reflection with constant operation, and stay under the 200 W/cm^2 limit. This provides a unique opportunity for reflection tolerant amplifier design; the circulator can be removed from the system, while still maintaining immunity to full reflection. There is also the added benefit of no temperature dependence or power range limits that occur with a circulator. The only issue with using these transistors in FRIB spec amplifiers would be the power requirements. Reaching power levels of 2 - 8 kW with 300 W blocks would require even more cost and complexity in the power combiners. Considering the high cost and unreliable performance of circulators though, this could be an option worth considering.

7.3 Diamond Transistors

Diamond is the ideal transistor material for high power, high frequency devices due to its extremely high thermal conductivity and high electric field breakdown [12]. With silicon based devices, the limiting factor preventing higher power operation is the amount of heat that can be removed from the transistor package using conventional

techniques. The current state of the art is to use a copper based heatsink cooled with water, and bolted as close as possible to the substrate of the transistor. Copper is a very good conductor of heat, but the issue is getting the heat from the silicon to the copper fast enough before thermal runaway occurs. This is a problem because of the low thermal conductivity of silicon. With diamond based transistors, the material that the device is made of is a better conductor of heat than copper at room temperature. This opens the door for solid state devices in frequency and power ranges previously occupied exclusively by vacuum tube based devices. See figure 7.1 for a comparison of the thermal conductivity of several device materials over a large temperature range.

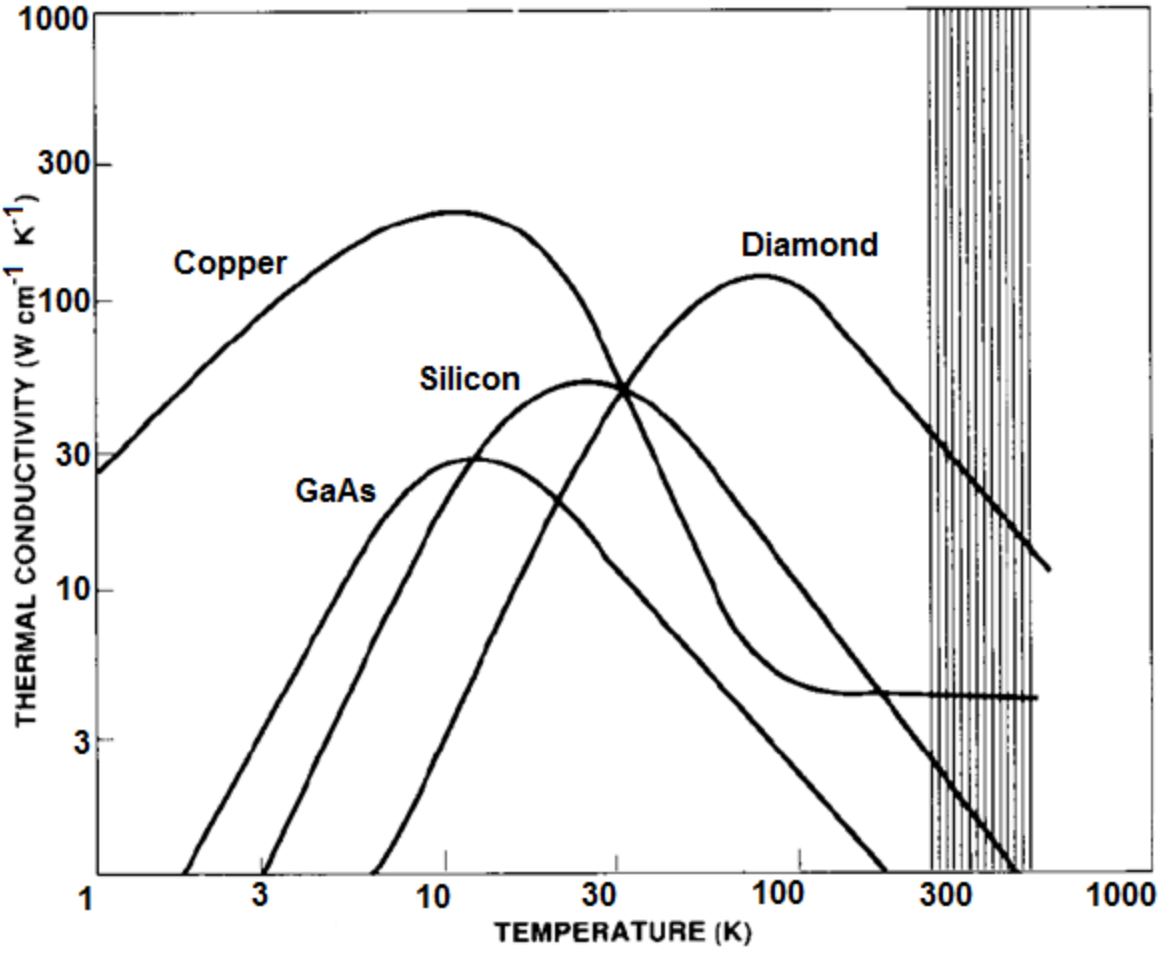

Figure 7.1: Thermal conductivity of diamond compared to copper and silicon [12].

The technology for creating a diamond based transistor exists today: diamond growth, either thin film or single crystal is possible using CVD, p-type and n-type diamond materials can be manufactured, and ohmic contacts to diamond have been demonstrated. The challenge is putting these three advances together in a process that is both reliable and low cost. Once this is achieved, it could be possible to create a 322 MHz 8 kW amplifier for FRIB using a single transistor. This could fit in a 1U size enclosure, compared to the full rack (50U) that the current silicon based amplifier uses. This would not only drastically reduce the amount of space used, but would also increase the reliability of the FRIB linear accelerator by an order of magnitude. The possible failure points of multiple amplifier blocks, power combiners, and circulators could be eliminated. This would be a disruptive technology that changes the entire field of high power high frequency amplifiers, compared to the incremental upgrades that are common in fields such as consumer electronics.

The difficulty of large projects such as FRIB is that the technology used has to be set in stone well before construction of the project even starts [5]. With a 10 year construction time for FRIB, this means that amplifier systems developed right now will be out of date before the first beam of particles is even accelerated. As an example, the National Ignition Facility (NIF) at Lawrence Livermore National Laboratory was designed using state of the art laser technology when construction was started in 1997, but by the time it was completed in 2009, solid state laser technology had greatly surpassed anything that was available in the late 1990s. The only thing an engineer can do to account for this is to make the initial design as modular as possible to facilitate the integration of new technologies as they become available.

While diamond transistors would be ideal for a project such as FRIB, it would take at least another 10 years before that dream was realizable, by which time construction of the facility would already be complete.

APPENDICES

APPENDIX A

2 kW RF Amplifier Setup Procedure

1. Water Leak Test

All of the water routing internal to the case is done with 3/8 inch plastic tubing. Before turning on the water supply, two things need to be checked: first that the water blocks are connected in the correct order, and second that each connection point is secure. The flow of water from input to output is as follows: Water IN => Bottom Parker Fitting => Lower Amplifier Shelf => Upper Amplifier Shelf => Dummy Load => Wilkinson Combiner => Top Parker Fitting => Water OUT.

Each amplifier shelf contains two separate water blocks; one to cool the power amplifier, and one to cool both the pre-amplifier and the filter. A short piece of tubing is used to connect the output of one block to the input of the other block, so the entire amplifier shelf can be treated as one block. Check to make sure that the flow of water from the input to the output of each amplifier shelf is continuous.

The dummy load and Wilkinson combiner sections only contain one water block, and can be identified based on the type of RF cable exiting the back of the shelf. The dummy load has a single thicker RG393 cable connected to it, and the Wilkinson combiner has two thinner RG302 cables connected to it.

Lastly, both the input and output water connections are split in two, forming two parallel water flow paths. The first path is for all of the components described above, and the second path is for the circulator. Since the initial testing is done without a circulator, this path will need to be shorted with a small length of tubing (about 2 ft).

Before turning on the water, inspect each connection point to locate and fix any potential leaks before they occur. Visually inspect the solder joints between each water block and the pipe fittings. Also check the pipe thread connection between this fitting and the Prestolok adaptor. Finally, check to make sure that each end of the water tubing is fully inserted into the Prestolok adaptor.

With all of these checks compete the water source can be turned on. Use a long enough length of water tubing with parker fittings to attach the amplifier to the LCW system. The water output of the amplifier should be connected to the pipe labeled LCWR (R for return). Turn on the return valve first, and then slowly turn on the supply valve while checking for leaks. The water flow rate with the supply valve fully on should be around 1-2 GPM.

2. Temperature Sensor Continuity Test

With the water flow tested, power can now be applied to the amplifier. The water must always be turned on before power is applied to the amplifier. The pre-amplifier is biased into class A, so even with no RF input it will still draw Amperes of current. There is also the possibility that the power amplifier could oscillate, producing enough heat to require water cooling, even with no RF input. As an added precaution, connect an SMA-type 50 ohm load to the input connector on the back panel. Also, connect a 10 kW Altronics water cooled load (RF_LOAD1 or RF_LOAD2) to the tee that combines the two outputs of the Wilkinson combiner using a 3 foot LMR400 cable. These loads must also be connected to the LCW system. When making the water connection, the return port can be identified by a red piece of tape. Note that a 7/16 female-female

adaptor might have to be used to make the connection. As a final check, make sure that the output of each amplifier shelf is securely connected to the input of the Wilkinson combiner.

Connect the amplifier to a 208V/30A plug using a properly rated extension cord if necessary. Make sure that the RF control board is connected to the front panel board with a ribbon cable. Turn the amplifier on using the switch located on the front panel. During normal operation, three green LEDs will be lit. For this initial test, only be concerned with the TEMP OK green LED. This LED will only turn on when all 8 of the TEMP FAULT 1-8 red LEDs are off. If this is the case proceed to the next paragraph. If one of the red TEMP FAULT LEDs is on the problem will need to be tracked down before continuing. If the red LED turned on immediately at power on, then the problem is either a bad (constantly open) temperature switch, or faulty wiring. Turn off power and disconnect the 208V/30A plug before using a multimeter to track down and fix the problem. Once the problem is fixed the green TEMP OK LED will turn on, but the red TEMP FAULT LED will stay on. To reset the trigger simply press the reset button located on the front panel. If a red LED turns on after the amplifier has been on for more than a few seconds, it is possible that a component is actually over-heating. If this is the case, then the faulty component will need to be tracked down and repaired or replaced before proceeding.

The second green LED is the PLC OK LED. This verifies that a PLC connection is made on the back of the amplifier. For initial testing without a PLC, attach an AMP connector to the PLC line with pin 2 shorted to pin 9. This should turn on the green PLC OK LED.

The third green LED on the front panel board is the PS OK LED. This LED is turned on when all three of the power supplies are above a certain voltage level, which will be set in the next section. If one or more of the red PS FAULT LEDs are on, turn the corresponding potentiometer on the RF control board (R24_1, R24_2, or R24_3) clockwise until the green PS OK LED turns on. To reset the red PS FAULT LEDs simply press the reset button again.

The last step in this section is to set the delay time of the reset button on the front panel. Turn one of the power supply reference potentiometer on the RF control board (R24_1, R24_2, or R24_3) counter-clockwise until a red PS FAULT LED turns on. Pressing the result button will temporarily turn off this red LED, but it will turn on shortly after due to the fact that the fault is still there. Use the adjustment potentiometer on the top of the front panel board to set the time between the point when the reset button is pressed, and the point when the red LED turns on again to about one second. Once this delay time is set, turn the same power supply reference potentiometer clockwise until the green PS OK LED turns back on.

At the end of this section all three green LEDs (PS OK, TEMP OK, and PLC OK) should be on, and all 11 of the red LEDs (PS FAULT 1-3 and TEMP FAULT 1-8) should be off.

3. Power Supply Calibration

This section involves two steps: setting the voltage low trip points of each of the three power supplies, and setting each power supply to its final value. The three power supplies in the amplifier are PS1 (a low current power supply for the control electronics

and pre-amplifiers 1 and 2), and PS2/PS3 (two high current power supplies for power amplifiers 1 and 2, respectively). Each of the three power supplies has a V+ ADJ potentiometer that sets the output voltage level. A measurement of this voltage level can be taken by probing the appropriate PS feedback line at the phoenix connector on the RF control board. For safety reasons do not attempt to measure the voltage directly at the outputs of the power supply.

To begin, set the voltage level of each power supply to the corresponding level that is considered to be an under voltage condition. For PS1 this value is 26.5V, and for PS2/3 this value is 42V. Again, this adjustment is made using the V+ ADJ potentiometers on the back of each power supply. The power supply voltage should be able to be set within +/- 50 mV (+/- 0.05V).

The next step will be to set the three power supply reference potentiometers on the RF control board (R24_1, R24_2, and R24_3). Start with all three potentiometers set clockwise such that the green PS OK LED is on, and all three PS FAULT LEDs are off.

Starting with PS1, adjust the potentiometer to the point where turning slightly in either direction turns the green PS OK LED on and off. Once at this point, turn the potentiometer about a half turn clockwise to turn the green PS OK LED on. Press the reset button on the front panel to clear the red PS FAULT LED, and going as slowly as possible, turn the potentiometer counter-clockwise and stop immediately when the red PS FAULT LED turns on. The trip point for PS1 is now set to 26.5V, and no further adjustment of the R24_1 potentiometer should be made. To verify that the trip point is correctly set, turn the power supply voltage up to 28V using the V+ ADJ potentiometer,

press the reset button on the front panel, and slowly lower the voltage to find the point where the red PS FAULT LED turns on again. This voltage should be within +/- 100 mV (+/- 0.1V) of the set point. If it is off by more than this amount, repeat this step, making sure to turn R24_1 as slowly as possible when setting the trip point. If the trip point is within range, set the power supply to its final value of 28V. Again, the power supply voltage should be able to be set within +/- 50 mV (+/- 0.05V).

Repeat this same procedure for the two remaining power supplies (PS2 and PS3), with the only difference being the voltage trip points and final voltage set points. PS2 and PS3 should both be set to trip at 42V, and the final voltage set point for each power supply is 44V.

4. RF Calibration

The final step in the procedure is the calibration of the RF signal chain. The end goal is to calibrate the system such that 10 dBm (10 mW) at the SMA input connector will produce 63 dBm (2 kW) at the 7/16 output connector. The gains in the system (41 dB for the pre-amplifier and 27 dB for the power amplifier) along with the losses (0.14 dB for the Wilkinson combiner and 0.4 dB for the circulator) are fixed and can't be changed. All adjustments must therefore be made at the low level in the RF control board. Along with amplitude, phase is also an important consideration that will be discussed later in this section.

The first step in the process is to set the amplitude and phase on the RF control board to the values that should get very close to the desired output level. For this step, leave the single 10 kW Altronics water cooled load connected to the output. Attach the

output of the signal generator to the SMA input connector of the amplifier with the cable that includes an inline low pass filter. Set the frequency of the generator to 80.5 MHz, ensure that FM modulation is turned off, and set the amplitude to 11.2 dBm. This amplitude setting will provide 10 dBm at the input of the amplifier after cable and filter losses. Next, disconnect the SMA cables from the outputs of the RF control board (RF OUT 1 and RF OUT 2), and connect channels 1 and 2 of the vector voltmeter to RF OUT 1 and RF OUT 2, respectively. A right angle BNC-male to BNC-female adaptor, and a BNC-female to SMA-male adaptor will be needed to make this connection. After checking to make sure that the water is turned on and a load is connected to the output of the amplifier, turn the power on.

Each signal path has separate adjustments for phase and amplitude. For the RF OUT 1 path the amplitude adjustment potentiometer is R6 and the phase adjustment capacitor is C10. For the RF OUT 2 path the amplitude adjustment potentiometer is R8 and the phase adjustment capacitor is C15. With the vector voltmeter set to read amplitude on both channels, turn R6 and R8 fully counter-clockwise such that the measured amplitude is minimized. Next, set each phase adjustment capacitor (C10 and C15) to the point where the measured amplitude is maximized. A full 360 degree rotation might be needed to find this point. Finally, rotate each gain adjustment potentiometer (R6 and R8) clockwise until an amplitude of 100 mV is measured. This is the voltage that corresponds to -7 dBm into a 50 ohm load, which after 41 dB of gain in the pre-amplifier and 27 dB of gain in the power amplifier should result in 61 dBm at the output of each amplifier shelf. Before continuing, disconnect the vector voltmeter probes from the RF control board and reconnect the two SMA cables that were

originally connected. Turn the power output of the signal generator down to -10 dBm and press the RF off button.

With the amplitude and phase values set in the low level, it is now time to proceed to the first high power test. This is the point where the most damage can be done to the amplifier if a mistake is made, so it is a good idea to go slow though this section. With the RF off and the AC power turned off and disconnected, remove the front cover of the amplifier. Between the output of each amplifier shelf and the two inputs of the Wilkinson combiner there will be a 7/16 break point. Disconnect these two cables, and connect the output of each amplifier to a 10 kW Altronics water cooled load though a 6 foot long RG-142 cable. These cables are terminated with a male 7/16 connector on one side and a female 7/16 connector on the other side. For consistency, connect the top amplifier shelf to RF_LOAD1 and the bottom shelf to RF_LOAD2. The directional couplers on each load are calibrated such that port A measures forward power and port B measures reverse power. Check to make sure that each directional coupler element is rotated fully clockwise. Again, for consistency connect channel 1 of the vector voltmeter to port A of RF_LOAD1, and connect channel 2 of the vector voltmeter to port A of RF_LOAD2. Before proceeding, make sure that water is connected to each of the loads. Reconnect the AC power connector on the back panel, and turn the power on.

RF should be set to -10 dBm and turned on at this point. At this input level the expected reading on the vector voltmeter should be around 15 mV/Channel. If this is true, proceed to the next paragraph. If this is not the case, the first thing to check is that the directional coupler elements are rotated fully clockwise. The next thing to check is

the RF signal path. Turn off the power, disconnect the power cable, and verify that the following signal path is correct: Signal Generator => SMA Input Connector => RF Control Board => Pre-amplifier => Power-amplifier => Filter => Dummy Load. Also check the power connections; PS1 should be connected to both preamplifiers, and PS2/PS3 should be connected to power amplifier 1 and power amplifier 2, respectively. If the problem persists then the culprit is most likely a faulty component, which will need to be tracked down and repaired or replaced before proceeding.

If everything checks out so far, slowly ramp up the power while comparing the measured voltages with the expected voltages. The values for forward power should be close to the following values: -5 dBm IN => 100 mV/Channel, 0 dBm IN => 200 mV/Channel, 5 dBm IN => 450 mV/Channel, and finally 11.2 dBm IN => 800 mV/Channel. These values are only the expected values, and could differ from the measured values by as much as 10%. If the measured voltage goes to zero at any point, turn off the amplifier immediately. Reflected power is not being measured in this case, so power that is not going into the load can be assumed to be reflected back towards the amplifier, which could cause serious damage.

If everything is good up to this point, continue with the final adjustment of the amplitude and phase on the RF control board. Accounting for the coupling factor of each directional coupler and the loss in the 6 foot RG-142 cable, the voltage level required for 61 dBm at the output of each amplifier shelf is 827 mV for port A of RF LOAD 1 and 806 mV for port A of RF LOAD 2. These adjustments will be easier to keep track of if the RF OUT 1 path is connected to RF LOAD 1, which is measured by channel 1 of the vector voltmeter. Likewise, the RF OUT 2 path should be connected to

RF LOAD 2, and measured by channel 2 of the vector voltmeter. If this is the case, adjust R6 on the RF control board until 827 mV is read on channel 1 of the vector voltmeter, and adjust R8 on the RF control board until 806 mV is read on channel 2 of the vector voltmeter.

Finally, switch the vector voltmeter to read the phase difference between channels 1 and 2. Make a note of the position of each phase capacitor before beginning. Adjust only one of the phase capacitors on the RF control board (C10 or C15) until the phase difference is within 1 degree of zero. If the first phase capacitor does not seem to be making enough of a difference, return it to its original position and try the second phase capacitor. With this adjustment competed, return to the voltage measurements of each channel, and make sure that they are within a few mV of the original value. If the voltage levels have changed by more than this amount, alternate between adjusting the amplitude and phase until the ideal case is reached (61 dBm output from each amplifier shelf with almost no difference in phase). When this condition is reached, turn the input power back down to -10 dBm and turn the RF off. Also, turn the AC power off and disconnect the power cable from the back panel.

With each amplifier shelf calibrated to output 61 dBm, the next step is to test the Wilkinson combiner, which will combine these two signals to give 64 dBm minus losses at the output. With the power turned off, reconnect the output of each amplifier shelf to the inputs of the Wilkinson combiner. Connect a directional coupler (RF DC1 or RF DC2) to the tee which combines the two outputs of the Wilkinson combiner, and connect this to an Altronics water cooled load (RF LOAD 1 or RF LOAD 2) through a 3 foot LMR400 cable. Attach channel 1 of the vector voltmeter to port A of the directional

coupler closest to the wilkinson combiner, and attach channel 2 to port B. Double check that the directional coupler elements are rotated fully clockwise and water to the load in use is turned on. Reconnect the power cable to the back panel, and turn the power on.

RF should be set to -10 dBm and turned on at this point. At this input level the expected reading on the vector voltmeter should be around 22.5 mV. Also check that the ratio between forward and reverse power (S11) is about -30 dB. Slowly ramp up the input power while monitoring both forward power and S11. The value of S11 should be around -30 dB at all times. If this value ever goes above -15 dB, turn off the amplifier immediately. The values for forward power should be close to the following values: -5 dBm IN => 150 mV OUT, 0 dBm IN => 300 mV out, 5 dBm IN => 670 mV out, and finally 11.2 dBm IN => 1150 mV out. If RF DC1 was used for the directional coupler, 64 dBm at the output would read around 1150 mV on the vector voltmeter. The difference between this and the actual measured value is the insertion loss in the Wilkinson combiner.

APPENDIX B

Circulator Testing Report:

RF-Lambda RFC2101 SN: 20110402

Introduction:

A circulator is required that can operate at a set frequency of 80.5 MHz, from an input power level of 0 W to 2.2 kW CW, and over a temperature range of 85 °F to 95 °F for a load, short, and an open circuit condition at the output port, while maintaining a value of S11 better than -17 dB. Testing was carried out with a network analyzer at low power (10 dBm input) to determine the value of S11 over frequency, and with a directional coupler and vector voltmeter at high power (up to 63.4 dBm input) to determine the value of S11 over power. Finally, the input water temperature was swept over a limited range to determine the value of S11 over temperature at both high and low power.

S11 Over Frequency:

Operating a circulator at high power creates internal heating, which shifts the frequency response of the device. Likewise, when power is turned off the device cools and the frequency response shifts the opposite direction. Eight tuning screws are used to tweak the frequency response of the circulator. Adding screws has the same effect as heating the circulator, while removing screws has the same effect as cooling the circulator. The best case tuning point used for all the following tests was achieved with 5 screws. Adding more screws would shift the value of S11 for a short circuit to an unacceptable level, and removing screws would give less margin for internal heating.

The original specification of S11 = -17 dB for a load, short, and an open circuit condition is not achieved with the current design. S11 drops below -17 dB for all three conditions individually, but there is no point where this specification is met for all three conditions at the same frequency. Since only one tuning point can be used at a time, a compromise must be made. The bandwidth is 0 MHz with S11 no greater than -17 dB, 5 MHz with S11 no greater than -13.5 dB, and 14.6 MHz with S11 no greater than -8.6 dB. As a final note, all measurements were carried out at a fixed temperature of 90.5 °F.

S11 Over Power:

The next step is to measure the value of S11 with increasing power for a load, short, and an open circuit condition. In theory this will heat the device and shift the response curves of the circulator. The frequency is fixed at 80.5 MHz for all of the testing carried out in this report, but the idea is that when looking at plots of S11, a frequency sweep at low power has the same effect as a power sweep at high power. This is confirmed by the value of S11 over power tracking the original network analyzer plots taken at low power. Remember than any shift in S11 over power is due to internal heating of the device. The load condition has the lowest insertion loss and almost no reflection back towards the device, so the frequency shift in this case is only 1.6 MHz over a power range of 2.2 kW. An S11 of -17 dB is maintained at all times, so the part would be acceptable if the load at port 2 was never removed. To be an effective circulator though, the part must also operate with a short or an open circuit at port 2. The short circuit condition has higher insertion loss and almost complete reflection back towards the device with a phase shift of 180°. The frequency shift in this case is 5.3

MHz over a power range of 2.2 kW. S11 is no worse than -13.5 dB, but this is at a fixed temperature of 90.5 °F. Finally, the open condition also has higher insertion loss and almost complete reflection back towards the device, but here the reflected wave is in phase with the forward wave. The frequency shift in this case is the worst at 9.1 MHz, and the power can only be taken up to 1.9 kW before the end of the operating range is reached, and damage to the device becomes likely. Again, remember that all testing up until this point has been carried out at a constant temperature of 90.5 °F.

S11 Over Temperature:

The ideal test of the temperature stability of the device would be to sweep the inlet water temperature from 85 °F to 95 °F at both low power and full power for load, short, and open circuit conditions. This is not possible with the current test setup, so the best option is to observe the change in S11 with the daily temperature variation of the current system of around +/-1 °F. This change in S11 over temperature was then lined up with the change in S11 over frequency to determine a temperature shift in MHz/°F. This calculation was carried out for a short circuit at both high and low power, and an open circuit at high power. There was not enough of a change in S11 for an open circuit at low power and a load at high or low power with such a small temperature variation to make a calculation. The three cases that did work produced similar results, and the average frequency shift due to temperature was determined to be 0.35 MHz/°F. A rough estimate of the frequency shift over a temperature range of +/-5 °F would be 3.5 MHz. It is possible that the frequency shift due to temperature is not linear and could vary with the port 2 terminal conditions, so again this is only a rough estimate. If

this is added to the previous frequency shift over power data that was taken at one temperature, this will result in the frequency shift over both power and temperature. The required bandwidths are then 5.1 MHz for the load, 8.8 MHz for the short, and 12.6 MHz for the open (only up to 1.9 kW). So the part will work up to 2.2 kW with a load or a short and 1.9 kW with an open over the full power range with a temperature range of 85° F to 95 °F, while maintaining an S11 no worse than -8.6 dB at all times.

Conclusion:

With the current device it is impossible to maintain S11 better than -17 dB for a load, short, and an open circuit condition over a power range of 0 W to 2.2 kW and a temperature range of 85 °F to 95 °F. To meet this specification, a different circulator must be used. With the current circulator and an improved cooling system that reduces the frequency shift over both power and temperature, it might be possible to operate over a bandwidth of 5 MHz with S11 better than -13.5 dB with the given operational conditions. Without changing anything in the circulator's design, it might be possible to operate with S11 better than -8.6 dB with the given operational conditions by adding additional tuning screws.

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