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FABRICATION AND ELECTRICAL CHARACTERIZATION
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FABRICATION AND ELECTRICAL CHARACTERIZATION OF ELECTRON BEAM EVAPORATED SILICON FIELD EMITTER ARRAYS

By

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ABSTRACT

FABRICATION AND CHARACTERIZATION OF ELECTRON BEAM EVAPORATED SILICON FIELD EMITTER ARRAYS

By

Garold P. Myers

The fabrication process for and electrical characterization of electron beam evaporated silicon field emitter arrays in a diode configuration are presented. Each array consists of 2000 unsharpened, n-type, polycrystalline emitters. The process produced 80 to 90 such arrays spaced 9 mm apart and isolated from each other on a 4 inch n-type silicon wafer. Additionally, to circumvent the need for small scale probing of the emitters in order to prove field emission, a method for completing the anode structure is given. Many of the arrays exhibited diode characteristics and Fowler-Nordheim emission behavior with turn on voltages in the range of 60 to 80 V. The data for two such arrays is offered. To evaluate the properties of these field emitter arrays, an outline of the currently accepted Fowler-Nordheim theory on field emission from metal surfaces and the assumptions necessary for application to semiconductor materials is included. For comparison, a comprehensive review of current fabrication techniques in addition to some pertinent electrical characterizations are given.

To Kristine, my wife and friend, with all my love.

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CHAPTER 1

INTRODUCTION

Over the last few years, there has been an increase in worldwide effort directed toward the development of structures with submicron geometries capable of cold field emission from various materials into vacuum. Vacuum microelectronics, a term introduced for the first time at the First International Vacuum Microelectronics Conference in 1988, utilizes modern microfabrication technology associated with solid state devices to fabricate structures that employ transport of electrons in a vacuum.

The benefits of vacuum operation such as radiation hardness, temperature insensitivity and high frequency operation leads to possible applications in microsensors, flat panel displays, microwave generation and amplification, and gigahertz to terahertz switching frequencies for digital applications.

Typically, silicon tip or wedge field emitters are formed by wet chemical etching. This process involves lithography on mostly nonplanar surfaces yielding nonuniform geometries within a particular array of emitters. Metal conical emitters are most commonly fabricated by electron beam evaporation. While exhibiting better geometric uniformity, these metal emitters need to operate in an

ultra-high vacuum and have thermal mismatch problems at the interface between the metal emitters and the substrate material.

This thesis presents an attempt to incorporate the best of both areas. Electron beam evaporation of silicon onto a silicon substrate to form the conical emitters involves lithography on mostly planar surfaces which should lead to better geometric uniformity and reproducibility over etched silicon emitters. It also removes the thermal mismatch problem which can occur in evaporated metal emitters on a dissimilar substrate. Another advantage of using silicon as an emitter material is that the tips can be sharpened by low temperature oxidation [30], though it has not been incorporated for use in this work. Also, silicon as an emitter material does not exhibit stringent vacuum requirements for operation.

The most widely accepted theory with respect to cold field emission is presented in Chapter 2. Chapter 3 exposes both a review of emitter fabrication technologies and an update and comparison on some of the most pertinent and successful electrical characterizations. The fabrication technology and physical results of this thesis are reported in Chapter 4 while an account of some electrical results are given in Chapter 5. Finally Chapter 6 summarizes and concludes the progress to date and offers suggestions for continuance of this endeavor.

CHAPTER 2

BASICS OF COLD FIELD EMISSION AND ASSOCIATED GEOMETRIC PARAMETERS

2.1 Introduction

The most widely accepted theory for cold field emission is that first proposed by Fowler and Nordheim [1]. While this theory mainly addresses the situation which involves emission from a planar metallic surface into vacuum it is generally accepted, [2,5,12-23], that with certain assumptions it can be employed in the analysis of nonplanar silicon emission surfaces with reasonable accuracy. Certain works [3,4], have exposed various modifications, such as image potential, field penetration and surface states, to the original theory in an attempt to quantitatively describe emission from semiconductors. These considerations lead to vastly more complex equations describing the tunneling coefficient and density of states and in themselves must use approximations in the solutions.

Since the main focus of this thesis is not a complete exposition on tunneling theory, an outline of the assumptions and derivation leading to the most often quoted form of the Fowler-Nordheim equation will be presented. For a more complete treatment, one can review the works cited in

this chapter and in particular the work by Modinos [4].

2.2 Tunneling theory

Since the emitters considered here are composed of polycrystalline silicon that has been degenerately doped with phosphorous to a concentration of $1x10^{19}\ cm^{-3}$, it is assumed that the material can be treated as metallic. Therefore, the exposition on tunneling theory developed by Modinos [4] and referred to most recently by Zurn et al. [2], is used as a guide. Knowing that the electron energy at the bottom of the conduction band is proportional to its wave vector squared, it is assumed that the electrons available for emission originate there. This allows the free electron model for metals to be used for the density of states. In addition, Fermi-Dirac statistics are deemed to apply with respect to the distribution of electrons among the available energy states.

The number of electron states per unit volume with energy between ϵ and $d\epsilon$ is given by

$$\rho(\epsilon)\ d\epsilon = \frac{8\pi\sqrt{2}m^{3/2}}{h^3}\epsilon^{1/2}d\epsilon \qquad (2.1)$$

where $\rho(\epsilon)$ is the density of states function, m is the electron mass and h is Planck's constant. The probability of an electron state with energy ϵ being occupied is given by the Fermi-Dirac distribution function

$$f(\epsilon) = \frac{1}{1 + \exp\left[\frac{(\epsilon - \epsilon_F)}{k_B T}\right]} \tag{2.2}$$

where T is the absolute temperature, ϵ_F is the Fermi energy level and k_B is Boltzmann's constant. The energy of a free electron is given by

$$\epsilon = \frac{h^2 k^2}{8\pi^2 m} \tag{2.3}$$

where k is the wave vector of the electron. Taking z as the direction normal to the emission surface and k_z as the component of the wave vector in that direction, the electron has energy normal to the emission surface expressed as

$$W = \frac{h^2 k_z^2}{8\pi^2 m} \tag{2.4}$$

Given these equations, it has been shown [4] that the number of electrons available for tunneling with total energy between ϵ and $d\epsilon$ and normal energy between W and dW is represented by

$$N(\epsilon, W)\, d\epsilon dW = \frac{4\pi m}{h^3} f(\epsilon)\, d\epsilon dW \tag{2.5}$$

and

$$N(W,T)\,dW = \frac{4\pi m dW}{h^3}\int_W^{\infty} f(\epsilon)\,d\epsilon = \frac{4\pi m k_B T}{h^3}\ln\left[1 + \exp\left(-\frac{(W-\epsilon_F)}{k_B T}\right)\right]dW \tag{2.6}$$

The emitted current density is given by

$$J(E,T) = e\int_0^{\infty} N(W,T)\,D(W)\,dW \tag{2.7}$$

where J is the current density, D(W) is the electron probability of transmission through the surface potential barrier, E is the applied electric field and e is the charge on an electron.

For an expression for D(W), consider the surface potential energy barrier shown in Figure 2.1 denoted by a solid curve. This curve includes the image potential and applied field effects with respect to how they affect a step barrier when combined. The image potential effect and applied field effect, as they pertain separately to a step barrier, are shown as dashed curves for comparison.

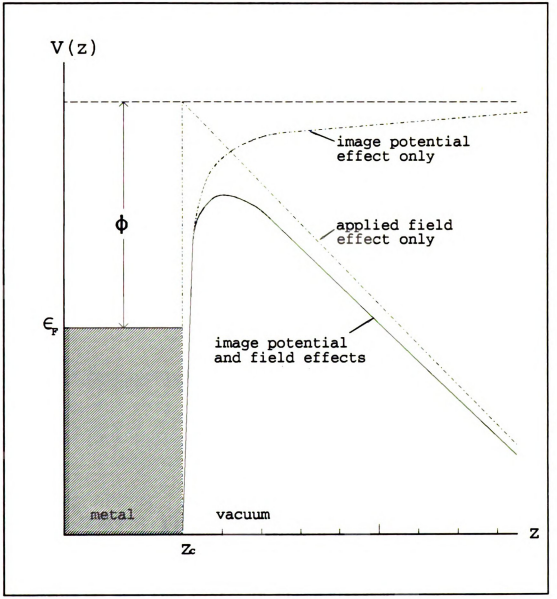

Figure 2.1 Potential energy barriers.

With ϕ as the work function, the potential energy barrier can be approximated by

$$V(z) = \epsilon_F + \phi - \frac{e^2}{16\pi\epsilon_0 z} - eEz \quad for\ z > z_c \qquad (2.8)$$
$$= 0 \qquad for\ z < z_c$$

such that $V(z_c) = 0$, where z_c is the point of the metal-vacuum interface. Then, the transmission coefficient (probability of transmission) is given by

$$D(W,F) = \{ 1 + \exp[Q(W)] \}^{-1} \qquad (2.9)$$

where

$$Q(W) = -2i \int_{z_1}^{z_2} \lambda(z)\, dz \qquad (2.10)$$

and

$$\lambda(z) = \left[\frac{8\pi^2 m}{h^2} [\, W - V(z)\,] \right]^{1/2} \qquad (2.11)$$

and z_1 and z_2 are the roots of the equation

$$\lambda^2(z) = 0 \qquad (2.12)$$

Combining these formulas it has been shown [4] that a

generalized equation for emission current density is given by

$$J(E,T) = \frac{4\pi emk_BT}{h^3}\left[\int_0^{W_1} \frac{\ln\left[1+\exp\left[\frac{-(W-\epsilon_F)}{k_BT}\right]\right]}{1+\exp[Q(W)]}dW\right]$$

$$+ \frac{4\pi emk_BT}{h^3}\int_{W_1}^{\infty} \ln\left[1+\exp\left[\frac{-(W-\epsilon_F)}{k_BT}\right]\right]dW \qquad (2.13)$$

where

$$W_1 = V_{max} + \left(1 - \frac{1}{\sqrt{2}}\right)(e^3E)^{\frac{1}{2}} \qquad (2.14)$$

and

$$V_{max} = \epsilon_F + \phi - 3.79x10^{-4}E^{\frac{1}{2}} \qquad (2.15)$$

After the integration is performed, equation (2.13) can be written in the well known form of the Fowler-Nordheim equation, [2,4-11],

$$J(E) = 1.54x10^{-6}\frac{E^2}{\phi t^2(y)}\exp\left[-6.83x10^7\ \frac{\phi^{\frac{3}{2}}}{E}v(y)\right] \qquad (2.16)$$

with J in A/cm^2, E in V/cm and ϕ in eV. Additionally,

$$y = \frac{3.79x10^{-4}\ E^{\frac{1}{2}}}{\phi} \qquad (2.17)$$

and v(y) and t^2(y) are elliptical functions which are field

dependent [9,25]. Some values for E, y, v(y), and $t^2(y)$ are given in Table 2.1. The values for y, v(y) and $t^2(y)$ were taken from Modinos [4] and the values for E were calculated from equation (2.17) above using ϕ = 4.1 eV for silicon.

Table 2.1 Values of E, y, v(y) and $t^2(y)$.

E (MV/cm^2)	y	v(y)	$t^2(y)$
0.00	0.00	1.0000	1.0000
1.17	0.10	0.9817	1.0072
4.68	0.20	0.9370	1.0223
10.5	0.30	0.8718	1.0418
18.7	0.40	0.7888	1.0648
29.3	0.50	0.6900	1.0897
42.1	0.60	0.5768	1.1162
57.3	0.70	0.4504	1.1443
74.9	0.80	0.3117	1.1733
94.8	0.90	0.1613	1.2032
117	1.00	0.0000	1.2337

Modinos [4] estimates that for field emission E ≤ 60 MV/cm with a typical value of 40 MV/cm. This can be seen by considering the statement by Blakemore [24] that the probability of tunneling by electrons of the Fermi energy is small unless the potential energy barrier thickness is less than 10Å. To facilitate the estimate of the electric field necessary to reduce the barrier thickness to 10Å, consider the triangle shown in Figure 2.2. This is seen to be the top of the pointed barrier shown in Figure 2.1 which

shows the applied field effect only and can be described by deleting the image potential effect term in equation (2.8).

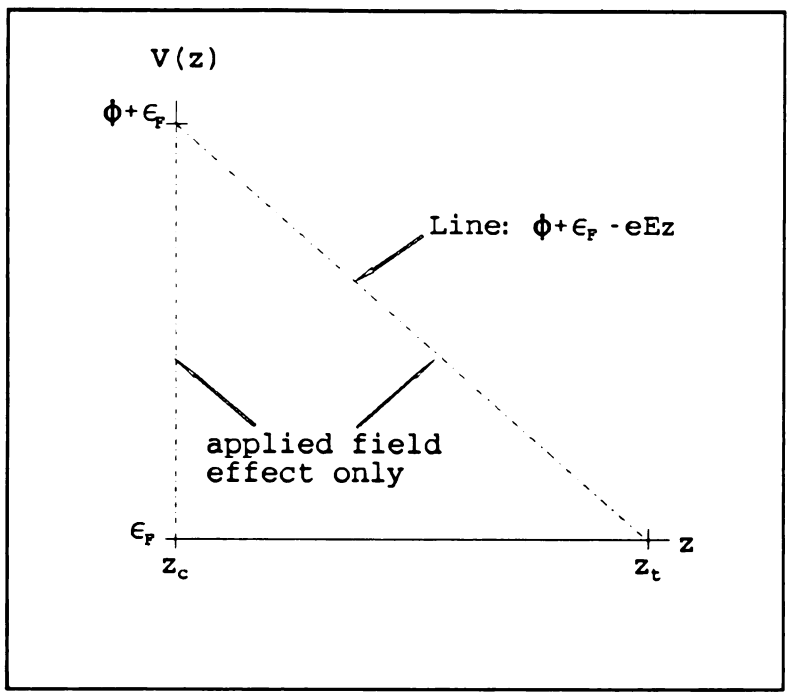

Figure 2.2 Electric field and potential barrier thickness.

Hence, the triangular potential energy barrier can be expressed as

$$V(z) = \epsilon_F + \phi - eEz \quad \text{for } z > z_c \qquad (2.18)$$
$$= 0 \quad \text{for } z < z_c$$

Note in Figure 2.1 that the solid curve which shows the image potential and field effects and the dashed curve which shows only the applied field effect, both have roughly the same negative slope for $z > z_c$ as z becomes large. The slope of this line is, from equation (2.18),

$$slope = -eE \tag{2.19}$$

Also, with regard to Figure 2.2, the slope of the same line can be given geometrically as

$$slope = -\frac{\phi}{z_t - z_c} \tag{2.20}$$

Equating these two expressions for the slope, the electric field can be written as

$$E = \frac{\phi}{e(z_t - z_c)} \tag{2.21}$$

With the work function $\phi = 6.569 \times 10^{-19}$ J (4.1 eV) and the barrier thickness at the Fermi level $z_t - z_c = 10$ Å, it is found that E = 41 MV/cm which is in agreement with Modinos estimate. However, Blakemore notes that cold field emission has been seen to occur for macroscopic electric fields about 30 times smaller than theoretically calculated or about 1.4 MV/cm. He attributes this to the probability that local surface irregularities permit extremely large electric fields on a highly local scale. This is exactly the effect that is sought by devising microtips for field emission.

2.3 Associated geometric parameters

As mentioned in the introduction to this chapter, the Fowler-Nordheim theory was intended to describe cold field emission from a planar metallic surface into vacuum. In

section 2.2 certain assumptions were made to apply this theory to the silicon emitters which are the subject of this thesis. At the end of section 2.2, it was noted that emission generally takes place at macroscopic electric fields at least an order of magnitude less than that which theory dictates and Blakemore [24] attributed this to surface irregularities. These surface irregularities, when they are controlled by microfabrication, have certain characteristics which can be deduced from current-voltage measurements and the use of equation (2.16) if it is assumed that the work function ϕ of the emission material is constant. The most important geometric characteristics with regard to field emitter tips are listed below with definitions to follow later in this section.

β = geometric factor (units of cm^{-1})

β' = field enhancement factor (no units)

r = emitting tip radius (units of length)

α = emitting surface area (units of area)

Figure 2.3 shows the sharp tip between two parallel planes geometry considered in the explanation of these characteristics. It is assumed that the emitter tip is conical and has a hemispherical emitting surface. The fact that the emitter tip has this geometry will be documented with Scanning Electron Microscopy (SEM) later in Chapter 4.

The geometric factor, β, is associated with the electric field and is defined [8,11,25] as

$$E = \beta V \tag{2.22}$$

where E is the electric field at the tip in V/cm and V is the applied voltage. α is the emitting surface area defined

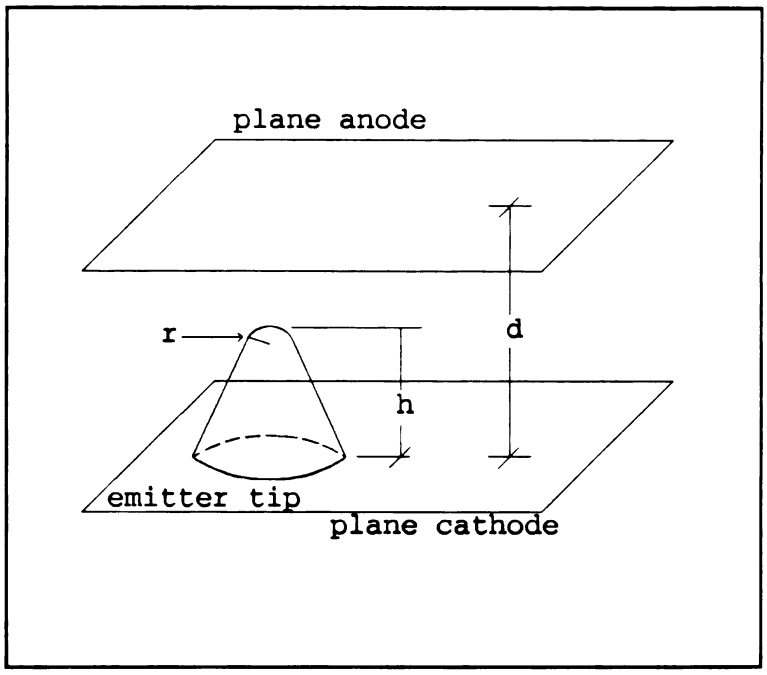

Figure 2.3 Sharp tip between two parallel planes geometry.

by

$$J = \frac{I}{\alpha} \tag{2.23}$$

where I is the measurable emission current. Using equations (2.22) and (2.23), equation (2.16) can be rewritten in terms of the applied voltage and measurable current as

$$\frac{I}{\alpha} = 1.54x10^{-6}\frac{\beta^2V^2}{\phi t^2(y)}\exp\left[-6.83x10^7\ \frac{\phi^{\frac{3}{2}}}{\beta V}v(y)\right] \quad (2.24)$$

or

$$\frac{I}{V^2} = 1.54x10^{-6}\frac{\alpha\beta^2}{\phi t^2(y)}\exp\left[-6.83x10^7\ \frac{\phi^{\frac{3}{2}}}{\beta V}v(y)\right] \quad (2.25)$$

after rearranging. Then, taking the log of both sides of equation (2.25) yields

$$\log\frac{I}{V^2} = \log\left[1.54x10^{-6}\frac{\alpha\beta^2}{\phi t^2(y)}\right] - 2.97x10^7\ \frac{\phi^{\frac{3}{2}}v(y)}{\beta V} \quad (2.26)$$

Looking at equation (2.26), it is noticeable that a plot of $\log\frac{I}{V^2}$ versus $\frac{1}{V}$ yields a curve with a slope of

$$m = -2.97x10^7\frac{\phi^{\frac{3}{2}}v(y)}{\beta} \quad (2.27)$$

which requires knowledge of the electric field at the emitting surface to determine v(y) and, thereby, m. Clearly, the electric field information is not available. However, from Blakemore [24] and Modinos [4] an approximate range for an electric field which supports cold field emission is seen

to be 1.4 MV/cm < E < 60 Mv/cm. From Table 2.1 this gives a range for v(y) of 0.45 < v(y) < 1.00. Another estimate of v(y) [10] gives the range 0.6 < v(y) < 1.0. So, it appears that taking v(y) ≈ 1 will yield the geometric factor β within an order of magnitude. Using v(y) = 1 in equation (2.26) gives

$$\log\frac{I}{V^2}=\log\left[1.54x10^{-6}\frac{\alpha\beta^2}{\phi t^2(y)}\right]-2.97x10^{7}\ \frac{\phi^{\frac{3}{2}}}{\beta V} \quad (2.28)$$

Here, a plot of $\log\frac{I}{V^2}$ versus $\frac{1}{V}$ yields a straight line

with slope given by

$$m = -2.97x10^{7}\frac{\phi^{\frac{3}{2}}}{\beta} \quad (2.29)$$

Therefore,

$$\beta = -2.97x10^{7}\frac{\phi^{\frac{3}{2}}}{m} \quad (2.30)$$

Noting that this equation is independent of the electric field, it is seen that β can be estimated from the slope of this straight line plot by knowing the applied voltage and the measured current. This straight line plot is referred to throughout the literature as the Fowler-Nordheim plot.

The field enhancement factor β' has been defined

[25] as

$$E = \beta' E_0 = \beta' \frac{V}{d} \tag{2.31}$$

where E_0 is the background electric field, V is the applied voltage as before and d is the plate separation. Comparing equations (2.22) and (2.31) it is seen that

$$\beta' = \beta d \tag{2.32}$$

Therefore,

$$\beta' = -2.97x10^7 \frac{\phi^{\frac{3}{2}}}{m} d \tag{2.33}$$

To estimate the emitter tip radius from the geometric factor β, it has been shown [26] that the electric field at the tip, E, is enhanced over the background field, E_0, between the two parallel planes by the equation

$$E = \frac{h}{r} E_0 \tag{2.34}$$

for h >> r, where h is the emitter tip height and r is the tip radius. From equation (2.31) it is seen that $E_0 = \frac{V}{d}$

so that equation (2.34) becomes

$$E = \frac{h}{r} \frac{V}{d} \tag{2.35}$$

Comparing equations (2.22) and (2.35) it is seen that

$$\beta = \frac{h}{rd} \tag{2.36}$$

which can be rewritten to find the tip radius as

$$r = \frac{h}{\beta d} \tag{2.37}$$

once β has been determined from equation (2.30) which requires the slope from the Fowler-Nordheim plot.

Since it is assumed that the emitting surface α is hemispherical, once the tip radius is estimated from equation (2.37) and the supporting equations, α can be found from

$$\alpha = 2\pi r^2 \tag{2.38}$$

which is simply one half the surface area of a sphere of radius r.

As it will be shown later in Chapter 4, the structure of the emitters in this thesis are not quite described by the geometry of Figure 2.3. Therefore, the geometry of an emitting sphere surrounded by a concentric spherical anode should be included. The electric field at the surface of a spherical emitter of radius r concentric with a spherical anode of radius r + t can easily be described using electrostatics and yields the equation [7]

$$E = \left(\frac{r + t}{r}\right) \frac{V}{t} \tag{2.39}$$

Comparing this with equation (2.31) it is seen that the field enhancement factor β' is given by

$$\beta' = \frac{r + t}{r} \tag{2.40}$$

Now, referring to equation (2.32) and noting that d has been replaced by t in this geometry, it can be shown that

$$r = \frac{t}{\beta t - 1} \tag{2.41}$$

So, when it becomes necessary to calculate the actual geometric quantities later, both geometries will be taken into consideration.

CHAPTER 3

COLD EMITTER TECHNOLOGIES: A REVIEW

3.1 Introduction

The fabrication and electrical characterization of densely packed arrays of field emitters has been the subject of considerable effort. A considerable variety of materials has been used to form the cathodes and equally as many fabrication techniques have been employed.

Different materials are used to form emitters in an ongoing attempt to produce devices which are less prone to degradation over periods of extended electrical testing. For example, such degradation can be due to adsorption by the tip of work function raising gasses [13,39] which can reduce current density as seen in equation (2.16). Looking at equation (2.16), it is seen that reduction of the work function [39] would result in an increase in current density if all other parameters are held constant and, thus, is an area of attention. Melting of the emitter tip [25] and surface migration of thin film coatings [39] on the emitter tip are also areas of concern.

One of the main reasons for different fabrication techniques is an attempt at obtaining better geometric uniformity. This leads to less variation between the

geometric parameters of each emitter in an array and also to less variation between arrays. With better geometric consistency it is plausible that a higher percent of the emitters within a particular array would be emitting at an applied potential and thus an increase in current density should be realized. Finally, the need for sharp tips is a constant concern since this is one of the most basic parameters with respect to field emission at low applied potentials.

This chapter gives a review of some of the most recent and noteworthy fabrication techniques and also offers some electrical characterizations for comparison.

3.2 Fabrication techniques

3.2.1 Silicon cathode formation

Due to its prevalence in the semiconductor industry, silicon has received a great deal of attention with respect to cold emitter formation. The most well explored method of fabrication is by the use of wet chemical etching. The etchants can be either isotropic or anisotropic, dopant dependent or not and have various degrees of selectivity with respect to different masking materials [27].

Hunt et al. [14] fabricated silicon cathodes by two wet etch methods and performed a comparison. These two methods are representative of most of the wet etch technology in use today. They both involved using Si_3N_4 as etch masks and employed an anisotropic KOH etch on some samples and

HNO_3:CH_3COOH:HF, a common silicon polish which etches silicon isotropically, on others. The KOH was mixed with secondary butanol such that the etching undercut the 10 μm mask pads on 20 μm centers selecting the <331> facets of silicon, leaving a six sided tip with a 54° side angle and an approximately 100 nm tip radius. The HNO_3:CH_3COOH:HF etch produced steep four sided pyramid structures with a similar tip radius.

Lee et al. [6] and Cade et al. [29] while seemingly working together produced separate reports on the etching of silicon in potassium hydroxide (KOH) and a combination of nitric/acetic/hydrofluoric acid (NAH) etchants. Masking pads of SiO_2 and <100> orientation p-type silicon wafers were used to produce pyramid shaped tips with tip angles of 80° and approximately 65° for the KOH and NAH etched tips respectively. The masking pads were varied in dimension to form tips of various heights. There was some discussion of difficulty in etching of n-type silicon though it was expected that the n-type emitters would prove to support a higher current density than p-type silicon.

Howell et al. [18] reported successful etching of n-type silicon with an impurity concentration of 10^{18} cm^{-3} by wet etching in KOH solution. Using 2 μm square masking pads of undisclosed composition, silicon tips 2 μm in height were realized. A phosphorous doped silica glass (PSG) was used as the dielectric insulating material and was grown by the dissociation of silane and subsequently planarized. After

sputtering of the grid material, lithography and etching produced the complete gridded emitter structure shown schematically in Figure 3.1 [18].

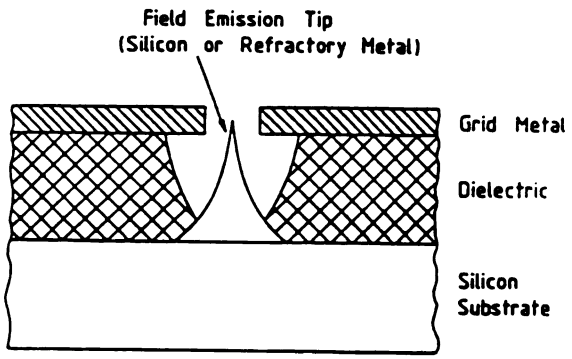

Figure 3.1 Schematic of gridded emitter structure [18], (© 1992 IEEE).

An orientation-dependent-etch (ODE) process, considered proprietary by Gray et al. [20,22], was seen to produce point-like field emitters whose sides are silicon <111> planes. The tip angle was found to be 70° and they reported a final tip radius of 100 Å after utilizing an oxidation step which preserves the <111> sidewalls.

Silicon pyramids created by anisotropic etching of silicon with ethylenediamine-pyrocatechol-water (EPW) using a rectangular mask of Si_3N_4 was reported by Orvis et al. [17,28]. They also used a sacrificial layer technique using phosphorous-doped silicon dioxide glass (PSG) to form the grid and anode of the triode configuration shown schematically in Figure 3.2 [28].

It is noteworthy that most wet chemical etching of silicon produces fairly sharp tips. However, with the

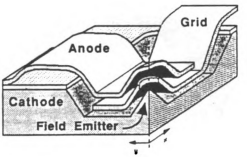

Figure 3.2 Schematic of triode structure [28], (© 1992 IEEE).

exception of Gray et al. [20,22], most of the experimentalists enlist a well known method for producing atomically sharp silicon tips by the exploitation of an anomaly of silicon oxidation which occurs at regions of high curvature [30]. This method involves thermal oxidation, usually dry, in the temperature range of 900 - 1050° C and for times sufficient to grow approximately 1000 Å of silicon dioxide. It was reported to have reduced tips with radii from 20-40 nm to < 1 nm.

Another method of etching silicon to form emitter tips that has received a fair amount of attention is that utilizing reactive ion etching (RIE) techniques.

Zurn et al. [2] have shown that conventional RIE can be used in the formation of planar polysilicon emission tips and edges. They produced lateral field emitters by using a PSG sacrificial layer. A schematic cross section of their planar processed cold microtriode device is shown in Figure 3.3 [2]. In addition to cold field emission testing, hot

cathode emission was also reported.

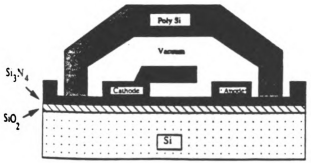

Figure 3.3 Schematic of planar triode [2], (© 1992 IEEE).

Several highly selective anisotropic RIE's and a high temperature lateral thermal oxidation technique were used to form strip-type silicon cathodes according to Spallas et al. [19]. The strip-type cathode diameters ranged from 20-30 nm and the length of the strips was 25 μm. They note that edge to edge spacings of 2 μm were realized and that this process can be used to form emission tips also. A schematic of the silicon strip cathode is shown in Figure 3.4 [19].

RIE and thermal oxidation sharpening were used by Betsui [21] to form silicon emitter tips from n-type wafers. Betsui noted that the shape of the emitter tip can be controlled by the conditions under which RIE occurs. It was reported that for the conditions used, the ratio of the vertical etch rate to side etch rate was approximately 2. Also, both cone shaped and bullet shaped emitters were formed by using circular masks of 2 μm and 1.2 μm diameter respectively. The tips were found to be quite sharp with a radius of 20 nm after oxidation sharpening.

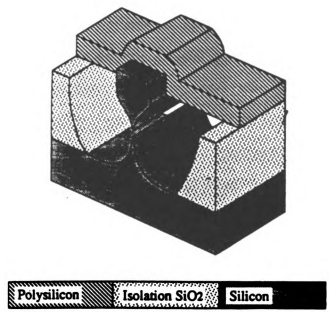

Figure 3.4 Schematic of silicon strip cathode [19], (© 1992 IEEE).

McGruer et al. [16] also revealed the use of RIE to form silicon emitter tips. They used n-type silicon wafers and SiO_2 discs of undisclosed diameter as the etching mask. The RIE consisted of 3:1 SF_6:O_2 at 100 watts RF power. A highly anisotropic 4 to 1 depth to undercut etching ratio was reported which after oxidation sharpening of the tips resulted in tips of 1.3 μm in height.

Another interesting method of silicon tip fabrication involves using a mold technique. Zimmerman et al. [31] offer a process that can be used for almost any emitter material that can be deposited on a surface. Basically, a hole is defined with vertical side walls. Then, the hole is partially filled with a sacrificial layer to the point where

a symmetrical cusp forms at the center of the hole as the side wall growth converges. The conductive emitter material is then deposited by any means appropriate to form the tip. After the sacrificial layer is removed, the resulting tip can be encapsulated in vacuum. Zimmerman's complete process allows for fabrication of a triode configuration which used chemical vapor deposition (CVD) of polysilicon to form the emitter. A schematic of the completed microtriode is shown in Figure 3.5 [31].

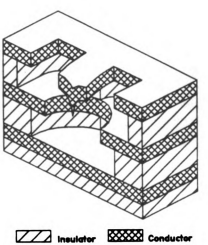

Figure 3.5 Schematic of molded emitter microtriode [31], (© 1992 IEEE).

A mold fabrication technique reported by Sokolich et al. [13] utilizes a KOH anisotropic etch to define pyramid shaped holes in a <100> silicon substrate. The holes are then thermally oxidized to produce a thin oxide etch barrier. Polysilicon is deposited into the holes to a thickness of several hundred microns. Then a silicon etch is used to remove the silicon substrate mold wafer which yields

very uniform tips on the self supporting polysilicon substrate. No mention of how the polysilicon was protected from the silicon etch was offered. A thin metal film is applied on top of the SiO_2 which is on top of the polysilicon tips to form a self aligned gate. Subsequent steps remove a portion of the metal film at the tip of the emitter exposing the SiO_2 so that it can be etched back to expose the polysilicon tip. The final device, referred to by the authors as a FETRODE (Field Emission Triode), is shown schematically in Figure 3.6 [13].

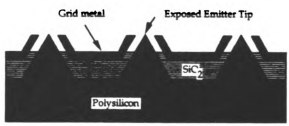

Figure 3.6 Schematic of molded emitter FETRODE [13], (© 1992 IEEE).

Some other processes worth mentioning are those of the silicon avalanche diode (SAC) and the use of argon sputtering of tips for sharpening purposes. Recent reports [32,33], both reveal the use of p-n junctions and avalanching as the means to obtain field emission from emitters of different configurations and shapes. Additionally, Asano and Tamon [12] have shown that argon sputtering of silicon emitter tips has proved useful in tip sharpening.

As a final note, Binh and Chaouch [34] have reportedly

fabricated silicon tips prepared exclusively from a thermal sharpening technique in a vacuum of 10^{-10} Torr. Here, the initial single crystal rods which are 0.5 x 0.5 mm^2 are cut from a p-type, boron silicon wafer, with selected orientations. The tips are held mechanically by clamps during heat treatments by electron bombardment of the tip end. The sharpening temperature of 1600 K resulted in final tip radii of about 100 nm.

3.2.2 Coated silicon cathode formation

In addition to bare silicon being used as a cathode material, many emitters consist of using silicon tips as a basis for thin film depositions of various materials that provide the actual emission material vacuum interface.

Busta et al. [25] covered anisotropically etched silicon pyramids with thin films of tungsten via low pressure CVD. They were successful in depositing both 50 Å and 1200 Å thick films by the silicon reduction method of WF_6. In a similar experiment Ravi et al. [35] deposited tungsten on sharp silicon tips by the same method as that described by Busta. Various thicknesses were deposited ranging from 10 Å to approximately 350 Å. A subsequent report by Marcus et al. [36] updated reports on tungsten deposition and also revealed successful depositions of a variation of tungsten referred to as β-W and the deposition of gold on silicon tips. TEM (Transmission Electron Microscopy) images of silicon tips with tungsten shells of

1.0, 5.0 and 35 nm thick are shown in Figure 3.7 [36].

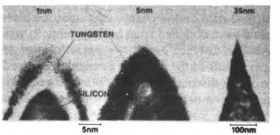

Figure 3.7 TEM images of tungsten coated silicon tips [36], (© 1992 IEEE).

Adler et al. [37] showed that molybdenum could also be deposited on silicon tips. The silicon tips were formed by a mold technique and the molybdenum was deposited by an undisclosed method. Subsequent deposition of oxide and molybdenum again followed by patterning and etching formed a diode configuration. Tip radii of the metal coated emitters was reported to be on the order of 300 Å.

Branston and Stephani [38] used ion beam etching with argon to form silicon tips that were used as the basis for deposition of titanium, tantalum and platinum films. The thickness of the metal film coatings was reported to be 30 to 50 nm and achieved by magnetron sputtering.

An interesting report was generated by van Gorkom and Hoeberechts [39] which utilized a p-n junction diode as the emitter. While this was seen earlier in the previous section, these authors included a monolayer of cesium on the n-type surface at the vacuum interface. This served to reduce the work function to approximately 1.7 eV thereby

increasing the probability of emission.

3.2.3 Non-silicon cathode formation

Since the list of materials that have been used to form various shapes of emitters is quite lengthy, a brief summary is offered on some of the most current results.

Diamond cold cathodes have been fabricated by Geis et al. [41]. The emitters were formed by fabricating mesa-etched diodes using carbon ion implantation into p-type diamond substrates. A schematic of the structure is shown in Figure 3.8 [41].

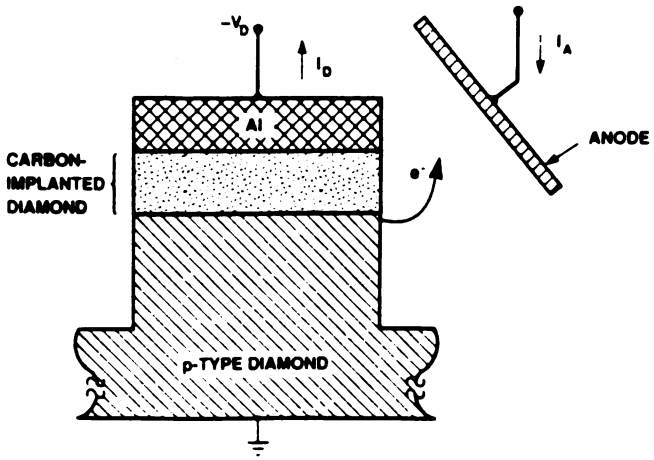

Figure 3.8 Schematic of diamond cold cathode diode [41], (© 1992 IEEE).

Tungsten lateral emitter triodes have been fabricated by Kanemaru and Itoh [44,45]. The tungsten electrodes are arranged laterally on a quartz glass substrate by using photolithography and dry etching.

Nureki and Araragi [46] have reported a planar field emission device which has a tungsten/aluminum thin-film

electrode deposited on a quartz substrate. The tungsten film is 1500 Å thick and serves as the source for field emission. The aluminum is used for stress relaxation of the tungsten and reduction of the sheet resistance. They also employed a three dimensional gate for electron extraction so as to approach the efficiency of a vertical device.

Another lateral tungsten device was fabricated by Carr et al. [42]. The wedge cathode is composed of a titanium:tungsten-tungsten film overlaying an aluminum adhesion film. Magnetron sputtering was used for metal deposition.

An interesting fabrication process was developed by Fukuta and Betsui [47]. This process uses tantalum as the emitter material which has the noteworthy characteristic in that it can be anodically oxidized. Wet chemical etching of the tantalum beneath square SiO_2 masks was used, which is highly reminiscent of the wet chemical etching of silicon. They also employed the oxidation characteristic to sharpen the tips and remove the mask pads which resulted in sharp tips of radius less than 20 nm.

Bakhtizin et al. [48] fabricated GaAs cathodes. The basic process involved magnetron sputtering of tantalum onto the wafer surface which was followed by oxidation of the tantalum to create the Ta_2O_5 etching mask. Formation of the GaAs tips was achieved by ion-plasma etching and removal of the protective mask was obtained by high-frequency discharge in an argon medium. The resultant tips varied in height from

5 to 30 μm with tip radii less than 1000 Å

Kaneko et al. [49] have documented the fabrication of wedge shaped field emitters made of molybdenum. The geometry is quite different and difficult to describe. The molybdenum emitters were deposited on a glass substrate through a stripe metal mask by either RF sputtering or electron beam evaporation. In a different report, Kaneko et al. [50] used the same methods for deposition of molybdenum to form star shaped emitters consisting of four wedges. Figure 3.9 shows (a) a planar view and (b) a cross sectional view at A-A′ of the star shaped emitter structure [50].

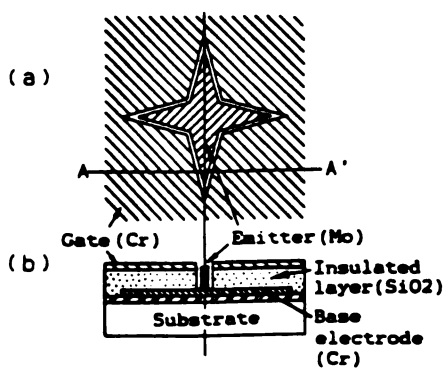

Figure 3.9 Schematic of molybdenum star shaped emitter [50], (© 1992 IEEE).

Of special interest is the fabrication of molybdenum cone emitters by Spindt et al. [11,40,43]. The reason is that their fabrication process was used as a guide to the formation of the silicon emitters which are the subject of this thesis. The highlight of the fabrication process involved electron beam evaporation of molybdenum at normal incidence to the substrate through a decreasing aperture,

caused by the sidewall adhesion of the evaporant, to form the cone shaped emitters as the circular opening closes. This process, with minor variations, will be disclosed in detail in Chapter 4. A schematic of the thin-film field emission cathode (TFFEC) [11] is shown in Figure 3.10.

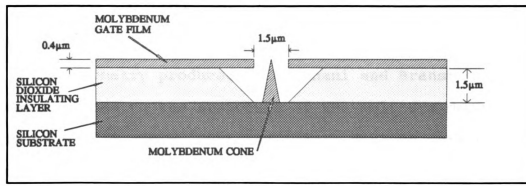

Figure 3.10 Schematic of a TFFEC.

Djubua and Chubun [51] evaluated and compared Spindt-type cold cathodes made of molybdenum, lanthanum hexaboride, hafnium and diamond-like carbon. All of the conical cathodes were formed by electron beam evaporation as in the process described by Spindt et al. [11,40,43] above.

3.3 Electrical characterization

As can be seen from the brief summary of current fabrication technologies, the list is large. It should be noted that since the device geometry plays such a large role in the emission characteristics of the device, that direct comparison with other devices has limited use unless the devices are almost alike in structure. It is seen as important that a concise cross section of reported

electrical characterizations for a few different emitter materials and geometries is needed in contrast to a larger quantity. In this section, some of the most recent and pertinent results will be presented with emphasis on silicon as an emitter material. For contrast, results from a silicon coated and non-silicon cathode will be included.

3.3.1 Silicon emitter electrical results

The geometry produced by Stephani and Branston [23] comes as close to the structure of the emitters described in this thesis as any encountered. Their devices were of a diode configuration with a point emitter 3 μm in height and having a tip radius of 25 nm. Additionally, the anode includes a hemispherical portion centered above the emitting tip.

Though the data available was limited, they reported results for a single emitter. A Fowler-Nordheim plot of one such diode is shown in Figure 3.11 [23]. At the bottom of this plot the equation of the regression line is given. This gives the slope of the line as m = -1123.88. The minimum and maximum voltages shown in the plot are approximately 130 V and 150 V respectively and the current range is about 6 to 100 nA. The data offered allows the calculation of some of the geometric characteristics for both the sharp tip between two parallel planes and that for the concentric spherical arrangement as elaborated on in Chapter 2.

Considering the sharp tip between two parallel planes

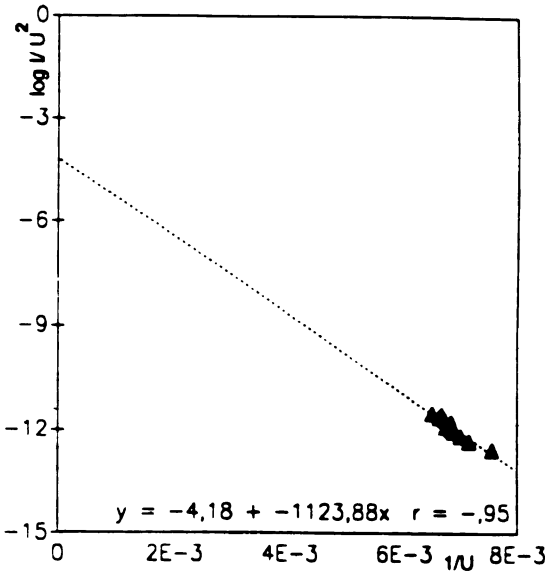

Figure 3.11 F-N plot of results [23], (© 1992 IEEE).

geometry, that was shown in Figure 2.3 and explained in section 2.3, and using equation (2.30) with the work function ϕ = 4.1 eV, it is found that the geometric factor β = 2.19×10^5 cm^{-1}. Using the authors suggested values of the tip height h = 3 μm and the tip to plane anode separation of 2 μm, leads to a plate separation of d = 5 μm. Using equation (2.32), this yields a field enhancement factor β' = 110. The value for the electric field at the emitting tip is E = 32.8 MV\cm for an applied voltage of 150 V using equation (2.22). As a check for validity, equation (2.37) shows the tip radius to be r = 27.4 nm, which is in close agreement with the authors estimate.

For the concentric spherical geometry related in

section 2.3, the distance between concentric spheres is estimated, from the data provided, to be 2.5 μm. From equation (2.41) r = 46 nm and from equation (2.40) β' = 55.

Contrasting the two sets of values it is clear that either is an acceptable estimate of the geometric parameters since, in the theoretical development of Chapter 2, it was noted that β and, hence, β' would be valid only within an order of magnitude due to the approximation of v(y).

Hunt et al. [14] tested KOH etched silicon emitters in a diode configuration. Since the KOH etched silicon tips are recessed into the wafer surface, the actual sharp tip between two planes geometry is altered. In their case, the tip to plane anode distance and the distance between the two parallel planes is equal, hence, d = 920 nm.

The I-V and Fowler-Nordheim plots for a diode structure tested at two slightly different temperatures is shown in Figure 3.12 [14]. The diode structure is composed of 9 arrays that have 50x50 tips each, combining to a total of 22,500 emitters. The average tip radius of the unsharpened silicon tips was estimated to be 100 nm. A noticeable aspect of the Fowler-Nordheim plot is that for the 300 K curve there is a dual slope. One at low voltage and current and another at the higher voltage and current. This has been reported elsewhere in the literature [15], however, no explanation for its cause is mentioned. For the calculations presented here, the higher voltage portion of the F-N curve is considered.

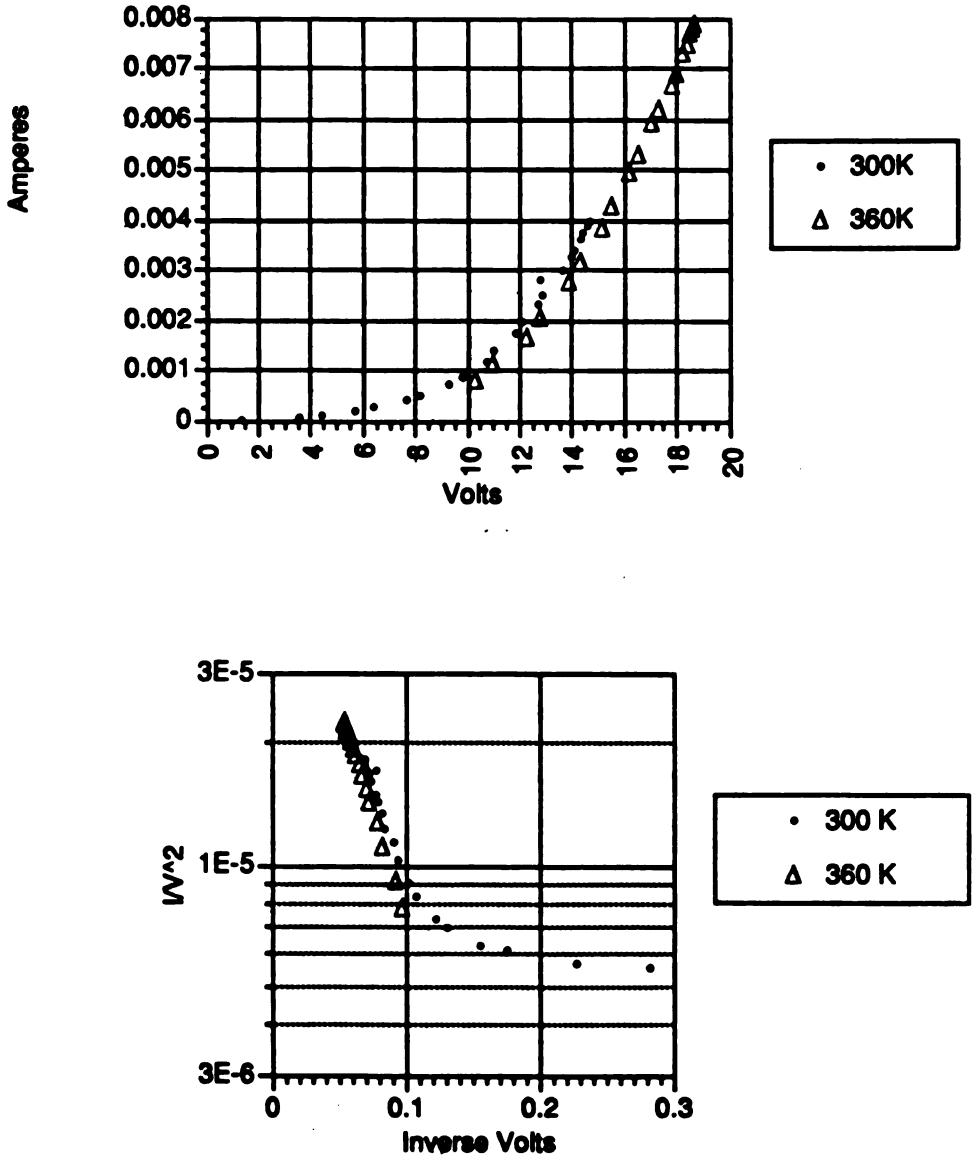

Figure 3.12 I-V and F-N plots, Hunt et al. [14], (© 1992 IEEE).

From the two plots, the maximum current is seen to be around 8 mA at 18.5 V and the minimum current to be about 0.75 mA at 10 V. Next, the slope of the Fowler-Nordheim curve is calculated to be m = - 1172. Taking ϕ = 4.1 eV, it is found that β = 1.04x10^5 cm^{-1} from equation (2.30) and β' = 9.6 from equation (2.32). The authors have estimated the field enhancement factor to be 47 by simulating the electric field on the tip. Though the value calculated here is low with respect to the simulated value, it is within an order of magnitude which is acceptable regarding the approximation made in section 2.3 for β and, hence, β'. Since the geometry differs from the theoretical work in this thesis, no further calculations are possible. It is noteworthy that the maximum current reported works out to be approximately 350 nA per emitter for the unsharpened tips, assuming all tips in the array are emitting.

With respect to the sharpened tips where no definite tip radius was given, the maximum current recorded was about 10 mA at 13 V which works out to 440 nA per emitter, again assuming all tips are emitting. The authors estimated value of the field enhancement factor was β' = 300.

While the dependence of β' on tip radius is not explicit in equations (2.30) and (2.32), it is seen that tip radius does have a noticeable effect on the emitted current versus applied voltage and hence on the slope of the Fowler-Nordheim curve which is a factor in equation (2.30). Also note, that the tip radius does appear explicitly in equation

(2.40) for the concentric spheres geometry.

3.3.2 Tungsten-coated silicon electrical results

Busta et al. [25] electrically characterized their tungsten clad silicon pyramids in a manner similar to that presented in this thesis. In fact, some of the theoretical aspects presented in Chapter 2 originated in their work.

Figure 3.13 [25] shows the Fowler-Nordheim plots for 50x50 emitter arrays coated with 50 Å of tungsten. Figure 3.14 [25] shows the Fowler-Nordheim plot for a 50x50 emitter array coated with 1200 Å of tungsten. In both testing situations, a brass anode sufficiently large to cover the whole array was brought within a distance d to the base of the cathodes. The three anode distances used were 7 μm, 16 μm, and 60 μm and were monitored by use of a stereo microscope. This test situation is described by the sharp tip between two parallel planes geometry for electrical testing and subsequent geometric considerations. The tip radius was estimated to be between 100 and 500 Å. The various distances used are noted on the plots.

The authors report that for the array depicted in Figure 3.13 and an anode distance of 16 μm the values of $\beta = 3.2 \times 10^5$ cm^{-1} and $\beta' = 510$ were calculated from the slope of the curve. Since no mention was made as to the tip heights, an estimate of the tip radius cannot be made with the equations presented in Chapter 2. However, from the same figure, the test voltage was seen to range from 200 to 330 V

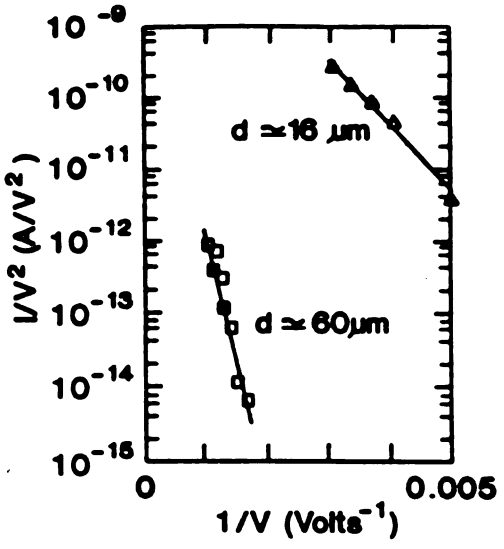

Figure 3.13 F-N plots for 50 Å tungsten film array [25], (© 1992 IEEE).

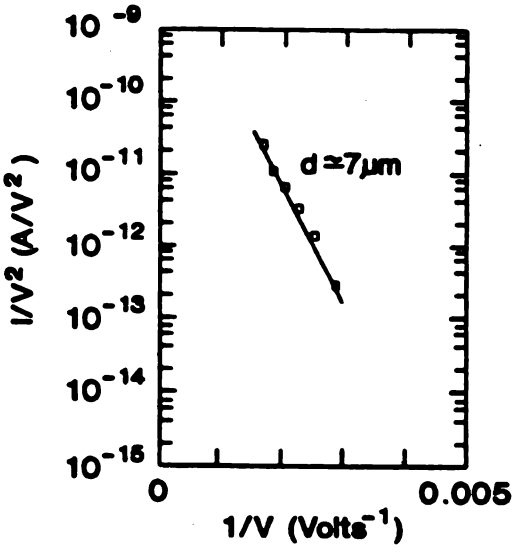

Figure 3.14 F-N plots for 1200 Å tungsten film array [25], (© 1992 IEEE).

and the measured current from 160 nA to 32 μA. This yielded a maximum current of 12.8 nA per emitter at 330 V, assuming all tips in the array are emitting.

For an anode distance of 60 μm, values of $\beta = 7.2 \times 10^4$ cm^{-1} and $\beta' = 480$ were reported. From the plot in Figure 3.13, the voltage range was approximately 600 to 1000 V and the measured current ranged from 22 nA to 1 μA. This showed a maximum current of 0.4 nA per emitter, again assuming all tips are emitting.

For an anode distance of 7 μm, a value of $\beta' = 100$ was reported. Using equation (2.32), this yields $\beta = 1.4 \times 10^5$ cm^{-1} for the geometric factor. From the plot in Figure 3.14, the voltage range was estimated to be from 350 to 600 V and the measured current range was 30 nA to 8 μA. The maximum current showed an emission current of approximately 3.2 nA per emitter, again assuming all tips are emitting.

3.3.3 Molybdenum conical emitter electrical results

Since the molybdenum cones created by Spindt et al. [11,40,43], are among the most thoroughly tested and were first reported in 1968, it seems appropriate that some of the most recent electrical characteristics of these field emitters be presented here.

Figure 3.15 [43] shows a current versus voltage plot for an array consisting of 10,000 emitter tips. The standard drive voltage used was 60 Hz, half wave rectified. The range of the applied voltage is seen to be from about 60 to 110 V

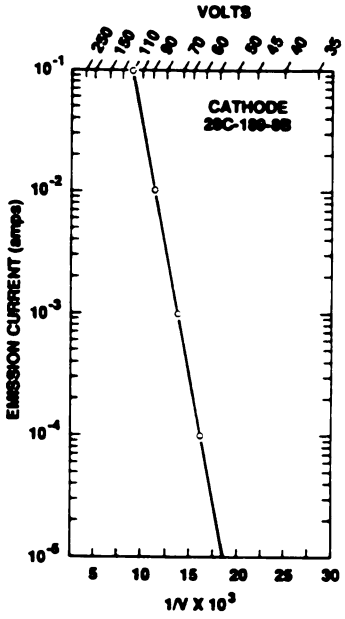

Figure 3.15 Current versus inverse voltage plot for a 10,000 emitter array [43], (© 1992 IEEE).

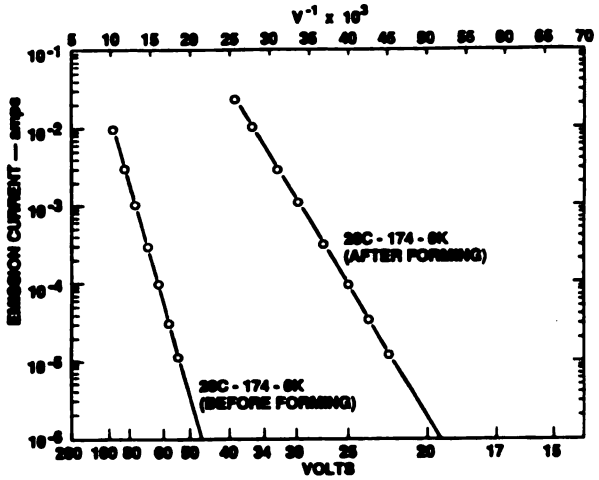

Figure 3.16 Current and voltage traits in regard to field forming [43], (© 1992 IEEE).

with a related current range from 10 μA to 100 mA. Calculating the necessary values to find the slope of the Fowler-Nordheim curve, not presented in the article, it is found that m = - 47.8. This leads to $\beta = 5.9 \times 10^5$ cm^{-1} using equation (2.30). Since the necessary geometric information for further calculations was not presented, the field enhancement factor cannot be computed.

The peak emission current of 100 mA for the 10,000 emitter array amounts to 10 μA per emitter, assuming all tips are emitting. While this seems quite large compared to other reports that have been reviewed here, it must be pointed out that geometric uniformity plays a large role in determining the number of tips that are actually emitting within a particular array. The authors have also noted that the largest tip loading that has been achieved to date is 500 μA per emitter with a 16 tip array [52].

An interesting feature was explored by Spindt et al. [43] that showed a marked effect on the emission characteristics of their emitters. They employed a field forming process [53,54] which resulted in enhanced emission. Figure 3.16 [43] shows the emission current versus inverse voltage curves for a 10,000 emitter array both before and after the forming process is performed. The forming process involves heating of the emitter while the tips are under a high electric field stress. The emitter tip is then altered to a configuration that causes the electric field to increase locally at the tip for a given applied voltage.

Thus, for the same applied voltage, a dramatic increase of several orders of magnitude in the emitted current is apparent. If the emitter is cooled while in this enhanced mode, then, when the emitter is restarted, the current and voltage characteristics are repeatable for the low voltage curve in Figure 3.16. Their experiments also disclosed that this field forming process is both reversible and repeatable.

3.3.4 Tabulation of electrical and geometric results

Table 3.1 offers a concise summary of some of the electrical results and geometric parameters given throughout section 3.3. The table includes values offered by the referenced authors as simulated or calculated. It also includes values calculated using the methods described in Chapter 2. Below each value in the table there is a notation in parentheses which describes which method was used. If no notation appears, the value was measured. Each notation has the following meaning:

(SA) Simulated by the referenced authors.

(CA) Calculated by the referenced authors.

(CP) Calculated by the parallel plane geometry from Chapter 2.

(CC) Calculated by the concentric spheres geometry from Chapter 2.

Additionally, the abbreviations Si for silicon, W for tungsten, Mo for molybdenum, Ref. for author reference and

NA for not available are used. In the cases where more than one set of results was reported, a set of values is given that relate horizontally across the table.

Table 3.1 Summary of electrical and geometric results.

Tip type	Ref.	β (cm^{-1}) x10^5	β'	Max. V	Max. I at Max. V	Max. I per tip
Si	[23]	2.19 (CP)	110 (CP)	150 V	100 nA	100 nA
		2.19 (CC)	55 (CC)			
Si	[14]	1.04 (CP)	9.6 (CP)	18.5 V	8 mA	350 nA
		NA	47 (SA)			
		NA	300 (SA)	13 V	10 mA	440 nA
W on Si	[25]	3.2 (CA)	510 (CA)	330 V	32 μA	12.8nA
		0.72 (CA)	480 (CA)	1000 V	1 μA	0.4 nA
		1.4 (CP)	100 (CA)	600 V	8 μA	3.2 nA
Mo	[43]	5.9 (CP)	NA	110 V	100 mA	10 μA
		NA	NA	NA	8 mA	500 μA

CHAPTER 4

FABRICATION OF SILICON FIELD EMITTER ARRAYS BY ELECTRON BEAM EVAPORATION

4.1 Introduction

While the process of fabricating conical field emitters by the use of electron beam evaporation is not novel [11,40], the use of silicon as the evaporated material is [60,77,78]. Details of a diode fabrication process pertaining to the final design, including problems encountered, will be given in this chapter in addition to the specification of relevant physical data. The final design was preceded by a process development phase which concentrated on the cone formation without the aluminum sacrificial layer.

4.2 Mask development

The fabrication process employed the use of a 3 mask set originally designed and fabricated as a part of this work. Mask 1 consisted of defining an array of squares, 1.2 μm on each side, on 14 μm spacings. Due to the feature size limit of the mask producer, the 1.2 μm squares actually turned out to be circles with a diameter of 1.2 μm, which was desired. Each array is composed of 40 columns and 50 rows for a total of 2000 squares per array. Each array is on

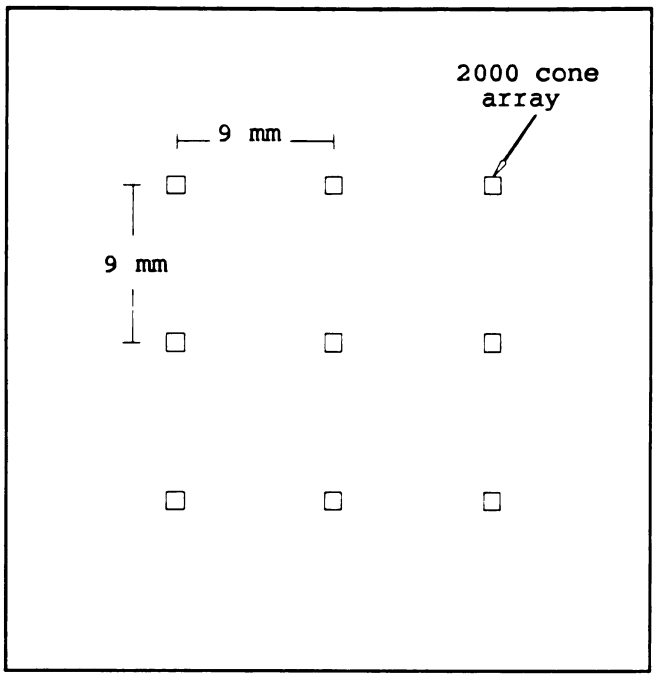

Figure 4.1 Mask 1; spacing between arrays.

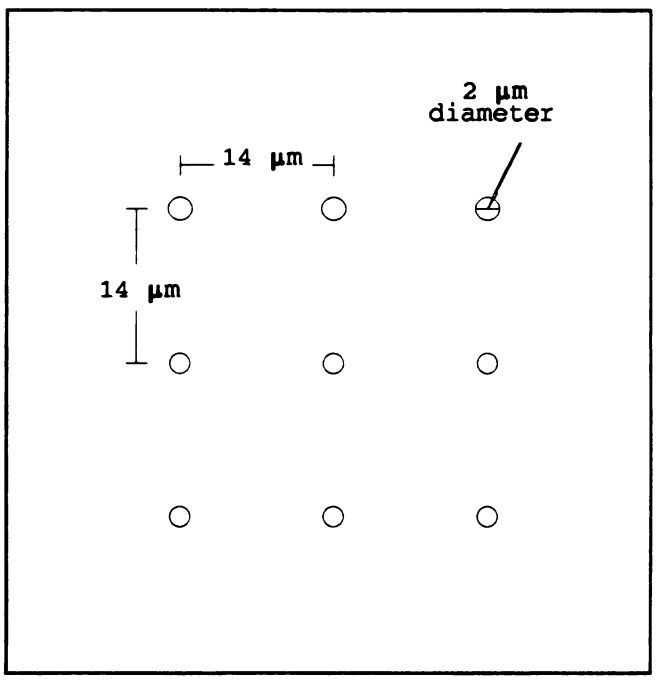

Figure 4.2 Mask 1; spacing for cone holes within an array.

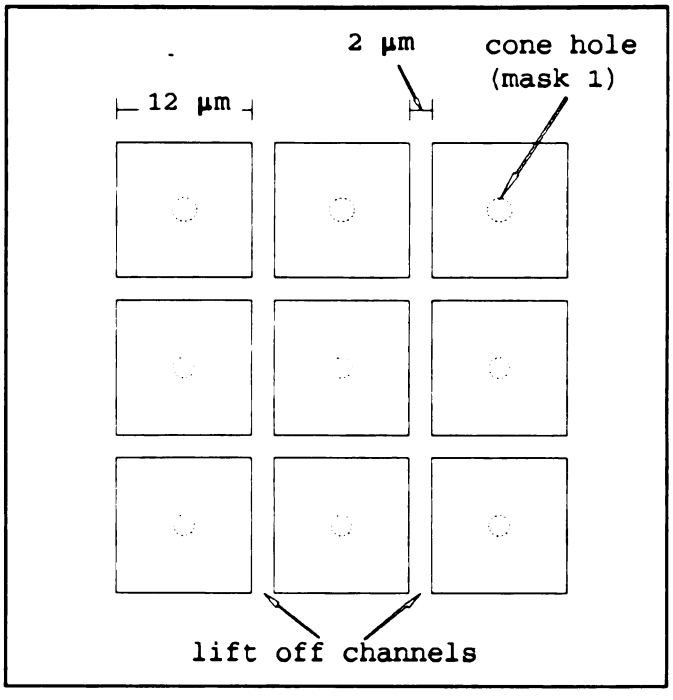

Figure 4.3 Mask 2; lift off channels between cone regions.

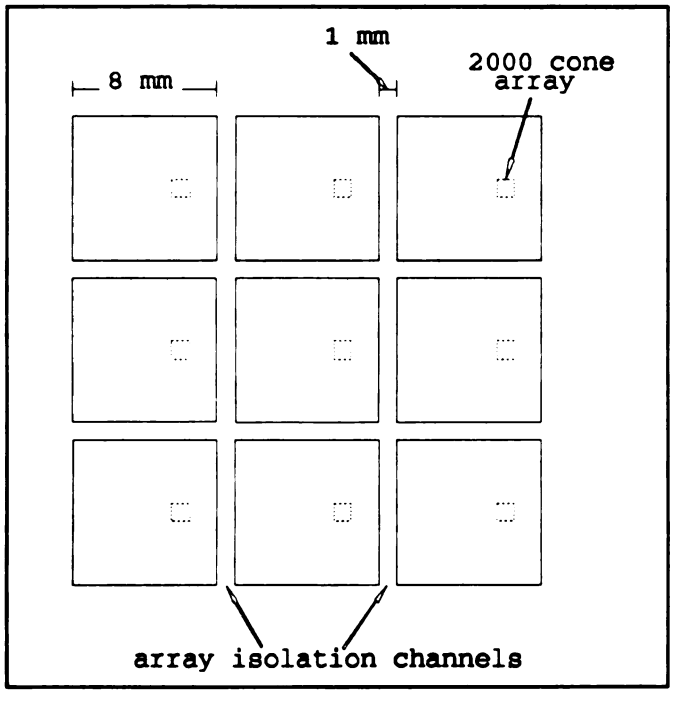

Figure 4.4 Mask 3; array isolation channels.

a 9 mm spacing. Figure 4.1 shows the spacing between arrays on mask 1 and Figure 4.2 shows a close up of a portion of one such array from mask 1.

Mask 2 was designed to provide the lift off channels between each element in each 2000 cone array. The lift off channels, to be described in section 4.3, are 2 μm wide and are concentric with the 1.2 μm diameter circles of mask 1. Figure 4.3 shows a close up of a portion of one such array using solid lines to denote mask 2 and dashed circles for mask 1.

Mask 3 defines the 1 mm wide array isolation channels around each array. The mask was designed so that each 2000 cone array would be near the right edge of the isolated area and centered top to bottom, with the major flat of the wafer at the top. The dimensions are shown in Figure 4.4.

4.3 Fabrication details

The major steps of the fabrication process are shown in Figure 4.5 and will be referred to when appropriate throughout this section. The process leads to a test wafer comprised of 81 arrays. Each array consists of 2000 emitters in a diode configuration. Figure 4.5 is drawn roughly to scale with the exception of the substrate. Dimensions of the materials will be given as they are fabricated. For reference, the silicon dioxide layer is 2 μm thick.

The process utilized 0.01-0.02 Ω-cm, n-type, phosphorous doped, <100> orientation, 4 inch silicon wafers.

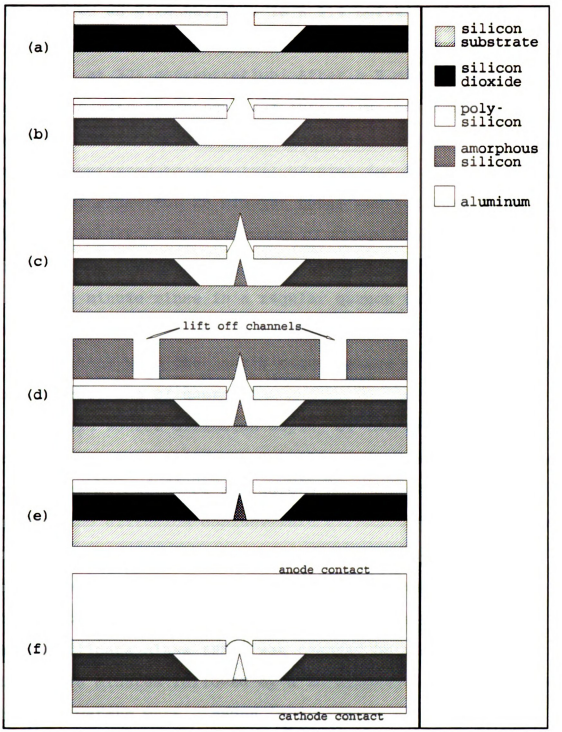

Figure 4.5 Major steps of the fabrication process.

Before the wafers were loaded into the phosphorous diffusion furnace they were cleaned for 20 minutes in a solution referred to as piranha. This is a 1:1 solution of H_2SO_4 (sulfuric acid) at 50% concentration and H_2O_2 (hydrogen peroxide) at 30% concentration. After a 5 minute DI rinse, the wafers were submersed in a 10:1 solution of deionized water (DI) and HF (hydrofluoric acid) at 50% concentration, commonly referred to as a 10:1 HF dip, for 1 minute. A cascade DI rinse for 25 minutes total was followed by a 4 minute spin dry in N_2. A cascade DI rinse involves rinsing the wafers in successively purer tanks of DI. This begins with a 10 minute rinse in a regular quench tank then 5 minutes each in a series of 3 tanks that cascade into the previous tank with the last 5 minute rinse occurring in the tank nearest the DI source.

Solid source diffusion doping of the wafers with phosphorous was carried out for 120 minutes at 1020° C. The subsequent oxidation of the wafers served as the drive in part of the diffusion doping. This diffusion doping provided for a degenerate level of doping on the silicon surface where the evaporated cone would eventually rest.

Before the actual oxidation of the wafers, phosphosilicate glass (PSG) was removed by using a 1:1 HF dip for 10 minutes followed by a 20 minute cascade DI rinse. Then the wafers were cleaned in a piranha solution for 20 minutes and a cascade rinse for 20 minutes. After a 4 minute spin dry in N_2 the wafers were ready for the oxidation

process. Oxidation to a thickness of 2 μm involved a process which included a dry oxidation for 15 minutes at 1100° C followed by a wet oxidation for 8.5 hours also at 1100° C. While still in the furnace, a N_2 anneal for 30 minutes at 1100° C was followed by an O_2 anneal for 30 seconds. The purpose of the O_2 anneal was to reduce the electron and hole traps caused during the oxidation process and subsequent N_2 anneal, and to improve the breakdown behavior of the SiO_2 [58].

The next step in the process was the low pressure chemical vapor deposition (LPCVD) of polysilicon formed by the pyrolytic decomposition of SiH_4 (silane) gas [59]. Before the deposition, the wafers were again cleaned in piranha for 20 minutes, dipped in a 10:1 HF dip for 10 seconds, cascade rinsed for 20 minutes and spun dry in N_2. Approximately 1 μm of polysilicon was deposited at 600° C and a pressure of 310 mTorr over a period of 2 hours and 35 minutes. An anneal for 60 minutes at 1050° C in N_2 was carried out to relieve any residual strain present in the polysilicon [56].

At this point the wafers were ready for the first lithographic procedure using mask 1. Before application of the Shipley MP-1470J positive photoresist, the wafers were treated in a vapor prime of hexamethyldisilazane (HMDS). This dried up any residual moisture on the wafers promoting better adhesion of the photoresist given that the photoresist is hydrophobic. 1.2 μm of photoresist was applied using a Multifab resist spinner (Machine Technology

Incorporated). For this thickness, a spin speed of 5000 rpm for 20 seconds was needed. After the application of the photoresist, the Multifab was also instructed to place the wafers on a 100° C hot plate for 45 seconds which is equivalent to a soft bake for half an hour at 90° C. Ultraviolet (UV) lithography was employed utilizing a Cannon PLA501F contact/proximity mask aligner in the soft contact mode for exposure using mask 1. The light integral was set at 4.4 seconds for a light intensity of 13.5 mW/cm^2. The wafers were then placed in a developer, made by KTI and consisting of approximately 5% tetramethylammonium and 95% DI which was then mixed 1:1 with DI, for 1 minute followed by a 10 minute DI quench and N_2 spin dry. To harden the photoresist in preparation for use as the masking material for the subsequent dry etch of polysilicon, the wafers were hard baked in an oven at 120° C for 30 minutes.

Inspection by use of the Vickers image shearing microscope showed the circular holes in the photoresist to be approximately 2.0 μm in diameter. The increase in hole diameter over the mask 1 dimensions was anticipated due to results from developmental experiments with regard to the light integral of exposure. In those experiments it was found that the diameter of the hole in the photoresist could be varied with the light integral so that the height of the cone could be controlled as shown later in this section.

A highly anisotropic dry etch of polysilicon was carried out using the Dry Tek 284 plasma etch system. This

procedure utilized RF plasma consisting of 50 sccm SF_6 and 50 sccm $CClF_3$ at 150 mTorr and 130 W which provided an etch rate of 0.2 μm/min on the average. The etch time was 5.5 minutes to insure complete etching of the polysilicon layer. This slight over etch was necessary since there existed a variation in etch rate decreasing in magnitude from a peak at the center of the wafer to a low at its periphery. Vertical side walls were realized with some lateral etching of the polysilicon at the oxide surface noted where the over etch occurred. At this time a dry etch of polysilicon was also performed on the back of the wafers for 6 minutes to expose the silicon dioxide there for subsequent removal.

Since the photoresist is quite hard at this point due to the previous hard bake and the dry etch, conventional resist stripper proved ineffective for complete removal of the photoresist. A piranha solution was used to remove the photoresist and took approximately 30 minutes. After a 10 minute DI quench and spin dry in N_2 the wafers were inspected using the Vickers microscope. 2.0 μm circular holes were noted in the polysilicon.

A wet buffered oxide etch consisting of 7:1:1 ammonium hydroxide/HF/DI was used to etch the silicon dioxide through the circular openings in the polysilicon. The etch is isotropic and undercuts the polysilicon as it etches through to the silicon substrate with an etch rate of approximately 700 Å/min. Etch time was 36 minutes which constitutes an over etch of approximately 5000 Å to ensure a clean seat for

the cones. This etch time was also sufficient to remove the silicon dioxide from the back of the wafers exposing the silicon wafer surface. The structure at this point is shown schematically in Figure 4.5(a) with the noted difference that the silicon dioxide walls are in reality curved not straight as shown.

Prior to the deposition of the sacrificial layer of aluminum, the wafers were cleaned in a piranha solution for 20 minutes, quenched in DI for 10 minutes and spun dry in N_2. Using a process reported elsewhere [11,40], a sacrificial layer of aluminum was deposited by electron beam evaporation. The wafer was first mounted on a motor assembly in the vacuum chamber of a Temescal BJD-1800 electron beam deposition system, 25 cm from the source and rotated about an axis normal to its surface at a rate of 4 rpm. The aluminum was deposited at a grazing incidence angle of 75° to the surface normal at 25° C and a pressure of 10^{-6} Torr. The evaporation rate was varied from 1 to 20 Å/sec on different wafers with the smoother layer obtained using the lowest rate. Even at the lowest rate, the evaporated aluminum was found to be grainy in composition. This would prove to be one of the more significant problems encountered and is addressed later in section 4.4. The grain size varied with evaporation rate increasing from approximately 3000 Å at 1 Å/sec to a few microns at 20 Å/sec. The cone height h is directly proportional to the hole diameter d_h by the equation $h = (1.6)d_h$, which was found experimentally. Since

the desired cone height was 1.9 - 2.0 μm, a 4000 Å thick layer was deposited at a rate of 1 Å/sec. It is noteworthy that at this particular angle of evaporation the hole radius decreased at the same rate as the thickness increased normal to the wafer surface. In previous experiments it was found that a 4000 Å thick layer of aluminum was the minimum thickness acceptable for effective use as a sacrificial layer, due in part to its grainy structure. The structure now has the form shown schematically in Figure 4.5(b) with a hole diameter of approximately 1.2 μm in the aluminum layer. Using the scanning electron microscope (SEM), a cross sectional view of the actual structure is shown in Figure 4.6.

In an attempt to preserve the cleanliness of the wafer prior to the cone deposition, the wafer was not removed from the vacuum chamber. The chamber was opened briefly to remount the wafer with the silicon source at a distance of 30 cm and normal to the wafer surface. A constant flow of N_2 was supplied to the chamber during this time. Cone formation by normal incidence electron beam evaporation through a decreasing aperture [11,40] was attained using crushed silicon wafers as the source material. The source wafers were originally phosphorous doped to a concentration of $5x10^{15}$ cm^{-3}.

Preceding evaporation, the chamber was reduced to a background pressure of $7x10^{-7}$ Torr and purged with N_2 numerous times to approach a more inert environment. The

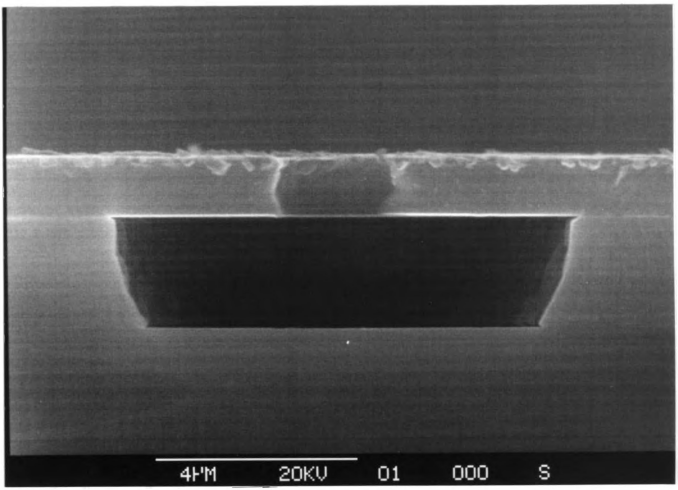

Figure 4.6 Cross sectional SEM showing aluminum sacrificial layer.

temperature was raised to 200° C for 2 hours prior to evaporation. Evaporation occurred at a pressure of 10^{-6} Torr and temperature of 200° C with the evaporation rate set at 3 Å/sec. The thickness was set at 2.5 μm to insure complete formation of the cones. The structure is shown schematically in Figure 4.5(c) and by SEM in Figure 4.7. From Figure 4.7 the conical tip is seen to have a height of approximately 1.9 μm with a tip radius between 350 and 500 Å as estimated from the SEM shown in Figure 4.8.

The as deposited silicon has an amorphous structure [55,57]. Resistance tests showed the doping concentration of the evaporated silicon to be on the order of 10^{11} cm^{-3} showing a loss of dopant during evaporation. This can be attributed to the greatly different partial pressures and melting points of phosphorous and silicon [61].

In preparation for the lithographic procedure using mask 2, the wafers were treated in a vapor prime of HMDS. The application of the photoresist, UV exposure and development were the same as for mask 1 with the exception that a light integral of 3.0 seconds was used for mask 2 since overexposure was not appropriate here.

Inspection of the photoresist using the Vickers microscope showed acceptable alignment of mask 2. The lift off channels were found to be approximately 2.0 μm wide and in agreement with mask 2 dimensions. Furthermore, complete coating of the area where the cone opening finally closes was noted. This was found to be a trouble spot on some

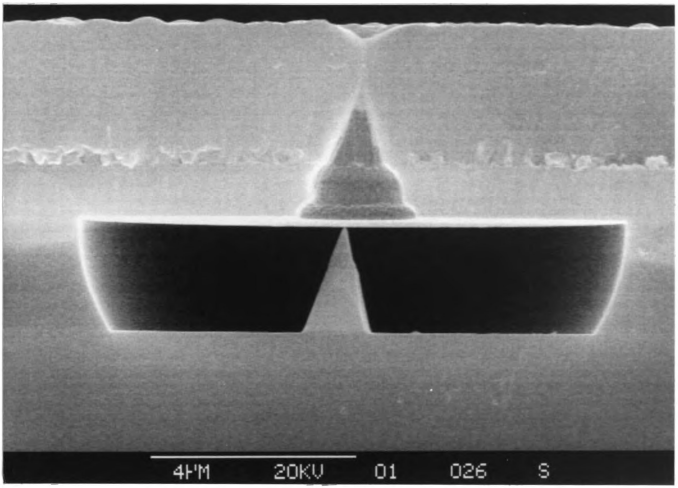

Figure 4.7 Cross sectional SEM showing evaporated silicon cone.

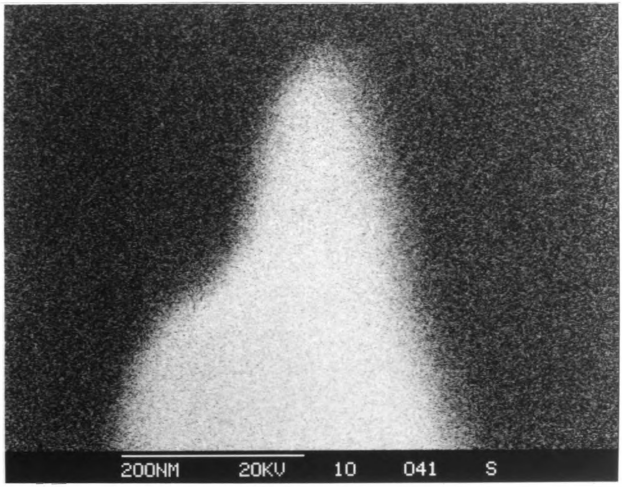

Figure 4.8 SEM close-up of silicon emitter tip.

wafers. It was noted that submicron facets formed on the top of the evaporated silicon layer above the cone holes as the hole closed during evaporation. This gave rise to problems with adherence of the photoresist there even after the wafers were treated in a vapor prime of HMDS.

Prior to a dry etch of the evaporated amorphous silicon layer, a hard bake of the photoresist was needed again. The amorphous silicon dry etch used the same device and parameters as for the polysilicon dry etch. The etch time was lengthened to 12.5 minutes to account for the 2.5 μm thickness of the silicon layer to be etched and an etch rate of approximately 0.24 μm/min for the amorphous film. An over etch was used again to compensate for the lack of uniformity of the etch noted earlier. This was done to insure that the aluminum sacrificial layer was exposed in all channels. The structure is shown schematically in Figure 4.5(d). Areas of the wafer which are not part of an array are etched completely down to the aluminum layer.

For the aluminum sacrificial layer etch, which leads to lift off of the amorphous silicon layer above each cone, a piranha solution was chosen due to the violent attack it exhibits on aluminum. Since the thickness of the aluminum is only 4000 Å and the undercut necessary is roughly 5 μm the total time required for the wafers to be in the piranha was found to be longer than one treatment usually lasts. Typically, 2 consecutive treatments of 30 minutes each were needed to complete this step. Figure 4.5(e) shows the

schematic of the structure after lift off has occurred. Figure 4.9 shows a SEM which depicts the polysilicon surface of a portion of one array at this time. Numerous cone well openings in the polysilicon can be seen. The SEM in Figure 4.10 shows a closer view of one of the cones through the 2.0 μm opening in the polysilicon. A cross sectional view of a sample, prepared during an earlier process development phase, that exhibits the structure at this stage is shown by SEM in Figure 4.11.

For the lithographic step using mask 3, a thicker photoresist was needed to completely cover and partially fill the 2.0 μm holes in the polysilicon layer and, hence, protect the cones which are now exposed through these holes from the upcoming polysilicon dry etch. Prior to application of the Shipley MP-1450 positive photoresist, the wafers were treated in a HMDS vapor prime. 2.2 μm of photoresist was applied. The spin speed sequence used consisted of 500 rpm for 20 seconds, where application of the photoresist occurred, a 20 second stop to allow the resist to seep into the cone wells through the circular openings in the polysilicon, and a final 20 second spin at 3000 rpm to thin the photoresist to the desired thickness. After a soft bake using the Multifab hot plate, the wafers were exposed in the same manner described earlier using mask 3 and a light integral of 10.0 seconds at the same light intensity. Following a 1 minute treatment in the developer, 10 minute quench in DI and spin dry in N_2, the wafers were inspected

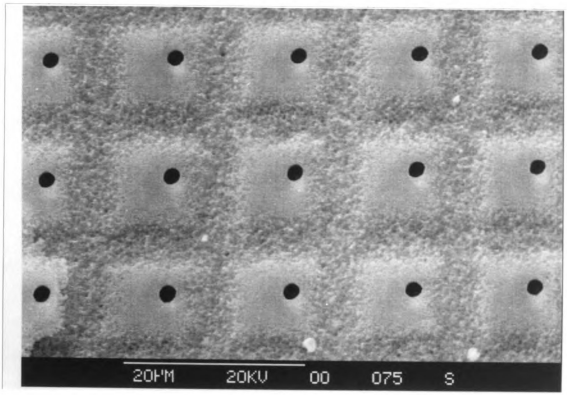

Figure 4.9 SEM of array site after aluminum sacrificial layer etch and lift off.

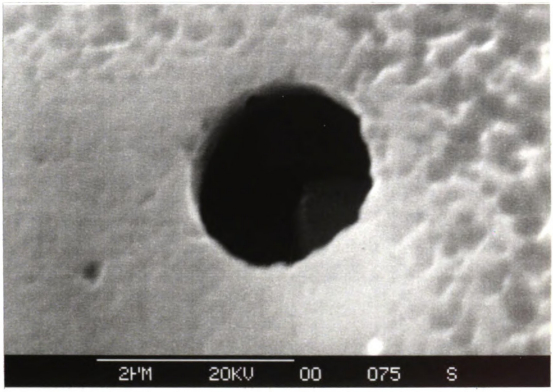

Figure 4.10 SEM close-up of one cone and cone hole after aluminum sacrificial layer etch and lift off.

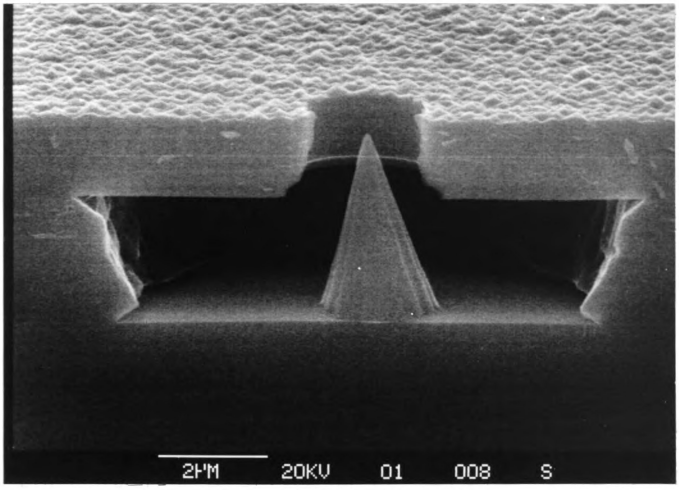

Figure 4.11 Cross sectional SEM of an earlier sample.

optically. Acceptable mask alignment was noted with good definition of the 1 mm wide array isolation channels. Additionally, all cone well openings were seen to be completely covered and closed by the photoresist.

In preparation for the polysilicon dry etch, the wafers were hard baked at 120° C for 30 minutes. The polysilicon layer dry etch was performed in the same manner as described earlier. Inspection using the microscope showed the array isolation channels to be well defined in the polysilicon layer and completely etched down to the silicon dioxide layer. Also, all cone well openings were still completely covered indicating that the cones were not affected by the dry etch procedure.

The photoresist was stripped in a piranha solution for 30 minutes after which the wafers were quenched in DI for 10 minutes and spun dry in N_2.

Since the polysilicon layer is not doped and the as evaporated amorphous silicon cones are lightly doped, a diffusion doping with phosphorous was deemed appropriate. Additionally, due to the high temperatures used during the following diffusion doping process, the amorphous cones were converted to strain free polysilicon in structure [55,56,57].

Prior to the phosphorous predeposition and between the predeposition step and the drive in step, the wafers were cleaned in a solution of piranha for 10 minutes and received a 10:1 HF dip for 10 seconds followed by a 25 minute cascade

DI rinse and N_2 spin dry. The solid source phosphorous diffusion predeposition step was carried out at 950° C for 6 hours with a N_2 flow rate of 3000 sccm. The phosphorous drive in occurred at 1050° C for a period of 1.5 hours with an N_2 flow rate of 1500 sccm.

The final phosphorous doping concentration profiles are shown in Figure 4.12 for the cone, Figure 4.13 for the polysilicon anode layer, and Figure 4.14 for the back of the wafer. These profiles were obtained from SUPREM simulation results of all steps of the fabrication process which affected the doping levels.

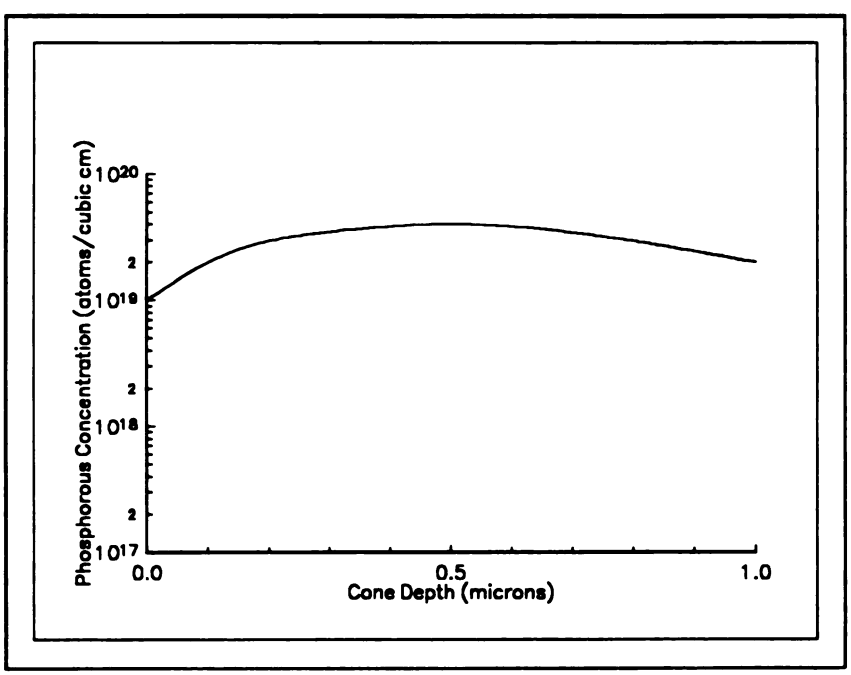

Figure 4.12 Doping concentration profile for the cone emitter.

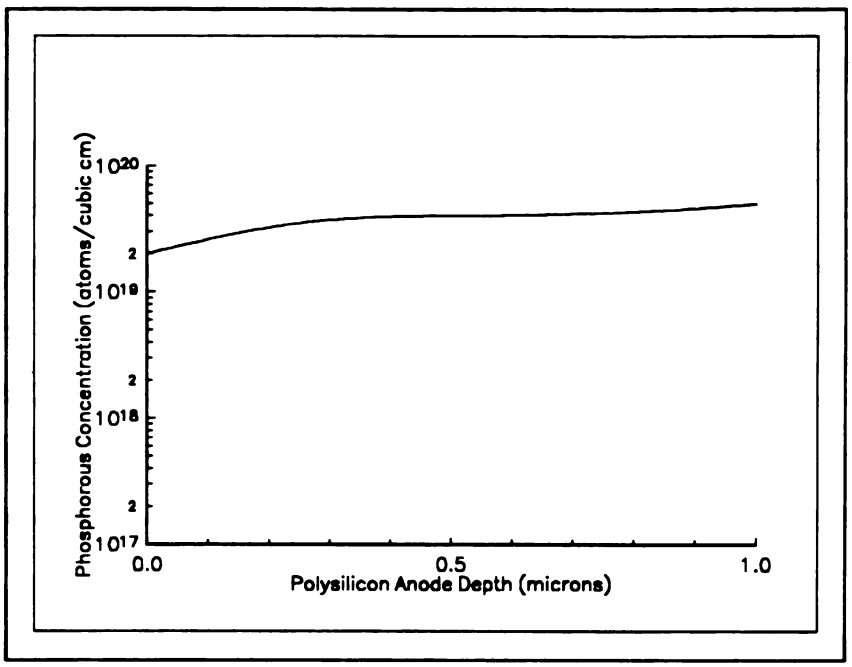

Figure 4.13 Doping concentration profile for the polysilicon anode layer.

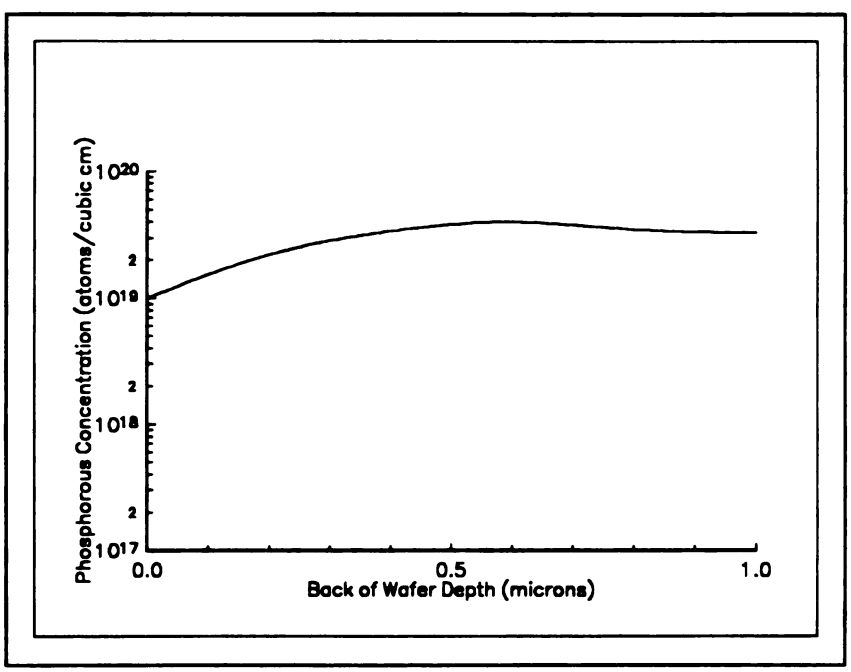

Figure 4.14 Doping concentration profile for the back of the wafer.

Taking note of the phosphorous concentrations at all three surfaces it is seen that $\epsilon_f \approx \epsilon_c$ [24] where ϵ_f is the Fermi energy level of electrons in the silicon and ϵ_c is the respective conduction band edge. This would provide for an ohmic contact on the back of the wafer between the silicon substrate and the aluminum anode contact when the aluminum was finally deposited there. Also, the doping level of the conical emitters partially supports the assumption that the emitters can be treated as metallic as discussed in Chapter 2.

Following a PSG removal by use of a 2 minute 1:1 HF dip and 10 minute DI quench, the wafers were cleaned in a piranha solution, quenched for 10 minutes in DI and spun dry in N_2 in preparation for the grazing incidence angle aluminum evaporation to form the complete anode.

The wafers were loaded into the electron beam evaporator in the same manner as described for the aluminum sacrificial layer deposition. The evaporator chamber was backfilled numerous times with N_2 and pumped down overnight to a pressure of 6×10^{-7} Torr, which was the initial evaporation pressure. Due to heat generated by the evaporation of the source material and the presence of the motor assembly in the chamber, a temperature rise in the chamber from an initial reading of 25° C to a final value of 80° C was noted and the final pressure was seen to be 4×10^{-6} Torr. The evaporation rate was set at 1 Å/sec for the first 1 μm of the layer to minimize the grainy structure of the

aluminum closest to the cone cathode. This was done with the anticipation that the aluminum layer, which completely covers the cone hole at about 1 μm of thickness, could maintain a vacuum in the cone well equal to the chamber pressure at the time of closure. Later, during testing, it was realized that this was not the case. The last 4 μm were deposited at 20 Å/sec for a total thickness of 5 μm.

A final lithographic step was needed to redefine the isolation channels that had been covered with aluminum. The thicker MP-1450 photoresist was applied with the same spin speed sequence noted in its first use. This was done to accommodate the grainy aluminum surface. UV exposure, developing and soft bake were carried out as before using mask 3. The light integral used in this step was set at 7.0 seconds for the given light intensity.

An aluminum etch developed by KTI and consisting of 5% acetic, 80% phosphoric and 10% nitric acids mixed with 10% water, was used to define the array isolation channels in the aluminum anode. Total time needed in the 65° heated etch was found to be approximately 30 minutes.

After stripping the photoresist for 20 minutes in KTI S-43 resist stripper composed of 96% sulfuric acid, 2% hydrogen peroxide and some stabilizers, the wafers were quenched in DI for 10 minutes and spun dry in N_2. Inspection by using the Vickers microscope showed that the etch was complete and the isolation channels were well defined.

The final step in the design was the electron beam

evaporation of the aluminum cathode contact on the back of the wafer. The final film thickness was 3000 Å and was obtained with an evaporation rate of 15 Å/sec, a pressure of $2x10^{-6}$ Torr and temperature of 30° C. Figure 4.5(f) shows a schematic of the final structure which includes both the aluminum anode and aluminum cathode contacts. The SEM's in Figure 4.15 and Figure 4.16 show the completed structure and are discussed in the following section. The array isolation channels, which do not have the aluminum or polysilicon anode layers, are not shown.

4.4 Completed structure and associated problems

Figure 4.15 shows a SEM of the cross sectional view of the completed structure. From this angle, the grainy composition of the aluminum deposited by electron beam evaporation at a grazing incidence angle is quite obvious. The grain size is noticeably smaller at the polysilicon surface where the rate of evaporation was 1 Å/sec than near the top of the aluminum layer where the evaporation rate was 20 Å/sec. The grainy structure of the aluminum did not maintain the vacuum in the cone wells as evidenced by characteristics noted during electrical testing reported in Chapter 5. However, this layer still provided the anode of the diode structure dispensing with the need for small scale electrical test probing of the emitter tips.

As a solution to the problem of the grainy aluminum layer, it is suggested that different materials be tried as

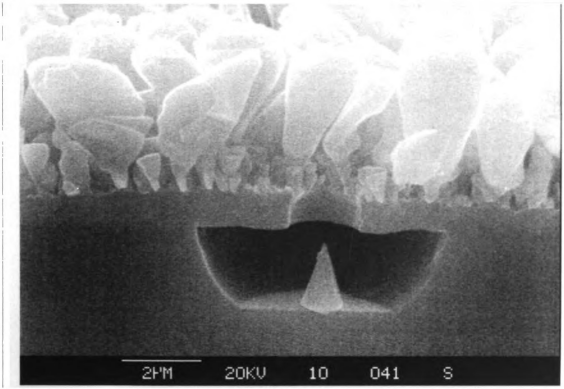

Figure 4.15 Cross sectional SEM of complete structure showing grainy aluminum.

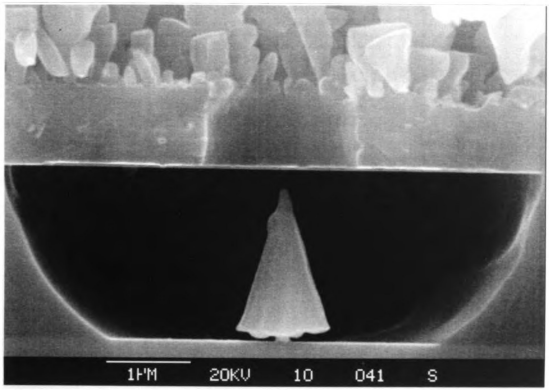

Figure 4.16 Cross sectional SEM of complete structure showing cone seating.

the sacrificial layer. Possible materials could include Al_2O_3 as reported elsewhere [40], which can be deposited by electron beam evaporation, or other metals whose respective etchants have little effect on silicon and silicon dioxide.

Figure 4.16 shows a cross sectional view taken at 90° to the wafer surface normal. From this angle it is obvious that the evaporated cones are not well seated. It appears that the base of the cone has been etched away in some manner during the processing steps that followed cone formation. Since most of the solutions used have very little effect on pure silicon, it is assumed that the base of the cones is not pure silicon. It has been reported elsewhere [55] that evidence of inclusions in electron beam evaporated silicon films were found to include SiON, Si_3N_4 (silicon nitride) and SiO_2 (silicon dioxide). The latter is readily etched in any of the HF dips that were used after cone formation.

Since only the first 1000 Å or so of the cone base has been etched away and not the whole cone, it seems reasonable to assume that the majority of the inclusions in the amorphous silicon cone are contained there. The most likely source of the impurities which could cause these inclusions would be the initial vacuum chamber environment. It is suggested that a secondary shutter be placed close to the target wafer. During the first few thousand angstroms of silicon evaporation with the primary shutter near the source open, the secondary shutter would remain closed and shield

the target wafer from the evaporated material. After this initial period, the secondary shutter would be opened and cone formation would take place. If the evaporated silicon did combine to form the materials listed above by bonding with residual gasses in the initial vacuum chamber environment, then this should prove to be a sufficient test to verify it.

CHAPTER 5

ELECTRICAL CHARACTERIZATION AND ASSOCIATED GEOMETRIC PARAMETERS OF EVAPORATED SILICON FIELD EMITTER ARRAYS

5.1 Introduction

One of the main intents of the work presented in this thesis was to show that field emission was the primary source of measured current from the silicon field emitter arrays fabricated as described in Chapter 4. As noted in Chapter 2, the most widely accepted way of proving field emission is to produce the straight line Fowler-Nordheim plots with respect to equation (2.28) and the subsequent discussion.

In this chapter, it will be shown that the silicon emitters presented in this thesis do produce straight line Fowler-Nordheim plots. Three separate stages of testing are described and the various results are given. In addition, a summary of the electrical test results and the geometric parameters referred to in Chapter 2 will be compiled in section 5.5.

5.2 Initial electrical testing

As a prelude to electrical testing, the breakdown field of the insulating silicon dioxide layer is considered. As it will be shown later in this chapter, the maximum voltage

applied to the emitter arrays was 140 V. With a 2 μm thick silicon dioxide layer, this shows that the maximum field across the oxide was on the order of 0.7 MV/cm. It has been reported [24,80] that a maximum oxide breakdown field of 10^7 V/cm can exist for an ideal oxide. It has been shown by experiment [79] that for thicker oxides a breakdown field greater than $3x10^6$ V/cm can be assumed. The oxide tested was approximately 450 Å For a dry oxide that has been exposed to an O_2 anneal [58], the oxide breakdown field was found experimentally to be about $5x10^6$ V/cm. It is seen that even the most conservative of these reported values is more than 4 times the electric field that was placed across the oxide insulating layer of the device presented here. This, in addition to the fact that a permanent rise in measured current was not noted during testing, supports the assumption that the current measured during emitter array testing was not due to oxide breakdown.

During the final stages of fabrication of the emitter arrays, it was hoped that the closure of the cone wells by the incident angle evaporation of the aluminum anode would maintain the vacuum present in the evaporation chamber at the time of closure. Therefore, initial testing of the arrays was carried out without the use of a vacuum test chamber.

The test setup consisted of placing the wafer on a metal wafer pedestal in a metal shielded enclosure. The pedestal was equipped with a vacuum attachment which held

the wafer in place during testing, similar to a wafer probe station. Cathode contact was made through the pedestal to the aluminum cathode contact on the back of the wafer. Anode contact was made by use of a wafer probe station micromanipulator. A 300 V DC power source in series with a Keithely 595 Quasistatic CV Meter was connected across the diode emitter array. The Keithely meter was used in the current mode and has the capability of measuring femtoamps under the right shielding conditions. It was not possible to provide this type of shielding for the test setup at hand. Consequently, tens of picoamps was the lowest discernable current possible. All cables were shielded with the exception of the ground return path to the power source. A digital multimeter was used to monitor the applied voltage and was connected in parallel directly across the DC power source.

With a negative potential applied to the cathode contact and the anode contact held at ground, numerous arrays were tested. Applied voltages ranged in magnitude from 0 V to 150 V. The diode emitter arrays were seen to catastrophically fail at applied voltages greater that approximately 150 V in magnitude. Figure 5.1 shows a SEM of a portion of one such array.

The results of initial testing in this manner were completely inconclusive with respect to electrical characterization. The current measured varied from tens of picoamps to microamps in a manner such that no average could

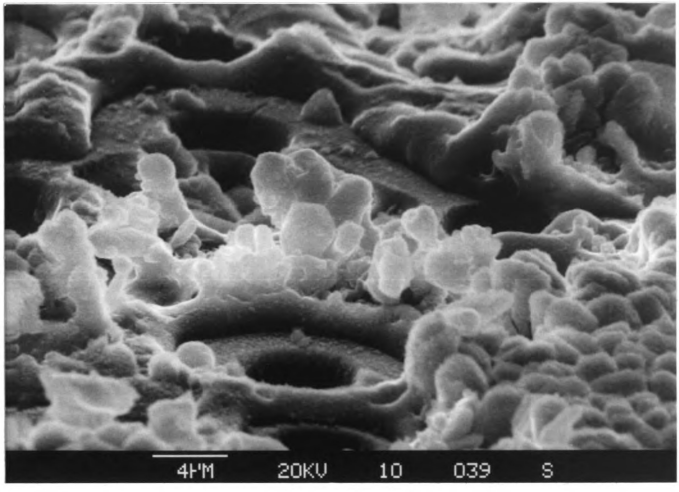

Figure 5.1 SEM of array site after catastrophic failure.

be deduced from the readings. Even after allowing the arrays to operate at various constant applied voltages for hours in an attempt to reduce current noise [15], the current readings were not stable. For comparison, resistors of various values were substituted for the diode array and stable currents were measured in the tens of picoamps range. This indicated that shielding was not a factor in the range of current that was being seen from the diode arrays. At this point, it was surmised that the cone wells might not be holding the vacuum as was hoped for. It was decided that testing in a vacuum chamber should be performed.

5.3 Vacuum chamber electrical testing using a warm up stage

The test setup used in this situation was as described in section 5.2 with a few exceptions. All cables were shielded and the wafer was mounted in a metal vacuum test chamber. The wafer was held to a metal base plate by a screw down clip. Contact to the cathode was made through the base plate and contact to the anode was made by a micromanipulator. Access to the vacuum test chamber was achieved using shielded coaxial feed through connectors.

Prior to electrical testing, the vacuum chamber was reduced to a pressure of 7×10^{-7} Torr. The applied voltage was raised slowly to a value of around 130 V to 140 V for the diode array under test and allowed to remain there for about an hour in an attempt to reduce current noise [15]. I refer to this as an initial warm up stage.

Figure 5.2 shows the forward bias and reverse bias I-V characteristics obtained from array 9-4 of the test wafer. The array clearly exhibits the traits of a diode. In forward bias, the measured current ranged from 0.43 μA to 36 μA for an applied voltage range from 80.4 V to 139.0 V respectively. This showed a maximum current of 18.0 nA per emitter at 139.0 V applied, assuming that all the tips were emitting. The reverse bias measurements yielded a current range from 0.07 μA to 0.17 μA for an applied voltage range from 104.1 V to 140.3 V, respectively. As can be seen, the forward bias current is more than two orders of magnitude greater than the reverse bias current at a magnitude of about 140 V applied. Since the reverse bias current is much larger than what can be expected from leakage current through the oxide insulator alone, it is suspected that field emission is occurring in the reverse bias mode also. A possible source of this current would utilize the circular wedge at the bottom of the polysilicon layer, closest to the cone, as the cathode and the cone as the anode.

Figure 5.3 shows the Fowler-Nordheim plot for array 9-4 in the forward bias mode. The graph clearly displays the straight line plot indicative of field emission as described in Chapter 2.

For comparison, results from a second array are presented. The same test conditions were used in electrically characterizing array 9-5. Figure 5.4 shows the forward bias and reverse bias I-V characteristics for array

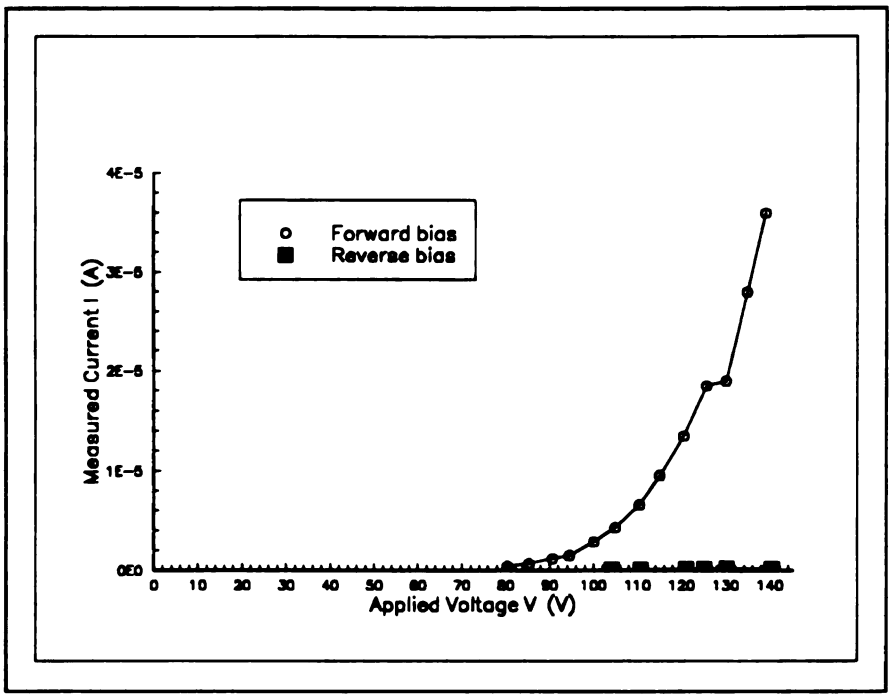

Figure 5.2 I-V characteristics for array 9-4 after an initial warm up stage.

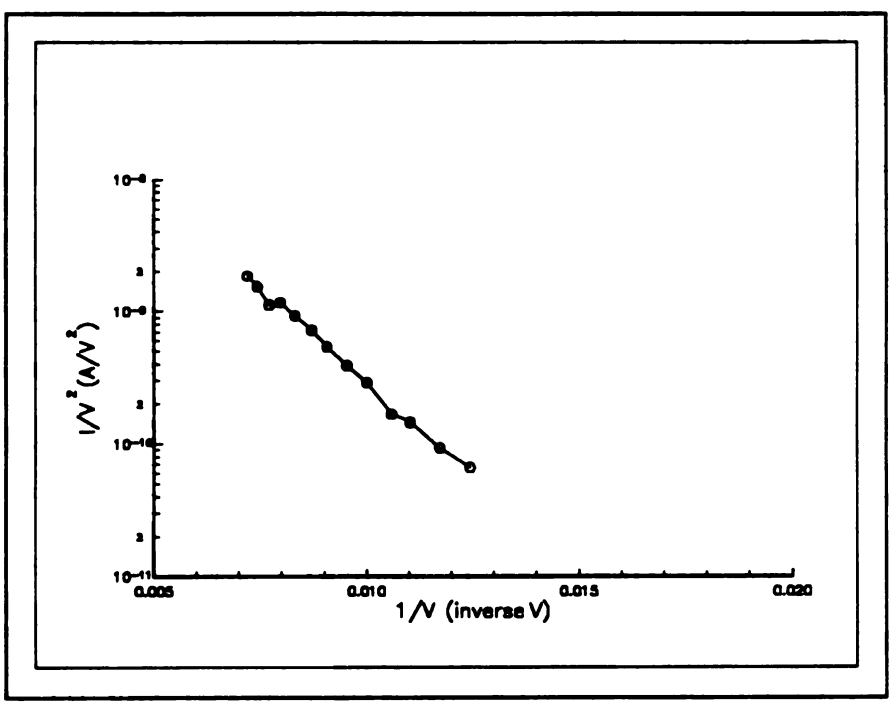

Figure 5.3 Fowler-Nordheim plot for array 9-4 after an initial warm up stage.

9-5. Again, the array exhibited the traits of a diode. In this case the forward biased measured current ranged from 0.18 μA to 25 μA for an applied voltage range from 80.3 V to 135.7 V respectively. This showed a maximum current of 12.5 nA per emitter at 135.7 V applied. The reverse bias measured current ranged from 0.3 μA to 1.4 μA for an applied voltage range from 96.8 V to 139.6 V. While the reverse bias current is an order of magnitude greater for array 9-5 than for array 9-4 it is still an order of magnitude less than the forward bias current measured. This variation in reverse bias current between arrays lends support to the idea that field emission is occurring in the reverse bias mode. It does not seem likely that such a noticeable variation in the silicon dioxide insulating layer capable of causing such a current variation would occur over the distance of 9 mm between the two side by side arrays.

In Figure 5.5 the Fowler-Nordheim plot for array 9-5 is shown. Again, a straight line plot indicative of field emission is noted.

The results presented in this section have shown that the attempted aluminum closure of the polysilicon layer cone hole in the hopes of containing a vacuum inside the cone well failed. This can be seen by the fact that when the wafers were tested in a vacuum the measured currents did stabilize to the point where meaningful data could be taken. Also, the results clearly indicated that field emission by way of Fowler-Nordheim tunneling theory [1] did occur. While

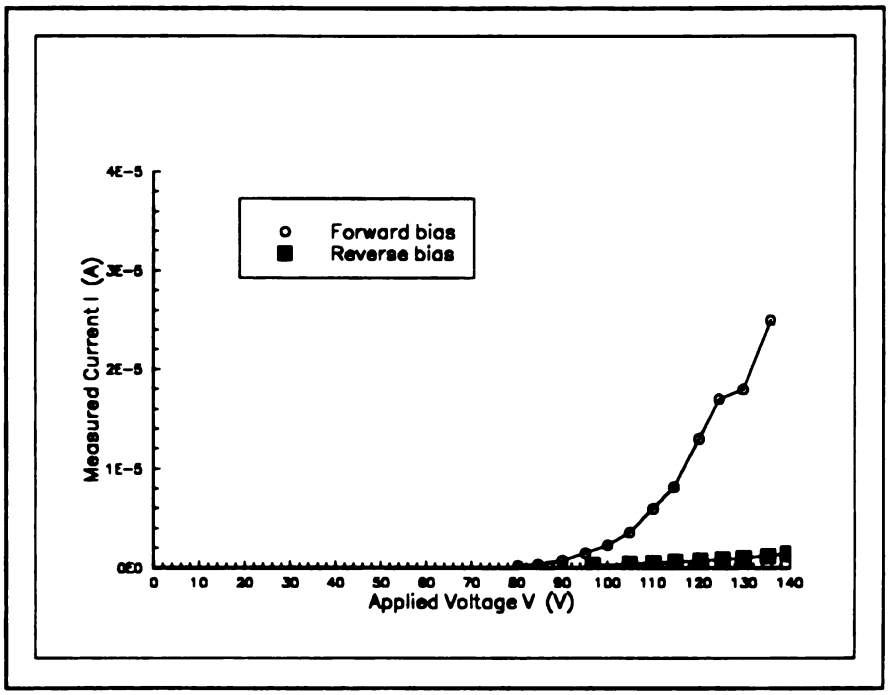

Figure 5.4 I-V characteristics for array 9-5 after an initial warm up stage.

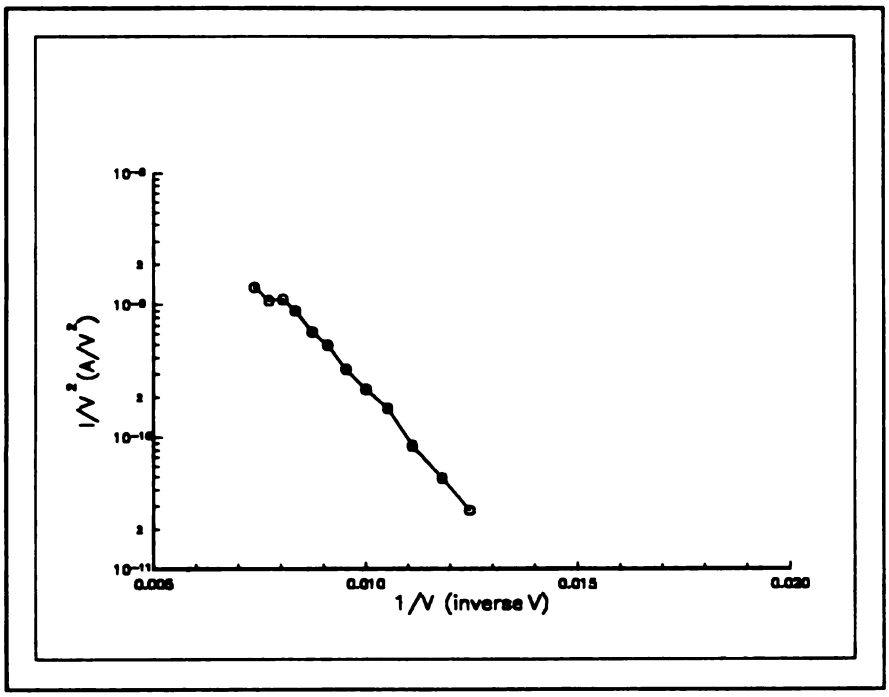

Figure 5.5 Fowler-Nordheim plot for array 9-5 after an initial warm up stage.

reproducible results were obtainable when measurements were made immediately without letting the arrays shut down, later testing showed that permanent damage had occurred to the arrays. Subsequent testing showed reduced currents for the same applied voltages. The next section provides some of the results from these tests.

5.4 Subsequent low current electrical testing

The test setup for this stage of electrical characterization of arrays 9-4 and 9-5 was identical to that described in section 5.3. An initial warm up stage was not used here since the current was already stable at the onset of testing.

Figure 5.6 shows the I-V characteristics for array 9-4 in the forward bias mode. For an applied voltage range from 60.8 V to 100.1 V a measured current range from 0.2 nA to 2.5 nA was noted. This showed a maximum measured current of 1.25 pA per emitter at 100.1 V applied. Since the measured current at about 100 V applied was approximately 3 orders of magnitude less than that seen at the same voltage during the testing reported in section 5.3, it was decided that permanent damage had occurred to the emitter array structure. Thus, higher applied voltages were not used.

Figure 5.7 shows the Fowler-Nordheim plot obtained from the data taken from array 9-4. The straight line plot indicates that field emission is still taking place even at this reduced current level. This could be due to the fact

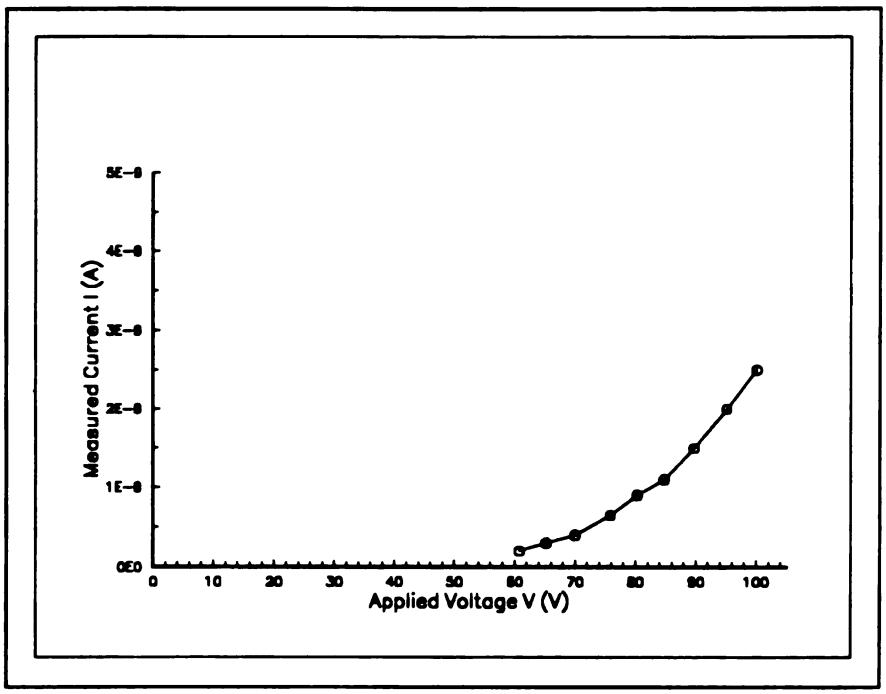

Figure 5.6 Low current I-V characteristics for array 9-4.

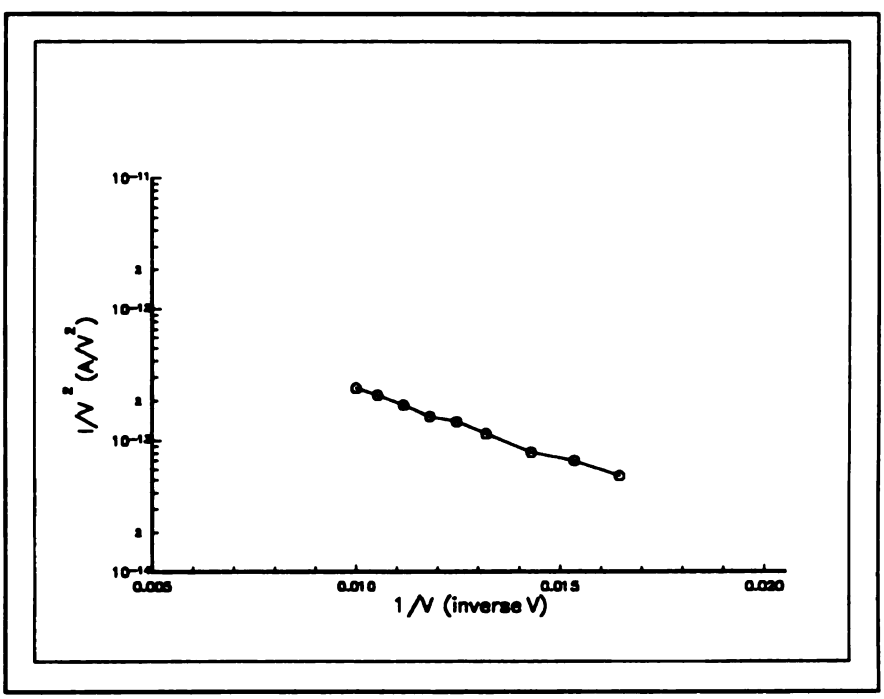

Figure 5.7 Low current Fowler-Nordheim plot for array 9-4.

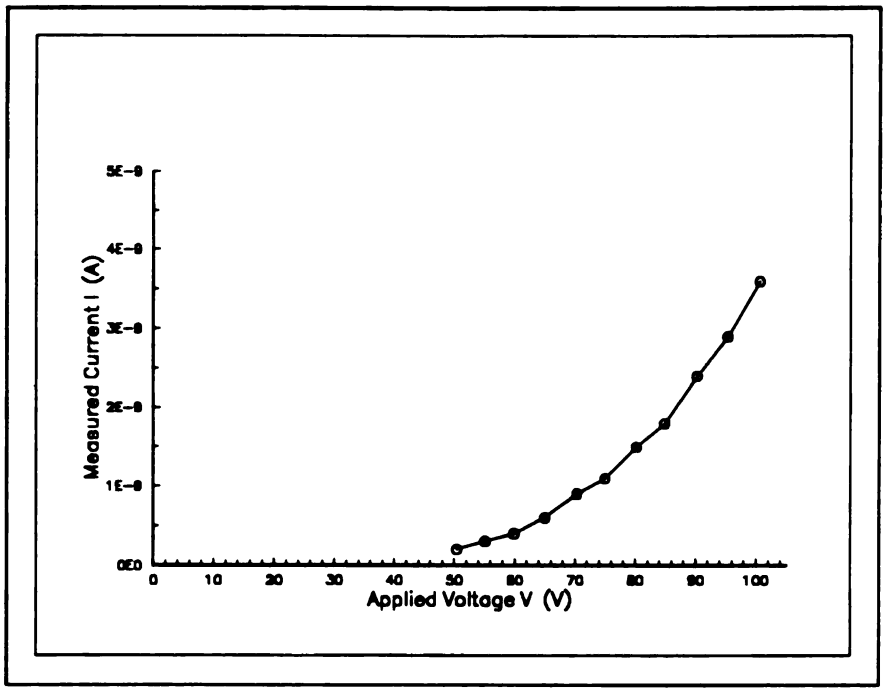

Figure 5.8 Low current I-V characteristics for array 9-5.

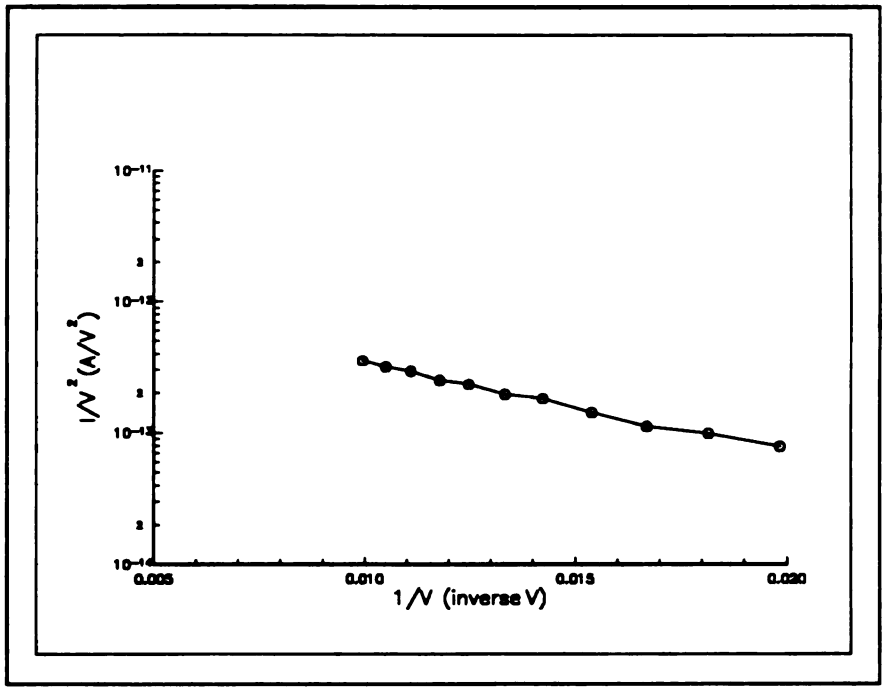

Figure 5.9 Low current Fowler-Nordheim plot for array 9-5.

that not all emitters in the arrays tested have failed and will be discussed in the following section.

Figure 5.8 shows the I-V characteristics for array 9-5 in the forward bias mode. For an applied voltage range from 50.4 V to 100.6 V a measured current range from 0.2 nA to 3.6 nA was seen. This showed a maximum measured current of 1.8 nA per emitter at 100.6 V applied. The reduction in the magnitude of the measured current over that seen in section 5.3 was noted for this array as well.

The Fowler-Nordheim plot obtained from the data taken from array 9-5 is shown in Figure 5.9. Again, the straight line plot indicative of field emission is noted.

5.5 Summary of electrical test results and associated geometric parameters

Table 5.1 gives a summary of some of the more interesting results from the electrical testing reported in the previous sections of this chapter. Table 5.2 shows a summary of the geometric parameters pertinent to the sharp tip between two parallel planes geometry elaborated on in Chapter 2. For the data in Table 5.2 the plane to plane spacing was estimated to be d = 2.3 μm and the tip height to be h = 1.9 μm from Figure 4.16 in Chapter 4. The number of the equation used for each calculation is listed below the respective character used to represent that particular geometric parameter.

Table 5.3 gives a summary of the geometric parameters

Table 5.1 Electrical results summary.

Test	Array	Max. V	Max. I at Max. V	Max. I per tip	I at 100V	I per tip at 100V
1	9-4	139.0V	36μA	18nA	2.9μA	1.45nA
1	9-5	135.7V	25μA	12.5nA	2.3μA	1.15nA
2	9-4	100.1V	2.5nA	1.25pA	2.5nA	1.25pA
2	9-5	100.6V	3.6nA	1.8pA	3.6nA	1.8pA

Table 5.2 Geometric parameter summary for the parallel plane geometry.

Test	Array	m (F-N slope)	β (cm^{-1}) x10^5 (2.30)	β' (unit less) (2.32)	r (nm) (2.37)	α $(nm)^2$ (2.38)
1	9-4	-270	9.13	210	9.0	510
1	9-5	-357	6.91	159	12.0	905
2	9-4	-100	24.7	568	3.3	68
2	9-5	-66	37.4	860	2.2	30

Table 5.3 Geometric parameter summary for the concentric spheres geometry.

Test	Array	m (F-N slope)	β (cm^{-1}) x10^5 (2.30)	β' (unit less) (2.40)	r (nm) (2.41)	α ($nm)^2$ (2.38)
1	9-4	-270	9.13	110	11.0	760
1	9-5	-357	6.91	83	14.6	1340
2	9-4	-100	24.7	294	4.1	106
2	9-5	-66	37.4	445	2.7	46

with respect to the concentric spheres geometry and is similar to Table 5.2 in structure. For the data in Table 5.3 the distance from the spherical emitting tip to the concentric spherical anode was estimated to be t = 1.2 μm from Figure 4.16 in Chapter 4.

In Table 5.2 and Table 5.3 the slope m of the respective Fowler-Nordheim plots was estimated from the applicable figures shown in sections 5.3 and 5.4 and the work function was assumed to be ϕ = 4.1 eV. In all three tables, Table 5.1, Table 5.2 and Table 5.3, Test 1 refers to the electrical testing using a warm up stage as related in section 5.3 and Test 2 refers to the subsequent low current electrical testing as related in section 5.4.

With regard to Test 1 results, the values for the maximum current per emitter tip as shown in Table 5.1 are in the same range as those reported in Chapter 3 for silicon [23,14] and tungsten coated silicon [25] emitters and about

3 to 4 orders of magnitude below those reported for molybdenum emitters [43]. The range of values for β and β' noted in Chapter 3 were $0.72 \times 10^5\ cm^{-1} < \beta < 5.9 \times 10^5\ cm^{-1}$ and $9.6 < \beta' < 510$. From the Test 1 results in both Table 5.2 and Table 5.3, it is seen that the values of β are close to this range and those for β' are within the range. It is noteworthy in particular that the values of β' reported in Table 5.3 for the concentric spheres geometry are quite close to the value of $\beta' = 55$ derived from the information supplied by Stephani and Branston [23] using the same theoretical geometry. It was mentioned in Chapter 3 that their actual geometry was quite similar to the geometry of the emitters presented here.

Considering the values estimated for the tip radius for Test 1, the two geometries considered yield values that are in reasonably close agreement. However, these values differ from the tip radius estimated by SEM to be in the range of 35 to 50 nm. There are several possible explanations for the discrepancy between the two estimates. Imaging of small tips on the order of 10 nm is difficult in the SEM. The beam specimen interaction tends to degrade the resolution of the instrument and make a small tip appear larger than it actually is. A TEM would be better for the tip radius measurement but additional difficult sample preparation would be necessary. It is also possible that the tips are not perfectly hemispherical and that emission takes place from small protuberances on the tip that are not easily

observable. As a final note, the theoretical models derived in Chapter 2 do not completely match the geometry of the actual device. A more precise analysis could be made by using a simulation program that solves Poisson's equation for the actual geometry.

The results from Test 2 deserve some attention. Though both arrays 9-4 and 9-5 exhibited field emission as noted earlier in section 5.4 there was a marked decrease in emission current as can be seen when compared with Test 1 results in Table 5.1. The resulting calculations of the geometric parameters led to values quite at odds with those reported in Chapter 3 and with those calculated for Test 1 and tabulated in Table 5.2 and Table 5.3. Considering these discrepancies it is obvious that the emitter arrays have undergone some type of permanent structural change. Possible explanations could include, but are not limited to, the following. Overheating of the emission tip due to vacuum arcing or intense localized emission from some of the emitters could cause partial failure of an array [8,16]. Ionization of the anode material could compromise the quality of the emitter surface [16]. Also, contamination of the emitter tip by adsorbates has been noted [15]. These adsorbates could increase the work function of the emitting surface and thereby reduce the emission current as per equation (2.24). Additionally, looking at Table 5.2 and Table 5.3 and comparing the values for the emitting surface α with respect to Test 1 and Test 2, a reduction is noted

from Test 1 to Test 2. For array 9-4, α has been reduced by a factor of about 7 and for array 9-5 by a factor of about 30. This indicates the likelihood that the number of tips taking part in emission in Test 2 is less than that for Test 1. While the reduction in α is not sufficient to completely account for the current reduction noted, it is seen as contributory.

CHAPTER 6

SUMMARY AND CONCLUSION

This thesis has introduced a novel electron beam evaporated silicon field emitter array in a diode configuration. Further, evidence has been offered that proves that field emission was the main mode of operation.

An outline of the currently accepted theory on field emission from metal surfaces has been presented. This was done with the inclusion of the assumptions required for application to semiconductor materials.

A comprehensive review of the current technology with regard to fabrication techniques, structural differences and the use of various emitter materials was presented in addition to some electrical characterizations of pertinent devices.

A detailed exposition of the fabrication process was given. The resultant emitter tips were seen to be approximately 1.9 μm in height with an unsharpened tip radius estimated by SEM to be in the range of 350 to 500 Å. Two major flaws in the fabrication process were disclosed that affected the geometric structure of the diode arrays. One problem had to do with the grainy structure of both the sacrificial and anode contact layers that were aluminum and

deposited at a grazing incidence angle. The grainy sacrificial layer could have an effect on the uniformity of the tip height since the tip height was seen to be directly proportional to the hole diameter in the aluminum layer. For the anode contact, the aluminum portion of the anode was assumed to be hemispherical. The grainy composition of the aluminum would distort the assumed geometry. The second problem had to do with the poor seating of the silicon cone which could adversely affect the current density and, therefore, the measured current. Proposals for their respective solutions were offered. It is necessary that these problems be resolved in order that the full capacity of the device can be realized.

Electrical characterization and subsequent calculations of relevant geometric parameters have been given and demonstrated as being competitive with current silicon field emitter technology. Turn on voltages in the range from 60 to 80 volts were seen. A maximum measured current of 18 nA per emitter tip at an applied voltage of 139 V was noted. The arrays were seen to fail catastrophically above 150 V applied.

Future endeavors to continue this work should include, first and foremost, resolution of the fabrication problems so that a stable more uniform geometry is attained. This should lead to reproducible electrical results and, thus, a more dependable device. Once dependability has been achieved in a typical test environment such as that specified in this

thesis, sensitivities to temperature, pressure and various wavelengths and intensities of electromagnetic radiation should be quantitatively characterized.

After the appropriate characterizations have been made, many applications are possible. Various degrees of success with both monochrome and color flat panel displays have been reported [62-67]. Other applications under current investigation include vacuum transistors [68,69], the potential for use in amplifiers [70-74] and sensor applications [75,76]. Actually, this is only a small sampling of the possible applications. Any where an electron source or high switching speed is required, there exists the possibility for utilization of field emitters.

BIBLIOGRAPHY

[1] R. H. Fowler and L. Nordheim, "Electron Emission in Intense Electric Fields", Proc. Roy. Soc. London, ser. A, vol. 119, p. 173, 1928.

[2] S. Zurn, Q. Mei, C. Ye, T. Tamagawa, and D. L. Polla, "Sealed Vacuum Electronic Devices by Surface Micromachining", IEDM Tech. Dig., p. 205, 1991.

[3] R. Stratton, "Field Emission from Semiconductors", Proc. Phys. Soc. (London), vol. B68, p. 746, 1955.

[4] A. Modinos, "Field, Thermionic and Secondary Electron Emission Spectroscopy", Plenum Press, New York, New York, 1984.

[5] R. N. Thomas, R. A. Wickstrom, D. K. Schroder and H. C. Nathanson, "Fabrication and Some Applications of Large-Area Silicon Field Emission Arrays", Solid-St. Electron., vol. 17, no. 2-D, p. 155, 1973.

[6] R. A. Lee, C. Patel, H. A. Williams and N. A. Cade, "Semiconductor Fabrication Technology Applied to Micrometer Valves", IEEE Trans. Elec. Dev., vol. 36, no. 11, p. 2703, Nov., 1989.

[7] R. B. Marcus, K. K. Chin, Y. Yuan, H. Wang and W. N. Carr, "Simulation and Design of Field Emitters", IEEE Trans. Elec. Dev., vol. 37, no. 6, p. 1545, June 1990.

[8] J. K. Cochran, K. J. Lee and D. N. Hill, "Comparison of Low-voltage Field Emission from TaC and Tungsten Fiber Arrays", J. Mater. Res., vol. 3, p. 67, 1988.

[9] H. C. Lee and R. S. Huang, "Simulation and Design of Field Emitter Array", IEEE Elec. Dev. Lett., vol. 11, no. 12, p. 579, Dec., 1990.

[10] H. G. Kosmahl, "Analytic Evaluation of Field Emission Enhancement Factors for Ellipsoidal Cones and Elliptic Cross-Section Wedges", IEEE Trans. Elec. Dev., vol. 38, no. 6, p. 1534, June, 1991.

[11] C. A. Spindt, I. Brodie, L. Humphrey and E. R. Westerberg, "Physical Properties of Thin-Film Field Emission Cathodes with Molybdenum Cones", J. Appl. Phys., vol. 47, no. 12, p. 5248, Dec., 1976.

[12] T. Asano and T. Tamon, "Fabrication of Si Tips by Ar Ion Sputtering", IVMC 91 Tech. Dig., p. 88, 1991.

[13] M. Sokolich, E. A. Adler, R. T. Longo, D. M. Goebel and R. T. Benton, "Field Emission From Submicron Emitter Arrays", IEDM Tech. Dig., p. 159, 1990.

[14] Charles E. Hunt, Johann T. Trujillo and William J. Orvis, "Structure and Electrical Characteristics of Silicon Field-Emitter Microelectronic Devices", IEEE Trans. Elec. Devices, vol. 38, no. 10, p. 2309, 1991.

[15] R. J. Harvey, R. A. Lee, A. J. Miller and J. K. Wigmore, "Aspects of Field emission from Silicon Diode Arrays", IEEE Trans. Elec. Devices, vol. 38, no. 10, p. 2323, 1991.

[16] Nicol E. McGruer, K. Warner, P. Singhal, J. J. Gu and Chung Chan, "Oxidation-Sharpened Gated Field Emitter Array Process", IEEE Trans. Elec. Devices, vol. 38, no. 10, p. 2389, 1991.

[17] W. J. Orvis, C. F. McConaghy, D. R. Ciarlo, J. H. Yee and E. W. Hee, "Modeling and Fabricating Micro-Cavity Integrated Vacuum Tubes", IEEE Trans. Elec. Dev., vol. 36, no. 11, Nov., 1989.

[18] D. F. Howell, R. D. Groves, R. A. Lee, C. Patel and H. A. Williams, "Experimental Results on Gridded Arrays of Field Emission Tips", IEDM Tech. Dig., p. 525, 1989.

[19] J. P. Spallas and N. C. MacDonald, "Fabrication and Operation of Silicon Field Emission Cathode Arrays", IEDM Tech. Dig., p. 209, 1991.

[20] H. F. Gray and J. L. Shaw, "Point and Wedge Tungsten-on-Silicon Field Emitter Arrays, IEDM Tech. Dig., p. 221, 1991.

[21] K. Betsui, "Fabrication and Characteristics of Si Field Emitter Arrays", IVMC 91 Tech. Dig., p. 26, 1991.

[22] H. F. Gray, J. L. Shaw, G. W. Jones and C. T. Sune, "High Current Density Silicon FEAs", IVMC 91 Tech. Dig., p. 30, 1991.

[23] D. Stephani and D. W. Branston, "Characterization and Fabrication of Single-Tip Field Emission Diodes Incorporating a Hemispherical Collector Electrode", IVMC 91 Tech. Dig., p.32, 1991.

[24] J. S. Blakemore, "Solid State Physics", 2nd edition, Cambridge University Press, p.192, 1985.

[25] H. H. Busta, R. R. Shadduck and W. J. Orvis, "Field Emission from Tungsten-Clad Silicon Pyramids", IEEE Trans. Elec. Dev., vol. 36, no. 11, p. 2679, Nov., 1989.

[26] Takao Utsumi,"Keynote Address - Vacuum Microelectronics: What's New and Exciting", IEEE Trans. Elec. Devices, vol. 38, no. 10, p. 2276, 1991.

[27] K. E. Petersen, "Silicon as a Mechanical Material", Proceedings of the IEEE, vol. 70, no. 5, p. 420, May, 1982.

[28] W. J. Orvis, D. R. Ciarlo, C. F. McConaghy, J. H. Yee, E. Hee, C. Hunt and J. Trujillo, "A Progress Report on the Livermore Miniature Vacuum Tube Project", IEDM Tech. Dig., p. 529, 1989.

[29] N. A. Cade, R. A. Lee and C. Patel, "Wet Etching of Cusp Structures for Field-Emission Devices", IEEE Trans. Elec. Dev., vol. 36, no. 11, p. 2709, Nov., 1989.

[30] R. B. Marcus, T. S. Ravi, T. Gmitter, K. Chin, D. Liu, W. J. Orvis, D. R. Ciarlo, C. E. Hunt and J. Trujillo, "Formation of Silicon Tips with <1 nm Radius", Appl. Phys. Lett., vol. 56, no. 3, p. 236, Jan., 1990.

[31] Steven M. Zimmerman and Wayne T. Babie, "A Fabrication Method for the Integration of Vacuum Microelectronic Devices", IEEE Trans. Elec. Devices, vol. 38, no. 10, p. 2294, 1991.

[32] Jung Y. Ea, Dazhong Zhu, Yicheng Lu, B. Lalevic and Robert J. Zeto, "Silicon Avalanche Cathodes and Their Characteristics", IEEE Trans. Elec. Devices, vol. 38, no. 10, p. 2377, 1991.

[33] A. M. E. Hoeberechts, "Novel Silicon Avalanche Diode as a Direct Modulated Cathode with Integrated Planar Electron Optics", IEDM Tech. Dig., p. 155, 1990.

[34] V. T. Binh and M. Chaouch, "A Field Emission Study of Silicon", Colloque de Physique, Colloque C8, Supplement au n°11, Tome 50, Nov., 1989.

[35] T. S. Ravi, R. B. Marcus, T. Gmitter, H. H. Busta and J. T. Niccum, "Fabrication of Atomically Sharp Tungsten Tips", Appl. Phys. Lett., vol. 57, no. 14, p. 1413, Oct., 1990.

[36] R. B. Marcus, T. S. Ravi, T. Gmitter, H. H. Busta, J. T. Niccum, K. K. Chin and D. Liu, "Atomically Sharp Silicon and Metal Field Emitters", IEEE Trans. Elec. Devices, vol. 38, no. 10, p. 2289, 1991.

[37] E. A. Adler, Z. Bardai, R. Forman, D. M. Goebel, R. T. Longo and M. Sokolich, "Demonstration of Low-Voltage Field Emission", IEEE Trans. Elec. Devices, vol. 38, no. 10, p. 2304, 1991.

[38] D. W. Branston and D. Stephani, "Field Emission from Metal-Coated Silicon Tips", IEEE Trans. Elec. Devices, vol. 38, no. 10, p. 2329, 1991.

[39] G. G. P. van Gorkom and A. M. E. Hoeberechts, "Performance of Silicon Cold Cathodes", J. Vac. Sci. Technol. B, vol. 4, p. 108, 1986.

[40] C. A. Spindt, "A Thin-Film Field-Emission Cathode", J. Appl. Phys., vol. 39, no. 7, p. 3504, June, 1968.

[41] M. W. Geis, N. N. Efremow, J. D. Woodhouse, M. D. McAleese, M. Marchywka, D. G. Socker and J. F. Hochedez, "Diamond Cold Cathode", IEEE Elec. Dev. Lett., vol. 12, no. 8, p. 456, Aug., 1991.

[42] W. N. Carr, J. M. Kim, R. J. Zeto, E. S. Zakar and C. D. Mulford, "Field Emission Diodes with Tungsten Wedge Cathode", IEDM Tech. Dig., p. 225, 1991.

[43] C. A. Spindt, C. E. Holland, A. Rosengreen and Ivor Brodie, "Field-Emitter Arrays for Vacuum Microelectronics", IEEE Trans. Elec. Devices, vol. 38, no. 10, p. 2355, 1991.

[44] Seigo Kanemaru and Junji Itoh, "Fabrication and Characterization of Lateral Field-Emitter Triodes", IEEE Trans. Elec. Devices, vol. 38, no. 10, p. 2334, 1991.

[45] J. Itoh, S. Kanemaru, N. Nishimura, K. Tsuburaya, T. Watanabe and S. Itoh, "Metal-Film-Edge Field Emitter Array with a Self-Aligned Gate", IVMC 91 Tech. Dig., p. 46, 1991.

[46] C. Nureki and M. Araragi, "Planar Field Emission Devices with Three-Dimensional Gate Structures", IVMC 91 Tech. Dig., p. 78, 1991.

[47] S. Fukuta and K. Betsui, "Fabrication and Characteristics of Tantalum Field Emitter Arrays", IVMC 91 Tech. Dig., p. 144, 1991.

[48] R. Z. Bakhtizin, S. S. Ghots and E. K. Ratnikova, "GaAs Field Emitter Arrays", IEEE Trans. Elec. Devices, vol. 38, no. 10, p. 2398, 1991.

[49] A. Kaneko, T. Kanno, K. Tomii, M. Kitagawa and T. Hirao, "Wedge-Shaped Field Emitter Arrays for Flat Display", IEEE Trans. Elec. Devices, vol. 38, no. 10, p. 2395, 1991.

[50] A. Kaneko, T. Kanno and K. Morishita, "Field Emitter Array with Lateral Wedges", IVMC 91 Tech. Dig., p. 50, 1991.

[51] B. C. Djubua and N. N. Chubun, "Emission Properties of Spindt-Type Cold Cathodes with Different Emission Cone Material", IEEE Trans. Elec. Devices, vol. 38, no. 10, p. 2314, 1991.

[52] C. A. Spindt, C. E. Holland and R. D. Stowell, "Recent Progress in Low-Voltage Field-Emission Cathode Development", J. de Phys., Comp. C9, Supp. to vol. 45, no. 12, p. 269, Dec., 1984.

[53] M. Benjamine and R. O. Jenkins, "The Distribution of Autoelectronic Emission from Single Crystal Metal Points 1. Tungsten, Molybdenum, Nickel in the Clean State", Proc. Royal Soc. London, Ser. A, no. 965, vol. 176, p. 262, Oct., 1940.

[54] A. V. Crewe, D. N. Eggenberger, J. Wall and L. M. Welter, "Electron Gun Using a Field Emission Source", Rev. Sci. Instrum., vol. 39, no. 4, p. 576, April, 1968.

[55] R. M. Anderson, "Microstructural Analysis of Evaporated and Pyrolytic Silicon Thin Films", J. Electrochem. Soc.: Solid-State Science and Technology, vol. 120, p.1540, Nov., 1973.

[56] H. Guckel, D. W. Burns, C. C. G. Visser, H. A. C. Tilmans and D. DeRoo, "Fine Grained Polysilicon Films with Built-In Tensile Strain", IEEE Trans. Elec. Dev., vol. ED35, p. 800, 1988.

[57] M. H. Brodsky, R. S. Title, K. Weiser and G. D. Pettit, "Structural, Optical and Electrical Properties of Amorphous Silicon Films", Phys. Rev. B, vol. 1, no. 6, March, 1970.

[58] M. Aslam, "Common Origin for Electron and Hole Traps in MOS", IEEE Trans. Elec. Dev., vol. ED-34, no. 12, p. 2535, Dec., 1987.

[59] D. W. Burns and H. Guckel, "Thin Films for Micromechanical Sensors", J. Vac. Sci. Technol. A, vol. 8, no. 4, p. 3606, Jul./Aug., 1990.

[60] G. P. Myers, M. Aslam, L. W. Cathey, R. E. Elder and B. E. Artz, "Fabrication of Silicon Cold-Cathodes by Electron Beam Evaporation", IVMC 91 Tech. Dig., p. 86, 1991.

[61] The Optical Industry and Systems Purchasing Directory, Handbook, Optical Pub. Co., Pittsfield, Mass, 1980.

[62] P. Vaudaine and R. Meyer, "Microtips Fluorescent Display", IEDM Tech. Dig., p. 197, 1991.

[63] R. Meyer, "Recent Development on Microtips Display at LETI", IVMC 91 Tech. Dig., p. 6, 1991.

[64] G. A. Vorobyev, V. M. Gaponenko, S. A. Ghyngazov, N. I. Koshinova, S. S. Kramor, R. B. Lubsanov and P. E. Troyan, "MIM Emitter Arrays Applied to Vacuum Fluorescent Display", IVMC 91 Tech. Dig., p. 54, 1991.

[65] S. Itoh, T. Watanabe, T. Yamaura, K. Ohtsu, M. Yokoyama, M. Taniguchi, H. Nakata, M. Miyamori and M. Yamaguchi, "Investigation of a Cathodoluminescent Display Device with FE Cathodes", IVMC 91 Tech. Dig., p. 58, 1991.

[66] N. N. Chubun, B. Ch. Djubua, B. I. Gorfinkel and E. V. Rusina, "Field-Emission Array Cathodes for a Flat-Panel Display", IVMC 91 Tech. Dig., p. 60, 1991.

[67] A. Ghis, R. Meyer, P. Rambaud, F. Levy and T. Leroux, "Sealed Vacuum Devices: Fluorescent Microtip Displays", IEEE Trans. Elec. Devices, vol. 38, no. 10, p. 2320, 1991.

[68] H. F. Gray, J. L. Shaw, A. I. Akinwande, and P. Bauhahn, "Film Edge Emitters: The Basis for a New Vacuum Transistor", IEDM Tech. Dig., p. 201, 1991.

[69] H. H. Busta, D. W. Jenkins, B. J. Zimmerman and J. E. Pogemiller, "Triode Operation of a Vacuum Transistor", IEDM Tech. Dig., p.213, 1991.

[70] H. P. Warren, T. J. Wiltsey, E. C. Chou, F. C. Wong and N. C. Luhmann, Jr., "1 to 25 GHz Vacuum FET Distributed Amplifier Analysis", IEDM Tech. Dig., p. 171, 1990.

[71] N. I. Sinitsyn, Yu. V. Gulyaev, V. A. Solntsev, A. M Alexeenko and M. B. Golant, "Recent Progress on Microwave Generation and Amplification by FEAs and Other Microvacuum Devices", IVMC 91 Tech. Dig., p. 64, 1991.

[72] N. E. McGruer and A. C. Johnson, "Field Emitter Structures in Microwave Generation and Amplification", IVMC 91 Tech. Dig., p. 68, 1991.

[73] P. M. Phillips, E. G. Zaidman, R. E. Neidert, C. Hor and C. A. Spindt, "Investigation of Field-Emission Triodes at NRL", IVMC 91 Tech. Dig., p. 72, 1991.

[74] V. I. Bayle, N. N. Chubun, B. C. Djubua and A. V. Sazonov, "Experimental Investigation of the Microvacuum Triode Amplifier", IVMC 91 Tech. Dig., p. 76, 1991.

[75] J. C. Jiang, P. K. Allen and R. C. White, "Microvacuum Diode Sensor for Measuring Displacement and Loads", IVMC 91 Tech. Dig., p. 128, 1991.

[76] T. Asano and R. Kajiwara, "Fabrication of a Tunnel Sensor with Cantilever Structure", IVMC 91 Tech. Dig., p. 204, 1991.

[77] M. Aslam, G. P. Myers, P. Klimecky, L. W. Cathey, B. E. Artz, "Characterization of Evaporated-Silicon Cold-Emitter Diodes", presented at the Fifth International Vacuum Microelectronics Conference, Vienna, Austria, July, 1992.

[78] G. P. Myers, M. Aslam, P. Klimecky, L. W. Cathey, R. E. Elder and B. E. Artz, "Fabrication and Characterization of Electron Beam Evaporated Silicon Field Emitter Arrays", submitted for publication to J. Vac. Sci. Technol., 1992.

[79] S. Wang, "Fundamentals of Semiconductor Theory and Device Physics", Prentice Hall, Inc., Englewood Cliffs, New Jersey, 1989.

[80] D. K. Reinhard, "Introduction to Integrated Circuit Engineering", Houghton Mifflin Co., Boston, Mass., 1987.