ENGINEERING GRAPHENE FOR NANOELECTRONICS

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ABSTRACT

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Graphene has attracted research interest since its discovery in 2004 and professor Geim's receipt of the Nobel prize in 2010. It has been used for constructing a variety of electronics and sensors due to its unique electrical, mechanical, thermal, and optical properties.

In this dissertation, we developed several technologies to control the electronic properties of graphene, which will pave the way for the future development of graphene nanoelectronics. First, since graphene properties vary depending on its number of layers, we identified a method for engineering the number of graphene layers using fine-tuned oxygen plasma etching. With this technique, a single layer of graphene can be removed at a time. In addition, we demonstrated a template-less nanofabrication technique for batch production of graphene nanomeshes and multiribbons, and explored the feasibility of using these nanopatterns to construct field effect transistors (FETs). By introducing nanopatterns into pristine graphene, we could effectively open the band gap of graphene and convert it from semimetal into semiconductor. Furthermore, we studied a doping method for making *n*-type graphene with long-term chemical stability in air and stability at wide range of temperature. Highly stable *n*-type graphene with minimal defects was achieved using photo acid generator (PAG) mixed with SU-8 epoxy resin as an effective electron dopant and encapsulation. The electronic properties of the as-doped *n*-type graphene were confirmed by measuring its current transport characteristics and Fermi level shifts.

Building on the aforementioned engineering techniques, we proposed a new Metal-SU8-graphene (MSG) technology, which is compatible with the conventional CMOS fabrication

technology. MSG FETs were fabricated on both rigid and flexible substrates. A graphene invertor was also constructed as a proof of concept.

Finally, we explored the potential applications of graphene in nanosensors, including chemical, temperature and flow sensors. We studied the possibility of using an inter-layer graphene nano configuration to detect the absorption/desorption of different chemical molecules. Our results show a remarkable enhancement in graphene surface sensitivity, which can be attributed to extra edges and inter-sheet tunneling effects. We also demonstrated the capability of using graphene nanowires in temperature and flow rate sensing.

Dedicated to my parents, my wife Areej, my daughters Rutaj and Jumana,
to my brother Amir and my sister Ban, for their love and support

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Lastly, a special thank to my parents, wife, brother and sister. This dissertation is dedicated to them for their love and support for achieving my academic goals.

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KEY TO ABBREVIATIONS

AFM: Field effect transistor

C_{ox}: Oxide capacitance

CNT: Carbon nanotube

d: distance between gate and closest layer (SiO_2 thickness)

$\boldsymbol{\varepsilon}_o$: permittivity of the vacuum

D (E): Density of state

DI: Deionized water

e: Electron charge

α: Resistance temperature coefficient

σ_s: Sheet resistance

E_f: Fermi energy

$E_{t,b}$: Electric field produces by top/back gate voltage

EBL: Electron beam lithography

F_0 (E): Fermi function

FET: Field effect transistor

FIB: Focused ion beam

FLG: Few layer graphene

λ: Mean free path

υ_F: Fermi velocity

V_g: Gate voltage

ħ: Reduced Plank's constant

h: Heat transfer coefficient

HOPG: Highly ordered pyrolytic graphite

IV: Current voltage relation

k: dielectric constant

K: Kelvin

n_s: Charge density

OPE: Oxigen plasma etching

PMMA: polymethyl methacrylate

RIE: Reactive ion etching

R_T: Room temperature

R_W: Wire resistance

Sccm: Standard cubic centimeter

SEM: Scanning electron microscope

SF_6: Sulfur hexafluoride

t_{ox}: Oxide thickness

T_W: Wire temperature

T_f : Fluid temperature

PAG: Photo acid generator

1 NTRODUCTION TO GRAPHENE

1.1 Introduction

Graphene has attracted research interest since its discovery in 2004. Unlike semiconductors, the band structure of graphene is unique. It is a zero band semiconductor, which means there is no band gap between the valance and the conduction bands, as shown in the Figure 1.1. The valance band and conduction band are symmetric around the six Dirac points. This unique band structure promotes high electron mobility of up to 2×10^5 $cm^2V^{-1}s^{-1}$ for suspended graphene and around 1.5×10^4 $cm^2V^{-1}s^{-1}$ for graphene on silicon dioxide (SiO_2) [1-4]. In addition, graphene has a high cutoff frequency theoretically. The reported study predicts a cutoff frequency of 400-600 GHz for 50 nm gated graphene field effect transistors (FETs) [5], whereas the maximum value recorded for silicon is only around 40 GHz. This makes graphene an excellent candidate material for the next generation of radio-frequency (RF) transistors and analog integrated circuits. Moreover, graphene has high thermal conductivity (5×10^3 $Wm^{-1}K^{-1}$), a high surface area (theoretically 2630 m^2/g), and high transparency (~97% over a wide range of wavelengths from the visible spectrum to the near infrared (IR)) [6]. These stunning properties provide a fertile ground for a wide variety of potential applications of graphene, such as electronics, photonics, and sensors. The unique combination of electrical, thermal, and optical properties of graphene can be better understood from its physics properties, which will be discussed in details in section 1.2.

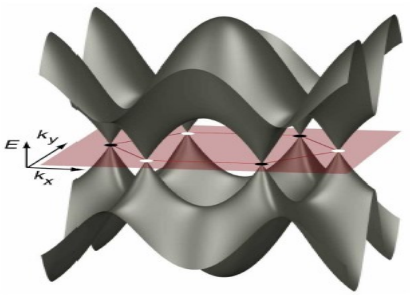
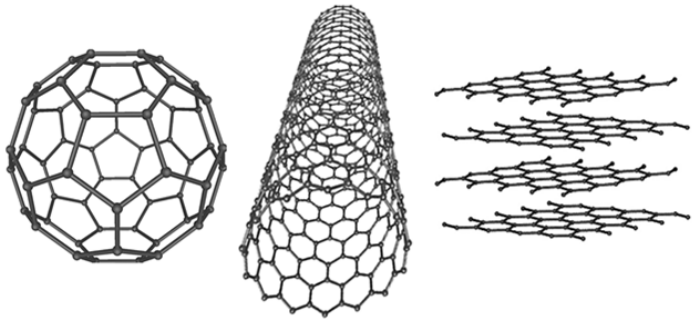


Figure 1.1 Graphene band structure [7].

1.2 Theoretical Background of Graphene

1.2.1 Crystal structure of graphene

Graphene is a one-atom thick layer of graphite, a honeycomb two dimensional lattice of carbon atoms with sp^2 hybridization. It can be wrapped up into zero dimension fullerenes, rolled into one dimension CNTs, or stacked into three dimensional graphite [8], as depicted in Figure 1.2. The crystal structure of graphite consists of multiple layers of carbon sheets in a Bernal stack. The s, p_x, and p_y atomic orbitals on each carbon hybridize to form strong covalent sp^2 bonds within a single layer graphene sheet (Figure 1.3 (a)) [9]. The remaining p_z orbital on each carbon overlaps with its three neighboring carbons to form a band of filled π orbitals (known as the valence band) and a band of empty π^* orbitals (known as the conduction band). This weak interlayer binding leads to out-of-plane electrical and thermal conductivities between multilayer graphene, which could be utilized as a sensing mechanism for detecting molecule adsorption/desorption, mechanical displacement, and atomic forces, etc., as discussed in Chapter 6. In addition, graphene has zero effective mass and minimum conductivity for holes and electrons near the six Dirac points (Figure 1.3 (b)). These charge carriers can travell thousand interatomic distances without scattering, owing to the super-fast mobility of graphene.



(a) (b) (c)

Figure 1.2 Conceptually, graphene is a building material for (a) fullerene (b) CNTs and (c) graphite [8].

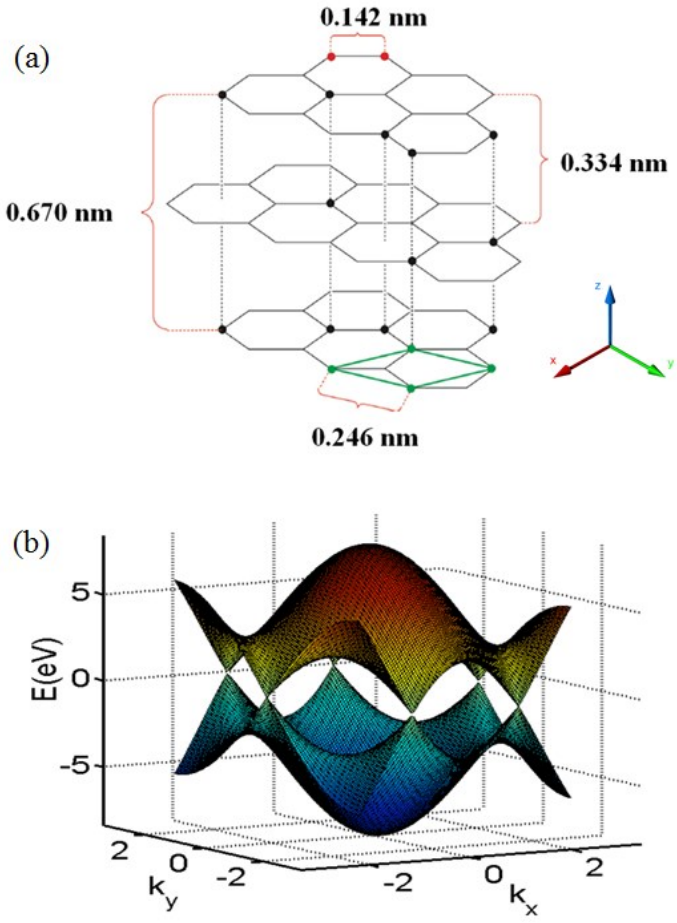


Figure 1.3 (a) Bernal stack of a typical graphite structure. (b) Band structure of graphene showing the six Dirac neutrality points [6].

In the a single-layer graphene sheet, the crystal structure consists of six carbon atoms in a unit cell, of which two are distinct atoms and the other atoms can be reached by a reciprocal

lattice vector translation (Figure 1.4 (a)). As in Figure 1.4 (b), the band structure of graphene can be simplified into two cones. The Fermi level is in the intersection of the cones with no energy gap between the valance band and the conduction band. The shifting in Fermi level upward to the conduction band or downward to the valance band can be calculated by $\Delta E_F = \sqrt{\pi n_s (\hbar \upsilon_F)^2}$ where n_s is the charge carrier and υ_F is the Fermi velocity.

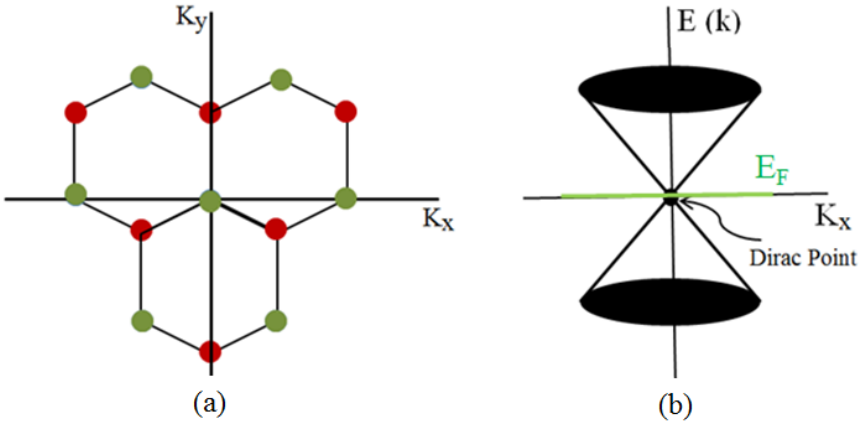


Figure 1.4 (a) The Brillouin zone and (b) simplified band structure of mono-layer graphene.

The energy bands can be derived using the following equation [10]:

$$E(k) = \pm \hbar \upsilon_F k = \pm \hbar \upsilon_F \sqrt{k_x^2 + k_y^2} \qquad \text{Equation 1-1}$$

Where $\hbar$ is the reduced Plank's constant and k is the wave vector. The Fermi velocity of electrons, υ_F, can be determined from the slop of *k-E(k)* [10],

$$\upsilon(k) = \frac{1}{\hbar}\frac{\partial E}{\partial k} = \upsilon_F \qquad \text{Equation 1-2}$$

From the above equations, it can be seen that the slop of *k-E(k)* is constant everywhere and the electron velocity is equal to Fermi velocity (υ_F), where $\upsilon_F \approx 3\times10^6$ m/s [11].

As discussed previously, unlike semiconductors, the band gap between the valance and conduction bands of graphene is zero. Therefore, a two-component wave function can be defined for mono-layer graphene, as given in Equation 1-3.

$$\Psi(x,y) = \begin{bmatrix} 1 \\ se^{i\theta} \end{bmatrix} e^{i(K_x x + K_y x)} \qquad \text{Equation 1-3}$$

Where, $s=sng(E)$ and $\Theta=arctan(K_y/K_x)$. Due to this zero band gap, graphene is expected to have very high electron mobility of around 2×10^5 cm^2 V^{-1} s^{-1} at room temperature [1] and exceptional thermal conductivity (5000 $Wm^{-1}K^{-1}$). In addition, the zero band gap of pristine graphene makes it a metallic behaving material.

1.2.2 Carrier density of graphene

From the physics point of view, one significant factor affecting the electron mobility in graphene is the carrier density. Theoretically, the density of state increases linearly with energy as shown in Figure 1.5, and can be discribed by:

$$D(E) = 2|E|/\pi\,\hbar^2 v_F^2 \qquad \text{Equation 1-4}$$

Where $\hbar$ is the reduced Plank's constant, v_F is the Fermi velocity of electrons, and E is the band energy.

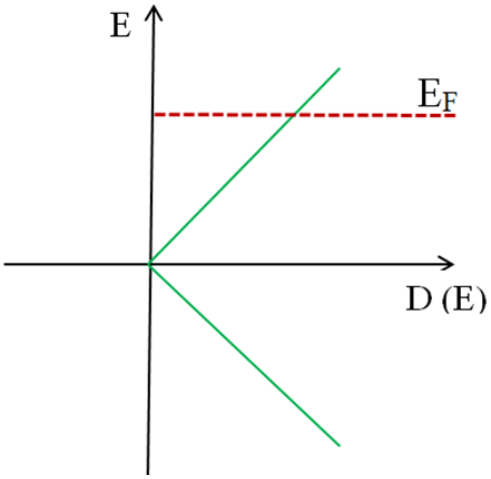


Figure 1.5 Energy and the density of state relationship in graphene

Therefore, the carrier density can be derived by integrating the density of state (*D(E)*) multiplied by the Fermi function (*$f_0(E)$*), as shown in the following equations.

$$n_s(E_F) = \int_0^{\infty} D(E) f_0(E) dE \qquad \text{Equation 1-5}$$

$$n_s(E_F) = \int_0^{E_F} D(E) dE \qquad \text{Equation 1-6}$$

$$n_s(E_F) = \frac{2}{\pi \hbar^2 v_F^2} \int_0^{E_F} E dE \qquad \text{Equation 1-7}$$

$$n_s(E_F) = \frac{E_F^2}{\pi \hbar^2 v_F^2} \qquad \text{Equation 1-8}$$

Increasing the carrier density leads to the decrease of the mobility, due to the dominant scatterers. In particular, the electron mobility can decrease significantly when graphene is transferred onto a dielectric substrate, depending on the nature and impurity of the insulator. As an example, the electron mobility of graphene on SiO_2 is reported to be only a few thousands of $cm^2V^{-1}s^{-1}$ [12].

1.2.3 Lattice vibration in graphene

Another reason of graphene's high mobility at room temperature is the behavior of lattice vibrations (phonons). In conventional semiconductors such as silicon, the scattering of optical phonons dominates at room temperature, causing a large decrease of the electron mobility with an increasing temperature [13]. In graphene, electrons do not interact with optical phonons due to the high energy ($\hbar\omega$~200 meV) of optical phonons [14]. However, electrons interact with longitudinal acoustic (LA) phonons of graphene and the emission and the absorption of acoustic phonon lead to momentum loss and generation of resistance. The contribution of the resistivity from LA phonons is temperature dependent and can be described by [15]:

$$\rho_{ph}(T,n) = \frac{\pi^2 D^2 k_B T}{e^2 2h^2 \rho_m v_{ph}^2 v_F^2} \qquad \text{Equation 1-9}$$

Where k_B is the Boltzmann constant, D is the acoustic deformation potential, T is the temperature, v_F is the Fermi velocity of electrons, v_{ph}=2.1$\times$10^4 m/s is the sound velocity of LA phonons in graphene, and ρ_m=6.5$\times$10^{-7} kg/m^2 is the areal mass density of graphene. The Equation 1-12 applies when temperature is greater than the Bloch-Gruneisen temperature (T_{BG}) where $T_{BG}=2\hbar k_F v_{ph}/k_B$. In fact, the effects of the LA scattering on the intrinsic mobility of graphene are very little at room temperature because of the high Fermi temperature at high carrier density of graphene [16, 17]. As a result, graphene is expected to exhibit much higher electron mobility than conventional semiconductors.

1.2.4 Gate-voltage modulating effect

While pristine graphene is known to be metallic, it is possible to modulate the Fermi level and thus the semiconducting properties of graphene, usually by applying a gate voltage either

though a back-, a top-, or a dual-gate configuration. In these cases, the gate voltage is defined as the voltage applied to a graphene sheet through an insulation layer, such as SiO_2. Through the gate-voltage modulating effect, the type of charge carriers in graphene can be tuned between electrons and holes with a doping concentration (n) as high as $1\times10^{13}cm^{-2}$ and an electron mobility (μ) of greater than 2×10^{5} cm^2 V^{-1} s^{-1} for suspended exfoliated graphene. Moreover, the sheet conductance is also affected by the gate voltage and its value, as well as the charge carrier concentration, and can be determined experimentally:

$$\sigma_S(E_F) \approx \frac{2q^2}{h} \lambda_{app}(E_F)\left(\frac{2E_F}{\pi\hbar\upsilon_F}\right) \quad \text{Equation 1-10}$$

$$n_s = C_{ox}V_G \approx \frac{1}{\pi}\left(\frac{E_F}{\hbar\upsilon_F}\right)^2 \quad \text{Equation 1-11}$$

Specifically, $C_{ox}=\varepsilon_o\varepsilon_{ox}/t_{ox}$ is the oxide capacitance, in which ε_o is the vacuum dielectric constant and ε_{ox} is the oxide relative dielectric constant, and t_{ox} is the oxide thickness. Graphene capacitance is negligible since the gate oxide thickness is relatively high (300 nm). Furthermore, the mean-free-path (λ) of charge carriers is inversely proportional to the Fermi energy (E_F), as described in Equation 1-12, and can be expressed by:

$$\lambda(E_F) = \frac{\sigma_S}{(2q^2/h)(2\sqrt{n_S/\pi})} \quad \text{Equation 1-12}$$

1.2.5 Influences of substrate on graphene mobility

In the absence of the gate voltage, the mobility, by which can be calculated by $\mu=t/(d\sigma/dv_g)$ where, t is the silicon oxide thickness (300nm), $\boldsymbol{\varepsilon}$ is the permittivity of the silicon dioxide $\boldsymbol{\varepsilon}$=8.85e-12 F/m, σ and V_G are the conductance and the gate voltage respectively, is mainly

limited by impurities and phonon scattering of the substrate where graphene is transferred onto. Usually during device fabrication, graphene is transferred onto a SiO_2 substrate, which is a polar substrate. Such substrates allow for existence of polar optical phonons localized near the graphene-substrate interface. This could be an important scattering source of graphene carriers that gives rise to additional resistance and temperature dependence. This type of scattering is called remote oxide phonons scattering [12, 18]. At room temperature there are two optical modes for a SiO_2 substrate, $\hbar\omega_1$~60 meV and $\hbar\omega_2$~150 meV, which together resemble an extrinsic mobility limit of around 4×10^4 $cm^2V^{-1}s^{-1}$ [18].

For exfoliated graphene on SiO_2, the best reported electron mobility is around 20000 $cm^2V^{-1}s^{-1}$ [19]. Based on the scanning tunneling microscope (STM) studies, suspension of graphene minimizes the optical phonon scattering and therefore improves the electron mobility by an order of magnitude [20]. Moreover, graphene that is achieved from silicon carbide (SiC) or chemical vapor deposition (CVD) methods typically has lower mobility in the order of several thousands of $cm^2V^{-1}s^{-1}$. The mobility declines due to the lattice defects and interfacial roughness, which is another source of extrinsic scattering.

In addition, although graphene is chemically inert and does not form chemical bonds with a SiO_2 surface, it is however subjected to charge transfer and Coulomb scattering as a result of ionized donors. Previously it has been reported that SiO_2 surface can transfer electrons to graphene, resulting in electron doping of graphene. This *n*-doping was observed after annealing graphene in high vacuum at 200 °C for 20 hrs [21]. Therefore, to further enhance electron mobility, it is required to use a chemical inert substrate such as crystalline boron

nitride substrate [22], with which the electron mobility of up to 60000 $cm^2V^{-1}s^{-1}$has been achieved.

1.2.6 Geometrical effects

As the width of graphene sheet shrinks in one dimension to several times of its unit cell, its electronic properties change accordingly. Graphene sheets with such a narrow width are called graphene nanoribbons (GNRs). Figure 1.6 shows schematics of two GNRs with an equal width but two different kinds of edges, armchair and zigzag.

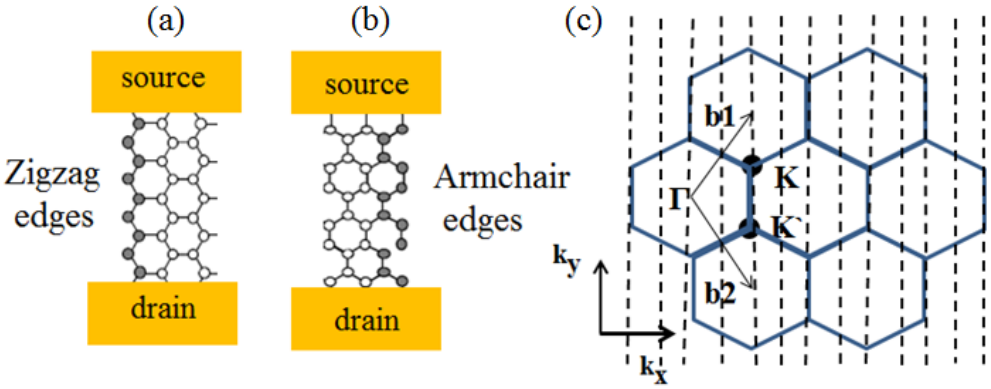


Figure 1.6 Illustration of two types of GNR edges: (a) zigzag and (b) armchair. (c) Confinement in the x-direction quantizes the *kx* quantization of graphene band into 1-D band.

The electronic states of both the armchair and zigzag are confined in the *x*-direction. This quantum confinement leads to quantized momentum, $k_x=n\pi/W$, where n=0, 1, 2… and W is the width of the GNR (in nm). The k_x quantization divides the Brillouin zone into discrete energy bands as shown in Figure 1.6 (c). With a narrow width, the energy gap between adjacent bands can be enlarged significantly. Theoretically, the energy gap between adjacent bands is on the order of $\Delta E \sim \hbar v_F \pi/W$ or 2 eV/W (nm), where W is the width of nanoribbon [23]. The possibility of opening the band gap in GNRs enables the potential application of graphene in the field of electronic devices. However, achieving a band gap close to

conventional semiconductors (e.g. Si) is still challenging since it would require a GNR with a width of a few nanometers.

In addition to the influence on the band gap, the width (W) of GNRs can significantly affect the current ON-OFF ratio of graphene-based transistors. For example, the ON-OFF ratio is around 10 when W is wider than 20 nm, whereas it is increased to 10^6 when W is approaching 2 nm [24, 25]. While a narrower GNR enables a higher ON-OFF ratio, GNR transistors suffer from low electron mobility in the order of several hundreds of $cm^2V^{-1}s^{-1}$ when W is $\leq$ 20 nm [26]. It has been found that, at W < 60 nm, the electron mobility highly depends on the edge scattering. The edge roughness induced by the etching process creates band edge fluctuations, which in turn produce electron-hole scattering and lead to the decrease in the carrier mobility.

In addition to the effect of the GNR width upon its electronic properties, the edge configuration of the GNR is another significant factor. Depending on the edge orientation, the GNRs with zigzag edges usually exhibit metallic properties, while the GNRs with armchair edges may exhibit either metallic or semiconductor properties. In particular, an armchair GNR is metallic when $W=(3n+1)a$, where W is the width of the nanoribbon, n is an integer, and a=0.246 nm is the lattice constant of graphene, and is semiconductor otherwise [27, 28]. Practically, the edges often consist of a mixture of zigzag and arm chair termination. Theoretical calculations show that zigzag edges dominate when the GNR is wider [23]. Despite the metallic properties of the GNR that exist theoretically, most fabricated GNRs are semiconductors since the edges of the zigzag GNRs could not survive even with a small surface disorder.

1.3 Graphene Applications in Nanoelectronic Circuits

The extraordinary electrical and thermal properties of graphene make it attractive for applications in nanoscale transistors and nanoelectronic circuits. While such promising properties have also been reported for carbon nano tubes (CNTs), the fact that graphene can be fabricated using conventional CMOS-technology is potentially a humongous advantage over CNTs. Moreover, in order to use CNTs for electronic devices, it is necessary to select CNTs that show semiconductor properties, which resembles another difficulty for device fabrication.

At present, the use of graphene in the design and development of nanoelectronic and integrated circuits can be divided into three main categories. The first category is radio frequency (RF) circuits, such as RF mixers [29-31], RF amplifier [32], Gigahertz ring oscillators [33], and frequency multipliers [34], due to the high cutoff frequency and the ambipolar transport property of graphene. Second, the high thermal conductivity of graphene makes it a promising alternative material to replace copper for on-chip interconnection. The main purpose of using graphene as interconnection is to improve heat dissipation, which resembles a bottleneck in the CMOS integrated circuit design [35-37]. Finally, graphene has also been explored in constructing logic gate circuits. However, unlike analog circuit and interconnect applications, the development of graphene-based logic circuits faces critical challenges that remain unsolved.

First, logic gate circuits require opening the band gap of pristine graphene to convert it from a metallic material to a semiconducting one. Several methods have been reported to produce GNRs as techniques for opening the band gap. For example, electron beam lithography has been demonstrated in the fabrication of GNRs with the width of around 20 nm, but with rough edges [26]. Chemical exfoliation of graphite can produce GNRs with the width of less

than 10 nm and smooth edges [38]. Unzipping multi-walled carbon nanotubes is another approach to generate narrow ribbons with a width of below 10 nm, and can be achieved by oxidative process [39] or by plasma etching of carbon nanotubes partially embedded in a polymer film [40]. However, these methods have high fabrication cost and non-controllability of the width of the fabricated GNRs.

The second challenge of making graphene logic circuits is the requirement of both *n*- and *p*-type transistors. Unlike *p*-type graphene that can be doped effectively and stably through chemical methods, chemically-doped *n*-type graphene is very unstable in air due to oxygen and impurity doping effects. Specific processes need to be developed in order to fabricate both *n*- and *p*- type graphene monolithically on a single substrate. Previously, Trarersi et al. [41] demonstrated an electrical annealing technique to clean up a part of a graphene sheet to restore the *n*-type property whereas the other part was left as the p-type region. However, this technique is unpractical since the electrical annealing greatly limits the operation lifetime of the transistor due to Joule heat induced damage to graphene. Li et al. fabricated a complementary-like graphene logic circuit, where the current transport properties of graphene were controlled by electrostatic doping. However, this technique is limited to bilayer graphene that usually has lower electron mobility and cutoff frequency than monolayer graphene. Moreover, the aforementioned techniques could not achieve stable n-type graphene in air due to its high surface sensitivity.

Therefore, the bottleneck in the fabrication of graphene-based logic circuits is the lack of a practical and reliable method for fabricating air-stable *n*- and *p*-type graphene transistors on the same sheet.

1.4 Mission and Outline

In order to address the above challenges, this PhD work presents the development of innovative techniques that are required for fabricating highly stable and reliable integrated graphene circuits. More specifically, we have developed a high-throughput and highly repeatable technique to engineer the number of graphene layers. We have also demonstrated the ability to engineer the graphene band gap by introducing nano-structures, such as nanomeshes and nanoribbons into pristine graphene. Moreover, we have investigated a polymer doping and encapsulation method to realize air-stable *n*-type graphene transistors. As a proof of principle study, we have design, fabricated, and characterized an integrated graphene invertor circuit on mechanically rigid and flexible platforms. Finally, we extended the range of graphene applications to the areas of chemical and temperature sensing.

The outline of the dissertation is given as follows. Chapter 2 introduces methods for graphene preparation, with specific focus on micromechanical exfoliation. Different techniques to identify the number of graphene layers are also discussed. Chapter 3 discusses engineering methods to control the number of graphene layers using oxygen plasma etching. In addition, methods to convert pristine graphene to semiconductors based on nanomesh and multiribbon structures are covered in this chapter. *P*-type FETs are designed, fabricated, and characterized to prove the concept. In Chapter 4, different *n*-doping techniques of thin graphene films are studied, followed by the demonstration of highly stable *n*-type FETs. Chapter 5 reports the design, fabrication, and characterization of graphene integrated circuits on both rigid and flexible substrates. Finally, Chapter 6 summarizes several potential applications of graphene, including gas sensors and flow/temperature sensors.

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2 GRAPHENE PREPARING METHODS

2.1 Introduction

High quality graphene thin films are required for making the proposed graphene transistors and nanoelectronic circuits. At present, the most commonly used methods for graphene production are micromechanical exfoliation/cleavage, epitaxial synthesis from silicon carbide (SiC) substrates, and chemical vapor deposition (CVD). This chapter provides a brief technical introduction to these three methods and compares their differences from several aspects such as graphene size, quality, and production yield. The methods to identify the layer number and quality of graphene are also discussed.

2.2 Methods to Produce Graphene

2.2.1 Micromechanical exfoliation and cleavage

Mechanical exfoliation and cleavage use mechanical energy to break weak van der Waals bonds between stacked graphene sheets in order to separate individual sheets from high-purity graphite flakes. Micromechanical exfoliation was first introduced by Novoselov and his group in 2004 [1], which typically involves a repeated peeling process. This method enables production of high-quality graphene in a very reliable and low-cost way, and thus has attracted great attention from researchers since it was invented. The exfoliation process is usually done in a clean environment to avoid any kind of contamination.

We have calibrated a robust process to exfoliate graphene samples using the KECK cleanroom facility at Michigan State University. Prior to the mechanical exfoliation, a substrate of 300 nm SiO_2 /Si (purchased from WRS Materials) was cleaned with acetone and rinsed in isopropanol alcohol (IPA) and deionized (DI) water. After drying the substrate with a nitrogen blower, two metal layers of 70 nm Au/5 nm Ti micro-markers (Figure 2.1) were

patterned on the SiO_2 substrate via photolithography, thermal evaporation, and metal liftoff processes. The minimum feature size of the markers was around 3 μm and the spacing between them was 150 μm. The purpose of these markers is to locate graphene sheets on the substrate and to use them in the alignment process of the electron beam lithography (EBL) in subsequent fabrication steps .

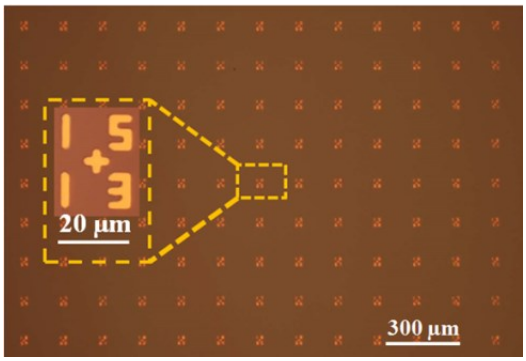

Figure 2.1 Metal markers on a SiO_2/Si substrate.

Graphene samples were exfoliated from commercially available, highly oriented pyrolytic graphite (HOPG) flakes of around 1 mm. After attaching these graphite flakes to a ~20 cm long Scotch tape with tweezers, the tape was folded to sandwich the flakes between the sticky sides, pressed to ensure a good adhesion, and then slowly peeled to cleave graphite into two layers. The tape was repeatedly folded and peeled until a very smooth layer of fine graphene sheets was achieved on the tape (Figure 2.2). After that, the tape with cleaved graphene was laid and pressed on the SiO_2/Si substrate in order to transfer graphene sheets onto the substrate. The tape was then slowly removed, leaving the graphene attached on the substrate. Finally, transferred graphene was cleaned in acetone, IPA, and DI water, and was ready for subsequent processes.

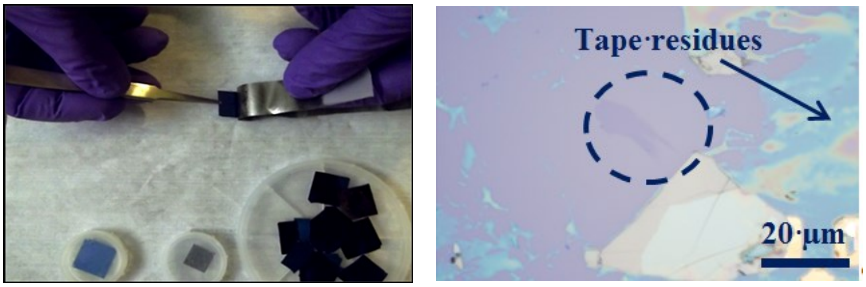

Figure 2.2 (a) Mechanical exfoliation of graphite using a Scotch tape. (b) A 300 nm SiO_2/Si substrate with transferred graphene. The dashed circle indicates a thin graphene sheet.

2.2.2 Epitaxial graphene from silicon carbide

Epitaxial growth is a commonly used technique for producing large-scale graphene from a SiC substrate. In this method, when SiC is heated to around 1400 °C in vacuum, some of the silicon atoms sublimate from the surface, which results in the formation of a graphene layer on top of the SiC substrate [2]. It has been reported that graphene transistors can be manufactured from a SiC substrate by epitaxial growth of graphene on a wafer-scale size [3]. The advantage of this method is that a device can be fabricated on a SiC substrate itself, without the need for transferring graphene to another substrate. However, graphene sheets generated by this method are non-homogeneous so the number of the layer cannot by precisely controlled, as shown in Figure 2.3. In addition, the electron mobility is limited to few thousands of $cm^2\ V^{-1}s^{-1}$ [4]. Therefore, although the epitaxial growth of exitaxial graphene is capable of preparing graphene with high throughput and large areas, it is relatively expensive and difficult to obtain uniform and high-quality graphene.

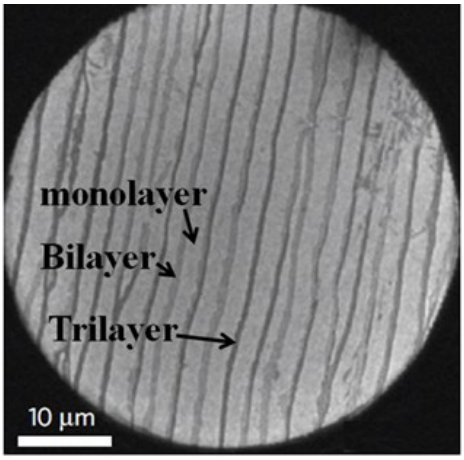

Figure 2.3 Mono-, bi- and tri-layer graphene produced by graphitization of SiC [4].

2.2.3 Chemical vapour deposition (CVD)

Another alternative method to produce graphene is a CVD method, which is capable of obtaning large graphene sheets (~1 m) [5] with reasonable good electron mobility (~10000 $cm^2\ V^{-1}s^{-1}$) [5, 6]. In the CVD approach, a copper substrate is typically used for growing graphene because copper does not absorb carbon atoms due to the weak bonds that hold the carbon atoms to copper. Consequently, carbon atoms can only form on the surface of copper. During the CVD synthesis, the copper substrate is inserted into a furnace and heated at low vacuum to around 1000 °C in order to increase the grain size. Methan and hydrogen gases are flowed through the furnace. The function of the hydrogen is to facilitate the reaction between the methan molecules and the copper substrate, which enables carbon atoms to deposit on the substrate. After that, the sample is rapidly cooled to achieve thin graphene sheets [7, 8].

One of the favorable features in the CVD method is the ability of transfering CVD graphene from coper substrate to different other substrates, such as Si, SiO_2, or polymers [5, 9]. Typically CVD graphene transfer can be accomplished by depositing a large area of polymethyl methacrylate (PMMA) on a graphene/copper foil, followed by etching the copper substrate in Ferric Cloride ($FeCl_3$). After the copper is completed etched away, the

graphene/PMMA film floating on the $FeCl_3$ solution will be cleaned with DI water and then transferred to another substrate. Finally, the PMMA can be dissolved in acetone, leaving only the graphene on the new substrate [7].

Compared to the mechanical exforliation and epitaxial growth, CVD synthesis cannot achieve high quality graphene, mainly due to surface disorder, defects, and different types of contamination (e.g. Cu residues) that require multiple cleaning processes (Figure 2.4).

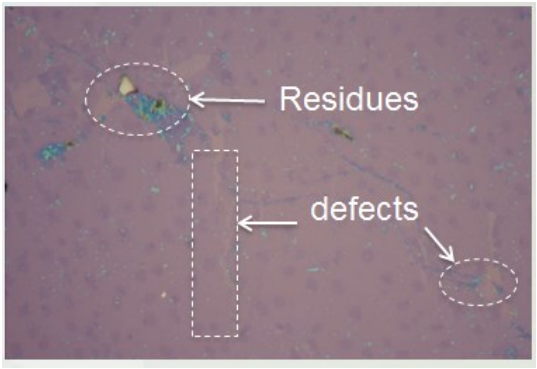

Figure 2.4 Optical microscopic image of a CVD graphene sample on a SiO_2/Si substrate.

2.2.4 Comparison of three methods

Table 2.1 compares the three representative methods for obtaining graphene films, in terms of film size, electron mobility, graphene transfer feasibility, cost, and mass production capability. Besides the abovementioned main techniques, attempts have been made to synthesize graphene through other approaches, such as un-zipping carbon nanotubes (CNTs) [10, 11], reduction of graphite oxide [12], or chemical extraction of graphene films from graphite [13, 14]. Among these methods, the mechanical exfoliation method is considered as the most effective and efficient way to produce high quality graphene films for research prototypes. For this reason, the pilot studies in this PhD work mainly use the mechanically exfoliated graphene to prove the principles.

Table 2.1 Three representative methods for producing graphene films

Method	Mechanical Exfoliation	Epitaxial growth on SiC	CVD synthesis on Ni, Cu, Fe, or Co
Size	10-100 μm	> 6 inch	> 6 inch
Mobility	Best	Bad	High
Transfer	Yes	Yes	Yes
Cost	Low	High	High
Mass production	No	Yes	Yes

2.3 Methods to Identify Graphene

The number of graphene layers is a very important factor that determines the properties of graphene. The thickness of graphene films can be differentiated using one of the three techniques: optical microscopy, atomic force microscopy (AFM), and Raman spectroscopy. Details for each method are given below.

2.3.1 Optical microscopy

Microscale graphene sheets can be visualized under an optical microscope fitted with a ×50 objective lens. The noticeable optical contrast between the graphene and the 300 nm SiO_2/Si allows for a rough estimate on the number of carbon layers [15, 16]. Theoretically, thicker graphene films have higher optical contrasts between the graphene and the substrate, which can be calculated by $C(\lambda)=R_S(\lambda)-R_G(\lambda)/R_S(\lambda)$ [17, 18], where $R_S(\lambda)$ is the reflection spectrum from the 300 nm SiO_2/Si substrate and $R_G(\lambda)$ is the reflection spectrum of the graphene sheet with a given wavelength λ. With this technique, the number of carbon layers in a graphene sheet can be determined precisely [17] by $C(\lambda)=0.0046+0.0925-0.00255N^2$, where $N \leq 10$ is

the number of carbon layers. Experimentally, the number of graphene layers can be distinguished just by the color of the graphene sheet under a high magnification optical microscope. With only little experience, one can differentiate between mono-, bi-, and few- (3 to 6) layers, and graphite (typically with more than 9 layers). Figure 2.5 shows the optical microscopic images of graphene sheets with different layer numbers. While optical microscopy is a simple and fast way to estimate the number of graphene layers, more advanced tools will be needed in order to determine the number of layer accurately.

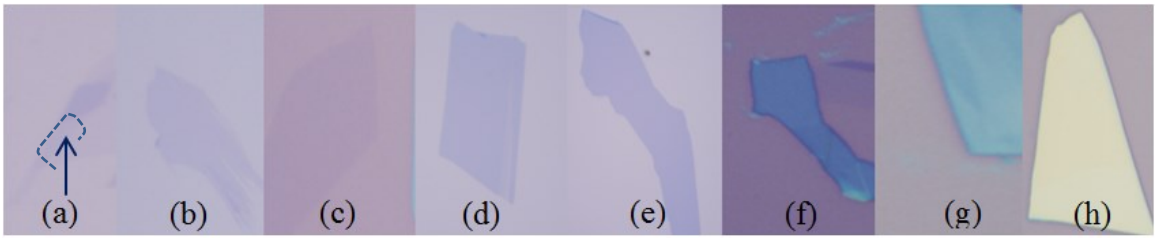

Figure 2.5 Optical microscopic images for graphene samples with different layer numbers: (a) monolayer; (b) bilayer; (c) 3 layer; (d) and (e) 4 to 6 layers; (f) to (h) more than 10 layers.

2.3.2 Atomic force microscopy (AFM)

The tapping mode technique of AFM is a commonly used method to measure the thickness of graphene on SiO_2. It also allows topographic imaging of sample surfaces with high resolution. Theoretically, since the thickness of the monolayer graphene sheet is known (0.335 nm), it is easy to determine the number of graphene layers from the total thickness measured by AFM. However, different groups have reported different thicknesses for a single graphene layer [1, 19-21] resulted from AFM measurements. We obtained similar results in our experiments, where the measured thickness of a monolayer graphene sheet was always higher than the theoretical value. As an example, Figure 2.6 shows the thicknesses of four typical monolayer graphene samples, measured by the DI 3100 AFM in the KECK cleanroom. The monolayer configuration of these samples later was confirmed using Raman spectroscopy, which will be discussed in the next section.

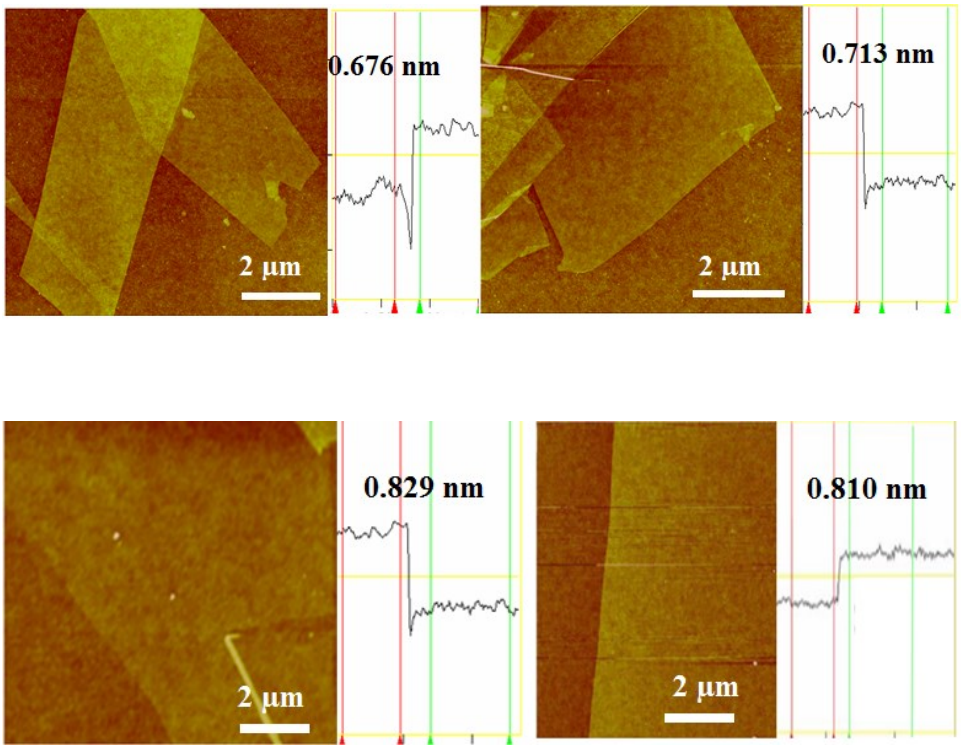

Figure 2.6 AFM (DI 3100) thickness measurements of four monolayer graphene samples. The thickness ranges from 0.676 nm to 0.829 nm.

The inaccuracy of the AFM thickness measurements can be attributed to several reasons: the folded regions in graphene [22], sample contamination, the nanoscale roughness of the SiO_2 substrate, the fluctuation in the interaction (or attractive forces) between the AFM tip and the different surfaces when scanning the across graphene and SiO_2 surfaces [23], and finally an unclean or worn AFM cantilever. Hence, it is relatively difficult to determine the exact number of graphene layers by just relying on the AFM method.

2.4 Raman Spectroscopy

Raman spectroscopy is based on inelastic scattering of laser light, meaning that the frequency of photons in laser changes due to interaction with a sample. Particularly, this interaction generates electric dipole moment that deforms the molecules of the sample. Consequently, the laser photons reemit with a shift in the original frequency that provides information about

the vibration of the molecules in the sample (phonons) [24]. Figure 2.7 (a) shows typical Raman spectra of several graphene sheets with various thicknesses. The Raman spectra were obtained from a YAG laser (λ=532 nm) with the laser power of 0.53 mW. The most significant Raman characteristic peaks of graphene are G band at ~1580 cm^{-1} and second D (2D) band at ~2700 cm^{-1} [25]. The G band is generated due to the doubly generated optical phonons, in both longitudinal and transverse modes, at the center of the Brilloun zone [26, 27]. These modes are high frequency modes, corresponding to the vibration frequency of atoms in the unit cell against each other. As shown in Figure 2.7 (a), the peak of the G band in graphene increases as the graphene thickness increases, simply because of the increment of carbon atoms. Hence, the peak of the G band can be used to determine the number of graphene layers [25].

The other significant band in the Raman spectrum is the 2D band. As depicted in the same figure, the peak of the 2D band is the key point to differentiate the mono-, bi-, tri- and few-layers of graphene sheets. In the monolayer graphene, the 2D peak is sharper and stronger than the G peak. Whereas the 2D peak of the bi-layer graphene has four edges (Figure 2.7 (b)) and its intensity is close to that of the G peak. It is also observed that the 2D peak of the tri-layer graphene contains only two edges and the peak intensity is close to that of the G peak. Furthermore, it is relatively difficult to differentiate graphene sheets with four to six layers, because they have similar shapes in their 2D peaks, with the typical peak intensity I_{2D} of around 70% of the G peak intensity I_G. For graphene sheets with more than six layers, the shape of their 2D band becomes closer to the 2D shape of graphite. Basically, as the number of graphene layers increases, new electronic bands will be generated, which leads to more electron-phonon interactions and thus different peaks appear accordingly.

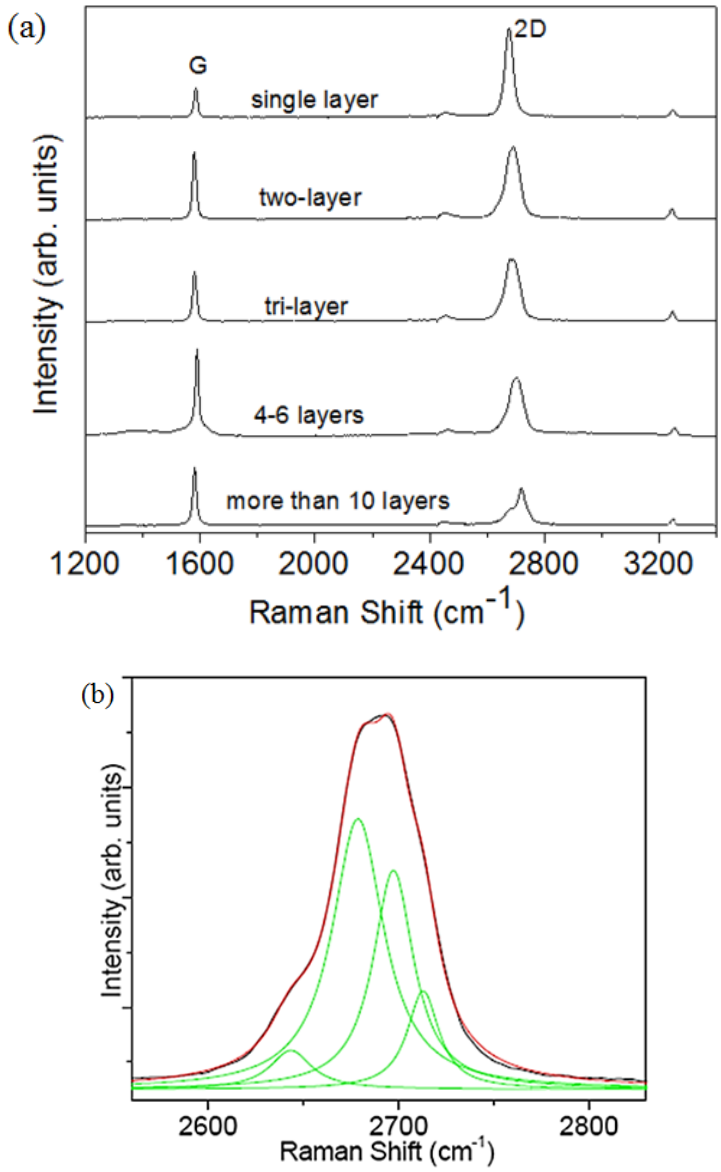

Figure 2.7 (a) Raman spectra of different numbers of graphene sheet layers obtained using HoloProbe Micro-Raman Spectrograph; (b) The 2D band Raman spectrum of a bilayer graphene sheet, showing 4 edges in one big peak.

As another important observation in Figure 2.8, a new band in ~1350 cm^{-1}, denoted as D, arises when the graphene surface has defects or mechanical deformation. The intensity of the D band increases with the increasing defect level of the graphene surface [28, 29]. The

defects can be classified as missing atoms, dangling or dislocation bonds in the carbon lattice. It is of note that, with the increasing number of graphene layer, the D-band intensity I_D can be seen to dramatically decline relative to the G-band intensity I_G, which is possibly due to the increase in rigidity of the thick graphene samples [30].

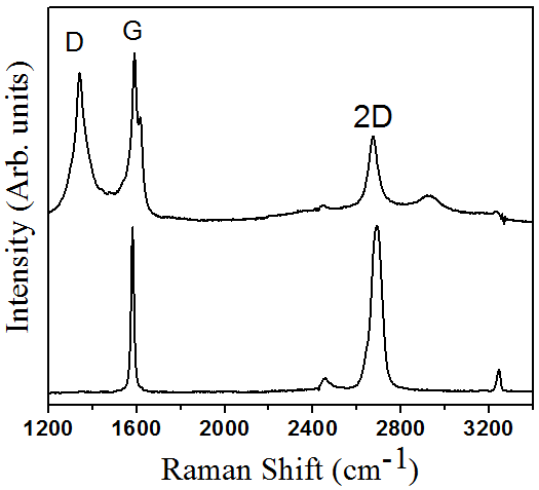

Figure 2.8 Raman spectra of a same graphene sample before and after introducing defects using O_2 plasma with 70 W RF power for 19 sec. The D band appeared as a result of surface defects.

2.5 Graphene Cleaning Method

As discussed earlier in this chapter, we mainly used the mechanically exfoliated graphene in our experiments. One major drawback of the mechanical exfoliation is that it leaves a lot of tape residues on the graphene surface and the SiO_2 substrate, which significantly reduce the carrier mobility of graphene [31, 32]. We found that the tape residues can be removed effectively by annealing the as-transferred graphene at 400 °C in Ar (97%) /H_2 (3%) atmosphere for 1 h. The gas mixture was introduced into the annealing furnace with the flow rate of 2000 sccm. Figure 2.9 shows the AFM images of a monolayer graphene sample before and after the cleaning treatment. It can be seen that after the annealing, the graphene appeared

with a smoother surface on the substrate, mainly due to the removal of surficial contamination and the recovery of defects. The measurement of the sheet thickness, after cleaning, is closer to the thickness of the reported monolayer graphene (~0.7 nm).

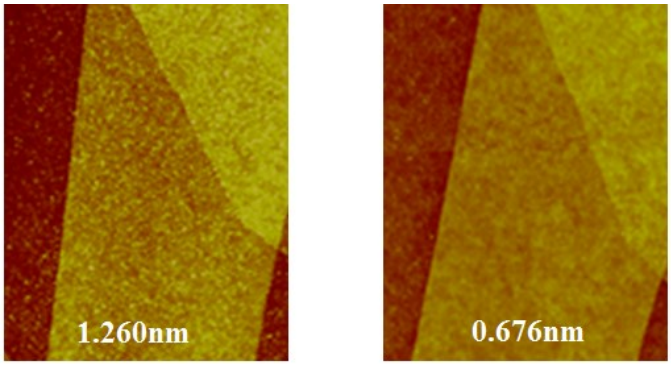

Figure 2.9 AFM images of a monolayer graphene before (left image) and after (right image) a heat treatment for removing tape residues. The sheet thickness decreased from 1.260 nm to 0.676 nm after cleaning.

After the cleaning process, the sample was checked by a Raman spectroscope to investigate the effect of Ar/H_2 annealing on the graphene sheet. As shown in Figure 2.10, the intensity ratio I_{2D}/I_G was decreased from 2.4 to 1.27, indicating that the graphene surface has been doped after the heat treatment. In addition, the defect peak was suppressed after annealing, due to the defect recovery in an H_2 environment. The graphene doping perhaps is due to the adsorption of hydrogen atoms on the graphene film [33, 34]. However, this doping source does not show a significant impact on graphene electronic properties since the H_2 concentration is only 3%. The chemical doping of graphene will be discussed in details later in Chapter 4.

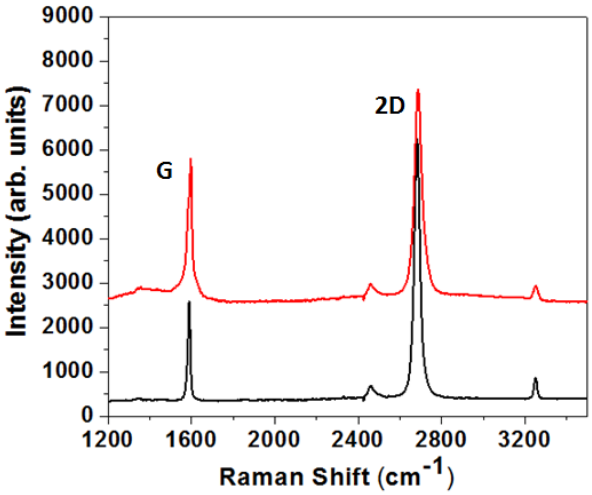

Figure 2.10 Raman spectra of a monolayer graphene sample before (black color) and after (red color) the cleaning treatment.

2.6 Conclusion

In conclusion, graphene produced via CVD is not as high quality as via mechanical exfoliation due to surface disorder, defects, in addition to the different types of contamination that require multiple cleaning processes. Therefore, the studies in this thesis will use mechanical exfoliation for graphene preparation.

Raman spectroscopy is the best method to identify graphene compared to the AFM and optical microscopy methods. On the other hand, optical microscopy technique resembles a fast and cheap tool to visualize thin graphene, but experience is required for identifying the number of graphene layers.

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3 ENGINEERING OF GRAPHENE SHEET

3.1 Introduction

In this chapter, two technologies will be discussed for controlling graphene electronic properties. The first section describes a controllable post-synthesis method for engineering the number of graphene layers. The second section presents a fabrication technique of graphene nanostructures, including graphene nanomesh and graphene multi-ribbon, for tuning the band gap of graphene.

3.2 Layer Engineering of Graphene Sheets

3.2.1 Background

As mentioned in Chapter 2, significant progresses have been made in producing graphene with both high yields and big sizes. However, a challenge remains to generate graphene with the desired number of layers. The ability to control the number of graphene layers is critical for the reproducibility of graphene-based devices in practical applications as well as for the fundamental study of graphene characteristics. Especially, the layer engineering of graphene will contribute greatly to the in-depth understanding of inter-layer transport properties in an inter-layer structured graphene sensor that will be discussed in Chapter 6. The influence of the number of graphene layers on graphene's electronic and optical properties has also been reported [1].

Over the past years, several efforts have been made towards the realization of the layer engineering of graphene [2-5]. For example, Tour *et al*. [6] reported the layer-by-layer removal of graphene sheets with a wet etching method by sputtering zinc on graphene surfaces and dissolving the zinc with diluted acid. This method provides a promising method for engineering the number of graphene layers, but the requirement of acid treatments makes

this method incompatible with conventional microelectronics manufacturing techniques. Recently, the atomic layer etching of graphene was also reported by oxidization of carbon sp^2 bonds to sp^3 bonds with oxygen radicals and the consequent bombardment with argon atoms [7]. Although this technique allows for the singular sheet etching of graphene, a large amount of defects could be introduced to the graphene due to the combination of radical oxidation and argon atom bombardment.

We proposed a simpler and less invasive method for engineering the number of graphene layers with pure oxygen plasma etching. By carefully tuning the variables of the oxygen plasma etching (e.g. power, oxygen flow rate, operating pressure and process duration), we were able to achieve "singular sheet etching" (SSE) of graphene, which removed only one graphene sheet at a time with both the powered electrode and ground electrode oxygen plasma. Due to the fact that plasma strength at the ground electrode is lower than that at the powered electrode, the "singular sheet etching" by the ground oxygen plasma can potentially introduce relatively less amount of defects to graphene. As a technical demonstration, monolayer graphene was produced from bilayer graphene by the "singular sheet etching" processes. Technical details will be discussed in the following sections.

3.2.2 Singular sheet etching method

Graphene flakes were produced with mechanical exfoliation from highly oriented pyrolytic graphite (HOPG) flakes and then transferred onto a Si substrate with a 300 nm thick SiO_2 layer. Optical microscopy and Raman spectroscopy (HoloProbe Micro-Raman Spectrograph) were used to locate and identify single- and double-layer graphene samples. Prior to oxygen plasma etching, the samples were cleaned with acetone rinse for 5 minutes, followed by an annealing process. The annealing treatment was carried out at 400 ^{o}C in an argon and

hydrogen (3% in volume percentage) atmosphere for 1 hr. It should be noted that the acetone rinse is used to remove tape residues and other organic contaminations prior to the annealing. Following the acetone clean, the graphene samples were rinsed with isopropanol alcohol and then DI water to remove the acetone residue so the chemical effect on graphene doping is negligible.

The SSE of graphene with oxygen plasma was conducted in a plasma etching system (March, PX-250) under the following conditions: RF frequency of 13.56 MHz, RF power of 70 W, oxygen flow rate of 10 sccm (standard cubic centimeter per minute), base pressure of 70 mTorr, and processing pressure of 313-326 mTorr. The etching durations were fine-tuned after a large amount of experiments and varied according to the location of graphene samples (at a powered electrode or ground electrode). Specifically in our plasma etching system, the powered electrode refers to the electrode plate that is connected to an RF bias, while the ground electrode plate is connected to the inner wall of the vacuum chamber and also to the ground of the etching system. Figure 3.1 shows the experimental setup of the SSE of graphene on the ground electrode. Since the strengths of oxygen plasma at the two electrodes are different, the etching effects on graphene may vary. The ground and powered electrodes are made of aluminum and have dimensions of 7 in. × 8 in. ×0.093 in. The distance between a ground electrode and the powered one is 2 in. It is clear that the intensity of plasma is higher in the powered electrode than the ground ones based on the brightness. The gentle plasma generated on the ground electrode explains why it required longer time to etch a single layer and generated fewer defects as confirmed later.

The process durations for single sheet removal of graphene were carefully tuned after a large number of experiments and varied according to the location of graphene samples (at powered electrode or ground electrode). AFM and SEM (scanning electron microscope, Hitachi-4700)

were used to inspect the surface topologies of graphene samples before and after being treated with oxygen plasma. Micro Raman spectroscopy was used to identify the number of graphene layers as well as to study quantitatively the defects of the plasma treated graphene samples.

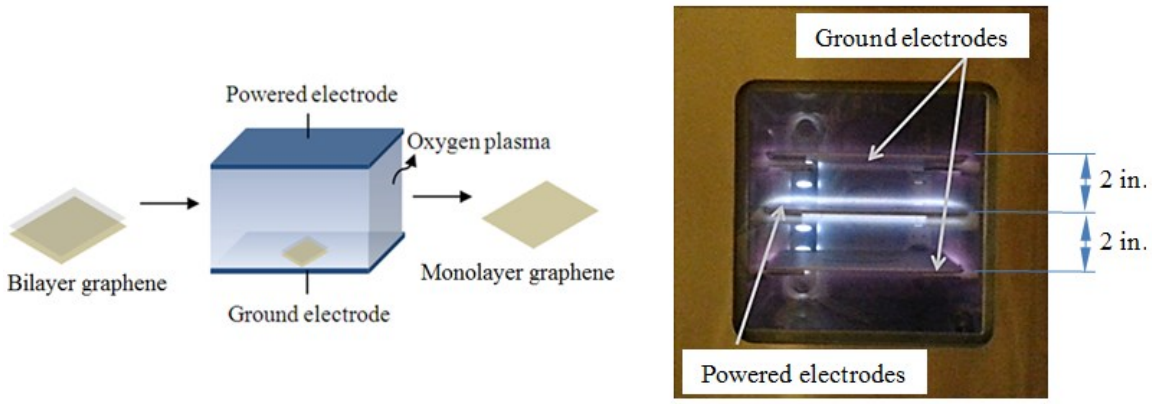


Figure 3.1 Conceptual schematic and experimental setup of the layer engineering process with oxygen plasma. The etching process can be performed with either the ground electrode oxygen plasma at the ground electrode or the powered electrode.

3.2.3 Results of graphene singular sheet etching

To validate the efficacy of the SSE method, both mono- and bi-layer graphene films were subjected to oxygen plasma etching for different process durations. The etching time was increased by a step of 2 seconds. AFM, SEM, and Raman spectroscopy were used to investigate graphene surfaces after each step. Figure 3.2 shows the evolution of a graphene duration of 38 seconds. In this case, the graphene sample started with both a sample upon the singular sheet etching with the ground oxygen plasma for optimum process monolayer region and a bi-layer region that were identified with Raman spectroscopy (Figure 3.2 (a)). After a "singular sheet etching" step, the monolayer region was completely removed, while the bilayer region was thinned down to a monolayer graphene, as shown in Figure 3.2 (b). By carefully comparing Figure 3.2 (a) and (b), it can be seen that the border (the upper edge) of

the bilayer region did not change obviously, which implies that the edges are not a preferred direction during the etching process. After the second etching, the bilayer region was completely etched away (Figure 3.2 (c)), leaving the SiO_2/Si substrate. Graphene residues were found at the boundary between the monolayer and bilayer regions, which were resulted from thicker graphene fragments and folded graphene edges (> 2 layers) around the boundary.

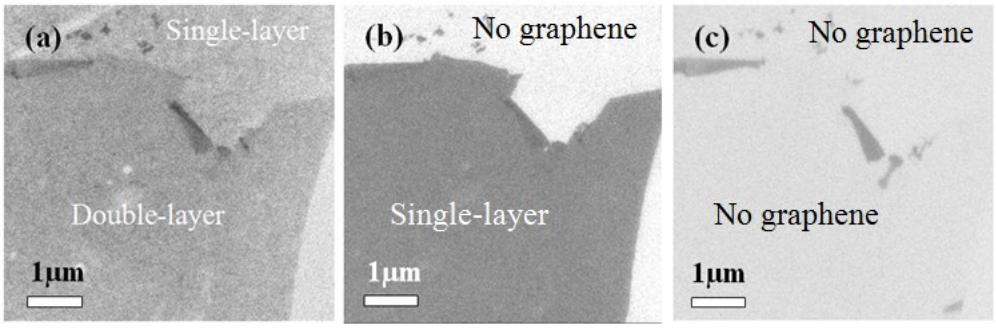


Figure 3.2 SEM images show the evolution of a graphene sample after each "singular sheet etching" step with ground electrode oxygen plasma: (a) as-produced; (b) after the first "singular sheet etching" step; (c) after the second "singular sheet etching" step.

To further demonstrate the repeatability and controllability of the SSE method with the ground electrode plasma, we applied the same recipe to several bilayer graphene samples and successfully obtained monolayer graphene sheets from the bilayer ones, as verified by AFM and Raman spectroscopy. Figure 3.3 shows the evolution of a representative bilayer sample when being subjected to the "singular sheet etching" process. After the first "singular sheet etching" (Figure 3.3 (b)), while the SEM and AFM images had no distinguishable difference between the untreated graphene and the treated one, their Raman spectra and AFM profiles clearly showed the changes caused by plasma etching. Particularly, the thickness of the bilayer graphene decreased from ~1.259 nm to ~0.810 nm, resulting in an apparent difference of 0.449 nm. Graphene thickness measurement using an AFM is typically not atomically precise due to sample contamination and/or an unclean or worn AFM cantilever. The step

size 0.449 nm is slightly larger than 0.335 nm (one layer) but obviously much smaller than 0.670 nm (two layers), indicating the removal of one atomic carbon layer. The 2D band of its Raman spectrum comprised only one Lorenzian peak, which is another indicator of a monolayer graphene. After the second etching step (Figure 3.3 (c)), the SEM and AFM images taken from the same regions indicates that the bilayer graphene was completely removed with only folded thicker portions of the graphene left on the substrate. This was further confirmed with the Raman spectrum taken from the same location, which contained no specific peak of graphene.

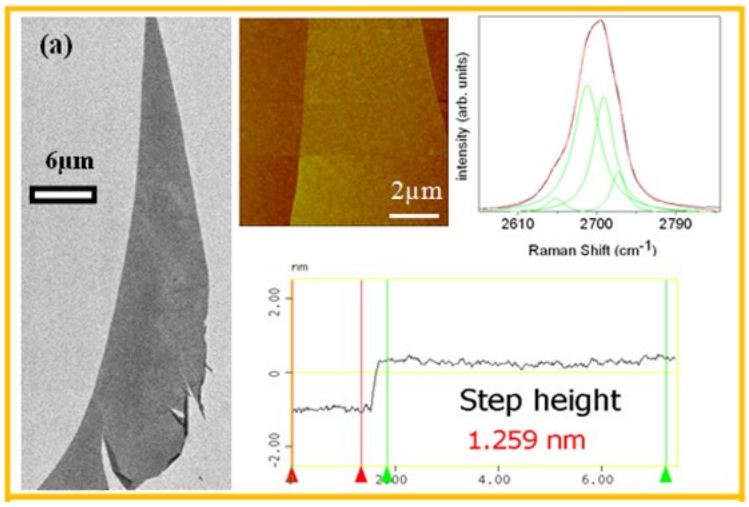
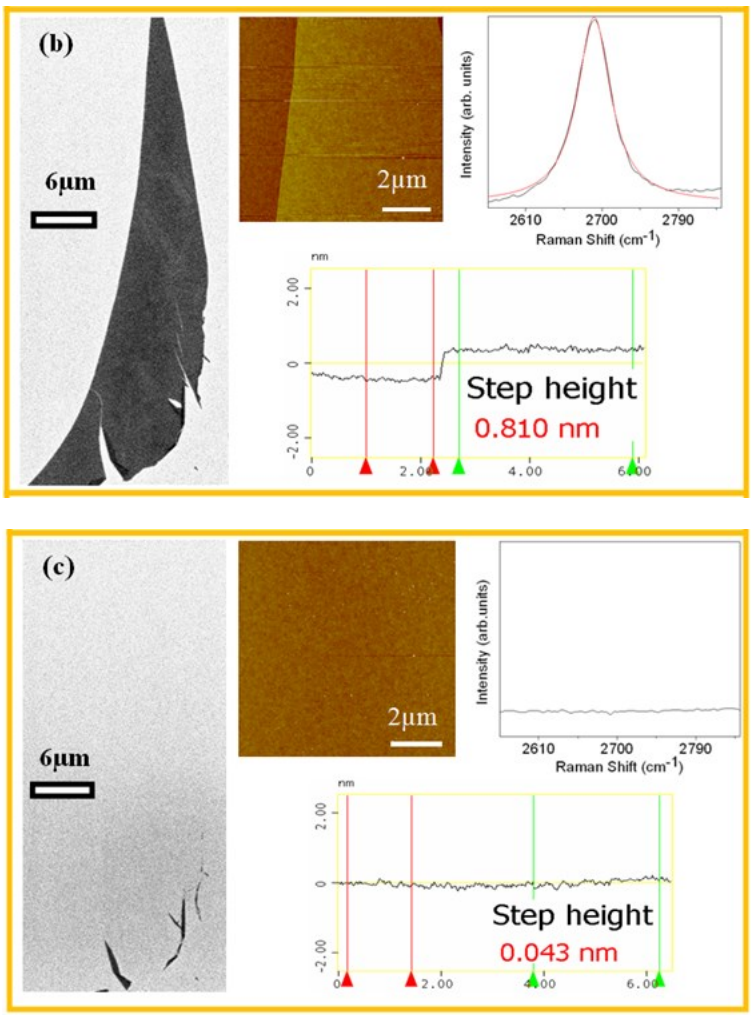


Figure 3.3 Demonstration of producing a monolayer graphene from a bilayer graphene using the SSE method. (a), (b), and (c) show the SEM image, AFM image (up left panel), 2D band of its Raman spectrum (up right panel) and its height profile from the AFM image (bottom panel) before being etched with oxygen plasma (a), after the first "singular sheet etching" process (b), and after the second "singular sheet etching" process (c), respectively.

Figure 3.3 (cont'd)



We have demonstrated that the SSE of graphene can be realized with the oxygen plasma, but it still remains unclear how the oxygen plasma interacts with graphene. An answer to that question is essential for further understanding the effects of oxygen plasma on the remaining graphene sheets after the etching process. Two possible etching mechanisms include isotropic etching and anisotropic etching. If the single sheet removal of graphenes by oxygen plasma is isotropic, the etching rate should be uniform everywhere on a graphene sheet regardless of graphene defects and edges. Initiatively, when a single atomic layer is removed from the top, a single or a couple of chains of atoms at the edge will be removed. This is because removing an atom from the top will need sufficient energy to break three bonds, while at the edges,

only one or two bonds need to be broken due to the existence of dangling bonds. That means the etching cannot be an isotropic process. For graphene sheets, there are two possible preferred directions for anisotropic etching: vertical (top surface) and horizontal (edges). Experimentally, it is possible to detect a removed single layer using Raman or optical microscopy, but the loss of a couple of chains of atoms at the edge is beyond the resolution of these instruments. Consequently, the sizes of the graphene sheet and the defective regions will not change during the etching in the case of anisotropically vertical etching, but will be projected to the bottom graphene sheet after the etching process, as illustrated in Figure 3.4 (a). While in the anisotropically horizontal etching mode, the etching rates at the graphene edges and defective regions are anticipated to be higher than that at other intact regions since the edges/defects of graphene tend to react faster with chemicals (e.g. oxygen plasma) than pristine graphene [8]. As schematically displayed in Figure 3.4 (b), the defective regions of the top graphene sheet will expand, resulting in larger defective areas on the bottom sheet after the etching process. Additionally, the size of the graphene sheet will shrink due to the anisotropic etching of oxygen plasma.

Experiments were conducted in order to investigate which one of these two possible mechanisms will better explain the single sheet removal of graphene. In this study, the etching rate of graphene was relatively fast and the time interval was too short, making it difficult to control the etching time accurately on the same graphene sheet. Therefore, different monolayer graphene samples were etched for various plasma durations and inspected with SEM to evaluate the time evolution of oxygen plasma etching. Etching conditions, such as RF power, oxygen flow rate and working pressure, except the process duration, were kept the same for each sample. Figure 3.4 (c)-(e) show the SEM images of three monolayer graphene samples before and after being etched by the oxygen plasma at the ground electrode with the plasma durations ranging from 28 s to 32 s. It can be seen that, first,

no noticeable area expansions of defective regions in the monolayer samples were observed during the etching. Second, no remarkable shrinkage of the monolayer graphene dimensions due to the possible faster etching rates at the graphene edges was observed during the etching processes. These results suggest that the single sheet removal of graphenes by oxygen plasma is most likely anisotropically vertical etching.

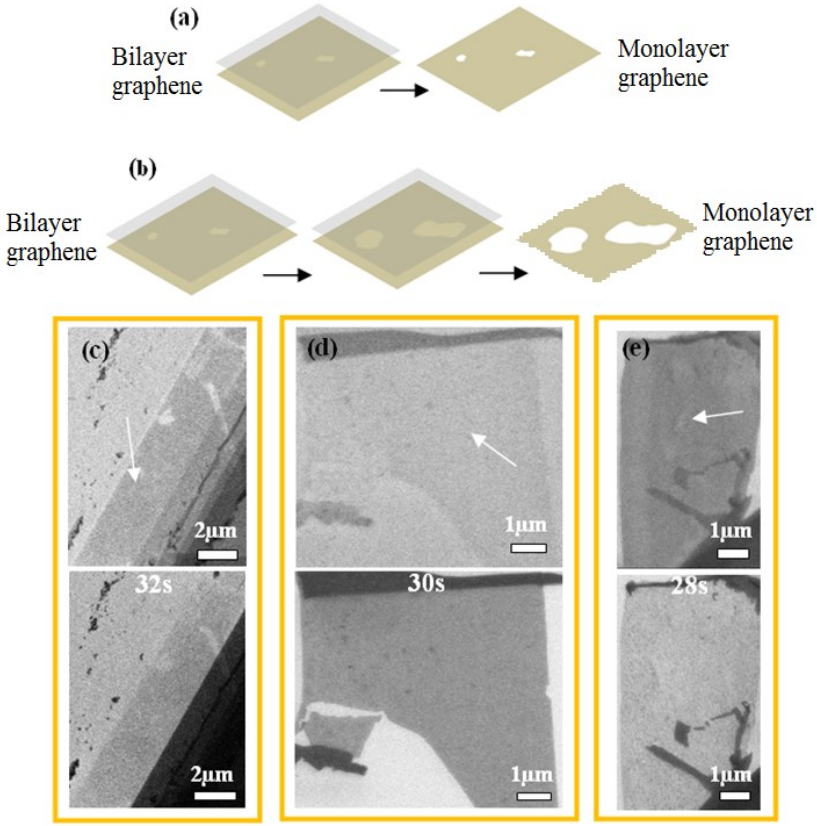


Figure 3.4 Schematic cartoons show two possible etching mechanisms of ground electrode oxygen plasma: (a) anisotropic vertical etching and (b) anisotropical horizontal etching. Illustrations (c)-(e) show the SEM images of monolayer graphene samples before and after being subjected to oxygen plasma etching for 32 s, 30 s and 28 s, respectively. The monolayer regions of the graphene samples were marked with arrows. In each sub-figure, the top and bottom SEM images show the graphene sample before and after being etched with the corresponding process duration, respectively.

With a similar means of investigation, singular layer etching of graphene can also be achieved with oxygen reactive ion etching at the powered electrode for a shorter etching duration of 17 seconds. Figure 3.5 provides the demonstration of a monolayer graphene produced from a bilayer graphene using the oxygen reactive ion etching. A ~0.4 nm thickness decrease of the graphene was observed after one SSE plasma treatment. The evolution of its Raman 2D band also demonstrated that a monolayer graphene was produced from the bilayer graphene.

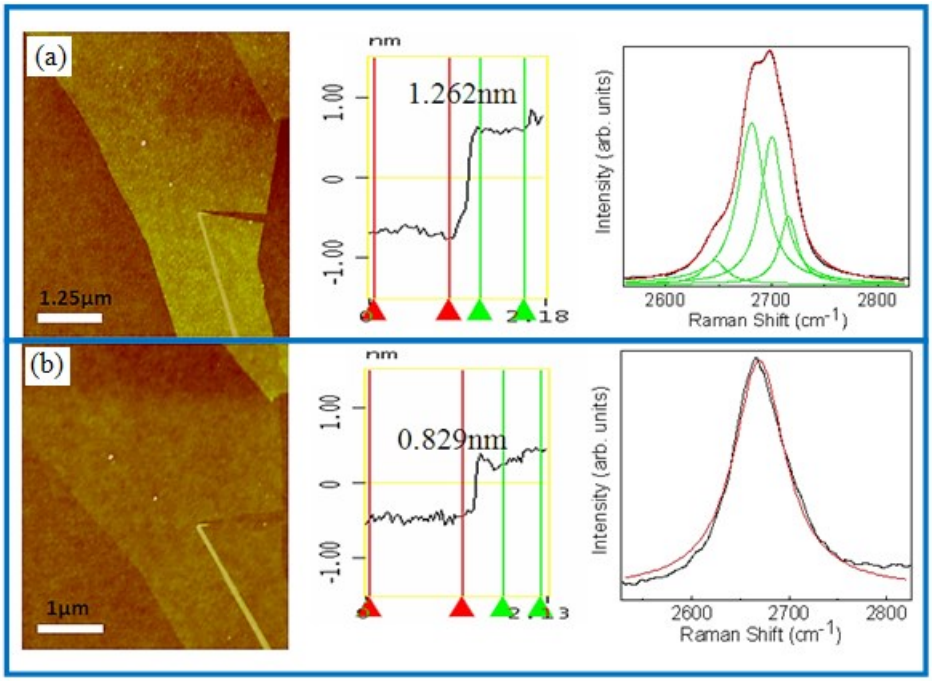


Figure 3.5 AFM images, height profiles, and the 2D bands of its Raman spectrum of a bilayer graphene (a) before and (b) after the SSE with powered electrode oxygen plasma, demonstrating the formation of a monolayer graphene from a bilayer graphene.

It is known that the strength of oxygen plasma varies at the powered electrode and the ground electrode (as shown in Figure 3.1), which is anticipated to result in different levels of physical damage and defects on the post-etch graphene sheets. Therefore, we investigated the plasma induced defects on a variety of plasma-treated graphene samples by measuring the intensity ratios of the D band and G band (I_D/I_G) in their Raman spectra. A higher I_D/I_G ratio

indicates a larger number of defects. Figure 3.6 (a) and (b) show the Raman spectra taken from two bilayer graphene samples before and after SSE by the oxygen reactive ion etching and the oxygen plasma etching, respectively. The Raman spectra show that the sample etched with the oxygen reactive ion etching at the powered electrode had an I_D/I_G ratio of ~1.18 (the bottom panel of Figure 3.6 (a)), while the I_D/I_G ratio of the graphene etched with the oxygen plasma at the ground electrode was ~0.94 (the bottom panel of Figure 3.6 (b)). The statistical analysis of the Raman I_D/I_G ratios of multiple plasma treated samples was summarized in Figure 3.6 (c). The average I_D/I_G ratio of graphene samples after etching with the powered electrode oxygen plasma was ~1.05, while the average I_D/I_G ratio after etching with the oxygen plasma was ~0.86. These results indicate that the oxygen plasma introduced fewer defects compared to the powered electrode oxygen plasma, which is mainly due to the relatively low strength of oxygen plasma at the ground electrode.

Furthermore, it is found that the amount of defects can be reduced significantly with a post-etch annealing treatment. The annealing process was carried out in an Ar environment at 900-1000 °C for 1h. Figure 3.6 (d) shows the Raman spectrum of a monolayer graphene, which was produced with the SSE method, after the annealing process. Compared with its Raman spectrum before the annealing process, which was shown in the bottom panel of (a), it can be seen that the intensity of the D band peak has been greatly suppressed by the annealing process. The recovery of disordered graphene by high temperature Ar annealing may be related to the thermally induced reconstruction of graphene lattice and dangling bonds [9] as well as graphene dehydrogenation [10]. It should be mentioned that electron beam irradiation during the SEM step is known to have effects on the transformation of the crystalline order and electronic properties of mono/bilayer graphene films [11]. During our quantitative studies of defects, the as-etched graphene samples were examined only by the micro Raman

spectroscopy in order to eliminate additional defect formation due to the electron beam irradiation. Therefore, the formation and partial recovery of defects on our graphene substrates are mainly attributed to the oxygen plasma etching and their successive annealing treatment.

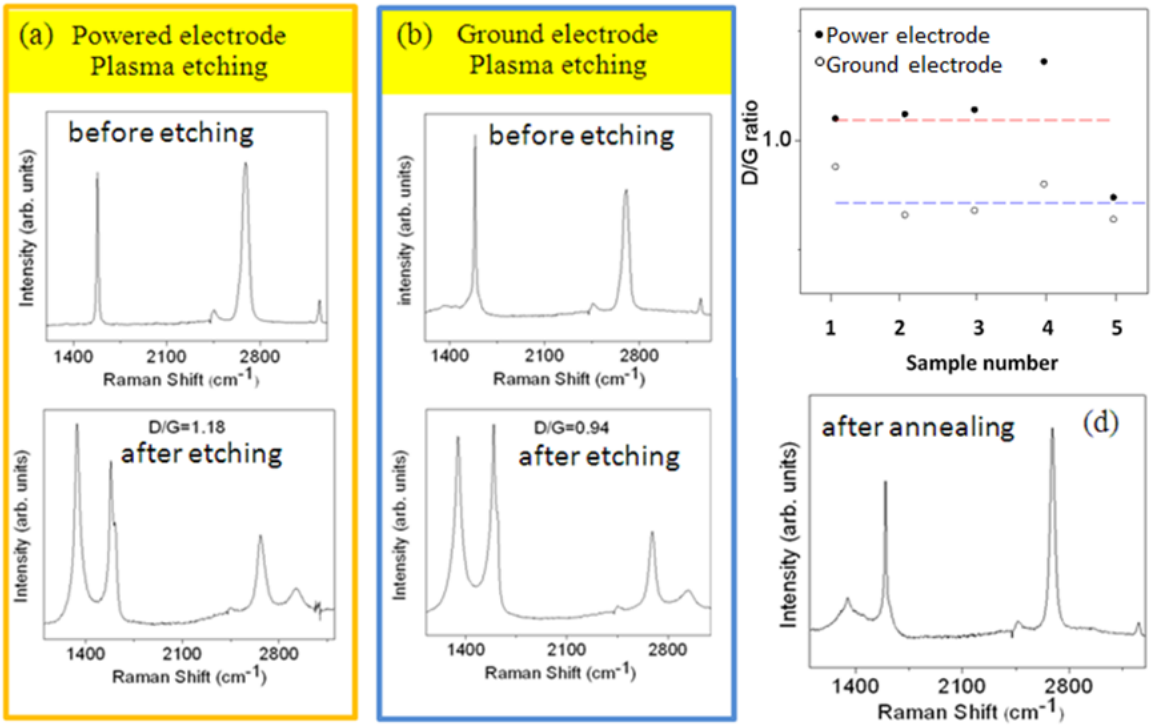


Figure 3.6 Raman spectra of bilayer graphene samples before and after the SSE process with (a) the powered electrode oxygen plasma and (b) the ground electrode oxygen plasma. (c) Statistic analysis of Raman I_D/I_G ratios of graphene samples after being etched with the powered electrode (solid circles) and the oxygen plasma (open circles). The red and blue dotted lines show the average values of data from solid and open circles, respectively. (d) Raman spectrum of a monolayer graphene sheet produced from a bilayer graphene sheet after the annealing treatment. Its Raman spectrum before annealing is shown in the bottom panel of (a).

3.2.4 Application of the SSE method

Our singular sheet etching process is completely compatible with microelectronics manufacturing techniques and shows the prospect of being a promising post-synthesis

method for engineering the number of graphene layers and producing graphene thin films with large sizes and high yield. We have also explored the application of this method in patterning several specific graphene structures, including an inter-layer graphene structure that will be discussed in Chapter 6 and a suspended thin graphene structure which will be discussed briefly below.

The remarkable electron mobility of suspended graphene (200000 cm^2/V s) makes it candidates for future nano electronic devices. To produce suspended graphenes, several methods have been reported. For example, Tombros *et al.* [12] constructed suspended graphene structures using pillars of lift-off resist (LOR) polymer as supports. Wet etching technique has also been explored to remove SiO_2 underneath graphene patterns [13]. However, in these approaches, critical-point-drying must be used in order to avoid the surface tension-induced collapse of the suspended graphene structure. Presently, a simple and reliable method to achieve large area suspened graphenes is still unavailable. Motivated by the limits of the existing methods, we have applied our SSE method in controlling the number of layers in the case of suspended graphene.

In this approach, tranches were made on the SiO_2 (300 nm)/Si substrates through photolithography and induced coupled plasma reactive ion etching (ICP-RIE), respectively. First, SiO_2 was completely removed and Si substrate was etched down by around 10 μm. Next, graphene layer was prepared using michromechanical exfoliation and then deposited over the tranches and the holes. After that, graphenes were located by optical microscope and Raman spectroscope. Then graphene layer was etched layer-by-layer using oxygen plasma, showing that the SSE method provides a possible way to produce graphenes directly from graphite flakes. Figure 3.7 shows a suspended graphene sheet with a thickness of ~2 nm

produced through layer by layer etching of a graphite flake of an original thickness of ~15 nm.

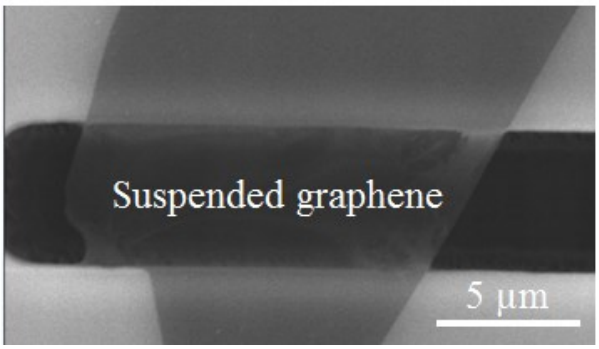


Figure 3.7 An SEM image of a 2-nm-thick suspended graphene film produced from graphite flake of ~ 15 nm using layer-by-layer oxygen plasma etching. Inset is the Raman spectra.

3.3 Band Gap Engineering of Graphene

3.3.1 Background

Pristine graphene is known to be semi-metallic with a zero band gap at room temperature, as discussed in Chapter 1. Therefore, an engineering approach must be developed to open the band gap in order to achieve desired semiconductor properties of grapheme for electronics fabrication. Recent studies have shown that the graphene band gap can be tuned by either modifying pristine graphene with dopants [14] or constructing specific structures such as nanoribbons [15-17] or nanomeshes [18-25]. However, field effect transistors (FETs) based on a single graphene nanoribbon often suffer from low driving current and conductivity [15].

Compared to nanoribbon, graphene nanomesh (GNM) is a more practical structure to effectively open the graphene band gap while allowing a favorably high driving current of the graphene FETs. Several fabrication techniques have been implemented to make the GNMs. For example, Bai *et al.* created sub-100-nm nanoholes on graphene using a block copolymer lithography method, in which a poly(styrene-*block*-methyl methacrylate) (P(S-*b*-MMA)) block copolymer thin film with cylindrical domains normal to the graphene surface was used

as the template of reactive ion etching (RIE) [15]. Self-assembled monolayers of colloidal microspheres were also exploited as the template to fabricate the GNMs [19, 26]. However, these approaches involve RIE or hydrofluoric acid (HF) to etch the SiO_2 mask layer and also the Si/SiO_2 substrate to make the GNMs, which might induce a leakage current into the back gate or even result in a short circuit between electrodes and the back gate of the GNM transistor. Alternative methods using chemical vapor deposition (CVD) of nanomesh graphene on porous MgO or Cu foil templates have been developed by several groups [20-22]. These methods, however, still require specific templates and expensive instrumentation (CVD), thus increasing the complexity and the cost of device fabrication. Recently, Zeng *et al.* reported a method for fabricating the GNM on a large area, simply using an anodic aluminum oxide (AAO) membrane as an etching mask [23]. However, the hole size and neck width of the GNM were determined by the prefabricated AAO mask and cannot be easily adjusted without changing the mask. The transistor fabricated with this method also showed a relatively low ON/OFF ratio. Other methods have also been explored for making the GNMs, such as local catalytic hydrogenation of carbon by Cu nanoparticles [24] and local photo degradation of graphene oxide at the tip of ZnO nanorods[25]. Nevertheless, precise control of the hole size and neck width of the GNMs in the current approaches still remains a challenge, increasing the demand for a new technology.

3.3.2 E-beam patterning method to engineer graphene band gap

To overcome this challenge, we propose a template-less technique based on direct electron beam (e-beam) lithography (EBL), which allows precisely controlled, high-throughput, low-cost fabrication of periodic nanomeshes on a large graphene sheet. Typically EBL processes use nanometer pattern generation system (NPGS) software to optimize the writing parameters through a run file editor. Two kinds of files are usually prepared: an alignment file and a

writing file. Our method is different from the conventional EBL process by utilizing only the alignment mode to directly write nanoholes on EBL resist. Such nanoholes can then be transferred onto the graphene sheet using oxygen plasma etching through the EBL resist mask. Figure 3.8 shows the conceptual schematic of our approach for making nanopatterned graphene FETs. This approach takes advantages of automation and high precision of EBL instrumentation and thus enables batch production of graphene nanomeshes or nanoribbons with high repeatability. The hole size and neck width of the nanomeshes can be controlled precisely by manipulating EBL processing parameters such as e-beam current, scanning area, e-beam resist thickness, and number of scanning cycles.

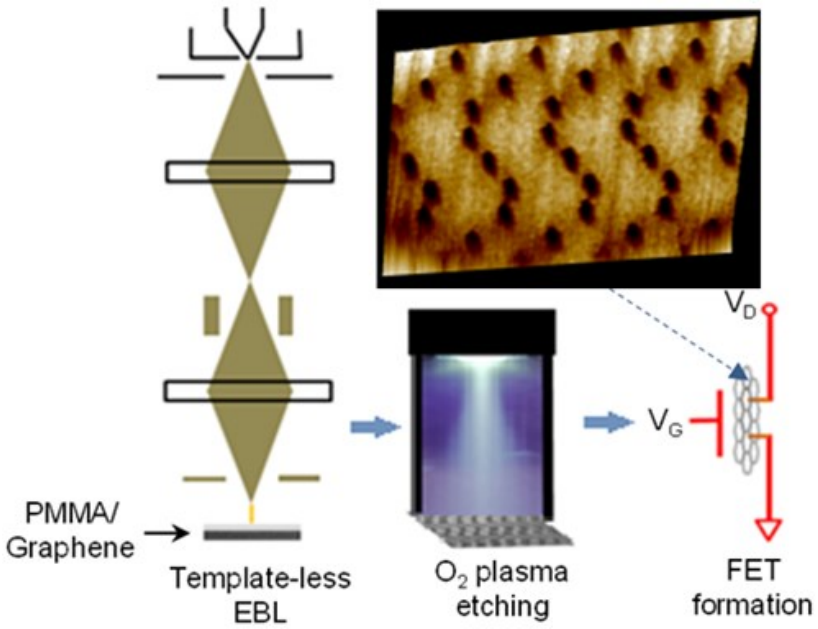


Figure 3.8 Conceptual diagram of the proposed template-less technique for fabrication of graphene nanopatterned FET transistors.

Monolayer and fewlayer (~ 4-9 layers) graphene sheets were used in this study. The graphene samples were prepared with a micromechanical exfoliation method and transferred onto SiO_2 (300 nm)/Si substrates. Ti/Au markers had been previously fabricated on the surface of the

SiO_2 substrate via thermal evaporation, photolithography patterning, and metal lift-off processes. These markers allowed one to easily identify the locations of thin graphene sheets on the substrate (as discussed in Chapter 2). After locating the graphene sheets on the substrate via optical microscopy, micro Raman spectroscopy was used to analytically determine the number of layers of the graphene sheets, based on the intensity, shape and position of G and second-order 2D bands of their Raman spectra. The chips with the graphene sheets were then annealed at ~ 400 °C in an Ar/H_2 environment for 1 hr to remove the tape residues. The hole engineering of the graphene sheets was performed with an EBL system (JEOL 840A, JEOL Ltd.) based on the aforementioned unconventional e-beam writing method.

The hole size and the neck width are the two key factors to control the dimensions of the GNMs, which determine the size of the band gap and thus the electrical properties of the nanopatterned graphene semiconductors [15, 16]. Therefore, we investigated several important processing parameters in order to fully control the hole size and the neck width in the poly(methyl methacrylate) (PMMA) resist layer. It is well known that the acceleration voltage affects the electron beam width such that a higher acceleration voltage leads to a thinner e-beam, thus smaller holes in the EBL process. Specifically in our experiment, the accelaration voltage remained a constant at 35 kV, which was set based on the previous calibration of the EBL instrutment. Other EBL parameters included the e-beam current, the scanning area, the resist thickness, and the number of scanning cycles. The effect of each of these parameters was studied individually while keeping the others constant. Under each testing condition, 20 samples were measured and their average minimum value of the hole size or the neck width was taken. After the PMMA layer was fabricated, transfer patterning of the nanomeshes or the multi-ribbons into the graphene sheets was conducted in a plasma

etching system (PX-250, March Instruments) using oxygen plasma. The plasma etching parameters including radio-frequency (RF) power and etching duration were also studied to ensure high yield and repeatability of the graphene nanopatterns.

The first parameter was e-beam current. In this case, the scanning area, the resist thickness, and the number of scanning cycles of the SEM-EBL were tuned at 50×50 μm^2, 900 nm, and one cycle, respectively. As shown in , a higher e-beam current resulted in a bigger hole size and therefore a smaller neck width. The neck width decreased from 300 nm to around 90 nm as the e-beam current increased from 30 pA to 100 pA. The minimum diameter of the through holes was around 100 nm obtained at the e-beam current of 30 pA.

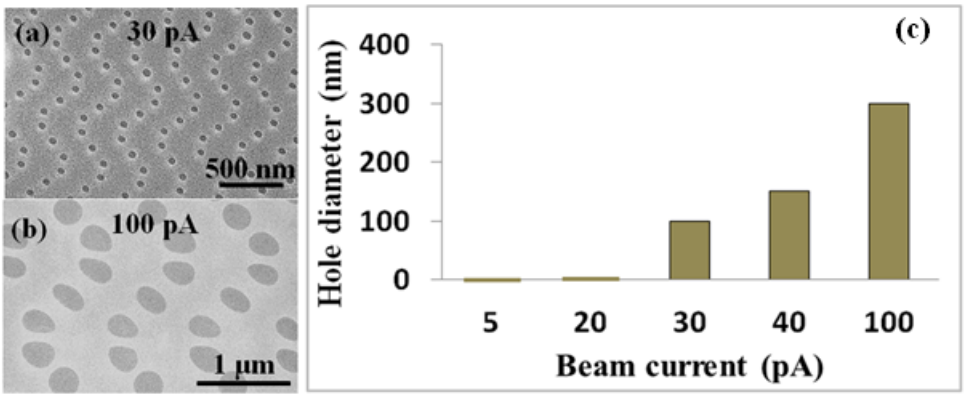


Figure 3.9 Periodic nanomesh patterned by e-beam with a scanning area of 50×50 μm^2, an e-beam resist thickness of 900 nm, and one scanning cycle. (a) and (b) SEM images show that the dimension of the holes increased as the e-beam current increased. (c) Histogram of the average sizes under different beam currents.

Small e-beam currents such as 5 pA and 20 pA resulted in incomplete exposure of the e-beam resist. In our experiments, PMMA-C_2 and PMMA-C_4 were used to obtain different thicknesses ranging from 450 nm to 900 nm. Technically, exposure of a thicker resist layer requires a greater amount of the e-beam current, leading to a larger hole size and a smaller

neck width. The experimental results suggested that a minimum e-beam current of 30 pA was required to fully expose 900 nm PMMA.

The descrease of the scanning area will lead to the descrease of the minimum neck width. Figure 3.10 (c) shows that a significant change of the neck width can be achieved by manipulating the scanning area. However, there is an area limit since a very small scanning area will cause overlapping holes (Figure 3.10 (d)). In this study, the e-beam current, the resist thickness, and the number of scanning cycles were 35 pA, 450 nm, and one cycle, respectively.

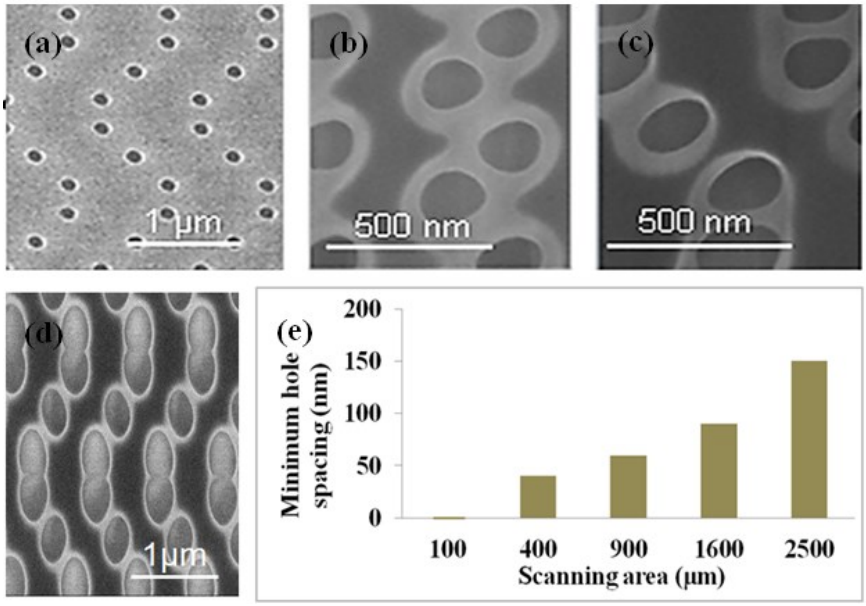


Figure 3.10 Nanoholes patterned on different scanning areas: (a) 2500 μm^2 with a neck with of ~150 nm, (b) 900 μm^2 with a neck width of ~ 90 nm, (c) 900 μm^2 with a neck width of ~ 50 nm, and (d) 100 μm^2 with overlapped holes. (e) Histogram shows the effect of the scanning area on the average minimum neck width of the GNMs.

When the e-beam scanning is repeated on a particular area more than once, the e-beam instability can cause the drift of the hole size and thus the neck width by a few nanometers from each scan. However, this phenomenon can be exploited for our purpose to decrease the neck width in the GNM structures. Figure 3.11 shows the statistical study of the average neck

width in relation to the number of the scanning cycles, with the beam current of 35 pA, the scanning area of 2500 μm^2, and the resist thickness of 900 nm. By increasing the number of the scanning cycles to three cycles, the minimum neck widths of ~ 25 nm and ~ 15 nm were achieved in PMMA layers with the thicknesses of 900 nm and 450 nm, respectively.

As the number of the scanning cycles continues to increase (> 4 cycles), overlapping holes were generated, resulting in long channels across the PMMA layer. The unexposed resist protected thin strips of the graphene sheet that eventually formed parallel nanoribbons after oxygen plasma etching. This process has been applied to successful fabrication of nanoscale graphene multi-ribbon structures with a minimum width ranging from 15 nm to 45 nm. Figure 3.11. Figure 3.12 shows the concept of our multi-scan technique for making nanoribbon patterns and a representative multi-ribbon array fabricated on a monolayer graphene sheet.

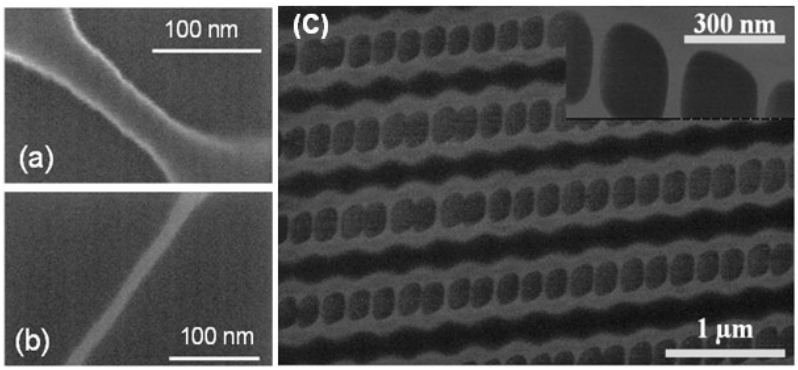
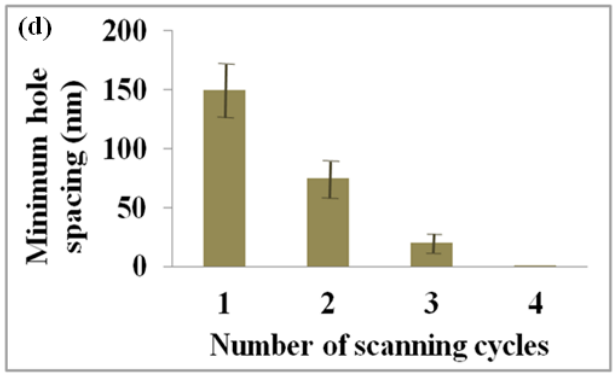


Figure 3.11 Average neck widths of 75 nm and 25 nm were obtained by two scans (a) and three scans (b and c), respectively. (d) Histogram shows the relation between the number of the scanning cycles and the average neck width of the GNMs.

Figure 3.11 (cont'd)



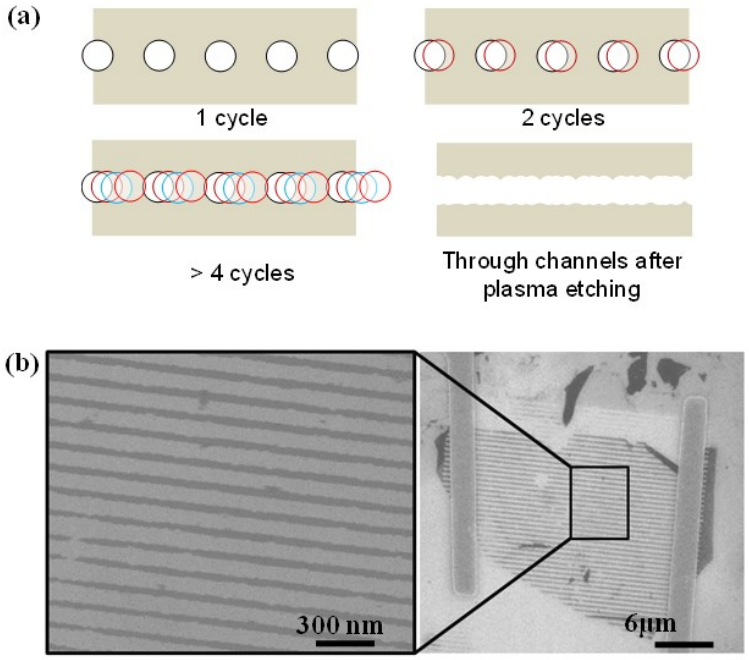


Figure 3.12 (a) Concept of the muliribbon fabrication teqnique. (b) A representative graphene multi-ribbon structure.

During the transfer patterning step, the isotropic nature of the plasma etching can induce undercut into the underlying graphene sheet. Therefore, the power and duration of the oxygen plasma etching must be fine tuned to ensure the integrity of the graphene nanopatterns, particularly the GNMs with 15-40 nm neck widths, and the repeatibility of the fabrication. In this study, a PMMA nanomesh mask was fabricated using the process described above, with the resist thickness of 450 nm, the minimum neck width of 15 nm, and the hole size of ~ 150

nm. The RF power of the plasma etcher was tuned between 70 W and 150 W and the etching duration was varied from 17 s to 120 s. Table 3.1 summarizes the yields of the nanomeshes etched into the single- and few-layer graphene sheets with different powers and durations of the oxygen plasma etching. For the single-layer graphene samples, the best yield was obtained atthe 70 W RF power for 17 s. The optimized recipe for etching the few-layer graphene was at the 150 W RF power for 40 s.

Table 3.1 The effect of oxygen plasma etching on graphene nanomesh

Plasma power (W)	Etching duration (s)	Yield of mono-layer graphene nanomesh (%)	Yield of (2-6)-layer graphene nanomesh (%)
70	17	100	No etching
150	40	50	100
150	60	0	50
150	120	0	0

Our fabrication process relies on the EBL alignment process that is independent of sample size and shape. Therefore, it is scalable to make nanoholes on a large area of the resist for the formation of nanomeshes or multi-ribbons on large-scale graphene sheets. As a demonstration, a block “S” logo of Michigan State University (MSU) was patterned on a 450-nm-thick MMA/PMMA layer, with the hole size of 70 nm and the average neck width of 150 nm (Figure 3.13).

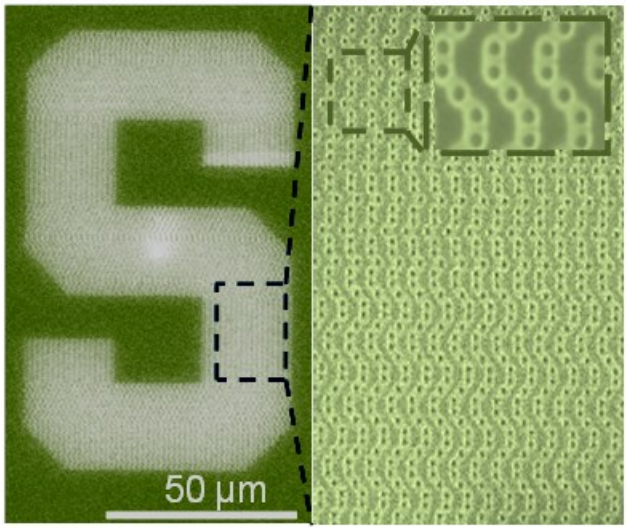


Figure 3.13 SEM image of an MSU logo with nanoholes on a large area.

3.3.3 Fabrication of *p*-type graphene nanomesh FETs

Graphene nanomesh FETs were constructed following the fabrication flow described in Figure 3.14 and Figure 3.15. The mechanically exfoliated pristine graphene sheets (mono- and few-layer) were first transferred onto the SiO_2/Si substrate. The graphene sheets were engineered to regular shapes by a fine-tuned oxygen plasma etching method (150 W, 10 sccm, 315 mTorr, for 1 minute). Ti (5 nm)/Au (70 nm) electrodes were built on the graphene as source and drain contacts, through thermal evaporation, e-beam lithography, and metal lift-off processes. 140-nm-thick PMMA-C_2 served as a protective layer for the oxygen plasma and a mask for metal lift-off. After dissolving the PMMA resist with acetone and isopropanol alcohol, the devices were rinsed with de-ionized (DI) water and dried with nitrogen. Metal was then deposited on the backside of the Si substrate as the back gate contact of the transistor. To convert the pristine graphene sheets into semiconductors**,** nanoholes were written on 450-nm-thick PMMA by e-beam scanning the area of interest, using the above mentioned unconventional EBL method. The EBL parameters were tuned as follows: 35 kV acceleration voltage, 30 pA beam current, and one scanning cycle. The developed nanoholes

were transferred into the mono- or few-layer graphene sheets using oxygen plasma etching with 150 W RF power, 10 sccm oxygen flow rate, 315 Torr chamber pressure, and 40 s duration. Based on the experimental data, this recipe can be used to etch 1 to ~ 10 layers of graphene sheets.

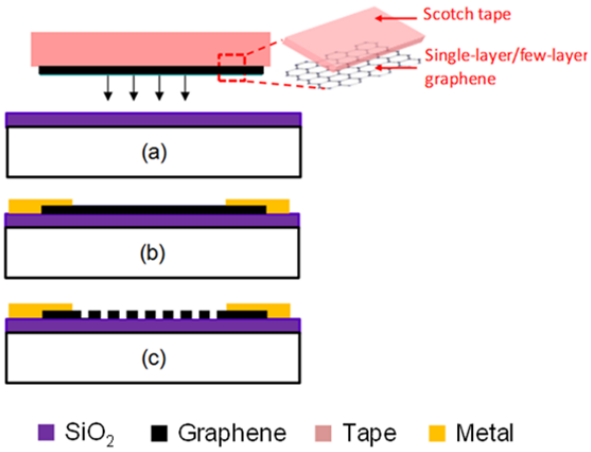


Figure 3.14 Process flow for making GNM transistors.

Figure 3.15 shows the SEM and the optical microscope images of two fabricated GNM FETs. The same etching parameters and e-beam resist thickness were used for making nanoholes on the mono- and few-layer graphene sheets, resulting in ~ 100 nm periodic holes. Initially, the electrodes were deposited on as-patterned GNMs. Some nonfunctioning devices fabricated in this way did not appear damaged under close inspection with SEM. We suspected the damage to these devices occurred in the GNM region covered by the electrodes. Depositing electrodes before nanoholes patterning corrected this problem and greatly improved the fabrication yield. Additionally, this method improved the performance of the GNM FETs by increasing the contact area and thus the driving current.

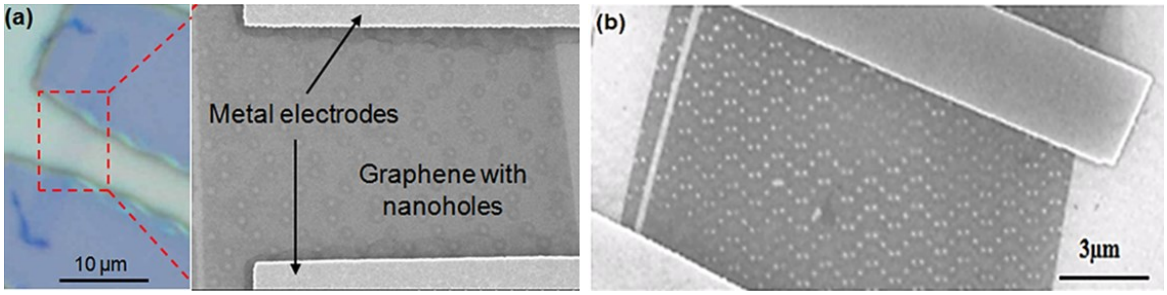


Figure 3.15 Representative GNR transistor fabricated by on (a) monolayer graphene sheet (b) few-layer graphene sheet.

The fabricated GNM transistors were characterized by measuring the drain current (I_{ds}) versus drain voltage (V_{ds}) at different gate voltages (V_g), using a semiconductor parameter analyzer (HP4145B, Hewlett Packard). All the devices were annealed in an H_2/Ar environment to remove resist residues and fabrication contaminants prior to the measurement. shows the V_{ds}-I_{ds} characteristics of the monolayer and few-layer GNM FETs. As shown in Figure 3.16 (b) and (d), the drain current decreases with the increase of the gate voltage. As discussed previously in Chapter 1, the Dirac point of graphene is defined as a certain gate potential where the valance and conduction bands meet. After the Dirac point, the conductivity type of graphene changes from *p*-type to *n*-type. Thus one can realize the ambipolar properties of graphene, which is different from conventional semiconductors, such as silicon, where only one ON state and one OFF state exist. In addition, the Dirac points of the as-fabricated GNM transistors were located in the positive region of the V_g axis, indicating that all the devices exhibited a *p*-type semiconductor property. From the physics point of view, this can be explained by the downward shift of the Fermi level into the valance band. The *p*-type properties of GNMs can be attributed to the high sensitivity and reactivity of abundant graphene edges exposed by introducing the nanopatterns into the pristine

graphene. The perimeters of these nanoholes will readily adsorb oxygen from the environment, particularly during oxygen plasma etching [27, 28]. Impurities generated during the fabrication processes may also have contributed to the *p*-type doping.

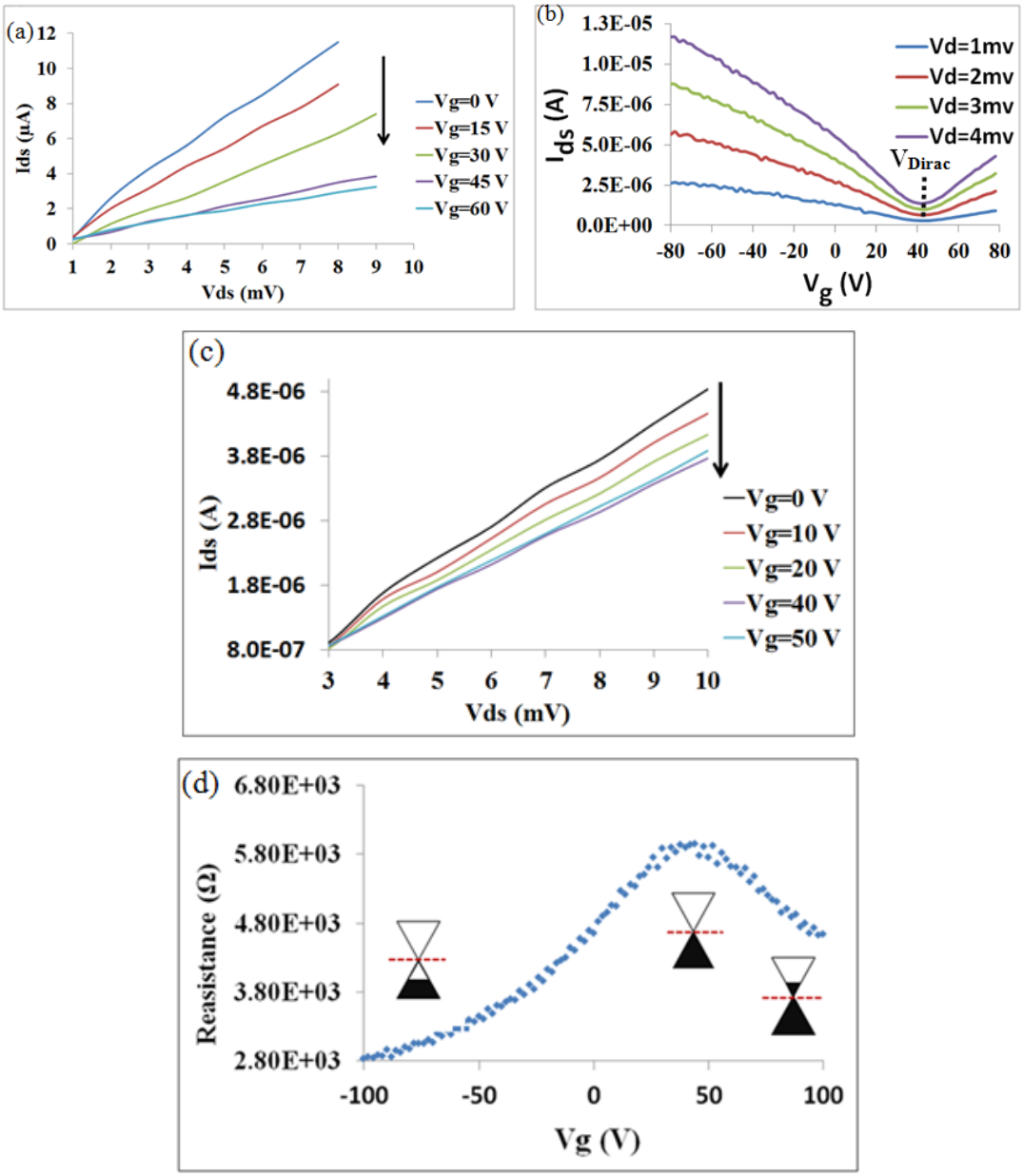


Figure 3.16 Drain current (I_{ds}) versus drain–source voltage (V_{ds}) at different gate voltages (V_g) for a monolayer GNM transistor (b) Ids versus *Vg* at different Vds voltages (c) Drain current (I_{ds}) versus drain–source voltage (V_{ds}) at different gate voltages (V_g) for a monolayer

Figure 3.16 (cont'd)

GNM transistor (d) resistance variation as the function of the gate voltage of a few-layer graphene device. All graphene nanomeshes had *p*-type semiconductor behavior.

The ON-OFF ratio of the monolayer GNM transistor was around 15. However, in order to achieve higher ON-OFF ratio of GNM transistors, the neck width must be very few nanometers, which is not easy to achieve by our fabrication process. From the experimental data, we also calculated the conductance of the monolayer graphene nanomesh, which was around 3.3 mS at the gate voltage (V_g) of 60 V, whereas the ON-OFF ratio and the conductance of the few-layer graphene FETs were ~ 2.8 and ~ 0.13 mS, respectively.

The electron mobility (μ_e) was calculated using the equation: $\mu_e=(t/\varepsilon)\times(d\sigma/dV_g)$, where t=300 nm is the thickness of the SiO_2, $\varepsilon=3.9\times\varepsilon_0=3.45\times10^{-11}$ F/m is the permittivity of the SiO_2, and $\sigma=L/RW$ is the conductivity. The maximum electron mobility achieved was 3332 cm^2/V s for monolayer device, while it is 1343 cm^2/V s for the few-layer one.

The performance of a monolayer GNM device under the vacuum condition of 5×10^5 Torr was investigated inside an environmental SEM (Carl Zeiss variable pressure SEM EVO LS25), in order to study the effect of environmental contaminations on the semiconductor properties of the GNMs. Measured I_{ds}-V_{ds} curves showed no significant deviation from those obtained at atmosphere (Figure 3.17), indicating device performance was resistant to contaminations or doping associated with normal atmospheric condition.

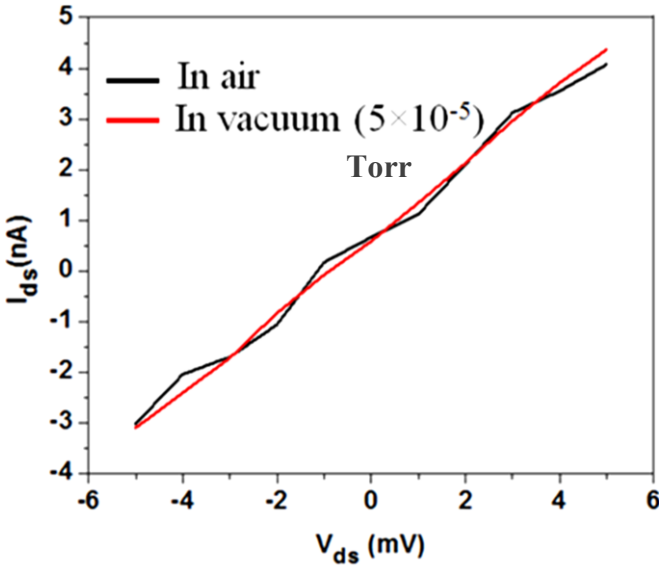


Figure 3.17 I_{ds}-V_{ds} characteristics of a monolayer GNM transistor tested under vacuum condition and at atmospheric pressure, showing no significant difference.

We also fabricated graphene *p*-type transistors based on nanoriboon configurations that were patterned using the aforementioned EBL method. The devices were characterized by measuring the drain current I_{ds} versus drain voltage V_{ds} at different gate voltages V_g (Figure 3.18) in addition to the current transport characteristic. The ON-OFF ratio of the multi-nanoribbon FET was ~ 1.5 and the conductance was ~ 0.04 mS at the gate voltage of 60 V. Fermi level positions relative to the Dirac point ($\Delta E_F = |E_F\text{-}E_D|$) were calculated for nanomesh and graphene multi-ribbon to be 203 meV and 904 meV respectively.

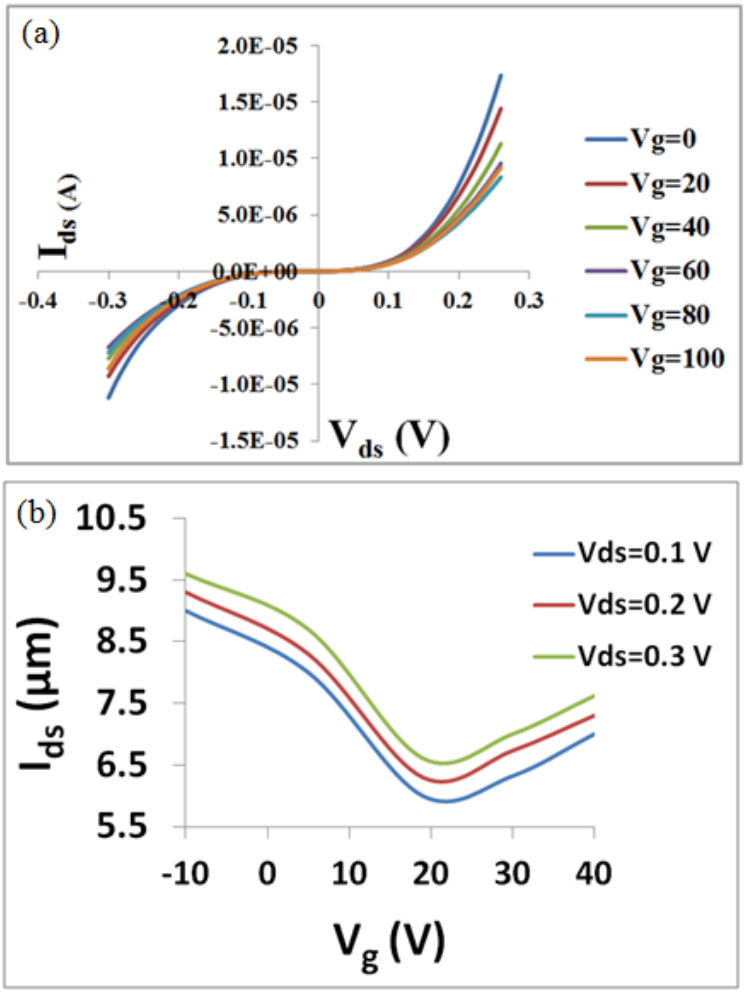


Figure 3.18 (a) Current voltage transfer characteristic of a graphene multi-ribbon transistor, and (b) its current transport characteristic.

3.4 Conclusion

In this chapter, we presented a method for engineering the number of graphene layers with fine-tuned oxygen plasma parameters. By this method, only one layer of graphene sheet can be etched at a time. Although this technique produces surface defects, it can be suppressed by annealing process. Additionally, we demonstrated a template-less nanofabrication technique that can be used for batch production of the graphene nanomesh and multi-ribbon structures. The EBL processing parameters have been investigated to precisely control the hole size and the neck width of the nanomeshes. The minimum hole size and neck width achieved was around 100 nm and 15 nm, respectively. Moreover, the same fabrication method has been

successfully applied to the fabrication of the graphene nanomesh and multi-nanoribbon FETs. Although we have realized *p*-type graphene transistors using the nanopatterning approach, fabrication of a digital nanocircuit will require both *p*-type and *n*-type graphene semiconductors. In the next chapter, a doping method to achieve *n*-type graphene will be introduced.

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4 GRAPHENE N-TYPE DOPING

4.1 Introduction

Chemical doping has been proven to be an effective solution to open the band gap and modulate the electrical properties of graphene. In this case, the absorption of chemical molecules and/or charge exchange on graphene surface can cause the shift of the initial Fermi level position upward (as shown in *n*-type graphene) or downward (as shown in *p*-type graphene) with respect to the charge neutrality point (the Dirac point). Compared to *p*-type doping, graphene *n*-type doping with long-term chemical stability is more challenging due to the rapid degradation of *n*-type properties upon exposure to air. The degradation of the *n*-type properties is mainly attributed to the absorption of oxygen molecules, which are known as effective hole-dopant for graphene. Electron transfer from the *n*-type graphene to the absorbed oxygen molecules will result in the reduction of the *n*-type doping concentration, which can be well quantified by the electronic band structure and the downward shift in the Fermi level of the doped graphene.

To date, a number of doping approaches have been developed to achieve *n*-type graphene: for example, substitution doping with nitrogen dopants [1-4], covalent functionalization [5, 6], and radiation-induced doping [7, 8]. However, these existing methods usually increase defects in carbon lattices, deteriorate the carrier mobility of as-doped graphene, and are limited in chemical stability. To minimize defects, electrostatic field tuning has been proposed to modulate the electronic properties of graphene devices [9-11] but this method does not open the band gap of monolayer graphene and thus has limited applications. Alternative methods, such as chemical modification of graphene surface with polymer [12, 13] and metallic thin films [14, 15], have also been reported. These *n*-type graphene devices still have limited thermal and chemical stability, and are vulnerable to the influence of the

surrounding environment. Recently, Ho *et al.* demonstrated the self-encapsulated doping of *n*-type graphene with high carrier mobility and extended air-stability using titanium suboxide thin films. However, the fabrication of such devices requires sol-gel and hydrolysis processes, which are incompatible with conventional microfabrication technology [16]. To mitigate these drawbacks, this study proposed a new technique for *n*-type graphene doping with minimum defects and enhanced chemical stability, using SU-8 photoresist as a doping and encapsulating material. The *n*-type graphene doped with uncrosslinked SU-8 can be reversed to the *p*-type graphene by removing SU-8 with organic solvents. The fabrication of the *n*-type graphene transistors is fully compatible with microfabrication technology, which provides possibilities for mass production of large-scale graphene-based electronics.

4.2 Method

Pristine graphene (PG) samples were mechanically exfoliated from highly oriented pyrolytic graphite (HOPG) flakes and then transferred onto SiO_2 (300 nm)/Si substrates.. The graphene samples were then annealed at ~ 400 °C in an Ar/H_2 environment for 1 hour to remove tape residues and contaminations.

Figure 4.1 (a) shows the schematic representation of a back-gated graphene field-effect transistor (FET) with SU-8 as an *n*-type doping and encapsulating material. The transistors were constructed prior to the SU-8 doping, using the following fabrication method. PG samples were patterned into regular shapes via oxygen plasma etching with 150 W RF power, 10 sccm oxygen flow rate, 315 mTorr chamber pressure, and 1 min duration. Ti (5 nm)/Au (70 nm) electrodes were fabricated on top of the graphene as source and drain contacts, via thermal evaporation, electron beam lithography (EBL), and metal lift-off processes. A 140-nm polymethyl methacrylate (PMMA) layer served as a protective layer for the oxygen plasma and a mask for the lift-off. The PMMA resist was dissolved with acetone, rinsed with isopropanol alcohol and de-ionized (DI) water, and then dried with nitrogen. Metal was

deposited on the backside of the highly doped Si substrate as the back gate of the transistor. After metallization, graphene nanomeshes (GNMs) with a hole diameter of ~ 100 nm and a neck width of ~ 300 nm were selectively patterned on the PG at the location of the transistor channel, using an unconventional EBL method [18]. GNM transistors are expected to have relatively higher on/off current ratios compared to GNR transistors and allow for favorably high driving current of the channel. Furthermore, these nanomeshes can enhance the *p*-type doping level of graphene due to the high sensitivity and reactivity of abundant edge defects, facilitating the reversibility study of the SU-8 doping effect.

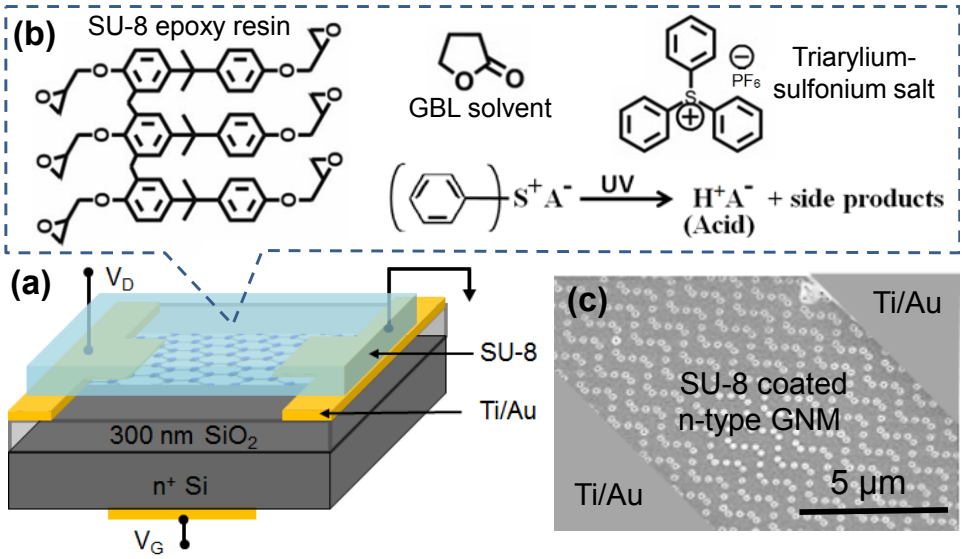


Figure 4.1 (a) Schematic of an n-type graphene transistor with SU-8 as the n-type dopant and self-encapsulation. (b) Three basic chemical compounds of the SU-8 resist and the chemical reaction for generating the photo-acid upon UV exposure. (c) A representative GNM transistor doped and encapsulated with SU-8.

The *n*-type doping of PG or *p*-type GNMs was performed by spinning 4-μm-thick SU-8 2 negative photoresist (NANO™, MicroChem) on the graphene surface. The SU-8 resist contains three basic components (Figure 4.1 (b)): an EPON SU-8 epoxy resin, a gamma-butyrolactone (GBL) solvent, and a photo-acid generator taken from the family of the triarylium-sulfonium salts [19]. Following the spin coating, the resist was pre-baked at 95 °C

for various durations to evaporate the GBL solvent and solidify the resist. Optionally, some SU-8-coated samples were exposed to ultraviolet (UV) radiation for 1 min and then post-baked at 105 °C. The UV exposure converts the photo-acid generator into the photo-acid, which readily reacts with polymer chains to enable the crosslinking of the SU-8 epoxy during the post-baking step [20]. During this *n*-type doping procedure, SU-8 is expected to offer several functions. First, it is hypothesized that the photo-acid generator in the SU-8 compound contains free radicals [21] as efficient electron donors for graphene. Second, SU-8 has good dielectric properties (1 GHz dielectric constant of 4.1 and dielectric strength of 112 V/μm), which make it an effective dielectric medium. Owing to its relatively low water vapor and gas permeability, SU-8 is also an excellent encapsulating material to protect *n*-type graphene and transistors from environmental interference. A fabricated prototype of the SU-8 doped and encapsulated GNM transistor is given in (c).

4.3 SU-8 Doping Results and Discussions

4.3.1 SU-8 *n*-type doping effect

The *n*-type effect of the SU-8 doped graphene was studied using Raman spectra taken from graphene samples with different treatments (). For the SU-8 doped samples, the characteristic peaks of the SU-8 resist were subtracted from the Raman spectra. The G band of the bilayer PG was located at ~ 1581 cm^{-1}, while the G band of the pristine monolayer PG shifted upward to ~ 1592 cm^{-1} due to the decrease in layer number [22]. From the Raman spectra of all the SU-8-coated samples, the G peak always stiffened and the intensity of the 2D peak decreased with respect to that of the G peak, which agrees with those observed in typical electron doping of graphene [13, 16]. The *n*-type doping effect is also evident in the slight upshift of the G peak frequency [13, 23, 24]. Referring to the electrostatic gating of graphene on a Si substrate [13], the change in the 2D to G intensity ratio (I_{2D}/I_G) has a strong

dependence on the doping level, and a smaller I_{2D}/I_G ratio indicates a higher concentration of electron doping. In this study, after the SU-8 doping, the I_{2D}/I_G ratios were reduced from 1.7 (PG) to ~1 (GNM coated with uncrosslinked SU-8), ~0.9 (graphene coated with crosslinked SU-8), and ~0.6 (graphene coated with uncrosslinked SU-8), as the indication of increasing doping levels. The doping concentration of the crosslinked SU-8 was lower than that of the uncrosslinked SU-8, mainly due to the reduced concentration of the photo-acid generator caused by the UV exposure and post-baking treatments. The rise of the D peak intensity indicates the substantial distortion of local carbon lattices, as shown in the Raman spectrum of the GNM (Figure 4.2). The changes in the D peak intensities of all the SU-8 doped samples were almost negligible compared with their Raman spectra before the doping treatment, suggesting that the SU-8 doping occurs mainly through surface change transfer doping at the SU-8/graphene interface [16]. Therefore, our doping method will not induce permanent damage in the local carbon lattice of graphene, unlike the covalent functionalization or the substitution doping of graphene in which the increased lattice disorder results in enhanced D band intensity. In addition, the Raman spectrum of the SU-8-coated graphene recovered to a shape similar to that of the PG (Figure 4.2 (a)) after removing the uncrosslinked SU-8, demonstrating the reversibility of our SU-8 doping process. It is of note that the crosslinked SU-8 epoxy cannot be attacked by general organic and inorganic chemicals or plasma etching and thus provides an excellent encapsulation for the *n*-type doped graphene.

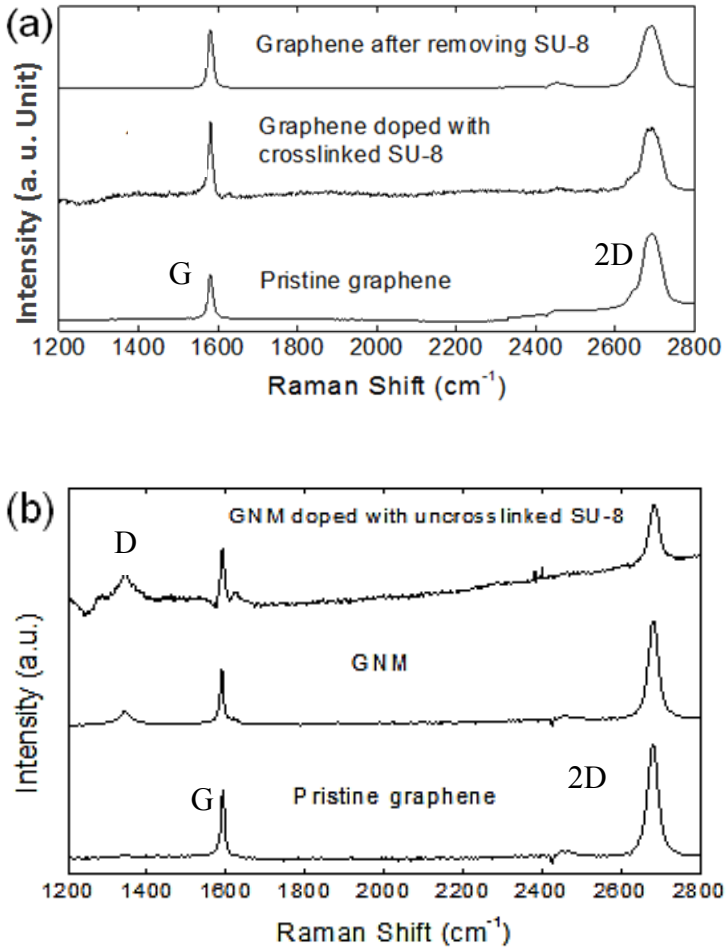


Figure 4.2 (a) Raman spectra of a representative bilayer graphene sample with different treatments. (b) Raman spectra of a representative monolayer graphene sample with different treatments. The spectra from the bottom to the top correspond to the monolayer PG without nanomesh, undoped monolayer GNM, and SU-8 doped monolayer GNM, respectively.

4.3.2 SU-8 doped n-type graphene FETs

After studying the *n*-type doping effect of SU-8, we explored the feasibility of using SU-8 doped GNM graphene to fabricate FETs and verified the *n*-type transport properties of the SU-8 doped and encapsulated GNM FETs. In this case, a ~ 4-μm-thick SU-8 layer was coated and soft baked at 95 °C for 10 min, followed by UV exposure using an UV curing lamp with ~ 365 nm wavelength for 1 minute. The devices were tested using a semiconductor parameter analyzer (HP4145B, Hewlett Packard). Figure 4.3 shows the transport properties of

a GNM FET, fabricated using the above method. It is observed that the SU-8 doping shifted the Dirac point from > 20 V to -17 V, representing typical *n*-type transport behavior of the graphene. The n-type doping effect is also evident in the gate-dependent characteristics of the transistor drain current (Figure 4.3 (b)). As the result of the SU-8 removal, the Dirac point returned to a positive gate voltage, suggesting the recovery of the *p*-type semiconducting behavior of the graphene.

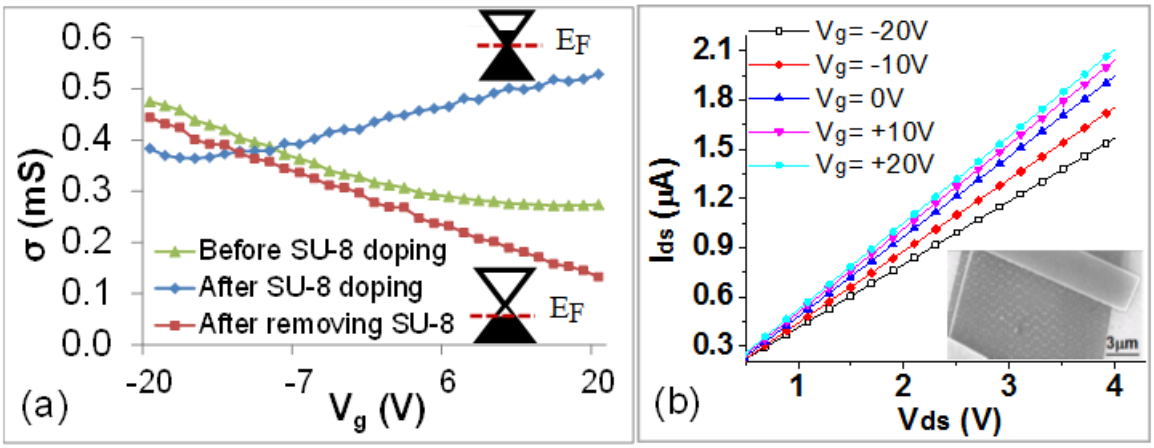


Figure 4.3 A representative GNM transistorwith the Si back gate, 300 nmSiO_2 dielectric, Au/Ti source and drain contacts. (a) Gate-dependent conductivity (σ) of graphene before the SU-8 doping, after the doping, and after removing SU-8. (b) Current-voltage (V_{ds}-I_{ds}) curve of the SU-8 doped device, measured at various gate voltages (V_g) ranging from -20 to +20 V.

The doping level, and hence the Fermi energy (E_F), of the graphene, can be tuned by controlling the soft-baking time and/or the thickness of the SU-8 coating, as shown in . Longer soft-baking shifted the Dirac point of the *n*-type doped graphene more negatively, corresponding to a higher doping level. This shifting is mainly caused by the increased concentration of the doping agent (the photo-acid generator) in the SU-8 compound, since more solvent was evaporated during the extended soft-baking treatment. Similarly, thick SU-8 coating contains more free radicals and thus enables a higher doping level compared to thin

SU-8 coating, which can be demonstrated by the substantial shift of the Dirac point from ~ 50 V to ~ -75 V ((b)).The electron areal concentrations (n_e) were estimated by $n_e = \eta(V_g - V_d)$ with $\eta = C_{ox}/e = (\varepsilon_0 \varepsilon_r)/(de) = 7.2 \times 10^{10}$ $cm^{-2}V^{-1}$, where C_{ox} is the capacitance per unit area calculated at zero gate bias, d is the thickness of the back-gate oxide (300 nm), ε_0 is the permittivity of free space, ε_r is the relative permittivity of SiO_2, V_g is the back-gate voltage, V_d is the gate voltage at the Dirac point, and e is the elementary charge. Given the electron areal concentration, the Fermi level position relative to the Dirac point ($\Delta E_F = |E_F - E_D|$) can be calculated using the equation: $\Delta E_F = \sqrt{\pi n_e (\hbar \upsilon_F)^2}$, where υ_F is the Fermi velocity of electrons ($\approx 10^8$ cm/s), and E_F and E_D are the energy positions of the Fermi level of the *n*-type graphene and the Dirac point, respectively [27]. The table in Figure 4.5 summarizes the calculated electron concentrations (n_e) of graphene samples under different SU-8 doping treatments and their corresponding Fermi level shift ΔE_F above the Dirac point. The band diagrams show the energy position of the Dirac point and the shifts in the Fermi level of *p*-type and *n*-type doped graphene, respectively. As expected, the increased absorption of the donors (the photo-acid generator) can effectively enhance the electron doping concentration, resulting in the upward movement of the Fermi level and thus larger ΔE_F.

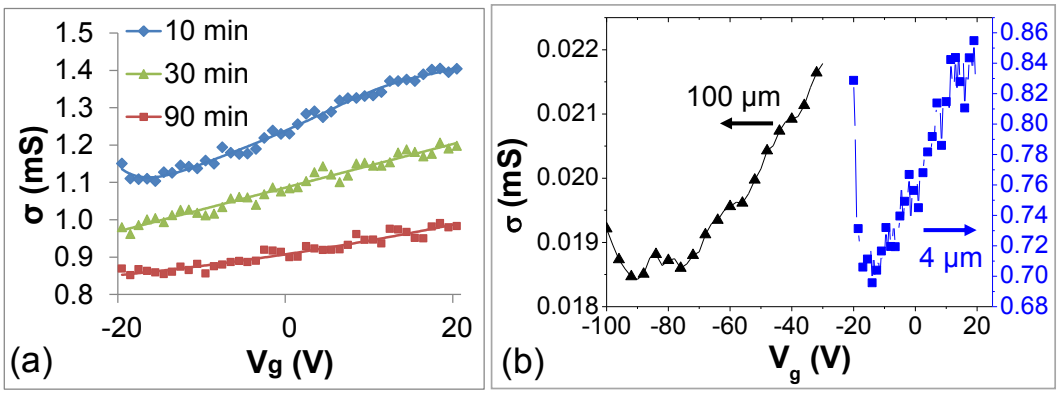
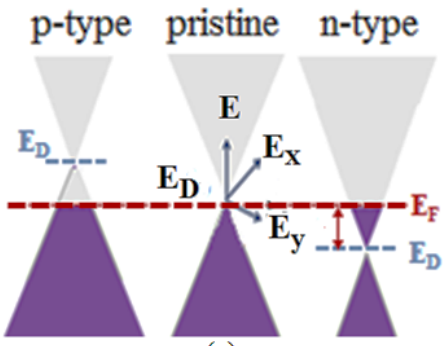


Figure 4.4 Gate-dependent conductivity curves (σ) of the n-type doped devices (a) with various SU-8 soft-baking durations of 10 min, 30 min, and 90 min, and (b) with various SU-8 thicknesses of ~ 4 μm and ~ 100 μm.



(a)

SU-8 doped n-type graphene (thickness, baking duration)	n_e (cm^{-2})	ΔE_F (meV)
4 μm, 10 min soft-baking	~2.5×10^{12}	~ 184.5
4 μm, 30 min soft-baking	>3×10^{12}	> 202.1
4 μm, 90 min soft-baking	>3×10^{12}	> 202.1
100 μm, 90 min soft-baking	~7×10^{12}	~ 308.7

(b)

Figure 4.5 (a) Band diagrams showing the shifts in the Fermi level of *p*-type and *n*-type doped graphene, respectively. (b) Calculated electron concentrations (n_e) and Fermi level shift (ΔE_F) of graphene samples, as a function of SU-8 thickness and soft-baking duration.

The positive slopes of the gate-dependent conductivity (σ-V_g) curves can give a measure of the electron mobility (μ_e) of the *n*-type graphene, which can be expressed using the equation: $\mu_e = \Delta\sigma/(C_{ox}\Delta V_g)$ in which the conductivity (σ) is estimated by $\sigma = (I_{ds}/V_{ds})(L/W)$, and L and W are the length and the width of the graphene channel, respectively. Typically the electron mobility of the as-fabricated *p*-type GNM FETs can reach a maximum value of ~ 3332 ± 500 $cm^2V^{-1}s^{-1}$, obtained from a monolayer GNM device. After the SU-8 doping, the electron mobility of the devices was calculated to be over 3 times lower than that of the undoped ones and varied in a wide range from ~ 382 $cm^2V^{-1}s^{-1}$ to 745 $cm^2V^{-1}s^{-1}$, depending on electron-doping concentration and the presence of nanoholes. The maximum electron mobility was observed in the graphene sample doped with 4 μm uncrosslinked SU-8. Since the SU-8 doping does not increase lattice disorder as demonstrated by the above Raman spectra (Figure 4.2), the reduction of the electron mobility is mainly attributed to the long-rang Coulomb scattering induced by impurities from the polymer. This finding also explains the reduced conductivities of the *n*-type graphene, in agreement with those observed in typical polymer doping of graphene [13]. As expected, the presence of nanomeshes further reduced the electron mobility due to the increased defects in the local carbon lattices. In addition, an asymmetric effect on electron and hole mobilities was observed in all the devices, which could be caused by the imbalanced injection of electrons and holes from the source- and drain-channel interfaces, respectively [12].

4.3.3 Doping mechanism of SU-8

While we have demonstrated that the SU-8 doping can achieve *n*-type graphene, more studies are necessary to validate that PAG is indeed the *n*-type doping source in SU-8. Two experiments were conducted successively. In the first experiment, only two of the three SU-8

components were prepared by dissolving Epon SU-8 (Epikote 157) in organic solvent (cyclopentanone). A composition of 40 wt% SU-8 resin and 60 wt% solvent was used. The compound was mixed for 1 hour and then left in air at room temperature for 2 days to mature. The mixture was spin-coated on the graphene surface, followed by soft baking at 65 ^{0}C for 10 min and then at 95 ^{0}C for another 10 min. The blue curve in Figure 4.6 shows the V_g-I_{ds} characteristic of the as-doped graphene, which exhibited a typical *p*-type property.

After the device characterization, the resin-solvent coating was dissolved in acetone in order to convert the *p*-type graphene to the pristine graphene that was immediately subjected to the second experiment. In this case, the doping chemical was prepared by mixing 40% SU-8 resin, 59% solvent, and 1% PAG. The mixture was baked and matured using the aforementioned procedures, and then coated on the same pristine graphene. The graphene transistor doped with the new mixture was characterized and its V_g-I_{ds} and V_{ds}-I_{ds} properties were given in the red curve of Figure 4.6 and Figure 4.7, respectively. The Dirac point of the graphene shifted to –29 V, indicating that the pristine graphene was converted to an *n*-type one. This result demonstrated that the PAG is an electron donor for the *n*-type doping of graphene.

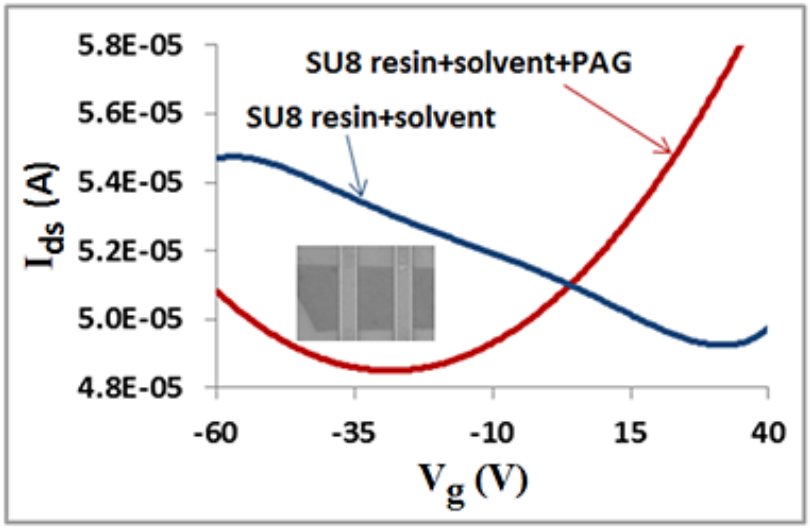


Figure 4.6 Current transfer characteristcs of graphene FETs doped by two different chemical mixtures. Case 1 (*p*-type): graphene doped with the resin-solvent mixture. Case 2 (*n*-type): Graphene doped by the resin-solvent-PAG mixture. The inset is the SEM image of the device.

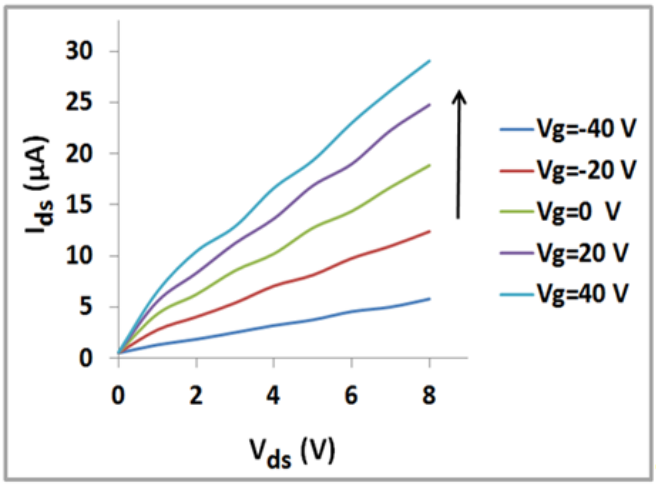


Figure 4.7 V_{ds}-I_{ds} relation of the graphene FET after n-doping with the resin-solvent-PAG mixture.

To further investigate the effect of the PAG, its percentage concentration in the mixture was doubled. Figure 4.8 shows that the shift in the Dirac point increased with the increase of the

PAG concentration, whereas the V_g-I_{ds} slope decreased, corresponding to a higher electron doping level and lower electron mobility, respectively. The electron mobility dropped from 2388 to 690 cm^2V^{-1} s^{-1} when the concentration of the PGA increased from 5.5% to 10%, while the charge carrier increased from 0.36×10^{12} to 1.08×10^{12} cm^{-1}. It should be noted that, since the concentration of the amount of solvent diminished during the soft baking step, it was difficult to determine the concentration of the PGA with respect to the other chemical components precisely after soft baking. Figure 4.9 observes the positions of the Dirac points of several graphene samples, which were doped using compounds with different PAG concentrations measured before soft baking.

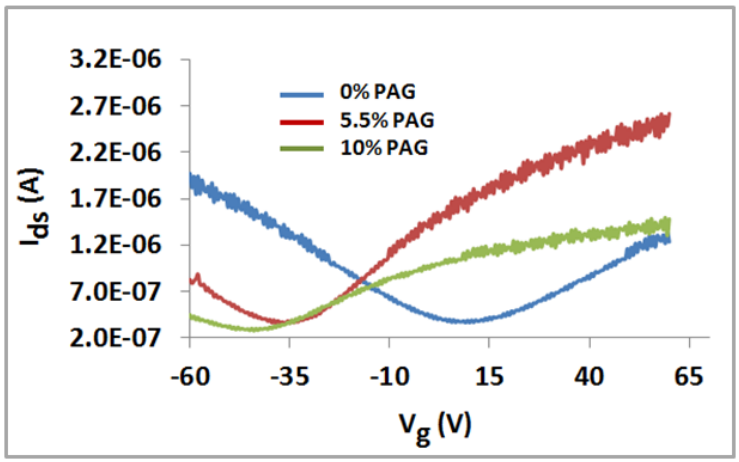


Figure 4.8 Device characteristics before and after n-doping with two different PAG concentrations.

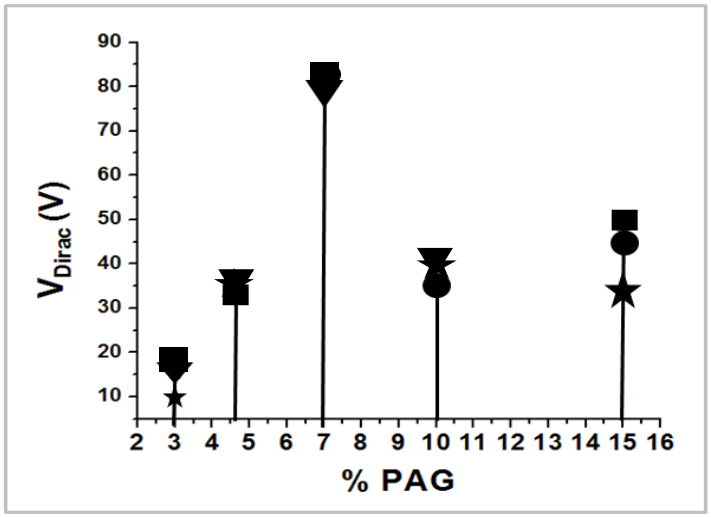


Figure 4.9 The positions of the Dirac points of four samples with different PAG concentrations. The triangle, square, circle and star symbols resemble different samples at different PAG concentrations. The Dirac point positions of some samples were observed at different PAG concentrations and some were observed at only one PAG concentration since sometimes it is hard to totally remove the PAG from graphene after soft baking.

4.3.4 Stability of SU-8 doped *n*-type graphene FETs

The chemical stability of the *n*-type graphene in air was investigated by monitoring the dynamic change in the transport properties of the GNM transistors, in which the UV exposed SU-8 was post-baked at 105 °C for at least 30 min to enable complete crosslinking of the resist. Then the devices were kept under ambient condition for a week and their gate-dependent resistances were recorded daily. As shown in Figure 4.10, the gate-dependent conductivity curves exhibited only a small upshift of the Dirac points by ~ 3 V from around -9.0 V to - 6.0 V, after 2 days of exposure in ambient air, and then remained stable over the course of testing. Quantitatively, the electron areal concentration was reduced by ~ 2×10^{11} cm^{-2}, corresponding to the downshift in the Fermi level by only ~ 15 meV from 143 meV to 128 meV. This slight change may be attributed to the reduced concentration of the photo-acid generator due to the slow crosslinking of SU-8 at room temperature in air. The slopes of the

conductivity curves showed no remarkable changes (within 15%) after 7 days of exposure in air, indicating no major decline in the carrier mobility of the *n*-type graphene.

Our result demonstrates that the SU-8 encapsulation effectively enhances the air stability of the *n*-type doped graphene, by minimizing impurity absorption and scattering associated with normal ambient condition. We also found that the post-baking was a critical step for the UV-exposed SU-8 to achieve good encapsulation of the graphene, without which the *n*-type graphene reverted to *p*-type after being exposed in air for several hours. One possible explanation for this phenomenon is that the photo-acid generated upon the UV exposure slowly interacts with the polymer chains at room temperature, resulting in the partial crosslinking of the local epoxy. The non-uniformly crosslinked SU-8 contained pores to enable the diffusion of *p*-type impurities (e.g. oxygen) through the encapsulating layer, which leads to the rapid degradation of the *n*-type graphene. In addition, the thin SU-8 coating of ~ 4 µm was desired for electron doping of graphene, since thermally induced stress in thick SU-8 films could damage the local carbon lattices.

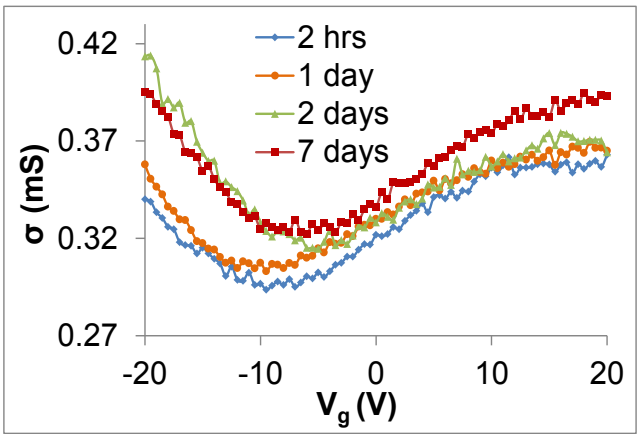


Figure 4.10 Air stability testing of a representative *n*-type GNM transistor doped and self-encapsulated with ~ 4 µm crosslinked SU-8. (a) Gate-dependent conductivity (σ) curves (b) Gate-dependent resistance of the device measured at different time points. The dash lines represent the positions of the Dirac points.

The temperature stability or operation temperature range of graphene transistors is one of the important factors that has to be taken into account. Therefore, we studied the current transfer characteristics of graphene FETs doped with cross-linked SU-8, in a wide temperature range from ~ -15 °C to + 100 °C. Figure 4.11 demonstrates the temperature stability of the *n*-type properties of two different devices within the testing temperature range, in which only a small shift in the Dirac point was observed.

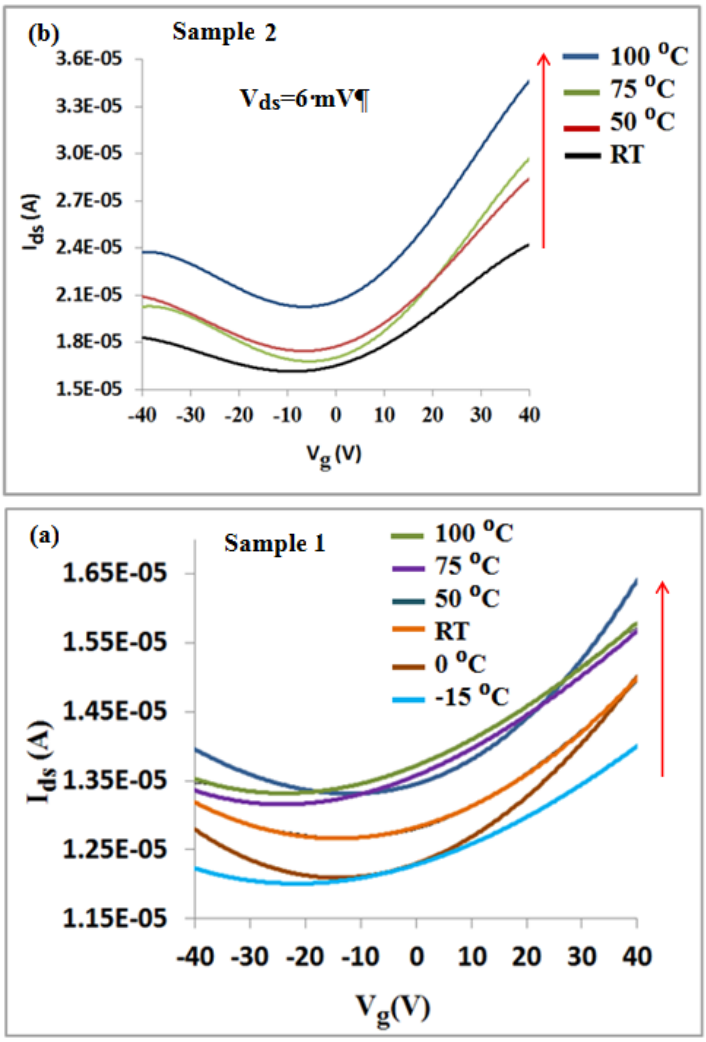


Figure 4.11 Temperature stability of two *n*-type graphene FETs: (a) V_g-I_{ds} curves at a temperature range from -15 °C to 100 °C. (b) V_g-I_{ds} curves at a temperature range from RT to 100 °C.

To better understand the temperature effect on SU-8 doped graphene crystalline structure, such as atomic bonds, phonons, and thermal expansion, we also studied the temperature dependence of Raman spectra of both pristine and *n*-doped graphene samples. During the measurements, the samples were placed on a hot stage under a HoloProb Raman spectroscope. All the spectra were excited using a visible (532 nm) laser with a relatively low laser power (0.53 mW) to avoid graphene heating by the excitation laser. A ×100 objective lens was used to focus the laser beam on the desired location of the sample. The temperature dependence of the G-band peak position was measured at several temperatures varying from room temperature (RT) to 150 °C for both the *n*-doped and pristine graphene FETs.

First, the temperature dependence of pristine mono- and bi-layer graphene was investigated. The experimental results show that the elevating temperature leads to the downward shift of the Raman G-band peak to a lower frequency (Figure 4.12). The extracted negative temperature coefficients of G-mode for mono- and bi-layer graphene were -0.042 cm^{-1}/°C and -0.023 cm^{-1}/°C, respectively.

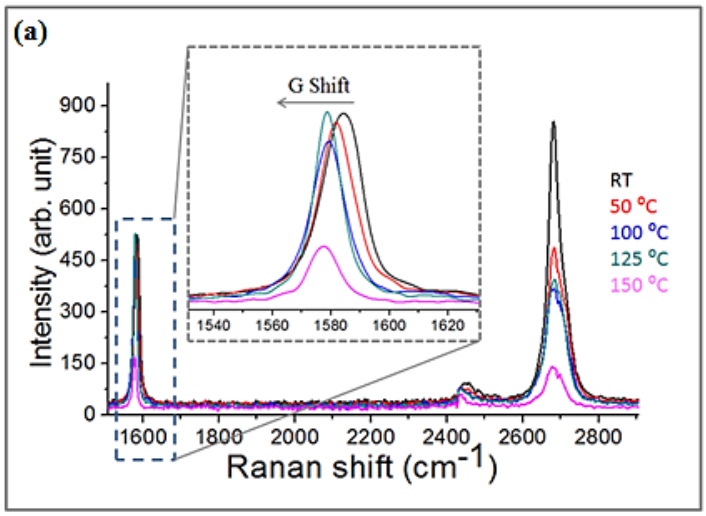
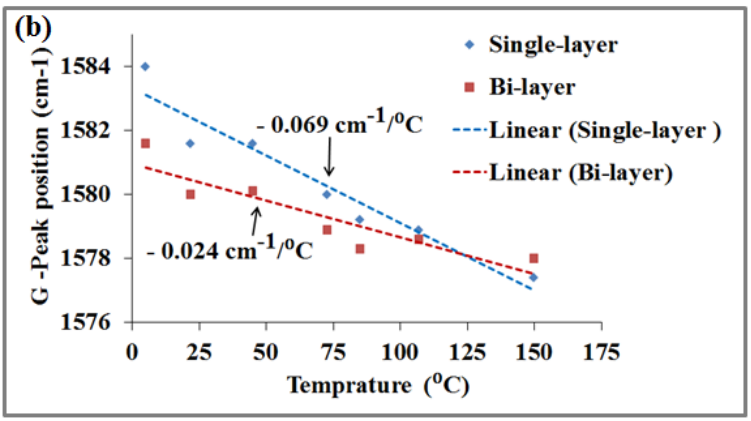


Figure 4.12 (a) Raman spectra of pristine graphene at different temperatures. (b) Temperature dependence of G-band peak for mono- and bilayer pristine graphene samples.

Figure 4.12 (cont'd)



Second, the temperature dependence of SU-8 doped *n*-type graphene FET was investigated, as given in Figure 4.13. Another peak appeared at 1607 cm^{-1}, which was the characteristic peak of the SU-8 resist. One remarkable observation is that the G-band peak of the *n*-type graphene became wider as the temperature elevated. The corresponded G-mode temperature coefficients of *n*-doped mono- and bi-layer were determined to be -0.069 and -0.024 $cm^{-1}/{}^{0}C$, respectively (Figure 4.13 (b) and (c)). The results indicate that the G-mode temperature coefficient of the *n*-doped monolayer graphene had a highest sensitivity to temperature. This can be attributed to the effect of the thermal expansion difference between SU-8 ($\sim 52\times10^{-6}/{}^{0}C$) and graphene ($\sim -0.03\times10^{-6}/{}^{0}C$).

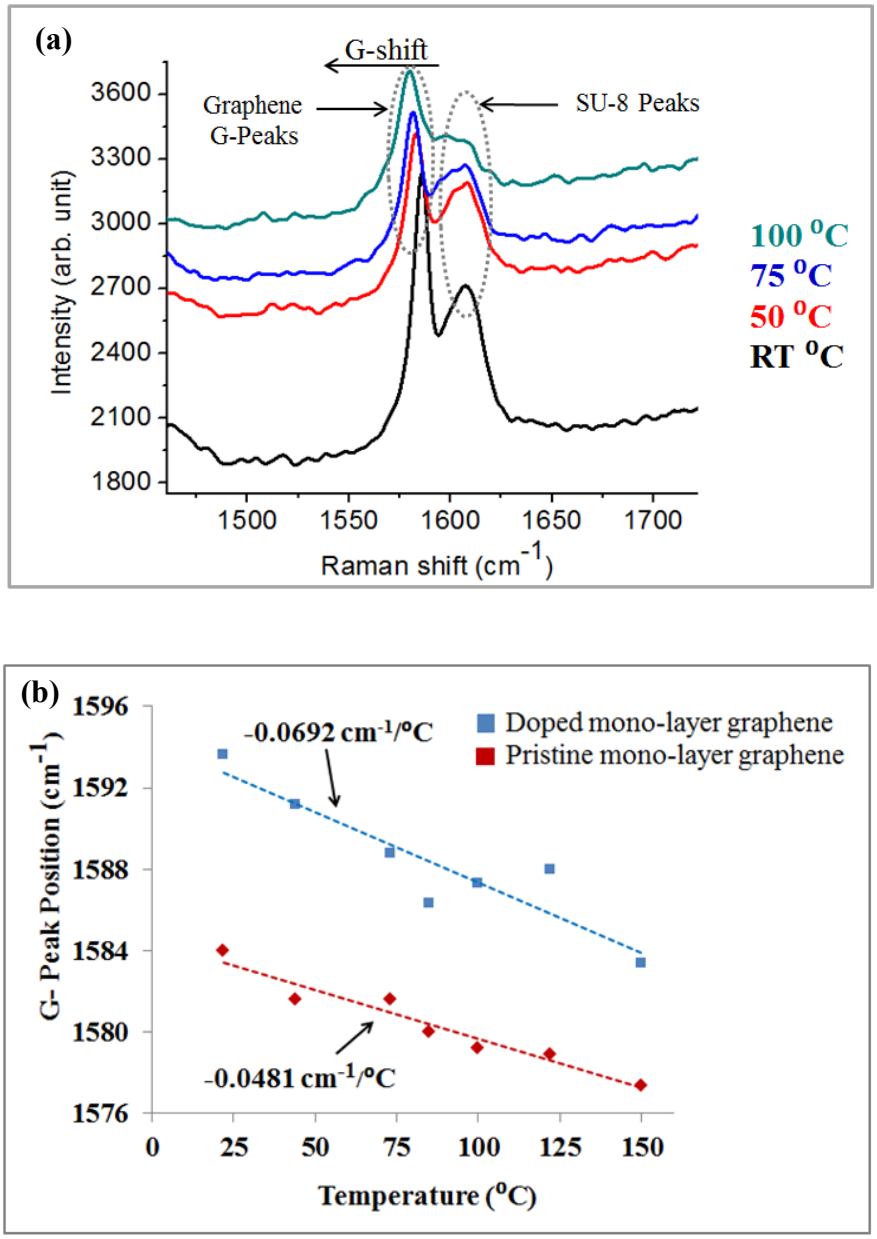
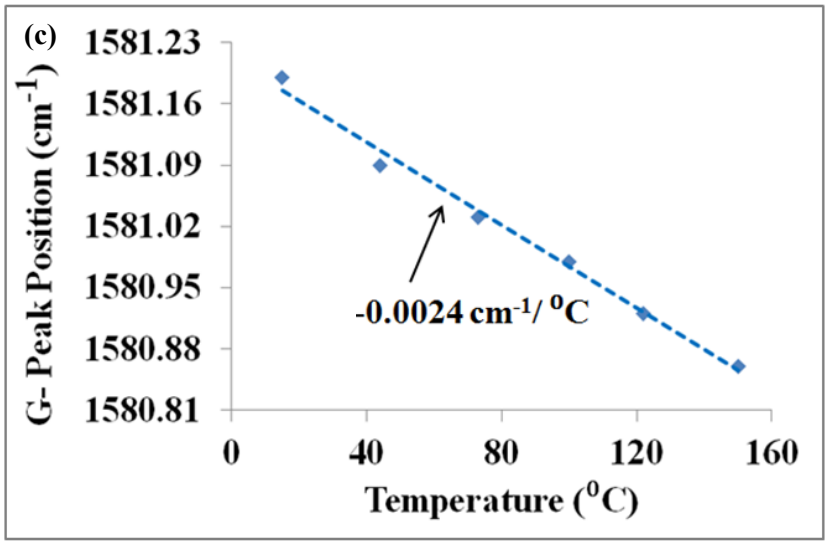


Figure 4.13 (a) Raman spectra of *n*-doped graphene at different temperatures. (b) Comparison of temperature dependence between pristine and *n*-doped monolayer graphene sheets. (c) Temperature dependence of bi-layer graphene. The slope of fitting curve represents the extracted temperature coefficient of G-band peak.

Figure 4.13 (cont'd)



The mechanism of the temperature-dependent downshift of the G-band peak is the elongation of the C-C bonds due to thermal expansion or an harmonic coupling of phonon modes [28]. The temperature dependence of the G-band can be represented by $\omega = \omega_0 + XT$, where ω is the frequency of the G-mode, X is the first-order temperature coefficient defined by the slope of the temperature dependent curve, T is the initial temperature value, and ω_0 is the G shift at the initial temperature. The measured frequency change $\Delta\omega = \omega - \omega_0$ can be written as [29]: $\Delta\omega = (X_T + X_V)\Delta T = \left(\frac{\partial\omega}{\partial T}\right)\Delta T + \left(\frac{\partial\omega}{\partial V}\right)\Delta V$, where X_T and X_V are the frequency shifts due to the intrinsic temperature effect as well as the thermal expansion that induces a volume change. The similar effect was also reported in [30], where the G-band peak of suspended graphene shifted to a lower value as a tension force was applied to its surface. Therefore, the G-band shift can be used as an indicator not only for thermal impact but also for mechanical impact on graphene.

It is of note that the Si/SiO_2 substrate does not strongly affect the thermal coefficient (X) since the measured G-band at ~ 1582 cm^{-1} is made up of optical phonons due to the in-plane vibrations. In addition, the E_{2g} symmetry of the G-band confines the motion of the atoms to the plane of the carbon atoms [31]. The out-of-plane vibrations (ZO phonons) in graphene are not coupled to the in-plane motion that defines the G-band spectrum position. The out-of-plane vibrations are expected to be more associated with the substrate influence [32]. Therefore, the G-band temperature dependence is mostly the properties of the graphene layer rather than the substrate characteristic. Furthermore, the thermal expansion coefficient for SiO_2 is low (2.6×10^{-6}), which does not induce thermal stress to the graphene layer.

4.4 Conclusion

In summary, we demonstrated a doping technique for making *n*-type GNM transistors with high chemical stability and low defect density, using SU-8 as the electron dopant and encapsulation simultaneously. The *n*-type semiconducting properties of the SU-8 doped grapheme were confirmed by the Raman spectra of the as-doped graphene, the negative shift of the Dirac point of the transistors, and the change in the energy position of the Fermi level. The influence of the SU-8 doping on the transport properties of the GNM transistors was also studied, and results were found to be consistent with the previously reported data.

The *n*-type effect of the as-doped devices was demonstrated to be chemically stable in air and completely reversible. Additionally, the *n*-doped graphene FET was stable between - 22 °C and 100 °C with no significant shifting in the Dirac point. The temperature effect on the crystalline structures doped and pristine graphene was also studied. The G-mode of the doped mono-layer graphene was demonstrated to have a greater sensitivity to temperature in

comparison to the pristine graphene, whereas the doped bi-layer graphene showed a relatively lower sensitivity.

Our developed fabrication of the GNM FETs is compatible with conventional microfabrication technology, which makes it a promising technique for the mass production of graphene electronics. Further development in flexible graphene electronics with SU-8 self-encapsulated doping layers also presents tremendous opportunities for future applications in various fields, such as flexible integrated circuits that will be discussed in the next chapter.

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5 GRAPHENE LOGIC CIRCUITS BASED ON A METAL SU-8 – GRAPHENE TECHNOLOGY

5.1 Introduction

Building on previously developed graphene engineering and doping techniques, this chapter will discuss the design, fabrication, and characterization of complementary two, *n*-type and *p*-type, transistor graphene integrated logic circuits on both rigid and flexible substrates. A technology, metal – SU-8 – graphene (MSG) was proposed for building graphene-based integrated circuits as an alternative to complementary metal-oxide-semiconductor (CMOS) technology.

5.2 E-beam Lithography of SU-8

In Chapter 4, we have demonstrated that SU-8 is an effective and reliable doping and encapsulation material for making *n*-type graphene field effect transistors (FETs). However, graphene logic circuits requires making both *n*-type and *p*-type transistors monolithically on a single substrate. Therefore, it is very important to develop a technique capable of selective doping and patterning *n*-type graphene using SU-8. Previously, photolithography of SU-8 has been widely used in microfabrication processes that required thick photoresist structures, but this method usually suffers from limited resolution and is not suitable for patterning nanoscale features. It has been reported that SU-8 with a thin thickness can be exposed using e-beam lithography to achieve small feature sizes down to 30 nm [1, 2]. The chemical reaction of SU-8 during e-beam exposure is similar to that during ultraviolet (UV) exposure. In both cases, SU-8 behaves as a negative resist. Upon irradiation, the photo-acid generator (PAG) decomposes to a photo-acid (hexaflouroantimonic acid) that causes a highly cross-linked and insoluble polymer.

In this section, we carefully calibrated the parameters of SU-8 e-beam lithography to achieve sharp and high-resolution patterns with minimal disturbance to the properties of graphene. For all experiments, we used the commercially available SU-8 2000.2 and SU-8 3005. The resist was spin-coated on the substrate with a spin speed of 6000 rpm to realize a thin layer of SU-8 of less than 1 μm. Different SU-8 thicknesses can be achieved by selecting different SU-8 models (2000 and 3000 series) and changing the spin speed. If a thinner SU-8 layer is desired, SU-8 thinner such as cyclopentanone can be added to the original SU-8 to further reduce the viscosity of the resin. Following spin coating, the SU-8 film was soft baked at 65 °C for 2 min and then at 95 °C for 2 min. The soft-baked SU-8 was exposed to e-beam using JEOL 840, which was operated at 35 kV with beam current of 25 pA. Then the exposed resist was developed by SU-8 developer for 1 min, followed by immersion in isopropanol alcohol (IPA) and a rinse with deionized (DI) water. Finally, the samples were post-baked at 95 °C for 3 min.

Since the e-beam voltage and current are fixed for the instrument, the minimal line-width is mainly determined by the beam dose of the e-beam lithography. In order to study the resolution limit of e-beam exposed SU-8 patterns, the SU-8 resist were exposed using different areal doses between 3 and 300 $\mu C/cm^2$. Figure 5.1 shows the optical microscope images of the resulting patterns. It can be seen that the e-beam writing resolution was significantly affected by the beam dose. Large areas of undeveloped SU-8 residues were observed around the desired patterns at high e-beam doses of over 270 $\mu C/cm^2$ (Figure 5.1 (a) and (b)), which broadened randomly the desired patterns. This was mainly caused by the scattering of impinging electrons at the resist interface, which leads to the over exposure of a larger SU-8 area. Therefore, using a smallest effective dose is considered to be the best solution to significantly decrease SU-8 residues and improve pattering resolution.

Preliminary result shows that the minimum effective areal dose for full exposure of ~ 0.5 μm thick SU-8 was ~ 3 μC/cm^2. It is of note that these residues were hard to remove even before the post-baking treatment.

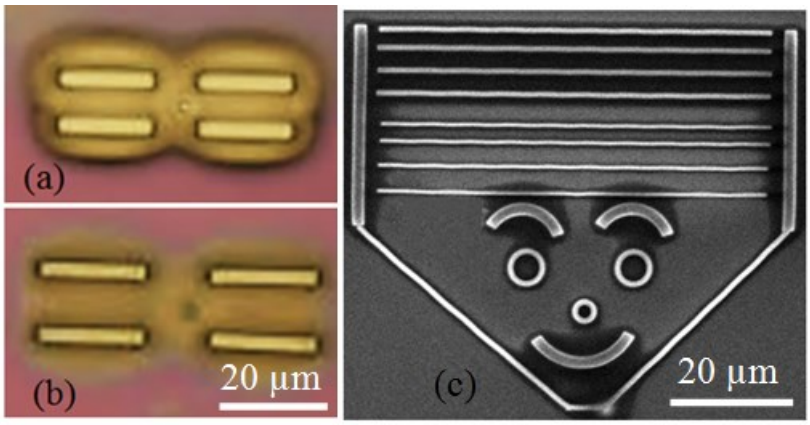


Figure 5.1 SU-8 patterns with various feature sizes (500 nm to 3 μm), exposed using different areal doses of: (a) 300 μC/cm^2, (b) 15 μC/cm^2, (c) 4 μC/cm^2.

5.3 Graphene Inverter Circuit

5.3.1 Fabrication of graphene circuit

One great benefit of using e-beam lithography to expose SU-8 is the ability to selevtively pattern and *n*-dope a graphene sheet at the nanoscale. In this section, we developed a method to realize a graphene inverter circuit (logic NOT gate), by integrating both *n*- and *p*- type graphene FETs on a single substrate. The graphene transistors were constructed monolithically using a single graphene sheet, where the SU-8 coated graphene was an *n*-type region and the uncoated graphene was a *p*-type region, as schematically shown in Figure 5.2 (a). The SU-8 doping and patterning followed the aforementioned methods. Three metal electrodes were constructed on the graphene sheet to form two transistors, via e-beam lithography, metal deposition, and the metal lift-off patterning. The two transistors shared a same back gate as an input voltage terminal (V_{in}). The source and drain contacts of the two

transistors were connected together for use as an output voltage terminal (V_0). Moreover, to avoid impinging electrons, a sacrificial layer of PMMA or Cu is required. After SU-8 development, the sacrificial layer can then be dissolved by acetone or $FeCl_3$ for PMMA and Cu respectively.

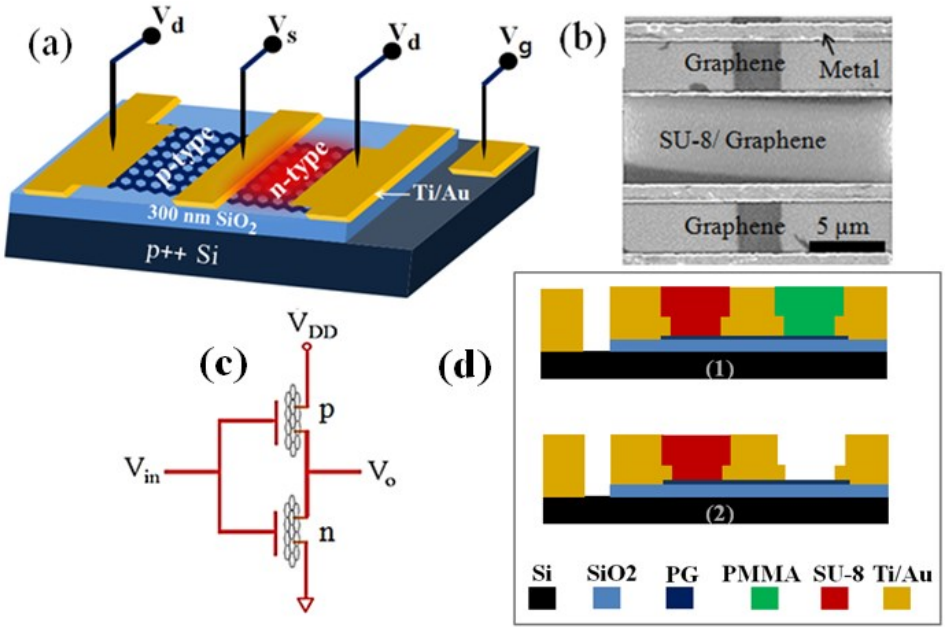


Figure 5.2 An integrated graphene inverter: (a) the schematic of the circuit fabrication; (b) the SEM image of the fabricated inverter; and (c) the circuit layout.(d) Schematic of the fabrication technique to avoid impinging electrons.

5.3.2 Characterization of graphene circuit

To verify the formation of the *n*-type and *p*-type transistors on the same graphene sheet, the transfer resistances R_p and R_n between the source and drain contacts of the individual FETs were measured as a function of the applied voltage V_{in} (Figure 5.3). The measured Dirac points of both the *n*-type and *p*-type graphene sheets were at -27 V and 17 V, respectively. By connecting the *p*-type FET to V_{DD} and the *n*-type FET to the ground, a Dirac point splitting

along the V_{in} axis and then the complementary configuration was achieved within the region between two of Dirac points.

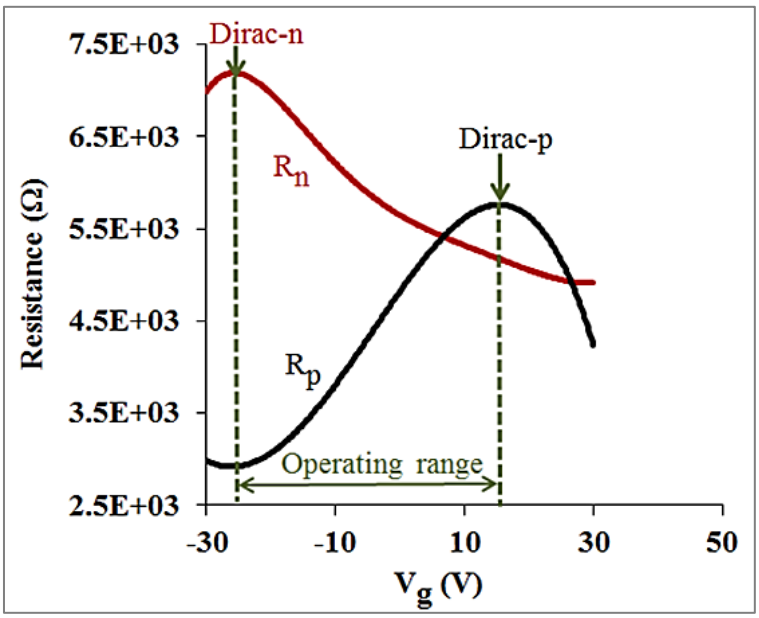


Figure 5.3 Resistance curve (R *vs* V_{in}) of graphene transistors schematically illustrated in Figure 5.1, measured at room temperature. R_n and R_P corresponded to the transfer resistances of the *n*-type and *p*-type graphene regions, respectively.

The inverter function was demonstrated by connecting the source of the *n*-type FET to the ground, the source of the *p*-type FET to a supply voltage (V_{DD}), and the output (V_0) to the common drain of the FETs. The output voltage for this configuration was given by $V_0=V_{DD}$ $R_n/(R_p+R_n)$. The voltage transfer characteristic of the fabricated inverter is given in Figure 5.4. The two FETs operated in the range between the Dirac points, where the increase in V_{in} caused the decrease of R_p and the increase of R_n, thus the increase in the ratio of R_n/R_p. As a result, V_0 decreased with the increase in V_{in}, leading to the voltage inversion. Away from the Dirac points, the saturation of the output voltage V_0 resulted in the approximately

constant ratio of R_n/R_p, when V_{in} < - 27 V for the *n*-type FET and V_{in} > 17 V for the *p*-type FET. Due to the small band gap of the doped gaphene, the output voltage could not saturate to zero or V_{DD}, indicating that the as-fabricated graphene inverter could not be completely turned off. The voltage gain of the inverter was much less than 1, as determined by $A = dV_0/dV_{in}$. The small voltage gain of the fabricated inverter could be mainly due to the very small change of the transistor resistances around the Dirac points. The voltage gain can be relatively increased by decreasing the oxide thickness. The swing voltage of the inverter was 3 mV at V_{DD} = 10 mV. The threshold voltage (V_{TH}), which is the input voltage at the maximum voltage gain of the inverter, was approximately 5.6 mV (V_{in}=V_{TH}) and slightly greater than V_{DD}/2, which is similar to the value of conventional CMOS inverters.

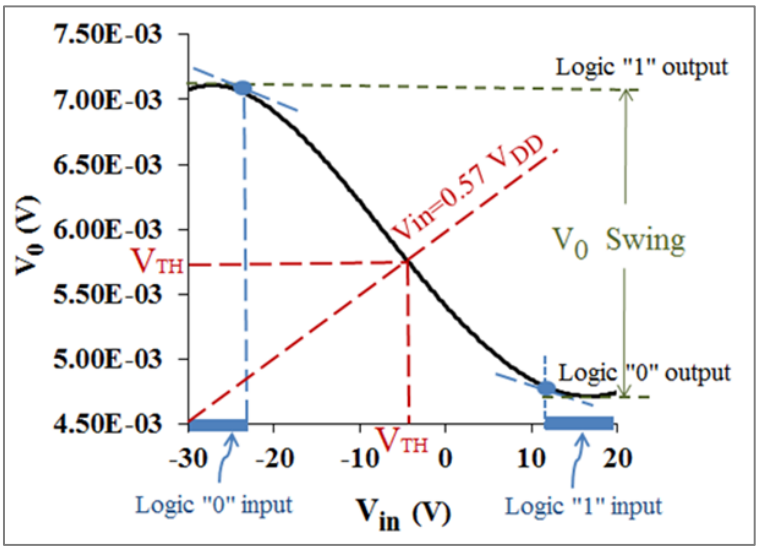


Figure 5.4 Voltage transfer characteristic, demonstrating a logic inverter function.

5.4 Flexible Graphene Transistor

Our developed metal - SU-8 - graphene technology can also be applied in the development of flexible graphene transistors. Flexible transistors have recently received wide attention due to its multiple potential applications including flexible screen [3], flexible solar cells [4], and

biomedical applications [5]. Conventionally, the fabrication of flexible transistor has used amorphous silicon or organic polymers [6]. However, the electron mobilities of these materials are low, which constrain their applications in making low frequency transistors and integrated circuits. The key advantages of graphene are its fast electron mobility and excellent mechanical properties, which are essential for fabricating flexible and stretchable electronic circuits [7-9].

In this work, two different approaches were explored to fabricate graphene FETs on mechanically flexible Parylene-C substrates. Parylene has been widely used as a polymeric material for micromachining [10]. It can be conformally coated at room temperature by chemical vapor deposition (CVD). Due to its electrical insulation, chemical stability, and biocompatibility, it has also been used as a structural and encapsulating material for implantable electronic devices and embedded electrodes [11].

5.4.1 Top-gated graphene FETs on mechanically flexible Parylene-C substrates

The first approach used a top gate configuration in the design and fabrication of the flexible graphene FETs. The fabrication of the trasistor began with the deposition of a 10 μm Parylene layer on a silicon substrate, which was used as a mechanical carrier during the subsequent fabrication processes. Graphene was transferred onto the Parylene surface through the Scotch tape method, located with optical microscope, and confirmed by Raman spectroscope (Figure 5.5). After that, source and drain electrodes were fabricated on the graphene sheet with e-beam lithography, Ti/Au metal thermal evaporation, and metal lift-off. Then the graphene sheet was tailored to a regular shape by oxygen plasma etching. To fabricate a FET gate, ~ 200 nm SU-8 was spun on the whole chip, followed by soft-baking at 65 °C for 2 min and then at 95 °C for 2 min. In this case, SU-8 was used as a gate dielectric layer and an *n*-type doping source. The chip was exposed using photolithography for 20 sec

and then hard-baked at 110 °C for 30 min. Next, a metal contact was deposited and patterned on top of the SU-8 dielectric layer as a top gate electrode. Finally, the flexible Parylene film was separated from the Si substrate, carrying the fabricated graphene transistors. Figure 5.6 shows the schematic of device fabrication.

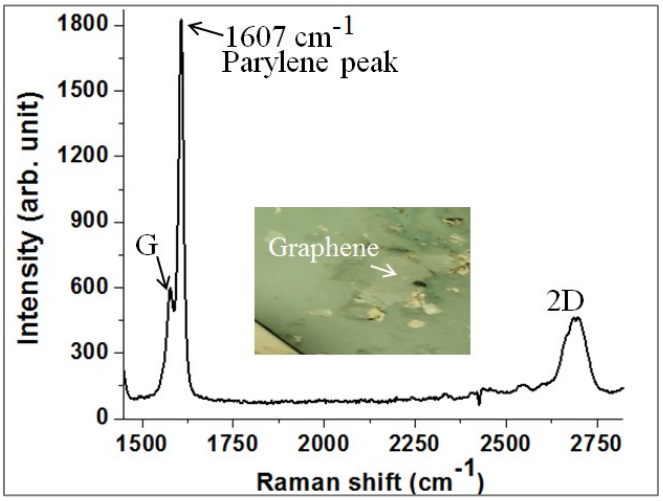


Figure 5.5 Raman spectrum of graphene transferred on a Parylene substrate. Inset is the optical microscope image of the graphene.

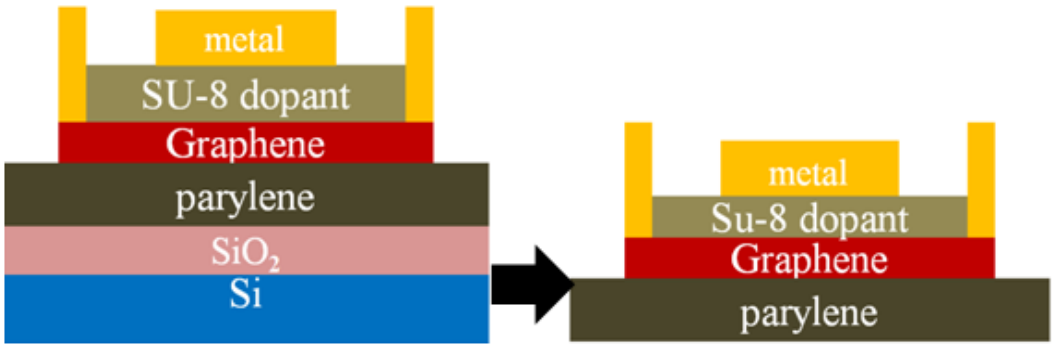
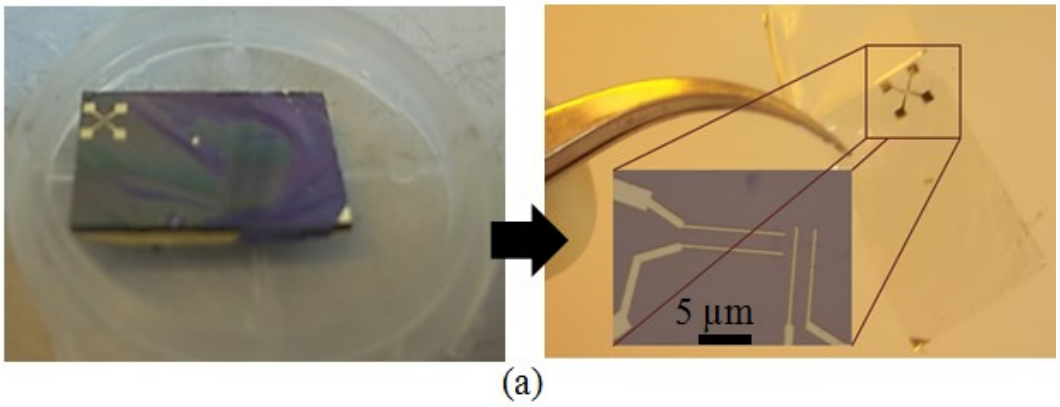
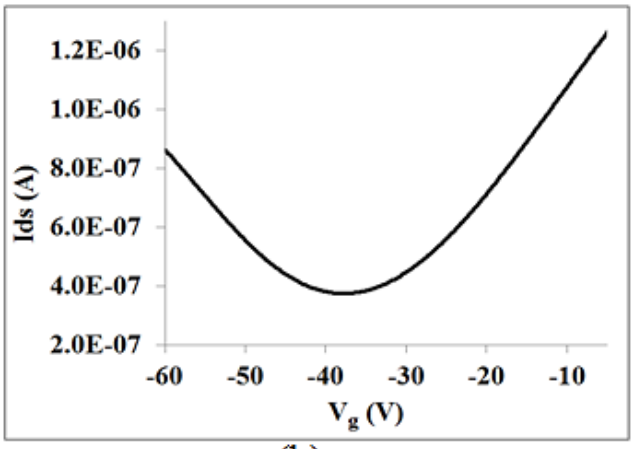


Figure 5.6 Schematic of the top-gated, *n*-type graphene FET before and after removing the carrier substrate.

Figure 5.7 show a representative flexible graphene transistor fabricated using the above method and the I_{ds}-V_g characteristic of this device. The Dirac point of the SU-8 doped graphene was around – 38 V, suggesting a strong *n*-type transport property that was consistent with the previous results in Chapter 4. While we realized flexible graphene transistors using the top gate technique, this device configuration is only suitable for making *n*-type graphene FETs on flexible substrates.



(a)



(b)

Figure 5.7 (a) A fabricated graphene *n*-type FET and (b) the measured I_{ds}-V_g characteristic of the device

5.4.2 Back-gated graphene FETs on mechanically flexible Parylene-C substrate

In the second approach, a back gate configuration was designed, with which both *n*- and *p*-type transistors can be constructed on flexible substrates, as shown in Figure 5.9 (a) and (b),

respectively. During the fabrication, a layer of a metal was deposited as the back gate electrode, followed by the deposition of an insulated layer (SU-8) as the gate dielectric layer. SU-8 was completely cross-linked by soft-baking, UV exposure, and long post-baking subsequently. After that, mechanically exfoliated graphene was transferred onto the SU-8 substrate. Then Ti/Au electrodes were fabricated on top of graphene as the source and drain contacts, through thermal evaporation, e-beam lithography, and metal lift-off processes. After that, *n*-type graphene could be obtained by covering the channel region with SU-8 electron dopant, while *p*-type graphene could be realized by leaving the channel region uncovered. Finally, the flexible transistors were released by separating the Parylene film from the silicon substrate. A representative *p*-type back-gated transistor and its current transfer property are given in Figure 5.10 (a) and Figure 5.10 (b). demonstrates the flexibility of the as-fabricated graphene transistor, which could sustain mechanical twisting and bending (> 90°).

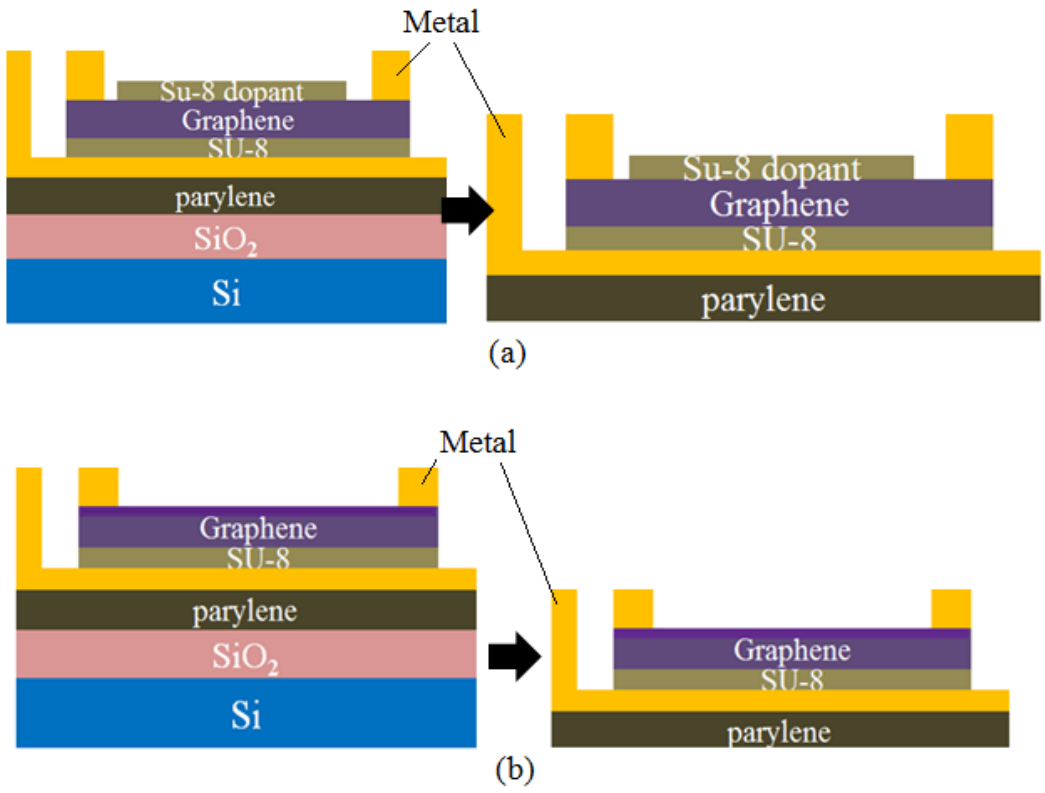


Figure 5.8 Device configurations of (a) n-type and (b) p-type back-gated graphene FETs.

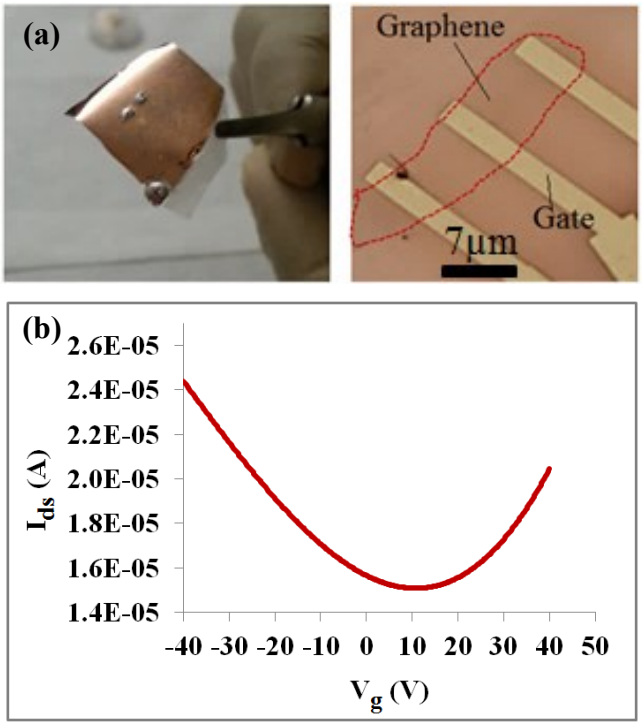


Figure 5.9 A fabricated *p*-type back-gated, flexible graphene transistor before and after removing the carrier substrate. Silver paste was applied to the contacts in order to avoid punching the substrate during device testing. Dashed area shows the transparent graphene sheet. (b) The current transfer characteristic of the device, showing the *p*-type transport property of the graphene.

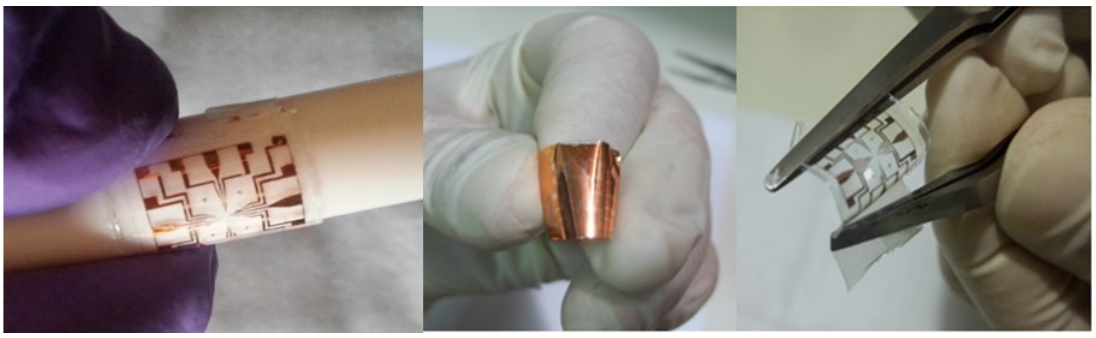


Figure 5.10 Mechanical flexibility of the as fabricated graphene transistors.

5.5 Conclusion

Graphene doping at a dedicated area represents a practical method for MSG technology. Building on the graphene doping technique, a graphene-based inverter has been fabricated and characterized, which exhibits clear voltage inversion property. However, it is difficult to completely turn off the inverter due to the small band gap of the doped graphene, in addition to the small voltage gain compared to CMOS inverters. Flexible graphene electronics with SU-8 doping have also been demonstrated, which provide tremendous opportunities for future applications of graphene electronics in various fields, such as biomedical systems and flexible integrated circuits.

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6 GRAPHENE APPLICATIONS IN NANOSENSING

6.1 Introduction

As discussed in Chapter 1, graphene has several unique properties. First, it has a large specific surface area (2630 m^2/g), meaning that all atoms can be considered as surface atoms that are capable of adsorbing different kind of molecules. Second, graphene has inherently low electrical noise [1] because of its high quality crystal lattice and two dimensional architecture. Third, graphene has high electron mobility (2×10^5 $cm^2V^{-1}s^{-1}$) at room temperature and high thermal conductivity (15000 $cm^2V^{-1}s^{-1}$ for graphene on SiO_2). These unique properties make graphene an ideal material for building not only nanoelectronics, but also nanosensors. Therefore, in this chapter, we explored several potential applications of graphene in nanosesing for the detection of chemical molecules, temperature, and gas flow rate.

6.2 Graphene Inter-sheet Sensor for Chemical Detection

6.2.1 Graphene inter-sheet and intra-sheet effects

To date, a variety of graphene-based nanosensors have been demonstrated, where the sensing mechanism mainly relied on the surface doping and edge effects on their intra-sheet transport properties [2-6]. Few-layer graphenes (FLGs), with their sub-nanometer inter-sheet spacing, can enable new transduction mechanisms if inter-sheet effects can be exposed. The merits of this exposure include inter-sheet tunneling, doping, and other effects besides the enhanced edge effects due to the extra sides. Such inter-sheet effects can be a function of the spacing change caused by molecule adsorption/desorption, force/displacement, pressure, surface tension, or thermal energy, and can potentially enrich the applicable transduction mechanisms remarkably. All these effects will be available if electrical contacts can be made on different

layers of FLGs. However, little effort has been made to the development of inter-layer graphene sensors due to the difficulties in structuring exposed inter-sheet steps in FLGs.

Figure 6.1 schematically illustrates the sensing mechanisms of the "intra-sheet" and "inter-sheet" structures.

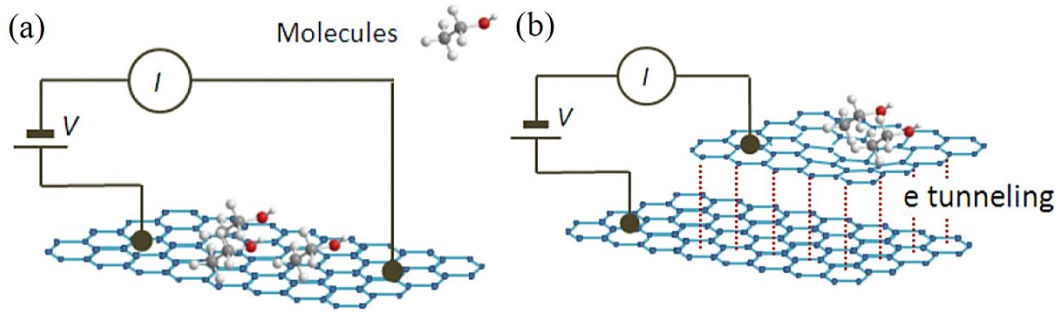


Figure 6.1 Schematic diagrams of (a) an "intra-sheet" and (b) an "inter-sheet" graphene sensors.

The commonly used "intra-sheet" structure (Figure 6.1 (a)) is based on the change of the transportation properties inside a single layer of a graphene, induced by external stimuli. Whereas in the "inter-sheet" version (Figure 6.1 (b)), both the top and bottom layers of a bilayer graphene (or a FLG) are used as active elements, so the sensing response is based on the change of the electrical properties between the adjacent graphene layers (e.g., tunneling current, doping, and edge effects), upon exposure to the external stimuli. For example, when it is used as gas molecule sensors, the electrical resistance of "intra-sheet" sensor is changed by the absorption or desorption of the gas molecules that act as donors or acceptors. Its response is proportional to the quantity of the molecules that absorbed to or desorbed from the graphene surfaces. However, for the "inter-sheet" sensor, an exponential relationship between the tunneling current through the two layers of a bilayer graphene and the inter-sheet distance makes it possible to significantly increase the sensitivity of the "inter-sheet" sensor. With few molecules attached onto the top sheet, local separation of the bilayer graphene can be shortened due to van der Waals forces, and the tunneling current will increase accordingly.

As the amount of the attached molecules increases, inter-molecular forces can induce surface tension, which may locally distort the top sheet and result in the increment/decrement of tunneling current.

Motivated by the potential increase of sensitivity, we designed, fabricated, and characterized "inter-sheet" sensors. The sensing feasibility of the fabricated devices was demonstrated upon exposure to various types of vapor molecules, including ethanol (donor-type) and water vapor (acceptor-type) molecules. The sensing behavior of the "inter-sheet" sensors was compared with "intra-sheet" sensors fabricated on the same or different graphene sheets. Details are discussed in the following sections.

6.2.2 Method

To make the inter-sheet graphene sensor, high quality mono-/bilayer graphene sheets were prepared with the mechanical exfoliation method and then transferred onto SiO_2/Si substrates. After locating the graphene sheets on the substrate, Raman spectroscopy was used to further identify their thicknesses based on the characteristics of G and the second-order Raman 2D bands. Figure 6.2 (a) shows a mechanical exfoliated graphene sample that consisted of both monolayer (region A) and bilayer (region B) regions on a same sheet. The Raman spectra and Lorenzian fittings of the 2D bands are given in Figure 6.2 (b). For the region A, the G and 2D band appeared at 1586 $cm^{-1}$and 2673 cm^{-1}, respectively. The intensity ratio of the 2D/G was approximately 2.68. Combined with the 2D/G ratio, the single peak of its 2D band (the bottom inset in Figure 6.2 (b)) confirmed that the region A was a monolayer graphene region. While for the region B, the intensity ratio of G and 2D bands, which appeared at 1578 cm^{-1} and 2682 cm^{-1}, was around 1.02. The 2D band of its Lorentzian fitting contained four peaks (the top inset in Figure 6.2 (b)), demonstrating a bilayer graphene on the area B.

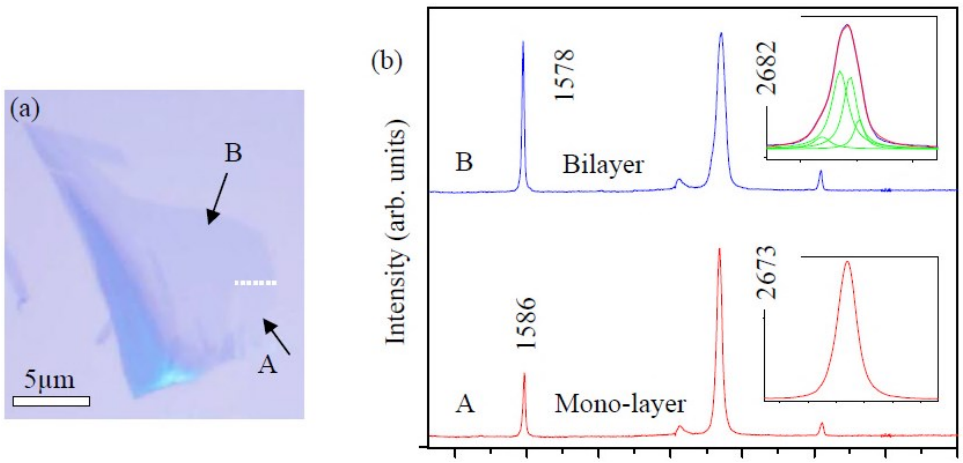


Figure 6.2 (a) Example of a mechanical exfoliated graphene containing both mono- and bi-layer regions. (b) Raman spectra of different regions. The top and bottom insets represent the enlarged 2D bands of regions B and A, respectively.

Devices were fabricated using conventional planar micro/nanomachining techniques. The processes for both "intra-sheet" and "inter-sheet" structured graphene sensors are schematically depicted in Figure 6.3. Briefly, graphene sheets prepared from the mechanical exfoliation were located on the SiO_2 (300 nm)/Si substrates. Then, the graphene sheets were engineered to regular shapes by a fine tuned oxygen plasma etching (OPE) method. This OPE process was developed not only to tailor the edge shapes but also to selectively thinner the thick graphene regions to a target number of layers (mono- or bi-layer) by removing an individual layer at each time, as discussed in Chapter 3. After that, Ti (5 nm)/Au (100 nm) electrodes were fabricated on the same (Figure 6.3 (a)) or different (Figure 6.3 (b)) graphene sheets through e-beam lithography and metal thermal evaporation processes. Poly(methyl methacrylate) (PMMA) served as a protective layer for the OPE and a mask for metal lift-off step. After dissolving PMMA with acetone and isopropanol alcohol (IPA), the devices were rinsed with deionized (DI) water and then dried with nitrogen. Finally, the sensors were degassed at 1×10^{-7} Torr for 12 hrs prior to testing.

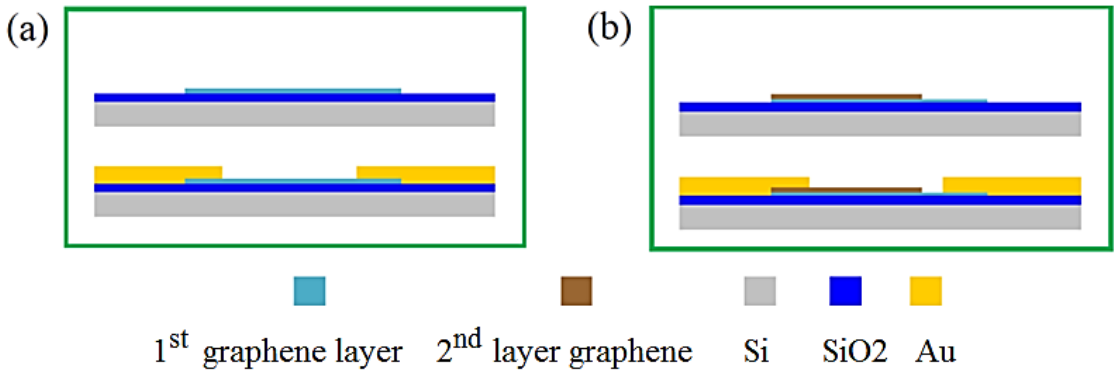


Figure 6.3 Schematic processes for fabricating (a) "intra-sheet" and (b) "inter-sheet" graphene sensors.

6.2.3 Result and discussion

"Intra-sheet" and "inter-sheet" sensors were initially fabricated on different graphene sheets to study for their vapor sensing behavior. Optical images of the fabricated "intra-sheet" and "inter-sheet" sensors are given in the Figure 6.4 (a) and (d), respectively. Raman spectra of the graphene areas of these sensors are also given in Figure 6.4 (b) and (e), respectively. The corresponding G and 2D bands of the graphene in the "intra-sensor" sensor were located at 1581 cm^{-1} and 2688 cm^{-1} with close intensities. The four Lorentzian peaks fitting of the Raman 2D band shown in Figure 6.4 (c) indicates a bilayer graphene structure. The Raman spectra of the graphene in the "inter-sheet" sensor are shown in Figure 6.4 (e) and (f). In area A, the intensity of the 2D band (2676 cm^{-1}) was near 3 times stronger than that of its G band (1585 cm^{-1}) and the 2D band (Figure 6.4 (f)) contained only one Lorentzian peak. Whereas in area B, the intensity ratio of the 2D band (2693 cm^{-1}) and the G band (1582 cm^{-1}) was about 1, and four Lorentzian peaks were needed to fit its 2D band (Figure 6.4 (f)). These confirmed that the graphene areas A and B are mono- and bi-layered graphene, respectively.

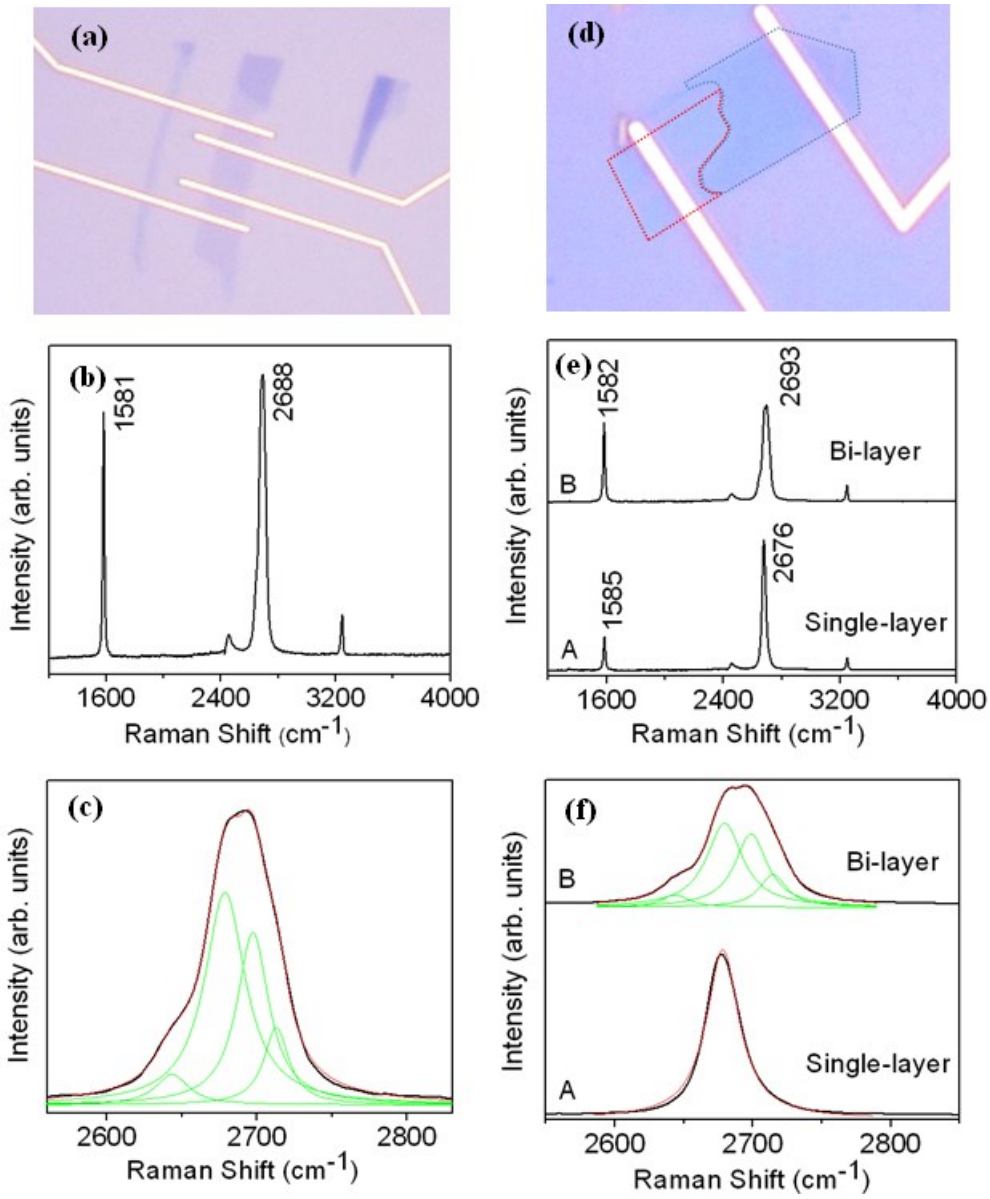


Figure 6.4 (a) Optical image, (b) Raman spectrum and (c) the enlarged Raman 2D band and its Lorentzian fitting of the bilayer graphene for an "intra-sheet" sensor. (d) Optical image, (e) Raman spectrum and (f) the enlarged Raman 2D bands and their Lorentzian fittings of the mono- and bi-layer graphene regions for an "inter-sheet" sensor.

Using the testing setup shown in Figure 6.5, the time dependencies of sensors, illustrated in Figure 6.6, were monitored using a picoameter Keithley 6487, before and after introducing 0.5% ethanol vapor (molar concentration) in nitrogen, with a 0.5 V voltage applied to both

the sensors. Data were collected after the resistance of each sensor reached its steady state, which can be attributed to the equilibrium of the vapor molecules adsorption and desorption.

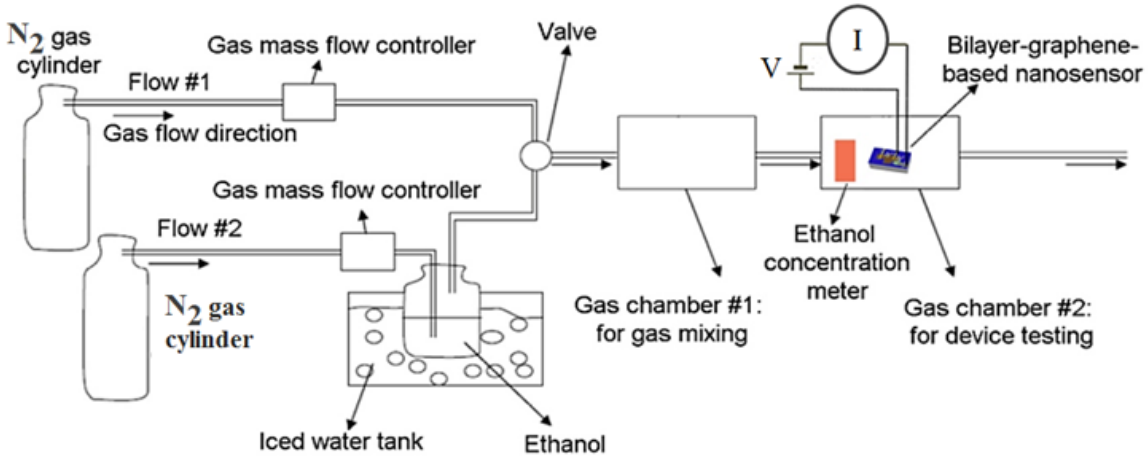


Figure 6.5 Schematic diagram of the testing system for both “intra-sheet” and “inter-sheet” ethanol molecule graphene sensors.

Figure 6.6 shows the resistance responses of these sensors after the introduction of 0.5% ethanol vapor. It can be seen that the resistance of the “intra-sheet” sensor decreased from 12.95 kΩ to 11.98 kΩ when 0.5% ethanol was introduced. This resistance decrease of the “intra-sheet” sensor was consistent with the previously reported results [6] because ethanol molecules serve as electron donors to graphene. As for the “inter-sheet” sensor, it was found from Figure 6.6 (b) that the resistance change had an opposite trend, which increased from 10.50 kΩ (black curve) to 14.96 kΩ (red curve). As the measured resistances highly depend on the occupied area of the graphene between two electrodes, a normalized resistance change ($\Delta R/R$) has been derived as the metrics of the device sensitivity, to eliminate the interference due to sensing area variance. Based on the measured raw data, the $\Delta R/R$ values for the intra-layer and the inter-sheet devices were calculated to be approximately 7.5% and 42.5% respectively, demonstrating that the inter-sheet senor exhibited a much higher sensitivity.

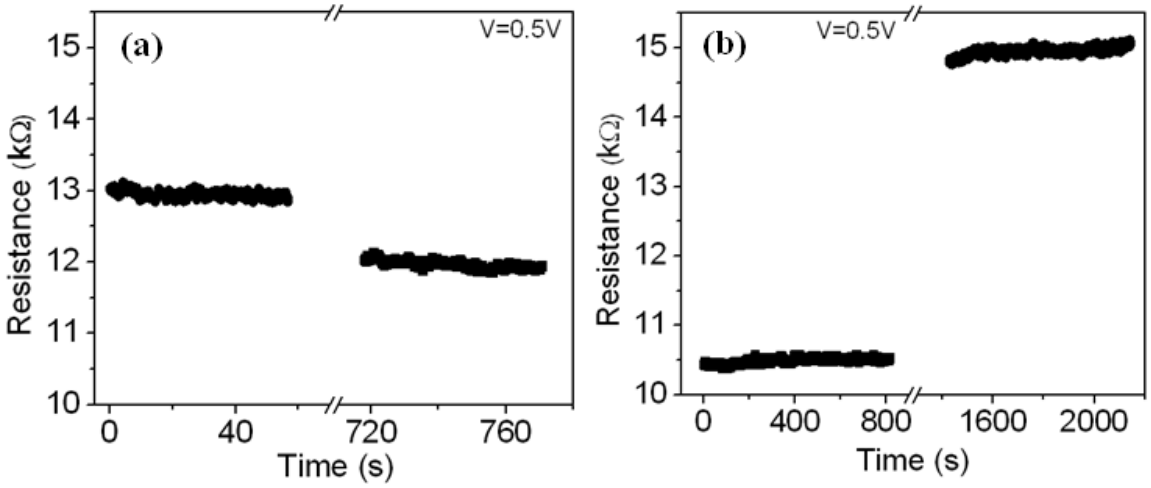


Figure 6.6 Resistance responses of (a) the "intra-sheet" sensor and (b) the "inter-sheet" sensor upon exposure to 0.5% ethanol vapor in nitrogen environment.

To further validate the sensitivity enhancement from the "inter-sheet" structure, we fabricated both "intra-sheet" and "inter-sheet" sensors on a same graphene sheet, as shown in Figure 6.7 (a). This graphene had both a monolayer area A and a bilayer area B, which were also identified with their Raman spectra and Lorenzian fittings of the 2D bands. An "intra-sheet" element was formed between electrodes 1 and 2 and an "inter-sheet" one was formed between electrodes 2 and 3. Similar test was performed by applying a 0.01 V bias to both sensors to avoid Joule heating damage and electrical breakdown of graphene. Figure 6.7(b) and (c) show the resistance responses of the "intra-sheet" and the "inter-sheet" configurations before and after introducing 0.5% ethanol to nitrogen environment. From Figure 6.7 (b), it can be seen that the current of the "intra-sheet" sensor increased from 2.2 μA to 2.67 μA upon exposure to 0.5% ethanol-nitrogen mixture, resulting the $\Delta R/R$ value of ~ 28.3%. In the "inter-sheet" situation, the measured current decreased from 0.55 μA to 0.22 μA, which agreed with the result of the stand-alone inter-sheet sensor. The $\Delta R/R$ was calculated to be ~ 59.6%, which was more than two times higher than that achieved from the on-chip "intra sheet" sensor.

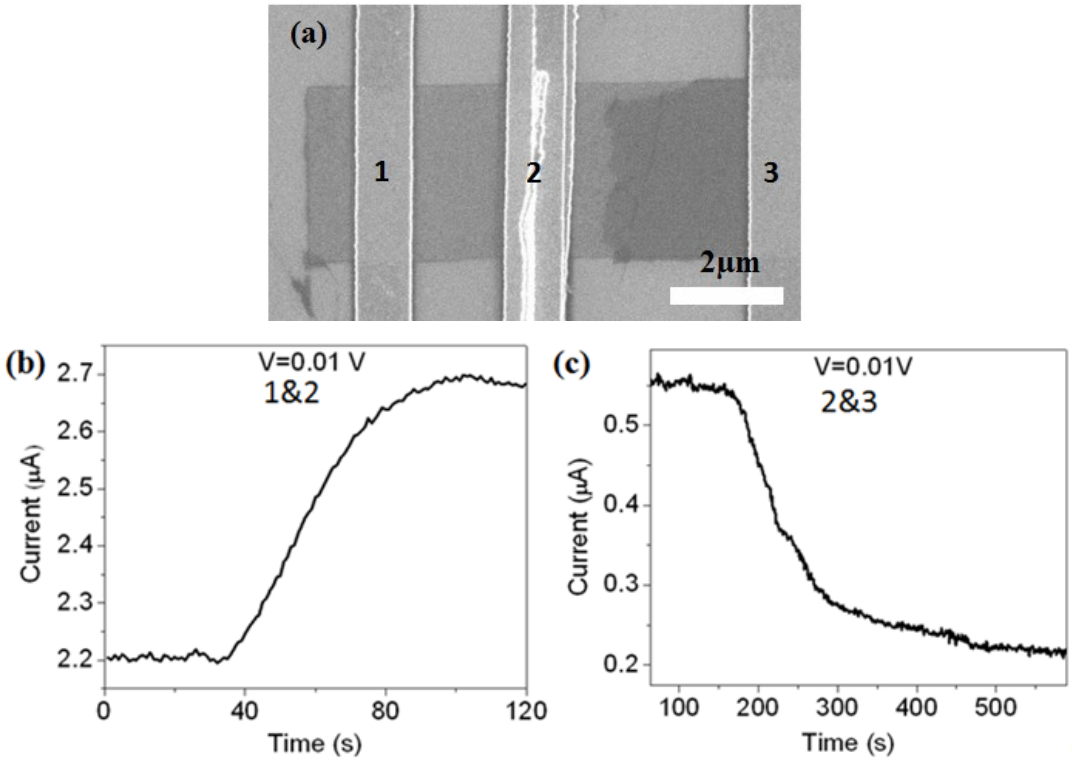


Figure 6.7 (a) SEM image of an "intra-sheet" sensor (electrodes 1 and 2) and an "inter-sheet" sensor (electrodes 2 and 3) fabricated on a same graphene sheet. Graphs (b) and (c) are time dependent responses of the "intra-sheet" and "inter-sheet" resistances before and after introducing 0.5% ethanol into nitrogen.

Both "intra-sheet" and "inter-sheet" sensing elements were also tested using water vapor in a vacuum environment to investigate their responses to the adsorption/desorption of water molecules. (a) shows an "inter-sheet" sensor by fabricating Ti/Au electrodes on two different graphene layers. The light gray and darker regions of the graphene underneath the electrodes were identified to be monolayer and bilayer structures, respectively (Figure 6.8 (d)). Figure 6.8 (b) and (c) show two other "intra-sheet" sensors fabricated on the monolayer and bilayer graphene sheets, as confirmed with their Raman spectra (Figure 6.8 (e) and (f)).

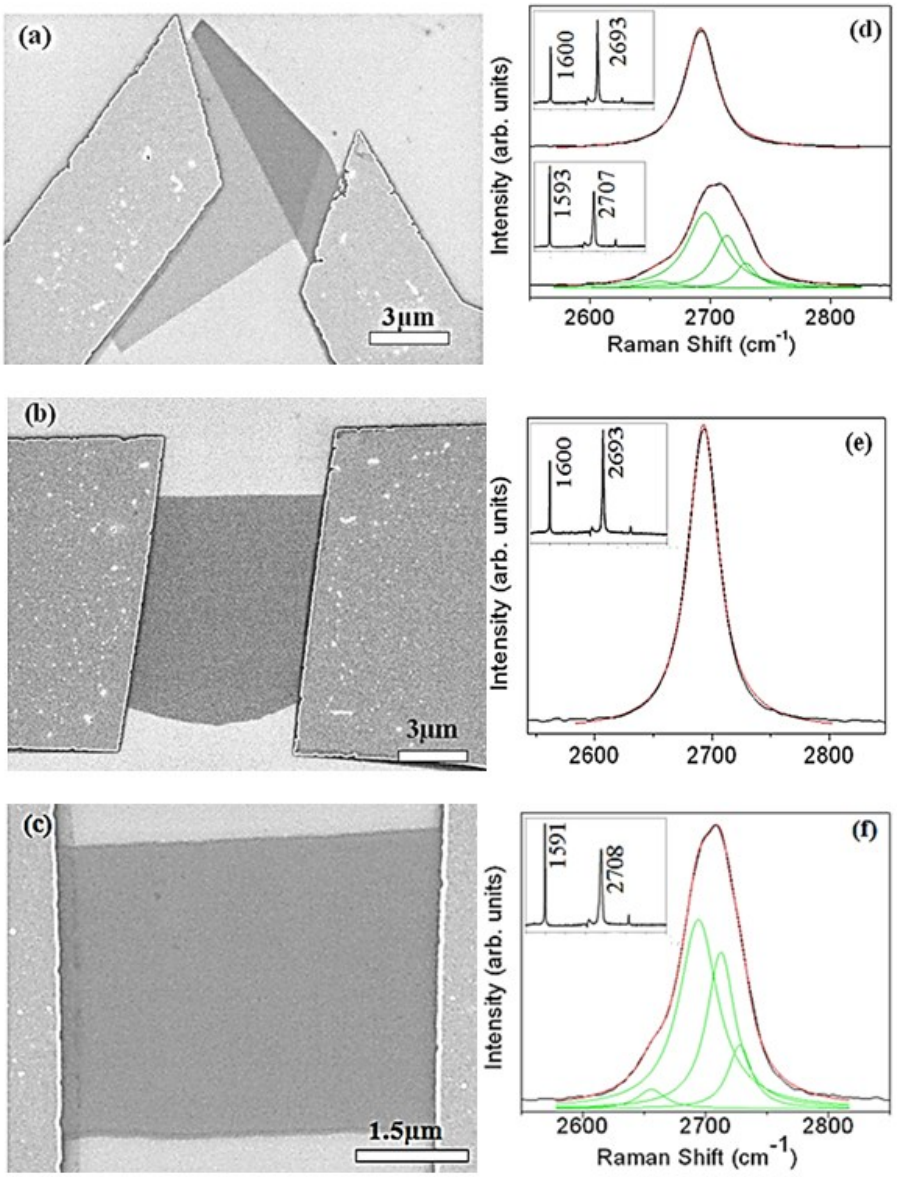


Figure 6.8 (a), (b) and (c) SEM images an "inter-sheet" sensor fabricated on different graphene layers, an "intra-sheet" sensor of fabricated on a monolayer graphene, and an "intra-sheet" sensor fabricated on a bilayer graphene, respectively. (d), (e) and (f) The corresponding Raman 2D bands and their Lorentzian fittings of the graphene samples in (a), (b) and (c), respectively. The insets show the entire Raman spectra of the graphene. The A and B curves in (d) correspond to the mono- and bi-layer graphene regions in (a).

The water vapor responses of the aforementioned "intra-sheet" and "inter-sheet" sensors were characterized in the SEM (Zeiss EVO LS25) chamber. During the experiments, the sample chamber was first pumped to a base pressure of less than 3.3×10^{-3} Pa, in order to remove possibly absorbed vapor molecules on the graphene surfaces of the sensors. Then, water vapor was introduced to the sample chamber and the pressure inside the sample chamber was maintained at 500 Pa. After several minutes, the water vapor source was turned off and the sample chamber was pumped down again to the base pressure. The sensor responses to water vapor in several ON-OFF cycles were monitored. Figure 6.9 (a) plots the current response of the "inter-sheet" sensor in one cycle. It can be seen that the current of the "inter-sheet" sensor had a dramatic decrease when water vapor was introduced into the sample chamber. When the water vapor supply was turned off, the current gradually increased to its original value before the introduction of water vapor. A slow recovery was observed, which is mainly due to the slow desorption of the physically absorbed vapor molecules on the graphene surface at room temperature. This recovering time can be significantly reduced by heating the device to increase the speed of desorption. Similar tests were performed on the "inter-sheet" sensor and the "intra-sheet" sensors in several ON-OFF cycles. Figure 6.9 (b), (c) and (d) show the typical current responses of the "inter-sheet" sensor, the "intra-sheet" sensor on a monolayer graphene, and the "intra-sheet".

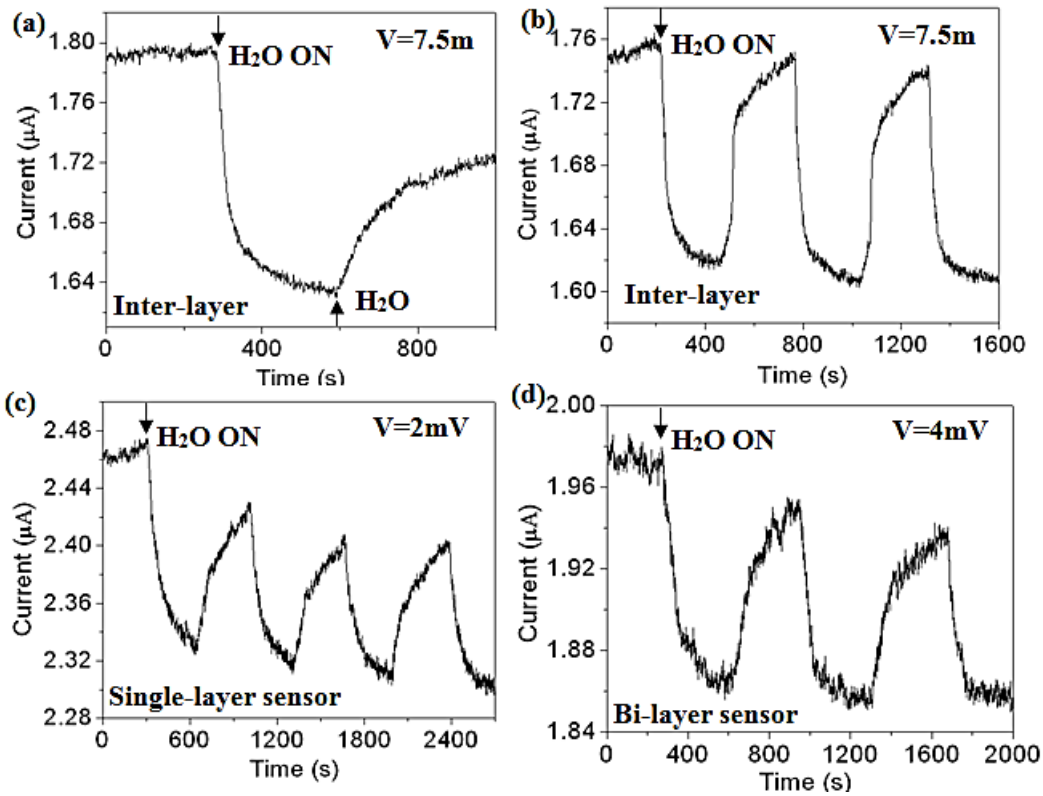


Figure 6.9 (a) Current response of the "inter-sheet" sensor upon exposure to water vapor at a pressure of 500 Pa in the sample chamber within one cycle. (b), (c), and (d) The current responses of the "inter-sheet" sensor, "intra-sheet" sensor on a monolayer graphene and the "intra-sheet" sensor on a bilayer graphene, respectively, in several cycles of water vapor turning ON and OFF.

6.2.4 Discussion of sensing mechanism

The higher sensitivity achieved from the "inter-sheet" configuration is promising for a new group of sensors. This can be attributed to the strong exponential relationship between the tunneling current through the two adjacent layers of the graphene and the inter-sheet distance, due to the absorption of ethanol vapor molecules. Since ethanol molecules act as electron donors, while water molecules act as electron acceptors, it is anticipated that the resistance of the "intra-sheet" sensor decreased when ethanol molecules were adsorbed on the graphene surface, and increased when water molecules were adsorbed [6], as shown in Figure 6.7

(b) and Figure 6.9 (c) and (d). However, it is noticed that, differs from the decreasing on the resistance of the "intra-sheet" sensor, the resistance of the "inter-sheet" sensor increases no matter whether the introduced vapor samples are donor-type (ethanol) or acceptor-type (water) molecules, as shown in Figure 6.7 (c) and Figure 6.9 (a) and (b). These results indicate that the "inter-sheet" sensor exhibits a different sensing mechanism compared to the "inter-sheet" sensor.

Although the exact sensing mechanism of such inter-sheet sensors needs further investigations, we believe that the current tunneling through the top and the bottom graphene layers plays an important role that contributes to the higher sensitivities and the increased resistances of the devices. First, due to the unavoidable absorbates such as photoresist residues and particles on the graphene surface, the as-fabricated graphene are intrinsically acceptor-type [7]. Therefore, the absorption of donor-type ethanol molecules decreases the hole tunneling current through the two layers of the graphene, resulting in the increase of the inter-layer resistance. While in our intra-layer sensor, the monolayer graphene has less activated open edges compared to the bilayer graphene in the inter-sheet sensor, and thus has less chance of being contaminated by those absorbates. In this case, a large portion of the "intra-layer" graphene possibly remains as the intrinsic monolayer graphene. So the resistance decreases when ethanol molecules are absorbed onto the monolayer graphene surface [6]. The other causation for the suppression to the tunneling current through two different graphene layers of the "inter-sheet" sensors could be the increase of the inter-sheet distance. When a large number of molecules are absorbed on the graphene surface at the overlap region of the "inter-sheet" sensors, the transverse intermolecular forces among the vapor molecules would made some changes to the microscopic corrugations [8] of the top graphene layer. This reconstruction of the microscopic corrugation would cause the significant increase on the inter-sheet distance, and thus the suppression on the tunneling

current. For our "inter-sheet" devices, the inter-layer structures possess extra open edges/steps to allow for the adsorption of vapor molecules. Therefore, the increase of the inter-sheet distance could be more prominent compared to doping effect, resulting in the increased resistance.

As a conclusion, although our results clearly demonstrate a completely different sensing characteristic in the "inter-sheet" graphene configuration, further investigations using in-situ measurements can be envisioned to uncover the exact inter-sheet sensing mechanism and improve sensor performance. The inter-sheet effects significantly enrich the applicable transduction mechanisms and provide a promising candidate for sensing various stimuli, such as chemical/biological molecules, force/displacement, pressure and surface tension, with high sensitivity.

6.3 Graphene Sensor for Flow/Temperature Sensing

6.3.1 Overview of flow/temperature sensors

Micro/nanoscale flow sensor offers tremendous opportunities for detecting flow rate in a wide variety of applications, such as microfluidics and lab-on-a chip systems. Modern flow sensor technologies can be classified into two basic categories: thermal-based [9-15] and mechanical-deflection-based [16-21] sensors. The thermal-based sensors usually involve a hot wire configuration at the millimeter scale, which is mainly made of materials with positive temperature coefficients (PTCs), such as tungsten or platinum [15]. However, PTC sensors suffer from self-heating effect and slow responding time. The sensing principle of the mechanical-deflection-based sensors relies on either cantilever deflection or lift force [16-18]. While these devices can achieve fast response and high sensitivity, they are often very fragile and not mechanically stable. Therefore, improved device design and careful selection

of materials are required to maximize sensor sensitivity and sensing range, enhance device reliability, and reduce device size suitable for use in micro and nanoscale systems.

To address these challenges, we propose to use graphene as the sensing material of the thermal-based flow sensor. Graphene is well known to have unique properties that make it an excellent choice for the thermo-flow and temperature sensing applications [22-24]. In particular, graphene has a large surface-to-mass ratio and a higher temperature coefficient of resistance (TCR) than tungsten and platinum, resulting in low thermal inertia and high sensitivity to temperature variation. In addition, the negative temperature coefficient (NTC) of graphene means that its resistance decreases as the environmental temperature increases [23, 25], which enables self-protection of graphene sensors and minimizes sensing error from current-induced Joule heating. Furthermore, the planar design of hot-wire sensors is mechanically more stable because it has no fragile elements such as cantilevers. Finally, our proposed graphene sensors can be built using conventional micro/nanofabrication techniques with nanoscale sizes, low power, and low cost, and thus can be easily integrated with microfluidic components to achieve complex functionality. In this study, we focused primarily on bi- and few-layer graphene devices and secondarily on mono-layer graphene because of its relatively lower temperature dependence due to the elevated intrinsic mobility of charge carriers [25, 26]. The subsequence sections describe the theoretical backgound, design, fabrication process, packaging, as well as characterization of the graphene hotwire flow/thermistor sensors.

6.3.2 Heat convection theory

Graphene has an NTC property and its resistance (R) at a certain temperature (T) can be represented by $R(T) = R(0) - \frac{\hbar/e^2}{4TV_0/\hbar v^2 E_f \tau_0}$ [25] where $\hbar$ is the Plank constant, e is the charge of an electron, v is the velocity, E_f is the Fermi energy, τ_0 is a backscattering rate from

atomically sharp defects in graphene lattice, and V_0 is the characteristic interaction constant. Heat conduction in graphite and graphene is achieved by both phonons and electrons but the contribution of electrons is very little because of the strong sp^2 bonds of carbon atoms [27]. Therefore, graphene sheet resistance (R_s) is approximately proportional to the number of scattered phonons (n_0): $R_s \propto n_0$ and $n_0 = \frac{1}{e^{\hbar w/K_B T}-1}$, where $\hbar w$ is the phonon energy, K_B is the Boltzmann constant, and T is the temperature [23]. Acoustic phonons have small energy ($\hbar w<K_B T$) so the number of scattered phonons can be approximated as: $n_0 = \frac{1}{e^{\hbar w/K_B T}-1} \approx \frac{K_B T}{\hbar w}$ and then $R_s \propto T$. Whereas for optical phonons, $\hbar w \approx K_B T$ which leads to $n_0 = \frac{1}{e^{\hbar w/K_B T}-1}$ and then $R_s \propto \frac{1}{e^{\hbar w/K_B T}-1}$. If graphene is deposited on a SiO_2 substrate, scattered phonons would be the combination of graphene phonons and SiO_2 phonons. In case of suspended graphene, the scattered phonons will be contributed only by graphene. However, the suspended graphene is not preferable in our study since it has little surface disorder, which makes it less sensitive to temperature [28-30]. For this reason, this work uses a planar hot wire configuration as the building block of the graphene sensors.

Theoretically, when a hot wire is heated by an electrical current, the thermal energy generated by the wire is equivalent to the energy loss due to convective heat transfer at thermal equilibrium, $I^2 R_w = A_w (T_w - T_f) h$, where A_w denotes the surface area of the wire, T_w and T_f are the wire and fluid temperatures respectively, h is the heat transfer coefficient, and $I^2 R_w$ resembles the thermal energy stored in the wire plus the heat transfer from the surrounding. The resistance of the hot wire (R_w) depends on the wire temperature (T_w). At steady state, this resistance can be expressed using a linear approximation of the wire temperature [31],

$R_w = R_{ref}[1+\alpha\,(T_w - T_f)]$, Where R_{ref} is the baseline wire resistance and α is the temperature coefficient of resistance (TCR). In addition, heat transfer coefficient (h) can be expressed as a function of fluid velocity (V_f) according to the King's Law: $h=a+bV_f^c$, where a, b and c are constants obtained from experimental calibrations. By combining the equations above, one could get the relation between the fluidic flow velocity and the temperature gradient of the hot wire: $V_f = \{[\frac{I^2 R_{ref}\ [1+\alpha(T_w - T_{ref})]}{A_w\,(T_w - T_f)} - a]/b\}^{1/c}$.

6.3.3 Fabrication method

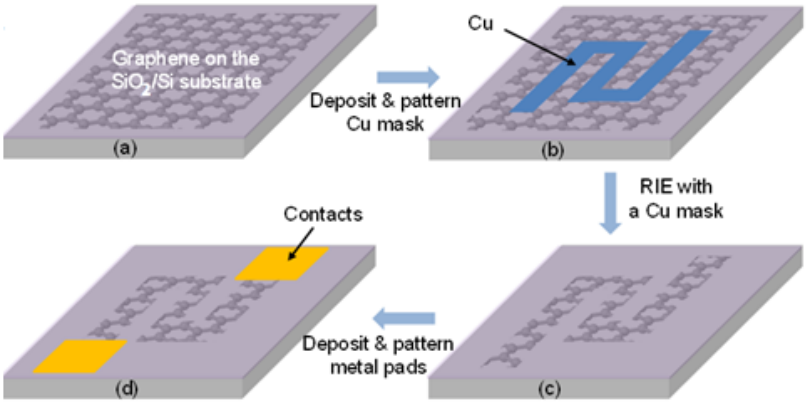


Figure 6.10 A typical process flow for making the proposed graphene hot-wire sensors.

The fabrication process of the proposed graphene hot wires used conventional micro/nanofabrication techniques, as depicted in Figure 6.10. Graphene thin films were prepared using a micromechanical exfoliation technique from highly oriented pyrolytic graphite (HOPG) flakes and then were transferred onto a 300 nm SiO_2/Si substrate. A micro Raman spectroscope was used to determine the number of layers of graphene sheet. The mechanical exfoliated bi- and few-layer graphene films were patterned through electronic-beam lithography (EBL) and then an 80 nm copper layer was deposited and patterned as a mask for graphene etching. The graphene sheet area that was not protected by the copper mask was etched in oxygen plasma for 40 s with 150 W radio-frequency (RF) power, 516 mT

pressure, and 10sccm flow rate. To dissolve the copper mask, the chip was immersed in a ferric chloride solution for one minute. After that, conductive electrodes were fabricated on the two terminals of the graphene wire through EBL, thermal evaporation of Ti (5 nm)/Au (75 nm), and then metal lift-off processes. Finally, the device was annealed in an H_2/Ar environment at 400 °C in order to improve electrode contact resistance and remove fabrication residues. Figure 6.11 shows the SEM images of as-fabricated bi- and few- layer graphene hot wires. The bilayer graphene wire had a length of ~ 53 μm and the average width of ~ 0.5 μm. For the few-layer device, the length was about 50 μm and the average width was about 10 μm.

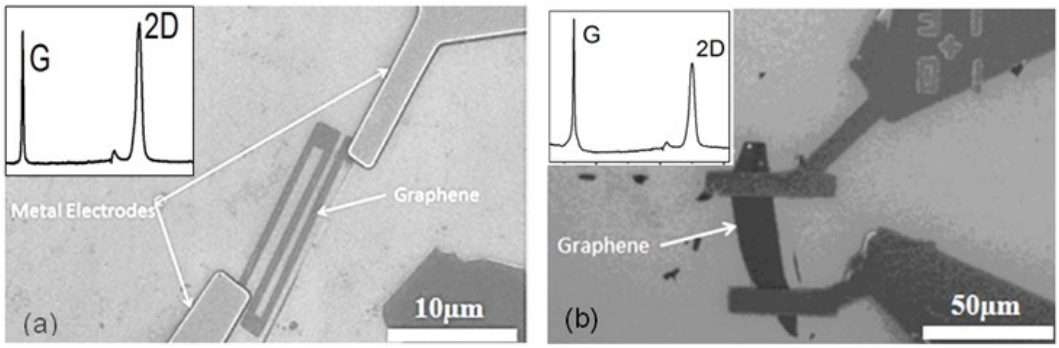


Figure 6.11 SEM images of the fabricated bilayer (a) and few-layer(b) graphene hot-wire sensors. The insets show the Raman spectra obtained from the bilayer and few-layer graphene areas.

6.3.4 Results and discussions

To measure the flow sensitivity of the devices, the graphene hot-wires were placed in a dual in-line package (DIP) socket and covered by a glass lid with capillaries (350 μm in outer diameter) as upstream and downstream flow interconnections (Figure 6.12 (a)). The gas chamber was sealed with epoxy to minimize side leakage. During the measurement, the temperature of the package was maintained at a constant temperature (70 °C) whereas the temperature of nitrogen (N_2) inflow was at room temperature (RT). Prior to flow testing, to

determine the proper placement of the graphene sensors, the temperature profile inside the package was simulated with COMSOL Multiphysics 4.3 at different inlet flow rates. As shown in Figure 6.12 (b), the temperature varied from RT to 70 °C within a narrow distance close to the inlet capillary, due to the cooling effect of N_2 inflow. The simulation result suggests that the sensor should be placed in a particular distance and orientation from the inlet in order to generate detectable response. For example, for a flow rate of 0.01 L/min, the sensor should be localized at less than 2 mm from the inlet capillary tube.

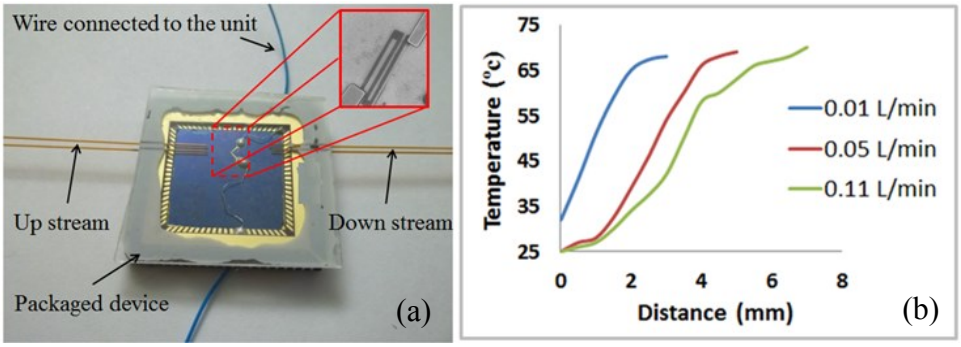


Figure 6.12 (a) Device sealed in a DIP carrier with capillaries as upstream and downstream connections. (b) COMSOL simulation shows temperature profile of the packagevs. distance from the inlet at different input flowrates.

The flow sensing responses of the as-fabricated devices was studied by monitoring the current and resistance changes of the graphene hot wires as the N_2 flow was introduced into the test chamber. Figure 6.13 shows the transient response of current of a representative bilayer graphene wire at various N_2 flow rates and also N_2 input pressures. When the gas flowed through the device, the current decreased rapidly with a significant undershoot and then stayed constant with little variations. The steady-state current decreased as the flow rate increased. The current undershoot could be attributed to the sudden rise of the graphene resistance, which was caused by the temperature drop on the graphene surface, due to the cooling effect of the N_2 flow. As the current continuously passed through the device, the

temperature of the graphene wire increased due to current-induced Joule heating, thereby, reducing the wire resistance until the equlibruim point was reached for a particular flow rate.

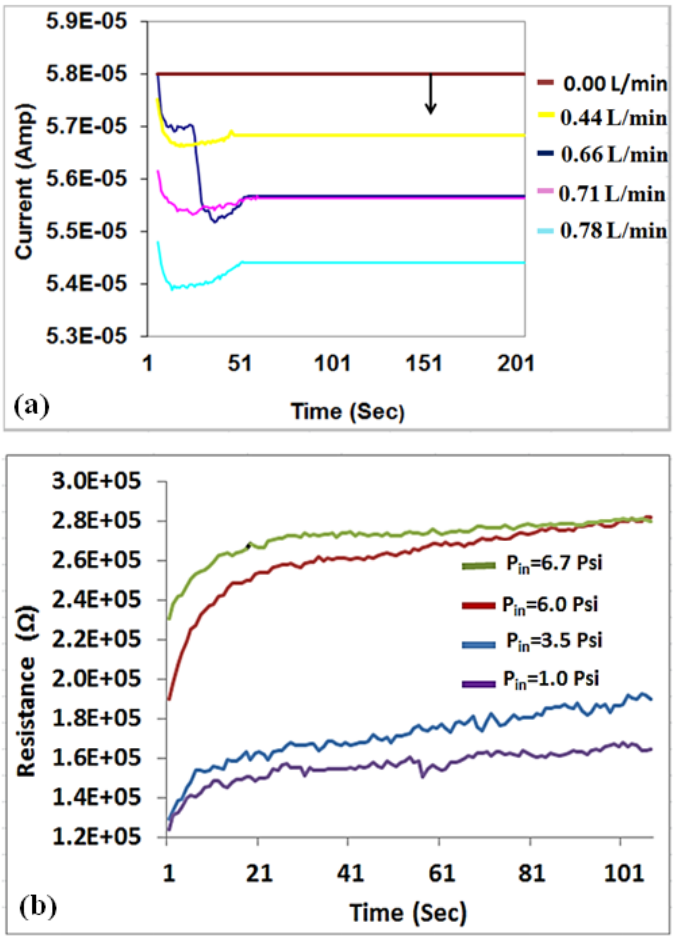


Figure 6.13 Transient current responses of a bilayer sensor with (a) different N_2 flow rates and (b) different N_2 input pressures.

Similar testing was performed for the few-layer graphene sensors. Figure 6.14 (a) and (b) summarize the normalized resistance variations of the bi- and few-layer devices as functions of the N_2 flow rate. In particular, the flow sensing resolutions of around 0.07 L/min and 0.1 L/min were obtained from the bilayer and few-layer graphene hot wires, respectively. Moreover, the negative TCRs of the bi- and few-layer graphene films were determined based

on a linear approximation method, resulting in the TCR ranges of -0.00619 K^{-1} to -0.008 K^{-1} for the bilayer graphene and -0.0014 K^{-1} to -0.00175 K^{-1} for the few-layer graphene.

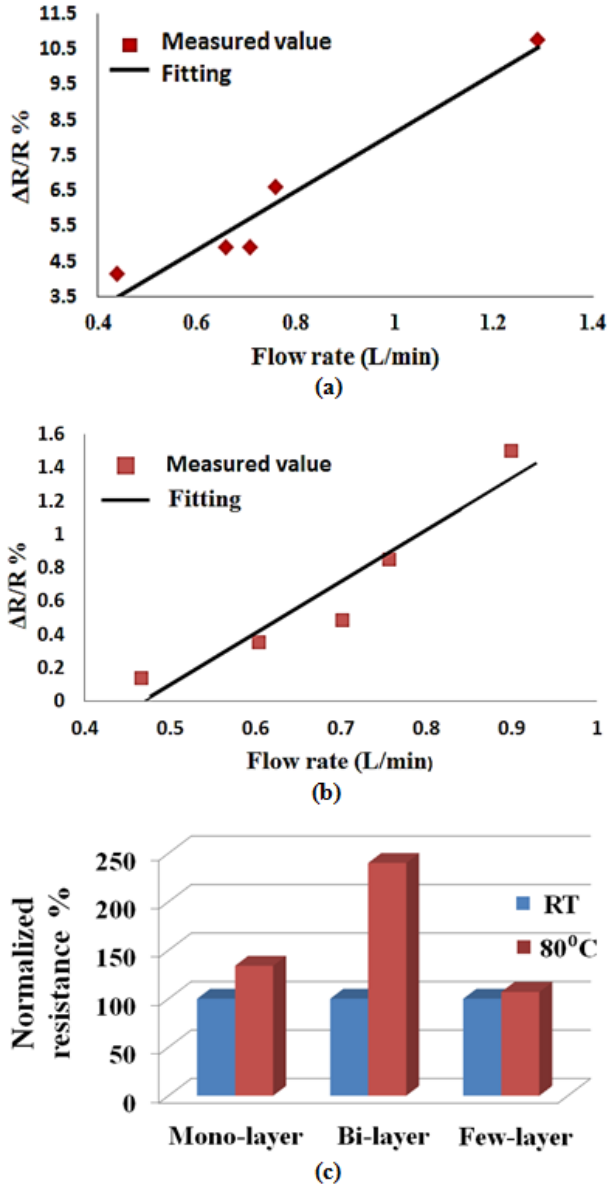


Figure 6.14 Normalized resistance changes at different flow rates for (a) a bilayer graphene hot wire and (b) a few-layer sensor. (c) Comparison between the normalized resistances of the mono-, bi- and few-layer graphene devices, measured as temperature changed between RT and 80 °C.

From the histogram of Figure 6.14 (c), compared to the mono- and few-layer graphene, the bilayer graphene has the highest negative TCR, measured as the temperature changed between RT and 80 °C, which is favorable to temperature sensing applications. Consequently, the bilayer device is expected to have a higher current capacity and a higher sensitivity than those of the mono- and few-layer ones.

Time responses to temperature variation for the packaged devices were also measured. During the experiment, each device was heated from RT to 70 °C and the corresponding current change was monitored and plotted as a function of time. From the experimental data, it can be found that the device response was faster with a greater applied voltage. For example, for the bilayer device, the time constant (the time frame when the current reached 63.2% of the steady-state value) was decreased by 18% as the applied voltage increased from 0.5 V to 3 V, whereas for the few-layer the time constant decreased by 40% as the applied voltage increased from 0.1 V to 1 V. The temperature sensitivity of the bilayer device was about 5 times greater than that of the few-layer device, with the applied voltages of 3 V and 0.3 V (Figure 6.15 (a) and (b)) for the bi- and few-layer devices, respectively. Figure 6.15 (c) shows the time response of the bilayer device during a heating-cooling cycle from RT to 70 °C and then 70 °C to RT. The time constant of the cooling (T_1) step was slightly smaller than the time constant of the heating (T_2) step because the heat source was a hot plate operated in an open environment. The other remarkable thing was that the settling levels of the currents of all the samples were around 10% to 20% lower at 70 °C than the currents at RT. This can be attributed to the variation of the metal-graphene contact resistance with temperature.

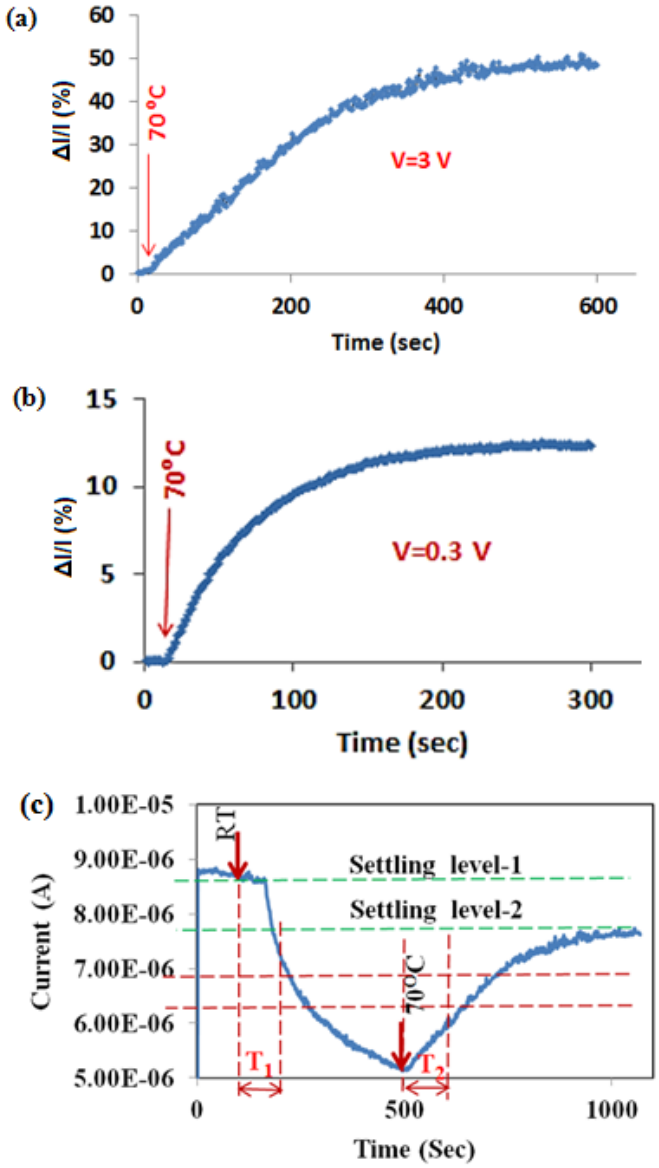


Figure 6.15 Transient responses of different graphene devices as the environmental temperature varied from RT to 70 °C: (a) the response of a bilayer graphene sensor, (b) the response of a few-layer graphene sensor, (c) the response of the bilayer device when temperature increased from 70 °C to RT then increased to 70 °C.

Although an increased voltage can enhance the time response of temperature sensing, the applied voltage was governed by the resistance of the as-fabricated graphene. This indicates that the device with a lower resistance has a lower allowable applied voltage, since a high voltage would damage a device by Joule heating. Therefore, we studied thecurrent-induced self-heating effect in the bilayer graphene sensor by applying a known voltage across the

graphene hot wire and measuring the resulting current change of the device with time. The self-heating can result in the temperature increase of the graphene and lead to the current increase due to the NTC of the bilayer graphene. shows the current variation with time due to self heating. For the sample 1 (Figure 6.16 (a)), with the applied voltage of 3 V, the currrent was increased by ~ 20% after ~ 55 seconds. The sample 2 (Figure 6.16 (b)) was supplied by 3 V and the corresponding current was increased from from 0.0072 A to 0.0092 A within 1000 sec. The sample 3 was burned due to Joule heating, after applying the 2.5 V input voltage for 2000 sec (Figure 6.16(c)). Since the self heating effect can cause imprecise temperature measurement and even device damage, the applied voltage should be selected properly during the sensing applications.

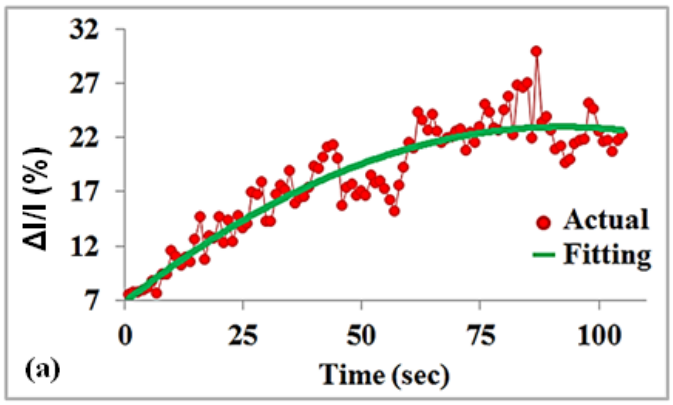
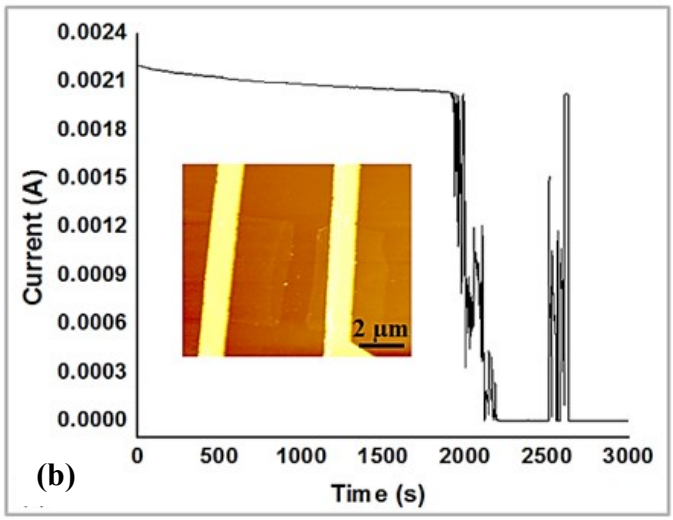
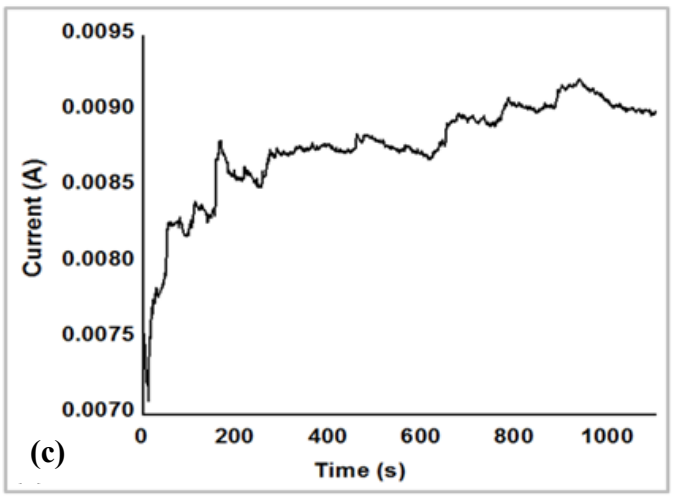


Figure 6.16 (a) Sample 1, Self-heating effects of bilayer graphene device with an applied voltage of 3V. (b) Sample 2 was damaged by Joul heating after applying 3 V for ~ 2000 sec. The inset is an AFM image of a failed device due to Joul heating. (c) Sample 3, current variation with supplied voltage of 3.5 V

Figure 6.16 (cont'd)





Based on the experimental results, the heat capacity of the device can be extrapolated using $C = \frac{IV}{\Delta T} \times \tau$, where V is the applied voltage, I is the sensor current, τ is the time constant obtained from the graph, and ΔT is the temperature gradient due to power of Joule heating ($P=I\times V$). Since we had two heat sources, Joule heat and a hot plate, it is important to measure the equivalent power of heating at 70 °C. To do this, we first measured the graphene resistance at 70 °C using the hot plate as the heat source. Then we replaced the hot plate heat with Joule heat and increased the supply voltage of the graphene wire until the same

resistance was obtained. The corresponding current (I) and voltage (V) were recorded and the equivalent power ($P=IV$) was calculated to determine the heat capacity of the overall system that contained the graphene hotwire, the SiO_2 substrate, and the microfluidic carrier by the above expression. The thermal capacity was ~7.35 μWs/°C for a bilayer graphene device with an overall area of 53 × 0.5 μm^2 at 2.42 V, which was the highest compare to the mono- and bi-layer devices.

Since the thermal capacity is one of the significant factors affecting the response time of the device, an alternative sensor package with a low thermal capacity and a low thermal mass will be needed to speed up the sensor response. For the flow/temperature sensing applications using graphene, device design can be tailored to obtain desired sensitivity and time response, by optimizing the dimensions of graphene wire (length and width), the number of graphene layers, supply voltage, and packaging technique.

6.3 Conclusion

This chapter has discussed the concept, fabrication, and characterization of graphene-based nanoscale sensors for chemical molecule, temperature, and flow detection. Chemical sensing of the inter-sheet graphene sensors has been studied, demonstrating that the inter-layer configuration enables higher sensitivities compared to the most commonly used intra-layer configuration. There is a high likelihood that this sensitivity improvement can be attributed to the variance of the tunneling current through the stacked graphene sheets due to the adsorption of vapor molecules, either mechanically by surface-tension-induced distortion or electronically by inter-sheet electron donation.

In addition, the surface heat convection properties of the bi- and few-layer graphene wires were studied and applied in the development of the flow and temperature sensors. The

graphene hot wires were fabricated with specific dimensions to achieve high resistances and uniform temperature distribution. The flow sensing resolutions of approximately 0.07 L/min and 0.1 L/min were achieved from the bi- and few-layer graphene hot wires, respectively. The bilayer graphene sensor exhibited greater sensitivity than the few-layer one because of the larger NTC of the bilayer graphene. Furthermore, the time response of the current through the graphene hot wires was studied, showing that the time constant decreased as the resistance of the hot wire decreased, due to the reduced Joule heat.

Future research efforts are necessary to produce large-scale graphene films with the desired number of layers and high quality. It is expected that, with the development of advanced surface functionalization and nano-processing technologies, graphene sensors will become more attractive for applications in the detection of various stimuli, such as chemical/biological molecules, force/displacement, pressure, and surface tension.

APPENDICES

APPENDIX A : Fabrication Recipes

A.1 Markers Fabrication

1- Prepare a substrate of 300 nm SiO_2 /Si (purchased from WRS Materials).

2- Spin on S1813 photo resist at 4000 rpm for 50 sec.

3- Bake at 110 °C for 1 min on hot plate.

4- Align and expose for 9 sec using ABM mask aligner (Figure A.1(a))

5- Develop in MF325 for 30 sec.

6- Rinse for 30 sec in DI water and then dry by N_2.

7- Check under optical microscope that development was successful.

8- Place the sample in Edward Auto-306 thermal evaporator with Ti and Au sources (Figure A.1 (b)).

9- Deposit 5 nm of Ti layer at a rate of ~0.02 nm/s.

10- Deposit 70 nm of Au layer at a rate of ~0.2 nm/s.

11- Remove the sample from the thermal evaporator and place in acetone for 24 h for liftoff.

12- Rinse in IPA, DI water and then dry by N_2.

13- Etch the photo resist residues by PX-250 O_2 plasma, Figure A.1 (c) (300 W, 22 sccm for 1 min).

Figure A.1 Microfabrication instruments (a) ABM Mask aligner (b) Auto 306 Thermal evaporator (c) PX-250 Plasma Etcher.

A.2 Mechanical Exfoliation of Graphite

1- Place graphite flake onto adhesive tape.

2- Fold the tape next to the flake and then slowly pull apart in order to smoothly cleave graphite.

3- Repeat steps 2 for around 10 times.

4- Gently place adhesive tape with cleaved graphite onto substrate.

5- Press out any air for 2 min using the handle of a pair of tweezers.

6- Very slowly peel off the tape.

Figure A.2 shows the exfoliation process.

Figure A.2 Micromechanical exfoliation of graphite.

A.3 Residue Cleaning Process

1- Insert the samples into a tube furnace (). Flow argon (97%) and hydrogen gases (3%) at 2000 sccm for 5 min to remove O_2 from the glass tube.

2- Heat up the furnace to ~400 °C under H_2/Ar flow for 1 hr.

Figure A.3 shows the annealing setup.

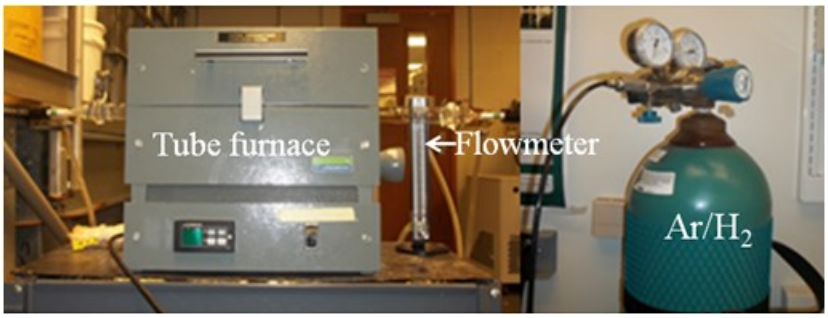


Figure A.3 Annealing setup

A.4 Metal Electrodes Deposition

1- Design electrodes using CAD.

2- Spin on MMA-EL9 at 4000 rpm for 50 s.

3- Bake at 180 °C for 90 sec on hot plate and then place on cooling block for 2 min.

4- Spin on PMMA-C2 at 4000 rpm for 50 sec.

5- Bake at 180 °C on hot plate for 90 sec.

6- Use JEOL 840A Electron Beam Lithography instrument (Figure A.4) to pattern electrodes (acceleration voltage=35 KV, dose=280 μC/cm^2 and beam current =30 PA).

7- Develop MMA/PMMA for 20 s in 1:3 methyl-isobutyl-ketones (MIBK) to isopropanol.

8- Rinse for 20 s in IPA and then N_2 dry.

9- Check under optical microscope that development was successful. Repeat steps 6 and 7 if under-developed.

10- Deposit 5 nm of Ti as a sticking layer at a rate of ~0.2 Å/s.

11- Deposit 70 nm of Au at a rate of ~2 Å/s.

12- Remove sample from thermal evaporator and place in acetone for 24 h for liftoff.

13- Rinse in IPA, DI water and then dry by N_2.

Figure A4. Shows photo images of the e-beam lithography instrument instrument.

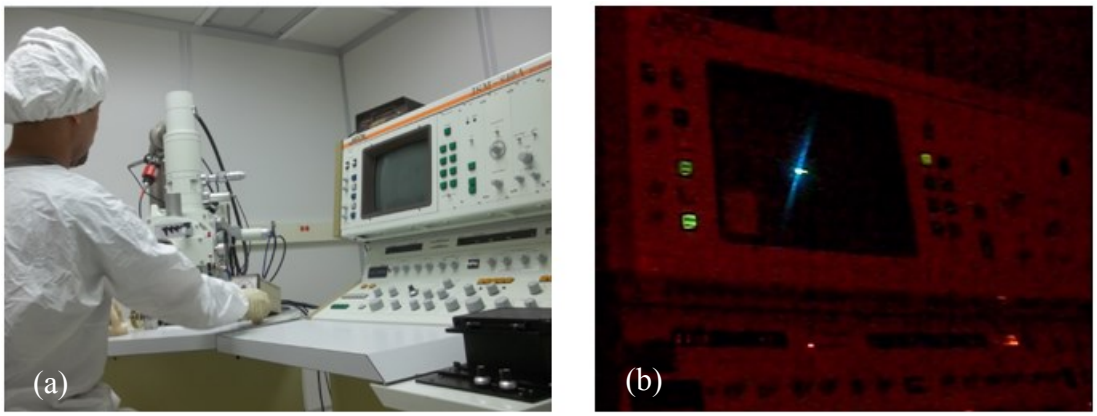


Figure A.4 JEOL 840A Electron Beam Lithography instrument (a) Sample loading (b) instrument during writing.

A.5 Graphene Patterning and Etching

1- Pattern e-beam resist by electronic-beam lithography (EBL) as in A.4 step 1-9.

2- Deposit 80 nm of copper layer as a mask for graphene etching.

3- Use O_2 plasma for 40 s with a power of 150 W and 10 sccm to etch the unprotected part of graphene sheet.

4- Dissolve the copper mask by immersing the chip in a Ferric Fluoride ($FeCl_3$) for 1 min.

5- Fabricate metal electrodes on the two terminals of the graphene sheet through EBL (step 1) then deposit Ti (5 nm)/Au (75 nm) layers.

6- Place the samples in acetone for 24 h for metal liftoff process.

7- Anneal in an Ar/H_2 environment at 400 °C in order to remove fabrication residues.

A.6 Graphene Surface Recovering after Plasma Etching

The amount of defects that usually produce due to plasma etching can be reduced significantly with a post-etch annealing treatment, as in the following steps:

1- Insert the samples into a tube furnace.

2- Flow argon gas into a tube furnace at 2500 sccm for 100 min to dismiss O_2 from the furnace to avoid graphene burning at high temperature.

3- Heat up the furnace to 900-1000 °C for 1 hr.

A.7 Graphene Nanomesh FET Fabrication Process

1- Prepare the 300 nm SiO_2/Si substrate.

2- Transfer graphene using micromechanical exfoliation.

3- Deposit metal electrodes (as in A.4).

4- Spin on a MMA/PMMA (as in A.4, steps 2-5).

5- Use EBL (alignment file only), to introduce nano holes, with the following recipe: beam current=40 PA, center to center distance=50 nm, spacing 500 nm, and magnification=×400, acceleration voltage=35 KV and the number of scans=1.

6- Develop (as in A4 steps 7-8).

7- Etch O_2 plasma to etch unprotected part of graphene to generate nanomesh.

8- Rinse by acetone, IPA and DI water and then dry with N_2.

9- Check graphene nanomesh under Hitachi S-4700 SEM (Figure A.5).

Figure A.5 Hitashi S-4700 SEM. The SEM screen shows a GNR sample.

A.8 Solving the CVD/Substrate Adhesion Problem:

After deposition PMMA (without baking), just leave it for 24 h to dry and then:

1- Dissolve cu in $FeCl_3$ salt.

2- Transfer graphene/PMMA to a beaker of DI water for 5 min.

3- Transfer to another beaker of water for another 5 min.

4- Transfer graphene/PMMA to RCA1 (1:1:20) NH_4OH, H_2O_2, H_2O for 10 to 15 min.

5- Transfer to RCA2 (1:1:20) HCL, H_2O_2, H_2O for 10 to 15 min.

6- Transfer to a beaker of DI water.

7- Before transfer to substrate, treat it by O_2 plasma 150W, 22 sccm for 3 min.

8- Transfer graphene/PMMA to a substrate.

9- Leave it in ambient to dry.

10- Bake at 150 ^{o}C for 10 to 15 min.

11- Dissolve PMMA by acetone.

12- Rinse by IPA and dry by N_2. Then Bake at 180-200 $^{\circ}$C in vacuum for 30min.

APPENDIX B: Testing

B.1 Testing methods

B.1.1 In air

REL-4100A probe-station which is connected to semiconductor parameter analyzer was used for testing in air (Figure B.1).

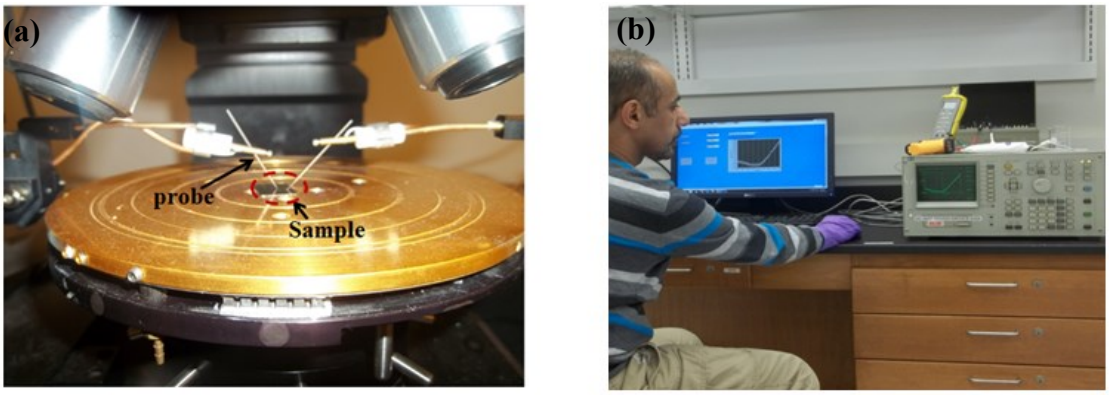


Figure B.1 Testing in air (a) REL-4100A probe station. (b) HP-4145semiconductor parameter analyser

B.1.2 Testing in inert enviroment

We have used Ar and Hellium enviroment in testing. A feed though testing setup (Figure B.2) was designed and them made in the MSU chemistry scientific glass shop. The set up made of Borosilicate-7740 with electrodes were made of three parts copper, tingistin and nichel matels. The tingistin part was sealed to glass.

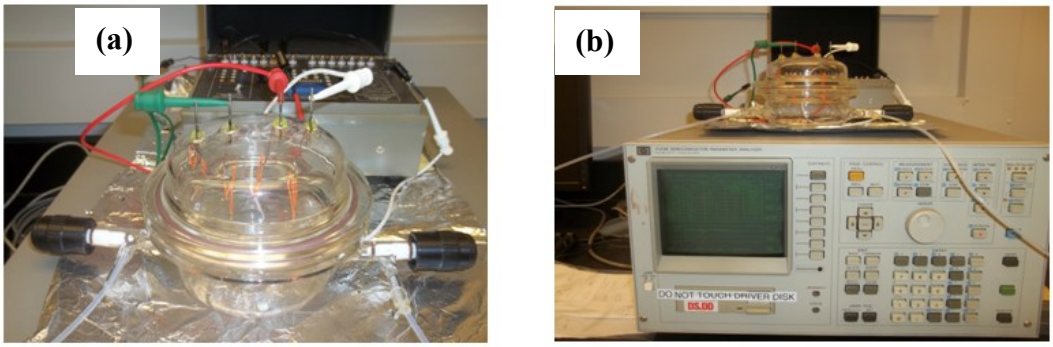


Figure B.2 Testing in an inert gas (a) feed through testing setup (b) set up connected to semiconductor parameter analyser.

B.1.3 Testing in vacuum

Feed through tool connected to EVO LS-25 SEM was used for vacuum testing. A plastic chip-holder with aluminum probes was designed and constructed in a CNC machine shop (Figure B.3).

Figure B.3 Feed-though for SEM (SEM EVO LS-25)

B.2 Testing Instruments

B.2.1 Atomic Force Microscope (Figure B.4)

Dimension 3100 SPM atomic force microscope. Taping made was used to avoid damaging graphene sheet. The system has the following specifications:

- Noise Level: < 0.5Å RMS in vertical (Z) direction

- X-Y imaging area approx. 90 µm × 90 µm
- Z range approx. 6 µm
- Lateral accuracy typically within 1%, maximum 2%
- Provides full 16-bit resolution on all axes for all scan sizes and offsets.

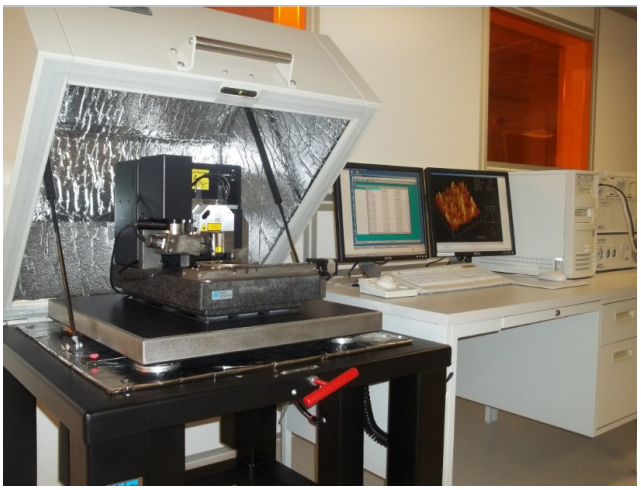


Figure B.4 Dimension 3100 SPM Atomic Force Microscope.

B.2.2 Raman Spectroscope (Figure B.5)

HoloProbe Raman Spectrograph coupled to an Olympus BX-60 optical microscope. The System has the following specifications:

- Excitation wavelengths: 532 nm
- Laser spot size: ~5-10 µm (with an 100× objective)
- Spectral resolution: 5 cm^{-1} (1 cm^{-1} with High-Resolution grating)
- Spectral coverage: ~250 - 4000 cm^{-1} Raman shift

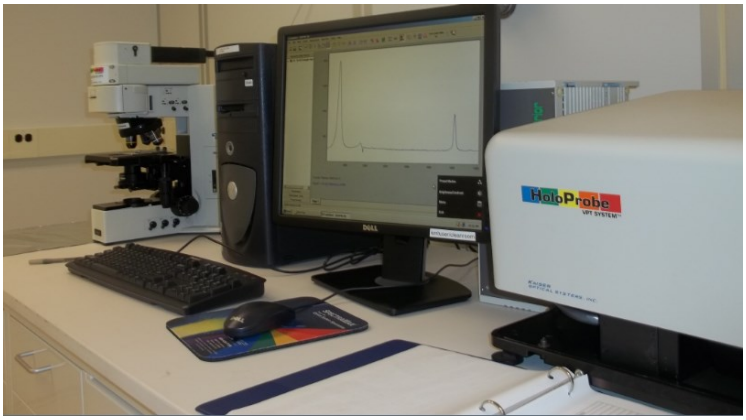


Figure B.5 HoloProbe Raman Spectrograph coupled to an Olympus BX-60 optical microscope

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