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CMOS SWITCHED-CURRENT DATA CONVERTERS

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DESIGN OF HIGH PERFORMANCE AND LOW POWER CMOS SWITCHED-CURRENT DATA CONVERTERS

By

Jin-Sheng Wang

A DISSERTATION

Submitted to
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ABSTRACT

DESIGN OF HIGH PERFORMANCE AND LOW POWER CMOS SWITCHED-CURRENT DATA CONVERTERS

By

Jin-Sheng Wang

The advent of portable communication and computing service has stirred a great deal of interests in both commercial and research areas. The circuit technology used in portable equipment has been changed from the conventional analog circuit technology to mixed-signal circuit technology. Low power and high performance are strongly needed for both analog and digital circuits to increase operation time of the portable equipment. The design of low power and high performance mixed-signal CMOS IC's is hindered by processing techniques that are optimized for digital applications. Moreover, scaling/reliability consideration are driving CMOS process towards submicrometer feature size and lower power supply voltages.

Switched-current (SI) technique has received considerable attention as an alternative for analog data acquisition and conversion circuit design. However, existing SI circuits cannot make the theoretically expected performance due in part to the use of non-optimal current copiers, its basic building blocks. Based on our development of design methodologies and synthesis process for optimally generating low power and high performance CMOS current copiers, SI technique becomes feasible.

This thesis develops high performance and low power CMOS SI data converters, ADCs (analog-to-digital converters) and DACs (digital-to-analog) converters. A 12-bit

CMOS cyclic ADC circuit which consumes 1.9mW in power and takes 2.13 mm^2 in chip area, has designed and fabricated. A 11-bit CMOS DAC circuit which consumes 4.4mW in power and achieves 100 MSamples per second in conversion rate, has been designed and simulated, where 3.3 V power supply voltage and *MOSIS SCN20* 2 μm CMOS process with 2-level transistor parameters are employed. This thesis also presents the design methodologies and performance analysis process. The developed design methodologies guide the designers to properly select the transistor sizes and capacitances based on a given set of design specifications including input dynamic range, full-scale current, SNR, power consumption, etc., and the performance analysis process estimates the calibration time, holding time, and accuracy of the data converter circuits.

This study also develops a built-in tester to enhance the testability of SI circuits, The tester possesses the features of autozeroing and self-testability. The autozeroing property increases the accuracy, while the self-testability ensures the correctness of the tester before it is used to test SI circuits.

With the successful development in this thesis study, we believe that SI technique will soon become an alternative industrial standard for designing analog components in mixed-signal circuits for low-voltage/low-power signal processing applications.

To my parents, wife, daughter and brothers

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Chapter 1

INTRODUCTION

High speed and low power data converters, analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), have been highly demanded in portable systems, such as personal communication systems, astronomy research equipments, and multimedia. The analog circuit technology conventionally employed for such applications has been gradually switched to analog/digital mixed-signal circuits technology [1]. Integrating both digital and analog on a single chip has improved performance and reduced board size and cost. Figure 1.1 shows the schematic diagram of a typical DSP (digital signal processing)-based mixed-signal IC. The current trend shows that data converters' interfaces are incorporated as a cell in a complex mixed-signal IC containing mostly digital blocks for DSP and control. Even though very complicated DSP circuits have been widely used, analog circuits will remain for processing or interfacing analog signals to/from I/O devices.

The silicon area in a typical mixed-signal integrated circuit (IC) contains 10% analog circuits and 90% digital circuits. The overall system cost can be reduced significantly if both analog and digital portions can use the same supply-voltage and the analog portions can be fabricated using the low cost digital CMOS process. If both analog and digital portions use the same supply-voltage, then the system does not need dc-dc converters to generate multiple supply voltages.

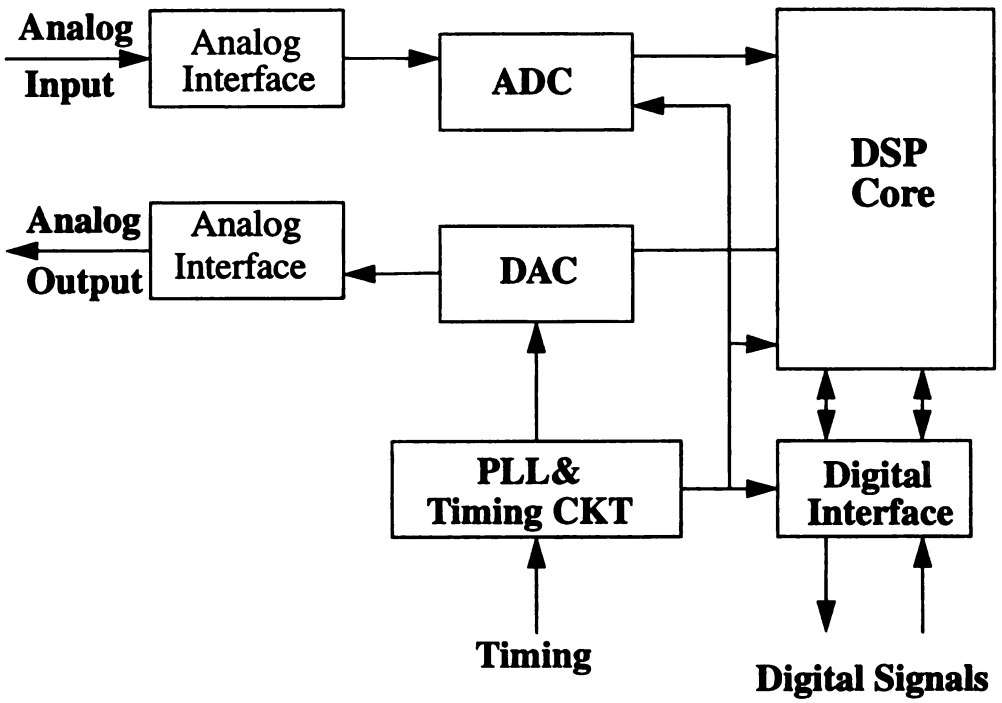


Figure 1.1 Schematic diagram of a typical DSP-based mixed-signal IC.

Since most of analog components in a mixed-signal ICs are used for processing and interfacing analog signals, their accessibility becomes drastically reduced [2,3]. Recently, manufacturers have found the costs associated with high-volume production of mixed-signal ICs are strongly affected by the cost of testing. Testing effort is just the opposite of the silicon areas in mixed analog and digital circuits; i.e., 90% for analog testing and 10% for digital testing. Therefore, enhancing testability can reduce test cost and thus further decrease system cost.

1.1 Switched-Current Circuits

Traditionally, the analog interface portion of a mixed-signal circuit employs the switched-capacitor (SC) technique which requires high quality linear capacitors [4]. The high quality linear capacitors are usually implemented using two layers of polysilicon. However, the second layer of polysilicon used by SCs is not needed by purely digital circuits and may become unavailable as process dimensions shrink to the deep submicron range. On the other hand, to be compatible with low-voltage systems, analog circuits must be operated at a supply voltage of 2 V or below. However, with lower supply voltages the realization of high-speed, high-gain operation amplifiers in the SC technique becomes more difficult [5,6].

Recently, a class of analog circuits wherein current, rather than voltage, is the primary signal medium has received considerable attention. The use of current-mode creates a potential for speed improvement because stray-inductance effects in such low-impedance switched-current (SI) circuits are much less severe than those in high-impedance SC circuits [5-18]. High accuracy can be obtained by using dynamic calibration to alleviate

the error due to element mismatch. The SI technique couples itself well with the down-scaled CMOS technology, where the transistors with a high cut-off frequency are available, leading to a higher calibration. In addition, highly linear capacitance is not needed for high accuracy analog signal processing. Alternatively, accuracy has been traded with speed in Σ–Δ modulations using oversampling techniques to achieve performance several orders of magnitude higher than traditionally associated with analog limitations [9]. The challenge and the gains are clear for the designer who can manage the extra demands on analog performance with diminishing resource of digitally-motivated VLSI process development [18].

Even though the SI technique possesses the salient features mentioned above, one frequently asked question is: why hasn't the SI technique become an industrial standard yet? A simple answer is that the accuracy, linearity, and noise problems are still not resolved completely and satisfactorily [18]. It is necessary to develop sound design methodology and synthesis processes for generating high performance analog circuits [18]. Since current copier is the basic building block of SI circuits, the performance of a SI circuit is determined by the performance of the current copiers it employs. Therefore, developing a sound design methodology and synthesis process for generating high performance current copiers becomes a very important task.

1.2 Objectives and Research Tasks

Based on the recently developed current copiers [5-7,14], our research goal is to develop high performance CMOS SI circuits for low-power/low-voltage signal applica-

tions and the objective of this thesis study is to develop high performance and low power CMOS SI data converters.

In the past years, a number of high-speed ADC and DAC circuits have been designed for portable systems [19-46]. For such applications, a sample rate above 5 MS/s (Mega Samples per second) and 8-12 bit resolutions is required. Most of such converter designs use the switched-capacitor (SC) technique. The power consumption is typically ranged from 100 mW to 500 mW. Apparently, for battery-powered portable applications, this level of power consumption is not suitable. Therefore, power reduction is essential for power-optimized ADC and DAC circuits.

To accomplish our research objective, the research tasks include the development of design methodologies and performance analysis processes for the optimized data converters. The design methodologies provide the designers to select appropriate structures and parameter values to meet the design specifications such as accuracy, speed, power consumption, signal-to-noise ratio (SNR), supply voltage, and etc., while the performance analysis processes allow the designers to evaluate the performance of the designed circuits. In this study, the developed data converter circuits will be designed and fabricated using the low-cost digital CMOS process and the same low supply voltage for both digital and analog parts. In addition, the developed data converters must be easily testable.

1.3 Thesis Organization

The thesis is organized as follows: Chapter 2 reviews the background which relates to this research. The basic current copier is introduced first. Several different structures and circuit cells are also presented to endorse the feasibility of SI technique. Two current-

mode ADC circuits in [8,16] and a current-mode DAC in [47] are discussed. Finally, the test generation and fault coverage of SI CMOS ADC developed in [48-52] are briefly described.

Chapter 3 describes the design and operation of the developed high performance and low power cyclic ADC circuit using modified redundant-signed-digit (RSD) algorithm. A 12-bit CMOS SI circuit has been designed, simulated, and fabricated. Both simulation results and measurements will be discussed.

Chapter 4 presents the design and operation of the developed DAC circuits. The weighted current references are generated using current reference generator (CRG) circuits. Two types of CRG circuits are introduced with their simulation results. The design methodology and performance analysis of DAC circuits for low power applications are also presented.

Chapter 5 introduces a built-in tester to enhance the testability of SI circuits. The tester is comprised of a current comparator, a voltage window comparator, and a digital latch. The current comparator is required to have high-accuracy, low-power consumption, simple structure with small chip area, and moderate speed. A comparator adopting an autozeroing technique is developed to achieve high accuracy, and it possesses the self-testing capability for detecting both catastrophic and parametric faults of all its components.

Finally, Chapter 6 summarizes the thesis study and gives concluding remarks and future research directions.

Chapter 2

BACKGROUND

This chapter reviews the background knowledges related to the thesis research. Current copier is the basic building block of SI circuits. Section 2.1 reviews the existing current copiers. Section 2.2 introduces the current-mode multiplier and divider circuits. Section 2.3 presents the design and operation of data converter circuits. Finally, test generation of both current copiers and ADCs are discussed in Section 2.4.

2.1 CMOS Current Copiers

A simple current copier, as shown in Figure 2.1(a) [7], is comprised of two switches S_1 and S_2, a current-storage transistor M_1, and a holding capacitor C_1. To copy the current I_{in}, S_1 and S_2 are turned on, therefore feeding I_{in} to M_1 and C_1. The capacitor charges up to whatever gate voltage is needed by M_1 to support a current equal to I_{in}. When S_1 and S_2 are off, the copier cell is disconnected from the current source. Thereafter, the copier cell is capable of sinking a current I_{in} when connected to a load. No well-matched components are needed in the current copier. However, the copier is suffered from two major error effects due to (1) the nonzero conductance of M_1 and (2) charge-feedthrough of S_2 [7]. The non-zero output conductance results from the channel length-modulation effect and the drain-gate capacitive coupling of M_1. The charge-feedthrough

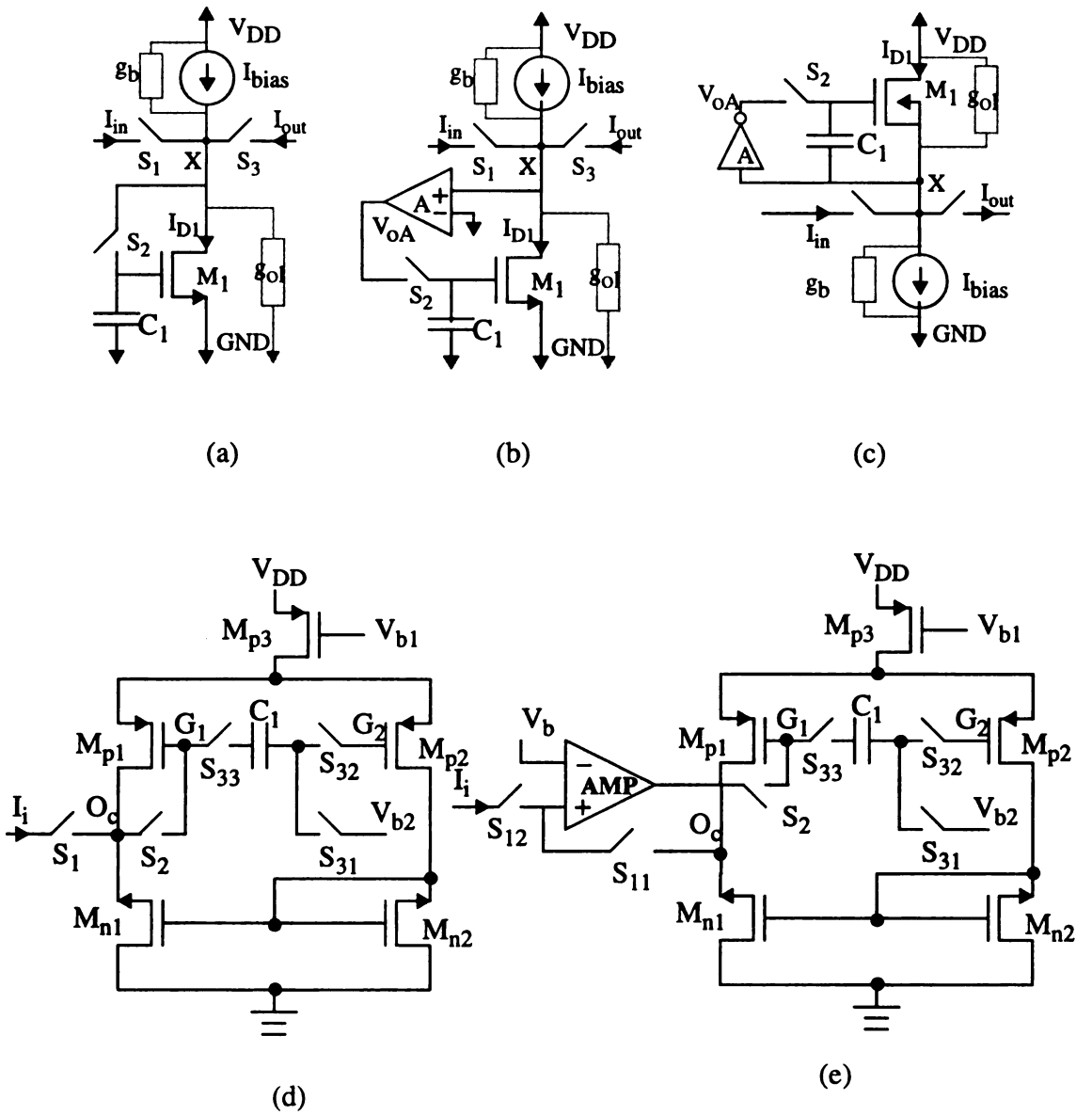


Figure 2.1 Various current copier structures: (a) simple copier; (b) negative feedback (inverter) structure; (c) negative feedback (follower) structure; (d) differential-pair; and (e) differential-pair with feedback amplifier.

error is caused as follows: when the gate voltage of S_2 goes down during the turn-off transient, the charge held in the transistor realized by S_2 will be forced to leave. Since one end of S_2 is connected to the gate node of M_1, some charges of S_2 will be dumped to the gate of M_1, which changes the voltage across C_1. As a result, the current held in M_1 will deviate from I_{in}, and the charge-feedthrough error results.

The effect of error due to nonzero conductance of M_1 can be alleviated by using cascode structures [6,9] and negative feedback structures [7,14,18]. The current-storage transistor M_1 together with the input current source constitutes a voltage inverter in Figure 2.1(b) [7], but forms a source follower in Figure 2.1(c) [14,18]. In order to keep the feedback negative, the former implements an amplifier with a positive gain, while the latter employs a negative-gain amplifier. On the other hand, the charge-feedthrough error effect can be reduced by either increasing the capacitance C_1, or using appropriate switches. Recently, a fully differential-pair current copier, as shown in Figure 2.1(d) [17], was developed in which the distortion is reduced by cancelling even-order harmonics and crosstalk from neighboring digital circuits. The current copier in Figure 2.1(e) [17] can reduce both error effects mentioned above.

2.2 Multiplier and Divider Circuits

Current multipliers and dividers are usually implemented by using resistor networks or weighted transistors. However, the accuracy of such solutions is limited by resistor or transistor mismatch. To obtain accurate signal multiplication/division without the need for well-matched components, switched-current multiply-by-two (MX2) circuits [8] and divide-by-two (DB2) circuits [53,54] are introduced.

Figure 2.2(a) illustrates a 3-cycle MX2 circuit [8] which generates an output current equal to $2I_{in}$ without the need of well-matched devices. Initially, Switches S_0, S_1, and S_2 are turned on. After the op-amp is settled, I_1 will equal I_{in}. When S_2 is turned off, the gate capacitance will cause transistor N_1 to "*memorize*" the input current level. This procedure is then repeated for transistor N_2 by turning on S_0, S_3, and S_4. Once N_2 has been set, an output current of $2I_{in}$ is produced by turning on S_1, S_3, S_5 and S_6, which will cause I_{out} to be equal to I_1+I_2 (or $2I_{in}$).

Figure 2.2(b) shows an accurate current divider [53] which divides an input current by two. The number of iterations necessary to obtain half the current with certain accuracy depends on the mismatch of transistors N_2 and N_3. Each iteration takes three clock cycles. The current copying sequences for the first iteration and the remaining iterations are listed in (a1)-(c1), and in (A1)-(C1), respectively [53].

(a1)	$I_{in} \rightarrow N_2 \,\&\, N_3$	(A1)	$I_{in} \,\&\, N_1 \rightarrow N_2 \,\&\, N_3$
(b1)	$N_2 \rightarrow P_4$	(B1)	$N_2 \rightarrow P_4$
(c1)	$P_4 \,\&\, N_3 \rightarrow N_1$	(C1)	$P_4 \,\&\, N_3 \rightarrow N_1$

where "$I_{in} \rightarrow N_2 \& N_3$" in (a1) means that the input current I_{in} is stored to both copiers with N_2 and N_3. By (b1) and (c1), $I_1=I_2-I_3$ which is stored to the copier with N_1. Since the NMOS copier stores only a positive current, hence the divider functions properly only when $I_2 > I_3$.

Let α_2 and α_3 be the mismatch factors of the transistors N_2 and N_3, respectively, where $I_2=\alpha_2 I_{in}$, $I_3=\alpha_3 I_{in}$, and

$$\alpha_2 = [k_2(V_{gs}-V_{T2})^2] / [k_2(V_{gs}-V_{T2})^2 + k_3(V_{gs}-V_{T3})^2] \qquad (2.1)$$

$$\alpha_3 = [k_3(V_{gs}-V_{T3})^2] / [k_2(V_{gs}-V_{T2})^2 + k_3(V_{gs}-V_{T3})^2] \qquad (2.2)$$

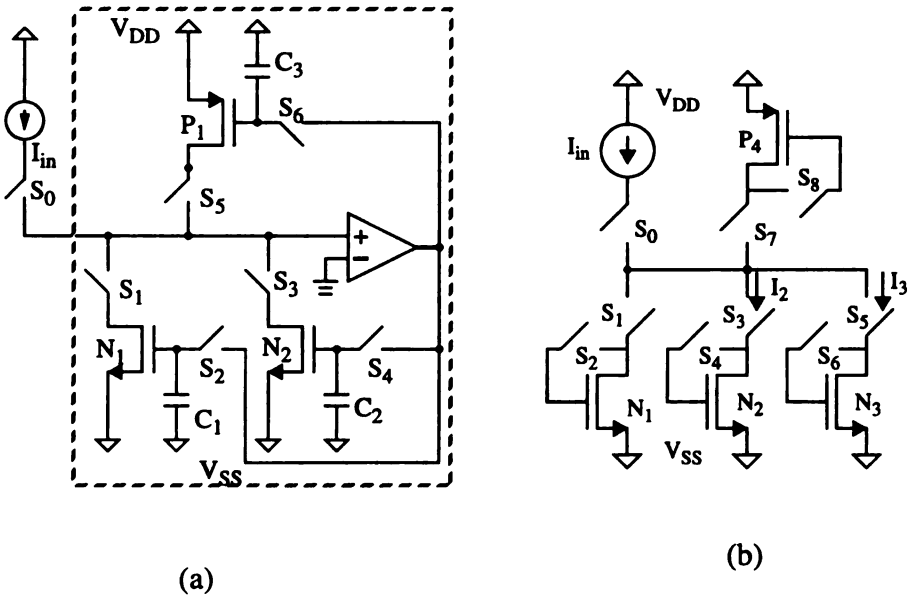


Figure 2.2 SI circuits: (a) MX2 [8]; and (b) DB2 [53].

where V_{T2} and V_{T3} are the threshold voltages of transistors N_2 and N_3, respectively, and the device transconductance $k_i=k_i'(W/L)_i$, i=1 or 2, is the aspect ratio of transistor N_i. Thus, $\alpha_2 > \alpha_3$ if $I_2 > I_3$. Because the transistor mismatch is generally unknown in advance, the current divider functions properly only when the mismatch factor $\alpha_2 > \alpha_3$. Thus, an alternative current divider is presented in [53], in which the division works for any mismatch factors. The relationship among the number of iterations required for the division process, the mismatch factor, and the desired accuracy, was derived as follows. Let γ denote the mismatch ratio, i.e., $\gamma=(\alpha_3/\alpha_2)-1$. According to the current copying sequence, the current held in N_3 at the end of the first cycle of the k-th iteration, denoted as I_{3k}, is expressed as [54]

$$I_{3k} = (I_{in}/2)\{1 + (-1)^{k-1}[\gamma/(2+\gamma)]^k\} \qquad (2.3)$$

Table 2.1 lists the relationship among the number of iterations k, the mismatch factor γ, and the accuracy, i.e., $|I_{3k}-I_{in}/2|/(I_{in}/2)$, or $|[\gamma/(2+\gamma)]^k|$. Apparently, the error term $[\gamma/(2+\gamma)]^k$ diminishes rapidly as k increases, i.e., $I_{3k} \approx I_{in}/2$. Thus, the error term is used to determine the number of iterations necessary to obtain $I_{in}/2$ with certain accuracy. Results show that the divider can achieve an accuracy of 6.21×10^{-6} by taking five iterations for 20%. On the other hand, for a practical 1% transistor mismatching, the circuit takes only two iterations to achieve an accuracy of 2.47×10^{-5}.

2.3 Data Converter Circuits

This section reviews the basic data converter algorithms and data converter circuits.

Table 2.1 Relationship among k, γ, and accuracy.

(k: number of iterations, γ: mismatch factor)

k	γ=20%	γ=10%	γ=5%	γ=2%	γ=1%
1	9.09e-02	4.76e-02	2.44e-02	9.90e-03	4.97e-03
2	8.26e-03	2.26e-03	5.95e-04	9.80e-05	2.47e-05
3	7.51e-04	1.07e-04	1.45e-05	9.70e-07	1.23e-07
4	6.83e-05	5.14e-06	3.53e-07	9.60e-09	6.12e-10
5	6.21e-06	2.45e-07	8.63e-09	9.51e-11	3.04e-12
k	γ=-20%	γ=-10%	γ=-5%	γ=-2%	γ=-1%
1	1.11e-01	5.26e-02	2.56e-02	1.01e-02	5.02e-03
2	1.23e-02	2.77e-03	6.57e-04	1.02e-04	2.52e-05
3	1.37e-03	1.45e-04	1.68e-05	1.03e-06	1.26e-07
4	1.52e-04	7.67e-06	4.32e-07	1.04e-08	6.37e-10
5	1.69e-05	4.03e-07	1.11e-08	1.05e-10	3.20e-12

2.3.1 Conversion Algorithms

A DAC converts binary numbers, represented by patterns of 1's and 0's, into discrete analog data represented by, either voltage or current. To simplify the discussion in the later chapters, current data conversion is referred to. Depending on how the DAC is configured, the transfer function of a DAC can be unipolar (outputs having only positive or negative values, but not both) or bipolar (outputs can be either positive or negative). There is a simple linear correspondence between the input codes and the output current levels. For an N-bit DAC, the output current is represented by

$$I_{out} = I_{FS} (b_1/2 + b_2/4 + .. + b_{N-1}/2^{N-1} + b_N/2^N) \quad (2.4)$$

where the coefficients, b_1, b_2, .., b_N, represent the logic levels of the input bits, which can be 1 or 0, b_1 is the *most significant bit* (MSB) while b_N is the *least significant bit* (LSB), and I_{FS} is the full-scale (FS) current. Eqn (2.4) can be achieved from the following recursive algorithm,

$$I_k = I_{k-1} / 2; \quad (2.5)$$

$$B_k = B_{k-1} + b_{N-k+1} \times I_{k-1}; \qquad k=1,2,..,N \quad (2.6)$$

where I_k is the reference current for the k-th bit conversion and B_k is the current that is accumulated at the end of the k-th bit conversion. The initial conditions for (2.5) and (2.6) are $B_0=0$, and $I_0=I_{FS}$. For simplicity, this approach is referred to as the *dividing conversion* (DC) approach.

On the other hand, $I_{FS}=2^N I_{LSB}$, or $I_{LSB}=I_{FS}/2^N$, where I_{LSB} is the current for converting the LSB. Eqn (2.4) can be rewritten as

$$I_{out} = (b_1 2^{N-1} + b_2 2^{N-2} + .. + b_{N-1} 2 + b_N) I_{LSB} \quad (2.7)$$

and can be achieved by the following recursive algorithm,

$$B_k = B_{k-1} + b_{N-k+1} \times J_{k-1}; \qquad k=1,2,..,N \tag{2.8}$$

$$J_k = 2 \times J_{k-1}; \tag{2.9}$$

where J_k is the reference current for the (N-k)-th bit conversion and B_k is the current that is accumulated at the end of the (N-k)-th bit conversion. The initial conditions for (2.8) and (2.9) are $B_0=0$, and $J_0=I_{LSB}$. This approach is referred to as *multiplying conversion* (MC) approach.

The objective of an ADC is to determine the output digital word corresponding to an analog input signal. The ADC usually requires a sample-and-hold (S/H) circuit at the input because it is not possible to convert a changing input signal. The characterization of the ADC is almost identical to that of the DAC if the input and output definitions are interchanged. Cyclic (or algorithmic) and successive-approximation (SA) ADCs convert an input signal (either current or voltage) into an N-bit digital data word using the MC or the DC approach, respectively.

More specifically, a cyclic ADC first samples and holds an input current/voltage, and converts the MSB of the input current/voltage by comparing twice the input current/ voltage to the reference current/voltage. If the signal exceeds the reference, the MSB will be a "1" and a residual current/voltage is the difference of twice the input signal and the reference. Otherwise, the MSB will be a "0" and the residual current/voltage is just the twice the input signal. The residual current/voltage is then converted to find the next bit. This sequence is repeated until the desired resolution has been achieved. Thus, a cyclic ADC requires a multiply-by-two (MX2) circuit to generate the double residual current/ voltage value.

On the other hand, the SA ADC requires a divide-by-two (DB2) circuit to generate

the weighted references, as in Eqn. (2.4). The SA ADC converts the MSB of the input current/voltage by comparing it to the generated weight which is half of the reference at this step. If the input signal exceeds the weight, the MSB will be a "1" and the residual current/voltage is the difference of the input signal and the weight. Otherwise, the MSB will be a "0" and the residual is just the input signal. The residual is then converted to calculate the next bit. This sequence is repeated until the desired resolution is achieved.

2.3.2 Design Specifications of Data Converters

One of th basic problems in specifying the transfer function of an A/D convert is that the characteristics of the transfer function are dependent on the application and test circuit, the type of input signal, and the sampling rate of the converter [55]. This section reviews the important parameters and terminology used in the data converters developed in this thesis.

Dynamic range is the ratio of the largest input that can be converted to the smallest step size of the converter. For example, a 10-bit current-mode ADC with an input range from 100μA to 600μA has a quantization step size of $(600\mu\text{-}100\mu)/2^{10} \approx 0.5\mu\text{A}$. Therefore, the dynamic ratio is 1024 and can be also expressed in decibnels as $20\ log1024 = 60$ dB.

Resolution refers to the number of quantization levels an input signal can be determined to. This number is usually given in bits. For example, if which of 1024 levels an input signal lies within can be identified, then the converter is said to have an 10-bit resolution.

Effective number of bits (ENOB) is a measure of overall A/D performance under dynamic conditions. Cumulative effects of many error sources such as quantization noise,

dynamic differntial nonlinearity error, missing codes, integral nonlinearity, jitter, and noise, all contribute to a lower effective number of bits. In general, ENOB can be calculated from the SNR obtained from dynamic FFT testing, i.e., ENOB=(SNR-1.76)/6.02.

Differential nonlinearity (DNL) error is a measure of how uniform the transfer function step sizes are. Each step size is compared to the ideal step size, i.e., $(I_{max}-I_{min})/(2^b-1)$. An difference in magnitude is DNL error. If the DNL error is less than one LSB, the converter will not have any missing codes. If the DNL error is less than 0.5 LSB, the converter will be monotonic.

Integral Nonlinearity (INL) error is the deviation of code midpoints from their ideal locations. A differential error is the error in a particular step size at any specific location in the converter transfer function. Integral error is equivalent to the integration (summation) of these errors along the converter's transfer function.

Signal-to-Noise ratio (SNR) is characterixed by sampling a pure sinusoidal input and performing an FFT on the collected data. SNR is the ratio of the magnitude of the fundamental frequency to the root mean square (rms) of all other frequencies including harmonics.

2.3.3 CMOS SI ADC Circuits

The ADC circuits can be generally classified into three categories according to their conversion speed: Flash/Folding techniques [29,32], Algorithmic/Successive approaches [34,56], and Oversampling techniques [35,36]. Flash/folding techniques have the fastest conversion speed but the lowest resolution, while the oversampling ones have the slowest speed but the highest resolution. *Cyclic* or *algorithmic conversion* is well

known for its ability to achieve medium resolution within small silicon area [58].

Figure 2.3 illustrates the cyclic conversion algorithms: (1) based on the conventional restoring numerical division principle [59], as shown in Figure 2.3(a), referred to as conventional cyclic conversion algorithm; (2) based on the RSD (Redundant Signed-Digit) cyclic conversion with the SRT division principle developed by Sweeney, Robertson, and Tocher [59], as shown in Figure 2.3(b); and (3) based on the RSD cyclic conversion with the modified SRT division principle [24], as shown in Figure 2.3(c), referred to as modified RSD cyclic conversion algorithm.

The conventional cyclic conversion algorithm, consists of the multiplication of two of the signal to be converted followed by a comparison of the result with a reference voltage (current): If the signal is larger than the reference, the MSB (most significant bit) of the output code is set to 1, and the reference is subtracted from the signal; else, the MSB is set to 0, and no arithmetical operation is carried out. The remaining part of the signal, the so-called "residue voltage (current)" corresponding to the partial remainder of the division, undergoes the same operation for the next bit decision, and the loop is run until the LSB (least significant bit) is obtained. The ADC in [8], as shown in Figure 2.4(a), adopts this conversion algorithm. For the modified RSD cyclic conversion algorithm, two conversion levels P and Q are used, where P is positive and Q is negative. If the input signal, twice of the residue voltage (current) is larger than 2P, the output code bits is set to a 1 and the reference is subtracted; if it is smaller than 2Q, the output code is set to -1 and the reference is added; else, then the bit is set to 0 and no arithmetical operation is carried out. The ADCs with switched-capacitor [58] and switched-current [10] techniques adopt this algorithm. The modified RSD conversion algorithm provides a large tolerance for the

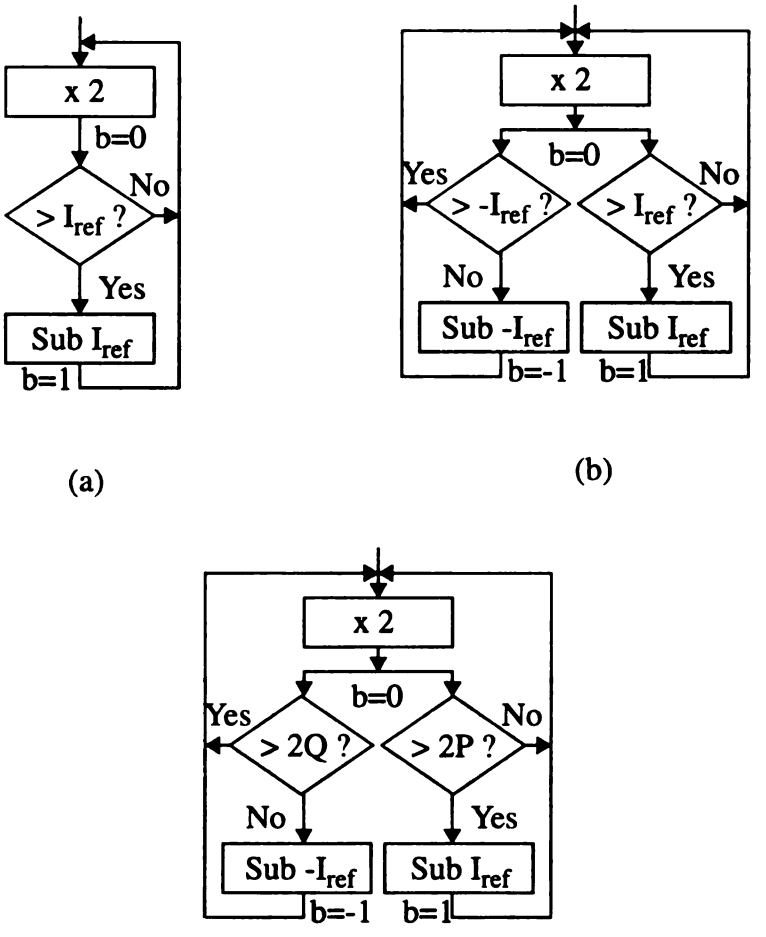
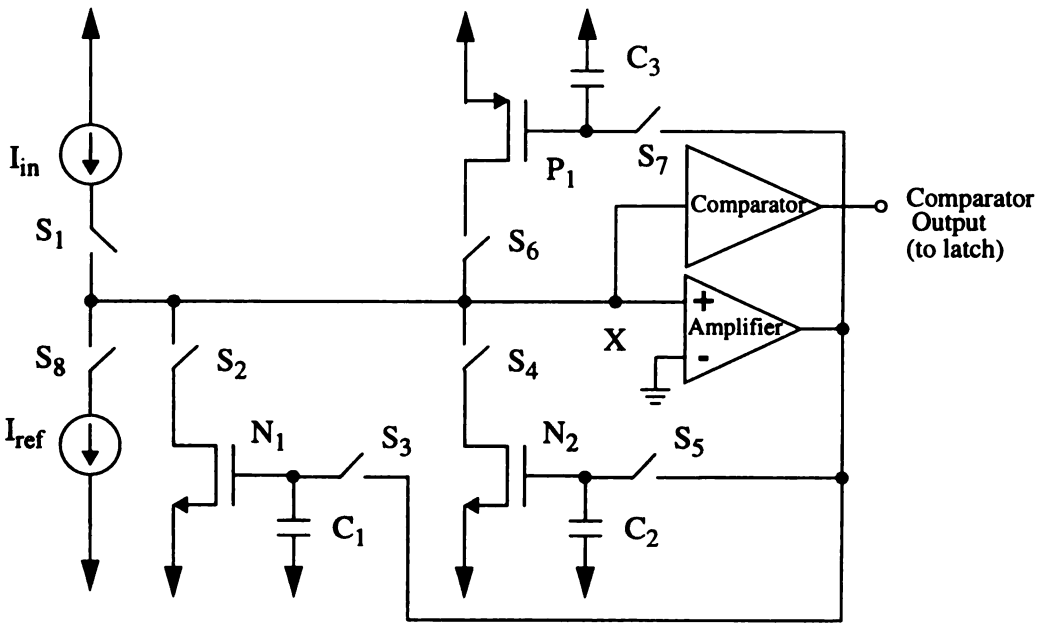
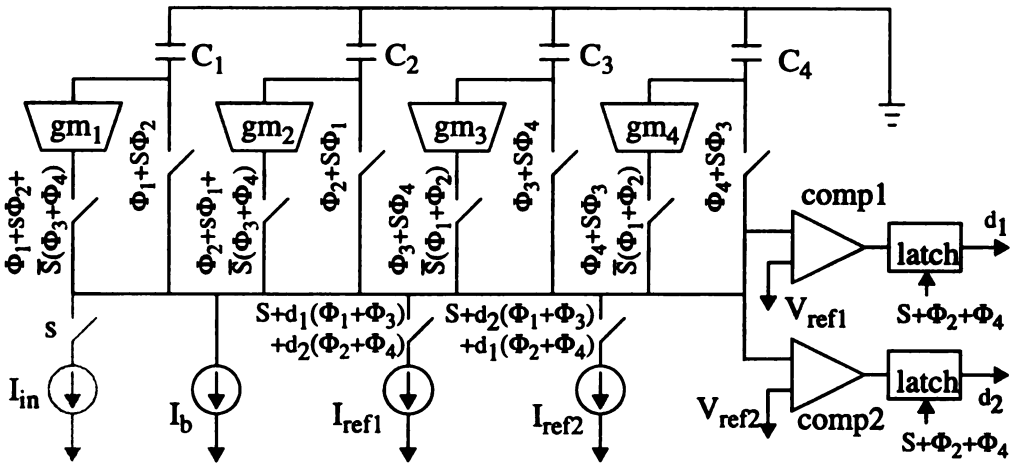


Figure 2.3 Cyclic conversion algorithms: (a) conventional restoring numerical division; (b) RSD approach on the SRT division; and (c) RSD approach on the modified SRT division (referred to as modified RSD approach)



(a)



(b)

Figure 2.4: Cyclic ADC Circuits: (a) in [8]; and (b) in [16,18].

comparator's inaccuracy, thus high levels of noise, error effect, and even hysteresis are allowed [58]. The detail design and operation of the ADCs with the above both conversion approaches will be discussed in the next section.

The ADC in [8] employs a residual amplifier which takes three cycles to double a current, and it requires 4 cycles to complete one bit conversion. The residual amplifier in [10,58] also requires 3 cycles to double a current, but the ADC's needs only 3 cycles to complete one bit conversion. A dynamic calibration technique was employed to alleviate the error due to component mismatch. However, the accuracy of the residual amplifier is limited by two major error effects, *charge-feedthrough* and *non-zero output conductance* of a copier. The errors are introduced and accumulated at each cycle. To reduce such errors, a two-cycle residual amplifier for a SI cyclic ADC, as shown in Figure 2.4(b), which takes only 2 cycles to complete one bit conversion was presented in [16,18].

2.3.3.1 4-cycle Conversion

Figure 2.4(a) illustrates the schematic diagram of the ADC circuit [8], where a 3-cycle residual amplifier, as shown in Figure 2.2(a), is employed. The converter is comprised of two NMOS current copiers, one PMOS copier, an op-amp, and a current comparator. The converter starts converting for the most significant bit (MSB) of an input current I_{in} by generating twice the input signal and holding into P_1. After doubling the current, the current held in P_1 compares with the reference current I_{ref} in the 4th cycle. If the signal exceeds the reference, the MSB will be a "1", otherwise it will be a "0". This completes the conversion for the MSB.

The remaining (N-1) bits are then converted in the same manner. The signal held in

P_1 is loaded into N_1. If the preceding bit was a "1", the reference is substracted from the signal in P_1. On the other hand, if it was a "0", the signal remains unchanged. Once N_1 is set, N_2 is followed by the same procedure of N_1. The signal is then doubled and stored on the gate of P_1. Finally, it is compared with the reference. This sequence is repeated until the desired resolution has been achieved. An end of conversion pulse is then generated to signal the end of conversion. The converter achieves a 10-bit resolution and a sample rate of 250 kbits/s.

This ADC adopts the conventional restoring numerical division principle. Taking the comparator error into consideration, the residual current may fall off the convergence region and provides incorrect decision [10]. Therefore, such an ADC design needs a comparator with high accuracy and an operation amplifier with low offsets.

2.3.3.2 2-cycle Conversion

The number of cycles in conversion can be reduced to two by using four current copiers and comparing the residual current in the amplification phase [16,18]. Figure 2.4(b) shows the structure of the 2-cycle A/D converter. During the conversion state, where the start signal S is low, the four copiers are grouped as two copier pairs, $gm_{1\text{-}2}$ and $gm_{3\text{-}4}$. At each bit conversion, the residue current, the sum of the currents stored in a copier pair, is copied during Φ_1 and Φ_2 (or Φ_3 and Φ_4) to two current copiers to gm_1 during Φ_1, while this sum is copied to gm_2 during Φ_2. The sum of the current stored in the latter pair (gm_1 and gm_2) becomes the new residue current and is copied back to the former pair (gm_3 and gm_4), respectively. Since it takes one cycle to copy the residue current in the

former pair to a current copier in the latter pair, the residue amplifier takes only two cycles to double a current. Two comparators are used to monitor the transconductance current indirectly. The relationship between the input voltage and the current in the transconductance is $I_i=gm_iV_{ci}$, where I_i is the current of transconductance gm_i and V_{ci} is the voltage on the capacitance Ci. Therefore, the voltages V_{ci} can be compared with the reference voltages V_{ref1} and V_{ref2} in the circuit. Since large comparator errors are permitted by a RSD algorithm, neither exact transconductance nor accurate comparators are needed. The comparison results are latched at the ends of Φ_2 and Φ_4, where the conversion for one bit is completed. The single-bit binary outputs d_1 and d_2 of the latches control the two reference currents I_{ref1} and I_{ref2} to implement a RSD algorithm. There exists a large tolerance of $I_{ref}/4$ for the comparison levels. Results show that the 2-cycle ADC can achieve 12-bit resolution, 50ns/b conversion rate, and 5mW power consumption.

2.3.4 CMOS SI DAC Circuits

Figure 2.5(a) illustrates a design of current-mode DAC, where the current reference generator (CRG) generates the current references, or binary weights, for the converter. Figure 2.5(b) shows a typical CRG circuit, where the current references are realized by ratioed currents. To obtain accurate signal multiplication/division without the need for well-matched components, a switched-current CMOS CRG circuit using MC approach, referred to as CRG_MC circuit, was developed in [60] which generates the current references in (2.8) and (2.9). Recently, a switched-current CRG circuit using DC approach, referred to as CRG_DC circuit, was presented in [47] which generates the cur-

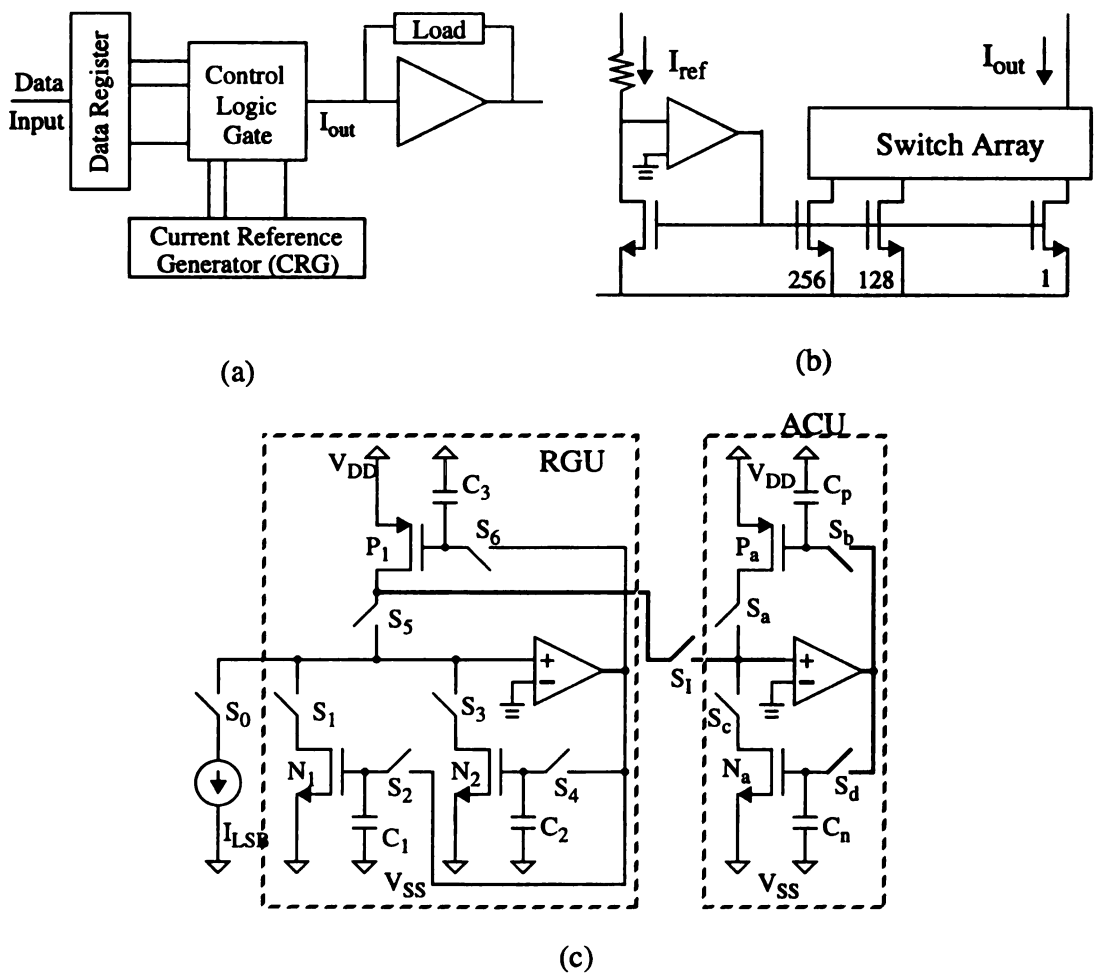


Figure 2.5 Current-Mode DAC circuits: (a) a typical design; (b) a typical current reference generator (CRG); and (c) a SI DAC with CRG_MC [47].

rent reference in (2.5) and (2.6). Thus, both CRG_DC and CRG_MC can be used as the current reference generator of the DAC in Figure 2.5(a).

Figure 2.5(c) shows the algorithmic current-mode DAC in [47]. The converter consists of a *current Reference-Generating Unit* (RGU), a *switch* S_I, and a *current ACcumulation Unit* (ACU). The RGU is used to generate the double current reference [60] which is exactly the same as the CRG_MC circuit; The switch S_I is controlled by the digital input code, where the switch is turned on when b_i=1 and off when b_i=0, for i=N, N-1,.., 1; The ACU is employed to conduct the current accumulation in (2.8). The RGU, realized by the multiply-by-two circuit (MX2), is shown in Figure 2.2(a). The double current reference I_k generated by the RGU is stored in P_1. The ACU is comprised of an NMOS copier and a PMOS copier with an op-amp. Whether or not a current reference generated by the RGU is accumulated is determined by each input bit b_k. If b_k=1, i.e., S_I is on, then the current reference is accumulated and finally stored in P_a; otherwise, the current held in P_a is unchanged. The RGU needs four cycles to generate a current reference for each bit conversion, while the ACU requires two cycles for the current accumulation. Therefore, for repetitive conversions of continuously changing inputs, the converter requires (4N-2) clock cycles for simultaneously converting three N-bit digital data signal. For a single conversion, the converter may need (4N-1) cycles. Conversion rate can be improved by using a parallel DAC presented in [47] in which the converter can simultaneously convert seven digital data signals in a demultiplexing fashion. The PMOS copier in the ACU is used to store the accumulated current while the NMOS copier acts as a temporary storage element. Conversely, the reference current is stored in the NMOS copiers of the RGU. Thus,

the NMOS copier in the ACU holds the accumulated current while the PMOS copier is used only as a temporary storage element.

2.4 Test Generation of SI Circuits

Although mismatched components are allowed in SI circuits, the SI circuits are still susceptible to faulty switching elements. Any faulty switching elements may result in an incorrect converted data. Based on single stuck-at fault model on the switching elements, the fault behaviors of the ADC in Figure 2.4(a) have been reported [51], in which a faulty switch can be either permanently stuck-at ON state (S/ON) or OFF state (S/OFF). The failure of other components can be modeled as the fault of the associated switch. Thus, the converter can be fully testable. Due to the simplicity of the test generation process, a built-in self-test (BIST) design of the ADC is developed in [62]. However, the simulation results reported in [48] show that stuck-at faults, or catastrophic faults, are approximately 70% of the total faults. This implies that 30% of the total faults are still undetectable. These faults are referred to as parametric faults. Therefore, an efficient and effective fault macromodeling process was developed to enhance the testability of SI circuits [48].

2.4.1 Fault Models

Based on circuit layout, technology data, and defect statistics, a set of fault types was developed [50]. According to the functionality of switches in a SI circuit, two types of switches can be identified: voltage switch and current switch. Based on the circuit layout, Table 2.2 shows five examples of process defects which are significant and cause the cir-

Table 2.2. Summary of defects and circuit faults.

Defect	Circuit fault	defect type
Break of metal	a floating drain/source	*Type f1*
	disconnects the switch's input/output	*Type f2*
Break of gate polysilicon	a floating gate may trap some amount of charges on the gate isolates the gate of PMOS transistor isolates the gate of NMOS transistor	*Type f3* *f3-P* *f3-N*
	shortens the channel width.	*Type f4*
Defects in active region	increases the channel impedance	*Type f5*

cuit to malfunction, and summarizes the faults due to these defects. Based on the defects, four fault types of the voltage switch and three fault types of the current switch are concluded and summarized in Table 2.3 [48-51]. Based on the fault types, test generation processes for current copiers [50] and SI ADC [49] were reported and they are discussed below.

2.4.2 Test Generation of Current Copiers

Consider the basic current copier cell in Figure 2.1(a). The switch faults are summarized in Table 2.2, and the faults on current-storage transistors and holding capacitors can be modeled as the equivalent faults of the associated switch(es) [48,61]. In addition, the following defects may occur in a current-storage transistor. Breaks on gate polysilicon, a Type f3 defect, is equivalent to an S/OFF fault on the associated voltage switch, a Type VS1 fault. Shorten channel width, a Type f4 defect, is equivalent to a Type CS1 fault. Break on metal, either drain or source, a Type f1 defect, is equivalent to an S/OFF fault on the associated current switch, a Type CS1 fault. A short between drain and gate implies an S/ON fault on the associated voltage switch, a Type VS2 fault; A short between source and gate, or between drain and source, is equivalent to a S/OFF fault on the associated voltage switch, a Type VS1 fault. Any defects in active region, a Type f5 defect, is equivalent to a Type CS1 fault. Any process deviation causing an increase of on-resistance implies the presence of a Type CS1 fault. The following defects may occur in the holding capacitors. Any defects causing a decrease of capacitance, or an open circuit in the capacitor, is equivalent to a Type VS4 fault on the associated voltage switch. Any defects caus-

Table 2.3. Fault types.

(a) Voltage Switch

Fault Types	Time Constant	Leakage Current
VS1	Intolerable	Tolerable
VS2	Tolerable	Intolerable
VS3	Intolerable	Intolerable
VS4	Excess charge flows out switch when switch is off	

(b) Current Switch

Fault Types	Error Current (switch is on)	Leakage Current (switch is off)
CS1	Intolerable	Tolerable
CS2	Tolerable	Intolerable
CS3	Intolerable	Intolerable

ing an increase of capacitance, or a short circuit in the capacitor is equivalent to a Type VS1 fault

The above equivalent faults include both catastrophic and parametric faults for both current-storage transistors and the holding capacitors in a copier. Based on the fault types in Table 2.3, the fault behaviors, as illustrated in Figure 2.6 [50], can be distinguished from the fault-free behavior by the test sequence. Thus, all fault types in Table 2.3 can be tested.

2.4.3 Test Generation of ADC Circuits

Consider the ADC from Figure 2.4(a) with a comparator, as shown in Figure 2.7. In the comparator, a current copier consisting of N_3, C_4 and switches S_x and S_y, is used as a load to copy the difference current I_x. Since the difference current may be positive or negative, a bias current source I_{b1} is used to keep a positive current to be copied to N_3. A current which is slightly higher than I_{ref} is chosen for I_{b1}. The copier memorizes the current I_x and produces a voltage deviation to compare to a zero-voltage in the comparator. Since the resolution of an ADC is 0.5 LSB, or 0.5 I_{ref}, here a simple comparator instead of window comparator, can be used. It should be noted that an additional bias current $I_{b2}=I_{ref}$ and the switch S_z are used only for testing purpose. During the normal operation, S_z is off and the bias current is isolated from the converter circuit. Thus, the extra circuitry does not affect the performance of the converter.

In Figures 2.4(a) and 2.8, S_1, S_2, S_4, S_6, S_8, S_x, and S_z are current switches, while S_3, S_5, S_7, and S_y are voltage switches. The ADC consists of four copiers. One may apply

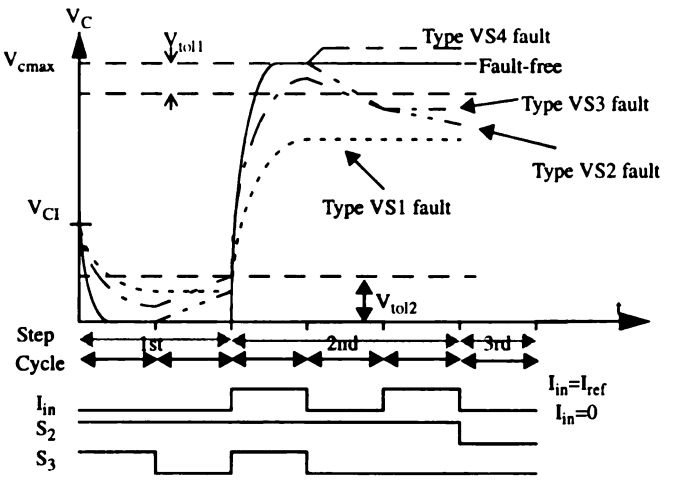


Figure 2.6 Fault behavior and switching sequence

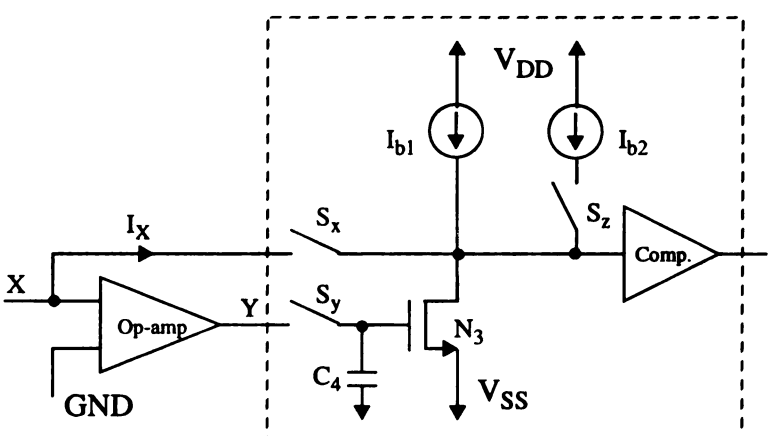


Figure 2.7 Simplified schematic diagram of SI algorithmic ADC with additional comparator

the test sequence developed in the previous section for all copiers in the ADC. However, in the ADC, we can only observe the result from the output of the comparator, i.e., the converted digital data. Thus, the test sequence should be generated to maximize the accumulated errors so that the error effect can be reflected to the converted digital data [49].

Figure 2.8 illustrates the fault behaviors and switching sequences of a test sequence, referred to as Test Sequence A, which detects *Types VS1, VS3,* and *VS4* faults for S_3, S_5, and S_7, *Types CS1-CS4* faults for S_1, S_2, S_4, S_6, and S_{10}, and *Types CS2* and *CS3* faults for S_x. Figure 2.9 shows the fault behaviors and switching sequence of another test sequence, referred to as Test Sequence B, which detects T*ypes VS2* and *VS3* faults for S_3, S_6, S_7, *Types CS1* and *CS3* faults for S_x, *Types CS1-CS3* faults for S_z, and *Types VS1-VS4* faults for S_y. This implies that both test sequence will detect all switching faults.

2.5 Discussion

Current copier is the basic building block of a SI circuit. The performance of a SI circuit is determined by the performance of the current copiers it employs. Thus, synthesizing optimum current copiers for SI circuits beomes very important task in the SI circuit design [63].

The objective of this study is to develop high performance and low power data converters. For the design of CMOS SI DAC circuits, as discussed in Section 2.3.4, the CRG circuit can be either realized by using the CRG_DC circuit or CRG_MC circuit. However, for an N-bit CRG_DC circuit, its LSB current, $I_{LSB}=I_{FS}/2^N$, cannot be lower than its SNR. This implies that its bit size is limited by the given full-scale current I_{FS}. It also implies that, for a given SNR of an N-bit CRG_DC circuit, the only way to increase

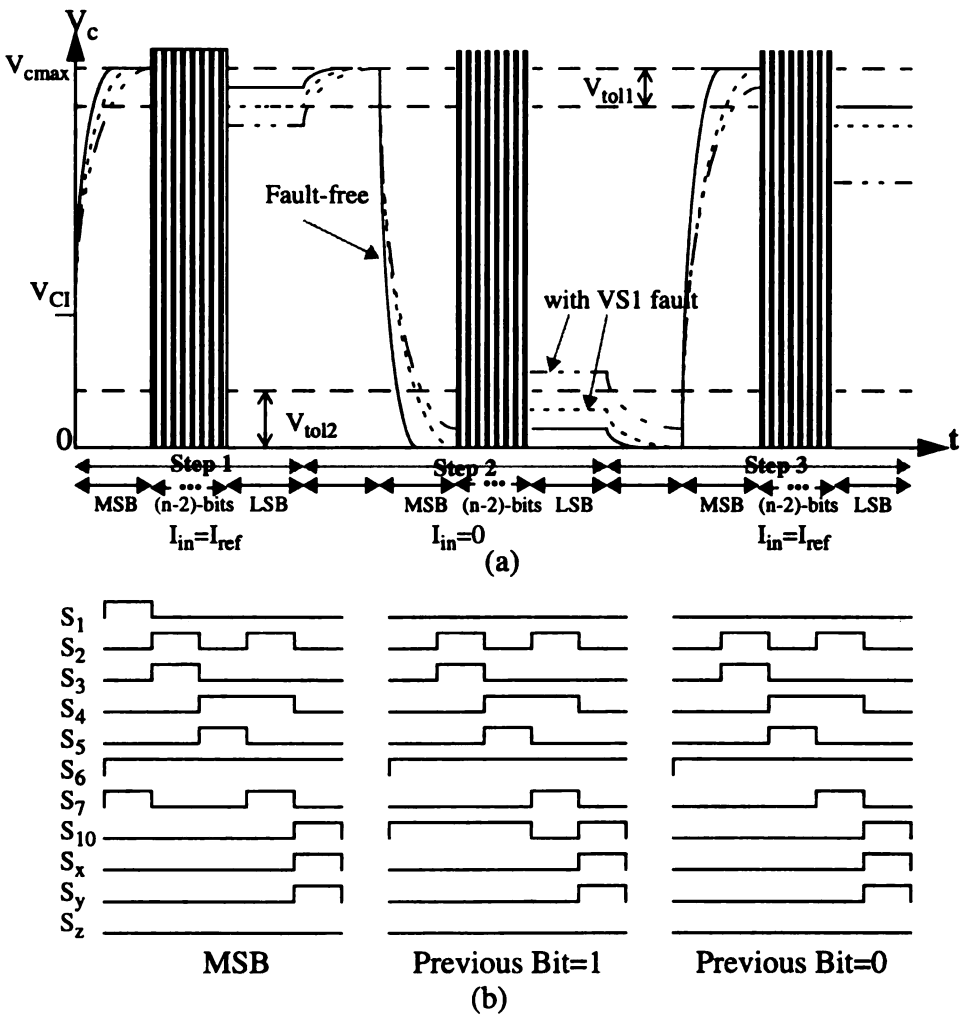


Figure 2.8 Test sequence A: (a) Fault behaviors; (b) Switching sequence.

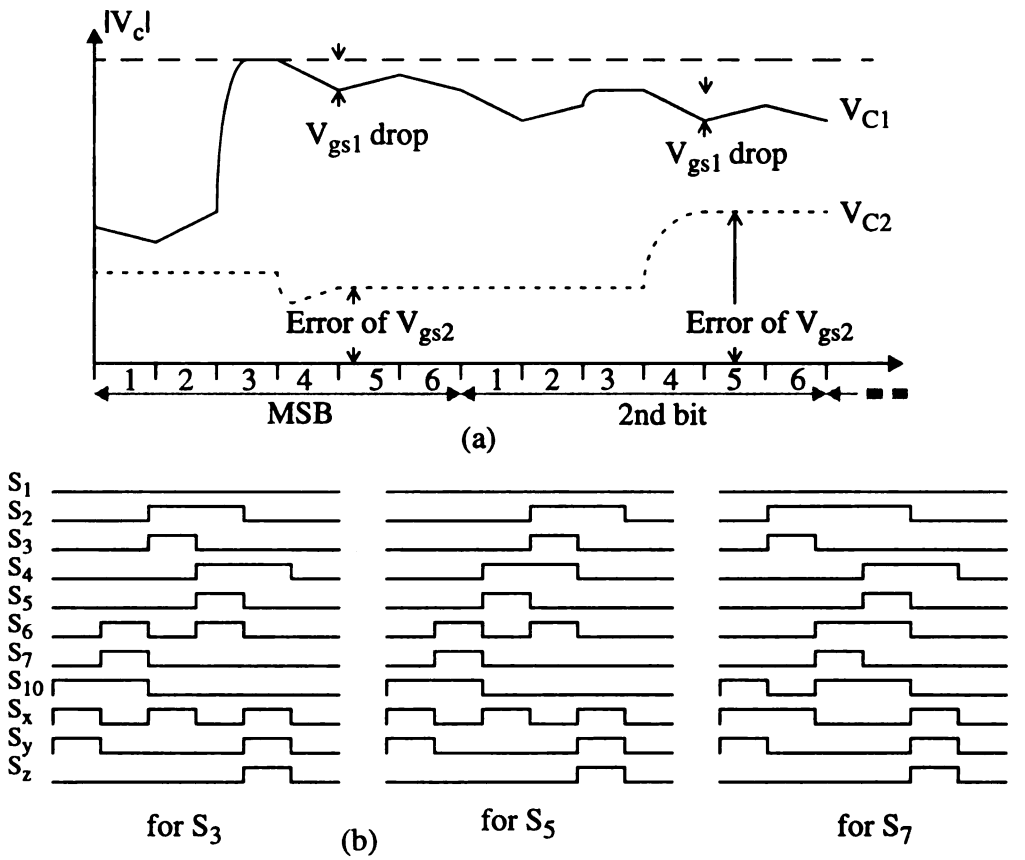


Figure 2.9 Test Sequence B: (a) Fault Behavior; and (b) Type VS2 fault.

the bit size is the use of larger I_{FS}, but it will be penalized by the increase of power consumption. This concludes that the bit size of both CRG_DC and CRG_MC circuits cannot be arbitrarily large for low-power applications. Therefore, to increase the resolution of a SI CMOS DAC circuit for low-power application, Chapter 4 will present alternative structures of DAC circuit combining CRG_DC and CRG_MC circuits.

As discussed in Section 2.4, test signals for testing current copiers and ADC circuits with the catastrophic faults can be easily generated and applied. However, test generation for those circuits with the parametric faults will become much complex [48]. This is partially due to the lack of accessibility. As suggested in [48], a built-in tester can be used to simplify the test generation and application. In practice, however, the built-in tester must be able to test itself to increase the reliability of the tester and also autozero the comparator to increase the accuracy of the tester. Chapter 6 presents a built-in tester which includes a current comparator with autozero and self-test capabilities.

Chapter 3

CMOS SI ADC CIRCUIT DESIGN

This chapter presents a high-speed, high-resolution, and low-power CMOS SI ADC circuit [64]. High performance is attributed to the use of the following components: (1) a high-performance residual amplifier which takes two clock cycles to double a current; and (2) an efficient cyclic RSD algorithm which provides 1.5b resolution without using two matched reference currents. Section 3.1 describes the design and operation of the developed ADC using a 2-cycle residual amplifire and 2-cycle conversion algorithm. Section 3.2. discusses the design consideration for achieving high performance and lower power. Section 3.3 presents the design, simulation, layout, and measurement of the fabricated chip. Finally, a concluding remark is given in Section 3.4.

3.1 Design and Operation

This section presents the developed 2-cycle residual amplifier and 2-cycle conversion algorithm. The special features in the residual amplifier are: (1) the amplifier has a negative gain; and (2) the use of two reference currents which do not need to be well-matched. Based on the special features, the modified RSD algorithm is used for the developed CMOS SI ADC.

3.1.1 2-cycle Residual Amplifier

To reduce the number of cycles, a 2-cycle residual amplifier is developed as shown in Figure 3.1(a), where four copiers are used. First, the input current is copied to copiers 1 and 2 in two consecutive cycles, where $I_1(1)=I_2(1)=I_{in}$. Then, the sum current, $I_1(1)+I_2(1)=2I_{in}$ are stored to copier 3 and then to copier 4. Both copiers 3 and 4 hold the same doubled current, i.e., $I_3(2)=I_4(2)=I_x=2I_{in}$. Similarly, the sum currents, $I_3(2)+I_4(2)=2I_x$, are then stored to copier 1 and then to copier 2. Thus both copiers 3 and 4 have the same doubled current, i.e., $I_1(1)=I_2(1)=2I_x$.

Let $I_1(2m-1)$ and $I_2(2m-1)$ be the currents held in copiers 1 and 2, respectively, and determine the (m-1)-th bit D_{m-1}. The sum current $I_1(2m-1)+I_2(2m-1)$ is stored to copier 3 and then copier 4, as shown in Figures 3.1(b) and 3.1(c), where $I_3(2m)=I_4(2m)=I_1(2m-1)+I_2(2m-1)$. The sum current determines the m-th bit. Similarly, as shown in Figures 3.1(d) and 3.1(e), the sum current $I_3(2m)+I_4(2m)$ is copied to copier 1 and then to copier 2 to determine the (m+1)-th bit. The process is repeated and it takes 2 cycles to double a current.

When the sum current $I_1(2m-1)+I_2(2m-1)$ is stored to copier 3, once the copier is settled, the voltage at node X, as denoted in Figure 3.1(a), is compared to determine the m-th bit. Similarly, the (m+1)-th bit is determined when the sum current is copied to copier 1, as shown in Figure 3.1(d). Thus, the ADC design using the developed residual amplifier takes only 2 cycles for one bit conversion.

3.1.2 2-cycle Conversion with Modified RSD Algorithm

Figure 3.2 shows the schematic circuit diagram and block diagram of the developed SI cyclic ADC design, where copiers 1 and 2 are implemented with NMOS copiers, and

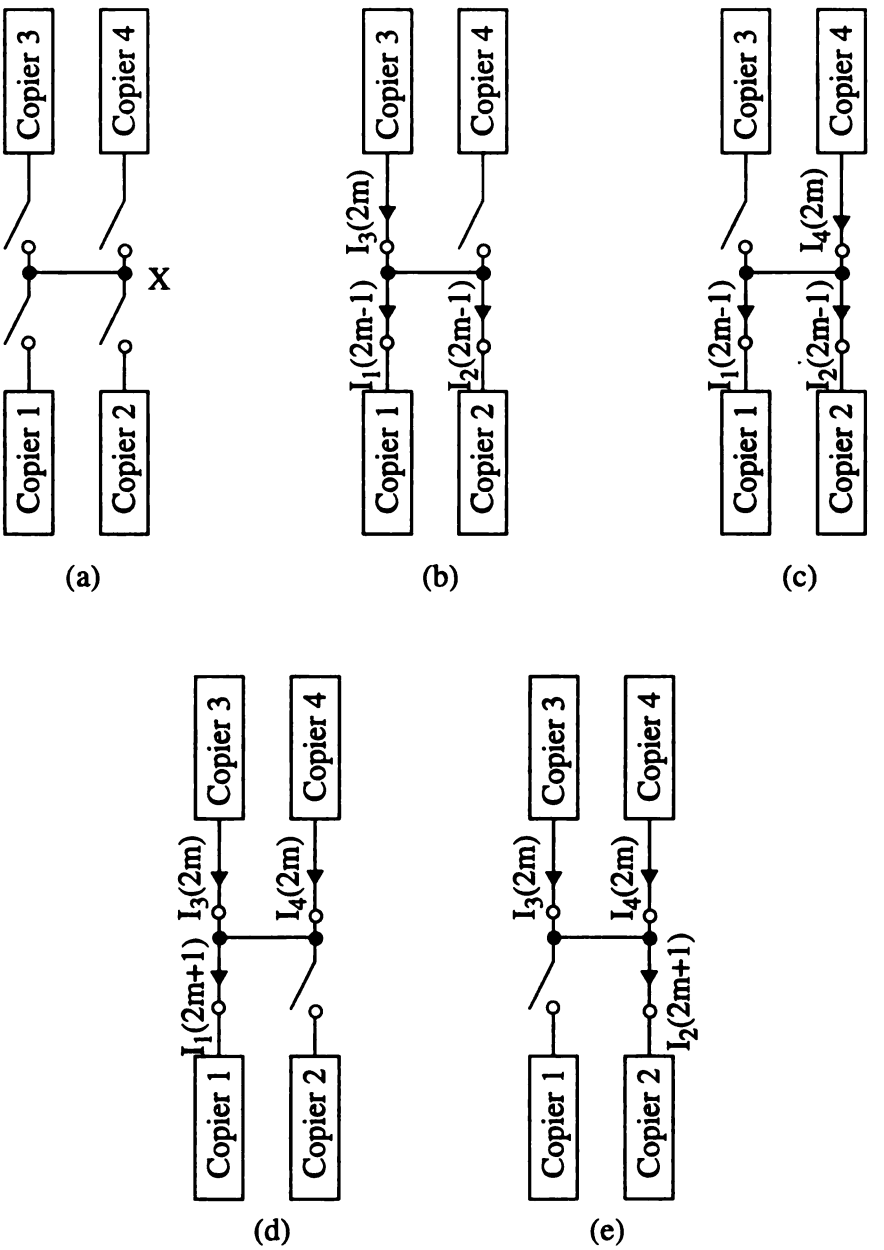
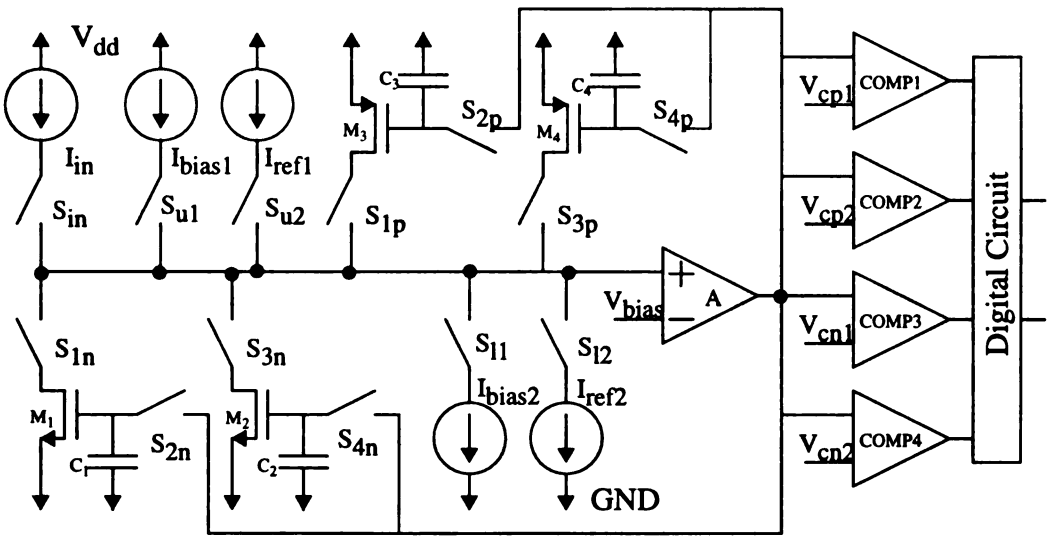
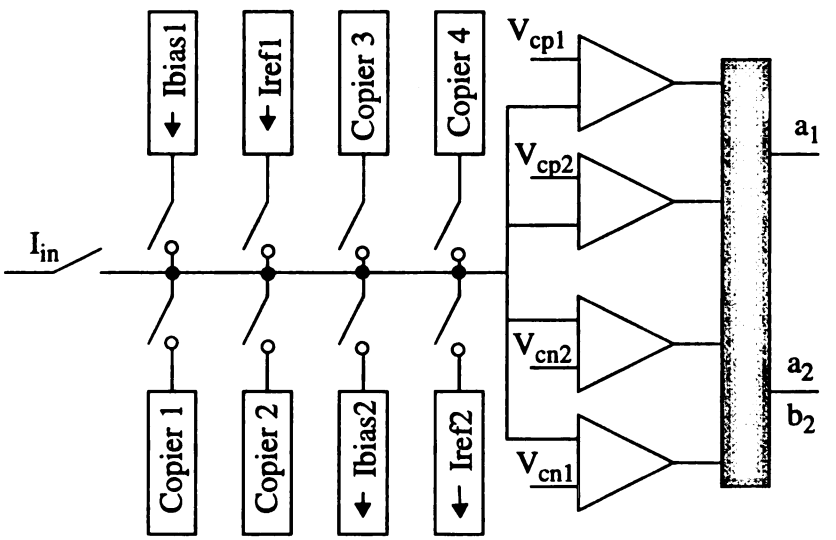


Figure 3.1 Proposed 2-cycle residual amplifier: (a) block diagram with 4 copiers; (b)&(c) operations for m-bit; and (d)&(e) operations for (m+1)-bit.



(a)



(b)

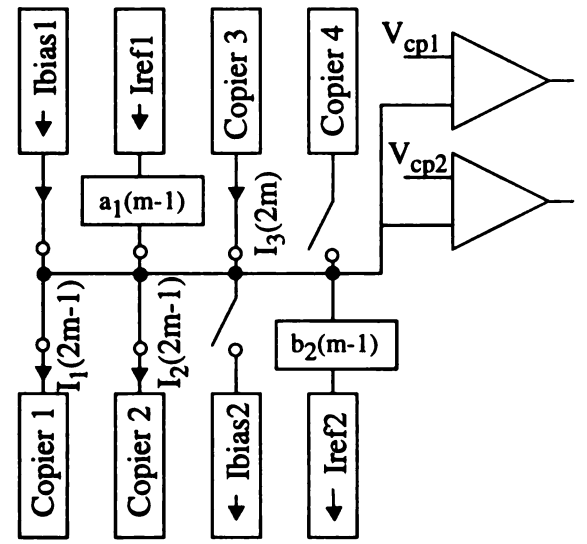
Figure 3.2 Proposed switched-current CMOS cyclic ADC:
(a) schematic diagram; and (b) block diagram.

copiers 3 and 4 are implemented with PMOS copiers. In addition, two bias current sources, I_{bias1} and I_{bias2}, and two reference current sources, I_{ref1} and I_{ref2}, are employed. Two pairs of comparators are used: the upper pair compares the voltage at node X when the residue current is copied to copier 3, as illustrated in Figure 3.3(a), while the lower pair compares the voltage when the residue current is copied to copier 1, as shown in Figure 3.3(c). The ADC design adopts a modified RSD conversion algorithm described below.

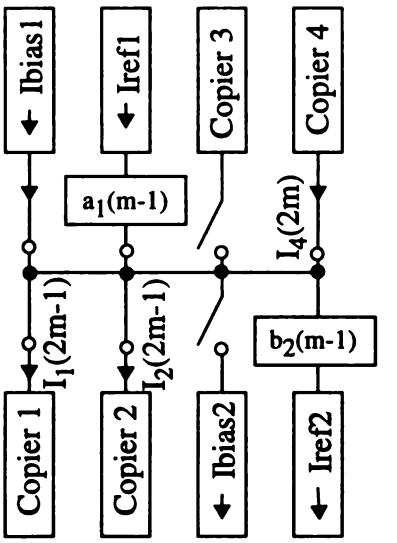
Consider the modified RSD conversion algorithm, as illustrated in Figure 2.3(c). At each bit decision, two comparison levels P and Q are used, with P positive and Q negative. If the input signal I_x is larger than P, the output code bit is set to 1 and the reference is subtracted; if I_x is smaller than Q, the output code bit is set to -1 and the reference is added; else, then the bit is set to 0 and no arithmetic operation is carried out. If the comparison takes place before the multiplication by 2, the only requirement on the comparison levels is $2P \in [0, I_{ref}]$ and $2Q \in [-I_{ref}, 0]$, as shown in Figure 3.4(a), i.e., $P \in [0, I_{ref}/2]$ and $Q \in [-I_{ref}/2, 0]$. Setting P and Q, respectively, at about $+I_{ref}/4$ and $-I_{ref}/4$, as shown in Figure 3.4(b), provides a large tolerance of $\pm I_{ref}/4$ for the comparator's inaccuracy, thus high levels of noise effect, and even hysteresis are allowed. However, the probability of having b=0 becomes only 25%, where both b=1 and b=-1 take 75%. Note that the converter circuit takes no operation when b=0. Therefore, this implementation chose $P=+I_{ref}/3$ and $Q=-I_{ref}/3$ to increase the probability of b=0 as 33%. Note that the tolerance of the comparator's inaccuracy is $\pm I_{ref}/6$ which is sufficiently large for us to comfortably design the comparator, where $I_{ref}=250\mu A$ is used in this implementation.

Let $I_{res}(m-1)$ be the residue current that determines the m-th digit, where

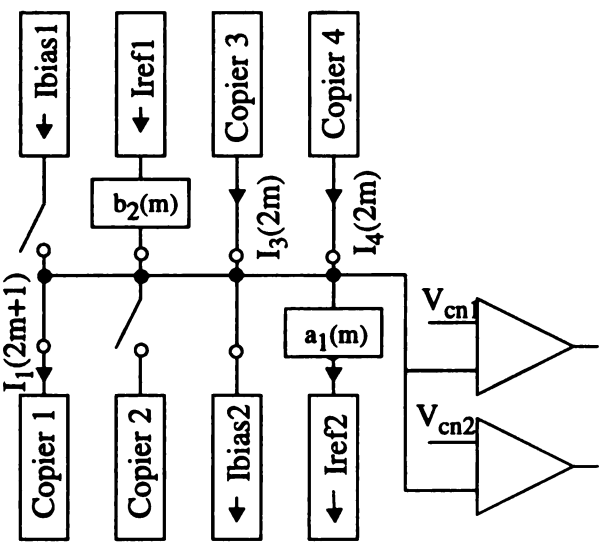
$$I_{res}(m-1)=I_1(2m-1)+I_2(2m-1)$$



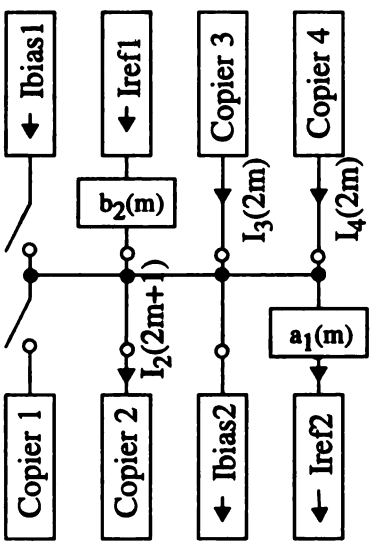
(a) $I_1+I_2 \rightarrow I_3$ and comparison



(b) $I_1+I_2 \rightarrow I_4$



(c) $I_3+I_4 \rightarrow I_1$ and comparison



(d) $I_3+I_4 \rightarrow I_2$

Figure 3.3 Bit conversion: (a)&(b) Operations for m-bit;
and (c)&(d) operations for (m+1)-bit.

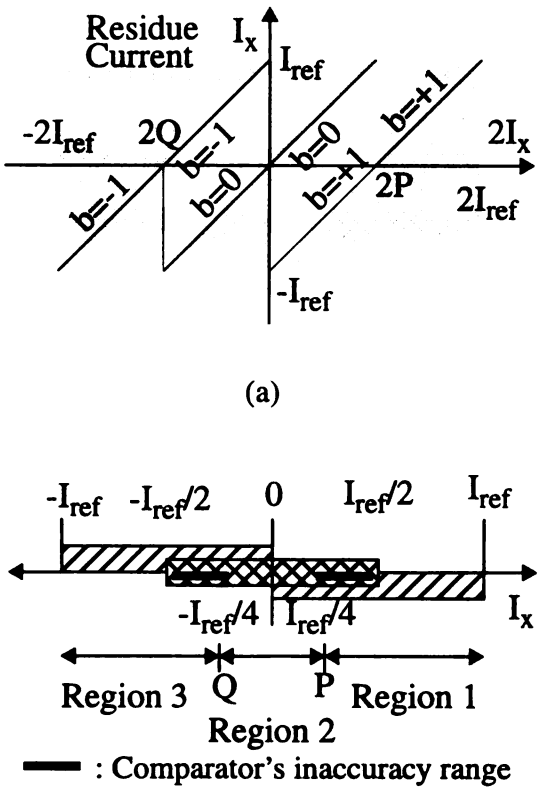


Figure 3.4 Modified RSD conversion algorithm: (a) Robertson diagram; and (b) Conversion ranges and comparison levels.

By Figures 3.3(a) and 3.3(b), the currents stored in copiers 3 and 4 are

$$I_3(2m)=I_4(2m)=\begin{cases} I_{res}(m-1) - I_{bias1} - I_{ref1} & : \text{Region 1} \\ I_{res}(m-1) - I_{bias1} & : \text{Region 2} \\ I_{res}(m-1) - I_{bias1} + I_{ref2} & : \text{Region 3} \end{cases} \quad (3.1)$$

where the convergency regions are defined as

$$D_{m-1} = \begin{cases} 1 \quad \text{if } I_{res}(m-1) > I_{bias1}+I_{ref1}/3 & : \text{Region 1} \\ 0 \quad \text{if } I_{bias1}-I_{ref1}/3 \le I_{res}(m-1) \le I_{bias1}+I_{ref1}/3 & : \text{Region 2} \\ -1 \quad \text{if } I_{bias1}-I_{ref1}/3 > I_{res}(m-1) & : \text{Region 3} \end{cases} \quad (3.2)$$

Similarly, for the (m+1)-th bit, by Figures 3.3(c) and 3.3(d) the residue current is $I_{res}(m)=I_3(2m)+ I_4(2m)$, and the currents held in Copiers 1 and 2 are

$$I_1(2m+1)=I_2(2m+1)=\begin{cases} I_{res}(m) - I_{bias2} - I_{ref2} & : \text{Region 1} \\ I_{res}(m) - I_{bias2} & : \text{Region 2} \\ I_{res}(m) - I_{bias2} + I_{ref2} & : \text{Region 3} \end{cases} \quad (3.3)$$

where the convergency regions are defined as

$$D_{m-1} = \begin{cases} 1 \quad \text{if } I_{res}(m) > I_{bias2}+I_{ref2}/3 & : \text{Region 1} \\ 0 \quad \text{if } I_{bias2}-I_{ref2}/3 \le I_{res}(m) \le I_{bias2}+I_{ref2}/3 & : \text{Region 2} \\ -1 \quad \text{if } I_{bias2}-I_{ref2}/3 > I_{res}(m) & : \text{Region 3} \end{cases} \quad (3.4)$$

The m-th converted digit D_m is encoded as <1,1>, <0,1>, <0,0> for D_m=1 (region 1), 0 (region 2), -1 (region 3), respectively. Let $b_2(m)$ be the bit complement of $a_2(m)$, i.e.,

$$b_2(m) = \begin{cases} 1 & \text{if } a_2(m)=0 \\ 0 & \text{if } a_2(m)=1 \end{cases} \quad (3.5)$$

Therefore, (3.1) and (3.3) can be respectively written as the following general form

$$I_3(2m)=I_4(2m)=I_{res}(m-1)-I_{bias1}-a_1(m-1)I_{ref1}+b_2(m-1)I_{ref2} \quad (3.6)$$

$$I_1(2m+1)=I_2(2m+1)=I_{res}(m)-I_{bias2}-a_1(m)I_{ref2}+b_2(m)I_{ref1} \quad (3.7)$$

where the residue currents are

$$I_{res}(m-1)=I_1(2m-1)+I_2(2m-1)=2I_{res}(m-2)-2I_{bias2}-2a_1(m-2)I_{ref2}+2b_2(m-2)I_{ref1} \quad (3.8)$$

$$I_{res}(m)=I_3(2m)+I_4(2m)=2I_{res}(m-1)-2I_{bias1}-2a_1(m-1)I_{ref1}+2b_2(m-1)I_{ref2} \quad (3.9)$$

It should be noted that, by (3.1) and (3.3), the stored current is with I_{ref1}, I_{ref2}, or neither. Thus, both reference currents I_{ref1} and I_{ref2} are not necessary to be well matched. However, the use of well-matched reference current sources guarantees the quality of the stored currents, i.e., $I_1=I_2$ and $I_3=I_4$, and also reduces the possible current variation in those copies. Let $I_{ref1}=I_{ref2}=I_{ref}$. Also, let $I_{bias1}=I_{bias2}=I_b$. Therefore, (3.1)-(3.4) can be summarized as follows.

Region	D_m	a_1	a_2	b_2	$I_{res}(m+1)$	Convergent Range
1	1	1	1	0	$2I_{res}(m) - I_{bias} - I_{ref}$	$I_{res}(m) > I_{bias}+I_{ref}/3$
2	0	0	1	0	$2I_{res}(m) - I_{bias}$	$I_{bias}-I_{ref}/3 \le I_{res}(m) \le I_{bias}+I_{ref}/3$
3	-1	0	0	1	$2I_{res}(m) - I_{bias} + I_{ref}$	$I_{bias}-I_{ref}/3 > I_{res}(m)$

3.2 Design Consideration

The goal of the developed ADC is to achieve low-power with low supply voltage and moderate conversion speed. There exist design tradeoffs among speed, power consumption, SNR (signal-to-noise ratio), and etc. The speed can be improved, i.e., the decrease of the settling time, by increasing the bias current at the cost of increasing power consumption. The SNR can be reduced by also increasing the bias current while keeping the same input dynamic range. On the other hand, the SNR can be increased by using a large storage capacitance.

Current copier is the basic building block of a SI circuit. The performance of the SI circuit is generally determined by the performance of the copiers it employs. The calibration speed of the copier is determined by the time constant $\tau=C/g_M$, where C is the capacitance of the storage capacitor and g_M is the transconductance of the storage transistor M. Apparently, increasing the gate capacitance results in a slow calibration speed. The questions are: *Can a copier with a large gate capacitance still be operated at a high calibration speed? how does g_{M1} affect the accuracy?* and *what are the design constraints on selecting C for keeping the time constant τ small?* The issues on selecting appropriate capacitance has been addressed and can be found in [13-16].

For low-power application, the storage capacitance should be limited by its SNR requirement and determined as follows [65-68],

$$SNR = 10 \log[V_{cn}^2(rms) / (kT/C)] \qquad (3.10)$$

where $V_{cn}(rms)$ is the tolerable noise variation across the capacitor, T is the operation absolute temperature, the Boltzmann constant $k=1.23*10^{-23}$ JK^{-1}, and C is the storage capacitance. Thus, for 12-bit resolution, i.e., SNR=74 dB, if $V_{cn}(rms)=1$ V, by (3.10), we obtain the storage capacitance C=0.093 pF, where $T=300^o$ K. Note that this implementation, $V_{cn}(rms)=0.85$ V. With a 74 dB SNR for the 12-bit ADC, the storage capacitance is approximately 0.11 pF. As mentioned, the larger capacitance can decrease noises and errors, and thus decreasing the DNL and INL.

The transistor sizes are determined by the input dynamic range and the bias current. The transistor size should be sufficiently large to operate in the saturation region so that the current can be held correctly. Note that $V_{gs}-V_T < V_{ds}$ when the transistor is operated in the saturation region. Taking the process variation into account, for purpose of safety, this im-

plementation sets the maximum voltage of $(V_{gs}-V_T)$ to be 85% of V_{ds}, i.e., $V_{gs(max)}-V_T=0.85V_{ds}$. For a power supply of 3.3V, $V_{ds}\approx 1.65V$. This implies that the maximum voltage $V_{gs(max)}-V_T=0.85V_{ds}\approx 1.4V$. In general, to keep the transistor inside the strong inversion region, we need $V_{gs(min)}-V_T=0.2V$. If the input currents are ranged from $I_{bias}-(I_{max}/2)$ to $I_{bias}+(I_{max}/2)$, then

$$[I_{bias}+(I_{max}/2)] / [I_{bias}-(I_{max}/2)] = [0.85V_{ds}/0.2]^2$$

Therefore, the transistor sizes are selected based on the selected I_{bias} and I_{max}.

3.3 Simulation Results and Measurements

The developed ADC circuit, as shown in Figure 3.2(a), employs four copiers with the current-storage transistors M_1-M_4. Both I_{ref1} and I_{bais1} are implemented with two PMOS transistors, M_{ref1} and M_{bais1}, and I_{ref2} and I_{bais2} are with two NMOS transistors, M_{ref2} and M_{bais2}. Switches S_{2n}, S_{2p}, S_{4n}, and S_{4p} are realized by CMOS switches with dummy switches to alleviate the charge-feedthrough errors, while the remaining switches are implemented with simple CMOS switches. The copiers with negative feedback structure are used to reduce the error due to channel-modulation. The digital logic circuits, realized by CMOS transistors, are used to produce the digital codes and the control signals.

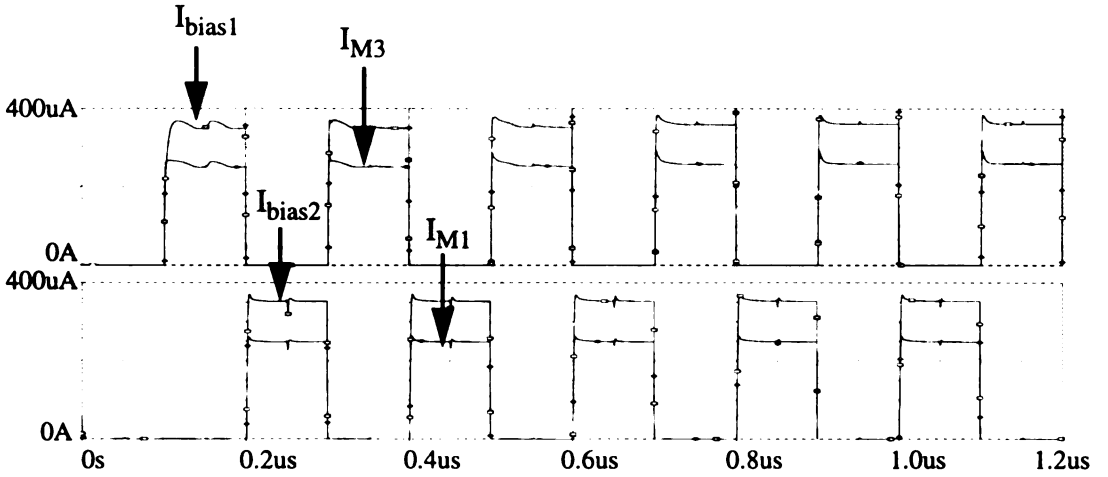
The circuit has been designed and simulated by ***pspice***, where the *SCAN20* 2μm CMOS process with level-2 transistor parameters and a supply voltage of 3.3 V are employed. The transistor sizes for both M_1 and M_2 are 36 μm/2 μm, and for both M_3 and M_4 are 80 μm/2 μm, where the transconductances of both NMOS and PMOS transistors are 780 μA/V and 730 μA/V, respectively. All capacitances are 0.2 pF. The reference and biased current are chosen as $I_{ref}=I_{ref1}=I_{ref2}=250$ μA and $I_{bias}=I_{bias1}=I_{bias2}=350$ μA. The

bias voltage for the feedback amplifier is V_{bias}=1.65 V. In the comparators, V_{cp1}=1.813 V, V_{cp2}=1.6 V, V_{cn1}=1.46V, and V_{cn2}=1.689 V were chosen. The chip layout has been generated by L-edit and simulated by ***pspice***. Simulation results show that the current storage transistor can be converged within 30 ns. However, a clock rate of 50 ns is chosen for this ADC simulation.

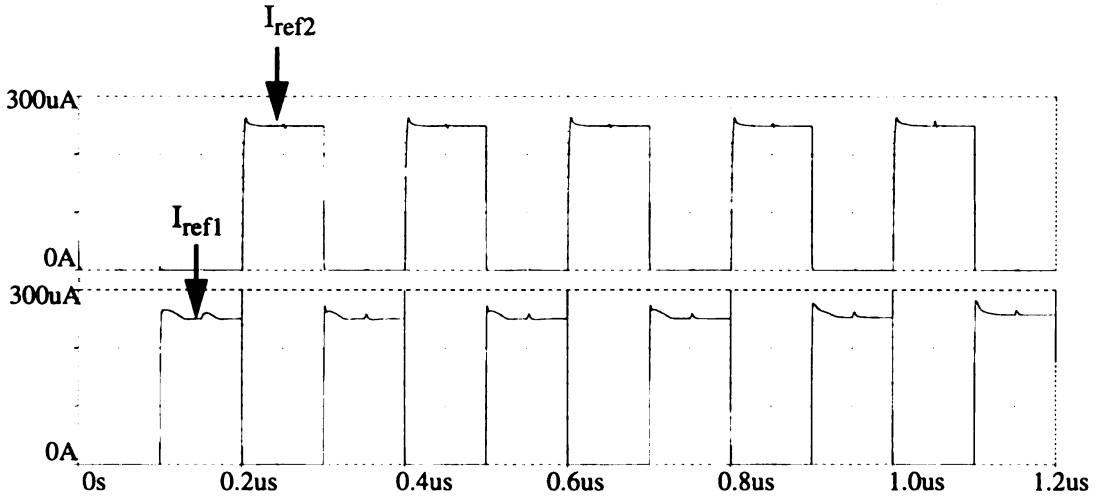
Figure 3.5(a) shows a typical current waveform in a current-storage transistor, where Figure 3.5(b) plots the partial output of I_{ref1} to demonstrate the three states in the RSD approach. Since the clock rate for calibration is 50 ns, one state is obtained in every 100 ns. Figure 3.5(c) summarizes the accuracy of the proposed ADC which achieves a 12-bit resolution for the input currents ranged between 100 μA and 600 μA. The power dissipation is approximately 1.9 mW.

It should be mentioned that the effects on mismatched reference currents, i.e., $I_{ref1} \neq I_{ref2}$, and loop offsets errors, have been studied. The proposed ADC will keep the same accuracy and the lower limit of the dynamic range. However, the upper limit of dynamic range decreases as the error effects. More specifically, if both currents I_{ref1} and I_{ref2} are off r% from I_{ref}, or the loop offset error increases r%, the upper limit of the dynamic range will be reduced approximately (r/2)%.

Figures 3.6(a) and 3.6(b) show the layout of the designed chip and the die photo of the fabricated chip, respectively. The ADC is fabricated by MOSIS with the SCNA20 2μm N-well CMOS process, where the threshold voltages for the NMOS and PMOS are 0.83V and 0.99V, respectively. The test chip does not use the double-poly linear capacitor, i.e., it is fabricated by a digital CMOS process. The 40-pin test chip is comprised of three major parts: analog portion, digital portion, and clock/pulse generator portion. The analog por-

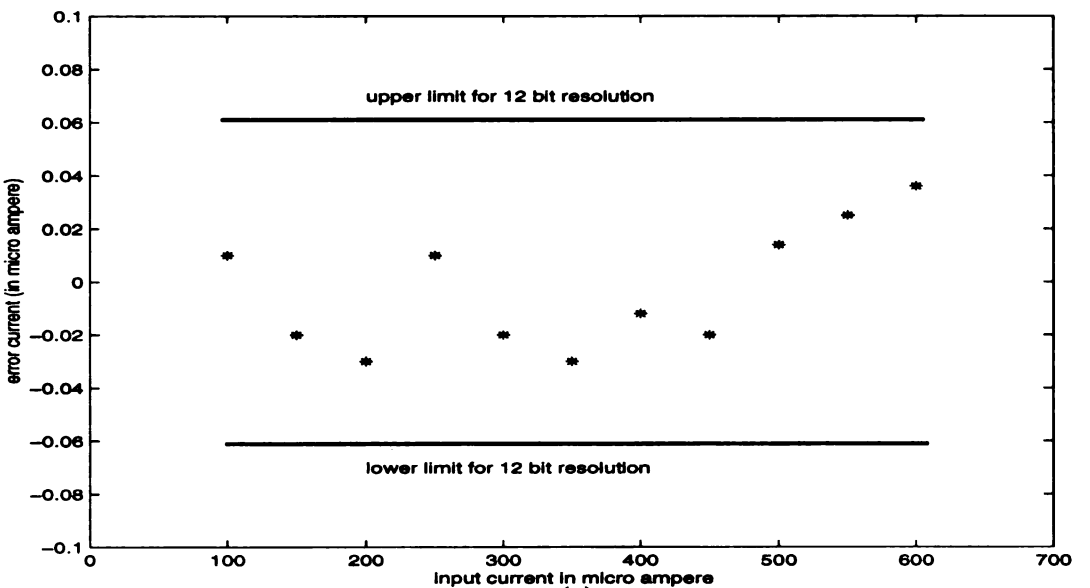


(a)



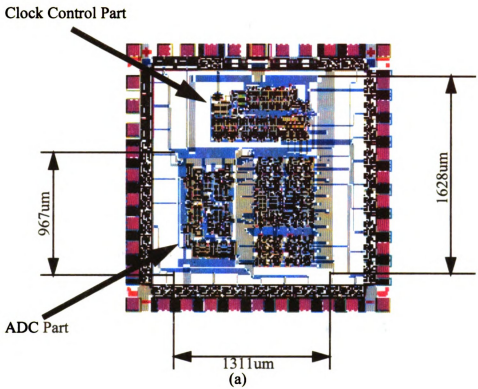
(b)

Figure 3.5 Simulation results: (a) typical current in a current-storage transistor; (b) partial outputs of Iref1; and (c) 12-bit resolution.

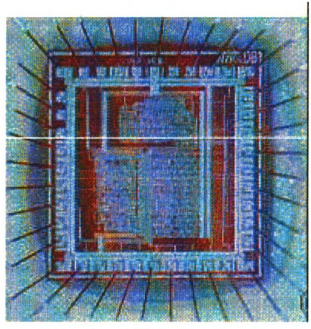


(c)

Figure 3.5 (cont'd)



(a)



(b)

Figure 3.6 Implementation: (a) The layout of the designed ADC; (b) the die photo of the fabricated ADC

tion is approximately (0.967*0.42)=0.41 mm^2, the digital portion is about (0.967*0.52)=0.50 mm^2, and the clock/pulse generator is nearly (0.6*0.31)=0.186 mm^2. The total active area of the fabricated chip is (1.628*1.311)=2.13 mm^2.

To measure the test chip, a voltage-to-current (V-I) converter, as shown in Figure 3.7 [30], and voltage sources are used to generate the input current signals, where the voltage source for the V-I converter is 5 V. A 24.4 kHz sine wave is applied to the test chip at a 0.8 Msamples per second conversion rate with a 3.3 V supply voltage to measure the linearity of the test chip. The total of 102,400 test data are collected to process the DNL and INL measurements. Figures 3.8(a) and 3.8(b) show the resultant DNL and INL, respectively, where the maximum DNL and INL are 0.6 LSB and 0.5 LSB, respectively. The linearity plots for 12-bit resolution show that the converter may potentially achieve 12-bit or more resolution.

More specifically, as discussed in Section 3.2, for 12-bit converter, the required SNR is set to 74 dB. For V_{cn}(rms)=0.85 V, the theoretical value of the storage capacitance is 0.11 pF to keep both DNL and INL within 0.5 LSB. In this implementation, the capacitances are all 0.2 pF for conservative design which will have about 77 dB theoretically. Note that the use of larger storage capacitance can decrease both DNL and INL. In addition, since the converter adopts the RSD correction scheme, the use of smaller capacitance can still achieve the desired DNL and INL. Therefore, with the RSD scheme and the use of larger storage capacitor, the converter achieves very small DNL and INL. If the design limits both DNL and INL to be within 1 LSB, the converter can have the potential to achieve a 13-bit resolution. However, since the clock generator in the test chip was designed for 12-bit resolution, the converter resolution is set to 12 bits.

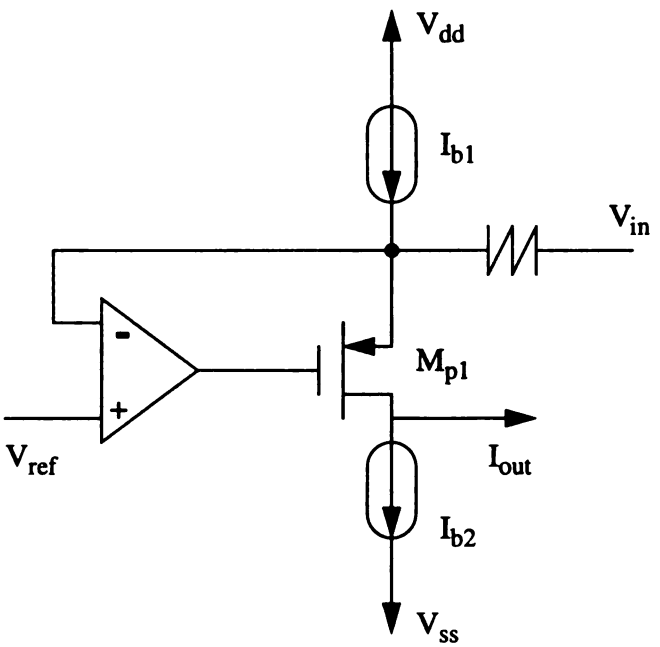
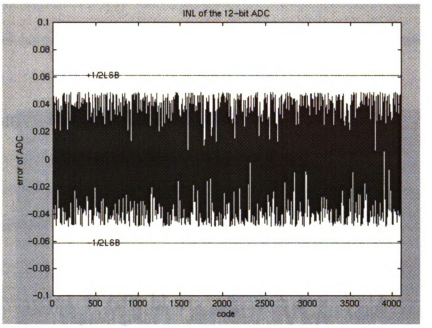
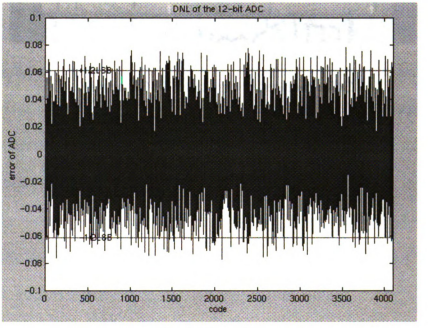


Figure 3.7 Schematic circuit of voltage-to-current converter



(a)



(b)

Figure 3.8 Analysis of nolinearity: (a) The INL of designed ADC; and (b) The DNL of designed ADC

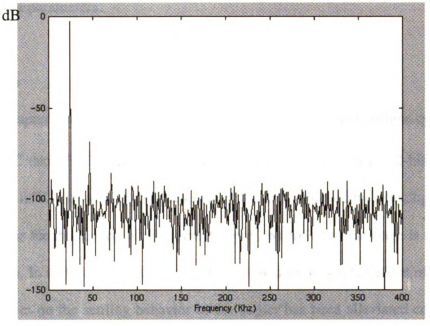


Figure 3.9 FFT analysis of designed ADC

Figure 3.9 shows the measured fast Fourier transform (FFT) spectrum of the test chip. The input signal 24.4 kHz was applied and 24,576 test data were collected to analyze. The total harmonic distortion (THD) is -66.7 dB and the signal-to-noise/distortion ratio (SNDR) is 65 dB which is about 9 dB less than the ideal value. Table 4.1 summarizes the performance parameters.

3.4 Conclusion

This chapter presents a high-performance CMOS switched-current cyclic ADC, where the ADC takes 2.13 mm^2 in chip area, achieves a resolution of 12-bits, and consumes only 1.9 mW in power. High-speed performance is achieved by reducing the amplifier stages in the feedback loop of the current copier, where only one stage is used in this implementation. In addition, with the carefully designed switches, the effect of their parasitic capacitances on the settling behavior of the copier has been alleviated considerably. Finally, the residue amplifier requires only two clock cycles and does not require the well-matched reference currents. The converter has been designed, simulated, fabricated, and tested. Experimental results endorse that the developed converter can be used for low-power/low-voltage mixed-signal circuits.

With the successful development of the high performance and low power CMOS SI ADC circuits, the next logical step is to develop high performance and low power CMOS SI ADC circuits which will be discussed in the next chapter.

Table 3.1 The summarized performance of ADC

	Parameter Values
Technology	2 μm N-well CMOS
Resolution	12 bits
Conversion Rate	800 KSample/s
Full Scale Current	500 μA
DNL	-0.6 ~ 0.6 LSB
INL	-0.45 ~ 0.45 LSB
SNDR	65 dB
THD	-66.7 dB
Power Supply	Single 3.3 V
Active Area	2.13 mm^2
Power Consumption	1.9 mW

Chapter 4

CMOS SI DAC CIRCUIT DESIGN

This chapter presents the design methodology and performance analysis of a high performance and low power SI CMOS DAC circuit [69,70]. As discussed in Section 2.2, the current reference generator (CRG) circuit is realized by ratioed currents as illustrated in Figure 2.5(b). This study presents the CRG circuit design using SI technique without the need of well-matched components. The CRG circuit can be designed using the MC approach, referred to as a CRG_MC circuit, or using the DC approach, referred to as a CRG_DC circuit. Section 4.1 presents the design and operation of both CRG_MC and CRG_DC circuits and the developed design methodology and performance analysis process. In order to demonstrate the design methodology, Section 4.2 shows some design examples. Section 4.3 disucsses the design limitations of the DAC circuit design using both approaches for low power applications, and presents the developed DAC circuits. Finally, a concluding remark for SI DAC circuit design is given in Section 4.4.

4.1 Current Reference Generator (CRG) Circuits

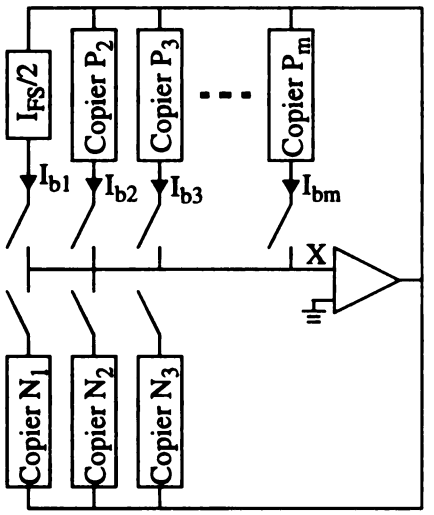
This section presents the design and operation of CRG_DC and CRG_MC circuits. For high performance and low power design, a design methodology is developed and the performance analysis process is also developed. The design methodology provides the se-

lection of the sizes for storage transistors and capacitors based on a given set of design specifications including input dynamic range, full-scale current, SNR, power consumption, etc., and the performance analysis estimates the calibration time, holding time, and accuracy of the CRG circuits.

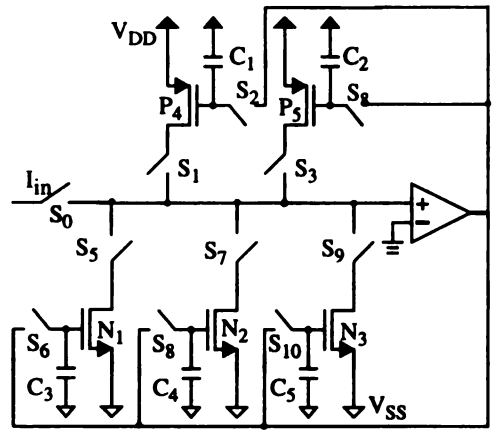
A CRG circuit generates multiple current references for data conversion. Its calibration time is defined as the time required to generate all current references. Since the generated current references are held in current copiers, the held currents will leak out as time progresses. The holding time is defined as the time for the circuit leaks a current which is 0.01% of the originally generated current. Finally, due to the charge injection error of the current copiers, error currents are accumulated when all current references are generated, and the accumulated error currents determine the accuracy of the CRG circuit.

4.1.1 CRG_DC Circuits

Figure 4.1(a) shows the block diagram of an m-bit CRG_DC circuit which is generalized from a basic divide-by-two (DB2) circuit in Figure 4.1(b) [71]. The DB2 circuit is comprised of three NMOS current copiers with N_1, N_2, and N_3, two PMOS current copiers with P_1 and P_2, and an op-amp. Basically, the DB2 circuit takes three clock cycles to obtain half the input current if both transistors N_2 and N_3 are perfectly matched. As mentioned in Chapter 2, a number of iterations, three clock cycles per iteration, may be needed if there exists a mismatch between N_2 and N_3. This subsection discusses the development of DB2 circuit and then presents the design and operation of CRG_DC circuits.



(a)

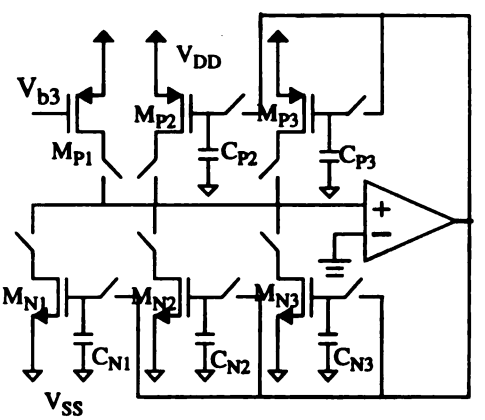


(b)

	Copying Sequence (Iterations 1 to k-1)		
D1	$I_{FS}/2=I_{MSB}$		
D2	$I_{b1} \rightarrow N_2$ & N_3	I_{b1} & $N_3 \rightarrow N_1$	N_1 & $N_2 \rightarrow P_2$
D3	$P_2 \rightarrow N_2$ & N_3	P_2 & $N_3 \rightarrow N_1$	N_1 & $N_2 \rightarrow P_3$
Dm	$P_{m-1} \rightarrow N_2$&N_3	P_{m-1}&$N_3 \rightarrow N_1$	N_1 & $N_2 \rightarrow P_m$

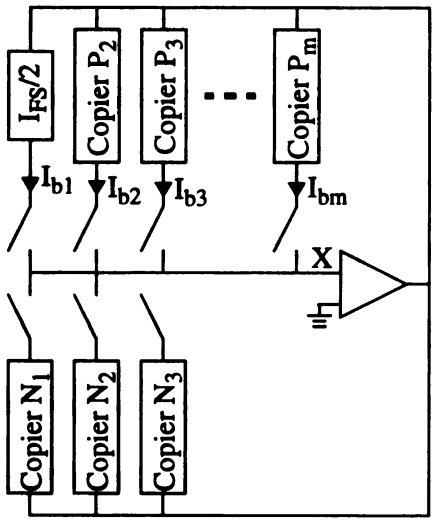
	Copying Sequence (k-th iteration)			I_{bi}
D1'	$I_{b1} \rightarrow N_1$	$N_1 \rightarrow P_2$		$I_{FS}/2$
D2'	$I_{b1} \rightarrow N_2$ & N_3	$N_3 \rightarrow P_2$	$N_3 \rightarrow P_3$	$I_{FS}/2^2$
D3'	$P_2 \rightarrow N_2$ & N_3	$N_3 \rightarrow P_3$	$N_3 \rightarrow P_4$	$I_{FS}/2^3$
Dm'	$P_{m-1} \rightarrow N_2$&N_3	$N_3 \rightarrow P_m$		$I_{FS}/2^N$

(c)

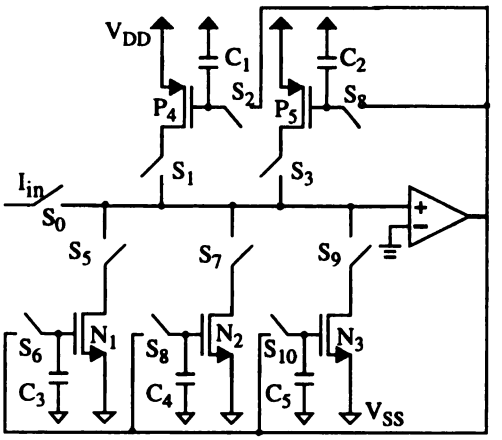


(d)

Figure 4.1 CRG_DC circuit: (a) block diagram; (b) divide-by-two (DB2) Circuit; (c) current copying sequence; and (d) a 3-bit CRG_DC circuit.



(a)

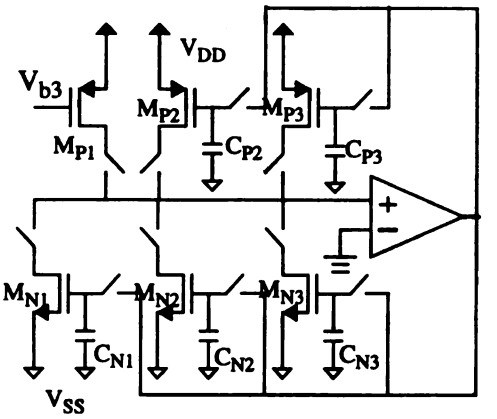


(b)

	Copying Sequence (Iterations 1 to k-1)		
D1	$I_{FS}/2=I_{MSB}$		
D2	$I_{b1} \rightarrow N_2$ & N_3	I_{b1} & $N_3 \rightarrow N_1$	N_1 & $N_2 \rightarrow P_2$
D3	$P_2 \rightarrow N_2$ & N_3	P_2 & $N_3 \rightarrow N_1$	N_1 & $N_2 \rightarrow P_3$
Dm	$P_{m-1} \rightarrow N_2$&N_3	P_{m-1}&$N_3 \rightarrow N_1$	N_1 & $N_2 \rightarrow P_m$

	Copying Sequence (k-th iteration)			I_{bi}
D1'	$I_{b1} \rightarrow N_1$	$N_1 \rightarrow P_2$		$I_{FS}/2$
D2'	$I_{b1} \rightarrow N_2$ & N_3	$N_3 \rightarrow P_2$	$N_3 \rightarrow P_3$	$I_{FS}/2^2$
D3'	$P_2 \rightarrow N_2$ & N_3	$N_3 \rightarrow P_3$	$N_3 \rightarrow P_4$	$I_{FS}/2^3$
Dm'	$P_{m-1} \rightarrow N_2$&N_3	$N_3 \rightarrow P_m$		$I_{FS}/2^N$

(c)



(d)

Figure 4.1 CRG_DC circuit: (a) block diagram; (b) divide-by-two (DB2) Circuit; (c) current copying sequence; and (d) a 3-bit CRG_DC circuit.

4.1.1.1 Divide-by-Two (DB2) Circuit

Consider the DB2 in Figure 2.2(b). Based on the copying sequence in (a1-c1) and (A1-C1), the circuit requires that $I_2 > I_3$ in order for the current copier to properly memorize the current difference. In this study, an alternative DB2 circuit with an alternaitve copy sequence is developed. Mor especifically, in the copying sequence (A1), the sum current of I_{in} and I_1 is stored into the copiers with N_2 and N_3, where, by (b1) and (c1), $I_1=I_2-I_3$. Therefore, the sum current can be expressed as $I_{in}+I_1=I_{in}+(I_2-I_3)$. It can also be expressed as $I_{in}+I_1=(I_{in}-I_3)+I_2$. Since I_{in} is always greater than N_3, the difference current $(I_{in}-I_3)$ can be stored in the NMOS copier with N_1. The divider circuit functions properly regardless of the mismatch. Note that the resultant current is held in the copier with N_3.

The following copying sequences can be used for the DB2 circuit in Figure 2.2(b)

(a2) $I_{in} \rightarrow N_2 \,\&\, N_3$ (A2) $P_4 \rightarrow N_2 \,\&\, N_3$

(b2) $I_{in} \,\&\, N_3 \rightarrow N_1$ (B2) $I_{in} \,\&\, N_3 \rightarrow N_1$

(c2) $N_1 \,\&\, N_2 \rightarrow P_4$ (C2) $N_1 \,\&\, N_2 \rightarrow P_4$

However, the input current needs to be available for many cycles, i.e., (a2), (b2), and (B2). Figure 4.1(b) illustrates the developed DB2 circuit, where an additional current copier with P_5 is employed to store the input current. Thus, the input current is sampled and held only once. The circuit implements the following switching sequence

(a3) $I_{in} \rightarrow N_1$ (A3) $P_4 \rightarrow N_2 \,\&\, N_3$

(b3) $N_1 \rightarrow P_4$ (B3) $P_5 \,\&\, N_3 \rightarrow N_1$

(c3) $N_1 \rightarrow P_5$ (C3) $N_1 \,\&\, N_2 \rightarrow P_4$

where (a3)-(c3) are for the preparation cycles, while (A3)-(B3) are for the conversion cycles.

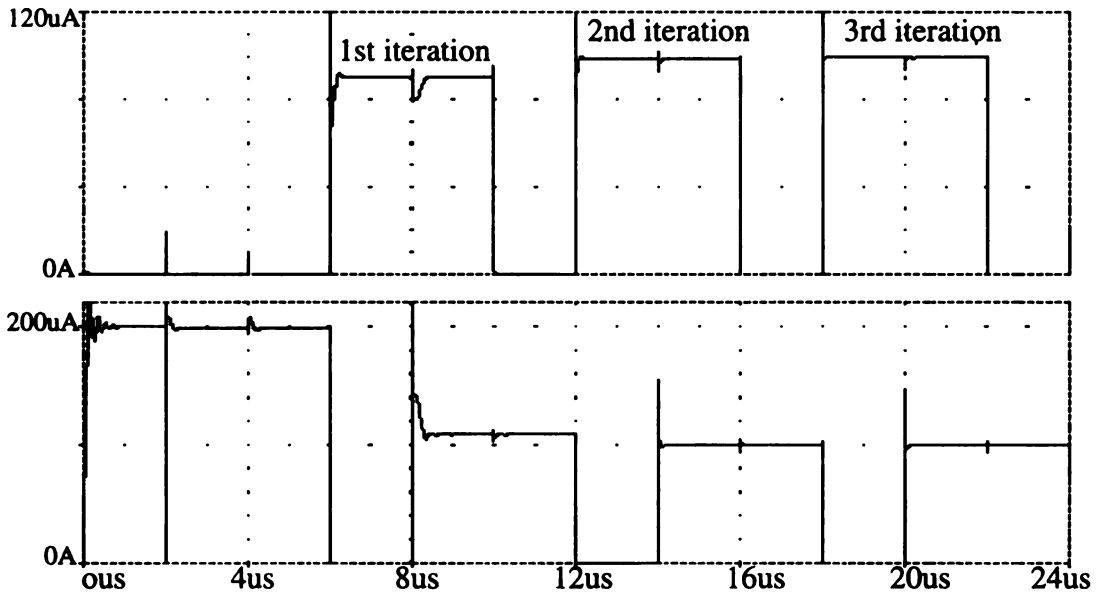
Figure 4.2(a) shows the ***pspice*** simulation results of theDB2 circuit with an input current 200μA, where *MOSIS SCNA20* 2μm process technology and 3.3V supply voltage were assumed., $C_1=C_2=C_3=C_4=C_5=8pF$, $(W/L)_4=(W/L)_5=152/2$, $(W/L)_1=(W/L)_3=71/2$, and $(W/L)_2=85.2/2$ are simualted. Note that the mismatch ratio between N_2 and M_3 is 20%. The figure shows the 3 cycles of the resultant currents I_2 and I_3. Results show that the DB2 circuit can reach 12-bit accuracy after 3 iterations.

Theoretically speaking, for a given mismatch ratio, the accuracy can be improved as the number of iterations increases. In practice however, errors may be accumulated in every cycle of the division process. As mentioned, a basic current copier suffers from two major error effects: due to non-zero output conductance and clock feedthrough. Consider the current copier with N_1 in Figure 5.1(b), a clock feedthrough error occurs when switch S_6 is opened. Additional charges will be dumped into the holding capacitor C_3. The dumped charges from a CMOS switch can be expressed as

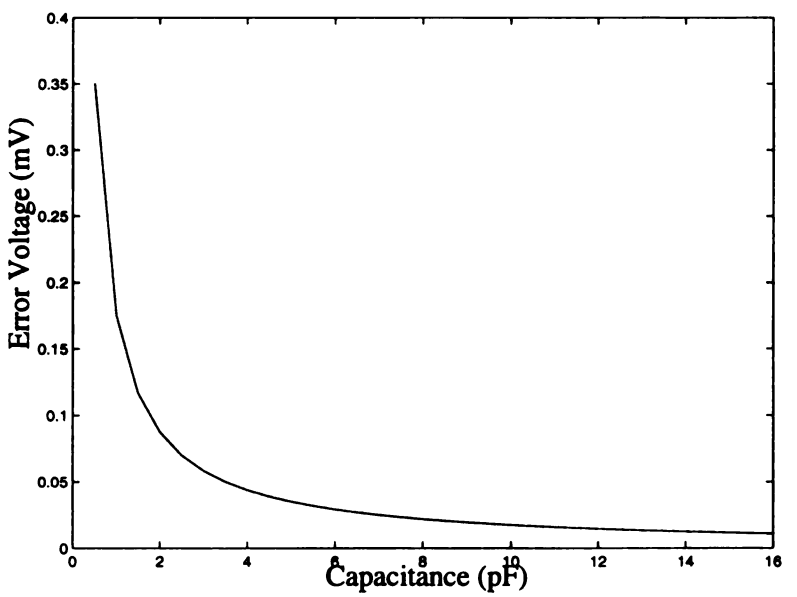
$$\Delta Q = |Q_{OLN} - Q_{OLP}| = C_{ox}*|L_{DN}-L_{DP}|*W*(V_H-V_L) \qquad (4.1)$$

where Q_{OLN} (Q_{OLP}) is the overlap capacitance charge in N- (P-) transistor, L_{DN} (L_{DP}) is the lateral diffusion, C_{ox} is the gate oxide capacitance, W is the channel width of the transistor for S_3, and V_H and V_L are the high- and low-level of the clock for the switch.

Figure 4.2(b) plots the voltage errors on the holding capacitor for various capacitances. It shows that the voltage error decreases significantly as the capacitance increases. (Note that the speed performance degrades as the capacitance increases.) The resultant error current can be expressed as $\Delta I=g_m*\Delta Q/C$, where g_m is the transconductance of the storage transistor. For an input current 100μA, the error current is 0.12μA, where C=1pF and g_m=600μA/V. This means that the maximum accuracy of the copier is 9-bit,

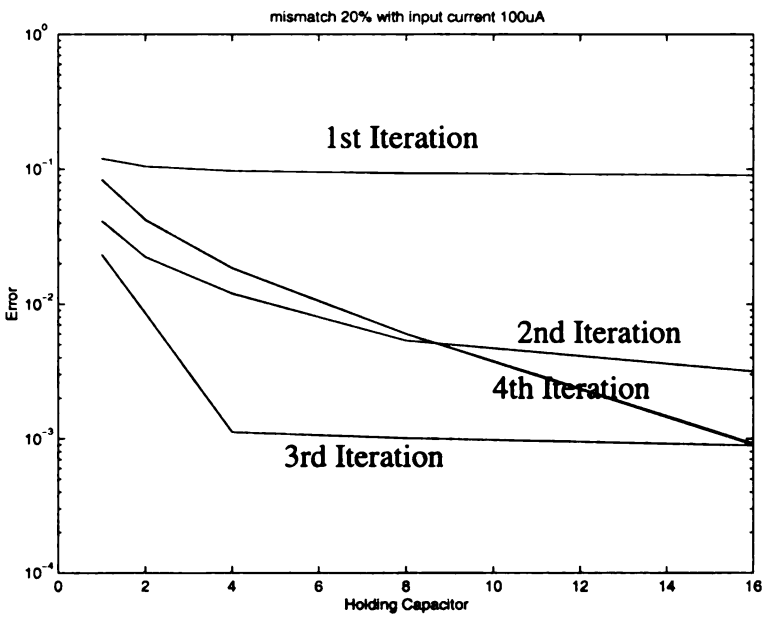


(a)



(b)

Figure 4.2 DB2 circuit analysis: (a) Simulation of DB2 circuit; (b) charge-injection errors on the holding capacitor; (c) accumulated errors for various iterations



(c)

Figure 4.2 (cont'd)

and thus limiting the number of iterations required for the divider circuit.

Taking the clock-feedthrough error effects into consideration, Figure 4.2(c) plots the simulation results for the percentages of the accumulated error current in each iteration for various capacitances, where the input current is 100μA and a 20% mismatch was assumed. Results show that the best accuracy is reached at the third iteration. The accuracy is getting worse in the 4th iteration because the accumulated errors dominate. Results also show that, in the 3rd iteration, the accuracy is no longer improved as the capacitance is up to 4 pF.

4.1.1.2 m-bit CRG_DC Circuit

Based on the DB2 circuit, an m-bit CRG_DC circuit is comprised of 3 NMOS current copiers with N_1, N_2, and N_3, one current source with $I_{FS}/2$, and (m-1) PMOS current copiers with P_2, .., P_m. The copying sequence for the m-bit RG circuit is listed in Figure 4.1(c), where the sequence (Di) is for the first (k-1) iteration of the i-th bit division, while the sequence (Di') is for the k-th iteration. Figure 4.1(d) shows a 3-bit CRG_DC circuit. For an m-bit RG circuit with k iterations, generating the first bit takes 2 cycles, the last bit needs 3(k-1)+2 cycles, and the remaining bit requires 3k cycles. Therefore, the total number of cycles is

$$\kappa_{DC} = 2 + (3k)(m-2) + 3(k-1)+2 = 3k(m-1) + 1 \qquad (4.2)$$

The generated current references are held in the current copiers with P_i's, i=1,2,..,m.

It should be mentioned that the PMOS copiers in the CRG_DC circuit are realized in slightly different way as those in the DB2 circuit. More specifically, the DB2 circuit employs the PMOS and NMOS switches for the PMOS and NMOS copiers, respectively,

while the CRG_DC circuit employs all CMOS switches to alleviate the charge injection error effect. In order to further reduce the charge injection error effect, the storage capacitors in the PMOS copiers of the CRG_DC circuit are connected to V_{SS} instead of V_{DD} in Figure 4.2(b). The same PMOS copiers will be also used for the CRG_MC circuits.

4.1.2 CRG_MC Circuit

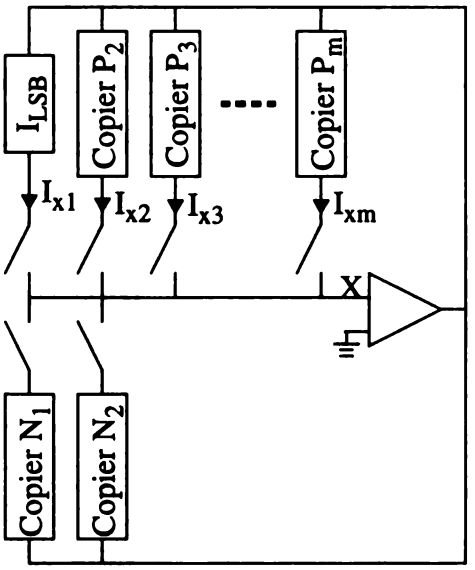
Figure 4.3(a) shows an m-bit CRG_MC circuit that produces $I_{xk}=2^{k-1}I_{LSB}$, k=1,2,..,m. The circuit is generalized from a basic multiply-by-two (MX2) circuit, as shown in Figure 2.2(a). Given a current I_{LSB}, the MX2 circuit accurately generates the doubled current $2I_{LSB}$. The circuit may take the generated current $2I_{LSB}$ as its input and again generate the doubled current of $2I_{LSB}$, i.e., 2^2I_{LSB}. The process can be repeatedly applied to generate the current references $I_{xk}=2^{k-1}I_{LSB}$, k=1,2,..,m. The m-bit CRG_MC in Figure 4.3(a) is realized by 2 NMOS current copiers, one current source with I_{LSB}, and (m-1) PMOS current copiers. Figure 4.3(b) shows the copying sequence. Therefore, the total number of cycles required for an m-bit CRG_MC circuit is

$$\kappa_{MC} = 3(m-1) \tag{4.3}$$

The generated current references are held in the PMOS current copiers.

For low power applications, the LSB current is generally very small and thus a bias current is needed for the copiers to function properly [14,15]. Figure 4.3(c) illustrates the realization of a 7-bit CRG_MC circuit. Instead of using $I_{x1}=I_{LSB}$, we set $I_{x1}=I_{LSB}+I_{bias\_2}$. The current reference I_{x2} is generated by the following copying sequence

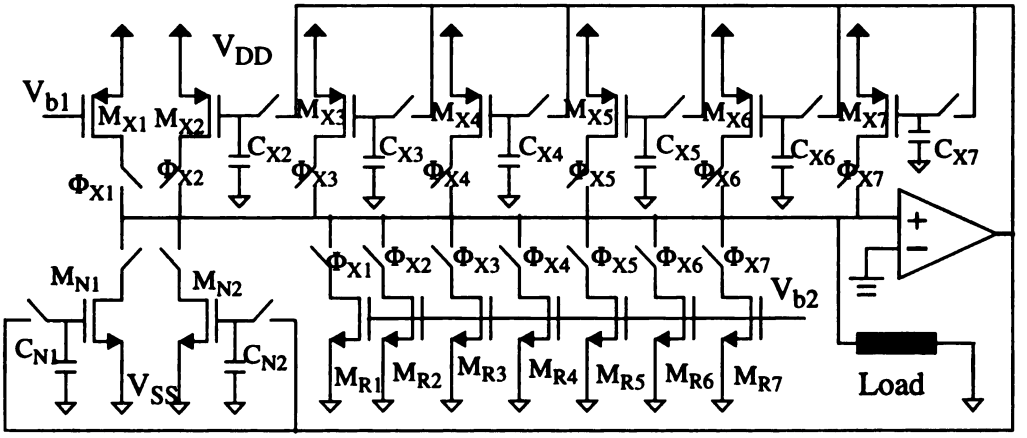
$$I_{x1} \rightarrow M_{N1};\quad I_{x1} \rightarrow M_{N2};\quad M_{N1}+M_{N2}-I_{bias\_2} \rightarrow M_{x2}.$$



(a)

	Copying Sequence		
M1			
M2	$I_{x1} \rightarrow N_1$	$I_{x1} \rightarrow N_2$	N_1 & $N_2 \rightarrow P_2$
M3	$P_2 \rightarrow N_1$	$P_2 \rightarrow N_2$	N_1 & $N_2 \rightarrow P_3$
Mm	$P_{m-1} \rightarrow N_1$	$P_{m-1} \rightarrow N_2$	N_1 & $N_2 \rightarrow P_m$

(b)



(c)

Figure 4.3 CRG_MC: (a) Block Diagram; (b) Copying Sequence; and (c) 7-bit CRG_MC.

At the end of the multiplying cycle, the current copier with M_{x2} holds a current of $(2I_{LSB}+I_{bias\_2})$, i.e., $I_{x2}+I_{bias\_2}$. When the current reference I_{x2} is read, the current held in the copier with M_{x2} and the bias current I_{bias_2} are sunk simultaneously, i.e., $I_{out}=(I_{x2}+I_{bias\_2})-I_{bias\_2}=I_{x2}$. Similarly, the current references I_{xi}'s, i=3,..,7, are generated by the following copying sequences,

$$I_{x,i-1} \rightarrow M_{N1};\quad I_{x,i-1} \rightarrow M_{N2};\quad M_{N1}+M_{N2}-I_{bias\_i} \rightarrow M_{x,i-1}.$$

where the copier with M_{xi} holds the current $(I_{xi}+I_{bias\_i})$, $I_{xi}=2I_{x,i-1}$, I_{bias_i} is the bias current associated with the I_{xi}, and the clock signals Φ_{xi}'s are shown in Figure 4.3(c). This results that each pair (M_{xi},M_{Ri}) together with I_{bias_i} produces the current reference I_{xi}. The use of the 7 bias currents allows the generated current references to be used simultaneously. For design simplicity, the bias currents I_{bias_i} are generated by the transistors M_{Ri} with the same biased voltage V_{b2}. Since the bias currents will be cancelled out during the operation, there exist no transistor mismatch problem in such an implementation. Additional transistor M_{R1} is needed for $I_{x1}=I_{LSB}+I_{bias\_2}$ to produce the bias current I_{bias_2}.

4.1.3. Design Methodology

In an m-bit CRG_DC, the current references $I_{bk}=I_{FS}/2^k$, k=1,2,..,m, are stored in the storage transistor M_{Pk}. As the copy sequence (D1') in Figure 4.1(c), the current $I_{b1}=I_{FS}/2$, the largest current references, is copied to N_1, and thus the transistor size of N_1 must be sufficiently large to operate in the saturation region so that I_{b1} can be held correctly. Taking the process variation into account, for purpose of safety, this implementation sets the maximum voltage $(V_{gs}-V_T)_{max}=0.85V_{ds}$. Therefore, the transistor size of N_1 is chosen as $I_{b1}=(k_n/2)(W/L)_{N1}(0.85V_{ds})^2 \approx (0.98k_n)(W/L)_{N1}$, or

$$(W/L)_{N1}=I_{b1}/0.98k_n \tag{4.4}$$

where k_n is the transconductance parameter of the NMOS transistor. Similarly, from the copy sequence (D2), both N_2 and N_3 must be able to hold the current $I_{b1}/2$. Thus, we need

$$(W/L)_{N2}= (W/L)_{N3}\approx(1/2)(W/L)_{N1} \tag{4.5}$$

The size in the PMOS transistors are selected in the same way. The size $(W/L)_{P1}$ of M_{P1} is chosen to generate the current I_{b1}, and $(W/L)_{P2}= (W/L)_{P1}$ because the transistor M_{P2} should be sufficient enough to hold I_{b1} in (D1'). Since M_{P3} needs to store the current $I_{b2}=I_{b1}/2$ at the end of (D2'), $(W/L)_{P3}\approx(1/2)\ (W/L)_{P2}$. Thus, the transistor sizes are chosen as

$$(W/L)_{P,k+1}\approx(1/2)\ (W/L)_{Pk},\ k=2,3,..,m-1 \tag{4.6}$$

In an m-bit CRG_MC circuit, the current references $I_{xk}=2^{k-1}I_{LSB}$, k=1,2,..,m, are stored in M_{xk}. As the sequence M_2 shown in Figure 4.3(c), I_{x1} is the minimum current stored in the copier with N_1. A typical value of $(V_{gs}-V_T)_{min}$ is 0.2V which keeps the transistor in the strong inversion region. Therefore, similar to (5.6), the transistor size for both N_1 and N_2 are chosen with

$$(W/L)_{N1}= (W/L)_{N2}=I_{x1}/(0.02k_n) \tag{4.7}$$

At the end of k's cycles, the PMOS transistor M_{xk} holds a current $I_{bias}+2I_{x,k-1}$, while the NMOS transistor M_{N1} holds a current $I_{bias}+I_{x,k-1}$. If we ignore the channel modulation effect, the currents held in M_{xk} and M_{N1} can be respectively expressed as $(k_p/2)(W/L)_{xk}(V_{DD}-V_{gp}-V_{Tp})^2$ and $(k_n/2)(W/L)_{N1}(V_{gn}-V_{SS}-V_{Tn})^2$, where V_{gn} (V_{gp}), V_{Tn} (V_{Tp}), k_n (k_p), and $(W/L)_{N1}$ [$(W/L)_{xk}$] are the gate voltage, threshold voltage, transconductance, and aspect ratio of the transistor M_{N1} (M_{xk}), respectively. Thus, the size $(W/L)_{xk}$ can be estimated

as follows

$$(W/L)_{xk} = k_{pn}V_{pn}(W/L)_{N1}[(I_{bias}+2I_{x,k-1})/(I_{bias}+I_{x,k-1})] \quad (4.8)$$

where $k_{pn}=k_n/k_p$ and $V_{pn}=[(V_{gn}-V_{SS}-V_{Tn})/(V_{DD}-V_{gp}-V_{Tp})]^2$. It is reasonable to assume that the charges dumped into the storage capacitors of both NMOS and PMOS copiers are the same if both copiers have the same gate voltage. The error current due to the charge injection effect must be considered. The current variation can be expressed as $\Delta I=gm*\Delta V=gm*\Delta Q/C$, where ΔV is the voltage variation across the holding capacitor, g_m is the transconductance of the storage transistor, and ΔQ is additional charge dumped into the holding capacitor [71]. Therefore, the total charge injection error current for both current copiers with N_1 and N_2 is approximately $2gm_{N1}*\Delta Q/C_{N1}$, where $C_{N1}=C_{N2}$ and $gm_{N1}=gm_{N2}$. If we make both gate voltages for both NMOS and PMOS copiers to be equal, i.e., $V_{gn}=V_{gp}=V_g$ and $2gm_{N1}*\Delta Q/C_{N1}=gm_{X2}*\Delta Q/C_{X2}$, or $C_{X2}=(gm_{X2}/2gm_{N1})C_{N1}$, then the charge injection errors may be compensated and thus reducing the error currents. Since the currents held in both copiers with N_1 and N_2 are copied to the PMOS copier with M_{xk}, similar to the above derivation, the capacitance C_{xk} is set to

$$C_{xk} = (gm_{xk}/2gm_{N1})C_{N1} \quad (4.9)$$

Since the dividing approach requires more cycles to obtain the current references with the desired accuracy, the charge injection errors are generally higher than that with multiplying approach. Our goal is to develop a CRG_DC which achieves about 11-bit resolution. Therefore, large capacitors are employed to alleviate the charge injection errors. A typical capacitance is 1 pF.

4.1.4. Performance Analysis

Calibration Time: Based on the transfer function of the small-signal equivalent circuit of a current copier in Figure 4.4. The following estimation of calibration time and holding time can be applied for both CRG_DC and CRG_MC circuits. As the input current decreases, the capacitance C_{gd} becomes very important because the gain for MOS increases and the Miller effect may affect the whole system. The characteristic function can be expressed as

$$\alpha s^2 + \beta s + \eta = 0 \tag{4.10}$$

where

$$\alpha = [(C_{gd} + C_{gs})C_d + C_{gd}C_{gs}]\left(\frac{1}{r_s} + \frac{1}{r_o}\right) \tag{4.11}$$

$$\beta = C_{gd}\left(\frac{1}{r_{ds}} + gm\right)\left(\frac{1}{r_s} + \frac{1}{r_o}\right) + \frac{C_{gd} + C_d}{r_s r_o} + \frac{C_{gs}}{r_s r_{ds}} - \frac{C_{gd}}{r_s} gm_a \tag{4.12}$$

$$\eta = \frac{1}{r_s r_o r_{ds}} + \frac{1}{r_s} gm gm_a \tag{4.13}$$

Since all three structures have the second order characteristic equation

$$s^2 + 2\zeta\omega_n s + \omega_n^2 = 0 \tag{4.14}$$

where the natural frequency $\omega_n = \sqrt{\eta/\alpha}$ and the damping ratio $\zeta = \beta/(2\sqrt{\alpha\eta})$. Considering the second order characteristic equation in (4.14), the settling time can be estimated. If the ratio ζ ranges between 0 and 1 and ε is the steady state error, then the settling time t_s can be determined by

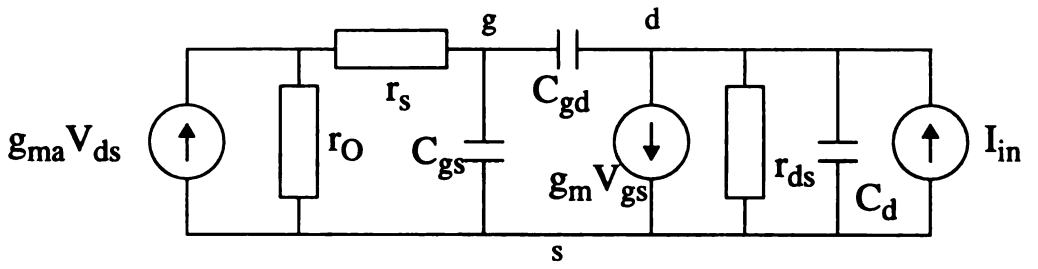


Figure 4.4 Small signal analysis of negative feedback current copier

$$t_s = \frac{-1}{\zeta\omega_n}\ln(\varepsilon\sqrt{1-\zeta^2}) \tag{4.15}$$

While ζ is larger than or equal to 1, the settling time can be decided by the roots, a and b, of the characteristic equation, where $|a| \geq |b|$ decides the dominant pole of the characteristic equation with 0.01% accuracy. The settling time can be approximated by

$$t_s = \frac{1}{b}\ln\varepsilon \tag{4.16}$$

Therefore, the settling time can be found and the comparison for different structures can be done.

Holding Time: Due to the leakage current, I_{leak}, of the holding capacitor, the currents held in the capacitor decreases. The leakage current is determined by that of the reverse-biased diode of a CMOS switch, and the time-dependent drain current due to the diode leakage can be expressed as [72]: $I_{ds,leak}(t)=I_{ref}-gm*I_{leak}/C_{gs}*t$. For a minimum CMOS switch, it consists of two transistors with the size of 3 μm/2 μm for 2 μm technology. A typical value is $I_{leak}=10$ mA/m^2 for each transistor [72]. Therefore, the current I_{leak} =0.12 pA for the CMOS switch. If we define the holding time as the time required for the holding capacitor to lose 0.01% of the generated current, then the holding time, τ_h, for an m-bit CRG circuit can be expressed as follows, where C_{pm} and g_{mp} are the capacitance and the transconductance of transistor in the m-th PMOS copier P_m, respectively

$$\tau_h = 10^{-4}*I_{bm}*C_{pm}/(gm_p*I_{leak}) \tag{4.17}$$

Accuracy: In the m-bit CRG_DC, the generated current reference is held in N_3, the current variation due to the charge injection error can be expressed as

$$\Delta I_{bk} = gm_k\,\Delta V \approx [2k_n(W/L)_{N3}I_{bk}]^{1/2}\,\Delta V \tag{4.18}$$

where g_{mk} is the transconductance of N_3 when the current I_{bk} is held. Therefore, the accu-

mulated error of the m-bit CRG_DC circuit is the sum of ΔI_{bk}'s, i.e., $\varepsilon_{acc(m)}=\Delta I_{b1}+\Delta I_{b2}+..+\Delta I_{bm}$.

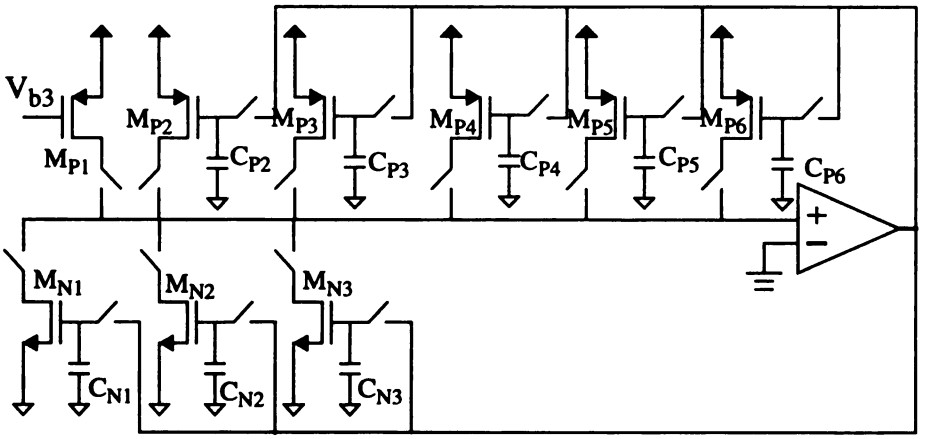
For the CRG_MC circuit, if we properly design the circuit so that $V_{gn}=V_{gp}=V_g$ in (4.8) and $C_{N1}=C_{N2}$, then the charge injection errors can be cancelled out because $\Delta Q_{N1}=\Delta Q_{xk}$. However, due to the process variation, there might have a mismatch between C_{N1} and C_{N2}. Without loss of generality, let $C_{N2}=C_{N1}+\Delta C_{N1}$, the error current can be expressed as $\Delta I=gm_n(\Delta Q/C_{N1})+gm_n[\Delta Q/(C_{N1}+\Delta C_{N1})]-gm_{xk}(\Delta Q/C_{xk}) \approx gm_n(\Delta Q/C_{N1})(\Delta C_{N1}/C_{N1})$. Since the CMOS process can control $\Delta C_{N1}/C_{N1}$ to be below 0.1%, the error current may be of insignificance.

4.2 Design Examples

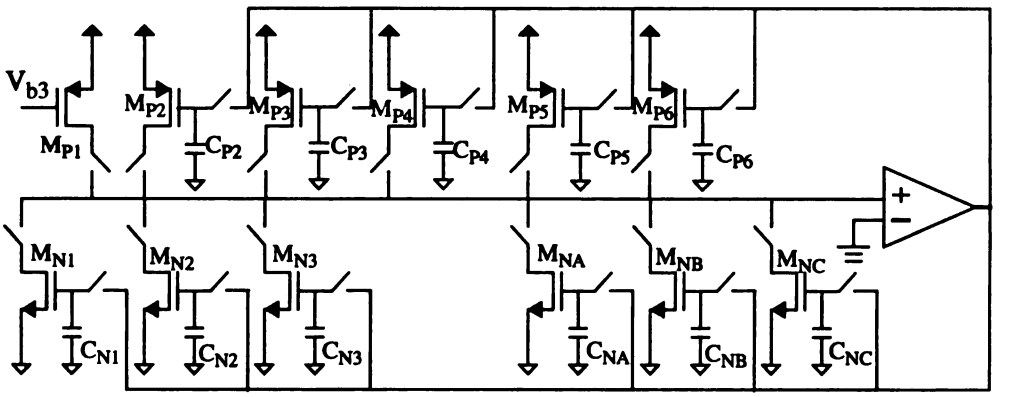
Based on the developed design methodology and performance analysis, a 6-bit CRG_DC circuit and a 7-bit CRG_MC circuit are demonstrated.

4.2.1 A 6-bit CRG_DC Circuit

Figure 4.5(a) shows a 6-bit CRG_DC circuit which is comprised of 3 NMOS current copiers with N_1, N_2, and N_3, one current source with $I_{FS}/2$ realized by a PMOS with a bias voltage V_{b3}, and 6 PMOS current copiers with M_{Pk}, k=2,3,.., 6. Consider the full scale current I_{FS}=1146.88 μA, i.e., $I_{MSB}=I_{FS}/2$=573.44 μA. The 6-bit CRG_DC circuit generates 4 current references I_{b1}=573.44 μA, I_{b2}=286.72 μA, I_{b3}=143.36 μA, I_{b4}=71.68 μA, I_{b5}=35.84 μA, and I_{b6}=17.92 μA. Note that k_n=48.92 μA/V^2 and k_p=19.16 μA/V^2 are considered in this design. By (4.4), the theoretically maximum values of $(W/L)_{N1}=I_{b1}/(0.98k_n')$=11.96, $(W/L)_{N2}=(W/L)_{N3}$=5.98. In this implementation, the transistors are cho-



(a)



(b)

Figure 4.5 6-bit CRG_DC circuits: (a) structure #1 and (b) structure #2.

sen as their sizes shown in Figure Table 4.1. In order to alleviate the charge injection errors, the capacitances are chosen as listed in Table 4.1 for achieving the accuracy better than 11 bits, i.e., the accumulated error currents must not exceed the limit ($1146.88*2^{-11}$), i.e., 0.56 μA.

The 6-bit CRG_DC in this implementation takes 2 cycles for each iteration [71], and thus, by (4.2), the total number of cycles required for generating the 6 current references is κ_{DC}=31. The cycle time is determined by the time required for generating I_{b6}. The settling time for I_{b6}=17.92 μA is estimated as follows: $\omega_n^2=3.7342*10^{17}$ and $2\zeta\omega_n=1.3107*10^{17}$. By (3.29), the settling time t_s=1.45 μs. This implies that the calibration time of the 6-bit CRG_DC circuit is 1.45 μs*31= 44.95 μs. By (5.10), the holding time of the 6-bit CRG circuit is τ_h=403 μs, where I_{leak}= 0.12 pA for the CMOS switch, I_{b6}=17.92 μA, gm_{p6}=37 μA/V, and C_{p6}=1 pF.

For sake of comparison, Table 4.2 lists the performance analysis for the CRG_DC circuit with 2 to 6 bits, including g_m, settling time, error current, and accumulated error currents. For example, a 4-bit CRG_DC circuit uses only 4 bits of the 6-bit CRG_DC circuit in Figure 4.5(a) and the corresponding parameters. For the accumulated error, by (4.8), the current deviation is ΔI_{b2}= 0.23 μA for I_{b2}=286.72 μA, where the transconductance g_{m2}=574.26 μA/V. Note that the voltage deviation due to the charge injection error is assumed to be ΔV=0.4 mV. (In practice, the deviation ΔV is not always constant.). Similarly, the error currents are calculated and listed in Table 4.1, where the accumulated error of the 6-bit CRG is 0.452 μA which is much smaller than 0.56 μA for 11-bit resolution. This concludes that, for a given full scale current I_{FS}=1146.88 μA, the 6-bit CRG circuit takes 44.95 μs to generate 6 current references with an accuracy better than 11-bits, where a supply

Table 4.1 Parameter Values for CRG_DC in Figure 4.5(a).

Transistor size W/L (μm)	M_{P1}	M_{P2}	M_{P3}	M_{P4}	M_{P5}	M_{P6}	Capacitance (pF)	C_{P2-P3}	C_{P4-P6}
	120/4	120/4	65/4	32/4	16/4	8/4		1.14	1.0
Transistor size W/L (μm)	M_{N1}	M_{N2}	M_{N3}				Capacitance (pF)	C_{N1-N3}	
	42/4	29/4	28/4					1.2	

Table 4.2 Performance Analysis for Various Bit Sizes of CRG_DC.

	characteristic equation	g_m (μA/V)	settling time (μs)	error current (μA)	acc. error current (μA)
I_{b2}	$s^2+3.3979*10^8s+2.8414*10^{17}=0$	574.26	0.055	0.230	0.230
I_{b3}	$s^2+1.4501*10^8s+2.3142*10^{17}=0$	298.86	0.127	0.119	0.349
I_{b4}	$s^2+5.2398*10^7s+1.6209*10^{17}=0$	148.27	0.352	0.059	0.408
I_{b5}	$s^2+1.9837*10^7s+6.7551*10^{16}=0$	74.1	0.928	0.029	0.437
I_{b6}	$s^2+1.3107*10^7s+3.7343*10^{16}=0$	37.0	1.450	0.015	0.452

voltage of 3.3 V and 2 μm CMOS process are employed. The resultant currents can be held for 403μs before they need to be refreshed.

The calibration time of the CRG_DC may be improved by using smaller holding capacitances and transistors. More specifically, the decrease of calibration time can be accomplished by using the smaller holding capacitances at the cost of increasing the error current. However, one may use a smaller NMOS transistor to bring the error current down. Figure 4.5(b) presents an alternative structure of a cascode 6-bit CRG_DC circuit and Table 4.3 lists the parameter values, where the parameter values of the first 4 bits are exactly the same as those in Figure 4.5(a), and three additional NMOS copiers with N_A, N_B, and N_C are employed. Note that the additional copiers function exactly the same as the copiers with N_1, N_2, and N_3. The PMOS copiers with P_5 and P_6 are used to generate and store the 5-th and 6-th current references. The parameter values for NMOS copiers with N_A, N_B, and N_C are selected for holding the maximum current $I_{b5}=I_{b1}/16$ to speed-up the settling times for I_{b5} and I_{b6}. Similarly, Table 4.4 lists the calculated gm, settling time, error current, and accumulated error current for both 5-th and 6-th bits. Results show that the 6-bit CRG_DC circuit takes 0.977 μs*31=30.29 μs to generate 6 current references with an accumulated error current of 0.472 μA which is better than 11-bit accuracy, and its holding time is 268 μs.

Comparing both 6-bit CRG circuits in Figures 4.5(a) and 4.5(b), the latter circuit improves the calibration time from 44.95 μs to 30.29 μs, i.e., 1.48 speed-up ratio, but the holding time drops from 403 μs to 268 μs and the accumulated error current increases from 0.452 μA to 0.472 μA. In addition, 3 extra NMOS copiers are needed in the latter circuit.

Table 4.3 Parameter Values for CRG DC in Figure 4.5(b).

Transistor size W/L (μm)	M_{P1}	M_{P2}	M_{P3}	M_{P4}	M_{P5}	M_{P6}	Capacitance (pF)	C_{P2-P3}	C_{P4-P6}
	120/4	120/4	65/4	32/4	32/4	18/4		1.14	1.0
Transistor size W/L (μm)	M_{N1}	M_{N2}	M_{N3}	M_{NA}	M_{NB}	M_{NC}	Capacitance (pF)	C_{N1-N3}	C_{NA-NC}
	42/4	29/4	28/4	10/5	16/10	15/10		1.2	0.6

Table 4.4 Performance Analysis for Various Bit Sizes of CRG DC

	characteristic equation	gm (μA/V)	settling time (μs)	error current (μA)	acc. error current (μA)
I_{b5}	$s^2+2.5278*10^7s+1.1453*10^{17}=0$	104.85	0.728	0.042	0.450
I_{b6}	$s^2+1.8843*10^7s+2.5387*10^{17}=0$	55.6	0.977	0.025	0.472

4.2.2 7-bit CRG_MC Circuit

Consider the 7-bit CRG_MC in Figure 4.3(c). With I_{LSB}=0.56 μA, the 7-bit CRG_MC circuit generates I_{x1}=0.56 μA, I_{x2}=1.12 μA, I_{x3}=2.24 μA, I_{x4}=4.48 μA, I_{x5}=8.96 μA, I_{x6}=17.92 μA, and I_{x7}=35.84 μA. Theoretically, by (4.7), the minimum size of the transistor N_1 must be exceed 0.56 μA/(0.02k_n)=0.572. Here, we chose $(W/L)_{N1}$=$(W/L)_{N2}$=5 μm/7 μm. Table 4.5 lists the parameter values. The holding time is determined by the copier with $M_{P1}$and it is approximately 509 μs.

4.2.3 Simulation Results

Figure 4.6(a) shows the simulation results of the 6-bit CRG_DC circuit in Figure 4.5(b), where the parameter values in Table 4.3 are used, and 3.3 V supply voltage and *MOSIS SCN20* 2 μm CMOS process with 2-level transistor parameters are simulated. Results show that the circuit takes 31 cycles with a clock rate of 1 μs, i.e., its calibration is 31 μs.

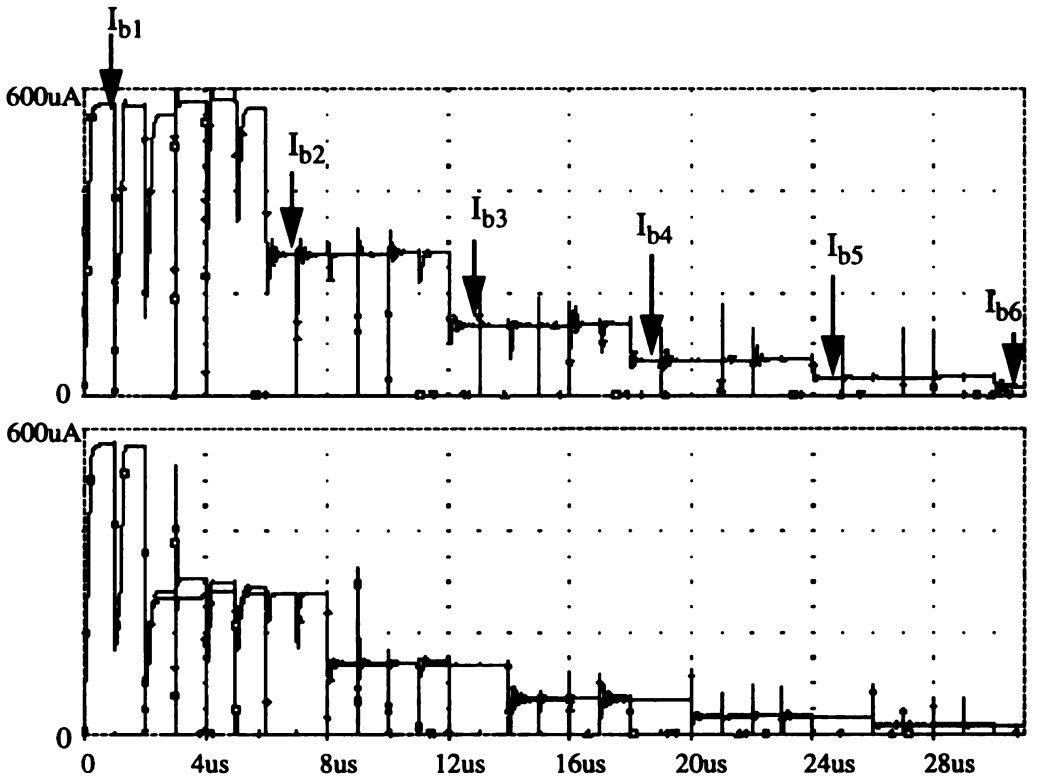
Figure 4.6(b) shows the simulation results of the 7-bit CRG_MC circuit in Figure 4.3(c) with the parameter values in Table 5.5. The circuit takes 18 cycles to generate the 7 current references, where the clock rate is also set to 1 μs, i.e., its calibration time is 18 μs.

4.3 DAC Circuit Design

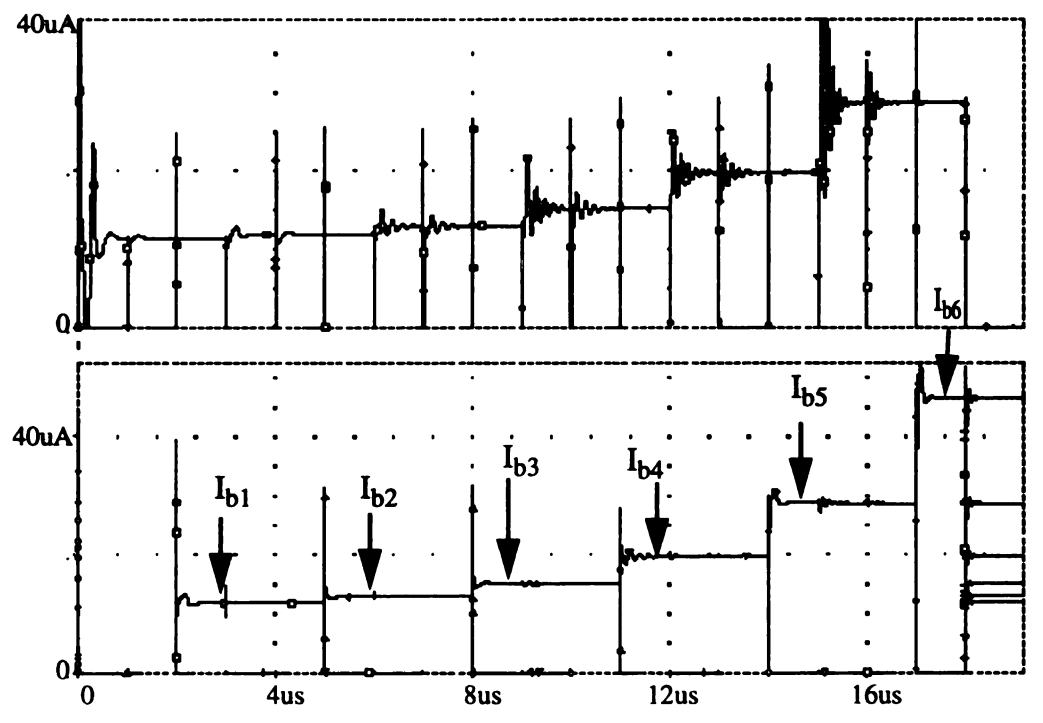
This section presents high-speed DAC circuits for low-power applications. As shown in Figure 4.7, the developed (α+β)-bit DAC circuit, i.e., MαDβ DAC circuit, is comprised of a α-bit CRG_MC to generate J_k's, k=1,2,..,α, from the LSB, and a β-bit CRG_DC to generate I_k's, k=1,2,..,β, from the MSB. Based on the design and simulation results of the 6-bit CRG_DC and 7-bit CRG_MC circuits presented in the previous section, we may construct the following hybrid 11-bit DAC circuits: M7D4, M6D5, and M5D6.

Table 4.5 Parameter Values for CRG_MC in Figure 4.3(c).

Transistor size W/L (μm)	M_{x1}	M_{x2}	M_{x3}	M_{x4}	M_{x5}	M_{x6}	M_{x7}	M_{N1}	M_{N2}	M_{Ri}
	5/16	9/11	8/4	7/3	10/3	11/3	18/3	5/7	5/7	6/5
Capacitance (pF)		C_{x2}	C_{x3}	C_{x4}	C_{x5}	C_{x6}	C_{x7}	C_{N1}	C_{N2}	
		0.69	0.72	0.85	1.1	1.1	2	0.35	0.35	



(a)



(b)

Figure 4.6 Simulation results: (a) 6-bit CRG_DC Circuit;
and 7-bit CRG_MC Circuit.

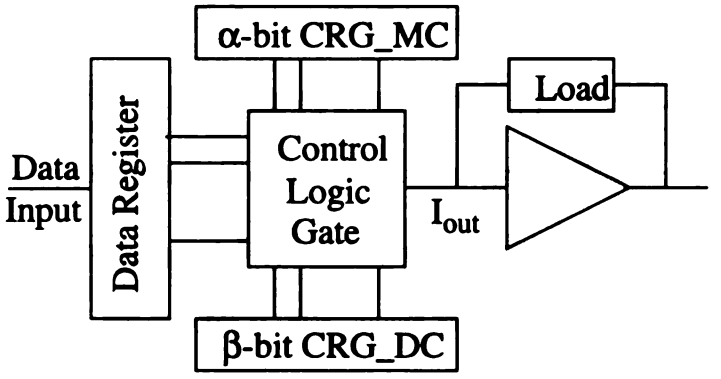


Figure 4.7 Proposed DAC circuit structure

4.3.1 Low Power SI DAC Design

In an N-bit CRG_DC circuit, its LSB current, $I_{LSB}=I_{FS}/2^N$, cannot be lower than its signal-to-noise ratio (SNR). This implies that its bit size is limited by the given full-scale current I_{FS}. It also implies that, for a given SNR of an N-bit CRG_DC circuit, the only way to increase the bit size is the use of larger I_{FS}, but it will be penalized by the increase of power consumption. This concludes that the bit size of both CRG_DC and CRG_MC circuits cannot be arbitrarily large for low-power applications. To increase the resolution of a SI CMOS DAC circuit for low-power application, the block diagram of a high-speed SI DAC circuit, as shown in Figure 5.8, is developed in this study. The developed (α+β)-bit DAC employs a α-bit CRG_MC to generate J_k's, k=1,2,..,α, from the LSB, and a β-bit CRG_DC to generate I_k's, k=1,2,..,β, from the MSB. For simplicity, the DAC is referred to as a MαDβ DAC circuit. For example, a M7D4 DAC circuit is a hybrid 11-bit DAC circuit with a 7-bit CRG_MC and a 4-bit CRG_DC. It should be mentioned that an alternative high-resolution hybrid current-mode DAC was reported in [40], but it employs well-matched components similar to Figure 2.5(b) to generate the current references.

4.3.2 Design Example -- an 11-bit DAC Circuit

Consider the 7-bit CRG_MC circuit in Figure 4.3(c) and the 4-bit CRG_DC circuit in Figure 4.5(a). (Note that the simulation results for the 4-bit CRG_DC in Figure 4.5(b) should be the same as those in Figure 4.5(a).) Results in Figure 4.6(b) show that the calibration time of the 7-bit CRG_MC circuit is 18μs and the holding time is 509 μs. For the 4-bit CRG_DC circuit, the first 19 cycles in Figure 4.6(a) shows that the calibration time is 19μs and the holding time is 402 μs. This concludes that the M7D4 DAC circuit takes 19μs

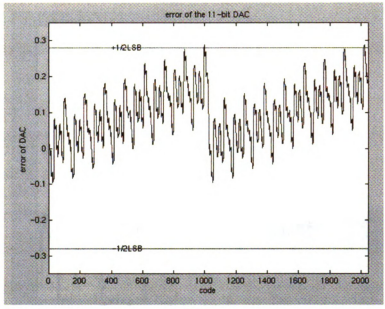
to generate the 11 current references which can be used for 402 μs before refreshing. The power consumption is approximately 4.4 mW, including 3.8 mW for loading the current references and 0.6 mW for the op-amp.

Figures 4.8(a) and 4.8(b) plots the integral nonlinearity (INL) and the differential nonlinearity (DNL) of the hybrid M7D4 DAC circuit, while Figure 4.8(c) shows the floor noise spectrum of the 1024-FFT. The output is the fill scale swing sinusoidal wave with 25 kHz. The difference between the signal to the floor noise is approximately 73 dB. Simulation results show that the M7D4 DAC circuit has 11-bit resolution, 100 MSample per second for conversion rate, and the power consumption is approximately 4.4 mW with 3.3 V power supply voltage and *MOSIS SCN20* 2 μm CMOS process with 2-level transistor parameters.

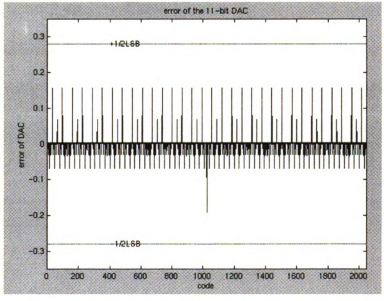
4.3.3 Alternative Designs

Consider the design of a hybrid M5D6 DAC circuit, where the 6-bit CRG_DC circuit in Figure 4.5(b) and the 5-bit of the CRG_MC in Figure 4.3(c) are employed. As shown in Figure 4.6(a), the calibration time of the 6-bit CRG_DC circuit is 31 μs and the holding time is 268 μs. On the other hand, as shown in Figure 4.6(b), the calibration of the 5-bit CRG_MC is 12 μs and the holding time is 509 μs. This concludes that the M5D6 DAC circuit takes 31 μs to generate the 11 references and needs to be refreshed at 268 μs. Similarly, Figures 4.9(a) and 4.9(b) plots the INL and DNL of the hybrid M5D6 DAC circuit. Both M5D6 and M7D4 DAC circuits have the same SNR of 62 dB which is a 11-bit resolution.

It should be mentioned that the CRG_DC circuit generates its current references from I_{MSB}, while the CRG_MC circuit does it from I_{LSB}. Therefore, the accumulated error

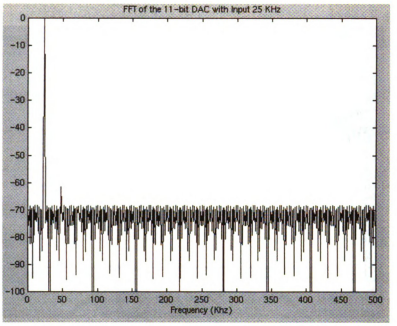


(a)



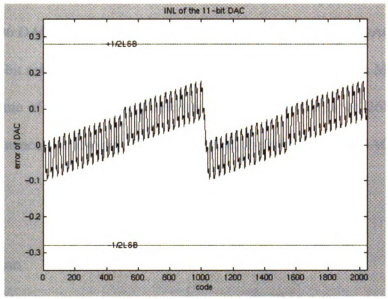
(b)

Figure 4.8 Nonlinearity analysis of M7D4 DAC: (a) INL; (b) DNL; and (c) Noise Floor.

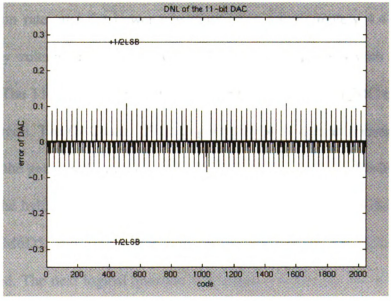


(c)

Figure 4.8 (cont'd)



(a)



(b)

Figure 4.9 Nonlinearity analysis of M5D6 DAC: (a) INL; and (b) DNL.

currents resulted from the CRG_DC circuit are generally smaller than those from the CRG_MC circuit. This can be seen from both INL and DNL plots in Figures 4.8 and 4.9, i.e., the M5D6 DAC circuit has better nonlinearities than the M7D4 DAC circuit, but both achieve a 11-bit resolution. Since the M7D4 DAC circuit is better than M5D6 circuit in the calibration time of 19 μs vs. 31 μs and the holding time 402 μs vs. 268 μs, as far as the speed performance and low-power are concerned, the hybrid M7D4 DAC circuit is recommended.

4.4 Conclusion

This chapter presents a high performance SI CMOS DAC circuit for low-power applications, where the DAC circuit achieves 11-bit resolution, 100 MSample per second for conversion rate, and the power consumption is approximately 4.4 mW with 3.3 V power supply voltage and *MOSIS SCN20* 2 μm CMOS process with 2-level transistor parameters. The 11-bit DAC circuit is comprised of a 7-bit CRG_MC circuit and a 4-bit CRG_DC circuit. The DAC takes 19 μs to generate the 11 current references for data conversion, and the generated currents can be held for 402 μs before refreshing.

For the hybrid 11-bit DAC circuits, three different structures may be constructed, i.e., M7D4, M6D5, and M5D6. For high speed performance, the M7D4 DAC circuit is recommended. The next logical question is whether it is feasible for developing the high speed hybrid DAC circuit with higher bit size for low power applications. The cascode structure for CRG_DC presented in Figure 4.5(b) can be potentially extended for higher bit size. For low-power applications, however, there exist some design trade-offs among accuracy and speed performance. This leads to a very important research topic that devel-

ops a synthesis process for generating high speed hybrid DAC circuits for low power applications.

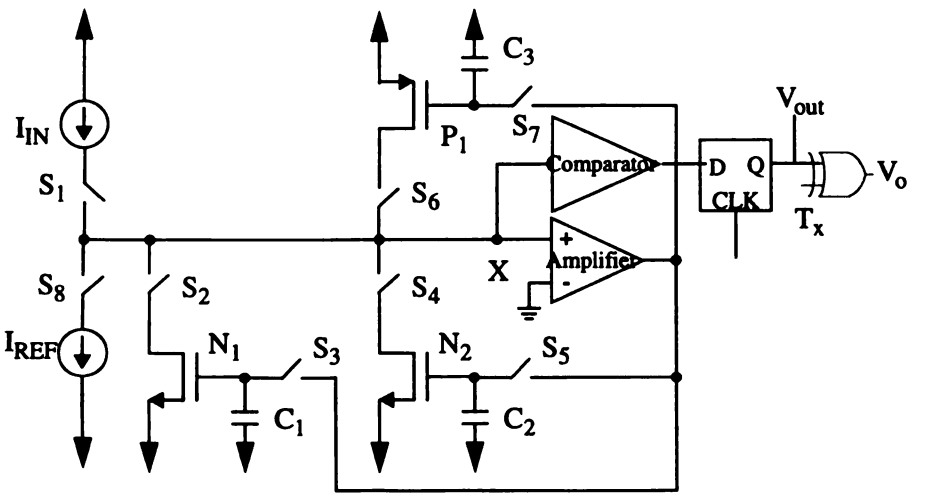
Chapter 5

BUILT-IN TESTERS FOR SI CIRCUITS

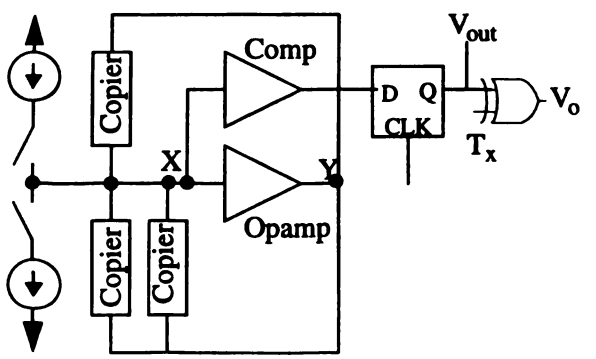
Built-in self-test (BIST) has been accepted as a tool for digital verification and production test. A tester is built inside the circuit to monitor the circuit performance. Thus, the tester will reduce the tester complexity, eliminate the need for off-chip interfacing, and allow the device to be tested many times during the manufacturing cycle of the product. The BIST approach has also been introduced for analog circuits [73]. However, the BIST approach may require additional hardware and degrade performance of the designed circuits. Section 5.1 reviews the structure of a built-in tester for SI circuits developed in [48]. The built-in tester is comprised of a high-accuracy CMOS current comparator, a voltage window comparator, and a latch [73-75]. Section 5.2 introduces a high performance current comparator which is capable of autozeroing and self-testability. Finally, Section 5.3 gives a concluding remark.

5.1 Built-in Testers

In order to enhance the reliability of SI circuits, a built-in tester was introduced in [48-50]. Consider the ADC circuit in Figure 2.4(a) with its output stage shown in Figure 5.1(a), and its simplified version in Figure 5.1(b), where the circuit is comprised of 3 current copiers. The current copier has an S/H function and can be implemented as an



(a)



(b)

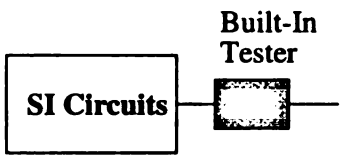
Figure 5.1 Tester: (a)Proposed test SI circuit; (b) Simplified of proposed test

analog scan structure for fault diagnosis and testing [73,76]. Test generation [47] and BIST design [61] of such a converter have been developed for single stuck-at fault models. Furthermore, the test generation of the ADC circuits for both stuck-at and parametric fault models were reported in [49] which shows that the N-bit resolution ADC circuit takes approximately 24N clock cycles to detect all switching element faults [50]. The ADC circuit can achieve 11-bit resolution and thus requires 264 cycles to detect the faults. The number of clock cycles for detecting the faults can be reduced significantly if a high-accuracy built-in tester can be used [50].

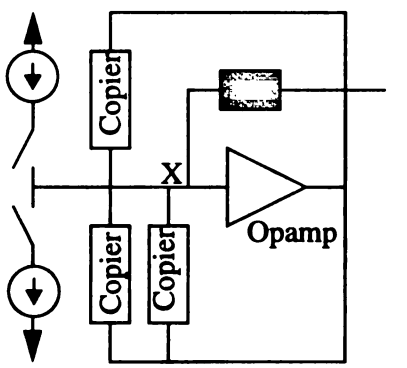
Figure 5.2(a) illustrates a typical SI circuit with a built-in tester which is currently not available in its counterpart SC circuits. Figures 5.2(b) shows an example of the ADC circuit in Figure 5.1(b) with the tester. With the self-testing capability, the tester can be first self-tested. The fault-free tester is then used to test each component in SI circuits, such as current copiers, current sources, amplifiers, etc. Finally, the tester will verify the interconnections. Here, both catastrophic and parametric faults are included.

Consider the block diagram of a built-in tester in Figure 5.3(a) [48]. The current comparator checks if the difference of two input currents I_{i1} and I_{i2} is sufficiently small. A corresponding voltage level V_y with respect to the current difference $I_x=I_{i1}-I_{i2}$ is generated. Thus, the current comparator is effectively a current-to-voltage (I-V) converter. The generated voltage level is then applied to a regenerative latch to determine the digital output.

If the comparator is designed in such a way that a corresponding voltage level V_y, $-V_w \le V_y \le V_w$, is generated for any input I_x, $-I_{tol} \le I_x \le I_{tol}$, then a simple voltage window comparator with a pair of symmetric the threshold voltages, V_w and $-V_w$, can be used. An

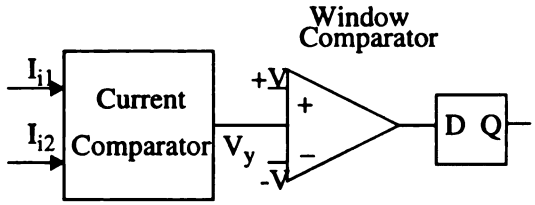


(a)

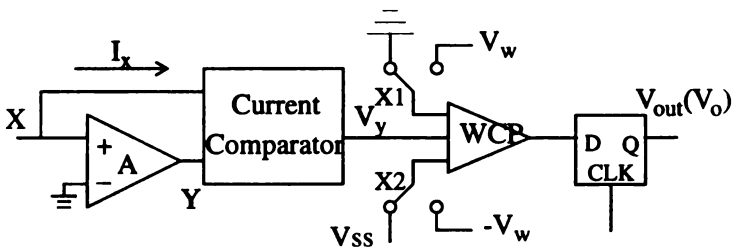


(b)

Figure 5.2 SI tester: (a) SI circuit with tester; (b) SI A/D converter



(a)



(b)

Figure 5.3 Schematic and configuration of built-in tester: (a) schematic; (b) configuration

ideal current comparator has a linear relationship between I_x and V_y as

$$V_y = I_x \quad r_k \tag{5.1}$$

where r_k is a constant transresistance.

Figure 5.3(b) shows the schematic diagram of the built-in tester which is applied to the A/D converter in Figure 5.1(a), where nodes X and Y are the same locations as those in Figure 5.1(b). Two multiplexers X1 and X2 are used in the voltage window comparator (WCP). During the normal operation, X1 and X2 are switched to Ground and V_{SS}, respectively. The output of WCP is set to "1" if $V_y > 0$, and to "0" otherwise. They are set to V_w and $-V_w$ during the test mode.

The threshold voltage V_w is determined by the predetermined tolerable current I_{tol} [48]. It should be noted that an ideal current comparator may have a linear relationship between I_x and V_y, as shown in (5.1). However, the voltage V_y may deviate because of the offset current due to mismatched components in the current comparator and the nonlinearity of r_k. The offset current may cause an offset voltage, V_{ofs}, in the output of the current comparator, while the nonlinearity of r_k leads to a nonlinearity quality $V_{nl}(I_x)$ which is a function of I_x. Thus, V_y in (5.1) can be re-written as

$$V_y = I_x \quad r_k + V_{ofs} + V_{nl}(I_x) \tag{5.2}$$

Hence, the accuracy can be improved by reducing the terms V_{ofs} and $V_{nl}(I_x)$. Let $V_{y(max)}$ and $V_{y(min)}$ be the maximum and minimum values of V_y in (5.2) due to the above deviations. Since designing a window comparator with symmetric threshold voltages, i.e., $V_1=-V_2$, seems to be easier than with non-symmetric ones, we choose $V_1=-V_2=V_w$. However, the window comparator may produce incorrect comparison results in the ranges

$[V_w, V_{y(max)}]$ and $[-V_w, V_{y(min)}]$. This becomes an important issue for the quality of the tester.

The quality of the tester is determined by its testing confidence with respect to the selected tolerant current I_x, where the *testing confidence* of a tester is defined as the probability that the comparison results are reliably determined. Based on the test confidence discussed in [48], Figure 5.4 plots the relationship between the testing confidence and the testing resolution. The testing resolution is defined as the number of bits that represent the ratio I_{tol}/I_{max}, where I_{max} is the maximum different current applied to the tester, i.e., $I_{max}=I_{x(max)}$. Mathematically, the number of bits, b, is

$$b = \lceil log_2(I_{max}/I_{tol}) \rceil \tag{5.3}$$

For example, suppose that I_{max}=100 μA and I_{tol}=40 nA; by (5.3), the testing resolution is b=12 bits. Similarly for I_{max}=100 μA and I_{tol}=20 nA, the testing resolution is 13 bits. Therefore, given a tolerance current I_{tol}, the threshold voltage V_w of the window comparator is chosen as

$$V_w = I_{tol} r_k = (I_{max} r_k)/(2^b) \tag{5.4}$$

Since the converter circuit implements a multiply-by-two circuit that doubles the residual current at each cycle of conversion, the tolerant current is also doubled. More specifically, at the first bit conversion, the tolerant current is $(1/2)I_{LSB}$; $I_{tol}=1I_{LSB}$ for the second bit conversion; and $I_{tol}=2^{M-1}I_{LSB}$ at the M-th bit conversion. Suppose a tester with b-bit resolution is used, we have

$$I_{tol}=2^{M-1}I_{LSB}=2^{-b}I_{max} \tag{5.5}$$

where $I_{max}=I_{ref}=2^N I_{LSB}$ for an N-bit A/D converter. This implies that b=(N+1)-M. For the

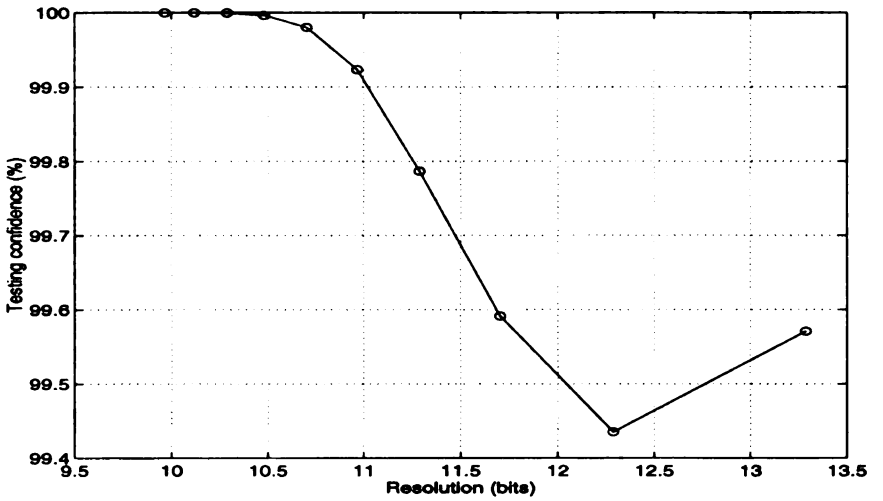


Figure 5.4 Test confidence vs. resolution

ADC circuit in Figure 5.1(a), the comparator requires $I_{tol}=(1/2)I_{ref}$, i.e., M=N, or b=1, i.e., this implies that the comparator used in the converter is equivalent to a tester with a testing resolution b=1.

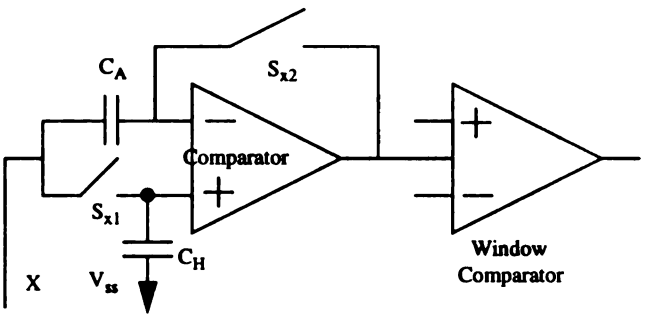
By (5.5), if we use the developed tester with 12-bit resolution, i.e., with a threshold voltage V_w=130 mV, for the ADC circuit in Figure 5.1(a), any faults can be detected during the conversion with a testing confidence of 99.5% and no test sequence is needed. On the other hand, if we use a tester with 11-bit resolution, with V_w=260 mV, for the ADC circuit, any faults can be detected with a testing confidence of 99.9% and 24 test cycles are needed. Similarly, for 10-bit resolution tester with V_w=521 mV, it has almost 100% testing confidence and takes 48 test cycles. This example concludes that the number of test cycles decreases as the accuracy of the tester increases.

5.2. CMOS Current Comparator

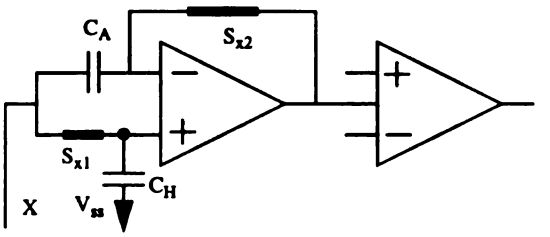
One of the most critical parameters which limit current comparator performance is the offset voltage of the comparators [16]. This study develops a high accuracy CMOS current comparator which is capable of autozeroing and self-testability. The autozeroing property is to reduce the offset voltage and to increase the accuracy of the tester, while the self-testability is to enhance the reliability of the tester.

5.2.1. Autozeroing

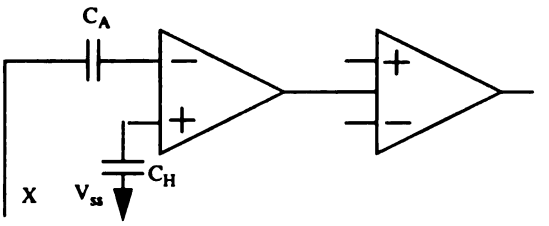
Figure 5.5(a) shows an autozeroed current comparator which is operated in two phases: autozeroing phase and comparing phase. During the autozeroing phase, the circuit



(a)



(b)



(c)

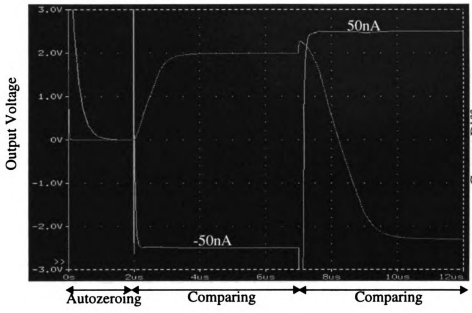
Figure 5.5. Autozeroed current comparator: (a) schematic;
(b) autozeroing phase; and (c) comparing phase.

is reconfigurated as shown in Figure 5.5(b), where switches S_{x1} and S_{x2} are ON. As a result, the offset voltage of the comparator is memorized by the capacitor C_A, and the voltage at node X is memorized in the capacitor C_H. During the comparing phase, the comparator is reconfigured as shown in Figure 5.5(c), where both S_{x1} and S_{x2} are OFF. The capacitor C_A is connected in such a manner as to cancel the offset voltage.

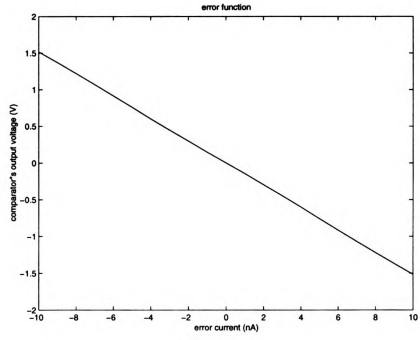
The current comparator in Figure 5.5(a) has been designed and simulated by ***pspice***, where the *SCNA20* 2μm CMOS process with level-2 transistor parameters are assumed. The switches are realized by CMOS transistors with dummy switches to alleviate the charge-injection error effects. Figure 5.6(a) shows the simulation results of the autozeroed comparator. The first stage is the autozeroing, the second stage is with an input current, or the current difference, of -50nA, while the third stage is with 50nA. From the transfer function of the comparator, as shown in Figure 5.6(b), one can determine the threshold voltages needed for the window comparator. Simulation results show that, for an input current 100μA, the comparator can achieves a resolution of 1nA. This is equivalent that the comparator can reach a 16-bit resolution.

5.2.2 Self-Testability

The self-testability of the tester is verified through fault simulation. Consider the ADC circuit in Figure 5.7, where the comparator and output latch circuit in Figure 5.1(a) are replaced by the tester in Figure 5.5(a). In this fault simulation, only one fault is injected at a time and the fault is assumed to be S/ON or S/OFF fault. The S/ON fault is simulated by connecting two node of the switch, while the switch is removed for S/OFF fault. To simplify the discussion, we only consider the equivalent circuit, as shown in Figure 5.8(a),

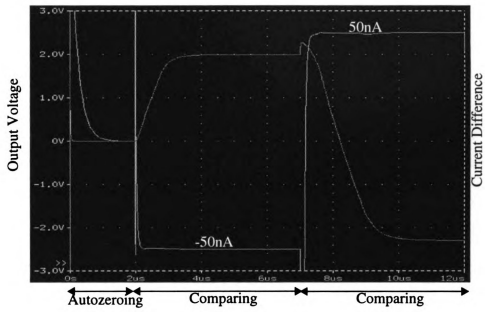


(a)

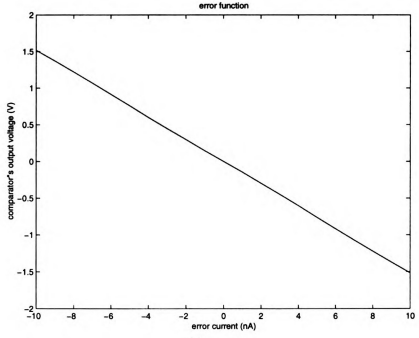


(b)

Figure 5.6 Analysis of current comparator: (a) simulation result for comparator; (b) transfer function of comparator



(a)



(b)

Figure 5.6 Analysis of current comparator: (a) simulation result for comparator; (b) transfer function of comparator

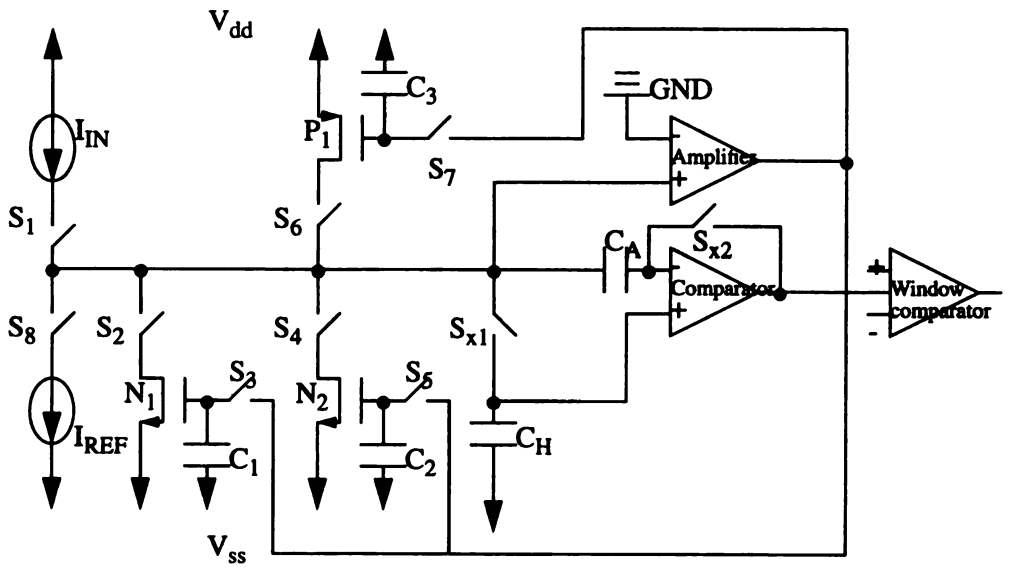


Figure 5.7 The configuration of circuit under testing

for fault simulation, where the current copiers with N_2 and P_1 are switched away during the simulation by turning off S_4, S_5, S_6, S_7, and S_8.

A test sequence is applied to detect the S/ON and S/OFF faults for both S_{x1} and S_{x2}. The test sequence is comprised of three cycles. In the first cycle, as shown in Figure 5.8(b), the current copier with N_1 is calibrated with $I_{IN}=I_{REF}$ and the comparator is in the autozeroing phase. Switches S_1, S_2 and S_3 in the copier are ON and switches S_{x1} and S_{x2} in the comparator are also ON. Since the comparator is performing autozeroing, the output of the comparator is zero. In the second cycle, as shown in Figure 5.8(c), switch S_3 in the copier and S_{x1} and S_{x2} in the comparator are all OFF. The offset voltage of the op-amp is stored in C_A and $V^-_{comp}=V^+_{comp}$. Thus, the output of the comparator is also zero. This concludes that, for fault-free tester, the output voltages of the comparator are all zeros with these two cycles.

Consider the S/OFF fault on S_{x2}. In the first cycle, the comparator fails to perform autozeroing. Since the comparator has a differential gain about 80 dB, the difference (V^+_{comp}-V^-_{comp}) forces the output of comparator to become very close to V_{dd}, as shown in Figure 5.9. The same output voltage is carried into the second cycle. Thus, the fault can be detected. For the S/OFF fault on S_{x1}, since the comparator performs autozeroing in the first cycle, the output voltage of the comparator is zero and thus the fault cannot be distinguished in the first cycle. However, in the second cycle, $V^-_{comp}=V_X+V_{CA}$, and the fault causes a negative V^+_{comp}. As a result, a negative output is obtained, and a "1" is detected from the window comparator which distinguishes the faulty circuit from the fault-free one.

When a S/ON fault occurs at S_{x1}, the comparator performs autozeroing in the first cycle regardless of the fault. In the second cycle, the fault causes $V^+_{comp}=V_X=V^-_{comp}$ and

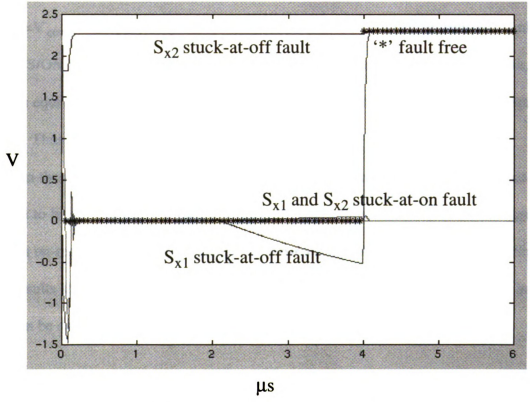


Figure 5.9 Fault simulation results

thus the output of the comparator is zero. In other words, the first two cycles of the test sequence cannot detect such a fault. In order to detect such a fault, the third cycle is applied with the same setting as in Figure 5.8(c), except that $I_{IN}=I_{REF}/2$. For the fault-free circuit, the capacitor C_H memorizes the voltage V_x when $I_{IN}=I_{REF}$. Now, when the input current decreases, the voltage V_x also decreases. As a result, $V^-_{comp} < V^+_{comp}$ and a negative output in the comparator is obtained, or a 1 is expected. However, in the presence of such a fault, $V^+_{comp}=V^-_{comp}$ and a zero output is resulted. Therefore, the fault can be detected. Similarly, for a S/ON fault on S_{x2}, a 1 is expected for the fault-free circuit. With such a fault, the circuit is equivalent to performing the autozeroing for the third cycle, i.e., a zero output is resulted. Thus, the fault can be detected.

In these fault simulations, the on-resistance and off-resistance of the switches are assumed to be 5.7 kΩ and 1.2 GΩ, respectively. The parametric faults in switch assume that both on-resistance and off-resistance are moved away from the defined values. Simulation results show that both catastrophic and parametric faults for the components in the tester can be detected. Thus, the tester circuit is fully testable.

5.3 Conclusion

This chapter presents the design and operation of built-in tester for high performance and low power CMOS switched-current circuits. The tester is comprised of a high accuracy current comparator, a voltage window comparator, and a digital latch. In this study, a simple, yet high accurate current comparator which is capable of autozeroing and self-testing is developed. The autozeroing property increases the accuracy of the tester. Simulation results show that the comparator can achieve a resolution of 1 nA which is

equivalent to a 16-bit resolution. This chapter also demonstrates the self-testability of the tester through a fault simulation. Since the current comparator possesses self-testing capability, the fault-free comparator can test all components in the SI circuit and thus simplifying the testing process. This study has evidently shown that the use of tester in SI circuit has made more attraction of using SI technique for the analog portion of the mixed-signal circuit design.

Chapter 6

CONCLUSION

The advent of portable communication and computing service has stirred a great deal of interests in both commercial and research areas. The circuit technology used in portable equipment has been changed from the conventional analog circuit technology to mixed-signal circuit technology. Low power and high performance are strongly needed for both analog and digital circuits to increase operation time of the portable equipment. The design of low power and high performance mixed-signal CMOS IC's is hindered by processing techniques that are optimized for digital applications. Moreover, scaling/reliability consideration are driving CMOS process towards submicrometer feature size and lower power supply voltages.

SI technique has received considerable attention as an alternative for analog data acquisition and conversion circuit design. However, existing SI circuits cannot make the theoretically expected performance due in part to the use of non-optimal current copiers, its basic building blocks. Based on our development of design methodologies and synthesis process for optimally generating low power and high performance CMOS current copiers [18,63], SI technique becomes feasible.

With the successful development in this thesis study, we believe that SI technique will soon become an alternative industrial standard for designing analog components in mixed-signal circuits for low-voltage/low-power signal processing applications.

6.1 Summary and Contribution

Chapter 1 introduces the advantages of using SI technique for designing analog portion of mixed-signal ICs. The objective of the thesis study is to develop high performance and low power data converters, ADC and DAC circuits. Chapter 2 reviews existing current copiers, current-mode multiplier and divider circuits, ADCs and DACs, and test generation for SI circuits.

Chapter 3 presents a high performance and low power CMOS cyclic ADC circuit. The ADC circuit has been designed, simulated, and fabricated. The designed ADC circuits takes 2.13 mm^2 in chip area, achieves a resolution of 12-bits, and consumes only 1.9 mW in power. High performance is attributed to the use of the following components: (1) a high performance residual amplifier which takes two clock cycles to double a current; and (2) an efficient cyclic RSD algorithm which provides 1.5b resolution without using two matched reference currents.

Based on efficient current-mode divider and multiplier circuits, Chapter 4 develops the design methodologies and performance analysis process for current reference current generator (CRG) circuits which generates the weighted reference currents for DAC circuits. The developed design methodologies guide the designers to properly select the transistor sizes and capacitances based on a given set of design specifications including input dynamic range, full-scale current, SNR, power consumption, etc., and the performance analysis process estimates the calibration time, holding time, and accuracy of the CRG circuits. For low power applications, a hybrid (α+β)-bit DAC circuit design is introduced, where a α-bit CRG_MC circuit and a β-bit CRG_DC circuit are employed. This chapter demonstrates the detailed design of a DAC circuit which achieves 11-bit resolution, 100

MSample per second for conversion rate, and the power consumption is approximately 4.4 mW with 3.3 V power supply voltage and *MOSIS SCN20* 2 μm CMOS process with 2-level transistor parameters. The 11-bit DAC circuit is comprised of a 7-bit CRG_MC circuit and a 4-bit CRG_DC circuit. The DAC takes 31 μs to generate the 11 current references for data conversion, and the generated currents can be held for 402 μs before refreshing. The trade-offs among the different structures are discussed such as M7D4, M6D5, and M5D6. The designer can choose the most feasible structure to reach the specification of the product and speed up the design period.

In order to enhance the testability of SI circuits, Chapter 7 presents a built-in tester design. A high performance current comparator was developed. The comparator possesses the features of autozeroing and self-testability. The autozeroing property reduces the offset voltage of the comparator and thus increasing the accuracy of the comparator, while the self-testability of the comparator enhances the self-testability of the tester.

The major contributions in this thesis study can be categorized as follows:

(a) *Developing high performance and low power SI CMOS cyclic ADC circuit*

(b) *Developing design methodologies and performance analysis process for high performance and low power SI CMOS hybrid DAC circuits.*

(c) *Developing a built-in tester for high performance and low power SI circuits.*

The simulation results and measures of the fabricated ADC chip demonstrate the feasibility of the SI technique. The considerably low power consumption will soon make the SI technique to become an alternative industrial standard for designing analog components in mixed-signal circuits. In addition, the salient feature of the self-testability of the built-in tester makes the SI circuits to be easily testable.

6.2 Future Work

Based on design trends that the complexity of analog/mixed-signal ICs will continuous to increase. Portable systems will become more and more popular as the size continues to shrink. Thus, further decreasing the power consumption to prolong the life of portable systems becomes more and more important. Also, enhancing the testability becomes necessary for quality improvement.

The quality of the developed data converter circuits can be further improved by using better process technologies and low supply voltages. In this study, the *MOSIS* 2μm digital CMOS process and 3.3 V supply voltage were assumed. The power consumption can be further reduced with the decrease of supply voltage. However, there exist design trade-offs between power reduction and speed performance. Therefore, it is worthwhile to examine the performance degradation of the developed data converters due to the decrease of supply voltages such as 2.5V or 1.5V, and to develop design methodologies for data converter to improve the performance while keeping low power consumption.

One solution to increase the conversion speed of the developed ADC circuit is the use of pipeline structures. The developed ADC circuits can be easily modified as pipeline structures. It is believed that the pipeline structure can achieve the same resolution and its data conversion rate can reach to 8 MSamples per second. However, the offset current for each stage must be carefully managed to keep the same accuracy.

The developed hybrid DAC circuits whose weighted currents are generated by both CRG_DC and CRG_MC circuits. The accuracy of both CRG circuits does not require well-matched components. However, due to the leakage currents, the generated current references need to be refreshed. Note that the data conversion will not be available

when the CRG circuits are being refreshed. Therefore, the DAC circuits will be perfectly applied to some applications which allow the DAC circuits have a period of idle time.

Finally, the developed built-in tester can significantly simplify the testing process of SI circuits. It is believed that the autozeroing scheme for current comparator can be modified for voltage comparators. Thus, the same concept of the tester design should be to apply for switched-capacitor circuits. This leads to a very interesting and important research topic for future study.

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