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HIGH PERFORMANCE CMOS SWITCHED-CURRENT CIRCUITS FOR LOW-VOLTAGE SIGNAL PROCEESSING APPLICATIONS

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ABSTRACT

HIGH PERFORMANCE CMOS SWITCHED-CURRENT CIRCUITS FOR LOW-VOLTAGE SIGNAL PROCEESING APPLICATIONS

By

Renyuan Huang

Portable televisions, camcoders, and compact disk players have been made available by consumer electronics companies. Cellular phones provide virtually unlimited access for voice communications; and laptops, notebooks and palmtops are the fastest growing types of computers. Portable multimedia terminal will come into being, which will be capable of providing speech communication, data transfer, handwriting recognition, and high-quality, full motion video. Each of these technologies relies on VLSI for cost and power-consumption effective implementation. Given sufficient complexity, even CMOS dissipation levels become excessive especially where high frequency is involved. It is necessary to optimize the VLSI-technology for low-power operation of digital/analog circuits.

CMOS switched-current (SI) technique has received considerable attention as an alternative for analog circuit design. However, existing SI circuits cannot make the theoretically expected performance due in part to the use of non-optimal current copiers, its basic building blocks. With the developed design methodologies and synthesis process for optimally generating low power and high performance CMOS current copiers, SI technique becomes feasible.

The objective of the thesis research is to develop new generation of high-performance, low-power/low-voltage current-mode circuits. The emphasis is placed on the development of sample/hold circuits, and analog-to-digital circuits for mixed-signal IC's in future portable equipment. In this study, a simple yet high performance SI V-I converter with the S/H function and an oversampled high linear S/H circuit are developed. Result shows that, with the small resistor in the V-I converter, a large dynamic range of the converted current can be obtained with a small swing of input voltages. Thus, the circuit is viable for low-voltage operation. The developed oversampled SI S/H circuit adopts a simple forward approach to reduce the output current of the integrator. With a simple structure and a small oversampling ratio, the circuit achieves high accuracy. This study also develops a high performance cyclic A/D converter circuit design. The high performance is attributed to: (1) the use of high performance current copiers; (2) the use of a residual amplifier which takes two clock cycles to double a current; (3) the use of an efficient Cyclic RSD algorithm which provides 1.5b resolution without using two matched reference currents.

The developed circuits meet the design requirement not only for portable equipments, but also for video signal processing, such as HDTV, high-frequency digital communications, and waveform acquisition/instrumentation. This research has demonstrated that this development is not merely an academic curiosity, but an important practical technology for the future.

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Chapter 1

Introduction

There is always the desirability of portable operation for all types of electronic systems. A significant market advantage can be obtained for virtually any electronic function by merely providing the same functionality of a wired system in a wireless implementation [1]. Portable televisions, camcoders, and compact disk players have been made available by consumer electronics companies. Cellular phones are going to provide virtually unlimited access for voice communications; and laptops, notebooks and palmtops are the fastest growing types of computers. In the next few years, portable multimedia terminal will come into being, which will be capable of providing speech communication, data transfer, handwriting recognition, and high-quality, full motion video. Through the multimedia terminal, individual users will have portable access to fixed computing facilities [2].

Each of these technologies relies on VLSI for cost and power-consumption effective implementation [3]. Complicated digital processing, such as audio/video compression and decompression will be used. Since the signals to and from I/O devices, such as magnetic recordings, microphones, speakers, CCD's, LCD's, and wireless modulators and demodulators, are analog, the use of analog processing will continue, however, to be confined mainly to the digital-analog interfaces [4]. Most of the chip area will be dedicated to

digital applications. The chip power consumption will originate mainly from the digital circuits. Given sufficient complexity, even CMOS dissipation levels become excessive especially where high frequency is involved. It is necessary to optimize the VLSI-technology for low-power operation of the digital circuits [5]. This situation creates a great challenge for analog circuit designers.

The power of a CMOS digital circuit can be optimized by minimizing the expression $Power=CV_{dd}^2f$. The capacitance C can be reduced by scaling down the MOS device, but not without a boundary. A limitation on the reduction of C is set by the interconnection capacitance that ceases to scale below 1μm due to photolithographic considerations. Reducing V_{dd} is the most strongly suggested way to achieve the power minimization. The *power* should go down quickly with V_{dd} because it is proportional to the square of the supply voltage. On the other hand, the reduction of V_{dd} will cause speed loss. The reason is that a gate has a longer delay for a lower supply voltage. Moreover, the speed loss can be compensated for by using parallelism. Suppose that the gate delay is doubled because of the supply voltage reduction, two paralleled gates can then be used to keep the throughput the same as that before the supply voltage is reduced. Although C will be doubled due to the double of the hardware, f will be halved as only half the throughput is provided by every device. Therefore, Cf is kept constant. This principle shows that parallelism can be used as much as possible for supply voltage reduction without reducing the throughput. Unfortunately, some overhead hardware is needed to realize the parallelism, which makes If increase with the degree of parallelism. As a result, there is an optimum supply voltage for achieving lowest power consumption. This voltage is found to be about equal to 1.5 and 1 volts for a 2μm and a 0.6μm process, respectively [2]. With such supply voltages, a high-

gain high-speed operation amplifier is unobtainable.

To keep the static power consumption low and the digital noise margin high, the threshold voltage will not be scaled down with the supply voltage [5]. The combination of low supply and high threshold voltages diminishes the allowed voltage swings in analog circuits which results in worsened dynamic range. The analog switch characteristics are also degraded [6].

Adequate yield and low cost with higher digital complexity will be achieved by process simplification. This again adds to the burden of analog design since special options included in today's processes to assist analog design (e.g. second polysilicon layer for implementing linear floating capacitors) may soon become a historic luxury. Still worse, the increasingly high performance of the digital signal processor must be matched by its analog interface (e.g. speed, dynamic range, linearity etc.) and this enhanced performance must be achieved in the noisy environment of digital circuits [5].

In summary, future analog circuits will need to perform better in nosier conditions and with less optimum, digitally-oriented, CMOS process.

1.1 Problem Statement

Some recent innovative work to lower the power supply to 3.3V or lower are indicating possible solutions to this dilemma. The insufficient-dynamic-range problem due to down-scaled supply voltage is avoided by using current, instead of voltage, to represent the signal [7]. This change from voltage to current mode creates also the potential for speed improvement because stray-inductance effects are less severe in low-impedance circuits than stray-capacitance effects in high-impedance circuits. High accuracy is obtained by so

called *switched-current (SI) technique*, using dynamic calibration to alleviate the error due to elements mismatch [8].

The SI technique couples itself well with the down-scaled CMOS technology, where transistors with a high cut-off frequency are available, meaning a high calibration speed. Another advantage of this technology is that highly-linear capacitance is not needed for high accuracy analog signal processing. Alternatively, accuracy has been traded with speed in Σ–Δ modulators using oversampled techniques to achieve performance orders of magnitude higher than traditionally associated with analog limitations [9]. The challenge and the gains are clear for the designer who can manage the extra demands on analog performance with diminishing resource of digitally-motivated VLSI process development. This thesis study addresses this challenge by making full use of the salient properties of switched-current circuits to improve the speed of the circuit with power supply voltage of 3.3V, or lower. New structures for high-performance, low-voltage/low-power current-mode data acquisition and conditioning circuits, such as, analog-to-digital converters (ADC's, or A/D converters) and sample and hold (S/H) circuits will be developed for mixed-signal IC's for future portable equipments.

1.2 Previous Works

A number of outstanding low-power pipelined CMOS ADC's have been reported recently, such as a 10-b, 20MS/s, 35mW ADC [10] in 3.3V supply voltage and 1.2μm process; a 10-b, 20MS/s, 50mW ADC [11] in 5V supply voltage and 1.2μm process, and a 10-b, 40MS/s, 85mW ADC [12] in 2.7V supply voltage and 0.8μm process. They are implemented with switched-capacitor techniques in which the accuracy and speed are limited by

(1) the accuracy of the capacitance matching; and (2) the use of high-gain amplifiers which have two or more stages for error reduction. It would be very difficult for them to increase the accuracy above 10 bits without having a substantial increase in area and power consumption. On the other hand, further reduction of the supply voltage is virtually impossible. Some reported current-mode Adds achieve low supply voltage, including a 12-b, 2V Current-Mode Pipelined A/D Converter Using a Digital CMOS Process [13], and a 1.5V Video-Speed Current-Mode Current-Tree A/D converter [6]. The design in [13] achieves only a sample rate of 1MS/s, but its power consumption is 60 mW. The design in [6] has a sample rate 20MS/s, but it uses current mirrors to create equal current sources. Its accuracy depends on element match and is limited to about 8-b.

For some applications, a sample rate higher than 50 MS/s may be needed. An effective bipolar solution using the bridge-diode S/H circuit has been provided [14]. In CMOS technology, an open-loop S/H using switched-capacitor has been demonstrated in a 8 b ADC with a sample rate of 85 MS/s [15], while closed-loop S/H circuits for 10 b at 50 MS/s [16] and 100 MS/s [17] have also presented. However, they have either high power consumption or low accuracy.

1.3 Research Tasks

The objective of the thesis research is to develop new generation of high-performance, low-power/low-voltage current-mode circuits. The emphasis is placed on the development of S/H circuits and ADC circuits for mixed-signal IC's in future portable equipment.

A simple, yet high-speed, high-linearity current copier with a compensator can be used as a S/H circuits. The compensator can reduce the errors due to the capacitive current and the increase of high-frequency linearity of the current copiers. Thus, the current copier can process rapidly varying continuous-time signal and acts as a high-performance S/H circuit. In this task, two types of S/H circuits are developed: a V-I converter with S/H function, and an oversampled S/H circuits.

Low speed of the switched-current ADC is not due to physical limitations, but non-optimized circuit structure and the use of switches with large stray capacitance in the signal path. In this task, new designs for high speed current copier and current switches with much smaller stray capacitance are presented. Based on the developed high-performance current copiers, the initial target performance of the proposed parallel ADC is set at an accuracy of 12 bits and 0.1mW/bit/MHz power consumption in 2-3V supply voltage with orbit standard SCDN20 2μm digital CMOS process. The performance can be further improved with better technology, such as 1.2μm or 0.8μm process. The major concern is higher accuracy, higher speed, and lower power. In addition, the approach must be compatible with modern digital CMOS process.

The circuits developed in this study will meet the design requirement not only for portable equipments, but also for video signal processing, such as HDTV, high-frequency digital communications, and waveform acquisition/instrumentation. This research will demonstrate that this development is not merely an academic curiosity, but an important practical technology for the future.

1.4 Thesis Organization

This thesis is organized as follows: Chapter 2 reviews the previous work in the design of current mirrors, current copiers, and some existing current-mode circuits. Chapter 3 presents the developed high-performance current copiers. Based on the developed high-performance current copiers, the designs of both S/H circuits and ADC circuits are discussed in Chapters 4 and 5, respectively. Finally, conclusions and future research are given in Chapter 6.

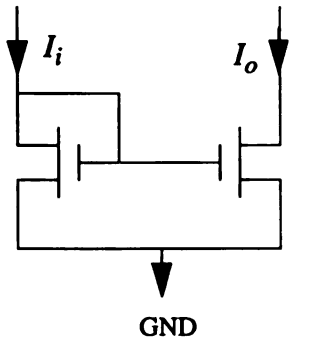
Chapter 2

Background

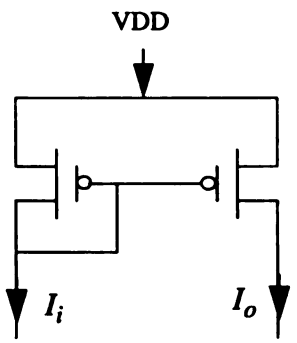
Current copier is the basic building block of Switched-Current (SI) circuits. It is developed to alleviate the errors of conventional current mirrors caused by fabrication tolerance. Section 2.1 reviews the current mirrors and their error effects, while Section 2.2 outlines the existing current copiers and the difficulties for achieving high speed and high accuracy. Finally, Section 2.3 discusses the existing SI circuits related to this study.

2.1 Current Mirrors

A current mirror, as shown in Figure 2.1, is a circuit that reproduces its input current. The output current I_0 equals the input current I_i if its two transistors are identical and their output impedances are very high. In practice however, it is virtually impossible to obtain identical transistors due to the following error effects: (1) Channel length modulation (r_o); (2) Aspect ratio mismatch (W/L); (3) Threshold voltage mismatch (V_T), and (4) mobility mismatch (μ). Note that the error due to the channel-length modulation can be reduced by using some circuit technologies presented in [18], while errors (3) and (4) can be alleviated when large-size transistors are used. On the other hand, the error due to the aspect



(a)



(b)

Figure. 2.1: Simple Current Mirrors: (a) NMOS; and (b) PMOS.

ratio mismatch can be reduced by using long-channel transistors [19], but it is penalized by limiting the speed performance particularly when high accuracy is required. As a result, the ADC design using current-mirrors have been limited up to 8 bits when power and area optimizations are considered [19,20], and up to 20MHz for the operating speed [6].

2.2 Current Copiers

Current copiers perform the same functions as current mirrors, but they alleviate the error effects in current mirrors [8]. Figure 2.2 illustrates the basic structure of a current copier. The input current I_{in} is reproduced by turning on switches S_1 and S_2. The circuit will settle to the state referred to as **calibration state**, where the capacitance C_1 has a voltage necessary to support the drain current I_{D1} that is equal to I_{in}, plus the bias current. Once the required settling accuracy is reached, the circuit can be turned into the **operation state** by opening S_1 and S_2, and closing S_3. Thus the input current source I_{in} is free for other uses, and a load current I_{out} which is equal to I_{in} can be sunk by transistor M_1. The transistor M_1 is called **a current-storage transistor**. The current I_{out} can be reproduced from the input current I_{in} without the need of well-matched elements. However, the current copier is not free of errors. It suffers from two errors due to (1) the nonzero output conductance g_{o1} of M_1; and (2) the clock feedthrough of S_2 [8].

The nonzero output conductance g_{o1} results from the channel length-modulation effect [18] and the drain-gate capacitive coupling of transistor M_1 [8]. The former effect reflects the fact that the depletion region in the channel of a MOS transistor stretches itself toward the source when the drain-source voltage V_{DS} increases. This means that the distance that a carrier from the source must pass to reach the drain is shorter for a higher drain-source

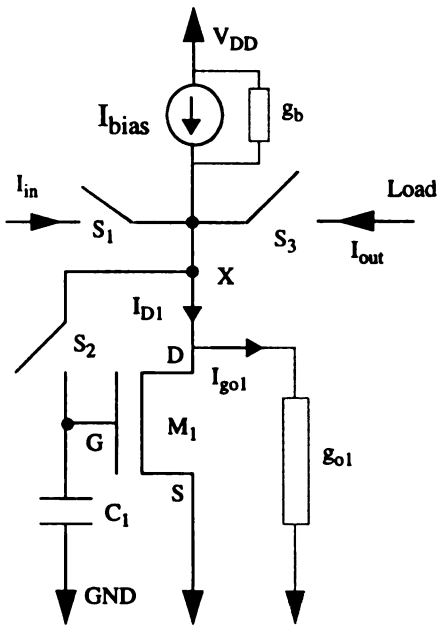


Figure. 2.2: Basic Structure of a Current Copier.

voltage difference than for a lower one, resulting in an increase of the drain current with V_{DS}. On the other hand, the drain-gate capacitive coupling may also cause the nonzero conductance when the gate of a MOS transistor is floating, as it is the case when a current-storage transistor is in the operation state. As the small-signal equivalent circuit shown in Figure 2.3, any variation on the drain voltage ΔV_D will couple to the gate and cause a gate voltage variation ΔV_G. As a result, a change of the drain current incurs through the transconductance g_{m1}. The output conductance can be expressed as $g_{oc}=C_{DG}(C_{DG}+C_1)^{-1}$ $g_{m1}\approx C_{DG}\tau^{-1}$, where $\tau=C_1 g_{m1}^{-1}$ is the time constant of the current copier. This relation reveals that for high-speed operation, i.e. small τ, the current copier will have a large output conductance.

The clock feedthrough error effect [21] is caused by the charge stored in the conducting channel of a MOS transistor. As shown in Figure 2.4, one end of the switch is connected to the gate node G of the transistor M_1. During the turn-off transient, the gate voltage V_g of the switch goes down, forcing the charge in the switch channel to leave. Some charges, in the channel of the switch will dump onto the gate G. The dumped charge changes the voltage across the capacitance, causing the current I_{out} sunk by M_1 in the operation state to be different from I_{in}. Note that the charge stored in the switch-transistor channel and the sharing of the charge by the both ends depend on the voltage V_G, which changes with the input current, thus, the error current will depend on the input current. In other words, the error current is not just an offset [22-24], but also causes gain error and distortion of the current copier.

A number of current copiers have been proposed recently to alleviate the error due to the output conductance g_{o1}, including cascode approach [8] and negative feedback ap-

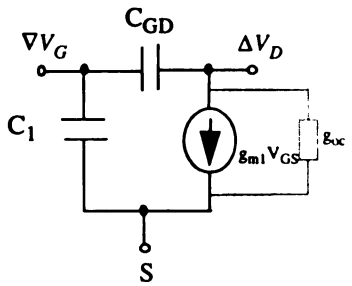


Figure. 2.3: Output Conductance Resulting From C_{GD}

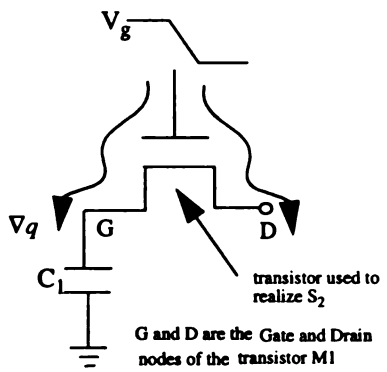


Figure 2.4: Charge Dumped Onto C_1 Through Switch S_2.

proach [25,26]. A cascode current source has an output impedance much higher than a simple one. This technique has been widely used to design high-speed and high-gain operation amplifiers [18], and to separate the drain of a current-storage transistor M_1 from the output/input node X to alleviate the effect of the input current on the drain potential. On the other hand, the latter approach separates the gate of the current-storage transistor from node X. This structural difference results in important performance difference of the copiers.

2.2.1 Cascode Current Copiers

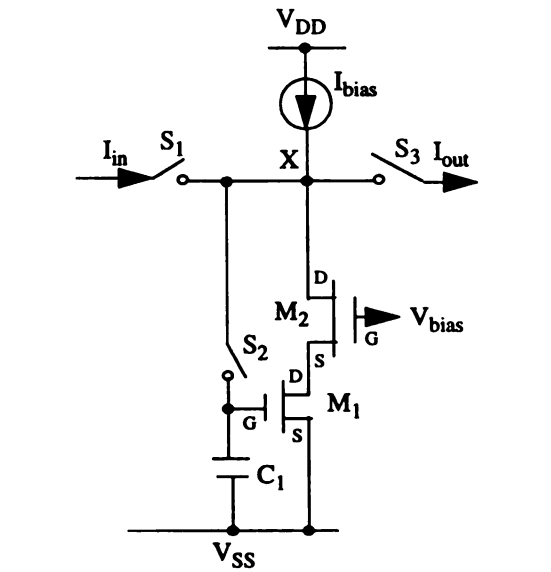
Figure 2.5(a) illustrates a basic cascode current copier [8], where the current-storage transistor M_1 in Figure 2.2 is replaced by a cascode structure with M_1 and M_2. Due to the cascode structure, the input current has a much smaller impact on the drain voltage of M_1 in this copier than that in the basic current copier shown in Figure 2.2. The drain voltage of transistor M_1 in Figure 2.2 is equal to the gate voltage during calibration and the variation of the error current I_{go} due to the output conductance is related to the input current variation and can be expressed as

$$\Delta I_{go} \approx [(g_{o1}+g_b)/g_{m1}]\,\Delta I_{in} \qquad (2.1)$$

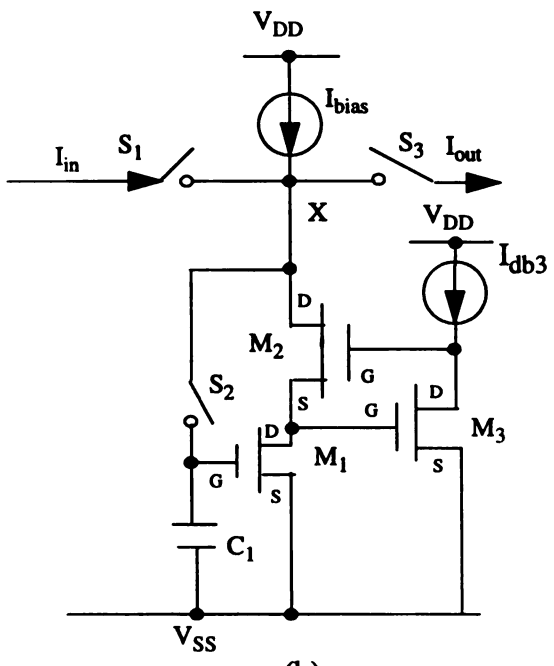
where g_b is the output conductance of the bias current source. In addition, due to the cascode structure, the drain voltage variation of transistor M_1 can be reduced by a factor of A_2, where $A_2=\Delta V_{D2}/\Delta V_{S2}\approx g_{m2}/(g_{o2}+g_b)$ is the voltage amplification of the common gate amplifier consisting of transistor M_2 and the bias current I_{bias}. Thus, the variation of the error current I_{go} can be written as

$$\Delta I_{go} \approx [g_{o1}/(g_{m1}A_2) + g_b/g_{m1}]\,\Delta I_{in} \qquad (2.2)$$

This implies that the error can be reduced by a factor A_2, if g_b is kept small. Therefore, to



(a)



(b)

Figure 2.5: Cascoded Copiers: (a) Simple; and (b) Regulated.

keep a small g_b, a cascode current source is needed for the bias current source.

The main disadvantage of the cascode copier is the use of the headroom transistor M_2, which reduces the gate available voltage swing of transistor M_1 and increases the requirement on the supply voltage. As can be seen in the later discussion.

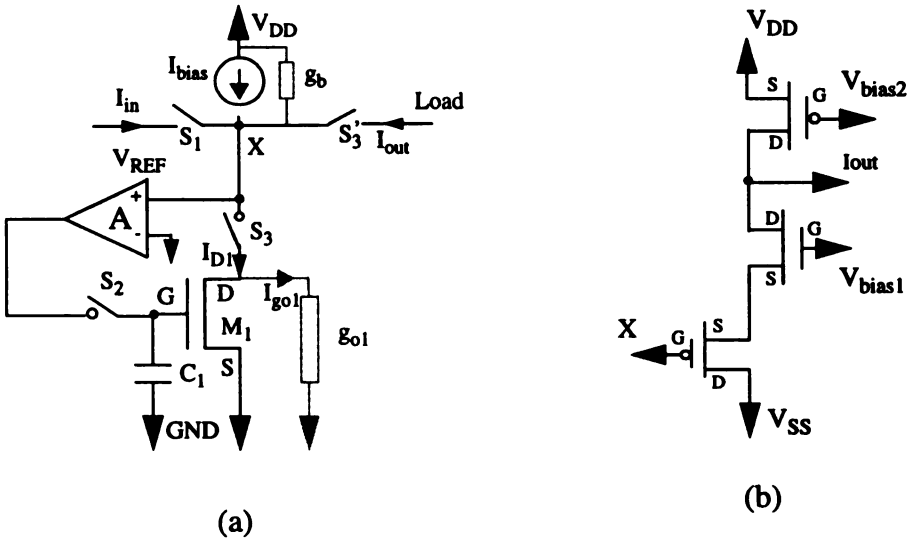
The accuracy of the simple cascode copier and its need of high supply voltage can be improved by a regulated cascode copier, as shown in Figure 2.5(b) [27], where the gate bias voltage of M_2 in Figure 2.5(a) is replaced by an amplifier consisting of M_3 and the bias current source on its drain I_{db3}. The input of the amplifier is connected to the drain of the current-storage transistor M_1. Thus, its drain voltage variation with respect to the input current is further attenuated by the voltage gain of the amplifier. If the voltage gain of the amplifier is A_3, the error current due to the output conductance can be expressed as

$$\Delta I_{go} \approx [g_{o1}/(g_{m1}A_2A_3) + g_b/g_{m1}]\ \Delta I_{in} \qquad (2.3)$$

In addition, the drain voltage of M_2 changes with its gate voltage. In other words, the transistor can work at the just-saturated bias point for all input currents. This will reduce the power supply voltage. This point is made clear in the later discussion. In fact, as a large error attenuation is provided by amplification A_3 and the main error is due to charge injection effect, M_1 can be designed to work in the linear region to further reduce the power supply voltage, without loss of its accuracy [27].

2.2.2 Negative Feedback Current Copier

Figure 2.6(a) illustrates a negative feedback current copier. The structure provides not only a constant drain voltage for the storage transistor, but also for the bias current source at the same time. Thus, the bias can be implemented as a simple current source. As



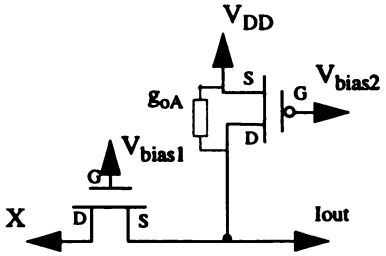


Figure. 2.6: INFCC: (a) Circuit Structure; (b) Feedback Amplifier with a High Input Impedance; and (c) with a Low Input Impedance.

no headrooms are used, the copier can be operated using low supply voltage. In fact, unlike the basic copier of Figure 2.2, where, in the operation state, the transistor M_1 has the lowest drain voltage for the largest drain current, the current-storage transistor in a negative feedback copier has always the same drain voltage for all drain current. This feature provides a negative feedback copier the ability to be operated with the lowest power supply. Since the current-storage transistor, together with the input current source, constitutes an inverter, the copier is referred to as an Inverter Negative Feedback Current Copier, or INFCC. The performance of an INFCC highly depends upon the type of feedback amplifier it implements. For simplicity, the INFCC with the amplifier in Figure 2.6(b) is referred to as INFCCI [25], while the INFCC with the one in Figure 2.6(c) is called INFCCII [9].

During calibration the switch S_2 is on. The variation of the drain voltage of M_1 is related to the variation of its gate voltage and the voltage gain of the amplifier as $\Delta V_{D1}=\Delta V_{G1}/A$. Thus, the error currents for INFCCI and INFCCII can be represented as

$$\Delta I_{go} \approx [(g_{o1}+g_b)/g_{m1}A]\ \Delta I_{in} \qquad (2.4a)$$

$$\Delta I_{go} \approx [(g_{o1}+g_b)/g_{m1}A + g_{oA}/g_{m1}]\ \Delta I_{in} \qquad (2.4b)$$

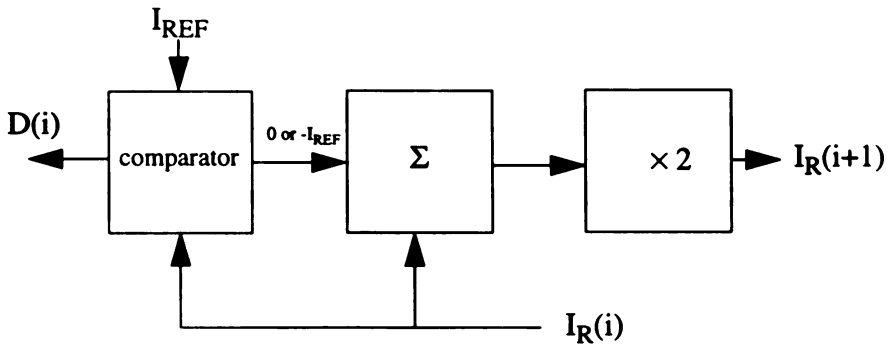
(2.4) confirms that the error due to the output conductance of the bias-current source is reduced at the same time with that of the current-storage transistor. The second term in (2.4 II) stands for a new error of INFCC II, because the amplifier has an input current changing with I_{in}. For high accuracy, the output conductance of the amplifier g_{oA} must be small, and a cascode current source has to be used to generate the bias for the amplifier. For the case shown in Figure 2.6(c), the error of the copier can be quite large.

2.3 Switched-Current Circuits

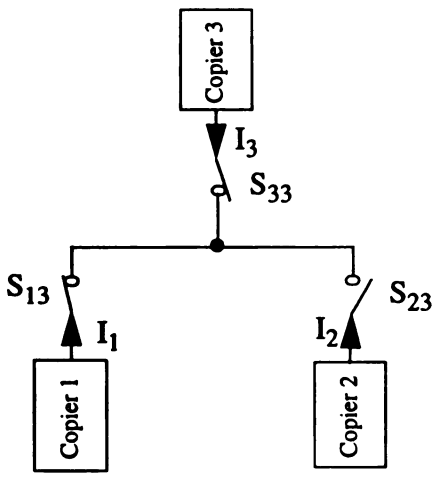
Current copiers are the basic building blocks in SI circuits. This sub-section presents the designs of some SI circuits, such as, data converters and sample/hold circuits.

2.3.1 Switched-Current Converters

Recently, SI technique has been applied to design high-resolution analog-to-digital converters [3,25,27]. An accuracy beyond what is possible using matched capacitor or resistor networks can be reached by a simple inexpensive digital fabrication process. Figure 2.7(a) shows the functional diagram of a bit cell in a cyclic analog-to-digital converter. The bit cell produces one bit digit word D(i) and the output residue current $I_R(i+1)$ from the input residue current $I_R(i)$. The core unit of the bit cell that determines the accuracy is the $\times 2$ unit, called a residue amplifier, which doubles the residue current. In SI technology, the unit is implemented using current copiers as shown in Figure 2.7(b). It consists of 3 current copiers and the switching states for the copier's operation are shown in Figure 2.7(c). Recall that the copier in the operation state outputs the current, while receiving the current in the calibration state. The current stored in *Copier 3* is copied to *Copier 1* in the first cycle, i.e., $I_1=I_3$, and to *Copier 2* in the second cycle, i.e., $I_2=I_3$, then the currents stored in both *Copiers 1* and *2* are copied back to *Copier 3* in the third cycle, where $I_{3(new)}=I_1+I_2=2I_{3(old)}$. This concludes the operation for the computation of the residual current for the next bits. In the above simplified explanation, the operation of a possible subtraction of a reference current from the amplified residue is omitted. The subtraction can be done separately [25] or at the same time as the residual amplification [27]. For the former case one more clock phase will be needed.



(a)



(b)

	1	2	3
Copier 1	Calib.	Idle	Oper.
Copier2	Idle	Calib.	Oper.
Copier 3	Oper.	Oper.	Calib.
S_{13}	ON	OFF	ON
S_{23}	OFF	ON	ON
S_{33}	ON	ON	ON

(c)

Figure 2.7: Cyclic Converter: (a) Block Diagram; (b) SI x2 Unit; and (c) State Table. (Calib - calibration, Oper. - operation.)

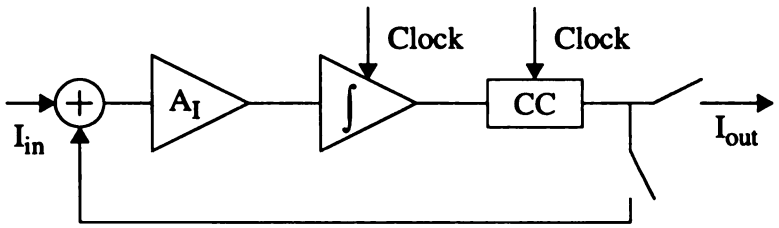
2.3.2 Switched-Current S/H Circuits

For current-mode data acquisition systems, current sample/hold (S/H) circuits are frequently required to freeze fast moving signals before processing by the system. A number of current S/H circuits have been reported [28]. The main problem with the current-mode S/H circuits is that high precision is difficult to achieve due to the signal-dependent clock feedthrough errors. Over-sample techniques have been proposed as an effective method to reduce the errors.

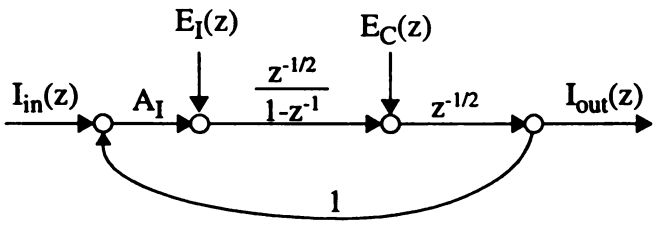
Recently, a design methodology for highly accurate oversampling current S/H circuits with an integrating feedback structure, as shown in Figure 2.8(a), has been proposed in [29]. The circuit consists of a gain stage (with DC gain of A_I), a switched-current integrator, and a current copier (CC). The same clock is applied to both the integrator and the current copier. Consequently, the varying input current is sampled in the integrator while a constant output is held by the current copier. The structure has the similar feature of a Σ–Δ modulator, which achieves a very high linearity by limiting the signal bandwidth. Also, it reduces both thermal noise and systematic errors simultaneously, thus the circuit provides a superb linearity and a very large dynamic range even for continuous-time input currents.

Figure 2.8(b) illustrates an equivalent z-domain signal-flow graph of the integrating feedback structure in Figure 2.8(a), where two potential errors may result from the structure: one is from the integrator while the other from the copier CC. Let $E_I(z)$ and $E_C(z)$ denote the errors resulting from the integrator and the copier, respectively. The output current can be expressed as

$$I_{out}(z) = \frac{-A_1 z^{-1}}{1+(A_1-1)z^{-1}}\left(I_{in}+\frac{E_I(z)}{A_1}\right)-\frac{(1-z^{-1})z^{-\frac{1}{2}}}{1+(A_1-1)z^{-1}}E_c(z) \quad . \qquad (2.5)$$



(a)



(b)

Figure 2.8: An Oversampling S/H Circuit with an Integrating Feedback Structure: (a) Basic Structure; and (b) Signal-flow Graph.

By (2.5), the term $|1-z^{-1}|$ decreases as the oversampling ratio increases and thus reducing the error effect due to $E_C(z)$ from the copier. On the other hand, the increase of the oversampling ratio does not affect the first term of (2.5). Apparently, by (2.5), the term $(E_I(z)/A_I)$ can be reduced significantly if a large gain A_I is used. However, to maintain the stability of the system, the pole has to be located inside of the unit circle. Therefore, $|A_I-1| < 1$, or $0< A_I < 2$, is required. Consequently, there are the needs for a large oversampling ratio to compensate the low gain of the direct path [29] and high-order structures have been suggested to reduce the error $E_I(z)$. Thus, a higher circuit complexity may be needed for such an implementation.

2.4 Discussion

It is believed that switched-current circuits can be operated with low power supply voltage because of small voltage swings associated with low-impedance nodes. Low-cost standard digital processes can be used for manufacturing since precision linear capacitors are not required. Thus, switched-current is ideally suited to mixed-signal IC's in future low-power/low-voltage analog signal processing applications. Since the current copiers are the major building blocks of switched-current circuits, it is desirable to develop high-performance current copiers. Different structures provide a current copier with different performances, including speed, power, capacitance and supply voltage requirement. Reducing the supply voltage is greatly desired to reduce the power consumption and cost of mixed-signal chips. However, there is not enough study dedicated to low- voltage performance of current copier circuits. No clear answer for the important question, such as, what sets the limit for supply voltage of different designs can be readily found in the literatures.

In practice, with the realistic switches where the stray effects are not negligible for low supply voltage, the speed performance may be degraded significantly. Thus a thoroughly study of the effects and structures which minimizes the effects will be handled in the next chapter. Several design issues on high accuracy and high speed current copiers are investigated.

Chapter 3

High Performance Current Copiers

The performance of SI circuits is mainly determined by the current copiers they employ. Therefore, high-performance current copiers are desired. The developed current copiers should be simple yet high-speed and high-accuracy, and can be used for low-power/ low-voltage analog signal processing applications. This chapter addresses the design issues and presents the developed current copiers and their performance analysis.

3.1 Performance Analysis

Current copiers suffer from two major effects which are due to the non-zero output conductance and charge feedthrough. Several circuits have been presented in the previous chapter to reduce the error due to the non-zero output conductance. The error effect due to charge feedthrough can be alleviated by increasing the gate capacitance C_1 [21]. An open question is: *how to make a copier with a larger gate capacitance to be operated at high calibration speed?* More specifically, the calibration speed of the copier in Figure 2.2 is determined by the time constant

$$\tau = C_1/g_{m1} \tag{3.1}$$

where g_{m1} is the transconductance of the transistor M_1. In fact, by (3.1), a slow calibration speed will result if a large capacitance C_1 is employed. On the other hand, the time constant can be kept small with the use of a large C_1 if a relatively large g_{m1} is chosen. The following important issues will be addressed: *what is the effect of g_{m1} on the accuracy*? and *what is the limitation on the choice of C_1, if a small τ is allowed by charge feedthrough effect*? *Is the charge injection error effect the main obstacle for high performance?* and *Does the stray effects limit the calibration speed?*

3.1.1 Charge-Feedthrough Error Effects

Consider the gain-error of a current copier defined as

$$\varepsilon = \frac{d(\Delta I)}{dI_{in}} \tag{3.2}$$

where $\Delta I = I_{out} - I_{in}$ is the error current of the copier. The error current due to charge Δq dumped by switch S_2 onto the gate capacitance C_1 can be written as

$$\Delta I = \frac{\Delta q}{C_1} g_{m1} \tag{3.3}$$

By (3.2) and (3.3), the gain-error ε can be re-written as

$$\varepsilon = \frac{\frac{d(\Delta I)}{dI_{out}}}{1 + \frac{d(\Delta I)}{dI_{out}}} \tag{3.4}$$

with

$$\frac{d(\Delta I)}{dI_{out}} = \frac{\Delta q}{C_1(V_G - V_{T0})} + \frac{1}{C_1}\frac{d(\Delta q)}{dV_G} \tag{3.5}$$

When (3.5) was derived, the following relation

$$g_{m1} = \beta(V_G - V_{T0}) = \sqrt{2\beta I_{out}} \tag{3.6}$$

has been used, where β is the transconductance constant and V_{T0} the threshold voltage of the current-storage transistor M_1. From (3.4) and (3.5), $|\varepsilon|$ can be kept small if we chose C_1 and V_G-V_{T0} to be sufficiently large. As a result, by (3.6), g_{m1} must be kept large. As mentioned, for relatively large C_1 and g_{m1}, by (3.1), the time constant τ can be kept small. Thus, *there is no direct impact on speed* τ *and accuracy* ε *with the error effect due to the charge feedthrough.* However, as far as the power consumption is concerned, the choice of C_1 is critical. More specifically, by (3.1) and (3.6), we have

$$\tau = \frac{C_1(V_G - V_{T0})}{2I_{out}} \tag{3.7}$$

As the minimal value of $C_1(V_G$-$V_{T0})$ will be limited by the required accuracy given by (3.5) or the *signal-to-noise ratio* (SNR) of the copier cell [30], the time constant τ can be made small only by choosing a large current I_{out}, resulting in a large power consumption.

Assume that C_1=*2pf*, V_G-V_{T0}=*0.5V*, and τ=2ns, by (3.7), we have I_{out}=250μA. For a supply voltage of 3.3V, the power consumption for a current copier is *0.825mW*. Therefore, the total power consumption of a 10-bit ADC which contains 20 current copiers is approximately 16.5mW. Assume that the settling time of the copier is 7τ and the residual amplifier of the ADC requires at least two calibration cycles. Thus, the sample rate of the ADC is 1/14τ, or 35.7 MSamples per second (MS/s). The above assumptions are all achievable. Unfortunately, existing pipelined ADC's have not yet reached the estimated power consumption level with this sample rate, mainly due to the effect of other time constants which make the calibration slower than that predicted. *This result reveals that charge injection is not the main obstacle for high performance, but the stray effects that limit the calibration speed.* The limitation on the choice of C_1 from SNR requirement will be discussed

later.

The choice of C_1 is also limited by the on-resistance of the switch S_2 and the supply voltage. To make the clock-feedthrough error small, a small transistor should be used for the switch S_2. The on-resistance r_{S2} of the switch S_2 is usually larger than 10KΩ due to the small size of the switch and the low bias voltage for low supply voltage applications. This low conductance together with the low power supply will limit the maximum current that is available to charge the capacitance C_1, as the shown by equivalent circuit Figure 3.1. The equivalent circuit is obtained from Figure 2.3 for the case V_{DD}-V_X < V_{ST}, where V_X is the voltage of node X and V_{ST} is the saturation voltage of the bias current source in Figure 2.3. During the transient, the voltage V_X approaches V_{DD}, forcing the transistor which implements the bias current source to operate in the triode region and resulting in a low output impedance. The transient state occurs when I_{in}-I_{D1}-I_{bias} > (V_{DD}-V_{G1}-V_{ST})/r_{S2}. As the time moves on, the current I_{D1} will approach I_{in}, making the current (I_{in}-I_{D1}-I_{bias}) flowing through r_{S2} to become smaller. At the end of the transient state, the circuit will go back to the state shown in Figure 2.2. When I_{D1} approaches I_{in}, in Figure 3.1, the time constant is τ_{S2}=$r_{S2}C_1$. Note that, for low supply voltage and small switch, the resistance r_{S2} is generally large. Thus, choosing large C_1 will definitely cause a large time constant τ_{S2}. It will also take much longer transient time from the state in Figure 3.1 to that in Figure 2.2. For example, if r_{S2}=*10KΩ* and C_1=*2pf*, then the time constant τ_{S2}=20ns. This large time constant may cause a longer transient response when the copier is driven into the state shown in Figure 3.1 with a large pulse input current. The amplitude of the pulse input current should be limited to keep the transient short.

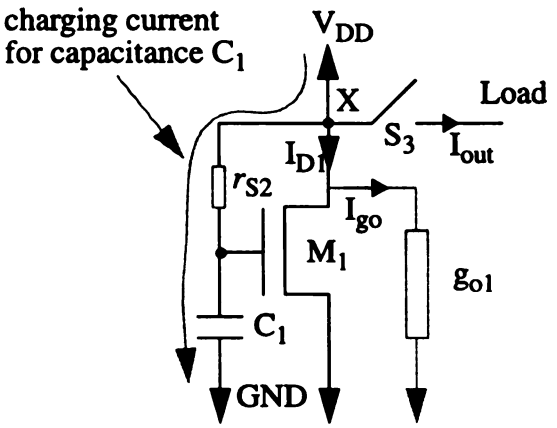


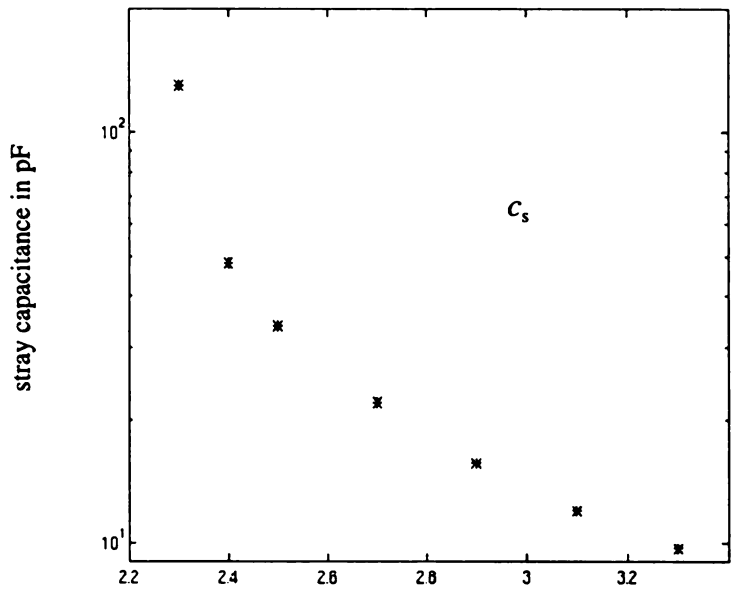
Figure 3.1 Equivalent Circuit of the Copier for V_{DD}-V_X<V_{ST}.

3.1.2 Stray Effects

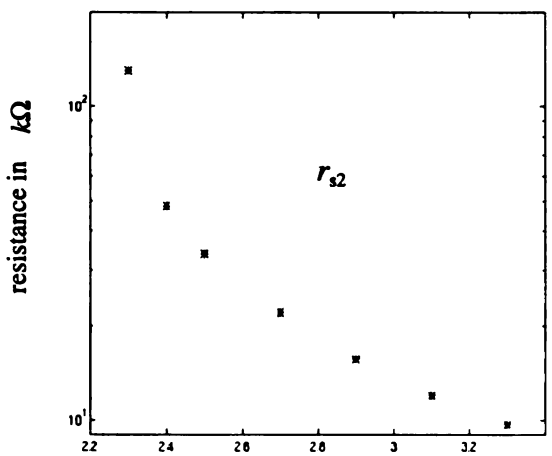
When an ideal switch is employed in the basic copier, the settling time of the copier is determined solely by the time constant τ. However, this may not be valid when low supply voltage and non-ideal switches with relative high threshold voltages are employed. Three switches are includes in the basic copier in Figure 2.2: S_1 and S_3 are current-steering switches and S_2 is a sampling switch. When S_1 must carry out a current equals to the input current, its area cannot be too small, and its stray capacitance cannot be ignored. On the other hand, S_2 must be kept small in order to minimize the charge injection error, and it may have large stray resistance. As a result, both stray capacitance and resistance generates a large time constant which will definitely affect the speed performance. The stray effects in various copiers are analyzed as follows.

Basic Current Copier

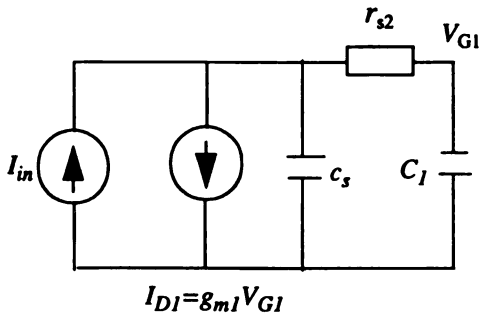
Figure 3.2 plots the stray capacitances, c_s, of both S_1 and S_3 and the stray resistance, r_{s2}, of S_2 for various supply voltages. The switches are implemented with CMOS switches, where the width of the PMOS transistor is twice that of the NMOS transistor. The width of switches S_1 and S_3 is chosen in such a way that the voltage drop across them is about 0.2V when a current 300μA flows through them. The widths of both NMOS and PMOS transistors are 6μm. The stray capacitance can be expressed as $c_s=C_{ox}(W_1+W_3)$, where C_{ox} is the oxide capacitance, and W_1 and W_3 are the total widths of S_1 and S_3, respectively. (The total width of a switch is the sum of the widths of the NMOS and the PMOS transistors.) In Figure 3.2(a), the stray capacitance increases as the supply voltage decreases, because the switch width has to be increased to keep the capacity of the switch to carry a current



(a)



(b)



(c)

Figure 3.2: Performance Analysis: (a) Effect of Power Supply Voltage on the Stray Capacitance c_s; (b) on the Resistance r_{s2}; and (c) Small Signal Linearized Model.

unchanged with a lower bias voltage. In Figure 3.2(b), the stray resistance r_{s2} of the switch S_2 as a function of the supply voltage, where the input voltage of the switch is assumed to be 1.6V. The resistance r_{S2} goes up as the supply voltage goes down, which reduces the bias voltage of the switch. Therefore, a large time constant may result for low-voltage supply applications.

To simplify the performance analysis, a small-signal linearized model, as shown in Figure 3.2(c), is employed. It should be noted that large change of the transistor currents may occur during the transient period. However, it occurs only during a very small fraction of the entire transient period. The currents are in near steady state in most of the period. Thus, the impact of the stray effects on the settling time can be studied from the small-signal linearized model. Solving the nodal voltage equations, one obtains a characteristics equation

$$s^2+(1+c_s/C_1)\tau_s^{-1}s+\tau_s^{-1}\tau^{-1}=0 \qquad (3.8)$$

where $\tau_s=c_s r_{S2}$ is the time constant introduced by the stray effects. Since the settling speed of system (3.8) is determined by the maximum absolute value of the real parts of the roots, the system can have a speed equivalently equal to the one determined by the time constant $2\tau_s/(1+c_s/C_1)$. Compared to the speed with ideal switches, the speed degradation can be represented as

$$D_s=2r_{s2}g_{m1}/(1+C_1/c_s) \qquad (3.9)$$

where D_s is speed ratio between using ideal and CMOS switches. From Figures 3.2(a) and 3.2(b), c_s may be in the same range as C_1 and $r_{s2}g_{m1}$ may be much larger than one, thus, great speed degradation may result.

Cascode Current Copiers

The speed performance can be improved by decreasing D_s in (3.9). This can be achieved by reducing either r_{s2} or c_s. Note that, for a given supply voltage, the only way to reduce r_{s2} is to increase its width which will cause the increase of channel feedthrough error. Therefore, it would be better to reduce c_s. The stray capacitance of a switch which is in the saturation region is much smaller than that in the linear region. More specifically, in the saturation region, the stray capacitance on the drain side includes the gate-drain overlap capacitance and the drain-body capacitance. The capacitance is much smaller than the on-state gate-channel capacitance of a switch driven into the linear region. However, a large drain-source voltage drop may occur when the switch is working in the saturation region.

The speed performance for both the simple and self-regulated cascode copiers, as shown in Figures 2.5(a) and 2.5(b), respectively, can be improved by reducing the stray capacitance c_s. Consider the simple cascode copier in Figure 2.5(a). Switch S_3 is removed and substituted by the transistor M_b, as shown in Figure 3.3(a). Two additional pairs of switches are added to control the gates of M_2 and M_b. During the calibration, M_2 is turned on and M_3 is off, where both S_{11} and S_{b2} are opened, and S_{12} and S_{b1} are closed, i.e., the gate of M_2 is connected to V_{bias}, while the gate of M_3 is grounded. In other words, during the calibration, both structures in Figure 3.3(a) and Figure 2.5(a) are exactly the same. The copier cell outputs its current I_{out} through the transistor M_b. More specifically, during copying, M_2 is turned off and M_b is switched on, i.e., both S_{12} and S_{b1} are opened, and S_{11} is grounded and S_{b2} is connected to V_{bias}. Similarly, S_1 can be also substituted by a transistor M_a similar to M_b with its associated switches. As a result, the stray capacitance at node X, denoted as c_X, is reduced significantly due to the substitution of both switches S_1 and S_3.

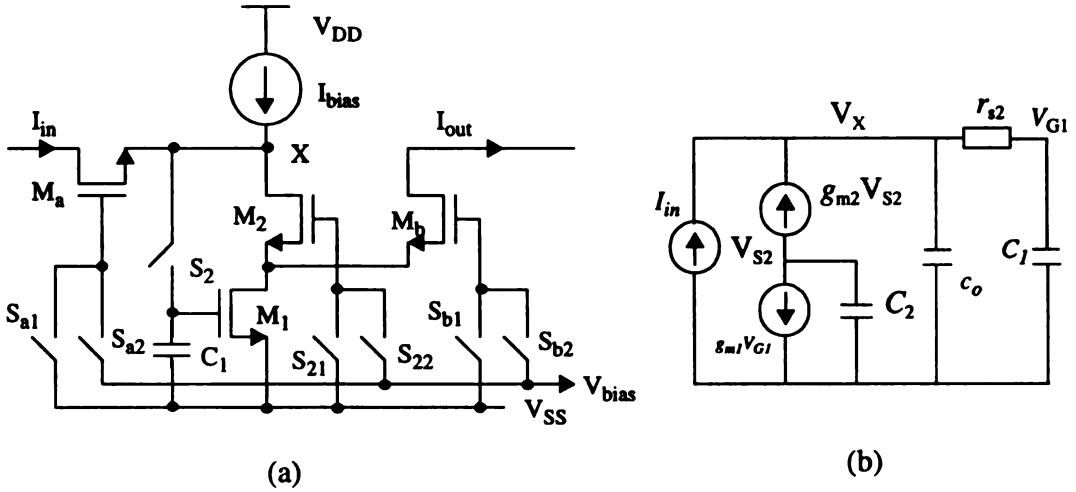


Figure 3.3: Simple Cascode Copiers: (a) Improved Version; and (b) Equivalent Circuit.

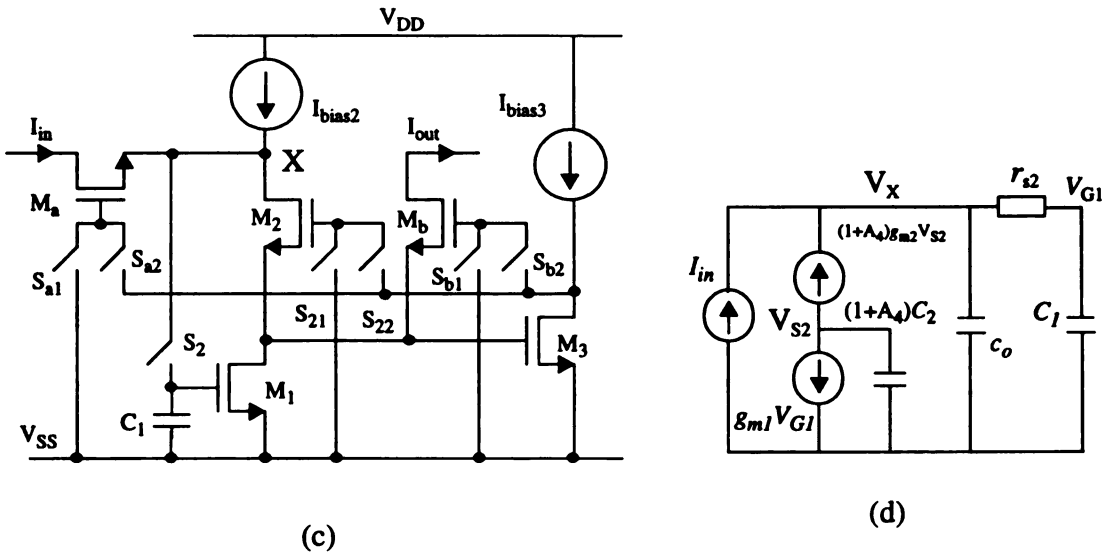


Figure 3.4: Regulated Cascode Copiers: (a) Improved Version; and (b) Equivalent Circuit.

The ratio C_1/c_X is much larger than C_1/c_s in (3.9), and thus the speed performance can be improved even with a large $g_{m1}r_{s2}$. Similarly, the regulated cascode copier in Figure 2.5(b) can be modified as shown in Figure 3.4(a) with its equivalent circuit in Figure 3.4(b).

The use of the headroom transistor M_2 introduces a new time constant τ_2. Figure 3.3(b) shows the small-signal linearized model of the circuit in Figure 3.3(a). One derives the following characteristic equation,

$$s^3 + \frac{1}{a}s^2 + \frac{1}{ab}s + \frac{1}{abc} = 0 \qquad (3.10)$$

with

$$a=[(1+c_o/C_1)+\tau_2^{-1}\tau_s']^{-1}\tau_s'; \; b=[(1+c_o/C_1)+\tau_2^{-1}\tau_s'](1+c_o/C_1)^{-1}\tau_2 ;$$

$$and \; c=(1+c_o/C_1)\tau \qquad (3.11)$$

where $\tau_s'=c_o r_{s2}$. It should be noted that the two copiers have the same characteristics equation. Based on (3.10), the speed performance can be optimized.

Negative Feedback Current Copiers

An INFCC has its current-storage transistor working as an inverter during calibration. As shown in Figure 2.6(a), the inverter consists of the transistor M_1 and the bias current source I_{bias}. If the amplifier of Figure 2.6(b) is used for high accuracy, the node X will be a high impedance node. On the other hand, the gate node G of M_1 is also a high impedance node. This means that INFCCI has two high-impedance nodes in the signal path of its feedback loop. The capacitive loads associated with these high impedance nodes cause large delays of the feedback signal, effecting the stability of the copier. Using the amplifier in Figure 2.6(c), the number of the high impedance nodes can be reduced to one, where node X now becomes a low impedance node due to the low input impedance of the amplifier. Thus, a much better stability can be obtained by INFCCII. A small-signal equivalent

circuit shown in Figure 3.5 is used to analyze the stability property. Using the equivalent circuits, where the stray effects of the switches are ignored, the following characteristic equations are obtained

$$s^2 + (\tau\tau_A)^{-1} = 0 \qquad (3.12I)$$

$$s^2 + \tau_A^{-1}s + (\tau\tau_A)^{-1} = 0 \qquad (3.12II)$$

where $\tau_A = C_A/g_{mA}$ is the time constant of the amplifier. The first equation is for INFCCI and the second for INFCCII. This implies that IFNCCI has a stability problem, while IFNC-CII has a settling speed determined by the time constant $\tau_A' = 2\tau_A$ which is twice the time constant of the amplifier. With the use of short-channel transistors where τ_A' is in the nano- or sub-nano-second range, IFNCCII may have a settling time in the nano-second range. However, as pointed out in Section 2.2.2, an IFNCCII suffers from a accuracy problem due the input current of the amplifier. Thus, neither INFCCI nor INFCCII can achieve the desired speed performance.

3.1.3. Signal-to-Noise Ratio (SNR)

A SI circuit samples and holds an input current signal. Any noise currents introduced with the signal or by the storage transistors undergo the same sampling process. Noise with frequency components above the Nyquist frequency are undersampled and therefore create replicas at base-band frequencies [31]. The major noise current sources in the storage transistors of current copiers are *thermal noise* and *flicker noise*. The analysis and model of such noise sources in current copiers have been studied extensively in [32]. It is well understood that the input current source has also a significant contribution to the total noise. However, the noise caused by the input current source was not included.

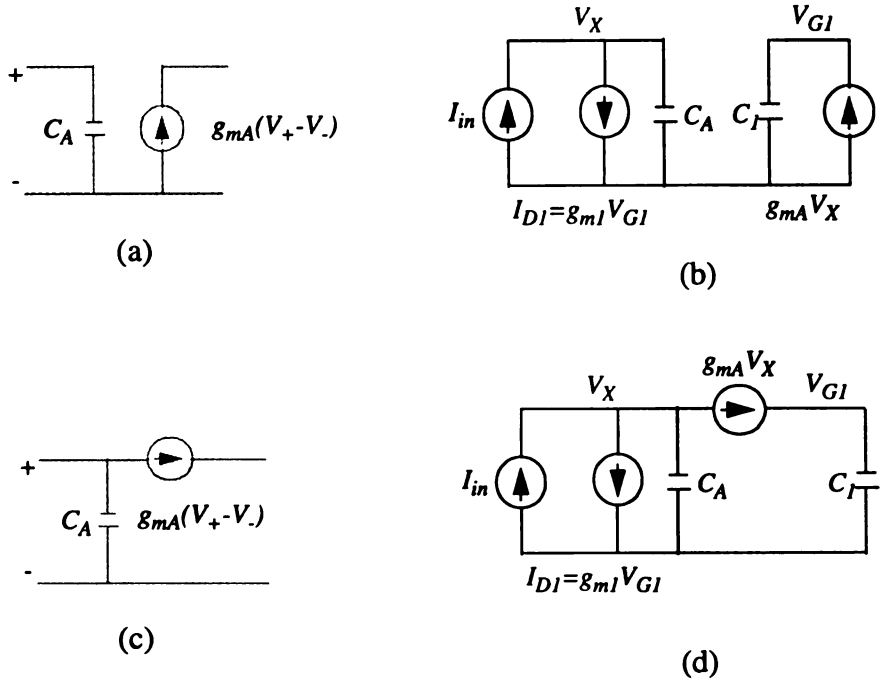


Figure 3.5. INFCC: (a) Amplifier Model & (b) Calibration Model of INFCCI; and (c) Amplifier Model & (d) Calibration Model of INFCCII.

In this study, the input current source is considered in the noise analysis. A pair of current copiers with a noise current sources i_{n1} and i_{n2}, as shown in Figure 3.6, is employed. The copier consists of two storage transistors M_1 and M_2, and the common bias transistor M_b with a noise current i_{nb}. During the hold time of the copier, while the sample and hold noise is being output from the storage transistor, the noise source flows directly to the output. Since the sampled noise and the direct noise have opposite signs, the low-frequency flicker noise can be ignored, and the thermal noise dominates [32]. The variances of the noise currents are respectively expressed as

$$\begin{aligned} \overline{i^2_{n1}} &= \frac{2}{3} m_{th} k T_j g_{m1} \Delta f \\ \overline{i^2_{n2}} &= \frac{2}{3} m_{th} k T_j g_{m2} \Delta f \\ \overline{i^2_{nb}} &= \frac{2}{3} m_{th} k T_j g_{mb} \Delta f \end{aligned} \tag{3.13}$$

where m_{th} is a process-dependent constant which in practice ranges from 1 to 2.5, k is the Boltzmann constant, T_j is the absolute temperature, $\Delta f = g_{m1}/(4C)$ is the noise bandwidth, and g_{m1}, g_{m2}, and g_{mb} are the transconductance of M_1, M_2, and M_b, respectively. Note that the transconductances are

$$g_{m1} = 2\sqrt{\beta_1 I_{D1}},\ g_{m2} = 2\sqrt{\beta_2 I_{D2}},\ \text{and}\ g_{mb} = 2\sqrt{\beta_b I_b} \tag{3.14}$$

where β_1, β_2, and β_b are the transconductance constants of M_1, M_2, and M_b. Since these noise currents are uncorrelated, the variance of the total noise is the sum of the variances in (3.13), i.e.,

$$\overline{i^2_n} = \frac{2}{3} m_{th} k T_j (g_{m1} + g_{m2} + g_{mb}) \Delta f = \frac{2}{3} m_{th} (k T_j / C) \xi g_{mb}^2 \tag{3.15}$$

where

$$\xi = \left(1 + \frac{g_{m2}}{g_{m1}} + \frac{g_{mb}}{g_{m1}}\right) \frac{g_{m1}^2}{g_{mb}^2}$$

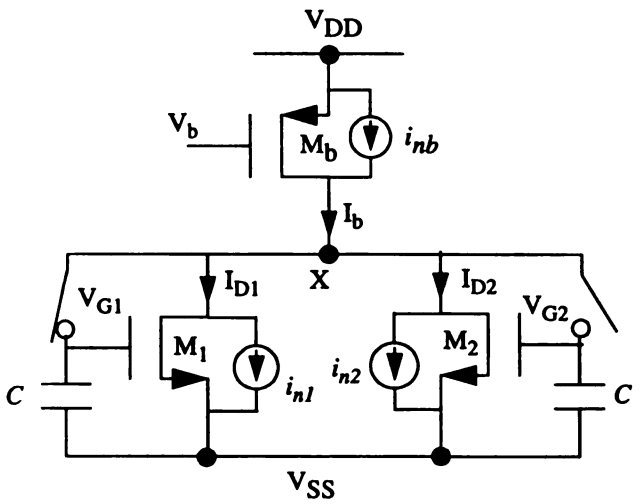


Figure 3.6: A Pair of Basic Copiers with Noise Current Sources.

Apparently, the maximum noise variance occurs when the ξ-value is maximum. Let $m_i=2I_{D1}/I_b-1$ be the modulation index and $\upsilon=\beta_1/\beta_b$ be the normalized transconductance constant. If we assume that $\beta_1=\beta_2$ and $I_b=I_{D1}+I_{D2}$, both drain currents are

$$I_{D1} = (1+m_i)I_b/2, \text{ and } I_{D2}=(1-m_i)I_b/2 \tag{3.16}$$

Therefore, by (3.14)-(3.16), we have

$$\xi = \xi(m_i,\upsilon) = [\upsilon(1+m_i) + \sqrt{\upsilon(1-m_i^2)} + \sqrt{2\upsilon(1+m_i)}\,] / 2 \tag{3.17}$$

Figure 3.7(a) plots the values of ξ for m_i ranged from 0 to 1 and υ=0.25, 2, and 4. Results show that, for small m_i, the noise increases as m_i increase, due to the increase of I_{D1}, causing a larger noise bandwidth. Let $m_{imax,\upsilon}$ denote the modulation index such that $\xi(m_{imax,\upsilon},\upsilon)$ is the maximum value of $\xi(m_i,\upsilon)$. The noise decreases when $m_i > m_{imax,\upsilon}$, due to the reduction of I_{D2}. Figure 3.7(b) shows that the maximum values $\xi(m_{imax,\upsilon},\upsilon)$ for all υ's ranged from 0 to 4 are located between 0.785 and 0.9. It should be noted that, in Figure 3.7(a), the ξ-value decreases as υ decreases. However, it does not imply that the total noise level is low for a small υ, but the noise generated from the bias transistor dominates.

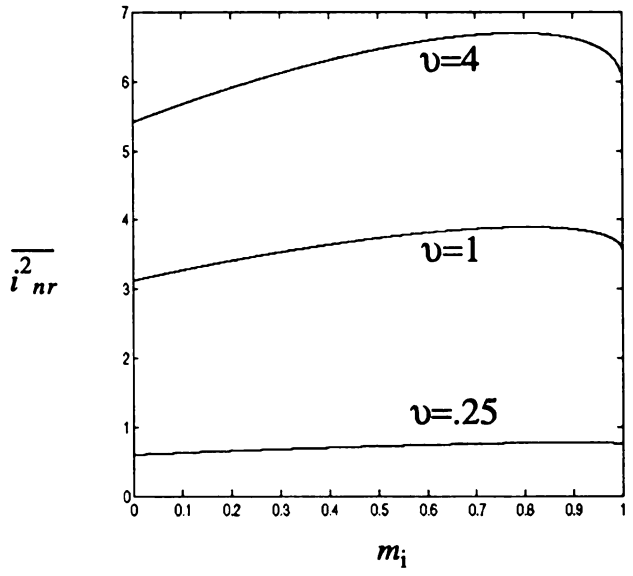
For a sinusoidal with peak amplitude $m_iI_b/2$, the RMS value is $m_iI_b/\sqrt{8}$, and the variance of the signal is

$$\overline{i_s^2} = m_i^2 I_b^2 / 8 \tag{3.18}$$

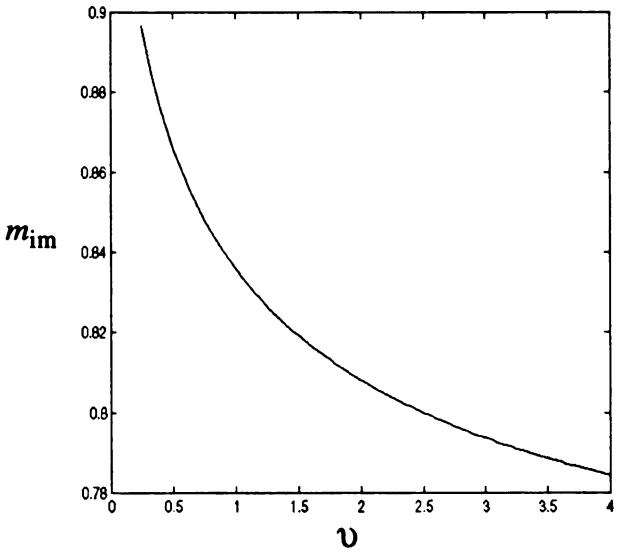
Therefore, with $I_b/\beta_b=(|V_{GSb}|-|V_{Tb}|)^2$, the SNR can be expressed as

$$SNR = 10\,log_{10}[\overline{i_s^2}/\overline{i^2}_n] = 10\,log_{10}\left(\frac{m_i^2(|V_{GSb}|-|V_{Tb}|)^2}{\frac{64}{3C}m_{th}kT_j\xi(m_i,\upsilon)}\right) \tag{3.19}$$

where the worst-case SNR can be obtained by substituting $m_i=m_{imax,\upsilon}$. With the time constant $\tau=C/g_{m1}$ and $g_{m1}=\sqrt{2\upsilon(1+m_i)}\,I_b/(|V_{GSb}|-|V_{Tb}|)$, the SNR in (3.19) can be expressed



(a)



(b)

Figure 3.7: Basic Copier: (a) Noise as a Function of Modulation Index; and (b) Modulation Index for Maximum Noise as a Function of υ.

as

$$SNR = 10\ log_{10}\left(\frac{\tau V_{DD} I_b}{\frac{16\sqrt{2}}{3} m_{th} k T_j}\eta(m_i, \upsilon)\right) \tag{3.20}$$

where $$\eta(m_i, \upsilon) = \frac{|V_{GSb}| - |V_{Tb}|}{V_{DD}} f(m_i, \upsilon) \text{ and} \tag{3.21}$$

$$f(m_i, \upsilon) = \frac{m_i^2}{\sqrt{2\upsilon} + \upsilon\sqrt{1+m_i} + \upsilon\sqrt{1-m_i}}$$

The function $\eta(m_i,\upsilon)$ is referred to as a *structure function*. Note that different copiers have different structure functions. The structure functions are derived as follows.

Basic Current Copier

Consider the basic current copier in Figure 3.6, the bias transistor M_b works in saturation if V_{DD}-V_X > V_{DD}-V_b-|V_{Tb}|. To make both transistors M_1 and M_2 to operate in saturation, it requires

$$V_{Xmin} > V_{Xmax} - V_{T1}, \text{ and } V_{Xmin} > V_{Xmax} - V_{T1}$$

where V_{T1} is the threshold voltage of M_1, and the maximum and minimum values of V_X are

$$V_{Xmax} = \sqrt{\frac{1+m_i}{2\upsilon}}(|V_{GSb}| - |V_{Tb}|) + V_{T1} \tag{3.22}$$

and

$$V_{Xmin} = \sqrt{\frac{1-m_i}{2\upsilon}}(|V_{GSb}| - |V_{Tb}|) + V_{T1} \tag{3.23}$$

Note that V_{Xmax} and V_{Xmin} are the voltages when the calibrated storage transistor has the maximum and minimum drain currents, respectively. Since V_{DD}=V_b+|V_{GSb}|, we obtain

$$V_{GSb}|-|V_{Tb}| \le V_{DD} / f_B(m_i,\upsilon)$$

where

$$f_B(m_i,\upsilon) = 1 + 2\sqrt{(1+m_i)/2\upsilon} - \sqrt{(1-m_i)/2\upsilon} \qquad (3.24)$$

Thus, the structure function is expressed as

$$\eta_B(m_i,\upsilon) = f(m_i,\upsilon)/f_B(m_i,\upsilon). \qquad (3.25)$$

Figure 3.8(a) plots the structure function of the basic current copier in Figure 3.6, where the υ-value is varied from 0 to 4 for m_i=0.4, 0.6, and 0.8. Figure 3.8(b) shows the optimum device parameter values υ for maximum $\eta_B(m_i,\upsilon)$ with m_i ranged between 0.4 and 0.8.

Cascode Current Copier

Figure 3.9(a) shows the cascode copiers which are used for noise analysis. Similarly, both M11 and M21 are operated in saturation when

$$V_{b1} - V_{GS12max} > V_{Xmax} - V_{T11}$$

and the condition for both M12 and M22 operated in saturation is

$$V_{Xmin} - (V_{b1} - V_{GS12min}) > V_{GS12min} - V_{T12}$$

Similarly, the conditions for both bias transistor in saturation are

$$|V_{GS32}| + V_{b3} - V_{Xmax} > |V_{GS32}| - |V_{T32}|$$

$$V_{DD} - |V_{GS32}| - V_{b3} > |V_{GS31}| - |V_{T31}|$$

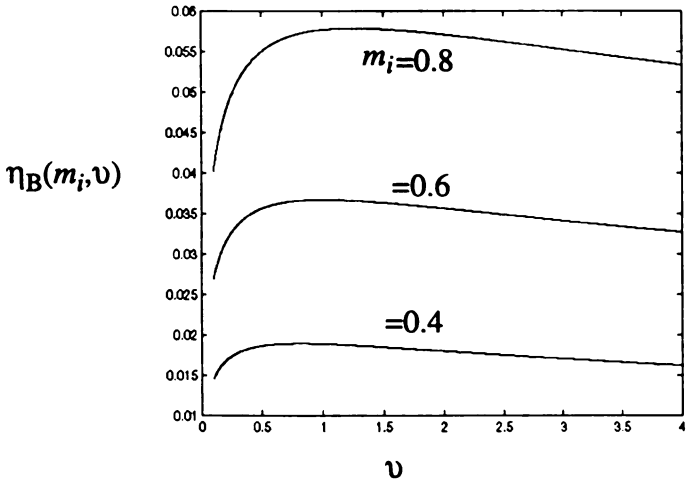
If we assume that both M_{11} nd M_{12} have the same size, then $V_{GS12max}=V_{GS11max}=V_{Xmax}$, and $V_{GS12min}=V_{GS11min}=V_{Xmin}$. Therefore, we obtain,

$$|V_{GSb}|-|V_{Tb}| = |V_{GS31}|-|V_{T31}| \le V_{DD} / f_C(m_i,\upsilon)$$

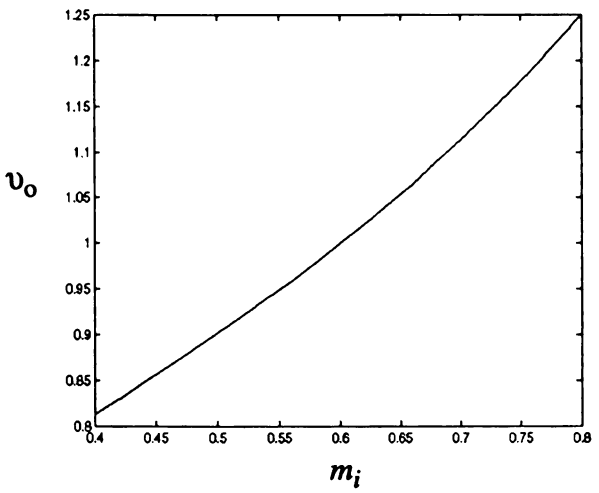
where

$$f_C(m_i,\upsilon) = 2 + 3\sqrt{(1+m_i)/2\upsilon} - \sqrt{(1-m_i)/2\upsilon} \qquad (3.26)$$

Thus, the structure function for the cascode current copier,



(a)



(b)

Figure 3.8: Structure Functions for Basic Copiers: (a) $\eta_B(m_i,\upsilon)$; and (b) Optimum Device Parameter Values υ_o.

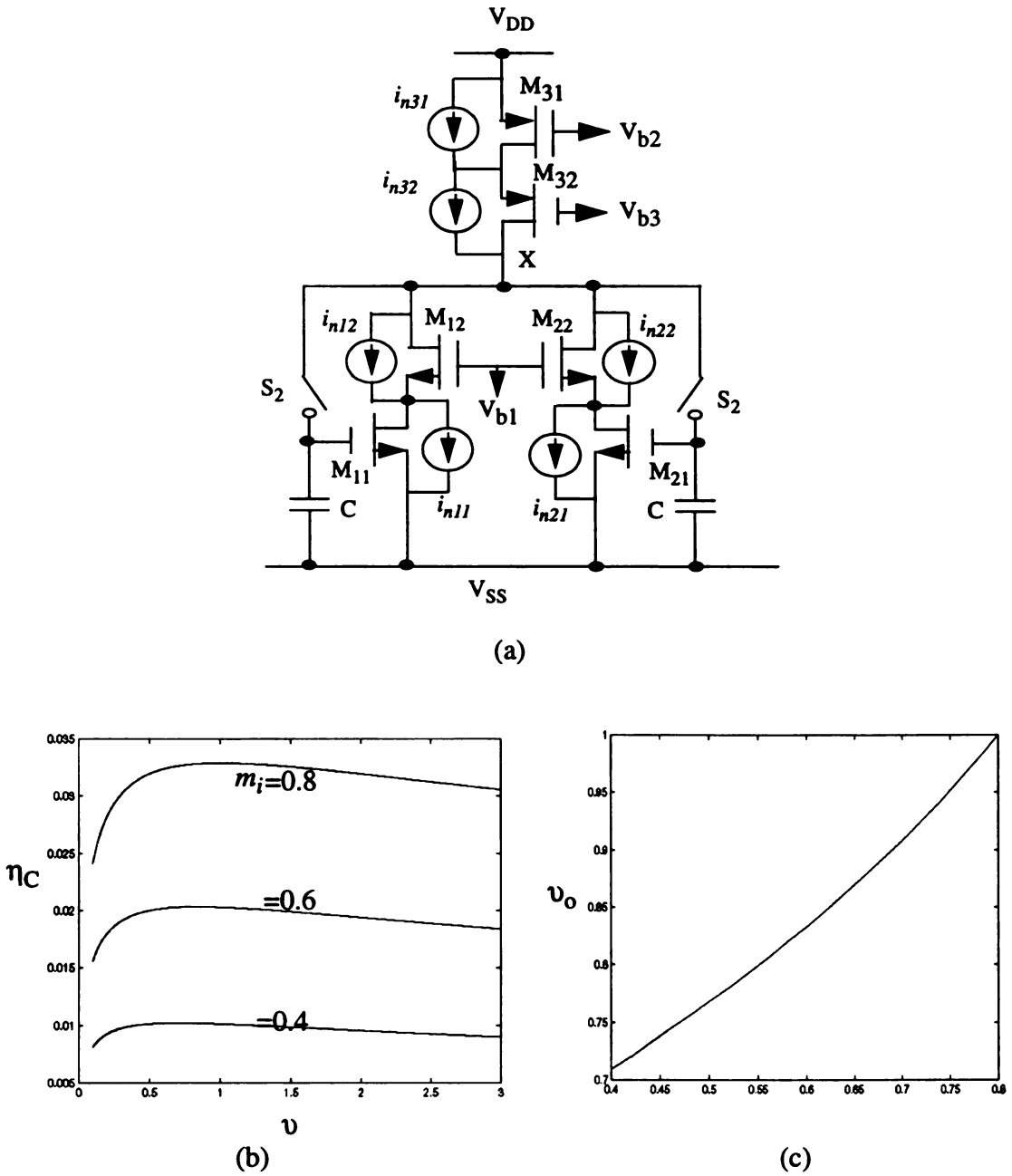


Figure 3.9: Cascode Copier: (a) Schematic; (b) $\eta_C(m_i,\upsilon)$; and (c) Optimum υ_o.

$$\eta_C(m_i,\upsilon) = f(m_i,\upsilon)/f_C(m_i,\upsilon). \quad (3.27)$$

Figure 3.9(b) plots the structure functions of the cascode copier, and Figure 3.9(c) shows the optimum device parameter values υ.

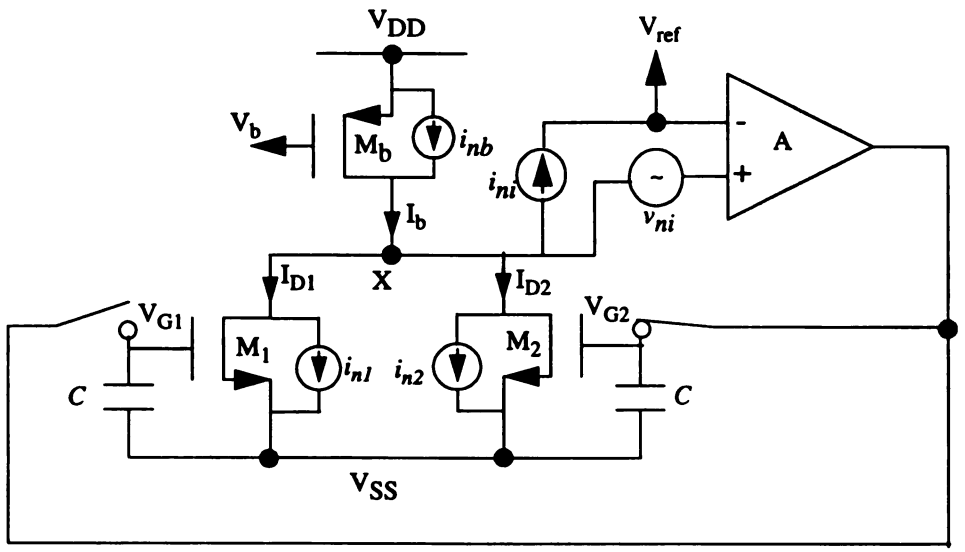
Note that, by (3.21), for a given design constraint on both speed and power, the current copier who has higher structure function value will achieves larger SNR. This implies that, for a given design constraint on both SNR and speed, the current copier which has the higher structure function value will require less power.

Negative Feedback Current Copiers

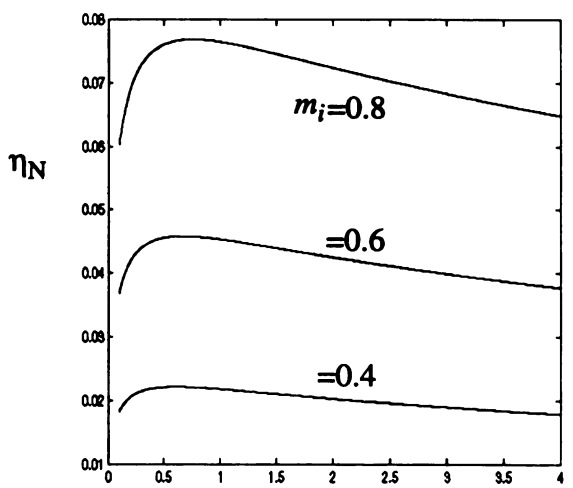
Figure 3.10(a) shows the copiers for noise analysis. In this structure, a new noise source is introduced by the additional feedback amplifier, where the noise source is modeled by adding an input current source i_{ni} and an input voltage source v_{ni}, as shown. However, the new noise source is not of significance to the total noise. More specifically, the noise voltage source causes the voltage on X to be deviated from the expected value V_{ref} by v_{ni}. Thus, the variance of the noise current caused by this voltage source is $g_o^2\overline{v_{ni}^2}$, where g_o is the equivalent conductance between X and ground. Since g_o is usually very small, the noise can then be ignored. On the other hand, it has been shown that the noise caused by the input noise current is also very small compared to the total noise [32]. Thus, the noise caused by the amplifier is ignored in this discussion. Similarly, the conditions for M_1, M_2, and M_b in saturation are

$$V_{G1max} - V_{T1} < V_X,\ V_{G2max} - V_{T1} < V_X, \text{ and } V_{DD}-V_X > V_{DD}-V_b-|V_{Tb}|$$

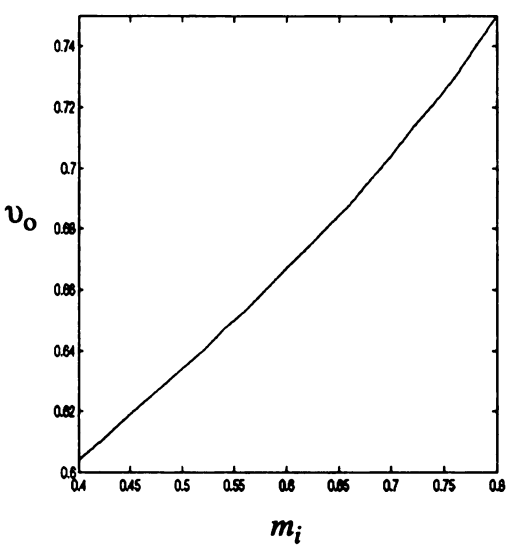
where V_{G1} and V_{G2} are the gate voltage of both M_1 and M_2, respectively. Therefore, we obtain,



(a)



(b)



(c)

Figure 3.10: Negative-Feedback Copier: (a) Schematic; (b) $\eta_N(m_i,\upsilon)$; and (c) Optimum υ_o.

$$|V_{GSb}|-|V_{Tb}| \leq V_{DD} / f_N(m_i,\upsilon)$$

where

$$f_N(m_i,\upsilon) = 1 + \sqrt{(1 + m_i)/2\upsilon} \qquad (3.28)$$

Thus, the structure function for the negative-feedback current copier,

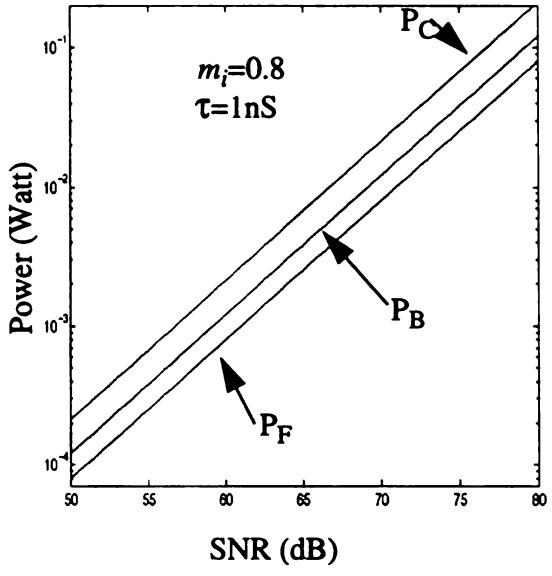
$$\eta_N(m_i,\upsilon = f(m_i,\upsilon)/f_N(m_i,\upsilon). \qquad (3.29)$$

Figure 3.10(b) plots the structure functions of INFCC, Figure 3.10(c) shows the optimum device parameter values υ.

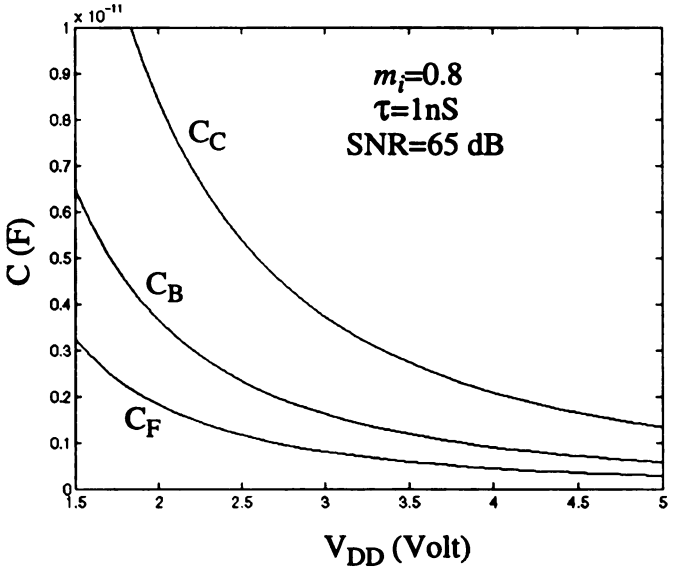
3.1.4. Discussion

According to the simulation results for the structure functions plotted in Figure 3.8(a), 3.9(b) and 3.10(a), we have $\eta_N(m_i,\upsilon) > \eta_B(m_i,\upsilon) > \eta_C(m_i,\upsilon)$, for the same m_i and υ. This implies that the negative-feedback current copier has the largest SNR. This also implies that, for a given design constraint on both SNR and speed, the current copier which has the higher structure function value will require less power. In other words, the negative-feedback current copier requires the least power to achieve the same SNR and speed comparing with the other two copiers.

Figure 3.11(a) plots the power consumptions for the three copiers, where τ=1ns m_i=0.8 were simulated, and P_b, P_c, and P_f denote the power of the basic, cascode, and the negative-feedback copiers, respectively. Since the cascode copier has the least structure function value, it requires the largest power. Figure 3.11(b) plots the capacitances required for the three copiers to achieve a SNR of 65dB, where τ=1ns m_i=0.8 were simulated, and C_b, C_c, and C_f denote the capacitance required for the basic, cascode, and the negative-feedback copiers, respectively. Results show that the negative-feedback copier requires the least



(a)



(b)

Figure 3.11: Performance Comparisons: (a) Power; and (b) Capacitance.

capacitance. For the same supply voltage, the capacitance required by the negative-feedback copier is nearly 5.6 times less than that by the cascode copier. The use of large capacitance also implies the need of more chip area. In other words, the negative-feedback copier takes much less chip area. In addition, designing sample switches to drive such large capacitance will be a problem. Thus, the use of small capacitance in the negative-feedback copier reveals the best candidate for low-voltage/high-performance operation.

3.2 Alternative Negative Feedback Current Copiers

As discussed in Section 2.2.2, in an INFCC, Inverter Negative Feedback Current Copier, the current-storage transistor, together with the input current source, constitutes an inverter, the copier takes a positive-gain amplifier to form a negative feedback loop. To further simplify the structure while improving speed performance, this section presents an alternative negative feedback structure which is comprised of a source follower and a simple negative-gain amplifier [24]. Such current copiers are referred to as *Follower Negative Feedback Current Copiers*, or FNFCCs.

3.2.1 Structure and Operation

Figure 3.12(a) shows the schematic circuit diagram of the FNFCC. The current-storage transistor M_1 works as a source follower and its source node connected to the I/O node X. Note that node X has a low impedance, during calibration, even if an amplifier with a high input impedance is used. Thus, high speed and high accuracy can be obtained simultaneously. Since the body effect of M_1 may increase the transconductance g_{o1}, the body of M_1 is connected to its source. Two negative-gain amplifiers, as shown in Figure 3.12(b) and

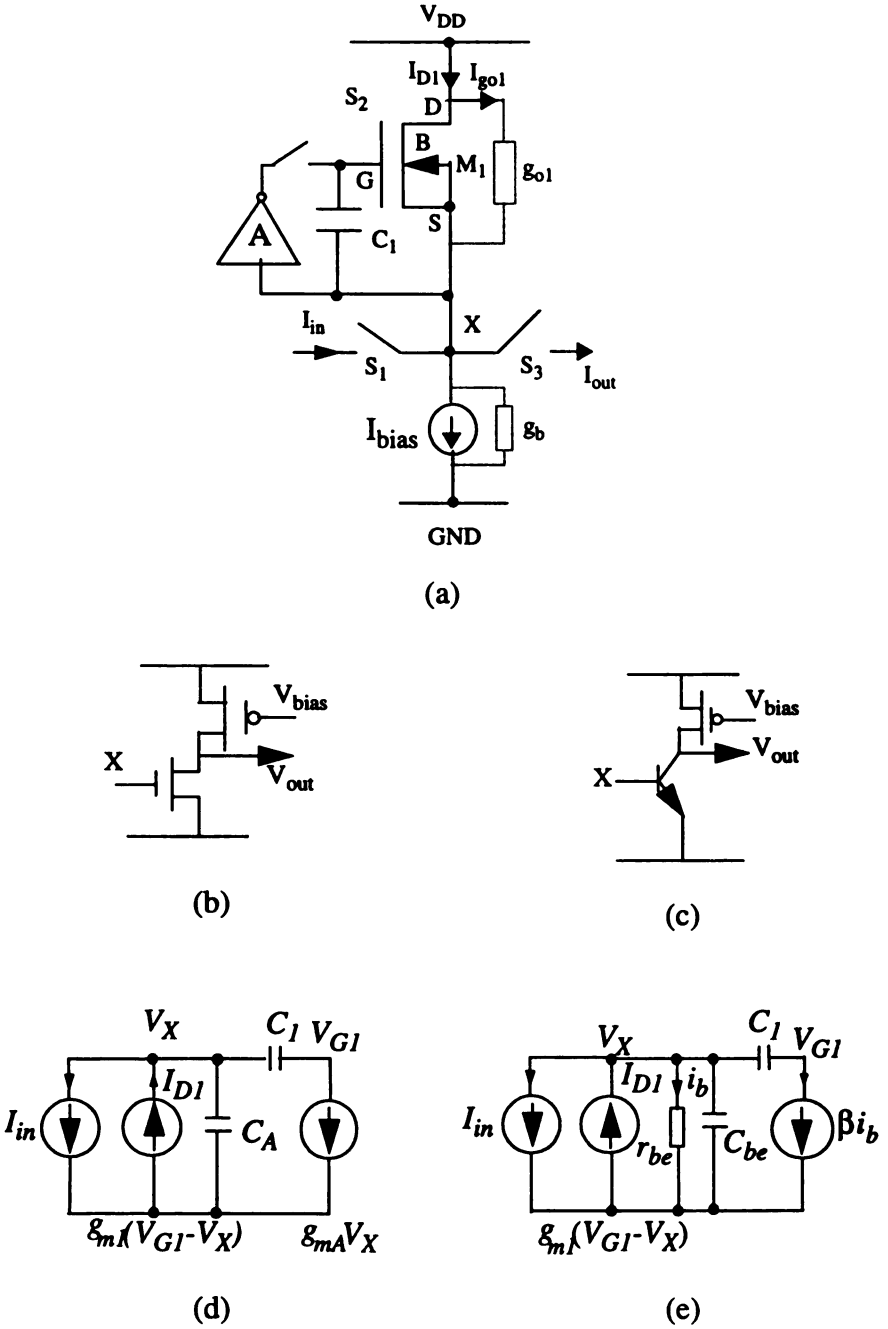


Figure 3.12: FNFCCs: (a) Schematic; (b) CMOS Amplifier; (c) BiCMOS Amplifier; (d) Equivalent Circuit for FNFCCI; and (e) for FNCCII.

Figure 3.12(c), are employed in this implementation. The BiCMOS amplifier is attractive for its large bandwidth and high voltage-gain. For simplicity of this discussion, the FNFCC using the CMOS amplifier is referred to as FNFCCI, while the one with BiCMOS amplifier as FNFCCII.

Similar to (2.2), the variation of the error current ΔI_{go} can be expressed as

$$\Delta I_{go} \approx -\begin{bmatrix} \dfrac{g_{o1}+g_b}{g_{m1}(A+1)} \\ \dfrac{g_{o1}+g_b}{g_{m1}(A+1)}+\dfrac{g_{oA}}{\beta_B g_{m1}} \end{bmatrix} \Delta I_{in} \qquad \begin{matrix} (3.30\text{I}) \\ (3.30\text{II}) \end{matrix}$$

where β_B is the current gain of the bipolar transistor in Figure 3.12(c). From (2.4I) and (3.30I), both FNFCCI and INFCCI have the same accuracy. In (3.30II) for the NFCCII, the first term can be ignored due to the large voltage amplification of a bipolar inverter. The second term reflects the fact that the base current of the bipolar transistor in Figure 3.12(c) depends on the input current. Typically, we have g_{m1}/g_{oA}=50 and β_B=100. Thus, as in (3.30II), the accuracy can be 1/5000, i.e. $2\text{x}10^{-4}$, which is nearly a 12-bit accuracy if the copier is used to design an ADC.

The characteristic equations, without considering the stray effects of the switches for both FNFCCI and FNFCCII, are derived as follows, where the small-signal equivalent circuits shown in Figures 3.12(d) and 3.12(e) are employed

$$\begin{bmatrix} s^2+\tau_A^{-1}s+(\tau_1\tau_A)^{-1} \\ s^2+(1+\beta_B^{-1})\tau_B^{-1}s+(\tau_1\tau_B)^{-1} \end{bmatrix} = 0 \qquad \begin{matrix} (3.31\text{I}) \\ (3.31\text{II}) \end{matrix}$$

where $\tau_B=(r_{be}/C_{be})/\beta_B$ is the time constant of the bipolar amplifier. (3.31) shows that both

FNFCCI and FNFCCII have short settling time.

As the speed predicted by (3.31) is quite high, the limitations determined by the stray effects of the switches may be approached. Thus, it is necessary to include the effects of the switches. To obtain a model which is simple, can accurately predict the settling behavior and give guidance on the choices of the parameters for the amplifier, the storage-transistor and the switches, we need to select appropriate time constants.

3.2.2 Stray Effects

For the FNFCC, the effect of the stray capacitance c_s is alleviated due to the fact that they are in parallel with the input capacitance of the feedback amplifier. The time constant associated with the input capacitance can be written as

$$\tau_A'' = \begin{bmatrix} (C_A + c_S)g_{mA}^{-1} & \text{(3.32I)} \\ (C_{be} + c_s)(r_{be}/\beta_B) & \text{(3.32II)} \end{bmatrix}$$

This express shows that the increase of τ_A' due to c_s can be alleviated by an increase of the transconductance g_{mA}. The stray resistance r_{S2} of the switch S_2 effects the settling time through the time constant

$$\tau_S' = r_{S2}C_o \qquad (3.33)$$

where C_o is the stray capacitance at the output of the amplifier. For the CMOS amplifier, this capacitance includes the drain-to-gate, and drain-to body capacitances of the transistors at the output of the amplifier. The gate capacitance of the switch S_2 makes also a contribution to the capacitance. For the BiCMOS amplifier, the capacitance will be mainly determined by the collector-base and collector-body capacitances of the bipolar transistor.

Taking the time constant of the current-storage transistor τ into consideration, the small-signal linearized equivalent circuit for both FNFCCI and FNFCCII are illustrated in Figure 3.13. From the equivalent circuits, both have the same characteristics equation as given in (3.10), but the coefficients for the FNFCCI are expressed as

$$\begin{aligned} a&=[1+c_o/C+c_o/(C_A+C_s)]^{-1}\tau_s' \\ b&=[1+c_o/C+c_o/(C_A+C_s)][1+g_{m1}c_o/(g_{mA}C)]^{-1}\tau_A'' \\ c&=[1+g_{m1}c_o/(g_{mA}C)]\tau \end{aligned} \qquad (3.34I)$$

and for the FNFCCII

$$\begin{aligned} a&=[1+c_o/C+c_o/(C_{be}+C_s)]^{-1}\tau_s' \\ b&=[1+c_o/C+c_o/(C_{be}+C_s)][1+c_o/C+r_{be}g_{m1}c_o/C]^{-1}\tau_A'' \\ c&=[1+c_o/C+r_{be}g_{m1}c_o/C]\tau \end{aligned} \qquad (3.34II)$$

Due to the stray effects of the current-steering switches, the stray capacitance at the input of the feedback amplifier is increased, from C_A to C_A+c_s for the FNFCCI and from C_{be} to $C_{be}+c_s$ for the FNFCCII. To keep the time constant τ_A'' unchanged, the transconductance g_{m1} or r_{be}^{-1} has to be increased accordingly. This asks for an increase of the device current. The increase of the device current will be accompanied by a number of side effects, including higher power consumption, larger noise and lower amplification of the amplifier. Thus, some other possibility to reduce the stray effects will be desired.

One way to achieve this is to move the switch from node X to the drain side of the current-storage transistors, as shown in Figure 3.14, where switches S_{i1}, with $1 \leq i \leq N$, control the current. This method can be useful when a number of current-storage transistors share the same feedback amplifier, as it is often the case for a switched current integrator and residue amplifier. The current can be transferred from one transistor to the others by

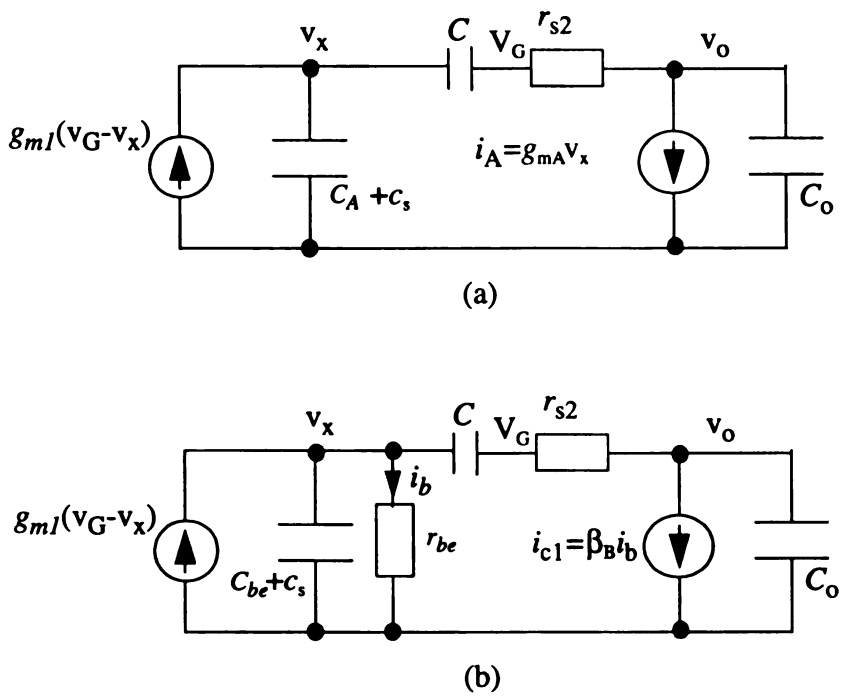


Figure 3.13: Equivalent Circuits: (a) FNFCCI; and (b) FMFCCII.

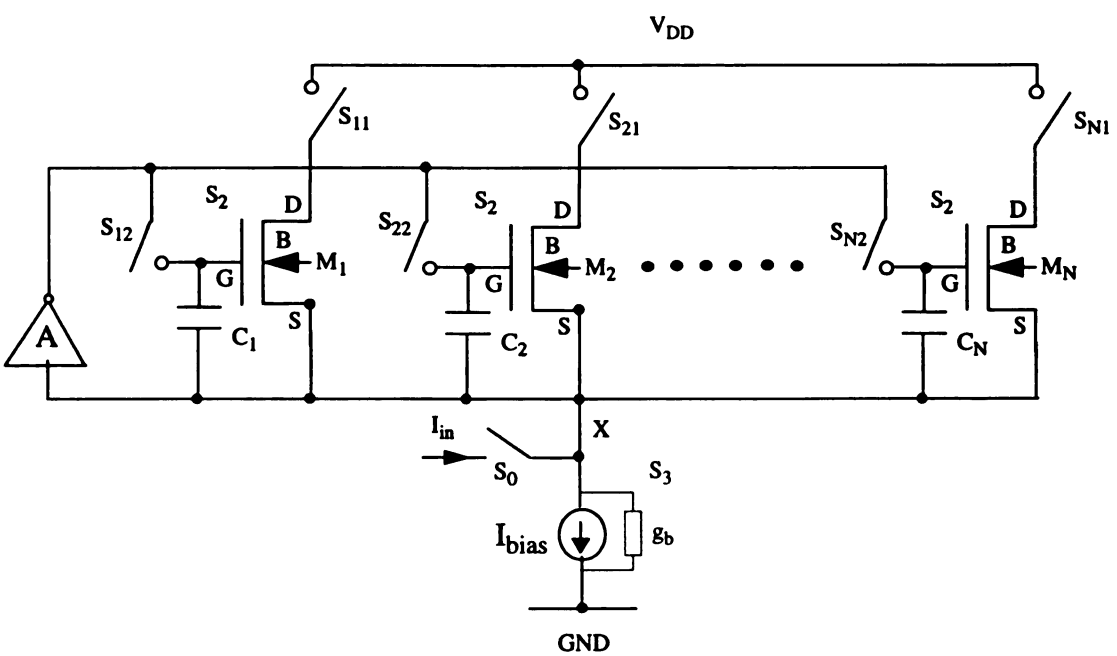


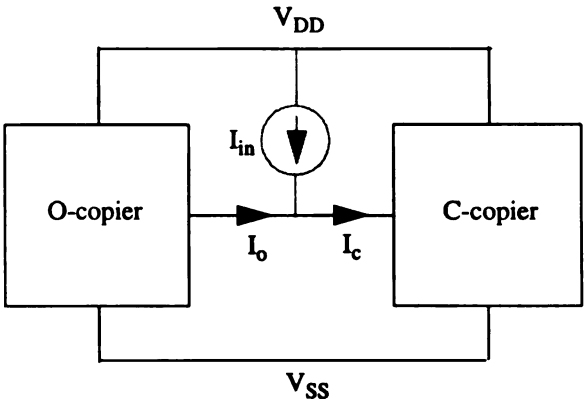
Figure 3.14: Stray Effect Reduction.

control the state S_{i1} and S_{i2}, to implement different functions. As the switches S_{i1} is separated from node x by the current storage transistors, their stray capacitance will have no effect on the stability of the feedback loop. The settling behavior can be analyzed using model (3.34) with c_s set to zero. An input switch S_0 is needed to control the input current I_{in}. The design of the switch and the way how to output current from the current-storage transistors will be discussed in Chapter 4.

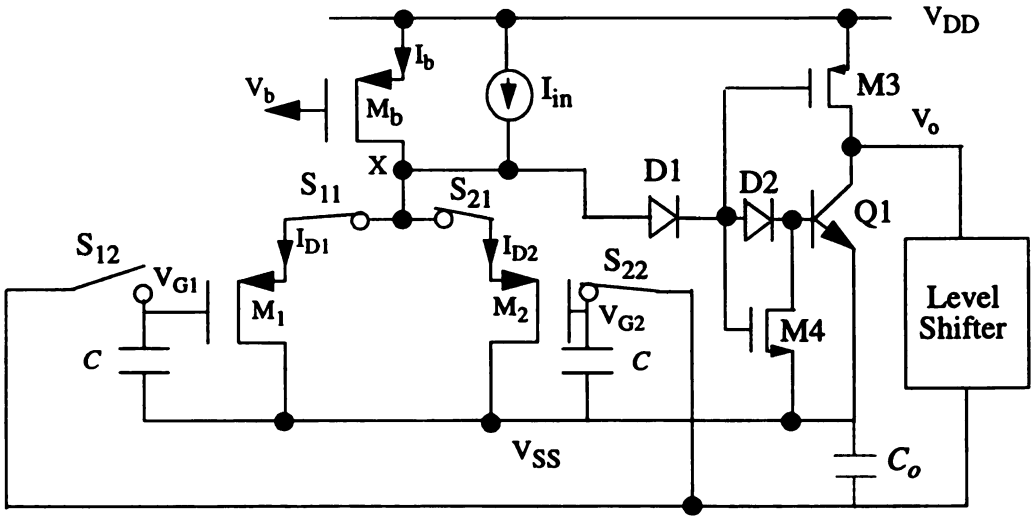
3.3 Simulation Results

The accuracy and settling performance of a FNFCCII and the effects of the current-sample and current-steering switches on the settling behavior are studied by simulations. The simulations verify the high accuracy and high speed of a FNFCCII. They show also large effects of the switches on the settling time and amplifier design.

The simulation is conducted using two identical copiers, as shown in Figure 3.15(a), where one is used as the operational copier (o-copier), and the other as the calibration copier (c-copier). The I_o and I_c are the output currents of the o-copier and the input current of the c-copier, respectively. This configuration implies that the current held in one copier is transferred to the other one. Therefore, the impact of the stray effects of both, the c-copier and the o-copier, are included in the simulation. The input current I_{in} is introduced to generate a pulse current for settling time simulation. The circuit of Figure 3.15(b) is used to implement the configuration of Figure 3.15(a). It contains two current-storage transistors M_1 and M_2, a feedback amplifier with transistors Q_1 and M_3 and some level shifters. Diodes D_1 and D_2 consists of a level shifter. It generates a proper potential for the node x. The level shifter at the output of the amplifier ensures that the output voltage of the ampli-



(a)



(b)

Figure 3.15: Simulated Circuits: (a) Block Diagram; and (b) Schematic.

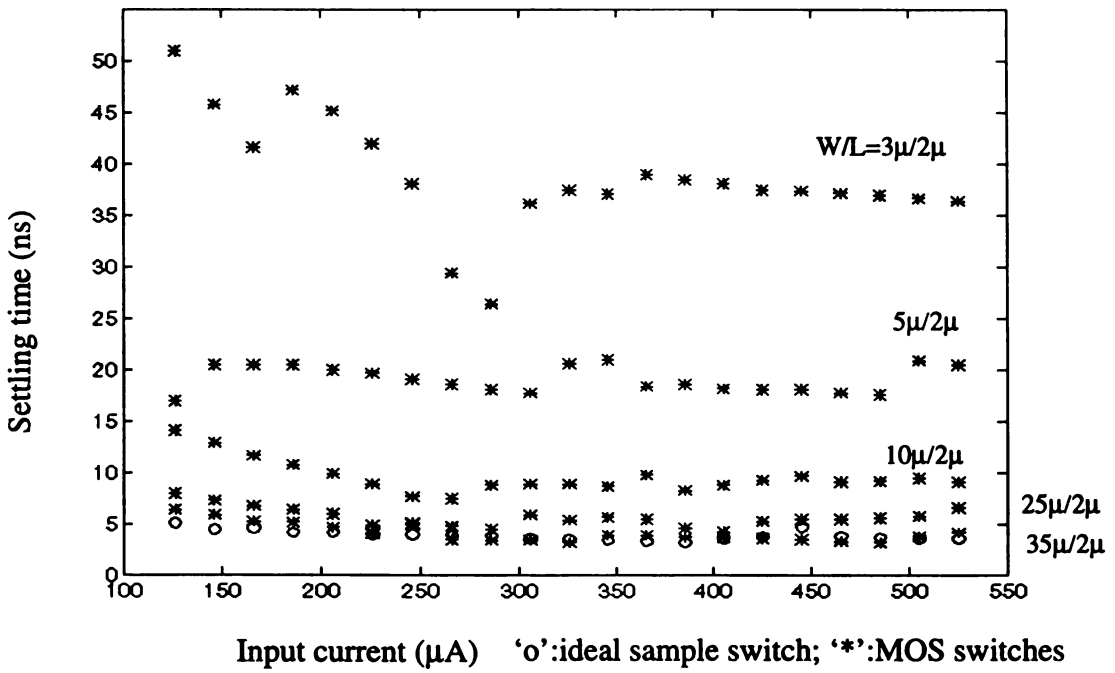
fier be in the range, such that the amplifier works properly. This shifter can be implemented using MOS capacitors and switches [34], where the detailed implementation will be described in Chapter 5. The supply voltage is chosen as 3.3V due to the high threshold voltages, about 0.8673V for NMOS and -0.9506V for PMOS. In the simulations, transistor M_2 is assumed to be the operation, while M_1 the calibration transistor.

3.3.1 Speed Limitation

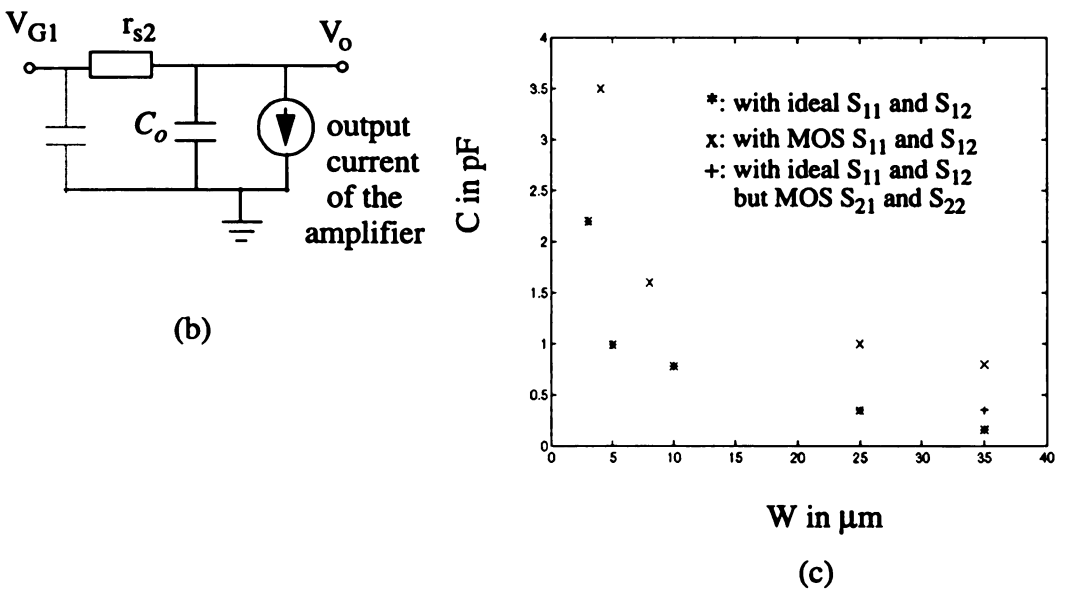
In order to study the speed limitation, the setup is simulated by assuming all with ideal switches. The closed switches, including S_{11}, S_{12} and S_{21}, are replaced by a wire and the opened switches S_{22} are simply removed. The impulse amplitude of the input current source I_{in} is set to 10μA. The capacitance *C* and the bias current of the transistor Q_1 are chosen so that the best speed can be reached. The simulated results is represented by the 'o'-cover shown in Figure 3.16(a). The settling time is defined as the time space from the onset of the impulse input current to the time for the drain current of the calibration transistor M_1 to settle within 0.1% of the impulse amplitude. As discussed in Section 2.2.2, the speed will be limited by the feedback amplifier. The settling time is expressed as a function of the current in the calibration transistor M_1, because the current affects the transconductance.

The settling time of a current copier may be affected by the sample switch, current-steering switches, and power supply voltage employed by the copier. The following discussion describes their effects on the settling behavior.

Sampling Switches To evaluate the effect of the sample switch, the switches S_{12} and S_{22} are replaced by MOS transistors in this simulation, where the channel length of the



(a)



(b)

(c)

Figure 3.16: Effects of Sample Switch: (a) Settling Time; (b) Equivalent Circuit; and (c) Optimal Capacitance.

switch transistor is chosen as 2μm, i.e., the minimum length allowed by the technology, and various channel widths are chosen. The gate capacitances are varied to reach the best speed for a given switch width. The results for the settling times are represented by the '*'-curves in Figure 3.16(a). Two changes of the settling behavior can be seen: a rapid increase of the settling time and an increase of the dependence of the settling time on the transistor current as the switch size goes down.

Recall that a large switch has a large gate capacitance and a small on resistance, and a small switch has a small gate capacitance and a large on-state resistance. The settling time becomes worse for a small switch reveals simply that the stray resistance has a severer impact than the stray capacitance. As shown in Figure 3.16(b), the stray resistance r_{s2} and the stray output capacitance C_o of the amplifier generates a R-C link between the output node V_o of the amplifier and the gate node V_{G1} of the calibrating current-storage transistor. The time constant $r_{s2}C_o$ becomes large as the switch size goes down, leading to a large delay through the link. The settling time increases.

For the circuit of Figure 3.15, the stray capacitance C_o is mainly the collector-to-substrate and the collector-to-base capacitances of the bipolar transistor Q_1. A small transistor should be used to keep these capacitances small. On the other hand, NMOS transistor should be chosen for the switch to reduce the stray resistance r_{s2}. This is the reason for choosing PMOS current-storage transistors in Figure 3.15. It allows low operating gate potentials V_{G1} and V_{G2}, so that the stray-resistance of the NMOS switches S_{21} and S_{22} can be reduced as much as possible.

The optimal gate capacitance for the best speed under a given switch width is shown in Figure 3.16(c). From the illustration, the capacitance decreases with the increase of the

switch width. Since a large gate capacitance and a small switch stands for a small charge-injection error, with the decrease of the switch width, the accuracy of the copiers will increase. On the other side, the speed of the copier decreases. Therefore, there is a trade-off between speed and accuracy. However, for the circuit of Figure 3.15, the switch should not go down below 5μ, to avoid strong dependence of the settling time on the transistor current.

Current-Steering Switches To control the current of the storage-transistors, switches S_{11} and S_{21} have to be used. Their introduction will cause another degradation of the settling time due to their stray resistances r_{s11} and r_{s12}, and stray capacitances C_{s11} and C_{s12}. Since they have to carry a current equal to that of the current-storage transistor, their size cannot be small. As shown in Figure 3.17(a), a R-C link, consisting of r_{s11} and $(C_{s11}+C_{s12})/2$ between node S_1 and x is introduced. The effect of the stray capacitance $(C_{s11}+C_{s12})/2$ can be reduced by increasing the bias current of the bipolar transistor, which increases the equivalent capacitance C_{be} and reduces the equivalent resistance r_{be}. However, the effect cannot be removed completely because of the stray base resistance r_b of the transistor Q_1, the stray resistance r_d of the level-shifting diodes and the stray resistance r_{s11} of the switch itself. Therefore, there is still some degradation of the settling time even if the transistor current is increased. The simulated settling times, with switches S_{11} and S_{22} also replaced by NMOS transistors and the bias current for Q_1 increased to 1.4mA, are shown in Figure 3.17(b). The optimal capacitance for the best speed is represented by the 'x'-curve in Figure 3.16(c). Compared with the results of Figure 3.16(a), where the bias current for Q_1 is only 350μA, some degradation can still be seen.

The increase of the bias current of Q_1 will introduce side effects, including increase of the power consumption, reduction of the amplification and enhancement of the noise of

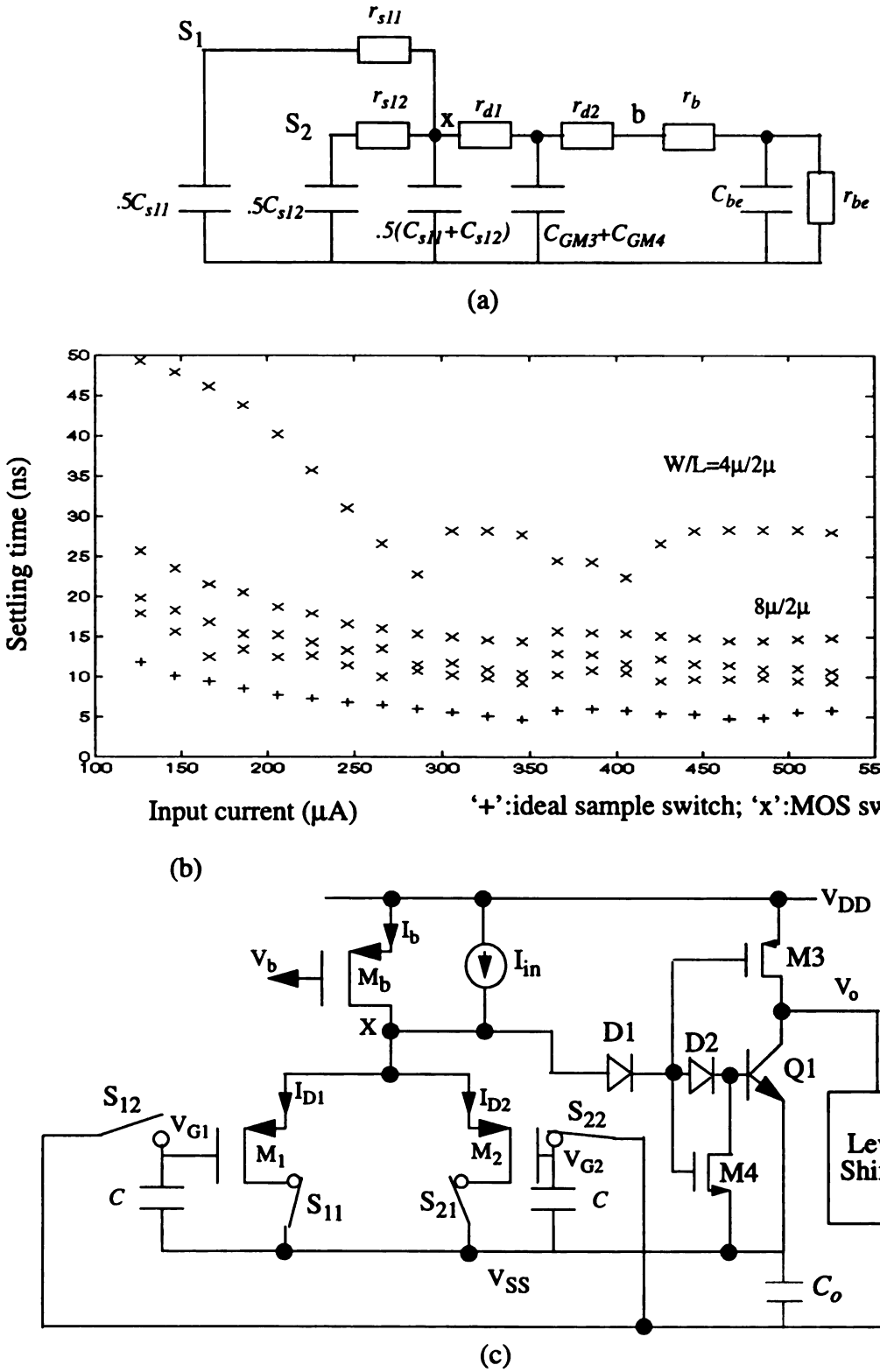


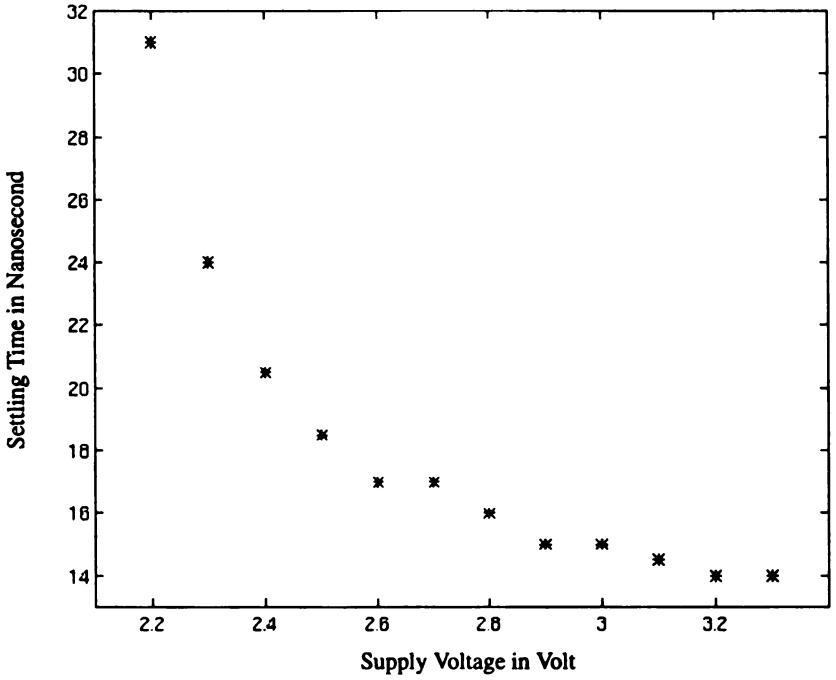
Figure 3.17: Current-Storage Switch Effects: (a) Equivalent Circuit; (b) Settling time; and (c) Current Cell Pair.

the amplifier. Thus, the bias current should be kept as small as possible. This forces us to look for other approaches for implementing the switches S_{11} and S_{12}, or to find other ways to switch the current in the storage transistors. A very effective method to achieve this is to move the switches S_{11} and S_{21} from the source side to the drain side of the current-storage transistors, as shown in Figure 3.17(c). This replacement can completely remove the effect of the switch. Simulation results, with all the switches implemented using MOS transistors and a bias current of 350μA for Q_1, show no noticeable deviation of the settling time from the one given in Figure 3.16(a). A MOS switch working in the saturation region can be used to supply the input and take the output current.

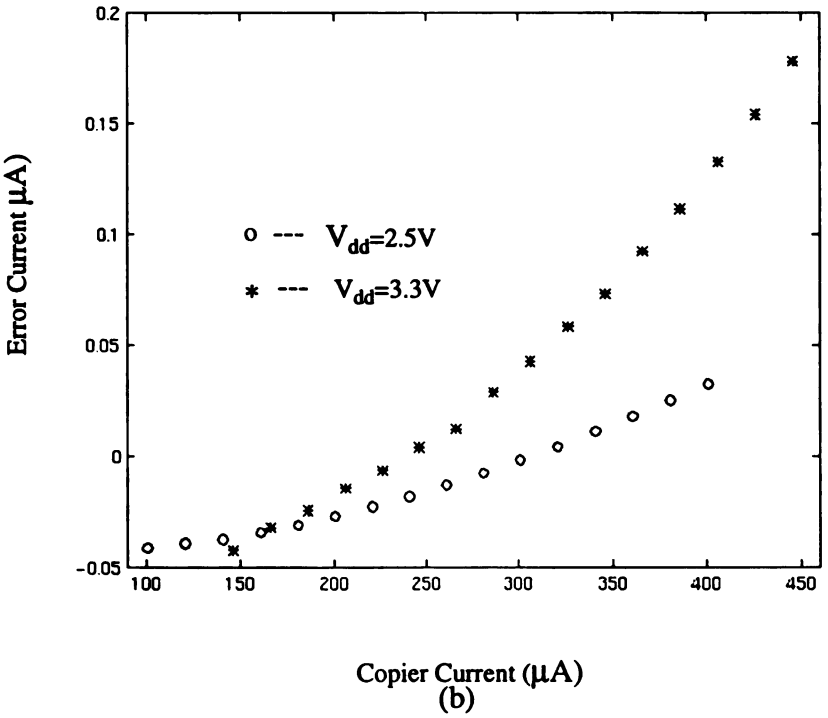
Power Supply Voltage Figure 3.18(a) shows the Pspice simulation results of the settling time of the circuit of Figure 3.17(c) for various supply voltages. The width of the sample switch is 6μm. The simulation result shows that the settling time increases significantly as the supply voltage goes down. This is due the increase of r_{s2}, which causes τ_{s2} becoming large.

3.3.2 Error Currents

Figure 3.18(b) illustrates the accuracy of the copier. The accuracy is calculated with the following process: (1) set the input current I_{in} to zero, (2) simulate the copier in the figuration of Figure 3.17(c) with one copier in operation and the other in saturation; and (3) exchange the copier states. The difference of the currents obtained in the steady-state at Steps (2) and (3) is defined as the error current. The error current exists because of the effects due to charge-feedthrough and non-zero output conductance. The copier current is varied by changing the initial on the gate capacitance of the operation copier in the step (2).



(a)



(b)

Figure 3.18: (a) Settling Time; and (b) Error Currents.

The copier has a smaller error current for V_{dd}=2.5V because the charge injection error is reduced.

3.4. Discussion

Based on the analysis of the charge-injection error, this chapter outlines the design trade-offs among accuracy, speed performance, and power consumption and addresses the stray effect of the switches which may degrade the speed performance of the copiers. It has been shown that the stray effects can be alleviated by reducing the stray capacitance of the current-steering switches, or by separating the large current-steering switches from the small current-sample switches, for the copier to achieve high speed operation.

The proposed FNFCC structure enhances the speed performance of INFCCI and resolves the accuracy problem in INFCCII. The proposed FNFCC can achieve a very high accuracy and speed by using BiCMOS technology. The simulation results have verified the operation of the proposed copiers and demonstrated that a very high accuracy and speed of FNFCCII can be attained even with a low supply voltage. Since the supply voltage is mainly determined by the switch performance to keep a short setting time, the supply voltage in the proposed copier can be reduced to 1.5V without affecting its speed performance if the threshold voltage is reduced to nearly 0.5V.

The results of this study have demonstrated that, with the proposed high-performance current copiers, the switched-current circuit techniques become promising. The development of the next-generation data acquisition and conversion circuits using these copiers will be discussed in Chapters 4 and 5.

Chapter 4

Sample and Hold (S/H) Circuits

This chapter presents the design of a simple high-performance SI V-I converter with the sample/hold (S/H) function [35,36] and an oversampled high-linear SI sample and hold (S/H) circuit using current copiers [37-39]. A V-I converter is often needed at the "front end" of some current-mode circuits to provide interface with a voltage-mode system. The proposed V-I converter combines both V-I conversion and S/H function to simplify the circuit. Concerns are paid to high-speed operation and to reducing distortion due to nonlinear properties of MOS devices.

The oversampled S/H circuit achieves a very high linearity. Using a digital technology, where no linear capacitor is available, the linearity of a S/H circuit will be degraded since a nonlinear capacitance has to be used for signal storage. This is true for both the traditional voltage-mode and the current-mode S/H circuits. Using the SI technique, integrators having a simple structure can be designed, which helps to reduce the overall complexity of an oversampled S/H circuit. This study adopts a feed-forward approach to further simplify the operation to reduce the order of integrations needed to meet a linearity specification.

4.1. A V-I Converter with S/H Function

A number of transconductor designs have been proposed and implemented [40]. However, a simple high-linear V-I converter can be realized using a resistor and a current copier, as shown in Figure 4.1, where the circuit has the advantage that it incorporates the S/H function. The circuit is operated in two modes: *sampling/conversion mode* and *holding mode*. During the sampling period, S_1 is closed and S_5 is opened, the copier is in its calibration state. Note that if the copier has a very small input impedance during calibration, its input/output node "G", serving as a virtual ground, has a potential that is virtually not affected by the input current I_i. Therefore, the relationship between the variations of I_i and V_i will be solely determined by the resistor R and thus the circuit achieves high-linear conversion. On the other hand, during the holding period, switches S_5 and S_1 are respectively turned on and off to deliver the held current to the load. The choice of the current copier is important for high-performance V-I converter.

Numerous current copiers have been presented and discussed in Chapters 2 and 3. However, in addition to simple structure and high-speed operation, the current copiers must have a very low input impedance during calibration and can be operated under low power supply. Therefore, this section presents an alternative copier, *differential current-storage unit*, using negative feedback to boost its transconductance. To demonstrate the high-speed operation, the settling behavior of the V-I converter is analyzed, where the non-ideality of the switches are taken into consideration and the switches are modeled by the small-signal linearized circuit model [21]. The analysis provides a guideline for selecting appropriate device parameters.

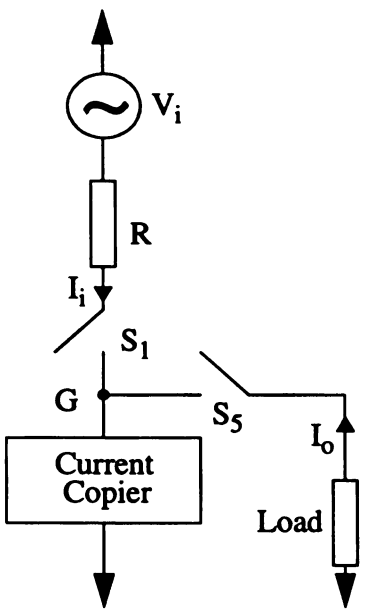


Figure 4.1: Proposed Current-Copier-Based V-I Converter with S/H Function.

4.1.1 Structure and Operation

Figure 4.2 illustrates the proposed current-copier-based V-I converter. The current copier is comprised of a *differential current-storage unit* and a *feedback amplifier*. PMOS transistors M_1, M_2, and M_5 constitute the differential current-storage unit, where the capacitance C memorizes the voltage needed by M_2 to support the input current flowing through M_1. The capacitor C is connected between the gate and source nodes of M_2, while the drain node of M_2 is grounded. The circuit is operated as follows. When switches S_1, S_2, and S_3 are closed, and S_4 and S_5 are opened, referred to as the *sampling period*, the output tracks the input. When S_1, S_2, and S_3 are opened, referred to as the *holding period*, the converted current is sampled and held by the current copier. During the holding period, the sampled current is read by turning on switch S_5. The amplifier is used to accurately transfer the sampled current to a current copier load by turning on switch S_4.

During the sampling period, the input node, X, serves as a *virtual ground*. The input current variation ΔI_i can be expressed in term of the input voltage variation ΔV_i as

$$\Delta I_i = \frac{\Delta V_i}{R + r} \tag{4.1}$$

where the small signal input impedance, r, of the copier is

$$r = \frac{1}{A g_{M1} g_{M2} / (g_{M1} + g_{M2})} \tag{4.2}$$

g_{M1} (g_{M2}) is the transconductance of M_1 (M_2), and A is the voltage gain of the feedback amplifier. Since the sum of both drain currents, I_{D1} and I_{D2}, of the transistors M_1 and M_2, is constant, increasing I_{D1}, equivalent to the input current, results in decreasing I_{D2}. Thus, by (4.1) and (4.2), the first-order dependence of the transconductance on the input current can be cancelled off. Equation (4.1) also implies that the linearity of the V-I conversion is

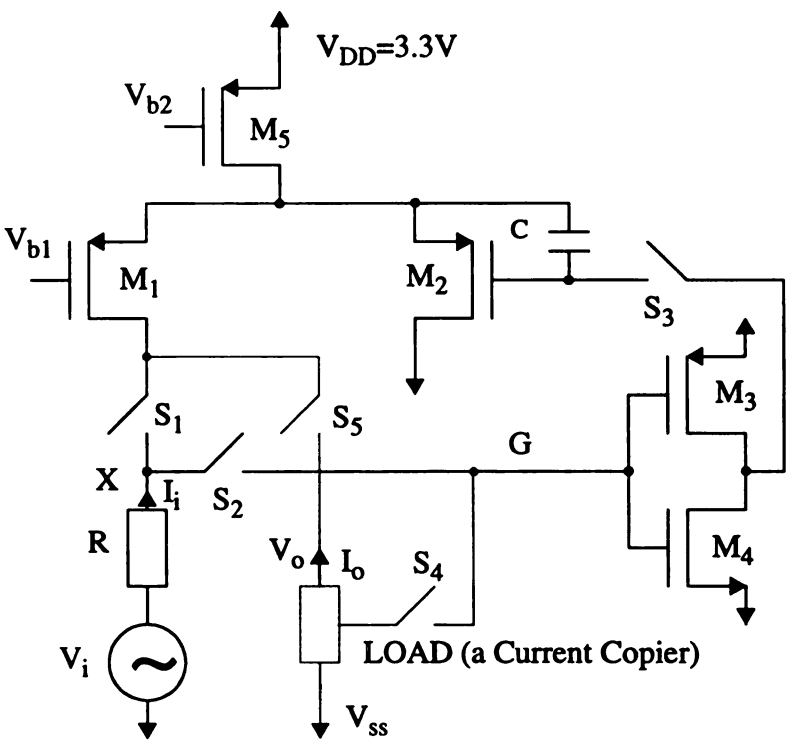


Figure 4.2: Schematic Circuit Diagram of the Propose V-I Converter.

increased with a larger resistance. In practice however, a larger resistance causes an increase of the feedback loop gain and the time constant associated with node X which decrease the loop stability and result in a longer settling time. A larger resistance also needs a larger input voltage swing to achieve the same range of dynamic output currents. This leads to a significant design trade-off among linearity, dynamic range, and conversion speed.

For high-frequency applications, large distortion may occur due to the modulation of the sample time through the input signal. To keep the distortion small it is essential that the potential at both ends of the sampling switch S_2 be only little effected by the input. Note that the potential of S_2 is determined by the gate voltage of M_2 and the variation ΔV_{g2} can be expressed as a function of the input voltage variation ΔV_i:

$$\Delta V_{g2} = \frac{\Delta V_i}{R g_{M1} g_{M2} / (g_{M1} + g_{M2})} \tag{4.3}$$

Apparently, choosing large transconductances, g_{M1} and g_{M2}, can reduce the variation ΔV_{g2}. Since the variation, $\Delta V_i/R$, is determined by the dynamic range given in a design specification, sufficiently large transconductances are then selected for both M_1 and M_2 to reduce the variation ΔV_{g2}. Note that the use of large transconductance g_{M2} does not imply the increase in the charge injection error, due to S_2, because the error depends on the time constant $g_{M2}^{-1}C$ [21], not on g_{M2} only. Thus, the charge injection error can still be kept reasonably small even though large g_{M2} is chosen.

4.1.2 Speed Limitations

For high-speed applications, fast settling time of the converter is needed. Settling time depends on the bandwidth of the CMOS inverter and the time constant $g_{M2}^{-1}C$, and it may also be affected by the use of practical switches which have non-zero on-resistances and gate capacitances. The following subsection discusses the settling behavior of the proposed V-I converter and describes the design principles of choosing the device parameters for achieving fast settling time.

To study the settling behavior of the proposed converter, the non-ideal switches are modeled by the small-signal linearized equivalent circuit, as shown in Figure 4.3(a) [21], where r_{sk} and C_{sk} are respectively the on-resistance and the half of the on-gate-capacitance of the switch S_k. Based on the switch model, Figure 4.3(b) illustrates the equivalent circuit of the proposed V-I converter during the sampling period. Based on the node-voltage equations of the equivalent circuit, we obtain a second order open-loop transfer function that can be used to estimate the main poles of the V-I converter,

$$H(S) = \frac{I_i(S)}{I_f(S)} = -\frac{(1+\tau_{M2,g2}S)(1-\tau_{M34,gd34}S)}{\alpha_0 S(1+\alpha_1 S)} \qquad (4.4)$$

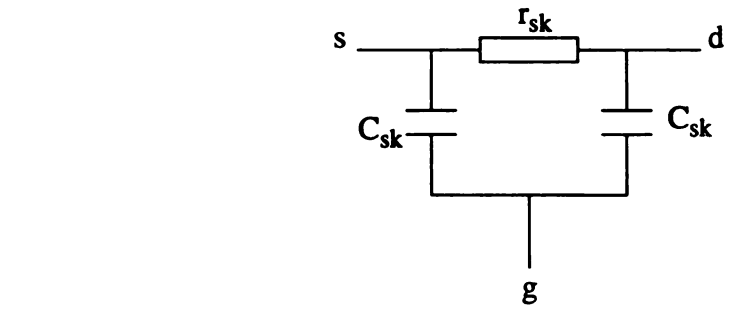
where $\tau_{a,b}$ denotes the time constant generated by r_a (or g_a) and C_b; $g_{M34}=g_{M3}+g_{M4}$ and $C_{gd34}=C_{gd3}+C_{gd4}$. If we assume that

$$\tau_{s3,g2} >> \tau_{x,y}, \quad \text{for all } x \neq s_3 \text{ and } y \neq g_2. \qquad (4.5)$$

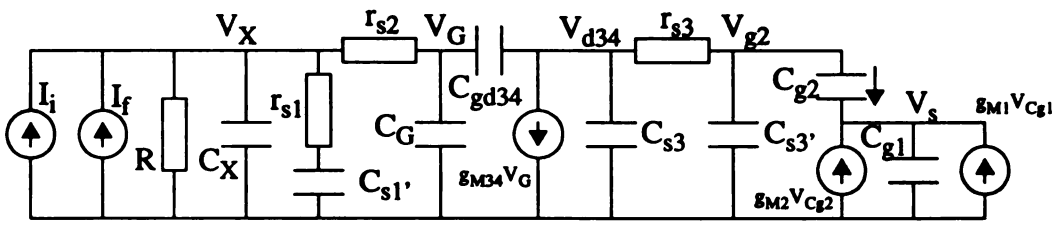
then both α_0 and α_1 can be approximated as

$$\alpha_0=\tau_{M2,g2}/Rg_{M34} \text{ and } \alpha_1 = \tau_{R,X_{tot}} + \tau_{s1,s1'} + \tau_{s2,G} + \tau_{s3,s3'} + \tau_{M1,g1} \qquad (4.6)$$

where $C_{X_{tot}}$, contributing to the time constant $\tau_{R,X_{tot}}$, is the total capacitance on node X when both r_{s1} and r_{s2} are shorted, and C_G is the total capacitance on node G. In the



(a)



$C_X = C_{s1}+C_{s2}$ $\quad C_{gd34}=C_{gd3}+C_{gd4}$ $\quad C_G=C_{g3}+C_{g4}+C_{s2}$

$C_{s1}' = C_{s1}+C_{gd1}$ $\quad I_i=V_i/R$ $\quad C_{s3}'=C_{s3}+C_{gd2}$

$I_f=[g_{M1}/(1+r_{s1}C_{s1}'S)]V_s$

(b)

Figure 4.3: Linearized Small-signal Equivalent Circuits: (a) Switch Transistor [21]; and (b) Proposed V-I Converter.

calculation of C_G, the capacitance C_{gd34} must be multiplied by a factor β ($=g_{M34}r_{s3}$) to take the Miller effect into account.

The assumption in (4.5) suggests that a small switch S_3 be employed to reduce the charge injection error. On the other hand, based on (4.6), the width of S_2 should be chosen appropriately so that the value of α_1 is minimum. More specifically, the increase of the width of S_2 results in decreasing the corresponding on-resistance r_{s2} and increasing the gate capacitance $C_{X_{tot}}$. Note that the time constant $\tau_{s2,G}$ decreases as r_{s2} decreases, while the time constant $\tau_{R,X_{tot}}$ increases as $C_{X_{tot}}$ increase. In other words, in (4.6), the term $\tau_{s2,G}$ decreases and $\tau_{R,X_{tot}}$ increases as the width of S_2 increases. Otherwise, the term $\tau_{s2,G}$ increases and $\tau_{R,X_{tot}}$ decreases. Therefore, there exists an optimum width of S_2 such that the value of α_1 is minimum.

In order for the copier to achieve the shortest settling time, the optimum resistance R is chosen as follows. Consider the poles given by (4.4). The poles can be approximated as

$$P_{1,2} \cong -\sigma \pm j\omega \tag{4.7}$$

where

$$\sigma = \frac{1 + Rg_M}{2\alpha_1} \text{ and } \omega = \sqrt{\frac{1}{\alpha_0\alpha_1} - \sigma^2} \tag{4.8}$$

For a large R, where $Rg_{M34} >> 1$, the first term in (4.6) dominates. Thus, σ can be represented as

$$\sigma \cong \frac{g_{M34}}{2C_{X_{tot}}} \tag{4.9}$$

and the settling time is limited by the time constant of the amplifier. On the other hand, as R decreases, σ becomes a constant

$$\sigma = 1/[2(\tau_{s1,s1'} + \tau_{s2,G} + \tau_{s3,s3'} + \tau_{M1,g1})] \tag{4.10}$$

The time constants associated with the device M_1 dominates and thus limits the settling time. Due to the Miller effect and the parasitic capacitances at the input, the amplifier may have a smaller bandwidth than the device M_1. Thus, the use of small R is preferred. However, as R decreases, the value of α_0, in (4.6), increases. This may cause ω to become an imaginary number even though a sufficiently small time constant $\tau_{M1,g1}$ may be chosen. Note that the settling time is determined by the smaller absolute value of the two main poles. By (4.8), the lower bound of the resistance R should be limited by the condition that ω is a real number. In other words, fast settling time can be achieved by choosing a small R that keeps ω as a real number.

4.1.3 Simulation Results

The proposed transconductor for V-I conversion has been simulated by *PSpice*, where the process parameters of *MOSIS 2μm CMOS technology* are assumed, and the following parameters are chosen: R=2KΩ, V_{b1}=2.1V, and V_{b2}=1.5V. To determine its viability for low-voltage operation, the circuit uses a single 3.3 V power supply. The transistor M_1 has a bias current, I_{bias1}=270 μA, and a constant voltage, 1.43V, the bias voltage of the amplifier, is used as the load. The above choice is, in fact, appropriate for the use of a current copier load whose output voltage is stabilized by the amplifier while S_4 is closed. The dimensions of each transistors were chosen as follows: $(W/L)_1$=500μm/2μm; $(W/L)_2$= 500μm/2μm; $(W/L)_5$=500μm/2μm; $(W/L)_3$=30μm/2μm; and $(W/L)_4$=20μm/2μm. The switches are realized by CMOS transistors. Since the circuit settles within 0.1% at 15ns, a sampling frequency 25MHz is used in this simulation, where the control pulses for the switches have a rise and fall time of 1ns. For a case that an input sine-wave voltage ranged

between 0.55V and 1.25V is applied with an input frequency 200KHz, the simulation results show that the output currents swing between 96μA to 440μA, and the total power consumption is less than 2.5mW.

Figure 4.4 shows the transconductance vs. the input frequency, where the transconductance is defined as the ratio of the amplitude of ΔV_i over that component of the held output current ΔI_o, where both have the same frequency. In this simulation, the sample frequency is 25MHz and the sine-wave input current has a peak-to-peak value of 0.4 I_{bias1}. Results show that the input impedance is about 50 Ω for the input frequency of 2MHz, while it is approximately 57 Ω for 10MHz. Since the feedback loop has a large bandwidth, a very flat frequency response is obtained, where a roll-off of about 0.05 dB results when the Nyquist frequency is reached.

Figure 4.5 illustrates the THD (*total harmonic distortion*) vs. the amplitude of the relative input currents, where the relative input current is defined as the peak-to-peak input current divided by 2 I_{bias1}, the sampling frequency is 25MHz, and the input frequency is 25/128 MHz (or, ~200KHz). Results show that a small THD (< -65dB) is obtained for input currents which swing a range of 300μA. As the amplitude of the relative input currents is larger than 0.8, the corresponding THD increases rapidly because the small drain currents of M_1 or M_2 cause a significant settling error for the current copier.

Figure 4.6 describes the THD vs. the input frequency, where the sampling frequency is 25MHz, and the amplitude of the relative input current is 0.2 (or 0.4 I_{bias1}). As input frequency increases, the current flowing through the gate capacitance C of M_2 causes a voltage drop at V_{DS} of S_2. The nonlinear relationship between the voltage drop and the capacitive current variation increases the THD. This concludes that the THD increases with

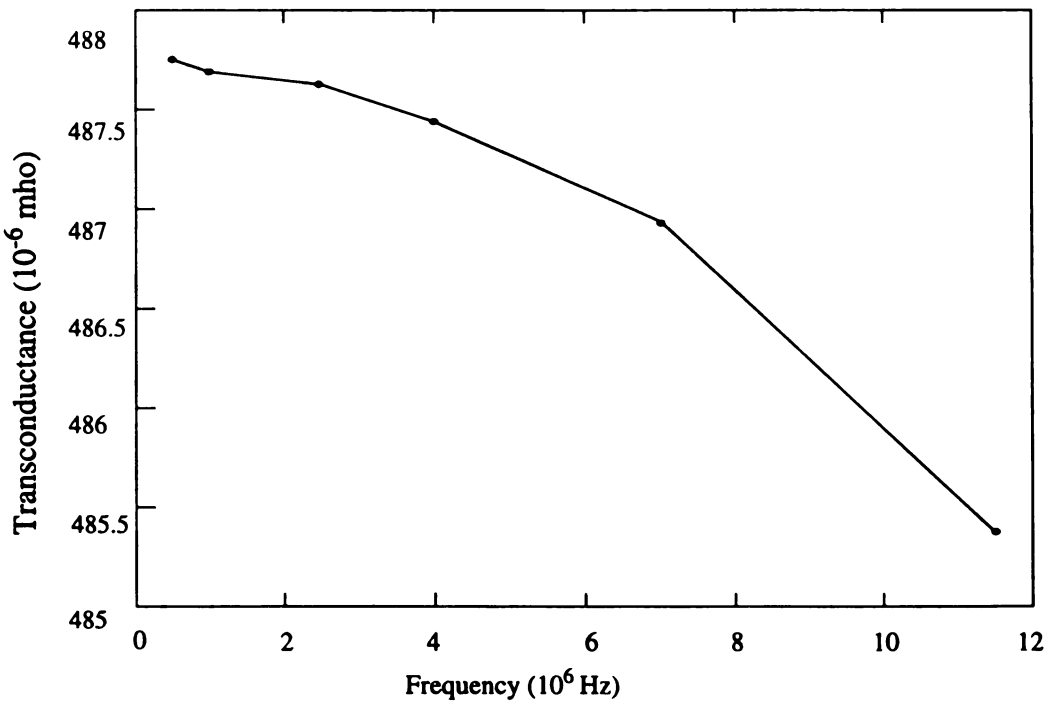


Figure 4.4: Transconductance vs. Input Frequency. (Sampling frequency, f_s=25 MHz, I_{bias1}=270μA, and $I_{i(p-p)}$=0.4 I_{bias1}.)

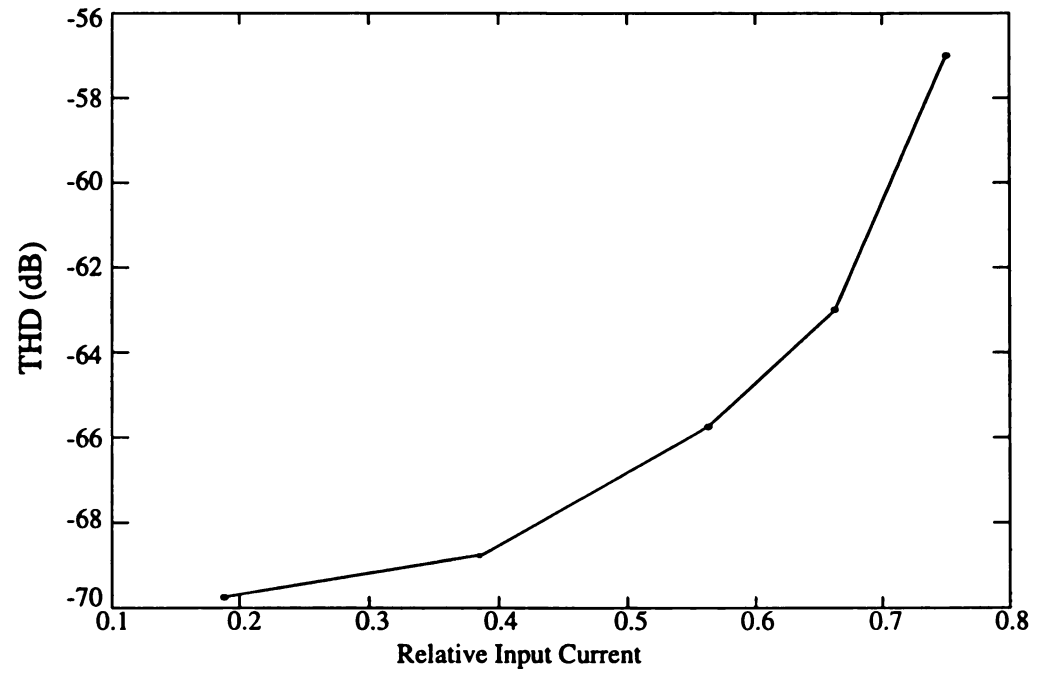


Figure 4.5: Total Harmonic Distortion (THD) vs. Relative Input Currents. (Sampling frequency f_s=25MHz, Input frequency = f_s/128, or ≈200 KHz)

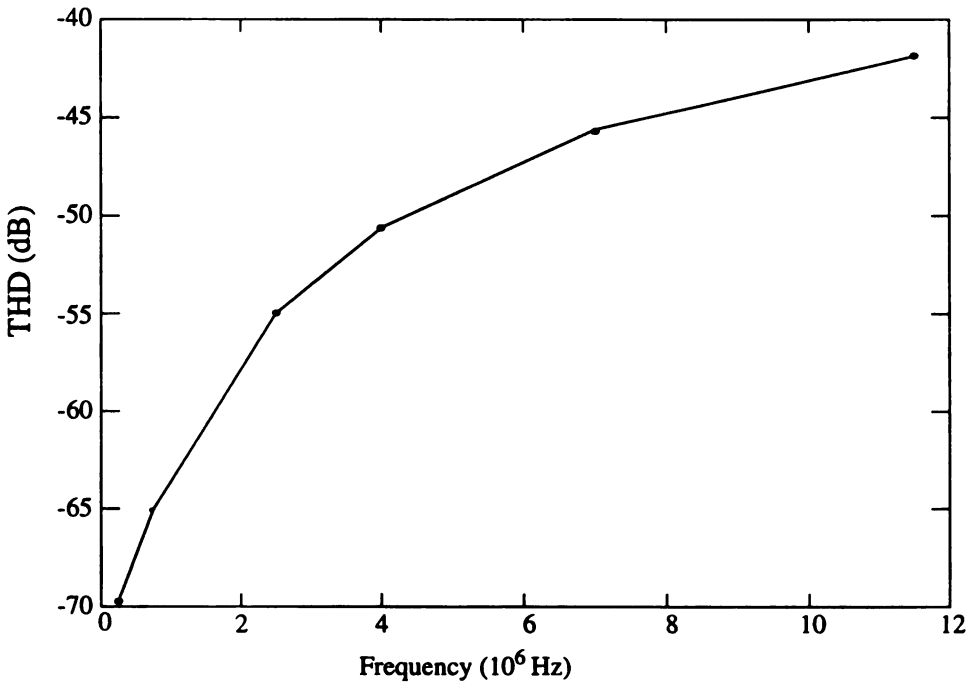


Figure 4.6: Total Harmonic Distortion (THD) Vs. Input Frequency.
(Sampling frequency fs=25MHz, and
Relative Input Current, $I_{i(p\text{-}p)} / 2\, I_{bias1}$=0.2)

the input frequency.

In summary, the simulation results show that the circuit achieves a high sampling rate, 25MHz, large dynamic range of the converted currents, and low power consumption with a low power supply (3.3V).

4.2 An Oversampled S/H Circuit

As discussed in Section 2.3.2, a high accuracy current-mode S/H circuit can be achieved by current copier with a compensator. Figure 2.11 illustrates a method of building a highly accurate oversampling current S/H circuit with an integrating feedback structure. However, the structure may result two major errors: one is from the integrator and the other from the copier CC. The use of a high-order structure may reduce the errors [29]. However, it would be penalized by the circuit complexity and the instability problem. Therefore, this task is to develop an alternative high-accuracy S/H circuit using a feedforward approach. The feedforward approach alleviates the error $E_I(z)$ due to the integrator, while the high-performance copier developed in the preliminary study is used to reduce the error resulting from the second term of (2.10).

4.2.1 The Feedforward Approach

Figure 4.7(a) illustrates the basic structure of the developed S/H circuit, where the input current I_{in} is connected to the inputs of both the gain stage and the copier CC via switches in different clock cycles. In this structure, the integrator needs only to output the error current of the copier CC and its output swing can be as much as several ten times lower than that in the structure shown in Figure 2.11(a). Thus, the error $|E_I(z)|$ is reduced

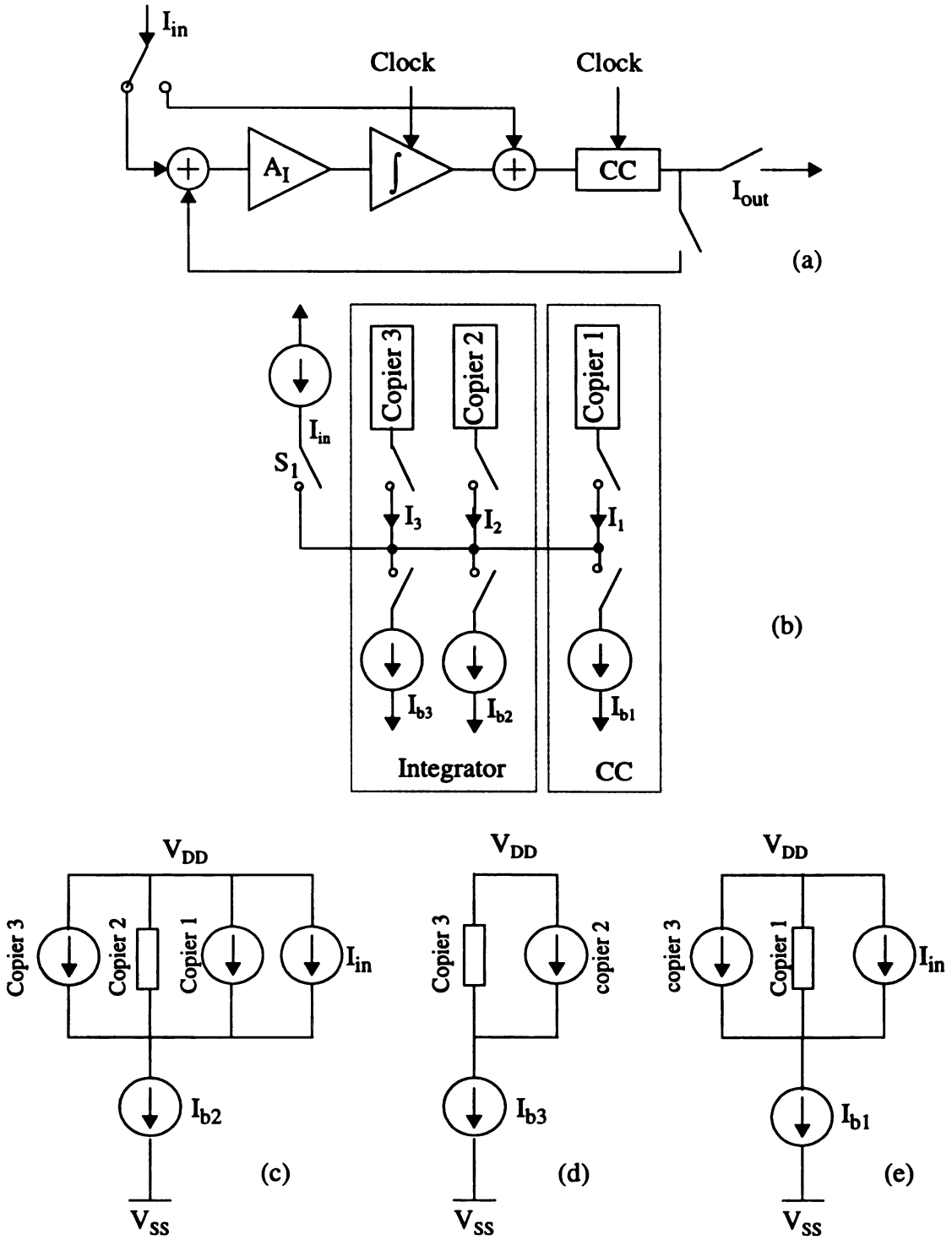


Figure 4.7: Proposed S/H Circuit with Feedforward Approach: (a) Basic Structure; (b) Current Copying Operation; and (c)-(e) Equivalent Circuits for the Three Clock Cycles in a Loop Operation.

considerably. The operation of the feedforward approach can be described by the block diagram illustrated in Figure 4.7(b), where Copier 1 is the current copier CC, while Copiers 2 and 3 form an integrator. The integrator requires two clock cycles to complete the integration, while the copier CC takes an additional clock cycle. Thus, the S/H circuit requires 3 clock cycles to complete a loop operation. The operation of the S/H circuit is summarized as follows. Let m, m+1/3, and m+2/3 denote the three clock cycles of the m-th loop operation. Copiers 2, 3, and 1 are calibrated at the first, second, and third clock cycles, respectively. Then, the current obtained by a copier in the m-th loop operation can be represented as I1(m+2/3), I2(m) and I3(m+1/3). The equivalent circuits of the S/H circuit for different cycles are given in Figure 4.7(c)-(e), where the operating copiers are represented by current sources and the calibrating one's by conductances.

During the first clock cycle of the m-th loop operation, switch S_1 is turned ON. Copier 2 is in calibration, while Copiers 1 and 3 are in operation. From Figure 4.7(c), we have,

$$I_2(m) = I_{b2} - I_{in}(m) - I_1(m-1/3) - I_3(m-2/3) + \Delta I_2(m) \qquad (4.11)$$

where $\Delta I_2(m)$ is the error of the copier 2 and $I_1(m-1/3)$ and $I_3(m-2/3)$ are the currents held in Copiers 1 and 3 at the third and second clock cycles of the (m-1)-th loop operation, respectively. At the 2nd clock cycle, S_1 is turned OFF. Copier 2 is in operation, Copier 3 is in calibration, and Copier 1 is OFF. From Figure 4.7(d), we have

$$I_3(m+1/3) = I_{b3} - I_2(m) + \Delta I_3(m+1/3) \qquad (4.12)$$

Finally, in the 3rd clock cycle, S_1 is turned ON again. Copier 1 is in calibration, Copier 3 is in operation, and Copier 2 is OFF. Therefore from Figure 4.7(e), we have

$$I_1(m+2/3) = I_{b3} - Iin(m+2/3) - I_3(m+1/3) + \Delta I_1(m+2/3) \qquad (4.13)$$

After completing the calibration of Copier 1, the m-th loop operation is completed and the same process is repeated.

The z-domain solution for the currents, $I_i(z)$, are

$$
\begin{aligned}
I_1(z) &= \frac{(1-z^{-5/3})I_{b1} + z^{-2/3}(I_{b2}-I_{b3})}{1-z^{-1}} - (1+z^{-2/3}-z^{-1})I_{in} + (1-z^{-1})\Delta I_1 + z^{-2/3}\Delta I_2 - z^{-1/3}\Delta I_3 \\
I_2(z) &= \frac{I_{b2}-z^{-1}I_{b1}}{1-z^{-1}} - (z^{-1/3}-1)I_{in} - z^{-1/3}\Delta I_1 + \Delta I_2 \\
I_3(z) &= \frac{z^{-1/3}(I_{b3}-I_{b2}) + z^{-4/3}I_{b1}}{1-z^{-1}} + (z^{-1/3}-z^{-2/3})I_{in} + z^{-2/3}\Delta I_1 - z^{-1/3}\Delta I2 + \Delta I_3
\end{aligned}
\tag{4.14}
$$

Some important properties for the proposed S/H circuit are summarized as below:

(i) The error $\Delta I_1(z)$ of the copier CC is attenuated by the transfer function $(1-z^{-1})$;

(ii) The error of the integrator, $\Delta I_2(z)$-$\Delta I_3(z)$, determines the accuracy of the S/H circuit for high oversampling ratio;

(iii) The integrator's output current, $I_3(z)$, is mainly determined by the error current $\Delta I_1(z)$ of the copier CC; and

(iv) The effect of the input current on the integrator current is attenuated by the transfer function $(1-z^{-1/3})$, where the oversampling ratio is 3 times of that provided by the transfer function $(1-z^{-1})$.

For a high oversampling ratio, the integrator has a very small output current. If the bias currents of copiers 2 and 3 are chosen to be the same, then both error currents $\Delta I_2(z)$ and $\Delta I_3(z)$ are virtually equal, i.e., $|\Delta I_2(z)-\Delta I_3(z)|$ is almost zero. Therefore, by Property (ii), the S/H circuit can accomplish a very high accuracy.

4.2.2 Structure and Operation

Figure 4.8(a) shows the schematic diagram of the oversampled current S/H circuit using the feedforward approach described in Figure 4.7. The current copier CC is realized by the current-storage transistor M_1, while the integrator is implemented with two current-storage transistors M_2 and M_3. The negative-gain feedback amplifier, realized by a simple inverter circuit shown in Figure 4.8(b), is used to stabilize the voltage on Node X enhancing the accuracy of both *Copier CC* and the integrator. For structural simplicity and fast convergency, we choose the gain A_I=1.

All switches, except S_1, are implemented with simple CMOS switches. Note that the simple CMOS switch has large on-state capacitance which is equal to the gate-source capacitance of its switching transistor. Since S_1 is connected to Node X, the input of the feedback amplifier, and its stray capacitance, as the dotted lines shown in Figure 4.8(a), is in parallel with the input of the amplifier, the on-state capacitance will strongly affect the settling time. Thus, for fast settling time, the on-state capacitance of S_1 much be kept as small as possible. In this implementation, a regulated cascode stage, as shown in Figure 4.8(c), where both M_{i21} and M_{i22} are switching transistors, the drain current of M_{i21} is connected to Node X, and the drain of M_{i22} is connected to the ground. The pair transistors M_{i1} and M_{iL1} form a feedback amplifier for reducing the input impedance of the switch so that high-linearity current transfer can be attained even when the input current source I_{in} has low output impedance. The pair transistor M_{if} and M_{ifL} form a level shifter to maximize the gate-source voltage difference among M_{i1}, M_{i21}, and M_{i22}. For a given current range, the use of the level shifter will reduce the transistor size and the output

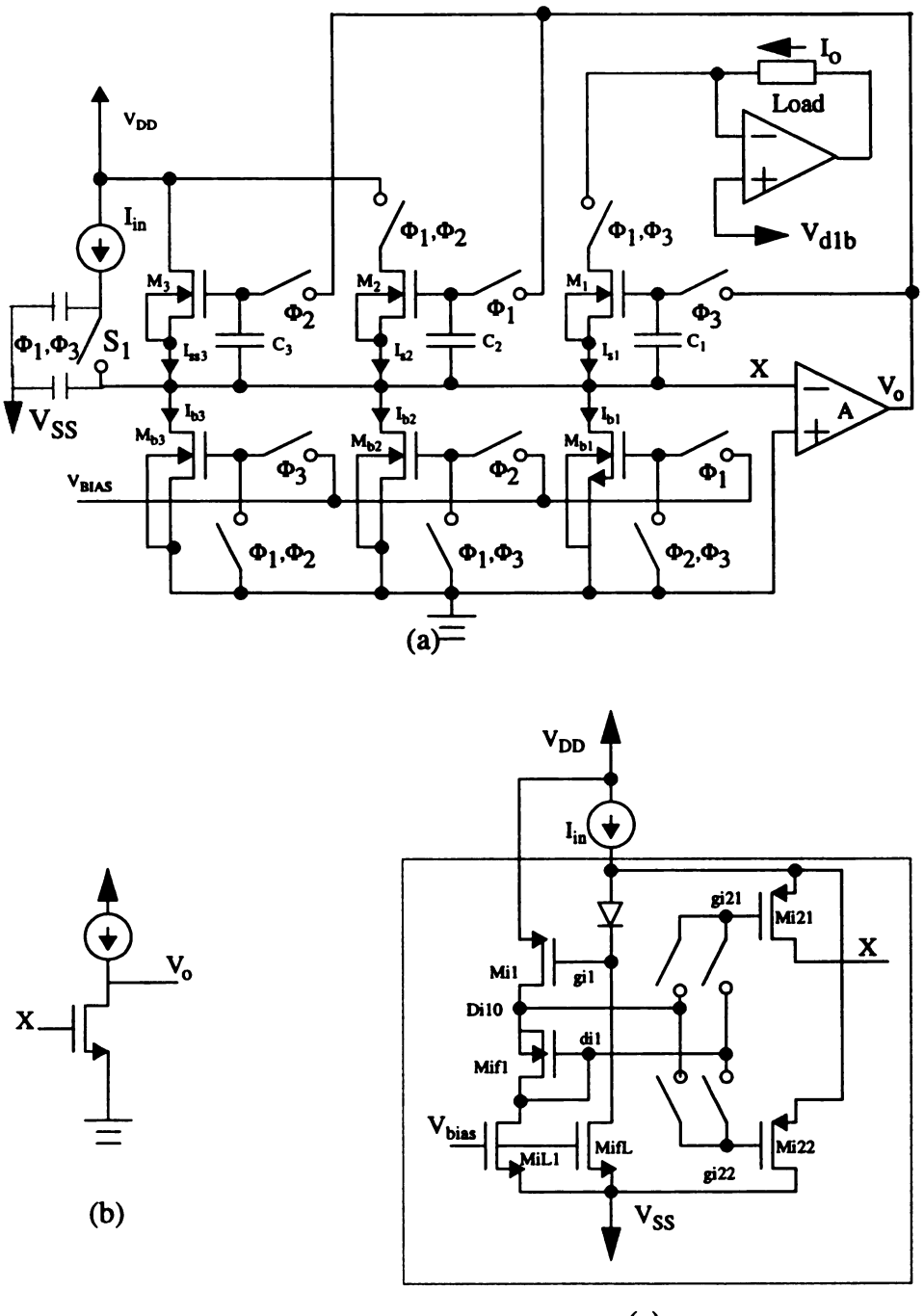


Figure 4.8: Transistor-level Implementation of Proposed S/H Circuit:
(a) Schematic Diagram; (b) Amplifier; and (c) Input Stage.

capacitance of the switch, and improve the settling speed. A regulated-cascode output stage with very high output impedance is also used so that the load will not affect the drain voltage of M_1 and thus keeping high accuracy and speed of the S/H circuit.

The bias currents I_{b1}, I_{b2}, and I_{b3} are generated by M_{b1}, M_{b2}, and M_{b3}, respectively, with a bias voltage, V_{BIAS}. The bias current must be chosen properly so that M_1, M_2, and M_3 have the correct bias. Assume that the input current has a bias I_{inb}, while I_{1b}, I_{2b}, and I_{3b} denote as the bias currents of M_1, M_2, and M_3, respectively. Using (4.14), the following relations between the bias currents I_{bi} and the bias currents I_{ib} and I_{inb}, of the input current and that in the devices, can be obtained:

$$I_{b1} = I_{1b} + I_{3b} + I_{inb}$$

$$I_{b2} = I_{1b} + I_{2b} + I_{3b} + I_{inb}$$

$$I_{b3} = I_{2b} + I_{3b}$$

In this implementation, we choose the bias currents $I_{1b}=I_{inb}=400\mu A$ and $I_{2b}=I_{3b}=200\mu A$. Thus, $I_{b1}=1mA$, $I_{b2}=1.2mA$, and $I_{b3}=0.4mA$. The bias currents are obtained by selecting an appropriate voltage V_{BIAS} and proper transistor sizes for M_{bi}, i=1,2,3.

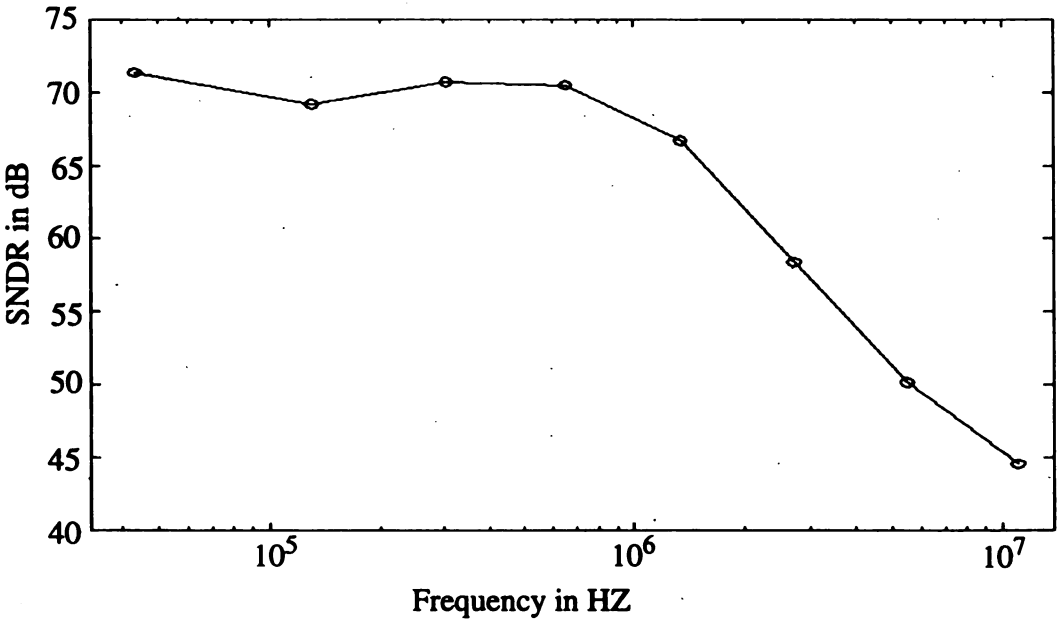
4.2.3 Simulation Results

The S/H circuit has been simulated by *Pspice*, where the parameters 2μm SCNA20 CMOS technology is used and 3.3V supply voltage is assumed. Simulation results show that the calibration of a current-storage transistor takes only 10ns for settling to 0.1% accuracy. Thus, in this simulation, we choose 15ns for a clock cycle. This implies that it takes 45ns, 3 clock cycles, for the loop operation in Figure 4.7(a). In other words, the cir-

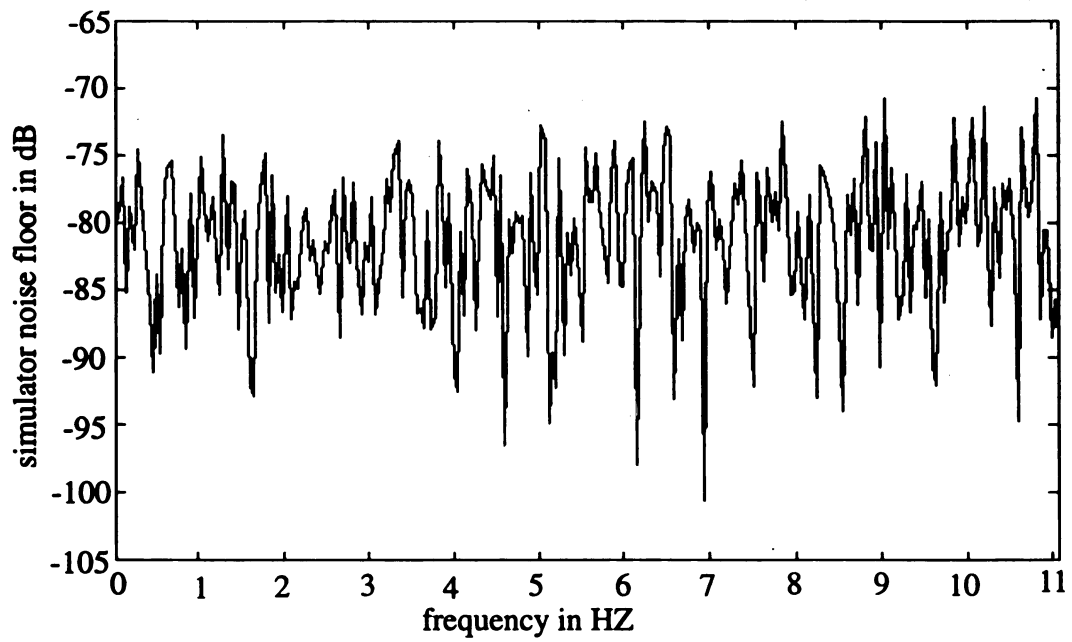
cuit can accomplish a sample rate of 22MSamples/s. Figure 4.9(a) shows the calculated *signal-to-distortion ratio* (SDR) of the output current I_{out} as a function of the signal frequency, where a sinusoidal input current with a 100μA peak-to-peak amplitude is applied; and then a 512-point FFT analysis for the output current is made, where the output current is taken at the end of the operating state of M_1. The SDR is defined as the ratio of the signal amplitude over the highest amplitude of the harmonic that has a frequency different from the signal. The input frequency is varied from very low to the Nyquist frequency, 11MHz. Results show that the SDR is higher than 60dB for input frequency lower than nearly 2MHz, or an oversampling ratio higher than 5.5. It should be mentioned that the saturation of the SDR at the low frequencies is caused by the limited accuracy provided by the *Pspice* simulator. The simulation errors result in a *noise floor*, as shown in Figure 4.9(b), which is obtained by applying a DC current to the S/H circuit and taking a 100μA peak-to-peak sinusoidal input current as a 0dB reference. In general, if no computational errors exist, no harmonics on the spectrum occurs when a DC input current is applied. Therefore, the simulation noise floor indicates the computational errors. In this simulation, the noise floor limits the SDR to 70.7dB for a 100μA peak-to-peak sinusoidal input current, and the AC current level is bounded by the distortion of the input switch and the output circuit.

4.3 Discussion

A simple transconductor circuit for V-I conversion is presented. The circuit is comprised of a simple yet high-linear current copier and a resistor, where the resistor can be realized on chip. Results show that a high-linearity of the V-I conversion is achieved even



(a)



(b)

Figure 4.9: Simulation Results: (a) Signal-to-Distortion (SDR) Ratio; and (b) Simulation Noise Floor.

though a small resistor is implemented. With the small resistance, a large dynamic range of the converted currents is obtained with a small swing of the input voltages. Thus, the circuit is viable for low-voltage operation. The sampling frequency of the V-I conversion can be increased if the channel length of the devices is further reduced. Based on the salient features described above, the proposed circuit is well suited for high-speed and low-power signal processing applications.

This study presents also a high-accuracy CMOS oversampling current S/H circuit using a feedforward approach. In an integrating feedback structure, the error current resulted from the integrator determines the performance of the S/H circuit. Conventionally, the integrator has an output current which is nearly equal to the input current in amplitude. Thus, the large error current of the integrator degrades the performance of the S/H circuit. As a result, it needs the used of high-order structure to resolve the accuracy problem and thus requiring high complex circuitry for implementing the S/H function. This study proposes a simple feedforward approach to reduce the output current of the integrator. Consequently, high accuracy is attained with a simple structure and a small oversampling ratio. The transistor level design of the S/H circuit has been simulated and simulation results are very promising.

Chapter 5

Analog-to-Digital Converter Circuits

This chapter presents a new high-speed, high-resolution, and low-power switched-current cyclic A/D converter [40]. Cyclic or algorithmic conversion is well known for its ability to achieve high resolution within small silicon area; the redundant signed digit (RSD) approach still reinforces the hardware simplicity. The cyclic conversion algorithm [24] is based on the conventional restoring numerical division principle [24], while the RSD cyclic conversion [41] is based on the SRT division principle [42]. The converter circuits in [24] and [41] takes 4 and 3 cycles to double a current. Both use the dynamic calibration technique to alleviate the errors due to component mismatches. However, the accuracy of the multiplication is still limited due to two major error effects, charge-feedthrough and non-zero output conductance of the copier. The errors are introduced and accumulated at each cycle. Therefore, to achieve high accuracy and high speed, it is necessary to reduce the number of cycles required for doubling a current.

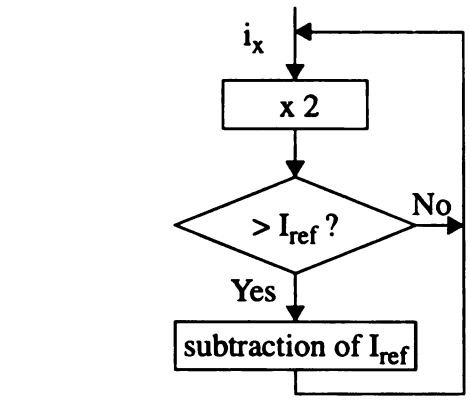
In this chapter, both conversion algorithms and the circuit implementations are reviewed in Sections 5.1 and 5.2, respectively. Section 5.3 presents a 2-cycle RSD cyclic converter circuit [34].

5.1 Cyclic Conversion Algorithms

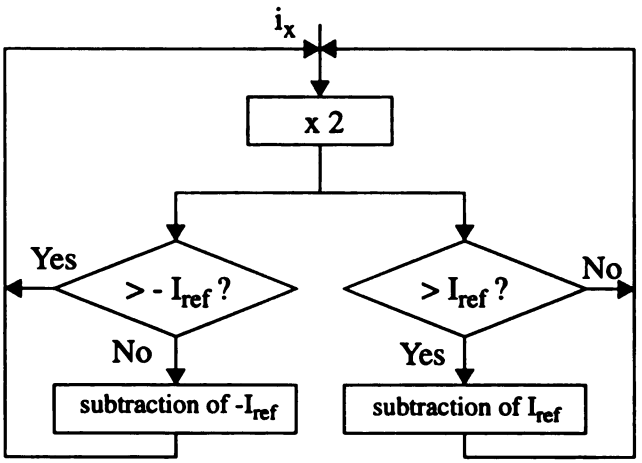
Figure 5.1 illustrates two cyclic conversion algorithms presented in [24,41]. The cyclic conversion algorithm [24] in Figure 5.1(a), referred to as *RC algorithm*, is based on the conventional restoring numerical division principle, while the RSD cyclic conversion [41] in Figure 5.1(b), referred to as RSD algorithm, is based on the SRT division principle. The RC algorithm uses only one comparator and one reference current, and the RSD algorithm requires two comparators with two reference currents. On the other hand, the comparator tolerance in the RC algorithm is equal to the resolution of the A/D converter, and the comparator tolerance in the RSD algorithm is much larger. Due to the larger comparator tolerance, the RSD algorithm has been widely used to simplify the comparator design, to enhance the speed performance, and to reduce the power consumption.

Figure 5.2 illustrates the transfer characteristics of the RC algorithm. For the ideal case, as shown in Figure 5.2(a), where no comparator error is considered, the residual current is I_{ref} when $i_x=I_{ref}/2$. In other words, the boundary i.e., I_{ref}, of the convergency region, the shaded region, is reached when $i_x=I_{ref}/2$. However, when the comparator error is taken into consideration, the residual current can easily fall outside of the shaded region, as illustrated in Figures 5.2(b) and 5.2(c), due to the errors of the comparator and the loop operation. These errors will cause either divergence or wrong digital output codes. As a result, implementing the RC algorithm requires a high accuracy comparator and an operational amplifier with low offsets.

Figure 5.3 illustrates the transfer characteristics of the RSD algorithm and its convergence region. For the ideal case, as shown in Figure 5.3(a), it has a very large margin between the boundary and the current ranged $-I_{ref}/2 \le i_x \le I_{ref}/2$. Therefore, implementing



(a)



(b)

Figure 5.1: Cyclic Analog-to-Digital Conversion Algorithms:
(a) RC Algorithm; and (b) RSD Algorithm.

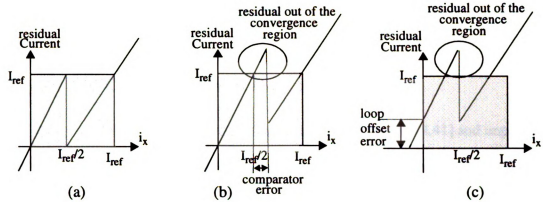


Figure 5.2: Transfer Characteristics of RC Algorithm: (a) Ideal Case; (b) with Comparator Error; and (c) with Loop Offset Error.

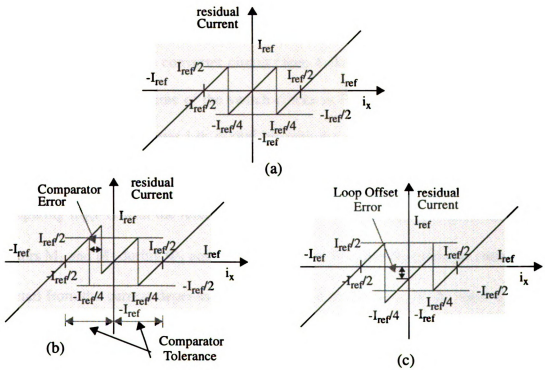


Figure 5.3: Transfer Characteristics of RSD Algorithm: (a) Ideal Case; (b) with Comparator Error; and (c) with Loop Offset Error.

the RSD algorithm can tolerate larger inaccuracy in the comparators and offset in the operation loops, as illustrated in Figures 5.3(b) and 5.3(c).

5.2 Cyclic A/D Converter Circuit Designs

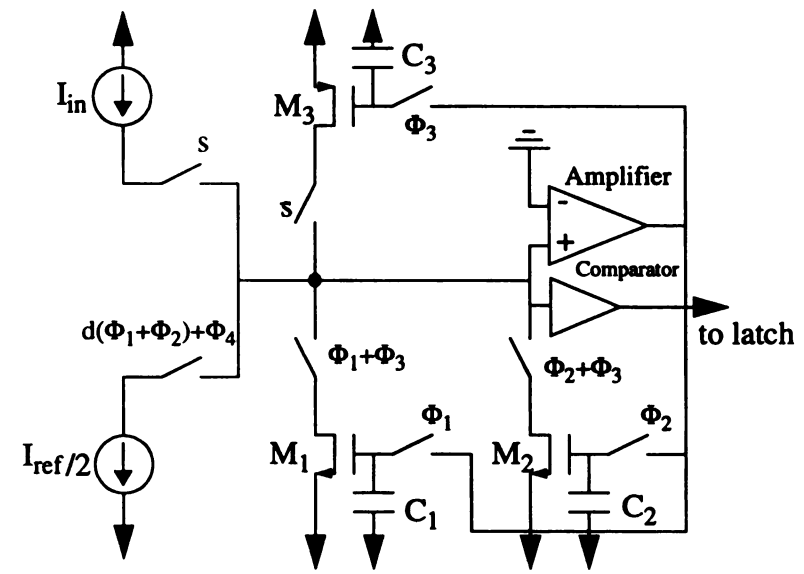
Two cyclic A/D converter circuits have been presented in [24,41] and implemented the RC algorithm and the RSD algorithm, respectively. This section reviews the circuit design and operation of both converters.

5.2.1 A 4-cycle cyclic converter

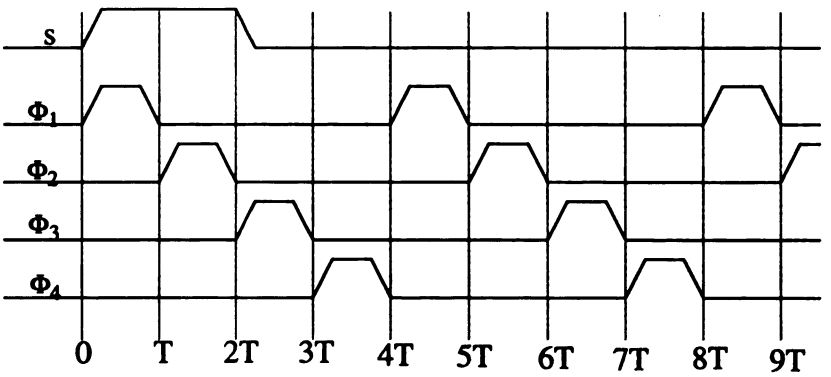
Figure 5.4(a) shows the schematic of a cyclic A/D converter [24] implementing with the RC algorithm. The converter circuit takes 4 clock cycles to generate one bit, as indicated by the timing scheme of the switch clocks in Figure 5.4(b). At first, let us consider the process that generates i-th digital bit with the s-signal having its state *low*. We denote the current sampled by the transistor M_3 as $Id_3(i-1)$ and the digital bit d_{i-1} produced by comparing $Id_3(i-1)$ with the reference current. The current $Id_3(i-1)$ will be sampled by transistors M_1 and M_2 during Φ_1 and Φ_2, respectively. Whether the reference current I_{ref} is subtracted from the current depends on the state of d at that time, or the value d_{i-1}. Note that $d_{i-1}=\text{sign}[Id_3(i-1)-I_{ref}/2]$ is a two-valued variable with $d_{i-1}=1$, if $Id_3(i-1)-I_{ref}/2 > 0$, and $d_{i-1}=0$ otherwise. Thus, we can write

$$Id_1(i) = Id_2(i) = Id_3(i-1) - d_{i-1}I_{ref}/2. \qquad (5.1)$$

In Φ_3, the sum of the drain currents $Id_1(i)$ and $Id_2(i)$ of the transistors M_1 and M_2 will be sampled by M_3. Thus, we have



(a)



(b)

Figure 5.4: A 4-cycle Cyclic A/D Converter: (a) Schematic; and (b) Switching sequence.

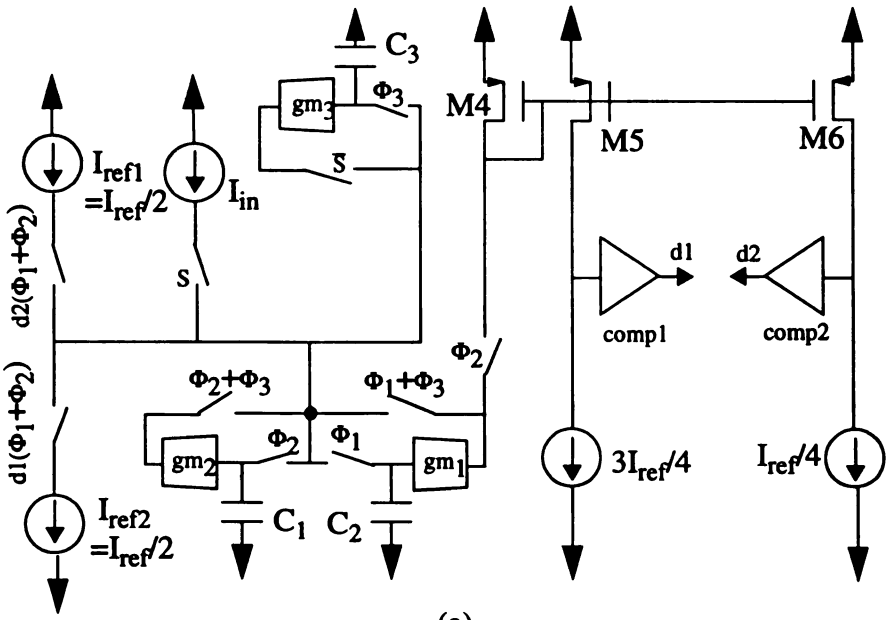
$$Id_3(i) = 2\,[Id_3(i-1) - d_{i-1}I_{ref}/2]. \qquad (5.2)$$

The digital bit d_i is obtained in Φ_4 by comparing $Id_3(i)$ with $I_{ref}/2$. The iteration (5.2) performed by Figure 5.4(a) is exactly the same one as defined by Figure 5.1(a), where i_x is replaced by Id_3. The s-signal is used to control the beginning of the conversion. Its effect is to substitute I_{in} for $Id_3(0)$ in (5.1). Another additional comparison is needed to generate the most-significant bit d_0.

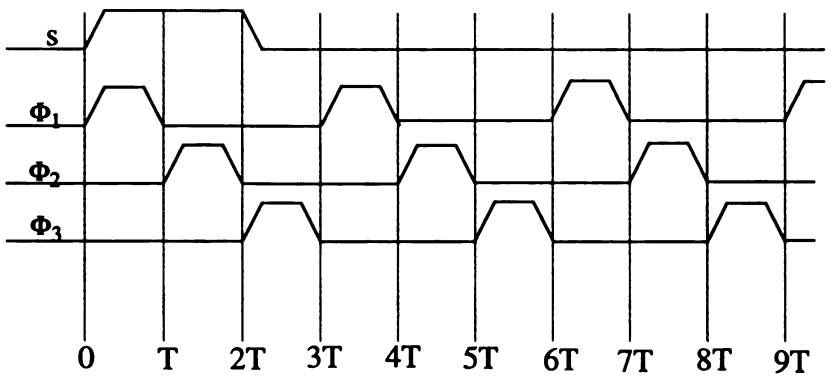
The converter achieves a 10-bit accuracy and a speed 250 kbit/s [24]. The low speed is mainly due to its use of INFCCI copiers.

5.2.2 A 3-cycle RSD cyclic converter

The number of clock cycles for one bit conversion can be reduced from 4 in [24] to 3 by removing the clock cycle Φ_4, and making the comparison in parallel with computing the residual current [41]. More specifically, the doubled current held in P_1 is copied to N_1 in the clock cycle Φ_1. Since N_1 is idle during the clock cycle Φ_2, the current held in N_1 is compared with $I_{ref}/2$ for determining the converters bit. Figure 5.5(a) illustrates the cyclic A/D converter circuit developed in [41], where three copiers are employed as the residual amplifier which takes 3 cycles to double a current. The self-regulated cascode copiers with the transconductance gm_1, gm_2, and gm_3, are used to achieve high speed, and no feedback amplifier is needed. The transconductance gm_1 is calibrated during the clock cycle Φ_1. During Φ_2, the current held in the copier with gm_1 is sent to the current mirror consisted of transistors M_4, M_5, and M_6, where the current is amplified by a factor of 2. The amplification is achieved by selecting the aspect ratios of M_5 and M_6 to be twice that of M_4. The out-



(a)



(b)

Figure 5.5: A 3-cycle Cyclic A/D Converter: (a) Schematic; and (b) Switching sequence.

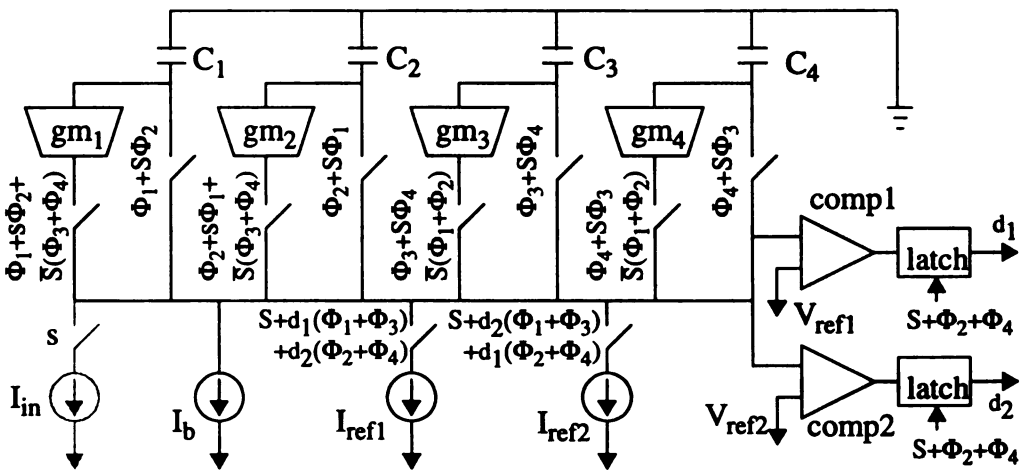
put currents I_{d5} and I_{d6} of the current mirror are compared with $(3/4)I_{ref}$ and $(1/4)I_{ref}$, respectively. The comparison results, d_1 and d_2, are then sampled at the end of Φ_2. Both bits d_1 and d_2 are used to control which reference current, I_{ref1} or I_{ref2}, is used for next comparison. The converter achieves a simulated 10-bit resolution and 4.5 MS/s sample rate with pipeline structure [41].

5.3 Proposed 2-Cycle RSD Cyclic A/D Converter

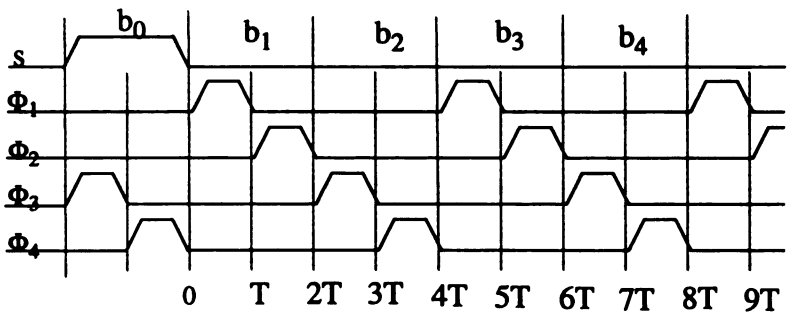
To alleviate the error effects in current copiers for high accuracy and high speed cyclic A/D converter, the number of cycles for a residual amplifier must be reduced. This section proposes a 2-cycle RSD cyclic A/D converter circuit design which achieves a 12-bit accuracy and 20 Mbit.s speed. This section presents the residual amplifier, the RSD algorithm, and the decoding scheme for the proposed A/D converter.

5.3.1 Structure and Operation

Figure 5.6(a) shows the proposed converter, where four current copiers represented by gm_{1-4} are employed. The circuit requires only two cycles to generate a ternary bit, represented by the two single-bit binary signal d_1 and d_2. During the conversion state, where the start signal s is low, the four copiers are grouped as two copier pairs, gm_{1-2} and gm_{3-4}. At each bit conversion, the residual current, the sum of the currents stored in a copier pair, is copied during Φ_1 and Φ_2 (or Φ_3 and Φ_4) to two current copiers in the other copier pair. Specifically in Figure 5.6(a), the sum of the currents in gm_3 and gm_4 is copied to gm_1 during Φ_1, and then copied to gm_2 during Φ_2. The sum of the currents stored in the pair



(a)



(b)

Figure 5.6: A 2-cycle Cyclic A/D Converter: (a) Schematic; and (b) Switching sequence.

(gm_1,gm_2) becomes the new residual current which will be copied back to the pair (gm_3,gm_4) during Φ_3 and Φ_4, respectively. Since it takes one cycle to copy the residual current in the pair (gm_1,gm_2) to a current copier in the pair (gm_3,gm_4), the residual amplifier takes only two cycles Φ_1 and Φ_2 (or Φ_3 and Φ_4) to double a current.

Two comparators are used to monitor the transconductance currents indirectly. The relation between the input voltage and the current in the transconductance can be expressed as $I_i=gm_iV_{ci}$, where, I_i is the current of transconductance gm_i and V_{ci} the voltage on the capacitance C_i. Therefore, instead of comparing the currents I_i with the reference currents, we can compare the voltages V_{ci} with the reference voltages V_{ref1} and V_{ref2}. The use of voltage comparison instead of the current comparison can simplify the circuit and reduce the power by avoiding using the current mirrors. Since large comparator errors are permitted by a RSD algorithm, neither exact transconductances nor accurate comparators are needed. The comparison results are latched at the ends of Φ_2 and Φ_4, where the conversions for one bit are completed. The single-bit binary outputs d_1 and d_2 of the latches control the two reference currents I_{ref1} and I_{ref2} to implement a RSD algorithm. It will be seen later that the conversion accuracy will not be affected by the mismatch of I_{ref1} and I_{ref2}.

The start signal s is used to sample the input current I_{in}. When s is high, a transconductance pair (gm_3,gm_4) is set to the calibration state and to receive the input current, while the pair (gm_1,gm_2) is turned off. Each reference current is turned on by the s-signal to produce a suitable bias current for the input current source. At the same time, the input current is compared with the two reference levels $\{gm_jV_{ref1}, gm_jV_{ref2}\}$ to produce the most significant bit b_0, where j=1,2,3,4. Here, the transconductances are chosen with the same

values. At the end of the s-signal, we have the residual current $I_R(0)$ in the conductance pair (gm_3,gm_4) and the most significant digital bit $d_1(0)$ and $d_2(0)$ in the latches.

Without loss of the generality, we assume that the residual current for the odd bits are held in the pair (gm_1,gm_2), while that for the even bits are in the pair (gm_3,gm_4). Let $I_j(i)$ denote the current stored at transconductance gm_j, j=1,2,3,4, and $I_R(i)$ be the residual current for the i-th bit. During Φ_1, the switch on the top of reference current I_{ref1} is controlled by the single-bit binary signal d_1 while the switch on the top of reference current I_{ref2} is controlled by the single-bit binary signal d_2, thus we have for the odd bit i, the current in gm_1 is expressed as

$$\begin{aligned} I_1(i) &= I_b+d_1(i-1)I_{ref1}+d_2(i-1)I_{ref2}-[I_3(i-1)+I_4(i-1)] \\ &= I_b+d_1(i-1)I_{ref1}+d_2(i-1)I_{ref2} -I_R(i-1) \end{aligned} \qquad (5.3I)$$

During Φ_2, the switch on the top of reference current I_{ref1} is controlled by the single-bit binary signal d_2 while the switch on top of reference current I_{ref2} is controlled by the single-bit binary signal d_1, we have the current in gm_2

$$\begin{aligned} I_2(i) &= I_b+d_2(i-1)I_{ref1}+d_1(i-1)I_{ref2}-[I_3(i-1)+I_4(i-1)] \\ &= I_b+d_2(i-1)I_{ref1}+d_1(i-1)I_{ref2} -I_R(i-1) \end{aligned} \qquad (5.3II)$$

and the new residual current can be expressed as

$$I_R(i) = [I_1(i)+I_2(i)]=2I_b+[d_1(i-1)+d_2(i-1)](I_{ref1}+I_{ref2}) -2I_R(i-1). \qquad (5.4)$$

The current in the transconductances is detected using the voltage on the node X. During Φ_2, the gate switch of the transconductance gm_2 is closed and its input is connected to node X. The current in this transconductance will determine the voltage on node X. Thus, the outputs of the comparators will determine the range of the current in gm_2. In other words, the

digital outputs d_1 and d_2 are determined by the current in gm_2, which is half the residual current. At the end of Φ_2, the comparison results will be sampled by the latches. The digital signals d_1 and d_2 will be changed from $d_1(i-1)$ and $d_2(i-1)$ to $d_1(i)$ and $d_2(i)$, respectively. Similar to (5.3), we have the current obtained by gm_3 in Φ_3,

$$I_3(i+1) = I_b+d_1(i)I_{ref1}+d_2(i)I_{ref2}-[I_1(i)+I_2(i)] = I_b+d_1(i)I_{ref1}+d_2(i)I_{ref2} -I_R(i),(5.5I)$$

and the current obtained by gm_4 in Φ_4,

$$I_4(i+1) = I_b+d_2(i)I_{ref1}+d_1(i)I_{ref2}-[I_1(i)+I_2(i)] = I_b+d_2(i)I_{ref1}+d_1(i)I_{ref2} -I_R(i).(5.5II)$$

The new residual current is

$$I_R(i+1) = [I_1(i+1)+I_2(i+1)]=2I_b+[d_1(i)+d_2(i)](I_{ref1}+I_{ref2}) -2I_R(i). \qquad (5.6)$$

During Φ_4, the gate switch of gm_4 is closed and its input is connected to node X. The current in this transconductance is used to determine the digital outputs d_1 and d_2. At the end of Φ_4, the new digital bit $d_1(i+1)$ and $d_2(i+1)$ will be sampled by the latches.

Equations (5.4) and (5.6) show that the scheme of implementing the RSD algorithm. The three output states of the redundant bit is d_1d_2={00, 01,11}. It should be noted that the two reference currents are averaged by the two clock cycles for a bit conversion. As a result, the sum of the two reference currents determines the reference level, and the mismatch between them will cause no loss of the resolution of the A/D converter circuit.

In (5.4) and (5.6), the old residual current is multiplied by a factor of (-2), before it is added to the new residual current. This is not the same as a conventional scheme, where a factor of +2 is used. The difference will result in a digital output which is not in a standard binary code. Thus, a decoder is introduced to change the generated code to a stand binary code. The negative sign will also change the determination of the comparator levels which will be discussed later.

5.3.2 Convergency Range

The convergency range is the current range of the transconductances, in which the residual current will not decrease or increase unboundly. The determination of the convergency ranges will permit us to find out the input current range for a given I_b and $I_{ref1}+I_{ref2}$, in which the converter can work properly. It permits us also to fix the comparator levels that gives maximum comparator error tolerance.

The residual current $I_R(i)$ is divided into three regions by the two comparators. They can be defined as:

$$\begin{aligned} &\text{R0:} && I_R(i) \le I_L && \Rightarrow && d_2d_1=00 \\ &\text{R1:} && I_L < I_R(i) < I_U && \Rightarrow && d_2d_1=01 \\ &\text{R2:} && I_U \le I_R(i) && \Rightarrow && d_2d_1=11, \end{aligned} \tag{5.7}$$

where I_L is the residual current level, at which the first comparator output d_1 changes state, and I_U the residual current level, at which the second comparator output d_2 changes state. In the above definitions, I_U being larger than I_L is assumed. Initially, the residual current can be in any of the regions. Using (5.4) or (5.6) one can find where the new residual current will be, when an initial residual current is given.

Figure 5.7 shows some possible transitions of the residual currents between different regions, with the initial residual current $I_R(1)$ being in R0. Case (a) corresponding to the situation that the initial residual current has such a value that the new residual current $I_R(2)$ will remain in R0. With the decrease of the initial residual current $I_R(1)$, the new residual current $I_R(2)$ will go into region R1, as indicated in Figure 5.7 (b). For a even more smaller $I_R(1)$, the residual current $I_R(2)$ will go into the region R2, and R2 can also be large

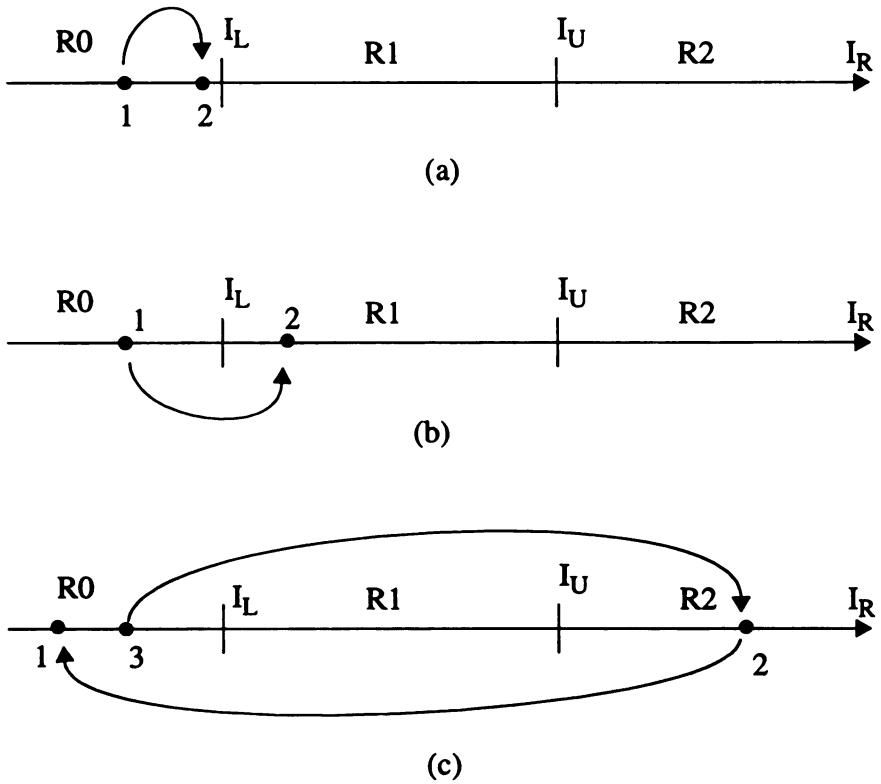


Figure 5.7: Residual Current Transition.

enough, such that residual current $I_R(3)$ goes back to region R0. For convergency, we require

$$I_R(3) > I_R(1) \tag{5.8}$$

Using (5.6) and (5.7), we have

$$I_R(2)=2I_b-2I_R(1);\ I_R(3)=2I_b+2I_{ref}-2I_R(2) \tag{5.9}$$

where $I_{ref}=I_{ref1}+I_{ref2}$. Similarly, if we assume that $I_R(1)$ and $I_R(3)$ are in R2, and $I_R(2)$ in R0, the convergency condition will be changed to

$$I_R(3) < I_R(1) \tag{5.10}$$

Using (5.6) and (5.7), we have

$$I_R(2)=2I_b+2I_{ref}-2I_R(1);\ I_R(3)=2I_b-2I_R(2) \tag{5.11}$$

Form (5.8)-(5.11), we have

$$2I_b/3-2I_{ref}/3 < I_R < 2I_b/3+4I_{ref}/3 \tag{5.12}$$

In the (5.12), the time index of the residual current is dropped off since the inequality must be meet by all the residual currents for convergency.

5.3.3 Comparator Levels

To determine the comparator levels, we have to find out the convergency regions for the different residual computation rules. From (5.6), there are three different ways to compute the new residual current from the initial one. Putting different possible values of d_2d_1 into (5.6), we have

$$I_R(2) = 2I_b - 2I_R(1) \qquad \text{rule 0}$$

$$I_R(2) = 2I_b + I_{ref} - 2I_R(1) \qquad \text{rule 1} \tag{5.13}$$

$$I_R(2) = 2I_b + 2I_{ref} - 2I_R(1) \qquad \text{rule 2}$$

The new residual current $I_R(2)$ must be in the range given by (5.12), no matter which rule is used. Thus, from (5.12) and (5.13), we obtain the convergency regions for different residual computation rules

$$\begin{aligned} &2I_b/3-2I_{ref}/3 < I_R < 2I_b/3+I_{ref}/3 && \text{rule 0} \\ &2I_b/3-0.5I_{ref}/3 < I_R < 2I_b/3+2.5I_{ref}/3 && \text{rule 1} \\ &2I_b/3+I_{ref}/3 < I_R < 2I_b/3+4I_{ref}/3 && \text{rule 2} \end{aligned} \qquad (5.14)$$

The convergency regions given in (5.14) are plotted in Figure 5.8. There are overlap convergency regions for rule0-1 and rule1-2. The middle points of both overlapping regions, $I_L=2I_b/3+I_{ref}/12$ and $I_U=2I_b/3+7I_{ref}/12$, are selected as the comparator levels. Thus, like a conversional RSD algorithm, the one presented here provides a tolerance of $\pm I_{ref}/4$ for the comparator's inaccuracy.

5.3.4 Decoding

As mentioned before, after one bit is generated, the residual current is multiplied by a factor of (-2). This is different than a conventional converter, where it is multiplied by a factor of (+2). The generated output digital codes must be transformed to standard binary codes and a decoder is developed. For a 2N-bit converter, the relation between the input current I_{in} and two one bit digital codes d_2 and d_1 can be written as

$$\begin{aligned} I_{in} &= I_0+I_{ref}\sum_{i=0}^{2N-1}[d_2(i)+d_1(i)](-2)^{-i} \\ &= I_0+I_{ref}\sum_{i=0}^{N-1}[d_2(i)+d_1(i)]2^{-i}-I_{ref}\sum_{i=0}^{N-1}[d_2(i)+d_1(i)]2^{-(2i+1)} \end{aligned} \qquad (5.15)$$

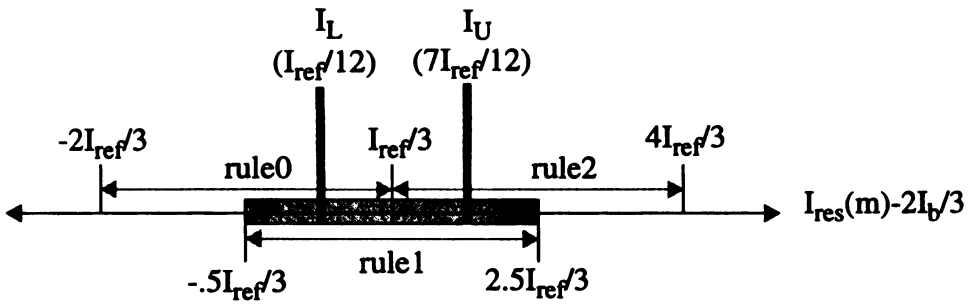


Figure 5.8: The Comparison Levels with Respect to the Convergence Regions.

Where I_o is a constant offset. Expressing I_o in the form

$$I_o = I_o' + I_{ref} \sum_{i=0}^{N-1} 2^{-2i}$$

we can rewrite (5.15) as

$$\begin{aligned} I_{in} &= I_o' + I_{ref} \sum_{i=0}^{N-1} [d_2(i)+d_1(i)]2^{-2i} + I_{ref} \sum_{i=0}^{N-1} [(1-d_2(i))+(1-d_1(i))]2^{-(2i+1)} \\ &= I_o' + I_{ref} \sum_{i=0}^{N-1} [d_2(i)+d_1(i)]2^{-2i} + I_{ref} \sum_{i=0}^{N-1} [\overline{d_2(i)}+\overline{d_1(i)}]2^{-(2i+1)} \end{aligned} \tag{5.16}$$

where $\overline{d}_1$ and $\overline{d}_2$ denote the logical complementary of d_1 and d_2 respectively. By defining

$$d_2'(i)\ d_1'(i) = \begin{cases} d2(i)\ d1(i) & \text{for even i} \\ \overline{d2(i)}\ \overline{d1(i)} & \text{for odd i} \end{cases} \tag{5.17}$$

we can express (5.16) as

$$I_{in} = I_o' + DI_{ref} \tag{5.18}$$

$$D = \sum_{i=0}^{2N-1} [d_2'(i)+d_1'(i)]2^{-i} \tag{5.19}$$

Based on (5.17) and (5.19), the decoder can be implemented as shown in Figure 5.9.

5.4 Circuit Description and Simulation Results

This section describes the circuits used to implement the proposed A/D converter circuit, including both the analog circuits and digital circuits for the clock generating and conversion control. Finally, the simulation results are given to verify the operation.

5.4.1 Circuit Implementation

Figure 5.10(a) shows the proposed cyclic A/D converter circuit. The transconductances gm_j, j=1,2,3,4, in Figure 5.6(a) can be implemented using any of the current copiers

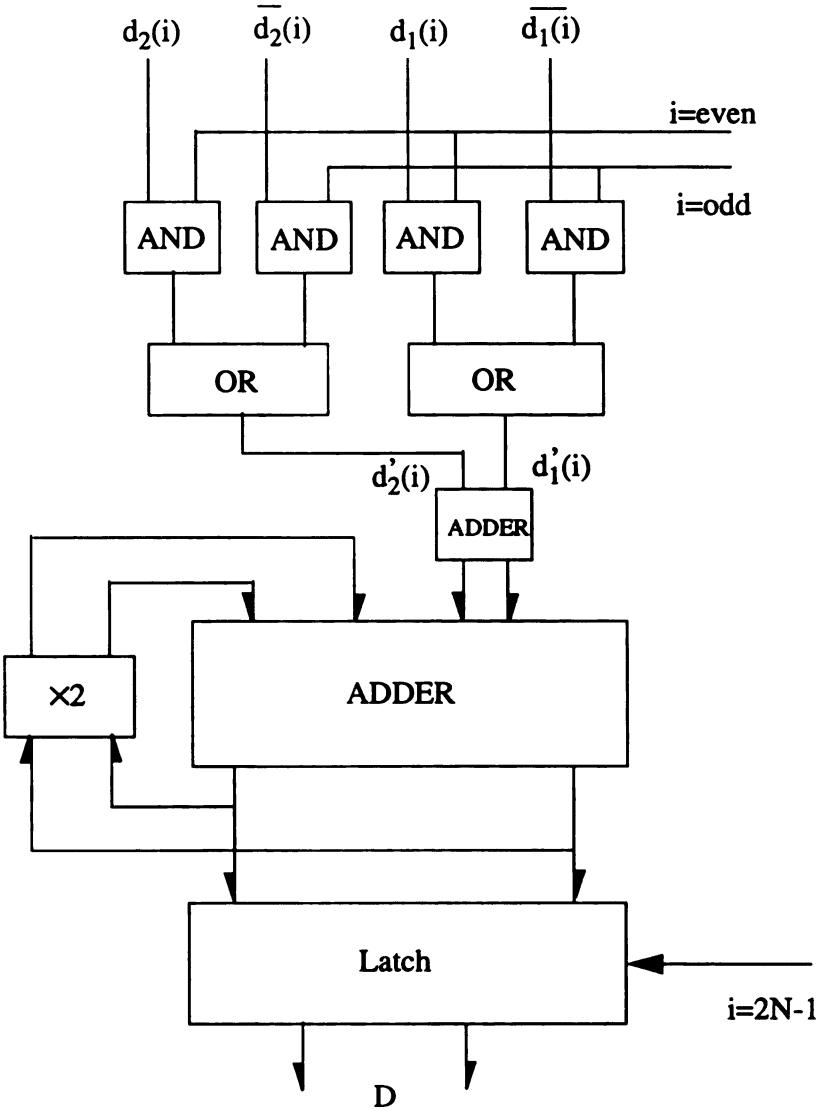


Figure 5.9: The Decoder.

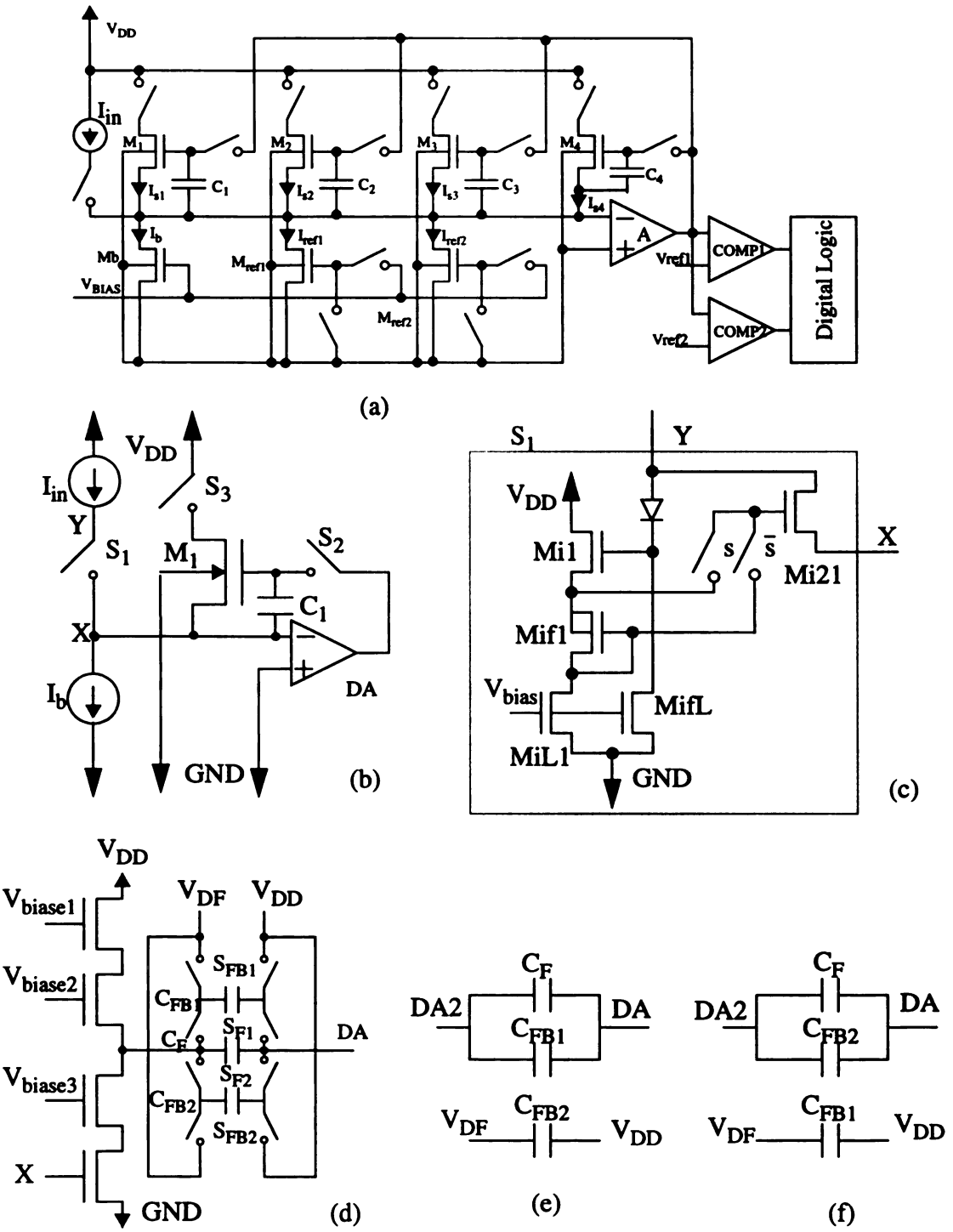


Figure 5.10: Proposed A/D Converter Circuit: (a) Schematic; (b) Modified FNFCC; (c) Input Stage with Switch S_1; (d) Feedback Amplifier; and Equivalent Circuits of the Level Shifter for (e) Φ_1 & Φ_3; and (f) Φ_2 and Φ_4.

discussed previously in Chapters 2 and 3. For high performance A/D converter design, this implementation employs the current copiers, as shown in Figure 5.10(b), which is modified from the FNFCCs in Figure 3.12(a). The copier has the best speed and noise performances under low supply voltage, and also permits the use of a simple N-well CMOS process that is preferred for digital circuit design considerations.

Three switches, S_1, S_2, and S_3, are used in the current copier. Switches can be generally implemented with simple CMOS transistors. However, the simple CMOS switch has large on-state capacitance which may slow the settling time. In this implementation, both S_2 and S_3 are realized by simple CMOS switches, but not S_1. Since S_1 is connected to node X, an input of the of the amplifier, its on-state capacitance must be kept as small as possible to reduce the settling time. Therefore, switch S_1 in Figure 5.10(c) is employed, where both M_{i21} and M_{i22} are the switching transistors, and the drain of M_{i21} is connected to node X. Note that the switching transistors are operated in saturation when they are turned on. Thus, the stray capacitance is only the overlap capacitance between gate and drain of the switching transistor, and this capacitance is much smaller than that in a simple CMOS switch.

Figure 5.10(d) shows a high-gain feedback amplifier which is used to reduce the error due to the increased output conductance. The amplifier is a simple cascode stage with a capacitive level shifter. With the level shifter, the output of amplifier can be higher than the power supply V_{DD}. The level shifting maximizes the gate source voltage difference V_{gs1} of M_1 for low power supply applications. Maximizing V_{gs1} will reduce both thermal noise and the error due to charge feedthrough effect.

The level shifter uses a three-capacitance approach to avoid the effect of the stray resistances on the settling time, thus, small switches can be used. The switches are con-

trolled, such that, for one operation cycle of the amplifier, where one of the current copiers is calibrated, capacitance C_{FB1} is connected between V_{DD} and V_{DF}, and C_{FB2} is paralleled with C_F. In the other operation cycle, the positions of C_{FB1} and C_{FB2} are exchanged. The equivalent circuits of the level shifter for different clock phases are illustrated in Figures 5.10(e) and 5.10(f). Suppose at time k the voltage across the capacitance C_F is $V_{CF}(k)$ and $C_{FB1}=C_{FB2}=C_{FB}$, then, at time k+1, the capacitance will have a voltage $V_{CF}(k+1)= [C_F V_{CF}(K)+C_{FB}(V_{DD}-V_{DF})]/(C_F+C_{FB})$. This expression gives a steady-state solution $V_{CF} = V_{DD} - V_{DF}$. The voltage on the output node DA is shifted up by $V_{DD}-V_{DF}$, relative to that on the node DA2. This structure of the level shifter has the advantage that a signal path from DA2 to DA is provided directly by C_F. The parasitic resistances of the switches have little effect on the settling of the copier.

It should be mentioned that the pair transistors M_{i1} and M_{iL1} form a feedback amplifier for reducing the input impedance of the switch so that high-linearity current transfer can be attained even if the output impedance of the input current source is small. The pair transistors M_{if} and M_{ifL} form a level shifter to maximize the gate-source voltage difference among M_{i1}, M_{i21}, and M_{i22}. For a given current range, the use of the level shifter will reduce the transistor size, improves the settling speed, and reduce the output capacitance of the switch. Simulation results show that the improved switch achieve a settling time of 8ns.

For time-interleaven parallel ADC structure, the drain current of M_{i22} can be used as the input of the other ADC cell, as shown in Figure 5.11. The number of channels can be increased for parallel ADC structure by increasing the switching transistors.

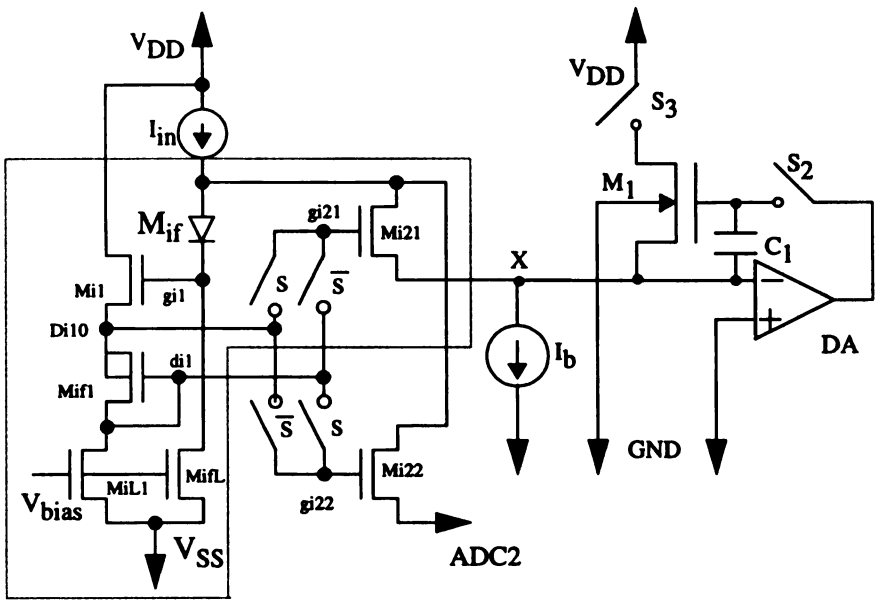


Figure 5.11: Current Copier with the Input Stage.

5.4.2 Control Circuitry

Figure 5.12(a) shows the control circuitry for managing the reference currents I_{ref1} and I_{ref2}, where the inputs of the control logic include s, $d_1(i)$, $d_2(i)$, Φ_1, Φ_2, Φ_3, and Φ_4.

The control signals for the input switches and the switches at the gates and drains of the current-storage transistors can be generated using a state machine. More specifically, the clock cycles presented in Figure 5.6(b) can be described by a state machine shown in Figure 5.12(b). The converter samples the input current during the state s=1. The current is then sampled by the current-storage transistor pair (M_1,M_2) or (M_3,M_4), depending on the state of the mode-4 counter before sampling. In Figure 5.6, we assumed that the current is sampled by the pair (M_3,M_4). Because the symmetry of the two pairs, the difference will make no effect on the conversion results. After the input current is sampled, the residual current will be transferred from one pair to another during the states $\Phi_{1\text{-}2}$ and $\Phi_{3\text{-}4}$. Every time the residual current changes its location a new digital bit will be generated, increasing the bit number i by 1. Because the residual current goes back and forth between the two pairs, the converter goes back to state Φ_1 after the state Φ_4. The mode-N counter counts how many bits is converted. After the last bit is obtained, a carry will be output by the mode-N counter, as shown in Figure 5.12(c), and the converter goes back to its initial state to sample a new input current. The whole process repeats itself again.

5.4.3 Simulation Results

Consider the schematic diagram of the proposed switched-current cyclic A/D converter in Figure 5.10(a), where four copiers implemented by the current-storage transistors

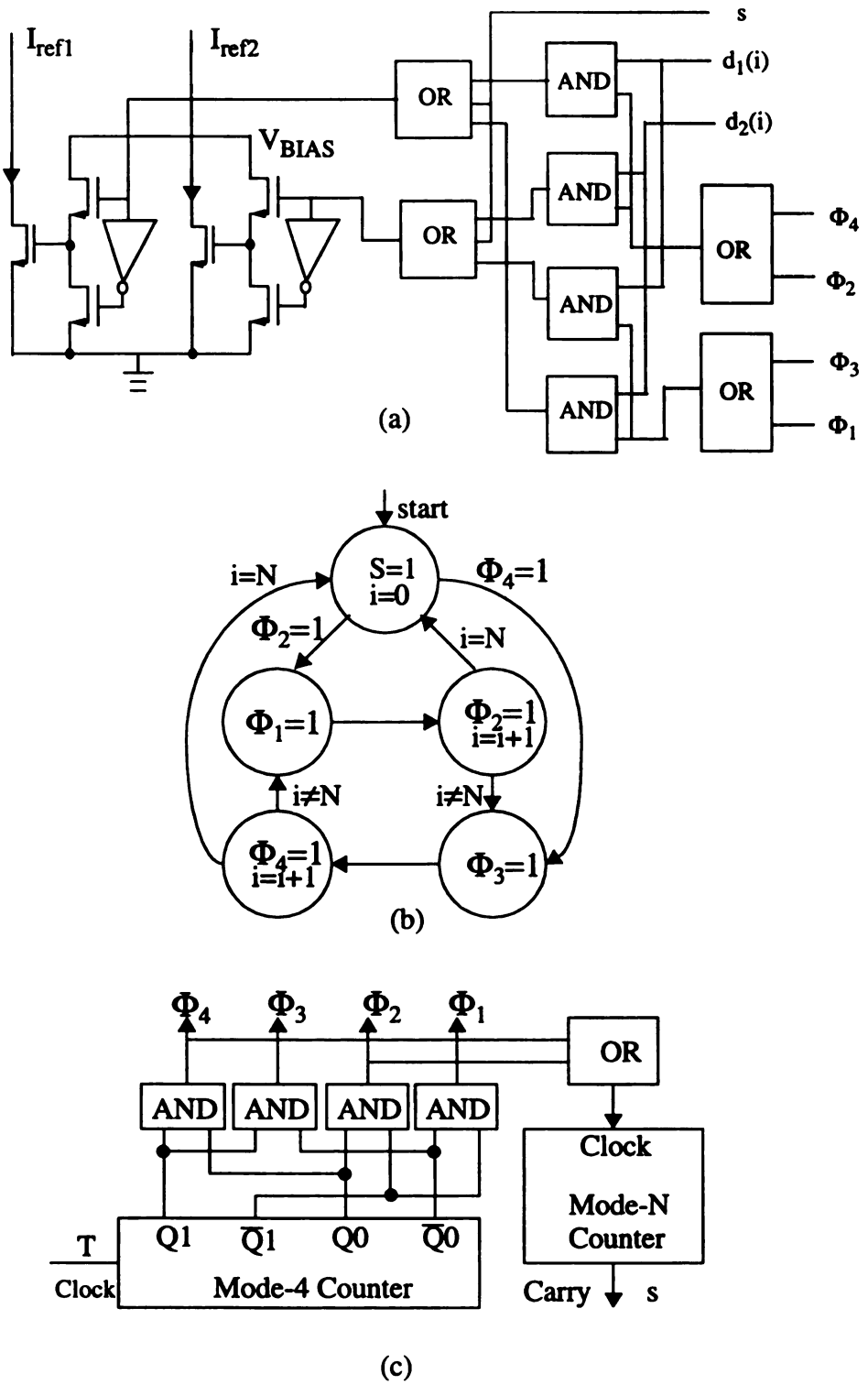


Figure 5.12: Control Circuitry: (a) Reference-Current Generating Circuit; (b) State-Transition Diagram; and (c) Logic Implementation.

M_1-M_4, and the two reference currents, I_{ref1} and I_{ref2}, and the bias current, I_b, are generated by the transistors M_{ref1}, M_{ref2}, and M_b; Switch S_1 is implemented by the circuit shown in Figure 5.10(c), while other switches are realized by simple CMOS switches; The circuit in Figure 5.10(d) is employed as the feedback amplifier; and the comparators and the digital logic, implemented by CMOS transistors, are used to produce the digital codes. The circuit has been simulated by ***pspice***, where the *SCDN20* 2μm CMOS process with level-2 transistor parameters and a supply voltage of 3.3V are employed. The reference and biased current are chosen as I_{ref1}=I_{ref2}=170μA and I_b=1mA. Simulation results show that the total power consumption is about 7mW, including 2mW for the input current switching unit.

Figure 5.13(a) shows a typical current waveform in a current-storage transistor, while Figure 5.13(b) plots the partial output of I_{ref1} to demonstrate the three states in the RSD approach, where the current pulse widths of 50ns, 25ns, and 0ns, represent the state 2, 1, and 0, respectively. (Since the clock rate for calibration is 25ns, i.e., one bit is obtained in every 50ns.) Figure 5.13(c) summarizes the accuracy of the proposed ADC which achieves a 12-bit resolution for the input currents ranged between 350μA and 850μA.

According to the simulation results in Figure 5.13(b), the time period for the steady-state can be further reduced and thus increasing the conversion rate. In addition, since a larger settling error is allowed for those lower significant bits, a shorter clock cycle can be used to perform the calculation. Therefore, the use of multiple clock cycles can also increase the conversion rate. We believe that the average bit conversion can be moved to 20-25ns in a 12-bit conversion.

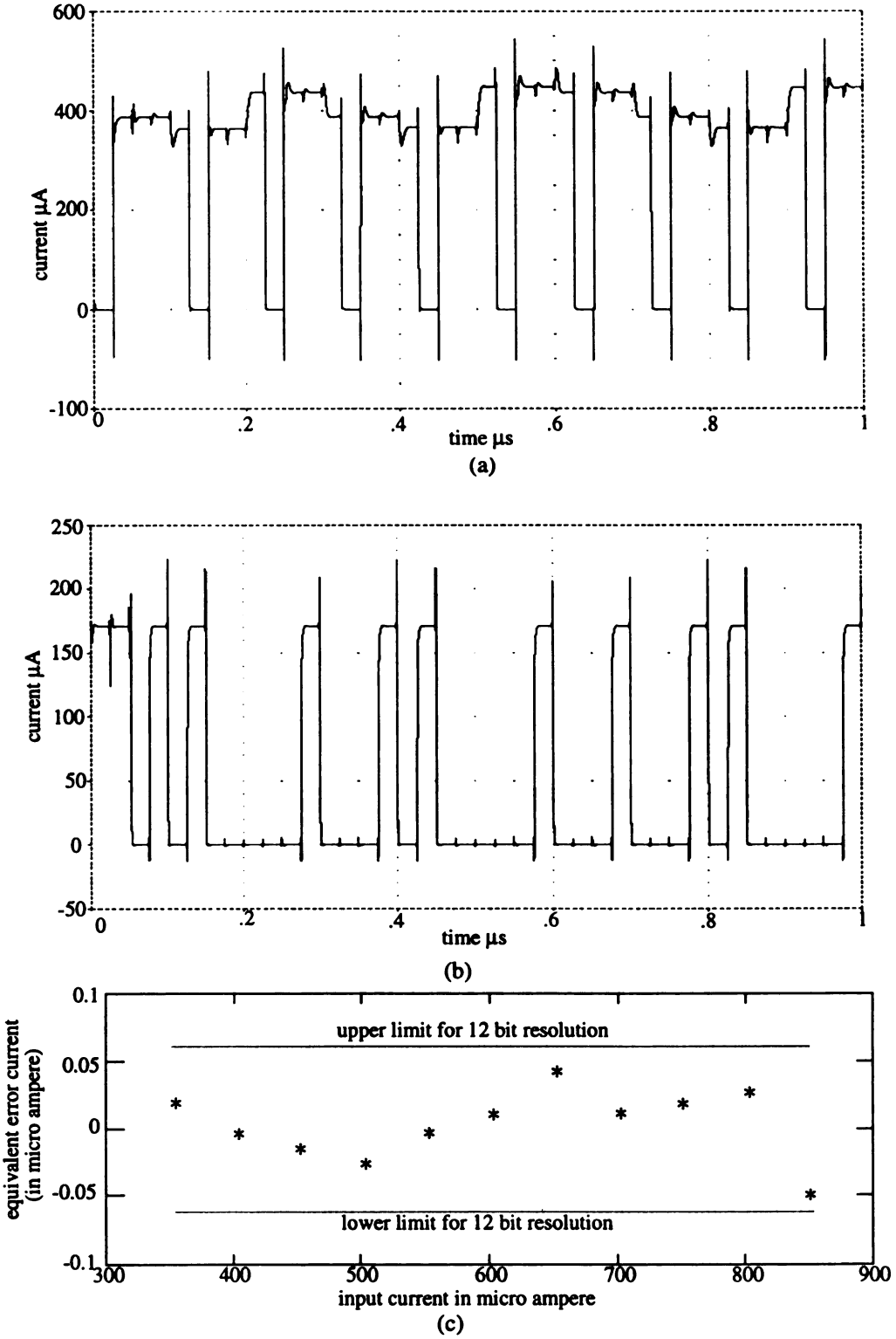


Figure 5.13: Simulation Results: (a) Typical Current Waveform; (b) Partial Outputs for I_{ref1}; and (c) 12-bit Resolution.

5.5 Discussion

This chapter presents a high performance cyclic A/D converter circuit design. The high performance is attributed to: (1) the use of high performance current copiers; (2) the use of a high performance residual amplifier which takes two clock cycles to double a current; (3) the use of an efficient Cyclic RSD algorithm which provides 1.5b resolution without using two matched reference currents.

The performance of A/D converter can be improved by further reducing the charge injection errors [43]. A fully differential switched-current A/D converter has been investigated, where high performance fully differential current copiers are implemented. Fully differential architectures are frequently employed in both continuous-time and switched-capacitor circuits to achieve the highest level of analog performance [44]. The approach reduces distortion by cancelling even-order harmonics and reduces cross-talk from neighboring digital circuits through common-mode and power supply rejection of the amplifiers. Thus, a fully differential current copier can further reduce charge injection errors [43].

Chapter 6

Conclusion

Portable televisions, camcoders, and compact disk players have been made available by consumer electronics companies. Cellular phones are going to provide virtually unlimited access for voice communications; and laptops, notebooks and palmtops are the fastest growing types of computers. Portable multimedia terminal will come into being, which will be capable of providing speech communication, data transfer, handwriting recognition, and high-quality, full motion video. Each of these technologies relies on VLSI for cost and power-consumption effective implementation. Given sufficient complexity, even CMOS dissipation levels become excessive especially where high frequency is involved. It is necessary to optimize the VLSI-technology for low-power operation of both digital and analog circuits.

SI technique has received considerable attention as an alternative for analog circuit design. However, existing SI circuits cannot make the theoretically expected performance due in part to the use of non-optimal current copiers, its basic building blocks. Based on our development of design methodologies and synthesis process for optimally generating low power and high performance CMOS current copiers, SI technique becomes feasible.

The objective of the thesis research is to develop new generation of high-performance, low-power/low-voltage current-mode circuits. The emphasis is placed on the development of sample/hold circuits, and analog-to-digital circuits for mixed-signal IC's in future portable equipment.

6.1 Summary and Contribution

In Chapter 1, the low power design issues were addressed and the advantages of using SI technique for designing analog portion of mixed-signal ICs were introduced. A number of previous works for designing high performance A/D converters and S/H circuits were reviewed. The research tasks were outlined. Chapter 2 reviews existing current copiers, switched-current data converters, and switched-current S/H circuits

Based on the analysis of the charge-injection error, Chapter 3 outlines the design trade-offs among accuracy, speed performance, and power consumption and addresses the stray effect of the switches which may degrade the speed performance of the copiers. It has been shown that the stray effects can be alleviated by reducing the stray capacitance of the current-steering switches, or by separating the large current-steering switches from the small current-sample switches, for the copier to achieve high speed operation. A simple, yet high performance current copier, FNFCC, was developed. Simulation results verify the operation and demonstrate high performance accomplished by the developed copier.

Chapter 4 presents the design of a simple high performance SI V-I converter with the S/H function and an oversampled high linear SI S/H circuit. The developed V-I converter is comprised of a high-linear current copier and a resistor. Result shows that, with the small resistor, a large dynamic range of the converted current can be obtained with a small

swing of input voltages. Thus, the circuit is viable for low-voltage operation. The developed oversampled SI S/H circuit adopts a simple forward approach to reduce the output current of the integrator. With a simple structure and a small oversampling ratio, the circuit achieves high accuracy.

In Chapter 5, a high performance cyclic A/D converter circuit design was presented. The high performance is attributed to: (1) the use of high performance current copiers; (2) the use of a high performance residual amplifier which takes two clock cycles to double a current; (3) the use of an efficient Cyclic RSD algorithm which provides 1.5b resolution without using two matched reference currents.

This work has established guidelines for designing high-speed current copiers and switched-current circuits, making them more attractive for the next generation low-power, low-voltage, high-speed high-accuracy analog circuit design. The major contributions can be categorized as follows:

(a) Developed a performance analysis process for current copiers and a synthesis process for developing high-performance current copiers for low-power/low-voltage signal processing applications.

(b) Developed two types of S/H circuits; and

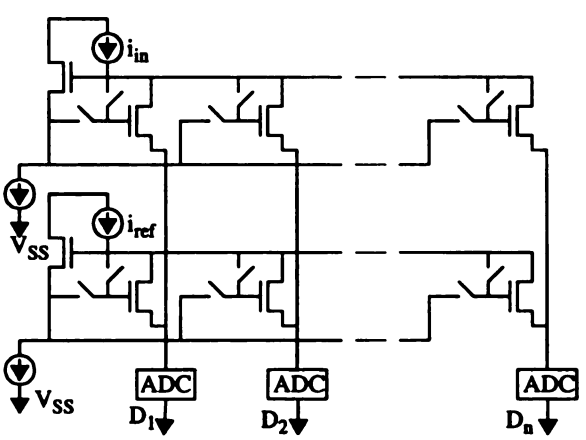
(c) Developed a novel high-speed and low-power cyclic A/D converter design.

The developed circuits meet the design requirement not only for portable equipments, but also for video signal processing, such as HDTV, high-frequency digital communications, and waveform acquisition/instrumentation. This research has demonstrated that this development is not merely an academic curiosity, but an important practical technology for the future.

6.2 Future Work

Circuit synthesis is to select the right circuit from among existing alternatives to fulfill the intended application. Conventionally, guided from past experiences designers choose a promising circuit architecture that could meet the given set of performance specifications. However, because of the large number of variables involved, it is difficult to accurately predict the circuit behavior. The circuit may partially fulfill the performance specifications, but it is not optimally designed. As a result, existing SI circuits cannot meet the expected theoretical performance even though with novel circuit structures. Thus, it is necessary to develop a design methodology for high-performance/low-voltage CMOS SI circuits. This can be accomplished by constructing the parameter space of current copiers for a given set of performance specifications and providing the optimally designed copiers. The performance analysis and synthesis process discussed in Chapter 3 can be further developed for synthesizing optimal current copiers and SI circuit.

In Chapter 5, a 12-b, 20 MS/s, and 7mW A/D converter circuit has been designed and simulated. The simulation results have confirmed the operation of the converter. The performance can be further improved by the following parallel-pipelined structure with calibration capability.



At any time one A/D converter will be calibrated by sending I_{ref} to the converter, The other converters will be used for conversion. The speed-up ratio of the parallel structure with n converter is (n-1) with calibration ability, while a speed-up ratio of n is achieved if no calibration capability is considered. With the calibration ability, the DC offset of different channels can be cancelled off; and the linearity can be made only determined by the units that controls the calibration of the input current and the reference current. Apparently, the sample rate increases with the number of converters. However, the increase of converters will also increase the total power consumption. It is expected that, with 10 converters, the parallel-pipelined converter achieves more than 12 bits, 40-50MS/s, and 60mW.

The performance of A/D converter also can be improved by further reducing the charge injection errors [43]. A fully differential switched-current A/D converter has been investigated, where high performance fully differential current copiers are implemented. The fully differential architectures reduce distortion by cancelling even-order harmonics and reduce cross-talk from neighboring digital circuits through common-mode and power supply rejection of the amplifiers. Based on the fully differential current copier developed in [43], it is worthwhile to develop a high performance A/D converter.

To develop high-performance D/A converters, it is necessary to develop a new current copier which is error-free from charge-feedthrough effects. The accuracy of the converter is expected to be the sum of the mismatch of components and the accuracy of the dynamic calibration. For example, 16-bit accuracy of D/A converter circuit may be realized by 8-bit accuracy of well-matched components and 8 bit accuracy with dynamic calibration. High-speed can be obtained by separating calibration from the output of the converter, making the speed of the conversion determined only by the output unit.

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