This is to certify that the

dissertation entitled

EFFICIENT TESTABILITY DESIGN METHODOLOGIES
FOR ANALOG/MIXED-SIGNAL INTEGRATED CIRCUITS

presented by

Cheng-Ping Wang

has been accepted towards fulfillment
of the requirements for

Ph.D. degree in Electrical Eng

Major professor

Date September 25, '97

EFFICIENT TESTABILITY DESIGN METHODOLOGIES FOR ANALOG/MIXED-SIGNAL INTEGRATED CIRCUITS

By

Cheng-Ping Wang

A DISSERTATION

Submitted to
Michigan State University
in partial fulfillment of requirements
for the degree of

DOCTOR OF PHILOSOPHY

Department of Electrical Engineering

1997

ABSTRACT

EFFICIENT TESTABILITY DESIGN METHODOLOGIES FOR ANALOG/MIXED-SIGNAL INTEGRATED CIRCUITS

By

Cheng-Ping Wang

More and more mixed-signal devices are being designed recently for the applications of multimedia, wireless communication, and portable data systems. The analog circuit technology conventionally employed for such applications has been gradually switched to analog/digital mixed-signal circuit technology. Even though much more complicated digital circuits have been widely used in the DSP-based mixed-signal IC, analog circuits will remain for processing or interfacing analog signals. Integrating both digital and analog on a single chip has improved performance and reduced board size and cost. However, the increasing complexity of mixed-signal circuits drastically reduces the controllability and observability of the circuit on the chip. As a result, testing of such complex circuit becomes very difficult and expensive. Therefore, the goal of the thesis study is to develop an efficient testability design system for analog/mixed-signal circuits so that all designed circuits are easily testable.

The thesis study has developed efficient testability design methodologies and testability enhancement methodologies. The developed design methodology defines a set of fault types from circuit layout, technology data, and process defect distribution, and it generates a set of test vectors based on the parameter deviation bounds which are derived from the design specification, discrete input set, and defined fault types. The test vectors

and parameter deviation bounds allow us to evaluate the fault coverage of a designed analog circuit. This methodology was developed using the inductive fault analysis (IFA) technique. However, the IFA technique requires a tremendous amount of computational time and thus it has been limited for small circuits. For reasonable large analog circuits, a hierarchical testability design methodology is developed to reduce the computational complexity. Basically, a designed circuit is decomposed into many components. The components can be further decomposed until they can be handled comfortably by the IFA technique. In other words, a circuit is decomposed as primitive cells and/or macros.

Based on the hierarchical fault macromodeling process, a hierarchical testability design system, namely, PETOMIC (Packages for Enhancing Testability Of Mixed-signal Integrated Circuit) is also developed. The system generates cell library, macro library, test set, and evaluates the fault coverage. The system has been developed and implemented in C language, Spice, and Matlab. The detail system development is discussed with examples of generating a cell library of an Opamp and a macro library of a current copier.

Some testability enhancement methodologies have also been developed in this study. Based on the given design specifications, a set of discrete inputs used for design verification, and the fault types, a set of testability design rules is developed to ensure the existence of the circuit parameter deviation bounds for these discrete inputs and for all fault types. These parameter deviation bounds are used to generate test vectors. Thus, the designed circuit can be easily testable. In addition, a high-accuracy current comparator is developed as a built-in tester (BITER). The use of BITER not only enhances the testability, but also simplifies the test generation process and reduces the test sequence length.

To my parents, brother and his wife.

ACKNOWLEDGEMENTS

I sincerely thank Professor Chin-Long Wey, my thesis advisor, for his support and valuable suggestions throughout this research. It has been a pleasure to work under his supervision and I have certainly learn a lot from him. I would also like to express my gratitude to the members of my guidance committee, Dr. James Resh, Dr. Gregory Wierzba and Dr. Chien-Peng Yuan, for taking time to serve in the committee.

I have to thank my fellow graduate students, Wei-Hsing Huang and Jin-Sheng Wang. I got much inspiration from the discussion with them.

A special thanks goes to my parents, my brother and his wife for the support and encouragement they have given me during the critical stage of my life.

A final note of appreciation must be sent to all the nice people who have ever enriched my campus life while I stayed in Michigan State University.

TABLE OF CONTENTS

LIST OF TABLES viii

LIST OF FIGURES ix

Chapter 1 INTRODUCTION 1
1.1 Objectives and Research Tasks 6
1.2 Thesis Organization 9

Chapter 2 BACKGROUND 11
2.1 Fault Definition 11
2.2 Test Generation of Switched-Current Circuits 14
2.2.1 Switched-Current Circuits 14
2.2.2 Structures and Operations 15
2.2.3 Fault Behaviors and Test Generation of an ADC 20
2.3 Analog/Mixed-Signal Testing Schemes 23
2.3.1 Design-for-Testability Techniques 23
2.3.2 BIST Designs 27

Chapter 3 FAULT MACROMODELING 30
3.1 Fault Types in Switches 31
3.2 Heuristic Fault Macromodeling Process 35
3.2.1 Example Circuit - Current Copier 36
3.2.2 Example Circuit - ADC 42
3.2.3 Discussion 49
3.3 IFA-Based Fault Macromodeling Process 50
3.3.1 Fault Classification 50
3.3.2 Testability Design Rules 56
3.3.3 Test Generation and Fault Coverage 60
3.3.4 Example 61
3.4 Discussion 72

Chapter 4 TESTABILITY ENHANCEMENT 74
4.1 Hierarchical IFA-Based Fault Macromodeling 74
4.1.1 Macro Library 76
4.1.2 Fault Coverage Estimation 82
4.2 Testability Design Rule 87

4.2.1 Development 88
4.2.2 Discussion 91
4.3 High-Accuracy Built-In Tester 91
4.3.1 Design and Operation 94
4.3.2 Simulation Results 98
4.3.3 Performance Analysis 104
4.3.4 Built-In Tester and Test Sequence 108

Chapter 5 HIERARCHICAL TESTABILITY DESIGN SYSTEM 111
5.1 CLG_Routine 111
5.2 MLG_Routine 128

Chapter 6 CONCLUSION 137
6.1 Summary 137
6.2 Future Work 139

APPENDICES 141

REFERENCES 166

LIST OF TABLES

Table 2.1	Fault types and expected outputs.	21
Table 3.1	Defect and fault count distributions.	69
Table 3.2	Defect and fault count distributions. (With inaccurate test instrument)	70

LIST OF FIGURES

Figure 1.1 Schematic diagram of a typical DSP-based mixed-signal IC. 2

Figure 1.2 Single stuck-at-fault-model-based testing in digital circuit. 4

Figure 1.3 Broad view of this thesis study. 7

Figure 2.1 Inductive fault analysis. 13

Figure 2.2 Current copier: (a) basic copier; (b) with feedback amplifier; and (c) CMOS switch with a dummy switch. 16

Figure 2.3 An SI algorithmic ADC: (a) schematic diagram; and (b) simulation results. 18

Figure 2.4 DSP-based IC with scan structures. 24

Figure 2.5 Test bus. 26

Figure 2.6 BIST design of an ADC. 26

Figure 3.1 Defects: (a) switch layout; (b) defected layout; and (c) summary of defects and circuit fault. 32

Figure 3.2 (a) Simulation results of I-V plot of M_1 with load lines for S_2; and (b) fault behavior and switching sequence. 37

Figure 3.3 Built-in tester: (a) schematic; (b) switching sequence; and (c) fault simulation results. 40

Figure 3.4 Test structure for SI algorithmic ADC: (a) schematic diagram; and (b) comparator. 43

Figure 3.5 Test sequence A: (a) fault behaviors; and (b) switching sequence. 45

Figure 3.6 Test sequence B: (a) fault behavior; and (b) type VS2 fault. 47

Figure 3.7 Step 1 of IFA-based fault macromodeling. 51

Figure 3.8 Step 2 & 3 of IFA-based fault macromodeling. 52

Figure 3.9 Switches: (a) schematic; (b) fault model for voltage switch; and (c) fault model for current switch. 54

Figure 3.10 Relationship between parameter deviation and performance deviation. 57

Figure 3.11 Example for the definition of parameter deviation bounds. 57

Figure 3.12 Equivalent circuit of the portion including transistor and current switch of the current copier, and its I-V characteristic. 62

Figure 3.13 Simulation results: (a) for f_1; and (b) for f_2. 67

Figure 3.14 Fault coverages with respect to accuracy of test instrument. 71

Figure 4.1 Computational complexities of IFA process. 75

Figure 4.2 Concept of hierarchical fault modeling. 77

Figure 4.3 Cell library of hierarchical IFA-based fault macromodeling. 78

Figure 4.4 Macro library of hierarchical IFA-based fault macromodeling. .. 79

Figure 4.5 Fault equivalence. 81

Figure 4.6 Macro "current copier": (a) layout; and (b) routing area. 83

Figure 4.7 Fault coverage for routing area: (a) due to etching defect; and (b) due to extra defect. 84

Figure 4.8 Examples for the definition of parameter deviation bounds: (a) in 1-dimension; and (b) & (c) in 2-dimension. 89

Figure 4.9 Current comparators: (a) in [52]; (b) in [60]; and (c) proposed design. 92

Figure 4.10 Current comparator: (a) schematic diagram; (b) switching sequence; (c) small signal equivalent circuit when S_1 is off; and (d) & (e) offset-compensated amplifier. 95

Figure 4.11 Proposed current comparator: (a) parameter values of Figure 4.10(a); (b) parameter values for Figure 4.10(e); and (c) physical

layout. 99

Figure 4.12 Transient responses: (a) during the compensation process; and (b) during the comparison process. 100

Figure 4.13 Simulation results: (a) I_x-V_y characteristic curve; (b) harmonic distortion; and (c) nonlinearity element $V_{nl}(I_x)$ vs I_x & V_y. 101

Figure 4.14 Performance analysis: (a) Gaussian distribution of V_y; (b) statistical confidence vs. window threshold voltage; and (c) statistical confidence vs. resolution. 106

Figure 4.15 ADC with built-in tester: (a) ADC; (b) with built-in tester; and (c) window comparator. 109

Figure 5.1 Structure of PETOMIC. 112

Figure 5.2 The use of defect generator in cell library establishing. 113

Figure 5.3 Example of extraction file and K. 115

Figure 5.4 Experiments for extract parameters from cell K, Opamp in this example. 116

Figure 5.5 Example of prem.cir. 117

Figure 5.6 The use of fault behavior evaluator and fault type classification environment in cell library establishing. 120

Figure 5.7 Example of cell library. 121

Figure 5.8 Fault behavior display window. 126

Figure 5.9 Summary of files used or generated in CLG_routine. 127

Figure 5.10 Example of macro.cir. 129

Figure 5.11 Example of macro library. 131

Chapter 1

INTRODUCTION

More and more mixed-signal devices are being designed recently for the applications of multimedia, wireless communication, and portable data systems. The analog circuit technology conventionally employed for such applications has been gradually switched to analog/digital mixed-signal circuit technology. Figure 1.1 shows a typical digital signal processing (DSP)-based mixed-signal integrated circuit (IC). The digital area typically takes more than 60% of the total IC area [1]. The main analog and mixed-signal components tend to be analog-to-digital converter (ADC), digital-to-analog converter (DAC), phase-locked-loop (PLL), operational amplifier (OP-amp), and filters. Even though much more complicated digital circuits have been widely used in the DSP-based mixed-signal IC, analog circuits will remain for processing or interfacing analog signals [2]. Integrating both digital and analog on a single chip has improved performance and reduced board size and cost. However, the increasing complexity of mixed-signal circuits drastically reduces the controllability and observability of the circuit on the chip. As a result, testing of such complex circuit becomes very difficult and expensive.

In mixed-signal circuits, the digital and analog components are tested separately. Procedure and equipment for testing stand-alone digital or analog chips have been well-established and implemented. However, manufacturers have found the costs associated

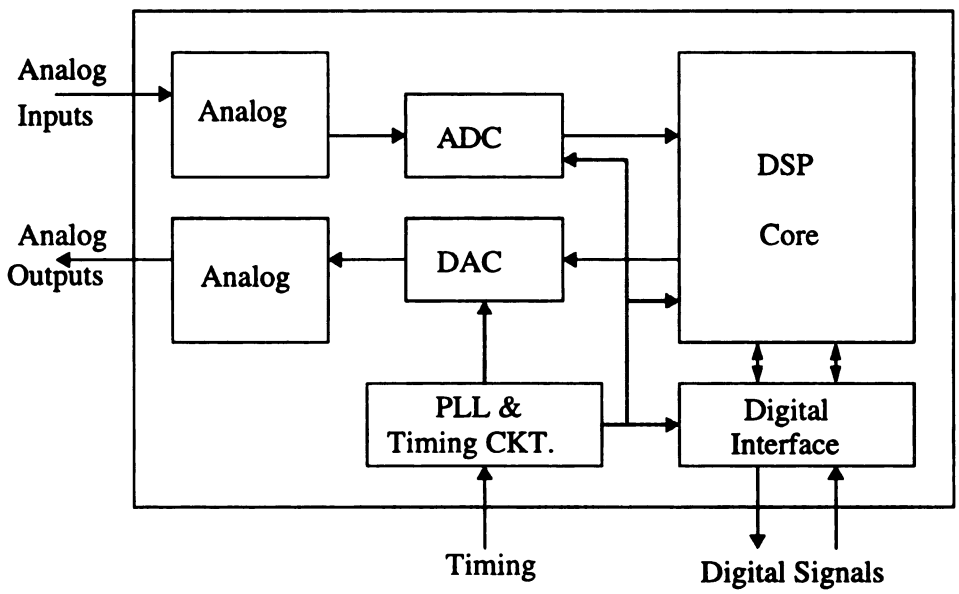


Figure 1.1 Schematic diagram of a typical DSP-based mixed-signal IC.

with high-volume production of mixed-signal ICs are strongly affected by the cost of testing, where the analog circuit testing dominates. Considerable effort has been devoted to identify the causes of the analog test complexity [3]. Unlike digital circuits, analog circuits do not have the binary distinction of pass and fail. The time and voltage continuous nature of their operation make them further susceptible to defects [4-6]. Analog systems are often nonlinear, thus their performance depends heavily on circuit parameters. Process variations within allowable limits can also cause unacceptable performance degradation.

In digital circuits, there exists a wide range of fault models [7]. These models or abstractions form the basis of representing the faulty circuit behavior as well as the test generation. Given a set of test vectors, if the simulated output (signature) of a fault differs from that of the good circuit, then this set of test vectors can detect the fault. This testing process is called *fault-model-based testing* in which the *fault definition* and *test generation* are the major tasks. Thus, simulation before manufacture can be used to determine a set of test vectors for post-manufacture testing. Similar analysis can be done to determine the testability of a design. Figure 1.2 shows an example of the fault-model-based testing process for an AND gate. For a stuck-at one fault (S/1) on input of the AND gate, we can use test input {0,1} to distinguish the faulty circuit under test (CUT) from good one by comparing their outputs.

Analog testing is usually a specification-driven process. It tests a circuit for all specifications both during wafer-probe and final tests. However, given a set of specifications for a circuit, a basic question is [8]: *Are these specifications necessary and sufficient?* In fact, insufficient specifications may result that some faults cannot be detected properly, while unnecessary specifications cause the increase of the complexity of test

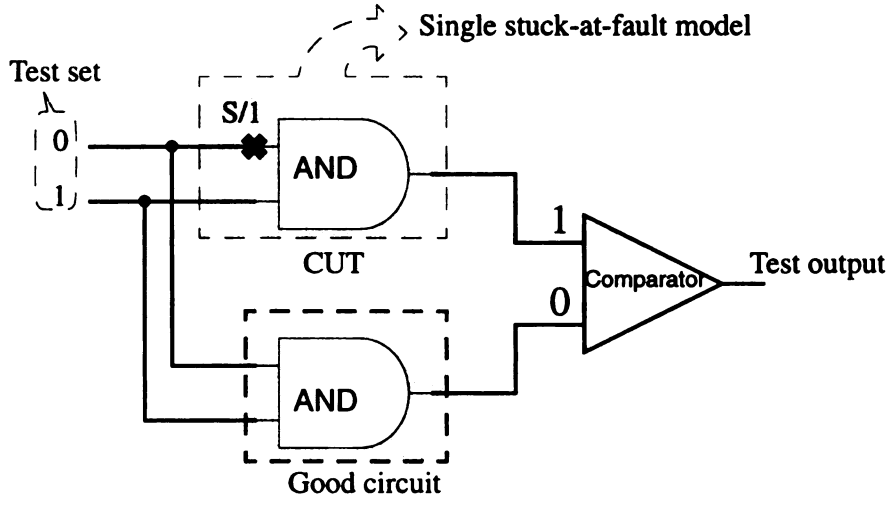


Figure 1.2 Single stuck-at-fault-model-based testing in digital circuit.

generation process. Therefore, analog testing may be simplified if the specification-driven process can be mapped to a fault-model-based process [9]. However, the effectiveness of applying digital fault models on analog circuit is questionable.

The similar stuck-at fault model has been applied for testing analog circuits. In order to enhance the reliability of ADCs for real-time applications, a CMOS switched-current algorithmic ADC which possesses the concurrent error detection (CED) capability was developed in [10-15] to detect transient faults and permanent faults. Based on single stuck-at fault model on the switching elements, the fault behaviors of the A/D converter (ADC) were reported. It was assumed that faulty switched are either permanently stuck-at-ON state (*S/ON*) or stuck-at-OFF state (*S/OFF*). The failure of other components can be modeled as the fault of the associated switch. Thus, the converter can be fully testable. Due to the simplicity of the generated test patterns for the ADC [10-15], a built-in self-test (BIST) design of the ADC is reported in [16] which demonstrates the self-testability with a simple BIST structure. The above studies have shown that the failure of non-switch components can be modeled as the fault of the associated switch. Thus, the converter can be fully testable, but only for stuck-at faults. As it will be discussed later in this thesis study, our simulation results will show that the stuck-at faults in a CMOS switch are about 70% of the total circuit faults. This implies that a 30% of the total faults are not detectable in those studies, and they are referred to as parametric faults. Therefore, to enhance the testability, the first major task is to develop an efficient and effective fault model for analog circuits.

The second major task is to develop test generation and fault coverage evaluation. Most analog circuits are presently designed without considering the testability. More spe-

cifically, a set of nominal parameter values and the associated tolerances are selected to meet a given set of design specifications. Therefore, a designed circuit meets the specifications, if all parameters are selected to be within the tolerances. In many circuit designs, however, a circuit may still meet the specification even if a parameter deviation is far beyond the tolerance. Testability design methodologies have been developed successfully for digital circuits, and its success is attributed to the well-defined fault models and testability design rules. Therefore, based on the fault models defined in the first task, it is necessary to develop certain testability design rules for the designed analog circuits in order to make it easily testable, i.e., the test vectors can be easily generated.

In summary, the goal of this thesis study is to develop an efficient testability design system for analog/mixed-signal circuits so that all designed circuits are easily testable.

1.1 Objectives and Research Tasks

The approaches for developing an efficient testability design system for analog/mixed-signal circuits include: (1) the development of efficient testability design methodologies; and (2) the development of testability enhancement methodologies. Figure 1.3 illustrates a broad view of the thesis study. The testability design system develops an analog circuit in two different cycles. In the design cycle, based on design specification, a set of testability rules is adopted to make the designed circuit easily testable. In the testing cycle, based on the process data and design circuit layout, the fault models of the design circuits are defined using an inductive fault analysis (IFA) technique [17]. Based on the defined fault models, test generation process is invoked to generate a test set and evaluate the fault coverage of the design circuit using the generated test set.

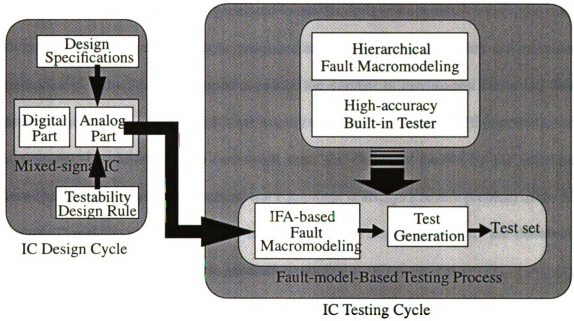


Figure 1.3 Broad view of this thesis study.

The IFA technique has been used to efficiently generate the layout defects and fault types. However, its computational complexity is always a major problem, and it is only applicable to small circuits. For reasonably large analog circuits, a hierarchical fault macromodeling process should be developed so that a large circuit can be hierarchically decomposed into smaller macros or primitive cells which can be handled comfortably by the IFA technique.

As mentioned, analog circuits are designed with a set of testability design rules. The rules ensure that a test set can be generated to test the designed circuit. However, the rules do not guarantee that the test set be generated at low cost. Thus, testability enhancement methodologies should be developed to reduce the number of hard-to-test faults and thus decrease the test generation cost. ICs are usually tested with expensive ATE (automatic test equipment). In addition to the instrument cost, the distortion caused by the interface between internal circuitry and external test equipment is always a severe problem in the IC testing. Therefore, the use of a built-in tester (BITER) not only prevents the distortion problem, but also simplify the test generation process.

In summary, the objectives of the thesis study are to develop efficient testability design methodologies and testability enhancement methodologies for analog/mixed-signal circuits. The major research tasks include the development of: (a) an IFA-based fault macromodeling process; (b) a hierarchical fault macromodeling process; (c) test generation and fault coverage evaluation processes; and (d) built-in testers. The final goal is to develop an efficient and effective testability design system which produces easily testable analog circuits.

1.2 Thesis Organization

The dissertation is organized as follows: Chapter 2 reviews the background required for the thesis study. The IFA technique [17] used for modeling digital circuits is first discussed. Then, the test generation and fault coverage of the switched-current CMOS ADCs [10-15] are briefly described. It will include the salient features of switched-current circuits [18-22,23], the designs and operations of current copiers and CMOS ADCs, the fault behaviors, test generation, and fault coverage evaluation. Finally, some design-for-testability schemes developed for analog/mixed-signal circuits are reviewed.

Chapter 3 presents the developed fault macromodeling process. The process includes two major tasks: Fault-Type definition and Test Generation. Two macro fault macromodeling processes have been developed: heuristic process and IFA-based process. The former process defines the fault types from the circuit layout, technology data, and possible defects, and generates test set based on the fault types. To systematically generate practical fault types, the latter process defines the fault types from the circuit layout, technology data, and the defect distribution from real manufacture process. The fault types are ranked in terms of their occurrences and the higher ranked fault types are used to generate test set. To demonstrate the effectiveness of the developed fault macromodeling process, both current copiers and switched-current ADCs are used as example circuits.

Chapter 4 presents some testability enhancement methodologies. To reduce the computational complexity of the fault macromodeling process with the IFA technique, a hierarchical fault modeling process is developed. A circuit is partitioned as primitive cells and/or macros. The procedures for generating cell library and macro library will be presented. Based on both cell library and macro library, the test set for the target circuit is

generated and the fault coverage of the generated test set is evaluated. To simplify the testability design process, the refinement of the set of testability design rules presented in Chapter 3 will be presented. Finally, a high-accuracy CMOS current comparator is introduced as a built-in tester. The detail design and operation of the tester will be discussed with the simulation results and performance analysis. In addition, this study also addresses the design trade-off between the accuracy of the tester and test sequence length.

Based on the hierarchical fault macromodeling process presented in Chapter 4, Chapter 5 presents a hierarchical testability design system, namely, PETOMIC (Packages for Enhancing Testability Of Mixed-signal Integrated Circuit). The system generates cell library, macro library, test set, and evaluates the fault coverage. The detail system development is discussed with examples of generating a cell library of an Opamp and a macro library of a current copier. The system demonstrates the feasibility of the hierarchical fault macromodeling process.

Finally, Chapter 6 summarizes the thesis study and gives a concluding remark and some future research directions.

Chapter 2

BACKGROUND

Analog circuit testing process can be simple and effective if the specification-driven test process can be mapped to a fault-model-based testing process. Fault definition and test generation are two major tasks in a fault-model-based testing process. Section 2.1 reviews the fault definition and IFA technique. Section 2.2 discusses a test generation process developed in [12,14,15] for switched-current (SI) ADCs. This section briefly describes the importance of SI circuits, the structures and operations of current copiers and an ADC, and the fault behaviors and test generation of an ADC. Finally, some analog/mixed-signal testing schemes are presented in Section 2.3.

2.1 Fault Definition

A number of factors contribute to the failure of a fabricated circuit. Process disturbance, which is essentially random in nature, result in either global or local defects [24-27]. Typically, local defects cause structural deformation at the physical level. The deformations that alter the circuit topology (hard shorts, opens) create *catastrophic faults*, while that do not alter the circuit topology (component deviation) or the DC circuit connection (capacitance bridges) appear as *non-catastrophic faults*. Catastrophic faults result in complete circuit malfunction. Circuit failures are marginal in the presence of non-catastrophic

faults. On the other hand, global defects result in either obvious failures (spotted by virtual inspection) or, subtle parametric faults. The deviation of process parameters beyond tolerable limits results in *parametric faults* which cause marginal failures of some design specifications [24].

Inductive fault analysis (IFA) [17] is a common technique for deriving a graded list of the most likely faults from a description of circuit layout, process parameters, and defect statistics of the fabrication process. The IFA procedure is comprised of three steps, as illustrated in Figure 2.1. The first step includes the defect generation and the defect-to-fault translation. Based on the defect distribution obtained from an actual manufacture process, a defect generator generates a collection of defects, and it injects these defects into the circuit layout. Note that the manufacture process statistics contains the defect density per area and the distribution of defect size. Once the defective layouts are generated, and their associated circuit parameters are extracted by a circuit extractor. This step translates the defects in the layout level to faults in the circuit-level. VLASIC [28] is a software tool commonly used for both defect generation and fault translation for catastrophic faults. The second step defines the macro-level fault behaviors of the faulty circuit parameters. The circuit parameters extracted from the defective layout are simulated by a circuit simulator, SPICE, to generate macro-level fault behaviors such as output impedance, DC bias voltage on macro output or frequency response, etc.

Step 3 groups the fault behaviors into a collection of fault types, where the fault types may be ranked according to the number of their occurrences. This generates a list of fault types.

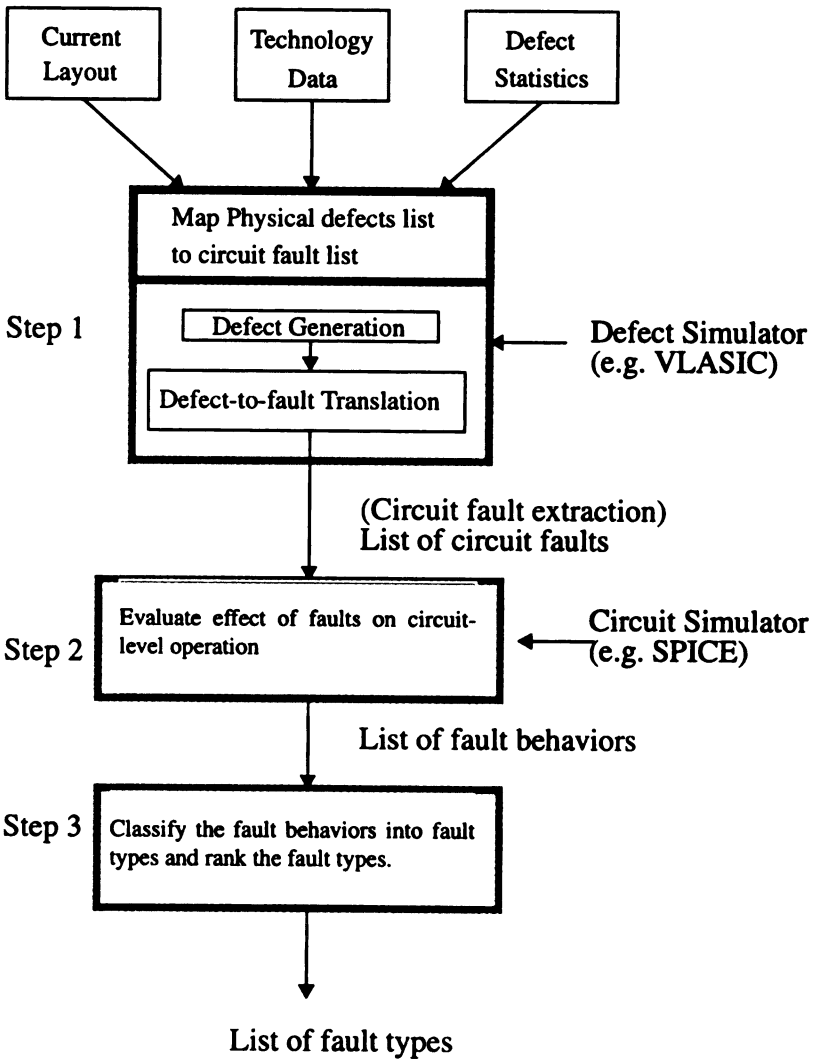


Figure 2.1 Inductive fault analysis.

2.2 Test Generation of Switched-Current Circuits

There exists many kinds of fault models in digital circuits. These fault models form the foundation of representing the faulty circuit behavior as well as the test generation. For given test vectors, if the simulated output (signature) of a faulty circuit is different from that of the good one, these test vectors can detect the fault. Thus, simulation before manufacture can be used to determine a set of test vectors for post-manufacture testing. In this section, a switched-current ADC is used as an example to demonstrate the test generation process.

2.2.1 Switched-Current Circuits

Low-voltage/low-power circuit design is strongly needed for both analog and digital circuit in portable data systems to increase operation time and to decrease the number of batteries and the weight, volume, and operating temperature of the equipment. With the trend that analog-digital interfaces are incorporated as a cell in complex mixed-signal integrated circuits, the use of the same supply-voltage for both analog and digital circuits can give advantages in reducing the overall system cost by eliminating the need of generating multiple supply voltages with dc-dc converters. Therefore, to be compatible with low-voltage systems, analog signal processing components must be able to operate at supply voltage 2-3 V. Reducing power dissipation associated with high-speed sampling and quantization is another important key factor.

Traditionally, the switched-capacitor (SC) technique has been employed extensively in the analog interface portion of mixed-signal designs. However, SC circuits are not fully compatible with digital CMOS processing technology and, as the technology

advances further, the drawbacks of SC technique are becoming more significant. SC techniques traditionally require high quality linear capacitors, which are usually implemented using two layers of polysilicon. The second layer of polysilicon used by SCs is not needed by purely digital circuits and may become unavailable as process dimensions shrink to the deep submicron range. The trend towards submicron processes is also leading to a reduction in supply voltages, directly reducing the maximum voltage swing available to SCs and consequently reducing their maximum achievable dynamic range. With lower supply voltages, the realization of high-speed high-gain operation amplifier becomes more difficult.

Recently, a class of analog circuits wherein current rather than voltage is the primary signal medium has been received considerable attention. The use of current-mode creates a potential for speed improvement because stray-inductance effects in such low-impedance switched-current (SI) circuits are much less severe than those in high-impedance SC circuits. The SI technique couples itself well with the down-scaled CMOS technology, where transistors with a high cut-off frequency are available, meaning a high calibration speed. In addition, highly-linear capacitance is not needed for high accuracy analog signal processing circuits using SI technique. Thus, the same low-cost digital CMOS process for the digital portion of mixed-signal circuits can also be used for the analog portion with SI technique [18-20].

2.2.2 Structures and Operations

Current copier is the basic building block of switched-current circuits. The performance of SI circuits is determined by the current copiers they employ. A copier, as shown

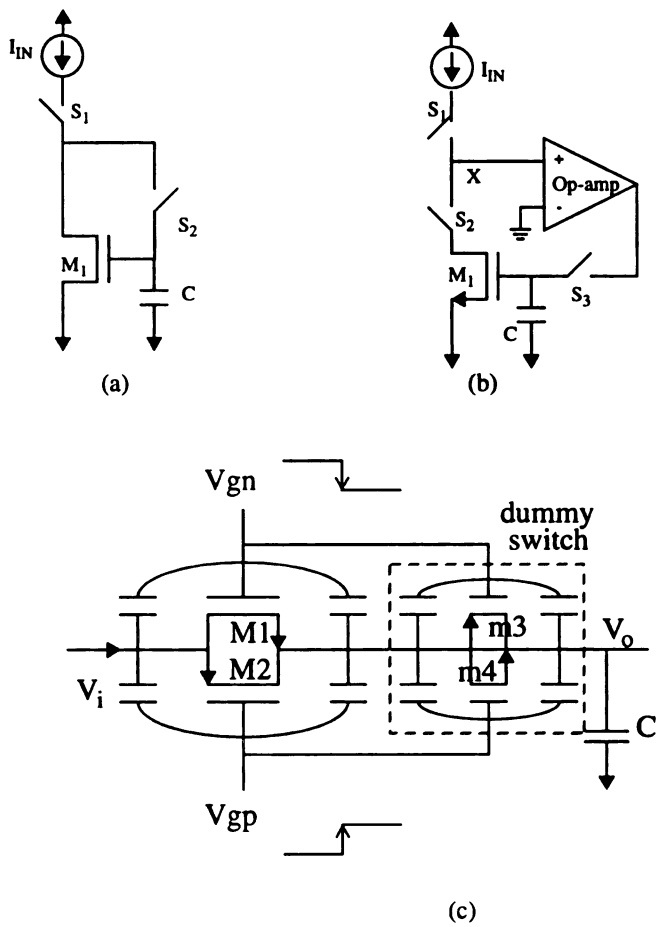
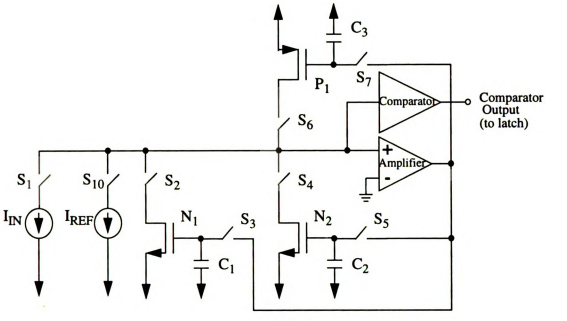


Figure 2.2 Current copier: (a) basic copier; (b) with feedback amplifier; and (c) CMOS switch with a dummy switch.

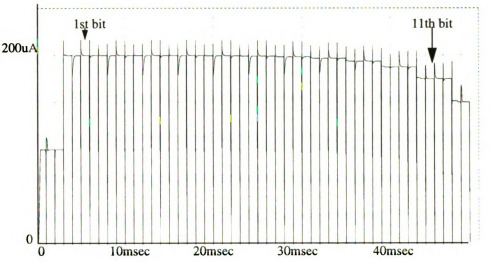
in Figure 2.2(a) [21], is comprised of S_1 and S_2, the current-storage transistor M_1, and the holding capacitor C. To copy the current I_{in}, S_1 and S_2 are turned on for feeding I_{in} to M_1 and C. The capacitor is charged up to whatever gate voltage is needed by M_1 to support a current equal to I_{in}. When S_1 and S_2 are turned off, the copier cell is disconnected from the current source; thereafter the copier cell is capable of sinking a current I_{in} when connected to a load.

Copier suffers from two major error effects: (1) the nonzero conductance of M_1 and (2) charge-injection of S_2 [22]. The non-zero output conductance results from the channel length-modulation effect and the drain-gate capacitive coupling of M_1. The charge-injection error effect is caused as follows: When the gate voltage of S_2 goes down during the turn-off transient, the charge held in the transistor realizing S_2 will be forced to leave. Since one end of S_2 is connected to the gate node of M_1, some charge of S_2 will be dumped to the gate of M_1 and change the voltage across C. As a result, the current held in M_1 will deviate from I_{in}, and charge-injection error results. The error effect due to the nonzero conductance of M_1 can be alleviated by using a negative feedback structure, as shown in Figure 2.2(b), where an amplifier is inserted between the drain and the gate of M_1. On the other hand, the charge-injection error effect can be reduced by either increasing the capacitance C, or the use of CMOS switch with a dummy switch, as shown in Figure 2.2(c) [29-30].

Figure 2.3 illustrates an SI algorithmic ADC that combines current mode and dynamic techniques [23]. This converter does not rely on high gain amplifiers or well-matched components to achieve high resolution and it's inherently insensitive to the amplifier's offset voltage. This converter is comprised of two NMOS current copiers, one



(a)



(b)

Figure 2.3 An SI algorithmic ADC: (a) schematic diagram; and (b) simulation results.

PMOS copier, an op-amp, and a current comparator. The conversion starts sampling the input current and holding it in P_1 by turning on S_1, S_6, and S_7, and converting for the most significant bit (MSB) of an input current I_{IN} by first switching on S_6, S_2, and S_3 to cause the current in N_1 to be set to I_{IN}. Once the current in N_1 is held, S_2 and S_3 are switched off while S_4 and S_5 are on to copy I_{IN} to N_2. The currents stored in N_1 and N_2, twice the input signal, are then loaded into P_1 by turning off S_1 and S_5 while switching on S_2, S_6, and S_7. After P_1 is set, S_2, S_4, and S_7 are turned off, and S_{10} is turned on, it allows the comparator to sense the current imbalance, and determines if the signal, $2I_{IN}$, is greater than I_{ref}. If the signal exceeds the reference, the MSB will be a "1" otherwise it will be a "0". This completes the conversion for the MSB.

The remaining (N-1) bits are then converted in the same manner. The signal held in P_1 is loaded to N_1 by turning on S_6, S_2, and S_3. If the preceding bit was a "1", S_{10} is also turned on to subtract the reference from the signal in P_1. On the other hand, if it was a "0", S_{10} is off so that the signal remains unchanged. Once N_1 is set, N_2 is set by the same procedure. The signal is then doubled and stored in P_1. Finally, it is compared with the reference. The sequence is repeated until the desired resolution is achieved: and the end of conversion pulse is then generated to signal the end of conversion. The converter needs 4N clock cycles for and N-bit conversion [29,31].

The circuit has been implemented and simulated using *MOSIS* 2μm CMOS process parameters, where supply voltages ±2.5V are used [29]. Figure 2.3(b) shows the *pspice* simulation results for the currents held in the PMOS copier at each conversion cycle, where an input currents I_{IN}=100μA is applied. The results show that the converter

achieves a 11-bit resolution. The results also show that the sampling rate and resolution can be improved. However, the performance improvement is not of primary concern in this study. The circuit is implemented to demonstrate and endorse the correctness of our fault simulations.

2.2.3 Fault Behaviors and Test Generation of an ADC

Although mismatched components are allowed in the ADC of Figure 2.3(a), the converter is still susceptible to faulty switching elements. Any faulty switching element may result in an incorrect converted data. Based on the single stuck-at fault model commonly employed for digital test generation, the implementation [12,14,15] assumes that only one faulty switch occurs at a time and the faulty switch is permanently stuck-at ON state (*S/ON*) or OFF state (*S/OFF*). That study generates test signals to completely test the ADC.

The analysis of the faulty switches in the ADC revealed that, due to the fault equivalence, the fault behaviors can be classified into three types: *Type 1 fault* behavior occurs when the faulty switch results in the same conversion output regardless of the values of the input current. Switches S_1, S_2, S_4, S_7, and S_{10} being *S/ON* and S_1, S_2, S_4, S_6, and S_{10} being *S/OFF* illustrate this fault behavior: *Type 2 fault* occurs when the faulty switch renders the conversion output dependent on the initial condition of the active capacitors. Switches S_3, S_5, and S_7 lead to this condition when *S/OFF*: and *Type 3 faults* makes the result of the conversion process dependent on the CMOS structure P_1/N_1 (or P_1/N_2) when S_3 (or S_5) is being *S/ON*. Throughout the next analysis, I_{P1} (I_{N1}, or I_{N2}) will denote the current held in P_1 (N_1, or N_2).

Table 2.1 Fault types and expected outputs.

Fault Types	Input Current To Be Converted	Expected Output Bit Pattern
Type 1A	xx...xx	00.....00
Type 1B	xx...xx	11.....11
Type 2	00...00	0..01x..x
	11...11	1..10x..x
Type 3	xx...xx	1xx.....x x..x1x..x x.....x1

More specifically, consider the case when S_1 or S_6 is *S/OFF*, the input current will not be copied into P_1; this is effectively equivalent to an input current of zero. S_{10} being *S/OFF* leads to the current in P_1 being compared to zero instead of I_{ref}. Hence conversion results in a string of ones. For simplicity of this discussion, Type 1 faulty elements are distinguished as *Type 1A* if they result in a string of zeros, and as *Type 1B* if they produce a string of ones. The detailed fault behaviors for various fault types can be found in [12,14,15].

Table 2.1 summarizes the expected output bit string for each type of faults. A string of zeros is expected in the presence of a Type 1A fault for applying any input current to the converter. Similarly, a string of ones is expected for Type 1B fault. Thus, two test currents, I_{T1}=0 and I_{T2}=I_{ref}, can detect both types of faults. More specifically, a bit string of zeros is expected when the test current I_{T1}=0 is applied to a fault-free converter. Thus, the test current I_{T1}=0 detects Type 1B faults. Similarly, the expected bit string of ones for I_{T2}=I_{ref} detects Type 1A faults. For Type2 faults, the application of I_{IN}=0 results in a bit-string pattern of 0..01x..x. This implies that the expected bit string of zeros for the test pattern I_{T1}=0 detects the faults. On the other hand, a bit pattern of 1..10x..x is produced when I_{IN}=I_{ref} is applied. Thus, the expected bit string of ones for the test current I_{T2}=I_{ref}, detects such faults. Finally, in the presence of a Type 3 fault, a bit string containing at least a 1 is generated and the fault can be detected by the test current I_{T1}=0. This concludes that both test currents, I_{T1}=0 and I_{T2}=I_{ref}, detect all single stuck-at faults at the switching elements of the ADC. If fault coverage is defined as the ratio of the number of faults can be detected over the total number of faults in that circuit, then the converter is

fi

2.

te

cir

co

and

2.3.

sign

digit

incre

regis

2.4(a

test d

two a

free. T

(ASRs

data, a

realize

circuit i

fully testable with respect to single switching element faults using these two test currents.

2.3 Analog/Mixed-Signal Testing Schemes

Design for testability (DFT) techniques and methodologies as well as *built-in self-test* (BIST) structures have been successfully developed and implemented for digital circuits [32,7], they are recently extended to mixed-signal circuits to increase both controllability and observability. This section reviews the development of DFT techniques and BIST structure.

2.3.1 Design-for-Testability Techniques

Conceptually, testability can be considered as the ability to control and observe signals at the circuit (internal) nodes. Given the complex chip in Figure 1.1, analog and digital blocks are generally tested separately. Each block is isolated with a scan path to increase both controllability and observability [33,34]. A scan chain using digital shift registers is added to the interface between the ADC/DAC and DSP core, as shown in Figure 2.4(a), where each register is connected to a node to be accessed. The scan chain allows the test data to be simultaneously loaded to the register and sequentially shifted out, where only two additional pins required for scan-in and scan-out to ensure the scan chain to be fault-free. The same scan design concept can be extended for analog block. Analog shift registers (ASRs), realized by sample/hold (S/H) circuits, can be used to load and shift out the test data, as shown in Figure 2.4(b) [35]. A switched-capacitor (SC) S/H circuit was used to realize the shift register for voltage test data measurement, while current copier, as S/H circuit in switched-current (SI) technique, implements for current test data measurement

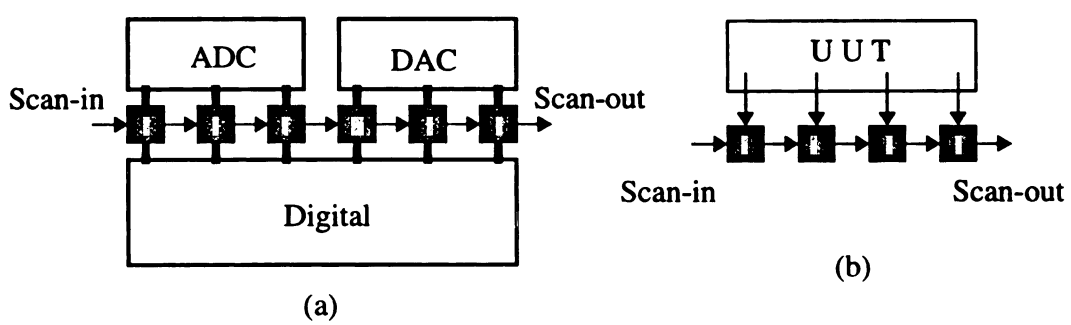
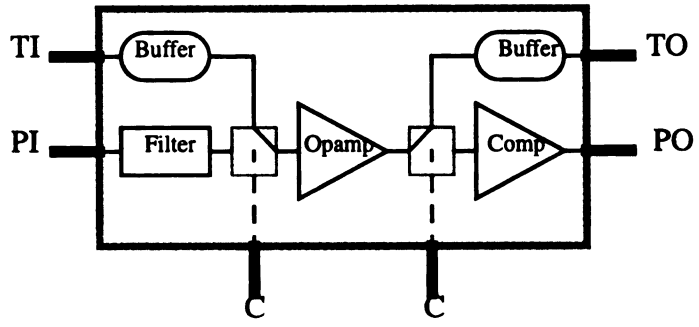


Figure 2.4 DSP-based IC with scan structures.

[36,37]. For voltage test data measurement, each unit (corresponding to a test point) of the scan structure requires a test-point buffer and an ASR. The test-point buffer is used to isolate the test circuit from the UUT (Unit Under Test) so that it will not affect the voltage level at the test point during the sampling period. The buffer is implemented by a voltage follower that has a very high input impedance and a very low output impedance. The scan structure allows parallel of loading the test data and serially shifting them to the output buffer for circuit testing and fault diagnosis. The scan chain also ensures the testability of the analog shift register, i.e., the scan structure is self-testable. Results show that high-accuracy, high-linearity, and high-speed performance can be achieved by the analog shift registers. Connecting all shift registers as scan chain works perfectly in digital circuits, however, the offset voltage in each analog SC S/H circuit may be accumulated to a huge error. This has motived the development of an alternative structure using analog multiplexers [36] which alleviate the error effects. The design concept of combining analog multiplexing and demultiplexing to analog inputs and outputs has been extended to develop analog test bus, as shown in Figure 2.5 [38]. It has also further extended as the IEEE 1149.4 standard for boundary scan design. Scan structures are well-suited for those designs which have insufficient probing pads, and have been applied to board- and system-level design to offset the hardware overhead. However, it may be applied in circuit-level design if the hardware overhead can be reduced.

In addition to *controllability* and *observability, fault coverage* is also a very important testability measure in digital testing. Fault coverage is a measure of completeness in testing. Instead of number of faults detected, the term *fault coverage* in analog testing should be: *how many parameters should be tested* to ensure adequate performance in the intended



PI: Primary Input
PO: Primary Output
TI: Test Input
TO: Test Output

Figure 2.5 Test bus.

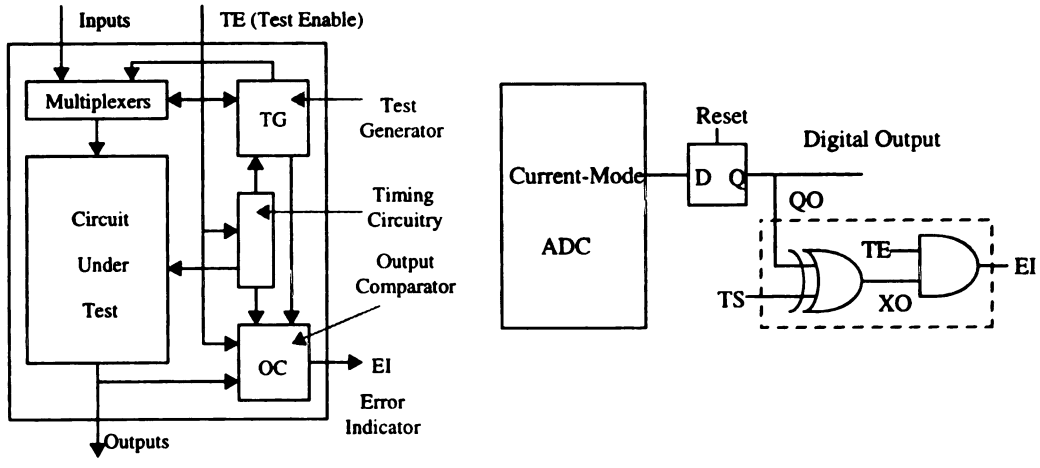


Figure 2.6 BIST design of an ADC.

application. The concern is *which parameters to test*. Analog circuits have many parameters to be tested, but only some parameters, referred to as *critical parameters*, may significantly affect the circuit behavior. The error effect due to the variations of such parameters may cause a system failure. Thus, it is desirable to investigate the relationship between parameter variation and system failure, and to further identify the critical parameters. The set of critical parameters should be minimal in order to simplify the testing/diagnosis process.

2.3.2 BIST Designs

Since most analog components in mixed-signal circuits are used for processing and interfacing analog signals, pin overhead becomes an important issue. A number of analog BIST structures have been presented [39-49,31] to enhance the testability and fault diagnosability of analog circuits. The major design issues include the hardware and pin overhead, self-testable capability of the added hardware, and performance degradation. A BIST structure of a digital circuit, as shown in Figure 2.6 [31], is comprised of five major parts: *Test Generator* (TG), *Input multiplexers* (INMUX), *UUT*, *Output Comparator*, and *Timing Circuitry*. The INMUX selects the input signals either from the normal input signals during the operation mode, or from the test signal generated from TG during the test mode. The timing circuitry is used to synchronize the entire operation. Two extra pins, *test enable* (TE) and *error indicator* (EI), are needed.

In [31], the single stuck-at fault model was assumed. A fault which occurs at any components in the BIST structure causes an error and will be indicated by EI. By faults, we mean the stuck-at ON/OFF faults at all switching elements in the converter circuit and the

stuck-at 0/1 faults at the D-input and Q-output (denotes as QO) of the flip-flop, TS, XO, TE, and EI. The self-testing process starts with checking the latter faults, and then testing the former faults in the converter circuit.

Checking the latter faults is conducted by turning on the power and resetting the flip-flop to a 0. The test enable signal TE is changed from a 0 to a 1, and it is expected that, for a fault-free *AND* gate, the signal EI is also changed from a 0 to a 1, where the signal TS is set to a 1. Consequently, an unchanged signal EI=1 implies that a stuck-at-1 (s-a-1) fault occurs at EI or TE. On the other hand, an unchanged signal EI=0 indicates the occurrence of either a s-a-0 fault at TE, EI, TS, or XO, or a s-a-1 at QO. Note that the s-a-1 fault at QO also implies that the flip-flop fails to perform the reset function. After passing the above test, the signal TS is set to a 0 and the signal TE remains as a 1, hence, the signal EI is expected to be a 0. Therefore, an unexpected EI=1 implies that a s-a-1 fault occurs at TS, QO, EI, or XO. Therefore, with these two tests, the only undetected stuck-at 0/1 faults include the s-a-0 fault at QO and the s-a-0/1 fault at the D-input of the flip-flop which will be tested later.

By Table 2.1, a converted bit string of zeros is the result of *Type 1A faults* and a string of ones for *Type 1B faults*; a bit string of 0...01x...x for Type 2 faults with the application of I_{IN}=0 and a string of 1...10x...x for *Type 2 faults* with the application of I_{IN}=I_{ref}; and a bit string having at least one 1 for *Type 3 faults*. Therefore, to test the converter circuit, we first apply the zero test current, where TS is set to a 0, the flip-flop is reset, and TE remains as a 1 for the test mode. In this test, the signals EI=0 and XO=1 are expected for a fault-free circuit. An unexpected EI=1 implies the occurrence of a *Type 1B, Type 2, or Type 3 fault*, or a s-a-1 fault at the D-input of the flip-flop. After passing the test,

the test current I_{ref} is applied, where TS is set to a 1, the flip-flop is reset, and TE=1. This test is also expected to produce EI=0. An unexpected EI=1 implies the occurrence of either a *Type 1A fault*, or a s-a-0 fault at QO or D-input of the flip-flop.

This concludes that the BIST structure is fully testable for all single stuck-at non-redundant faults [31].

Chapter 3

FAULT MACROMODELING

This chapter presents two fault macromodeling processes that map the specification-driven analog testing process to a simple fault-model-based process: *Heuristic* [29,30,50] and *IFA-based* [51]. The former process defines the fault types from the circuit layout, technology data, and possible defects, and generates test set based on the fault types. To systematically generate practical fault types, the latter process defines the fault types from the circuit layout, technology data, and the defect distribution from real manufacture process. The fault types are ranked in terms of their occurrences and the higher ranked fault types are used to generate test set.

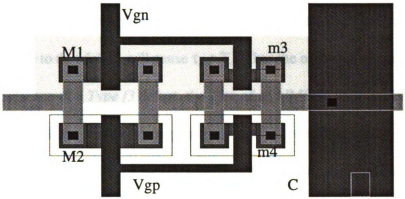
Switches are commonly used in both SI and SC circuits. According to the functionality, two types of switches, *voltage switch* and *current switch*, can be identified. Section 3.1 describes some defects and circuit faults of both switches and illustrates their fault behaviors and fault models. Based on the circuit faults, Section 3.2 presents the heuristic fault macromodeling process. Two example circuits, current copier and ADC, are used to demonstrate the process. Section 3.3 introduces the developed IFA-based fault macromodeling process. Finally, summary and concluding remark for the fault macromodeling is discussed in Section 3.4.

3.1 Fault Types in Switches

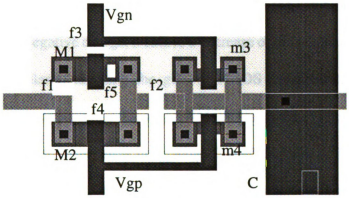
Current switches have been commonly used in SI circuits, while Voltage switches are used in both SC and SI circuits. As their names imply, the current switch passes current signal, while the voltage switch passes voltage signal. For example, as shown in Figure 2.2(b), S_2 is used to pass the currents held in copiers, S_1 used to pass I_{IN}. Thus, they are all implemented by current switches. On the other hand, S_3, used in copier for calibration, is implemented with voltage switches.

Figure 3.1(a) shows the physical layout of the switch in Figure 2.2(c), where the *MOSIS* 2μm CMOS technology, a two-metal, single polysilicon, and n-well, was assumed. Figure 3.1(b) gives five examples of process defects which are significant and cause the circuit to be malfunction. The faults due to these defects are summarized in Figure 3.1(c). In addition, other process defects may also cause faults, such as variations of channel size, errors in doping concentration, errors in the thickness of the gate oxide, etc.

Consider a voltage switch. Let T_{clk} be the clock pulse width applied to the switch. When a fault-free switch is on, the time constant $\tau_{on}=R_{on}C$ should be smaller than T_{clk} for sampling the input voltage signal. On the other hand, when the switch is off, the maximum leakage current I_{leak} should be tolerable, i.e., $I_{leak} < I_{tol}$. The on-resistances of both PMOS and NMOS transistors in the switch should be connected in parallel when the switch is on. As shown in Figure 3.1(c), the presence of the *Type f1* defect causes a floating drain/source in PMOS/NMOS transistors. This results in an increase of on-resistance, while the off-resistance remains the same. Therefore, the increase of on-resistance due to this defect will cause $\tau_{on}>T_{clk}$. This implies that the capacitor C samples and holds a unsettled, incorrect input voltage when the switch is on. Note that the fault does not affect the switch when it



(a)



(b)

Defect	Circuit fault	defect type
Break of metal	a floating drain/source	*Type f1*
	disconnects the switch's input/output	*Type f2*
Break of gate polysilicon	a floating gate may trap some amount of charges on the gate	*Type f3*
	isolates the gate of PMOS transistor	*f3-P*
	isolates the gate of NMOS transistor	*f3-N*
	shortens the channel width.	*Type f4*
Defects in active region	increases the channel impedance	*Type f5*

(c)

Figure 3.1 Defects: (a) switch layout; (b) defected layout; and (c) summary of defects and circuit fault.

is off. A *Type f2* defect is equivalent to a *S/OFF* fault in the switch, in which both the on- and off-resistances are sufficiently large. In other words, when the switch is on, the increase of on-resistance due to this defect will cause $\tau_{on}>T_{clk}$, but the off-resistance is not affected.

In the presence of a *Type f3* defect, the gate of an NMOS transistor is isolated and traps some charges, either positive or negative charges. Three cases can be identified for trapping a positive charge: (1) for larger positive charges, it causes a decrease of off-resistance, but the on-resistance remains the same; (2) for large negative charges, it causes an increase of on-resistance, but the off-resistance remains the same; and (3) for a small amount of positive or negative charge, it causes a decrease of off-resistance and an increase of on-resistance. Similarly, isolating the gate of PMOS transistor has the same fault behaviors but exactly opposite to those of NMOS transistors. The first case causes $I_{leak}>I_{tol}$, while the second case results in $\tau_{on}>T_{clk}$. Case 3 includes both defect effects and causes a larger time constant τ_{on} and an intolerable leakage current. *Types f4* and *f5* defects cause an increase of on-resistance. Based on the fault behaviors of the defects, the following three fault types are concluded,

Type VS1 fault: causes an intolerable time constant τ_{on} and a tolerable leakage current;

Type VS2 fault: causes a tolerable time constant τ_{on} and an intolerable leakage current; and

Type VS3 fault: causes an intolerable time constant τ_{on} and an intolerable leakage current;

Note that the charge-injection error occurs at the moment when switch is turned off. Since the charge held by the capacitor changes when switch state is changed, an additional fault type should be included.

Type VS4 fault: cause excess charge flows out of switch at the moment when switch is turned off.

Consider the fault models of a current switch. Let V_{max} be the maximum voltage across the switch. In general, $V_{max}=V_{DD}$ (power supply voltage). For a fault-free current switch, its on-resistance R_{on} must be sufficiently small so that the maximum switch current ($=V_{max}/R_{on}$) is larger than the maximum input current, $I_{IN(max)}$, and its off-resistance R_{off} has to be sufficiently large so that the maximum leakage current I_{leak} ($=V_{max}/R_{off}$) is smaller than a tolerance, I_{tol}. Therefore, an increase of on-resistance, i.e., $V_{max}/R_{on} < I_{IN(max)}$, results in an error current, $\Delta I=I_{IN}-V_{max}/R_{on}$ when $I_{IN}>(V_{max}/R_{on})$ is applied. On the other hand, a decrease of the off-resistance causes the maximum leakage current V_{max}/R_{off} to be greater than the predetermined current tolerance I_{tol}. Let V_{tol} be the equivalent voltage across the switch, where $V_{tol}=I_{tol}R_{off}$. Therefore, it produces an intolerable leakage current, V/R_{off}, where $V_{tol} < V < V_{max}$. Three fault types can be concluded in a current switch as follows,

Type CS1 fault: causes an error current when switch is on, and a tolerable leakage current when switch is off;

Type CS2 fault: causes an intolerable leakage current when switch is off

and no error current when switch is on; and

Type CS3 fault: causes an error current when switch is on and an intolerable leakage current when switch is off.

The deviation of an output current in a current switch is caused only by the channel resistance, but not influenced by the charge-injection errors. Thus, the charge-injection should not be considered in the fault model for the current switch.

This study shows that a fault-free switch macro may be used as either a current switch or a voltage switch. However, the number of fault types in a current switch is less than those in a voltage switch. In other words, the fault model of current switch is simpler than that of voltage switch. This concludes that a fault-free macro may be used for different applications, but the fault models of the same macro may be different depending upon the applications. Those fault types causing only minor or no effects should be excluded in order to simplify fault simulation and test generation.

3.2 Heuristic Fault Macromodeling Process

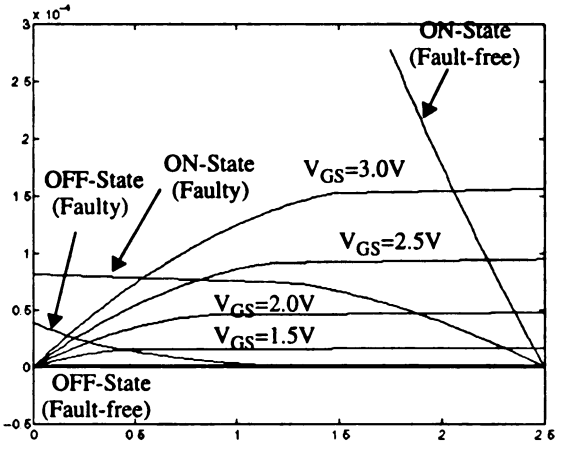
The heuristic fault macromodeling process defines the fault types based on circuit layout, technology data, and some possible defects on the circuit layout. Based on the defined fault types, a test set is generated. For simplicity of discussion, two example circuits, current copiers and ADC, are used to demonstrate the process.

3.2.1 Example Circuit - Current Copier

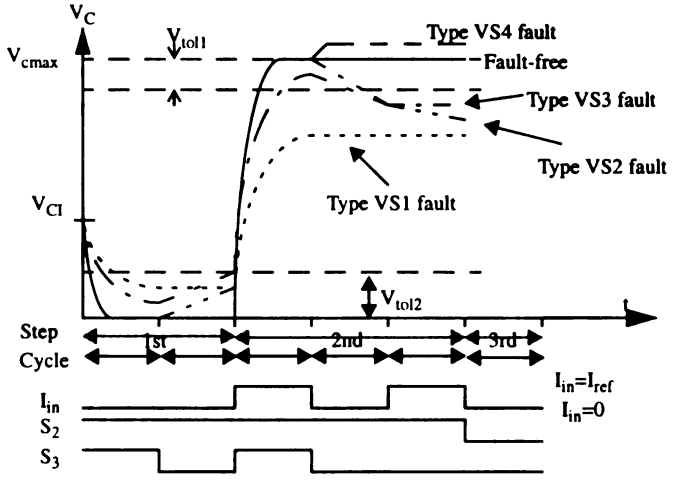
A current copier, as shown in 2.2(c), is comprised of switches and other components. The faults on current-storage transistors and holding capacitors can be modeled as the equivalent faults of the associated switch(es) [12,14,15]. It is also valid in this study based on the defects shown in Figure 3.1(c). More specifically. the following defects may occur in a current-storage transistor: Breaks on gate polysilicon, i.e., *Type f3 defect*, is equivalent to a *S/OFF* fault on the associated voltage switch, i.e., *Type VS1 fault*; Shorten channel width, i.e., *Type f4 defect*, is equivalent to a *Type CS1 fault*; Break on metal, either drain or source, i.e., *Type f1 defect*, is equivalent to a *S/OFF* fault on the associated current switch, i.e., *Type CS1 fault*; Short between drain and gate implies that a *S/ON* fault on the associated voltage switch, i.e., *Type VS2 fault*; Short between source and gate, or between drain and source, is equivalent to a *S/OFF* fault on the associated voltage switch, i.e., *Type VS1 fault*. Any defects in active region, i.e., *Type f5 defect*, is equivalent to a *Type CS1 fault*. Any process deviation causing an increase of on-resistance implies the presence of a *Type CS1 fault*. The following defects may occur in the holding capacitors: Any defects causing a decrease of capacitance, or an open circuit in the capacitor, is equivalent to a *Type VS4 fault* on the associated voltage switch. Any defects causing an increase of capacitance, or a short circuit in the capacitor is equivalent to a *Type VS1 fault*.

The above equivalent faults include both catastrophic and parametric faults for both current-storage transistors and the holding capacitors in a copier. Based on the fault types for both current switches and voltage switches, the test generation process for the current copier is described as follows.

Figure 3.2(a) plots the I-V characteristics of M_1 and the load S_2 with and without



(a)



(b)

Figure 3.2 (a) Simulation results of I-V plot of M_1 with load lines for S_2; and (b) fault behavior and switching sequence.

faults, where the aspect ratio of M_1 is (W/L)=6μm/4μm. The copier including S_2 and M_1 can be treated as an amplifier with a switch which acts as a voltage control active load. For a fault-free current copier, M_1 can store a current of 100μA when the switch is on and V_{GS}=2.5V. Figure 3.2(b) illustrates the behaviors of faulty and fault-free copiers with the application of the test sequence. The test sequence is comprised of three steps, or six clock cycles, and can detect all types of switch faults, i.e., *Types CS1-CS3* and *VS1-VS4 faults*. It also shows the test currents with the switching sequences for both switches S_2 and S_3 at each clock cycle.

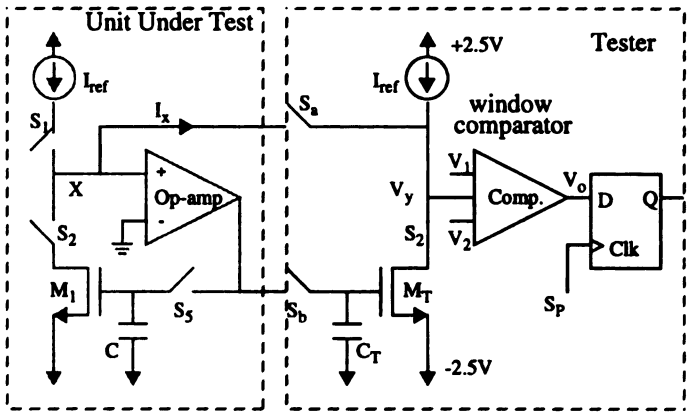
Let V_{CI} be the initial voltage held in the holding capacitor C, and V_{cmax} be the maximum voltage across the capacitor. Taking the process variation into account, let V_{tol1} and V_{tol2} be the allowable voltage deviations for both V_{cmax} and 0, respectively. The corresponding current tolerances are $I_{tol1}=\beta(V_{cmax}-V_{th})*V_{tol1}$ and $I_{tol2}=0.5\beta(V_{tol}-V_{th})^2$, where V_{th} is the threshold voltage of M_1. In the first cycle of Step 1, the input current I_{in}=0 is copied and stored in M_1, where both S_2 and S_3 are on, to discharge the capacitor. Thus, after turning off S_3 in the second cycle of Step 1, the current held in M_1 is compared with an expected zero-current. Step 2 consists of three clock cycles. An input current $I_{in}=I_{ref}$ is applied and copied to M_1 so that the capacitor is charged up to V_{cmax} within the clock cycle T_{clk}. Once the current is copied, both S_2 and S_3 are turned off and the current I_{ref} is held in M_1 even though the test current is changed in these three clock cycles, as shown in Figure 3.2(b). Thus, at the end of Step 2, the current held in M_1 is compared with an expected current I_{ref}. Finally, in the Step 3, when I_{in}=0 and both S_2 and S_3 are off, a zero-current is expected for fault -free circuit.

M_1 is expected to hold a zero-current at the end of the 2nd cycle of Step 1,

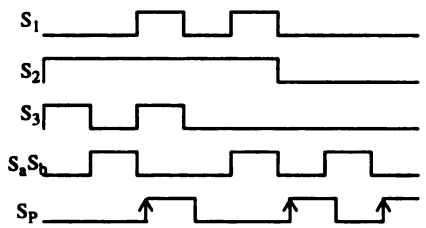
unsuccessful test implies the existence of a *Type VS1, VS2*, or *VS3* fault. More specifically, the presence of a *Type VS1* or *VS3* fault causes an intolerable time constant τ_{on} which may be too short to discharge the capacitor so that the voltage across the capacitor exceeds V_{tol2}. On the other hand, a *Type VS2* or *VS3* fault produces an intolerable leakage current and results in a current held in M_1 to exceed I_{tol2}.

If the copier passes the test in Step 1, the test pattern and clock sequence in Step 2 are applied. At the end of the 3rd cycle in Step 2, for fault-free circuit, the current held in M_1 is expected to be I_{ref}, i.e., the voltage across the capacitor is expected to be between (V_{cmax}-V_{tol1}) and V_{cmax}. Unsuccessful test implies the existence of a *Type VS1-VS4, CS1* or *CS3* fault. More specifically, an intolerable time constant τ_{on} caused by a *Type VS1* or *VS3* fault may be too short to charge up the capacitor and result that the voltage across the capacitor is below (V_{cmax}-V_{tol1}). On the other hand, during the second cycle of Step 2, for fault-free circuit, switches S_2 is on and S_3 is off, the test current is changed from I_{ref} to 0, where the current held in M_1 is still I_{ref}, i.e., the voltage across the capacitor is V_{cmax}. Since the output of the amplifier is zero, the voltage across S_3 is also V_{cmax}. However, when S_3 is off, an intolerable leakage current caused by a *Type VS2* or *VS3* fault will discharge the capacitor so that the voltage across it is below (V_{cmax}-V_{tol1}). Even though the test current is changed back to I_{ref}, the leakage current may continuously discharge the capacitor, as shown in Figure 3.2(b). Since a *Type VS4* fault causes excess charge flows at the moment when S_3 is off, the fault is identified if the voltage across the capacitor exceeds V_{cmax}.

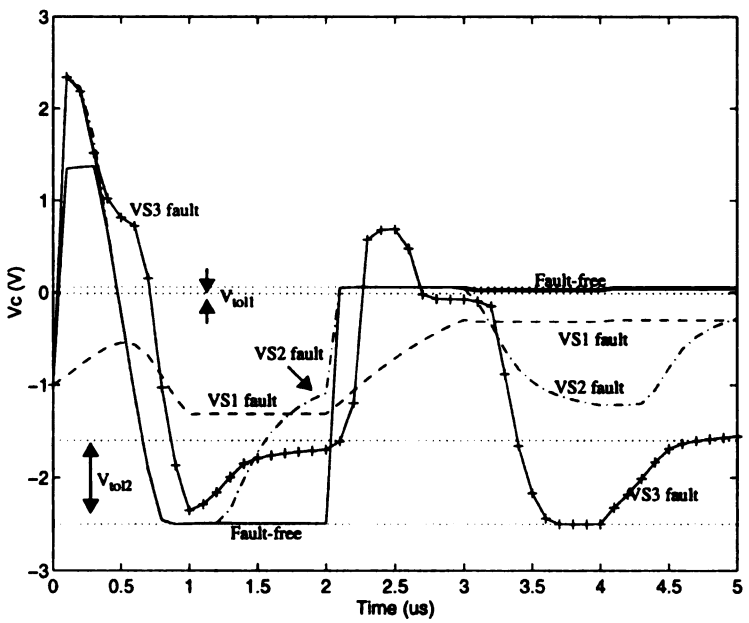
Finally, as illustrated in Figure 3.2(a), a *Type CS1* or *CS3* fault causes the maximum current which can be stored in M_1 being reduced. Hence, when I_{in}=I_{ref} is applied, the fault is identified if the current held in M_1 is less than (I_{ref}-I_{tol1}). Finally, unsuccessful test for



(a)



(b)



(c)

Figure 3.3 Built-in tester: (a) schematic; (b) switching sequence; and (c) fault simulation results.

Step 3 identifies a *Type CS2* or *CS3* fault. Since the fault causes an intolerable leakage current when S_2 is off, the fault is identified if a non-zero leakage current is detected. This concludes that the test sequence in Figure 3.2(b) detects *Type VS1-VS4* and *CS1-CS3* faults.

In the above test process, a tester is needed to compare the current held in M_1 to 0 in Step 1 and I_{ref} in Step 2. The tester, as shown in Figure 3.3(a), is comprised of a current copier, a window comparator, and a D-flip-flop, and its switching sequence is illustrated in Figure 3.3(b). Let I_{M1} denote the current held in M_1. Turning on S_1 and S_2 causes a difference current $I_x=I_{in}-I_{M1}$. Turning on S_a and S_b will copy a current $(I_{ref}+I_x)$ to M_T and virtual ground V_y. A zero current or I_{ref} is applied from the input source through S_1 when I_{M1} is compared to a 0 or a I_{ref}. Applying a zero current is equivalent to turning off S_1. Closing S_a and S_b, then, will lead to a shift of V_y from 0. The voltage V_y is compared with the threshold voltages V_1 and V_2 of the window comparator. The output is defined as: $V_o=0$ if $V_2 < V_y < V_1$, and $V_o=1$ otherwise. Let I_{tol} be the tolerance of $|I_x|$, then the values v, V_{tol1}, and V_{tol2} can be expressed in terms of I_{tol} as follows,

$$v = V_1 = -V_2 = I_{tol} / [I_{ref} * (\lambda_n+\lambda_p)]$$

$$V_y=-I_x / [I_{ref} * (\lambda_n+\lambda_p)]$$

$$V_{tol1} = I_{tol} / \sqrt{2I_{ref}\beta_n}$$

$$V_{tol2} = V_{th} + \sqrt{2I_{tol}/\beta_n}$$

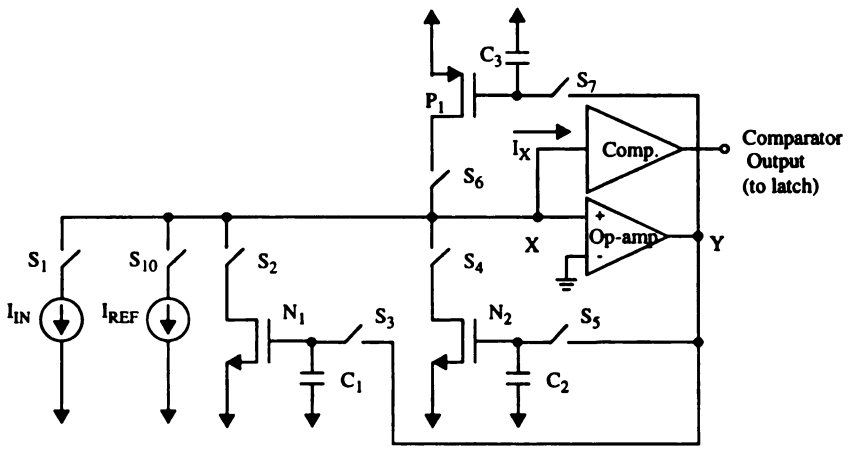
If $I_x=0$, the voltage V_y is equal to 0. On the other hand, if a current equal to or greater than I_{tol}, by the above equations, $|V_y| \geq v$, and thus $V_o=1$. Thus, the digital data Q=0 means the comparison is asserted, and Q=1, otherwise.

Figure 3.3(c) shows the simulation results of the circuit in Figure 3.3(a), where the transistor size is W/L=6μm/4μm for both M_1 and M_T, I_{ref}=100μA, and V_1=-V_2=v=0.1V. The process parameters are λ_n=1.991479e-2, λ_p=4.921086e-2, V_{th}=0.822163, k_p= 4.89376e-5, and β_n=k_p*(6/4)=7.3406e-5. Thus, we obtain I_{tol}=0.69126μA, V_{tol1}=5.7mV, and V_{tol2}=0.9594V. Results show that Step 1 takes 1 cycle to initialize the circuit, 2 cycles to force a zero current to be held in N_1, and 1 cycle to compare the result, Step 2 takes 2 cycles to keep I_{ref} and 1 cycle to compare the result, and Step3 takes 2 cycles. Results conclude that *Type VS1-VS3* faults can be detected in Steps 1 and 2, Step 2 also detects *Type VS4*, *CS1* and *CS3* faults, and Step 3 detects *Type CS2* and *CS3* faults.

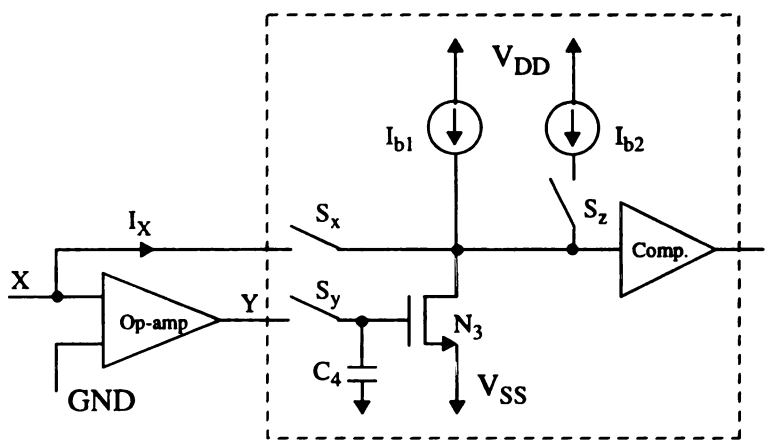
3.2.2 Example Circuit - ADC

In the test generation process for current copier, the emphasis was placed on generating a test sequence that maximizes the error effects caused by failure switch(es). However, for ADC, the emphasis should be on maximizing the accumulated error generated at each conversion step. Based on the accumulated errors, a test sequence is generated to excite the fault and the fault effects are observed from the converted digital data.

Consider the ADC in Figure 3.4(a) [23] with a comparator in Figure 3.4(b). In the comparator, a current copier consisting of N_3, C_4 and switches S_x and S_y, is used as a load to copy the difference current I_x. Since the difference current may be positive or negative, a bias current source I_{b1} is used to keep a positive current to be copied to N_3. A current which is slightly higher than I_{ref} is chosen for I_{b1}. The copier memorizes the current I_x and produces a voltage deviation to compare to a zero-voltage in the comparator. Since the



(a)



(b)

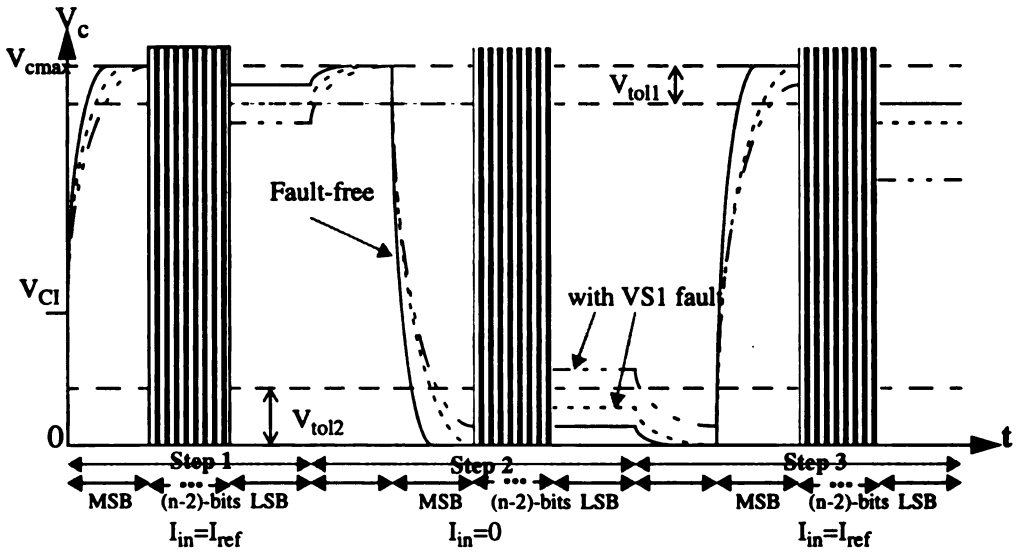
Figure 3.4 Test structure for SI algorithmic ADC: (a) schematic diagram; and (b) comparator.

resolution of an ADC is 0.5LSB, or $0.5I_{ref}$, here a simple comparator instead of window comparator, can be used. It should be noted that an additional bias current $I_{b2}=I_{ref}$ and the switch S_z are used only for testing purpose. During the normal operation, S_z is off and the bias current is isolated from the converter circuit. Thus, the extra circuitry does not affect the performance of the converter. The function of this extra circuitry will be explained shortly. Just like current copier, the current switch and voltage switch are also used in ADC.

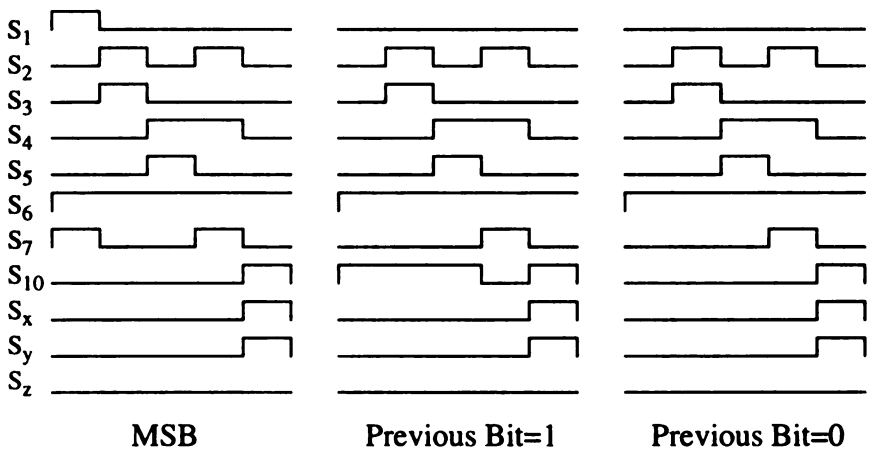
In Figure 3.4, S_1, S_2, S_4, S_6, S_{10}, S_x, and S_z are current switched, while S_3, S_5, S_7, and S_y are voltage switches. The ADC consists of four copiers. One may apply the test sequence developed in the previous section for all copiers in the ADC. However, in the ADC, we can only observe the result from the output of the comparator, i.e., the converted digital data. Thus, the test sequence should be generated to maximize the accumulated errors so that the error effect can be reflected to the converted digital data.

As discussed in Section 3.2.1, the current switch faults, *Type CS1-CS3* faults, can be detected by applying a test current I_{ref}. when $I_{in}=I_{ref}$ is applied, a *Type CS1* or *CS3* fault at S_2 is identified if the current held in N_1 is less than $(I_{ref}-I_{tol1})$. This error will be accumulated so that the converted digital data with the pattern 1...0xx..x, "x" means "don't care", i.e., either 0 or 1, is obtained. On the other hand, with the application of a zero input current, an intolerable leakage current occurs in the presence of a *Type CS2* or *CS3* fault at S_2 when the switch is turned off. The accumulated error will cause the converted digital data pattern to be 0...1xx..x. Thus, both I_{ref} and 0 detects the current switch faults.

Consider a *Type VS1* fault at S_3. Figure 3.5(a) illustrates a test sequence, referred to as *Test Sequence A*, for detecting such fault. When an input current $I_{in}=I_{ref}$ is applied in the first step, the fault causes an intolerable time constant τ_{on} which is too short to charge up



(a)



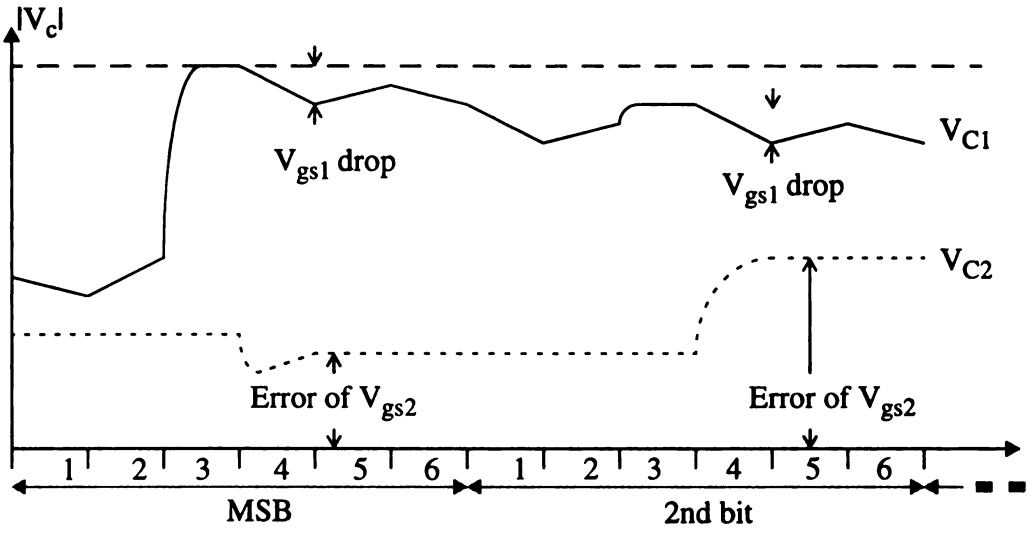
(b)

Figure 3.5 Test sequence A: (a) fault behaviors; and (b) switching sequence.

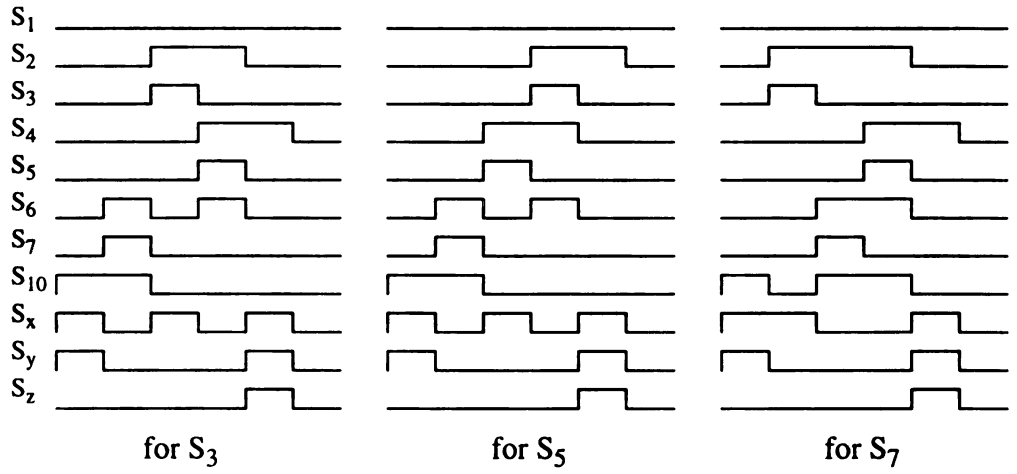
the capacitor C_1 so that the voltage across the capacitor cannot reach (V_{cmax}-V_{tol1}) within the clock period T_{clk}. In other words, the transistor N_1 stores a current less than I_{ref}. As a result, the converted digital data pattern 1...0xx..x identifies such fault. However, this fault may pass this test if the initial voltage held in C_1 is sufficiently high. An input current I_{in}=0 is applied in the second step to ensure that the voltage across the capacitor is below V_{tol2}.

In the first cycle of Step 2, the voltage across the capacitor C_1 is charged up to V_{cmax}. This is simply because the fault may marginally pass the first test, say, $V_{C1} \approx V_{cmax}$-V_{tol1}, and it could discharge C_1 to below V_{tol2} when I_{in}=0 is applied in the next cycle. As a result, the fault may not be able to be identified. After conversion, if the converted digital pattern 0...1xx..x is resulted, this implies that C_1 fails to be discharged to below V_{tol2}, and thus the fault is detected. Finally, if the switch passes the second step, it implies that the initial voltage across the capacitor is below V_{tol2}. Thus, applying an input current $I_{in}=I_{ref}$ in the third step will detect the fault if the pattern 1..0xx..x is resulted. Similarly, the C_1 is discharged to below V_{tol2} in the first cycle of Step 3. The similar process can be applied to test the *Type VS1* fault for S_5 and S_7. *Test Sequence A* can also detect a *Type VS3* fault in these switches. Figure 3.5(b) illustrates the switching sequence of all switches. In fact, the switching sequence is the one for normal conversion process.

Consider a *Type VS2* fault at S_3. The fault causes an intolerable leakage current which changes the current held in N_1, and the voltage across the capacitor. The fault can be detected by the sequence shown in Figure 3.2(b) for the copier. However, it becomes difficult to detect the fault by observing the converted digital data pattern. Figure 3.6(a) illustrates the test sequence, referred to as *Test Sequence B*, for detecting such faults. There are six steps for each bit conversion. Figure 3.6(b) shows the switching sequence. In the



(a)



(b)

Figure 3.6 Test sequence B: (a) fault behavior; and (b) type VS2 fault.

first step, the reference current I_{ref} is copied and stored in N_3, where the current store in N_3 is (I_{b1}-I_{ref}). In Step 2, the reference current is again copied and stored in P_1. Then, the copier with N_1 is calibrated in the third step by turning on S_x, S_2,and S_3, i.e., to copy the current I_{ref} held in N_3 and the bias current source I_{b1} to N_1. This attempts to raise the voltage across the capacitor C_1 to V_{cmax}.

In the next step, the copier with N_2 is calibrated by N_1 and P_1. This means that a zero current is copied and held in N_2. This will cause the output voltage of the amplifier, Node Y in Figure 3.4(b), drops to zero, and thus a maximum voltage across S_3, i.e., V_{cmax}, is resulted. Note that switch S_3 is off in this step. As a result, an intolerable leakage current in S_3 caused by this fault will discharge the capacitor C_1 and change the current held in N_1. In Step 5, switches S_4, S_x, S_y, S_z are turned on to copy and store the current difference between I_{b2}=I_{ref} and the current held in N_2 to the copier with N_3. In Step 6, all switches are turned off and the current held in N_3 is compared and a converted digital data is obtained. For the fault-free circuit, the current held in N_2 is 0 and thus the current held in N_3 with I_{b1} is I_{ref}. A "1" results in the conversion.

As illustrates in Figure 3.5(a), the voltage across C_1 is charged up to V_{cmax} in Step 3, but it drops slightly in Step 4 due to the leakage current caused by this fault. The voltage drop of C_1, decreasing the current held in N_1, will result in an increase of the current held in N_2, and increase the voltage across C_2. If the error in V_{C2} is sufficiently large, then a digital "0" is resulted in the conversion. Since the S_3 is off for 5 clock cycles, the effect due to the leakage current will be getting severe in the presence of such fault. This will cause the error of V_{C2} to be sufficiently large. Thus, repeating the 6-step sequence for converting n-bit, a converted digital pattern 1..0xx.x detects the fault. Similarly, Figure 3.6(b) also

illustrates the switching sequences for detecting the faults in S_5 and S_7. Test Sequence B can also detect a *Type VS3* fault in these switches.

Considers a *Type VS4* fault in S_3. The fault causes excess charge flows at the moment when S_3 is off. The charge can be positive or negative. If it is negative, then the accumulated error will cause V_{c1} to be less than (V_{cmax}-V_{tol1}) when the third step of *Test Sequence A* is applied. Thus, the fault results in a converted digital data with the pattern 1..0xx..x. On the other hand, if the charge is positive, then the accumulated error will cause V_{c1} to be more than V_{tol2} when the test sequence in Step 2 is applied. Thus, the fault results in a pattern of 0..1xx..x. This implies that the test sequence for testing *Type VS1* fault can also detect *Type VS4* faults.

The test sequence for the ADC consists of *Test Sequence A* and *Test Sequence B*, where *Test Sequence A* detects *Types VS1, VS3,* and *VS4* faults for S_3, S_5, and S_7, *Types CS1-CS4* faults for S_1, S_2, S_4, S_6, and S_{10}, and *Types CS2* and *CS3* faults for S_x, and *Test Sequence B* detects T*ypes VS2* and *VS3* faults for S_3, S_6, S_7, *Types CS1* and *CS3* faults for S_x, *Types CS1-CS3* faults for S_z, and *Types VS1-VS4* faults for S_y. This implies that both test sequence will detect all switching faults.

3.2.3 Discussion

This subsection addresses an important issue on simplifying test generation process using a built-in tester. The range of the threshold voltages, ($-V_2$,V_1), in the window comparator limits the current tolerance, I_{tol}, and the voltage tolerances, V_{tol1} and V_{tol2}. A better current comparator is needed if a tighter tolerance is required. However, testing with tighter tolerance may reduce testing time. Moreover, a better comparator is costly.

Therefore, developing high-precision yet low-cost current comparators as built-in testers are of importance for simplifying the test generation process and reducing testing time.

The fault types are defined in a brute-force approach with the possible defects on the circuit layout. In fact, some fault types may occur with a very low possibility. To simplify the fault simulation and test generation processes, only those fault types with higher possibilities are considered. The fault types should be defined based on the defect distribution generated from the manufacturing process and ranked according to their occurrences. This motivated the development of a fault macromodeling process using the IFA technique discussed in the next section.

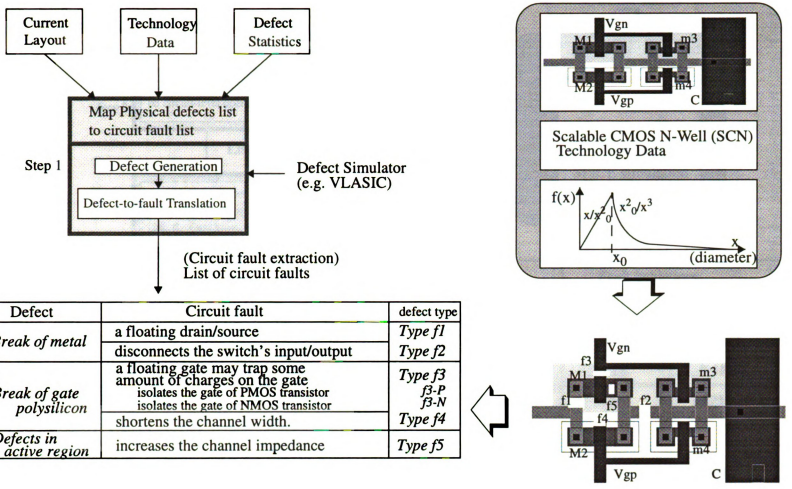
3.3 IFA-Based Fault Macromodeling Process

This section describes two important steps in the IFA-based fault macromodeling process: fault classification and test generation.

3.3.1 Fault Classification

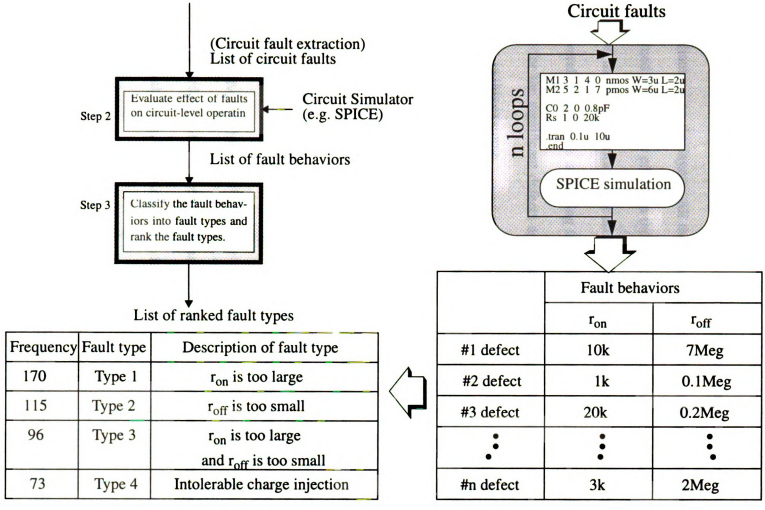
The IFA technique, as illustrated in Figure 3.7, contains three steps, where the voltage switch with dummy circuit is used as example. In the first step, the input data includes layout, technology data, and defect statistics, where the Scalable CMOS N-Well (SCN) technology is employed, and the following density function [17] is used.

$$f(x) = \begin{cases} x/x^2_o, x < x_o \\ x^2_o/x^3, x > x_o \end{cases} \qquad (3.1)$$



Defect	Circuit fault	defect type
Break of metal	a floating drain/source	*Type f1*
	disconnects the switch's input/output	*Type f2*
Break of gate polysilicon	a floating gate may trap some amount of charges on the gate	*Type f3*
	isolates the gate of PMOS transistor	*f3-P*
	isolates the gate of NMOS transistor	*f3-N*
	shortens the channel width.	*Type f4*
Defects in active region	increases the channel impedance	*Type f5*

Figure 3.7 Step 1 of IFA-based fault macromodeling.



Frequency	Fault type	Description of fault type
170	Type 1	r_{on} is too large
115	Type 2	r_{off} is too small
96	Type 3	r_{on} is too large and r_{off} is too small
73	Type 4	Intolerable charge injection

	Fault behaviors	
	r_{on}	r_{off}
#1 defect	10k	7Meg
#2 defect	1k	0.1Meg
#3 defect	20k	0.2Meg
⋮	⋮	⋮
#n defect	3k	2Meg

Figure 3.8 Step 2 & 3 of IFA-based fault macromodeling.

Note that x_0 is the mean of x, and the probability density function, f(x), of the diameter of defect, x. The defect distribution is based on the real process data collected from clean room. Based on this distribution, the defect generator program generates defects with different diameter on the layout. All the defects are passed through a decision process and determined if they have effect on the circuit performance or not. The defects which have effect on the circuit performance are called significant defects and they can be classified into several defect types according to what kind of effect they will cause. All the faulty layouts for the significant defects are then translated into spice program by the Magic extractor, in this example.

Figure 3.8 shows the operation of step 2 and 3 of the process. The *Spice* files are simulated by *Spice*. Therefore, n times simulations are needed if there are n significant defects. The purpose of these simulation is to find the fault behavior values of the circuit parameters in interest for every significant defect. For the voltage switch in this example, the on-resistance r_{on} and off-resistance r_{off} are the two circuit parameters of interest, thus the corresponding values of r_{on} and r_{off} of every significant defect are found and listed in the fault behaviors table.

According to the list of fault behavior values, the significant defects are translated to a list of fault types. In Figure 3.8, the fault types of voltage switch can be concluded as below,

Type 1 fault: On-resistance is too high, off-resistance is unchanged;

Type 2 fault: Off-resistance is too low, on-resistance is unchanged;

Type 3 fault: On-resistance is too high and off-resistance is too low; and

Type 4 fault: Intolerable charge injection error.

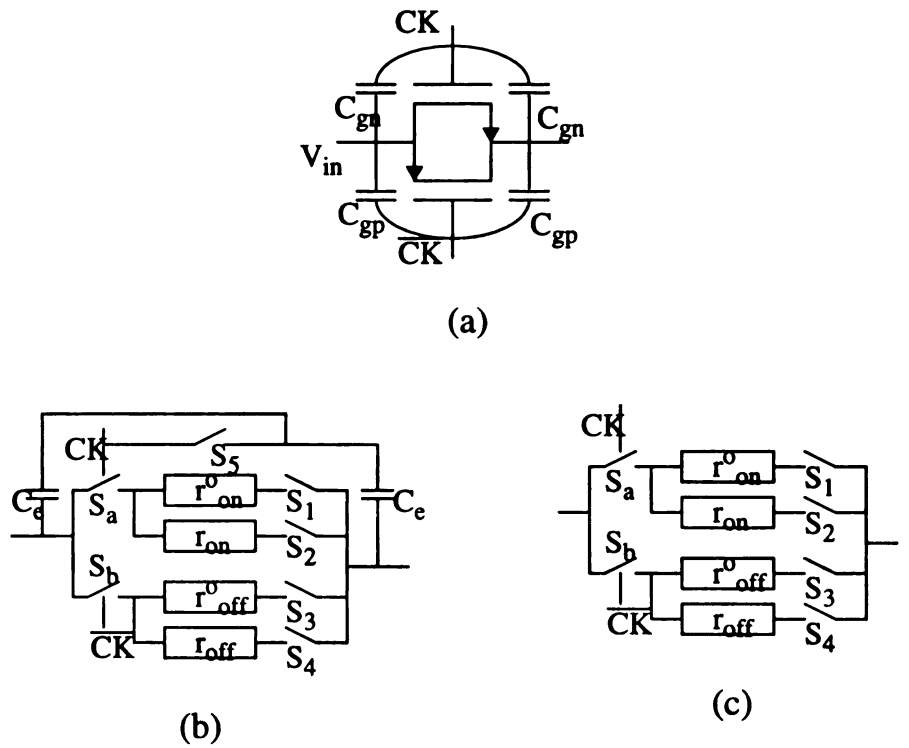


Figure 3.9 Switches: (a) schematic; (b) fault model for voltage switch; and (c) fault model for current switch.

As mentioned previously, a Type 4 fault occurs only in the voltage switches. We may use the same macromodel for both current or voltage switches. However, they should use different fault macromodels for both switches. The fault macromodel of voltage switch includes the above four fault types, while the fault macromodel of current switch excludes the Type 4 fault.

Based on the fault types obtained from IFA, the fault macromodel can be established. Consider a CMOS voltage switch, shown in Figure 3.9(a), where C_{gn} and C_{gp} are the gate capacitance of NMOS and PMOS transistors, respectively. The voltage switch can be modeled as shown in Figure 3.9(b), where r^o_{on} and r^o_{off} are nominal on-resistance and off-resistance, respectively, r_{on} and r_{off} are the on-resistance and off-resistance of a faulty switch, respectively, and C_e is the difference of C_{gn} and C_{gp}. The switches in Figure 3.9(b) are all ideal, where S_a and S_b are controlled by the clock signals CK and $\overline{CK}$, respectively, while S_i, i=1,...,5, are on and off depending upon the fault types. Based on the fault model, the switches S_i's are assigned as follows, where "0" means "off" and "1" is "on".

fault free: $(S_1,S_2,S_3,S_4,S_5)=(1,0,1,0,0)$;

Type 1 fault: $(S_1,S_2,S_3,S_4,S_5)=(0,1,1,0,0)$;

Type 2 fault: $(S_1,S_2,S_3,S_4,S_5)=(1,0,0,1,0)$;

Type 3 fault: $(S_1,S_2,S_3,S_4,S_5)=(0,1,0,1,0)$; and

Type 4 fault: $(S_1,S_2,S_3,S_4,S_5)=(1,0,1,0,1)$;

Similarly, a current switch is modeled as shown in Figure 3.9(c), where both C_e and S_5 are

removed from the voltage switch fault model. The use of ideal switches for fault macro-models makes the fault simulation and test generation easier, and the linear resistors definitely speeds-up the fault simulation, while keeping the accuracy.

3.3.2 Testability Design Rules

Let Δr and Δy be the parameter deviation and performance deviation, respectively, and Δy^{lb} and Δy^{ub} be the lower and upper bounds of a design specification (Figure 3.10). An analog circuit can be easily testable if it is designed in such a way that, for any fault type, there exist the parameter deviation bounds Δr^{lb} and Δr^{ub} such that, for all u,

$$\Delta y^{lb} \le \Delta y \le \Delta y^{ub}, \text{ if and only if } \Delta r^{lb} \le \Delta r \le \Delta r^{ub}, \text{ for all } \Delta r. \qquad (3.2)$$

In other words, for each fault type, there exist a pair of Δr^{lb} and Δr^{ub} such that the circuit meets the design specification if and only if the parameter deviations are within the bounds for all u. In fact, the parameter bounds Δr^{lb} and Δr^{ub} can be determined by the design specification, Δy^{lb} and Δy^{ub}, the inputs u, and the fault types. Therefore, the test generation problem is to find a set of inputs u that determine the bounds Δr^{lb} and Δr^{ub}. In other words, with the application of such inputs, if the parameter deviations are out of the bounds, by (3.2) the corresponding circuit performance will not meet the specification, and thus the circuit fails.

Unfortunately, during the design process, most analog circuits are designed to meet specifications without consideration of the testability, and thus fail to meet the condition in (3.2). More specifically, a set of nominal parameter values and the associated tolerances are

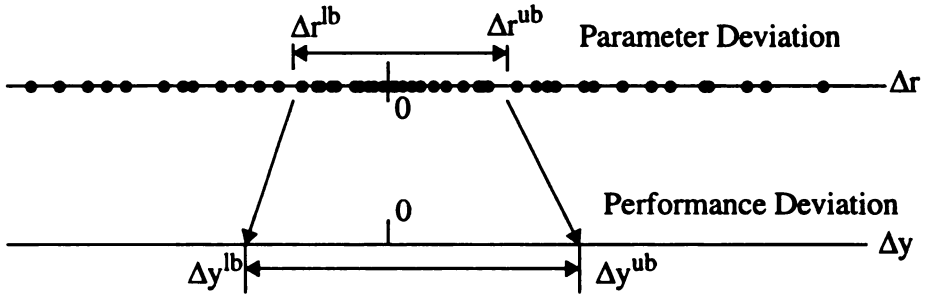


Figure 3.10 Relationship between parameter deviation and performance deviation.

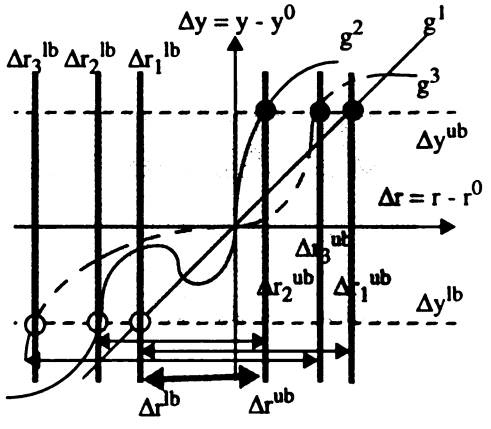


Figure 3.11 Example for the definition of parameter deviation bounds.

selected to meet the design specification. The designed circuit meets the specification, if all parameters are selected within the tolerances. In many designs, however, the circuit still meets the specification even if a parameter deviation is much larger than the tolerance. A simple testability design rule can be developed for the designed analog circuits to satisfy (3.2) and thus we are able to define the parameter bounds for generating test vectors for all fault types.

Consider the performance of a designed circuit

$$y=Y(u,r) \tag{3.3}$$

where $u=(u_1,u_2,...,u_n)$, $r=(r_1,r_2,...r_q)$, and $y=(y_1,y_2,...,y_m)$, are the vectors of the input variables, circuit parameters, and specifications, respectively. Let $r^0=(r_1^0,r_2^0,...,r_q^0)$ and $y^0=(y_1^0,y_2^0,...., y_m^0)$ be the nominal parameters and nominal performance, respectively, and $\Delta r=r-r^0$ and $\Delta y=y-y^0=(\Delta y_1,\Delta y_2, ...,\Delta y_m)$ are the parameter deviation and performance deviation, respectively. The i-th specification deviation can be expressed as

$$\Delta y_i=y_i-y^0_i=Y_i(u,r^0+\Delta r)-Y_i(u,r^0)=g_i(u,\Delta r) \tag{3.4}$$

Note that, a specified behavior of an analog circuit is required for a whole range of input signals, for example, a frequency range, but an analog circuit can be tested at only a finite subset of the specifications. Without loss of generality, let $U=\{u^1,u^2,..,u^v\}$ be the collection of the discrete input vectors that are used to verify the above design. In other words, the circuit meets the i-th specification for all $u \in U$.

For simplicity, we first consider the case that $r=(r_1)$, i.e., $q=1$. Let Δy_i^{lb} and Δy_i^{ub}

be the lower and upper bounds of Δy_i, respectively. Thus,

$$\Delta y_i^{lb} \leq g_i(u^j, \Delta r) \leq \Delta y_i^{ub} \text{ for all } u^j \in U. \tag{3.5}$$

Let Δr_j^{lb} and Δr_j^{ub} be the circuit parameter deviations, for u^j, that satisfy

$$\Delta y_i^{lb} = g_i(u^j, \Delta r_j^{lb}) \text{ and } \Delta y_i^{ub} = g_i(u^j, \Delta r_j^{ub}) \tag{3.6}$$

i.e. each function $g^j = g(u^j, \Delta r)$ intersects Δy_i^{lb} and Δy_i^{ub} at Δr_j^{lb} and Δr_j^{ub}, respectively, as shown in Figure 3.11, with the input set $U=\{u^1, u^2, u^3\}$. The circuit performance meets the i-th specification for u^j if the parameter deviation lies within the bounds, i.e., $\Delta r_j^{lb} \leq \Delta r \leq \Delta r_j^{ub}$. Therefore, a circuit is easily testable if it is designed in such a way that the performance variation falls outside the bounds when the parameter deviation falls outside the bounds. In other words, a circuit is easily testable if the function g^j intersects at most one point to each of the performance deviation bounds, Δy_i^{lb} and Δy_i^{ub}, as shown in Figure 3.11, each g^j intersects Δy^{lb} and Δy^{ub} at Δr_j^{lb} and Δr_j^{ub}, respectively. This concludes the following testability design rule,

A designed circuit is easily testable if g intersects at most one point to each of the performance deviation bounds for all Δy_i and for all $u^j \in U$.

Similarly, the testability design rule can be applied for the general case $r=(r_1, r_2, ..., r_q)$.

3.3.3 Test Generation and Fault Coverage

The conditions in (3.2) implies that the performance deviation lies within the bounds, i.e., $\Delta y_i^{lb} \le g(u,\Delta r) \le \Delta y_i^{ub}$, if the parameter deviation Δr_j, for u^j, also lies within bound $[\Delta r_j^{lb}, \Delta r_j^{ub}]$. Note that all bounds $[\Delta r_j^{lb}, \Delta r_j^{ub}]$ contain the point $\Delta r=0$. Therefore, there exists a bound $[\Delta r^{lb}, \Delta r^{ub}]$ that ensures the circuit performance meets the i-th specification for all $u^j \in U$, where

$$[\Delta r^{lb},\Delta r^{ub}] = \cap \{[\Delta r_j^{lb},\Delta r_j^{ub}] \mid j=1,2,...,v\} \tag{3.7}$$

For example, as shown in Figure 3.11,

$$[\Delta r^{lb},\Delta r^{ub}] = [\Delta r_1^{lb},\Delta r_1^{ub}] \cap [\Delta r_2^{lb},\Delta r_2^{ub}] \cap [\Delta r_3^{lb},\Delta r_3^{ub}] = [\Delta r_1^{lb},\Delta r_2^{ub}]$$

i.e. both bounds Δr^{lb} and Δr^{ub} are determined by u^1 and u^2, respectively. This means that the i-th specification fails if the parameter deviation Δr_1 is less than Δr_1^{lb} when u^1 is applied, or greater than Δr_2^{ub} when u^2 is applied. Therefore, both u^1 and u^2 are taken as the test vectors. This concludes that u^{jl} and u^{ju} are taken as the test vectors if $\Delta r_{jl}^{lb}=\Delta r^{lb}$ and $\Delta r_{ju}^{ub}=\Delta r^{ub}$. Note that if more than one input satisfies $\Delta r_{jl}^{lb}=\Delta r^{lb}$ or $\Delta r_{ju}^{ub}=\Delta r^{ub}$, one of them is selected as a test vector.

Let F=(f_1, f_2, ..., f_w) be the collection of the fault types, and $U^b(f_k)$, k=1,2,...,w, be the set of test vectors for testing the fault type f_k. Since the test vectors are selected from the discrete input set U, one test vector may simultaneous determine several bounds for different fault types. The duplicated test vectors should be eliminated. Thus, the developed test generation process is comprised of two steps: *Test set selection* and *Test set compaction*. The former step selects the test vectors as described above, and the latter step eliminates the duplicated test vectors. The final test set is compacted as follows,

$$TS = \cap \{U^b(f_k) \mid k=1,2,..,w\} \tag{3.8}$$

Let F=(f_1,f_2,..., f_w) be the collection of the collapsed fault types, and N_{Fi} be the number of defects that cause their circuit behaviors to be with the fault type f_i. Thus, the total number of faults N_F is the sum of all N_{Fi}'s, i=1,2,...,w. Based on the test set derived from the test generation process, the test set TS will detect M_{Fi} faults with the fault type f_i, and the total detected faults, M_F, is the sum of all M_{Fi}, i=1,2,...,w. Therefore, the fault coverage is defined as M_F/N_F.

3.3.4 Example

Consider the current copier in Figure 2.2(b). Figure 3.12 is its equivalent circuit excluding the amplifier, where the current switch S_1 is modeled as a linear resistor r_S, and the input current I_{in}, $0 \le I_{in} \le I_{ref}$. In the presence of a Type 1 fault, or a non-catastrophic Type 2 fault, the transistor M_1 works in the linear region, and thus its drain current I_d, or

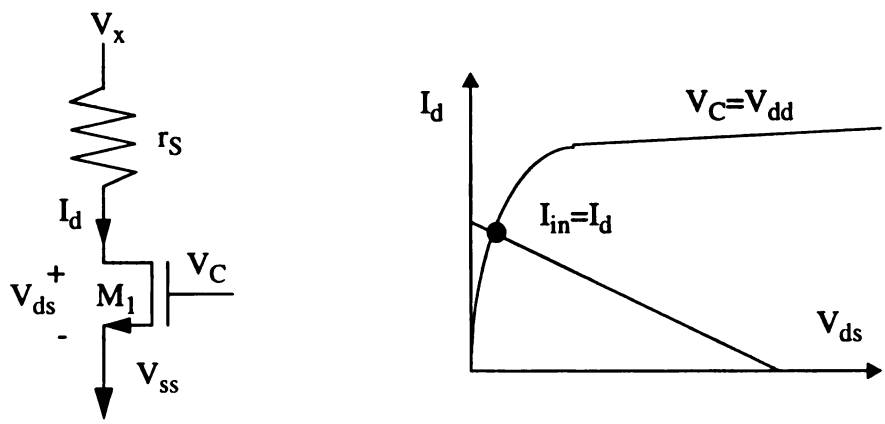


Figure 3.12 Equivalent circuit of the portion including transistor and current switch of the current copier, and its I-V characteristic.

the current held in the copier, can be expressed as follows,

$$I_d=F_d(r_S,V_C)= \frac{1}{r_S}\times\left(V_x-V_C+V_{th}-\frac{1}{r_S\beta}+\sqrt{\left(V_{dd}-V_{ss}-V_{th}+\frac{1}{r_S\beta}\right)^2-\frac{2(V_x-V_{ss})}{r_S\beta}}\right) \qquad (3.9)$$

where V_{th} and β are the threshold voltage and gain factor of M_1, respectively, and V_C is the voltage across the capacitor. Let r_{on} and $I_{out(on)}$ be the on-resistance and output current when S_1 is on, respectively, in the presence of a Type 1 fault, and r_{off} and $I_{out(off)}$ be the off-resistance and leakage current when S_1 is off, respectively, in the presence of a Type 2 fault. By (3.9), the output current $I_{out(on)}=F_d(r_{on},V_{dd})$ because, in the presence of a Type 1 fault, the largest voltage $V_C=V_{dd}$ is calibrated to make $I_{out(on)}$ to be as close to I_{in} as possible, and $I_{out(off)}=F_d(r_{off},V_C)$ in the presence of a Type 2 fault, where V_C is a function of I_{in}. Let $I^o_{out(on)}$ and $I^o_{out(off)}$ be the nominal output currents when the switch is on and off, respectively, i.e., $I^o_{out(on)}=I_{in}$ when the switch is on, and $I^o_{out(off)}=0$ when the switch is off. Let r^0_{on} and r^0_{off} be the nominal on-resistance and off-resistance, respectively, where $r_{on}=r^0_{on}+\Delta r_{on}$, and $r_{off}=r^0_{off}+\Delta r_{off}$. Therefore, the output current deviations are

$$\Delta I_{out(on)}=I_{out(on)}-I^o_{out(on)}=F_d(r_{on},V_{dd})-I_{in}=g_{on}(I_{in},\Delta r_{on}); \text{ and} \qquad (3.10a)$$

$$\Delta I_{out(off)}=I_{out(off)}-I^o_{out(off)}=F_d(r_{off},V_C)=g_{off}(I_{in},\Delta r_{off}) \qquad (3.10b)$$

It can be shown that both g_{on} and g_{off} meet the conditions for the testability design rule. Suppose that the system specification are given as follows

"the error output current is less than I_{error} when S_1 is on,

and the leakage current must be less than I_{leak} when S_1 is off"

Let f_i, i=1,2,3, be the Type i fault of the current switch. For f_1, the on-resistance is too high and the off-resistance is unchanged, i.e., r_{on} is critical, but r_{off} is non-critical, or $\Delta r=(\Delta r_{on},0)$. From the system specification, $-I_{error} \le \Delta I_{out(on)} \le 0$, by (3.9) and (3.10), the bounds of r_{on} can be derived as follows,

$$r_{on}^{lb}=0; \text{ and } r_{on}^{ub}=F_S(V_{dd},-I_{error}+I_{in})/(-I_{error}+I_{in})$$

where

$$F_S(V_C,i)=-(V_C-V_x-V_{th})+\sqrt{(V_c-V_x-V_{th})^2+(V_x-V_{ss})(2V_{dd}-V_{ss}-2V_{th}-V_x)-\frac{2}{\beta}i} \qquad (3.11)$$

As a result, the lower and upper bounds are

$$\Delta r_{on}^{lb} = r_{on}^{lb} - r^o_{on} = -r^o_{on} \text{ ; and}$$

$$\Delta r_{on}^{ub} = r_{on}^{ub} - r^o_{on} = F_S(V_{dd},-I_{error}+I_{in})/(-I_{error}+I_{in}) - r^o_{on}$$

Since the minimum upper bound is obtained when $I_{in}=I_{ref}$, for Type 1 fault, f_1, we conclude

$$\Delta r_{on}^{lb}(f_1) = -r^o_{on}; \text{ and } \Delta r_{on}^{ub}(f_1) = \Delta r_{on(min)}^{ub}$$

$$= F_S(V_{dd},-I_{error}+I_{ref})/(-I_{error}+I_{ref}) - r^o_{on}, \qquad (3.12)$$

Similarly, for Type 2 fault, the off-resistance R_{off} is too small and the off-resistance is unchanged when the switch is off. Thus, we only consider the critical parameter r_{off}. Based on the specification, $0 \leq \Delta I_{out(off)} \leq I_{leak}$, the bounds of r_{off} can be derived as follows,

$$r_{off}^{lb} = F_S(V_c, I_{leak})/I_{leak}; \text{ and } r_{off}^{ub} = +\infty$$

Since the maximum lower bound is obtained when $V_C = V_{C(max)}$, for Type 2 fault, f_2, we conclude

$$\Delta r_{off}^{ub}(f_2) = +\infty; \text{ and } \Delta r_{off}^{lb}(f_2) = r_{off(max)}^{lb} - r^o_{off}$$

$$= F_S(V_{c(max)}, I_{leak})/I_{leak} - r^o_{off}. \quad (3.13)$$

Note that $V_{C(max)}$ is derived from the equation, $I_{ref} = (\beta/2)(V_{c(max)} - V_{ss} - V_{th})^2$. For Type 3 fault, both r_{on} and r_{off} are critical and the bounds are

$$\Delta r_{on}^{ub}(f_3) = \Delta r_{on}^{ub}(f_1) \text{ and } \Delta r_{on}^{lb}(f_3) = -r^o_{on}. \quad (3.14)$$

$$\Delta r_{off}^{ub}(f_3) = +\infty \text{ and } \Delta r_{off}^{lb}(f_3) = \Delta r_{off}^{lb}(f_2).$$

The following fault ranges are derived based on the following parameter values:

V_{dd}=2.5V; V_{ss}=-2.5V; V_x=0V;I_{ref}=100μA; V_{th}=0.822163V; β=7.34e-5;

I_{error}=0.1μA; I_{leak}=0.1μA; R_{on}=5.9kΩ; R_{off}=6.3x10^{12}Ω

As a result, the voltage $V_{c(max)}$=-0.027V. Thus, the bounds are

$\Delta r_{on}^{ub}(f_1)$ = 15.726kΩ and $\Delta r_{on}^{lb}(f_1)$ = -5.9kΩ

$\Delta r_{off}^{ub}(f_2)$ =+∞ and $\Delta r_{off}^{lb}(f_2)$ =-6.299975x10^{12}Ω

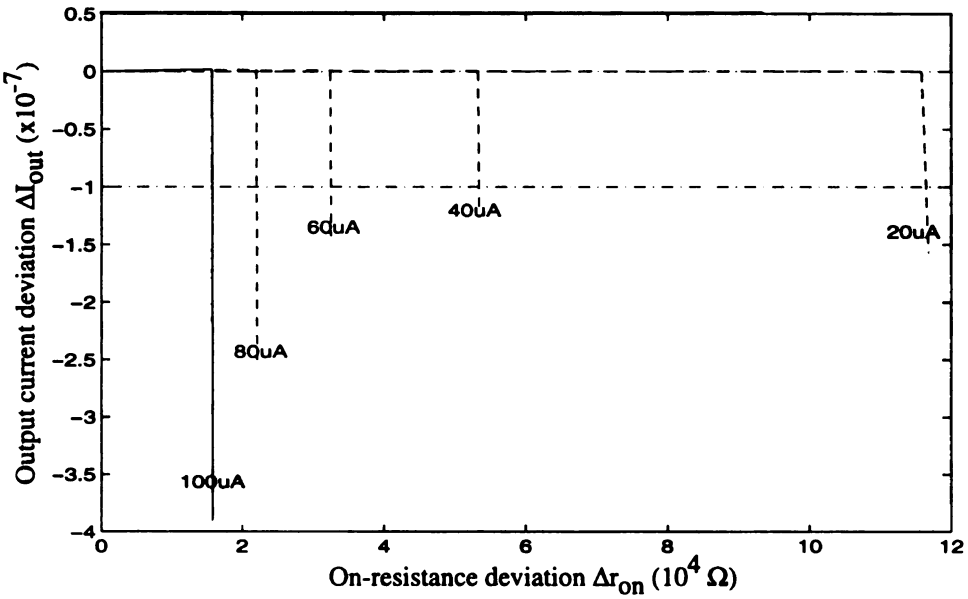
$\Delta r_{on}^{ub}(f_3)$ = 15.726kΩ and $\Delta r_{on}^{lb}(f_3)$ = -5.9kΩ

$\Delta r_{off}^{ub}(f_3)$ =+∞ and $\Delta r_{off}^{lb}(f_3)$ =-6.299975x10^{12}Ω

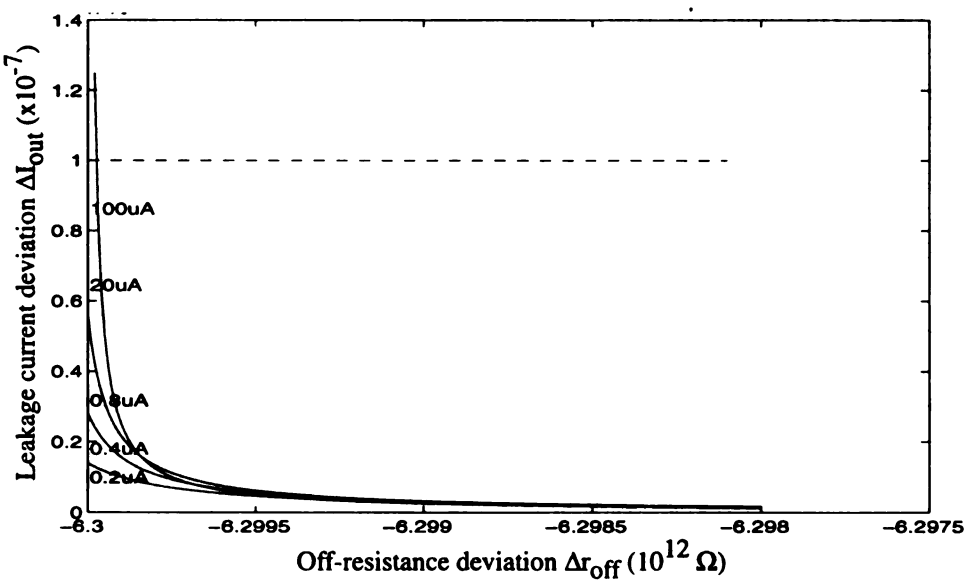
Figure 3.13(a) shows the simulation results of $\Delta I_{out(on)}$ versus various Δr_{on} for the input current I_{in}= 20, 40, 60, 80, 100μA. Results show that $\Delta r^{ub}{}_{on}(f_1)$=15.726kΩ and $\Delta r^{lb}{}_{on}(f_1)$=-$r^{o}{}_{on}$=-5.9kΩ. In other words, when the switch is on, the system fails when r_{on}>21.626kΩ or r_{on}< 0Ω. Similarly, Figure 3.13(b) illustrates the simulation for f_2, where $\Delta r^{ub}{}_{off}(f_2)$=∞, $\Delta r^{lb}{}_{off}(f_2)$=-6.299975x$10^{12}$Ω.

For Type 1 fault, as shown in Figure 3.13(a), $\Delta r^{ub}{}_{on}$=15.726kΩ, when I_{in}=I_{ref}=100μA, and $\Delta r^{lb}{}_{on}$=-5.9kΩ, for all I_{in} Thus, $U^b(f_1)$={100μA}. Similarly, $\Delta r^{lb}{}_{off}$=-6.299975x10^{12}Ω when I_{in}= 100μA, i.e., $U^b(f_2)$={100μA}, and $U^b(f_3)$={100μA}. By (3.9), the compacted test set is TS={100μA}, i.e., the input current I_{in}=100μA detects all three fault types.

As mentioned, In this experiment, we have injected 3500 defects to the current switch layout and the defects are generated using the IFA procedure. Among the defects, the statistics of the defect counts and fault counts for three fault types are summarized in



(a)



(b)

Figure 3.13 Simulation results: (a) for f_1; and (b) for f_2.

Table 3.1. It shows that there are 3146 defects that would not cause any major malfunction of the switch, i.e., they do not change the on-resistance and off-resistance of the switch, and 354 defects that change on-resistance and/or off-resistance, where the fault counts for Types 1, 2, and 3 faults are 202, 137, and 15, respectively. As shown in Table 3.1, for Type 1 faults, there are 172 defected circuits whose on-resistances are out of bounds, while the remaining 30 are kept within the bounds even though the defects cause the parameter deviations. Among the 172 defected circuits, 114 are open circuits, i.e., $r_{on}= +\infty$. Similarly, among 137 circuits with the Type 2 fault, the off-resistances of 134 circuits are out of bounds, and 3 remains within the bounds. Among the 134 circuits, 121 are short circuits, i.e., $r_{off}=0$. Finally, for Type 3 faults, 12 are out of bounds, while 3 are within the bounds. In summary, among 3500 defects, 3182 circuits are fault-free and only 318 circuits are faulty. Using the test vector $I_{in}=I_{ref}=100\mu A$, we detect all 318 faults. Thus, the fault coverage is 100%.

The fault counts in Table 3.1 also show that the total number of catastrophic faults, i.e., open and short circuits, is 235, while the number of parametric faults is 83. In other words, the catastrophic faults take 76.1% of the total faults. This concludes that, with the assumption of catastrophic faults, the fault coverage can achieve at most 76%.

It should be mentioned that the full coverage is achieved based on the assumption that the measurement is performed by a perfect instrument. There always exist some measurement errors in any test environment. Thus, the test environment should be one of the major parameters for fault coverage evaluation. When the measurement errors are taken into consideration, some fault ranges may be changed. In general, the fault ranges may be shrunk and thus some faults may not be detected due to the measurement errors. Thus, the

Table 3.1 Defect and fault count distributions.

Type 1 faults

On-resistance	count
$-5.9k\Omega < \Delta r_{on} < 15.726k\Omega$	30
$15.726k\Omega < \Delta r_{on} < +\infty$	58
$\Delta r_{on} = +\infty$ (open circuit)	114

Type 2 faults

Off-resistance	count
$-6.299975 \times 10^{12}\Omega < \Delta r_{off} < +\infty$	3
$-6.3 \times 10^{12}\Omega < \Delta r_{off} < -6.299975 \times 10^{12}\Omega$	13
$\Delta r_{off} = -6.3 \times 10^{12}\Omega$ (short circuit)	121

Type 3 faults

count: Δr_{on} / Δr_{off}	$-5.9k\Omega < \Delta r_{on} < 15.726k\Omega$	$15.726k\Omega < \Delta r_{on} < +\infty$	$\Delta r_{on} = +\infty$
$-6.299975 \times 10^{12}\Omega < \Delta r_{off} < +\infty$	3	0	--
$-6.3 \times 10^{12}\Omega < \Delta r_{off} < -6.299975 \times 10^{12}\Omega$	5	7	--
$\Delta r_{off} = -6.3 \times 10^{12}\Omega$ (short circuit)	--	--	--

Defect Count Distribution

Circuit Behavior	count	out-of-bounds	within bounds
Type 1 faults	202	172	30
Type 2 faults	137	134	3
Type 3 faults	15	12	3
Fault-free	3146		3146
Total	3500	318	3182
		faulty	fault-free

Table 3.2 Defect and fault count distributions.
(With inaccurate test instrument)

Type 1 faults

On-resistance	count
$-5.9k\Omega < \Delta r_{on} < 15.726k\Omega$	30
$15.726k\Omega < \Delta r_{on} < +\infty$	58
$\Delta r_{on} = +\infty$(open circuit)	114

Type 2 faults

Off-resistance	count
$-6.299975x10^{12}\Omega < \Delta r_{off} < +\infty$	5
$-6.3x10^{12}\Omega < \Delta r_{off} < -6.299975x10^{12}\Omega$	11
$\Delta r_{off} = -6.3x10^{12}\Omega$ (short circuit)	121

Type 3 faults

count: Δr_{off} \ Δr_{on}	$-5.9k\Omega < \Delta r_{on} < 15.726k\Omega$	$15.726k\Omega < \Delta r_{on} < +\infty$	$\Delta r_{on} = +\infty$
$-6.299975x10^{12}\Omega < \Delta r_{off} < +\infty$	5	2	--
$-6.3x10^{12}\Omega < \Delta r_{off} < -6.299975x10^{12}\Omega$	3	5	--
$\Delta r_{off} = -6.3x10^{12}\Omega$ (short circuit)	--	--	--

Defect Count Distribution

Circuit Behavior	count	out-of-bounds	within bounds
Type 1 faults	202	172	30
Type 2 faults	137	132	5
Type 3 faults	15	10	5
Fault-free	3146		3146
Total	3500	314	3186
		faulty	fault-free

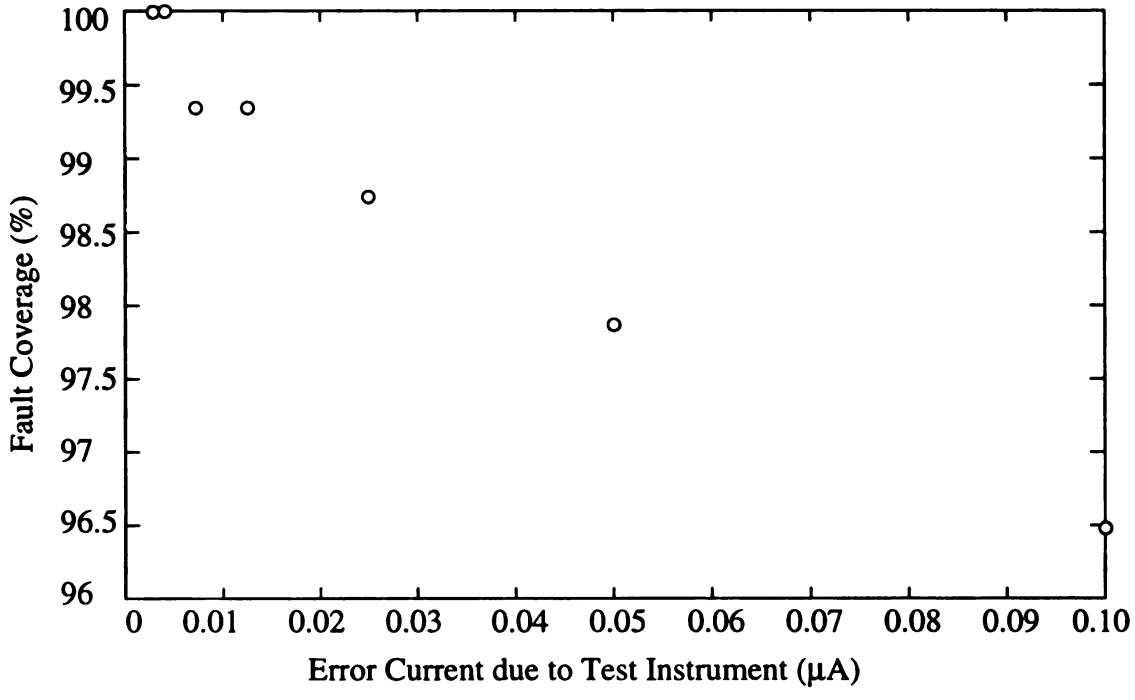


Figure 3.14 Fault coverages with respect to accuracy of test instrument.

fault coverage may be affected by the inaccurate measurement instrument.

For example, assume that the test instrument has a 10% inaccuracy, i.e., $\Delta I_{out(on)}$<-0.11μA and $\Delta I_{out(off)}$>0.11μA. Therefore, the bounds are obtained as Δr^{lb}_{off}=-6.2999773x$10^{12}\Omega$ and Δr^{ub}_{on}=15.729kΩ. The experimental results, as summarized in Table 3.2, show that, when Δr^{ub}_{on} is changed from 15.726kΩ to 15.729kΩ, the number of circuits whose on-resistances are out-of-bounds remains the same. However, the change of Δr^{lb}_{off}, from -6.299975x$10^{12}\Omega$ to -6.2999773x$10^{12}\Omega$, causes two circuits with a *Type 2* fault and two with a *Type 3* fault to become undetectable. Thus, with the test vector *Iin*=100μA, we detect only a total of 314 faults. The fault coverage is M_F/N_F=314/318=98.7%. This concludes that the full fault coverage is not achieved because of the inaccuracy of the test environment.

Figure 3.14 plots the fault coverages of the current switch with respect to the inaccuracy of the test instrument ranging from 0 to 100%. It shows that a full coverage can be achieved when the inaccuracy is within 0.002mA for the output current. It is necessary to keep within 0.5% for achieving a 99% fault coverage.

3.4 Discussion

This chapter presents an effective IFA-based fault macromodeling process that maps the specification-driven analog testing process to a simple fault-model-based process. The IFA-based fault macromodeling process defines practical fault types and generates test sets. A set of testability design rules was included to guarantee the existence of parameter deviation bounds and to simplify the test generation process. It also shows that the use of

built-in tester can further simplify the test generation process and reduce testing time. However, the IFA has inherent high computational complexity and limited to small circuit applications. Therefore, for practical circuit design, the reduction of computational complexity with the IFA technique is of major concern.

Based on the parameter deviation bounds derived from the design specification, a set of discrete inputs used for design verification, and the faulty types, one can generate the test vectors and evaluate the fault coverage. However, the assumption that the parameter deviation bounds exist may not be always valid for today's circuit design process. This is simply because that today's design process placed its emphasis on the design for functionality, but not for testability, and thus the bounds may not exist. More specifically, a set of nominal parameter values and the associated tolerances may be selected to meet the design specification by the most of commercial design tools. The designed circuit meets the specification, if all parameters are selected within the tolerances. In many designs, however, the circuit still meets the specification even if a parameter deviation is far beyond the tolerance. Therefore, the testability design concept is needed for designing easily testable analog circuits. This can be accomplished by a set of testability design rules.

Finally, as discussed in Section 3.2.3, a high-precision built-in tester can simplify test sequence and reduce testing time significantly.

Chapter 4

TESTABILITY ENHANCEMENT

To reduce the computational complexity of the fault macromodeling process with the IFA technique, Section 4.1 presents a hierarchical fault macromodeling process [17]. Section 4.2 proposes some refinements of the testability design rules [51] which generate easily testable circuits. Section 4.3 presents high-accuracy built-in tester [61] which not only increases the observability of ICs, but also simplifies the test generation process and resultant test sequence. It also discusses the trade-offs between the complexities of the tester and the test sequence and addresses some design issues.

4.1 Hierarchical IFA-Based Fault Macromodeling

The IFA technique is applicable only for small circuits because it requires a tremendous computational time. The hierarchical structures, as shown in Figure 4.1, illustrate the computational complexity of the process with the IFA technique. Note that the ADC is constructed from two NMOS current copiers and one PMOS current copier together with other components such as comparator, sources, and digital circuits, while the current copier includes a current switch. For purpose of comparison, the simulation cost is modeled as

$$T_{CS} = T_S * N + T_{ovh} \tag{4.1}$$

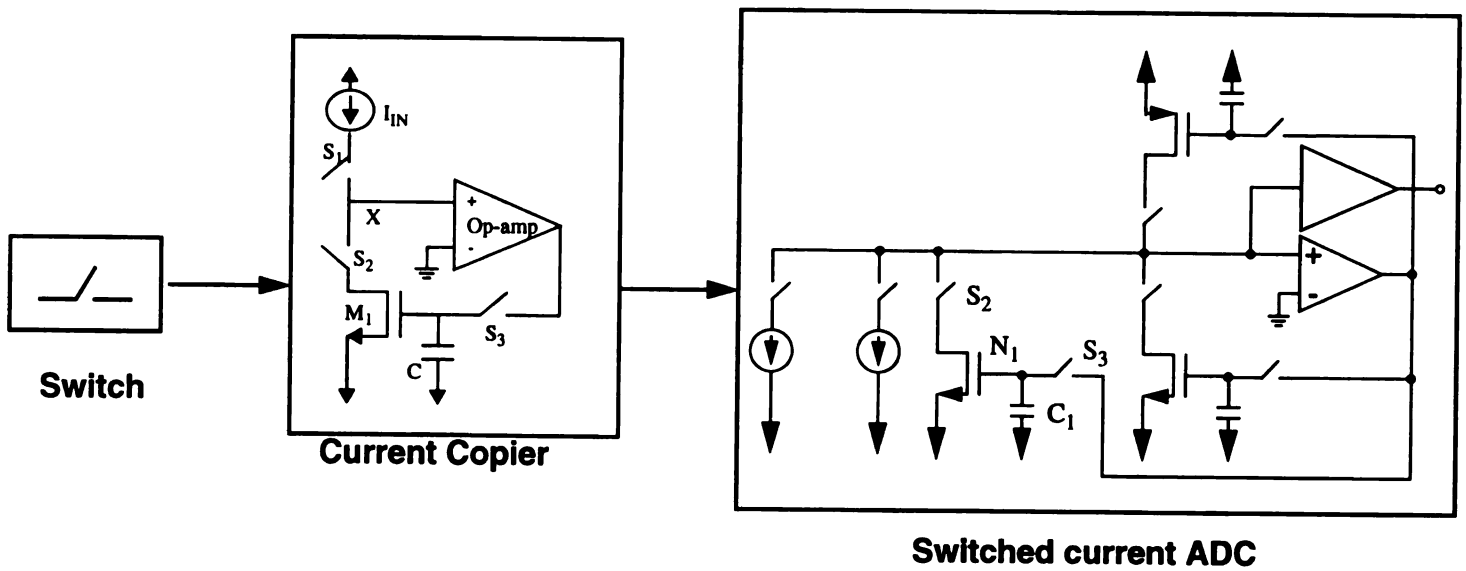


Figure 4.1 Computational complexities of IFA process.

where T_{CS} is the time required for circuit simulations for entire IFA process, T_S is the time required for simulating a circuit one time, N is the number of significant defects to be simulated, and T_{ovh} is the time overhead due to unsuccessful simulations. Note that the value of N is proportional to the layout area. For simplicity, we assume that $T_{ovh}=0$, i.e., all simulations are successful. For the current switch, N=354 and $T_s=2$ seconds, for the current copier, N=2242, and $T_s=20$ seconds, and for the ADC, N=5310 and $T_s=15$ minutes. Thus, by (4.1), the simulation costs for the current switch, current copier, and ADC are 11.8 minutes, 12.45 hours, and 55.3 days, respectively.

The basic concept behind the hierarchical fault macromodeling is to decompose a large circuit into many smaller subcircuits. For example, the ADC can be decomposed into three current copiers, one comparator, and two current sources. If we assume that all 6 components have the same computational complexity with the IFA technique, i.e., each component takes 12.25 hours. Thus, the 6 components take a total of 74.7 hours, or 3 days, which is much better than 55.3 days for directly applying the IFA technique to the ADC.

Section 4.1.1 describes the decomposing principles and how to build a macro library for the hierarchical fault macromodeling process. Based on cell and macro libraries, Section 4.1.2 presents the estimation of fault coverage in a hierarchical structure.

4.1.1 Macro Library

For a reasonably large circuit, it is decomposed into smaller subcircuits. The subcircuits may be further decomposed until they can be handled comfortably by the IFA technique. For simplicity of discussion, the subcircuits which can be comfortably handled

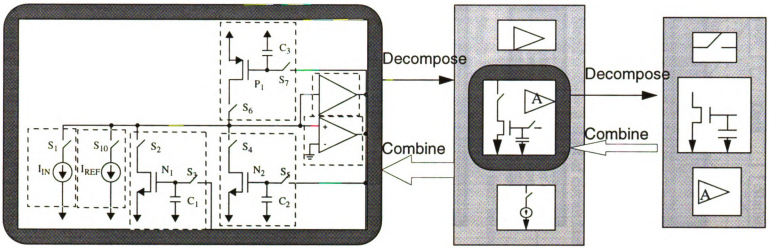


Figure 4.2 Concept of hierarchical fault modeling.

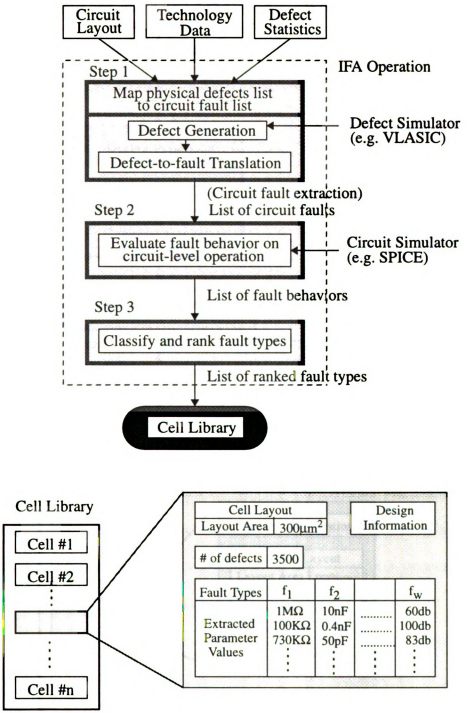
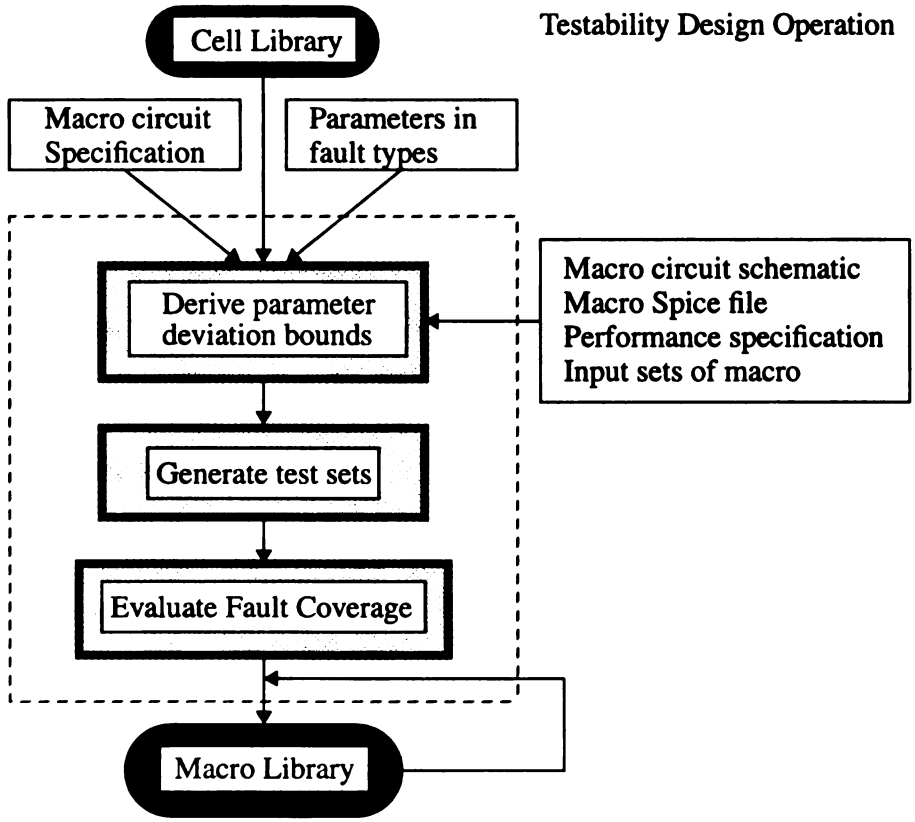
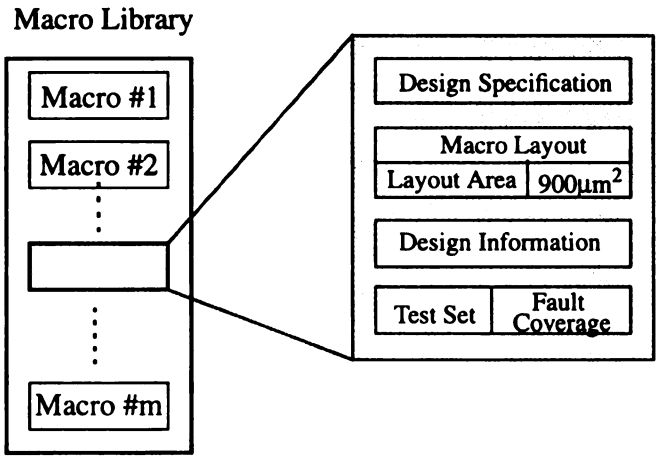


Figure 4.3 Cell library of hierarchical IFA-based fault macromodeling.



(a)



(b)

Figure 4.4 Macro library of hierarchical IFA-based fault macromodeling.

by the IFA technique is referred to as primitive cells (PCs), and a macro is a subcircuit which is comprised of many PCs and/or some smaller macros. Figure 4.2 shows a current copier macro which is comprised of four PCs: current switch, voltage switch, storage unit, and an op-amp. It also shows that the ADC is comprised of the current copier macros and the PCs: comparator and current sources.

A cell library, as illustrated in Figure 4.3, is generated by the IFA-based fault macromodeling process for each PC. The database for each PC includes the number of defects has been simulated, cell layout and layout area, the ranked fault types, the extracted parameter values for each fault types, and some design information. The cell library is used to construct a macro library, as illustrated in Figure 4.4. The test set of a macro is a collection of the test sets of all PCs it employs, and the fault coverage of the macro is estimated from those of the PCs. Given a macro specification, the macro schematic, Spice file, and input sets for design verification were generated during the design phase. Based on the macro circuit specification, parameters in fault types, and the input sets for design verification, parameter deviation bounds for the macro are derived. The database of each macro includes the macro specification, macro layout and layout area, design information, test sets, and fault coverage. In our implementation, the hierarchical structure allows a macro includes many other macros and/or PCs.

Since the test set of a macro is a collection of those of the PCs it employs, the test set can be reduced by dropping the equivalent faults. For example, the voltage switch, VSW, in Figure 4.5, has four fault types, as described in Section 3.2, and the op-amp (OP) is assumed to has two fault types: The open loop gain is too small (fault type f_{OP1}), and the output resistance r_o is too large (f_{OP2}). Since the faults on r_o and r_{on} have the same fault

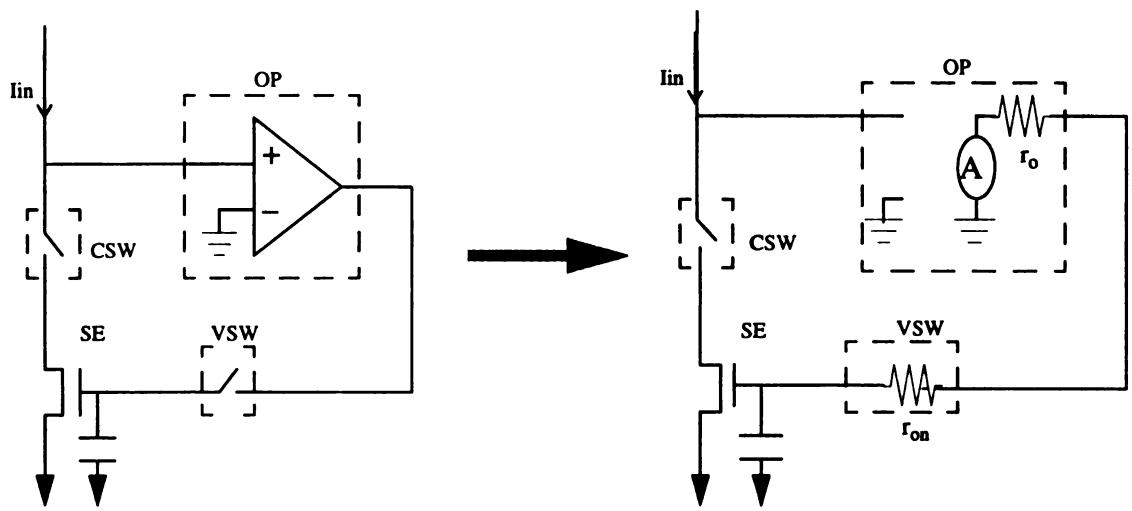


Figure 4.5 Fault equivalence.

behaviors when the voltage switch is on, as the equivalent circuit shown in Figure 4.5, the fault type f_{OP2} is equivalent to the fault type f_1 in the VSW. Thus, dropping the equivalent faults will reduce the number of fault types to be simulated and thus simplify the test generation and fault simulation processes.

4.1.2 Fault Coverage Estimation

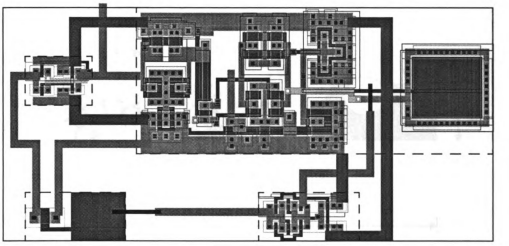
The fault coverage of a macro can be evaluated as follows. Let A_{pi} be the layout area of the i-th primitive cell, P_{si} be the ratio of the significant defects over all injected defects, and FC_i be its fault coverage. Thus, the fault coverage of a macro is

$$FC = (\sum_i A_{pi} P_{si} FC_i)/(\sum_i A_{pi} P_{si}) \qquad (4.2)$$

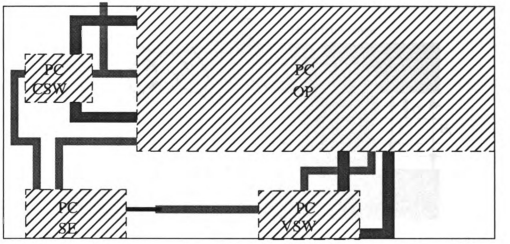
In practice however, the routing area is still susceptible to defects. The routing area depends on applications. The fault coverage of the routing area should be also evaluated.

Consider a macro, namely, current copier, in Figure 4.1. It is comprised of four primitive cells (PCs): current switch (CSW), voltage switch (VSW), storage element (SE), and Op-amp (OP). The macro layout is shown in Figure 4.6(a). Figure 4.6(b) shows the primitive cells and the remaining routing area.

The fault coverage for the routing area is evaluated as follows. Two major defects on interconnects are considered: etching and extra. The etching defects cause the interconnect layer to become narrower or even break, while the extra defects make two adjacent interconnects to become closer or even short. Let W_t be the etching width caused by etching defect(s), as shown in Figure 4.7(a). A hard fault (open circuit) occurs if $W_t > W_{max}$; a parametric fault results if $W_{min} \le W_t \le W_{max}$; and no fault occurs if $W_t < W_{min}$. Empirical

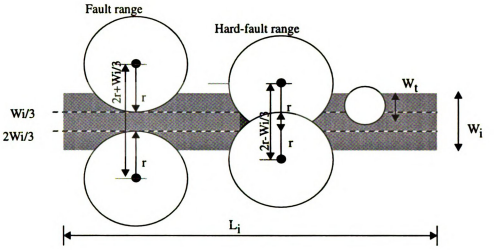


(a)

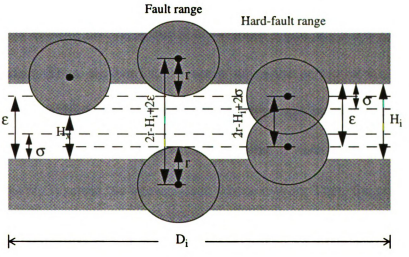


(b)

Figure 4.6 Macro "current copier": (a) layout; and (b) routing area.



(a)



(b)

Figure 4.7 Fault coverage for routing area: (a) due to etching defect; and (b) due to extra defect.

results show that $W_{max}=2W_i/3$ and $W_{min}=W_i/3$, where W_i is the width of the interconnect. On the other hand, let H_x, as indicated in Figure 4.7(b), be the shrinking distance between two interconnects due to extra defects. If the normal distance between two segment is H_i, then the faults caused by extra defect(s) can be modeled as follows: a hard fault (short circuit) occurs if $H_x < \sigma$; a parametric fault results if $\sigma \le H_x \le \varepsilon$; and no fault occurs if $H_x > \varepsilon$, where σ and ε are determined by the technology employed.

To simplify the estimation of fault coverage of both defects on the interconnects of the routing area, it is assumed that only hard faults are testable. This implies that the fault coverage is the worst case estimation. Let FC_t be the fault coverage for the total faults caused by the etching defects, P_{th} and P_{ts} respectively be the probabilities of having the hard faults and total faults. Thus, the fault coverage for etching defects is $FC_t=P_{th}/P_{ts}$. Hard faults due to etching defects occur if the etching width $W_t > 2W_i/3$. Let r be the radius of the defect. Thus, the hard faults occur when the center of the defect locates within a range with width of $(2r-W_i/3)$ across the interconnect, as shown in Figure 4.7(a), where $r > W_i/3$. Similarly, a fault occurs when the center of defect locates within a range with width of $(2r+W_i/3)$ across the interconnect, where $r > W_i/6$. Thus, the probability P_{ts} is

$$P_{ts}= \frac{1}{A_s}\sum_i \int_{W_i/6}^{\infty} L_i\left(2r+\frac{W_i}{3}\right) f(r)\,dr \qquad (4.3)$$

where A_s is the entire routing area, and the p.d.f. of the defect radius is given in (3.1). Therefore,

$$P_{ts}=\frac{1}{A_s}\sum_i L_i\left[\frac{8}{3}x_o+\frac{W_i}{3}-\frac{5W_i^3}{648x_o^2}\right], \text{ if } (W_i/6)\le x_0; \text{ or } P_{ts}=\frac{1}{A_s}\sum_i \frac{18L_i x_o^2}{W_i}, \text{if } (W_i/6)>x_0; \qquad (4.4)$$

Similarly, the probability of P_{th} is

$$P_{th}= \frac{1}{A_s}\sum_i \int_{W_i/3}^{\infty} L_i\left(2r-\frac{W_i}{3}\right)f(r)dr \text{ , } r > W_i/3.$$

Thus,

$$P_{th}=\frac{1}{A_s}\sum_i L_i\left[\frac{8}{3}x_o-\frac{W_i}{3}-\frac{W_i^3}{162x_o^2}\right], \text{ if } (W_i/3)\le x_0; \text{ or } P_{th}= \frac{1}{A_s}\sum_i \frac{9L_i x_o^2}{2W_i}, \text{if } (W_i/3)>x_0; \quad (4.5)$$

Let P_{xh} and P_{xs} respectively be the probabilities of having the hard faults and total faults due to extra defects. Thus, the fault coverage for extra defects is $FC_x=P_{xh}/P_{xs}$. Hard faults due to extra defects occur when the center of the defect locates within the range with width of $(2r-H_i+2\sigma)$ in the gap between the two adjacent interconnects, as indicated in Figure 4.7(b), where $(H_i-\sigma)/2<r<r_M$ and r_M is a specified maximum value of r such that a defect with radius larger then r_M will also caused sever damage on primitive component. Similarly, a fault occurs when the center of defect locates within the range with width of $(2r-H_i+2\varepsilon)$ in the gap between the two adjacent interconnects, where $(H_i-\varepsilon)/2<r<r_M$. Thus, the probability P_{xs} is

$$P_{xs}=\frac{x_o^2}{A_s}\sum_i \int_{\frac{(Hi-2\varepsilon)}{2}}^{r_M} D_i(2r-H_i+2\varepsilon)f(r)dr \quad (4.6)$$

Therefore,

$$P_{xs}=\frac{x_o^2}{A_s}\sum_i D_i\left(-\frac{2}{r_M}+\frac{H_i-2\varepsilon}{2r_M^2}+\frac{2}{H_i-2\varepsilon}\right), \text{ if } (H_i-2\varepsilon)<2r_M \quad (4.7)$$

Similarly, the probability of P_{xh} is

$$P_{xh}=\frac{x_o^2}{A_s}\sum_i\int_{\frac{(Hi-2\sigma)}{2}}^{r_M} D_i(2r-H_i+2\sigma)f(r)dr \tag{4.8}$$

Thus,

$$P_{xh}=\frac{x_o^2}{A_s}\sum_i D_i\left(-\frac{2}{r_M}+\frac{H_i-2\sigma}{2r_M{}^2}+\frac{2}{H_i-2\sigma}\right), \text{ if } (H_i\text{-}2\sigma)<2r_M \tag{4.9}$$

If we assume that the occurrences of both etching and extra defects have the same probabilities, the fault coverage of the interconnects in the routing area is the average of both fault coverages, i.e., $FC_s=(FC_t+FC_x)/2$, or $[P_{th}/P_{ts}+P_{xh}/P_{xs}]/2$. Therefore, the total fault coverage of the macro is

$$FC = (A_sP_sFC_s+\sum_i A_{pi}P_{si}FC_i)/(A_sP_s+\sum_i A_{pi}P_{si}) \tag{4.10}$$

where A_s is the area of the routing area, and P_s is the ratio of the significant defects over the all defects.

4.2 Testability Design Rule

Due to the nonlinearity of their parameter-performance mapping, it is usually hard to generate test set with high fault coverage for analog/mixed-signal ICs. In order to solve this problem, the testability design rule has to be considered as early as in the design cycle.

A basic testability design rule has already been discussed in Section 3.3.2. This section presents a refinement of the testability design rule defined by the given design specifications, a set of discrete inputs used for design verification, and the fault types. The rule ensures the existence of the circuit parameter deviation bounds for these discrete inputs and for all fault types. The intersection of these parameter deviation bounds for each fault

type defines a parameter bound which is used to generate test vectors for that fault, to determine whether or not the corresponding specification fails, and to evaluate the fault coverage.

4.2.1 Development

Based on the test vector generation, the testability rule previously stated (Section 3.3.2) can be simplified as follows. The original testability rule requires that all g^j intersects at most one point at each of Δy_i^{lb} and Δy_i^{ub}, for all $u^j \in U$. In fact, since only u^{jl} and u^{ju} are taken as the test vectors, it is necessary only for g^{jl} and g^{ju} to intersect at most one point at Δy_i^{lb} and Δy_i^{ub}, respectively. Consider Figure 4.8(a), for example, g^3 intersects Δy_i^{ub} at three points, but u^3 does not determine Δr^{ub}. On the other hand, g^2 intersects Δy_i^{lb} at three points, and u^2 determines Δr^{lb}, but not Δr^{ub}. Therefore, the testability design rule can be modified as follows.

> *A designed circuit is easily testable if g^{jl} and g^{ju} intersects at most one point at Δy_i^{lb} and Δy_i^{ub}, respectively, for all Δy_i.*

The testability rule can be generalized. Consider the case of two-dimensional parameter deviations, as shown in Figure 4.8(b), where $U=\{u^1, u^2, u^3, u^4\}$. The bound for each u^j includes the point $\Delta r=0$. The intersection of the four bounds, as indicated by the shaded area, is bounded by those for u^2 and u^4. Thus, they are taken as the test vectors.

Figure 4.8(c) illustrates two cases that may affect the testability, where u^2 and u^4

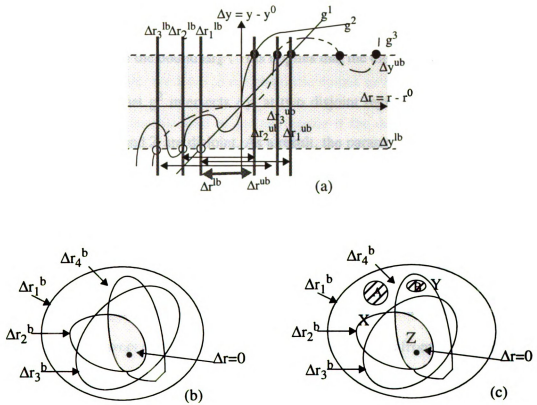


Figure 4.8 Examples for the definition of parameter deviation bounds: (a) in 1-dimension; and (b) & (c) in 2-dimension.

determine the parameter deviation bound Δr^b in the region Z. Suppose that g^2 intersects Δy_i at two disjoint regions A and X, where X defines $\Delta r_2{}^b$, and A and Y are also disjoint. Therefore, when a parameter deviation occurs in region A, it may be tested as fault-free with the application of the test vector u^2, but it will be identified as faulty by u^4 because region A lies outside of the bound $\Delta r_4{}^b$. This implies that the circuit is still testable. On the other hand, suppose that g^2 intersects Δy_i at two disjoint regions B and X, where B is included by Y, and B and Z are disjoint. As a result, the parameter deviations in region B are located outside of $\Delta r_3{}^b$ and thus they can be detected as faulty when u^3 is applied. Unfortunately, u^3 was not selected as a test vector. Thus, the fault can not be detected, and u^3 should be included as a test vector. This implies that, if g intersects $\Delta y_i{}^b$ more than one regions bounded by all test vectors, then those inputs whose corresponding parameter deviation bounds covers only the region with $\Delta r=0$, but disjoints from others, should also be selected as the test vectors. This concludes that the circuit is easily testable if the g functions intersects $\Delta y_i{}^b$ at most one region formed by the selected test vectors, and the following testability rule for the general case r results.

A designed circuit is easily testable if g intersects $\Delta y_i{}^b$ in at most one region bounded by all test vectors, for all Δy_i.

Note that the rule allows more than one regions bounded by a vector, or many vectors, but not all the vectors.

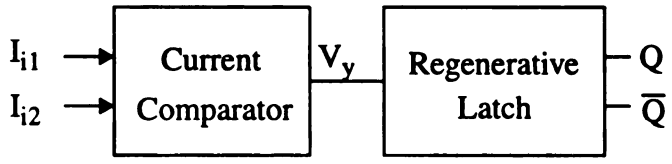
4.2.2 Discussion

The developed testability rule enables us to design an easily testable analog circuit. If a circuit design fails to satisfy the rule, it will be very difficult to define the parameter deviation bounds for test generation and fault coverage evaluation. For example, as shown in Figure 4.8(a), if g^2 intersects Δy_i^{ub} in more than one points, then u^2 cannot be used as the test vector. Therefore, we have to re-design the circuit to meet the testability design rule. However, u^2 can be still used as the test vector if the design specification can be modified, i.e., Δy_i^{ub} can be lowered so that g^2 intersects Δy_i^{ub} at only one point. This implies that the testability rule may play an important role for the design trade-off of testability and the design specification.

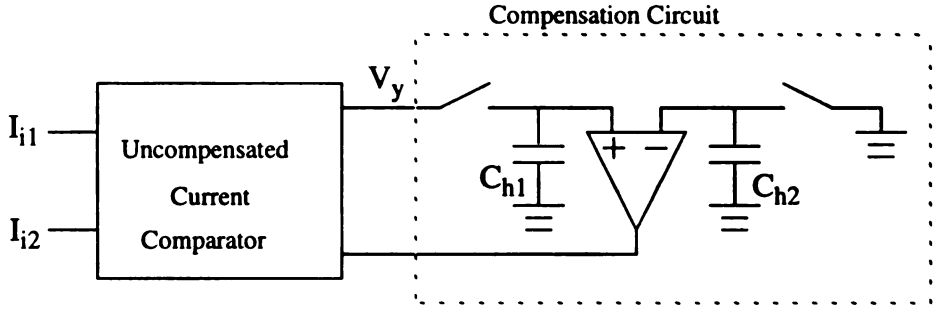
4.3 High-Accuracy Built-In Tester

The distortion caused by the interface between internal circuitry and external test equipment is always a severe problem in the IC testing. One solution to this problem is using the built-in tester (BITER). The BITER not only relieves the distortion, but also simplifies the test generation process. In addition, with a low cost BITER, the expensive ATE (automatic test equipment) may not be needed.

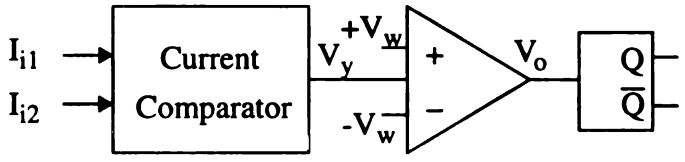
The BITER can be designed using a high accuracy CMOS current comparator. The objective of a current comparator, as shown in Figure 4.9(a), is to check if the difference of two input currents I_{i1} and I_{i2} are sufficiently small [52]. A corresponding voltage level V_y with respect to the current difference $I_x=I_{i1}-I_{i2}$ is generated. Thus, the current comparator is effectively a current-to-voltage (I-V) comparator. The generated voltage level is then applied to a regenerative latch to determine the digital output [52]. The original CMOS



(a)



(b)



(c)

Figure 4.9 Current comparators: (a) in [52]; (b) in [60]; and (c) proposed design.

current comparator was proposed in [53] using current mirrors to construct the input and output stages. For high-speed current-mode circuits, positive feedback structures [54,55] and prebiasing techniques [56,57] have been applied to improve speed performance. One of the most critical parameters which limits current comparator performance is the offset which affects the accuracy of comparators. The first offset compensated current comparator was presented in [58] and generalized in [59,60] for accuracy improvement. Figure 4.9(b) shows an offset compensated current comparator which is comprised of a uncompensated comparator and a compensation circuit [60]. It uses an amplifier and two holding capacitors C_{h1} and C_{h2} for the compensation circuit. Both switches in the compensation circuit are first closed to form a feedback loop making V_y equal to the offset voltage of the amplifier. When both switches are opened, both holding capacitors memorize the bias point. In addition, the use of switches and capacitors alleviates the charge-injection error effect [60], but both capacitors must be identical. Otherwise, the errors due to mismatched components may be amplified by the amplifier and result in a large offset voltage. To avoid the error amplification and still reducing the charge-injection errors, an alternative design is developed. The comparator is used as a BITER of the SI circuits and thus it is expected to have high accuracy with a moderate speed and can be operated in a low-voltage/low-power environment.

Section 4.3.1 describes the design and operation of the developed high-accuracy current comparator. The simulation results are presented in Section 4.3.2, and the performance analysis of the comparator as a BITER is given in Section 4.3.3. Finally, the advantages of using BITER are discussed in Section 4.3.4.

4.3.1 Design and Operation

Figure 4.9(c) shows the block diagram of the developed BITER which is comprised of a current comparator, a voltage window comparator, and a digital latch. Suppose the comparator is designed in such a way that a corresponding voltage level V_y, $-V_w \le V_y \le V_w$, is generated for any input I_x, $-I_{tol} \le I_x \le I_{tol}$. Then, a simple voltage window comparator with a pair of symmetric the threshold voltages, V_w and $-V_w$, can be used. An ideal current comparator, or I-V comparator, has a linear relationship between I_x and V_y as

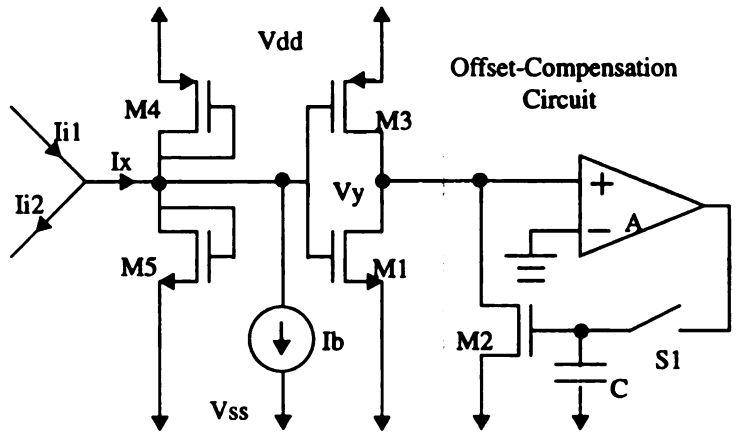
$$V_y = I_x \; r_k \tag{4.11}$$

where r_k is a constant transresistance. In practice however, the accuracy may be affected by: (a) the offset current due to mismatched components in the current comparator; and (b) the nonlinearity of r_k. The offset current may cause an offset voltage, V_{ofs}, in the output of the current comparator, while the nonlinearity of r_k leads to a nonlinearity quality $V_{nl}(I_x)$ which is a function of I_x. Thus, the output voltage V_y in (4.11) can be re-written as

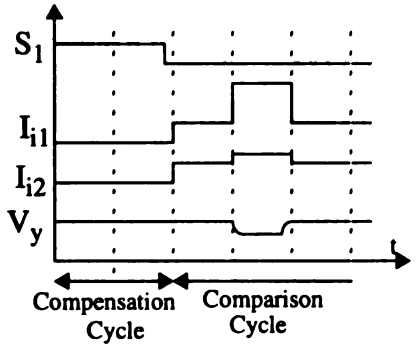
$$V_y = I_x \; r_k + V_{ofs} + V_{nl}(I_x) \tag{4.12}$$

As a result, the accuracy of a current comparator can be improved by reducing the terms V_{ofs} and $V_{nl}(I_x)$. The proposed comparator attempts to achieve very small V_{ofs} and moderate $V_{nl}(I_x)$.

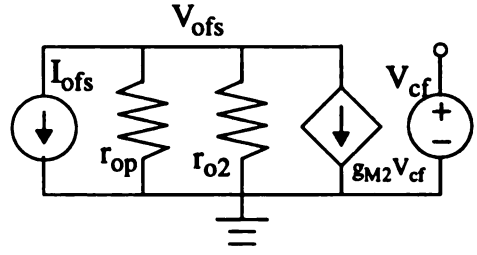
Figure 4.10(a) shows the circuit diagram of the proposed current comparator, where the uncompensated comparator is constructed by the transistors M_1, M_3, M_4, and M_5. The



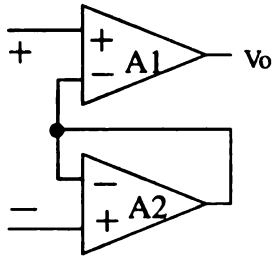
(a)



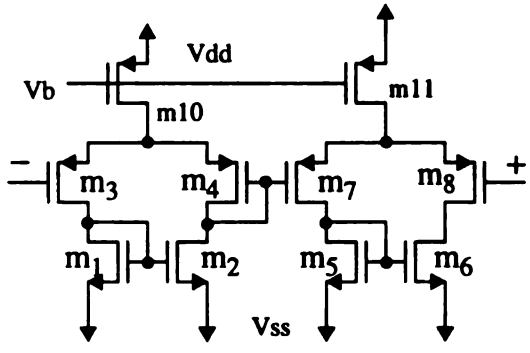
(b)



(c)



(d)



(e)

Figure 4.10 Current comparator: (a) schematic diagram; (b) switching sequence; (c) small signal equivalent circuit when S_1 is off; and (d) & (e) offset-compensated amplifier.

input stage, comprised of the diode-connected transistors M_4 and M_5, results in a very small input resistance and a near zero input bias voltage. To maintain large sensitivity of V_y with respect to I_x, by (4.11), a large transresistance r_k is required. In Figure 4.10(a), the transresistance $r_k=r_{o1}||r_{o3}$, where r_{o1} and r_{o3} are the output resistances of M_1 and M_3, respectively. Note that an output resistance r_{oi} is approximately inversely proportional to the drain current I_{di}, i.e., $r_{oi} \approx 1/(\lambda I_{di})$, where λ is channel modulation coefficient. Therefore, a large transresistance r_k can be obtained by keeping small drain currents I_{d1} and I_{d3}, for M_1 and M_3. The offset compensation circuit is comprised of a current copier with a negative-feedback amplifier [18-20,22] and a bias current source I_b. The bias current I_b is equal to the current difference $(I_{d1}-I_{d3})$. The current copier includes a transistor M_2, an amplifier A, a holding capacitor C, and a switch S_1.

Figure 4.10(b) illustrates the switching sequence of S_1, the application of input currents, and the resultant output voltage of the proposed current comparator. The circuit takes the first two clock cycles for the offset-compensation process, where S_1 is closed and $I_{i1}=I_{i2}=0$. At the end of the offset compensation process, the current I_b, $=I_{d1}-I_{d3}$, is held in M_2, S_1 is opened, and V_y is biased with the offset voltage V_{ofs} which is the sum of V_a, the offset of the amplifier A, and V_{ch}, the offset voltage caused by the charge-injection errors. After the offset compensation process is completed, the comparison process takes place, where two input currents I_{i1} and I_{i2} are applied. As illustrated in Figure 4.10(b), two identical input currents, $I_{i1}=I_{i2}$ are applied to the comparator in the third cycle, and a zero-valued V_y results. On the other hand, two inputs currents $I_{i1} > I_{i2}$ are applied in the forth cycle, a negative V_y is obtained.

To analyze the offset voltage of the comparator, a small signal equivalent circuit is

shown in Figure 4.10(c), where S_1 is opened, and only those effects caused by the offset current and charge-injection errors are considered. In Figure 4.10(c), $r_{op}=r_{01}||r_{03}$, I_{ofs} is the equivalent offset current caused by the offset voltage of the amplifier A, and V_{cf} is the deviation of the voltage across the holding capacitor C due to the charge-injection error effect. Therefore, the offset voltage is expressed as

$$V_{ofs} = V_a + V_{ch}, \tag{4.13}$$

where

$$V_a = (r_{op}||r_{o2})I_{ofs} \text{ and } V_{ch} = (r_{op}||r_{o2})(g_{M2}V_{cf}). \tag{4.14}$$

To reduce both V_a and V_{ch}, the current copier should be designed as follows. The negative feedback amplifier A is implemented by two identical amplifiers, as shown in Figure 4.10(d). The amplifier A2 forms a unit-gain buffer which produces the offset voltage V_a to cancel that produced by the amplifier A1. Both amplifiers are realized by differential pairs, as shown in Figure 4.10(e). On the other hand, the term V_{ch} can be decreased by reducing g_{M2}. Since $g_{M2}=\sqrt{2\beta I_{d2}}$, where β and I_{d2} are the gain factor and drain current of M_2, respectively, g_{M2} is reduced if a small I_{d2} is used. In Figure 4.10(a), the drain current I_{d2} is determined by the biased current I_b. In fact, I_{d2} is much smaller than both I_{d1} and I_{d3}, and thus the output resistance r_{o2} is very large. In Figure 4.9(b), a pair of switch/capacitor was used in [60] to reduce the charge-injection error effect. But, the error due to mismatched components may be amplified. In this implementation, the switch/capacitor circuit is moved to the output of the amplifier, and thus the charge-injection error effect will not be amplified. Since the current copier is used as the compensation circuit, no well-matched

components are needed.

Finally, the term $V_{nl}(I_x)$ in (4.12) may be increased rapidly if both transistors M_1 and M_3 are operated towards the linear region. Therefore, to keep $V_{nl}(I_x)$ reasonably small, both transistors must be operated in the saturation region. This can be achieved by appropriately choosing the threshold voltage, V_w, of the window comparator. Note that the threshold voltage V_w should be smaller than both the threshold voltages of NMOS and PMOS transistors.

4.3.2 Simulation Results

The current comparator has been designed and simulated by *Pspice* with the *MOSIS SCN* 2μm CMOS process parameters and 2V supply voltage. The transistor dimensions for current comparator and the amplifier in Figures 4.10(a) and 4.10(e) are listed in Figures 4.11(a) and 4.11(b), respectively. The drain currents and the bias current in Figure 4.10(a) are assigned as: I_{d1}=0.9μA, I_{d2}=0.1μA, I_{d3}=1μA, and I_b=0.1μA. Figure 4.11(c) shows the circuit layout generated by the layout editor, *Magic*. The layout size is approximately $0.01mm^2$.

As mentioned, S_1 in Figure 4.10(a) is closed during the offset compensation process. The current copier memorizes the bias current I_b and sets V_y to the offset voltage V_{ofs}. Figure 4.12(a) plots the transient responses of the comparator. Results show that the circuit, in the offset compensation process, is settled within 0.1% of accuracy in nearly 1.8μs, where the voltage V_y is settled at about V_{ofs}=10μV. Note that the offset voltage V_{ofs} is contributed only by V_a. In other words, the offset voltage of the amplifier is V_a=10μV. Switch S_1 is then opened at 2.5μs in this simulation, the voltage V_y is changed due to

Parameter values for
Current Comparator

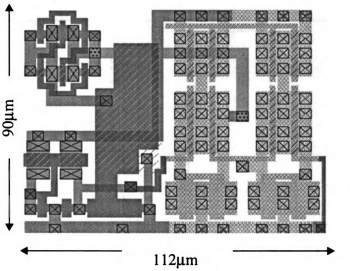
M_1,M_5	3/3
M_3,M_4	8/5
M_2	3/20
C	0.5pf
I_b	0.1μA
I_{d3}	1μA
V_{dd},V_{ss}	+1V, -1V

(a)

Parameter values for
Offset-Compensated Amplifier

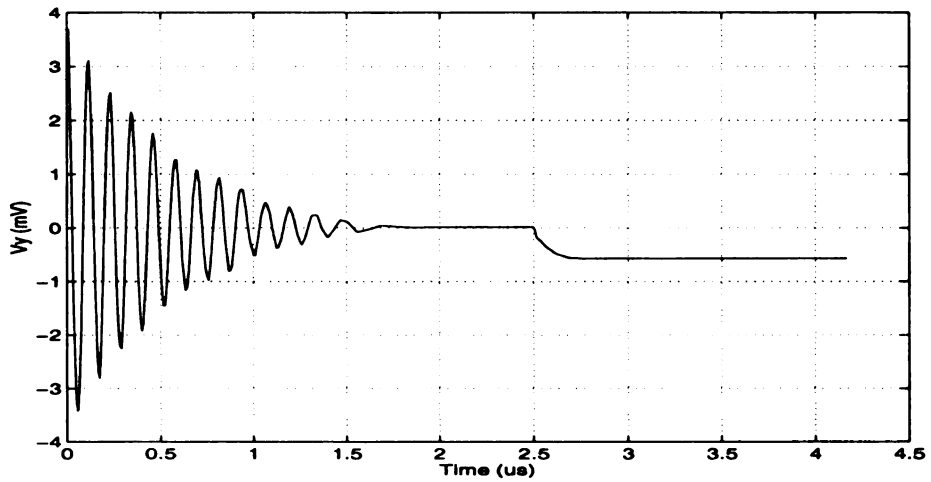
m_1,m_2,m_5,m_6	13/5
m_3,m_4,m_7,m_8	25/2
m_{10},m_{11}	36/2
I_{d11}	4μA
V_{dd},V_{ss}	+1V, -1V

(b)

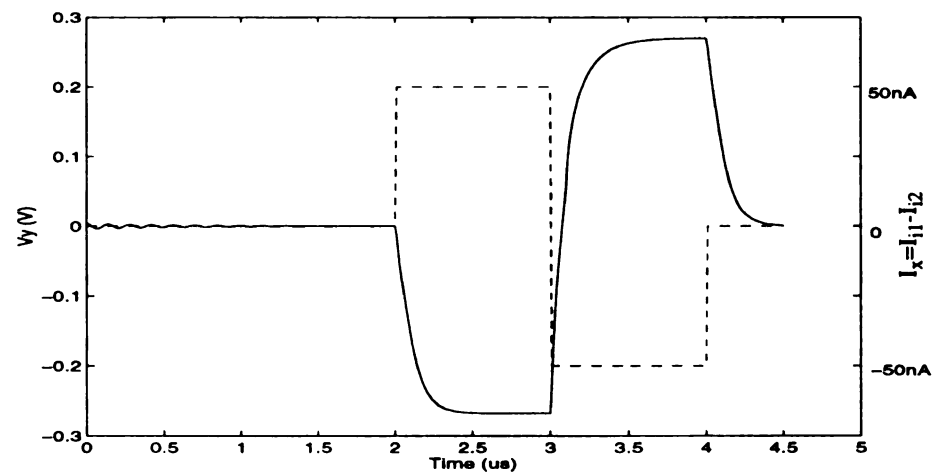


(c)

Figure 4.11 Proposed current comparator: (a) parameter values of Figure 4.10(a); (b) parameter values for Figure 4.10(e); and (c) physical layout.



(a)



(b)

Figure 4.12 Transient responses: (a) during the compensation process; and (b) during the comparison process.

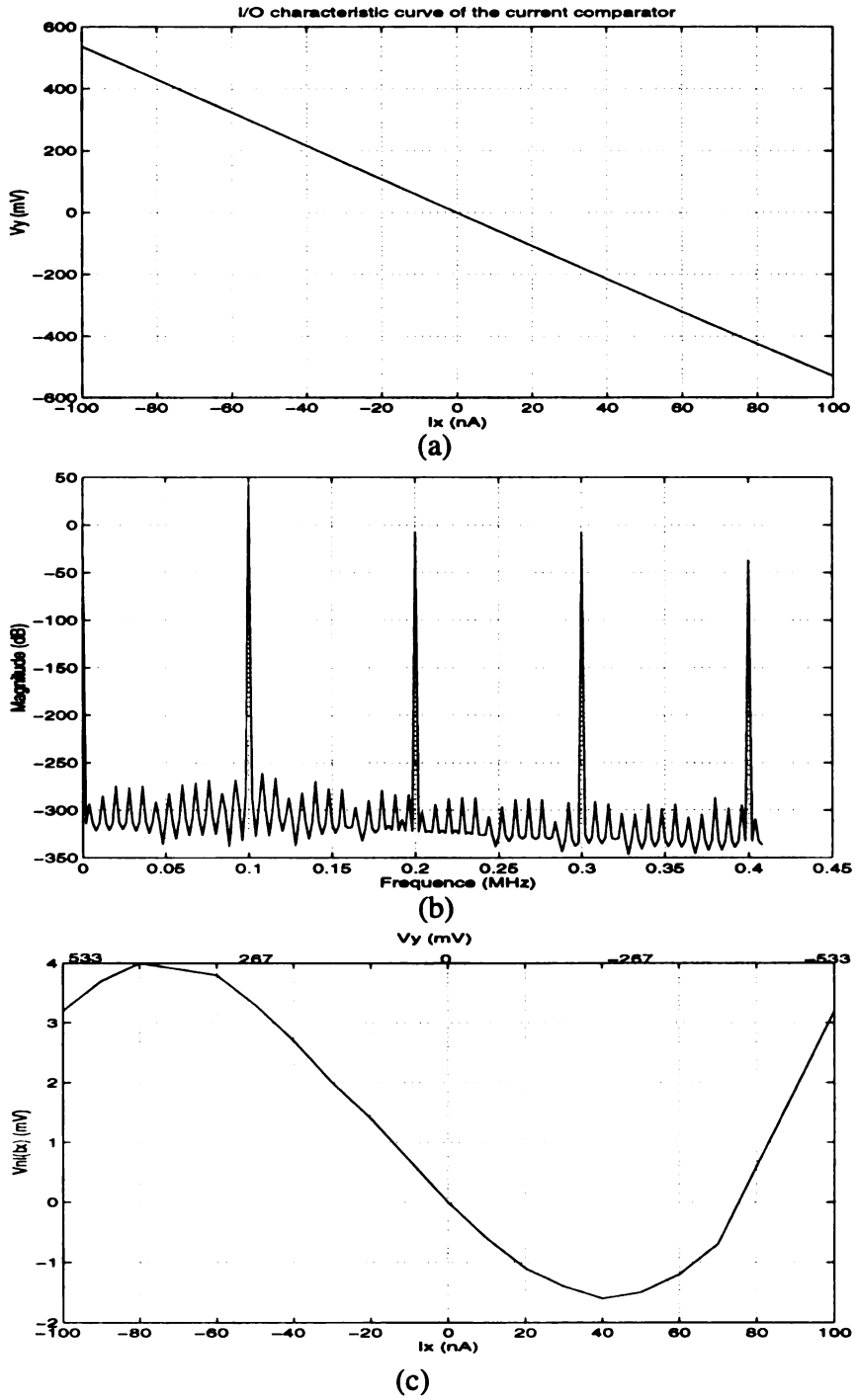


Figure 4.13 Simulation results: (a) I_x-V_y characteristic curve; (b) harmonic distortion; and (c) nonlinearity element $V_{nl}(I_x)$ vs I_x & V_y.

charge-injection errors. As shown in Figure 4.10(a), V_y is about 0.6mV. Figure 4.12(b) plots the transient responses of the comparator during the comparison process. Since the circuit, in the offset compensation process, can be settled at 1.8μs, here the input currents are applied after 2μs when Switch S_1 is opened. The plot shows that, as indicated by the dotted lines, I_x=50nA is applied in the third cycle, and I_x=-50nA is applied in the forth cycle. Results show that it takes about 600ns for V_y to settle.

Figure 4.13(a) plots V_y with respect to I_x ranged from -100nA to 100nA, and the transresistance $r_k=(V_y/I_x)\approx-5.33\text{x}10^6\Omega$. Consequently, the equivalent offset current $I_{ofs}=V_{ofs}/r_k=$ (0.6m)/5.33x10^6, i.e., $I_{ofs}\approx$0.1nA. The harmonic distortion has also been analyzed with the input difference current I_x, a sinusoidal waveform with a 100nA peak-to-peak amplitude, and the simulation results, as plotted in Figure 4.13(b), show that an attenuation of 55dB results on second and third harmonics. Figure 4.13(c) plots the nonlinearity element $V_{nl}(I_x)$ with respect to I_x ranged from -100nA to 100nA. Results show that a maximum $V_{nl}(I_x)$=4mV occurs when I_x=-80nA, or, equivalently, by Figure 4.13(b), the maximum $V_{nl}(I_x)$=4mV occurs when V_y=440mV.

In summary, simulation results show that the offset voltage of the amplifier in Figure 4.10(e) is V_a=10μV and the equivalent offset current is I_{ofs}=0.1nA. The maximum $V_{nl}(I_x)$=4mV occurs when I_x=-80nA, or V_y=440mV. The simulation result has shown that the proposed comparator achieves high accuracy and can be operated in low-voltage (V_{dd}-V_{ss}=2V supply voltage) environment. The power dissipation is only 20μW. However, the circuit takes about 600ns for V_y to settle which is rather slow, but it is sufficient for the built-in tester application.

For built-in tester application, the threshold voltage V_w is determined by the

predetermined tolerable current I_{tol}. For example, if I_{tol}=40nA, by Figure 4.13(a), we choose V_w=213.2mV. As a result, $-V_w \le V_y \le V_w$ for all I_x, $-I_{tol} \le I_x \le I_{tol}$. $V_y=V_w$ if $I_x=-I_{tol}$, and $V_y=-V_w$ if $I_x=I_{tol}$. Let $V_{nl}^+=V_{nl}(-I_{tol})$ and $V_{nl}^-=V_{nl}(I_{tol})$. In this case, by Figure 4.13(c), V_{nl}^-=-1.5mV and V_{nl}^+=2.6mV. Since V_{ofs}=-0.6mV, the maximum and minimum values of V_y are

$$V_{y(max)}=V_w+V_{ofs}+V_{nl}^+=215.2\text{mV}, \text{ and } V_{y(min)}=-V_w+V_{ofs}+V_{nl}^-=-215.3\text{mV}.$$

Therefore, the threshold voltages of the window comparator are chosen by V_1=215.2mV, while V_2=-215.3mV. Similarly, if I_{tol}=80nA, then we choose $V_1=V_{y(max)}$= 429.8mV and $V_2=V_{y(min)}$=--426.4mV, where V_{nl}^-=0.6mV and V_{nl}^+=4mV. On the other hand, for I_{tol}=20nA, we choose $V_1=V_{y(max)}$=104.6mV and $V_2=V_{y(min)}$=-108.3mV.

In the design of a window comparator, a comparator with symmetric threshold voltages, i.e., $V_1=-V_2$, is much easier than that with non-symmetric ones. Since the terms $(V_{ofs}+V_{nl}^+)$ and $(V_{ofs}+V_{nl}^-)$ are relatively smaller than V_w and $-V_w$, respectively, for design simplicity, we may choose $V_1=V_w$ and $V_2=-V_w$ as the threshold voltages of the window comparator. However, with such an implementation, the window comparator may produce incorrect results in the following ranges $[V_w, V_{y(max)}]$ and $[-V_w, V_{y(min)}]$. Since V_w, $(V_{ofs}+V_{nl}^+)$, and $(V_{ofs}+V_{nl}^-)$ are determined by I_{tol}, hence the probability that V_y lies in those ranges depends upon I_{tol} and the distribution of V_y is similar to that of I_x with a scalar factor r_k. The detail discussion is presented in the next section.

4.3.3 Performance Analysis

For design simplicity, the threshold voltages of the window comparator are chosen as $V_1=V_w$ and $V_2=-V_w$. For a given I_{tol}, the voltage V_w is chosen from the plot in Figure 4.13(a). For the ideal case that the relation between I_x and V_y is linear, then $-V_w \le V_y \le V_w$ for all I_x, $-I_{tol} \le I_x \le I_{tol}$. Therefore, the window comparator with the threshold voltages $V_1=V_w$ and $V_2=-V_w$ determines the result correctly. On the other hand, when the offset voltage and nonlinearity of the current comparator are taken into consideration, the window comparator may not always provide correct comparison in the ranges $[V_w, V_{y(max)}]$ and $[-V_w, V_{y(min)}]$, where $V_{y(max)}=V_w+V_{ofs}+V_{nl}^+$ and $V_{y(min)}=-V_w+V_{ofs}+V_{nl}^-$. More specifically, given a current I_x, $I_x>I_{tol}$, its corresponding V_y may be $V_y < V_{y(min)}$ and $V_y \ge -V_w$, i.e., V_y lies in $[-V_w, V_{y(min)}]$. Since $V_y < V_{y(min)}$, or $I_x>I_{tol}$, a "fail" comparison should be resulted. However, because V_y lies in $[-V_w, V_{y(min)}]$, the window comparator will misjudge the result and a "pass" comparison will result. Similarly, given a current I_x, $I_x \le I_{tol}$, its corresponding $V_{y \text{ may lie in}}$ $[V_w, V_{y(max)}]$. A "pass" comparison may be misjudged by the window comparator and a "fail" comparison results. In other words, some comparison results are misjudged due to the choice of the threshold voltage of the window comparator. This section is to analyze the quality of the built-in tester which is constructed by the circuit shown in Figure 4.9(c). We define a testing confidence of the built-in tester as the probability that the comparison results are reliably determined. Thus, this section discuss the testing confidence of the proposed built-in tester with respect to the selected current tolerance.

Assume that the probability density function (pdf) of I_x is Gaussian with a zero

mean, i.e., $E(I_x)=0$. By (4.12), the pdf of V_y is also a Gaussian if the nonlinearity term $V_{nl}(I_x)$ is very small compared with $I_x r_k$. (The statement is true and can be verified from Figures 4.13(a) and 4.13(c)) Therefore, if the term $V_{nl}(I_x)$ is omitted, the mean of the distribution for V_y is

$$E(V_y) = r_k \; E(I_x) + V_{ofs} = V_{ofs} \tag{4.15}$$

Figure 4.14(a) shows the Gaussian distribution for $V_y \sim N(V_{ofs}, \sigma^2)$, where σ is its standard deviation.

By the definition, the testing confidence of the built-in tester is expressed as follows,

$$P_{TC} = 1 - \left[\int_{-V_w}^{V_{y(min)}} \frac{1}{\sqrt{2\pi}\sigma} \exp\left(-\frac{(V_y - V_{ofs})^2}{2\sigma^2}\right) dV_y \right.$$

$$\left. + \int_{V_w}^{V_{y(max)}} \frac{1}{\sqrt{2\pi}\sigma} \exp\left(-\frac{(V_y - V_{ofs})^2}{2\sigma^2}\right) dV_y \right] \tag{4.16}$$

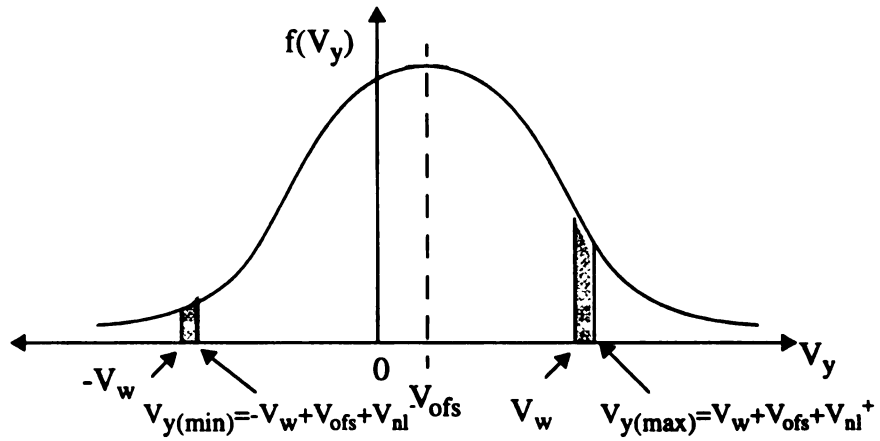
With the standardization, the testing confidence can be re-written as

$$P_{TC} = 1 - [\Phi((-V_w+V_{nl}^-)/\sigma)-\Phi((-V_w-V_{ofs})/\sigma)]$$

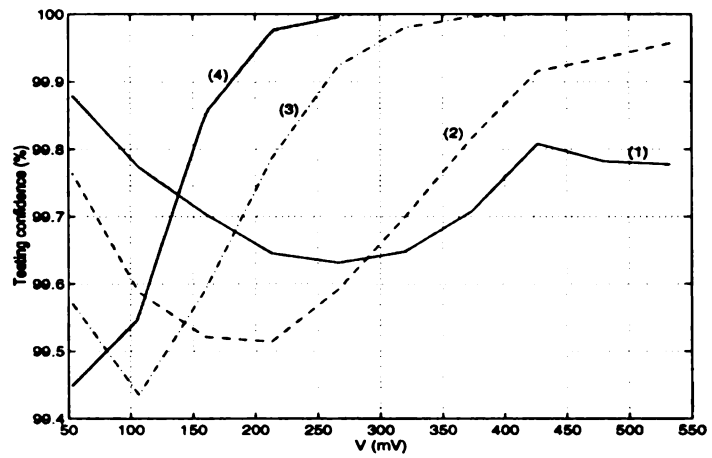
$$- [\Phi((V_w+V_{nl}^+/\sigma)-\Phi((V_w-V_{ofs})/\sigma)] \tag{4.17}$$

where

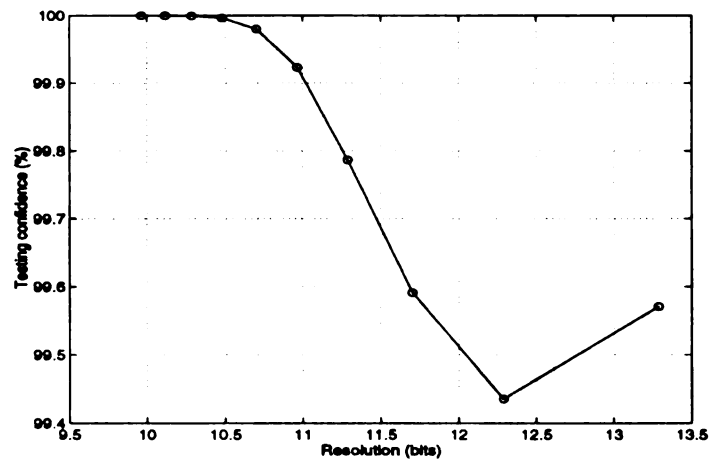
$$\Phi(x) = \int_{-\infty}^{x} \frac{1}{\sqrt{2\pi}} \exp\left(-\frac{y^2}{2}\right) dy \tag{4.18}$$



(a)



(b)



(c)

Figure 4.14 Performance analysis: (a) Gaussian distribution of V_y; (b) statistical confidence vs. window threshold voltage; and (c) statistical confidence vs. resolution.

Figure 4.14(b) plots the testing confidences for various standard deviations: (1) σ=0.4264V, (2) σ=0.2132V, (3) σ=0.1066V and (4) σ=0.071V, where V_{ofs}=-0.6mV. From Figure 4.13(c), V_y=0.4264V is equivalent to I_x=80nA. The simulation results plotted in Figure 4.14(b) may be interpreted as follows: When $V_w \approx 0$, the nonlinearity element is near zero, i.e., $(V_{ofs}+V_{nl}^{+}) = (V_{ofs}+V_{nl}^{-}) \approx V_{ofs}$. Thus, as σ increases, the total shaded areas decrease and the testing confidence increases. As V_w increases, the increase of nonlinearity element $V_{nl}(I_x)$ causes that the total shaded areas increase and the testing confidence decreases for each σ. Our empirical results show that the testing confidence keeps decreasing until $V_w \approx \sigma$, for small σ. The plots also show that, when V_w > 300mV, the testing confidence increases as σ decreases. As shown in the curve (4), σ=0.071V, with V_w=300mV, the testing confidence can reach almost 100%.

Since the choice of V_w is determined by the given I_{tol}, Figure 4.14(c) plots the relationship between the testing confidence and the testing resolution for the testing resolution is defined as the number of bits that represent the ratio I_{tol}/I_{max}, where I_{max} be the maximum difference current applied to the built-in tester, i.e., $I_{max}=I_{x(max)}$. Mathematically, the number of bits, b, is

$$b = \lceil \log_2(I_{max}/I_{tol}) \rceil \qquad (4.19)$$

For example, if I_{max}=100μA and I_{tol}=40nA, then, by (4.19), the resolution is b=12 bits. For I_{tol}=20nA, the testing resolution is 13 bits. Therefore, given a tolerance current I_{tol}, the threshold voltage V_w of the window comparator is chosen as

$$V_w = I_{tol} r_k = (I_{max} r_k)/(2^b) \tag{4.20}$$

In Figure 4.14(c), σ=0.1066V, I_{max}=100μA, and r_k=5.33x10^6. If b=11, by (4.20), the threshold voltage V_w=260.2mV is chosen. By Figures 4.14(b) and 4.14(c), the testing confidence is over 99.9%.

4.3.4 Built-In Tester and Test Sequence

The high-accuracy current comparator can be used as a built-in current tester. Consider the ADC in Figure 4.15(a) which is a simplified version of the ADC in Figure 3.4, where the digital part is included. Figure 4.15(b) illustrates the implementation of the current tester to the ADC, where the voltage window comparator, WCP, is realized as illustrated in Figure 4.15(c). Two multiplexers X1 and X2 are used in WCP. During the normal operation, X1 and X2 are switched to Ground and V_{SS}, respectively, and the output of WCP is set to a "1" if $V_y > 0$, and to a "0" otherwise, while they are set to V_w and $-V_w$ during the test mode.

As illustrated in Figure 2.3, the ADC achieves a 11 bits resolution and, without a built-in tester, the ADC requires a test sequence which is comprised of 11 same test cycles (Figure 3.5) to detect the faults. In practice however, the test sequence length (number of test cycles) can be reduced significantly if a better comparator or tester with high accuracy is used. Because the ADC in Figure 2.3 is implemented by using a multiply-by-two circuit, the tolerance current I_{tol} will be doubled in each test cycle. That is to say, before the beginning of the test sequence, the original I_{tol} is 2^{-1}LSB; while after one test cycle, I_{tol} becomes 1LSB, and it would be 2LSB after two test cycles. Thus, $I_{tol}=2^{M-1}$LSB after M

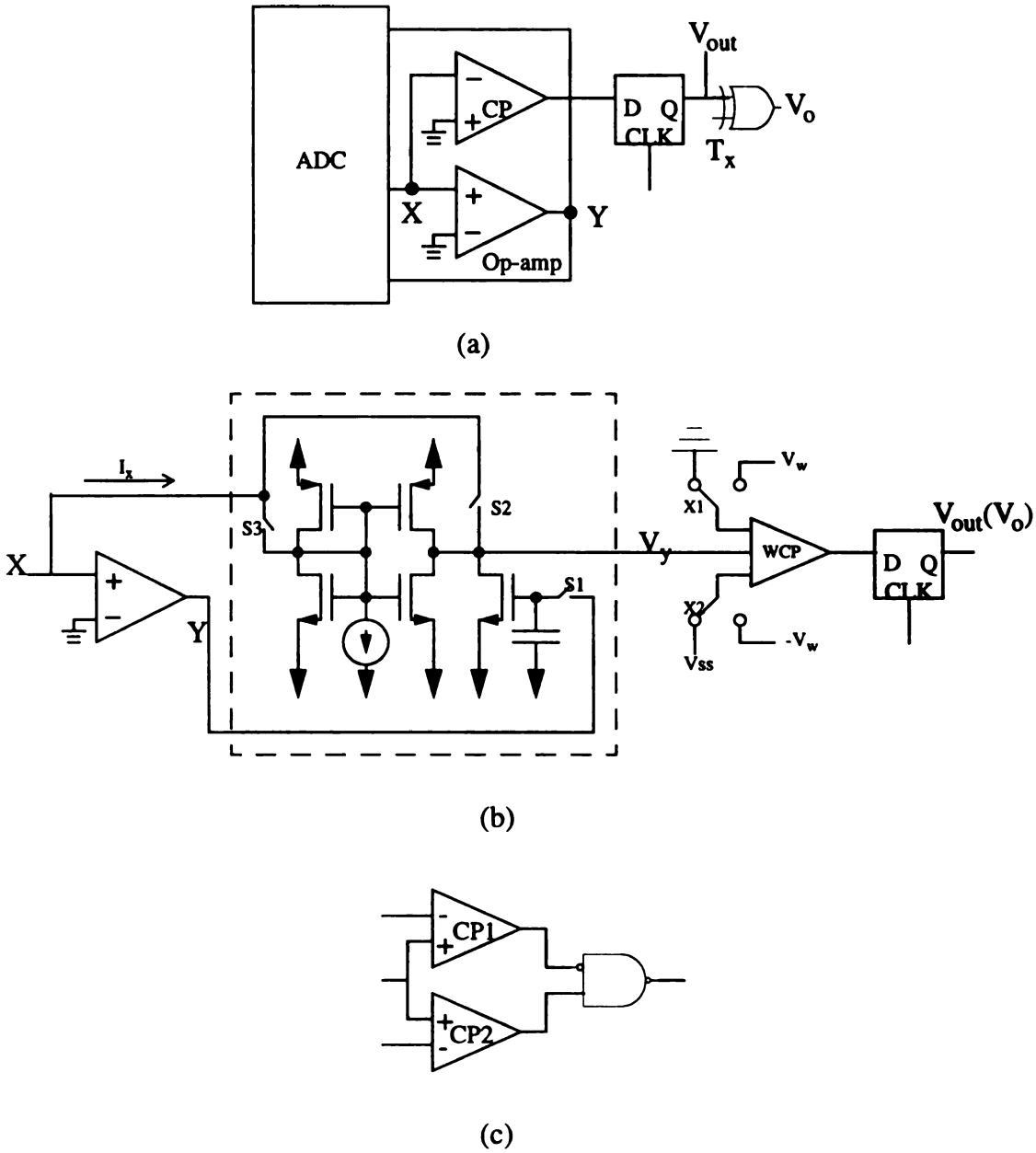


Figure 4.15 ADC with built-in tester: (a) ADC; (b) with built-in tester; and (c) window comparator.

test cycles. Obviously, if we want to decide if the ADC is faulty, i.e. the error current exceeds I_{tol}, just after M test cycles, then a current tester which is capable of detect I_{tol} is needed. By (4.19), a current tester with resolution b is thus required such that $I_{tol}=2^{M-1}LSB=2^{-b}I_{max}$. For the 11-bit ADC in Figure 2.3, I_{max} is equal to I_{ref}. Therefore, $2^{M-1}LSB=2^{-b}Iref=2^{11-b}LSB$. This is to say, b=12-M. Because the test sequence of the ADC has 11 test cycles(M=11), a comparator (or tester) with resolution of only 1 bit (b=1) can be used. If a shorter test sequence, i.e. smaller M, is wanted, then a tester with higher resolution, i.e. larger b, is needed. In the most extreme case, if we want to eliminate all the test cycles in Figure 3.5 (M=0) and test the building blocks, current copiers, directly, then a current tester with 12-bit resolution is required. According to the performance analysis in Section 4.3.3, the proposed high-accuracy current tester can provided 12-bit resolution (with V_w equal to 130mV, by (4.20)) with test confidence over 99.5%. Thus, the ADC which uses the proposed built-in tester (Figure 4.15(b)) can effectively achieve zero test sequence length. Although the comparator in Figure 4.10(a) requires a test sequence length of 11 test cycles, it contains only 16 transistors. The ADC using proposed built-in current tester in Figure 4.10(b) needs no test sequence, but it contains 36 transistors. Thus, there exists a design trade-off between comparator circuit complexity and the test length.

Chapter 5

HIERARCHICAL TESTABILITY DESIGN SYSTEM

Based on the hierarchical fault macromodeling process, this chapter presents a hierarchical testability design system, namely, PETOMIC (Packages for Enhancing Testability Of Mixed-signal Integrated Circuit). The system has been developed and implemented in C language, Pspice, Matlab [62,63,64]. The system includes two routines (Figure 5.1), CLG_Routine and MLG_Routine. The former generates a cell library, as discussed in Figure 4.3, while the latter builds a macro library, as illustrated in Figure 4.4. Given a reasonably large analog/mixed-signal circuit, the user first partitions the circuit into smaller circuits and employs PETOMIC to generates both cell library and macro library including all primitive cells and macros contained in that circuit.

Section 5.1 describes the system development for the routine generating the cell library with a detailed example, while Section 5.2 presents that for the routine for generating macro library.

5.1 CLG_Routine

CLG_Routine, as show in Figure 5.1, is a routine that generates the cell library. The routine contains three major subroutines: DG (Defect Generator), FBE (Fault Behavior Evaluator), and FTCE (Fault Type Classification Environment). The above three

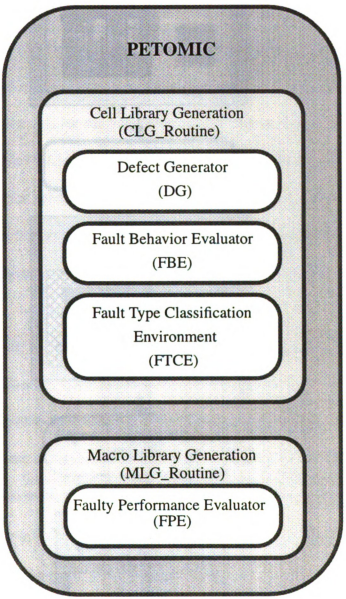


Figure 5.1 Structure of PETOMIC.

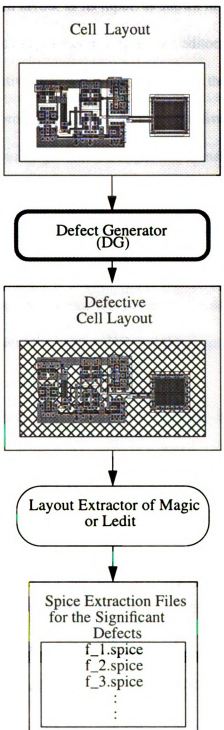


Figure 5.2 The use of defect generator in cell library establishing.

subroutines implements the three steps in Figure 4.3 for generating a cell library.

The DG takes a cell layout as its input, as shown in Figure 5.2, produces defective cell layouts. Either Magic [65] or Ledit [66], layout editors, is used to extract Spice files from both good and defective layouts. In this discussion, the Opamp in a current copier is used to demonstrate the procedure. The good and defective Opamp layouts are shown in Figure 5.2. The DG subroutine generates a Spice file, namely, f_0.spice, for the good cell, and Spice files, namely, f_i, for the i-th defective cell layout, where i=1,2,...,n. In this implementation, the file "f_7.spice" indicates the Spice file for the 7-th defective cell layout. Figure 5.3 shows the Spice sub-circuit K, where the middle part is generated from the DG, and both top and bottom portions are added by the user. A Matlab program "dfectgen.m" is used to implement the routine DG and the program must be executed with the Matlab environment.

To evaluate fault behaviors, a set of parameters to be extracted must be prepared. For example, for the Opamp, three parameters, offset voltage, DC gain, and output resistance, will be extracted for evaluating the fault behaviors. The test circuits for extracting parameters are illustrated in Figure 5.4. In Figure 5.4(a), the offset voltage, Vin, is selected when the absolute value of V_o is minimum, where V_{in} is swept from -2.5V to 2.5V. In Figure 5.4(b), the DC gain is obtained by applying an AC signal, v_{in}, with an amplitude 1, and checking the amplitude response of v_o at very low frequency. Finally, in Figure 5.4(c), the output resistance is the value of V_o at very low frequency when an AC current source with an amplitude of 1 is applied to the output of the Opamp with its two inputs grounded. Figure 5.5 presents the Spice files for the circuits setup in Figure 5.4, and it is called "prem.cir".

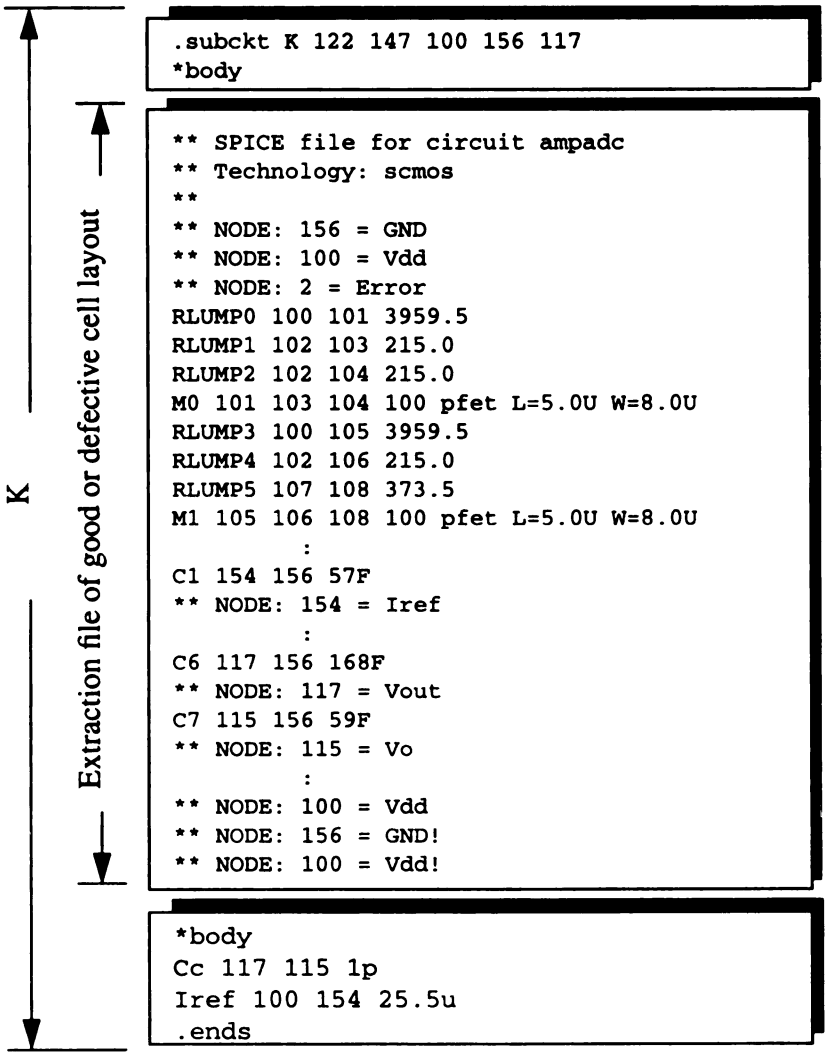
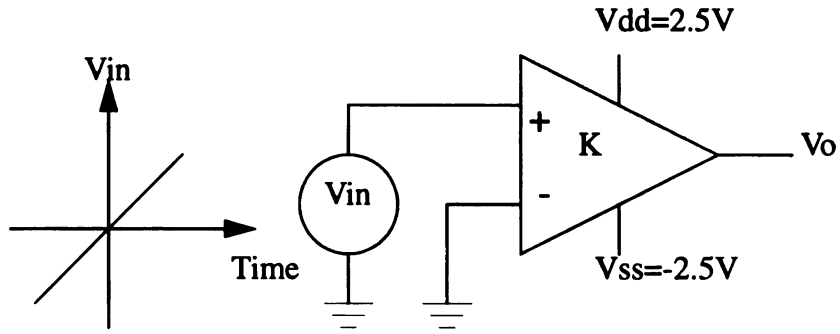
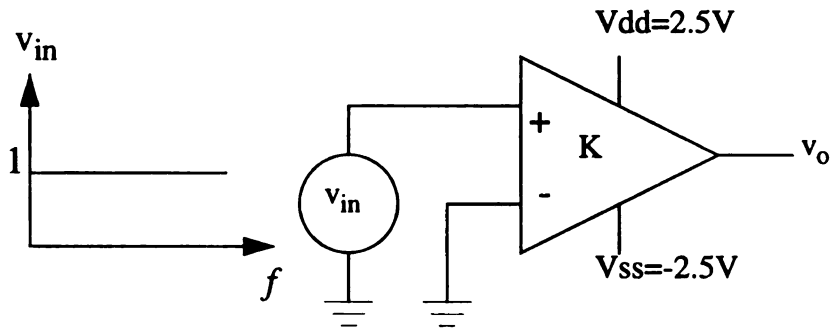


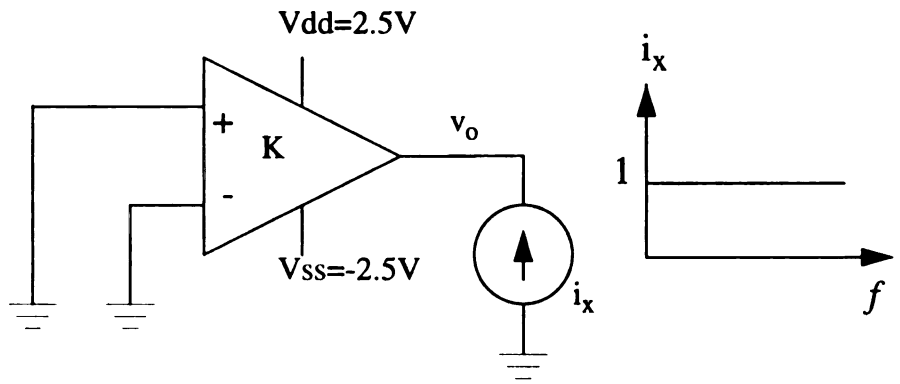
Figure 5.3 Example of extraction file and K.



(a)



(b)



(c)

Figure 5.4 Experiments for extract parameters from cell K, Opamp in this example.

```
* Retrieve Voff
xamp 3 0 1 2 4 K
Vdd 1 0 2.5
Vss 2 0 -2.5
Vin 3 0 dc -2
.Lib K
.dc Vin -2 2 0.01
.print dc v(4)
.Model sv vswitch Ron=4e5 Roff=1e6
+von=2 voff=-2
*parameters: MOSIS 2 micron CMOS process
.model nfet nmos level=2 Ld=.115u TOX=423e-10 NSUB=1.0125225e16
+VTO=.822163 kp=4.893760e-5 gamma=.47 phi=0.6 UO=599.496
+UEXP=5.324966e-3 UCRIT=12714.2 DELTA=3.39718e-5 VMAX=65466.1
+XJ=0.55u lambda=1.991479e-2 NFS=5.66758e11 Neff=1.0010e-2
+NSS=0.0 TPG=1.00 rsh=28.070 CGSO=0.9388e-10 CGDO=0.9388e-10
+cj=1.4563e-4 MJ=0.6 cjsw=6.617e-10 mjsw=0.31
.model pfet pmos level=2 Ld=.18u TOX=423e-10 NSUB=1.421645e15
+VTO=-.776658 kp=1.916950e-5 gamma=.52 phi=0.6 UO=234.831
+UEXP=0.142293 UCRIT=20967 DELTA=1e-6 VMAX=34600.2
+XJ=0.41u lambda=4.921086e-2 NFS=4.744781e11 Neff=1.0010e-2
+NSS=0.0 TPG=-1.00 rsh=45.92 CGSO=1.1957e-10 CGDO=1.1957e-10
+cj=2.4e-4 MJ=0.5 cjsw=3.62e-10 mjsw=0.29
.OPTIONs RELTOL=1E-6.5 pivtol=1e-36 pivrel=1e-36
+CHGtol=1e-13 Abstol=1e-13 VNtol=1e-10 Itl5=0 Itl4=80
+NUMDGT=8 gmin=1e-18
 NOECHO NOMOD NOPAGE
.end
* Retrieve Adc
.xamp 3 0 1 2 4 K
Vdd 1 0 2.5
Vss 2 0 -2.5
vin 3 0 ac 1 dc -0.14
.Lib K
.ac dec 10 1 1k
.print ac v(4)
.Model sv vswitch Ron=4e5 Roff=1e6
+von=2 voff=-2
*parameters: MOSIS 2 micron CMOS process
.model nfet nmos level=2 Ld=.115u TOX=423e-10 NSUB=1.0125225e16
+VTO=.822163 kp=4.893760e-5 gamma=.47 phi=0.6 UO=599.496
```

Figure 5.5 Example of prem.cir.

```
+UEXP=5.324966e-3 UCRIT=12714.2 DELTA=3.39718e-5 VMAX=65466.1
+XJ=0.55u lambda=1.991479e-2 NFS=5.66758e11 Neff=1.0010e-2
+NSS=0.0 TPG=1.00 rsh=28.070 CGSO=0.9388e-10 CGDO=0.9388e-10
+cj=1.4563e-4 MJ=0.6 cjsw=6.617e-10 mjsw=0.31
.model pfet pmos level=2 Ld=.18u TOX=423e-10 NSUB=1.421645e15
+VTO=-.776658 kp=1.916950e-5 gamma=.52 phi=0.6 UO=234.831
+UEXP=0.142293 UCRIT=20967 DELTA=1e-6 VMAX=34600.2
+XJ=0.41u lambda=4.921086e-2 NFS=4.744781e11 Neff=1.0010e-2
+NSS=0.0 TPG=-1.00 rsh=45.92 CGSO=1.1957e-10 CGDO=1.1957e-10
+cj=2.4e-4 MJ=0.5 cjsw=3.62e-10 mjsw=0.29
.OPTIONs RELTOL=1E-6.5 pivtol=1e-36 pivrel=1e-36
+CHGtol=1e-13 Abstol=1e-13 VNtol=1e-10 Itl5=0 Itl4=80
+NUMDGT=8 gmin=1e-18
 NOECHO NOMOD NOPAGE
.end
* Retrieve ro
xamp 3 0 1 2 4 K
Vdd 1 0 2.5
Vss 2 0 -2.5
vin 3 0 -0.14
ix 0 4 ac 1
.Lib K
.ac dec 10 1 10k
.print ac v(4)
.Model sv vswitch Ron=4e5 Roff=1e6
+von=2 voff=-2
*parameters: MOSIS 2 micron CMOS process
.model nfet nmos level=2 Ld=.115u TOX=423e-10 NSUB=1.0125225e16
+VTO=.822163 kp=4.893760e-5 gamma=.47 phi=0.6 UO=599.496
+UEXP=5.324966e-3 UCRIT=12714.2 DELTA=3.39718e-5 VMAX=65466.1
+XJ=0.55u lambda=1.991479e-2 NFS=5.66758e11 Neff=1.0010e-2
+NSS=0.0 TPG=1.00 rsh=28.070 CGSO=0.9388e-10 CGDO=0.9388e-10
+cj=1.4563e-4 MJ=0.6 cjsw=6.617e-10 mjsw=0.31
.model pfet pmos level=2 Ld=.18u TOX=423e-10 NSUB=1.421645e15
+VTO=-.776658 kp=1.916950e-5 gamma=.52 phi=0.6 UO=234.831
+UEXP=0.142293 UCRIT=20967 DELTA=1e-6 VMAX=34600.2
+XJ=0.41u lambda=4.921086e-2 NFS=4.744781e11 Neff=1.0010e-2
+NSS=0.0 TPG=-1.00 rsh=45.92 CGSO=1.1957e-10 CGDO=1.1957e-10
+cj=2.4e-4 MJ=0.5 cjsw=3.62e-10 mjsw=0.29
.end
```

Figure 5.5 (continue)

The FBE takes the Spices files previously generated, as shown in Figure 5.6, as its inputs and generates a list of fault behavior values. The FBE, executed by the program "ifa_fbe.exe", evaluates the fault behaviors from executing the Spice file "prem.cir" with the sub-circuit K, where K is substituted, in turns, by f_0.spice and f_i.spice, for all i. Note that the code ".Lib K" in the "prem.cir" (Figure 5.5) indicates that the sub-circuit K defined above. The resultant fault behaviors are listed in Figure 5.7. Finally, the FTDE, executed by a Matlab program "ifaftde.m", is an environment that defines the fault types, and provides a fault behavior display window, as shown in Figure 5.8, for user to define the fault types. In Figure 5.8, the offset voltage, DC gain, and output resistance are denoted as Parameters A, B, and C, respectively, where the parameter values are the normalized deviation values. Results show that a group of fault behavior values result in a deviation of about -17 on the offset voltage (Parameter A), but almost no deviations on both DC gain (Parameter B) and output resistance (Parameter C). Thus, the fault behaviors are concluded as a fault type, *Offset voltage is too large*, referred to as *Type 1 fault.* Similarly, we can identify the other fault type, *Large offset voltage, small DC gain, and small output resistance*, referred to as *Type 2 fault.*

The resultant cell library information for Opamp indicates that the cell layout area is 21837 $(\mu m)^2$, and 700 defects were injected. Among the 700 defects, there are only 48 significant defects. It also shows that 6 significant defects cause simulation failures during the process of FBE, thus they will lead to hard faults. Among the remaining 42 significant defects, 10 are Type 1 faults, while 32 are Type 2 faults.

Figure 5.9 summarizes the program files, input files, and output files used in the CLG_routine. Two major programs, *ifa_fbe.exe* and *ifaftde.m*, are used and they include

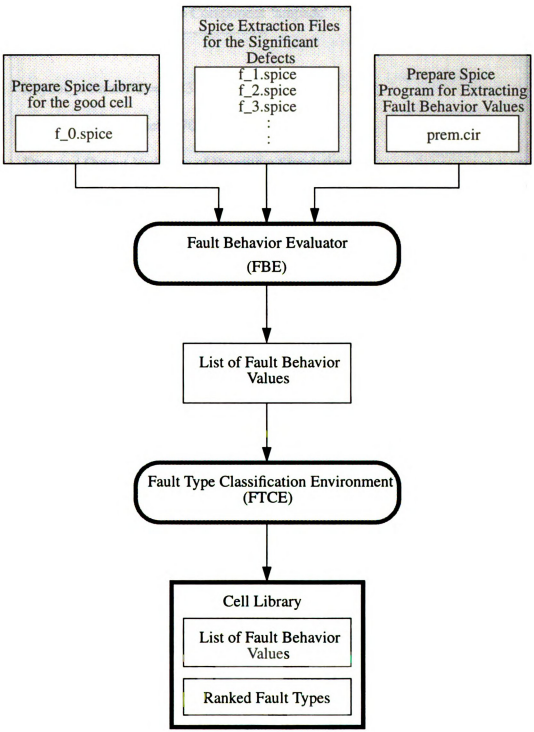


Figure 5.6 The use of fault behavior evaluator and fault type classification environment in cell library establishing.

```
Cell Library for Primitive Component 'ampadc'
---------------------------------------------


Layout_area(um^2)= 21837

N_of_injected_defects= 700

Detected Output Variables of Premitive Simulation #1
      dc ---------> sig1
    v(4) ---------> sig2

Detected Output Variables of Premitive Simulation #2
      ac ---------> sig3
    v(4) ---------> sig4

Detected Output Variables of Premitive Simulation #3
      ac ---------> sig5
    v(4) ---------> sig6



Parameter1= sig2(200)
Norminal value of parameter1= -0.14

Parameter2= sig4(2)
Norminal value of parameter2= 68.093461

Parameter3= sig6(2)
Norminal value of parameter3= 1.573879e+5



List of fault behavior values(normalized deviation):
(1st column: index of defects; last column: norm)

  1  -1.8857143e+01  -1.0000000e+00  -1.0000000e+00   1.8910099e+01

  2  -1.6572788e+01   1.3068817e-02   8.8352408e-03   1.6572795e+01

  3  -1.6572788e+01   1.3068817e-02   8.8352408e-03   1.6572795e+01
```

Figure 5.7 Example of cell library.

4	-1.6572788e+01	1.3068817e-02	8.8352408e-03	1.6572795e+01
5	-1.7586038e+01	-1.0000000e+00	-9.8446606e-01	1.7641936e+01
6	1.6850217e+01	-9.9996792e-01	-9.4990723e-01	1.6906569e+01
8	-1.7580645e+01	-1.0000000e+00	-9.8439981e-01	1.7636556e+01
11	-1.6621526e+01	-4.6783200e-02	-3.2783969e-02	1.6621624e+01
12	-1.6539791e+01	4.7342431e-02	2.8293090e-02	1.6539883e+01
13	1.6833645e+01	-9.9994250e-01	-9.4794733e-01	1.6889941e+01
14	1.6832875e+01	-9.9993934e-01	-9.4777378e-01	1.6889163e+01
15	-6.8232061e+00	-9.4497440e-01	-9.3952527e-01	6.9521094e+00
16	-1.6614704e+01	4.6763521e-03	8.7878420e-03	1.6614707e+01
17	-1.5623640e+01	-9.3104522e-01	-9.3485659e-01	1.5679252e+01
18	1.6720809e+01	-9.9999695e-01	-9.4990989e-01	1.6777597e+01
19	-1.7959396e+01	-1.0000000e+00	-9.8648082e-01	1.8014246e+01
20	-1.7611227e+01	-9.9974363e-01	-9.8412991e-01	1.7667012e+01
21	1.6846133e+01	-9.9994609e-01	-9.4990537e-01	1.6902497e+01
22	1.6855477e+01	-9.9999407e-01	-9.4990906e-01	1.6911813e+01
23	-1.7009515e+01	-9.8954084e-01	-9.6569965e-01	1.7065619e+01
24	-1.6500823e+01	2.2174097e-02	2.7479940e-02	1.6500861e+01
25	-1.6500823e+01	2.2174097e-02	2.7479940e-02	1.6500861e+01
27	1.6855930e+01	-9.9999787e-01	-9.5637415e-01	1.6912629e+01
28	1.6857143e+01	-1.0000000e+00	-1.0000000e+00	1.6916361e+01

Figure 5.7 (continue)

29	-1.6558173e+01	2.5844376e-02	1.7222544e-02	1.6558202e+01
31	1.6857143e+01	-1.0000000e+00	-9.4990993e-01	1.6913474e+01
32	-1.8818706e+01	-1.0000000e+00	5.6125100e+04	5.6125103e+04
33	1.6857143e+01	-1.0000000e+00	-9.4990997e-01	1.6913474e+01
34	1.6857143e+01	-1.0000000e+00	-9.4990997e-01	1.6913474e+01
35	-9.9963657e+00	-9.9980209e-01	-9.6785226e-01	1.0092753e+01
36	-1.6499108e+01	2.5146937e-02	6.5279478e-03	1.6499128e+01
37	1.6857143e+01	-9.9745402e-01	6.3298820e+04	6.3298823e+04
38	-1.8857143e+01	-1.0000000e+00	-1.0000000e+00	1.8910099e+01
39	-1.7112481e+01	-9.9389041e-01	-9.7173330e-01	1.7168840e+01
40	1.6833710e+01	-9.9994276e-01	-9.4796199e-01	1.6890006e+01
41	-1.7611227e+01	-9.9974363e-01	-9.8412991e-01	1.7667012e+01
42	-1.8857143e+01	-1.0000000e+00	-9.8473501e-01	1.8909298e+01
43	1.6833710e+01	-9.9994276e-01	-9.4796199e-01	1.6890006e+01
44	1.6857143e+01	-1.0000000e+00	-9.4990993e-01	1.6913474e+01
45	-1.8818708e+01	-1.0000000e+00	5.6124511e+04	5.6124514e+04
46	-1.7959374e+01	-1.0000000e+00	-9.8648082e-01	1.8014224e+01
47	-1.7398881e+01	-1.0000000e+00	-9.8189994e-01	1.7455234e+01

N_of_significant_defects= 48

N_of_sim_fail= 6

Figure 5.7 (continue)

```
----------------------------------------
Type1 fault: Offset voltage is too large

N_of_type1 fault= 10

  2 -1.657279e+01  1.306882e-02  8.835241e-03  1.657279e+01
  3 -1.657279e+01  1.306882e-02  8.835241e-03  1.657279e+01
  4 -1.657279e+01  1.306882e-02  8.835241e-03  1.657279e+01
 11 -1.662153e+01 -4.678320e-02 -3.278397e-02  1.662162e+01
 12 -1.653979e+01  4.734243e-02  2.829309e-02  1.653988e+01
 16 -1.661470e+01  4.676352e-03  8.787842e-03  1.661471e+01
 24 -1.650082e+01  2.217410e-02  2.747994e-02  1.650086e+01
 25 -1.650082e+01  2.217410e-02  2.747994e-02  1.650086e+01
 29 -1.655817e+01  2.584438e-02  1.722254e-02  1.655820e+01
 36 -1.649911e+01  2.514694e-02  6.527948e-03  1.649913e+01


----------------------------------------
Type2 fault: Large Vofs, small DC gain and small ro

N_of_type2 fault= 32

  1 -1.885714e+01 -1.000000e+00 -1.000000e+00  1.891010e+01
  5 -1.758604e+01 -1.000000e+00 -9.844661e-01  1.764194e+01
  6  1.685022e+01 -9.999679e-01 -9.499072e-01  1.690657e+01
  8 -1.758065e+01 -1.000000e+00 -9.843998e-01  1.763656e+01
 13  1.683365e+01 -9.999425e-01 -9.479473e-01  1.688994e+01
 14  1.683288e+01 -9.999393e-01 -9.477738e-01  1.688916e+01
 15 -6.823206e+00 -9.449744e-01 -9.395253e-01  6.952109e+00
 17 -1.562364e+01 -9.310452e-01 -9.348566e-01  1.567925e+01
 18  1.672081e+01 -9.999969e-01 -9.499099e-01  1.677760e+01
 19 -1.795940e+01 -1.000000e+00 -9.864808e-01  1.801425e+01
 20 -1.761123e+01 -9.997436e-01 -9.841299e-01  1.766701e+01
 21  1.684613e+01 -9.999461e-01 -9.499054e-01  1.690250e+01
 22  1.685548e+01 -9.999941e-01 -9.499091e-01  1.691181e+01
 23 -1.700952e+01 -9.895408e-01 -9.656997e-01  1.706562e+01
 27  1.685593e+01 -9.999979e-01 -9.563742e-01  1.691263e+01
 28  1.685714e+01 -1.000000e+00 -1.000000e+00  1.691636e+01
 31  1.685714e+01 -1.000000e+00 -9.499099e-01  1.691347e+01
 32 -1.881871e+01 -1.000000e+00  5.612510e+04  5.612510e+04
 33  1.685714e+01 -1.000000e+00 -9.499100e-01  1.691347e+01
```

Figure 5.7 (continue)

```
 34  1.685714e+01  -1.000000e+00  -9.499100e-01  1.691347e+01
 35  -9.996366e+00  -9.998021e-01  -9.678523e-01  1.009275e+01
 37  1.685714e+01  -9.974540e-01  6.329882e+04  6.329882e+04
 38  -1.885714e+01  -1.000000e+00  -1.000000e+00  1.891010e+01
 39  -1.711248e+01  -9.938904e-01  -9.717333e-01  1.716884e+01
 40  1.683371e+01  -9.999428e-01  -9.479620e-01  1.689001e+01
 41  -1.761123e+01  -9.997436e-01  -9.841299e-01  1.766701e+01
 42  -1.885714e+01  -1.000000e+00  -9.847350e-01  1.890930e+01
 43  1.683371e+01  -9.999428e-01  -9.479620e-01  1.689001e+01
 44  1.685714e+01  -1.000000e+00  -9.499099e-01  1.691347e+01
 45  -1.881871e+01  -1.000000e+00  5.612451e+04  5.612451e+04
 46  -1.795937e+01  -1.000000e+00  -9.864808e-01  1.801422e+01
 47  -1.739888e+01  -1.000000e+00  -9.818999e-01  1.745523e+01


----------------------------------------
N_of_fault_type= 2
```

Figure 5.7 (continue)

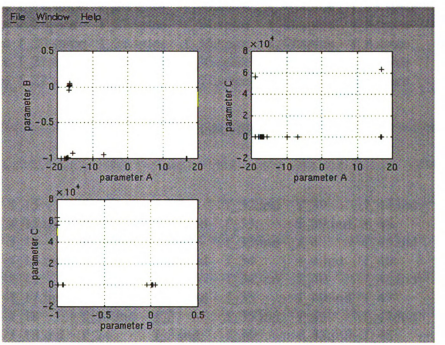


Figure 5.8 Fault behavior display window.

ifa1	ifa2	ifa3.m	ifaBCH1	ifa_fbe.ext	ifaftde.m	ifastep1

(a) Program files

f_0.spice	f_16.spice	f_23.spice	f_30.spice	f_38.spice	f_45.spice	f_9.spice
f_1.spice	f_17.spice	f_24.spice	f_31.spice	f_39.spice	f_46.spice	prem.cir
f_10.spice	f_18.spice	f_25.spice	f_32.spice	f_4.spice	f_47.spice	
f_11.spice	f_19.spice	f_26.spice	f_33.spice	f_40.spice	f_48.spice	
f_12.spice	f_2.spice	f_27.spice	f_34.spice	f_41.spice	f_5.spice	
f_13.spice	f_20.spice	f_28.spice	f_35.spice	f_42.spice	f_6.spice	
f_14.spice	f_21.spice	f_29.spice	f_36.spice	f_43.spice	f_7.spice	
f_15.spice	f_22.spice	f_3.spice	f_37.spice	f_44.spice	f_8.spice	

(b) Input files

Cell_lib	f_15	f_20.ind	f_27	f_32.ind	f_39	f_44.ind	f_7
f_1	f_15.ind	f_21	f_27.ind	f_33	f_39.ind	f_45	f_7.ind
f_1.ind	f_16	f_21.ind	f_28	f_33.ind	f_4	f_45.ind	f_8
f_10	f_16.ind	f_22	f_28.ind	f_34	f_4.ind	f_46	f_8.ind
f_10.ind	f_17	f_22.ind	f_29	f_34.ind	f_40	f_46.ind	f_9
f_11	f_17.ind	f_23	f_29.ind	f_35	f_40.ind	f_47	f_9.ind
f_11.ind	f_18	f_23.ind	f_3	f_35.ind	f_41	f_47.ind	paradeg1
f_12	f_18.ind	f_24	f_3.ind	f_36	f_41.ind	f_48	paradeg2
f_12.ind	f_19	f_24.ind	f_30	f_36.ind	f_42	f_48.ind	paradev1
f_13	f_19.ind	f_25	f_30.ind	f_37	f_42.ind	f_5	paradev2
f_13.ind	f_2	f_25.ind	f_31	f_37.ind	f_43	f_5.ind	paraidx1
f_14	f_2.ind	f_26	f_31.ind	f_38	f_43.ind	f_6	paraidx2
f_14.ind	f_20	f_26.ind	f_32	f_38.ind	f_44	f_6.ind	

(c) Output files

Figure 5.9 Summary of files used or generated in CLG_routine.

the subroutines, *ifa1*, *ifa2*, *ifaBCH1*, *ifastep1*, and *ifa3.m*. The detail function of each subroutine can be found in [67]. The input files include *f_0.spice*, *f_i.spice*, and *prem.cir*, as shown in Figure 5.9(b), while the output files are listed in Figure 5.9(c).

5.2 MLG_Routine

The MLG_Routine establishes the macro library described in Figure 4.4. For simplicity of discussion, consider the target macro "current copier" in Figure 4.6 which is comprised of four primitive cells (PCs): OP, CSW, VSW, and SE. Based on the CLG_Rouine, the cell library for these four PCs have been built. In MLG_Routine, the Faulty Performance Evaluator (FPE) derives the parameter deviation bounds, generates test set, and evaluates the fault coverage of the macro with only one defective PC. Thus, for the marco "current copier", The FPE will be respectively used to generate the macro data for the defective OP, CSW, VSW, and SE. Here, the detail operation of evaluating the faulty performance of the macro with the defective OP is presented. The same procedure can be applied for the remaining 3 PCs and the results are attached in Appendix B.

In MLG_Routine, a Spice file, namely "macro.cir", is used to simulate the good and faulty circuit behaviors. Figure 5.10 shows the "macroamp.cir" for the macro with the defective Opamp, where the code "Xamp 4 0 1 14 10 K" will call the sub-circuit K in Figure 5.3, where K will be substituted, in turns, by f_0.spice, and f_i.spice in the cell library of Opamp. Similarly, the files macrostr.cir for SE, macroswN.cir for CSW, macroswx.cir for VSW can be found in Appendix B.

The FPE evaluates the faulty behaviors by executing the program "ifa_fpe.exe" for "macro.cir" with various Spice files for good and defective Opamps. The simulation

```
*** Current copier
*
* This program contains the current copier structure
* used to verify the hierarchical IFA fault modeling.
* Treating it as a macro, the current copier includes
* four premitive components, i.e. amplifier, current
* switch, voltage switch and storage element, and they
* are represented by the 'K' files in cell libraries
* 'ampadc', 'switchN', 'switchx' and 'store', respec-
* tively. All these 'K' files are extracted from the
* corresponding premitive component (cell) layouts.

M2 15  12 1 1 pfet w=27u l=3u
M9  3  2  1  1 pfet w=23u l=5u
M10 2  2  1  1 pfet w=23u l=5u

C2 12 1 0.5p

Xamp 4 0 1 14 10 K

Xstore 7 9 14 storeNz

G1 2 14 (17,0) 1
r1 17 0 1meg

Xs1  3  4  5 switchCz
Xs2  24  7  8 switchCz
Xs3 10  9 11 switchxz
Xs4  4 15 16 switchCz
Xs5 10 12 13 switchxz

Vdd 1 0 2.5
Vss 14 0 -2.5

Vs1 5 0 pwl(0 -2.5 1n 2.5 1.999u 2.5 2u -2.5)
Vs2 8 0 pwl(0 -2.5 1n 2.5)
Vs3 11 0 pwl(0 -2.5 1n 2.5 1.9u 2.5 1.901u -2.5)
Vs4 16 0 pwl(0 -2.5 1.999u -2.5 2u 2.5)
Vs5 13 0 pwl(0 -2.5 1.999u -2.5 2u 2.5)

Vt 4 24 0
```

Figure 5.10 Example of macro.cir.

```
Vi 17 0 input

.ic v(9)=0 v(12)=0 v(4)=0

.Lib K
.Lib /home/ub/wangche4/ADT/lib/switchxz
.Lib /home/ub/wangche4/ADT/lib/switchCz
.Lib /home/ub/wangche4/ADT/lib/storeNz
.tran 0.05u 4u
.print tran i(Vt)

*N34O  SPICE LEVEL 2 PARAMETERS
.Model sv vswitch Ron=4e5 Roff=1e6
+von=2 voff=-2
*parameters: MOSIS 2 micron CMOS process
.model nfet nmos level=2 Ld=.115u TOX=423e-10 NSUB=1.0125225e16
+VTO=.822163 kp=4.893760e-5 gamma=.47 phi=0.6 UO=599.496
+UEXP=5.324966e-3 UCRIT=12714.2 DELTA=3.39718e-5 VMAX=65466.1
+XJ=0.55u lambda=1.991479e-2 NFS=5.66758e11 Neff=1.0010e-2
+NSS=0.0 TPG=1.00 rsh=28.070 CGSO=0.9388e-10 CGDO=0.9388e-10
+cj=1.4563e-4 MJ=0.6 cjsw=6.617e-10 mjsw=0.31

.model pfet pmos level=2 Ld=.18u TOX=423e-10 NSUB=1.421645e15
+VTO=-.776658 kp=1.916950e-5 gamma=.52 phi=0.6 UO=234.831
+UEXP=0.142293 UCRIT=20967 DELTA=1e-6 VMAX=34600.2
+XJ=0.41u lambda=4.921086e-2 NFS=4.744781e11 Neff=1.0010e-2
+NSS=0.0 TPG=-1.00 rsh=45.92 CGSO=1.1957e-10 CGDO=1.1957e-10
+cj=2.4e-4 MJ=0.5 cjsw=3.62e-10 mjsw=0.29

.OPTIONs RELTOL=1E-6 pivtol=1e-36 pivrel=1e-36
+CHGtol=1e-13 Abstol=1e-13 VNtol=1e-10 Itl5=0 Itl4=80
+NUMDGT=8 gmin=1e-18 NOECHO NOMOD NOPAGE
.end
```

Figure 5.10 (continue)

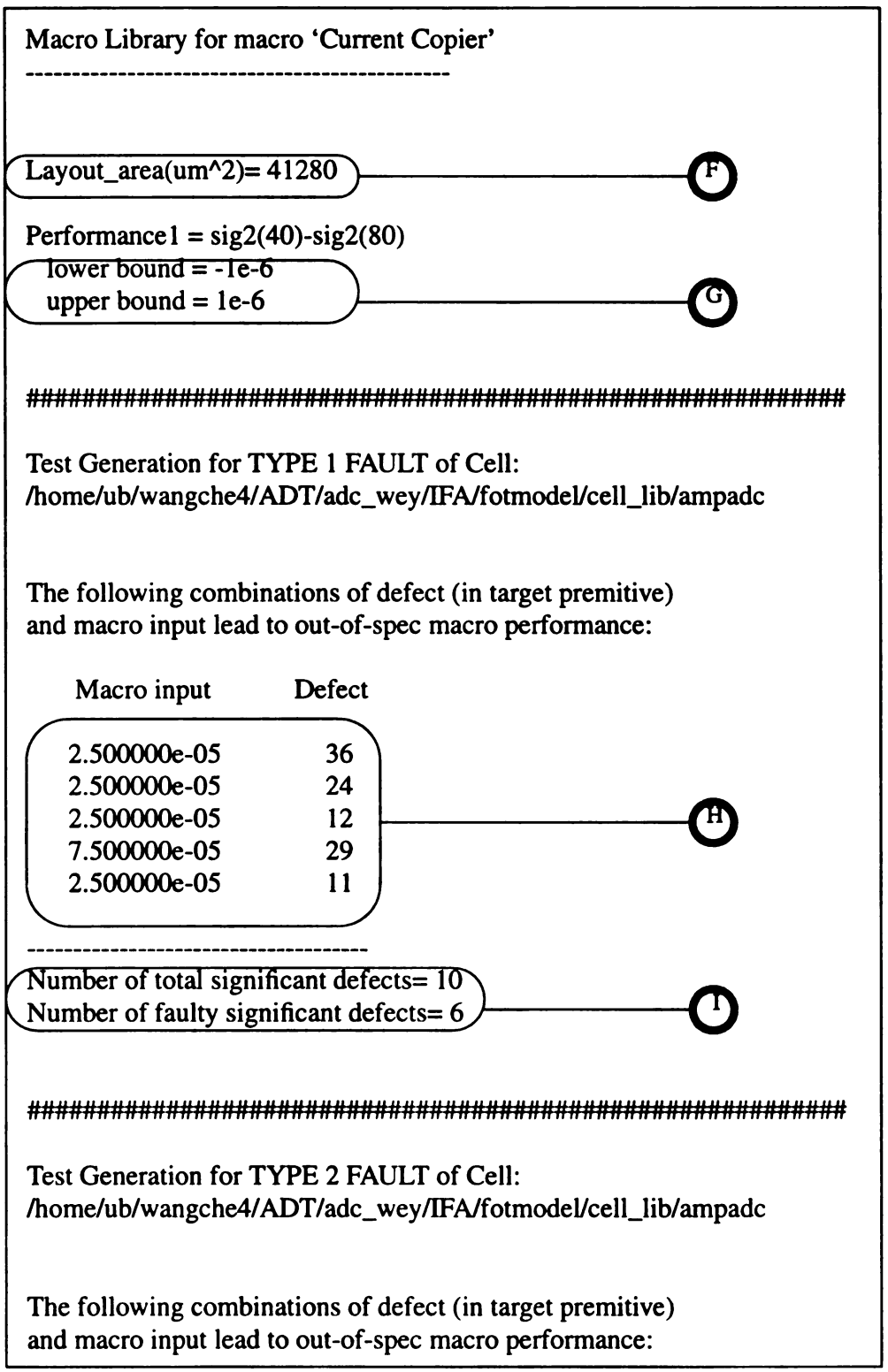


Figure 5.11 Example of macro library.

Macro input	Defect
2.500000e-05	15
0.000000e+00	35
2.500000e-05	35
5.000000e-05	35
7.500000e-05	35
1.000000e-04	35
2.500000e-05	17
2.500000e-05	18
5.000000e-05	18
7.500000e-05	18
1.000000e-04	18
2.500000e-05	23
2.500000e-05	39
2.500000e-05	47
5.000000e-05	47
7.500000e-05	47
1.000000e-04	47
2.500000e-05	8
5.000000e-05	8
7.500000e-05	8
1.000000e-04	8
2.500000e-05	5
5.000000e-05	5
7.500000e-05	5
1.000000e-04	5
2.500000e-05	20
5.000000e-05	20
7.500000e-05	20
1.000000e-04	20
2.500000e-05	46
5.000000e-05	46
7.500000e-05	46
1.000000e-04	46
2.500000e-05	42
5.000000e-05	42
7.500000e-05	42
1.000000e-04	42
2.500000e-05	1
5.000000e-05	1

Figure 5.11 (continue)

```
7.500000e-05        1
1.000000e-04        1
2.500000e-05        45
5.000000e-05        45
7.500000e-05        45
1.000000e-04        45
2.500000e-05        32
5.000000e-05        32
7.500000e-05        32
1.000000e-04        32
0.000000e+00        37

-------------------------------------
Number of total significant defects= 32
Number of faulty significant defects= 19
```

Figure 5.11 (continue)

results are listed in Figure 5.11. Results first show that the layout area of the current copier is 41280 μm^2, and the performance specification is that the stored current is ranged between -1e-6A and 1e-6A. For Type 1 fault, i.e., *Offset voltage is too large*, the input current 2.5e-5A excites faulty performance when the 11th, 12th, 24th, or 36th significant defect occurs, while the input current 7.5e-5A excites the 29th significant defects. Thus, both 2.5e-5A and 7.5e-5A are used as the test signals to defect Type 1 faults. Results also show that 10 significant defects are classified as the *Type 1 faults,* which is exactly the same as the result shown in Figure 5.7. Computation results conclude that 6 out the 10 significant defects lead to faulty performance. The number of total significant defects is not necessary to be equal to that shown in the list of input-defect combination because the test generator embedded in FPE automatically eliminates the simulation of some significant defects which has same fault behavior space degree as that of previously simulated defect in order to speed up the test generation[67]. These eliminated significant defects will not be shown in the list of input-defect combination, however will be count for the number of total significant defects. Similarly, 32 significant defects are classified as *Type 2 faults.* both 0A and 2.5e-5A can excite 16 defects listed in Figure 5.11, and they are chosen as the test set. Combining the test sets for both Type 1 fault and Type 2 fault, the test set of the Opamp cell employed by the macro "current copier" is {0A,2.5e-5A,7.5e-5A). Because that the test input 0A detects only 35th and 37th significant defects, between them, the 35th significant defect can also be covered by 2.5e-6A. Thus the input 0A can be eliminated from the test set for simplifying the testing process while still maintaining high fault coverage. That is to say, by using test set {0A,2.5e-6A,7.5e-6A}, all the 25 significant defects can be detected; however, 24 out of the 25 significant defects can still be detected

if we only use the test set {2.5e-6A,7.5e-6A}. Thus, the final test set could be {2.5e-5A,7.5e-5A}.

As shown in Appendix B, the three other PCs, CSW, VSW, and SE, can be tested by 1.0e-4A. Thus, the compacted test set for the current copier is (2.5e-5A,7.5e-5A,1.0e-4A). Based on the test set, the fault coverage is almost 100% if the tester has a 100% accuracy, as discussed in Table 3.1.

Similar to Table 3.2., consider an inaccurate tester is used and the fault coverage is degraded. The inaccuracy of the tester can be viewed as a deviation on the performance specifications used in establishing the macro library. For example, let the inaccuracy of the tester is 25%. Thus, the performance specification bounds are changed from 1e-6A to 1.25e-6A to represent the 25% inaccuracy of the tester. The same procedures are applied to generate the macro current copier and simulation results are shown in Appendix C.

The fault coverage of a macro can be computed as defined in (4.2), where the ratio of the significant defects overall injected defects is defined as

$$P_{si} = [N_{sf} + \Sigma N_{fsd}] / N_{jd} \tag{5.1}$$

where N_{sf} is the number of failure simulations, i.e., the term N_of_sim_fail in Figure 5.7 for Opamp cell, N_{fsd} is the number of faulty significant defects (Figure 5.11), and N_{jd} is N_of_injected_defects (Figure 5.7). For example, for the Opamp, N_{sf}=6, N_{fsd}=6 for Type 1 fault and 19 for Type 2 fault, and N_{jd}=700. Thus, the ratio $P_{si}=P_{Opamp}=[6+(6+19)]/700=0.044286$.

The fault coverage of the i-th primitive cell is defined as

$$FC_i = [N_{sf} + \Sigma N_{fsd}]_i / [N_{sf} + \Sigma N_{fsd}] \tag{5.2}$$

where $[N_{sf} + \Sigma N_{fsd}]_i$ is the total significant defects with the inaccurate tester. For example,

As shown in C1 (Appendix C), $[N_{sf} + \Sigma N_{fsd}]_i$=6+(4+18)=28. Thus, by (5.2),

$$FC_{Opamp} = (6+22) / (6+25) = 0.903226.$$

Similarly, for current switch (CSW), voltage switch (VSW), and Storage element (SE)

$$P_{CSW} = [17+(4+0+3)]/350=0.068571; FC_{CSW}=[17+7]/[17+7]=1.0$$

$$P_{VSW} = [14+(2+1+6+3)]/350=0.074286; FC_{VSW}=[14+12]/[14+12]=1.0$$

$$P_{SE} = [1+23]/350=0.068571; FC_{SE}=[1+23]/[1+23]=1.0$$

Note that the areas for the four PCs and the macro are

$$A_{Opamp}=21837; A_{CSW}=1638; A_{VSW}=1666\ A_{SE}=1100, \text{ and } A_{copier}=41280.$$

By (4.2),

$$A_{Opamp}P_{Opamp}FC_{Opamp}=21837x0.044286x0.903226=873.4858$$

$$A_{CSW}P_{CSW}FC_{CSW} =1638x0.068571x1.0=112.3193$$

$$A_{VSW}P_{VSW}FC_{VSW}=1666x0.074286x1=123.7605$$

$$A_{SE}P_{SE}FC_{SE}=1100*0.068571*1=75.4281$$

and the sum of the above terms, FC_x, is 1.185e+3. Similarly,

$$A_{Opamp}P_{Opamp}=967.0736; A_{CSW}P_{CSW}=112.3193;$$

$$A_{VSW}P_{VSW}=123.7605; A_{SE}P_{SE}=75.4281.$$

The sum of the above terms, FC_y, is 1.2786e+3. Thus, with 25% inaccuracy of the tester, the fault coverage

$$FC = FC_x / FC_y = 1.185e+3 / 1.2786e+3 = 0.9268.$$

Chapter 6

CONCLUSION

Mixed-signal ICs gradually becomes the main-stream solutions for the applications such as portable data systems, wireless communication, and multimedia. Manufacturers have made every effort to enhance the function and performance an mixed-signal IC can achieve; but the complexity of the IC is also increased at the same time. Due to the increasing complexity, manufacturers confront the problem of long testing cycle by using the conventional external functional test performed on ATE machine. This not only reduces the testing confidence, but also increases the cost directly. Existing design-for-testability techniques cannot resolve the testing complexity problem because most of the techniques need exhaustive test set. Therefore, it is necessary to develop a testability design methodology that maps the specification-driven testing process to a simpler fault-model-based process. This thesis presents the methodologies that target the issues on testability design rule, hierarchical fault macromodeling procedure, and test generation process.

6.1 Summary

Two major tasks in the fault-model-based testing process, fault definition and test generation, have been reviewed. Inductive Fault Analysis (IFA), a practical fault definition

technique used as the basis of proposed fault modeling methodology, was introduced. The structures and operations of switched-current circuits were discussed in order to show the test generation of algorithmic switched-current ADC based on the single stuck-at-fault model which is widely used in digital circuit testing. Several commonly used testing schemes for enhancing the testability of analog/mixed-signal ICs were also reviewed.

The single stuck-at-fault model only represents part of the fault types which may occur in analog/mixed-signal circuits. The proposed testability design methodology uses the IFA technique to develop a practical fault model to represent both stuck-at faults and parametric faults. The IFA-based fault modeling process firstly derives a graded list of the most likely fault types from a description of circuit layout, process parameters, and defect statistics of the fabrication process. The fault model is then established using these fault types. Given the performance specifications and a discrete input set which used for design verification, the parameter bound is derived for each fault type and is then used for test generation and fault coverage calculation. To make the test generation process simple and successful, a circuit should be designed with the testability design rules to ensure the existence of parameter bounds.

This thesis also presents the testability enhancement methodologies to further decrease the testing cycle time and increase the testability of analog/mixed-signal ICs. The hierarchical IFA-based fault macromodeling process is developed to reduce the computational complexity of IFA-based fault modeling. In this hierarchical testing scheme, a design is decomposed into primitive cells and/or macros, and their IFA testing data such as fault behavior values, number of injected defects, test set, and fault coverage are stored in cell/macro library. A software tool has been developed to establish the testing

environment.

High-accuracy built-in tester not only help increase the observability of a design, but also simplify the test sequence. Thus, it decreases the testing cycle time. The study shows that there exists a trade-off between the accuracy of the built-in tester and the test sequence. The test sequence length can be reduced significantly if a high-accuracy tester is used.

6.2 Future Work

It is believed that the complexity of analog/mixed-signal ICs will continuously increase. Thus, further enhancing testability is necessary and the developed testability design methodologies can be improved in many different ways.

The success of a developed fault macromodeling process is determined by the fault coverage that the generated test set can achieve. The developed fault macro macromodeling process can precisely evaluate the fault coverage of a primitive cell. The evaluated fault coverage for each cell can be carried out for a macro. However, a macro not only contains a number of primitive cells, but also includes the interconnect among these cells. The routing area is still susceptible to defects. In Section 4.1.2, the evaluation of fault coverage including the routing area has been developed. However, it was assumed that the defects in the routing area which causes hard faults are testable. This means that the evaluation obtains the worst case fault coverage. To obtain more accurate evaluation, the testability of the defects that cause parametric faults must be further investigated. Since the routing area and interconnects depend on the applications and design style, the way of precisely evaluating the fault coverage in the routing area is a challenging research task.

A designed analog circuit can be easily testable if the circuit is designed based on the testability design rules developed in Section 4.2. In addition, the testability can also be enhanced by using the built-in tester developed in Section 4.3. It is believed that some hard-to-test faults can be eliminated if the circuit layout is changed. In the IFA-based fault macromodeling process. the generated test set is determined in part by the circuit layout. Different layout style may generate different test sets. Thus, developing a set of testability rules in the layout level can easily eliminate some hard-to-test faults and indirectly simplify the test generation process.

Finally, as discussed in Section 4.3, the testability can be enhanced by accessing the internal test points using the built-in tester. There exists a trade-off between the tester's circuit complexity and test sequence length. Note that a high-accuracy tester may be needed to measure the test signals on an insensitive test point. Thus, a higher complexity tester is required for maintaining the testing speed. This implies that selecting the measurements on highly sensitive test points can reduce the tester cost, and how to select them becomes an important research topic for future study.

APPENDICES

APPENDIX A

APPENDIX A

A.1 Cell Library of Current Switch

Cell Library for Primitive Component 'switchN'

Layout_area(um^2)= 1638

N_of_injected_defects= 350

Detected Output Variables of Premitive Simulation #1
tran ---------> sig1
i(vx) ---------> sig2

Detected Output Variables of Premitive Simulation #2
tran ---------> sig3
v(1) ---------> sig4

Parameter1= 0.7/sig2(18)
Norminal value of parameter1= 2.8622e+3

Parameter2= 2.5/sig2(38)
Norminal value of parameter2= 8.4198e+12

List of fault behavior values(normalized deviation):
(1st column: index of defects; last column: norm)

1	-1.4057295e-06	-1.0000000e+00	1.0000000e+00
2	2.8196669e+14	3.1038731e-01	2.8196669e+14
3	2.2785931e-01	-1.8788078e-01	2.9532872e-01
4	1.6586275e+13	3.4527163e-01	1.6586275e+13
5	1.8797779e+13	1.9368736e-01	1.8797779e+13

```
  8   4.7876678e-01  -2.2565036e-01   5.2927849e-01

 16   2.6104129e-01  -2.0270987e-01   3.3050544e-01

 17   3.8246059e+00  -1.6004544e+01   1.6455182e+01

 19  -1.4057295e-06  -1.7262414e-01   1.7262414e-01

 21  -1.4057295e-06  -1.0000000e+00   1.0000000e+00

 27   2.6104129e-01  -2.0270987e-01   3.3050544e-01


N_of_significant_defects= 28

N_of_sim_fail= 17



----------------------------------------
Type1 fault: On resistance is too large

N_of_type1 fault= 4

   5  1.879778e+13  1.936874e-01  1.879778e+13
   8  4.787668e-01  -2.256504e-01  5.292785e-01
  16  2.610413e-01  -2.027099e-01  3.305054e-01
  27  2.610413e-01  -2.027099e-01  3.305054e-01


----------------------------------------
Type2 fault: Off resistance is too small

N_of_type2 fault= 2

   1  -1.405730e-06  -1.000000e+00  1.000000e+00
  21  -1.405730e-06  -1.000000e+00  1.000000e+00


----------------------------------------
Type3 fault: Ron is too large and Roff is too small
```

N_of_type3 fault= 5

2	2.819667e+14	3.103873e-01	2.819667e+14
3	2.278593e-01	-1.878808e-01	2.953287e-01
4	1.658628e+13	3.452716e-01	1.658628e+13
17	3.824606e+00	-1.600454e+01	1.645518e+01
19	-1.405730e-06	-1.726241e-01	1.726241e-01

N_of_fault_type= 3

A.2 Cell Library of Voltage Switch

Cell Library for Primitive Component 'switchx'

Layout_area(um^2)= 1666

N_of_injected_defects= 350

Detected Output Variables of Premitive Simulation #1
tran ---------> sig1
i(vx) ---------> sig2

Detected Output Variables of Premitive Simulation #2
tran ---------> sig3
v(1) ---------> sig4

Parameter1= 0.7/sig2(18)
Norminal value of parameter1= 3.4345e+3

Parameter2= 2.5/sig2(38)
Norminal value of parameter2= 6.5526e+12

Parameter3= sig4(38)
Norminal value of parameter3= 1.5396328e-2

List of fault behavior values(normalized deviation):
(1st column: index of defects; last column: norm)

1	6.0736083e-06	-2.3245778e-06	0.0000000e+00	6.5032592e-06
2	1.4546818e-02	-6.1743795e-02	-7.5052961e-03	6.3876722e-02
3	6.0736083e-06	-2.3245778e-06	0.0000000e+00	6.5032592e-06
4	6.0736083e-06	-2.3245778e-06	0.0000000e+00	6.5032592e-06

5	6.0736083e-06	-2.3245778e-06	0.0000000e+00	6.5032592e-06
6	6.0736083e-06	-2.3245778e-06	0.0000000e+00	6.5032592e-06
7	6.0736083e-06	-2.3245778e-06	0.0000000e+00	6.5032592e-06
8	-4.8205323e-02	3.7287928e-02	3.4908713e-02	7.0233617e-02
11	5.1776463e-01	-5.4653168e-02	-8.5467780e+00	8.5626212e+00
13	7.1099815e+01	-1.0000000e+00	-1.0000000e+00	7.1113879e+01
15	5.5948052e+12	1.7493363e+01	2.1710909e+00	5.5948052e+12
17	6.1226732e-06	-1.4964461e-01	-3.1183130e-01	3.4587898e-01
20	2.1449866e-01	1.1071757e+00	-1.3940769e+00	1.7931252e+00
24	3.0505743e-01	2.3733617e-01	-8.1491956e+00	8.1583563e+00
27	1.7389233e-01	-2.9947582e-01	5.1564574e+00	5.1680729e+00
28	6.0736083e-06	-9.6127504e-02	1.9391124e-01	2.1643028e-01
29	-1.2626046e-03	-1.6883154e-01	2.1266332e+00	2.1333247e+00
30	1.2147192e-02	5.0288629e-01	-6.2277837e-03	5.0307152e-01
31	6.0736083e-06	-5.5974618e-02	3.9199542e-01	3.9597167e-01
33	-1.8481847e+00	-1.0000000e+00	1.6137638e+02	1.6139006e+02
34	-1.8481847e+00	-1.0000000e+00	1.6137638e+02	1.6139006e+02
35	-1.8481847e+00	-1.0000000e+00	1.6137638e+02	1.6139006e+02
36	-1.8481847e+00	-1.0000000e+00	1.6137638e+02	1.6139006e+02

N_of_significant_defects= 37

N_of_sim_fail= 14

Type1 fault: On resistance is too large

N_of_type1 fault= 2

11 5.177646e-01 -5.465317e-02 -8.546778e+00 8.562621e+00
24 3.050574e-01 2.373362e-01 -8.149196e+00 8.158356e+00

Type2 fault: Off resistance is too small

N_of_type2 fault= 1

27 1.738923e-01 -2.994758e-01 5.156457e+00 5.168073e+00

Type3 fault: Charge injection is too large

N_of_type3 fault= 6

15 5.594805e+12 1.749336e+01 2.171091e+00 5.594805e+12
29 -1.262605e-03 -1.688315e-01 2.126633e+00 2.133325e+00
33 -1.848185e+00 -1.000000e+00 1.613764e+02 1.613901e+02
34 -1.848185e+00 -1.000000e+00 1.613764e+02 1.613901e+02
35 -1.848185e+00 -1.000000e+00 1.613764e+02 1.613901e+02
36 -1.848185e+00 -1.000000e+00 1.613764e+02 1.613901e+02

Type4 fault: Ron is too large & Roff is too small

N_of_type4 fault= 14

1 6.073608e-06 -2.324578e-06 0.000000e+00 6.503259e-06
2 1.454682e-02 -6.174379e-02 -7.505296e-03 6.387672e-02
3 6.073608e-06 -2.324578e-06 0.000000e+00 6.503259e-06
4 6.073608e-06 -2.324578e-06 0.000000e+00 6.503259e-06
5 6.073608e-06 -2.324578e-06 0.000000e+00 6.503259e-06
6 6.073608e-06 -2.324578e-06 0.000000e+00 6.503259e-06
7 6.073608e-06 -2.324578e-06 0.000000e+00 6.503259e-06
8 -4.820532e-02 3.728793e-02 3.490871e-02 7.023362e-02

```
 13  7.109982e+01  -1.000000e+00  -1.000000e+00  7.111388e+01
 17  6.122673e-06  -1.496446e-01  -3.118313e-01  3.458790e-01
 20  2.144987e-01  1.107176e+00  -1.394077e+00  1.793125e+00
 28  6.073608e-06  -9.612750e-02  1.939112e-01  2.164303e-01
 30  1.214719e-02  5.028863e-01  -6.227784e-03  5.030715e-01
 31  6.073608e-06  -5.597462e-02  3.919954e-01  3.959717e-01


----------------------------------------
N_of_fault_type= 4
```

A.3 Cell Library of Storage Element

```
Cell Library for Primitive Component 'store'
---------------------------------------------


Layout_area(um^2)= 1100

N_of_injected_defects= 350

Detected Output Variables of Premitive Simulation #1
     tran ---------> sig1
   i(vdd) ---------> sig2



Parameter1= -1*sig2(40)
Norminal value of parameter1= 9.44844e-5



List of fault behavior values(normalized deviation):
(1st column: index of defects; last column: norm)

  1  -1.0000000e+00   1.0000000e+00

  2  -1.0000000e+00   1.0000000e+00

  3  -1.0000000e+00   1.0000000e+00

  4  -1.0000000e+00   1.0000000e+00

  5  -1.0000000e+00   1.0000000e+00

  6  -1.0000000e+00   1.0000000e+00

  7  -1.0000000e+00   1.0000000e+00

  8  -1.0000000e+00   1.0000000e+00
```

```
 9   1.5369818e-01   1.5369818e-01

10  -1.0000000e+00   1.0000000e+00

11  -1.0000000e+00   1.0000000e+00

12  -1.0000000e+00   1.0000000e+00

13  -1.0000000e+00   1.0000000e+00

14  -1.0000000e+00   1.0000000e+00

15  -1.0000000e+00   1.0000000e+00

16  -1.0000000e+00   1.0000000e+00

17  -1.0000000e+00   1.0000000e+00

18  -1.0000000e+00   1.0000000e+00

19  -1.0000000e+00   1.0000000e+00

20  -1.0000000e+00   1.0000000e+00

21  -1.0000000e+00   1.0000000e+00

22   1.1083183e+00   1.1083183e+00

24  -1.9927927e-01   1.9927927e-01


N_of_significant_defects= 24

N_of_sim_fail= 1



----------------------------------------
Type1 fault: Deviation of memorized current is too large

N_of_type1 fault= 23
```

```
 1 -1.000000e+00  1.000000e+00
 2 -1.000000e+00  1.000000e+00
 3 -1.000000e+00  1.000000e+00
 4 -1.000000e+00  1.000000e+00
 5 -1.000000e+00  1.000000e+00
 6 -1.000000e+00  1.000000e+00
 7 -1.000000e+00  1.000000e+00
 8 -1.000000e+00  1.000000e+00
 9  1.536982e-01  1.536982e-01
10 -1.000000e+00  1.000000e+00
11 -1.000000e+00  1.000000e+00
12 -1.000000e+00  1.000000e+00
13 -1.000000e+00  1.000000e+00
14 -1.000000e+00  1.000000e+00
15 -1.000000e+00  1.000000e+00
16 -1.000000e+00  1.000000e+00
17 -1.000000e+00  1.000000e+00
18 -1.000000e+00  1.000000e+00
19 -1.000000e+00  1.000000e+00
20 -1.000000e+00  1.000000e+00
21 -1.000000e+00  1.000000e+00
22  1.108318e+00  1.108318e+00
24 -1.992793e-01  1.992793e-01


----------------------------------------
N_of_fault_type= 1
```

APPENDIX B

APPENDIX B

B.1 Macro Library of Current Copier With Target Cell, Current Switch, and Specifications of (+/-)1e-6

Macro Library for macro 'Current Copier'

Layout_area(um^2)= 41280

Performance1 = sig2(40)-sig2(80)
  lower bound = -1e-6
  upper bound = 1e-6

##

Test Generation for TYPE 1 FAULT of Cell:
/home/ub/wangche4/ADT/adc_wey/IFA/fotmodel/cell_lib/switchN

The following combinations of defect (in target premitive)
and macro input lead to out-of-spec macro performance:

Macro input	Defect
1.000000e-04	16
0.000000e+00	8
2.500000e-05	8
5.000000e-05	8
7.500000e-05	8
1.000000e-04	8
0.000000e+00	5
2.500000e-05	5
5.000000e-05	5
7.500000e-05	5
1.000000e-04	5

Number of total significant defects= 4
Number of faulty significant defects= 4

```
##########################################################

Test Generation for TYPE 2 FAULT of Cell:
/home/ub/wangche4/ADT/adc_wey/IFA/fotmodel/cell_lib/switchN


The following combinations of defect (in target premitive)
and macro input lead to out-of-spec macro performance:

     Macro input          Defect


-----------------------------------
Number of total significant defects= 2
Number of faulty significant defects= 0


##########################################################

Test Generation for TYPE 3 FAULT of Cell:
/home/ub/wangche4/ADT/adc_wey/IFA/fotmodel/cell_lib/switchN


The following combinations of defect (in target premitive)
and macro input lead to out-of-spec macro performance:

     Macro input          Defect

    0.000000e+00           17
    2.500000e-05           17
    5.000000e-05           17
    7.500000e-05           17
    1.000000e-04           17
    0.000000e+00           4
    2.500000e-05           4
    5.000000e-05           4
    7.500000e-05           4
    1.000000e-04           4

-----------------------------------
Number of total significant defects= 5
Number of faulty significant defects= 3
```

B.2 Macro Library of Current Copier With Target Cell, Voltage Switch, and Specifications of (+/-)1e-6

Macro Library for macro 'Current Copier'

Layout_area(um^2)= 41280

Performance1 = sig2(40)-sig2(80)
  lower bound = -1e-6
  upper bound = 1e-6

##

Test Generation for TYPE 1 FAULT of Cell:
/home/ub/wangche4/ADT/adc_wey/IFA/fotmodel/cell_lib/switchx

The following combinations of defect (in target premitive)
and macro input lead to out-of-spec macro performance:

Macro input	Defect
2.500000e-05	24
5.000000e-05	24
1.000000e-04	24
0.000000e+00	11
2.500000e-05	11
5.000000e-05	11
7.500000e-05	11
1.000000e-04	11

Number of total significant defects= 2
Number of faulty significant defects= 2

##

Test Generation for TYPE 2 FAULT of Cell:
/home/ub/wangche4/ADT/adc_wey/IFA/fotmodel/cell_lib/switchx

The following combinations of defect (in target premitive)
and macro input lead to out-of-spec macro performance:

Macro input	Defect
1.000000e-04	27

Number of total significant defects= 1
Number of faulty significant defects= 1

##########

Test Generation for TYPE 3 FAULT of Cell:
/home/ub/wangche4/ADT/adc_wey/IFA/fotmodel/cell_lib/switchx

The following combinations of defect (in target premitive)
and macro input lead to out-of-spec macro performance:

Macro input	Defect
1.000000e-04	29
0.000000e+00	33
7.500000e-05	33
1.000000e-04	33
0.000000e+00	15
2.500000e-05	15
5.000000e-05	15
7.500000e-05	15
1.000000e-04	15

Number of total significant defects= 6
Number of faulty significant defects= 6

##########

Test Generation for TYPE 4 FAULT of Cell:
/home/ub/wangche4/ADT/adc_wey/IFA/fotmodel/cell_lib/switchx

The following combinations of defect (in target premitive)
and macro input lead to out-of-spec macro performance:

Macro input	Defect
1.000000e-04	8
1.000000e-04	20
5.000000e-05	13
7.500000e-05	13
1.000000e-04	13

Number of total significant defects= 14
Number of faulty significant defects= 3

B.3 Macro Library of Current Copier With Target Cell, Storage Element, and Specifications of (+/-)1e-6

```
Macro Library for macro 'Current Copier'
-----------------------------------------


Layout_area(um^2)= 41280

Performance1 = sig2(40)-sig2(80)
  lower bound = -1e-6
  upper bound = 1e-6


############################################################

Test Generation for TYPE 1 FAULT of Cell:
/home/ub/wangche4/ADT/adc_wey/IFA/fotmodel/cell_lib/store


The following combinations of defect (in target premitive)
and macro input lead to out-of-spec macro performance:

     Macro input         Defect

    2.500000e-05          9
    2.500000e-05          24

-----------------------------------
Number of total significant defects= 23
Number of faulty significant defects= 23
```

APPENDIX C

APPENDIX C

C.1 Macro Library of Current Copier With Target Cell, Opamp, and Specifications of (+/-)1.25e-6

```
Macro Library for macro 'Current Copier'
-----------------------------------------


Layout_area(um^2)= 41280

Performance1 = sig2(40)-sig2(80)
  lower bound = -1.25e-6
  upper bound = 1.25e-6


############################################################

Test Generation for TYPE 1 FAULT of Cell:
/home/ub/wangche4/ADT/adc_wey/IFA/fotmodel/cell_lib/ampadc


The following combinations of defect (in target premitive)
and macro input lead to out-of-spec macro performance:

     Macro input        Defect

    2.500000e-05          24
    2.500000e-05          12
    7.500000e-05          29

-----------------------------------
Number of total significant defects= 10
Number of faulty significant defects= 4


############################################################

Test Generation for TYPE 2 FAULT of Cell:
/home/ub/wangche4/ADT/adc_wey/IFA/fotmodel/cell_lib/ampadc
```

The following combinations of defect (in target premitive) and macro input lead to out-of-spec macro performance:

Macro input	Defect
2.500000e-05	15
0.000000e+00	35
2.500000e-05	35
5.000000e-05	35
7.500000e-05	35
1.000000e-04	35
2.500000e-05	17
2.500000e-05	18
5.000000e-05	18
7.500000e-05	18
1.000000e-04	18
2.500000e-05	23
2.500000e-05	47
5.000000e-05	47
7.500000e-05	47
1.000000e-04	47
2.500000e-05	8
5.000000e-05	8
7.500000e-05	8
1.000000e-04	8
2.500000e-05	5
5.000000e-05	5
7.500000e-05	5
1.000000e-04	5
2.500000e-05	20
5.000000e-05	20
7.500000e-05	20
1.000000e-04	20
2.500000e-05	46
5.000000e-05	46
7.500000e-05	46
1.000000e-04	46
2.500000e-05	42
5.000000e-05	42
7.500000e-05	42
1.000000e-04	42
2.500000e-05	1
5.000000e-05	1

7.500000e-05	1
1.000000e-04	1
2.500000e-05	45
5.000000e-05	45
7.500000e-05	45
1.000000e-04	45
2.500000e-05	32
5.000000e-05	32
7.500000e-05	32
1.000000e-04	32
0.000000e+00	37

Number of total significant defects= 32
Number of faulty significant defects= 18

C.2 Macro Library of Current Copier With Target Cell, Current Switch, and Specifications of (+/-)1.25e-6

Macro Library for macro 'Current Copier'

Layout_area(um^2)= 41280

Performance1 = sig2(40)-sig2(80)
  lower bound = -1.25e-6
  upper bound = 1.25e-6

##

Test Generation for TYPE 1 FAULT of Cell:
/home/ub/wangche4/ADT/adc_wey/IFA/fotmodel/cell_lib/switchN

The following combinations of defect (in target premitive)
and macro input lead to out-of-spec macro performance:

Macro input	Defect
1.000000e-04	16
0.000000e+00	8
2.500000e-05	8
5.000000e-05	8
7.500000e-05	8
1.000000e-04	8
0.000000e+00	5
2.500000e-05	5
5.000000e-05	5
7.500000e-05	5
1.000000e-04	5

Number of total significant defects= 4
Number of faulty significant defects= 4

```
############################################################

Test Generation for TYPE 2 FAULT of Cell:
/home/ub/wangche4/ADT/adc_wey/IFA/fotmodel/cell_lib/switchN


The following combinations of defect (in target premitive)
and macro input lead to out-of-spec macro performance:

     Macro input          Defect


-----------------------------------
Number of total significant defects= 2
Number of faulty significant defects= 0


############################################################

Test Generation for TYPE 3 FAULT of Cell:
/home/ub/wangche4/ADT/adc_wey/IFA/fotmodel/cell_lib/switchN


The following combinations of defect (in target premitive)
and macro input lead to out-of-spec macro performance:

     Macro input          Defect

    0.000000e+00           17
    2.500000e-05           17
    5.000000e-05           17
    7.500000e-05           17
    1.000000e-04           17
    0.000000e+00           4
    2.500000e-05           4
    5.000000e-05           4
    7.500000e-05           4
    1.000000e-04           4

-----------------------------------
Number of total significant defects= 5
Number of faulty significant defects= 3
```

C.3 Macro Library of Current Copier With Target Cell, Voltage Switch, and Specifications of (+/-)1.25e-6

```
Macro Library for macro 'Current Copier'
----------------------------------------


Layout_area(um^2)= 41280

Performance1 = sig2(40)-sig2(80)
  lower bound = -1.25e-6
  upper bound = 1.25e-6


############################################################

Test Generation for TYPE 1 FAULT of Cell:
/home/ub/wangche4/ADT/adc_wey/IFA/fotmodel/cell_lib/switchx


The following combinations of defect (in target premitive)
and macro input lead to out-of-spec macro performance:

     Macro input         Defect

    2.500000e-05          24
    5.000000e-05          24
    1.000000e-04          24
    0.000000e+00          11
    2.500000e-05          11
    5.000000e-05          11
    7.500000e-05          11
    1.000000e-04          11

-----------------------------------
Number of total significant defects= 2
Number of faulty significant defects= 2

############################################################

Test Generation for TYPE 2 FAULT of Cell:
/home/ub/wangche4/ADT/adc_wey/IFA/fotmodel/cell_lib/switchx
```

The following combinations of defect (in target premitive)
and macro input lead to out-of-spec macro performance:

Macro input	Defect
1.000000e-04	27

Number of total significant defects= 1
Number of faulty significant defects= 1

##########

Test Generation for TYPE 3 FAULT of Cell:
/home/ub/wangche4/ADT/adc_wey/IFA/fotmodel/cell_lib/switchx

The following combinations of defect (in target premitive)
and macro input lead to out-of-spec macro performance:

Macro input	Defect
1.000000e-04	29
0.000000e+00	33
1.000000e-04	33
0.000000e+00	15
2.500000e-05	15
5.000000e-05	15
7.500000e-05	15
1.000000e-04	15

Number of total significant defects= 6
Number of faulty significant defects= 6

##########

Test Generation for TYPE 4 FAULT of Cell:
/home/ub/wangche4/ADT/adc_wey/IFA/fotmodel/cell_lib/switchx

The following combinations of defect (in target premitive)

and macro input lead to out-of-spec macro performance:

Macro input	Defect
1.000000e-04	8
1.000000e-04	20
5.000000e-05	13
7.500000e-05	13
1.000000e-04	13

Number of total significant defects= 14
Number of faulty significant defects= 3

C.4 Macro Library of Current Copier With Target Cell, Storage Element, and Specifications of (+/-)1.25e-6

```
Macro Library for macro 'Current Copier'
-----------------------------------------


Layout_area(um^2)= 41280

Performance1 = sig2(40)-sig2(80)
  lower bound = -1.25e-6
  upper bound = 1.25e-6


############################################################

Test Generation for TYPE 1 FAULT of Cell:
/home/ub/wangche4/ADT/adc_wey/IFA/fotmodel/cell_lib/store


The following combinations of defect (in target premitive)
and macro input lead to out-of-spec macro performance:

     Macro input         Defect

    2.500000e-05           9
    2.500000e-05           24

-------------------------------------
Number of total significant defects= 23
Number of faulty significant defects= 23
```

REFERENCES

1. R. Mehtani, B. Atzema, M. De Jonghe, R. Morren, G. Seuren, and T. Zwemstra, "MixTest: A mixed-Signal Extension to a Digital Test Systems," Proc. International Test Conference, pp. 945-952, 1993.

2. A. Mastsuzawa, "Low-Voltage and Low-Power Circuit Design for Mixed Analog/ Digital Systems in Portable Equipment," IEEE Journal of Solid-State Circuits, Vol.29, No.4, pp.470-480, April 1994.

3. M. Sachdev, "A Realistic Defect Oriented Testability Methodology for Analog Circuits," Journal of Electronic Testing: Theory and Applications, No.6, pp.265-276, 1995.

4. C.L. Wey and R. Saeks, "On the Implementation of an Analog ATPG: The Linear Case", IEEE Trans. on Instrumentation and Measurement, Vol. IM-34, pp.277-284, 1985.

5. R.-W. Liu, *Testing and Diagnosis of Analog Circuits and Systems*, North-Holland, 1991.

6. L. Milor and A. Sangiovanni-Vincentelli, "Minimizing Production Test Time to Detect Faults in Analog Circuits," IEEE Trans. on Computer-Aided-Design, Vol.13, pp.706-813, June 1994.

7. T.W. Williams, *VLSI Testing*, North-Holland, 1986.

8. V. Visvanathan, "Testing of Analog Integrated Circuits," Chapter 9, pp.235-250, in *Testing and Diagnosis of Analog Circuits and Systems*, edited by R.-W. Liu, North-Holland, 1991.

9. C.P. Wang and C.L. Wey, "Efficient Defect-Oriented Testability Design Methodologies for Analog/Mixed-Signal Integrated Circuits," Proc. 3rd IEEE International Mixed-signal Testing Workshop, pp.68-74, Seattle, June 1997.

10. C.L. Wey, "Concurrent Error Detection in Current-Mode A/D Converter," Electronics Letters. Vol.27, No.25, pp.2370-2372, December 1991.

11. S. Sahli, "Test Generation and Concurrent Error Detection in Current-Mode A/D Converters," M.S. Thesis, Department of Electrical Engineering, Michigan State University, May 1992.

12. S. Krishnan, S. Sahli, and C.L. Wey, "Test Generation and Concurrent Error Detection in Current-Mode A/D converters," Proc. IEEE International Test Conference (ITC), Baltimore, MD., pp. 312-320, September 1992.

13. C.L. Wey, S. Krishnan, and S. Sahli, "Design of Concurrent Error Detectable Cur-

rent-Mode A/D converters for Real-time Applications," Analog Integrated Circuits and Signal Processing, No.4, pp.65-74, July 1993.

14. S. Krishnan, "Design and Test of Current-Mode Signal Processing Circuits," Ph.D. Disseertation, Department of Electrical Engineering, Michigan State University, August 1993.

15. C.L. Wey, S. Krishnan, and S. Sahli, "Test Generation and Concurrent Error Detection in Current-Mode A/D Converters," IEEE Trans. on CAD, Vol. 14, No.10, pp. 1191-1198, October 1995.

16. C.L. Wey, "Built-in Self-Test (BIST) Design of Current-mode Algorithmic A/D Converter" IEEE Trans. on Instrumentation and Measurement, Vol.IM-46,No.3, pp.667-671, June 1997.

17. J.P. Shen, W. Maly, and F.J. Fergruson, "Inductive Fault Analysis of MOS Integrated Circuits," IEEE Design and Test of Computers. Vol.2, pp.13-26, 1985.

18. R. Huang and C.L. Wey, "Simple Low-Voltage, High-speed, High-Linearity V-I Converter with S/H for Analog Signal Processing Applicatiosn," IEEE Trans. on Circuits and Systems. Part II. Analog and Digital Signal Processing. Vol.43, No.1, pp.52-55, January 1996.

19. R. Huang and C.L. Wey, "Design of High-speed, High-accuracy Current Copiers for Low-Voltage Analog Signal Processing Applications," IEEE Trans. on Circuits and Systems, Part II. Analog and Signal Processing, Vol.143, No.12, pp.836-839, December 1996.

20. R. Huang and C.L. Wey, "A High-performance CMOS Oversampling Current Sample/Hold (S/H) Circuit Using Feedforward Approach." accepted to appear in IEEE Trans. on Circuits and Systems, Part II. Analog and Digital Signal Processing.

21. S.J. Daubert, D. Vallancourt, and Y.P. Tsivids, "Current Copier Cells," Electronics Letters, Vol.24, No.25, pp.1560-1562, December 1988.

22. C. Toumazou, J.B. Hughes, and N.C. Battersby, *Switched-Currents: An analogue technique for digital technology*, London: Peter Peregrinus Ltd, 1993.

23. D. G. Naim and C. S. Salama, "A Ratio-Independent Algorithmic Analog-to-digital Converter Combining Current Mode and Dynamic Techniques," IEEE Trans. on Circuits and Systems, Vol.37, No.3, pp.319-325, March 1990.

24. A. Balivada and J. Abraham, "Fault Modeling and Fault Simulation of Analog and Mixed-Signal Circuits: A Tutorial," 2nd IEEE International Mixed signal Testing Workshop, Quebec City, Canada, May 1996.

25. G. Devarayanadurg and M. Soma, "Analytical Fault Modeling and Static Test Generation for Analog ICs," Proc. IEEE Int'l Conference on Computer-Aided Design, Nov. 1994.

26. R. J. A. Harvey, A. M. D. Richardson, E. M. J. G. Bruls and K. Baker, "Analogue Fault Simulation Based on Layout Dependent Fault Models," Proc. Int'l Test Conf., IEEE CS Press, 1994, pp.641-649.

27. A. Meixner and W. Maly, "Fault Modeling for the Testing of Mixed Integrated Circuits," Proc. IEEE International Test Conference, 1991.

28. H. Walker and S.W. Director, "VLASIC" A Catastrophic Fault Yield Simulator for

Integrated Circuits," IEEE Trans. on Computer-Aided-Design, No.5, October 1986.

29. C.P. Wang and C.L. Wey, "Test Generation of Switched-Current A/D Converters," 2nd IEEE International Mixed Signal Workshop, Quebec City, Canada, pp. 98-103, May 1996.

30. C.-P. Wang and C.L. Wey, "Fault Macromodel for Switches in Switched-Current Circuits," Accepted to appear in International Journal of Circuit Theory and Applications.

31. C.L. Wey, "Built-In Self-Test (BIST) Design of Current-mode Algorithmic A/D Converters," accepted to appear in IEEE Trans. on Instrumentation and Measurement.

32. E.J. McCluskey, "Built-In Self-Test Technique," IEEE Design and Test of Computers, Vol.2, No.2, pp.21-28, April 1985.

33. P.P. Fasang, "Analog/digital ASIC Design for Testability", IEEE Trans. on Industrial Electronics, Vol.36, No.2, pp.219-226, May 1989.

34. K.D. Wagner and T.W. Willams, "Design for Testability of Analog/Digital Networks," IEEE Trans. on Industrial Electronics, Vol.36, No.2, pp.227-230, May 1989.

35. C.L. Wey, "Built-In Self-Test (BIST) Structure for Analog Circuit Fault Diagnosis," IEEE Trans. on Instrumentation and Measurement, Vol.39,No.3, pp.517-521, June 1990.

36. C.L. Wey and S. Krishnan, "Built-In Self-Test (BIST) Structures for Analog Circuit Fault Diagnosis with Current Test Data," IEEE Trans. on Instrumentation and Measurement, pp.535-539, August 1992.

37. M. Soma, "Structure and Concepts for Current-based Analog Scan," Proc. CICC, pp.517-520, 1995.

38. B.R. Wilkins, S. Oresjo, and B.S. Suparjo, "Towards a Mixed-Signal Testability Bus Standard P1149.4," Proc. European Test Conference, pp.58-65, 1993.

39. C.-P. Wang, A.A. Hatzopoulos, and C.L. Wey, "A Test Paradigm for Analog and Mixed-signal Circuits and Systems," Proc. IEEE International Symposium on Circuits and Systems, Atlanta, GA, Vol. III, pp.194-197, May 1996.

40. O. Ohletz, "Hybrid Built-in Self-Test (HBIST) for Mixed Analogue/Digital Integrated Circuits," Proc. European Test Conference, pp.307-316, 1991.

41. A.A. Hatzopoulos, S. Siskos, and J. M. Kontoleon, "A complete scheme of built-in self-test (BIST) structure for fault diagnosis in analog circuits and systems," IEEE Trans. on Instrumentation and Measurement, Vol. 42, pp. 689-694, June 1993.

42. J.L. Huertas, A. Rueda, and D. Vazquez, "Testable Switched-Capacitor Filters," IEEE Journal of Solid-State Circuits, Vol.28, pp.719-724, July 1993.

43. L.T. rtz, "Built-in Self-Test Structures for Mixed-Mode Circuits," IEEE Trans. on Instrumentation and Measurement, Vol.42, pp.25-29, Feb. 1993.

44. K. Arabi, B. Kaminska, and J. Rzeszut, "A new Built-In Self-Test Approach for Digital-to-Analog and Analog-to-Digital Converters," Proc. ICCAD, pp.491-494, 1994.

45. B. Vinnakota, and R. Harjani, "The Design of Analog Self-checking Circuits," IEEE

International Conference on VLSI Design, 1994.

46. S. Mir, V. Kolarik, M. Lubaszewski, C. Niclsen, and B. Courtois, "Built-in Self-Test and Fault Diagnosis of Fully Differentiable Analogue Circuits," Proc. ICCAD, pp.486-490, 1994

47. M. Lubaszewski, M. Salvador, and L. Pulz, "A Multifunctional Test Structure for Analog BIST," IEEE International Mixed signal Testing Workshop, Quebec City, Canada, pp.239-244, May 1996.

48. K. Damm and W. Anheier, "HBIST Using Multifrequent Test Stimuli," IEEE International Mixed signal Testing Workshop, Quebec City, Canada, pp.245-249, May 1996.

49. A. Chatterjee, B.C. Kim, and N. Nagi, "DC Built-In Self-Test for Linear Analog Circuits," IEEE Design and Test of Computers, pp.26-33, Summer 1996.

50. C.-P. Wang and C.L. Wey, "Test Generation of Analog Switched-Current Circuits," Proc. Asian Test Symposiums, Taiwan, pp. 376-381, November 1996.

51. C.-P. Wang and C.L. Wey, "Efficient Testability Design Methodolgoies for Mixed-Signal/Analog Integrated Circuits," Proc. 3rd IEEE International Mixed Signal Testing Workshop, Seattle, WA, pp.68-74, June 1997.

52. C.-Y. Wu, C.-C. Chen, and J.-J Cho, "A CMOS Transistor-Only 8-b 4.5Ms/s Pipelined Analog-to-Digital Converter Using Fully-Differential Current-Mode Circuit Techniques," IEEE Journal of Solid-State Circuits, Vol.30, pp.522-532, May 1995.

53. D. A. Freitas and K. W. Current, "CMOS current comparator circuit," Electronics Letters, vol.19, no.17, pp.695-697, Aug. 1983.

54. H. Traff, "Novel approach to high speed CMOS current comparator," Electronics Letters, vol.28, no.3, pp.310-312, Jan. 1992.

55. A. Tang and C. Toumazou, "High performance CMOS current comparator," Electronics Letters, vol.30, no.1, pp.5-6, Jan. 1994.

56. J. Carreira and J. Franca, "High-speed CMOS current comparators," Proc. IEEE International Symposiums on Circuits and Systems, pp.731-734, 1994.

57. G. Palmisano and G. Palumbo, and S. Pennisi, "A High-Accuracy, High-Speed CMOS Current Comparator," Proc. IEEE International Symposiums on Circuits and Systems, 1994.

58. C.-Y. Wu, C.-C. Chen, M.K. Tsai, and C.-C. Cho, "A 0.5 μA Offset-Free Current Comparator For High Precision Current-Mode Signal Processing," Proc. International Symposiums on Circuits and Systems, pp.1829-1832, 1991.

59. G. Palmisano and G. Palumbo, "Offset-compensated low power current comparator," Electronics Letters, vol.30, no.20, pp.1637-1639, Sept. 1994.

60. G. Palmisano and G. Palumbo, "High Performance CMOS Current Comparator Design," IEEE Trans. on Circuit and Systems-II: Analog and Digital Signal Processing, vol.43, no.12, Dec. 1996.

61. Wang, C.-P., and Wey, C.L., "High-Accurate CMOS Current Comparator," accepted to 40th Midwest Symp. on Circuits and Systems, Davis, CA, August 1997.

62. M. Waite and S. Prata, *C: Step-by-Step, SAMS*, 1994.

63. M. H. Rashid, *SPICE FOR CIRCUITS AND ELECTRONICS USING PSPICE*, Prentice Hall, 1995.

64. Robert D. Strum and Donald E. Kirk, *Contemporary Linear Systems Using MATLAB 4.0*, PWS Publishing Company, 1996.

65. Magic User's Manual, DEC, 1993.

66. Ledit User's Manual, Turner, 1996.

67. C. P. Wang and C. L. Wey, *User's Manual of PETOMIC*, EE Dept., Michigan State University, 1997.