CMOS INSTRUMENTATION FOR ELECTROCHEMICAL BIOSENSOR ARRAY MICROSYSTEMS

By

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ABSTRACT

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Understanding the structure and function of proteins has become increasingly important since the completion of the Human Genome Project and the sequencing of several other important genomes. In recent years, lab-on-a-chip systems have introduced some new capabilities for protein analyses. Rapid progress in the field of microsystems, miniaturized devices, combining sensor and electronics, facilitates a new generation of miniaturized biosensor arrays utilizing silicon CMOS chips that acquire and process bio-electrochemical signals. Such biosensor array microsystems permit improved sensitivity, measurement throughput and cost per assay. This thesis research addresses the design and development of high performance electrochemical instrumentation circuits that enable simultaneous characterization of multiple protein interfaces in a high throughput chip-scale biosensor arrays microsystem. A CMOS amperometric biosensor readout circuit with current resolution of 1pA has been developed. Furthermore, a new compact, low power, 100fA current resolution impedance analysis circuit that utilizes mixed-mode signal processing to extract real and imaginary impedance components has been developed and tested with an on-chip protein interface. Moreover, to realize a multi-protein array of sensors with different instrumentation needs, a hardware efficient CMOS electrochemical circuit has been designed to achieve both amperometric and impedimetric measurement while sharing hardware source. Finally, by integrating an

understanding of both protein assays challenges and microelectronics design limitations, a novel 1000-element array instrumentation architecture that permits rapid high-throughput characterization of membrane proteins with single protein resolution has been designed. The CMOS instrumentation circuitry developed in this thesis research could significantly advance proteomics research and progress in characterizing newly sequenced genomes.

Dedicated to my family

ACKNOWLEDGEMENTS

The work presented in this thesis would not have been possible without the support, contribution, and encouragement of many individuals that I have had the privilege of interacting with during my stay at Michigan State University. Indeed this is now a unique opportunity to acknowledge them, even though in a very small way.

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My utmost gratitude, love and affection belong to my family. My parents always unconditionally love and support me and I thank them for everything they have given me. I would like to thank my husband, Yang Liu, who accompanied me through the past years at Michigan State University. This thesis is dedicated to them.

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Chapter 1 Introduction

1.1 Electrochemical Protein Biosensor

Proteins are vital entities in human cells and are involved in nearly all body functions both in healthy and diseased individuals [1-3]. Proteins can support the skeleton, control senses, move muscles, digest food, fight infections and process emotions. Understanding the structure and function of gene products, that is proteins, has been increasingly emphasized for the completion of the Human Genome Project and the sequencing of several other important genomes. Because proteins are the targets for virtually all pharmaceutical drugs and for most diagnostics [1], proteins can be used in detecting disease and creating new treatments for health problems such as cancer, cardiovascular and neurological disorders. According to American Cancer Society report, about 1,638,910 new cancer cases are expected to be diagnosed and about 577,190 Americans are expected to die of cancer in 2012 (more than 1,500 people a day) [4]. The deaths could potentially be prevented by better understanding the role of proteins in biological operations.

Protein characterization (also referred to as proteomics) and sensing are two directions in proteins study. Protein characterization is analyzing protein sequence, structure and post-translational modifications [5]. Protein characterization has been used widely in drug discovery, development of biosensors, clinical and forensic analysis [6-9]. In general, protein characterization is laboratory research, which requires high resolution

detector (or instrumentation). Sometimes, the instrumentation even needs continue record the proteins kinetic characterization. Protein sensing is detection the concentration of target proteins. There is a direct correlation between protein levels and disease states in human serum, which makes protein as an attractive target for sensors and diagnostics [10]. Compared with characterization, sensing emphasizes real-time detection.

Techniques for protein sensing and characterization are generally divided into two groups, label and label-free. The most applied label technique is enzyme-linked immunosorbent assay (ELISA), which is complex, time-consuming and laborious. All the optical label techniques require expensive free-space optical equipment and difficult alignment of all the components. To overcome these drawbacks, label-free techniques have been introduced. Surface Plasmon resonance (SPR), quartz crystal microbalance (QCM), and electrochemical are the main techniques used in proteins interactions measured. Compared with SPR and QCM, electrochemical biosensors provide more rapid, simple and low-cost on-field detection [11]. Electrochemical biosensor is a molecular sensing device that intimately couples a biological recognition element to an electrode transducer. The principle for electrochemical biosensor transducers is that many chemical reactions produce or consume ions or electrons, causing some change in the electrical properties of the solution, which can be sensed as measuring parameters.

Recently, protein sensing and characterization fields are moving towards point-of care diagnostics [12]. Point-of-care diagnostics play an important role in bridging the gap between centralized laboratory diagnostics and peripheral healthcare service providers. This is particularly true in infectious diseases such as HIV/AIDS and H1N5 where early detection is imperative to improve disease outcome [13]. Electrochemical biosensors are

good candidates for point-of-care devices due to their easy integration and miniaturization. Now, the trend of point-of-care devices is to combine with array technique, which allows rapid and quantitative detection of a wide range of biomolecules [14, 15]. These trends suggest that electrochemical biosensors could have a major impact on future diagnostic (e.g., point-of-care devices) and therapeutic approaches (e.g., personalized medicine).

1.2 Miniaturized Protein Array Biosensor

A miniaturized, high throughput array takes advantage of the fact that a large number of targets can be analyzed in parallel measurements with low sample consumption. The reduction of sample volume is of great importance for all applications in which only minimal amounts of samples are available. The volume of the liquids at the micro scale is also great in molecular concentrations control and interactions [16]. Parallel measurements reduce the assay time significantly. Furthermore, it is possible to perform comparative analyses of several different samples within a single array chip. For example, in medical research, all relevant immune diagnostic parameters of interest can be analyzed in parallel, which saves cost and time.

Microfluidics (or lab-on-a-chip) provide an attractive platform for array applications because microfluidics can automatically control the liquid flow for each bio-cell individually. The automation of chemical processing controlled by microfluidics also reduces errors caused by manual operation [17]. The optical DNA array associated with microfluidics shows the advantages of less sample usage and reduced incubation time [18]. However, the optical method still needs expensive optical instrumentation, which

limits its point-of-care application. Recently, microfluidic electrochemical hybridization techniques have shown substantial successes in point-of-care diagnostic and therapeutic approaches [19]. Electrochemical biosensors require electronic instrumentation, and most modern instrumentation relies on complementary metal–oxide–semiconductor (CMOS) microelectronics technology due to the success of CMOS in integrated circuits (IC) industry. CMOS instruments are low-cost and easily miniaturized devices, which is well suited for point-of-care diagnostic.

Traditional lab-on-a-chip devices do not include instrumentation electronics. As such, when microfluidics technologies are integrated with sensor array approaches, a wiring bottleneck to physically separated electronics is encountered. Thus, there are challenges inherent to forming hundreds of individually measurable protein elements on a single substrate.

The Advanced MicroSystems and Circuits (AMSaC) lab at Michigan State has been developing new approaches to combine microfluidics and CMOS instrumentation into one miniaturized system (called lab-on-CMOS), wherein no wires are required between protein interface and instrumentation electronics. In the proposed platform, a CMOS instrumentation chip acts as the substrate of the microsystem. An array of gold electrodes fabricated post-CMOS directly on the surface of the chip are connected through overglass contact openings to the underlying CMOS electronics. To insulate surface metal routing and define size-adjustable openings over individual electrodes, a post-CMOS package is applied after metallization. This insulation layer also planarizes the surface and provides an interface to a variety of possible fluid handling schemes, including microfluidics illustrated in Figure 1-1. The direct, on-chip, electrical

connection of electrodes to the instrumentation improves the signal to noise ratio due to the elimination of the external wiring and immunity from environmental interference. This noise reduction permits highly sensitive circuits to measure the responses of miniature biosensors, allowing a high-density sensor array within the small platform of a CMOS chip.

1.3 Challenges for CMOS Instrumentation

The challenges in forming miniaturized and high throughput array biosensors can be organized into three main categories: biointerface formation, CMOS instrumentation, and physical integration of all system components including electronics and microfluidics. Each of these presents complex and challenging problems to solve. While the biointerface formation and physical integration challenges are being explored by other researchers, the work under this thesis will focus on the challenges highlighted below for implementing CMOS instrumentation necessary for next-generation electrochemical biosensor arrays.

Limited area is the first challenge of CMOS instrumentation for high throughput application. All the electrochemical detection circuits have to be integrated in a less than 1 cm^2 chip. To achieve one chip reading hundreds or even thousands of protein elements in parallel, the detection circuits are needed to be extremely hardware efficient.

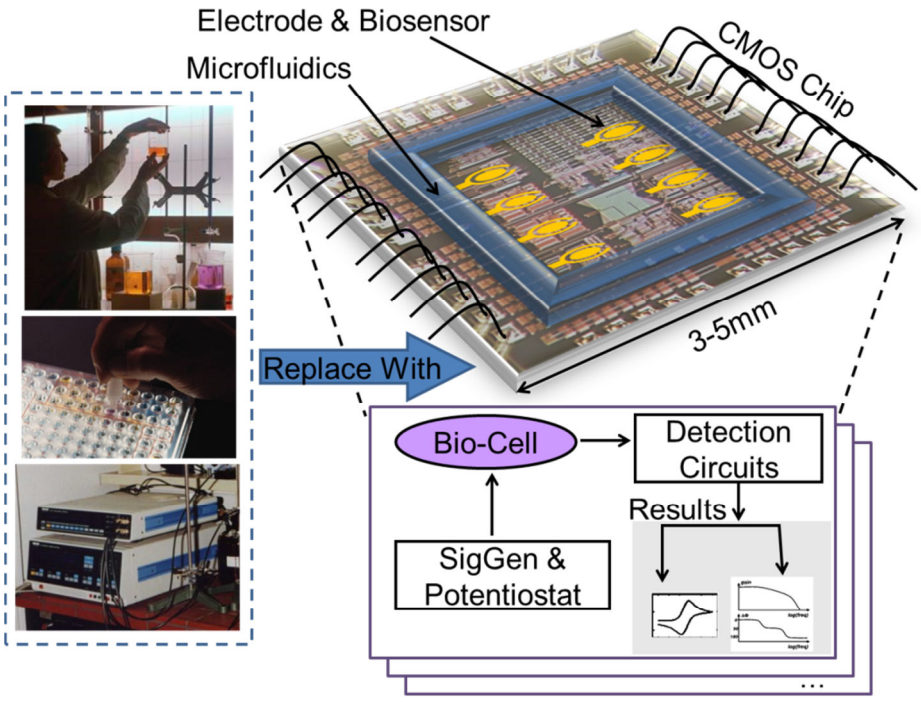


Figure 1-1. Conceptual illustration of a CMOS electrochemical biosensor array microsystem use in a liquid environment (For interpretation of the references to color in this and all other figures, the reader is referred to the electronic version of this dissertation).

In general, multiple electrochemical techniques are required to perform protein characterization or sensing. This creates an expectation that single chip instrumentation for next-generation biosensor arrays must be able to achieve multi-function electrochemical measurement. Thus, another significant challenge this thesis research must address is how to implement highly integrated multi-function circuits in limited area.

As biosensors advance to high throughput arrays, they produces a tremendous load of raw data. This, in turn, creates a requirement for the instrumentation that must be able

to acquire, process, and communicate results for many sensor elements in parallel. At the same time, the power must be minimized to support portable applications and ensure no local heating that could degrade on-chip biointerfaces. The handling of this high data density while maintaining low power consumption is inherently challenging.

Miniaturization of biosensor arrays into the chip-scale platform shown in Figure 1-1 requires the size of on-chip electrodes to be very small to fit up to hundreds of electrodes on the protein array chip. This miniature electrode size causes the biosensor output signals to be extremely weak, on the order of femto to pico amperes (~fA – pA). Furthermore, some of the most interesting and important bio-reaction responses are inherently weak. For example, single molecule detection is considered to be the "holy grail" of high resolution biosensing. However, responses from single molecules are naturally very small and measuring them is beyond the capability of most existing instruments. Therefore, acquiring single molecule reaction signals is one of the main challenges for development of next-generation high throughput protein array microsystems.

1.4 Dissertation Goals

The primary goal of this research is to develop CMOS instrumentation electronics that enhance the evolution of protein biosensors toward miniaturized high throughput array microsystems. Specifically, this thesis research seeks to:

- Develop CMOS electrochemical circuits with state-of-the-art performance in terms of hardware efficiency, power consumption and bio-reaction current readout resolution.
- Efficiently integrate multi-mode electrochemical techniques onto a single chip for protein characterization and sensing under widely varied controlled conditions.
- Develop electrochemical instrumentation circuitry that addresses the many challenges in forming high throughput chip-scale biosensor arrays with simultaneous characterization of multiple bio-interfaces.

These proposed CMOS instrumentations will establish new biological-to-silicon communication pathways that enable future advances in many areas of microsensor technology and biomedical instruments.

1.5 Outline

In this thesis, Chapter 2 covers the background of electrochemical biosensor components, detection methods, and different structures of electrochemical CMOS instrumentation are reviewed. A low noise amperometric instrumentation chip is introduced in Chapter 3 and test results with a cytochrome protein interface are shown. Chapter 4 introduces a compact, low power impedance spectroscopy circuit that was developed to characterize tethered lipid bilayer membranes. Chapter 5 presents a novel hybrid multifunctional readout circuit and test results from a Herceptin biosensor. Chapter 6 presents a CMOS electrochemical instrumentation circuit for high throughput

membrane proteins characterization. Chapter 7 summarizes the thesis work and contributions, and it outlines future work related to this research.

Chapter 2 Background

2.1 Electrochemical Biosensor Introduction

2.1.1 Electrochemical biosensor components

An electrochemical biosensor is commonly composed of four components, as shown in Figure 2-1: analyte, bio-probe, transducer and instrumentation. The analyte is the target of interest, such as a specific type of protein, DNA, bacteria or tissue. The bio-probe is the element that provides the selective recognition capability for a target analyte. The transducer translates the biorecognition event into electrical signal. The typical transducer of an electrochemical biosensor is an electrode, which translates the chemically generated ions into a current or voltage. Instrumentation electronics serve to record the response current or voltage.

2.1.2 Transducer

In electrochemical biosensors, electrodes are the dominate transducer. The electrode can be made from metal, mixed metal oxide, carbon, graphite, or any other conductive material. Because bio-reactions occur in close proximity to the electrode surface, the study of the processes at the electrode-solution interface is crucial [20]. Two types of processes occur at the electrode-solution interface. When electron charge is transferred across the interface, the reactions is called as *faradic processes* and is

governed by Faraday's law. Processes that do not transfer charges cross the electrode-solution interface are called *nonfaradaic,* and these can generate electrode current when the potential, electrodes, or solution composition changes. For example, adsorption and desorption reactions are typical *nonfaradaic* processes.

2.1.3 Immobilization

Bio-probe interfaces are often immobilized onto a solid surfaces, especially in miniaturized biosensors. Adsorption, cross linking, covalent bonding, entrapment, encapsulation, etc. have all been used for binding to solids [21]. The selection of an appropriate immobilization method depends on the nature of the biological element, the type of transducer used, the physicochemical properties of the analyte, and the operating conditions for the biosensors. The most common methods for immobilization of bio-components are adsorption and covalent bonding. Physical adsorption of the bio-probe is based on van der Waals attractive forces. Covalent bonding is based on a reaction between the same terminal functional groups of the protein and reactive groups on the solid surface of the insoluble bed.

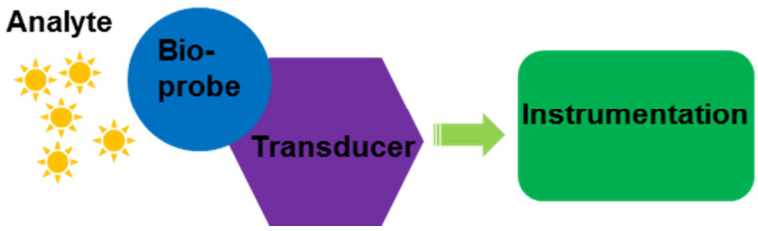


Figure 2-1. Common components of electrochemical biosensor.

2.2 Electrochemical Biosensor Techniques

Electrochemical biosensors can be classified according to the operating technique used to measure electrochemical changes during a biorecognition event. These classes have been popularly defined as potentiometric, amperometric, impedimetric and field-effect transistor (FET) biosensors [22]. Table 2-1 lists the typical biosensor electrochemical techniques for different types of bio-probes. From this table, we found that one bio-probe could be characterized by multiple electrochemical techniques. This leads to a future research direction for multi-mode electrochemical measurement.

2.2.1 Potentiometric biosensor

In potentiometric biosensors, the analytical information is obtained by converting the biorecognition events into a potential signal, which is proportional to the concentration of analyte [23]. The measured potential should be made at zero-current or quasi-equilibrium condition [24]. The most common potentiometric devices are pH electrodes; several other ion (F^-, I^-, CN^-, Na^+, K^+, Ca^{2+}, NH_4^+) selective electrodes are available. The potential differences between these indicator and reference electrodes are proportional to the logarithm of the ion activity, as described by the Nernst-Donnan equation [22]. Potentiometric biosensors have been used for antigen and DNA detection. The fundamental disadvantage of the potentiometric technique is that the double-layer charging effects are frequently larger and occur throughout the experiment [25].

Table 2-1. Types of bio-probes used in biosensors and their common electrochemical technique.

Bio-probe	potentiometry	amperometry	impedance	FET
enzymes	✓	✓	✓	✓
Membrane protein		✓	✓	
whole cells	✓	✓	✓	
antigen/antibody	✓	✓	✓	✓
plant or animal tissue	✓	✓	✓	

2.2.2 Amperometric biosensors

Amperometric biosensors are based on monitoring the current associated with oxidation and/or reduction of an electro-active species involved in the recognition process. In amperometric biosensor, a constant or ramp potential is applied on electrode-electrolyte interface. The applied potential serves as the driving force for the biorecognition process, and the response current directly relates to the analyte concentration. Amperometry is a common electrochemical detection method in immunosensors [26], enzyme biosensor [27] and pesticide monitoring [28]. Compared to potentiometry, amperometry has higher sensitivity and wider linear range [29].

2.2.3 Impedimetric biosensor

Impedimetric biosensors measure the electrical impedance of the electrode-electrolyte interface at equilibrium [30]. Impedimetric biosensors take advantage of the bio-interfacial characteristics, i.e., capacitance and resistance change, during biorecognition events. An impedimetric biosensor is created by imposing a small sinusoidal stimulus voltage (or current) of variable frequency and measuring the phase and/or amplitude change of the resulting current (or voltage) that contains information regarding biorecognition events. This technique is generally referred to as the impedance spectroscopy (IS) and has been employed in a variety of applications such as monitoring bilayer lipid membranes [31, 32], detecting small molecules of biological relevance [33, 34], measuring cell concentrations [35, 36]. Compared to potentiometric and amperometric biosensors, an important advantage of impedimetric biosensor is that the stimulus sinusoidal voltage is small (usually 5-10 mV in amplitude) and does not damage or disturb most bio-probe layers.

2.2.4 Ion-sensitive field effect transistor biosensor

Another method to measure ion concentrations in a solution utilizes ion-sensitive field effect transistors (ISFET). As illustrated in Figure 2-2, an ISFET operates in a manner similar to a MOSFET, where the current between source and drain terminals is proportional to the gate voltage that, for an ISFET, is set by reactions between analytes and bio-probes (immobilized on the gate) during biorecognition events [37]. ISFET biosensors have been developed for enzyme sensing [38], measuring antigen-antibody

bonding reactions [39] and DNA detection [40, 41], and immobilizing nanomaterials such as nanoparticles, nanotubes, and nanowires on the gate has been shown to improve sensitivity [42]. Unlike potentiometric, amperometric and impedimetric biosensors that use an electrode transducer, the ISFET's transducer is the gate oxide layer. As a result, ISFETs require unique instrumentation circuitry that is dissimilar to the other categories of electrochemical sensors. The remainder of this chapter will focus on biosensors with electrode transducers. For more information on the principles, applications and challenges of ISFET biosensors, the reader is referred to other sources [37, 43].

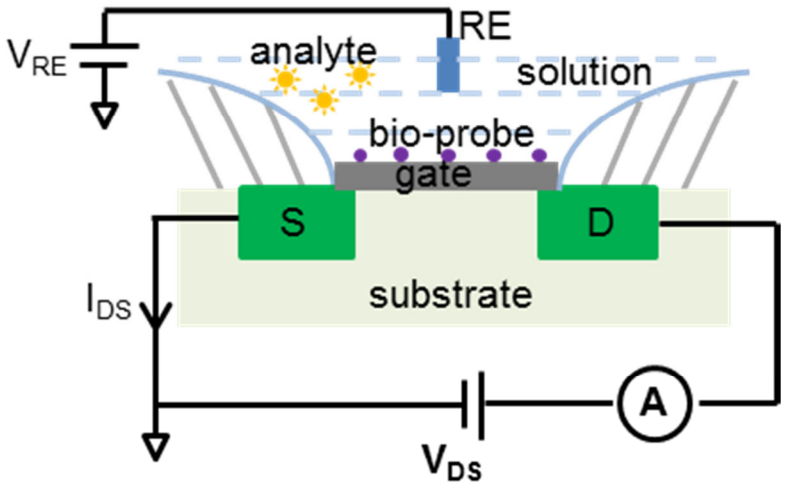


Figure 2-2. The structure of ISFET biosensor.

2.2.5 Electrode transducer

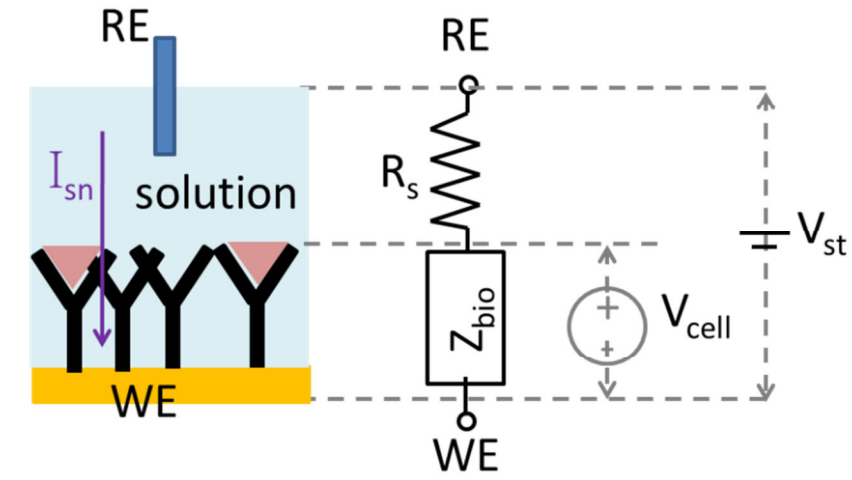
Electrochemical biosensors employ multiple electrode transducers to translate biorecognition responses into electrical signals. The electrode where electrochemical reaction of interest takes place is called the working electrode (WE). The electrode that

provides a stable and known potential is called the reference electrodes (RE). The simplest electrode system utilizes only these two electrodes. In such two-electrode systems, a known stimulus voltage, V_{st}, is applied between RE and WE. The resulting potential across the electrochemical cell's electrode-electrolyte interface, V_{cell}, is, ideally, equal V_{st} throughout the electrochemical reaction. However, as shown in Figure 2-3 (a), in addition to the electrode-electrolyte interface represented by impedance Z_{bio}, electrochemical cells inherently possess a solution resistance, R_s, representing the ion flow path through the electrolyte solution to an electrode. As a result, V_{cell} is always less than V_{st} because of voltage dropped across R_s, which is commonly referred to as the "IR drop". Because the IR drop cannot typically be known in advance and can change with environmental conditions, reaction kinetics, etc., it is generally considered to be an undesirable source of noise/error.

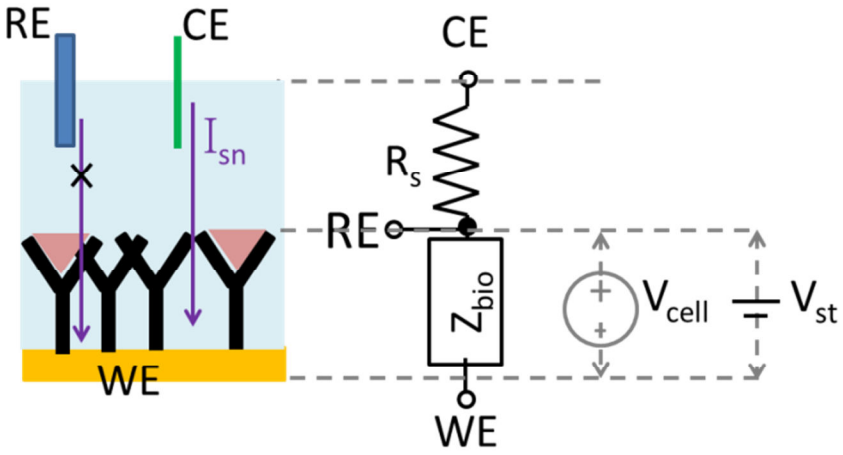
Although R_s cannot be entirely removed from an electrochemical cell, the negative effects of IR drop can be eliminated by adding a third electrode, called a counter electrode (CE), to the system. As shown in Figure 2-3(b), in a three electrode system, the stimulus voltage across Z_{bio} is established between RE and WE, and no current is allowed to flow through the RE terminal thus eliminating any IR drop. Instead, the response current is read through the CE where the IR drop will have no effect on the biosensor response current. Because of the performance advantages of eliminating the IR drop effect, three electrode systems are widely used in electrochemical biosensors. Note

that potentiometric sensors are generally measured at zero current, and impedimetric sensors generally have small signal AC currents with negligible IR drop. Thus, three electrode systems are especially useful with amperometric techniques (typically with redox reactions) where larger response currents are generally observed.

Biosensor interfaces with low turnover rates can result in low response currents and low sensitivity. For redox active bio-probes, the redox recycling effect can be utilized to electrochemically magnify the faradic current by increasing mass transport of the redox active species of interest. To utilize redox recycling in biosensors, four electrode electrochemical systems have been developed [25, 44-47]. Four electrode systems have one RE, one CE and two WEs with redox probes immobilized on both. They are ideally suited for micro-scale interdigitated electrode arrays where the close proximity of WEs enhances redox recycling. Because redox recycling is rarely used and only available with redox bio-probes, four electrode systems are not very common.



(a)



(b)

Figure 2-3. The equivalent circuit model of (a) a two electrode system and (b) a three electrode system.

2.3 Interface Circuitry for Electrochemical Biosensors

After electrode translating the biorecognition events to electronic domain, the electronic signals are measured by instrumentation. Instrumentation also provides a potential voltage for the electrode-electrolyte interface. CMOS process has been the most popular integrated circuit technology in recent decades, so most of the instrumentation for electrochemical biosensors is CMOS instrumentation.

CMOS instrumentation can be divided into four elements based on function: signal generator, potentiostat, readout circuit and signal processing. Signal generator generates various shapes of stimulus signals, such as triangle, constant potential, saw, and pulse etc. Potentiostat controls the biasing potential of electrodes. The readout circuit is developed to detect the response current/voltage. Signal processing block analyzes the data coming from the readout circuits. The structure of the CMOS instrumentation is shown in Figure 2-4. The signal generator and signal processing blocks are excluded from this paper, because these two blocks are not highly related to the electrode-electrolyte interface, and can be implemented by general commercial circuits. The potentiostat and readout circuit is discussed in detail in following sections.

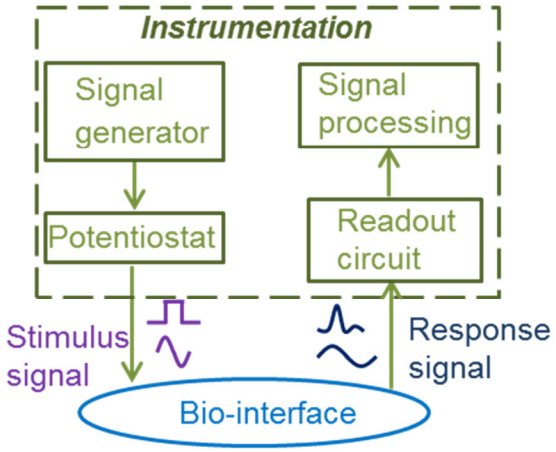


Figure 2-4. The structure of the instrumentation for electrochemical biosensors.

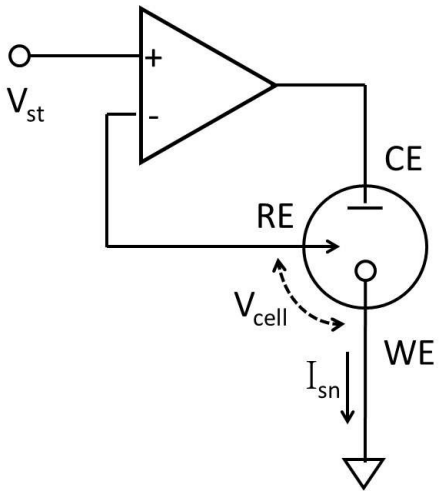
2.3.1 Potentiostat

In an electrochemical reaction, when V_{cell} reaches the analyte's redox potential, the biochemical reaction occurs, so it is critical to have circuits to set V_{cell} during measuring. The circuit served as providing accurate V_{cell} to the electrode-electrolyte interface is called the potentiostat.

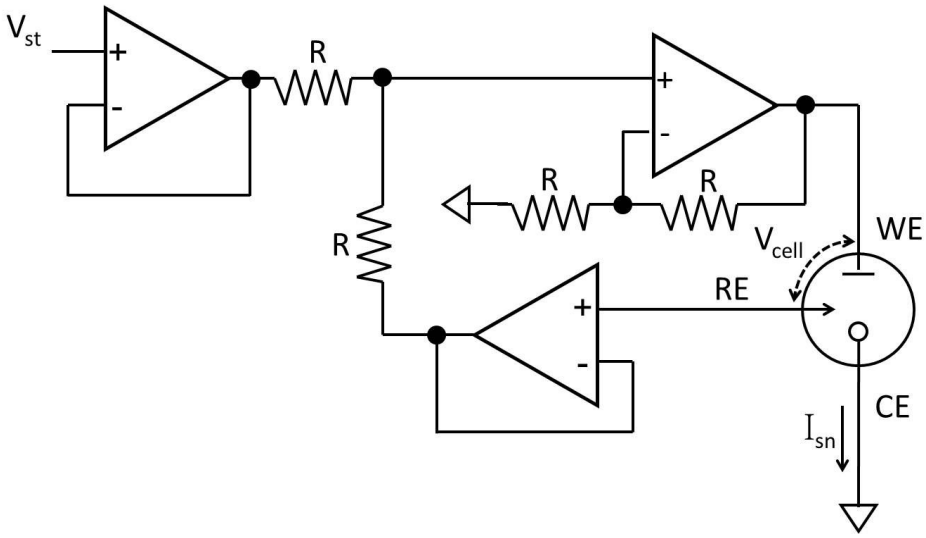
The first CMOS potentiostat was presented on 1987 for two electrodes amperometric chemical sensors [48], in which one operation amplifier achieves the potentiostat function. Due to the advantages of the three electrodes compared to two electrodes system, most of the modern potentiostats [49-57] are designed for three electrodes system.

There are three configurations of potentiostat in three electrodes system: ground WE; ground RE; and ground CE [51]. The first two configurations are electrically same;

thus, in fact, there are really only two configurations: ground WE and ground CE. The simplest ground WE potentiostat is implemented by one operational amplifier (OPA). The two inputs of the OPA connect to V_{st} and RE, respectively and WE connects to ground. V_{cell} equals V_{st} because of the inputs OPA having same potential. The output of the OPA connects to CE for providing current path from CE to WE. The schematic of the grounded WE potentiostat is shown in Figure 2-5 (a). Because the RE and WE voltages (related to ground) vary at the same time, more circuits are needed to make sure the voltage difference between RE and WE equaling to Vst, as shown in Figure 2-3. "A grounded CE potentiostat circuit is presented in Figure 2-5 (b) which is more complex than the circuit for the grounded WE, therefore nearly all potentiostats use the grounded WE structure [50, 53-57].



(a)



(b)

Figure 2-5. (a) 3-electrode potentiostat with grounded WE structure. (b) 3-electrode potentiostat with grounded CE structure

The potentiostats structures introduced above are single-ended potentiostats. The low power supply trend of CMOS process, however, limits the functionality of potentiostat because biosensors' redox potentials can be higher than the power supply. To solve this problem in low-voltage process, a fully-differential potentiostat was developed

to increase the output swing of potentiostat [50]. The fully-differential potentiostat as shown in Figure 2-6, is based on a fully-differential amplifier, OP3, which dynamically controls the RE and WE voltages. This developed fully-differential potentiostat doubles the Vcell output range in single-ended potentiostat [50].

2.3.2 Readout circuits

In electrochemical biosensor, the electrolyte response signals are detected by readout circuits. Because the potentiometric technique is barely used in biosensor, only current readout circuits for amperometric and impedimetric biosensors are introduced in this paper. Based on the characters of biosensing current, the current readout circuitry can be classified by DC and AC current readout.

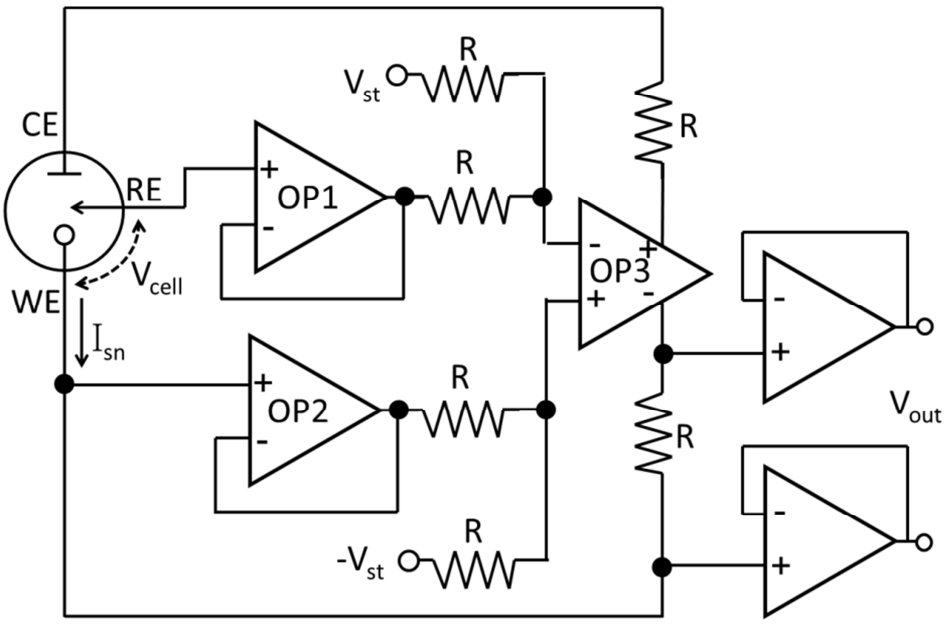


Figure 2-6. Fully-differential potentiostat. (adapted from [50])

2.4 DC Current Readout Circuitry

For amperometric biosensors, the biointerfaces response current is DC, so the readout circuits are DC current readout. In general, the amperometric readout circuit should provide wide current range, high resolution at interested bandwidth and allow measurement of bidirectional currents (sink/source). Numerous CMOS amperometric circuits have been introduced over the past decades with various functionality and performance to meet different applications demands [48, 54, 55, 58-64]. Basically, there are three structures for amperometric current readout circuits: resistive, capacitive and current conveyor current readout.

2.4.1 Resistive current readout circuits

The simplest way to readout the response current is to use a sense resistor. The resistive feedback current readout circuitry uses an operational amplifier with a feedback resistor to convert the biosensor sensing current I_{sn} to voltage, as shown in Figure 2-7. The biosensor sensing current I_{sn} can be calculated by

$$I_{sn} = -\frac{V_{out}}{R_f} \tag{2-1}$$

where R_f is the feedback resistance, V_{out} is the output voltage of the operational amplifier. The dynamic range of the current readout circuitry can be achieved by changing the R_f value. This resistor feedback structure is very simple to develop, however it does not fit for the low noise amperometric application because the feedback

resistor, R_f, generates significant thermal noise. That is the major drawback of this structure [65].

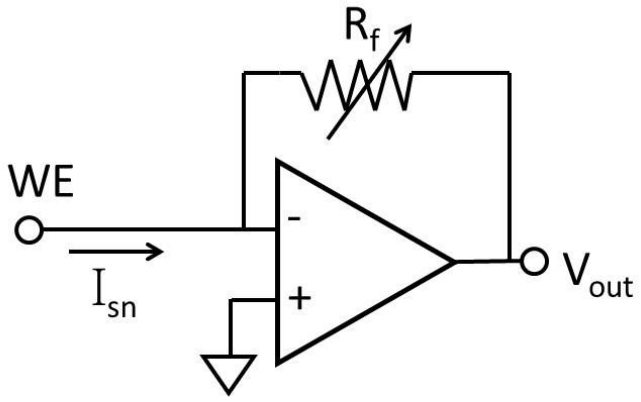


Figure 2-7. Resistive feedback current readout circuit.

2.4.2 Capacitive current readout circuits

To eliminate the thermal noise generated by the feedback resistor, capacitive feedback structure has been introduced [60, 61, 64, 66-69]. Detailed noise analysis of the resistive feedback and capacitive feedback structure was presented [65], in which claimed the capacitive feedback system provides better noise performance than the resistive feedback structure.

The basic structure of the capacitive feedback current readout is an integrator converting the input current to a voltage, as shown in Figure 2-8 [70]. The biosensor sensing current I_{sn} can be calculated by

$$V_{out} = \frac{1}{C_f}\int_0^T I_{sn}\,dt \tag{2-2}$$

where C_f is the feedback capacitor, T is the integration time, V_{out} is the output voltage of the operational amplifier.

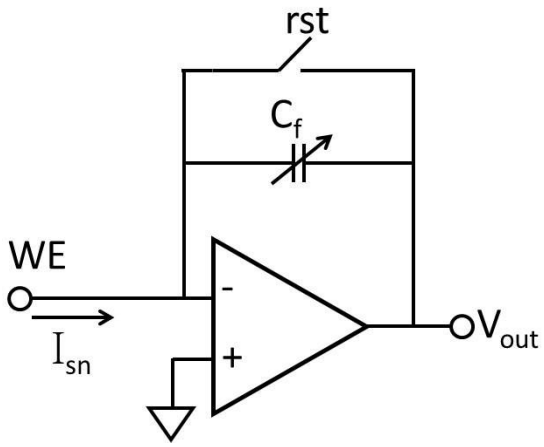


Figure 2-8. Capacitive feedback current readout circuit.

The performance of this capacitive feedback current readout circuit is degraded by the switching effect, which presents as offset errors (including clock feed through, charge injection, and KT/C noise). To eliminate the offset error, correlated double sampling (CDS) technique has been introduced in the capacitive feedback readout circuit [49]. CDS technique also can reduce the 1/f noise that is a significant noise source in DC readout circuitry. The CDS circuit structure is presented in Figure 2-9, where a switched-capacitor (SC) charge integrator converts the input current to a voltage. The voltage is sent to a programmable gain amplifier (PGA) with a gain of C_1/C_2, where C is a digitally programmable on-chip capacitor array. The output of the PGA is sampled and held and then fed to an analog-to-digital converter (ADC) after a low pass filter. The non-

overlapping clock signals for switches ph1, ph2 are generated by an on-chip clock generator block. The input current range can be adjusted to different biosensors through programmable selection of the clock frequency and the PGA gain. These programmable features can be used to calibrate sensors over time.

To reduce the effects of charging currents and currents due to undesired analyte, pseudo-differential amperometric readout circuits were developed [52, 71]. Two WEs are used instead of one. The schematic of pseudo-differential readout is presented in Figure 2-10, where the reading time controlled by switches S_n and S_p. By subtraction of the currents from WE_n and WE_p, nearly all parasitic currents can be canceled while preserving the analytical signal of interest [52].

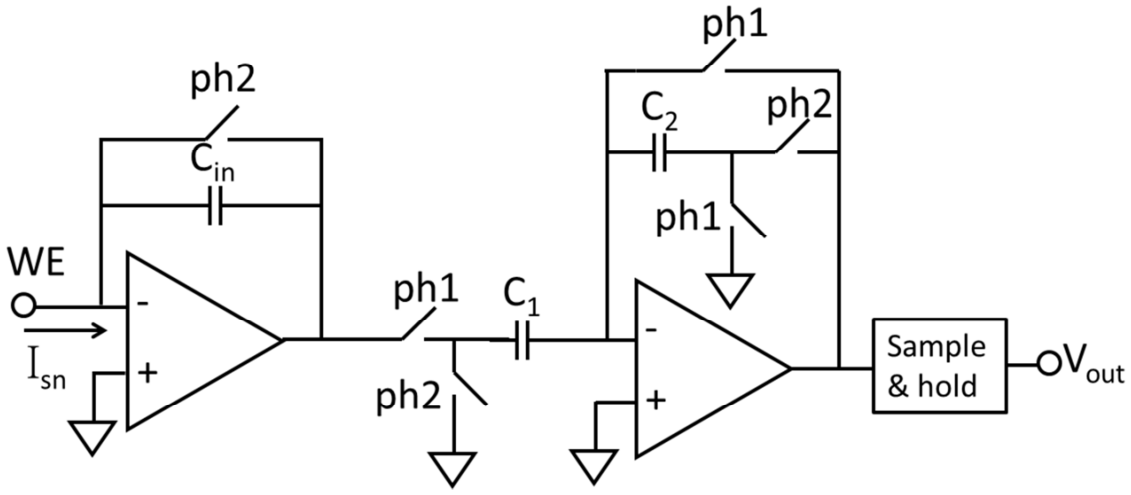


Figure 2-9 The structure of CDS circuit (adapted from [49]).

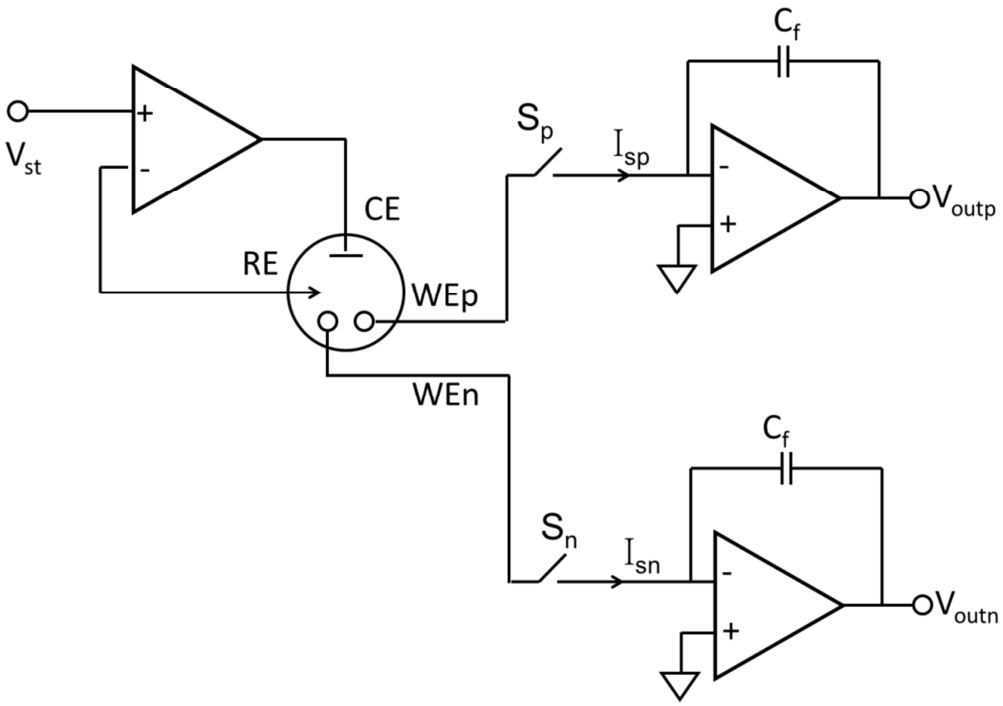


Figure 2-10. The structure of the pseduo-differential amperometry readout circuit (adapted from [52])

2.4.3 Current conveyor current readout circuits

Current conveyor structure is the third type of the amperometric current circuitry. Current conveyor is a current mode amplifier to amplify the input current eliminating the noise sources from the following stages [51, 61, 72, 73]. Figure 2-11 presents a schematic of a typical current conveyor used for measuring currents. The biosensor sensing current I_{sn} can be calculated by

$$\frac{I_{sn}}{I_{sn}^{*}} = \frac{(W/L)_1}{(W/L)_2} \tag{2-3}$$

where W/L is the transistor size. The current conveyor circuit performs decoupling and linear operations in current mode in the same way that the operational amplifier performs in voltage mode. One drawback of the current conveyor is a one current direction readout circuit, which is not suitable for bi-direction current applications. To overcome the one direction drawback, a pseudo bidirectional current conveyer with a DC offset current has been presented [72]. Its structure is presented in Figure 2-12. Compared to the capacitive and resistive feedback structure, the drawback of the current conveyor is the bias current noise can directly sum with the input current, which causes larger error [65].

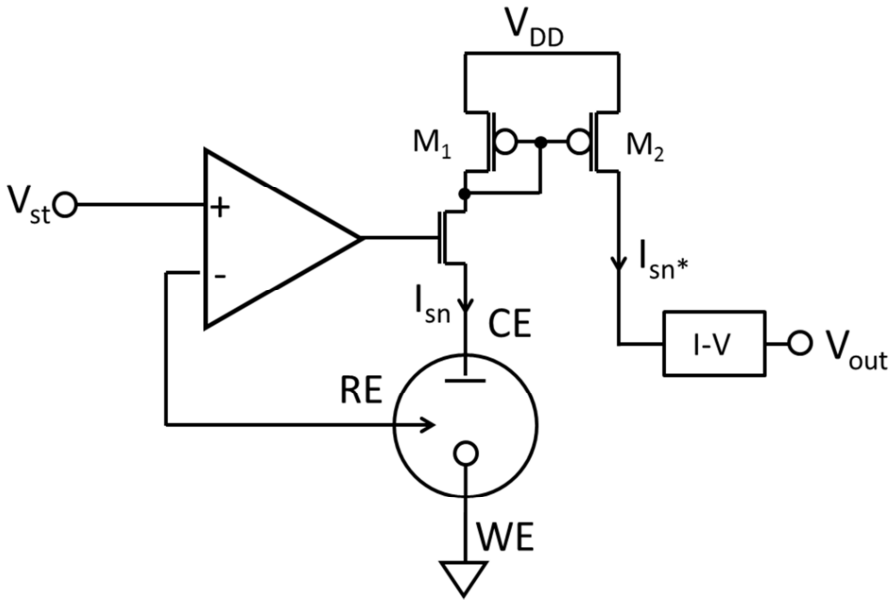


Figure 2-11. The structure of current mirror amperometric readout circuit with potentiostat. (adapted from [51])

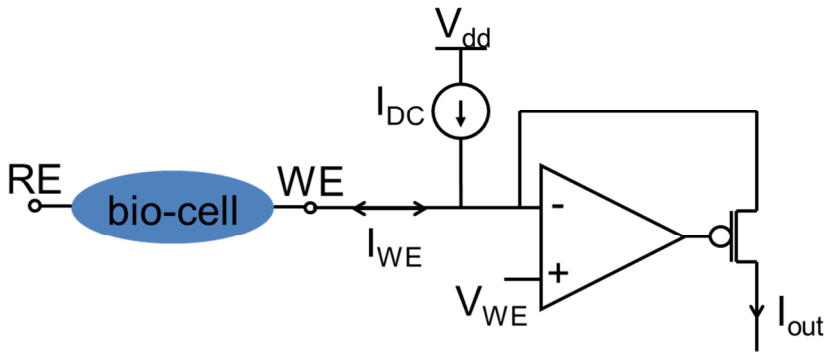


Figure 2-12. pseudo-bidirectional current conveyer with a DC offset current [72].

To improve the noise performance of the current conveyor, current mode sigma-delta modulator has been introduced [60, 74, 75]. Sigma-delta modulator takes advantage of the noise shaping by oversampling, which moves the low frequency noise to high frequency and then is removed by a low pass filter. A current mode sigma-delta structure is shown in Figure 2-13. The duty-cycle modulation of current feedback in the $\sum$-Δ loop together with variable oversampling ratio provide a programmable digital range selection of the input current spanning [74]. The performance of several amperometric readout circuits is listed in Table 2-2.

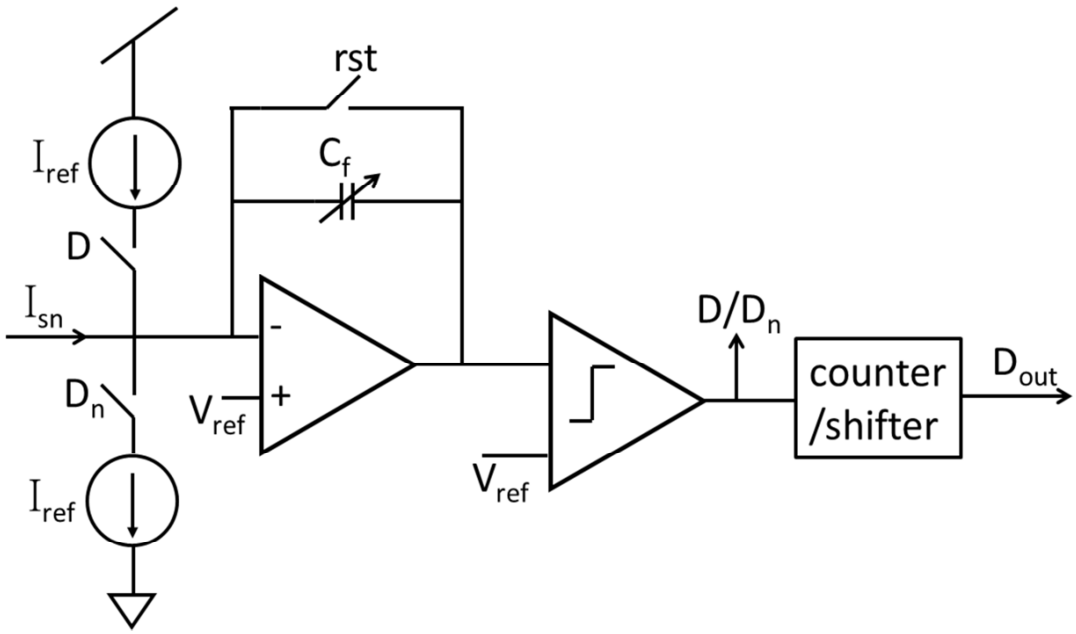


Figure 2-13 The structure of current mode sigma-delta ADC circuit.

2.5 AC Current Readout Circuitry

Impedimetric current readout circuitry is an AC current readout. In impedimetric test, a stimulus sine wave with known frequency content is applied to the electrode-electrolyte interface. When biorecognition events occur, the resulting output response contains a phase and/or amplitude shift, algebraically related to real and imaginary components. Thus, to detection the biorecognition event, the impedimetric readout circuit should have the capability to extract the phase/amplitude or real/imaginary shift, which makes circuits more complex than amperometric readout circuits.

The phase and amplitude shift can be extracted in the analog domain or the digital domain. The extraction method in the digital domain is the Fast Fourier Transform (FFT)

algorithm [30]. The FFT algorithm utilizes a broadband stimulus, such as a pulse, and computes the result at all frequency points simultaneously, producing an impedance spectrum. The composite signal source and the computationally intensive Fourier transform require FFT-based impedance spectroscopy instrumentation to use a digital signal processor (DSP) with extensive computational resources [76]. The phase and amplitude extraction method in analog domain is called frequency response analyzer (FRA). The FRA processes the response of one frequency point at a time and sweeping over the whole interested frequency range. Compared to FFT, the FRA method can be realized with simple and compact analog circuits, making it suitable for sensor array microsystems [76]. Therefore, most of the CMOS impedimetric current readout circuits use the FRA method [77-83].

In the FRA method, the only reported phase/amplitude extraction technique is the lock-in technique. Lock-in is achieved by multiplying the electrolyte response AC signal with a reference signal with same frequency. The multiplying results provide a DC output proportional to the real/imaginary portions of the AC signal under investigation. To indicate how lock-in extracts the phase/amplitude or real/imaginary change, a block diagram of the lock-in based the FRA algorithm is presented in Figure 2-14. A signal generator generates the sinusoidal voltage $\sin(\omega t)$ to stimulus the bio-cell. The biosensor response signal is $A\sin(\omega t+\theta)$ with phase shift θ and amplitude shift A. Then $A\sin(\omega t+\theta)$ multiplies with reference signal, $\sin(\omega t)$ or $\cos(\omega t)$ respectively. The equations follow

$$A\sin(\omega t+\theta)\sin(\omega t)=\frac{A}{2}[\cos\theta-\cos(2\omega t+\theta)]$$

$$=\frac{A}{2}\cos(\theta)-\frac{A}{2}\cos(2\omega t+\theta)\overset{\text{LPF}}{\Longrightarrow}\frac{A}{2}A\cos(\theta)=\frac{1}{2}\mathrm{Re}_{\mathrm{bio}}$$

(2-4)

$$A\sin(\omega t+\theta)\cos(\omega t)=\frac{A}{2}[\sin\theta+\sin(2\omega t+\theta)]$$

$$=\frac{A}{2}\sin(\theta)+\frac{A}{2}\sin(2\omega t+\theta)\overset{\text{LPF}}{\Longrightarrow}\frac{1}{2}A\sin(\theta)=\frac{1}{2}\mathrm{Im}_{\mathrm{bio}}\quad(2\text{-}5)$$

where $\mathrm{Re}_{\mathrm{bio}}$ and the $\mathrm{Im}_{\mathrm{bio}}$ is the extracted real and imaginary portions of the bio-cell impedance, respectively. ω is the frequency of stimulus signal, $A\cos(2\omega t+\theta)$ and $A\sin(2\omega t+\theta)$ are the higher order frequency components, which can be removed by low pass filter (LPF) [31, 81]. Based on (2-4), (2-5), the amplitude *A* and phase *θ* shift can be calculated by

$$A=\sqrt{\mathrm{Re}_{\mathrm{bio}}^2+\mathrm{Im}_{\mathrm{bio}}^2}\quad(2\text{-}6)$$

$$\theta=\tan^{-1}\frac{\mathrm{Im}_{\mathrm{bio}}}{\mathrm{Re}_{\mathrm{bio}}}\quad(2\text{-}7)$$

The sinusoid reference signals shown in Figure 2-14, can be replaced by rectangular waveform with the same phase of sin(ωt) and cos(ωt). This simplifies the signal generator design. Ideally it maintains the same performance as the structure in

Figure 2-14 because the higher odd harmonics caused by the rectangular waveform can be eliminated by LPF.

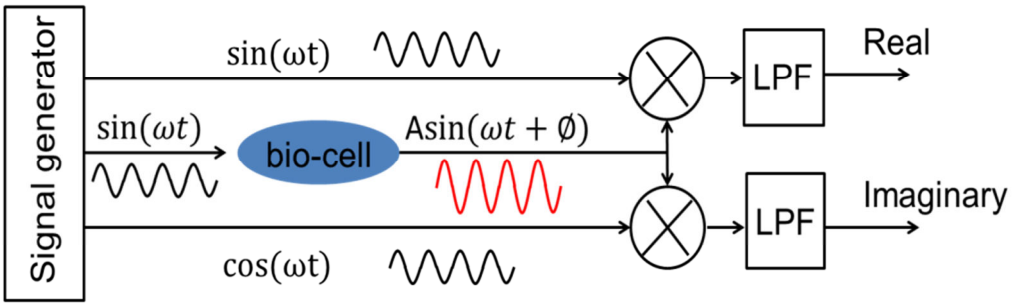


Figure 2-14. Block diagram of a lock-in based impedance spectroscopy.

Several EIS readout circuits have been developed based on the lock-in technique [31, 78, 79, 81, 83, 84]. A novel structure has been reported which combines the sigma-delta technique and the lock-in multiplier to support impedance extraction and digitization [31]. This circuit shares resources for impedance extraction and digitization to maximize the hardware efficiency, which permits over 100 readout channels within a 3x3 mm die. Its blocks diagram was presented in Figure 2-15., where the real and imaginary portions are extracted by the multiplier and the higher frequency noise is removed by the integrator.

The other impedance extraction circuit uses a transimpedance amplifier to convert the input current into voltage and then extracts impedance by the lock-in technique [81]. This chip is capable of concurrently measuring admittance values as small as 10^{-8} Ω^{-1} within the array with the detection dynamic range of more than 90 dB in the frequency

range of 10 Hz - 50 MHz [81]. An array of on-chip gold electrodes have been implanted in the developed chip, which takes advantage of the coherent detector to measure the impedance of the associated electrode-electrolyte interface [81, 82].

An impedance spectroscopy DNA analyzer with dual-slope multiplying ADC has been reported [83]. The developed EIS circuit, as shown in Figure 2-16, can extract the analyte impedance in one cycle of the interrogation. It also includes an on-chip signal generator to generate a sine waveform as the stimulus signal in the EIS measurement. The performance of several impedimetric readout circuits is listed in Table 2-3.

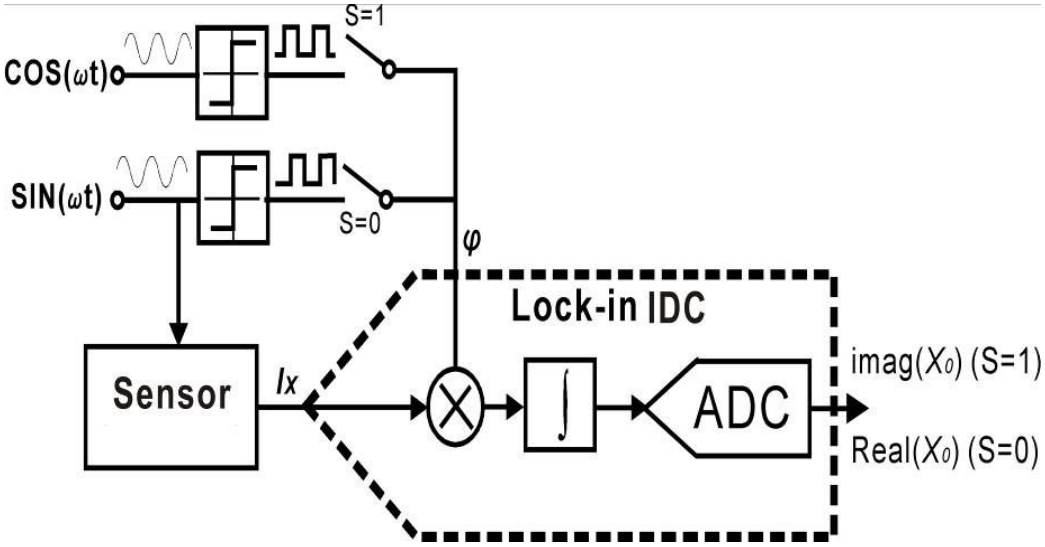


Figure 2-15. The structure of the lock-in ∑-Δ impedance extraction circuit. The circuit extracts the imaginary portion of admittance when S=1 and real portion when S=0. (adapted from [31])

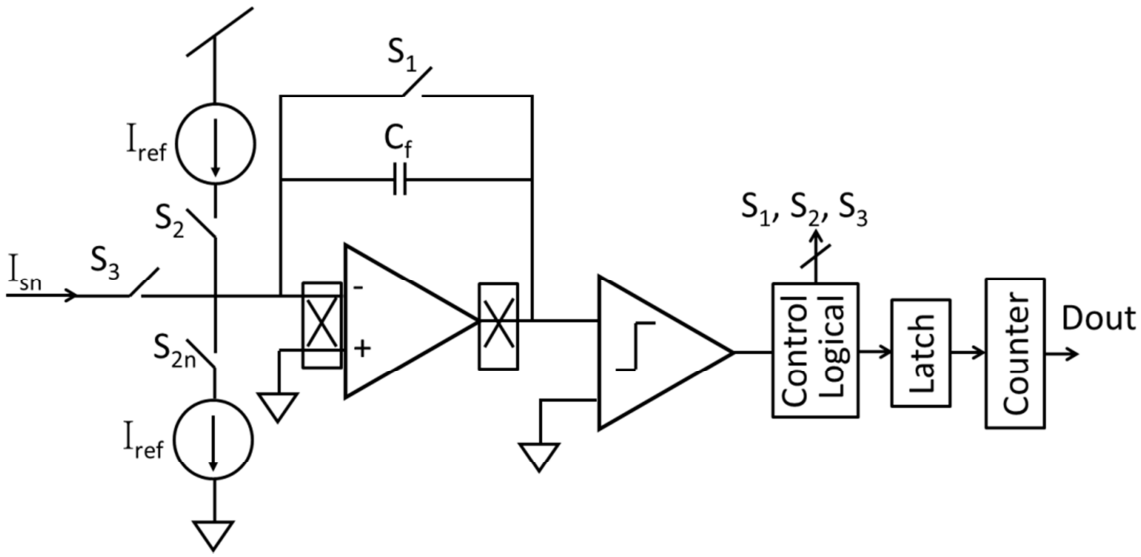


Figure 2-16. Dual-slope multiplying ADC VLSI architecture.

Table 2-2. The performance summary of amperometric current readout circuitry.

	Circuit description	Minimum detection line	Dynamic range	Technology	Area/channel	Power per channel	On-chip electrode	On-chip biointerface test
Ayers [59]	Half-amplifier structure; CDS	110pA (at 2 kHz)	NA	0.5μm, 5V	525μm^2	1uW	Yes	None
Li [49]	CDS technique	1pA	120dB	0.5μm, 5V	400 μm^2	None	Yes	Yes
Gore [60]	∑-Δ ADC+	50fA	60dB	0.5μm, 5V	None	11μW	None	None
Levine [54]	Dual-slope ADC	~240pA	~50dB	0.25μm, 2.5V	None	NA	Yes	None
Turner [48]	Two stages OPA	10nA	32dB	5μm, ±5V	None	2mW	None	None
Narula [61]	Current to time converter	100fA	116dB	0.5μm, 5V	None	0.13mW	None	None
Reay [62]	Integrator + dual-slope ADC	100fA	172dB	2 μm, ±5V	None	5mW	None	None
Breten [63]	dual-slope ADC	2.44pA	74dB	0.7μm, 5V	None	None	None	None
Stanac´evic´[74]	∑-Δ ADC	100fA	140dB	0.5μm, 3V	None	3.4μW	None	None

Table 2-3. The performance summary of impedimetric readout circuitry

	Circuit description	Frequency range	Detection current range	Technology	Area/channel	Power	On-chip electrodes
Yang [31]	Lock-in Σ-Δ ADC	10mHz-10kHz		0.5μm, 3.3V		5.4μW/channel	None
Manickam [81]	TIA + mixer	10Hz-5MHz	330pA-40uA	0.35μm, 3.3V	0.001mm^2	84.8mW (@100kHz)	Yes
Jafari [83]	Dual-slope multplying ADC	0.1Hz - 10kHz	100fA-400nA	0.13μm, 1.2V	0.06mm^2	42uW	None
Yúfera [80]	Mixer, incremental ADC	10Hz-50MHz	330pA-40uA	0.8μm, 3V	6.95mm^2	2.1mW	None
Gozzini [79]	Mixer + Σ-Δ ADC	100Hz-100MHz	None	0.35μm, 3V	0.65mm^2	60mW	None

Chapter 3 CMOS Amperometric Potentiostat and Readout Circuits

In order to achieve the miniaturized CMOS electrochemical biosensor array microsystem concept, as shown in Figure 1-1, one of the goals listed in Chapter 1 is development of CMOS electrochemical circuits with state-of-the-art performance in terms of hardware efficiency, power consumption and bio-reaction current readout resolution. To achieve this thesis goal, a CMOS amperometric potentiostat and current readout circuit was designed and characterized, as described in this chapter. The new CMOS amperometric readout circuit achieves to detection current down to 1pA that is the state of the art resolution for amperometry biosensors. The readout and potentiostat circuits were implemented in a monolithic amperometric instrumentation system with on-chip electrodes and a protein bio-interface, and tested in a liquid environment. The monolithic amperometric instrumentation system has demonstrated electrochemical performance comparable to commercial benchtop instruments. Very good agreement was observed between the commercial instrument and the CMOS amperometric instrumentation system, which is reported in the test results Section 3.4.

3.1 Amperometric Instrumentation System Structure

For an autonomous microsystem, the CMOS instrumentation would include all necessary instrumentation electronics and a communication interface to allow user control of measurement operations and reporting of measurement results. In the proposed amperometric instrumentation, a potentiostat array is needed to control individual electrode biasing in chemical reaction, a multi-function waveform generator is needed to produce the stimulus signals necessary for amperometric techniques, and a highly sensitive amperometric readout circuit is required to measure the response current. Figure 3-1 illustrates this arrangement of components and serves as the system diagram for the CMOS amperometric instrumentation chip. Furthermore, an on-chip flat gold microelectrode array was fabricated on top of the amperometric instrumentation chip and the amperometric chip was packaged by parylene for liquid environments and harsh chemical cleaning. The programmable waveform generator is designed by Waqar A. Qureshi and the post-CMOS microfabrication is designed by Lin Li. The waveform generator and post-CMOS microfabrication have been reported in [85], so they are not covered in this chapter.

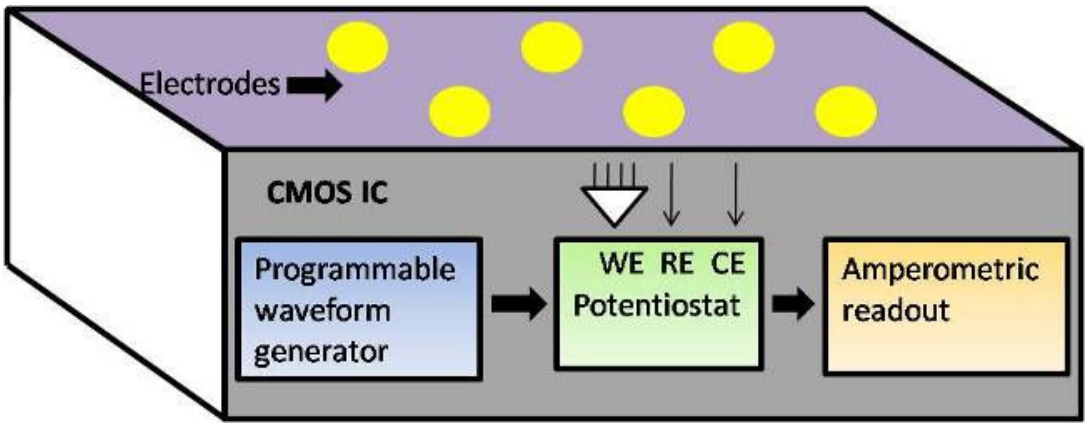


Figure 3-1. Block diagram of the amperometric instrumentation system.

3.2 Potentiostat Circuit

In generally, ±2V covers most of the electrochemical reaction range, so a 5V power voltage CMOS process is selected for the instrumentation circuits. The basic function of the potentiostat circuit is to control and maintain the biasing voltage for electrodes. The detail analysis of the potentiostat circuit function and requirements have been presented in Chapter 2. In this chapter, a single-end potentiostat circuit has been developed to support 3-electrode amperometric biosensor system. There are three operation amplifiers in the potentiostat. Compared with one amplifier potentiostat, this structure can adjust the offset between and the stimulus signal and the potential at RE. The schematic of the proposed potentiostat has been shown in Figure 3-2. OP1 and OP3 are standard one stage cascode amplifiers because there are no special requirements for them and the one stage amplifier saves area. V_{ref2} is a DC offset control input to adjust the offset between and proposed stimulus signal and V_{RE}. Output from the

waveform generator (V_{DAC}) is level shifted by OP_1 to match the input range of OP_2 by summing it with V_{ref1}. The output of OP_2, which is buffered through negative feedback using OP_3, is connected to the CE. For microscale sensors, the solution resistance between RE and CE can be assumed to be negligible so that CE and RE are at the same potential. The input of OP_3 is connected to RE and no current flows through OP_3. The output current resulting from the input stimulus voltage at CE can flow only between CE and WE. OPA1 and OPA3 are standard one stage amplifier.

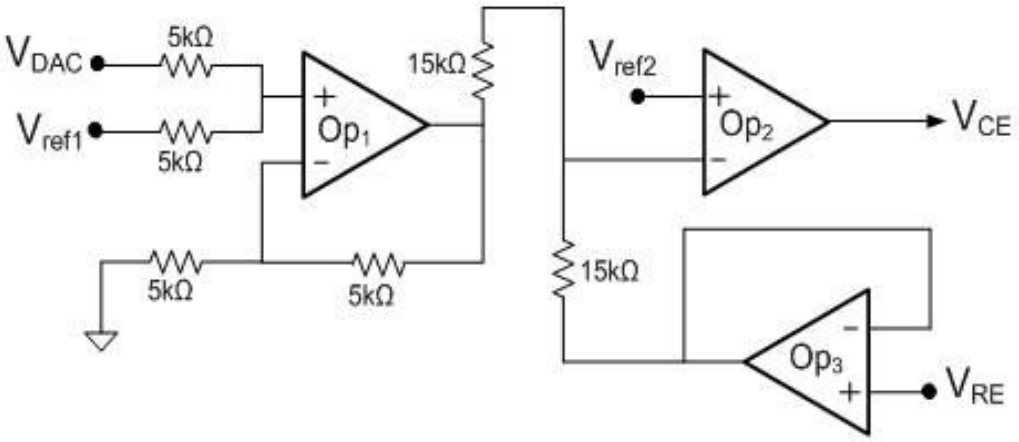


Figure 3-2. Structure of the potentiostat designed for amperometric biosensor.

One consideration in the potentiostat design is the stability. Because the range of the potentiostat load (including the analyte, solution, transducer, connection wires etc.) is wide (a couple of pF to tens of pF), there is a potential stability problem for a potentiostat

with a large load. OPA_2 is the critical amplifier because it is the driver and may cause the instability issues for large loads. An OPA with enough phase margins is needed to avoid the instabilities. As we know, a compensation capacitor (C_C) has been widely used in OPA for increasing the phase margin by splitting the poles and moving the second pole to far away from the original point. Another way to realize the same pole splitting is carefully set the value of g_{m2} (the transconductance of the second stage of the OPA). The second pole frequency is determined by $g_{m2}/(C_L)$, where C_L is the load capacitor. If g_{m2} is large enough, the second pole can move away the first pole no matter the value of C_L, which increases the phase margin of the OPA. There are two ways to increase g_{m2}: increase the drain current or increase the second stage transistors size. The large drain current in the second stage is also expected for driving large load. In summary, increasing compensation capacitance Cc and/or the second stage transcendence always help for the stability in large load condition. The structure of OPA2 is presented in Figure 3-3. The Cc=1pF, the size of the second stage transistors, Ma, Mb are W/L=96μm/0.6 μm. This op amp (OP2) was simulated in Cadence with a phase margin of 68^o with a large load of 5nF. The simulation results showed this design is stable to such large loads as shown in Figure 3-4.

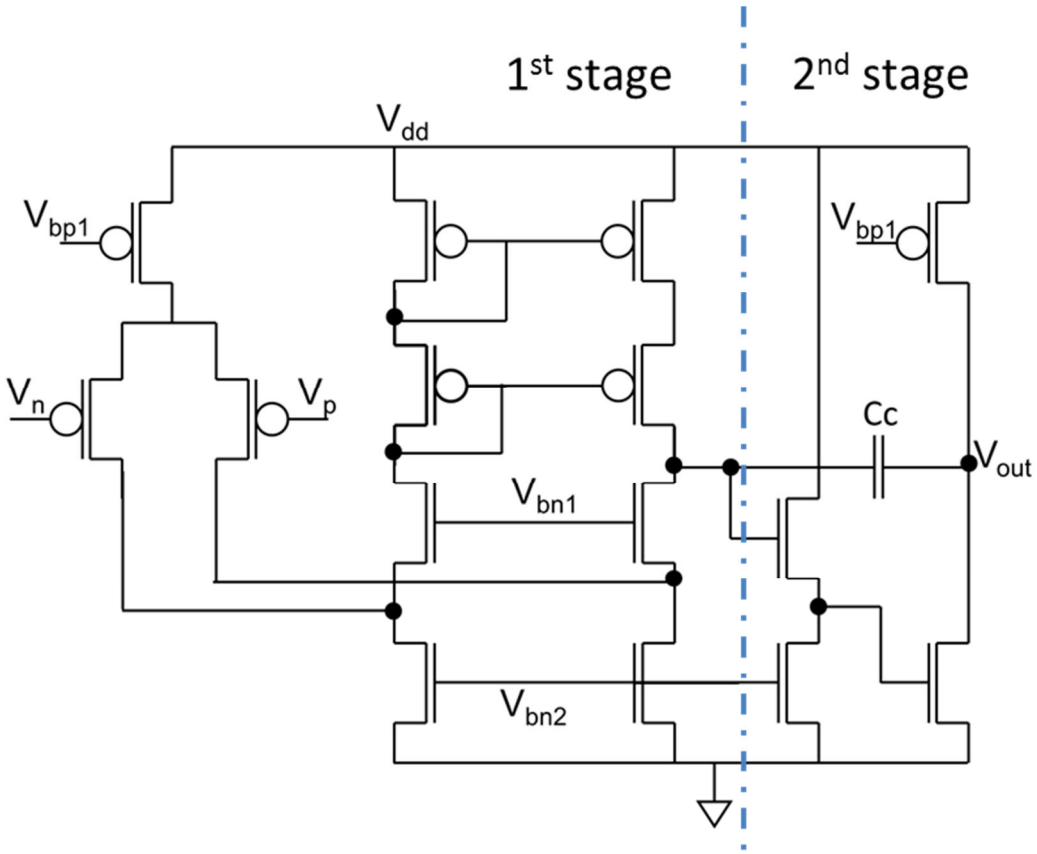


Figure 3-3.Structure of the OPA2 used in potentiostat.

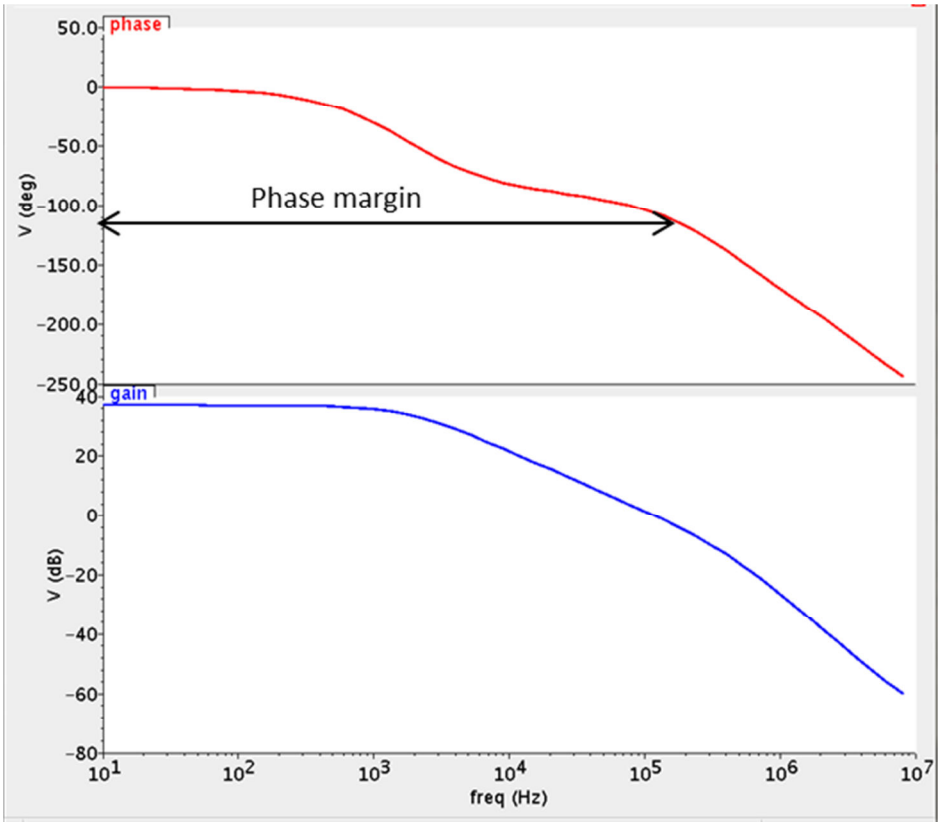


Figure 3-4. The phase margin simulation result of OPA2.

3.3 Readout Circuit

The important electrical parameter for the current readout circuit is the resolution. For typical enzyme biosensors, the bio-response current range is hundreds of μA to few mA with 1 cm^2 electrode [86, 87]. For gated ion channel membrane proteins, the detection limit is lower, around tens of nA with 1 cm^2 electrode [88, 89]. It is easy to calculate that the current for one disk electrode with 100μm diameter would be down to the pA level in a biosensor array. Thus, the readout circuit noise significantly affects the measurement resolution. For most amperometric biosensors, the stimulus signal

frequency is less than 100 Hz, and within this operating frequency, the readout circuit noise is dominated by 1/f noise rather than thermal noise. Thus, in the amperometric readout circuit design, the 1/f noise has to be considered and a solution to eliminate the 1/f noise must be found.

Correlated double sampling (CDS) and chopping techniques are the two methods used to eliminate the 1/f noise. The concept of the CDS technique is that the 1/f noise is sampled in the first phase and then subtracted in the second phase. The concept of the chopping technique is modulation the 1/f noise into a frequency band outside the signal band and which can be removed by a low pass filter. The inclusion of such low pass filters increases the circuit complexity, power consumption, and area.

As an alternative to using low pass filters, a switched capacitor current readout circuit using correlated double sampling (CDS) with reducing the 1/f noise and amplifier DC offset is described in this section. The schematic of the CDS amperometric readout circuit is shown in Figure 3-5, where a switched-capacitor (SC) charge integrator converts the input current to a voltage. The voltage is sent to a programmable gain amplifier (PGA) with a gain of C_2/C_3, where C_2 is a digitally programmable on-chip capacitor array. The area of the capacitors C_2, C_3 implemented for CDS is $0.019\mu m^2$, which is significantly smaller than the typical area of a low pass filter. The output of the PGA is sampled and held and then fed to an analog-to-digital converter (ADC) after a low pass filter. The non-overlapping clock signals for switches ph_1, ph_2 and ph_3 are generated by an on-chip clock generator block. The output voltage of the current readout circuit is given by

$$V_{out} = \frac{I_{WE}}{f_s \bullet C_1} \bullet \frac{C_2}{C_3} \tag{3-1}$$

where I_{WE} is the current at the WE and f_s is the frequency of switch ph_2, C_1 is the integrating capacitor. Thus, the input current range can be adjusted to accommodate a range of biosensors through programmable selection of the clock frequency and the PGA gain. These programmable features can be used to calibrate sensors over time.

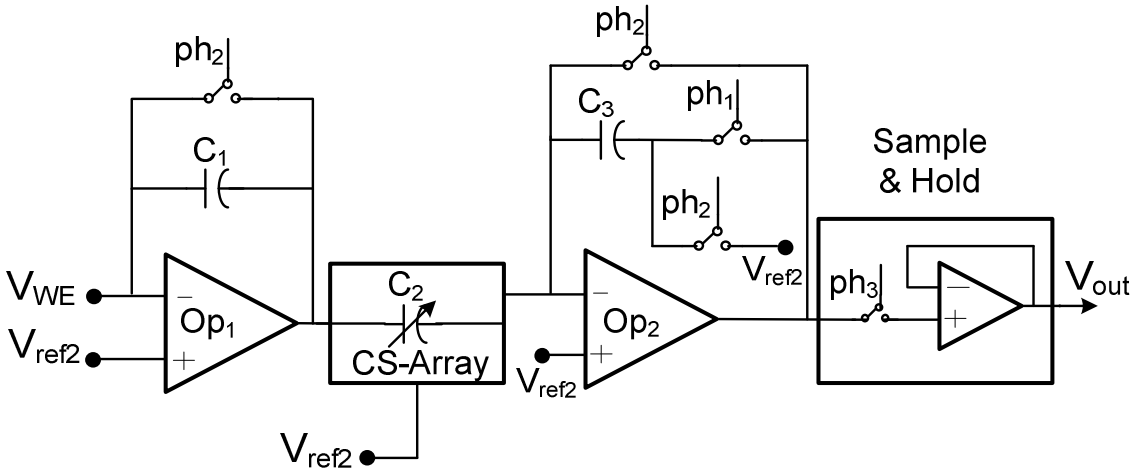


Figure 3-5. Schematic of amperometric readout circuit.

An on-chip clock generator was developed to provide precise time sequence control for switches activation. The structure of the clock generator is presented in Figure 3-6. The invertors used in the clock generator have large driving capability to keep a sharp rising/falling slope. The delay cells determine the time delay between ph1 and ph2. In the design, the time delay should be selected carefully because it limited the maximum

operation frequency of master clock. Figure 3-7 is the simulation results of the ph_1, ph_2 ph_3, ph_{1_b} and ph_{2_b} at 200kHz master clock. The clock generator has been simulated at different master clock frequency to ensure its function as expected.

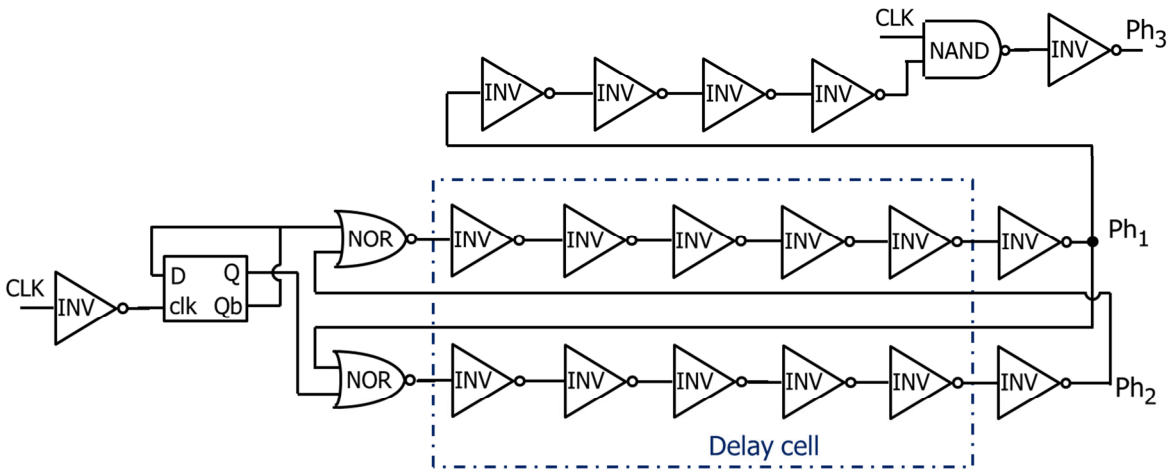


Figure 3-6. The schematic of the clock generator to generate ph_1, ph_2 and ph_3 signals.

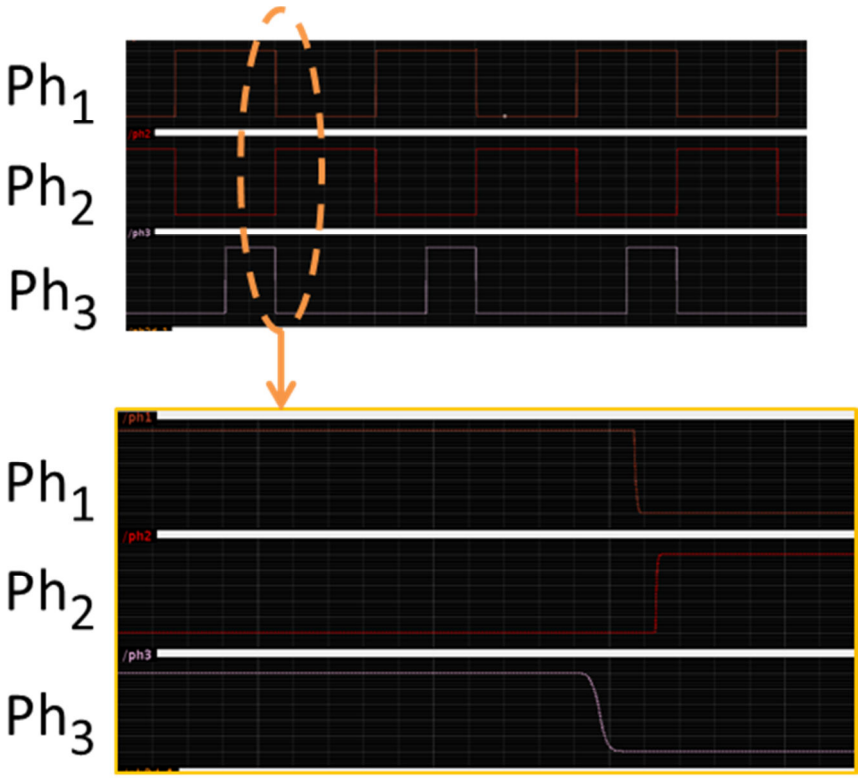


Figure 3-7. The simulation results of the time sequence of ph_1, ph_2, and ph_3 generated by the clock generator.

Several improvements have been implemented in the readout circuit to increase measurement sensitivity. In the CDS technique, the noise reduction factor is typically determined by device matching, timing errors, charge injection and clock feedthrough. To curtail charge injection, all switches were realized with minimum size transistors because the charge injection error is proportional to W•L (W is the channel width, L is the channel length). Clock feedthrough errors are the results of the coupling between the clock signal and the analog signal passing through the switch [90]. To reduce clock feedthrough errors, the NMOS switches were replaced by a structure with one NMOS

switch and two NMOS dummy transistors. The schematic of the switch is shown in Figure 3-8. M2, M3 are the two NMOS dummy transistors with half width of transistor M1. A delay cell is inserted to keep the control signals: Cntl and Cntl_b have exactly the reverse phase. The clock feedthrough simulation results of the designed switch are presented in Figure 3-9, where the error voltage caused by clock feedthrough is only 2.5mV with around 0.2pF load capacitance generated by switches' parasitic capacitors. This 2.5mV error can be reduced by having larger load capacitors at the switch output point. In our design, the switches' load capacitors are at least 2pF; Because the error voltage is inversely proportional to the load capacitors, the voltage error is easily less than 1mV.

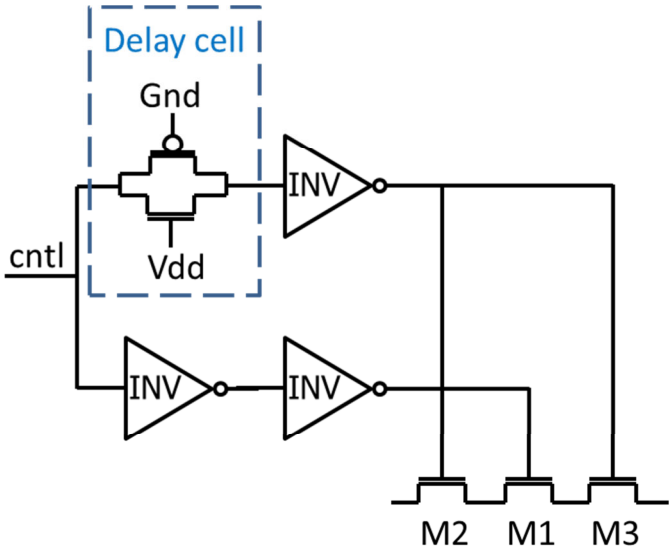


Figure 3-8. The schematic of the switch used on the readout circuit.

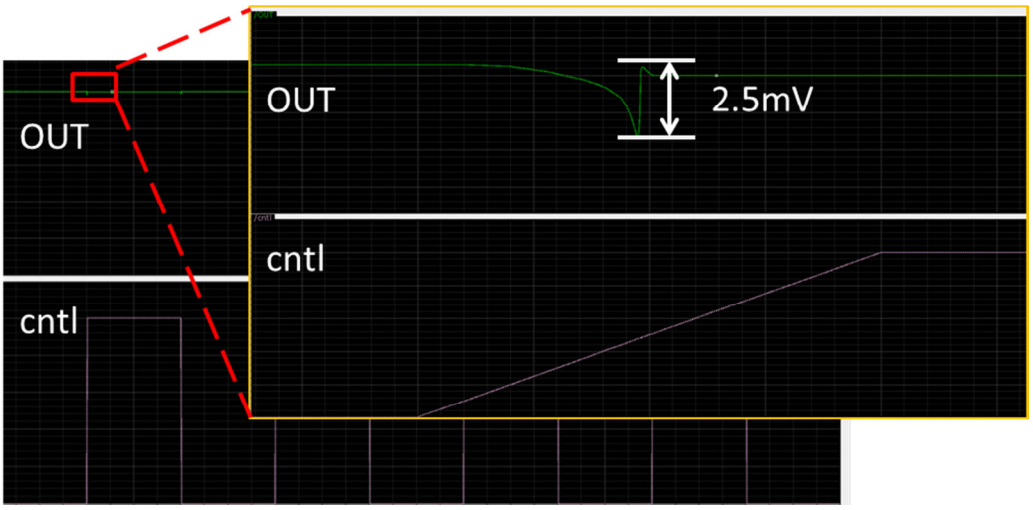


Figure 3-9. The simulation results of the switch clock feedthrough cancellation by dummy NMOS transistors.

Noise in the amplifier also directly affects the sensitivity of the readout circuit. A folded cascode amplifier was chosen because it provides high DC gain and wide dynamic range. According to the noise analysis in [91], the size of the input transistors is critical. Increasing the value of WL and W/L can reduce the 1/f noise and thermal noise. However, larger input transistors will lead to larger input bias current, which limits the sensitivity of the readout circuit. An input bias current of hundreds of fAs at 25ºC was reported for an input NMOS of W/L = 150 µm /1.8µm [91]. To optimize the tradeoff between noise, speed and input bias current, this design sets W/L = 72 µm /1.8µm for the NMOS input transistors. The structure of the operational transconductor amplifier (OTA) used in readout circuit is shown in Figure 3-10. This is a single stage fold-cascode structure, which can achieve wide bandwidth and high gain. To further improve noise performance,

all of the analog circuits were surrounded by capacitors between V_{DD} and GND to minimize power supply noise, and the analog and digital power routings were separated over the whole chip to minimize digital clock noise coupling onto analog signals. Through these improvements, the sensitivity was increased by a factor of six compared to prior work [91].

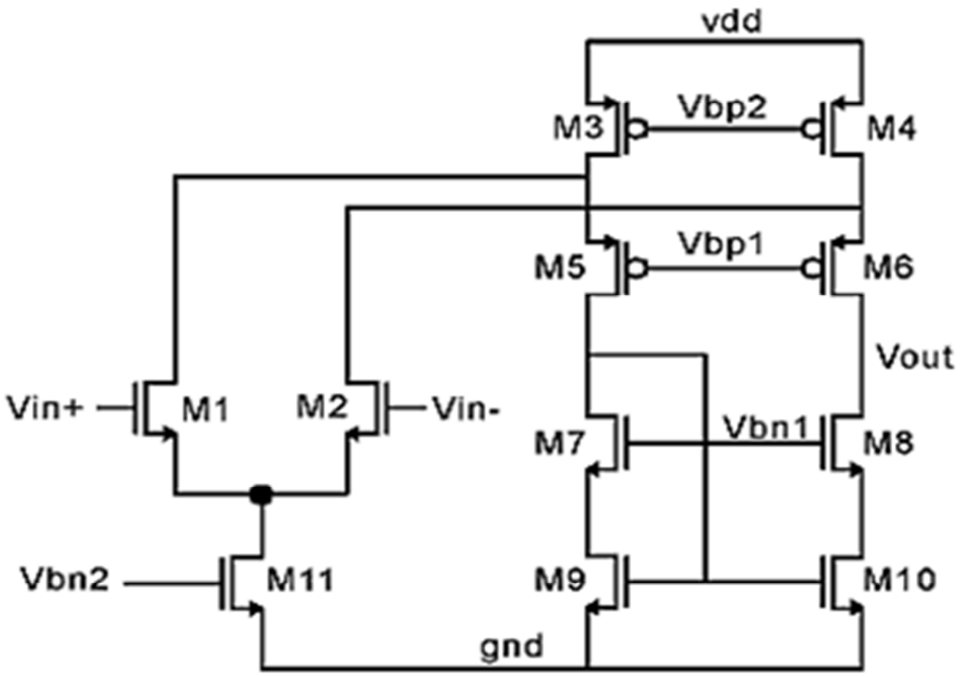


Figure 3-10. Schematic of OTA in amperometric readout circuit.

3.4 Test Results

The amperometric potentiostat and readout circuit array was simulated by Cadence Spectre simulator and was fabricated in AMI 0.5µm CMOS process. The $3\times3mm^2$

amperometric chip shown in Figure 3-11, includes the multi-function waveform signal generator and a 4-channel potentiostat and amperometric readout circuit array.

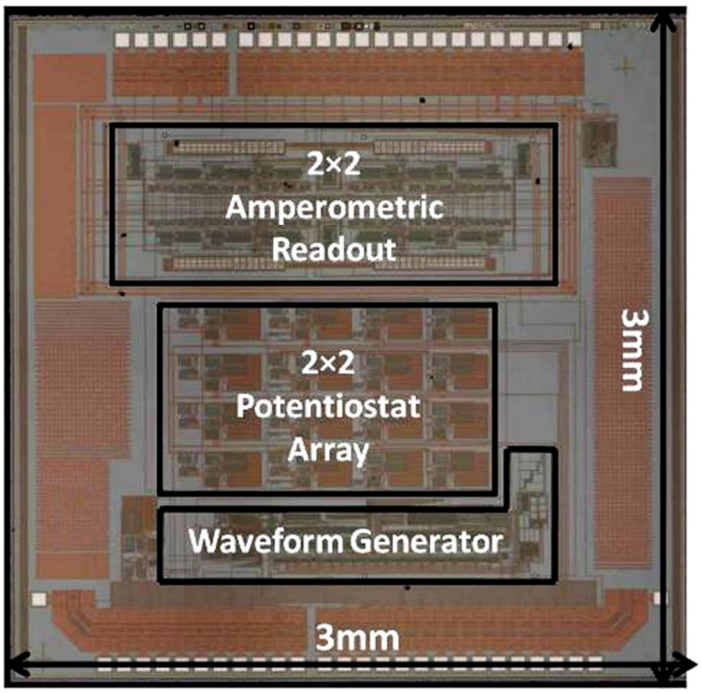


Figure 3-11. The 3×3mm^2 CMOS amperometric instrumentation chip with waveform generator and 4-channel potentiostat and amperometric readout array.

A printed circuit board (PCB) was developed for the amperometric potentiostat and readout circuit characterization. In the PCB design, elimination the noise generated by the PCB is the most important thing for characterizing the resolution of the readout circuit. To reduce the noise generated by the power source, a battery was used to provide the supply voltage for the amperometric chip. Also, several decoupling capacitors were added between Vdd, analog ground and the digital ground to reduce the noise. Moreover, a metal electrical junction box connected to the earth ground is implemented to isolate the

environment noise. BNC connectors were used for connecting the input pin of the readout circuit. The 2-layer PCB was fabricated by Advanced Circuits using an FR-4 board with 0.062" contact spacing and a lead free solder finish.

To characterize the voltage range, scan rate, and resolution of the potentiostat circuit, a triangle waveform generated by a National Instruments data acquisition (DAQ) card 6259 with programmable amplitude and frequency was used. The waveform from the DAQ board was connected to the VDAC pin of the potentiostat. The output signal at V_{CE} pin was recorded by the DAQ 6259 card. The triangle waveform was swept from 0-5V and the frequency was adjusted to ensure its scan rate would cover the interested 10mV/s - 10V/s range. The test results shown in Table 3-1, presents that the potentiostat achieve the 10mV/s - 10V/s scan rate target. However, the voltage rang is ±1.8V, which is less than the ±2V range expectation. In Chapter 5, a rail-rail potentiostat will be introduced, which overcomes the ±1.8V voltage limitation.

Table 3-1. Potentiostat characteristics.

Area	$0.4mm^2$
Voltage range	0.7-4.3V
Scan rate	1mV/s-10V/s
Resolution	10mV

To characterize the range and resolution of the amperometric readout circuit, the input current was swept using a Keithley 6430 sub-femtoamp source meter at different

clock frequencies and gain settings to span the functional input current range. Within each range, the maximum deviation between measured current and the linear input source was recorded as the linearity error. Table 3-2 shows a set of test results spanning the circuit's functional input range, with range settings from ±47pA to ±47μA. Within each setting, the input range defines the max current before the op-amp response becomes nonlinear. The 200Hz to 2MHz data show that the resolution decreases roughly linearly with clock frequency, and at 2kHz and above the resolution is about 0.3% of the range. Figure 3-12 shows test results where the maximum resolution of ±500 fA is achieved with a gain setting of 2 with a 20Hz clock; leakage currents prevent operation at lower frequencies. The power consumption of the 4-channel instrumentation circuit could not be measured independently of test circuits. However, the amperometric chip was simulated to be 22.5mW at a maximum clock frequency of 200 kHz.

The signal generator was tested by my colleague, Waqar A. Qureshi [85]. The programmable waveform generator can output a constant potential, triangle waveform, pulse, and sinusoidal waveform. Table 3-3 summarizes the characteristics of the waveform generator.

Table 3-2. Amperometric readout circuit characteristics.

Clock frequency	20 Hz	200 Hz	2 KHz	20 KHz	200 KHz	2 MHz
Gain setting	2	1	1	1	1	1
Input current range	±47 pA	±4.8 nA	±48 nA	±489 nA	±4.8 μA	±47 μA
Linearity error	1pA	13pA	150 pA	1.5nA	15nA	190 nA

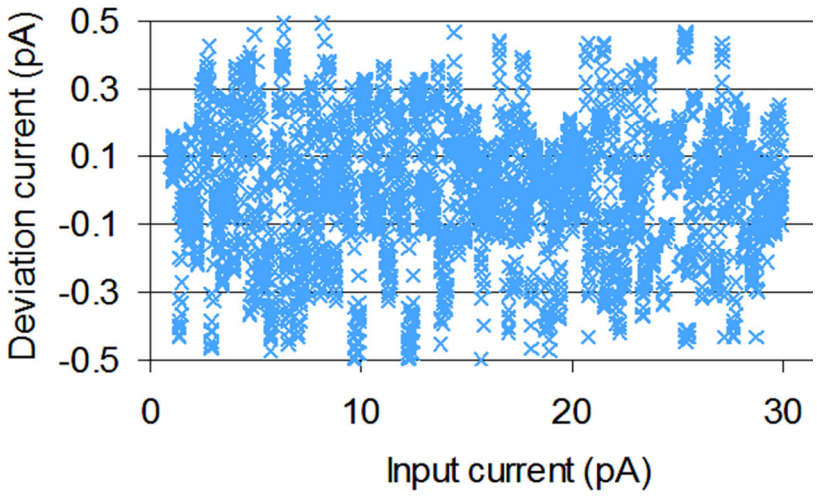


Figure 3-12. The deviation between input current and measured current for 1pA to 30pA inputs at 20Hz updating clock and gain=2 setting.

Table 3-3. Waveform generator characteristics

Area	0.44mm^2
DAC Resolution	10 bit
Scan range	0- 2V pk-pk, 10-bits
Scan rate	1mV/sec-1000V/sec
Step size	2mV

The final packaged amperometric chip with electrode array is shown in Figure 3-13. A 2×2 gold electrode array was fabricated on the surface of the amperometric chip. The chip was packaged with parylene for compatibility with liquid test environments. The on-chip electrodes and parylene packaging were designed and fabricated by Lin Li [85].

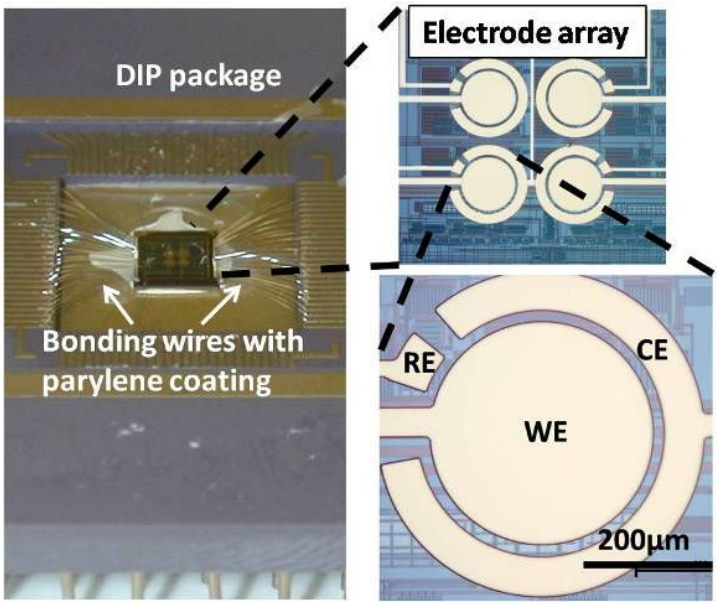


Figure 3-13. Photograph of a CMOS biosensor array chip-in-package and close up views of the post-CMOS surface electrode array.

To verify electrochemical measurement capability of the integrated system, a test setup composed of an amperometry chip, a packaged on-chip electrode array, and a PC with a DAQ card and a LabVIEW user interface was prepared. A typical electrolyte solution with 1M potassium chloride and 0.5mM potassium ferricyanide was prepared, and cyclic voltammetry measurements were performed at 25^{o}C using an on-chip WE, a commercial liquid junction Ag/AgCl RE and a platinum CE. Figure 3-14 shows the results from both a commercial potentiostat (CHI760C, CH Instruments Inc.) and the AIC at scan rates of 100mV/s and 200mV/s. In cyclic voltammetry, the peak locations give important information for biochemical identification, and these results demonstrate that the peak locations and amplitudes of the CMOS system compare extremely well with the commercial system even at different scan rates. In another experiment, a second solution

with 1mM potassium ferricyanide was prepared and cyclic voltammetry measurements were performed. Figure 3-15 shows results from both the commercial potentiostat and the reported CMOS amperometric system at two different electrolyte concentrations. As expected, the peak current increased with electrolyte concentration, and again the peak locations and amplitudes of the CMOS system compare extremely well with the commercial system. These experiments verify the proper operation of the AIC, the functionality of the post-CMOS electrodes, and the suitability of the parylene-based packaging for operation in liquid environments.

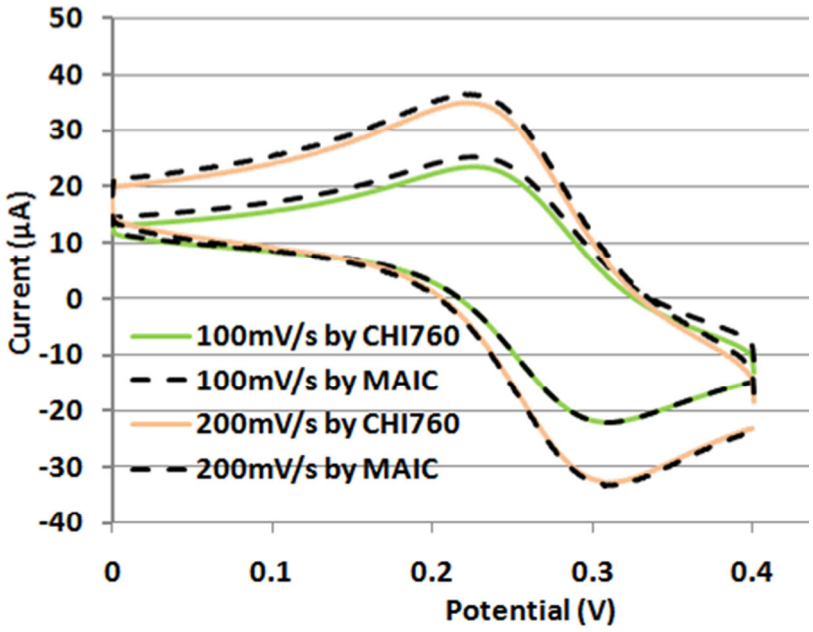


Figure 3-14. CV measurement of 0.5mM potassium ferricyanide at 100mV/s and 200mV/s for both the CHI 760 commercial instrument and the proposed circuit.

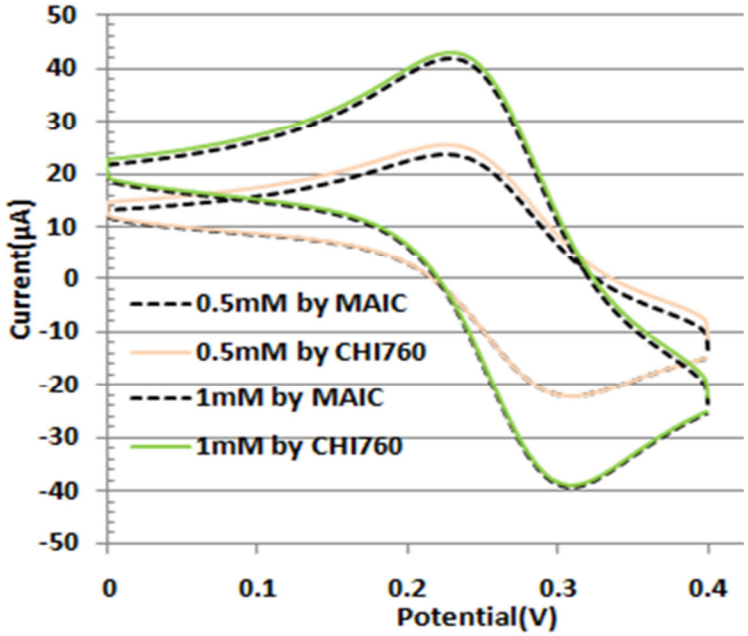


Figure 3-15. CV measurement of potassium ferricyanide at 0.5mM and 1mM for both the CHI 760 commercial instrument and the proposed circuit.

To demonstrate functionality of the microsystem as an electrochemical biosensor, a cytochrome protein biointerface was formed on the on-chip electrodes of the CMOS microsystem. Cytochrome PpcA from *Geobacter sulfurreducens* was expressed heterogeneously in E. coli and purified using cation exchange chromatography. The biointerface was prepared by cleaning the WE with piranha solution and contacting it with ethanolic solution of 5 mM 11-mercaptoundecanoic acid and 11-mercaptoundecanol (1:3 ratio) to form a self-assembled monolayer. Then, cytochrome PpcA was immobilized on the self-assembled monolayer by covalent bonding using 50mM (N-(3-dimethylaminopropyl) -N'-ethylcarbodiimide) and 5mM (N-hydroxysuccinimide) solution. Unbound cytochrome PpcA was rinsed away using 20mM phosphate buffer. CV electrochemical characterization was performed using an on-chip WE, a commercial

liquid junction Ag/AgCl RE and a platinum CE. The cytochrome PpcA results for both the CHI760 instrument and the reported amperometric circuit are shown in Figure 3-16. To determine the ability of the immobilized cytochrome biosensor interface to detect dissolved iron, different concentrations of Fe-NTA (Ferric nitrilotriacetate) in phosphate buffer were placed in a reservoir formed on top of the CMOS chip. A dose-dependent increase in peak reduction current with increasing iron concentration confirmed suitability of the PpcA interface as a biosensor. Very good agreement was observed between the commercial instrument and the CMOS microsystem.

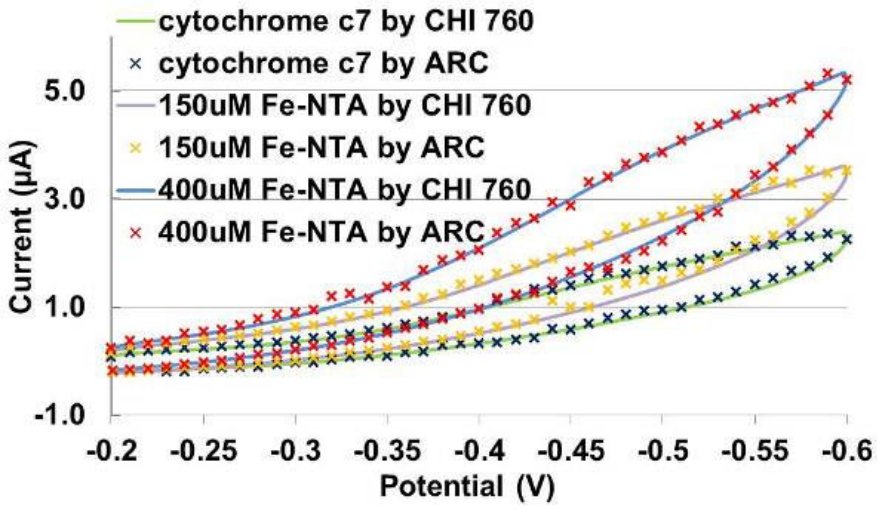


Figure 3-16. CV measurement of cytochrome PpcA interface in 150µM and 400µM Fe-NTA for both CHI 760 commercial instrument and AIC chip.

Tests were also performed to characterize the measurement variation arising from differences in readout channels and electrodes across the array. Variation results will be reported as $\mu\ (1\pm\sigma/\mu)$ where μ and σ are mean and standard deviation, respectively.

Variations in readout channels occur due to intra-chip process variations. When four readout channels on one chip were tested with a 20μA input current, the results were 20(1±0.8%)μA. Variations in electrodes could be caused by variations in the photolithography process, alignment errors, or differences in the cleanliness of electrodes. When four electrodes on the same array were tested electrochemically, oxidation and reduction peak separations were found to be 0.09 (1±2.2%) V. For comparison, peak separation was measured for a single electrode while sweeping the potassium ferricyanide potential for 15 cycles, and variation in peak separation was recorded as 0.074(1±4%) V. These results indicate that the observed intra-chip variations in circuits and electrodes are less significant than variations caused by the electrochemical solution.

The long term stability of CMOS biosensor arrays are potentially limited by a) electronics, b) packaging, c) biointerface. Absent radiation and temperature extremes that are not common to biosensor applications, CMOS electronics stability will be limited by chemical interactions with the liquid environment, which must be protected by the packaging. The reported parylene packaging was chosen specifically for its ability to provide this protection, and a parylene coated CMOS chip has been reported to remain stable in 77 °C saline for more than six months [92]. Thus, stability of biosensors based on the reported CMOS array likely are limited by the performance of specific biointerfaces chosen to implement the sensor.

Chapter 4 CMOS Impedance Spectroscopy Instrumentation

One of the goals of this dissertation is the development of electrochemical circuits with state-of-the-art performance in terms of hardware efficiency, power consumption and current readout resolution. As discussed in Chapter 2, the primary types of electrochemical instrumentation are amperometric and impedimetric circuits. Chapter 3 covered a new high performance amperometric circuit, and the high performance impedimetric readout circuit developed for this thesis research is covered in this chapter.

Impedance spectroscopy is a powerful tool for bio-interfacial characterization and the bio-interfacial impedance change caused by biorecognition events. This chapter describes the design and implementation of an impedimetric readout circuit provides a programmable current measurement range from 100pA to 100nA with a measured resolution of ~100fA. Occupying only 0.045mm^2 per measurement channel, the hardware efficiency circuit is compact enough to include nearly 200 channels in a 3 x 3mm^2 die area. The power consumption of one impedimetric readout circuit is only 5.2 μW at 200kHz clock frequency and 3.3V supply voltage, which demonstrates the efficiency of the impedimetric readout circuit. A total 26 impedimetric readout channels were integrated in a prototype impedance spectrum array (ISA) chip that was fabricated in 0.5μm CMOS. The chip was implemented in a monolithic impedimetric instrumentation system with on-chip electrodes and packaging for a cellular membrane interface

characterization in a liquid environment. Test results of the monolithic systems are shown at the end of this chapter.

4.1 Impedance Spectroscopy Methods

For impedance biosensors, biorecognition events alter the phase and amplitude of the stimulus signal in a manner that is algebraically related to real and imaginary components of the sensor's instantaneous impedance. The phase and amplitude shift caused by biorecognition can be extracted in the digital domain using a Fast Fourier Transform (FFT) algorithm [30] that utilizes a broadband stimulus, such as a pulse, and computes the result at all frequency points simultaneously, producing an impedance spectrum. The composite signal source and the computationally intensive Fourier transform require FFT-based impedance spectroscopy instrumentation to use a digital signal processor (DSP) with extensive computational resources [76]. Alternatively, in the analog domain, sensor phase and amplitude can be extracted using the frequency response analyzer (FRA) method. FRA processes the response of one frequency point at a time as it sweeps over the frequency range of interests. Compared to FFT, the FRA method can be realized with simple and compact analog circuits, making it more suitable for biosensor arrays [76]. As a result, most of the reported CMOS impedance extraction circuits have used FRA methods [77-83].

In the FRA-based impedance measurement method, a sinusoidal stimulus signal with known frequency is applied to the sensor interface. Thus, two main functional blocks are needed in FRA impedance spectroscopy instrumentation: a sinusoidal

frequency synthesizer and an impedance readout circuit. The frequency synthesizer serves to generate a sinusoidal stimulus with programmable frequency and amplitude, and the impedance readout circuit extracts the phase/amplitude or real/imaginary shift.

To achieve phase/amplitude extraction, all reported FRA readout circuits have utilized the lock-in technique. Lock-in is achieved by multiplying the biosensor's AC response signal with a reference signal matched to the frequency of the stimulus. This multiplication results in a DC output that is proportional to the real/imaginary portions of the AC signal under investigation. Figure 4-1 illustrates how the lock-in technique extracts phase/amplitude or real/imaginary response components in the lock-in based FRA algorithm. A frequency synthesizer generates the sinusoidal voltage sin(ωt) as stimulus signal. The bio-cell response signal is Asin(ωt+θ) with phase shift θ and amplitude shift A. After multiplying separately with reference signals sin(ωt) and cos(ωt), the DC component of the products are proportional to the real and imaginary parts, respectively, of the bio-cell response signal. This function can be expressed as

$$A\sin(\omega t+\theta)\sin(\omega t)=\frac{A}{2}[\cos\theta-\cos(2\omega t+\theta)]=\frac{A}{2}\cos(\theta)-\frac{A}{2}\cos(2\omega t+\theta)\overset{LPF}{\Longrightarrow}\frac{1}{2}A\cos(\theta)=\frac{1}{2}Re_{bio} \quad (4\text{-}1)$$

$$A\sin(\omega t+\theta)\cos(\omega t)=\frac{A}{2}[\sin\theta+\sin(2\omega t+\theta)]=\frac{A}{2}\sin(\theta)+\frac{A}{2}\sin(2\omega t+\theta)\overset{LPF}{\Longrightarrow}\frac{1}{2}A\sin(\theta)=\frac{1}{2}Im_{bio} \quad (4\text{-}2)$$

where Re_{bio} and the Im_{bio} are the real and imaginary portions of the bio-cell impedance, respectively. ω is the stimulus frequency, and Acos(2ωt+θ) and Asin(2ωt+θ) are higher order frequency components that can be removed by a low pass filter (LPF) [31, 81]. Based on (1) and (2), the amplitude shift *A* and phase shift θ can be calculated by

$$A = \sqrt{Re_{bio}^2 + Im_{bio}^2} \tag{4-3}$$

$$\emptyset = \tan^{-1}\frac{Im_{bio}}{Re_{bio}} \tag{4-4}$$

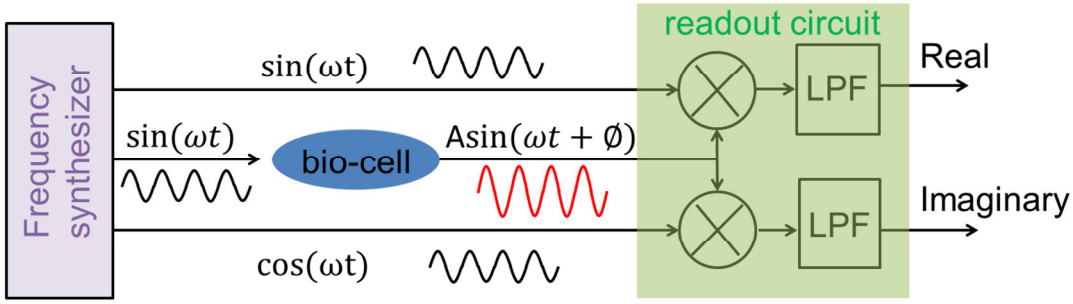


Figure 4-1. Illustration of the lock-in based FRA impedance component extraction method.

The reference signals sin(ωt) and cos(ωt) can be replaced by rectangular waveform having the same phase as sin(ωt) and cos(ωt) without loss of performance because the higher odd harmonics caused by the rectangular waveform substitution would be eliminated by the included LPF. As a result, no cos(ωt) generator is need within the frequency synthesizer, which simplifies the complexity of this circuit. The ISA chip

described in this chapter utilizes this lock-in technique with rectangular sin(ωt) and cos(ωt) reference signals.

4.2 CMOS Implementation

Figure 4-2 illustrates the biosensor array microsystem that serves as the conceptual model for the work in this chapter. The ISA chip acts as the substrate for the microsystem. An array of biosensor electrodes are fabricated post-CMOS on the surface of the chip. The SFS circuit generates stimulus signals for the bio-cell array, and the IRC circuit measures the bio-cells' response signals. The ISA chip communicates with a PC to send control commands and analyze data from the ISA chip. To support electrochemical measurements in a liquid environment, the ISA chip is packaged using a parylene coating process following post-CMOS deposition of an electrode array on the surface of the chip. The ISA chip includes a digitally programmable sinusoidal frequency synthesizer (SFS) and multiple channels of a compact impedance readout circuit (IRC). The IRC cell includes analog domain impedance extraction and local digitization while remaining compact enough to be instantiated for each sensor element, enabling massively parallel IS interrogation. The ISA chip was combined with an electrode array fabricated on the CMOS chip to form a monolithic measurement system.

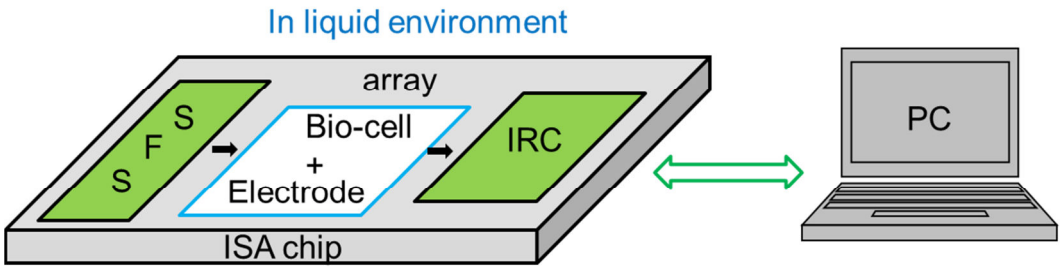


Figure 4-2. Conceptual illustration of the impedance spectroscopy circuit with SFS and IRC circuitry and on-chip electrode and biointerface array. The chip communicates with a PC to upload configuration data and download digitized measurement results.

4.2.1 Frequency synthesizer

Many circuits for sinusoid frequencies have been reported, including DSP-based solution [93], quadrate oscillators [93, 94] and triangle-to-sine generators [95]. The drawback of the DSP-based solution is the large memory requirement for very low frequencies. The limitations of the quadrate oscillators and triangle-to-sine generators are their poor linearity and difficulty in precisely controlling frequency. Our group reported an alternative method that is controlled purely by digital signals and produces excellent frequency accuracy and linearity [96]. It provides seven orders of frequency-tuning range (1 mHz to 10 kHz) appropriate for impedance characterization of many biosensor interfaces. This SFS topology employs a hybrid architecture, integrating two different structures, one for low frequencies and one for high frequencies, to accurately cover a wide range of frequencies. For high frequency (above 100Hz), an unevenly tipped resistor chain with tunable updating clock was employed. At lower frequency (below 100Hz), a subsampling method was utilized.

The SFS reported in this chapter is based on our reported hybrid structure. However, by utilizing rectangular waveform reference sin(ωt) and cos(ωt) signals, as described in Section 4.1, the ISA chip eliminates the need for an analog sinusoidal cosine frequency generator. This permits significant reduction of circuit area, increasing potential density of sensor elements on the chip, without loss of performance. The block diagram of the SFS is shown in Figure 4-3. In the R-chain based high frequency sinusoid generator, the resistive DAC (R-DAC) is a 1000 identical unit-value resistor chain with sinusoidally spaced taps. These taps are selected by the output of the token ring in the proper sequence to generate the next sine wave sample. The token ring also determines the state of the digital sin(ωt) and cos(ωt) (square waveform in phase with sin(ωt) and cos(ωt)). A second order Butterworth filter was implemented using a gm-C biquadratic filter to remove high frequency quantization replicas from the R-DAC output. Its cutoff frequency is adjustable (2kHz-200kHz) by programming both the gm and capacitor values. The R-DAC output is also provided as an input to the subsampling signal generator, which samples this signal at a frequency that is very close to the signal frequency, i.e., the frequency difference is very small. The output of the sampling circuit contains a low-frequency replica that represents the frequency difference between the input signal and the sampling clock. A detailed analysis was presented in [96]

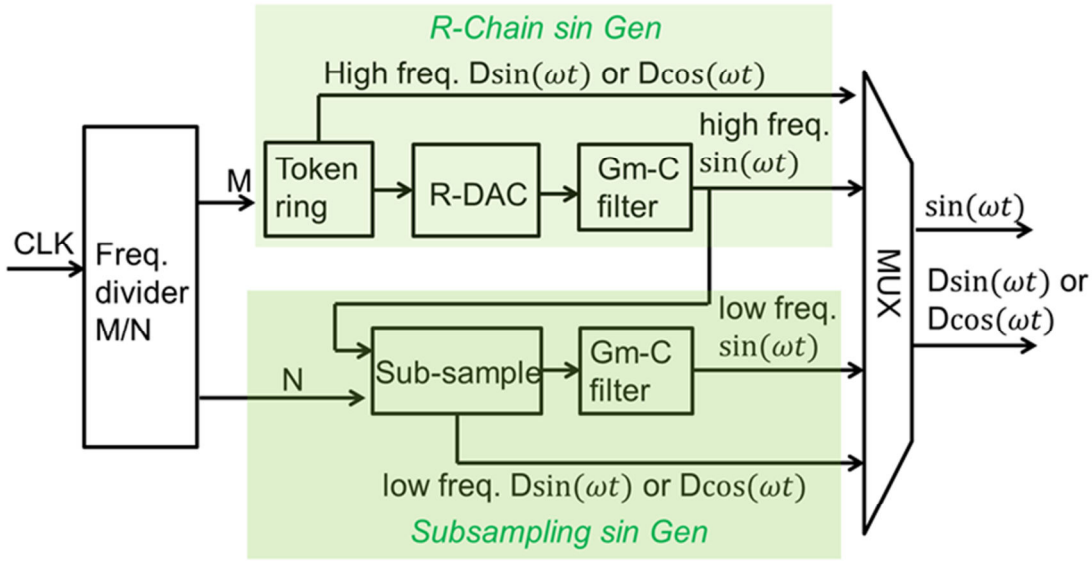


Figure 4-3. Block diagram of the signal generator that produces stimulus signal sin(ωt) and the reference square wave Dsin(ωt) and Dcos(ωt) (online version in color).

4.2.2 Impedance readout circuit CMOS design

The IRC presented here is based on the lock-in FRA method described in above where the main functional blocks are a multiplier and an LPF. The *real* and *imaginary* components are represented by only the DC output. All of the high frequency harmonic noise after the multiplier has to be removed by the LPF, so the performance of the LPF is critical for the resolution of impedance extraction. Thus, an LPF with a low cut off frequency and a high rate of frequency roll off is required. To relax the challenge in achieving such difficult requirements, a hybrid method we previously reported [31] was adopted. This method combines the lock-in and oversampling techniques to achieve a high sensitivity impedance readout circuit. The oversampling technique moves the low frequency noise to high frequency where it can be removed easily by an LPF with less

stringent design requirements. The impedance readout circuit in [31] includes an analog multiplier, an integrator, two comparators and two bidirectional counters. The integrator achieves the LPF function. The two comparators and two bidirectional counters were utilized for calibration of the mismatch between two current references. In the new IRC reported in this chapter, the current reference mismatch is reduced by increasing the WL size of transistors within the current references. Thus, the DC offset caused by reference mismatch can be calibrated by a digital calibration method and then removed from the digital output [97, 98]. As a result, only one comparator and one bidirectional counter are needed in the IRC, as shown in Figure 4-3. Furthermore, an additional block from the prior design was eliminated, and together these changes make significant improvements to hardware efficiency and power consumption.

The first stage of the IRC is a multiplying integrator stage that is based on previous work in our lab [31]. It shares resources to realize both the multiplication and integration functions shown in Figure 4-4. The multiplying integrator changes its polarity according to the value of the square wave φ. In the IRC, if the square wave reference φ(t) is in phase with sin(ωt), then φ(t) can be described by

$$\varphi(\mathrm{t}) = \mathrm{sgn}(\sin(\omega \mathrm{t})) = \begin{cases} 1, & \mathrm{nT} \le \mathrm{t} < (nT + \mathrm{T}/2) \\ -1, & \mathrm{nT} + \mathrm{T}/2) \le \mathrm{t} < (\mathrm{n}+1)\mathrm{T} \end{cases} \quad (4\text{-}5)$$

where T is the period of the stimulus signal and *n* is any integer. If the biosensor response current I_{in} is multiplied by (4-5) and integrated over *N* continuous stimulus cycles, then the integrator's output is given as

$$\int_0^{NT} I_{in} \cdot \varphi(t)dt = \sum_{i=0}^{N-1}\left(\int_{iT}^{(i+1/2)T} I_{in}dt - \int_{(i+1/2)T}^{(i+1)T} I_{in}dt \right)$$
$$= \frac{2T}{\pi} \cdot N \cdot A\cos(\theta) = \frac{2T}{\pi} \cdot N \cdot \mathrm{Re}_{bio} \tag{4-6}$$

where $I_{in} = A\sin(\omega t + \theta)$. Thus, the real component, Re_{bio} of the biosensor response signal can be extracted with a multiplier, an integrator, and reference square-wave φ(t) that is in phase with sin(ωt).

Based on (6), if the $\int I_{in}dt$ in different integration cycles can be calculated, then the real component can be determined. To simplify analysis, it is assumed that φ(t) is in phase with sin(ωt) and that both comparator results, D and D*, are low at all of φ's transition edges. If not, the multiplexing switches controlled by φ will force D and D* to exchange their polarity of charge injection through reference current I_{ref1} or I_{ref2}. From time 0 to T/2, φ is high and the counter is counting up. Just before φ's edge at time T/2, according to the charge conservation theory, at the input node, we have

$$\int_0^{T/2} I_{in}\cdot dt = CV_{res1} + I_{ref1}T_0\sum_{i=1}^{N/2} D_i - I_{ref2}T_0\sum_{i=1}^{N/2} D_i^* \tag{4-7}$$

where V_{res1} is the residue value at the integrator output, T_0 is the updating clock period, and N is the number of clock cycles from time 0 to T/2. From time T/2 to T, φ is low, the

integrator capacitor is reversed, and the counter is set to down counting mode. This mode produces

$$\int_{T/2}^{T} I_{in}\,dt = C(V_{res1} + V_{res2}) + I_{ref1}T_0 \sum_{N/2+1}^{N} D_i - I_{ref2}T_0 \sum_{N/2+1}^{N} D_i^* \tag{4-8}$$

where V_{res2} is the integrator's output voltage at time T. Simplifying the equation with D*=1-D and combining (4-7) and (4-8), the full cycle produces

$$\int_{T/2}^{T} I_{in}\,dt = -CV_{res2} + T_0 \cdot (I_{ref1} + I_{ref2})\left(\sum_{N/2+1}^{N/2} D_i - \sum_{1}^{N/2} D_i \right) \tag{4-9}$$

Thus, the real result is represented by the contents of the counter (the summations in (4-9)), provided the circuit parameters are chosen such that $\left|CV_{res2}\right| < \frac{1}{2}\min(I_{ref1}T_0, I_{ref2}T_0)$ where the residue on the integrator can be treated as noise. If the IRC is operated for N consecutive stimulus cycles after initial reset, the residue term in (4-9) remains in the same range while the digital part is magnified by N. Therefore, the error due to ignoring the residual will decrease with repeated cycles. The real component after N cycles can be expressed as

$$\mathrm{Re}_{bio} = \frac{\pi}{2TN} \cdot \int_0^{NT} I_{in}(t) \cdot \varphi(t) dt$$

$$= \frac{\pi T_0}{2T} \cdot (I_{ref1} + I_{ref2}) \cdot \left(\sum_{N/2+1}^{N} D_i - \sum_{1}^{N/2} D_i \right) \quad (4\text{-}10)$$

Following a similar analysis, it can be shown that the counter will contain the imaginary portion of admittance when $\varphi(t)$ is in phase with $\cos(\omega t)$. The imaginary portion can be presented by

$$\mathrm{Im}_{bio} = \frac{\pi}{2TN} \cdot \int_0^{NT} I_{in}(t) \cdot \varphi(t) dt$$

$$= \frac{\pi T_0}{2T} \cdot (I_{ref1} + I_{ref2}) \cdot \left(\sum_{N/4}^{3N/4} D_i - \sum_{1}^{N/4} D_i - \sum_{3N/4+1}^{N} D_i \right) \quad (4\text{-}11)$$

Thus, by setting φ to be in or out of phase with the stimulus sinusoid, the IRC circuit can extract both portions of the full impedance utilizing a structure that inherently digitizes the result while sharing resources to minimize size and power. The bidirectional counter also serves as a shift register to permit serial data upload of all channels.

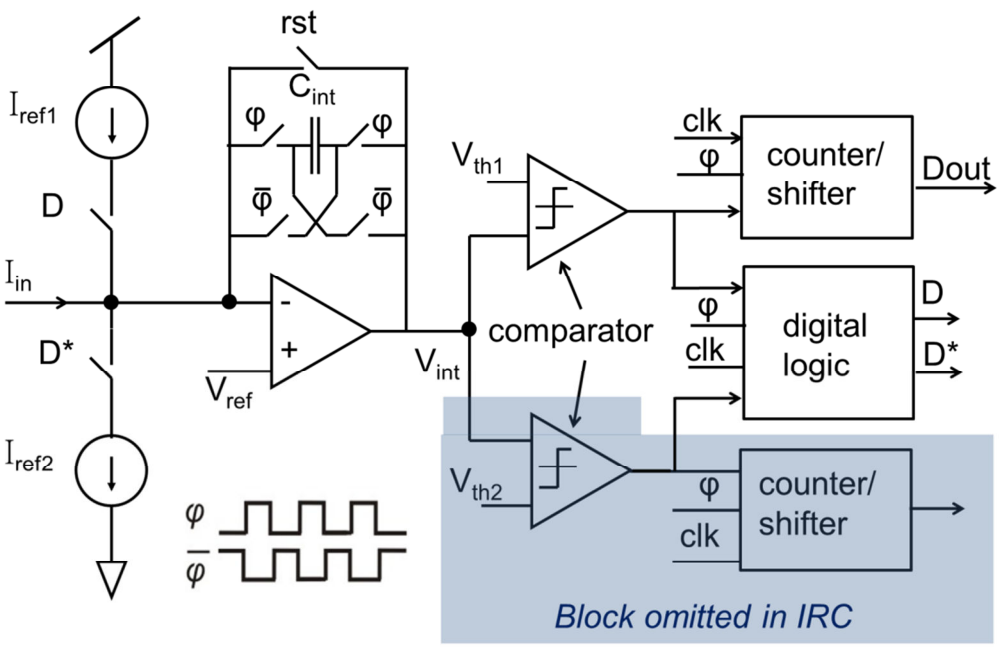


Figure 4.-4. Simplified structure of the impedance readout circuit presented in [31] and the IRC (except for gray part). *φ* and *not-φ* are non-overlapping reference square waves.

4.3 Test Results

The ISA chip was fabricated in a standard 0.5μm CMOS process, and photographs of the parylene packaged chip with 10 × 10 on-chip electrode array are shown in Figure 4-5. The diameter of each on-chip electrode is 100μm. One SFS and 26 IRC channels have been integrated on the 3 × 3mm^2 chip. The area of each IRC channel is 0.045mm^2, which is 25% less than the area of impedance readout circuit reported in [31].

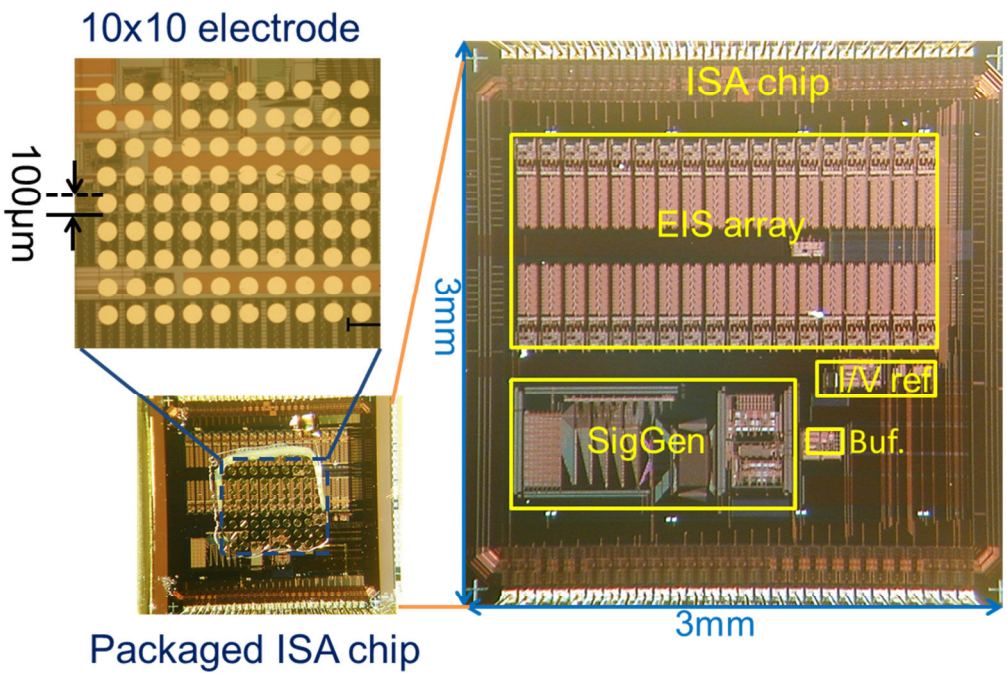


Figure 4-5. Photo of the packaged ISA chip with on-chip electrode array.

To characterize the performance of the IRC circuit, a DAQ 6259 was used to generate the sinusoid stimulus voltage, reference square wave, global clock and digital control signals and to record digital output results from the IRC on the second generation thermal control chip. An equivalent impedance model for a biomimetic membrane sensor interface [99] was utilized to characterize the chip. This model is shown in Figure 4-6 along with other elements of the IRC test setup.

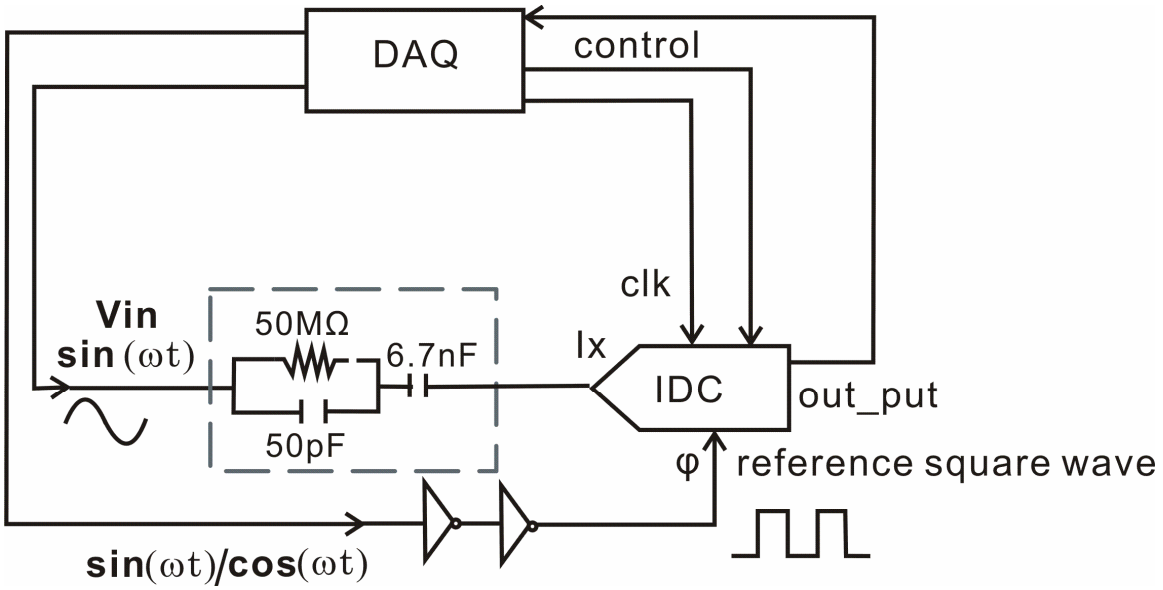


Figure 4-6. Test platform for the IRC chip with biosensor equivalent circuit model.

To verify the impedance extraction capability of the IRC circuit, a sinusoidal voltage stimulus with frequency from 0.1 to 100Hz was applied to the biosensor circuit model. Figure 4-7 plots the results obtained from the digital output of the IRC along with the theoretical curve for the model impedance. The IRC tracks both *real* and *imaginary* components of the test impedance very well, with a maximum mismatch of 1% of the full scale response.

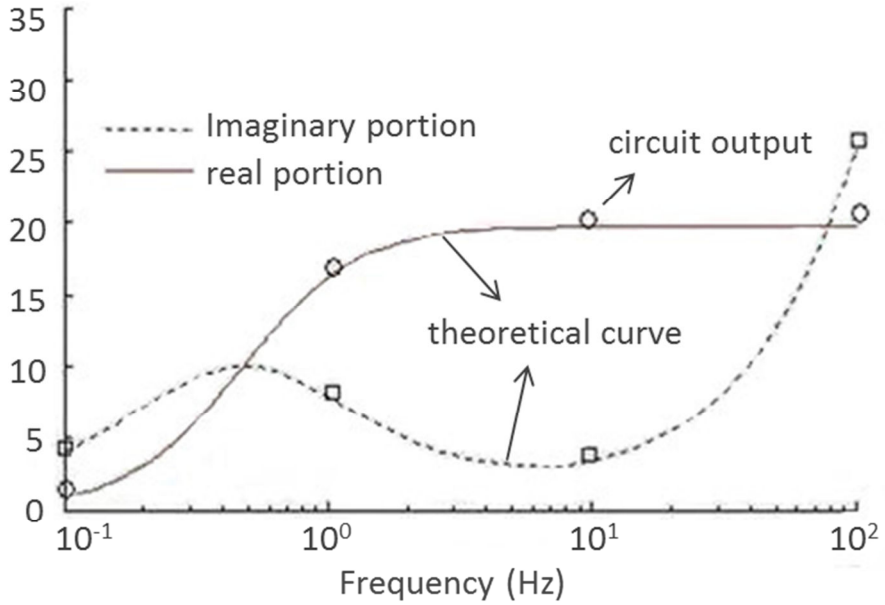


Figure 4-7. The real (circles) and imaginary (squares) results from the IRC circuit for the test setup shown in Figure 4-6 along with theoretical (expected) curve for comparision.

To characterize the circuit's response to variable impedance, an IRC channel output was recorded while independently changing the phase and amplitude of the stimulus input. Ideally, the relationship between the input signal's amplitude and the digitized real component output is linear for a constant phase and frequency. To verify the amplitude transfer function, a 10Hz, zero initial phase sinusoid signal was supplied with amplitude swept from 0 to 10nA. The IRC digital output data was recorded by data acquisition card (DAQ6259). The measured differential nonlinearity (DNL) and integral nonlinearity (INL) characteristics of the digitized real portion output are plotted in the Figure 4-8, which shows that the real portion dynamic range is more than 50.2dB for the 10nA input range.

The relationship between the input signal's phase and the digitized imaginary component output is theoretically a sine wave for a constant amplitude and frequency. To measure the phase transfer function, a cosine input with constant 100Hz frequency, constant 3nA amplitude and variable phase was supplied. The normalized digitized imaginary portion output is plotted in Figure 4-9. The output fits the expected sine wave with an RMS error of only 0.02.

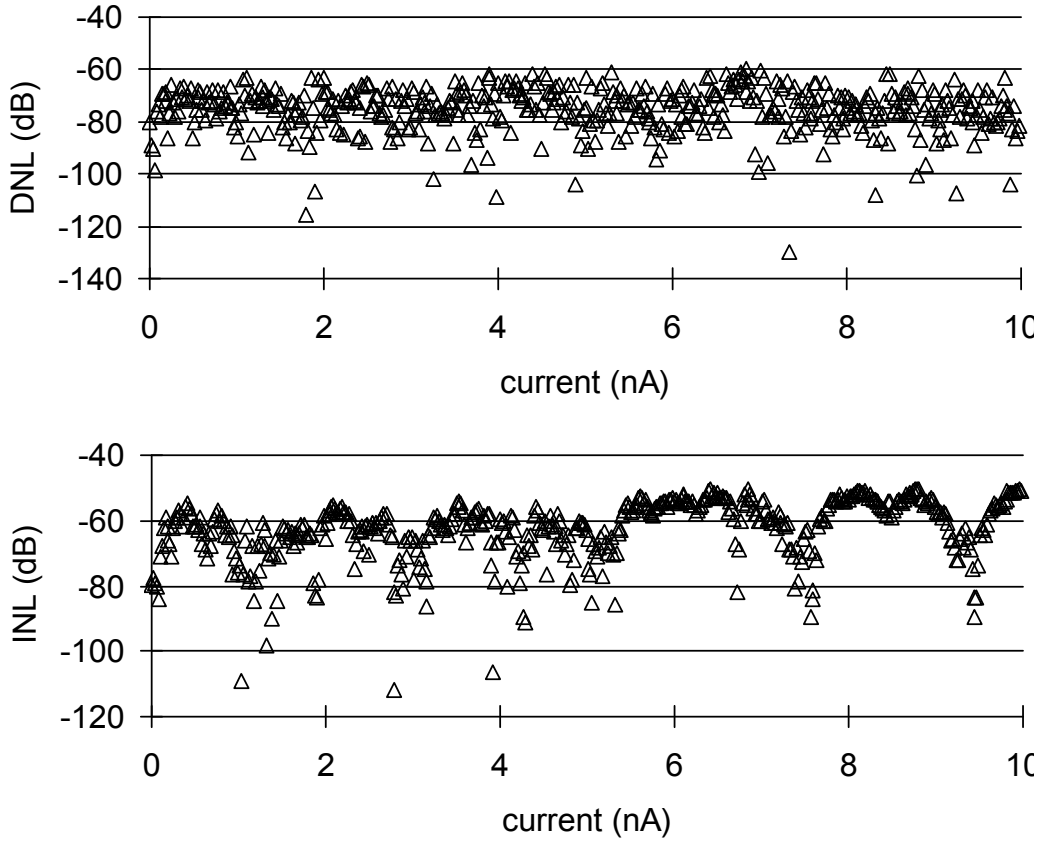


Figure 4-8. Measured DNL and INL curve of one IRC channel output when the sinusoid input amplitude was swept from 0 to 10nA. The maximum DNL and INL are 59.8dB and 50.2dB, respectively.

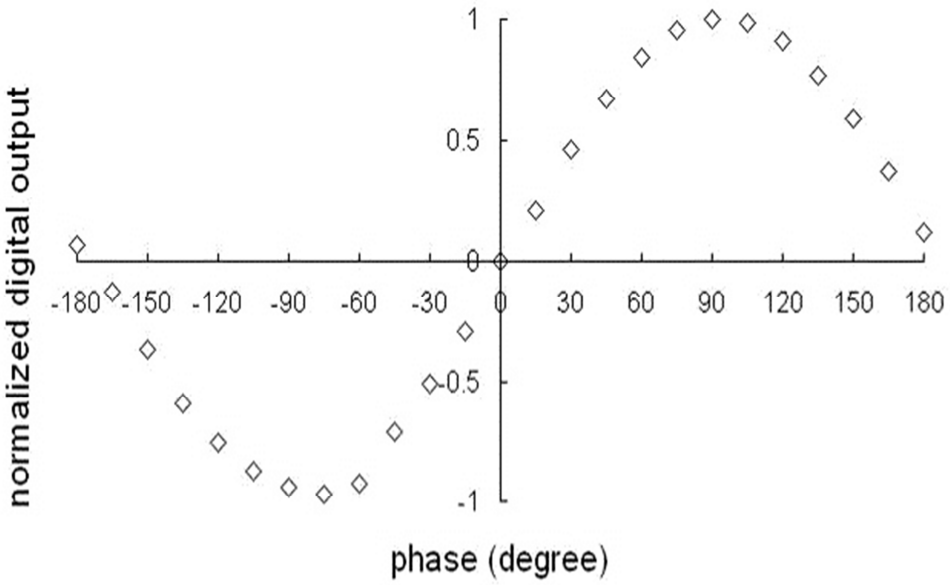


Figure 4-9. Response of an IRC readout channel as the phase of the input signal is varied from -180° to +180° degrees. Input amplitude (30nA) and frequency (100Hz) are kept constant.

Table 4-1. The performance of impedance-to-digital converter circuit.

Power/channel	5.2 μW@ 3.3V power, f_{clk}=200kHz
Area/channel	0.045 mm^2
Channel density	200 channels on a 3x3mm chip
Amplitude conversion resolution	7-8 bit
Phase conversion RMS error	<2%
Frequency range	10mHz ~ 10KHz
Maximum input current	100 nA
Maximum current sensitivity	100 fA

A tethered bilayer lipid membrane (tBLM) is useful in functional proteomics research to characterize novel membrane proteins and can be used to develop membrane protein biosensors [100, 101]. The equivalent circuit model of a tBLM interface is presented in Figure 4-10, where, Rm and Cm represent the resistance and capacitance, respectively, of the lipid bilayer and any embedded proteins, RS is the solution resistance, and Cdl is the double layer capacitance [102]. The values of Rm and Cm can be measured to characterize tBLM interface or interrogate any embedded membrane protein sensing elements.

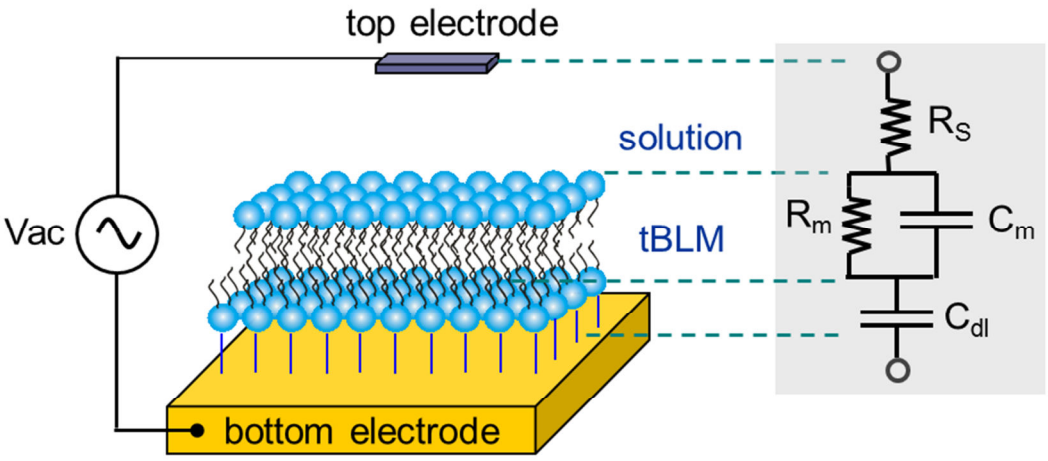


Figure 4-10. Schematic view and equivalent model of a two-electrode electrochemical site with bottom electrode coated with a tBLM. In the tBLM equivalent model, Rm and Cm represent the resistance and capacitance of the BLM assembly, respectively, while RS is the resistance of the solution and Cdl describes the double layer capacitance.

To validate the capability of the IRC to measure a real biointerface, an example tBLM was constructed. First, a self-assembled monolayer (SAM) of 1, 2-dipalmitoyl-sn-glycero-3-phosphothioethanol (DPPTE) tether lipid was formed on a clean gold electrode that was patterned on a silicon chip. Then the upper leaflet of the bilayer membrane was deposited by fusion of liposome vesicles made of 1, 2-dioleoyl-sn-glycero-3-phosphocholine (DOPC) mobile lipids. A data acquisition card (Agilent 6259) was connected to a computer and employed to generate the stimulus sinusoid and collect output data from the IRC, from which the tBLM values of Rm, RS and Cm and Cdl can be determined. Impedance measurements were conducted with the IRC circuit over the frequency range of 10 mHz to 100 Hz after the tBLM was formed. Figure 4-11 shows the amplitude and phase data obtained from the IRC as a function of frequency. For comparison, the same biointerface was tested using a commercial impedance instrument (CHI 660 B) and those results are included in Figure 4-11. These data demonstrate that the IRC circuit generates similar results as commercial equipment for extraction of biosensors impedances. The impedance difference between the commercial instrument and IRC circuit measurement results is less than 5% across the frequency spectrum. The real and imaginary impedance values extracted by the IRC were used to determine the element values of the tBLM equivalent circuit model shown in Figure 4-10. After fitting by ZView® software, the normalized values of each component are Rs = 95Ω, Rm = 211×103 $\Omega \cdot cm^2$, Cm= 0.23μF/cm^2, and Cdl = 2.87 μF/cm^2. These values are in good agreement with reported values for tBLM [103]. Using state of the art techniques, BLMs with impedance in the giga-ohm range have been reported [104]. The presented IRC chip can detect impedance up to tens of giga-ohms (>1pA resolution at 10mV stimulus),

which is well beyond the limits of traditional instruments. Thus the IRC chip enables a new capability to characterize high quality BLMs using impedance techniques.

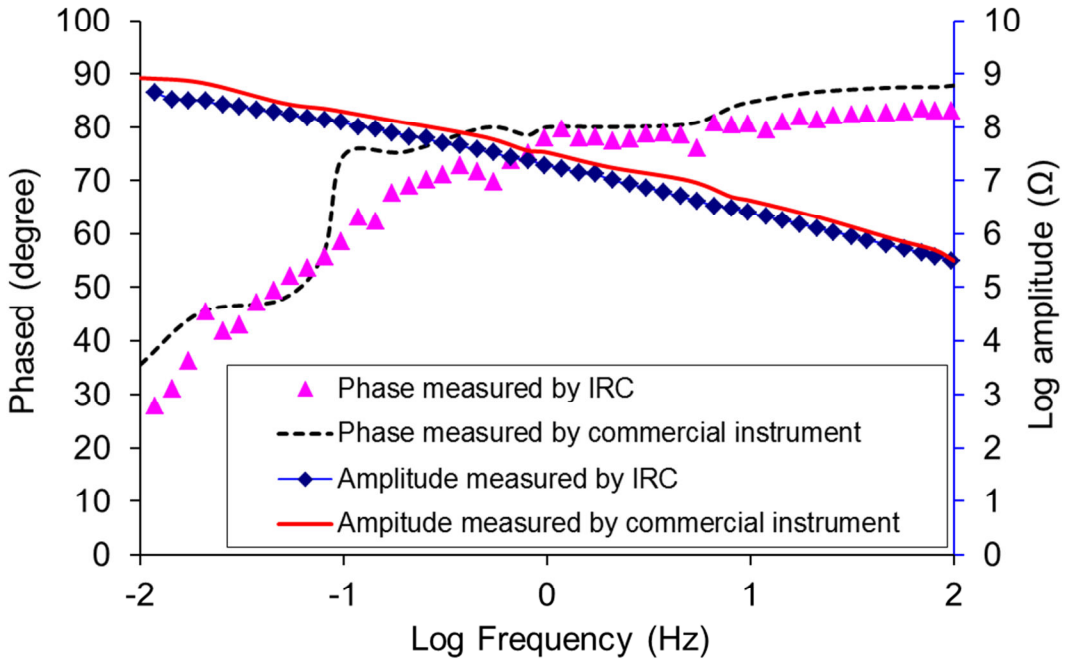


Figure 4-11. tBLM amplitude and phase measured by a commercial instrument (CHI 660 B) and by the IRC circuit at different frequencies.

Chapter 5 Hardware Efficiency Multi-mode Electrochemical Readout Chip

A high performance amperometric circuit and a high performance impedimetric readout circuit have been introduced in Chapters 3 and 4, respectively. One of the goals listed in Chapter 1 is to efficiently integrate multi-mode electrochemical techniques onto a single chip for protein characterization and sensing under widely varied controlled conditions. To achieve this goal, a hardware efficient, multi-mode, electrochemical instrumentation circuit has been developed, enabling amperometric and impedimetric measurement while sharing hardware sources. The developed multi-mode electrochemical readout circuit significantly reduces the circuit area and the power consumption for a miniaturized high throughput array microsystem.

5.1 Design Goals

Amperometry and impedimetry are the two dominating electrochemical techniques used for protein characterization and sensing. These two electrochemical techniques provide interdependent results in many assays. For example, in antigen/antibody biosensors, the amperometric technique is firstly used to verify/confirm the probe-interface formation is as expected. Then the impedimetric technique is applied to detect the concentration of the targets. Moreover, more than one electrochemical technique is

generally required for detecting multiple types of protein array. In summary, a multi-mode electrochemical instrumentation circuit is desired for biosensor arrays.

In general, the speed of the bio-reaction is less than kHz, so a tens (tenth or tens?) of kHZ bandwidth of the current readout circuit would ensure that the circuit is quick enough for monitoring the bio-reaction. The biosensor current response value is various, depending on the type of biointerfaces and the electrodes size. For a high throughput array microsystem, the response current could be small due to the small area of the electrodes and the low volume of solution. The response current can be as low as pA-~fA, which brings challenges for the circuit design. Another parameter that needs to be considered during design is the area of the circuit. Area is critical for the chip-scale biosensor array microsystem because hundreds of the multi-mode readout circuits would be integrated into a $5x5mm^2$ chip. Finally, the low power consumption is always expected for an electrochemical instrumentation.

The goals of the multi-mode electrochemical instrumentation circuits are: 1) design a CMOS electrochemical instrumentation circuit that supports both amperometric and impedimetric measurement techniques; 2) utilize hardware sharing to minimize hardware resources for array implementation; 3) achieve low power and high resolution readout performance.

5.2 Chip Architecture

To achieve the goals defined in Section 5.1, a multi-mode electrochemical readout chip (MERC), as shown in Figure 5-1, was designed. There is a potentiostat in the chip,

which generates the bias potential between RE and WE. The bias generator (BiasGen) circuit generates all the internal reference voltages/currents for the other circuits. Multi-mode electrochemical current detection is achieved by the multi-mode current readout (MCR) blocks. The clock generator provides the non-overlapped clocks for switched-capacitor circuits within the MCR. The control circuit sets the chip operation mode and the current range.

The most important block in the MERC chip is the MCR, which is responsible for realizing most of the critical performance goals. The MCR is also the most suitable block for realizing hardware sharing in order to minimize chip area, power consumption, and cost. Most of the effort was applied to improve the performance of the MCR block.

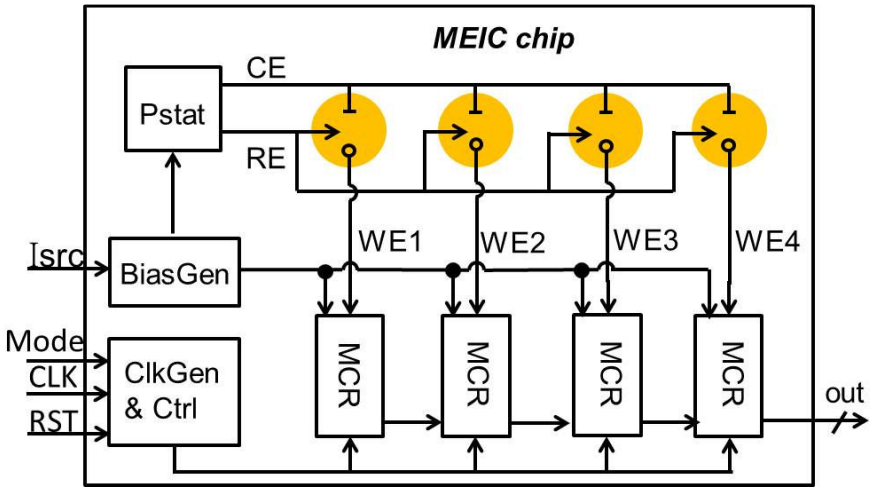


Figure 5-1. Block diagram of the multi-mode electrochemical readout chip (MERC).

5.3 Multi-mode Current Readout Approach

Because a multiplier and an integrator are two essential components for FRA impedance extraction [105], they have to be included in the MCR. Different structures of ADCs, such as ∑-Δ ADC, dual-slope ADC (integrating ADC), and pipeline ADC, etc., are used to readout the DC current in commercial amperometric equipment. Among these types of ADCs, only ∑-Δ ADC and dual-slope ADC include integrator components and both can achieve high resolution. However, the structure of the dual-slope ADC determines that it needs a long integration time to achieve the high resolution, which limits the speed. In contrast, ∑-Δ ADC uses an oversampling technique to achieve high resolution without sacrificing speed.

To readout current at the femtoampere level, the current readout circuit needs strong noise filtering capabilities. A hysteretic comparator was added in the conventional ∑-Δ ADC structure to improve the circuit noise performance. The hysteretic comparator reduces the converter switching cycles when operating with small magnitude currents, as shown in Figure 5-2. This leads to a reduction in substrate noise interference and improves linearity of the converter by reducing the number of switching operations (concept shown in Figure 5-3) on reference current sources. A hysteresis lock-in ∑-Δ ADC, as shown in Figure 5-3, has been developed to achieve amperometric and impedimetric functions. The amperometric and impedimetric modes are determined by the switches S0 and S1. The current readout circuit is in amperometric mode when S0 is open and S1 is closed. The current readout circuit is in impedimetric mode when S1 is open and S0 is closed.

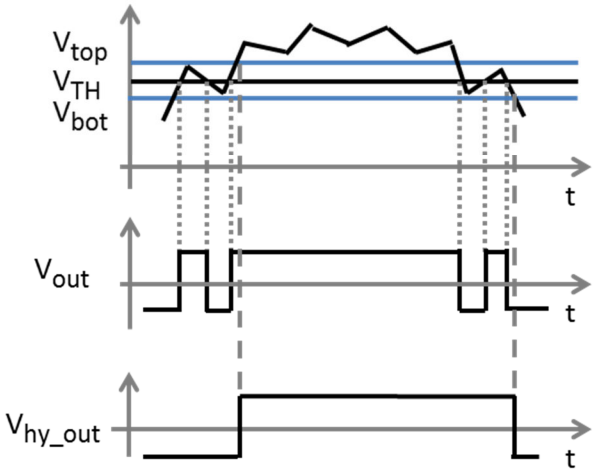


Figure 5-2. The hysteretic comparator reduces the undesired switching caused by noise.

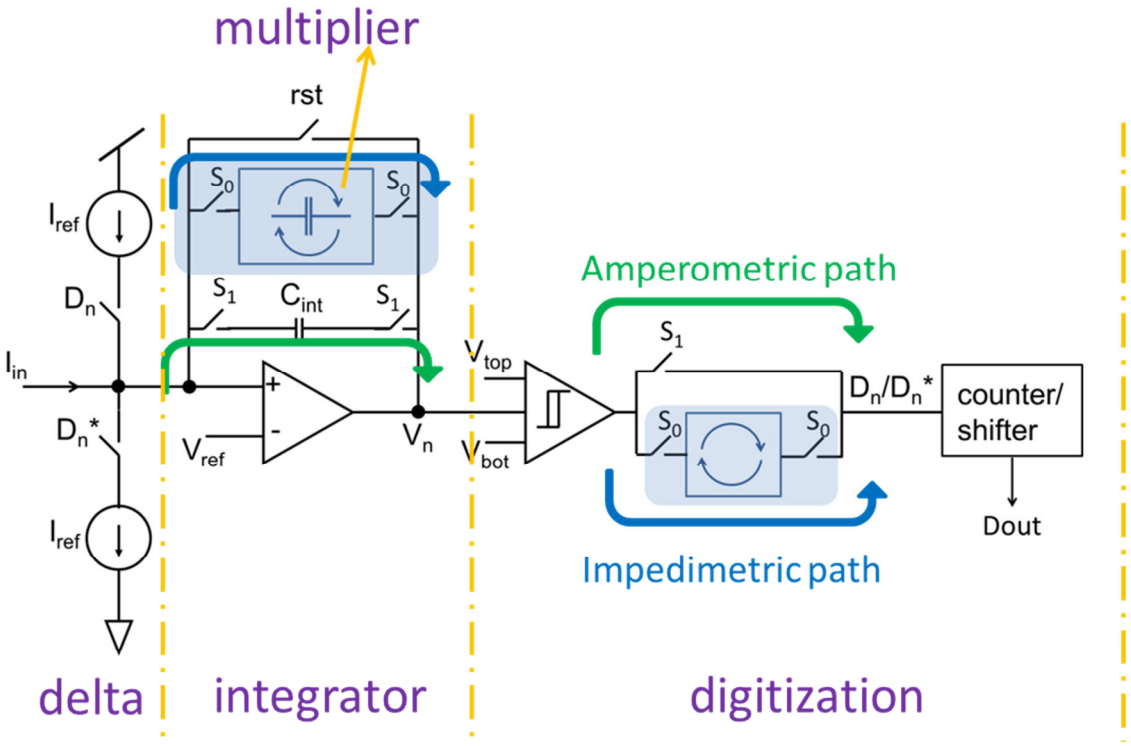


Figure 5-3. The structure of multi-mode current readout channel. The blue path is implemented for the impedimetric mode. The green path is implemented for the amperometric mode.

5.3.1 MCR noise model

In this section, we analyze the effect of thermal noise on the performance of the MCR and illustrate benefits of using a hysteretic comparator for low current measurements. For simplified analysis, we only consider the case where the input current and the integration capacitance in Figure 5.3 are being charged and discharged by only reference currents. The thermal noise contribution due to current references and the operational amplifier, can be summarized as a single equation

$$I_{noise}^2 = 4\gamma kTg_m BW \tag{5-1}$$

where k is Boltzmann's constant, T is absolute temperature, and g_m is the equivalent transconductance that combines the effects of input referred noise due to the current references and the operational amplifier. BW denotes the bandwidth of the converter. $\gamma = \frac{2}{3}$ for the above-threshold operation and $\gamma = \frac{1}{2}$ for subthreshold operation. For zero input current, the transition points of the integrator output are marked by events where the hysteretic comparator changes its state (comparator switching cycle). The total integration time between two comparator events can be approximated by

$$T_{int} = 2\frac{C_{int}\delta + I_{ref}}{I_{ref}} \tag{5-2}$$

The reference current noise is integrated to obtain an equivalent voltage noise whose signal power is given by

$$V_{niose}^2 = I_{noise}^2\left(\frac{T_{int}}{Cint}\right)^2 \tag{5-3}$$

For the sake of simplicity, BW is approximated by $1/T_{int}$ which leads to a total noise power of

$$V_{niose}^2 = \frac{4kT\gamma g_m}{C_{int}^2} T_{int} \tag{5-4}$$

The signal power is given by the square of the integrated voltage and is at the output of an integrator

$$V_{sig}^2 = \frac{(T_{int} I_{ref})^2}{C_{int}^2} \tag{5-5}$$

From (5-7) to (5-9), the signal-to-noise ratio (SNR) per integration cycle can be computed as

$$SNR = \frac{C_{int}\delta I_{ref}}{8\gamma g_m KT} + \frac{I_{ref}^2 T_{clk}}{8\gamma g_m KT} \tag{5-6}$$

where δ is the hysteresis magnitude of the hysteric comparator. For small values of reference currents, transistors in current references and amplifiers can be biased in weak inversion, where the equivalent transconductance $g_m = \frac{k}{U_T}(I_{ref} + I_{bias})$, with I_{bias} being the tail current of the operational amplifier. Substitute values of $k = \frac{1}{2}U_T$ for weak-inversion into (5-4), then the SNR achieved during a single comparator switching cycle is given by

$$SNR = \frac{C_{int}\delta U_T}{8\eta KT} + \frac{I_{ref} T_{clk} U_T}{8\eta KT} \tag{5-7}$$

where $\eta = (\frac{I_{bias}+I_{ref}}{I_{ref}})$, and U_T is the thermal voltage. The SNR consists of thermal noise contribution due to integration of reference current I_{ref} and is directly proportional to the product $I_{ref}T_{clk}$. Decreasing I_{ref} in (5-7) has to be compensated by an increase in the clock period T_{clk} to maintain a constant SNR. If δ in (5-6) is 0 V, then SNR degrades as the reference current decreases. The addition of hysteresis ensures that the SNRs between comparator switching cycles are at least $\frac{C\delta U_T}{8\eta KT}$. This is weakly dependent on the reference currents and independent of the clock frequency. Thus, for large operational currents, the SNR in (5-7) is dominated by conventional ∑-Δ operation, whereas for a low operational current I_{ref}, the SNR is determined by the hysteresis magnitude. In summary, the noise performance for small input currents (~nA) can be improved by using a hysteretic comparator.

5.3.2 Amperometric mode

When switch S1 closes, the multi-mode current readout is in the amperometric mode. In the amperometric measurement, the bandwidth of the input current is assumed to be much less than the sampling frequency. Therefore, the time-domain analysis can be simplified by considering only a DC input current, which will be denoted by I_{in}. The structure of the hysteresis lock-in ∑Δ ADC working as an amperometric function was shown in Figure 5-3.

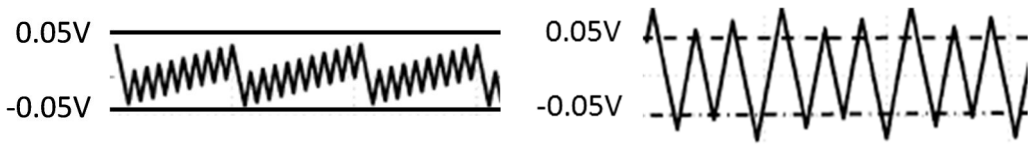
During each clock cycle, the integrator voltage, V_n, (n=1, …N) is updated according to:

$$V_n = V_{n-1} + \left(\frac{I_{in}}{I_{ref}} - D_n\right)\frac{I_{ref}T_{clk}}{C_{int}} \tag{5-8}$$

$$D_n = \mathrm{sign}(V_{n-1} + D_{n-1}\delta) \tag{5-9}$$

where D_n ($D_n \in (-1, +1)$) is the comparator output; T_{clk} is the clock period; I_{in} is the input current; I_{ref} is the reference current; and C_{int} is the integrator capacitor.

The magnitude of δ plays a key role in the noise performance of the developed ∑-Δ ADC. When the magnitude $\delta \ll \frac{I_{ref}T_{clk}}{C_{int}}$, the integrator output exhibits significantly high switching cycles, as shown in Figure 5-4 (a). After increasing the magnitude of δ, the number of integrator switching cycles decreases significantly, as shown in Figure 5-4 (b). The reduction in switching cycles reduces substrate noise and integrator nonlinearity, which are important for measurement of ultra-low magnitude input currents.



(a) (b)

Figure 5-4. The output of integrator when (a) the hysteresis magnitude is 0V, and when (b) the hysteresis magnitude is 100mV

5.3.3 Impedimetric mode

The structure of the MCR working as an impedance extraction function is shown in Figure 5-6. Based on the concept of the lock-in technique explained in Chapter 2, the signal φ and the stimulation sinusoidal is in-quadrature. To extract the *real* coefficient information, the stimulation sinusoidal, sin(ωt), is multiplied by the reference signal φ, which is in phase with sin(ωt). According to the analysis in [106], the extracted *real* portion in *N* continuous stimulus cycles can be presented by

$$real \quad portion \quad = \frac{\pi}{2T_{stim}N} \cdot \int_0^{NT_{stim}} I_{in}(t) \cdot \varphi(t) dt$$
$$= \frac{\pi T_{clk}}{T_{stim}} \cdot (I_{ref}) \cdot \left(\sum_{N/2+1}^{N} D_i - \sum_{1}^{N/2} D_i \right) \tag{5-10}$$

where T_{stim} is the period of the stimulation signal.

Following a similar analysis, it can be shown that the counter will contain the *imaginary* portion of admittance when φ is in phase with cos(ωt). The *imaginary* portion in N continuous stimulus cycles can be presented by

$$imaginary \quad portion \quad = \frac{\pi}{2T_{stim}N} \cdot \int_0^{NT_{stim}} I_{in}(t) \cdot \varphi(t) dt$$
$$= \frac{\pi T_{clk}}{T_{stim}} \cdot (I_{ref}) \cdot \left(\sum_{N/4}^{3N/4} D_i - \sum_{1}^{N/4} D_i - \sum_{3N/4+1}^{N} D_i \right) \tag{5-11}$$

5.4 MERC CMOS Implementation

5.4.1 Potentiostat

The function of the potentiostat circuit is to control and maintain the voltage between the working electrode and the reference electrode under varying current conditions. Its structure is shown in Figure 5-5, where the stimulus signal was applied at the positive input pin of OP1. The CE potential follows the stimulus signal by OP2 and there is no current going through RE because RE is the input pin of OP3. In Chapter 3, a potentiostat was developed with 3.6V input range, which is slightly less than the 4V input range goal. To increase the input range of the potentiostat, a rail to rail amplifier was implemented [107], which includes three stages: an input stage, a gain stage and a buffer stage.

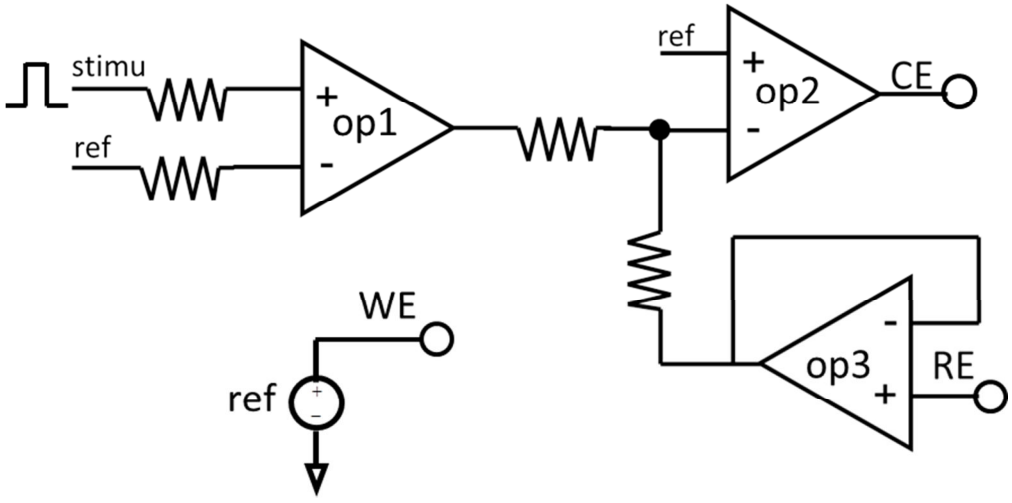


Figure 5-5. Schematic of the potentiostat.

5.4.2 MCR circuit

The schematic of the hysteretic comparator is shown in Figure 5-6. The two threshold values of the hysteretic comparator are controlled by Vbpr and Vbnr. When Vbpr equals Vbnr, the hysteresis magnitude of the comparator is zero and working as a normal comparator. The hysteretic comparator is simulated by Cadence Spector simulator at 25ºC with a TT (typical-typical) N/PMOS process corner [108] that represents the typical mobility of the carrier (electron/hole) in N/PMOS. The simulation of the hysteretic comparator is shown in Figure 5-7, where the hysteresis magnitude, δ, is 100mV.

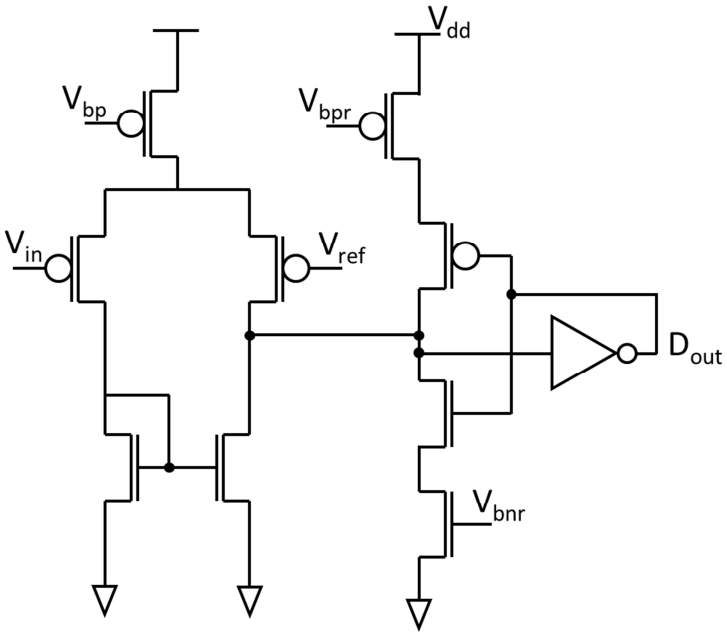


Figure 5-6. Schematic of the hysteretic comparator.

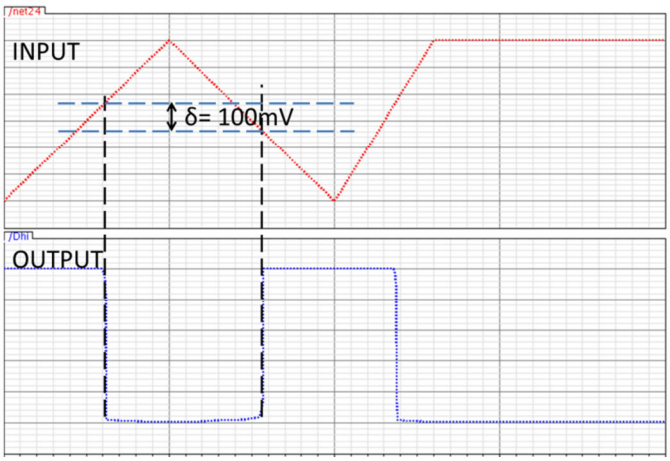


Figure 5-7. The simulation results of the hysteretic comparator.

The schematic of the amplifier used in the integrator is shown in Figure 5-8. This is one stage folded cascade amplifier which provides 87dB gain. The bidirectional counter used in the MRC is from our previous work [31], which achieves up and down counting by one counter. The BiasGen circuit was designed to support all the reference voltage for other analog blocks.

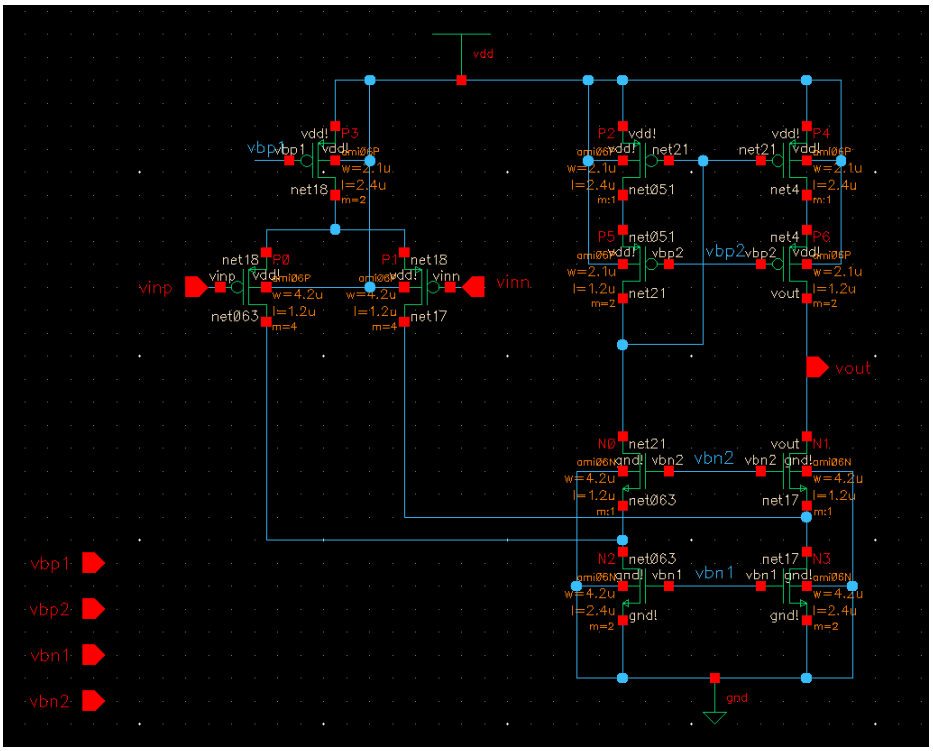


Figure 5-8. Schematic of the amplifier used in the integrator.

5.5 Test Results

5.5.1 Circuits characterization

The multi-mode electrochemical readout chip was fabricated in a 0.5μm CMOS process, and the die photograph is shown in Figure 5-9. A rail-rail potentiostat and 4 multi-mode readout channels have been integrated on a 1.5mm × 1.5 mm chip. The testing printed circuit board (PCB) for MERC is shown in Figure 5-10. This PCB was fabricated by Advanced Circuits in 2-layers, using FR-4 with a 0.062” pad spacing and a lead free solder finish.

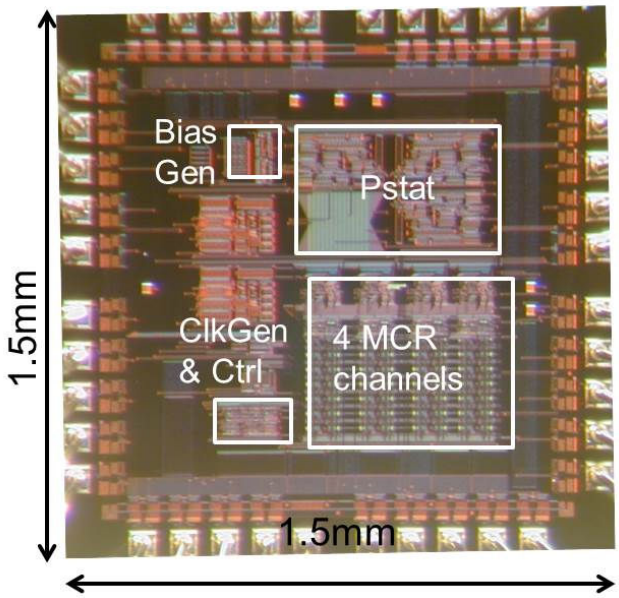


Figure 5-9. The photograph of the multi-mode electrochemical readout chip.

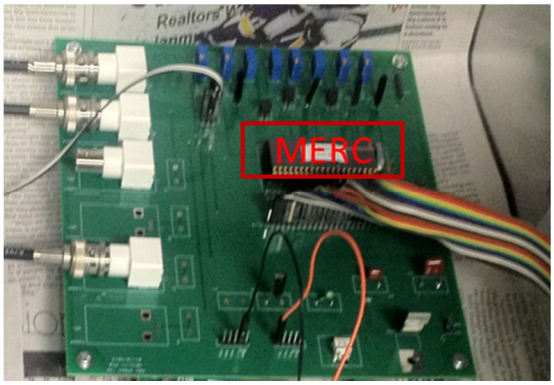


Figure 5-10. The printed circuit board for MERC characterization.

To calculate operation and the input range of the potentiostat, a triangle waveform from 0 to 5 V as an input signal was connected to the input node of the potentiostat. The output voltage of the potentiostat is plotted as a function of input voltage in Figure 5-11. The effective input range of the potentiostat is 0.1-4.8V.

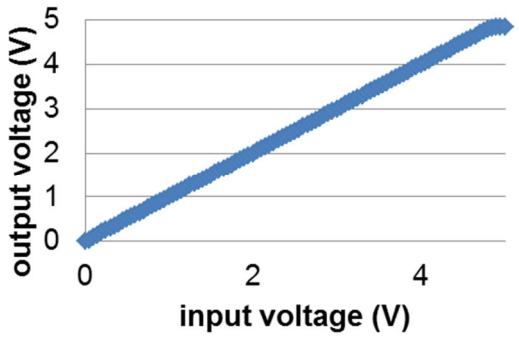


Figure 5-11. The test result of the potentiostat.

To characterize the resolution improved by the hysteretic comparator, the MRC was tested with both 100mV and zero hysteretic magnitude. For a ±10 pA input current with a 100pA current reference, the differential nonlinearity (DNL) results of the MRC with and without the hysteresis magnitude ($\delta = 100\text{mV}$) are presented in Figure 5-12. One bit resolution is increased by the hysteretic comparator. This shows that noise performance at small currents is improved by using a hysteretic comparator. The power consumption of the MRC with the hysteretic comparator is also reduced because of a corresponding reduction in the switching cycles. The performance of the MERC is listed in Table 5-1.

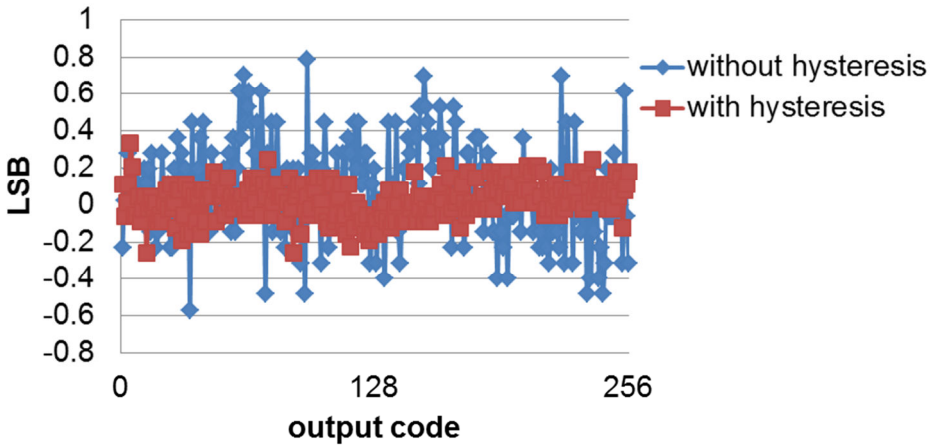


Figure 5-12. The DNL results (represented as the least significent bit (LSB)) of the MCR circuit with and without hysistersis.

Table 5-1. The performance summary of the MERC chip.

CMOS process	AMI 0.5µm
VDD	5V
Current range of the MRC	±100nA
sensitivity	150fA (without hysteresis) 60fA (with 100mV hysteresis)
Input range of the potentiostat	0.1V - 4.8V

5.5.2 Electrochemical test results

To verify the amperometry and impedimetry function of the MERC, the chip was used to measure Herceptin, a therapeutic monoclonal antibody (mAb) for the treatment of HER2-positive breast cancer [109]. Trials have shown that Herceptin reduces the risk of recurrence of early HER2-positive breast cancer by approximately 50% [110-113]. Herceptin influences its effectiveness, so physicians need careful monitoring of Herceptin

levels in the patients. The test results of cyclic voltammetry and impedimetricy measured by MERC are presented in this section.

5.5.2.1 Materials

Peptide CH-19 as a bio-probe was used to detect Herceptin in this assay. Peptide CH-19 (primary sequence: CGSGSGSQLGPYELWELSH) is a short synthetic peptide that has high specificity binding to Herceptin with rapid response time and low cost advantages [114]. Synthetic peptide, designated CH-19, was purchased from Bio. Basic, Inc. (Ontario, Canada) and received in lyophilized condition. The quality of CH-19 was assessed by high performance liquid chromatography (HPLC) and confirmed through matrix-assisted laser desorption/ionization (MALDI) mass spectrometry analysis (Purity > 95%). Therapeutic monoclonal antibody, Herceptin® (Trastuzumab) was provided by Beaumont Hospital, Royal Oak, Michigan. The UltraPureTM distilled water (Cat. No. 10977-015) and phosphate buffered saline (PBS, Cat. No. 10010-049) were obtained from Invitrogen Corporation. These chemical materials were prepared by Dr. Yuqin Shang, Oakland University.

Interdigitated electrodes (IDE) are commonly used for impedance sensing applications. [115]. IDE was used as the electrode in this assay. IDE was fabricated in Dr. Mason's lab. Work was completed by colleague Xiaoyi Mu. First, the silicon substrate with 1.5um thick thermal oxide was cleaned by acetone, isopropanol and DI water for 1min each respectively, followed by dehydrating on hotplate at 100°C for 10min. Then the substrate was spin-coated with Shipley 1813 photoresist at 3000rpm and soft-baked in

an oven at 95°C for 10 minutes. Afterward it was exposed through a designed photomask by UV light at 365nm wavelength for 10 seconds using a mask aligner. Next, the photoresist was developed in AZ352 developer for 45 seconds. Then the photoresist was hard-baked at 120°C for 1 minute. A 50Å Ti (titanium) adhesion layer and 1000Å Au (gold) layer were deposited on the substrate using Edward 360 thermal evaporator at 1×10^{-6} Torr. The photoresist was then lifted-off by rinsing with acetone, isopropanol and DI water. The geometry of the micro-fabricated electrodes is shown in Figure 5-13. The gap between two fingers is 15µm and each electrode consists of 12 fingers with size of 300µm x 30µm.

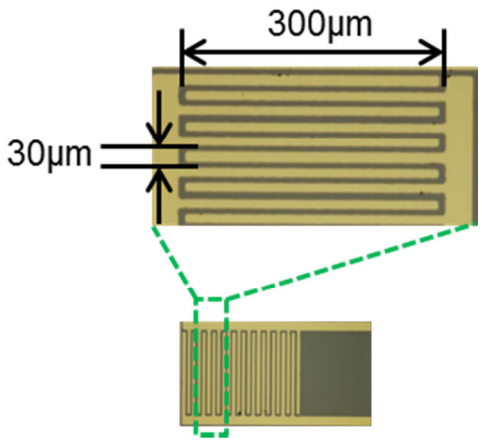


Figure 5-13. The photo of the interdigitated electrode (IDE).

5.5.2.2 Test setup

To verify the electrochemical measurement capability of MERC, a test bench composed of MERC, one IDE, and a PC with a DAQ card 6259, and a LabVIEW user

interface was developed. A triangle waveform (for CV measurement) and a sine waveform (for EIS measurement) working as the stimulus signals for the Herceptin interface, were generated by the DAQ card with programmable amplitude and speed. The MCR digital output data was also recorded by the DAQ card 6259. The schematic of the test bench is shown in Figure 5-14.

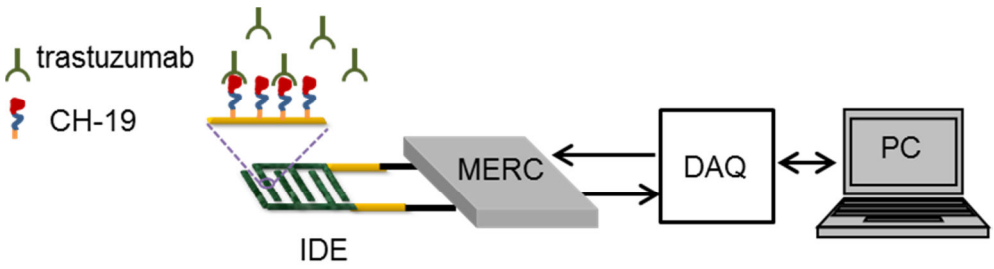


Figure 5-14. The test bench schematic for MERC chip with Herceptin bio-interface.

5.5.2.3 Surface immobilization

CH-19 immobilization onto an IDE surface was carried out as described for gold electrode preparation with modifications [116-118]. First, the IDE surface was cleared by one drop of a concentrated nitric and sulfuric acid mixture (1:1 v/v). Then, the IDE surface was washed thoroughly by biological grade water, and pure ethanol (200 proof) three times to remove impurities. The IDE surface was then dried under pure nitrogen stream. In order to functionalize the IDE, the freshly cleaned IDE surface was immersed in peptide CH-19 solution (1 mM in ultrapure water) and kept at 4 ^{o}C. After an overnight incubation at 4 ^{o}C, the surface of the CH-19 modified IDE was rinsed thoroughly with bio-grade water and PBS buffer (pH 7.4). The IDE surface functionalized with peptide

CH-19 was then ready for electrochemical measurements. The CH-19 immobilization was developed by Dr. Yuqin Shang, Oakland University.

5.5.2.4 Measurement and results

To verify the C-19 formation performance, cyclic voltammetry (CV) was applied to the CH-19 modified IDE. A typical electrolyte solution with 1M potassium chloride and 0.5mM potassium ferricyanide was prepared. The cyclic voltammetry measurements of the modified IDE and bared IED were performed at room temperature at scan rates of 100mV/s. The bared gold IDE was measured by a commercial potentiostat (CHI760C, CH Instruments Inc.). There were reduction/oxidation peak currents for the bared gold electrode in the results, as shown in Figure 5-15. MERC was used to do the CV to characterize the modified IDE performance. The result of modified IDE is also shown in Figure 5-15 where no reduction/oxidation peak currents were found. That proved the whole gold electrode was coated with CH-19 as expected.

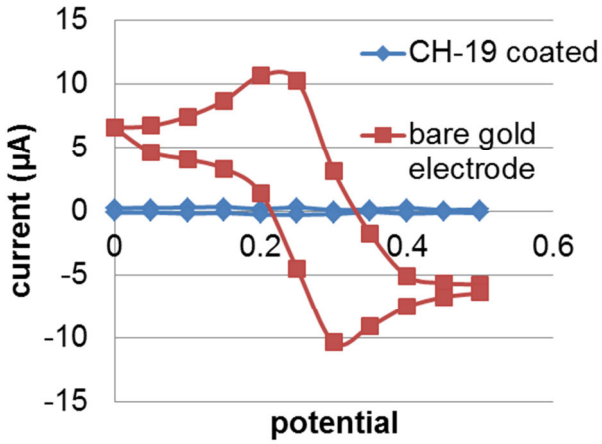


Figure 5-15. The CV measurement of the gold electrode before and after coating with peptide CH-19.

Impedance measurements were conducted with the MERC chip over the frequency range of 10 to 100 Hz after 0.001 pg/µL of Herceptin was added. For comparison, this biointerface was tested using a commercial impedance instrument (CHI 760 C) and those results are included in Figure 5-16. These data demonstrate that the MERC circuit generates similar results as in commercial equipment.

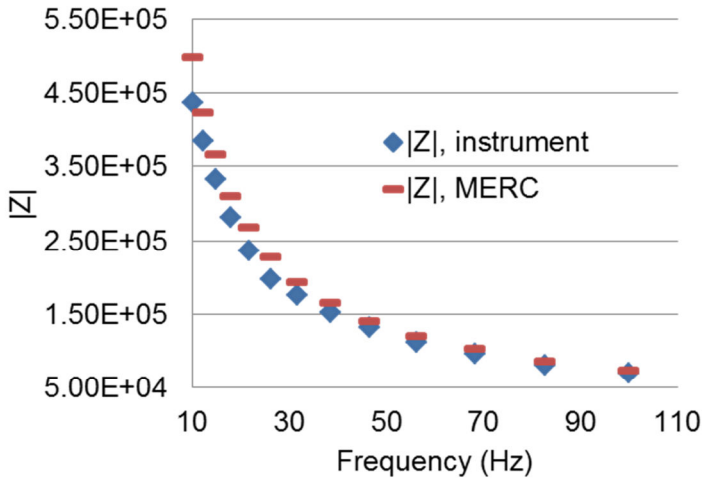


Figure 5-16. The impedance of Herceptin measured by the commercial instrument and MERC.

The interface impedance is proportional to the Herceptin concentration. Three calibrators containing 0.001, 0.01, and 0.1 pg/μL of Herceptin in HBS-EP buffer were prepared prior to each impedance assay. The test results shown in Figure 5-17 present that the impedimetric biosensor can detect the Herceptin concentration down to 0.001pg/μL with a high linear response (R^2=0.995).

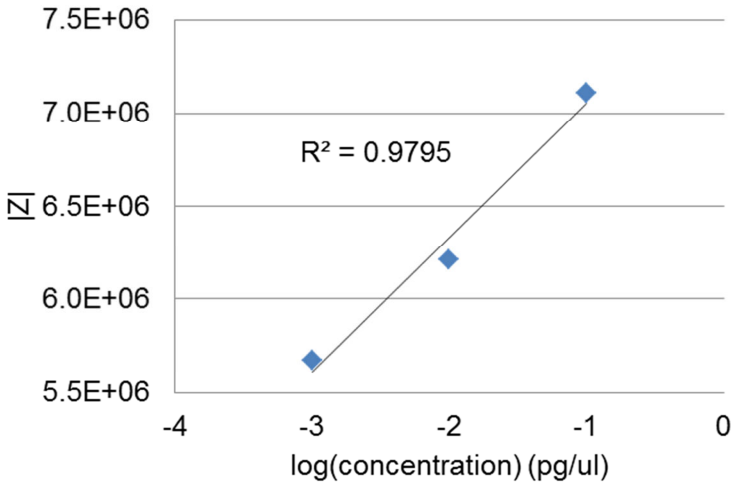


Figure 5-17. The Herceptin concentration curve vs. the impedance measured by MERC chip. A high level of linearity (R^2=0.9795) was achieved.

Chapter 6 CMOS Electrochemical Instrumentation Array for On-chip High Throughput Characterization of Single Ion Channel Proteins

Membrane proteins, and in particular ion channels, are main drug targets, and thus, ion channels have received widespread recognition for their application in biosensors, drug discovery, and protein/ligand screening. To study the characters of ion channels, a 1024-element high throughput array concept was proposed by our lab for rapid and simultaneous ion channel characterization. An electrochemical array instrumentation circuit for single ion channel characterization was developed to address the many challenges in forming high throughput chip-scale biosensor arrays with simultaneous characterization of multiple bio-interfaces, which is one of the thesis goals. A smart and power/hardware efficient instrumentation circuit architecture was developed to address the cross talk noise caused by simultaneous measurement, the large array parasitic capacitors, and the multi-modes electrochemical measurements requirements. Moreover, the instrumentation circuits provide a solution for the noise floor vs. bandwidth tradeoff in a manner that permits both single ion channel current resolution (pA) as well as tens of MHz bandwidth.

6.1 Single Ion Channel Detection: History and Background

Approximately one-third of all proteins comprising pores, ion channels, receptors, and enzymes are membrane associated. Information about how membrane proteins work, their interactions with lipids and other proteins, and their dynamics and structure, is essential for the understanding of biological membranes and cell functioning in general. The implications of ion channels in a variety of diseases, including diabetes, epilepsy, hypertension, cancer and even chronic pain, have signaled them as pivotal drug targets [119]. Approximately 15% of the world's 100 top-selling drugs are targeted at ion channels [120]. Thus, ion channels have received widespread recognition for their application in biosensors, drug discovery, and protein/ligand screening.

To understand the kinetic of ion channels and other membrane proteins, two techniques, patch clamp and pore-based membranes, have been applied for single ion channel detection (SICD). Patch clamp has been used for characterizing ion channels in membrane proteins since 1970s. Patch clamp is a laboratory technique in electrophysiology that allows for the study of single or multiple ion channels in cells. Patch clamp recording uses a glass micropipette that has an open tip diameter of about one micrometer. The open tip encloses a membrane surface area or "patch" that often contains one or a few ion channel molecules [121]. The major drawback of patch clamp is the lack of control over the protein and lipid composition of the membrane patch. The pore-based membrane technique overcomes this drawback by incorporating a purified channel protein into a bilayer lipid membrane (BLM) with a controlled lipid environment.

Such BLMs have a simple structure with predictable, well-defined electrical properties [122]. The pore-based BLM method is preferred when a membrane protein needs to be characterized in a controlled environment.

Both patch clamp and pore based membrane techniques can be measured by optical or electrochemical instrumentation. Traditionally, ion channel detection was based on fluorescence. In fluorescence detection methods, target molecules are labeled fluorescently and the opening and closing rates of molecules are measured by optical techniques such as fluorescence correlation spectroscopy and single-molecule fluorescence resonance energy transfer. Despite the high specificity of fluorescence based techniques , the fact that light is used as an intermediary between the biological system and measurement electronics results in fundamental constraints in resolution and bandwidth due to the countable number of photons emitted [123].

Electrochemical techniques are now being explored which provide higher bandwidth ion channel measurements compared with optical techniques [124]. Moreover, electrochemical methods have the advantage of low cost and a capability for miniaturization [125] [126].

6.2 Single-Ion-Channel Array Microsystem

6.2.1 Pore-based pBLM and Electrochemical Methods

Planar lipid bilayer membrane (pBLM) is one type of artificial lipid bilayer. PBLM with pore supported technique is widely used in functional studies for single ion channels

because the pore structure supports ions passing through the ion channel. The general structure of a pore-based pBLM is presented in Figure 6-1. Two sides of the BLM are isolated in fluid chambers, which are filled with electrolyte solution. One protein is inserted in the pBLM and ions go through the ion channel under a given potential. The ion channel opening/closing events are recorded by the constant potential amperometry (CPA) technique that measures the response current pulse between electrode A and B at a DC potential. CPA is also used to evaluate the pBLM formation quality by measuring the pBLM impedance. Additionally, the electrical properties of a pBLM can be characterized using the electrochemical impedance spectroscopy (EIS) technique, which enables extraction of pBLM equivalent circuit model parameters.

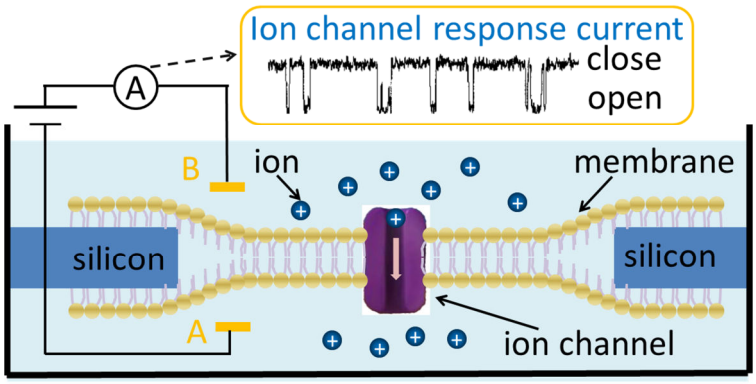


Figure 6-1. General structure of a pore-based pBLM cell with a single ion channel protein. The opening/closing events of the ion channel can be detected by monitoring response currents between electrodes A and B.

6.2.2 Microfluidic structures for self-assembled pBLM

Recently several groups have introduced microfluidic structures using poly(methyl methacrylate) (PMMA), polytetrafluoroethylene (PTFE), and polydimethylsiloxane (PDMS) to flow lipid solutions across an aperture, including a device with a 500μm hole through a glass slide [127]. Initially, it was common to construct a pBLM positioned horizontally by flowing lipid solution across an aperture so that lipid molecules self-align at the aperture where the organic lipid solution interfaces with an aqueous buffer. Alternatively, in a modern adaptation of the Montal-Mueller method that eliminates the use of heavy non-volatile solvent, an aqueous solution having a thin layer of phospholipid stock solution at the gas/liquid interface is passed across both sides of the micropore, forming phospholipid monolayers that merge to form a BLM across the aperture. Such devices typically consist of microfluidic channels on one or both sides of a substrate containing the aperture [128-130]. Aperture sizes range from 100s of micrometers in diameter to as small as sub-micron. While these reports demonstrate that micropore structures and microfluidics are well suited to forming stable BLMs, these new methods, like traditional ones, suffer from a low yield in BLM formation that makes it difficult to get consistent measurements of membrane proteins.

In contrast to horizontal devices with apertures, a new approach where the pBLM is positioned vertically within a microfluidic channel was recently reported [137-140]. The approach forgoes the need of an aperture-containing substrate and permits an array of pBLMs to be self-assembled within microchambers shaped into the sidewall of the main microfluidic channel. When a buffer and organic lipid solution are sequentially flowed through the channel, a pBLM is constructed at the mouth of each microchamber. One

PDMS microchamber with electrode fabricated by Dr. Mason's lab, as shown in Figure 6-2. The structure of the pBLM microchamber is shown in Figure 6-3(a). With one electrode in each pBLM microchamber and one electrode is in the main channel, this structure enables many electrochemical measurements to be made in parallel. This structure is also suitable for high density array formation, as illustrated in Figure 6-3(b-c). Microfluidic techniques facilitate rapid and cost-effective fabrication of BLM microarrays, whose properties vary combinatorial across the array. The capability of rapidly altering the solute environment around the pBLM by virtue of microfluidics provides be a major technical advance.

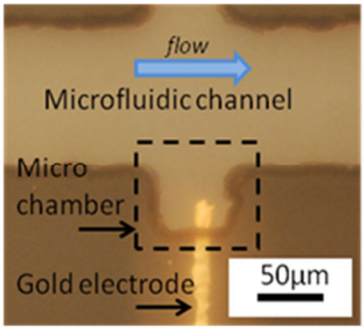


Figure 6-2. PDMS microchamber with electrode fabricated in Dr. Mason's lab. Work completed by colleague Lin Li.

6.2.3 High throughput microsystem approach

Multiple microfluidic channels provide the capability of automatic, rapid, and high throughput pBLM formation. One challenge for a high throughput SICD microsystem is the wiring bottleneck inherent in connecting hundreds of individually measurable

microchambers to instrumentation electronics. To overcome this challenge and enable high throughput membrane protein characterization, the pBLM microchamber arrays can be embedded with a CMOS electrochemical instrumentation chip. When the microfluidics are combined with CMOS instrumentation for electrical recording, the integrated system can achieve rapid and parallel-screening membrane proteins under multiple environmental conditions.

The SICD array microsystem being developed utilizes a carrier substrate to expand the surface area beyond the instrumentation chip, allowing room for multiple fluidic inlets/outlets while also connecting circuits I/O pads to external electrical contacts. The high density electrode array is fabricated on the surface of the instrumentation chip and directly connected to circuits for electrochemical readout. When connected to a computer-controlled data acquisition system, the user would have full control of the pumps and valves managing microfluidic operation as well as display and storage of characterization data. The SICD microsystem is illustrated in Figure 6-3 (c). For a typical $5 \times 5\text{mm}^2$ instrumentation chip, eight independent fluidic channels fit well within the area based on our experiences. When a buffer and organic lipid solution are sequentially flowed through the microfluidic channel, a pBLM can be constructed at the mouth of each microchamber. The width of the pBLM microchamber is 50μm and the center-center pitch of the microchambers is 80μm. 64 pBLM microchambers could be in each microfluidic channel for a $5 \times 5\text{mm}^2$ chip, making the total number of the pBLM microchambers equal to 1024. This microsystem has been designed to enabled, for the first time, simultaneous characterization of single-molecule events within multiple biomembranes.

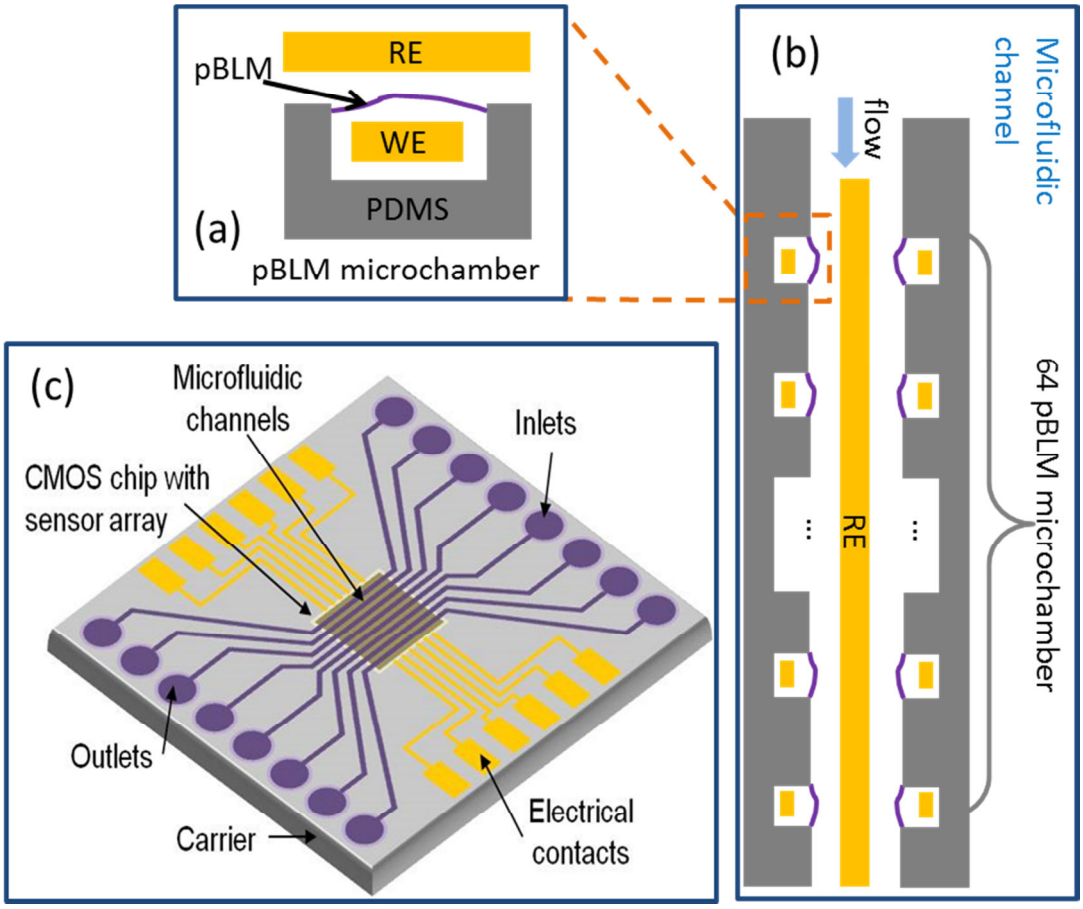


Figure 6-3. (a) The structure of one pBLM microchamber with working electrode (WE) and reference electrode (RE). (b) One microfluidic channel with shared RE. (c) Concept view of the high throughput array microsystem for single ion channel detection.

6.3. Instrumentation Circuits Requirements and Challenges

6.3.1 Multi-mode instrumentation circuits

Microfluidic-driven pBLM formation and protein characterization are complicated processes. The CMOS instrumentation circuits are designed to support multiple modes based on the needs of different assays.

Mode 1: pBLM formation quality test by CPA technique.

Mode 2: pBLM classification by EIS technique.

Mode 3: simultaneous single ion channel event detection by CPA technique.

The pBLM quality can be evaluated by the membrane impedance because a poor quality pBLM has a large leakage current (as noise) that considerably reduces the membrane impedance. In *mode 1*, the circuit will determine if/when a high quality membrane is formed by comparing the pBLM impedance with a programmable threshold value selected from 100MΩ and 1GΩ. Generally, the impedance of a good quality pBLM should be above 1GΩ [8], and when the pBLM impedance is less than 100MΩ it is assumed to be poor. Any poor pBLMs will be skipped over during subsequent modes.

Mode 2 provides pBLM classification via EIS characterization. The different formation shapes of pBLM, as shown in Figure 6-4, could be considered as different classes. Different classes of pBLM have unique phase/amplitude characteristics, which

provide a second layer of information to describe the protein's environment beyond the impedance information provided in mode 1.

Mode 3 is the most challenging because it requires recording single channel opening/closing events with MHz speed and sub-pA resolution. The instrumentation electronics have to guarantee mode 3 performances, which require ultra-low noise and high speed readout circuits.

Figure 6-4. Example for different classes of pBLMs.

6.3.2 Instrumentation circuits requirements and challenges

The multi-modes measurement, single-molecule resolution, and high density array instrumentation requirements bring a lot of challenges in the circuit implementation. One challenge is addressing the noise floor vs. bandwidth tradeoff in a manner that permits both pA resolution as well as tens of MHz bandwidth, as needed to measure typical single ion channel events. Assuming it is necessary to achieve a minimum SNR of around 3, a

noise floor of less than 330fA is needed to record the a 1pA response of a single ion channel. The array requirement adds even more of a challenge because of the crosstalk noise between the tens of readout circuits working simultaneously. Further difficulty is added by the need to keep the circuit small so that many readout blocks can be placed on a chip for parallel array measurement. Additionally, power consumption must be closely managed to maintain a surface temperature suitable for pBLMs (~40ºC max).

6.4. Instrumentation Array Approach

To address the requirements and realize high throughput chip-scale biosensor arrays with simultaneous characterization of multiple bio-interfaces, a single protein electrochemical characterization (SPEC) chip was designed. For a 1024-element BLM array with simultaneous characterization, a straightforward approach is to have 1024 CPA/EIS readout blocks. However, the power consumption for 1024 readout blocks would be extreme (up to hundreds of watts), which would generate local hotspots that would degrade pBLM interface.

Because of the delicate nature of pBLM formation, this initial step of array formation can be expected to have a low yield, around 30% based on empirical evidence. Our experience also suggests the good quality pBLMs will occur roughly equally in three distinct structural classes. Furthermore, we estimate that the likelihood of populating an individual pBLM with a single membrane protein to be about 20% after experimental optimization. In other words, we expect a very low yield of single-protein, single-pBML-class interfaces, demanding a high density array. However, this low yield provides an

opportunity for several pBLM interfaces to share one CPA/EIS readout circuit. Based on these estimates, we expect 1-3 good quality, single-class, single-protein interfaces within each microfluidic channel (the calculation detail shown in appendix). Thus, the instrumentation array has been designed with four CPA/EIS readout circuits per channel. This should ensure capture of single ion channel events, simultaneously across most functional interfaces, while also achieving hardware efficiency; a total of 32 CPA/EIS readout circuits occupies only 3.1% of area required for an instrumentation chip with 1024 CPA/EIS circuits and enables implementation within a $5x5mm^2$ chip.

Tens of CPA/EIS current readout circuits working simultaneously introduce a noise immunity challenge. The high throughput array also has a large parasitic capacitance that distorts the electrochemical current signals. To solve these problems, an in-pixel electrochemical current amplifier for each pBLM element was chosen in the SPEC chip. This pixel amplifier significantly increases immunity to signal interference, solves the signal distortion caused by the array parasitic capacitance, and loosens the resolution requirement of the CPA/EIS readout circuit.

The architecture of the designed SPEC chip is shown in Figure 6-5. There are eight independent potentiostats that set the independent bias potential for each microfluidic channel during CPA and EIS measurement. Digital memory is used to buffer the results between the CPA/EIS readout and uploading to an external host system through a serial peripheral interface communication bus. A digital control block manages the operation mode. Potentiostat and CPA/EIS readout circuit specifications for each mode are listed in Table 6-1.

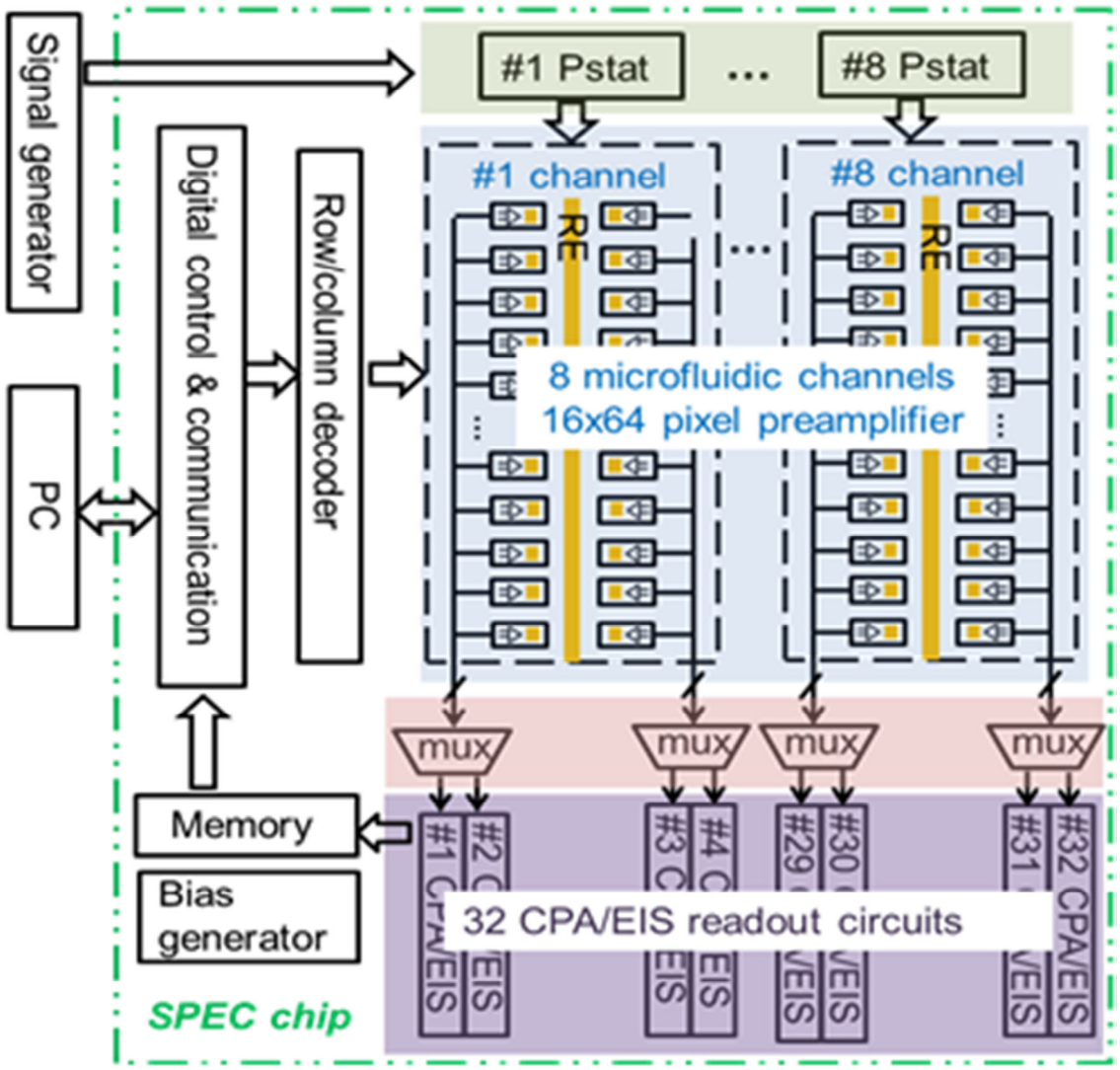


Figure 6-5. Architecture of the single protein electrochemical characterization (SPEC) high density array chip.

Table 6-1. The performance requirement for potentiostat and readout circuits for each mode.

	potentiostat	CPA/EIS readout circuit
mode 1 (CPA)	(1) frequency: DC (2) voltage range: -250mV - 250mV' (3) step resolution: 10mV	(1)current readout mode: DC (2)current range: pA to mA (3)bandwidth: 10kHz
mode 2 (EIS)	(1) frequency range: 100mHz-100Hz; (2) AC amplitude: 10mV; (3) DC bias range: -±250mV;	(1)current readout mode: AC (2)current range: pA to mA (3)phase range: -180° - 180° (4)bandwidth: 100kHz
mode 3 (CPA)	(1) frequency: DC (2) voltage range: ±250mV; (3) step resolution: 10mV;	(1)current readout mode: DC (2)current range: pA to 200pA (3)resolution: 300fA (4)bandwidth: 10MHz

6.5 CMOS Implementation

6.5.1 Preamplifier design

Noise and speed are the two key considerations in the pixel amplifier design because the input signal of the amplifier is a high speed (down to 10μs pulse width) and weak (~pA) current pulse. A resistive feedback amplifier is simple to implement, but it suffers from the noise generated by the feedback resistor. A capacitor feedback amplifier is not suitable for measuring high speed low-level signals because the feedback capacitor

limits amplifier speed. A current conveyor was selected as the amplifier in our design because it is good at high speed and for weak current amplification.

A cascade current mirror structure was utilized in the pixel amplifier to reduce crosstalk noise generated by the high speed switch coupling. The schematic of the pixel amplifier is shown in Figure 6-6. Transistor M1 is a current sink controlled by 'Bias' that ensures amplification of the bi-direction ion-channel current. 'Sel' is the pixel selection signal. A large, pF-level, column parasitic capacitor (Cp) is associated with each pixel amplifier output in the high throughput array, and the total gain of the amplifier was set as 25 to ensure capability to drive the Cp load. To eliminate the delay caused by transistor parasitic capacitances, the minimal gate length (L=0.6μm) was selected for all transistors. The layout size of the pixel amplifier is 27μm × 80μm, as shown in Figure 6-7, which is small enough to ensure that each pBLM microchamber has its own pixel amplifier.

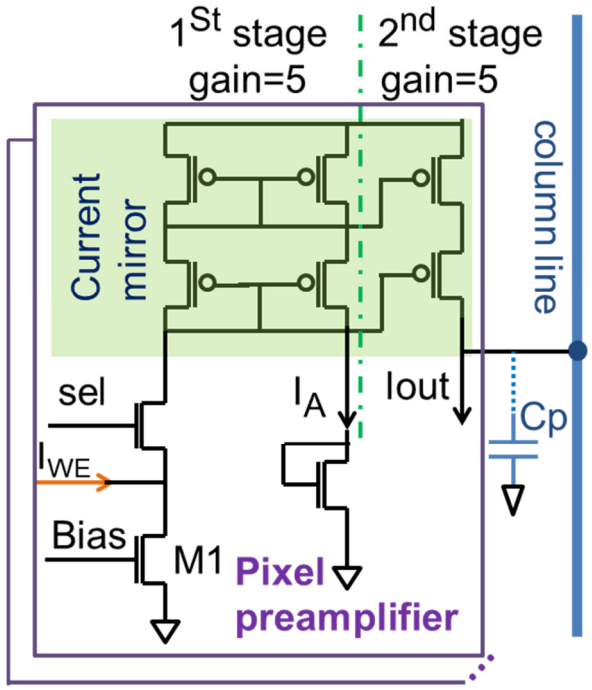


Figure 6-6. Schematic of the two stages current conveyor pixel preamplifier.

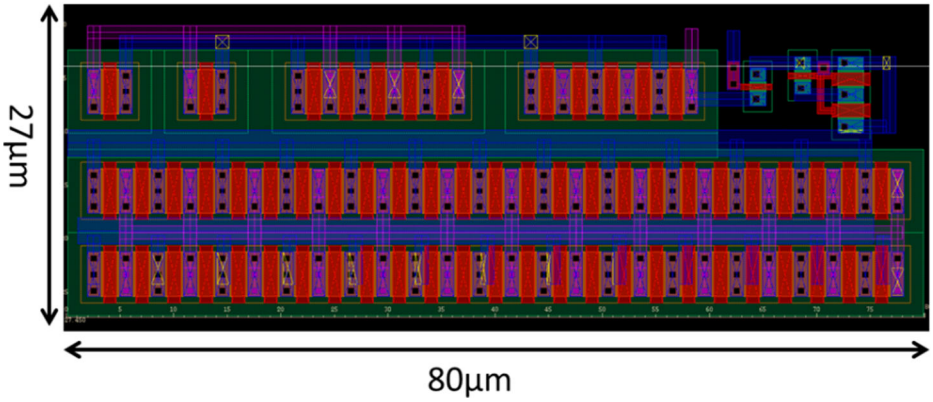


Figure 6-7. Layout of the pixel preamplifier.

6.5.2 CPA/EIS blocks

The multi-mode electrochemical readout circuit introduced in Chapter 5 is a great candidate for the CPA/EIS blocks in terms of function and resolution. The Chapter 5 readout circuit is designed for an input signal less than 10KHZ (typical biosensors speed range), which is not capable to detect the ion channel events with tens of microseconds time scale [124]. The readout speed of the Chapter 5 circuit is limited by the large parasitic resistance and capacitance of the 0.5μm CMOS process. This limitation could be solved by shifting the Chapter 5 circuit to a smaller size CMOS process in order to reduce the parasitic resistance and capacitance. Based on our experience, we believe that shifting the Chapter 5 readout circuit to a more advanced technology is more like an engineering project. Besides changing processes, an alternative solution is using commercial ADCs to readout the preamplifier's output current. No matter which method, the CPA/EIS block is not the most challenging component in the instrumentation circuit design.

6.6 Simulation Results

6.6.1 Simulation condition

The pixel amplifier was designed at AMI 0.5μm CMOS technology and simulated in Cadence Spectre. The simulation parameters are listed in Table 6-2. Cp = 1.5 pF was added at the load of the pixel amplifier in the simulation. To verify the function of the pixel amplifier, a 5pA, 10μs width current pulse was connected to the input of the pixel

amplifier to mimic the fastest single ion channel opening/closing current. The parameters used in the simulation are summarized in Table 6-3.

Table 6-2. Simulation parameters with Candece Spectre simulator.

Process	2-Poly 3-Metal, AMI 0.5μm
VDD	5 V
temperature	25°C
Simulation model	ami06N, ami06P @ TT
Load capacitor	1.5pF

6.6.2 Simulation results

To verify the function of the preamplifier, a 5pA, 10μs width current pulse is connected to the input of the preamplifier and monitors the first and second stage current mirror output. The simulation results are presented in Figure 6-8, where the value of I_A and I_{OUT} are as expected.

The pulse waveform distortion caused by the parasitic capacitance can be identified as a pulse width distortion percentage (PWDP), as shown in Figure 6-9. The purple is the original pulse waveform, and the black is the distorted waveform. To calculate the processing speed limitation of the preamplifier, a series of various width pulse current inputs are simulated. The simulation results are shown in Figure 6-10. The PWDP for the 10us pulse width current (the fastest ion channel speed) is only 1.04%. Thus, the pixel amplifier is fast enough to track the high speed opening/closing events.

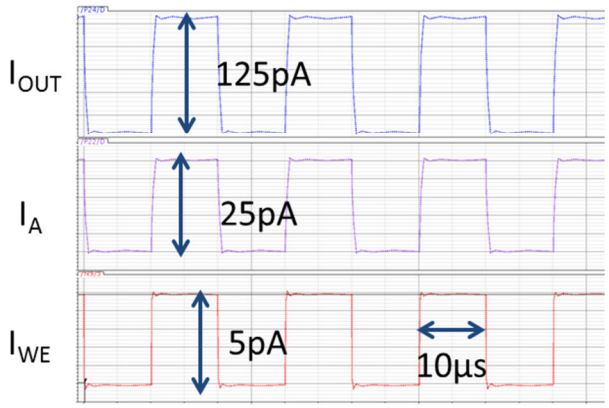
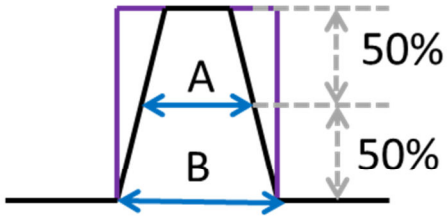


Figure 6-8. The simulation results of the first stage output (I_A) and second stage ouput (I_{OUT}) of the preamplifier with a 5pA, 10µs width pulse current input (I_{WE}).



$$PWDP = \frac{(B-A)}{B} \times 100\%$$

Figure 6-9. The definition of the pulse width distortion percentage (PWDP).

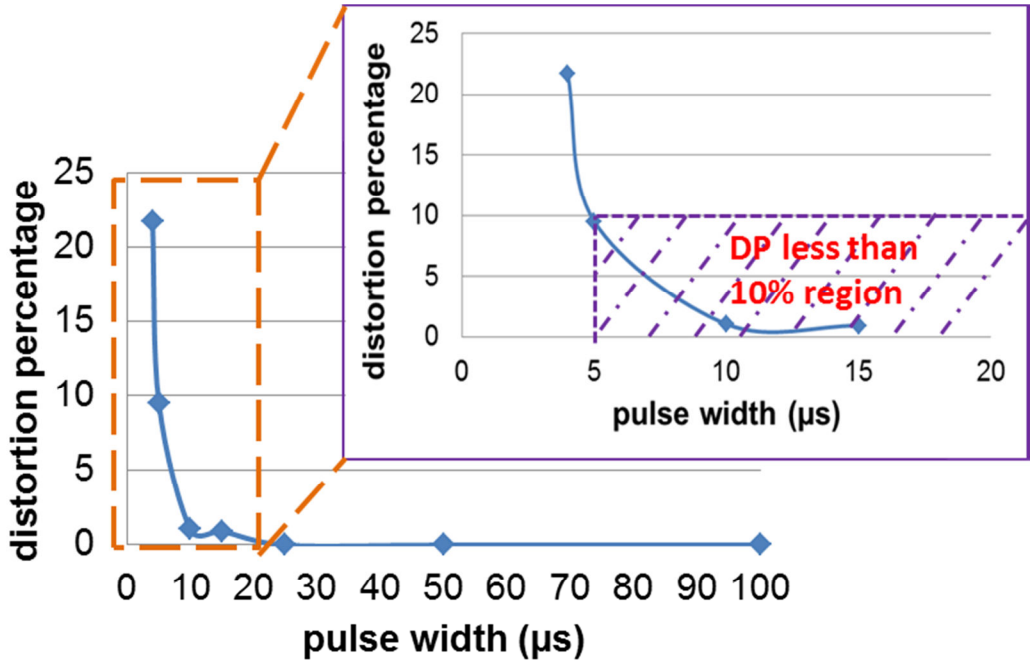


Figure 6-10. Simulated results of the distortion percentage (DP) with various pulse widths of the input current (I_{WE}).

In order to evaluate the pixel amplifier operation in a larger scale biosensor array, dependence of PWDP on array capacitance was simulated. Figure 6-11 shows the simulated PWDP of I_{OUT} under various array capacitor values for a 10µs pulse input I_{WE}. The PWDP is only 2% even for a large Cp = 15pF.

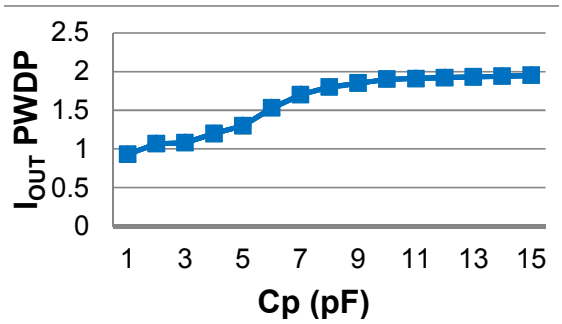


Figure 6-11. Simulated I_{OUT} pulse width distortion percentage (PWDP) as a function of the column line parastic capacitance (Cp).

6.6.3 Power consumption analysis

To manage power consumption, the preamplifiers and readout block will be realized with the least power needed to achieve performance goals, and power management schemes will be implemented to regulate surface heating. The estimated power consumption of each component is listed in Table 6-3. The total power consumption of SICD instrumentation circuits is only 200mW. Based on our prior work with CMOS heaters to control biointerface temperatures [131], ~22.75W/mm^2 is needed to heat a surface liquid to 50^{o}C, so it appears that it is easy to avoid the local overheating.

Table 6-3. The power consumption estimation of the single ion channel detection instrumentation circuits.

Component	**Quality**	**Power/element**
preamplifier	1024	15.5μW
CPA/EIS readout circuit	32	5.4mW
Bias	1	50μW
Row/column selector &digital communication	1	100μW-1mW
Total power		**~200mW**

6.6.4 Area estimation

Based on our previous experience on the potentiostat, row/column decoder, bias, memory and the digital control & communication circuits, an estimated area of the designed SICD circuits is listed in Table 6-4. The estimated area of the potentiostat, bias, CPA/EIS readout, row/column decoder, digital controller and communication blocks are referenced [64, 106, 131], The memory size is calculated based on that the area of a standard 6-transitor memory cell is $25x33\mu m^2$, and the total needed number of the memory is 2^8x32 (assume the resolution of CPA/EIS is 8 bit). The total estimated area of the designed SICD instrumentation circuit is $5.36mm^2$, which is within the $5x5mm^2$ chip size goal.

Table 6-4. Area estimation for each components in the single ion channel detection instrumentation circuit with AMI 0.5um process.

Item	**Area/block**	**Number of item**
Potentiostat	200x300μm^2	8
Pixel preamplifier	27x80 μm^2	1024
CPA/EIS readout circuit	500x100μm^2	32
Bias	300x300μm^2	1
Row/column decoder	300x500μm^2	1
Memory	25x33μm^2 x2^{8}x32	1
Digital control &communication	~200x400μm^2	1
Total area		**9.96mm^2**

Chapter 7 Summary and Future Work

7.1 Summary

This thesis research developed technologies that overcome the challenges of implementing CMOS instrumentation circuits for miniaturized high throughput biosensor array microsystems. The requirements of the electrochemical instrumentation have been studied, and different structures of amperometric and impedimetric instrumentation have been evaluated. A high resolution amperometric instrumentation circuit based on correlated double sampling (CDS) technique was developed as a low-noise solution for readout of the weak signals in an array. Furthermore, a compact, low power, impedance analysis circuit that utilizes frequency response analysis (FRA) method to extract real and imaginary impedance components has been developed. A multi-mode electrochemical instrumentation circuit was implemented for protein characterization and sensing while sharing hardware resources. Finally, a CMOS monolithic electrochemical instrumentation circuit architecture for high throughput, single protein, characterization was designed, enabling a significance improvement in the time and cost to acquire statistically relevant single protein measurements.

The work in this thesis provides the following significant contributions:

Developed high performance electrochemical instrumentation for miniaturized biosensor array microsystems

A CMOS amperometric biosensor readout circuit with current resolution of 1pA has been developed. Furthermore, a new compact, low power, ~100fA current resolution impedance analysis circuit that utilizes mixed-mode signal processing to extract real and imaginary impedance components has been developed and tested with an on-chip protein interface. Very good agreements were observed between the commercial instrument and the CMOS amperometric instrumentation circuit and the impedimetric instrumentation circuit, respectively.

Implemented a hardware efficient multi-mode CMOS electrochemical readout circuit for biointerfaces characterization and sensing

To realize a multi-protein array of sensors with different instrumentation needs, a hardware efficient CMOS electrochemical circuit has been designed to achieve both amperometric and impedimetric measurement while sharing hardware source. The area of one channel multi-mode readout circuit is 0.045mm^2, which indicates around 500 readout circuits integrated in a be in a 5x5mm^2 chip. A hysteretic comparator was applied in this readout circuit with improved resolution and reduced power consumption. Functionality of the multi-mode instrumentation circuit was verified by characterization of a Herceptin biosensor useful for detecting cancer biomarkers.

Developed a novel 1000-element array instrumentation architecture that permits rapid high-throughput characterization of membrane proteins with single protein resolution within a chip-scale

By integrating an understanding of both protein assays challenges and microelectronics design limitations, an intelligent instrumentation circuit architecture was developed for a complex, high throughput single-protein array. The pixel preamplifier structure overcomes the cross talk noise caused by the simultaneous measurement and the signal distortion caused by the large array parasitic capacitors. Simulation results of the array instrumentation circuit demonstrates capability to detect the pA-level single protein current with more than 10MHZ bandwidth. The total area of the designed instrumentation circuit easily permits a 1000-element array within a silicon chip of only 9.96mm^2.

7.2 Future Work

This thesis work demonstrates high performance electrochemical instrumentation circuits that enable simultaneous characterization of multiple protein interfaces in a high throughput chip-scale biosensor arrays microsystem. Based on the results in this research, there are some promising directions for future research.

A. CMOS implementation for single ion channel instrumentation circuits

The architecture of the single ion channel detection (SICD) instrumentation circuit has been developed in Chapter 6. The next step is to implement the SICD instrumentation circuit in an advance CMOS process. To achieve the best figure of merit (includes the bandwidth, power consumption, noise performance and area parameters) of the

instrumentation circuit, various advanced CMOS processes have been analyzed. Based on our analysis, the best CMOS process for the SICD instrumentation is 0.25μm CMOS process. In the future, the SICD instrumentation could be implemented in this process or alterative process to realize a functional high throughput membrane protein array characterization system.

B. Development of a "smart" monolithic electrochemical measurement device

Today, commercial controllers are powerful tools that can provide the hardware necessary to control external CMOS circuits, analyze data, and communicate to an external system such as a wireless mesh radio or a laptop PC. For example, the MSP430 is an ultra-low power controller. It supports a variety of communication standards permitting a wide range of digital interfaces with simple software modifications. It also includes DACs that can generate various types of waveform as stimulus signals. The developed CMOS instrumentation associated with a commercial controller could enable a compact monolithic electrochemical measurement device that could be widely used in point of care applications.

APPENDIX

APPENDIX

Estimates that the percent of good quality pBLM produced will be around 30%, the percentage of *Class 1* pBLMs will be about 33%, and the percentage of membranes including only single ion channels will be about 20%. If we assume that the pBLMs follow a normal distribution, then there will be around 0.5~1.6 good quality, *Class 1*, single-ion-channel pBLMs in one column. The calculation for this estimation is as follows

(1) Mode 1, calculate the number of the 25% good quality pBLM. Assume pBLMs the normal distribution: (μ=64*25%=16, σ=4) and [μ-2σ, μ+2σ] covers 95% confidence interval.

Then (μ-2σ) =8, (μ+2σ) =24. [8, 24] will cover 95% range

(2) Mode 2, calculate the number of pBLM in one class. Assume 1/3 pBLMs are one pBLM class

[8, 24]*1/3=[2.7, 8] (6-1)

(3) Mode 3, calculate the number single ion channel pBLM

[2.7, 8]*20% = [0.5, 1.6] (6-2)

Based on (6-2), there will be 0.5~1.6 (with 95% confidence interval) single protein pBLMs in each column, so it is reasonable to believe that two CPA/EIS readout circuits are enough in each column for single protein pBLM detection. Two readout circuits not only ensures capture of the single ion channels events, but also ensures hardware efficiency. The total number of CPA/EIS readout circuits in the instrumentation is 32.

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