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CLASS G AMPLIFIER

By

Adam Darwin Downey

A THESIS

Submitted to
Michigan State University
in partial fulfillment of the requirements
for the degree of

MASTER OF SCIENCE

Department of Electrical and Computer Engineering

2002

ABSTRACT

CLASS G AMPLIFIER

By

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Power efficient circuits are becoming more important as technology advances to using more portable devices such as cell phones, walkmans, and laptop computers. A Class G Amplifier is a power amplifier that can achieve better power efficiency than the Class B Amplifier. This thesis presents using an operational amplifier with a Class G power stage and feedback to lower the total harmonic distortion of the amplifier. This thesis shows how to solve the stability problems associated with the Class G Amplifier. Also presented here is the examined efficiency of this amplifier. In addition, this thesis presents the lab work verifying the performance of the amplifier.

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ACKNOWLEDGEMENTS

I would like to thank Dr. Gregory M. Wierzba for his guidance in the thesis. I would also like to thank my parents for their continuing support in my efforts to obtain my Master's degree.

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Chapter 1: Introduction and Background

1.1 Introduction

In the modern world, audio amplifiers sacrifice power efficiency for better sound quality. However, with the increasing use of portable devices such as cell phones, walkmans, and laptop computers, the need for audio circuits to use less battery power is increasing. With a more efficient amplifier, a large power amplifier could be made smaller because the amplifier would operate at lower temperatures, which would require less heat sinks. There are articles that discuss using a Class G amplifier for an improved efficiency circuit [7] [8] [10]. However, few discuss the overall performance of the circuit in audio applications. This thesis presents using an operational amplifier with feedback along with the Class G amplifier to produce a more efficient circuit that would be suitable for audio applications.

1.2 Background

A course in Application of Analog Integrated Circuits (ECE 484), offered at Michigan State University, was an important stimulant for the topic of this thesis. In this course, students learn about using operational amplifiers for audio circuits, filters, and some of the stability problems associated with them. Motorola expressed interest in a study of the Class G amplifier to increase battery life in cell phones. With an existing interest in audio circuits and an application for a major company, this inspired the author of this thesis to conduct research on the Class G amplifier.

1.3 Thesis Outline

The thesis begins in chapter two by explaining the design of a Class G output stage. This chapter shows two possible designs for the output stage with equations and shows which design will be better to use in this thesis. Chapter three introduces using an operational amplifier with feedback to the Class G output stage to lower the distortion. Chapter four addresses some known issues with this Class G amplifier before building the circuit in the lab for testing. In chapter five, construction details as well as performance results are presented. This chapter will show stability problems with this new amplifier design. Chapter six analyzes the lab data and uses PSpice to located the stability problem by making the computer simulation match the results found in lab. Chapter seven performs a Beta Network Analysis on the computer simulation circuit that matches the lab data to further identify what is causing the stability problem. This chapter uses a new technique for finding the stability problem. A program called Sspice (Symbolic SPICE), developed by Dr. Gregory Wierzba at Michigan State University, is used to approximate the symbolic representation of the circuit when it is unstable. After identifying the problem, a solution is implemented to eliminate the stability problem. Chapter eight analyzes the efficiency and total harmonic distortion of the final circuit. Chapter nine offers some more possible design improvements. Chapter ten presents future work on using a closed-loop analysis approach to identifying stability problems. Chapter eleven presents the conclusion. The appendices contain all the PSpice simulation files. The appendices also contain information on Sspice and the Beta Network Analysis Technique. A bibliography is presented as the last chapter in this thesis.

Chapter 2: Designing Class G amplifier

2.1 Introduction

The Class G amplifier gives improved power efficiency compared to the conventional Class B amplifier. The Class B amplifier is not very efficient for small input signals because there is a large voltage drop across the output transistors with current flowing through the transistors and causing them to dissipate power as heat. The Class G amplifier switches to a lower voltage power supply during times when the input signal is small. The output transistors will not get as hot and use less power [4] [10]. This, in turn, increases the efficiency of the amplifier. This improved efficiency will keep the amplifier cooler requiring less heat sinks and will use less energy to operate. The schematic of the general design of the Class G amplifier is shown in Figure 2.1.

The Class G amplifier introduces multiple power supplies to achieve this improved efficiency. This new amplifier requires more circuitry than the class B design and careful considerations must be made to keep the circuit stable. This chapter will show two possible designs for controlling the Class G amplifier shown in Figure 2.1.

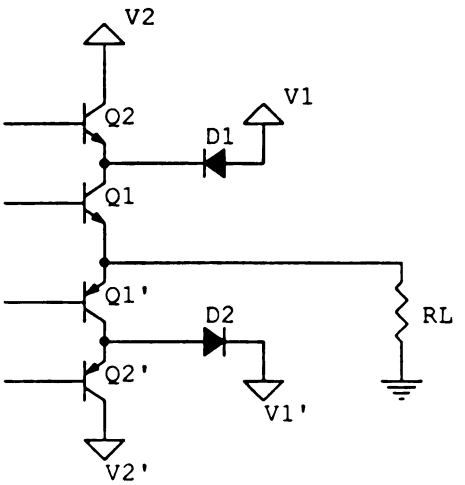


Figure 2.1: Schematic of basic Class G amplifier design

2.2 Class G Amplifier Design #1

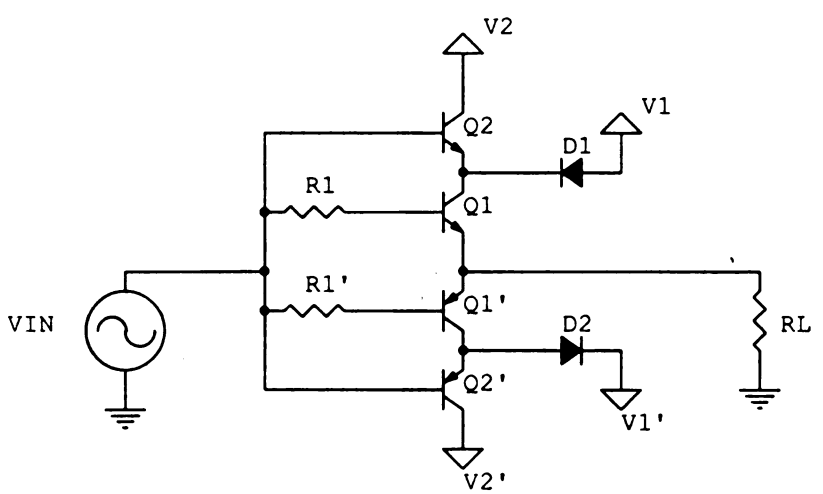


Figure 2.2: Schematic of Class G amplifier design #1

Design #1 of the Class G amplifier is shown in Figure 2.2. This design uses a complementary pair layout commonly used in the Class B amplifier design except with more transistors. A main characteristic of this design is the use of resistors in the base of transistors Q_1 and Q_1'. The functionality of this circuit design can be analyzed in stages.

The first stage will be when only the power supply, V_1 is being used. The second stage will be when only the V_2 power supply is being used. For each stage, the large signal and the small signal model of the circuit will be analyzed. The same analysis can be applied to the circuit when the negative power supplies are active due to the symmetry of the circuit design.

2.2.1 Stage One Analysis - Large Signal Model

Stage One of the Class G amplifier is operational when only the lower value power supply is being used. Particularly, for this analysis, this stage is on when the input signal is positive but small enough that only power supply, V_1, is supplying current. Power supplies, V_1', V_2, and V_2' will not be supplying any current to the circuit. Figure 2.2.1.1 shows a simplified schematic of the design #1 when V_{IN} is positive. Transistors Q_1' and Q_2' will be in Cut-Off.

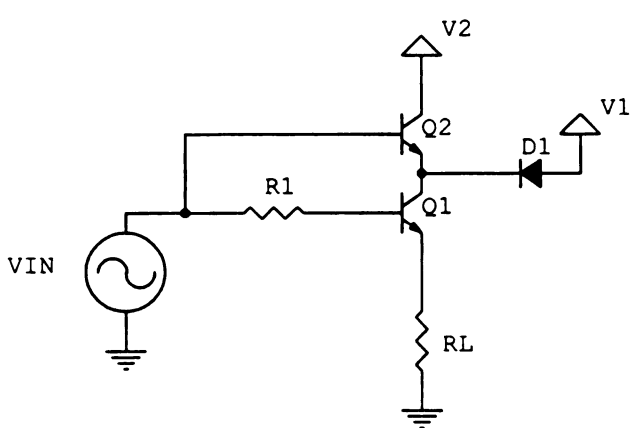


Figure 2.2.1.1: Simplified schematic of design #1 when $V_{IN} > 0$

Figure 2.2.1.2 shows the large signal model of the first stage when V_{IN} is greater than $V_{BE}(on)$ of Q_1 but less than the voltage required to put transistor,Q_2, into the Active Region and causing transistor, Q_2, to be in Cut-Off.

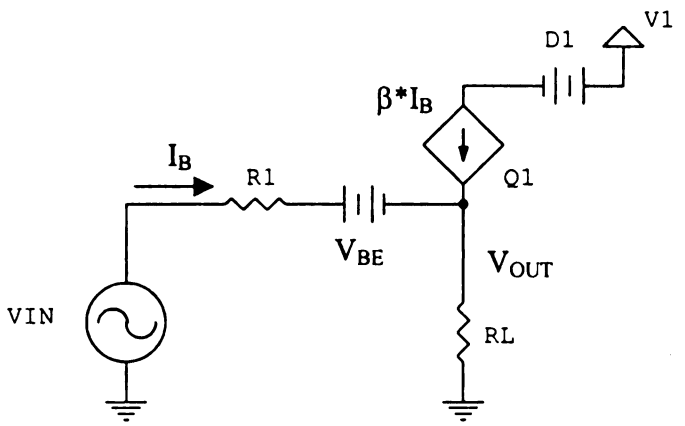


Figure 2.2.1.2: Schematic of Stage One - large signal model

The equation for V_{OUT} using the large signal model can be solved as follows.

$$V_{OUT} = (\beta+1) * I_B * R_L$$

$$I_B = \frac{V_{IN} - V_{OUT} - V_{BE(ON)}}{R_1}$$

$$V_{OUT} = (\beta+1) * \frac{(V_{IN} - V_{OUT} - V_{BE(ON)})}{R_1} * R_L$$

$$= (\beta+1) * (V_{IN} - V_{BE(ON)}) * \frac{R_L}{R_1} - (\beta+1) * V_{OUT} * \frac{R_L}{R_1}$$

$$= \frac{(\beta+1) * (V_{IN} - V_{BE(ON)})}{1 + (\beta+1) * \frac{R_L}{R_1}} * \frac{R_L}{R_1}$$

$$= \frac{(\beta+1) * (V_{IN} - V_{BE(ON)})}{\frac{R_1}{R_L} + (\beta+1)}$$

$$\boxed{V_{OUT} = \frac{(V_{IN} - V_{BE(ON)})}{\frac{R_1}{R_L * (\beta+1)} + 1}}$$

The equation for V_{OUT} shows that the smaller R_1 is, the closer V_{OUT} will equal V_{IN} - $V_{BE(ON)}$.

Using PSpice, an example of what V_{IN} and V_{OUT} would look when only the smaller power supplies are being used is shown in Figure 2.1.1.3. The simplified schematic of the circuit simulated is shown in Figure 2.1.1.4.

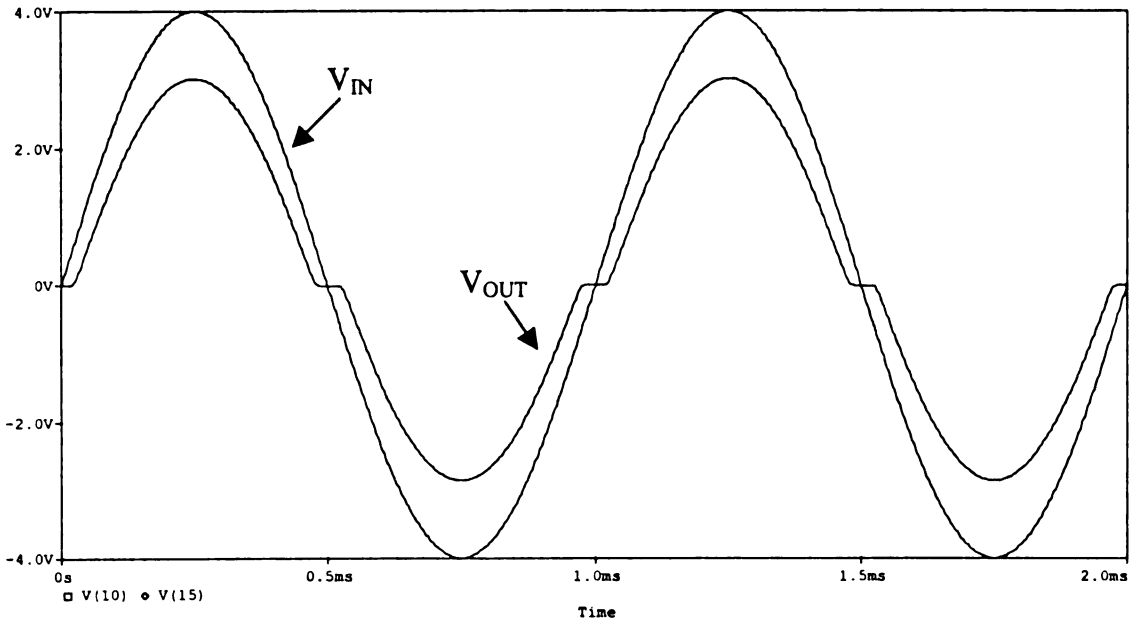


Figure 2.1.1.3: Graph of Stage One V_{IN} and V_{OUT}

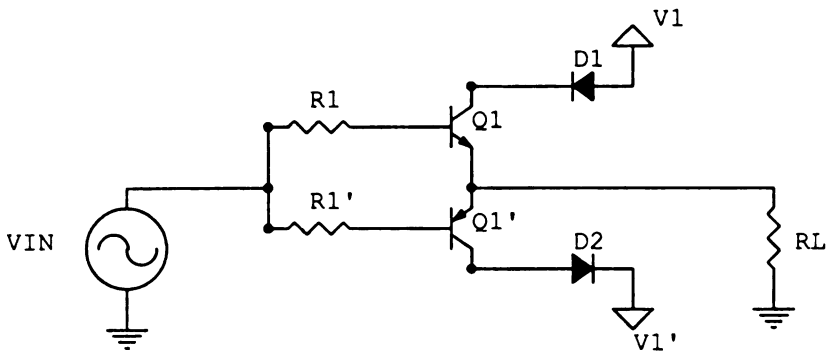


Figure 2.1.1.4: Simplified Schematic of Stage One

Figure 2.1.1.5 shows the base current of Q_1 (I_B) and the emitter current of Q_1. The emitter current was divided by 20 to fit on the graph.

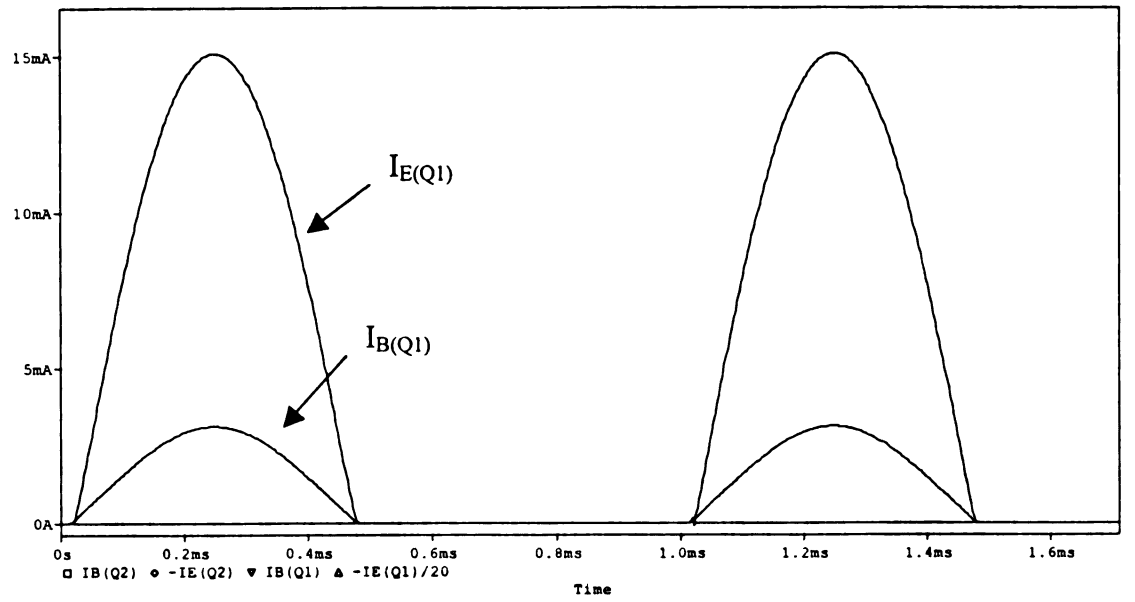


Figure 2.1.1.5: Graph of base current and emitter current of Q_1

From the graph of V_{IN} and V_{OUT} (Figure 2.1.1.3), cross over distortion is observed. This Stage One of the Class G amplifier is the same as a Class B amplifier. However, the maximum output voltage for this stage is less than the Class B amplifier because of the diode connected the V_1. The maximum efficiency of the Class G amplifier operating in Stage One will be lower than the Class B amplifier also because of the diode connected to V_1.

2.2.2 Stage Two Analysis - Large Signal Model

Stage Two happens when V_{IN} has increased above V_1-V_{D1} causing diode D_1 to open circuit and disconnect V_1 from the circuit. In Stage Two, transistor Q_2 is in the Active Region. But, depending on the value of R_1, transistor Q_1 can be either remain in the Active Region (Figure 2.2.2.1), or go into the Saturation Region (Figure 2.2.2.2).

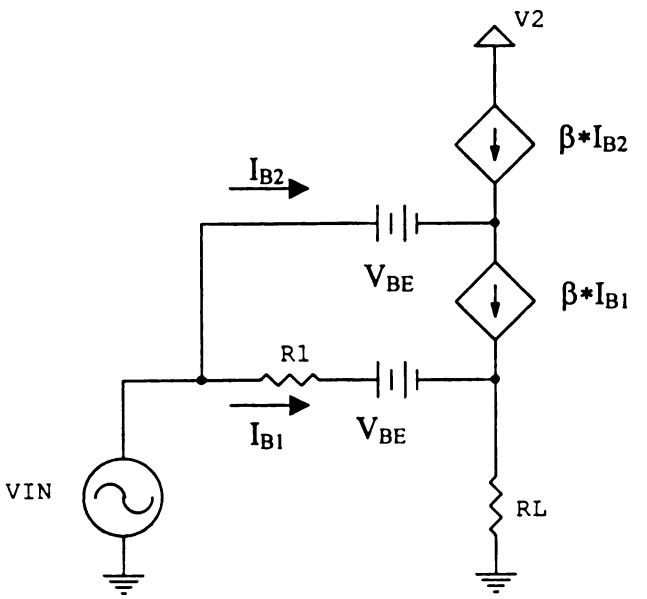


Figure 2.2.2.1: Q_1 in Active Region

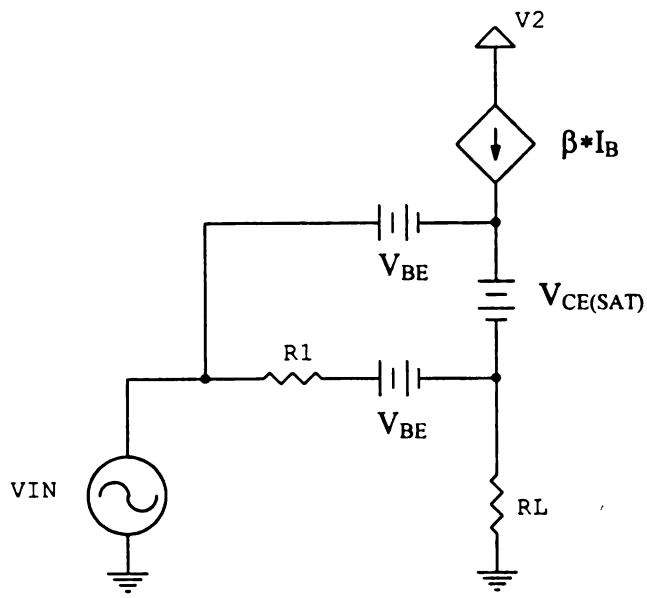


Figure 2.2.2.2: Q_1 in Saturation Region

2.2.3 Stage Two Analysis - Q1 in Saturation Region

Choosing R_1 small enough will cause transistor Q_1 to go into the Saturation Region. This implies that V_{BC} of Q_1 is greater than $V_{BC(ON)}$ of Q_1 and I_{C1} is less than $\beta * I_{B1}$.

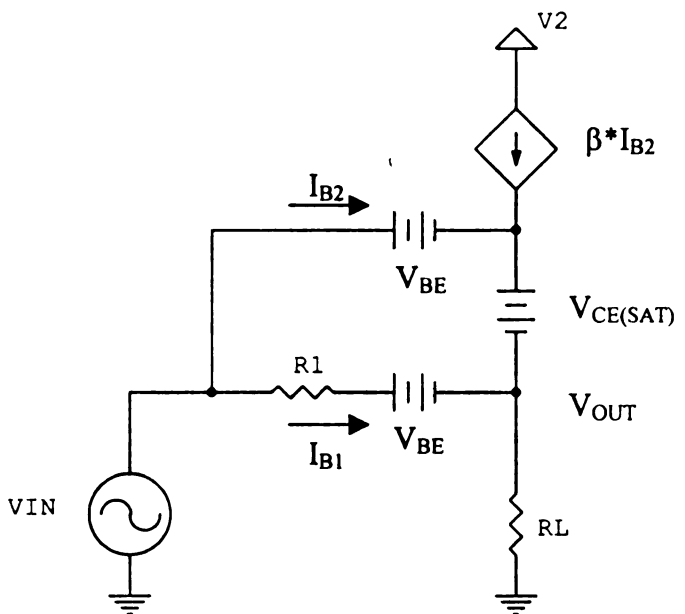


Figure 2.2.3.1: Schematic of Stage Two - Q_1 in Saturation Region

A large signal model of the Class G amplifier in stage two where transistor Q_1 is in the saturation region is shown in Figure 2.2.3.1. The equation for V_{OUT} can be found using the model as shown below. For simplification purposes, assume that $V_{BE1(ON)} = V_{BE2(ON)}$.

$$I_{B1} = \frac{(V_{BE2} + V_{CE(SAT)} - V_{BE1})}{R_1} \approx \frac{V_{CE(SAT)}}{R_1}$$

$$V_{OUT} = ((\beta + 1) * I_{B2} + I_{B1}) * R_L$$

$$= \left((\beta + 1) * I_{B2} + \frac{V_{CE(SAT)}}{R_1} \right) * R_L$$

$$V_{OUT} = V_{IN} - V_{BE1} - I_{B1} * R_1$$

$$V_{OUT} = V_{IN} - V_{BE1} - V_{CE(SAT)}$$

The equations show that the current in I_{B1} is controlled by the value of R_1. As the value of R_1 is decreased, the base current of Q_1 increases. As long as R_1's value is small enough for Q_1 to be in the Saturation Region, $V_{OUT} = V_{IN} - V_{BE1(ON)} - V_{CE(SAT)}$.

Figure 2.2.3.2 shows a PSpice simulation graph of the currents in transistor Q_1. This graph shows that the base current of Q_1 jumps up as V_{IN} increases to where Q_2 goes into the Active Region. However, the emitter current of Q_1 does not jump up indicating the Q_1 is now in the Saturation Region. (The emitter current was divided by 10 to fit on the graph.)

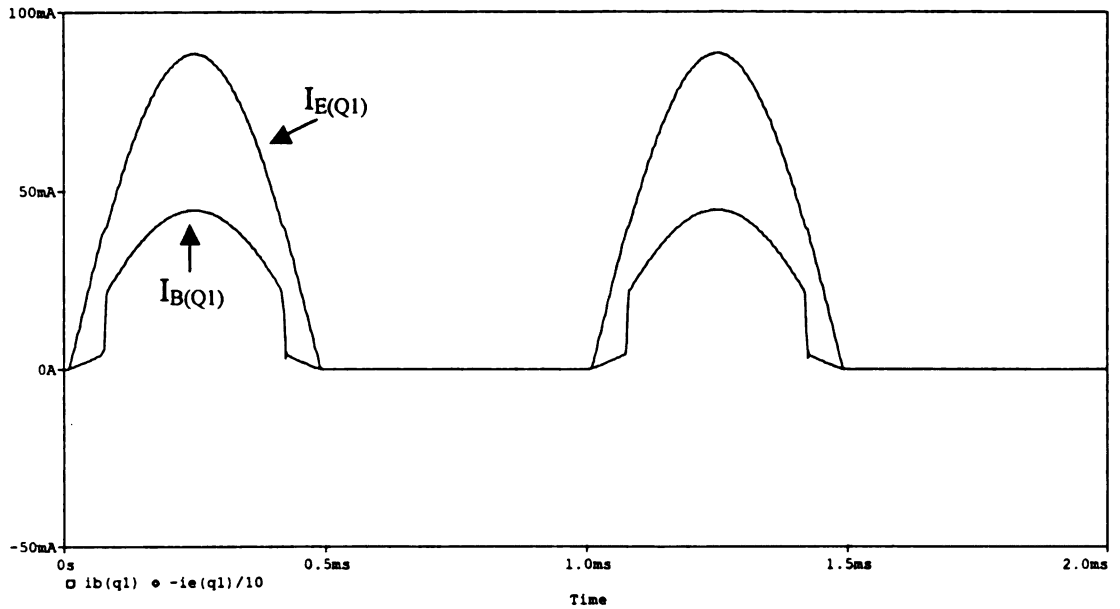


Figure 2.2.3.2: Graph of base and emitter currents of transistor Q_1

Figure 2.2.3.3 shows that the base voltage of Q_1 exceeds the collector voltage of Q_1. The characteristics for an NPN Transistor in the Saturation Region are $I_B>0$, $I_C>0$, $I_C< \beta*I_B$, and $V_{BE}>V_{BE(ON)}$. This graphs helps to verify that Q_1 is indeed in the Saturation Region.

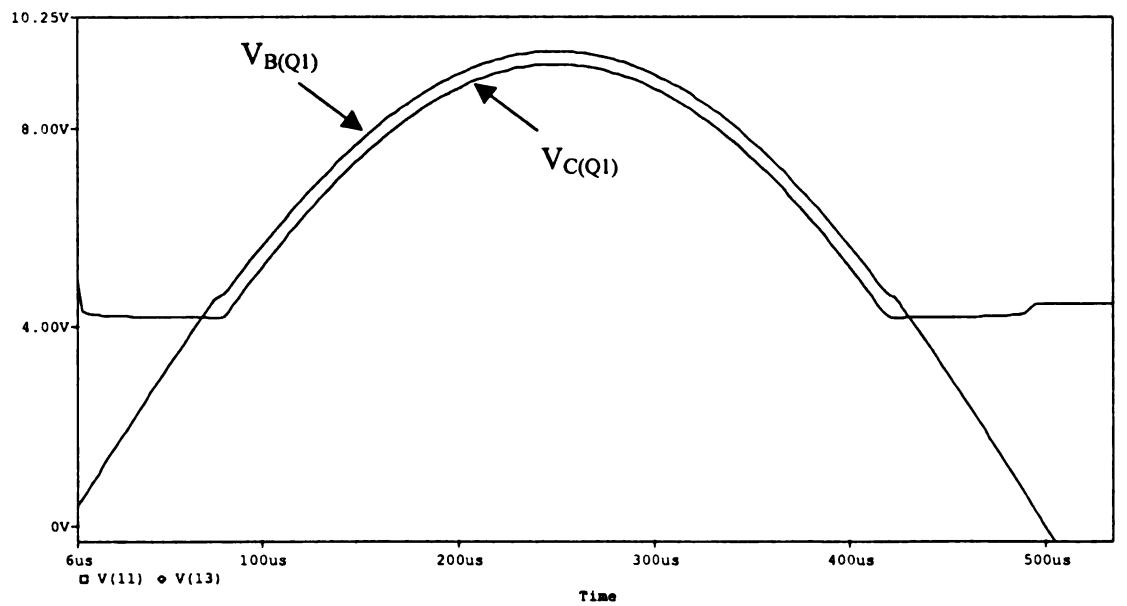


Figure 2.2.3.3: Graph of base and collector voltages of transistor Q_1

The following equations were used to find what values of R_1 will satisfy the conditions needed to have transistor Q_1 go into the Saturation Region.

$$I_{C1} < \beta * I_{B1}$$

$$(\beta+1) * I_{B2} < \beta * I_{B1}$$

$$(\beta+1) * \left(\frac{V_{OUT}}{R_L} - I_{B1} \right) * \frac{1}{(\beta+1)} < \beta * I_{B1}$$

$$V_{OUT} < (\beta+1) * I_{B1} * R_L$$

$$V_{IN} - V_{BE1} - I_{B1} * R_1 < (\beta+1) * I_{B1} * R_L$$

$$V_{IN} - V_{BE1} < I_{B1} * ((\beta+1) * R_L + R_1)$$

$$V_{IN} - V_{BE1} < \frac{V_{CE(SAT)}}{R_1} * ((\beta+1) * R_L + R_1)$$

$$\frac{V_{IN} - V_{BE}}{V_{CE(SAT)}} < (\beta+1) * \frac{R_L}{R_1} + 1$$

$$\left(\frac{V_{IN} - V_{BE1}}{V_{CE(SAT)}} - 1 \right) * R_1 < (\beta+1) * R_L$$

$$\boxed{R_1 < \frac{(\beta+1) * R_L}{\left(\frac{V_{IN} - V_{BE1}}{V_{CE(SAT)}} - 1 \right)}}$$

2.2.4 Stage Two Analysis - Q_1 Stays in Active Region

The other case that can happen is when transistor Q_1 remains in the Active Region. Figure 2.2.4.1 shows the simplified large signal model of this case give that V_{IN} is positive.

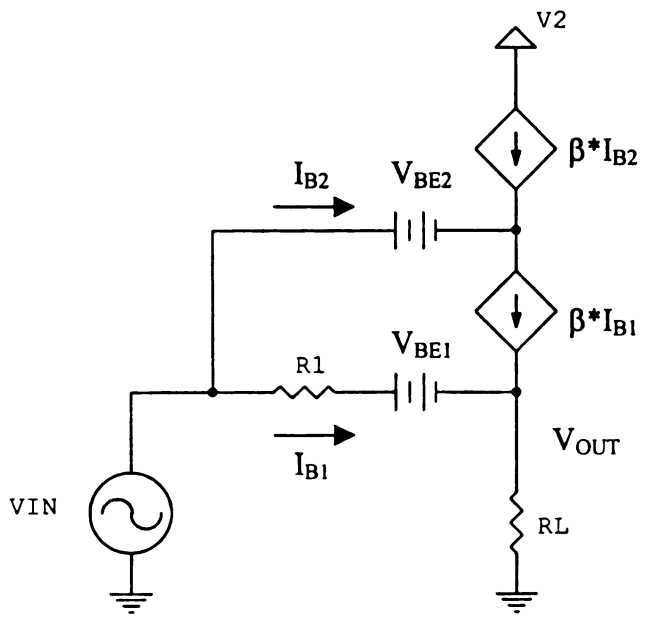


Figure 2.2.4.1: Schematic of Stage Two - Q_1 in Active Region

For both transistors Q_1 and Q_2 to be in the Active Region, the following conditions must be met.

$$I_{C1} = \beta * I_{B1}$$
$$I_{C2} = \beta * I_{B2}$$
$$I_{B1} > 0$$
$$I_{B2} > 0$$
$$V_{BE1} > V_{BE1(ON)}$$
$$V_{BE2} > V_{BE2(ON)}$$

These equations will be true when

$$R_1 > \frac{(\beta+1)*R_L}{\left(\frac{V_{IN}-V_{BE1}}{V_{CE(SAT)}}-1\right)}$$

Solving for V_{OUT} gives the following equations:

$$I_{C1} = \beta * I_{B1}$$
$$I_C1 = (\beta + 1) * I_{B2}$$
$$V_{OUT} = (I_{B1} + (\beta + 1) * I_{B2}) * R_L$$
$$= (\beta + 1) * I_{B1} * R_L$$
$$= (\beta + 1) * (V_{IN} - V_{OUT} - V_{BE1}) * \frac{R_L}{R_1}$$

$$V_{OUT} * \left(\frac{R_1}{(\beta + 1) * R_L} + 1 \right) = V_{IN} - V_{BE1}$$

$$\boxed{V_{OUT} = \frac{V_{IN} - V_{BE1}}{\left(\frac{R_1}{(\beta + 1) * R_L} + 1 \right)}}$$

This result is the same as the case for Stage One. Resistor R_1 needs to be large enough to keep Q_1 in the Active Region but at the same time, as R_1 is increased, V_{OUT} will decrease. As the maximum V_{OUT} decreases, so does the maximum efficiency (given that V_{OUT} can not exceed V_2).

2.3 Class G Amplifier Design #2 - Using Diodes

A second design is to use a diode instead of the resistor to keep Q_1 in the Active Region in Stage One and Stage Two. Figure 2.3.1 shows a simplified schematic of this design when V_{IN} is positive.

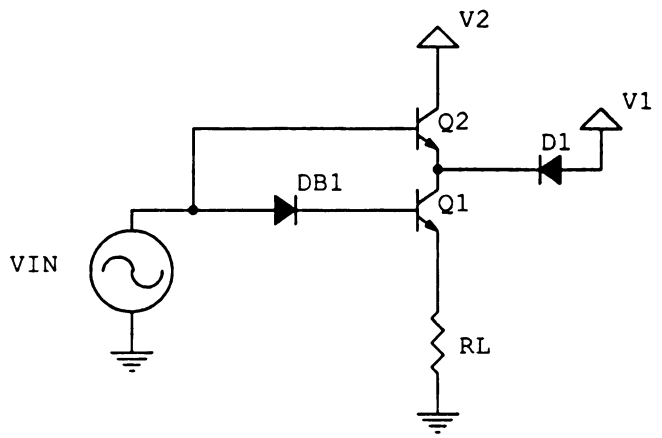


Figure 2.3.1: Schematic of design #2

2.3.1 Stage One Analysis - Large Signal Model

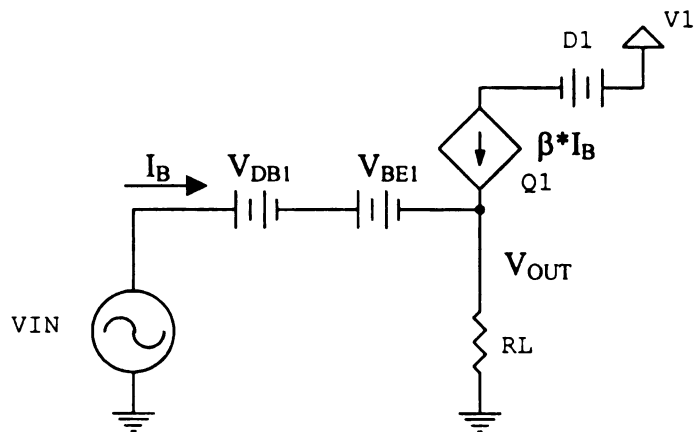


Figure 2.3.1.1: Schematic of Stage One - large signal model

Figure 2.3.1.1 shows the simplified schematic of Stage One of this design (when V_{IN} is positive). The following shows the equations for V_{OUT} and the base current of transistor Q_1.

$$V_{OUT} = V_{IN} - V_{BE} - V_{DB1}$$

$$I_B = \frac{V_{OUT}}{R_L * (\beta + 1)}$$
$$= \frac{V_{IN} - V_{BE} - V_{DB1}}{R_L * (\beta + 1)}$$

An example circuit was modeled using PSpice to examine the voltage and current levels of this design when it is in Stage One. Figure 2.3.1.2 shows the PSpice circuit file along with the schematic of the circuit simulated.

```
Class G Amplifier
V2   2 0   12
V1   3 0    4
V1P  4 0   -4
V2P  5 0  -12
VIN 10 0 DC 0V AC 1 SIN 0 3 1k
Q2   2 10 13 TIP31
Q1  13 11 15 TIP31
Q3  14 12 15 TIP32
Q4   5 10 14 TIP32
DB1 10 11 D1N4148
DB2 12 10 D1N4148
D1   3 13 D1N5817
D2  14  4 D1N5817
RL  15  0 10
.TRAN .1U 2000U 0 .1U
.MODEL DMOD D
.LIB ECE484.LIB
.LIB DIODE.LIB
.PROBE
.END
```

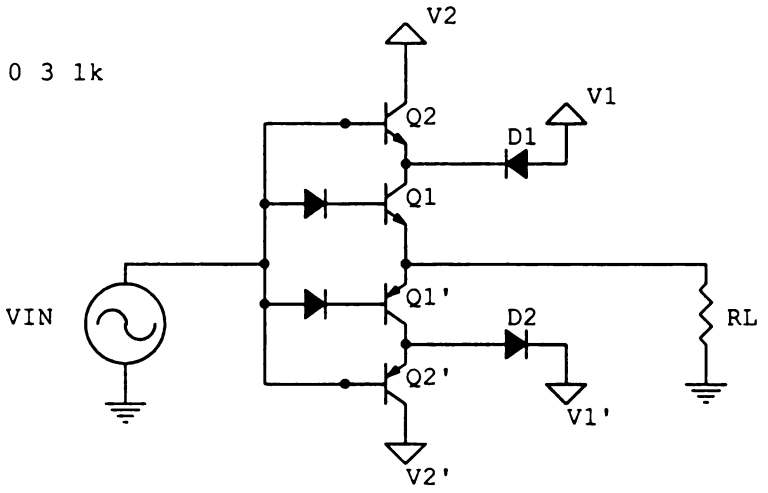


Figure 2.3.1.2: PSpice circuit file with schematic

The results for V_{IN} and V_{OUT} are shown in Figure 2.3.1.3. Notice that there is more crossover distortion than in the case where a resistor was used in instead of D_{B1} and D_{B2}.

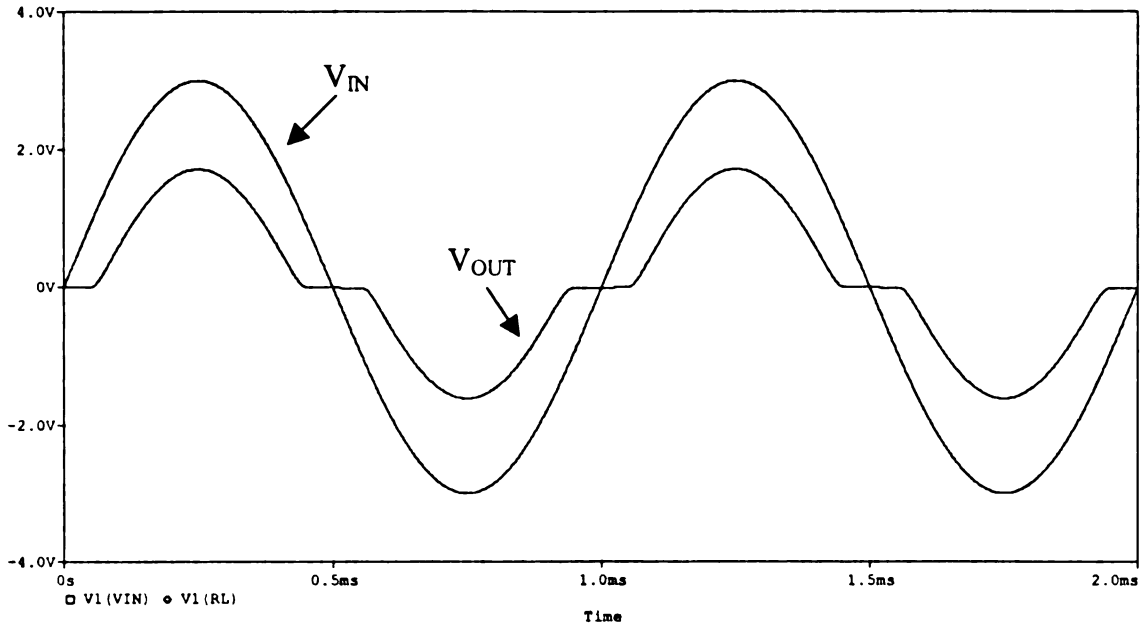


Figure 2.3.1.3: Graph of V_{IN} and V_{OUT}

Figure 2.3.1.4 shows the base and emitter current, I_B and I_E, of transistor Q_1. The emitter current was divided by 20 to fit on the graph.

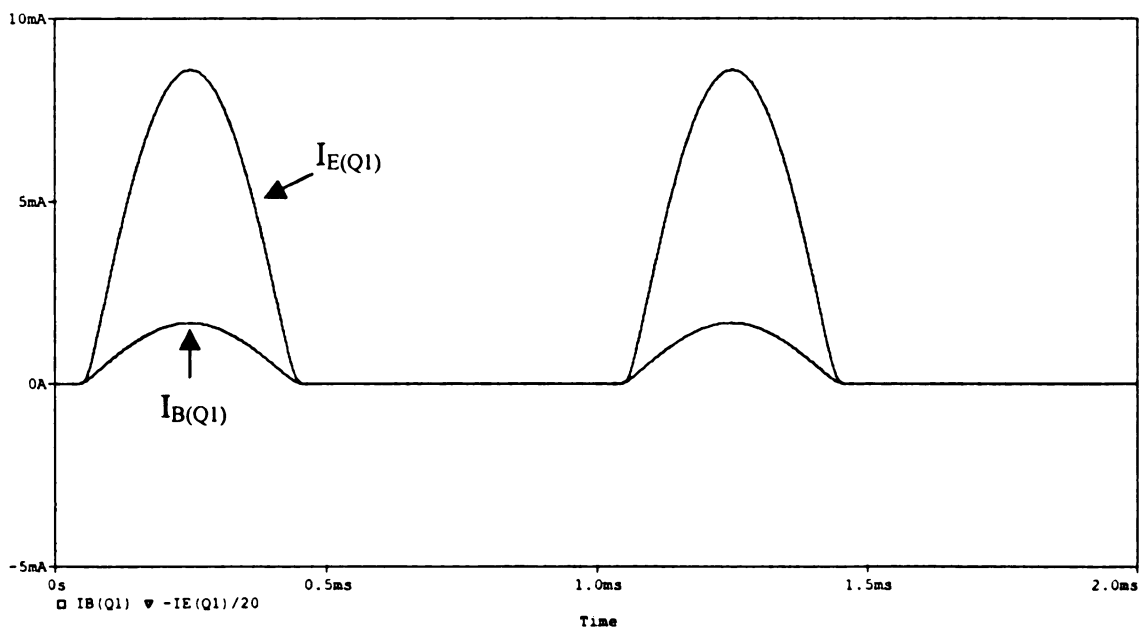


Figure 2.3.1.4: Graph of the base and emitter current of transistor Q_1

2.3.2 Stage Two Analysis - Large Signal Model

For Stage Two, transistor Q_1 will remain in the Active Region and transistor Q_2 will be in the Active Region. The large signal model of Stage Two is shown in Figure 2.3.2.1.

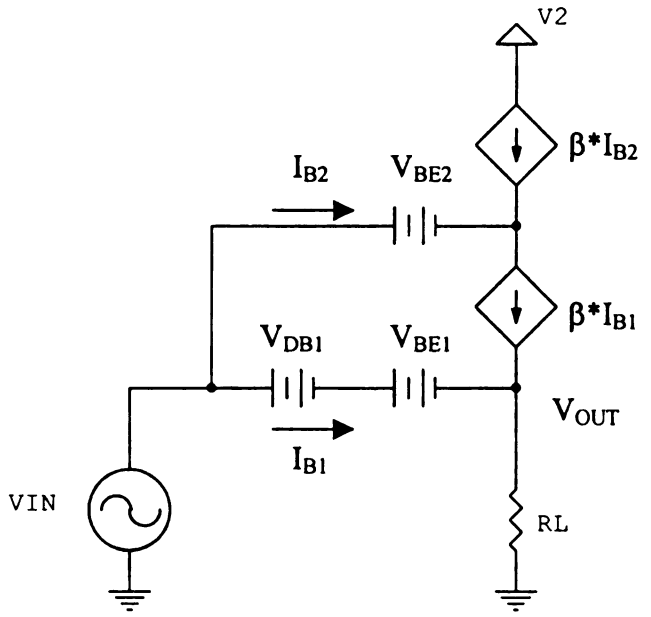


Figure 2.3.2.1: Schematic of Stage Two - large signal model

Using the model from Figure 2.3.2.1, the equation for V_{OUT}, I_{B1}, and I_{B2} can be found as follows:

$$V_{OUT} = V_{IN} - V_{BE1} - V_{DB1}$$

$$I_{B1} = \frac{V_{OUT}}{R_L * (\beta + 1)}$$

$$I_{B2} = \frac{\beta}{(\beta + 1)} * I_{B1}$$

A PSpice example of this circuit operating in Stage One and Stage Two was simulated using the same circuit as in Figure 2.3.1.3 but the input voltage was changed

from 3 volts peak-to-peak to 10 volts peak-to-peak. (VIN 10 0 DC 0V AC 1 SIN 0 10 1k) The graph of V_{IN} and V_{OUT} is shown in Figure 2.3.2.2. Notice that there does not seem to be any distortion when V_{IN} increases to where power supply V_2 in now on and V_1 is now disconnected from the circuit. Or, there doesn't seem to be distortion when V_2 is turned off and V_1 is turned back on.

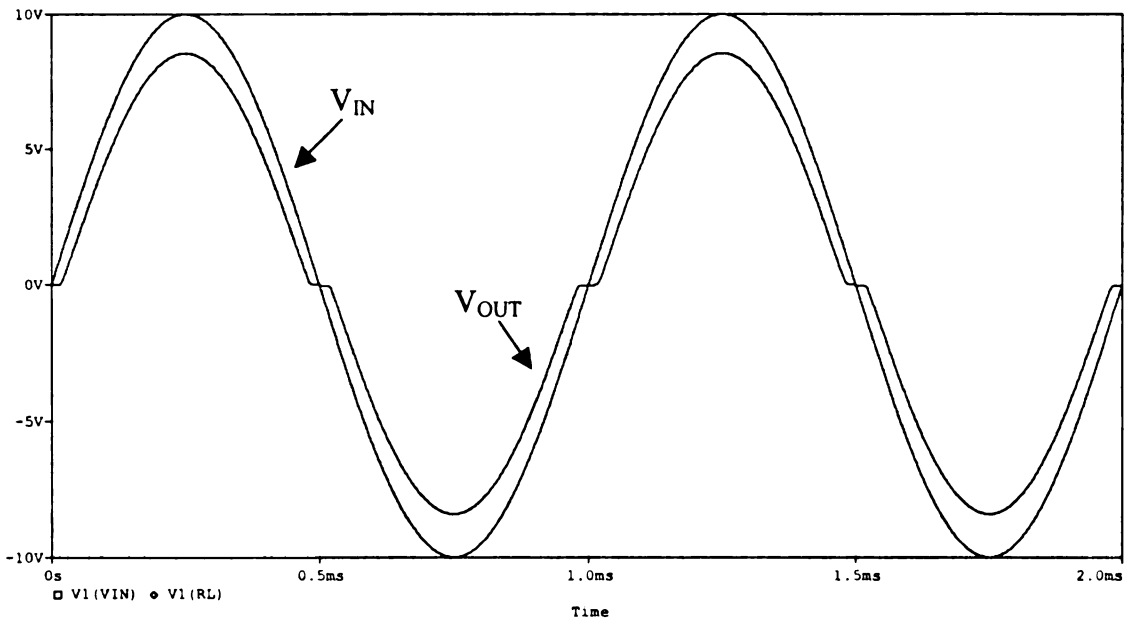


Figure 2.3.2.2: Graph of V_{IN} and V_{OUT} - Stage One and Stage Two

The base and emitter currents of transistor Q_1 and Q_2 are shown in Figure 2.3.2.3. The emitter currents were divided by 20 to fit results on the graph. When V_2 is on and V_1 is off, the emitter currents of Q_1 and Q_2 are about equal to each other. The base currents of Q_1 and Q_2 are also about equal to each other. This corresponds to the equations derived previously. The graph and equations also show that when the Class G operates in Stage Two, it takes twice as much base current for a given output current than it would in the Class B amplifier circuit.

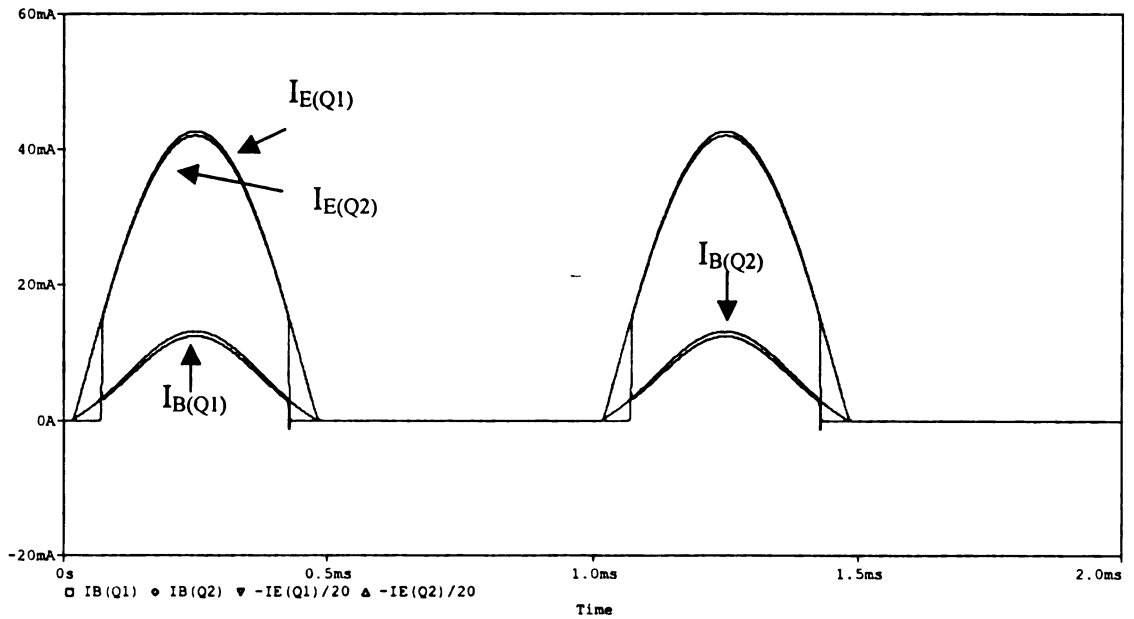


Figure 2.3.2.3: Graph of I_{B1}, I_{B2}, $I_{E1}/20$, and $I_{E2}/20$

Figure 2.3.2.4 shows the graph of V_{BC} of Q_1. This graph shows that Q_1 does not saturate when V_2 is on because $V_{BC} < V_{BC(ON)}$. In fact, V_{BC} is about 0 volts when V_2 is on.

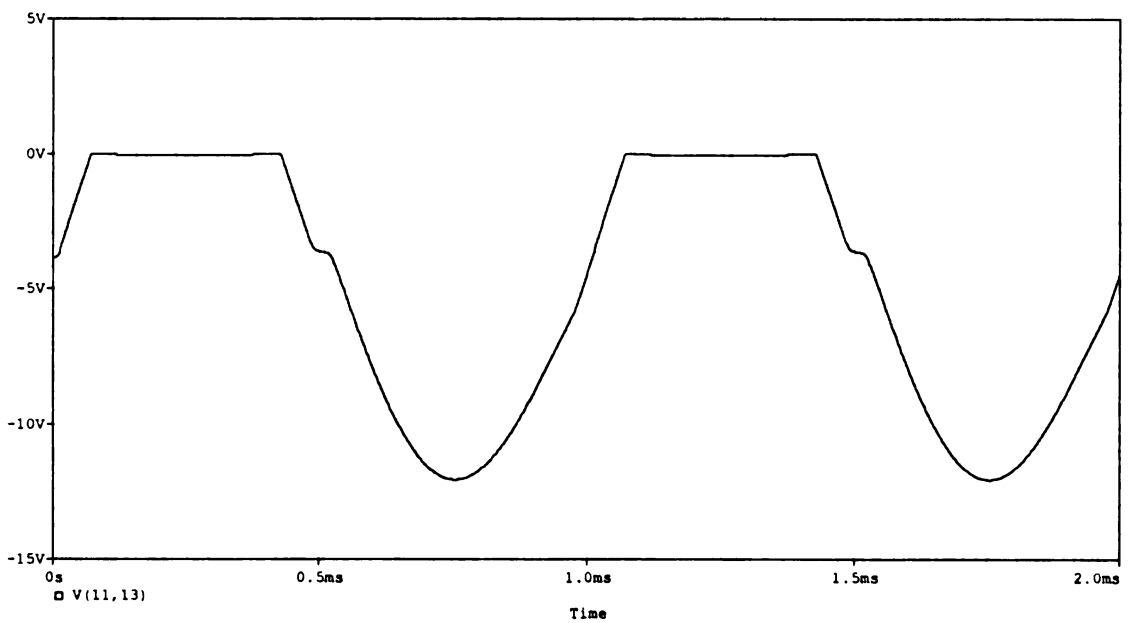


Figure 2.3.2.4: Graph of V_{BC} of transistor Q_1

When looking at the base current of transistor Q_2, one can notice that there are current spikes when V_2 turns on and also when V_2 turns off. This is shown in Figure 2.3.2.5. These current spikes may cause noise problems.

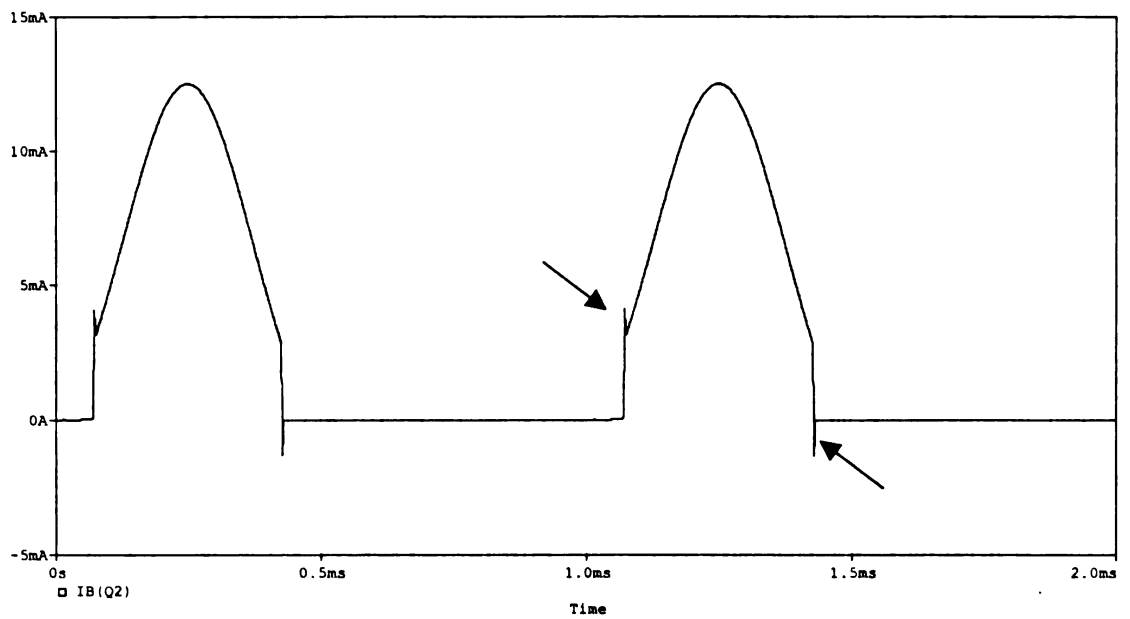


Figure 2.3.2.5: Graph of current spikes in base of transistor Q_1

2.3.3 Limitations of Design

For a typical transistor such as the TIP31A Power Transistor, the base-emitter reverse breakdown voltage is around 5 volts. To keep from destroying the transistor, V_{EB} of all the transistors must stay less than 5 volts ($V_{EB} < 5$ volts). To accomplish this, a diode is placed on the base lead of Q_2 and Q_2' to prevent reverse breakdown of the transistor [8] [10]. Another diode must be added to the base of Q_1 to keep it in the Active Region to compensate for adding the diode to the base of Q_2. The simplified schematic of this new circuit is shown in Figure 2.3.3.1 (V_{IN} is positive). A similar design can be found in reference [4].

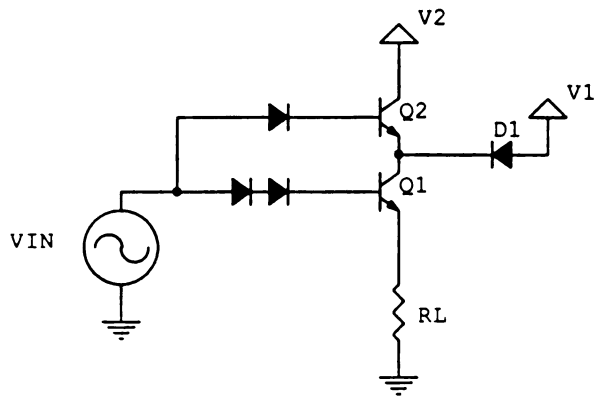
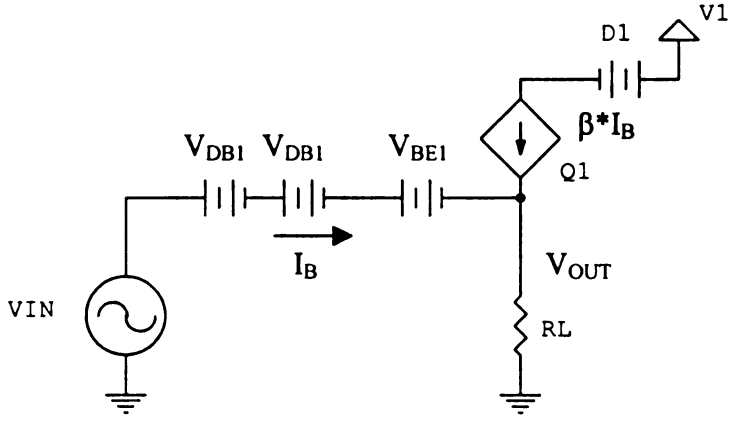


Figure 2.3.3.1: Schematic of circuit with protection diode added

2.3.3.1 Stage One Analysis

Again, the large signal model of this circuit in Stage One is created and analyzed to solve for V_{OUT} and I_B (Figure 2.3.3.1.1).



$$V_{OUT} = V_{IN} - V_{BE1} - 2 * V_{DB1}$$

$$I_B = \frac{V_{OUT}}{R_L * (\beta + 1)}$$

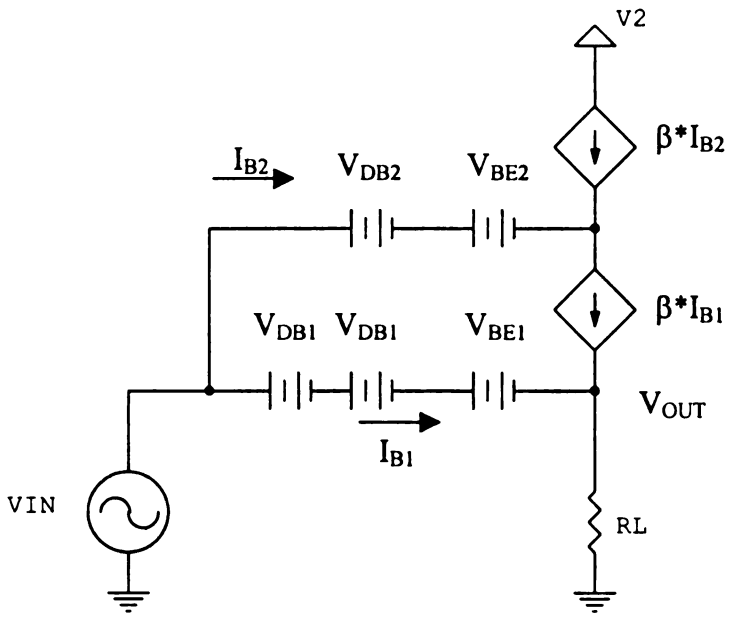
$$= \frac{V_{IN} - V_{BE1} - 2 * V_{DB1}}{R_L * (\beta + 1)}$$

Figure 2.3.3.1.1: Schematic and equations

The effect of adding the extra diode is that V_{OUT} will be smaller than V_{IN} by three diode drops instead of two. This will cause the crossover distortion to increase by another diode drop.

2.3.3.2 Stage Two Analysis

The large signal model of this new circuit with the protection diode is shown in Figure 2.3.3.2.1 along with the equations for V_{OUT}, I_{B1}, and I_{B2}. Again, V_{OUT} will be smaller than V_{IN} by three diode drops.



$$V_{OUT} = V_{IN} - V_{BE1} - 2 * V_{DB1}$$

$$I_{B1} = \frac{V_{OUT}}{R_L * (\beta + 1)}$$

$$I_{B2} = \frac{\beta}{(\beta + 1)} * I_{B1}$$

Figure 2.3.3.2.1: Schematic and equations

2.4 Keeping Transistors from Saturating

It is a good idea to keep the transistors in this circuit from saturating [4], because the maximum current in the collector of the transistor is $\beta * I_{B2}$ when the transistor Q_1 is in the Saturation Region and more current will go through the base of Q_1. More power will be lost because of the diodes connected to the base thus making the circuit less efficient for analog amplification. Another point to keeping the transistors from saturating is that the switching speeds of the transistors are slower if the transistor is coming out of the Saturation Region and into the Active Region.

Chapter 3: Using an Operational Amplifier with Feedback

3.1 Introduction

In order to get rid of the crossover distortion and distortions due to the β of the transistor changing with current, an operational amplifier (Op-Amp) with feedback may be used to bias this circuit (Figure 3.1.1). An LF411 Op-Amp will be used. However, the output current of the LF411 is limited to 25mA. This will limit the maximum output voltage. To analyze the effects of the Op-Amp on this circuit, V_{IN} will be kept small enough to keep the Op-Amp from current limiting.

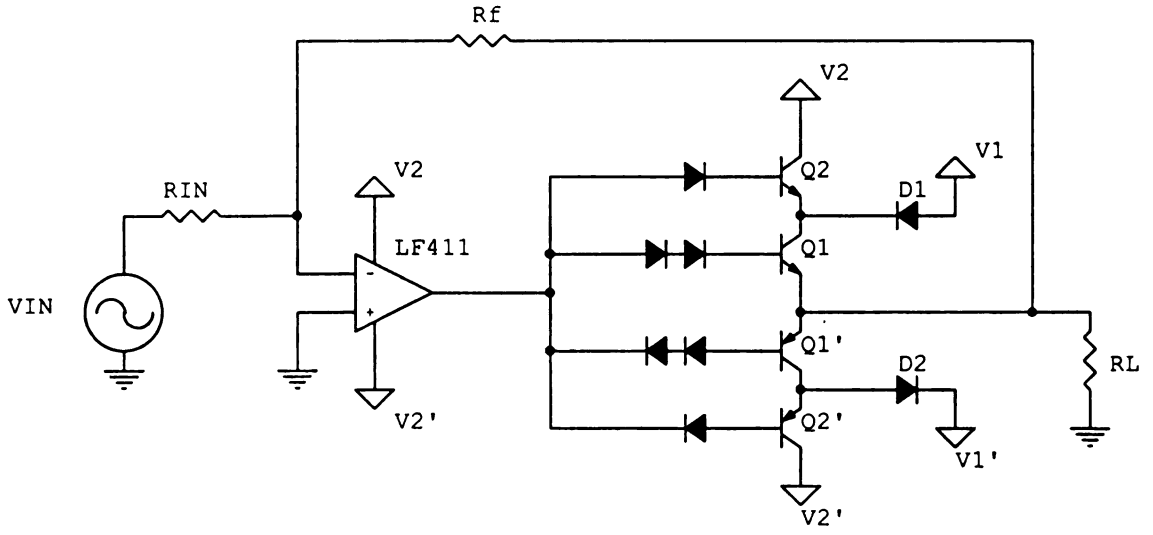


Figure 3.1.1: Schematic using Op-Amp with feedback in design

3.2 PSpice Simulations of Stage One

This circuit was simulated using PSpice. The input voltage (V_{IN}) is small enough to keep transistors Q_2 and Q_2' in cut off so that only the smaller power supplies are active (V_1 and V_1') which is denoted as Stage One. Figure 3.2.1 shows the graph of V_{IN} and the

output voltage of the Op-Amp. The output voltage of the Op-Amp jumps to compensate and eliminate the crossover distortion. Figure 3.2.2 shows the current coming in and out of the Op-Amp which would also be the base currents of transistors Q_1 and Q_1'. There is a current spike as transistor Q_1 and Q_1' goes from the Cut-Off Region to the Active Region. Figure 3.2.3 shows the collector voltage of transistor Q_1. The graph shows that when the power supply V_1 is on (current flowing) the collector voltage drops due to the diode D_1. The voltage across the load resistor, V_{OUT}, is shown in Figure 3.2.4. The crossover distortion has been greatly reduced by the addition of the Op-Amp. However, by closer inspection, there can be seen some ringing in the output as V_{OUT} crosses zero volts which is a sign of marginal stability problems (see Figure 3.2.5).

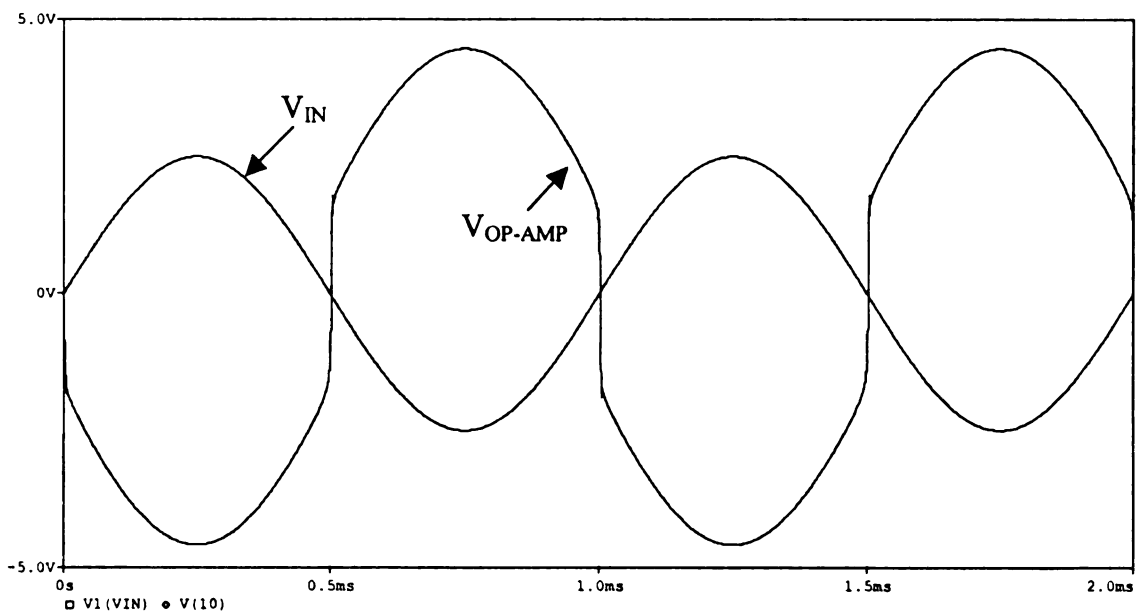


Figure 3.2.1: Graph of V_{IN} and output voltage of Op-Amp

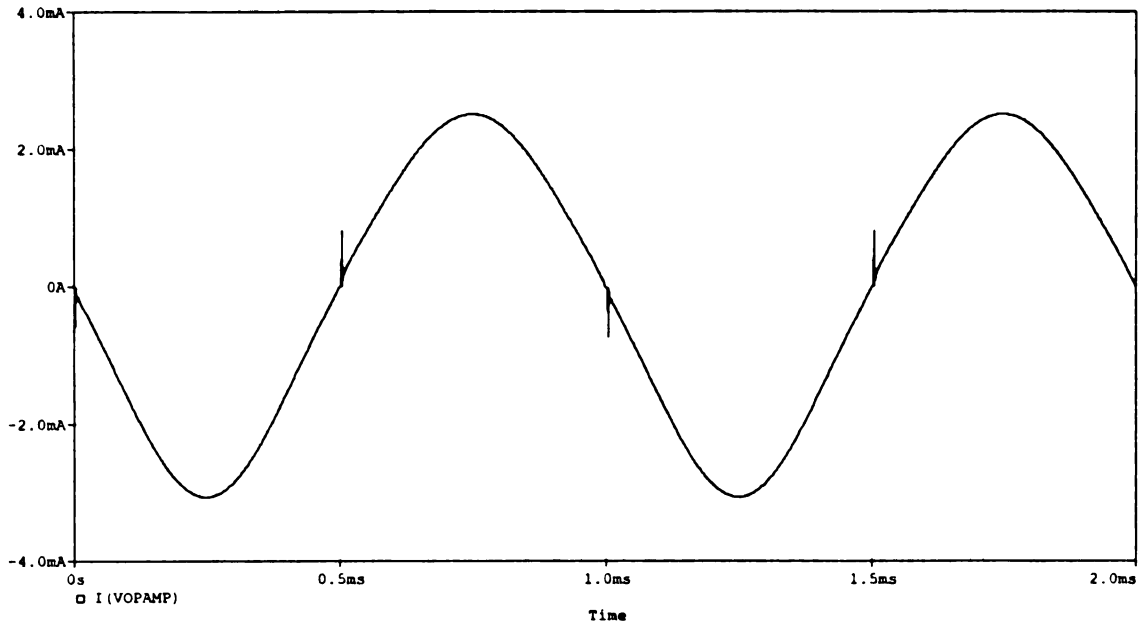


Figure 3.2.2: Graph of current flowing from the Op-Amp

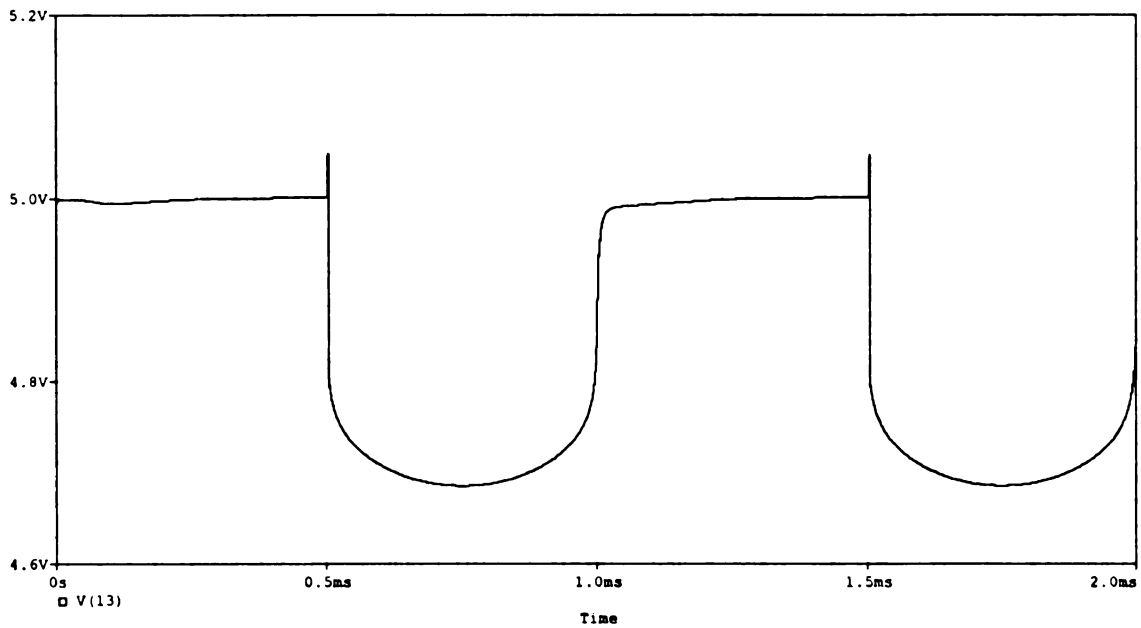


Figure 3.2.3: Graph of the collector voltage of Q_1

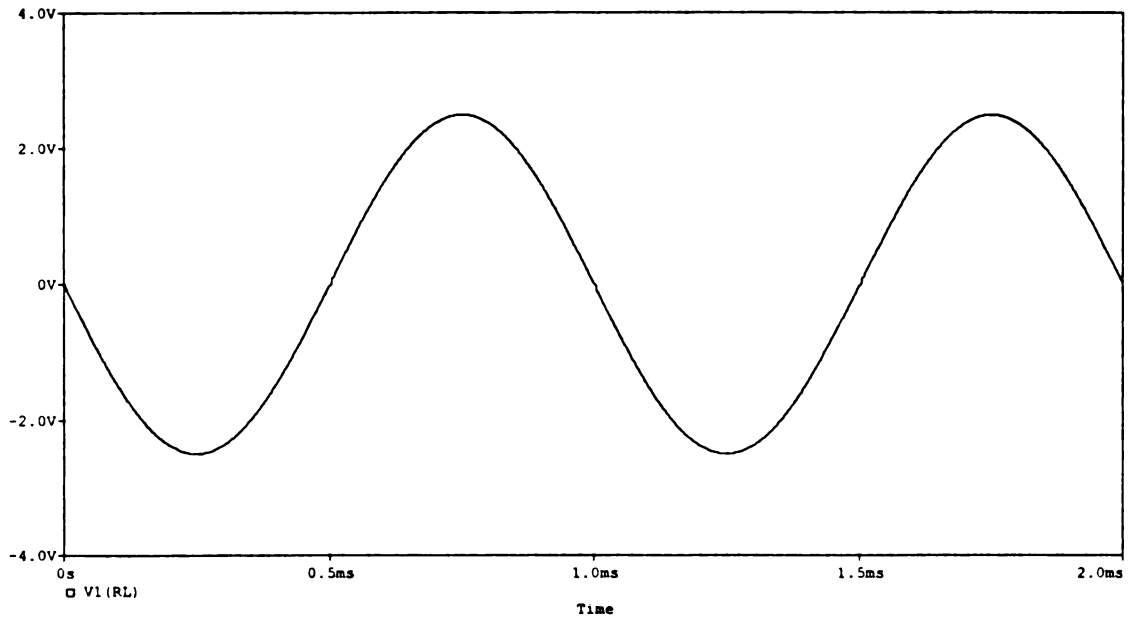


Figure 3.2.4: Graph of V_{OUT} across the load

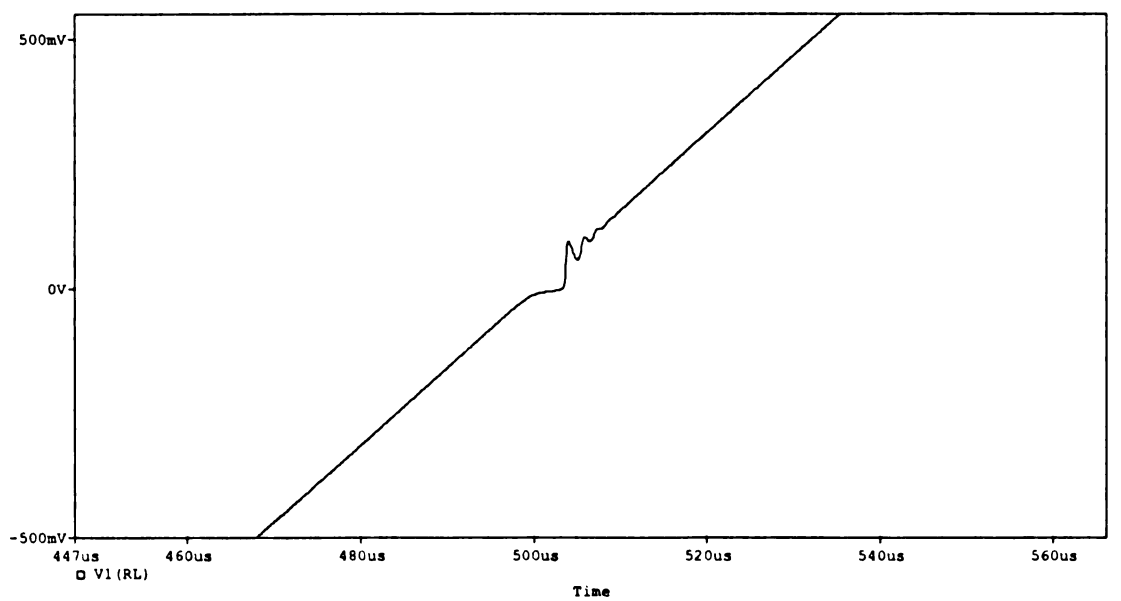


Figure 3.2.5: Graph of V_{OUT} - closer view

3.3 PSpice Simulations of Stage One and Stage Two

The input voltage (V_{IN}) here is large enough to need the use of the larger power supplies (V_2 and V_2') but small enough to keep the Op-Amp from current limiting.

Figure 3.3.1 shows the graph of V_{IN} and the output voltage of the Op-Amp. The output voltage of the Op-Amp jumps twice to compensate and eliminate the crossover distortion and the switching of the power supplies. Figure 3.3.2 shows the current coming in and out of the Op-Amp. Figure 3.3.3 shows the base currents of transistors Q_1 and Q_2. The base current of Q_2 must quickly jump up to match the current that is going into the base of transistor Q_1 when power supply V_2 turns on. Figure 3.3.4 shows the collector voltage of transistor Q_1. The graph shows that when the power supply V_1 is on (current flowing) the collector voltage drops due to the diode D_1. Then the collector voltage rises as power supply V_1 is turned off and the current increases coming from power supply V_2. Figure 3.3.5 shows the current coming from the power supplies V_1 and V_2. Notice how quickly the current changes during the switching of the power supplies. The voltage across the load resistor, V_{OUT}, is shown in Figure 3.3.6. There is no visible distortion in the output due to the switching of the power supplies because of the addition of the Op-Amp at this frequency.

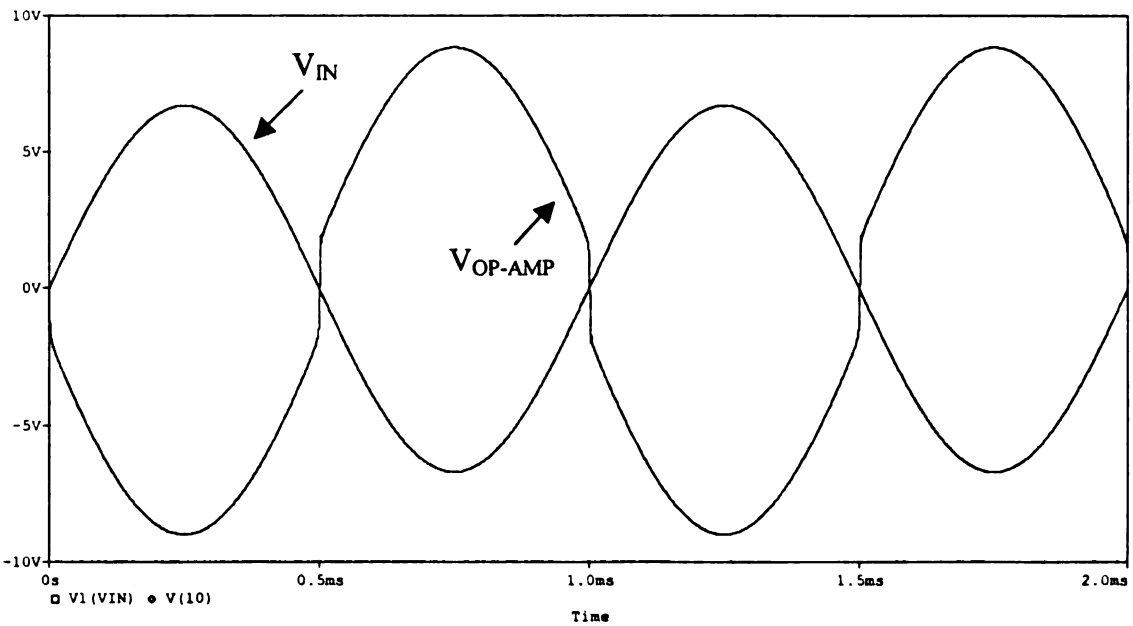


Figure 3.3.1: Graph of V_{IN} and output voltage of Op-Amp

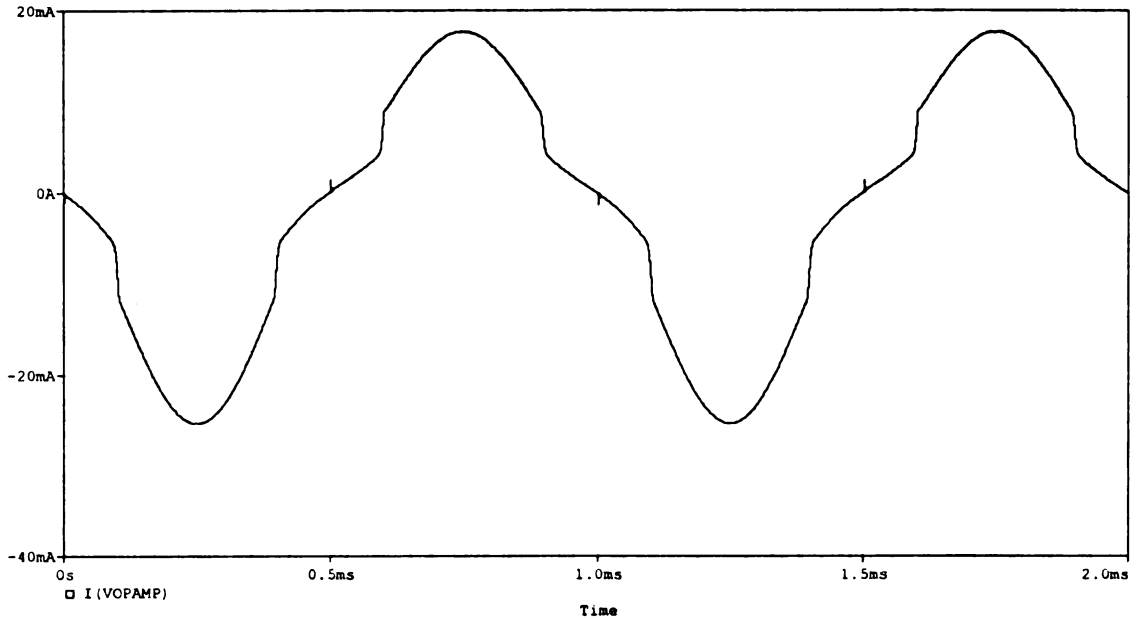


Figure 3.3.2: Graph of current from Op-Amp

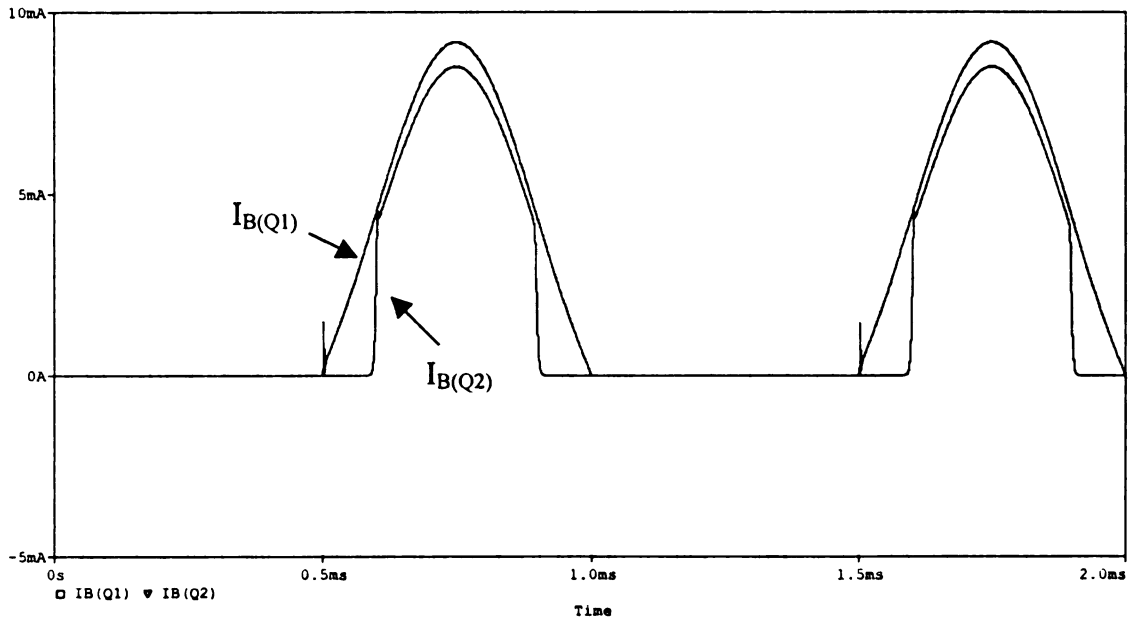


Figure 3.3.3: Graph of the base currents of transistors Q_1 and Q_2

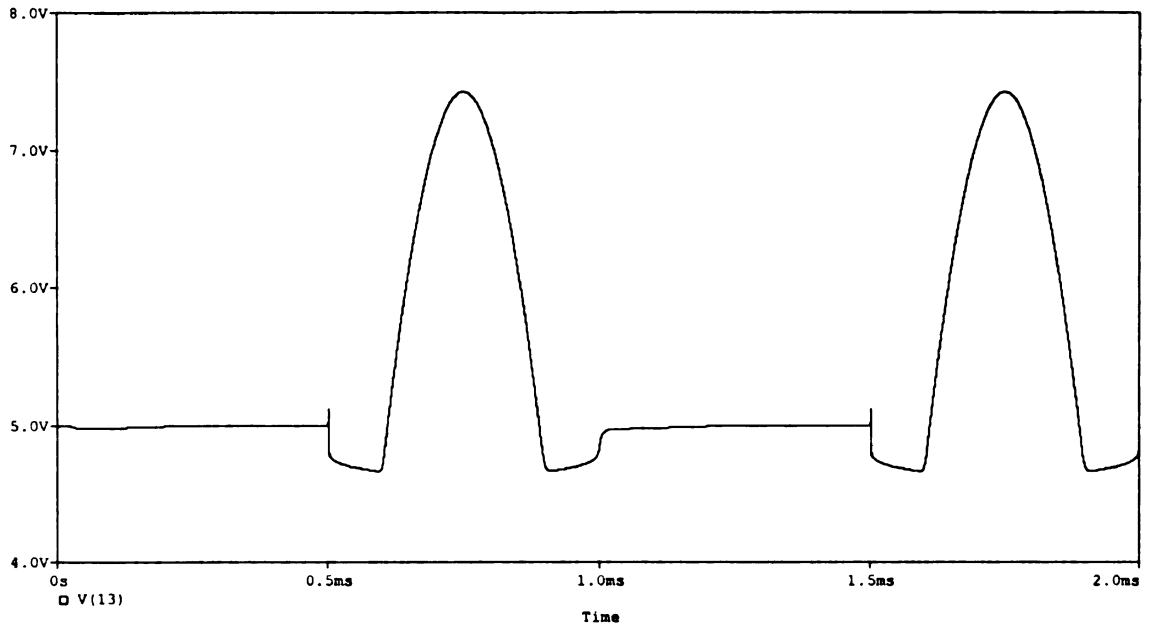


Figure 3.3.4: Graph of the collector voltage of transistor Q_1

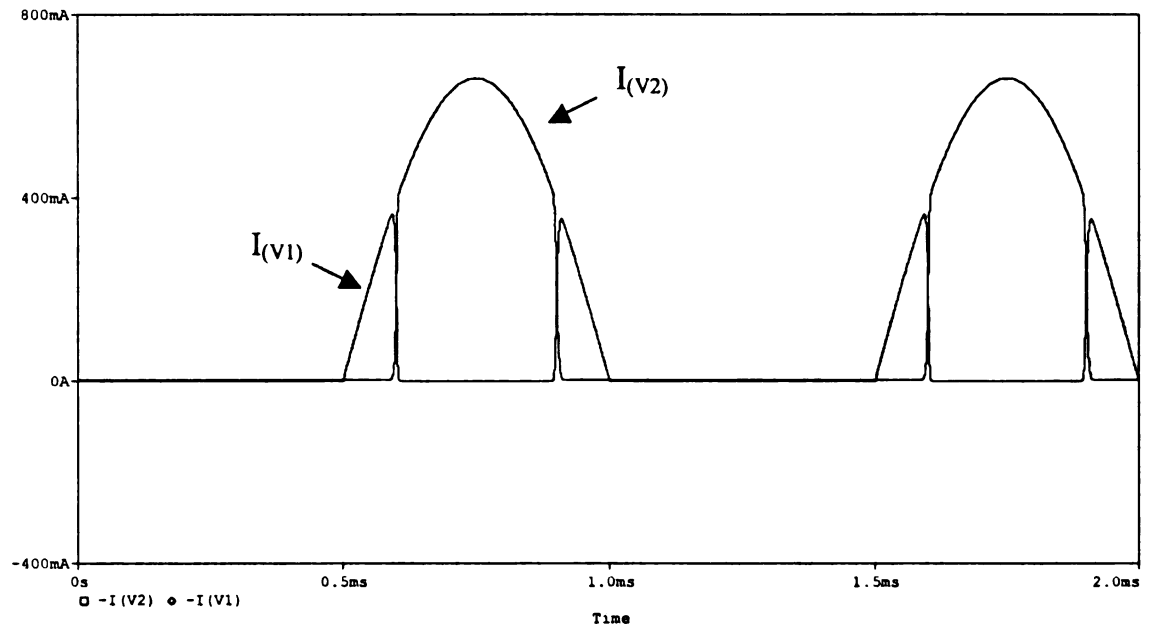


Figure 3.3.5: Graph of the current from power supplies V_1 and V_2

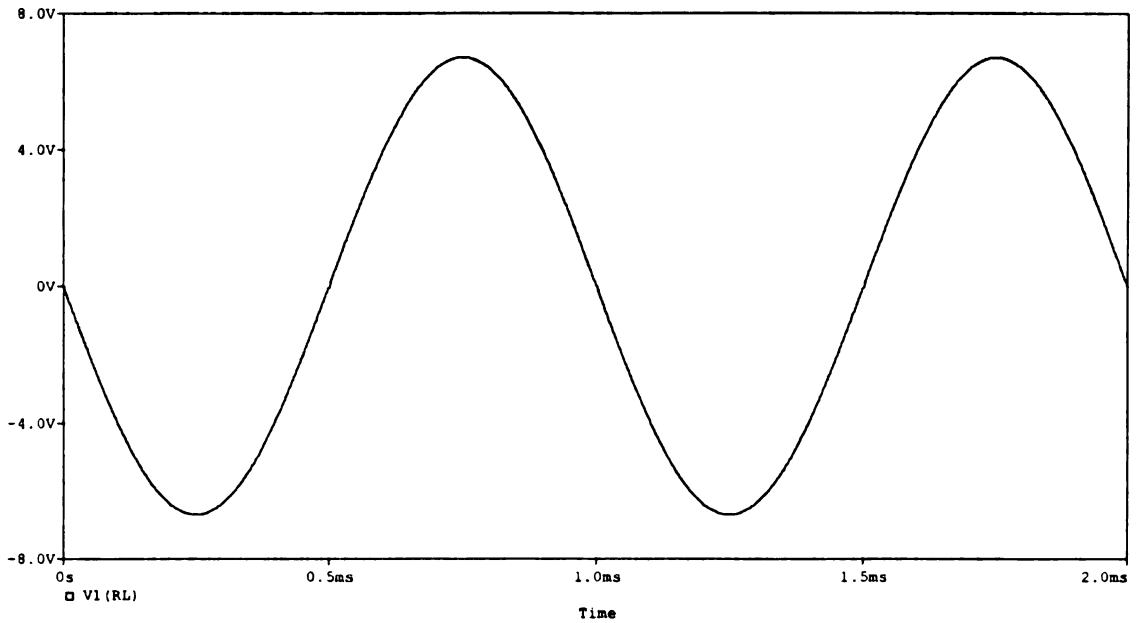


Figure 3.3.6: Graph of V_{OUT} across the load

3.4 Adding a Class B Stage

Adding the Op-Amp improves the performance of the Class G amplifier, but the maximum voltage swing of the circuit is limited by the current from the Op-Amp. An Op-Amp can be powered with +/- 18 volts. In order to get the most voltage swing out of the Op-Amp without current limiting, another Class B stage was added to the output of the Op-Amp. The Class B stage will cause all the base currents for transistors Q_1, Q_1', Q_2, and Q_2' to come from the larger power supplies (V_2 and V_2') instead of from the Op-Amp. Figure 3.4.1 shows the new circuit schematic.

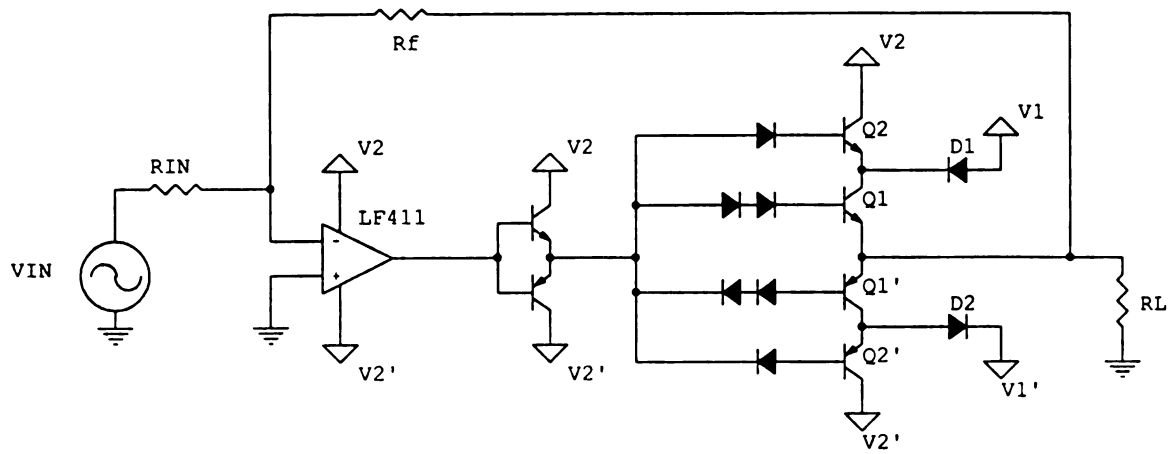


Figure 3.4.1: Schematic of Class G with an additional Class B stage

Figure 3.4.2 shows a PSpice graph of V_{OUT} across the load resistor. With V_2 equal to +18 volts and V_1 equal to 6 volts, the maximum output voltage is 13.7 volts because of the diode drops, the output voltage limit of the Op-Amp, and the β of the transistors changing as the current increases.

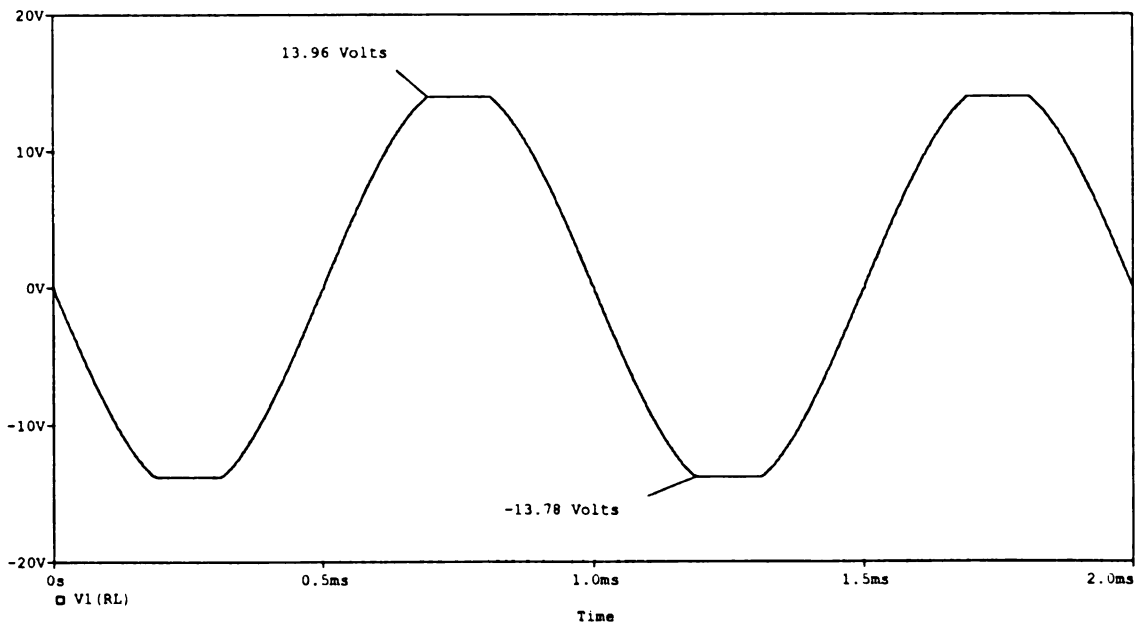


Figure 3.4.2: Graph of maximum V_{OUT}

Now by setting VIN to equal 13.7 volts peak, the output voltage of the Op-Amp can be seen without clipping in Figure 3.4.3. The output voltage is the maximum voltage swing for this Op-Amp, therefore it is not current limiting. Figure 3.4.4 shows V_{OUT} across the load resistor without any visible distortion.

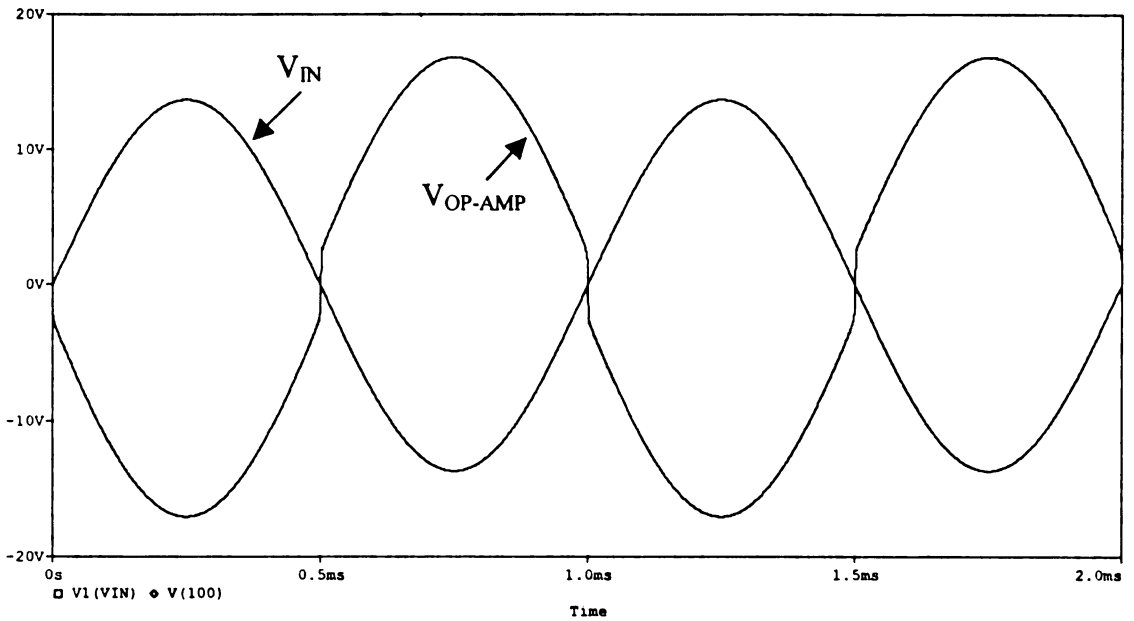


Figure 3.4.3: Graph of V_{IN} and the output voltage of the Op-Amp

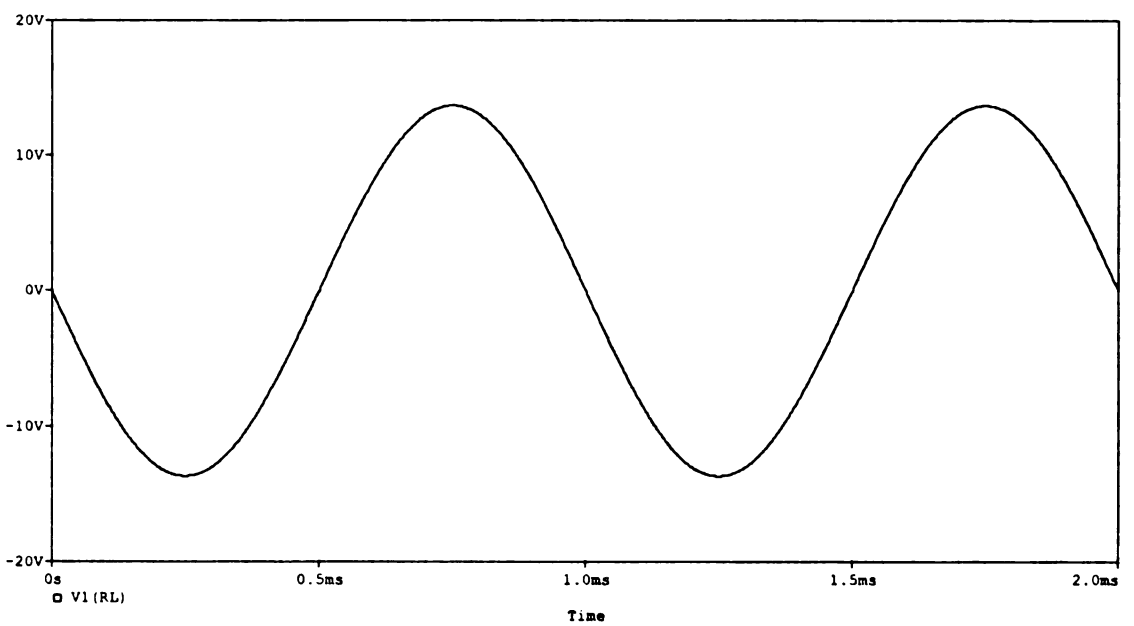


Figure 3.4.4: Graph of V_{OUT}

Chapter 4: Possible Issues

4.1 Introduction

There are some design considerations with the Class G amplifier. The effects of switching between power supplies are looked at more closely. The power supplies that are used will have an impact on the performance of the circuit. Also, the diodes that are part of the lower power supplies have an impact on the performance of the circuit because of the switching.

4.2 Using Schottky Diodes

The Class G amplifier uses diodes to keep current coming from the larger power supplies from going into the smaller power supplies. For this circuit, a small signal PN junction diode is not sufficient because it cannot handle the high amount of current needed to pass through the diode (about 1 Amp for this test circuit). When a PN junction 1N4001 rectifier diode was used for D_1 and D_2, which can handle the large current, large distortions appeared in the output current of the power supplies in the PSpice simulations (Figure 4.2.1). Figure 4.2.1 shows this spike in current only happening when the amplifier switches from the smaller power supply to the larger power supply. This distortion is due to the fact that a PN junction diode can store charge.

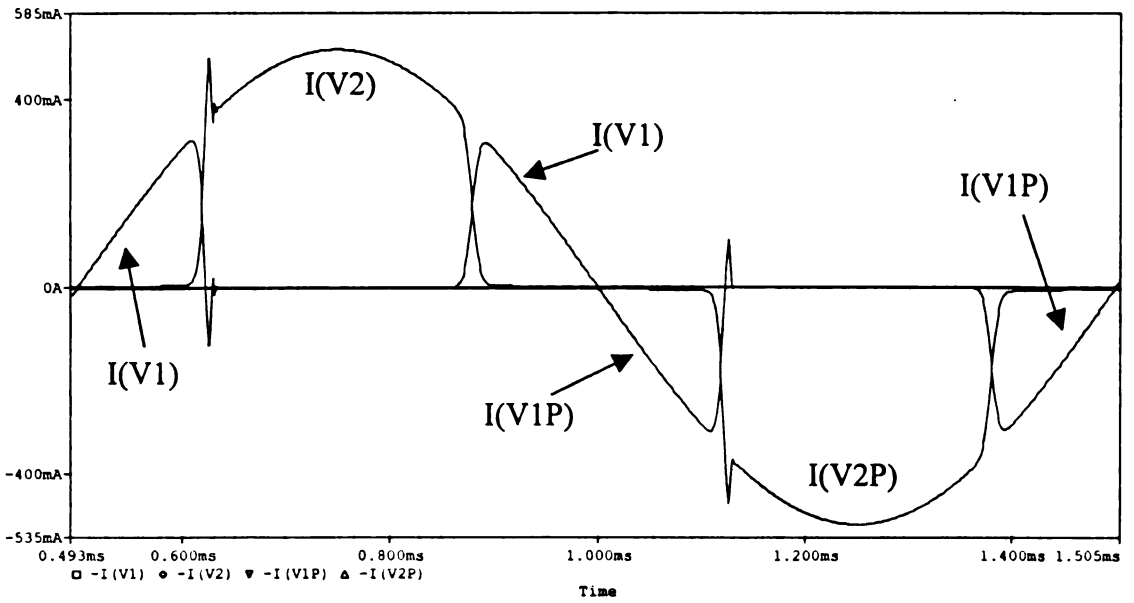


Figure 4.2.1: Graph of current from all power supplies

This spiking in the current coming from the power supplies will cause problems when there is some high frequency noise in the circuit. Figure 4.2.2 is the circuit which has a 1 kHz sine wave source plus a 500 kHz sine wave source used to simulate noise. Figure 4.2.3 shows the graph of the output voltage with major distortions happening in the areas where switching between the power supplies occur.

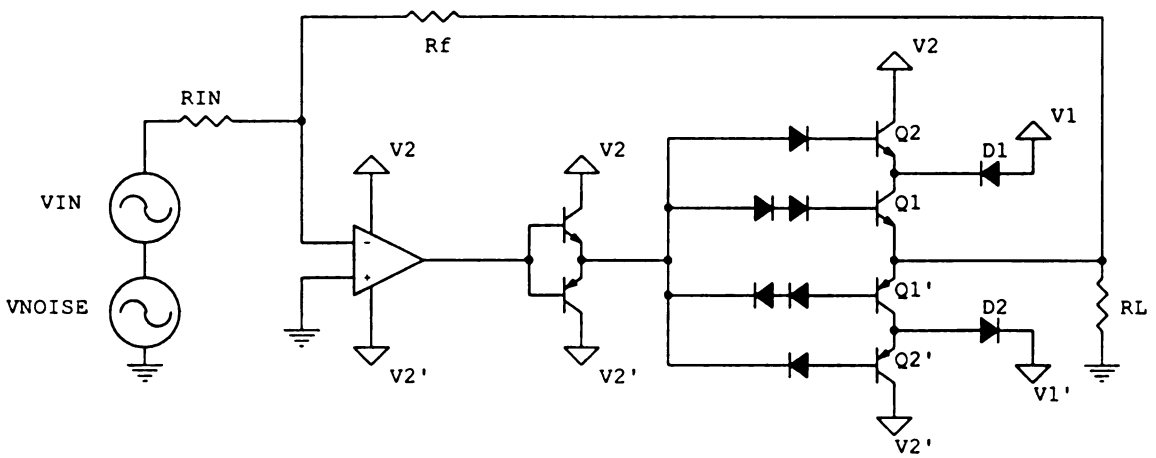


Figure 4.2.2: Schematic of amplifier with noise and PN junction diodes

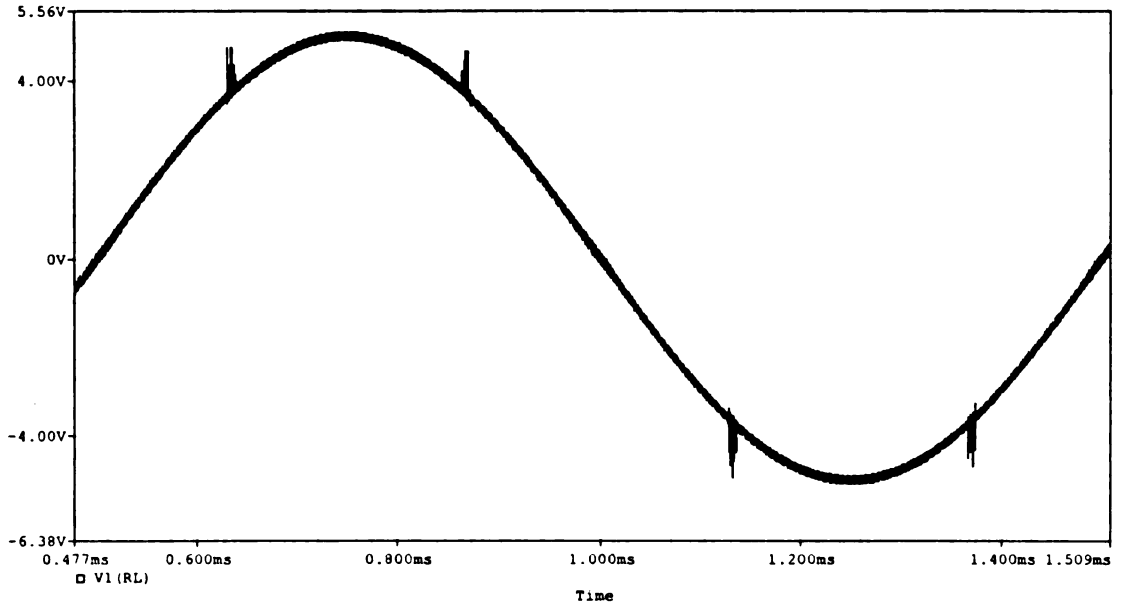


Figure 4.2.3: Graph of noise in V_{OUT} due to PN junction diodes

A way to eliminate this problem of noise in the output voltage is by using Schottky diodes for D_1 and D_2 [10]. Schottky diodes do not have a PN junction but instead have a metal to semiconductor junction. They will not store as much charge as the PN junction diodes do [1]. Figure 4.2.4 shows the graph of the current coming from the power supplies but this time, there is not the spike in current when the circuit switches from the lower power supply to the larger power supply.

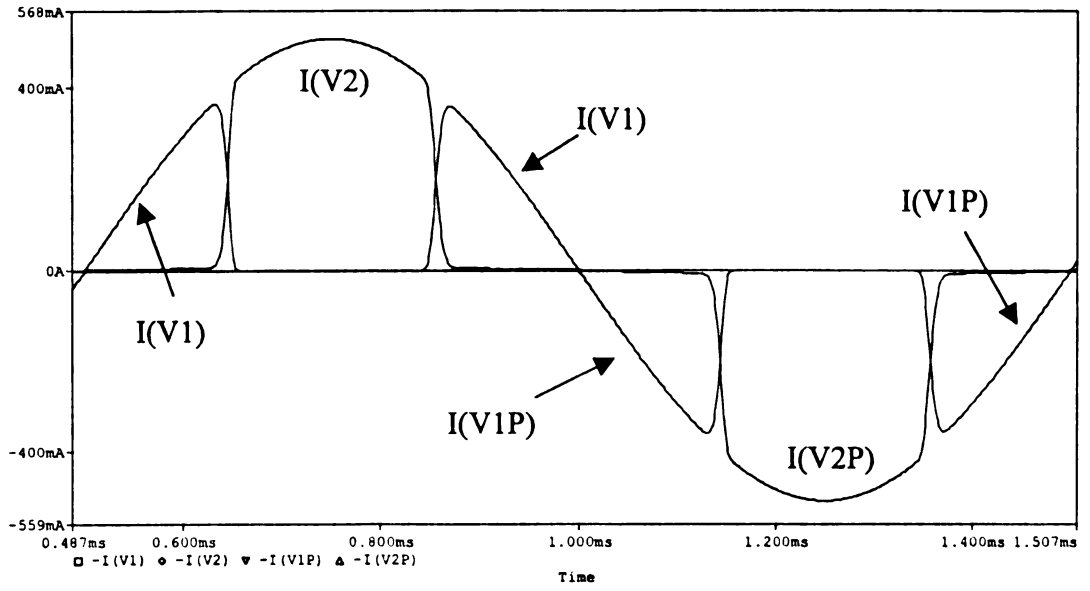


Figure 4.2.4: Graph of current from power supplies using Schottky diodes

Again, the circuit was tested by adding a 500 kHz signal to the 1 kHz V_{IN} signal to simulate noise. Refer to Figure 4.2.2 for the schematic. Figure 4.2.5 shows the output voltage of this circuit. By replacing the PN junction diodes D_1 and D_2 with Schottky diodes, the noise problem in the output is eliminated.

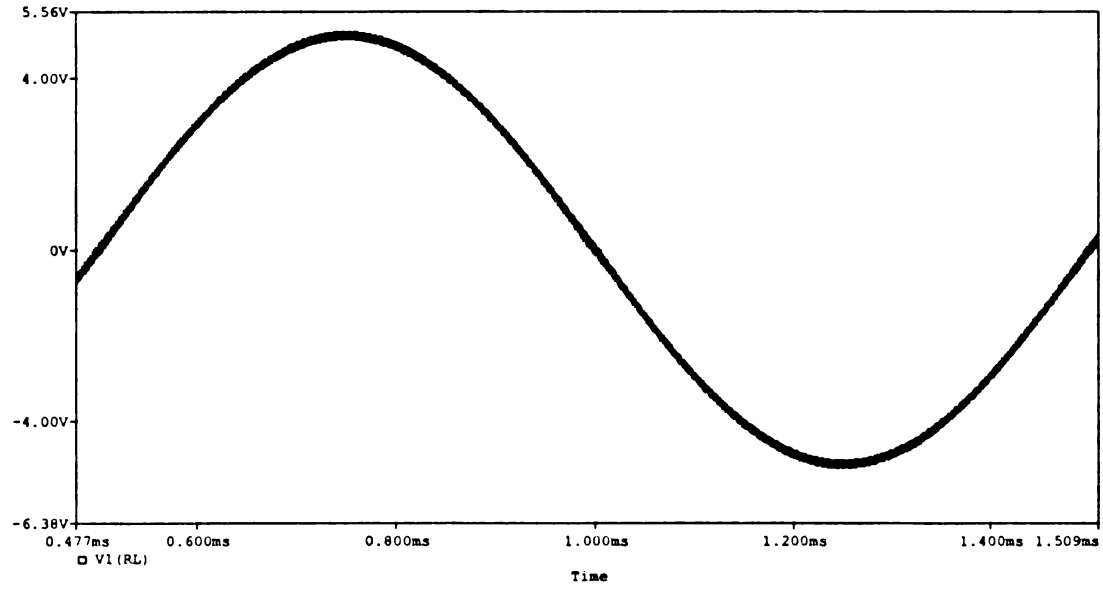


Figure 4.2.5: Graph of V_{OUT} using Schottky diodes

4.3 Power Supply Issues

The transient response of the power supplies will be an important factor for the stability of the Class G amplifier. This is because when V_1 is turned off and V_2 is turned on, the current of V_2 must instantly match the current that was coming from V_1. The currents coming from the power supply using a 10kHz sine wave is shown in Figure 4.3.1. This graph indicates how fast the power supply V_2 must be able to switch.

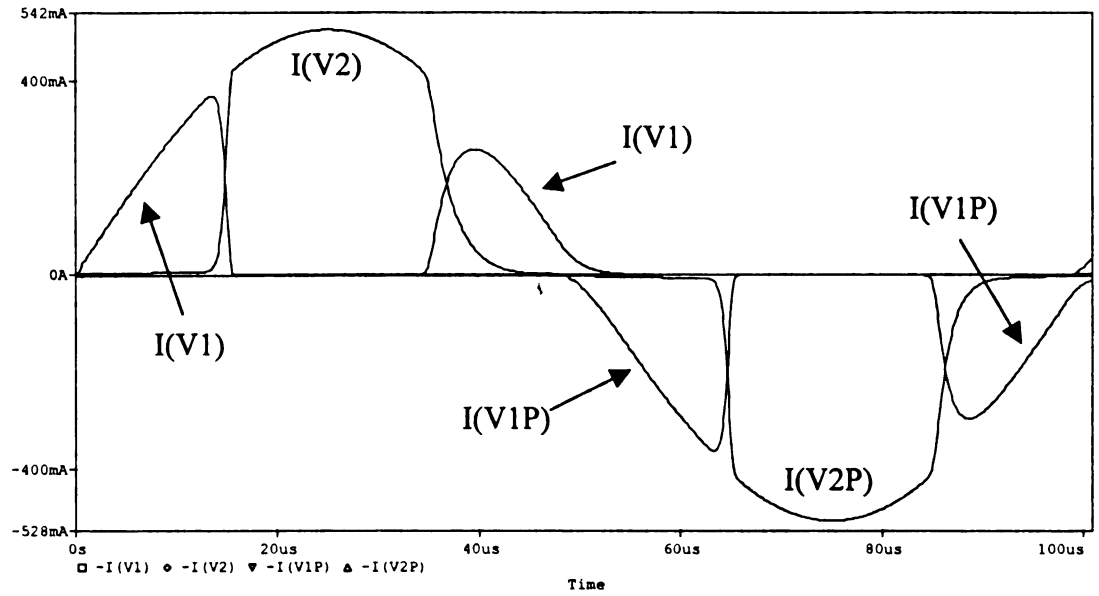


Figure 4.3.1: Graph of currents from the power supplies using a 10kHz signal

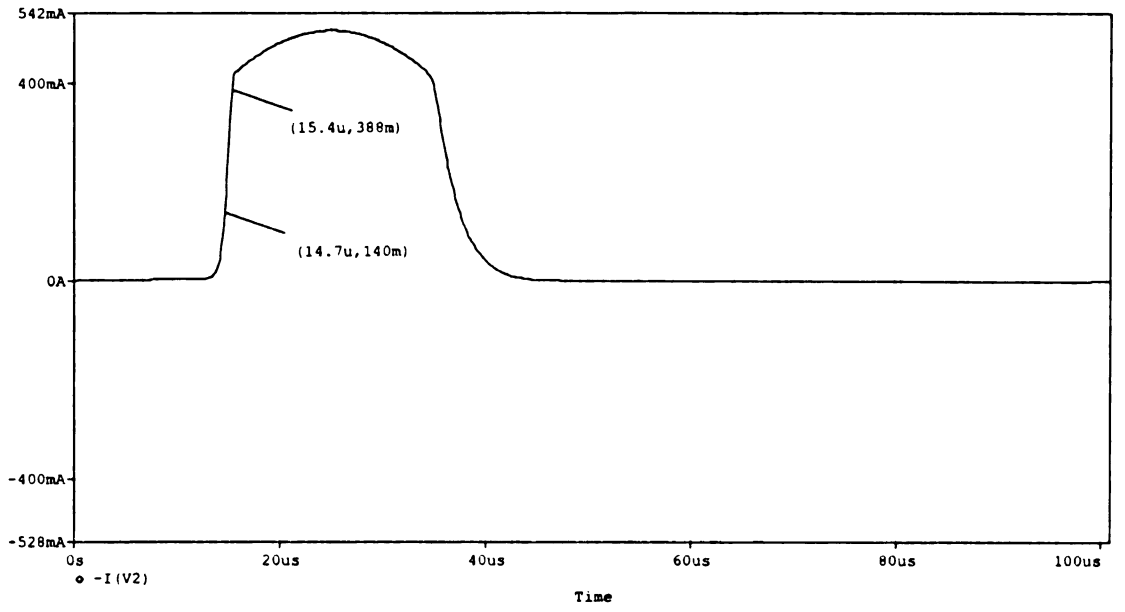


Figure 4.3.2: Graph of the current from V2 - rise time analysis

By analyzing the current coming from power supply, V_2 (Figure 4.3.2), the change in current over time can be calculated as follows:

$$\text{The rate of increase equals } \left(\frac{di}{dt}\right) = \frac{388m - 140m}{15.4\mu - 14.7\mu} = 354286\frac{A}{sec} \approx 350\frac{kA}{sec}$$

Some power supplies may not be able to switch this fast.

Chapter 5: Construction of the Circuit

5.1 Introduction

An actual circuit was constructed to observe the performance of the Class G amplifier. This tested if the circuit worked at all, if it showed signs of being more efficient than the Class B amplifier, and how music sounded when it was played through the Class G amplifier. The main benefit of building this circuit was the identification of the stability problem, which will be discussed in this chapter.

5.2 Breadboard Lab Data

The Class G amplifier was first built on a breadboard (Figure 5.2.1). The circuit was laid out to keep the connecting wires as short as possible. XANTREX power supplies where used to provide enough current to test this circuit. A function generator provided the test signal of a 1kHz sine wave. The circuit that was constructed used quarter-watt resistors. The transistors used were TIP31 (NPN) and TIP32 (PNP) with heat sinks attached. The small signal diodes were 1N4148 and the diodes for the power supplies were 1N5817 Shottky diodes.

The output of the Class G amplifier showed high frequency oscillations. Figure 5.2.2 shows the output of the Op-Amp and the voltage across a load resistor (10 Ω). This high frequency oscillation appeared when the input signal was large enough to cause the Class G amplifier to use the larger power supplies. After many attempts at rebuilding the circuit, the source of the high frequency oscillations could not be found. The decision was made to take the circuit off the breadboard and solder the circuit onto a perforated

board. No further calculations were made due to the fact that the circuit seemed to be unstable.

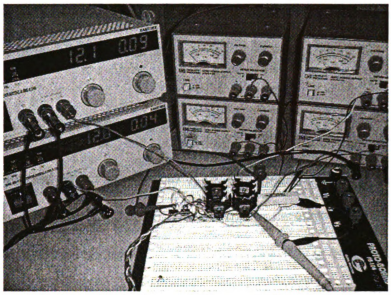


Figure 5.2.1: Picture of breadboard circuit

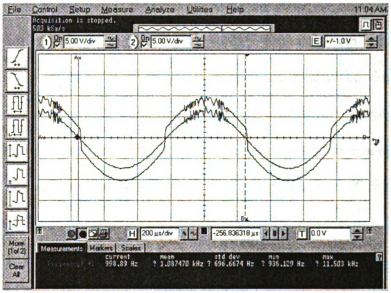


Figure 5.2.2: Plot of V_{OUT} and $V_{OP\text{-}AMP}$

5.3 Perforated Prototype Board Lab Data

The circuit was taken off the solderless protoboard and rebuilt on a radio shack perf-board to see if the parasitic capacitances of the solderless protoboard were effecting the performance of the Class G amplifier.

5.3.1 Using Switch-Mode Power Supplies

The protoboard circuit was hooked up to XANTREX switch-mode power supplies. Figure 5.3.1.1 is the graph of the output of the Op-Amp and the output across the 10 Ω load. There is a high frequency oscillation appearing in the output causing distortion. Figure 5.3.1.2 shows a close up view of the high frequency oscillations that are showing up in the output. The graph shows that the frequency of the oscillation is about 12 MHz. Figure 5.3.1.3 is the graph of the AC signal of the +15 volt power supply pin and the -15 volt power supply pin. Again, the high frequency oscillations appear. Figure 5.3.1.4 is a close-up view of the high frequency oscillations showing up on the power pins. The graph shows that the frequency of the oscillation is about 16 MHz. Figure 5.3.1.5 shows the output of the Op-Amp and the output voltage across the load when a 0.01uF capacitor was place from the +15 volt supply to the -15 volt supply. This is a suggested technique to eliminate high frequency oscillations [5] [6]. The high frequency oscillations have been eliminated. However, it is still unknown at this point what is causing the high frequency oscillation.

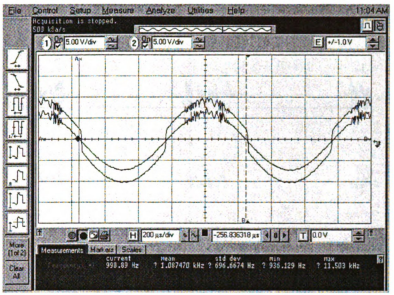


Figure 5.3.1.1: Plot of V_{OUT} and $V_{OP\text{-}AMP}$

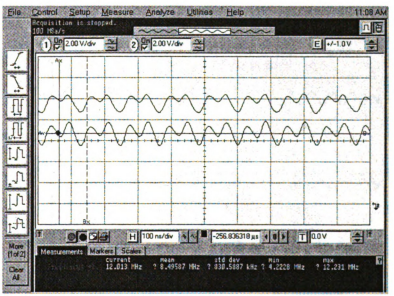


Figure 5.3.1.2: Plot of V_{OUT} and $V_{OP\text{-}AMP}$ - closer view

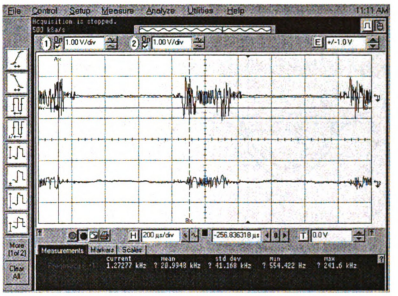


Figure 5.3.1.3: Plot of +/- 15 volt power supply pins

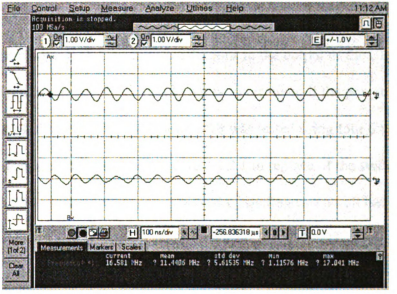


Figure 5.3.1.4: Plot of +/- 15 volt power supply pins - closer view

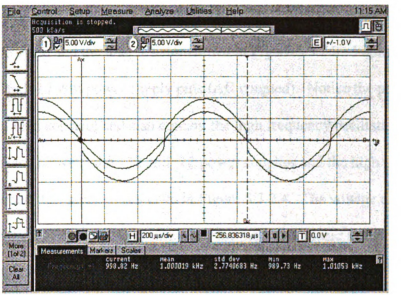


Figure 5.3.1.5: Plot of V_{OUT} and $V_{OP\text{-}AMP}$ with bypass capacitor added

5.3.2 Using Batteries

Since there were high frequency oscillations in the output of the Class G amplifier using switch mode power supplies, it could not be determined if the power supply was becoming momentarily unstable. The protoboard was tested using four 6 volt lantern batteries in the configuration shown in Figure 5.3.2.1 in replace of the switch mode power supplies. +12 and -12 volts was achieved by putting two 6 volt batteries in series.

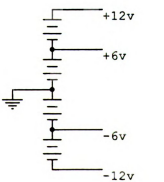


Figure 5.3.2.1: Schematic of power supply using batteries

Even when using batteries, a high frequency oscillation still appeared in the output of the Op-Amp and the load resistor shown in Figure 5.3.2.2. Figure 5.3.2.3 shows the +12 and -12 volt power supply pins (AC coupled). Notice the power supply voltages are not held constant and also contain the high frequency oscillation. A capacitor was place between the +12 and -12 power supplies and the high frequency oscillations seemed to disappear as shown in Figure 5.3.2.4. The voltage drops, however, still remain. Instead of using a 1kHz sine wave for the input, music from a CD player was used for this circuit. Figure 5.3.2.5 shows the +/- 12 volt supply pins without the added capacitor. Figure 5.3.2.6 shows the +/- 12 volt supply pins after the capacitor was added. The added capacitor has eliminated the high frequency noise problems in the circuit.

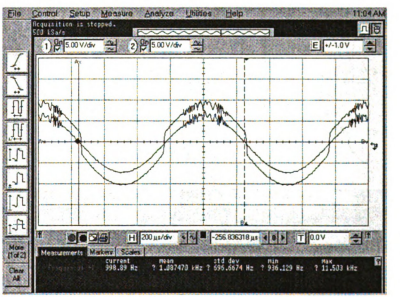


Figure 5.3.2.2: Plot of V_{OUT} and $V_{OP\text{-}AMP}$

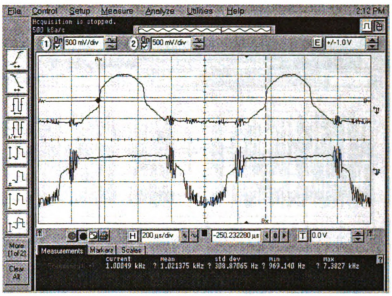


Figure 5.3.2.3: Plot of +/- 12 volt power supplies

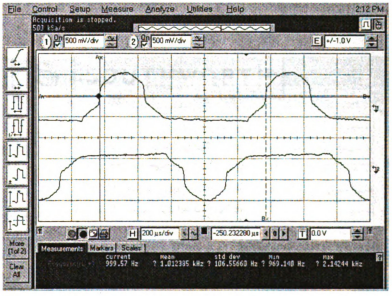


Figure 5.3.2.4: Plot of +/- 12 volt power supplies with bypass capacitor added

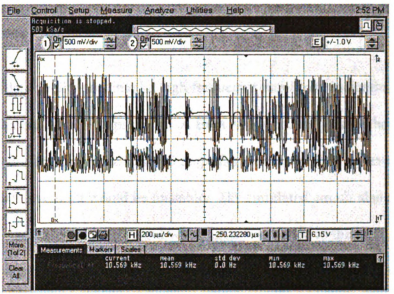


Figure 5.3.2.5: Plot of +/- 12 volt power supplies while playing music

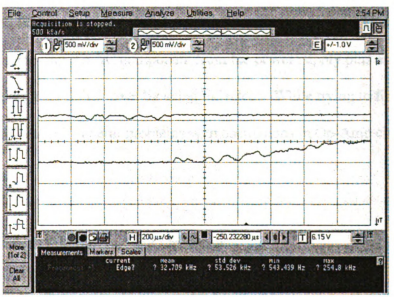


Figure 5.3.2.6: Plot of +/- 12 volt power supplies with capacitor while playing music

Chapter 6: Identifying Noise in Lab Data

6.1 Introduction

The lab data results presented a high frequency oscillation indicating that the Class G amplifier has a stability problem. A Beta Network Analysis method was used to try and identify that the simulated Class G amplifier was unstable. However, this method did not show that the circuit would be unstable. The simulated circuit also did not show high frequency oscillations in the output when noise was added to the input. Since the simulated data was not matching the lab data, the simulated circuit model needed to be revised. This chapter explains how the simulated circuit model was revised. Since the lab data showed that the power supply pins were oscillating, the circuit model was analyzed when the power pins were forced to oscillate by adding an AC component. This proved to be helpful in identifying the source of the stability problem. Then, the model was revised by removing the AC component from the power supply pins and allowing the power lines to oscillate on their own by using inductors. While trying to find ways to revise the Class G model, general problems with oscillations in Op-Amp circuits were also noted.

6.2 Problems with Oscillations and Op-Amps

From Analog Devices application notes [2], the Op-Amp can be simplified to the circuit in Figure 6.2.1. This schematic shows that most of the voltage difference between the amplifier output and the negative supply appears across the compensation capacitor.

Because the negative PSRR is limited at high frequencies, the oscillations on the negative power supply will appear on the output.

For testing the stability of the circuit, one method is to analyze the beta network of the Op-Amp (See Appendix B) [15]. This will test the stability of the circuit due to gain-bandwidth-product, input and output impedance, but because the Op-Amp is removed during the beta network analysis, it will not account for high frequencies coming through the Op-Amp via the negative supply.

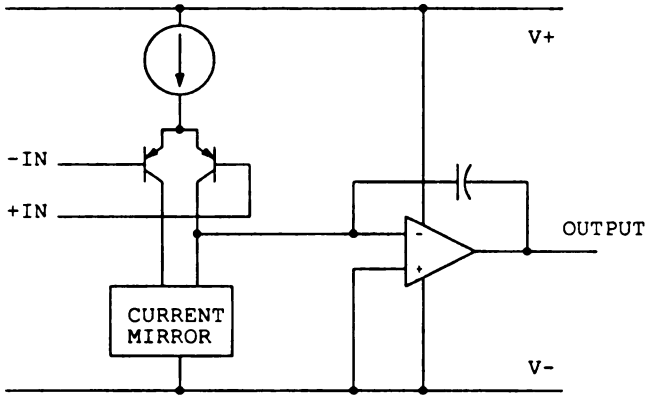


Figure 6.2.1: Simplified "real" Op-Amp

6.3 Oscillating the Power Lines

New stability problems came from the lab results. The problem that was found was that when Q_1 was active and Q_2 was just becoming active, the output would have a lot of distortion at the top of the wave. Lab results also showed that the power lines for the +15 and -15 volts where oscillating out of phase at a high frequency. In order to figure out where this problem was coming from, the power supplies in the PSpice circuit model where made to oscillate at 12MHz by adding an AC component to the voltage

sources V_2 and V_2'. The PSpice circuit model used the full model of the 741 Op-Amp (ICL8741) [16] so that the power pins of the Op-Amp would also be modeled.

Figure 6.3.1 shows the V_{OUT} and $V_{OP\text{-}AMP}$ with the power supplies oscillating out of phase by 180°. This graph shows the same output that was obtained from the circuit built in lab. Figure 6.3.2 shows a close up view of Figure 6.3.1 in the location where the output is oscillating along with the large power supply lines.

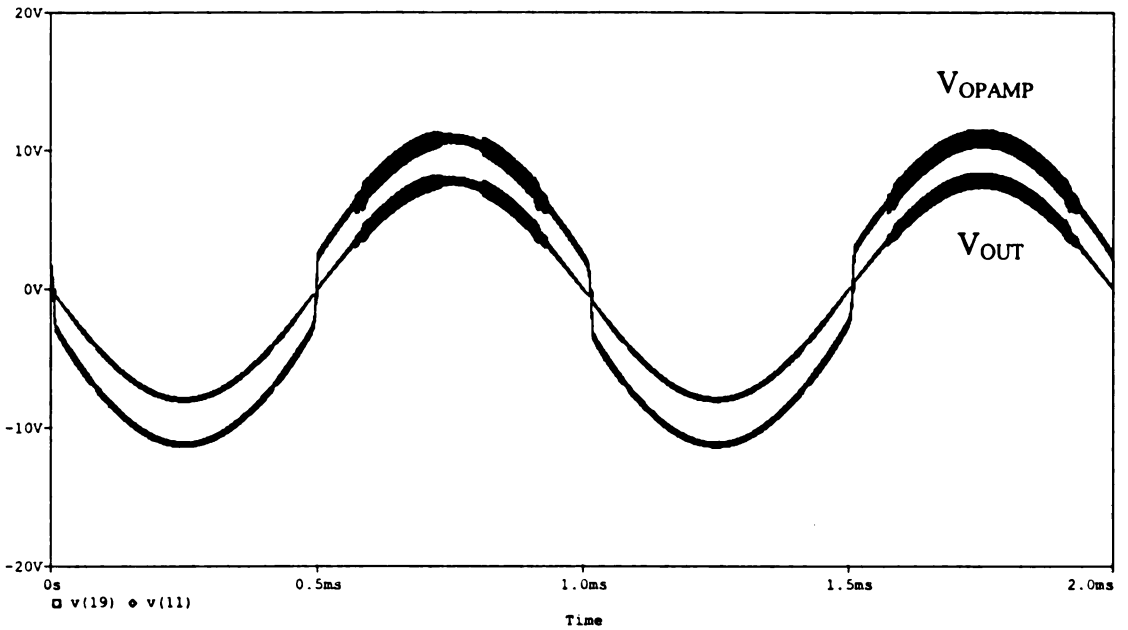


Figure 6.3.1: Graph of V_{OUT} and $V_{OP\text{-}AMP}$ - oscillating power supplies in out of phase

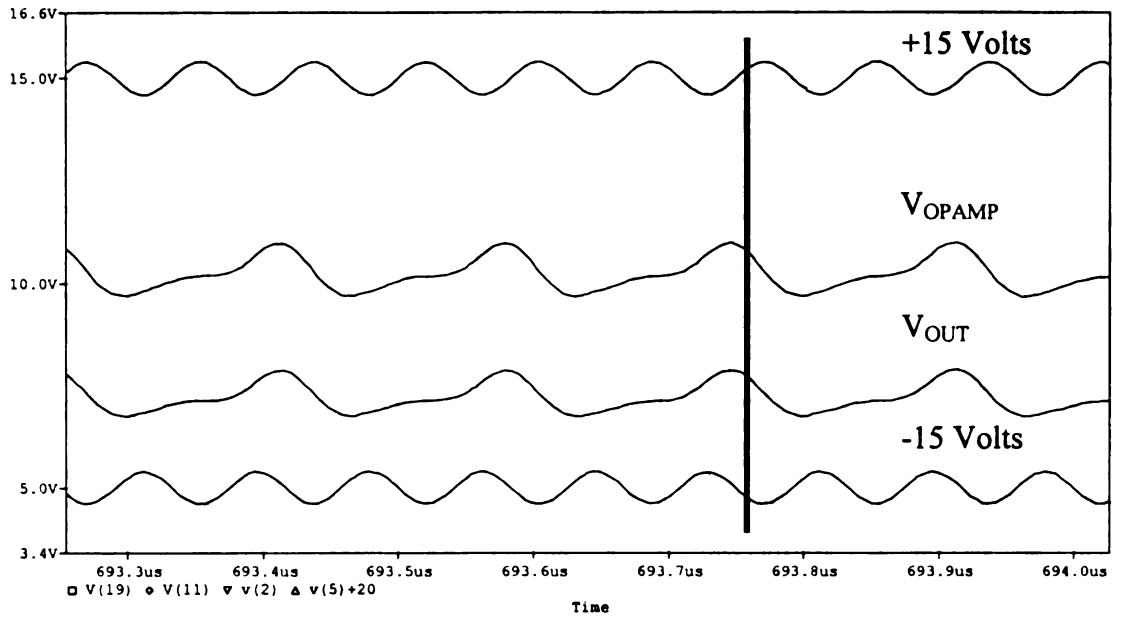


Figure 6.3.2: Close up view of Figure 6.3.1

The circuit was tested by oscillating only the negative power supply, by oscillating only the positive power supply, and by oscillating both power supplies in phase. The results from these three tests can be seen in Figure 6.3.3, 6.3.4, 6.3.5, 6.3.6, and 6.3.7. Oscillating the negative power supply has more of an effect on the output than oscillating only the positive power supply. Also, oscillating the power supplies out of phase causes more distortion in the output than oscillating the power supplies in phase. The PSpice circuit file used for these tests can be seen in the Appendix for Chapter 6.

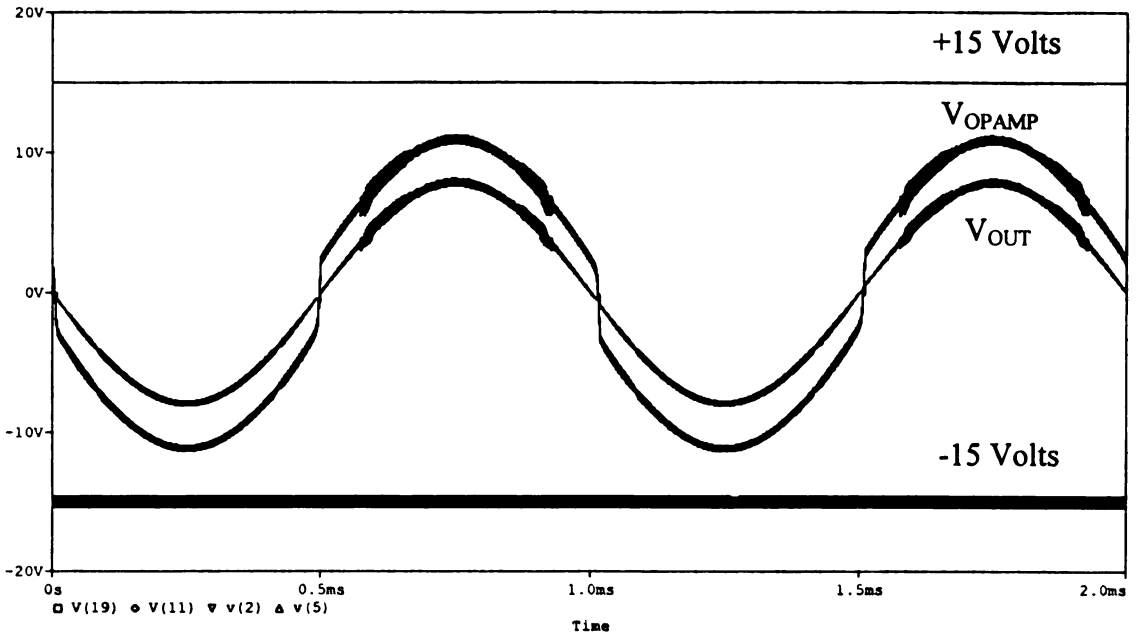


Figure 6.3.3: Graph of V_{OUT} and $V_{OP\text{-}AMP}$ - oscillating negative power supply only

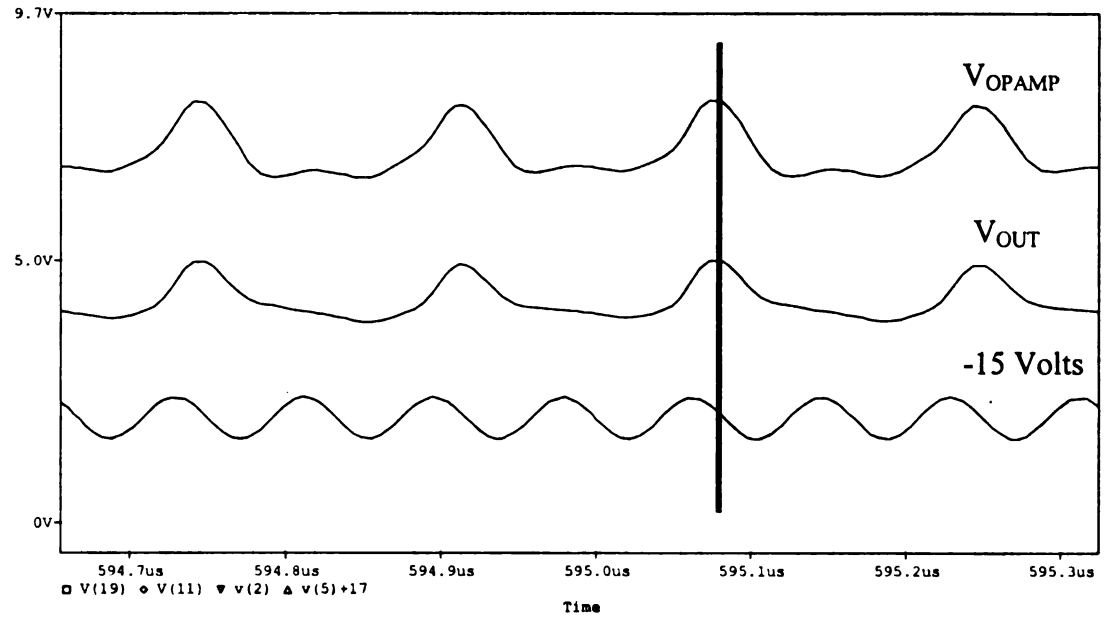


Figure 6.3.4: Close up view of Figure 6.3.3

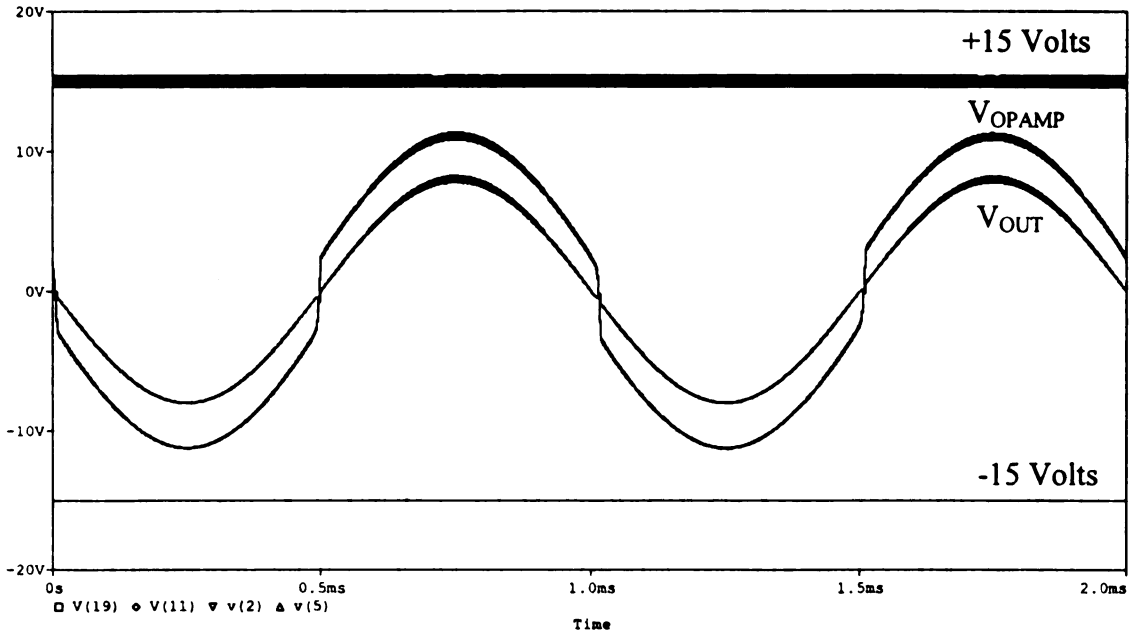


Figure 6.3.5: Graph of V_{OUT} and $V_{OP\text{-}AMP}$ - oscillating positive power supply only

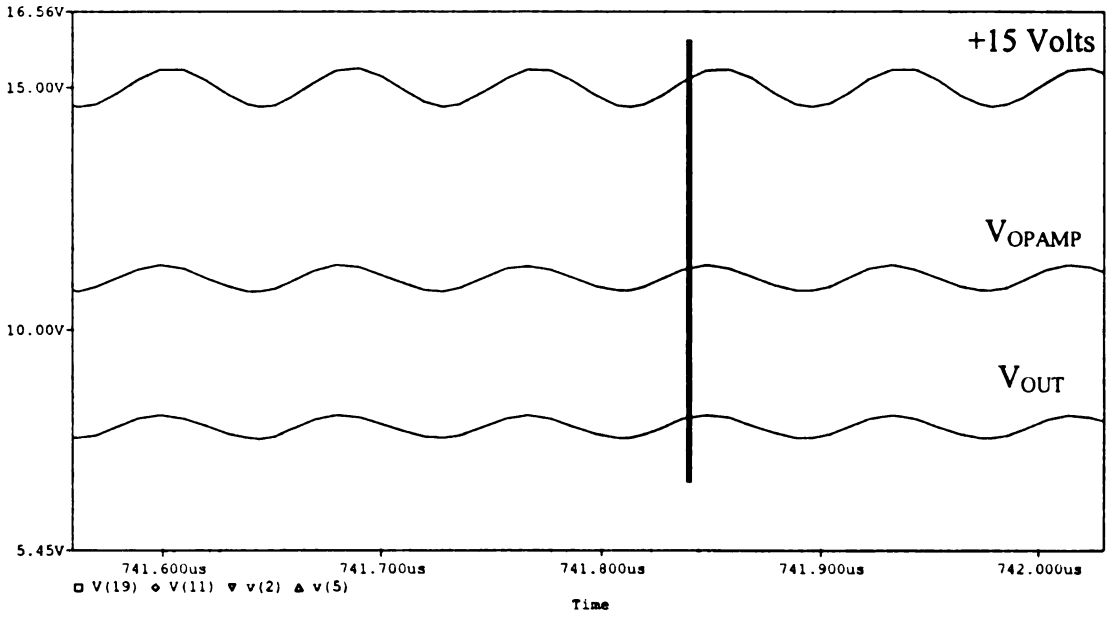


Figure 6.3.6: Close up view of Figure 6.3.5

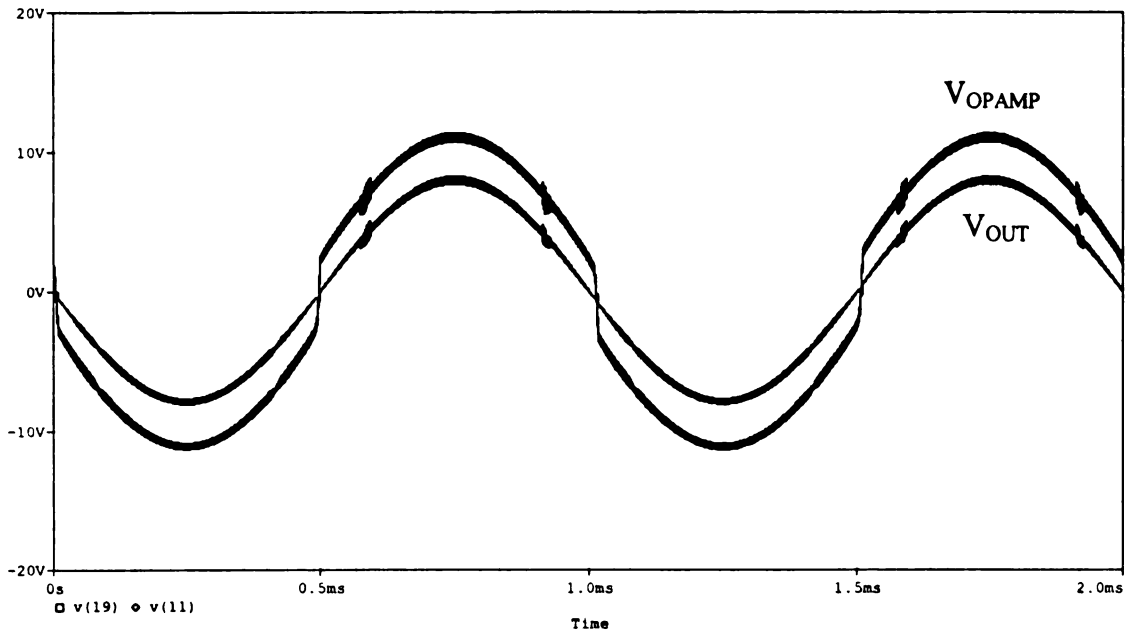


Figure 6.3.7: Graph of V_{OUT} and $V_{OP\text{-}AMP}$ - oscillating power supplies in phase

6.4 Putting Inductors on the Power Lines

When the large power supplies were made to oscillate at 12MHz, the output of the circuit was similar to the output of the built circuit in the lab. Another approach was used to test the stability of the circuit with the Op-Amp. Because the change in current of the power supplies is so high (di/dt), it was assumed that inductance in the power supply leads would cause problems with the output of the circuit. To see how the circuit would behave if the power supply lines were allowed to oscillate, a small inductance was added to the large power supplies. This will not affect the DC voltages needed to power the Op-Amp, but will, however, allow high frequencies to get from the output stage transistors to the negative power supply pin of the Op-Amp. Figure 6.4.1 shows the new schematic of this circuit to be analyzed by PSpice.

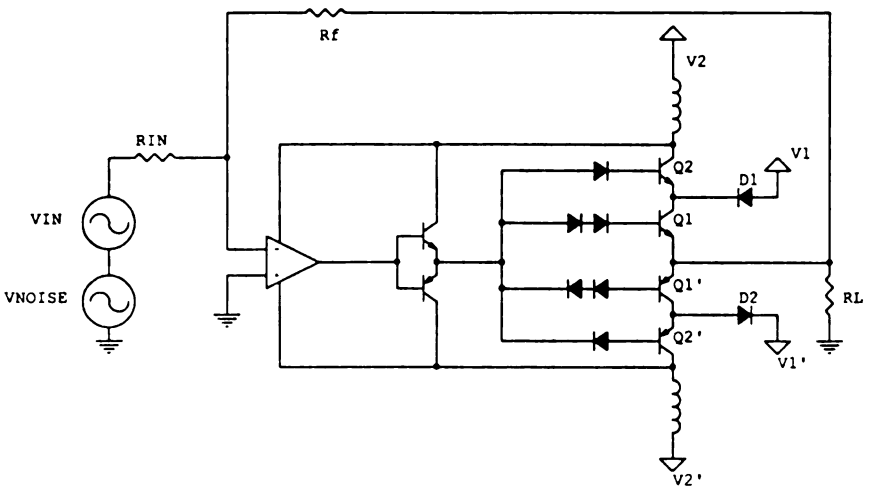


Figure 6.4.1: Schematic for testing stability

The circuit in Figure 6.4.1 has a V_{IN} of 1kHz and an added noise signal V_{NOISE} of 400kHz. The circuit will amplify the added noise in the circuit if the circuit is marginally stable. The output of this circuit is shown in Figure 6.4.2. In most of the output wave, the 400kHz signal appears but it is attenuated. However, when the larger power supplies are being used, the noise signal has caused a high frequency oscillation at the top of the waveform. Figure 6.4.3 shows V_{OUT} with V_{IN} on top to clearly that the noise signal is being amplified only at the top of the output wave. This output looks just like the output that was achieved in the lab. Figure 6.4.4 shows that the positive power supply is oscillating with a larger magnitude than the negative power supply. Figure 6.5.5 shows a close up view of the positive and negative large power supplies. This graph shows that the oscillations are out of phase, which is similar to the lab data collected.

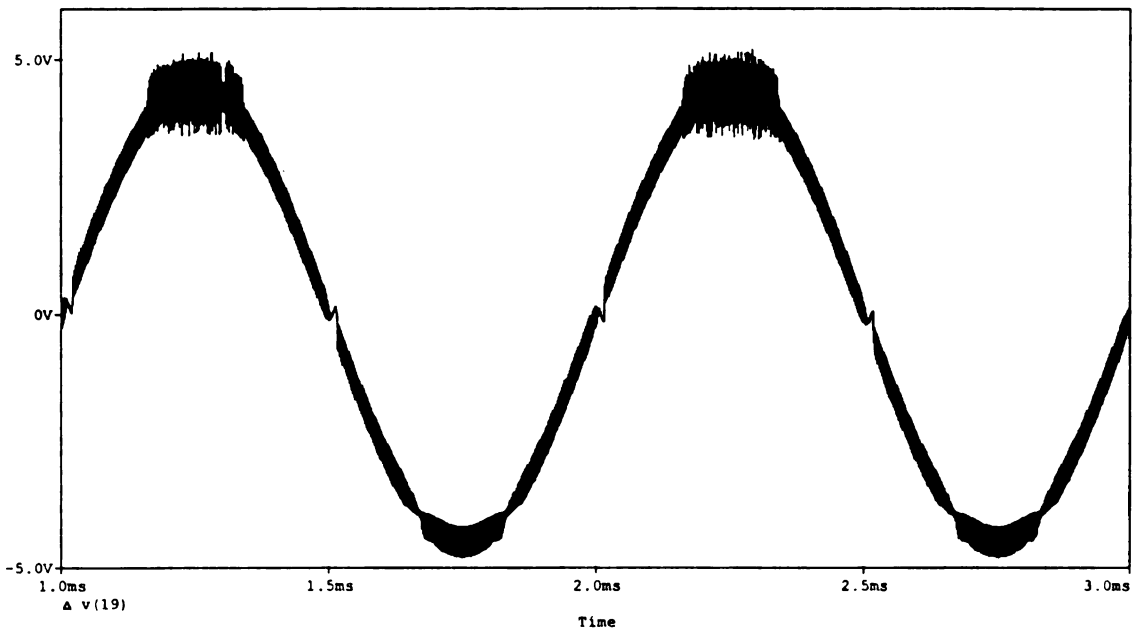


Figure 6.4.2: Graph of V_{OUT}

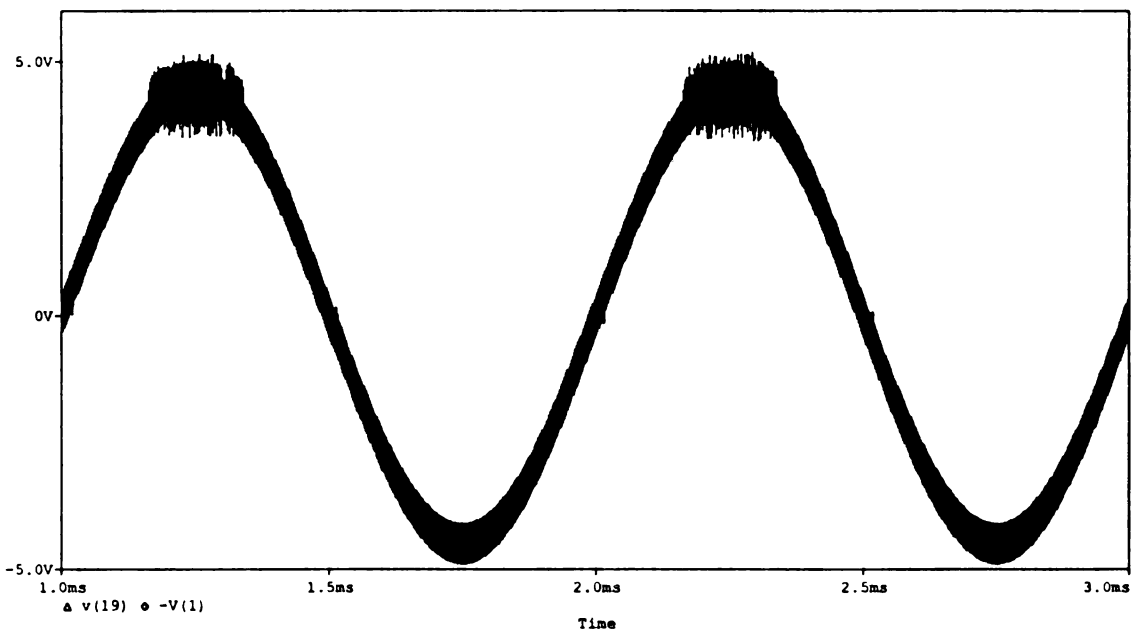


Figure 6.4.3: Graph V_{OUT} and $-V_{IN}$

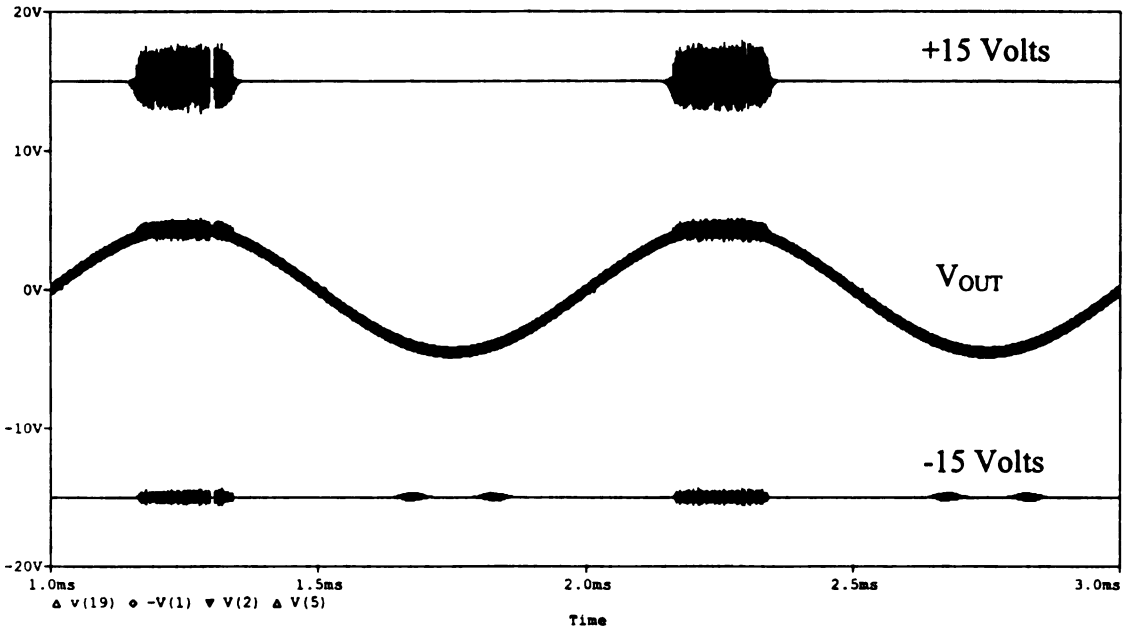


Figure 6.4.4: Graph of V_{OUT}, $-V_{IN}$, and power supply pins

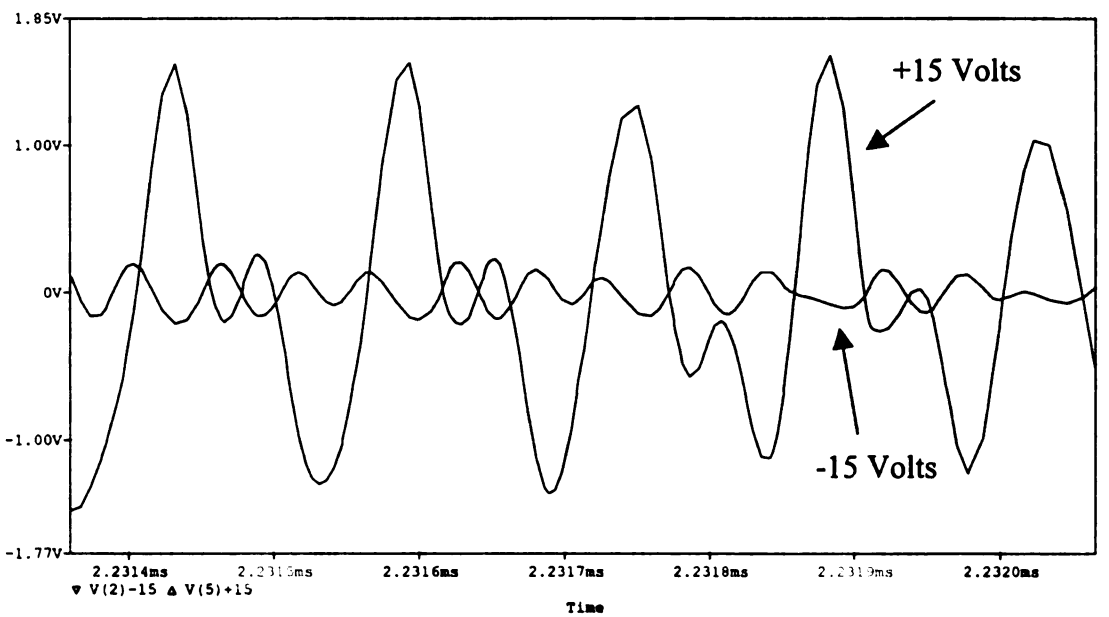


Figure 6.4.5: Graph of power supply pins – close up view

Chapter 7: Beta Analysis Method

7.1 Introduction

The Beta Network Analysis Method (See Appendix B and reference [15]) was used to show the stability of the circuit. With this particular problem, only part of the output waveform is unstable. In order for the Beta Network Analysis Method to show that the circuit can become unstable, many input biasing points need to be tested first. PSpice was used to get the numerical results for the AC models of the transistors and diodes in the circuit.

7.2 Converting to Beta Network Circuit

To convert the Class G amplifier to a beta network for analysis, high frequency models were used for the transistors and the diodes. The high frequency model for the transistor is the Giacoletto's hybrid-π model shown in Figure 7.2.1 [11] [12].

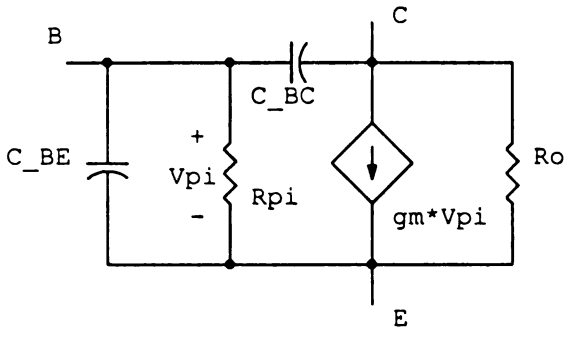


Figure 7.2.1: Giacoletto transistor model

7.2.1 Beta Network

The transistors and diodes in the circuit were replaced with their high frequency AC models. The Op-Amp was replaced with its input resistance and capacitance, and its output resistance.

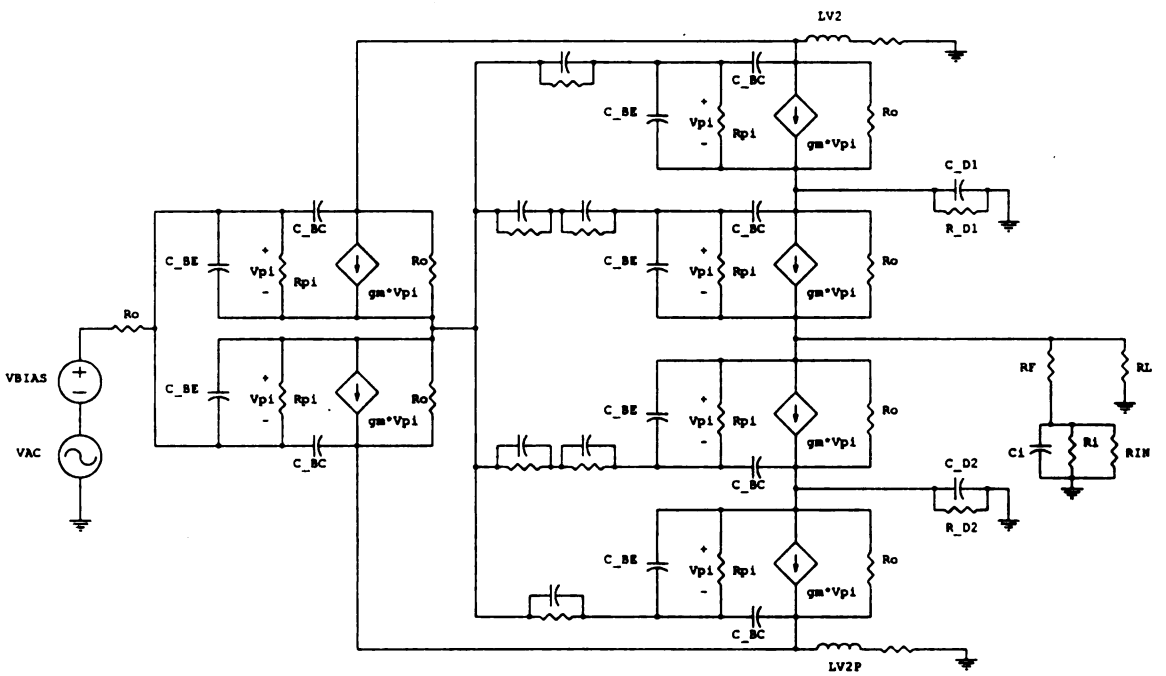


Figure 7.2.1.1: Beta network - high frequency model

7.2.2 Identifying Stability Problems

The beta network was analyzed by changing the input biasing level and observing the gain of $1/\beta$ compared to the open-loop gain of the Op-Amp. The phase angle where these two plots cross gives the phase margin of the full circuit. The values for the transistor and the diode models were obtained from PSpice by setting the input of the original circuit to the desired biasing level and observing the small signal bias solution

from the PSpice output file. For most of the biasing levels, the phase margin indicated that the circuit would be stable. However, there were two biasing levels (6.133 volts & -6.233 volts) that caused the gain of $1/\beta$ to cross the open-loop gain of the Op-Amp a second time! The phase margin at these two points indicated that the circuit would be unstable (Figure 7.2.2.1 & Figure 7.2.2.2).

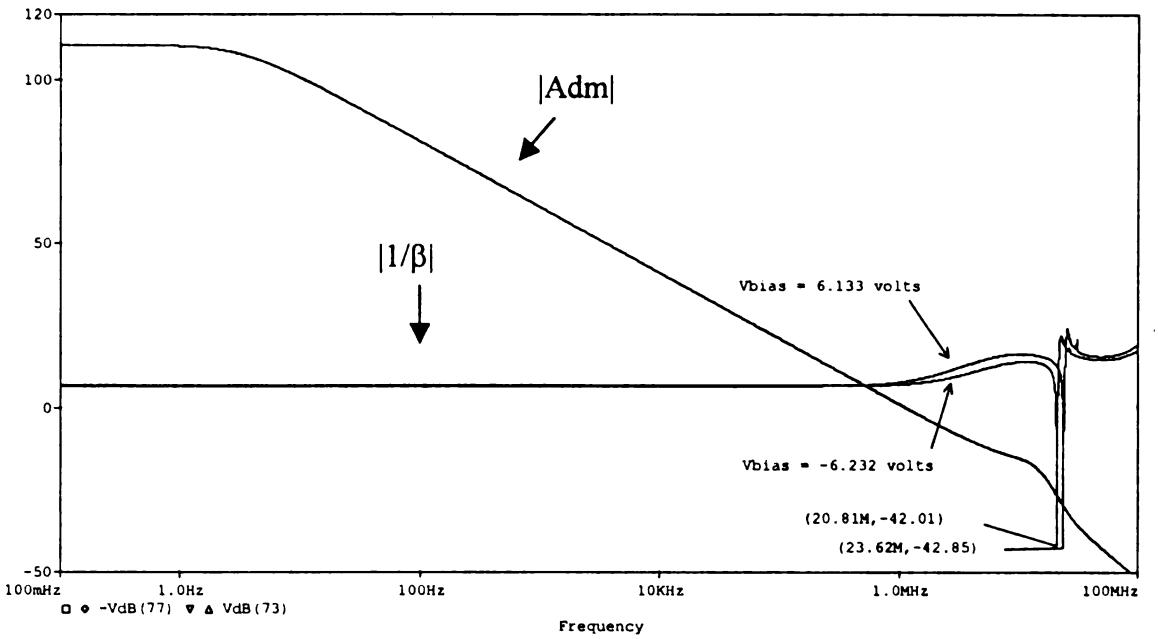


Figure 7.2.2.1: Graph of $\left|\frac{1}{\beta}\right|$ and $|Adm|$

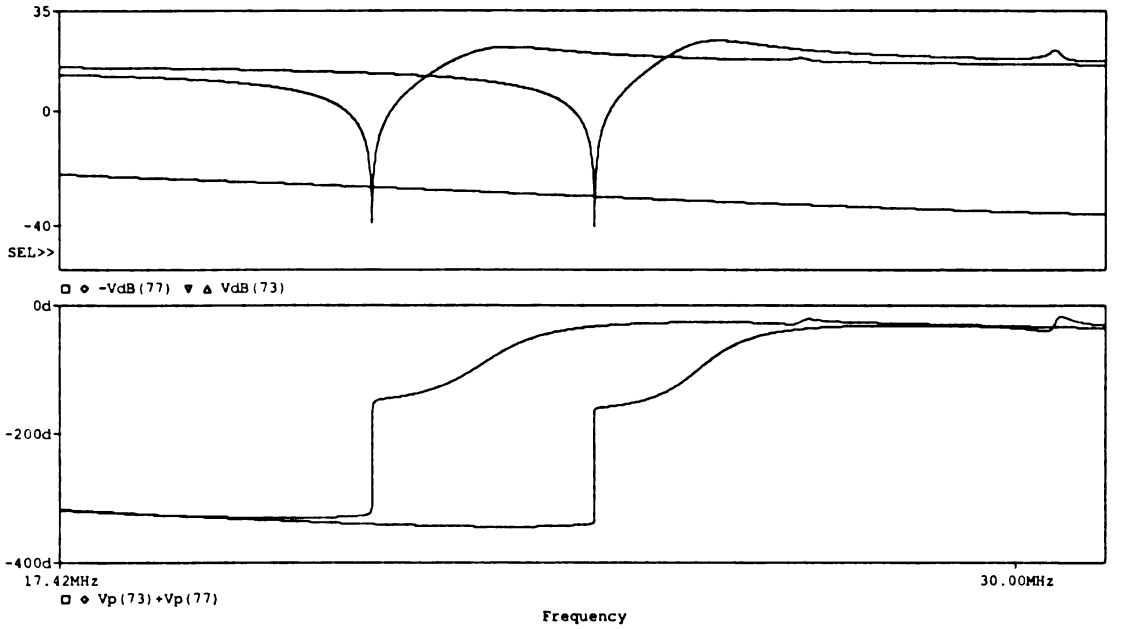


Figure 7.2.2.2: Close up view of Figure 7.2.2.1

7.3 Simplifying the Beta Network

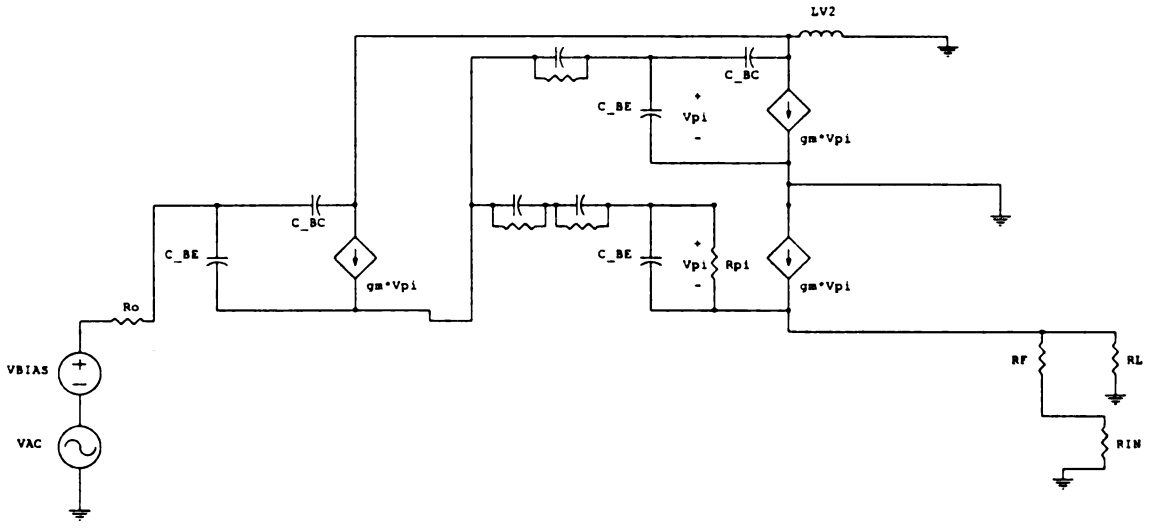


Figure 7.3.1: Schematic of simplifying the beta network

The beta network was then simplified to just focus on what was causing the gain of 1/β to cross the open-loop gain of the Op-Amp a second time (Figure 7.3.1, 7.3.2, & 7.3.3). The output of 1/ β of the simplified circuits was compared to the original beta

circuit and is shown in Figure 7.3.4 & Figure 7.3.5.

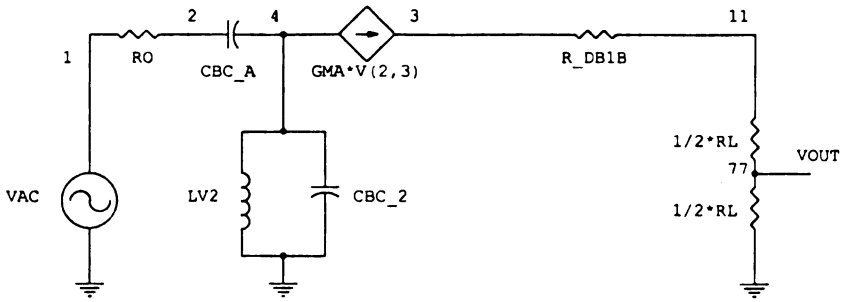


Figure 7.3.2: Simplified schematic when V_{BIAS} = 6.133 volts

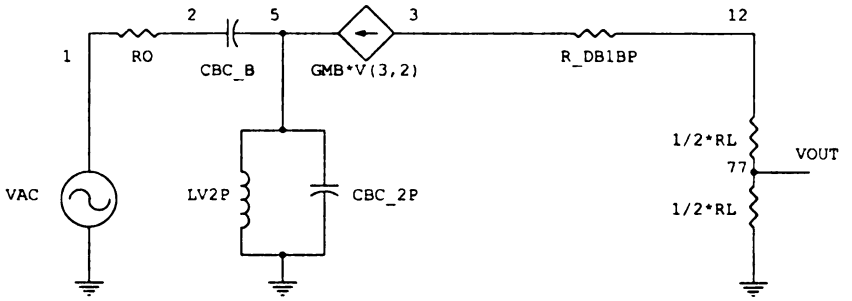


Figure 7.3.3: Simplified schematic when V_{BIAS} = -6.232 volts

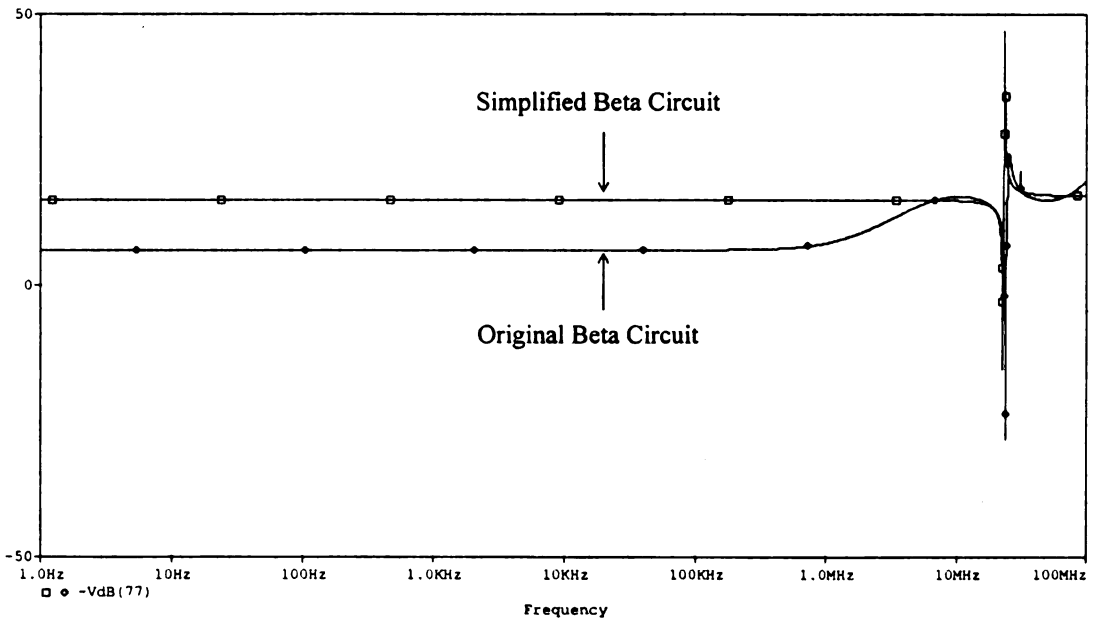


Figure 7.3.4: Graph of $\left|\frac{1}{\beta}\right|$ where V_{BIAS} = 6.133 volts

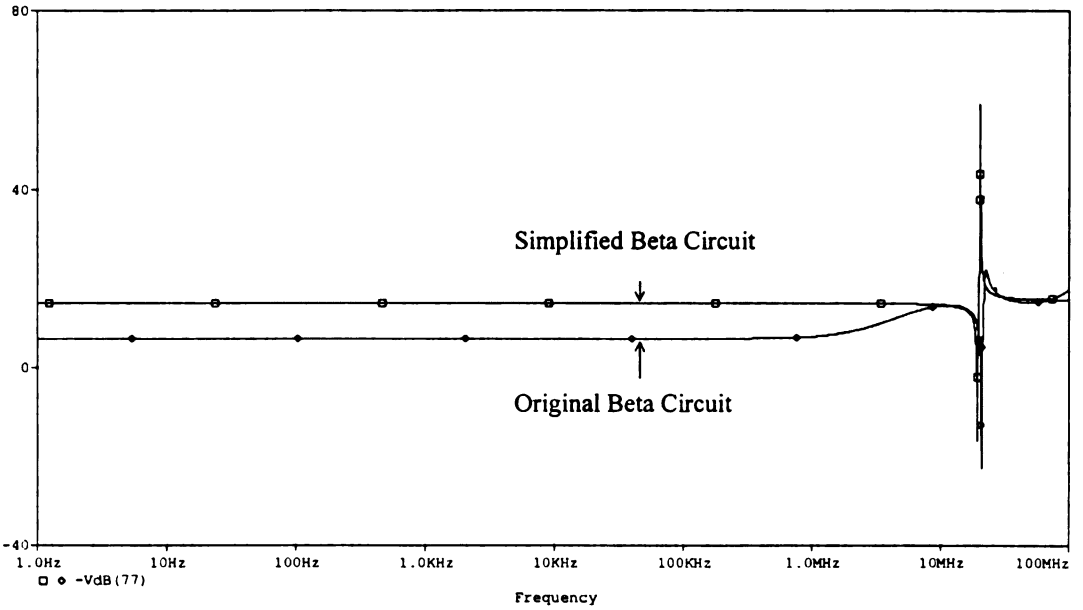


Figure 7.3.5: Graph of $\left|\frac{1}{\beta}\right|$ where V_{BIAS} = -6.232 volts

7.4 Verifying Using Sspice

These simplified circuits were then analyzed using Symbolic SPICE (Sspice). To cause the graph of the gain of 1/ β to shoot down towards negative infinity like it does, the Laplace Transform of the output equation must contain a second order zero, which will be called a "Form VII", with a very high Q [15]. This will be the same as saying 1/V(77) (which is $1/V_{OUT}$) will have a second order pole, which will be called a "Form VIII", with a very high Q value [15]. Sspice found the symbolic output equation along with the numerical output equations shown.

The first Sspice analysis was performed while using V_{BIAS} = 6.133 volts. The equation obtained from Sspice for the $1/V_{OUT}$ is as follows:

$$\frac{1}{V(77)} = \frac{1}{\beta} = \frac{.9181e-30\cdot(s+.9052e10)\cdot(s^2+.2775e6\cdot s+.1981e17)}{.1239e-20\cdot s^2+.2667e-4}$$

$$= \frac{6.17\cdot\left(\frac{s}{1.44GHz\cdot 2\pi}+1\right)\cdot\left(\frac{s^2}{(22.4MHz\cdot 2\pi)^2}+\frac{s}{(22.4MHz\cdot 2\pi)\cdot 507}+1\right)}{\left(\frac{s^2}{(23.35MHz\cdot 2\pi)^2}+1\right)}$$

$$\text{Numerator of } V(77) = \frac{2\cdot(LV2\cdot(CBCA+CBC2)\cdot s^2+1)}{RO\cdot GMA\cdot RL\cdot REQDBIB}$$

$$\text{Form VII of } \frac{1}{V(77)} = (LV2\cdot(CBCA+CBC2)\cdot s^2+1)$$

$$= \frac{s^2}{\left(\sqrt{\frac{1}{LV2\cdot(CBCA+CBC2)}}*\frac{1}{2\pi}\right)^2}+\frac{s}{\left(\sqrt{\frac{1}{LV2\cdot(CBCA+CBC2)}}*\frac{1}{2\pi}\right)*\infty}+1$$

$$fc \approx \sqrt{\frac{1}{LV2\cdot(CBCA+CBC2)}}*\frac{1}{2\pi}$$

$$Q \approx \infty$$

Using the approximator option in Sspice with a threshold of 0.9, the denominator can be found to be:

$$\text{Denominator of } V(77) = \frac{2}{RL}\cdot\left(CBCA\cdot s+\frac{1}{RO}\right)\cdot(LV2\cdot CBC2)\cdot s^2+1)$$

$$\text{Form VIII of } V(77) = 1/(LV2\cdot CBC2)\cdot s^2+1$$

$$f_c \approx \sqrt{\frac{1}{LV2\cdot CBC2}}\cdot\frac{1}{2\pi}$$

$$Q \approx \infty$$

The second Sspice analysis was performed while using V_{BIAS} = -6.232 volts. The equation obtained from Sspice for the $1/V_{OUT}$ is as follows:

$$\frac{1}{V(77)} = \frac{1}{\beta} = \frac{.2239e-29\cdot(s+.6806e10)\cdot(s^2+.3097e6\cdot s+.1470e17)}{.2592e-20\cdot s^2+.4198e-4}$$

$$= \frac{5.34\cdot\left(\frac{s}{1.08GHz\cdot 2\pi}+1\right)\cdot\left(\frac{s^2}{(19.3MHz\cdot 2\pi)^2}+\frac{s}{(19.3MHz\cdot 2\pi)\cdot 391}+1\right)}{\left(\frac{s^2}{(20.25MHz\cdot 2\pi)^2}+1\right)}$$

$$\text{Numerator of } V(77) = \frac{2\cdot(LV2P\cdot(CBCB+CBC2P)\cdot s^2+1)}{RO\cdot GMB\cdot RL\cdot REQDBIBP}$$

$$\text{Form VIII of } \frac{1}{V(77)} = (LV2P\cdot(CBCB+CBC2P)\cdot s^2+1)$$

$$= \frac{s^2}{\left(\sqrt{\frac{1}{LV2P\cdot(CBCB+CBC2P)}}*\frac{1}{2\pi}\right)^2} + \frac{s}{\left(\sqrt{\frac{1}{LV2P\cdot(CBCB+CBC2P)}}*\frac{1}{2\pi}\right)*\infty}+1$$

$$fc = \sqrt{\frac{1}{LV2P\cdot(CBCB+CBC2P)}}*\frac{1}{2\pi}$$

$$Q = \infty$$

Using the approximator option in Sspice with a threshold of 0.9, the denominator can be found to be:

$$\text{Denominator of } V(77) = \frac{2}{RL}\cdot\left(CBCB\cdot s+\frac{1}{RO}\right)\cdot(LV2P\cdot CBC2P)\cdot s^2+1)$$

$$\text{Form VIII of } V(77) = 1/(LV2P\cdot CBC2P)\cdot s^2+1)$$

$$f_c \approx \sqrt{\frac{1}{LV2P\cdot CBC2P}}\cdot\frac{1}{2\pi}$$

$$Q \approx \infty$$

7.4.1 Identifying the problem

The Q of the simplified circuits at the two different biasing levels is too high. A Q this high means that at this frequency, the noise will be greatly amplified in the circuit to the point where the output will oscillate at this frequency. This is the stability problem with the original circuit and can be fixed.

7.5 Fixing the Stability Problem

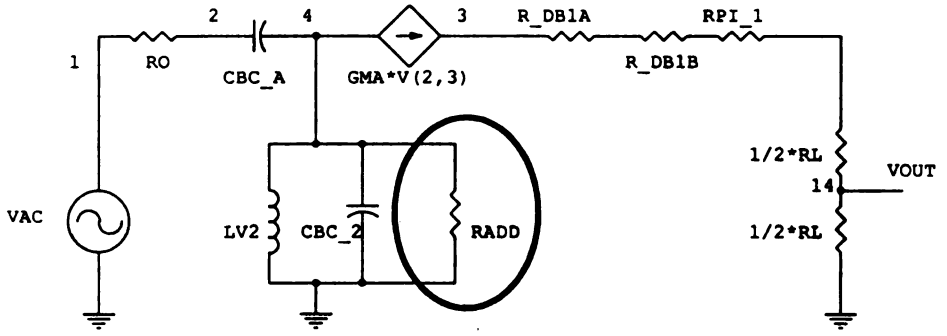


Figure 7.5.1: Adding R_{ADD} to lower the Q value

To fix the stability problem previously shown, the Q of the simplified beta network circuits must be dramatically lowered. The general equation of V_{OUT} for the circuit in Figure 7.5.1 is shown below (general equation). Before the resistor R_{ADD} was added to the circuit, Q1=∞ and Q2=362.8. The stability problem can be solved by adding a small resistance, R_{ADD} into the circuit to lower the values of Q1 and Q2. A value of 10 Ohms was chosen for R_{ADD}, which lowered Q1 to 0.068 and Q2 to 0.074 (Numerical Analysis).

General Equation:

$$\frac{V_{OUT}}{V_{AC}} = \frac{A\left(\frac{s^2}{(w_1)^2} + \frac{s}{w_1 \cdot Q_1} + 1\right)}{\left(\frac{s}{w_3} + 1\right)\cdot\left(\frac{s^2}{(w_2)^2} + \frac{s}{w_2 \cdot Q_2} + 1\right)}$$

Numerical Analysis:

$$\frac{V_{OUT}}{V_{AC}} = \frac{0.285\cdot\left(\frac{s^2}{(23.37MHz\cdot 2\pi)^2} + \frac{s}{(23.37MHz\cdot 2\pi)\cdot 0.068} + 1\right)}{\left(\frac{s}{1.607GHz\cdot 2\pi} + 1\right)\cdot\left(\frac{s^2}{(21.29MHz\cdot 2\pi)^2} + \frac{s}{(21.29MHz\cdot 2\pi)\cdot 0.074} + 1\right)}$$

7.5.1 Additions to the circuit

Adding the resistor of 10 Ohms would cause problems at low frequencies (Figure 7.5.1.1). At low frequencies, too much current would be going through R_{ADD} and cause the circuit to not function properly or become very inefficient.

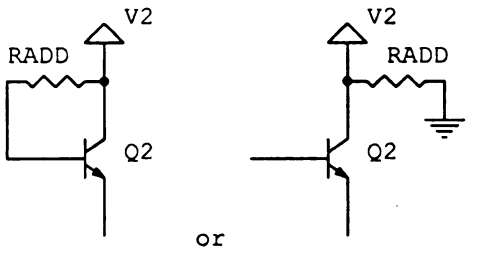


Figure 7.5.1.1: Adding R_{ADD} in original circuit

By adding a capacitor in series with R_{ADD}, C_{ADD} (0.01uF), the desired effect can be achieved without the major power losses at low frequencies (Figure 7.5.1.2). Figure 7.5.1.3 shows how this would be added to the simplified circuit.

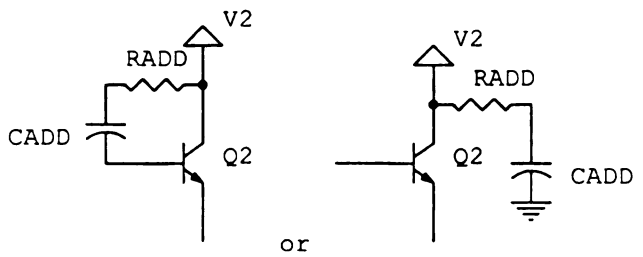


Figure 7.5.1.2: R_{ADD} in Series with C_{ADD}

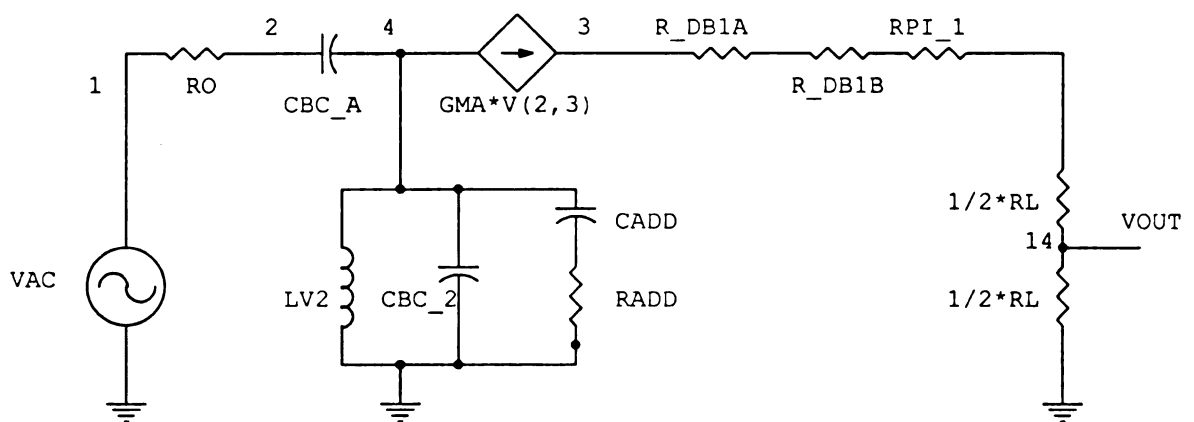


Figure 7.5.1.3: Adding C_{ADD} and R_{ADD} in series

7.5.2 Reevaluating Using Sspice

The capacitor in series with the resistor (R_{ADD} and C_{ADD}) was added to the simplified circuit where R_{ADD} equals 10Ω and C_{ADD} equals 0.001uF. The output equation was reevaluated using Sspice and shown below (Numerical Analysis). The capacitor affected the center frequency of the Form VII and Form VIII and also added a pole and a zero at very close frequencies. The pole and zero, because the frequencies are so close (343MHz and 284MHz), can be approximated to cancel each other out. The Form VII and VIII center frequencies are the same (1.59MHz) with low Q values (6.3) so they also

can be approximated to cancel each other out. This leaves only a pole at 1.6GHz. Therefore, the capacitor in series with the resistor should eliminate the stability problem.

Numerical Analysis:

$$\frac{V_{OUT}}{V_{AC}} = \frac{0.284 \cdot \left(\frac{s}{343.3MHz \cdot 2\pi} + 1\right) \cdot \left(\frac{s^2}{(1.59MHz \cdot 2\pi)^2} + \frac{s}{(1.59MHz \cdot 2\pi) \cdot 6.31} + 1\right)}{\left(\frac{s}{1.607GHz \cdot 2\pi} + 1\right) \cdot \left(\frac{s}{284.9MHz \cdot 2\pi} + 1\right) \cdot \left(\frac{s^2}{(1.59MHz \cdot 2\pi)^2} + \frac{s}{(1.59MHz \cdot 2\pi) \cdot 6.32} + 1\right)}$$

$$\approx \frac{0.284}{\left(\frac{s}{1.607GHz \cdot 2\pi} + 1\right)}$$

7.5.3 Verifying with PSpice

The numerical analysis equation can then be verified using PSpice to plot the equation. Figure 7.5.3.1 shows the gain of V_{OUT}/V_{AC} of this modified circuit. Figure 7.5.3.2 shows the graph of the numerical analysis equation separated into a Form VII and a Form VIII. This graph shows the canceling of the pole and zero described above. The PSpice file to plot the Form VII and Form VIII is shown in Figure 7.5.3.3.

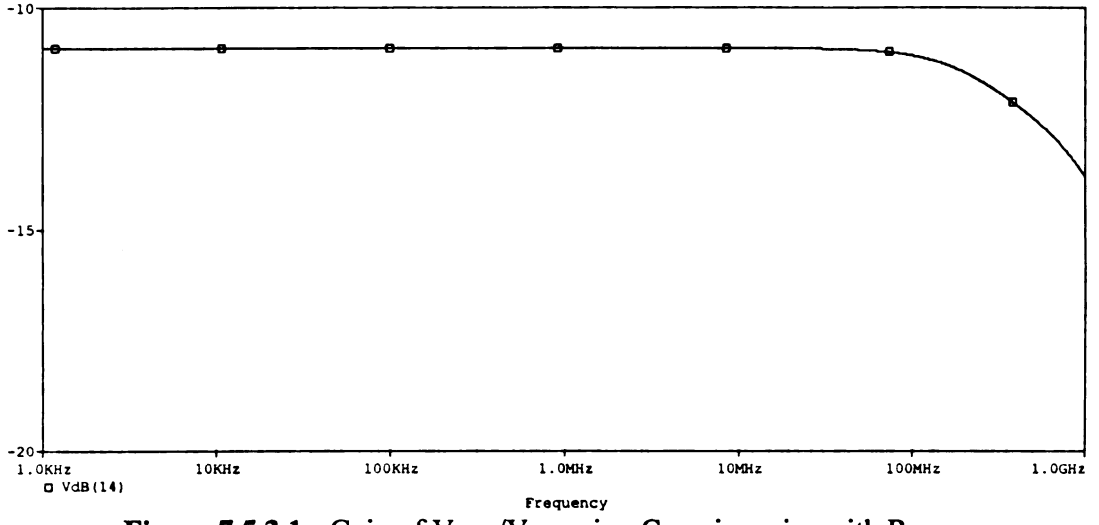


Figure 7.5.3.1: Gain of V_{OUT}/V_{AC} using C_{ADD} in series with R_{ADD}

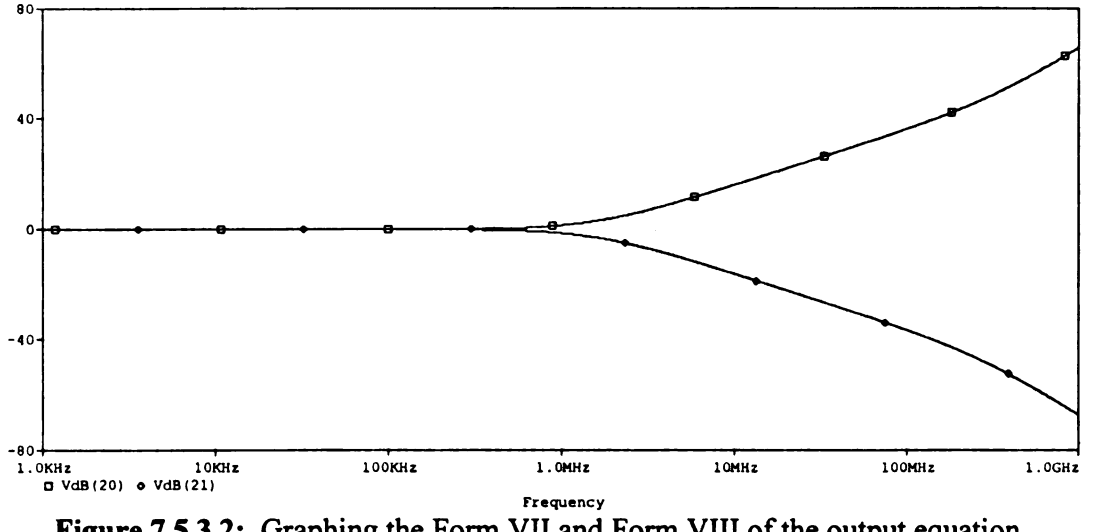


Figure 7.5.3.2: Graphing the Form VII and Form VIII of the output equation

The PSpice circuit file:

```
Plotting Forms 7 and 8VAC 1 0 AC 1
*  V14 is the output voltage of the circuit above
*  The Form 7 of the equation for this simplified circuit
E5 20 0 LAPLACE {V(1,0)}
{s^2/(23.37e6*2*3.1416)^2+s/((23.37e6*2*3.1416)*0.068)+1}
*  The Form 8 of the equation for this simplified circuit
E6 21 0 LAPLACE {V(1,0)}
{1/(s^2/(21.29e6*2*3.1416)^2+s/(21.29e6*2*3.1416*0.074)+1)}
.AC DEC 9000 1000 1000MEG
.PROBE
.END
```

Figure 7.5.3.3: PSpice circuit file to plot Form VII and VIII

Now, going back to the original Class G amplifier circuit using actual parts and not the AC models, the Beta Network Analysis is performed again with the addition of R_{ADD} and C_{ADD} (R_{ADD} = 10 Ω, C_{ADD} = 0.001 μF). The graph of the Beta Network Analysis when V_{BIAS} equals 6.133 volts is shown in Figure 7.5.3.4. The graph shows a plot of the phase of the beta network plus the Op-Amp. This plot indicates that the phase margin is 180°-108 ° = 72 °, which is stable. The graph of the Beta Network Analysis when V_{BIAS} equals -6.232 volts is shown in Figure 7.5.3.5. The graph shows a plot of the phase of the beta network plus the Op-Amp. This plot indicates that the phase margin is 180°-103 ° = 77 °, which is also stable.

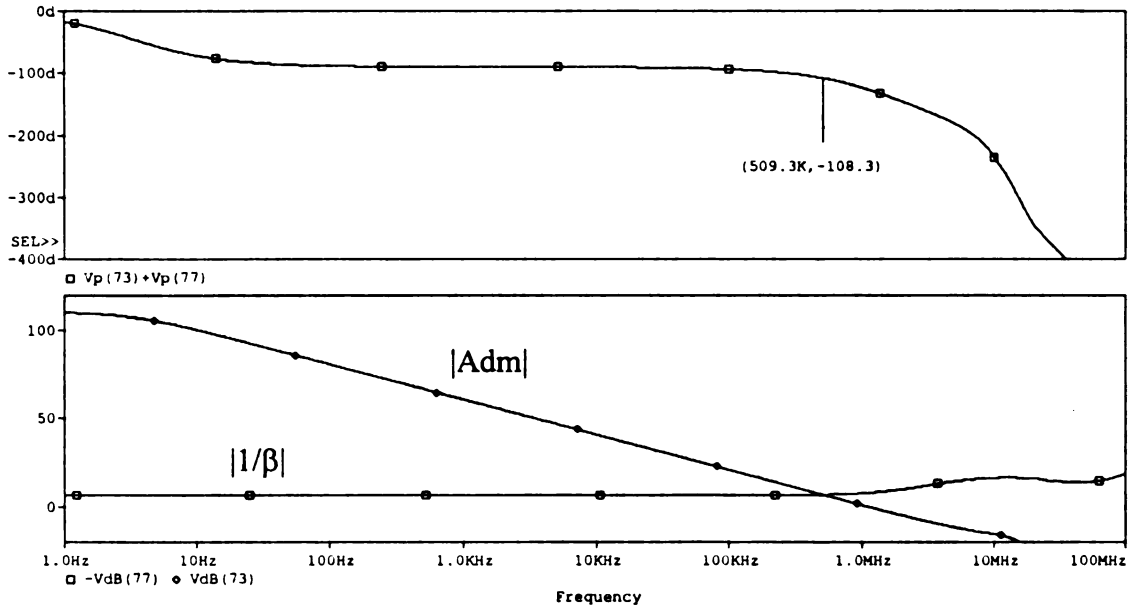


Figure 7.5.3.4: Graph of Beta Network Analysis with V_{BIAS} = 6.133 volts

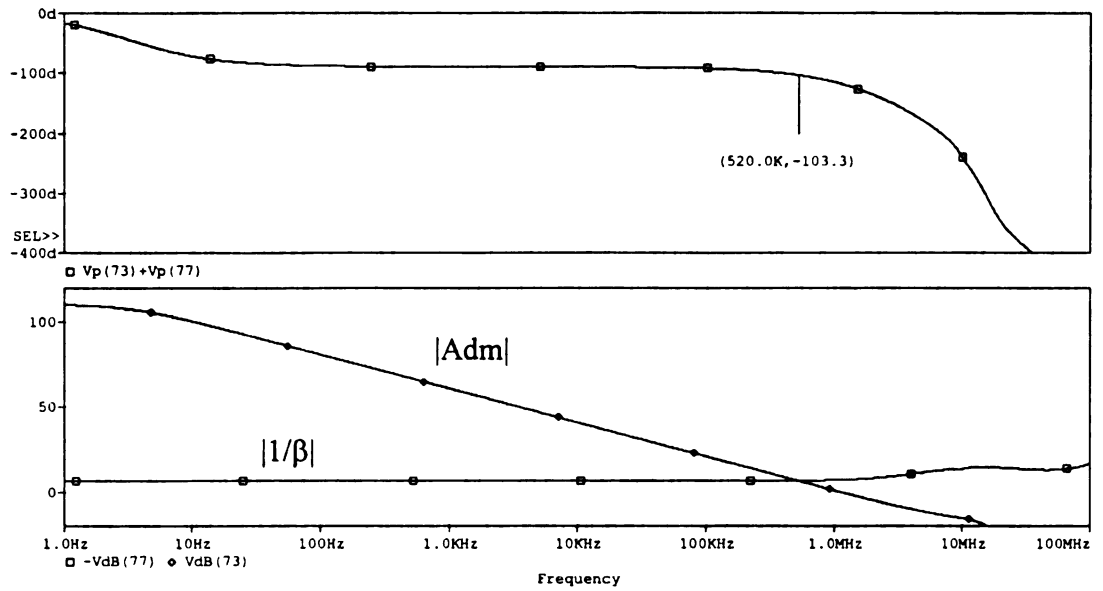


Figure 7.5.3.5: Graph of Beta Network Analysis with V_{BIAS} = -6.232 volts

7.5.4 Verifying with Lab Data

The Addition of R_{ADD} and C_{ADD} were tested in the lab. The circuit in the lab produced exactly the same results that were achieved when the bypass capacitor was added (See Figure 5.3.1.5). Therefore, it can be concluded that one way to help eliminate stability problems for this Class G amplifier design is to include R_{ADD} and C_{ADD}.

Chapter 8: Efficiency and Total Harmonic Distortion

8.1 Introduction

The reason for the Class G amplifier is to have a power amplifier that will be more efficient than the Class B amplifier without sacrificing sound quality. With a more efficient circuit, the overall circuit temperature would be cooler and would use smaller heat sinks. More importantly, though, if the circuit were using portable power supplies (batteries), the life of the battery would be extended. This chapter will examine the efficiency of the amplifier and measure the Total Harmonic Distortion using PSpice.

8.2 PSpice Simulations

The Class G amplifier circuit was tested using a voltage ratio for V_1 to V_2 of 1:3. This is suggested to be the best result for music production [4]. In this case, V_1 equals 6 volts and V_2 equals 18 volts. The efficiency of the Class G amplifier can be measured by dividing the average power of the load by the average power of the power supplies.

$$\text{Efficiency} = \frac{\text{AVG}(V_{RL} * I_{RL})}{\text{AVG}(V_1 * I_{V1}) + \text{AVG}(V_{1'} * I_{V1'}) + \text{AVG}(V_2 * I_{V2}) + \text{AVG}(V_{2'} * I_{V2'})}$$

To compare the efficiency of the Class G amplifier to the Class B amplifier, a Class B amplifier circuit was modeled shown in Figure 8.2.1. This Class B circuit uses an Op-Amp and an additional Class B stage because the Op-Amp cannot provide enough current for the voltage swing required. Also note that the Class B amplifier can have a

voltage swing that is closer to the power rails than the Class G amplifier. However, only the full voltage range of the Class G amplifier was used to test the efficiency of the Class B design. The power supplies were at +/- 18 volts but the output voltage range was from 0 to +/- 13.7 volts. The efficiency of the Class B amplifier will continue to increase a little more as the input voltage increases before clipping begins. The graph of the efficiency is shown in Figure 8.2.2. This graph does show that the efficiency of the Class G amplifier is better than the Class B amplifier when the signal is smaller than the lower power supplies. The efficiency equations for the Class B amplifier are:

$$\text{Efficiency} = \frac{AVG(V_{ROUT} * I_{ROUT})}{AVG(V_{HIGH} * I_{V(HIGH)}) + AVG(V_{LOW} * I_{V(LOW)})}$$

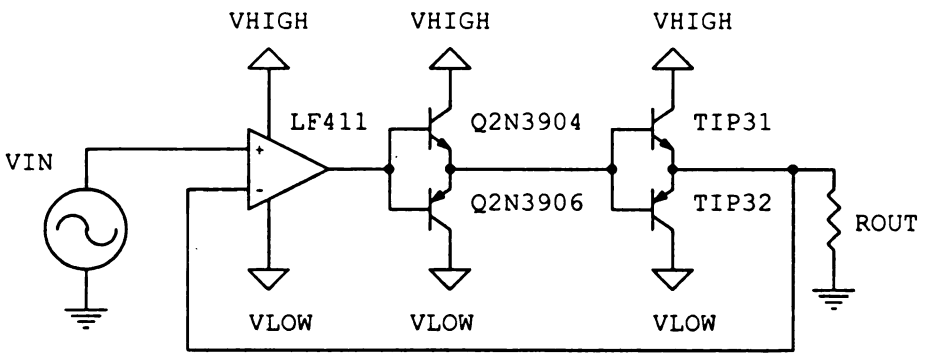


Figure 8.2.1: Schematic of Class B - efficiency testing

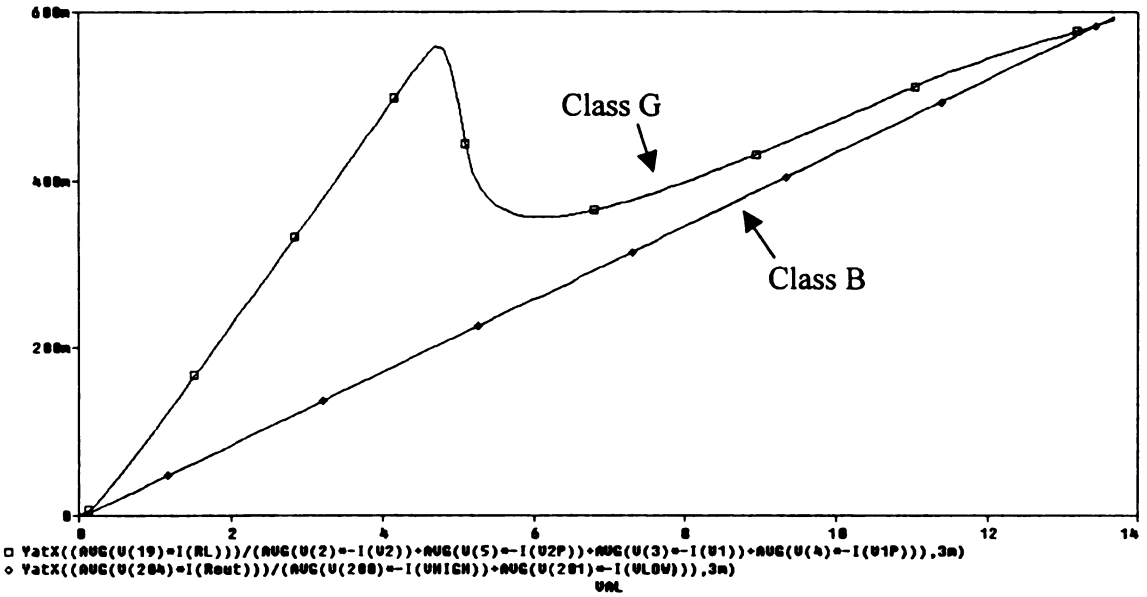


Figure 8.2.2: Graph of Class G verses Class B efficiency

The graph of the efficiency for the Class G amplifier is comparable to the articles referenced in this thesis.

8.3 Lab Data

The Class G amplifier and the Class B amplifier were built in the lab. The Class G amplifier used +/- 15 volt and +/- 5 volt power supplies. The Class B amplifier used +/- 15 volt power supplies. Both amplifiers were tested using a 1kHz input sine wave. The magnitude of the input was incrementally increased from 0 until the output began to clip. The efficiency of the Class B amplifier for different voltage output levels is shown in Table 8.3.1. This table shows the output voltage level and the current from each of the power supplies. The table also shows a calculation for the average power out, the average power in, and the average efficiency. Table 8.3.2 shows the results of testing the Class G amplifier The plot of the efficiencies for both amplifiers is shown in Figure

8.3.1. Notice that the Class G amplifier does show and improved efficiency over the Class B amplifier. This result is similar to the efficiency measure by PSpice.

Voltage (peak-to-peak) Across 10Ω Load	Measured Average Current from Power Supply (mA)		Average Power (W)		Power Efficiency
	+15 Volt	-15 Volt	Power Out	Power In	
0.43	8.5	9.4	0.0023	0.2685	0.86%
0.799	13.2	14	0.0080	0.4080	1.96%
1.186	25	20	0.0176	0.6750	2.60%
1.606	32	29	0.0322	0.9150	3.52%
1.981	37	35	0.0491	1.0800	4.54%
2.378	40	40	0.0707	1.2000	5.89%
2.755	49	47	0.0949	1.4400	6.59%
3.147	57	50	0.1238	1.6050	7.71%
3.533	61	60	0.1560	1.8150	8.60%
3.928	68	68	0.1929	2.0400	9.45%
4.33	78	72	0.2344	2.2500	10.42%
4.7	82	83	0.2761	2.4750	11.16%
5.16	85	89	0.3328	2.6100	12.75%
5.54	59	93	0.3836	2.2800	16.83%
5.9	98	96	0.4351	2.9100	14.95%
6.29	100	100	0.4946	3.0000	16.49%
6.65	110	110	0.5528	3.3000	16.75%
7.07	115	115	0.6248	3.4500	18.11%
7.43	119	120	0.6901	3.5850	19.25%
7.82	120	125	0.7644	3.6750	20.80%
8.44	130	130	0.8904	3.9000	22.83%
8.75	140	140	0.9570	4.2000	22.79%
9.12	140	140	1.0397	4.2000	24.75%
9.62	150	150	1.1568	4.5000	25.71%
10.05	160	160	1.2625	4.8000	26.30%
10.36	160	160	1.3416	4.8000	27.95%
10.73	170	170	1.4392	5.1000	28.22%
11.25	180	180	1.5820	5.4000	29.30%
11.65	180	180	1.6965	5.4000	31.42%
11.97	190	190	1.7910	5.7000	31.42%
12.35	200	200	1.9065	6.0000	31.78%
12.79	200	200	2.0448	6.0000	34.08%
13.17	210	210	2.1681	6.3000	34.41%
13.49	210	210	2.2748	6.3000	36.11%
14.42	230	230	2.5992	6.9000	37.67%
15.18	240	240	2.8804	7.2000	40.01%
16.15	250	250	3.2603	7.5000	43.47%
16.8	270	270	3.5280	8.1000	43.56%
17.68	280	280	3.9073	8.4000	46.52%
18.43	290	290	4.2458	8.7000	48.80%
19.23	300	300	4.6224	9.0000	51.36%
19.83	310	310	4.9154	9.3000	52.85%
20.83	330	330	5.4236	9.9000	54.78%
21.61	330	340	5.8374	10.0500	58.08%
21.93	340	350	6.0116	10.3500	58.08%

Table 8.3.1: Measure Class B efficiency

Voltage (peak-to-peak) Across 10Ω Load	Measured Average Current from Power Supply (mA)				Average Power (W)		Power Efficiency
	+5 Volt	-5 Volt	+15 Volt	-15 Volt	Power Out	Power In	
0.602	8	7	4.3	4.3	0.0045	0.1690	2.68%
0.819	10	10	4.32	4.32	0.0084	0.1796	4.67%
0.968	15	15	4.36	4.36	0.0117	0.2058	5.69%
1.157	19	19	4.4	4.4	0.0167	0.2270	7.37%
1.354	20	20	4.43	4.43	0.0229	0.2329	9.84%
1.544	21	23	4.5	4.5	0.0298	0.2400	12.41%
1.68	25	25	4.54	4.54	0.0353	0.2612	13.50%
1.871	27	27	4.6	4.6	0.0438	0.2730	16.03%
2.062	30	30	4.71	4.71	0.0531	0.2914	18.24%
2.262	32	33	4.72	4.72	0.0640	0.3017	21.20%
2.468	38	38	4.76	4.76	0.0761	0.3329	22.87%
2.629	39	39	4.8	4.8	0.0864	0.3391	25.48%
2.825	40	40	4.85	4.85	0.0998	0.3456	28.87%
3.028	42	42	4.9	4.9	0.1146	0.3571	32.10%
3.171	43	43	4.96	4.96	0.1257	0.3639	34.54%
3.333	50	50	5	5	0.1389	0.4001	34.71%
3.581	52	53	5.03	5.03	0.1603	0.4110	39.00%
3.722	56	56	5.08	5.08	0.1732	0.4325	40.04%
4.01	59	59	5.12	5.12	0.2010	0.4487	44.80%
4.19	60	60	5.18	5.18	0.2195	0.4555	48.18%
4.34	62	62	5.21	5.21	0.2354	0.4664	50.48%
4.52	66	66	5.25	5.25	0.2554	0.4876	52.37%
4.71	70	71	5.38	5.38	0.2773	0.5115	54.21%
4.86	75	75	5.4	5.4	0.2952	0.5371	54.97%
5.01	78	78	5.45	5.45	0.3138	0.5536	56.67%
5.28	80	80	5.5	5.5	0.3485	0.5651	61.66%
5.43	82	82	5.56	5.56	0.3686	0.5769	63.88%
5.58	83	83	5.64	5.64	0.3892	0.5844	66.60%
5.75	88	88	5.71	5.71	0.4133	0.6115	67.59%
5.9	91	91	5.79	5.79	0.4351	0.6289	69.19%
6.26	98	99	5.9	5.9	0.4898	0.6672	73.42%
6.67	100	100	5.9	5.9	0.5561	0.6772	82.12%
6.98	103	104	6.22	6.22	0.6090	0.7018	86.78%
7.45	110	112	6.68	6.68	0.6938	0.7506	92.43%
7.74	120	119	7.4	7.4	0.7488	0.8222	91.08%
8.17	117	117	22	22	0.8344	1.2452	67.01%
8.34	105	105	30	30	0.8694	1.4252	61.01%
8.53	98	100	35	40	0.9095	1.6152	56.31%
8.65	90	91	40	50	0.9353	1.8002	51.96%
8.88	80	82	50	60	0.9857	2.0501	48.08%
9.19	78	79	60	70	1.0557	2.3401	45.11%
9.55	69	70	80	80	1.1400	2.7451	41.53%
9.9	60	60	80	90	1.2251	2.8501	42.99%
10.33	60	60	100	100	1.3339	3.3001	40.42%
10.65	58	59	100	110	1.4178	3.4401	41.21%
11.03	52	50	110	120	1.5208	3.7101	40.99%
11.34	49	50	120	130	1.6074	3.9951	40.24%
11.75	45	45	130	140	1.7258	4.2751	40.37%
12.08	42	42	140	150	1.8241	4.5601	40.00%
12.5	41	41	140	150	1.9531	4.5551	42.88%

12.84	40	40	150	160	2.0608	4.8501	42.49%
13.27	40	40	160	170	2.2012	5.1501	42.74%
13.55	39	39	170	180	2.2950	5.4451	42.15%
13.96	39	39	170	190	2.4360	5.5951	43.54%
14.25	39	39	180	190	2.5383	5.7451	44.18%
14.64	39	39	190	200	2.6791	6.0451	44.32%
14.97	38	38	190	200	2.8013	6.0401	46.38%
15.34	38	38	210	210	2.9414	6.4901	45.32%
15.85	38	38	220	220	3.1403	6.7901	46.25%
16.21	32	32	230	230	3.2846	7.0601	46.52%
16.6	31	31	230	230	3.4445	7.0551	48.82%
16.97	30	30	240	240	3.5998	7.3501	48.98%
17.23	30	30	250	250	3.7109	7.6501	48.51%
17.65	28	28	250	250	3.8940	7.6401	50.97%
17.88	28	28	260	260	3.9962	7.9401	50.33%
18.34	25	25	260	260	4.2044	7.9250	53.05%
18.69	25	25	270	270	4.3665	8.2250	53.09%
19.09	24	24	280	280	4.5554	8.5200	53.47%
19.28	23	23	280	280	4.6465	8.5150	54.57%
19.54	23	23	290	290	4.7726	8.8150	54.14%
20.28	22	22	300	300	5.1410	9.1100	56.43%
20.59	22	22	310	310	5.2994	9.4100	56.32%
20.92	20	20	310	310	5.4706	9.4000	58.20%

Table 8.3.2: Measuring Class G efficiency

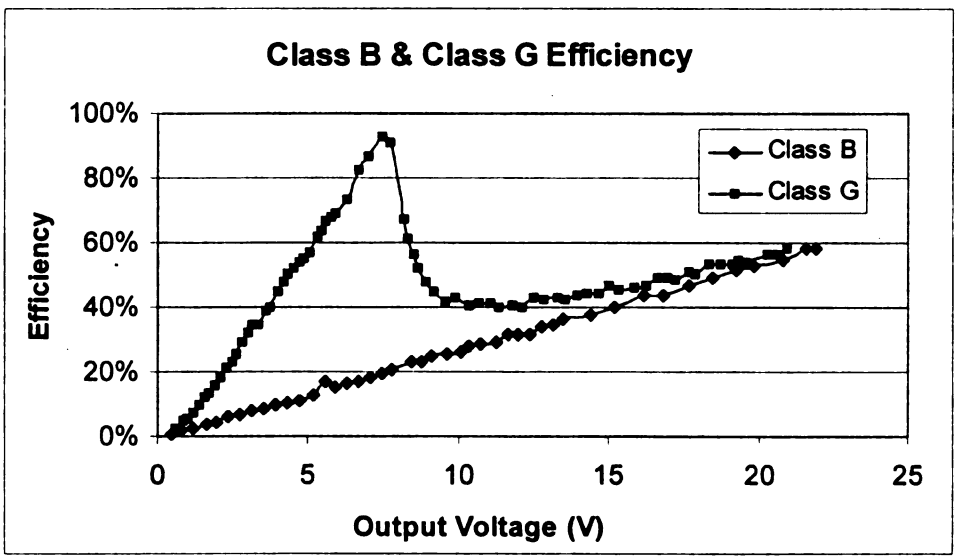


Figure 8.3.1: Graph of Class B and Class G efficiency - lab data

8.4 Total Harmonic Distortion

The Total Harmonic distortion of the final circuit, including the added resistors and capacitors, was analyzed using a LF411 for the operational amplifier. This test circuit, however, did not include the inductors of the power lines. The measurement was taken at 1kHz, 10 kHz, and 20 kHz at maximum output voltage (without clipping). This test used a 10 Ω resistor for the load. Using PSpice to analyze the first 20 harmonics, the THD at 1 kHz, 10 kHz, and 20 kHz was 0.0184%, 0.174%, and 0.354% respectfully. It is generally believed in hobbyist magazines that a total harmonic distortion of less than 1% is considered inaudible. The data can be found in Appendix F.

8.5 Efficiency for Audio

The Class G amplifier has been shown to be more efficient than the Class B amplifier when the input signals are relatively small compared to the power supplies. This can be beneficial for audio circuits where the input is spending more time at lower voltages than it is at high voltages. Studies show that under music listening conditions, an audio amplifier is called upon to deliver full or nearly full output for only a small fraction of the time it is operating [8]. One way to analyze this is by using the crest factor (the ratio of peak level to rms level) [7] [8]. Symphonic music, for example, has a high crest factor compared to popular music because the volume of symphonic music is always changing from long periods of soft to long periods of loud. Speech has a crest factor that is between popular music and symphonic music. With speech, though, people rarely speak at full volume. This means that a Class G amplifier would work for audio devices involving speech, like cell phones and walkie-talkies. Since the majority of the

time the volume would be medium to low, the efficiency of the Class G amplifier would become even better because the circuit would be spending more time in the area where the circuit is more efficient.

9 Design Improvements

9.1 Introduction

This chapter offers some improvements to the basic Class G amplifier design to increase efficiency and lower the total harmonic distortion. By analyzing the basic design of the Class G amplifier and by using bipolar-junction transistors (BJTs) to get the general equations that describe the basic behavior of the Class G amplifier, more advanced designs could be created. Many Class G amplifier designs may have been overlooked in the past due to the stability problem. By using the Beta Network Analysis method describe in this thesis, it is possible to identify the source of some stability problems.

9.2 Using Better Op-Amp to Lower THD

Using an Op-Amp with high bandwidth and high slew-rate such as the LF411 compared to the UA741 Op-Amp will lower the THD. An Op-Amp with higher bandwidth can switch faster than an Op-Amp with lower bandwidth. The Op-Amp with more bandwidth will reduce the distortion caused by crossover.

An Op-Amp that uses less power will help to improve the efficiency of the circuit for small input signals. This would be more useful in designs that require a Class G amplifier with a low output wattage, such as building the entire Class G amplifier on an integrated circuit chip.

9.3 Using More Biasing to Lower THD

Another improvement for lowering the THD would be to not require the Op-Amp output voltage to jump as much due to crossover. This could be done by adding more biasing (V_{BIAS1} and V_{BIAS2}) to the Class-G output stage shown in Figure 9.3.1. This design is similar to that of the Class AB amplifier. Now, the Op-Amp would only have to correct a small amount of crossover.

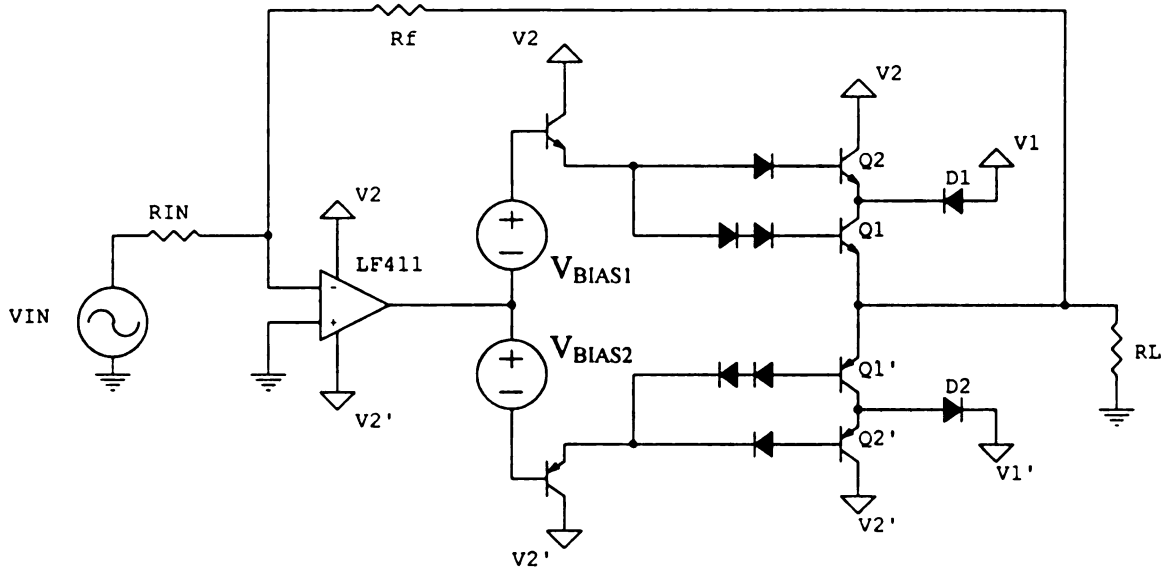


Figure 9.3.1: Schematic model for improved Class G amplifier

A possible circuit that would implement the model shown in Figure 9.3.1 is shown in Figure 9.3.2. This circuit uses diodes to get the proper biasing voltage levels for V_{BIAS1} and V_{BIAS2} and uses Op-Amps to provide the necessary current. The THD was tested at 1 kHz, 10 kHz, and 20 kHz using PSpice to analyze the first 20 harmonics. The measurement was taken at the maximum output voltage without clipping. The THD at 1 kHz, 10 kHz, and 20 kHz was 0.0147%, 0.134%, and 0.279% respectively. Figure 9.3.3

shows the output of this circuit at maximum voltage (13.7 volts) at 20 kHz with very small amounts of visible distortion. The efficiency of this circuit is shown in Figure 9.3.4. This new circuit would need more components and the efficiency would be less for a trade off of lower THD.

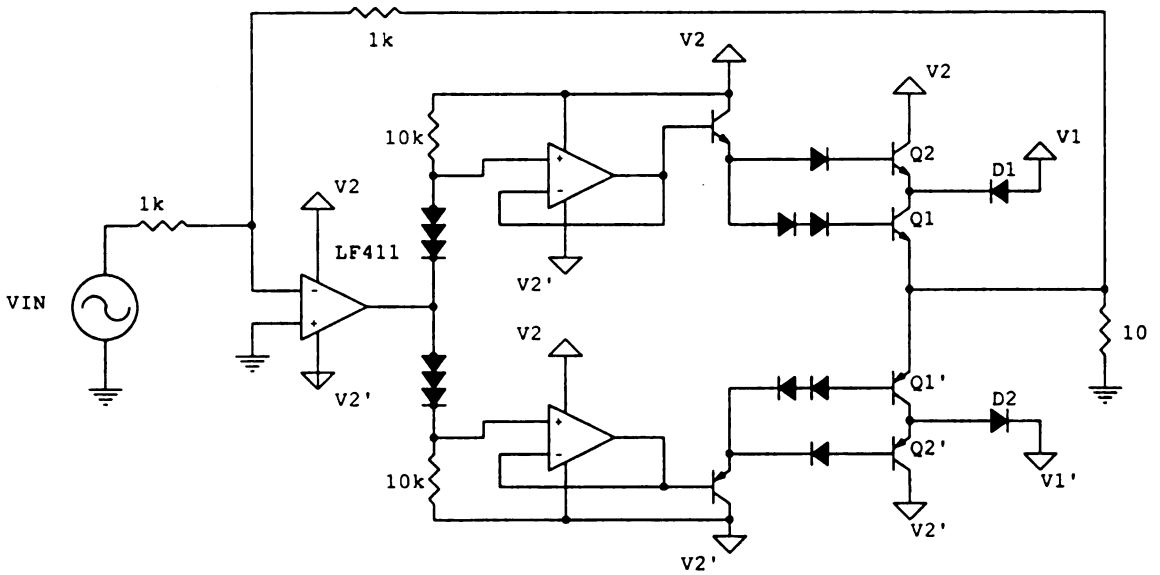


Figure 9.3.2: Schematic of Class G with more biasing

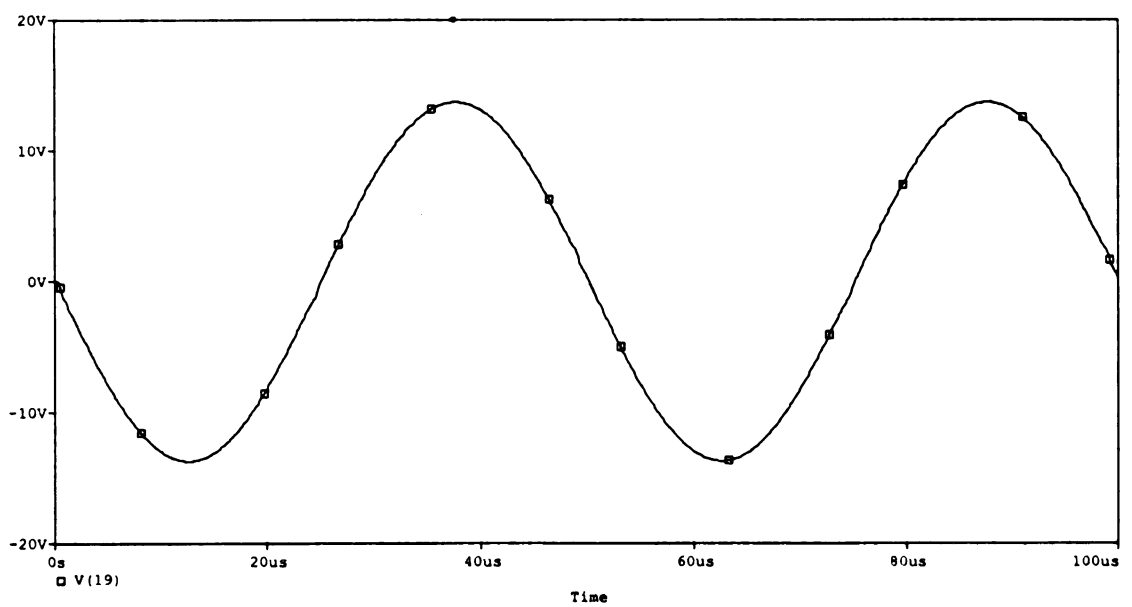


Figure 9.3.3: Graph of V_{OUT} (MAX) at 20 kHz

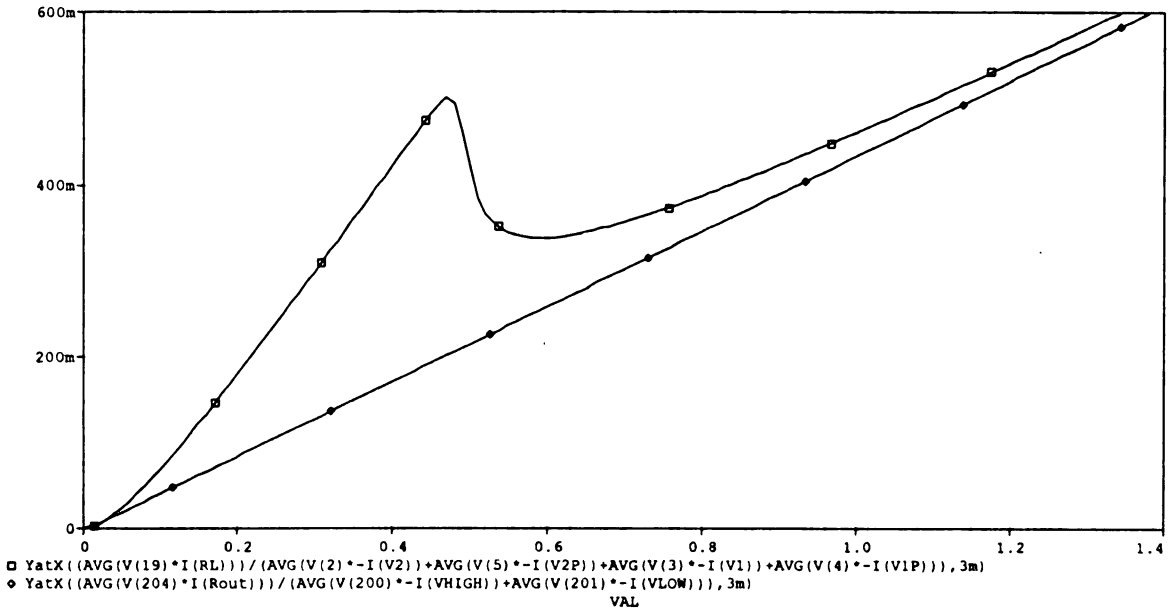


Figure 9.3.4: Efficiency of Class G with more biasing and Class B amplifier

Chapter 10: Future Study

10.1 Introduction

There may be a way to identify stability problems with Op-Amp circuits using a closed-loop approach and PSpice. By having a closed-loop approach, circuits could be quickly analyzed for verification of stability problems. This chapter will use common Op-Amp circuits such as inverting and non-inverting amplifiers to show how this identification technique may be applied to circuits with and without stability problems.

10.2 Identifying Stability Problems using Closed-Loop Approach

Here is a proposed technique to find how stable a closed-loop Op-Amp circuit is without needing to replace the Op-Amp with a model and analyzing the beta network.

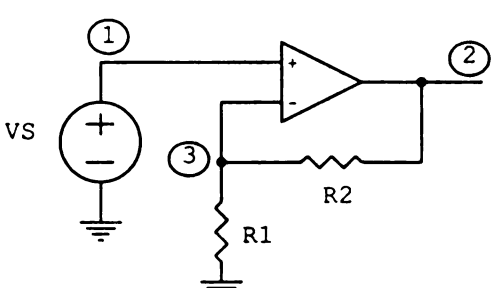


Figure 10.2.1: Schematic of example circuit

A non-inverting amplifier example circuit was used to develop the steps necessary to find the stability of the circuit using different gains shown in Figure 10.2.1. The gain of this circuit is $\left(1+\frac{R2}{R1}\right)$. The Adm of the Op-Amp was chosen to be:

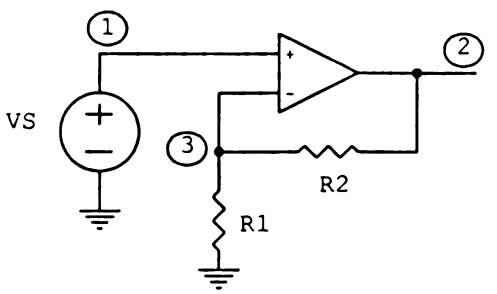
$$100k * \frac{2\pi(10)}{s+2\pi(10)} * \frac{2\pi(10k)}{s+2\pi(10k)} * \frac{2\pi(100k)}{s+2\pi(100k)}$$

10.2.1 Transient Response

First, the circuit was analyzed by stepping the voltage of VS from 0 to 0.5 volts and observing the transient response. The gains tested were 9, 10, 11, and 12. Resistor R1 was 1kΩ and resistor R2 was changed to achieve the desired gains (8kΩ, 9kΩ, 10kΩ, and 11kΩ). Figure 10.2.1.1 shows the PSpice files used to simulate this circuit. Figure 10.2.1.2-A through Figure 10.2.1.2-D show the output of the circuit at node 2. When the gain of the circuit was 9 and 10, the circuit began to oscillate indicating that the circuit is unstable. And, when the gain of the circuit was 11 and 12, the circuit had some ringing in the output but was being dampened indicating that this circuit is marginally stable.

Stability Testing

```
VS 1 0 PULSE (0 .5 10U)
R1 3 0 1K
R2 2 3 8K
X1 1 3 2 OPAMP
.SUBCKT OPAMP 1 2 3
RIN 1 2 100MEG
EADM 3 0 LAPLACE {V(1,2)} {(100K)*(6.28*10)*(6.28*10K)*(6.28*100K)/
+ ((S+6.28*10)*(S+6.28*10K)*(S+6.28*100K))}
.ENDS OPAMP
.TRAN .01U 400U 0 .01U
.PROBE
.END
```




```
Stability Testing
VS 1 0 PULSE (0 .5 10U)
R1 3 0 1K
R2 2 3 9K
X1 1 3 2 OPAMP
.SUBCKT OPAMP 1 2 3
RIN 1 2 100MEG
EADM 3 0 LAPLACE {V(1,2)} {(100K)*(6.28*10)*(6.28*10K)*(6.28*100K)/
+ ((S+6.28*10)*(S+6.28*10K)*(S+6.28*100K))}
.ENDS OPAMP
.TRAN .01U 400U 0 .01U
.PROBE
.END

Stability Testing
VS 1 0 PULSE (0 .5 10U)
R1 3 0 1K
R2 2 3 10K
X1 1 3 2 OPAMP
.SUBCKT OPAMP 1 2 3
RIN 1 2 100MEG
EADM 3 0 LAPLACE {V(1,2)} {(100K)*(6.28*10)*(6.28*10K)*(6.28*100K)/
+ ((S+6.28*10)*(S+6.28*10K)*(S+6.28*100K))}
.ENDS OPAMP
.TRAN .01U 400U 0 .01U
.PROBE
.END

Stability Testing
VS 1 0 PULSE (0 .5 10U)
R1 3 0 1K
R2 2 3 11K
X1 1 3 2 OPAMP
.SUBCKT OPAMP 1 2 3
RIN 1 2 100MEG
EADM 3 0 LAPLACE {V(1,2)} {(100K)*(6.28*10)*(6.28*10K)*(6.28*100K)/
+ ((S+6.28*10)*(S+6.28*10K)*(S+6.28*100K))}
.ENDS OPAMP
.TRAN .01U 400U 0 .01U
.PROBE
.END
```

Figure 10.2.1.1: PSpice files with schematic

$$\frac{1}{\beta} = \left(1 + \frac{8k}{1k}\right) = 9 \quad \textbf{NOT STABLE}$$

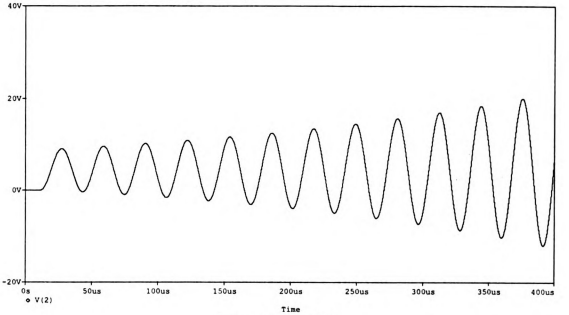


Figure 10.2.1.2-A

$$\frac{1}{\beta} = \left(1 + \frac{9k}{1k}\right) = 10 \quad \textbf{NOT STABLE}$$

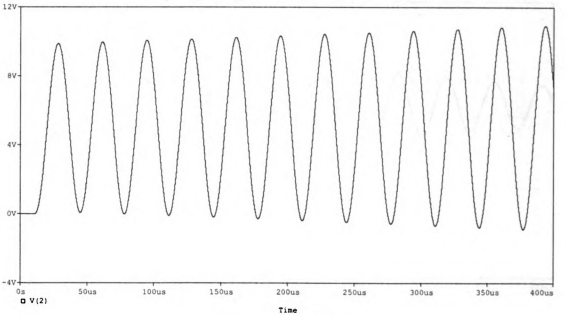


Figure 10.2.1.2-B

$$\frac{1}{\beta} = \left(1 + \frac{10k}{1k}\right) = 11 \textbf{ STABLE}$$

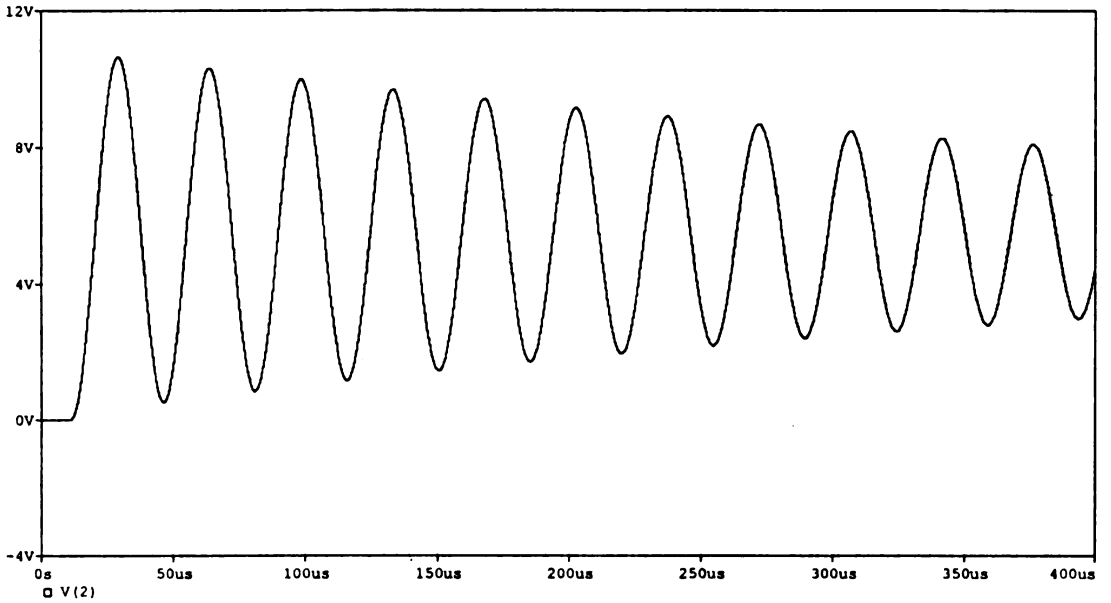


Figure 10.2.1.2-C

$$\frac{1}{\beta} = \left(1 + \frac{11k}{1k}\right) = 12 \textbf{ STABLE}$$

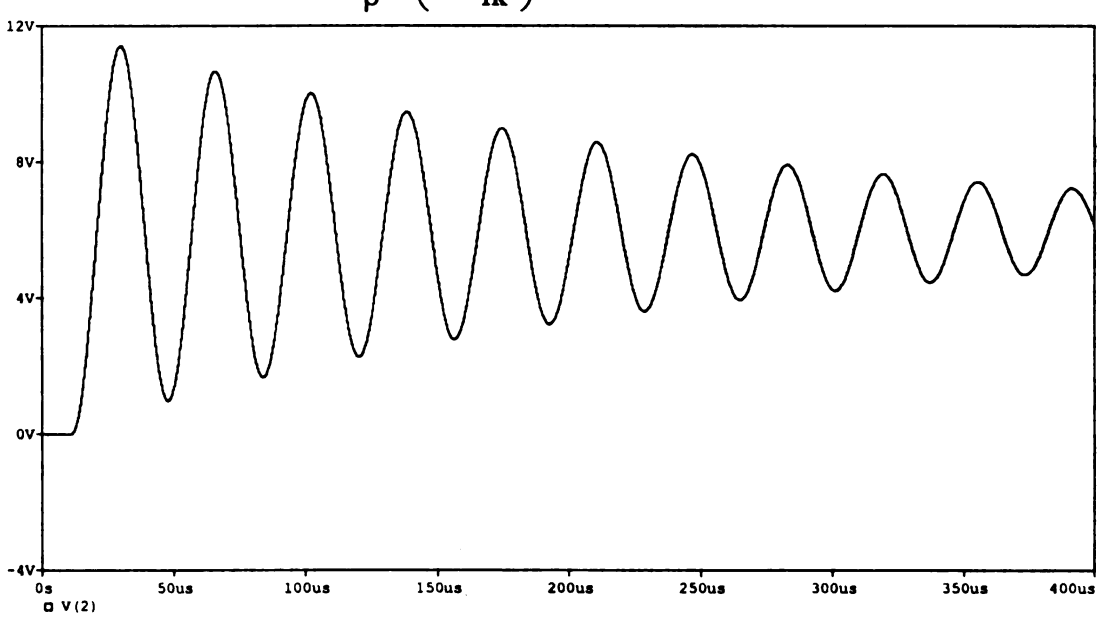


Figure 10.2.1.2-D

Figure 10.2.1.2: PSpice output graphs

10.2.2 AC Frequency Response

The AC analysis was performed on the same circuit. Instead of stepping the voltage of VS, like in the transient analysis, the frequency of voltage VS with amplitude of 1 was swept from 100mHz to 10MHz. Again, the gain of the circuit was changed to be 9, 10, 11, and 12. Figure 10.2.2.1 shows the PSpice file used for simulation. The phase shift due to the Op-Amp can be seen by plotting the difference between the phase of V2 and V(1,3) shown in Figure 10.2.2.2. The phase matches the predicted open-loop phase shift of the Op-Amp. Figure 10.2.2.2 also shows the gain of the Op-Amp by measuring $dB\left(\frac{V(2)}{V(1,3)}\right)$ and the gain at node 3. Upon closer examination of the graph (Figure 10.2.2.3), it is observed that when the gain of node 3 crosses the gain of the Op-Amp with a negative slope, the phase angle will tell the phase margin of the circuit. The phase margin is defined as $PM = 180° - \left|\angle Adm * \beta\right|$.

```
Stability Testing
VS 1 0 AC 1
R1 3 0 1K
R2 2 3 {VAL}
X1 1 3 2 OPAMP
.SUBCKT OPAMP 1 2 3
RIN 1 2 100MEG
EADM 3 0 LAPLACE {V(1,2)}
+ {(100K)*(6.28*10)*(6.28*10K)*(6.28*100K)/
+ ((S+6.28*10)*(S+6.28*10K)*(S+6.28*100K))}
.ENDS OPAMP
.PARAM VAL = 1
.STEP PARAM VAL LIST 8K 9K 10K 11K
.AC DEC 1000 .1 10MEG
.PROBE
.END
```

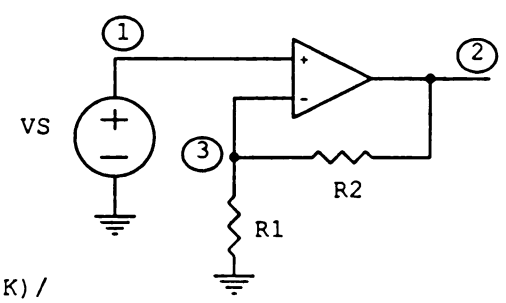


Figure 10.2.2.1: PSpice file with schematic

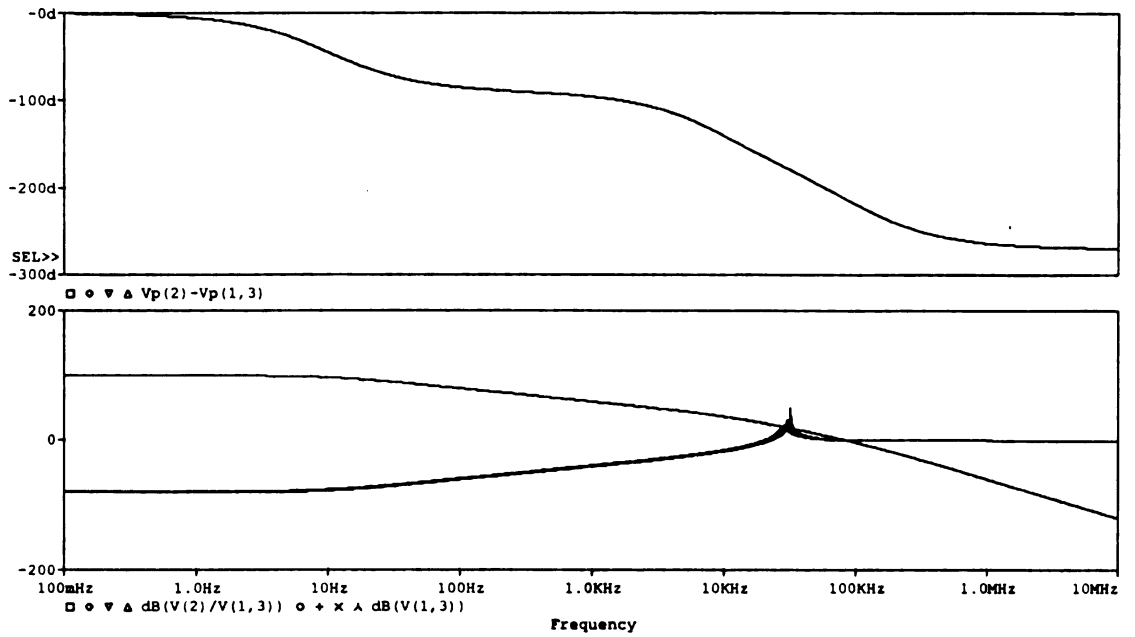


Figure 10.2.2.2: Graph of Beta Network Analysis

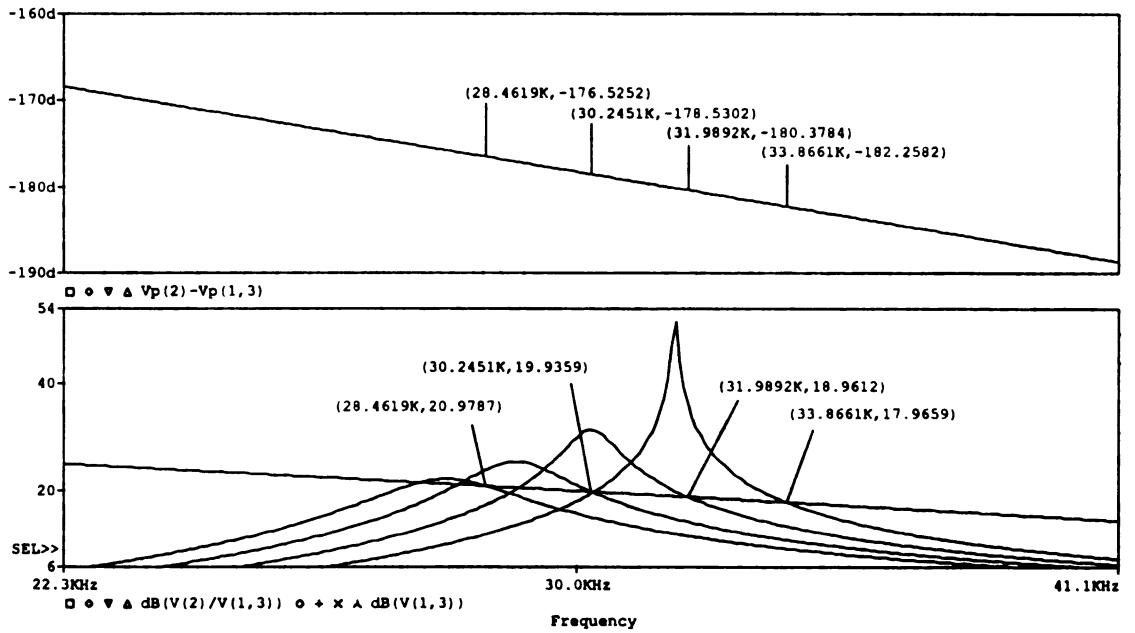


Figure 10.2.2.3: Close up view of Figure 10.2.2.2

The phase margin, according to the graph (Figure 10.2.2.3) of the different gains, are as follows:

$$\text{Gain} = 9 \Rightarrow \text{PM} = 180^{\circ} - \left|-182.26^{\circ}\right| = -2.26^{\circ}$$

$$\text{Gain} = 10 \Rightarrow \text{PM} = 180^{\circ} - \left|-180.37^{\circ}\right| = -0.37^{\circ}$$

$$\text{Gain} = 11 \Rightarrow \text{PM} = 180^{\circ} - \left|-178.53^{\circ}\right| = 1.47^{\circ}$$

$$\text{Gain} = 12 \Rightarrow \text{PM} = 180^{\circ} - \left|-176.53^{\circ}\right| = 3.47^{\circ}$$

When the phase margin is between 0° and 45°, the circuit is said to be marginally stable. When the phase margin is less than 0°, the circuit is said to be unstable and will oscillate. The phase margin, when the gain of the beta network is 9 and 10, shows that the circuit will be unstable. The phase margin, when the gain is 11 and 12 shows that the circuit will be stable but will have ringing in the output.

The following would be a procedure for analyzing a closed-loop Op-Amp circuit and finding the phase margin:

Step 1. Plot the difference in phase angle between the phase of the output and the phase across the input terminals of the Op-Amp.

Step 2. Plot the gain of the Op-Amp by finding the difference between the gain of the output and the gain of the voltage across the input terminals of the Op-Amp.

Step 3. Plot the gain of the voltage across the input terminals of the Op-Amp.

Step 4. Check to see if the gain of the voltage across the Op-Amp crosses the gain of the Op-Amp.

A. If it does, check to see if the gain of the input terminals crosses the gain with a negative slope.

   i. If it does, use the phase plot at this frequency to measure the PM.

   ii. If it does not, find where the gain of the input terminals is maximum. Use the phase plot at this frequency to measure the PM. (See Figure 10.2.2.4)

B. If it does not, find where the gain of the input terminals is at it's maximum value. Use the phase plot at this frequency to measure the PM. (See Figure 10.2.2.5)

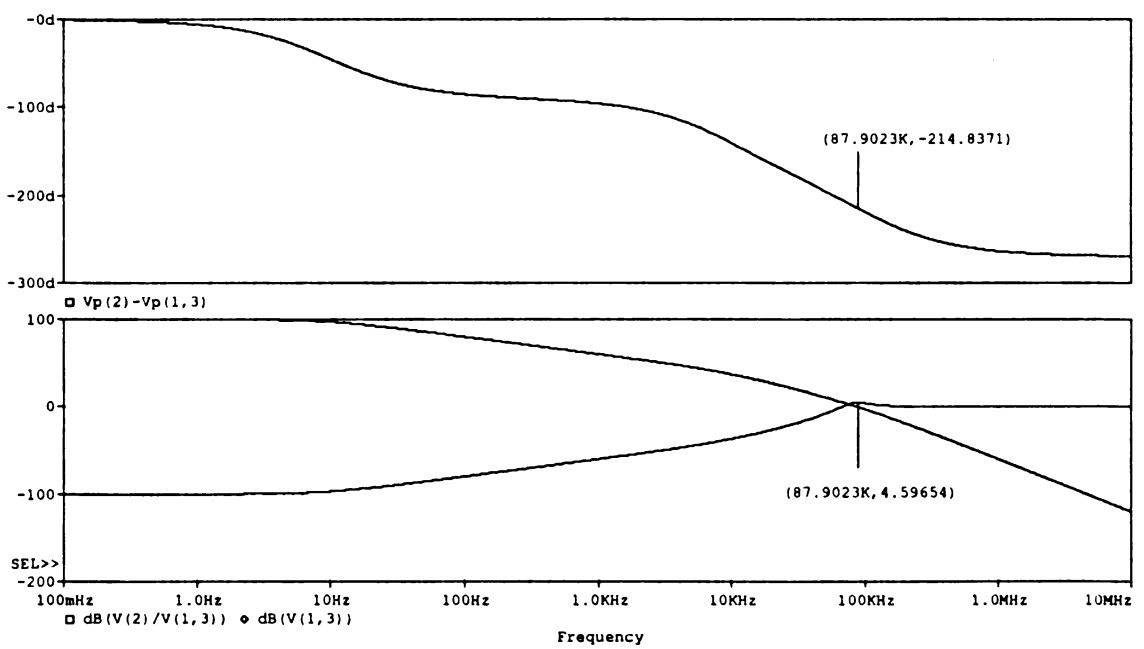


Figure 10.2.2.4: Graph of Beta Network Analysis, Gain = 1

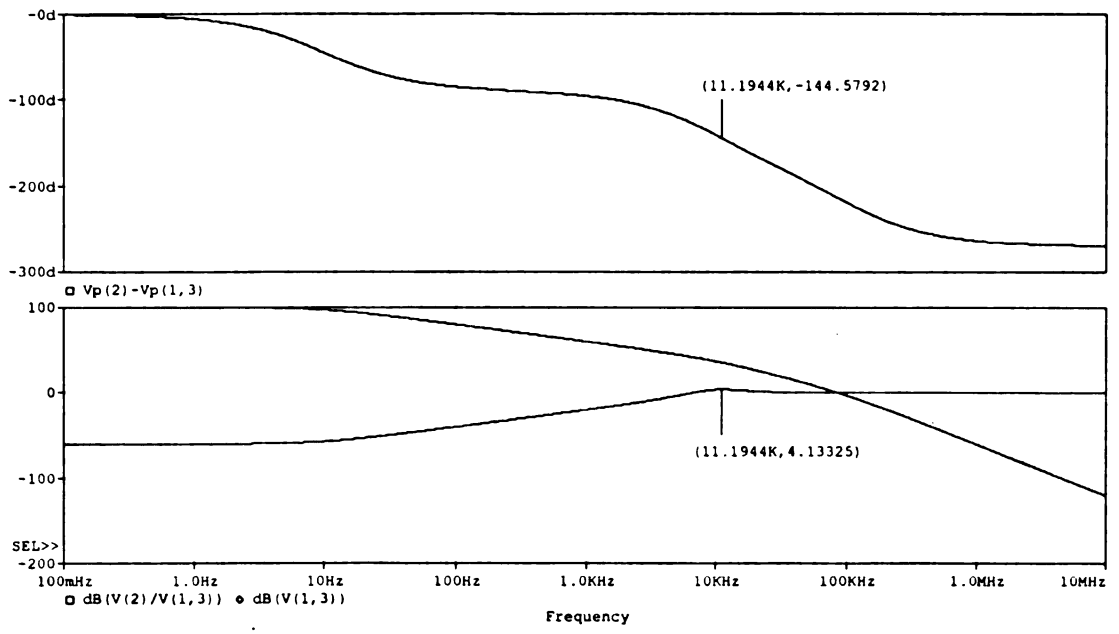


Figure 10.2.2.5: Graph of Beta Network Analysis, Gain = 100

10.2.3 Another Test Using an Inverting Amplifier Design

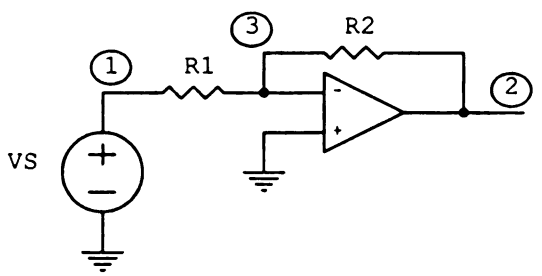
The same Op-Amp is used in this circuit but now the layout is an inverting amplifier (Figure 10.2.3.1). The results of the inverting amplifier slightly differ from the non-inverting amplifier circuit. Figure 10.2.3.2 shows the transient response of the circuit with a gain of 8, 9, 10, and 11. A gain of 10 for the non-inverting circuit was unstable, but a gain of 10 for the inverting circuit was stable. Figure 10.2.3.3 shows the phase and gain of the Op-Amp along with the plot of gain of V(3). Figure 10.2.3.4 shows a closer view of Figure 10.2.3.3 with the measurements to find the phase margin. Figure 10.2.3.5 and Figure 10.2.3.6 show more examples of measuring the PM when the circuit has a gain of 100 and a gain of 1, respectively. The PM for the different gains can be seen below.

Gain = 8 $\Rightarrow$ PM = -1.97^{o}

Gain = 9 $\Rightarrow$ PM = -0.14^{o}

Gain = 10 $\Rightarrow$ PM = 1.69^{o}

Gain = 11 $\Rightarrow$ PM = 3.87^{o}




```
Stability Testing
VS 1 0 AC 1
R1 1 3 1K
R2 3 2 {VAL}
X1 0 3 2 OPAMP
.SUBCKT OPAMP 1 2 3
RIN 1 2 100MEG
EADM 3 0 LAPLACE {V(1,2)}
+ {(100K)*(6.28*10)*(6.28*10K)*(6.28*100K)/
+ ((S+6.28*10)*(S+6.28*10K)*(S+6.28*100K))}
.ENDS OPAMP
.PARAM VAL = 1
.STEP PARAM VAL LIST 8K 9K 10K 11K
.AC DEC 1000 .1 10MEG
.PROBE
.END
```

Figure 10.2.3.1: PSpice file with schematic using inverting amplifier

$$\frac{1}{\beta} = \left(\frac{8k}{1k}\right) = 8$$ **NOT STABLE**

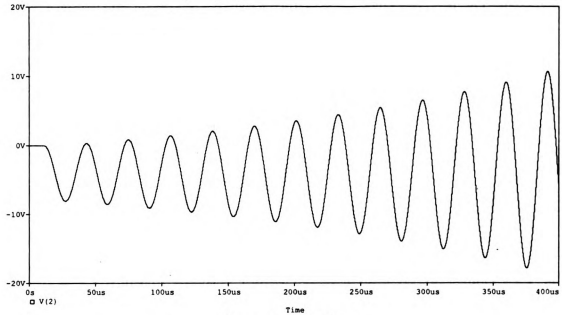


Figure 10.2.3.2-A

$$\frac{1}{\beta} = \left(\frac{9k}{1k}\right) = 9$$ **NOT STABLE**

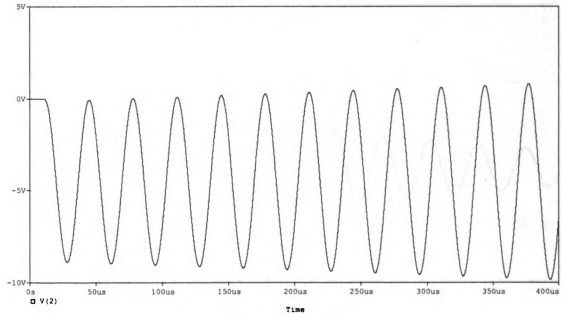


Figure 10.2.3.2-B

$$\frac{1}{\beta} = \left(\frac{10k}{1k}\right) = 10 \textbf{ STABLE}$$

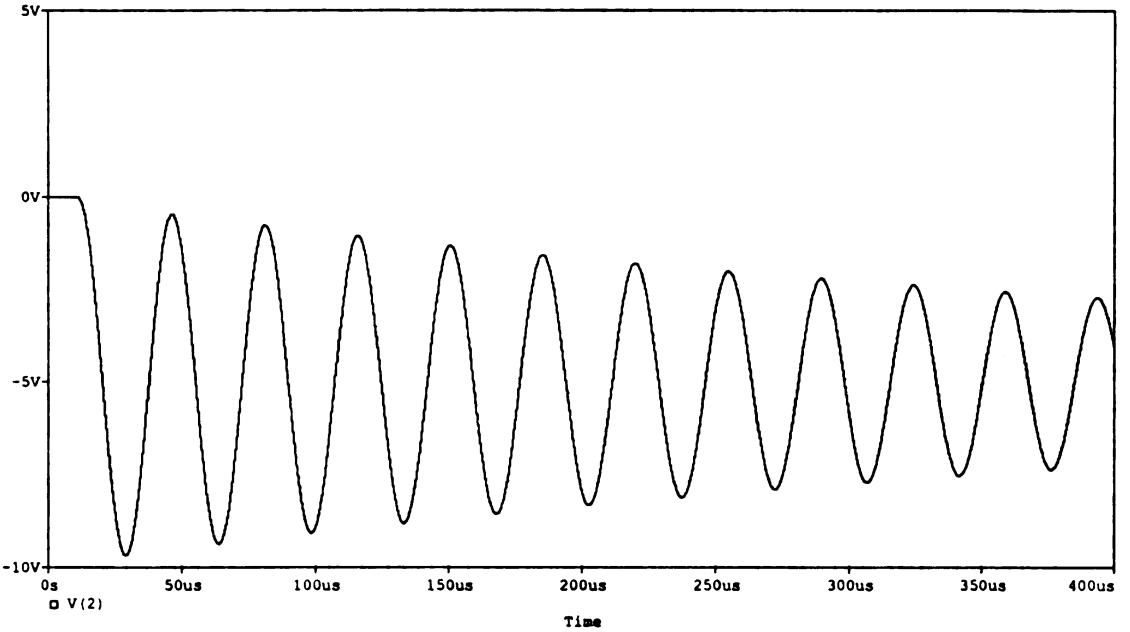


Figure 10.2.3.2-C

$$\frac{1}{\beta} = \left(\frac{11k}{1k}\right) = 11 \textbf{ STABLE}$$

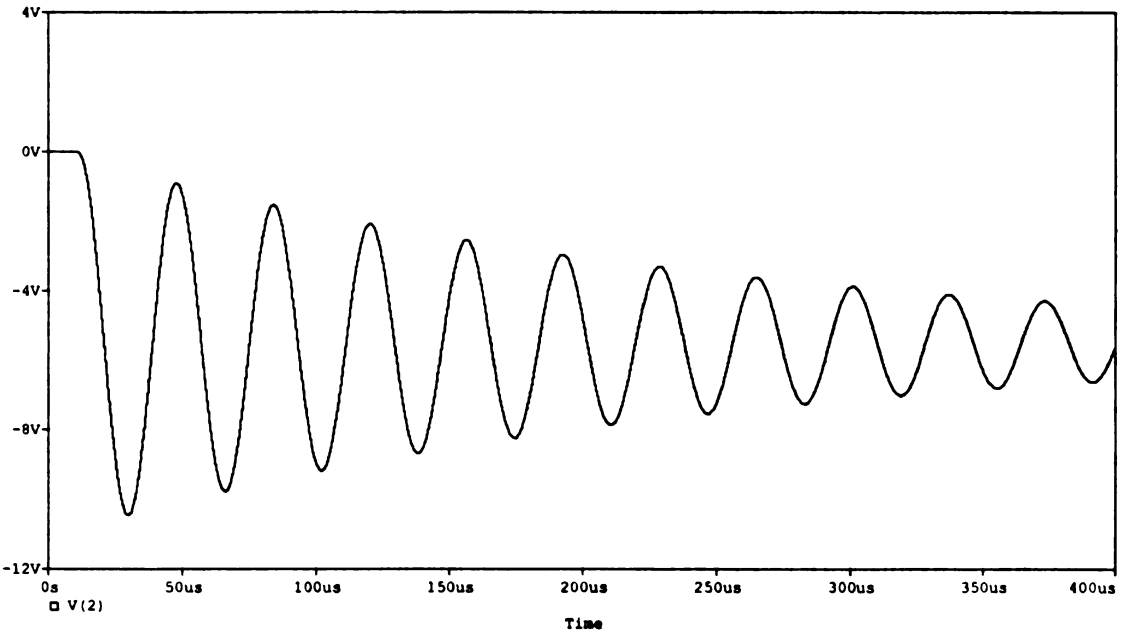


Figure 10.2.3.2-D

Figure 10.2.3.2: PSpice output graphs

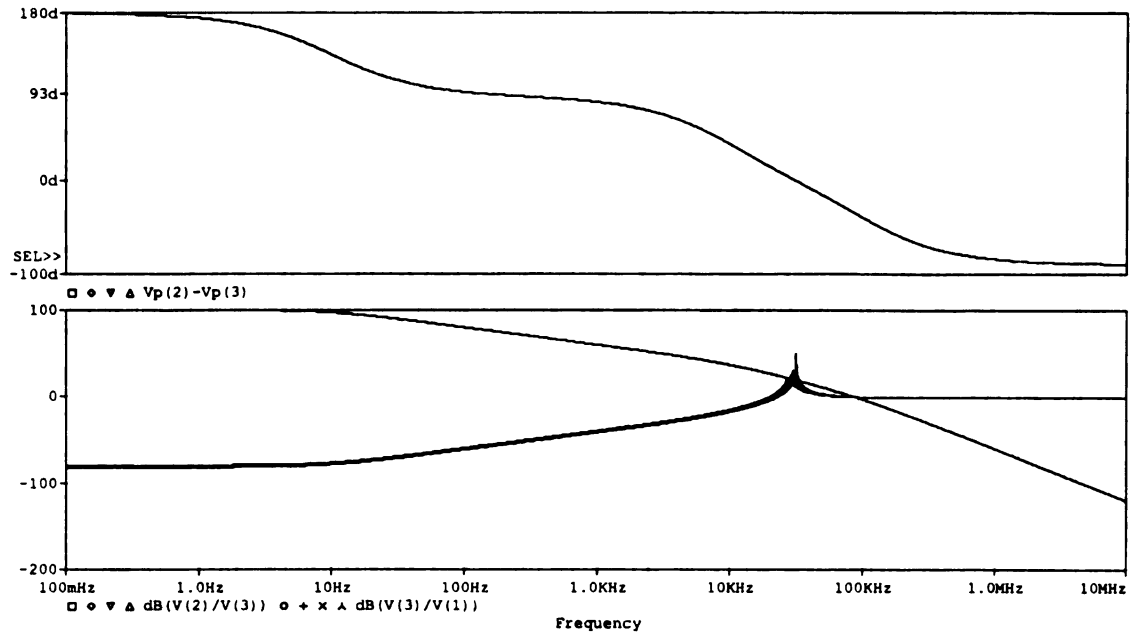


Figure 10.2.3.3: Graph of Beta Network Analysis

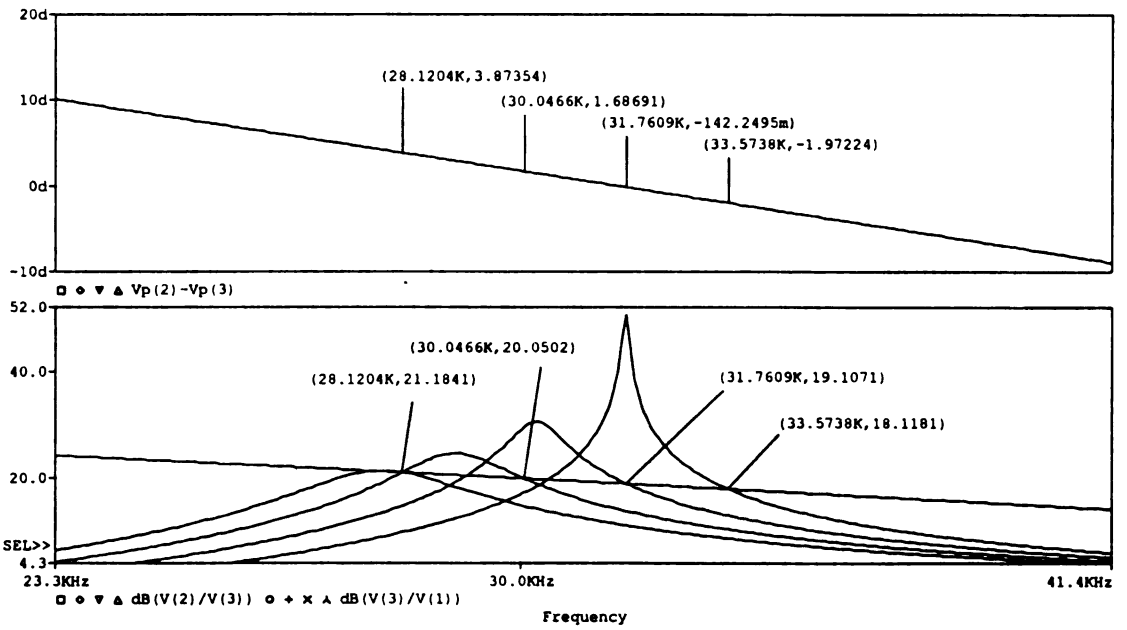


Figure 10.2.3.4: Close up view of Figure 10.2.3.3

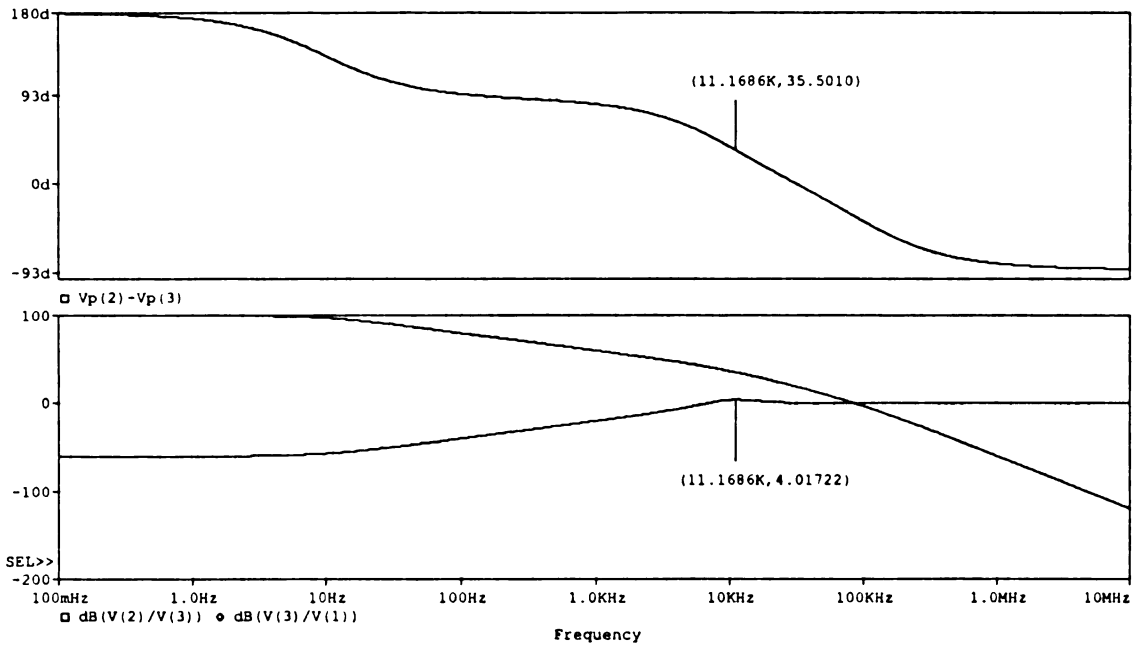


Figure 10.2.3.5: Graph of Beta Network Analysis, Gain = 100

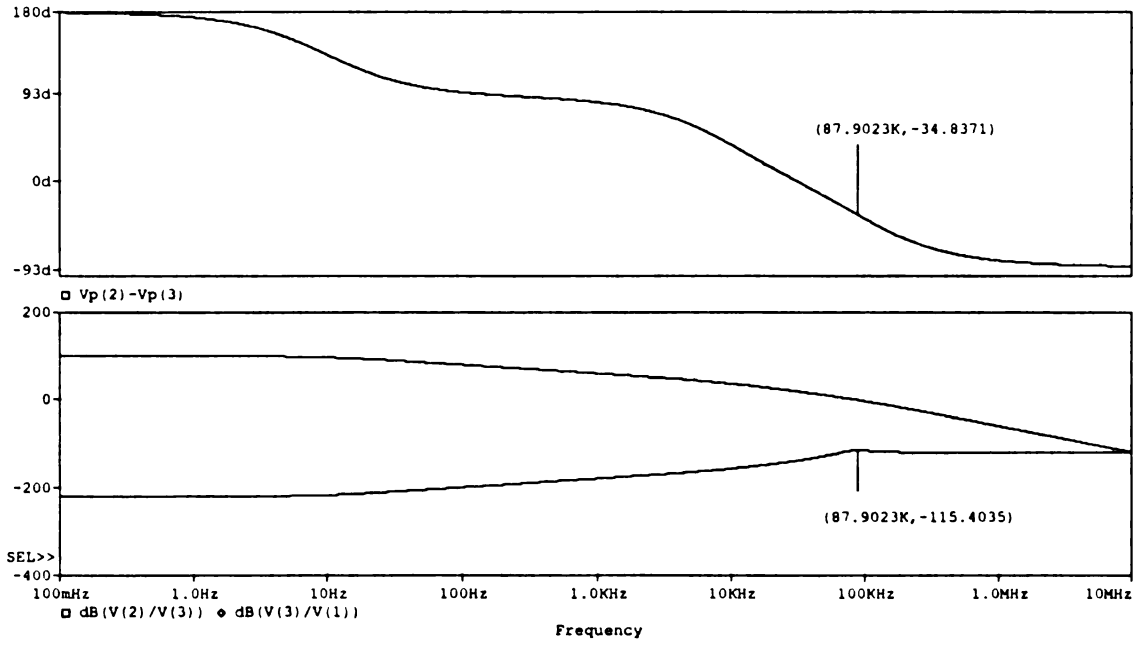


Figure 10.2.3.6: Graph of Beta Network Analysis, Gain = 1

Chapter 11: Conclusion

This thesis has shown the basic design of a Class G amplifier, using bipolar junction transistors, with the help of circuit modeling and equations to get the desired performance with the fewest number of parts. Using this design, an operational amplifier with feedback was used to lower the Total Harmonic Distortion. Data collected from the lab of the Class G amplifier with the Op-Amp showed an output that was only partially unstable.

This stability problem caused concern in the performance of the Class G amplifier and needed to be solved before further analyzing this amplifier. Before any methods could be used to identify the source of the problem, the simulated circuit model had to be revised to match the data collected in the lab. This was done by making sure the Op-Amp was fully modeled and by including wiring inductances that may be coming from the power supply wires. Once the Class G amplifier was properly modeled, the cause of the stability problem was identified using a variation on the Beta Network Analysis Method. This involved using a small signal input and changing the input biasing level because the output was only unstable at certain levels. With the help of Sspice, a mathematically proven solution to the problem was found and experimentally confirmed to work.

While studying the stability problem of the Class G amplifier, a proposed technique for identifying if a circuit would be stable or not using a closed-loop analysis was given. This technique needs to be further examined but it would allow Op-Amp circuits to be examined without remodeling the circuit, which is used for the Beta Network Analysis Method.

The Class G amplifier was shown to be a more efficient circuit than the Class B amplifier for small input signals. The trade off for more efficiency is the cost and space of more circuit components. The Total Harmonic Distortion was also shown to be at reasonable levels for audio applications. The Class G amplifier could be used in portable devices with a specially developed battery, which would provide the necessary voltages to help increase battery life.

This thesis also proposes more study of the Class G amplifier to gain better performance. Using bipolar transistors for analysis lays down the "ground work" for more designs such as Class G amplifiers using FETs, MOSFETs, and combinations thereof. More work also needs to be done using more than four power supplies and identifying how the Class G amplifier can be optimized for different applications, such as amplifying speech versus amplifying symphonic music.

Appendix A

Sspice

Sspice - Circuit Analyzer and Approximator

Sspice (Symbolic Simulation Program with Integrated Circuit Emphasis)

Developed by Vivek Joshi, Anupam Srivastava, James MacKay, Sin-Min Chang, and Dr. Gregory Wierzba with support from Michigan State University.

Evaluation and Approximation

"Besides analyzing circuits, Sspice can also optionally evaluate its results and even make some global approximations. In sorting by powers of the Laplace variable s many terms may be added or subtracted. Given numeric values for the coefficients for each power of s, Sspice finds the largest magnitude term. Using a user specified threshold magnitude, Sspice multiplies the largest magnitude term by the user specified threshold magnitude and then discards any terms for that power of s which are below this value."

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Appendix B

Beta Network Analysis Method

An operational amplifier circuit can be modeled as a basic feedback topology shown in Figure B-1.

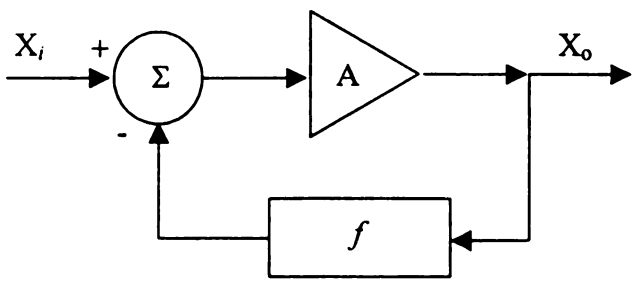

Figure B-1: Basic negative-feedback topology

The overall gain of the system including the effects of feedback is written as

$$A_f(s) = \frac{A(s)}{1 + A(s) \cdot f}$$

Stable amplifier operation requires the magnitude of the loop gain, |A(s)f|, to be less than unity when its phase angle approaches 180°. The magnitude of the loop gain (in decibels) can be expressed as the difference of the magnitude of the open-loop gain and the magnitude of the inverse of the feedback ratio.

$$20 \cdot \log|A(s) \cdot f| = 20 \cdot \log|A(s)| - 20 \cdot \log\left|\frac{1}{f}\right|$$

The loop gain is the difference between the open-loop gain and the inverse of the feedback ratio [3].

The gain for an inverting Op-Amp is:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_2}{R_1} * \frac{1}{1 + \frac{1}{A_{DM}} \cdot \frac{1}{\beta}}$$

Testing the stability of the Op-Amp circuit with the following conditions:

$$A_{DM} = A_o \cdot \frac{w_o}{s + w_o}$$

$$\frac{1}{\beta} = \frac{B_o \cdot (s^2 + w_z^2)}{s^2 + \frac{w_z}{Q_o} \cdot s + w_z^2}$$

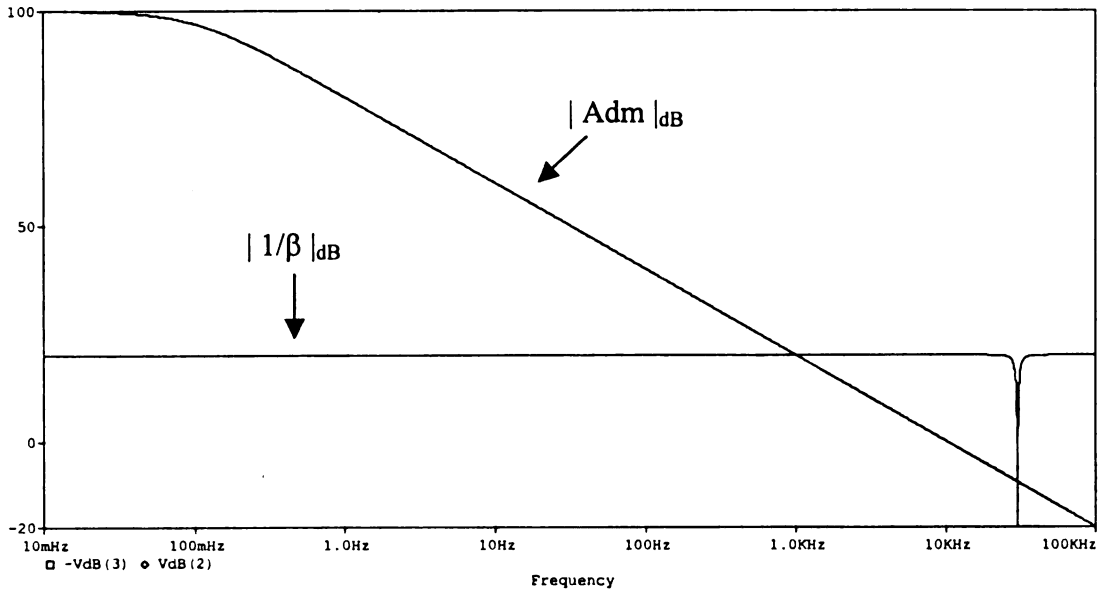

Figure B-2: Example graph of Adm and 1/β

Figure B-2 shows the graph of the gain of Adm and 1/β. Notice that the gain of 1/β crosses the gain of the Op-Amp more than once.

Substituting A_{DM} and β into the gives the following equations:

$$\text{Gain} = -\frac{R2}{R1}\cdot\frac{1}{1+\frac{1}{\left(A_o\cdot\frac{w_o}{s+w_o}\right)}\cdot\frac{B_o\cdot(s^2+w_z{}^2)}{\left(s^2+\frac{w_z}{Q_o}\cdot s+w_z{}^2\right)}}$$

$$= -\frac{R2}{R1}\cdot\frac{1}{1+\frac{(s+w_o)\cdot B_o\cdot\left(s^2+w_z{}^2\right)}{A_o\cdot w_o\cdot\left(s^2+\frac{w_z}{Q_o}\cdot s+w_z{}^2\right)}}$$

$$= -\frac{R2}{R1}\cdot\frac{A_o\cdot w_o\cdot\left(s^2+\frac{w_z}{Q_o}\cdot s+w_z{}^2\right)}{A_o\cdot w_o\cdot\left(s^2+\frac{w_z}{Q_o}\cdot s+w_z{}^2\right)+(s+w_o)\cdot B_o\cdot\left(s^2+w_z{}^2\right)}$$

$$= -\frac{R2}{R1}\cdot\frac{A_o\cdot w_o\cdot\left(s^2+\frac{w_z}{Q_o}\cdot s+w_z{}^2\right)}{s^3+w_o\cdot\left(\frac{A}{B}+1\right)\cdot s^2+w_z{}^2\cdot\left(\frac{A\cdot w_o}{B\cdot Q\cdot w_z}+1\right)\cdot s+w_o\cdot w_z{}^2\cdot\left(\frac{A}{B}+1\right)}$$

The next steps will show that equation can take on the following form:

$$= -\frac{R2}{R1}\cdot\frac{A_o\cdot w_o\cdot\left(s^2+\frac{w_z}{Q_o}\cdot s+w_z{}^2\right)}{(s+X)\cdot(s^2-Y\cdot s+w_z{}^2)}$$

$$= -\frac{R2}{R1}\cdot\frac{A_o\cdot w_o\cdot\left(s^2+\frac{w_z}{Q_o}\cdot s+w_z{}^2\right)}{s^3+[X-Y]\cdot s^2+(w_z{}^2-X\cdot Y)\cdot s+X\cdot w_z{}^2}$$

Solving for X and Y:

Let X equal the following:

$$X = w_o \cdot \left(\frac{A}{B} + 1\right)$$

Now solve for the coefficient of s^1.

$$w_z{}^2 - X \cdot Y = w_z{}^2 \cdot \left(\frac{A \cdot w_o}{B \cdot Q \cdot w_z} + 1\right)$$

$$Y = \frac{w_z}{\left(\frac{B}{A} + 1\right) \cdot Q}$$

What happens as Q goes to infinity?

$$\lim_{Q \to \infty} Y = \frac{w_z}{\left(\frac{B}{A} + 1\right) \cdot \infty} = 0$$

Now solve and verify the coefficient of s^2

.

$$X - Y = w_o \cdot \left(\frac{A}{B} + 1\right)$$

$$Y = 0$$

The revised equation for the gain of the circuit is:

$$= -\frac{R2}{R1} \cdot \frac{A_o \cdot w_o \cdot (s^2 + w_z{}^2)}{\left[s + w_o \cdot \left(\frac{A}{B} + 1\right)\right] \cdot \left[s^2 + w_z{}^2\right]}$$

Do not cancel (s2+wz2) from the numerator and the denominator because they will not be equal. This is only an approximation to solve for the

$$= -\frac{R2}{R1} \cdot \frac{A_o \cdot w_o \cdot (s^2 + w_z{}^2)}{\left[s + w_o \cdot \left(\frac{A}{B} + 1\right)\right] \cdot \left[\left(s + \sqrt{-w_z{}^2}\right) \cdot \left(s - \sqrt{-w_z{}^2}\right)\right]}$$

The above equation indicates that as the Q of the circuit gets larger and larger, the transfer function shows that the circuit will be unstable and oscillate at the frequency

$$\sqrt{\left|-w_z{}^2\right|}$$

Here is an example:

Given:

$$A_{DM} = 100k \cdot \frac{2\pi \cdot 0.1}{s + 2\pi \cdot 0.1}$$

$$\frac{1}{\beta} = 10 \cdot \frac{s^2 + (2\pi \cdot 30k)^2}{s^2 + \frac{(2\pi \cdot 3Meg)}{1E6} \cdot s + (2\pi \cdot 30k)^2}$$

$$R_1 = 1k$$

$$R_2 = 1k$$

Using Matlab to solve for the roots of the denominator, the following Matlab code will show the gain symbolically.

```
syms s;
syms w1 w2 A B Q;
R2 = 1e3;
R1 = 1e3;
ADM = (A*w1/(s+w1));
disp('Adm = ')
pretty(ADM)
Beta = ((s^2+w2/Q*s+w2^2) / (B*(s^2+w2^2)));
disp('1/Beta = ')
pretty(1/Beta)
sol = -R2/R1 * 1/( 1 + 1/ADM * 1/Beta  );
sol = simplify(sol)
disp('GAIN = ')
pretty(sol)
```

MATLAB Results:

```
» example.m
GAIN =

                2                  2        /          2                              2
  - w1 A (s  Q + w2 s + w2  Q)  /  (w1 A s  Q + w1 A w2 s + w1 A w2  Q
                                /

                  3             2             2             2
          + Q B s  + Q B s w2  + Q B w1 s  + Q B w1 w2 )
```

Now just analyzing the denominator, the following Matlab code will give the numerical results of the denominator and the roots of the numerator and denominator (notice that they are indeed different).

```
w1 = 0.1*2*pi;
w2 = 30E3*2*pi;
A = 100E3;
B = 10;
Q = 10;
num = -A*w1*(s^2*Q+w2*s+w2^2*Q);
den=(A*w1*s^2*Q+A*w1*w2*s+A*w1*w2^2*Q+Q*B*s^3+Q*B*s*w2^2+Q*B*w1*s^2+Q*B
*w1*w2^2);

roots_num = vpa(solve(num,s),3)
roots_den = vpa(solve(den,s),3)
```

MATLAB Results:

```
roots_num =
[ -.942e4+.188e6*i]
[ -.942e4-.188e6*i]

roots_den =
[          -.609e4]
[ -.19e3-.189e6*i]
[ -.19e3+.189e6*i]
```

These roots confirm that the approximated equation for finding the roots is reasonable. Using the derived equation, the roots for the denominator are:

$$\sqrt{\left|-w_z^2\right|} = \sqrt{(2\pi \cdot 30k)^2} = 0.188e6 \text{ rad/sec}$$

Figure B-2 shows the gain of Adm and 1/b plotted on the same graph. The graph shows that there are 2 points of intersection. Figure B-3 includes the phase of Adm plus the phase of the beta network. This graphs shows that the phase margin of the circuit is negative indicating that it is unstable. This shows that a Beta Network Analysis can be used to test for stability when the graph of Adm and 1/ β intersect at multiple points. All intersections must have a positive phase margin to be stable.

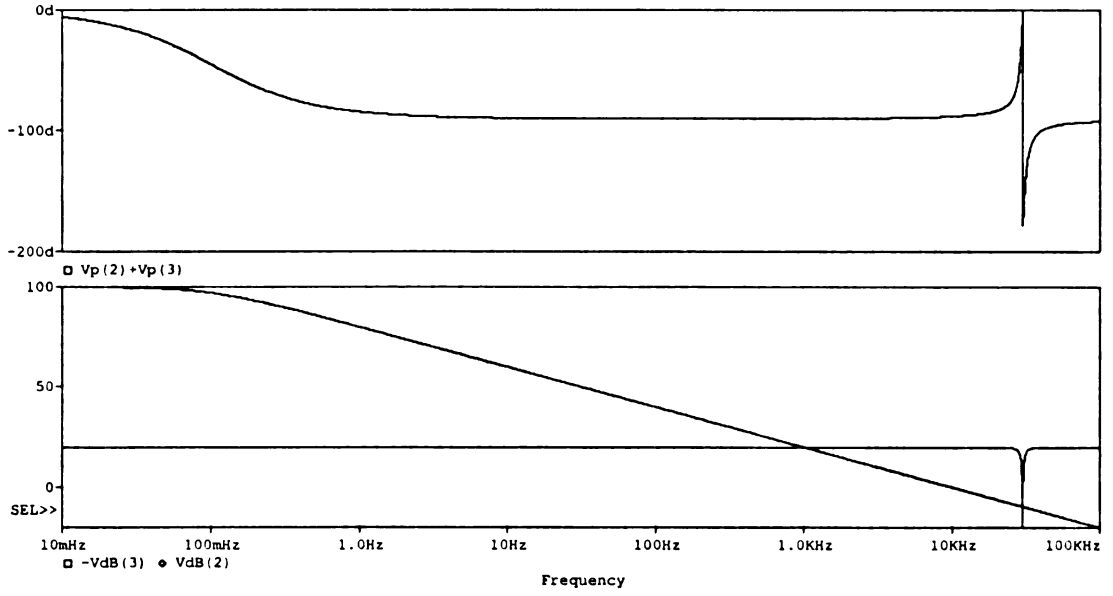

Figure B-3: Graph of Adm, 1/β and the phase of Adm + 1/β

Appendix C

```
Class G Amplifier
V2  2 0  12
V1  3 0   5
V1P 4 0  -5
V2P 5 0 -12
VBIAS A 101 2.1V
VBIASP 101 B 2.1V
VIN 1 N DC 0V AC 1 SIN 0 5 1k 0m 0 0
VNOISE N 0 DC 0V AC 1 SIN 0 .1 500K
X1 0 30 2 5 100 LF411
VOPAMP 100 101 0
RIN 1 30 1K
RF 15 30 1K
QA 2 A 10 Q2N3904
QB 5 B 105 Q2N3906
Q2 2  20 13 TIP31
Q1 13 11 15 TIP31
Q1P 14 12 15 TIP32
Q2P 5  23 14 TIP32
DB2   10  20 D1N4148
DB1A  10  21 D1N4148
DB1B  21  11 D1N4148
DB1AP 12  22 D1N4148
DB1BP 22 105 D1N4148
DB2P  23 105 D1N4148
D1  3 13 D1N5817
D2 14  4 D1N5817
RL 15  0 10
.TRAN 1U 2000U 0 1U
.MODEL DMOD D
.LIB ECE484.LIB
.LIB DIODE.LIB
.PROBE
.END
```

Figure C-1: PSpice circuit file

Appendix D

Forcing the power lines to oscillate *.cir file

```
Class G Amplifier
V2  200 0  15
*v2osc X 0 sin 0 .4 12Meg
V1  3 0   5
V1P 4 0  -5
V2P 500 0 -15
*v2posc Y 0 sin 0 -.4 12Meg
LVP2 5 500 1U
LV2 2 200 1U
*  Input Sources
VIN 1 a DC 0V AC 1 SIN 0 -4.5 1K
*RO 110 11 75
VNOISE A 0 DC 0V AC 1 SIN 0 .4 400K
*VBIAS B C {VAL}
X1 0 10 2 5 11 ICL8741
RIN 1 10 1K
RF 19 10 1K
QA 2 11 12 Q2N3904
QB 5 11 12 Q2N3906
Q2 2 13 16 TIP31
Q1 16 15 19 TIP31
Q1P 21 18 19 TIP32
Q2P 5 20 21 TIP32
DB2   12 13 D1N4148
DB1A  12 14 D1N4148
DB1B  14 15 D1N4148
DB1AP 18 17 D1N4148
DB1BP 17 12 D1N4148
DB2P  20 12 D1N4148
D1 3  16 D1N5817
D2 21  4 D1N5817
XL 190  0 G12H100
VXL 190 19 0V
*RL 19 0 10
.PARAM VAL = 1
.STEP PARAM VAL LIST 0
.TRAN .1U 3000U 1000U .1U
.LIB ECE402.LIB
.LIB DIODE.LIB
.LIB IC.LIB
.OP
.PROBE
.END
```

Figure D-1: PSpice circuit file

The small signal bias solution output from PSpice:

```
****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C
****     CURRENT STEP                     PARAM VAL =   -4.2
********************************************************************************
 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE
(    1)   -4.2000  (    2)   15.0000  (    3)    5.0000  (    4)   -5.0000
(    5)  -15.0000  (    B)   -4.2000  (   10) 205.7E-06  (   11)    7.0695
(   12)    6.3292  (   13)    5.6231  (   14)    5.6148  (   15)    4.9005
(   16)    4.9277  (   17)    6.3292  (   18)    6.3292  (   19)    4.2007
(   20)    6.3292  (   21)   -5.0000  (  190)    4.2007  (  200)   15.0000

****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C
****     CURRENT STEP                     PARAM VAL =   -3
********************************************************************************
 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE
(    1)   -3.0000  (    2)   15.0000  (    3)    5.0000  (    4)   -5.0000
(    5)  -15.0000  (    B)   -3.0000  (   10) 209.5E-06  (   11)    5.7695
(   12)    5.0621  (   13)    4.9304  (   14)    4.3741  (   15)    3.6862
(   16)    4.6523  (   17)    5.0621  (   18)    5.0621  (   19)    3.0007
(   20)    5.0621  (   21)   -5.0000  (  190)    3.0007  (  200)   15.0000

****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C
****     CURRENT STEP                     PARAM VAL =    3
********************************************************************************
 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE
(    1)    3.0000  (    2)   15.0000  (    3)    5.0000  (    4)   -5.0000
(    5)  -15.0000  (    B)    3.0000  (   10) 243.3E-06  (   11)   -5.9535
(   12)   -5.2050  (   13)    5.1698  (   14)   -4.0288  (   15)   -2.8150
(   16)    5.0000  (   17)   -4.5003  (   18)   -3.7956  (   19)   -2.9993
(   20)   -5.0834  (   21)   -4.6526  (  190)   -2.9993  (  200)   15.0000

****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C
****     CURRENT STEP                     PARAM VAL =    4.2
********************************************************************************
 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE
(    1)    4.2000  (    2)   15.0000  (    3)    5.0000  (    4)   -5.0000
(    5)  -15.0000  (    B)    4.2000  (   10) 247.1E-06  (   11)   -7.2658
(   12)   -6.4822  (   13)    5.1684  (   14)   -5.2700  (   15)   -4.0151
(   16)    5.0000  (   17)   -5.7470  (   18)   -5.0117  (   19)   -4.1993
(   20)   -5.7570  (   21)   -4.9496  (  190)   -4.1993  (  200)   15.0000
```

Figure D-2: PSpice small signal bias solutions

```
Class G Amplifier
V2  2 a  15
v2osc a 0 sin 0 .4 12MEG
V1  3 0   5
V1P 4 0  -5
V2P 5 b -15
v2posc b 0 sin 0 -.4 12MEG
*  Input Sources
VIN 1 0 DC 0V AC 1 SIN 0 8 1K
X1 0 10 2 5 11 ICL8741
RIN 1 10 1K
RF 19 10 1K
QA 2 11 12 Q2N3904
QB 5 11 12 Q2N3906
Q2 2 13 16 TIP31
Q1 16 15 19 TIP31
Q1P 21 18 19 TIP32
Q2P 5 20 21 TIP32
DB2   12 13 D1N4148
DB1A  12 14 D1N4148
DB1B  14 15 D1N4148
DB1AP 18 17 D1N4148
DB1BP 17 12 D1N4148
DB2P  20 12 D1N4148
D1 3  16 D1N5817
D2 21  4 D1N5817
*  Speaker Model
XL 190  0 G12H100
VXL 190 19 0V
.TRAN 1U 2000U 0 1U
.LIB ECE402.LIB
.LIB DIODE.LIB
.LIB IC.LIB
.PROBE
.END
```

Figure D-3: PSpice circuit file

```
Class G Amplifier

V2  200 0  15
*v2osc X 0 sin 0 .4 12Meg
V1  3 0   5
V1P 4 0  -5
V2P 500 0 -15
*v2posc Y 0 sin 0 -.4 12Meg
LVP2 5 500 1U
LV2 2 200 1U
*  Input Sources
VIN 1 a DC 0V AC 1 SIN 0 -4.5 1K
*RO 110 11 75
VNOISE A 0 DC 0V AC 1 SIN 0 .4 400K
*VBIAS B C {VAL}
X1 0 10 2 5 11 ICL8741
RIN 1 10 1K
RF 19 10 1K
QA 2 11 12 Q2N3904
QB 5 11 12 Q2N3906
Q2 2 13 16 TIP31
Q1 16 15 19 TIP31
Q1P 21 18 19 TIP32
Q2P 5 20 21 TIP32
DB2   12 13 D1N4148
DB1A  12 14 D1N4148
DB1B  14 15 D1N4148
DB1AP 18 17 D1N4148
DB1BP 17 12 D1N4148
DB2P  20 12 D1N4148
D1 3  16 D1N5817
D2 21  4 D1N5817
XL 190  0 G12H100
VXL 190 19 0V
*RL 19 0 10
.PARAM VAL = 1
.STEP PARAM VAL LIST 0
.TRAN .1U 3000U 1000U .1U
.LIB ECE402.LIB
.LIB DIODE.LIB
.LIB IC.LIB
.OP
.PROBE
.END
```

Figure D-4: PSpice circuit file

```
Class G Amplifier
V2  2 a  15
v2osc a 0 sin 0 .4 12MEG
V1  3 0   5
V1P 4 0  -5
V2P 5 b -15
v2posc b 0 sin 0 -.4 12MEG
*  Input Sources
VIN 1 0 DC 0V AC 1 SIN 0 8 1K
X1 0 10 2 5 11 ICL8741
RIN 1 10 1K
RF 19 10 1K
QA 2 11 12 Q2N3904
QB 5 11 12 Q2N3906
Q2 2 13 16 TIP31
Q1 16 15 19 TIP31
Q1P 21 18 19 TIP32
Q2P 5 20 21 TIP32
DB2   12 13 D1N4148
DB1A  12 14 D1N4148
DB1B  14 15 D1N4148
DB1AP 18 17 D1N4148
DB1BP 17 12 D1N4148
DB2P  20 12 D1N4148
D1 3  16 D1N5817
D2 21  4 D1N5817
*  Speaker Model
XL 190  0 G12H100
VXL 190 19 0V
.TRAN 1U 2000U 0 1U
.LIB ECE402.LIB
.LIB DIODE.LIB
.LIB IC.LIB
.PROBE
.END
```

Figure D-5: PSpice circuit file

Appendices E

Full Beta Network Circuit File

```
Beta Analysis
*
V2       200 0  15
V1       3   0   5
V1P      4   0  -5
V2P    500   0 -15
rlvp2 499 500 1
rlv2  199 200 1
LVP2     5 499 1U
LV2      2 199 1U
VBIAS 1 A {VAL}
VNOISE A 0 AC 1
*X1 0 10 2 5 11 ICL8741
RIX1 77 0 2MEG
CIX1 77 0 2P
ROX1 1 11 75
RIN 0 77 1K
RF 19 77 1K
QA 2 11 12 Q2N3904
QB 5 11 12 Q2N3906
Q2 2 13 16 TIP31
Q1 16 15 19 TIP31
Q1P 21 18 19 TIP32
Q2P 5 20 21 TIP32
DB2    12 13 D1N4148
DB1A   12 14 D1N4148
DB1B   14 15 D1N4148
DB1AP 18 17 D1N4148
DB1BP 17 12 D1N4148
DB2P   20 12 D1N4148
D1 3   16 D1N5817
D2 21   4 D1N5817
RL 19 0 10
* ICL8741 POLE GRAPHING
VH 70 0 15
VL 71 0 -15
VIN 100 0 AC 1
VIO 100 B 226.08U
X1 B 0 70 71 73 ICL8741
ROUT 73 0 10K
.PARAM VAL = 1
.STEP PARAM VAL LIST 6.133 -6.232
.AC DEC 2000 1MEG 100MEG
.LIB ECE402.LIB
.LIB DIODE.LIB
.LIB IC.LIB
.OP
.PROBE
.END
```

Figure E-1: PSpice circuit file

```
****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C
****     CURRENT STEP                     PARAM VAL =     6.133
********************************************************************************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE
(    1)    6.1330  (    2)   14.9960  (    3)    5.0000  (    4)   -5.0000
(    5)  -15.0000  (    A)    0.0000  (    B)-226.1E-06  (   11)    6.1314
(   12)    5.4342  (   13)    5.1041  (   14)    4.7658  (   15)    4.0974
(   16)    4.6697  (   17)    5.4342  (   18)    5.4342  (   19)    3.4231
(   20)    5.4342  (   21)   -5.0000  (   70)   15.0000  (   71)  -15.0000
(   73) 55.85E-06  (   77)    1.7111  (  100)    0.0000  (  199)   14.9960
(  200)   15.0000  (  499)  -15.0000  (  500)  -15.0000
```

Figure E-2: PSpice small signal bias solutions

```
****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C
****     CURRENT STEP                     PARAM VAL =     6.133
**************************************************************************
**** DIODES
NAME          DB2          DB1A         DB1B         DB1AP        DB1BP
MODEL         D1N4148      D1N4148      D1N4148      D1N4148      D1N4148
ID            3.45E-06     3.64E-03     3.64E-03    -2.94E-13    -2.94E-13
VD            3.30E-01     6.68E-01     6.68E-01    -3.38E-06    -3.39E-06
REQ           1.42E+04     1.34E+01     1.34E+01     1.15E+07     1.15E+07
CAP           6.39E-12     8.67E-10     8.67E-10     4.00E-12     4.00E-12

NAME          DB2P         D1           D2
MODEL         D1N4148      D1N5817      D1N5817
ID           -4.98E-13     3.40E-01    -2.41E-12
VD           -5.74E-06     3.30E-01    -2.86E-09
REQ           1.15E+07     1.12E-01     1.19E+03
CAP           4.00E-12     6.62E-10     4.72E-10

**** BIPOLAR JUNCTION TRANSISTORS
NAME          QA           QB           Q2           Q1           Q1P
MODEL         Q2N3904      Q2N3906      TIP31        TIP31        TIP32
IB            2.14E-05     4.25E-12     3.45E-06     3.64E-03     2.96E-13
IC            3.62E-03    -4.78E-11     5.29E-05     3.40E-01    -9.54E-12
VBE           6.97E-01     6.97E-01     4.34E-01     6.74E-01     2.01E+00
VBC          -8.86E+00     2.11E+01    -9.89E+00    -5.72E-01     1.04E+01
VCE           9.56E+00    -2.04E+01     1.03E+01     1.25E+00    -8.42E+00
BETADC        1.69E+02    -1.12E+01     1.53E+01     9.34E+01    -3.22E+01
GM            1.34E-01    -1.09E-12     2.04E-03     9.52E+00    -8.42E-14
RPI           1.38E+03     1.81E+14     1.13E+04     8.06E+00     4.34E+14
RX            1.00E+01     1.00E+01     1.00E-01     1.00E-01     1.00E-01
RO            2.29E+04     3.10E+11     2.08E+06     2.95E+02     8.41E+11
CBE           4.69E-11     6.33E-12     3.25E-10     1.90E-07     1.03E-10
CBC           1.66E-12     1.39E-12     4.48E-11     1.17E-10     5.84E-11
CJS           0.00E+00     0.00E+00     0.00E+00     0.00E+00     0.00E+00
BETAAC        1.85E+02    -1.97E+02     2.30E+01     7.68E+01    -3.66E+01
CBX/CBX2      0.00E+00     0.00E+00     0.00E+00     0.00E+00     0.00E+00
FT/FT2        4.39E+08    -2.25E-02     8.78E+05     7.99E+06    -8.32E-05

NAME          Q2P
MODEL         TIP32
IB            4.96E-13
IC           -1.25E-11
VBE           1.04E+01
VBC           2.04E+01
VCE          -1.00E+01
BETADC       -2.51E+01
GM           -1.00E-13
RPI           4.34E+14
RX            1.00E-01
RO            7.67E+11
CBE           5.64E-11
CBC           4.77E-11
CJS           0.00E+00
BETAAC       -4.34E+01
CBX/CBX2      0.00E+00
FT/FT2       -1.53E-04
```

Figure E-3: PSpice operating point information

```
     ****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C
****     CURRENT STEP                         PARAM VAL =   -6.232
**********************************************************************************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE
(    1)   -6.2320  (    2)   15.0000  (    3)    5.0000  (    4)   -5.0000
(    5)  -14.9950  (    A)    0.0000  (    B)-226.1E-06  (   11)   -6.2307
(   12)   -5.4944  (   13)    5.1695  (   14)   -4.3310  (   15)   -3.1671
(   16)    5.0000  (   17)   -4.8142  (   18)   -4.1340  (   19)   -3.3514
(   20)   -5.2084  (   21)   -4.6710  (   70)   15.0000  (   71)  -15.0000
(   73) 220.8E-06  (   77)   -1.6753  (  100)    0.0000  (  199)   15.0000
(  200)   15.0000  (  499)  -14.9950  (  500)  -15.0000
```

Figure E-4: PSpice small signal bias solutions

```
****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C
****     CURRENT STEP                     PARAM VAL =   -6.232
******************************************************************************
**** DIODES
NAME          DB2          DB1A         DB1B         DB1AP        DB1BP
MODEL         D1N4148      D1N4148      D1N4148      D1N4148      D1N4148
ID           -7.09E-09    -5.02E-09    -5.02E-09     4.58E-03     4.58E-03
VD           -1.07E+01    -1.16E+00    -1.16E+00     6.80E-01     6.80E-01
REQ           1.52E+10     4.27E+09     4.28E+09     1.08E+01     1.08E+01
CAP           1.42E-12     2.68E-12     2.68E-12     1.08E-09     1.08E-09

NAME          DB2P         D1           D2
MODEL         D1N4148      D1N5817      D1N5817
ID            1.40E-06     8.50E-09     3.32E-01
VD            2.86E-01     1.01E-05     3.29E-01
REQ           3.49E+04     1.19E+03     1.14E-01
CAP           5.61E-12     4.72E-10     6.61E-10

**** BIPOLAR JUNCTION TRANSISTORS
NAME          QA           QB           Q2           Q1           Q1P
MODEL         Q2N3904      Q2N3906      TIP31        TIP31        TIP32
IB           -2.88E-11    -1.79E-05    -7.09E-09    -5.02E-09    -4.58E-03
IC            5.52E-11    -4.56E-03     1.36E-08     1.50E-08    -3.32E-01
VBE          -7.36E-01    -7.36E-01     1.69E-01     1.84E-01    -7.83E-01
VBC          -2.12E+01     8.76E+00    -9.83E+00    -8.17E+00     5.37E-01
VCE           2.05E+01    -9.50E+00     1.00E+01     8.35E+00    -1.32E+00
BETADC       -1.91E+00     2.55E+02    -1.92E+00    -2.99E+00     7.26E+01
GM           -2.77E-13     1.70E-01     7.29E-08     1.27E-07     8.08E+00
RPI           4.16E+14     1.45E+03     8.67E+06     6.00E+06     6.40E+00
RX            1.00E+01     1.00E+01     1.00E-01     1.00E-01     1.00E-01
RO            6.40E+11     6.02E+03     5.45E+10     3.16E+10     3.02E+02
CBE           3.76E-12     4.46E-11     2.14E-10     2.16E-10     1.11E-07
CBC           1.28E-12     2.24E-12     4.49E-11     4.83E-11     1.19E-10
CJS           0.00E+00     0.00E+00     0.00E+00     0.00E+00     0.00E+00
BETAAC       -1.15E+02     2.46E+02     6.32E-01     7.65E-01     5.17E+01
CBX/CBX2      0.00E+00     0.00E+00     0.00E+00     0.00E+00     0.00E+00
FT/FT2       -8.73E-03     5.77E+08     4.49E+01     7.66E+01     1.16E+07

NAME          Q2P
MODEL         TIP32
IB           -1.40E-06
IC           -5.94E-05
VBE          -5.37E-01
VBC           9.79E+00
VCE          -1.03E+01
BETADC        4.24E+01
GM            2.29E-03
RPI           2.21E+04
RX            1.00E-01
RO            1.85E+06
CBE           3.17E-10
CBC           5.95E-11
CJS           0.00E+00
BETAAC        5.07E+01
CBX/CBX2      0.00E+00
FT/FT2        9.69E+05
```

Figure E-5: PSpice operating point information

```
Class G Amplifier Vbias 6.133 Simplified
*  Input Sources
VBIAS  A 1 {VAL}
VNOISE 1 0 AC 1
LV2   4 0 1U
GMA   4 3 2 3 0.134
CBEA 2 3 4.69E-11
CBCA 2 4 1.66E-12
GM2   4 0 8 0 2.04E-3
CBE2 8 0 3.25E-10
CBC2 8 4 4.48E-11
GM1    0 12 11 12 9.52
RPI1 11 12 8.06
CBE1 11 12 1.90E-7
REQDB2 3 8 1.42E4
REQDB1A  3 10 13.4
CAPDB1A  3 10 8.67E-10
REQDB1B 10 11 13.4
CAPDB1B 10 11 8.67E-10
RF   12 77  5
RIN 77  0  5
RO    A  2 75
*************************
* ICL8741 POLE GRAPHING
VH 70 0 15
VL 71 0 -15
VIN 100 0 AC 1
VIO 100 B 226.08U
X1 B 0 70 71 73 ICL8741
ROUT 73 0 10K
*************************
.PARAM VAL = 1
.STEP PARAM VAL LIST 6.1
.AC DEC 900 1 100MEG
.LIB IC.LIB
.OP
.PROBE
.END
```

Figure E-6: PSpice circuit file

```
Class G Amplifier Vbias 6.133 Simplified
*
VNOISE 1 0 AC 1
LV2 4 0 1U
GMA 4 3 2 3 0.134
CBCA 2 4 1.66E-12
CBC2 0 4 4.48E-11
REQDB1B 3 11 13.4
RL1 11 77 5
RL2 77 0 5
RO 1 2 75
*
.AC DEC 900 1 100MEG
.PROBE
.END
```

Figure E-7: PSpice circuit file

```
Class G Amplifier Vbias -6.232
*
VNOISE 1 0 AC 1
LV2P 5 0 1U
GMB 3 5 3 2 .170
CBCB 2 5 2.24E-12
CBC2P 0 5 5.95E-11
REQDB1BP 3 12 10.8
RL1 12 77 5
RL2 77 0 5
RO 1 2 75
*
.AC DEC 900 1 100MEG
.PROBE
.END
```

Figure E-8: PSpice circuit file

Class G Amplifier Vbias 6.133 Simplified

```
[0   ] [-GO   sCBCA+GO 0         -sCBCA    0         0         0       ][V1 ]
[0   ] [0     -GMMA    Y 2,3     0         -GEQDB1B 0         0       ][V2 ]
[0   ] [0     Y 3,2    -GMMA     Y 3,4     0         0         1       ][V3 ]
[0   ]=[0     0        -GEQDB1B  0         Y 4,5     -GL1      0       ][V4 ]
[0   ] [0     0        0         0         -GL1      GL2+GL1   0       ][V11]
[1   ] [1     0        0         0         0         0         0       ][V77]
[0   ] [0     0        0         sLV2+1    0         0         -sLV2   ][V79]

Y( 2,3 ) = +GMMA+GEQDB1B
Y( 3,2 ) = -sCBCA+GMMA
Y( 3,4 ) = +sCBCA+sCBC2-1
Y( 4,5 ) = +GL1+GEQDB1B
*Ignore nodes 78 and higher if present. They are used for internal
numbering.

Numerator of: v77

TERMS SORTED ACCORDING TO POWERS OF s
s**2 terms:
 + sLV2*sCBCA*GO*GMMA*GL1*GEQDB1B + sLV2*sCBC2*GO*GMMA*GL1*GEQDB1B
s**0 terms:
 + GO*GMMA*GL1*GEQDB1B
************************************************
NUMERICAL VALUE OF ABOVE SYMBOLIC RESULT
+ 1.23893e-021 * s**2 + 2.66666e-005 * s**0
************************************************

Denominator of: v77
TERMS SORTED ACCORDING TO POWERS OF s
s**3 terms:
 + sLV2*sCBCA*sCBC2*GMMA*GL2*GL1
 + sLV2*sCBCA*sCBC2*GMMA*GL2*GEQDB1B
 + sLV2*sCBCA*sCBC2*GMMA*GL1*GEQDB1B
 + sLV2*sCBCA*sCBC2*GL2*GL1*GEQDB1B
s**2 terms:
 + sLV2*sCBCA*GO*GMMA*GL2*GL1 + sLV2*sCBCA*GO*GMMA*GL2*GEQDB1B
 + sLV2*sCBCA*GO*GMMA*GL1*GEQDB1B + sLV2*sCBCA*GO*GL2*GL1*GEQDB1B
 + sLV2*sCBCA*GMMA*GL2*GL1*GEQDB1B + sLV2*sCBC2*GO*GMMA*GL2*GL1
 + sLV2*sCBC2*GO*GMMA*GL2*GEQDB1B + sLV2*sCBC2*GO*GMMA*GL1*GEQDB1B
 + sLV2*sCBC2*GO*GL2*GL1*GEQDB1B
s**1 terms:
 + sCBCA*GMMA*GL2*GL1 + sCBCA*GMMA*GL2*GEQDB1B
 + sCBCA*GMMA*GL1*GEQDB1B + sCBCA*GL2*GL1*GEQDB1B
s**0 terms:
 + GO*GMMA*GL2*GL1 + GO*GMMA*GL2*GEQDB1B + GO*GMMA*GL1*GEQDB1B
 + GO*GL2*GL1*GEQDB1B
************************************************
NUMERICAL VALUE OF ABOVE SYMBOLIC RESULT
+ 9.18079e-031 * s**3 + 8.31135e-021 * s**2 + 2.04928e-014 * s**1 +
0.000164601 * s**0
************************************************
```

Figure E-9: Sspice results

Class G Amplifier Vbias 6.133 Simplified and using Sspice approximator option

```
[0  ] [-GO  sCBCA+GO 0         -sCBCA   0         0         0       ][V1 ]
[0  ] [0    -GMMA    Y 2,3     0        -GEQDB1B 0         0       ][V2 ]
[0  ] [0    Y 3,2    -GMMA     Y 3,4    0         0         1       ][V3 ]
[0  ]=[0    0        -GEQDB1B  0        Y 4,5     -GL1      0       ][V4 ]
[0  ] [0    0        0         0        -GL1      GL2+GL1   0       ][V11]
[1  ] [1    0        0         0        0         0         0       ][V77]
[0  ] [0    0        0         sLV2+1   0         0         -sLV2   ][V79]

Y( 2,3 ) = +GMMA+GEQDB1B
Y( 3,2 ) = -sCBCA+GMMA
Y( 3,4 ) = +sCBCA+sCBC2-1
Y( 4,5 ) = +GL1+GEQDB1B
*Ignore nodes 78 and higher if present. They are used for internal
numbering.

RESULTS APPROXIMATED USING A THRESHOLD MAGNITUDE OF: 0.90

Numerator of: v77
TERMS SORTED ACCORDING TO POWERS OF s
s**2 terms:
 + sLV2*sCBC2*GO*GEQDB1B
s**0 terms:
 + GO*GEQDB1B
************************************************
NUMERICAL VALUE OF ABOVE SYMBOLIC RESULT
+ 4.4577e-020 * s**2 + 0.000995023 * s**0
************************************************

Denominator of: v77
TERMS SORTED ACCORDING TO POWERS OF s
s**3 terms:
 + sLV2*sCBCA*sCBC2*GL2
s**2 terms:
 + sLV2*sCBC2*GO*GL2
s**1 terms:
 + sCBCA*GL2
s**0 terms:
 + GO*GL2
************************************************
NUMERICAL VALUE OF ABOVE SYMBOLIC RESULT
+ 1.48736e-029 * s**3 + 1.19466e-019 * s**2 + 3.32e-013 * s**1 +
0.00266666 * s**0
************************************************
```

Figure E-10: Sspice results

Class G Amplifier Vbias -6.232

```
[0  ] [-GO  sCBCB+GO 0        -sCBCB   0        0        0       ][V1 ]
[0  ] [0    -GMMB    Y 2,3    0        Y 2,5    0        0       ][V2 ]
[0  ] [0    Y 3,2    -GMMB    Y 3,4    0        0        1       ][V3 ]
[0  ]=[0    0        Y 4,3    0        Y 4,5    -GL1     0       ][V5 ]
[0  ] [0    0        0        0        -GL1     GL2+GL1  0       ][V12]
[1  ] [1    0        0        0        0        0        0       ][V77]
[0  ] [0    0        0        sLV2P+1  0        0        -sLV2P ][V79]
Y( 2,3 ) = +GMMB+GEQDB1BP
Y( 2,5 ) = -GEQDB1BP
Y( 3,2 ) = -sCBCB+GMMB
Y( 3,4 ) = +sCBCB+sCBC2P-1
Y( 4,3 ) = -GEQDB1BP
Y( 4,5 ) = +GL1+GEQDB1BP
*Ignore nodes 78 and higher if present. They are used for internal
numbering.
Numerator of: v77
TERMS SORTED ACCORDING TO POWERS OF s
s**2 terms:
 + sLV2P*sCBCB*GO*GMMB*GL1*GEQDB1BP
 + sLV2P*sCBC2P*GO*GMMB*GL1*GEQDB1BP
s**0 terms:
 + GO*GMMB*GL1*GEQDB1BP
************************************************
NUMERICAL VALUE OF ABOVE SYMBOLIC RESULT
+ 2.59155e-021 * s**2 + 4.19752e-005 * s**0
************************************************
Denominator of: v77
TERMS SORTED ACCORDING TO POWERS OF s
s**3 terms:
 + sLV2P*sCBCB*sCBC2P*GMMB*GL2*GL1
 + sLV2P*sCBCB*sCBC2P*GMMB*GL2*GEQDB1BP
 + sLV2P*sCBCB*sCBC2P*GMMB*GL1*GEQDB1BP
 + sLV2P*sCBCB*sCBC2P*GL2*GL1*GEQDB1BP
s**2 terms:
 + sLV2P*sCBCB*GO*GMMB*GL2*GL1 + sLV2P*sCBCB*GO*GMMB*GL2*GEQDB1BP
 + sLV2P*sCBCB*GO*GMMB*GL1*GEQDB1BP
 + sLV2P*sCBCB*GO*GL2*GL1*GEQDB1BP
 + sLV2P*sCBCB*GMMB*GL2*GL1*GEQDB1BP
 + sLV2P*sCBC2P*GO*GMMB*GL2*GL1
 + sLV2P*sCBC2P*GO*GMMB*GL2*GEQDB1BP
 + sLV2P*sCBC2P*GO*GMMB*GL1*GEQDB1BP
 + sLV2P*sCBC2P*GO*GL2*GL1*GEQDB1BP
s**1 terms:
 + sCBCB*GMMB*GL2*GL1 + sCBCB*GMMB*GL2*GEQDB1BP
 + sCBCB*GMMB*GL1*GEQDB1BP + sCBCB*GL2*GL1*GEQDB1BP
s**0 terms:
 + GO*GMMB*GL2*GL1 + GO*GMMB*GL2*GEQDB1BP
 + GO*GMMB*GL1*GEQDB1BP + GO*GL2*GL1*GEQDB1BP
************************************************
NUMERICAL VALUE OF ABOVE SYMBOLIC RESULT
+ 2.2391e-030 * s**3 + 1.52401e-020 * s**2 + 3.7632e-014 * s**1 +
0.000223999 * s**0
************************************************
```

Figure E-11: Sspice results

Class G Amplifier Vbias -6.232

```
[0  ] [-GO  sCBCB+GO 0        -sCBCB   0        0        0       ][V1 ]
[0  ] [0    -GMMB    Y 2,3    0        Y 2,5    0        0       ][V2 ]
[0  ] [0    Y 3,2    -GMMB    Y 3,4    0        0        1       ][V3 ]
[0  ]=[0    0        Y 4,3    0        Y 4,5    -GL1     0       ][V5 ]
[0  ] [0    0        0        0        -GL1     GL2+GL1  0       ][V12]
[1  ] [1    0        0        0        0        0        0       ][V77]
[0  ] [0    0        0        sLV2P+1  0        0        -sLV2P ][V79]

Y( 2,3 ) = +GMMB+GEQDB1BP
Y( 2,5 ) = -GEQDB1BP
Y( 3,2 ) = -sCBCB+GMMB
Y( 3,4 ) = +sCBCB+sCBC2P-1
Y( 4,3 ) = -GEQDB1BP
Y( 4,5 ) = +GL1+GEQDB1BP
*Ignore nodes 78 and higher if present. They are used for internal
numbering.

RESULTS APPROXIMATED USING A THRESHOLD MAGNITUDE OF: 0.90

Numerator of: v77
TERMS SORTED ACCORDING TO POWERS OF s
s**2 terms:
 + sLV2P*sCBC2P*GO*GEQDB1BP
s**0 terms:
 + GO*GEQDB1BP
************************************************
NUMERICAL VALUE OF ABOVE SYMBOLIC RESULT
+ 7.34566e-020 * s**2 + 0.00123456 * s**0
************************************************

Denominator of: v77
TERMS SORTED ACCORDING TO POWERS OF s
s**3 terms:
 + sLV2P*sCBCB*sCBC2P*GL2
s**2 terms:
 + sLV2P*sCBC2P*GO*GL2
s**1 terms:
 + sCBCB*GL2
s**0 terms:
 + GO*GL2
************************************************
NUMERICAL VALUE OF ABOVE SYMBOLIC RESULT
+ 2.6656e-029 * s**3 + 1.58666e-019 * s**2 + 4.48e-013 * s**1 +
0.00266666 * s**0
************************************************
```

Figure E-12: Sspice results

Appendix F

```
Class G Amplifier
V2  2 0  18
V1  3 0   6
V1P 4 0  -6
V2P 5 0 -18
*  Input Sources
VIN 1 0 DC 0V AC 1 SIN 0 {VAL} 1K
X1 0 10 2 5 11 LF411
RIN 1 10 1K
RF 19 10 1K
QA 2 11 12 Q2N3904
QB 5 11 12 Q2N3906
Q2 2 13 16 TIP31
Q1 16 15 19 TIP31
Q1P 21 18 19 TIP32
Q2P 5 20 21 TIP32
DB2   12 13 D1N4148
DB1A  12 14 D1N4148
DB1B  14 15 D1N4148
DB1AP 18 17 D1N4148
DB1BP 17 12 D1N4148
DB2P  20 12 D1N4148
D1 3  16 D1N5817
D2 21  4 D1N5817
RL 19 0 10
**********************************
*  Class B Amplifier for Comparison
VHIGH 200   0  18
VLOW  201   0 -18
XB    1   204 200 201 202 LF411
QH1   200 202 203 Q2N3904
QL1   201 202 203 Q2N3906
QH2   200 203 204 TIP31
QL2   201 203 204 TIP32
ROUT  204   0  10
**********************************
.PARAM VAL = 1
.STEP PARAM VAL 0 13.7 0.1
.TRAN 1U 3000U 0 1U
.LIB ECE402.LIB
.LIB DIODE.LIB
.LIB IC.LIB
.OP
.PROBE
.END
```

Figure F-1: PSpice circuit file

Total Harmonic Distortion Test Circuit

```
Class G Amplifier
V2  2 0  18
V1  3 0   6
V1P 4 0  -6
V2P 5 0 -18
*  Input Sources
VIN 1 0 DC 0V AC 1 SIN 0 13.7 1K
X1 0 10 2 5 11 LF411
*ICL8741
RIN 1 10 1K
RF 19 10 1K
CADD1 2 80 0.01U
RADD1 80 13 10
CADD2 5 81 0.01U
RADD2 81 20 10
QA 2 11 12 Q2N3904
QB 5 11 12 Q2N3906
Q2 2 13 16 TIP31
Q1 16 15 19 TIP31
Q1P 21 18 19 TIP32
Q2P 5 20 21 TIP32
DB2   12 13 D1N4148
DB1A  12 14 D1N4148
DB1B  14 15 D1N4148
DB1AP 18 17 D1N4148
DB1BP 17 12 D1N4148
DB2P  20 12 D1N4148
D1 3  16 D1N5817
D2 21  4 D1N5817
RL 19 0 10
.TRAN .1U 2000U 0U .1U
.LIB ECE402.LIB
.LIB DIODE.LIB
.LIB IC.LIB
.OP
.FOUR 1K 20 V(19)
.PROBE
.END
```

Figure F-2: PSpice circuit file

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(19)
DC COMPONENT = 8.462706E-05

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	1.370E+01	1.000E+00	1.800E+02	0.000E+00
2	2.000E+03	1.753E-04	1.280E-05	-8.597E+01	-4.459E+02
3	3.000E+03	8.606E-04	6.282E-05	1.013E+02	-4.387E+02
4	4.000E+03	1.780E-04	1.299E-05	8.965E+01	-6.303E+02
5	5.000E+03	8.551E-04	6.242E-05	7.761E+01	-8.223E+02
6	6.000E+03	1.703E-04	1.243E-05	-8.664E+01	-1.167E+03
7	7.000E+03	8.162E-04	5.958E-05	1.012E+02	-1.159E+03
8	8.000E+03	1.696E-04	1.238E-05	9.144E+01	-1.348E+03
9	9.000E+03	8.232E-04	6.009E-05	7.743E+01	-1.542E+03
10	1.000E+04	1.603E-04	1.170E-05	-8.601E+01	-1.886E+03
11	1.100E+04	7.902E-04	5.768E-05	1.003E+02	-1.879E+03
12	1.200E+04	1.569E-04	1.146E-05	9.354E+01	-2.066E+03
13	1.300E+04	8.129E-04	5.934E-05	7.784E+01	-2.262E+03
14	1.400E+04	1.463E-04	1.068E-05	-8.545E+01	-2.605E+03
15	1.500E+04	7.778E-04	5.677E-05	9.886E+01	-2.601E+03
16	1.600E+04	1.407E-04	1.027E-05	9.559E+01	-2.784E+03
17	1.700E+04	8.061E-04	5.884E-05	7.841E+01	-2.981E+03
18	1.800E+04	1.294E-04	9.449E-06	-8.501E+01	-3.325E+03
19	1.900E+04	7.624E-04	5.565E-05	9.704E+01	-3.323E+03
20	2.000E+04	1.224E-04	8.936E-06	9.769E+01	-3.502E+03

TOTAL HARMONIC DISTORTION = 1.814640E-02 PERCENT

Figure F-3: PSpice THD results

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(19)
DC COMPONENT = 7.012749E-05

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+04	1.370E+01	1.000E+00	1.798E+02	0.000E+00
2	2.000E+04	3.461E-04	2.526E-05	-1.297E+02	-4.893E+02
3	3.000E+04	8.629E-03	6.299E-04	1.005E+02	-4.390E+02
4	4.000E+04	6.546E-04	4.778E-05	-1.753E+02	-8.945E+02
5	5.000E+04	8.406E-03	6.135E-04	1.040E+02	-7.951E+02
6	6.000E+04	1.032E-03	7.535E-05	-1.452E+02	-1.224E+03
7	7.000E+04	8.101E-03	5.913E-04	1.125E+02	-1.146E+03
8	8.000E+04	1.316E-03	9.602E-05	-1.592E+02	-1.598E+03
9	9.000E+04	7.882E-03	5.753E-04	1.159E+02	-1.502E+03
10	1.000E+05	1.662E-03	1.213E-04	-1.393E+02	-1.937E+03
11	1.100E+05	7.697E-03	5.618E-04	1.247E+02	-1.853E+03
12	1.200E+05	1.910E-03	1.394E-04	-1.463E+02	-2.304E+03
13	1.300E+05	7.484E-03	5.462E-04	1.273E+02	-2.210E+03
14	1.400E+05	2.233E-03	1.630E-04	-1.300E+02	-2.647E+03
15	1.500E+05	7.303E-03	5.331E-04	1.356E+02	-2.562E+03
16	1.600E+05	2.418E-03	1.765E-04	-1.342E+02	-3.011E+03
17	1.700E+05	6.994E-03	5.105E-04	1.375E+02	-2.919E+03
18	1.800E+05	2.738E-03	1.999E-04	-1.204E+02	-3.357E+03
19	1.900E+05	6.763E-03	4.936E-04	1.457E+02	-3.271E+03
20	2.000E+05	2.852E-03	2.082E-04	-1.229E+02	-3.719E+03

TOTAL HARMONIC DISTORTION = 1.746231E-01 PERCENT

Figure F-4: PSpice THD results

Appendix G

```
Class G Amplifier with more biasing
V2  2 0  18
V1  3 0   6
V1P 4 0  -6
V2P 5 0 -18
*  Input Sources
VIN 1001 0 DC 0V AC 1 SIN 0 {VAL} 20K
E2 1 0 1001 0 .2
X1 0 10 2 5 11 LF411
*ICL8741
RIN 1 10 1K
RF 19 10 5k
*  Biasing Network
RBIAS 2 A 10K
DBIAS1 A AA D1N4148
DBIAS1A AA AAA D1N4148
DBIAS2 AAA 11 D1N4148
DBIASB 11 BBB D1N4148
DBIAS3 BBB BB D1N4148
DBIAS4 BB B D1N4148
RBIASP B 5 10K
X2 A 41 2 5 41 LF411
X3 B 42 2 5 42 LF411
QA 2 41 12 Q2N3904
QB 5 42 120 Q2N3906
CH1 2 22 0.01U
RH1 22 13 10
CH2 5 23 0.01U
RH2 23 20 10
Q2 2 13 16 TIP31
Q1 16 15 19 TIP31
Q1P 21 18 19 TIP32
Q2P 5 20 21 TIP32
DB2   12 13 D1N4148
DB1A  12 14 D1N4148
DB1B  14 15 D1N4148
DB1AP 18 17 D1N4148
DB1BP 17 120 D1N4148
DB2P  20 120 D1N4148
D1 3  16 D1N5817
D2 21  4 D1N5817
RL 19 0 10
**********************************
*  Class B Amplifier for Comparison
VHIGH 200   0  18
VLOW  201   0 -18
*E1 1000 0 1 0 10
XB    1001   204 200 201 202 LF411
QH1       200 202 203 Q2N3904
QL1    201 202 203 Q2N3906
QH2 200 203 204 TIP31
QL2 201 203 204 TIP32
ROUT  204   0  10
**********************************
*(AVG(V(19)*I(RL)))/(AVG(V(2)*-I(V2))+AVG(V(5)*-I(V2P))+AVG(V(3)*-
I(V1))+AVG(V(4)*-I(V1P)))
*YatX((AVG(V(19)*I(RL)))/(AVG(V(2)*-I(V2))+AVG(V(5)*-I(V2P))+AVG(V(3)*-
I(V1))+AVG(V(4)*-I(V1P))),3m)
*YatX((AVG(V(204)*I(Rout)))/(AVG(V(200)*-I(VHIGH))+AVG(V(201)*-I(VLOW))),3m)
```

```
.PARAM VAL = 1
.STEP PARAM VAL 0 13.8 0.1
.TRAN .1U 300U 0 .1U
.LIB ECE402.LIB
.LIB DIODE.LIB
.LIB IC.LIB
.OP
.FOUR 20K 20 V(19)
.PROBE V(19) I(RL) V(2) I(V2) V(5) I(V2P) V(3) I(V1) V(4) I(V1P) V(204) I(Rout)
+ V(200) I(VHIGH) V(201) I(VLOW) V(1001) V(1)
.END
```

Figure G-1: PSpice circuit file

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