ON THE DESIGN AND IMPLEMENTATION OF HIGH VOLTAGE GAIN MODULAR MULTILEVEL DC-DC CONVERTERS

By

Dennis K. Wey

A THESIS

Submitted to Michigan State University in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Electrical Engineering

2012

ABSTRACT

ON THE DESIGN AND IMPLEMENTATION OF HIGH VOLTAGE GAIN MODULAR MULTILEVEL DC-DC CONVERTERS

By

Dennis K. Wey

Switched capacitor DC-DC converters have features that make them ideal for many industries, including the aerospace and automotive industries. The converter solely relies on switches and capacitors to accomplish the energy transfer task. Additionally, this converter does not require the use of magnetic components to operate, thus enabling the switched capacitor circuit to be small, lightweight, and more immune to EMI problems, making it possible for the whole converter to be manufactured on a single IC chip.

This study develops the design and implementation of modular multilevel switched capacitor DC-DC converters. The converter takes two charge pump paths feed the load directly, leading to less power loss in the energy transfer, and making the output voltage almost ripple-free. The converter is suitable for high voltage gain applications. This study also investigates the feasibility of implementing the converter with output power of 200 W for the photovoltaic (PV) applications using the TSMC (Taiwan Semiconductor) T25HV process. A four-stage 8X converter has been developed and the circuit is fabricated in TSMC T25HV process. The simulation and experiment results are presented, and some issues regarding maximizing output power are also addressed.

ACKNOWLEDGEMENT

I would like to thank my advisor Dr. Fang Z. Peng, for his guidance and encouragement throughout the development of my thesis. I also extend thanks to my committee, Dr. Gregory M. Wierzba and Dr. Donnie K. Reinhard for their guidance and insight during the final stretch of completing my thesis. Additionally, I express my gratitude to Rickey Chen, whose efforts at CIC in Taiwan were invaluable for the layout and fabrication of the chip to be included in my thesis.

LIST OF T	ABLE	S	vi
LIST OF F	IGUR	ES	vii
Chapter 1	INT	RODUCTION	1
	1.1	Switched Capacitor DC-DC Converters	2
	1.2	Motivation	3
	1.3	Thesis Organization	4
Chapter 2	BAG	CKGROUND	5
	2.1	DC-DC Converters	6
	2.2	Switched Capacitor Converters	9
	2.3	Multilevel DC-DC Converters	11
		2.3.1 Flying-Capacitor DC-DC Converter	11
		2.3.2 Modular Multilevel Capacitor Clamped DC-DC Converter	15
Chapter 3	MU	LTILEVEL DC-DC CONVERTERS	18
	3.1	Multi-level DC-DC Converters	18
	3.2	Circuit Operation	20
		3.2.1 4X Converter	20
		3.2.2 6X Converter	23
		3.2.3 NX Converter	26
	3.3	Circuit Design and Simulation	26
		3.3.1 8X Converter Design	27
		3.3.2 Circuit Simulation	28
	3.4	Discussion	32
Chapter 4	DES	IGN AND IMPLEMENTATION	35
	4.1	Design Environment	35
	4.2	Circuit Design and Simulation	36
	4.3	Chip Implementation	42
	4.4	Chip Measurement	50
	4.5	Discussion	52
		4.5.1 One-Stage 2X Converter	53
		4.5.2 Performance Evaluation	58
		4.5.3 Increasing Voltage Gain Ratio	59
		4.5.4 Increasing Switch Area – Multiple Chips Solutions	62

TABLE OF CONTENTS

Chapter 5 CONC	LUSIONS AND FUTURE RESEARCH WORKS	66
APPENDICES		69
Appendix A SPICE	FILE USED FOR PRE-LAYOUT SIMULATION	70
REFERENCES		74

LIST OF TABLES

Table 2.1 Categories of DC-DC Converters	8
Table 2.2 Programmable Voltage Output of 3X FCC	14
Table 2.3 4-States of 4X MMCCC	16
Table 2.4 2-States of 4X MMCCC	
Table 3.1 Capacitor Voltage for 8X with m=32000	
Table 3.2 Output Performance for 8X with m=32000	
Table 4.1 Capacitor Voltage for 8X with m=10	40
Table 4.2 Capacitor Voltages (Pre-Layout Vs. Post-Layout)	
Table 4.3 Output Performance (Pre-Layout Vs. Post-Layout)	
Table 4.4 Design Specification	
Table 4.5 Summary – Capacitor Voltages	56
Table 4.6 Summary – Output Performance	
Table 4.7 Performance Comparison (Pre-Layout Simulation)	59
Table 4.8 Simulation Results – 8X with m=10	60
Table 4.9 Simulation Results – 12X with m=6	61
Table 4.10 Simulation Results – 14X with m=5	61
Table 4.11 Simulation Results – 8X with m=20	63
Table 4.12 Simulation Results – 8X with m=40	63

LIST OF FIGURES

Figure 2.1 Classification of DC-DC Converters	5
Figure 2.2 Boost Converter	6
Figure 2.3 Switched Capacitor Converters	9
Figure 2.4 Two Switch States for Boost Switched Capacitor Converter	10
Figure 2.5 FCC with a Voltage Conversion Ratio of 3	11
Figure 2.6 Switch States for 3X FCC	12
Figure 2.7 Switch States for 3X FCC for 2X	13
Figure 2.8 Switch States for 3X FCC for 1X	13
Figure 2.9 A Modular Multilevel Flying Capacitor Converter	14
Figure 2.10 MMCCC	14
Figure 3.1 N-Stage Modular Multilevel DC-DC Converters, HVGC	19
Figure 3.2 HVGC with 2 stages for 4X Conversion	21
Figure 3.3 Switch States of 4X	22
Figure 3.4 HVGC with 3 stages for 6X Conversion	24
Figure 3.5 Switch States of 6X	25
Figure 3.6 A Stage of HVGC	26
Figure 3.7 HVGC with 4 stages for 8X Conversion	27
Figure 3.8 Capacitor Voltage Waveforms for 8X with m=32000	
Figure 3.9 Waveforms for 8X with m=32000	
Figure 3.10 Switch Area vs. Output Voltages (Load=1 KΩ)	
Figure 3.11 Switch Area vs. Output Voltages (Load=32 Ω)	

Figure 4.1 PMOS Transistor as Switching Device	37
Figure 4.2 Capacitor Voltage Waveforms for 8X with m=10	39
Figure 4.3 Waveforms for 8X with m=10	41
Figure 4.4 Physical Layout of 8X Converter	43
Figure 4.5 HV Layout Design Rules	44
Figure 4.6 Output Voltage Waveforms in Post-Layout Simulation	46
Figure 4.7 Waveforms in Post-Layout Simulation	48
Figure 4.8 Agilent Measurement Instruments	50
Figure 4.9 Pin Assignment	51
Figure 4.10 Pre-layout Simulations - Output Voltage Waveforms for Single Stage	53
Figure 4.11 Waveforms in Pre-layout Simulation	54
Figure 4.12 Post-layout Simulations – Output Voltage Waveforms for Single Stage	55
Figure 4.13 Waveforms in Post-layout Simulation	56
Figure 4.14 8X Performance for various m	65

Chapter 1

INTRODUCTION

Power converters play an important role in Hybrid Electric Vehicle (HEV) systems [1-4]. A typical HEV drive train consists of a battery, power converter, and a traction motor to drive the vehicle. A power converter could be as simple as a traditional inverter or a DC-DC converter paired with an inverter. The latter configuration provides more flexibility and improves the system performance, where the DC-DC converter interfaces the battery and the inverter DC bus. The bus is usually a variable voltage converter so that the inverter can always operate at its optimum operating point [1]. In most commercially available systems, traditional boost converters are used, which requires the use of large inductors, a component which is often bulky, heavy, costly, and heat-prone. With the trend of higher coolant temperature of the converters in HEVs, as the only power magnetic component in the system, the DC-DC inductor becomes a major obstacle in further reducing converter size, weight, and cost.

Recent technological advancement of silicon carbide (SiC) devices and ceramic capacitors promise the availability of very high temperature components (above 250°C) with the exception of magnetic cores [2-5]. Thus, very high temperature operation of magnetic-less converters becomes possible and very attractive because natural air cooling can be adopted, reducing the size, weight, and the cost of the converter significantly.

1.1 Switched Capacitor DC-DC Converters

Switched capacitor DC-DC converters have been gaining popularity lately [6-15]. The most prolific example is the charge-pump circuit. These converters have features that make them ideal for many industries, including the aerospace and automotive industries [6]. This converter relies solely on switches and capacitors to accomplish the energy transfer task previously accomplished by inductors and/or capacitors in many switched-mode power converters. By controlling the time duration of charging and discharging of the capacitors, the switches and capacitors can form a switched-capacitor network that switches among different predetermined topological stages and provides a stable output to the load. Because no magnetic devices are needed, the switched capacitor circuit features small size, light weight, has fewer electromagnetic interference (EMI) issues and makes it possible for the whole converter to be manufactured on a single integrated circuit (IC) chip.

Recently, multilevel DC-DC converters [4,5,16-20] have been developed to reduce the inductance requirement in DC-DC converters and to achieve higher power density and higher efficiency than conventional DC-DC converters. Among them, a magnetic-less flying-capacitor DC-DC converters [4] is capable of flexible voltage ratios with small component count and lower low voltage stress across the switching devices; a modular multilevel capacitor clamped DC-DC converter [21] offers many advantageous features, such as high frequency operation capability, low input/output current ripple, low on-state voltage drop, and bi-direction power flow management. A multilevel DC-DC converter [22] reduces the device count, capacitor voltage rating, and power loss with very low total device power rating, and it is suitable for high voltage gain applications.

1.2 Motivation

The switched capacitor converters renounce the use of any magnetic element and rely solely on switches and capacitors to accomplish energy transfer [6]. Due to the lack of magnetic devices, the switched capacitor circuit features small size and light weight, and makes it possible for the whole converter to be manufactured on a single IC chip.

Targeting the consumer, automotive, and industrial markets, BCD (Bipolar-CMOS-DMOS) process technology offers a cost-effective solution for a broad range of power management and smart-power applications. The BCD process technology integrates transistor devices, such as Bipolar, CMOS (complementary metal-oxide-semiconductor) and LDMOS (lateral double-diffused MOS), into one chip so as to form a Smart Power integrated circuit, a term which refers to the combined manufacture of control and power circuits on one chip. The high voltage process current available for us to access is the TSMC (Taiwan Semiconductor) 0.25um CMOS high voltage mixed signal based on BCD 1P5M SALICIDE 2.5/5/60V, referred to as T25HV process. The process permits designers to fabricate analog and mixed-signal integrated circuits operating up to 60V.

This study attempts to investigate the feasibility of implementing the modular multilevel switched capacitor DC-DC boost converter with a voltage conversion of NX [22] using the TSMC T25HV process. The implementation targets to a 200 W DC-DC converter for the photovoltaic (PV) applications. Due to the limitation of the core size (1.9x1.9 mm²), this study is to design and fabricate a chip based on the constraints of core size and process technology. Several issues will be addressed in this study, including the whether or not realizing 200 W physically possible with T25HV process, and evaluating several strategies for maximizing power efficiency.

1.3 Thesis Organization

Chapter 2 reviews the categories of DC-DC converters and addresses the design issues for the modular multilevel DC-DC converters. Chapter 3 presents the design and implementation of the modular multilevel switched capacitor DC-DC boost converter, and discusses some design and implementation issues for multi-level DC-DC converters. The optimal voltage conversion ratio for the converter is also analyzed. Chapter 4 briefly describes the TSMC T25HV process and some design experiences. The details of the pre-layout and post-layout simulations of the circuit implementation are also presented with the chip layout. The measurement results of the fabricated chip will be shown. The chapter also addresses the issues of how to maximize the power efficiency. Finally, the conclusions and future research works are given in Chapter 5.

Chapter 2

BACKGROUND

A DC-DC converter is an electronic circuit which converts a source of DC from one voltage level to another. The converter generally can be classified into two categories [23]: (1) Linear regulator; and (2) Switching regulator, as shown in Figure 2.1. Based on the usage of inductors, the switching regulator can be divided into two types: (a) Inductor-based switching regulator; and (b) Inductorless (switched capacitor).

This chapter reviews typical DC-DC converters, switched capacitor converters, and modular multilevel DC-DC converters.



Figure 2.1 Classifications of DC-DC Converters. For interpretation of the references to color in this and all other figures, the reader is referred to the electronic version of this thesis.

2.1 DC-DC Converters

DC-DC converters can be classified into three categories: (a) Buck converter; (b) Boost Converter; and (c) Buck-Boost Converter. Table 2.1 summarizes the architecture and voltage conversion ratio M(D) as function of the duty cycle D for these three types of DC-DC converter

The boost converter is used to transfer a lower input voltage to a higher output voltage. Figure 2.2(a) shows a boost converter, where the switch S is used to control the switch state, thus determining the direction of the energy to be stored or transferred; the inductor L is used to transfer and store the energy and to filter AC current noise signals. The switching device S can be realized by a power transistor (BJT or MOSFET) and a diode, as shown in Figure 2.2(b).





Figure 2.2 Boost Converter: (a) with Ideal Switch; (b) Switch is realized by Transistor and Diode D₁; (c) M_p is On; and (d) M_p is OFF.

When the power transistor M_p is turned on, as shown in Figure 2.2(c), the input voltage V_{in} transfers its energy to the inductor. When M_p is turned off, as shown in Figure 2.2(d), the inductor and diode form a loop, and the inductor releases the stored energy to the load. At this moment, the release of energy stored by the inductor reverses the polarity of VL, and both input and the inductive voltages charge up the capacitor such that the output voltage equals to twice of the input voltage. Let D denote the duty cycle of the clock signal applied to the switch. Assuming that there is no voltage drop across the diode:

$$V_{in} = (1-D) V_{out}$$
 (2.1)

Thus, the voltage conversion ratio M(D) is:

$$M(D) = V_{out}/V_{in} = 1 / (1-D)$$
(2.2)

It should be mentioned that the use of larger capacitor results in a smaller output voltage ripple and more stable output voltage at the cost of large chip area. On the other hand, the smaller capacitor can reduce the area significantly at the cost of requiring higher switching frequency. The higher frequency may increase the switching loss and decrease the conversion efficiency. Thus, there exist design trade-offs among inductor and capacitor size, switching frequency, and output voltage/current.

A switching regulator offers the advantage of achieving higher efficiency for both buck and boost converters, but requires the use of inductors which take up larger chip area and generally must be connected externally for integrated circuits. In such implementations, the circuit must be designed to tolerate the voltage ripple.



Table 2.1 Categories of DC-DC Converters.

2.2 Switched Capacitor Converters

The switched capacitor DC-DC converter, also called a charge pump converter, is comprised of switches and capacitors used for the storage and transfer of energy [4,5,16-20,24]. By turning switches on and off to change the connection of capacitors, energy can be directed through the capacitor network appropriately in order to control the amount of energy delivered to the output.

Figure 2.3(a) shows a typical switched capacitor converter which is comprised of four switches (S_1 , S_2 , S_3 , and S_4) and one capacitor (C_1). A set of complementary signals are used to control the switches, where one signal controls S_1 and S_3 , and the complementary signal control S_2 and S_4 . Figures 2.3(b) and 2.3(c) illustrate the boost-type and buck-type switched capacitor converters, respectively.



Figure 2.3 Switched Capacitor Converters: (a) Basic Structure; (b) Boost; and (c) Buck.

Consider the boost-type switched capacitor converter in Figure 2.3(b). Both S₂ and S₄ are turned on and both S₁ and S₃ are off, as shown in Figure 2.4(a), the converter is equivalent to the circuit on the right-hand side, where the input voltage charges up the capacitor C₁. On the other hand, Both S₁ and S₃ are turned on and both S₂ and S₄ are off, as shown in Figure 2.4(b), Vin and C₁ charge up the output capacitor C₀, i.e., V_{in} + V_{C1} \rightarrow V_{C0}. Since V_{C1}=V_{in} in the first state, V_{C0}=V_{in}+V_{C1}=2*V_{in}.





Figure 2.4 Two Switch States for Boost Switched Capacitor Converter.

2.3 Multilevel DC-DC Converters

Two modular multilevel DC-DC converters are reviewed in this section: (a) Flying capacitor DC-DC Converter (FCC) [4]; and (b) Modular multilevel capacitor clamped DC-DC converter (MMCCC) [21].

2.3.1 Flying-Capacitor DC-DC Converter

Unlike conventional DC-DC converters, which take a fixed input voltage and generate a pre-determined constant output voltage, the FCC with a voltage conversion ratio of 3, as shown in Figure 2.5, takes an input voltage of V_{in} and produces 3V_{in}.



Figure 2.5 FCC with a Voltage Conversion Ratio of 3.

Similar to the switched capacitor converter described previously, the input voltage V_{in} charges up the capacitor C₁, i.e., V_{in} \rightarrow C₁, in the first state. Then the capacitor C₂ is charged up by both V_{in} and the charges stored in C₁, i.e., V_{in}+ C₁ \rightarrow C₂, in the second state. Finally, the capacitor C₃ is charged by Vin and C₂, i.e., V_{in}+ C₂ \rightarrow C₃, in the third state. Once the output

voltages are stable, $V_{in} \rightarrow C_1$ results in $V_{C1}=V_{in}$; $V_{in}+C_1 \rightarrow C_2$, implying that $V_{C2}=V_{in}+V_{C1}=2V_{in}$; it follows from $V_{in}+C_2 \rightarrow C_3$ that $V_{C3}=V_{in}+V_{C2}=3V_{in}$. Figure 2.6 illustrates the three switch states. In Switch State I, as shown in Figure 2.6(a), switches S_{1p} , S_{2n} , and S_{3n} are on, and the remaining switches are off, so that $V_{in} \rightarrow C_1$. In Switch State II, as shown in Figure 2.6(b), switches S_{1n} , S_{2p} , and S_{3n} are on, and the remaining switches S_{1n} , S_{2p} , and S_{3n} are on, and the remaining switches S_{1n} , S_{2p} , and S_{3n} are on, and the remaining switches S_{1n} , S_{2n} , and S_{3p} are on, and the remaining switches are off, so that $V_{in}+C_1 \rightarrow C_2$; Finally, as shown in Figure 2.6(c) for Switch State III, switches S_{1n} , S_{2n} , and S_{3p} are on, and the remaining switches are off, so that $V_{in}+C_2 \rightarrow C_3$.



Figure 2.6 Switch States for 3X FCC: (a) State I; (b) State II; and (c) State III.

In fact, with different setting of switches, the output of the 3X FCC can also produce V_{in} and $2V_{in}$, given the input voltage V_{in} .

Figure 2.7 illustrates that the switching states for generating $2V_{in}$. Similar to previous description, the first switch state, $V_{in} \rightarrow C_1$, where the switches S_{1n} and S_{2p} are off, and the remaining switches are on, as shown in Fig. 2.7(a); and in switch state II, $V_{in+} C_1 \rightarrow C_3$, where

the switches S_{1p} and S_{2n} are off, and the remaining switches are on, as shown in Figure 2.7(b). Thus, $V_{C3}=V_{in}+V_{C1}=2V_{in}$.



Figure 2.7 Switch States for 3X FCC for 2X: (a) State I; and (b) State II.

Similarly, Fig. 2.8 shows the 3X FCC generates V_{in} . The switch state is $V_{in} \rightarrow C_3$, where the switches S_{1n} is off, and the remaining switches are on. Thus,, $V_{C3}=V_{in}$.



Figure 2.8 Switch States for 3X FCC for 1X.

Table 2.2 summarizes the salient feature of the 3X FCC which is the ability to generate various output voltages, i.e., Vin, 2Vin, and 3Vin.

Vout	Switch State	Operations	S _{1n}	S _{2n}	S _{3n}	S _{1p}	S _{2p}	S _{3p}
	Ι	$V_{in} \rightarrow C_1$	off	on	on	on	off	off
3V _{in}	II	$V_{in}+C_1 \rightarrow C_2$	on	off	on	off	on	off
	III	$V_{in}+C_2 \rightarrow C_3$	on	on	off	off	off	on
214	Ι	$V_{in} \rightarrow C_1$	off	on	on	on	off	off
\angle v in	II	$V_{in}+C_1 \rightarrow C_3$	on	off	off	off	on	on
Vin	Ι	$V_{in} \rightarrow C_3$	off	off	off	on	on	on

Table 2.2 Programmable Voltage Output of 3X FCC.

Fig. 2.9 illustrates a modular multilevel FCC, where each module takes two switches and one capacitor. The modular multilevel FCC can be developed for any output/input boost ratio (hence, NX). This magnetic-less FCC is capable of flexible voltage ratios with small component count and lower voltage stress across the switching devices [4]. However, when it comes to high voltage conversion ratios, it has its practical limits. For NX conversion, the input current has to go through N switching devices. The resultant voltage drop and power loss soon overshadows the advantages present at lower voltage ratios.



Figure 2.9 A Modular Multilevel Flying Capacitor Converter.

2.3.2 Modular Multilevel Capacitor Clamped DC-DC Converter

Figure 2.10(a) illustrates the MMCCC with NX conversion, where each module is comprised of three switches and a capacitor.



Figure 2.10 A MMCCC: (a) NX [22]; and (b) 4X [21].

Consider the 4-stage MMCCC which is comprised of 3 stages of the MMCCC modules and a stage with a switch (S_{4a}) and output capacitor C4. Similar to the operation of FCC, the 4stage MMCCC generates $4V_{in}$ with the switching states shown in Table 2.3.

Switc State	h Operations	S _{1n}	S _{2n}	S3n	S _{1p}	S _{2p}	S3p	S _{1a}	S _{2a}	S3a	S4a
Ι	$V_{in} \rightarrow C_1$	on	off	off	off	off	off	on	off	off	off
II	$V_{in+} C_1 \rightarrow C_2$	off	on	off	on	off	off	off	on	off	off
III	$V_{in+} C_2 \rightarrow C_3$	off	off	on	off	on	off	off	off	on	off
IV	$V_{in+} C_3 \rightarrow C_4$	off	off	off	off	off	on	off	off	off	on

Table 2.3 4-States of 4X MMCCC.

Note that Switch States I and III in Table 2.3 can be merged to one state, while Switch States II and IV can also be merged to one state, as shown in Table 2.4. Interestingly, the switching signals in both Switch State are complementary to each other

Table 2.4 2-States of 4X MMCCC.

Switch State	Operations	S _{1n}	S2n	S3n	S1p	S _{2p}	S3p	S1a	S2a	S3a	S4a
Ι	$V_{in} \rightarrow C_1 \& \\ V_{in} + C_3 \rightarrow C_3$	on	off	on	off	on	off	on	off	on	off
II	$V_{in+} C_1 \rightarrow C_2 \&$ $V_{in+} C_3 \rightarrow C_4$	off	on	off	on	off	on	off	on	off	on

Compared to the FCC, the MMCCC has significant improvements [21]: (1) the current needed to charge a capacitor flows through at most 3 switching devices, regardless of voltage ratio; (2) the average current through the switching devices and capacitors reduces to roughly 2/N times the average component current in FCC for a voltage ratio of N. However, the component count is increased. The NX MMCCC requires (3N-2) switching devices, while the NX FCC takes only (2N). The extra (N-2) switching devices have to sustain the voltage stress of twice the input voltage when the converter operates in boost mode.

As illustrated in Table 2.4, switch S_{ja} (j=1,2,3,4) creates a path to charge the capacitor C_j , where C_1 is charged directly from the input voltage, while other capacitors C_j (j=2,3) is charged from the input voltage and the capacitor C_{j-1} . Switches Sjp and Sjn are controlled by the complementary signals and connected in series with the input voltage source, the structure creates the independent current paths. As a result, the four states in Table 2.3 can be merged to two states in Table 2.4, and the MMCCC has a shorter current path than the FCC.

Chapter 3

MULTILEVEL DC-DC CONVERTER

This Chapter first presents the design and simulation of the multi-level DC-DC converter with high voltage gain in [22]. Section 3.2 describes the circuit structure and the operation principles for 4X, 6X, and NX conversions. Section 3.3 shows the design and simulation results, where the TSMC 0.25um CMOS high voltage mixed signal based on BCD 1P5M SALICIDE 2.5/5/60V, referred to as T25HV process, is used to implement the converter. Finally, Section 3.4 discusses some issues on design and implementation of multi-level DC-DC converters.

3.1 Multi-level DC-DC Converters

Chapter 2 has reviewed the structure and the operations of two multi-level DC-DC converters: a magnetic-less flying-capacitor DC-DC converter (FCC) [4] and a modular multilevel capacitor clamped DC-DC converter (MMCCC) [21]. The FCC achieves the NX conversion with small component count and low voltage stress across the switching devices. However, the input current must pass through N switching devices. The resultant voltage drop and power loss overshadow the advantages present at small N [22]. On the other hand, the current needed to charge the capacitor in MMCCC flows through at most 3 switching devices regardless of N, leading to the reduced total device power rating (TDPR).

For a given input voltage V_{in} , the N-stage FCC and MMCCC achieve output voltage of N*V_{in}. However, the N-stage HVGC, as shown in Figure 3.1 results in an output voltage of 2N*V_{in}.



Figure 3.1 N-Stage Modular Multilevel DC-DC Converters, HVGC. [22]

The HVGC has its unique features, compared to the original MMCCC with a voltage ratio of NX [22]:

- Two charge pump paths feed the load directly, leading to less power loss in the energy transfer;
- (2) Half of the capacitors reduced their voltage by (N/2)*Vin. Multilevel DC-DC converters rely on capacitors to transfer energy and to filter the output voltage. Normally the larger equivalent series resistance (ESR) associated with the higher capacitor voltage rating lowers the efficiency;
- (3) The output voltage ripples are reduced given the same capacitance as in the MMCCC, due to the interleaved charge/discharge of two output capacitors. The sum of the complementary voltage ripples makes the output voltage almost ripple-free;
- (4) Employs fewer switches with no penalty to total device power rating. The associated gate drive and accessory power supply are saved accordingly; and

(5) Each pair of complementary switching devices is truly capacitor-clamped. This is a virtue for designing a high power converter without assistance from extra clamping circuits.

3.2 Circuit Operations

This section describes the circuit operation for HVGC with voltage conversion ratios of four, six, and N, i.e., 4X, 6X, and NX conversions. In other words, the boost converter will generate 4-, 6-, and N-times of the input voltage, respectively. The circuit can also function as a buck converter when the energy flows in the opposite direction.

3.2.1 4X Converter

Figure 3.2(a) shows the HVGC with two stages for a voltage conversion ratio of 4. The converter alternates between two switching states as illustrated in Figure 3.2(b), Figure 3.2(c) tabulates the switch states, where the signals in both switch states are complementary clock signals with 50% duty cycle, as shown in Figure 3.2(d).



(a)

Swit	ch State I	Switch State II				
Capacitor Charge Paths On-state Switches		Capacitor Charge Paths	On-state switches			
$V_{in} \rightarrow C_{1a}$	S _{1a} ,S _{1n}	$V_{in} \rightarrow C_{1b}$	S _{1b} ,S _{1p}			
$\begin{array}{c} C_{1b}+V_{in} \rightarrow \\ C_{2b} \end{array}$	S2b,S2p,S1n	$\begin{array}{c} C_{1a}+V_{in} \rightarrow \\ C_{2a} \end{array}$	S _{2a} ,S _{2n} ,S _{1p}			

(b)

$ \begin{array}{ c c c c c c c c } I & V_{in} \rightarrow C_{1a} \& \\ C_{1b} + V_{in} \rightarrow C_{2b} \end{array} & \text{on off on off on off on off on off on} \end{array} \\ \hline II & V_{in} \rightarrow C_{1b} \& \\ C_{1a} + V_{in} \rightarrow C_{2a} \end{array} & \text{off on off on off on off on off on off} \end{array}$	Switch State	Operations	S _{1n}	S _{1p}	S _{1a}	S _{1b}	S _{2n}	S _{2p}	S _{2a}	S _{2b}
II $V_{in} \rightarrow C_{1b} \& \\ C_{1a}+V_{in} \rightarrow C_{2a} $ off on off on on off on off on off	Ι	$V_{in} \rightarrow C_{1a} \& \\ C_{1b} + V_{in} \rightarrow C_{2b}$	on	off	on	off	off	on	off	on
	II	$V_{in} \rightarrow C_{1b} \& \\ C_{1a} + V_{in} \rightarrow C_{2a}$	off	on	off	on	on	off	on	off

(c)



(d)

Figure 3.2 HVGC with 2 stages for 4X Conversion.

Figure 3.3 shows equivalent circuits for both switch states, where the switching devices marked in solid lines are on-state devices; the remaining switching devices in dashed lines are off-state devices. Switches S_{1a} (S_{2a}) and S_{1b} (S_{2b}) are complementary, while S_{1p} (S_{2p}) and S_{1n} (S_{2n}) are also complementary. In Switch State I, switches S_{1a} and S_{1n} are on to transfer the energy from input voltage V_{in} to the capacitor C_{1a} , as shown in Fig. 3.3(c) and marked in green. Then, switches S_{2b} and S_{2p} are turned on with the on-state switch S_{1n} to transfer the energy from V_{in} and C_{1b} to C_{2b} , as marked in blue.



Figure 3.3 Switch States of 4X: (a)&(c) Switch State I; and (b)&(d) Switch State II. For interpretation of the references to color in this and all other figures, the reader is referred to the electronic version of this thesis.

Note that switches S_{1b} , S_{1p} , S_{2a} , and S_{2n} are off in this switch state. On the other hand, in Switch State II, the complementary switch states are applied. Similarly, the switch states for the two steps in Figure 3.2(b) are illustrated in Figure 3.3(d).

In Switch State I, the capacitors C_{1a} and C_{2b} are charged, while C_{1b} is discharged. The capacitor C_{2a} is then discharged by the load current. On the other hand, the capacitors C_{1b} and C_{2a} are charged and C_{1a} is discharged in Switch State II, where the capacitor C_{2b} is discharged by the load current. Combining the voltage relations in these two switching states and neglecting the voltage drop, one can get $V_{C2a}=V_{C2b}=2V_{in}$, i.e., $V_{out}=4V_{in}$, thus demonstrating that the converter in Figure 3.2(a) is a 4X converter.

3.2.2 6X Converter

Figure 3.4(a) shows the HVGC with three stages for a voltage conversion ratio of 6. The converter alternates between two switching states as illustrated in Figure 3.4(b). Figure 3.5 shows the equivalent circuits for both switch states. In the first step of Switch State I, switches S_{1a} and S_{1n} are on to transfer the energy from input voltage V_{in} to the capacitor C_{1a} , as shown in Fig. 3.5(c) and marked in green. Then, switches S_{3a} , S_{3n} , and S_{2p} are turned on to transfer the energy from V_{in} and C_{2a} to C_{3a} , as marked in blue. Finally, switches S_{2b} and S_{2p} are turned on with the on-state switch S_{1n} to transfer the energy from V_{in} and C_{1b} to C_{2b} , as marked in red. On the other hand, in Switch State II, the complementary switch states are applied. Similarly, the switch states for the two steps in Figure 3.4(b) are illustrated in Figure 3.5(d).

In Switch State I, the capacitors C_{1a} , C_{2b} , and C_{3a} are charged, while C_{1b} and C_{2a} are discharged. The capacitor C_{3b} is discharged by the load current. On the other hand, the capacitors C_{1b} , C_{2a} , and C_{3b} are charged and C_{1a} and C_{2b} are discharged in Switch State II,

where the capacitor C_{3a} is discharged by the load current. One can get $V_{C3a}=V_{C3b}=3V_{in}$, i.e., $V_{out}=6V_{in}$. This concludes the converter in Figure 3.4(a) is a 6X converter.



Figure 3.4 HVGC with 3 stages for 6X Conversion.



Figure 3.5 Switch States of 6X: (a)&(c) Switch State I; and (b)&(d) Switch State II.

Figure 3.6 shows one stage of the HVGC with a voltage conversion ratio of 2. With the N stages, as shown in Figure 3.1, the HVGC achieves a voltage conversion ratio of 2N. The converter alternates between Switch States I and II, with 50% duty cycle for each state. If N is even, the capacitors C_{Na} and C_{Nb} are discharged by load current in Switch State I and II, respectively, and V_{CNa}=V_{CNb}=2N*V_{in}. Thus, the converter achieves a voltage ratio of 2N. On the other hand, if N is odd, capacitors C_{Nb} and C_{Na} are discharged by load current in Switch State I and II, state I and II, respectively. Similarly, the converter achieves a voltage ratio of 2N.



Figure 3.6 A Stage of HVGC. [22]

3.3 Circuit Design and Simulation

The design task is to develop a boost DC-DC converter with an output rating of 200W, suitable for photovoltaic (PV) applications. With an input voltage of 10 V, the converter will produce an output voltage of 80 V with the output current of 2.5 A. Thus, an HVGC with a voltage conversion ratio of 8 is employed, where the stage capacitor of 150 uF is used, and operated at a frequency of 600~1000 KHz with 50% duty cycle. This section presents the circuit design and simulation results based on the above design specification.

Based on the design specification, the input and output voltages are 10 V and 80 V, respectively. This implies a voltage conversion ratio of 8. Thus, 4 stages of the HVGC are cascaded as shown in Figure 3.7(a), where the complementary switching states are illustrated in Figure. 3.7(b).



Figure 3.7 HVGC with 4 stages for 8X Conversion.

In Switch State I, the capacitors C_{1a} , C_{2b} , C_{3a} , and C_{4b} are charged, while C_{1b} , C_{2a} , and C_{3b} are discharged. The capacitor C_{4a} is discharged by the load current. On the other hand, the capacitors C_{1b} , C_{2a} , C_{3b} , and C_{4a} are charged and C_{1a} , C_{2b} , and C_{3a} are discharged in Switch State II, where the capacitor C_{4b} is discharged by the load current. Thus, $V_{C4a}=V_{C4b}=4V_{in}$, i.e., $V_{out}=8V_{in}$, and the output voltage of 80 V can be obtained with the input voltage of 10 V.

3.3.2 Circuit Simulation

The stage capacitances used are 150 μ F using ideal capacitors, and the resistive load is 32 Ω . The PMOS transistor size of W/L= 900 μ m/800nm is selected with m=32000, i.e., each switching device is comprised of 32000 PMOS transistors with the above size and they are connected in parallel. The best switching frequency is from 600 to 1000 KHz.



Figure 3.8 Capacitor Voltage Waveforms for 8X with m=32000 (f=50 kHz, T=2us/div): (a) Stage #1; (b) Stage #2 (c) Stage #3; and (d) Stage #4.
Figure 3.8 cont'd:



Fig. 3.8 shows the simulation results of waveforms for the voltage across the capacitors in various stages of the converter. The values are tabulated in Table 3.1.

Vc1a=Vc1b	9.932 V ~ 9.964 V
Vc2a=Vc2b	19.840 V ~ 19.874 V
Vc3a=Vc3b	29.748 V ~ 29.748 V
Vc4a=Vc4b	39.682 V ~ 39.702 V

Table 3.1 Capacitor Voltages for 8X with m=32000.

Figure 3.9 plots the waveform for input/output currents/voltages. Results show that the input voltage and current are 10 V and 19.5 A, respectively, and the output voltage and current The 79.38 respectively. are V and 2.481 A, 8X converter only achieves Vout/Vin=79.38/10=7.938 times. The output current is reduced from 20 A to 2.481 A. The voltage conversion efficiency is 79.38/80=99.225 %.



(a)

Figure 3.9 Waveforms for 8X with m=32000:

(a) Input Voltage; (b) Output Voltage; (c) Input Current; and (d) Output Current.

Figure 3.9 cont'd



(b)



(c)

Figure 3.9 cont'd:



Table 3.2 Output Performance for 8X with m=32000.

Vin	Vout	Iin	Iout	Efficiency
10 V	79.38 V	20 A	2.481 A	99.225%

3.4 Discussion

Figure 3.10 shows the output voltage of the 8X converter with the input voltage of 10 V for various m values. Simulation results show that when the PMOS transistor dimension is $W/L=800\mu/800n$, m=10, an output voltage of 47.3 V is obtained implying a voltage conversion efficiency of approximately 60%. As m increases, the output voltage also increases. For example, m=70, the output voltage is 72.8 V which implies that a voltage conversion efficiency of 91% is achieved. Similarly, the output voltage increases to 77.8 V, or 97.25 efficiency, with m=250. When m is doubled, i.e., m=500, the output voltage is 78.9 V, or 98.625% in efficiency. The efficiency improvement is approximately 0.1375%. When the output voltages are 79.4 V

and 79.6 V for m=1000 and 2000, respectively, their efficiencies are 99.25% and 99.5%, respectively. With the difference of 1000 for m, the efficiency improvement is only 0.25%. Thus, there exists a design trade-off between the transistor size and the conversion efficiency.



Figure 3.10 Switch Area vs. Output Voltages. (With PMOS Transistor 800u/800n and Load=1 K Ω .)

The simulation results in Table 3.2 are for the 8X converter with an input voltage of 10 V, load resistance of 32 Ω , PMOS transistor size W/L= 900u/800n, m=32000. Results show that the output voltage is V_{out}=79.4 V, as plotted in Fig. 3.11. When PMOS transistors are used as the switching devices, the larger transistor size can pass more current and results in a larger output voltage. As m=2000, the output voltage drops to 73 V, i.e., 91.25% efficiency. When m value is doubled, i.e., m=4000, the output voltage is 76.3 V, or 95.4% efficiency. Diminishing returns in efficiency are apparent as m is increased from 2000 to 4000, where efficiency gains are limited to near 4.2%



Figure 3.11 Switch Area vs. Output Voltages. (With PMOS Transistor 900u/800n, and Load=32 Ω .)

Chapter 4

DESIGN AND IMPLEMENTATION

This chapter describes the design and chip implementation of the 8X boost DC-DC converter, utilizing the TSMC T25HV process is implemented. Section 4.1 briefly describes the BCD process and the design environment; Section 4.2 presents the design and simulation of the 8X converter under the design environment; Section 4.3 discusses the chip implementation and Section 4.4 shows the measurement results; Finally, Section 4.5 addresses some implementation issues presented by the design environment.

4.1 Design Environment

Targeting the consumer, automotive, and industrial markets, BCD (Bipolar-CMOS-DMOS) process technology offers a cost-effective solution for a broad range of power management and smart-power applications. The BCD process technology integrates transistor devices, such as Bipolar, CMOS and LDMOS (lateral double-diffused MOS), into one chip so as to form a Smart Power integrated circuit. The main function of a Bipolar device is to provide high-frequency and high-drive current to meet the needs of the circuit. The robust high voltage DMOS capability provides MOSFET switch integration to reduce the Bill of Materials (BOM). The process permits designers to fabricate analog and mixed-signal integrated circuits operating at up to 60V. Recently, a broad range of proprietary IP blocks, based on TSMC's 0.25um BCD process nodes, have already been developed by many IP providers for the next generation PMICs.

The TSMC 0.25um CMOS high voltage mixed-signal process supports:

- 1P5M (Single poly, 5 metal layers)
- Salicide (Self-Aligned Silicidation)
- AL technology
- 2.5V core, 5V I/O's, and 60V high voltage
- 30KÅ thick top metal
- 1fF/mm² MIM (Metal-insulator-metal) Capacitor

The process supports the following components: MOS, BJT, Diode (Schottky and Zener), Resistor ($1K\Omega$ /square), and capacitor.

The design environment includes

- Process Design Kit (PDK): Calibre DRC/LVS/RC extraction command file; HSpice/Spectre model; P-cell & library; Virtuoso Techfile; and Laker Techfile
- Design rules: Layer definition; Layout rule; Mask definition; and Model description
- 60V N/PMOS Power cell: Layout; and Measurement result

4.2 Circuit Design and Simulation

Consider the multi-level switched-capacitor boost DC-DC converter, as shown in Figure 3.7(a), the 8X converter is comprised of switching devices and capacitors. The 8X converter contains four stages of the modules, where the output voltage of each module is increased to

twice that of the input voltage. The converter design is designed and implemented under two constraints: (a) PMOS transistor characteristics; and (b) limitation on chip dimension.

Due to the non-symmetrical structure of the PMOS transistors in T25HV process, the PMOS transistor, as a switching device, cannot be completely turned off. In order to prevent the current flowing from the load to the power supply, the switching device in this implementation is made of two PMOS transistors which are connected back-to-back, as shown in Figure 4.1. With such switching devices, the power supply can be isolated from the load to completely protect the power supply. The shuttle service provides the package with the core size of $1.9 \text{mm} \times 1.9 \text{mm}$. In general, the core size can contain roughly 300 PMOS transistors, depending on how they are laid out. For the 8X converter, it is comprised of 32 PMOS transistors. Thus, the following simulation assumes that the PMOS transistor size is W/L=750m/800nm and m=10, and the external capacitance is 10 uF.



Figure 4.1 PMOS Transistor as Switching Device.

The 8X converter is simulated with the following parameters: $V_{in}=2$ V, capacitances $C_{ia}=C_{ib}=10$ uF, i=1, 2, 3, and 4, and the load resistance = 1 K Ω . The complementary signals are applied as described in Fig. 3.2(c), where the clock frequency is 50 KHz. Fig. 4.2 shows the simulation results with the waveforms for the voltage across the capacitors in various stages of the converter. Results show that the voltage across V_{c1a} (V_{c1b}) is 1.397~1.416V, as tabulated in Table 4.1; similarly, the voltages across V_{c2a} (V_{c2b}), V_{c3a} (V_{c3b}), and V_{c4a} (V_{c4b}) are

2.407~2.426V, 3.416~3.435V, and 4.630~4.639V, respectively. Fig. 4.3 plots the waveform for input/output currents/ voltages. Results show that the input voltage and current are 2 V and 74.25 mA, respectively, and the output voltage and current are 9.27 V and 9.27 mA, respectively. Due to implementation constraints with the small m value, i.e., m=10, in this simulation, the 8X converter only achieves $V_{out}/V_{in}=9.27/2=4.64$. The output current is reduced from 74.25 mA to 9.27 mA, i.e., $I_{out}/I_{in} \approx 1/8$. The voltage conversion efficiency is approximately 50%. Interestingly, for the ideal case of 8X, the voltage conversion ratio is 8, while the current conversion ratio is 1/8. Thus, the voltage conversion efficiency is equivalent to the power conversion efficiency. The term "efficiency" is then calculated from the ratio V_{out}/V_{in} .



Figure 4.2 Capacitor Voltage Waveforms for 8X for m=10 (f=50 kHz, T=2us/div): (a) Stage #1; (b) Stage #2; (c) Stage #3; and (d) Stage #4.





(d)

Table 4.1 Capacitor Voltages for 8X with m=10.

Vc1a=Vc1b	1.397v~1.416v
Vc2a=Vc2b	2.407v~2.426v
Vc3a=Vc3b	3.416v~3.435v
Vc4a=Vc4b	4.630v~4.639v



Figure 4.3 Waveforms for 8X with m=10: (a) Input Voltage; (b) Output Voltage; (a) Input Current; and (d) Output Current







4.3 Chip Implementation

Figure 4.4 shows the physical layout of the 8X converter, employing the T25HV process. The core area of the converter was developed within the area constraint of $1.9 \text{ mm} \times 1.9 \text{ mm}$. The layout includes 32 PMOS switching devices, where each stage takes 4 PMOS switching devices, as shown in Figure 3.6.



Figure 4.4 Physical Layout of 8X Converter.

The width of the metal layers for the power line (VDD) and ground line (GND) must be sufficiently wider allowing much larger currents to flow through it; otherwise, the chip may be burned out due to excess current flowing through it. A stacked metal layer is generally designed, as shown in Fig. 4.5(a), for the interconnection from the power/ground line to the source terminal of a PMOS transistor. With the stacked metal layer, the chip can function properly even when excess current flows through it.

Floor-planning is a crucial task. The location and orientation of the pins must be carefully designed. The top metal layer is generally used to connect the pins to I/O pads. The connected wire should reach at the edge of an I/O pad instead of running over a pad, as shown in Fig. 4.5(b), otherwise a short circuit may occur and cause the chip to malfunction. Note that longer metal lines generally exhibit greater parasitic effects, resulting in path delay. Thus, the shortest path between two devices is always desired when metal lines are used for interconnection.



Figure 4.5 HV Layout Design Rules: (a) Stacked Metal Layer; (b) Pad Connection; (c) Multi-Transistors.

When m=10, this implies that ten PMOS transistors are connected in parallel, i.e., their source terminals and drain terminals are respectively connected. To minimize chip area, both source and drain terminals are placed as shown in Figure 4.5(c), labeled S and D, respectively. The 32 PMOS transistors, as switching devices, are divided into two banks, as shown in Figure 4.4, and both are placed on the top and the bottom of the core, respectively. The space between both top and bottom banks accommodates power and ground lines connected to the source terminals of the switching devices. The above floor-planning scheme can significantly reduce the

wire interconnection between the switching devices and power/ground lines, and considerably decreases the parasitic capacitances and effects.

Determining the number contacts/vias needed is also an important issue. In general, redundant contacts/vias are necessary as far as chip yield is concerned. It is necessary to make two or more contacts/vias to ensure that the chip to works properly even in the presence of a faulty contact/via. In analog circuit layouts, the contacts should be sufficiently large to reduce resistance and to let current uniformly distribute to both source and drain terminals of the transistor. In addition, when the devices are connected to the power lines, a sufficient number of vias must be placed to reduce current density and alleviate the skin effect, potentially prolonging the chip life.

The TSMC T25HV process requires a guard ring to rope the PMOS transistor alleviating any signal interference. The guard ring includes a metal layer surrounding the transistor, a contact (CONT layer), a diffusion (DIFF layer), and N+implantation (NIMP layer).

Figure 4.6 shows the capacitor voltages in the post-layout simulation. Results show that the voltages across V_{c1a} and V_{c1b} are 1.155~1.170 V and 1.190~1.205 V, respectively, as tabulated in Table 4.2; similarly, the voltages across V_{c2a} (V_{c2b}), V_{c3a} (V_{c3b}), and V_{c4a} (V_{c4b}) are, 1.869~1.883 V (1.872~1.887 V), 2.623~2.606 V (1.586~2.601 V), 3.625~3.632 V (3.566~3.575 V), respectively.

Fig. 4.7 plots the waveform for input/output currents/voltages. Results show that the input voltage and current are 2 V and 57.55 mA, respectively, and the output voltage and current are 7.2 V and 7.2 mA, respectively. Due to the implementation constraints with small m, i.e., m=10, the output-input voltage ratio is dropped from 4.64 times from the pre-layout simulation to 7.2/2=3.6 times in the post-layout simulation, as listed in Table 4.3; and the output-input

current ratio in both pre-layout and post-layout simulations are about the same. Table 4.4 summarizes the design specification.



Figure 4.6 Output Voltage Waveforms in Post-Layout Simulation (f=50 kHz, T=2us/div): (a) Stage #1; (b) Stage #2; (c) Stage #3; and (d) Stage #4.





(d)



Figure 4.7 Waveforms in Post-layout Simulation: (a) Output Voltage; (b) Input Current; and (c) Output Current.





(c)

Table 4.2 Capacitor Voltages (Pre-layout Vs. Post-layout).

	Pre-layout Simulation	Post-layout Simulation
Vc1a	1.397 V ~ 1.416 V	1.155 V ~ 1.170 V
Vc1b	1.397 V ~ 1.416 V	1.190 V ~ 1.205 V
Vc2a	2.407 V ~2.426 V	1.869 V ~ 1.883V
Vc2b	2.407 V ~2.426 V	1.872 V ~ 1.887 V
Vc3a	3.416 V ~ 3.435 V	2.623 V ~ 2.606 V
Vc3b	3.416 V ~ 3.435 V	2.586 V ~ 2.601 V
Vc4a	4.630 V ~ 4.639 V	3.625 V ~ 3.632 V
Vc4b	4.630 V ~ 4.639 V	3.566 V ~ 3.575 V

Table 4.3 Output Performance (Pre-layout Vs. Post-layout).

	Pre-layout Simulation	Post-layout Simulation
Input Voltage	2 V	2 V
Output Voltage	9.27 V	7.2 V
Voltage Ratio	4.64	3.6
Input Current	74.25 mA	57.55 mA
Output Current	9.27 mA	7.2 mA

Process	TSMC HV 0.25 μm
PMOS Transistors	750um/800nm, m=10
Capacitor	10 µF
Switching frequency	50 KHz
Gate count	32 PMOS Transistors
Power Dissipation	155.21 mW
Chip Implementation	1.9 mm x 1.9 mm

Table 4.4. Design Specification

4.4 Chip Measurement

The test environment is set up as follows: The Agilent E3640A power supply generates the input voltage of 2 V, and the Agilent 33210A function generator to generate the input signals to switching devices, the output current and voltage waveforms are observed by the Agilent DSO 1012A Oscilloscope, as shown in Figure 4.8.



Figure 4.8 Agilent Measurement Instruments: (a) Power Supply; (b) Function Generator; and (c) Oscilloscope.

As described previously, the capacitances in the 8X converter are 10uF which takes a large chip area. This implementation takes the external capacitors. The total number of pins in the fabricated chip is 76, where 16 pins for VDD, 16 pins for GND, 8+4 pins for the 8 capacitors, and 32 pins for switching devices. The pin function is given in Fig. 4.9(a) and the external capacitors are connected as illustrated in Fig. 4.9(b).



Figure 4.9 Pin Assignment: (a) Pin Function; and (b) External Capacitor Connection.

4.5 Discussion

This study investigated the feasibility of developing a 200 W DC-DC converter, potentially suitable for photovoltaic (PV) applications, using the TSMC T25HV process under the core size limitation (1.9x1.9 mm²). The previous section establishes that realizing 200 W is not physically possible under the above design constraints. Based on the simulation results for the 4-stage 8X converter, the following section discusses the issue of maximizing power efficiency. The principle cause of power loss is the leakage current associated with the switches. Possible solutions include: (a) splitting stages into multiple chips to increase m values per chip; and (b) changing the voltage conversion ratio. Increasing the conversion ratio will result in higher output voltage and lower current requirement. Thus, it will have less power loss.

The chip layout in Figure 4.4 includes 32 PMOS transistor for the 4-stage 8X converter. This section considers two possible chip configurations: (a) One-stage 2X converter; and (b) Two-stage 4X converter. To achieve the voltage conversion ratio of 8, one can either take one 4stage 8X converter, or two cascaded 2-stage 4X converters, or four cascaded 1-stage 2X converters.

This section first presents the design and simulation of a one-stage 2X converter under the core size limitation with the TSMC T25HV process. The performance of a 4-stage 8X converter is compared with that of a circuit which is comprised of four cascaded one-stage 2X converters. Then, based on the above three different configurations for the converter with a voltage conversion ratio of 8, their maximal power efficiencies are analyzed and discussed. Finally, issues regarding the optimal voltage conversion ratio for NX converters are also addressed.

4.5.1 One-Stage 2X Converter

The one-stage 2X converter, as shown in Figure 3.6, is simulated with the following parameters: $V_{in}=10$ V, capacitances $C_{1a}=C_{1b}=10$ uF, and the load resistance = 1 K Ω . The complementary signals are applied as described in Fig. 3.2(d), where the switching frequency is 50~100 KHz. The PMOS transistor size 800u/800n and m=64. Figure 4.10 shows pre-layout simulation results for waveforms for the voltage across the capacitors C_{1a} and C_{1b} . Results show that the voltages across V_{c1a} and V_{c1b} are 9.87~9.88 V and 9.873~9.884 V, respectively, as summarized in Table 4.5.



Figure 4.10 Pre-layout Simulations - Capacitor Voltage Waveforms for Single Stage (f=50 kHz, T=2us/div).

Fig. 4.11 plots the waveform for input/output currents/voltages in Pre-layout simulation. Results show that the input voltage is 10 V, the input current, output current, and output voltage at TT corner are 39.78 mA, 19.75 mA, and 19.75 V, respectively. The one-stage 2X converter is also simulated at the FF and SS corner, the simulations results are summarized in Table 4.6. For the TT corner, the output/input voltage ratio in the pre-layout simulation is 19.75/10=1.975 for the 2X converter with m=64, and the efficiency is 98.75%. Similarly, Figure 4.12 plots the capacitor voltage in the post-layout simulation, where the voltages across V_{c1a} and V_{c1b} are $9.682\sim9.701$ V and $9.652\sim9.672$ V, respectively.



(a)



(b)

Figure 4.11 Waveforms in Pre-layout Simulation: (a) Output Voltage; (b) Input Current; and (c) Output Current.

Figure 4.11 cont'd:



Figure 4.12 Post-layout Simulations - Capacitor Voltage Waveforms for Single Stage.

Figure 4.13 plots the waveform for currents/voltages in Post-layout simulation, where the input current, output current, and output voltage at TT corner are 38.72 mA, 19.35 mA, and 19.35 V, respectively. For the TT corner, the output/input voltage ratio in the post-layout simulation is 1.935 with an efficiency of 96.75%.

Table 4.5 <u>Summary – Capacitor Voltages</u>

	Pre-layout Simulation	Post-layout Simulation
V _{c1a}	9.87 V ~ 9.88 V	9.682 V ~ 9.701 V
V _{c1b}	9.873 V ~ 9,884 V	9.652 V ~ 9.672 V



Figure 4.13 Waveforms in Post-layout Simulation: (a) Output Voltage; (b) Input Current; and (c) Output Current.

Figure 4.13 cont'd:



	corner	Vin	Vout	Iin	Iout	Efficiency
	TT	10v	19.75v	39.78mA	19.75mA	98.75%
Pre-layout Simulation	FF	10v	19.79v	39.51mA	19.79mA	98.95%
Simulation	SS	10v	19.69v	39.38mA	19.69mA	98.45%
D	TT	10v	19.35v	38.72mA	19.35mA	96.75%
Post-layout Simulation	FF	10v	19.39v	38.36mA	19.39mA	96.95%
	SS	10v	19.30v	38.42mA	19.30mA	96.50%

Table 4.6 <u>Summary – Output Performance</u>

There are three process corners which are commonly used. They are: T (Typical), F (Fast), and S (Slow). For TT corner, the first letter refers to the NMOS corner, and the second letter refers to the PMOS corner [25]. F and S corners exhibit carrier mobilities that are higher and lower than normal, respectively. In semiconductor manufacturing, a process corner is an example of design-of-experiments technique that refers to a variation of fabrication parameters used in applying an integrated circuit design to a semiconductor wafer. Process corners represent the extremes of these parameter variations within which a circuit that has been etched onto the wafer must function correctly. A circuit running on devices fabricated at these process corners may run slower or faster than specified and at lower or higher temperatures and voltages, but if the circuit does not function at all at any of these process extremes the design is considered to have inadequate design margin [25].

4.5.2 Performance Evaluation

The simulation and chip implementation of a 4-stage 8X converter, referred to as an 8X converter, were presented in Section 4.2. The simulation of 1-stage 2X converter was shown in

Section 4.4. With four cascaded 1-stage 2X converters, referred to as a 4*2X converter, one can achieve the voltage conversion ratio of 8. Note that the transistors in 8X converter take m=10, while those in 4*2X-converter are m=64. The performance comparison of both converters is given in Table 4.9. For the FF corner, the 8X converter achieves 4.96 times, while the 4*2X converter reaches to 7.34 times, and the efficiency is improved from 62% to 91.75%.

	corner	Vin	Vout	Iin	Iout	efficiency
4*2X Converter	TT		72.3v	580mA	72.3mA	90.375%
	FF	10 V	73.4v	588mA	73.4mA	91.75%
	SS		70.6v	564mA	70.6mA	88.25%
8X Converter	TT		46.3v	370mA	46.3mA	57.875%
	FF	10 V	49.6v	396mA	49.6mA	62%
	SS		41.9v	335mA	41.9mA	52.375%

Table 4.7 Performance Comparison (Pre-layout Simulation).

4.5.3 Increasing Voltage Gain Ratio

The simulation results shown in Table 4.7 for 8X converter assumed the input voltage of 10 V and m=10. A higher voltage ratio reduces output current for a given load, but more stages required to increase output voltage. M value decreases as the number of stages increases due to the area constraint. Based on the area constraint, the m values can be roughly estimated as: m=10 for 8X; m=8 for 10X; m=6 for 12X; m=5 for 14X; and m=4 for 16X. Figure 3.10 and Figure 3.11 show the plots of the output voltages of 8X converter with the resistive loads of 1 K Ω and 32 Ω for various m values, respectively. The following simulation results are investigated the

relationship between the output voltages and the load currents for various m values, where the load currents are generated with various resistive loads.

Table 4.8 shows the 8X converter with m=10 and the input voltage of 10 V for various load currents. Results show that among the simulated load currents, the maximum power, P=2.05 W, occurs at R=750 Ω , where the output voltage and current are 39.2 V and 52.3 mA with a voltage conversion efficiency of 49%.

R	Vout	Iout(mA)	P(W)	Efficiency
50	5.28	106	0.56	6.6%
500	31.7	63.4	2.01	39.625%
750	39.2	52.3	2.05	49%
1000	44.6	44.6	1.99	55.75%
2000	56.6	28.3	1.602	70.75%
5000	68.4	13.68	0.936	85.5%
10000	73.678	7.3678	0.543	92.10%

Table 4.8 <u>Simulation Results -8X with m=10</u>.

Similarly, Table 4.9 and Table 4.10 describes the 12X converter with m=6 and 14X converter with m=5 with the input voltage of 10 V for various load currents. Results in Table 4.9, show that, among the simulated load currents, the maximum power, P=1.68 W, occurs at R=2000 Ω , where the output voltage and current are 57.92 V and 28.96 mA with a voltage conversion efficiency of 48.27%. Comparing with the results in Table 4.8 for 8X with m=10, the maximum power is reduced from 2.05 W to 1.68 W, or a reduction ratio of 1.68/2.05, or 81.95%.

Results in Table 4.10, show that, among the simulated load currents, the maximum power, P=1.58 W, occurs at R=2000 Ω , where the output voltage and current are 56.22 V and 28.11 mA with a voltage conversion efficiency of 40.16%. Comparing with the results in Table 4.8 for 8X with m=10, the maximum power is reduced from 2.05 W to 1.58 W, or a reduction ratio of 1.58/2.01, or 77.61%.

From the simulation results, less output current requirement with the increased voltage gain ratio does not overcome the lowered m values. With the increased voltage gain ratio, the overall efficiency decreases. It concludes that, without increasing the overall switch area, the maximum power potential does not increase significantly.

R	Vout	I _{out} (mA)	P(W)	Efficiency
100	6.02	60.24	0.36	5.02%
200	11.42	57.12	0.65	9.52%
500	24.44	48.89	1.19	20.37%
1000	39.58	39.58	1.57	32.98%
2000	57.92	28.96	1.68	48.27%
5000	82.62	16.52	1.37	68.85%
10000	97.5	9.75	0.95	81.25%

Table 4.9 <u>Simulation Results – 12X with m=6</u>.

Table 4.10 <u>Simulation Results – 14X with m=5</u>.

R	Vout	I _{out} (mA)	P(W)	Efficiency
100	5.01	50.1	0.25	3.58%
200	9.66	48.3	0.47	6.90%
500	21.56	43.12	0.93	15.40%
1000	36.52	36.52	1.33	26.09%
2000	56.22	28.11	1.58	40.16%
5000	85.6	17.12	1.47	61.14%
10000	105.6	10.56	1.12	75.43%

4.5.4 Increasing Switch Area – Multiple Chips Solution

As discussed previously, without increasing overall switch area, the maximum power potential does not increase significantly, and under this constraint increasing the voltage gain ratio actually decreases overall efficiency. Thus, maximizing switch area and increasing M appears to be the most important factor in improving converter output characteristics. Splitting stages multiple chips allows for double/quadruple switch area.

The original 8X converter with m=10 contains 4 stages of the 2X module. The switch area can be doubled, i.e., m=20, if we split the 4 stages into two chips, where each chip contains only two stages of the 2X module, referred to as a 4X converter, as shown in Figure 3.2(a). The switch area can be quadrupled, i.e., m=40, if we split the 4 stages into four chips, where each chip contain only one stage of the 2X module, referred to as a 2X converter, as shown in Figure 3.6. In fact, as discussed in Section 4.5.1, for a 1-stage 2X converter, the maximum value of m can be carefully implemented up to 64. To achieve the voltage gain ratio of 8, one can implement it with either one 8X converter, or two 4X converter, i.e., 2*4X converter, or four 2X converter, i.e., 4*2X converter.

Table 4.11 shows the 2*4X converter with m=20 and the input voltage of 10 V for various load currents. Results show that among the simulated load currents the maximum power, P=3.98 W, occurs at R=500 Ω , where the output voltage and current are 44.63 V and 89.2 mA with a voltage conversion efficiency of 55.79%. On the other hand, the lowest power occurs at the lowest load current and the highest output voltage. Compared to the results in Table 4.8 for 8X with m=10, the maximum power is increased from 2.05 W to 3.98 W, or an improvement ratio of 3.98/2.05, or 195%, i.e., the maximum power is nearly doubled.

Similarly, Table 4.12 shows the 4*2X converter with m=40 and the input voltage of 10 V for various load currents. Results show that among the simulated load currents, the maximum power, P=7.73 W, occurs at R=100 Ω . The lowest power occurs at the lowest load current and the highest output voltage. Results show that among the simulated load currents the maximum power, P=7.73 W, occurs at R=100 Ω . The improvement ratio is 3.85 times.

R	Vout	Iout(mA)	P(W)	Efficiency
100	17.3	172.6	2.99	21.63
500	44.63	89.2	3.98	55.79
1000	56.7	56.7	3.21	70.88
2000	66	33	2.18	82.5
5000	73.7	14.73	1.09	92.13
10000	76.7	7.67	0.59	95.88

Table 4.11 Simulation Results – 8X with m=20.

Table 4.12 Simulation Results – 8X with m=40.

R	Vout	Iout(mA)	P(W)	Efficiency
100	27.8	278	7.73	34.75%
500	56.7	113.4	6.43	70.88%
1000	66	66	4.36	82.50%
2000	72.2	36.1	2.61	90.25%
5000	76.7	15.34	1.18	95.88%
10000	78.25	7.83	0.61	97.81%

Figure 4.14(a) plots the output power of the converters with m=10, 20, 30, and 40, for various load currents ranged from 0 to 350 mA. Results show that, for smaller m values (m < 100), the output power scales linearly with m. Figure 4.14(b) plots the voltage conversion efficiency for the above converters for various load currents. For larger m value, less current can be blocked. Thus, both voltage conversion efficiency and power increase with the m value.


(a)



(b)

Figure 4.14 8X Performance for various m: (a) Power; and (b) Efficiency.

Chapter 5

CONCLUSIONS AND FUTURE RESEARCH WORKS

Switched-capacitor DC-DC converters [6-15] find increasing relevance in industrial switched mode power supplies, due to their salient features, namely magnetic-less operation and very high efficiency. Furthermore, in order to reduce the inductance requirement in DC-DC converters, multilevel DC-DC converters [4,5,16-20] have been proposed to achieve higher power density and higher efficiency than the conventional ones. This study reviews two multilevel DC-DC converters: a magnetic-less flying-capacitor DC-DC converter (FCC) [4] and a modular multilevel capacitor clamped DC-DC converter (MMCCC) [21]. Based on the design principle of MMCCC, this study designs and develops an alternative modular multilevel switched-capacitor DC-DC converter which is suitable for the application of high voltage gain, referred to as HVGC. Compared with FCC and MMCCC, the HVGC has several key advantages [22]: (1) less power loss; (2) substantially reduced total capacitor voltage ratings; (c) lower capacitance and ripple current requirement of the output capacitors; (d) reduced switching device count, low device current stress and low total device power rating; (e) lower cost; (f) improved efficiency; (g) bidirectional operation; and (h) modular structure.

In Chapter 3, the design and operation of the HVGC with voltage conversion ratios of 4 and 6 were presented. A HVGC circuit with a voltage conversion ratio of 8 was simulated using the TSMC high-voltage process, T25HV. With an input voltage of 10 V and the resistive load of

1 K Ω , the HVGC produces an output voltage near 80 V and output current near 2.5 A. This amounts to an output power of 200 W, suitable for photovoltaic (PV) applications. As discussed in Figure 3.10, the output voltage and currents are highly dependent on the size of switching devices, PMOS transistors in our case. For example, using PMOS transistors with W/L=800 um/800 nm, m=10, the output voltage and current is 47.3 V and 47.3 mA, respectively, and conversion efficiency is nearly 60%. On the other hand, with m=2000, the output voltage and current is 79.6 V and 79.6 mA, respectively, a conversion efficiency of 99.50 %. Thus, there exists a design trade-off between the transistor size and conversion efficiency.

Chapter 4 describes the design and chip implementation of the HVGC with a voltage conversion ratio of 8. Due to the chip size limitation for the available chip design service organization, the maximal chip size is $1.9 \text{ mm} \times 1.9 \text{ mm}$. Under this design constraint, with the external capacitor of 10uF, the PMOS transistor size was selected with 750um/800nm, and m=10. Lower output voltage and current in such chip implementation is expected, as illustrated in Figure 3.9 with m=10. Section 4.1 briefly describes the experiences for designing chip with high voltage process. The chip was developed, simulated, fabricated, and measured. The post-layout simulation results introduce non-ideal effects not present in pre-layout simulation results, mostly related to the path delays associated with interconnection wiring, and show slightly reduced performance because of it. Section 4.5 addresses the issues of how to maximize the output power. It is shown that increasing the overall switch area does not increase the maximum power potential significantly. It concludes that increased m value allows for better performance and splitting stages into multiple chips allows for doubling/quadrupling of the switch area.

This study investigated the feasibility of developing a 200 W DC-DC converter for the photovoltaic (PV) applications under the core size limitation (1.9x1.9 mm²) with the TSMC

T25HV process. This study has concluded that realizing 200 W is not physically possible under the above design constraints. There are two possible solutions that can maximize the output voltage: (a) change the voltage gain ratio; and (b) splitting stages into multiple chips. This study has shown that with the increased voltage gain ratio, the overall efficiency decreases and the maximum power is lower than the original 8X converter. Splitting stages into multiple chips is a feasible solution that increases m value and the output power.

Layout and floor-planning of the switching devices can affect the chip performance considerably. Careful study with regards to placement and routing under the high voltage process can significantly improve design quality in post-layout simulation results and the fabricated chip. Thus, it is essential to develop an efficient, yet simple, design methodology for the chip design with the high voltage process. This particular issue has the potential to be a very interesting problem for further development. APPENDICES

APPENDIX A:

Spice file used for pre-layout simulation

** 8X Converter

.TRAN 1e-9 20e-3

.lib 'c025bcd60v.l' TT_HV

.lib 'c025bcd60v.l' TT_MIM

.lib 'c025bcd60v.l' DIO

.TEMP 25

** Library name: 8X_DC-DC

** Cell name: power_sw

** View name: schematic

.subckt power_sw p1 p2 clk

m0 net5 v2 p2 net16 pa60_g5_full_soa l=800n w=900u as=594e-12 ad=6.68628e-

9 ps=1.80132e-3 pd=1.82676e-3 m=10

m8 net5 v1 p1 net16 pa60_g5_full_soa l=800n w=900u as=594e-12 ad=6.68628e-

9 ps=1.80132e-3 pd=1.82676e-3 m=10

d1 p2 net16 hvnwnblhvpw area=400e-12 m=1

d5 p1 net16 hvnwnblhvpw area=400e-12 m=1

e1 v1 p1 0 clk 1

e2 v2 p2 0 clk 1

.ends power_sw

V1 b 0 PWL (0 0 80n 5 2.42e-6 5 2.50e-6 0 5.00e-6 0 R)

V3 a 0 PWL (0 0 2.5e-6 0 2.58e-6 5 4.92e-6 5 5e-6 0 R)

XU1 N001 N009 a power_sw

XU2 N009 0 b power_sw

XU3 N002 N001 b power_sw

XU4 0 N016 a power_sw

V7 N001 0 10

XU5 N001 N010 b power_sw

XU6 N010 0 a power_sw

XU7 N003 N002 a power_sw

XU8 N016 N017 b power_sw

C1 N002 N009 4u

C2 N009 N016 4u

C3 N003 N010 2u

C4 N010 N017 2u

XU9 N001 N011 a power_sw

XU10 N011 0 b power_sw

XU11 N004 N003 b power_sw

XU12 N017 N018 a power_sw

XU13 N001 N012 b power_sw

XU14 N012 0 a power_sw

XU15 N005 N004 a power_sw

XU16 N018 N019 b power_sw

C5 N004 N011 1u

C6 N011 N018 1u

C7 N005 N012 1u

C8 N012 N019 1u

R1 N005 N019 750

.op

.probe i(r1)

.probe v(*)

.probe tran output=par('V(N005,N019)')

.probe tran pwr=par('V(N005,N019)*I(R1)')

.end

REFERENCES

REFERENCES

- [1] W. Qian, H. Cha. F. Z. Peng, L. M. Tolbert, "A 55-kW Variable 3X DC-DC Converter for Plug-in Hybrid Electric Vehicles," *IEEE Transactions on Power Electronics*, vol. 27, 2012.
- [2] M. Shen, F. Z. Peng, and L. M. Tolbert, "Multilevel DC–DC Power Conversion System with Multiple DC Sources," *IEEE Trans. on Power Electronics*, vol. 23, pp. 420-426, January 2008.
- [3] W. Qian, H. Cha. F. Z. Peng, L. M. Tolbert, "A 55-kW Variable 3X DC-DC Converter for Plug-in Hybrid Electric Vehicles," *IEEE Transactions on Power Electronics*, vol. 27, 2012.
- [4] W. Qian, F. Z. Peng, M. Shen, and L. M. Tolbert, "3X DC-DC Multiplier/Divider for HEV Systems," Proc. of Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 1109-1114, February 2009.
- [5] F. Z. Peng, F. Zhang, and Z. Qian, "A Magnetic-less DC-DC Converter for Dual-Voltage Automotive Systems," IEEE Trans. on Industry Applications, vol. 39, pp. 511-518, 2003.
- [6] M.L. Gebben, J.G. Cintron-Rivera, W. Qian, D. Cao, X. Pei, and F.Z. Peng, "A Zero-Current-Switching Multilevel Switched Capacitor DC-DC Converter," IEEE Energy Conversion Congress and Exposition (ECCE), pp. 17-22, 2011.
- [7] J. F. Dickson, "On-Chip High-Voltage Generation in MNOS Integrated Circuits Using an Improved Voltage Multiplier Technique," IEEE Journal of Solid-State Circuits, vol. 11, pp. 374-378, November 1976.
- [8] C. K. Tse, S. C. Wong, and M. H. L. Chow, "On Lossless Switched Capacitor Power Converters," IEEE Trans. on Power Electronics vol. 10, pp. 286-291, 1995.
- [9] B. Arntzen and D. Maksimovic, "Switched-Capacitor DC/DC Converters with Resonant Gate Drive," IEEE Trans. on Power Electronics, vol. 13, pp. 892-902, 1998.
- [10] A. Ioinovici, "Switched-Capacitor Power Electronics Circuits,", IEEE Circuits and Systems Magazine, vol. 1, pp. 37-42, 2001.
- [11] H. S. Chung, A. Ioinovici, and C. Wai-Leung, "Generalized Structure of Bi-directional Switched-Capacitor DC/DC Converters," IEEE Trans. on Circuits and Systems I: Fundamental Theory and Applications, vol. 50, pp. 743-753, 2003.
- [12] F. L. Luo and H. Ye, "Positive Output Multiple-Lift Push-Pull Switched-Capacitor Luo-Converters," IEEE Trans. on Industrial Electronics, vol. 51, pp. 594-602, 2004.
- [13] M. D. Seeman and S. R. Sanders, "Analysis and Optimization of Switched-Capacitor DC-DC Converters," IEEE Trans. on Power Electronics, vol. 23, pp. 841-851, 2008.

- [14] R. Jain, "A Novel Switched Capacitor Circuit for Efficient Voltage Regulation," in Proc. of 7th International Caribbean Conference on Devices, Circuits and Systems ICCDCS), pp. 1-6, 2008.
- [15] Y. S. Lee and Y. Y. Chiu, "Zero-Current-Switching Switched-Capacitor Bidirectional DC-DC Converter," IEE Proceedings, Electric Power Applications, vol. 152, pp. 1525-1530, 2005.
- [16] V. Yousefzadeh, E. Alarcon, and D. Maksimovic, "Three-level buck converter for envelope tracking applications," IEEE Trans. on Power Electronics, vol. 21, pp. 549-552, 2006.
- [17] M. Xu, J. Sun, and F. C. Lee, "Voltage divider and its application in the two-stage power architecture," Proc. of Twenty-first Annual IEEE Applied Power Electronics Conference and Exposition (APEC), p.7, 2006.
- [18] F. Zhang, L. Du, F. Z. Peng, and Z. Qian, "A New Design Method for High-Power High-Efficiency Switched-Capacitor DC-DC Converters," IEEE Trans. on Power Electronics, vol. 23, pp.832-840, 2008.
- [19] K. Jin, M. Yang, X. Ruan, and M. Xu, "Three-Level Bidirectional Converter for Fuel-Cell/Battery Hybrid Power System," *IEEE Trans. on Industrial Electronics*, vol. 57, pp. 1976-1986, June 2010.
- [20] K. Sano and H. Fujita, "Performance of a High-Efficiency Switched-Capacitor-Based Resonant Converter with Phase-Shift Control," IEEE Trans. on Power Electronics, 2010.
- [21] F. H. Khan and L. M. Tolbert, "A Multilevel Modular Capacitor-Clamped DC-DC Converter," *IEEE Trans. on Industry Applications*, vol. 43, pp. 1628-1638, November/December 2007.
- [22] W. Qian, J. G. Cintrón-Rivera, F. Z. Peng, and D. Cao, "A Multilevel DC-DC Converter with High Voltage Gain and Reduced Component Rating and Count," Proc. of Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), pp.1146-1152, March 2011.
- [23] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*, 2nd edition, John Wiley, New York, 1950.
- [24] O. Abutbul, A. Gherlitz, Y. Berkovich, and A. Ioinovici, "Step-Up Switching-Mode Converter With High Voltage Gain Using a Switched-Capacitor Circuit," *IEEE* Trans. on Circuits and Systems—I: Fundamental Theory and Applications, vol. 50, pp. 1098-1102, August 2003.
- [25] Available at http://en.wikipedia.org/wiki/Process_corners