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THE DESIGN OF LOW-POWER INTEGRATED RADIO-FREQUENCY FRONT-END IN CMOS

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THE DESIGN OF LOW–POWER INTEGRATED RADIO–FREQUENCY FRONT–END IN CMOS

By

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ABSTRACT

THE DESIGN OF LOW–POWER INTEGRATED RADIO–FREQUENCY FRONT–END IN CMOS

By

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Previous attempts to design low-power radio-frequency (RF) front-end in standard CMOS technology have failed to produce satisfying results in terms of design optimization and topology improvement. The problem of how to reduce front-end power without degrading RF performance remains challenging. A review of the literature shows that a good rationale as well as innovative design techniques is needed to deal with the problem.

For each building block in low-IF front-end, this thesis identifies the major tradeoff involved in the design, then analyzes the tradeoff to derive new design techniques and circuit topologies. Such rationale leads to several design methods effectiveness of which is later demonstrated by the design and layout of a 2.4-GHz Bluetooth receiver front-end in TSMC 0.18-μm CMOS technology. A novel method for noise-constrained optimization for low power is developed for integrated CMOS low noise amplifier (LNA). A novel analyzing method as well as modified topology is developed for Gilbert mixer to improve linearity. Finally, a novel low-power implementation of complex analog filter, which is the asymmetric polyphase network filter with Nauta's transconductor, is developed for image rejection in the front-end.

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1 INTRODUCTION

A radio-frequency (RF) communication system transmits information using radio waves of frequencies from 400MHz to 2.5G-Hz [1]. The RF spectrum lies between the VHF spectrum and the microwave spectrum.

The unique combination of several characteristics of RF electromagnetic waves makes it suitable for personal communication purpose. First, compared with those of VHF band, the higher frequencies of RF band make it possible to accommodate more channels, to increase channel capacity, and to increase signal-to-noise ratio (SNR) according to Shannon's theorem [2]. Second, unlike its microwave counterpart, most work in RF circuit design can be done with a lumped model due to the relatively large wavelengths (12cm–75cm) of RF waves [3,4]. In this way the design process becomes simpler and system cost is reduced. Finally, compared with microwave waves, RF waves suffer less propagation loss from atmospheric absorption caused by water vapor and molecular oxygen. Such absorption is a major factor affecting the performance of RF communication systems in practice [4].

One historically important RF application is radar, such as L-band Synthetic Aperture Radar (SAR) for ocean imaging [5], and C-band weather penetration radar for commercial airlines [6]. Another major RF application has been wireless communication systems since 1970s, when satellite mobile radio systems operating in UHF frequency band of approximately 400MHz were launched [7]. However, the high costs of satellite mobile

radio systems prevented them from being widely used in public domain. The emerging of cellular mobile radio communication systems in late 1970s, such as Nordic Mobile Telephone (NMT) system by Ericsson, and Advanced Mobile Phone Service (AMPS) by AT&T Bell Laboratories, arguably marked the beginning of portable communications revolution which would fundamentally change people's life style in the following decades [8]. Other important RF applications include global positioning system (GPS) and cordless telephony.

Cellular mobile radio systems provide their users with opportunities to travel freely within the service area and simultaneously communicate with any telephone, fax, data modem, and electronic mail subscriber anywhere in the world [7]. Advances in VLSI and RF IC technologies keep making the cellular mobile radio headsets cheaper, smaller, and less power-consuming. Consequently, since 1980s the market of cellular mobile radio systems (cellular phones) has been experiencing explosive growth, and the trend is expected to continue at least in the near future [1]. The first generation of cellular mobile radio, AMPS, employs FDMA with analog FM and FDD modulation. Today, the widely used second generation GSM employs TDMA with digital coding modulation GMSK to achieve better performance than that of the first generation. Meanwhile, the third generation CDMA based on direct-sequence CMDA and FDD with OQPSK that offers more robust operation and more channel capacity than GSM is right on the way [3]. All generations of cellular mobile radios operate in the RF band.

A GPS (global positioning system) is a system for determining a user's position in space as well as in time. A GPS consists of satellites (transmitters), receivers (GPS radio), and land control centers for satellite-monitoring. The satellites transmit RF signals contain-

ing position and clock time information, while the receivers recover the information from received RF signals [9]. For example, the NAVSTAR GPS includes 24 L-band polar-orbit satellites transmitting signals at 1575.42 MHz and 1227.6 MHz simultaneously. The received RF signal for civilian use yields an rms position error of about 50-100m. With more accurate signaling, the error can be reduced to around 15m [10]. The GPS receiver is widely used in navigation systems. The FCC has mandated location finding for cell phones with GPS as the prevailing technology, and GPS radio is expected to be standard equipment for cars in the near future [11,12]. As a result, the demand of GPS receivers, particularly those of low cost, low power and small size is rapidly increasing in recent years.

Cordless telephony has been using RF frequencies to provide short-range voice communication since the birth of analog cordless standard known as CEPT/CT1 operating in the bands 914-915/959-960 MHz [13]. The efforts to increase the number of channels as well as channel capacity result in several digital cordless standards which employ carriers of higher RF frequencies, digital signaling and modulation schemes including TDMA, FDD, and GFSK. One good example of digital cordless telephony framework is the widely used Digital European Cordless Telephone (DECT) standard that operates in the bands 1880-1950MHz and has many advanced features such as traffic balance and uncoordinated operation [13]. Because of its low cost and flexibility, digital cordless telephony has a rapidly expanding market [14].

While the demand for traditional RF applications keeps growing, the use of RF bands to provide radio links for local-area data communication such as wireless LAN is increasingly attractive [15]. There are many technologies competing to implement the function of data transfer between communication devices and PCs, and Bluetooth is the

most promising one due to its longer connection distance than other standards such as IrDA [16][17]. A Bluetooth radio operates in the unlicensed 2.5 GHz industrial, scientific, and medical (ISM) RF band with features of low cost, automatic service discovery and ad hoc device connection. Such salient features make Bluetooth suitable for a wide range of applications such as automobile, laptop, PDA, etc [18]. Other technologies for short-range RF communication such as ultra-wideband wireless standard [114] are also emerging.

1.1 RF Transceiver

A RF communication system in the strict sense refers to a set of sub-systems that operate independently and communicate with each other using RF radio links. Figure 1.1 shows a simplified configuration of GSM system consisting of several sub-systems [19]. MHS (Mobile Headset Sub-system) is the mobile radio carried by user as personal communications terminal; BTS (Base Transceiver Station) manages the RF radio links with nearby MHS's; BSC (Base Station Controller) deals with radio resource management and handover.

From the perspective of RF system design, the sub-systems of RF communication system are quite similar in framework in most cases despite their difference in specification. For example, MHS and BTS in Figure 1.1 may share the same framework because of their similar functions of transmitting and receiving RF signals. Consequently, in the wide sense each of the sub-systems is considered a RF communication system itself, or in other word, a *transceiver*.

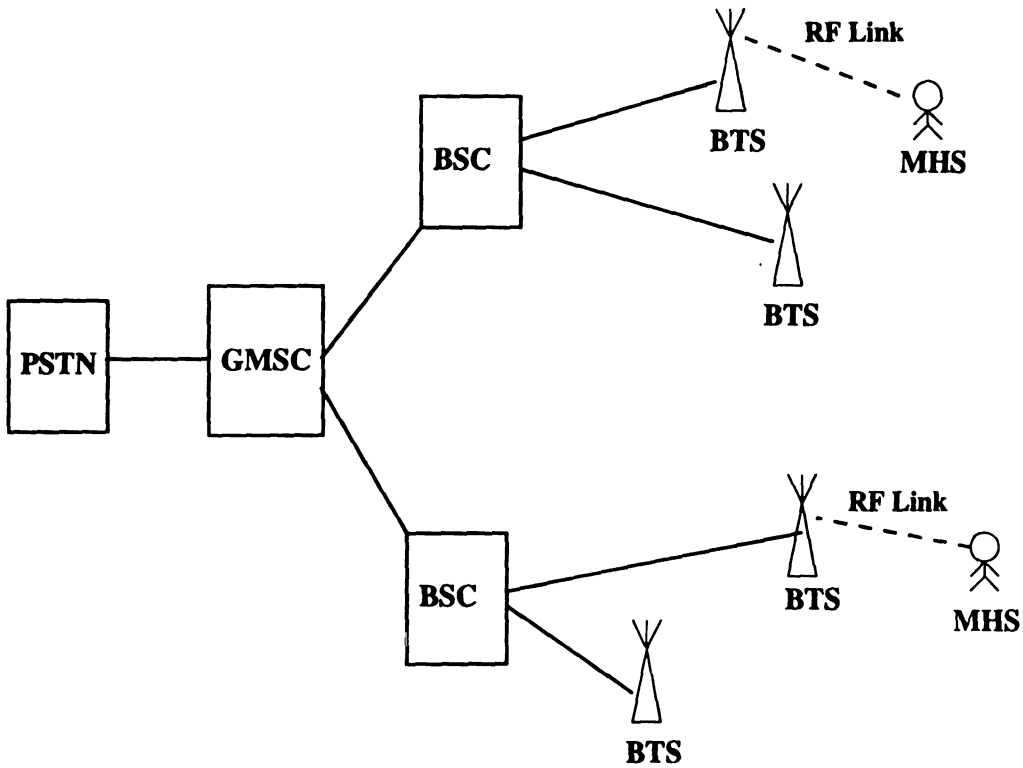
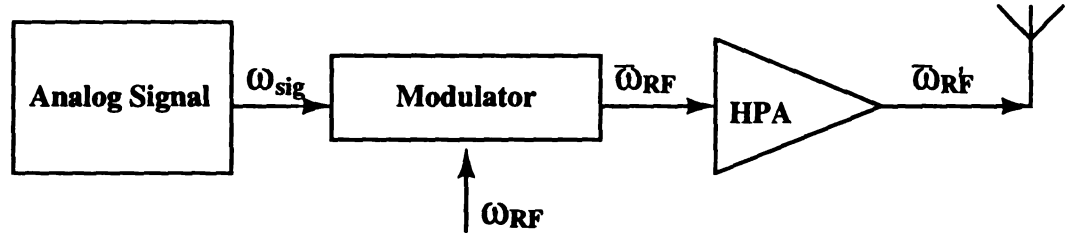


Figure 1.1: A Simplified Configuration of GSM Network.

A RF transceiver usually consists of a *receiver* and a *transmitter*. The receiver recovers the information data from RF signal received with antenna, whereas the transmitter modulates RF signal with the information data and sends RF signal to open air with antenna.

Historically the RF transceiver was first implemented with analog modulation techniques, and later with digital modulation techniques. Generic architectures of analog RF transceivers and digital RF transceivers are shown in Figure 1.2 and Figure 1.3, respectively [20]. Compared with their analog-modulation counterpart, digital-modulation transceiver (DMT) has several important advantages. First, a DMT consumes less power due to the higher level of integration. Second, a DMT is less sensitive to system noise and therefore produces higher SNR. Third, a DMT requires much less tuning work. Finally, more complicated functions such as image rejecting in digital domain can be performed with the use of DSP in a DMT. Today, digital-modulation transceiver has been widely used in mainstream RF applications for wireless communications [19].

The analog electronics for processing RF signal in a transceiver, as shown in Figures 1.2 and 1.3, is called transceiver front-end. A RF transceiver front-end consists of transmitter front-end and receiver front-end. Compared with transmitter front-end, the receiver front-end consumes more power and is much more difficult to design because of the hostile operating environment for typical wireless applications [3]. Thus, low-power design methodology for receiver front-end has been greatly needed for portable communication applications. Unless stated otherwise, by "front-end" we refer to receiver front-end in the rest of this thesis.



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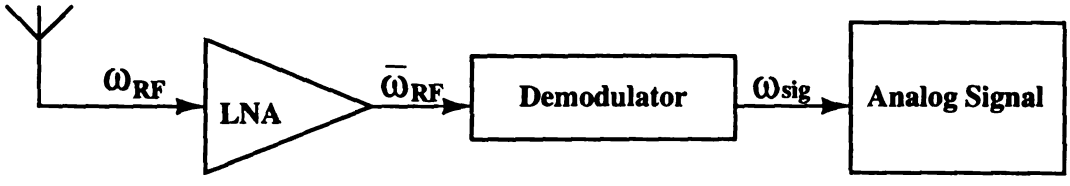
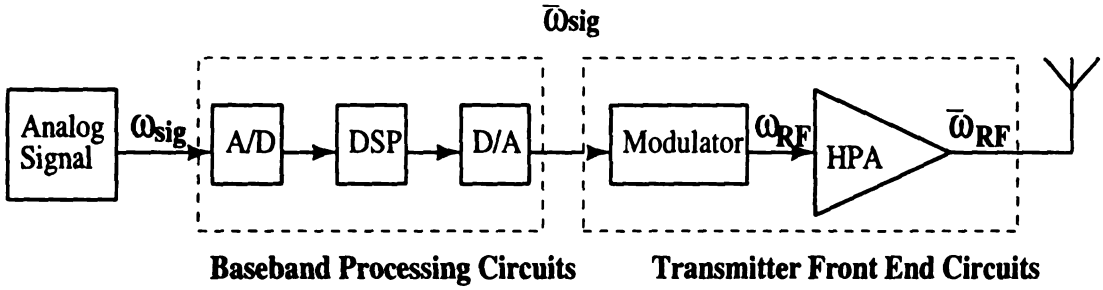


(b)

Figure 1.2: Generic Architecture of Analog Transceiver: (a) Transmitter; and (b) Receiver.



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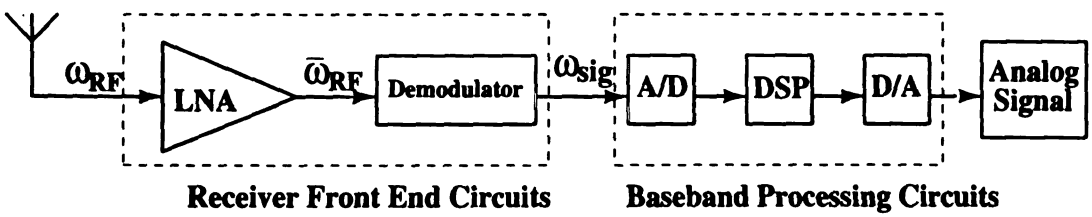


(b)

Figure 1.3: Generic Architecture of Digital Transceiver: (a) Transmitter; and (b) Receiver.

1.2 Low Power RF Receiver Front-End

Examination of consumer electronics market shows that the great demand of RF portable communications systems is driven by the development of low-cost and small-footprint wireless headsets [22]. The major contributors to the cost and size of such headsets are the transceiver integrated circuits (IC) and the battery. Therefore, it is desirable to increase integration level of transceiver IC to minimize the number of discrete components for less cost and smaller size. Since there is no substantial improvement expected in performance of battery technology in the near future [23], reduced power consumption of transceiver IC relaxes the requirements of battery such that cheaper battery can be used to cut the cost. Therefore, the low-power monolithic transceiver IC that operates without discrete components and consumes minimal power is particularly attractive for portable wireless communication terminals [22].

The fundamental tradeoff in RF transceiver IC design is the balance among cost, power and speed. To achieve the goal of low power and monolithic integration, innovations in various aspects of RF transceiver design and implementation are required [24]. Particularly, the choice of semiconductor technology is of crucial importance, since the RF performance of transceiver IC is limited by RF characteristics of the semiconductor technology used for fabrication. Traditionally, RF IC's are fabricated with GaAs technology featuring high gain and low noise. However, the GaAs fabrication process is generally expensive and unstable [1,4].

Recently, CMOS technology has become a serious contender to the conventional GaAs technology for RF IC realization [25]. Advance of CMOS technology has made it the

dominant choice for realizing the baseband digital electronics in transceiver [26]. Therefore the implementation of transceiver analog electronics in CMOS technology is attractive due to the promise of integrating the whole transceiver on a single chip. On the other hand, the RF performance of CMOS technology has been improving rapidly, where RF IC transceivers up to 5 GHz have been reported [27]. Considering that the front-end is the most power hungary part in a RF transceiver [1], it is natural to develop the low-power RF front-end in CMOS technology.

1.3 Thesis Objective and Organization

Despite the many research efforts on the design and implementation of low-power integrated CMOS RF IC in past years, a fully-integrated CMOS transceiver for wireless voice communication terminals such as GSM headsets is still not commercially available. When the requirements of image-rejecting and intermodulation are relaxed, however, full integration of RF transceiver becomes possible, as is in the case of many wireless data communication applications such as Bluetooth [29,92,99]. The bottleneck of realizing a high-performance low-power monolithic RF transceiver IC is the design of its front-end components [1]. The difficulty for such design comes in three ways. First, RF performance of CMOS technology is inherently inferior to that of GaAs technology in terms of gain and noise. This disadvantage often makes it a very difficult job to balance the tradeoff between power and speed in front-end design. Second, unlike the design of CMOS VLSI circuits, there is not much help available from CAD tools in CMOS RF IC design, including the front-end design. Therefore, the design cycle tends to be long, and no optimum results are

guaranteed. Third, the lack of high-quality passive integrated circuit components, such as high-Q integrated inductors, degrades the front-end performance seriously [3].

As mentioned before, RF receiver front-end consumes more power than transmitter front-end and is much more difficult to design because of the hostile operating environment for typical wireless applications [3]. For this reason, this research will focus on the development of the receiver front-end design.

The objective of this thesis study is to explore the problems of designing and developing low-power monolithic receiver front-end IC using standard digital CMOS technology, referred to as MRFEC, for portable RF wireless communication applications. The main focus is placed on how to optimize the building blocks (LNA, mixer, image-rejecting filter) of MRFEC in terms of both design methodology and circuit topology. For each building block, the major tradeoff affecting its performance is identified, then novel analysis methods are developed to treat such tradeoff, finally novel design guideline or circuit topology is derived from the analysis results. The thesis is organized as follows.

Chapter 2 reviews the literature on RF CMOS front-end design. Existing work is examined at four levels in front-end design: device technology, integrated circuit component, RF building block, and front-end architecture. Emphasis is put on important RF building blocks (LNA, mixer, and image-rejecting filter) and front-end architectures (low-IF, high-IF, zero-IF, and image-rejecting). The chapter is concluded with a summary of research topics involved in this thesis work.

Chapter 3 describes the proposed approaches for the design of front-end building blocks. For each building block, a novel analysis is first given to characterize the RF behavior, then our efforts to improve RF performance in terms of either design optimization or

topology improvement are presented. The chapter begins with a novel analysis of LNA noise behavior, then derives a method to perform noise-constrained optimization for minimum power consumption. Followed is the discussion on design of downconversion mixer, which analyzes the linearity issue of Gilbert-cell mixer in a novel manner based on feedback system model. Subsequently a new topology of Gilbert cell is proposed. Next a thorough analysis on image-rejecting operation of complex analog filter is presented. This chapter is concluded with a novel implementation of complex analog filter in silicon based on lattice prototype.

In Chapter 4, a 2.4 GHz front-end for Bluetooth is designed with the techniques proposed in preceding chapters, and is implemented in TSMC 0.18-μm digital CMOS process. Post-simulation results from Cadence SpectreRF tools are analyzed and compared with those in the literature. Our designed MRFEC consumes considerably less power than those reported, with comparable performance in the other aspects. Therefore, the effectiveness of our design approaches is clearly demonstrated.

Finally, Chapter 5 summarizes the thesis work, presents future research directions on low-power integrated RF front-end in CMOS, and gives the conclusion.

2 BACKGROUND

The design of integrated front-end is a complicated job involving tradeoffs at four levels: device technology, integrated circuit device, front-end building block, and front-end architecture [24]. RF characteristics of device technology impose physical limits on RF performance of the front-end, particularly limiting its frequency response. To utilize the device technology to its full potential in terms of RF-band operation, how to construct integrated circuit devices such as integrated transistors becomes important. Further, to accommodate advantages and disadvantages of available integrated circuit devices, the topology of RF building blocks such as LNA has to be carefully designed to meet the specification while consuming minimum resources such as power, chip area, etc. Finally the front-end architecture determines how the front-end specification should be distributed among RF building blocks, and consequently influences the front-end performance significantly.

Research efforts to design low-power high-performance integrated front-end at the mentioned four levels could be broadly classified into two categories: design optimization and topology improvement. Design optimization concerns modeling and analyzing circuits and devices to derive the optimum values of design parameters such as the optimum number of fingers in a multi-finger transistor structure [48]. Meanwhile topology improvement involves modifying circuit structure or device layout to promote RF performance such as gain, stability, etc. One example is 3D spiral inductor [44].

Existing work on RF front-end design in digital CMOS technology addresses various issues at the higher three levels which are integrated-device level, building-block level, and architecture level [1]. Most design techniques at integrated-device level, however, are not scalable and could not be implemented with standard digital CMOS process without increasing costs [45]. For example, the fabrication of high-quality metal-insulator-metal (MIM) capacitor requires two additional masking steps beyond those needed for a pure logic process flow [44]. For this reason, emphasis will be given to design efforts at building-block level and architecture level in following discussion.

2.1 Preliminaries

A RF front-end provides a convenient interface between electromagnetic fields and digital signal processing [32]. From the perspective of signal processing, major functions of a RF front-end include gain (to convert the usually weak signals to convenient amplitude levels for further processing) and frequency conversion (to translate signals to convenient frequency bands for further processing).

A typical CMOS RF (receiver) front-end for 1.9-GHz PCS (Personal Communication Standard) headsets with heterodyne architecture is shown in Figure 2.1 [33]. As the first component in the receiver chain, the duplexer (DUP) isolates the received signal from transmitted signal. After passing the duplexer, the RF signal is amplified by the low noise amplifier (LNA). The bandpass filter BPF1 suppresses the image, while the mixer down-converts the receive band to an intermediate frequency (IF) centered at 260 MHz. The IF signal is further filtered by the bandpass filter BPF2 before it is amplified by an IF amplifier [33]. The building blocks (LNA, mixer, filter, etc.) involved here will be explained shortly.

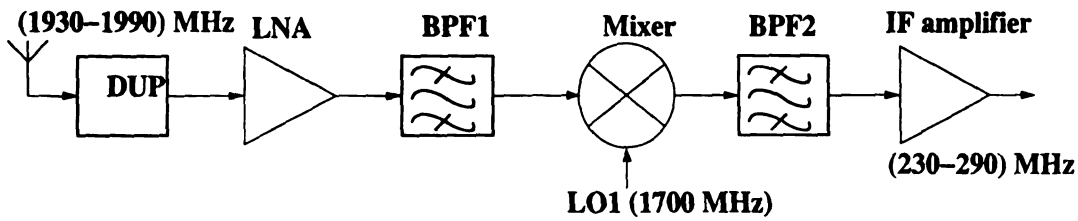


Figure 2.1: RF (Receiver) Front-End for 1.9 GHz PCS Headset [33].

The key parameters for measuring performance of a RF front-end are gain, noise factor, gain compression point, third-order interception point, blocking point, and power consumption. Gain describes the signal-amplifying capability of front-end. Noise factor describes to what degree the front-end degrades the signal-to-noise (SNR) ratio of signal. Gain compression point, third-order interception point, and blocking point characterize front-end linearity in different aspects.

The voltage gain of a front-end is defined as

$$G_v = \frac{A_{IF}}{A_{RF}},$$

where A_{IF} is the amplitude of IF signal at front-end output, and A_{RF} is the amplitude of RF signal at front-end input.

The noise factor of a front-end is defined as

$$F = \frac{SNR_{in}}{SNR_{out}},$$

where SNR_{in} and SNR_{out} are signal-to-noise ratios at front-end input and output, respectively. Then the noise figure of a front-end is given by

$$NF = 10\log F$$

Assuming the input signal to front-end has single frequency component ω_{RF} and amplitude A_{RF}, the voltage gain G_v decreases as A_{RF} increases due to the effect of nonlinearity. Consequently, $A_{-1dB,\,in}$, the gain compression point, is defined as A_{RF} for which G_v is 1 dB less than what it is supposed to be in the ideal case (e.g. without nonlinearity).

Consider the case that the input signal to front-end has two frequency components of ω_{RF} and ω_{block}, for which amplitudes are A_{RF} and A_{block}, respectively. Then G_v

decreases as A_{block} increases for $A_{RF} \ll A_{block}$ due to the effect of nonlinearity. Hence the blocking point $A_{block,\,in}$ is defined as A_{block} for which G_v drops to zero.

Consider the case that input signal to front-end has two frequency components of ω_{RF1} and ω_{RF2}, for which amplitudes are A_{RF1} and A_{RF2}, respectively. Due to the effect of nonlinearity the output signal contains new frequency components of ω_{IF1} and ω_{IF2} given by

$$\omega_{IF1} = 2\omega_{RF1} - \omega_{RF2}$$
$$\omega_{IF2} = 2\omega_{RF2} - \omega_{RF1}$$

For wireless applications employing FDMA, it is quite likely that ω_{IF1} and ω_{IF2} lie in the frequency bands for some other channels [3]. Consequently, G_v, the voltage gain for output signal at ω_{IF1} decreases as A_{RF1} and A_{RF2} increase, and so does the voltage gain for output signal at ω_{IF2}. This effect is usually caused by the third-order nonlinearity of front-end [105]. Assuming A_{RF1} and A_{RF2} always have the same value, then A_{IIP3} is defined as A_{RF1} for which G_v for frequency component ω_{IF1} at front-end output drops to zero.

2.2 Front-End Architecture

The most important consideration in choosing front-end architecture is the performance of image rejection. As shown in Figure 2.2, both the signal and its image fall into the same IF band after downconversion. Therefore in the presence of a strong image, the signal may be overwhelmed after downconversion. The common approach to solving this problem is to reject the image signal with a BPF or LPF before the downconversion stage [105]. A common measure for the degree of image rejection is image-rejection ratio (IRR), which is defined as the ratio of signal power to image power at front-end output while both signal and image have the same power at front-end input.

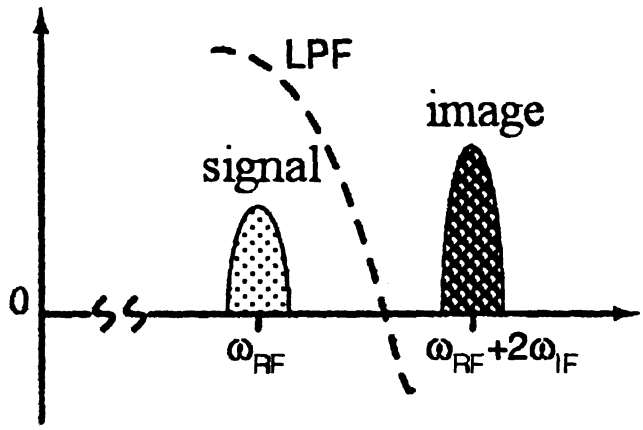


Figure 2.2: Image Rejection in RF Front-End.

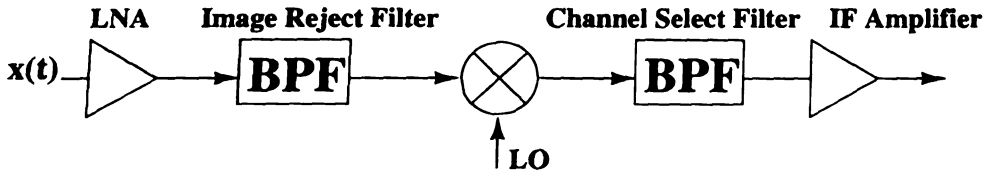
The integrated active filter in silicon can only achieve IRR no more than 40 dB [34]. This disadvantage essentially limits the use of integrated CMOS RF front-end in lucrative mobile communication applications such as GSM headsets that usually require IRR higher than 80 dB [80]. Front-end architecture plays a dominant role in addressing this issue.

The key design parameter of front-end architecture is intermediate frequency (IF), which indicates the tradeoff between image rejection and channel selection [3]. A higher IF results in higher degree of image rejection, lower degree of channel selection, and more power consumption. Good understanding of this point is important for choosing proper front-end architecture to meet design specification.

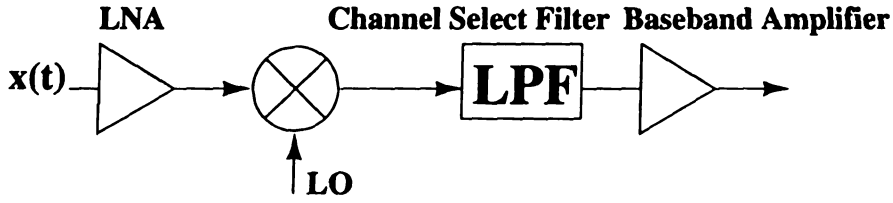
Four types of front-end architecture are available: high-IF architecture, zero-IF architecture, low-IF architecture, and image-rejecting architecture [88].

The high-IF architecture is shown in Figure 2.3 (a). Typical value of IF for such architecture ranges from 80 MHz to 300 MHz for RF applications [102]. While relaxing the requirement of image filtering, the use of high IF, however, results in IF processing electronics of high power consumption.

The zero-IF architecture is shown in Figure 2.8 (b), where image rejecting filter as well as IF processing electronics is eliminated, and only a LPF is needed for channel selection [3]. Such architecture, however, is sensitive to LO leakage, DC offset, and 1/f noise [3]. One way to deal with the disadvantages of zero-IF scheme is to employ multiphase downconversion at the cost of increased design complexity and more power consumption [112].



(a)



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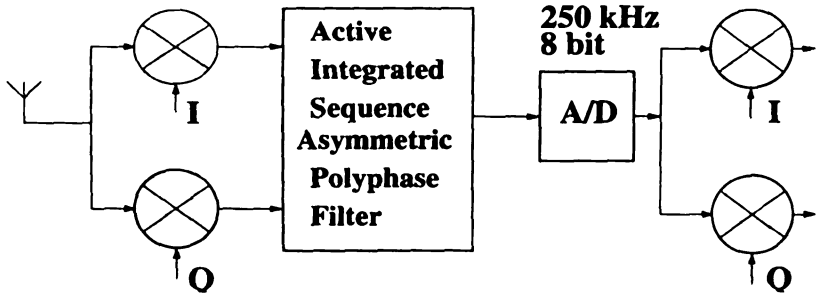

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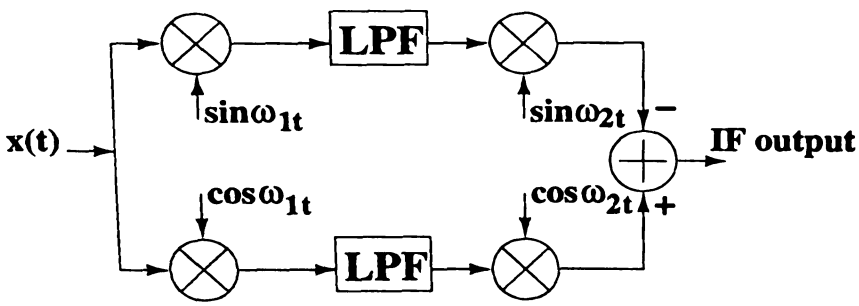


(d)

Figure 2.3: Front End Architectures: (a) High IF; (b) Zero IF; (c) Low IF [88]; and (d) Image Rejecting (Weaver).

The low-IF architecture is shown in Figure 2.3 (c). Typical value of IF for such architecture ranges from 1M to 3M for RF applications [28]. The use of low IF makes the receiver insensitive to DC offset and beyond the 1/f noise corner while maintaining the advantages of zero-IF scheme.

One image-rejecting architecture (Weaver) is shown in Figure 2.3 (d). The image-rejecting architecture removes image by cancellation. Therefore no image-rejecting filters are needed. However, the scheme is sensitive to mismatching of integrated components. Consequently the image rejection ratio is limited to 40dB, which is too low in the cases of personal wireless communication applications such as GSM [3].

Current trends in RF front-end research are multiband, wideband, and auto-tuning for mismatch. Multiband operation is achieved by using multiple LNA's and mixers [99], meanwhile wideband operation is achieved by using LNA's with feedback loop [31]. It is also shown recently that the phase error caused by mismatch in Weaver architecture can be calibrated with least mean square (LMS) technique [101].

In the design of integrated front-end in CMOS, the low-IF scheme appears attractive because it is amenable to integration without troubles such as DC offset and 1/f noise. However, a low IF makes it difficult to reject image signal before downconversion. In a typical low-IF Bluetooth front end, ω_{RF} and ω_{IF} equal 2.4 GHz and 2 MHz, respectively. Considering that the typical IRR requirement for Bluetooth front end is 50dB, then the required attenuation in the transition band of IR filter around ω_{LO} is about 250,000 dB per octave! To eliminate this problem, the image could be removed after downconversion with a complex analog filter (CAF) [98], as will be explained later in this chapter.

2.3 Front-End Building Blocks

2.3.1 Low Noise Amplifier

An ideal low noise amplifier (LNA) amplifies the incoming signal without adding noise or causing distortion. The most important function of LNA in a RF receiver is to alleviate the degradation of system noise performance caused by the inherently noisy RF frequency-conversion devices (e.g. RF mixer) in following stages. Meanwhile a typical LNA itself exhibits nonlinear and noisy characteristics that degrades system performance mainly due to the use of active devices [3]. As a result, merits from the use of LNA are partially offset by the disadvantages introduced simultaneously. A general characterization of LNA's impact on noise factor of overall RF receiver is given by the Friis equation [107]

$$F_{tot} = 1 + (F_1 - 1) + \frac{F_2 - 1}{A_{p1}} + \ldots + \frac{F_m - 1}{A_{p1}A_{p2}\cdots A_{p(m-1)}}, \tag{2.1}$$

where F_{tot} is noise factor of the RF system; A_{pm} and F_m are available power gain and noise factor of the *k*-th stage, respectively. To minimize the system noise factor F_{tot}, LNA is usually the first gain stage in a RF receiver, and therefore determines noise factor of the overall system according to the Friis equation.

Major requirements of LNA include low noise figure (NF), (reasonably) high gain, good linearity, good input/output (IO) matching, and good reverse isolation [3]. For the LNA to be used in portable applications such as GSM headsets, low power consumption is also required.

Conventionally there are three topologies for single-transistor LNA: common source (CS), common gate (CG), and common drain (CD) [3]. CD scheme hardly provides any gain, and CG scheme results in high noise figure. Consequently, CS scheme has been the dominant topology for the gain stage of RF LNA in CMOS because of its potential of high gain and low noise [62].

It is often difficult for a single-stage CS LNA to meet all requirements simultaneously, particularly when both good reverse isolation and high gain are required [3]. Therefore a current buffer is usually added to LNA as the second stage to improve reverse isolation for better stability without reducing LNA gain. The current buffer also extenuates the Miller effect. In practice an output buffer is often needed as the third stage of LNA to drive 50-Ω load.

2.3.1.1 Common-source cascode LNA with inductive degeneration

The classic common-source LNA topology is shown in Figure 2.4 (a) [54]. Such topology is often called the common-source cascode LNA with inductive degeneration (CSID LNA) in the literature. Note that the output buffer stage of LNA is not shown in the figure. In a CSID LNA, transistor M1 provides enough gain while transistor M2 serves as a current buffer. The cascode structure saves power because of current reuse. Good input matching as well as low noise figure is achieved by tuning parameters of LNA input network such as L_s, L_g, M1 bias, and M1 width. Larger output swing is achieved by use of inductive load L_d. The major advantage of CISD topology over its competitors is its capability of achieving good input matching without adding noise or limiting the transconductance of input stage. The good reverse isolation exhibited by the topology is a plus.

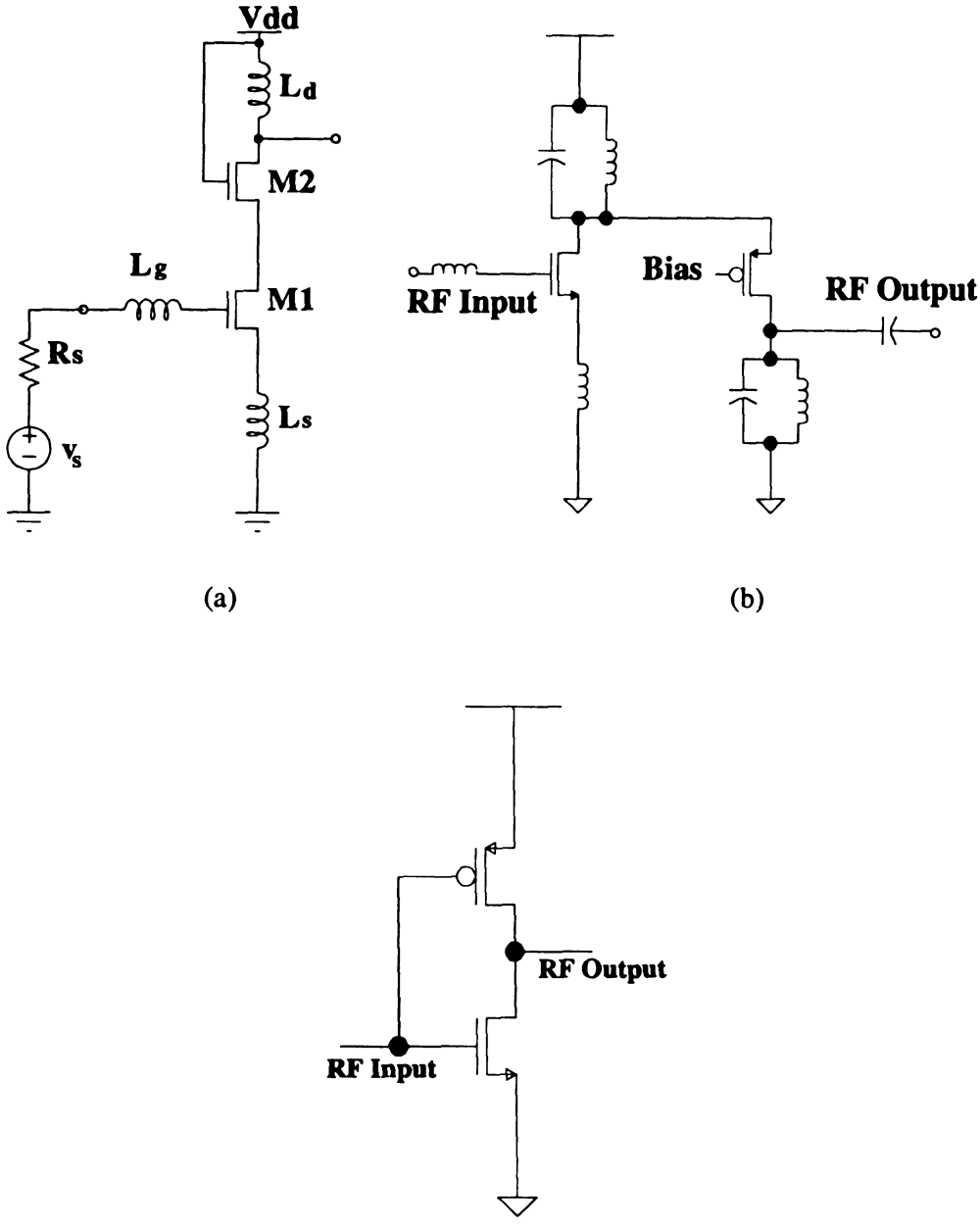


Figure 2.4: Integrated LNA Topologies: (a) Classic [54]; (b) LC-Folding [33]; and (c) CMOS Current-Reusing [53].

2.3.1.2 Topology improvement of CSID LNA

The major challenge in CSID LNA design toward low-power integrated implementation in CMOS is how to reduce power without affecting RF performance [24]. Many efforts have been devoted to addressing this challenge in terms of topology improvement, and several trends are observed.

The first trend is to save power with reduced power supply voltage. The main obstacle to the use of low supply voltage is the cascode structure employed in CSID LNA. One proposed technique eliminates cascode structure by use of LC folding structure shown in Figure 2.4 (b) and 1-V power supply [33]. The problem of linearity degradation caused by reduced supply voltage is solved by reducing LNA gain slightly [33]. The use of LC-folding technique with silicon-on-insulator (SOI) technologies in LNA could further reduce supply voltage to as low as 0.5 V [58].

The second trend is to save power by reusing drain current with PMOS transistor for larger gain. The classic topology for LNA with CMOS current-reusing is shown in Figure 2.4 (c), where CMOS amplifier is extensively used to increase gain. Traditionally LNA with such topology suffers from the poor RF performance of PMOS transistor. Recently PMOS technology has been improved significantly and low-power low-noise-figure LNA with PMOS and NMOS inductive degeneration has been reported [60].

The third trend is to save power by increasing Q-value of the RLC network at LNA output with active negative conductor [55]. The increased Q-value typically means larger gain, such that less current of LNA is needed to meet design specification. However, the resultant power saving depends heavily on the effectiveness of available LNA optimization methods, since negative conductor itself contributes considerable power consumption.

2.3.1.3 Design optimization of CSID LNA

The classic methodology for design optimization of CSID LNA uses the small-signal equivalent circuit of LNA input stage shown in Figure 2.5 for noise and gain calculation, where $\overline{v^2}_{rg}$ is RMS value of the gate-induced noise and $\overline{i^2}_d$ is RMS value of the drain current noise, both exhibited by transistor M1 [54].

In this methodology, the major tradeoff between RF performance and power consumption of LNA is identified as the one between the magnitude of gate induced noise and that of drain current noise. Intuitively, this is because that for fixed gate overdrive of transistor M1 a larger device width results in smaller input-referred drain current noise yet larger gate induced noise. Therefore, a minimum noise factor can be calculated for given power budget as well as a minimum power for given noise factor.

2.3.2 Mixer

A downconversion mixer in front-end translates the signal spectrum from RF carrier frequency (several Giga-Hz) to IF frequency (up to several hundred MHz) [4]. The mixer input is usually the amplified RF signal from LNA, filtered or not.

Performance of mixer is mainly characterized by its noise factor, linearity, and conversion gain [3]. The mixer linearity is further measured by two parameters, namely, 3-dB compression point A_{-1dB} and input third-order intercept point IIP3. Ideally a mixer should have low noise factor, high linearity and reasonable (several dBs) conversion gain. In mixer design for integrated front-end, the additional requirement of low power consumption has to be met.

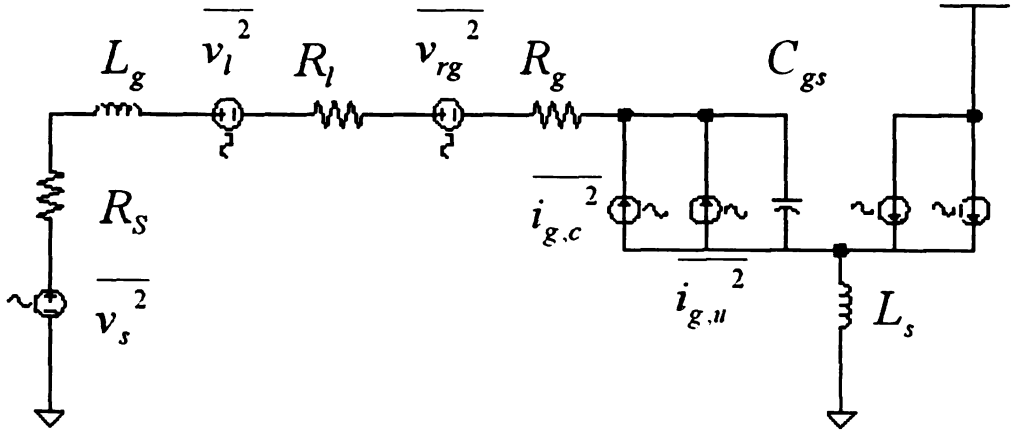


Figure 2.5: Small-Signal Equivalent Circuit for Noise and Gain Calculation in Classic CSID LNA Design [54].

There are two fundamental types of integrated mixer available: square-law-based mixer and multiplier-based mixer [105]. Usually the latter is preferred due to its superior performance of port isolation.

2.3.2.1 Gilbert cell

In practice the dominant topology for multiplier-based mixer is the Gilbert cell shown in Figure 2.6 (a) [105]. The Gilbert cell consists of two stages, namely, transconductance stage and multiplying stage. For the transconductance stage, the differential drain current of M1 and M2 is modulated by differential RF input signal connected to their gates. For the multiplying stage, the different drain current of M1 and M2 is multiplied by differential LO signal connected to gates of M3, M4, M5, and M6. The differential IF output results from the combination of the drain currents of M3, M4, M5, and M6 in some specific pattern.

Several important advantages make Gilbert cell attractive in integrated mixer design [105]. First, mixers based directly on multiplication generally exhibit superior performance because they ideally generate only the desired intermodulation product. This merit is crucially important for mixer in integrated front-end where the available linearity is limited by the low power budget. Second, because the inputs to a multiplier enter at separate ports, there can be a high degree of isolation among all three signals (RF, LO, and IF). Finally, the use of double balanced structure eliminates the LO frequency in output spectrum, which may have overloaded the subsequent stage because of the typically high value of LO magnitude. Furthermore, it can be shown that the IIP3 of double balanced structure is twice that of the active single-balanced mixer [108].

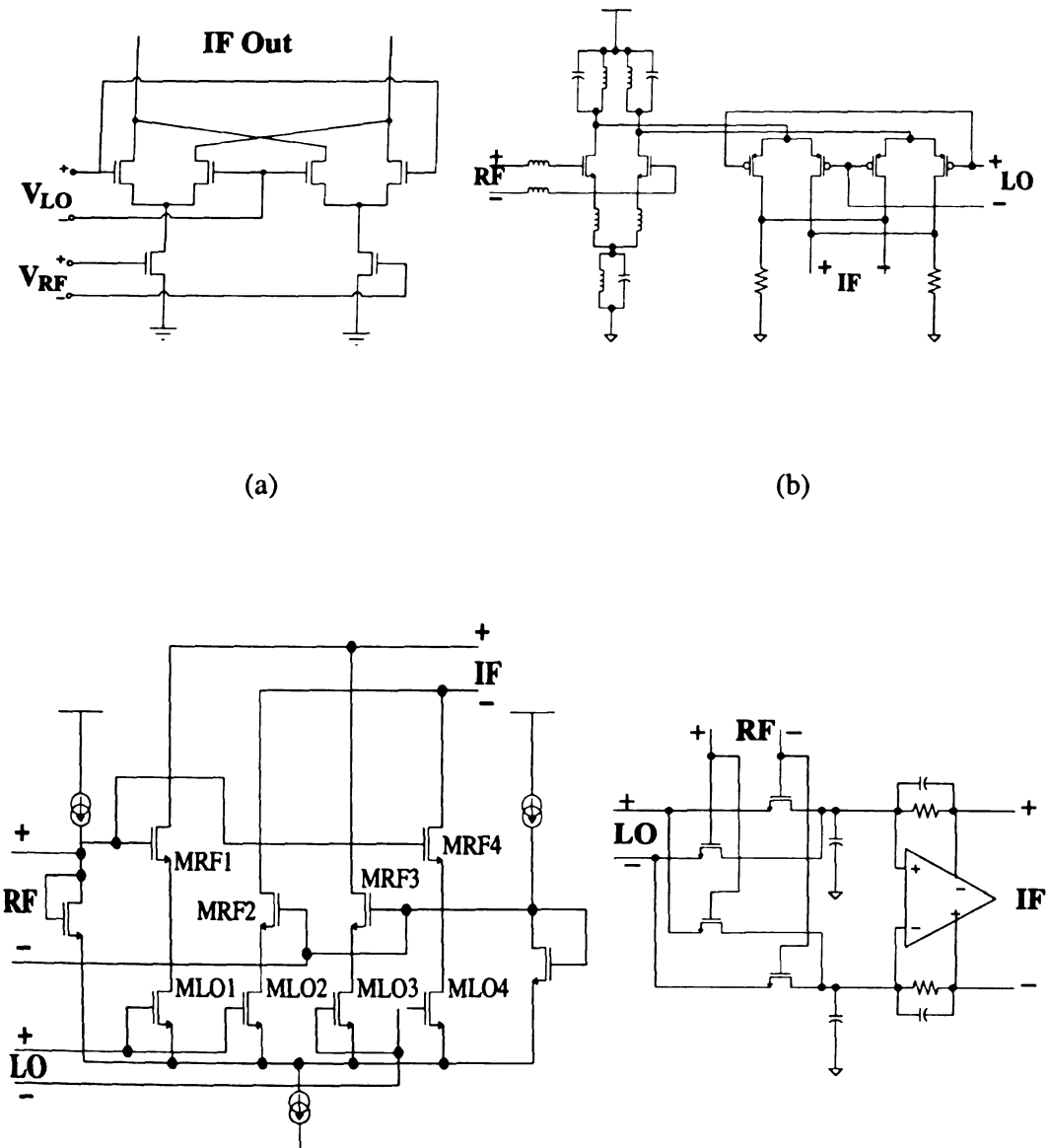


Figure 2.6: Integrated Mixer Topologies: (a) Gilbert Cell [105]; (b) LC-Folded Gilbert Cell [33]; (c) Triode-Biased Mixer [69]; and (d) Pass-Gate Mixer [66].

2.3.2.2 Topology improvement of Gilbert cell

Similar to the design of low-power integrated LNA, the key issue in low-power integrated mixer design is how to reduce power without degrading mixer RF characteristics, particularly mixer linearity. And progress has been made in two trends to address this issue.

The first trend is to save power with reduced power supply voltage. The use of LC-folding structure in Gilbert cell results in the mixer topology shown in Figure 2.6 (b), for which supply voltage can be as low as 1 V [33]. Another advantage of Gilbert cell with LC-folding is the increased linearity [33]. The major disadvantage of LC-folding Gilbert cell scheme is that the LC tank has to be tuned exactly at RF input frequency, which is very difficult for integrated LC implementation.

The second trend is to develop novel mixer scheme for low supply voltage and high linearity. The key idea here is to use transistors biased in triode region that is conventionally undesired. Consequently the supply voltage can be reduced and linearity improved. By contrast, transistors in a Gilbert cell are typically biased in saturation region with emphasis on reducing noise and switching nonlinearity [105]. One proposed mixer topology based on triode-biased transistors is shown in Figure 2.6 (c), where transistors MLO1-4 serve as multiplying stage and transistors MRF1-4 serve as transconductance stage [69]. Further improvement has been proposed to implements LO switch with MOS pass gate transistors as shown in Figure 2.6 (d) [66]. In this way, mixer power is further reduced because less transistors are used when compared with the scheme in Figure 2.6 (c).

2.3.2.3 Design optimization of Gilbert cell

The most important part of design optimization for integrated mixer is distortion analysis, which analyzes nonlinear effects (e.g. intermodulation) and predicts IIP3 as well as other linearity parameters.

Generally there are two ways to deal with distortion analysis in integrated circuits.

One way is to employ Taylor series to model the intermodulation behavior as given by following equation [3]

$$y(t) = a_0 + a_1 x(t) + a_2 x(t)^2 + a_3 x(t)^3 + \dots \quad , \tag{2.2}$$

where $x(t)$ is the input AC signal (e.g. $v_{rf}\cos\omega_{rf}t$), and $y(t)$ is the output AC signal. Therefore in the case of two-tone intermodulation, the value of IIP3 is determined by coefficients a_2 and a_3. Such method has been known to predict mixer gain characteristics well but not mixer IIP3 [97].

The other way is to model mixer intermodulation behavior with Volterra series [96], where the mixer output is represented in following form

$$y(t) = A_1(s)x(t) + A_2(s_1,s_2)x(t)^2 + A_3(s_1,s_2,s_3)x(t)^3 + \dots \quad , \tag{2.3}$$

where $x(t)$ is AC input signal, and $A_n(\circ)$ is the Volterra series coefficient which is a linear function of n number of frequencies. Though the way using Volterra series predicts mixer intermodulation behaviors very well, the computation involved is quite complicated and is not suitable for hand calculation in design. For this reason, such approach mainly finds its applications in RF simulators such as Cadence SpectreRF.

2.3.3 Integrated Continuous-Time Filter

Integrated filters are needed in front-end for image rejecting and channel selection. General requirements of integrated filters are high Q, low insertion loss, high dynamic rage, and low power consumption [82].

Conventionally there are two classes of integrated filters, which are switched-capacitor (SC) filter and continuous-time (CT) filter [75]. The SC filter utilizes the excellent matching characteristics of CMOS integrated capacitors, yet suffers from aliasing effect. The CT filter does not has the aliasing problem of SC filter, yet suffers from the significant process variation of digital CMOS technology, because center frequency of the filter heavily depends on the absolute values of integrated capacitors and transistors. Classic techniques for implementing integrated CT filter are active R-C filter [74] and active MOSFET-C filter [77]. All these implementations of SC filters and CT filters employ integrated operational amplifiers (OpAmp's). Hence the poor performance of integrated OpAmp available in CMOS technology becomes a common limiting factor for conventional analog filters. Because of the drawbacks mentioned above, the operating frequency range of conventional SC and CT filters in standard digital CMOS technologies is less than 1 MHz [5].

2.3.3.1 OTA-C continuous time filter

Recently CT filters implemented with operational transconductance amplifiers (OTAs) and capacitors have received much attention due to its good performance in high-frequency range [5,76]. A practical implementation of transconductor is called a OTA, and

integrated OTA-C bandpass filters in CMOS operating at 10.7 MHz and 12 MHz have been reported [78,110].

A typical first-order lowpass OTA-C filter is shown in Figure 2.7 (a) [5], where an integrator is constructed by the capacitor and transconductor on the left, meanwhile the transconductor on the right acts as an active resistor.

Three reasons account for the success of integrated OTA-C filter. First, the use of OTA instead of OpAmp in the filter makes high-frequency operation possible due to the low impedances of transconductor internal nodes [83]. Second, the use of OTA enables the tuning of filter after fabrication [76]. Finally, the use of OTA relaxes output swing and dc-gain requirements, hence reduces the power consumption [111].

General requirements of OTA are low power, low noise, and high linearity. For active filter in integrated RF front-end for image rejecting, linearity is a particularly important issue because of the significant magnitude of amplified signal from previous gain stages (LNA and mixer) that appears at filter input.

Compared with conventional passive RC filters, OTA-based active filters still suffer from performance loss in several important aspects, which are increased power consumption, degraded linearity, and reduced quality factor at high frequencies [79]. Low linearity results from the inherent nonlinearity of transconductor and capacitor, meanwhile low Q is mainly caused by the mismatching of integrated components. The key to reduce the performance loss is to use OTA that behaves well at RF frequencies. Ideally such OTA should have high DC gain, low noise, high output impedance, low input impedance, enough bandwidth, and excellent linearity.

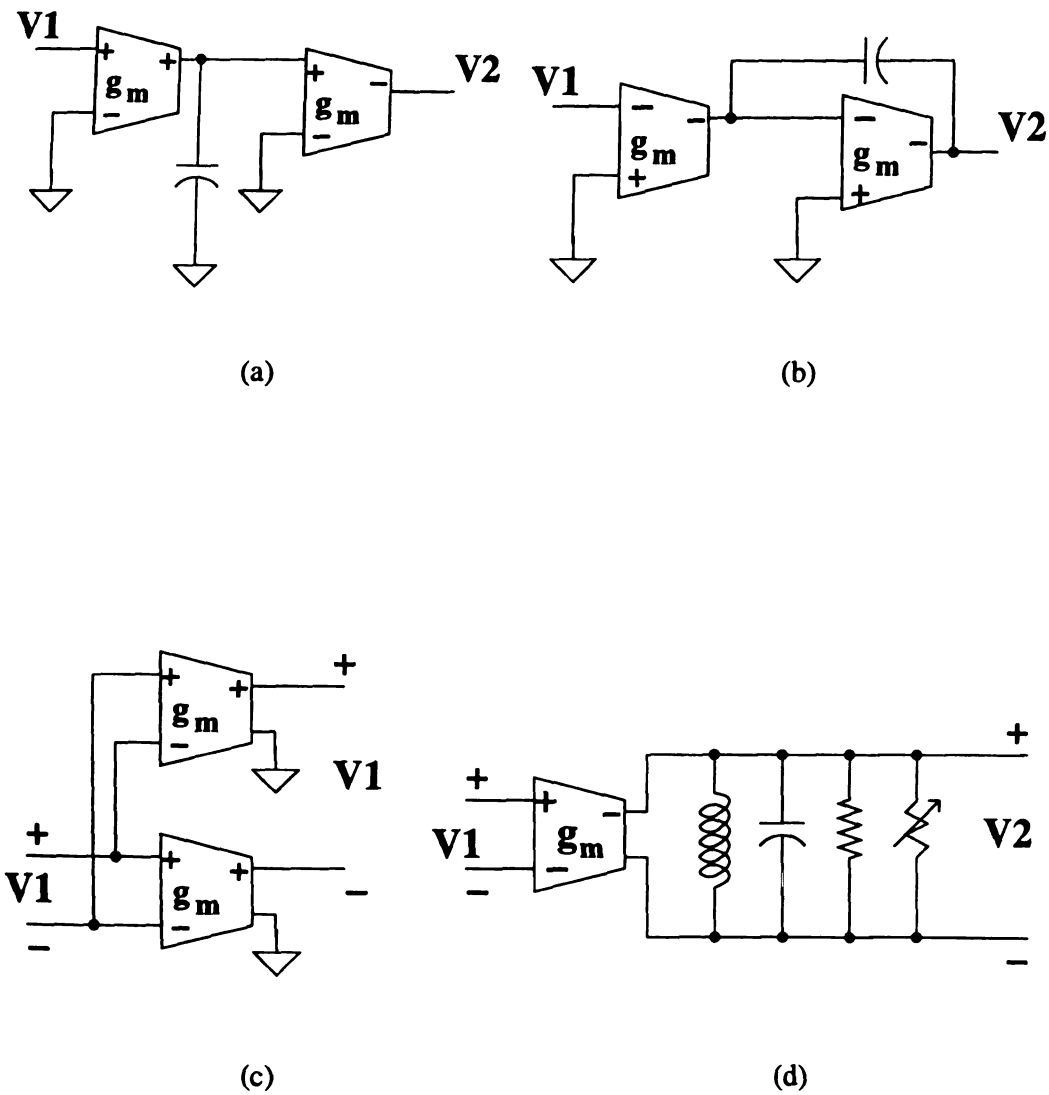


Figure 2.7: Integrated OTA-C Filter Topologies: (a) Classic [6]; (b) OTA [112]; (c) Balanced [80]; and (d) Q-Enhanced [88].

Several efforts have been made to deal with the problems of integrated OTA-C filter. In Figure 2.7 (b), a capacitor is connected in a feedback loop around the high gain amplifier which makes the input of the amplifier to appear as a virtual ground [111]. In this way, the requirement of output swing is relaxed, and linearity is improved. In Figure 2.7 (c), a balanced structure of transconductor cell is designed to cancel the second-order nonlinearity at the output [79]. In Figure 2.7 (d), negative conductor is used to boost the Q-value of integrated OTA-C filter [87].

Among the proposed schemes of OTA for improving linearity, Nauta's scheme in Figure 2.8 [81] is attractive because of its good linearity and high quality factor [83][106][3]. Being based on inverters, this balanced transconductor is very suitable for low voltage applications; further, the absence of nodes internal to the transconductor enables the straightforward implementation of advanced filter architectures, since the only parasitic time constants introduced by the transconductor are those associated to the distributed nature of the transistor channels [109].

2.3.3.2 Complex analog filter

The use of low IF in RF front-end relaxes the requirement of channel selection filter and reduces power consumption of analog electronics for IF signal processing [88]. Meanwhile troublesome effects such as DC offset, flicker noise, and mixer LO feedthrough are avoided. These advantages may, however, be offset by the expensive external bandpass filter (BPF) required, since the high value of quality factor (Q) of image-rejecting filter resulting from low IF can not be achieved with available integrated BPF, either passive or active [45]. To reduce Q-value of needed BPF while maintaining a low IF, the image-rejecting function has to be performed on IF signal *after* the downconversion stage, when the

downconverted signal and image are the same in frequency yet opposite in phase. In this way the required Q-value of BPF could be reduced to as low as three for Giga-Hz front-ends [64]. To reject the image a complex analog filter that attenuates negative-frequency components while keeping positive-frequency components has to be used.

There are two ways to build a complex analog filter: frequency translation [109] and sequence asymmetric filtering [94]. The first way converts a low pass filter (LPF) into a complex band pass filter (BPF) employing frequency translation. The second way attenuates the input signal sequence of negative phase using asymmetric polyphase network (also called *lattice*). The frequency-translation-based approach has been popular since its design process is similar to that of common LPF. However, the lattice-based approach has the potential of achieving less power consumption than the frequency-translation one does. The reason is that the gyrators heavily used in frequency-translation approach are no longer needed in lattice-based approach.

Existing research efforts tend to construct analog complex filter using frequency-translation approach based on operational transconductance amplifier (OTA), and focus on the design optimization of LPF prototype needed, such as Butterworth LPF [64], or Chebyshev LPF [109].

2.4 Research Topics

Though much progress has been made toward low power in the design of integrated CMOS front-end, power consumption remains the major factor limiting the use of such front-end in commercial portable communication applications. The problem here is how to effectively reduce front-end power *without* degrading RF performance or increasing costs.

One promising solution is to develop novel ways of analyzing front-end to gain a good understanding of front-end behavior at RF frequencies. Based on the analysis, efficient methods of design optimization for low power can be developed without adding costs, as have been shown by several previous attempts [54][57].

In this thesis work we investigate novel ways of analyzing front-end building blocks by considering several factors that affect building-block performance significantly, such as the very low quality factor of integrated inductor. Effects of such factors have not been properly accounted for in previous work on design analysis within the low-IF front-end architecture we used in this thesis work. We further showe that good design analysis helps develop novel topology for front-end building blocks. The topics investigated in the thesis work are listed below.

1) Analyze the noise performance of RF CMOS LNA with integrated inductors of very low (<10) quality factor. Develop method of noise-figure-constrained optimization for reducing LNA power.

2) Analyze the linearity performance of RF CMOS mixer implemented with Gilbert cell. Develop new mixer topology for improving linearity.

3) Analyze the image-rejecting operation of complex analog filter based on asymmetic polyphase network. Develop new way to implement the complex analog filter for saving power.

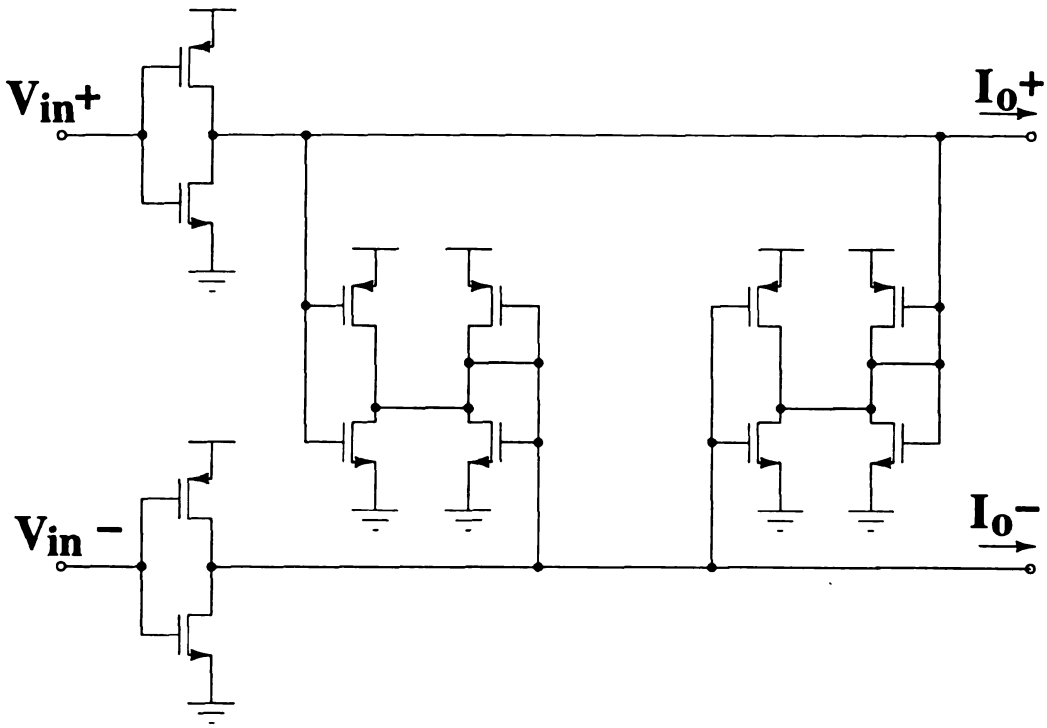


Figure 2.8: Nauta's Transconductor [106].

3 DESIGN APPROACH

The proposed front-end employs the low-IF architecture shown in Figure 3.1 and has three types of building block: low noise amplifier (LNA), mixer, and complex analog filter (CAF). The received RF signal is first amplified by LNA, then is downconverted to two quadrature signals I and Q with the mixers. The resultant I and Q signals at IF frequency are filtered by the CAF to reject the image. The LO signals needed by mixers are generated externally.

In proposed front-end the LNA employs CSID topology, the mixer is based on Gilbert cell, and the complex analog filter uses asymmetric polyphase network. Our proposed methods for analyzing and designing the front-end building blocks are detailed below.

3.1 Low Noise Amplifier

3.1.1 Tradeoff between Performance and Power

The first step in LNA design for low power is to understand how the LNA performance varies with power consumption. Particularly, short-channel effects of MOS transistors have to be properly considered.

As mentioned in Chapter 2, LNA performance is described by a set of parameters including noise factor (or noise figure), gain, linearity, input/output matching, and reverse isolation, etc. According to the Friis equation, however, the fundamental function of LNA

concerns only two parameters: noise factor and gain. The reason is that LNA noise factor adds to the noise factor of front-end, and LNA gain reduces the noise contributions from building blocks that follows LNA in receive path. Hence for simplicity without losing generality, our study here will focus on how the power consumption is related to noise factor and voltage gain of LNA. This issue has not been treated well in the literature and an in-depth discussion is worthwhile.

In following analysis we begin with the LNA that employs long-channel NMOS devices, then study the LNA in the case of short-channel NMOS devices by considering major short-channel effects.

The input stage of CSID LNA determines noise factor the front-end, and is typically implemented with a single NMOS transistor [54]. Meanwhile the output stage of LNA provides the input stage with a steady load to maintain a reasonable gain. Therefore the noise factor and gain of LNA can be calculated using the small-signal equivalent circuit shown in Figure 3.2, where the output stage is represented as an impedance Z_L. Only the drain current noise of NMOS transistors is considered since it dominates the intrinsic noise of MOS devices at RF frequencies [3]. The root mean square (RMS) value of input-referred drain current noise is given by [54]

$$\overline{v^2}_{n,in,ch} = 4kT\frac{\gamma}{g_m}\Delta f, \tag{3.1}$$

where k is Boltzmann's constant, T is the absolute temperature in kelvins, γ equals 2/3 for long-channel NMOS devices in saturation, g_m is device transconductance, and Δf is the noise bandwidth in hertz.

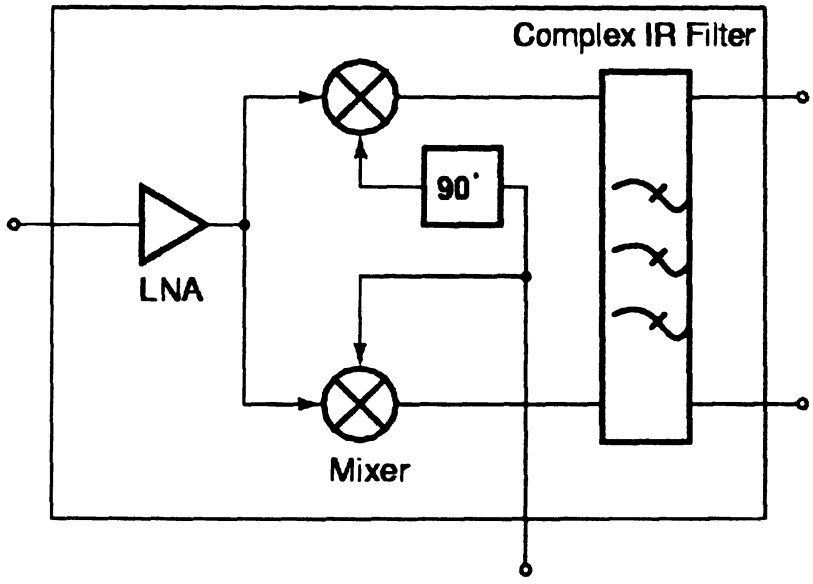


Figure 3.1: Low-IF Architecture of Proposed Front-End.

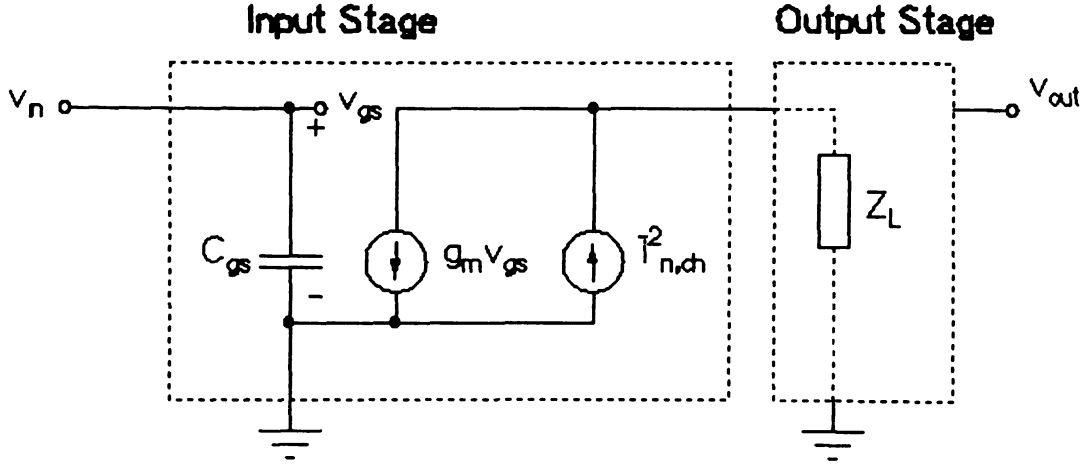


Figure 3.2: Generic Model of Input Stage of CSID LNA.

The device transconductance of long-channel NMOS devices is given by

$$g_m = \frac{2P_d}{(V_{gs} - V_t)V_{dd}}, \tag{3.2}$$

where P_d is power consumption, V_{gs} is gate-source bias voltage, V_t is the threshold voltage of NMOS devices, and V_{dd} is power supply voltage. For a given IC fabrication process, V_{dd} and V_t are usually fixed.

It follows that

$$\frac{g_m}{P_d} \propto \frac{1}{V_{gs} - V_t}. \tag{3.3}$$

The value of gate overdrive $V_{gs} - V_t$ is chosen only large enough to keep the NMOS transistor in active region, and changes little around several hundred millivolts [105]. Hence for simplicity without losing much accuracy it is reasonable to assume that the value of $V_{gs} - V_t$ is constant.

Referring to Figure 3.2, the minimum noise factor is

$$F_{min} = \frac{\gamma}{R_s g_m}. \tag{3.4}$$

Meanwhile the voltage gain is calculated by

$$|A_v| = g_m |R_L|. \tag{3.5}$$

It follows from equation (3.3) that

$$g_m \propto P_d. \tag{3.6}$$

Finally we have

$$\frac{1}{(F_{min}-1)} \propto P_d, \tag{3.7}$$

$$A_v \propto P_d. \tag{3.8}$$

From above relations it is clear that higher power budget generally results in lower noise factor and higher gain. To reduce the power, however, we would prefer the minimum (or nearly minimum) power budget required to meet the design specification. In practice the tuning of A_v is much easier than that of noise factor since the former is determined by LNA input stage (g_m) and LNA output stage (Z_L), while the latter depends almost solely on the characteristics of LNA input stage. Therefore the design of LNA is essentially to optimize design parameters such that the specified noise factor is achieved with minimum power consumption and reasonable gain. Note that the gain of LNA output stage can be utilized as an additional degree of freedom to compensate the gain loss resulting from the optimization on LNA input stage.

So far our analysis is based on long-channel NMOS device model. For short-channel transistors, the preceding analysis is still valid and explanations follow.

The I-V characteristics of short-channel NMOS devices with velocity saturation effect is given by [105]

$$I_{d,\,short} = I_{d,\,long}\frac{1}{1+\theta V_{od}}, \tag{3.9}$$

where $I_{d,long}$ is the drain current calculated with long-channel assumption, θ is a small real number between zero and unit, and V_{od} is the gate overdrive. It is easily seen from above

equation that in short-channel regime g_m has weaker dependence on gate overdrive than it does in long-channel regime, as is characterized by following relation

$$\frac{g_m}{P_d} = \left(\frac{1}{V_{gs} - V_t} - \frac{\theta}{2}\right). \tag{3.10}$$

With constant gate overdrive, the same relations between performance and power can be drawn as those in equations (3.7) and (3.8). Two important observations are made here. First, while reduced gate overdrive can increase the value of (g_m/P_d) effectively in long-channel regime, such effect tends to diminish as the IC technology scales down, as is shown in equation (3.10). The reason is that reduced channel length increases the strength of horizontal electric field in device channel, therefore the effect of velocity saturation becomes significant at lower drain-source voltage, and larger value of θ is needed to model such change of device behavior [105]. Second, it can be shown that the value of short-channel (g_m/P_d) is smaller than that of long-channel, as illustrated by following equation

$$\frac{(g_m/P_d)_{short}}{(g_m/P_d)_{long}} = 1 - \frac{\theta(V_{gs} - V_t)}{2}. \tag{3.11}$$

The typical value of θ for 0.18-μm process is 0.4 V^{-1}. For a gate overdrive of 0.4 V, the value of short-channel (g_m/P_d) is about 8% less than of long-channel.

Consequently, in short-channel regime the low power requirement is more stringent due to the reduced (g_m/P_d) ratio. This makes the development of low-power design methodology even more desirable. On the other hand, the value of g_m becomes less sensitive to the change of P_d, therefore new methods to reduce power consumption have to be explored.

3.1.2 Noise Analysis

The circuit topology of CSID LNA to be studied is shown in Figure 3.3. As mentioned in Chapter 2, the classic method for noise analysis deals with the tradeoff between induced gate noise and drain current noise of NMOS devices [54]. While this method works well for LNA with external inductors, it has problem dealing with the design of integrated LNA in CMOS. To see why, we first note the fact that currently available integrated inductors exhibit low values of quality factor between 3 and 10 [41]. Then it is seen from Figure 3.4 that with such integrated inductors a lower bound of noise factor exists for LNA with CSID topology:

$$F_{min} > 1 + \frac{R_l}{R_s}. \tag{3.12}$$

where R_l is the series resistance of L_g. At the frequency of 900 MHz, the typical inductance of L_g is 9nH, and quality factor is 3. In this situation F_{min} is larger than 1.8 (2.5 dB)! Further examination shows that the required inductance of L_g increases as the width of transistor M1 decreases. Since the thermal noise from low-quality L_g directly adds to the LNA noise factor, the impact of L_g overwhelms that of gate-induced noise as device width reduces.

As a result, we observe a *new* tradeoff dominating the design of integrated LNA in CMOS, which is the tradeoff between gate inductor noise and drain current noise. Note that the noises from integrated inductors L_s and L_d are ignored for simplicity since they do not have significant impact on LNA noise factor. For a detailed treatment of the new tradeoff, we first describe the transistor and inductor models involved in hand calculation, then derive the noise factor of LNA as well as degree of input matching.

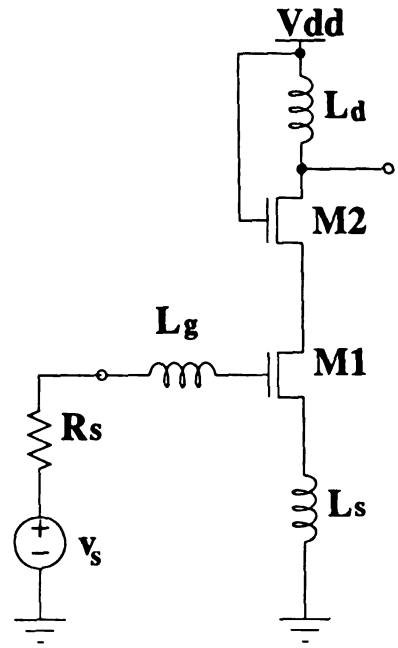


Figure 3.3: Cascode LNA with Inductive Source Degeneration

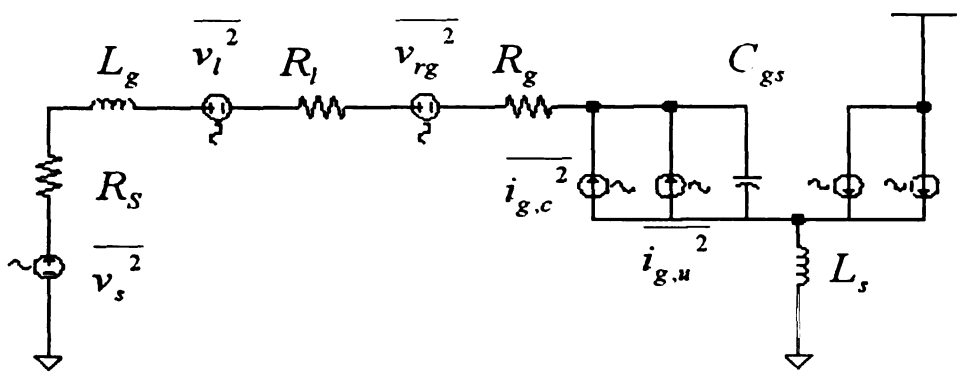


Figure 3.4: Small-Signal Equivalent Circuit for Noise and Gain Calculation in Classic CISD LNA Design [55].

3.1.2.1 NMOS Transistor model

Recently the I-V model of NMOS transistor considering velocity saturation effect has been widely used in the research on short-channel RF CMOS LNA design, where the square-law model is in general considered inappropriate due to short-channel effects [54,62]. However, it can be shown that for small gate overdrive the conventional square-law I-V model still holds for short-channel transistors. As we will see shortly, for LNA with CSID topology, large gate overdrive will result in the use of large integrated inductance, which is not favorable due to the significant degradation of LNA noise performance. So that for simplicity, square-law equation is used in our work to model DC characteristics of NMOS transistor

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L_{eff}}V_{od}^{\ 2}, \tag{3.13}$$

where L_{eff} is effective channel length of transistor M1 in Figure 3.3, V_{od} is the gate over-drive of transistor M1 given by

$$V_{od} = V_{gs} - V_{tn1}, \tag{3.14}$$

V_{tn1} is the threshold voltage of M1.

The power is given by

$$P = I_D V_{dd}, \tag{3.15}$$

where V_{dd} is the supply voltage.

The small-signal model of NMOS transistor for hand calculation is shown in Figure 3.5, where

$$C_{gs} = \frac{2}{3} C_{ox} W L_{eff}, \tag{3.16}$$

$$g_m = \mu_n C_{ox} \frac{W}{L_{eff}} V_{od}. \tag{3.17}$$

The transition frequency of NMOS transistor, ω_T, is given by

$$\omega_T = \frac{g_m}{C_{gs}} = \frac{3}{2} \frac{\mu_n}{L^2_{eff}} V_{od}. \tag{3.18}$$

Note that for specific fabrication process ω_T is solely determined by gate overdrive when velocity saturation effect is ignored.

3.1.2.2 Integrated inductor model

For hand calculation, we use the circuit in Figure 3.6 to model the integrated inductor, of which the quality factor is given by

$$Q_L = \frac{\omega_0 L}{R_L}, \tag{3.19}$$

where R_L is the series resistance of integrated inductor. The typical value of Q_L is between 3 and 10 [45].

3.1.2.3 Derivation of noise factor

The small-signal circuit for the input stage of CSID LNA is shown in Figure 3.7. The series resistance of L_s is ignored since usually the following relation holds for frequencies of Giga-Hz:

$$L_s \ll L_g. \tag{3.20}$$

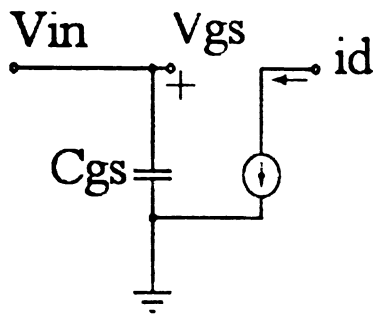


Figure 3.5: Small-Signal Model of NMOS Transistor for Hand Calculation.

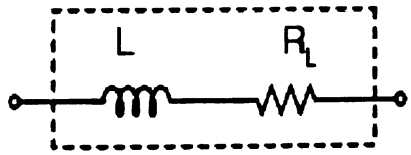


Figure 3.6: Simplified Model of Integrated Inductor.

The input impedance is given by

$$Z_{in} = (R_{Lg} + \omega_T L_s) + s(L_g + L_s) + \frac{1}{sC_{gs}}. \tag{3.21}$$

At the working frequency ω_0 the input impedance becomes real when

$$\omega_0^2(L_g + L_s)C_{gs} = 1. \tag{3.22}$$

At this time the input resistance is given by

$$Z_{in} = R_{in} = R_{Lg} + \omega_T L_s. \tag{3.23}$$

Usually we want that R_{in} is equal to R_s for perfect input matching which is, however, difficult to achieve in practice. To account for the effect of imperfect input matching, we define the following relation

$$\frac{\omega_0 L_g}{Q_{Lg}} + \omega_T L_s = \zeta R_s, \tag{3.24}$$

where ζ is a positive real number between unit and zero indicating the degree of imperfect input matching.

At high frequencies, the series resistance of L_g accounts for a considerable portion of input resistance of CSID LNA because of the low Q_{Lg}. Particularly, too large integrated L_g will make perfect input matching impossible when following relation holds

$$R_s < \frac{\omega_0 L_g}{Q_{Lg}}, \tag{3.25}$$

since ζ is always larger than unit. Therefore there exists an upper bound on the value of L_g, which is around 18nH for ω_0 of 1.8G Hz and Q_{Lg} of 4.

The small-signal circuit for calculating noise factor of CSID LNA is shown in Figure 3.8. Here we consider only channel noise of transistor M1 and thermal noise of the input stage. The noise of transistor M2 is ignored. The noise sources in the figure are characterized by

$$v_{ns}^2 = 4kTR_s, \tag{3.26}$$

$$v_{n,Rlg}^2 = 4kTR_{Lg} = 4kT\left(\frac{\omega_0 L_g}{Q_{Lg}}\right), \tag{3.27}$$

$$i_{nd}^2 = 4kT\left(\frac{2}{3}g_m\right), \tag{3.28}$$

where g_m is the transconductance of M1. The transconductance of LNA input stage at resonance is

$$G_m = g_m Q_{in} = g_m \frac{\omega_0(L_s + L_g)}{R_s + R_{Lg} + \omega_T L_s}. \tag{3.29}$$

With equations (3.23) and (3.24) we have

$$G_m = \frac{g_m}{(1+\zeta)R_s\omega_0 C_{gs}}. \tag{3.30}$$

Finally the noise factor of LNA is given by the following equation

$$F = 1 + \left(4kTR_{Lg} + \frac{8kTg_m}{3G_m^2}\right)\frac{1}{4kTR_s}$$

$$= 1 + \frac{\omega_0 L_g}{R_s Q_{Lg}} + \frac{2}{3}(1+\zeta)^2 R_s \frac{(\omega_0 C_{gs})^2}{g_m}. \tag{3.31}$$

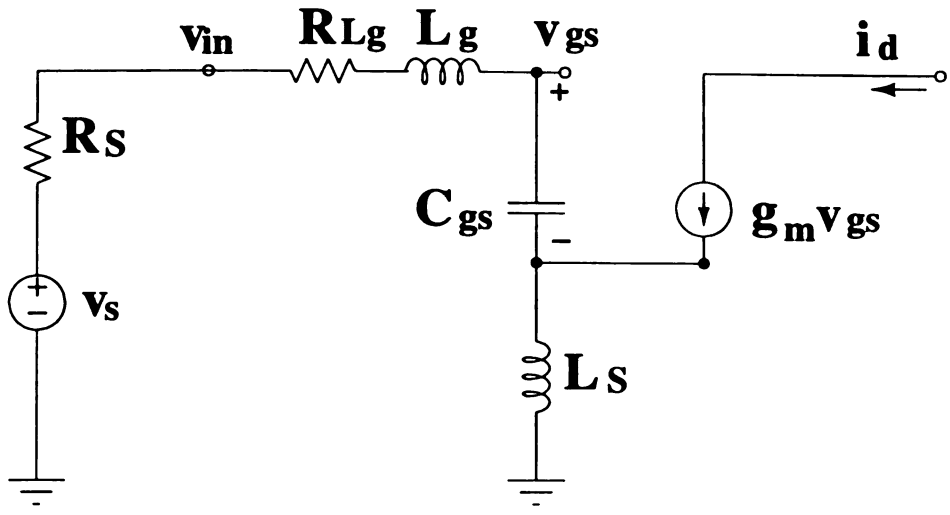


Figure 3.7: Small-Signal Circuit of Input Stage of CISD LNA.

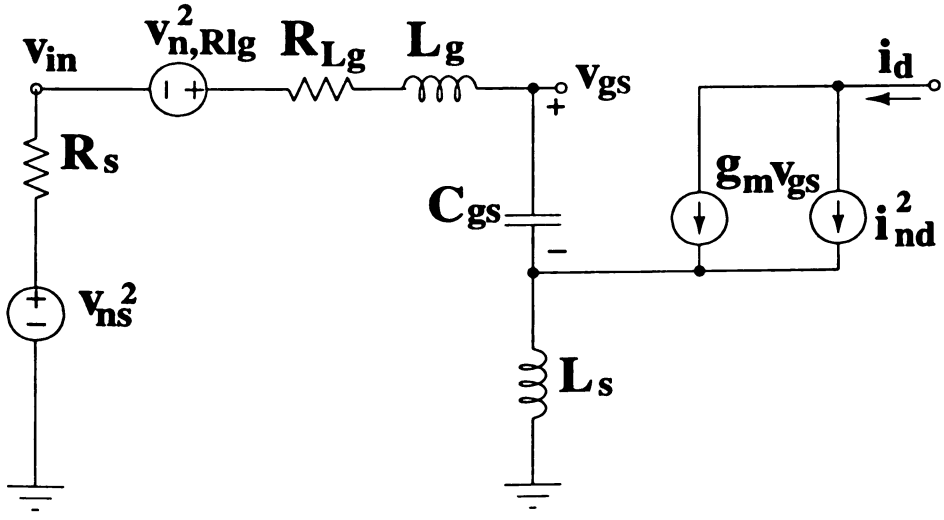


Figure 3.8: Small-Signal Circuit for Calculating Noise Factor.

3.1.2.4 Noise-constrained optimization for minimum power

Based on preceding analysis, we propose a novel methodology for noise-constrained optimization of CSID LNA design. The methodology is essentially to choose optimum parameter set for LNA such that given noise factor could be achieved with minimum power consumption. Further, it can be shown that the problem of noise-constrained optimization for minimum power is equivalent to that of power-constrained optimization for minimum noise.

As mentioned earlier in this chapter, the down-scaling of IC technology makes it desirable to explore new ways to reduce LNA power besides the method based on noise-power tradeoff. One promising way is to employ imperfect input matching. Though perfect input matching is usually assumed in classic treatment of CISD LNA design [55], such requirement may be relaxed for LNA in some wireless applications. In fact, the required S11 for Bluetooth LNA is only -10dB [104]. As will be shown, by adjusting S_{11} the noise factor can be reduced without increasing power. Consequently a quantitative method, which is not available in the literature, is needed to balance the tradeoff between the degree of input matching and noise factor.

To gain good insight into the noise-constrained optimization, we rewrite the noise factor in equation (3.31) as the function of V_{od}.

Let

$$L_{tot} = L_g + L_s . \tag{3.32}$$

With equations (3.23-31) we have

$$L_{tot} = \frac{V_{od}^2}{K_1}, \tag{3.33}$$

where

$$K_1 = \frac{4}{3} I_D \frac{1}{\mu_n} \omega_0^2 L_{eff}^2. \tag{3.34}$$

Note that K_1 is linear function of I_D.

Let

$$K_2 = 1.5 \frac{\mu_n}{L_{eff}^2}. \tag{3.35}$$

With equation (3.24), we have

$$L_g \approx L_{tot}. \tag{3.36}$$

With above equations, noise factor of LNA can be expressed in terms of V_{od} as below:

$$F \approx 1 + \frac{2}{3}(1+\zeta)^2 R_s \frac{K_1}{K_2} \frac{1}{V_{od}^3} + \frac{\omega_0 V_{od}^2}{K_1 R_s Q_{Lg}}. \tag{3.37}$$

With equations (3.33-3.37) the minimum noise factor given above can be rewritten as

$$F_{min} \approx 1 + 1.67(1+\zeta)^{0.8} \frac{\omega_0^{0.6}}{R_s^{0.2} K_1^{0.2} K_2^{0.4} Q_{Lg}^{0.6}}, \tag{3.38}$$

when

$$V_{od} = V_{od,opt} = \left(\frac{(1+\zeta)^2 K_1^2 R_s^2 Q_{Lg}}{K_2 \omega_0} \right)^{0.2} . \tag{3.39}$$

Particularly, in the case of perfect input matching where ζ is equal to unit, the minimum noise factor can be rewritten as

$$F_{min,\zeta=1} = 1 + 2.9 \frac{\omega_0^{0.6}}{R_s^{0.2} K_1^{0.2} K_2^{0.4} Q_{Lg}^{0.6}}, \tag{3.40}$$

when

$$V_{od,\zeta=1} = \left(\frac{4 K_1^2 R_s^2 Q_{Lg}}{K_2 \omega_0} \right)^{0.2} . \tag{3.41}$$

Since power consumption P is linear function of K_1, equation (3.38) indicates that for given power budget there exists a minimum noise factor. In other words, there exists a minimum power consumed by LNA to maintain a desired noise factor. To be specific, for given noise factor F the minimum power required is given by

$$P_{min} = V_{DD} I_D = \frac{1}{2} \frac{1.67^5 (1+\zeta)^4}{(F-1)^5} \frac{\omega_0 V_{DD}}{Q_{Lg}^3 K_2 R_s}, \tag{3.42}$$

when

$$K_1 = K_{1,min} = \left(2.9 \frac{\omega_0^{0.6}}{R_s^{0.2} K_2^{0.4} Q_{Lg}^{0.6} (F-1)} \right)^5 . \tag{3.43}$$

Several important observations are made from equation (3.42). First, lower noise factor requires higher power consumption. This point agrees well with the conclusion from our qualitative analysis earlier this chapter. Second, both the degree of input matching and

the quality factor of integrated inductor can be used to reduce power for given noise factor. This is evident from equation (3.42), where both lower ζ and higher Q_{Lg} results in lower P_{min}. However, low ζ, which means degraded input matching, may cause troubles such as antenna leakage and reduced gain. Meanwhile high Q_{Lg} simply makes the design of integrated inductor for use in LNA more difficult. Nonetheless, equation (3.42) reveals new ways to perform noise-constrained optimization on LNA toward low power.

Based on the preceding analysis, a four-step methodology for the design of low-power noise-constrained LNA is formulated below.

1. LNA noise factor is determined from the design specification of RF front-end. This can be done with the help of Cadence SpectreRF tools using behavioral simulation [115].

2. The bias and sizes of NMOS transistor M1 of LNA input stage as shown in Figure 3.3 are calculated from equations (3.13), (3.39), and (3.43) by assuming ζ of unit value and low inductor quality (e.g. Q_{Lg}= 3). Values of L_g and L_s are determined from equations (3.24), (3.32), and (3.33). Inductances and transistor sizes in LNA output stage are chosen using the classic power-optimization method [105]. The theory value of power consumption for the calculated parameters is determined from equation (3.42). Necessary simulation should be performed to tune the design parameters.

3. To further reduce power, the value of L_g could be reduced to degrade input matching. This means reduced value of ζ, and only the bias of transistor M1 needs to be changed as specified in equation (3.39). The resultant side effects include degraded LNA linearity and reduced LNA gain. Therefore simulation is needed to closely monitor the overall performance of LNA.

4. With design manpower permitting, higher quality factor of integrated inductor (e.g.Q_{Lg}= 8) can be used to achieve even less power. To do so, advanced design techniques [116] for integrated inductor in CMOS have to be applied, and more design time is expected.

3.1.2.5 Mapping from ζ to S11

In practice the degree of input matching is represented as S_{11}, one of the scattering parameters (S-parameters), instead of ζ in design specification. Following discussion presents a way to convert ζ defined by equation (3.24) to S11 which is the input reflection coefficient defined by following equation [105]

$$S_{11} = \frac{Z_L - Z_0}{Z_L + Z_0}, \tag{3.44}$$

where Z_L is load impedance, and Z_0 is the characteristic impedance of transmission line.

Assume that the source is perfectly matched to the other end of transmission line, so that

$$Z_0 = R_s. \tag{3.45}$$

At resonance, the input stage of LNA exhibits pure resistance, so that

$$Z_L = R_{in}. \tag{3.46}$$

At this time

$$|S_{11}| = \left|\frac{R_{in} - R_s}{R_{in} + R_s}\right|. \tag{3.47}$$

The above equation can be rewritten as

$$|S_{11}| = \left|\frac{1-\zeta}{1+\zeta}\right|, \tag{3.48}$$

where ζ indicates the degree of input matching, and is defined by equation (3.44). For given S_{11}, possible values of ζ are

$$\zeta_1 = \frac{1-|S_{11}|}{1+|S_{11}|}, \tag{3.49}$$

$$\zeta_2 = \frac{1+|S_{11}|}{1-|S_{11}|}. \tag{3.50}$$

Based on previous analysis, ζ_1 is always preferred for S11 calculation. Therefore theory value of S_{11} could be estimated with equation (3.49). For example, in Bluetooth applications S_{11} is usually required to be less than -10dB, this translates to a minimum ζ of 0.52. Consequently, ζ could be reduced to as low as 0.52 in exchange for reduced power consumption.

3.2 Downconversion Mixer

3.2.1 Tradeoff between Performance and Power

Adopting the same rationale used for LNA analysis, we first study how the mixer performance changes with power consumption. As mentioned in Chapter 2, the most important parameters of mixer performance include noise factor, conversion gain, and linearity. A mixer typically exhibits noise factor much higher than that of LNA due to its nonlinear function of frequency manipulation which translates noise in multiple RF bands to the IF signal band [90]. However, high noise factor is hardly a concern in mixer design since the noise requirement of mixer can be greatly relaxed according to the Friis equation with a properly-designed LNA. Furthermore, the use of a high-performance LO oscillator could reduce the mixer noise effectively. Conversion gain of several dBs is normally required for a mixer so that the LNA gain can be reduced to achieve better stability. For the active mixer commonly used in integrated RF front end, the conversion gain is proportional to the magnitude of LO signal, and little power is drawn from external LO source [70]. Therefore enough conversion gain can be achieved without increasing mixer power by using a low-power LO oscillator with appropriate magnitude.

The key parameter of mixer performance that limits the reduction in power consumption is linearity. This is because portable wireless applications typically requires the use of high-linearity mixer, of which the linearity dominates that of RF front-end [108]. Meanwhile the already tight power budget of portable wireless applications makes it difficult to further reduce power without degrading mixer linearity, considering that better linearity usually requires more power, and present methods for linearity analysis are either

unaccurate or complicated as mentioned in Chapter 2. Therefore good technique for linearity analysis is needed in low-power mixer design to develop a good understanding of how mixer linearity varies with power consumption.

Our work in this thesis gives a novel two-step approach to analyzing mixer linearity in terms of power consumption, and details are given below.

3.2.1.1 Two-step approach for linearity analysis of mixer

One important observation in active mixer design is that MOS device is the only circuit component capable of performing frequency translation in an active mixer, hence its linearity accounts for that of the RF front-end. By contrast, noise factor of LNA is determined by both circuit topology and MOS device noise. Consequently, the mixer linearity is determined by the linearity of NMOS devices used, and can be studied with a two-step approach described below (for simplicity only third-order intermodulation is discussed here).

1. The input-referred interception point of third-order intermulation (IIP3) for NMOS transistor that dominates the mixer linearity is derived.
2. The IIP3 of mixer is determined from that of NMOS transistor by use of a mapping circuit network.

The two-step approach is also illustrated in Figure 3.9. The first step provides insight on the tradeoff between IIP3 and power of NMOS device, whereas the second step gives insight on the tradeoff between IIP3 and power of the mixer. In this way, lots of complicated computation is saved, and the impacts that the NMOS devices have on the mixer linearity in terms of intermodulation become clear.

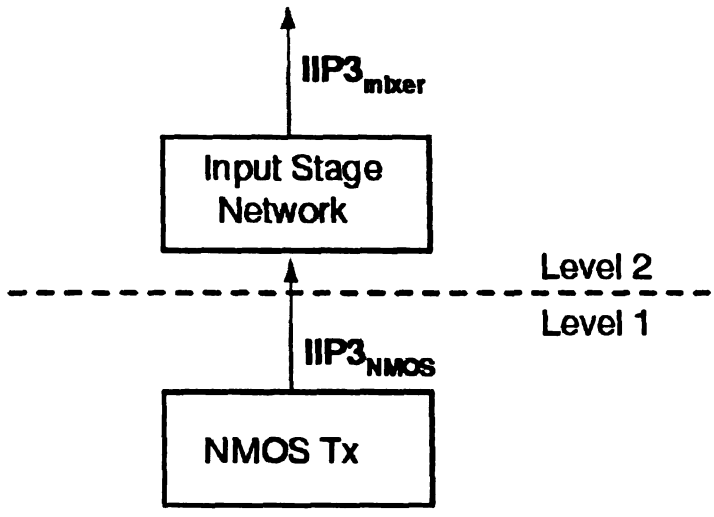


Figure 3.9: Two-Level Design Approach.

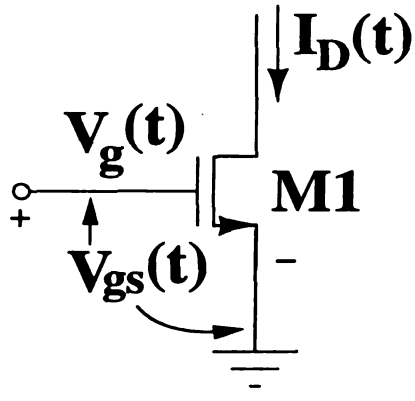


Figure 3.10: Input Stage of Gilbert Cell.

3.2.1.2 Derivation of IIP3 for NMOS device

One important source of nonlinearity the transistor exhibits is the velocity saturation effect for short-channel devices, which is given by following equation [105]

$$I_D = MV_{od}^2 \frac{1}{1 + \theta V_{od}}, \tag{3.51}$$

where V_{od} is gate overdrive voltage, θ is a positive real number used to represent the degree of velocity saturation. The value of θ ranges from zero to unit. M is given by

$$M = \frac{1}{2} C_{ox} \mu_n \frac{W}{L}. \tag{3.52}$$

Next we define

$$V_{in} = V_{gs} - V_t, \tag{3.53}$$

where V_{gs} the large-signal gate-source voltage of NMOS device in Figure 3.10, and V_t is threshold voltage of NMOS device.

To calculate IIP3, we represent the drain current I_D in power series shown below

$$I_D = K_0 + K_1 V_{in} + K_2 V_{in}^2 + K_3 V_{in}^3 + \ldots, \tag{3.54}$$

where K_n is the n-th coefficient of power series.

With equations (3.51) and (3.54) we have

$$MV_{in}^2 \frac{1}{1 + \theta V_{in}} = K_0 + K_1 V_{in} + K_2 V_{in}^2 + K_3 V_{in}^3 + \ldots. \tag{3.55}$$

In normal cases we have

$$0 < \theta V_{in} < 1, \tag{3.56}$$

such that the Taylor expansion can be applied to the left term of equation (3.55). Hence

$$M\left(V_{in}^2 - \theta V_{in}^3 + \frac{1}{2}\theta^2 V_{in}^4 + \ldots\right) = K_0 + K_1 V_{in} + K_2 V_{in}^2 + K_3 V_{in}^3 + \ldots . \quad (3.57)$$

It follows that

$$K_0 = 0, \quad (3.58)$$

$$K_1 = 0, \quad (3.59)$$

$$K_2 = M, \quad (3.60)$$

$$K_3 = -M\theta, \quad (3.61)$$

$$K_4 = \frac{1}{2}M\theta^2. \quad (3.62)$$

In the case of two-tone intermodulation, we have the following input

$$V_{in} = V_b' + v_{rf}(\cos\omega_{rf1}t + \cos\omega_{rf2}t), \quad (3.63)$$

where V_b' is the bias voltage.

Then it can be shown that magnitude of frequency component ω_{rf1} in output I_D is given by

$$A_{out,rf1} = 2K_2 V_b' v_{rf}. \quad (3.64)$$

Magnitude of frequency component $(2\cos\omega_{rf1}t - \cos\omega_{rf2}t)$ is given by

$$A_{out,IM} = \frac{3}{4}K_3 v_{rf}^3 + 3K_4 V_b' v_{rf}^3. \quad (3.65)$$

To calculate IIP3, we let

$$|A_{out,rf1}| = |A_{out,IM}|. \tag{3.66}$$

Finally we have

$$IIP3 = A_{in,IP3} = \sqrt{\frac{8}{3\theta}\frac{V_b'}{1-2\theta V_b'}}, \tag{3.67}$$

where the condition

$$0 < V_b' < \frac{1}{2\theta} \tag{3.68}$$

usually holds.

Therefore better linearity in terms of IIP3 can be achieved with higher bias voltage, which means higher power consumption. An important observation from equation (3.67) is that for the same gate overdrive, the IIP3 improves as the process scales down.

3.2.1.3 Derivation of IIP3 for mixer

After the IIP3 of NMOS device is derived, the IIP3 of mixer can be determined with a mapping circuit network. For the Gilbert mixer, the transconductance stage is the major contributor to mixer nonlinearites [96], and its mapping circuit network is shown in Figure 3.11, where Z_s is used for source degeneration to improve mixer linearity. In practice, Z_s is implemented with either an inductor or a resistor.

Ignoring the gate current of NMOS transistor, the gate voltage is given by

$$V_g = V_{od} + V_t + I_D Z_s, \tag{3.69}$$

where I_D is given by equation (3.51).

Taking the second order approximation, V_g could be rewritten as

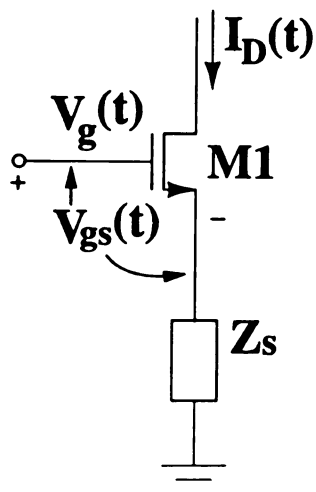


Figure 3.11: Source Degenerated Input Stage of Gilbert Mixer.

$$V_g = V_{od} + V_t + MZ_s(V_{od}^2 - \theta V_{od}^3). \tag{3.70}$$

Generally it is difficult to express I_D in terms of V_g in a understandable way. Here we use a novel approach to attack this problem.

The circuit of mixer input stage in Figure 3.11 is represented with the closed-loop model shown in Figure 3.12. Part of the output current I_D is fed back to input V_g with a feedback gain of F, then the difference between V_g and the feedback signal V_D' is processed by a nonlinear function A(v), whose output is further filtered to remove all frequency components except ω_{rf}.

The input voltage is given by

$$V_g(t) = V_{g0} + v_g \cos\omega_{rf} t. \tag{3.71}$$

The output current is given by

$$I_D(t) = I_{D0} + i_d \cos\omega_{rf} t. \tag{3.72}$$

Since F(v) is a linear function of Z_s,

$$F(v) = F \equiv constant. \tag{3.73}$$

The feedback output is given by

$$V_D(t) = FI_D = I_{D0}R + i_d R\cos\omega_{rf} t. \tag{3.74}$$

It follows that the transient gate-to-source voltage of NMOS transistor is given by

$$V_{od}(t) = (V_{gs0} - I_{D0}R) + (v_g - i_d R)\cos\omega_{rf} t. \tag{3.75}$$

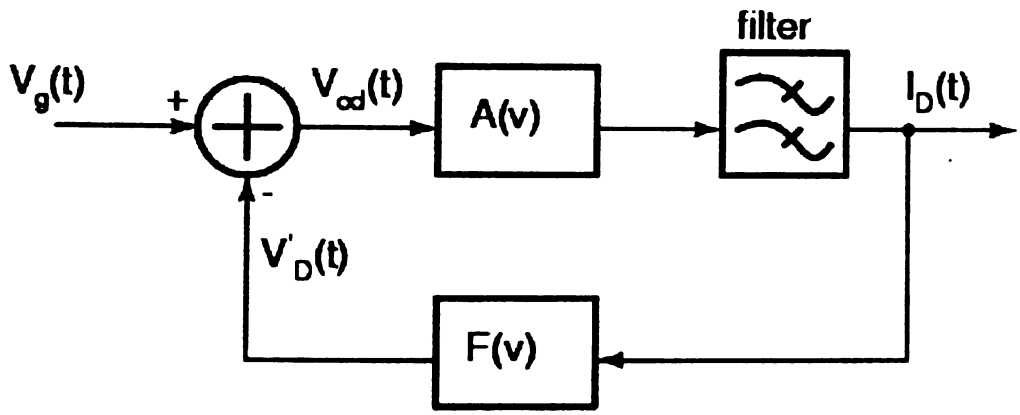


Figure 3.12: Nonlinearity Model of NMOS Transistor with Source Degeneration.

Note that in this model the nonlinearity of transconductance stage of mixer is introduced by the nonlinearity of $A(v)$.

Finally $IIP3_{mixer}$, the estimated input-referred third-order interception point of mixer, is given by

$$IIP3_{mixer} = IIP3_{NMOS}[1 + A(IIP3_{NMOS})F], \tag{3.76}$$

where $IIP3_{NMOS}$ is the input-referred third-order interception point of NMOS device.

Therefore the use of source degeneration in a mixer actually provides a negative feedback loop that improves the IIP3 of mixer. Nonetheless, the IIP3 of NMOS transistor in transconductance stage fundamentally determines the mixer IIP3. Equation (3.76), together with equation (3.67), provides an effective way to estimate mixer linearity in terms of IIP3 from power budget.

3.2.2 Topology Improvement of Mixer for High Linearity

Though the use of source degeneration technique improves mixer IIP3, it degrades the mixer performance in terms of gain compression. This point has never been mentioned in the literature, and will be discussed below.

Denote the input-referred gain compression point of NMOS device by $IGCP_{NMOS}$, and assume $A'(v)$ to be the *ideal* gain function of NMOS device without any nonlinearities. Then according to the definition of gain compression point, the following relation holds:

$$A(IGCP_{NMOS}) \approx 0.891 A'(IGCP_{NMOS}). \tag{3.77}$$

Meanwhile the transconductance of mixer is given by

$$g_{m,\,mixer} = \frac{A(v)}{1 + A(v)Z_s} = \frac{1}{\frac{1}{A(v)} + Z_s}. \tag{3.78}$$

Therefore $IGCP_{mixer}$, the input-referred gain compression point of mixer, satisfies the following equation

$$\frac{1}{\frac{1}{A(IGCP_{mixer})} + Z_s} \approx 0.891 \frac{1}{\frac{1}{A'(IGCP_{mixer})} + Z_s}. \tag{3.79}$$

It follows that

$$0.122Z_s + \frac{1}{0.891A'(IGCP_{mixer})} \approx \frac{1}{A(IGCP_{mixer})}. \tag{3.80}$$

Compare equation (3.80) with equation (3.77), it is clear that

$$IGCP_{mixer} < IGCP_{NMOS}. \tag{3.81}$$

Therefore with the use of source degeneration the mixer linearity improves in terms of intermodulation, yet suffers in terms of gain compression.

To alleviate the degradation of mixer gain compression point caused by source degeneration, we propose a modified topology of Gilbert mixer. The idea is illustrated in Figure 3.13, where an active resistor is used in place of Z_s. The long-channel NMOS device M2 gives active resistance

$$R(v) = \frac{1}{2MV_{od}}. \tag{3.82}$$

where M is a constant. Meanwhile the gain function in Figure 3.12 could be written to the first order approximation as

$$A(v) = KV_{od}, \tag{3.83}$$

where K is a constant determined by transistor bias point.

Therefore we can further write

$$A(v)R(v) = C, \tag{3.84}$$

where C is a constant. Consequently, transconductance of the modified mixer is

$$g'_{m,\,mixer} = \frac{A(v)}{1 + A(v)Z_s} = \frac{A(v)}{1 + C}. \tag{3.85}$$

It is seen from above equation that the new mixer topology does not have the trouble of degradation in gain compression, meanwhile maintains the advantage of high IIP3. Finally the complete topology of improved Gilbert mixer is shown in Figure 3.14.

3.3 Complex Analog Filter

One key issue in RF receiver design is image-rejecting [3]. Given RF input $x(t)$ consisting of input signal at frequency ω_{rf} and its image at frequency ω_{im}, we want to downconvert the signal from ω_{rf} to ω_{if} without introducing the image at ω_{im}, where

$$x(t) = v_{rf}\cos\omega_{rf}t + v_{im}\cos\omega_{im}t, \tag{3.86}$$

$$\omega_{if} = \omega_{lo} - \omega_{rf} = \omega_{im} - \omega_{lo}. \tag{3.87}$$

The conventional approach to rejecting the image is to filter $x(t)$ before downconversion to remove the image at frequency ω_{im}. Such approach, however, is not appropriate for front-end using low-IF architecture, where the image is rejected after downconversion.

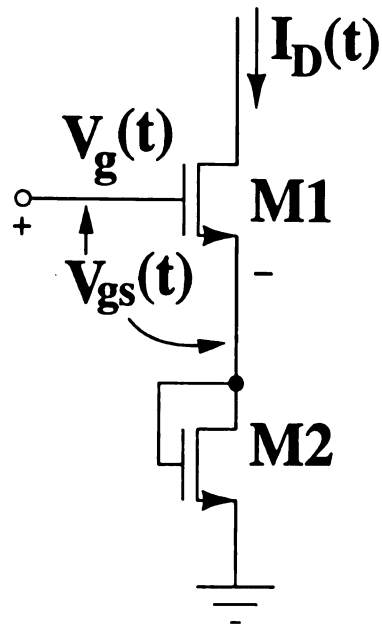


Figure 3.13: Transconductance Stage of Gilbert Cell with Active Degeneration.

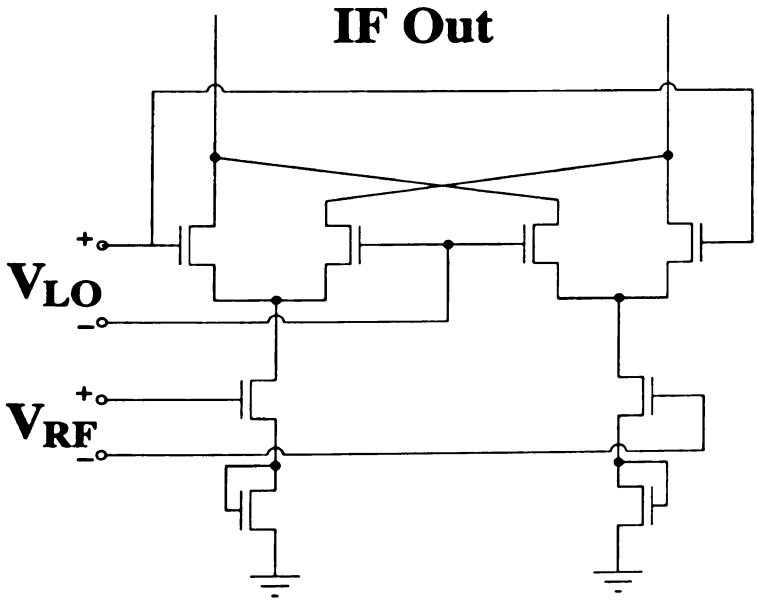


Figure 3.14: Modified Gilbert Cell.

Consider the output of mixer when no function of image-rejecting is performed before downconversion:

$$x'(t) = x(t)v_{lo}\cos\omega_{lo}t = \frac{v_{rf}v_{lo}}{2}\cos\omega_{if}t + \frac{v_{im}v_{lo}}{2}\cos\omega_{if}t + \ldots. \tag{3.88}$$

For simplicity without losing generality, we omit the frequency components other than ω_{rf} resulting from frequency manipulation of mixer and complex filter throughout the discussion in the rest of this chapter. From equation (3.88) it is clear that after downconversion the signal spectrum overlaps that of the image. Consequently, the image can not be attenuated with BPF filter in real domain.

To distinguish the image from the signal after downconversion, consider the mixer output with LO signal of $v_{lo}\sin\omega_{lo}t$:

$$x''(t) = x(t)v_{lo}\sin\omega_{lo}t = \frac{v_{rf}v_{lo}}{2}\sin\omega_{if}t - \frac{v_{im}v_{lo}}{2}\sin\omega_{if}t + \ldots. \tag{3.89}$$

where the phase of IF signal is different from that of the image by the degree of 180.

As a result, if we mix $x(t)$ with a pair of quadrature LO signals as shown in Figure 3.15, the resultant output can be written in complex form

$$\begin{aligned} y(t) &= y_I(t) + jy_Q(t) = x(t)v_{lo}\exp(j\omega_{lo}t) \\ &= \frac{v_{rf}v_{lo}}{2}\exp(j\omega_{if}t) + \frac{v_{im}v_{lo}}{2}\exp(-j\omega_{if}t) + \ldots \end{aligned} \tag{3.90}$$

It follows that the image contributes the frequency component of $-\omega_{if}$ in the output, whereas the signal contributes the frequency component of ω_{if} as shown in Figure 3.16. Therefore, a complex analog filter is needed to reject the image in the complex domain after downconversion.

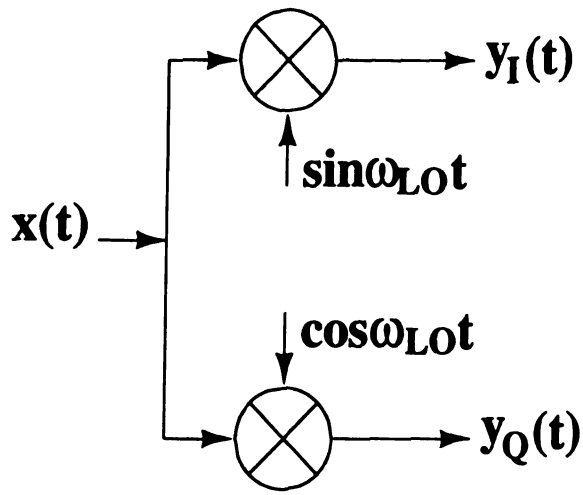


Figure 3.15: Downconversion with Quadrature LO Signals.

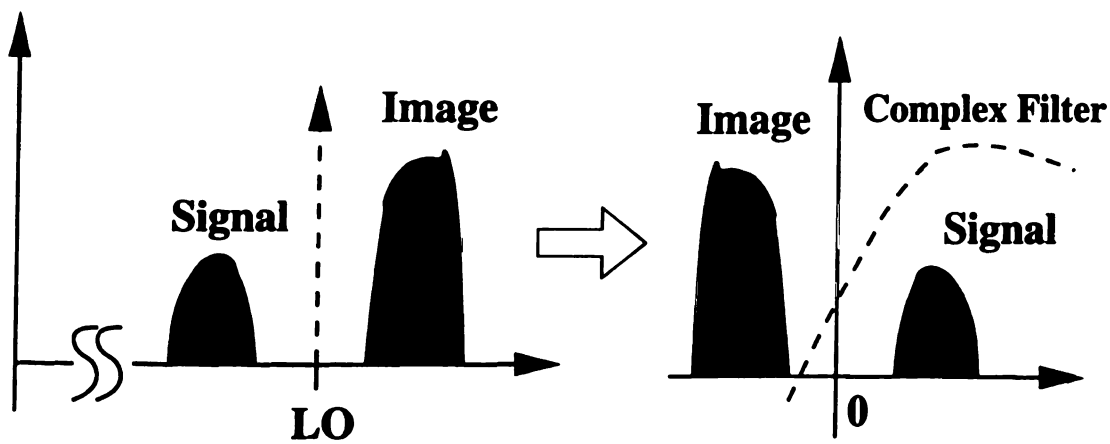


Figure 3.16: Spectrum Translation in Complex Filtering.

As mentioned in Chapter 2, the complex analog filter (CAF) needed for image rejection in low-IF front-end is conventionally implemented with frequency-translation approach. Our work in this thesis explores the way of image rejection using asymmetric polyphase network, which has the potential of achieving less power consumption than the frequency-translation approach. In following discussion we first analyze image-rejecting operation of complex analog filter based on passive-RC implementation of asymmetric polyphase network, then give an active OTA-C implementation of the filter.

3.3.1 Analysis of Image Rejection with Asymmetric Polyphase Network

3.3.1.1 Asymmetric polyphase network

A polyphase signal is a set of two or more vectors having the same frequency but different in phase [17]. A polyphase signal is said to be symmetric if its vectors have the same magnitude and are equally spaced in space. A positive polyphase signal has a clock-wise phase order, while a negative sequence has an anti-clockwise phase order. The follow-ing sequence is a example of positive and symmetric polyphase signal

$$\{\exp(j\omega t), j\exp(j\omega t), -\exp(j\omega t), -j\exp(j\omega t)\}.$$

A N-phase polyphase network has N input ports and N output ports. One phase of a generalized N-phase network is shown in Figure 3.17.

The open-load voltage gain referred to the k-th port of N-phase network is given by

$$H_k(s) = \frac{V_{k,out}}{V_{k,in}} = \frac{Y_1 + \exp(j\theta)Y_2}{Y_1 + Y_2}. \qquad (3.91)$$

A 4-phase passive-RC polyphase network is shown in Figure 3.18, where

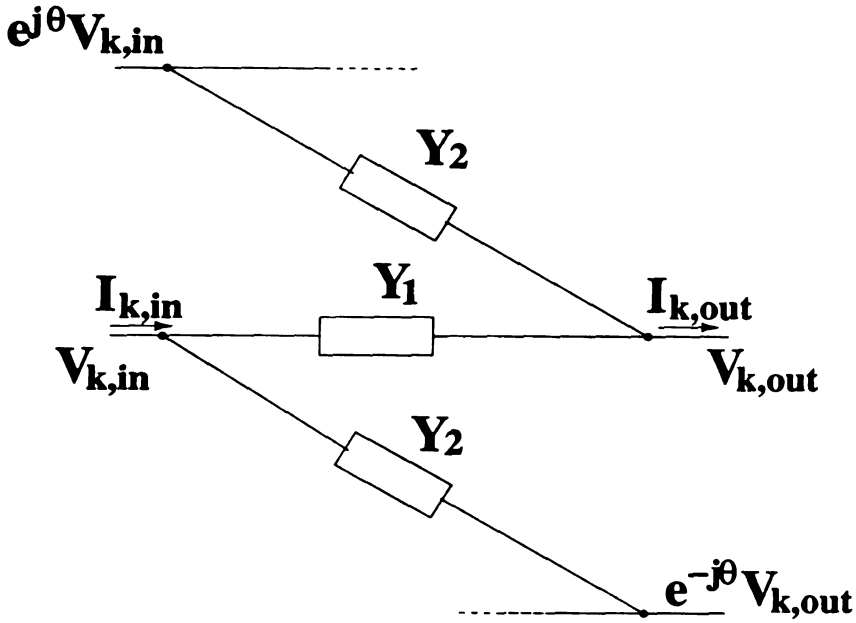


Figure 3.17: One Phase of a Generalized N-Phase Network [94].

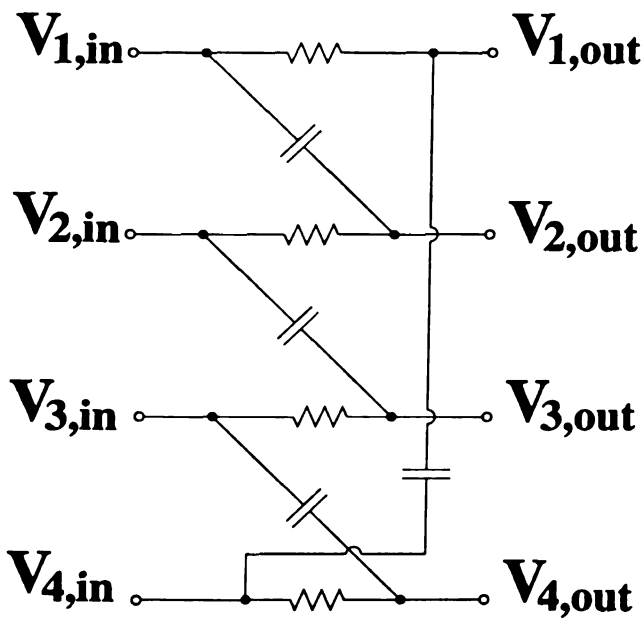


Figure 3.18: 4-Phase Passive RC Network.

$$Y_1 = \frac{1}{R}, \tag{3.92}$$

$$Y_2 = sC. \tag{3.93}$$

Therefore the open-load voltage gain referred to the k-th port of network is given by

$$H_k(s) = \frac{V_{k,out}}{V_{k,in}} = \frac{1 + \exp(j\theta)s\tau}{1 + s\tau}, \tag{3.94}$$

where

$$\tau = RC. \tag{3.95}$$

To show how the polyphase network could be used as complex analog filter, we have the following result according to equation (3.94):

$$\left|\frac{H_k(j\omega)}{H_k(-j\omega)}\right|^2 = \frac{(1 - \sin\theta\omega\tau)^2 + (\cos\theta\omega\tau)^2}{(1 + \sin\theta\omega\tau)^2 + (\cos\theta\omega\tau)^2}. \tag{3.96}$$

It follows that negative frequency components are attenuated for $\theta < 0$, whereas positive frequency components are attenuated for $\theta > 0$.

3.3.1.2 Operation of complex analog filter based on polyphase network

To show how the 4-phase polyphase network could be used to perform image-rejecting in the complex domain, consider the circuit configuration in Figure 3.19, where

$$y_I(t) = \frac{v_{rf}v_{lo}}{2}[\exp(j\omega_{if}t) + \exp(-j\omega_{if}t)] + \frac{v_{im}v_{lo}}{2}[\exp(j\omega_{if}t) + \exp(-j\omega_{if}t)], \tag{3.97}$$

$$y_I(t) = \frac{v_{rf}v_{lo}}{2}[-j\exp(j\omega_{if}t) + j\exp(-j\omega_{if}t)] + \frac{v_{im}v_{lo}}{2}[j\exp(j\omega_{if}t) - j\exp(-j\omega_{if}t)]. \tag{3.98}$$

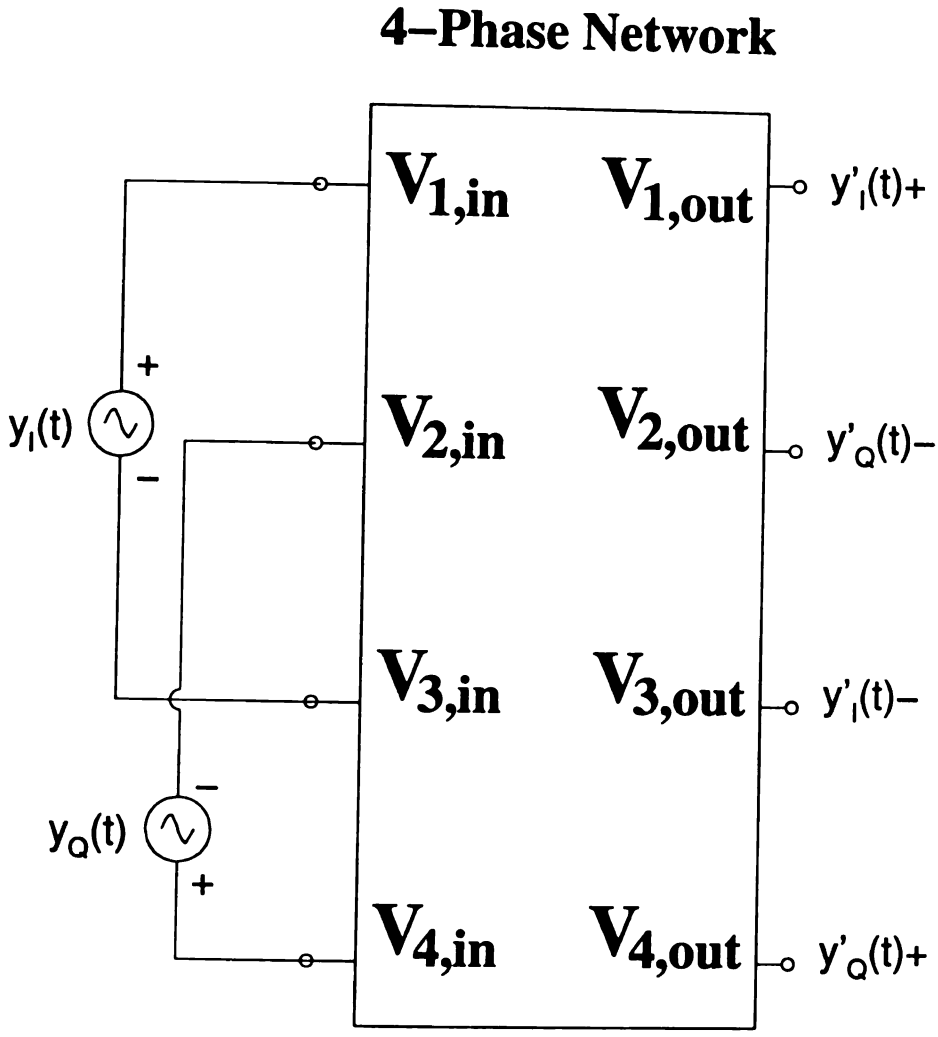


Figure 3.19: Circuit Configuration for Image Rejecting with 4-Phase RC Polyphase Network.

The input of 4-phase network in Figure 3.19 can be represented as the sum of following symmetric polyphase signals

$$S_{rf,1} = \frac{v_{rf}v_{lo}}{4}\exp(j\omega_{if}t)\{1, j, -1, -j\}, \tag{3.99}$$

$$S_{rf,2} = \frac{v_{rf}v_{lo}}{4}\exp(-j\omega_{if}t)\{1, -j, -1, -j\}, \tag{3.100}$$

$$S_{im,1} = \frac{v_{im}v_{lo}}{4}\exp(j\omega_{if}t)\{1, -j, -1, j\}, \tag{3.101}$$

$$S_{im,2} = \frac{v_{im}v_{lo}}{4}\exp(-j\omega_{if}t)\{1, j, -1, -j\}. \tag{3.102}$$

Note that $S_{rf,1}$ and $S_{rf,2}$ are sequences of the signal, while $S_{im,1}$ and $S_{im,2}$ are sequences of the image. For image rejecting, we want to attenuate sequences of the image while keeping sequences of the signal.

For $S_{rf,1}$ we have

$$\theta = -\frac{\pi}{2}, \tag{3.103}$$

$$H_{rf,1}(\omega) = \frac{1+\omega\tau}{1+j\omega\tau}. \tag{3.104}$$

For $S_{rf,2}$ we have

$$\theta = \frac{\pi}{2}, \tag{3.105}$$

$$H_{rf,2}(\omega) = \frac{1+\omega\tau}{1-j\omega\tau}. \tag{3.106}$$

For $S_{im,1}$ we have

$$\theta = \frac{\pi}{2}, \tag{3.107}$$

$$H_{im,1}(\omega) = \frac{1-\omega\tau}{1+j\omega\tau}. \tag{3.108}$$

For $S_{im,2}$ we have

$$\theta = -\frac{\pi}{2}, \tag{3.109}$$

$$H_{im,2}(\omega) = \frac{1-\omega\tau}{1-j\omega\tau}. \tag{3.110}$$

Consequently at frequency $\omega_0 = \frac{1}{\tau}$, the image component is completely removed from output signal in Figure 3.19.

Finally the output signals in Figure 3.19, which are quadrature signals with the image removed, are given by

$$y'_I(t) = V_{1,out} - V_{3,out}, \tag{3.111}$$

$$y'_Q(t) = V_{4,out} - V_{2,out}. \tag{3.112}$$

3.3.2 Active Implementation of CAF

The major obstacle to integration of passive-RC polyphase filter is the passive resistors used. Therefore we propose a novel way to implement the active complex analog filter by replacing passive resistor with active resistor constructed from operational transconductor amplifier (OTA). Circuit topology of the active resistor is shown in Figure 3.20 [5], where the resistance is given by

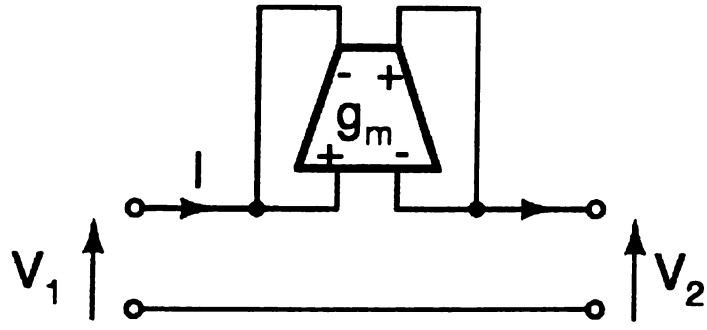


Figure 3.20: Active Resistor with Transconductor [6].

$$R = \frac{1}{g_m}, \tag{3.113}$$

and g_m is the transconductance of OTA. Time constant (τ) of such active filters can be adjusted by changing bias condition of OTAs after chip fabrication.

Compared with the frequency-translation implementation of CAF using OTAs and capacitors, our proposed implementation has the advantage of low power consumption, because no gyrators are needed. The disadvantage is weak out-band rejection, of which impacts on filter performance could be alleviated by cascading several polyphase networks and using high-performance OTA, such as the Nauta's transconductor [81].

4 SIMULATION RESULTS

To demonstrate the effectiveness of the proposed design techniques in Chapter 3, an integrated CMOS front-end was designed for 2.4-GHz Bluetooth applications. The front-end was laid out in TSMC 0.18-μm CMOS technology with Cadence Virtuoso layout editor. The parasitic parameters were extracted from the front-end layout for post-layout simulation with Cadence SpectreRF tools.

This chapter describes the design process of the front-end, discusses some practical issues involved, and compares the post-simulation results with those of a recently-reported Bluetooth receiver IC in similar 0.18-μm CMOS technology. The comparison shows that our front-end implementation achieves less power consumption and better linearity, yet worse image-rejection performance.

4.1 Design Specification for Bluetooth Front-End

A Bluetooth receiver operates in the RF band from 2.400 GHz to 2.4835 GHz. The channel bandwidth is 2 MHz. The required sensitivity is -70 dBm for 0.1% bit-error-rate (BER), which translates to a NF of 26dB and IIP3 of -17.5 dBm. Image-rejection-ratio is required to be at least 33 dB, and conversion gain 18dB to 22dB [65][114]. The power consumption should be as small as possible. The input of front-end is required to be matched to 50 Ω with S_{11} no higher than -11 dB.

4.2 Circuit Design

The low-IF architecture in Figure 3.1 is used for the front-end that consists of LNA, mixer, and complex analog filter. The LNA employs the cascode topology with inductive source degeneration in Figure 3.3. The mixer employs the modified Gilbert cell topology proposed in Figure 3.14. The complex analog filter for image rejection consists of two 4-phase lattice-based filters in Figure 3.18 connected in series.

4.2.1 LNA

The first step in designing LNA is to specify the key performance parameters. A 4.5-dB noise figure is stipulated for LNA to make sure the front-end noise figure is no less than 26 dB as required by Bluetooth specification. The gain is expected to be no less than 15 dB. And IIP3 should be higher than -17.5 dBm.

The second step is to apply the proposed noise-constrained design techniqes to designing LNA of circuit configuration in Figure 4.1. The curves shown in Figure 4.2 and Figure 4.3 resulting from our work in Chapter 3 are helpful to simplify the design task. From Figure 4.2, the chosen value for the on-chip inductor quality factor is 3.0, for which a noise figure less than 2.7 dB can be achieved at 2.44 GHz with 2-mW power consumption. To further save power and boost performace, the input matching degree of LNA is degraded to 0.9 according to Figure 4.3. To find out if the proposed method provides enough design accuracy, theory prediction and simulation results for Q of 3.0 are plotted in Figure 4.4 and Figure 4.5. It is seen from Figure 4.4 that for power consumption between 4 mW and 12 mW, the predicted noise figure differs from simulated data by less than 0.5 dB, which is accurate enough for hand-design purpose. Power consumption less than 4 mW

is rarely found in practice for LNA in standard CMOS technology [1]. It is seen from Figure 4.5 that our method characterizes the tradeoff between noise figure and degree of input matching very well. Therefore the proposed design method gives theory prediction that agree well with simulation results for power ranging from 4 mW to 12 mW.

The third step is to determine the bias and sizes of transistors as well as values of inductances in the LNA. The smallest channel length (0.20 μm) allowed by the technology is used for all transistors in the LNA. The width of transistor M1 is carefully chosen to make sure that the transistor works in weak saturation region. Particularly, the width of transistor M2 is the same as the width of transistor M1 as a rule of thumb [105]. The gate overdrive is determined with the help of the curve in Figure 4.6.

The final step is to calculate values of the inductances used in LNA with equations (3.24), (3.32), and (3.33). The values of the inductances used in practice are smaller than those calculated because of the increased gate-source capacitance of NMOS device caused by short-channel effects.

4.2.2 Mixer

First, the key performance parameters of mixer are specified. An IIP3 of -8 dBm is stipulated for the mixer to make sure the front-end has good linearity. A conversion gain no less than 3 dB is preferred. Noise figure should not exceed 15 dB.

Second, the modified topology for the Gilbert cell proposed in Chapter 3 is validated by simulating the circuits shown in Figure 4.7 and Figure 4.8. The mixer in Figure 4.7 employs the classic topology without source degeneration, whereas the mixer in Figure 4.8 is modified using active source degeneration as proposed in Figure 3.13. A third mixer

with 100-Ω resistive source degeneration is also simulated. The three ports of mixer (LO, RF, and IF) are carefully matched to 50 Ω with input/output matching network as illustrated in Figure 4.7 and Figure 4.8. The power of LO signal is 0 dBm. IIP3 points for three versions of mixer are simulated for input power ranging from -25 dBm to 10 dBm with SpectreRF PSS and PAC analysis modes. The simulated data is plotted in Figure 4.9. It is seen from the simulation results that resistive degeneration improves the mixer IIP3 for low power consumption (less than 1.5 mW in our case). However, for higher power consumption, the linearity performance of mixer with resistive degeneration is no better than that without any degeneration. The reason is that the voltage drop on the degenerating resistor increases linearly as the drain current increases. Consequently the gate overdrive of transconductance transistor tends to be reduced. Meanwhile the mixer with our proposed technique has the best performance in terms of IIP3 among the three versions.

The disadvantage of our proposed technique can also be observed in Figure 4.9. For extremely low power consumption, the performance of active degeneration technique is worse than that of resistive degeneration, because a minimum voltage drop is required for the degenerating transistor to work in active region.

Finally, a power consumption of 2 mW is chosen for the proposed mixer, which results in a IIP3 of around -2 dBm as shown in Figure 4.10. Due to the difficulty for analyzing the mixer behavior in aspects such as noise figure and conversion gain, intensive simulation work is used to determine the bias and sizes of transistors in the mixer.

4.2.3 Complex Analog Filter

Circuit configuration for the complex analog filter is shown in Figure 4.11. The transconductor cell is implemented with Nauta's scheme in Figure 2.8. The phase difference between two input signals to the polyphase network is 90 degree to model the quadrature output signals from downconversion mixers in Figure 3.15. The attentuation on both the signal and the image is measured with transcient analysis.

For Bluetooth applications, the filter shall have a center frequency of 2 MHz and a bandwidth of 2 MHz [65]. In the design we use the filter prototype in Figure 3.18. The values of resistor and capacitor have to be carefully selected. A small resistor may overload the preceding mixer stage and increase the power of transconductance cell, meanwhile a large resistor makes transconductance cell sensitive to the process variation. In our case of polyphase network filter, all resistors have the value of 80 kΩ and all capacitors 1 pF. For a resistance of 80 kΩ, the required transconductance of the transconductor cell is 12.5 μS according to equation (3.20). Such transconductance approximately translates to a drain current of 50 μA for the technology in use.

Frequency responses of the designed filter for the signal and the image are shown in Figure 4.12 (a) and in Figure 4.12 (b), respectively. The 3-dB bandwidth for the signal is 2.5 MHz, and the gain is higher than 1 dB over the passband centered at 2 MHz. Note that the simulated 3-dB bandwidth (2.5 MHz) is slightly larger than that required by the Bluetooth specification (2 MHz). This is to compensate the bandwidth loss caused by the cascading of several polyphase networks for higher degree of image rejection. For the image 13-dB attenuation is achieved over the 3-dB passband of the signal, which translates to the image-rejection ratio (IRR) of 14 dB. Since the minimum requirement of IRR for

Bluetooth applications is 33 dB [65], a cascaded network of at least three 4-phase polyphase filters is needed to provide sufficient image rejection. However, in the thesis project only two filters are used due to the concern of design complexity.

4.2.4 Impedance Matching between Building Blocks in Front-End

One important issue in practical front-end design is the impedance matching between front-end building blocks, particularly the matching between LNA and mixer. Conventionally the degree of input impedance matching is described by S_{11} parameter, and the degree of output impedance matching by S_{22} parameter. Assuming the characteristic impedance is 50 Ω, the simulated S_{22} values for LNA are plotted in Figure 4.13 for frequencies from 2.4 GHz to 2.5 GHz, and the simulated S_{11} values for mixer are plotted in Figure 4.14 for the same frequency range. From the figures it is clear that both LNA output and mixer input exhibit capacitive characteristics. To achieve perfect impedance matching between LNA and mixer, the LC network shown in Figure 4.15 is employed, for which a 0.39-pF capacitor and 1.3 nH inductor are used. Fortunately, the values of capacitor and inductor are small enough for on-chip integration. With the impedance matching network nearly perfect impedance matching is achieved as shown in Figure 4.16.

4.3 Post-Layout Simulation Results

The proposed integrated RF front end is laid out using Cadence Virtuoso in TSMC 0.18-μm digital CMOS technology as shown in Figure 4.17. The post-layout simulation results are summarized in Table 4.1.

Several observations are made when comparing the simulated performance of the front-end with the measured performance of a similar chip reported recently [114]. First, the power consumption of our implementation is 20% less than that reported in the literature. This shows that our design techniques for low power are effective. Second, the linearity of our implementation is much better than that reported in the literature. This is because our implementation uses the proposed mixer topology as well as impedance matching network between receiver building blocks. Third, our implementation has worse image-rejecting peformance than that reported in the literature. To solve this problem in the future, three-stage cascaded filter should be used.

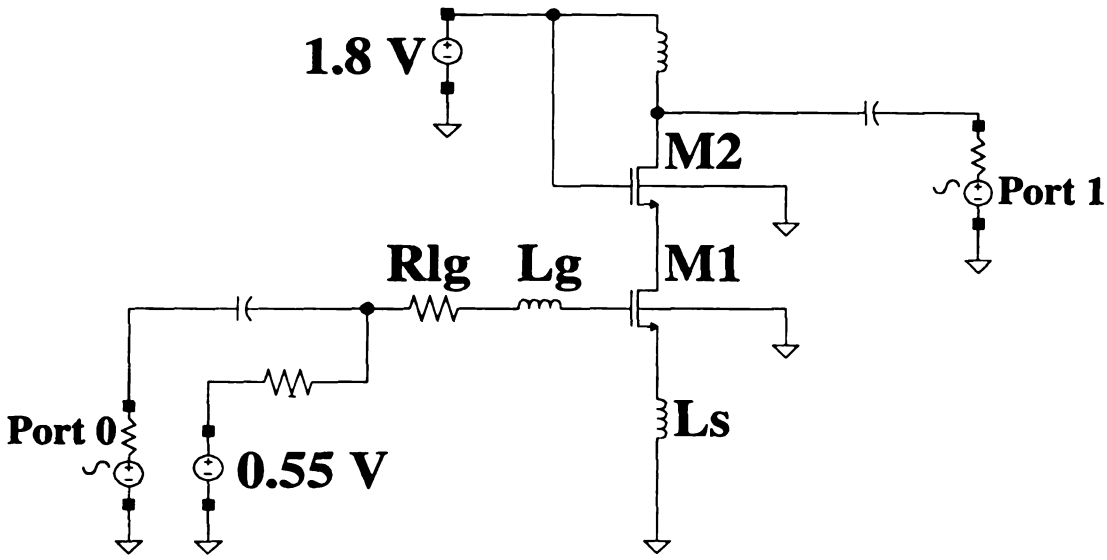


Figure 4.1: Circuit Configuration for LNA Simulation.

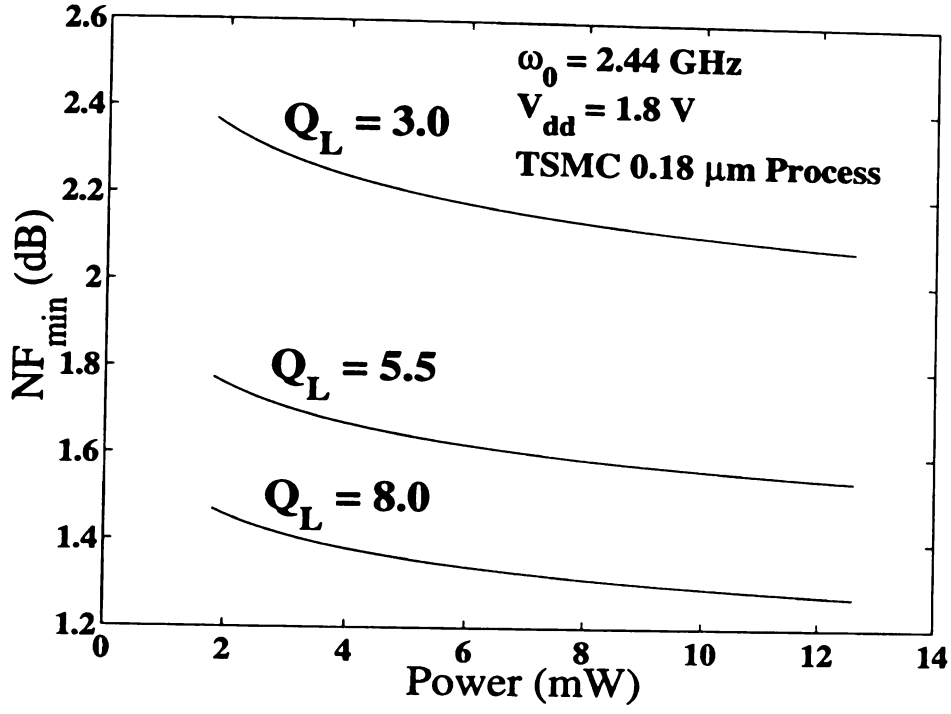


Figure 4.2: Minimum Noise Factor versus Power for Different Q-Value.

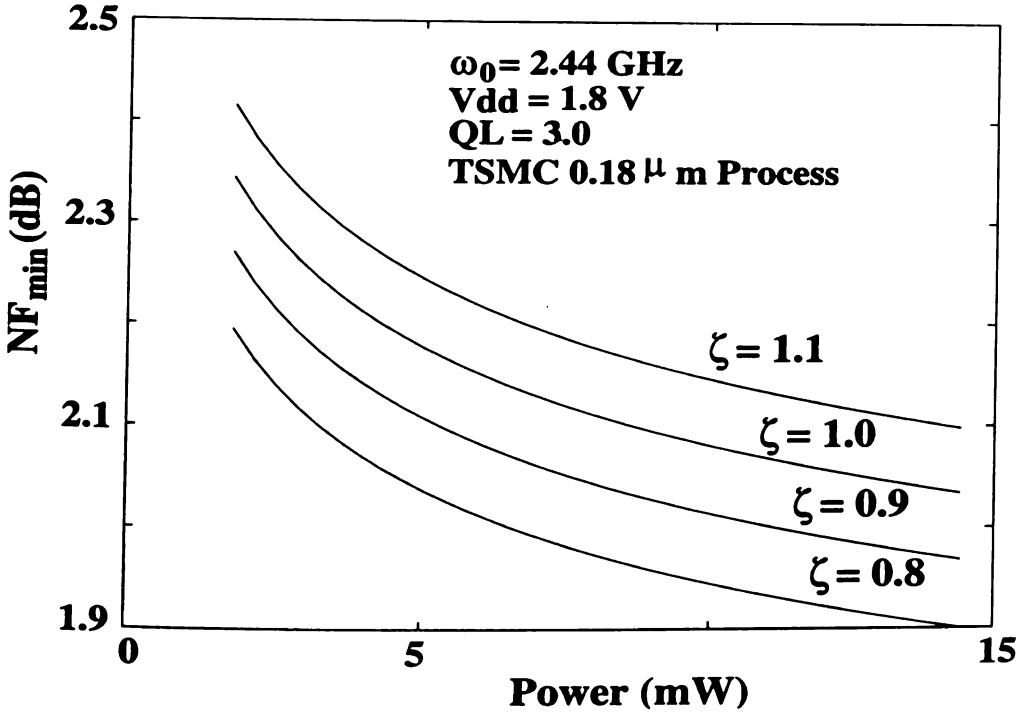


Figure 4.3: Minimum Noise Factor versus Power for Different Degree of Input Matching.

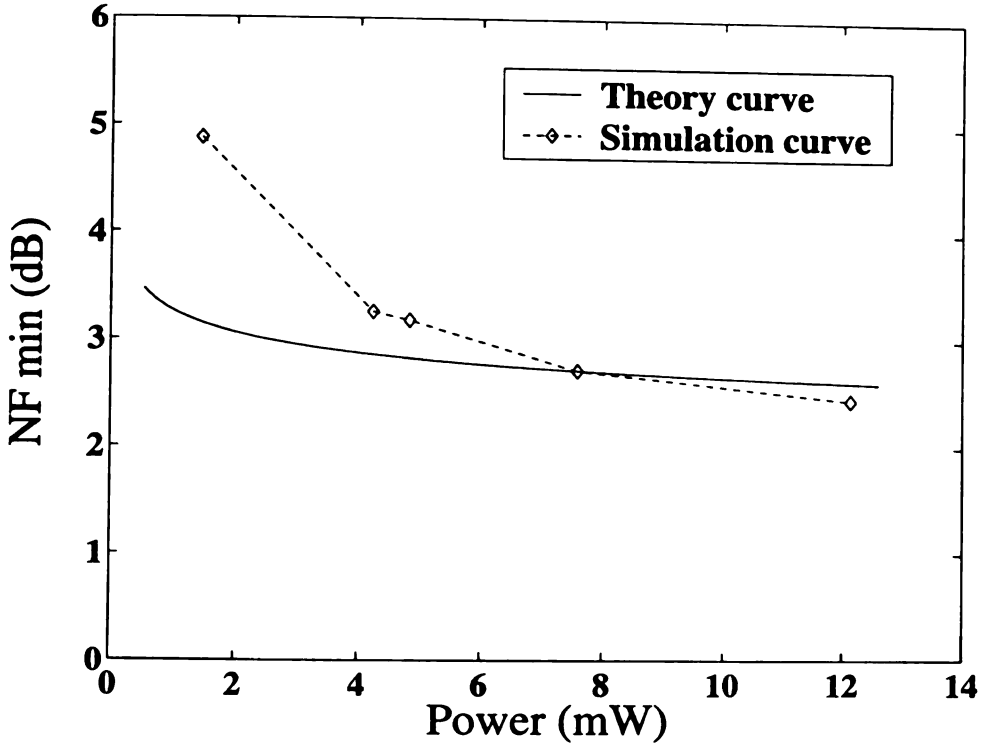


Figure 4.4: Minimum Noise Figure versus Power with Perfect Input Matching.

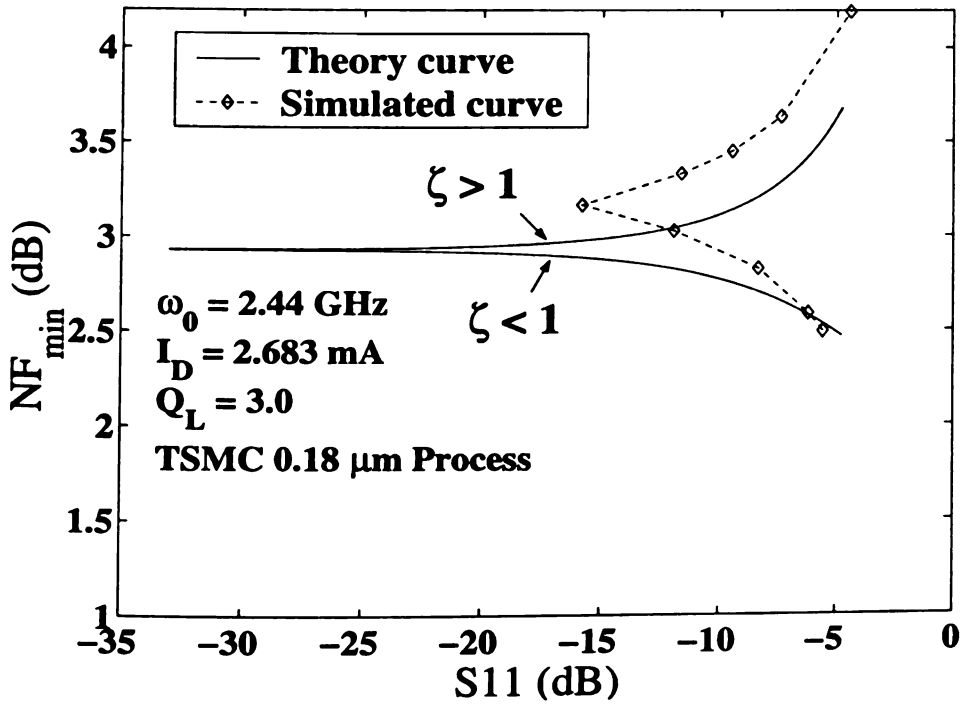


Figure 4.5: Minimum Noise Factor versus Power with Imperfect Input Matching.

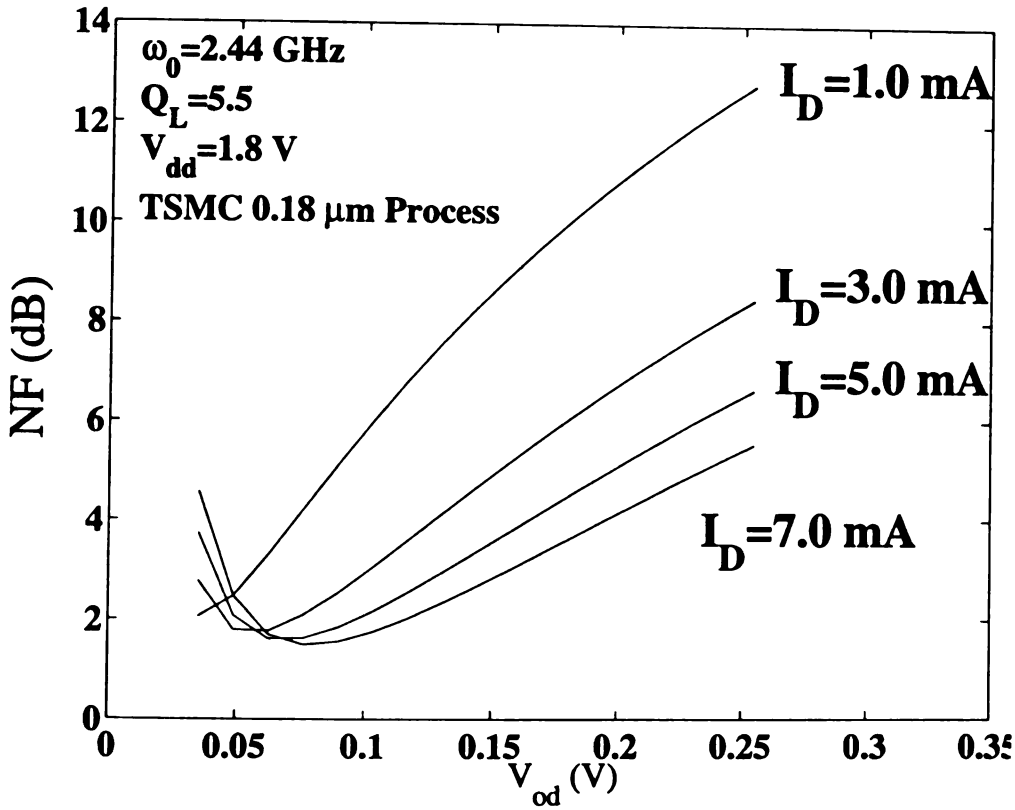


Figure 4.6: Noise Factor versus Gate Overdrive for Q=3.0.

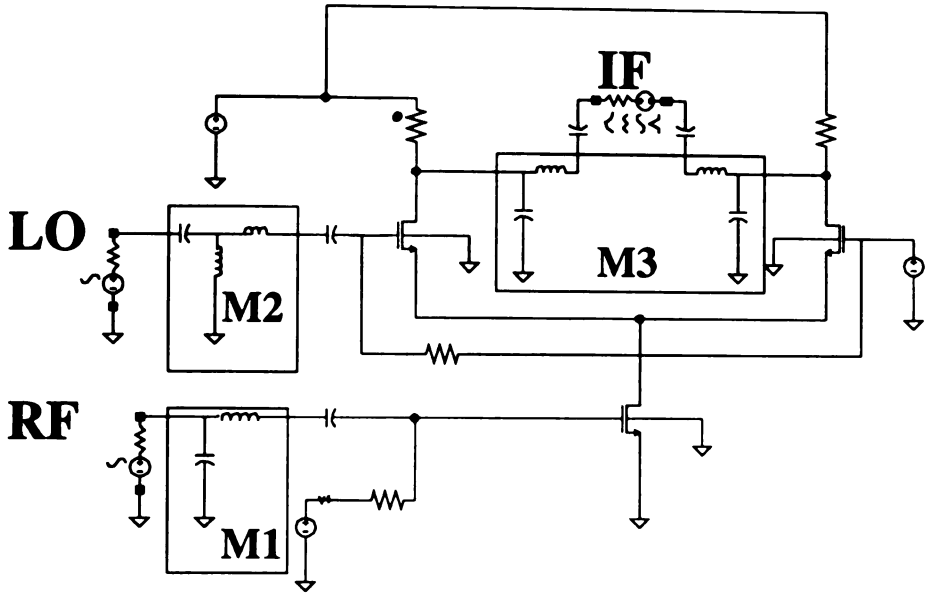


Figure 4.7: Circuit Configuration of Mixer without Degeneration.

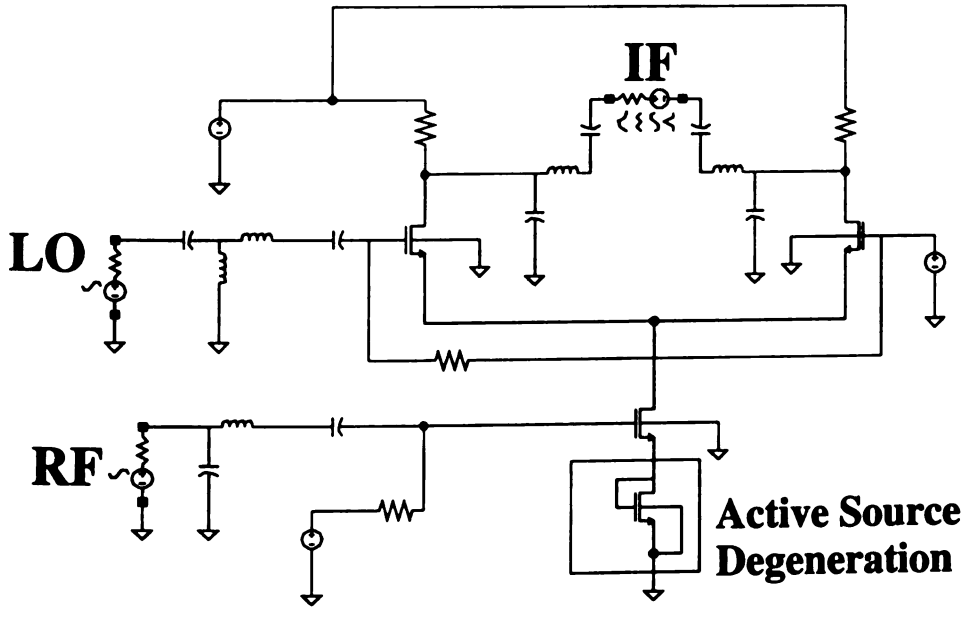


Figure 4.8: Circuit Configuration of Mixer with Active Degeneration.

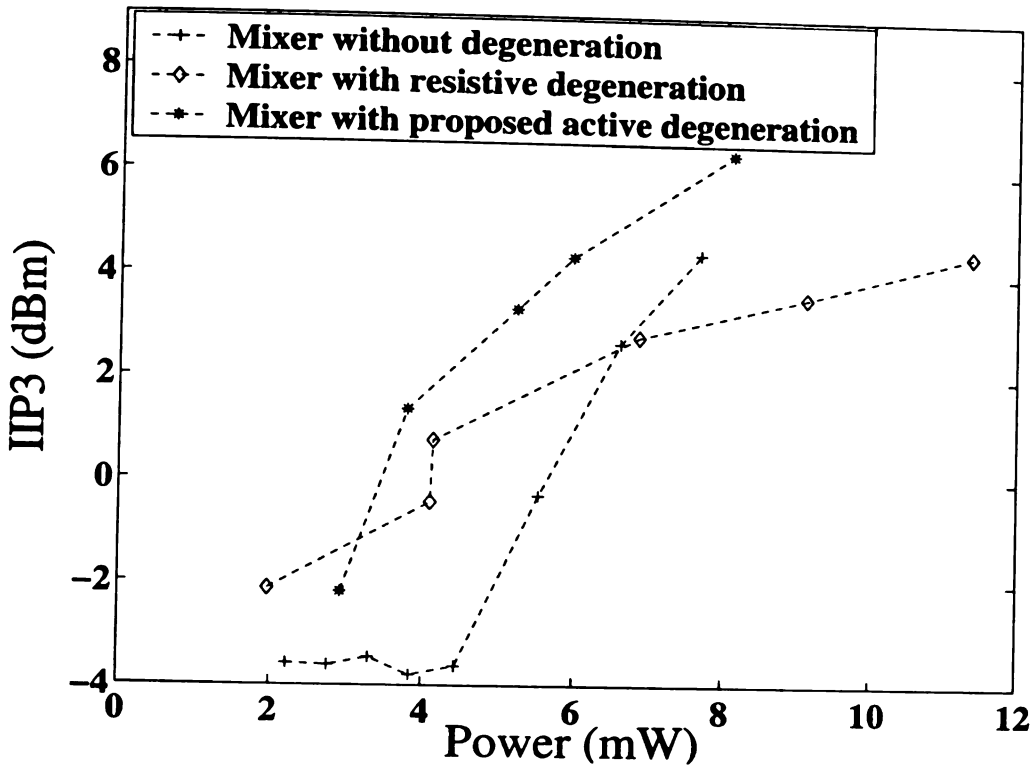


Figure 4.9: Simulated IIP3 Performance for Three Mixer Versions.

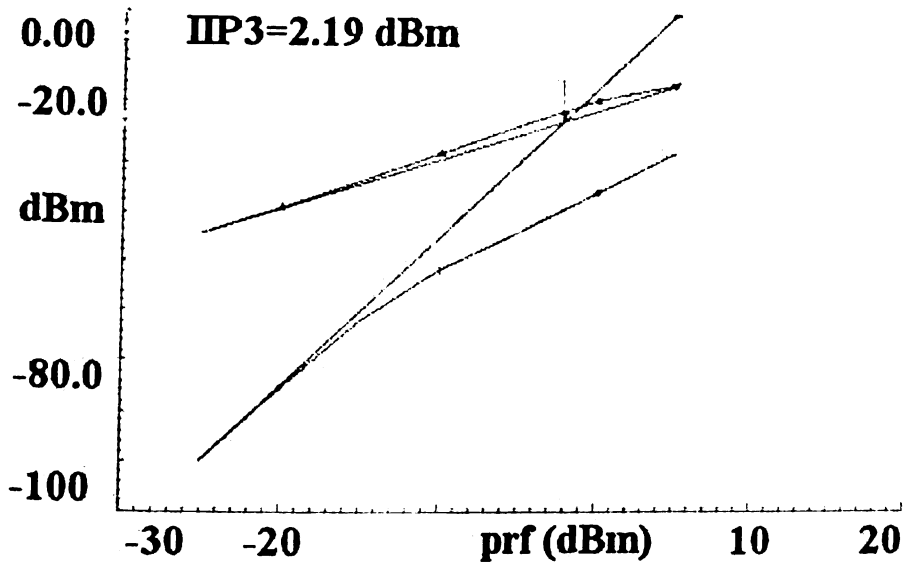


Figure 4.10: Simulated IIP3 Curve for 2mW Mixer with Active Degeneration .

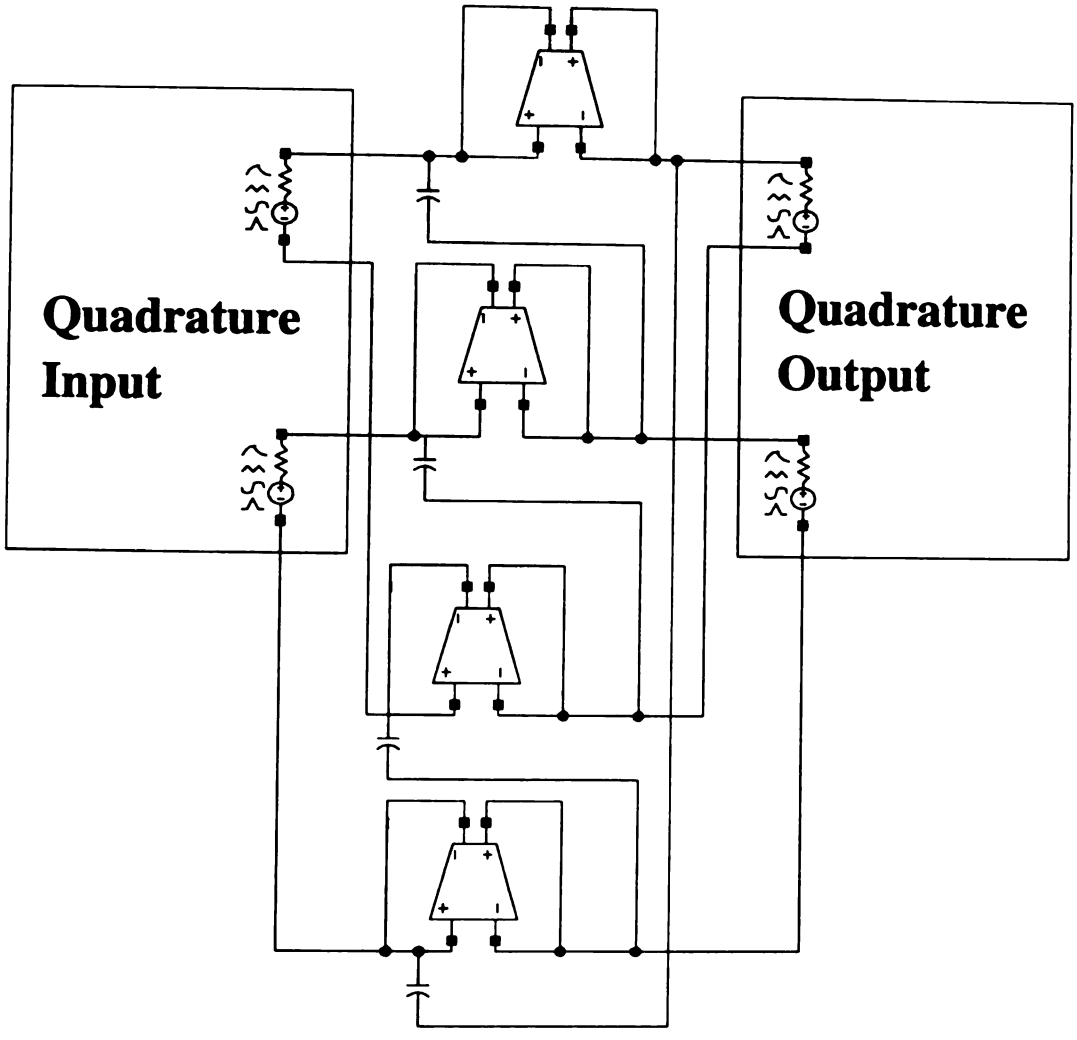
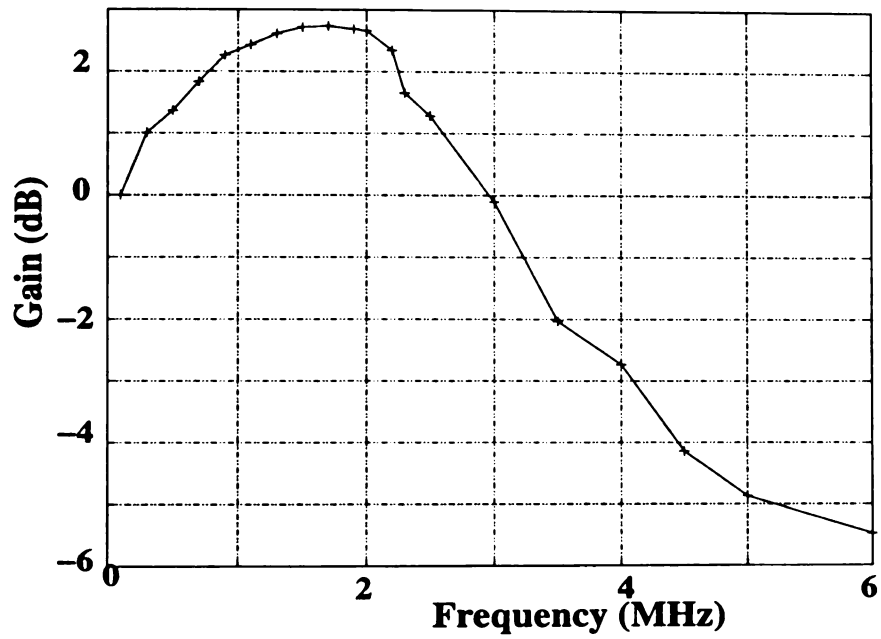
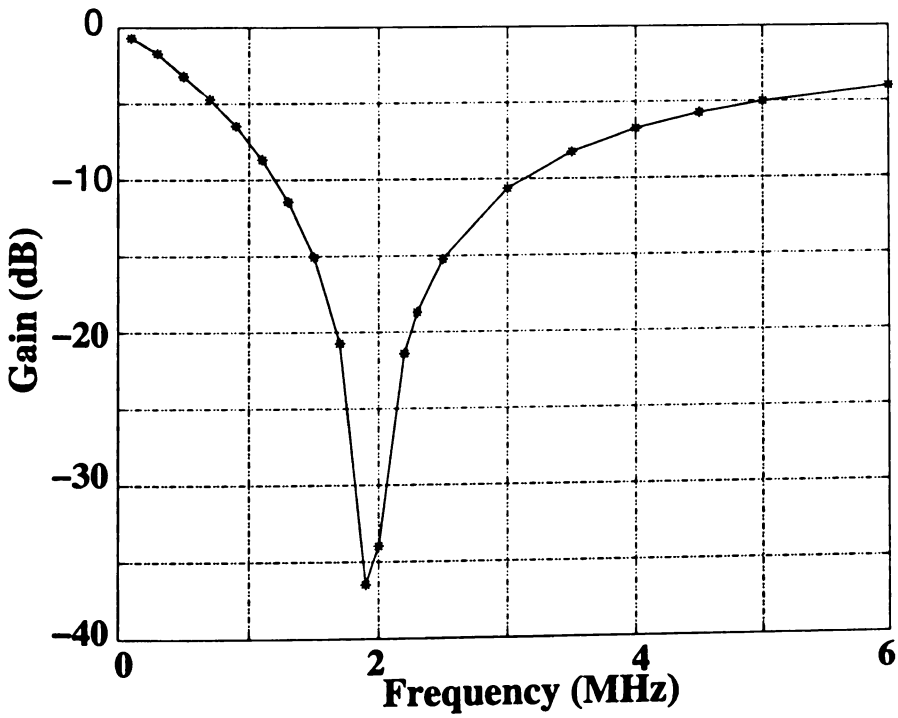


Figure 4.11: Circuit Configuration for Active Polyphase Filter Simulation.



(a)



(b)

Figure 4.12: Simulated Frequency Response of 4-Phase Polyphase Filter with Nauta's Gm Cell: (a) Signal Gain; and (b) Image Gain.

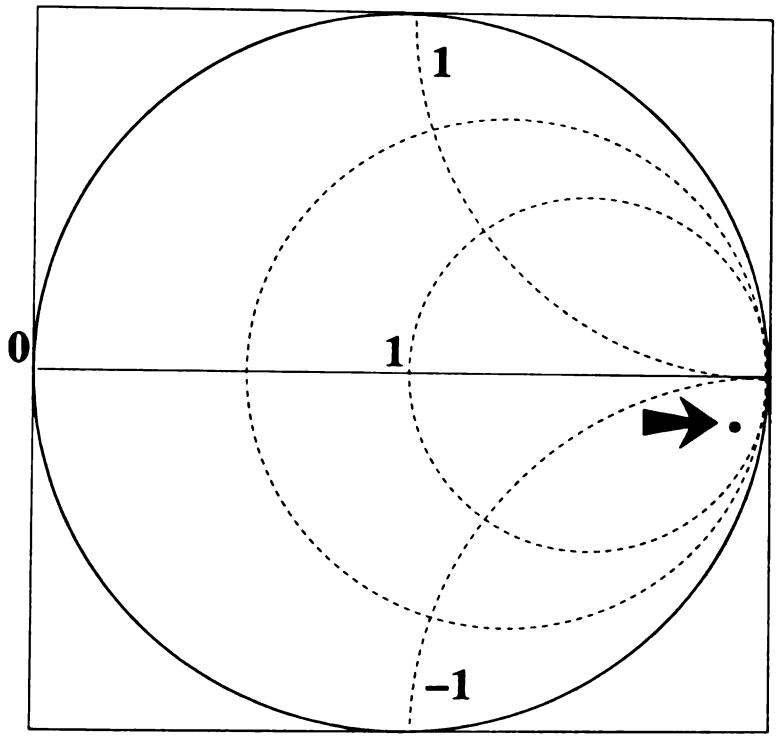


Figure 4.13: S_{22} of LNA for Frequencies from 2.4-GHz to 2.5-GHz.

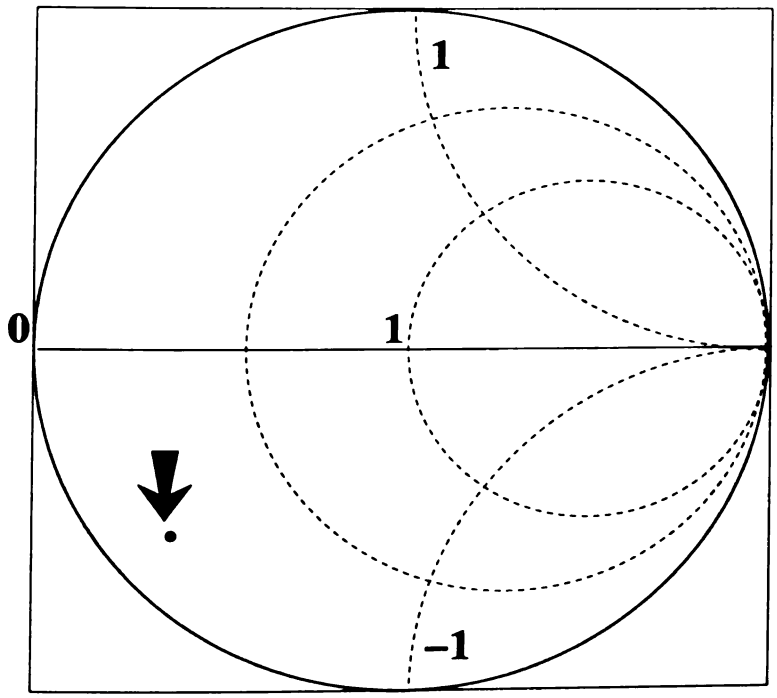


Figure 4.14: S_{11} of Mixer for Frequencies from 2.4-GHz to 2.5-GHz.

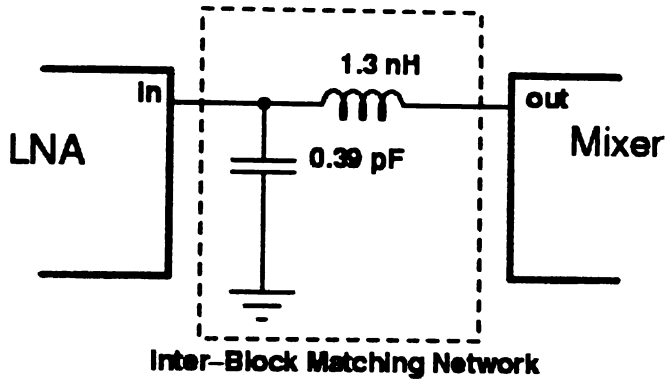


Figure 4.15: Impedance Matching Network between LNA and Mixer.

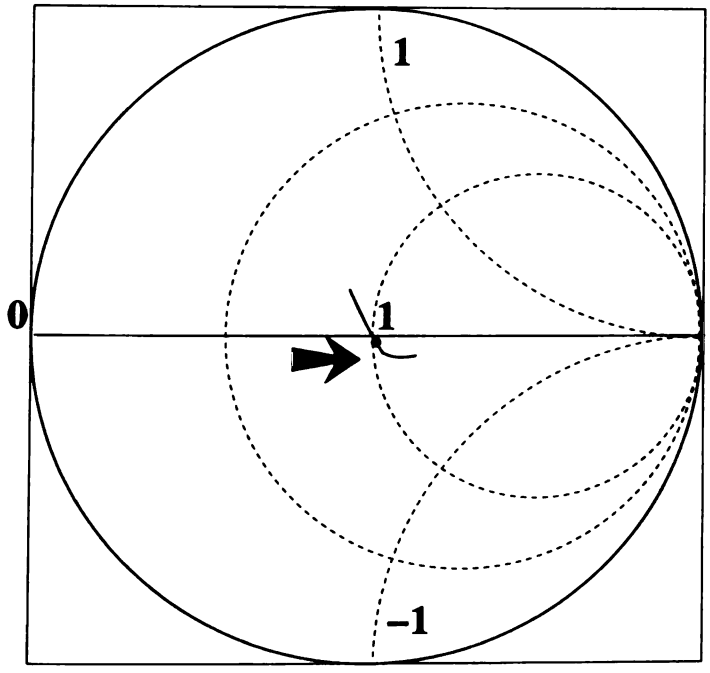


Figure 4.16: S_{11} of Mixer with Impedance Matching Network for Frequencies from 2.4-GHz to 2.5-GHz.

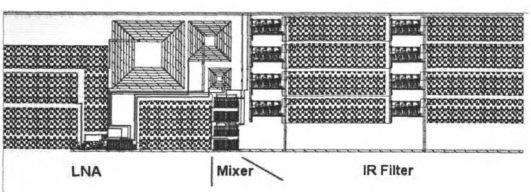


Figure 4.17: Front-End Layout.

Table 4.1: Post-Layout Simulation Results of MRFEC

	MRFEC	F. Beffa *et al.*[114]
I_{dd}	3.0 mA	3.6 mA
Conversion Gain	18 dB	21.4 dB
Image Rejection Ratio	20 dB	28 dB
IIP3	-5.89 dBm	-18 dBm
Noise Figure	8 dB	13.9 dB

5 CONCLUSIONS

This thesis deals with the problem of designing low-power monolithic receiver front-end IC in standard digital CMOS technology for portable radio-frequency wireless communication applications. Such design is difficult largely because of the complicated balances among power, speed, and linearity. Proper decisions have to be made to address the balance issue at four design levels, namely, technology level, device level, building block level, and architecture level. The designers have much more control over the design at building-block level than they have at the other three levels. Therefore success of the whole front-end design heavily depends on the design quality at building block level, which entails various design techniques and circuit topologies.

This thesis has proposed effective design techniques and circuit topologies for low-power RF front-end design in CMOS. The rationale behind the thesis work is that, for each design problem we first *identify* the major tradeoff involved, then develop methods or circuit styles to *address* such tradeoff. For integrated LNA, the major design tradeoff was identified to be the balance among power, thermal noise of low-Q inductors, and channel thermal noise of transconductance transistors. Therefore we proposed a novel method for noise-constrained optimization of integrated CMOS LNA for low power. For integrated Gilbert mixer in CMOS, the major design tradeoff was identified to be the balance between power and linearity of mixer tranconductance stage. Therefore we proposed a novel method to analyze the linearity performance of mixer transconductance stage, which lead to a novel

modified topology of Gilbert Cell. For integrated image-rejecting filter in CMOS, we did not identify the major design tradeoff due to tight time budget for the thesis. Rather, we explored a novel implementation of integrated image-rejecting filter, which is the asymmetric polyphase network filter with Nauta's transconductor.

An integrated CMOS front-end for 2.4-GHz Bluetooth applications has been designed and laid out using the design techniques and circuit topologies proposed in this thesis. The simulation results have shown that the frond-end power is significantly reduced compared with similar implementations in the literature. Meanwhile, the front-end performance is still good except that image-rejection-ratio (IRR) fails to meet the Bluetooth requirement. Better image rejecting could be achieved as long as we identify the major design tradeoff for integrated complex filter and develop methods for optimization in future.

In conclusion, this thesis presented several effective design techniques and circuit topologies for the design of integrated CMOS front-end. Further, this study outlined a number of interesting research topics for future research:

1. How to model the relationship between intrinsic IIP3 of NMOS device and that of the whole mixer in a quantitative way.
2. How to identify the major tradeoff involved in the design of integrated image-rejecting filter.
3. How to optimize the tradeoffs *among* building blocks of RF receiver for low power and integrated implementation.

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