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Analysis and Design of Post-CMOS Thermally Controlled Biosensor Array Microsystems

presented by

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Major Professor's Signature

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ANALYSIS AND DESIGN OF POST-CMOS THERMALLY CONTROLLED BIOSENSOR ARRAY MICROSYSTEMS

By

Nathan Andrew Dotson

A THESIS

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ABSTRACT

ANALYSIS AND DESIGN OF POST-CMOS THERMALLY CONTROLLED BIOSENSOR ARRAY MICROSYSTEMS

By

Nathan Andrew Dotson

A post-CMOS design and fabrication methodology has been investigated for the generation of a microsystem which supports a protein-based biosensor array with thermal control. Implementation of this microsystem design requires a clear understanding of the various layers and their role in CMOS processing technology, especially when the MEMS structures are to be fabricated post-CMOS. In this work, cost-effective post-CMOS design and fabrication methodology has been developed utilizing an experimentally-derived understanding of the various CMOS layers in the AMI C5F/N 0.5μm process available through the MOSIS service. Derived techniques have been applied to the design of thermally isolated biosensor sites for fabrication on MOSIS integrated circuit die. A study of the laws governing heat transfer has been completed for proper integration of temperature control to the designed biosensor sites. Necessary circuitry for the control and design of the thermal system has been designed and is discussed in this work. The results of this thesis work enable the construction of thermally controlled biosensor array microsystems through basic MEMS fabrication steps.

To my grandfather,

James Bloom

and

to my wife,

Kerry

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I thank my parents for all of their support and encouragement, without them none of this would have been possible. Whenever I have been in need, there was always

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Chapter 1. Introduction

Micro-Electro-Mechanical Systems (MEMS) is the combination of mechanical elements, transducers, and electronic circuitry on a common silicon wafer through microfabrication technology. The electronic circuitry is fabricated using IC fabrication technologies such as CMOS, while the MEMS components are fabricated using compatible micromachining processes that selectively etch away parts of the silicon wafer or add new structural layers to form the mechanical and electromechanical devices. These micromachining processes, in many instances, must be performed very carefully in a controlled process flow and developing these processes can be quite difficult depending on the MEMS devices and the fabrication process used for the circuitry. MEMS technology has opened the doorway to an entirely new category of "smart" products by combining the computational power of microelectronics with the observational and control capabilities of sensors and actuators. Sensors within the system extract information from the environment by the measurement of parameters such as mechanical, thermal, biological, or numerous other attributes. The electronics then process the information derived from the sensors and control the environment for some desired outcome or purpose. MEMS devices are created using many of the same fabrication steps as integrated circuits and, because of this, many types of sensors can be scaled down to the micron level at low cost without sacrificing the reliability and functionality of the transducer. There has been a trend to miniaturize and generate all types of sensors in MEMS systems, but MEMS biosensor systems are still in the early stages and there are

many challenges involved in combining biosensors with control circuitry in one system-on-chip. Traditionally biosensors are quite large and integrating them into a microsystem can pose a problem. Research in the area of biosensors and their applications has been widely studied and investigated at macroscopic level. However, interest has shifted to the area of MEMS biosensors for several reasons. First, it is believed that by scaling down the biosensors to a microscopic level, a more robust sensor can be developed. Not only can a sensor be more sensitive and accurate, but also many more sensors can be placed into one system-on-chip that will allow for multiple element detection in a solution. One other important reason for the push of MEMS biosensors is the ease of mass-fabrication and lower cost biosensor systems that can be developed using VLSI design and foundry services.

1.1 Motivation

Biosensor systems have been developed for several applications to date, but one critical area has been overlooked. Temperature plays a vital role not only in the operation of biosensors, but also in the lifetime of the sensor. This thesis proposes a technique for improving biosensor lifetime and functionality by integrating temperature control within the sensor along with low cost fabrication techniques to realize biosensor microsystems. Polysilicon resistive elements are used to heat up biosensor structures to the optimal operating temperature. This is the chosen method for temperature control for several reasons:

- Polysilicon is a common material to all CMOS processes.
- Polysilicon heaters are well characterized and controlled within the operating range of many biosensors.

- Heating of these devices improves the overall operation of the device.
- Device performance can be controlled and tailored to different applications via temperature control.
- By utilizing polysilicon as both a temperature sensor and heating element, each biosensor site can contain individual temperature control and sensing capabilities which will in turn improve the operation of the biosensor.

1.2 Previous Research

To date several key areas have been investigated which contribute to this work; biosensor functionality, thermal isolation schemes, and post-CMOS processing techniques. Thermal isolation is a key aspect of this thesis. Methods for generating thermally isolated structures have been established and covered in numerous works [1-7]. Most of these structures are fabricated through a micromachining process post-electronics fabrication. Thermal isolation is an important aspect since uniform heating of the biosensor sites is desired, but elimination of cross-heating between array elements is also a key factor behind thermal isolation. Post-CMOS processing techniques have been used to generate all types of structures and devices in the MEMS arena from MEMS accelerometers to micropumps [2, 8-16]. Previous work has shown that not only can functional MEMS devices be fabricated individually, but they can also be mass fabricated using foundry services and even be developed and integrated into commercial products.

1.3 Summary

Chapter 2 covers the background information on post-CMOS MEMS processing techniques as well as the background heat transfer material and used for the design and generation of post-CMOS thermally isolated structures independent of biosensors. The

design methodology for structures to be generated via a standard CMOS foundry service and the challenges involved will be addressed.

Chapter 3 addresses the specific processing steps involved for the AMI C5F/N process available through the MOSIS foundry service along with a description of the thermal analysis and how it applies to the structural design of several possible thermal isolation structures for biosensor arrays that are possible through this design. Experimental results for generating structures and analyzing their thermal characteristics will also be covered.

Chapter 4 covers the design of a thermally controlled biosensor array microsystem. A description of the microsystem and all of the necessary circuitry for realizing this system are covered. Along with the chip design, preliminary simulation results will be given, and testing techniques will be discussed.

Chapter 5 presents the conclusions of this work and will also show the long term goals and future work to be generated from this project.

Chapter 2. CMOS Post-Fabrication Processing and Heat Transfer Background

The combination of mechanical elements, transducers, and electronic circuitry on a common silicon wafer through microfabrication technology is becoming common practice in the engineering world. However, most services that offer such capabilities are limited in their scope or can be quite expensive. In terms of saving money, any MEMS steps that can be performed "in-house" are always desired. There are some downsides to this approach when producing MEMS devices. First, most cleanroom facilities at the university level are very limited in their ability to produce small feature-size electronics. Sub-micron feature sizes are basically not available unless an outside foundry service is used. This is an important point since most control and readout circuitry for MEMS devices are quite advanced and require large chip areas. Also, most academic cleanrooms do not have multi-metal/multi-poly fabrication capabilities which further limits the scope of the electronics. Another critical consideration is process compatibility. Many times a foundry service is used to produce the circuit chip and post-processing steps will be performed on these chips to realize MEMS structures. The post-processing steps required in most all cases are not trivial and careful design and post-processing procedure characterization are required to generate working MEMS microsystems.

Laws of heat transfer must also be considered when designing MEMS systems for thermal applications. A thorough understanding of the laws as they apply to the system is

critical for both an efficient design and predicting the systems operational behavior. This chapter focuses on background material for MEMS post-processing techniques and the challenges involved when combining electronics and structural devices, as well as basic heat transfer analysis as it applies to MEMS design.

2.1 Post CMOS Processing

Post CMOS processing consists of steps taken on silicon wafers or die after circuitry has been fabricated. Multiple procedures can be performed post-CMOS such as photolithography, material etching, and material deposition. There are several key points that must be carefully considered when performing process steps on silicon wafers:

- The steps taken must be compatible with CMOS technology.
    - Low Temperature
    - Prevent contamination
- The wafer must be well protected.
- There must be consistency in the process steps.

Without careful consideration of such issues, the CMOS circuitry can be rendered useless or the functionality may differ from the designed plan. Figure 2.1 shows a flow chart by which most integrated circuitry or ICs are designed. Traditionally in circuit design little consideration needs to be given to such issues as post-CMOS photolithography, but when designing MEMS systems this is a consideration that needs addressed from the first step of functionality for the system. Each step along the way, not only does the circuitry need to be properly designed and tested, but the MEMS portion of the design also needs very careful design planning, especially when the chip will be processed after fabrication to realize one working system on-chip.

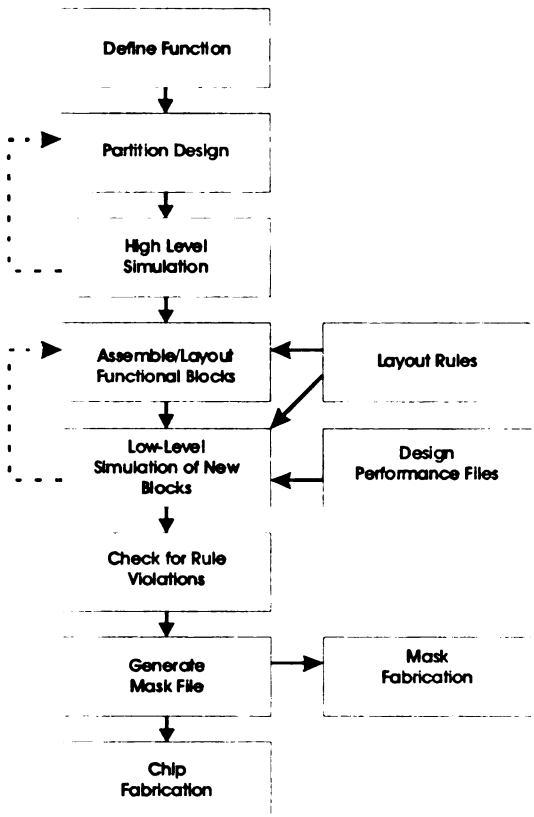

Figure 2-1: *Basic flow chart for VLSI design.*

In this work, photolithography, material etching, and material deposition have been implemented on fabricated wafers. Techniques for performing these steps and key issues for each are to be discussed [17].

2.1.1 Photolithography

Lithography is the most expensive, complex, and critical process in mainstream microelectronic fabrication. As mentioned, lithography is very expensive and accounts for upwards of one-third of the total fabrication cost. To put this into perspective a Pentium 4 processor has approximately 20 masks required. Each of these masks has a

cost of around one million dollars and also, each of these masks needs to be carefully aligned to prior layers, which is a very complex process with feature sizes that are around 0.15μm in newer processor technologies.

Figure 2.2 shows a simple system for optically exposing a wafer during processing procedures. Some type of an optical source is used to shine light through a mask. The image from the mask is then projected onto the wafer surface, which is then coated with some photosensitive material known as photoresist. There are two parts of optical photolithography, the design and operation of the exposure system that passes the mask image onto the wafer and the chemical processes that happen within the photoresist to realize that mask image. The basic physics of optical exposure will be discussed. The tools for photolithography are optical, which means they use light as the exposing radiation whether it is visible light or some wavelength of ultraviolet.

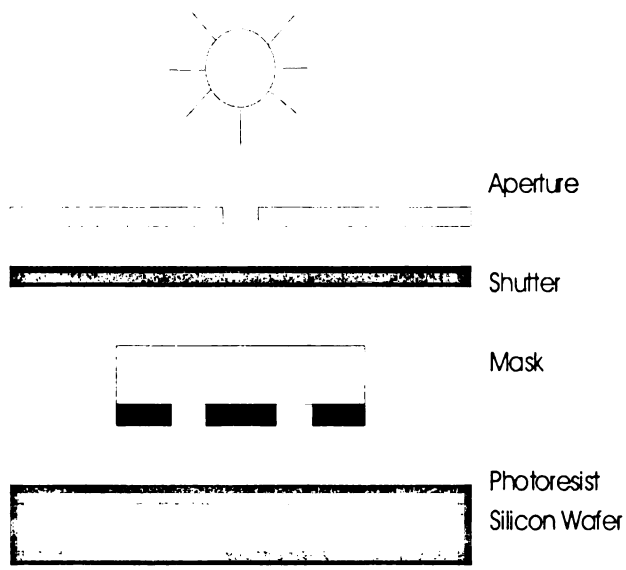

Figure 2-2: *Basic photolithographic exposure system setup.*

Mask aligners are the optical tools used to pass the image of a mask onto a silicon surface. There are several types of aligners used for microfabrication; however the only

one to be discussed is the contact aligner since that is the aligner used in this research. The contact aligner is the simplest type of aligner. In contact alignment printing, the mask is pressed against the photoresist-coated wafer during exposure. The biggest advantage of these systems is the small features that can be generated using relatively inexpensive equipment. In a typical contact system, the mask is held image side down in a frame just below the microscope objectives of the system. Adjustment screws are used to move the wafer with respect to the mask for alignment purposes. Once the wafer is aligned to the mask, they are put into contact with each other, the microscope is retracted, and the wafer/mask is ready to be exposed to the light source. The wafer is then exposed to the high intensity light.

Ideally during this exposure step the entire wafer needs to be in contact often referred to as "hard contact" with the mask. This means that the distance between the wafer and the mask basically goes to zero so effects due to diffraction are minimized and there is essentially a perfect transfer of the mask image onto the wafer surface. The gap can never truly be zero due to the thickness of the photoresist layer. Also, the mask is usually not in complete contact with the wafer since the wafer and the mask are not totally flat. By using very thin masking layers and thin layers of photoresists, however, very small feature sizes are possible during the hard contact. The major downfall of hard contact lithography is the defect generation due to the contact between the resist coated wafer and the mask. These defects cannot be avoided and they are generated both on the wafer and mask during every contact cycle. Because of this, contact printers are used mainly for research or other applications that can tolerate a large amount of defects.

The mask used in the photolithographic process is a key component on the fabrication process. The mask is in most all cases a glass plate that is transparent to ultraviolet light. This glass is then patterned with the desired pattern. Traditionally the pattern of interest is generated on the glass by depositing a very thin layer of metal, usually chromium or gold. In mass fabrication the pattern is usually repeated multiple times so many copies of the design can be fabricated simultaneously. Depending on the polarity of the mask, positive or negative as seen in Figure 2.3, light can either pass through the patterned regions or pass through the regions outside of the pattern onto the photoresist.

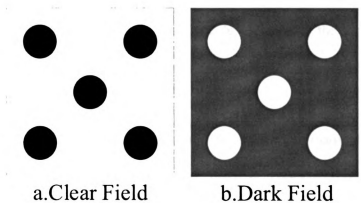

Figure 2-3: *a. Clear field mask. B. Dark field mask. Light is permitted through clear regions and protective polymer will be removed in these regions. Both types of masks will be utilized in post-CMOS fabrication steps.*

The photoresist, often referred to as PR, is a polymer whose chemical properties are altered when it is exposed to UV light. Upon exposure, the PR can be developed in a "developer" much like that used in traditional photography. Depending on the type of PR used there are two results that can be expected. Positive PR is used to etch away areas that have been directly exposed to UV light. Negative PR is hardened in areas that have been exposed to UV light and therefore cannot be removed in the developer solution.

Negative PR requires a more complex procedure to realize patterns and for that reason positive PR is used in this research. PR is in liquid form that is spun onto a wafer at speeds of a few thousand RPM's. Depending on the spinning speed and the characteristics of the PR, a uniform PR thickness in the range of one to tens of microns can be realized. Careful process characterization must be developed for photolithography in this work, issues and solutions for photolithography will be presented in later chapters.

2.1.2 Film Deposition

In standard CMOS fabrication, film deposition is the procedure by which various layers of conductive and insulating materials are deposited onto the surface of a silicon wafer. There are two major types of deposition techniques, physical vapor deposition and chemical vapor deposition.

Physical vapor deposition is capable of depositing many materials onto a surface. The material to be deposited is placed in a chamber that is pumped down to vacuum; the material is then transformed into a gas phase by a variety of methods. In this fashion, atoms of the source material are able to be transferred to the target. It is necessary for the molecular species of the source material to be in a gaseous phase and there are three standard techniques utilized to create this condition; evaporation, sputtering, and ion beam deposition. Physical vapor deposition is typically used to deposit most metals, insulators, and semiconductor films in standard IC processes.

One method for transforming the source material into the gas phase is to use evaporation techniques. The source material is heated so that it melts and then evaporates and there are three approaches, thermal evaporation and electron-beam

evaporation, used to achieve this goal. Thermal evaporation is the easiest of the three and requires the most basic system. The material to be deposited is place inside of a crucible in a vacuum chamber and the crucible is then heated until the material evaporates. Heating of the crucible is accomplished in several fashions, but resistive and inductive heating techniques are the most common in practice. The temperature required to evaporate the material depends on the vapor pressure of the material and on the pressure. The downfall to this method of deposition is that few materials can be deposited in this fashion. Deposition is limited to metals such as Al, Au, and metals with higher vapor pressures.

Another common technique used to evaporate materials is electron-beam evaporation. A high-energy electron beam is used to heat and melt the source material in e-beam evaporation. Higher temperatures can be achieved using this technique and because of this, a wider range of materials can be deposited. In addition to metals with lower vapor pressures, some insulators can be deposited. Also, since the crucible is not directly heated as much, the possibility of contamination through e-beam evaporation is lowered when compared to thermal evaporation. For these reasons, e-beam evaporation is commonplace in the IC industry today.

The third method of physical vapor deposition is sputtering. Basically sputtering consists of bombarding the source material with an ion beam. The ion beam is generated through an arc discharge in a pressure range of 1-100μTorr, with voltages of 500-1000V. The ion beam is then formed into a narrow column, accelerated and then impinged upon the source. As the ions hit the source, the source atoms are knocked off and land on the substrate. Sputtering is the best of the three PVD methods for a few reasons. First,

sputtering offers excellent cleanliness and control to the deposition process. Another key feature is the fact that both deposition of materials and etching can be performed at the same time. This is accomplished by focusing the ion beam on the wafer to achieve etching. Multiple ion beams can be used in this fashion to achieve deposition and etching. Sputtering is also very desirable due to the wide range of materials that are able to be deposited; insulators such as silicon oxide that in other cases must be thermally grown can be deposited.

A key feature of each PVD technique is the fact that the temperature of the source material in each is raised significantly, but the temperature of the substrate is typically maintained at or near room temperature. This is of particular importance when dealing with MEMS post-processing as in this work. The temperature of fabricated devices cannot be raised too much or the Al used in the fabrication process may melt.

The alternative to physical vapor deposition is chemical vapor deposition. Chemical vapor deposition is used to deposit thin films onto a substrate from a gas phase. Several types of chemical vapor deposition techniques are available; low pressure chemical vapor deposition, plasma-enhanced chemical vapor deposition, and photo chemical vapor deposition. Most all of these techniques raise the substrate temperature above 300°C, so these are performed at higher temperatures than the physical vapor deposition techniques already discussed and can cause problems especially in fabricated circuitry. Chemical vapor deposition techniques are mostly used for the deposition of insulators and semiconductor materials due to the conformal nature of the deposition. Due to temperature, complexity, and contamination issues that may arise due to CVD

techniques, these techniques are not favorable for use in this research and will not be discussed in further detail.

2.1.3 Etching Techniques

The etching process in CMOS and MEMS fabrication consists of removing a selected material by adding a substance to the environment, usually a liquid or gas that will selectively attack a target material. When discussing etching it is useful to begin with a discussion of prime factors in the etching process. The main factor is the etch rate, which is defined as thickness etched over time. A high etch rate is usually desired in the manufacturing environment, but if the etch rate is too high, the process may be very difficult to control and reproduce. It is very common to have etch rates on the order of hundreds or thousands of angstroms per minute. Another important factor is the etch rate uniformity which is measured in percentage variation of the etch rate. This is often quoted across the wafer and from one wafer to another. Another very important etching factor, especially in MEMS design is the selectivity of the etchant. Selectivity is the ratio of the etch rates of various materials, such as a PR mask or an underlying layer, referenced to the film that is being patterned or material being etched away. In many cases photoresist is used as the making layer in CMOS fabrication, so etchants must be selected that do not etch PR. When post-CMOS processing is to be implemented, careful planning in the design phase for all phases of the design is crucial for a working system. One area for careful consideration must be substrate damage. For example, p-n junctions have been shown to degrade under certain types of etching. The amount of degradation depends not only on the etch process, but also on the depth and type of junction.

Etchants must be chosen for post-CMOS processing that will not effect the active circuitry and this may prove difficult in certain scenarios.

After the design phase the type of etchant to be used must be decided upon. The first consideration to be taken into account when choosing an etchant for post-processing is whether to use an isotropic or an anisotropic etchant. Some etchants are purely isotropic, which means they will etch the target material at the same rate in all directions. Many times these etchants are avoided, if possible, since there can be considerable reduction in feature sizes, especially as a layer's thickness becomes larger. The other type of etchant, anisotropic, is often preferred since the exact pattern and dimension of the mask can be patterned onto the thin-film material. Often times, the masking layer is attacked by the etchant at a greatly reduced rate. So for long etches, mask erosion and undercut may be a problem. Examples of these etching techniques are seen in Figure 2.4.

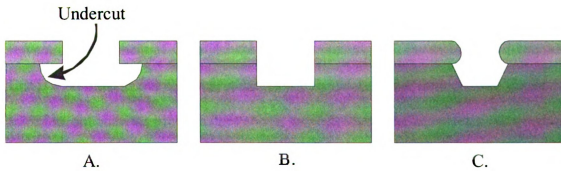

Figure 2-4: *A. Isotropic etch, note that the etch rate is the same for all directions. B. Anisotropic etch, note, the etch is direction dependant which adds some control to the etching process. C. Mask erosion and undercut which can result from very long etches.*

The next major consideration is whether to choose a wet or dry etching process. Wet etching is a purely chemical process that, if not performed carefully, can have serious drawbacks: a lack of anisotropy, poor process control, and excessive

contamination to the system. However, wet etching can be highly selective and often does not damage the substrate. As a result it continues to be used for a wide range of applications. A more complete overview of wet etching can be found elsewhere [18].

The reactive species is often present in the etching solution, so wet chemical etching consists of three processes: movement of the etchant species to the surface of the wafer, a chemical reaction with the exposed material to be etched that produces soluble by-products, and movement of the reaction products away from the surface of the wafer. All three of these processes must occur and the slowest one, referred to as the *rate limiting step*, determines the etch rate. Since it desired to have a large, uniform, well controlled etch rate, the wet etch solution is often agitated in some manner to assist in the movement of etchant to the surface and the removal of the etch product.

For most chemical wet processes, the film or material to be etched is not directly soluble in the etchant solution. It is usually necessary to change the material to be etched from a solid into a liquid or a gas. If the etching process produces a gas, this gas can prevent the movement of fresh etchant to the surface through the formation of bubbles. This is a problem in wet chemical etching since the formation of these bubbles cannot be predicted, although the problem does appear to be the most pronounced near the edges of a pattern. Agitation in the wet chemical etch can help to reduce this problem, at the same time preventing the bubbles from adhering to the surface if they do happen to form. Microscopic bubbles of trapped gas have been linked to this phenomenon [19]. Another common problem in wet etching is that of resist scumming. Resist scumming occurs when some of the exposed PR layer is not removed during the developing step. This can be caused by several factors including incomplete exposure and PR layer non uniformity.

This can be a major factor when etching, since even a thin layer of PR can retard the wet etch process.

Wet etching is used to pattern a wide variety of materials. A table of common wet etchants and the materials they etch is found in Table 1.

Table 1: *Wet etchants and basic properties.*

Material	Wet Etchant	Masking Material
SiO_2	Buffered Hydrofluoric Acid (BHF)	Photoresist
Si_3N_4	Hot Phosphoric Acid	Silicon Dioxide
Al	Phosphoric + Acetic + Nitric Acid	Photoresist
Cr	Hydrochloric Acid (HCl)	Photoresist
Au	Potassium Iodine (KI)	Photoresist
Si (Isotropic)	HF + HNO_3 + Acetic (1:3:8)	Silicon Dioxide or Silicon Nitride
Si (Anisotropic)	KOH, TMAH, EDP	Silicon Dioxide or Silicon Nitride

Isotropic etching is sufficient for many applications, but some technologies including MEMS require directional specific etching to realize structures. Many times the bulk silicon is etched away from patterned areas to create such structures. Common anisotropic wet etchants for silicon etch the (100) and (110) directions much faster than the (111) directions and the specific etch rates have been reported [20-26]. This type of etching is widely used when creating MEMS structures post-CMOS, especially when electronics on-chip are located near structural elements as a preventative measure against device contamination and malfunction. Isotropic etchants and the issues involved with post-CMOS processing on MOSIS die will be discussed in further detail later.

The other major technique used for etching is dry etching. There are several techniques used for dry etching that are common place in microfabrication today: plasma etching, reactive ion etching, high density plasma etching, and ion milling. There are

some definite advantages to dry etching when compared to wet etching. Dry etches are usually much easier to start and stop than typical immersion wet etching. Also these etching procedures are less sensitive to small temperature changes of the wafer. These two factors make dry etching more repeatable than most wet etches. Another key feature is the high anisotropy of dry etching. Usually plasma environments have far fewer particles in the system than in wet etching, which can lead to much less chemical waste and a reduced chance of contamination to the wafer. Dry etching has its advantages, but usually these systems are much more expensive and require a high level of attention. Dry etching may be utilized in the future in this research, but for the current work, wet etching techniques are used for the cost and ease of experimental setup.

2.2 Basic Heat Transfer Analysis

The area of thermal science in the engineering world includes thermodynamics and heat transfer. Heat transfer's role is to supplement thermodynamic analyses, which consider only systems in equilibrium, with additional laws that allow prediction of time rates of energy transfer. These laws are based upon the three fundamental laws of heat transfer, conduction, convection, and radiation [27].

2.2.1 Conduction

A temperature gradient within a homogeneous substance results in an energy transfer rate within a medium that can be calculated by *Fourier's Law*

$$q = -kA\frac{\partial T}{\partial n} \qquad \textbf{Eq. 2-1}$$

here $\frac{\partial T}{\partial n}$ is the temperature gradient in the direction normal to the area A. The thermal conductivity k is an experimental constant for the medium involved, and this constant may depend on other properties, such as temperature and pressure which will be discussed in further detail later. The units for k are $W/_{m \cdot °K}$.

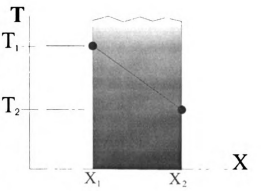

Figure 2-5: *Graphical representation of Fourier's Law.*

The minus sign in *Fourier's Law* is required by the second law of thermodynamics, which states: thermal energy results from a thermal gradient which must be from a warmer to a colder region.

If the temperature profile within the medium is linear as shown in Figure 2-6 above, it is allowable to replace the temperature gradient with

$$\frac{\Delta T}{\Delta x} = \frac{T_2 - T_1}{x_2 - x_1} \qquad \textbf{Eq. 2-2}$$

This type of linearity is always seen in a homogeneous medium of fixed k during steady state heat transfer.

Steady state heat transfer occurs whenever the temperature at every point within the body, including the surfaces, is independent of time. If the temperature changes with time, energy is either being stored in or removed from the body. The storage rate is

$$q_{stored} = mc_p \frac{\partial T}{\partial t} \qquad \textbf{Eq. 2-3}$$

where the mass m is the product of volume V and density ρ [27].

2.2.2 Convection

Whenever a solid body is exposed to a moving fluid having a temperature gradient from that of the body, energy is carried or convected from or to the body by the fluid.

If the temperature of the upstream temperature of the fluid is T_∞ and the surface temperature of the solid is T_s, the heat transfer per unit time is given by

$$q = hA(T_s - T_\infty) \qquad \text{Eq. 2-4}$$

which is known as Newton's law of cooling. This equation defines the convective heat transfer coefficient h as the constant proportionality relating the heat transfer per unit time and unit area to the overall temperature difference. The units of h are $W/m^2 \bullet ^\circ K$. The fundamental energy exchange at a solid-fluid boundary is by conduction, and this energy is then convected away by the fluid flow. From earlier equations we obtain

$$hA(T_s - T_\infty) = -kA\left(\frac{\partial T}{\partial y}\right)_s \qquad \text{Eq. 2-5}$$

where the subscript on the temperature gradient indicates evaluation in the fluid at the surface [27]. Convection can be via two modes forced convection and natural convection. Natural convection will be the mode of convective heat transfer in this work and the analysis will be discussed further in later sections.

2.2.3 Radiation

The third mode of heat transmission which does not really apply to this research is due to electromagnetic wave propagation, which can occur in a total vacuum as well as in

a medium. Experimental shows that radiant heat transfer is proportional to the fourth power of the absolute temperature, whereas conduction and convection are proportional to a linear temperature difference. The fundamental Stefan-Boltzmann law is

$$q = \sigma A T^4 \qquad \textbf{Eq. 2-6}$$

where T is the absolute temperature. The constant σ is independent of surface, medium, and temperature; its value is $5.6697 \times 10^{-8} W/m^2 \bullet °K^4$.

The ideal emitter or blackbody, is one which gives off radiant energy according to the Stefan-Boltzmann law. All other surfaces emit somewhat less than this amount, and the thermal emission from many surfaces can be represented by

$$q = \varepsilon \sigma A T^4 \qquad \textbf{Eq. 2-7}$$

where ε, the *emissivity* of the surface, ranges from zero to one [27].

2.3 Material Properties Affecting Heat Transfer

2.3.1 Thermal Conductivity of Solids

Thermal conductivities of numerous pure metals and alloys are well known and widely available. The thermal conductivity of the solid phase of a metal of known composition is primarily dependent only upon temperature. In general, *k* for a pure metal decreases with temperature; alloying elements tends to reverse this trend.

The thermal conductivity of a metal can usually be represented over a wide range of temperature by

$$k = k_0(1 + b\theta + c\theta^2) \qquad \textbf{Eq. 2-8}$$

where $\theta = T - T_{ref}$ and k_0 is the conductivity at the reference temperature T_{ref}. For many engineering applications the range of temperature is relatively small and $k = k_0(1 + b\theta)$.

The thermal conductivity of a nonhomogeneous material is usually very dependent upon the apparent bulk density, which is the mass of the substance divided by the total volume occupied. This total volume includes the void volume, such as air pockets within the overall boundaries of the piece of the material. The conductivity also varies with temperature. As a general rule, *k* for a nonhomogeneous material increases both with increasing temperature and increasing apparent bulk density.

2.3.2 Thermal Conductivity of Liquids

For most liquids, *k* is usually temperature dependent on temperature but insensitive to pressure. Thermal conductivities of most liquids decrease with increasing temperature. The exception to this is water, which exhibits increasing *k* up to 150 °C and decreasing *k* after this point. Water has the highest thermal conductivity of all common liquids except the liquid metals.

2.3.3 Thermal Conductivity of Gases

The thermal conductivity of a gas increases with increasing temperature, but is essentially independent of pressure for those close to atmospheric. At high pressures, the effect can be very significant.

2.3.4 Density

Density can be defined as the mass per unit volume. Density data for most solids and liquids are only slightly temperature dependent and are negligibly influenced

by pressure up to 100 atm. The density of a gas, however, is strongly dependent upon the pressure as well as upon the temperature. In the absence of specific gas data, the density can be represented by

$$\rho = \rho_1 \left(\frac{p}{p_1} \right) \qquad \textbf{Eq. 2-9}$$

The specific volume is the reciprocal of the density,

$$v = \frac{1}{\rho} \qquad \textbf{Eq. 2-10}$$

and the specific gravity is the ratio of the density to that of pure water at a temperature of 4°C and a pressure of one atmosphere. Thus

$$S = \frac{\rho}{\rho_w} \qquad \textbf{Eq. 2-11}$$

where S is the specific gravity.

2.3.5 Specific Heat

The *specific heat* of a substance is a measure of the variation of its stored energy with temperature. From thermodynamics the two specific heats are:

$$\text{specific heat at constant volume: } c_v \equiv \left. \frac{\partial u}{\partial T} \right|_v$$

$$\text{specific heat at constant pressure: } c_p \equiv \left. \frac{\partial h}{\partial T} \right|_p$$

Here u is the energy per unit mass and h is the enthalpy per unit mass. In general, u and h are functions of two variables: temperature and specific volume, and temperature and pressure, respectively. For substances which are incompressible, solids and liquids,

c_p and c_v are numerically equal. For gases, however, the two specific heats are considerably different. The units of c_p and c_v are $J/kg\bullet^\circ K$.

For solids, specific heat data are only weakly dependent upon temperature and are even less affected by pressure. It is usually acceptable to use to use the limited specific heat values at constant pressure, over a fairly wide range of temperatures and pressures. Specific heats of liquids are even less pressure dependent than those of solids, but they are somewhat temperature influenced.

Gas specific heat data exhibit a strong temperature dependence. The pressure effect is slight except near the critical state, and the pressure dependence diminishes with increasing temperature. For most engineering calculations specific heats for gases found in common tables are suitable for pressures up to 1.4×10^6 Pa.

2.3.6 Thermal Diffusivity

A useful combination of terms already considered is the *thermal diffusivity* α, defined by

$$\alpha \equiv \frac{k}{\rho c_p} \qquad \textbf{Eq. 2-12}$$

It is seen that α is the ratio of the thermal conductivity to the thermal capacity of the material. Its units are m^2/s. Thermal energy diffuses rapidly through substances with high α and slowly through those with a low α [27].

2.4 One-Dimensional Steady-State Conduction

The conductive heat transfer rate at a point within a medium is related to a local temperature gradient by Fourier's Law **Eq. 2-1**. In many one-dimensional problems we can write the temperature gradient simply by inspection of the physical situation. The situation we are dealing with can be modeled from this basic heat transfer situation by taking the physical geometry of the situation into consideration.

2.4.1 General Conductive Energy Equation

Consider a small control volume consisting of the parallelepiped shown at the right. This may be an element of material from a homogeneous solid or homogeneous fluid so long as there is no relative motion between the macroscopic material particles. Heating of this material then results in an energy flux per unit area within the control volume. This flux is, in general, a three-dimensional vector. For simplification reasons, heat flow is only shown in the x direction.

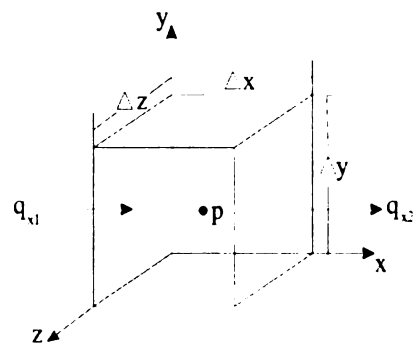

Figure 2-6: *Control solid for general conductive energy equation.*

Application of the first law of thermodynamics to the control volume yields the general conduction equation through the following procedure:

For the control volume shown above, the first law of thermodynamics can be expressed as

(1)

(rate of heat transfer in) + (rate of work in) + (rate of other energy conversion)=

(rate of heat transfer out) + (rate of work out) + (rate of internal energy storage)

For an incompressible substance the net work done on the control volume is converted to internal energy. Denoting the rate of energy conversion (from work, chemical reaction, etc.) as q''', (1) becomes

(2)

$$q_{x1} + q_{y1} + q_{z1} + q'''\Delta x\Delta y\Delta z = q_{x2} + q_{y2} + q_{z2} + \frac{\partial U}{\partial t}$$

Examining the heat transfer terms in (2). In the x-direction the two terms may be grouped to form

(3)

$$q_{x1} - q_{x2} = -\Delta y\Delta z\left[\left(k\frac{\partial T}{\partial x}\right)_{x1} - \left(k\frac{\partial T}{\partial x}\right)_{x2}\right]$$

by the application of Fourier's Law. Notice that k may be temperature dependent and because of this, spatially dependent. By a Taylor series expansion about the center point P.

$$\left(k\frac{\partial T}{\partial x}\right)\Bigg|_{x1} = k\frac{\partial T}{\partial x} + \left(-\frac{\Delta x}{2}\right)\frac{\partial}{\partial x}\left(k\frac{\partial T}{\partial x}\right) + \ldots$$

$$\left(k\frac{\partial T}{\partial x}\right)\Bigg|_{x2} = k\frac{\partial T}{\partial x} + \left(-\frac{\Delta x}{2}\right)\frac{\partial}{\partial x}\left(k\frac{\partial T}{\partial x}\right) + \ldots$$

so that (3) becomes

(4)

$$q_{x1} - q_{x2} = \Delta y\Delta z\left[\Delta x\frac{\partial}{\partial x}\left(k\frac{\partial T}{\partial x}\right) + \ldots\right]$$

Similarly,

(5)

$$q_{y1} - q_{y2} = \Delta x \Delta z \left[\Delta y \frac{\partial}{\partial y}\left(k \frac{\partial T}{\partial y} \right) + \ldots \right]$$

(6)

$$q_{z1} - q_{z2} = \Delta x \Delta y \left[\Delta z \frac{\partial}{\partial z}\left(k \frac{\partial T}{\partial z} \right) + \ldots \right]$$

Finally, the internal energy storage per unit volume and per unit temperature is the product of density and specific heat, so

(7)

$$\frac{\partial U}{\partial t} = \rho c \left(\Delta x \Delta y \Delta z \right) \frac{\partial T}{\partial t}$$

Substituting expressions (4) through (7) into (2), dividing by the volume ΔxΔyΔz, and taking the limit as Δx, Δy, Δz simultaneously approach zero yields the general conduction equation.

$$\frac{\partial}{\partial x}\left(k \frac{\partial T}{\partial x} \right) + \frac{\partial}{\partial y}\left(k \frac{\partial T}{\partial y} \right) + \frac{\partial}{\partial z}\left(k \frac{\partial T}{\partial z} \right) + q''' = \rho c \frac{\partial T}{\partial t} \qquad \textbf{Eq. 2-13}$$

This equation is for the temperature T as a function of x, y, z, and t. Here, k is the thermal conductivity, ρ is the density, c is the specific heat per unit mass, and q''' is the rate of internal energy conversion ("heat generation") per unit volume. A common instance of q''' is provided by resistance heating in an electrical conductor.

In most engineering applications k can be taken as a constant, and Eq. 2-12 reduces to

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} + \frac{q'''}{k} = \frac{1}{\alpha} \frac{\partial T}{\partial t} \qquad \textbf{Eq. 2-14}$$

where α is given by Eq. 2-11 [27].

2.4.2 Plane Wall Fixed Surface Temperatures

The simplest heat transfer problem is that of one-dimensional, steady-state conduction in a plane wall of homogeneous material having constant thermal conductivity and with each face held at a constant uniform temperature as shown at the right.

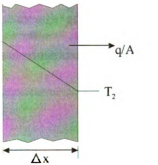

Figure 2-7: *Heat transfer by conduction in a plane wall.*

Separation of variables and integration of Eq. 1 where the gradient direction is x results in

$$q\int_{x_1}^{x_2} dx = -kA\int_{T_1}^{T_2} dT \qquad \textbf{Eq. 2-15}$$

or

$$q = -kA\frac{T_2 - T_1}{x_2 - x_1} = -kA\frac{T_2 - T_1}{\Delta x}$$

This equation can be rearranged as

$$q = \frac{T_1 - T_2}{\Delta x / kA} = \frac{\text{thermal potential difference}}{\text{thermal resistance}} \qquad \textbf{Eq. 2-16}$$

Notice that the resistance to the heat flow is directly proportional to the material thickness, inversely proportional to the material thermal conductivity, and inversely proportional to the area normal to the direction of heat transfer.

These principles are readily extended to the case of a composite plane and can be directly applied to the various layers in the CMOS design flow. The case for the composite plane which will later be extended to multiple layers is shown in Figure 2-8 (a) below:

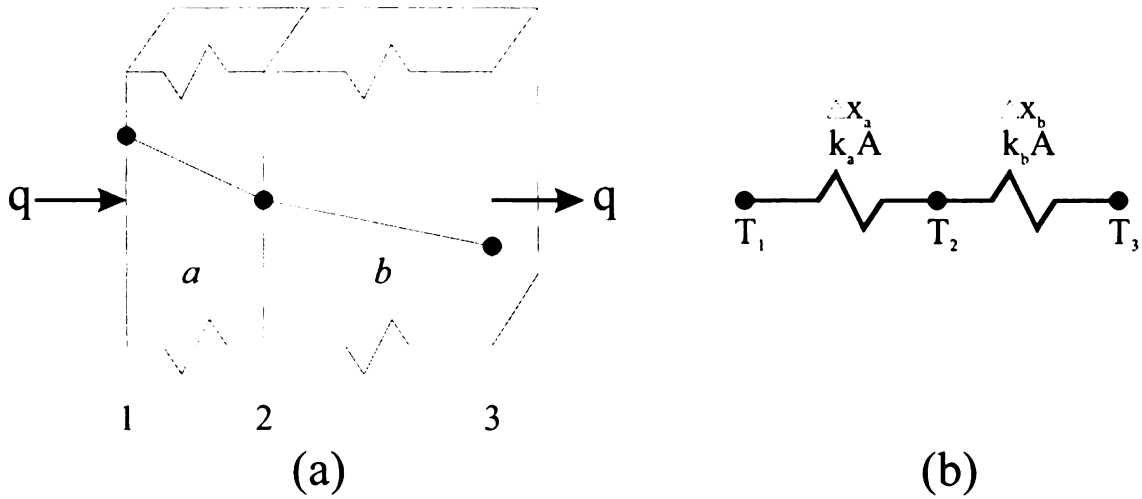

Figure 2-8: *(a) Heat transfer through a composite wall. (b) Equivalent thermal resistance of composite wall.*

In the steady-state the heat transfer rate entering the left face is the same as that leaving the right face. Thus,

$$q = \frac{T_1 - T_2}{\Delta x_a / k_a A} \quad \text{and} \quad q = \frac{T_2 - T_3}{\Delta x_b / k_b A}$$

Together these give:

$$q = \frac{T_1 - T_3}{\left(\Delta x_a / k_a A\right) + \left(\Delta x_b / k_b A\right)} \qquad \textbf{Eq. 2-17}$$

Equations 12 and 13 illustrate the analogy between conductive heat transfer and electrical current flow, an analogy that is rooted in the similarity between Fourier's and Ohm's laws. It is convenient to express Fourier's law as

$$\text{conductive heat flow} = \frac{\text{overall temperature difference}}{\text{summation of thermal resistances}} \qquad \textbf{Eq. 2-18}$$

In the case of Figure 2-8 (a) above the total thermal resistance is simply the sum of the two resistances in series as shown in Figure 2-8 (b) above. The extension to three or more layers is obvious.

2.5 Thermal Equivalent Circuit

The above arguments and analyses can be combined to form an electric circuit that will simulate the operation of our MEMS biosensor system. In performing these simulations and the basic heat flow analysis that follows from these results, there are several assumptions that have been made to simplify the model for basic design and characterization:

- Material is much longer and wider than it is thick, so that only the vertical heat flow must be considered
- Region inside the heater material has a uniform temperature, T_F (final temperature after heating)
- All transfer is by conduction within the solid and a convective boundary layer between our structure and the fluid environment (negligible radiation)
- A conductive analysis is used when analyzing sealed air cavities due to small finite geometry of sealed cavity
- Temperature changes are small enough that the thermal conductivity, *k*, can be assumed constant (generally, *k* is a function of temperature, layer thickness, and doping)

The basic thermal circuit for spice simulations is shown below [28]. This circuit allows simulations to be run on proposed biosensor structures. These are important simulations since they give estimates of what temperatures can be realized for the CMOS process that will be used when fabricating these MEMS devices.

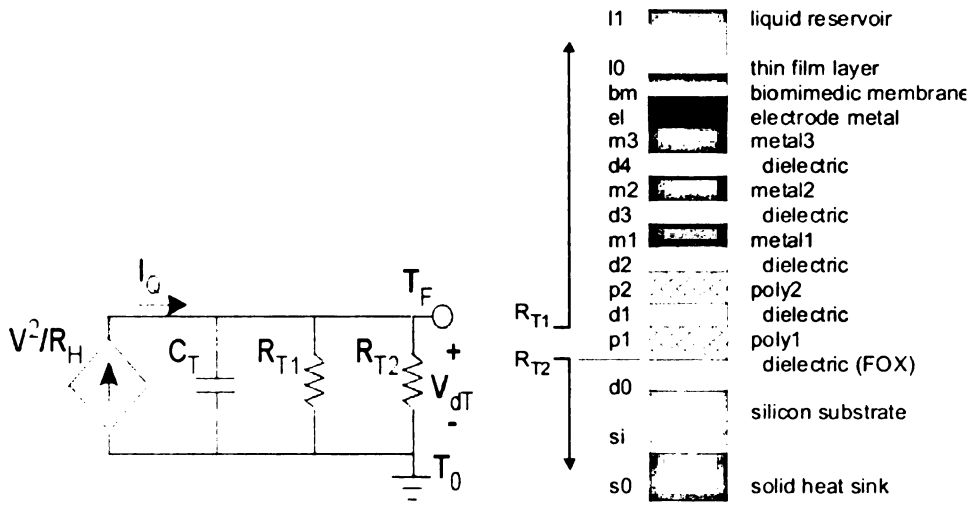

Figure 2-9: *(left) thermal equivalent circuit for a biosensor heater, and (right) diagram of the base layers that comprise the biosensor structure without structural etch release.*

The components used in this thermal model are defined by the following:

R_H is the heater resistance [Ohms]

V is the voltage across the heater resistor [Volts]

$V=I_H R_H$, where I_H is the heater electrical current

C_T is the heat capacity of the heater [Joules/Kelvin]

R_{T1} is the thermal resistance above the heater [Kelvin/Watt]

R_{T2} is the thermal resistance below the heater [Kelvin/Watt]

T_F is the final temperature [Kelvin]

T_0 is the initial (background) temperature [Kelvin]

V_{dT} is the equivalent thermal voltage due to temperature difference, $dT = T_F - T_0$ [Kelvin]

I_Q is the equivalent thermal current [Watts]

[Watt = Volt * Amps = $Volt^2/Ohm$]

[Joules = Watt * seconds]

The thermal equivalent circuit can be analyzed by looking at basic conduction and convective heat transfer and building the heat flow model for the structure.

The difference in temperature, = $T_F - T_0$, (created by delivering electrical power to the heater) generates a heat flux out of the heater given by Fourier's law for heat conduction, Eq. 1 above. Where $\nabla T = dT/dn$ is the change in temperature over vertical distance x, k is the thermal conductivity [25 Watts/(Kelvin-meter)] of the heater material and J_Q has units of [Watts/meter^2].

If we assume the surface area through which this heat flows is a square around the heater element with a side length of W [meters], then we can express the total heat current through the surface as

$$I_Q = kW^2 \frac{\partial T}{\partial x} \qquad \textbf{Eq. 2-19}$$

where the negative sign is dropped since temperature decreases with increasing distance, x, from the heater. Solving this for dT we get,

$$T_F - T_0 = \int_0^{X_f} \frac{I_Q}{kW^2} \partial x = \frac{I_Q}{kW^2} X_f \qquad \textbf{Eq. 2-20}$$

where X_f is the distance from the heater that the temperature reaches T_0. For a more general expression, we note that the temperature will drop to some value T_i ($T_F > T_i > T_0$) at a distance Xi from the heater which will be given by the expression

$$T_F - T_i = \frac{I_Q}{kW^2} X_i \qquad \textbf{Eq. 2-21}$$

2.5.1 Thermal Resistance

It is useful at this point to introduce the notation of thermal resistance of a material, R_T, defined the temperature drop across the material per unit heat current, or

$$R_T = \frac{\Delta T}{I_Q} = \frac{X}{kW^2} = \frac{1}{hW^2} \qquad \text{Eq. 2-22}$$

where X is the thickness of the material. This expression combined with ideas laid out in the section dealing with heat transfer through a plane wall above, made for this structure, suggest that a series of adjacent thermal resistances will add linearly so that the total equivalent thermal resistance is just the sum of individual thermal resistances for this structure.

$$R_T = \sum_i \frac{X_i}{k_i W^2} \qquad \text{Eq. 2-23}$$

2.5.2 Thermal Boundary Layer: Flat Plate

In modeling the thermal resistance layers for the circuit simulations and heat transfer analysis, the liquid-sensor interface must be analyzed to determine the behavior of this interface.

When a fluid at one temperature is along the surface of a plane which is at another temperature, the behavior of the fluid cannot be described by typical hydrodynamic equations alone. There is an additional thermal boundary layer which develops. In these situations, a temperature gradient exists across the thermal boundary layer. The equation heat transfer in natural convection between fluids and solids of definite geometric shape are of the form:

$$\frac{hL}{k_f} = b\left[\frac{L^3 \rho_f{}^2 g \beta_f \Delta T}{\mu_f{}^2}\left(\frac{c_p \mu}{k}\right)_f\right]^n \qquad \textbf{Eq. 2-24}$$

b and n are constants dependent on the system, in our case we have a heated horizontal plate facing upwards so the components of the equation are defined by:

b=0.54

n=0.25

h= heat transfer coefficient (this is what we are solving for)

L= length of horizontal square surface

k_f = thermal conductivity of fluid

ρ_f = density of fluid

g = gravitational acceleration

β_f = coefficient of volumetric expansion of fluid

ΔT = temperature change dependent on environment and heater temperature

μ_f = absolute viscosity of the fluid

c_{p_f} = specific heat of fluid

Solving for this heat transfer coefficient will allow us to determine the thermal resistance of this boundary layer which is an key parameter in the thermally equivalent circuit [29]. This method for determining the heat transfer coefficient may not be fully accurate for heat transfer at the micro scale, as certain assumptions are being made as to the size of the system.

An additional method for determining the heat transfer coefficient due to natural convection across a wider range of systems is given by a different approach [27]. The thermal boundary layer at this level consists of a laminar flow system. The heat transfer coefficient is given by the following equation:

$$\bar{h} = \frac{\overline{Nu_L} \cdot k}{L} \qquad \textbf{Eq. 2-25}$$

Here $\overline{Nu_L}$ is the Nusselt number which is a ratio of the heat transfer coefficient from the surface of interest to the conductivity of the fluid. The Nusselt number is a function of the Raleigh number which is described by:

$$Ra = Gr \cdot \mathrm{Pr} \qquad \textbf{Eq. 2-26}$$

In this equation, Gr and Pr are the Grashof and Prandtl number respectively. The Grashof-Prandtl number product is used to determine what analysis is applicable to a naturally convective system. For a constant surface temperature, The following equation can be used for determining the Nusselt number across the entire range of Raleigh numbers.

$$\overline{Nu_L} = 0.68 + \frac{0.670 Ra_L^{1/6}}{\left[1 + (0.492/\mathrm{Pr})^{9/16}\right]^{4/9}} \qquad \textbf{Eq. 2-27}$$

In this equation all properties for natural convection are evaluated at the Fluid temperature. The Prandtl is given as a constant for the particular fluid of interest and the Grashof number is then given by:

$$Gr = \frac{g\beta(T_S - T_\infty)L^3}{\nu^2} \propto \frac{\text{buoyancy force}}{\text{viscous force}} \qquad \textbf{Eq. 2-28}$$

The components used in this equation are defined by the following:

g = gravity constant

β = coefficient of volumetric expansion of fluid

L = Characteristic length of convective surface

ν = kinematic vicosity

Both of these techniques for determining the heat transfer coefficient have been used for analysis of thermal array sites in chapter 3.

2.5.3 Heat Capacity of a Polysilicon Resistor

The heat capacity of a material can be expressed as

$$C_T = \rho_m t W L \overline{C}_m \qquad \text{Eq. 2-29}$$

where ρ_m is the mass density of the material (2330 kg/m^3 for polysilicon), t, W, and L are the thickness, width, and length, respectively, of the material, and $\overline{C}_m$ is the specific heat per unit mass (753 J/(kg-Kelvin) for polysilicon). Heat capacity is sometimes given as a per volume constant, such that

$$C_T / V = \rho_m \overline{C}_m \qquad \text{Eq. 2-30}$$

2.5.4 Temperature Coefficient of Resistance

Resistance of a material is a function of temperature (unless specifically designed otherwise). The temperature coefficient of resistance (TCR), αR, is itself generally a function of temperature, but can often be assumed constant over a small temperature range. The TCR is defined as

$$\alpha_p = \frac{R_T - R_{T_0}}{R_{T_0}\left(T - T_0\right)} \qquad \text{Eq. 2-31}$$

where, R_T is the resistance at temperature T and R_{To} is the resistance at temperature T_o. The resistance of the polysilicon is also a function of stress in the material. However the change in resistance due to stress is negligible compared to the change due to temperature and can be neglected for basic analysis.

Extraction of αR is very important for the characterization and performance of the polysilicon resistor that will be acting as a temperature sensor. This parameter must be found through experimental analysis of the resistor in a highly controlled temperature environment over a wide temperature range to ensure accuracy in temperature readings.

2.6 Self-Heating Limitations in Sensor-Resistors

When using resistors to measure temperature, it is important to minimize self heating due to the current applied to measure the resistance. If the sensor-resistor is in good thermal contact with the background temperature reservoir, there will be limited self heating. However, in thermally isolated structures (where there is a large thermal resistance between the resistor and the background temperature reservoir), heat produced from the readout current will not dissipate well. As a result, only a small amount of electrical power can be applied to the sensor-resistor without substantial self-heating. This is a consideration that must be made when designing readout circuitry for the temperature sensing resistor.

2.7 Verification of Thermal Equivalent Circuit Analysis

When checking what types of analysis with which to model the system it is important that we look at the Biot number. The Biot number is dimensionless, and it can be thought of as the ratio

$$Bi = \frac{\text{resistance to internal heat flow}}{\text{resistance to external heat flow}} = \frac{\text{resistance of solid}}{\text{resistance of film}} \qquad \text{Eq. 2-32}$$

Whenever the Biot number is small, the internal temperature gradients are also small and a transient problem can be treated by the "lumped thermal capacity" approach wherein the object for analysis is considered to have a single mass-averaged temperature.

This is the situation that arises in our thermal model. The thermal resistance of the thin film layer is much higher than the internal resistances which allows for the use of a lumped analysis when considering the various structural possibilities for MEMS biosensors as seen in tables contained in the Appendix.

2.8 One Dimensional Systems: Transient Analysis Fixed Surface Temperature

Another key component in analyzing various structures for thermal isolation is the transient characteristics of heat transfer. For some proposed structures there is no thermal boundary layer of high resistance providing thermal isolation between array sites. In these cases there is silicon substrate, an oxide layer, or a combination of the two separating the biosensor array sites. In these cases, the temperature at a distance x away from our heater layer into the silicon substrate, oxide, or other material can be approximated by this particular analysis. In this manner we will see if sufficient thermal isolation coinciding with proper operation of an array site is feasible.

In considering this transient conduction problem, it can be treated approximately by considering the body to be initially at some uniform temperature and suddenly having the temperature of part of the surface changed to and held at a known constant value different from the initial temperature.

The solution to this conductive problem is approximated by using the transient analysis for a semi-infinite body. The solution to a temperature at some distance x below the surface is

$$\frac{T(x,t)-T_s}{T_i-T_s} = erf\left(\frac{x}{\sqrt{4\alpha t}}\right) \qquad \textbf{Eq. 2-33}$$

Values for the Gaussian error function can be obtained from various mathematical tables.

From such analysis MEMS structures can be designed and their behavior modeled down into the body of the MEMS chip.

Chapter 3. MOSIS Post-Processing and Thermal Analysis of Biosensor Array Sites

Analysis of the biosensor array sites is a key component in the design of the MEMS biosensor system. Operation of the system as a whole must first be analyzed by thermal analysis and simulation techniques on individual array site structures to gain an understanding of their operation. After testing and characterization of individual sites has been completed, a better understanding of how these sites will operate and interact with one another can be achieved. On the whole, interaction between array sites is not desired. Ideally in a biosensor array system each array site will be sensing for a different substance and one site should not interfere with the operation of any other sites in the system. One key aspect to this work is the idea of temperature controlled biosensor array sites. It is known that in biosensors there is usually some temperature for which operation of the biosensor is optimized and this is usually at room temperature or above. Also of note is the fact that longevity of the biosensor itself can be lengthened by keeping the biosensor in a low temperature environment. These two factors must be combined to not only extend the lifetime and operation of the sensor itself, but also to achieve the best results from the sensor. In order to achieve this goal, each array site is designed with a heating element and a temperature sensing element. However, each array site must be sufficiently thermally isolated from the system to ensure proper operation of the biosensors. In order to ensure operation of the system, thermodynamic and heat transfer analysis is a crucial component in the design of the biosensor array sites. This chapter

focuses on heat transfer analysis and the basic principals involved that will lead to several design possibilities for array sites.

3.1 Proposed MEMS Structures

The basic fabrication techniques covered thus far are vital for the successful fabrication of MEMS devices. In IC fabrication, the primary interest is in the electronic properties of the materials used. The materials are used to design transistors and other circuit elements in combination to build complex devices sometimes consisting of millions of transistors. One of the key features of microelectronics and planar microfabrication technologies is its ability to form millions of electronic devices on a small substrate and then utilize these simple functions to implement a complex task, cost effectively. MEMS fabrication uses many of the same techniques as IC fabrication to generate complex systems of mechanical devices. There are many microstructures of different shapes, sizes, and materials that can be fabricated. These structures include beams, diaphragms, bridges, and numerous other structures. Many of these structures need specialized techniques to be fabricated. For the proposed MEMS biosensor chip, there are a few possibilities for creating isolated thermal structures post-CMOS which are derived from two basic techniques: silicon bulk micromachining and surface micromachining.

Silicon bulk micromachining is a very common technique used in MEMS fabrication. Bulk micromachining consists of removing the bulk silicon, usually using wet etching techniques, to realize MEMS structures. It is very common to use backside etching which is taking away silicon from the backside of the wafer to realize thin films and diaphragms. This can be a very useful technique; however backside alignment to

circuitry and structures on the front side can be extremely difficult. Another common technique in bulk micromachining is to utilize some masking layer on the frontside of a wafer and to etch the bulk silicon from underneath.

Surface micromachining is often referred to as sacrificial micromachining. In surface micromachining deposited thin films are used for both mechanical and sacrificial layers. All types of standard CMOS materials can be used. Multiple steps are required in this process to realize some structures, but in many cases surface micromachining can be described by two steps. In the first step, a mechanical layer is deposited over a sacrificial layer and somehow anchored to the bulk substrate. In the final step the sacrificial layer is etched away to release the mechanical microstructure. A critical requirement in this release process is that an etchant removes the sacrificial layer very quickly and stops on the mechanical structure. One of the main advantages of surface micromachining is that many layers can be deposited and patterned on top of one another.

The desired MEMS structure for the heated biosensor array is one that will provide sufficient thermal isolation for each array site from its nearest neighbor. Two techniques, backside bulk micromachining and a combination of frontside sacrificial micromachining and bulk micromachining, can be used to generate a structure capable of providing such isolation. Examples of these structures can be seen in Figure 3.1. The issues, including feasibility, associated with each of these structures and the chosen fabrication process will be discussed in further detail.

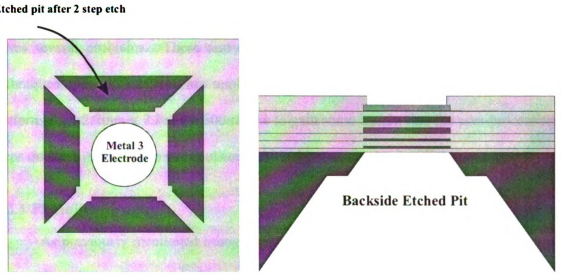

Figure 3-1: *(Left) Suspended structure formed by an anisotropic etch procedure. (Right) Isolated diaphragm formed using a backside etching procedure.*

3.2 MOSIS Post-CMOS Processing

As previously mentioned the fabrication of circuitry for control of a MEMS system is usually always performed by a fabrication service. In this research the MOSIS service is used for the base fabrication of the MEMS system. MOSIS is a low-cost prototyping and small-volume production service for VLSI circuit development. Since 1981, MOSIS has fabricated more than 50,000 circuit designs for commercial firms, government agencies, and research and educational institutions around the world [30].

The process being used is AMI Semiconductor's (AMIS) C5F/N 0.5 micron process. This is a non-silicided CMOS process with 3 available metal layers and 2 poly layers, and a high resistance layer. Stacked contacts are supported. The process is for 5 volt applications. PiP (poly2 over poly) capacitors (950 aF/μm^2) are available but not used for this research. This is a planarized process which does add some degree of difficulty into the design and post-fabrication processing which will be discussed. In

addition to this issue, the circuit die to be fabricated are 3mm x 3mm x 500μm which poses several problems. These and other issues will be discussed as the processing techniques already discussed are applied to the MOSIS die. Trial experiments were performed on 2.2mm x 2.2mm x 500μm die to gain some insight into the post-processing steps on MOSIS die and to workout some critical issues involved with these steps.

3.2.1 Photolithography

As previously mentioned lithography is the most expensive, complex, and critical process in mainstream microelectronic fabrication. The very first step to be performed on MOSIS die will be photolithography and difficulties associated with photolithography become apparent. The post-processing flow will consist of deposition of biosensor electrodes followed by etching procedures to generate thermally isolated regions.

The first photolithography step that must be performed on the die is the spinning of PR. Normally on the wafer level when the PR is being spun across a large uniform surface such as a full wafer, uniformity of the PR layer across the wafer is not an issue. When dealing with individual MOSIS die, however, uniformity of the PR layer on the die surface is a crucial requirement. As discussed previously, small nonuniformities in the PR layer can result in fabrication faults. In the first experiments a die was attached to the surface of a wafer and patterning of PR was attempted. The wafer was placed on the spinner and PR was spun on and after the necessary steps, patterning in the mask aligner was attempted. Initial patterning yielded poor results and after investigation it was found that the PR layer was not uniform across the surface of the die. Due to the viscosity and surface tension of the liquid PR at the corners of the die, caused by the height of the die above the wafer, the PR was thicker at the four corners. As mentioned, patterning of the

PR was inconsistent and results were poor. This issue needed to be resolved in order to ensure repeatability and consistency when performing the post-processing photolithographic procedure. There are a couple of solutions to this problem, one is to use a spray-on type PR layer and the other is to design a die holder for post-processing steps that leaves the die surface level with the holder on the spinner.

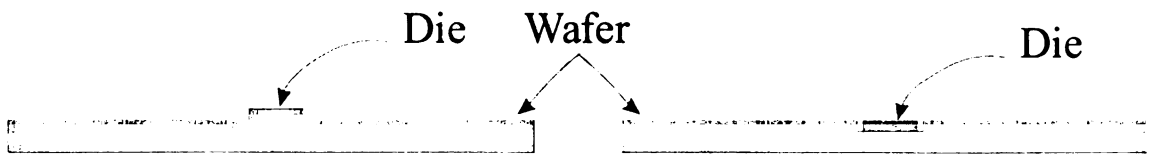

Figure 3-2: *(Left) Initial experimental setup with MOSIS die attached to a silicon wafer. (Right) Proposed die holder for MOSIS die. Consists of a recessed area in either aluminum or Teflon.*

The first option to use a spray-on PR was not chosen for a couple of reasons. First, a new process would have to be learned and perfected. Also, these chemicals can be quite expensive when compared to conventional photoresists. The option of creating a holder is chosen for this work. Preliminary experiments were conducted using die holders from MOSIS for PR application as seen in figure 3-3. This approach yielded much better uniformity across the die. There were still some issues, but they were greatly reduced and the PR could be effectively patterned with some consistency. When a specially designed die holder is made results should improve for the PR application. There are two die holders that will be made for this research one made out of glass for PR and material deposition steps and a holder made from Teflon for etching procedures.

Microfiche Masking

Masking procedures were performed on MOSIS die using transparency masks generated through microfiche technology [31, 32]. This masking technique can achieve

features in the 1-10μm range depending on the reduction ratio used when generating the microfiche. For this work a 25x reduction was performed onto film by *MicroGraphics Plus, Inc.* [33].

3.2.2 MOSIS Post-CMOS Metal Deposition

The next key processing technique will be to deposit the various metal layers needed for the formation of a working biosensor system. Electron beam evaporation will be used in this research for the deposition of the metal layers. One major reason this approach has been chosen is due to the die temperature. The die is held basically at room temperature so there will be no thermal complications to the fabricated die. Another reason electron beam evaporation has been chosen is because of the reproducibility of the deposition. The system being used is very precise and basically identical results can be achieved from one sample to the next. As previously mentioned, metal layers have been deposited on MOSIS die. The results showed patterns were successfully transferred to the die surface, but there were some inconsistencies in the transferred pattern. The results improve with better PR uniformity so the design and implementation of the mentioned die holders should yield acceptable results.

3.2.3 MOSIS Post-CMOS Etching

The final step in processing the MOSIS die will be to perform etching steps to generate thermally isolated structures for the temperature controlled array sites. There are two possibilities for generating thermal isolation regions on a MOSIS die. The first is a backside etching technique. This technique is attractive because of the relative ease of backside etching, the problems associated with a biosensor array containing electronics,

however, prevent this method from being practical. Figure 3-3 shows a very rudimentary block diagram of the frontside of the die if backside etching is to be implemented.

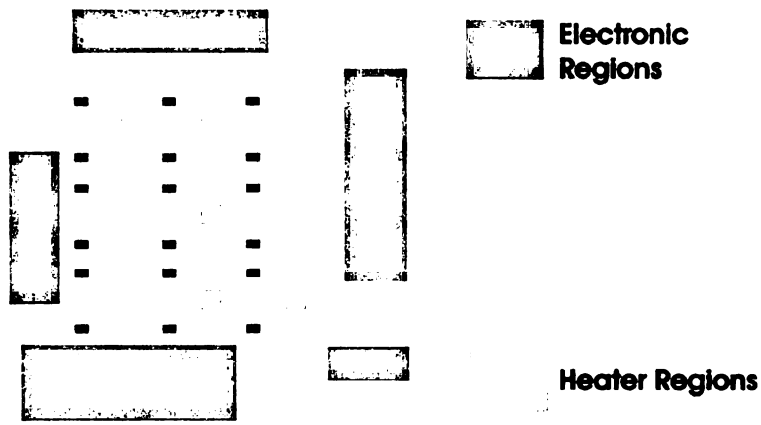

Figure 3-3: *Basic block diagram of biosensor chip for backside etch design. Light grey regions represent heater regions, dark grey regions represent areas where electronics are present.*

The first issue that comes to mind when considering a backside etch is the presence of electronics on the frontside of the die. Often with backside etching, the etching is allowed to proceed for a long period of time after which the etch stops on some layer, usually an insulator. This is a huge issue for this layout, since the etch would dissolve the necessary doped layers for transistor operation if it was allowed to continue until reaching the oxide at the wafer surface. A simple one step anisotropic etch would not work for this setup. In order for backside etching to work, a two step etch procedure would be required. The first etch would be a large, one region, timed bulk etch. This step would not require careful alignment and would need to be stopped at some depth below the surface where electronics in the array would not be affected. The second etch would be consist of nine separate anisotropic etch regions that would need to be masked by some layer that is not effected by the etchant and then aligned to features on the frontside to ensure proper isolation for each array site. This is a complex procedure that

would be very difficult to duplicate time and time again if it was even achievable with the fabrication facilities used for this work.

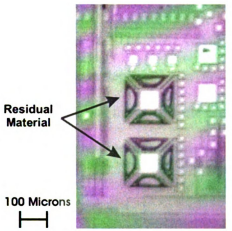

Figure 3-4: *Microstructure design with residuals left in designed openings to silicon substrate. Residuals are a result of the AMI planarized process.*

The second option is to use a frontside processing procedure utilizing process layers as the appropriate masking and sacrificial layers to realize a thermally isolated structure. Ideally we would like to have a series of layers that would leave an opening to the silicon surface after fabrication steps. Normally this would consist of drawing layers of Active, Contact, via layers, and Overglass. These layers generate the appropriate openings in passivation layers between the material layers in a CMOS process. This is exactly what happens in a CMOS process which has larger feature sizes. In these processes a conformal surface does not cause serious issues for device fabrication and their operation. However, when feature sizes are scaled down and more layers are added to a process it becomes very difficult to fabricate devices unless the surface is planar between all layers as they are generated. In a planarized process there are many more design rules that must be followed especially when dealing with interconnect layers such as contact or via. Because of these restrictions and the nature of the planarized process,

openings to the silicon substrate are not possible directly from the fabrication facility. Preliminary test procedures were created on past fabrication runs to test the validity of this hypothesis. As seen in the Figure 3-4, residues can clearly be seen in the regions that one might expect to contain bare silicon. The AMI C5F/N process does not allow for oversize contacts or vias so materials are deposited into these regions. This material can be etched away, but it is difficult to mask the rest of the die to protect against the harsh chemicals used to perform such an etch. Because of this problem, it is necessary to use a sacrificial micromachining technique which employs the existing layers in the AMI C5F/N process to expose the silicon surface. There are two possibilities here which both incorporate openings in the overglass layer from the fab house as a starting point after all electrode deposition has been carried out.

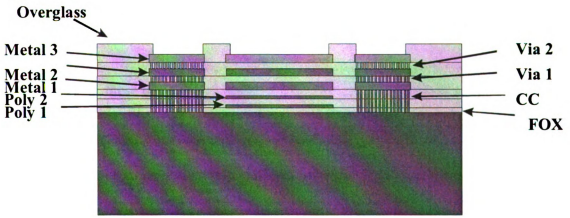

Figure 3-5: *First sacrificial etch design. Metal and via layers are used as sacrificial layers. In this design a post-CMOS metal etch will be performed to remove all metal and via layers leading to the silicon substrate, not protected by a PR mask layer. An additional oxide etch may be required to successfully reach the silicon surface, but this will be determined through experimental trial. After all layers are removed an anisotropic etch step will be performed to undercut and realize suspended MEMS structures.*

It is imperative that any post-processing for the addition of features, such as electrodes, other than the etched structures be carried out before the micromachining steps. After these steps have been carried out the entire wafer other than the areas to be sacrificed be protected by the PR masking layer. The sacrificial designs are illustrated in Figures 3-5 and 3-6.

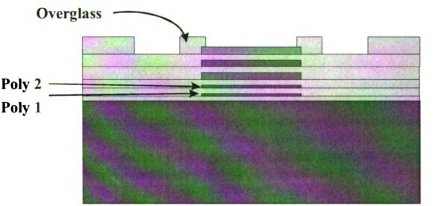

Figure 3-6: *Second sacrificial etch design. Insulating dielectric layers are used as sacrificial* ***layers. In this design, a post****-CMOS oxide etch will be performed to remove all dielectric layers leading to* ***the silicon substrate, not*** *protected by a PR mask layer. After all oxide is removed an anisotropic etch step will be performed to undercut and realize suspended MEMS structures.*

Both of these designs will utilize a PR masking layer, since it is not attacked by the aluminum or oxide etchant. The etching procedure in the case of sacrificial structure with metal layers and vias will consist of a two etch process. The first etch will be an aluminum etch. This will clear out the metal 3,2, and 1 layers. After the metal is etched away, there will be hundreds of contact holes down to the silicon, but there will also be oxide passivation layers with via and contact holes through them. So the second etch step will be to conduct an oxide etch to remove these layers and expose the silicon surface. Another option is to conduct an isotropic silicon etch as the second step. This will undercut the bottom passivation layer and should expose a large area of silicon that can

then be etched with an anisotropic etchant to create the suspended structure as proposed. The second option is to again mask the die in PR only exposing the overglass openings and then performing an oxide etch on the remaining oxide underneath the opening. This oxide layer is around 2μm thick so the etch will be a longer etch. After the silicon is exposed an anisotropic etch will be performed to realize the proposed MEMS suspended structure. This structure will provide excellent thermal isolation and support for the biosensor system.

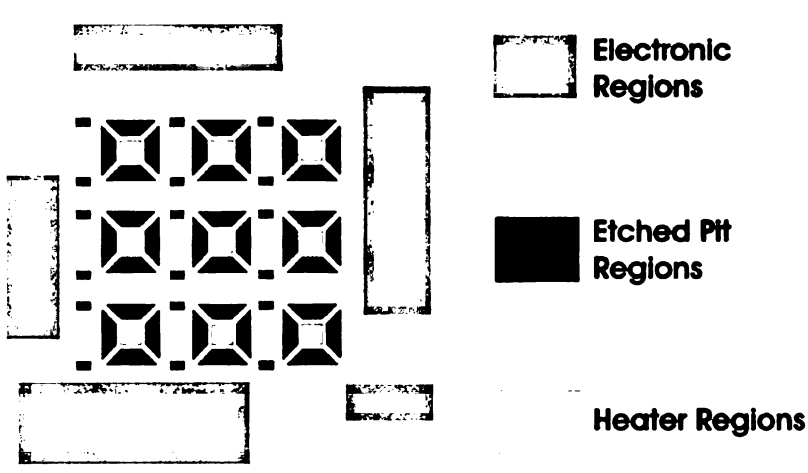

Figure 3-7: *Basic block diagram of biosensor chip for frontside sacrificial etch design. Light grey regions represent heater regions, dark grey regions represent areas where electronics are present.*

3.6 Simulation and Heat Transfer Analysis Results for Isolation Structures

The following subsections provide descriptions of thermal analysis as it applies to the estimation of heat transfer out of the system due to convection, choice of resistive heating element, and finally a comparison and discussion of the various thermal isolation schemes possible through this design. All thermal power estimations were made at the high end of the biosensor operational spectrum with the assumption that the maximum

temperature difference between the heater and ambient environment will be around 70°C. This was done so that a high end limit could be established for device characterization.

3.6.1 Validation of Heat Transfer Analysis

The first step in the analysis of the proposed structures is to verify the appropriate modeling for the thermal structures. This discussion will begin by showing the possible thermal structures available through this design.

Non-Thermally Isolated Structure

The first possible structure for the biosensor array site is the simplest one, no post-processing steps performed on the die, and its basic structure is shown in Figure 3-8 below.

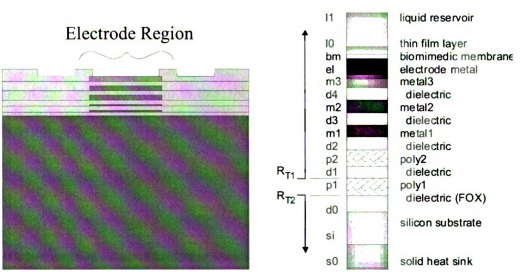

Figure 3-8 *(Left) Basic biosensor array site with no post-processing steps performed, (Right) layer structure taken into consideration for basic heat flow modeling.*

There are two possible environments in which this system can operate, air or water. Both of these systems operate under the assumption that there is a high thermal resistance above the heater due to the heat transfer characteristic of the thin film layer. However, there is very little thermal resistance below the heating element due to the high

conductivity of the silicon layer. This structure offers low thermal isolation, however the chip can be operated with minimum post-processing. The downsides to this approach are limited operational range and thermal contamination to surrounding array sites. These issues will be discussed in subsequent sections.

Thermally Isolated Structures

Several other structures are possible in this design with varying degrees of post-processing steps and each of these structures introduces thermal isolation into the design. Each thermal isolation variation stems from the suspended island as seen on the right. The suspended island is one of the most basic and widely utilized MEMS structures. Quite often this design shows up in thermal isolation and heating applications. This structure was decided upon due to ease of fabrication and wide use in the MEMS arena.

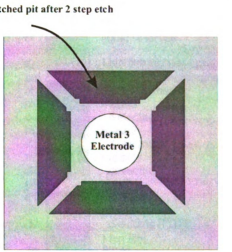

Figure 3-9: *Suspended Island Structure.*

Basic Suspended Island

The most basic and easily fabricated structure for thermal isolation is the suspended island structure. There are two operational possibilities for this structure; operation in air or in water. Figure 3.9 shows the situation where the microsystem is immersed and operated in an aqueous environment. This is the most likely structure and operating environment for biosensor applications. There is also the possibility of operating this structure in air, however this situation would only be used for little more than verification of functionality for the heating and temperature sensing array. The

structure is exactly as shown in Figure 3-10, except the water is replaced with air. In both instances, operation in air or water, this structure provides high thermal isolation and allows for a wide operational range.

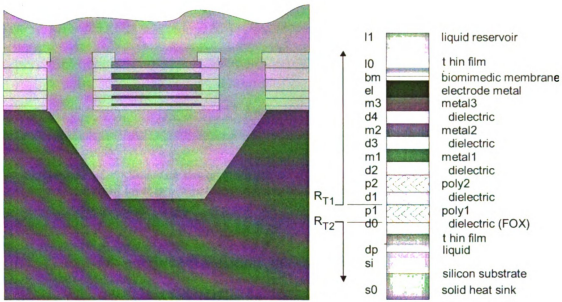

Figure 3-10: *(Left) Cross-section of basic biosensor array site with etch release steps performed and water above and below the heating element. (Right) layer structure taken into consideration for basic heat flow modeling.*

Sealed Cavity

Another thermal isolation design possible with the suspended island as a base for fabrication in the sealed cavity design. This structure is generated via standard low temperature, conformal oxide deposition after the heater region has been undercut. The steps involved in generating this structure are more advanced, which is a negative for this structure. There are again two operational possibilities for this structure; operation in air or in water, however the cavity below will always consist of air. Figure 3.11 shows the situation where the microsystem is operated in air. There is also the possibility of operating this structure in an aqueous environment, which would be used in biosensor applications.

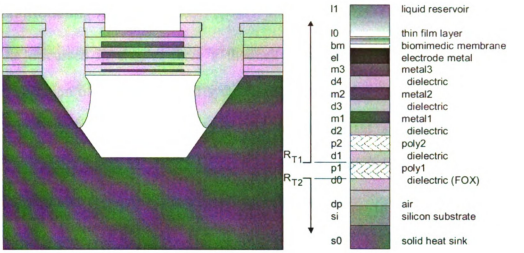

Figure 3-11: *(Left) Sealed air cavity biosensor array site with etch release and fill steps performed, (Right) layer structure taken into consideration for basic heat flow modeling.*

Etched Pit Filled with Insulator

The final envisioned variation on the suspended island structure involves releasing the structure and the filling the pit region with a spin on dielectric using basic fabrication techniques. The cross-section of this structure is shown below

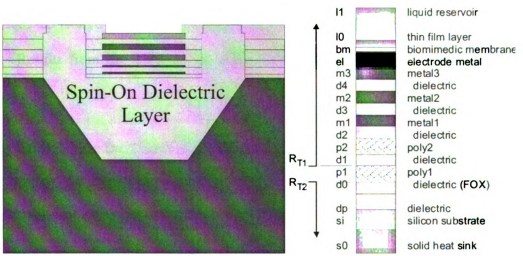

Figure 3-12: *(Left) Basic biosensor array site with etch release and fill steps performed, (Right) layer structure taken into consideration for basic heat flow modeling.*

Thermal Modeling Approach

As discussed in chapter three a thermally equivalent circuit can be used to estimate operation of the Joule heated system. In all of the structures proposed above, both thermally and non-thermally isolated, one thing is constant, a fluid/solid interface where heat transfer due to natural convection is occurring. The fluid can either be air or water as shown above. There are two equations which can be utilized in determining this coefficient; Eq. 2-24 and Eq. 2-25. It is important that an accurate estimate is found for this parameter to provide a decent prediction of the system's operation, since this layer is the largest thermal barrier in all cases. Simulations were run on each structural variation for each equation and then the results were compared to comparable structures and MEMS systems in literature. Through experimental trial it is found that Eq. 2-25 provides a more accurate estimate of the heat transfer coefficient for our heating situation due to the agreement between the expected operational results and other works. For this reason Eq. 2-25 is used when determining the heat transfer coefficient for analysis in this section. Results from Eq. 2-24 can be observed for all structures in the tables of the Appendix.

3.6.2 Resistor Value for Heating Element

This design incorporates several resistor values for the polysilicon heating element. These values were chosen before proper heat transfer analysis could be carried out to give a better idea of an appropriate resistor value. The values of 340Ω, 1.05kΩ, and 2.6kΩ were chosen due to the 100micron square size constraints and these are comparable to values in literature. In determining which resistor value is the most appropriate, the peak output power dissipated from the heater resistor must be determined

for this process. The maximum power a resistor can dissipate is given by $P=V^2/R$. The maximum voltage that can be used for this AMI process is 10V without causing damage to the metal supply lines, therefore the maximum power can easily be determined for each of the resistor values.

Table 2: *Maximum Allowable Power Dissipated Across Heater Element.*

	340 Ω Heater	1.05 kΩ Heater	2.6 kΩ Heater
Power dissipated at 10V peak voltage	294 mW	95.2 mW	38.5 mW

In order to determine how these values fit into the analysis of the system, the heating of the structure with the worst thermal isolation is used to determine the maximum needed power to heat to the peak temperature of 70°C. Table 3 shows results for this simulation which was carried out in Spice.

Table 3: *Current required to provide sufficient Joule heating effects from polysilicon heating element in water without thermally isolated MEMS structure. Voltage levels formatted as bold are too high for AMI process.*

Heater Structure with Water Above and No Isolation Below			
Power Scenario	**340 Ω Resistor Estimated Power and Voltage Level for 70° Temperature Change**	**1050 Ω Resistor Estimated Power and Voltage Level for 70° Temperature Change**	**2600 Ω Resistor Estimated Power and Current Level for 70° Temperature Change**
Spice Thermal Modeling using Eq. 2-25	232.8 mW 8.897 V	232.8 mW ***15.6 V***	232.8 mW ***24.6 V***

From these simulations it is clear that the only heater value that is suitable across all structural possibilities while still maintaining the maximum temperature is the 300Ω resistor. The other resistor values are suitable for structures that provide thermal isolation, however the 340Ω heater is used for all testing and characterization purposes.

The values for all structures for all heater resistive values can be found in table form in the Appendix.

3.6.3 Simulation Results and Comparison for Possible Structures

The structure of choice for this work is one that can provide sufficient i^2R heating, provide appropriate thermal isolation, and is also easy to fabricate. Table 4 provides a breakdown of each structure and its operational characteristics including fabrication complexity.

Table 4: *Operational comparison of various structures operated at 70 ℃.*

340 Ω Heating Element at 70°C	Power Required	Voltage Level	Current Level	Processing Complexity
Non-isolated structure in air	200.6 mW	8.26 V	24.3 mA	Low No masking required
Non-isolated structure in water	232.8 mW	8.897 V	26.2 mA	Low No masking required
Suspended island structure in water	13.73 mW	2.16 V	6.35 mA	Medium 1 Masking step required
Suspended island structure in air	303.7 μW	0.321 V	0.944 mA	Medium 1 Masking step required
Sealed air cavity structure in air	303.7 μW	0.321 V	0.944 mA	High Multiple masking and etching steps
Sealed air cavity structure in water	7.07 mW	1.55 V	4.56 mA	High Multiple masking and etching steps

The following graph shows data for the structures in graphical form including the level of thermal isolation provided when compared to the structure with the best thermal isolation.

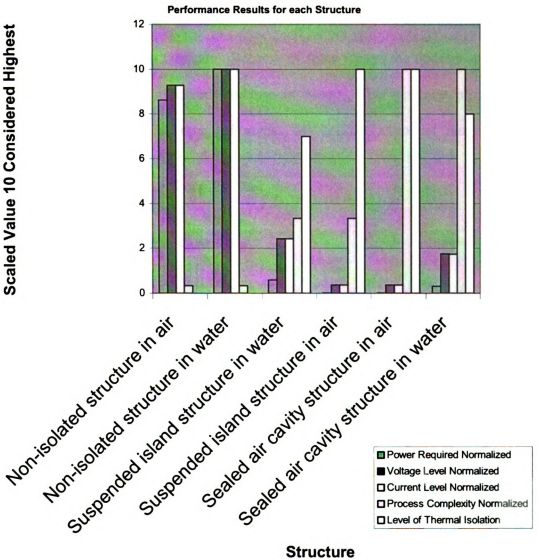

Figure 3-13: *Comparison of various structures. Y-axis is a 1-10 scale for the particular value of interest, 10 being a maximum value. X-axis composed of various structures. Values are normalized to values of 0-10 based on maximum value for category from Table 4. Structures with low power characteristics, low process complexity, and high thermal isolation are the most desired structures.*

Figure 3-13 shows that the best isolation is provided by the structures with air above and below, however these structures are not feasible for a biosensor since they need an aqueous environment and will only prove useful for operational testing. The structures, which are immersed in water, show the best performance results overall are for the isolated structure with the sealed air cavity. There is a tradeoff for this structure, in that it is very difficult to fabricate. Because of these factors the optimal structure for biosensors is the suspended island structure in water. This structure provides high thermal isolation, it can be operated across the entire operational range, and the fabrication process is basic.

Chapter 4: Biosensor Array Microsystem

An array for biosensor applications has been designed. The biosensor array consists of a 3x3 array of elements. Each array site has individual temperature sensing and heating capabilities. The block diagram for this chip design is shown in Figure 4-1, below.

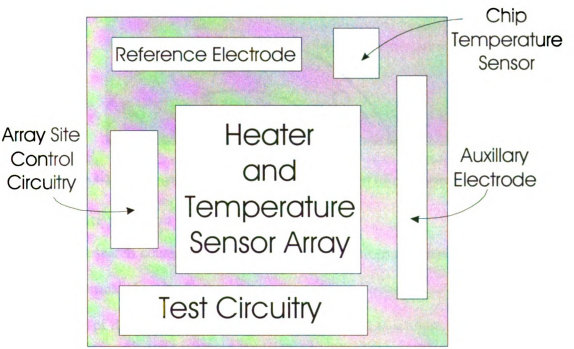

Figure 4-1: *Basic block diagram of MEMS biosensor chip design*

The necessary control circuitry for the array consists of row and column decoders and signal buffers. This and other circuitry will be the major focus of this chapter. The design principals and simulations will be covered.

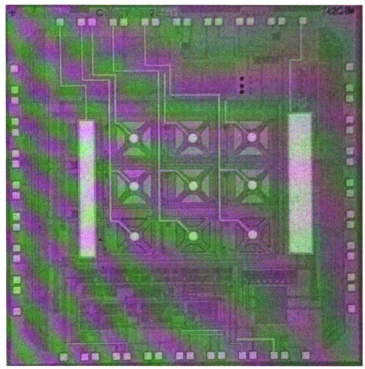

Figure 4-2: *Photograph of fabricated circuit die prior to MEMS fabrication procedures*

4.1 Array Site Selection Circuitry

This research consists of an array of elements for the purpose of multi element testing and thermal characterization. Anytime an array of elements is used there needs to be some kind of decoding in order to select the array site of interest. In this design the decoder used is a NOR type decoder as seen in Figure 4.3. The operation of this circuit is straight forward. There are two control bits, S0 and S1, which determine which bit line will be activated. The row and column decoders are identical in this design and both use the above circuit. The only input combination for any of the NOR gates that will yield a high output is 00. Therefore depending on the input signals, only one bit line can be logic high at any time. The operation of the decoder is given in Table 5.

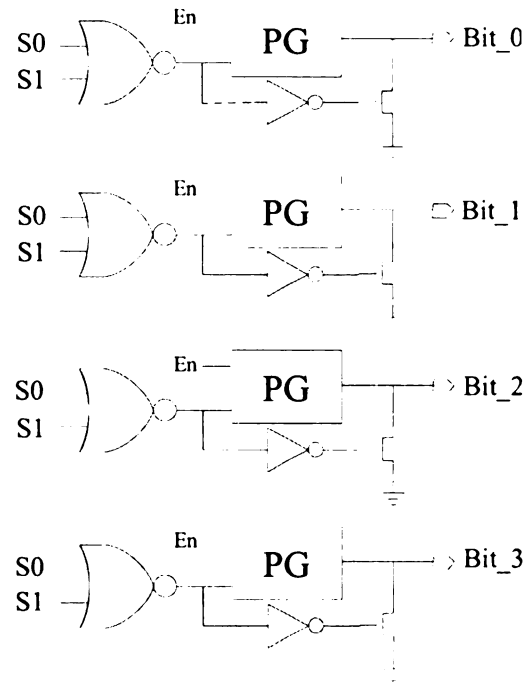

Figure 4-3: *Schematic of NOR decoder used in array selection circuit design.*

Table 5: *Bit line selection for column and row decoders.*

Selection Bit Input (S0 S1)	Bit Line Activated
00	Bit_0
01	Bit_1
10	Bit_2
11	Bit_3

As seen in Figure 4-3, each bit line is equipped with a transmission gate followed by a discharge resistor. The transmission gate is controlled by an enable bit. This is simply present so that the array as a whole can be turned on or off. The ground connected transistor is present to discharge the bit line immediately when it is no longer active. Due to the large loads on the bit lines, there is a longer delay in the response of the bit lines that could cause errors in array operation.

There are two main blocks which utilize this row and column decoding scheme; the heater array and temperature sensing array. Each of these blocks has its own decoding network with select bits independent of the other network. This feature is to not only keep one block's operation completely independent of the other, but also to allow for testing of thermal isolation by checking if there is thermal leakage form one array site to adjacent sites. One other thing to note is the presence of four bit line for the rows and columns, yet we are using a 3x3 array. There was not sufficient chip area available to generate a 4x4 array so the array dimensions were brought down. Due to this factor, row bit_0 and column bit_3 are not connected to any active circuitry in the system.

4.2 Heater Array

A key feature of the design is the ability to incorporate heating into each array site. There are two main advantages to this feature. First, the lifetime of the biosensors is extended. Secondly, the sensors are more robust. The heaters are simple polysilicon resistors of varying sizes that will experience joule heating due to the power across the resistor. This is a common technique used in numerous research for heating MEMS and circuit designs [34-38]. Polysilicon heaters have been designed using a serpentine type of design in several sizes. The amount of current through each heating element is basically limited by the Maximum allowed Vdd for the AMI process. This voltage is 5 volts, however a voltage of 10 volts may be safely used due to the direct connection to the voltage source with wide supply lines. However, larger voltages may cause the metal lines to degrade over time. There are several heater iterations that have been designed for the array sites. All of the resistive poly heaters cover the same chip area, 100μm x 100μm, yet they do differ in resistive values. The purpose of this is to determine what

resistive value will yield the best heating results and controllability given our process and thermal operation range for the biosensors. Four resistive values, 195Ω, 300Ω, 1.05kΩ, and 2.6kΩ, have been implemented into the 9x9 array. These values coincide with values used in prior research of polysilicon heaters. The following table shows the results from circuit simulations for the maximum current through each heater for 5V and 10V.

Table 6: *Current levels through heater resistors through Spice circuit simulation.*

Resistive Value	Current at 5V Supply	Current at 10V Supply
195 Ω	19.23 mA	38.46 mA
340 Ω	12.69 mA	25.38 mA
1.05 kΩ	4.56 mA	9.12 mA
2.6 kΩ	1.89 mA	3.78 mA

These current levels are also in line with those reported in research for achieving joule heating effects for temperatures up to 180°C for systems that provide sufficient thermal isolation. The temperature range we will be working in is roughly 0-100°C, so there should be no major issues with achieving the desired response from the heating elements under heating conditions with sufficient thermal isolation. This becomes apparent when looking at the heat transfer analysis for each of the proposed structures as laid out in Chapter 3. It is also seen that for the situation where there is no thermal isolation, a wide operational temperature range may not be possible with the restrictions placed on the current levels due to voltage limitations for the AMI process used for device fabrication. The approximations made through basic heat transfer analysis will need to be verified through testing of the polysilicon heating system.

4.3 Temperature Sensing Network

The ability to accurately measure the ambient temperature as well as the temperature at each array site is key to proper operation and calibration of the system. There are several main components that will allow these goals to be achieved from a design standpoint. The design and operation of the resistive bridge circuit for temperature sensing at the array sites, the temperature sensor array sites, and the basic ambient sensor will be discussed.

4.3.1 Resistive Bridge Network

A Wheatstone bridge is used for detecting the small variations in the resistive value for the temperature sensor resistor. The Wheatstone bridge circuit basically consists of two voltage dividers with matched resistors. The bridge configuration designed for this chip is shown in the Figure 4-4.

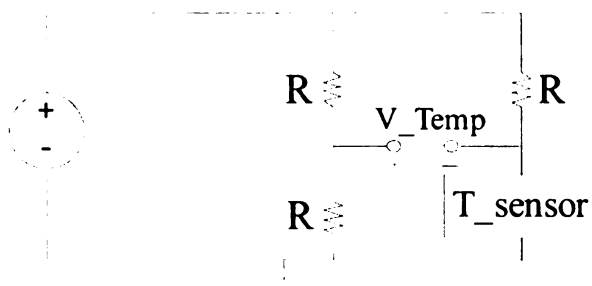

Figure 4-4: *Bridge configuration for temperature sensing network of MEMS system*

The bridge circuit operation is quite straight forward. A control voltage is applied to the circuit which will establish a voltage differential which is defined by the two voltage dividers. In this system, all resistors are matched on the layout and, other than the temperature sensor resistor which is located at an array site, all resistors are very close on chip to ensure device matching. The first voltage divider in the middle of the circuit is governed by the following:

$$V_{OUT_1} = V_{IN}\left(\frac{R}{R+R}\right) = \frac{V_{IN}}{2} \qquad \textbf{Eq. 4-1}$$

Since the resistors are matched this is the behavior we expect from the circuit. The second voltage divider is a bit different. The resistors are also matched, however one of these resistors is being used as a temperature sensor. This changes the circuit because the temperature sensor is located directly above a heating element and is at a temperature different from the background temperature of the rest of the chip. The resistive value of the temperature sensor will be $R + \Delta R_T$, where ΔR_T is given by the following equation:

$$\Delta R = \alpha_p R \Delta T$$

where α_p is the TCR of the polysilicon temperature sensor resistor as described in 3.4.4. Using this relationship we have an equation for the second voltage divider given by,

$$V_{OUT_2} = V_{IN}\left(\frac{R+\Delta R}{2R+\Delta R}\right) \qquad \textbf{Eq. 4-2}$$

If there is no difference in temperature the temperature sensor will have a ΔR of zero so the output voltage will simplify to Eq. 4-1. The voltage of interest in the bridge circuit, to determine if there is any temperature difference is the difference between V_{OUT_1} and V_{OUT_2}. The output voltage, V_temp given in Eq. 4-2, will correspond to a temperature difference on the temperature sensor resistor.

$$V\_temp = \left(\frac{-\Delta R_T}{2(2R+\Delta R_T)}\right) \qquad \textbf{Eq. 4-3}$$

Ideally, with no heating and the chip at some constant temperature, this output voltage would be zero. In order to achieve this, however, all resistors would have to be perfectly matched and interconnect resistances would also need to be matched. At first glance this

equation may seem useless, however when we combine and rearrange the above equations, the result is:

$$\Delta T = \frac{4V\_temp}{-\alpha_p\left(V_{IN} + 2V\_temp\right)} \qquad \textbf{Eq. 4-4}$$

This is an important relationship since the temperature at the temperature sensor can be found given α_p is known. The TCR will be found by characterizing the change in resistance of a temperature sensor resistor over a wide temperature range in a highly controlled temperature environment. ΔT is the difference in temperature between the reference temperature at which the chip is held and the temperature at the heated array site which is connected to the bridge circuit. In order to ensure accuracy in the temperature readings, careful derivations of the resistance and TCR must be made. Also, the changes in resistance will be small relative to the overall resistor value so the V_temp must be amplified to ensure small changes in temperature will accurately be recorded.

4.3.2 Temperature Array Sites

Each array site in this design has a temperature sensor with the sole purpose of measuring the temperature at the array site relative to the background temperature. The temperature sensing operation of the resistors is based on the TCR of the material as previously described. This is a common technique used in many commercial temperature sensing devices. However, a material such as platinum is usually used for the temperature sensing resistor. Polysilicon is used in this research due to the availability of the material in the chosen fabrication process and the close proximity of the layer with respect to the heating layer. Polysilicon temperature sensors have been designed using a

serpentine type of design as with the heaters. Contrary to the operation of the heating elements, self heating of the temperature sensing resistor would be detrimental to the accuracy of temperature measurements. These effects cannot be completely eliminated, however they can be kept at a negligible level. The amount of current through each heating element must be kept very small in order to achieve basically no self-heating and there are two basic techniques which can be employed to do this. The first is to make the resistive value of the temperature sensing resistor large. Due to Ohm's Law the current will be reduced. The voltage driving the bridge readout circuit can also be reduced to minimize the current levels. Since the voltage difference due to temperature will be amplified when performing temperature measurements, reducing the drive voltage should not pose any major operation issues. Again careful testing and characterization of the readout process will be required to find the optimum readout condition. The variable that was designed and cannot be changed is the nominal value of the temperature sensing and bridge circuit resistors. These resistors were all designed with resistance values of 200 kΩ. The circuit schematic for a temperature sensing site is seen in Figure 4-5.

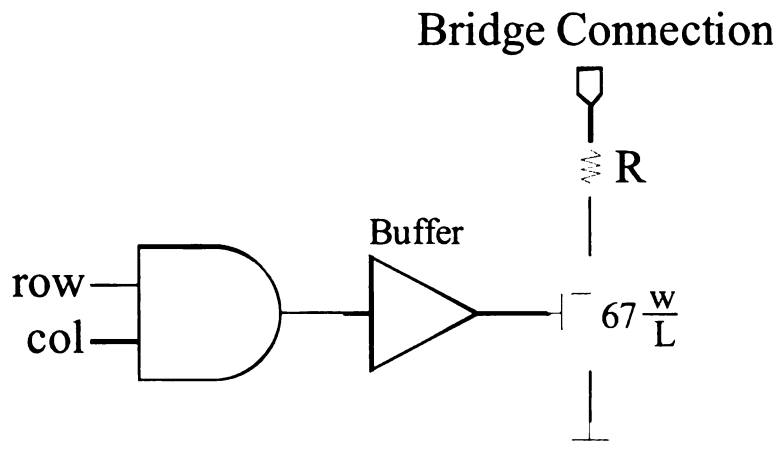

Figure 4-5: *Circuit schematic array temperature sensing site.*

The circuit is controlled by the described decoding scheme. The signal is then buffered to provide the necessary drive to the large transistor, which, when enabled, connects the chosen temperature sensor into the bridge circuit. There is only one bridge circuit for the entire array so the buffer must be capable of driving the large capacitance associated with the nine array sites basically in parallel. The response time of the array bridge combination circuit is on the order of microseconds which is more than adequate for proper operation of this feature. The reason behind the large transistor is to minimize the resistance of the MOSFET. In doing so the voltage dividers of the bridge circuit should be closely matched. Additional simulations on the expected operation of the temperature sensing network, given the TCR of the poly resistors is known.

4.4 Thermal Isolation Design

As previously discussed the need for thermal isolation in this design is key. The suspended structures will be generated by taking advantage of the fabrication layers available and performing post-CMOS fabrication micromachining techniques. It is imperative that extreme care is taken when performing these procedures to ensure circuit functionality and to minimize contamination to the system. These points and in depth coverage of the thermal isolation designs are covered in Chapters 2 and 3.

4.5 Ambient Temperature Sensor

There is also the need to know the background temperature of the environment for accurately performing the temperature measurements using the bridge circuit. Generation one of this design uses a simple polysilicon resistor as the temperature sensor. This approach is crude but will give a decent approximation of environmental temperature to ensure that the basic operation of the thermal array can be verified.

4.6 Three Electrode System

A traditional three electrode sensor system is possible through this design. Each array site contains a working electrode. There is one reference electrode and auxiliary electrode for the chip. Together all of these electrodes can be connected to a readout device and measurements such as cyclic voltammeter can be performed.

4.7 Results

Results were achieved for this design, in depth characterization was not done. A 3mm x 3mm circuit die was fabricated through the MOSIS foundry service using the AMI C5F/N 0.5 micron process. This chip contains all blocks as described in this document. Basic functionality was verified through laboratory simulation and experiment in several areas.

4.7.1 MEMS Post-Processing Results

MEMS post-processing steps were successfully achieved on the MOSIS die. Successful photolithographic and deposition steps were carried out as seen in Figure 4-6. The PR application was carried out using a standard PR spinner with the die in a holder as previously described. Patterns were then generated on the die surface using a Karl-Suss contact mask aligner. The masks used were standard CMOS masks. Metal deposition steps were carried out in an e-beam evaporation system.

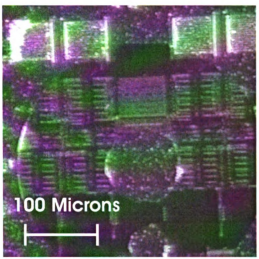

Figure 4-6: *Die photo of chromium patterns transferred onto MOSIS die through standard CMOS processing steps.*

The next and most important verification was to perform the necessary steps and show that the design for generation of suspended structures was successful. Suspended structures were generated ass seen in figure 4-7.

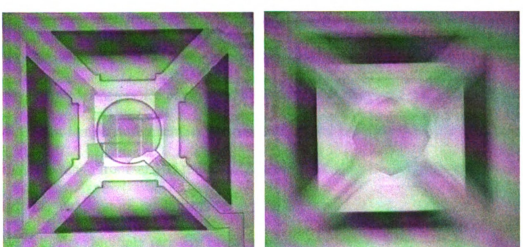

Figure 4-7: *(Left) Photograph of heater array site surface after etch and release steps. (Right) Same array site with focus on the bottom of the etched pit approximately4o microns in depth.*

The etching procedure consisted of an aluminum etch followed by an oxide etch to reach the silicon substrate. The final etching step was an anisotropic wet etch in

TMAH for almost 60 minutes. More experiments are required to perfect this procedure, but the design has been verified though trial.

4.7.2 Circuit Functionality

Functionality of the individual circuit blocks was not necessary for this work. The only circuitry that was tested was an individual array site for functionality. Using a probe station and a microscope, a voltage was applied across a 300Ω heater. The resistance across the temperature sensor resistor directly above the heating element was then monitored and showed an increase in resistance with temperature. This was the expected result, however more in depth testing will be required to fully characterize this MEMS device.

4.7.3 TCR of Polysilicon Temperature Sensor Resistor

The temperature coefficient of resistance for the polysilicon temperature sensor was determined using the methodology discussed in 2.5.4 above. In order to extract the necessary parameters accurately a highly controllable temperature environment was used. A Bryant temperature chamber was used to control the temperature of the environment over the range from –0.7°C to 65°C. A precise platinum temperature sensor was used to provide temperature readings from within the chamber while resistive measurements were made. Multiple resistive measurements were taken across the temperature range and the TCR was determined to be $4.803\times10^{-4}K^{-1}$. This result is agreement with values that are to be expected for doped polysilicon.

Chapter 5: Conclusions and Future Work

One of the main focuses of this work was to gain a clear understanding of the various structural layers in a CMOS fabrication process for the design and implementation of micromachined MEMS devices. A methodology for characterization of a process, using test structures and past designs, for fabrication of MEMS devices through a commercial planarized CMOS process was developed during the course of this research. Necessary processing steps were carried out to show validity in the design and the results indicate that this design was sound and thermally isolated suspended structures are possible in small feature size planarized processes. These structures have the potential to be used for thermal control of biosensor systems.

Another main focus of this research was the characterization and heat transfer analysis of the heated array sites. Analysis and simulation on a basic level have shown that proper device functionality is possible over the operating range of interest using the AMI process and its limitations. This will be beneficial in future work and shows how CMOS micromachining technology for a process with newer materials and applications can be applied for MEMS applications

5.1 Future Work

Future work on this design will consist of full characterization and testing of the thermal array. From heating to temperature sensing all aspects need to be tested so that improvements can be made to this design. Biosensor material will also be deposited onto the array sites to achieve a working sensor. Combining all findings from this work and

the testing procedure, necessary modifications will be made to the design and future versions of this MEMS system will be generated.

APPENDIX

Table 7: *Physical parameters and thermal properties for thermal modeling of suspended structure with water as liquid above and below using* [27].

Suspended Structure with Water as Liquid Above and Below					
Layer Name	**Material**	**Approximate Thickness**	**Thermal Conductivity, k $(W/m\cdot K°)$**	**Heat Transfer Coefficient due to Natural Convection, $\bar{h}$ *(calculated using Eq. 2-24)* $(W/m^2\cdot K°)$**	**Thermal Resistance R_T (K/W)**
Stagnant Layer (H_2O)	Water	N/A	N/A	2773.78	36,015
Metal 3 Electrode Region	Al, Cr, Au Combo	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Metal 2	Al	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Metal 1	Al	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Poly 2	Polysilicon	0.4 μm	25		1.6
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Poly 1	Polysilicon	Heater Region: N/A	Heater Region: N/A	N/A	N/A
Field Oxide	Silicon Dioxide	0.4 μm	1.15		34.78
Stagnant Layer (H_2O)	Water	N/A	N/A	2773.78	36,015

Table 8: *Physical parameters and thermal properties for thermal modeling of suspended structure with water as liquid above and below using* Eq. 2-25.

Suspended Structure with Water as Liquid Above and Below					
Layer Name	**Material**	**Approximate Thickness**	**Thermal Conductivity, *k*** $(W/m\cdot K°)$	**Heat Transfer Coefficient due to Natural Convection, $\bar{h}$ *(calculated using data from Eq. 2-25)*** $(W/m^2\cdot K°)$	**Thermal Resistance** R_T $\left(K/W\right)$
Stagnant Layer (H_2O)	Water	N/A	N/A	9913	10,088
Metal 3 Electrode Region	Al, Cr, Au Combo	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Metal 2	Al	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Metal 1	Al	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Poly 2	Polysilicon	0.4 μm	25		1.6
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Poly 1	Polysilicon	Heater Region: N/A	Heater Region: N/A	N/A	N/A
Field Oxide	Silicon Dioxide	0.4 μm	1.15		34.78
Stagnant Layer (H_2O)	Water	N/A	N/A	9913	10,088

Table 9: *Heat transfer results for multiple heater resistor values for suspended structure with water above and below.*

Suspended Structure with Water as Liquid Above and Below			
Power Scenario	**340 Ω Resistor Estimated Power and Current Level for 70° Temperature Change**	**1050 Ω Resistor Estimated Power and Current Level for 70° Temperature Change**	**2600 Ω Resistor Estimated Power and Current Level for 70° Temperature Change**
Eq. 2-12 Calculation using Eq. 2-24	3.866 mW 3.37 mA	3.866 mW 1.919 mA	3.866 mW 1.219 mA
Spice Thermal Modeling using Eq. 2-24	3.866 mW 3.37 mA	3.866 mW 1.919 mA	3.866 mW 1.219 mA
Eq. 2-12 Calculation Using Eq. 2-25	13.73 mW 6.35 mA	13.73 mW 3.617 mA	13.73 mW 2.30 mA
Spice Thermal Modeling using Eq. 2-25	13.73 mW 6.35 mA	13.73 mW 3.617 mA	13.73 mW 2.30 mA

Table 10: *Physical parameters and thermal properties for thermal modeling of suspended structure with air as liquid above and below using* [27].

Suspended Structure with Air as Liquid Above and Below					
Layer Name	**Material**	**Approximate Thickness**	**Thermal Conductivity, k $(W/m\cdot K°)$**	**Heat Transfer Coefficient due to Natural Convection, $\bar{h}$ *(calculated using Eq. 2-24)* $(W/m^2\cdot K°)$**	**Thermal Resistance R_T (K/W)**
Stagnant Layer (H_2O)	Water	N/A	N/A	40.16	2,490,075
Metal 3 Electrode Region	Al, Cr, Au Combo	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Metal 2	Al	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Metal 1	Al	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Poly 2	Polysilicon	0.4 μm	25		1.6
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Poly 1	Polysilicon	Heater Region: N/A	Heater Region: N/A	N/A	N/A
Field Oxide	Silicon Dioxide	0.4 μm	1.15		34.78
Stagnant Layer (H_2O)	Water	N/A	N/A	40.16	2,490,075

Table 11: *Physical parameters and thermal properties for thermal modeling of suspended structure with air as liquid above and below using* Eq. 2-25.

Suspended Structure with Air as Liquid Above and Below					
Layer Name	**Material**	**Approximate Thickness**	**Thermal Conductivity, k $(W/m\cdot K°)$**	**Heat Transfer Coefficient due to Natural Convection, $\bar{h}$ *(calculated using data from Eq. 2-25)* $(W/m^2\cdot K°)$**	**Thermal Resistance R_T (K/W)**
Stagnant Layer (H_2O)	Water	N/A	N/A	216.8	461,254
Metal 3 Electrode Region	Al, Cr, Au Combo	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Metal 2	Al	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Metal 1	Al	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Poly 2	Polysilicon	0.4 μm	25		1.6
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Poly 1	Polysilicon	Heater Region: N/A	Heater Region: N/A	N/A	N/A
Field Oxide	Silicon Dioxide	0.4 μm	1.15		34.78
Stagnant Layer (H_2O)	Water	N/A	N/A	216.8	461,254

Table 12: *Heat transfer results for multiple heater resistor values for suspended structure with air above and below.*

Suspended Structure with Air as Liquid Above and Below			
Power Scenario	**340 Ω Resistor Estimated Power and Current Level for 70° Temperature Change**	**1050 Ω Resistor Estimated Power and Current Level for 70° Temperature Change**	**2600 Ω Resistor Estimated Power and Current Level for 70° Temperature Change**
Eq. 2-12 Calculation using Eq. 2-24	1.43 μW 64.8 μA	1.43 μW 36.90 μA	1.43 μW 23.50 μA
Spice Thermal Modeling using Eq. 2-24	1.485 μW 66.1 μA	1.485 μW 37.60 μA	1.485 μW 23.90 μA
Eq. 2-12 Calculation Using Eq. 2-25	303.45 μW 0.945 mA	303.45 μW 0.538 mA	303.45 μW 0.342 mA
Spice Thermal Modeling using Eq. 2-25	303.7 μW 0.945 mA	303.7 μW 0.538 mA	303.7 μW 0.342 mA

Table 13: *Physical parameters and thermal properties for thermal modeling of suspended structure with water as above and air below using* [27].

Suspended Structure with Water Above and Air Below					
Layer Name	**Material**	**Approximate Thickness**	**Thermal Conductivity, k $(W/m\cdot K°)$**	**Heat Transfer Coefficient due to Natural Convection, $\bar{h}$ *(calculated using Eq. 2-24)* $(W/m^2\cdot K°)$**	**Thermal Resistance R_T (K/W)**
Stagnant Layer (H_2O)	Water	N/A	N/A	2773.78	36,015
Metal 3 Electrode Region	Al, Cr, Au Combo	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Metal 2	Al	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Metal 1	Al	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Poly 2	Polysilicon	0.4 μm	25		1.6
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Poly 1	Polysilicon	Heater Region: N/A	Heater Region: N/A	N/A	N/A
Field Oxide	Silicon Dioxide	0.4 μm	1.15		34.78
Stagnant Layer (Air)	Air	N/A	N/A	40.16	2,490,075

Table 14: *Physical parameters and thermal properties for thermal modeling of suspended structure with water as liquid above and air below using* Eq. 2-25.

Suspended Structure with Water Above and Air Below					
Layer Name	**Material**	**Approximate Thickness**	**Thermal Conductivity, k $(W/m\cdot K°)$**	**Heat Transfer Coefficient due to Natural Convection, $\bar{h}$ *(calculated using data from Eq. 2-25)* $(W/m^2\cdot K°)$**	**Thermal Resistance R_T (K/W)**
Stagnant Layer (H_2O)	Water	N/A	N/A	9913	10,088
Metal 3 Electrode Region	Al, Cr, Au Combo	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Metal 2	Al	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Metal 1	Al	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Poly 2	Polysilicon	0.4 μm	25		1.6
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Poly 1	Polysilicon	Heater Region: N/A	Heater Region: N/A	N/A	N/A
Field Oxide	Silicon Dioxide	0.4 μm	1.15		34.78
Stagnant Layer (Air)	Air	N/A	N/A	216.8	461,254

Table 15: *Heat transfer results for multiple heater resistor values for suspended structure with water above and air below.*

Suspended Structure with Water Above and Air Below			
Power Scenario	**340 Ω Resistor Estimated Power and Current Level for 70° Temperature Change**	**1050 Ω Resistor Estimated Power and Current Level for 70° Temperature Change**	**2600 Ω Resistor Estimated Power and Current Level for 70° Temperature Change**
Eq. 2-12 Calculation using Eq. 2-24	1.93 mW 2.38 mA	1.93 mW 1.356 mA	1.93 mW 0.862 mA
Spice Thermal Modeling using Eq. 2-24	1.936 mW 2.38 mA	1.936 mW 1.356 mA	1.936 mW 0.862 mA
Eq. 2-12 Calculation Using Eq. 2-25	6.97 mW 4.53 mA	6.97 mW 2.58 mA	6.97 mW 1.64 mA
Spice Thermal Modeling using Eq. 2-25	7.07 mW 4.56 mA	7.07 mW 2.59 mA	7.07 mW 1.65 mA

Table 16: *Physical parameters and thermal properties for thermal modeling of structure with water as liquid above and no thermal isolation below using* [27].

Heater Structure with Water Above and No Isolation Below					
Layer Name	**Material**	**Approximate Thickness**	**Thermal Conductivity, k $(W/m\cdot K°)$**	**Heat Transfer Coefficient due to Natural Convection, $\bar{h}$ *(calculated using Eq. 2-24)* $(W/m^2\cdot K°)$**	**Thermal Resistance R_T $\left(K/W\right)$**
Stagnant Layer (H_2O)	Water	N/A	N/A	2773.78	36,015
Metal 3 Electrode Region	Al, Cr, Au Combo	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Metal 2	Al	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Metal 1	Al	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Poly 2	Polysilicon	0.4 μm	25		1.6
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Poly 1	Polysilicon	Heater Region: N/A	Heater Region: N/A	N/A	N/A
Field Oxide	Silicon Dioxide	0.4 μm	1.15		34.78
Silicon Substrate	Silicon	500 μm	148		337.8

Table 17: *Physical parameters and thermal properties for thermal modeling of structure with water as liquid above and no thermal isolation below using* Eq. 2-25.

Heater Structure with Water Above and No Isolation Below					
Layer Name	**Material**	**Approximate Thickness**	**Thermal Conductivity, k $(W/m\cdot K°)$**	**Heat Transfer Coefficient due to Natural Convection, $\bar{h}$ *(calculated using data from Eq. 2-25)* $(W/m^2\cdot K°)$**	**Thermal Resistance R_T (K/W)**
Stagnant Layer (H_2O)	Water	N/A	N/A	9913	10,088
Metal 3 Electrode Region	Al, Cr, Au Combo	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Metal 2	Al	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Metal 1	Al	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Poly 2	Polysilicon	0.4 μm	25		1.6
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Poly 1	Polysilicon	Heater Region: N/A	Heater Region: N/A	N/A	N/A
Field Oxide	Silicon Dioxide	0.4 μm	1.15		34.78
Silicon Substrate	Silicon	500 μm	148		337.8

Table 18: *Heat transfer results for multiple heater resistor values for structure with water above and no thermal isolation below.*

Heater Structure with Water Above and No Isolation Below			
Power Scenario	**340 Ω Resistor Estimated Power and Current Level for 70° Temperature Change**	**1050 Ω Resistor Estimated Power and Current Level for 70° Temperature Change**	**2600 Ω Resistor Estimated Power and Current Level for 70° Temperature Change**
Power Calculation for Spice Thermal Modeling using Eq. 2-24	209.8 mW 24.80 mA	209.8 mW 14.13 mA	209.8 mW 8.98 mA
Power Calculation for Spice Thermal Modeling using Eq. 2-25	232.8 mW 26.2 mA	232.8 mW 14.89 mA	232.8 mW 9.46 Ma

Table 19: *Physical parameters and thermal properties for thermal modeling of structure with air as liquid above and no thermal isolation below using* [27].

Heater Structure with Air Above and No Isolation Below					
Layer Name	**Material**	**Approximate Thickness**	**Thermal Conductivity, k $(W/m\cdot K°)$**	**Heat Transfer Coefficient due to Natural Convection, $\bar{h}$ *(calculated using Eq. 2-24)* $(W/m^2\cdot K°)$**	**Thermal Resistance R_T (K/W)**
Stagnant Layer (H_2O)	Water	N/A	N/A	40.16	2,490,075
Metal 3 Electrode Region	Al, Cr, Au Combo	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Metal 2	Al	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Metal 1	Al	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Poly 2	Polysilicon	0.4 μm	25		1.6
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Poly 1	Polysilicon	Heater Region: N/A	Heater Region: N/A	N/A	N/A
Field Oxide	Silicon Dioxide	0.4 μm	1.15		34.78
Silicon Substrate	Silicon	500 μm	148		337.8

Table 20: *Physical parameters and thermal properties for thermal modeling of structure with air as liquid above and no thermal isolation below using* Eq. 2-25.

Heater Structure with Air Above and No Isolation Below					
Layer Name	**Material**	**Approximate Thickness**	**Thermal Conductivity, *k*** $(W/m\cdot K°)$	**Heat Transfer Coefficient due to Natural Convection, $\bar{h}$ *(calculated using data from Eq. 2-25)*** $(W/m^2\cdot K°)$	**Thermal Resistance** R_T $\left(K/W\right)$
Stagnant Layer (H_2O)	Water	N/A	N/A	216.8	461,157
Metal 3 Electrode Region	Al, Cr, Au Combo	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Metal 2	Al	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Metal 1	Al	0.7 μm	180		0.389
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Poly 2	Polysilicon	0.4 μm	25		1.6
Oxide	Silicon Dioxide	0.5 μm	1.15		43.48
Poly 1	Polysilicon	Heater Region: N/A	Heater Region: N/A	N/A	N/A
Field Oxide	Silicon Dioxide	0.4 μm	1.15		34.78
Silicon Substrate	Silicon	500 μm	148		337.8

Table 21: *Heat transfer results for multiple heater resistor values for structure with air above and no thermal isolation below.*

Heater Structure with Air Above and No Isolation Below			
Power Scenario	**340 Ω Resistor Estimated Power and Current Level for 70° Temperature Change**	**1050 Ω Resistor Estimated Power and Current Level for 70° Temperature Change**	**2600 Ω Resistor Estimated Power and Current Level for 70° Temperature Change**
Power Calculation for Spice Thermal Modeling using Eq. 2-24	200 mW 24.3 mA	200 mW 13.8 mA	200 mW 8.77 mA
Power Calculation for Spice Thermal Modeling using Eq. 2-25	200.6 mW 24.3 mA	200.6 mW 13.82 mA	200.6 mW 8.78 mA

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