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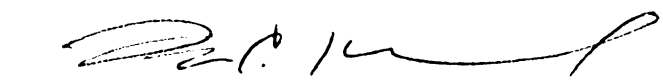

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By

Michael John O'Farrell

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ABSTRACT

LOW LEVEL RADIO FREQUENCY CONTROL OF RIA SUPERCONDUCTING CAVITIES

By

Michael John O'Farrell

High velocity superconducting radio frequency (SRF) cavity designs at MSU, for the proposed Rare Isotope Accelerator (RIA), have an unloaded Q on the order 10e9. RIA applications use low beam currents resulting in loaded Qs of the order 10e7. In order to maintain stable fields, RF power requirements will be dominated by control of the cavity fields in the presence of low-level perturbations on the cavity.

A field programmable gate array (FPGA) based, low level radio frequency (LLRF) controller has been designed to compensate for perturbations on accelerating cavities, maintaining driving amplitude and phase levels, on a point-by-point basis, thereby stabilizing cavity fields. Originally designed at Lawrence Berkeley National Labs, for use at another accelerator project, the controller was adapted for use on RIA prototype medium beta cavities. Supporting circuitry was designed and built for cavity controls, and its performance was measured.

The emphasis of this thesis concerns the understanding of the digital control loop, its implementation at the National Superconducting Cyclotron Laboratory for RIA, and an analysis of the controller's performance.

This thesis is for my beautiful bride Ivana,

Ethan and Madeline for whom I returned to school.

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I must acknowledge Leo Kempel for his help and instruction over the last three years, making my time at MSU more interesting. I thank Dr. Kempel for getting me in at one of the coolest workplaces a graduate student could wish for.

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CHAPTER 1

Introduction

Increased pressure from the physics community for further research into nuclear particle physics has created a demand for high velocity, high energy accelerators. Superconducting cavities are capable of supporting high fields with low power losses due to the reduced surface resistances. The quality factor (Q) of a cavity is indicative of how high the fields can be achieved. Higher Q-factors represent stronger internal fields, but with a more narrow bandwidth. In the presence of perturbations, maintaining amplitude and phase control, or field stability becomes increasingly difficult with very high Q-factors, because of the associated narrow bandwidths. Superconducting Radio Frequency (SRF) cavity prototypes, designed and built at Michigan State University (MSU) for the proposed Rare Isotope Accelerator (RIA), have obtained an unloaded Q of 10^{10}. Loaded Q-factors of magnitude 10^7 are anticipated during beam operation. Maintaining amplitude and phase of such high Q cavities is only possible with digital controllers capable of compensating for disturbances as they occur.

A low level radio frequency (LLRF) controller, designed for Spallation Neutron Source (SNS), and built at Lawrence Berkeley National Labs (LBNL) in collaboration with Los Alamos Labs, was acquired by the National Superconducting Cyclotron Laboratory (NSCL) for phase and amplitude control of SRF cavities. This thesis is based on the implementation and operation of the controller. In order to understand the operation of the controller, a background review of electromagnetics, particle physics, control systems, signal processing, digital signal processing and VHDL is presented. Verification of the output data is performed and finally a user manual is attached as an appendix.

Table 1.1. Numbers and types of cavities in RIA linac.

Type	Six-cell elliptical			Triple spoke	
β_{opt}	0.49	0.63	0.83	0.50	0.62
Number of cavities	68	64	32	42	96
Total	164			138	
Temperature($K°$)	2			4.2	

In 2004, the Department of Energy deemed (RIA) as a high priority for further research in physics. Beam physicists search for new isotopes of known elements by colliding high energy beams of specific ions onto targets of known materials, creating isotopes which are used for the advancement of materials and medicine. RIA would extend research to isotopes of heavier elements [1].

The NSCL SRF research group designed a proposal for RIA which specified the ability to accelerate ions up to uranium to 400MeV/u to high energy, with a final beam power of 400kW [3]. The number of cavities in the linear accelerator (linac) are listed in table 1.1.

To achieve required beam powers, the linac is designed with various group of cavities. Each group is designed to allow for an increase in velocity of the beam, an example of each group is shown in figure 1.1. The β_{opt} is the optimum design $\beta = \frac{v}{c}$, where v is the velocity of the beam and c is the speed of light.

The elliptical accelerator cavity is a microwave resonator whose shape is derived from a pillbox shaped resonator. Radio frequency (RF) power is transmitted to the cavity and is coupled to the particle beam. Electric field and magnetic field patterns in the cavity are illustrated in figure 1.2, where the electric fields are normal to the metal surface, and peak electric fields occur along the center axis of the cavity. Magnetic fields patterns are azimuthal, where the peak magnetic field occur on the equator of the cavity and are zero along the center axis of the cavity [2].

The beam is accelerated through the center of the cavity axis. As the power supplied is time varying, the particles are delivered in bunches, coinciding with a harmonic of the cav-

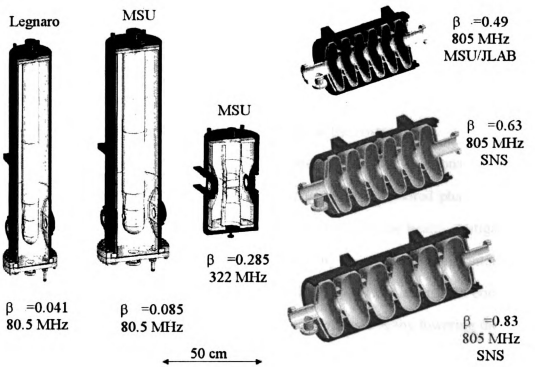

Figure 1.1. Illustration of various linac cavities.

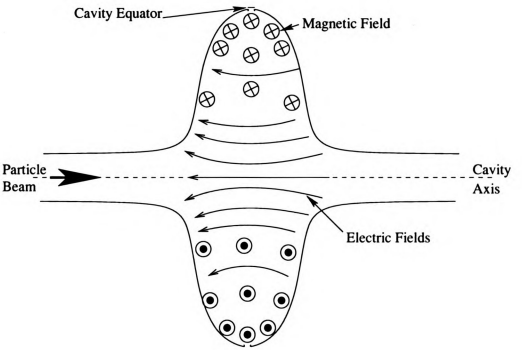

Figure 1.2. Cavity dynamics.

ity frequency. The bunches must be timed correctly to obtain the maximum acceleration. The cavity RF drive signal must be held in phase with all cavities in the linac to accelerate the beam for the length of the accelerator. If for example, the phase was offset by 180°, the beam would undergo deceleration. For beam stability all cavities are synchronized to a reference signal to accelerate the bunches of particles at the correct time.

A disturbance imposed on the cavity is observed by a change in resonant frequency. A change in resonant frequency also produces a change to the desired phase, since resonant cavities are highly dispersive, causing timing issues for the beam. Mitigating the disturbances is partially accomplished mechanically, by reducing environmental effects, and stiffening the cavity structurally to lessen sensitivity to perturbations. To compensate for disturbances, cavities have been over-coupled with power thereby lowering the Q_{ext} of the cavity. Which in turn lowers the operational Q_{ext} during beam loading. By lowering the Q_{ext}, the cavity with beam load or loaded Q (Q_l) also decreases and the effective system bandwidth increases. An increased bandwidth effectively decreases the effects of phase and amplitude offsets due to a change in resonance.

Heavier ion acceleration calls for lighter beam currents which have considerably less effect on the loaded Q of the cavity. For the low RIA beam current, it is necessary to control the resonant frequency to obtain the desired higher fields while not requiring vast amounts of power. A properly controlled system will result in significant power savings during accelerator operation [4].

The LBNL controller is called the 'low level radio frequency' (LLRF) controller, because it is capable of compensating for microphonics as well as low level disturbances, occurring within the system bandwidth. The LLRF controller is a combination of analog signal distribution and more importantly digital design. The system is based on a Xilinx Spartan XC2S150, [12] Field Programmable Gate Array (FPGA) processor whose realtime parallel processing allows for point-by-point compensation of the RF drive signal, based on information from the cavity.

To supply the controller with the appropriate signal levels, a support chassis was designed and built to support the LLRF. Testing of the cavities with the controller was completed to determine the level of performance with a five cell copper mock up cavity at room temperature.

The controller is a simple Proportional Integrator control loop, but its implementation is complex. Code for the system, largely undocumented, is written in Verilog, a hardware description language, and high level C. The lack of documentation, manual, direction, and experience at NSCL has been the impetus for this thesis to evolve into a reference manual to be used for further research.

Chapter 2 is background information for the understanding of the relationship between cavity dynamics, beam physics, and the cavity de-tuning that is a result of disturbances on the cavity. A circuit model of the cavity is used to simplify some of the equations leading to the relationship of cavity input power and the limit of controllable de-tuning.

Chapter 3 describes the source of disturbances and methods previously used to mitigate these perturbations. Discussion leads to a digital method of controlling the cavity and how it may be implemented into a linac.

Background information regarding analog and digital demodulation of signals is presented in Chapter 4. A method of capturing signal information in the rectangular form of complex real and imaginary values (I and Q), is explained, in addition to analog to digital conversion (ADC). The method of signal capture for digital processing in the controller is established and discussed. Chapter 5 concerns a detailed breakdown of the digital control aspect of compensation, along with some of the additional functionality.

Chapter 6 discusses the method of distributing and supplying analog signals at the correct level to the ADC for proper signal capture. A support chassis was designed and built to house components and supply the appropriate level signals to the LLRF. The relationship between graphical user interfaces, supporting computers and the LLRF are explained in Chapter 7.

The analysis of the support chassis design and the accuracy of the LLRF is substantiated in Chapter 8, where experimental results confirm that the LLRF output values are accurate to specific levels.

CHAPTER 2

Cavity Parameters

2.1 Description of the SRF

Superconducting RF cavities are used for producing the high cavity fields necessary for charged particle acceleration. An introduction to SRF cavities will be presented, and modeled, deriving the parameters to explain the behavior of low-level radio frequency (LLRF) disturbances imposed on the cavity. The goal is to present background material describing the problem and outlining the factors necessary to achieve the ultimate goal of controlling the cavity fields. The properties of a superconducting cavity are such that very high fields are obtained with relatively low power input. The unloaded Quality factor (Q_u) for the MSU $\beta = 0.47$ RIA prototype cavity is measured to be 10^{10}, while operating at 805 MHz at $2°K$. The resulting bandwidth is less than 1Hz (see equation (2.3)). This very narrow bandwidth means the cavity is sensitive to small vibrations or disturbances which physically change its shape, presenting the difficulty in maintaining the constant amplitude and phase required for a linear accelerator.

A linear accelerator or linac, is comprised of many cavities arranged for a straight line of flight beam of particles. The initial cavities are designed for a low β_o. In this $\beta_o = \frac{v}{c}$, where v is the speed of the particles and c is the speed of light. As the beam proceeds along the linac, the particles are accelerated and the β of the cavity msut be increased. To minimize costs, cavities are grouped in similar velocities, such that each group can accommodate a range of velocities. Identical cavities designed for an optimum β (β_{opt}) is used for the entire group. The frequency of each group of cavities must be a harmonic of

the initial cavity frequency. For example, MSU's RIA design includes an initial frequency in the low β cavities of 80.5 MHz, middle β cavities of 322 MHz and several high β groups of cavities operating at 805 MHz. These are the fourth and tenth harmonic frequencies of the initial 80.5 MHz.

Each cavity driving the linac must be synchronized to a common reference frequency so the beam is accelerated efficiently. The RF signal in the cavity is phase locked to this reference signal. The reference signal is designed to ensure the synchronization of the phase of all other cavities in the linac. Regardless of all exterior conditions, the cavity fields must ultimately remain phase locked and amplitude stable relative to a reference signal to maintain beam stability.

2.2 Circuit Model of the Cavity

In order to show the effect of disturbances on the cavity, it is necessary to introduce variables that are relevant to the system. A useful means of describing the system is through a model of a resonant circuit. The overall system may be broken down into the cavity itself, a current source driving the system, a transmission line to feed the cavity, and a load. Figure 2.1 represents a schematic of a 6-cell cavity set-up. The load is the beam passing through the cavity absorbing energy as it is accelerated.

The current source is driven from an amplifier. The transmission line and the RF coupler feeding the resonator are designed to provide the power to the cavity. Since the cavity is overcoupled, to maintain stability, a circulator is necessary to ensure reflected signals do not saturate or damage the amplifier. The amplifier, circulator, coupler, and lines are lumped together as the Norton equivalent of the external current source consisting of the current source I_s and the shunt impedance Z_{ext}.

Resonating circuits or cavities act as a band pass filter and have a bode plot similar to that presented in figure 2.3. The ratio of the output signal relative to the input signal

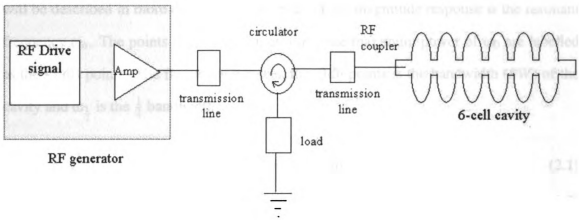

Figure 2.1. General system set-up for a single 6-cell elliptical cavity.

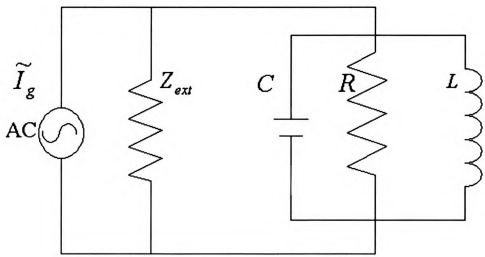

Figure 2.2. Equivalent RLC circuit

is called the transfer function, and is presented in terms of the its magnitude and phase response. Here we can identify some fundamental aspects of the cavity response, which will be described in more detail later. The peak of the magnitude response is the resonant frequency ω_o. The points at which we measure $\frac{1}{2}$ the maximum power of ω_0 are labelled as the -3 dB points. The frequency between the -3db points is the bandwidth (BW) of the cavity and $\omega_{\frac{1}{2}}$ is the $\frac{1}{2}$ bandwidth.

$$BW = \omega_2 - \omega_1 \tag{2.1}$$

$$= 2\omega_{\frac{1}{2}} \tag{2.2}$$

where ω_1 is the lower -3dB frequency and ω_2 is the higher -3dB frequency. In (2.2), an even symmetric function about the center frequency ω_o, is assumed.

The phase plot undergoes a 180 degree phase change over the frequency span of the resonator. Hence, the reactance of the circuit moves from an inductive circuit to a capacitive circuit through a frequency sweep, while the reactive components are equal at ω_0. As the impedance is complex off–resonance, there is a phase difference between the voltage and current. At ω_0 the relative phase difference is 0, while at the -3dB points the phase is either ± 45 degrees.

The quality factor, or Q, of the cavity or resonator is defined by the magnitude response.

$$Q = \frac{\omega_0}{BW} \tag{2.3}$$

More specific equations of Q will be defined later in the chapter.

It is important to recognize that the equivalent circuit of the cavity is a reasonable representation of the cavity within the bandwidth of the cavity. Outside the bandwidth, the model illustrated in figure 2.2 does not normally hold.

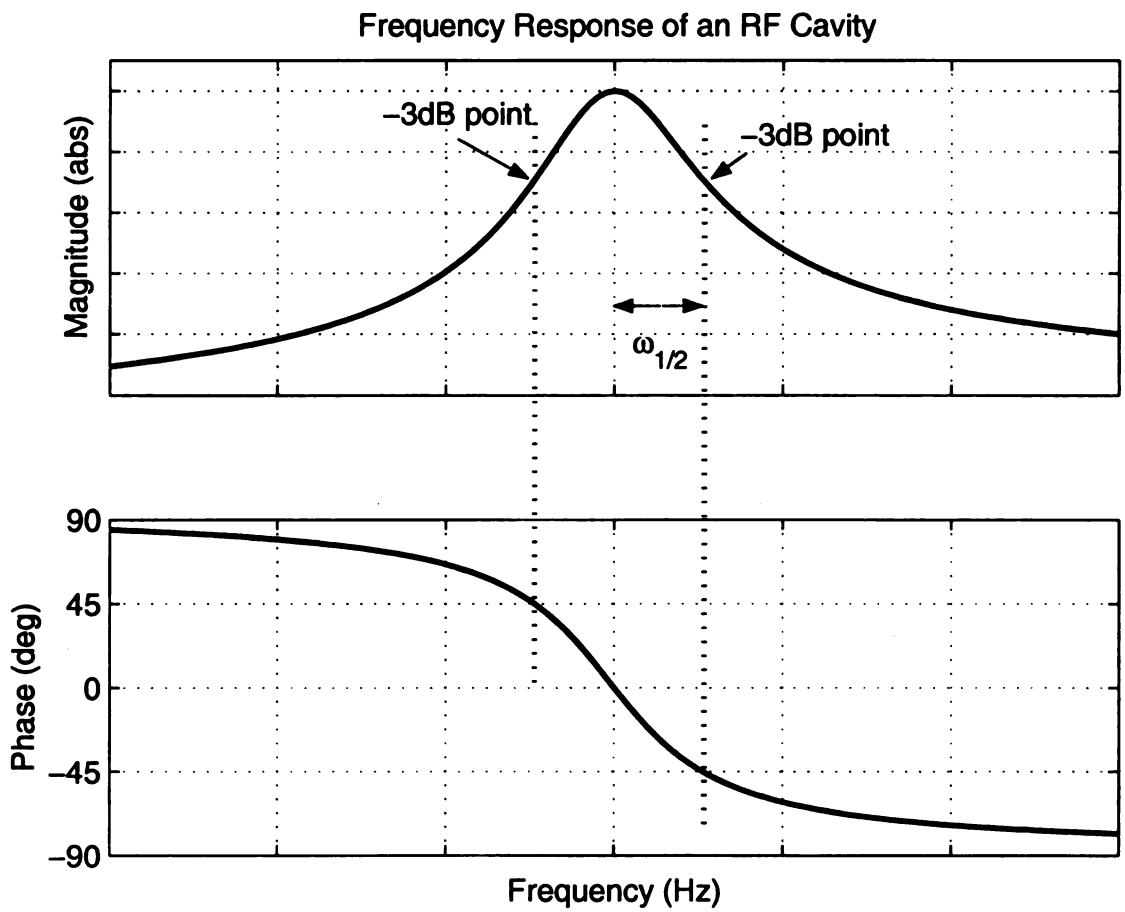

Figure 2.3. Bode Plots.

2.3 Resonator Description and Simplification

Referring to the cavity as a RLC circuit implies that we are looking at a form of resonator, the simplest of which is a pillbox. Due to the symmetry of a pillbox resonator we can define the coordinate system in cylindrical coordinates, where z is the axis of symmetry, while the theta (θ) and rho (ρ) components are symmetric about the z axis. For the pillbox, a TM_{010} mode is present.

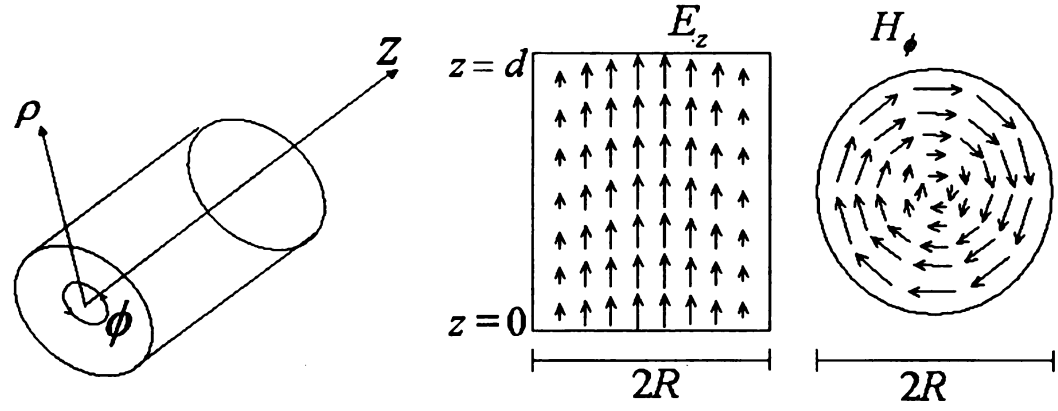

Figure 2.4. Cavity fields for TM_{010}.

A coupling probe induces fields in the cavity so that the electric field will propagate in the z direction. As the beam passes through the cavity in the z direction, it is accelerated by the electric field within the cavity, $E(z,t)$.

$$E(z,t,\phi) = E(z)\cos(\omega t + \phi) \tag{2.4}$$

where $\omega = 2\pi f$ of the RF frequency

The beam is made up of bunches or packets of charged particles, consisting of ions, electrons, or protons. $E(z,t)$ is time varying and therefore, for the beam to obtain maximum

possible acceleration in the correct direction, the bunches must pass through the cavity while the electric field is at its maximum or "on-crest" (point 1 in figure 2.5).

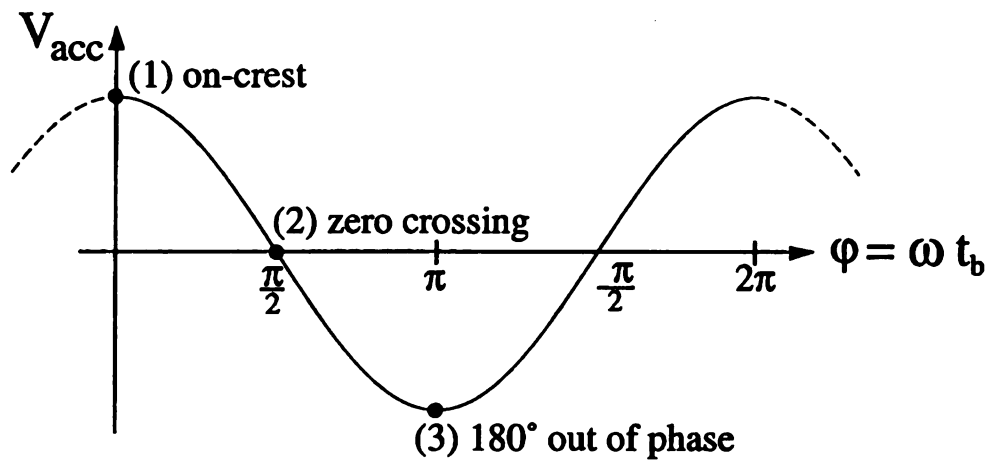

Figure 2.5. Timing of the bunch.

We can define the phase delay as

$$\psi = \omega t_b \tag{2.5}$$

where t_b is the particle injection time delay of the beam.

Figure 2.5 indicates that if the particles are injected with no delay, they are on crest. If the delay is $\frac{\pi}{2}$ (point 2 on figure 2.5), there is no acceleration, while if the delay is π the bunch will be decelerated (point 3 in figure 2.5).

2.4 Beam Dynamics

From beam dynamics, there is a desired value of phase offset to maintain or reduce the bunch size of each beam packet. A synchronous phase ϕ_s, from the peak or crest, allows

bunches to remain tightly grouped. Slower particles obtain more energy, faster particle obtain less energy so the bunch remains in tight formation. This is known as the *second Robinson's stability criterion.*

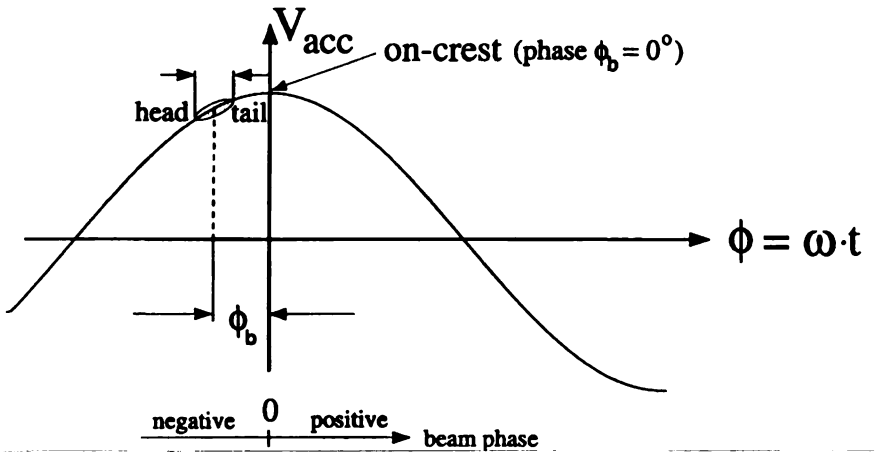

Figure 2.6. Phase, i. e. synchronous phase $\phi_s = \phi_b$.

An important consideration here is the intended phase delay of the beam or phase delay in the cavity fields. There are desired set-points for the phase in individual cavities to ensure that beam particles accelerate as a bunch correctly.

Additionally, in an ideal linac, each progressive cavity would have an increasing β to account for the increasing speed of the beam. Cavity designs are shaped to match the frequency to the velocity of the particles and are referred to in terms of their β. In reality it is less costly to design a single cavity with an optimum β or β_{opt} to operate at a harmonic of the initial β frequency. Within a range of cavities of mutual design, the beam velocity will be too slow for the first cavity, appropriate for the middle cavity and too fast for the last cavity. By adjusting the phase set-points, a cavity can accommodate the beam with the most appropriate electric field to accelerate the beam efficiently. The amplitude and phase set-points of the cavity fields, are critical in terms of accelerating the beam.

2.5 Derivation of the Quality Factor

In the circuit model of figure 2.2, the resonance of the RLC circuit is defined as the frequency at which the inductive and capacitive reactance's are equal. This is given in terms of inductance (L) and a capacitance (C) as

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{2.6}$$

The impedance of the parallel combination of inductor and capacitor at resonance is infinite, and all the generator current flows through the resistor (R) at this frequency. As noted earlier, as the cavity moves off resonance, either inductive or capacitive reactance exist in the circuit or cavity.

Comparing the circuit model to the cavity, the relationship of R in our model is relative to the resistive losses R on the walls of the cavity from surface currents induced by the electromagnetic fields. This value R is important in determining the power dissipated in the cavity. This is valuable in deriving the alternate definition of Q. In this case the unloaded Q or Q_u is defined as the ratio of stored energy (U), to energy (P_{cav}) lost in one rf cycle (T). Where

$$P_{cav} = \frac{V_p^2}{2R} \cdot T \tag{2.7}$$

For the optimum cavity design where the beam β includes the cavity β_o, the ideal transit time for the particles corresponds to 180° of phase accumulation. In this scenario the particles are accelerated during the total time while exposed to the electric fields. Also at β_o, $V_{acc} = V_{cav}$. The cavity potential is then

$$V_{cav} = \frac{2V_p}{\pi} \tag{2.8}$$

The accelerator community relates the cavity voltage to losses via R_{sh}, where $R_{sh} = 2R$;

hence,

$$P_{diss} = \frac{V_{cav}^2}{R_{sh}} \tag{2.9}$$

and

$$Q_u = \frac{\omega U}{P_{cav}} \tag{2.10}$$

The time average stored energy at resonance is defined as the peak electric or magnetic field energy stored in the system. Alternatively, the time average stored energy can be in the capacitor and inductor used in the model of figure 2.2.

$$U = \frac{1}{2}\mu_0 \int_V |\mathrm{H}|^2 d\mathrm{v} \tag{2.11}$$

$$U = \frac{1}{2} L I_p^2 \tag{2.12}$$

$$U = \frac{1}{2}\varepsilon_0 \int_V |\mathrm{E}|^2 d\mathrm{v} \tag{2.13}$$

$$U = \frac{1}{2} C V_p^2 \tag{2.14}$$

By definition, at resonance the stored energy in the capacitor and inductor are equal; hence,

$$U = \frac{1}{2} C V_p^2 = \frac{1}{2} L I_p^2$$

$$Q_u = \frac{\omega U}{P_{cav}}$$

$$Q_u = \frac{\omega \frac{1}{2} C V_p^2}{\frac{1}{2}\frac{V_p^2}{R}}$$

$$Q_u = \omega R C \tag{2.15}$$

From the circuit model, we derive this equation which will be used later to define the cavity tuning angle.

2.5.1 Additional Quality Factors of Interest

We have considered thus far the unloaded cavity; we can also derive the Q for other cavity conditions, such as when the beam passes through the cavity. We may do so by using the circuit model again, considering the external driving current $\hat{I}_g$, the external impedance z_{ext}, and a load. Our load is the beam passing through the cavity and represented by I_b. As the particles are accelerated they absorb energy from the cavity fields and must be represented by a load. The beam must be considered as part of the system, not as a simple resistive load but as a current load, due to the reactive components of the beam.

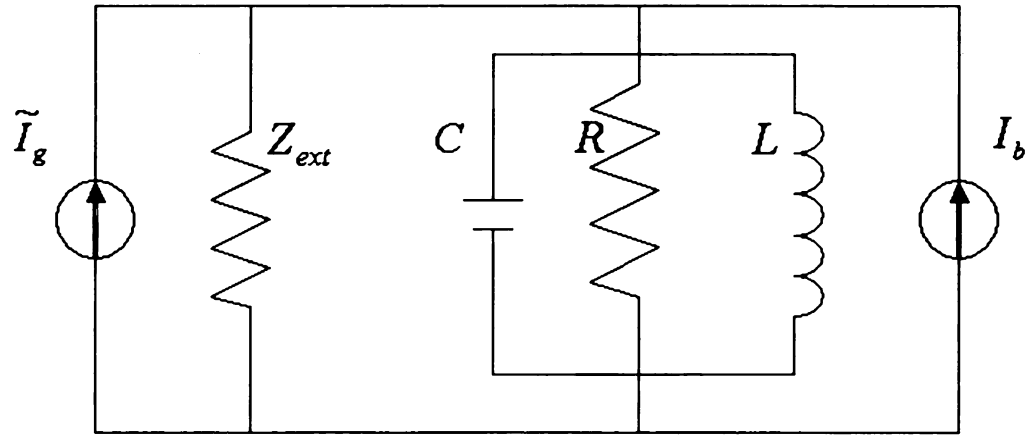

Figure 2.7. Equivalent RLC circuit with load.

The unloaded Q, as previously determined, was the ratio of stored energy to dissipated energy in the cavity. External Q (Q_{ext}) is the ratio of energy stored in the cavity relative to the power dissipated in external devices from the cavity. This is given by,

$$Q_{ext} = \frac{\omega U}{P_{ext}} \tag{2.16}$$

while the loaded Q, which is the Q of the cavity with a beam passing through it, is given by

$$Q_l = \frac{\omega U}{P_{tot}} \tag{2.17}$$

where

$$P_{tot} = P_{cav} + P_{ext} \tag{2.18}$$

The loaded Q may be calculated as

$$\frac{1}{Q_l} = \frac{1}{Q_o} + \frac{1}{Q_{ext}} \tag{2.19}$$

We can describe the beam, by its own effective Q. Here the beam quality factor (Q_b) can be described as the ratio of stored energy in the cavity compared to the power delivered to the beam.

$$Q_b = \frac{\omega U}{P_{beam}} \tag{2.20}$$

In general the $Q_{ext} \approx Q_l$. As Q_o is typically orders of magnitude larger, Q_{ext} dictates the Q_l. This is because most of the power lost in the system is to the power coupler, transferring RF power to the cavity. By increasing the coupling, or overcoupling the cavity with power, more power is lost in the coupler further reducing the Q_{ext} and Q_l. The lower Q_l broadens the bandwidth of the system making it less susceptible to amplitude and phase offset from shifting resonant frequencies.

2.6 Tuning Angle and Cavity Voltage Requirements

The circuit model in figure 2.7 considered the effective generator current I_g and the beam load as a current I_b. Both I_g and I_b are sinusoidal and of the same frequency. The phase

difference between these two currents is represented as θ in figure 2.8. The timing of beam injection relative to the reference signal synchronizing all the cavities can control this phase angle θ. If we combine the two parallel currents into a single source *I* and analyze the circuit we will determine the steady state solution of the cavity voltage. This combined current is given by

$$I = \tilde{I}_g + I_b \tag{2.21}$$

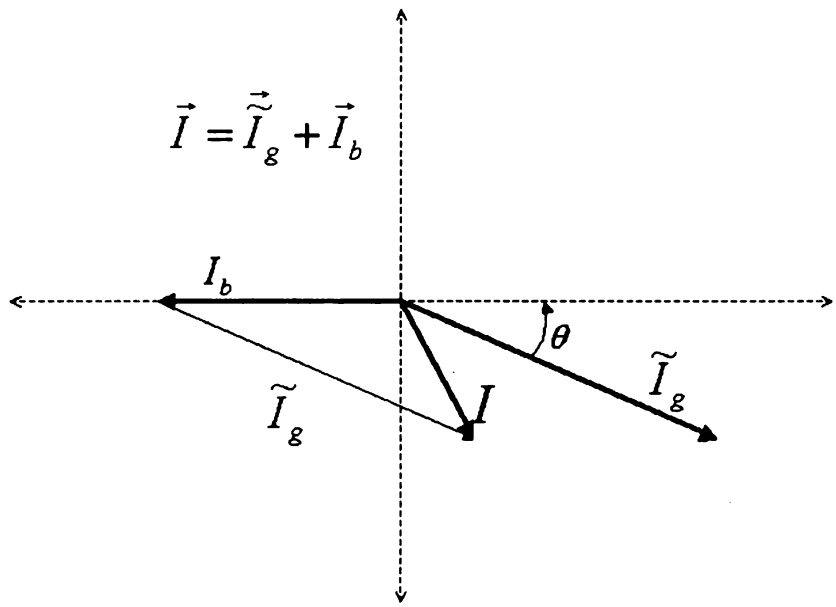

Figure 2.8. *I* representing generater and beam currents

Using Kirckoff's current law we know that

$$I = I_R + I_L + I_C \tag{2.22}$$

and

$$I = \frac{V_c}{R} + \frac{1}{L}\int_0^t V_c dt + \frac{C dV_c}{dt} \tag{2.23}$$

By differentiating both sides of (2.23), we find

$$\frac{dI}{dt} = \frac{1}{R}\frac{dV_c}{dt} + \frac{1}{L}V_c + \frac{Cd^2V_c}{dt^2} \tag{2.24}$$

and divide by C, we have

$$\frac{1}{C}\frac{dI}{dt} = \frac{1}{RC}\frac{dV_c}{dt} + \frac{1}{LC}V_c + \frac{d^2V_c}{dt^2} \tag{2.25}$$

This second-order differential equation represents the cavity voltage driven by the amplifier, accelerating the beam.

Let the applied current be

$$I = I_o sin(\omega t) \tag{2.26}$$

The steady state solution of the differential in (2.25) equation will be given by

$$V_{cav} = V_c \sin(\omega t + \psi) \tag{2.27}$$

Utilizing (2.26) and (2.27) in (2.25) and comparing both sides of the equation for $\sin(\omega t + \psi)$ as well as $\cos(\omega t + \psi)$, we can find the equations solution,

$$\tan\psi = R_l(\frac{1}{\omega L} - \omega C) \tag{2.28}$$

where the beam load included in R_l,

$$V_c = \frac{R_l I}{\sqrt{1+[R_l(\frac{1}{\omega L}-\omega C)]^2}} \tag{2.29}$$

The angle ψ is the phase angle between the generated current and the generated voltage, or between the beam current and beam voltage. This is known as the cavity-tuning angle.

$$\begin{aligned}
\tan\psi &= R_l\frac{C}{\omega}(\frac{1}{LC}-\omega^2) && (2.30)\\
&= \frac{R_l C}{\omega}(\omega_0^2-\omega^2) && (2.31)\\
&= \frac{R_l C}{\omega}[(\omega_0+\omega)(\omega_0-\omega)] && (2.32)\\
&\cong \frac{R_l C}{\omega}\cdot 2\omega\triangle\omega && (2.33)
\end{aligned}$$

Where $\triangle\omega$ is the difference between the driving frequency ω and the cavity frequency ω_o. If $\triangle\omega$ is small, than ψ may be used in the approximation (2.33).

Alternatively given (2.15)

$$\tan\psi = \frac{2Q_l\Delta\omega}{\omega} \tag{2.34}$$

Finally

$$\tan\psi \approx 2Q_l\frac{\Delta\omega}{\omega} = 2Q_l\frac{\Delta f}{f} \tag{2.35}$$

and

$$V_c \approx \frac{R_l I}{\sqrt{1+\tan^2\psi}} \tag{2.36}$$

Graphing this V_c versus frequency verifies the fundamental cavity responses mentioned earlier, as seen in figure 2.3. The bandwidth of the loaded system is noted by the points where the voltage drops to $\frac{1}{\sqrt{2}}$ of the voltage or the -3dB value of the maximum voltage, or the stored energy drops to $\frac{1}{2}$. The -3dB occurs when the angle is $\frac{\pi}{4}$ which equates to $\frac{1}{\sqrt{2}}R_l I$

when used in equation (2.36).

2.7 Controlling Bandwidth

Understanding the relationship of the various Q's (especially that of Q_b of the cavity to the bandwidth) is essential in designing the power requirements necessary to obtain and control the desired cavity fields. As mentioned earlier, very high Q factors relate to very narrow bandwidth and therefore a very sensitive environment. Any noise or low level disturbance will de-tune the resonant frequency. Once the ω_0 of the cavity does not agree with the RF drive frequency, which is governed by a reference signal throughout the linac, the cavity fields will drop in amplitude and will deviate from the desired phase set-point.

Existing high velocity accelerators have usually had high beam currents. The high beam current relates to a low Q_b. The low Q_b reduces the overall Q_l, which in turn increases the bandwidth of the cavity. Microphonic induced frequency variations become relatively insignificant to the loaded bandwidth, creating small amplitude variation in the system, and the majority of RF power provided is transferred to the beam. Disturbances in the form of microphonics have little effect on the phase and amplitude of the system when the $\Delta\omega$ is considerably less than the cavity bandwidth.

RIA has a low beam current and therefore has a high Q_b. The overall loaded Q_l of the system will remain very high, resulting in cavity field control dominating the power requirements in the presence of microphonic disturbances.

2.7.1 Calculate the Power Requirements for Detuning

With some form of amplitude and phase control, there is still a maximum amount of power that may be available to adjust for resonant frequency offset. Hence, the maximum amount of detuning possible can be calculated for a given amount of power generated.

RIA beam currents are designed to be relatively low at 0.328 mA. The amount of power

required to sustain the field in the cavities has been designed to be at a level where the delivered or coupled power level is twice that of the required beam loading power.

In deriving the equations to determine the control bandwidth, let P_{bd} be the beam design power and P_b be the power of the beam.

$$P_g = \frac{P_{bd}}{4}\left[\left(1+\frac{P_b}{P_{bd}}\right)^2 + 4\left(\frac{\delta\omega}{\Delta\Omega}\right)^2\right] \tag{2.37}$$

where

$$\Delta\Omega = BW = \frac{\omega_0}{Q_l} \tag{2.38}$$

$$Q_l = \frac{\omega U}{P_{bd}} \tag{2.39}$$

$$Q_b = \frac{\omega U}{P_b} \tag{2.40}$$

$$\frac{Q_l}{Q_b} = \frac{P_b}{P_{bd}} \tag{2.41}$$

$$Q_b = \frac{\omega_0}{BW_b} \tag{2.42}$$

$$\omega_0 = Q_b BW_b \tag{2.43}$$

$$BW = 2\omega_{\frac{1}{2}} \tag{2.44}$$

$$\omega_0 = 2Q_b\omega_{\frac{1}{2}b} \tag{2.45}$$

Using (2.41) and (2.39) in (2.37) and dividing by P_b, we get

$$\frac{P_g}{P_b} = \frac{P_{bd}}{4P_b}\left[\left(1+\frac{P_b}{P_{bd}}\right)^2 + 4\left(\frac{\delta\omega Q_l}{\omega_0}\right)^2\right] \tag{2.46}$$

Substituting (2.41) and (2.43) into (2.46)

$$\frac{P_g}{P_b} = \frac{Q_b}{4Q_l}\left[\left(1+\frac{Q_l}{Q_b}\right)^2 + 4\left(\frac{\delta\omega Q_l}{BW_b Q_b}\right)^2\right] \tag{2.47}$$

If we assume that

$$Q_{ext} \approx Q_l \tag{2.48}$$

then

$$\frac{P_g}{P_b} = \frac{Q_b}{4Q_l}\left[\left(1+\frac{Q_l}{Q_b}\right)^2 + \left(\frac{\delta\omega Q_l}{\omega_{\frac{1}{2}b}Q_b}\right)^2\right] \tag{2.49}$$

By rearranging (2.47) so that its derivative with respect to $\frac{Q_l}{Q_b}$ and evaluating it at 0, we find the maximum ratio of Q_{ext} to Q_b. Assuming the overall generator power to be twice the beam power, the maximum ratio of $\frac{Q_l}{Q_b}$ calculates to be 0.33. Using this in (2.47) to determine the maximum allowable detuning, to occur, while maintaining control of amplitude and phase, calculates to 5.68 of the beam BW from equation (2.42). The system can maintain control even if microphonics detunes the system 5.68 times the beam bandwidth, under these conditions.

2.8 Graphically Demonstrate Loss of Resonance

The left graph of figure 2.9 is the magnitude response of a cavity where the cavity resonance frequency (ω_{RF}) occurs at the peak voltage of the initial curve (line 1) at $t = 0$. The required voltage at resonance is indicated by a dot. Line 2 represents a shift in frequency due to some disturbance where the new resonant frequency is established at ω_o at time t_1. To compensate for the drop in voltage at the cavity resonance frequency due to the shift, an increase in power is necessary (line 3) to maintain the proper cavity fields at the resonant frequency ω_0.

Similarly, the phase plots on the right represent the shift in phase due to the disturbance represented by lines 1 to 2. Corresponding phase compensation is also necessary to bring

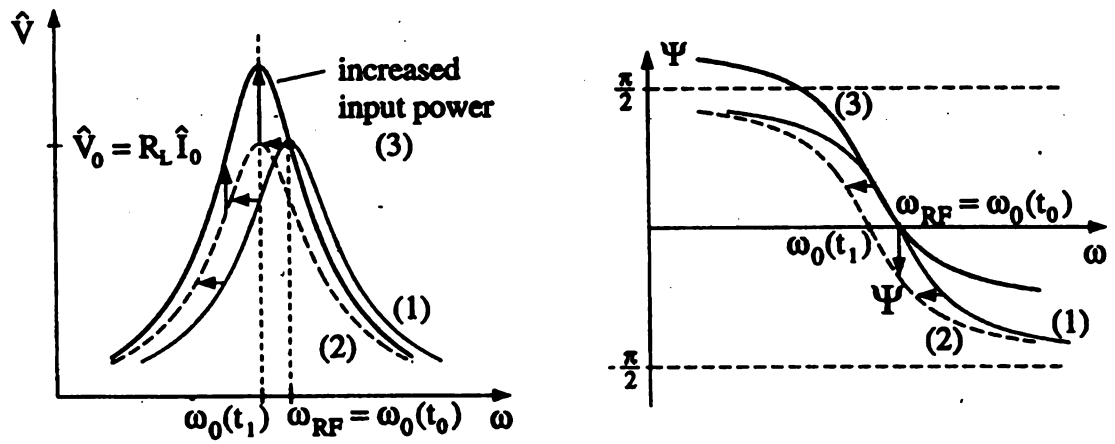

Figure 2.9. Effects of disturbance on resonant frequency.

the phase of the cavity back in line with the reference signal.

2.9 Conclusion

We have introduced a number of factors relative to Superconducting Radio Frequency cavity dynamics and have established the relationship between the cavity parameters, bandwidth and quality factors of the cavity. For more detailed review of cavity parameters and beam dynamics, the interested reader is referred to [2].

The Q factors of the cavity play a significant role in that the amount of over-coupling determines the loaded Q. The loaded Q dictates the performance of the cavity and its sensitivity to disturbances. Efficient beam acceleration is possible only if cavity fields are steady and phase locked to a reference signal synchronizing the entire linac. Ultimately, a form of control is necessary to regulate the phase and amplitude of the cavity fields in a manner such that the desired phase and amplitude may be established and maintained to a specific accuracy.

CHAPTER 3

Mitigation of Disturbances

3.1 Disturbances

With a background regarding cavity dynamics and an understanding of the control parameters of the cavity, the source of disturbances and methods of controlling them can now be described. There exists both mechanical and electrical methods of dealing with these disturbances. Mechanical methods mitigating dealing with disturbances are capable of reducing the level of disturbance to a workable range, but not eliminating them completely. This chapter describes general mechanical and electrical methods to virtually eliminate the disturbance.

Microphonics is the definition of low level disturbances which affect the cavity. In the case of the RIA high β cavities, which are the most sensitive cavities, it has been determined that most frequencies over 300 Hz may be neglected due to their insignificant effect on the cavity.

Microphonics are mechanical vibrations from the surrounding environment. The cavity is connected directly and indirectly to cryogenic lines, pumps, other plumbing, and to the building floor itself. Motors, equipment, even ground vibrations from road traffic may be considered sources of vibrations. There are a multitude of synchronous machines in our environment, vibrating at approximately 60 Hz and harmonics of 60Hz. As our environment is surrounded by sources of vibrations, managing the disturbances is critical to maintain stable cavity fields.

3.2 Mechanically Dealing with Disturbances

The simplest method of damping any vibrations would be to isolate and even remove the source of the vibrations permanently. Locating cavities in an isolated environment away from motors, traffic and other vibrating sources will help, but there are numerous connections that cannot be completely isolated. Cryogenic feed lines, necessary to maintain superconductivity, may be damped so as to reduce the vibration from pumps and motors, but can not be eliminated. Reducing the amount of physical vibration within proximity of the cavity will help reduce the amount of detuning.

Mechanically damping the vibrations is possible by stiffening parts of the cavity. By increasing the mechanical stiffness of the cavity by welding support struts, we increase the stiffness K matrix, thereby increasing the natural resonant frequency of the parts themselves. The forced response of the cavity due to a disturbance will be of a higher frequency, which may be out the susceptible range of problematic frequencies, or in the high β cavities $\omega_{dis} > 300$Hz.

The critical component for reducing vibrations in the cavity mechanically, is the tuner. A tuning arm connected directly to the SRF cavity, mechanically alters the length and shape of the cavity thereby changing the resonant frequency of the cavity. A piezoelectric actuator activated by a controller can be use as a means for compensating microphonic vibrations, by applying an equivalent disturbance with the reverse phase [8]. The reduction in mechanical vibration will bring down the disturbance to within the BW, so it may be controlled electrically. Additionally, it will reduce the RF power requirements necessary to phase stabilize the cavity.

3.2.1 Overcoupling

We have described the relationship between the Q_l of the cavity and its bandwidth. If the cavity has a lower Q_l due the over-coupling of the cavity, the overall bandwidth is increased.

If the BW of the system is large enough, then small variations in the resonant frequency (i. e. microphonics) will have little affect on the cavity fields.

In order to over–couple the cavity it is necessary to increase the power delivered by the source. The amount of RF power required for over–coupling is dependent on beam loading and the amplitude of the induced noise, and can determined through testing in a realistic environment. This higher power increases the loaded Q and broadens the BW of the system, allowing for phase stabilization. Aside from various methods of mechanical, and digital control, this has historically been an effective method of handling microphonics.

3.2.2 Reactive Tuning

ATLAS, the heavy ion accelerator at Argonne National Labs, use a reactive tuner to control microphonics. The idea is based on controlling the reactive component of the detuning field. A circuit made of diode switches, fast switches the load impedance of the reactive power stored in the transmission line, coupled to the cavity, to compensate for the detuning. This method has been used to phase stabilize cavities of 48–150 MHz at ATLAS, and has proved to be an effective and stable system with numerous hours of operation. The system has not been effectively used on higher frequency systems.

3.2.3 Changing the Resonant Frequency

The tuner mechanically changes the ω_o of the cavity is a method of adjusting the resonant frequency. Another method of adjusting for the shifting resonant frequency, is by allowing the driving frequency of the cavity to shift with the changing resonant frequency. This can be accomplish by means of modulating or adjusting the RF signal driving the system.

We shall consider two methods of generating the driving RF signal, the self excited loop, and the generator driven control loop. The former system has the ability to shift its resonant frequency while the latter is based on a fixed known frequency.

Self excited system

In the self excited loop, the signal from the cavity output is compared to the driving RF signal. The two signals are processed by a mixer where the RF and LO signals are of the same frequency. The filtered IF is the instantaneous phase difference between the two signals. This measured phase difference has a direct relationship to the frequency offset by equation (3.1). By applying this phase difference to the signal generator in the form of a modulation, the driving signal can be adjusted for the difference just measured. The drive signal moves in relation to the resonant frequency of the cavity thereby allowing for constant fields within the cavity.

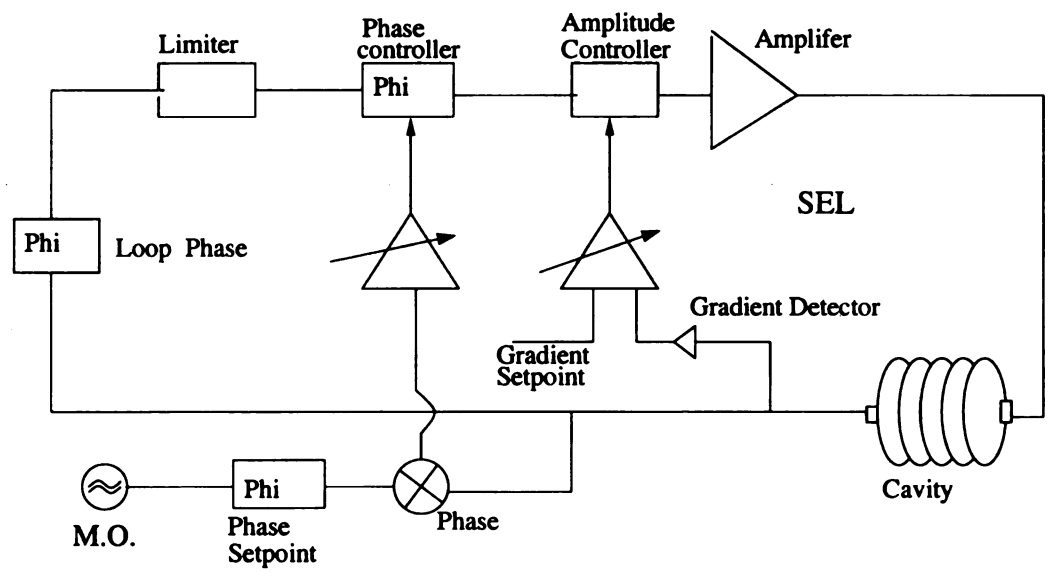

Figure 3.1. Self Excited Loop

$$\frac{d\omega}{dt} = \phi \tag{3.1}$$

Generator driven

The second means of driving the system is through generator driven loop, which is based on a fixed frequency and operates under the assumption that the cavity is at a fixed resonance. Any offset from resonance will have to be adjusted elsewhere. The controller procured by NSCL and under consideration for this thesis is a generator driven system. We will refer to the controller as the LLRF controller.

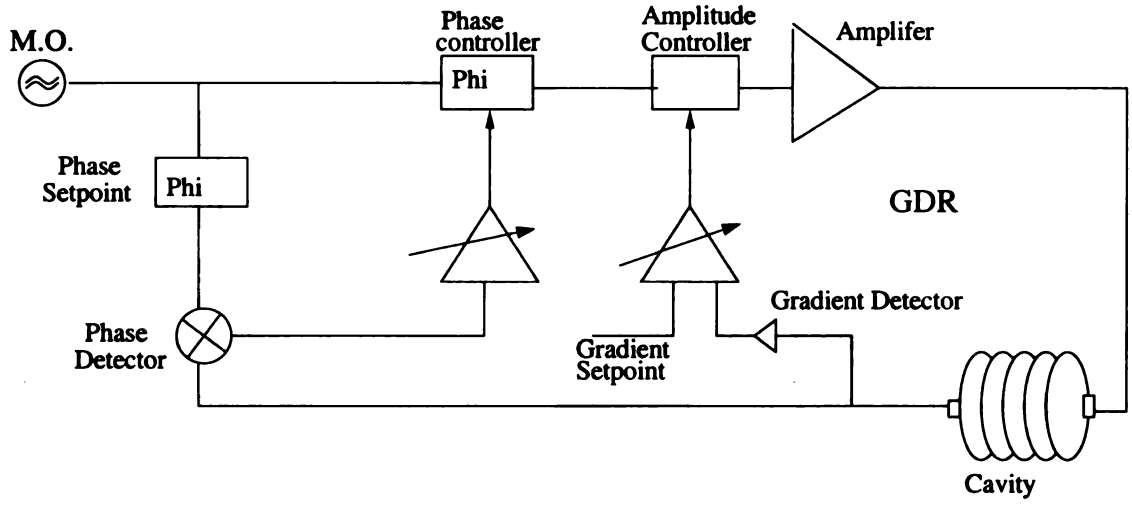

Figure 3.2. Generator Driven Loop

3.2.4 Digital Control

While diminishing the disturbances, mechanical methods cannot over-come the very narrow bandwidth of high Q superconducting cavities to maintain resonance. The digitization and re-creation of the RF drive signal back to an analog signal allows for discrete analysis and correction of the driving signal. The speed at which digital systems operate makes a disturbance under 300 Hz appear relatively slow. This is accomplished by electrically correcting the signal, by point-by-point adjustment of the signal using a Proportional Inte-

grating (PI) control loop to keep values at their desired set-points. This control system will fit in with a generator driven control system so that the resonance of the cavity is maintained as well as the cavity fields.

Digital Signal Processing

One method of digital control is through the use of a Digital Signal Processor (DSP). The DSP is capable of manipulating digital data by analyzing and modulating signals in real time. In this case, it would alter or adapt the values necessary to ensure the RF drive signal is at its proper frequency. DSP's have been used at numerous facilities around the world; for example, the Telsa Test Facility have used DSPs for systems operating at 1.3GHz for a pulsed beam. Pulsed beams are considerable more complicated in that there are Lorentz forces present. Each pulse induces a new electric field, magnetically altering the shape of the cavity and changing the resonant frequency at each pulse. Positive aspects of DSPs are that they are relatively easy to program and available through several manufacturers.

Field Programmable Gate Array

Another processor, which is commonly used in telecommunications, is a Field Programmable Gate Array (FPGA) chip. Similar to Programmable Logic Chip (PLC), the FPGA is made up of thousands of logic units. The benefits of using a FPGA, are its high speed throughput and parallel processing capabilities that allow for real time processing, as well as its ability to be reprogrammed along with its cost. It may be programmed to do similar functions as a processor chip may do, but does not have the overhead architecture. A simple logic output may take ten times longer to process on the processor because of its overhead, but the FPGA is limited to less complicated math operations, because it lacks some of the necessary overhead. The number of operations per sample is much higher with FPGA due to its architecture, accounting for its speed [11].

The FPGA is faster when complicated co-processing procedures are not required, in

which case a DSP is faster. For example, a trigonometric calculation is faster on a DSP compared to an FPGA, unless a form of digital manipulation of shifting registers to multiply and process numbers is used in the FPGA code. Using a routine called Cordic, one can determine the phase and magnitude of a signal without using a single trigonometric function.

FPGA's are faster in terms of raw performance but there are downsides as well. An FPGA is much more complicated to program. There are limited number of qualified programmers with the skill set for Verilog or VHDL. Due to the complexity of the FPGA, the manpower and implementation costs are disadvantageous for most small applications. Newer FPGA chips have DSP functionality built in, allowing for some more complicated processing. The LLRF controller referred to in this thesis is based on the FPGA chip.

3.3 Digital Controls Within the Linac

A generic method of how a controller would fit into the overall linac is described in figure 3.3. This is a representation of a single cavity control. Each cavity would have the similar set-up, operating at the appropriate frequencies. The reference distribution at the top is distributed throughout the linac and must be extremely stable in phase. The entire system is dependent on the phase stability of this reference signal. The right side of the figure displays the cavity, amplifier and measured signal from the system. The piezoelectric actuator is connected to the tuner to mechanically control vibrations. The control for the actuator is in the form of a fast and slow tuner from the main controller.

We define fast tuning as the signal applied to the tuner to reduce vibrations under 300 Hz. In this case, the LLRF controller is the tool to measure the change in frequency and or phase, while a separate controller, such as an Adaptive Feed-forward Controller (AFC) may be implemented, to mechanically dampen cyclical sinusoidal disturbances [8].

Slow tuners will be in the form of screw type device, stepper motor or prestressing the

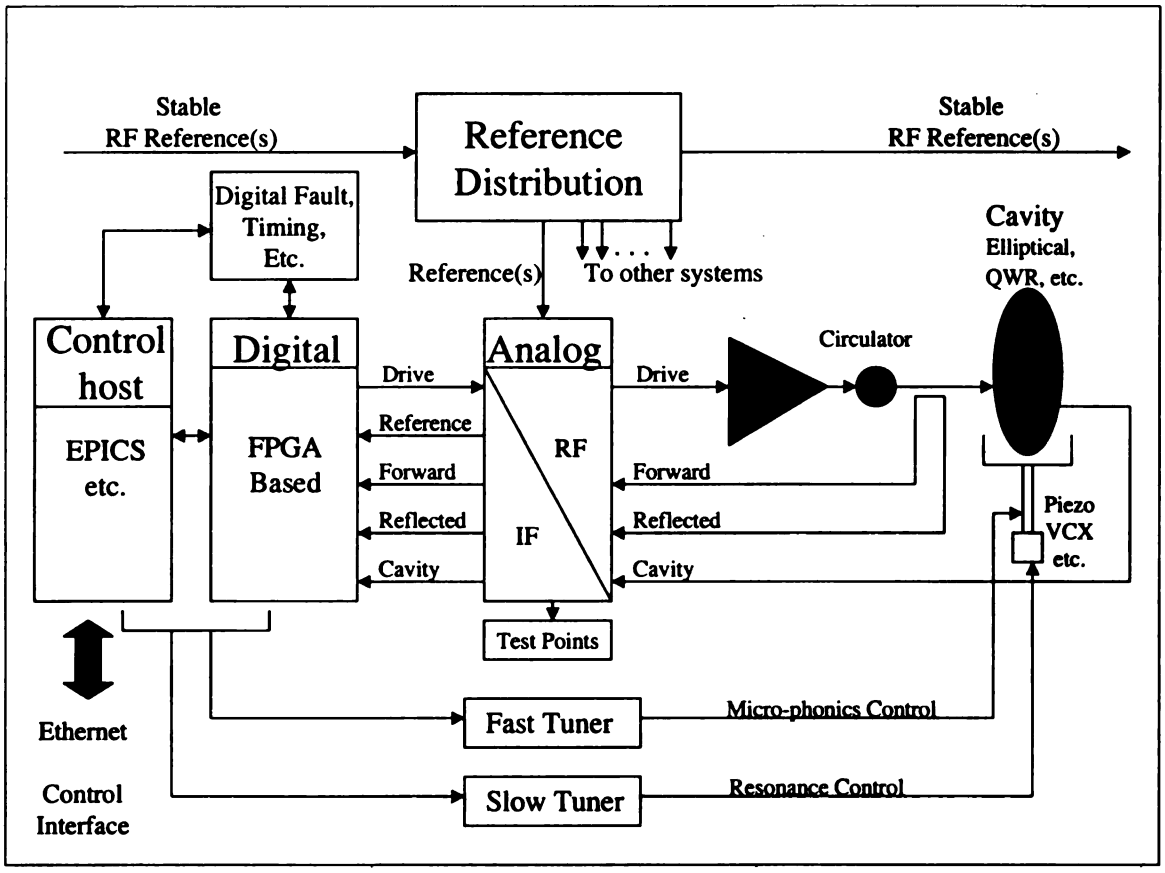

Figure 3.3. System diagram.

piezoelectric actuator to handle tuning or very slow drifts in frequency. Again the control will be dictated from the main controller which monitors all system parameters.

The left side of the figure contains the control host and the digital controller. The control host is the interface that handles the user interface and communicates directly with the digital controller. Experimental Physics Industrial Controls Systems (EPICS) is a well known system used in most accelerator labs, to interface with, monitor and control sensors as well as motors throughout the entire accelerator.

The digital controller is where the analog signals are digitized, measured and processed to create the corrected new output driving signal to the cavity. The controller will be described in detail in chapter 5.

In the middle of the figure is the analog converter. It splits and downconverts the mea-

sured signals from the cavity to the appropriate intermediate frequency (IF) and amplitude that the digital controller can handle. Test points allow verification of the signals at the IF and RF levels.

This arrangement is not specific to any one type of digital controller. In our case, it suitably represents how the controller ties into the overall system.

3.4 Reasons for Choosing LBNL LLRF Controller

We procured the LLRF controller from Lawrence Berkeley National Labs (LBNL) as this design was tested and being commissioned for use at Spallation Neutron Source (SNS) accelerator, in in Oak Ridge, Tennessee. While their system is pulsed, and RIA is continuous wave (CW), its complexity would likely be able to support RIA specifications. Dr. Larry Doolittle who put together the LLRF controller has a wealth of experience in the field accelerator physics and microphonic detuning. Additionally, LBNL was willing to support outside labs, making their controller the only system of its type available.

It would appear that this design would have the best chance of success, given the background and the lessons that we could learn from the installation and commissioning at SNS.

3.5 Conclusion

By understanding the source of disturbance and several methods of reducing or eliminating them, we can look at one specific type of controller that shows promise in stabilizing cavity fields. The digital controller, specifically the LBNL LLRF controller, will be discussed in its method of operation. We have seen a glimpse of how the controller ties in to the system. Further discussion of signal processing will help in understanding the method this controller operates.

CHAPTER 4

Signal Capture

4.1 Introduction

Having decided on a digital controller to stabilize cavity fields, a basic understanding of various components and signal processing tools is necessary to discuss some of the methods used in the LLRF controller. A brief discussion of mixers, downconversion, and sampling rates will be described.

4.2 Vector Control

If we consider the two methods discussed in 3.2.3 of how to drive the cavity, both the generator driven and self-excited system rely on measurements of the cavity field amplitude and phase. Cavity voltages can be expressed as vectors in the complex plane, and may be described either in terms of amplitude and phase in polar coordinates, or as real and imaginary components in rectangular coordinates.

Real and imaginary components are sometimes referred to as I (in phase 0°) and Q (quadrature 90°). Analog components such as IQ demodulators are capable of extracting information such as phase modulation or frequency offset from center frequency. Alternatively, the I and Q values may be extracted digitally using analog-to-digital converters (ADC). In analyzing control systems for large disturbances, a vector controller based on real and imaginary components is preferable. A phase controller could possibly correct the phase into the wrong quadrant due to the cyclic periodicity of phase response, as informa-

tion is based on phase location only. A change of 30° from 0° may be in the first or forth quadrant. Its relation to a previous input may not account for a three quadrant shift in phase. The phase appear to be the same but the direction of the change is not the same, and the compensation would not be correct, if based on the incorrect phase position. In complex form the exact position is known relative to a previous point. The LLRF controller uses a digital method to obtain I and Q signal information.

4.3 Downconversion

The RIA cavity tested for this report operates at 805 MHz. Even as technology improves, the fastest commercially available ADC today, can sample at 105 MHz. It is therefore necessary to downconvert the high frequency signal to a lower frequency that the ADC can handle. Choosing the appropriate frequency depends on the ADC sample rate, as well as other issues such as imaging. Image frequencies are repetitions of a frequency spectrum, resulting from discreet sampling.

Downconverting is performed through the use of mixers. A mixer is essentially a signal multiplier of two input signals, a radio frequency (RF) signal and a local operator (LO) signal. The output is an intermediate frequency (IF) which is the sum and difference of the two frequencies. Filtering out the unwanted frequency and harmonics will leave an IF of a specific frequency. The trigonometric function (4.1) may be evaluated by applying two separate signals A (4.2) and B (4.3),

$$\sin x \sin y = \frac{1}{2}\left[\cos(x-y) - \cos(x+y)\right] \tag{4.1}$$

We refer to A as,

$$a(t) = A\sin[(\omega_a t) + \theta_a] \tag{4.2}$$

and B as,

$$b(t) = B\sin[(\omega_b t) + \theta_b] \tag{4.3}$$

Multiplying these two signals, the output becomes,

$$\begin{aligned} a(t)b(t) &= \frac{AB}{2}[\cos(\omega_a - \omega_b)t + (\theta_a - \theta_b)] \\ &\quad -\frac{AB}{2}[\cos(\omega_a + \omega_b)t + (\theta_a + \theta_b)] \end{aligned} \tag{4.4}$$

The result is the sum and difference of frequencies A and B, as shown in (4.4). If for example A operated at 100 MHz and B at 10 MHz the IF would be both 90 MHz and 110 MHz. Adding a low pass filter would leave the 90 MHz signal to work with. This is the basis for modulating and demodulating signals. While these equations are true for ideal components, in reality there are some non-linear responses at higher amplitudes and image frequencies that may add some distortion or noise into the system.

Noise, or unwanted signals can emerge from mixers in the form of harmonics from the original signal or internally from the switching action of the mixer itself. Double balanced mixers (DBM) have the ability to avoid spurious noise on the IF port due to its construction. A diode ring completely isolates the IF from the RF and the LO. Equation (4.5) calculates the IF frequency for all possible harmonics of the input signals. An ideal DBM rejects all spurious responses when either or both input harmonics are even (m and/or n are even). For this reason, DBMs are a preferred mixer. Various combinations of integer multiples of either or both the RF and LO can emanate from the mixer. It is therefore necessary to consider the possible combinations of the sum of multiples of each frequency as an image frequency.

$$\omega_{IF} = \pm m\omega_{RF} \pm n\omega_{LO} \tag{4.5}$$

Note that m and n are integer harmonics of both RF and LO that mix to create spurious products. In reality the amplitude of the spurious components decrease in amplitude as the value of m or n increase, so higher-order multiples cause minor distortion relative to the first harmonic and are typically filtered out.

Looking back at our example, the first image occurs when the 2nd harmonic of B mixes with A, resulting in ±20 MHz from the 100 MHz. DBMs reduce this even harmonic so we can neglect it and consider the 3^{rd} harmonic which produces a disturbance out of range. The 2^{nd} harmonic of A (200 MHz) and 9^{th} harmonic of B (90 MHz) result in images at 110 MHz and 290 MHz. At issue is when our desired IF is 110MHz and an image occurs at that same frequency. The amplitude readings for the IF signal would sum the two signals resulting in incorrect measurements. The amplitude of the 9^{th} harmonic may cause problems depending on the sensitivity of the system.

Another issue is phase noise, which is the result of an unstable LO, or a clock with jitter. An unstable reference clock has some shift in time. Any movement in time is relative to a phase shift and will be seen at the output as jitter in amplitude or phase. Clock drift sometimes occurs as environmental changes occur that would also affect measurements. To compensate or correct for drift in clock cycles in our cavity set up, a reference signal is used to phase match all cavities in the linac. The controller uses the reference signal to phase lock the cavity signal. By phase locking the cavity signal the frequency is kept in complete synchronization in phase and therefore the amplitude is also matched in terms of clock cycles. Phase locking the signals ensures that the sampling frequency is correct and avoids sampling uncertainties.

In the case of the 805 MHz cavity, 50 MHz is the IF frequency. The LO frequency was decided to be 755 MHz. The IF is far enough from both the RF and LO to easily filter out any sideband or images that might appear as a result of the mixer.

4.4 Digital Sampling

Sampling acquires waveform representation through a sequence of discrete values of a continuous time signal taken at uniform time intervals. Each discrete value is a measurement of the waveform amplitude at its sample time. Resulting in a sequence of numbers representing amplitude at even timed intervals. The inverse interval period, or sampling frequency (f_s), is usually required to be a minimum of twice that of the maximum frequency in question (f_a), to obtain sufficient data to reconstruct the original signal with no loss of information. Images or aliases may still exist after sampling, depending on the sampling frequency, therefor some care must be taken in the design to avoid noise.

Nyquist zones

The first Nyquist zone is defined as the range of frequencies between DC and $\frac{f_s}{2}$. The frequency spectrum is divided into infinite Nyquist zones. The 1^{st} Nyquist zone starts at DC, the 2^{nd} Nyquist zone starts at $\frac{f_s}{2}$, the 3^{rd} zone starts as f_s, and continues on, as can be seen if figure 4.2.

The sampling frequency must adhere to the Nyquist bandwidth to avoid aliasing. Nyquist Bandwidth states that the sampling frequency must be greater than twice the frequency spectrum bandwidth of the input signal in order to be able to reconstruct the original signal perfectly from the sampled version. If a signal has a center frequency of 805 MHz, ± 1 MHz, then the spectrum BW is 2 MHz and the minimum sampling frequency would be 4 MHz after downconversion. Images of the original signal occur at integer multiples of the sampling frequency. $|\pm \mathrm{m} f_s \pm f_a|$

where $\mathrm{m} = 1, 2, 3, \ldots$

Looking at figure 4.1, we can see the frequency domain representation of f_s, f_a, and the alias frequencies of the original signal.

f_s = Samplingfrequency

f_a = Frequencyspectrumofinterest

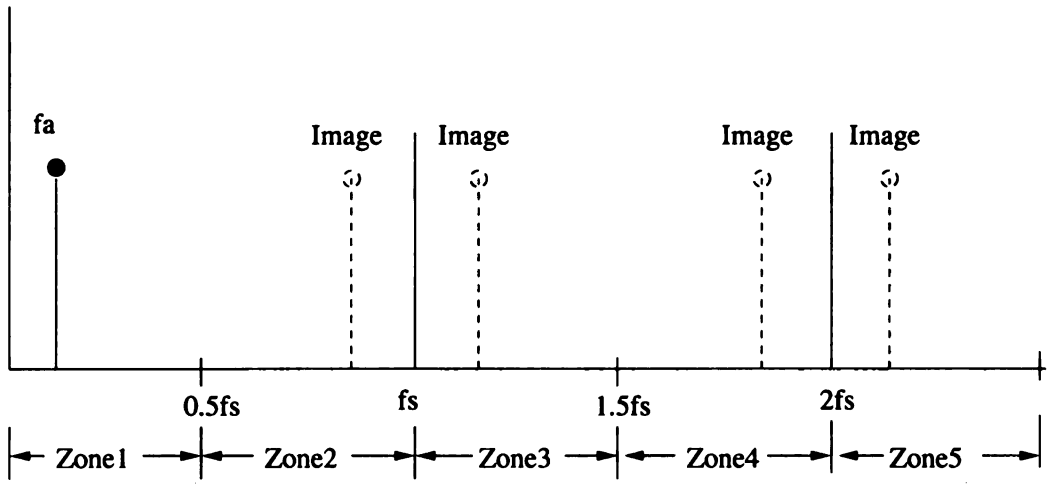

Figure 4.1. Signal f_a sampled at f_s using ideal sampler with images at $|\pm m f_s \pm f_a|, m = 1,2,3,\ldots$

Figure 4.2, shows that if f_s is too close to f_a, an image frequency is produced in the 1^{st} Nyquist zone. Note that if we consider the condition of figure 4.2 where a potential noise (unwanted signals) exits at any of labeled image frequencies, there will be an image of that particular noise in the 1^{st} Nyquist zone. In this case the noise will be sampled as well as the intended signal. To avoid any spurious frequency components in the 1^{st} Nyquist zone, appropriate filtering is required on the analog signal prior to the ADC. A well designed 'anti-aliasing filter' will avoid any spurious signals outside the Nyquist bandwidth. This will be even more important when we discuss undersampling techniques.

Just as in analog demodulation, a f_s too close to $2f_a$ makes it more difficult to filter away unwanted images, due to limitations on the spectral sharpness of the response filter. By

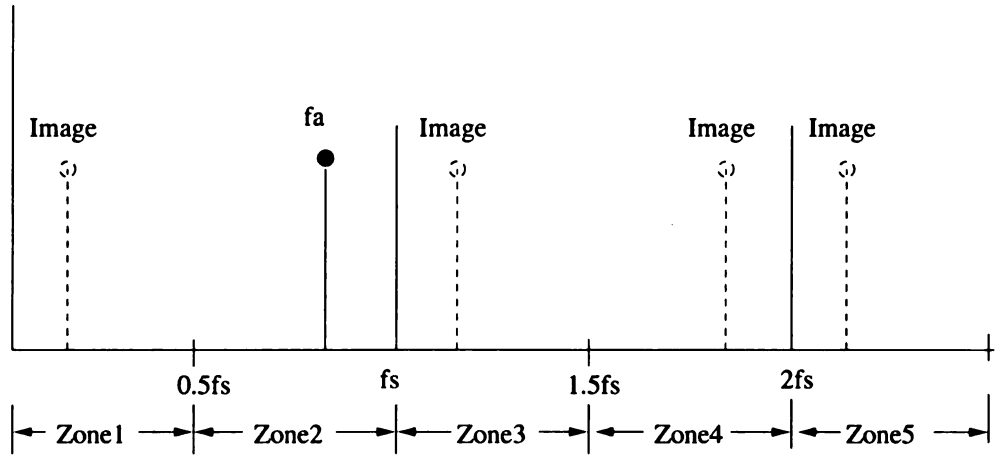

Figure 4.2. Sampling a signal outside the first Nyquist zone, image falls within the first Nyquist zone.

increasing the sampling rate, the anti-aliasing filter roll-off requirements may be lowered. Of course, there are limitations on how fast ADCs can sample, and inherently the cost is reflected in the speed.

Baseband sampling occurs when all signals of interest are within the 1^{st} Nyquist zone. With baseband signals all the images occur outside the 1^{st} Nyquist zone. Undersampling or harmonic sampling occurs while sampling a f_s higher than the 1^{st} Nyquist zone.

Undersampling

Observing the sampled data spectrum of a frequency in the second Nyquist zone reveals output identical, yet frequency reversed relative to the baseband frequency (figure 4.3). The original spectrum is folded in the second Nyquist zone and then again for the third Nyquist zone, and continues folding in each zone. Exact data representation may be acquired from a signal from any odd Nyquist zone, given the signal with the Nyquist bandwidth. This limitation is known as the *Nyquist critea.* Otherwise stated as *a signal must be sampled at a rate equal to or greater than twice its bandwidth in order to preserve all the signal information.*

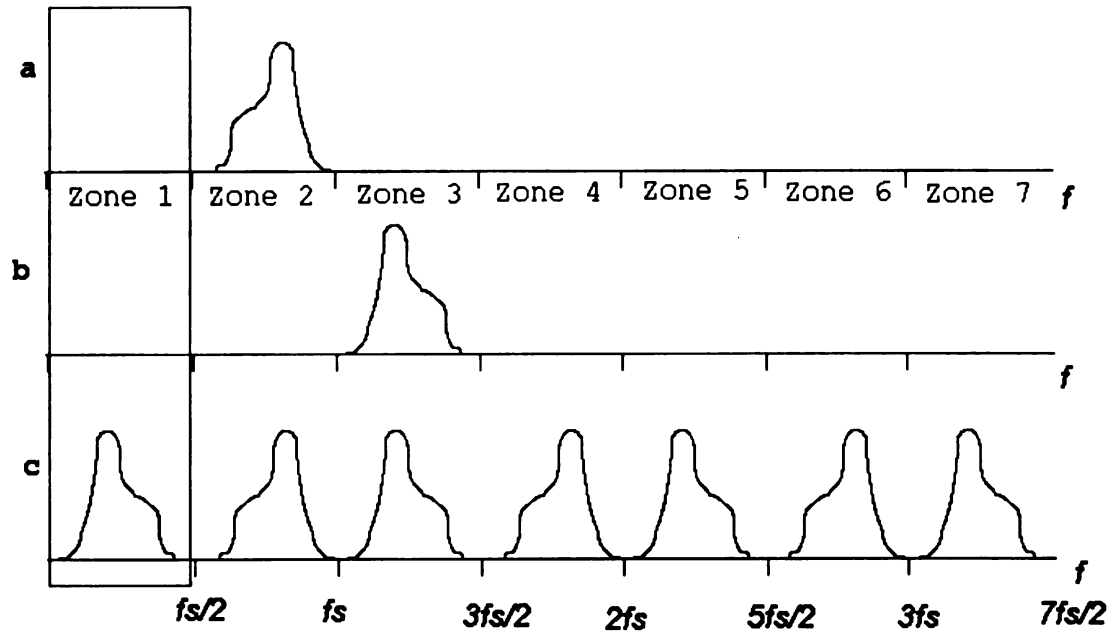

Figure 4.3. Undersampling a signal in second and third Nyquist zone resulting in identical sampled data spectrum.

Figure 4.3, plot **a**, is an example of a signal whose frequency spectrum resides in the 2^{nd} Nyquist zone, and plot **c** is the resulting frequency spectrum. Plot **b**, is the reversed frequency spectrum of plot **a** and sits in the 3^{rd} Nyquist zone. The output from plot **b**, also results in the equivalent frequency spectrum plot **c**. Note how the even zones have a reversed frequency spectrum, and that the sampled signal is clearly within the Nyquist bandwidth, and therefore not aliased.

Any additional signals or noise outside the original Nyquist bandwidth will create images in all other zones, producing noise or a corrupted frequency spectrum within the sampled data. For under-sampling techniques, the anti-aliasing filter prior to the ADC needs to be a bandpass filter with high roll off to ensure a clean sampled spectrum of the original signal, by confining the sampled frequency to the Nyquist bandwidth.

4.5 Demodulation

4.5.1 Analog

Traditional analog I/Q demodulators require the RF signals to be split and compared to a LO to determine I and Q, through the use of mixers. The filtered output of the LO and RF signal is I, while Q is the filtered output of RF mixed with LO phase shifted 90°. The values of both I and Q are then sampled by an ADC and digitized to obtain the digital version.

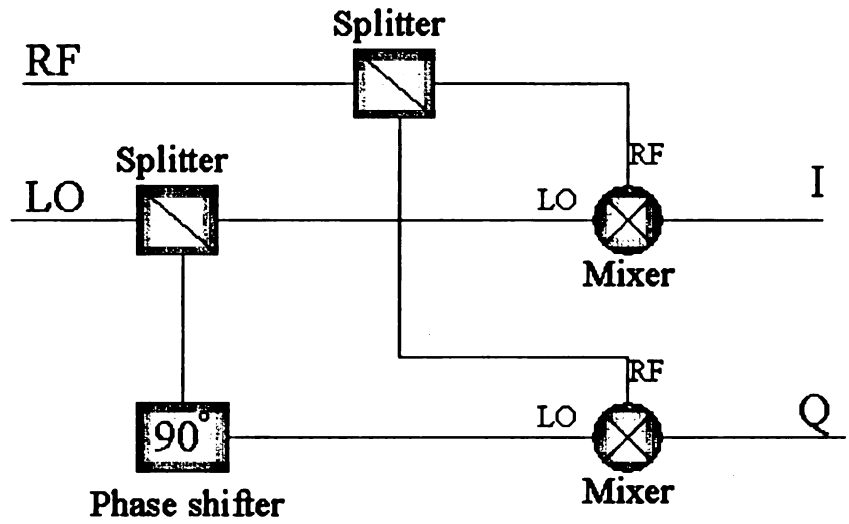

Figure 4.4. Analog method of determining I and Q values.

Areas of difficulty with analog IQ demodulation arise from any gain or difference in signal amplitudes, or phase errors to mixer inputs. Mixers inputs must have identical amplitude inputs for both I and Q measurements. The phase separation for the LO must be exactly 90°, for true Q values. Physical issues such as cable lengths for phase matching, amplitude gains, leakage through any mixer ports, DC offsets, as well as impedance matching components are all potential sources of error. These errors may be eliminated or compensated for by careful RF design, but any single error may cause RF measurement errors.

4.5.2 Digital

An alternate method of acquiring I/Q data is by sampling a signal at four points for each period. Hence, samples are taken at 90° intervals, assuming that the frequency is fixed. Assuming the first sample is at 0°, corresponding to I, the next sample is at 90°, or Q, the next sample is at 180°, or -I, and finally a sample at 270° corresponding to -Q. The ADC streams a series of I, Q, -I and -Q which can be manipulated once it is digitized.

Of course this is possible with an appropriate speed ADC. It may be necessary to down-convert the original RF signal to a reasonable frequency that is exactly four times slower than the ADC sampling rate. We mentioned the necessity for proper filtering post down-conversion to eliminate the unwanted sideband. For digital sampling purposes it is necessary to install an anti-aliasing filter prior to the ADC to reduce any noise from frequencies outside the desired range.

In the case of comparing more than one signal, one of the greatest concerns with digital sampling are the signal levels. During down-conversion, signal amplitude are usually attenuated through mixers and must be enhanced to ensure proper signal levels are input to the ADC's. The amplitude of the signal is what is measured by the ADC's, therefore it is important that the signal inputs to the ADC's are matched, otherwise digitized levels are incorrect. Alternatively, low input signals may be scaled higher digitally, but this does not improve the resolution of the reading and account for a larger possible error in phase or amplitude measurements. Ideally all readings are made at full scale to ensure maximum resolution of the digital value.

Knowing that the sampling must be performed four times per period, and understanding the under-sampling theory, a formula for determining the rate of sampling can be established.

$$f_s = \frac{4f_a}{(2\mathrm{N}-1)}\mathrm{Hz} \tag{4.6}$$

where N is a Nyquist zone.

Relative to analog demodulation once the IF frequency has been filtered, the benefits of using a digital demodulator are in eliminating issues regarding gain balancing, phase matching, or even impedance matching as the readings are sampled prior to any use of a mixer. There are no DC offset or drift to manage either. Conversely, some issues can be troublesome. Any clock jitter is still a major concern as the timing of the samples is critical in maintaining true I/Q measurements. Additionally, if the frequency sampled is not exactly at the desired frequency the samples are no longer 90° apart. However, quadrature phase error is representative of the frequency offset [24].

4.6 An I/Q Sample Example

Consider the case of the LLRF controller in our scenario. The cavity in our system operates at 805 MHz. Our initial concern is to decrease the frequency to a level that an ADC may read. A 50 MHz IF was determined to be an appropriate level and was obtained by down-converting the cavity output at 805 MHz with a 755 MHz reference signal. The reference signal is phase and amplitude stable across each cavity to ensure the 50 MHz IF is in phase with all other cavities by the on-board Phase Lock Loop (PLL). The PLL synchronizes the phase of reference signal to the on board clock of the LLRF. The ADC's and DAC are based on the LLRF clock and once locked to the reference signal, the ADCs ensures that the sampling is performed at the same phase for each cavity.

Care must be taken to ensure the signal levels for various inputs are all amplified to a limit and attenuated so they are matched. This signal is filtered by a 50 MHz band-pass filter to avoid any extraneous aliasing of any images during the digitization process. To digitally determine IQ values of the 50MHz signal, we use the fact that four sampled points are necessary per period to obtain I and Q data. With the formula 4.6 and some simple math we can determine the appropriate Nyquist zone to use for under-sampling.

$$f_{image} = \frac{1}{4} f_s \tag{4.7}$$

and from imaging we know

$$f_{image} = f_a - f_s \tag{4.8}$$

so

$$\begin{aligned} \frac{1}{4} f_s &= f_a - f_s \\ \frac{5}{4} f_s &= f_a \end{aligned} \tag{4.9}$$

Now plug 4.9 into 4.6

$$\begin{aligned} f_s &= \frac{4 \cdot \frac{5}{4} f_s}{(2N-1)} \\ 1 &= \frac{5}{2N-1} \\ N &= 3 \end{aligned}$$

If the $f_a = 50\ MHz$, then the f_s for the 3^{rd} Nyquist zone is 40MSPs. If we were to consider the 1^{st} Nyquist zone, the resulting sampling rate would be 200MSPs which is beyond the ability of our ADC. It is still important to use the highest sampling rate available so as to reduce quantization noise and aperture jitter [14]. Consider the example of sampling a 50 MHz signal at 40 MHz and the image at 10 MHz as is represented by the figure 4.5. In figure 4.6, the square wave is the clock cycle of the ADC running at 40 MHz, where the rising edge of the clock measures the amplitude of the 50 MHz signal at discrete points. The points extracted are the discrete values of the 50 MHz and the 10 MHz signal because the 10 MHz image is an exact representation of the 50 MHz signal. The measured

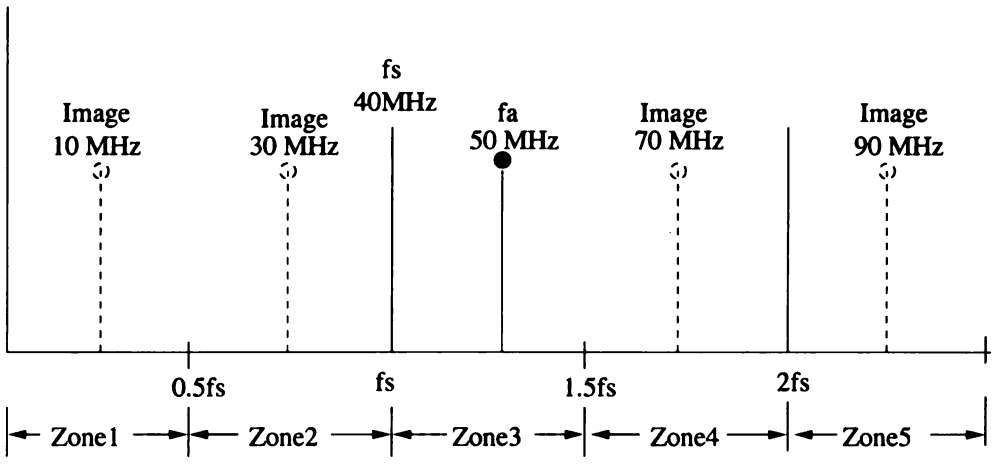

Figure 4.5. Example of images from a 50 MHz signal sampled at 40 MHz.

values equate to the I, Q, -I, -Q values of the 10 MHz image. This is identical to sampling the 10 MHz image at 40 MHz, where there are four samples per period which are 90° apart. If the clock for the ADC and the IF signals are phase locked, these sampled values represent the I, Q, -I, and -Q values of the intermediate 50 MHz frequency.

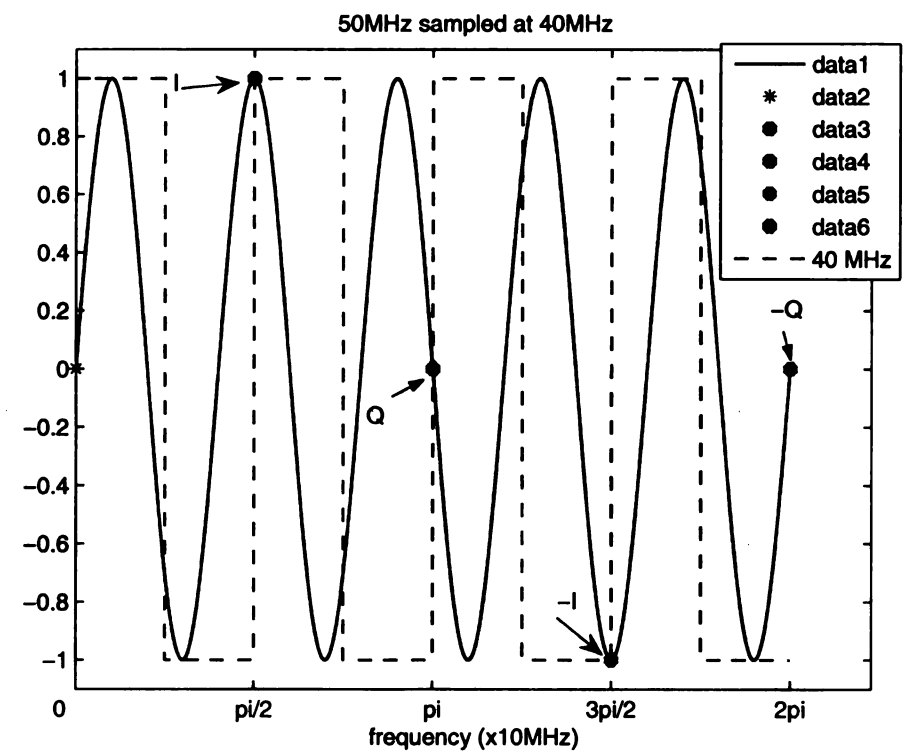

Figure 4.6. Sampling 50 MHz signal with a 40MSPs ADC.

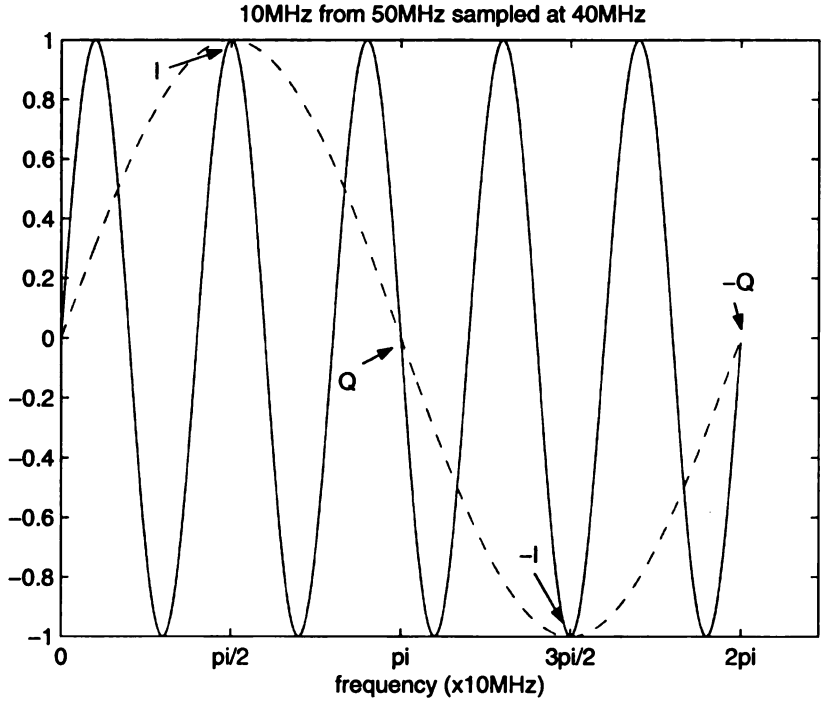

Figure 4.7. The 10 MHz image extracted from sampling.

4.7 Conclusion

An introduction to both some analog and digital methodology has been presented to aid in describing the means by which the LLRF works. Moreover a analysis of how I and Q data are obtained from the cavity output has been described. We have seen that under-sampling a signal such as the cavity output can be demodulated into I and Q values for manipulation. The FPGA easily supports complex variable and the associated math in rectangular coordinates.

The next phase is to overview the manipulation of data to ensure that cavity field are maintained.

CHAPTER 5

Digital Flow

5.1 Introduction

The LLRF controllers main function is to correct the phase and amplitude of the driving signal to ensure consistent fields within the cavity. Once the signal information is digitized, the error can be determined and data streamed through a Proportional Integrator (PI) control loop. This chapter investigates the digital design and flow of data to perform the compensation. Starting with some fundamentals of PI compensator, and then describing the elements used in the system to generate data to feed the control loop, we conclude by following the data stream of the LLRF controller from a system bitwise flowchart.

A generalized form of a control loop is represented in figure 5.1 where the compensator modifies the error signal between the plant output and input, to attain desired transient response of the system. The goal of the LLRF compensator is to virtually eliminate steady state error. Borrowing the terminology from control engineering, the plant represents the SRF system (cavity, amplifiers, microwave components, etc.), while the controller represents the PI loop. The error signal ($e(s)$) is determined by the difference between the calculated set-points and the cavity output.

The cavity output C(s), is a stream of I, Q, -I, and -Q values as described in chapter 4. User set-points are entered using the LLRF Graphical User Interface (GUI), modified by a direct digital synthesizer and a CORDIC routine, to generate a stream of I, Q, -I, and -Q set-point values.

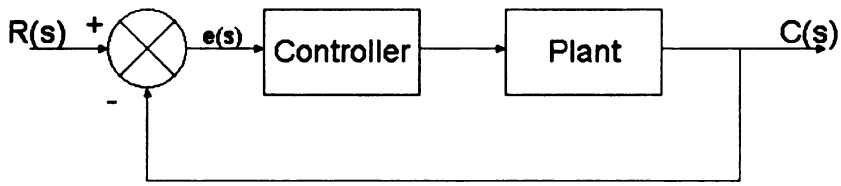

Figure 5.1. Closed loop system.

5.2 Proportional Integrator Controllers

Controllers are designed to improve the transient response of a system. Continuous time systems are frequently transformed into the S-domain by Laplace transformation to simplify the math. The Laplace operator translates a set of integral and derivative equations into a set of linear algebraic equations in the s-domain. Analysis of systems in the s-domain provides useful information regarding the system performance. Figure 5.1 represents a closed loop system with unity feedback. The plant has some transfer function in the s-domain in the form of equation (5.1), for example;

$$G(s) = \frac{(s+3)}{s(s+1)(s+2)(s+4)} \tag{5.1}$$

where corresponding roots of s in the numerator are called "zeros" and the corresponding roots of s in the denominator are called "poles". In equation (5.1), there is a zero at $s = -3$, and poles at 0, -1, -2, and -4. The transfer function of the plant can be plotted as a root locus as shown in figure 5.2. The root locus is a plot of the pole and zero locations in the s-plane. All points must be on the Left Hand Side (LHS) for the system to be stable. The vertical axis is the imaginary axis corresponding to $j\omega$. The horizontal axis is the real value of the transfer function components, corresponding to σ.

A controller is placed prior to the plant to improve the system performance. Increasing the gain alone of a controller decreases the rise time and may improve the steady state error, but at the expense of a higher percent overshoot in the transient response. Conversely,

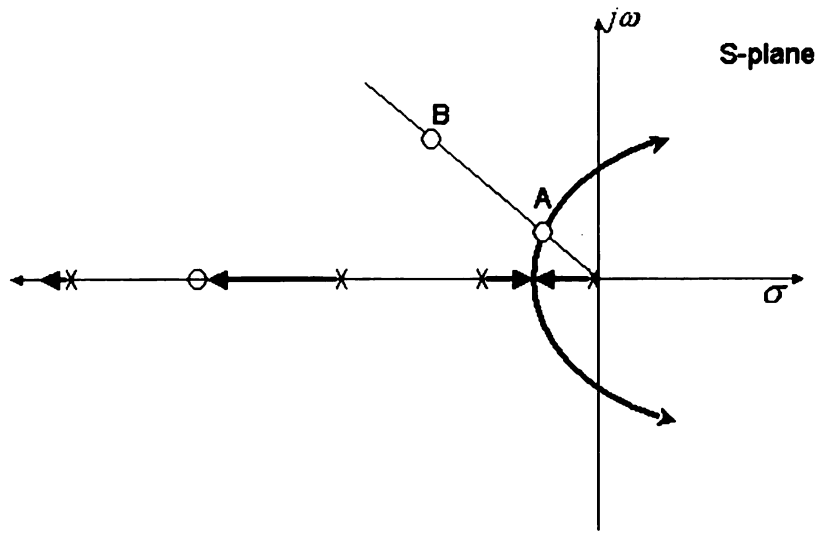

Figure 5.2. Example root locus where A is stable and B is higher gain but not stable.

reducing gain to reduce percent overshoot increases the rise time. With the addition of an integrator controller only, the steady state error will be eliminated, and the transient response will suffer from increased settling times and a poorer overall system response. To illustrate the concept of a controller and its effects on the system, consider the root locus (the heavier dark arrows) shown in figure 5.2. Choosing any point on the root locus will ensure stability and determine the gain, percent overshoot, settle time, and rise time of the transient response. If the desired transient response has a higher gain, for example point B instead of point A in figure 5.2, a compensator is necessary with additional poles and zeros to move the root locus to a stable region that includes point B.

An ideal integrator will move the root locus, by the addition of a pole at the origin and a zero placed very near to the origin. By locating the pole and zero near to each other the overall root locus changes very little, but has the effect of increasing the order of the transfer function and in turn eliminating steady state errors. In the case of the LLRF, eliminating the steady state error is the primary concern. The compensator can maintain the gain but requires the addition of an integrator to eliminate the error [16].

A block diagram of the compensator is shown in figure 5.3 and may be regarded in the

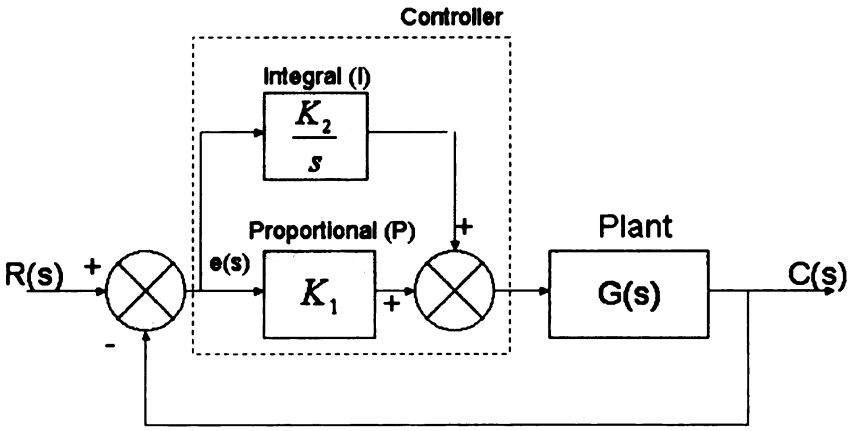

Figure 5.3. Block diagram of a PI compensator.

form of equation (5.2).

$$G_c(s) = K_p + \frac{K_i}{s} = \frac{K_p\left(s + \frac{K_i}{K_p}\right)}{s} \tag{5.2}$$

5.3 Z-transform

Analogous to studying continuous time systems in the s-domain via the Laplace Transformation, the study of discrete time sampled data can be transformed into the z-plane. The z transform can describe the stability of a discrete Linear Time Invariant (LTI) system. Consider sampled data of a continuous time signal as a series of Dirac delta functions in the form of

$$x(t) = \sum_{k=0}^{\infty} x(kT)\delta(t - kT) \tag{5.3}$$

The z-transformation is defined as

$$X(z) = \sum_{k=0}^{\infty} x(kT)z^{-k} \tag{5.4}$$

The relation between discrete signal $x[n]$ and $X(z)$ has a one to one correspondence,

$$x[n] \Longleftrightarrow X(z) \tag{5.5}$$

The relation of $x[n]$ to z^{-k} is such that z^{-1} is a unit delay operator. The relationship between z-domain and s-domain is

$$z = e^{sT} \tag{5.6}$$

Since the Laplace variable s is complex, the variable z is also complex having a real and an imaginary part. The transfer function can be plotted as a function of z on an *Argand diagram*, also called the z-plane, and has similar characteristics to the s-plane. The stability of the system depends on the location of the poles of the system $H(z)$ transfer function. The system transfer function of a closed loop system is

$$H(z) = \frac{X(z)}{Y(z)} \tag{5.7}$$

A discrete-time LTI system is stable if the the poles of the $H(z)$ transfer function lie within the unit circle and the region of convergence (ROC) includes the unit circle. The region of convergence describes how stable the system is. The ROC of a causal LTI system excludes the origin and is less than the magnitude of the largest pole.

$$ROC = 0 > |z| > |p| \tag{5.8}$$

An example of a $H(z)$ transfer function is described in equation (5.9), and is plotted in figure 5.4.

$$H(z) = \frac{X(z)}{Y(z)} = \frac{z}{(z^2+1)(z+0.5)} \tag{5.9}$$

The poles in this case are roots of $Y(z)$ and are located at $(0, \pm 0.5)$ and at $(-0.5, 0)$. Two points lie on the unit circle, which indicate marginal stability [15].

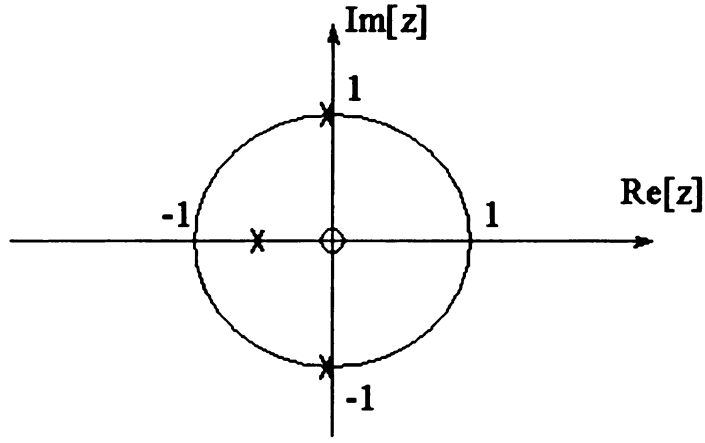

Figure 5.4. Example z-plane plot of $H(z)$.

5.4 LLRF Operational Data Input and Set Points

It is understood that the data flow into the LLRF controller has previously been sampled into complex values of the cavity output signal in the form of I, Q, -I, -Q, by means of signal capture. The second set of data of importance is the set-point values of desired phase and magnitude. These values are determined by the physicists conducting beam experiments and would vary for specific beam composition and target goals. The set-point values are inputs to the controller entered by an operator, who controls the beam via the Graphical User Interface (GUI). The GUI is part of the overall design of the LLRF controller and interfaces indirectly with the FPGA via a network protocol system called EPICS. Determination of phase and amplitude set-point values are unique and are not within the scope of this thesis.

LLRF GUI slide-switches allow the operator to adjust amplitude and phase settings which are used to determine the set-I and set-Q levels. Other main settings are also used to establish stability in the system during operation. These include gain setting for K_p, the proportional gain of the compensator, and K_i, the integral gain setting of the PI loop. Finally, a 'gain rotation' setting is used to compensate for any phase lag acquired in cables. If all cables had zero length, the angle of the feedback would be set to $-180°$. The 'gain rotation' allows for compensation of phase offset caused by all the cables and/or waveguides

in the system, so the cavity sees pure negative feedback.

The following sections begin to outline some the functionality built into the system, that also plays a crucial role in the digital control and flow of bits.

5.4.1 Direct Digital Synthesis

A Direct Digital Synthesis (DDS) is named after the point-by-point synthesis of digital data used to build an analog waveform, otherwise termed a digital frequency generator. DDS has attractive features such as being controlled digitally, fast frequency changes as there is no settling times, and a broad range of frequencies, which are limited only by the filters used in the system. A DDS uses look-up tables to stream a series of phase angles at specific time intervals to a Digital-to-Analog Converter (DAC) where the output can generate a sinusoidal waveform [18].

In the LLRF, a DDS is used but not immediately converted to analog. As discussed previously, the system is designed to sample a fixed 10 MHz frequency (an image of the 50 MHz signal), with sampling rate of 40 MHz, resulting in each clock cycle equaling a 90° phase shift. A register delay holds the bit for one clock cycle which equates to 90°. If the DDS value input is 0, then the stream of angles out of the DDS block phase register is 90°, 180°, 270°, and 360°. If there is an input of a non-zero frequency, the angle input would be different and cumulative in each step. For example if DDS was set to 111 kHz the stream of angles out of the phase register would be approximately $91°, 182°, 273°, 4°, 95°$.... This stream of phase angles is crucial to the operation of the CORDIC rotation process used to calculate the set-point data.

As normal-conducting (non-SRF) cavities ramp up with power, temperature gradients increase significantly on the surface of the cavity and change the shape of the cavity by thermal expansion. To compensate for the resulting substantial change in resonant frequency, the DDS component of the LLRF controller is manually used to adjust the driving frequency to the cavity frequency during the warm up period. For superconducting cavi-

ties, there is also some deformation of the cavity by Lorentz forces. Lorentz forces cause a magnetic deformation attributed to increased electric fields in the cavity. In a CW system Lorentz forces are only issue during the ramping the cavities up to full power. In the Lorentz detuning during initial operation of the cavities, the DDS function can be used maintain resonant frequency while slowly ramping the power. An external measurement of the cavity frequency would be necessary to determine the cavity resonant frequency, which can be adjusted by the DDS function.

An additional advantage to having a built-in DDS is that the controller can work as a stand alone frequency generator, if the controller is left in an open loop.

5.4.2 CORDIC

CORDIC or COordinate Rotation DIgital Computer, calculates and manipulates sine and cosine functions utilizing magnitude and phase data. It is best used when a hardware multiplier is not available and a minimum number of gates is desired, such as the case with a FPGA. Dealing with complex variables of amplitude and phase, or I and Q values, CORDIC iteratively rotates the angle until 0°, adjusting the values of set-I and set-Q at each step. Rotating shifts are based on $\frac{1}{2}$ angles until the final angle is approximately 0°. Determining $\frac{1}{2}$ angles is accomplished by binary shifting [17].

Recall that in rectangular form, a number may be rotated by 90° by multiplying the number with $R = 0 + j1$ where the form here is $R = I + jQ$. The angle can be calculated as

$$\theta = \arctan\left(\frac{Q}{I}\right) \tag{5.10}$$

Similarly, to rotate a number by 45°, we would multiply by $R = 1 + j1$. Note that $\frac{1}{2}$ of 45° is 26.565° and is found by multiplying a number by $R = 1 + j0.5$. The general formula for rotating by successive smaller angles of base 2 is $R = 1 + jK$, where $K = 1, 0.5, 0.25, 0.125\ldots$, or $K = 2^{-0}, 2^{-1}, 2^{-2}, 2^{-3}\ldots$, which is easily accomplished with simple binary shifting, as

opposed to overhead heavy, trigonometric processor architecture.

In the LLRF control loop, a block labeled "16 stage cordic" inputs the rotation angle and constant values of set-I, set-Q. The rotation angle is the phase from the DDS phase register and changes at each clock cycle. If we consider the simplest case where no additional frequency is added from the DDS, than output from the phase register is a stream of multiple angles of 90°. Cordic shifts the I and Q values by $R = 0 \pm j1$ either $\pm 90°$, in its first stage, to get closer to 0°. This ensures that the value is between $-90°$ and 90°. In the second stage the I and Q values are shifted by rotating either $R = 1 \pm j1$ or $\pm 45°$ to get closer to 0°. This routine continues rotating set-I and set-Q based on adding or subtracting successively smaller angles until the error in rotation is essentially 0°. The accuracy is based on the number of bits the phase register has. In our case a true 14 bit rotation occurs producing an accuracy of

$$\begin{aligned} \theta &= \arctan\frac{Q}{I} \\ &= \arctan\frac{1}{2^{-14}} \\ &= 0.003497° \end{aligned}$$

The last stage of the CORDIC routine is the rotated values of I and Q rotated from the DDS phase value shifted to 0°. Of interest is only the resultant set-I value after rotation. The set-Q values are necessary to calculate the set-I with each iteration.

Table 5.1. I/Q values from set-I.

Set-I + angle	Resulting point
Set-I + 0°	Set-I
Set-I + 90°	Set-Q
Set-I + 180°	-Set-I
Set-I + 270°	-Set-Q

Consider an example of an amplitude and phase set-points of $1\angle 30°$, and DDS set to 0, meaning the rotation phase is 90°. Table 5.2 shows resultant outputs of the rotated set-I and set-Q values from the final stage of the CORDIC routine for 5 consecutive rotations.

The output from the "16 stage pipelined cordic rotation" is simply the final set-I value. The final set-I value after each 90° phase rotation is the stream of I, Q, -I and -Q. Figure 5.5 is a representative plot of the sinusoidal wave that would be constructed from only the set-I values of table 5.2. Note that the set-I values in the table are the values at each 90° point which is the rate at which the system operates, i.e. the clock time. The first value is delayed by one clock cycle and plotted at 90°. The incoming value from the cavity to be compared with for error measurement, is also delayed by one clock-cycle.

Table 5.2. Example of CORDIC rotation of set-points.

Rotation (°)	Cumulative rotation (°)	Set-I	Set-Q	Mag. Phase
0	0	0.866	$+0.5j$	$1\angle 30°$
90	90	-0.5	$+0.886j$	$1\angle 120°$
90	180	-0.866	$-0.5j$	$1\angle 210°$
90	270	0.5	$-0.866j$	$1\angle 300°$
90	360	0.866	$0.5j$	$1\angle 30°$

5.4.3 Error signal

The error signal between input and the reference signal is the difference between the discrete set-point value and the discrete cavity output value. If the system was operating with no disturbance and right on target, there would be an error value of 0. If there is a disturbance on or within the cavity, the result is a change in resonance of the cavity and the I/Q values would differ from the unperturbed set-points in the form of a phase shift. Recall that

$$\theta = \frac{d\omega}{dt} \tag{5.11}$$

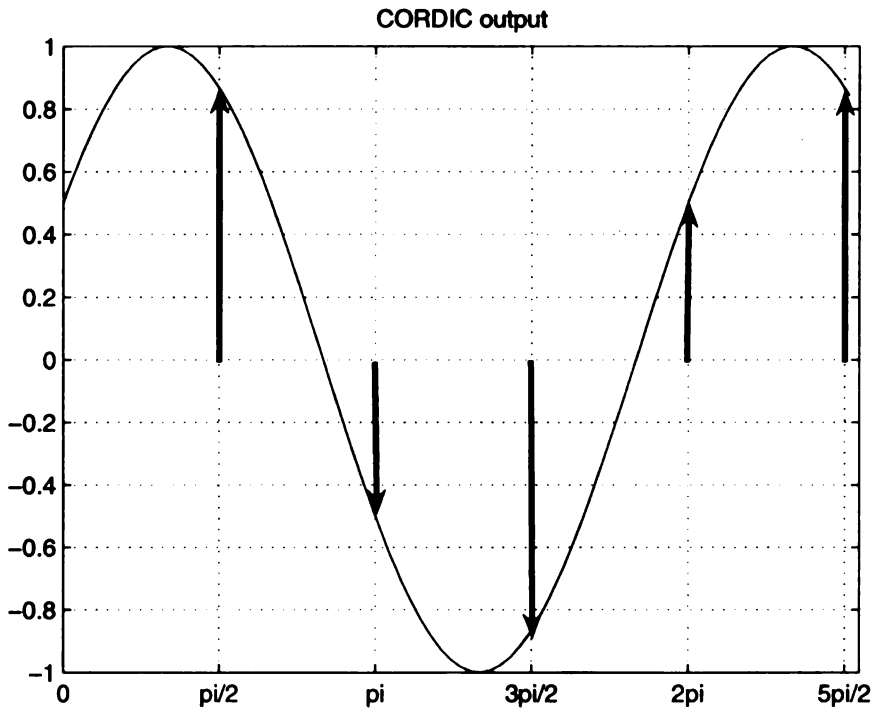

Figure 5.5. Simulated plot of CORDIC output.

The phase offset is measured by a difference in set-point to cavity value. The compensator will generate an adjusted error value to the cavity to compensate for the phase shift and bring the error back to zero.

The function of the DDS is to ensure the set-point values are correct and represent an unperturbed reference. In the presence of Lorentz forces while ramping up the cavity, it is desirable to change the resonant frequency of the cavity drive signal. The DDS frequency can be used to offset the set frequency of the drive signal by implementing a phase offset.

5.5 Follow the Bit Path

A flowchart of the FPGA data flow at a bit level is displayed in figure 5.6. Each shaded block represents a flip-flop, or a latch, where a slight delay allows for accumulated data to

collect and move on at the next clock-cycle. As a result of the one clock-cycle clock delay, these blocks also act as a 90° phase shifter. It is the designers function to ensure that all information has arrived and that the settle time is stable prior to the time of the next clock increment. The blocks in between the latches manipulate the data quickly enough to reach the next latch before the latch is reset.

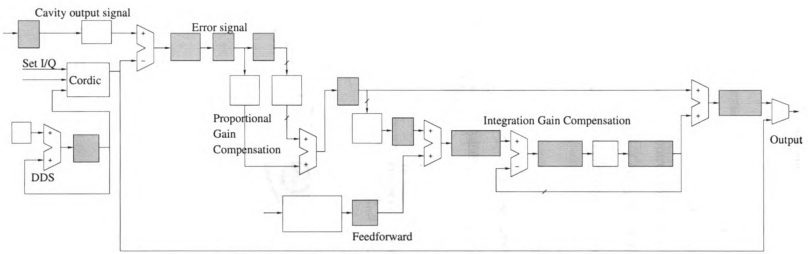

Figure 5.6. Flow chart of digital data and processing for PI.

The blocks labeled as registers work as latches and provide an opportunity for data to transfer from the FPGA to the supporting microprocessor, and EPICS for display purposes.

5.5.1 Inputs

The upper left of the flowchart in figure 5.6 is enlarged to figure 5.7, where 'Cavity Field ADC' input represents C(s) in the general control form. This cavity output signal is digitized, held in a register for display and then fed through a digital bandpass filter to remove any DC offset. This is the I, Q, -I, -Q data stream from the cavity or plant output, which is input into the adder.

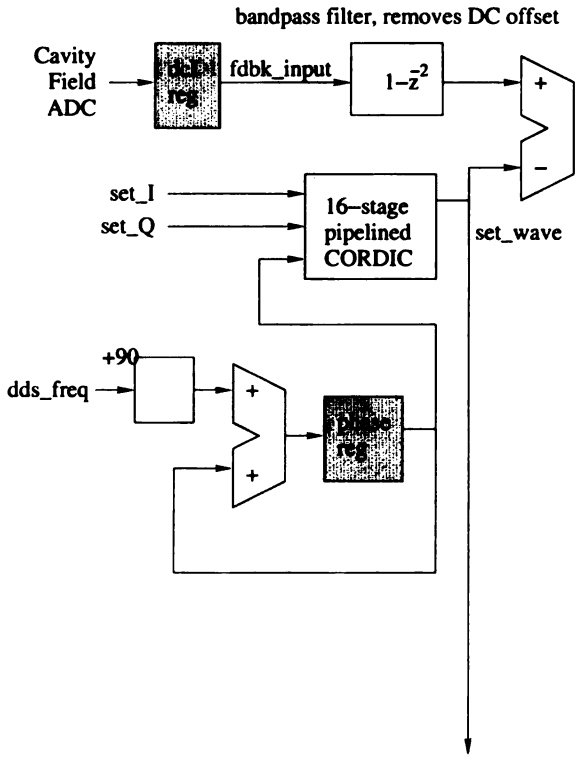

Figure 5.7. Set-point creation by DDS and Cordic.

Below the 'Cavity Field ADC' signal is the set-I set-Q information loaded into the "16-

stage pipelined CORDIC" block, along with the DDS frequency phase output. The output from the "CORDIC" block is the set-I, set-Q, –set-I, and –set-Q stream discussed in the previous section, and relates to R(s) in the general control loop form of figure 5.1. The stream of set-point I/Q data flows to the adder and to multiplexer at the end of the chart. The multiplexer allows only one of either of its inputs to be output depending on its control setting. If the DDS substitute enable is activated then the output of the system is the stream of set-point values. This would be allow the system to operate at any frequency within its filtered range, without the compensator operating, i. e. open loop.

If the DDS substitute enable is off than the set-point data flows to the adder where the set-I is subtracted from cavity output I, during a single clock cycle. The next clock cycle set-Q would be subtracted from cavity output Q value. The data from the adder is the error signal, e(s), on a point by point basis of I and Q.

5.5.2 Proportional Gain

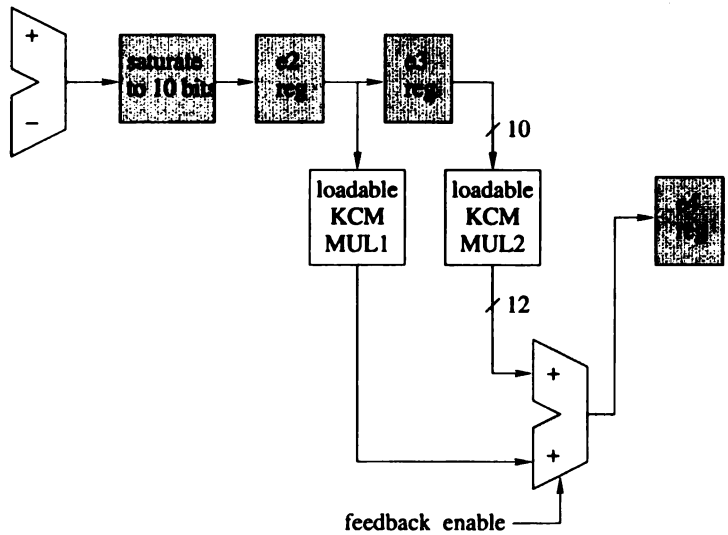

Figure 5.8. Proportional gain.

The accuracy of the error may be reduced at this point (figure 5.8) and the value drops 4 bits in the 'saturate to 10 bits' block, to reduce the volume of data flow. The assumption is that error is not more than 10 bits accurate, and limits the compensation per cycle to that degree of accuracy. Data is passed on to the 'e2' error register. The next clock cycle the 'e2' value is loaded into another error register 'e3', and the loadable Konstant Coefficient Multiplier (KCM) block simultaneously. The effect in loading the second error register allows for a delay so that both I and Q data pass through the KCM blocks and are summed together before reaching the next latch, 'e4'. In the loadable KCM block, the error value is multiplied by the K_p rotated by the gain rotation value. The host processor adjusts the K_p value input from the GUI by the 'Gain Rotation' input to account for cable lengths. The adjusted K_p is now labeled A_p. The host loads the adjusted gains to the FPGA KCM for fast multiplication of the error. The multiplied errors are summed and loaded into the 'e4' register. At this point the proportional aspect of the PI loop is complete, and the value in the 'e4' register is $(I(A_p) + Q(A_p)z^{-1})$. The general form at this stage is $K_p e(s)$. This value flows to an adder and onto the integrator block.

5.5.3 Integrator

In the integrator block, shown in figure 5.9, the adjusted error values are multiplied by the 'KCM MUL3', which is the integral gain $\frac{K_i}{K_p}$ input value from the GUI. The 'e6' register holds the data and sums it with a 'feedforward pipe', and loads the 'Integrate input register'. For CW systems the feedforward value is 0. The feedforward block is designed specifically to deal with ongoing Lorentz forces developed with each pulse of a pulsed system, and is not used in our CW system.

The final set of registers are the integral stage where two registers hold two consecutive values. The integrate sum register holds the value of the $(A_i(I(A_p) + Q(A_p)z^{-1})$ less the previous two values. This holds a history of values and accumulates these values with the new error data, outputting an integral form of data. This is fed to the final adder, shown in

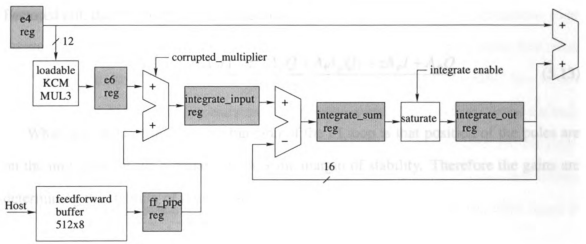

Figure 5.9. Integrater.

figure 5.10, filling the 'feedback error out' register prior to loading the DAC for output.

5.5.4 Compensated Output

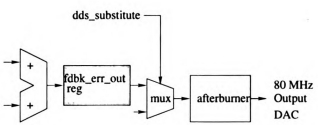

Figure 5.10. Final adder and output.

The output value now has the form

$$(I(A_p) + Q(A_p)z^{-1}) \cdot (1 + \frac{A_i}{(1+z^{-2})}) \tag{5.12}$$

Factored out, the H(z) in polynomial form is

$$\frac{z^3(A_pI + A_iA_pI) + z^2(A_pQ + A_iA_pQ) + zA_pI + A_pQ}{(z^2+1)z} \tag{5.13}$$

What is evident of the transfer function of the PI loop is that position of the poles are on the unit circle of the z-plane, which is the margin of stability. Therefore the gains are determining the stability of the system.

5.6 Digital-Analog Converter Output

The final stage of the data flow passes through the 'afterburner' block, prior to being recreated as an analog signal by the DAC (Digital Analog Converter). For input signal capture, under-sampling was used to create a 10 MHz image of the 50 MHz cavity signal. Under-sampling techniques enabled the retrieval of I,Q, -I, -Q data from the 10 MHz image. Recreating the 50 MHz signal with 40 MHz worth of I/Q data is slightly more difficult. A 200 MHz DAC would enable 4 points plotted per cycle to create a properly represented 50 MHz signal. High speed DAC are not yet readily available. Inputing a 10 MHz data flow of I, Q, -I, and -Q values, onto a 40 MHz DAC will create images at 10 MHz, 30 MHz, 50 MHz, and 70 MHz. Each image would have a decrease in power of $\frac{1}{f^2}$. The desired 50 MHz signal would be available, but after filtering the signal is weak.

The afterburner block adds additional interpolated points between the I, Q values. If the points I, Q stream was of the order of points,

$$a_i,\ a_{i+1},\ a_{i+2}\ldots$$

Interpolating between each of the points above, using the formula $-\frac{a_i + a_{i+1}}{\sqrt{2}}$ builds a stream of data exiting the 'afterburner' block in the form of,

$$a_i,\ -\frac{a_i + a_{i+1}}{\sqrt{2}},\ a_{i+1},\ -\frac{a_{i+1} + a_{i+2}}{\sqrt{2}},\ a_{i+2},\ -\frac{a_{i+2} + a_{i+3}}{\sqrt{2}},\ a_{i+4}\ldots$$

The DAC is also increased in speed to 80MSPs which is still within its limitations. The output is at double the original speed intended with double the amount of data. The result will be a higher frequency output from the DAC. The output from the DAC is a square waveform whose amplitude depends on the incoming value. The DAC output of the controller is represented in figure 5.11, which includes the original output data and the interpolated points added by the 'afterburner'. The original compensated I/Q values are marked as square points, while the added points are marked as hexagons. The 30 MHz signal is

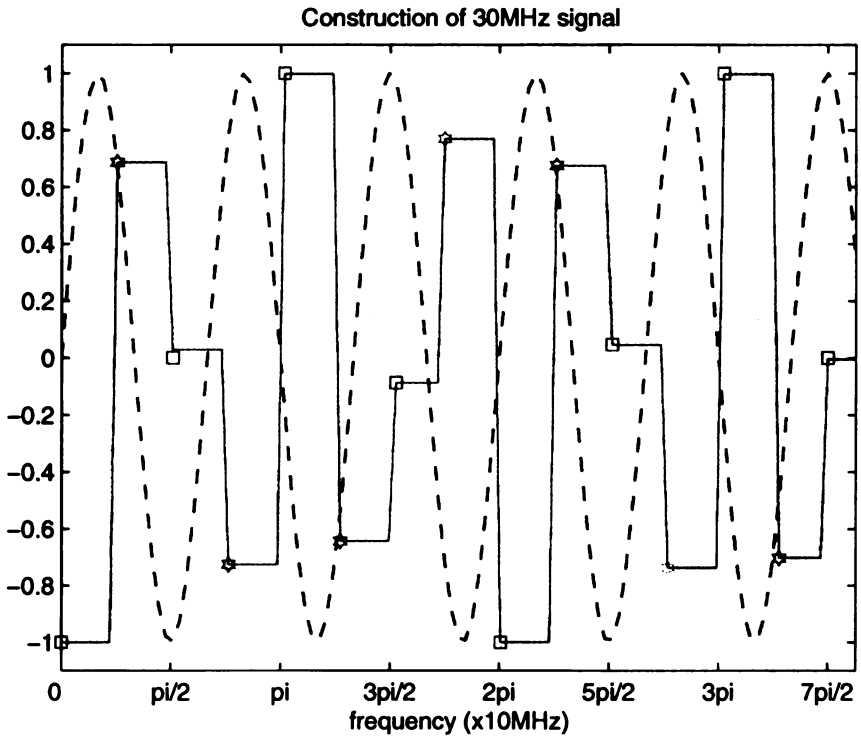

Figure 5.11. DAC output with additional points from 'afterburner'.

the dashed line on the plot along with the DAC output, but the correlation is is not easily understood from the DAC output. A square waveform can be represented as an infinite sum of sine waves of varying frequencies. The Fourier components needed to create the square waveform is a Fourier series comprised of many sine waves, where the most domi-

nant component is a 30 MHz waveform. In addition to the 30 MHz frequency component, there are 50 MHz, 110 MHz, and 130 MHz components that decrease in strength, but are major contributors to the square waveform. A fast fourier transform of the square wave is shown in figure 5.12, displaying the various components of the waveform. For the LLRF, the 50MHz component is band-pass filtered to reveal a perfect representation and stronger signal than would have occurred from the DAC output of the only 10MHz I/Q stream [20].

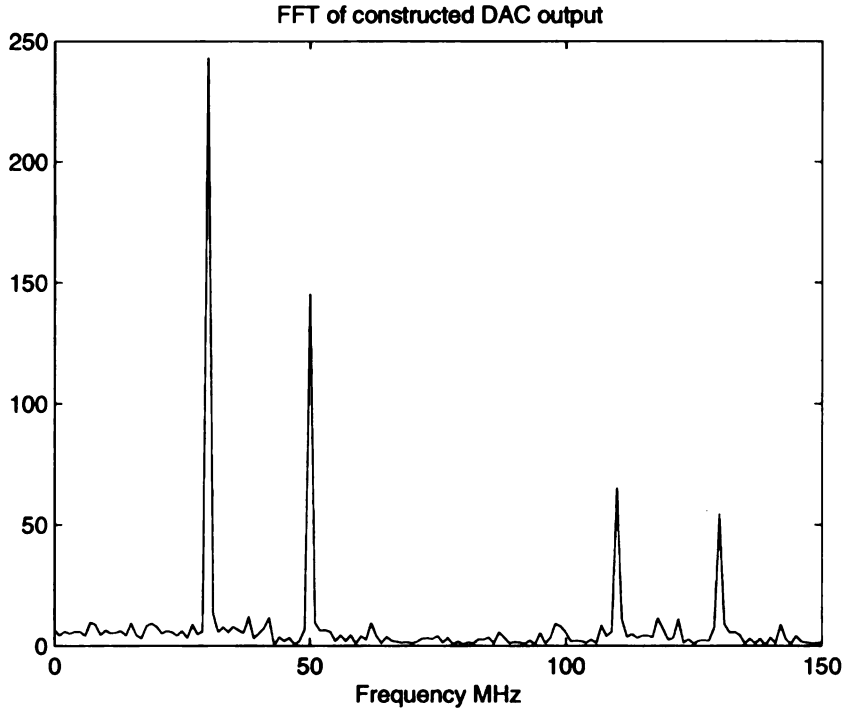

Figure 5.12. Frequency spectrum of DAC output with additional points.

The 50 MHz component being one of the largest components of the frequency spectrum, is band-passed filtered and up-converted with the original 755 MHz LO signal back up to 805 MHz to drive the cavity.

5.7 Conclusion

The compensator in the form of a digital proportional integrator has been detailed and followed step by step through a bit-wise flowchart. The compensator concept is simple, but its implementation, and the transfer of information from the FPGA to the host processor is not trivial. Methods for creating signals from a DDS, and generating the ouput analog signal are all implemented in the FPGA. A CORDIC routine is necessary to shift set points, ensuring the correct resonant frequency is synthesized. The PI loop compensates for the error and the integrator holds a history of values ensuring the proper output to the DAC. The result is a point-by-point compensator adjusting the RF drive signal to the cavity at a frequency of 10 MHz. If disturbances are not outside the range of detuning of the loaded cavity, this method will be able to ensure that 300Hz disturbances or microphonics are compensated for.

CHAPTER 6

Analog Signal Preparation

6.1 Introduction

Signals have thus far been labeled as cavity output, cavity drive and reference signal and have been referred to as the 50 MHz version of these signals. The cavity under test for this thesis operates at 805 MHz. To monitor and control the cavity, we are concerned with four signals which must exist at 805 MHz for cavity operation. The cavity drive signal is the compensated signal sent to the amplifier to drive the cavity. The cavity output signal is measured by a weakly coupled pick-up probe in the cavity and attenuated for our measurements. The forward drive signal measures the actual amount of the drive signal that is input to the cavity after the circulator, and the reflected signal is a measurement of the signal that is reflected from the cavity input. Both the reflected and forward signals are measured with directional couplers, where the output is isolated from the original signal and than attenuated for our measurements.

The SRF research group at NSCL have existing methods for measurement and control of the cavity. To obtain proper input levels, some signal level modification is required, while not interfering with the SRF groups measurements. This chapter discusses the requirements of the LLRF and the LLRF support chassis designed for appropriate signal level distribution.

6.2 Signal Level Requirements

The LLRF controller is housed in a chassis and contains a digital board and its own analog distribution. The digital board includes a StrongArm microprocessor, otherwise referred to as the host processor, the FPGA, the ADCs as well as all the circuitry supporting the digital processing. Supplying the analog signals to the ADCs is the analog distribution within the LLRF chassis, where the signals are split, amplified and filtered to ensure the levels are matched at each ADC. It is assumed that a specific level of signal is obtained and brought to the LLRF chassis. A copy of the LLRF analog schematic is included in appendix B. The LLRF chassis is designed to work for a specific frequency for a particular group of cavities. However, by changing band-pass filters to the appropriate frequency, the system can be adapted to work for lower frequencies than 805 MHz. The upper limit of the existing mixers limits increasing the operational frequency much above 805 MHz.

To obtain maximum control with the LLRF, certain input signal levels are required. Accuracy of amplitude and phase control is dependent of the resolution of the input levels. The maximum allowable input signal will give the highest digital resolution. LLRF input signals must pass through the LLRF chassis analog distribution. Table 6.1 is a list of the optimum input levels directly into the LLRF necessary to achieve the highest resolution. These values were obtained from the component schematics available from Berkeley (See appendix B).

Signal levels that are too high will saturate the ADC and rail the input values causing corrupted data. The LLRF IF signal can be within a range of power levels as PLLs are capable of picking up a very weak signal and maintaining phase lock.

The terminology of the inputs labeled on the LLRF are somewhat confusing, so we refer to IF, which is the reference signal as the 'LLRF IF', the LO as the 'LLRF LO', and the 'LLRF Output' which is the compensated cavity drive signal.

The goal of the 'LLRF support' design is to achieve the signal levels listed in table 6.1.

Table 6.1. LLRF Input signal labels and levels.

LLRF input/output	Description	Signal level required
IF	Reference 50 MHz	-33dBm to 3.5dBm
LO	Local Oscillator 755 MHz	3dBm
FOR	Forward Signal 805 MHz	10dBm
RFL	Reflected Signal 805 MHz	8dBm
CAVITY	Cavity Output 50 MHz	3.5dBm
OUTPUT	LLRF Output 805 MHz	varies

The expected signal levels from the cavity have been documented by the SRF group who have previously conducted experiments with the prototype cavity, and are listed in table 6.2. The cavity output and LLRF IF inputs are 50 MHz signals, which have been down-converted and filtered prior to the LLRF. The cavity drive signal generated within the LLRF is 50 MHz and requires the LLRF LO input to up-convert the output signal to 805 MHz for direct input to the amplifier. To maintain synchronization between all the cavities in the linac, the 50 MHz IF signal phase locks the ADC sampling clocks in the LLRF. The stability of the reference signal is crucial for the PLL to ensure the clocks are all phase locked.

Table 6.2. Anticipated output levels from cavity.

Signal		Power level
Forward Power (FOR)		10dBm
Reflected Power (RFL)		10dBm
Cavity Power (CAV)	up to	10dBm
Cavity Drive (OUTPUT)		20dBm

6.3 Reference Signal

Determining a reference system that is exceptionally phase stable across the linac to each controller is crucial in the design of the system. A method used at SNS requires the use of a reference signal of the same frequency of the cavities. This reference signal is in a strictly controlled temperature, humidity, and pressure environment, to ensure no phase drift occurs. This signal runs the length of the linac to the appropriate group of similar frequency cavities. At the location of the cavity pick-up probe, the reference signal is tapped and both the 805 MHz cavity output signal and the 805 MHz reference signal run together in parallel with the exact same cable lengths until they are down-converted by the LO signal. The cables are low loss, heat treated heliax phase matched cables to ensure there is no phase drift or additional attenuation in either cable [23].

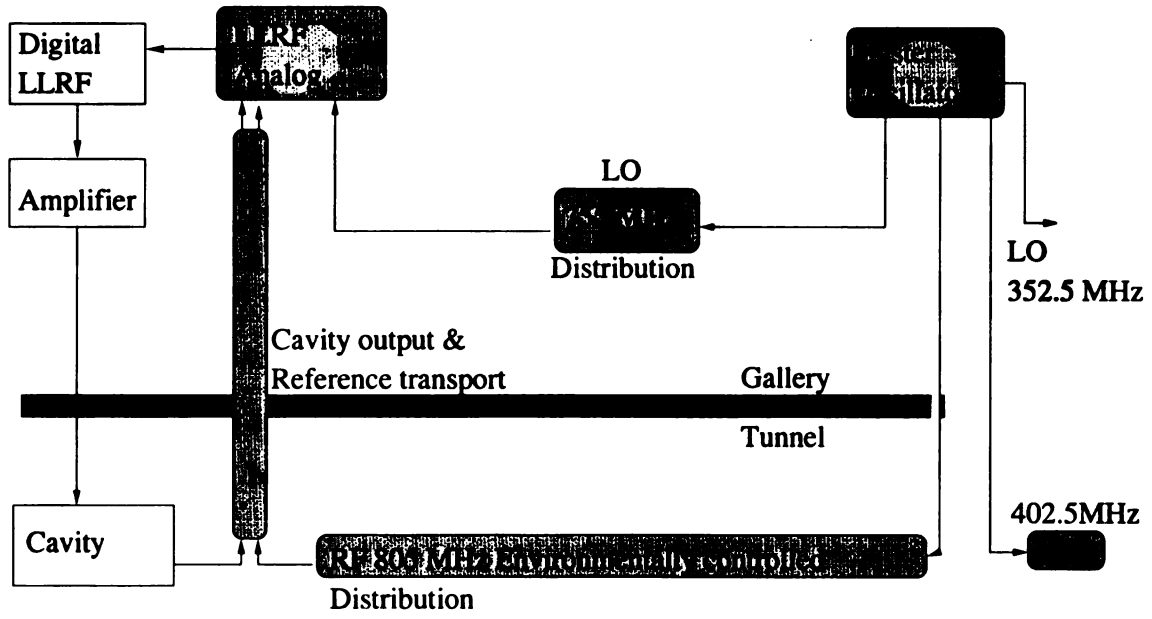

Figure 6.1. Example of reference distribution from SNS.

Interestingly the LO signal can be somewhat noisy without disrupting the system, because the noise appears in "common-mode" to all mixers. Imagine that the 805 MHz refer-

ence signal had a phase of ϕ, and the LO had a phase θ of its own of plus some additional unwanted phase of σ. Once the reference signal is mixed with the LO and filtered, the result is an IF that contains the unwanted noise σ at 50 MHz, as seen in equation (6.1). Then that signal is phase locked to the LLRF clock controlling the ADCs. The cavity output is clocked with the same phase of the reference including σ.

$$IF = \cos(\omega_{805MHz}t + \phi)\cos(\omega_{755MHz}t + \theta + \sigma)$$
$$IF_{(filtered)} = \cos(\omega_{50MHz}t + \phi - \theta - \sigma) \tag{6.1}$$

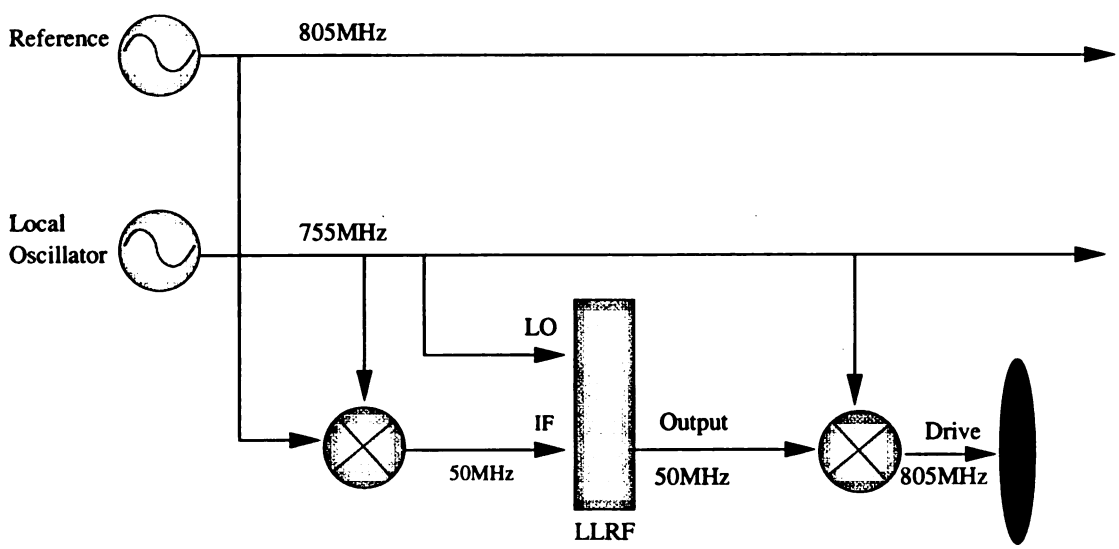

Figure 6.2. Mixer downconversion and upconversion using noisy reference.

The output of the LLRF is a 50 MHz compensated signal that has been phase locked to the LLRF IF signal by the DAC clock, and still carries with it the additional unwanted phase σ. The 50 MHz compensated output is than mixed with the 755 MHz reference signal again and labeled as the drive signal in figure 6.2, where the noise is subtracted out and the final output has only the original phase θ, as seen in equation (6.2).

$$RF_{(Drive)} = \cos(\omega_{50MHz}t + \phi - \theta - \sigma)\cos(\omega_{755MHz}t + \theta + \sigma)$$

$$RF_{(Drivefiltered)} = \cos(\omega_{805MHz}t + \phi) \tag{6.2}$$

Other methods are possible for generating a stable reference signal, such as using the beam itself as the reference signal, in which case a similar analog donwconversion is necessary. In the design of the LLRF support, we took into account that the reference signal would be a fixed frequency such as the SNS model. The downconversion of the reference signal to 50 MHz for the LLRF occurs in the support chassis.

6.4 LLRF Support Chassis

A separate chassis is necessary to contain the analog signal setup prior to the LLRF. The LLRF support chassis was designed to serve multiple purposes. Firstly, a general location is needed to contain the mixers for down-conversion of the signals to 50 MHz. Secondly, the support chassis includes test points for the cavity and reference signals at both 50 and 805 MHz. Finally, there was a desire to allow the SRF research team to use their existing testing procedure totally independent of the LLRF. The MSU SRF group designed and built a prototype cavity at the NSCL. Their method of control was to move the resonant frequency via FM modulation of the drive signal. The modulation is the error signal from the cavity input relative to the cavity output. This method is more in line with a self excited driven system, whereas the LLRF operates strictly on a generator driven loop. In order to not complicate any testing on their behalf, it was important to leave the opportunity to disconnect our LLRF support and situate our control module completely out of the loop, guaranteeing that no reflection or transmission of any signal from our system could interfere with their existing test stand. N-type connectors are available for the SRF group to conduct

tests while the LLRF controller operates. Alternatively, independent signals are available for their testing by simply changing three N-type connectors.

6.4.1 Overall Implementation

The basic implementation of the support chassis can be broken into various groups of input/output signals. Figure 6.3 is a representation of how the support chassis fits into the system and the following descriptions of the groups will help identify their purpose.

1. The cavity, amplifier and associated signals.
2. LLRF signals.
3. Testpoints, 50 MHz and 805 MHz cavity and reference.
4. SRF monitor.
5. Reference input signals.
6. Feedthrough panel.

The first group, 'Cavity signals' require an output driving signal compensated to keep constant fields in the cavity. Inputs to the support chassis are forward and reflected signals as well as the cavity output signal. All connectors are N-type to ensure proper connection especially with the higher power cables.

'LLRF signals' are all the input and output between the support chassis and LLRF. They include the LLRF LO, LLRF IF, LLRF cavity, LLRF forward, LLRF reflected, and LLRF output. Each has a specific frequency and an optimum signal level, as discussed in a previous section. All support feedthroughs are SMA while the LLRF has its own PkZ connector.

The group 'labeled testpoints' are SMA outputs to verify the control of the cavity by comparing the reference signal to the cavity output at both 805 MHz and at 50 MHz. Ideally, as a performance standard, this is where we can determine the accuracy of the LLRF controller.

The SRF group has methods of verifying cavity dynamics that are out of the scope of the LLRF and this thesis. A set of signals are distributed to 'SRF Monitor' by N-type connectors, immediately after entering the support chassis to supply an unaltered copy of the cavity signals to the SRF group.

The intended location of the support chassis is in a rack that contains the LLRF controller and the cavity amplifier. Above the support chassis will be a feed-through panel where the cables directly from the cavity will be connected. Using the LLRF controller, connectors from the feed-through to the support chassis will be installed. To allow for complete disassociation with the LLRF, the SRF group can obtain cavity signals directly from the feed-through panel.

6.4.2 RF Design Techniques

A main consideration in the analog design was to isolate the signals as much as possible. Directional couplers were used when signal levels allowed, to take advantage of the isolation in the coupled port. Occasionally it was necessary to use splitters because the signal levels were not high enough to undergo the attenuation of the coupler, and still be effective. High level mixers were necessary to maintain a relatively strong intermediate frequency that could be used without further amplification in pursuing stages. Mixers also have a tendency to transmit and reflect harmonics of both the input and output values. In order to reduce the effects of the mixer dynamics, a pad or an attenuator is positioned both prior to and after the mixer, in addition to the filters necessary to eliminate sidebands and unwanted multiples of the inputs.

For our test set-up we used signal generators to produce both the 805 MHz signal and the 755 MHz LO signal. In order to achieve the appropriate mixer input levels for the LO we need a minimum 20dBm output from the signal generator. Our HP 8647A signal generator has a maximum output of 13dBm. In considering potential realities of a reference signal input, it was decided that an amplifier was necessary for the LO signal to achieve

the necessary levels throughout the chassis. Of course, where there is an amplifier, a power supply is needed. A power switch, fuse and indicator light are also incorporated into the design.

6.5 Schematic

The majority of the RF components were purchased from Mini-Circuits. The frequency range for each component was available including the amplifier. Only the 50 MHz bandpass filter did not meet requirements regarding roll-off. SIF-50 BPF from Mini-Circuits, has 10dB attenuation at 11.5 and 200 MHz. The Mini-Circuit 50 MHz BPF was available and reasonably priced. In pricing out low quantity BPF with high drop off, the cost seemed prohibitive, so we used the lower grade, wider bandwidth filter from Mini-Circuits. In testing the LLRF, we did not see the affects of sidebands from the mixer output.

The 755 MHz LO signal is amplified with a Mini-Circuits ZHL-2 amplifier to obtain the correct signal levels for the Mini-Circuits ZP-5H, level 17 mixers. The high level mixer is required to maintain some reasonable signal level for the following stages. The 755 MHz LO signal mixes with both the 805 MHz signal from the cavity and the 805 MHz reference. The resulting 50MHz signals are split to the LLRF and testpoints for verification. The ZHL-2 amplifier has a gain of 17.2dB and a maximum output of 29.4 dBm.

Main points of the schematic are that all signals are split to allow the controller to function and allow some verification as well as allow for further testing during cavity operation.

6.6 Conclusion

An analog support chassis has been built to house the downconversion and distribution of the required signals for the LLRF controller while allowing other research members to analyze output concurrently. N-type connectors also allow other researchers to completely

eliminate the LLRF support and controller and use a fundamentally different control technique.

Testing with support chassis allowed us to verify the accuracy of the controller with the new testpoints of reference and cavity output. We were encouraged by the available data, and did not observe additional noise factor attributed to by using the support chassis.

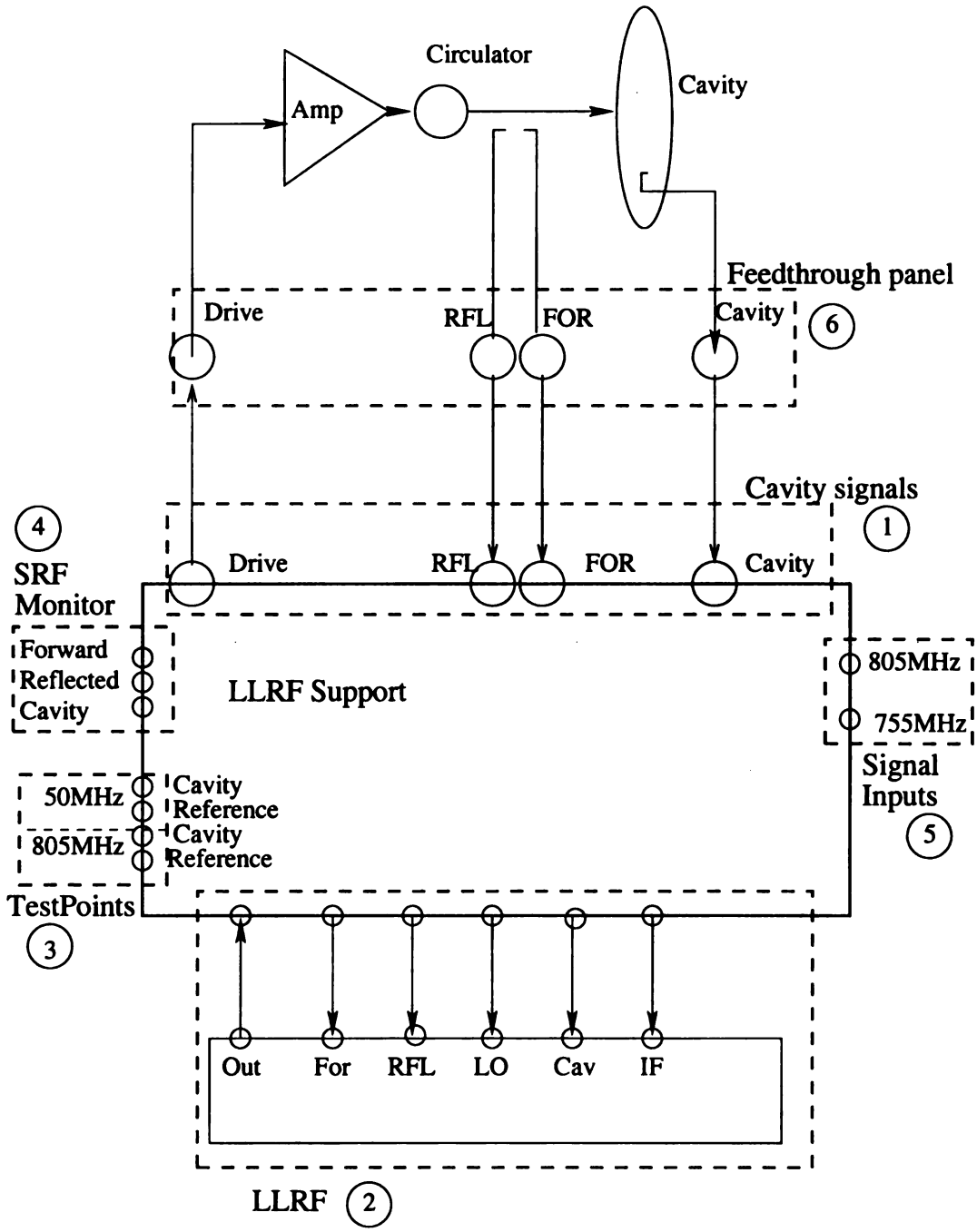

Figure 6.3. LLRF support chassis block diagram.

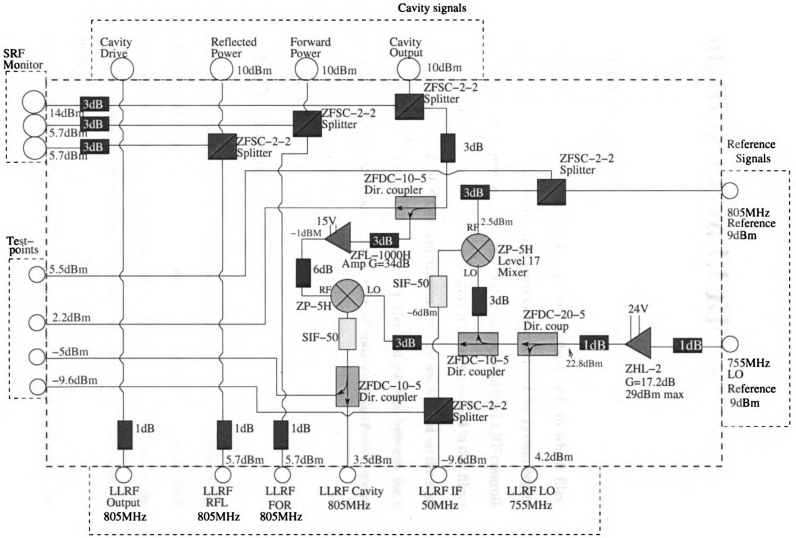

Figure 6.4. LLRF Support chassis schematic.

CHAPTER 7

Link from PC to LLRF

7.1 Introduction

A sequence of events occur during the boot-up of the LLRF, in which files are loaded, interfaces established, data input/output ports connected and the system begins to operate. There are three main computers involved to start and operate the LLRF controller at NSCL. The system implemented at the NSCL is slightly more complicated in that files necessary to load the LLRF and the EPICS GUI application files are not located on the same computer. For a better understanding of information transfer and the link between the user and the controller, this chapter describes the relevance of individual hardware systems and their relation to the LLRF controller.

7.2 SUN Station

When the LLRF boots up, the on-board microprocessor loads a version of Linux from its limited ROM and is directed to look for more files to continue its boot-up. At NSCL, these source data files reside in a Sun Station for the LLRF. It loads the source files via TFTP, and the LLRF continues its boot up. The LLRF microprocessor then begins to operate as an EPICS server.

At the NSCL, other EPICS files also reside on the Sun. The Sun Station is not dedicated to the LLRF, and contains its own operating system providing EPICS files applications to other parts of the lab. Files are simply loaded into the LLRF from the Sun Station. Once

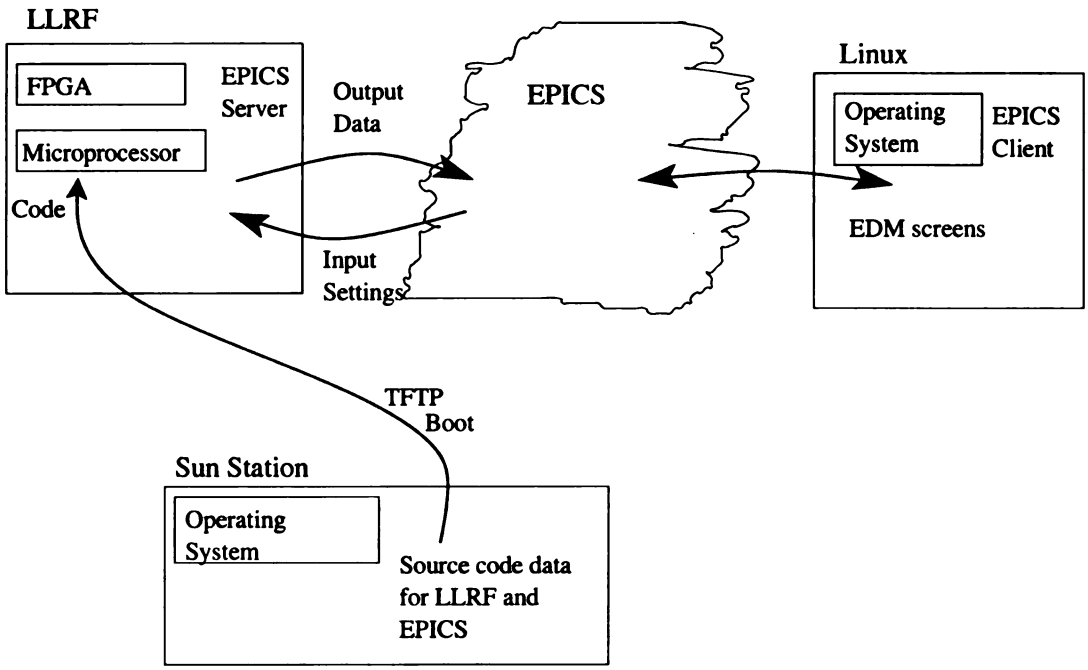

Figure 7.1. Relationship between hardware components.

boot-up is complete, there is no further interaction with Sun.

7.3 EPICS

Experimental Physics Industrial Control Systems (EPICS) is software, and applications that enables the monitoring of data and adjustment of system parameters in real time. Initially designed at Los Alamos and Argon National Labs for use in large research institutions, the EPICS system is used in accelerators and astronomical research facilities around the world.

EPICS is capable of networking many computers to transfer real-time data, and making adjustments to any component throughout the system via Channel Access (CA) network protocols. There are many EPICS applications that are available, incorporating many types of other possible hardware and interfaces such as Matlab.

Within EPICS, the data transfer is server and client based. Once the LLRF is operating

it acts as an EPICS server exchanging data from the FPGA to the GUI on the Linux Station. EPICS sits in the middle overseeing all commands and monitoring data as a distributed data exchange mechanism.

7.4 Linux

Our Linux system resides on a PC, which is referred to as the Linux PC. It also is a non dedicated computer which houses the LLRF EPICS user files and acts as a EPICS client to the LLRF EPICS server. The Linux PC is where the EPICS interface and GUI screens are stored and manipulated. The EPICS GUIs can be written in various formats. The screen shots for the LLRF controller are in EDL format and stored in the Linux PC. From the EDL GUIs, EPICS channels may be read or set. The EDL screens are located and are accessible from the Linux PC or any remote computer linked over Ethernet connection.

The alternate method of set-up is to have all the source code for the LLRF in the Linux PC thereby eliminating the need for the Sun Station. When this project was first established at the NSCL, some Linux applications had not been installed on the Linux PC, such as the TFTP transfer protocol. This made the present set-up the simplest to establish.

7.5 StrongArm

A StrongArm microprocessor (MP) works in tandem with the FPGA. Often referred to as the host computer, the StrongArm operates at 200 MHz, and contains multiple inout/output pins including an ethernet port. The MP is able to load files from an ethernet connection, and transfer data back and forth to the FPGA, via a 16 bit direct bus. The combination allows the FPGA to perform its high throughput without loading it up with heavy architecture. The MP provides support in both supplying C code functions to the FPGA and handling data transfer to and from the FPGA.

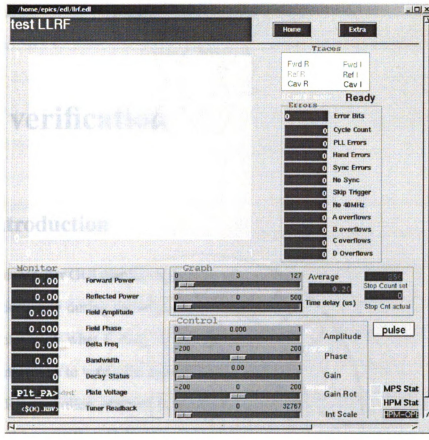

Figure 7.2. Example EDL screenshot.

7.6 Field Programable Gate Array

The Field Programable Gate Array (FPGA), is a programmed logic device with many thousands of logic gates. Its high throughput provides realtime measurements and controls digital control loop in the LLRF controller. It suffers one large drawback. The FPGA is coded in verilog, of which few programmers at NSCL are familiar, making it difficult to decipher manipulate or troubleshoot through code.

CHAPTER 8

Data verification

8.1 Introduction

The LLRF controller GUI displays the cavity output signal and is the measure of the degree of control occurring during normal operation. Our goal is to confirm that the LLRF GUI data correlates with what is truly occurring in the cavity. This chapter contains several experimental results to verify the controllers performance.

The LLRF controllers function is to compensate for disturbances perturbing the cavity. Identifying the controllers performance and compensating bandwidth is needed to ensure it meets with RIA specifications. A research group at NSCL has determined that phase regulation of better than 0.5°, and amplitude regulation better than 0.5%, is required to meet the performance needs of the overall linac [3]. The accuracy of the cavity will be set and adjusted for during calibration of beam operation, but the controller must be able to regulate at least up to the values specified.

In order to test the LLRF controller, equipment accurate enough to measure voltage levels near the noise floor is necessary, because a regulated cavity has a very small phase error. Equipment used for testing included a Vector Network Analyzer (VNA), a Vector Volt Meter (VVM) model HP 8508A, and a Stanford Research model SR844 Lock-in-Amplifier (LIA). The VNA functioned well in some circumstances and not well in others due to the complexity of the signal distribution. The VVM was used to verify output as long as the signal strength was large enough to lock on to. The resolution of the VVM is 0.1° with an accuracy of $\pm 3°$ from the specifications. A Lock-in-Amplifier was used as an

alternative to the VVM, which is capable of locking onto a lower minimum signal strength. The LIA accuracy specified to be ±0.25dB in magnitude, and with an absolute phase error of less than 2.5°. Absolute normalized amplitude accuracy relative to the LLRF set-points is limited to 5.7%. The resolution of the data is displayed to 0.01dB and 0.02° [22]. Finally, the DC intermediate frequency of a level 17 mixer was used to compare the reference and cavity output signals at the same frequency. An amplified and filtered version of the mixer output was analyzed on a digital oscilloscope.

In each test, the reference signal was compared to the cavity output signal. Testpoints on the front of the support chassis enabled easy access to each signal. Signals were occasionally retrieved interior of the chassis, prior to the panel connections to ensure no loss of signal in the connectors. The SRF N-type connections were also available to take simultaneous measurements.

In general the test set-up appeared as in figure 8.1 and the components are listed in table 8.1.

Table 8.1. List of components used in test.

Component	Manufacturer	Model number
Signal Generators	HP	8647A
Amplifier	Mini-Circuits	ZFL-1000H
Isolater	UTE	CT-1057-OT
Bi-directional Coupler	Mini-Circuits	ZFBDC20-900HP

The first set of tests are a simple demonstration of the controller operation by a 'bead pull'. The second set of tests are a more detailed analysis of the controllers performance to correct phase error measured from a perturbed multi-cell copper cavity. The third set of tests are a comparison of the amplitude output relative to the set-points. The GUI, VNA and LIA amplitude outputs are plotted together illustrating the consistency between

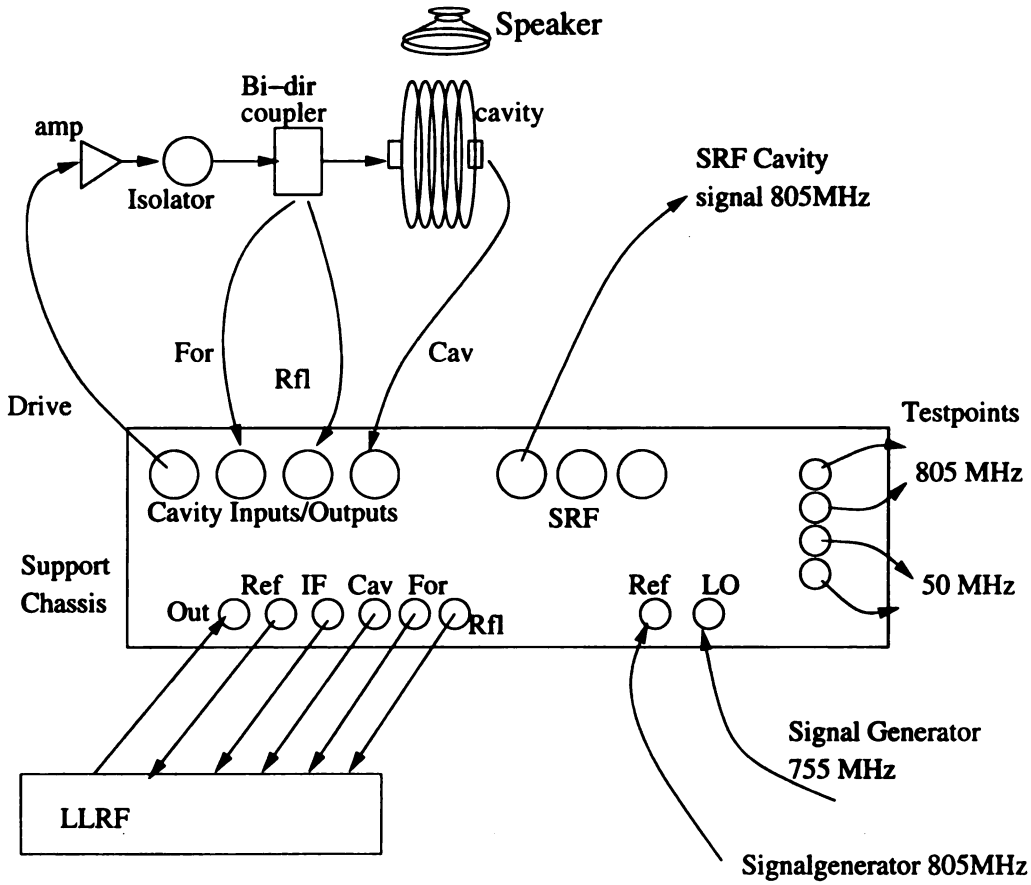

Figure 8.1. Test set-up for support chassis.

measurements.

8.2 Bead Pull

Initial operation of the LLRF controller included a bead-pull test on a single cell copper cavity. A metallic bead pulled through the cavity causes a disturbance on the electric fields inside the cavity, perturbating the cavity resonant frequency and linearly represented by a phase change. This demonstrates the LLRF controllers ability to compensate for low frequency perturbations to the cavity.

The LLRF was calibrated prior to the bead pull, as described in the Appendix A. A

metal bead on a fishing line was suspended through the center of the cavity and mechanically passed from one end to the other with a constant speed. The VVM is used to monitor the phase difference between the reference signal and the cavity output.

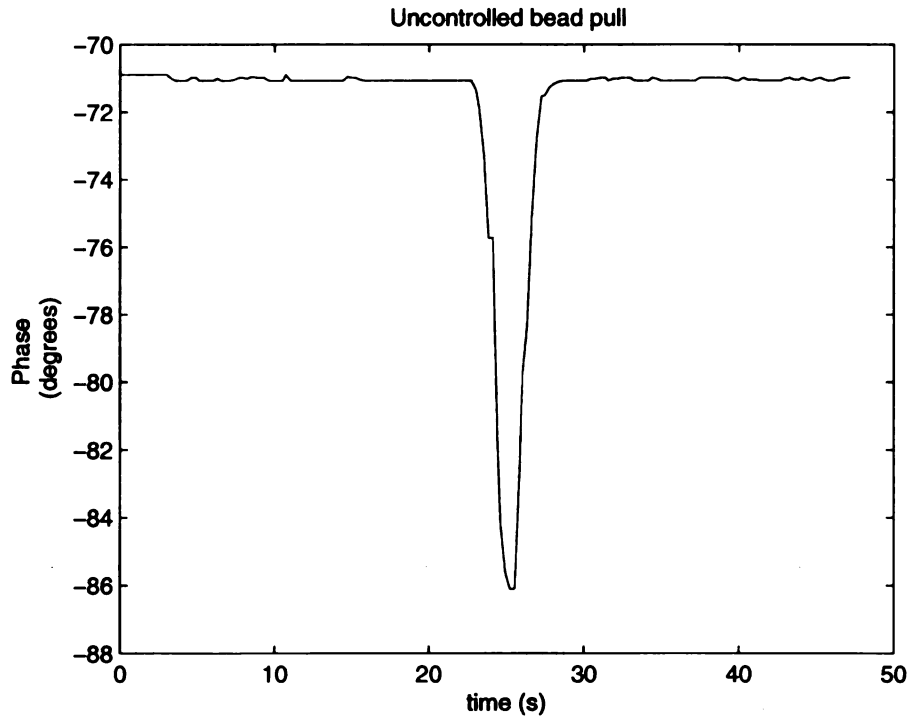

Figure 8.2. 15.1° phase disturbance from an uncontrolled bead pull.

The single-cell copper cavity has a $Q_u = 15000$, and has a resonant frequency of 808.02 MHz. During an 'uncontrolled bead-pull', a phase change of 15.1° was measured when the bead passes through the geometric center of the cavity with the LLRF controller not regulating the signal, as seen in figure 8.2. The phase measured during the 'controlled beam pull', with the LLRF regulating the cavity input signal is shown in figure 8.3. The regulated cavity has a relative phase error of approximately 0.12°.

These plots demonstrate the simple case of a single cell with a compensated drive signal and the resulting controlled phase. Qualitatively, they do not contain information about the

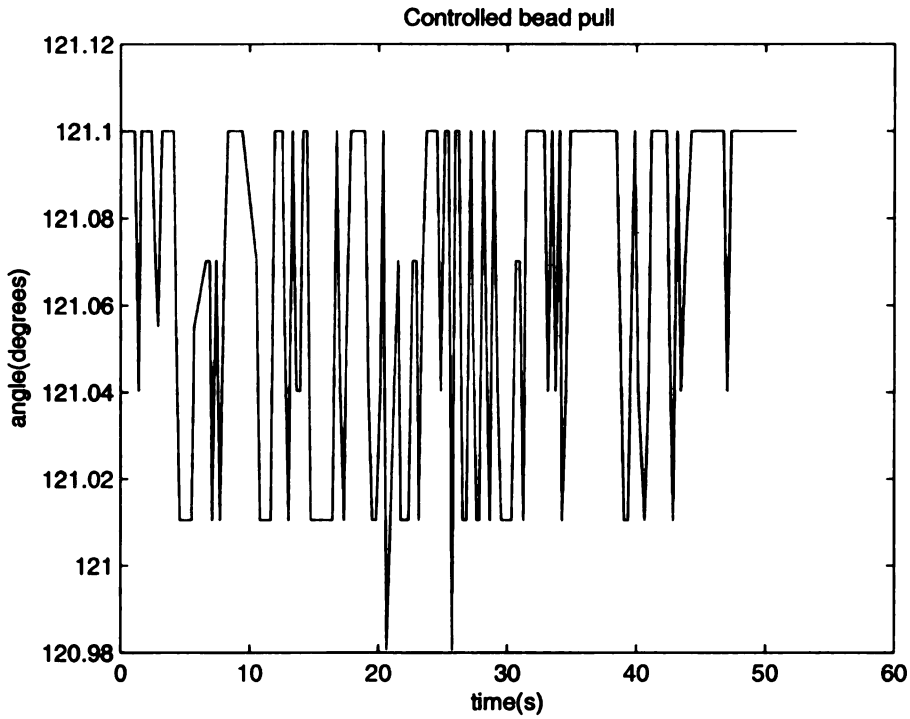

Figure 8.3. 0.12° phase disturbance from a controlled bead pull.

bandwidth or accuracy of the controller. For this we move on to the multicell cavity tests using various methods of measurements.

8.3 Performance of Phase Compensation

A five cell copper cavity was set up with the LLRF controller to run in a simulated environment. The cavity output and reference signals from the support chassis are compared to determine the phase error of the cavity. Measurements were taken with the controller operating in the regulated and unregulated modes as well with, and without a disturbance applied to the cavity. The goal of these tests was to verify testing methods of the phase error and verify the performance of the LLRF in maintaining phase stability.

The five cell copper cavity has a Q_u of 11700, and operates at 805.740 MHz with a

bandwidth of 69 kHz. The large bandwidth allows the LLRF to operate over a larger range. There are limitations to LLRF compensation outside the cavity bandwidth. A speaker mounted on the frame supporting the cavity is the source of perturbations. A separate signal generator and amplifier induces any frequency through the speaker. It was determined by a frequency sweep, that the cavity develops its strongest mechanical perturbation at 40Hz.

The phase change occurring in the cavity is measured by comparing the cavity output signal relative to the reference signal, and plotted with respect to time. The swing from maximum phase offset, to minimum phase offset is referred to as the phase error. Figure 8.4 has a measured phase change of about $\pm 9°$ over a period of time, so the phase error is approximately 18°.

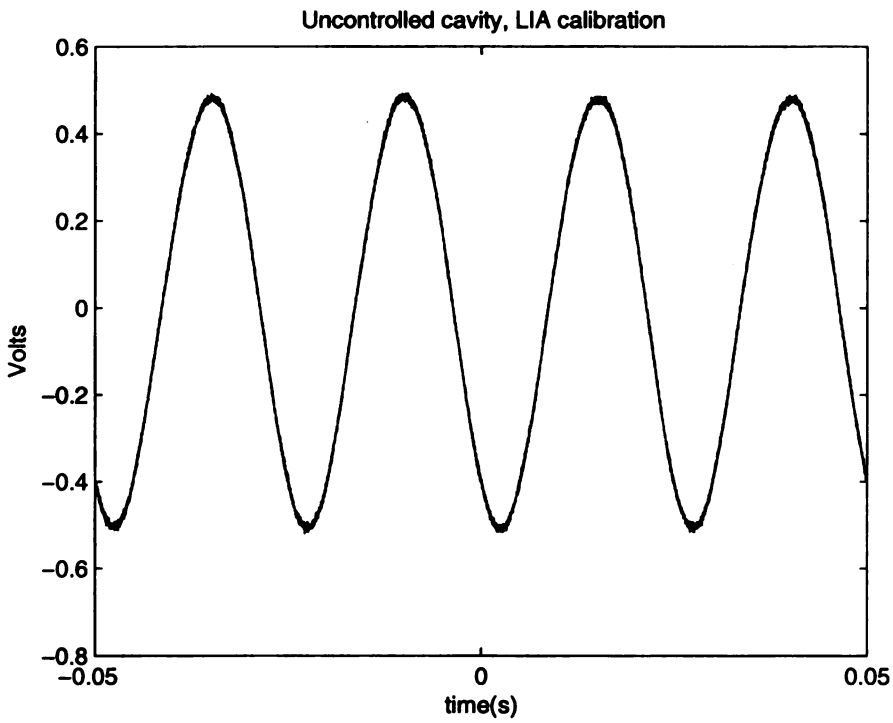

Figure 8.4. Cavity phase measurement with Lock-in-Amplifier at 18°.

While three different measurements were taken, two measurements are referenced to

each other for calibration. The first measurement is directly from the LLRF GUI, which is a measurement of the phase error from the EPICS data, and is referred to as the 'EPICS reading'. The 'EPICS reading' is real-time, averaged data directly from the FPGA displayed on the LLRF GUI. The phase error is determined from the peak-to-peak values of the GUI screen shots.

A second measurement was obtained from the 50 MHz support chassis testpoints, with the Stanford Research SR844 Lock-in Amplifier (LIA). The settings for the LIA were adjusted to output the phase relative to the reference. The 50 MHz reference signal was the reference input of the LIA, while the 50 MHz cavity output signal was connected to channel A of the LIA. The LIA analog output was the measured phase error of the cavity, and was measured on a digital scope.

The third measurement is the 805 MHz cavity and reference signals from the support chassis testpoints. Both the cavity output and 805 MHz reference signal were mixed together via a level 17 mixer, creating an IF that is the phase error of the cavity. The IF was sent through a homemade audio amplifier, filtered and measured on the digital oscilloscope, where the captured data was later recreated in Matlab for study. We refer to this mixer output as the "805 mixer error". The amplification and filtering of the error signal allows for more accurate measurements of the regulated phase.

The homemade audio set-up is a simple circuit containing a MOT 33071AP op-amp with variable amplification and a passive low pass filter with a corner frequency of 100 Hz. The circuit is housed in a box and is easily connected with BNC connectors. The variable gain introduces a problem in that the gain is not truly known. A method of calibrating the amplified gain is necessary to use the mixer output as a measurement of phase error at low levels.

To determine the amplifier gain, a second signal such as the LIA error signal or the EPICS reading was used for comparison. By comparing a known amount of phase error, to 'the 805 mixer' voltage, a ratio of $\frac{degree}{V}$ can be determined. This calibration factor is

a linear representation of the amplifier gain and is used to determine the phase error for future '805 mixer error' measurements.

The LIA has a range of ± 10 Volts; hence the full-scale reading of 360° spans 20 Volts. The peak-to-peak value of 1.012Volts measured from the 'Uncontrolled cavity LIA' test of figure 8.4 is a direct measurement of the phase error and equates to 18.216°. By comparison, EPICS peak-to-peak value is approximately 18.18° confirming the LIAs relative phase error values.

Meanwhile, the '805 mixer error' is amplified, filtered in the homemade audio circuit, and measured with a digital oscilloscope. This '805 mixer' measurement, seen in figure 8.5, is taken simultaneously with the previous 50 MHz LIA phase measurement 18.216°. Comparing the two measurements enables for calibration of the 805 MHz 'mixer error' signal. In this case, the calibration results in the ratio of $\frac{3.462°}{V}$. A higher relative accuracy of the phase error can be determined from the '805 mixer error' measurements since the signal is amplified and filtered to clear the noise floor.

Continued measurements from the LIA and '805 mixer error' are used to compare phase errors ensuring correct calibration of the amplifier gain until the LIA can no longer find or lock to the signal. In which case the '805 mixer error' will be used and compared solely to the EPICS readings. Once the values have been calibrated and verified with other measurements, the mixer becomes the better testing tool.

To this point all measurements have been utilizing unregulated cavity operation. Under the identical setup and with the same disturbance applied, the regulated cavity response measured by the mixer output was $V_{(p-p)} = 15.2mV$, and can be seen in figure 8.6. The phase error is then

$$0.0152V \times \frac{3.462°}{V} = 0.0526°$$

The LLRF controller demonstrates its performance by controlling the disturbance from 18.216° to 0.0526°. The phase error at this level cannot be measured below 0.0526° pri-

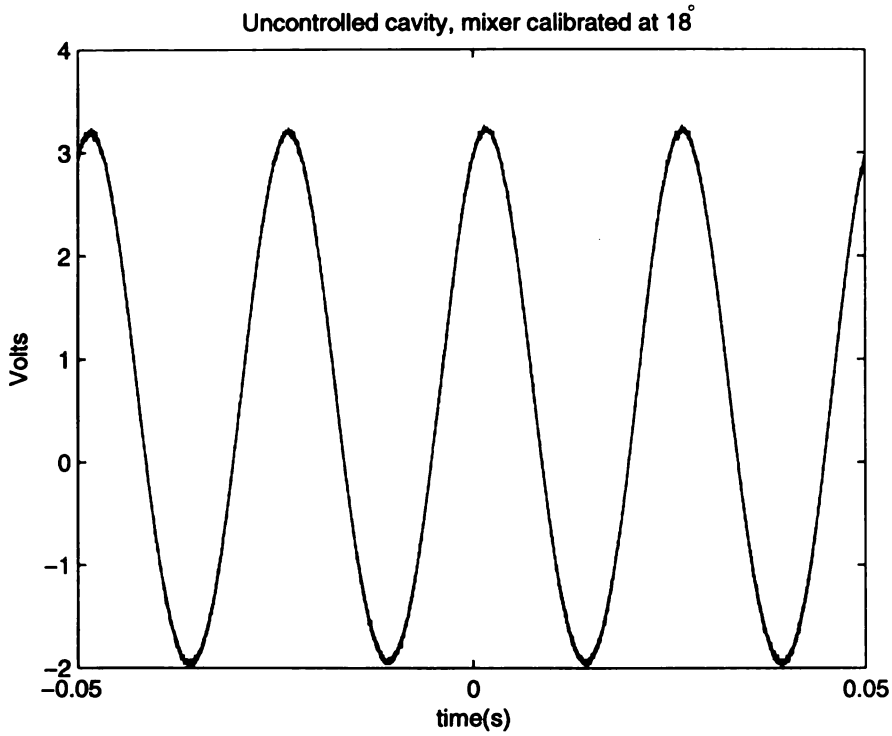

Figure 8.5. '805 mixer error' measurement at 18.216°.

marily due to noise in the system.

Results of the phase error when no disturbance is applied to a regulated cavity are shown in figure 8.7. The peak-to-peak value of the '805 mixer error' output is 0.013V. Using the calibration obtained earlier, we calculate the phase shift to be

$$0.013V \times \frac{3.462°}{V} = 0.045°$$

of phase error. In comparing the measured phase error of a regulated cavity with a disturbance (0.0526°) and without a disturbance (0.045°), the controller maintains approximately the same phase to within 0.01° over a varied level of disturbances.

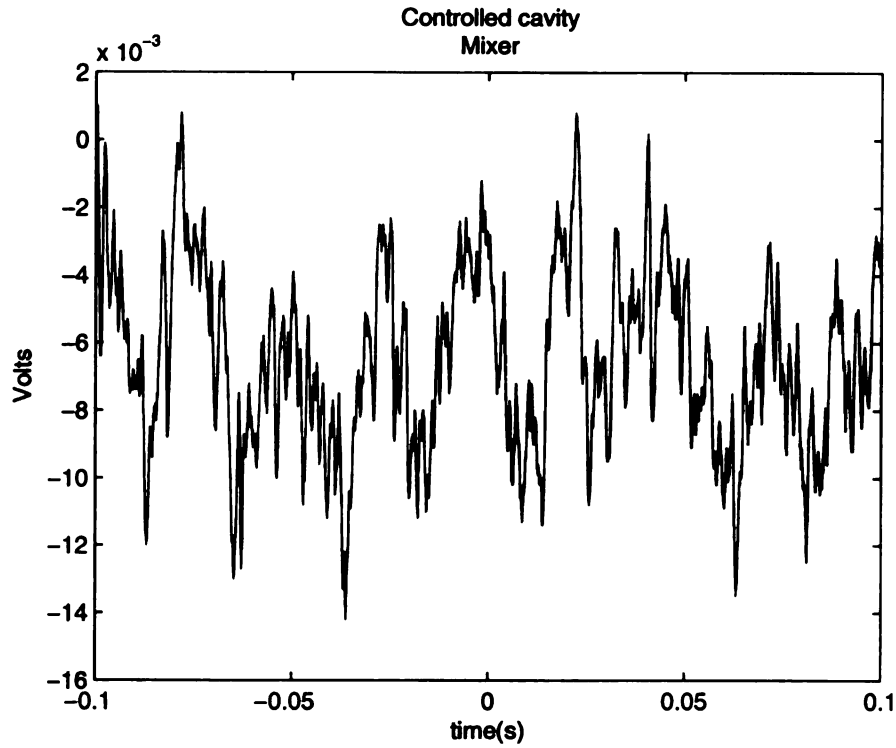

Figure 8.6. Controlled cavity mixer error measurement of 0.0526°.

8.3.1 Noise Floor

To determine how much noise is in the electronics, the cavity was replaced with a 10dB attenuator. Vibrating disturbances will have no effect on the attenuator, ensuring all other noise issues originate from the cabling and RF components incorporated into the support chassis.

Tests were performed in the same manner as previously described, with the attenuator to determine the phase noise of the system. The phase measurements are shown in figures 8.8 and 8.9. Note that with the controller running, the phase error is reduced from 0.1198° to 0.658°, for a difference of 0.054°. As only the attenuator is in-line, the measured difference between the regulated attenuator and the unregulated attenuator must be noise within the set-up. The set-up noise of 0.658° was regulated in the second test, and can be attributed to cables, amplifier, circulator, bi-directional coupler, and is referred to as 'interior

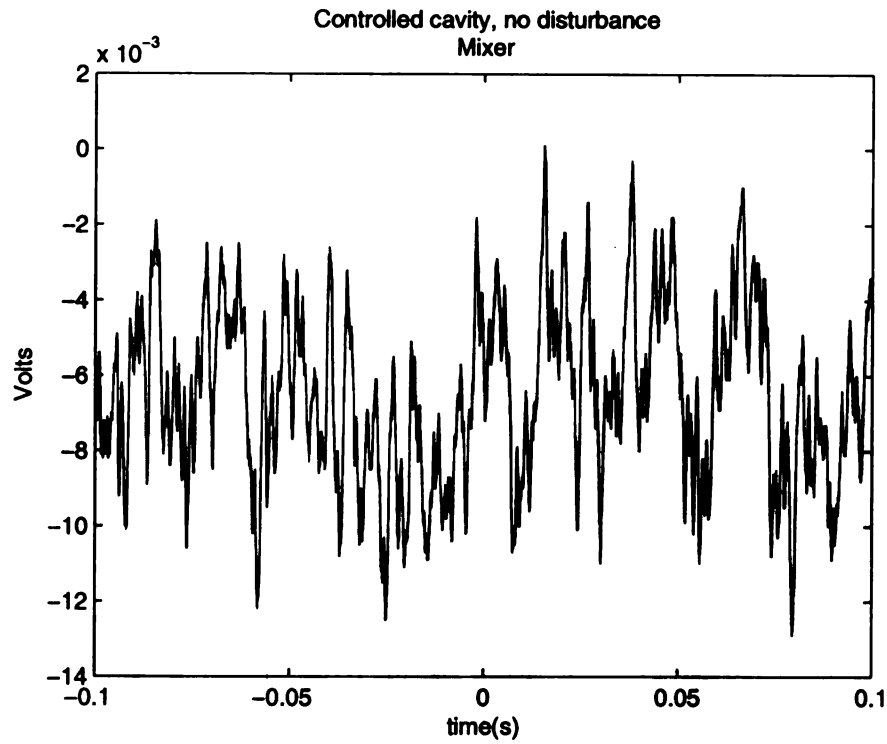

Figure 8.7. Controlled cavity with no disturbance resulting in 0.045° error.

electronics'. The remainder noise level must be the noise floor of the system as measured. We can conclude that the system has a inherent measured noise level of 0.054° regardless of the configuration.

In order to conduct the tests with the attenuator rather than the cavity, the controller parameters had to be changed. Replacing components or cable set-ups requires re-calibrating GUI parameters to obtain the best gain vs stable operation. As the controller parameter levels may not match levels in previous tests, the resulting data may vary slightly. Additionally the attenuator output signal levels to the support chassis were not identical to the cavity output signal levels. Although every effort is made to match signal levels for each test, mismatched signal level would also vary output. It is for this reason that results vary for tests that require different components. We are not able to achieve consistent results as low as the controlled cavity in figure 8.7. Although there exists variability in the test re-

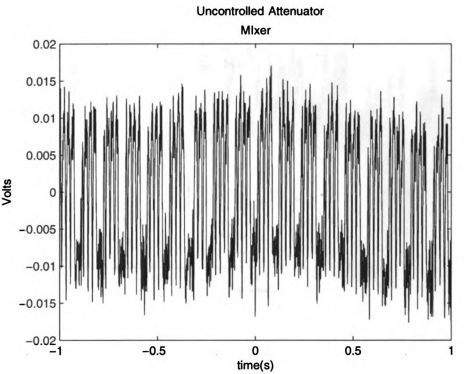

Figure 8.8. Phase error of uncontrolled attenuator equates 0.1198°.

Table 8.2. Measured noise of the attenuator.

Attenuator	$V_{(p-p)}$ 805 mixer error (V)	Calculated Phase error (°)	EPICS (°)
Controlled	0.0156	0.05401	0.06
Uncontrolled	0.0346	0.11978	0.102

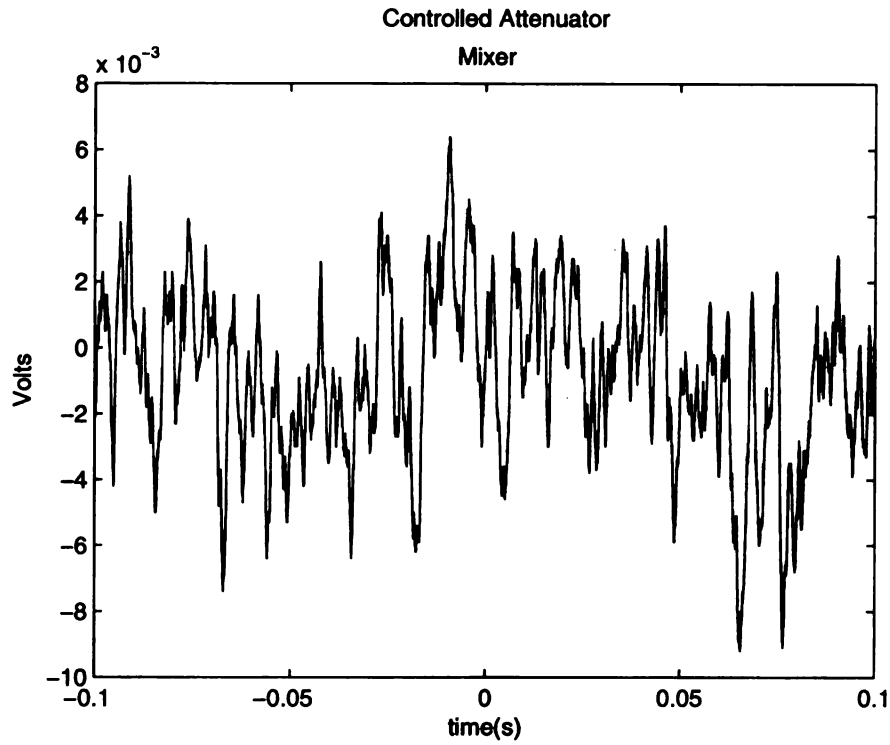

Figure 8.9. Phase error of controlled Attenuator equates to 0.054°.

sults, the level of measured accuracy is within 0.02° which is better than the requirements demanded.

The independent testing of output with alternate equipment was performed to ensure the LLRF GUI output is correct. The LIA used, has an accuracy level to only 2.5°, therefore we can only base these measurements relative to the resolution of the test equipment. The comparison of the calculated '805 mixer error' phase errors, relative to the EPICS GUI readings are listed in table 8.3. Variance between measurements was better than 0.064°, which is within RIA specifications. The results indicate a margin of error exists for low-level phase measurements below the noise floor. The noise floor of 0.05° means we are limited in our measurements, and that the controllers accuracy cannot be measured below 0.05°. The relative phase measurement based on resolution relative to EPICS are within 0.064°. The EPICS levels indicate a better level of performance that cannot be absolutely

ascertained.

Table 8.3. All phase errors, measured vs calculated.

Applied Disturbance		$V_{(p-p)}$ '805 mixer error' (V)	Calculated Phase error (°)	EPICS (°)	EPICS vs. mixer
Yes	Uncontrolled cavity	1.012	18.210	18.18	0.03
Yes	Controlled cavity	0.0152	0.0506	0.023	0.028
No	Uncontrolled cavity	0.0618	0.2139	0.15	0.064
No	Controlled cavity	0.013	0.0450	0.016	0.035

8.4 Amplitude performance

Analysis of amplitude performance is achieved by measuring the power output of the cavity with three pieces of equipment, the vector network analyzer, lock-in amplifier, and the on-board EPICS readings. Our concern is not the accuracy of the cavity output by a nominal value, but rather the output relative to the set-points. Each cavity may have a degree of offset, which will be reset during calibration of the beam. The beam operator will calibrate any offset in the performance of the beam by resetting the LLRF parameters as necessary. Once the beam is operational with proper cavity calibrations, it is necessary that the controller regulates the cavity to with the specified degree of accuracy.

Amplitude performance tests were performed in a similar manner to phase error testing. A Vector Network Analyzer (VNA), HP8714C, was included for amplitude testing. The VNA is an accurate tool to measure cavity transmission and reflection signals. The VNA accuracy is 0.03dB for peak to peak magnitude measurements which is normalized

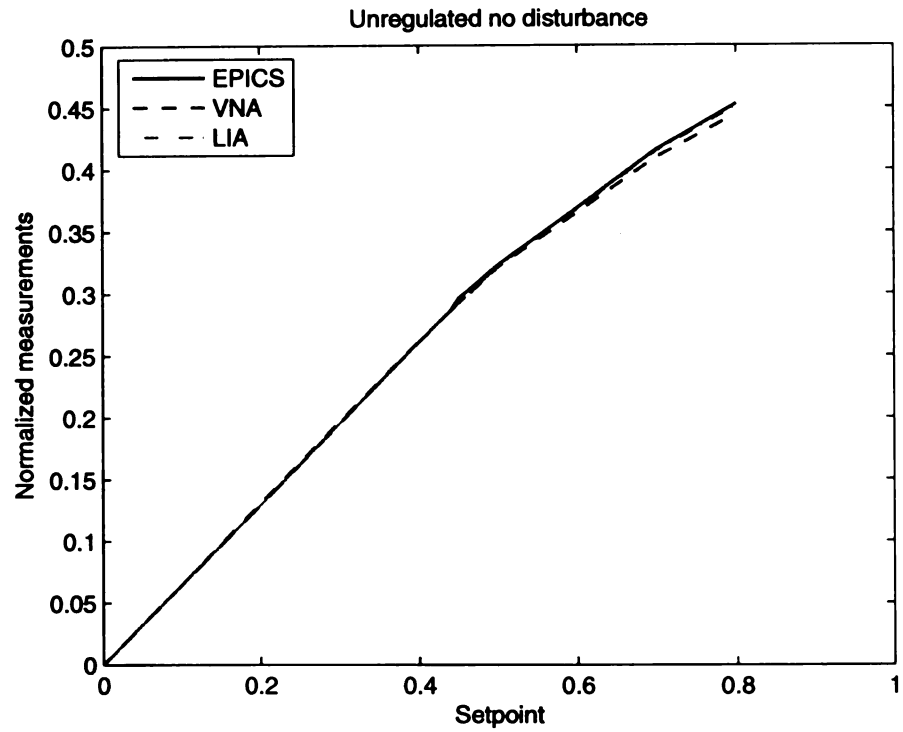

Figure 8.10. Amplitude measurements vs. set-point, uncontrolled and no disturbance.

to 0.35% in amplitude relative to the LLRF set-points. The phase accuracy for the VNA is 0.2° for phase measurements. Its display resolution is as low as 0.01dB/div in magnitude, and 0.1°/div for phase measurements [21]. Unfortunately, it must be connected as a signal source to obtain transmission measurements. VNA features such as 'frequency sweep' are problematic when the reference signal is downconverted to the LLRF IF signal in the support chassis. The sweep would consequently affect the LLRF IF. Any change on this reference signal has detrimental effects on the overall control. It is absolutely necessary that the reference signal is stable and without jitter for the LLRF controller to operate properly. This is an inherent problem for testing the system with the VNA but would not be an issue in normal operation. Avoiding the additional functionality, the VNA was used as a signal source for amplitude testing.

Testing amplitude performance comprised of incrementing the GUI amplitude set-point

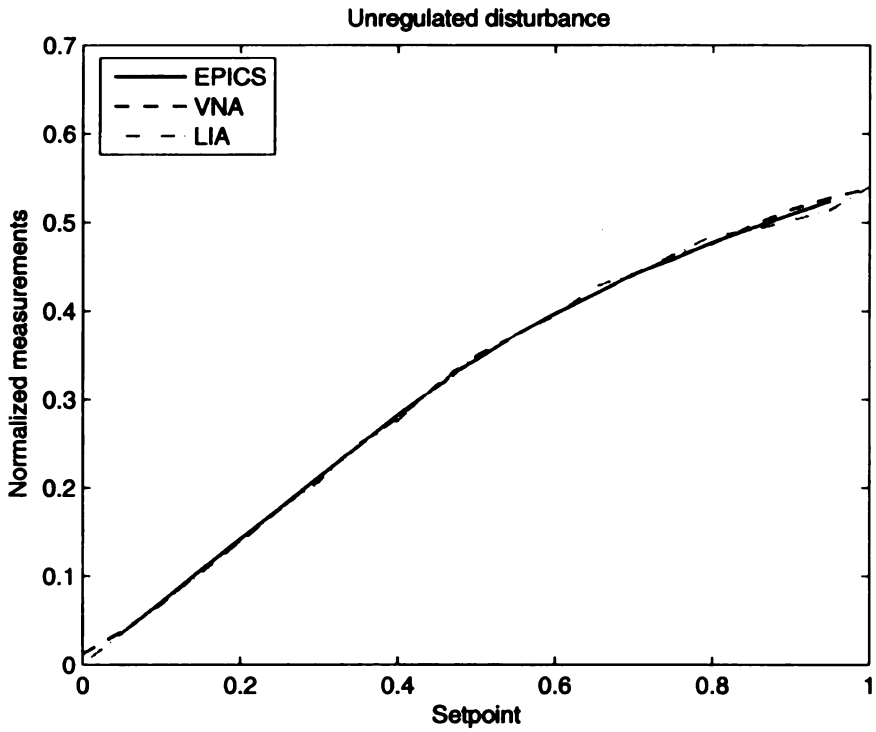

Figure 8.11. Amplitude measurements vs. set-point, uncontrolled with a disturbance.

by specific values and measuring the amplitude of the cavity output. The output measured was normalized for comparison to the set-point values. Figures 8.10, 8.11, and 8.12 are the different measurements where VNA, LIA and EPICS outputs are plotted against the set-points.

In figures 8.10 and 8.11, the controller was unregulated and ran freely. Unregulated, the cavity output amplitude is adjustable but not controlled; therefore, the relation to the set-point is not of concern. Of relevance is that all three measurements are in tight formation. With the exception of very low amplitude readings which enhance percent deviation values, the VNA readings are within 1.97% of the EPICS reading and the LIA values within 2.6% deviation from the EPICS readings (see table 8.5) for each operation. If we consider only the regulated case, the largest percent deviation, from the EPICS values, was 0.8% for the VNA, and 0.74% for the LIA.

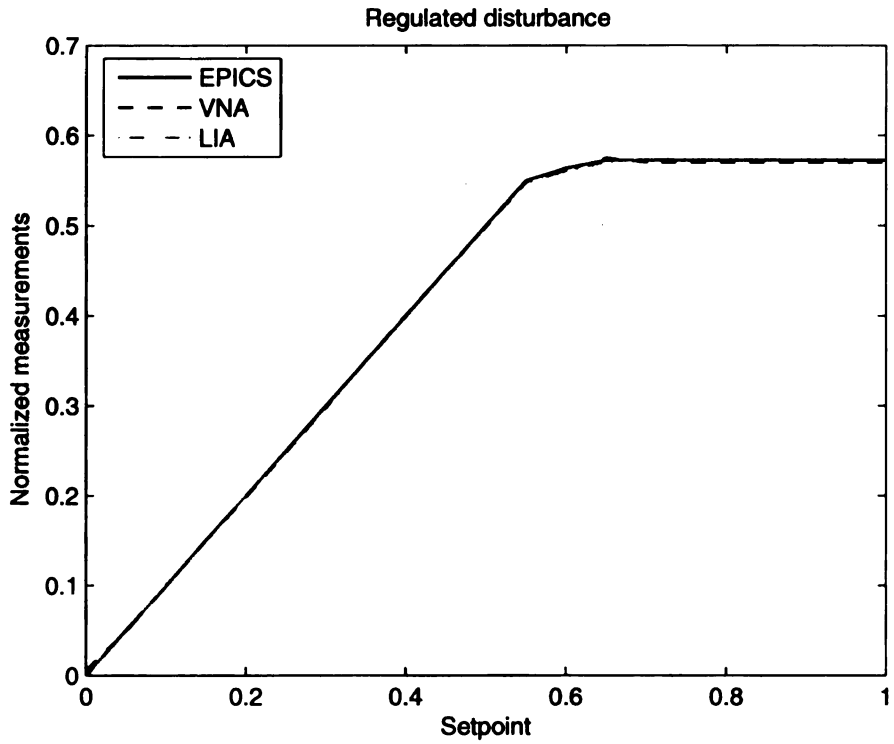

Figure 8.12. Amplitude measurements vs. set-point, controlled with a disturbance.

Consider the calculated percent deviation of the measurements relative to the set points in table 8.4. Prior to the output saturating the amplifiers, we see the percent deviation from the set-point value less than the required 0.5% for all measurements. The values indicate that the EPICS GUI values are within a 0.5% margins of the set-points.

Amplitude values start to drop away from the set points when the amplitude is set above the limits of the controller. When amplitudes are beyond controller limits, amplifiers are saturated and no longer respond linearly. This railed effect occurs during unregulated operation as well, because signals are sent through the same analog system but not controlled by the digital PI loop.

Our main concern is whether the controller GUI output represents true output, so that we can rely on the LLRF GUI for performance during operation. Only during regulated operation will the output be relative to the set-points, where the response should be within

0.5% of the set-point value. In the regulated amplitude comparison plot of figure 8.12, there is a one-to-one ratio of the set-points to the measured values, until the controller limit is reached. The deviation from the set-points for each measurement is listed in table 8.4.

As in the phase measurements, independent verification of output data using alternate pieces of equipment have been performed to ensure LLRF GUI data is within specification ranges. Each measurement has its own level of accuracy that must be accounted for and our measurements are limited to those accuracies. The measurements at these levels can only be relative to the resolution of the test equipment as the measurements are below the specified accuracy of the equipment. Table 8.4 shows the deviation from EPICS for each reading. As long as those readings are within RIA specifications we can claim EPICS is outputting real data to within RIA specifications.

Measurements of the amplitude noise were not taken as each measurement has its own noise floor determined by the resolution and accuracy of the piece of equipment.

Table 8.4. Percent deviation of amplitude from set-point.

	% Deviation		
Set-point	EPICS	VNA	LIA
0			
0.05	0.3	3.61	2.1
0.1	1.20	0.002	0.57
0.15	0.033	0.138	0.711
0.2	0.063	0.890	0.124
0.25	0.060	0.791	0.562
0.3	0	0.649	0.489
0.35	0.057	0.132	0.477
0.4	0.05	0.180	0.475
0.45	0.022	0.110	0.281
0.46	0	0.031	0.406
0.47	0.04	0.033	0.369
0.48	0.033	0.023	0.401
0.49	0.01	0.346	.391
0.50	0.01	0.374	0.340
0.55	0.05	0.464	0.430
0.60	6.08	6.47	6.60
0.65	11.92	11.54	12.28
0.7	18.21	18.59	18.08
0.75	23.67	24.02	23.54
0.8	28.42	28.77	28.31
0.85	32.64	32.96	32.53
0.9	36.38	36.68	36.28
0.95	39.73	40.01	39.63

Table 8.5. Percent deviation of measured values to EPICS.

	% Deviation of measured values vs. EPICS					
	Unregulated No Disturbance		Unregulated Disturbance		Regulated Disturbance	
	VNA	LIA	VNA	LIA	VNA	LIA
0.05	0.242	0.357	5.398	1.183	3.322	1.864
0.1	0.741	0.197	2.760	0.952	1.217	0.632
0.15	1.033	0.084	1.547	3.655	1.171	0.744
0.20	1.070	0.121	1.971	1.439	0.818	0.061
0.25	1.062	0.026	0.570	0.155	0.731	0.502
0.30	0.773	0.0357	0.417	2.583	0.649	0.489
0.35	0.4593	0.233	0.773	0.761	0.189	0.420
0.40	0.196	0.092	1.185	2.282	0.230	0.425
0.45	0.111	0.062	0.547	0.779	0.133	0.259
0.46	0.013	0.159	1.033	0.038	0.031	0.406
0.47	0.038	0.096	1.291	0.117	0.311	0.093
0.48	0.075	0.191	0.356	0.982	0.565	0.369
0.49	1.326	1.383	0.072	1.0144	0.336	0.381
0.50	0.508	0.278	1.233	0.733	0.364	0.330
0.55	1.011	0.326	0.130	0.164	0.410	0.376
0.60	1.461	0.320	0.208	0.642	0.414	0.552
0.65	1.810	0.4444	0.018	2.041	0.431	0.410
0.70			0.191	0.131	0.467	0.165
0.75			0.508	1.077	0.467	0.165
0.80			0.283	1.629	0.467	0.165
0.85			0.625	0.527	0.467	0.165
0.90			1.070	1.310	0.467	0.165
0.95			0.696	1.902	0.467	0.165
1.00			0.609	0.957	0.467	0.165

Table 8.6. Percent deviation of amplitude from set-point.

	Averaged % Deviation from Epics	
Condition	VNA	LIA
Unregulated no disturbance	0.702	0.259
Unregulated disturbance	0.667	1.139
Regulated disturbance	0.409	0.387

8.5 Conclusions

The level of performance of the LLRF controller is beyond the measurement level of available equipment at the lab. Various types of measurements using separate pieces of equipment were used to correlate the data and confirm that the displayed output is with design parameters.

By comparing output data with various other pieces of equipment, we can see the general correlation between EPICS, the VNA, the LIA, and the mixer data. The consistent deviation in VNA measurements correlates the EPICS data, which gives confidence that the EPICS values are real output from the cavity. This relationship indicates that the output is correct relative to the set-point values, and the close-fit between measured values is indicative of the accuracy of the GUI EPICS readings. We may correlate the data based on the resolution of the various methods of testing, yet only the accuracy of each piece of equipment is the limiting factor in determining the accuracy of the EPICS data.

From the resolution of each piece of equipment, the relative accuracy of the data is at worst 0.064° in phase and the relative accuracy of the EPICS data is at worst 0.74% in amplitude. The resolution of the equipment is not the true accuracy of the measurements.

The accuracy of the measurements is limited to the accuracy of each piece of equipment. Accuracy level limitations of the equipment are normalized to 5.7% for the LIA, and 0.35% for the VNA for amplitude measurements. The values are normalized for comparison to the dimensionless values of the set-points from zero to one. Using the VNA measurements for the regulated disturbance in table 8.5, we can claim that the EPICS output is accurate to within 0.649% for the dimensionless amplitude set-points above 0.3. The accuracy of the phase measurements is limited to 2.5°, therefore the best claim we can make is that the phase readings are better than 2.5°, and amplitude readings better than 0.649%.

CHAPTER 9

Conclusion and Future Work

A low-level RF controller designed to compensate cavity fields in the presence of perturbations has been presented to help the user understand its method of operation. This thesis is meant to be a guide for future use of the LLRF controller. Little documentation supplied with the controller required reverse engineering the system to understand its operation.

The controller is a digital PI controller that can adjust on a point-by-point basis the driving signal to a cavity for beam acceleration. Methods used to obtain compensation are analog downconversion of system frequency to 50 MHz, analog to digital conversion, digital processing, recreating the analog signal, and upconversion to system frequency. Digital conversion of the input signals are digitally demodulated into I and Q values. Working with I/Q values facilitates the use of digital registers and loops in a FPGA environment which has high throughput and low latency. Recreating the output signal is also performed in a unique method ensuring little sideband frequencies and an acceptable power level.

Additional functionality of the controller resides in some of its complexity in the form of a direct digital synthesizer which can operate the LLRF as a stand alone frequency generator and scope at the cavity frequency with a bandwidth of 625kHz.

The accuracy of the LLRF is beyond the accuracy of the independent equipment used to verify the LLRF output data. The best possible accuracy for test equipment was 2.5° in phase and 0.35% in amplitude. Our measurements were better than the accuracy of the test unit but we can only claim that the LLRF is accurate to within 2.5°. The amplitude measurement relative to the EPICS data were within 0.649% above the dimensionless set-point value of 0.3. We can claim the confidence level of the LLRF output data is within

0.65%

It was determined using the display resolution of the equipment that the relative accuracy was better than 0.064° in phase and amplitude 0.649%, when the set-point was above the dimensionless value of 0.3. The EPICS output, which is the measurement that will be used during normal operation, was within the these relative accuracies.

9.1 Future Work

Further testing of the LLRF needs to be performed on SRF cavity where narrow cavity bandwidths limit the range of control of the LLRF. A limited amount of testing did occur on the NSCL RIA prototype cavity, but the resonant frequency fluctuated beyond the abilities of the LLRF controller. It is necessary to eliminate or reduce the disturbances to a level that are near or within the bandwidth of the system.

A system has been developed and tested at the NSCL called Adaptive Feed Forward [8]. Using an algorithm with Matlab and a DSpace DSP board, the AFC controller is designed to cancel out disturbances with piezo-electric actuator. Testing has shown tremendous promise for its implementation.

Testing is has been performed with both controllers working in conjunction with each other on the multi-cell copper cavity. The bandwidth of the copper cavity is wide enough so that the LLRF can easily control all disturbances. The AFC controller was also capable of controlling the disturbance. The important result of the test with both controllers operating simultaneously was that they did not conflict with one another. This is a promising combination of control and requires further testing on an SRF cavity.

Additional future work would be to add a Matlab application to the EPICS programming. This would allow user operation of the DDS function of the LLRF so as to sweep the unregulated cavity and determine its resonant frequency. The additional functionality would simplify and reduce some of equipment necessary for testing.

APPENDICES

APPENDIX A

User Manual

The LLRF controller is a device to compensate cavity driving signals in the presence of low level disturbances in a cavity. The accompanying thesis provides information in the operation of the controller. This is intended for a user who is familiar with setup procedures and microwave circuitry components.

This controller was originally designed for a different project that operates under different parameters and has different requirements. SNS is a pulsed system and relies more on the decay of the wave form to determine frequency displacement. The cavity output waveform is monitored during the ramp-up, peak of the pulse, and during the decay of each pulse. There are a number of parameter adjustments that apply to SNS, that have no bearing to the RIA continuous wave (CW) environment.

Controlling the LLRF is performed over the EPICS GUI, which is the interface between the controller and the user. EPICS provides realtime adjustment and monitoring of system levels. The GUI are edl extensions that can be navigated and manipulated.

A description of all the parameters is followed by a method of calibrating the controller for each individual case. Once calibrated the system can be set up for stability. Then the user has the ability to adjust phase and amplitude while monitoring the system. The GUI displays the power of cavity output, forward and reflected signals, which are scaled depending on the signal strengths from the system. Finally, step by step instructions are

outlined for calibrating and operating the system in section A.4, followed by a description of some additional functionality and a means to modifying the GUI windows for individual preferences.

A.1 Hardware and Software

Component that came with this particular chassis.

- Power cable,
- Serial cable for direct connection to LLRF by a unix based computer.
- Software for installation on a unix based, or sun station computer.

Software must be loaded onto an available computer to house the Linux source code for the LLRF host processor. These are loaded up each time the LLRF is booted. At NSCL we currently have a system established as an EPICS server which is ussed to hold the LLRF source code.

- Sun Sparkstations running Solaris 8.
- Our main system is epicssun.nscl.msu.edu, IP:35.9.57.201.

A Linux computer is needed for holding the EPICS windows edl files, for the LLRF. The source files for the LLRF, and the edl files may be housed on the same machine. A cd with all the necessary files for downloading is available and is included as part of the package. At NSCL the source code was loaded on the Sun station, and the LLRF EPICS files were loaded into the Linux PC.

When the LLRF boots up, it targets the Sun and loads all the remaining files. The LLRF becomes an EPICS server looking for Channels anywhere in the lab. The Linux PC that houses the edl EPICS screens responds to exchange data. The EPICS system is a protocol

network allowing various computer to access Channels over the network. There is no direct link from the Linux PC to the LLRF.

We are able to view the edl EPICS windows by connecting to the Linux PC remotely. In order to see the edl screens on a remote PC, one must have the IP address of the Linux PC and xwin-32 installed. An xwin-32 session needs to be open to view the EPICS windows on a PC. The Xwin-32 configuration parameters are.

- Session Name: LLRF
- Host Name: elec8.nscl.msu.edu
- Login: epics.
- Command: setenv DISPLAY $MYIP:$DNUM;/home/epics/runllrf
- Password is available upon request

A shortcut can be established for easy opening of files. At NSCL, a script has been written to install the xwin-32 session as a shortcut. In the Lab the link, \\baltic\develop\setup\misc\LLRFXWin32Setup.exe, will create a shortcut icon on the desktop to access the EPICS windows immediately. Once the system is loaded and EPICS files are saved to a computer, the xwin-32 session can load the EPICS window applications.

A history of the boot up is held in memory and can be obtained remotely by the address http://35.9.57.225/var/log/bootleg.txt

A.2 Connection and set-up

Once the software is loaded and running, the LLRF is ready for operation. In this section we discuss all the connections and what purpose they serve.

A.2.1 Connection on rear

The rear of the chassis has multiple ports, which include,

- Ethernet port
- RJ-45 connector for serial port connection
- Limo connection
- Weidmuller (p/n: 172863) interlock connector

The ethernet connection allows communication from the LLRF host processor with the outside world. The LLRF loads source files upon boot-up, and serves EPICS channels remotely. The FPGA can be reprogrammed directly over the ethernet connection via a jtag connection on the host processor. A 100Mb/s is required for connection speed.

A serial cable can be connected directly to the LLRF instead of using the ethernet connection. If the host computer is a windows PC, a 'terra term' session with com1 or com2 depending on the port connected to will be able to communicate with the LLRF. In order to see the edl window, it is necessary to use the Linux PC for the serial connection. On the Linux PC, open a 'minicom' session to communicate with the LLRF. To view the edl screens from the Linux PC, the command './runLLRF', will open up the GUI screens.

The trigger is meant to pulse a beam for a specified duty factor. During the positive cycle of a duty factor, the LLRF outputs RF drive signal to the cavity. For RIA and our test purposes, we are using a CW drive signal, so the Limo connector is presently fed a constant five Volts from the power supply inside the LLRF, with some external connectors.

There is also a safety interlock connection. The interlock signal is passed through an opto-coupler regulator, and two logic gates prior to supplying a TTL switch with a high signal, to turn on the output signal to the cavity. If for some reason the system needs to shut down, the lack of signal for this interlock will absolutely prevent any output to the cavity. The LLRF output is dependent on the interlock switch. This would typically be

used in conjunction with all other safety interlocks. This needs a positive five volts to operate the LLRF. The GUI has a display across the upper right side of the 'main' window that indicates either 'ready' or 'fault', of the interlock status. For testing purposes we have 9 volt battery connected to the Weidmuller connector supplying the 5 volts. A LED output from the connector externally indicates the status of the system as well.

A.2.2 Front panel

The front panel of the LLRF has a series of LEDs, indicating the status of the controller. The condition of the LEDs is dependent on the booting process of the LLRF. As the host processor boots and connects to the Sun to load files, a series of four LEDs lights up . The final LED flashes with a period of five seconds given everything loaded correctly. If there was an error in the boot-up process the last LED flashes with a period of 0.7 seconds.

Three SMA testpoints are available at 50 MHz and may be used for verification of forward, reflected, and cavity signals.

A pKz (part number 26-1080-1201) connection housing is used for the cables from the cavity or the support chassis. These include the LLRF, IF, LO, Forward, Reflected, Cavity output and the cavity drive signals. The connectors are available from "The Phoenix Company" in Chicago. Cables are low attenuations and should be approximately the same length to the support chassis. The cables used in the present setup are rg-223. These where used to connect the pKz connections.

General set up for system may be set up as per figure 6.3 in chapter 6.

A.3 Explain all parameters on GUI

If the software has been successfully installed, clicking on the LLRF shortcut will load up the 'main' LLRF EPICS GUI. The main window is the operational window that allows for adjustment of phase and amplitude as well as a monitor for output levels, and status

indicators.

The upper right corner has buttons labeled 'Extra', which opens a second window with calibration settings, and 'More'. The more button opens a menu of other possible windows.

- Main
- Extra
- 3-D
- Config Reg
- Calibrate
- Phase plots

The Main and Extra windows are the most used during operation. The following section outlines all the functions on each window.

A.3.1 Main

The main screen is where calibration of the controller is performed as well as operational settings. In the upper right corner are buttons to other optional screens. On the lower right corner there is a button labeled 'pulse' or 'cw', indicating the mode in use. In cw operation this button is used temporarily in 'pulse' mode during calibration and then switched to 'cw' during normal operation.

The pulse is used for calibration to see the decay of a signal and determine its the location of stability which depends on the gain settings. At the very bottom right corner are 'MPS and HPS Status' which are specific to SNS and not used in cw operation. There are other blocks of displays that are described in further detail.

Error Block

Just right of the waveform plots are a list of potential errors. The display is an accumulation of errors as they occur with the exception of the cycle count which is the accumulated number of all compensated values.

1. **Error Bits** A complete count of the all the errors as they arise.

2. **Cycle Count** This is general count of each set of data compensated through the controller.

3. **PLL** The phase lock loop error reading. This accumulates if the system loses phase lock with the reference signal. This can be confirmed with the display number 1 on the lower left of the 'extra' screen. That group is the measured value of the ADC signal level for the reference signal. Number 1 is the level of the PLL input, if this is out of range than the PLL error will accumulate. If teh reference signal is too high and saturates the ADC, the D-overflow will accumulate.

4. **Hand Error** Accumulates if there are data transfer problems between the host and the FPGA. This can be fixed by reducing the acquisition rate, which done by increasing both 'IR_time' and 'idle_time', on the 'extra' screen. Maximized these two slide switches establishes an acquisition rate of 24Hz, which is a reasonable rate for testing.

5. **Sync Errors** Accumulates if there are synchronization problems between the host processor and the FPGA.

6. **No sync** A constant accumulation would indicate a break in the link between processors.

7. **Skip Trigger** If in pulsed mode the trigger does not occur, an error count will accumulate.

8. **No 40MHz** Accumulate if the 40 MHz clock is not working.

9. Overflows If any of the ADC values are saturated the count begins. ADCs read signal levels where, A is forward power, B is reflected power, C is the cavity output, and D is the reference signal IF.

Graph Block

The most prominent feature of this screen is the waveforms. The displayed waveform legend is to the right of the graph. Waveforms are of I and Q values as they are read by the ADCs.

Just below the waveforms is a section of slide switches labeled 'Graph'. There are two input values for controlling the waveform plot. The upper slide-switch controls the amount of the waveform one would wish to see. The x-axis is in units of mircro-seconds, by increasing the amount of the visible waveform one would be able to see the decay time of the pulse. In cw operation the waveform are straight lines.

The lower slide switch is a delay in the waveform plot. In pulsed mode a delay would be necessary to see the ramp up of the signal when triggered. The two graph controls in conjunction allow the user to focus on a section of the pulse waveform.

Control Block

Directly below the 'graph' control is the control block where initial calibration of the gains are set and the final amplitude and phase settings are input. Amplitude setting are dimensionless values between zero and one. Because the output is amplified, the values can be scaled according to the amplification, on the 'calibrate' screen. Phase is set to degrees and is relative to the desired phase. There is a method to recalibrate phase to zero on the 'extra' screen to reset the zero phase set-point to zero, compensating for cables and components phase offset.

The last three settings are part of the calibration of the controller, where Gain is the K_p, and 'Int Scale' is the K_i compensation gains. The 'Gain Rot' setting is the phase rotation to

compensate for the phase offset in cables and microwave components. When adjusting this value there are two points that appear to be stable across the 360° range. One is negative feedback and the other is positive feedback. The negative feedback position will be the controller setting, as the positive feedback will destabilize the system.

Monitor Block

The display on the lower left corner of the main screen shot are output levels displayed in power, voltage and degrees. The output values are dependent on the scaling factor provided in the calibration window. Functions that are not operation at the NSCL version are 'Delta Freq', 'bandwidth', 'plate voltage' and 'Tuner Readback'.

A.3.2 Extra

The extra screen contains parameters that are set during the calibration of the controller but are not necessary to adjust during normal operation. The screen contains graphs, monitored values and slides switch settings. The Upper plot is based on the feed-forward design of SNS and corresponds to the Feed-forward block. The cw system is not designed to use feedforward information. The lower plot is strictly the cavity output signal.

The phase reference block has the phase zero calibrate button to reset the phase reading to zero and allow for easier tuning of phase. There are amplitude and phase adjustment slide switches available here as, which control the same set points in the 'main' window.

Below the 'Phase reference' is a set of timing scales adjusting acquisition data for waveforms. The plotting of waveforms is more informative in the pulsed system and requires some display tuning to see the decay of the wave. In SNS the decay of the waveform is used to determine the frequency offset to control the mechanical tuners for slow tuning. In the cw system the decay does not occur and most of these parameter are not used.

1. **IR Time** Inhibit retrigger. Combined with the Idle time, control the acquisition rate for waveform plots, or refresh rate. Handshake errors may result from the host computer

processing some data. Increasing both IR and Idle times lowered the acquisition rates

2. **Idle Time** Allows for some down time prior to uploading next value for plotting.

3. **Warm Time** Sets a delay prior to pulse before plotting. During calibration this should be set to 600.

4. **FF Time** Adjusts the display when feed-forward data is applied.

5. **FB Time** Adjust the display when feedback is applied.

6. **Decay Time** Adjusts the display time of the waveform decay. Only functions if mode settings are to display decay.

In the lower right corner are the displays for the mechanical motor controller which controls frequency drifts and slow tuning of the system. This is particular to SNS and not presently used at NSCL. Although the screens have not been modified for NSCL, it is clear that if further modification of the controller occurs, the LLRF EPICS interface can be used to set and monitor additional features.

ADC Level Monitor Block

In the lower left hand side of the window are a list of 16 displayed monitor levels. The majority of the display windows are unused. In the first column of the display, one through eight have values displayed. The second column has no values displayed and are SNS ADC values and are not relevant to NSCL.

1 Phase Lock Loop, this is the level of the LLRF IF signal into the PLL ADC. The displayed value is scaled from 0 - 3.3 Volts. A reading over 1.5 is good. The PLL has an ability to lock onto a weak signal. Testing revealed that an input IF level of -33dBm was the low threshold and 5dBm was the upper limit of the PLL input, see table A.1. The high limit saturates the ADC and the phase lock is lost, which can be seen with an accumulation of D overflow in the error display.

Table A.1. ADC signal level response to IF input levels.

IF input level	ADC level (mV)	Comment
-33dBm	4	Too low
-32dBm	1790	Good
↓		Good
5dBm	1800	Too high

2 LO power levels. Mixers within the LLRF use the LO signal for input, if the LO signal is low then the mixer response will also be reduced. To drive the cavity the LLRF compensated signal is upconverted to the 805 MHz. A reduced LO results in lower signal to the cavity, and weaker signal from the cavity output and therefore lower resolution of LLRF signals.

Levels should be around 2V, a much improved cavity output signal was observed when the LO input level was above 1V. See table A.2 for the ADC level response to various LO levels.

Table A.2. ADC signal level response to LO input levels.

LO input level	ADC level (mV)
-10dBm	800
-6dBm	1040
-4dBm	1200
-2dBm	1410
0dBm	1610
1dBm	1800
2dBm	1920
3dBm	2000
4dBm	2075
5dBm	2130

3 Unused.

4 Unused.

5 Unused.

6 Unused.

7 15 Volt Power supply. Scaled from 0 - 4.95V. Scaled by 0.24. To determine real output from power supply divide by scale factor. Example; our reading of 3.719V is $\frac{3.719}{0.24} = 15.496$V.

8 Cavity output level. Also scaled to five volts. Higher values indicate stronger cavity output, which may be reduced by the digital attenuator.

Status and Mode Block

Just right of the signal level measurement, in middle bottom of the window are five reading of importance. The top is the temperature reading of the digital board. In pulsed mode it typically runs approximately at 50°, while in cw it runs closer to 80°. This should be monitored once the chassis is mounted into a rack. Additional ventilation may be required.

The 'status' is a hexadecimal reading of the status of the controller.

The 'mode set' is an input which is a primary critical setting of the controller. The mode establishes the operating settings of the controller. A 16 bit register for the mode determines multiple functions as listed in table A.3.

A default mode is set and needs to changed for use in cw. Modes we have been operating are listed in table A.4

In order to achieve output in CW the 'ignore_RF_off' and 'self-re-trigger' bits had to set. In addition five volts had to be supplied to the trigger on the back panel.

There may be different configurations of the mode_set that would be appropriate for cw use. Not all configurations have been tested.

The 'Out Atten' is also an input for the digital attenuator. This enables the cavity output signal level to be controlled digitally. It is set during the initial calibration of the controller.

Table A.3. Mode register setting.

Default	RIA	Description
0	0	Raw DDS select
0	0	Totalizer channel
0	0	DDS pass-thru (cw)
0	0	CW_request
0	0	RF kill
1	1	Integrate select
1	1	Feedback select
0	0	Trace select[1]
1	1	Trace select[0]
0	0	Halt
1	0	Self re-trigger
1	0	Ignore RF off
0	0	continuous Feedforward
1	0	unused
1	0	unused
1	1	Trace Select
6B7	687	Hexadecimal
1719	1671	Decimal

Table A.4. Mode settings.

Mode	Hexadecimal	Decimal
CW-unregulated	36B7	14007
Normal regulated DDS	16B7	5815
Normal regulated	6B7	1719
Pulsed unregulated	86B7	34487

The very bottom input is the 'DDS Freq' where an range of 625 kHz may be used to alter the resonant frequency of the cavity. A value of 0 - 32767 may be entered where the entered value is multiplied by 19.07 Hz. A value of 1 shifts the frequency by 19.07 Hz.

3-D

This is a plot of the values viewed parallel with the x-axis of the main waveform plots. In cw mode this gives you an idea of how the I/Q values literally rotate around in phase.

A.3.3 Config Reg

This window is not for inputting but viewing the state of the mode register. It may help in determining what mode may be most appropriate.

Calibrate

This window is where you set level of cavity signals to scale the displayed values correctly.

The 'Control' block is the same amplitude and phase control as the main window. Adjusting the values here changes the amplitude and phase values in every window. The 'monitor' block is also identical as the main window.

Right of the Monitor block are settings for Forward and Reflected power, you enter the amount of kW that full-scale represents. The mean squared value of the waveforms is scaled according to that value. Cavity signal is the number of Volts (kV) that full-scale represents. The mean value of the waveform is scaled according to that value.

In each case, only a subset of the waveform is averaged, so for a pulsed system one would only want the average during the flat top of the pulse. Setting the AvgStart and AvgDuration settings adjusts the amount of the waveform that would be averaged. In CW, we should set the window to start at 0 and have length 256 to see the entire waveform.

A.3.4 Phase plots

These are plots of the amplitude and phase in magnitude and degrees, not I/Q values. The points are from the Field Amplitude, and Field Phase output channels also displayed on the main window.

A.4 Start and calibration

Set up equipment as described in figure 6.3. Turn on signals to support chassis and power up the support chassis, and finally power up the LLRF.

Start the GUI by opening the shortcut created with Xwin-32.

The first screen to appear should be the 'main' window. Ensure the upper right hand corner has 'ready' written in red. This means the interlocks are set. If a 'fault' appears, the interlock is not powered, and in the test set-up the battery may need replacing. Set amplitude and 'int scale' to slightly above zero. Adjust gain to zero.

Go to the 'extra' screen. Set Warm time to 600.

We need to determine the level of digital attenuation to set. We will adjust the attenuation to achieve highest power output while not compromising linearity. In the Feedforward block set the mode to 3 which is a triangular input. Maximize the amplitude and adjust the phase to see a straight line along the x-axis and a stepped curve, in the lower plot. Manually change the level of digital attenuation, increasing the amplitude of the curve while maintaining step formation in the curve. If the curve becomes round, step down the attenuation. There is a point where little gain is added with additional attenuation, while still maintaining step formation in the curve.

Too much power in the output channel will be visible by trapezoidal shape in the curve and phase rotation between I and Q not of 90°.

We can approximate the level of amplification on the main setting at this point. Looking at the Forward power on the main window, adjust the phase so that I or Q is horizontal. The amplitude of the other forward variable can be divided by full scale of 32000, to approximate the limit of amplitude.

For example the forward power measurement is 20000.

$$\frac{20000}{32000} \approx 0.625 \tag{A.1}$$

An amplitude setting of 0.625, will be the limit before saturating the components.

In Feedforward block reset mode to 0, and turn the amplitude down to 75% - 80% of the amplitude just calculated. In this case 0.47.

Set the gain to 0.5 and int scale approximately half way, and start to adjust the 'gain rot'. As you scroll across the system should appear unstable. At a point right on the edge of unstability should be a point where I and Q lines for all three signal are critically damped. It is possible for forward and reflected signals to have some transient, as the cavity charges. The cavity signal should be critically damped. There are two point that meet this description, one is positive feed back and the other negative feedback, which would be apparent by adjusting the amplitude setting and observing the response of the system. In positive feedback at a stable point, an increase in amplitude will lose stability. In negative feed back, the system response would an linear increase in power during an increase in amplitude.

A means of approximating the 'int scale' is also possible. Scaling the decay time which is indicative of the frequency offset, or noise bandwidth, of the waveform against the system bandwidth The decay time of the output signal can be approximated by the time from time of critical damping in the main waveform plot. The time scale is in microseconds. For example; a measured time of 60 microseconds of the waveform is read on the copper cavity which has a known bandwidth of 67 kHz. The signal bandwidth is

$$f = \frac{1}{60 \times 10^{-6}} = 16.6kHz \tag{A.2}$$

Now scale the ratio of signal bandwidth to the system bandwidth.

$$\frac{16.6}{67} \times 32767bits = 8150 \tag{A.3}$$

Set the int scale level to approximately 8150.

Once this gain rot is found, manipulate the gain and int scale settings to achieve the best stability for highest gain. the system should be ready to regulate now.

Press the pulse/cw button to the right and the waveforms will change to straight lines. Adjusting the amplitude should have a linear response in terms of power output until the

components are saturated. This may not be clear in cw mode but in pulsed mode the system is clearly unstable after the amplitude limit is reached.

Phase change will be visible through the rotation of the I and Q around the x-axis. See the 3-D plots.

A.5 Additional Controls

The DDS function is a direct digital synthesizer, or frequency generator. It may be set to offset known parameter offsets, such as in the case of normal conducting cavities. a normal conducting cavity is not super cooled, but water cooled. As power is delivered to the cavity it begins to warm up due to resistive losses in the metal. As the temperature rises, the shape of the cavity increases with thermal expansion. The DDS is used to follow the resonant frequency of the cavity, to within the system bandwidth and maintain control of the cavity fields.

A.6 Viewgraphs

The plots on the main page are the I and Q values for the forward, reflected and cavity signal. The data running on the FPGA is I/Q form and is presented in the same manner because of the rate at which the FPGA can process register values. Converting to phase and amplitude is performed on the host processer in C code. It operates at a slower speed relative to the high throughput of the FPGA. On a personal level, it is difficult to understand the effect of the control looking at specifically the I and Q data. A separate window called 'Phase plots' was created to present the amplitude and phase of the output based on the C code processed data shown on the main window display. These plots are more intuitive in describing the system performance.

A.7 Manipulating EDL

Edl screens are based on a Linux environment and requires the use of three button mouse. Clicking the middle button anywhere on the edl window will open up a drop down menu with several options. Click 'edit' to be able to manipulate the GUI. In edit mode it possible to double left click on any display box, and obtain information concerning the data source and the display parameters. Changing sources or adding data is very intuitive once the parameters values are known.

It is possible to create a new window and build relative information for a particular need. Create changes to a window and 'Save as' a new name with the edl extension to save the window on the Linux PC.

Once completed, again click the center button to open the drop down menu, if a particular display has been selected for editing, it must be 'deselected', then click on execute to activate the window and regain control of the window. The amplitude and phase plots are created with the same data that is provided on the 'main' screen, only plotted against time. Time in this case is the number of bits holding data, which is 256 or less. The Epics Channel variable name 'p$aveCavAmpTime' was the channel access variable needed to plot the amplitude.

APPENDIX B

LLRF Schematic

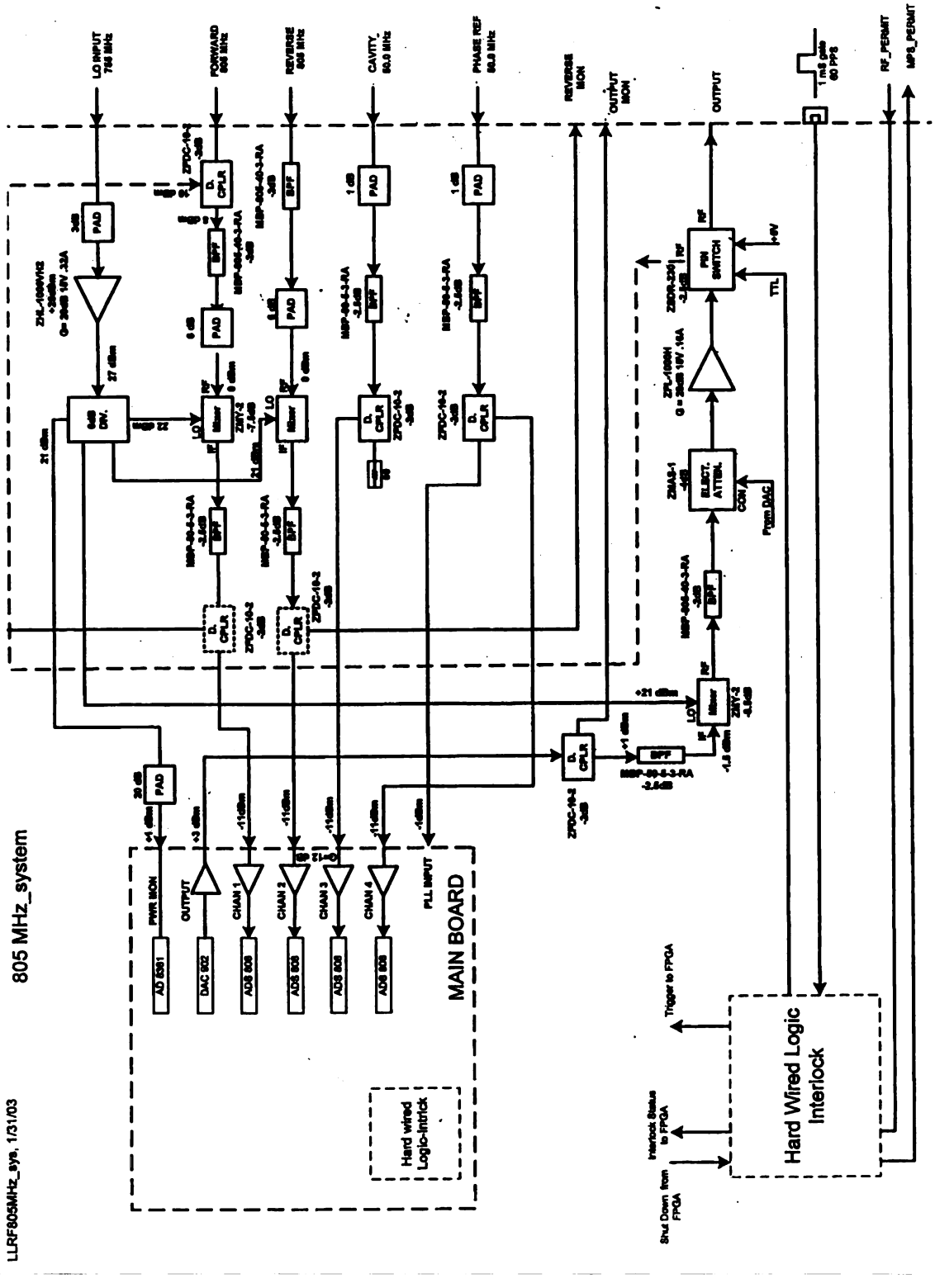

Figure B.1. LLRF schematic.

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