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MULTILEVEL INVERTERS AND THEIR APPLICATIONS IN POWER SYSTEM

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MULTILEVEL INVERTERS AND THEIR APPLICATIONS IN POWER SYSTEM

BY

Jin Wang

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ABSTRACT

Multilevel Inverters and their Applications in Power Systems

by

Jin Wang

A power system composes three interconnected subsystems: generation, transmission, and distribution. With the ongoing expansion and deregulation, there are also three major trends to reform the power systems: 1) to utilize distributed generation (DG) to meet the increasing power demands; 2) to utilize Flexible AC Transmission devices (FACTs) to improve the transmission and distribution systems; and 3) to utilize Custom Power devices to improve the power quality to the end users at the distribution level.

Power electronics inverters are enabling parts of DG and core parts of FACTs and Custom Power devices. In the power electronics inverter family, multilevel inverters are the newest breed. Compared with other inverters, multilevel inverters have two distinguished features that make them more suitable for the aforementioned power system applications: 1) the multilevel structures enable the utilization of low voltage rating power semiconductor devices in high voltage applications; 2) and the almost near sinusoidal output voltage waveforms from the multilevel inverters make it

possible to eliminate the output filters and zigzag transformers, which are often connected after traditional inverters. Three major issues involved with multilevel inverters in power systems are DC bank voltage maintenance, balance of DC banks, and harmonics optimization of the inverters' output voltage.

This dissertation first summarizes the previous works on FACTs, Custom Power, DG and multilevel inverters, and discusses the major application issues for cascade multilevel inverters. A new harmonics elimination method for multilevel inverters is proposed. Then, in the main part of the dissertation, two applications of cascade multilevel inverters in FACTs devices — a new Unified Power Flow Controller (UPFC) and a Universal Static Synchronous Compensator (U-STATCOM) — are proposed. Unlike conventional UPFC, in the proposed UPFC, cascade multilevel inverters can be used without compromising power flow controllability. The proposed U-STATCOM can be used to compensate not only reactive power and harmonics but also load current imbalance. The circuit structures, control methods, comparisons with conventional solutions, and simulation results are shown for both cases. Furthermore, new applications of multilevel inverters in Custom Power and DG are presented as the extended applications of cascade multilevel inverters in power systems.

In the end, the realization of the control unit for a seventeen level cascade multilevel inverter is described. Experimental results based on the inverter are shown to prove the validity of proposed harmonics elimination method.

To my mother, father, and wife

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Foremost, I would like to acknowledge all the invaluable help from my advisor, Dr. Fang. Z. Peng, without whom this work would not have been possible. This dissertation comes from numerous discussions with him, from his keen insight and guidance in a fruitful research area. I would like to thank all my committee members, Dr. Schlueter, Dr. Strangas, and Dr. MacCluer. Their insightful comments and suggestions have enhanced the technical soundness of this dissertation. I am grateful to my friends and colleagues from the Power Electronics and Motor Drive Laboratory. Not only the knowledge, but also the research experience and friendship I gained here will be beneficial for the rest of my life. I would like to express my great appreciation to Mr. Zhiguo Pan, Mr. Alan Joseph, and Mr. Eduardo I. Ortiz for the assistance in the tests of cascade multilevel inverter, and Mr. Joel Anderson for helping revising my dissertation.

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CHAPTER 1
INTRODUCTION

1. 1. Background

With the ongoing expansion and growth of the electric utility industry, including deregulation in many countries, the generation and transmission systems are being pushed closer to their stability and thermal limits. Meanwhile the focus on quality of power distribution has become greater than ever. Environmental impacts also play a larger role than ever in investment decision makings, in all levels of power systems. Thus, at the beginning of the 21st century, with major blackouts threatening the whole world, power systems are now at a dawn of reformation. Optimization of the already established transmission system, implementation of new technologies to ensure power quality, and utilization of renewable energy, now become three major reformation directions. And in this global battle of power system reformation, power semiconductor

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based Power Electronics, a new technology with a history less than three decades long, answers the call.

The very beginning of Power Electronics can be traced back to 1912, when E.F.W Alexanderson of General Electric patented his magnetic amplifier, which worked like an ac-ac converter [12]. Modern power semiconductor based Power Electronics started with the applications of thyristors in 1960s. Since then, several generations of power semiconductor devices have been developed. Now the Isolated Gate Bipolar Transistor (IGBT) has become the major device used in high power conversions. IGBT rated at 4500 Volts, 900 Amperes are already available in the market. With the development of solid devices, Power electronics circuits also evolve. Summarized in big categories, till now, there have been DC-DC converters, DC-AC inverters, and AC-AC converters. The power range of the converters and inverters varies from several watts to hundreds of mega watts. Nowadays, converter and inverter based power electronics equipments have been widely used in all levels of power systems:

1) for the *transmission systems*, Flexible AC Transmission Systems (FACTs) are adopted to control the system voltage, compensate reactive power, and improve system stability and transmission capacity;

2) for the *distribution system*, numerous Custom Power devices are used to improve the power factor, compensate voltage sags, and eliminate harmonics;

3) for the *distributed power generation*, the power electronics equipments are utilized as interfaces between the renewable energy sources and the grid

1. 2. Flexible AC Transmission Systems

In transmission systems, to avoid over stable and thermal limitations, the traditional solution has been to construct more transmission lines and substations. However, experience throughout the last several decades proves that it has been more and more expensive, time consuming and controversial to construct new transmission lines. It has been widely recognized that more efficient utilization and better control of the existing power system is the only way to achieve both operational stability and financial profitability. To achieve these goals, Flexible AC Transmission Systems (FACTs) is the only right choice [44-49].

FACTs devices provide improved transmission system operation with minimal infrastructure investment, environmental impact, and implementation time. To better illustrate how FACTs devices improve operation of the transmission line, some basics of the power system will first be introduced. Figure 1.1 is the well-known power system diagram. When considering the power flow and voltage stability, a two bus power system can be simply described as the sending end voltage, $\vec{V}_{SO}$, and the receiving end voltage, $\vec{V}_R$, connected together by the transmission line impedance, X.

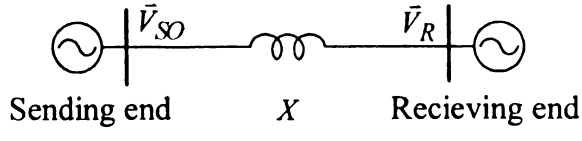

Figure 1.1: The two-bus power system diagram.

Equations

$$P = \frac{V_{SO} V_R \sin\theta}{X}, \tag{1.1}$$

and

$$Q = -\frac{(V_R \cos\theta - V_{SO}) V_{SO}}{X} \tag{1.2}$$

describe real and reactive power transferred from the sending end to the receiving end, where θ is the angle difference between $\vec{V}_{SO}$ and $\vec{V}_R$. From these equations, it can be seen that in transmission system, there are three basic variables that can be used to control the active and reactive power flow:

- Voltage (both Sending and Receiving ends);
- Angle; and
- Impedance.

FACTs devices indeed are devices that enhance the transmission capacity by dynamically changing these three variables. Depending on functions, FACTs devices are usually installed at the ends or the middle point of the transmission line. Compared with the corridor needed by a new transmission line, installations of FACTs devices require almost no additional space [44-49].

1. 3. Custom Power

The term 'Custom Power' is usually used to describe advanced equipments that installed in distribution systems to improve power quality for end-user customers.

Power quality is related to reliability issues in power system. A power quality problem is an occurrence manifested in a nonstandard voltage, current, or frequency

deviation that results in the failure or mis-operation of end-user equipments. In the distribution system, power quality now has become a major concern for the end users. Although, in the last two decades, numerous efforts have been put in place to increase the power quality of existing systems, it seems that power quality still has not reached the desired levels to be consistent with the high degree of automatization and sophistication of modern electronic equipments. The major power quality problems are [93-97]:

- voltage sag
- voltage swell
- voltage flicker
- momentary interrupt
- impulsive transient voltage
- oscillation transient voltage
- voltage harmonics
- three-phase voltage unbalance.

Recently, more and more special attention has been focused on critical loads, such as medical centers, automobile manufacturing plants, the semiconductor industry, broadcasting facilities, and commercial buildings.

1. 4. Distributed Generation

Traditionally, the focus of power generation has been on large central stations. Power

is generated from central power plants and transmitted to end users, which generally are hundreds of miles away. With the world wide rapid increase of demands on power generation, 80,000 MW per year, and deregulation in most regions, small and local generation-Distributed Generation (DG), will play a more and more important role in power system. Research by Electric Power Research Institute (EPRI) indicates that, by year 2010, 25% of the new generation will be DG [129].

DG technology includes [126-129]:

- **Combustion Turbines**: 1-30 MW
- **Reciprocating Engines**: 10 kW-10 MW
- **Micoturbines**: 1-300 kW
- **Fuel Cells**: 1 kW-20 MW
- **Biomass**: 5 MW maximum
- **Wind turbines**: 1 kW- 1 MW
- **Photovoltaic**: 1 kW- 1 MW

Due to environmental concerns, more effort has now been put into the clean DG methods, such as, geothermal, solar thermal, photovoltaic, and wind generation, as well as fuel cells that use hydrogen, propane, natural gas, or other fuels to generate electricity without increasing pollution.

For solar, wind and fuel cell based DG, Power electronics is one of the enabling technologies. Power electronics equipments are used as interfaces between the power sources and the grid to distribute the generated power and provide ancillary services.

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One of the main obstacles in the commercialization of aforementioned types of DG is the high installation cost. The converters or inverters used in the DG are usually the most expensive parts in the systems. So to reduce the cost of the power electronics interface and at the same time achieving maximum power efficiency and quality, now has become very important and urgent.

1. 5. Multilevel Inverters

Multilevel Inverters were first introduced in 1981 by Nabae [13]. Now there are three major types of the multilevel inverters: diode-clamped, flying-capacitor clamped and cascade multilevel inverter. The general concept of multilevel inverters involves producing an AC waveform from small voltage steps by utilizing a bank of series capacitors or separated DC sources. To visualize the idea, a general nine level waveform is shown in Figure 1.2.

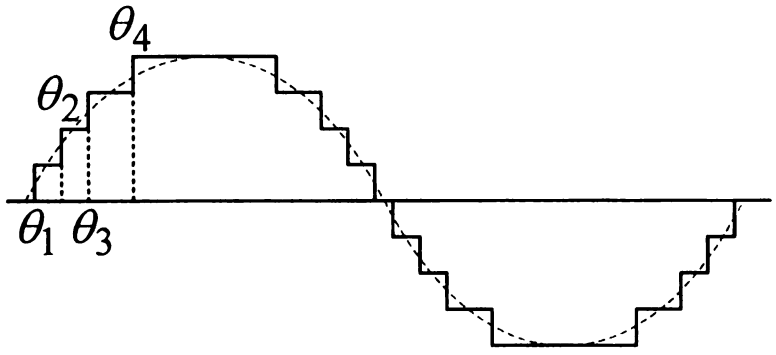

Figure 1.2: The nine level waveform.

The small voltage steps shown in Figure 1.2, yield several of the advantages of the multilevel inverters [1, 2]:

1) very low dv/dt and distortion in the voltage output waveform;

2) low distortion in the input current;

3) enable the utilization of low voltage devices in medium voltage applications;

4) low switching frequency; and

5) low common mode voltages.

These advantages lead to a promising future of multilevel inverters in medium voltage drives and power system applications.

Being a new breed of inverters, multilevel inverters attract researches on themselves as well as their industrial applications. The ongoing research topics of multilevel inverter include [1-12]:

1) maintenance and balance of DC bank voltages;

2) output voltage harmonics elimination;

3) PWM control method, especially at low modulation index;

4) circuit structures and soft switching; and

5) applications in power systems.

1.

1. 6. Outline of the Dissertation

This dissertation mainly proposes two feasible applications of cascade multilevel inverters in transmission systems. The real application issues of multilevel inverters are discussed. One practical harmonics elimination method is proposed. Extended applications of multilevel inverters in power systems are also presented.

Chapter 2 reviews the most current developments in FACTs, Custom Power, DG, and multilevel inverter technologies. The feasible applications of multilevel inverters in power system are summarized.

Chapter 3 discusses the real application issues of multilevel inverters in FACTs devices. Current solutions are summarized and a new harmonics elimination method is proposed.

Chapter 4 proposes a novel Unified Power Flow Controller (UPFC) circuit configuration. The proposed configuration has several unique features and advantages over the conventional configuration. As a result, cascade multilevel inverter can be used in the new configuration to lower the cost, volume, and increase the reliability. Detailed comparison between the new and conventional configuration is made. Analytical and simulation results are also presented.

Chapter 5 introduces a Universal Static Synchronous Compensator (U-STATCOM) based on a delta-connected cascade multilevel inverter. It is believed that the cascade multilevel inverter will be the major circuit to be used in STATCOM. Recently, all the researches regarding STATCOM have been focused on the wye-connected cascade

multilevel inverters. But STATCOM with this kind of circuit structure can only compensate reactive power and harmonics. Other than reactive power and harmonics compensation, the proposed U-STATCOM can also be used to compensate negative sequence current caused by unbalanced loads. The compensation theory based on delta-connected compensation network is illustrated. The operation principle and control scheme are verified by simulation results. For extended applications, the proposed circuit structure also can be used in D-STATCOM (STATCOM in distribute system).

Chapter 6 shows extended applications of multilevel inverters in Custom Power and DG. For Custom Power, a non-traditional cascaded multilevel inverter structure is proposed for a Dynamic Voltage Restorer (DVR). The non traditional multi-level inverter is created by cascading two uneven H-bridges. In this way, the inverter structure can operate as a nine-level cascade multilevel inverter and naturally splits the power conversion into two parts: 1) a higher-voltage lower-frequency power inverter, and 2) a lower-voltage higher-frequency conditioning inverter. The control strategy of the uneven cascade multilevel inverter is presented. For DG, three applications cascade multilevel inverters are proposed. The DC voltage regulator that used to transfer power from DC source to the cascade multilevel inverter is discussed in detail. An optimized circuit of the DC voltage regulator is identified. The analysis and comparisons between different circuits are shown to support the selection. The experimental results are also presented at the end of the chapter.

Chapter 7 shows a 17 level 1 MVA cascade multilevel inverter and the realization of its control unit. Experimental results from the inverter are shown to verify the proposed harmonics cancellation method.

Chapter 8 summarizes the content and the contributions of this work. Some recommendations for future work are also presented.

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CHAPTER 2

SUMMARY OF PREVIOUS WORKS

2. 1. Introduction

Since their initial introduction, multilevel inverters have received much research attention in all industrial areas. The first applications of multilevel inverters in power system are three level diode clamped inverters, which at the time were used in STATCOMs and UPFCs [76-78]. The newest trend of multilevel inverter applications in power system are the multilevel inverter based STATCOM [85-88], Back-to-Back DC Link [62-64], and DVRs [114, 115].

This chapter reviews the technical literature regarding the applications of multilevel inverters in power systems. First, the basic system structures and newest developments of different types of FACTs, Custom Power devices and DG interfaces are shown and explained. Then, technical literature of developments of multilevel inverters and their application in power system are fully reviewed and summarized.

2.2

2.2

2. 2. FACTs Devices

2. 2. 1 Structures and Functions of FACTs

Started in the 1970s, after more than two decades developments, FACTs devices have turned from concepts presented in papers to real Mega watts devices around the world.

The early FACTs devices were mostly thyristor controlled devices. By far, the most widely installed FACTs device is the thyristor controlled reactor or capacitor based Static VAR Compensator (SVC), which mainly controls voltage by injecting or absorbing reactive power to and from the grid. Till now, more than 1000 SVCs have been installed world widely [45-49].

With the development of power electronics, nowadays researches on FACTs devices are mainly focused on Voltage Source Inverter (VSI) based devices. VSI utilizes self-commutated power electronics devices, such as GTOs and IGBTs, to inverter DC to AC. Figure 2.1 shows a general three-phase VSI with IGBTs.

Compared with thyristor controller FACTs devices, the VSI based FACTs devices have better dynamic response and more versatile functions. That is the reason they are now also popularly called as FACTs controllers.

Major FACTs devices includes:

- **Static Synchronous Compensator (STATCOM)**-Controls voltage;
- **Static Synchronous Series Compensator (SSSC)**-Controls voltage, angle and impedance;

- **Unified Power Flow Controller (UPFC)**-Controls voltage, angle and impedance;
- **Interline Power Flower Controller (IPFC)**- Controls voltage, angle and impedance;
- **Back to Back DC Links (BTB)**-Controls the power transmission between two transmission systems.

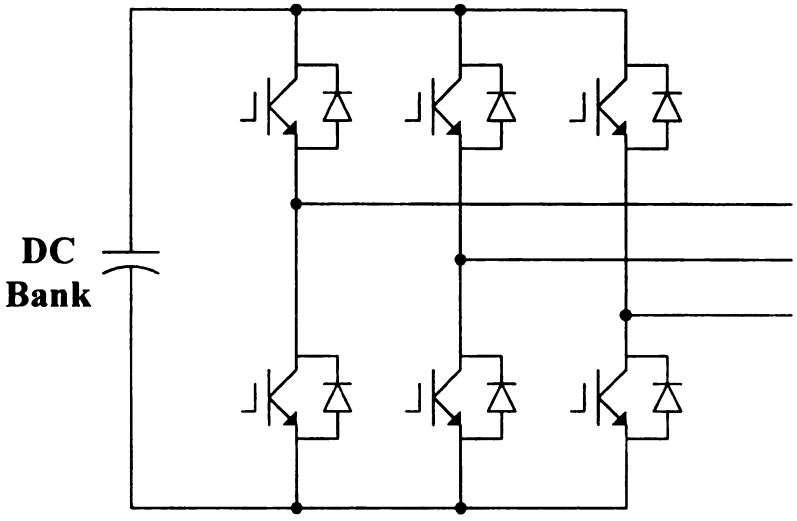


Figure 2.1: The VSI structure.

Figure 2.2 through Figure 2.6, together with a short description of the functions of each device gives the basic idea of how the FACTs devices benefit the grid.

a. STATCOM [78-92]

STATCOM is a VSI shunt connected to the grid. The VSI is controlled to inject or absorb reactive current to or from the grid, thus supporting the voltage and improving the system stability.

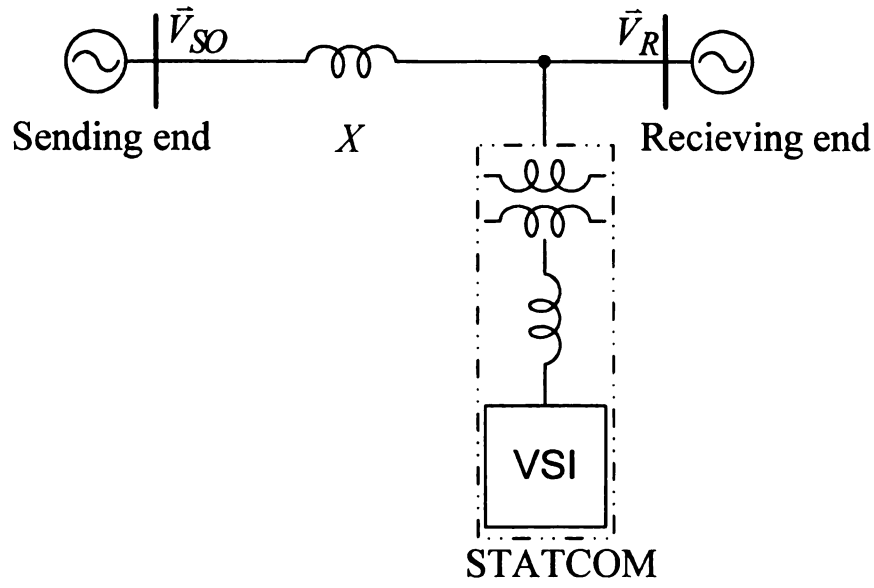


Figure 2.2: STATCOM Configuration.

***b. SSSC* [59-61]**

SSSC is a VSI connected in series with the grid through a transformer. It acts like a voltage source cascaded with the receiving end of the system. Thus by changing the receiving end's voltage, phase, and impedance, it changes the power flow over the grid.

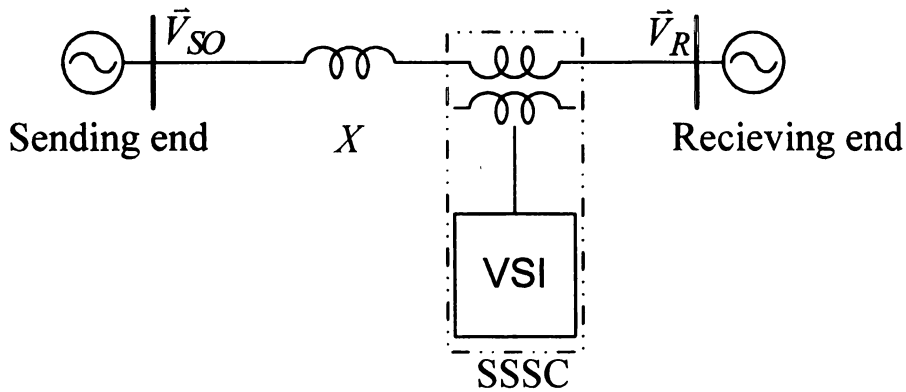


Figure 2.3: SSSC configuration.

*c. **UPFC*** [65-76]

A UPFC is the combination of a STATCOM and a SSSC by back-to-back connecting them together with a common DC link. With this combination, the UPFC inherits all the functions of the STATCOM and SSSC and maximize the operational region [65-72].

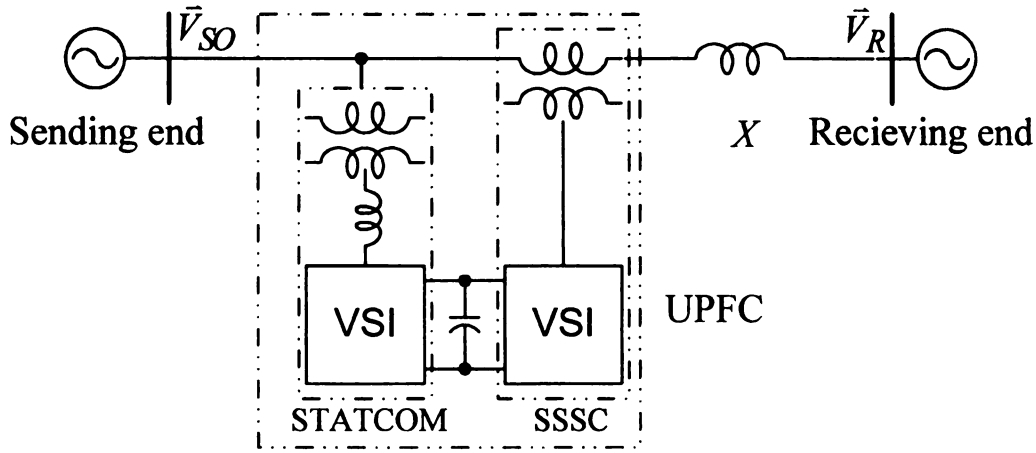


Figure 2.4: UPFC Configuration.

*d. **IPFC*** [57, 58]

IPFC is designed for use in multi-line transmission system. The VSIs share the same DC link, and are series connected in different transmission line. In other word, an IPFC is a combination of several SSSCs with one common DC link. In this structure, power flows from line to line through the DC link. With proper control, the power exchange between different lines can be conditioned and optimized. Similar as the SSSC, an IPFC controls the grid's voltage, phase and impedance.

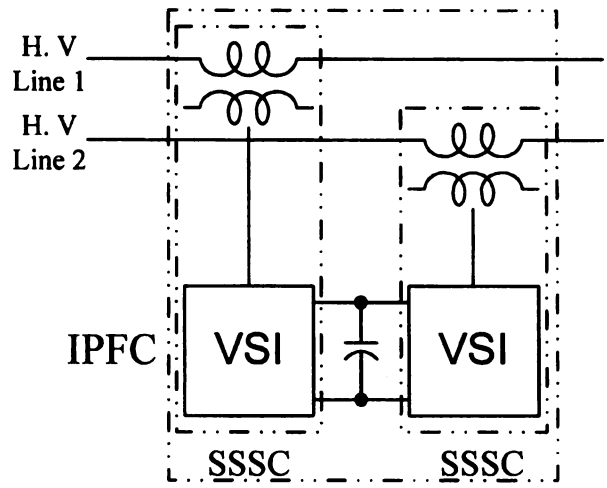


Figure 2.5: IPFC configuration.

e. ***BTB DC Link*** [62-64]

A Back-to-Back DC Link is used to connect two asynchronous systems together. Viewed from the each side of the systems, BTB DC link functions either as a voltage source or load depending on the direction of the power flow. The structure of the BTB DC Link is a combination of two STATCOMs with one common DC link. It controls the power flow between two asynchronous systems by allowing power flow through the common DC Link.

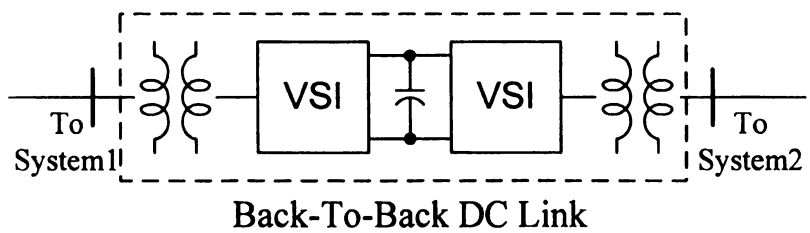


Figure 2.6: BTB DC Link configuration.

From the figures and descriptions above, it can be seen that the FACTs devices can be simply described as VSIs, either shunt or series connected to the grid through transformers. Table 2.1 summarizes circuit structures of FACTS devices.

Table 2.1: Summary of FACTs Configurations

FACTs Device	Number of VSI	Configuration
STATCOM	1	Shunt
SSSC	1	Series
UPFC	2	Shunt+Series back-to-back
IPFC	N (number of the High Voltage Lines)	Series back-to-back
Back-to-Back DC Link	2	Shunt back-to-back

2. 2. 2 History and Trends

Though it is not quite widely recognized, the world's first functional STATCOM was installed in 1991, in Inuyama Substation, Japan. The STATCOM is rated at 80 MVA, and connected to 154 kV bus. It was built and installed by Mitsubishi Electric [63, 78].

The world's first UPFC was commissioned in Inez, Kentucky, USA, in 1998, by American Electric Power (AEP). The UPFC is composed of one ± 160 MVA STATCOM and one ± 160 MVA SSSC [76, 77].

In 1999, the wolrd's first VSI based Back to Back DC link was put into operation in Japan. The BTB conveys 53 MVA of power between one 50 Hz and one 60 Hz system at 275 kV [63, 64].

Figure 2.7 shows the major FACTs devices that already have been installed in United States.

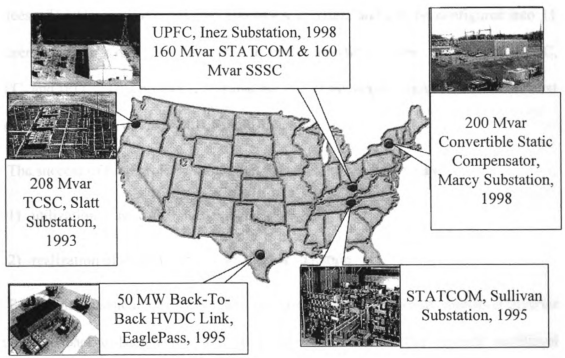


Figure 2.7: The installation of FACTs devices in United States.

In the newest developments of FACTs devices, two major projects show the trends of the FACTs.

One is the ± 75 MVA STATCOM for the 400 kV British National Grid [86, 87]. The STATCOM was built by Alstom and installed at East Clayton, UK, in the year 2000. The highlight of this project is that a cascade multilevel inverter is used as the basic circuit structure for the STATCOM. This, from one aspect, shows that the cascade multilevel inverter would be one of the major circuit candidates for the new STATCOMs in the years to come.

Another project is the ± 200 MVA Flexible Multi-functional Compensator, also called Convertible Static Compensator, which was commissioned at Marcy Substation, NY, in year 2002 [53, 54]. This Compensator stands for the latest generation of FACTs devices. The Compensator has two 100 MVA inverters and can be configured into 11 different configurations for a total of four basic operating modes: STATCOM, SSSC, UPFC, and IPFC. This project shows that the one of the major requirements for the next generation of FACTs devices will be multi-functional.

The success of both projects shows that the trends of the FACTs are:

1) utilization of cascade multilevel inverters; and

2) realization of multi functions with one installation.

But one inconsistency exists in these two trends. That is cascade multilevel inverter can not be back-to-back connected. It is generally believed that cascade multilevel inverters can not be used in UPFC and IPFC. Trying to overcome this problem and widening the applications of cascade multilevel inverter, this work proposes a new UPFC circuit configuration and a Universal STATCOM in the following chapters.

2. 2. Custom Power Devices

As Custom Power devices are in their infancy, there are very few useful standards to enable customers and suppliers to communicate performance requirements on these devices. But with the high demand of better power quality, all types of Custom Power Devices have already been installed around the world for both industrial and residential purposes [93-99].

The most common Custom Power Devices include:

- **Uninterrupted Power supply (UPS)**-Corrects voltage sag, momentary interrupt, and acts as backup power;
- **Dynamic Voltage Restorer (DVR)**-Corrects voltage sag;
- **Shunt/Series Active Power Filter (APF)**-Compensates harmonics and voltage unbalance;
- **Unified Power Quality Conditioner (UPQC)**-Compensates harmonics, voltage imbalance, reactive power, and voltage sag;
- **Distributed STATCOM**-Compensates reactive power, adjusts user end voltage.

Custom Power equipments are also based on VSIs. The configurations of Custom Power equipments are similar with the FACTs controllers. These two types of systems can be seen as applications of VSIs at different power system levels. Besides UPS, Custom Power devices are usually installed in medium voltage system (10 kV to 35 kV). The current ratings of Custom Power devices typically ranges from 300 A to 1200 A. The structures and operating principles of these devices are introduced as following.

a. Uninterrupted Power Supply (UPS)

UPS is the most widely used Custom Power devices. Currently there are three major types of UPS in the market: 1) Standby UPS; 2) Line Interactive UPS; and 3) Online UPS (also called 'True UPS').

Among these three, the Online UPS is the most promising and is receiving most of the research attentions. Figure 2.8 shows its basic structure. For this type of UPS, the power is sent to the load through the UPS all the time. During normal conditions, the battery in the UPS is charged, the power flows from the grid through the UPS to the load. When there is interrupt or voltage sag, the VSI is controlled to generate a stable voltage output. The battery is forced to supply partial or full power to the load.

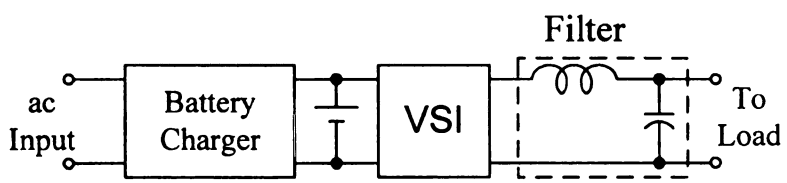


Figure 2.8: The basic Online-UPS system.

b. Dynamic Voltage Restorer (DVR) [114-125]

A DVR's main function is to correct voltage sag. Research shows that voltage sags contribute 92% of the voltage disturbance in power systems. Besides DVR, there have been several other commercially available solutions for voltage sag:

1) ***Static Transfer Switch (STS)***, which utilizes thyristor switches to transfer the load from the main power supply to a backup line; the drawback is the need for two power line;

2) ***Superconducting Magnetic Energy Storage (SMES),*** which provides a ride-through solution; high cost and the need for cooling are the main drawbacks;

3) ***Different storage type based UPS,*** like Flywheel UPS and battery UPS; the maintenance and cost are the limiting factors of their application.

DVR is usually used in medium voltage level and to compensate the voltage sag for all the loads that are connected to the feeder. Compared to other solutions mentioned above, DVRs have better performance, lower cost, less maintenance, and in some cases, have a comparatively smaller size. Figure 2.9 shows one basic structure of a DVR. It combines a VSI and a series-connected transformer to inject additional voltage during voltage sags. A grid connected rectifier or power storage device will supply the real power needed by the VSI.

In recent papers, it has been shown that the newest trend for the DVR is the utilization of cascade multilevel inverters [114, 115]. In Chapter 6, an uneven cascade multilevel inverter based DVR is also presented.

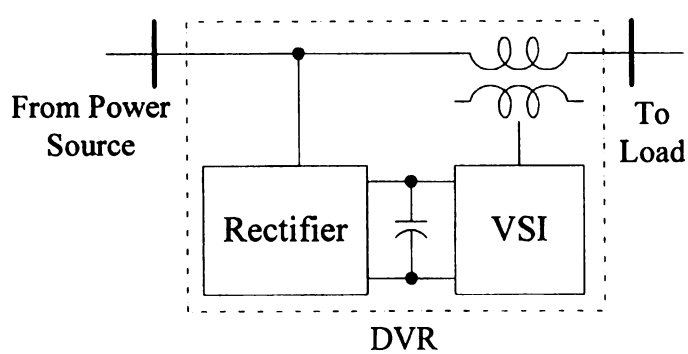


Figure 2.9: The DVR structure.

c. Active Power Filters (APF) [105-110]

APFs are mainly used to compensate the harmonics in current and voltage. There are two kinds of APFs: shunt APF and series APF. The shunt APF is a VSI shunted with the grid. It injects harmonics current to neutralize the harmonics in the load current. Series APF is a VSI series connected to the grid to generate a harmonics voltage to correct the input voltage and block the harmonics in the load current.

The realization of the APF needs an effective harmonics detection method and a coordinated control strategy. The harmonics detection methods are always strongly related with instantaneous power theory. Thus, the history of APF is also a history of instantaneous power theory and other modern power theories. Though the first Shunt APF was built more than 16 years ago [105], the research on APF still remains a hot topic in the power electronics world. New circuit structures, new control strategies, and arguments of different power theories still can be seen very often [100-104].

d. Unified Power Quality Conditioner (UPQC) [111-113]

UPQC is a combination of Shunt and Series APF by connecting them back-to-back together. The circuit structure is exact the same as its FACTs relative: UPFC. The difference is that the UPQC is aimed at the distribution system and mainly compensates harmonics, reactive power and system imbalance.

e. Distributed STATCOM (D-STATCOM)

D-STATCOM is the application of STATCOM at the distribution level. A D-STATCOM is usually installed near critical load and only guarantees the voltage and stability of the load direct paralleled with it. In recent years, D-STATCOM has become very popular as more and more end users begin to understand the damage that can be caused by the voltage problems [91].

2. 3. Distributed Generation [126-138]

As mentioned in Session 1.4, power electronics equipments are interfaces between the distributed power sources and the grid to distribute the generated power and provide ancillary services. Table 2.2 summarizes the types of DGs that involve power electronics interfaces.

Table 2.2: The DGs and their interface to grid

DG	Interface to Grid
Photovoltaic	dc-ac inverter
Wind turbine	ac-ac converter
Microturbine	ac-ac converter
Fuel Cell	dc-ac inverter

With the proper interface with the grid, DG can benefit the power system from all perspectives. The benefits are summarized as following [126-129]:

utility perspective

- transmission capacity relief

- distribution capacity relief
- hedge against high market prices

end-user perspective

- efficient use of energy from combined heat and power
- improved reliability by having backup generation and ancillary services (reactive power, voltage sag compensation, etc)
- incentives from utility to provide capacity reserve or power market hedge

commercial power producer perspective

- owner market (to sell power)
- to sell ancillary services (reactive power, standby capacity, etc.).

Recent research about DG includes maximum power tracking of photovoltaic and wind turbine, low cost inverter system, stability and other problems when connected with grid, and applications of cascade multilevel inverter.

2. 4. Multilevel Inverters

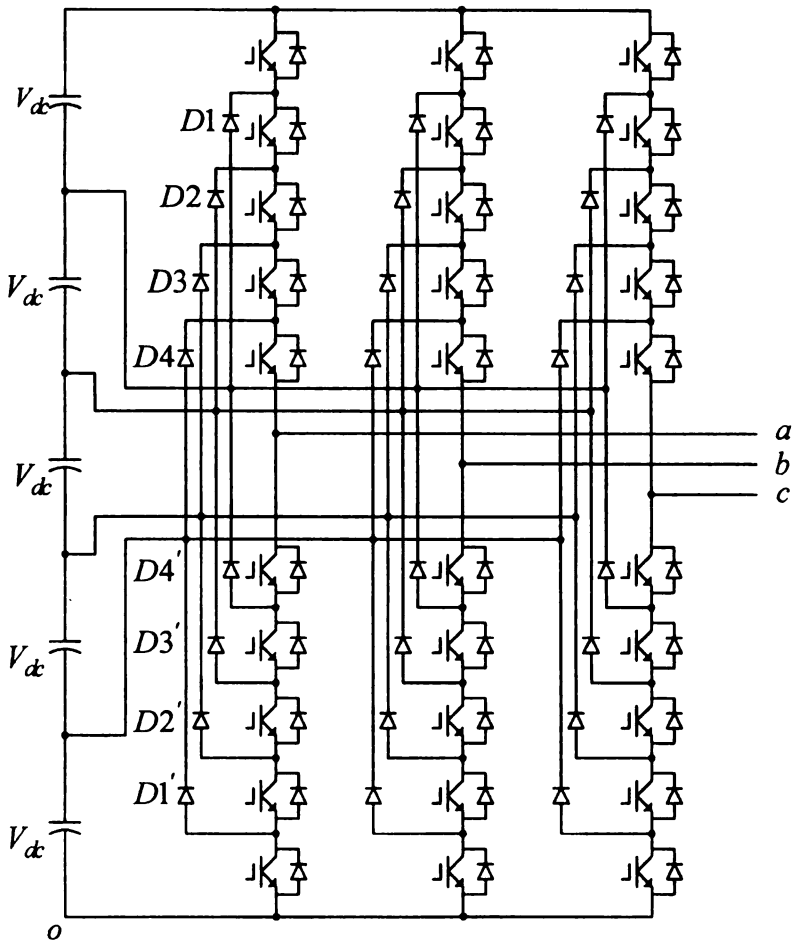
2. 4. 1. Diode Clamped Inverter [13-23]

The multilevel inverter family started with the 3 level diode clamped inverter in 1981 [13]. The first industrial application of the diode clamped inverter was for the bullet train in Japan. After two decades' of development, the diode clamped inverter has become the

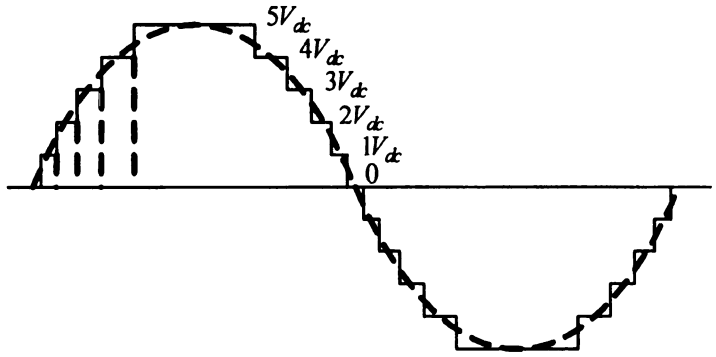
most widely used multilevel inverter in the world [14-23]. In the 1990's, people began to propose and build diode clamped inverters with more than 3 levels. Figure 2.10 shows the structure of a three phase, 6 level diode clamped multilevel inverter and its output line-line voltage waveform. In the DC bus of the inverter, there are five capacitors in series. The voltage cross each capacitor is V_{dc}. Thus by turning on and off the switches following a particularly sequence at pre-calculated angles, the phase voltage can be 0, 1 V_{dc}, 2 V_{dc}, 3 V_{dc}, 4 V_{dc}, and 5 V_{dc} correspondently. By proper synthesizing V_{ao} and V_{bo} together, the line-line voltage, V_{ab}, can change from -5 V_{dc} to +5 V_{dc}. In real applications, $\theta_1 \sim \theta_5$, is usually calculated according to the desired modulation index and harmonics elimination. In multilevel inverters, the modulation index is defined as the following:

$$MI = \frac{V_{peak}}{\frac{4}{\pi} N \cdot V_{dc}}, \qquad (2.1)$$

where V_{peak} is desired peak value of fundamental frequency in the staircase waveform, N is the maximum number of the level. In equation (2.1), the coefficient $4/\pi$ is the amplitude of the fundamental component of a unit square waveform.



(a). The 6 level diode clamped inverter.



(b) The line-line voltage.

Figure 2.10: The six level diode clamped inverter and its line-line waveform.

In the diode clamped inverter, three phases share the same DC bank, which makes the back-to-back connection possible. The switching frequency of the inverter is minimized to the fundamental frequency. Each active switching device has same voltage and current stress. However, each clamping diode in the circuits needs to clamp different voltage levels. For example, the clamping voltage for D1 and D1' is V_{dc}, whereas D4 and D4' clamp $4V_{dc}$.

In summary, the major advantages and disadvantage of the diode clamped inverter are:

Advantages:

- Low switching frequency;
- Feasibility for back-to-back connection;

Disadvantage

- Different voltage ratings for different clamping diodes.

Till now, diode clamped inverters have mostly been used in medium voltage drives [15-17]. The major power system applications of this kind of inverter include STATCOM, interface between DC and AC transmission line, and back-to-back connected power conditioners [18-20].

2. 4. 2. Flying Capacitor Multilevel Inverter [24-30]

Flying capacitor multilevel inverters were first introduced by Meynard and Foch in 1992 [24]. A three-phase, 6 level flying capacitor multilevel inverter is shown in Figure

2.11. Each capacitor shown in Figure 2.11 has the same voltage. All the switching devices have the same voltage and current stress.

This kind of inverter has similar structure as the diode clamped inverter. The difference is that it utilizes capacitors other than diodes to clamp the voltage. With this kind of structure, the flying capacitor multilevel inverter has more switching state redundancy in producing the staircase waveform. But at the same time, the bulky capacitors also make the system more expensive and difficult to build. The charge and balance of the capacitors in the inverter also makes the control more complex [25-28].

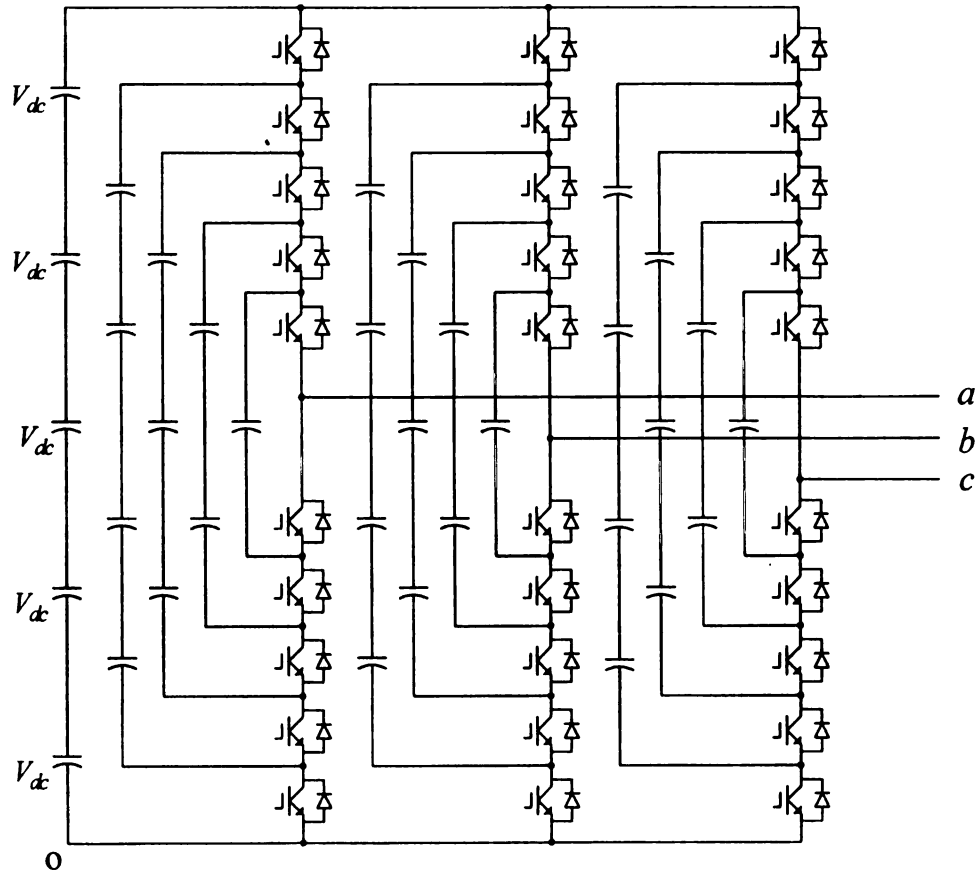


Figure 2.11: The 6 level flying capacitor multilevel inverter.

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The advantages and disadvantages of flying capacitor multilevel inverter are summarized as following:

Advantages:

- More switch state redundancy;
- Large number of capacitors, which enables better performance during voltage sags;

Disadvantages:

- High cost and high volume caused by the large number of the capacitors;
- More complex control required to balance the voltages cross each capacitor.

Flying capacitor multilevel inverters are suitable for all the applications that are suitable for diode clamped inverters. But due to their disadvantages, applications of this type of inverters are seldom reported [29, 30].

2. 4. 3. Cascade Multilevel Inverter [31-42]

Cascade multilevel inverter is quite different from the aforementioned two multilevel inverters. It utilizes H-bridge inverter units by cascading them together to produce desired staircase waveform. Each H-bridge has a separated DC source and can produce 0 and ± 1 V_{dc} voltage levels. Thus, the phase voltage would have 2N+1 levels, where N is the number of separated DC sources per phase. Figure 2.12 shows the wye-connected three-phase 11 level cascade multilevel inverter.

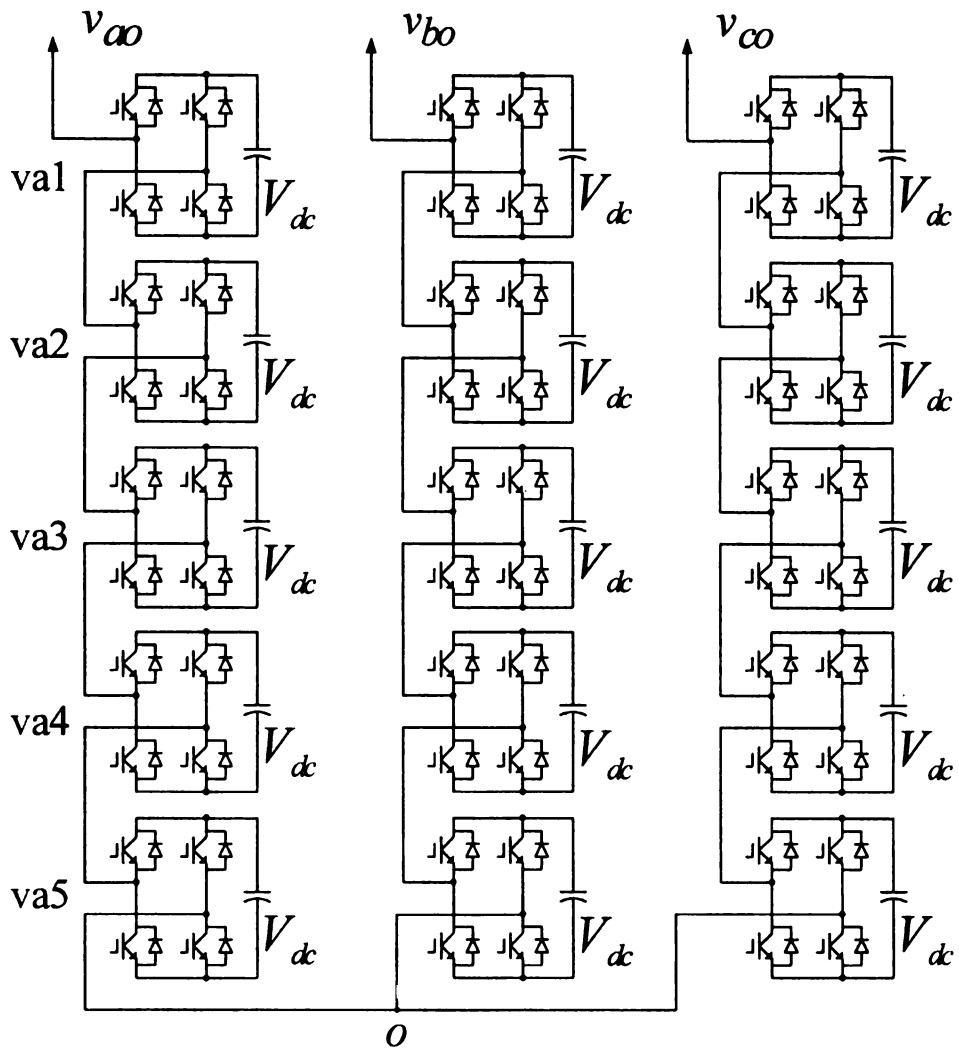

Figure 2.12: 11 level cascade multilevel inverter.

Each module in Fig 2.12 produces a three level staircase waveform at different duty cycle. As modules' outputs are cascaded with each other, the phase waveform as shown in Figure 2.13 can be achieved.

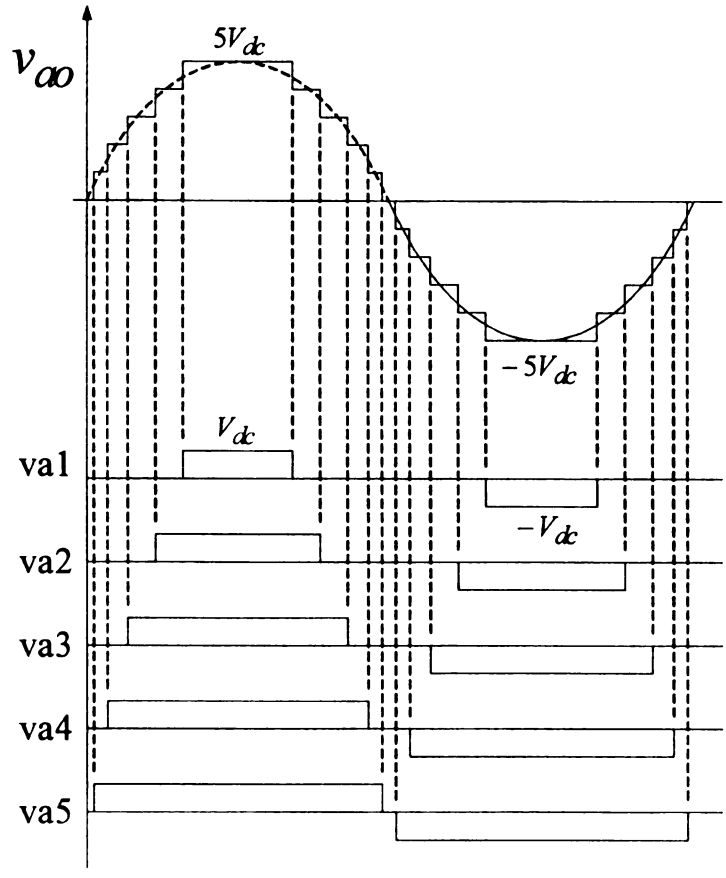

Figure 2.13: The phase voltage of an 11 level cascade multilevel inverter.

Because the H-bridge can be modularized, the cascade multilevel inverter is now the most favored circuit for new designs of power system compensation and large motor drives. Applications of cascade multilevel inverters in HEV are also proposed [41].

As for power system applications, Peng, Lai, Joo, Visser and other authors have demonstrated that cascade multilevel inverters can be either shunt or series connected to the grid to act as power conditioners such as STATCOM and DVR [36-40]. Full comparisons between different circuit candidates for STATCOM are made in [85]. It is proved that the cascade multilevel inverter is by far the best choice for STATCOM.

One of the most important features of the cascade multilevel inverter is that separated DC sources are needed. This feature, on one hand, prevents connecting two cascade multilevel inverters back-to-back together; on the other hand, makes cascade multilevel inverters the best choice for many conditions that a lot of DC sources that are used for generation purpose, such as fuel cells and photovoltaic cells in DG.

The main advantages and disadvantages are summarized as following:

Advantages:

- Utilization of modularized H-bridges, which lowers the cost and makes the manufacture and maintenance much easier;
- Maximal utilization of the DC sources by producing 2N-1 level phase voltage;
- The best choice for HEV, fuel cell and photovoltaic applications where many small DC power cells are involved;

Disadvantages

- The need for separate DC sources, which makes it not infeasible for back-to-back connection applications.

2. 5. Applications of Multilevel Inverters in Power System

After the above review of FACTs device, Custom Power, DG and the multilevel inverters, the feasible application of multilevel inverters in power systems can be summarized in Table. 2.3.

Table 2.3: The feasible applications of multilevel inverters in power system

FACTs					
	STATCOM	SSSC	UPFC	IPFC	Back-to-Back DC Link
Diode Clamped Multilevel Inverter	√	√	√	√	√
Flying Capacitor Multilevel Inverter	√	√	√	√	√
Cascade Multilevel Inverter	√	√	X	X	X
Customer Power					
	UPS	DVR	APF	UPFC	D-STATCOM
Diode Clamped Multilevel Inverter	√	√	√	√	√
Flying Capacitor Multilevel Inverter	√	√	√	√	√
Cascade Multilevel Inverter	√	√	√	X	√
DG					
	Photovoltaic	Fuel Cell	Wind Turbine	Microturbine	
Diode Clamped Multilevel Inverter	√	√	√	√	
Flying Capacitor Multilevel Inverter	√	√	√	√	
Cascade Multilevel Inverter	√	√	√	√	

2. 6. Summary

In this chapter, the developments of FACTs, Custom Power and DG were reviewed first. Then three major multilevel inverters were introduced one by one. Their circuit structures, advantages and disadvantages were explained. The literature about their developments and applications were reviewed. In the end, their feasible power system applications of multilevel inverters were summarized.

By utilizing multilevel inverters in power system applications, the bulky transformers usually used for traditional inverters can be eliminated, whereas the stresses on the switches can be greatly reduced. Because of its modular structure, among the three major types of the multilevel inverters, cascade multilevel inverter is the most suitable one for power system application.

All the applications of multilevel inverters in power systems have some common implemental issues. So before breaking into detailed application cases, the next chapter will first address the following most common implemental issues of multilevel inverters: maintenance and balance of DC bank voltages and harmonics elimination in output voltage.

CHAPTER 3

REAL APPLICATION ISSUES OF MULTILEVEL INVERTERS

3. 1. Introduction

DC bank (capacitor) voltage maintenance and balance, and output voltage harmonics elimination are the three most important issues for real applications of multilevel inverters in power systems. Without well maintained and balanced DC banks, the synthesis of a stable staircase voltage waveform would be impossible. To meet the THD requirement of the power system, the switching angles of multilevel inverters must be optimized to eliminate the lower order harmonics.

This chapter introduces the methods to maintain and balance the DC bank voltages, and proposes a practical harmonics elimination method.

3. 2. DC Bank Voltage Maintenance and Balance

3. 2. 1. DC Bank Voltage Maintenance

In all the power system applications of multilevel inverters, it is always crucial to maintain DC bank voltages at a certain value. But depending on different applications, the ways to maintain the voltages are also different. Summarized in the nature of the applications, basically, there are three different conditions for DC bank voltage maintenance:

1) pure reactive and harmonics compensation;
2) back-to-back connected applications; and
3) distributed generations applications.

a) pure reactive and harmonics compensation

In the case of STATCOM, SSSC, and APF, the multilevel inverter only outputs or absorbs reactive power. Ideally, no real power is consumed by the inverter. Thus, the DC bank voltage should automatically maintain. But in the real applications, there is always power loss in the multilevel inverters. Besides power loss on parasitic resistance in the bus bar, wires, inductors and capacitors, the switches and diodes have switching loss and conduction losses. In most cases, the major power loss of multilevel inverters is from the switches and diodes. Without compensating for the power loss in the inverter, the DC bank voltages will drop gradually, and the desired functions of the inverter can not be realized.

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To compensate for the power loss and adjust the DC bank voltages to the desired value, the inverter needs to be controlled to absorb or output a small amount of real power. Usually, a simple PI controller would be used to decide how much real power is needed by the inverter.

In the cases where multilevel inverters are shunt connected to the utility line, such as STATCOM and Shunt-APF, the real power exchange between the inverter and the utility line is realized by controlling the inverter to send and absorb real current as shown in Figure 3. 1.

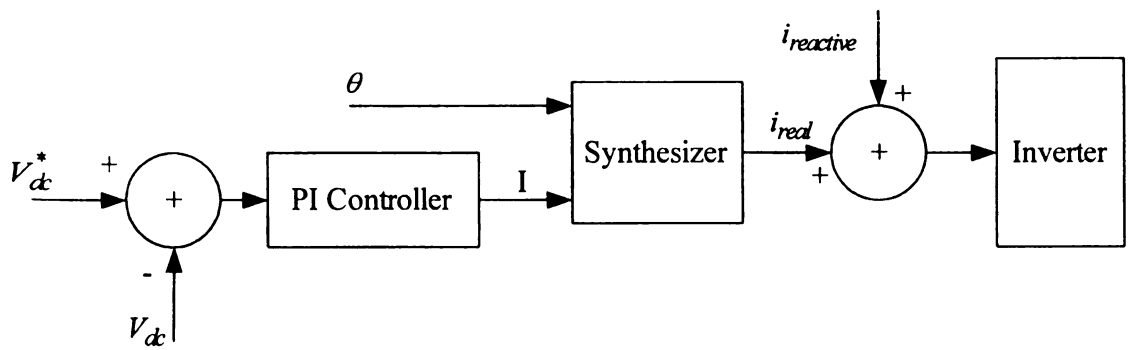

Figure 3.1: The DC bank voltage maintenance for shunt connected inverter.

Assuming all the DC banks in the multilevel inverter are balanced, only one DC bank voltage is monitored. The monitored voltage, V_{dc}, is compared with the desired DC bank voltage, V_{dc}^*. The result is fed into the PI controller to calculate the amplitude of the needed real current. Then, together with the detected phase angle of the utility phase voltage, θ, an instantaneous real current reference, i_{real}, can be synthesized. The

multilevel inverter would be controlled by the combination of the reactive current command, $i_{reactive}$, and real current reference, i_{real}.

Similarly, in the series connected cases, such as SSSC and Series-APF, the multilevel inverters could be controlled to output a voltage in phase with the utility phase current to absorb or output real power to maintain the DC bus voltage.

Another commonly used method for shunt connected inverter is to control the shunt inverter to output a voltage, which has a slight angle difference from the grid voltage. In this method, the inverter and grid can be seen as two AC voltage sources connected together through the inductor. Thus, the power flow in these cases will obey equation (1.1) and (1.2). With the slight angle difference between inverter voltage and grid voltage, real power can flow into or out of the inverter.

b) back-to-back connections

In the back-to-back connection systems like UPFC, UPQC, IPFC, and BTB, the DC bank acts as a link to transfer the real power from one inverter to another.

For example, in UPFC, the SSSC is controlled to inject a voltage to the utility line. If the phase angle difference between the injected voltage and utility phase current is not 90°, real power flow will occur between the SSSC and the utility line. Thus, the SSSC will charge or discharge the DC link. To maintain the DC link voltage, the STATCOM should be controlled to absorb or output the same amount of real power to charge or discharge the DC link to make the total charge or discharge to zero. At the same time, the power loss in both inverters will tend to lower the DC link voltage. So the STATCOM also needs to be controlled to compensate for the power losses. Figure 3.2

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shows one example of the real power flow in the UPFC. The shadowed arrows indicate the real power flow in the UPFC.

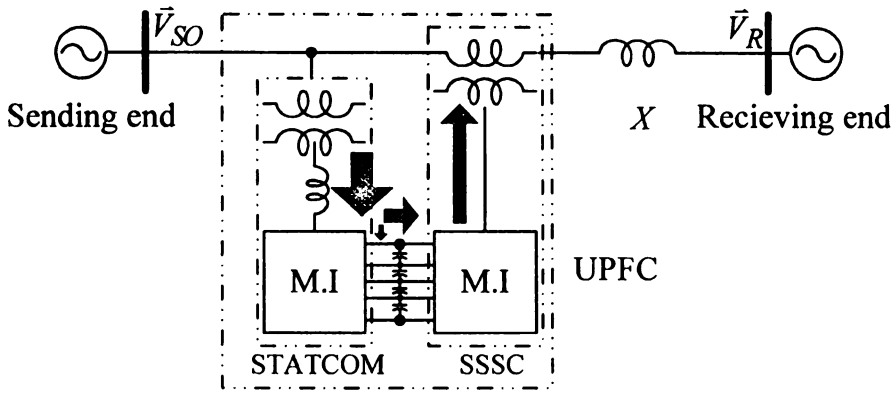

Figure 3.2: Example of real power flow in UPFC.

c) distributed generations

In DG, the DC banks of the inverters are powered by energy sources like fuel cells and wind turbines. Between a DC bank and an energy source, there always is a voltage regulator to regulate the input voltage to the DC bank. Depending on applications, the regulator can be a dc-dc converter or a rectifier cascaded with a DC-DC converter. The DC-DC converter will be discussed in detail in Chapter 6.

3. 2. 2. Balance of DC Bank Voltages

Though the circuit structure and applications of multilevel inverters may be different, the methods to balance the DC bank voltages can be the same. In this section, an 11 level voltage waveform and corresponding general current waveform is used to show how to balance the DC bank voltages.

As shown in Figure 3.3, each level of the voltage waveform is realized by utilizing the voltage on different DC banks. The current has a phase angle difference from the fundamental of the voltage waveform. Thus, the current has both reactive and active components, which stands for a general condition. The power consumption on each DC bank can be calculated as:

$$P_n = \frac{1}{2\pi}\left(\int_{\theta_n}^{\pi-\theta_n} V_{dc}\cdot i(\theta)\cdot d\theta + \int_{\pi+\theta_n}^{2\pi-\theta_n} V_{dc}\cdot i(\theta)\cdot d\theta\right). \quad (3.1)$$

Since θ_n is different for each level, the power consumption on each DC bank during one fundamental cycle is also different. Further more, the conduction loss and switching losses that faced by each DC bank are also different too. So, without any voltage balance procedure, the DC bank voltages in the multilevel inverter would be different from each other.

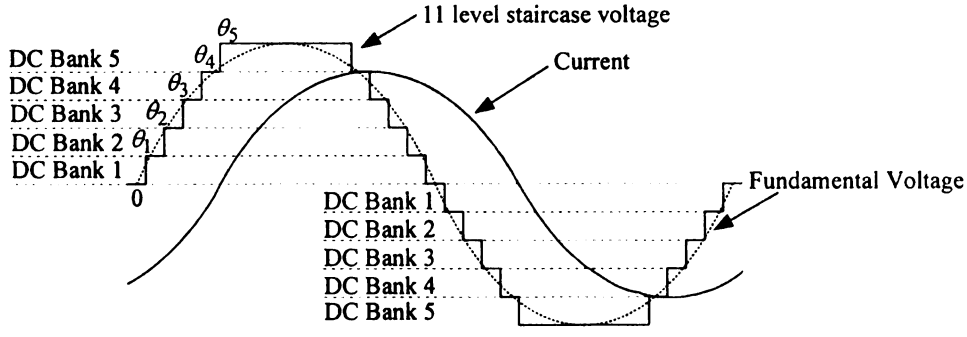

Figure 3.3: 11 level voltage waveform and general current waveform.

One simple solution to avoid the unbalance between the DC banks is to rotate the switching angles between DC banks, as shown in Figure 3.4. By rotating the switching

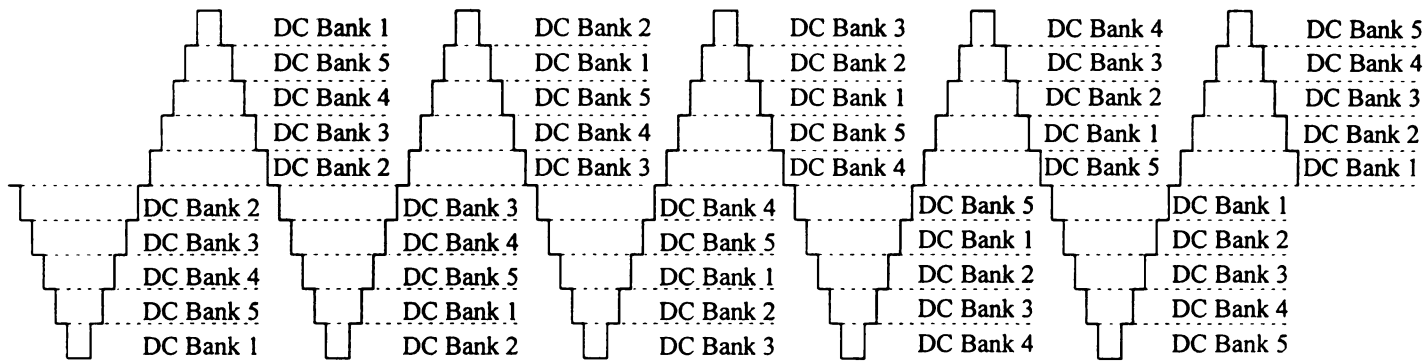

Figure 3.4: Rotation for DC Bank balancing.

angles through each DC bank, after five fundamental cycles, each DC bank would have experienced exactly the same amount of power consumption. Thus, the DC bank voltages will be balanced.

3. 3. Harmonics Elimination

Since the first introduction of the multilevel inverters, many harmonics elimination methods have been proposed [6, 9, 139-143]. But harmonics elimination still remains as a major and hot topic for the multilevel inverters. A simple and practical way to solve this problem is still needed.

To answer the call of a simple solution, a new practical harmonics elimination method is proposed in this dissertation. Unlike other methods published before, the proposed method does not need to solve high order polynomials. Only four simple equations and minimum calculation time are needed to realize the elimination of selected harmonics. Experimental results based on the proposed method will be shown in Chapter 7.

3. 3. 1. Existing Harmonics Elimination Methods

Till now, there are two major types of harmonics elimination methods: 1) PWM methods, which include both sinusoidal PWM and space vector PWM methods [140-143]; and 2) optimized switching angles methods [6, 9, 139].

The PWM methods are usually used when the number of voltage steps is quite limited, e.g., 2 or 3 steps. The performance of these methods is decided by the switching

frequency. The higher the switching frequency, the lower the harmonics content in the lower frequency range.

Optimized switching angle methods are often used for cases with more voltage steps. The switching frequency in these methods is the same as the fundamental frequency. The number of eliminated harmonics is decided by the number of voltage steps.

In this section, only optimized switching angle methods are discussed. The general 11 level voltage waveform is shown again in Figure 3. 5 as an example to explain how the optimized switching angle methods work.

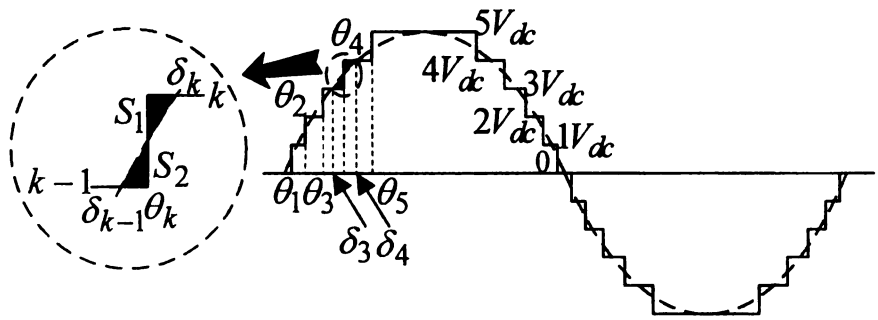

Figure 3.5: 11 level voltage waveform and equal area criteria.

The Fourier series expansion of the voltage waveform shown in Figure 3.5 is

$$V(\omega t) = \sum_{m=1,3,5,\cdots}^{\infty} \frac{4V_{dc}}{m\pi}(\cos(m\theta_1) + \cdots \cos(m\theta_N))\sin(m\omega t), \qquad (3.2)$$

where N is the number of switching angels and m is the harmonic order.

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Based on equation (3.2), ideally, the optimized switching angles, $\theta_1 - \theta_5$, can be found by solving the following equation groups

$$\begin{cases} \frac{4V_{dc}}{\pi}(\cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)+\cos(\theta_4)+\cos(\theta_5)) = V_F \\ \cos(5\theta_1)+\cos(5\theta_2)+\cos(5\theta_3)+\cos(5\theta_4)+\cos(5\theta_5) = 0 \\ \vdots \\ \cos(13\theta_1)+\cos(13\theta_2)+\cos(13\theta_3)+\cos(13\theta_4)+\cos(13\theta_5) = 0 \end{cases} . \quad (3.3)$$

In this equation group, the first equation will guarantee the desired modulation index, where V_F is the desired fundamental voltage. The followed equations will ensure the elimination of 5^{th}, 7^{th}, 11^{th}, and 13^{th} harmonics. To eliminate more harmonics, more switching angles and more voltage steps are needed. But with more angles, the equation group would have more equations and higher orders.

Methods proposed in [6, 9, 139] essentially are methods that try to solve the equation group (3. 3) with different approaches. Due to the high order polynomial nature of the equation groups, there are several disadvantages of these kinds of methods:

1) these methods usually involve complex algorithm and huge calculation time; when the number of switching angle increases, the capability limitation of contemporary computer algebra software would be easily reached;

2) the number and order of polynomial equations increase with the switching angles;

3) only $N-1$ harmonics can be eliminated;

4) the algorithms in these methods are often based on special theories, which makes it difficult for users to re-perform the methods.

Researches shows that to solve the simplest case like equation groups (3. 3), it still takes special algorithm and long calculation times to solve. For larger and higher order equation groups, there would be a point that to find the solutions becomes impractical [6, 9, 139].

3. 3. 2. Proposed Harmonics Elimination Method

A. The Basic Idea of the Proposed Method

The proposed method in this work tries to solve the harmonic elimination problems from a totally different approach. No high order multi-variable polynomial equations would be involved in proposed method.

Unlike all the other methods, the proposed method is not originated from equations, but from the basic ideas of switching angle initialization and utility line harmonics compensation.

To better illustrate the proposed method, equal area criteria and harmonics compensation principle of APF are first introduced and restated as following:

1) The equal area criteria for switching angle calculation.

In the earlier papers about multilevel inverters, the equal area criterion is introduced as one method to calculate the initial value of switching angles. The calculated initial values will be used in the process of solving equation group (3. 3). The basic idea of equal area criteria is also shown in the circled area of Figure. 3.5.

The initial switching angle, θ_k is found by solving

$$S1 = S2, \tag{3.4}$$

where $S1$ and $S2$ are the areas of the shadowed part in Figure. 3. It has been proven that by using the equal area criteria, the fundamental of the stair case waveform would resemble the sinusoidal modulation waveform. However, with only equal area criteria, no harmonics elimination can be realized.

The proposed method tries to answer the question of how to utilize the initial values from equal area criteria to find the optimized angles without solving the high order multi-variable polynomials equations.

2) Harmonics injection in Active Power Filters

As mentioned in Chapter 2, Active Power Filter (APF) is used to eliminate voltage and current harmonics in utility line.

APFs will inject new harmonic voltages or currents into the utility line to eliminate harmonics that already exist in the utility line. The injected harmonics would have the same amplitudes but opposite phase angles of the selected harmonics they are intended to eliminate. Thus the harmonics in the utility line are neutralized.

The key point of harmonics elimination in APF is to realize harmonics elimination by injecting new harmonics. Combining equal area criteria and the idea of harmonics injection together, a new method to find optimum switching angles can be found.

B. The Proposed Method

The proposed method indeed is a combination of equal area criteria and harmonics injection. The basic idea behind this method is described as following:

1) by using equal area criteria, pure sinusoidal modulation waveform, $h_1 = v\sin\omega t$, will derive a set of angles $\theta_1 - \theta_N$;

2) the staircase waveform formed by $\theta_1 - \theta_N$ will have the fundamental component, $h_1^{'}$, and harmonics content $h_3, h_5, h_7 \cdots h_m$, the fundamental component, $h_1^{'}$, will resemble the sinusoidal modulation waveform, h_1;

3) ideally, if take $(-h_5 - h_7 \cdots - h_m)$ as the modulation waveform, by using equal area criteria, another set of angles, $\theta_1^h - \theta_N^h$, can be found; the staircase waveform formed by $\theta_1^h - \theta_N^h$ would have component $-h_5^{'} - h_7^{'} \cdots - h_m^{'}$ and other higher order harmonics; due to the nature of equal area criteria, $-h_5^{'} - h_7^{'} \cdots - h_m^{'}$ will resemble $-h_5 - h_7 \cdots - h_m$;

4) so if use $h_1 - h_5 - h_7 \cdots - h_m$ as the modulation waveform to find a series of switching angles, the selected harmonics content in the resulted staircase waveform would be around $h_5 + h_7 \cdots + h_m - h_5^{'} - h_7^{'} \cdots - h_m^{'}$; because $-h_5^{'} - h_7^{'} \cdots - h_m^{'}$ resembles $-h_5 - h_7 \cdots - h_m$, the harmonics elimination is partly realized.

5) if the same process in 2)-4) is iterated, the harmonics elimination can finally be realized.

To implement this idea, the following five steps need to be followed.

1) first, based on equal area criteria, find the initial switching angles ($\theta_1 - \theta_N$) for a given modulation waveform, h_1, at a certain modulation index;

2) then find the non-third harmonics content ($h_5, h_7 \cdots h_m$) of the staircase waveform formed with switching angles , $\theta_1 - \theta_N$; the 5th, 7th, and all the way to the mth harmonics are the selected harmonics for elimination;

3) subtract the harmonics content, $h_5, h_7 \cdots h_m$, from the original modulation waveform h to form a new modulation waveform, $h - h_5 - h_7 \cdots - h_m$; for the first iteration, $h = h_1$; from this step, the modulation waveform would have injected harmonics and become nonsinusoidal;

4) finally, use the new nonsinusoidal modulation waveform to calculate a new set of ($\theta_1 - \theta_N$) based on the equal area criteria;

5) repeat steps 2)-4) until achieving the best switching angles, which would result in zero selected harmonics content.

In step 1), the modulation waveform is pure sinusoidal, after step 3), the harmonics are already injected; the modulation waveform would never be sinusoidal again. The more the iteration, the more the harmonics in the modulation waveform. Though the

modulation waveform has large injected harmonics content, the stair case waveform formed by the final switching angles would have almost no selected harmonics.

To prove the concept, this method has been used to calculate the switching angles for the case shown in Figure 3.3. In the calculations, five harmonics are chosen for elimination. After about 100 times of iterations, the values of 5^{th}, 7^{th}, 11^{th}, 13^{th}, and 17^{th} harmonics drop under 10^{-6} p.u, which means these harmonics are totally eliminated. The number of totally eliminated harmonics is equal to the number of switching angles, N. For a desktop computer with a 2.8 GHz CPU, the calculation time of one modulation index is less than 1 second. Table 1 shows the switching angle examples for modulation index at 0.85 and 0.86. The modulation index is defined as:

$$MI = \frac{V_F}{\frac{4}{\pi} N \cdot V_{dc}}, \tag{3.5}$$

where V_F is the peak value of the fundamental components.

Table 3.1: Switching angles examples

	θ_1 (rad.)	θ_2 (rad.)	θ_3 (rad.)	θ_4 (rad.)	θ_5 (rad.)
MI=0.85	0.11466	0.25769	0.41205	0.6465	1.0134
MI=0.86	0.11465	0.2577	0.41202	0.64646	1.0134

C. The Four Equations

To perform the 5 steps listed above, there are only four equations that need to be calculated:

Equation 1: to use the equal area criteria, δ_k, the junction point of the modulation waveform and voltage level k must first be found. For a modulation waveform with harmonics contents, it is difficult to find a symbolic solution for δ_k, but a numeric value can easily be found by doing simple iterations of the following equation:

$$\delta_k = arctg(\frac{k \cdot V_{dc} + h_5 \sin(5\delta_k) \cdots h_m \sin(m\delta_k)}{V_F \cos(\delta_k)}). \tag{3.6}$$

Equation 2: after δ_k s are found, the switching angle, θ_k, can easily be calculated from

$$\theta_k = k\delta_k - (k-1)\delta_{k-1} + V_F(\cos(\delta_k) - \cos(\delta_{k-1})) - \frac{h_5}{5}(\cos(5\delta_k) - \cos(5\delta_{k-1}))$$

$$\cdots - \frac{h_m}{m}(\cos(m\delta_k) - \cos(m\delta_{k-1})), \tag{3.7}$$

where m is the order of the harmonic;

Equation 3: with a new set of θ_k, the new harmonics contents can be found as

$$h_m = \sum_{k=1,2,\cdots N}^{N} \frac{2}{(2k-1)\pi}(\cos(m\theta_k) - \cos(m(\pi - \theta_k))); \tag{3.8}$$

Equation 4: to perform iterations of step 2)-4) mentioned earlier in this section, the modulation waveform would have a general expression as:

$$V_F \sin(\omega t) - h_{5\_s} \sin(5\omega t) \cdots - h_{m\_s} \sin(m\omega t), \tag{3.9}$$

where h_{m_s} is the sum of the h_m found after every iteration,

$$h_{m\_s} = \sum_{i=1,2,3\cdots iter}^{iter} h_m \,. \tag{3.10}$$

For different numbers of switching angles and eliminated harmonics, the four equations will remain the same. Since there is no multi-variable polynomial, the calculation time has a near linear relationship with the number of the switching angles. No huge increase in calculation time is expected when there is a small change in the number of the switching angles.

D. Application Issues of Proposed Method

Like all the other switching angle optimizing methods, the proposed method also has its limitations. Thus, modifications of the proposed method are needed at certain modulation index and voltage step combinations. The following part of this section will discuss the limitations and possible solutions.

1) In equal area criteria method, $h_1^{'}$ is not totally equal to h_1, thus the fundamental component of the final staircase waveform will be slightly different from the original modulation waveform. This means that try to find the switching angles

for a modulation index, a different initial modulation index is needed. This problem can be solved by calculating switching angles at different initial modulation indexes and using these to form a mapping table between the initial and desired modulation index.

2) Directly applying the proposed method will not always guarantee desired harmonics elimination for all the modulation indexes with all kinds of voltage steps. This is mainly caused by possible multiple solutions or no solutions of δ_k after harmonics injection. With a pure sinusoidal waveform, at each voltage step, there is only one solution of δ_k. But after the harmonics injection, the modulation waveform may have more than one junction point at a certain voltage step, meanwhile, the junction at the highest voltage step may disappear. In these cases, judgment and corresponding modification in the method should be made.

3) It is quite difficult to find a symbolic solution for δ_k, thus the harmonics elimination is very hard to be qualitatively described. This makes it not very inconvenient to further modify this method to improve the harmonics elimination performance at different switching angle numbers and modulation indexes.

3. 4. Summary

In this Chapter, first, methods to maintain DC bank voltages at different application situations were summarized. Then, a universal DC bank voltage balancing method was introduced. Finally, a practical harmonics elimination method was proposed.

In the applications of multilevel inverter in power systems, there are three conditions for DC voltage maintenance. In this chapter, the conditions of reactive power compensation and back-to-back connection were discussed. The voltage regulator used in DG will be discussed in Chapter 6. For DC bank voltage balance, one universal method is introduced. The same method was used in the experiments that will be shown is Chapter 7.

Before the proposed method, the optimized switching angles are always found by solving high order multi-variable polynomial equation groups, whereas the proposed method only involves four simple equations. Compared with the existing methods, the proposed method is much simpler and more practical.

Since the applications of multilevel inverter in power systems and their implemental issues have been fully reviewed and discussed, from the next chapter, individual application cases will be discussed.

Chapter Four

A NOVEL UPFC WITH CASCADE MULTILEVEL INVERTER

4. 1. Introduction

The idea of the Unified Power Flow Controller (UPFC) was first proposed by L. Gyugi in 1992 [65]. By far, the UPFC is the most sophisticated FACTs device. Since its first introduction, many papers about the UPFC have been published in the last decade. Papers by Gyugi, Sen, Fujita, Keri and many other authors summarize the UPFC's theory, modeling, analysis, control, and field applications [65-73]. Papers by Fardanesh and Sanchez examine the possibility of using diode clamped multilevel inverters for the UPFC [75, 76]. Papers by Wang investigate the multivariable design of a multiple-functional UPFC [74].

However, till now, almost no paper has ever challenged the UPFC's back-to-back circuit configuration. In this Chapter, the functions of the UPFC, as well as its

conventional configuration, are briefly described, and then a new circuit configuration is proposed. Comparisons between the new and conventional configurations show that the proposed configuration has several unique features and advantages over the conventional configuration. As a result, the cascade multilevel inverter can be used in the new configuration to lower the volume and cost, and at the same time increase the reliability of the system. Analysis and simulation results are presented.

4. 2. The Conventional UPFC

The UPFC combines the functions of several FACTS devices and is capable of realizing voltage regulation, series compensation, and phase angle regulation at the same time, thus realizing simultaneous separate control of active power and reactive power transmitted over the line. The conventional circuit configuration of the UPFC is shown in Figure 4.1 [65-74].

As it can be seen, the conventional UPFC configuration consists of two voltage source inverters. Inverter 1 is in parallel with the transmission line, while Inverter 2 is in series with the transmission line. The two inverters are connected back-to-back through a common DC-link. This arrangement enables real power flow in either direction between the two inverters.

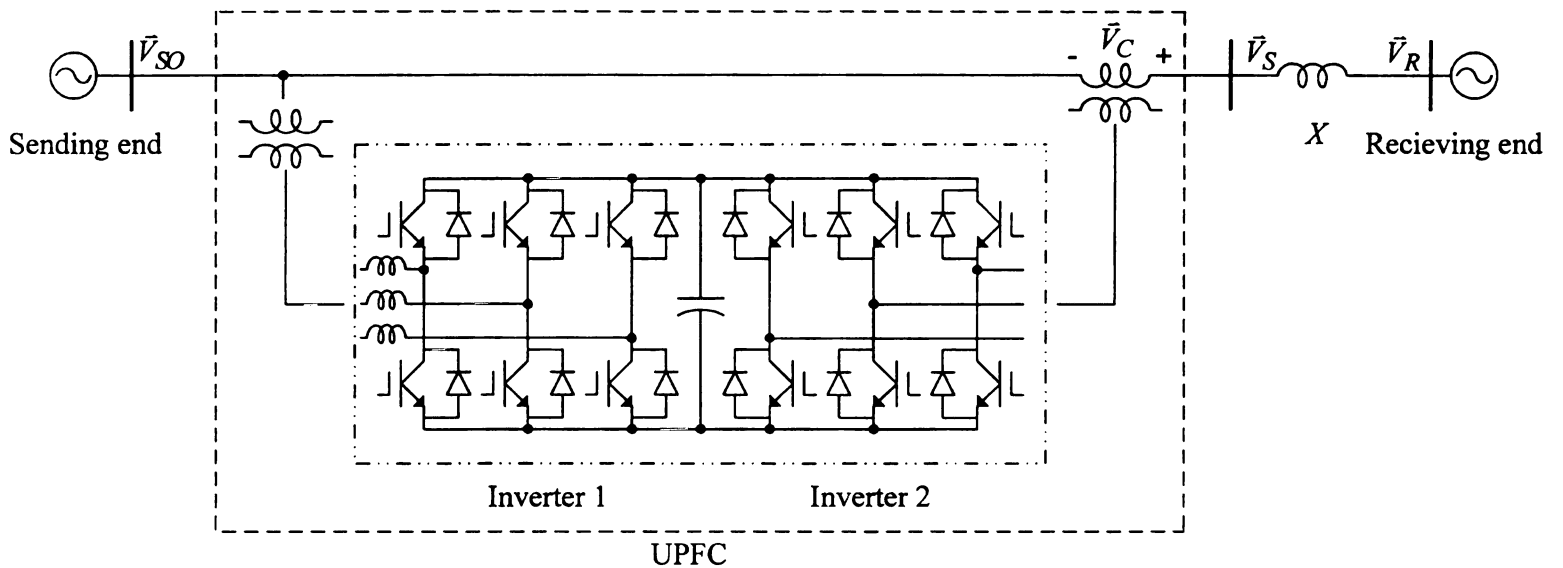

Figure 4.1: Conventional circuit configuration of UPFC.

Between the two inverters, Inverter 2 provides the main function of the UPFC by injecting an AC voltage $\vec{V}_C$ through a series connected transformer. $\vec{V}_C$ has controllable magnitude V_C ($0 \le V_C \le V_{C\max}$) and phase angle δ ($0 \le \delta \le 360^\circ$). Thus, Inverter 2 can be considered as a synchronous AC voltage source. Because the transmission line current flows through this voltage source, Inverter 2 needs to exchange active and reactive power with the transmission line through the transformer. The needed reactive power can be generated independently by Inverter 2 itself. The active power exchange is actually provided through the common DC link.

Thus, the basic function of the Inverter 1 is to supply or absorb the real power demanded by Inverter 2 at the common DC link. Besides this, Inverter 1 also can generate or absorb reactive power independently.

Figure 4.2 is a vector diagram of Figure 4.1, illustrating the principle of the UPFC. When $\vec{V}_C$ is added to the system, the equivalent sending end voltage changes from $\vec{V}_{SO}$ to $\vec{V}_S$, the angle difference between the sending end and the receiving end voltages changes from θ to θ', the active and reactive power transmitted from the sending end to the receiving end over a transmission line changes from

$$P = \frac{V_{SO} V_R \sin\theta}{X} \tag{4. 1}$$

and

$$Q = -\frac{(V_R \cos\theta - V_{SO}) V_{SO}}{X} \tag{4. 2}$$

to

$$P' = \frac{V_S V_R \sin\theta'}{X} \tag{4.3}$$

and

$$Q' = -\frac{(V_R \cos\theta' - V_S)V_S}{X}. \tag{4.4}$$

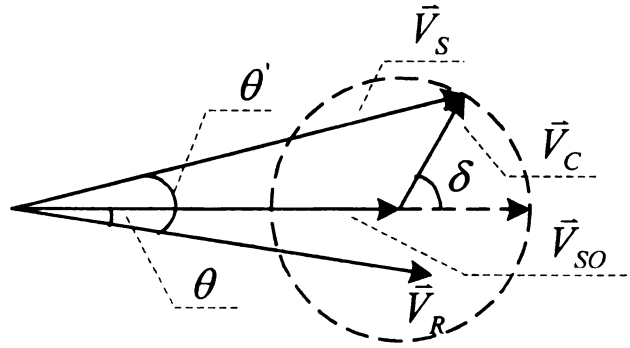

Figure 4.2: Basic UPFC control function.

where V_{SO} is the amplitude of $\vec{V}_{SO}$, V_S is the amplitude of $\vec{V}_S$, V_R is the amplitude of $\vec{V}_R$, and X is the line impedance. The equations show power transmitted over the transmission line can be modified to the desired value by controlling the injected voltage, $\vec{V}_C$.

To summarize, the features of the conventional configuration are:

1) Both inverters share the same DC link;

2) Both inverters need to exchange active power with each other and the transmission line;

3) A transformer is usually used as an interface between the transmission line and each inverter.

4. 3. Two Problems of the Conventional Configuration

4. 3. 1. Zigzag Transformer

In the real applications of FACTs devices like the UPFC and the STATCOM, multi-pulse inverters with zigzag transformer were often used to substitute for the inverters as shown in Figure 4.1. The multi-pulse inverter is formed by back-to-back connecting several three phase inverters, and then cascading the AC outputs at secondary sides of the zigzag transformer. One 48 pulse inverter with zigzag transformer is shown in Figure 4.3.

In the multi-pulse inverter, each three phase inverter cell is controlled to output the same three level line-line voltages. The switches in the inverters turn on and off only once per fundamental cycle. Thus, the switching losses of the devices are minimized.

The zigzag transformer will realize the phase shifting and output cascading. The purpose of the phase shifting is to optimize harmonics content. The primary sides of the zigzag transformer are delta-connected to eliminate 3^{rd} harmonics. The phase shifting of each secondary side for the 48 pulse inverter is 7.5°. The total output of the multi-pulse inverter with zigzag transformer will resemble the waveform of multilevel inverters. The phase voltage of the 48 pulse inverter has a maximum of 23 voltage levels.

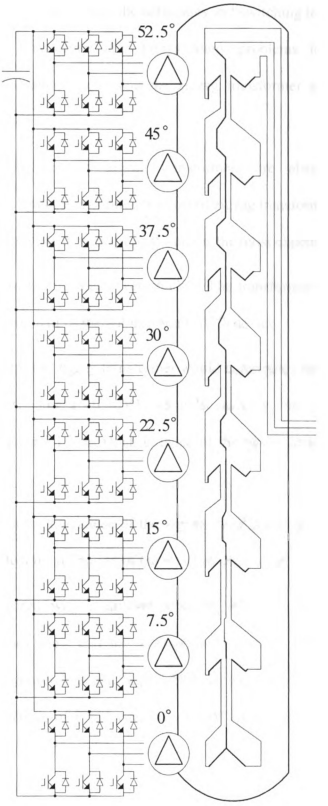

Figure 4.3: The 48 pulse inverter.

By utilizing the zigzag transformer, the harmonics and switching loss are both limited. However, the zigzag transformer also brings many problems to the multi-pulse transformer. The disadvantages of using the zigzag transformer are summarized as following:

1) Unlike switching devices, zigzag transformers are always custom-made. Compared with regular transformer, the cost of zigzag transformer is much higher. In the multi-pulse system, zigzag transformer is the most expensive part.

2) Zigzag transformers are usually very bulky. The transformer itself alone would make up more than half of the volume of a FACTs device.

3) The power loss on the zigzag transformer would contributes more than half of the total power loss. For a 40 MVA, 48 pulse inverter, the power loss on the transformer is around 1.2%, which is twice of the power losses on the switches [85].

4) The operation and maintenance of the zigzag transformer is very crucial, which will strongly affect the reliability of the multi-pulse inverter.

Furthermore, compared with multilevel inverters with the same amount output voltage levels, researches show that the multi-pulse inverter would have higher cost, higher volume, higher power loss and higher THD in the output voltage [36-40, 85]. Thus, in the future practices of FACTs devices, multilevel inverters will be the major circuit candidates.

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4. 3. 2. The Problem with Cascade Multilevel Inverter

Among the three major types of multilevel inverters, the cascade multilevel inverter is the one most suitable for most FACTs applications. The reason for this is that the H-bridge in the cascade multilevel inverter can be modularized, which would make it much easier for manufacture and maintenance.

But unfortunately, the cascade multilevel inverter can not be used for the back-to-back configuration of conventional UPFC structure. If two cascade multilevel inverters are back-to-back connected as shown in Figure 4.4, short connections of DC banks will form during certain operation states. In Figure 4.4, the dashed line shows one current path that indeed shorts the upper capacitor. When the shadowed parts in the inverters conduct at the same time, the upper capacitor will be shorted.

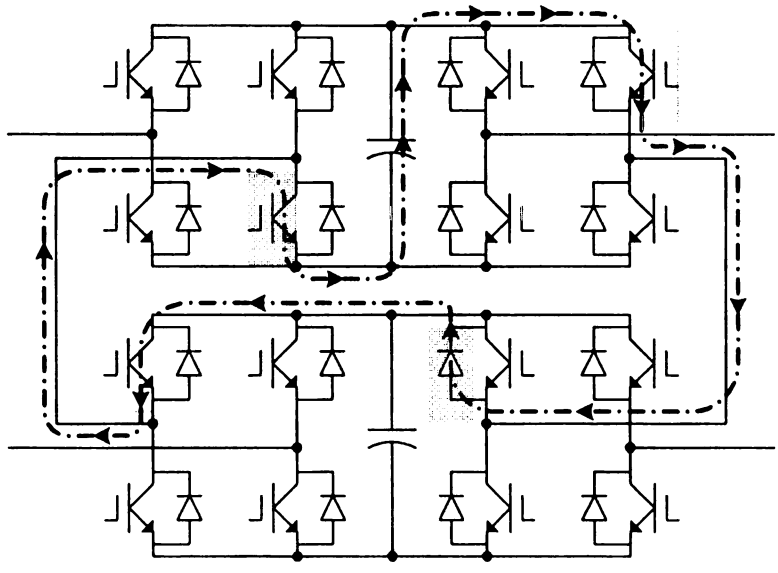


Figure 4.4: The short connection when cascade multilevel inverters are connected back-to-back.

4. 4.The Proposed Configuration

4. 4. 1. The Proposed Configuration

In an attempt to eliminate the zigzag transformer and utilize the cascade multilevel inverter in the UPFC, a new UPFC circuit configuration as shown in Figure 4.5 is proposed. In the proposed configuration,

1) each inverter has its own DC bank, thus cascade multilevel inverters can be used in place of Inverter 1 and Inverter2;

2) since cascade multilevel inverters can be utilized, the zigzag transformer is no longer needed in the proposed configuration;

3) there would be no active power exchange between the two inverters and the line because the two inverters use separated DC banks;

4) unlike the conventional back-to-back DC link coupling, the two inverters are coupled face-to-face on the AC sides instead.

Like in the conventional configuration, Inverter 2 in the new configuration is still controlled to generate the desired $\vec{V}_C$ to control the active and reactive power flow, thus acting as a controlled voltage source.

Inverter 1, the parallel inverter, rather than supplying or absorbing active power for Inverter 2, injects a current to the line to guarantee that active power flowing into both of the inverters be zero.

While cascade multilevel inverters can be used for this circuit configuration, the zigzag transformers are no longer needed. However, for Inverter 2, a connection

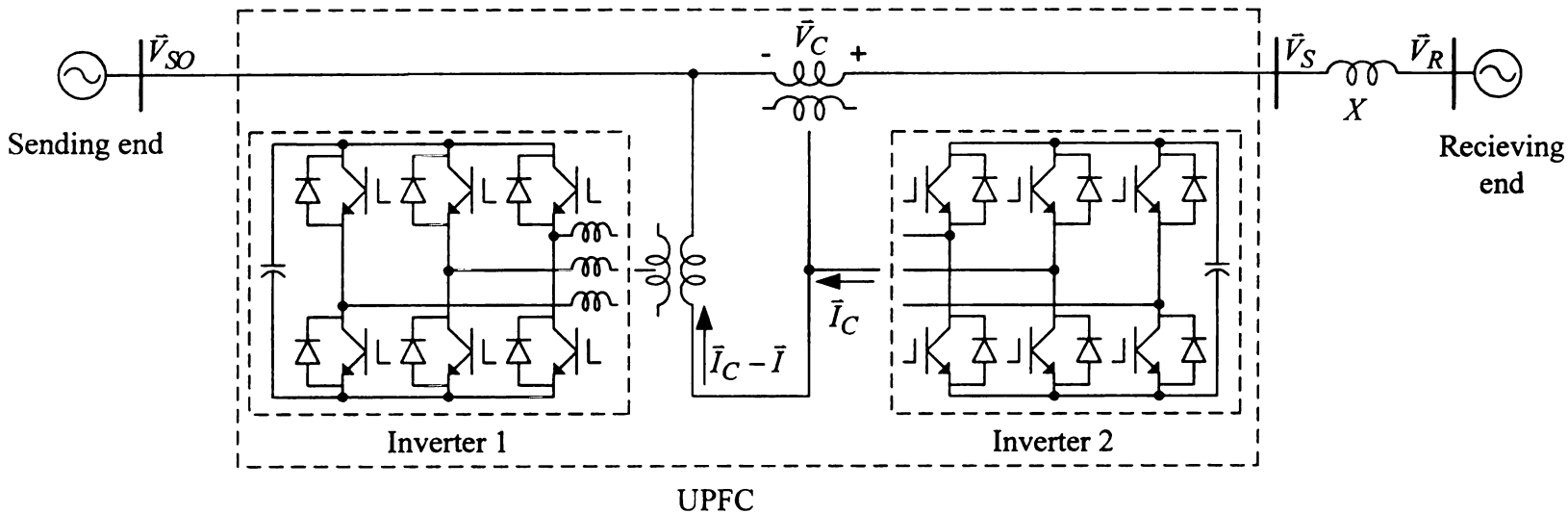


Figure 4.5: The proposed circuit configuration of UPFC.

transformer is still needed to connect the inverter to the utility line. Compared with the zigzag transformer, the connection transformer is much cheaper, much smaller, and more reliable.

The proposed configuration utilizing cascade multilevel inverters is shown in Figure 4. 6.

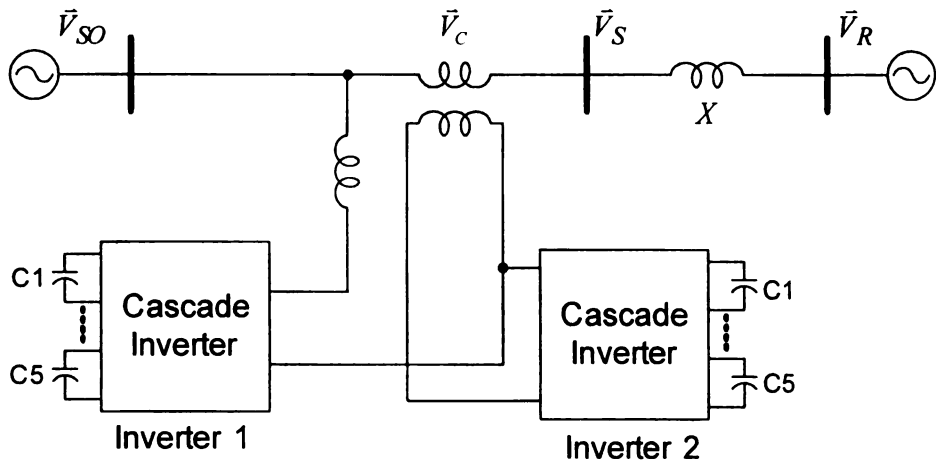


Figure 4.6: The proposed UPFC with cascaded multilevel inverter.

4. 4. 2. Control Strategy

Figure 4.7 is the equivalent circuit of the proposed configuration. When Inverter 2 is controlled to output the desired compensation voltage, $\vec{V}_C$, the voltage drop on Inverter 1 would automatically be $\vec{V}_{SO} - \vec{V}_C$. To ensure zero active power flow through both inverters, Inverter 2 current, $\vec{I}_C$, and Inverter 1 current, ($\vec{I}_C - \vec{I}$), should be

perpendicular to their voltage drops, $\vec{V}_C$ and $(\vec{V}_{SO} - \vec{V}_C)$, respectively, where $\vec{I}$ is the receiving end line current.

In summary, the control command for Inverter 2 is the desired compensation voltage, $\vec{V}_C$, while the control command for Inverter 1 is $\vec{I}_C - \vec{I}$. $\vec{V}_C$ can easily be calculated according to the power demand of the system. After $\vec{V}_C$ is given, the desired $\vec{I}_C - \vec{I}$ can be found by the following analysis:

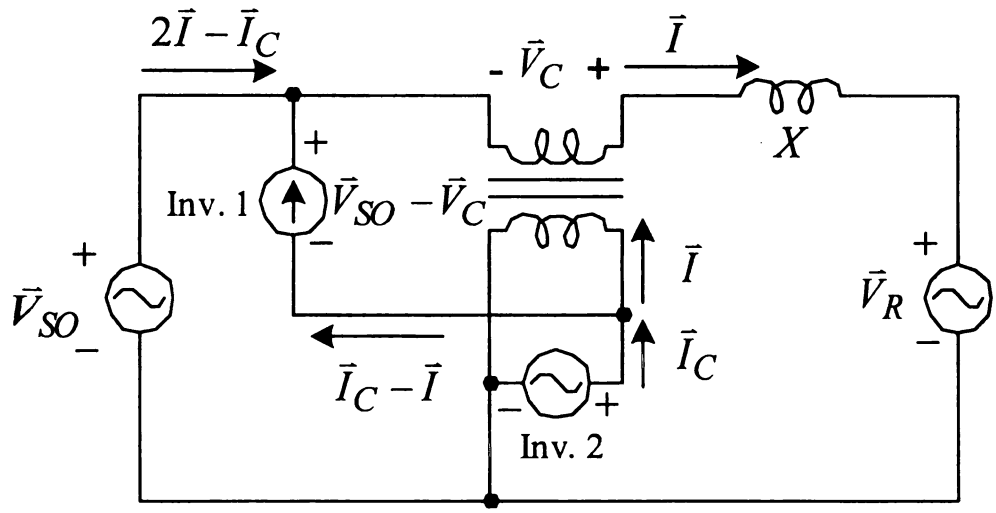


Figure 4.7: The equivalent circuit of UPFC.

To ensure that the active power flowing into Inverter 2 is zero, given that the phase angle of the $\vec{V}_C$ is δ, the phase angle of $\vec{I}_C$ should be

$$\angle \vec{I}_C = \delta \pm 90^0, \tag{4.5}$$

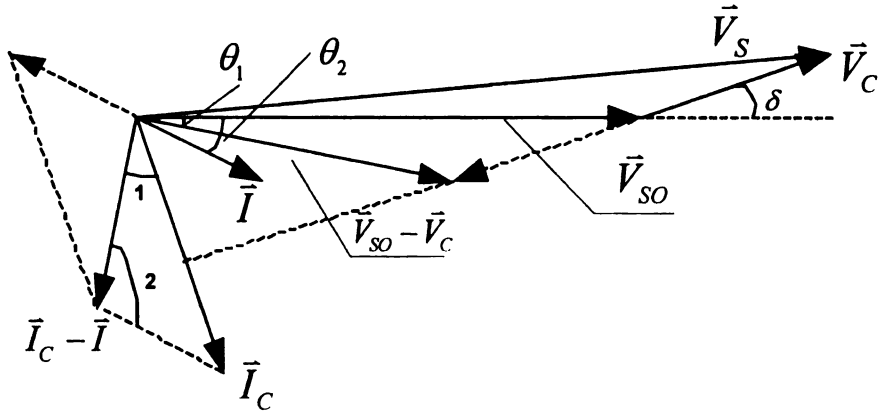


Figure 4.8: The relationship between $\vec{V}_C$ and $\vec{I}_C$.

Based on the analysis above and Figure 4.5, the equation of the active power flowing into Inverter 1 can be written as

$$P_1 = (\vec{V}_{SO} - \vec{V}_C)\cdot(\vec{I}_C - \vec{I})$$

$$= V_{SO} I_C \cos(\delta \pm 90^0) + V_C I \cos(\delta - \theta_2) - V_{SO} I \cos\theta_2 = 0. \qquad (4.6)$$

From equation (4. 6), the amplitude of $\vec{I}_C$ could be found to be:

$$I_C = \frac{V_{SO} I \cos\theta_2 - V_C I \cos(\delta - \theta_2)}{V_{SO} \cos(\delta \pm 90^0)} \qquad (4.7)$$

Combine equation (4. 5) and (4. 7), we have

$$\vec{I}_C = \frac{V_{SO} I \cos\theta_2 - V_C I \cos(\delta - \theta_2)}{V_{SO} \cos(\delta \pm 90^0)} \angle \delta \pm 90^0. \qquad (4.8)$$

In equation (4. 8), V_{SO}, I, and θ_2 can be measured with sensors; V_C and δ are pre-calculated. Since $\vec{I}$ is measured with sensors, after $\vec{I}_C$ is decided, the control command of Inverter 1, ($\vec{I}_C - \vec{I}$), is also decided.

4. 5. Comparison of the New and Conventional Configurations

The proposed configuration of the UPFC has several advantages over the conventional one:

1) In the conventional configuration, there is active power exchange between the two inverters, whereas in the new configuration there is no active power exchange between the two inverters and both inverters only provide (or absorb) reactive power;

2) Cascade Multilevel Inverter can be used to eliminate the zigzag transformers, which reduces power losses, cost, and volume, and increases reliability of the system;

3) The modular structure of cascade multilevel inverters and its inherent redundancy provide greater flexibility to system design and maintenance;

4) The total VA rating of the UPFC can be greatly reduced under most load conditions, which will be verified in the following section.

4. 6. VA Rating Analysis

For the conventional UPFC, the VA rating for Inverter 1 and Inverter 2 are:

$$S_{1O} = \sqrt{(V_C \cdot I\cos(\angle \vec{V}_C - \angle \vec{I}))^2 + (V_{SO} I_q)^2}\ , \text{and } S_{2O} = V_C I\ , \qquad (4.9)$$

where I_q is the reactive current that Inverter 1 generates for reactive power compensation. In the equation, $V_C \cdot I\cos(\angle \vec{V}_C - \angle \vec{I})$ is the real power required by Inverter 2. Therefore, the total VA rating of the conventional UPFC configuration is

$$S_O = S_{1O} + S_{2O} = \sqrt{(V_C \cdot I\cos(\angle \vec{V}_C - \angle \vec{I}))^2 + (V_{SO} I_q)^2} + V_C I\ . \qquad (4.10)$$

For the proposed UPFC, the VA rating for Inverter 1 and Inverter 2 are:

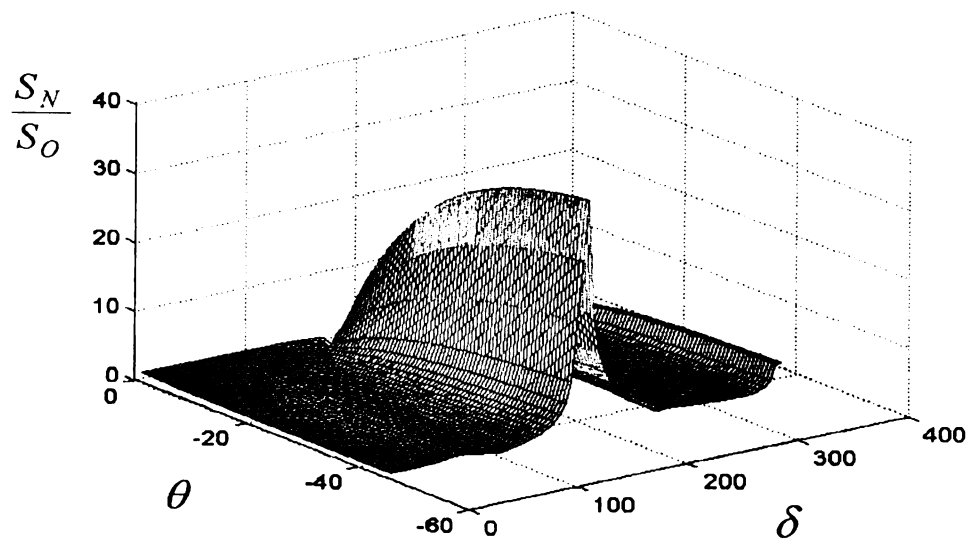
$$S_{1N} = \left|\vec{V}_{SO} - \vec{V}_C\right| \cdot \left|\vec{I}_C - \vec{I} + \vec{I}_q\right|, \text{ and } S_{2N} = V_C I_C\ . \qquad (4.11)$$

Thus the total VA rating of the new UPFC configuration is

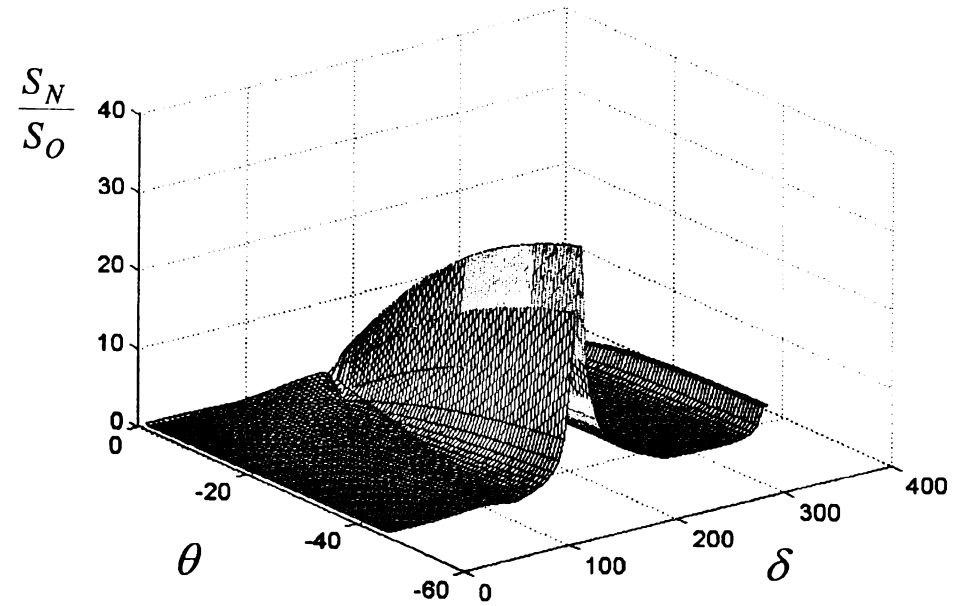
$$S_N = V_C \cdot I_C + \left|\vec{V}_{SO} - \vec{V}_C\right| \cdot \left|\vec{I}_C - \vec{I} + \vec{I}_q\right|. \qquad (4.12)$$

Figure 4.9 and 4.10 show the ratio of the total VA rating between the new and conventional configuration, S_N / S_O.

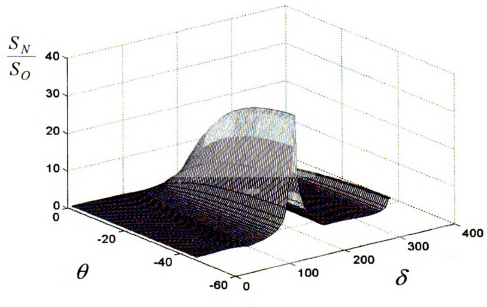
According to equation (4. 7) and (4. 12), in the new configuration, when δ is exactly at 0° and 360°, the Inverter 2 current and total system VA rating would become infinite. This means that the new configuration is not suitable for δ very close to 0°. Further calculations show that when δ changes from 0.6° to 359.4°, the Inverter 2 current and system VA rating will be in an acceptable region.



(a) $V_C = 0.5$ p.u. and $I_q = 0$ p.u.

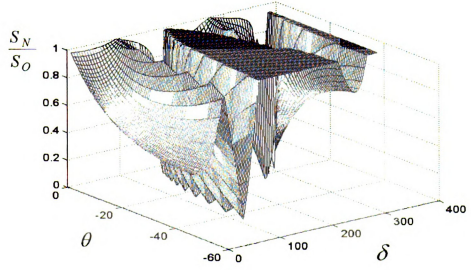


(b) $V_C = 0.5$ p.u. and $I_q = 0.25$ p.u.

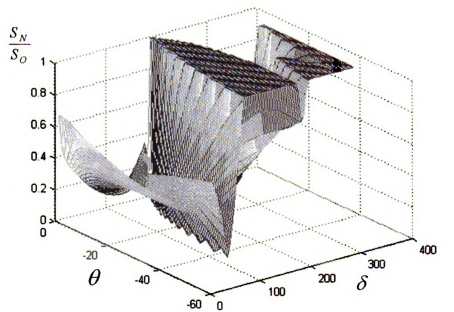


(c) $V_C = 0.5$ p.u. and $I_q = -0.25$ p.u.

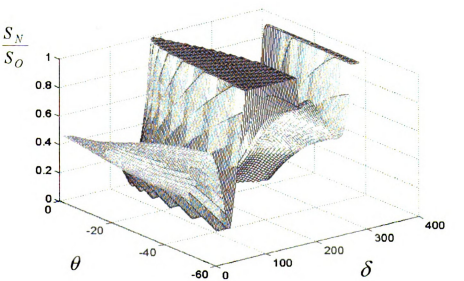
Figure 4.9: The full view of total VA rating between the new and conventional configuration.



(a) $V_C = 0.5$ p.u. and $I_q = 0$ p.u.



(b) $V_C = 0.5$ p.u. and $I_q = 0.25$ p.u.



(c) $V_C = 0.5$ p.u. and $I_q = -0.25$ p.u.

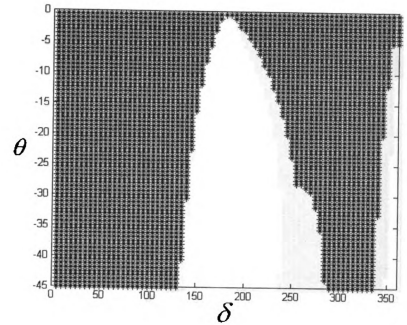
Figure 4.10: The ratio of total VA rating between the new and conventional UPFC configuration.

Thus, in Figure 4.9 and 4.10, calculation results of S_N / S_O at $-45^\circ \le \theta \le 0^\circ$ and $0.6^\circ \le \delta \le 359.4^\circ$ are shown. Figure 4.9 is the full view of the plot. Figure 4.10 shows operating areas where the VA rating can be greatly reduced with the proposed configuration. Normalized voltages, currents and impedance are used in all the calculations. The transmission line impedance, X, is fixed as 0.1 p.u.

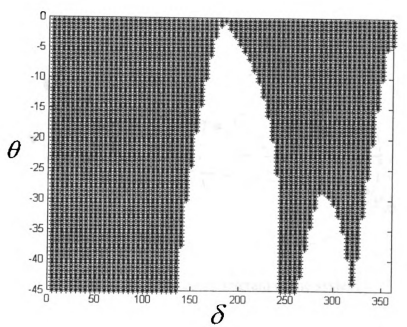
Figure 4.11 shows the $\theta - \delta$ plan projects of the points in Figure 4.9. The shaded areas in the plots are the areas in which the VA rating ratio, S_N / S_O, is smaller than 1 whereas the blank areas represent the areas with the VA rating ratio greater than 1. In all the figures, the shaded areas are much larger than the blank areas. And the major blank areas are all almost in near the center of each figure. Figure 4.9 to Figure 4.11 can be explained and further explored by the following illustrations:

Illustrations 1:where and why some points has VA rating ratio greater than 1

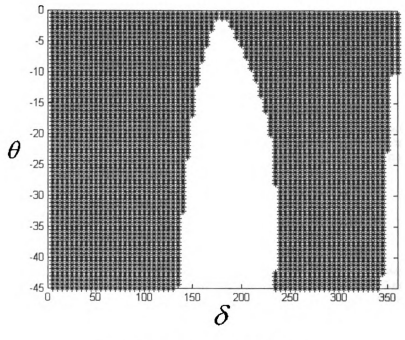
In the center area of Figure 4.11, as δ moves to the center (180°) from both directions, $\vec{V}_C$ begins to point towards the origin of $\vec{V}_{SO}$. This is shown as an example in Figure 4. 12. As a result, $\left|\vec{V}_{SO} - \vec{V}_C\right|$, the amplitude of the voltage of the Inverter 1 in the proposed configuration, becomes larger whereas the amplitude of the new sending end voltage, V_S, in both configurations, become smaller. When δ becomes 180°, they attain



(a) $V_C = 0.5$ p.u. and $I_q = 0$ p.u.



(b) $V_C = 0.5$ p.u. and $I_q = 0.25$ p.u.



(c) $V_C = 0.5$ p.u. and $I_q = -0.25$ p.u.

Figure 4.11: The $\theta - \delta$ projects of the Figure 4. 9.

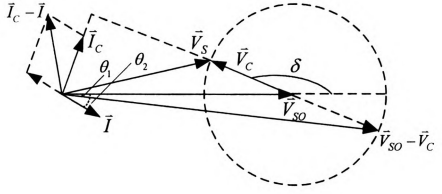


Figure 4.12: The vector diagram of the system.

their maximum and minimum respectively as shown in Figure 4.13. From equation (4. 1), and (4. 2), it is known, the transferred power is proportional to V_S, and affected by the angle difference between the sending end and receiving end voltage. One example of

transferred power and receiving end line current at the condition that $\theta = -45°$ and $0.6° \leq \delta \leq 359.4°$ are shown in Figure 4.14.

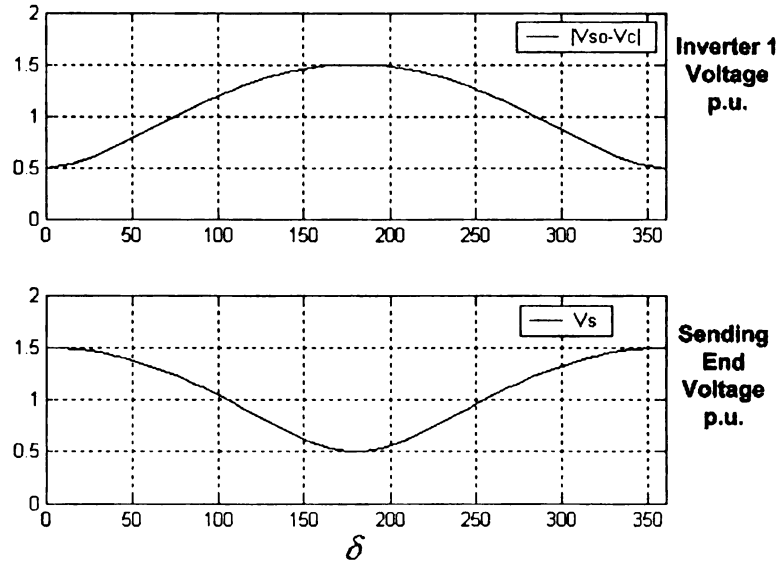


Figure 4.13: The relationship between inverter voltages and δ.

By comparing Figure 4.13 and Figure 4.14, it can be concluded that the areas that the VA rating ratio is greater than 1 in Figure 4. 11 (the blank areas) are also the areas in which the smallest power is transferred. And in this area, Inverter 1 in the new configuration will have a higher total voltage stress than in other areas, whereas the receiving end line current is smaller. Thus S_N / S_O becomes greater than 1 in the center blank area.

According to calculation results, the major reason for the blank area around 350° is the large amplitude of the Inverter 2 current at some compensation conditions. Furthermore, the purpose of a UPFC is to transmit more power without compromising stability. Therefore, the blank areas are normally not operating regions of the UPFC.

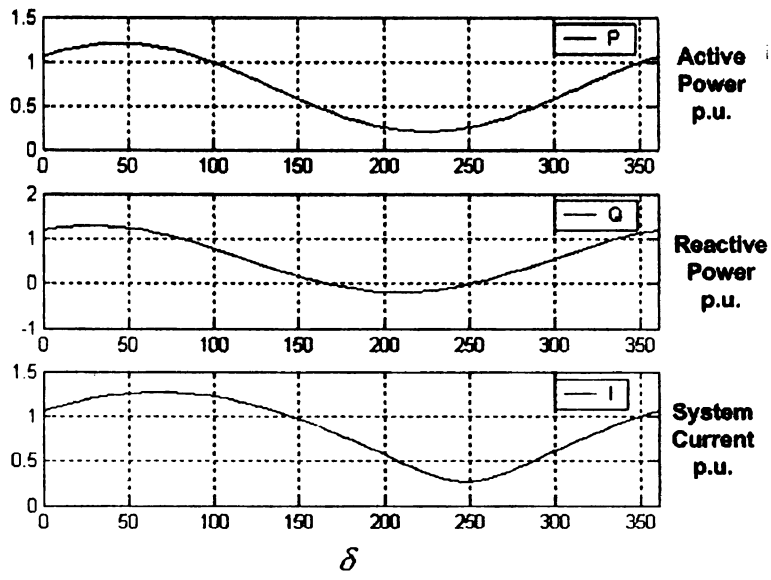
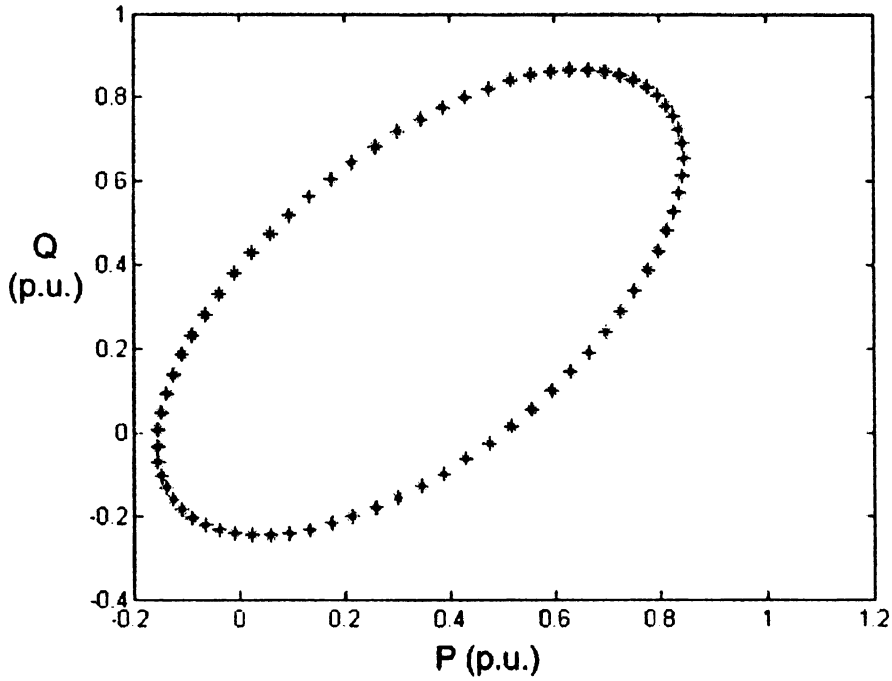


Figure 4.14: The active power, reactive power and receiving end line current when $\theta = 45°$ and δ changes from 0° to 360°.

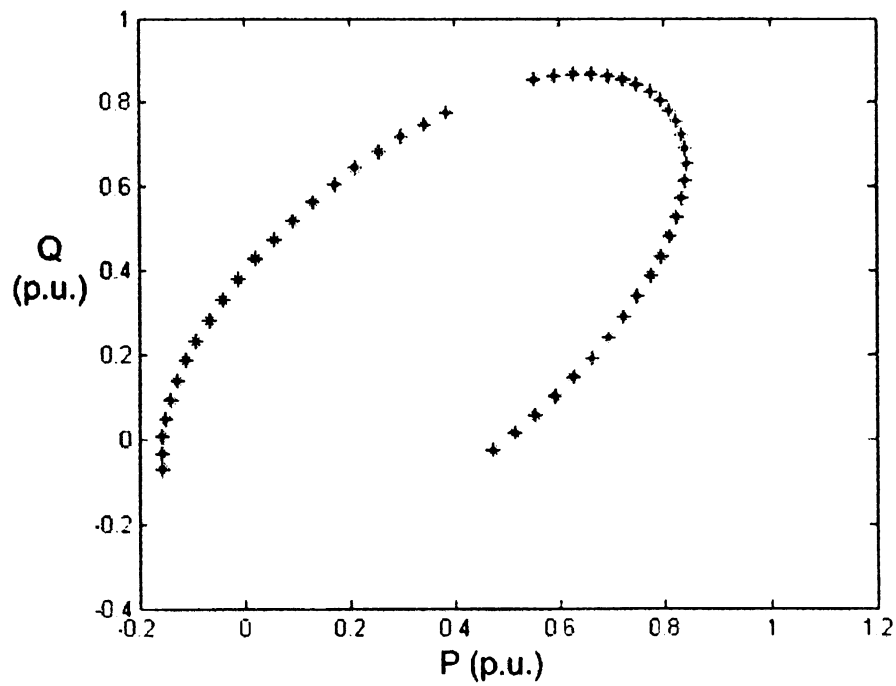
Illustrations 2: the total P-Q pairs covered by the shaded area

After Illustration 1, another remain question is whether the full function of the UPFC can be achieved within the shaded area in Figure 4.11. This question can be answered by the P-Q plot.

In the papers dealing with the UPFC, the P-Q plot is often used to show the function of the UPFC by showing the basic controllable pairs of active and reactive power (where $I_q = 0$) by plotting the reactive power, Q, versus active power, P. Figure 4.15 is an example of this.



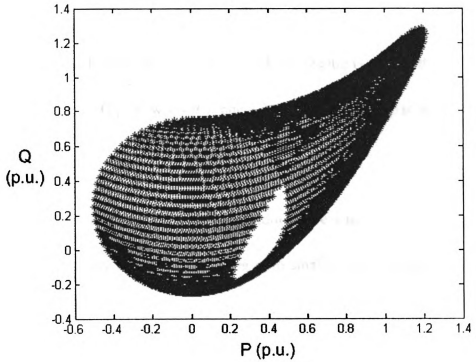
(a) all the P-Q pairs



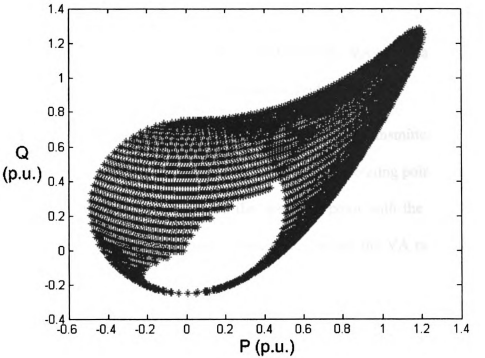
(b) P-Q pairs at which the VA rating ratio is smaller than 1

Figure 4.15: The P-Q pairs when $\theta = -25^\circ$, $V_C = 0.5$ p.u. and δ rotates from 0° to 360°.

Figure 4.15(a) shows all the basic P-Q pairs when $\theta = -25°$, $V_C = 0.5$ p.u. and δ rotates from 0° to 360°. Figure 4.15(b) shows only the basic pairs that have a VA rating ratio smaller than 1 at the same condition. Comparing Figure 4.15(a) and (b), some portion of the P-Q plot in Figure 4.15(a) is missing in Figure 4.15(b). So if all the P-Q plots at different θ are put into one figure, it will be easy to figure out the total missing P-Q pairs. Figure 4.16(a) shows the plots of all the basic P-Q pairs that the UPFC can achieve when θ changes from 0° to -45°. Figure 4.16(b) shows the plots of the basic P-Q pairs that have VA rating ratio less than 1 under this condition.



(a) all the P-Q pairs



(b) P-Q pairs at which the VA rating ratio is smaller than 1

Figure 4.16: The P-Q pairs when θ changes 0°to -45°, $V_C = 0.5$ p.u. and δ rotates from 0.6° to 359.4°.

The following conclusion can be drawn from Figure 4.16:

1) The operating area with VA rating ratio smaller than 1 (shaded areas in Figure 4.11(a)) covers almost all the basic P-Q pairs that the UPFC can achieve;

2) The pairs not covered are those that have both smallest active and reactive powers, which usually are not in the operating area of the UPFC;

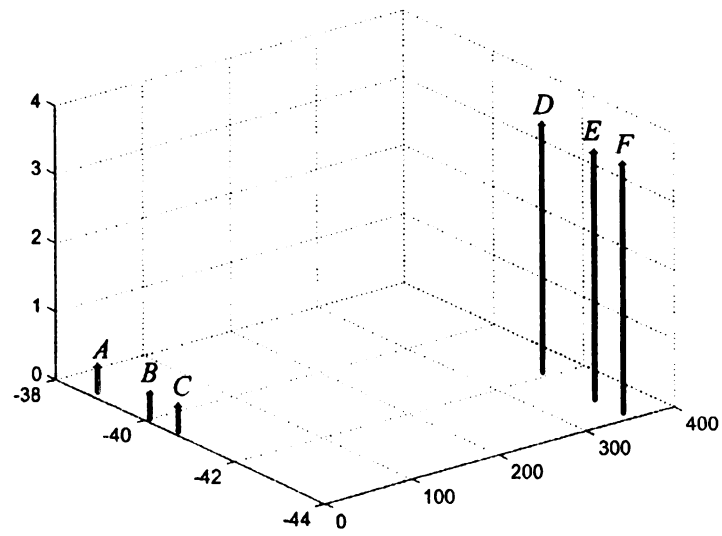
So it can be concluded that within the shaded area in Figure 4.11(a), the basic functions of the UPFC can be fully realized.

Illustrations 3: the VA rating optimization

Another interesting phenomenon that found from the VA rating analysis is that the VA rating of the system can be optimized in some load conditions.

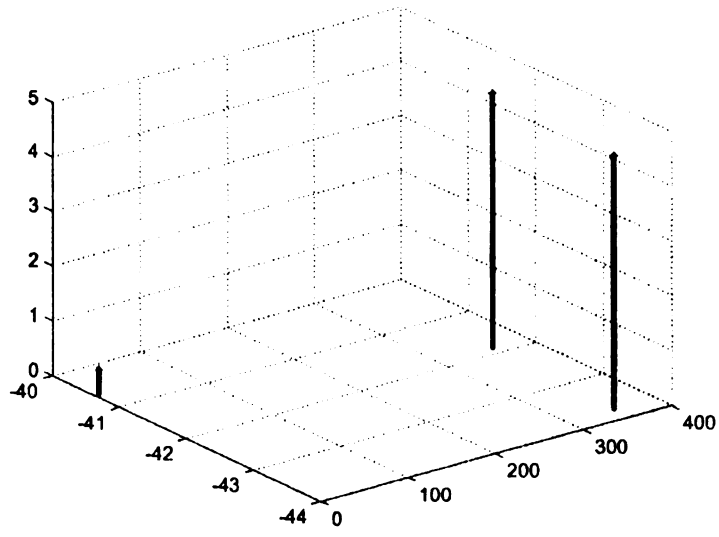
In Figure 4.9, different points may yield the same power transmitted. In other words, if a required active and reactive power is given, different operating points that transfer the same desired power can be found, and the operating point with the smallest total VA rating ratio can be chosen from these points, which means the VA rating of the system can be optimized.

Figure 4.17 shows the operating points that have the same power transfer but different VA rating ratios. The '*' points in Figure 4.17 are points extracted from Figure 4.9. At these points, the transferred active and reactive powers are almost the same. Thus the point that has the smallest VA ratio can be selected to minimize the UPFC' VA rating.



(a) V_C = 0.5 p.u. and I_q = 0 p.u.

0.99 p. u. < P <1.01 p.u. and 1.12 p. u. < Q <1.14 p.u.



(b) $V_C = 0.5$ p.u. and $I_q = 0.25$ p.u

0.99 p. u. $< P <$ 1.01p.u. and 0.83 p. u. $< Q <$ 0.85 p.u.

Figure 4.17: Operating points that have the same power but different VA rating ratio.

4. 7. Simulation Results

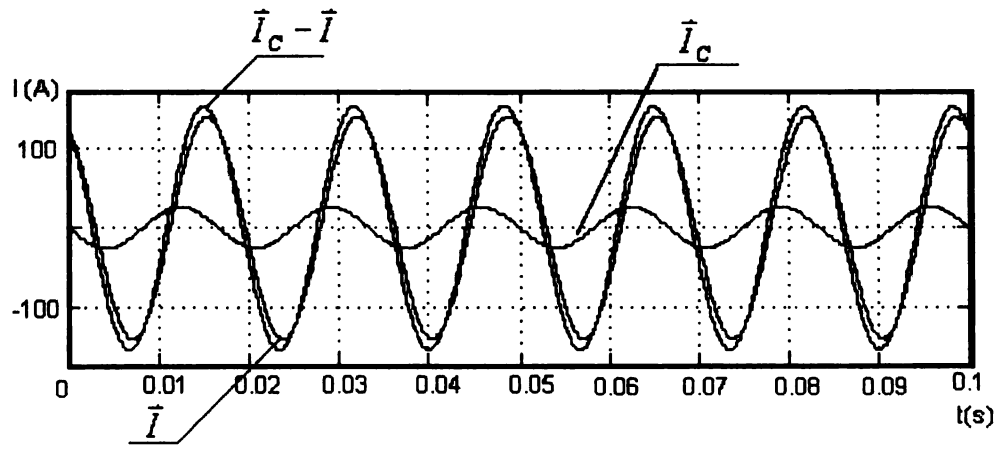
Simulations of the proposed and conventional configurations have been carried out. In the simulations, the system voltage is 1 pu constant. To make good verify of the analysis performed above, the transmission line impedance is fixed at 0.1 pu. Simulation results of the points in Figure 4.17(a) are summarized in Table 4.1. In Table 4.1, P and Q are the power transmitted with the UPFC; S_N/S_O is the ratio of the total VA rating between the new and conventional configuration.

Figure 4.18 shows the simulation waveforms of the proposed configuration at the operation point A ($\delta = 10^\circ$ and $\theta = -38.75^\circ$). $\vec{I}$ is the receiving end current; $\vec{I}_C$ is the Inverter 2 current; $\vec{I}_C - \vec{I}$ is the Inverter 1 current. In the simulation results, the Inverter

2 current is much smaller than the load current, $\vec{I}$, which is the reason that the total VA rating of the proposed configuration is much smaller than the VA rating of the conventional configuration. The simulation results agree with the analytical results obtained in the previous section and clearly show that the new UPFC is feasible and advantageous over the conventional UPFC in terms of required VA rating.

Table 4.1: Part of the simulation results of the new configuration

	A	B	C	D	E	F
δ (Deg.)	10	5	5	360	355	355
θ(Deg.)	-38.75	-40	-40.625	-41.875	-43.125	-43.75
P (p.u.)	1.002	0.996	1.009	1.001	0.992	1.004
Q(p.u)	1.125	1.127	1.138	1.133	1.123	1.134
S_N/S_O	0.42478	0.43604	0.43523	4.3776	4.3445	4.3488



$\delta = 10^\circ$, $V_C = 0.5$ p.u., $\theta = -38.75^\circ$, and $I_q = 0$

Figure 4.18: Currents through both inverts and the line in the new configuration.

4. 8. Summary

In this chapter, a new configuration of the UPFC has been proposed, which provides a feasible alternative to the conventional UPFC. The operation, analysis, and features of the new configuration were illustrated. Simulation results were shown to verify the operation and control principle.

It is shown that the functions of UPFC can be fully realized with optimized system VA rating. Thanks to the proposed face-to-face structure, the cascade multilevel inverters can finally be used in the UPFC application. As a result, the four major advantages of the new configuration of the UPFC, as stated at beginning of session 4.5, make the proposed circuit configuration very promising for new designs of UPFC.

This chapter proposed a cascade multilevel inverter solution for the most complicated FACTs device: UPFC. In the next chapter, another cascade multilevel inverter solution for the most widely used modern FACTs device – STATCOM will be proposed.

Chapter Five

DELTA-CONNECTED UNIVERSAL STATCOM

5. 1. Introduction

Power system compensation and conditioning has been a long existing problem. Compensation with power electronics devices first appeared in the later 1970s. At that time, thyristor controlled reactor or capacitor based Static VAR Compensator (SVC) were used in the power system to compensate reactive power. Since then, more than 1000 SVCs have been installed worldwide. In the last decade, the VSI based Static Synchronous Compensator (STATCOM) began to take over the place of the thyristor based SVCs. Compared with the traditional SVCs, the STATCOM has better dynamic response, larger compensation range and less dependence on the system voltage [43]. It mainly provides reactive power compensation, voltage regulation, harmonics compensation and system stability improvements.

By far, Static the STATCOM is the most widely installed modern FACTS device. Several STATCOMs with a power rating at the mega watt level have already been installed in real power systems [77-80, 86]. And with the urgent demand of system compensation in both transmission and distribution systems, the STATCOM now receives more and more research attention each year.

In this Chapter, a new delta-connected cascade multilevel inverter STATCOM is proposed. Unlike the conventional STATCOMs, the proposed STATCOM circuit not only can be used to compensate reactive power and harmonics, but also can be used to compensate negative sequence current caused by load imbalanced. Thus it is named as the Universal STATCOM (U-STATCOM).

5. 2. The Circuit Candidates of STATCOM

Multi-pulse inverters and multilevel inverters are the major circuits used in STATCOMs [77-80]. Full comparisons between these two circuits have already been performed [85]. The first generation STATCOMs were all built with multi-pulse inverter circuits.

In 1995, the cascade multilevel inverter was introduced to be an alternative circuit of the STATCOM [38]. Then lots of researches have been done towards the cascade multilevel inverter STATCOM. In year 2000, a 75 MVASTATCOM with cascade multilevel inverter structure has been installed in the power systems in U. K [86, 87]. Compared with the multi-pulse inverter STATCOMs, no zigzag transformer is needed in the cascade multi-level inverter STATCOM. The cost, volume and power loss are

greatly reduced. The control also becomes quite simplified. Since year 1995, the cascade multilevel inverter has become the trend in the application of STATCOM.

Recently, most researches have been focused on the STATCOM with three-phase wye-connected cascade multilevel inverter. Figure 4.1 shows its system configuration. The three-phase wye-connected cascade multilevel inverter is connected to the utility line through the inductor $L_{a,b,c}$. The cascade inverter's output voltage $v^c_{a,b,c}$ is controlled to be fundamentally in phase with the system voltage $v_{as,bs,cs}$. Then the reactive power produced or absorbed by the STATCOM is decided by the following equation:

$$Q = \frac{V^c_a - V_{as}}{X_L} V_{as}, \tag{5. 1}$$

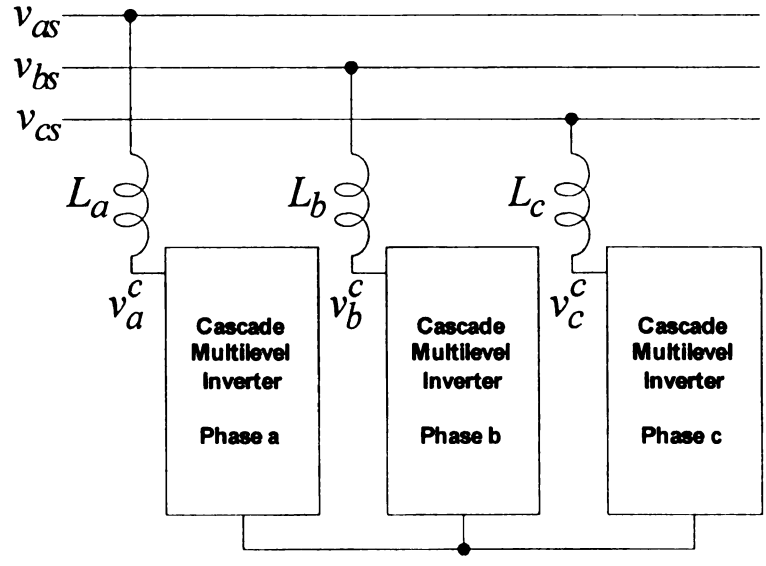


Figure 5.1: The system configuration of wye connected STATCOM.

where X_L is the impedance of the inductor $L_{a,b,c}$. Ideally, there will be no real power exchange between the inverter and the utility line. The DC capacitors in the inverter will sustain the desired voltage.

However, in most cases, the power system will have an unbalance load. At unbalanced conditions, the wye connected cascade multilevel inverter still can be used to compensate reactive power. But it cannot be used to correct the imbalance of the system currents. To explain this, one simple example is shown in Figure 5.2.

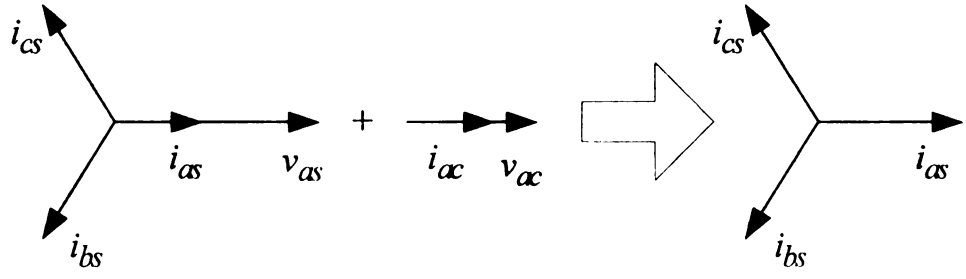


Figure 5.2: The imbalance compensation with wye structure.

To compensate the imbalance current shown in Figure 5.2, the STATCOM with wye structure would be controlled to output a compensation current, i_{ac}, which is in phase with the inverter output voltage, v_{ac}. Thus, there must be real power exchange between the inverter and the utility line. And the real power exchanges will overcharge or discharge the DC capacitors in the inverter. This is against the basic operating principle of the STATCOM.

For general imbalance compensation with wye structure, if there was imbalance in the active component of the line current, there would be active power exchange between the inverter and utility line.

To overcome this problem, this paper proposes a U-STATCOM with a delta-connected cascade multilevel inverter.

5. 3. The Proposed U-STATCOM

5. 3. 1. Proposed U-STATCOM

Figure 5.3 shows the U-STATCOM circuit structure and one line-line voltage waveform. Each phase leg of the STATCOM will have several full bridge inverter modules and one output inductor. The inverter module can be either a two-level H-bridge or three-level H-bridge depending on application requirement. The three phase legs of the inverter are connected to each other head to tail by the output inductor, L. Then the whole cascade multilevel inverter becomes delta-connected to the utility lines.

To illustrate the function of the U-STATCOM, the fundamental compensation theory will first be introduced.

5. 3. 2. The compensation theory [91]

With balanced three-phase voltage, an ungrounded three-phase load can always be represented by a delta-connected network as shown in Figure 5.4(a) [91]. The load

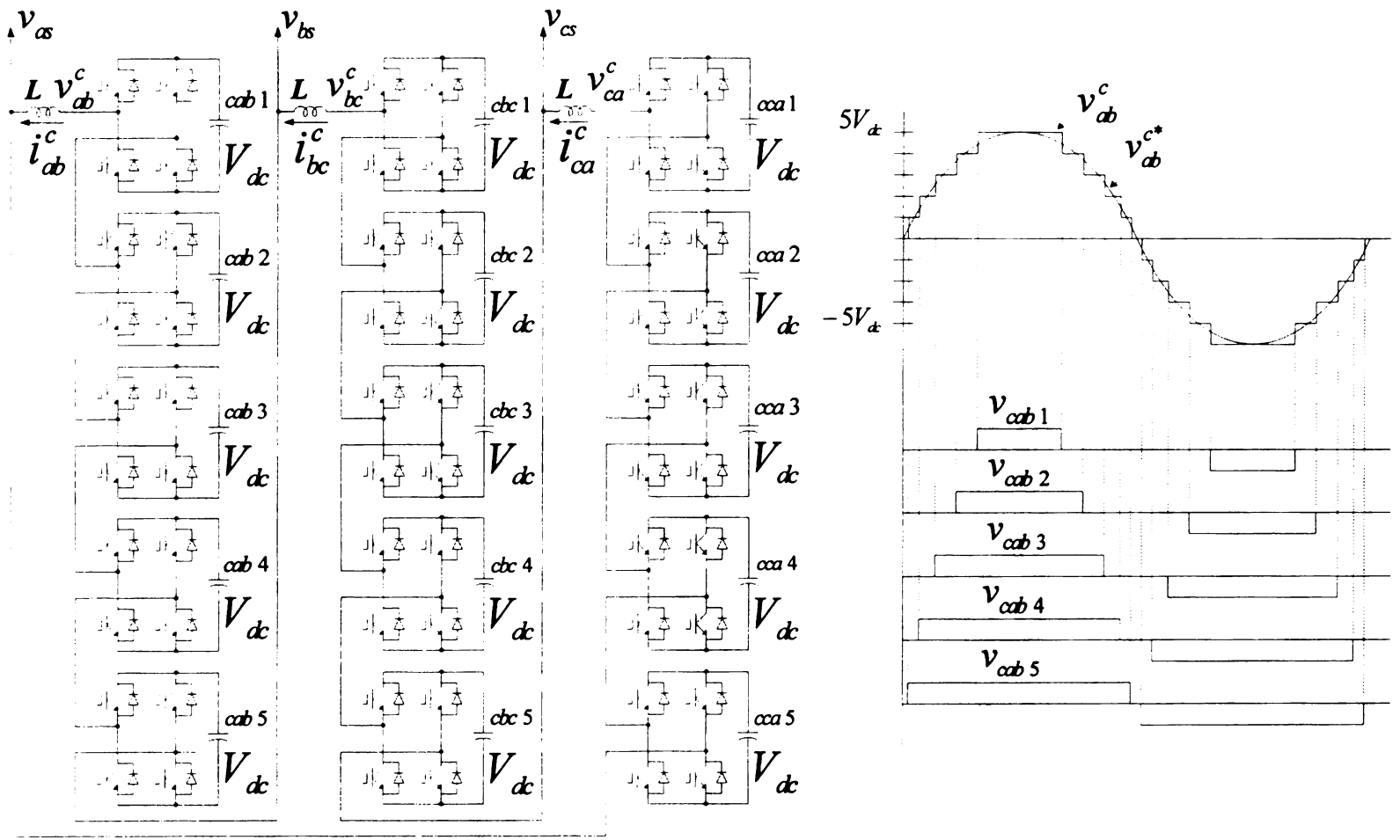


Figure 5. 3: The U-STATCOM structure and one phase voltage waveform.

admittances $Y^l_{ab} = G^l_{ab} + jB^l_{ab}$, $Y^l_{bc} = G^l_{bc} + jB^l_{bc}$ and $Y^l_{ca} = G^l_{ca} + jB^l_{ca}$ can be complex and unequal. It has been proven that just one delta-connected pure reactive network is needed to fully compensate the reactive power and system unbalance as shown in Figure 5. 4(b). The pure reactive compensation network is defined by:

$$\begin{cases} Y^r_{ab} = jB^r_{ab} = j(-B^l_{ab} + (G^l_{ca} - G^l_{bc})/\sqrt{3}) \\ Y^r_{bc} = jB^r_{bc} = j(-B^l_{bc} + (G^l_{ab} - G^l_{ca})/\sqrt{3}) \\ Y^r_{ca} = jB^r_{ca} = j(-B^l_{ca} + (G^l_{bc} - G^l_{ab})/\sqrt{3}) \end{cases} . \qquad (5.2)$$

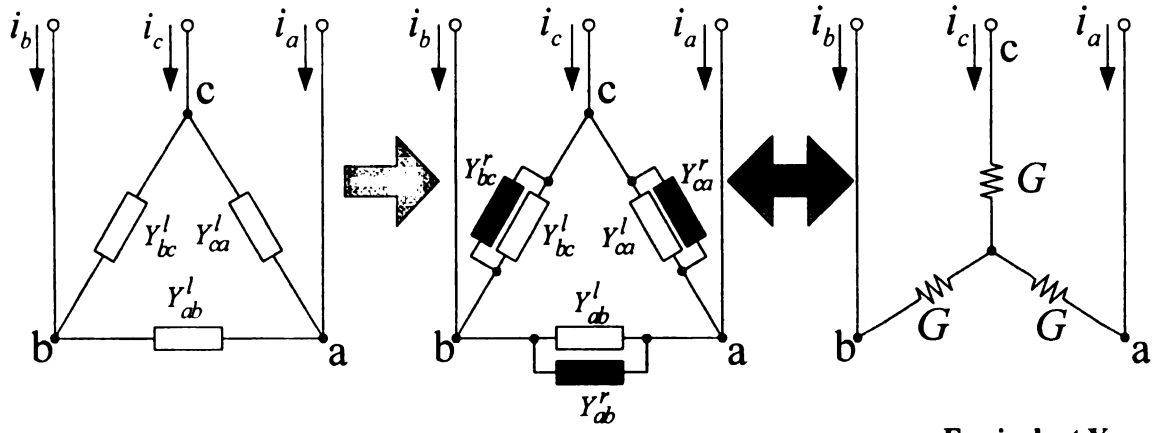


Figure 5.4: The general three-phase compensationnetwork.

After compensation, the equivalent wye-connected system is totally resistive and balanced as shown in Figure 5.4(c). The equivalent phase admittance, G, is equal to $G^l_{ab} + G^l_{bc} + G^l_{ca}$.

To realize the active compensation based on this compensation theory, the admittance $Y^r_{ab,bc,ca}$ can be substituted by the U-STATCOM shown in Figure 5.3. The only criteria for this substitution is that the cascade inverter output voltage, $v^c_{ab,bc,ca}$, should be controlled to keep the current on the inductor L (seen in Figure 4.3) equal to the current on $Y^r_{ab,bc,ca}$. This guarantees the following two things:

1) full compensation of reactive power and load imbalance;

2) no real power flows through the inverter.

5. 4. Control Scheme and Reference Current Detection

A. System Control Scheme

To realize compensation for both the reactive power and load current imbalance, ideally the inverter output voltages, $v^c_{ab,bc,ca}$, should be controlled to be in phase with the utility line-line voltages, $v_{ab,bc,ca}$. The current output of the inverter, $i^c_{ab,bc,ca}$, should always be 90° lagging or leading the inverter voltage to produce or absorb the needed reactive power. However, the inverter will always consume a small amount of active power because of the power losses on the switches and capacitors. So in the real control, the inverter control reference, $v^c_{ab,bc,ca}$, will have a very small lag angle difference, $\alpha_{ab,bc,ca} << 0.6^\circ$ [36], from the utility line-line voltages. By introducing this small lagging angle to the voltage command, the resulted output voltage of STATCOM

will have a phase difference from the grid voltage. Thus, real power will flow into the STATCOM to charge the DC capacitor..

Figure 5.5 shows the control diagram of reactive power and load current imbalance compensation. The total control is a combination of the output voltage control and the DC voltage control.

In the output voltage control loop, a reference current, $I^{*}_{ab,bc,ca}$, is first calculated based on the sensed load currents and system voltages. This reference current will guarantee both the reactive power and load current imbalance and compensation. Then the amplitude of inverter output voltage, $V^{c*}_{ab,bc,ca}$, is calculated based on the current reference.

For var and harmonics compensation, the method to keep the capacitors in different inverter modules equally charged or discharged has been discussed in Chapter 3. By properly rotating the voltage levels produced by each module, the DC voltages on each capacitor will always be kept same. So for the DC voltage control, it is only necessary to sense one capacitor voltage per phase. The sensed voltage is compared with a reference voltage, V^{*}_{dc}. Then a PI controller is employed to calculate a small lagging angles, $\alpha_{ab,bc,ca}$.

The final voltage command of the inverter, $v^{c*}_{ab,bc,ca}$, is synthesized from $V^{c*}_{ab,bc,ca}$, $\alpha_{ab,bc,ca}$ and the system line-line voltage phase angles, $\theta_{ab,bc,ca}$, which are obtained from phase lock loops.

B. Reference Current Detection Method

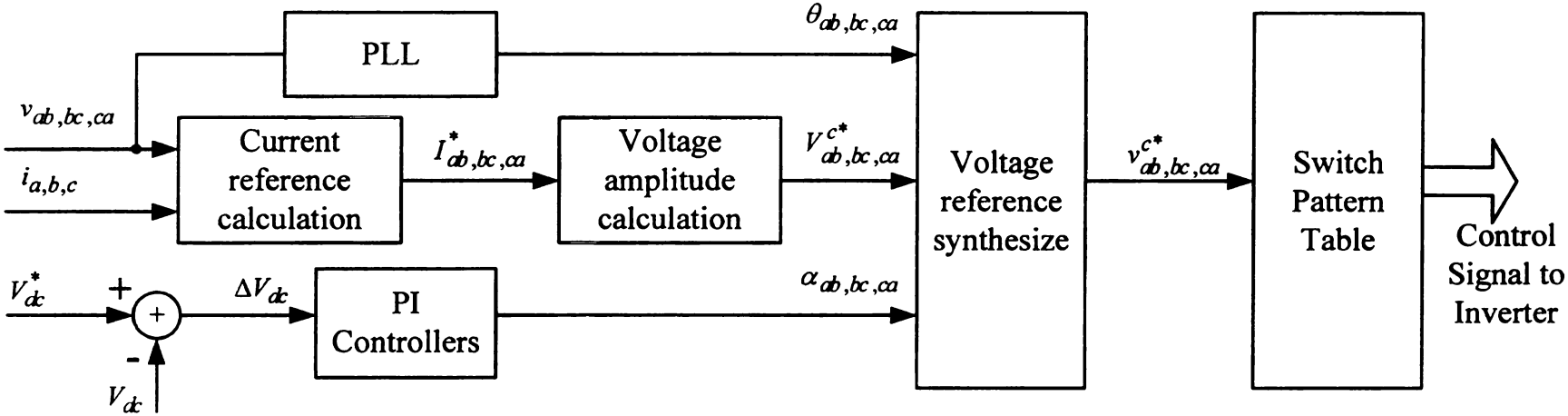


Figure 5.5: Control diagram.

From the Figure 5.5, it can be seen that, the whole control strategy is built based on the correct detection of the reference current amplitude, $I^{*}_{ab,bc,ca}$. To calculate the $I^{*}_{ab,bc,ca}$, the most direct method is to figure out the compensating susceptances, $B^{r}_{ab,bc,ca}$, and the input voltage's amplitude, V.

There are several methods to get the value of compensating susceptances, $B^{r}_{ab,bc,ca}$. The conventional way is to express the susceptances in terms of instantaneous currents and voltages [91].

It is proved that $B^{r}_{ab,bc,ca}$ can be calculated by

$$\begin{cases} B^{r}_{ab} = -\dfrac{1}{3V}\left[\mathrm{Im}(I_a) + \mathrm{Im}(I_b) - \mathrm{Im}(I_c)\right] \\ B^{r}_{bc} = -\dfrac{1}{3V}\left[\mathrm{Im}(I_b) + \mathrm{Im}(I_c) - \mathrm{Im}(I_a)\right] \\ B^{r}_{ca} = -\dfrac{1}{3V}\left[\mathrm{Im}(I_c) + \mathrm{Im}(I_a) - \mathrm{Im}(I_b)\right] \end{cases}, \tag{5.3}$$

where $\mathrm{Im}(I_{a,b,c})$ are the imaginary parts of the phasors of the load current. Because $\sqrt{2}\,\mathrm{Im}\,I_{a,b,c}$ is the maximum value of reactive current, which appears when the phase voltage is zero, so there is

$$\mathrm{Im}(I_{a,b,c}) = \left.\frac{i_{a,b,c}(t)}{\sqrt{2}}\right|_{\substack{v_{a,b,c}(t)=0 \\ dv_{a,b,c}(t)/dt>0}}. \tag{5.4}$$

The zero crossing of the voltages, current amplitude at that time and the voltage amplitude, V, can be detected with sensors. By substituting equation (5. 4) into equation (5. 3), $B^r_{ab,bc,ca}$ is then expressed in the terms of the instantaneous currents and voltages as the following

$$\begin{cases} B^r_{ab} = -\dfrac{1}{3\sqrt{2}V}\left[i_a(t)\Big|_{\substack{v_a(t)=0 \\ dv_a(t)/dt>0}} + i_b(t)\Big|_{\substack{v_b(t)=0 \\ dvb(t)/dt>0}} - i_c(t)\Big|_{\substack{v_c(t)=0 \\ dv_c(t)/dt>0}} \right] \\ B^r_{bc} = -\dfrac{1}{3\sqrt{2}V}\left[i_b(t)\Big|_{\substack{v_b(t)=0 \\ dv_b(t)/dt>0}} + i_c(t)\Big|_{\substack{v_c(t)=0 \\ dv_c(t)/dt>0}} - i_a(t)\Big|_{\substack{v_a(t)=0 \\ dv_a(t)/dt>0}} \right] \\ B^r_{ca} = -\dfrac{1}{3\sqrt{2}V}\left[i_c(t)\Big|_{\substack{v_c(t)=0 \\ dv_c(t)/dt>0}} + i_a(t)\Big|_{\substack{v_a(t)=0 \\ dv_a(t)/dt>0}} - i_b(t)\Big|_{\substack{v_b(t)=0 \\ dv_b(t)/dt>0}} \right] \end{cases} . \qquad (5.5)$$

After the V and $B^r_{ab,bc,ca}$ are known, the reference current $I^*_{ab,bc,ca}$ can be found out with ease.

5. 4. Simulation Results

The major functional difference between the U-STATCOM and conventional STATCOM is the compensation of load current imbalance. Simulation of the compensation of unbalanced load current with U-STATCOM as shown in Figure 5.3 is presented.

In the simulation, the system line-line voltage is 60 Hz, 13 kV. The unbalanced load is described by $Y^l_{ab} = Y^l_{bc} = 0.02$ S and $Y^l_{ca} = 0$ S. In this case, the compensation susceptances are

$$\begin{cases} B^r_{ab} = -\dfrac{1}{50\sqrt{3}} \\ B^r_{bc} = \dfrac{1}{50\sqrt{3}} \\ B^r_{ca} = 0 \end{cases} . \tag{5.6}$$

The amplitudes of the reference currents are $I^*_{ab} = I^*_{bc}\dfrac{V_{ab}}{50\sqrt{3}}$, and $I^*_{ca} = 0$. The phase angles of the references are $-90°$, $-30°$ and $0°$ respectively.

Figure 5.6 shows the uncompensated three-phase current. Figure 5.7 shows the compensated three-phase system currents, inverter voltages and currents.

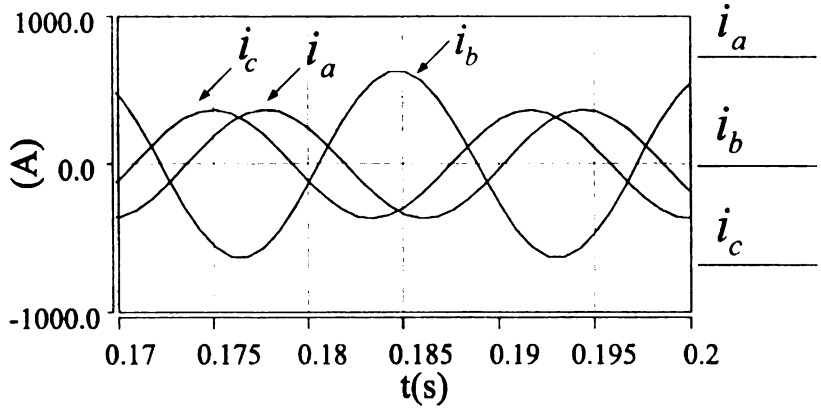


Figure 5.6: The uncompensated system current.

It can be seen that, after compensation, the system three-phase current becomes balanced. The goal of compensation is achieved. There is almost a 90°'s difference

between the inverter fundamental voltages and currents, which means there is almost no real power flow between the inverter and the system. There are third harmonic components present in the inverter currents. This is because the staircase inverter voltage is optimized to minimize the 5^{th}, 7^{th}, and 11^{th} harmonics. The 3^{rd} harmonic does not affect the total compensation result. The simulation result verifies the circuit structure and control scheme of the U-STATCOM.

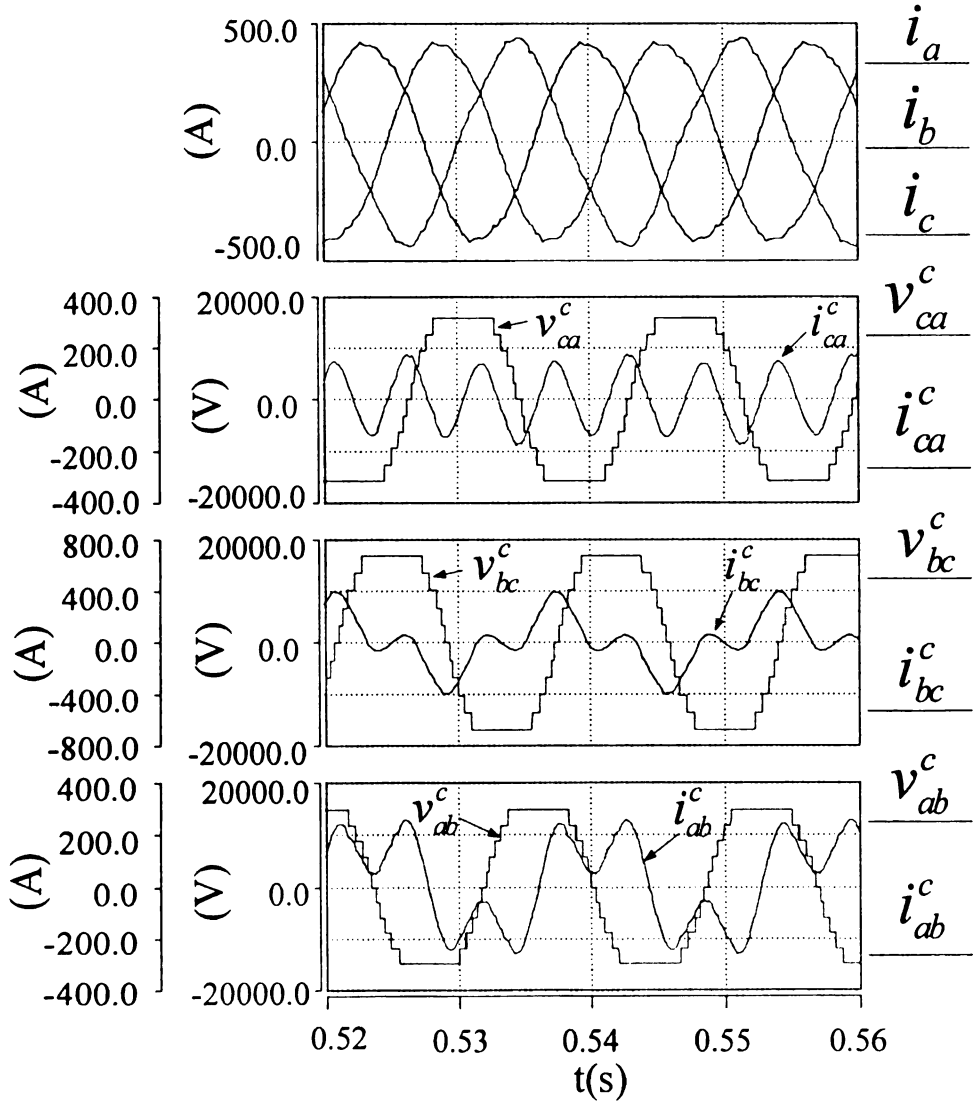


Figure 5.7: The compensated system current and inverter voltages and currents.

5. 5. Summary

STATCOM is the most popular modern FACTs device. Researches have shown that cascade multilevel inverter is the best circuit choice for the next generation of STATCOM. A 75 MVA STATCOM based on cascade multilevel inverter has been built and installed in the year 2000. However, till now, the cascade multilevel inverter based STATCOMs all utilize three phase wye-connection. With wye-connection, in terms of compensation varieties, only limited compensation can be realized.

In this chapter, the U-STATCOM was proposed to realize universal compensation of the power system. Other than reactive power and harmonics, the proposed U-STATCOM can also compensate the negative sequence current caused by unbalanced loads. The circuit structure and the basic compensation theory were introduced. The control strategy and compensation component detection method were shown. Simulation results of load current imbalance compensation with proposed U-STATCOM was presented.

Chapter 4 and 5 proposed applications of cascade multilevel inverters in FACTs devices for the transmission systems. In the next chapter, extended applications of cascade multilevel inverter in the distribution systems will be introduced.

Chapter Six

EXTENDED APPLICATIONS OF MULTILEVEL INVERTERS

6. 1. Introduction

Chapter 4 and 5 mainly deal with the applications of multilevel inverters in transmission systems. While in this chapter, extended applications of multilevel inverters in other levels of power systems are presented. For Custom Power, one DVR circuit with an uneven cascade multilevel structure is proposed. For DG, the DC voltage regulator for cascade multilevel inverters is fully discussed.

6. 2. DVR Circuits

Among all the power quality problems, voltage sag is the number one cause of equipment failure and other economic damages in the distribution system. Thus, the

Dynamic Voltage Restorer (DVR) has become the most researched Custom Power device. In the early papers of the DVR [116-119], the theory and operating principle of the DVR is well described. The design of circuit parameters were summarized [120]. Field experiences of the DVR have been often reported [117, 122, 124]. Cascade multilevel inverter was first proposed as a circuit topology for the DVR by Peng's paper [36, 37]. The utilization of the cascade multilevel inverter eliminates the line frequency transformer in the old circuits, thus reduces the cost and volume. In 2003, a cascade multilevel inverter DVR was built and reported [115]. But widespread application of the cascade multilevel inverter in the DVR is also constrained by the need of separated DC sources.

As shown in Figure 2.9, the most common DVR circuit topology is one VSI connected in series with the grid through a line transformer. The DC bank of the VSI can be either powered from the grid through a rectifier or a backup DC source such as battery packs and fuel cells. The line transformer in the DVR system is the efficiency killer. It also makes the system bulky and expansive. That is the reason that the cascade multilevel inverter was introduced. Figure 6.1 shows the one structure of DVR that utilizes the cascade multilevel inverter.

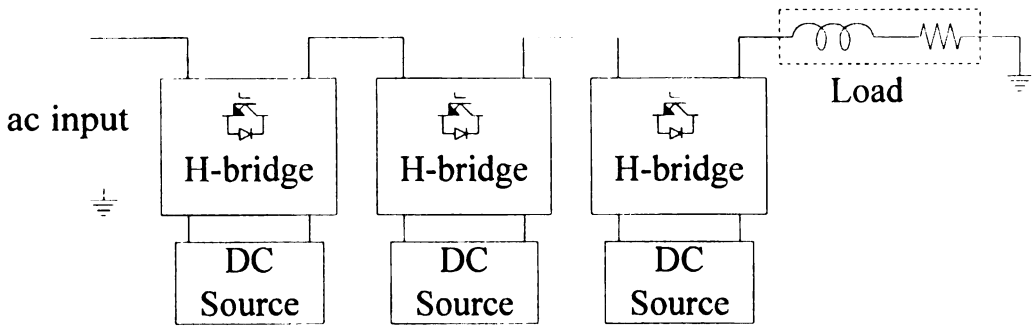


Figure 6.1: The cascade multilevel inverter based DVR.

The transformer is no longer needed in this structure. But the separated dc bank either need isolated DC regulator or multiple separated DC source to supply the power. The need of separated DC sources really becomes a bottleneck of the application of the cascade multilevel inverter in the DVR.

6. 3. Proposed DVR Circuit.

The proposed DVR circuit is shown in Figure 6.2. Inverter 1 is a bulky power inverter. Voltage compensation is realized solely by Inverter 1. Inverter 2 is a smaller sized inverter whose dc bus voltage is only 1/3 Inverter 1. The major job of inverter 2 is to compensate the harmonics produced by Inverter 1. Thus, Inverter 2 can also be called as a conditioning inverter.

6. 3. 1. The Theory of Two Non-identical Inverter in Cascade

In the proposed circuit, two inverters with different dc bus voltages are cascade connected. Similar circuit topology for an open winging motor has been proposed in one of author's paper [31]. The difference is that in the paper [31], two three level diode clamped inverters are cascaded. Since the H-bridge inverter also has three-level output, the mathematic essences behind the two circuits are exactly the same.

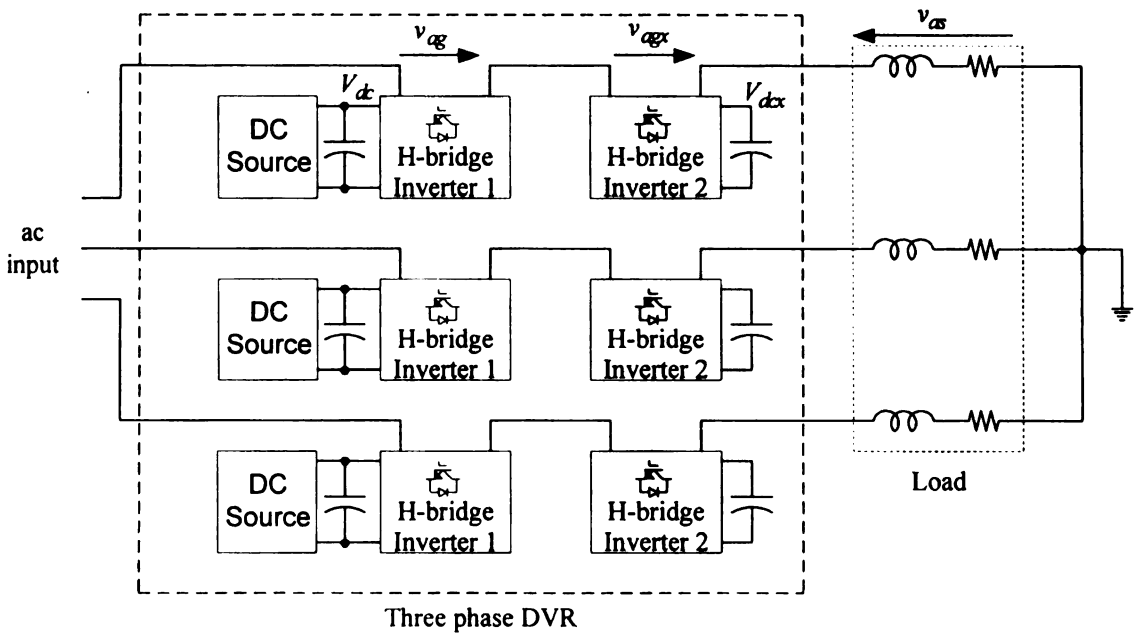


Figure 6.2: The proposed DVR system.

The output voltages of the Inverter 1 and Inverter 2 may be expressed as:

$$\begin{bmatrix} v_{ag} & v_{bg} & v_{cg} \end{bmatrix}^{\mathrm{T}} = \begin{bmatrix} s_a & s_b & s_c \end{bmatrix}^{\mathrm{T}} V_{dc} \tag{6.1}$$

and

$$\begin{bmatrix} v_{agx} & v_{bgx} & v_{cgx} \end{bmatrix}^{\mathrm{T}} = \begin{bmatrix} s_{ax} & s_{bx} & s_{cx} \end{bmatrix}^{\mathrm{T}} V_{dcx}, \tag{6.2}$$

where s_a, s_b, and s_c are the switching states for the Inverter 1 and s_{ax}, s_{bx}, and s_{cx} are the switching states for the Inverte 2. For three-level inverters, the switching states correspond to the output voltage levels and can have the values of 0, 1, or -1. When just considering the effects of the two inverters on the load, the load phase voltages can be expressed in terms of the v_{ag} and v_{agx} as

$$\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} = \begin{bmatrix} v_{ag} + v_{agx} \\ v_{bg} + v_{bgx} \\ v_{cg} + v_{cgx} \end{bmatrix}. \tag{6. 3}$$

The effective line-to-line load voltages may be expressed in terms of the phase voltages as

$$\begin{bmatrix} v_{abs} \\ v_{bcs} \\ v_{cas} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix}. \tag{6. 4}$$

Since in the proposed circuit structure, the DC bank voltages are no longer identical, the numbers of output voltage levels in phase and line-line voltage no longer follow the general rules. At this condition, it is necessary to look at the voltage vector plot of the proposed circuit structure to analysis the voltage levels in the output voltages. The voltage vector plot is formed by plotting the space vector of phase voltages in the *d-q* stationary reference frame for all possible combinations of switching states. In the case as shown in Figure 6.2, vector plots vary widely depending on the ratio of the DC voltages. Figure 6.3 shows the voltage vector plots of the proposed cascade inverter for several DC voltage ratios, whereas Figure 6.4 shows the maximal distention. Therein, the axes of each subplot of Figure 6.3 are the same as those shown in Figure 6. 4.

As shown in Figure 6.3, when the voltage ratio is set to $V_{dcx} = \frac{V_{dc}}{6}$, the vector plot appears as several three-level vector plots arranged in a three-level pattern. If the voltage ratio is increased further to $V_{dcx} = V_{dc}/2$ and $V_{dcx} = V_{dc}$, the cascade-3/3 inverter can operate as a seven-level and five-level inverter respectively. However, these modes of

operation are not as desirable as that of maximal distention, which yields the highest power quality.

In general, the voltage rating which yields maximal distention for an arbitrary number of voltage levels is

$$\frac{V_{dcx}}{V_{dc}} = \frac{n_x - 1}{n\, n_x - n_x}, \tag{6. 5}$$

where n and n_x are the voltage levels of the upper and lower inverter respectively. For the connection of two 3 level inverters, the maximal distention is achieved when $V_{dcx} = \frac{V_{dc}}{3}$. At this condition, the vector plot is the same as that of a nine-level inverter. Thus, the proposed DVR is capable of emulating. a maximum of nine voltage levels.

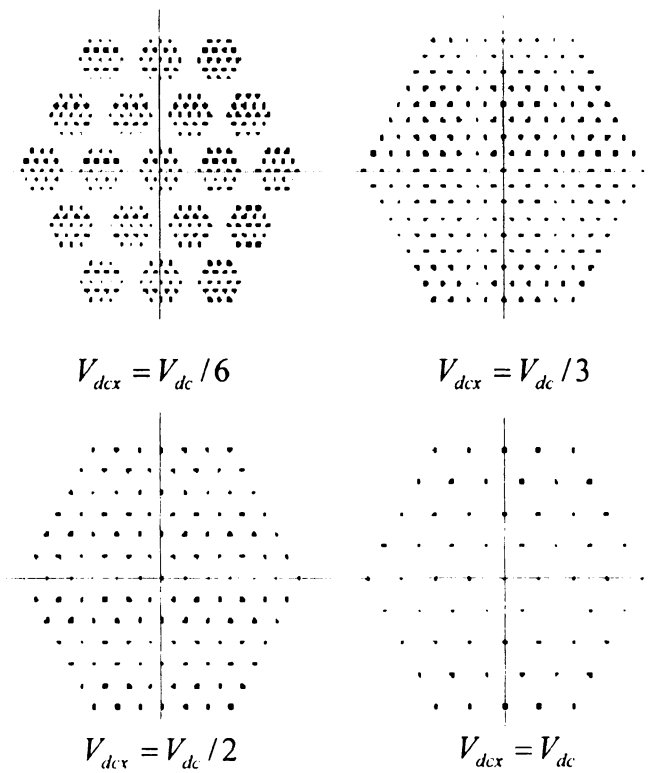


Figure 6.3: Cascade 3/3 vector plots.

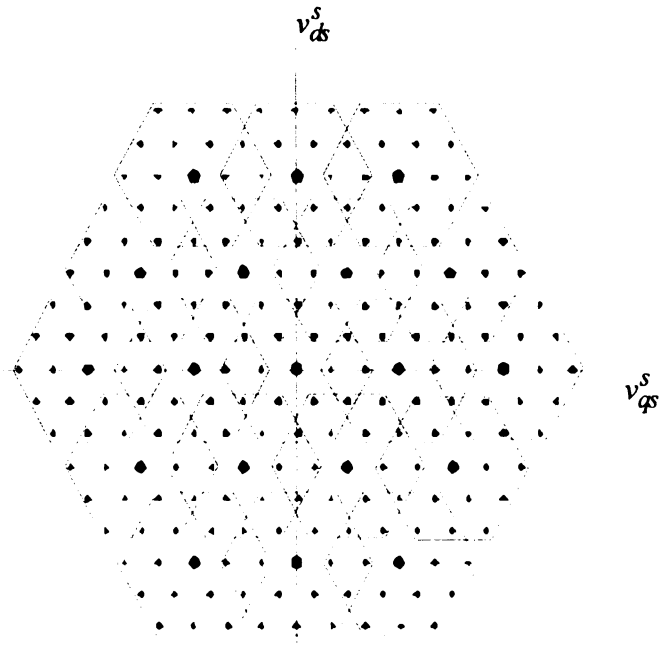


Figure 6.4: The vector plots of maximal distention.

6. 3. 2 Control of Proposed DVR System

There are two ways to control the two inverters. One is joint control, which utilizes multiple Sinusoidal Pulse Width Modulation (SPWM); another is separated control. Compared with joint control, separated control makes the system more robust and flexible [31]. In this chapter, only separated control will be introduced.

The separate inverter control utilizes isolated algorithms for the bulky power Inverter 1 and the smaller conditioning Inverter 2. The Inverter 1 is controlled by the staircase, or low switching frequency PWM method to provide the voltage needed to compensate for the voltage sag, whereas the Inverter 2 utilizes high-frequency PWM to shape the compensation voltage and current and achieve high power quality. It should be noted that, as with the separate-inverter control, Inverter 2 only perform harmonics elimination

and does not consume real power, thus does not need a dc power supply to support its DC bank..

The staircase control of the bulky Inverter 1 is shown in Figure 6.5. By controlling the switching angle, α, the fundamental of the staircase waveform can be controlled.

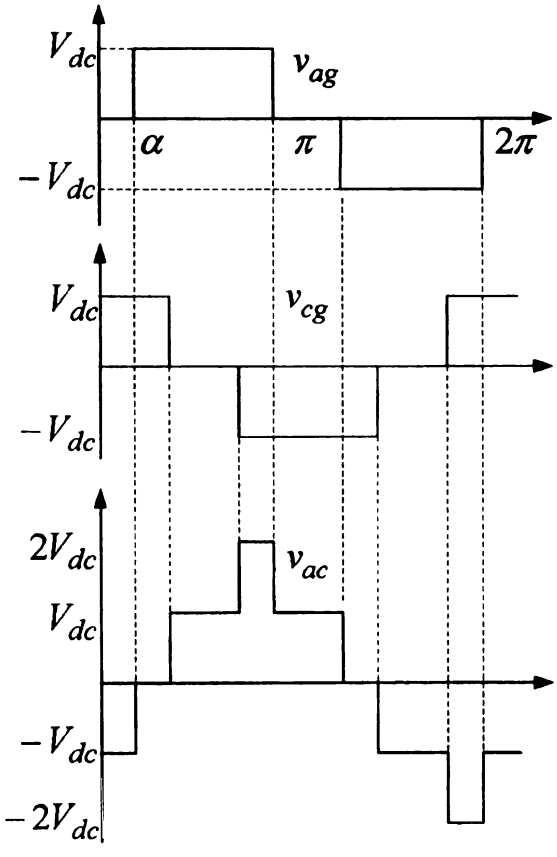


Figure 6.5: The staircase control of the bulk inverter (Inverter 1).

The control reference for the Inverter 2 is the harmonics content in the output voltage of Inverter 1. The total harmonic content of the phase voltage can be expressed as

$$v_{ag,h} = v_{ag} - v_{ag,f}, \tag{6.6}$$

where $v_{ag,f}$ is the fundamental component of v_{ag}. The fundamental component, $v_{ag,f}$

can be obtained simply through a low pass filter. However, it should be noted that a three-phase vector PLL circuit based on the line-to-line voltages gives better performance because the three-phase line-to-line voltages contain no triplens and their lowest harmonic is the 5th. Once the phase angle information is obtained by the PLL circuit, the synchronous frame method can be used to extract the fundamental component. After $v_{ag,f}$ is found, the control reference for the conditioning Inverter 2 is also found.

Another consideration of the separate inverter control is the DC voltage control of the conditioning inverter. In order to maintain maximal distention, the DC capacitor voltage on the conditioning inverter should be kept at one third of the DC voltage of the bulk inverter. To achieve this, a straightforward PI control is adopted to regulate active power flow into the conditioning inverter. The control scheme of the conditioning inverter is shown in Figure 6.6 for the *a*-phase.

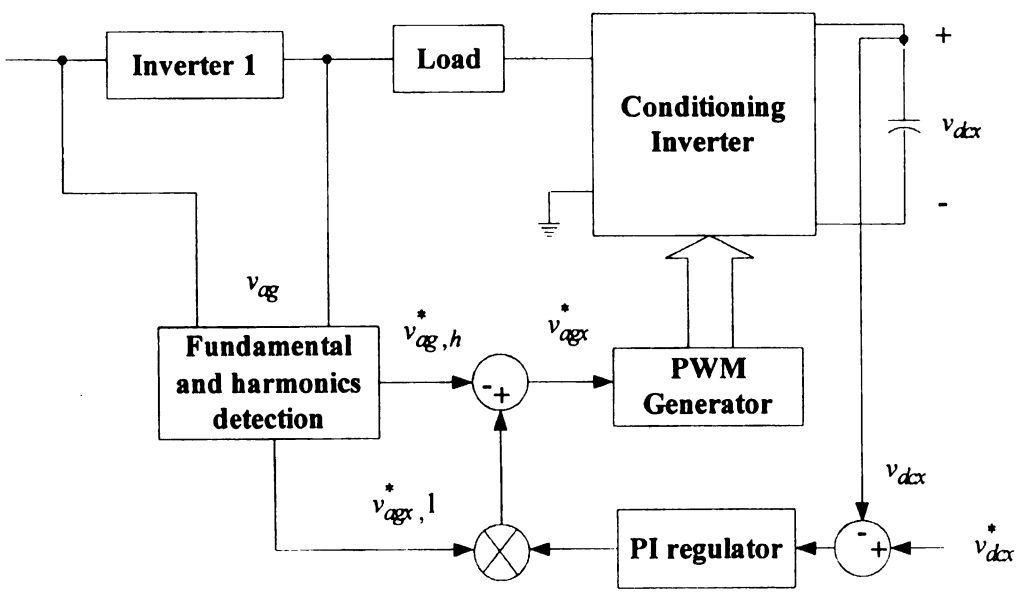


Figure 6.6: Conditioning inverter control diagram.

Therein, v_{dcx}^{*} is the DC voltage reference, which is set to one third of V_{dc}. The voltage $v_{ag,1}^{*}$ is a unit sine wave in phase with the phase voltage $v_{ag,f}$ and can be directly obtained from the vector PLL circuit . The resulting reference voltage is used as an input for the PWM modulator of the conditioning inverter. Similar control channels are used for the *b*- and *c*-phase.

Figure 6.7 shows simulation results of the cascade multi-level inverter using the separate control, in which a) is the DC voltage of the conditioning inverter; b) is the load current; c) is the total load line-line voltage; d) is the bulk inverter line-line voltage; e) is the conditioning inverter line-line voltage; and f) is the harmonics in the line-line voltage of the bulk inverter. In simulation, V_{dc} was set to 600 V, and α was set to 15°. It can be seen that the DC link voltage of the conditioning inverter is kept at one third of the dc voltage of the bulk inverter. The total line-to-line voltage is improved from the bulk inverter five-level waveform by the conditioning inverter and the maximal distention of the cascaded inverter is realized. The proposed circuit structure and control strategy are proved.

The cascade multilevel inverter with uneven DC bank voltages can be used in a lot of low voltage and low power applications to achieve good power quality with minimum circuitry. But for high voltage and high power applications like UPFC and STATCOM, the uneven structure is no longer attractive. In these applications, the bulky inverter will be very expensive and hard to design, manufacture, and maintain. With only two modules, high voltage devices will be used. This will become impractical when the voltage level is higher than several kilo volts.

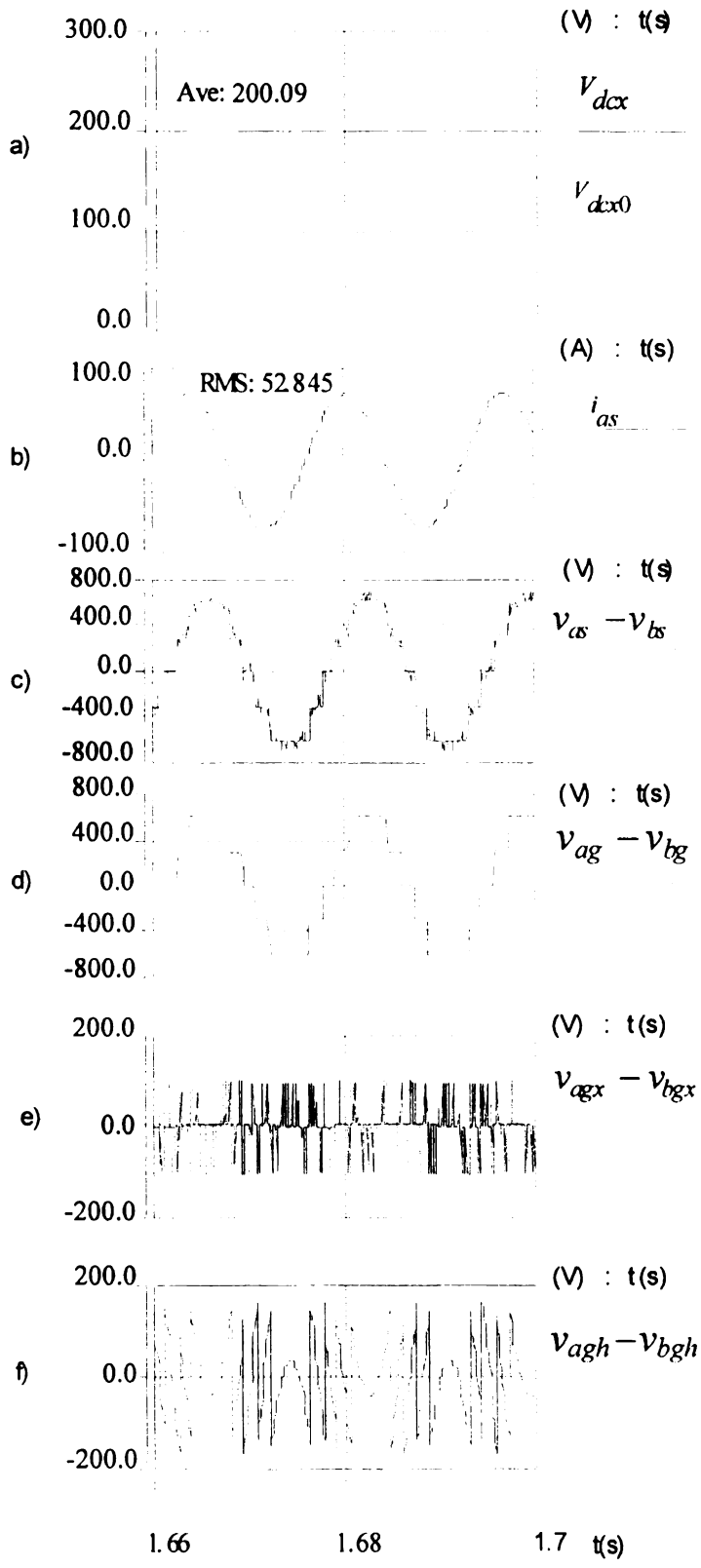


Figure 6.7: The simulation result of the separate control.

6. 4. Applications of Cascade Multilevel Inverters in DG

6. 4. 1. Proposed Applications Examples

The cascade multilevel inverter is the best choice for certain types of DG, where many separated power supply units are involved, such as photovoltaic, fuel cell and wind farm. Figures 6.8-6.10 shows three proposed application examples of cascade multilevel inverters in DG. The circuit topology in Figure 6.8 is aimed at fuel cell and photovoltaic applications, where separated DC sources are available. The topology in Figure 6.9 is for a wind farm, where the ac voltage from the wind turbines are first converted to DC then applied to the cascade multilevel inverter. Figure 6.10 is proposed for the cases that high power quality is required whereas only one DC power supply unit is available to supply the power.

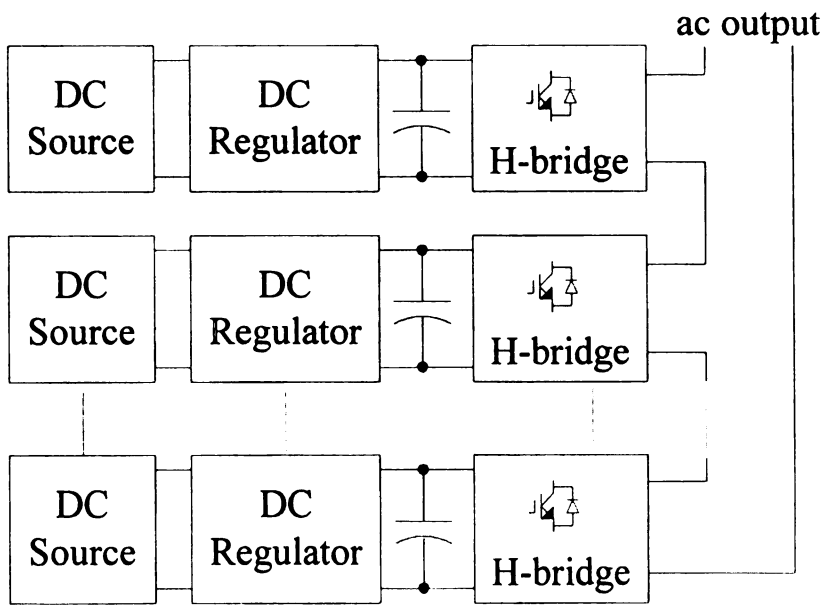


Figure 6.8: The proposed topology 1.

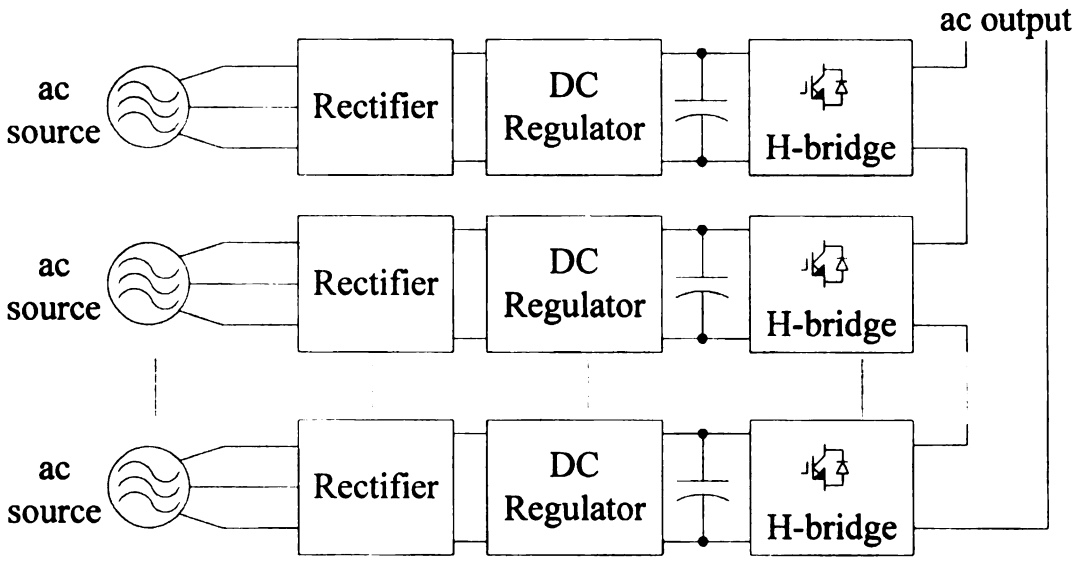


Figure 6.9: The proposed topology 2.

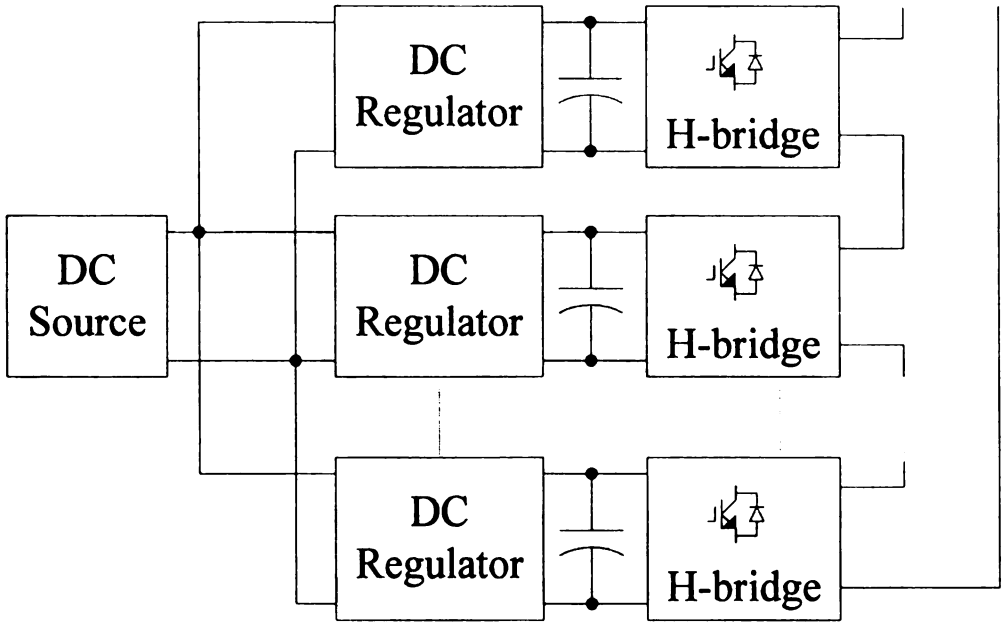


Figure 6.10: The proposed topology 3.

In all three circuits, DC voltage regulators are needed to make sure each module in the cascade multilevel inverter has the same input dc voltage. One thing that must be

noticed is that the DC voltage regulator is needed only in DG applications. In FACTs devices, where in most cases, there is no real power exchange from the inverter to the utility line, the DC voltage on each capacitor of the cascade multilevel inverter can be self-maintained and balanced with proper control. In the proposed DVR, the DC power is from the utility line through the rectifier, and the voltages on each capacitor can also be self-balanced. In DG, real power flows through the cascade multilevel inverter itself. There is no way to balance the capacitor voltages just by rotating the switching sequence. Thus, a DC voltage regulator is needed for each module in the cascade multilevel inverter.

The DC voltage regulator partly decides the performance and cost of the whole DG system. So it is important to find the optimized DC regulator circuit with the best performance, lowest cost and smallest volume for the applications of cascade multilevel inverters in DG.

6. 4. 2 DC-DC Circuit Selection

In general, there are two types of DC-DC converters: isolated and non-isolated. Usually, non-isolated DC-DC converters like buck, boost, buck-boost, and Cuke converter are used at low power applications. In the cases of DG, utilizing these types of converters will result in high cost and low efficiency. Moreover, in the circuit shown in Figure 6.10, isolation is needed. So this chapter mainly focuses on comparisons of isolated dc-dc converters. The general diagram of an isolated DC-DC converter is shown in Figure 6.11.

For isolated DC-DC converters, forward, push-pull, half bridge and full bridge can be considered as topology candidates [131-138]. The advantages and disadvantages of these topologies are fully discussed in [131, 137]. In general, forward and push-pull converters

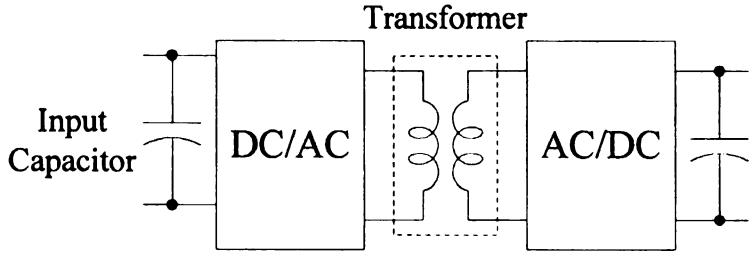


Figure 6.11: The general diagram of isolated dc-dc converter.

are not suitable for high power applications. Forward converters have restrained duty cycles and lossy resetting of excitation; in push-pull converters, the two halves of a center-tapped winding cannot be equal or symmetrically wound, and the power switch on/off times as well as their forward voltage drops are never equal. These irregularities, which exist in practice, can contribute to transformer core saturation and result in the converter failure. In both forward and push-pull converters, the voltage rating of the device is two times that of the half and full bridge. Though the full bridge, compared with the half bridge, has more components, the current in the devices and the transformer turns ratio can both be reduced to half. The current ripple in the front end capacitor is also minimized. The voltage and current stresses on the devices in the full bridge are the smallest in all of the four topologies.

There are also several topology options for the secondary side of the DC-DC converter, such as diode rectifier, controlled rectifier, voltage doubler and controlled voltage doubler. All these four topologies have the same device voltage rating. For the

secondary side, which is directly connected with the cascaded multilevel module, the major concerns for the topology selection should be:

1) Efficiency;

2) Cost;

3) The resulted transformer turns ratio;

4) Power control flexibility.

Voltage doubler circuits will give smaller transformer turns ratio. But it will also lead to a large current ripple in the output capacitor. The current ripple will result in low efficiency, and possible overheat of the capacitor and reduced lifetime of the capacitors. So in the applications of DG, a voltage doubler should only be used when the power is less than 10 kW.

By using the active switches, there will be more flexibility in controlling the power flow and voltage. Active devices will also create more possibility in the control the current waveforms over the transformer, thus the current stress on switches will be depressed. However active switches are more expansive. Furthermore experimental results also show that active control of the secondary side, in order to achieve a higher voltage transfer ratio than in the non-controlled case, will greatly lower the overall system efficiency. Therefore, a full analysis and comparison between the controlled and non-controlled case is performed in the next session.

6. 4. 3. Comparisons Between Two Cases

The circuit structures of controlled and non-controlled case are shown in Figure 6.12(a) and (b). The transformer primary side referred equivalent circuits of the two configurations are shown in Figure 6.12(c) and (d), respectively. The correspondent voltages and current waveform over the transformer are shown in Figure 6.12 (e) and (f). It is found that the voltage doubler and full bridge rectifiers yield the same voltage and current waveforms. The only thing that will make a difference in the current and voltage waveforms is whether the secondary is controlled or not. So, the controlled voltage doubler and uncontrolled full bridge are shown in Figure 6.12(a) and (b), respectively.

Case 1. Controlled rectifier

In Figure 6.12, Ls is the leakage inductance of the transformer. The full bridge and voltage doubler are controlled to switch at high frequency to produce two square voltage waveforms with a phase shift, θ, as shown in Figure 6.12(e). The two square-wave voltages are impressed across the both sides of the transformer, respectively. So the current over the leakage inductance would look like the i_s as shown in the Figure 6.12(e). As i_s is a function of ωt, where ω is the switching frequency, the current waveform can be analyzed as following:

At 0 radian in Figure 6.12(e), the primary side voltage becomes positive while the secondary side voltage remains negative, creating a positive voltage across the leakage inductance making the current increase until $\omega t = \theta$, where the secondary voltage changes polarity from negative to positive. The current at this point can be written as

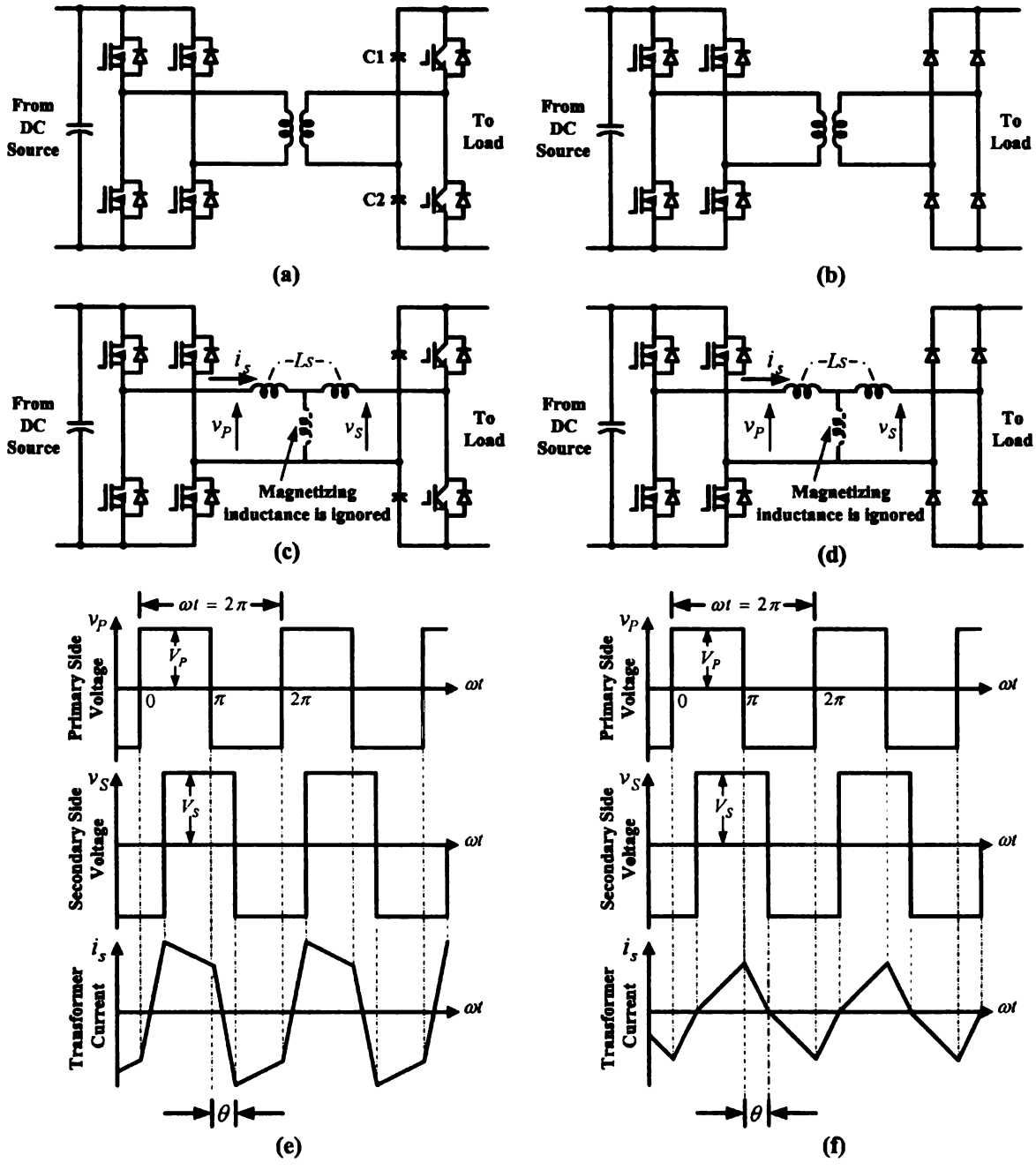


Figure 6.12: Two configurations of the secondary side in the isolated dc-dc converter.

$$i_s(\theta) = \frac{V_P + V_S}{\omega Ls}\theta + i_s(0), \quad \omega t = \theta \tag{6. 7}$$

where V_P and V_S are the amplitudes of the transformer primary side and secondary side voltage.

With proper control, V_S can be smaller, bigger or equal to V_P. The peak current will be minimized when $V_S = V_P$ is met. Figure 6.12(e) shows the case of $V_P < V_S$.

At $\omega t = \theta$, the secondary side voltage becomes positive while the primary side voltage remains positive, making the voltage across the leakage inductance negative, allowing the current to decay until $\omega t = \pi$, where the primary voltage changes from positive to negative,

$$i_s(\pi) = \frac{V_P - V_S}{\omega Ls}(\pi - \theta) + i_s(\theta), \qquad \omega t = \pi . \tag{6. 8}$$

At this point, the primary side voltage becomes negative while the secondary side voltage remains positive, creating a negative voltage across the leakage inductance, making the current keep decreasing until $\omega t = \pi + \theta$, where the secondary voltage changes polarity again,

$$i_s(\pi + \theta) = -\frac{V_P + V_S}{\omega Ls}(\pi - \theta) + i_s(\pi), \qquad \omega t = \pi + \theta . \tag{6. 9}$$

After the secondary voltage changes polarity, the secondary side voltage becomes negative while the primary side voltage remains negative, making the voltage across the leakage inductance positive allowing the current to increase to point 1, where

$$i_S(2\pi) = -\frac{V_P - V_S}{\omega Ls}(\pi - \theta) + i_S(\pi + \theta), \qquad \omega t = 2\pi . \tag{6. 10}$$

Because $i_S(\theta) = -i_S(\pi + \theta)$ and $i_S(\pi) = -i_S(2\pi)$, the exact relationship between the current and voltages can be found as equation (6. 11) and (6. 12) by solving equation(6. 7)-(6. 10)

$$i_S(\theta) = \frac{2V_P\delta + (V_S - V_P)\pi}{2\omega Ls} \tag{6. 11}$$

$$i_S(\pi) = \frac{2V_S\theta + (V_P - V_S)\pi}{2\omega Ls} . \tag{6. 12}$$

From the representation of $i_S(\omega t)$, the RMS value of the transformer current and the power transferred through the transformer can be found as:

$$Irms = \frac{1\cdot\sqrt{12}}{24\cdot\pi}\cdot\sqrt{\frac{12\cdot\pi\cdot\theta^2\cdot V_P\cdot V_S - 8\cdot\theta^3\cdot V_P\cdot V_S - 2\cdot\pi^3\cdot V_P\cdot V_S + \pi^3\cdot {V_S}^2 + \pi^3\cdot {V_P}^2}{\pi\cdot f^2\cdot Ls^2}} , \tag{6. 13}$$

and

$$P = -\frac{1}{2}\cdot\theta\cdot V_P\cdot V_S\cdot\frac{(-\pi + \theta)}{(\pi^2\cdot f\cdot Ls)} . \tag{6. 14}$$

Three conclusions can be made based on the Figure 6. 12(e) and the equations obtained above:

1) The power is transferred through the leakage inductance;

2) By controlling the phase shift of the voltages between the two sides of the transformer, the power transferred over the transformer as well as the secondary side dc voltage, V_S, can be precisely controlled;

3) If the system is controlled to have $V_S \approx V_P$, the current wave form would be rather flat, which means the peak current can be smaller.

In summary, for the controlled rectifier case, the voltage angle difference, θ, and the secondary side voltage, V_S, are both controllable by properly coordinating the control of the primary side and secondary side. The power transferred over the transformer, P, can be variable at fixed secondary dc voltage, V_S. V_S can be equal to or larger than the primary voltage V_P.

Case 2. Uncontrolled Rectifier

The analysis of the uncontrolled case can be made by using the same method used for the controlled case. In uncontrolled case, θ is no longer controllable, the relationship between θ and V_S, is found as

$$\theta = \pi \cdot \frac{V_P - V_S}{2 \cdot V_P}, \tag{6. 15}$$

where $V_P > V_S$.

The power transferred over the transformer and RMS value of the current are

$$P = \frac{1}{T}\int_0^T v_p \cdot i_s \cdot dt = \frac{(V_P{}^2 - V_S{}^2)\cdot V_S}{8 \cdot V_P \cdot Ls \cdot f}, \tag{6. 16}$$

and

$$I_{rms} = \sqrt{\frac{1}{T}\int_0^T i_s{}^2 dt} = \frac{\sqrt{3}\cdot\left(V_P{}^2 - V_S{}^2\right)}{12 \cdot V_P \cdot Ls \cdot f}. \tag{6. 17}$$

From equations 6. 15-6. 17, it can be seen that θ decides both the secondary side voltage, V_S, and the transferred power, P. For the diode rectifier, V_S can not be equal to or larger than V_P, thus, the controllable ranges of output voltage and power are quite limited.

Figure 6.13 shows the comparisons of the power transfer ability and the RMS current over the transformer in the two cases.

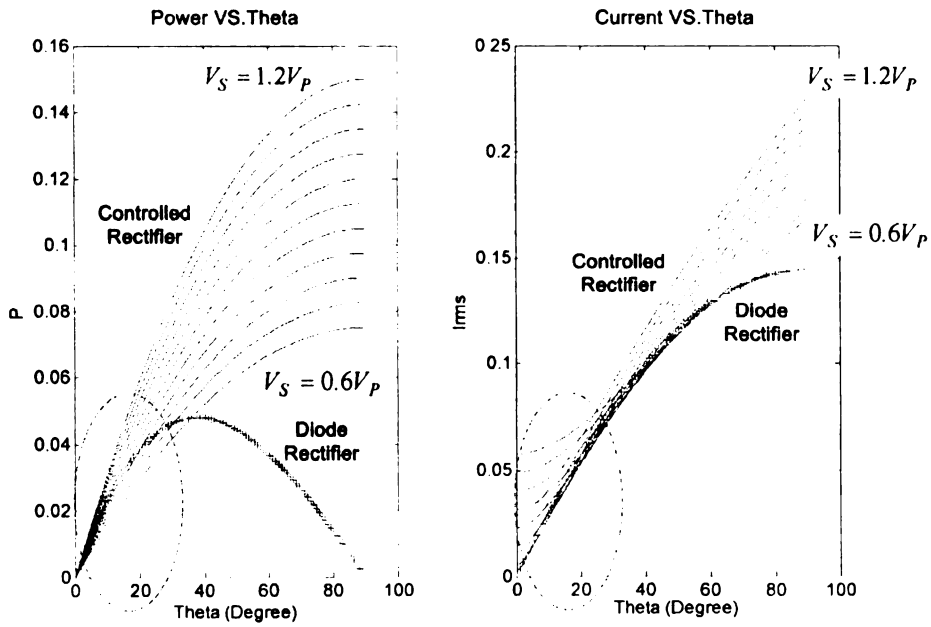


Figure 6.13: The transferred power and RMS current on the transformer in these two cases.

For the uncontrolled diode rectifier case, there is only one power curve and one current curve related to θ. In the controlled rectifier case, for both power and current, there is a region related to each θ respectively. Figure 6.13 only shows several most often used curves in the region that V_S changes from 0.6 V_P to 1.2 V_P.

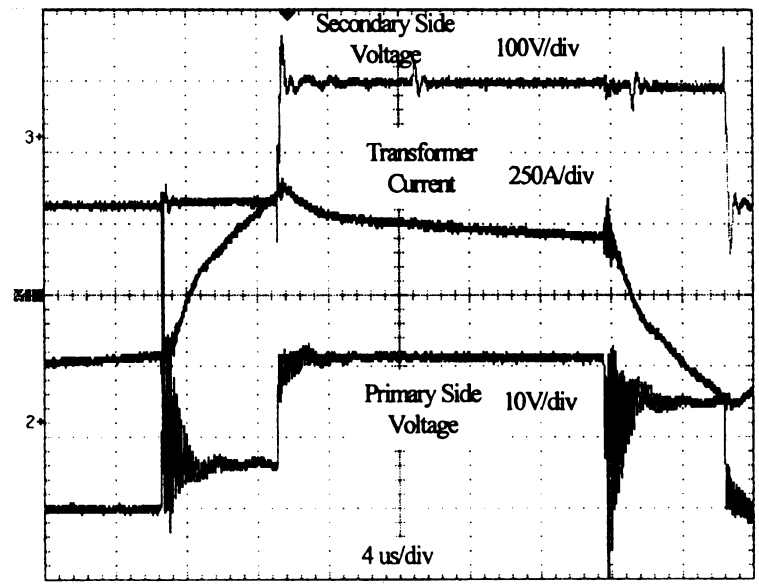
One major observation from the Figure 6.13 is that when θ changes from 0 to 20 degree, which is the common DC-DC converter operating area, the controlled rectifier has a higher RMS current, whereas there is no big difference in the power transferred in both cases. This means there will be more power loss on the transformer and switches in the controlled rectifier case. Besides the power losses introduced by the RMS current, switching loss of high power devices at high frequency is also much larger than the rectifier diodes reverse recovery loss. In one word, the controlled rectifier case will not have better efficiency than the uncontrolled case.

Further research on the system stability shows that the controlled case is stable while the uncontrolled case is asymptotically stable, which means the uncontrolled case would have better stability performance.

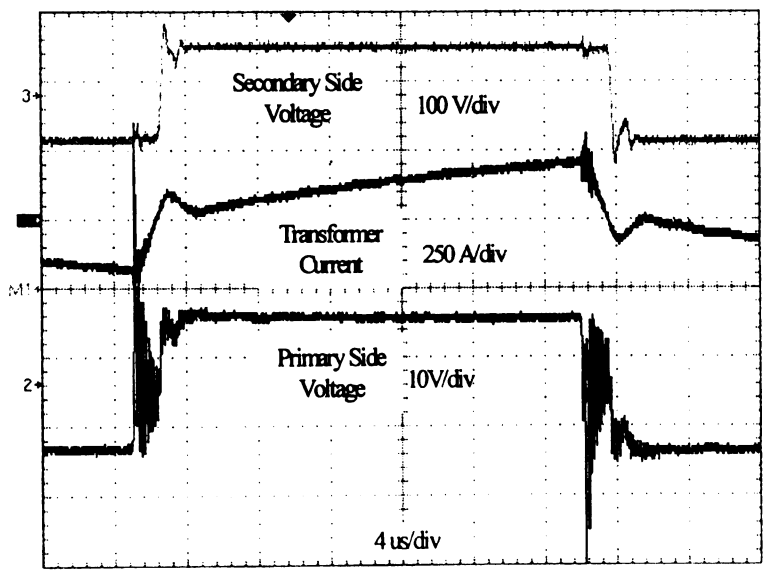
6. 4. 4 Experimental Verification

Experimental results on one 5 kW fuel cell DC-DC converter is shown in Figure 6.14. Figure 6.15 is a photo of the testing setup. In the experiments, the input power to the dc-dc converter is supplied by a 12 V battery. The transformer turns ratio is 1:8. The secondary side is a voltage doubler with two IGBTs. The DC-DC converter is connected to a resistive load. For the controlled case, the secondary side IGBT was controlled to

switching at 20 kHz. For the uncontrolled case, the IGBTs were not switching, and therefore all the current goes through the free wheeling diodes paralleled with the IGBT. The efficiency comparison results are summarized in Table 6.1.



(a) The controlled rectifier case



(b) The uncontrolled rectifier case

Figure 6.14: The experimental waveforms of the two different cases.

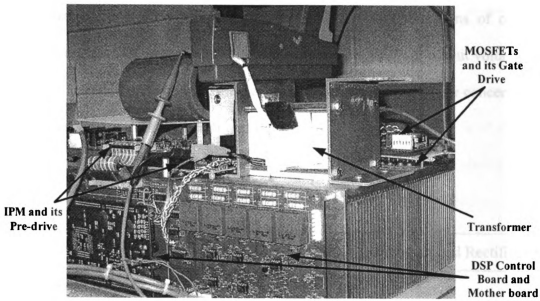


Figure 6.15: Test setup of the DC-DC converter.

Table 6.1: The efficiency comparison

	Vp (V)	Vs	Efficiency
Uncontrolled Case	11.2	78.5	91%
Controlled Case	11.15	79	68%

The waveforms shown in Figure 6.15 resemble the idea analytical waveforms. In the controlled case, during the phase shifting, there is a voltage drop on the primary voltage. This is caused by the voltage drop on the leakage inductance of the transformer. The measured efficiency also verifies the analysis. The experimental results verified the analytical results.

Table 6.2 summarizes the comparisons between the controlled and uncontrolled cases.

Based on the comparison results, it can be concluded that the full bridge inverter cascaded with a high frequency transformer and uncontrolled rectifier would be the

optimized circuits for the isolated DC regulator in the DG applications of cascade multilevel inverters. The controlled rectifier has a larger controllable output voltage and power range. But the when the cost, efficiency, and stability are the major concerns, the uncontrolled rectifier becomes more practical.

Table 6.2: The summary of the comparisons

	Controlled Rectifier	Uncontrolled Rectifier
Controllable Voltage Range	Larger controllable output voltage range	
Controllable Power Range	Larger controllable output power range	
System Stability		Better system stability performance
Transformer Current	Almost square waveform with less peak current	Triangular Waveform with higher peak current
Efficiency		Higher Efficiency
Cost		Lower Cost

6. 5. Summary

In this chapter, the applications of multilevel inverters in distribution system were proposed. With the UPFC and U-STATCOM proposed in Chapter 4, and 5, applications of multilevel inverters in all levels of power system have been demonstrated. After figuring out the optimized DC regulator circuit, together with the methods mentioned in

Chapter 3, the question of how to maintain and balance of the DC banks in multilevel inverters has been fully answered.

Since all the different levels of applications of multilevel inverters and their implementation issues have been addressed, in the next Chapter, one 17 level cascade multilevel inverter together with the realization of its control unit will be shown. With the 17 level cascade multilevel inverter setup, the harmonics cancellation method proposed in Chapter 3 will be experimentally verified.

Chapter Seven

A 17 LEVEL CASCADE MULTILEVEL INVERTER AND EXPERIMENTAL RESULTS

7. 1. Introduction

A 17 level cascade multilevel inverter is shown in this chapter. Each module of the cascade multilevel inverter indeed is a three level diode clamped H-bridge. Thus, each module can output a 5 level voltage. For each phase, a total of four modules are cascaded to output a 17 level phase voltage. The realization of the control unit for the inverter is described in detail. Experimental results from this inverter are used to prove the harmonics elimination method proposed in Chapter 3.

7. 2. The 17 Level Cascade Multilevel Inverter

A 17 level, 1 MVA, 6000 V cascade multilevel inverter is shown Figure 7.1. The inverter was designed and built in house at Power Electronics and Motor Drive Laboratory of Michigan State University. Each phase of the cascade multilevel inverter has four modules, resulting in a total of 12 modules. Each module is a diode clamped H bridge with a maximum 5 level output. This topology makes it possible for the total output phase voltage to have a maximum of 17 level phase voltage and 33 level line-to-line voltage. Figure 7.2 shows the schematic of the cascade multilevel inverter.

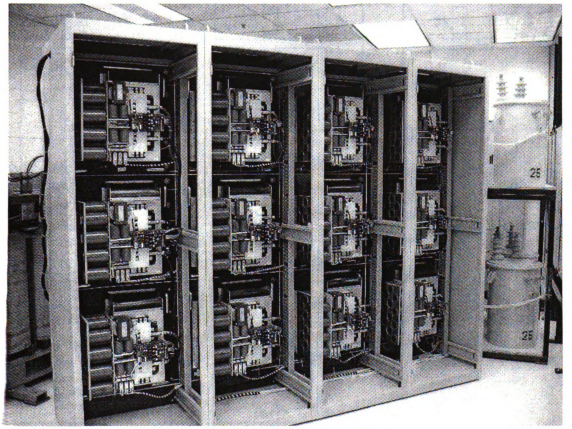


Figure 7.1: The 17 level cascade multilevel inverter.

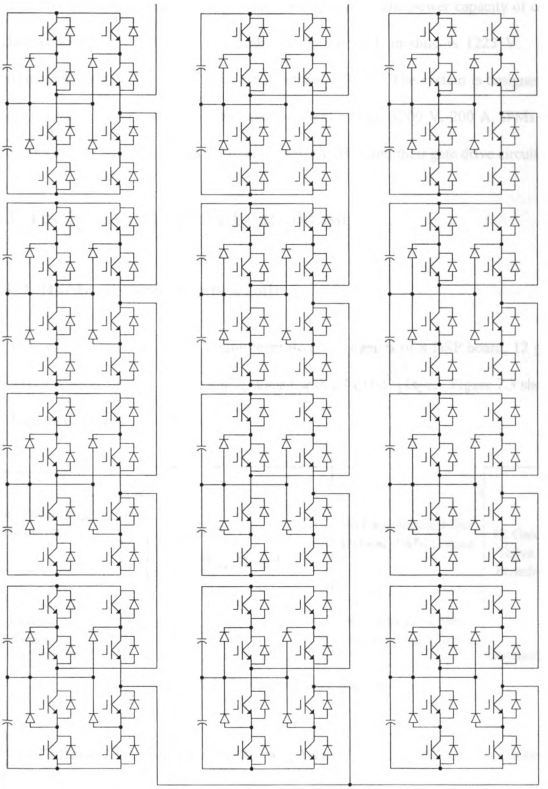


Figure 7.2: The schematic of the 17 level cascade multilevel inverter.

The inverter was designed as an induction motor drive. The power capacity of each module is 83 kVA. The rated DC bank voltage for each module is 1225 V. The maximum DC voltage is 1600 V. The rated current is 96 A. The system is designed to ensure operation under and up to 120% rated current. Thus, 1200 V, 200 A, IPMs are used as switching devices. Each IPM integrates two IGBTs and their gate drive circuits.

7. 3. The Realization of the Control Unit

7. 3. 1. Hardware of the Control Unit

The control unit of the cascade multilevel inverter consists of a DSP board, 12 gate drive boards, three current sensors and a keypad with a LED displayer. Figure 7.3 shows the diagram of the control unit.

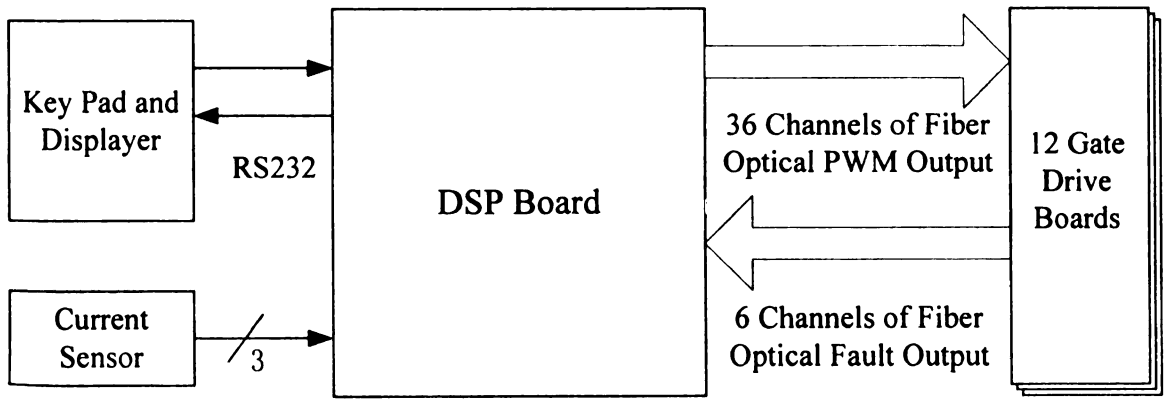


Figure 7.3: The control unit diagram.

The DSP board is the core part of the control unit. It receives the control command from the keyboard, generates the control signals for the gate drives, sends information to

the displayer for display, responses to the outputs of the current sensors, and realizes the protection of the system during fault conditions.

The DSP board is shown in Figure 7.4.

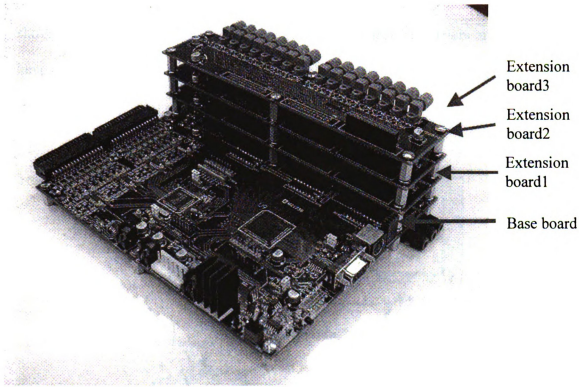


Figure 7.4: Picture of the DSP board.

The DSP board consists of one base board and three extension boards. The base board has one DSP chip, one CPLD chip, 16 channels of A/D, one RS232 communication port, one can bus, 8 channel optical inputs and 16 channel optical outputs. The calculation, command response, communication, A/D conversion, part of logic combination, and generation of control signals are realized inside the DSP chip. The CPLD performs the most of the logic combinations. Each extension board receives 16

control signals from the CPLD and outputs 16 optical signals. In the case of the 17 level cascade multilevel inverter, only two extension boards are utilized.

The DSP board communicates with the keyboard and displayer through a RS232 serial communication port. The connection diagram of the keyboard and displayer is shown in Figure 7.5. During operation, the initial control parameters are setup with the keypad and displayer. Then, the DSP board generates 36 coded control signals to 12 gate drive boards.

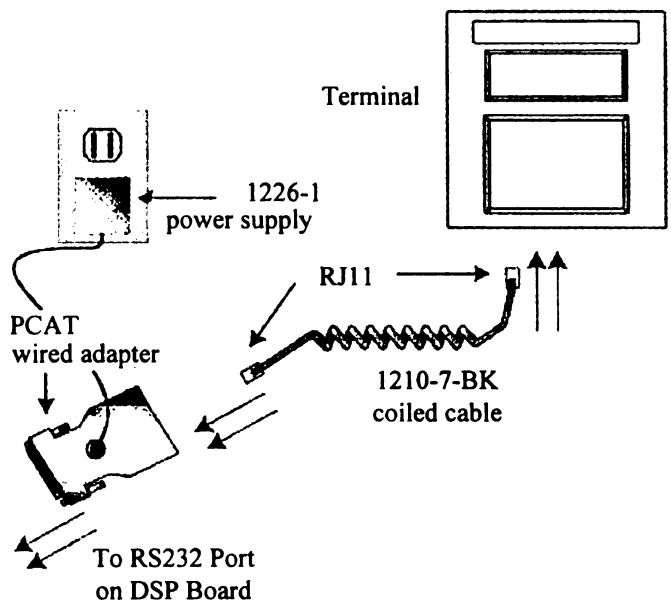


Figure 7.5: The connection of the keyboard/displayer.

For each module of the cascade multilevel inverter, there is one gate drive board to drive the 8 switches. Since the IPMs already integrate the gate drive circuit, the 12 gate drive board's main functions are receiving optical control command, decoding, and realizing protection at fault conditions. Each gate drive board has three optical inputs for control signals and one optical output for fault output. The core part of the gate drive

board is a CPLD chip. This CPLD chip decodes eight control signals, realizes protections, and sends out a fault output at fault conditions. Since each gate drive board has one fault output, total there are 12 fault outputs. As the DSP board only has 8 optical receivers, every two fault signals from the inverter modules are first cascaded, then sent to the DSP. Thus there are total 6 fault outputs to the DSP board. The fault output connection is shown in Figure 7.6.

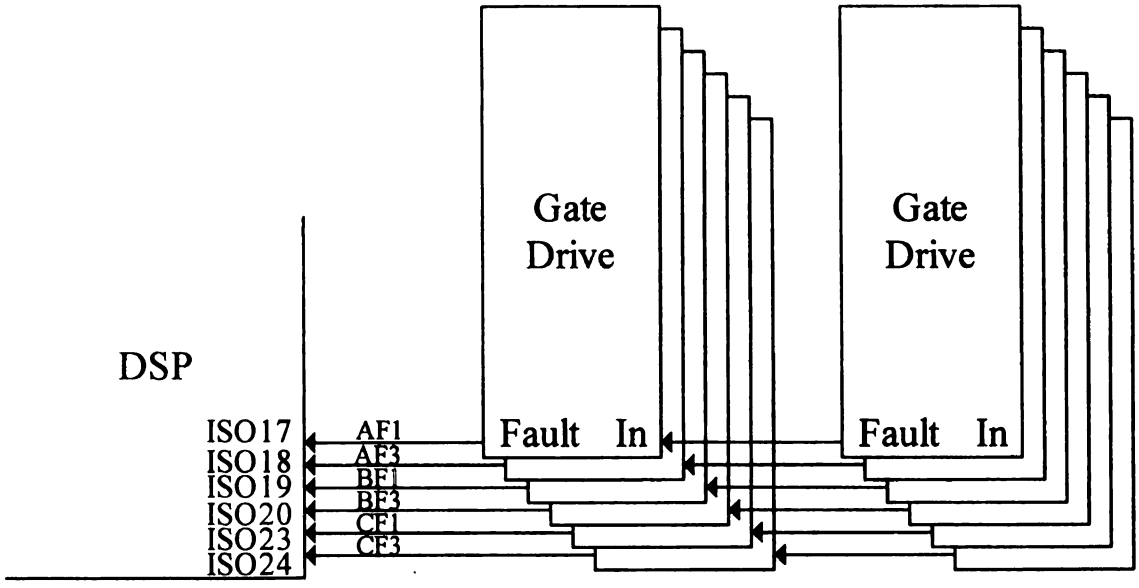


Figure 7.6: The connection of fault signal.

7. 3. 2. Control Signal Generation

In the control of the multilevel inverter, there are two ways to generate control signals for the inverters:

1) at higher modulation index, utilizing optimized switching angles to control the inverter to output staircase waveform;

2) at lower modulation index, utilizing the multiple carrier PWM method to generate PWM signals to control the inverter to have PWM output.

a. stair case waveform generation

To realize the staircase waveform, one simple solution is to use lookup tables. Tables are used to store all the switch states and their angle intervals. To better illustrate this idea, a simple example is shown in Figure 7.7.

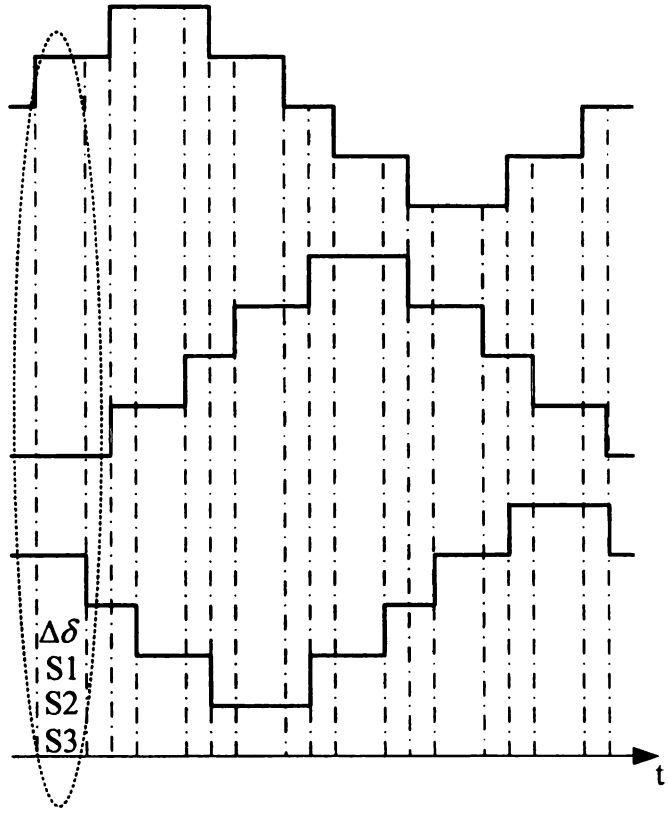


Figure 7.7: The storage unit in the table.

For a fixed modulation index, the waveform is divided into many small divisions by the edges of step changes in the three phases. Each angle interval, $\Delta\delta$, and its three phase switch states, S1, S2 and S3, are stored in the following format in the table:

```
.WORD 972                    ;Plength,, time length of angle interval, Δδ, at 60 Hz
.WORD 1100110011101100B     ;S1, phase a switch states
        A1 A2 A3 A4
.WORD 1010111011101110B     ;S2, phase b switch states
        B1 B2 B3 B4
.WORD 1110100010101110B     ;S3, phase c switch states
        C1 C2 C3 C4
```

In this example, 'Plength' equals 927, and stands for the time length of $\Delta\delta$ when the fundamental frequency is 60 Hz. The calculation of 'Plength' can be expressed as $Plength = \frac{\Delta\delta}{2\pi \times 60} / 50 \times 10^{-9}$. The underlined 12 bits in each switch states word is the status of the 12 output pins of DSP.

To drive the 8 switches in one inverter module, at least 3 inputs to the gate drive board are required. So a total of 36 independent outputs from DSP board are needed. The DSP chip alone does not have this output capacity. Thus, a time sharing scheme is used in the software to generate 12 control signals for one phase at a time. 12 Pins on the DSP chip are configured as general I/O pins to fulfill this task. The statuses of these 12 I/O pins are decided by the bits in S1, S2, and S3. A GP timer inside the DSP is used to count the time of the switch status. An additional four I/O pins are fed into the CPLD as timing control pins. Three of them decide which phase the 12 control signals belong to. The fourth timing signal will flip all the 36 output at the time that a new switch state starts. The functional diagram of the CPLD for this method is shown in Figure 7.8.

b. PWM generation

To generate PWM signals, for regular inverter with only six control signals, the DSP's build-in PWM unit can be utilized to directly realize hardware PWM. But for a

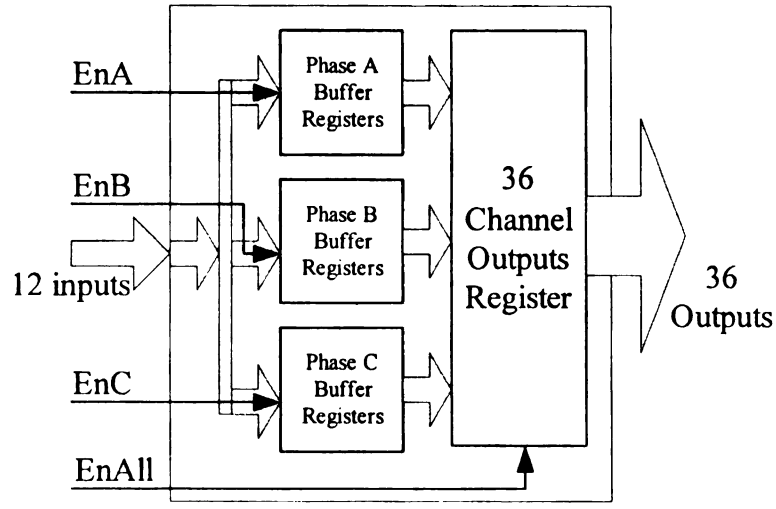


Figure 7.8: The detailed functional diagram of the CPLD.

multilevel inverter with at least 36 control signals, there are not enough independent output pins in the DSP's PWM unit to accomplish this. In this case, there are two methods to realize PWM signals.

One method is to use the exact same method used for the staircase waveform. The switch states and time interval of PWM can be pre-calculated and stored in tables. The problem with method is that at very low modulation index, where more PWM pulses are involved, the table becomes very large. The total number of tables that can be saved in the 32 kbyte of the flash of the DSP chip is limited.

Another method is to utilize the hardware PWM and software allocation at the same time. In this method, sinusoidal reference waves will be cut into several sessions by voltage levels. Then after the corresponding offset has been subtracted from each section, the section will be used to compared with the same triangular carrier wave to generate PWM signals. However, the PWM generated at this time only means a voltage level change in the output. It even does not show in which level the change happens. Thus,

software must kick in to decide, at a particular time, which section to be compared with the triangular and which voltage level has to be changed, and eventually encode at least four additional controls pins to feed the CPLD. Since software is involved in the PWM generation, timing is still very important. The best way to guarantee the timing is to use compare interrupt from the EV block of DSP.

c. *decoding in the CPLD of the gate drive board*

It is mentioned that the CPLD on the gate drive needs to decode the three inputs signals to eight control signals. If the three control inputs to the CPLD on the gate drive board are named as K1, K2, and K3, and the 8 control signals to the switches are Sa1, Sa2, Sb1, Sb2, Sa1', Sa2', Sb1', and Sb2', the relationship between them can be summarized in Table 7.1. The control signals and their correspondent switches are shown in Figure 7.9.

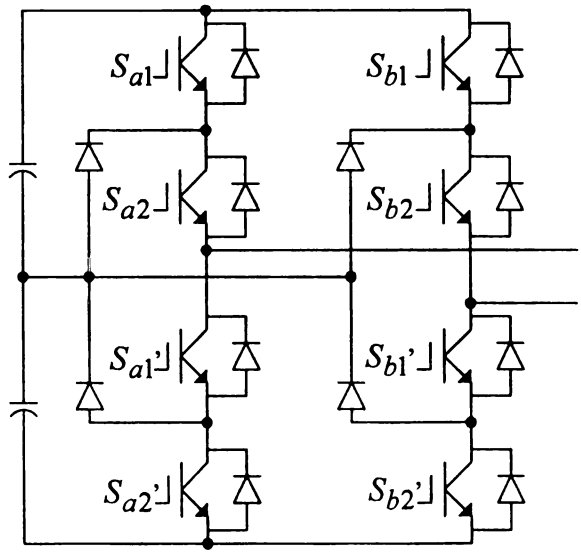


Figure 7.9: The inverter module structure.

Table 7.1: The gate drive CPLD decoding table.

K1	K2	K3	Sa1	Sa2	Sb1	Sb2	Sa1'	Sa2'	Sb1'	Sb2'
1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	0	1	0	0	1	0	1
1	0	1	1	0	1	1	0	1	0	0
1	0	0	0	0	1	1	1	1	0	0
0	1	1	0	0	1	0	1	1	0	1
0	1	0	1	0	0	0	0	1	1	1
0	0	1	1	1	0	0	0	0	1	1
0	0	0	1	1	1	0	0	0	0	1

When K1, K2, and K3 are all '1', all the control signals to IGBT are also '1'. Due to the circuit nature, at all the other conditions, Sxx should be complimentary with Sxx'. Based on Table 7.1, the relationship between Kx and Sxx can be described with following equations:

$$Sa1 = K1 \& K2 \& K3 + K1 \& K2 \& \overline{K}3 + K1 \& \overline{K}2 \& K3$$
$$+ \overline{K}1 \& K2 \& \overline{K}3 + \overline{K}1 \& \overline{K}2 \& K3 + \overline{K}1 \& \overline{K}2 \& \overline{K}3$$

$$Sa2 = K1 \& K2 \& K3 + \overline{K}1 \& \overline{K}2 \& K3 + \overline{K}1 \& \overline{K}2 \& \overline{K}3$$

$$Sb1 = K1 \& K2 \& K3 + K1 \& K2 \& \overline{K}3 + K1 \& \overline{K}2 \& K3$$
$$+ K1 \& \overline{K}2 \& \overline{K}3 + \overline{K}1 \& K2 \& K3 + \overline{K}1 \& \overline{K}2 \& \overline{K}3$$

$$Sb2 = K1 \& K2 \& K3 + K1 \& \overline{K}2 \& K3 + K1 \& \overline{K}2 \& \overline{K}3$$

7. 3. 3. Inverter Module Voltage Balancing

Each phase of the inverter has 4 modules. To keep the voltages on the modules balanced with each other, the DC bank voltage balance method introduced in Chapter 3 is used. In the programming, module voltage balancing is realized inside DSP. The main

idea is to rotate the switch states from one module to another every fundamental cycle. The rotation scheme is shown in Figure 7.10. Since the inverter is designed for induction motor drive. The DC banks of the inverter are powered by isolated rectifiers. Thus, DC voltage maintenance is not needed in this case.

7. 3. 4. Fault Protection Scheme

There are four levels of protection in the whole system:

1) The first level is inside the IPMs. Each IPM has over current, over temperature and UVLO protection. When one of the faults happens, the IPM will protect itself and send a fault output to the gate drive board.

2) The second level of protection is inside the CPLD of the gate drive board. The fault outputs from the IPMs are fed to the CPLD. Once the CPLD detected fault, it will wait 6 μs, then shut down the module and send fault output to DSP board. The 6 μs waiting period is to ensure that the faulty IPM has enough time to soft shut down.

3) The fault inputs to the DSP board are first fed to the CPLD chip, the CPLD will shut down all the output immediately. At the same time, a protection signal is fed to the DSP chip.

4) The protection signal will trip hardware blocking of DSP's I/O ports and initiate a protection interrupt routine. The interrupt routine will again block all the I/O and disable all the interrupts, show "Stopped" on the displayer, then wait for

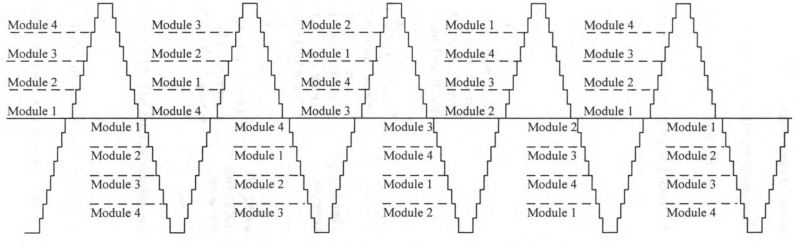


Figure 7.10: The rotation of switch states between modules.

manual reset. The load current sensor outputs are also fed to the DSP chip. If the peak current is bigger than 200 A, the program will goes to the protection routine and shows "Over Current" on the displayer.

The diagram of protection scheme is shown in Figure 7.11.

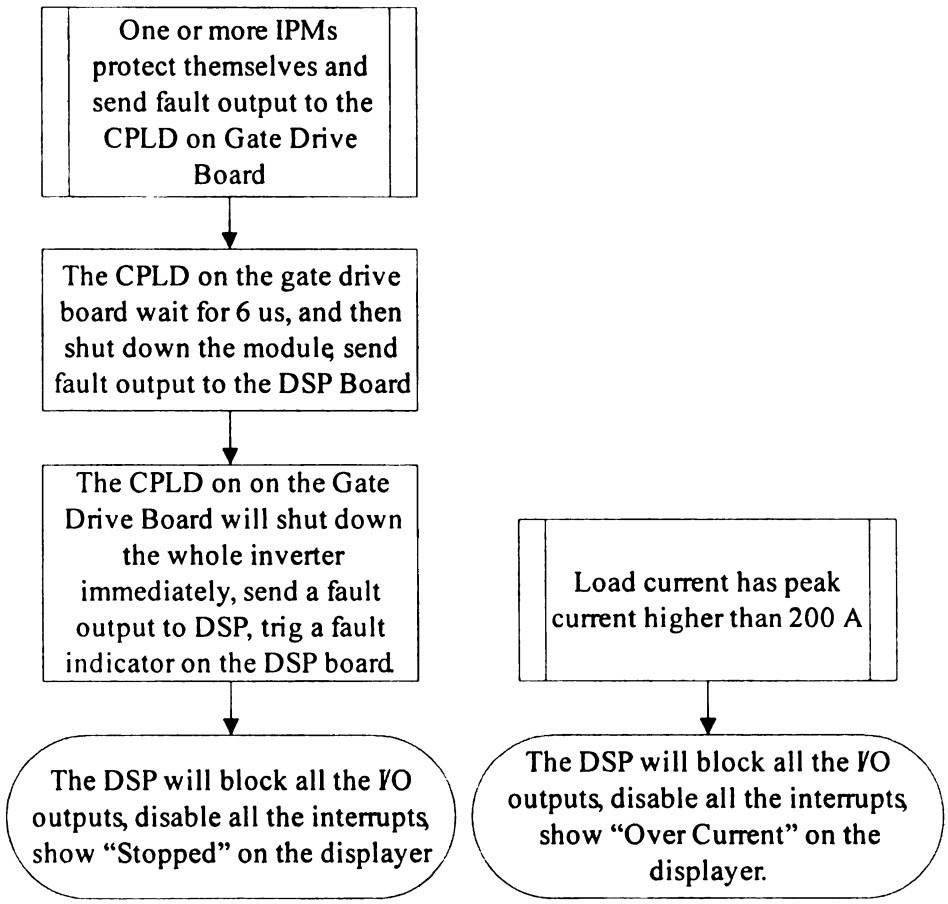


Figure 7.11: The fault protection scheme.

The detailed function blocks of the control unit are shown in Figure 7.12. In the experiments of the 17 level cascade multilevel inverter, look up tables are used to generate staircase waveform and PWM waveforms.

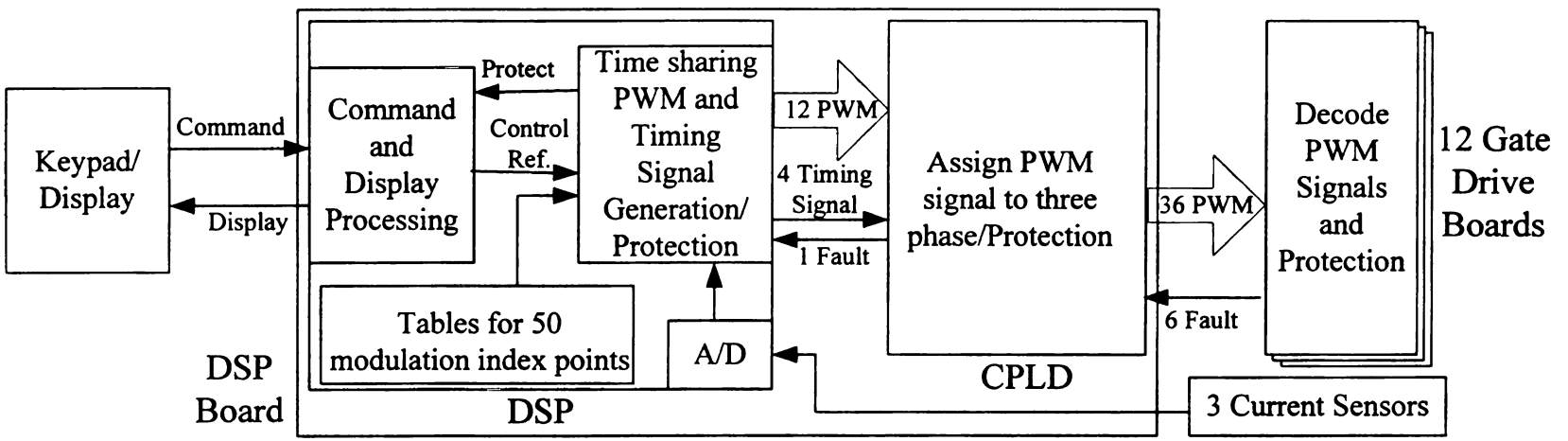


Figure 7.12: The detailed function block of the control unit.

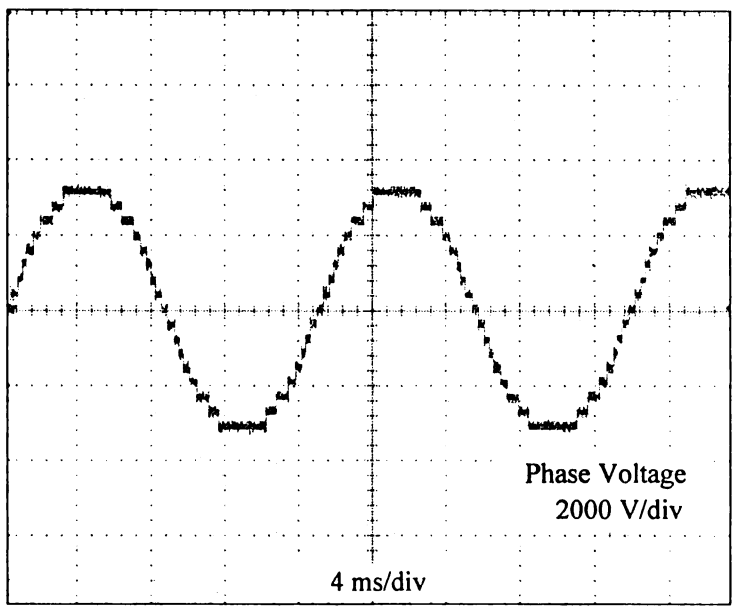
7. 4. The Experimental Results

Experiments have been carried out to prove the harmonics cancellation method proposed in Chapter 3 with the 1 MVA 17 level cascade multilevel inverter. In the experiments, the dc bank voltage of each inverter module was fixed at 800 V, thus each voltage level was 400 V. The modulation index was fixed as 0.84. Six harmonics, 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th} and 19^{th}, are optimized with eight switching angles listed in Table 7.1.

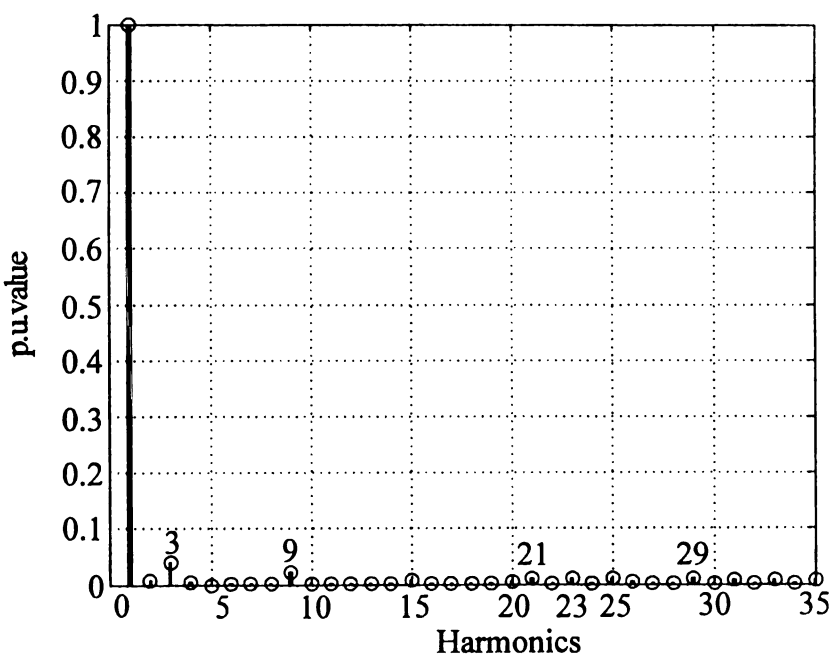
In calculation results, the selected harmonics are less than 1 pico p.u. Figure 7.13(a) shows the phase voltage. Corresponding FFT analysis of the waveform is shown in Figure 7.13(b). Figure 7.14 shows the line-line voltage and its FFT analysis. Both FFT results in Figure 7.13 and Figure 7.14 show the selected harmonics are eliminated. In the line-line voltage, there are also no third harmonics. The experimental results verify the proposed method.

Table 7.2: The switching angles for MI=0.84

	θ_1 (rad.)	θ_2 (rad.)	θ_3 (rad.)	θ_4 (rad.)
	0.05995	0.18863	0.28101	0.36322
MI=0.84	θ_5 (rad.)	θ_6 (rad.)	θ_7 (rad.)	θ_8 (rad.)
	0.50503	0.63771	0.87771	1.0889

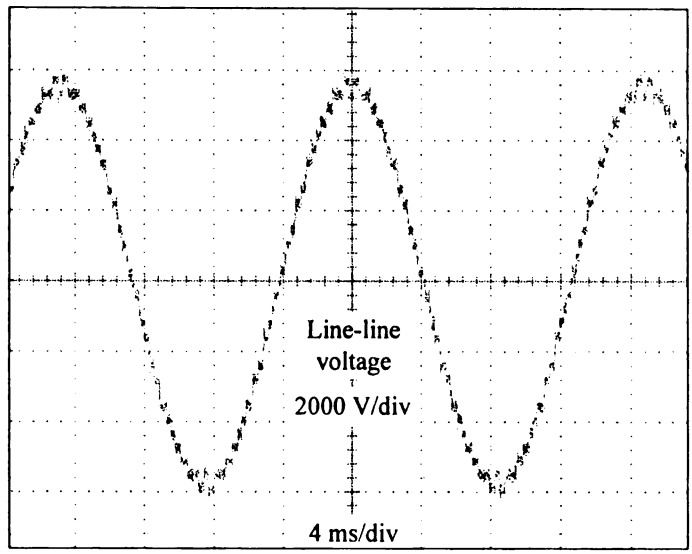


(a). The phase voltage at MI=0.84

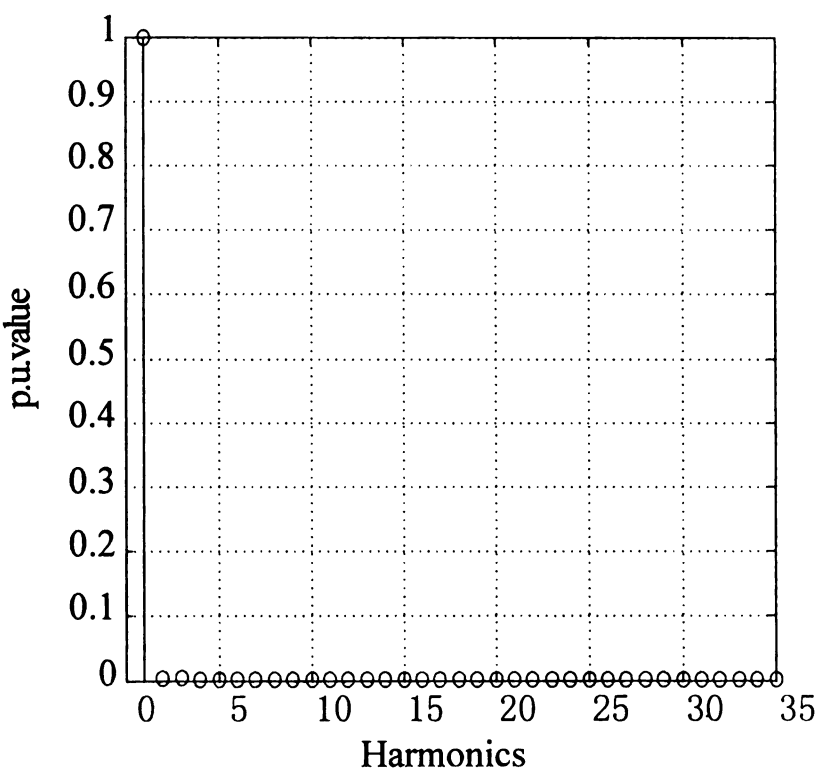


(b). FFT analysis result

Figure 7.13: The phase voltage when MI=0.84.



(a). The line-line voltage at MI=0.84



(b). FFT analysis result

Figure 7.14: The line-line voltage when MI=0.84.

7. 4. Summary

In this chapter, a 1MVA 17 level cascade multilevel inverter was shown. The hardware and software realization of its control unit were described in detail. Experimental results were shown to prove the harmonics elimination method proposed in Chapter 3.

Chapter Eight

CONCLUSIONS

8. 1. Conclusions

Multilevel inverters are the next generation inverters for utility applications. With multilevel inverters, the bulky transformers used in FACTs, Custom Power and DG devices are no longer needed. The power loss, volume, and cost of these devices will be greatly reduced, whereas the reliabilities of the devices will be increased. Among the three major multilevel inverters, the cascade multilevel inverter is the most suitable one for power system applications. In the cascade multilevel inverter, the H-Bridge can be modularized. For high voltage and high power applications, this characteristic of the cascade multilevel inverter will greatly increase the flexibility in the design, manufacture, and maintenance.

The major effort of this work was to propose new ways of utilizing cascade multilevel inverters in FACTs devices. Extension applications of multilevel inverters, real implementation issues, as well as the realization of a DSP based control unit for a 17 level cascade multilevel inverter were also presented.

The most important issues for the implementations of multilevel inverters are output voltage harmonics elimination and DC bank voltage maintenance and balance. In Chapter 3, a new harmonics elimination method based on equal area criteria and harmonics injection was proposed. The basic idea and steps for the realization steps of the proposed method were described in detail.

In power system applications, there are three conditions for DC voltage maintenance: 1) pure reactive and harmonics compensation, 2) back-to-back connection structures, and 3) voltage regulation in DG. The first two conditions were discussed and shown in Chapter 3 and 4. The method for DC voltage regulation in DG was shown in Chapter 6. The optimized DC voltage regulator circuit has been identified and proved by experimental results.

The most important applications of multilevel inverters in the power system are FACTs devices for the transmission system. But for the most advanced FACTs device—the UPFC, the cascade multilevel inverter can not be used since it can not be back-to-back connected. In Chapter 4, a new face-to-face UPFC circuit structure was proposed. The circuit analysis, operating principle, and control strategy of the proposed structure were presented. Full comparisons between the conventional and proposed structures were carried out. Simulation results were used to verify the proposed structure.

As for the most commonly used FACTs device—the STATCOM, a delta-connected cascade multilevel inverter structure was proposed in Chapter 5. The current imbalance compensation theory, compensation component detection method, control strategy and simulation results were presented.

Extended applications of multilevel inverters in power system were discussed in Chapter 6. For Custom Power, a DVR with uneven cascade multilevel inverter structure was proposed. Three examples of applications of cascade multilevel inverter in DG were also shown.

A 1 MVA 17 level cascade multilevel inverter was introduced in Chapter 7. The realization of the DSP based control unit was fully described. Experiments were performed to verify the harmonics elimination method proposed in Chapter 3.

8. 2. Contributions

This work has contributed to the existing body of knowledge as follows.

- A new UPFC circuit configuration has been proposed. Benefiting from the proposed face-to-face configuration, the cascade multilevel inverter can be used. With proper control, no active power flows through either inverter. The total VA rating of the proposed configuration is smaller than the conventional configuration at most operating conditions. Thus the stress and power loss on the devices could be reduced, which will further increase the total efficiency and reliability.

- A delta-connected cascade multilevel inverter based Universal STATCOM has been proposed. Unlike the conventional STATCOM, the proposed U-STATCOM can be used to compensate imbalance in the load current without active power flow through the inverter. Thus universal compensation can be realized.

- A new harmonics elimination method has been proposed. Many harmonics elimination methods have been proposed in the last decades. But no simple and practical method has ever been found. Almost all the proposed methods need to solve multi-variable, high order polynomial equation groups. The method proposed in this work only involves five steps and four simple equations. It is much simpler and more practical than all the other methods.

- An uneven cascade multilevel inverter - based transfomerless DVR with only one DC source per phase has been proposed. The proposed DVR shows the possibility and advantages of utilizing uneven cascade multilevel inverter in low voltage and low power situations. For the high voltage and high power applications, the uneven structure will reduce the benefits of utilizing the cascade multilevel inverter since in the uneven structure the H-Bridges can no longer be modularized.

- The optimized DC voltage regulator circuit for application of cascade multilevel inverter in DG has been identified. Compared with other circuits, the optimized circuit has the lowest voltage and current stress and the highest efficiency.

- Three applications of cascade multilevel inverters have been proposed for different types of DG.

- A DSP based control unit for a 17 level cascade multilevel inverter was realized. For the commercially available DSPs, a single DSP chip is usually designed to drive a maximum of three 6-switch inverters at one time. In the realization of the control unit with only one DSP chip, time sharing scheme and lookup tables are used to overcome this problem.

8. 3. Recommendations for Future Work

The proposed face-to-face configuration for UPFC can also be extended to other applications. One direct example is the Unified Power Quality Conditioner (UPQC). The main functions of the UPQC are to eliminate harmonics, compensate reactive power, and correct system imbalance in the distribution systems. Though the functions of UPQC are quite different from the UPFC, they have the same back-to-back structure. The same active power flow control strategy used in the UPFC can also be used in the UPQC. Even when the UPQC is controlled to correct current or voltage imbalance, the active power flow through both inverters can be controlled to be zero.

The uneven cascade multilevel inverter structure used for the DVR can also be used for some DG applications, where the power rating is not too high and only one DC or AC source is available. The DC bank of the major inverter will be connected to the power source. The load current also flows though the power source, the cascade multilevel inverter, and the load. But because the conditioning inverter is controlled to output only harmonics voltage, there would be no active power exchange between the conditioning inverter and any other part of the circuit. Thus, with proper control, the load would have

a high quality voltage input. And at the same time, the DC voltage of the conditioning inverter automatically remains constant.

The same idea behind the proposed harmonics elimination method can be applied to calculate optimum PWM for high power inverters. In high power inverters, to reduce the switching loss, switching frequency is limited to very near the fundamental frequency. Thus, high harmonics content will appear in the output voltage of the inverter. To eliminate the harmonics, optimum PWM angles are usually calculated based on complex algorithm like linear least squares with constraints. In this case, to simplify the PWM switching angle calculation, the equal area criteria and harmonics injection can also be used. The same five steps and similar equations as in the method proposed in Chapter 3 can be used to calculate PWM angles.

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List of Projects and Publications

Projects since Aug. 2001:

- 2003~2005: Leaded the design, building and testing of a 260 kVA Auxiliary Power Supply for passenger train.
- 2004~2005: Participated in 50 kW Z Source Inverter Project.
- 2003~2005: Programmed and tested 1 MVA Cascade Multilevel Inverter for induction motor drive.
- 2004: Completed 1.5 MVA Traction Inverter Module programming and testing.
- 2002~ 2003: 50 kW Universal Inverter Module programming and testing.
- 2002~2003: Completed the 10 kW Fuel Cell Inverter System, leaded in designing, building, programming and testing.
- 2002: Performed simulation and analysis of Cascade Multilevel Inverter's control strategy.
- 2002: Designed and completed a Sensor-Less Drive for Brushless DC motor.
- 2002: Completed 10 kW Z Source Inverter prototype, participated in building, programming and testing.
- 2001: Performed simulation and analysis of a novel Multi-Level Converter based of Unified Power Flow Controller (UPFC).

Publications:

IEEE Transaction Papers:

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Major Conference Papers:

[6] Jin Wang, Yi Huang, and F.Z. Peng, "*A Practical Harmonics Elimination Method for Multilevel Inverters*", accepted by 40th Industry Application Society annual meeting. Hong Kong, 2005

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[10] F.Z. Peng and Jin Wang *"A Universal STATCOM with Delta Connected Cascade Multilevel Inverter"*, 35th IEEE Power Electronics Specialists Conference PESC04, pp: 3529~3533, June, 2004

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[12] Jin Wang and F.Z. Peng *"Low Cost Fuel Cell Inverter System For Residential Power Generation"*, 19th IEEE Applied Power Electronics Conference and Exposition, 2004. APEC '04, pp: 367~373, Feb. 2004

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