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Minority Carrier Injection in Schottky Barrier Diodes

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D. K. Reinhard
Major professor

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MINORITY CARRIER INJECTION IN SCHOTTKY BARRIER DIODES

By

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ABSTRACT

"MINORITY CARRIER INJECTION IN SCHOTTKY BARRIER DIODES"

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Mohsen Alavi

For low to moderate current densities, current flow in Schottky barrier diodes (SBDs) is primarily due to majority carrier injection over the metal-semiconductor interface. However, at high current densities, such as are encountered in advanced integrated circuits, minority carrier effects become significant. The objective of this study was to experimentally verify and quantify minority carrier injection in platinum-silicide SBDs, develop boundary conditions expressing carrier injection at the metal-semiconductor interface which extend to high injection conditions, and correlate the results with numerical simulation. Two experimental measures of minority carrier injection have been investigated, minority carrier storage and conductivity modulation. Also, new methods have been devised to accurately determine the barrier height of the SBD from its I-V characteristics.

Minority carrier storage has been experimentally determined by integration of the reverse bias switching current which, after correction for capacitance stored charge, yields the minority carrier charge removed from the diode on switching from forward to reverse bias. The stored charge was found to increase monotonically both with temperature and forward biased current over the experimental range of 27°C to 125°C and 10^4 A/cm^2 to 10^5 A/cm^2. For 12.5X12 μm unguarded SBDs fabricated on a 1 μm thick n-type epitaxial layer, stored minority carrier charge at 10^5 A/cm^2 was on the order of 10^{-5} C/cm^2. For guarded SBDs, the stored

minority carrier charge was higher, on the order of $5X10^{-5}$ C/cm^2 at 10^5 A/cm^2. Conductivity modulation was investigated by current-voltage measurements at current densities up to $4X10^5$ A/cm^2 and was found to be appreciable, causing the series resistance of the diode to decrease by approximately a factor of 5 at the higher currents.

One dimensional numerical simulation results using traditional boundary conditions agree well with both charge storage and conductivity modulation measurements up to $5X10^4$ A/cm^2. At higher current densities, however, there is significant difference between simple simulation results and experiment, and additional phenomena including hole tunneling, image-force induced band-gap shrinkage, hole barrier height lowering at high injection, Auger recombination, and lateral voltage drop are considered.

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CHAPTER ONE

INTRODUCTION

1.1 Statement of Problem

Schottky barrier diodes (SBDs) are widely used in electronic circuits for a variety of functions. Current flow in these diodes, at low to moderate current densities and temperatures, is primarily due to majority carrier injection from the semiconductor to the metal over the metal-semiconductor interface. The lack of minority carrier injection, and therefore lack of minority carrier storage, leads to considerable SBD speed advantages as compared to p-n junction diodes. At sufficiently high current densities or temperatures, however, minority carrier effects in Schottky barrier diodes become significant.

The issue is of current interest in advanced bipolar logic circuits that utilize SBDs. As bipolar integrated circuits are scaled down in size, higher current densities are necessary to exploit

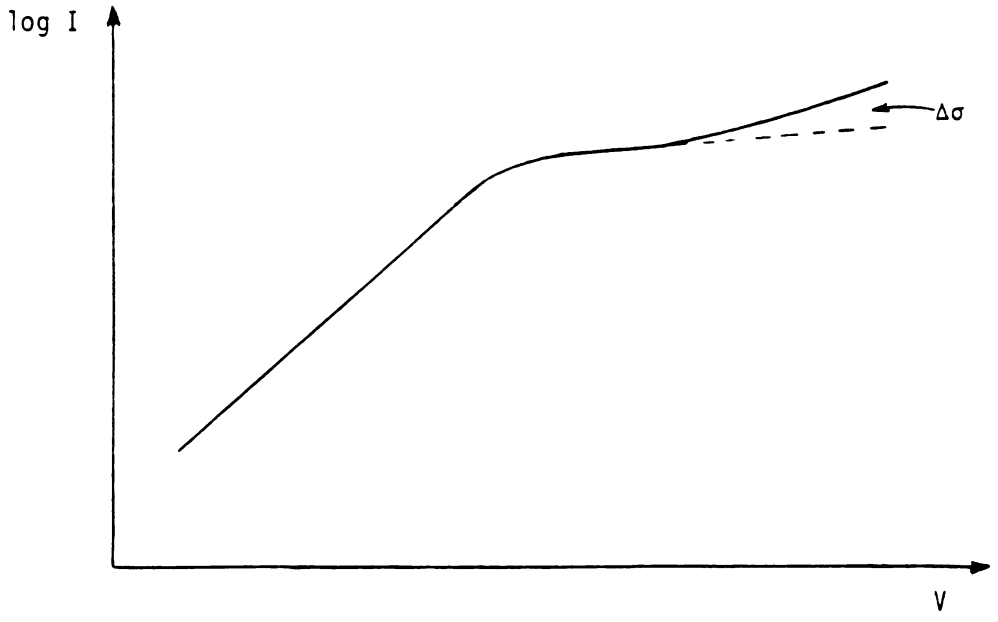
advantages of scaling related improvements in speed. This is in part because the junction voltages required to turn on a bipolar junction transistor do not scale down since they are already low. Gate delay times in a digital circuit may be expressed in general form as

$$t_d = C_o V/J \qquad (1\text{-}1)$$

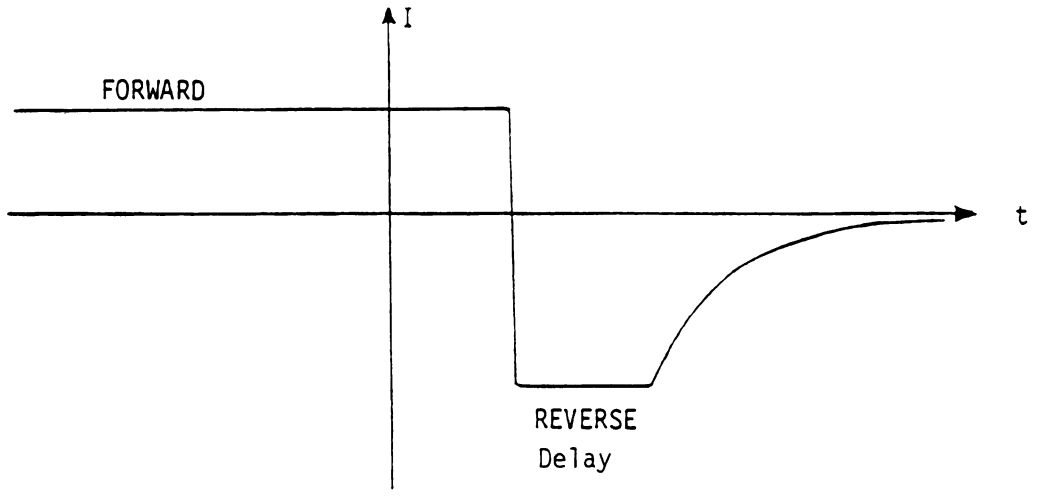
where C_o is the capacitance per unit area to be charged and discharged over a voltage range V by a current density J. Since C_o increases with scaling due to decreasing depletion layer widths, the current density must also increase to avoid increased delay times. The combination of higher current densities and unscaled voltages result, in turn, in a higher density of dissipated power and hence, larger operating temperatures.

Current densities as high as $1.3X10^5$ A/cm^2 have been reported in high performance bipolar switching circuits that have been fabricated with VLSI device dimensions [1]. At such current levels, SBD models which incorporate minority carrier injection effects are required. Minority carrier injection is further pronounced in guarded SBDs in which p-type guard rings are used to avoid undesirable effects associated with high electric fields at the electrode edge.

Injection of minority carriers leads to excess carrier storage in the bulk of the device. The stored excess carriers, in turn, change SBD characteristics in two principal ways, as illustrated in Figure 1-1. Static current-voltage characteristics are altered because of conductivity modulation induced by excess carriers, and dynamic properties are modified due to carrier-storage induced switching delay times. So, in circuits operating at high current densities, minority



(a)



(b)

Figure 1-1 Minority carrier injection results in excess carrier storage which changes device characteristics in two principal ways. (a) The bulk conductivity is modulated. (b) Switching delay is induced.

carrier injection has to be properly considered for its effects on the value of the bulk conductivity as well as the added switching delay. Another motivation for understanding the phenomenon is the possible latching of an integrated circuit Schottky diode and an adjacent npn transistor caused by minority carrier injection, due to a mechanism similar to the latching of a silicon controlled rectifier (SCR), [2].

The purpose of this study is to provide experimental quantification of minority carrier injection in planar platinum-silicide Schottky barrier diodes and to correlate the results with a numerical device simulation in order to aid in establishing correct device models. Specifically, two experimental measures of minority carrier injection are investigated. First, the charge due to stored minority carriers is measured by current integration during the diode switching transient from forward to reverse bias. Secondly, the conductivity modulated forward I-V characteristics of the device are measured under large forward bias conditions. The results are then correlated with a numerical simulation of the basic equations governing carrier transport in the device.

1.2 Preview of Contents

Chapter 2 covers the background material, starting with a brief discussion of the physical structure of an SBD and various mechanisms of current transport in the device. Then, the attention is focused on minority carrier injection in SBDs, discussing its effects and reviewing the previous theoretical and experimental studies of the phenomenon.

Chapter 3 presents the experimental part of the study. Specifically, a measurement technique is described which detects the pico-coulombs of charge associated with minority carrier storage, which discharge in nanosecond time frames, for current densities as high as 10^5 A/cm^2. Additionally, a method is described to measure conductivity modulated forward J-V characteristics for current densities as high as 4×10^5 A/cm^2. The experimental results, along with the experiment's limits and accuracy are presented after the discussion of each measurement method.

Chapter 4 describes the theoretical simulation, starting by discussing the basic theory of carrier transport in the device. Then the approach to the solution of the problem by previous investigations is briefly discussed and finally, other phenomena beyond the previous work are explored and new corrections are made.to the traditional theory. Specifically considered are energy gap shrinkage, hole barrier height lowering, and hole tunneling at high injection, all of which result from the effect of the image-force on the valence-band in silicon near the junction. Additionally, a method is presented to correct the one dimensional simulation for the lateral voltage drop in the n^+ buried layer.

An important parameter in the numerical simulation is the value of the barrier height of the device. Since the value of the barrier height depends on the processing involved in the fabrication of the device, It must be measured for the devices under study. Chapter 5 describes various I-V methods for the measurement of barrier height and demonstrates shortcomings of each method theoretically as well as experimentally. A modification of one of the methods is then proposed which provides highly accurate results for the value of the barrier

height. This method is then used to determine the barrier height at four temperatures.

Chapter 6 is devoted to the comparison of the experiment and simulation results. First, the correlation between experiment and theory based on the traditional simulation is examined and shortcomings of the simulation are demonstrated. Subsequently, lateral voltage drop, hole barrier height lowering, image-force induced energy-gap shrinkage, and Auger recombination are considered separately and the effect of each phenomenon on correlation of simulation and experiment is observed Finally, high temperature comparison of simulation and experiment is discussed.

Chapter 7 includes the summary and conclusions of the work and discusses recommendations for further studies of the phenomenon. The chapter is followed by three appendices which contain the details of various experimental procedures (Appendix A), and derivations of some of the theoretical results developed in this work (Appendices B, C).

1.3 Main Contributions of this Work

This thesis presents a comprehensive study of minority carrier injection in Schottky barrier diodes by direct measurement of both minority carrier storage and forward J-V characteristics, correlated with numerical simulation. Such a study has not been previously reported. Furthermore, the experiment extends reverse-recovery minority carrier storage measurements to current densities several orders of magnitude higher than previously reported [3].

Theoretically, modifications of some forward I-V methods for determining the barrier height of an SBD are developed to improve their

performance, and one modification is shown to generate highly accurate results. The numerical simulations were performed by C.C. Yu [4] at IBM corporation. The contributions of this work to the simulation were the inclusion of effects due to hole barrier lowering, energy gap shrinkage, Auger recombination, and buried-layer lateral voltage drop.

CHAPTER TWO

BACKGROUND

2.1 Introduction

A metal-semiconductor contact may show rectification properties or the characteristics of an ohmic contact depending on the choice of metal and semiconductor as well as the impurity concentration in the semiconductor and the processing involved in its fabrication. The asymmetric nature of electrical conduction between metal contacts and semiconductors such as copper and iron sulphide was first discovered in the late 19^{th} century and while the rectification mechanism was not understood, contacts between metal points and metallic sulphides were used extensively as detectors in early experiments on radio. The rapid growth of broadcasting in the 1920s owed much to the "cat's-whisker" rectifier which consisted of a tungsten point in contact with a crystal, usually of lead-sulphide [5].

In 1938, Schottky and, independently Mott, pointed out that the observed direction of rectification in a metal-semiconductor contact could be explained by supposing that majority carriers from the semiconductor passed over a barrier through the normal processes of drift and diffusion. Mott assumed that the barrier region of the semiconductor was devoid of charged impurities so that the electric field was constant and the electrostatic potential varied linearly as the metal was approached. In contrast, Schottky supposed that the barrier region contained a constant density of charged impurities so that the electric field increased linearly and the electrostatic potential quadratically [5].

Schottky's assumption on the shape of the barrier conforms fairly closely to what usually occurs in practice, so that barriers associated with metal-semiconductor contacts are often referred to as Schottky barriers and contacts which have rectifying properties are referred to as Schottky barrier diodes. Modern planar SBDs are extended area contacts formed by the deposition of metal films in high-vacuum. Such planar contacts are much more stable and reproducible than point contacts. The SBD is usually fabricated using n-type semiconductors since a larger barrier height and consequently, more rectification is achieved.

This chapter discusses the structure of a planar SBD, considers various mechanisms of current transport in the SBD, and then focuses on minority carrier injection, discussing its effects and reviewing the previous theoretical and experimental studies of the phenomenon. Throughout the remainder of this work, n-type devices are considered while similar arguments could be made and parallel conclusions could be drawn for p-type devices.

2.2 Structure of a Planar SBD

In bipolar silicon integrated circuits, SBDs are fabricated as follows. A lightly to moderately doped n-type epitaxial layer is grown on a p-type substrate on top of which is a heavily doped n-type (n^+) area, and then a metal layer is deposited on the epitaxial layer to form the anode. A metal contact to an n^+ region that is connected to the n^+ buried layer forms the cathode ohmic contact. A p-type guard ring is sometimes fabricated around the anode to eliminate undesirable leakage currents caused by the high electric fields present at the edge of the metal. Figure 2-1 shows examples of the cross sections of the guarded and unguarded SBDs and Figure 2-2 shows the energy band diagram of the planar SBD, neglecting the effect of the image force at the junction. As will be shown later, minority carrier injection is much more profound in guarded devices due to the presence of the guard ring as an additional source of minority carriers.

2.3 Current Transport Mechanisms

The various ways in which electrons can be transported across the junction of an SBD under forward bias are shown schematically in Figure 2-3. The mechanisms include the emission of electrons from the semiconductor over the top of the barrier into the metal, quantum-mechanical tunneling through the barrier, recombination in the space charge region and minority carrier injection [5].

The principle mechanism of current flow in the SBD is the emission of majority carriers over the barrier which is governed by the thermionic emission, as well as diffusion and drift in the depletion

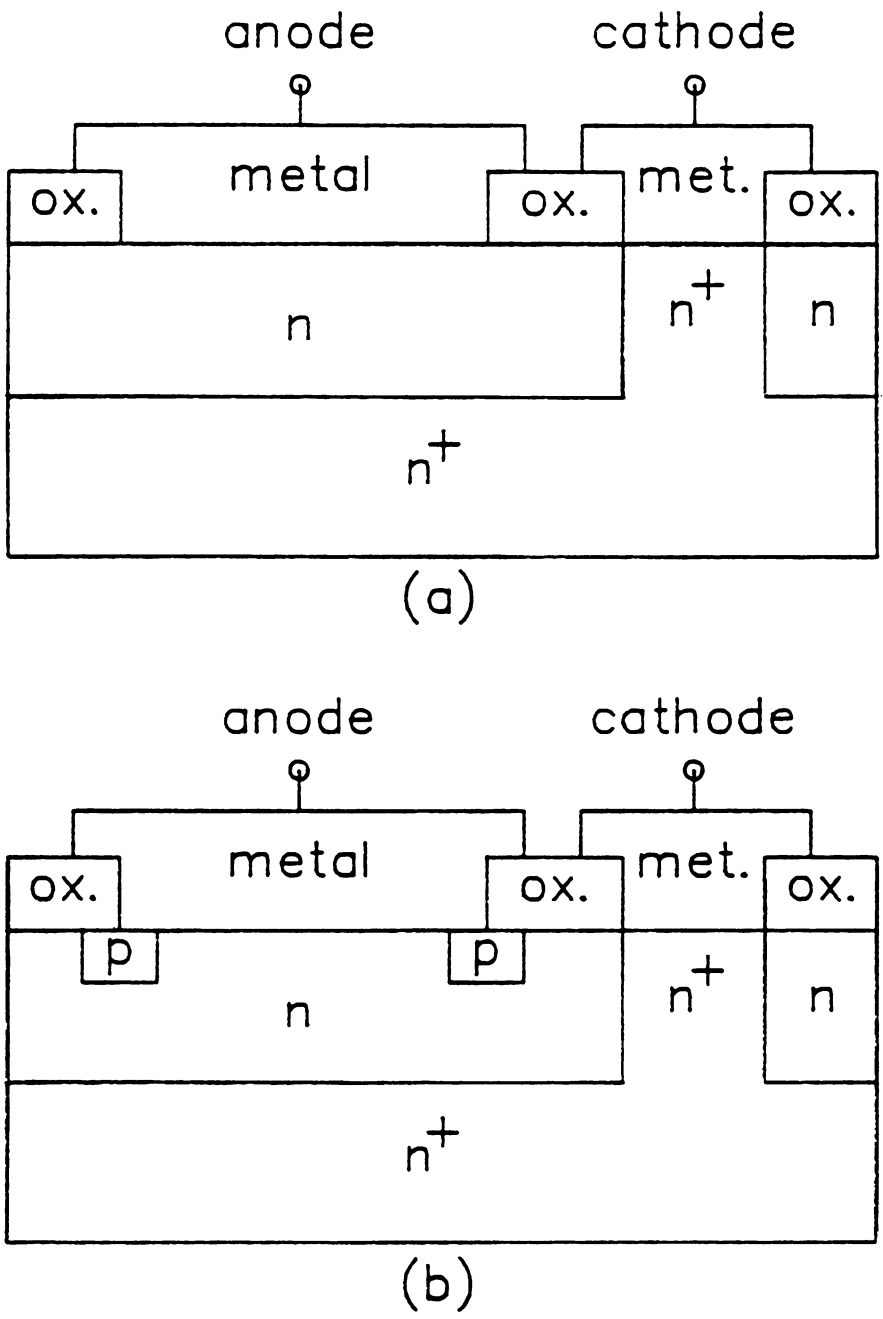


Figure 2-1 Structure of a planar SBD. (a) Unguarded. (b) Guarded.

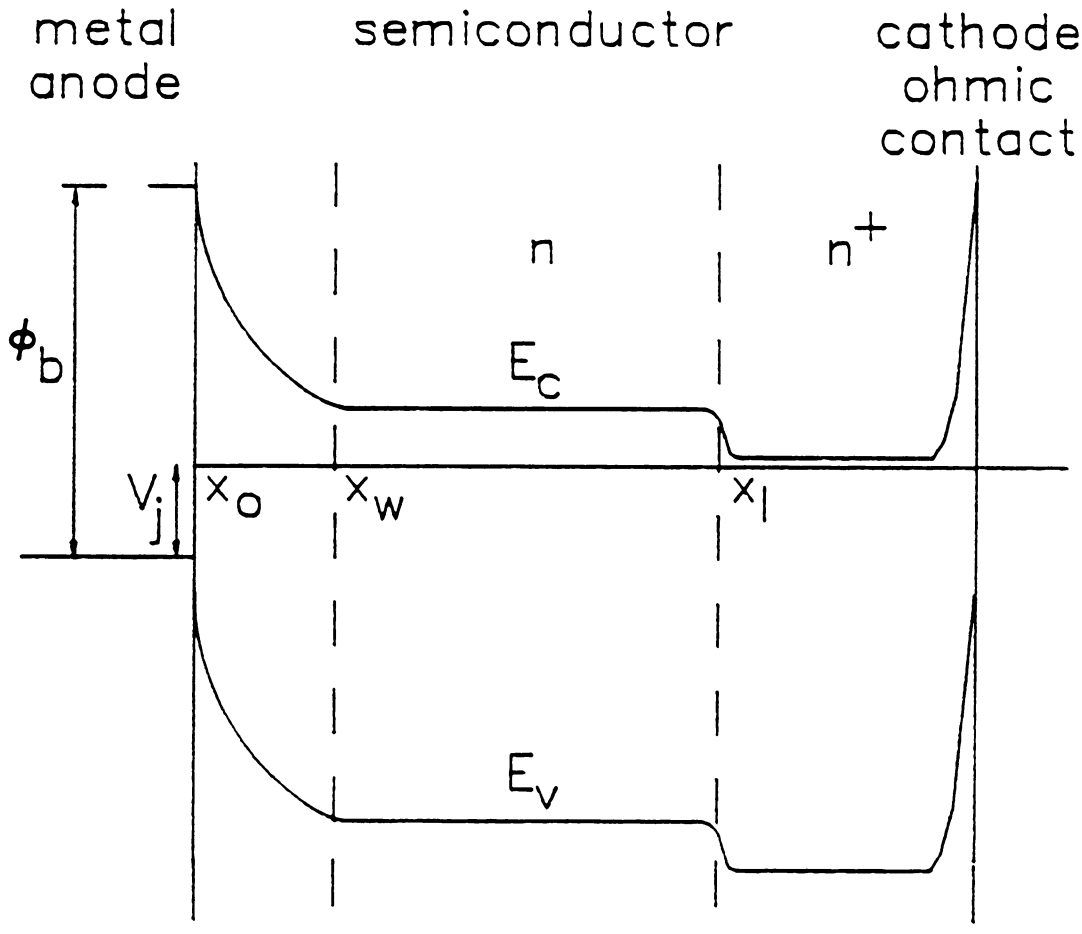


Figure 2-2 Energy band diagram of a planar SBD neglecting the effects of image-force at the metal-semiconductor interface. The horizontal axis is not to scale. The position of the contact is denoted by x_o, the position of the edge of the depletion layer is denoted by x_w, and the interface of the epitaxial and the n^+ buried layers is denoted by x_1. V_j is the applied junction voltage and Φ_b is the barrier height.

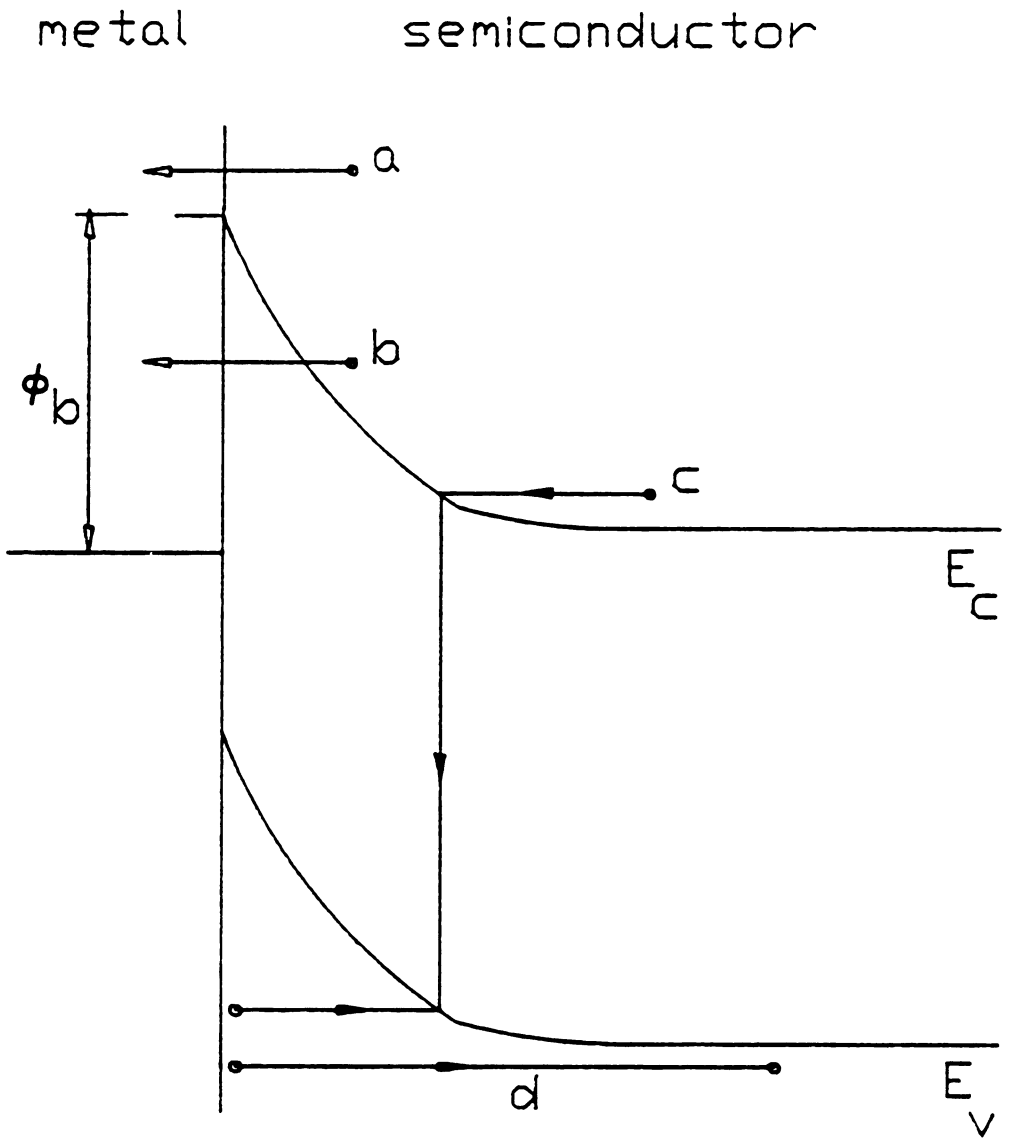


Figure 2-3 Current transport mechanisms over the metal semiconductor interface. (a) Thermionic emission. (b) Tunneling of majority carriers. (c) Recombination in the depletion region. (d) Minority carrier injection. Φ_b is the barrier height of the interface.

region of the device. The current-voltage relationship for the combined thermionic emission-diffusion process is developed by Crowell and Sze [6] and is given by

$$J = A^{**} T^2 \exp(-q\Phi_b/kT) \{\exp(qV_j/kT) - 1\} \qquad (2\text{-}1)$$

where J is the current density, A^{**} is the modified Richardson's constant, V_j is the junction voltage, and Φ_b is the barrier height of the diode as shown in Figure 2-3. In this work, Equation 2-1 is referred to as the ideal Schottky diode equation and the other processes of current transport shown in Figure 2-3 cause departures from this ideal behavior.

Quantum-mechanical tunneling of majority carriers through the barrier and carrier recombination in the depletion region are significant at low bias. Minority carrier injection, on the other hand, is significant at high injection and introduces additional delays in the switching response of the diode.

2.4 Effects of Minority Carrier Injection

Under forward bias, minority carriers are injected into the bulk of the semiconductor and travel for an average distance equal to their diffusion length before they recombine with electrons. For semiconductors with large diffusion lengths compared to the thickness of the epitaxial layer, such as silicon with a diffusion length on the order of tens to hundreds of micrometers, most of the minority carriers reach the cathode before being recombined. Therefore, minority carrier

injection leads to the presence of excess minority carriers throughout the bulk.

In a device that is heavily forward biased, the excess hole concentration in the bulk of the semiconductor can be substantially higher than the material's equilibrium concentration. These excess holes, in addition to the excess electrons stored in the bulk to maintain quasi charge neutrality, give rise to an increase in the the bulk conductivity σ. The increase in conductivity (or conductivity modulation), $\Delta\sigma$, is given by

$$\Delta\sigma = q(\mu_n \Delta n + \mu_p \Delta p) \qquad (2\text{-}2)$$

where Δn and Δp are excess electron and hole concentrations and μ_n and μ_p are electron and hole mobilities. Conductivity modulation results in a decrease of the resistance of the epitaxial layer. Therefore, the diode conducts a larger value of current for a given voltage compared to the case of no modulation.

The excess holes also affect the switching characteristics of the device. Upon rapid switching from forward to reverse bias, a reverse transient current, much larger than the diode's steady-state reverse current, flows to sweep the excess holes out of the device. Figure 2-4 shows the minority carrier profile in the bulk during the transition from forward to reverse bias, and the current through the diode, during the reverse-recovery for a semi-infinite device initially under low to moderate forward bias. As shown in this figure, for times t_0 to t_3, the reverse current remains relatively constant since the presence of minority carriers pins the junction voltage near its value prior to switching until the hole concentration at the edge of the space charge

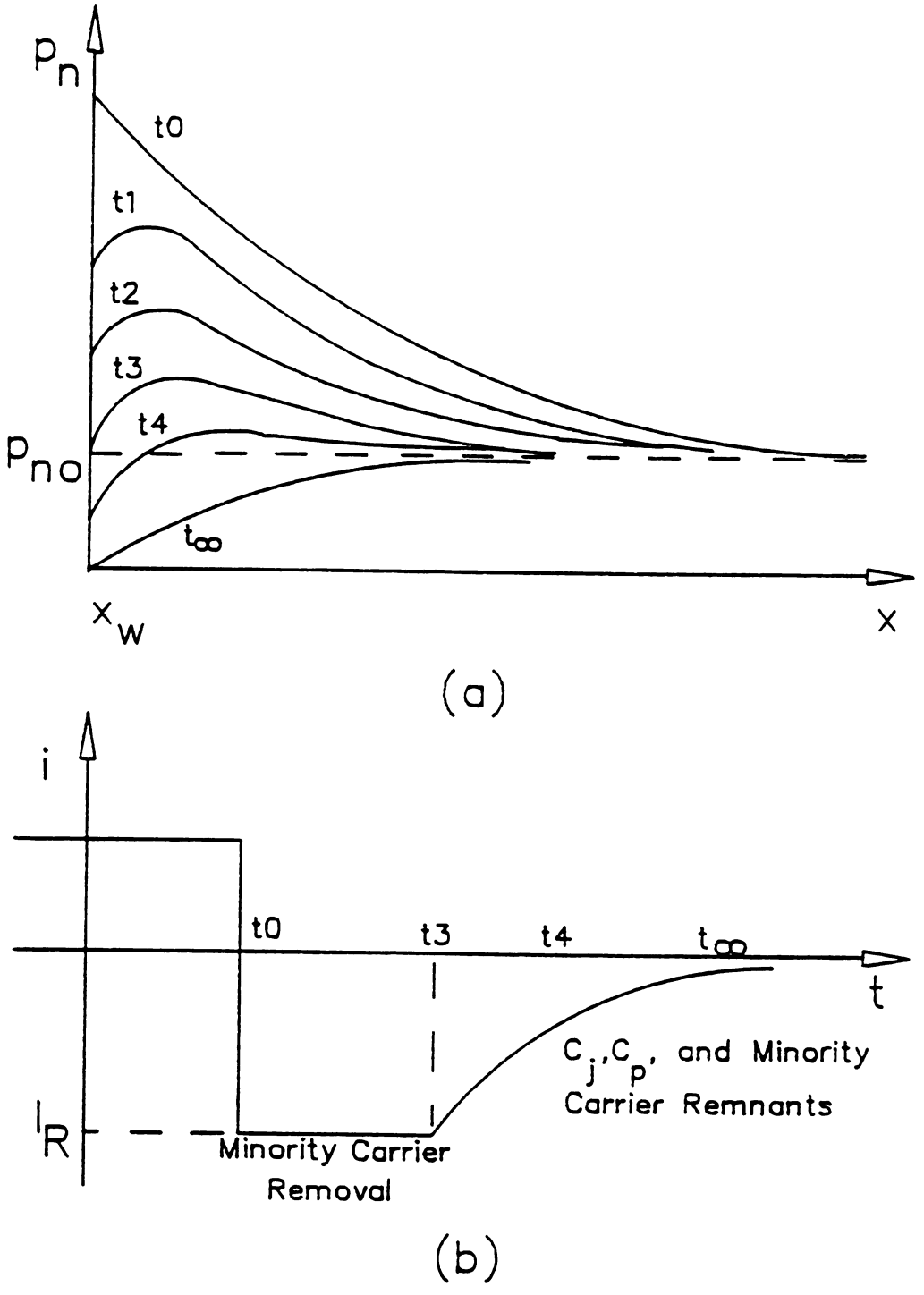


Figure 2-4 Dynamics of reverse-recovery for a semi-infinite device initially under low to moderate forward bias. (a) Hole concentration profile. (b) Switching current. C_j and C_p correspond to the junction and parasitic capacitances respectively.

region, x_w as shown in Figure 2-2, becomes small. The pinning is due to the boundary condition [7];

$$P_n(x_w) = P_{no}\exp(qV_j/kT) \tag{2-3}$$

where P_{no} is the equilibrium minority carrier concentration in the bulk. The primary source of reverse current during the exponential decay after t_3 in Figure 2-4 is the discharge of the junction and parasitic capacitances. Minority carrier removal, however, may also continue as the junction becomes reverse biased, as shown for time t_4.

The boundary condition of Equation 2-3 is based on the assumption that the minority carrier quasi-Fermi level at the edge of the depletion region, x_w, lines up with the metal Fermi level. This assumption is only valid at low to moderate injection levels and fails at high injection [8]. Additionally, the minority carrier profiles shown in Figure 2-4 correspond to a semi-infinite bulk. Therefore, the reverse-recovery response shown in this figure does not necessarily describe the exact switching behavior of a planar diode under high injection. As will be shown from switching measurements described in Chapter 3, however, the observed response is similar to that of Figure 2-4.

The value of reverse current upon switching (I_R as shown in Figure 2-4) is determined primarily by the equivalent resistance of the switching circuit as seen by the diode, as well as the final reverse voltage that the device reaches after switching. Therefore, I_R is independent of the amount of stored minority carriers. The effect of minority carrier storage is merely to lengthen the time involved in the reverse-recovery. Consequently, the time during which I_R is constant

(from t_0 to t_3 in Figure 2-4) is called the storage delay time and serves as a figure of merit for the amount of stored excess minority carriers.

2.5 Review of Previous Work on Minority Carrier Injection

2.5.1 Theory

Historically, the interest in minority carrier injection was initially focused on point contacts which were used as emitters in the early bipolar transistors. An example of the theoretical study of point contacts is the work by Braun and Henisch [9] who developed a closed form expression for the ratio of minority carrier current to the total current (minority carrier injection ratio). While the point contact is a good injector of minority carriers, the planar SBD shows much smaller values of minority carrier injection ratio. In 1965, Sharfetter analyzed the phenomenon in planar SBDs under steady-state dc bias and developed an expression for the minority carrier injection ratio in these devices [3]. The expression developed in his work for the excess minority carrier storage depends on the value of the recombination velocity for holes at the $n\text{-}n^+$ interface originally introduced by Gunn [10]. His analysis was limited to low injection conditions. Others, including Chuang [7,11], Green and Shewchun [12], Wagner [13], Masszi et. al. [14], and C.C. Yu [4] have extended the analysis to the higher injection levels as well.

Chuang [7] solves the one dimensional steady-state dc carrier transport equations analytically and develops implicit equations to calculate the total amount of minority carriers stored in the device.

The boundary conditions used to obtain the analytical solution, however, limit the results to moderate injection levels. His solution is based on the use of boundary conditions at the edge of the depletion region x_w, and the n-n^+ interface, x_1 (see Figure 2-2). In particular, he assumes a constant velocity, independent of the hole concentration, for holes at the n-n^+ interface, x_1. This assumption is also used by Sharfetter for low injection conditions [3]. At x_w, the boundary condition used in reference [7] is based on Equation 2-3. As discussed previously, this boundary condition is obtained by using the assumption that the quasi-Fermi level for holes is essentially the same as the metal's Fermi level. So, to the extent that the assumptions made to obtain these boundary conditions fail under high injection, Chuang's results are limited to moderate injection levels. In fact, in a recent publication [8], Chuang and Wagner reported that under high injection, the hole quasi-Fermi level is significantly lower than the metal's Fermi level. It must also be noted that the charge associated with the total excess minority carrier storage, Q_p, obtained from Chuang's equations, reflects the total charge between x_w and x_1 and does not include the depletion region or the n^+ region. In another paper [11], Chuang developed an analytical expression for the I-V characteristics of the planar SBD which was shown to give accurate results for current levels extending to high injection (up to 10^4 A/cm^2). That work, however, did not produce a solution for the amount of charge associated with the stored excess minority carriers.

Green and Shewchun [12] solve the one dimensional equations numerically, under both steady-state dc and small signal ac conditions. The dc solution is used to get the the total minority carrier stored charge, Q_p, and the ac solution is used to obtain a small signal

equivalent circuit model for the device. Their choice of device structure is somewhat different from what was previously discussed. Specifically, they do not have the n^+ buried layer in their analysis. In other words, the cathode ohmic contact is assumed to be directly connected to the epitaxial region (see Figures 2-1, 2-2). Their boundary condition for electron current at x_o is originally due to Crowell and Sze [6] and is based on the assumption that excess electrons at x_o travel to the metal with an average velocity equal to their thermal velocity. The boundary condition used by Green and Shewchun on hole current at x_o assumes that the above argument is true for holes at that point as well, and the boundary conditions applied at the ohmic contact assume no excess carriers there. The method presented by their work can be limited in two ways. First, by neglecting the n^+ region, the effects of the n-n^+ interface as well as the minority carrier storage in the n^+ region are not accounted for. Secondly, the boundary condition on hole current applied at x_o does not consider the effect of image force on the valence band which results in an energy gap shrinkage near the barrier and also leads to hole barrier height lowering and tunneling of holes through the barrier at high injection. The effect of image force on the valence band near the barrier will be discussed in detail in Chapter 4.

The numerical simulation described above was later used by Clark et. al. [15] to explain the difference between minority carrier injection behavior of point contacts and planar devices. A simulation similar to the work of Green and Shewchun was also used by Wagner [13] to develop a large signal model for the device. His model consists of ideal diodes, resistors, capacitors, and a constant current source and, since the model was developed to match the simulation results, the

limitations of the simulation as described above, apply to the model as well. Recent modifications of the numerical simulation include the work by C.C. Yu [4] who considered the n^+ region of the device and the work by Mosszi et. al. [14] who considered the effect of hole barrier lowering at high injection on the hole current boundary condition.

2.5.2 Experiment

Early experimental work on minority carrier injection in SBDs also focused on point contacts and is reviewed by Henisch [16] and Smith [17]. For example, the original Haynes-Shokley experiment studied hole injection from a metallic point rectifying-contact on n-type germanium [18].

Experimental observations of minority carrier induced conductivity modulation in planar epitaxial silicon SBDs have been reported in the literature. An example is the work by Jager and Koseak [19] on 45 μm diameter devices for current densities up to 10^3 A/cm^2. Also, metal emitter transistor structures have been used to measure minority carrier injection in planar silicon SBDs by Yu and Snow [20] and in GaAs SBDs by Chan et. al. [21].

Direct measurement of minority carrier storage in planar SBDs, based on the reverse-recovery experiment, has only been reported for low injection conditions (10 A/cm^2) by Sharfetter [3]. The technique involves the integration of the reverse-recovery current with respect to time to obtain the total charge removed from the device upon switching. Subsequent correction of the total charge for the charge associated with the parasitic and junction capacitances then yields the charge associated with the excess minority carriers. The difficulty of

this measurement is due to the fact that, unlike p-n junctions, planar SBDs are primarily majority carrier devices and minority carrier injection corresponds only to a small fraction of the total current flow. Consequently, reverse-recovery of the switching response usually lasts, at most, on the order of nanoseconds and hence, high time resolution circuits and test devices with low values of parasitic capacitance are required for such measurements. The reverse-recovery method is used in this work to measure the excess minority carrier storage in the device and will be explained in greater detail in Chapter 3.

Various methods have been used to measure the storage delay time in p-n junctions and, while the time scales of interest for SBDs may be small compared to p-n diodes, the same experimental methods are applicable in principle to SBDs. The most common and straightforward method is to switch the diode from forward to reverse bias and observe the diode current during the transient [22]. As discussed in section 2.4, the storage delay time corresponds to the time between t_0 and t_3 as shown in Figure 2-4. Various circuits reported in the literature for this type of measurement differ mainly in the circuits used to control the amplitude of the forward and reverse current upon switching [23,24,25]. This method has been used by Zetter and Cowly [26] for qualitative observations of minority carrier injection in SBDs.

Dean and Nuese [27] reported a "refined" step recovery method in which the switching diode is the terminating load on a single 50 Ω coaxial line of arbitrary length. The method involves the observation of the incident and reflected waveforms of a single transmitted pulse using a high impedance probe. During the storage delay time, the diode is highly conductive, and the reflection coefficient is negative. After

the storage delay time, the diode approaches an open circuit in an exponential fashion and the reflection coefficient approaches unity. Consequently, the reflected signal can be used to obtain the storage delay time. This method was used by Dean and Nuese to measure storage delay times on the order of nanoseconds in GaAs p-n junctions. An advantage of this method is that only one electrical line is required to contact the test diode. The one-port connection makes it easy to vary ambient conditions, such as temperature. A disadvantage is the requirement of a high impedance probe. The fastest sampling probes are 50Ω rather than high impedance.

A double pulse experiment has been used by Silver et. al. [28], to avoid confusion between true storage delay currents and displacement currents due to capacitance. The method is useful for special cases where displacement currents are usually large, but it was not reported to achieve very high time resolutions.

The last measurement method to be discussed here was developed by Krakauer [29]. Unlike the methods previously discussed, which observe the response of the diode to input pulses, this method excites the diode with a sinusoidal input. Figures 2-5 and 2-6 show SPICE simulation results of the response of a diode to sinusoidal excitation. Figure 2-5 shows the response of a device with purely capacitive charge storage corresponding to a linear reverse-recovery current. Figure 2-6, on the other hand, shows the response of a device in which some minority carrier storage is present. As shown in this figure, the reverse-recovery current due to excess minority carriers can easily be distinguished from the linear capacitive current. Krakauer developed an expression, for a figure of merit concerning the excess minority carrier storage in the device, which is related to the exciting

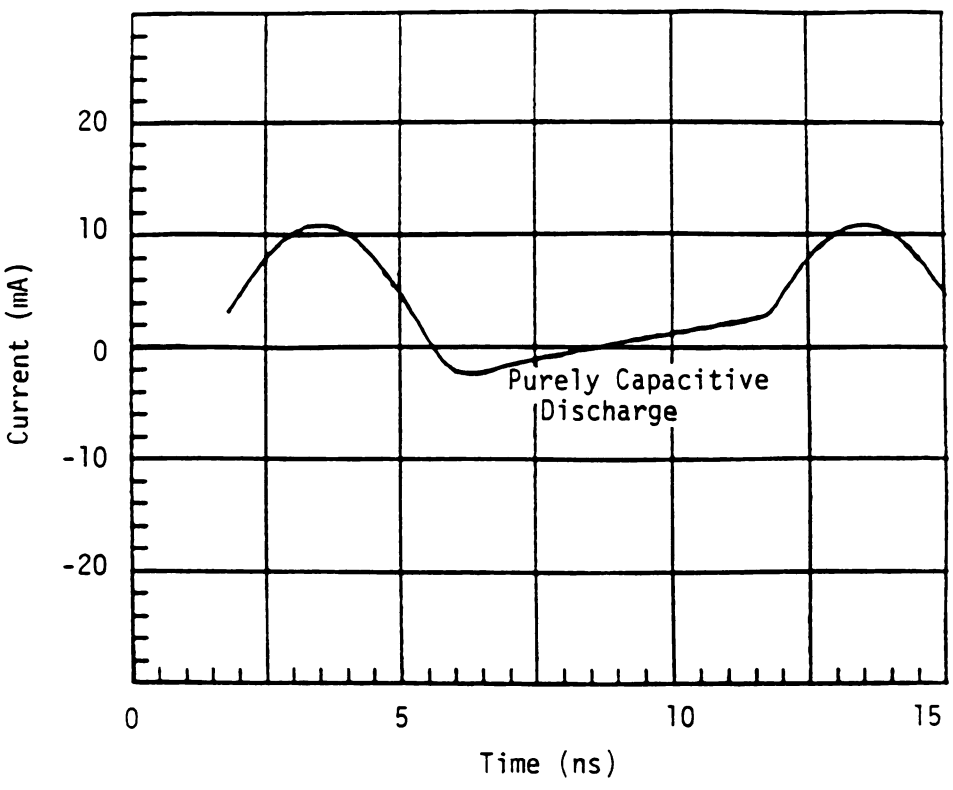


Figure 2-5 SPICE simulation results for the current through a diode excited by a sinusoidal signal when minority carrier storage is not present.

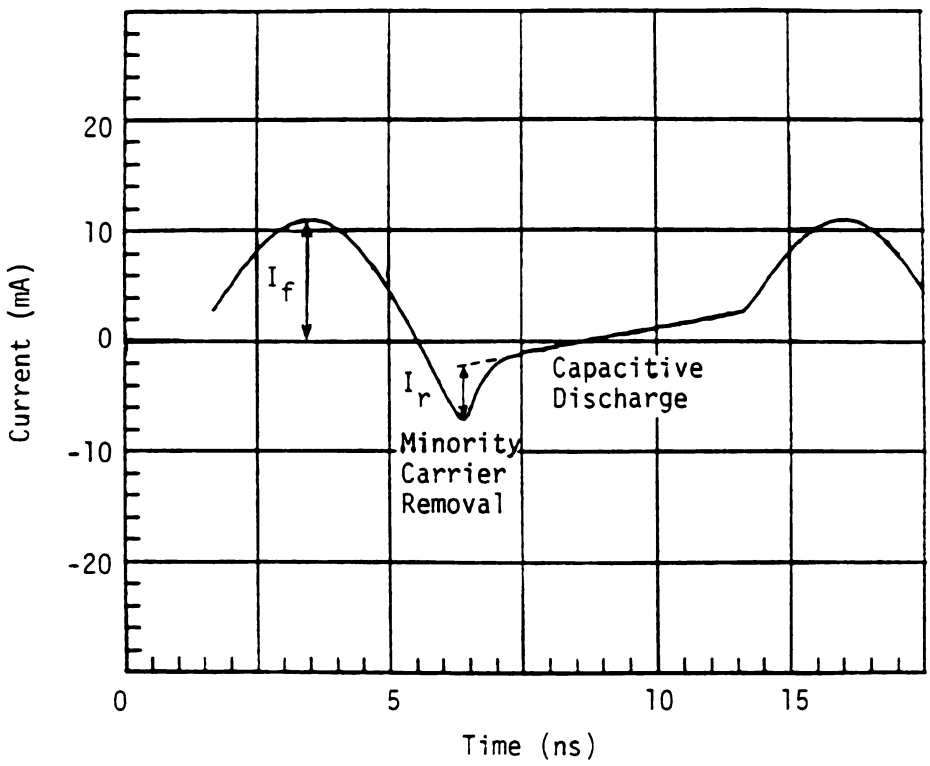


Figure 2-6 SPICE simulation results for the current through a diode excited by a sinusoidal signal when minority carrier storage in the diode is significant.

frequency, the voltage of the source, the impedances involved in the circuit, and the ratio of I_f to I_r as shown in Figure 2-6.

The advantages of this method are its ability to distinguish capacitive effects from excess carrier storage effects as well as the fact that the driving frequency need not be very high and, consequently, high time resolution measurement circuits are not needed. The method, however, is useful only for obtaining a figure of merit for minority carrier storage in the device and does not provide quantified information about stored charge, nor does it provide any information about conductivity modulation. Krakauer's method has been used in the literature for SBDs [30,31] as well as p-n diodes [32,33] and is also sometimes used by SBD manufacturers in their device specifications. In this study, as will be discussed in Chapter 3, the method is used for qualitative observations of the minority carrier storage phenomenon.

CHAPTER THREE

EXPERIMENT

3.1 Introduction

As previously discussed, the two major effects of minority carrier injection on SBD properties concern modification of the switching response of the diode and modification of the forward bias I-V characteristics. This chapter describes experiments which quantify both of these effects, and provide a basis of comparison with simulation.

For the switching experiment, the emphasis of both the experiment and simulation is on determining the total amount of stored excess carriers that are removed during the transient from forward to reverse bias. This is as opposed to determining the switching delay time, since there are problems with determining the delay time in both the experiment and simulation. Because of pulse noise and the effect of parasitic capacitance, an experimental determination of delay time is

to some degree subjective. Furthermore, delay time is a function of the test circuit. However, the fundamental cause of the delay time, which is the stored excess carriers, can be measured accurately and is not a function of the test circuit. For the simulation, a steady-state numerical solution provides values for the stored excess carriers but a time dependent solution, which is much more difficult to carry out, is required in order to obtain values for the delay time.

Therefore, the primary thrust of the switching measurements is to obtain values for the stored excess carrier charge, rather than switching delay times which result from the stored carriers. In the process of carrying out the experiments, approximate delay times are obtained but they do not form the basis of comparison with theory.

The effect of minority carrier injection on conductivity modulation is determined from the overall I-V characteristics which depend on junction characteristics as well as the characteristics of the series epitaxial layer. Direct comparison of the theoretically and experimentally determined I-V characteristics of the device provides the insight necessary to check the adequacy of the theory in treating the effects of conductivity modulation.

This chapter discusses experimental methods to measure the total excess carrier storage in the device for current densities extending to 10^5 A/cm^2 at several temperatures. The conductivity modulated J-V characteristics are also measured for current densities as high as $4x10^5$ A/cm^2. Results of such experiments are presented for unguarded and guarded devices. The primary emphasis of the work, however, is on unguarded devices in which injection over the metal-semiconductor interface is the only source of minority carriers.

3.2 Test Devices

All experimental data was obtained from planar platinum-silicide epitaxial test diodes provided by IBM. The test device in the experiment using Krakauer's method was unguarded and had an anode area of 30 μm^2. With that exception, the results reported here for unguarded devices are on devices with an anode area of 150 μm^2 and a 1 μm thick n-type epitaxial layer doped approximately at $2.5X10^{16} cm^{-3}$ and grown over an n^+ buried layer. The guarded SBD device area was 189 μm^2. Each test diode, along with several other types of test devices, is fabricated on a 0.15 cm^2 chip. Except for the Krakauer experiment, test devices had two pairs of available terminals, allowing four terminal measurements. Fig. 3-1 shows the top view of the metallization layout of the 150 μm^2 unguarded SBD and Fig. 3-2 shows the doping profile of silicon under the anode of that device.

3.3 Measurement of Minority Carrier Storage

3.3.1 Experimental Method

Before the excess minority carrier storage was measured, Krakauer's method, as described in Chapter 2, was used to obtain a qualitative knowledge of the current densities at which the phenomenon is significant in platinum-silicide SBDs. The sinusoidal signal which was used to excite the diode, had a frequency of about 50 MHz. Figure 3-3 shows the response of the diode for peak current values of 2.5×10^4 and 10^5 A/cm^2. As can be seen from this figure, for a peak current value of 2.5×10^4 A/cm^2, excess minority carrier storage is

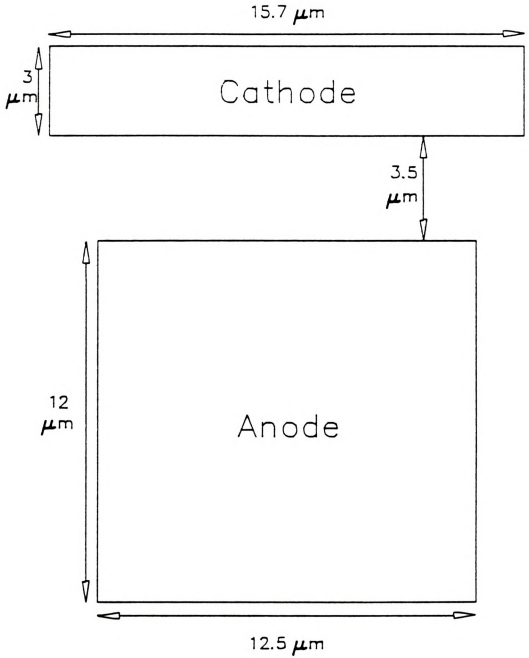


Figure 3-1 Metallization layout of the unguarded SBD.

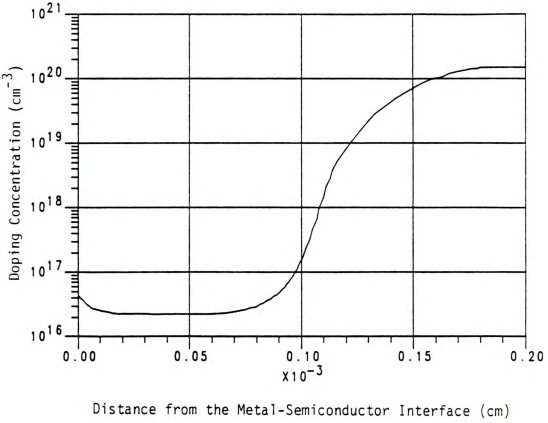
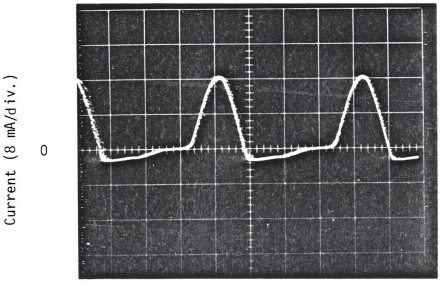


Figure 3-2 Doping profile of silicon under the anode of the SBD. Data from C.C. Yu [4].



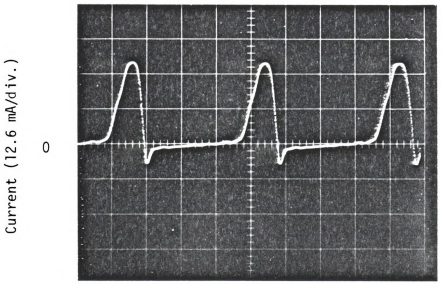


Figure 3-3 Response of a 30 μm^2 unguarded test device to sinusoidal excitation at room temperature. (a) Shows the response at a peak current density of 2.67 X 10^4 A/cm^2 and does not show a significant amount of minority carrier storage. (b) Shows the response at a peak current density of 10^5 A/cm^2 and evidence of minority carrier storage is clearly observed.

not observed while, for 10^5 A/cm^2, evidence of excess carrier storage is clear. It must be noted, however, that these values of current density, which correspond to sinusoidal excitation, do not relate directly to what would be expected from switching measurements which correspond to excess minority carrier storage under the quasi steady-state dc conditions that hold when the diode is pulsed into the forward bias state.

As previously discussed in Chapter 2, if an appreciable fraction of the forward bias current in the device is due to minority carriers, then upon rapid switching to reverse bias, a reverse current flows while the excess carriers stored in the quasi-neutral regions are being swept out. Integration of the reverse-recovery current yields the total charge removed from the diode. In order to determine the charge associated with stored minority carriers, the total charge obtained from the integration must be corrected for junction and parasitic capacitance stored charge. With this correction, current integration yields the charge associated with excess minority carriers stored in the device prior to switching provided that the lifetime of excess carriers is much larger than the reverse-recovery time such that excess carrier recombination is negligible during reverse-recovery.

The reverse-recovery currents to be measured last on the order of nano-seconds. Therefore, the test circuit must have a high time resolution. Special care must also be taken in mounting the sample in order to avoid any significant parasitic capacitance exterior to the device. The test circuit along with its equivalent circuit is shown in Fig. 3-4. A 10 ns wide pulse at 375 Hz is used to forward bias the device from a fixed reverse bias of -2 V. The low duty cycle of the pulse helps avoid self heating in the device at high current densities.

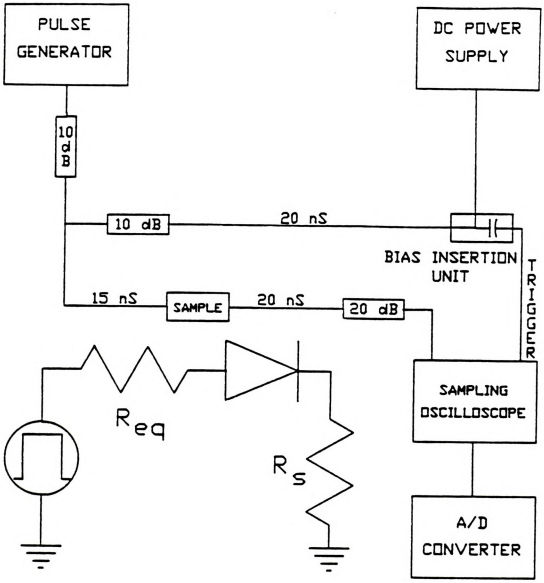


Figure 3-4 Diagram of the circuit for minority carrier charge storage measurement along with its equivalent circuit. R_{eq} denotes the equivalent resistance of the driving circuit and R_s corresponds to the input impedance of the sampling oscilloscope.

The reverse-recovery was observed on the falling edge of the pulse with a sampling oscilloscope and then digitized. The resulting fall time of the overall circuit was observed to be about 450 ps. Low-loss, low-dispersion coaxial cables with General Radio connectors were used for interconnections in the circuit. The length of the cables were chosen such that no reflections would arrive at the sampling oscilloscope while the step recovery was being observed. Additionally, the length of the cable going to the triggering input of the sampling oscilloscope was chosen such that sufficient delay for proper triggering was obtained. The coupling capacitor in the bias insertion unit provided the isolation of the oscilloscope's trigger input from the dc supply. Attenuators were used to improve impedance matching and to suppress reflections. The bare chip containing the diode was wire bonded in our laboratory and mounted in a modified General Radio coaxial sample insertion unit. The parasitics of the sample mount were observed to be negligible compared to the chip parasitics. To perform the experiment at elevated temperatures, the sample mount was heated using a hot plate controlled by a digital temperature controller which detected the sample temperature using an RTD (resistance temperature detector) sensor. Detailed information regarding the equipment used in each circuit, sample mounting, data collection, and test device integrity is provided in Appendix A.

3.3.2 Correction for the Parasitic Capacitance

At low forward bias, the minority carrier injection level in a planar device is negligible [3], as verified by the Krakauer experiment previously described, and the entire switching current is due to the

discharge of the junction capacitance and the parasitic capacitance. Therefore, integration of the low bias current waveform provides the means to correct for capacitive stored charge. Fig. 3-5 shows idealized waveforms of the reverse-recovery associated with the low injection, primarily capacitive case, and the high injection case which includes the discharge of minority carriers. If the dominant parasitic capacitance is in parallel with the junction capacitance of the diode, then the voltage across the capacitor remains relatively constant from low to high injection since the junction voltage of a forward biased diode does not change much with increasing current. Therefore, the reverse current upon switching remains approximately constant (i.e. $I_{2R} = I_{1R}$ in Fig. 1) since the initial conditions for discharge are approximately equal. Specifically,

$$I_{1R} \approx I_{2R} \approx (V_{jf} - V_r)/(R_{eq} + R_s) \qquad (3\text{-}1)$$

where V_{jf} is the voltage drop across the junction of the forward biased diode, V_r is the reverse bias voltage, and R_{eq} and R_s are the circuit's equivalent resistors as shown in Figure 3-4. In this case, integration of the low injection waveform provides a constant charge to be subtracted from high injection charge integrations. If, on the other hand, the voltage across the dominant parasitic capacitance changes considerably, then I_R increases as the forward bias level increases (i.e. $I_{2R} > I_{1R}$) and the low bias capacitive charge must be multiplied by I_{2R}/I_{1R} before being subtracted from the high injection charge integration. For the device in this study, I_R was observed to remain relatively constant as forward bias changed and the low injection

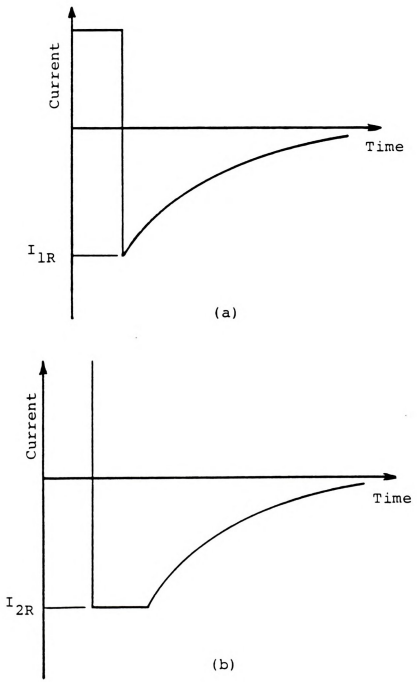


Figure 3-5 Idealized reverse-recovery waveforms. (a) Corresponds to a purely capacitive response while (b) shows the minority carrier induced switching delay.

waveform integration was used as a constant correction to charge integrations.

3.3.3 Experimental Limits and Accuracy

Experimental conditions were varied to check the validity of the measurement technique. To verify that during the 10 ns of forward current the diode does reach its steady-state conditions, reverse-recovery after a 14 ns wide pulse was observed and found to be the same as results associated with the 10 ns wide pulse. Also, if the effect of parasitic capacitance is subtracted correctly, then results obtained for minority carrier storage should be independent of the dc reverse bias. To verify this, the experiment was performed using higher values of reverse voltage and agreement with the -2 V results was observed.

As discussed previously, if the excess carrier lifetime is not much larger than the reverse-recovery time, then some of the excess carriers recombine before they can be swept out in the reverse-recovery and they are not observed in the experiment. The lifetimes associated with trap assisted recombination are on the order of μs. Therefore, trap assisted recombination is insignificant during the reverse-recovery. The Auger recombination lifetime, on the other hand, is inversely proportional to the square of carrier density and reaches values on the order of a fraction of a ns as the carrier concentration reaches 10^{20} cm^{-3}.

As will be shown later in Chapter 6, for the bias range of interest, the concentration of excess carriers in the device does not reach high enough values for Auger recombination to be significant during reverse-recovery in the lightly doped epitaxial region. In the

n^+ region, however, the doping density reaches values in excess of 10^{20} cm^{-3} and therefore, some of the excess carriers stored in the n^+ region recombine before they are swept out in reverse-recovery. It will be shown in Chapter 6 that an upper bound on this effect can be determined from the simulation.

The upper limit on the applied forward current was essentially imposed by the pulse generator. While the generator used in the experiment was capable of supplying more current than the maximum value of current reported here, in other words beyond 10^5 A/cm^2, the falling edge of the pulse was too noisy and the desired time resolution could not be obtained. The test equipment was checked for proper calibration and did not contribute significant error to the data. The primary source of error was found to be due to the possibility of minority carrier discharge during the fall time of the pulse. Considering all sources of error, the reverse-recovery charge integration results are considered to have less than 5% error over most of the bias range. Measuring the temperature of the sample using two independent probes confirmed the accuracy of the temperature measurements to within one degree Celsius.

3.3.4 Minority Carrier Storage Results

Typical reverse-recovery currents observed at low and high injection are shown in Figures 3-6 and 3-7. Figure 3-6 shows the low injection capacitive discharge and Figure 3-7 shows the reverse-recovery when minority carrier injection is present. Figure 3-7 shows that while the bulk of minority carriers are removed in the first two nanoseconds after switching, there is a secondary discharge which lasts

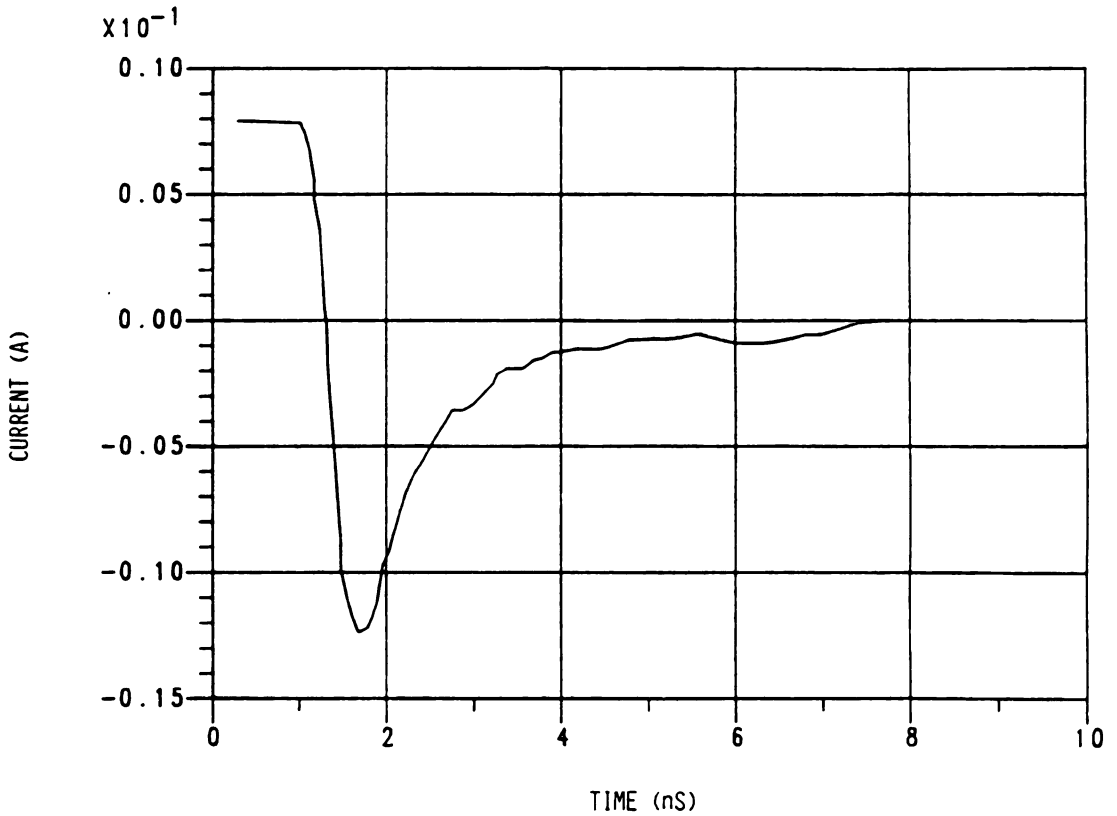


Figure 3-6 Measured reverse-recovery response of the unguarded test diode at room temperature, corresponding to a forward current density of 5.6×10^3 A/cm^2 prior to switching. The waveform shows that at this level of forward current density, the discharge is primarily capacitive.

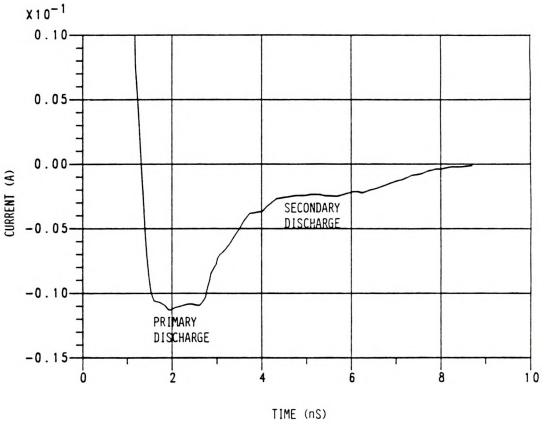


Figure 3-7 Measured reverse-recovery response of the unguarded test diode at room temperature, corresponding to a forward current density of 7 X 10^4 A/cm^2 prior to switching. Evidence of minority carrier storage is clear at this level of forward current density.

a few nanoseconds after the initial discharge. As shown in Figures 3-8 and 3-9, testing the device at higher forward currents and elevated temperatures shows that the reverse current during the secondary discharge increases with forward current density (Figure 3-8) as well as with temperature (Figure 3-9). This indicates that a significant portion of the secondary discharge is due to minority carriers.

Figure 3-10 shows the measured stored minority carrier charge for the unguarded SBD at 27, 85, 100, 125 °C for current densities up to about 10^5 A/cm^2. The data points in this figure represent averaged data from four devices. As would be expected, the minority carrier storage increases with temperature. Over the current range investigated, the minority carrier storage also increases with current density. Noting that the stored minority carrier density reaches values in excess of 10^{-5} coulombs/cm^2, if the reverse current densities during switching are on the order of 10^4 A/cm^2, as is the case for the measurement circuit, the discharge time required to remove the minority carriers is necessarily on the order of ns. Typical delay times associated with the primary discharge are on the order of one or two ns, and for this test circuit, the secondary discharge persists for an additional 4 to 6 ns.

Considerably larger values of stored minority carriers are found in guarded SBD's as shown in Figure 3-11. The p-type guard rings for these devices are electrically connected to the anode and therefore, the guard ring creates a p-n junction diode in parallel with the SBD. At high SBD forward bias conditions, the p-n junction turns on and injects additional minority carriers into the n-type epitaxial layer. In fact, significantly more minority carriers are injected from the guard ring than over the SBD metal-semiconductor interface as is shown in Figure 3-12 which compares minority carrier storage in guarded and

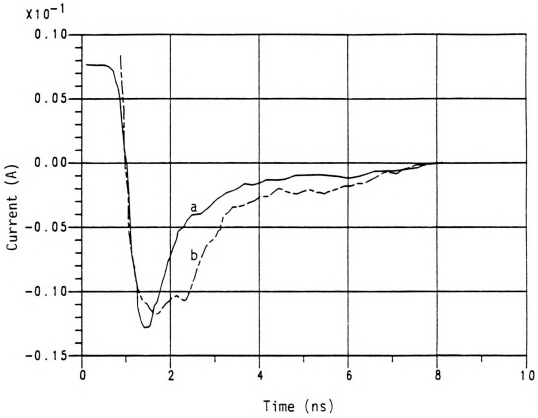


Figure 3-8 Measured reverse-recovery waveforms of the unguarded test diode at room temperature. Values of current density prior to switching are (a) 5.5 X 10^3 A/cm^2, and (b) 4.2 X 10^4 A/cm^2. This figure shows that the secondary discharge increases as forward current density increases.

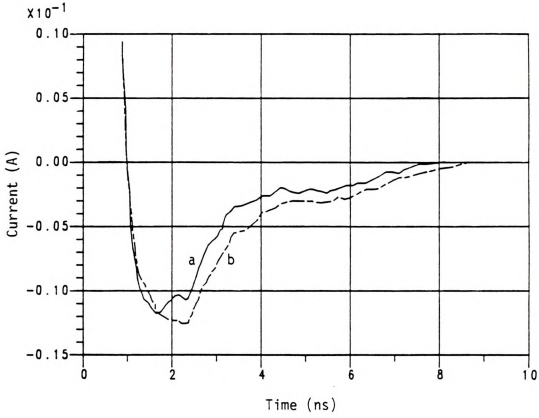


Figure 3-9 Measured reverse-recovery waveforms of the unguarded test diode corresponding to a current density of 4.2×10^4 A/cm^2 prior to switching. (a) Shows the response at 27 °C, and (b) shows the response at 125 °C. This figure shows that the secondary discharge increases as temperature increases.

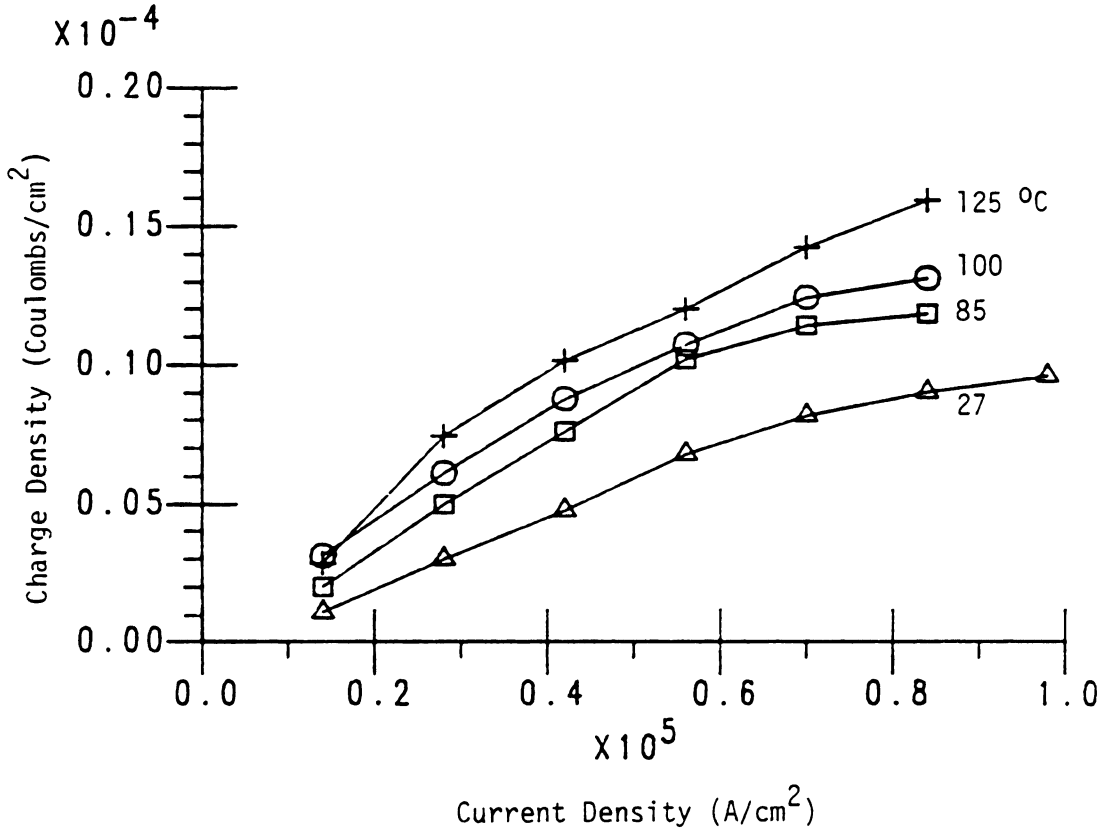


Figure 3-10 Measurement results for the charge density associated with stored excess minority carriers at four temperatures. The results correspond to average of the data obtained for four unguarded devices.

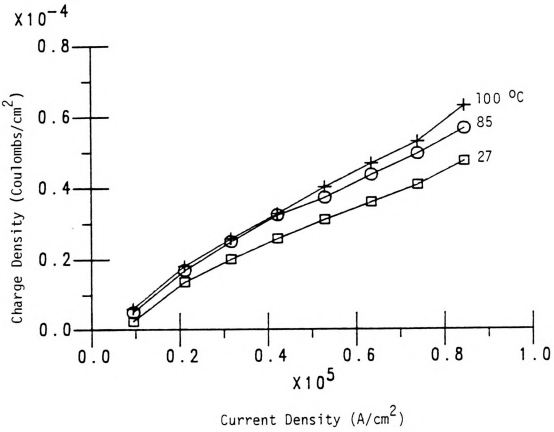


Figure 3-11 Measurement results for the charge density associated with stored excess minority carriers at three temperatures for a guarded device.

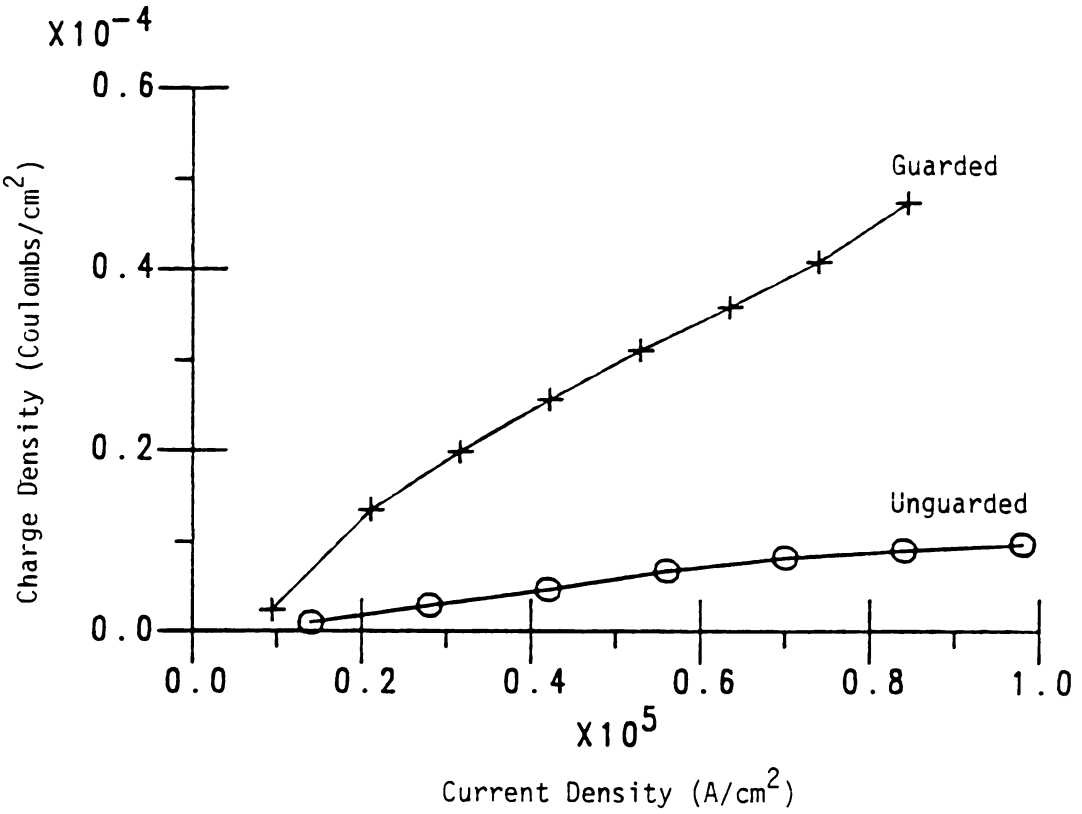


Figure 3-12 Comparison of room temperature results of the stored minority carrier charge density between guarded and unguarded devices.

unguarded devices. Figure 3-13 shows a typical high injection reverse-recovery of the guarded device. As seen in this figure, a large reverse-recovery current in these devices persists for several nanoseconds.

3.4 Measurement of Current-Voltage Characteristics

3.4.1 Experimental Method

The I-V measurement was done using a four terminal technique. Two forcing terminals were used to drive current through the device while the sensing terminals were used to measure the voltage across the device. At low currents (up to 1 mA), the measurement was dc while for the higher currents, 0.5 μs wide pulses with a 12 Hz repetition rate were used to avoid self-heating. An oven with controlled temperature was used to heat the sample for measurements at elevated temperatures. Figure 3-14 shows the measurement circuits at low and high bias. As shown in this figure, the low bias measurement involved the use of a curve-tracer for the bias supply as well as current measurement. The voltage was measured using a high input impedance multimeter.

The high bias measurement was performed by biasing the diode, in series with a 10Ω resistor, by a pulse generator. Two storage oscilloscopes were used to measure the current and voltage, and the oscilloscope monitoring the diode voltage was in the differential mode. The value of the loading resistor (10Ω), had to be chosen large enough so as not to load down the pulse generator, but yet small enough to keep the common voltage in the differential voltage measurement within the oscilloscope's requirements. The body of the oven was grounded to

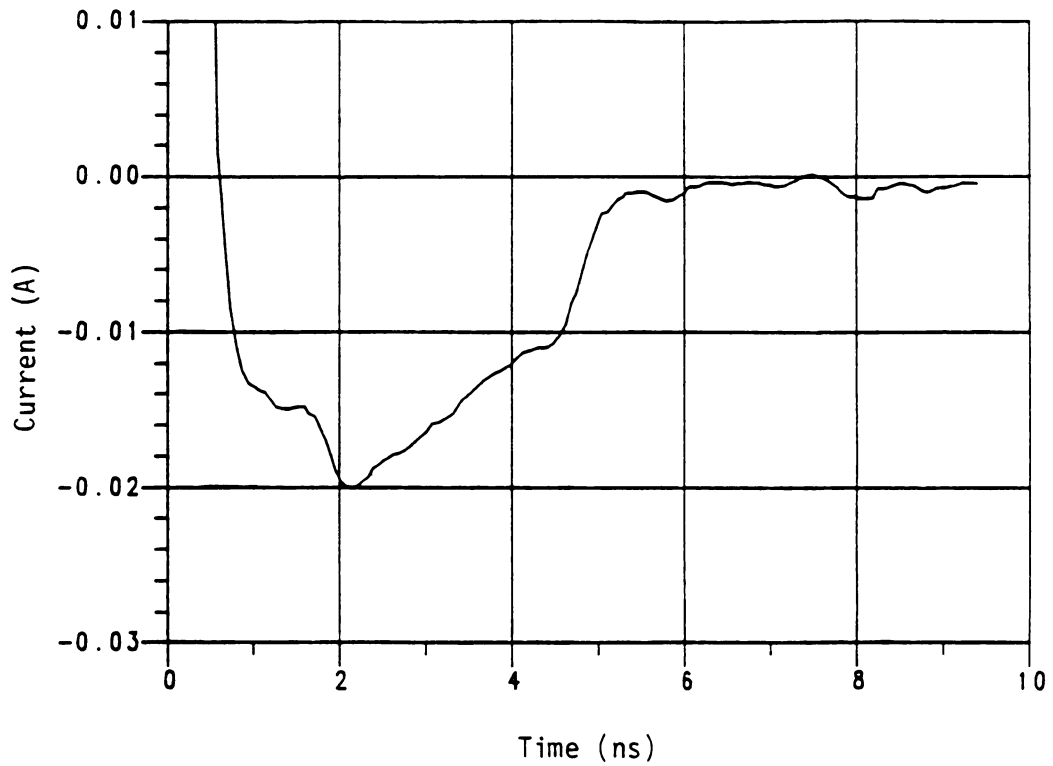
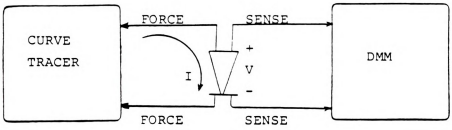
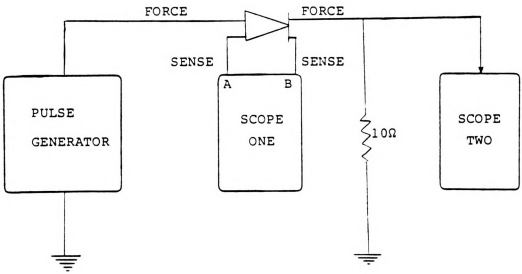


Figure 3-13 Switching response of a guarded diode at room temperature corresponding to a current density of 4.2 X 10^4 A/cm^2 prior to switching.



(a)



(b)

Figure 3-14 Current-voltage measurement circuits. (a) The low bias circuit; (b) the high bias circuit (above 1 mA).

provide shielding for the device against noise. Details about the equipment used in the measurement circuit are described in Appendix A.

3.4.2 Experimental Limits and Accuracy

Various instruments used in the measurement, were checked for proper calibration to minimize any instrument induced error. The low bias dc measurements were found to be quite reliable while, for high bias measurements, the reading from the oscilloscope trace was prone to some error due to the differential measurement technique and the uncertainties in reading data from a CRT scale. Special care was taken to ensure that the common voltage of the probes used in the differential voltage measurement was less than the maximum allowable value suggested by the oscilloscope manufacturer. Some error, due to a finite common mode rejection, however, is expected. The measured I-V data, is considered to have less than 1% error at low bias and less than 5% error at high bias. The temperature measurement accuracy for the I-V measurement is again accurate to one degree Celsius.

3.4.3 Current-Voltage Results

Current density vs. voltage at 27, 85, 100, and 125 °C for the unguarded SBDs are shown in Figure 3-15. At low currents, the semilogarithmic plots show the characteristic straight lines expected for diodes. At current densities above 10^3 A/cm^2, however, the series resistance of the epitaxial region becomes a dominant factor. Figure 3-16 shows a linear plot of the room temperature data to emphasize the high bias region. The expected J-V characteristics in the absence of

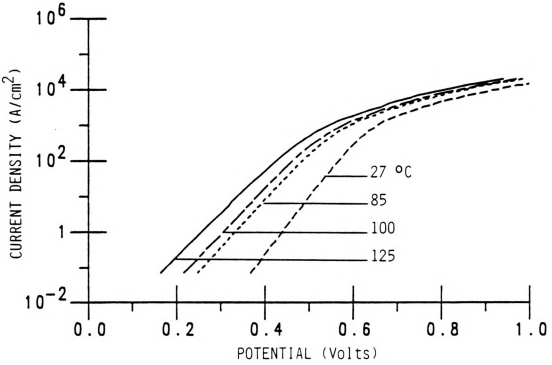


Figure 3-15 Measured J-V characteristics of an unguarded device at four temperatures.

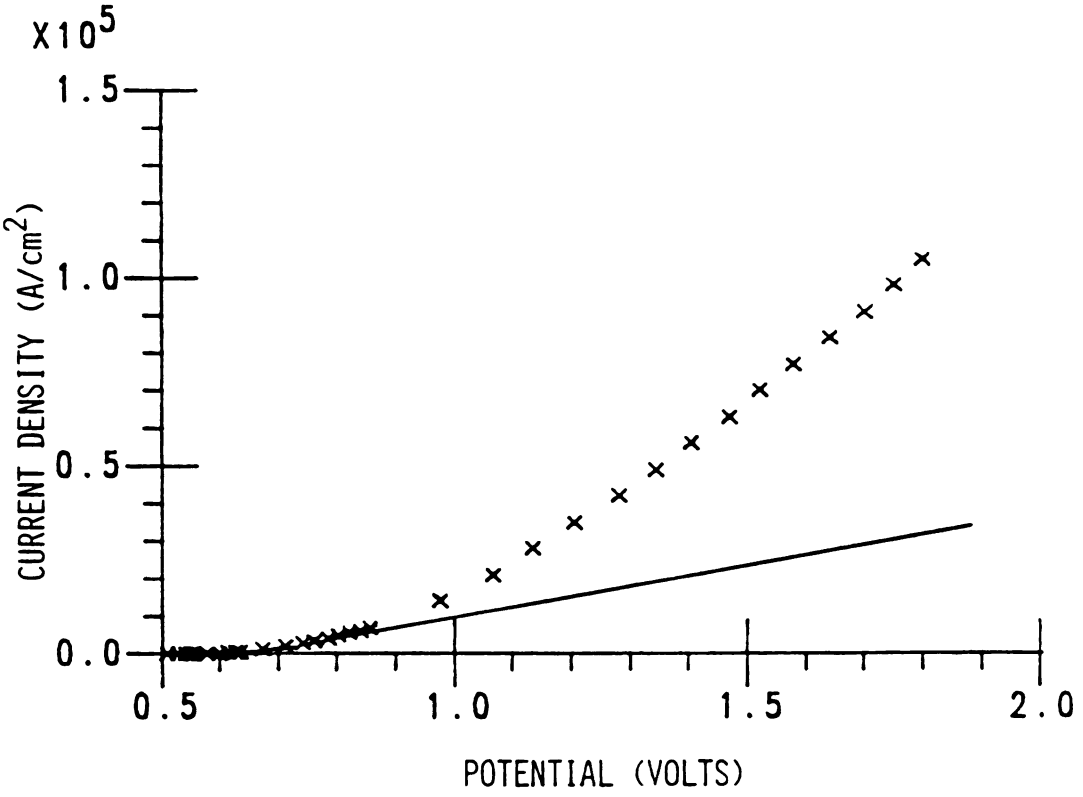


Figure 3-16 Linear plot of the room temperature J-V characteristics of the unguarded device emphasizing high current densities. (X) Shows the measured data points while the solid line shows the expected J-V characteristics in the absence of conductivity modulation.

bulk conductivity modulation is also shown in this figure to demonstrate the presence of conductivity modulation at the high bias levels. Figure 3-17 shows the current density vs. voltage measured for the guarded device at 27, 85, and 100 °C, and the same type of behavior is observed.

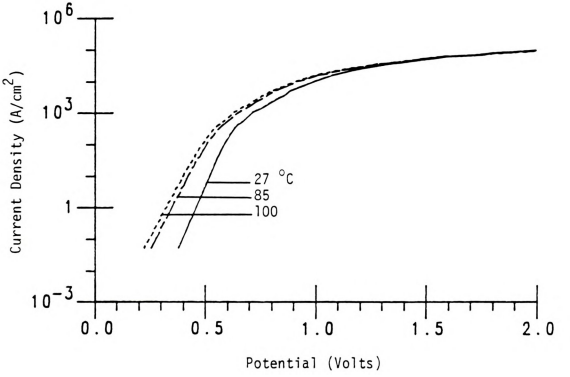


Figure 3-17 Measured J-V characteristics of a guarded device at three temperatures.

CHAPTER FOUR

THEORETICAL SIMULATION

4.1 Introduction

The SBD is analyzed theoretically by solving the basic equations governing carrier transport in the device. In their most general form, these equations form a set of non-linear partial differential equations. However, the phenomena of interest in this study (i.e. stored minority carriers and conductivity modulation) correspond to the forward bias dc steady-state condition under which the equations are ordinary for a one dimensional analysis.

This chapter first discusses the basic theory of carrier transport in the device. Then, the approach to the solution of the problem by previous investigations is discussed and finally, other phenomena beyond the previous work are explored and new corrections are made to the traditional boundary conditions. Specifically, hole barrier height

lowering, energy gap shrinkage, tunneling through the barrier, band-to-band tunneling, impact ionization, Auger recombination and lateral voltage drop are considered. In guarded structures, guard rings are additional sources of minority carriers. However, only unguarded structures are considered by the simulation. The equations are solved numerically by C.C. Yu [4] at IBM using a simulation program developed by Yu. The contributions of this thesis to the simulation are concerned with the inclusion of several corrections to the traditional theory, which is described in the following section.

4.2 Basic Theory

4.2.1 Basic Equations

The basic macroscopic equations governing carrier transport in the semiconductor are as follows.

$$\vec{E} = -\nabla\phi \qquad (4\text{-}1)$$

$$\nabla.\vec{E} = q/\epsilon\,[p - n + N_D - N_A] \qquad \text{Gauss's law} \quad (4\text{-}2)$$

$$\vec{J}_p = q\mu_p p\vec{E} - qD_p\nabla p \qquad \text{Hole current density equation} \quad (4\text{-}3)$$

$$\vec{J}_n = q\mu_n n\vec{E} + qD_n\nabla n \qquad \text{Electron current density equation} \quad (4\text{-}4)$$

$$\nabla.\vec{J}_p = q\,[G_p - R_p - dp/dt] \qquad \text{Hole continuity equation} \quad (4\text{-}5)$$

$$\nabla.\vec{J}_n = -q\,[G_n - R_n - dn/dt] \qquad \text{Electron continuity equation} \quad (4\text{-}6)$$

where the scalar potential ϕ, electric field $\vec{E}$, electron concentration n, hole concentration p, electron current density $\vec{J}_n$, and hole current density $\vec{J}_p$ are the unknowns. N_D and N_A are the donor and acceptor concentrations, μ_n and μ_p are electron and hole mobilities, D_n and D_p are electron and hole diffusion coefficients, G_n and G_p are electron and hole generation rates and R_n and R_p are electron and hole recombination rates.

These six equations form a set of partial, nonlinear, first order differential equations. In addition to the nonlinear terms of Equations 4-3 and 4-4, the electron and hole recombination rates in Equations 4-5 and 4-6 are usually nonlinear functions of the electron and hole concentrations.

As previously discussed, the phenomena of interest in this study (i.e. stored minority carriers and conductivity modulation) correspond to the forward bias dc steady-state condition. Additionally, if the dimensions of the anode of the device are much larger than the epitaxial layer thickness (such as the IBM devices under study), then edge effects are small and hence, a one dimensional solution is a good approximation of the device behavior provided that the lateral current flow in the n^+ buried layer is considered properly.

Under steady-state conditions, the carrier concentrations have zero time derivatives. Additionally, generation and recombination of holes and electrons happen in pairs. Therefore,

$$G_n = G_p = G \quad \text{and} \quad R_n = R_p = R \ .$$

Incorporating these modifications along with the one dimensional approximation simplifies the differential equations to an ordinary set as shown below.

$$E = - d\phi/dx \tag{4-7}$$

$$dE/dx = q/\epsilon \, [p - n + N_D - N_A] \tag{4-8}$$

$$J_p = q\mu_p pE - qD_p dp/dx \tag{4-9}$$

$$J_n = q\mu_n nE + qD_n dn/dx \tag{4-10}$$

$$dJ_p/dx = q[G - R] \tag{4-11}$$

$$dJ_n/dx = -q[G - R] \tag{4-12}$$

Solution of these equations requires appropriate boundary conditions and expressions for G and R, as is discussed in the following sections.

4.2.2 Carrier Generation

In the absence of external effects such as incoming photons, band-to-band tunneling and impact ionization are the two principle mechanisms for carrier generation in the semiconductor. When the electric field in the semiconductor is increased above a certain value, the carriers gain enough energy so that they can excite electron-hole pairs by impact ionization. The electron-hole pair generation rate G_i from impact ionization is given by

$$G_i = \alpha_n n v_n + \alpha_p p v_p \qquad (4\text{-}13)$$

where α_n is the electron ionization rate defined as the number of electron-hole pairs generated by an electron per unit distance traveled. Similarly, α_p is the analogous ionization rate for holes. Also, v_n and v_p are electron and hole drift velocities respectively [34]. The values of ionization rate increase at higher electric fields and decrease with increasing temperature. In silicon at room temperature, as the electric field increases from 2 X 10^5 to 10^6 V/cm, experimental values of α_n increase from about 1.5 X 10^3 to 1.5 X 10^5 cm^{-1} and α_p increases from 35 to 10^5 cm^{-1}[34].

Band-to-band tunneling also takes place at high electric fields (on the order of 10^6 V/cm)[34]. The process involves the quantum tunneling of electrons from the valance band into the conduction band (i.e. generation of electron-hole pairs). The generation rate resulting from this phenomenon is usually smaller than that of impact ionization with the exception of the case when a very large electric field exists over a very short distance (such as the case of heavily doped p-n junctions).

4.2.3 Carrier Recombination

In the absence of a significant amount of 'hot' carriers, the different mechanisms responsible for carrier recombination can be classified into two categories. The first category involves a direct decay of electrons from an energy level near the bottom of the conduction band to an energy level near the top of the valence band. Such a decay may be radiative, generating a photon in the process or,

may be carrier assisted with the lost energy going to the assisting carrier (Auger recombination). The second category is trap assisted recombination which involves a decay from the bottom of the conduction band to the top of the valence band via one or more energy levels in the bandgap created due to donor or acceptor impurities, deep level impurities, or crystal defects [34].

In silicon, the radiative direct decay is negligible since the material has an indirect energy gap. As a result, phonons are required to conserve crystal momentum. and the lifetime associated with such a process is very long, on the order of one second. The Auger recombination, however, may be significant in the presence of a large density of carriers in a heavily doped region of the material, or under extreme non-equilibrium conditions in a moderately doped material. The Auger recombination rate, R_A, is given by;

$$R_A = g(np^2 + pn^2) \tag{4-14}$$

Where, the Auger coefficient g, has a value on the order of 10^{-31} cm^6/S [34].

Trap-assisted recombination is the dominant recombination mechanism in silicon for low to moderate carrier densities. This process can be modeled by the Shockley-Read-Hall theory which is based on a single trap level [34]. The trap-assisted recombination rate, R_t, is given by;

$$R_t = (pn - n_i^2)/[\tau_p(n + n_i) + \tau_n(p + n_i)] \tag{4-15}$$

where τ_p and τ_n are the equilibrium hole and electron lifetimes and n_i is the intrinsic carrier concentration. The lifetimes associated with this recombination process are on the order of μs resulting in diffusion lengthes on the order of mm. Comparing the device dimensions (order of μm) with the diffusion length shows that trap-assisted recombination is not very significant for our analysis. The total recombination rate, R, is the sum of R_t and R_A.

4.2.4 Traditional Boundary Conditions

Ohmic contact boundary conditions are usually imposed at the $n\text{-}n^+$ interface [12,13,14] with the justification that the voltage drop across the n^+ region is negligible, due to the low resistivity of the n^+ material, and that the excess carrier storage is insignificant there. These boundary conditions are

$$p=p_o \quad \text{and} \quad n=n_o \tag{4-16-a,b}$$

where p_o and n_o are the equilibrium hole and electron concentrations.

Boundary conditions on current densities, applied at the junction, are that the electron current density at the juction is given by

$$J_n = q\,(n - n_o)\,v_n \tag{4-17}$$

where v_n is the thermal velocity of electrons. Similarly,

$$J_p = -q\,(p - p_o)\,v_p \tag{4-18}$$

where v_p is the thermal velocity of holes. The boundary condition on electron current density was originally introduced in a single carrier analytical solution of the device characteristics [6] and was later extended to holes and used in numerical simulations [4,12,13,14]. Equation 4-17 implies that any conduction band electron at the junction travels to the metal freely and that the average velocity for this process is the carriers' thermal velocity.

The remaining two boundary conditions are the values of semiconductor potential at the cathode and at the junction. Namely, the cathode potential is zero and the potential at the junction is given by

$$\phi(0) = V - q\,(\Phi_b - \Delta\Phi(V)) \qquad (4\text{-}19)$$

where Φ_b is the barrier height of the junction, $\Delta\Phi$ is the image-force induced barrier lowering, and V is the applied bias. Equation 4-19 is based on the assumption that the semiconductor near the cathode is degenerately doped such that the Fermi energy is approximately at the edge of the conduction band.

4.3 The Effect of Image-Force on Boundary Conditions

4.3.1 Energy Bands Near the Barrier

The image-force is an attractive force induced on a charged particle near a metal surface. This force results in lowering of the potential energy for charge carrier emission when an electric field is applied (Schottky effect) [34]. Considering an n-type semiconductor, the effect of image potential on the conduction band, which results in

the lowering of the electron barrier height, is widely accepted and used in the literature to analyze Schottky barrier characteristics. Consideration of the corresponding effect on the valence band is due to Inkson [35,36] who noted that the combination of the image potential effect on both bands indicates a collapse of the bandgap very close to metal surface. Although some spectroscopy results have been interpreted as supporting Inkson in a qualitative fashion [37,38,39], this theory applies macroscopic relations to microscopic dimensions and therefore, may not be valid very close to the junction [38,39]. As will be shown later, however, the point of interest where the junction boundary conditions are applied is several atomic layers away from the actual interface and the macroscopic relations are valid. In what follows, the effect of image-force on the bands is considered under low bias before flat-band condition and under high bias beyond flat-band.

4.3.2 Low Bias Condition

Under bias conditions below flat-band, the image potential causes a peak in the conduction band near the barrier as shown in Figure 4-1. The position of the peak, x_m, is effectively the starting point of the simulation which, as discussed previously, is several atomic layers away from the junction. As a result of the electron image potential, the barrier height of the junction, Φ_b, is reduced by the barrier height lowering $\Delta\Phi$. The point x_m is located close enough to the junction that the conduction band, excluding the effect of the image potential, can be approximated to be linear as shown by the dashed line labeled qEx in Figure 4-1. As a result of this approximation, the position of x_m coincides with where qEx and the energy due to electron

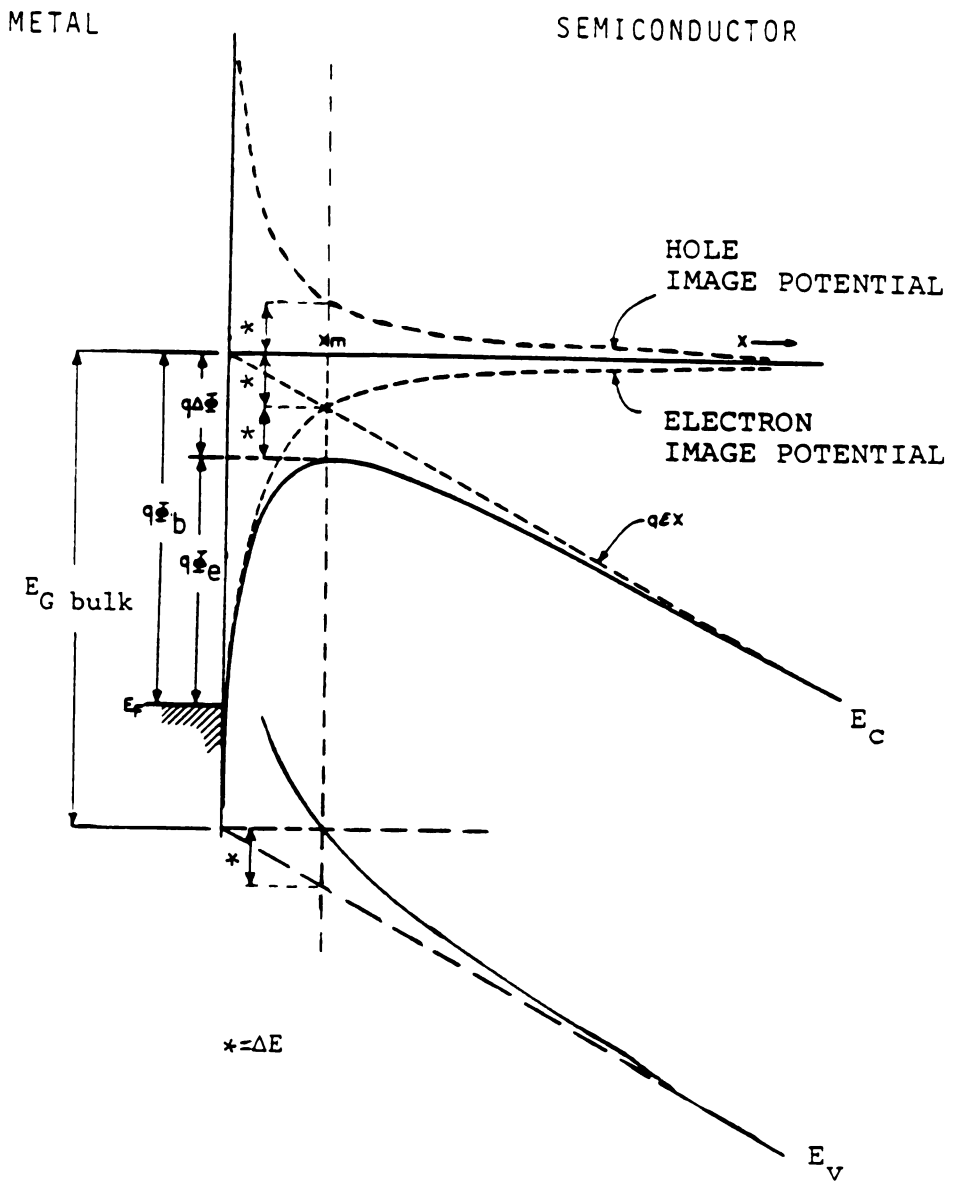


Figure 4-1 Energy band diagram of the device near the metal-semiconductor interface under low bias conditions. Φ_b is the barrier height excluding the effect of barrier lowering, Φ_e is the effective barrier height which includes the effect of barrier lowering, $\Delta\Phi$ is the barrier lowering potential, and $E_{G\ bulk}$ is the energy gap of the bulk semiconductor.

image potential intersect as shown in the Figure. Using this fact and the symmetry between the electron and hole image potentials, it is concluded that the four energy differentials labeled as ΔE in Figure 4-1 are all equal and have a value equal to $q\Delta\Phi/2$. Note that for the valence band, the hole image-potential is positive and the band bends up at the interface.

From a quantum mechanical point of view, the distortion in the bands near the interface results because the correlation energy of an electron in the semiconductor changes as one goes toward the metal. Consider an electron in the bulk semiconductor. It repels the other electrons away from it, leaving a hole in the electron sea. The potential gain from this correlation effect is an important part of the potential energy of the electron. Near the interface, however, the metal alters the correlation potential. Inkson has taken this into account in calculating corrected one-electron quantum wave functions. His results support the concept of opposite image potential signs for the conduction and valence bands and a shrinking gap.

Referring to Figure 4-1 it can be concluded that the energy difference between the metal Fermi level and the valence band at x_m is equal to the difference of the two energy levels at the junction in the absence of image potential. In other words, at equilibrium where the Fermi energy of the metal and the semiconductor line up,

$$E_f - E_v(x_m) = E_{G_{bulk}} - q\Phi_b \qquad (4\text{-}20)$$

where $E_{G_{bulk}}$ is the energy gap of in the bulk of the semiconductor. By inspection of Figure 4-1 it is also concluded that at equilibrium,

$$E_c(x_m) - E_f = q\Phi_b - q\Delta\Phi \qquad (4\text{-}21)$$

and that in general,

$$E_G(x_m) = E_{G_{bulk}} - 2\,\Delta E = E_{G_{bulk}} - q\,\Delta\Phi \qquad (4\text{-}22)$$

From Equation 4-22 it is concluded that the intrinsic carrier concentration at x_m, $n_i(x_m)$, is higher than that of the bulk by a factor of $\exp(q\Delta\Phi/2kT)$. As a consequence of this 'energy gap shrinkage', n_o and p_o used in Equations 4-17 and 4-18 to obtain boundary conditions on current densities are given by

$$n_o = N_c \exp(-q/kT\ (\Phi_b - \Delta\Phi)\ ) \qquad (4\text{-}23)$$

$$p_o = N_v \exp(-q/kT\ (E_{G_{bulk}} - \Phi_b)\ ) = [n_i^2\ /n_o]\ \exp(q\Delta\Phi/kT) \qquad (4\text{-}24)$$

where n_i is the bulk intrinsic carrier concentration and N_c and N_v are the conduction and valence band density of states.

4.3.3 High Bias Condition

As the applied bias increases beyond the flat-band condition, the sign of the electric field in the depletion region changes and the image potential energy results in a minimum in the valence band at x_m as shown in Figure 4-2. Using an analysis similar to that of the low bias case, at x_m as shown in this Figure,

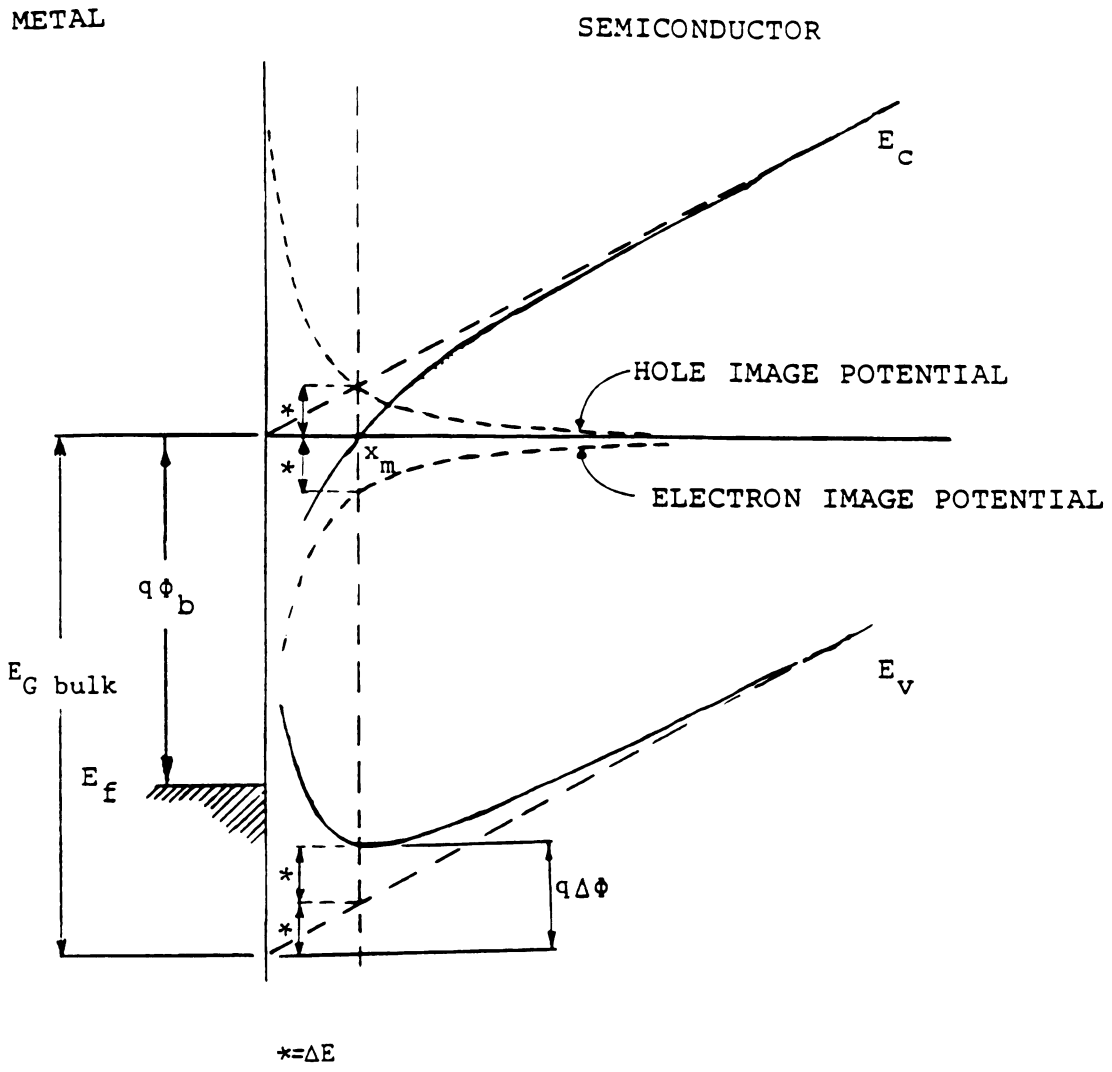


Figure 4-2 Energy band diagram of the device near the metal-semiconductor interface under high bias conditions (beyond flatband). Φ_b is the barrier height of the device, $\Delta\Phi$ is the hole barrier height lowering potential, and $E_{G\ bulk}$ is the energy gap of the bulk semiconductor.

$$E_c(x_m) - E_{f_{metal}} = q\Phi_b \tag{4-25}$$

$$E_{f_{metal}} - E_v(x_m) = E_{G_{bulk}} - q\Phi_b - q\Delta\Phi \tag{4-26}$$

$$E_G(x_m) = E_{G_{bulk}} - q\Delta\Phi \tag{4-27}$$

Consequently, under these conditions, n_o and p_o used in Equations 4-17 and 4-18 are given by

$$n_o = N_c \exp(-q\Phi_b/kT) \tag{4-28}$$

$$p_o = N_v \exp(-q/kT\ (E_{G_{bulk}} - \Phi_b - \Delta\Phi)\ ) = [n_i^2/n_o] \exp(q\Delta\Phi/kT) \tag{4-29}$$

The energy gap shrinkage in this case is identical to that of the low bias condition. The barrier height lowering, however, is a phenomenon related to the valence band and hence, effects the hole injection.

It is interesting to note that at x_m, $n >> n_o$ under forward bias (see Equation 4-17) while at large forward bias, in contrast, $p_o >> p$ (see Equation 4-18). Therefore, at large forward bias, the effect of hole barrier height lowering on p_o is far more significant in the hole current density boundary condition than the effect of the low bias electron barrier height lowering on n_o, in the electron current density boundary condition. Qualitative observations concerning a reversal of band bending and barrier height lowering for holes at high bias has been made by others [13,14,40].

4.4 Effect of Tunneling on Boundary Conditions

A source of current flow, in addition to the thermionic emission and diffusion mechanisms considered earlier, is tunneling through the barrier. From Figures 4-1 and 4-2, which correspond to n-type material, it is evident that tunneling of electrons through the conduction band barrier at low bias and that of holes through the valence band barrier at high bias could contribute to the total current. Since the tunneling current is higher for thinner barriers, the electron tunneling current is more significant for devices with higher doping of the semiconductor. The hole tunneling current, on the other hand, is more significant for a device with lower doping levels since the flat-band condition in such a device is reached at a lower value of forward bias.

The primary mechanism of forward current flow in moderately doped n-type SBDs is due to thermionic emission and diffusion of electrons. Therefore, the contribution of electron tunneling current is very small compared to the overall electron current. The phenomenon is most significant at very low bias where the barrier is narrow. The thermionic emission and diffusion induced hole current, on the other hand, is small and therefore, under very high bias where the hole barrier is sufficiently narrow, hole tunneling current could play a significant role in the overall hole injection and therefore, should be considered at such bias levels.

Analytical expressions for the electron tunneling current have been developed in the literature [41,42]. These treatments are applicable under low to moderate injection levels since they assume that the forward current is proportional to $\exp(qV_j/\eta kT)$, where V_j is the junction voltage, η is the ideality factor and k is Boltzmann's

constant. They use a parabolic approximation for the shape of the barrier which spans the space charge region and, which can be determined from the semiconductor doping density and the applied bias. In this section, an analytical expression for the hole tunneling current is developed. The expression depends on some of the simulation variables and therefore, may be used as a boundary condition in the simulation.

As discussed in the previous section, the hole barrier is formed under high bias beyond flat-band. Therefore the shape of the barrier can not be easily determined. To obtain an analytical expression for the hole tunneling current, however, it is desirable to approximate the shape of the barrier with a simple geometry. Triangular and parabolic geometries have been considered for treatment of band-to-band tunneling under high field conditions in the literature [34]. The triangular barrier approximation results in simpler expressions for the tunneling transmission coefficient than the parabolic approximation while the parabolic approximation is used to properly account for momentum transfer in tunneling mechanisms involving a change in carrier momentum. An example of such a process is band-to-band tunneling in indirect gap materials such as silicon.

The case under study here involves the tunneling of carriers within the same band over the barrier near the junction. Therefore, there is no change of momentum involved. A triangle as shown in Figure 4-3 is used to model the hole potential barrier. The tunneling transmission coefficient for such a barrier is given by [34]

$$T(\phi) = \exp\left((-\alpha m^{*1/2}/E) (\Phi_{bh} - \phi)^{3/2} \right) \qquad (4\text{-}30)$$

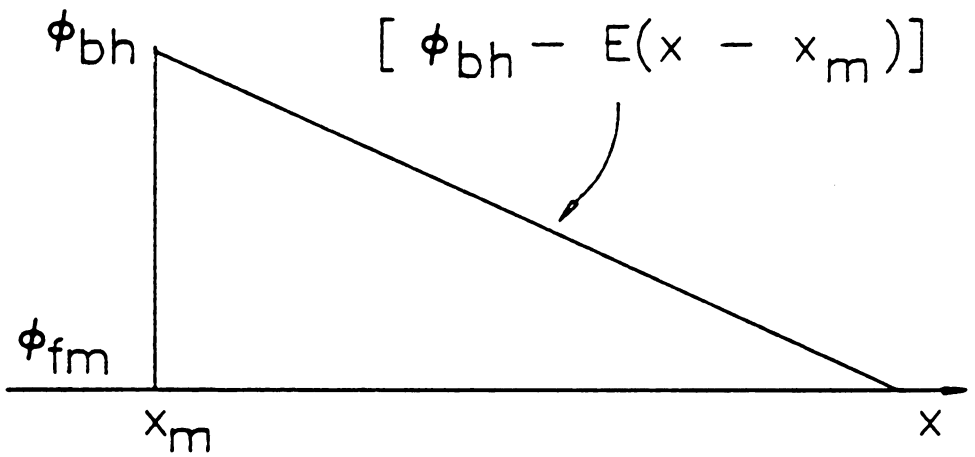


Figure 4-3 A triangular approximation of the potential barrier for holes at the metal-semiconductor interface under high bias conditions (beyond flatband). Φ_{fm} is the metal fermi potential, Φ_{bh} is the hole barrier height, E is the electric field in the semiconductor, and x is the distance from the interface.

where E is the electric field near the barrier, ϕ is the hole potential with respect to the potential at the metal Fermi level (note that q x ϕ is the hole energy taking E_{fm} as the zero reference energy), m^* is the hole relative effective mass, Φ_{bh} is the hole barrier height given by Equation 4-26 and α is given by

$$\alpha = \frac{4(2mq)^{1/2}}{3h} = 6.831 \times 10^7 \ V^{-1/2}.cm^{-1} \qquad (4\text{-}31)$$

where m is the mass of a free electron and h is the reduced Plank's constant.

The net hole tunneling current is obtained from the difference between the tunneling current from the metal to the semiconductor and the tunneling current from the semiconductor to metal and is given by

$$J_t = \frac{A^* qT}{k} \int_0^{\Phi_{bh}} F_m(\phi) \ [1 - F_s(\phi)] \ T(\phi) \ d\phi - \frac{A^* qT}{k} \int_0^{\Phi_{bh}} F_s(\phi) \ [1 - F_m(\phi)] \ T(\phi) \ d\phi \qquad (4\text{-}32)$$

where J_t is the net hole tunneling current density, $F_m(\phi)$ and $F_s(\phi)$ are the metal and semiconductor Fermi-Dirac distribution functions and A^* is the effective Richardson's constant [34]. In appendix B, it is shown that using Equation 4-30 for the tunneling transmission coefficient, the hole tunneling current density at x_m can be approximated by

$$J_t = A\,T^2\beta\,\exp(-\beta\Phi_{bh}) \int_0^{\Phi_{bh}} [\exp(\beta S) - p/p_o]\ X$$

$$\left\{ m_l^* \exp[(-\alpha m_l^{*1/2}/E)\,S^{3/2}] + m_h^* \exp[(-\alpha m_h^{*1/2}/E)\,S^{3/2}] \right\} dS \qquad (4\text{-}33)$$

where $\beta = q/kT$, m_l^* and m_h^* are the light and heavy hole relative effective masses, A is the Richardson's constant for a free electron ($A = 120\ A/K^2$), E is the electric field at x_m, p is the hole concentration (which varies with x, and therefore S, since $x = x_m + S/E$), and p_o is given by Equation 4-29. The tunneling current given by this equation can be added to Equation 4-18 to obtain a more complete boundary condition for the simulation.

4.5 Correction for the Lateral Voltage Drop

The one dimensional simulation discussed above assumes the voltage drop between the n^+ region and the cathode to be negligible. Under high forward-bias conditions, however, the voltage drop in the parasitic resistance between the cathode and the n^+ region, as well as the lateral voltage drop in the n^+ region, becomes significant. The lateral voltage drop, which causes the current density in the device to be non-uniform, can be considered by modeling the device as many narrow devices next to each other as shown in Figure 4-4. As shown in this figure, resistor R is the parasitic resistance from the n^+ region under the anode area to the cathode. The area under the anode is divided into m elemental diodes and the resistance of the n^+ region under each elemental diode is r. Figure 4-5 shows the equivalent circuit for this model. Knowing the doping concentration distribution in the device,

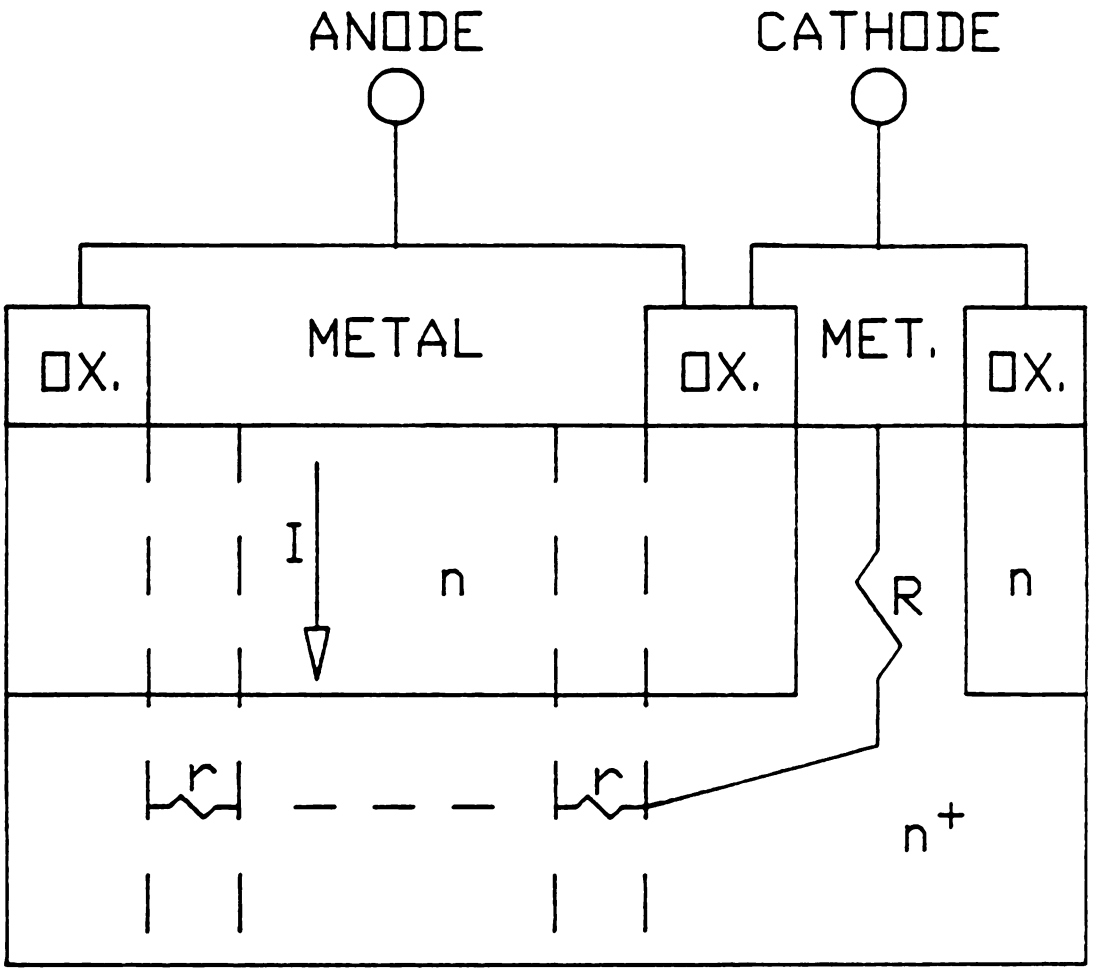


Figure 4-4 Cross section of the unguarded diode and the parasitic resistances involved, used as a model for the lateral resistance correction to the simulation.

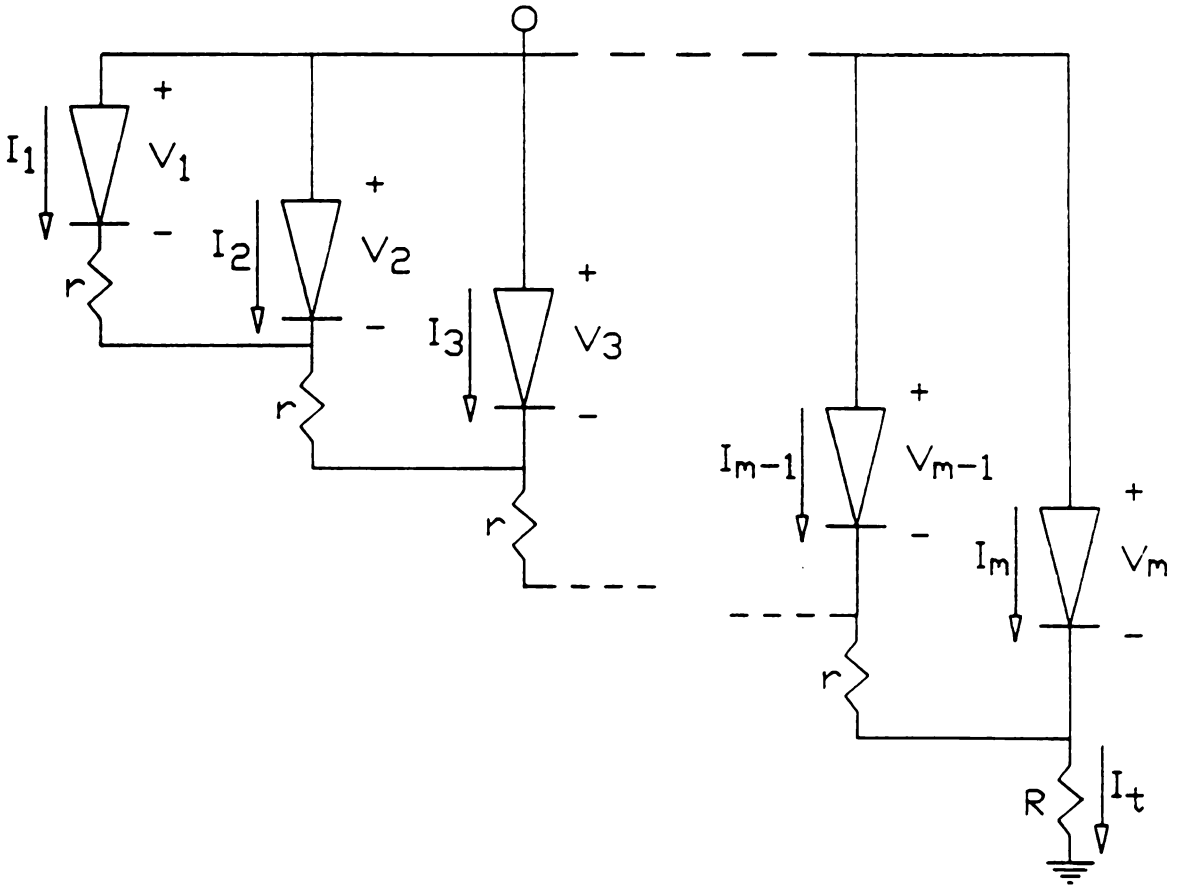


Figure 4-5 The diode equivalent circuit used to correct the lateral voltage drop in the n^+ buried layer.

values of R and r have been determined to be 4.2 Ω and (6/m) Ω respectively. Using the results of the one-dimensional simulation for the current voltage characteristics of each elemental diode in the equivalent circuit of Fig 4-5, the I-V characteristics of the overall device (V_t , I_t) can be calculated using the following algorithm.

$$V_1 + rI_1 = V_2$$

$$V_2 + r(I_1 + I_2) = V_3$$

$$*$$

$$*$$

$$*$$

$$V_{m-1} + r(I_1 + I_2 + \ldots + I_{m-1}) = V_m$$

$$V_m + RI_t = V_t$$

$$I_t = I_1 + I_2 + \ldots + I_m$$

Knowing the current density and the corresponding excess carrier storage in each elemental diode, the total amount of stored minority carriers vs. forward current can be calculated as well.

As long as the current flow in the area between the boundaries used in the simulation is in a vertical direction (i.e. in the direction shown in Figure 5-4), this model can be used to account for the lateral voltage drop in the n^+ region provided that the value of m is large enough.

4.6 Method of Approach

4.6.1 Approach of the Previous Work

The one dimensional equations stated in section 4.2.1 have previously been solved numerically [4,12,13,14]. In these simulations, carrier generation has been neglected and recombination has been considered to be primarily trap-assisted with a rate given by Equation 4-15. The hole current density boundary condition given by Equation 4-18 has been used and therefore, tunneling of holes through the barrier at high bias has been neglected. The hole barrier lowering has not been considered by [4,12,13] while [14] considers the phenomenon improperly. The effect of the lateral voltage drop has also not been considered.

4.6.2 Approach of this Work

As discussed previously, carrier generation is significant only at very high electric fields corresponding to very high forward bias and therefore, has been neglected. For carrier recombination, the Auger process and the trap-assisted process have both been considered in the simulation. The effects of hole barrier lowering and energy gap shrinkage near the junction on the current density boundary condition have been included as well. The simulation is also corrected for lateral voltage drop in the n^+ region. The tunneling of holes through the barrier, as given by Equation 4-32, has not been included in the simulation due to the added complexity to the numerical solution.

As previously mentioned, the numerical solutions were performed by C.C. Yu at IBM corporation [4]. The contributions of this thesis to the

simulation were the inclusion of effects due to hole barrier height lowering, energy gap shrinkage, Auger recombination, and buried layer lateral voltage drop. The simulation results are to be presented later in Chapter 6 in the context of comparison with experimental results.

4.6.3 Parameter Determination

The various parameters in the differential equations and the boundary conditions are related to the material properties as follows;

i) Carrier mobilities in the Yu simulation are related to the doping density as well as temperature and the electric field. Empirical functions relating the mobility with the above variables developed by [43] have been used to determine the mobility at each point in the device for a given bias level.

ii) Einstein's relation has been used to relate diffusion coefficients with carrier mobilities.

iii) The electron and hole thermal velocities v_n and v_p are obtained from [34];

$$v_n = A^* T^2/qN_c \tag{4-34}$$

$$v_p = A^* T^2/qN_v \tag{4-35}$$

iv) The image-force induced barrier height lowering, $\Delta\Phi$, is given by [34];

$$\Delta\Phi = [qE/4\pi\epsilon_s]^{1/2} \qquad (4\text{-}36)$$

where E is the electric field in the semiconductor near the barrier and ϵ_s is the dielectric constant of the semiconductor.

v) Due to the formation of platinum-silicide at the interface during the fabrication of the device, the barrier height of the device depends on the temperatures involved in the fabrication process [34]. Therefore, the value of the barrier height must be experimentally determined for the devices under study. The various measurement techniques and their corresponding results are addressed in the following chapter.

CHAPTER FIVE

BARRIER HEIGHT DETERMINATION

5.1 Introduction

The barrier height of a Schottky diode is an important parameter in the simulation of the device and a variety of methods have been developed for its measurement. These methods include capacitance vs. voltage measurements, photo-electric emission measurements, and current vs. voltage measurements. However, when the Schottky diode test device is a part of an LSI/VLSI integrated test site, one is often limited to current-voltage measurements. This is due to the fact that in such a test structure, there is no optical access to the device and the parasitic capacitance of the test structure often overwhelms the small junction capacitance of the SBD. Such is the case for the test devices used in this work.

The most traditional methods for evaluating the barrier height from I-V data are the activation energy method and the Richardson's

constant method both of which rely on obtaining the saturation current from the linear portion of a semilog plot of the I-V data where the effect of the parasitic series resistance is negligible. A third method, originally proposed by Norde [44] and later modified by others [45,46,47], has the advantage of tolerating a large resistance in series with the device.

These three methods generate results with discrepancies, sometimes on the order of tens of millivolts [47,48]. Considering the fact that small errors in the value of barrier height result in large errors in the theoretical simulation of the device and also, in light of the fact that the value of barrier height for a device depends on the processing involved in its fabrication [5,34], it is desired to have I-V methods which generate reliable and consistent results.

This chapter discusses some limitations to each method and develops more general forms for Richardson's constant method and Norde's method which account for effects due to the barrier lowering phenomenon. The results of each approach are compared for our test devices which, as discussed earlier, are platinum-silicide Schottky barriers on n-type epitaxial silicon. Checking each method for self-consistency shows that for these devices, the modified Norde's method gives the most accurate results.

5.2 Barrier Height Lowering and the Ideality Factor

The ideal Schottky equation based on thermionic emission-diffusion theory, and ignoring the effect of barrier height lowering, is given by [34]

$$I = I_s \exp(\beta V_j) = A_e A^{**} T^2 \exp(-\beta \Phi_b) \exp(\beta V_j) \qquad (5\text{-}1)$$

for V_j > several β^{-1} where $\beta = q/kT$, A_e is the effective area of the junction, A^{**} is the modified Richardson's constant, and Φ_b is the barrier height. The voltage across the junction, V_j, is given by

$$V_j = V - RI \qquad (5\text{-}2)$$

where R is the parasitic series resistance of the device. In this chapter, the saturation current term, I_s, is generically used as a prefactor in front of the $\exp(\beta V_j)$ term. As additional physical phenomena are considered, the specific expression for I_s changes from that in Equation 5-1.

It is common practice to approximately account for many of the effects by which the diode characteristics deviate from Equation 5-1 (i.e. non-ideal effects) by a non-rigorously introduced and empirically determined constant called the ideality factor η such that

$$I = C \exp(\beta V_j/\eta) \qquad (5\text{-}3)$$

where C is a constant of proportionality. For forward biased junctions, most of these non-ideal effects are significant at low bias. Low bias non-ideal effects include barrier height lowering, quantum mechanical tunneling of carriers through the junction, and recombination of carriers in the depletion region, all of which result in currents in

excess of what is given by Equation 5-1. The effects of drift and diffusion of carriers in the space charge layer and minority carrier injection, on the other hand, are significant at very high bias corresponding to large current densities [5].

With the proper choice of C and η, Equation 5-3 can be used to approximately describe the behavior of a given diode. However, when using current voltage data to provide diagnostic information about the barrier, it is necessary to treat this equation with caution since different barrier structures can result in the same value of η over a given range of current [49]. Also, for $\eta > 1$, interpreting the value of C as the saturation current given by Equation 5-1 results in a low value of barrier height since $C > I_s$. Figure 5-1 shows a plot of Equation 5-1 and a hypothetical set of observed data with exaggerated non-ideal effects to demonstrate this point.

One important 'non-ideal' effect which is unavoidable is the barrier height lowering, $\Delta\Phi$, caused by the image force at the junction. This effect gives rise to an effective barrier height, Φ_e, as below;

$$\Phi_e(V_j) = \Phi_b - \Delta\Phi(V_j) \qquad (5\text{-}4)$$

Assuming no interfacial layer at the junction, Φ_b is independent of voltage [5]. However, barrier height lowering, $\Delta\Phi$, and therefore Φ_e, are voltage dependent. Correcting Equation 5-1 for barrier lowering

$$I = I_s \exp(\beta V_j) = A_e A^{**} T^2 \exp[-\beta \Phi_e(V_j)] \exp(\beta V_j) \qquad (5\text{-}5)$$

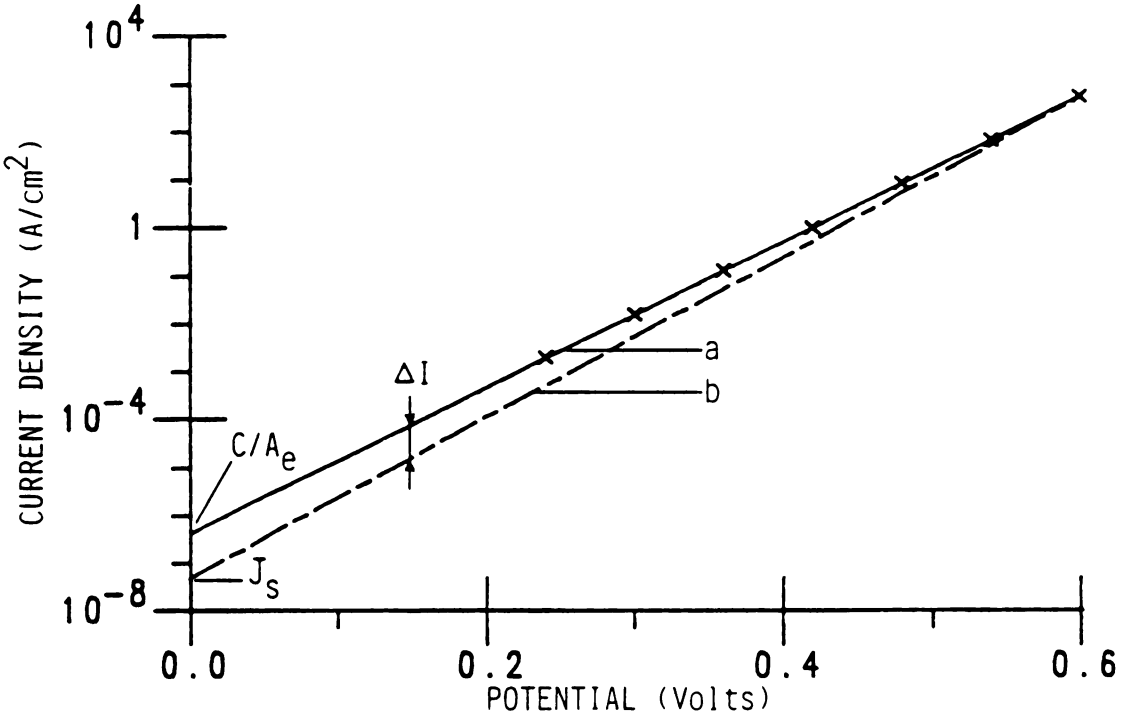


Figure 5-1 A hypothetical set of observed data with exaggerated non-ideal effects is shown by X. (a) shows a plot of Equation 5-3 with the best fit to the data (η =1.1). (b) shows the plot of the ideal diode equation (Equation 5-1). The excess current due to non-ideal effects is denoted by ΔI. The non-ideal effects cause the extrapolated current density intercept, C/A_e, to be greater than $J_s = I_s/A_e$ for I_s as given by Equation 5-1.

In the absence of other non-idealities, Equation 5-5 is an exact relation which, as will be shown, forms the basis of our modified Norde's method. The activation energy method and the Richardson's constant method, on the other hand, require fitting experimental data to an equation with a voltage independent value of I_s. For real Schottky diodes, however, I_s is voltage dependent as seen from Equation 5-5 and therefore, these methods have to utilize an approximation of Equation 5-5.

In some treatments, the effect of barrier lowering on forward I-V characteristics has been folded into the ideality factor η [5,34] such that

$$I = I_s \exp(\beta V_j/\eta) \tag{5-6}$$

where $$I_s = A_e A^{**} T^2 \exp(-\beta\Phi_e(0)) \tag{5-7}$$

However, this approach has inherent disadvantages as may be seen from the following discussion. Equation 5-5 can be written as

$$I = A_e A^{**} T^2 \exp[-\beta \Phi_e(0)] \exp[\beta(V_j - f(V_j))] \tag{5-8}$$

where, $$f(V_j) = \Phi_e(V_j) - \Phi_e(0) \tag{5-9}$$

Obviously, $\beta(V_j - f(V_j))$ could be written as $\beta V_j/\eta$ if $f(V_j)$ was linearly proportional to V_j. However, $f(V_j)$ goes only as $V_j^{1/4}$ and

hence, is far less sensitive to changes in junction voltage than a linear relation. In Appendix C, a method is developed to better approximate the voltage dependence of barrier height as below;

$$I = I_s \exp(\beta V_j/\eta^*) = A_e A^{**} T^2 \exp\{-\beta[\Phi_e(V_m)+\Delta\dot{\Phi}(V_m).V_m]\}\exp[\beta V_j/\eta^*] \quad (5\text{-}10)$$

and

$$\eta^* = [1 + \Delta\dot{\Phi}(V_m)]^{-1} \quad (5\text{-}11)$$

where η^* is the ideality factor due to barrier lowering, V_m is the mean value of the range of voltage to which the above equation is applied, and $\Delta\dot{\Phi}(V_m)$ is the first order derivative of $\Delta\Phi$ evaluated at V_m.

The barrier lowering $\Delta\Phi(V_j)$ of an n-type device is given by [5]

$$\Delta\Phi(V_j) = \{q^3 N_D/8\pi^2\epsilon_s^3 [V_c - V_j - 1/\beta]\}^{1/4} \quad (5\text{-}12)$$

where ϵ_s is the semiconductor dielectric constant, the equilibrium contact potential, V_c, is given by

$$V_c = \Phi_b - (E_c - E_f)_{bulk}$$

and N_D is the doping concentration. Furthermore,

$$(E_c - E_f)_{bulk} = 1/\beta \ln(N_C/N_D) \quad (5\text{-}13)$$

where N_C is the effective density of states in the conduction band.

$$\text{so,} \quad \Delta\Phi(V_j) = \left\{ q^3 N_D / 8\pi^2 \epsilon_s^3 \left[\Phi_b - V_j - 1/\beta \left(1 + \ln(N_C/N_D) \right) \right] \right\}^{1/4} \qquad (5\text{-}14)$$

$$\text{and,} \quad \Delta\dot{\Phi}(V_j) = -\left[q^3 N_D / 32\pi^2 \epsilon_s^3 \right]^{1/4} \left[\Phi_b - V_j - 1/\beta \left(1 + \ln(N_C/N_D) \right) \right]^{-3/4} \qquad (5\text{-}15)$$

5.3 The Activation Energy Method

The activation energy method is based on Equation 5-7 which assumes that the voltage dependence of barrier height lowering can be accounted for by the ideality factor η. Equation 5-7 can be written as [34]

$$\ln(I_s/T^2) = \ln(A_e A^{**}) - (q/KT) \Phi_e(0) \qquad (5\text{-}16)$$

In order to apply this method, values for I_s are obtained from the abscissa intercept of the linear portion of the log(I)-V plot of the experimental data at several temperatures. Subsequently, as can be seen from Equation 5-16, the slope of a semilog plot of I_s/T^2 vs. 1/T yields the zero bias effective barrier height $\Phi_e(0)$.

The advantage offered by this method is that knowledge of either the Richardson's constant A^{**} or the diode's effective area A_e is not necessary [5,34]. However, small but systematic deviations of the

experimentally determined value of I_s from what is given by Equation 5-7, caused by the voltage dependence of Φ_e and other non-idealities as previously discussed, may lead to appreciable changes in the slope which results in erroneous calculated values for the barrier height. Equation 5-10, which is a better approximation of the voltage dependence of the effective barrier height, may not be used for this method since the mean value of the range of measured voltages, V_m, usually varies with temperature. The temperature dependence of the barrier height may also lead to additional error in the value of the calculated barrier height.

Rhoderick [5] has considered the case where Φ_e depends on temperature due to the temperature dependence of work functions and shows that to the extent that the effect can be approximated by a linear relation, the activation energy method yields the value of $\Phi_e(0)$ at zero temperature.

5.4 The Richardson's Constant Method

The standard Richardson's constant method is also based on Equation 5-7. However, this approach uses the values of A^{**} and I_s at a given temperature to calculate Φ_e. A potential disadvantage of this method is that the value of A^{**} which depends on the electric field, must be known. However, A^{**} is well known for silicon Schottky diodes [34] and is relatively constant ($\simeq$110 A/cm^2K^2 for n-type Si) over the range of electric field present at the contact (see [50] for values of A^{**} for

GaAs). Additionally, the value of Φ_e obtained from Equation 5-7 depends on the logarithm of A^{**} and is therefore, insensitive to variations in the value of A^{**}.

As has been previously discussed, however, Equation 5-7 is based on the assumption that the barrier lowering effect can be incorporated into a diode ideality factor, η. As shown in section 5.2, a more accurate approach of accounting for the effect of barrier lowering is to use (see Equation 5-10)

$$\Phi_e(V_m) + \Delta\dot{\Phi}(V_m).V_m = 1/\beta \ln (A_e A^{**}T^2/I_s) \qquad (5\text{-}17)$$

where again, values of I_s are obtained by extrapolating the abscissa intercept of the log(I)-v plot. This forms the basis for obtaining Φ_b in a modified Richardson's constant method. Since $\Phi_e(V_m)$ and $\Delta\dot{\Phi}(V_m)$ both depend on Φ_b (see Equations 5-4 and 5-14), Equation 5-17 gives an implicit relation for Φ_b and may be solved iteratively. The accuracy of this method depends on the absence of other non-idealities besides barrier lowering. In other words, the experimentally determined value of η should not be larger than the value of η^* obtained from Equation 5-11.

5.5 Modified Norde's Method

The original method proposed by Norde [44] is based on Equation 5-1. The method calculates the barrier height by plotting the function

$$F(V) = V/2 - 1/\beta \ln(I/A_e A^{**} T^2) \qquad (5\text{-}18)$$

then finding its minimum at $(V_o , F(V_o))$ and finally calculating the barrier height from

$$\Phi_b = F(V_o) + V_o/2 - 1/\beta \qquad (5\text{-}19)$$

This method has been used in the literature as a better alternative to other I-V methods [51,52,53,54]. As originally presented, however, the method did not consider barrier lowering and assumed a unity ideality factor for the device with the justification that non-ideal effects are significant only at low values of current and therefore, can be neglected at the higher bias levels used by the method. Later, Schwartz et. al. [47] modified Equation 5-19 to account for a non-unity ideality factor. Their modification, following the discussion in section 5.2, is expected to underestimate the value of barrier height since it takes C, given by Equation 5-3 to be the saturation current I_s as given by Equation 5-1. Lien et. al. [46] have used this method to first find the series resistance R, then subtract series resistance effects from the original I-V data in order to find the barrier height by the Richardson's constant method. Therefore, their method has the same limitations as discussed in section 5.4 for the Richardson's constant method. Chot [45] proposes a method which involves plotting F(V) at several temperatures and obtaining the barrier height by a slope method. Temperature-variable methods for determination of barrier height, however, are compromised by the fact that the barrier height

itself is temperature dependent. These modifications do not explicitly consider the barrier height lowering effect.

While the assumption of insignificant non-ideal effects at high bias is true for most non-ideal phenomena, in what follows, a more general form of Norde's method which considers barrier height lowering is developed and shows that the voltage dependence of barrier lowering plays a significant role in barrier height determination by this method.

F(V) is more generally defined as

$$F(V) = V/\alpha - 1/\beta \ln(I/A_e A^{**} T^2) \qquad (5\text{-}20)$$

where α is an arbitrary constant > 1. In the standard Norde's method, I is expressed as in Equation 5-1. However, in this modification, Equation 5-5 which explicitly accounts for barrier lowering is used. From Equations 5-2, 5-4, and 5-5

$$F(V) = (1/\alpha - 1)V + IR + \Phi_b - \Delta\Phi(V_j) \qquad (5\text{-}21)$$

Under high bias, minority carrier injection into the bulk of the device may be significant and consequently, the parasitic series resistance, R, may be modulated. For bias values below that level, however, R is independent of bias and therefore,

$$dF(V)/dV = (1/\alpha - 1) + R dI/dV - d\Delta\Phi/dV \qquad (5\text{-}22)$$

This equation is solved for $dF/dV = 0$ to find the minimum $(V_o, F(V_o))$ in Appendix C and results in

$$RI_o = 1/\beta\ (\alpha - 1/S) \tag{5-23.a}$$

and

$$V_o = 1/\beta\ [\ln(\alpha - 1/S)/\beta RI_s] \tag{5-23.b}$$

where

$$S = 1 + \Delta\dot{\Phi}(V_{jo})$$

and I_s is given by Equation 5-5. Therefore, from Equation 5-21

$$\Phi_b = \Delta\Phi(V_{jo}) + F(V_o) + (\frac{\alpha - 1}{\alpha})V_o - \frac{\alpha S - 1}{\beta S} \tag{5-24}$$

where using Equation 23.a,

$$V_{jo} = V_o - 1/\beta\ (\alpha - 1/S) \tag{5-25}$$

Equation 5-24 provides a relation for the barrier height which corrects for the barrier lowering at a specific junction voltage. Also, since $\Delta\Phi(V_j)$ depends on Φ_b (see Equation 5-14), Equations 5-24 and 5-25 form an implicit expression for the barrier height and must be solved iteratively.

To find the best choice for α, note that (see Appendix C)

$$[d^2F/dV^2]_{Vo} \approx \beta\ (\alpha - 1)/\alpha^3 \tag{5-26}$$

differentiating this with respect to α and setting the result equal to zero yields $\alpha = 1.5$. Therefore, for this value of α, the second derivative of F(V) is maximized and hence, the minimum of the F(V) plot is the sharpest and the best resolution is achieved. If, however, due to the limitations posed by the data, it is desired to have the minimum occur at a particular point, one can use Equation 5-23.b to find the value of α which makes the minimum occur at that point. In that case, an apriori knowledge of R is not necessary to obtain α since by approximating S by 1, from Equation 5-23.b

$$V_o(\alpha_2) - V_o(\alpha_1) = 1/\beta \, [\ln (\alpha_2 - 1)/(\alpha_1 - 1)] \qquad (5\text{-}27)$$

So, by using an arbitrary value of α_1 and finding $V_o(\alpha_1)$, one can find the value of α_2 which yields the desired value for $V_o(\alpha_2)$.

This method has several advantages. First, it can be applied to a device with a large series resistance (i.e. the existence of a linear region in the semilog plot of the I-V data is not required). Secondly, it can utilize data at higher bias where the non-ideal effects are negligible and finally, α may be chosen to utilize the data about a desired bias level. A potential disadvantage of the method is the fact that it only uses a few data points about the minimum V_o and therefore, is sensitive to error in that data [46].

5.6 Results and Discussions

The experimental procedure for obtaining the I-V data has previously been discussed in Chapter 3 and the results of the current

density vs. voltage measurements at four temperatures are shown in Figure 3-15. Table 5-1 contains the extrapolated current density axis intercept, C/A_e, and ideality factor obtained from the data by a least squares fit over the linear portion. Beyond about 0.7 volts, the current is limited by the series resistance of the epitaxial layer, which is on the order of 20 Ohms.

The diode ideality factor, η is approximately 1.04 in the straight line portion of the curves which indicates that barrier lowering is not the only non-ideal effect in play. Typical values of η^*, the ideality factor due to barrier lowering alone, are found to be on the order of 1.02. Consequently, as discussed previously, the activation energy method and the Richardson's constant method underestimate the barrier height.

When the values of C/A_e from Table 5-1 are used to obtain the barrier height using the activation energy method, an effective barrier height of 0.888 V was obtained. As discussed in section 5.3, to the first order, this value may be interpreted as the effective barrier height at zero temperature under zero bias. Correcting for barrier lowering results in a value of $\Phi_b(T=0) = 0.918$ V.

The Richardson's constant method was used to obtain the barrier height both for the traditional method using Equation 5-7 and the modified method introduced in this work using Equation 5-17. Results are shown in Table 5-2 where it is seen that the modified method results in slightly higher values for Φ_b as expected.

Table 5-1 Experimentally determined current density axis intercepts and ideality factors.

Temp. °C	C/A_e (A/cm^2)	η
27	8.81×10^{-8}	1.045
85	3.23×10^{-5}	1.046
100	1.10×10^{-4}	1.042
125	7.44×10^{-4}	1.040

Table 5-2 Barrier height values obtained from; (a) original Richardson's constant method using Equation 5-7, (b) modified Richardson's constant method using Equation 5-17.

Temp. °C	Barrier Height ϕ_b in V	
	a	b
27	.866	.871
85	.856	.858
100	.853	.856
125	.847	.849

Table 5-3 shows the results obtained by using Norde's method. Column a shows the results obtained using the originally proposed method which neglects the barrier lowering effect. Column b contains the results obtained from the method proposed by Schwartz et. al. to account for an ideality factor [47] and Column c shows the results of the modified method presented in section 5.5 which accounts for the barrier lowering effect. A value of 1.5 was chosen for α for the latter method and Figure 5-2 shows the plots of F(V) for this choice of α.

The difference between the various barrier height values listed in tables 5-2 and 5-3 are significant. Noting that all the methods discussed here are fundamentally based on Equation 5-5, to check for self-consistency each of the resulting barrier heights at room temperature are used to plot Equation 5-5. Comparing these plots with the experimental data shows how accurate each method is. Figure 5-3 shows that a barrier height value of 0.881 V, generated by the modified Norde's method (Column C of Table 5-3), gives excellent agreement with the experiment. Furthermore it will be shown in Chapter 6 that when this barrier height value is used in the numerical simulation, the results also match the experimental values. The barrier height values determined by the Richardson's constant method and the original Norde's method, however, produced considerably different results. Figure 5-3 also confirms that the modified Richardson's constant method is an improvement of the original method.

The barrier height is expected to change with temperature because of the temperature dependence of the energy gap, the electron affinity of silicon, and the work function of the metal. Experimental data is available only on the energy gap temperature dependence which has a

Table 5-3 Barrier height values obtained from; (a) original Norde's method, (b) Norde's method modified by Schwartz et. al. [47] to account for the ideality factor η, (c) Norde's method modified to account for barrier lowering $\Delta\Phi$, as in this work.

Temp. °C	Barrier Height ϕ_b in V		
	a	b	c
27	.866	.837	.881
85	.852	.827	.869
100	.849	.826	.864
125	.842	.819	.858

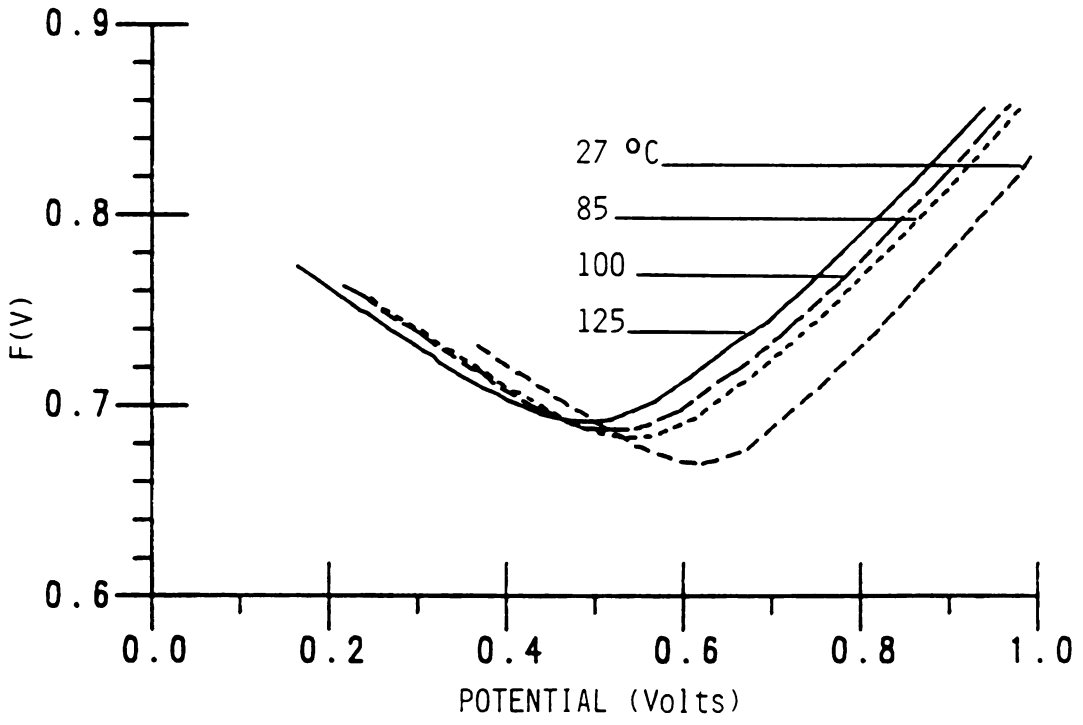


Figure 5-2 Plots of F(V) as defined by Equation 5-20 for α=1.5 using the experimental data of Figure 3-15.

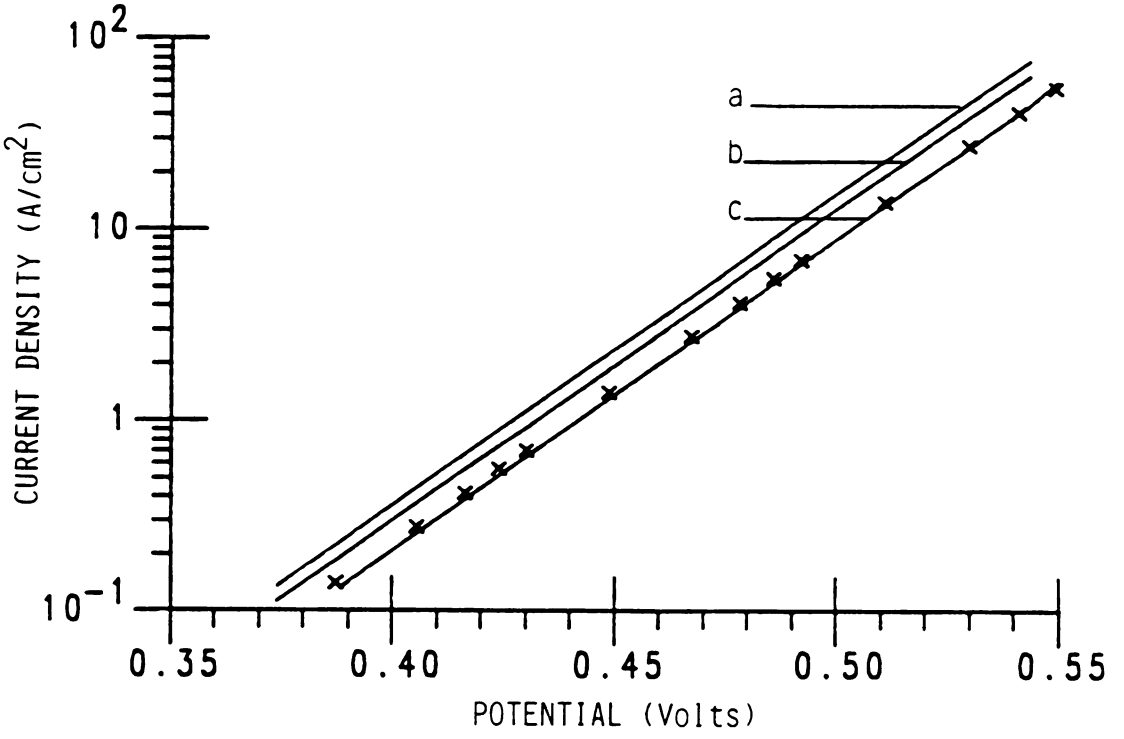


Figure 5-3 Solid lines show plots of Equation 5-5 at 27°C using the barrier height value of; (a) original Norde's and Richardson's constant method (0.866 V), (b) modified Richardson's constant method (0.871 V), (c) modified Norde's method (0.881 V). The experimental data is marked with X. As expected, the best agreement between c and experiment is at higher current levels where the non-ideal effects are negligible.

linear coefficient equal to 4.7×10^{-4} eV/K [34]. The barrier height obtained by the modified Norde's method is observed to decrease monotonically with temperature in a relatively linear fashion with a coefficient approximately equal to 2.3×10^{-4} V/K. This may be compared with a barrier height temperature coefficient of 3×10^{-4} V/K reported for photoelectric measurements on Au-Si diodes [5]. Figure 5-4 shows the agreement between Equation 5 using the barrier height values in Column c of Table 5-3 and experiment at 85°C, 100°C, 125°C.

The barrier height results in Column b of Table 5-3 are significantly smaller than the values in Column c of that table which, following the discussion made on the ideality factor in section 5.2, is to be expected. This difference is also consistent with the observation made by Schwartz et. al. [47] that their modification of Norde's method resulted in barrier height values which were considerably lower than the values determined by photo response. The 15 to 17 mV difference in the values of Columns a and c in Table 5-3 show the significance of considering the barrier lowering phenomena in the modified Norde's method. The results in Column b of Table 5-2 are also smaller than those in column c of Table 5-3 due to the error in the modified Richardson's constant method caused by the fact that the measured values of ideality factor (≈ 1.04) are larger than the values obtained by Equation 11 (≈ 1.02) (i. e. barrier height lowering is not the only significant non-ideality in this device).

If the values obtained for the barrier height (Table 5-3, Column c) are extrapolated to find Φ_b at zero temperature assuming a linear temperature dependence, a value of 0.950 V is obtained. This value is 32 mV higher than what the activation energy method gives using the

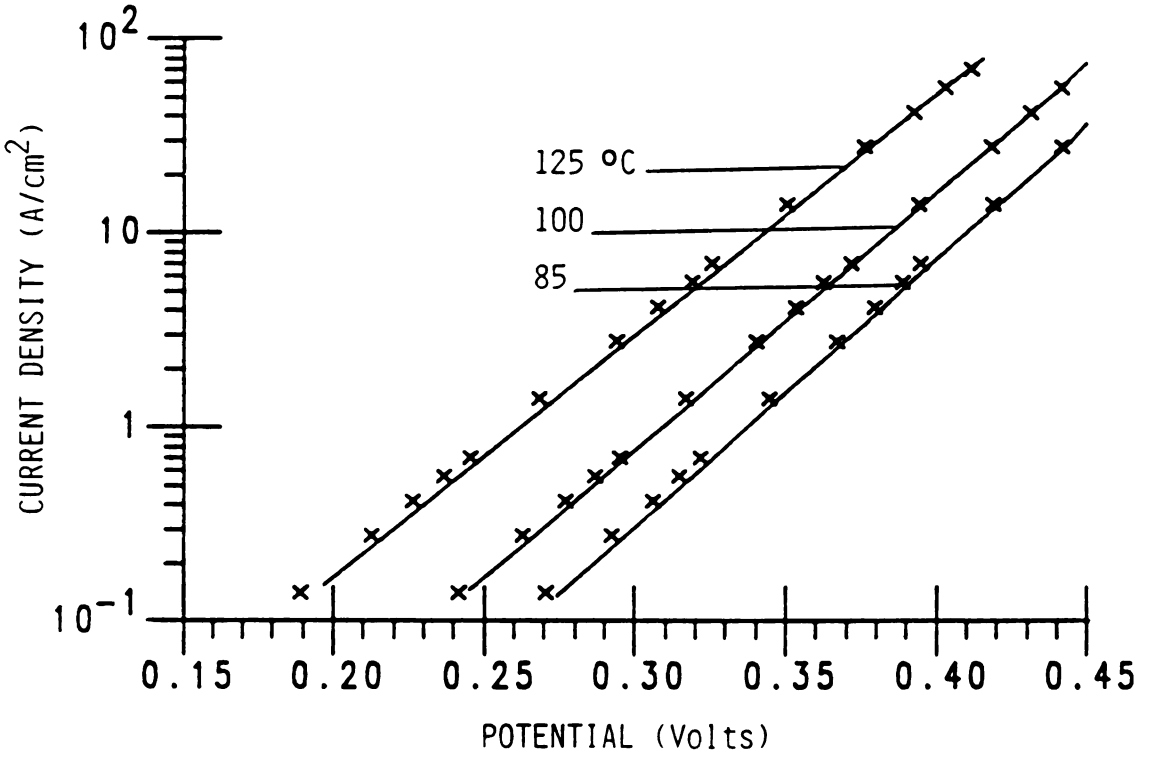


Figure 5-4 Comparison of experiment with plots of Equation 5-5 at elevated temperatures using the barrier height values obtained from modified Norde's method and experiment. The experimental data is denoted by X.

same linear relation with temperature. This discrepancy is due to the fact that, as discussed in section 5.3, the activation energy method neglects the voltage dependence of the effective barrier height as well as other non-ideal effects.

To check for variations in the barrier height values obtained for different devices, the modified Norde's method was applied to data obtained for two other devices. One device showed barrier height values almost identical to the test device used to obtain the values reported here while the other device had room temperature barrier height of 0.903 V. As discussed previously, such variations from device to device are expected since the barrier height of the device depends on the processing involved in its fabrication.

5.7 Chapter Summary and Conclusions

Three methods have been compared for calculating the value of the barrier height of an SBD from the forward bias I-V data. The Richardson's constant method and the Norde's method are modified to account for barrier lowering and the modified Norde's methods is shown to generate accurate results as determined by its self-consistency demonstrated by the agreement between Equation 5-5 and experiment. The barrier height of a platinum-silicide Schottky diode is determined to be 0.881 V at room temperature and to decrease with increasing temperature with a coefficient of about 2.3×10^{-4} V/K. Less accurate are the modified Richardson's constant method and the activation energy method. While the former method can generate accurate results for devices with barrier lowering as their only non-ideal effect, the

latter method can only be used to obtain an estimate of the barrier height at zero temperature. A comparison of the measured ideality factor and the one calculated using Equation 5-11 shows whether or not barrier lowering is the dominant non-ideal effect.

Comparing the three methods, it is concluded that the following criteria may be used to choose the proper I-V method to calculate the barrier height.

i) If the values of A_e, A^{**}, ϵ_s, and N_D are known, then the modified Norde's method which explicitly accounts for barrier height lowering, is preferred. However, the technique is sensitive to statistical error in the I-V data.

ii) If the values of A_e, A^{**}, ϵ_s, and N_D are known and the semilog plot of the I-V data has a large enough linear range such that the abscissa intercept can be extrapolated and η can be determined, but, the data is suspected of having non-negligible statistical error, then the modified Richardson's constant method is preferred. The accuracy of this method depends on how close the measured η is to what is obtained by Equation 5-11.

iii) If the values of A_e and A^{**} are known while either ϵ_s or N_D are not known, then the original Norde's method or the original Richardson's constant method may be used to estimate the barrier height.

iv) If the value of A^{**} or A_e is not known, then the activation energy method may be used to obtain a rough estimate of the zero temperature barrier height.

For the test devices used in this work, the first condition applies.

CHAPTER SIX

COMPARISON OF SIMULATION AND EXPERIMENT

6.1 Introduction

In order to check the validity of the theoretical treatment of current transport in the SBD, which was discussed in Chapter 4, and also to check the significance of various physical phenomena in the device behavior, the results of numerical simulation are compared with experimental data. The comparison is made both for the excess minority carrier storage data and the J-V characteristics in order to provide a comprehensive diagnoses of the device behavior as related to minority carrier injection.

To consider the conductivity modulation effect explicitly, it is necessary to extract the J-V characteristics of the bulk from the overall J-V characteristics of the diode. To obtain the bulk voltage, the junction voltage must be subtracted from the measured diode voltage for every given value of current. Consequently, an accurate relation

between the junction voltage and the current through the device is required.

The ideal diode equation (Equation 2-1) can be used for this purpose for low to moderate injection levels. At high injection, however, the equation is no longer valid and the junction and bulk voltages can not be separated accurately. An alternative to the explicit method discussed above, which eliminates the problem of determining the junction voltage, is simply to consider the overall J-V characteristics which implicitly includes the bulk conductivity effects. Direct comparison of the theoretically and experimentally determined J-V characteristics of the device, provides the insight necessary to check the adequacy of the theory in treating the effects of conductivity modulation.

This chapter first examines the correlation between experiment and theory based on the traditional simulation discussed in Section 4.6.1. Subsequently, lateral voltage drop, boundary condition considerations such as hole barrier height lowering and image-force induced energy gap shrinkage, and Auger recombination are considered separately, and the effect of each phenomenon on correlation of simulation and experiment is examined. Throughout the steps outlined above, only room temperature results have been considered while later in the chapter, higher temperatures are examined.

6.2 Traditional Simulation

6.2.1 Simulation Method

The traditional one dimensional numerical simulation has already been discussed in Section 4.2. In summary, the one dimensional differential equations given in Section 4.2.1 are solved subject to boundary conditions outlined in Section 4.2.4. Carrier generation is assumed negligible, and in this version of the simulation recombination is considered limited only to the trap assisted process described by Equation 4-15. Lateral voltage drop and Auger recombination are neglected in this simulation and the effect of the image-force has only been considered in relation with the conduction band. Therefore, phenomena such as hole barrier height lowering at high injection, band gap shrinkage near the barrier and hole tunneling at high injection have also been neglected.

6.2.2 Current-Voltage Comparison

Figure 6-1 shows a comparison between experiment and simulation for a room temperature unguarded SBD for bias up to 1 V. In the low current region, excellent agreement is observed, but above about 10^3 A/cm^2, the simulation predicts more current than what is measured. The good agreement at low currents, where junction characteristics dominate the diode current, primarily indicates the accuracy of the measured barrier height which was obtained from the modified Norde's method. Figure 6-2 shows the simulation results using two barrier height values which are only 22 mV different and demonstrates the sensitivity of the

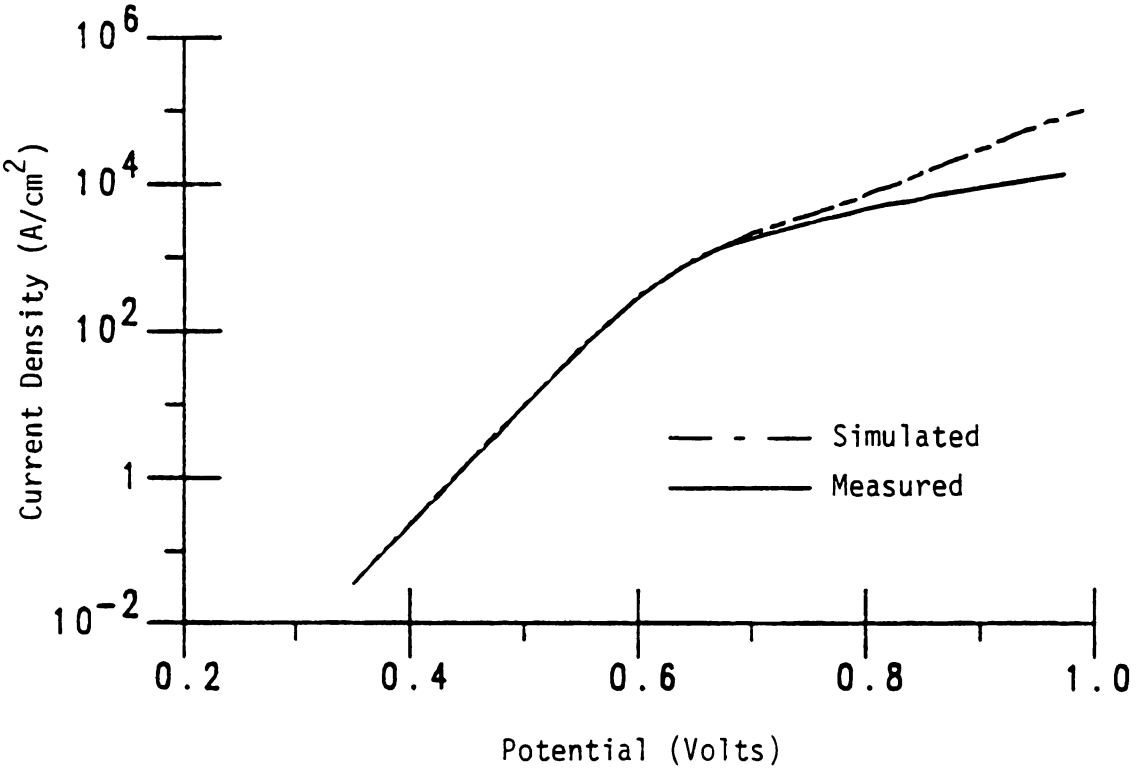


Figure 6-1 Comparison between current-voltage characteristics of the experiment and the traditional simulation for bias up to one Volt.

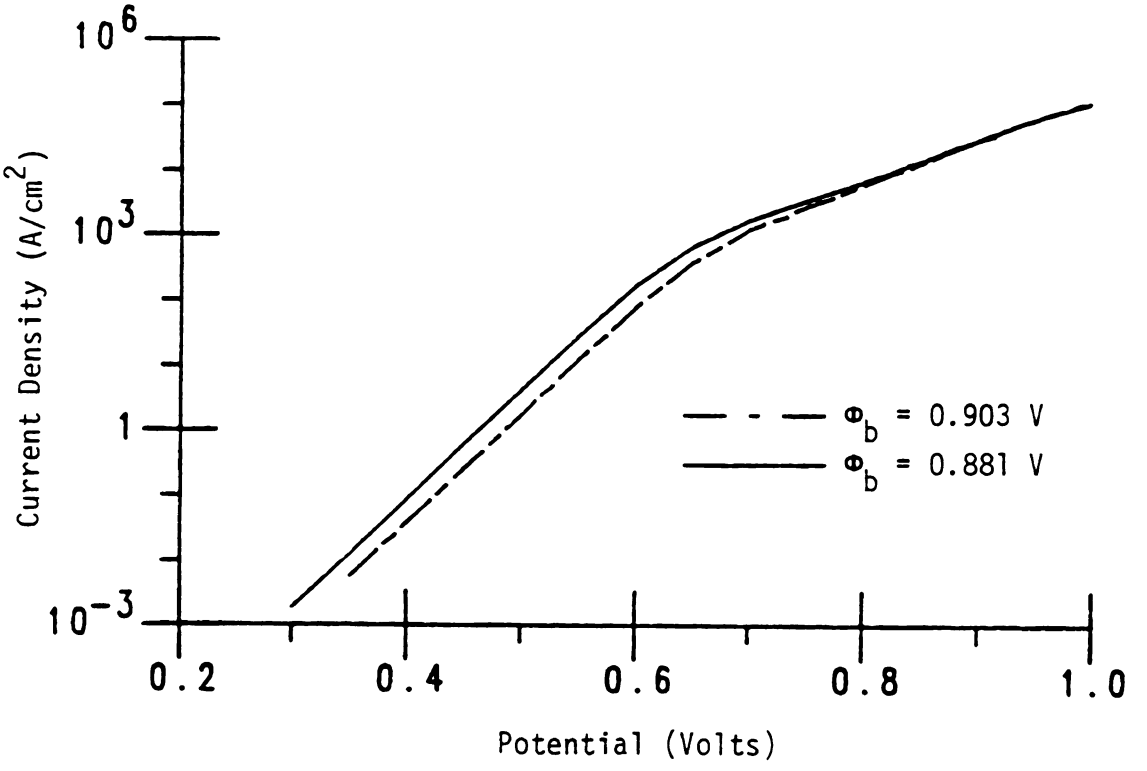


Figure 6-2 Simulation results of the J-V characteristics showing the sensitivity of the simulation on the value of the barrier height, Φ_b.

J-V characteristics on the value of barrier height. The discrepancy in Figure 6-1 between experiment and simulation at high currents, where the bulk resistance plays a dominant role, is due to the resistance associated with the buried n^+ layer and the n^+ contact as will be shown in Section 6.3.

Measured J-V characteristics at room temperature extend to slightly beyond 3 V and 4 X 10^5 A/cm^2. Figure 6-3 shows the comparison between simulation and experiment over this extended range using a linear scale to emphasize the high bias region and a large difference is seen for these very high injection conditions. The traditional simulation initially shows more conductivity modulation than is measured, then a plateau in current (which is not observed experimentally), and eventually the measured current exceeds the simulated current. Clearly, the traditional simulation does not adequately model high current behavior in these test devices.

6.2.3 Stored Minority Carrier Comparison

Figure 6-4 shows the room temperature simulation and experimental results for the charge density associated with stored excess minority carriers. Again, good agreement is found for low bias levels. Beyond about 1.4 Volts, or 6 X 10^4 A/cm^2, less stored charge is measured than predicted. The experimental data is limited to maximum current densities of about 10^5 A/cm^2 by the pulse generator, and at this current density, the simulated charge density is about 40% higher than measured.

Another interesting behavior of the simulation is a peak in the amount of stored charge at a current density of about 2.6 X 10^5 A/cm^2.

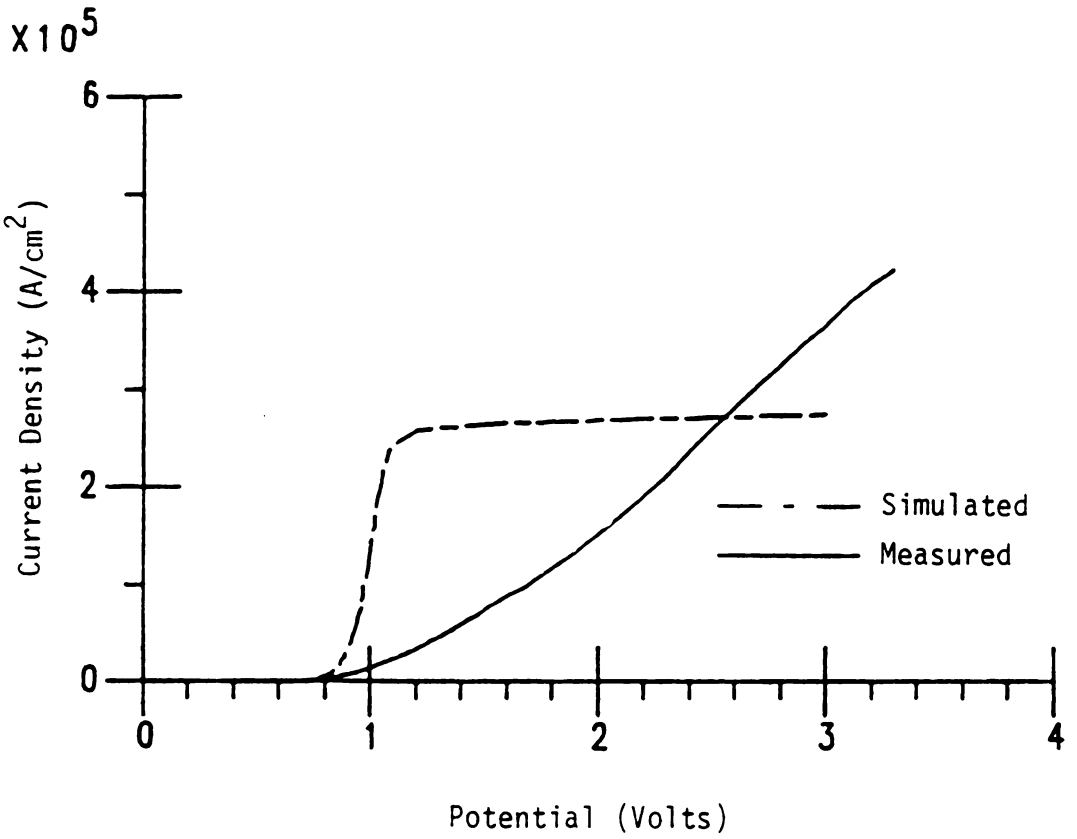


Figure 6-3 J-V comparison between the experiment and the traditional simulation for high injection conditions.

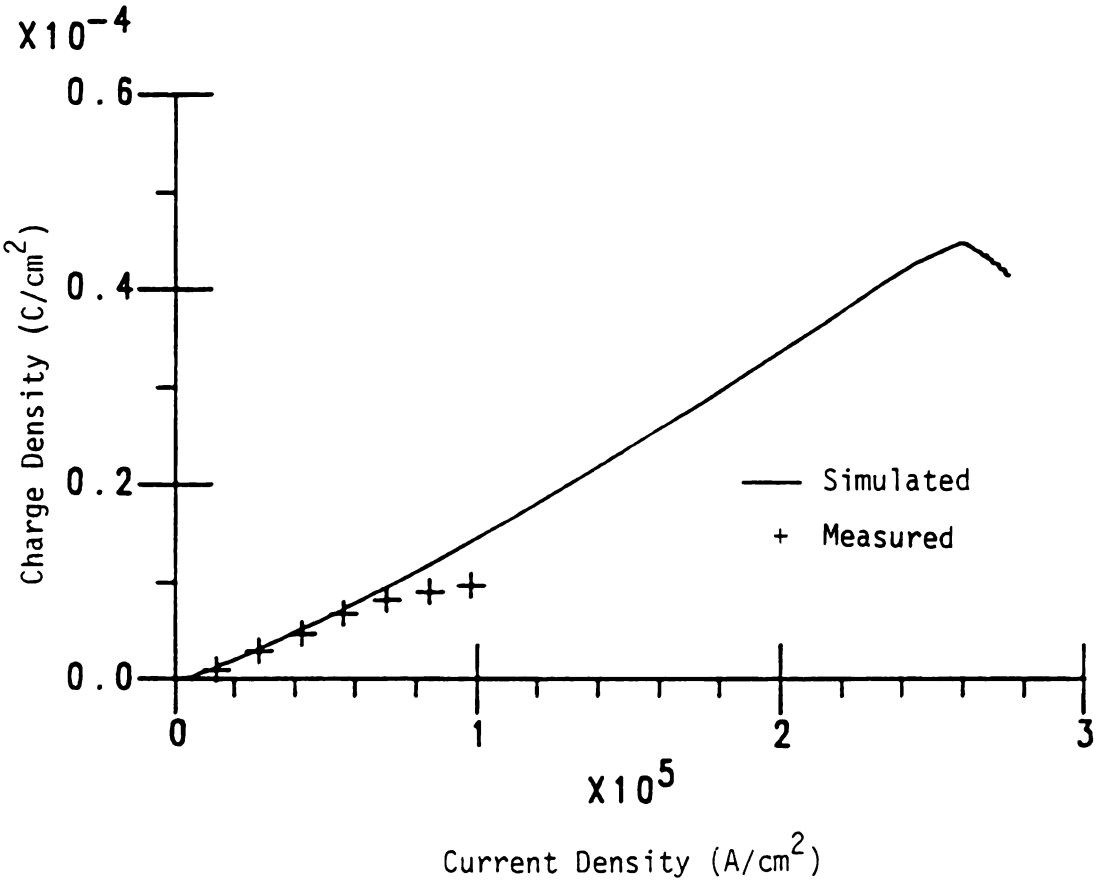


Figure 6-4 Comparison between the experiment and the traditional simulation for the charge density associated with minority carrier storage in the unguarded device. The experimental data is obtained by averaging of the data obtained from four devices.

The mathematical origin of this peak is the limit on the supply of holes imposed by the hole current density boundary condition used in the traditional simulation (Equation 4-18). The same boundary condition is responsible for the plateau in the J-V characteristics that is predicted by the simulation in Figure 6-3 but not seen experimentally. Therefore, the peak in the charge storage results of the traditional simulation, shown in Figure 6-4, is expected to be an artifact not observable experimentally, had the range of experiment reached this level of current density.

6.3 Simulation Corrected for Lateral Voltage Drop

6.3.1 Simulation Method

The method of correcting for the lateral voltage drop was discussed in Section 4.5. Using the algorithm discussed in that section, the current-voltage characteristics of the device and minority carrier stored-charge vs. current were calculated. The area under the anode was divided into 36 elemental diodes (i.e. m = 36 in the algorithm) since larger values of m gave identical results. The lateral voltage drop causes the current in the device to be non-uniform and therefore, current density is a function of position. For the purpose of presentation, however, the device current for experimental and theoretical results is normalized by the diode area to obtain an average current density, J.

6.3.2 Current-Voltage Comparison

With this modification of the traditional simulation, the J-V results are now in good agreement with experiment up to 10^5 A/cm^2 as shown by Figures 6-5 and 6-6 which compare the experiment and the simulation at low and high bias respectively. In Figure 6-6, curve b and the data points show the simulation and experiment results. Curve a shows the simulation results without correction, and the large difference between this curve and curve b shows that the lateral voltage drop is highly significant. Curve c in Figure 6-6 shows the expected J-V characteristics in the absence of conductivity modulation. This curve was generated by treating the SBD as a series combination of a diode and a resistor as described by Equations 5-2 and 5-3. A resistance value of 18Ω, which is the resistance of the epitaxial layer in the absence of conductivity modulation, was used in Equation 5-2. Table 5-1 contains the values of the parameters used in Equation 5-3. Comparing curves b and c of Figure 6-6 points to a considerable amount of conductivity modulation in the device.

At current densities beyond 10^5 A/cm^2, the lateral voltage drop corrected simulation produces currents less than measured, as shown in Figure 6-7. This indicates the presence of additional physical phenomena not considered by the simulation.

6.3.3 Stored Minority Carrier Comparison

As shown in Figure 6-8, the lateral voltage drop correction does not appreciably change the simulated stored minority carrier results since the relationship between forward current density and stored

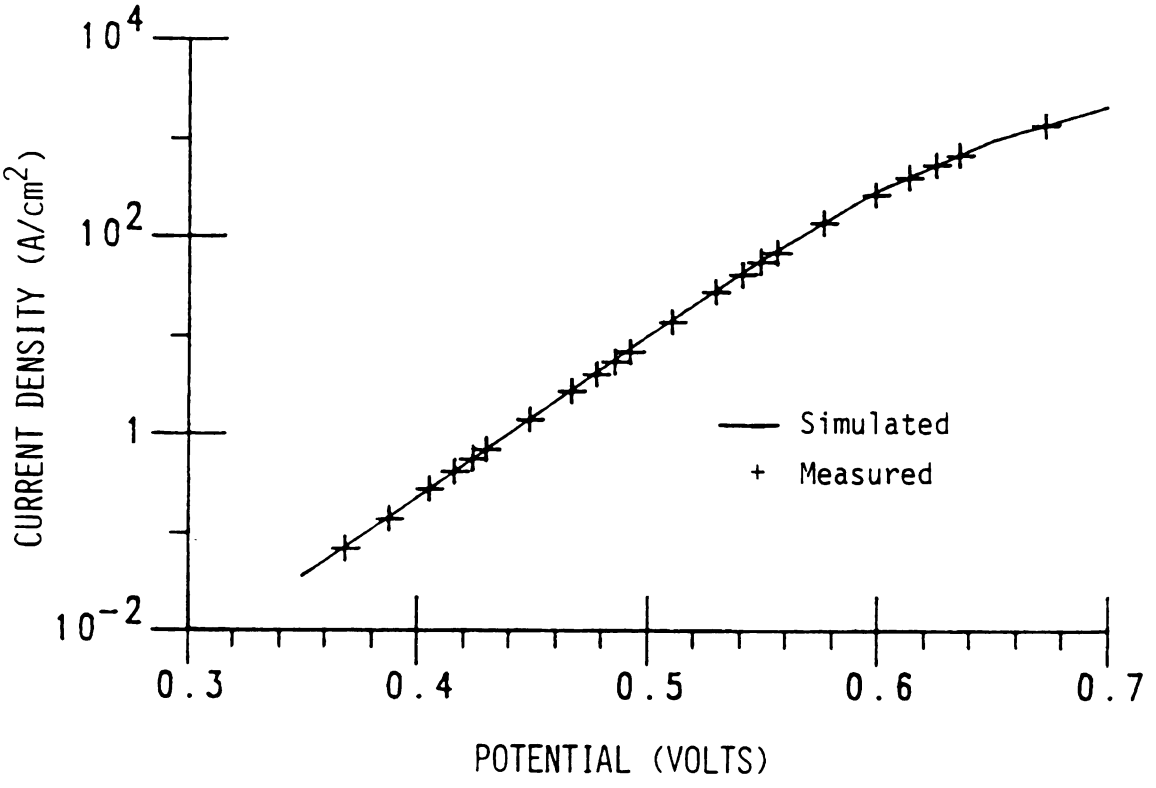


Figure 6-5 Low bias comparison of the measured J-V characteristics with the simulation corrected for lateral voltage drop.

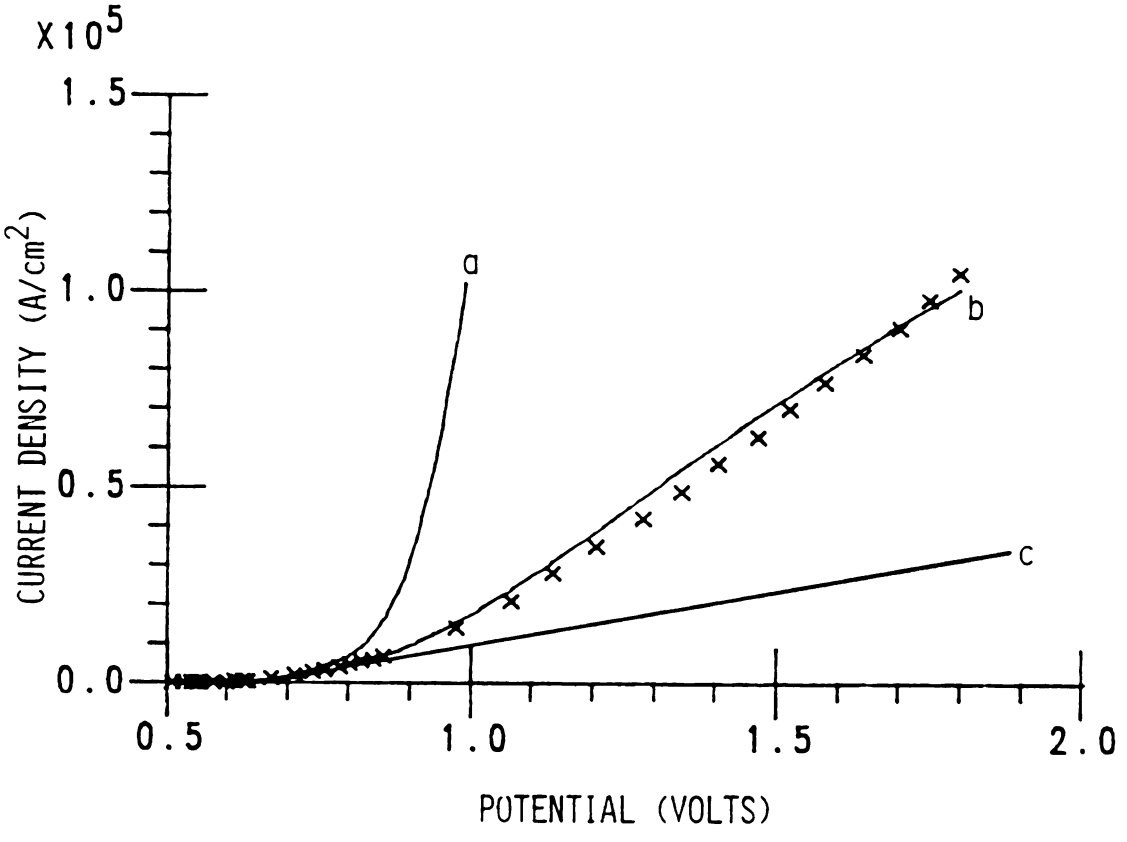


Figure 6-6 Effect of lateral voltage drop correction to the simulation for current densities up to 10^5 A/cm^2. Curve a is the traditional simulation, curve b is the simulation corrected for the lateral voltage drop in the n^+ buried layer, data points shown by X are the measured results, and curve c corresponds to the expected current with no conductivity modulation.

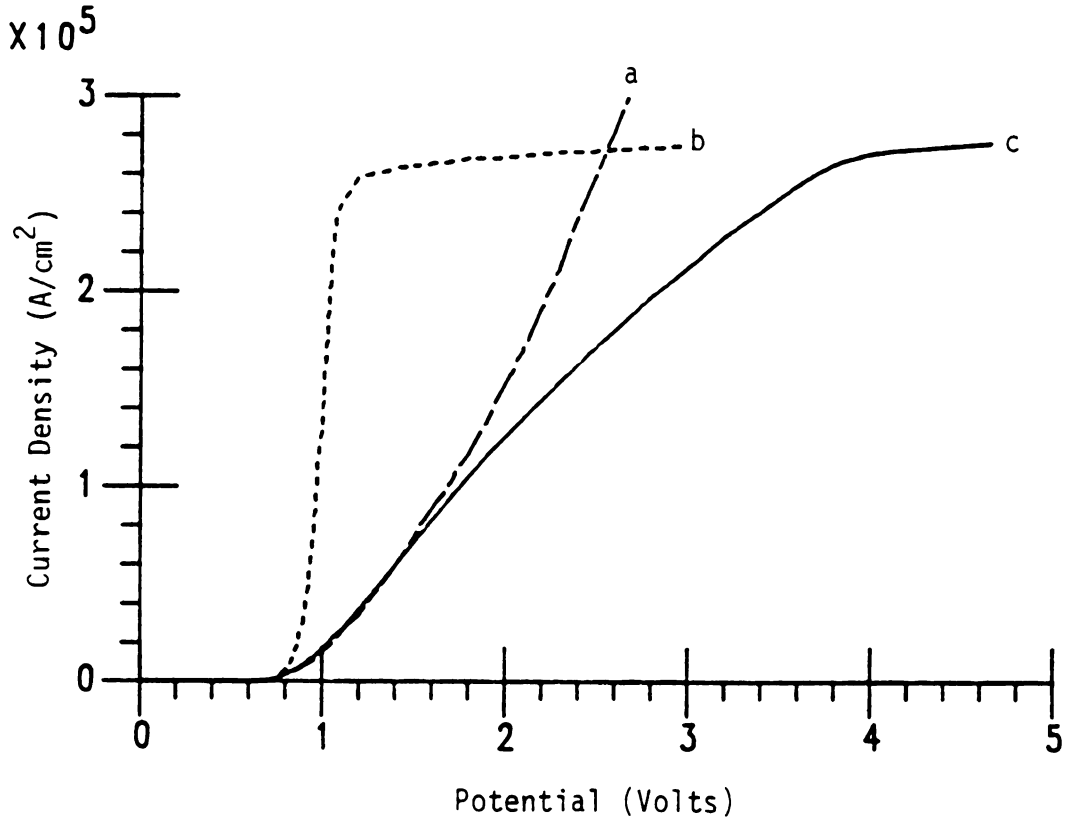


Figure 6-7 Comparison of the lateral voltage drop corrected simulation and experiment for an extended bias range. (a) Shows the measured results, (b) corresponds to the traditional simulation, and (c) corresponds to the simulation corrected for lateral voltage drop.

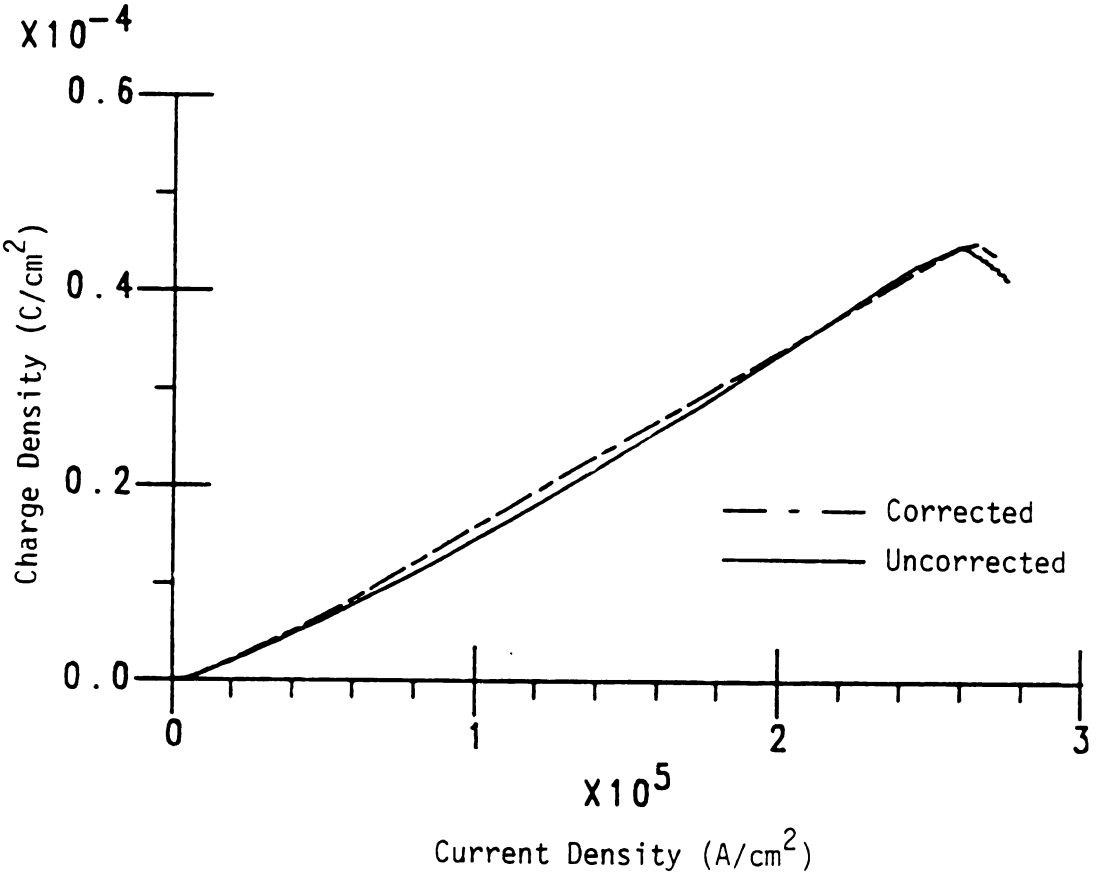


Figure 6-8 Simulation results for the charge density of stored minority carriers with and without correction for the lateral voltage drop.

charge density is close to being linear. Therefore, the average charge density of stored minority carriers vs. the average current density is close to the values calculated by the traditional simulation, which neglects lateral voltage drop. It must be noted, however, that the distribution of the excess stored carriers in the lateral direction is very non-uniform since the current flow in that direction is not uniform.

6.3.4 Additional Remarks

Minority carrier injection is sometimes characterized by the injection ratio, γ, defined as the ratio of minority carrier current and the total current. Figure 6-9 shows the simulation results for γ vs. forward current density. Injection coefficients close to 0.3% are obtained at 10^5 A/cm^2.

As a result of the lateral voltage drop, the current density and minority carrier storage vary significantly in the lateral direction. In fact, most of the current and most of the stored charge is due to the last few diodes in the model of Figure 4-5. Consequently, for good high injection performance, the SBD should be designed with a high anode periphery to reduce the lateral drop. A long, narrow SBD will have a more homogeneous current distribution, and presumably better reliability than a square layout.

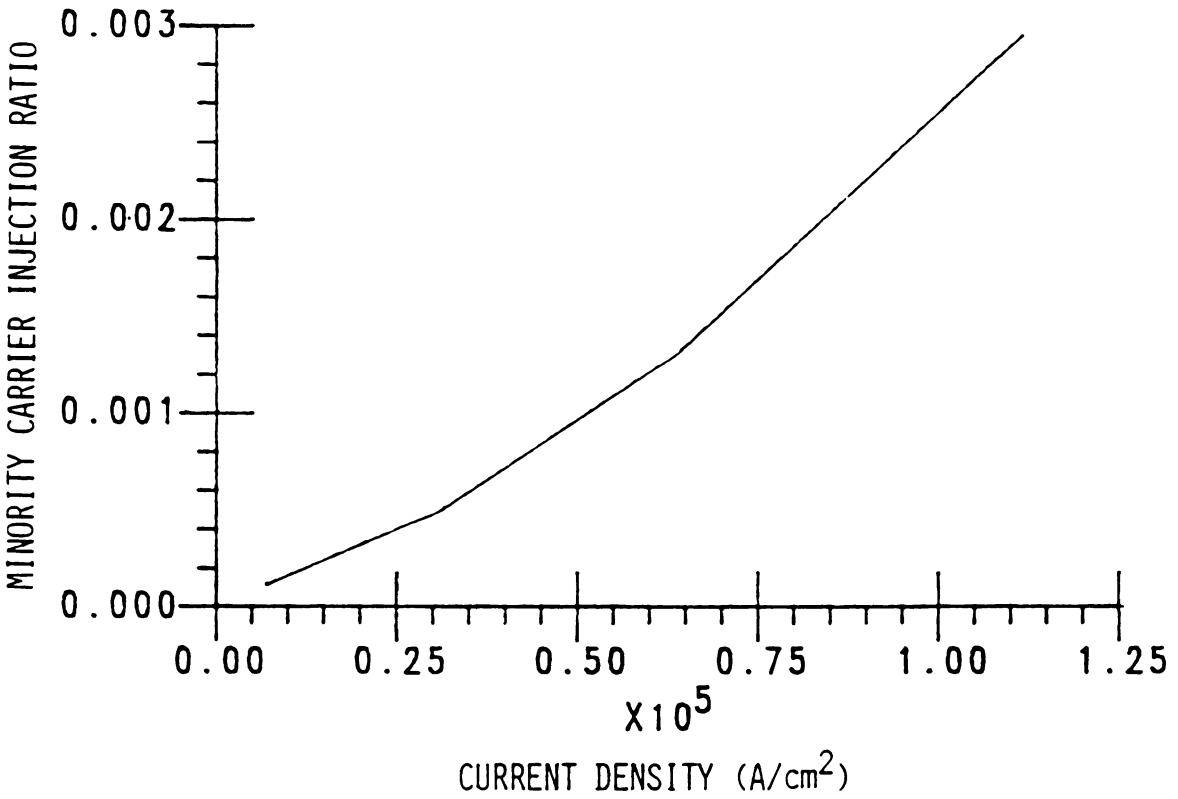


Figure 6-9 Traditional simulation results for the minority carrier injection ratio.

6.4 Boundary Condition Corrections

6.4.1 The Simulation Method

Further modifications to the simulation arise from the effect of the image-force on the valence band which, as discussed in Chapter 4, results in the shrinkage of the semiconductor band-gap near the metal-semiconductor interface and also leads to hole barrier height lowering and hole tunneling through the barrier at high injection. In the modification of the simulation presented in this section, band-gap shrinkage and hole barrier height lowering effects have been considered. To do so, n_o and p_o which are used in the current density boundary conditions (Equations 4-17 and 4-18) have been calculated using Equations 4-23 and 4-24 for bias levels below the flat-band condition and using Equations 4-28 and 4-28 beyond flat-band. Due to the added complexity to the simulation, the effect of hole tunneling at high injection has not been considered.

6.4.2 Current-Voltage Comparison

This additional modification of the simulation has an insignificant effect on the low bias region of the current-voltage characteristics where minority carrier injection is negligible, but has an appreciable effect beyond about 10^5 A/cm^2. Figure 6-10 shows the simulated and measured J-V characteristics of the device and shows that the modified simulation remains in excellent agreement with the experiment at low bias as expected. To observe the high injection behavior of the simulation, the J-V results are shown in a linear plot

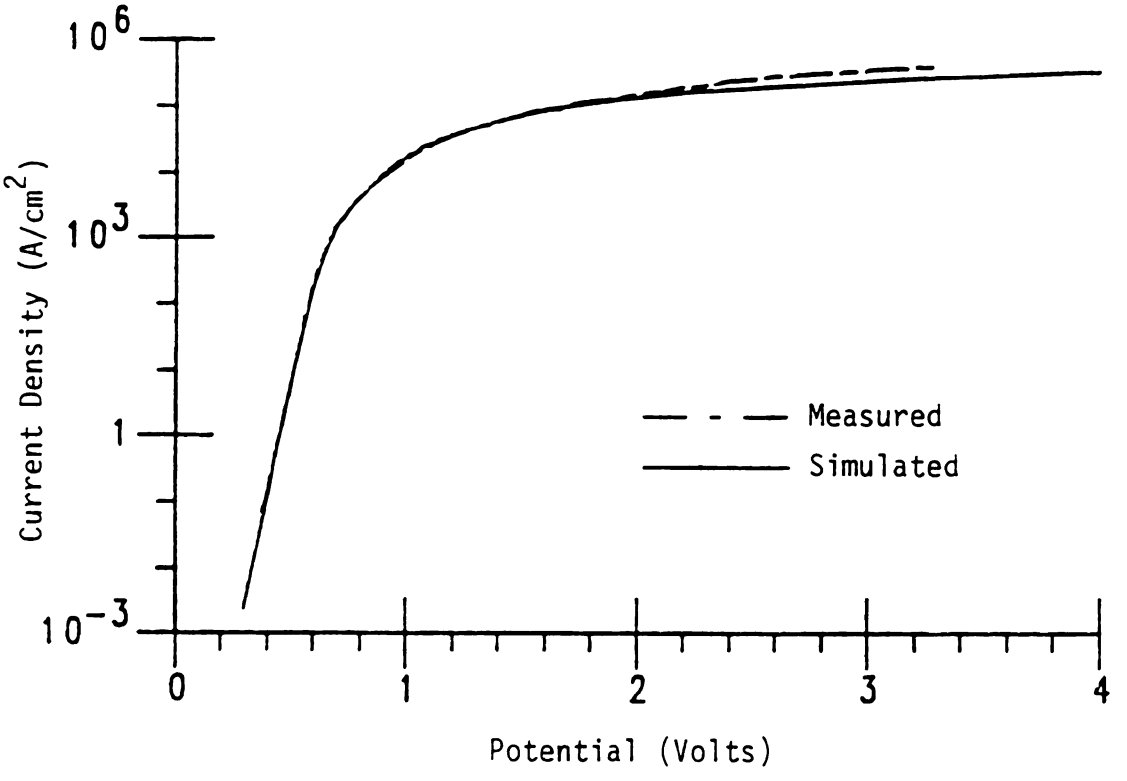


Figure 6-10 Comparison of simulated and measured J-V characteristics with the simulation including the effects of lateral voltage drop, image-force induced bandgap shrinkage, and hole barrier height lowering.

in Figure 6-11. As seen in this figure, the new modification extends the region of agreement between simulation and experiment to current densities up to 1.2 X 10^5 A/cm^2. Furthermore, beyond 1.2 X 10^5 A/cm^2, the modification changes the simulation results in the right direction. Figure 6-12 covers even higher values of current density and shows that the plateau in the current values of the previous simulation is no longer observed in the modified simulation.

As discussed in the previous section, tunneling of holes through the barrier at high injection was not included in the simulation. The tunneling effect can potentially account for much of the difference between simulated and measured current-voltage characteristics at high injection. Tunneling of holes through the barrier results in additional minority carrier current and a larger excess carrier storage which would, in turn, result in more conductivity modulation and consequently, even higher currents. Impact ionization and shortcomings of the one-dimensional approximation could also account for some of the discrepancy between simulation and experiment at very high injection.

6.4.3 Stored Minority Carrier Comparison

Figure 6-13 shows the results of the traditional simulation and the modified simulation. As is evident from this figure, at high injection more minority carrier storage is predicted by the modified simulation and the peak observed in the previous simulation is no longer observed. These observations are consistent with the J-V observations regarding an increase of current and the absence of a plateau at high injection, since the plateau in the J-V characteristics corresponds to the peak in the carrier storage results. It is also

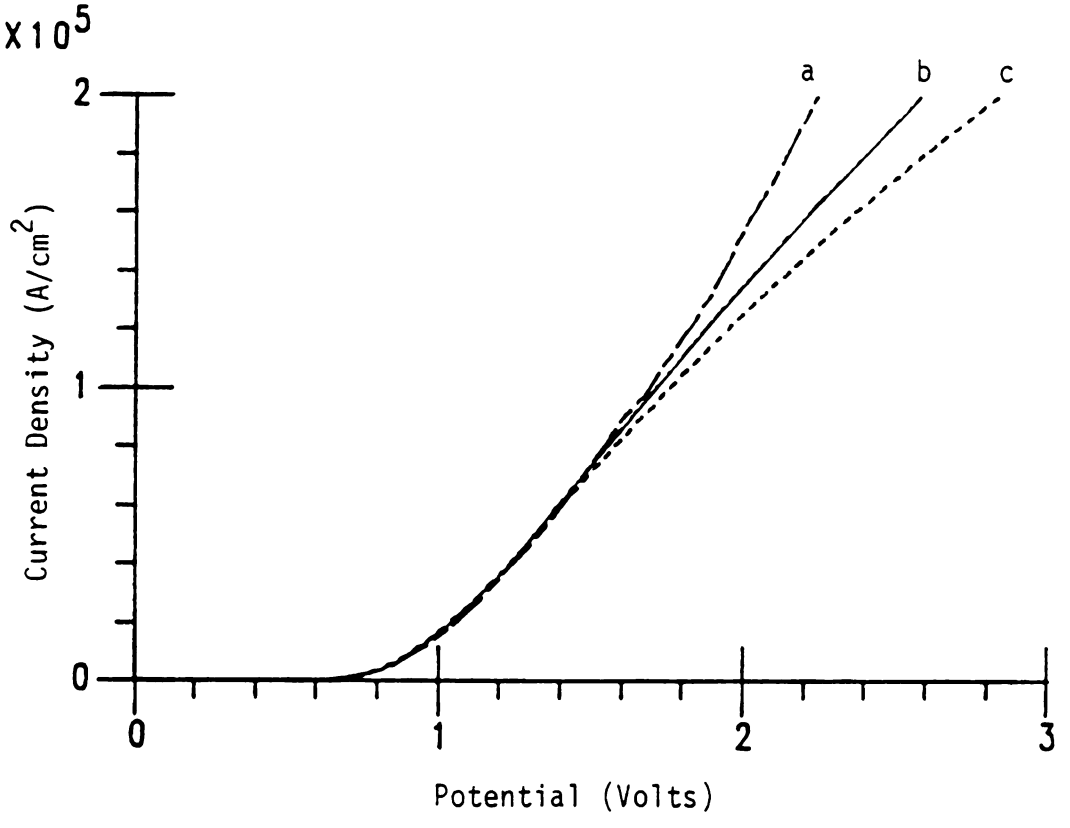


Figure 6-11 Linear plot of the current-voltage characteristics comparing the measured results (curve a), the simulation corrected for the lateral voltage drop only (curve c), and the simulation corrected for lateral voltage drop as well as the image-force induced bandgap shrinkage and the hole barrier height lowering (curve b).

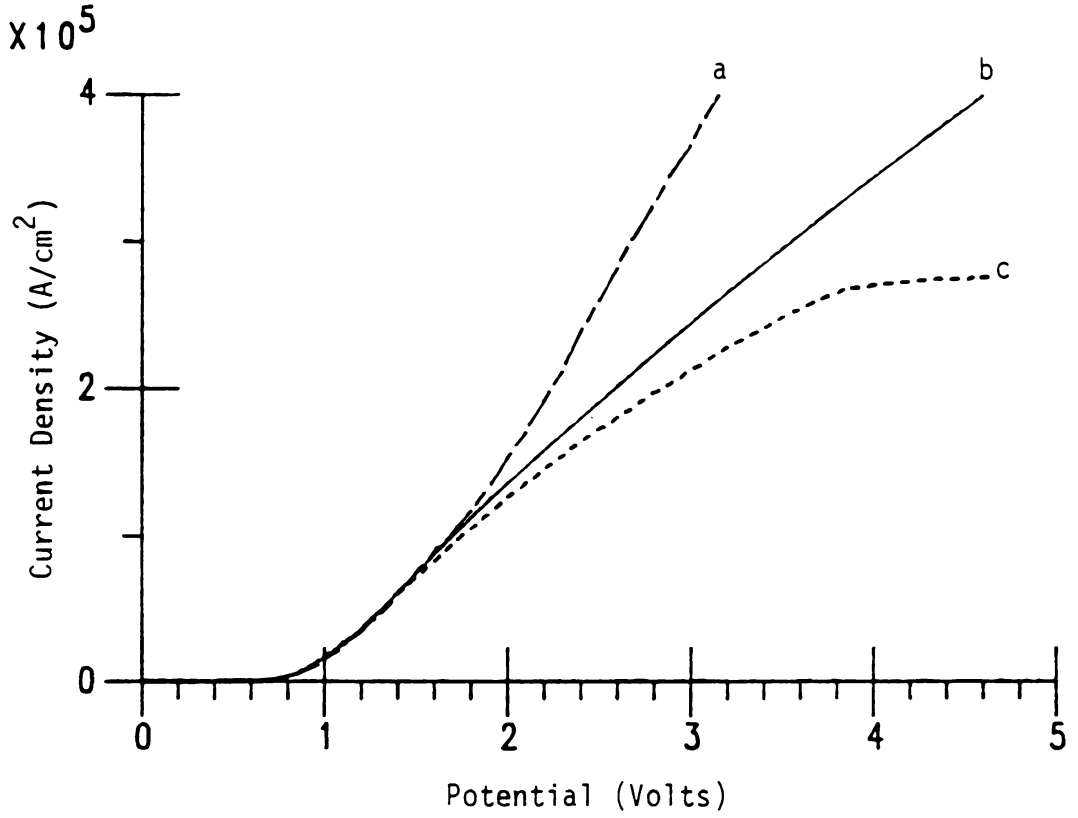


Figure 6-12 Plot of the current-voltage characteristics over an extended range and comparing the measured results (curve a), the simulation corrected for the lateral voltage drop only (curve c), and the simulation corrected for lateral voltage drop as well as the image-force induced bandgap shrinkage and the hole barrier height lowering (curve b).

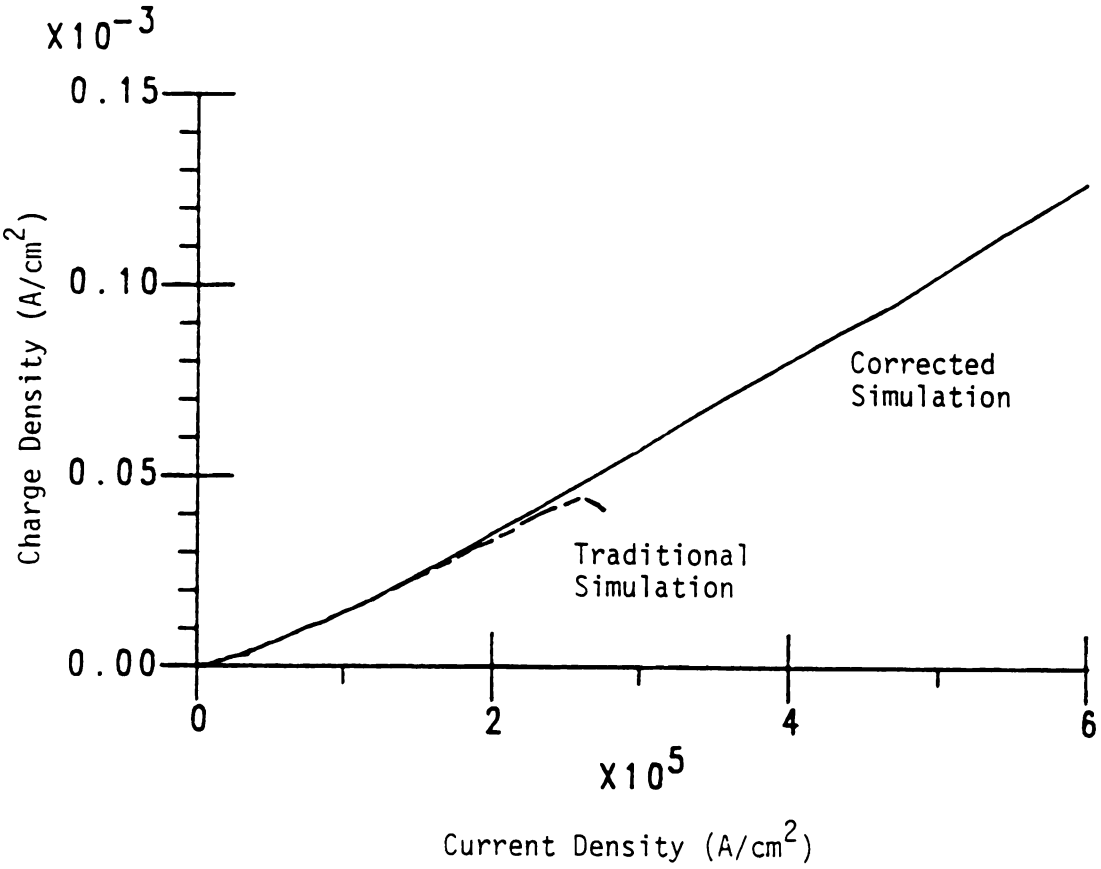


Figure 6-13 Comparison of minority carrier charge-storage results between the traditional simulation and the simulation corrected for image-force induced bandgap shrinkage and hole barrier height lowering.

evident from Figure 6-13 that this modification of the simulation has a negligible effect in the range of current densities where experimental charge storage data is available (up to 10^5 A/cm^2).

6.5 Consideration of Auger Recombination

6.5.1 The Simulation Method

Auger recombination in silicon is significant only at high values of carrier concentration, and therefore has been considered in the literature in simulations of heavily doped materials [55,56], as well as simulations of devices under high injection [57,58,59]. The values reported for the Auger coefficient (parameter g in Equation 4-14), vary in the range of 10^{-31} to 7 X 10^{-31} cm^6/sec [34,55,57,58,60,61].

To include Auger recombination in the simulation, the corresponding recombination rate given by Equation 4-14, has been added to the previously considered trap-assisted recombination rate. A value of 10^{-31} cm^6/sec has been used for the Auger coefficient to obtain a qualitative measure of the effect of the phenomenon. For simplicity, the traditional simulation without the consideration of boundary condition corrections has been used here.

6.5.2 Effect of Auger Recombination on the Simulation

Figures 6-14 and 6-15 show the simulation results of the current-voltage characteristics and the minority carrier stored-charge vs. forward current with and without Auger recombination. Ignoring the peaks in charge storage and the plateaus in J-V results which, as

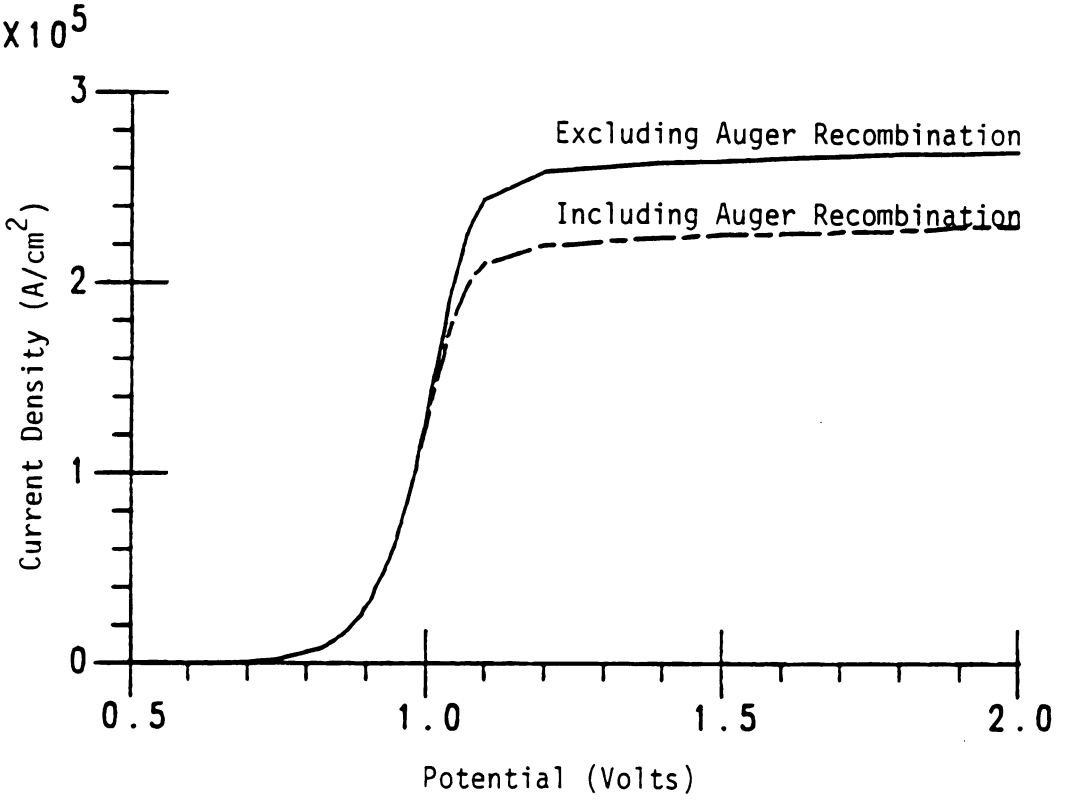


Figure 6-14 Current-voltage characteristics resulting from the traditional simulation with and without consideration of Auger recombination.

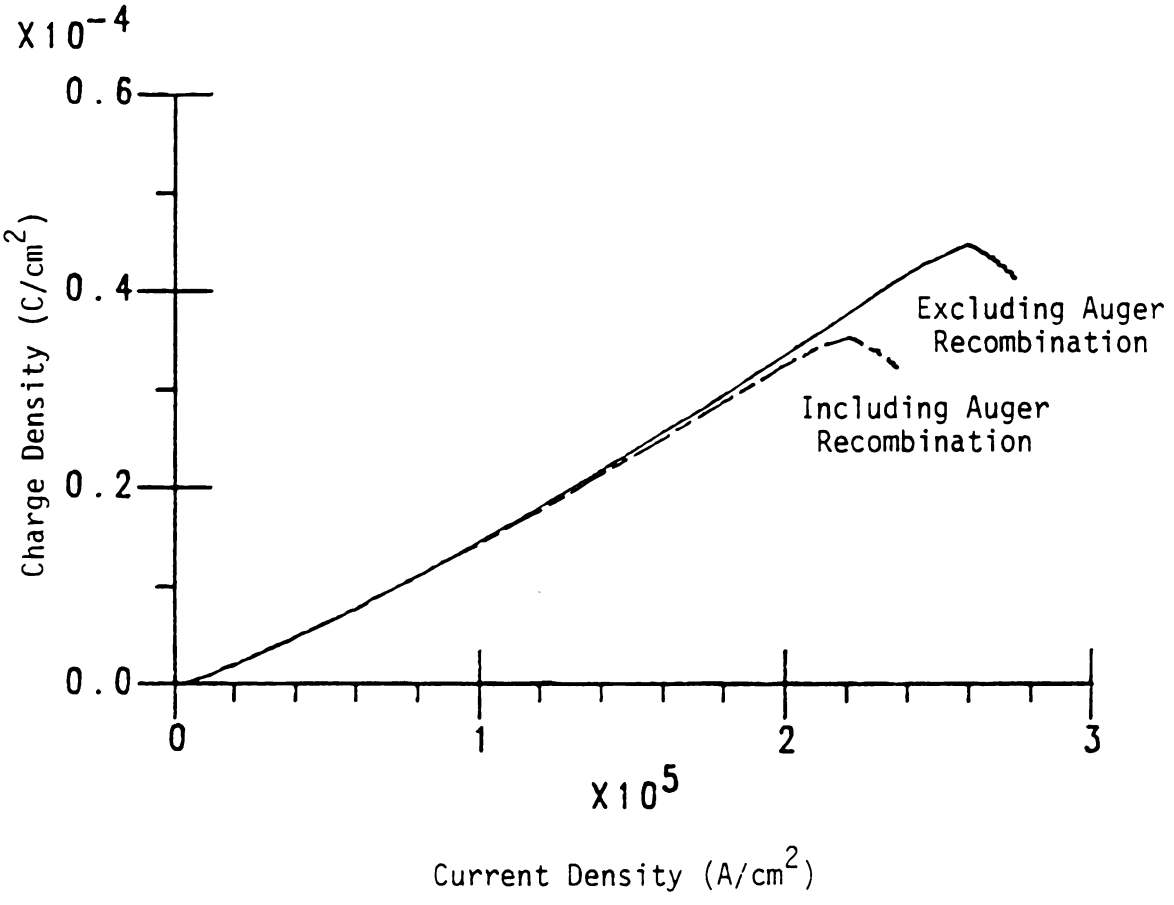


Figure 6-15 Minority carrier stored-charge density results from the traditional simulation with and without consideration of Auger recombination.

discussed in section 6.2, are artifacts of the traditional simulation, the Auger recombination is shown to have a small effect at high injection and a negligible effect at lower injection levels. Specifically, Figure 6-15 shows that in the range of current density for which experimental data is available (up to 10^5 A/cm^2), Auger recombination is insignificant in the simulation.

6.5.3 Effect of Auger Recombination on Experiment

As discussed in chapter 3, the accuracy of the minority carrier charge storage measurement depends on the ability of the switching circuit to sweep all the excess minority carriers out before they are recombined. In other words, the minority carrier lifetime must be much larger than the time involved in the reverse recovery, or alternatively, the diffusion length of the minority carriers must be much larger than the depth of the bulk. The hole lifetime, τ_p, and the hole diffusion length, L_p, due to Auger recombination are given by

$$\tau_p = 1/gn^2 \qquad (6\text{-}1)$$

and

$$L_p = [D_p \tau_p]^{1/2} \qquad (6\text{-}2)$$

where D_p is the hole diffusion coefficient.

Tables 6-1.a and 6-1.b show calculated values of hole Auger lifetime and diffusion length for two values of carrier concentration (10^{18} and 10^{20} cm^{-3}). Table 6-1.a corresponds to the lower limit of the Auger coefficient (10^{-31} cm^6/s), and Table 6-1.b corresponds to the the upper limit of the Auger coefficient (7 X 10^{-31} cm^6/s). As can be seen

Table 6-1 Hole Auger lifetimes and Auger diffusion lengths in silicon under various conditions. (a) For Auger coefficient, $g = 10^{-31}$ cm^6/s, (b) for $g = 7 \times 10^{-31}$ cm^6/s.

n	10^{18} cm^{-3}	$10^{20} cm^{-3}$
τ_p	10 μs	1 ns
L_p	1.01×10^{-2} cm	0.13 μm

(a)

n	10^{18} cm^{-3}	10^{20} cm^{-3}
τ_p	1.43 μs	143 ps
L_p	3.8×10^{-3} cm	0.05 μm

(b)

from these tables, for an electron concentration of 10^{18} cm^{-3}, the Auger hole lifetime is on the order of μs and the corresponding diffusion length is on the order of 10^{-3}cm. Therefore, compared to a few ns of reverse recovery and a bulk depth on the order of μm, Auger recombination is insignificant for this level of electron concentration. For an electron concentration of 10^{20} cm^{-3}, however, Auger lifetime is a nanosecond or less and the diffusion length is on the order of 0.1 μm. Therefore, Auger recombination is significant at this level of electron concentration.

Figure 6-16 shows the simulation results for the minority carrier profile in the device at a forward current density of about 10^5 A/cm^2, which is the upper limit of the range in which experimental data for minority carrier storage is available. This figure points to two important observations. First, at this current level, the highest value of excess carrier concentration in the epitaxial region ($0 \leq x \leq 1$ μm) is only about 1.8×10^{18} cm^{-3}. So, following the above discussion, at least up to this current density level, Auger recombination in the epitaxial region is negligible. The second observation from Figure 6-16 is the fact that a significant amount of excess carriers are stored in the n^+ region ($x > 1$ μm). The doping concentration in this region, as previously shown in Figure 3-2, increases from 10^{17} cm^{-3} to beyond 10^{20} cm^{-3}. Therefore, Auger recombination is significant in this region during the reverse recovery measurement and some of the excess carriers stored in the buried n^+ region may recombine before being collected by the switching circuit.

Figure 6-17 shows the simulation results for total stored-charge and epitaxial-only stored-charge as compared to experiment. As would be expected, the experimental values are between the two simulation

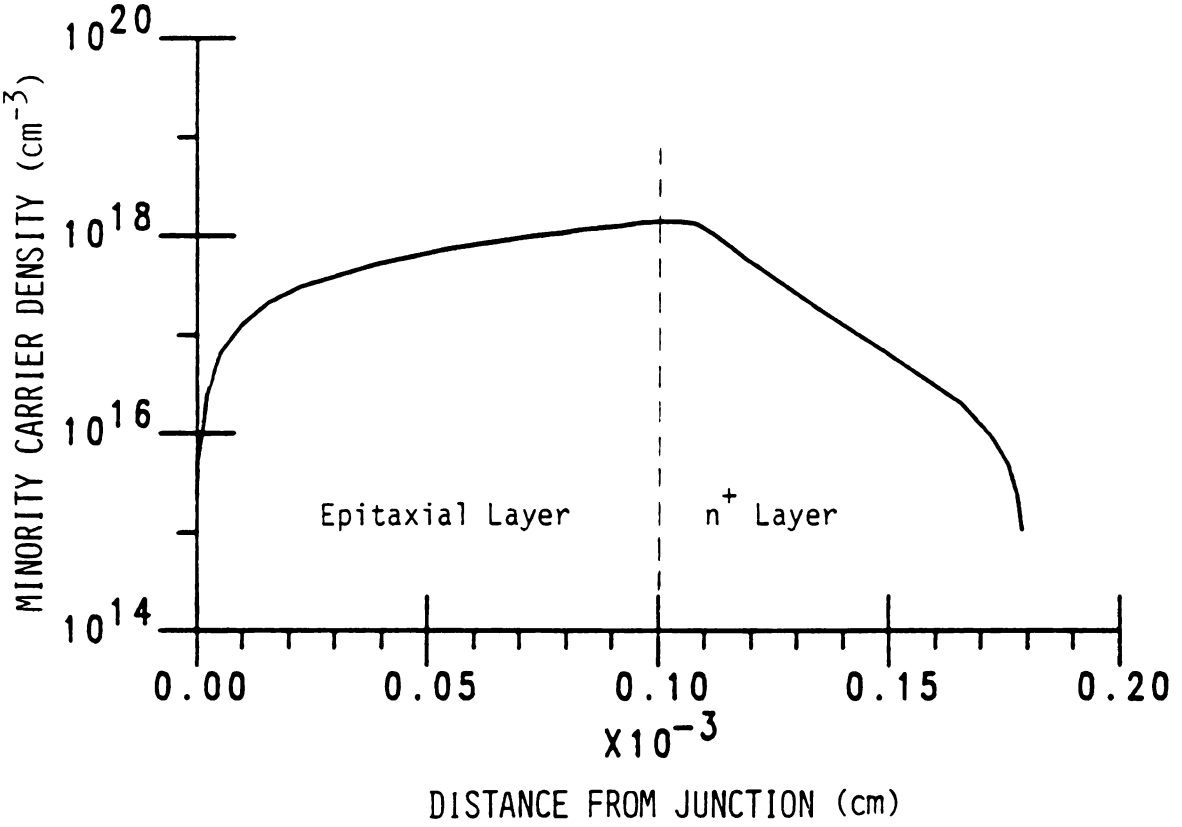


Figure 6-16 Traditional simulation results for minority carrier profile at a forward current density of 1.1 X 10^5 A/cm^2 (from C.C. Yu [4]).

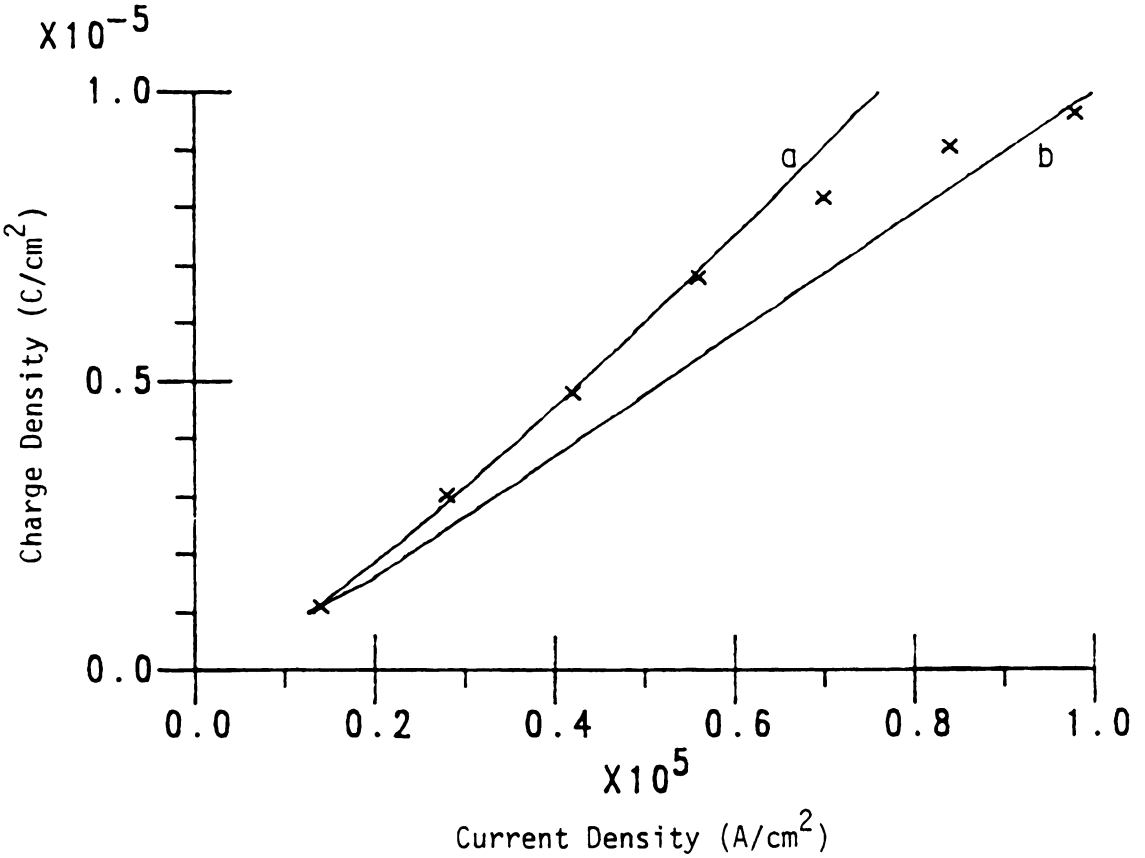


Figure 6-17 Comparison of minority carrier stored-charge density results of the traditional simulation and experiment. Curve a shows the simulation results considering the epitaxial region only, curve b shows the simulation results for the total device, and the experimental data points are shown by X.

results since some, but not all, of the excess carriers in the n^+ layer are collected experimentally.

6.6 High Temperature Comparison

Figures 6-18 and 6-19 show the simulation results at 27, 85, 100, and 125 °C. The J-V results shown in Figure 6-18 show that the simulation predicts more current as temperature increases, and the minority carrier storage results shown in Figure 6-19 show that the simulation predicts more charge storage for increased temperatures. Therefore the simulation results show the same trend for device behavior vs. temperature as the experiment (see Figure 3-10 and 3-15). The agreement between simulation and experiment at elevated temperatures, however, is not as good as that of room temperature. Figures 6-20, 6-21, and 6-22 show the J-V comparison of simulation and experiment at 85, 100, 125 °C respectively, and Figures 6-23, 6-24, and 6-25 show the minority carrier charge storage comparison at those temperatures. The observed discrepancies between simulation and experiment at elevated temperatures are believed to be due to a shortcoming in the simulation to properly account for temperature dependent phenomena. All of the simulation results presented in this section (Figures 6-18 to 6-25), correspond to the traditional simulation corrected only for the lateral voltage drop since, as previously demonstrated, other corrections to the simulation are significant at current densities beyond 10^5 A/cm^2, and the available experimental data at elevated temperatures do not exceed that level of current density.

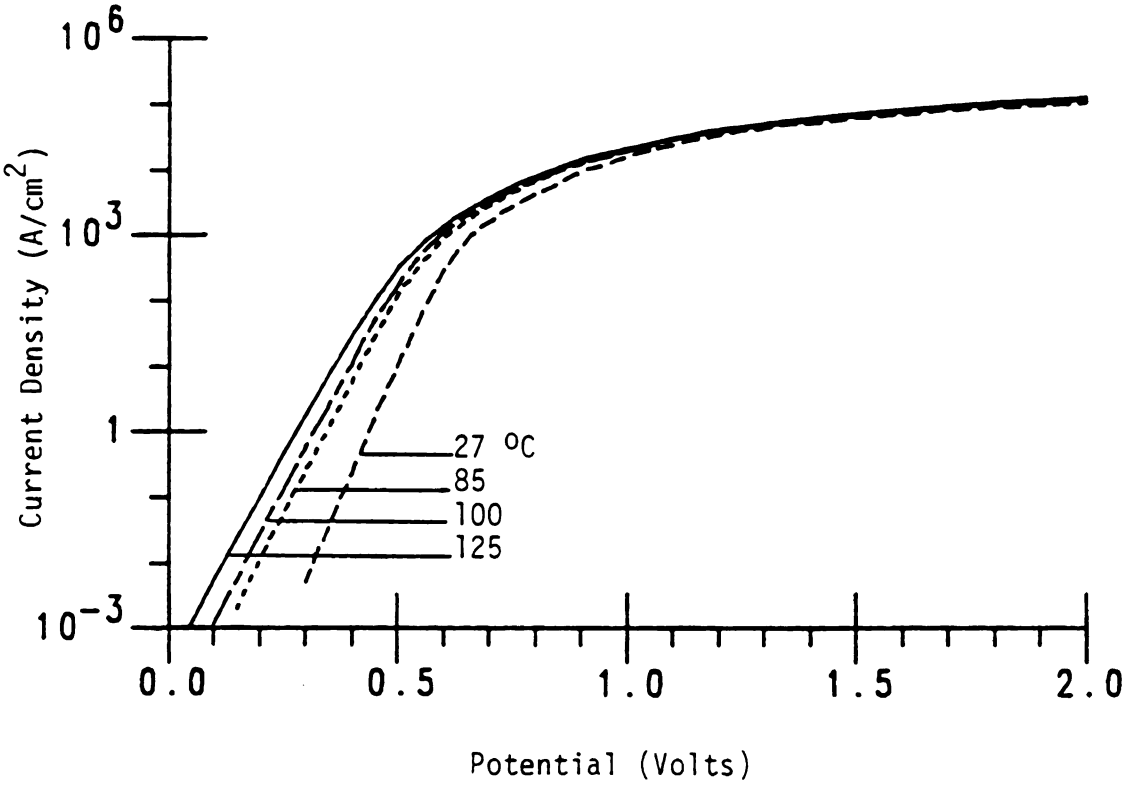


Figure 6-18 Traditional simulation results for the J-V characteristics of the device at four temperatures.

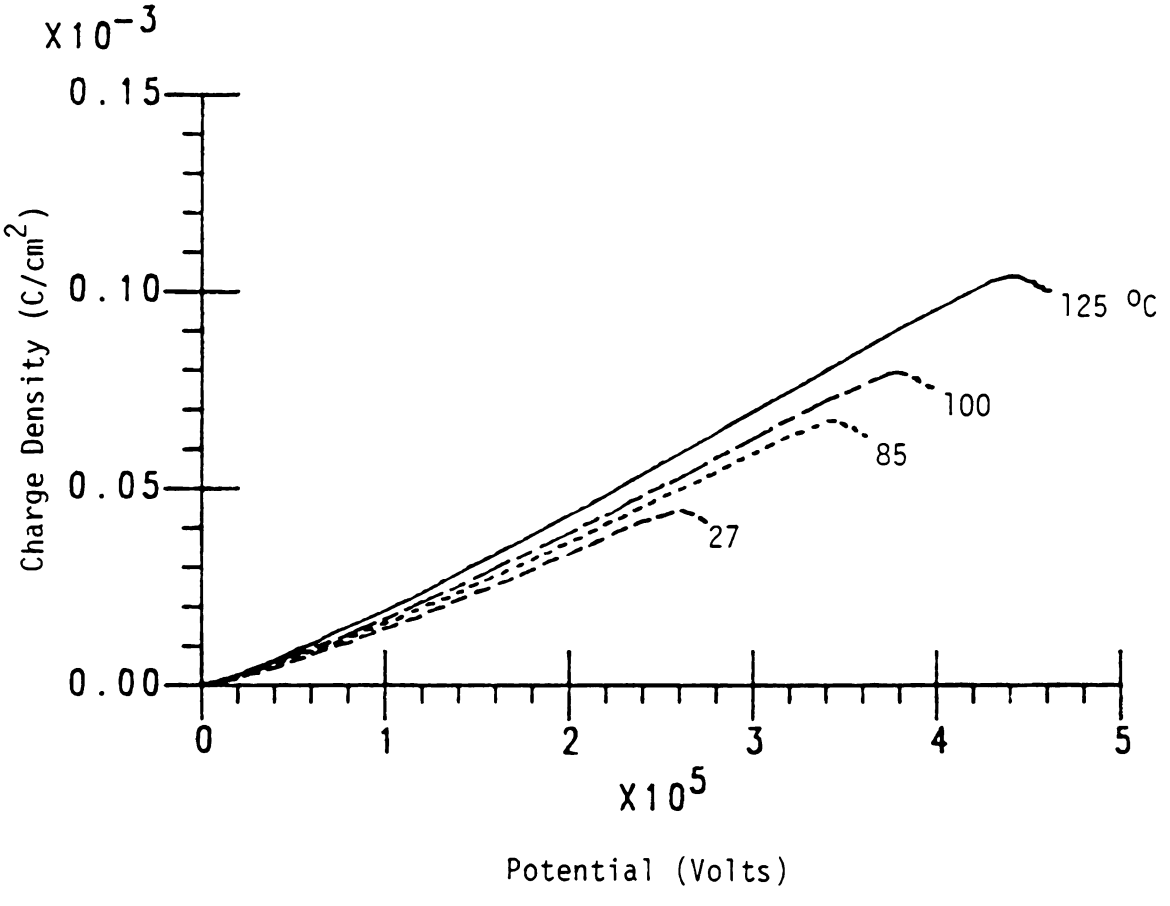


Figure 6-19 Traditional simulation results for the minority carrier stored-charge density at four temperatures.

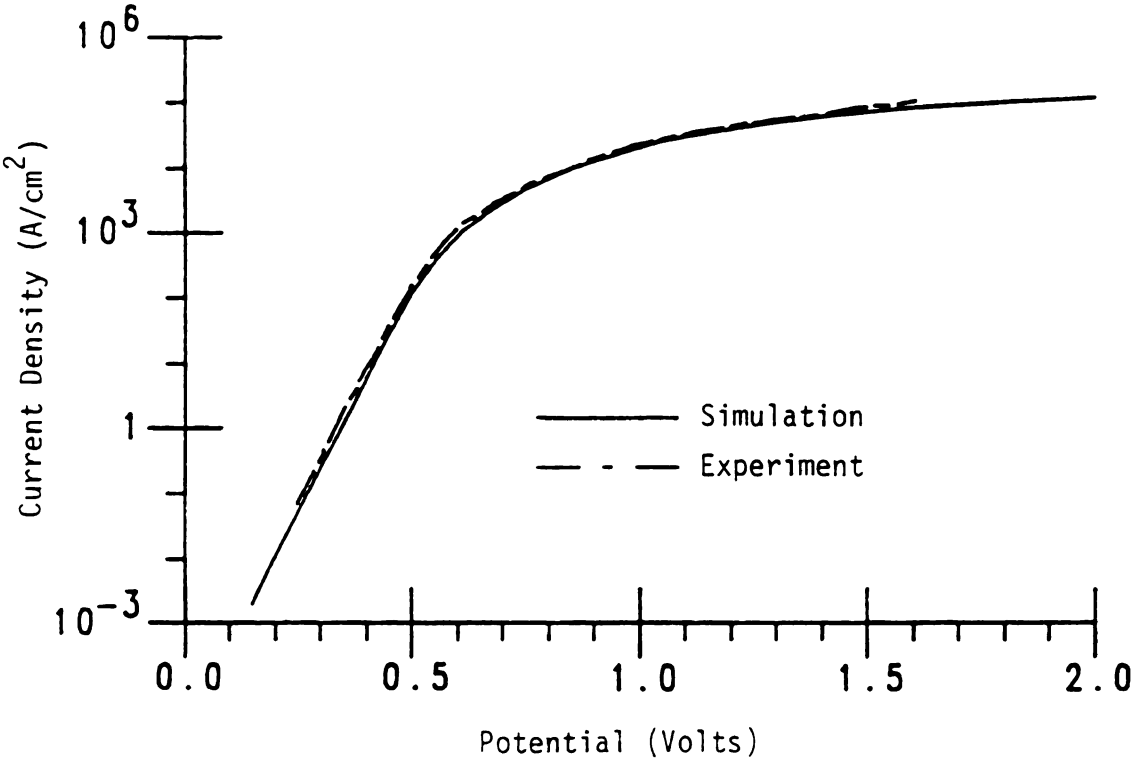


Figure 6-20 Comparison of the J-V characteristics obtained from the traditional simulation and experiment at 85 °C.

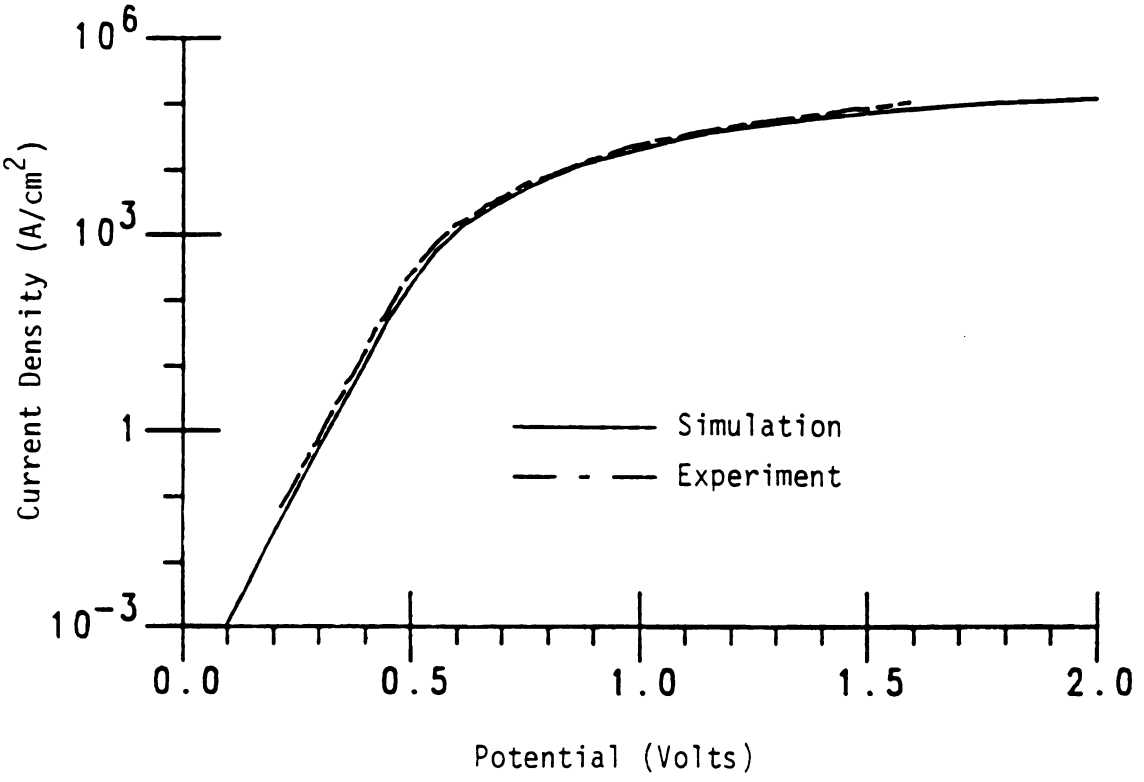


Figure 6-21 Comparison of the J-V characteristics obtained from the traditional simulation and experiment at 100 °C.

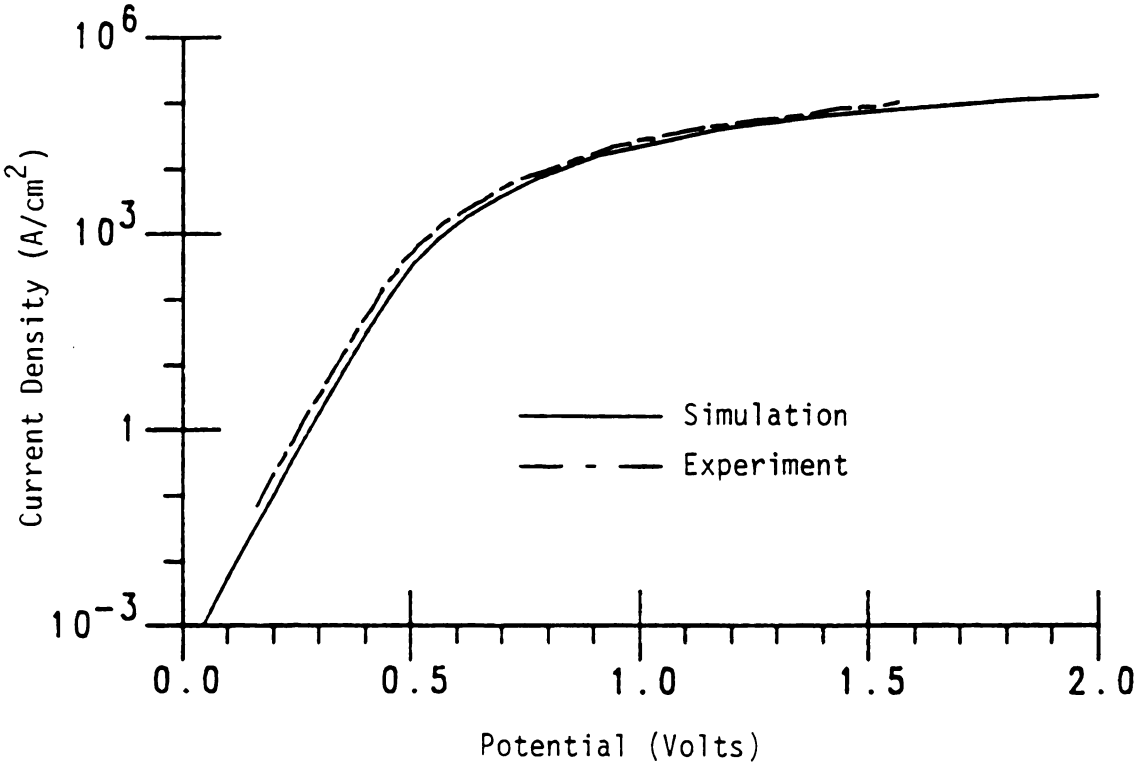


Figure 6-22 Comparison of the J-V characteristics obtained from the traditional simulation and experiment at 125 °C.

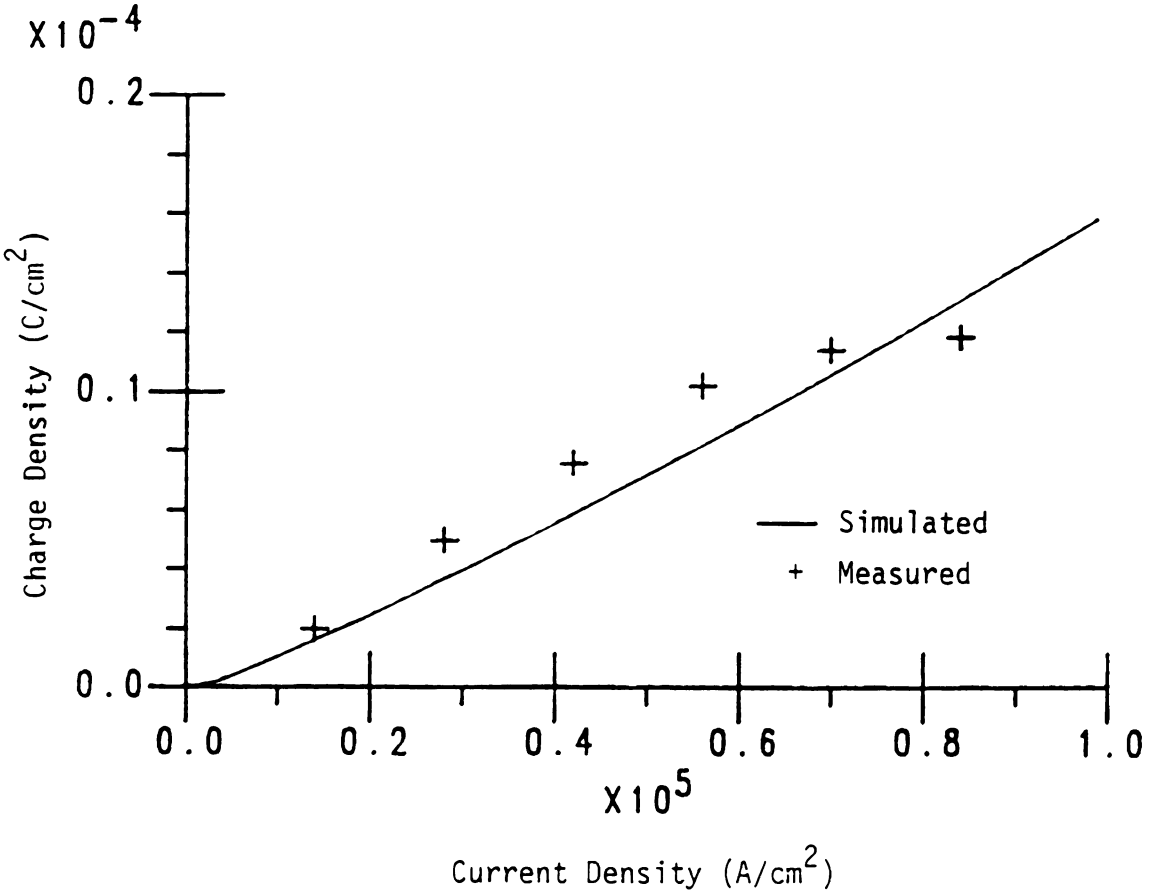


Figure 6-23 Comparison of the minority carrier stored-charge density obtained from the traditional simulation and experiment at 85 °C.

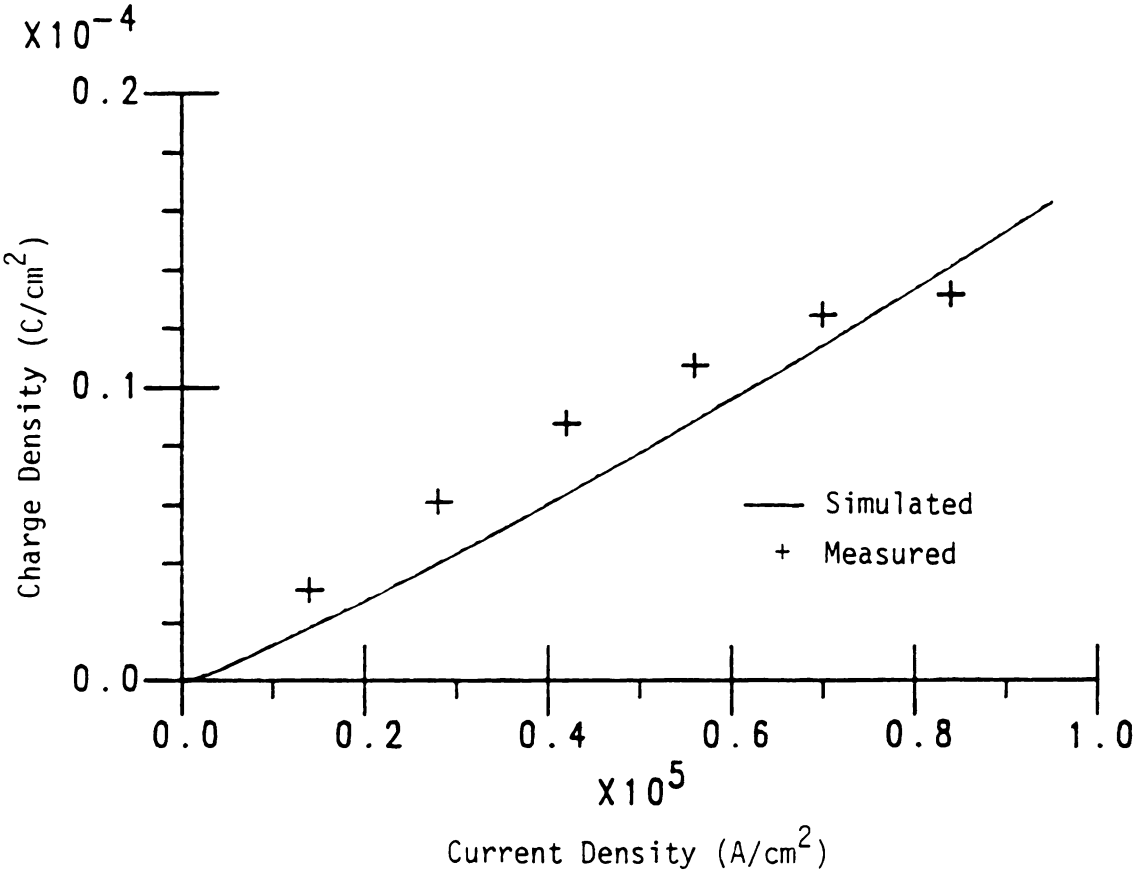


Figure 6-24 Comparison of the minority carrier stored-charge density obtained from the traditional simulation and experiment at 100 °C.

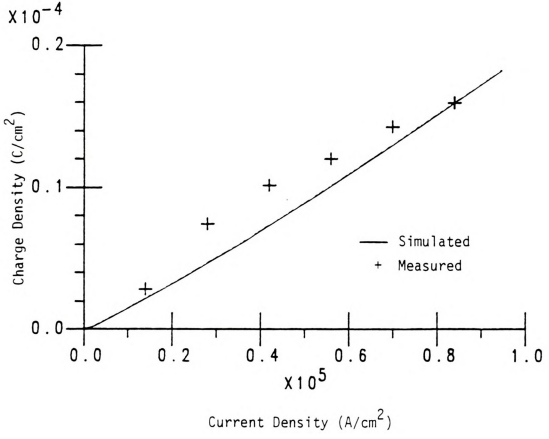


Figure 6-25 Comparison of the minority carrier stored-charge density obtained from the traditional simulation and experiment at 125 °C.

CHAPTER SEVEN

CONCLUDING REMARKS

7.1 Summary of Major Results and Conclusions

Steady-state dc minority carrier storage and conductivity modulated J-V characteristics of platinum-silicide Schottky barrier diodes are determined experimentally and compared with results from a numerical simulation. The experimental method for measuring the minority carrier storage uses a high time resolution switching circuit to measure the reverse-recovery response of the diode. The reverse-recovery current is then integrated to measure the total charge swept out of the device. The total charge is subsequently corrected for parasitic capacitance effects to yield the charge associated with stored minority carriers. The reverse-recovery measurement, as well as the high current density portion of the J-V measurement, is performed

using a train of pulses with a very low duty cycle to avoid self-heating. The J-V measurement is done using a four terminal technique to avoid errors in voltage measurement, caused by the parasitic resistance of the leads connecting the device to the circuit. The carrier storage results extend to current densities as high as 10^5 A/cm^2 and the J-V characteristics are measured up to 4 X 10^5 A/cm^2. Guarded SBDs show considerably more minority carrier storage than do unguarded SBDs.

The barrier height of the device is an important input parameter in the simulation of the device and therefore, three methods have been compared for calculating the value of the barrier height from the forward bias I-V data. The Richardson's constant method and Norde's method were modified to account for barrier lowering and the modified Norde's method was shown to generate accurate results as determined by its self-consistency. The barrier height of a representative platinum-silicide Schottky diode was determined to be 0.881 V at room temperature and to increase with increasing temperature with a coefficient of about 2.3 X 10^{-4} V/K. Less accurate were the modified Richardson's constant method and the activation energy method. While the former was shown to be able to generate accurate results for devices with barrier lowering as their only non-ideal effect, the latter method is only useful for obtaining an estimate of the barrier height at zero temperature.

The device simulation is for the unguarded SBD, and is based on a one dimensional numerical solution of the basic equations governing steady-state carrier transport in the device. Both simulation and experiment show considerable conductivity modulation and charge storage due to minority carrier injection. The one dimensional simulation using traditional boundary conditions shows considerable discrepancy with the

measured J-V data at high current densities. However, when corrected for lateral voltage drop, energy gap shrinkage near the barrier, and barrier height lowering for holes, the simulation agrees with experimental current-voltage characteristics for current densities up to 1.2×10^5 A/cm^2. At higher bias levels, more current is measured than predicted by the simulation. The major contributor to the discrepancy is believed to be hole tunneling at high injection which is not considered by the simulation. A boundary condition is developed which approximates hole tunneling using a WKB approximation and a triangular barrier. Two dimensional effects beyond the lateral voltage drop, and impact ionization are other potential sources of the high injection discrepancies. The stored minority carrier measurements agree with simulation up to about 6×10^4 A/cm^2. Beyond that, Auger recombination in the buried layer prevents some of the stored minority carriers from being measured in the reverse-recovery experiment. The measured stored charge at high injection is found to lie between simulation results for charge storage only in the epitaxial region, and charge storage in the overall device.

The fraction of forward current due to minority carriers is small. Simulation results show that the minority carrier injection ratio is about 0.3% at 10^5 A/cm^2. However, this degree of injection causes appreciable conductivity modulation which has a large effect on the I-V characteristics. It also leads to stored charge densities on the order of 10^{-5} coulombs/cm^2 which must be removed from the device on switching from forward to reverse bias. If reverse switching currents are on the order of 10^4 A/cm^2, the time required to remove the minority carriers is on the order of ns. For the reverse-recovery experiments in this study, the majority of stored excess carriers were observed to

discharge during the first two ns, but a secondary discharge of minority carriers lasting a few additional ns was observed.

For the nearly square SBDs in this study, high injection lateral voltage drops are significant and the current density is highly non-uniform in the lateral direction. In narrow devices, this effect would be reduced.

7.2 Suggestions for Further Investigations

The steady-state simulation may be improved in several ways. The tunneling boundary condition, developed in this work for hole tunneling under high injection, may be incorporated in the simulation to achieve better agreement with experiment at high current densities. Also, the lateral voltage drop can be considered more properly by a two dimensional simulation instead of the multiple resistor model presented here. As the device area gets much smaller, edge effects become more significant and a three dimensional simulation may be necessary to account for such phenomena.

While the steady-state simulation calculates the amount of excess minority carriers stored in the device, no direct information about the transients of switching, such as the primary and secondary discharge observed in this work, is obtained. A transient numerical simulation would provide such information and would prove useful in investigating possible correlations between device geometry and reverse-recovery.

While device simulations provide a considerable amount of information about the expected device behavior, the ultimate objective is to develop proper circuit models, which are much simpler to use in aiding device and circuit design. Present available models are based on

the traditional simulation and do not account for the corrections developed by this work [13]. Therefore, a better device model may be developed. The model presented here for lateral voltage drop may be useful to that end.

As shown in Chapter 6, a significant amount of the stored excess carriers recombine in the n^+ buried layer before being collected by the switching circuit in the charge storage measurement. Elimination of this problem requires a significant amount of speed improvement over the already fast switching circuit. Therefore, extending the range of carrier storage data to higher current densities may prove extremely difficult. The J-V data, however, may be extended to a higher level of current density with the use of a better differential measurement set-up.

APPENDICIES

APPENDIX A

DETAILS OF EXPERIMENT

A.1 Krakauer's Method

The circuit used for this measurement is shown in Figure A-1. The primary purpose of this circuit was to excite the test diode with a sinusoidal input. At current levels where minority carrier injection was found to be significant, however, the continuous sine wave damaged several test devices. Therefore, instead of the continuous sine wave, a sinusoidal burst was used to reduce the average power delivered to the test device. The pulse generator shown in Figure A-1 (Hewlett-Packard 214), was set to generate a train of pulses with a pulse width of 50 μs and a repetition rate of 1 KHz. The pulse train, in turn, was taken to the modulation input of the signal generator (Wavetek 2000) and consequently, the output of the signal generator was bursts of

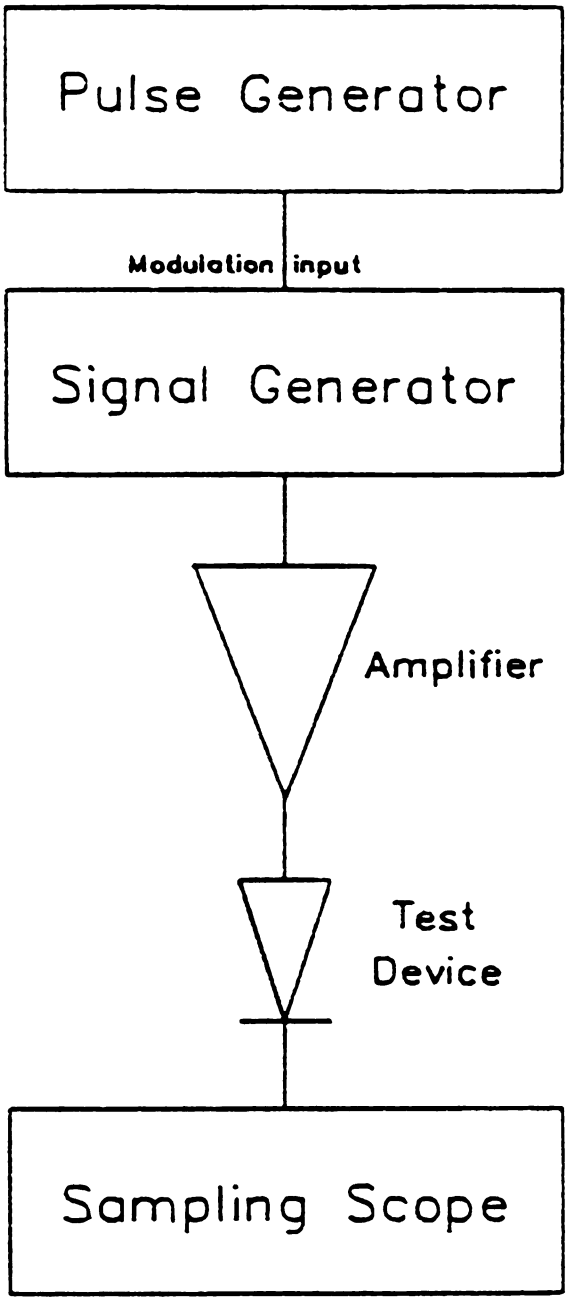


Figure A-1 Diagram of the circuit for measurements using Krakauer's method.

sinusoidal signal generated every ms and lasting 50μs. The signal generator was set for a frequency of 50 MHz.

The sinusoidal signal had to be amplified to generate enough current to be able to drive the test device into high injection. The amplifier used for this purpose was part of the trigger take-off circuitry of a Tektronix 110 pulse generator. The output of the amplifier was used to drive the test diode which was loaded with the 50Ω internal input impedance of the sampling oscilloscope. A Tektronix 661 sampling oscilloscope with type 4S1 sampling heads was used to observe the current through the test device.

A.2 Charge Integration Measurement

A.2.1 The Circuit

The circuit used for the charge integration measurement has been previously shown in Figure 3-4. The pulse generator used in this circuit was a Tektronix 109 model with a rise time of 250 ps. This pulse generator operates by discharging a transmission line (a coaxial cable in this case) using a mechanical mercury reed switch. The pulse amplitude is determined by the voltage to which the delay line is charged , and the pulse width is determined by the length of the delay line as Figure A-2 shows. The pulser can use two delay lines, but since a low noise display on the sampling oscilloscope strongly depends on having identical input pulses and, considering the fact that it is unlikely for two delay lines to be identical, only one of the two delay lines was used. The repetition rate of this pulse generator, for a single delay line, is fixed at about 350 Hz due to limitations posed by

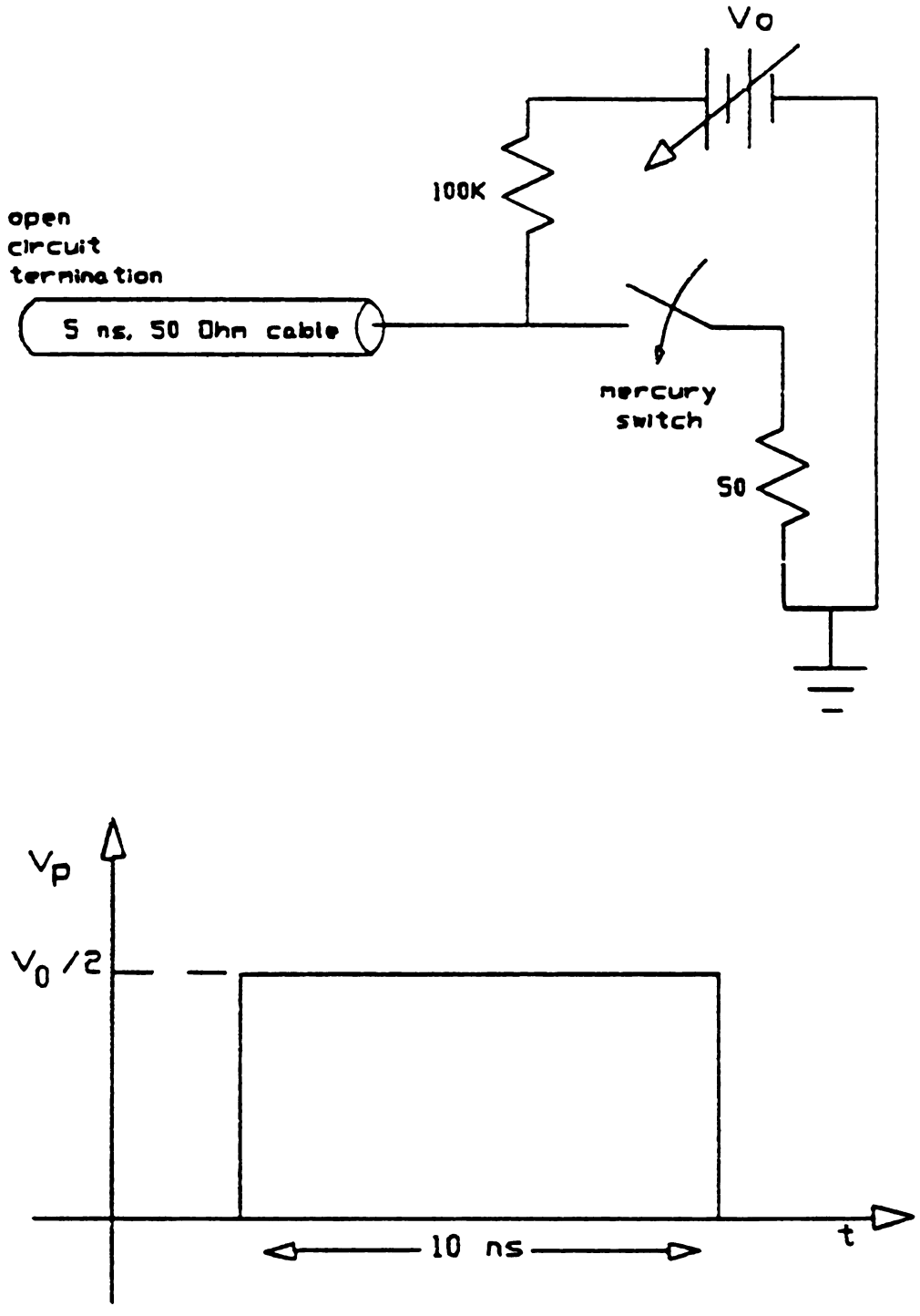


Figure A-2 A simplified schematic of the pulse generator circuit and the resulting pulse.

the reed switch. A coaxial cable, with the length equivalent to 5 ns of wave propagation, was connected to the delay line input to obtain a 10 ns wide pulse. Also, an external dc power supply (Universal Electronics 520A) was used to charge the delay line since the internal supply of the pulse generator was incapable of providing sufficiently high voltages.

All of the connectors and attenuators, as well as the bias insertion unit were coaxial General Radio components. Also, coaxial, low loss, low dispersion, RG9 cables were used to connect the circuit components. The length of each cable, in terms of its equivalent wave propagation time, is shown in Figure 3-4. The values of cable length, as discussed in Chapter 3, was properly chosen to obtain the desired timing relation between the oscilloscope trigger input, the diode response, and the reflections due to impedance mismatches in the circuit.

A Tektronix 661 sampling oscilloscope with 4S1 sampling heads was used to observe the diode response. The oscilloscope had a 50Ω input impedance and a 350 ps risetime which, combined with the risetime of the pulse generator, resulted in a total risetime of 450 ps for the observed pulse. Additionally, the oscilloscope was used in the external trigger mode and was set for 100 samples per horizontal division of display. The analog outputs of the oscilloscope's horizontal and vertical amplifiers were used as inputs to the analog-to-digital (A/D) converter.

A.2.2 Data Acquisition

The horizontal and vertical amplifier outputs of the sampling oscilloscope provided 200 mV for every centimeter of displacement on the CRT display. The dc offset adjustment and the horizontal position adjustment on the oscilloscope were used to match the zero level of the amplifier outputs to the desired reference location on the oscilloscope display. These output signals were also observed on a second oscilloscope (Hewlett-Packard 1727-A) to ensure proper dc offset adjustment and calibration. The output signals were, in turn, taken to an IBM personal computer equipped with a Data Translation DT2801 A/D converter board for digitization, and subsequently, integration of the vertical signal (corresponding to the diode current) with respect to the horizontal signal (corresponding to time).

The time involved in a single sweep of the oscilloscope trace is determined by the repetition rate of the pulse generator and the desired sample density as set on the sampling oscilloscope. In this experiment, each sweep of the trace took about 3 seconds and the A/D converter was set to take 150 samples. Therefore, a sampling frequency of about 50 Hz was used. The A/D board, however, was capable of sampling at much higher frequencies (up to 13.7 KHz).

In order to trigger the sampling at the beginning of the sweep of the oscilloscope trace, The A/D board was used in the external triggering mode. The signal by which the A/D conversion was triggered, was taken from the retrace portion of the horizontal raster signal. Figure A-3 shows the circuit which was used to generate the trigger signal. The 0.01 μF input coupling capacitance was used to filter out the slowly varying sweep portion of the raster signal while

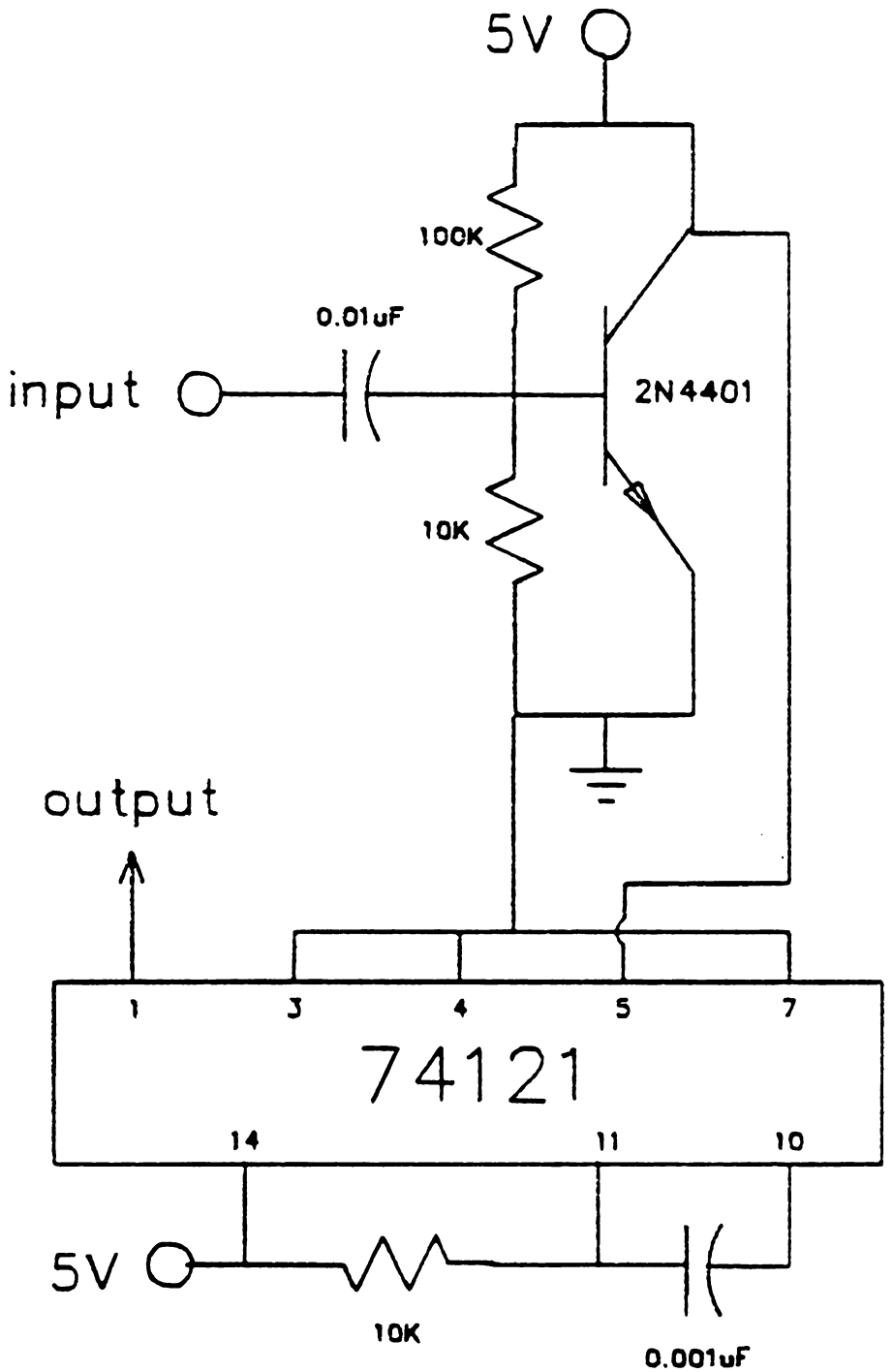


Figure A-3 Diagram of the circuit used to condition the retrace portion of the horizontal sweep raster of the sampling oscilloscope to generate a 7 μs down-going pulse suitable for triggering the A/D convertor.

transmitting the fast retrace portion of the signal. The retrace signal was subsequently amplified by the transistor circuit and was finally used to trigger a one shot, which generated a down-going 7 μs wide pulse suitable for the trigger input of the A/D converter board. The software used to control the A/D board was written in basic and made use of a real-time assembly language software package written by the manufacturer of the board, called PCLAB.

A.3 Sample Mounting

The initial intent was to use test chips which were mounted on ceramic subtrate using flip-chip technology. A shielded sample mount, large enough for the ceramic substrate, was fabricated so as to provide a gradual impedance change between the 50 Ω coaxial lines and the diode. Essentially, this sample mount was a coaxial cavity with an air dielectric, and tapered inner and outer conductors made from brass and copper, with the test diode being a part of the inner conductor. The sample mount was tested in the charge storage measurement circuit under open and short circuit conditions and showed little apparent parasitic capacitance or inductance. However, when a ceramic substrate with the test chip removed was inserted, the open circuit and short circuit conditions showed appreciable values for both parasitic capacitance and inductance, estimated to be on the order of 2 pF and 50 nH, respectively.

In order to reduce parasitics, it was decided to use bare chips (i.e. chips which were not mounted on a ceramic substrate). Thermal gold wire bonds were made to the chip solder balls at a temperature of approximately 160 °C using a West Bond wire bonder. A modified General

Radio type 874-X 50 Ω coaxial sample insertion unit was used, since the bare chips were small enough to fit into it. The modification of the sample mount involved the use of longer center conductors machined from brass rods to minimize the length of the discontinuity of the inner conductor to a value limited by the chip size. Checking this sample holder under open and short conditions showed no significant parasitic effects and the test chip mounted in this sample holder did not reduce the circuit's time resolution.

To perform the experiment at elevated temperatures, it was necessary to heat the test chip. To do so, the sample mount was heated up using a hot plate controlled by an Omega 4201 PC digital temperature controller which monitored the air temperature inside the sample mount using an RTD (resistance temperature detector) sensor. As a check, the sample temperature and the air temperature inside the sample holder were once measured using independent sensors to ensure that that the air temperature inside the sample holder does accurately reflect the sample temperature. The dielectric pellets holding the inner conductors in the GR connectors of the sample mount showed some deformity when exposed to high temperature and therefore, were replaced subsequent to every high temperature measurement.

A.4 Current-Voltage Measurement

Circuits used in the low and high bias current-voltage measurement have previously been shown in Figure 3-14. A Tektronix 577 curve tracer and a Fluke 8060-A digital multimeter were used in the low bias circuit. The multimeter was used in the high input impedance mode, with a value of at least 10,000 MΩ.

A Hewlett-Packard 214-A pulse generator and two Hewlett-Packard 1727A storage oscilloscopes were used in the high bias circuit. All test chips used in current-voltage measurements were mounted on ceramic substrates by the manufacturer (IBM) using fip-chip technology. To perform the experiment at elevated temperatures, the test device was heated in a Blue M oven equipped with a temperature controller.

A.5 Test Device Integrity

Under stressful conditions including high forward bias, the SBD may suffer degradation or damage [62,63]. occurrence of such damages during a measurement process, therefore, may result in erroneous data. To avoid this problem, all of the test devices used in various measurements were initially tested for damage. Subsequent tests of the device quality were done during various stages of each set of measurements and at the end of all measurements made on each test device. The data obtained from any device, which did not show good properties during the subsequent quality test, was discarded. The principal method to reduce the occurrence of device damage was found to be the use of low duty cycle pulses or bursts of signal to reduce the average power delivered to the device while achieving the desired high current levels. In spite of these precautions, however, several devices were found by the quality check to be damaged before the desired amount of data was collected

The criteria used to check the quality of the test device was the reverse current of the diode under a few volts of reverse bias. A 'good' unguarded device showed a reverse current on the order of one nA while stress related damage increased the reverse current, sometimes as

high as hundreds of μA. Efforts to restore the damaged devices by heat treatment, as suggested in the literature [62], were unsuccessful. The guarded devices showed much more robust characteristics as expected. The reverse current of these devices were found to be less than 0.1 nA which was the limit of the measurement equipment and stress related damage was rarely observed.

APPENDIX B

DERIVATION OF THE HIGH INJECTION HOLE TUNNELING BOUNDARY CONDITION

Equation 4-31 can be written as;

$$J_t = A^* qT/k \int_0^{\Phi_{bh}} [F_m(\phi) - F_s(\phi)]\, T(\phi)\, d\phi \qquad \text{(B-1)}$$

$F_m(\phi)$ is given by;

$$F_m(\phi) = \left\{1 + \exp[\, \beta(\phi - \phi_{fm})\,]\right\} \qquad \text{(B-2)}$$

Similarly,

$$F_s(\phi) = \left\{1 + \exp[\, \beta(\phi - \phi_{fs})\,]\right\} \qquad \text{(B-3)}$$

where β=q/kT, ϕ_{fm} is the metal Fermi potential and ϕ_{fs} is the quasi Fermi potential for holes in the semiconductor. As shown in Fig. 4-3, the potential reference is chosen to be the metal Fermi level.

Therefore, $\phi_{fm} = 0$. Considering the fact that the tunneling transmission coefficient is significant near the top of the barrier where $\phi >> 1/\beta$, $F_m(\phi)$ and $F_s(\phi)$ can be approximated by;

$$F_m(\phi) = \exp(-\beta\phi) \tag{B-4}$$

$$F_s(\phi) = \exp[-\beta(\phi - \phi_{fs})] \tag{B-5}$$

Using Equation 4-30 for the tunneling transmission coefficient and considering that

$$A^* qT/k = A^* T^2\beta \tag{B-6}$$

Equation B-1 can be written as;

$$J_t = A^* T^2\beta \int_0^{\Phi_{bh}} \left\{ \exp(-\beta\phi) - \exp[-\beta(\phi - \phi_{fs})] \right\} X$$
$$\exp\left[(-\alpha m^{*1/2}/E) (\Phi_{bh} - \phi)^{3/2}) \right] d\phi \tag{B-7}$$

which simplifies to

$$J_t = A^* T^2\beta \int_0^{\Phi_{bh}} [1 - \exp(\beta\phi_{fs})] X$$
$$\exp\left[(-\alpha m^{*1/2}/E) (\Phi_{bh} - \phi)^{3/2} - \beta\phi \right] d\phi \tag{B-8}$$

To evaluate the term $\exp(\beta\phi_{fs})$, note that

$$p = N_v \exp[(q\phi_{fs} - E_v)/kT] \tag{B-9}$$

where p is the hole concentration, N_v is the valence-band density of states, and E_v is the energy level of the valence band. Since the shape of the barrier is assumed triangular, and since the reference potential is the metal Fermi level

$$E_v = -q(\phi - \phi_{fm}) \tag{B-10}$$

Therefore, Equation B-9 can be written as

$$p = N_v \exp[\ \beta(\phi_{fs} + \phi - \phi_{fm})] \tag{B-11}$$

Rearranging the terms and adding and subtracting Φ_{bh} to the exponent gives

$$p = N_v \exp[\beta(\phi_{fm} - \Phi_{bh})] \exp[-\beta(\phi - \Phi_{bh})] \exp(\beta\phi_{fs}) \tag{B-12}$$

but

$$p_o = N_v \exp[\beta(\phi_{fm} - \Phi_{bh})] \tag{B-13}$$

where p_o is the hole concentration in the absence of excess carriers. Therefore, from Equation B-12

$$\exp(\beta\phi_{fs}) = [p/p_o] \exp[\beta(\phi - \Phi_{bh})] \tag{B-14}$$

Changing the integration variable in Equation B-8 to $S = \Phi_{bh} - \phi$, and using Equation B-14

$$J_t = A^* T^2 \beta \left\{ - \int_{\Phi_{bh}}^{0} \left[1 - p/p_o \exp(-\beta S)\right] X \right.$$

$$\left. \exp\left[(-\alpha m^{*1/2}/E)\ S^{3/2} - \beta(\Phi_{bh} - S)\right] dS \right\} \qquad \text{(B-15)}$$

Simplifying this equation further,

$$J_t = A^* T^2 \beta \exp(-\beta\Phi_{bh}) \left\{ \int_{0}^{\Phi_{bh}} \left[1 - p/p_o \exp(-\beta S)\right] X \right.$$

$$\left. \exp\left[(-\alpha m^{*1/2}/E)\ S^{3/2} + \beta S \right] dS \right\} \qquad \text{(B-16)}$$

The relation for tunneling current shown by Equation B-16 applies to both light and heavy holes in silicon. Therefore, the net hole tunneling current is the sum of the currents in the two valence bands. Noting that $A^* = A\ m^*$ where A is the Richardson's constant for a free electron (A = 120 A/K), the net tunneling current is given by;

$$J_t = A\ T^2 \beta \exp(-\beta\Phi_{bh}) \int_{0}^{\Phi_{bh}} \left[1 - p/p_o \exp(-\beta S)\right] X$$

$$\left\{ m_l^* \exp[(-\alpha m_l^{*1/2}/E)\ S^{3/2} + \beta S\ ] + \right. \qquad \text{(B-17)}$$

$$\left. m_h^* \exp[(-\alpha m_h^{*1/2}/E)\ S^{3/2} + \beta S\ ] \right\} dS$$

where m_l^* and m_h^* are the light and heavy hole relative effective masses. Equation B-16 can be reduced to Equation 4-33.

APPENDIX C

DERIVATIONS CORRESPONDING TO BARRIER HEIGHT MEASUREMENT METHODS

C.1 Modified Richardson's Constant Method

The Taylor series expansion for $f(V_j)$ from Equation 5-10 about zero gives

$$f(V_j) = f(0) + \dot{f}(0).V_j + 1/2\ \ddot{f}(0).V_j^2 + \ldots \qquad (C\text{-}1)$$

The zero order term f(0) equals zero as is evident from Equation 5-9. Therefore, to the extent that second and higher order terms may be neglected, $f(V_j)$ is directly proportional to V_j. However, using Equation 5-15 to examine the higher order terms of the expansion, it can be shown that the coefficients $\ddot{f}(0)$, ... are not negligible. Therefore, truncating the series after the first term is justified only at low values of V_j.

For the voltage range of interest (0.2 to 0.6 V), V_j is not small. Therefore, a better linear first order approximation to correct barrier height lowering is obtain by expanding $f(V_j)$ about a voltage V_m defined as the mean value of the voltage range of interest.

$$f(V_j) = f(V_m) + \dot{f}(V_m).(V_j - V_m) + [\ddot{f}(V_m)/2]\ (V_j - V_m)^2 + \ldots \qquad (C\text{-}2)$$

For this expansion, the higher order terms are negligible if $V_j - V_m$ is small, which is a better approximation than the one associated with the expansion about zero voltage. Using the expansion given by Equation C-1, Equation 5-8 can be approximated by

$$I = A_e A^{**} T^2 \exp\{-\beta\ [\Phi_e(0) + f(V_m) - \dot{f}(V_m).V_m + \dot{f}(V_m).V_j]\ \} \exp(\beta V_j) \qquad (C\text{-}3)$$

In order to obtain an expression with a voltage independent I_s, this equation can be written as

$$I = A_e\ A^{**}\ T^2\ \exp\{-\beta\ [\Phi_e(V_m) + \Delta\dot{\Phi}(V_m).V_m]\}\ \exp(\beta V_j/\eta^*) \qquad (C\text{-}4)$$

where
$$\eta^* = [1 - \dot{f}(V_m)]^{-1} = [1 + \Delta\dot{\Phi}(V_m)]^{-1} \qquad (C\text{-}5)$$

C.2 Modified Norde's Method

To solve Equation 5-22 for dF/dV = 0, note that

$$dI/dV = dI/dV_j\ [1 + R\ dI/dV_j]^{-1} \qquad (C\text{-}6)$$

where $V_j = V - IR$

But, $dI/dV_j = \beta SI$ (C-7)

where $S = 1 + \Delta\dot{\Phi}(V_j)$

Therefore, $dI/dV = \beta SI/(1 + \beta SRI)$ (C-8)

Also, $d\Delta\Phi/dV = d\Delta\Phi/dV_j \; [1 + R \; dI/dV_j]^{-1} = d\Delta\Phi/dV_j \; [1 + \beta SRI]^{-1}$ (C-9)

Therefore, Equation 5-22 becomes

$$dF(V)/dV = (1/\alpha - 1) + [\beta SRI - d\Delta\Phi/dV_j] \; / \; (1 + \beta SRI) \quad \text{(C-10)}$$

or $$dF(V)/dV = 1/\alpha - S/(1 + \beta SRI) \quad \text{(C-11)}$$

Setting $dF(V)/dV = 0$ to obtain the location of the minimum (V_o, I_o) yields

$$RI_o = 1/\beta \; [\alpha - 1/S] \quad \text{(C-12)}$$

and $$V_o = 1/\beta \; \ln(I_o/I_s) = 1/\beta \; \ln[(\alpha - 1/S)/\beta RI_s] \quad \text{(C-13)}$$

where I_s is given by Equation 5-5. These expressions correspond to Equations 5-23.a and 5-23.b.

To solve for d^2F/dV^2, approximating S by 1 and differentiating Equation C-11

$$d^2F(V)/dV^2 = \beta R\ [1 + \beta RI]^{-2} dI/dV \qquad \text{(C-14)}$$

So, using Equation C-8

$$d^2F(V)/dV^2 = \beta[\beta RI/(1 + \beta RI)^3] \qquad \text{(C-15)}$$

Therefore, at V_o, using Equation C-12

$$[d^2F(V)/dV^2]_{Vo} = \beta\ (\alpha - 1)/\alpha^3 \qquad \text{(C-16)}$$

which is Equation 5-26.

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