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ABSTRACT

CURRENT SATURATION MECHANISM IN FIELD-EFFECT TRANSISTORS

By

Sukhbir Singh

It is proposed that current saturation in Field-Effect Transistors is due to the presence of space-charge layers which develop inside the channel normal to the direction of current flow. This space charge is induced by the gate field. It is shown that the spatial variation of the majority carriers in the channel gives rise to High-Low junctions inside the channel region and that these induced junctions are responsible for a large diffusion current to exist inside the channel.

An idealized model of a junction, field-effect transistor is considered. The two gates are assumed to be two abrupt p-n junctions placed symmetrically with respect to the center of the channel. It is also assumed that the drain and source contacts are ohmic and that the source contact overlaps the gates. Only the case in which a drain voltage is specified is considered.

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The device is analyzed in two space variables with the majority carriers as the sole current carriers. It is shown that the drain current flow is restricted to a very narrow region around the center of the channel and that the channel width never reduces to zero--even for moderately large fields. Two electric double layers are found to be present in the channel; these double layers are responsible for the observed current saturation phenomenon. Channel current control is found to be analogous to the control of collector current by the collector field in a bipolar transistor. The existence of a diffusion mechanism in the channel and the absence of velocity saturation are two important conclusions. Furthermore, it is concluded that the presence of an electric double layer is a fundamental property of field-effect devices.

CURRENT SATURATION MECHANISM IN FIELD-EFFECT TRANSISTORS

By

Sukhbir Singh

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TABLE OF CONTENTS

LIST OF SYMBOLS

a	width of half channel
b	length of channel
k	permittivity of semiconductor
n	mobile electron density
n_i	intrinsic carrier density
p	mobile hole density
x, y	spatial variables
u_n	electron mobility
u_p	hole mobility
D_n	diffusion constant for electrons
D_p	diffusion constant for holes
F	electric field
I	drain or channel current
J_n	electric current density due to electrons
J_p	electric current density due to holes
K	Boltzman's constant
L_d	Debye shielding distance or Debye length
N	concentration of impurities

q	electronic charge
Q	charge density
U	dimensionless electrostatic potential
V_d	applied drain voltage
w	channel width
ϕ_n	quasi-Fermi level for electrons
ϕ_p	quasi-Fermi level for holes
ψ	electrostatic potential

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (cont.)

CHAPTER 1

INTRODUCTION

1.1 Background

The Field-Effect Transistor (FET) is a unipolar device. The electric current which flows through the device is due to the majority carriers. Current control is obtained by changing the dimensions of the channel and/or by changing the carrier concentration in the channel.

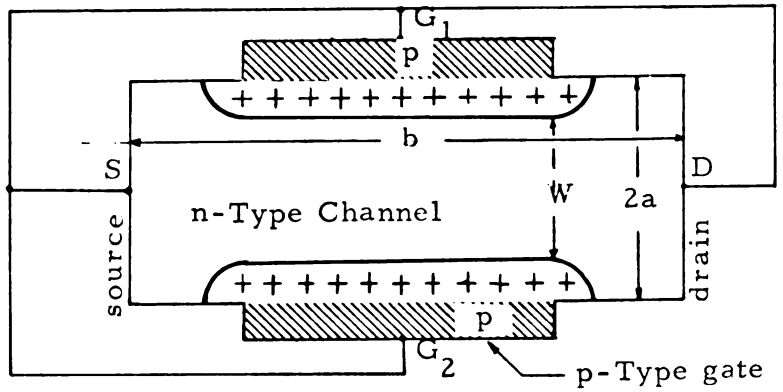
There are basically two types of field-effect transistors: the Junction Field-Effect Transistors (JFET) and the Insulated Gate Field-Effect Transistors (IGFET). The latter is sometimes called the 'metal-oxide-semiconductor' (MOS) transistor. Their principle of operation (current controlled by an electric field) is very similar to the JFET; the primary difference being the manner in which the control element is made. In the junction FET, reverse biased p-n junctions are used to change the dimensions of the conducting channel. In the surface FET, both the carrier concentration and dimensions of the channel are controlled by an

electric field at the surface. In this thesis, only the case of JFET's is considered.

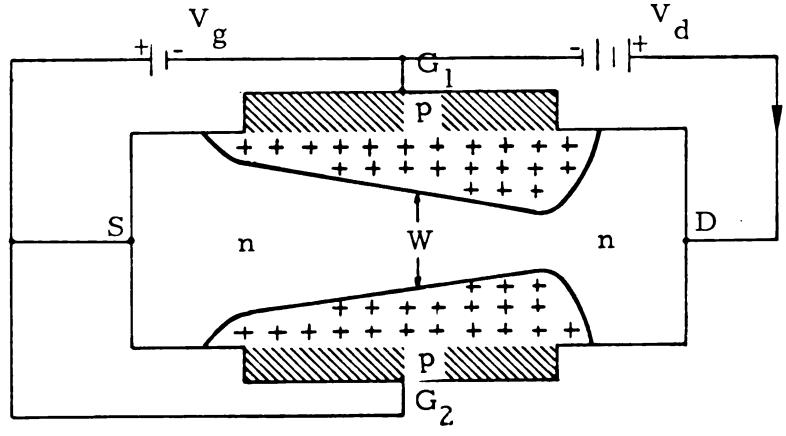
Field-effect devices are attractive both as active and passive components because of the readiness with which they can be integrated into large-scale monolithic circuitry. They are also easier to manufacture by evaporation techniques and can be made from less refined materials than can the bipolar transistors. The most notable advantages of field-effect transistors are their high input impedance and their 'self-biasing' feature. Absence of any charge storage mechanisms makes them especially useful for switching purposes.

1.2 Basic FET Amplifier

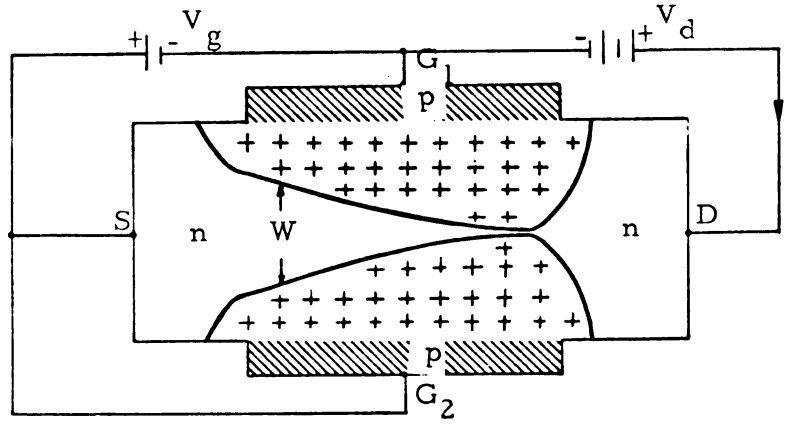
A field-effect transistor is essentially a voltage controlled resistor. The 'resistor' consists of a region of n-type material sandwiched between two regions of p-type material. In Figure 1.1(a) the electrical contacts S and D at the two ends of the 'resistor' are called the Source and Drain respectively. The p-type regions, called the Gate G_1 and Gate G_2, are generally connected together. When the gates have a reverse or no bias with respect to the source terminal, the space charge of p-n junctions lies partially in the n-type region. The dimensions of the conducting region, therefore, depend upon the bias on the gates. The length b of the conducting region between the two gates is called the



(a) $V_d = 0$; $V_g = 0$



(b) $V_d > 0$; $V_g \leq 0$



(c) $V_d \geq V_p$; $V_g \leq 0$

Figure 1.1. Schematic diagram of an n-channel junction FET under various bias conditions. The approximate shape of space charge regions in the channel is shown. (a) Zero bias on all electrodes; (b) Negative gate-source voltage and positive drain source voltage; (c) Saturation condition for negative gate voltage.

channel. The width, w, is smallest between the gates and therefore determines the resistance of the channel. In an undepleted channel, w = 2a, and the resistance is the lowest.

When a voltage is applied between the source and the drain, current flows in the channel. Also the reverse bias on the gate-channel junctions gradually increases from S to D and space charge expands into the channel as depicted in Figure 1.1(b). The channel has the largest width near the source end, where the voltage drop is low, and has the smallest width near the drain end, where the voltage drop is the largest. The p-n junction can thus be used to control the dimensions and hence the resistance of the channel. As the reverse bias on the gates increases, a condition is reached where the space charge extends completely across the channel and the width of the channel reduces to zero [see Figure 1.1(c)]. The reverse bias needed to achieve this condition is called the Pinch-Off voltage V_p. The pinch-off can also be achieved, with zero gate voltage, by increasing the drain voltage till the channel width becomes zero.

In typical devices the pinch-off voltage varies from one to ten volts and the resistance of the channel may vary from as little as 100 ohms with zero bias to as high as many Megohms near the pinch-off condition.

The above explanation was in terms of an FET with an n-type channel; FET's are also fabricated with p-type channel

and n-type gates. These two FET's are complementary.

To optimize the working of the device, it is so designed that the space charge of p-n junctions expands primarily into the channel. This is done by choosing the channel to have a higher resistance than the gates. Under these conditions the space charge lies entirely in the channel.

Figure 1.2 shows schematically an FET as an amplification device. Amplification action occurs because of the fact that the width of the space charge depends upon v_{gs}--the signal voltage. A changing channel current causes a changing voltage drop across R_d--the load resistance. Amplification is obtained because the change in v_{ds}--the output voltage, can be many times larger than the change in v_{gs}.

In normal operation of an FET the gates are always reverse biased. The reverse current of the gates, and hence the power drawn from the source is negligible. The input impedance is, therefore, very large.

1.3 FET Characteristics

The important characteristics of the FET are shown in Figure 1.3. Figure 1.3(a) is the drain or output characteristics. At low drain-source voltage, for fixed bias, the current increases in proportion to voltage. The portions of the curve where the slope is not zero correspond to the condition in which the channel

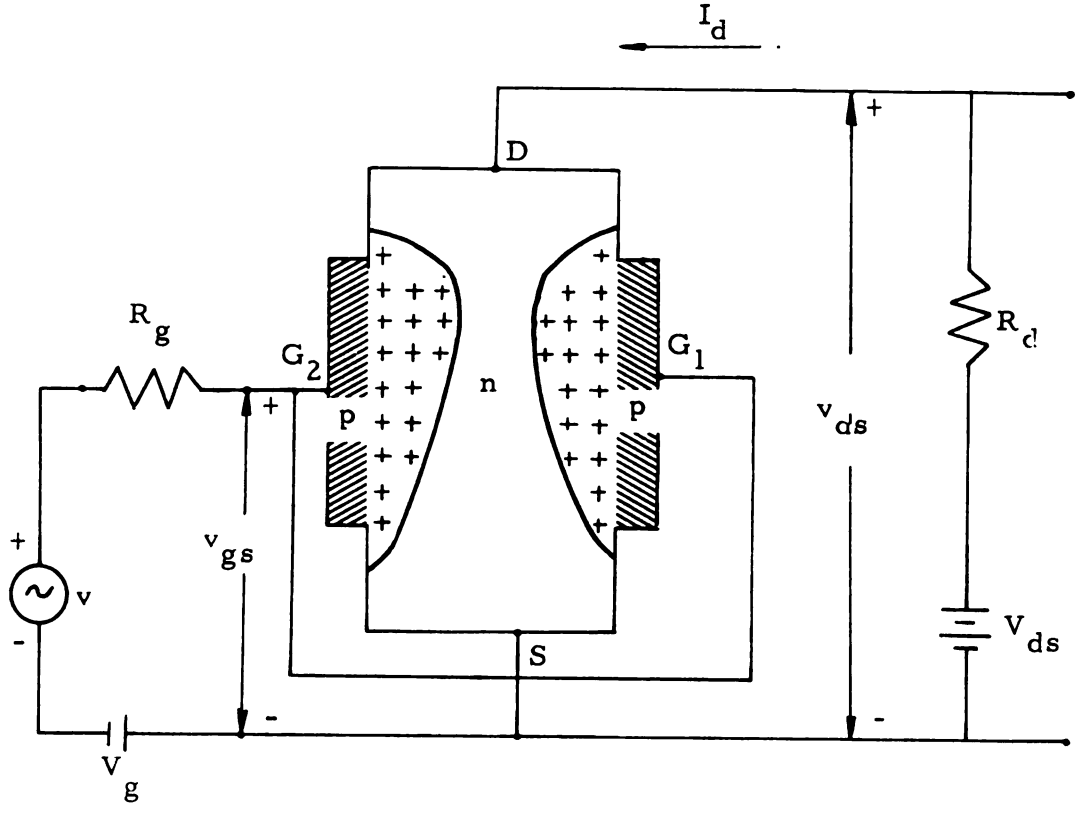


Figure 1.2. An FET Amplifier; A pictorial representation.

between the drain and source acts like a controlled resistor. This region is sometimes referred to as the triode region. In this region of operation, volt-ampere characteristics can be derived from the Gradual Channel Approximation Model [1]. At higher drain voltages the current begins to bend over indicating an increased resistance of the channel. When V_d becomes greater than V_p, the curve levels off and the current becomes essentially independent of the drain voltage. The portion of the curve where the slope is zero (V_d greater than V_p) corresponds to the condition of pinch-off, and the current is said to be saturated. The transistor in this region is a voltage-controlled, constant-current device. It is in this region that it is normally operated as an amplifier. A sharp increase in current at higher voltages indicates the onset of avalanche breakdown. Figure 1.3(b) illustrates a typical family of output characteristics and shows the kind of control exercised by the gate voltage on the drain current.

Figure 1.3(c) is the gate-drain transfer characteristic for the condition when the channel is pinched-off. The unique shape of these characteristics makes FET's very suitable as 'remote control' devices.

1.4 Objectives of the Present Work

In the above simplified model of the FET, the behavior of the device, in terms of its drain current, is the same as that

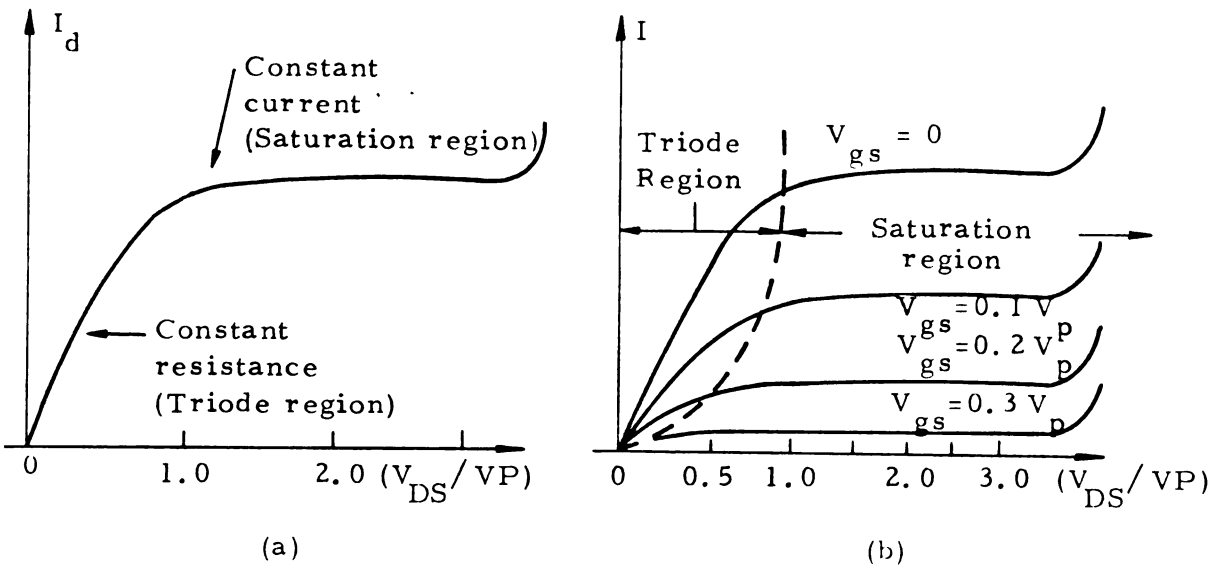


Figure 1.3. The output family of characteristics. (a) Variation of drain current with drain voltage. (b) Drain current versus drain voltage with different values of gate bias.

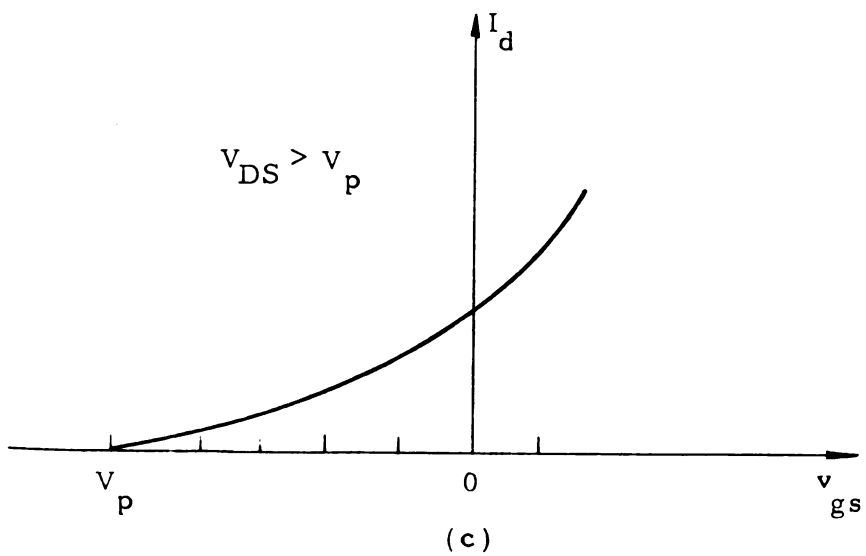


Figure 1.3. (c) Drain voltage-gate bias transfer characteristics for $V_{ds} = V_p$.

predicted by the Gradual Channel Approximation theory [1]. According to this theory the channel width decreases in proportion to the square root of the drain voltage. Thus for drain voltages equal to or greater than the pinch-off voltage, the channel is pinched off and has a zero width--at least over some portion of its length. In other words, the channel is incapable of sustaining a flow of current. Similarly, at a fixed drain voltage, the space charge regions of the gate junctions expand with increasing gate bias and eventually extend completely across the channel. A large negative bias is thus able to make the drain current zero. This predicted value of drain current is contrary to the observed effects in the actual devices, i.e., even for a pinched off channel a large current continues to flow and is independent of the drain voltage.

The present work endeavors to explain:

1. The phenomenon responsible for the saturation of drain current.

2. The mechanism which tends to maintain the drain current at a near constant value with drain voltage.

3. The non-zero slope of the drain-current versus drain-voltage characteristics.

CHAPTER 2

EXISTING THEORIES OF CURRENT SATURATION

The analysis of the unipolar transistor was first accomplished by Shockley in 1952 [1]. The keypoint in his analysis was the so-called 'Gradual Channel Approximation,' whereby it was assumed that the rate of change of channel width was much smaller than the actual width of the channel. Space charge regions of the gates were assumed to be completely depleted of the majority carriers. Shockley further assumed that the transition from the depleted to the neutral channel was abrupt, and, accordingly, that electrical neutrality existed inside the channel. For drain voltages larger than the pinch-off voltage, the channel was assumed to be pinched off; any increase in drain voltage would be absorbed by the expanding gate-channel boundary. Under these conditions Shockley's model predicted the current to be confined to an infinitely thin plane near the center of the channel and that the current was maintained at the saturation level as a result of the channel length modulation by the drain voltage.

Numerous subsequent elaborations of Shockley's model have been in the direction of interpreting the saturation

phenomenon while staying within the Gradual Channel Approximation. The most significant extensions of Shockley's original theory are: (1) carrier mobility dependence on electrical field [3-7], (2) different geometries and impurity distributions, and (3) the effect of temperature and charge injection [8-11].

Kennedy [11] used the special geometry of the SCAD (Small Current Amplification Device) to establish the presence of High-Low junctions [12] in the channel. This prevents the channel from choking itself due to its own current. Kennedy has further shown [13], by an extensive numerical analysis of the device, that a high-low junction is also present in a uniformly doped channel provided the mobility of the carriers is taken to be dependent upon the electric field. By an approximate analytical solution of Poisson's equation, Goldman [14] predicted the presence of an inversion layer inside the channel. This inversion layer should give rise to increased minority carriers which are responsible for maintaining a large current even in the pinched off channel.

2.1 Shockley's Model

In an idealized p-n-p structure, two abrupt and reverse biased p-n junctions are used to modulate the width of a uniformly doped n-type channel. If p-type regions are doped much more heavily than the n-type channel, the space charge regions can be assumed to lie entirely inside the n-type channel. The space charge

within the channel can be adequately described by Poisson's equation:

$$\frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2} = - Q(x, y)/k, \tag{1}$$

where $Q(x, y)$ is the charge density (coulombs - cm^{-3}) in the channel and k is the permittivity of the material.

When the drain and source are at the same potential, Equation (1) reduces to one dimension,

$$\frac{d^2 V}{dy^2} = - \frac{dE}{dy} = - Q(y)/k , \tag{2}$$

where $E = - \frac{dV}{dy}$ is the potential gradient. As shown in Figure 2.1(a), the boundary conditions are

$$Q(y) = \begin{cases} 0 & y < d \\ qN_d & y \geq d \leq a \end{cases} \tag{3}$$

$E_y = 0$ at $y = d$,

and

$V = 0$ at $y = a$;

q and N_d are defined as the electronic charge and the donor impurity density in atoms - cm^{-3} respectively. Equation (2) is readily solved and yields

$$d(V) = a \left[1 - \left(\frac{V(y)}{V_p} \right)^{\frac{1}{2}} \right], \tag{4}$$

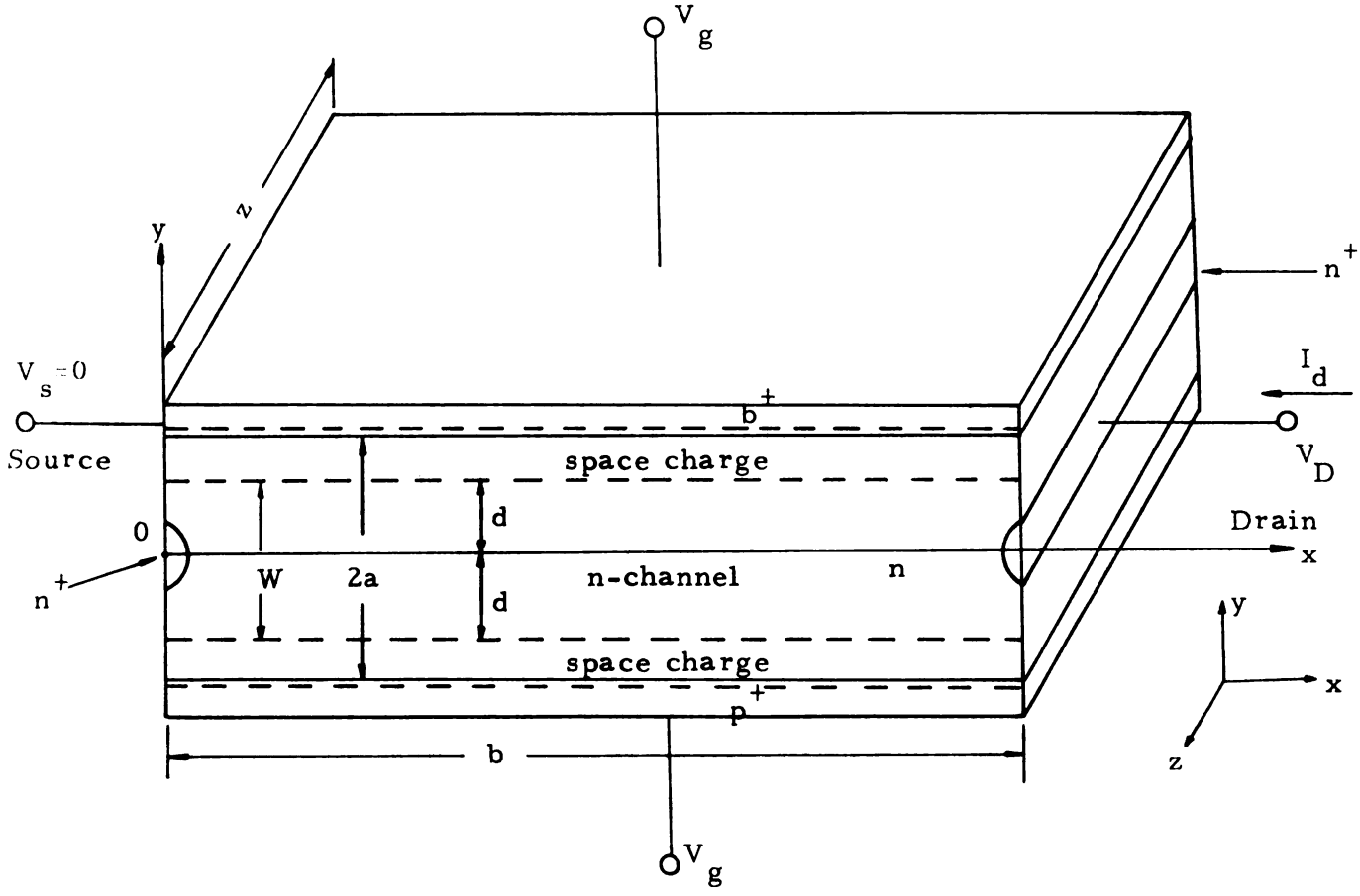


Figure 2.1. JFET model; space charge regions are shown for the case of zero drain voltage.

where $V_p = \frac{qN_d a^2}{2k}$ is the voltage necessary to extend the space charge completely across the channel. V_p is called the pinch-off voltage.

When the drain is raised to a positive potential, the current flows and causes a potential change along the x-direction. Since the gate electrodes are equipotential, the reverse voltage between the gate and the channel varies with x; hence the channel width varies. The channel slope, variation of w with x, can be obtained by solving Equation (1). This equation is nonlinear and cannot be solved conveniently in terms of known mathematical functions. However, if $\frac{\partial^2 V}{\partial x^2}$ is very small compared to Q(x, y), then a one-dimensional approximation can be used for V(x, y), with the channel width still being described by Equation (4). The condition for

$$\frac{\partial^2 V}{\partial x^2} << \frac{\partial^2 V}{\partial y^2}$$

is termed as the Gradual Channel Approximation [1]. This approximation means that the voltage at any point in the channel is determined by the voltage on the gates only and is independent of the drain voltage and drain current.

The ohmic flow of current in the channel is given by

$$dV = \frac{I\, dx}{\sigma\, z\, 2[a - d(V)]} \quad * \qquad (5)$$

---

* σ is the conductivity of the channel material.

Equations (4) and (5) are then combined to integrate V(x) with respect to x. The constant of integration is so chosen that d = a when x = 0. The resulting shape of channel is

$$x = \left(\frac{aI_o}{I}\right)\left\{\frac{1}{6} - \left[\left(\frac{s^2}{2}\right) - \left(\frac{s^3}{3}\right)\right]\right\}, \qquad (6)$$

where s = d/a and

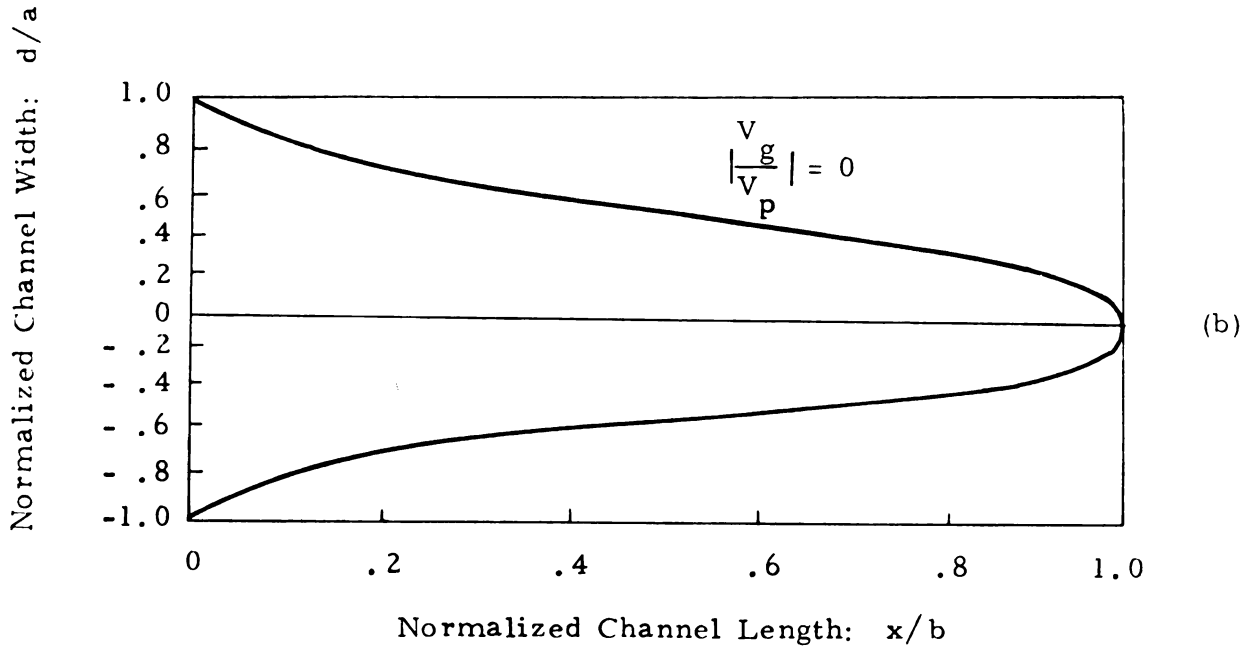
$$I_o = 8 u_o k V_p z/a^2 \quad **.$$

Figure 2.1(b) shows the shape of the channel at pinch off. Variation of drain current with drain voltage, below the pinch-off condition, is shown in Figure 2.1(c).

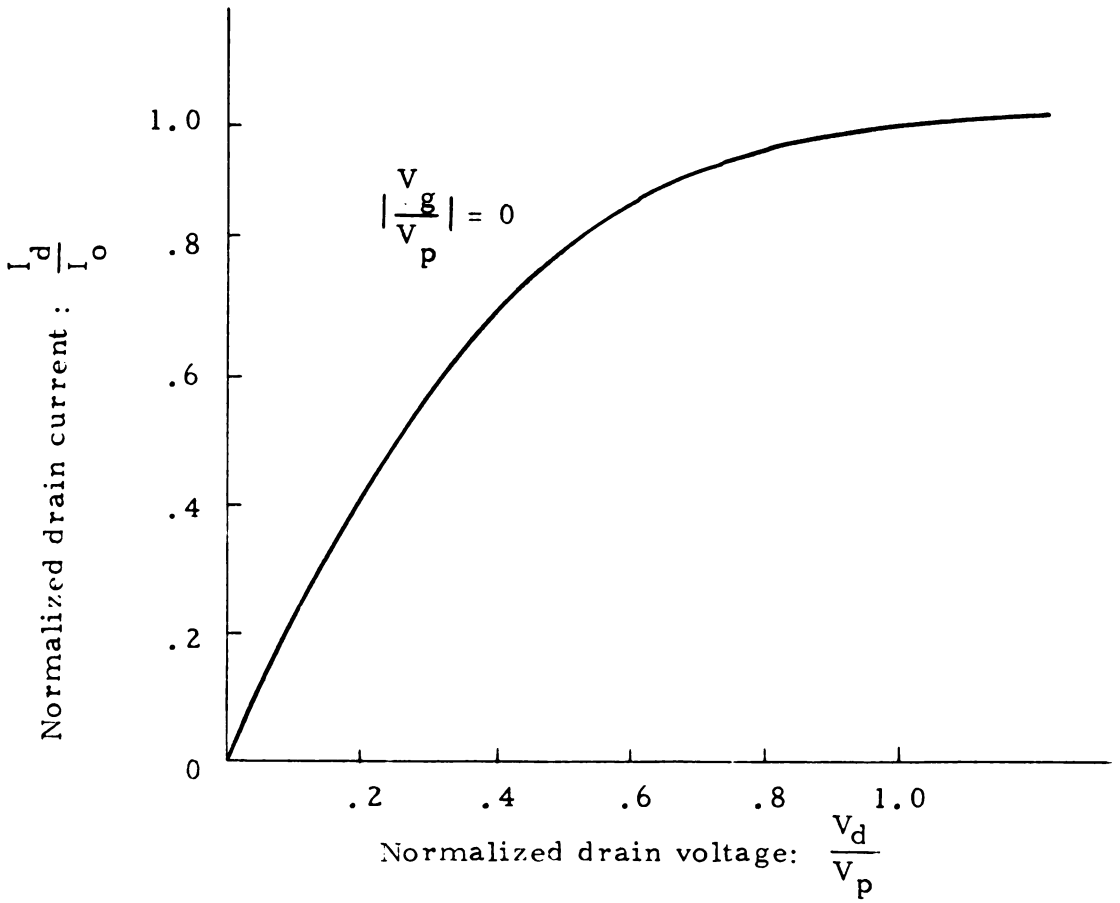
As the drain voltage is increased from zero volts, the current increases linearly at first, and then finally tends to level off as V_d becomes comparable to V_p. For V_d greater than V_p, the model is no longer adequate to describe the large and almost constant flow of current in the channel.

The gradual channel model is quite adequate for drain voltages less than the pinch-off voltage; however, it fails to explain the behavior of the FET beyond pinch off. In this region (V_d greater than V_p) some of the approximations are no longer valid. The most notable assumptions are:

** z is the thickness of the channel and u_o is the mobility of the carriers.



(b)



(c)

Figure 2.1. The gradual channel approximation; (b) shape of channel, (c) drain current.

1. The longitudinal electric field due to the drain electrode and carrier flow in the channel is ignored. For short devices ($b/a << 10$) this cannot be justified; near the drain contact the longitudinal field is large and comparable to the laterial field.

2. Equation (6) predicts that at pinch-off an infinite current density may exist. Under this condition the gradual channel approximation is badly violated. It can be shown that the gradual channel approximation is not valid for distances less than $a/2$ from the drain end [2].

3. The assumption that abrupt termination of space charge on the neutral channel exists, eliminates any mechanism by which a space charge can terminate on a neutral semiconductor.

4. Due to the back biasing of the gates, Shockley's theory implies that the space charge regions should completely penetrate across the channel and reduce the drain current to zero. This, however, does not occur in practice. Thus field-effect theory, based on complete depletion, is not correct.

5. Near the drain end, where extremely large fields are predicted, no account is taken of the nonlinearity of the mobility of the charge carriers.

6. Because of the large amount of the charge present in the channel, the mathematical analysis should be by the use of Poisson's equation rather than the Laplace equation.

2.2 Shockley-Prim Modification

Shockley and Prim [1-2] extended the above theory further by including the effect of expansion of the depletion region towards the source contact. When the drain voltage is larger than the pinch-off voltage, the depletion expands as shown in Figure 2.2. The point

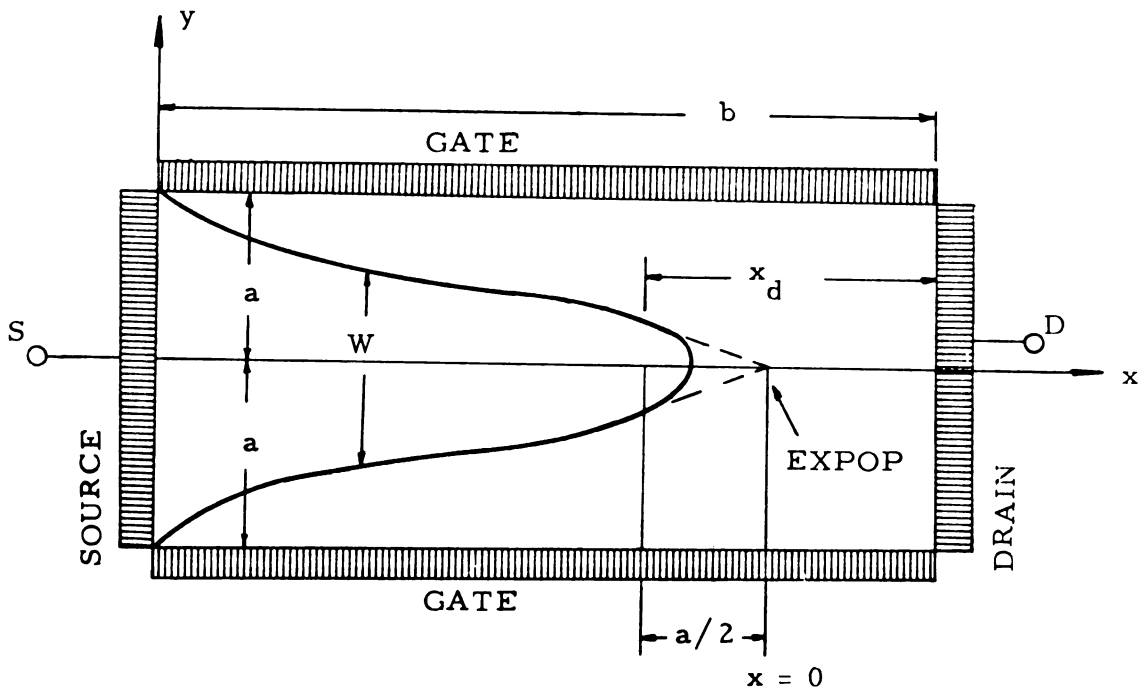


Figure 2.2. Channel length modulation by gate space charge.

$x = 0$, the extrapolated pinch-off point (expop), is defined as the point where s would reduce to zero if the channel were extrapolated beyond the range of its validity.

On the right of the expop the electrons, instead of flowing over a finite width of the channel, can be assumed to be constrained to the $y = 0$ plane. This shift does not effect the total potential much because the field of the electrons is much smaller than the field due to the gate space charge and the drain electrode voltage. The only field responsible for moving the carriers is E_x--the field due to the drain electrode. Towards the right of the expop and at the $y = 0$ plane, the charge due to the electrons is so small that the channel can best be described by the Laplace equation

$$\frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2} \approx 0 . \tag{7}$$

solution of Equation (7) is matched at $x = -a/2$ to the field due to the electrons [2] to give the width of the depletion region x_d; one finds that

$$x_d = \frac{a}{\pi} \left\{ \left[\ell n (V_d - V_p)^2 \left(\frac{I_o}{I V_p^2} \right) \right] - (0.65 - 0.64 \ell nf) \right\} ,$$

where f is the scaling factor used to match the solution of Equation (7) and Equation (6). The value of f has been estimated [1-2] to be about 0.254.

There are several flaws in this theory: The electric fields encountered in this formulation are within the range of nonlinear carrier mobilities and yet the nonlinearities were not taken into account. Also, the model does not give a satisfactory explanation of the manner in which the current flows through the space charge region of the gate channel. The saturation conductance of the channel is zero and is far less than the measured value in the actual transistors.

2.3 Kennedy's Model

In his report on the 'mathematical investigation of semiconductor devices' [11] Kennedy explains very successfully the current saturation in a SCAD (Small Current Amplification Device). Figure 2.3 shows the geometry of the SCAD under investigation. The channel lies between specially shaped p-type gates symmetrically placed with respect to the center of the channel. The source contact is diffused with an impurity gradient of the type shown in Figure 2.4. The gates are so shaped that the channel has a narrow neck in the region where the impurity gradient changes rapidly. The two dimensional Poisson's equation was solved numerically to obtain the charge density in the channel. A High-Low junction [12] was shown to be present at the neck of the channel where the depletion layer theory would predict a channel pinch-off. The High-Low junction arises as a consequence of the spatial distribution of the

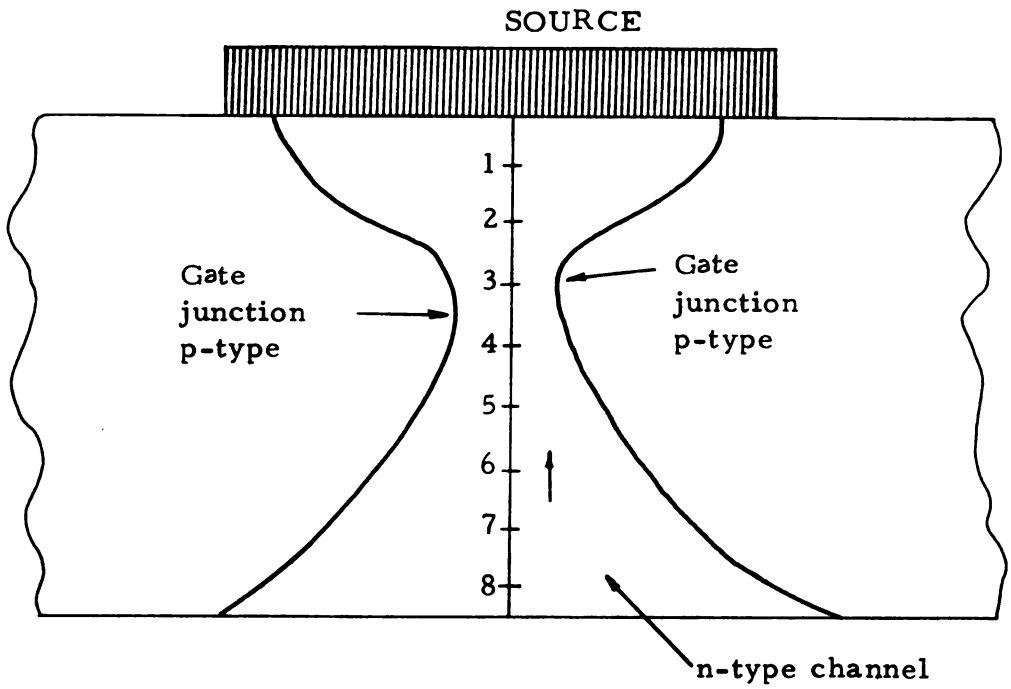


Figure 2.3. Small Current Amplification Device [11].

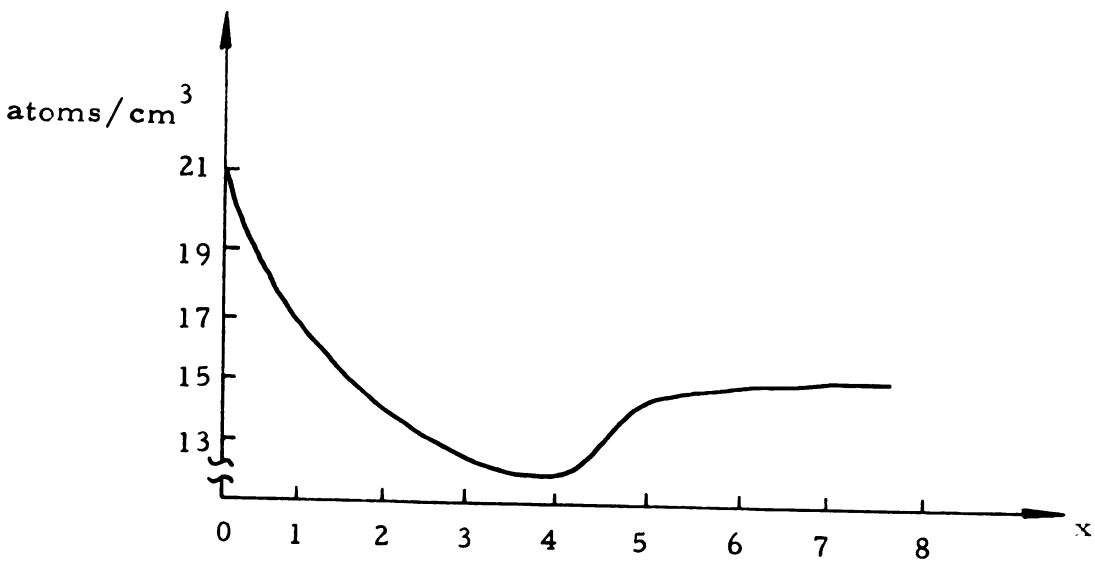


Figure 2.4. Impurity profile at the center of the SCAD.

majority carriers to form an accumulation layer adjacent to the depletion layer. The space charge of this accumulation-depletion layer is equivalent to an electric double layer.

With appropriate biasing voltages, the expansion of gate-channel depletion layers into the channel is blocked by the presence of the electric double layers and hence the channel width cannot be completely reduced to zero. With certain dimensions of the channel the accumulation layer seems to enhance the electric conduction. Various combinations of channel dimensions and bias voltages were tried to confirm that it is an electric double layer that is responsible for the current saturation.

Kennedy proposes the presence of such a double layer, as the cause of current saturation, in all field-effect devices. In uniformly doped channels, it is further proposed, that an electric double layer is present in the drain current path, because of the redistribution of the voltage, after the pinch off. For a near zero drain current, the charge in the channel, obtained by the integration of the longitudinal field, consists of an equal number of positive and negative charges. Due to the partial depletion of the channel, positive charges are balanced by an adjacent layer of accumulated negative charges. This, Kennedy surmises, gives rise to an electric double layer. However, a near zero value of drain current is necessary for the above hypothesis to hold. This is not always found to be the case.

2.4 Goldberg's Model

Goldberg [14] predicts the presence of an inversion layer in the channel as a result of an approximate solution of one-dimensional Poisson's equation. For a p-n-p structure, if the width of the n region is made extremely small--either through metallurgy or by reverse biasing the p-n junctions, then an inversion layer is shown to be present in the n region.

As shown in Figure 2.5, U_b is the bulk electrostatic potential, in equilibrium, in the n region. As the width of the n region is reduced U passes through a maximum in passing from one p region to the other. If the n region is made so narrow that U never reaches its bulk value then the majority carrier density reduces at this point. The corresponding minority carrier density increases, Goldberg proposes, thereby giving rise to an inversion layer.

However, it is well known that with such narrow junctions, the Fermi levels can be assumed to be constant and continuous across the p-n junction and hence, before an inversion can take place, the junction is completely depleted.

Actually an inversion layer, in the channel, is not needed to cause a saturation. Even a little depletion, at any point in the channel in the path of current, can give rise to a high-low junction and can thus modify the current flow.

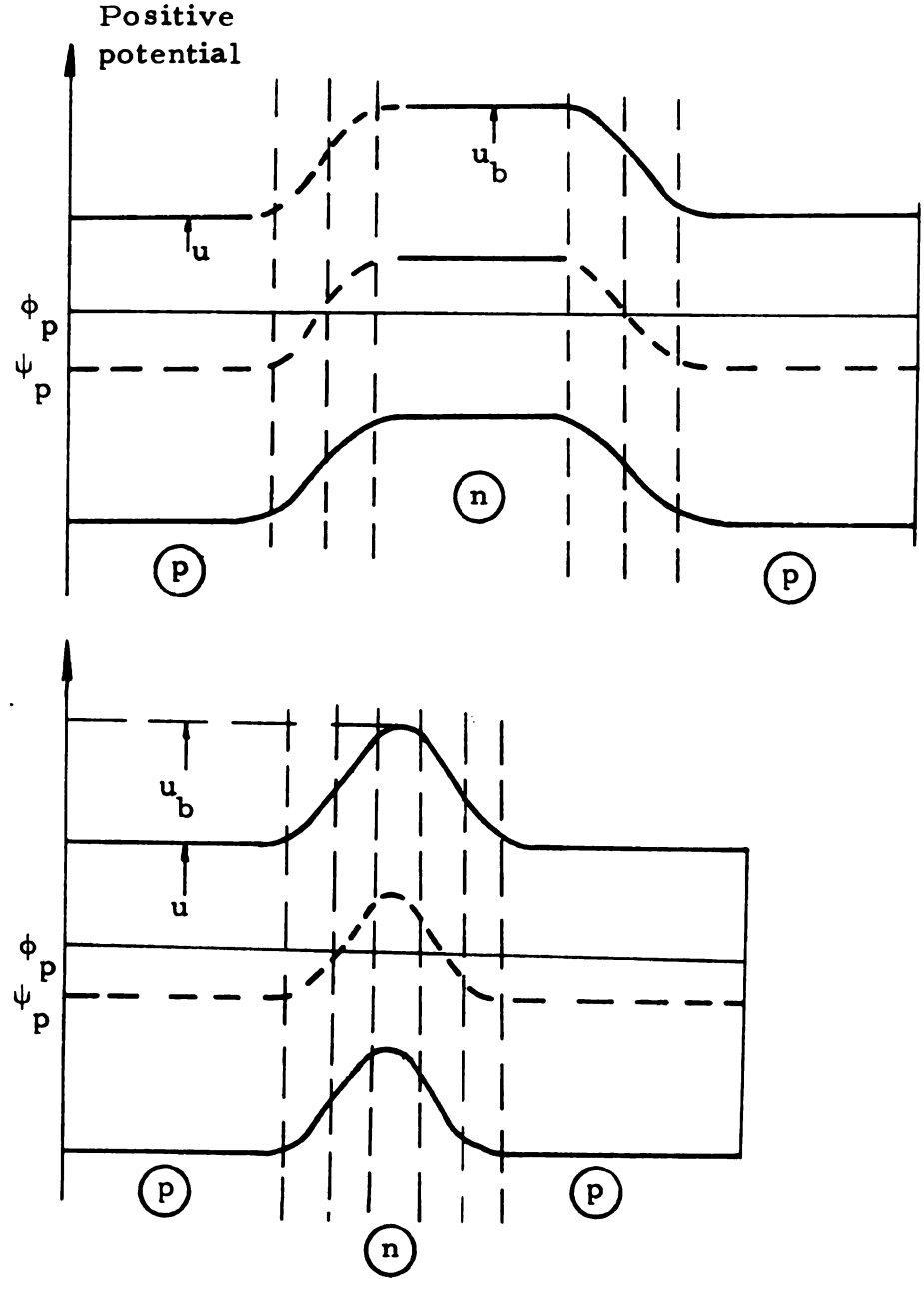


Figure 2.5. Electrostatic potential variation in a p-n-p structure; (a) wide n-region, (b) narrow n-region.

2.5 Gradual Channel Nonlinear Mobility

Various attempts have been made to explain the saturation phenomenon by incorporating into the above model the phenomenon of field dependence of the charge carrier mobility. For field values as large as those near the drain contact, on the basis of gradual channel model, the carrier mobilities are in the nonlinear range. From experimental data there are two critical fields E_{c1} and E_{c2} with E_{c1} less than E_{c2}. For fields below E_{c1}, the mobility is constant. For fields between E_{c1} and E_{c2} the mobility is proportional to the square root of the field. For fields above E_{c2}, the mobility is inversely proportional to the field. For Silicon the values of these fields are approximately:

	n-type	p-type
E_{c1}	2.5 KV/cm	7 KV/cm
E_{c2}	15.0 KV/cm	20 KV/cm

Reduced mobility at increased fields requires still larger fields to maintain the current at the same level and the velocity quickly saturates to its maximum value. With the velocity of carriers saturated at its maximum value, Grebne and Ghandhi [4] postulate a minimum residual thickness of the channel near the pinch-off point in order to estimate the longitudinal field. This field is then matched with the field obtained from Shockley-Prim formulation; the result is the saturated drain current.

Dacey and Ross [8-9] considered the effect of temperature on the mobilities to explain the output conductance of the field-effect transistor.

All the above modifications start with the gradual channel approximation as the basic model; therefore, the explanation of saturation mechanism is avoided. At pinch off almost all the drain voltage drop is across the depleted region; also, in spite of the large space charge present in the channel, the space charge current is ignored.

CHAPTER 3

THE PROPOSED CURRENT SATURATION MODEL

The works of Shockley [1], Sah [3] and Ghandhi [4] assume that the transition between the conductive channel and the depletion region takes place abruptly, and accordingly, electric neutrality exists in the channel. This assumption is correct for channel widths much larger than the transition region width which is of the order of 5 to 10 Extrinsic Debye Lengths in Silicon [11]. With a uniform impurity doping of the order of 10^{15} atoms/cm^3 the extrinsic Debye length in silicon is of the order of 4×10^{-2} microns and with no voltage applied, the depletion layer of a p-n junction, has a width of the order of 0.8 microns; that is, about 20 Debye lengths. Thus with channel widths of the order of two microns the usual assumption of abrupt termination of space charge on the neutral semiconductor is no longer valid. Again under normal operation of the field-effect transistor, when the channel is near "pinched off," the transition regions occupy nearly the whole width of the channel.

With the drain voltage near the pinch-off value and the channel narrowed at the drain end of the gates, the width of

transition regions becomes comparable to the residual width of the channel. When the two transition regions meet at the center of the channel, the channel passes from its neutral state to quasi-neutral state. This partial depletion of the channel gives rise to a spatial variation of the majority carriers. As a consequence, double layers are formed normal to the current flow; these modify the current in a manner similar to the emitting and collecting junctions of a bipolar transistor.

3.1 Geometry of the Model

The device is schematically represented by two abrupt p-n junctions placed symmetrically with respect to the center of the channel [See Figure 3.1]. Uniform impurity doping of N_a atoms/cm^3 in the gates and of N_d atoms/cm^3 in the channel is assumed. The source and drain contacts are placed at x = 0 and x = b respectively. The gate metallurgical junctions M_1 and M_2 are placed at y = 0 and y = 2a respectively. In order to simplify the mathematical formulation, the gate contacts are taken to be overlapping the source contact. Also, in order to make the analysis tractable several assumptions are made. These are outlined in the next section.

3.2 Assumptions

1. The gates are metallic (degenerate) so that the depletion region is entirely in the channel, i.e., $N_a >> N_d$.

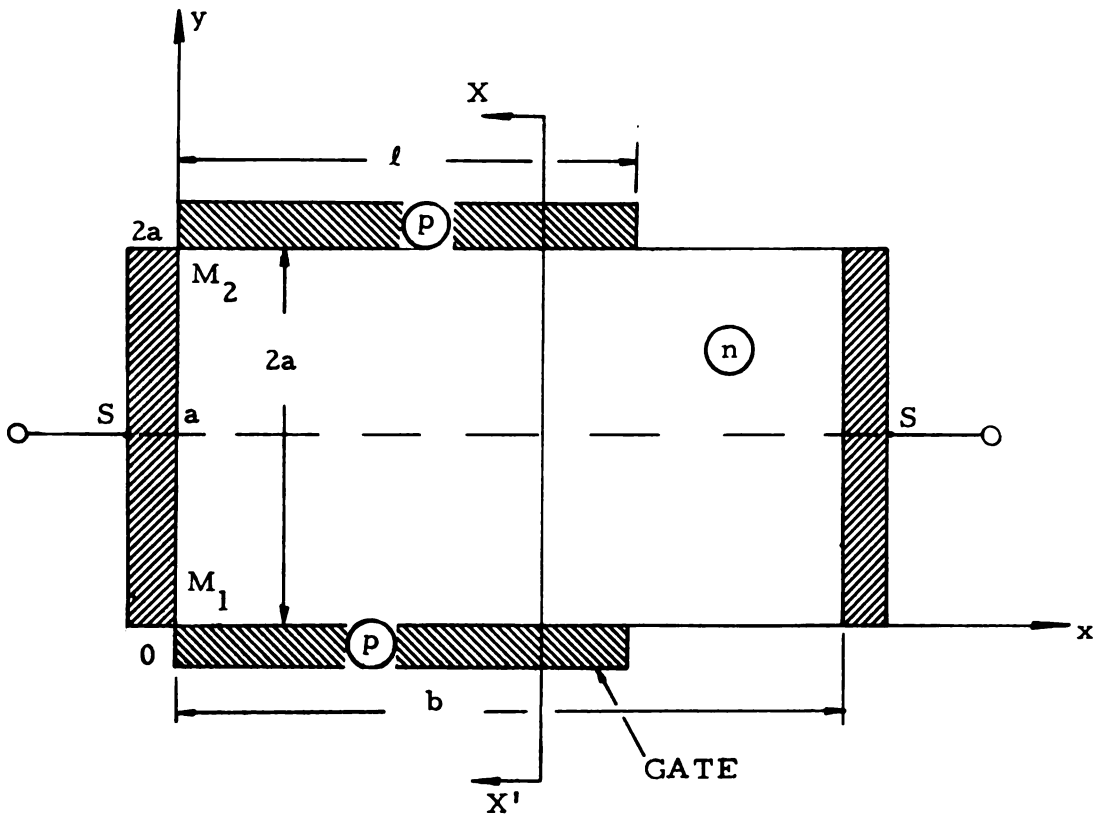


Figure 3.1. JFET model.

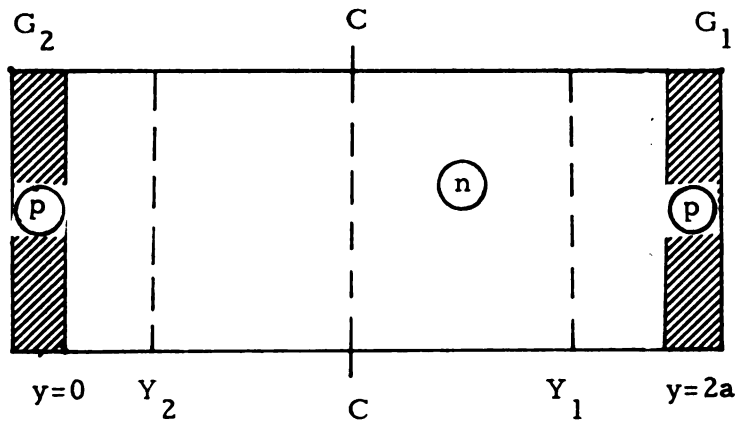


Figure 3.2. Section at xx' of Figure 3.1.

2. The potential in the absence of applied gate voltage at the metallurgical junctions (at y = 0 and y = 2a) is taken to be as zero. This also is taken as the boundary condition.

3. The donor impurity atoms in the channel are completely ionized. Also, the space charge region of the gate channel junctions is completely depleted of the majority carriers.

4. The channel current is only due to the majority carriers. The recombination and generation in the gate transition region and the channel is ignored.

5. The current flow in the channel is entirely due to the longitudinal component of the field, such that,

$$E_x(x, y) = E_x(x).$$

6. The reverse current of the gate junctions is neglected.

7. The boundary between the space charge of the gate and the channel is taken as abrupt. Also, the charge density in the channel, at right angles to the current flow, is approximated to have a constant value which will give the same current as would be obtained by the integration of current density in the actual channel.

8. The two cases of majority carrier mobility are considered: (1) mobility independent of the electric field, and (2) mobility related to the electric field as formulated in Section 2.5.

3.3 Mathematical Model

The analysis of a field-effect transistor involves the knowledge of the majority carrier distribution. This is obtained by solving simultaneously Poisson's equation, the Continuity equation, and the Transport equation; subject to constraints imposed by

the geometrical configuration of the device and the external bias voltages.

In this work, a simplified form of the current transport equation, combined with the Poisson's equation and the continuity equation for the majority carriers, is taken as the mathematical description of the device.

Equation (1) is the Poisson's equation which relates the divergence of the electric field [$E(x, y) = -\text{grad } V(x, y)$] to the charge density arising out of the mobile charge carriers, $p(x, y)$ and $n(x, y)$ (holes and electrons, respectively) and immobile impurity atoms $N(x, y)$. Equations (2) and (3) are the Transport equations and express the current density, in terms of electron and hole concentration, mobilities u_n and u_p and diffusion constants D_n and D_p. Equations (4) and (5) are the Continuity equations and are in terms of the current densities due to electrons and holes; R_n and R_p are recombination and generation currents. Equation (6) is the total current.

$$\text{div grad } \psi(x, y) = -\frac{q}{k} [N(x, y) - n(x, y) + p(x, y)] \quad (1)$$

$$J_p(x, y) = -q D_p \text{ grad } p(x, y) + q u_p(x, y) p(x, y) \text{ grad } \psi(x, y) \quad (2)$$

$$J_n(x, y) = q D_n \text{ grad } n(x, y) + q u_n(x, y) n(x, y) \text{ grad } \psi(x, y) \quad (3)$$

$$\text{div } J_n(x, y) = -R_n \quad (4)$$

$$\text{div } J_p(x, y) = -R_p \quad (5)$$

$$J_t(x, y) = J_n(x, y) + J_p(x, y) \tag{6}$$

In addition to the above, Einstein's equations, are assumed valid:

$$D_n = V_t\, u_n(x, y)$$

$$D_p = V_t\, u_p(x, y)$$

where V_t is the thermal potential ($V_t = \frac{KT}{q}$; T is the absolute temperature of the device).

The analytical solution of these equations in terms of known mathematical functions is a difficult task; therefore, some approximation techniques are employed.

Since the field-effect transistor is a majority carrier device, the contribution, to the total current, of the minority carriers (in this case holes) is negligible. Therefore, this set of equations is further simplified by ignoring the presence of minority carriers and the absence of recombination and generation. The system then reduces to:

$$\text{div grad } \psi(x, y) = -\frac{q}{k}\left[N(x, y) - n(x, y)\right] \tag{7}$$

$$J_n(x, y) = q\, D_n \text{ grad } n(x, y) + q\, u_n(x, y)\, n(x, y) \text{ grad } \psi(x, y) \tag{8}$$

$$\text{div } J_n(x, y) = 0 \tag{9}$$

Equations (8) and (9) can be further simplified to one-dimensional form as is explained in the following sections.

3.4 Space Charge in the Channel.

Along any x-plane the gates and the channel form a p-n-p structure (see Figure 3.2). For a sufficiently wide n-region,

space charge effects at M_1 and M_2 do not cause a disturbance at C; hence, the two junctions can be analyzed independent of each other. However, for a narrow n-region, space charge at M_1 is not independent of that at M_2; therefore, the boundary condition at C must be chosen very carefully.

Consider the case when the drain and source are at the same potential so that a one-dimensional analysis can be undertaken. The junction at M_1 is described by the Poissons's equation

$$\frac{d^2\psi}{dy^2} = -\frac{q}{k}\left[N(y) + p(y) - n(y)\right] \tag{10}$$

where $N(y) = \begin{cases} N_d & ; \quad 0 \leq y \leq 2a, \\ N_a & ; \quad y \leq 0, \end{cases}$

and N_d and N_a are the Donor and Acceptor impurity density levels. Since the compensation is not relevant to our analysis, we will assume $N_a = 0$ in the n-region and $N_d = 0$ in the p-region.

Introducing the normalized potential $U = \alpha\psi$ we have in the n-region

$$U_n = \ln (n_n / n_i)$$

and

$$U_p = \ln (n_p / n_i),$$

where $\alpha = 1/V_t$.

In the n-region,

$$\frac{d^2\psi}{dy^2} = -\frac{q}{k}\left[p - n + N_d\right]$$

$$= -\frac{q}{k}\left[n_i \exp(-U) - n_i \exp(U) + N_d\right],$$

or alternately,

$$\frac{d^2U}{dy^2} = \frac{2n_i q^2}{KTk}\left[\frac{\exp(U) - \exp(-U)}{2} - \frac{N_d}{2n_i}\right]$$

$$= \frac{1}{L_d^2}\left[\mathrm{Sinh}(U) - \frac{N_d}{2n_i}\right] , \qquad (12)$$

where $L_d = \frac{KTk}{2n_i q^2}$ is the intrinsic Debye Length (33.8 microns in Silicon).

For large distances from the junctions (neutral region) the charge density from Equation (12) is zero and we can write

$$\mathrm{Sinh}(U_b) = \frac{N_d}{2n_i} ,$$

where U_b is the height of the potential barrier. In the quasi-neutral region, the potential can be writen as $U = U_b + \delta$, where δ is the small deviation from the equilibrium potential. Equation (12) can then be reduced to the linear form as

$$\frac{d^2U}{dy^2} = \frac{\delta}{L_{de}^2} \qquad (13)$$

where L_{de} is defined as the Extrinsic Debye Length, and

$$L_{de} = \left[\frac{KTk}{2q^2 n_i \sqrt{1 + (N_d/2n_i)^2}}\right]^{1/2} .$$

In a reasonably intrinsic material, L_{de} reduces to

$$L_{de} = \frac{L_d}{(N_d/2n_i)^2} .$$

Equation (13) shows that in a region where the departure from neutrality is small, the potential varies exponentially with position.

If the potential were exponentially dependent upon position, for large distances from neutrality, we would expect a distance of 5 to 6 Debye Lengths in order to change from complete neutrality to complete depletion.

Similarly, in the p-region,

$$\frac{d^2U}{dy^2} = \frac{1}{L_d^2}\left[\text{Sin h}(U) + \frac{N_a}{2n_i}\right] \tag{14}$$

Equations (12) and (14) can be integrated once under the conditions

$$\left.\frac{dU}{dy}\right|_{=-\infty} = \left.\frac{dU}{dy}\right|_{y=+\infty} = 0 \tag{15a}$$

$$U\Big|_{y=+\infty} = U_n \quad \text{and} \quad U\Big|_{y=-\infty} = U_p \tag{15b}$$

to yield

$$\left(\frac{dU}{dy}\right)^2 = \frac{2}{L_d^2}\left[\cos h\, U - \cos h\, U_n - (U - U_n)\frac{N_d}{2n_i}\right] \tag{16a}$$

$$\left(\frac{dU}{dy}\right)^2 = \frac{2}{L_d^2}\left[\cos h\, U - \cos h\, U_p + (U - U_p)\frac{N_A}{2n_i}\right]. \tag{16b}$$

Under reverse bias conditions, the Fermi levels ϕ_p and ϕ_n are assumed constant and parallel and are separated by a potential V across the junction (Figure 3.3). In effect, this assumption means that in the transition regions the spatial variation of n and p is dependent only on ψ. This will result in the free carriers being

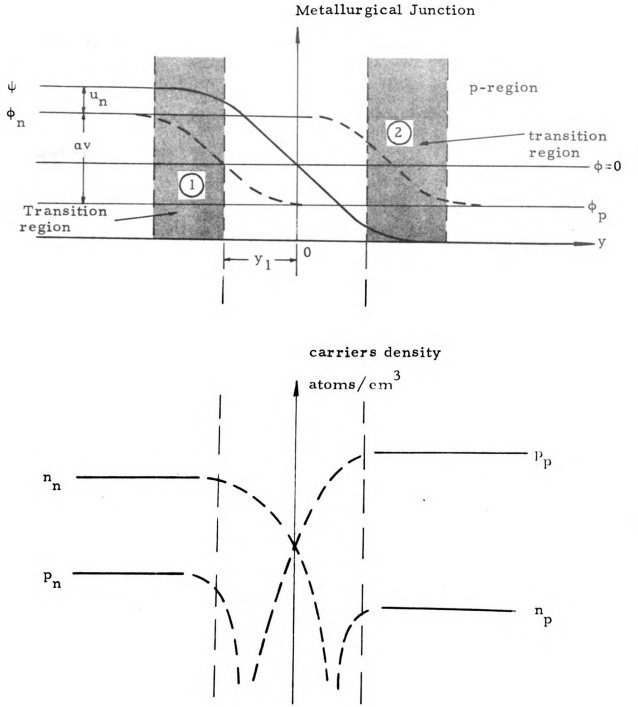


Figure 3.3. Electrostatic potential variation across a p-n junction; (a) reverse biased junction, (b) carrier density levels in the space charge regions.

slightly underestimated. However, in these regions where they are minority carriers, they do not contribute significantly to the total space charge.

If an average Fermi level $\phi = \frac{\phi_n + \phi_p}{2}$ is defined, then the new carrier concentration is

$$n = n_i \exp(U_n)$$
$$p = n_i \exp(-U_n + \alpha V), \tag{17}$$

and Equation (16a) becomes

$$\left(\frac{dU}{dy}\right)^2 = \frac{2}{L_d^2}\left\{\exp\left(-\frac{\alpha V}{2}\right)\left[\cosh(U) - \cosh\left(U_n + \frac{\alpha V}{2}\right)\right] + \frac{N_d}{2n_i}\left(U_n + \frac{\alpha V}{2} - U\right)\right\}. \tag{18}$$

Equation (18) is correct as long as condition (17) is valid. However, Equation (17) does not describe actual strength of the holes. This, as assumed earlier, does not cause any significant error because even in the bulk region, the concentration of holes is many orders of magnitude less than the electron concentration.

Let $(U - \alpha V/2) = U_d$. The the field in the transition region is

$$\frac{dU}{dy} = \frac{1}{L_d}\left[\exp(U) + \exp-(U_d + \alpha V) - \frac{N_d}{2n_i} U_d\right]^{1/2} \tag{19}$$

Even for moderately low negative bias (U_d is negative in most of the space charge region), the term $\exp-(U_d + \alpha V)$ can be ignored, and hence, the field in the transition region is

$$\frac{dU_d}{dy} \approx \frac{1}{L_d}\left[\exp(U_d) + \frac{N_d}{n_i} U_d\right]^{1/2} \tag{20}$$

Thus, the width of the transition region (see Figure 3.4) is independent of the bias. Also, the spatial variation of the electrostatic potential remains the same and is more or less logarithmic.

The boundary conditions at the junction between the n and p regions are

$$U\Big|_{y=-o} = U\Big|_{y=+o} = U_o$$

and

$$\left.\frac{dU}{dy}\right|_{y=-o} = \left.\frac{dU}{dy}\right|_{y=+o} . \tag{15c}$$

Combining Equations (15a), (15b) and (15c), the potential at the junction is

$$U_o = \frac{\cosh(U_p) - \cosh(U_n) + (N_d U_n + N_A U_p)/2n_i}{(N_D + N_A)/2n_i} . \tag{21}$$

for an unsymmetrical junction.

For an infinitely thin n-region, the boundary condition for the space charge is defined by

$$\left.\frac{dU}{dy}\right|_{y=+\infty} = 0$$

and

$$Q(y)\Big|_{x=C} = N_d - n_i \exp(U_n) + n_i \exp(-U_n + \alpha V) \tag{23}$$

without a serious error. The corresponding equation in the p side is

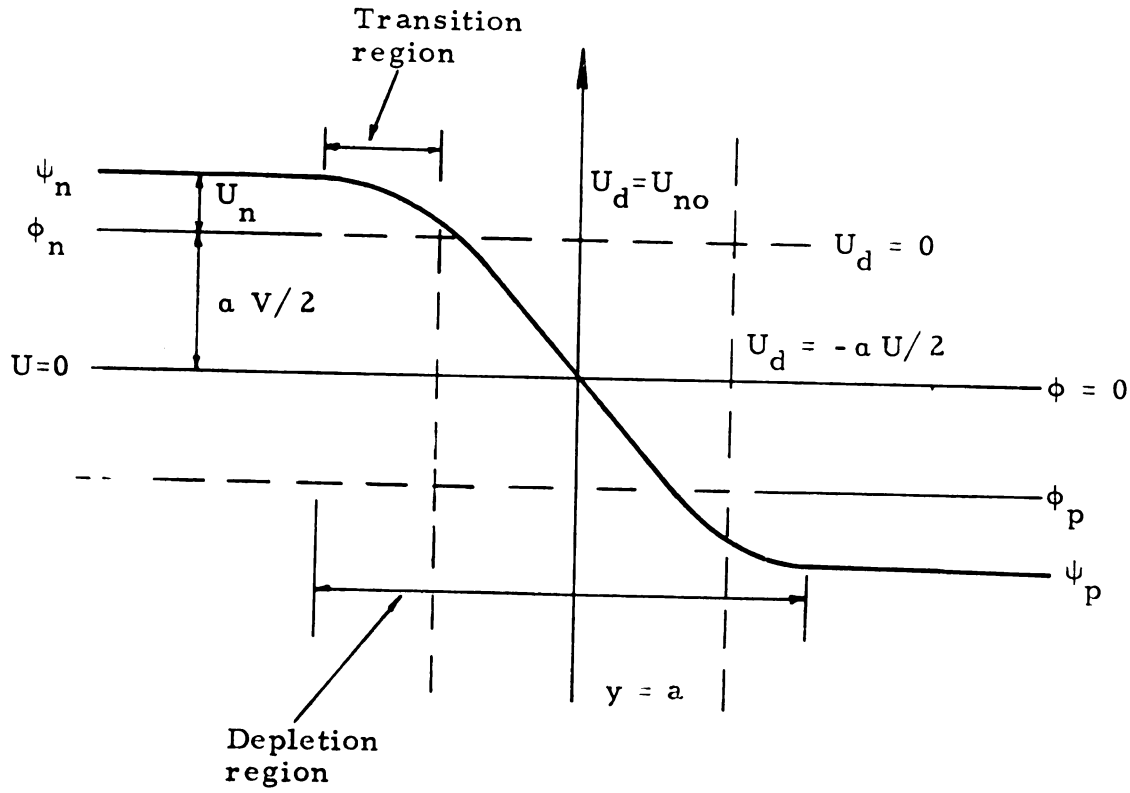


Figure 3.4. Effect of bias on the width of a transition region (Equation 29).

$$\left(\frac{dU}{dy}\right)^2 = \frac{2}{L_d^2}\left\{\exp\left(-\frac{aV}{2}\right)\left[\cosh U - \cosh U_p\right] + \frac{N_A}{2n_i}\left(U + \frac{aV}{2} - U_p\right)\right\} \quad (24)$$

Note: The far side in the p-region is the gate contact where ϕ_n and ϕ_p coincide.

Variation of bulk potential U_b in the p-region can be shown to be defined by the equation

$$U_b = \frac{\cosh U_p - e^{-aV/2} \cdot \cosh\left(U_n + \frac{aV}{2}\right) + \frac{N_D}{2n_i}\left(U_n + \frac{aV}{2}\right) + \frac{N_A}{2n_i}\left(U_p - \frac{aV}{2}\right)}{\left(\frac{N_D}{2n_i} + \frac{N_A}{2n_i}\right)} \quad (25)$$

The computed values of U_b are sketched in Figure 3.5 for various bias voltages.

For junction, field-effect transistors the electrostatic potential gradient passes through zero at the center of the channel. We always have a potential maxima at this point. If the channel width is reduced either through metallurgy or by increased reverse bias, then, for a fixed distance between the gate junctions, the potential maxima is lowered. Figure 3.6 depicts modified potential at the channel center. The corresponding majority carrier density is now lower than its value in the neutral region. The lowered potential maxima in the channel gives rise to two interesting situations:

1. For an extremely narrow n-region and the junctions in thermal equilibrium ($pn = n_i^2$), the electrostatic potential meets the

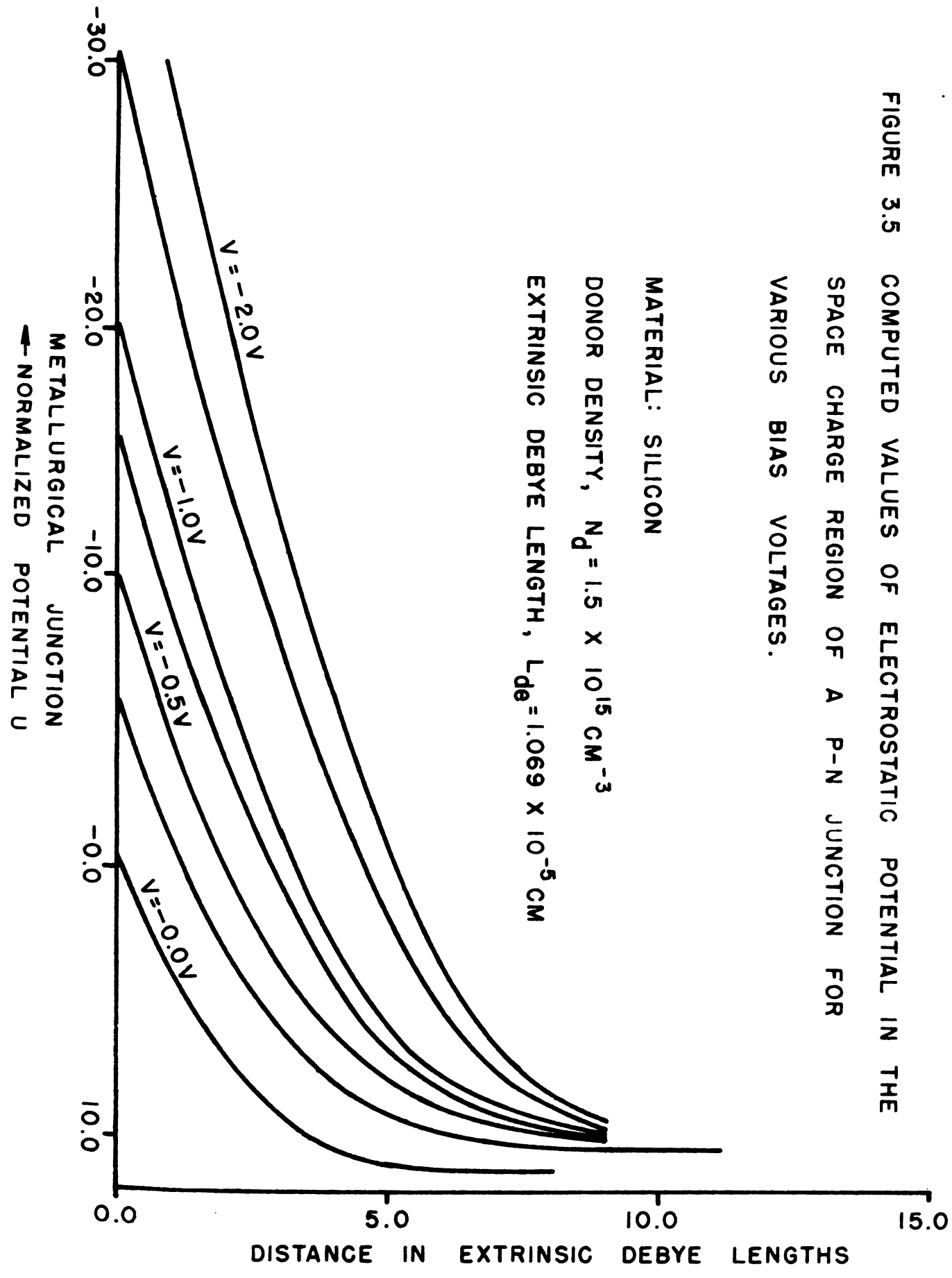


FIGURE 3.5 COMPUTED VALUES OF ELECTROSTATIC POTENTIAL IN THE SPACE CHARGE REGION OF A P-N JUNCTION FOR VARIOUS BIAS VOLTAGES.

MATERIAL: SILICON

DONOR DENSITY, $N_d = 1.5 \times 10^{15}\ CM^{-3}$

EXTRINSIC DEBYE LENGTH, $L_{de} = 1.069 \times 10^{-5}\ CM$

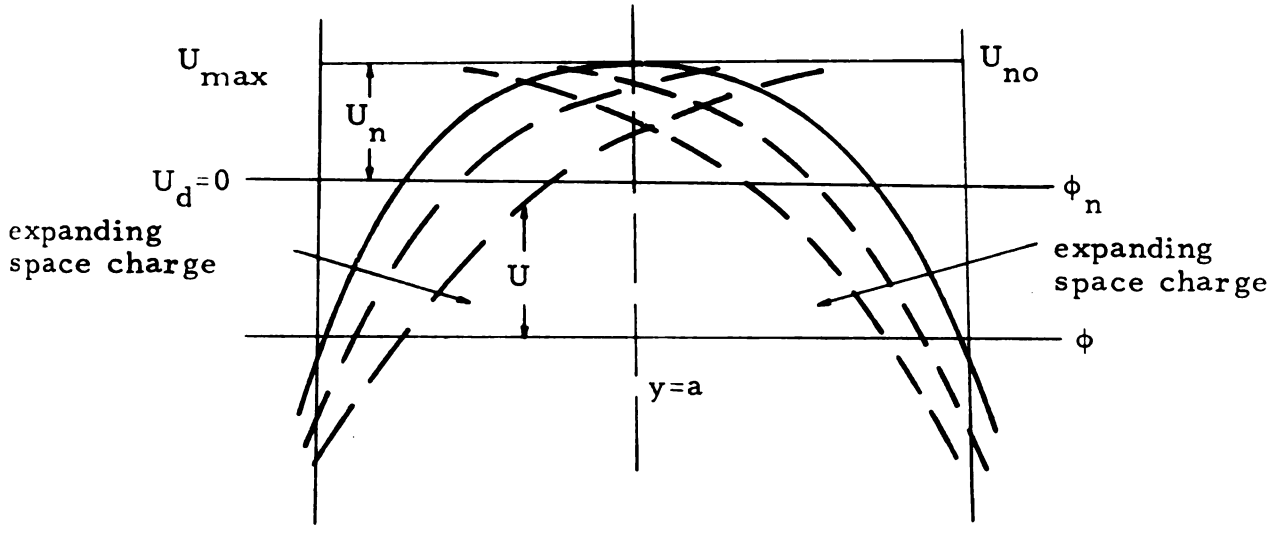


Figure 3.6. Gate space charge in a symmetrical channel.

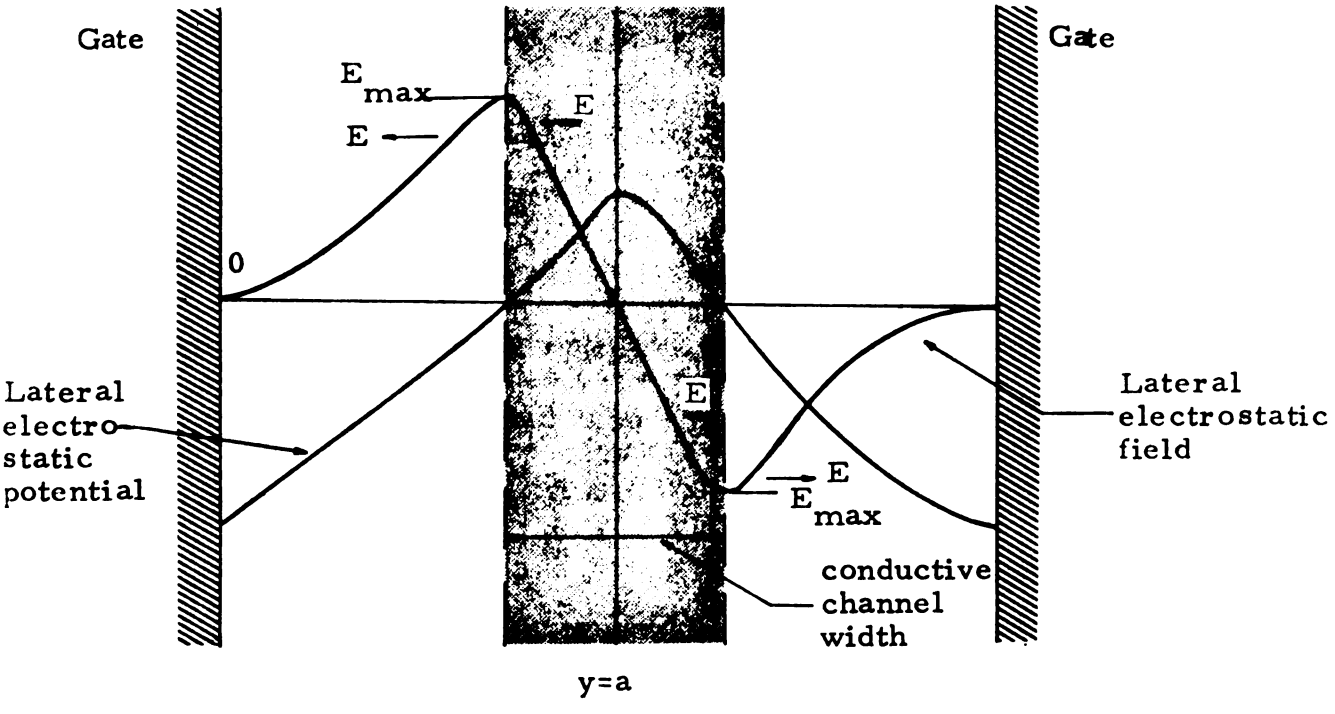


Figure 3.7. Variation of electrostatic potential and field normal to the flow of channel current.

Fermi level and the channel becomes intrinsic. For an n-region width of the order of 0.1 micron in Silicon, the electron density falls below the equilibrium value at the cost of increased hole concentration. This gives rise to an inversion layer in the channel.

2. In case of reverse bias on the gates the hole electron product is given by $np = n_i^2 [\exp -(\alpha V)]$. For narrow n regions, when the electrostatic potential meets the Fermi level, the density of holes is many orders of magnitude lower than the electron concentration; hence, before inversion can occur, the channel is already depleted. Thus, in the case of an FET, the inversion is not the cause of current saturation, as is predicted by Goldberg.

Again, as shown by Equation (20) and Figure 3.5, the depletion layer does not terminate abruptly on the neutral region and the depletion of channel is a continuous process. The channel current instead of suddenly going to zero, as predicted by complete depletion theory, is now governed by the behavior of the space charge of the partially depleted channel. The nature of this space charge is investigated in the next section.

Figure 3.7 shows quantitatively the variation of lateral field in a partially depleted channel. The field is of such a polarity that the electrons are not swept away by the gates but are rather

restricted to a narrow region around the center of the channel. The drain current is still confined to the central part of the channel where the conductivity is the highest. Away from the center, the electron density decreases almost exponentially, and for all practical purposes, it can be taken as constant at some effective value n_{eff} over the width of the channel. For the rest of the analysis, the lateral variation in the electron density and the electrostatic potential is ignored. Thus, the Equations (8) and (9) reduce to a one-dimensional form:

$$J_n(x) = q D_n \text{ grad } n(x) + q u_n(x) n(x) \text{ grad } \psi(x) \qquad (26)$$

and

$$\text{div } J_n(x) = 0 . \qquad (27)$$

Equations (26) and (27) along with Equation (7) describe completely the behavior of the FET.

3.5 Mechanism of Drain Current Saturation.

With increasing reverse bias on the gates (either through applied voltage at the gates or as a consequence of the drain current flow), the neutral channel narrows to such an extent that its width is comparable to the width of the transition regions of the space charge of the gate channel junctions. The transition region of one space charge instead of terminating on the neutral channel now encounters the transition region of the second space charge as a boundary. A further increase in the reverse bias results in the 'partial depletion' (section 3.4) of the channel at its narrowest

point (electron density falls below its equilibrium value, but is larger than the intrinsic carrier density). The uncompensated impurity centers at this point give rise to a positive space charge. The conductive channel is no longer neutral and has a spatial variation of the majority carriers, at the y = 0 plane, as depicted in Figure 3.8.

The positive space charge in the conductive channel modifies the flow of the drain current in a very significant manner. For a qualitative explanation the following terms are defined:

1. 'Gradual Channel' - The part of the neutral conductive channel between the source and the 'pinched-off' region (S - A). The current flow and the dimensions of this part of the channel are described by Shockley's gradual channel approximation [1].
2. 'Pinched-off Region' - That part of the channel where the carrier density is below its equilibrium value.
3. n^- - The carrier density in the pinched-off region. Its value is solely determined by the bias on the gate junction.

Because of its higher resistivity the pinched-off part of the channel absorbes a larger part of the drain voltage than would the same length of neutral channel. The carriers are now subjected to an increased drain field and move with a greater velocity.

The current flow in the gradual channel is purely due to drift field and is governed by Ohm's law. However, in the 'pinched-off' part of the channel, the current has a large diffusion component. The diffusion density gradient in the region AB acts like an injecting

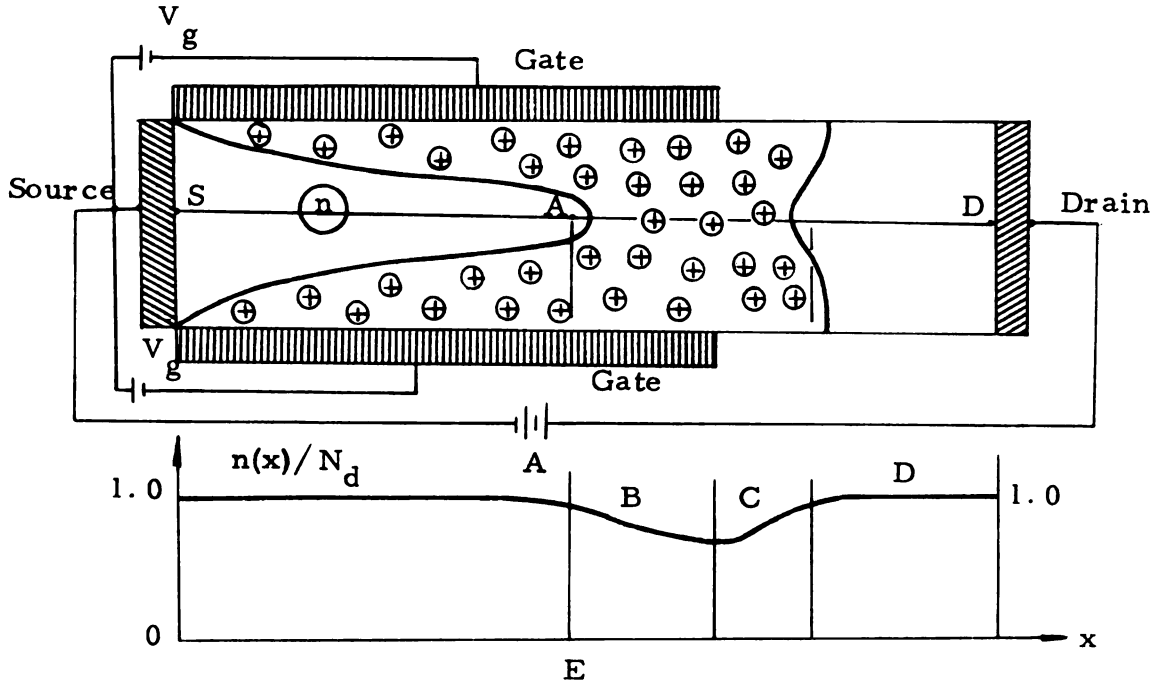


Figure 3.8. Majority carrier density in a "partially" depleted channel for V_d V_p.

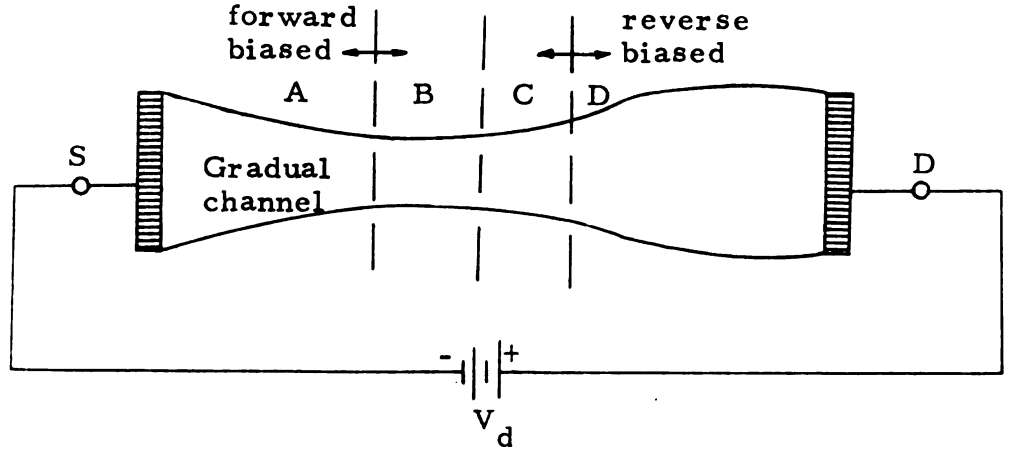


Figure 3.9. Conductive channel analogous to a n-p-n bipolar transistor.

junction. The injection is further aided by the drain field which 'forward biases' this junction. In the region CD the diffusion density gradient is in the opposite direction and impedes the flow of carriers towards the drain contact. The drain contact field acts as a reverse bias on this 'junction'. Thus, the carriers 'injected' by the forward biased 'junction' AB are accelerated by the field in the region BC and are then 'swept away' by the 'reverse biased junction' CD. The current is thus analogous to that of a n-p-n transistor as pictured in Figure 3.9.

The three salient characteristics of the device at this point are:

1. An increase in drain voltage is absorbed, in most part, across the 'junction' CD. The control of the drain voltage on the current is thus reduced.
2. The current 'injected' by the 'junction' AB is determined by its diffusion potential and is limited by the resistance of the gradual channel. This resistance is a function of its length, V_g and V_p. The 'injected' current, therefore, stays constant, for a fixed V_g and with changing drain voltage.
3. The redistribution of majority carriers in the channel gives rise to two High-Low junctions (Appendix A). The high-low junction at AB causes a voltage minima and therefore a zero field at point E. This is equivalent to a virtual cathode being

present at E, and the device behaves as a temperature saturated cathode current device.

For $V_d > V_p$ the length of 'pinched-off' channel (n^- region) increases because of expanding space charge towards the source contact. This effects the current in the following ways:

1. Increased resistance of the gradual channel tends to reduce the injected current.
2. Current increases due to the increased field across the 'pinched-off' channel.
3. A virtual cathode at E and the space-charge density in the 'pinched-off' region are precisely the conditions for a space charge limited current (the current is proportional to $E^{3/2}$[2]. However, any increase in the field also increases the length of the n^- region. The net effect is a slight increase in the drain current with drain voltage.

The current saturation in the above model is thus a consequence of the space charge in the channel. The mobility dependence on the field and space charge limited current effects only appear as second order effects. The gates control the current by reducing the dimensions of the gradual channel and thus decreasing the injected current available to the 'junction' AB.

3.6 Solution of Transport Equation.

If the transport equation (26) is combined with equation (27), we obtain

$$d\dot{w}\,[J_n(x)] = 0$$

$$= d\dot{w}\,[q\,U_n(x)\,n(x)\,\text{grad}\,\psi(x) + q\,D_n\,\text{grad}\,n(x)]\,. \tag{28}$$

Substituting for n(x) from the Boltzman's equation

$$n(x) = n_i \exp a(\psi - \phi)\,,$$

we get

$$\text{div}\,[qU_n(x)\,n(x)\,\text{grad}\,\phi(x)\,] = 0.$$

The drain current at any section of the channel is constant and is obtained by the integration of Equation (29) over the width of the conductive channel. The drain current is

$$I = 2\int_o^{w(x)} J_n(x)\,dy$$

$$= 2\int_o^{w(x)} q\,U_n(x)\,n(x)\,\text{grad}\,\phi(x)\,dy$$

$$= 2\,q\,n_i\,\text{grad}\,\phi(x)\exp[-a\phi(x)]\int_o^{w(x)} U_n(x)\exp[a\psi(x)]\,dy$$

$$= 2\,q\,n_i\,\text{grad}\,\phi(x)\exp[-a\phi(x)]\,F(x)\,, \tag{30}$$

$$\text{where } F(x) = \int_o^{w(x)} U_n(x)\exp[a\psi(x)]\,dy \tag{31}$$

Rewriting Equation (30) in terms of $\phi(x)$ and integrating with respect to x yields,

$$\exp[-a\phi(x)] = \frac{aI}{2qn_i}\int_o^{w(x)}\frac{dx}{F(x)} + C_n\,,$$

where C_n is the integration constant. Taking the limits of integration as x and b and expressing c_n in terms of the boundary

conditions at the point b we have

$$\exp\left[-\alpha\phi(x)\right] = n_i \exp\left[-\alpha\phi(b)\right] + \frac{\alpha I}{2qn_i} \int_x^b \frac{dx}{F(x)}$$

Substituting from the Boltzman's equation the values of $\phi(x)$ and $\phi(b)$ the electron density in terms of the applied drain voltage is given by

$$n(x) = \exp\left[\alpha\psi(x)\right]\left[n(b) \exp\left[-\alpha\psi(b)\right] + \frac{\alpha I}{q N_d} \int_x^b \frac{dx}{F(x)}\right] \quad (32)$$

If the electron density is evaluated at the $x = 0$, then from Equation (32) we obtain an expression for the drain current as a function of the applied drain voltage and the boundary conditions for the electron density:

$$I = \frac{2qN_d}{\alpha} \frac{n(0) - n(b) \exp\left[-\alpha\psi(b)\right]}{\int_0^b \frac{dx}{F(x)}} . \quad (33)$$

The only approximation in the solution of the transport equation was in ignoring (section 3.5) the lateral component of current in the transition regions between the gate and the channel.

The set of two boundary conditions n(0) and n(b) at the external contacts 0 and b is in general given by the relationships involving the currents at the external contacts. Assuming the simplest form of the contacts of the ohmic type, the boundary conditions are:

$$n(0) = n_N$$

and (32.1)

$$n(b) = n_N ,$$

where n_N is the electron equilibrium density at the external contacts of the n-type material. An equivalent definition requires charge neutrality at the contacts:

$$n(0) - p(0) - N_d(0) = 0$$

and

$$n(b) - p(b) - N_d(b) = 0 .$$

Since the Fermi levels for the holes and electrons coincide at the contacts, the hole electron product is given by $np = n_i^2$ and hence the boundary conditions can be written in terms of the doping concentrations as:

$$n(0) = n_N = \sqrt{\frac{N_d(0)}{2}^2 + 1} + \frac{N_d(0)}{2}$$

for $N(0) \geq 0$,

where $n(b) = n_N$. (32.2)

3.7 Numerical Method

In order to explain the first and second order effects responsible for current saturation in the FET, knowledge of the detailed picture of the distribution of the carriers and voltage in the channel is necessary. However, because of the nonlinear nature of Poisson's equation [Equation (7)], an analytical solution is impossible and, therefore, recourse is taken to the numerical

methods of solution. Of the various numerical methods of solution the choice is limited by the accuracy, a guarantee of convergence, the total time of computation and, most important of all, the mesh size. A large number of mesh points indicates the difficulty in a method in actual computation in that it requires a large storage space and large computation time.

The most straight-forward numerical method of solution is via the relaxation techniques. Through a judicious selection of the mesh size and the relaxation factor, the convergence of this scheme is more or less assured. However, 10 to 15 iterations are needed for a fourth place decimal accuracy. Another disadvantage of this technique is that it requires a storage space for 2(N x M) words per variable (where N and M is the number of node points in the x and y direction, respectively).

For a reasonable amount of accuracy the mesh size should be less than or at least comparable to the extrinsic Debye Length--the characteristic length of decay of voltage in Equation (20). Also, an FET, in saturation, should be analyzed for drain voltages of the order of t to 10 times the pinch-off voltage. In the solution of the transport equation (Equation 32), the size of the numbers range between $\exp(40\,V_D)$ and $\exp(-40\,V_d)$. Thus, if $V_d = 5\,V_p$ the largest number is $\exp(200\,V_p)$. So that these numbers can be handled efficiently in a large sized computer, the value of V_p should not

exceed 2 volts. From equation (13) the extrinsic Debye Length L_{de} and the pinch-off voltage V_{pa} are related by the equation

$$a/L_{de} = 2V_p/V_t \approx 80V_p,$$

where a is the half-channel width. Thus from the point of view of the size of numbers which can be safely handled in a computer we have

$$a/L_{de} \leq 160.$$

As was assumed in section 3.2, if the transition between complete depletion and neutrality is taken to be abrupt then

$$\frac{\text{Length of transition region}}{\text{Half-channel width}} < 0.1.$$

The length of the transition region has been determined in Equation (13) and therefore,

$$5L_{de}/a < 0.1$$

or

$$a/L_{de} > 50.$$

In short devices (devices in which the gradual channel approximation does not apply), let

$$b/a = 2.0.$$

If $a = 50L_{de}$ then: $N = 101$ and $M = 101$.

Thus for a numerical solution via relaxation techniques, the storage space needed is of the order of 2(101 x 101) words per variable.

In this work a truncated Fourier's series is used to construct the required function; since the function can be constructed in one step--the required number of storage spaces is therefore, only $N \times M = 101 \times 101$. Advantage is taken of the symmetry of the device structure and thus we need only $N \times M/2$ storage spaces. The required

number of storage spaces can be further reduced if the device length is divided into sections. The required functions are then constructed in one section at a time. In fact the entire computer program was developed for IBM 1800 computer which has storage space of about 2500 real variable words.

3.8 Solution of Poisson's Equation

For any drain voltage V_d and gate voltage V_g, the shape of conducting channel is a function of x (Figure 3.10). If V(x,y) is the potential in the rectangular region x = 0, x = b, y = 0, and y = 2a, the net charge density in the channel is defined by the equation

$$\frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2} = -Q(x,y)/k \qquad (34)$$

where $Q(x,y) = -q(N_d-n) \quad -qN_d; \quad 0 \le y \le Y_1(x)$

$= -q(N_d-n); \quad Y_1(x) \le y \le Y_2(x)$

$= -q(N_d-n) \quad -qN_d; \quad Y_2(x) \le y \le 2a,$

where N_d is $\le$ the donor density in the channel and n is the density of the mobile majority carriers. The boundary conditions on V(x,y) are

$V(x,0) = V(x,2a) = V_b(x)$,

$V(b,y) = V_d$, and

$V(0,y) = 0$.

Let $L = \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} \equiv$ Laplacian.

Let F(x,y) satisfy LF=0 and

$F=V_b$ on boundary.

Let V - F = G such that G is zero on the boundary. Therefore,

LG = LV - LF

= LV; because LF = 0.

Therefore,

$$F(b,a) = \frac{4V_d}{\pi} \sum_{N=1}^{\infty} \frac{1}{N} \text{Sin } N\pi/2 \quad N = 1,3,5,.... \tag{38}$$

$$= \frac{4V_d}{\pi} \cdot \frac{\pi}{4} = V_d; \; [y \neq 0 \text{ and } y \neq 2a].$$

The effect of this term on the channel current (b/a greater than 10) can be ignored. However, for smaller channel length to width ratios, this effect is very significant.

The solution of LG = 0 with G = 0 on the boundary can again be represented by a two-dimensional Fourier's series:

$$G(x,y) = \sum_{M=1}^{\infty} \sum_{N=1}^{\infty} A_{MN} \text{Sin } \frac{M\pi y}{2a} \cdot \text{Sin } N\pi x/b \; , \tag{39}$$

where A_{MN} is the coefficient determined by the boundary conditions such that

$$A_{MN} = -\frac{64}{M\pi^3} \frac{V_p}{b} \frac{1}{M^2+\left(\frac{2aN}{b}\right)^2} \left\{ \frac{2}{N\pi} \text{Sin}^2 \frac{M\pi}{2} \cdot \text{Sin}^2 \frac{N\pi}{2} \right.$$

$$\left. -\frac{1}{b} \int_o^{g_1} n(x) \text{Sin } \frac{M\pi}{2} \text{ Sin } \frac{M\pi}{4} \frac{W(x)}{a} \cdot \text{Sin } \frac{N\pi x}{b} \, dx \right\}$$

$$= -\frac{64}{M\pi^3} \frac{V_p}{b} \frac{1}{M^2+\left(\frac{2aN}{b}\right)^2} \left\{ \frac{2}{N\pi} \right.$$

$$\left. -\frac{1}{b} \int_o^{g_1} n(x) \text{Sin } \frac{M\pi}{2} \cdot \text{Sin } \frac{M\pi}{4} \frac{W(x)}{a} \cdot \text{Sin } \frac{N\pi x}{b} \, dx \right\}$$

for all values of N and for all odd values of M. (40)

Thus LF = 0 with F = V_b on the boundary and LG = Q(x,y) with V = 0 on the boundary is the solution of Equation (7).

The solution of LF = 0 is a two-dimensional Fourier series

$$F(x,y) = \sum_{N=1}^{\infty} a_N \text{Sin } \frac{N\pi x}{2a} \cdot \text{Sinh } \frac{N\pi y}{2a},$$

where a_N is determined by the boundary conditions. The potential in the channel due to applied voltages is:

$$F(x,y) = \frac{4V_d}{\pi} \sum_{N=1}^{\infty} \frac{\text{Sinh } N\pi x/2a}{\text{Sinh } N\pi b/2a} \cdot \text{Sin } N\pi y/2a$$

$$+ \frac{2}{b} \sum_{N=1}^{\infty} \frac{\text{Sinh } N\pi y/b}{\text{Sinh } N\pi 2a/L} \cdot \text{Sin } N\pi x/b \int_o^b V_b(x) \cdot \text{Sin } \frac{N\pi x}{b} \cdot dx \qquad (35)$$

where $V(x,2a) = V(x,0) = V_b(x)$

$$= V_g \text{ for } 0 \leq x \leq g_L. \qquad (36)$$

For $g_L \leq x \leq L$; $V_b(x)$ is given by the solution of one dimensional Poisson's equation

$$\frac{\partial^2 V}{\partial x^2} = 0 \qquad (37)$$

such that $V_b(x = L) = V_d$.

The first term in Equation (35) is convergent for all odd values of N.

At x = a,

$$F(a,x) = \frac{4V_d}{\pi} \sum_{N=1}^{\infty} \frac{1}{N} \frac{\text{Sinh } N\pi x/2a}{\text{Sinh } N\pi b/2a} \text{ Sin } N\pi/2.$$

The term $\frac{\text{Sinh } N\pi x/2a}{\text{Sinh } N\pi b/2a}$ is much smaller than unity and is almost zero (for b/2a greater than 10) for all values of x except x = b, where

$$\frac{\text{Sinh } N\pi x/2a}{\text{Sinh } N\pi b/2a}\Big|_{x=b} = 1.$$

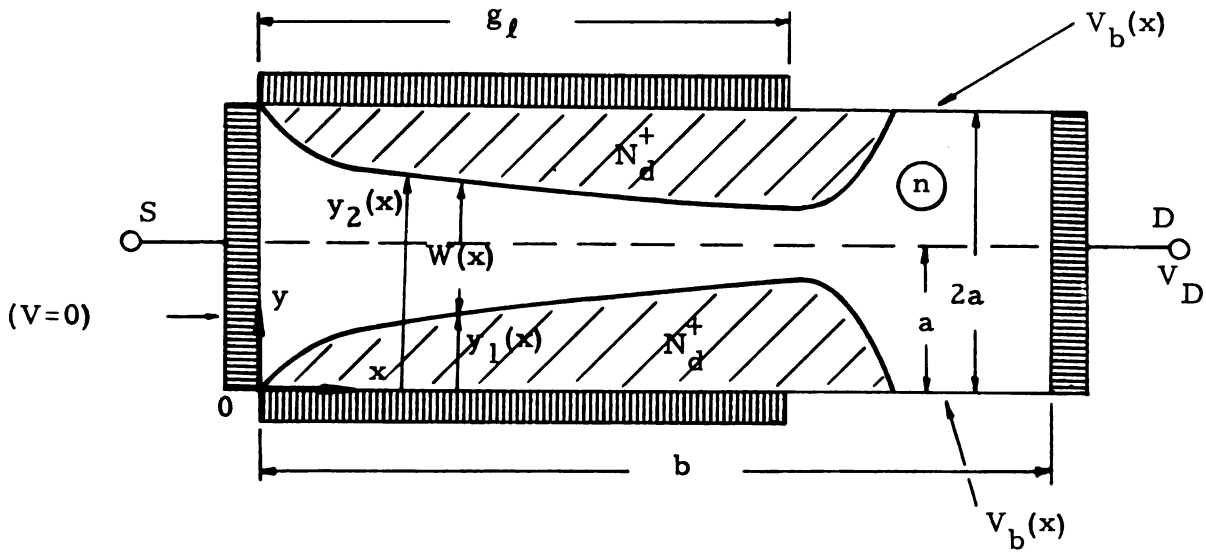


Figure 3.10. Coordinate system and device structure parameters used in the solution of Poisson's equation.

Equation (39) is the voltage due to space charge effects of the gates and channel current. The factor N(x) represents the effect of charge in the channel both due to the applied field and the channel current. In the region of the partially depleted channel, this component decreases; consequently, it tends to reduce the total voltage in the channel. (The second term of Equation (40) equals the first term for W(x)=2a). Any applied voltage on the drain contact increases the drain current until the reverse bias reduces the channel width to a point where a further reduction tends to reduce the voltage at that point. For large channel length to width ratios (b/a>>10) the terms of Equation (40) decay very rapidly with increasing values of M. For computational purposes the Fourier's series has been truncated and terms up to and including M=N=21 are considered. The step size taken was 0.05 normalized to half channel width.

3.9 Iteration Scheme

The six basic Equations (1) to (6) have been rearranged and approximated to set of three equations (7), (26) and (27). Equations (26) and (27) combined with the boundary conditions (32.2) define the electron concentration in Equation (32). The solution of Poisson's Equation (7), subject to the constraints of the applied voltage and geometrical boundaries, is given by Equations (35) to (37) and (40). In this new formulation of the problem, the electrostatic potential V(x,y), the electron density n(x) and the channel width W(x) are chosen as the independent quantities. These three quantities represent the unknowns of the reduced equations.

An iterative scheme is now used to cope with the various non-linearities of the problem. The complete iteration scheme is shown in Figure 3.11. The applied drain contact voltage V_d is specified. F(x,y)--the component of channel voltage due to V_d, is computed from Equation (35). A trial channel width $W^j(x)$ and a trial electron distribution $n^j(x)$ are chosen. To start the first cycle of the main iteration loop, $G^{j+1}(x,y)$--the component of channel voltage, due to the gate bias and channel current, is computed from Equation (40), in terms of $W^j(x)$ and $n^j(x)$. Total voltage in the channel $V^{j+1}(x,y)$ is the sum of $G^{j+1}(x,y)$ and F(x,y). $W^j(x)$ and $V^{j+1}(x,y)$ are used to compute, from Equation (32), the new value of electron density--$n^{j+1}(x)$. Poisson's equation with $V^{j+1}(x,y)$ is now used to obtain the charge density and hence the modified channel width $W^{j+1}(x)$. Solution of Poisson's Equation (34) with $n^{j+1}(x)$ and $W^{j+1}(x)$ yields an improved potential distribution. Iteration is continued until a stable value of drain current [Equation (33)] is obtained.

Different initial values of $W^{j+1}(x)$ and $n^{j+1}(x)$--other than those shown in Figure 3.11, can be chosen to hasten the convergence of the iteration scheme. The computed electron density $n^{j+1}(x)$ is tested for any unrealistic values (n(x) orders of magnitude larger than the impurity density N_d). In such a case a secondary iteration loop is used to scale down the voltage $G^{j+1}(x,y)$.

With this method complete freedom is available in the choice of impurity distribution, the carrier boundary conditions at the external contacts, and the dependence of mobility on the electric field and doping. If applied voltage V_d is specified, the method solves for total current and all the quantities of interest in the interior of device as a function of position.

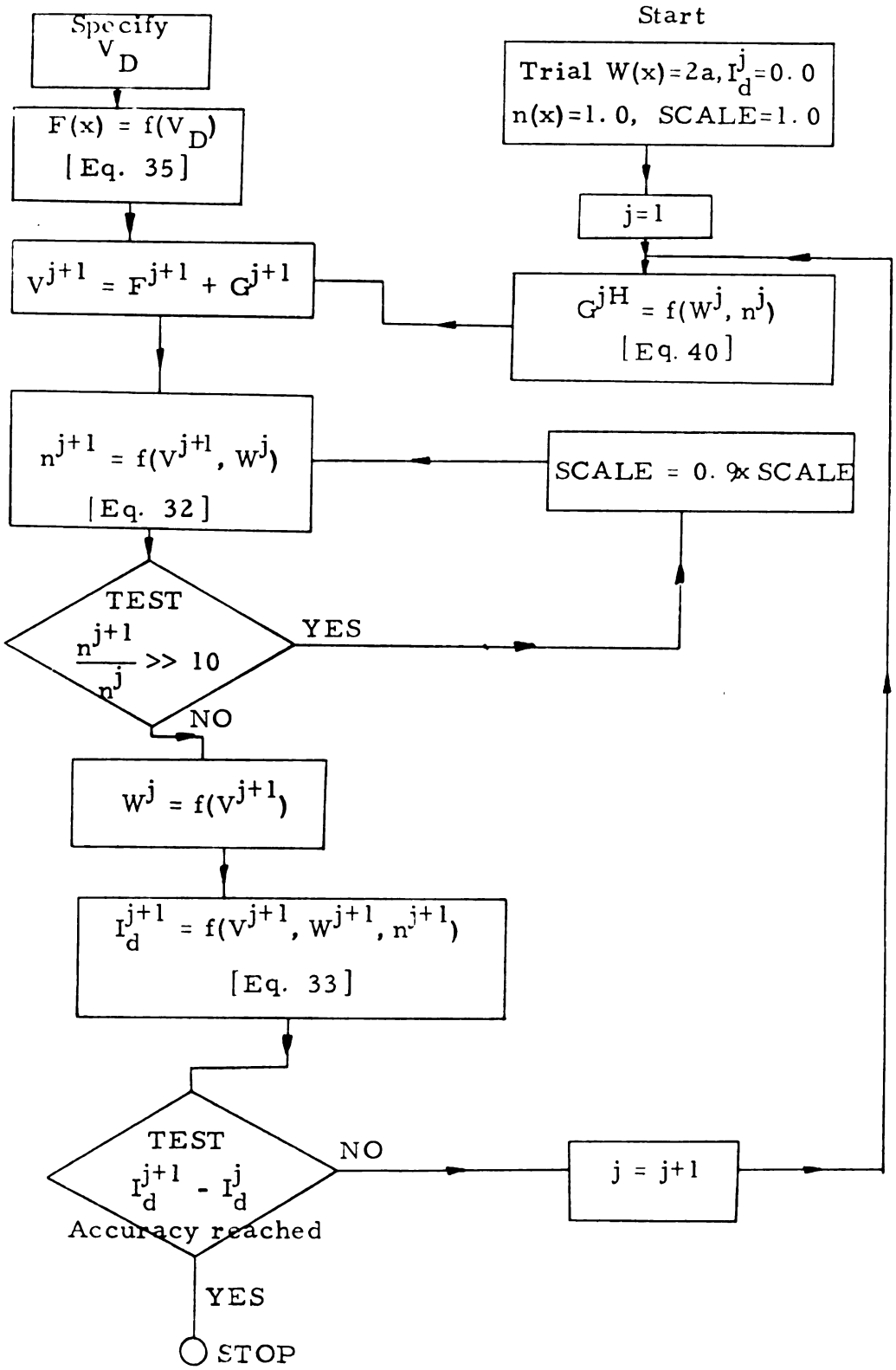


Figure 3.11. Block diagram of iterative scheme.

CHAPTER 4

RESULTS

Solutions obtained with the numerical procedure outlined in the previous chapter are presented for two special structures: (1) an n-channel FET with the gate length equal to a fraction of the channel length and (2) Shockley's model (gate and the channel of equal lengths; the gates overlap the source and the drain contacts). Distributions of electrostatic potential, mobile carrier density and the channel width are shown as functions of position throughout the interior of the device. The terminal property in the form of drain current versus drain voltage is illustrated. "Exact" and conventional approximate analytical results are compared and discrepencies are exposed.

In the previous chapter a numerical method of solution of the two-dimensional, one-carrier, transport equation and Poisson's equation describing the behavior of the FET has been described in detail. Although the method of solution and numerical technique allow for an arbitrary doping profile, boundary conditions at the external contacts, and mobility dependencies, the results for a special type of idealized structure are presented as an example of the numerical technique. The analysis is restricted to "short" structures ($b/a \ll 10$) so that the effects of drain field are accentuated. The choice of abrupt doping profiles has two motivations:

(a) the achievement of an analysis for the numerically worst case (abrupt boundary conditions).

(b) the comparison between "exact" and approximate analytical solutions are available only for idealized structures.

Motivation (b) also justifies the selection of appropriate constant values for the carrier mobilities.

In addition to the above assumptions, external contacts of ohmic type are specified for the device under consideration. The physical parameters characterizing the structure are listed in Table 4.1.

For efficient arithmetic relevant quantities are expressed in dimensionless form; the set of normalizing constants is chosen with the criterion of achieving the highest simplification in the relations of interest. The list of normalizing factors is given in Table 4.2.

Calculations were performed on the CDC 6500 system. The output data was punched on cards and displayed in graphical form with the help of HYPLOT routine on the IBM 1800 system. The computation time for one value of drain voltage is of the order of 18 seconds.

4.1 The Results of the Present Analysis

For various applied voltages the electron distribution, channel width, electrostatic potential and carrier mobilities are shown in Figures 4.1 to 4.6 for the structure I; the same set of quantities is shown in Figures 4.7 and 4.8 for the structure III and in Figures 4.9 to 4.10 for the structure II. Figures 4.11 and 4.12 illustrate the variation of electrostatic potential and carrier densities, for $V_d = V_p$, for channels of various initial widths. The drain current versus drain voltage characteristics is shown in Figure 4.13, for the three structures, for $V_d > V_p$. For $V_d < V_p$ the drain current is calculated only for the structure I. For all the above cases there was no significant variation in the general shape and size of the channel width, for $V_d > V_p$ and therefore only one curve is shown (Figure 4.5). For all the above results the carrier mobility was assumed constant with the electrostatic field.

Material:	Silicon (relative permittivity 12)		
Temperature:	300°K		
Intrinsic carrier density:	1.5×10^{10} cm^{-3}		
Doping:	n-channel, $N(x)=N_d=1.0 \times 10^{16}$ cm^{-3}		
	gates, $N(x)=N_a$=Metallic		
Mobility:	electrons, 1306.0 cm^2/volt-sec.		
Parameter	Structure		
	I	II	III
channel length:	80 L_{de}*	80 L_{de}	80 L_{de}
channel width:	20 L_{de}	40 L_{de}	20 L_{de}
Gate length:	80 L_{de}	80 L_{de}**	60 L_{de}
Pinch-off voltage:	1.293V***	5.172V	1.293V

Table 4.1. The physical parameters characterizing the FET structure, analyzed under steady-state conditions for various applied voltages.

---

* Unit of length in Extrinsic Debye Lengths.

** Voltage distribution on the drain contact is sinusoidal in the y-direction.

*** Unit of voltage in Volts.

DESCRIPTION	NORMALIZING QUANTITY	NORMALIZATION FACTOR	
		SYMBOL	NUMERICAL VALUE
position coordinates	x,y	a	
half-channel width	a	$L_{de}=V_t k/qN_d$	0.41407×10^{-5} cm
electrostatic potential		$V_t=KT/q$	0.02586 volt
applied (drain) voltage	V_d	V_t	0.02586 volt
Electric field	E	V_t	623.0 volt/cm
carrier density	n	N_d	1.0×10^{16}
diffusion (or barrier) potential	V_b	V_t	0.02586 volt
quasi-Fermi level	$\emptyset_n$	V_t	0.02586 volt
net impurity, donor, and acceptor densities	N, N_d, N_a	N_d	1.0×10^{16}

Table 4.2. List of Normalization factors for the quantities of interest

The weakness of the gradual channel theory is evident in Figures 4.3, 4.4, 4.10 and 4.12. The carrier density distribution has little resemblance for the first order idealization (neutral channel); even for structures with very wide channels the effect of drain contact field and the current space charge cannot be ignored.

For narrow channels (structures I and III), the channel is more or less depleted near the drain end. This kind of situation exists in modern devices with extremely low pinch-off voltages. Figure 4.2 illustrates the progressive depletion of the channel with increasing drain voltage. The carrier density passes through a minimum near the drain contact. For higher drain voltages ($V_d > V_p$) this minima lies and stays near the drain contact; also, it has a higher minimum value than in the case of lower drain voltages. This is due to the contribution of the space charge of increasing drain current (Figure 4.4). The minimum value of carrier density in the channel is dependent upon the device struture and drain voltages (see Figures 4.3, 4.4, 4.8, 4.10 and 4.12).

In the Figures 4.3, 4.8 and 4.10 the effect of drain voltage on the carrier density minimum should be noted; the minima moves towards the source contact with increasing drain contact field. This effect confirms Shockley's theory [1] of travelling pinch-Off point towards the source.

The carrier density minima near the drain contact (Figure 4.4) gives rise to a high-low junction. The confirmation for the presence of a second high-low junction is made by the magnitude of diffusion current in the channel; or, in other words, the gradient of the carrier density in the channel. Towards the left of the carrier

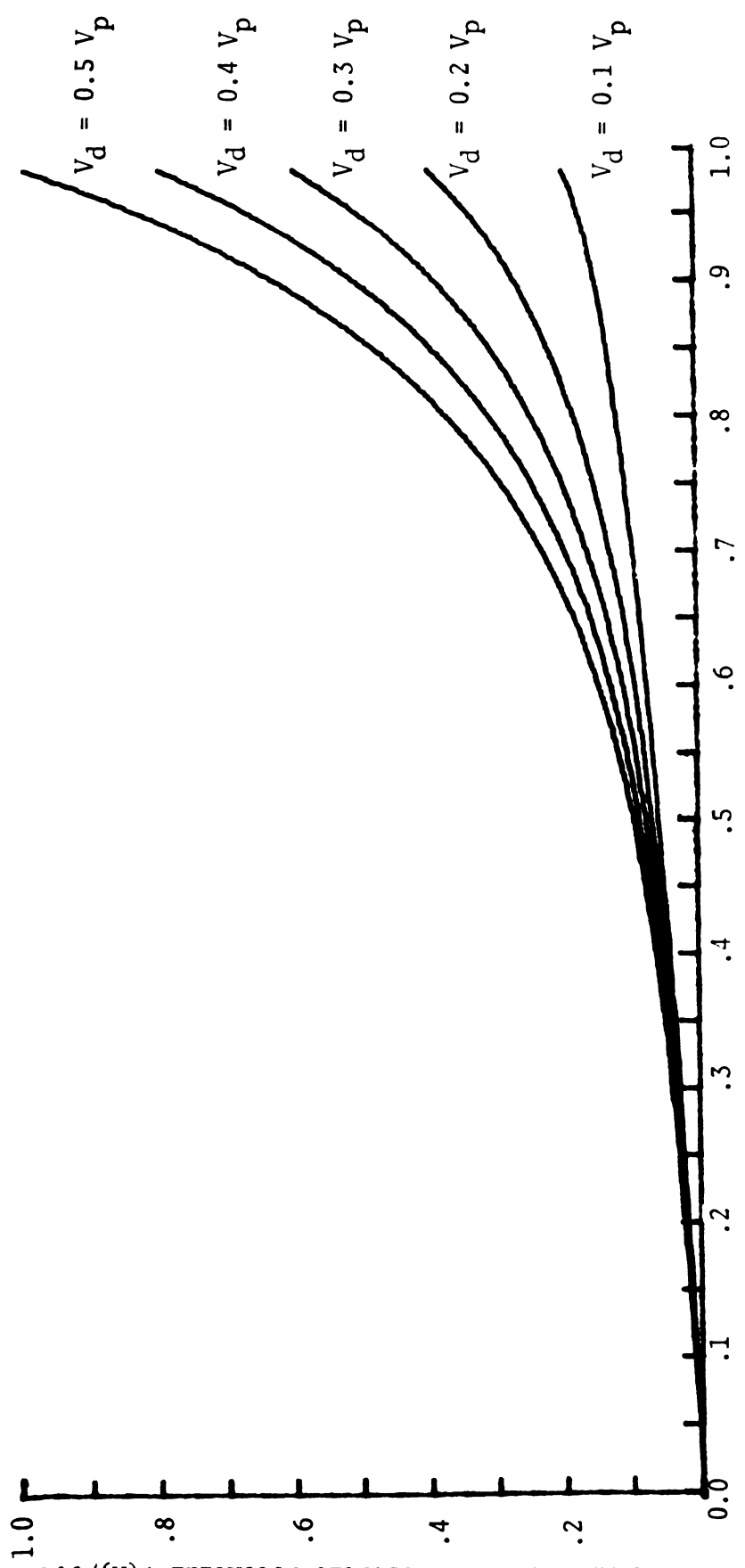


Fig. 4.1. Structure I; Electrostatic potential in the channel as a function of position.

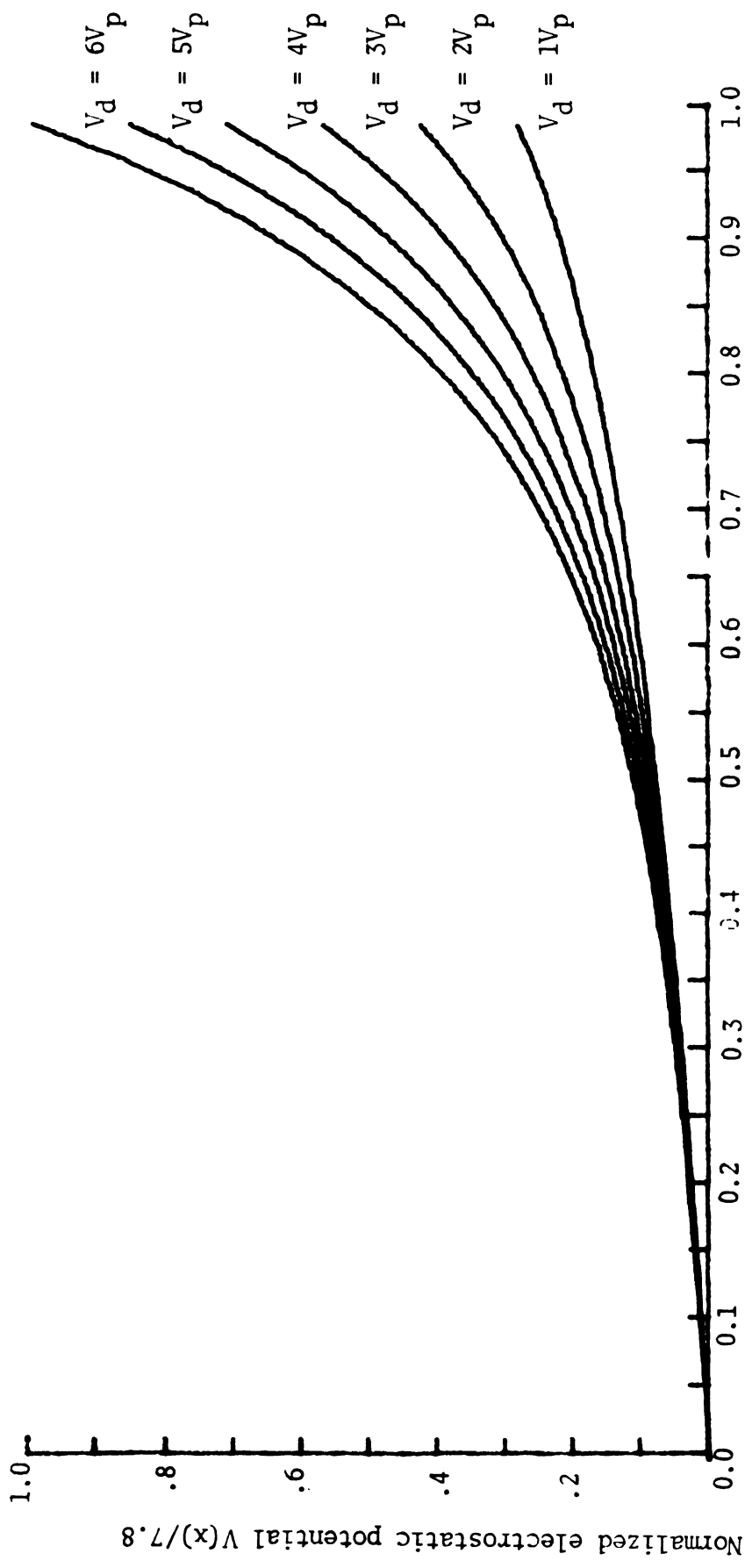


Fig. 4.2. Structure I; Electrostatic potential in the channel as a function of position.

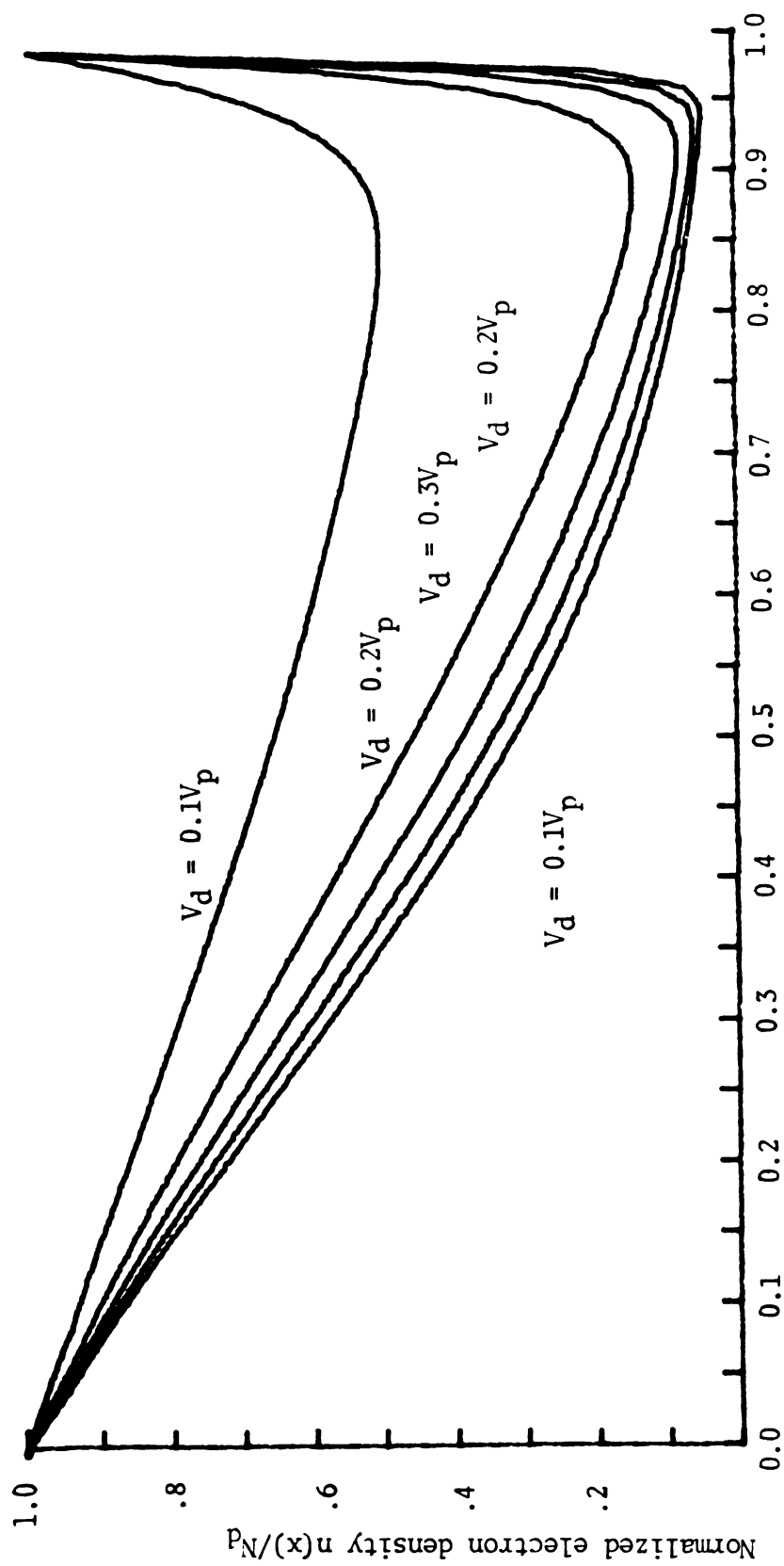


Fig. 4.3. Electron density in the center on the channel as a function of position; Structure I.

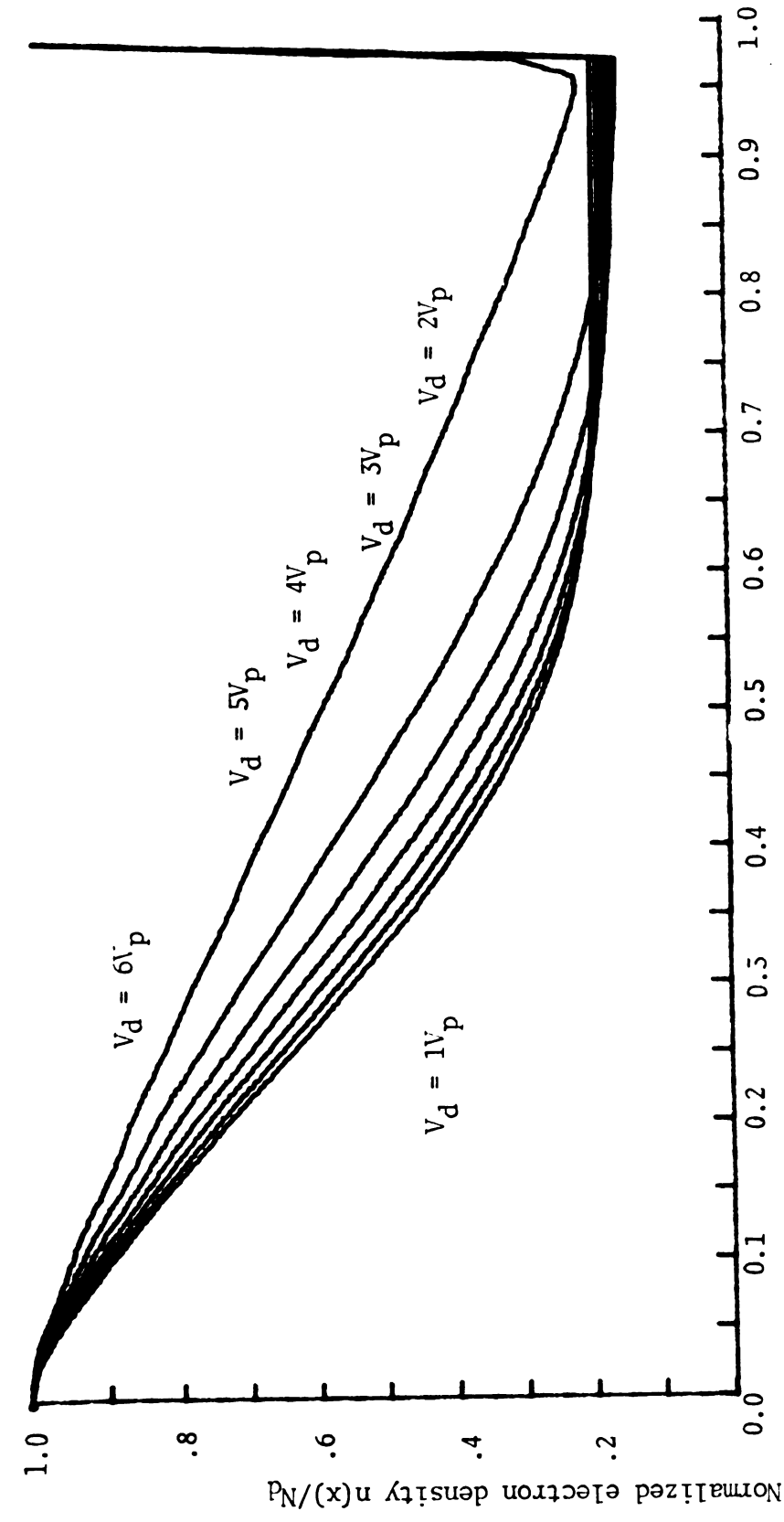


Fig. 4.4. Structure I; Electron density in the center of channel as a function position.

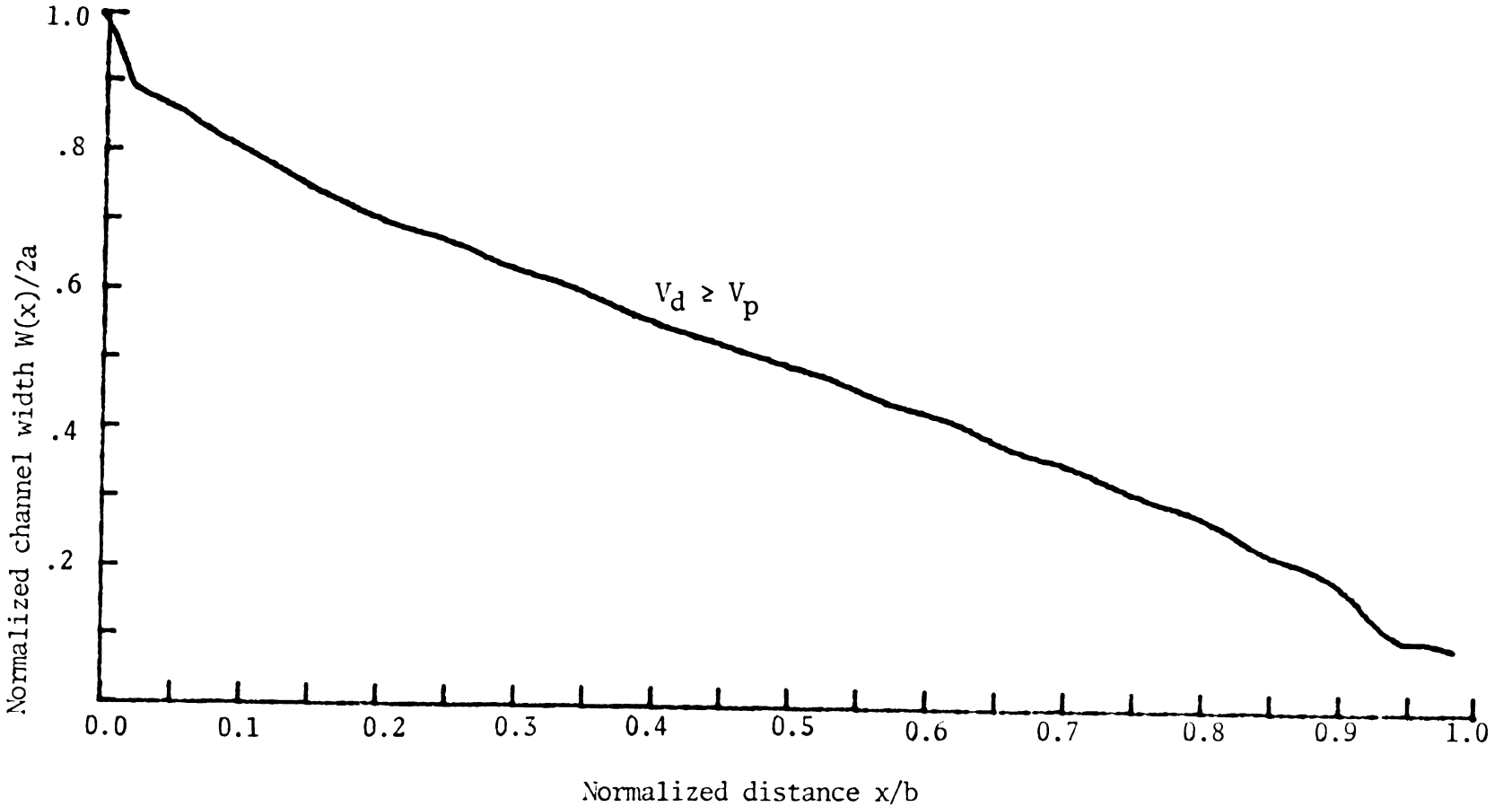


Fig. 4.5. Structure I; Channel width as a function of position.

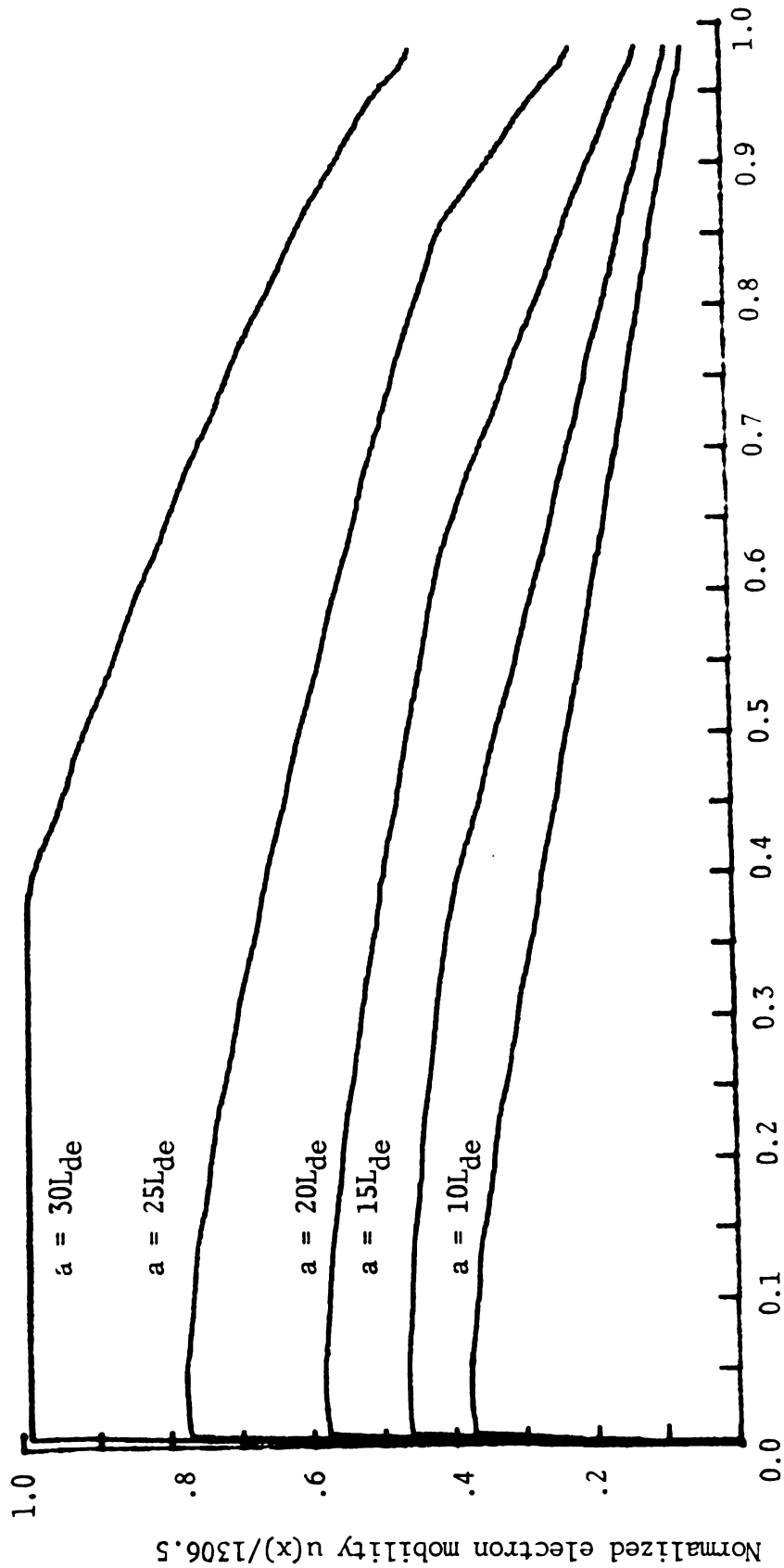


Fig. 4.6. Electron mobility as a function of position.

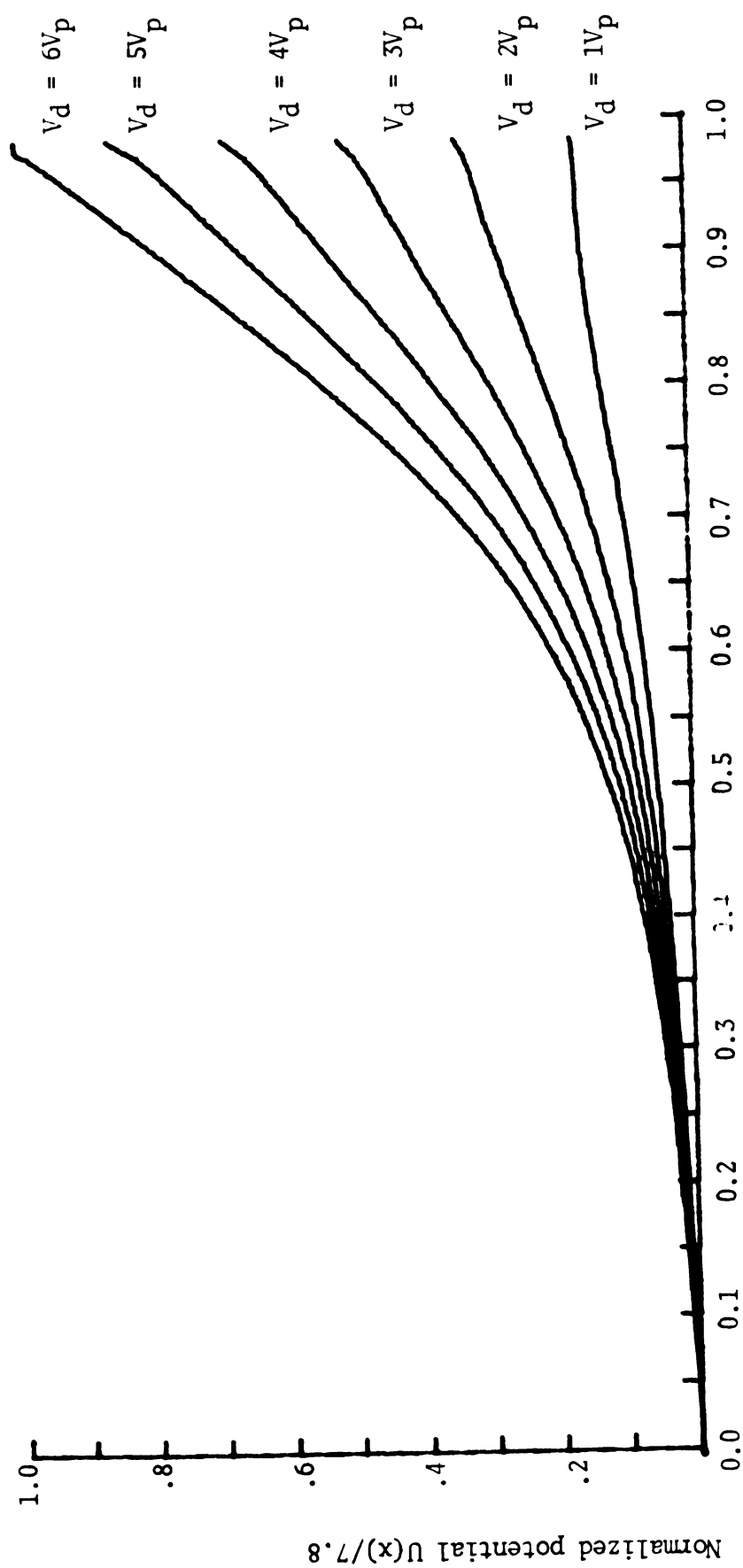


Fig. 4.7. Structure III; Normalized electrostatic potential in the channel as a function of position.

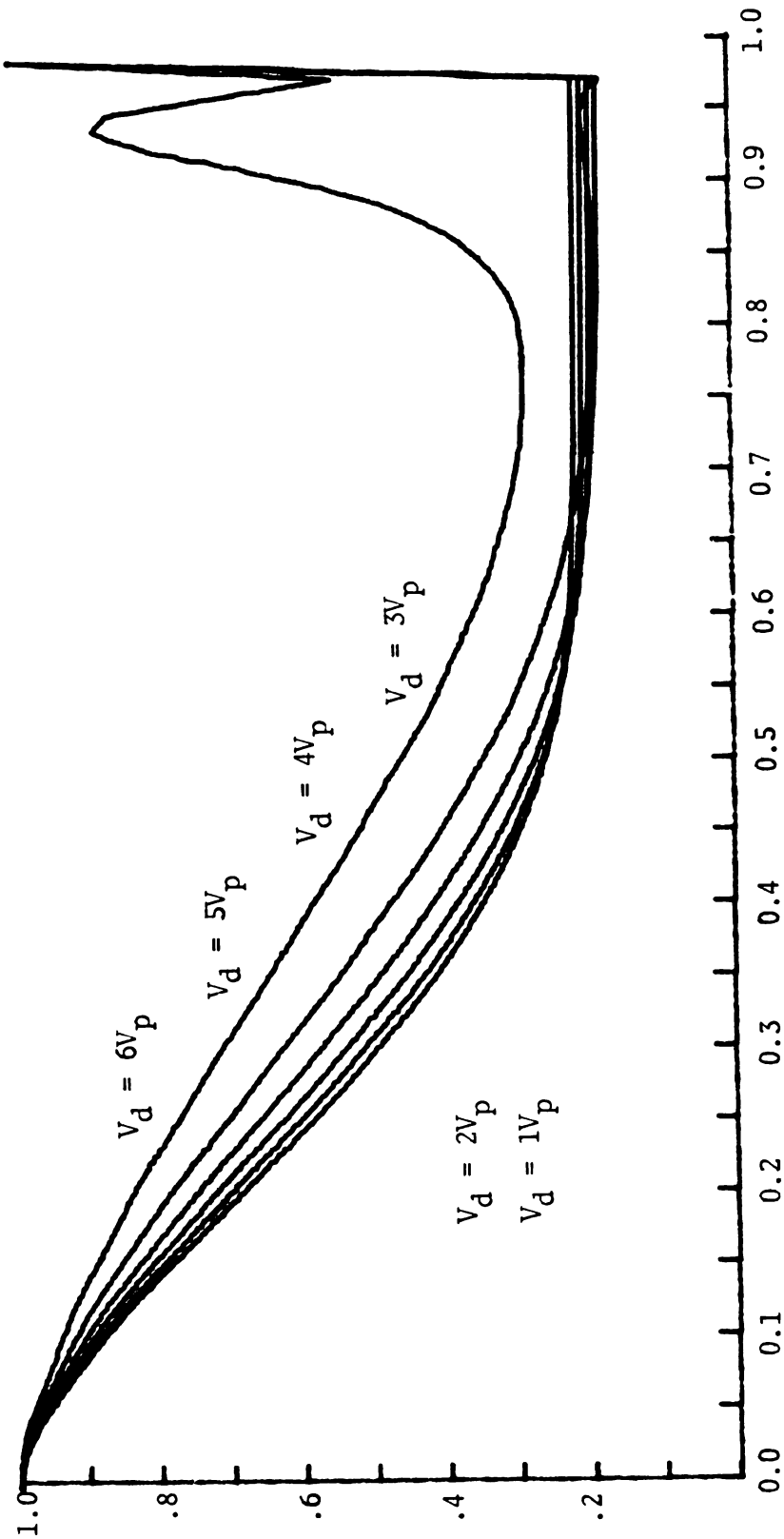


Fig. 4.8. Structure III; Electron density in the center on channel as a function position.

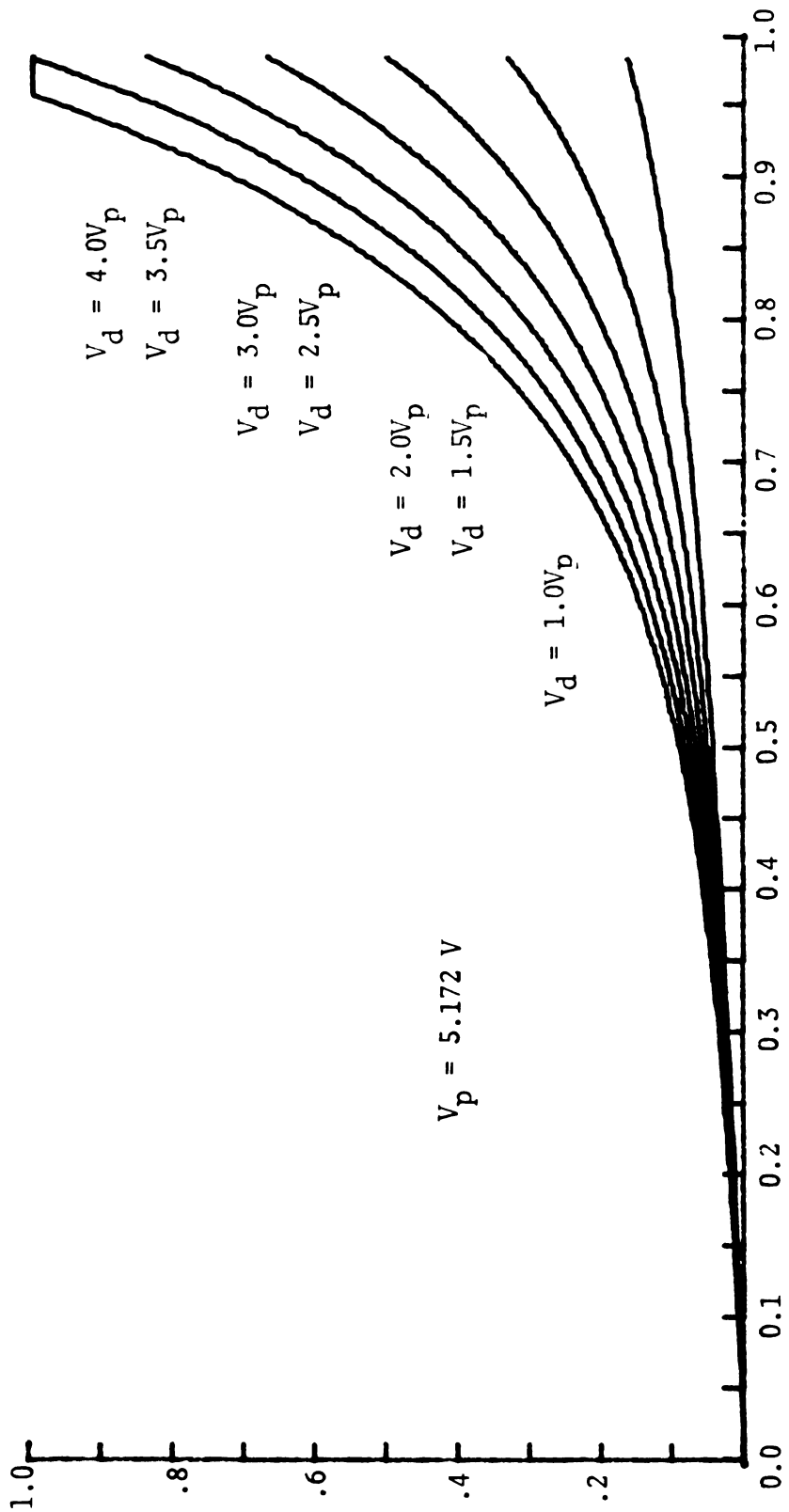


Fig. 4.9. Structure II; Electrostatic potential in the center of channel as a function of position.

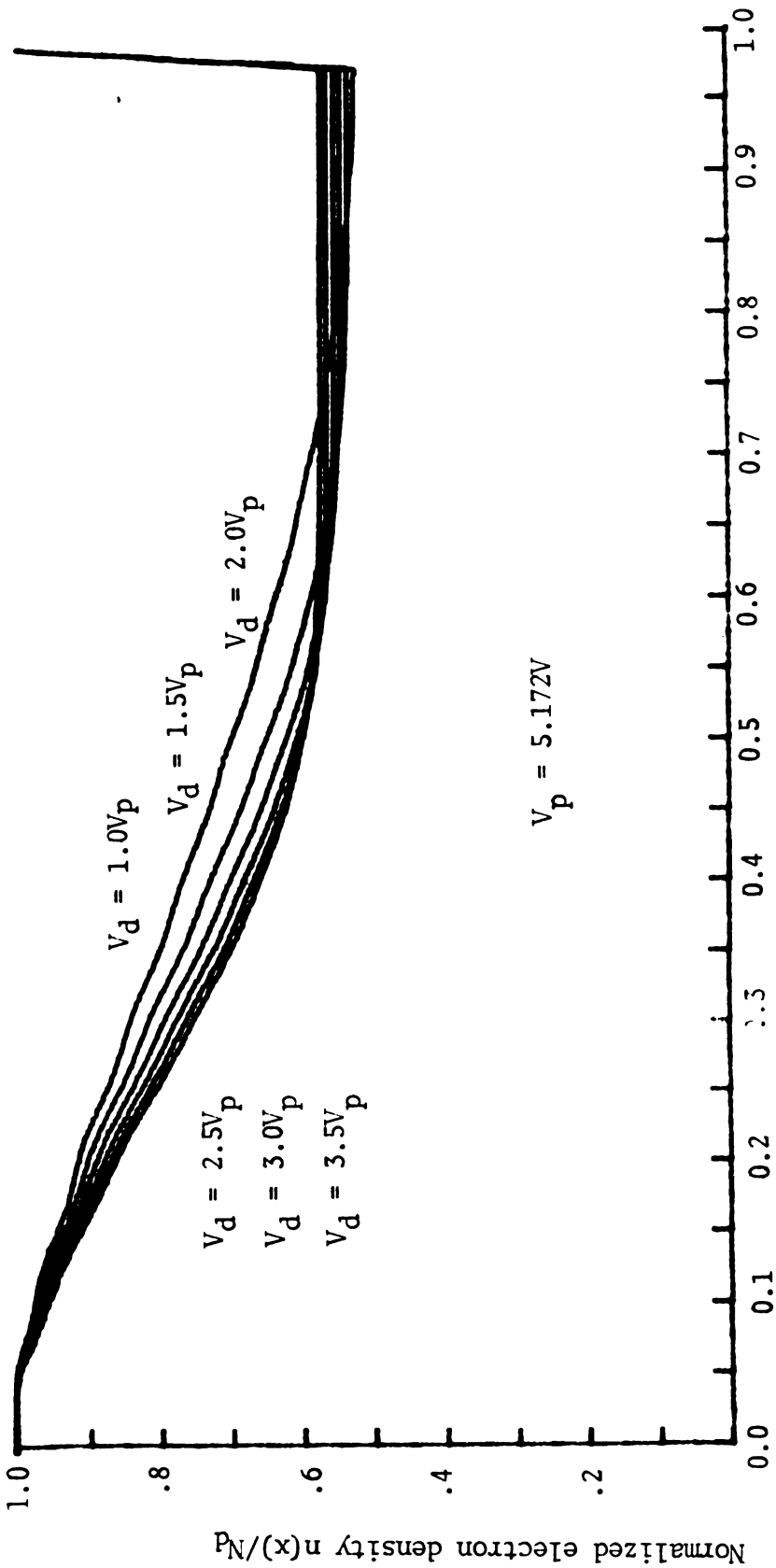


Fig. 4.10. Structure II: Electron density in the center of channel as a function of position.

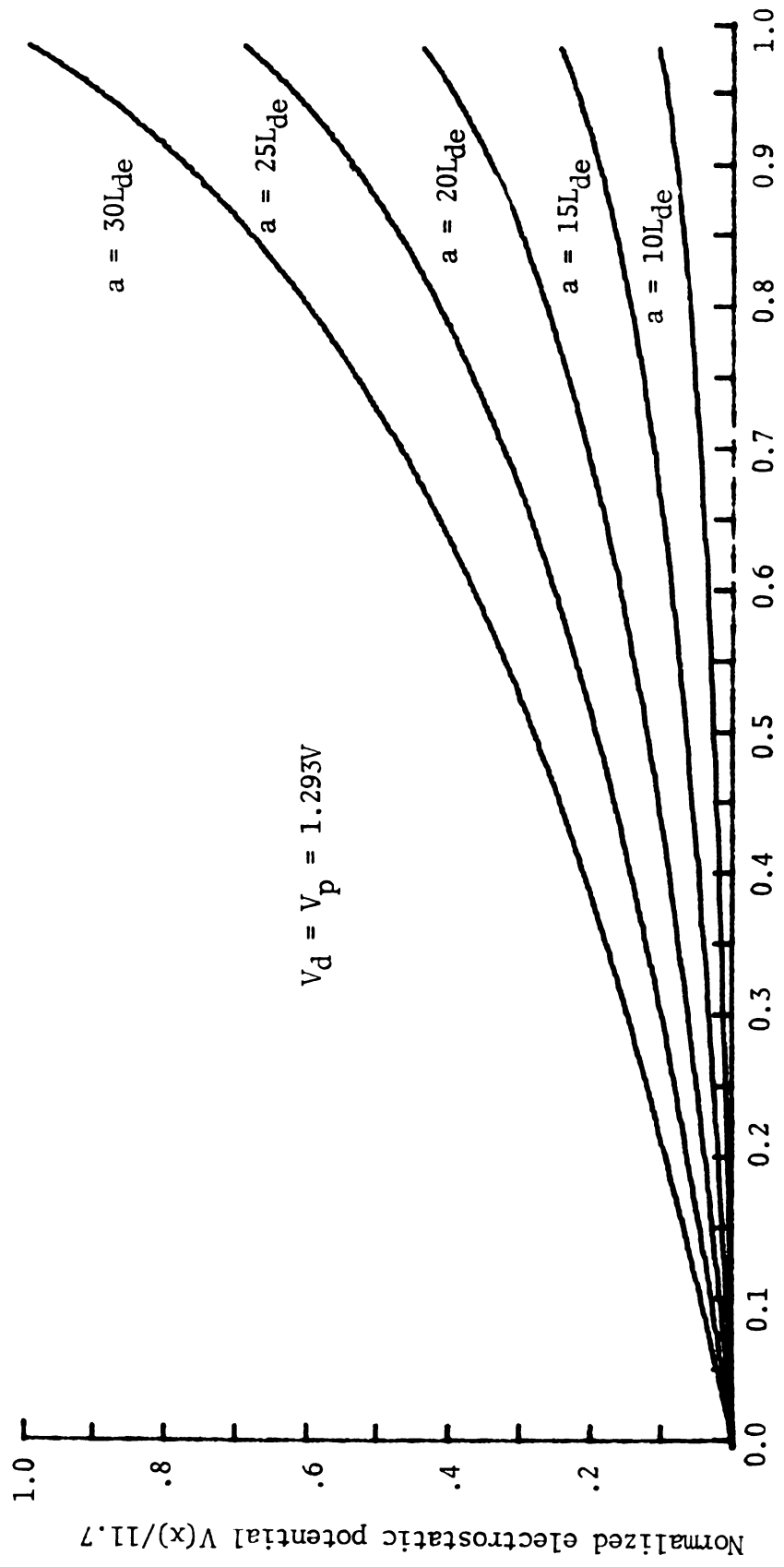


Fig. 4.11. Effect of different initial channel widths on the potential drop in the channel.

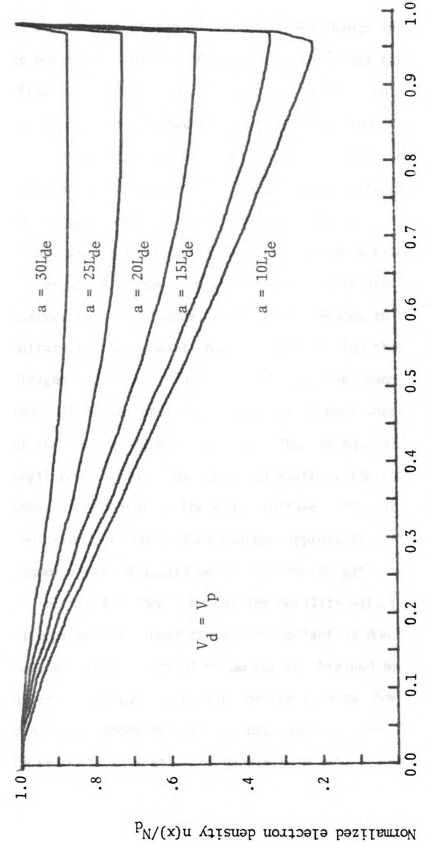


Fig. 4.12. Effect of different initial channel widths on the electron distribution in the channel.

density minima, it can be seen that any change in drain voltage or the position of pinch-off point does not alter the magnitude of diffusion current by any significant amount. This is precisely the property of a forward biased injecting junction. Near the source end of the channel, the current is predominently of the diffusion type. However, at higher drain voltages the drain current is completely of drift type near the drain contact. Again the channel is never completely depleted of the mobile carriers.

Figure 4.5 shows the channel shape with drain voltage. One observes that the channel width never reduces to zero; this is contrary to the gradual channel approximation theory. For low voltages the current control is through the channel width modulation. At higher drain voltages, the channel shape remains unchanged but the carrier density reduces. This is equivalent to channel length modulation. The shape and width of the channel drain end is almost independent of the drain voltage. This is different from the predictions of the gradual channel approximation theory whereby the channel width is always determined by the gate field.

Figure 4.6 shows the carrier mobility with position (the zero value of mobility near the source contact is due to an error in the computer program; actual value can be obtained by extrapolating the curves). For the calculation of the results shown in Figures 4.1 to 4.12 the above effects are not taken into account. Therefore, the velocity saturation of carriers is not a factor in the saturation of drain current.

Figure 4.13 shows the drain current variation with drain voltage. The method of analysis confirms the predictions of the gradual channel approximation theory below the pinch-off point. For $V_d > V_p$ non-zero conductance is self-evident; also, the conductance is larger than that predicted by the earlier models considered and is more near the values observed for the practical transistors. The near linear variation of drain current, with drain voltage, is indicated by the denominator of Equation (32), chapter 3. This factor is only influenced by the potential variation near the source; the contribution of the field near the drain contact being insignificant.

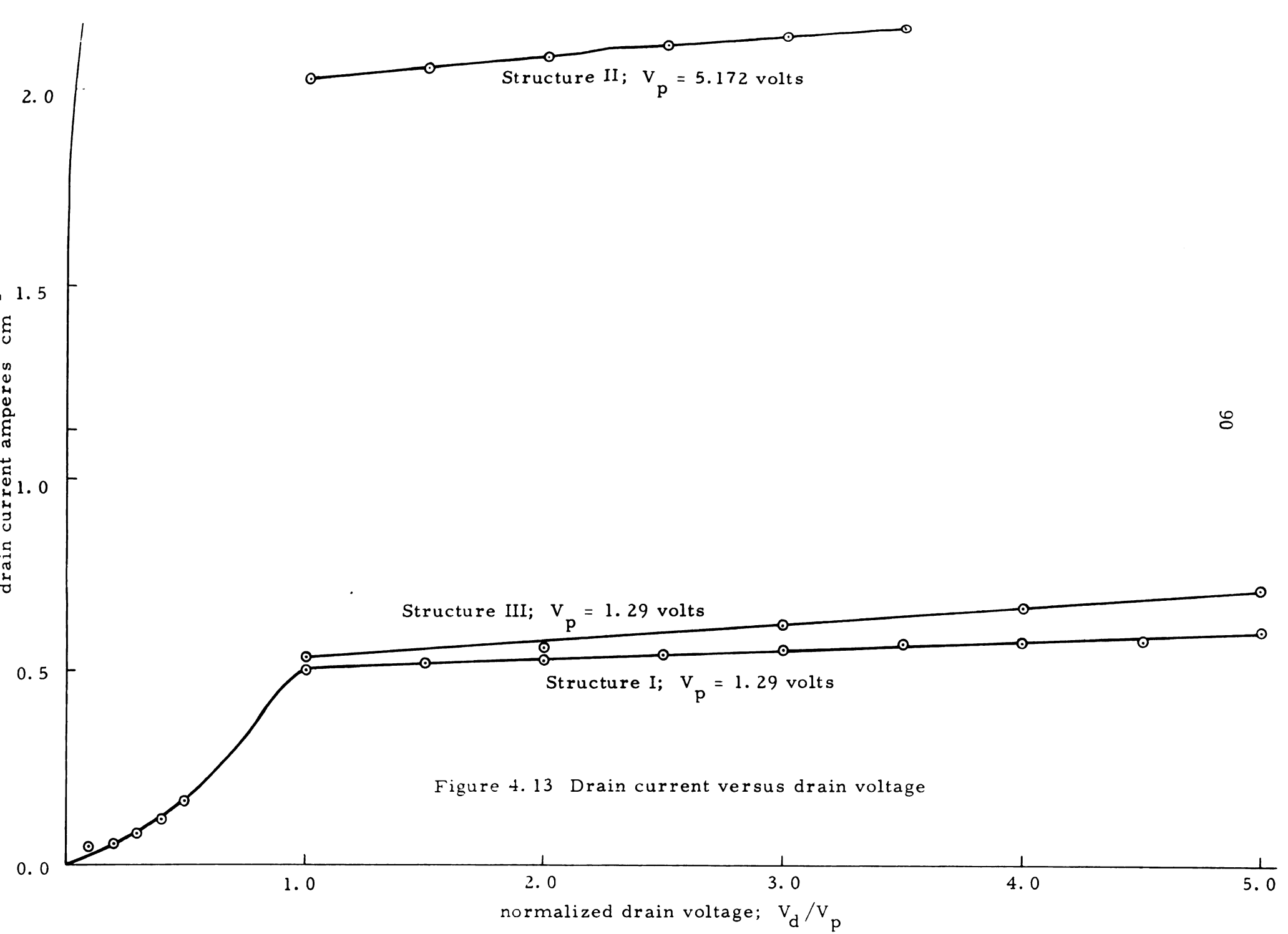


Figure 4.13 Drain current versus drain voltage

4.2 Advantages of Present Theory

The attempts at explaining the saturation current in FET's [1-12] centered around the classical model of the gradual channel approximation. This approximation, as explained earlier, is very satisfactory for $V_d<V_p$ but fails in the saturation region. Moreover, the precondition for this approximation to hold, in a long device ($b/a>>10$), is seldom met in practice.

The major drawback in this approximation is in the fact that the space charge effects of the channel current and drain voltage are ignored. The "feedback" mechanism present due to this space charge controls the channel width (reduction of current reduces the voltage drop; hence, the bias on the gate junctions is lowered).

In this analysis the current saturation is shown to be due to physical phenomena--space charge and applied accelerating fields rather than the geometry of the device. No voltage component in the channel is ignored. This is made possible by the solution of the two-dimensional Poisson's equation.

The numerical method adopted here has the advantage of a large saving in the storage space required in the computer and hence the computation cost; the storage space requirement is only one-fourth of that needed for the relaxation techniques. The method is particularly suitable for small computers which are handicapped due to the memory space.

4.3 Disadvantages of Present Theory

The present method consists of the analytical solution of the Poisson's equation for the applied voltages; this is convenient only for simple geometry. For more complicated geometry and boundary conditions the solution is very involved and a large number of additional calculations is required for the construction of the voltage function.

The solution of the transport equation, for the carrier density, in the form used here, requires the use of very large and very small numbers. This problem is especially critical for $V_d > 2V_p$. The Fourier's series is not suitable for constructing the step-type drain voltage boundary; an infinite number of terms is needed to do this near the gate end of the channel. Use of truncated Fourier's series results in the superimposed ripples on the voltage distribution.

The channel width W(x) does not appear as a by-product of the solution but its judicious initial selection is essential for the faster progress of the iteration.

Saving in the storage space is at the cost of increased computation time. Also, the large number of mathematical functions needed is a drawback. However, by clever programming these functions need be called only once.

CHAPTER 5

SUMMARY AND CONCLUSIONS

A research program was undertaken with the objective of developing a more accurate model to explain current saturation in field-effect transistors. In particular, we wished to uncover the principal phenomena responsible for current saturation in field-effect transistors. Also, we wanted to develop a more exact model for the mechanism which tends to maintain the drain current at a mean constant value with drain voltage as well as the mechanism responsible for the non-zero slope of the drain-current versus drain-voltage characteristic.

The field-effect transistor selected for analysis was schematically represented by two abrupt p-n junctions placed symmetrically with respect to the center of the channel. In order to simplify the mathematical formulation, the gate contacts were taken to overlap the source contact, and the gate and channel were assumed to be uniformly doped.

Numerical solutions to Poisson's equation were obtained subject to certain restraints (See Sections 3.3-3.5) and the results were analyzed. The major conclusions drawn from the analysis are:

1. The partial depletion of the channel (uniformly distributed impurity density) and the consequent spatial gradient of the majority current carriers is responsible for the current saturation. This is in striking contrast to the models of Kennedy [11] and Kim and Yang [16]. In their models the property of spatial distribution of the carriers was deliberately introduced by selecting special impurity density profiles in the channel.

2. Dependence of carrier mobility on the electrostatic field does not seem to play any significant part in the saturation of current. All the results presented in Section 4.1 have been obtained under the assumption that the carrier mobility is independent of the electric field. No accumulation of carriers has been observed in the channel and the electric field increases continuously from the source towards the drain.
3. The channel cannot be regarded as neutral even for voltages less than the pinch-off value. With increasing drain voltage, the high-low junction near the drain electrode remains more or less fixed in position [Figures 4.3, 4.4 and 4.8]. The position of second high-low junction is a function of drain voltage and drain current. The slight increase in drain current, with increasing drain voltage, is due to the increase of diffusion gradient across this "junction" [Figures 4.4 and 4.8]. The movement of the carrier density minima with the increase of drain voltage, in the partially depleted region, towards the source is clearly noticed in these figures.
4. Near the source contact the channel shape resembles the shape predicted by the gradual channel approximation theory. However, near the drain contact the channel width never reduces to zero and reaches a minimum value of the order of 2 Debye lengths. For narrow channels and voltages greater than the pinch-off value the channel shape is invarient with the drain voltage.

APPENDIX

HIGH-LOW JUNCTIONS IN SEMICONDUCTORS

High-low junctions arise due to a discontinuity in the impurity concentration in a semiconductor. Figure A1 shows a junction between a heavily doped material n^+ and a lightly doped material n. The difference in concentration across the x=0 plane sets up a carrier concentration gradient. The electrons diffuse into the n-region causing an accumulation of electrons on the right side of the x=0 plane. Equilibrium is established when the accumulated charges are balanced by the fixed positive charges of the impurity atoms.

An accumulation layer adjacent to a positive space charge gives rise to an electric double layer. This layer impedes the flow of current through it and is thus equivalent to a junction. Such layers can arise in devices which have n^+ type contacts. Contacts obtained by diffusing similar type impurity into a substrate are examples of this behavior.

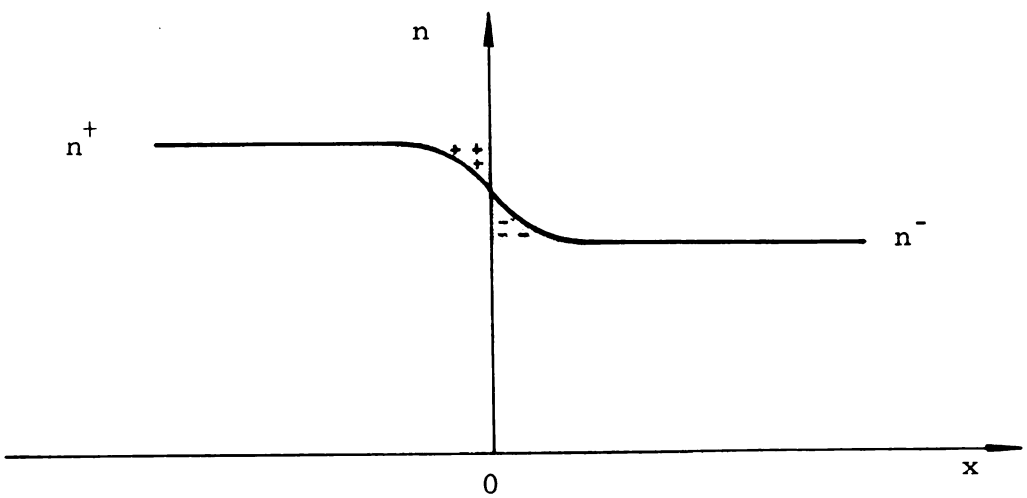


Figure A. Electron concentration in a high-low junction.

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