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HIGH-PERFORMANCE DATA ACQUISITION
FOR REAL-TIME TURBULENCE MEASUREMENTS

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HIGH-PERFORMANCE DATA ACQUISITION FOR REAL-TIME TURBULENCE MEASUREMENTS

By

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ABSTRACT

HIGH-PERFORMANCE DATA ACQUISITION FOR REAL-TIME TURBULENCE MEASUREMENTS

By

Pierre Georges Meyer

A high-performance, computer-controlled, data acquisition system has been designed, constructed and tested. This system, which is based on an LSI-11 microcomputer, collects voltage information from up to sixteen hot-wire anemometers located in the cross-section of a wind tunnel. These voltages are later converted to velocities. For ample flexibility, the acquisition unit provides a wide range of sampling rates for any number of channels and offers the advantage of user-definable random channel selection. Moreover, calibration circuits, accessible from the front panel, allow the operator to perform simple tests and make parameter adjustments for any selected channel. Typical sampling rates between 250 Hz and 10 kHz/channel for eight channels are achieved. And variable gains between two and two hundred are provided to amplify input signals to as large as $\pm$ 2.5 V before converting them into 12-bit digital data words by means of ultra-high-speed A/D converter.

To my fiancēe Midori Shibayama (柴山 みどり) for

her thoughtfulness and love

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CHAPTER I

INTRODUCTION

The study of turbulent and unsteady flows in wind tunnels has become an important aspect of modern applied research in fluid mechanics (1,2). Randomly occurring coherent motions within such flows are being investigated in order to uncover their physical properties. To examine such three-dimensional flow features, detailed quantitative information about the streamwise and normal velocity fluctuations is required. Hot-wire anemometry is a technique commonly used for this purpose (3). This research effort deals with the design, construction and evaluation of a data acquisition system that is used to sample, digitize, and store real-time turbulence data derived from an array of anemometers placed in a flow field. This instrument offers a wide range of sampling rates to accomodate an equivalently large series of signal frequency ranges. It collects data from up to sixteen anemometers, since such a number is required to perform measurements with satisfactory spatial resolution. In the long range, the unit is intended to connect to a computer system with powerful storage facilities-- high-density memory or disc. This operation will permit long data streams to be taken. Such streams facilitate the detection of an increased number of coherent motions during a single acquisition experiment. Eventually, the data acquisition system will also command the shutter-release of a camera to combine the hot-wire anemonetry measurements with simultaneous flow visualization in order to obtain a pictural description of the phenomena under

investigation.

This thesis presents a complete study of the data acquisition system in question. Chapter 2 delineates the basic requirements for the features to be incorporated in the design. Chapter 3 examines the analog-to-digital conversion chain and its associated calibration circuits. The hardware organization of the microcontroller and the utility logic is treated in Chapter 4. Finally, Chapter 5 summarizes the development phases, including testing and evaluation of the overall system.

CHAPTER II

REQUIREMENTS AND DESIGN ALTERNATIVES

This chapter establishes the requirements of the data acquisition system and presents the various alternatives. The first section, Section 2.1, introduces the data acquisition unit and its interrelation with its environment and closely examines its different requirements. Section 2.2 illustrates the design alternatives with their respective advantages and disadvantages. Finally, the last section, Section 2.3, defines a precise model for the desired data acquisition system.

2.1 System Requirements

2.1.1 General System Description

Figure 2.1 gives the block diagram of the overall system in which the data acquisition unit is incorporated. The data acquisition system collects analog information from the transducer and signal conditioning unit. This unit comprises a given number of transducers - anemometers - that deliver the signals to be processed by the data acquisition system. Each transducer generates a signal proportional to the physical variations in the resistance of its probe (4); such variations are induced by equivalent variations of the flow of gas in the wind tunnel. The data acquisition unit then converts the signals from the different anemometers into a digital code that is consecutively sent to the microcomputer through appropriate interface devices. The system uses an LSI-11 (5). This

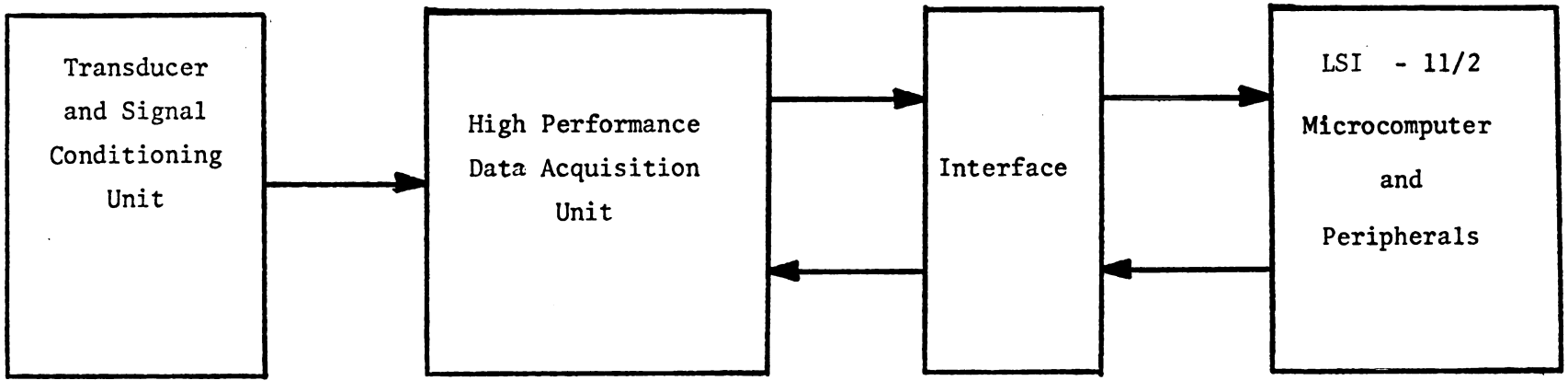


Figure 2.1 Block diagram of the overall measurement system

microcomputer performs the following tasks: initialize the data acquisition unit, start the acquisition process, store the converted data temporarily in main memory, transfer blocks of data to disc, execute diagnostic tests, and, finally, retrieve the information from disc for further processing.

This study focuses on the data acquisition unit. Nevertheless, it is essential to understand the characteristics of the computer and its interface as well as those of the transducer and signal conditioning unit to meet the front and rear-end compatibility criteria; so, these factors, too, will often have to be referred to in later sections and chapters.

2.1.2. Major Requirements

The overall system requirements constitute the cornerstone for this study and may be subdivided into two areas: analog and digital.

2.1.2.1. Analog

For the analog circuitry the requirements may be enumerated as follows. First, the unit has to process signals through eight different channels, a number which should be expandable to sixteen, with channel inputs fully compatible with the transducer outputs. The second requirement regards the conditioning of the anemometer output signals. The signals delivered by the transducers have a dc offset of a few volts on which an ac component of a few tens-of-millivolts is superimposed (see Figure 2.2). Both components are important for the turbulence studies (2). The dc component corresponds to the average velocity of the fluid flow as seen by the transducer. A feature

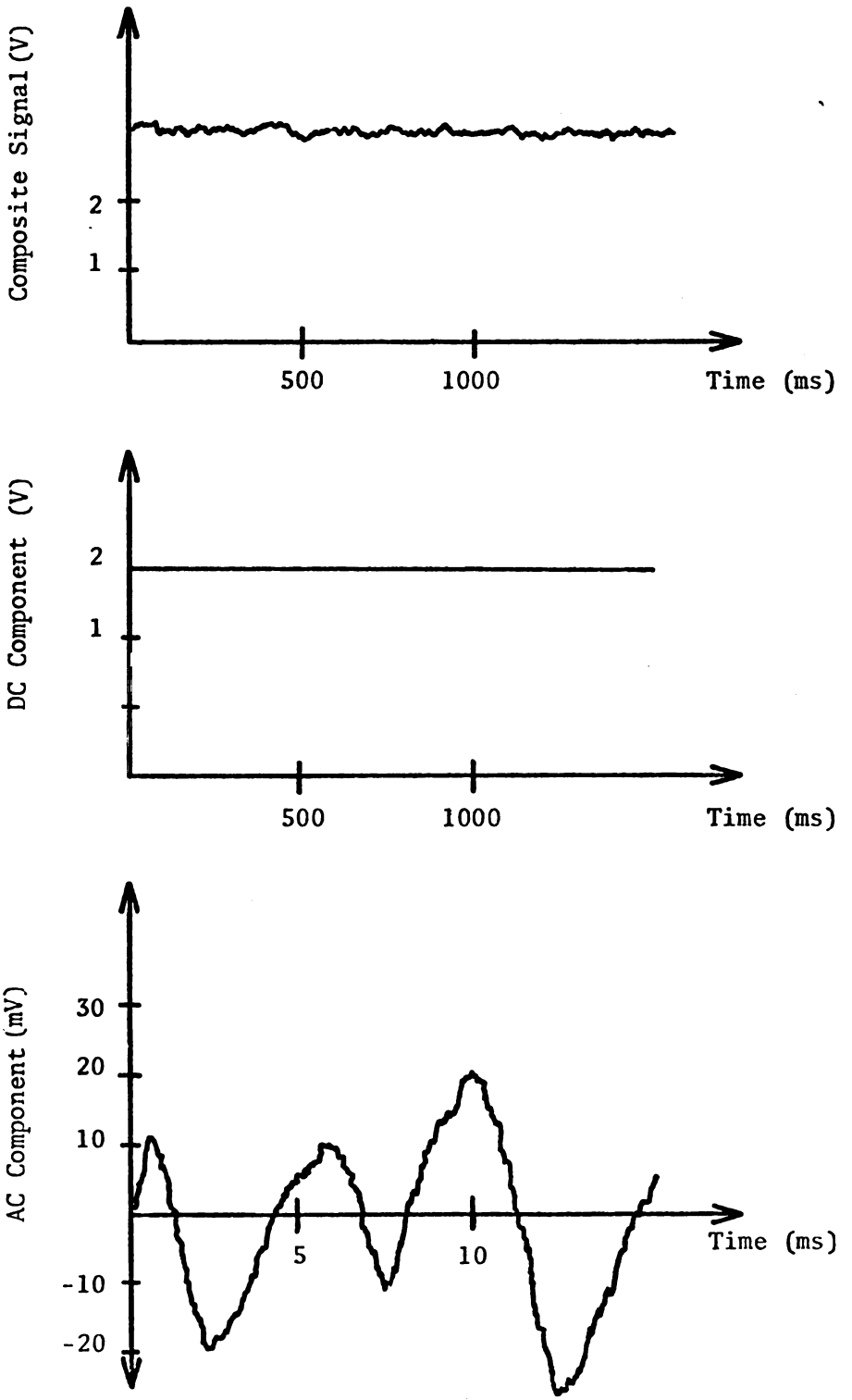


Figure 2.2 Typical anemometer output signal

in the calibration circuit has to be implemented to evaluate its value. In addition, for optimal use of the resources, this dc component must be eliminated during the data acquisition process to save only the information corresponding to the ac component. And this ac component must be amplified by means of an instrumentation amplifier with variable gain. Gains of 2 to 200 must be available. As a third requirement, high stability -- $\pm$ 0.5 mV/min -- and minimization of the noise have to be given a high priority in the design and construction phases of the analog chain. Finally the calibration procedure and its features on the front panel must be made as simple and attractive as possible to the user. However, for this objective, a compromise will have to be found because simplicity for the user undoubtedly means complexity in the circuitry. But circuit complexity must be balanced with the need for timeliness in the completion of the design objectives.

2.1.2.2 Digital

Three main requirements must be considered with the digital circuitry. First, provisions must be made so that analog channels can be accessed either randomly or sequentially. In addition, all channels must be sampled simultaneously and their sampling rate must be made variable and definable under program control. Rates between 500 Hz/channel and 10 kHz/channel must be allowable for eight channels or less. The last requirement concerns the intrinsic characteristics of the A/D converter(s). Since the word length of the computer is sixteen bits, for optimal use of its storage space the word length of the A/D converter(s) should be at least twelve bits; the remaining

four bits must contain the analog channel address. And the choice of the A/D converter(s) must be dictated by such important criteria as accuracy, stability and linearity.

For both the analog and digital circuits, additional hardware must be provided for convenient diagnostic tests and easy trouble-shooting. But any increase in hardward renders the system less cost-effective and lengthens system development time. Fifteen-thousand dollars was budgeted for this data acquisition system, and six months were allocated to design, construct, and test it. Therefore, compromises were imperative for the final design.

Having defined all the general requirements, the different design alternatives can now be considered. And this is the purpose of the next section.

2.2 Design Alternatives

To fulfill the requirements delineated in the preceding section, trade-offs must be established between circuit complexity, convenience for the user, sampling speed and cost. These factors will be examined in the next subsections for the different design alternatives. These can be classified into two main categories depending on the type of conversion -- parallel or serial -- and the type of multiplexing -- analog or digital -- involved.

2.2.1. Parallel Conversion and Digital Multiplexing

Figure 2.3 illustrates the organization of a parallel conversion/digital multiplexing data acquisition system. The signals from all channels are sampled simultaneously and subsequently converted in

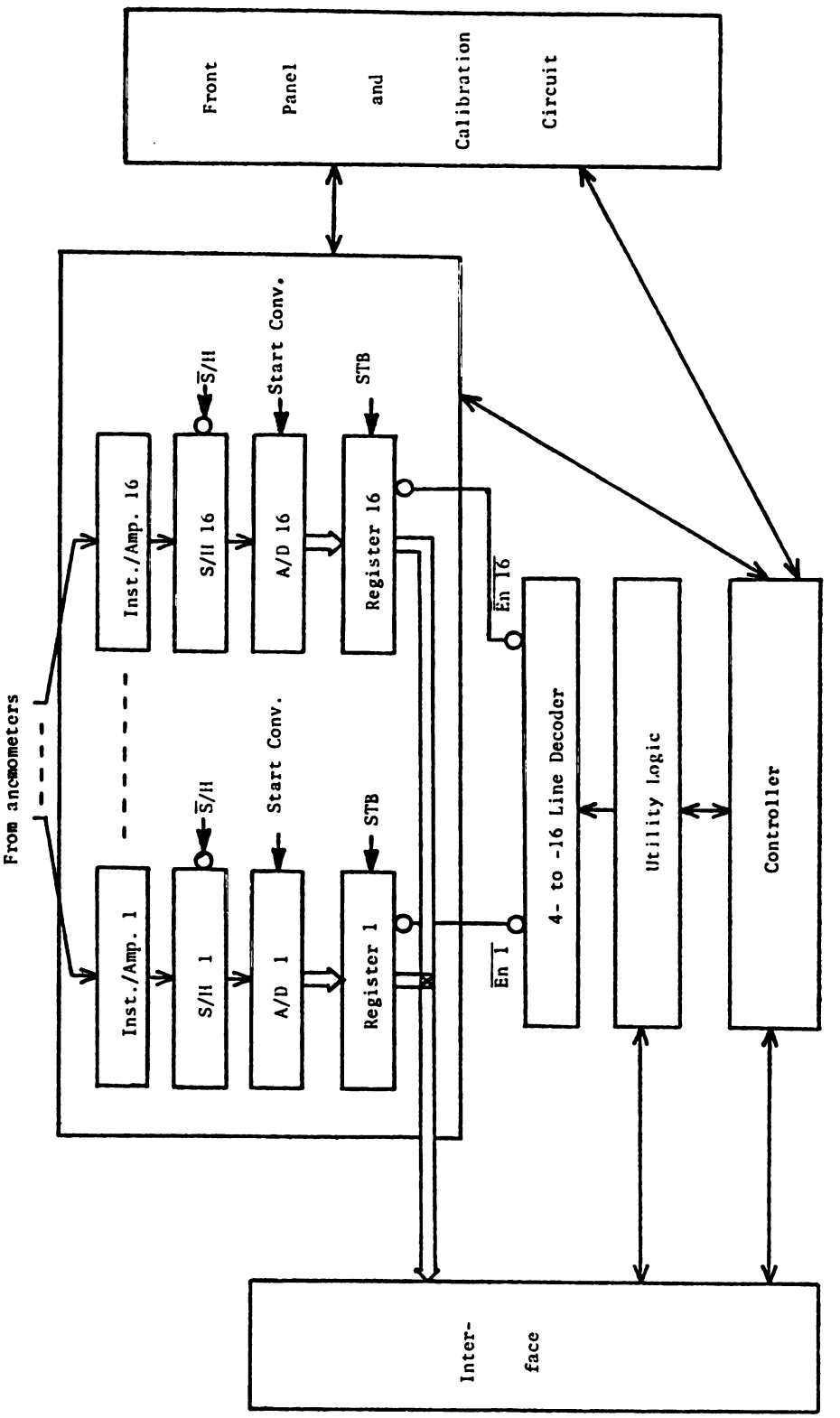


Figure 2.3 Block diagram of the parallel conversion/digital multiplexing alternative

parallel. The digital codes are then strobed into their corresponding registers. These registers have tri-state outputs and are enabled in sequence or randomwise. To drive the address lines of the 4-to-16 line decoder, the utility logic may include the following features:

A register loaded under program control selects the desired channel before reading in the information. With this method, any number of registers may be scanned and in any order, but at an important sacrifice in speed.

A 16 x 4 RAM, driven by a 4-bit binary counter, is pre-loaded with any sequence of analog-channels during an initialization cycle. This scheme allows the control logic to access the analog channels randomly by incrementing the RAM counter sixteen times. Such a method, however, may result in the acquisition of a significant amount of superfluous data if less than sixteen channels are desired. In other words, it may not procure an optimal use of the storage resources of the system.

A 4-bit binary counter addresses all sixteen registers directly and therefore in a fixed sequence. A gain in speed is achieved over the previous alternative but only sequential access is possible, and the problem of waste of memory space remains unaltered.

An improvement in speed and minimization of storage of useless information can be achieved by using a presettable counter instead. But this method still prohibits random access.

To keep the attractiveness of random channel selection along with high-speed achievement and a total elimination of wasteful code, a 16 x 5 RAM, driven by a counter, may be used. This

memory, when pre-loaded, contains only zeros in the fifth bit except for the last channel. The control logic examines the status of this bit to decide when to terminate the sequence. Also, identical performances may be achieved with a 16 x 4 RAM driven by a presettable counter.

These alternatives, except for the first one, are all suitable for very high acquisition rates. The drawback, however, lies in the cost. The A/D converters are the most expensive devices; therefore, their number should be minimized. The next subsection presents an alternative that takes this factor into account.

2.2.2 Analog Multiplexing and Serial Conversion

The block diagram of the typical circuit is given in Figure 2.4. In the case of analog multiplexing and serial conversion, again all channels are sampled simultaneously. Then, during the hold time, they are multiplexed and converted serially in a sequential or random order. All features, outlined in the preceding subsection for the utility logic, are still valid and their relative advantages and disadvantages remain the same. Nevertheless, in a global way, due to serial conversion, the performances in speed are drastically degraded. The trade-off, however, is an important upgrading in cost-effectiveness in comparison with the previous cost.

Using the general considerations discussed in this section, the next section describes a prototype of the final design.

2.3 General Description of the Prototype

The compromise between speed and cost, when weighted with the

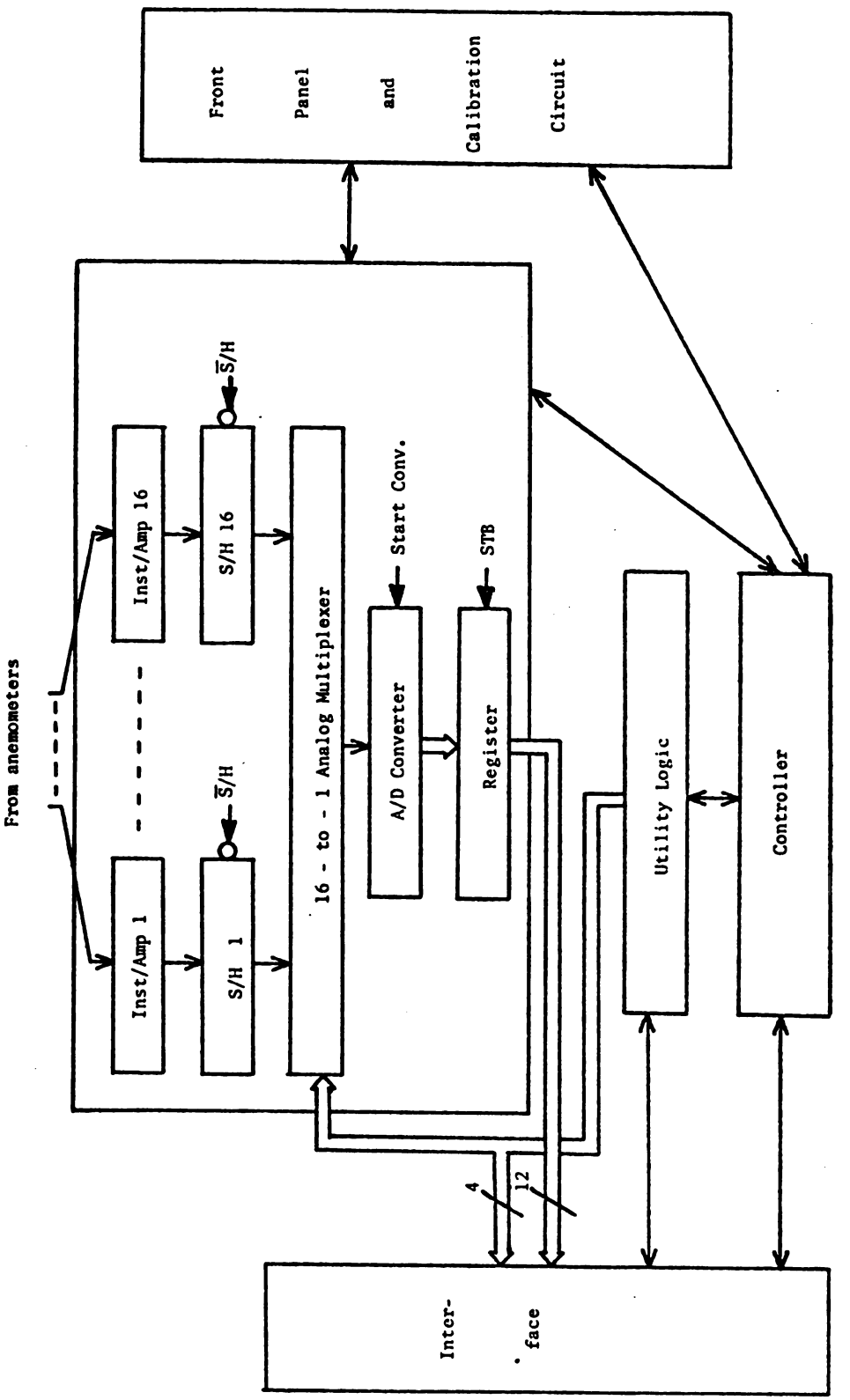


Figure 2.4 Block diagram of an analog multiplexing/serial conversion circuit

requirements, suggests the choice of an analog multiplexing and serial conversion type system. Due to the poor implicit speed performances of such a system, to achieve a 10 kHz/channel sampling rate, the following elements must be considered for speed enhancement. The sample-and-hold devices must be chosen so as to have a short acquisition time; the multiplexer a low settling time; and, finally, the A/D converter a very fast conversion rate. Moreover, the minicomputer must possess the capability of acquiring the digital data in the shortest time possible. Therefore, the unit must make use of direct memory access (DMA). Finally, the utility logic must include the following features. To implement a variable sampling rate, a delay counter combined with a delay register loaded under program control during initialization, will have to be introduced. After the successive conversions within each sampling period, the control logic may preset the counter to the value stored in the delay register and decrement it to zero. And, to keep the flexibility of random channel selection, the utility logic will also comprise a 16 x 5 RAM to contain the sequence of the channel addresses with an extra bit for the last channel indication.

Figure 2.5 gives the general timing diagram for the data acquisition process and illustrates the sequence of the various tasks of the unit. As shown, for optimal effectiveness the DMA cycle for a given channel overlaps with the conversion cycle of the next channel. The different tasks are controlled by a microcontroller which is enabled and disabled under program control. Chapter IV will fully describe this microcontroller as well as the utility logic and their associated diagnostic circuits.

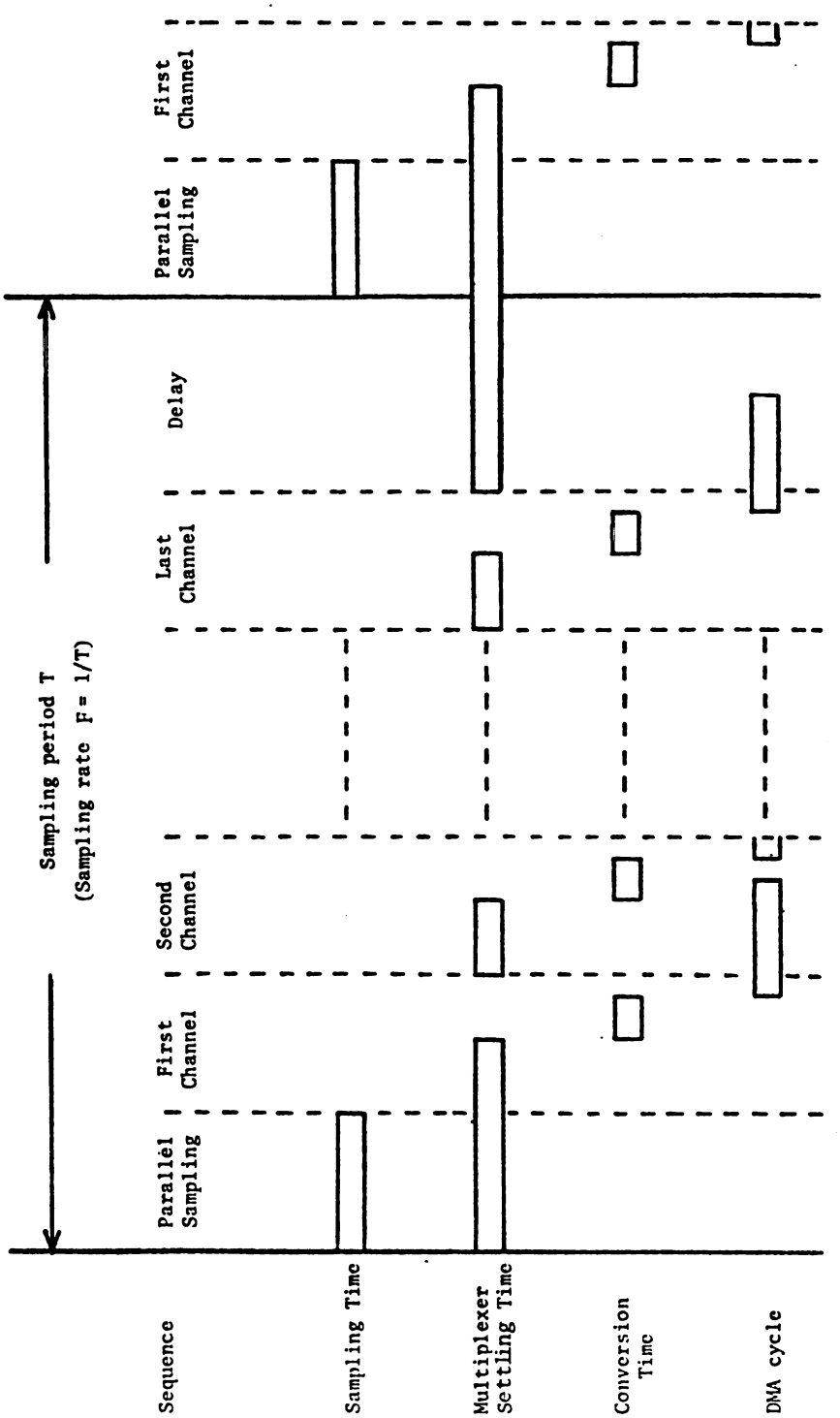


Figure 2.5 General timing diagram of the prototype design

CHAPTER III

ANALOG CONVERSION

The purpose of this chapter is to give a detailed presentation of the analog-to-digital conversion chain and the calibration features that it uses. Section 3.1 is an introductory paragraph describing the principal connections between the major building blocks. These blocks and their more elementary components are examined more thoroughly in the subsequent sections. Section 3.2 focuses on the amplification and conversion devices as well as the interface needed for data transfers to the computer. And Section 3.3 concludes the chapter by discussing the calibration and front panel circuits and by outlining the theory of the required single-channel chain calibration.

3.1 General Block Diagram of the Conversion Circuit

Figure 3.1 illustrates the organization of the conversion chain. The given block diagram primarily attempts to emphasize the data flow between all constituent parts. In this perspective, it shows that the outputs of the anemometers connect to the inputs of the instrumentation amplifiers via the front panel and calibration circuit. The outputs of the instrumentation amplifiers drive the inputs of the sample- and-hold devices through a similar path. For circuit simplicity, however, such a scheme has been abandoned for the link between the sample-and-hold devices and the multiplexer. Instead, direct connections are provided. But this restriction finds its compensation in a special calibration feature that allows these lines to be inspected, too, if desired. Any

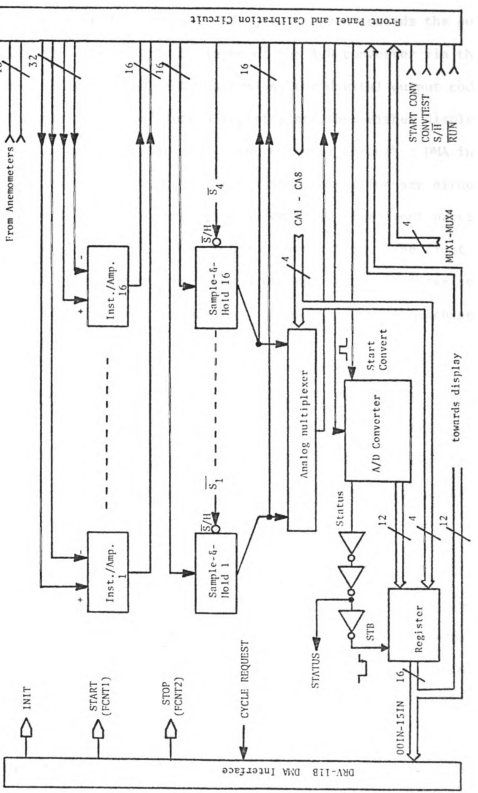


Figure 3.1 Conversion chain and associated circuits

of the multiplexer inputs, when selected by means of the four channel address lines --CA1, CA2, CA4, CA8--, is steered towards the output and consecutively connects to the input of the A/D converter via the calibration circuit. After each conversion, the digital output code of the A/D converter is strobed into a register and then either displayed on the front panel or transferred to the computer through a DMA interface. Sampling, channel selection, or conversion initiation are either performed manually or under microprogram control. The front panel and calibration circuit is used to control either mode. The front panel and calibration circuit are presented more completely in a later section. The other blocks of the overall conversion circuit are discussed in the next section.

3.2 Devices of the Conversion Chain and DMA Interface

This section is devoted to a brief review of the different elements of the conversion chain. Emphasis is placed on their major characteristics. The section finally concludes by treating the DMA interface and its properties.

3.2.1 Instrumentation Amplifiers

The system uses for all the channels the AM-201C instrumentation amplifier from Datel Systems, Inc. (7). This device provides the user with a variable voltage gain -- 1 to 1000 -- programmable by means of an externally adjustable resistor R_G. For high stability, this resistor must have a very low tempature coefficient. The gain is inversely proportional to the value of R_G and its equation is simply $G = 200\ K/R_G$. For internal offset adjustment, a good quality external trimming

potentiometer is required. Additional characteristics of the AM-201C are an excellent common-mode-rejection ratio (CMRR) -- 114dB --, a worst case input drift of -25 $\mu V/^{o}C$, a maximum gain nonlinearity of .01% and a 3 dB bandwidth of at least 45 kHz for all allowable gains. These properties make this component an excellent option for this type of application.

3.2.2 Sample-and-Hold Devices

Monolithic integrated circuit sample-and-hold devices SHM-IC-1 from Datel Systems have been chosen (7). Their selection was based on such important criteria like short aperture delay --50 ns-- and a low acquisition time. The circuit must include a good quality polystyrene type capacitor of .001 µF to achieve an acquisition time of 5 µs for a 10 V step up to .01% of its final value. The sample-and-hold devices are used in the unity gain noninverting configuration with an external trimming potentiometer for offset cancellation. For optimal operating conditions, their arrangement on the circuit board follows exactly the scheme of the manufacturer's proposed layout.

3.2.3 Multiplexer

The circuit makes use of a 16-channel MX-1606 single-ended CMOS multiplexer from the same company (7). It allows channel sampling rates of up to 200 kHz and a transfer accuracy of .01% over $\pm$ 10V signal swings. Very low source impedances -- under 1 kΩ -- and an extremely high load impedance -- above 100 MΩ -- are needed to achieve such an accuracy. The first requirement is undoubtedly met because the output impedance of the sample-and-hold devices is typically 0.2 Ω.

But for output compatibility with the low input resistance of the A/D converter -- typically 2 kΩ --, a unity gain buffer amplifier is inserted between the two stages. In this respect, a CA3140 operational amplifier from RCA is the right choice (8). Indeed, this device has a typical input resistance of 1.5 TΩ in addition to a very low offset and a high bandwidth.

3.2.4 Analog-to-Digital Converter

For ultra-high speed data conversion, the system makes use of a 4133-22 12-bit A/D converter from Teledyne Philbrick (9). This device has been selected because of the excellent performance/price compromise it offers. By means of the successive approximation technique, typical conversions are executed in 2.5 μs. Two conversion modes are available, unipolar or bipolar, but bipolar is imperative for this application. For this mode, an extra option is provided. Both offset binary or two's complement codes are offered but for easy data handling, the natural choice is two's complement because this is the number system representation used by the computer. The correspondence between the analog inputs and the digital outputs for this code is shown in Table 3.1. With regard to the transfer characteristics of the A/D converter, the typical nonlinearity, differential nonlinearity and quantizing errors are ±1 LSB, ±1/2 LSB and ±1/2 LSB, respectively. Finally, only two control/status lines are needed. A positive-going pulse with a duration from 35 ns up to 200 ns on the Start Convert line is required to initiate a conversion. And the high-to-low transition on the Status line can be utilized to strobe the output code into a register. This line may also be inspected by the microcontroller to check if the

TABLE 3.1

ANALOG-VOLTAGE/DIGITAL-CODE CORRESPONDENCE

Analog Input	Input (Volts)	Digital output (12 bits)
+FS	+ 5.0000	100...000
+FS - 1 LSB	+ 4.9976	100...001
+ 3/4 Scale	+ 3.7500	101...000
+ 1/2 Scale	+ 2.5000	110...000
0 + 1 LSB	+ 0.0024	111...111
0 +	0.0000	000...000
0 - 1 LSB	- 0.0024	000...001
- 1/2 Scale	- 2.5000	010...000
- 3/4 Scale	- 3.7500	011...000
- FS + 1 LSB	- 4.9976	011...111

FS = Full Scale

LSB = Least Significant Bit

conversion time remains within prescribed margins.

3.2.5 DMA Interface

The interface is a general pupose direct memory access DRV-11B interface from Digital Equipment Corp. (6). Transfer rates of up to 250 kwords (16 bits/word) are possible in single cycle mode. The interface contains five registers. These are a word count register -- WCR --, a bus address register -- BAR --, a control/status register -- CSR --, an input data buffer register and an output data buffer register. As suggested by their denominations, WCR contains the two's complement of the number of words to transfer and BAR the address to which an input transfer takes place or from which an output transfer originates. During normal operation, the contents of WCR and BAR are incremented after each transfer unless disabled by means of a dedicated bit in the control/status register. When WCR increments to zero, the processor automatically branches to an interrupt routine, provided that the interrupts have been previously enabled. Interrupts and DMA transfers are enabled under program control by setting special purpose bits in the CSR register. Once they are enabled, the user's device must assert specific control lines to define the desired transfer type -- word or byte, input or output. These lines may just be tied to fixed levels if, for a given interface peripheral, the transfer type is predefined and unique as it is the case for this system. The most important line required to initiate a DMA cycle is CYCLE REQUEST. This line must be conditioned by the microcontroller at appropriate times. As indicated in Figure 3.1, the system makes use of a few additional features offered by the DRV-11B interface board, namely, INIT, FCNT1,

FCNT2. These lines, asserted under program control, initialize the system, start the data acquisition process and terminate it, respectively.

3.3 Front Panel and Calibration Features

3.3.1 General Description

Figure 3.2 illustrates a detailed block diagram of the front panel and calibration circuit. The inputs and outputs of the devices from the sixteen channels connect to the measurement aparatus via the calibration switching circuit and a set of seventeen eight-pole double-throw interlocked switching modules -- SW1, SW2, .., SW17. Each switching module, except SW17, selects a given analog channel and directs its particular devices towards the calibration switching circuit. Interlocking provides mutually exclusive channel selection. The modules also connect the positive input terminals of the instrumentation amplifiers to variable DC voltages which will constantly be referred to as external offsets. These offsets are available from a series of potentiometers -- TR1, ..., TR16 -- fixed on the front panel and with terminals connected to a very stable voltage reference. Figure 3.2 depicts, as an example, the case in which channel #16 has been selected for calibration. Switching module #17 is not drawn. Its sole purpose is to lock out all other switches at the end of a specific channel inspection. It is important to note that this switch must remain depressed during multichannel data acquisition in order to keep the entire acquisition chain isolated from the calibration switching circuit. Subsection 3.3.2 presents a complete schematic of this switching circuit and analyses the corresponding calibration modes.

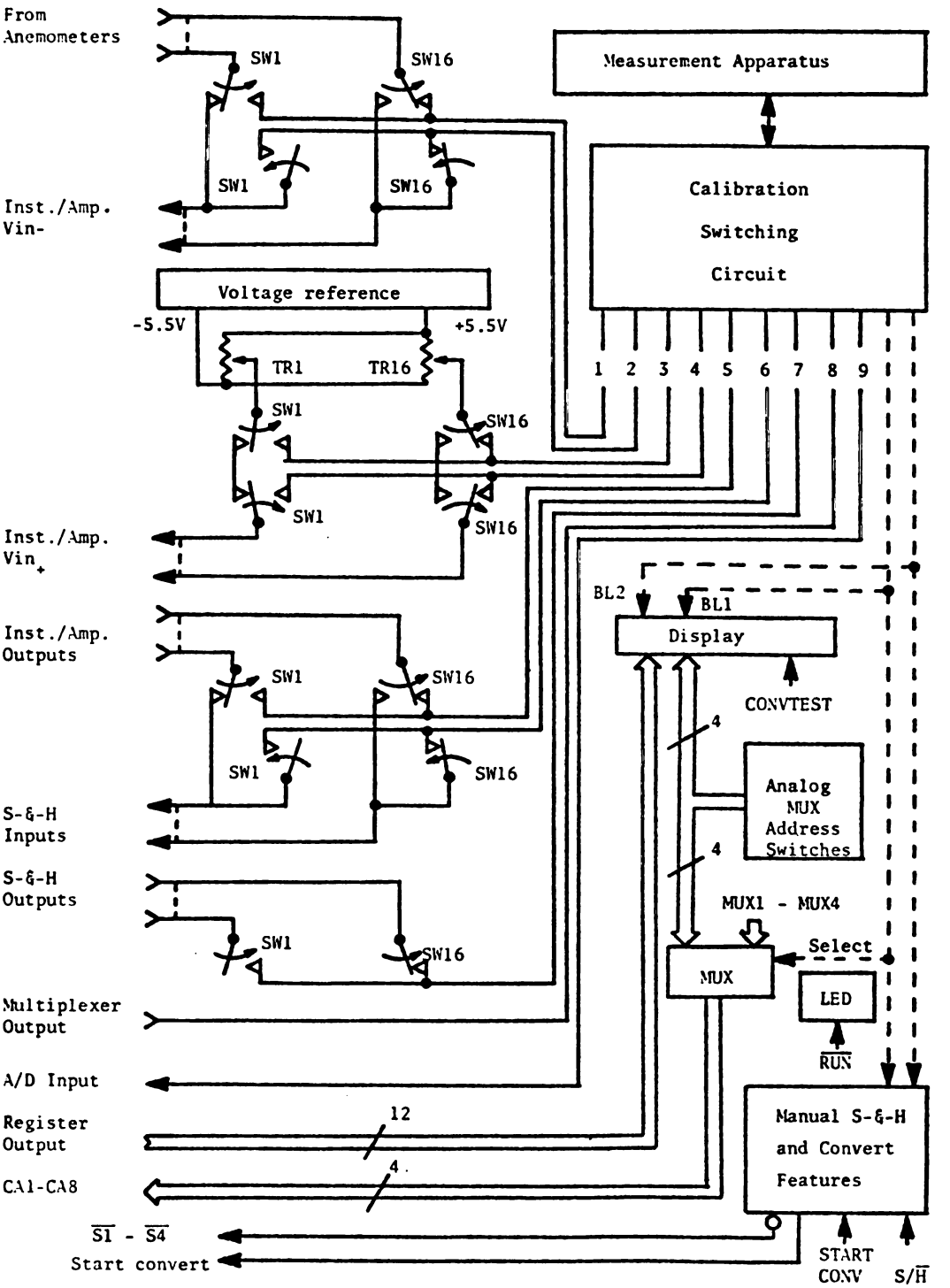


Figure 3.2 Front panel and calibration circuit

Besides the aforementioned features, the front panel includes dedicated circuits to select, for a specific application, either manual or microcontrolled sampling, conversion and multiplexer channel specification, as shown in Figure 3.2. In addition hexadecimal LED modules are provided to display, during manual operation, the selected multiplexer channel and the result of a conversion and to reveal a possible conversion error during the acquisition process. Finally, an extra LED on the front panel is used to inform the user when the microcontroller is in the RUN mode.

3.3.2 Operation Modes

Figure 3.3 gives a detailed sketch of the calibration switching circuit. Three arrangements of multi-pole double-throw interlocked switching modules can be distinguished. These are reproduced in Figure 3.4. The different operation modes are selected with the main switchrack. They can be classified as independent, test or calibration modes according to the grouping in Figure 3.4. The unique purpose of the external mode is to permit external AC or DC signals to be measured by means of the installed apparatus without having to disconnect it from the calibration circuit; and the non-calibration push-button is just used to lock-out all other switches. The test and calibration modes, exclusively, make use of the two extra switch sets. The AC/DC switchrack allows the gain adjustment of the instrumentation amplifier to be performed either by an AC source or a DC source. And the Input/Output set (V_{in-}/V_{in+}, respectively) is required to link with the desired measurement instrument either the input or the output (the V_{in-} or the V_{in+}, terminals, respectively) of the device being tested or calibrated (the instrumentation

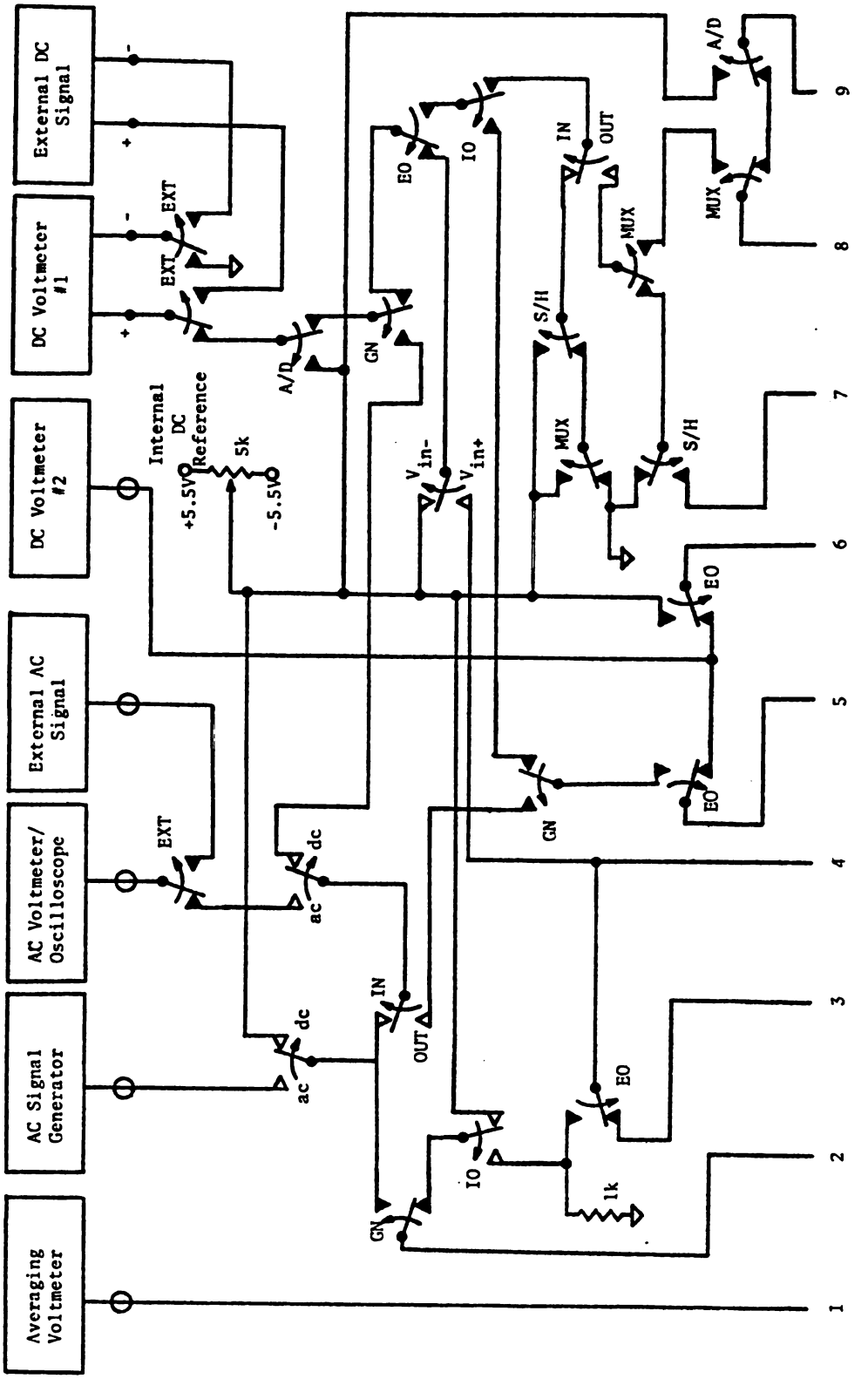
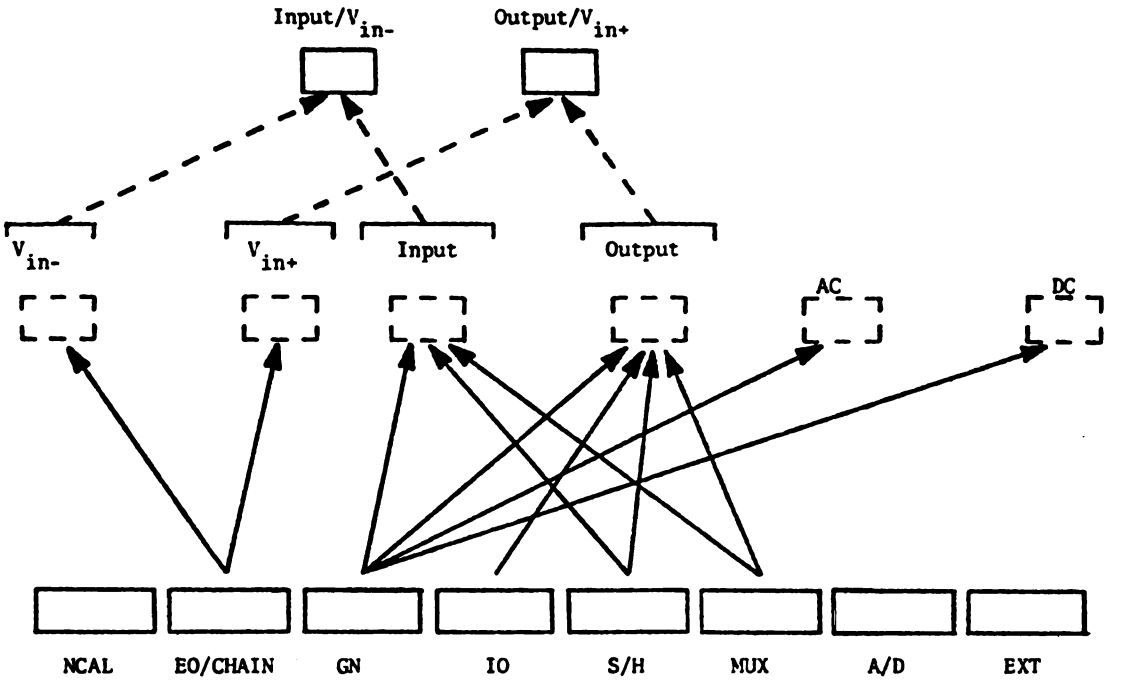


Figure 3.3 Calibration switching circuit and measurement apparatus



NCAL	=	Non-calibration mode	Independent
EXT	=	External measurement	
EO/CHAIN	=	External offset/chain calibration	Calibration
GN	=	Gain adjustment	
IO	=	Internal offset reduction	Test
S/H	=	Sample-and-hold test	
MUX	=	Multiplexer test	
A/D	=	A/D Converter test	

Figure 3.4 Calibration switching modules on front panel

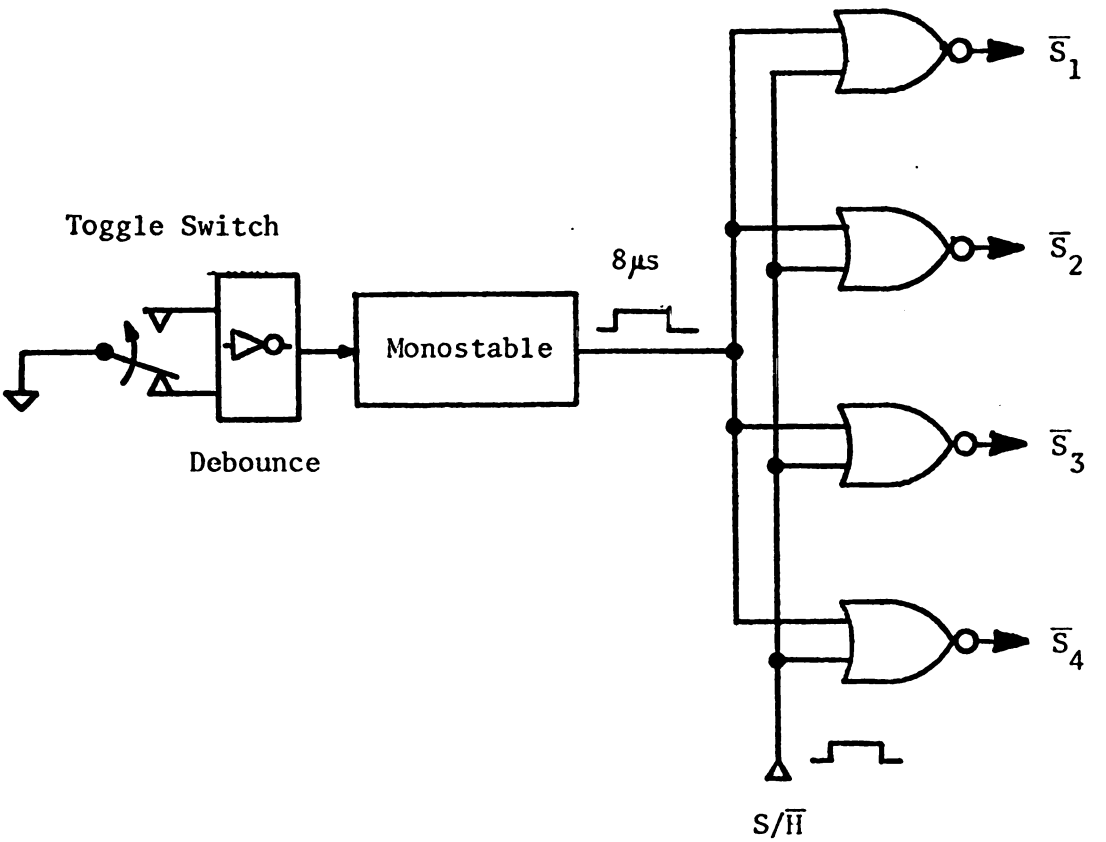
amplifier, respectively). The interdependence among the various switching modules is also illustrated in Figure 3.4, but the role of these switches finds a better explanation throughout the following subsections.

3.3.2.1 Test Modes

There are four test modes. During the internal offset mode -- IO --, both inputs of the selected instrumentation amplifier are connected to the analog ground. DC Voltmeter #1 is directly connected to its output so that it displays the actual internal offset. This offset can then be reduced by means of the associated trimming potentiometer on the amblifier board. When the S/H or MUX push-buttons are depressed, the input of the sample-and-hold device is automatically linked with the variable internal DC reference shown in Figure 3.3. The value of the corresponding voltage can be read on DC voltmeter #1 if the Input switch is set. When switching over to Output, either device presents its output to the same voltmeter, depending upon which mode has been selected. Both modes enable manual sampling and channel selection. To see if the device in question works properly, the sample-and-hold toggle switch, shown in Figure 3.5, must be activated and the value read from either output must coincide with the value previously measured for the input. Finally, for the A/D mode the internal DC reference is directly connected to DC Voltmeter #1 and to the input of the A/D converter. The conversion toggle switch, represented in Figure 3.5, is then used to start a conversion. The resulting code appears on the display and may be compared to a more detailed version of Table 3.1.

3.3.2.2 Calibration Modes

During gain calibration -- GN -- the positive input terminal of



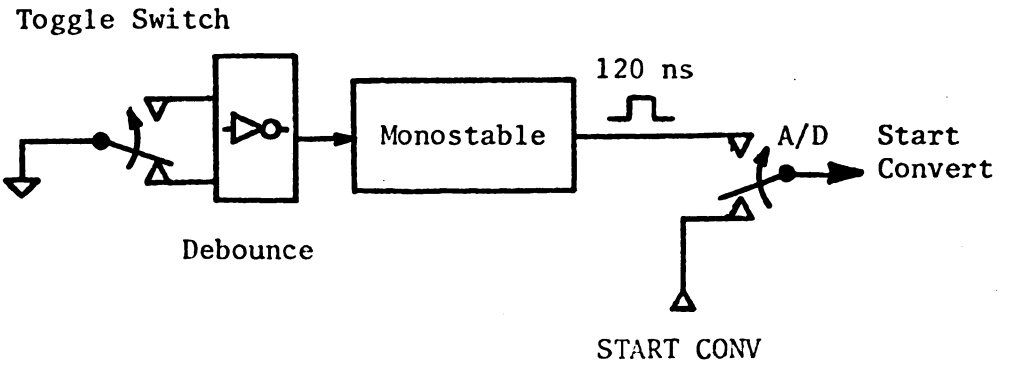


Figure 3.5 Manual sample and convert features

the instrumentation amplifier is tied to the analog ground. The negative terminal is either connected to the internal DC reference or to an external AC generator depending upon the status of the AC/DC switches. For both options, the Input/Output switches allow the inspection on the AC or DC voltmeters of both the input and output signals. The ratio between both signals defines the gain. Due to the high common-mode-rejection ratio of the amplifiers, gain calibration with or without external offset yield the same results. With the AC option, both input and output can be viewed on an oscilloscope. This feature is useful when noise phenomena or possible oscillations at very high gains are to be examined. For the external offset/chain calibration -- EO/CHAIN -- modes, the positive input of the instrumentation amplifier connects directly to the external offset and the negative input to the internal DC reference. The value of the output is automatically displayed on DC Voltmeter #2. The Input/Output switching modules permit both signals on the input terminals to be checked and have been renamed Vin-/Vin+ for this case for obvious reasons. This mode is not only devoted to the adjustment of the external offset but also to perform the evaluation of the overall transfer equation for each individual channel. This operation is entitled chain calibration and is exposed in the next paragraph.

3.3.3 Chain Calibration

Chain calibration is necessary to take care of all inherent errors. Even when minimized, their cumulative effects can be significant. The major errors are the internal offsets of the instrumentation amplifier, the sample-and-hold device and the buffer amplifier as well as the offset of the A/D converter and its nonlinearity, differential nonlinearity and

quantizing errors. Gain and nonlinearity errors of the sample-and-hold device can be considered as negligeable according to the manufacturer's data sheets. In addition, due to the excellent impedance characteristics of its sources and load, the multiplexer does not introduce any transfer error. Taking the main errors into account, the partial transfer equationa are

$y_1 = Ax + B$ for the instrumentation amplifier

$y_2 = y_1 + C$ for the sample-and-hold device

$y_3 = y_2 + D$ for the buffer amplifier

$y = Ey_3 + F + G$ for the A/D converter

where:

$x = V_{in-} - V_{in+}$

A = gain of the instrumentation amplifier

B = offset of the amplifier

C = offset of the sample-and-hold device

D = offset of the buffer amplifier

E = gain of the A/D converter

F = offset of the A/D converter

G = nonlinearity + differential nonlinearity + quantizing errors

y = digital code

All parameters, except G, are fixed but may vary slightly with temperature. G on the other hand occurs randomly in time with positive and negative excursions and therefore may be considered as a random variable with zero mean. For that reason, when taking the average of several digital samples for a very stable analog voltage x, the overall transfer equation is simply:

$$y = AEx + (EB + EC + ED + F).$$

Thus each channel has a transfer equation of the form:

$$y = Mx + N$$

This equation may be rewritten in an equivalent form as:

$$y = Mz + P$$

where:

$$z = x + Vin_{+}$$

$$P = N - M \cdot Vin_{+}$$

M and P are two coefficients to be evaluated. Once their values have been computed, the analog voltage samples are easily recovered from the stream of digital data by applying the following equation:

$$z = \frac{y-P}{M}$$

To compute M and P, the requesite steps are as follows. First, by means of the gain calibration feature, the gain is adjusted to a desired value that will remain unaltered at least until the overall data acquisition process has been completed. Then with the external offset calibration circuit, the positive input terminal of the instrumentation amplifier is adjusted to the value displayed by the averaging voltmeter. This value represents the DC component of the signal delivered by the anemometer of the given channel. From that point in time, Vin- is adjusted so as to yield a value on DC Voltmeter #2 close to the upper extreme of the full scale of the A/D converter.

A series of conversions is then performed under program control and a first couple of values (z_1, y_1) obtained. The process is finally repeated with Vin- chosen so as to produce an output voltage on DC Voltmeter #2 near the lower extreme of the full scale. This operation yields a second

result (z_2, y_2). M and P are then simply obtained by the formulas:

$$M = \frac{y_2 - y_1}{z_2 - z_1} \text{ bits/Volts}$$

$$P = \frac{z_2 y_1 - z_1 y_2}{z_2 - z_1} \text{ bits}$$

These coefficients define a precise correspondence between the analog voltages and their corresponding digital samples. After each chain-calibration, care must be taken not to alter the external offset or the gain of the amplifiers in order to keep the coefficients unchanged for the overall data acquisition process.

3.4 Summary

The chapter presented a typical data acquisition system with sixteen analog inputs and a 12-bit digital output. The incoming signals can be amplified with gains of two to two-hundred, adjustable with on-board potentiometers accessible from the front panel. DC components between -5.5 V and +5.5 V can be eliminated by means of external offset voltages. With a gain of two, AC signals with maximum deviations of $\pm$ 2.5 V can be converted. On the other hand, only peak values not exceeding $\pm$ 25 mV are measurable for a gain of two hundred. In the optimal case, sampling rates of 10 kHz/channel can be achieved for eight channels. Due to the short duration of the calibration procedure and the data acquisition process, drifts due to temperature are expected to be negligeable. As optimal conditions are rarely met, inherent transfer errors will have to be minimized by allowing more acquisition time for the sample-and-hold devices and more settling time for the multiplexer, i.e, by reducing the maximum expected

sampling rate. The next chapter treats the design of the microcontroller and considers this important factor, when allocating specific time frames to the elementary operations within a data acquisition cycle. All additional inherent errors, namely the internal offsets, are taken care of by the chain calibration of each individual channel. But special attention must be given to the minimization of noise voltages at the inputs because they yield digital output errors that are proportional to the gain. As a reference, with a gain of two, the output error corresponding to an input noise voltage of $\pm$ 0.5 mV is 1/2 LSB. This problem must be dealt with during the construction of the circuits. The tests performed to evaluate all the real performances of the system with respect to the previous considerations, and their results will be presented in Chapter 5.

CHAPTER IV

HARDWARE ORGANIZATION OF THE MICROCONTROLLER AND THE UTILITY LOGIC

This chapter presents a more in-depth analysis of the microcontroller and its associated utility logic. The utility logic is described in Section 4.1. As indicated in Chapter 2, its purpose is to store the sequence of the selected channels and the delay required for a variable sampling rate. These user-defined functions serve as parameters for the microcontroller. Section 4.2 discusses the hardware organization of the microcontroller and the necessary steps in its design.

4.1 Hardware Organization of the Utility Logic

Figure 4.1 illustrates the organization of the utility logic. Two main hardware sections can be distinguished: the interface and the RAM/delay circuit. These are described in detail in the following subsections.

4.1.1 Interface

The interface, a general purpose DRV-11 parallel interface board from Digital Equipment Corp. (6), directly connects to the LSI-11 bus. It is characterized by sixteen diode-clamped data input lines -- IN00-IN15 -- and sixteen latched output lines -- OUT00-OUT15 for input/output data transfers operated under program control. In addition, the interface provides the user with four control lines for hand-shaking purposes. These are: NEW DATA RDY, DATA TRANS, REQ A and REQ B. The latter two permit interrupt requests to be generated from the interface peripheral

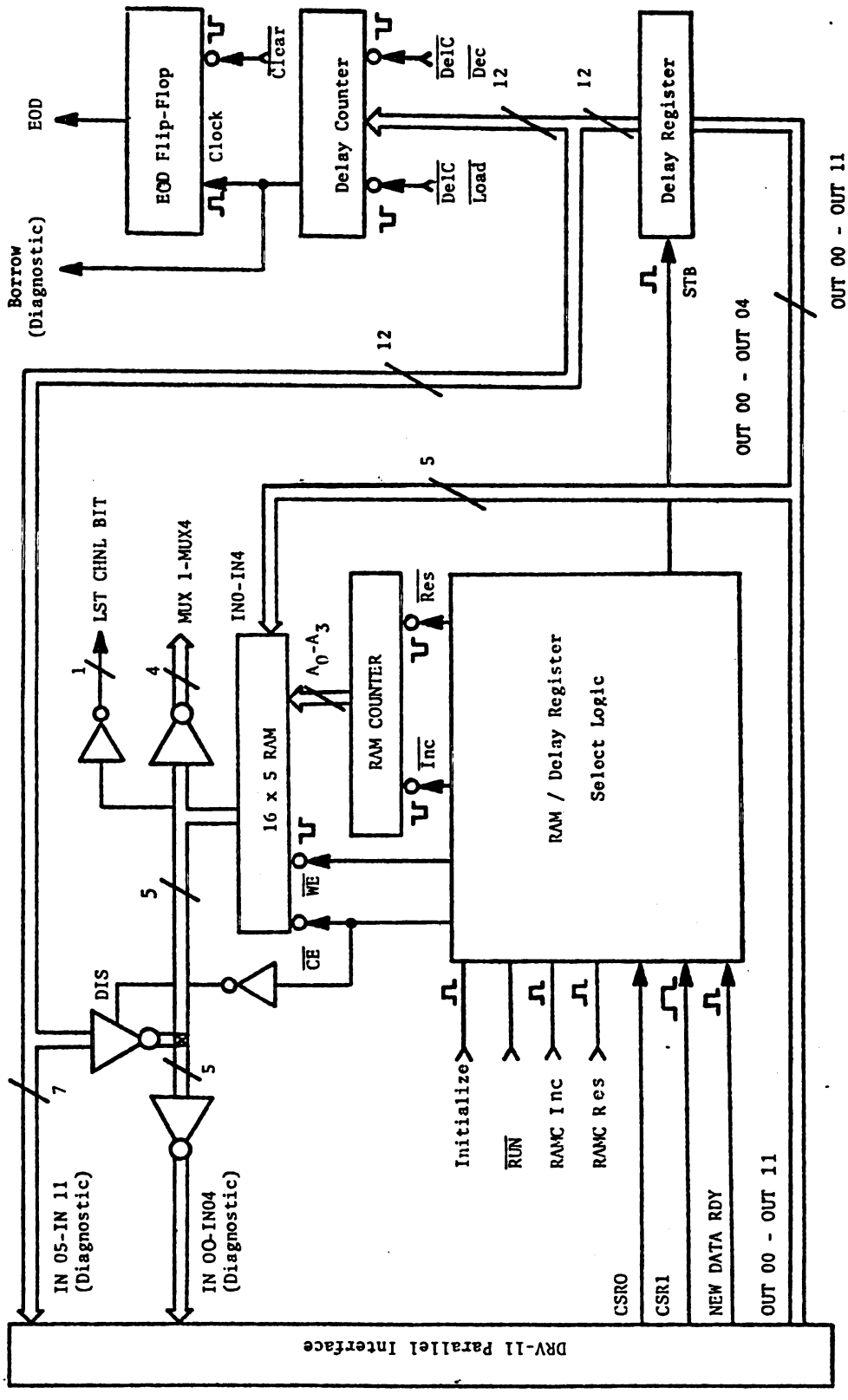


Figure 4.1 Hardware organization of the utility logic

to the computer. NEW DATA RDY (DATA TRANS, respectively) is a pulse which informs the user that an output transfer (an input transfer, respectively) is taking place. This particular application makes use of the NEW DATA RDY pulse only. Its pulse width is normally 350ns but can be extended to higher values of up to 1500ns by adding an external capacitor. The trailing edge of NEW DATA RDY may be used to strobe the output data into the user's device. Since the data is not stable when the leading edge of the pulse occurs, an option on the board allows the pulse to be shifted in order to use this leading edge for the same purpose. Finally, two additional lines -- CSR0 and CSR1 -- are available to control the interface peripheral. They are set and reset under program control by setting or resetting their respective bits in the Control Status Register. Also, an initialization line -- INIT -- is provided for optional interface resetting.

4.1.2 RAM/Delay Circuit

As illustrated in Figure 4.1, the DRV-11 interface board, described in the previous section, is used to transfer data to the RAM and to the delay register. Figure 4.2 gives the detailed diagram of the select logic that is used to strobe the data into one terminal or the other. Data transfers only take place when the microcontroller is in the idle mode, i.e., none of the lines controlled by the microcontroller are in their true state. A low level on CSR0 (high level, respectively) selects the delay register (the RAM, respectively). To load the RAM, only the five least significant bits are necessary. For the register on the other hand, twelve bits are required for reasons which become obvious in the next section. The CSR1 line is used to increment the RAM counter. This

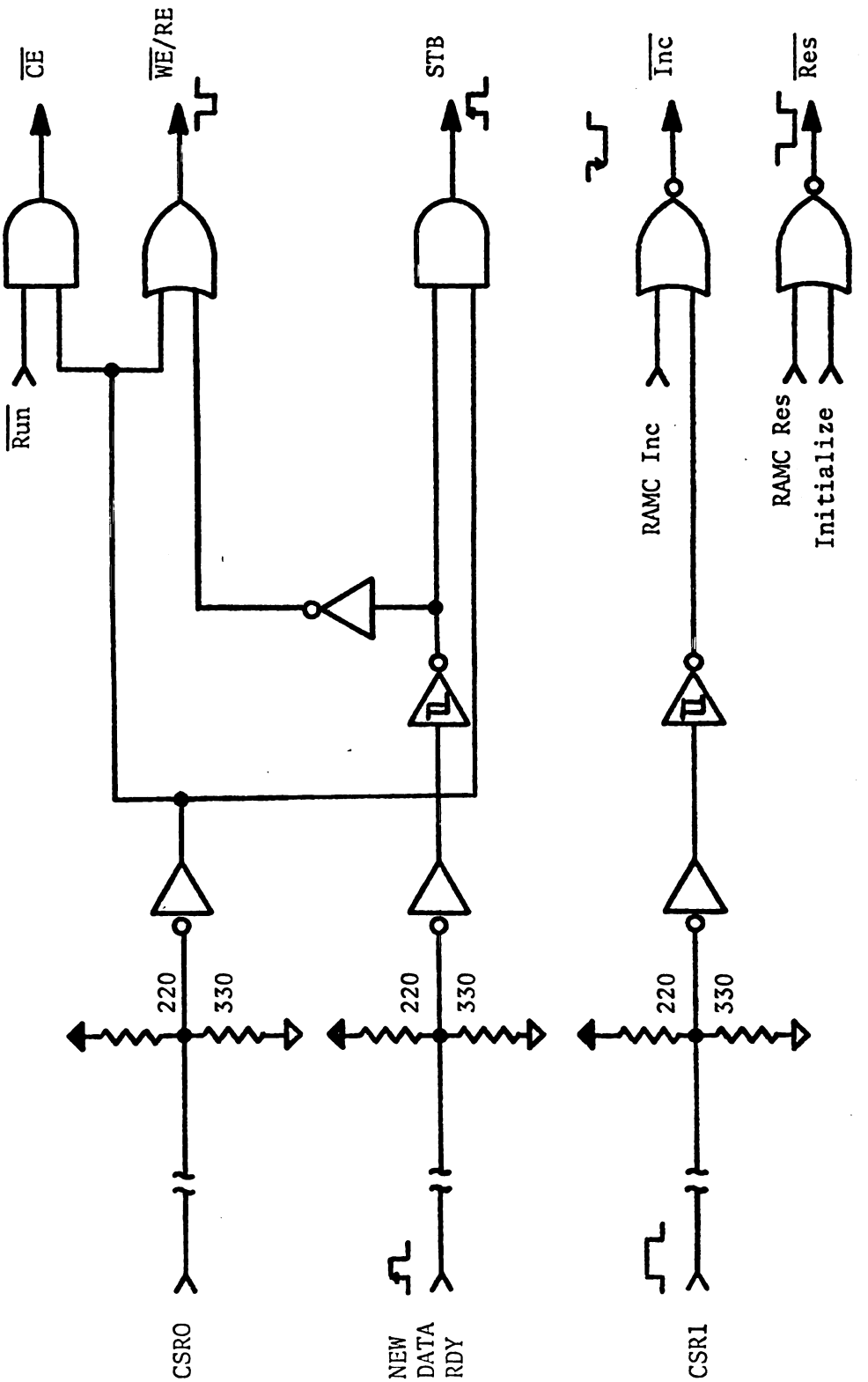


Figure 4.2 RAM/delay register select logic

counter is reset by means of the Initialize line. In other words, it is automatically reset during the Power-On transition of the acquisition unit and the Power-On mode of the minicomputer -- caused by the reset pulse on the INIT line; and it may also be reset under program control by making use of the FCNT2 line of the DRV 11-B. NEW DATA RDY is employed to control the Write Enable line -- $\overline{WE}$/RE -- as well as the strobe -- STB-- of the delay register. The resistor ladder networks are provided to eliminate unwanted transmission line effects.

When the microcontroller is in the RUN mode, the RAM is constantly enabled and its counter controlled by the RAMC Inc and RAMC Res lines. In a similar way during the RUN mode, the delay counter is loaded and decremented by the $\overline{\text{DelC Load}}$ and $\overline{\text{DelC Dec}}$ lines at appropriate times. This counter consists of three cascaded synchronous 4-bit binary up/down counter modules --74193 -- with preset inputs and generates a Borrow pulse during the transition from zero to underflow. The Borrow signal sets the End of Delay flip-flop -- EOD -- which notifies the microcontroller of the termination of the delay. The statuses of the EOD flip-flop and of the last channel bit -- LST CHNL BIT -- are regularly examined by the microcontroller that uses these as parameters to generate a unique sequence of states among the set of the allowable sequences.

Finally, a minimum of hardware has been implemented to check under program control the contents of the RAM and the delay register. The input buffer of the interface is utilized to perform this task. In addition a few lines, namely RAMC Inc, RAMC Res, LST CHNL BIT, Borrow and EOD, can be tested with the diagnostic features of the microcontroller. These features are referred to in more detail in the next section.

4.2 Hardware Organization of the Microcontroller

The main blocks of the microcontroller are represented in Figure 4.3. The control logic represents the core of this unit. In normal operation it is driven by the internal clock circuit, but for diagnostic purposes it is driven by a program-controlled clock generated through a DRV-11 interface board. The CSR1 line of this interface is used to select either mode. The control logic also drives the ROM counter and uses the microcode of the ROM to generate the desired commands and decide upon the next state. The following paragraphs are devoted to a more complete discussion of these building blocks, their properties and the tasks they perform.

4.2.1 The Clock Circuit

The clock circuit generates a square wave -- TP -- at a rate of 1MHz (see Figure 4.4). This pulse train is used to increment the ROM counter. Its frequency, therefore, corresponds to the basic execution cycle of the microinstructions. This frequency has been chosen because it allows very precise sampling rates in the integer range. The execution cycle is composed of two phases represented by the timing pulses tp_1 and tp_2. These series of impulses originate from a 4-MHz CMOS crystal-controlled oscillator that is enabled and disabled by setting or resetting a flip-flop. A low-to-high transition on the FCNT1 line from the DRV-11B board initiates the data acquisition process, by triggering a monostable whose outputs are used to reset the control logic and to set the enable flip-flop. On the other hand, any pulse on the Initialize line, mentioned in the previous section, ends or disables the process. The $\overline{\text{RUN}}$ line, also shown in Figure 4.4, is used

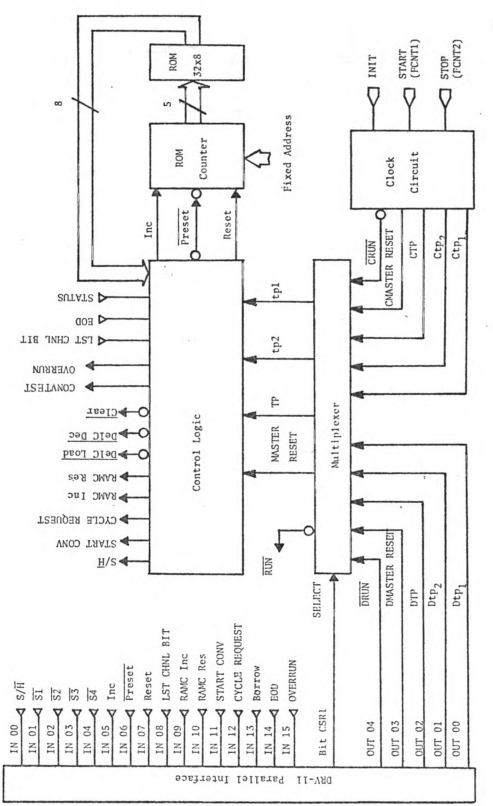


Figure 4.3 Block diagram of the microcontroller

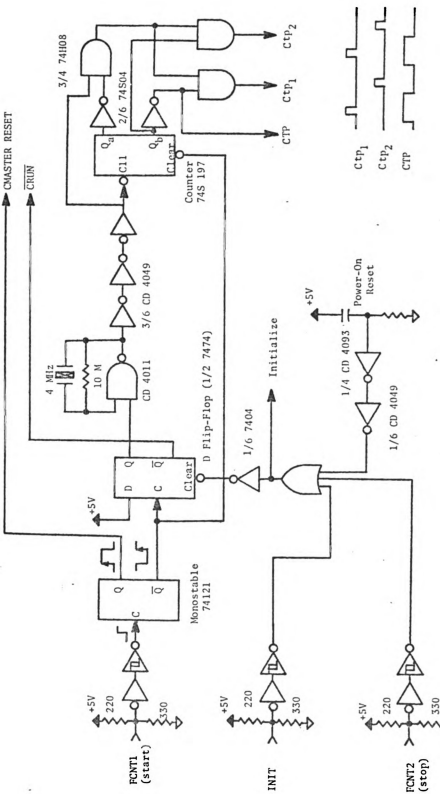


Figure 4.4 Function block diagram of the clock circuit

to enable the RAM of the utility logic and to drive an LED circuit on the front panel to inform the user that the system is in the RUN mode.

4.2.2 Microcontroller Design Considerations

4.2.2.1 Basic Microinstruction Cycle

Figure 4.5 illustrates a typical microinstruction cycle with the transitions in the ROM circuit. The data on the ROM output is not stable during tp_1, therefore tp_2 is used to generate most of the commands by simply AND-ing this pulse with dedicated output lines of the ROM. Combined with the statuses of LST CHNL BIT and EOD, these commands control most of the state transitions of the control logic. tp_1 and TP are only used for minor state transitions.

4.2.2.2 Time Allocation for the Main Tasks

The diagram given in Figure 2.5 serves as a starting point in allocating fixed time intervals for the sampling, settling, conversion and data transfer tasks.

To achieve at least a 10 kHz/channel sampling rate for eight channels, one must try to solve the equation:

$$A + 8B + D = 100\ \mu s, \qquad (1)$$

where

A = allowed sampling time in μs;

B = allowed conversion period for one channel in μs;

100 μs = sampling period corresponding to 10 kHz;

D = optional delay in μs which should be kept small when solving this equation.

Equation (1) has three unknowns. A and B are two degrees of freedom that satisfy the following:

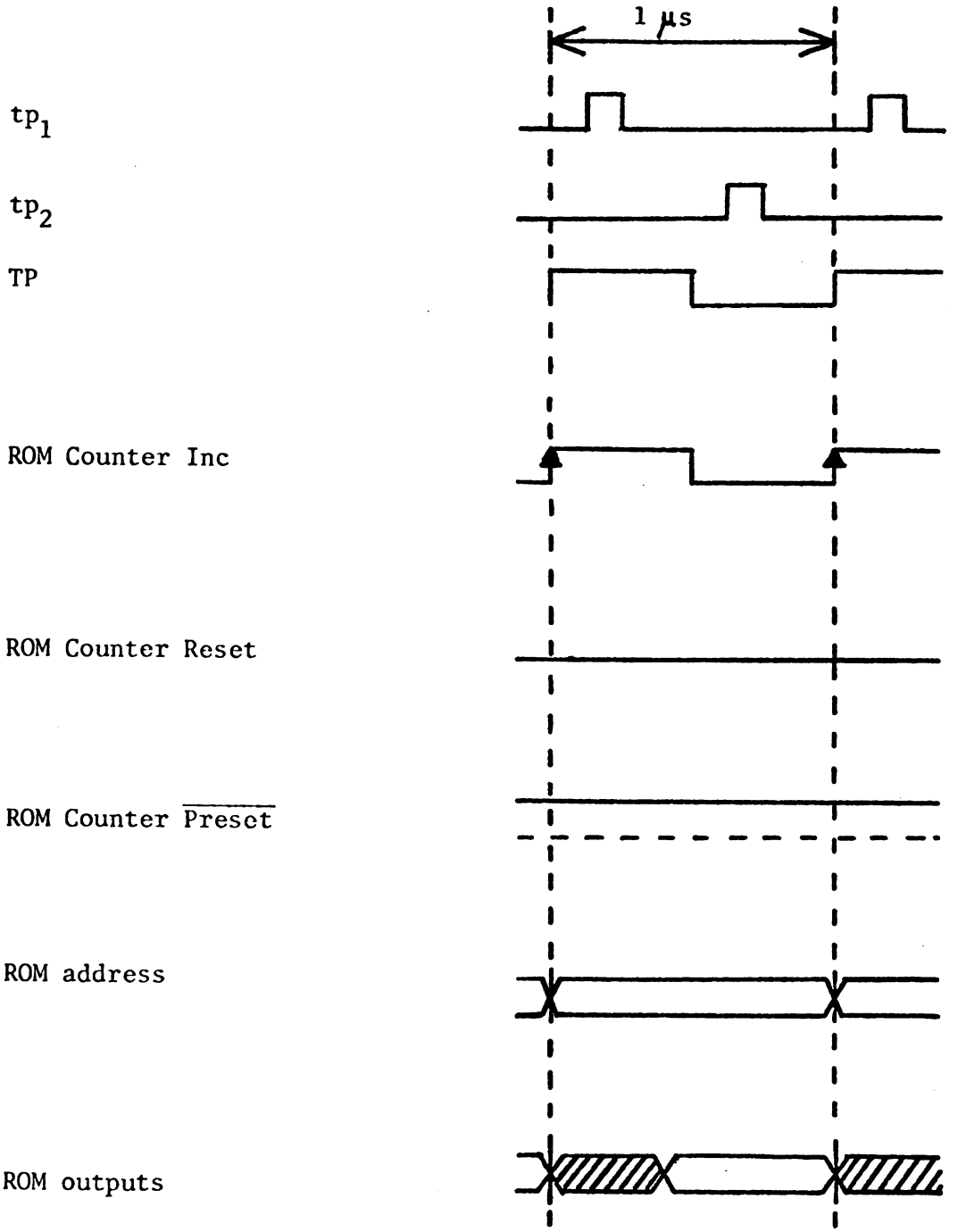


Figure 4.5 Typical microinstruction cycle

A > rated acquisition time of the sample-and-hold devices

B > rated settling time of the multiplexer + rated analog-to-digital conversion time

Moreover, since D, the delay time must be positive,

$$A + 8B \leq 100\ \mu s.$$

Furthermore, for simplicity, it is strongly recommended to take integer numbers for A and B, and D a fortiori, so that all tasks can be performed in an integer number of microinstruction cycles.

An optimal choice for A and B is

A = 8 μs

B = 11 μs

This selection allows enough additional time to perform each task within adequate safety margins. Both rated and allowed time intervals are indicated in Figure 4.6, a more detailed version of Figure 2.5, which shows the sequence for two channels only. Figure 4.6 also explains how the data acquisition process is initiated.

With the values of A and B established previously, any allowable data acquisition sequence can be described by the following more general equation:

$$A + NB + D = T, \qquad (2)$$

where

N = number of channels

T = desired sampling period in μs

D = delay in μs that may include a small fixed delay D_f and an optional variable delay D_v stored in the delay register.

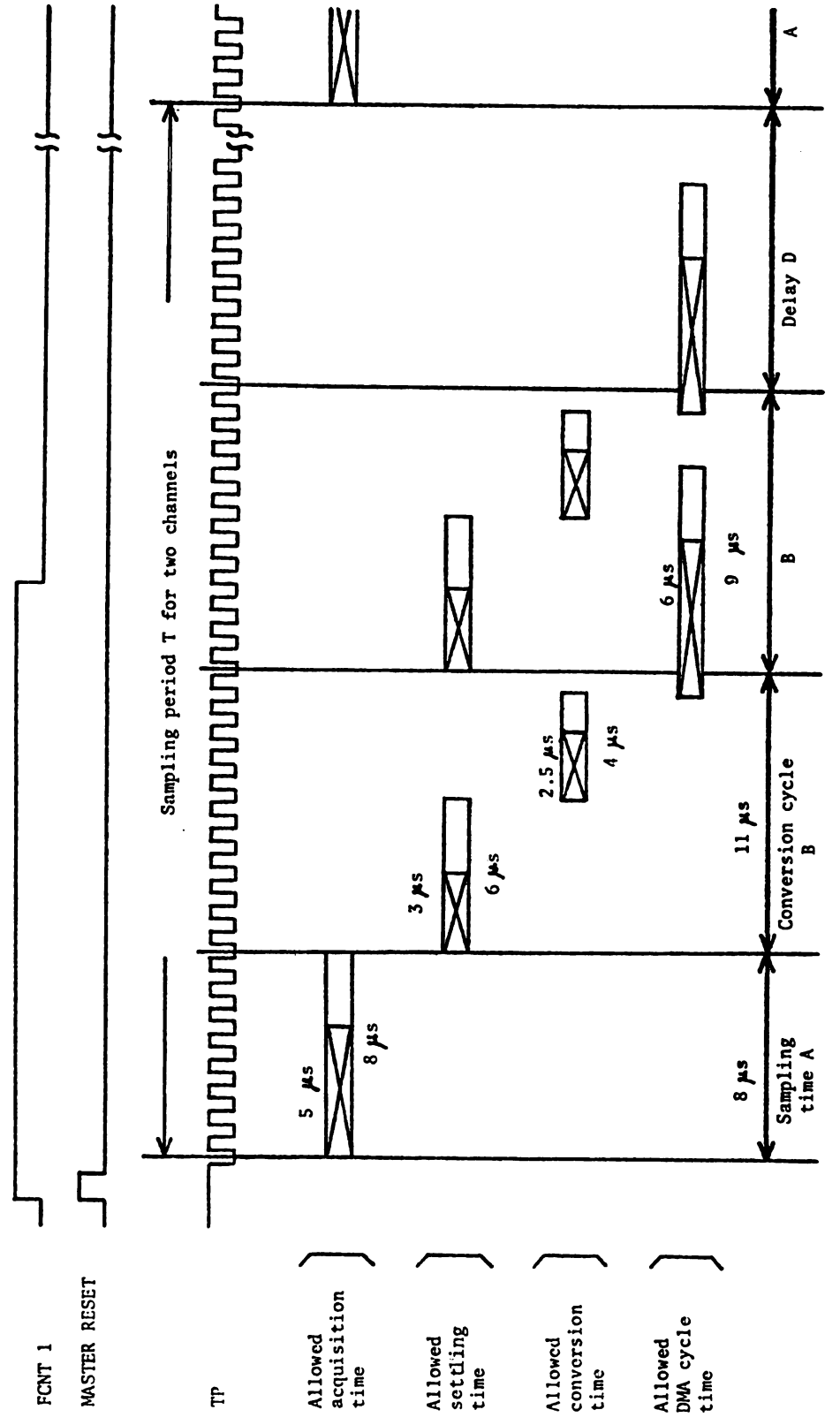


Figure 4.6 Microcontroller timing relationships

In this application, D_f is a fixed delay of 2 μs, corresponding to two additional microinstruction cycles added to the conversion period of the last channel. The purpose of this fixed delay becomes more obvious when examining the detailed timing diagrams given in later subsections. From the aforementioned equation it appears that for a given number of channels N, the maximum sampling rate, i.e., the minimum sampling period, can be easily computed by taking $D_v = 0$. Similarly, the minimum possible sampling rate is attained with $D_v = D_{v_{max}}$. A twelve-bit register is used for the delay register to achieve sampling rates of as low as 250 Hz. Therefore, $D_{v_{max}} = 2^{12} - 1 = 4095$ μs. Thus, the minimum -- $Tmin_N$ (μs) -- and maximum -- T_{max_N} (μs) sampling periods are

$$T_{min_N} \text{ (μs)} = A + NB + D_f$$

$$T_{max_N} \text{ (μs)} = A + NB + D_f + D_{v_{max}}.$$

So, the maximum and minimum sampling rates can be evaluated for any number of channels. Their values are presented in Table 4.1.

4.2.2.3 Design of the Control Logic

The control logic drives the ROM Counter and decodes the microcode to generate the required commands. To minimize the hardware, the ROM is kept as small as possible. Therefore, the microcode of any repetitive sequence is only stored once and a presettable counter is used to repeat the sequence in question. Only two levels of repetition are involved. The overall sampling period is repeated by resetting the counter and the channels are converted successively by presetting the counter repetitively

TABLE 4.1

SAMPLING RATES AS A FUNCTION OF THE NUMBER OF CHANNELS

N	T_{min_N} (μs)	T_{max_N} (μs)	f_{max_N} (kHz)	f_{min_N} (Hz)
1	21	4116	47.619	243
2	32	4127	31.25	242.3
3	43	4138	23.256	241.6
4	54	4149	18.518	241
5	65	4160	15.385	240.3
6	76	4171	13.158	239.7
7	87	4182	11.494	232.1
8	98	4193	10.204	238.5
9	109	4204	9.174	237.9
10	120	4215	8.333	237.2
11	131	4226	7.634	236.6
12	142	4237	7.042	236
13	153	4248	6.536	235.4
14	164	4259	6.098	234.8
15	175	4270	5.714	234.2
16	186	4281	5.376	233.6

to the same fixed address. The series of events the control logic must follow is represented in Figure 4.7. A thorough analysis of the circuit diagrams of the control logic and the related timing diagrams yields a clear understanding of the way these operations are carried out. Figure 4.8 illustrates the commands associated with the output lines of the ROM. Bit 1 and Bit 2 take care of the sampling and conversion tasks. Bit 4 and Bit 7 are dedicated to diagnostic tests. The first one, combined with t_{p2}, sets a flip-flop that indicates a conversion error on the front panal if the conversion time exceeds 4 μs. Bit 7 on the other hand allows the detection of a malfunction in the Preset or Reset inputs of the ROM counter, during the program-controlled diagnostic procedure. Indeed, this bit is only set in non-allowed microinstructions. If a one is detected, during the diagnostic run mode, the ROM counter overruns the allowed sequence, i.e., the ROM counter is not reset or preset in time. All the ROM data lines just mentioned can be classified as special purpose lines. The remaining lines generate a group of four multi-purpose commands -- CMD3, CMD5, CMD6, CMD8 -- that control most of the state transitions of the main part of the control logic (see Figure 4.9). This circuit is especially necessary at the end of the conversion cycles because it decides upon the next sequence to enter, according to the levels of the LST CHNL BIT and EOD. CMD5 generates either the RAMC Inc or RAMC Res pulses to drive the RAM. It may also disable the Inc line and enable the Preset line of the ROM counter during a given sequence. CMD6 enables the Reset line of the ROM counter and its inverse is simply $\overline{\text{DelC Load}}$. And CMD8 initializes or reinitializes the circuit, and enables the Inc line of the ROM counter; its

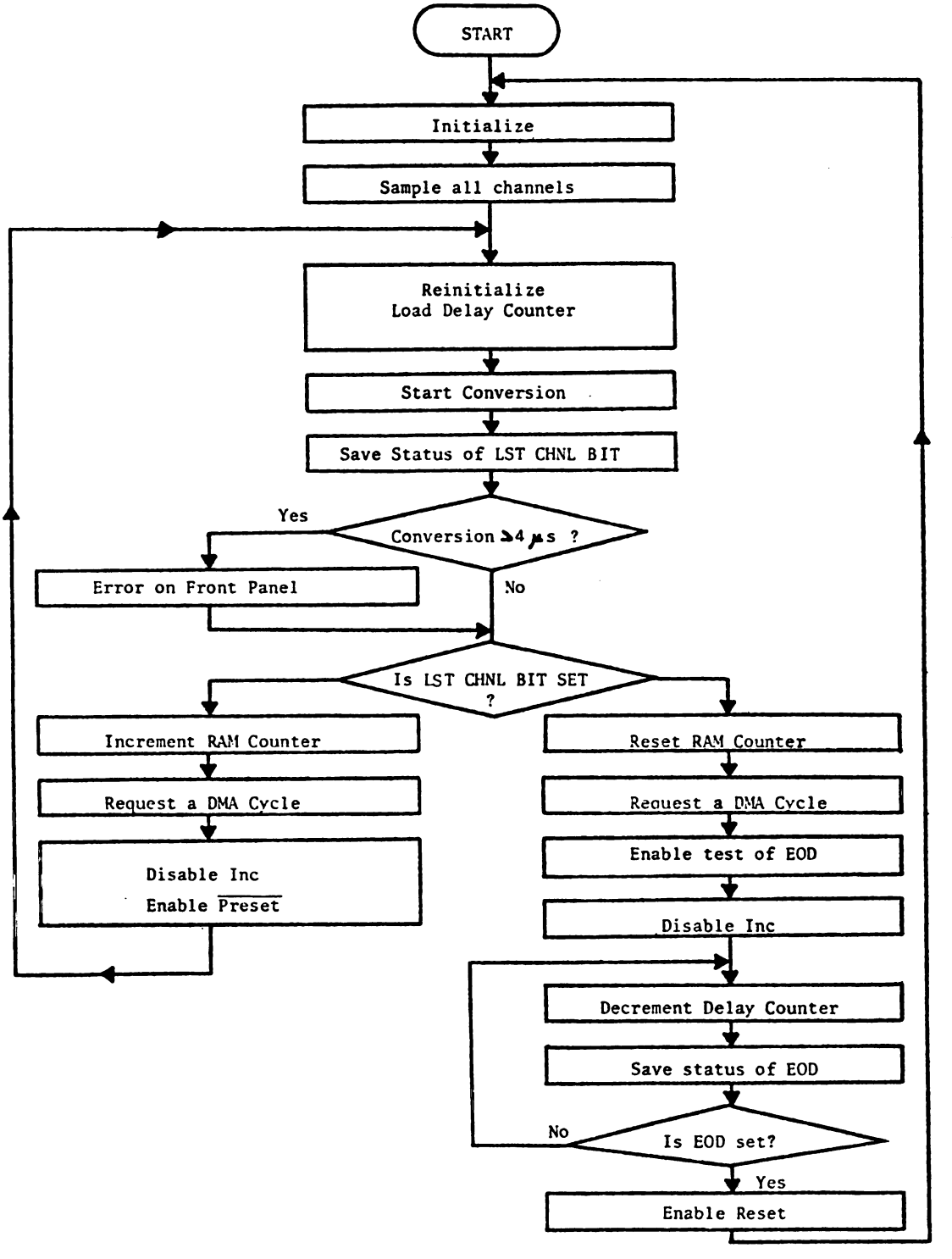


Figure 4.7 Flowchart for control logic activities

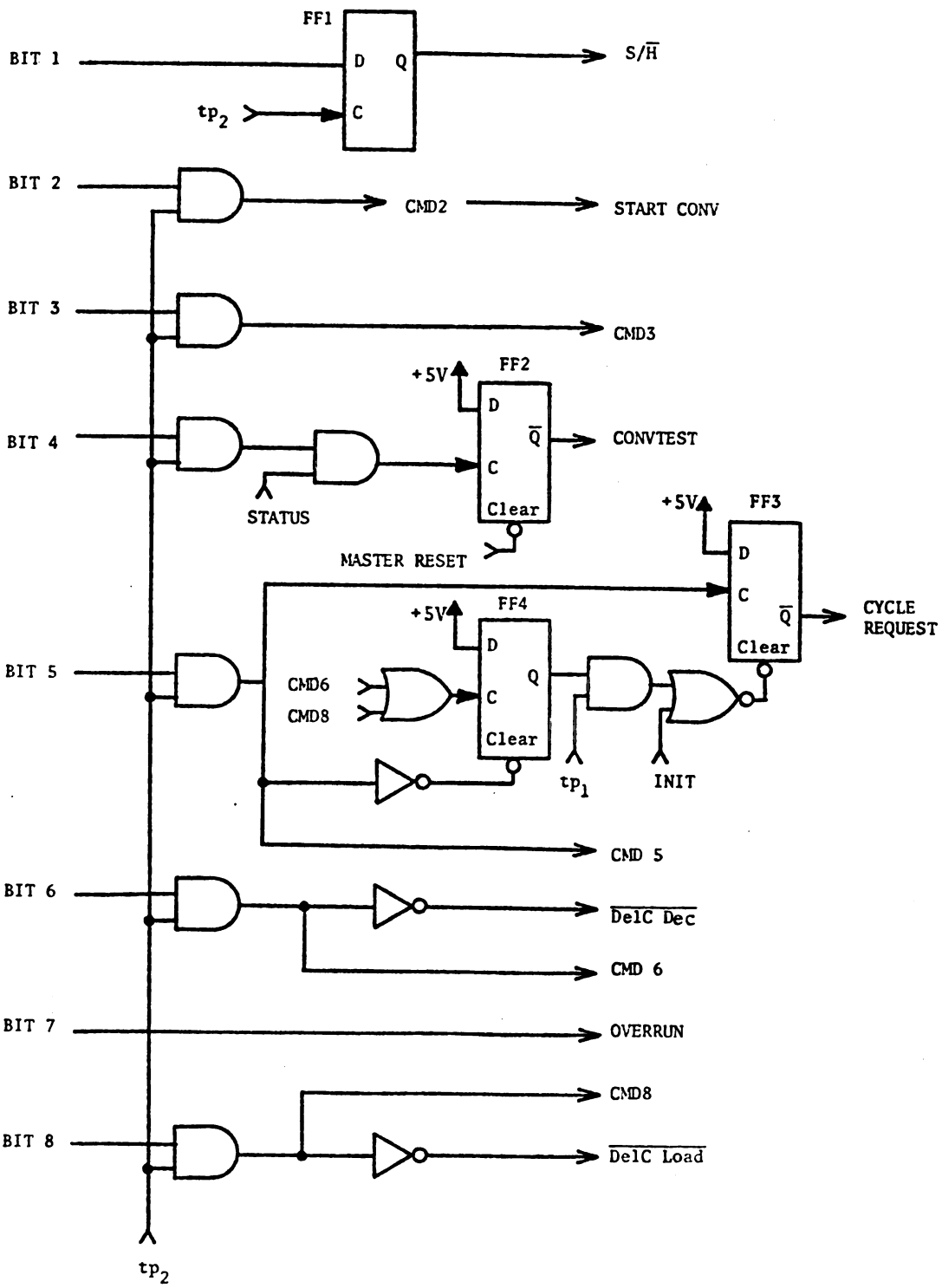


Figure 4.8 Control logic (part one)

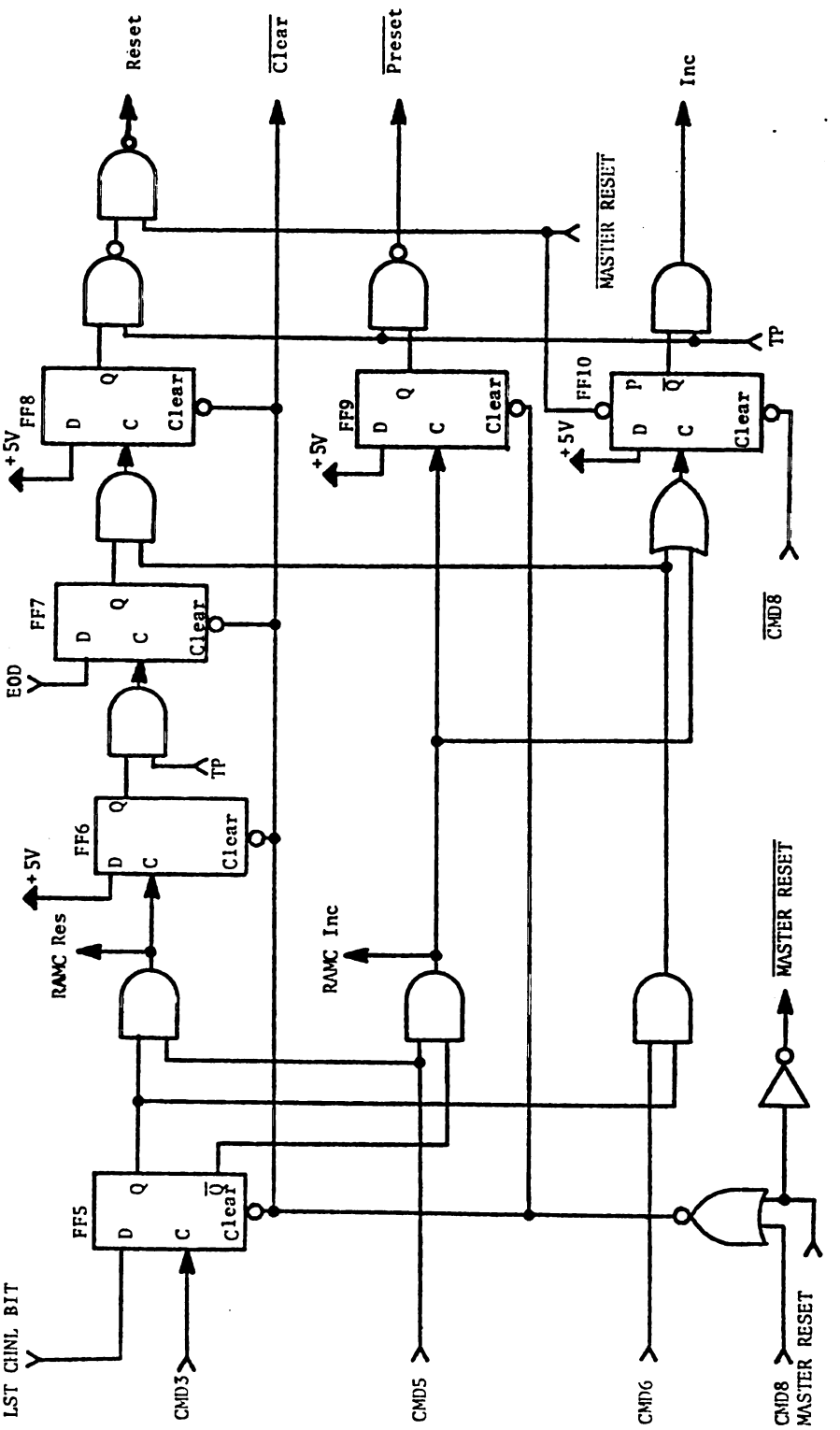


Figure 4.9 Control logic (part two)

inverse is used to load the delay counter. Finally a special circuit was necessary to generate a 1.5 μs cycle request pulse, as illustrated in Figure 8.

Detailed timing diagrams are given in Figure 4.10 and Figure 4.11. For conciseness reasons, identical successive microinstructions have simply been grouped into a single microinstruction. The main state transitions occurring during each cycle are also illustrated. It should be noted that microinstruction x '14' is never entered except at the end of the conversion cycle of the last channel, where it is repeatedly executed until the delay counter decrements to zero. Finally, the complete microcode for the whole sequence is shown in Table 4.2.

4.2.2.4 Diagnostics

The circuits of the control logic are tested by means of program-generated clock pulses. These pulses have a lower frequency than the ones delivered by the internal clock circuit. After each elementary transition, the diagnostic program reads in a 16-bit word. This bit-configuration contains the statuses of the most important control lines of the control logic. The resulting sequence, describing the actual functioning of the circuits during the diagnostic tests, is compared to a table that keeps memorized all the steps of the ideal operation (10). Figure 4.3 shows all the lines that are scanned in order to localize any defective device.

4.3 Summary

Chapter 3 and Chapter 4 discussed all the circuits, analog and digital, involved in the data acquisition unit. The next chapter deals with the tests performed on these circuits and the overall system and with the conclusions they suggest.

TABLE 4.2

MICROCONTROLLER MICROCODE

ROM Address (Hexadecimal)	ROM Contents							
	8	7	6	5	4	3	2	1
x'00'	1	0	0	0	0	0	0	1
x'01'	0	0	0	0	0	0	0	1
x'02	0	0	0	0	0	0	0	1
x'03'	0	0	0	0	0	0	0	1
x'04'	0	0	0	0	0	0	0	1
x'05'	0	0	0	0	0	0	0	1
x'06'	0	0	0	0	0	0	0	1
x'07'	0	0	0	0	0	0	0	1
x'08'	0	0	0	0	0	0	0	0
x'09'	1	0	0	0	0	0	0	0
x'0A'	0	0	0	0	0	0	0	0
x'0B'	0	0	0	0	0	0	0	0
x'0C'	0	0	0	0	0	0	0	0
x'0D'	0	0	0	0	0	0	0	0
x'0E'	0	0	0	0	0	0	1	0
x'0F'	0	0	0	0	0	0	0	0
x'10'	0	0	0	0	0	0	0	0
x'11'	0	0	0	0	0	1	0	0
x'12'	0	0	0	0	1	0	0	0
x'13'	0	0	0	1	0	0	0	0
x'14'	0	0	1	0	0	0	0	0
x'15'	x	1	x	x	x	x	x	x

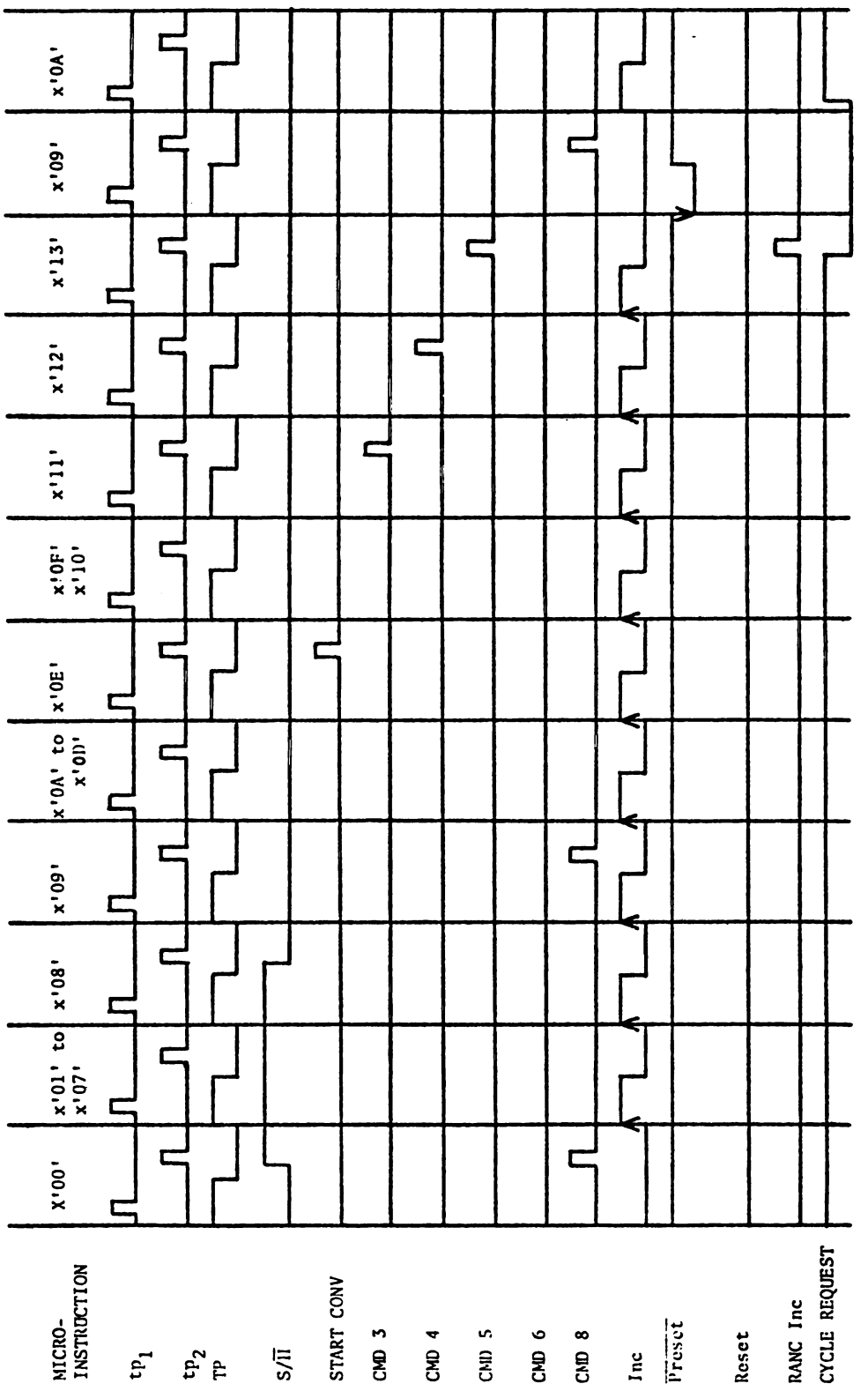


Figure 4.10 Timing diagram for all channels, except the last

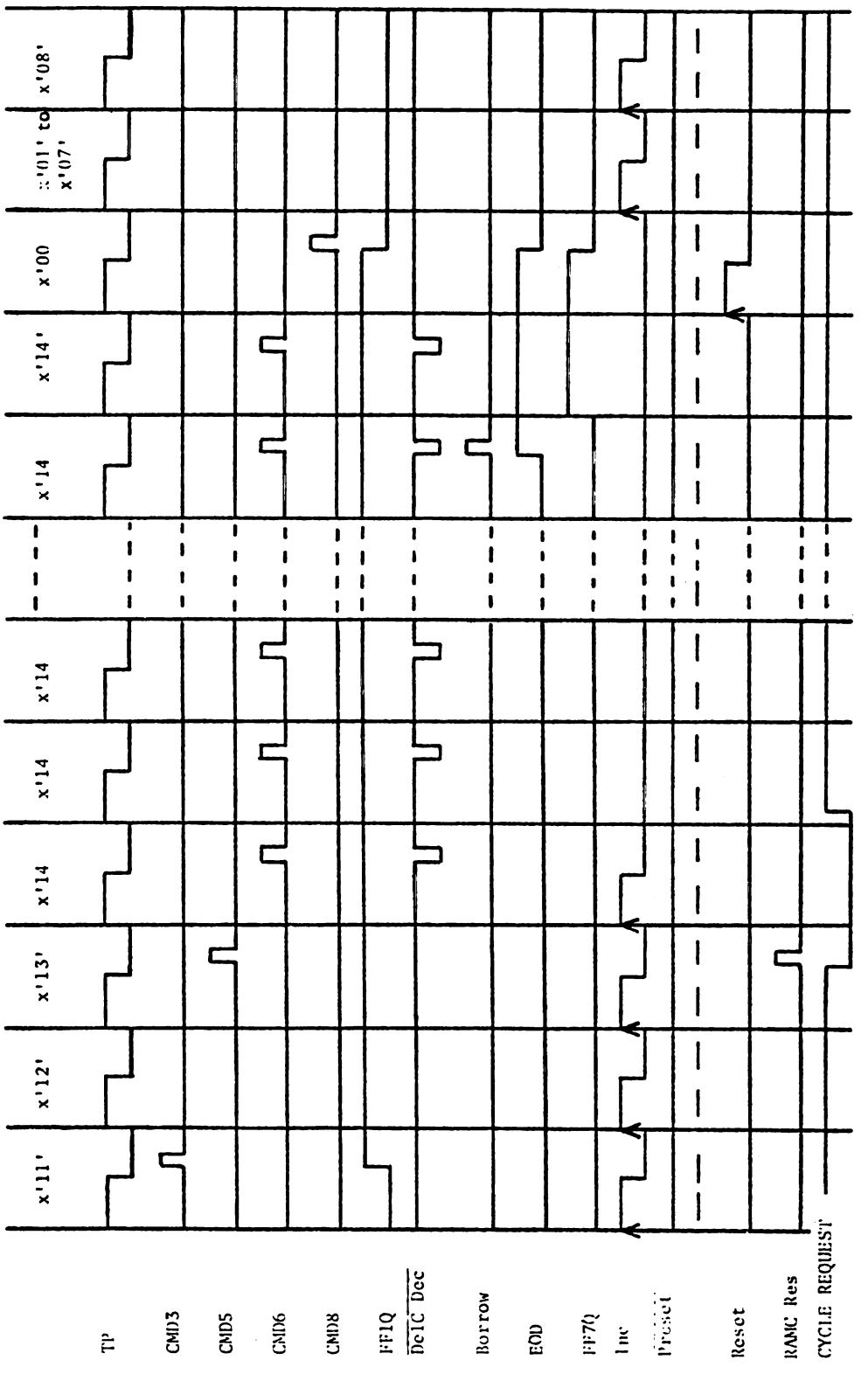


Figure 4.11 Timing diagram for the last channel

CHAPTER V

DEVELOPMENT AND EVALUATION

This chapter summarizes the procedures involved in the development and evaluation of the data acquisition system. Section 5.1 examines the steps in the preliminary study and design phase. The next section focuses on the construction of the data acquisition system and Section 5.3 discusses the tests and their results. These phases account for most of the development time. Other relatively time consuming tasks, such as ordering parts and carrying out unnecessary and annoying administration procedures, will barely be mentioned.

5.1 Preliminary Study and Design

To conduct such a study, a thorough understanding of the requirements and their related aspects was imperative; a few sessions with the project director and research adviser were dedicated to this purpose. Priorities regarding timeliness and cost were also discussed at these meetings. Approximately one man-week (40-hour week) was then necessary to perform a characteristics survey of the devices available on the market. In their comparison, special attention had to be given to the performance vs. cost criterion. Instrumentation amplifiers, sample-and-hold devices, multiplexers and A/D converters from different manufacturers, namely Datel-Intersil, Analog Devices, Teledyne Philbrick, Analogic and Burr Brown were the primary candidates for this application. LSI-11 compatible data acquisition modules from Data Translation were also considered but their capabilities were too restricted, especially

regarding random channel selection and appreciable variations in the sampling rate. A few telephone calls to these companies were necessary for additional technical guidance and procurement of up-to-date information on both cost and specifications. The final assessments forced the decision towards the ultimate choice of an analog-multiplexing/serial-conversion type system using the elements described in Chapter 3. These devices were then immediately ordered because of their lengthy delay time before delivery. The next stage consisted of defining the safety margins for all the tasks within a sampling period (refer to Section 4.2.2.2) and of designing the microcontroller accordingly. This operation and the assignment of ordering the corresponding parts required three additional man-weeks. Finally, four more man-weeks were necessary to design the front panel and the calibration circuit and purchase the necessary components. From that point in time, due to delivery delays, three extra weeks elapsed before construction could really begin.

5.2 Construction

The construction phase lasted nearly three man-months and involved three distinct yet sequential stages. The microcontroller and the analog-to-digital conversion chain were constructed first. Two card-racks with ten vector boards each were necessary (see Figure A.2 in Appendix). The amplifier and sample-and-hold devices for all channels were implemented on sixteen identical and interchangeable boards (see specimen in Figure A.7). The remaining four boards were allocated as follows: one served for the multiplexer and the A/D conversion circuit, two were used for the microcontroller and the last one as an input/output board, as illustrated in the Appendix. An additional board was necessary for the software-

controlled diagnostics. These boards were built and then tested separately. As a following step, the front panel and calibration circuits were implemented. And the final stage was devoted to the interconnections between the various circuits. For this operation, shielded wire was used for all analog connections in order to reduce any undesirable noise effects. Also, to minimize cross-talk between adjacent channels, signal leads were interleaved with ground strips on all connectors. Finally, signal continuity was checked for all connections, and defective wires with short-circuits between shield and core were detected and replaced.

5.3 System Evaluation

5.3.1 General Data Acquisition Procedure

Figure 5.1 shows the general data acquisition procedure. It arranges, in a single sequence, all the operations described in the previous chapters. Before this general procedure could be implemented, more elementary tests had to be performed, as discussed in the next subsection.

5.3.2 Tests and Results

The analog circuits were tested first. Signals from waveform generators were used to evaluate the response of the amplifiers and sample-and-hold devices. During these tests, very-high-frequency oscillations with zero mean (above 10 MHz) with a peak-to-peak amplitude of $\pm$ 1 mV were noticeable on the voltage reference. At first hand they seemed to be worrisome, but it appeared that, due to the bandwidth of the amplifiers, they were not significantly amplified and then they were

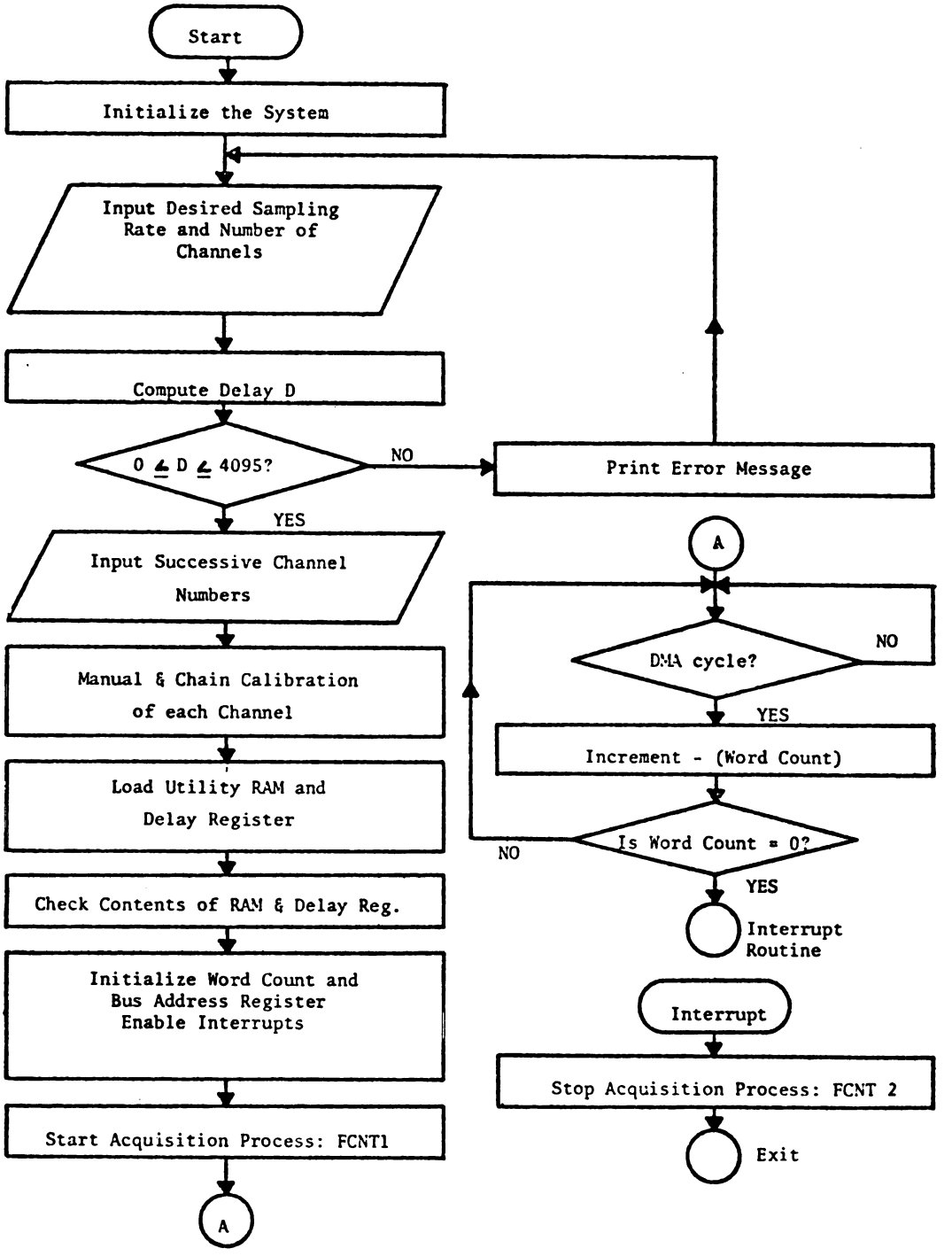


Figure 5.1 Flow-chart of calibration and data acquisition procedure

filtered out by the capacitor of the sample-and-hold devices. Cross-talk between adjacent channels was barely noticeable, in particular the cross-talk due to the multiplexer was around -80 dB as indicated in the specifications. The droop of the various sample-and-hold devices varied significantly from channel to channel but never exceeded $\pm$ 0.500 mV/180 μs. At this point it should be noted that, for any channel, it never takes more than 180 μs till its analog signal gets converted, after each sampling. Finally, the noise induced by the logic circuits was reduced to a tolerable level by means of additional shielding and filtering.

The second phase in the tests concerned the logic circuits. The LSI-11 compatible interfaces were checked first. A maintenance cable was used to connect the outputs of these boards back to their inputs. This method provided a good means to conduct program-controlled diagnostics. In addition, software-generated waveforms were displayed on an oscilloscope to test some of the control lines of these interfaces. The data acquisition unit was then progressively connected to the computer. At first, unwanted transmission line problems were detected and immediately solved. Also, undesired spikes from the computer had to be eliminated by inserting appropriate RC filters. A final problem concerned the utility logic RAM. The contents of the first location were deleted at random points in time. This was caused by an unstable $\overline{WE}$/RE line and solved by appropriate waveshaping circuits.

At this point in time (February 1980) the instrument has gone through its reliability tests and proven to be an appreciable tool for the work it was intended to perform. A more detailed survey of the final test procedures (software and hardware) and their results can be found in the User's Manual that complements this work (10).

CHAPTER VI

CONCLUSION

The design, construction and evaluation of a high-performance computer-controlled data acquisition system were the objectives of this work. Such an instrument is to be incorporated into a complete turbulent flow measurement system using combined simultaneous flow visualization/hot-wire anemometry and located in laboratory facilities of the Mechanical Engineering Department at Michigan State University.

The design of the microcontroller and the choice of the analog components were mainly dictated by the fundamental requirement of achieving sampling rates of 10 kHz/channel for eight channels. Important calibration features had to be implemented to provide the user with adequate and attractive calibration and testing methods. Also, the instrument had to make provision for random channel selection, and to offer gains from two to two hundred to allow a wide range of input signals to be measured in optimal conditions. These basic requirements were all met with the final design. In addition, the effects due to noise could be kept within the expected margins. Concerning the total cost of the project, Table 6.1 summarizes the costs. As it appears, labor cost accounted for two thirds of the overall expenditure.

During the tests, data streams of no more than 32 k-works were taken. The limitation came from the maximum storage space available from the microcomputer. During later experiments, data is expected to be directly transferred to a 23 M-word disc via a microprocessor-based

TABLE 6.1

COMPONENT COSTS

Instrumentation amplifiers	$1,504.00
Sample-and-hold devices	192.00
Multiplexer	75.00
Buffer amplifier	2.00
A/D converter	309.00
Sockets	56.00
Integrated circuits (ROM + RAM + 90 chips)	150.00
Augat sockets	70.00
Display, LEDS	20.00
Crystal	5.00
Card racks	60.00
Boards, connectors	220.00
Flat cable, connectors	230.00
Interlocked switching modules, toggle switches	100.00
Potentiometers, trimming potentiometers	300.00
Resistors, capacitors	20.00
Wire-wrap wires, shielded wire, solder	50.00
Miscellaneous 1 (front panel)	100.00
Miscellaneous 2 (Items from Dr. Fisher's Laboratory)	1,500.00
Power supplies	60.00
	$5,023.00
2 DRV-11 boards	420.00
1 DRV-11B board	580.00
	$6,023.00
Publication fees	200.00
Labor	8,760.00
TOTAL	$14,983.00

interface. The output words of the A/D converter will be strobed into this interface by means of the CYCLE REQUEST pulses that were previously used to initiate DMA cycles. This procedure will allow very long data records to be taken. Another extension concerns the use of the sampling rate to control the shutter-release of a camera for simultaneous flow visualization. Due to the difference between the sampling rates and the shutter speed of the camera, pictures will have to be taken at much slower speeds. For that reason, the camera could be triggered at rates which are integer fractions of the sampling rates. The required pulses could originate, for example from a user-presettable counter driven by the S/$\overline{H}$ pulses generated by the microcontroller. Additional features could be envisioned in the future, but they don't enter the scope of the study. A major improvement in sampling rate could be achieved by using sixteen A/D converters and a multi-processor based system to control the overall data acquisition process. Each individual channel would be associated with a separate microprocessor that has its own data storage capabilities. Moreover, this method could allow the calibration and test operations to be performed automatically, and it may permit data acquisition cycles to be interleaved with cycles for dynamic offset cancellation.

APPENDIX

DATA ACQUISITION SYSTEM PHOTOGRAPHS

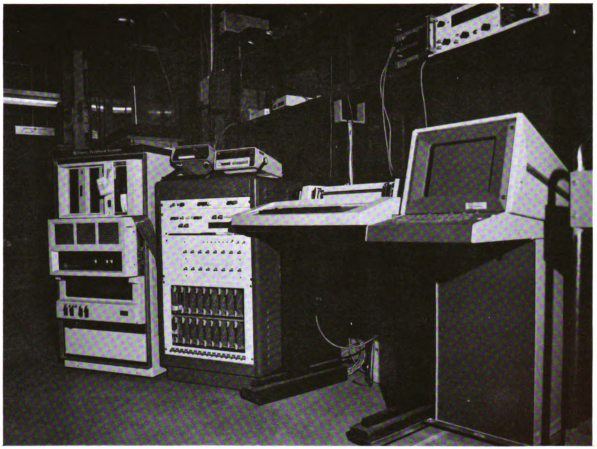


Figure A.1 Data acquisition unit with minicomputer system

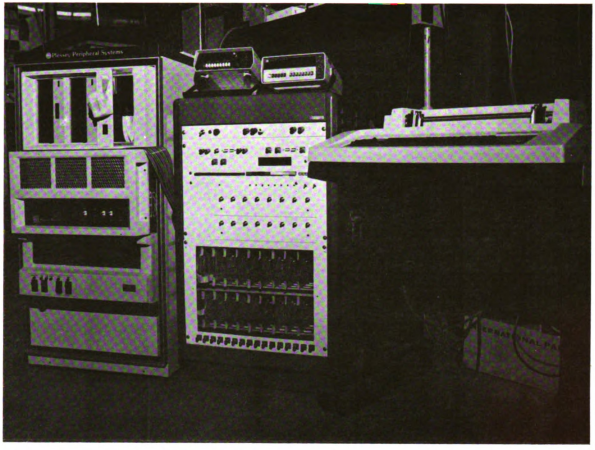


Figure A.2 Closer view of the front panel

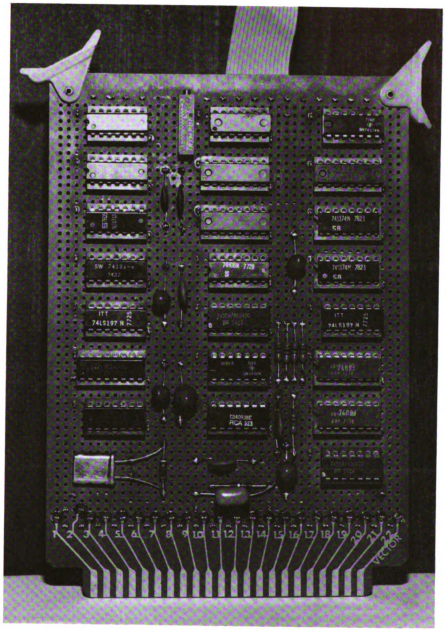


Figure A.3 Logic circuit board 1

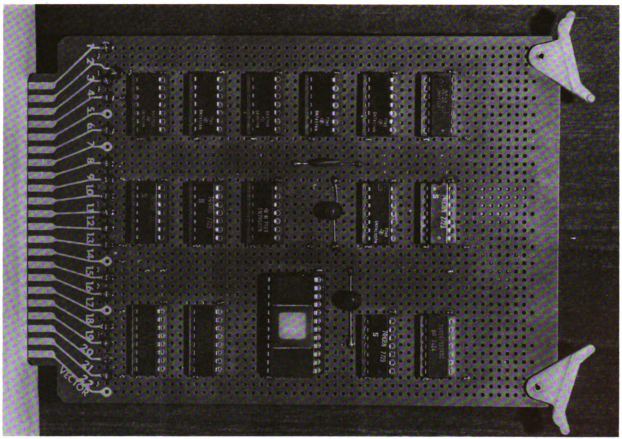


Figure A.4 Logic circuit board 2

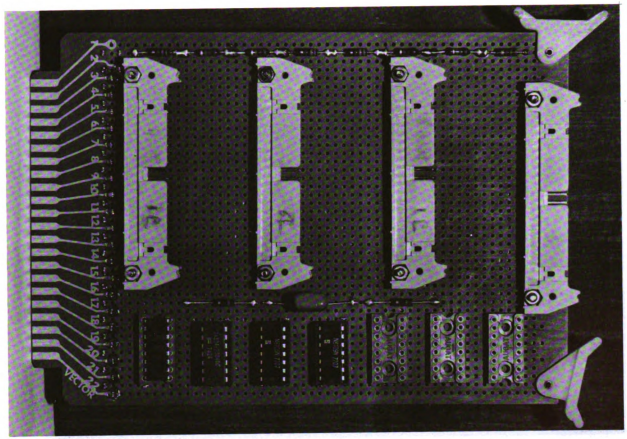


Figure A.5 Input/output board

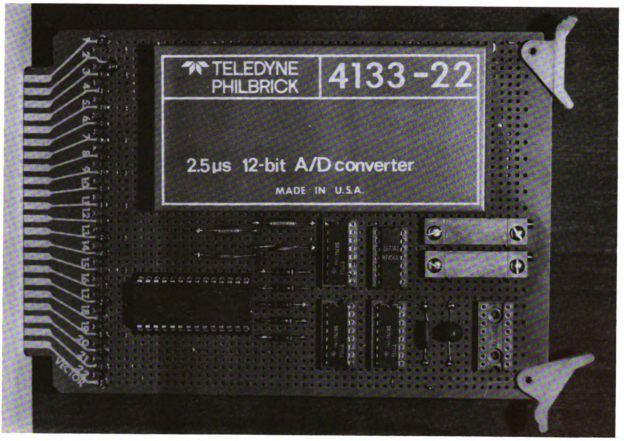


Figure A.6 Analog-to-digital conversion board

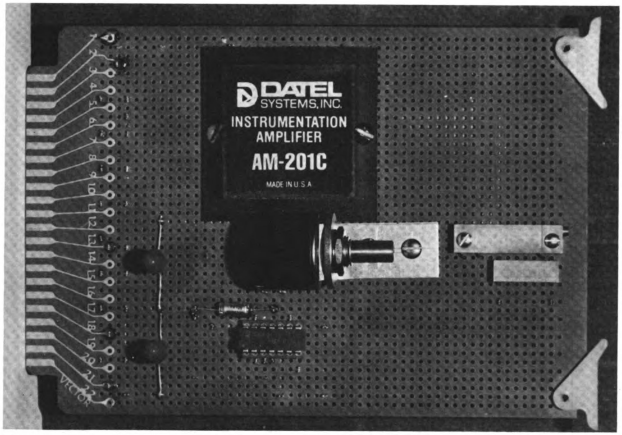


Figure A.7 Typical analog board

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