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By

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ABSTRACT

Inverters For Interconnected Random Sources

By

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Techniques of converting the random power available in the wind into utility-compatible electric form are analyzed. A variable speed rotor is capable of extracting more power from a wind resource than a constant speed one. To utilize variable-speed generators in a utility-interconnected wind system requires some means of frequency conversion. Both current source and voltage source static frequency changers are investigated and field data obtained on operating units is presented. An approach which allows control over utility-side reactive power, ease of harmonic filtering, and which provide a continuous (pulsating) current demand on the power source is developed. These three features are shown to be lacking in the performance data obtained from commercial units.

A 200 VA cascade converter was built and tested in the laboratory. For the dc voltage link regulator to remain stable with simultaneous random variations on its input and high frequency current pulsations at its output, required the development of a multiple feedback controller. Link

voltage level is used for reactive power control of injected current. Low order harmonics are minimized using a PWM inverter and filter. The necessary high frequency switching was accomplished using bipolar transistors.

For Doreen

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CHAPTER I

INTRODUCTION

The need for conservation of conventional fuels has stimulated investigation of alternative electric energy sources. On the scale of the electric power industry some of these sources represent minuscule contributions to capacity while others appear to have the potential of supplying several per cent of capacity. From a functional point of view, alternative energy sources can be considered dispersed storage and generation (DSG) or solar driven. When considering the form of the electrical energy produced by many of these sources the need for power conditioning becomes evident because it is necessary to inject electrical energy into the utility network in controlled AC form. Although the use of power electronic devices is not new to the electric power industry, e.g.: the use of thyristors in high voltage direct current (HVDC) transmission, the integration of inherently direct current sources requires the use of switching semiconductors in increasing numbers.

Dispersed storage and generation includes small hydro installations, battery peaking, fuel cells, and superconducting magnetic energy storage (SMES). Even though hydro is not dependent on power electronic switching devices, the

desire for more efficient storage and generation may require variable speed pumps. In this case power electronics would be required. As for batteries and SMES of utility capacity there is no choice, both are inherently dc.

The DSG class also includes the fuel cell which consumes a variety of hydrogen-rich fuels. It is attractive for dispersed generation near large load centers. Again the need to transmit its output over existing power networks requires converting its output to alternating current.

The solar category includes most sources that are renewable. These include solar photovoltaic, thermionic and wind. The first two are inherently dc in character, the last dependent upon the electrical generator used. This brief introduction illustrates the sources involved. Some are for utility load leveling or fuel-saving only while others serve to augment the capacity of the utility.

The topic of this thesis stems from research performed at the Michigan State University wind test site. Additional data and experience were gained from field tests performed at operating wind generation sites within the state. Unsatisfactory performance of existing wind power conditioning devices stimulated this investigation into inverters.

Because semiconductor switching devices are bistable, the generation of a sinusoidal waveform relies on their proper switching sequence. The class of non-dissipative static converters produces a sequence of output pulses at a frequency equal to or greater than that of the utility

frequency. When switching at the line frequency, the pulse duration and amplitude are chosen to have a fundamental component of some specified character. The fundamental component is separated from this pulse waveform by filtering techniques. By switching at greater than the base frequency this filtering process can be performed more efficiently both in terms of energy and economics. The case where switching is less than some base frequency will not be considered. Power conditioning performed by this class of sampling converters has been extensively researched. The cycloconverter is an example. In the cycloconverter the output frequency is limited to one-third to one-half of the input frequency [44].

The trend to higher switching frequency is from converters operating at 60 Hz quasi-square wave to phase-staggered vector summation at 1080 Hz and more, to pulse width modulated converters operating at several kilohertz. The availability and refinement of switching devices continues the upward trend of switching frequency.

In Chapter Two a survey of present converter design is given along with the conditioning needed for wind generation. Active waveshaping of current has increased to keep high order harmonics at a minimum on the utility networks to avoid interference and overheating. The multi-converter concept has emerged as one topology capable of meeting this requirement. This research adds to the findings of those working in the photovoltaic conversion area by investigating

the cascade topology using a wind turbine as the energy resource.

It is shown in Chapter Five that this converter topology produces minimum torque pulsations on the wind generator. Chapter Three and Appendices present background on switching converters and compares ideal and actual converter behavior. Actual field measurements confirm this and illustrate the pulsating load inverters can impose upon their source. Chapter Four develops the background for the pulse width modulation technique. Here the concepts of real power flow, reactive voltamperes and distortion voltamperes are defined. This material is essential, even though switching converters operate without magnetic energy storage, because their effect on the utility is similar to an induction generator.

The cascade topology represents a viable method of reducing the negative aspects of static converters interconnected to the utility. By providing a continuous flow of input current, the load presented to any of the inherently dc sources is much easier to characterize. Active current waveshaping reduces the filter requirements and minimizes interference with nearby communication and data processing equipment. This occurs because low psophometric current is produced by higher fidelity current waveforms. Psophometric current is a fictitious current such that if it flows in power conductors, the same level of communication interference results as that actually observed. Magnitude con-

trol of an otherwise random source voltage makes it possible to achieve enhanced power factor performance. This is so because the ratio of converter dc port voltage to ac port voltage defines the reactive power requirement.

This multi-stage approach is not without disadvantages. The power must be processed twice. Once to achieve regulation and input current smoothing and again during inversion to alternating current. The forward converter in the wind turbine application is the analog of the series diodes used in photovoltaic systems to protect the array from power reversal (because of heat dissipation limitations).

The conclusions of this research are presented in Chapter Six. Areas open for future research are given. Some practical aspects of interconnected operation are described. These include tolerance to both internal and external faults, capability for soft starting and sequenced disconnect. Utility voltage matching and both frequency and phase matching are required. Finally the inclusion of a "smart" controller is described.

CHAPTER II

WIND ENERGY CONVERSION: THE VARIABLE SPEED METHOD

2.1 Why Variable Speeds?

The conversion of kinetic energy in wind to electrical power can be accomplished in several ways. When it is desired that converted electrical power meet the frequency and voltage constraints of an electrical distribution network for the purpose of offsetting conventional generation, the conversion schemes become limited. At present, electrical power generation from the wind is most economically accomplished by first converting wind energy into mechanical torque. This rotational energy is then converted into electrical energy of a form dictated by the character istics of the particular generator used. Thus the conversion of wind energy into electrical form involves at least two separate conversions. First is the conversion to mechanical torque with some energy escaping in the form of heat, turbulence, and sound so that the efficiency is less than 100%. Then conversion of this torque into electrical current is again accompanied by loss mechanisms, mostly heat, so that efficiency is again less than 100%.

The second conversion stage relies on electrical conversion equipment that has been under development for

decades. When horizontal axis wind turbines are used, the advantages of operating the turbine in a variable speed versus a constant speed mode are several [1,2]. In the low wind regimes characteristic of most inland portions of this country, the blade power coefficient C_p, a function of wind speed, can be maximized if the rotor speed is allowed to vary in direct proportion to the wind speed. It is known that propeller-type turbines have a maximum C_p of .59 only at one value of λ. This parameter λ is the ratio of blade tip tangential velocity to the wind stream velocity normal to the blade swept area. It is apparent that since λ varies with the wind speed, the variation of C_p is less when a variable speed rotor is used. A further advantage of variable speed rotors is a smoothing of the electrical power produced because energy in wind gusts can be partly absorbed in accelerating and decelerating the rotor. Also, blade pitch control is not necessary.

The disadvantage is that variable speed rotors produce variable frequency electric power unless commutation is used. In [1] tests on both a variable speed alternator (a 3-phase, self excited, field controlled 20 kW unit) and a constant speed induction generator (3-phase, 25 kW unit) both using the same rotor (34'9" diameter) were evaluated. In tests performed on the induction generator, it was found that overall efficiency (including blade C_p of about .30) was low in the 11 to 13 MPH wind speed range but improved substantially above that. For the alternator tests it was

found that having the generator operate into a battery bank as a means of local energy storage exhibited the lowest overall efficiency. The battery acts to clamp the alternator output voltage which, in turn, reduces the rotor rpm range and thus C_p. This technique has the further disadvantage that at higher power levels battery overcharging becomes a problem. Because the battery charge-discharge efficiency is low (60%-75%), system efficiency suffers. Reducing the overcharge condition and the attendant gassing may require the incorporation of a charge regulator on the battery bank or some means of battery switching. Operation of the alternator with the battery replaced with a large capacitor for energy storage exhibited greater net efficiency. The reason is that C_p is larger due to a wider rpm range of the rotor. The inverter (synchronous, line commutated) input voltage range was greater. A disadvantage of variable speed operation with direct current output is the inclusion of an inverter for operation into the utility network. This represents a third power conversion stage wherein the character istics of the electrical power are modified. The term static frequency changer best defines the function of this third conversion process.

2.2 Electromechanical Converters

In [3] the authors present similar arguments in favor of the variable speed technique. Also presented is a classification of present static frequency changers. These

techniques will be discussed later. First look at methods allowing the generator to operate directly into the utility. These schemes belong to the class of rotating converters. This class can be partitioned into two subgroups, those having a rotating air gap flux in synchronism with the utility, and those in which the armature slips relative to the rotating air gap flux.

The first group contains all synchronous devices in which the torque-producing magnetomotive force (mmf) is stationary with respect to either the stator or rotor. Rotor here refers to the moving portion or armature of the converter which is coupled to the rotor of the wind turbine. The remaining member then has mmf moving with respect to its reference frame whereby electrical energy flows out from its windings in proportion to the input mechanical torque (or vice-versa). Machines in this group are d-c generators, synchronous generators, and alternators--both inductor and permanent magnet types.

The second group contains machines in which the mmf has relative motion to both rotor and stator--hence the term slip. In this case electrical energy is supplied to or from both members. Machines belonging to this group are induction and doubly-fed induction machines. The induction type includes the common caged rotor machine, ac-commutator, and multiple rotor devices. The last category of this group is the wound rotor induction generator. A

T_m, the rotor angular velocity ω_r is less than ω_s so that slip is positive. The electrical input power includes the slip power dissipated in the rotor. When delivering aerodynamic power to the rotor with s negative, the slip power will be dissipated as heat in the generator mode. By providing local VAR support this induction generator will deliver electrical power to the utility in response to the wind turbine torque input. Because mechanical torque (T_m) is proportional to wind speed (WS) squared and WS is a random process, then T_m is random. More will be said on this later. If the induction machine is of the wound rotor type, this slip energy can be recovered. In [3] a matrix of options between the four basic motor types is given and four basic converter types suited to variable speed operation are noted.

The first of these slip energy recovery schemes is from the adjustable speed ac drive field and is the semiconductor implementation of the original "Kramer" drive. In this scheme (also called the subsynchronous static converter cascade), only slip power is converted so that the converter rating is only a fraction of the machine KVA rating. Its topology is that of a rectifier (uncontrolled), d-c link, and line-commutated inverter interconnected to the utility. By varying the inverter firing angle, the loading on the wound rotor of the double output induction generator can be varied (amounts to controlling the rotor resistance) so that power output is controllable. The power factor of this

scheme is poor because lagging VARS are needed by both the machine stator and inverter.

The second technique also derives from the ac drives field. In this method the uncontrolled rectifier of the Kramer scheme is replaced with a fully controlled converter (cycloconverter). This is the static Scherbius system in which slip power flow is bi-directional. This has the advantage that operation is over both positive and negative values of slip (typically $\pm$50% of ω_s). Again, converter rating is less than the machine rating and is typically 50%.

2.3 Interconnection Considerations

It was stated above that wind turbines produce a very random output. Injection of such unpredictable power into a utility presents problems not encountered in the past. These include concerns of system stability, adequate levels of spinning reserve, and unloadable generation. Suppose an array of wind turbines (wind farm) having a total rating that is a significant fraction of system capacity is subjected to a large wind speed variation. This would be the case for example during a storm frontal passage. In [4] the authors consider various levels of wind turbine penetration on a utility and how the cycling of conventional generation (steam turbines) can be controlled. One technique calls for coordinated blade pitch control to reduce wind power variations over some interval (1 to 10 minutes). From this a methodology is developed for setting system spinning

reserve, and unloadable generation so that load following is not impaired. This is a very serious problem since wind speed during a storm passage may increase at a rate exceeding that of unloadable generation. By simplifying matters greatly this can be viewed as the case of many small time constant generators and a few large time constant generators supplying energy to a common load. What are the limits of stability of such an arrangement? This is typical of the questions arising when variable output alternate energy sources are interconnected with a utility.

Characterization of the wind has been done previously. In [5] it is shown that the two parameter Wiebull distribution gives a good fit to short-term wind velocity probability density. In addition to short-term behavior are the cyclic diurnal, seasonal, and annual trends. To adequately define these requires a long-term measurement pro gram. Stochastic modelling of the wind resource is then of great concern to the system planner in assessing reliability of his system with wind generation.

Further assessment of wind turbines of both constant speed and variable speed are given in [6,7,8,9]. The important effects on performance are several. Although there is no fuel cost, a large capital investment is needed per kW (this is partly due to the need to get the wind turbine rotor area off the ground to heights where the wind is). Below about 300m altitude, wind speed usually obeys a power law increasing with height. Towers are expensive, espe-

cially those sturdy enough to support a bulky rotor and generator. The generator output cannot be scheduled and, further, the power changes are fast. This is illustrated with field data records in [8]. Other than safety issues, the main interconnection concerns are of harmonics, VAR requirements, and power factor. The term power quality encompasses these concerns.

Measurements have been performed on distribution systems [10,11,12] to assess the power quality issue. In [10] the digital simulations of two distribution systems are compared with measurements to determine harmonic content and suggest methods to minimize harmonics. Large installations which generate substantial harmonic currents are power supplies for transit systems, dispersed storage and generation, motor speed controllers, and arc furnaces. The harmonics so generated are specified by frequency, magnitude, and phase angle. The sources can be either voltage or current depending upon commutation technique. That is, a line-commutated (commutation VARS supplied by the utility) inverter is a source of current harmonics. Similarly a force-commutated inverter is represented as a source of harmonic voltages behind an impedance. The arc furnace is modeled as a source of harmonic currents. The most prevalent being the third, fifth, seventh, and ninth. The fifth harmonic rises to 20% of the fundamental current during the melt down phase. It was further shown that the typical distribution system resonance (of low Q) is near the seventh

harmonic. An important finding was that the size and location of capacitor banks had a marked effect on harmonic voltage amplitude. Feeder location between the harmonic source and the capacitor bank appears to be the most sensitive arrangement. The main impact of the capacitor bank is a downward shift in system resonance. The KVAR and voltage rating of capacitor banks thus installed are critical since they are shunt paths for harmonic currents, $I_h=h\omega CV$ where h is the harmonic number. Filter VA rating must account for system harmonics.

One notable addition to the list of distribution system harmonic sources is the static var compensator (SVC). This is a utility size (MVA rated) phase controlled reactor. The SVC includes switched capacitor bank, reactor, and trap filters (series tuned) to hold harmonics below 5%. In operation the phase control of this reactor allows system voltage control by sinking or sourcing vars as needed to hold system voltage near nominal. It is also used near arc furnaces (25 to 150 MVA) and rolling mills for var support and minimization of voltage flicker. In EHV systems it provides line compensation. With frequency control the SVC provides damping of power oscillations.

2.4 Effect of Harmonics

What are the effects of these harmonics? This question can be answered in two parts. First, the effect on equipment and second, on control metering, and protection. In

the first case, high harmonic voltages and currents can cause failures of equipment, and produce high losses. Susceptible utility equipment includes capacitor banks as mentioned above, transformers, and switchgear. The most pronounced effect is overheating. In [13] the effect of system voltage harmonics on induction motors is investigated. It is found that for total harmonic distortion of the voltage wave (THDV) less than 5%, the increased Joule heating and subsequent temperature rise remains within specified limits. However, since voltage harmonics give rise to large current harmonics it is not known at what THDV level the life of induction motors will be significantly reduced.

Considering transformers [14,15], investigation indicates that the most severe performance degradation results from operation on an asymmetrical B-H curve. When harmonic order and phase is such that system voltage exceeds rated voltage, substantial odd-order harmonic currents are generated. Both system overvoltage and core asymmetry yield harmonic currents. Although the pulse burst modulation (PBM) technique described in [15] contains only low-order harmonics, radiated interference is negligible as is telephone interference. However, the production of even- order harmonic currents is detrimental to not only transformers but induction watthour meters [11].

Also, the current harmonics produced at different locations on the same network can reinforce each other in cer-

tain circumstances. In [16] this was shown to be the case for electric vehicle battery chargers. In three phase systems, the phases cannot be perfectly balanced so that even though the delta-connected transformer blocks triplen harmonics, the degree of imbalance determines how much positive and negative sequence third harmonics are passed. Of significance is the presence of a negative sequence fifth harmonic.

As for control and metering, the problems are similar: interference with carrier current systems, and ripple control systems must be minimized. It has been found that at 20% fifth harmonic, an electronic watt transducer was more than 10% in error. The problem with telephone interference is now more severe due to use of phone lines as a data transmission medium. In fact, the line current flowing in a distribution system is greater than that current required to deliver the real power of the connected loads. This extra current can be broken into two components. The first is a reactive component due to phase displacement and is at fundamental frequency. The second component, called the psophometric current, represents the distortion components, i.e., the harmonics. It is the psophometric component which interfers with communication and data channels. In [29] the telephone influence factor TIF and weighting function are explained.

Psophometric current is defined as that single frequency current which would cause the same interference on a

neighboring telephone circuit as does the actual harmonic containing line current.

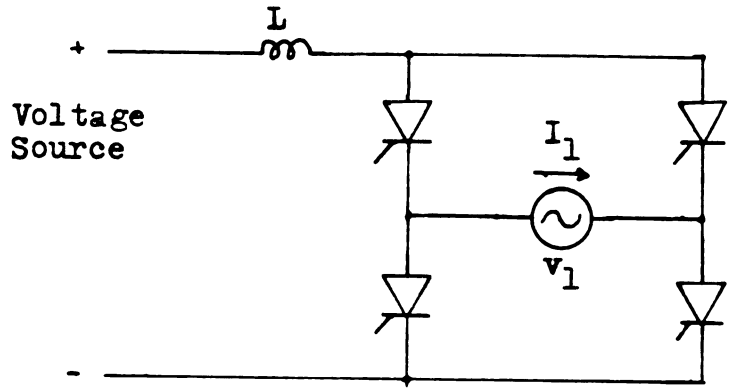
2.5 Classification of Converters

The above discussion gives several examples of why the power quality issue is so important--especially when large switching converters are tied to the utility. What are some of the converter circuits now in use and how is the harmonics problem corrected? First, all static converters can be grouped into two broad categories. The terms line-commutated and force-commutated refer to how the d-c port source current is transferred from one path in the inverter to an alternate path such that a reversal of current direction is achieved at the a-c port. The line-commutated (also source or natural) inverter can function only in a utility interconnected configuration. This is necessary with thyristor switching elements because the device can only turn off if its forward current is reduced to zero and held there for a short time. So, the utility must supply the volt-amperes to achieve this by producing an abrupt potential reversal across the thyristor. As a consequence the power factor as seen by the utility is always lagging. In the very early days of power conditioning, the converter harmonic behavior at both its d-c and a-c ports was found to be integrally related to the number of commutations per period of the base ac wave. It was observed that only even harmonics were present at the d-c port. Depending upon

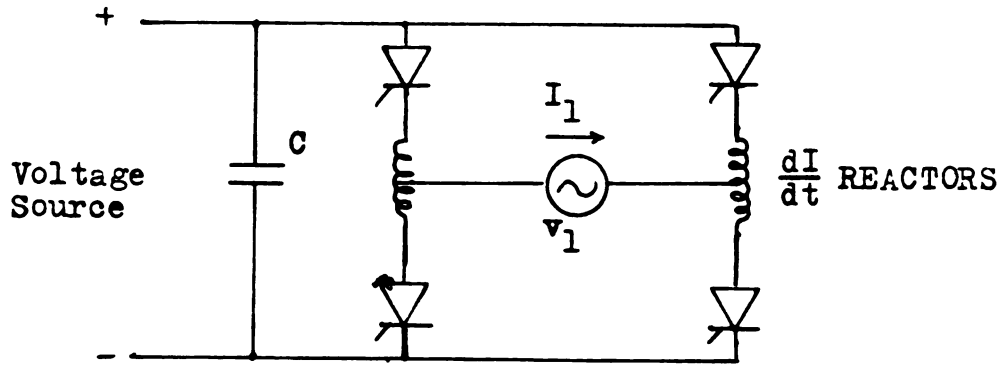
whether the converter input defined quantity is current or voltage determines which types of harmonics (dependent quantities) current or voltage are present. A current source inverter has current as the defined input and voltage harmonics are the dependent quantity at the d-c port. The converse holds for the voltage source inverter (Figure 2.1a and b).

The number of cycles of ripple in the d-c port dependent quantity per base ac wave period was termed the pulse number p. Thus, if h is the harmonic order and n any integer, the d-c port harmonics are given as $h=np$. At the a-c port only odd harmonics were found to be present with order given as $h=np\pm1$. In his book, Direct Current Transmission, Vol. 1, E.W. Kimbark gives an excellent discussion on the positive and negative sequence characteristics of these a-c port harmonics.

Force-commutated (also self or impulse) inverters can operate in a stand alone mode. As such they find application for powering static loads, e.g., an uninterrup tible power source (UPS). In this topology, the switching devices are capable of commutating the current independently of any utility interconnection. When thyristors are used as the main switching elements, auxiliary thyristors and passive commutating components are used to provide the commutation energy locally. The main advantage of this converter type is its control over power factor. Further examples of present converter topologies are to be found in [17,18].



a) Current Source Inverter CSI.



b) Voltage Source Inverter VSI.

Figure 2.1. Two basic converter types

Also presented are techniques of harmonic cancellation or neutralization and filtering.

Harmonic cancellation in use at the present is best illustrated by the vector addition method (stepped wave). In this approach multiple-phase-shifted (parallel connected on the d-c port; series connected at the a-c port) converter bridges using specialized magnetics sum the phase-shifted components of the output. The harmonic cancellation takes place in a specially-designed transformer which supports only the voltage harmonics. As was the case in capacitor bank, VA rating also applies here and the harmonic neutralization transformer rating is 40% of the total converter VA rating. The final vector summation is accomplished at the main utility interface or service transformer bank via wye-delta low side windings. Many variations are possible by paralleling more converters at appropriate phase angles in conjunction with more wye-delta transformer sets. Two significant drawbacks are attributed to this configuration. First, this series connection of transformers at the high side is not prudent at distribution and transmission voltages. Second, the VA rating penalty is high.

So far the discussion has centered on low frequency converters. The pulse numbers encountered in these methods are the paralleling of 6-pulse units for 12-pulse operation and tripling for 18-pulse. One theme keeps running through this--large magnetics and capacitors are needed. The magnetics are for both harmonic neutralization and in trans-

formers for voltage matching and isolation. Capacitors are used along with magnetics for compensation of power factor and in series tuned shunt filters to divert uncan celled harmonics from the utility. In recent years the trend is to higher speed switching devices and circuits which exploit them. This is possible because semiconductor devices are more economical than capacitors and magnetics.

2.6 The Trend to Higher Operating Frequency

Present research in power semiconductors is centered around improving ratings and switching characteristics--especially voltage withstand capability and switching times [19]. The power MOSFET is rapidly finding application in low-power lightweight converters. However, operation at high voltage is penalized by large on-state dissipation. Power bipolar transistors are taking over increasing proportions of the thyristor domain and gate-turn-off thyristors (GTO) are being improved in their turn-off capability. Present devices require a gate current pulse of a tenth to one fifth of the rated anode current. Their advantage lies in the fact that gate energy for turn off is much less than anode energy needed in classic auxiliary commutating methods. Recent power semiconductor devices are the static induction transistors--essentially a vertical junction FET. In power converter applications, a drawback arises from the normally ON characteristics of this device. Another recent development is the field controlled thyristor (FCT). This

FCT is a minority carrier device in which on-state resistance is very low. However, it is also a normally ON device.

The pulse width modulated (PWM) technique discussed in this thesis is one method whereby the high switching speed of power semiconductors can be used to achieve dc to ac conversion. The technique is based on principles of modulation theory to realize the translation of available power at zero frequency (dc) to some higher frequency (60 Hz). By using this method, the problems of harmonic filtering are reduced because the harmonics are now spaced about multiples of the carrier frequency. When bipolar power transistors are used, this frequency may now be several to perhaps twenty kilohertz. GTO's can achieve still higher powers (because of higher withstand voltage) up to two kilohertz and as high as six kilohertz at lower powers.

This PWM technique has been used in the photovoltaic area [20]. Here a single phase bridge topology was designed to interface between a 160V to 240V dc photo-voltaic (PV) array and a 240 Vrms utility at 6 KVA. The power output from PV arrays is predictable in areas with few cloudy days per year [8]. Inverter control in the PV appli cation is accomplished using ripple phase sensing to track the array peak power point. Tests on this particular PWM inverter, with a 19 mH series waveshaping filter to the utility, resulted in current harmonics that were less than 5%. A similar PWM inverter is described in [21] using power

bipolar transistors for a residential 8 kW rated PV inverter and a commercial 200 kW rated thyristor inverter.

In recent years a further refinement to the PWM technique has been explored. This is the concept of active waveshaping. As explained above, a passive filter is used to provide waveshaping. Reference [22] proposes that one method of achieving current waveshaping for an interconnected converter is by use of time-varying gains. In this approach, the dc input current to a parallel inverter (thyristor implementation called a parallel-capacitor-commutated inverter whose operation is described in [41]) is shaped into a half sinusoid. With such half sinusoids of current present in the link inductance, the current zero crossings must coincide exactly with that of the ac voltage wave. Thus a very strict requirement of unity power factor operation is imposed. Actual power distribution systems are inductive so that achieving exact current zero-voltage zero coincidence will be difficult.

The control of the link inductor current is accomplished using a buck converter with time varying feedback gains. These gains not only vary at the 60 Hz line frequency rate but their magnitude is a function of the injected current level. This converter was built and tested on a simulator. Control problems encountered were due to an open loop pole at the origin and a right hand plane zero in both the inductor current and filter capacitor voltage state equations. The action of time varying gains causes the closed loop

poles to move so that system response is time varying and load dependent. Because of this amplitude modulation of the input current, the d-c source will be subjected to a high second harmonic. This itself may present interface problems depending upon the source used.

A further refinement of this technique is to use a high-frequency link. A photovoltaic application of this is given in [23]. The scheme developed is a three-stage conversion process. In the first stage, high power bipolar transistors follow a PWM switching function at 10 to 20 KHz. The output of this PWM single-phase bridge is coupled through a high-frequency ferrite-core transformer to a rectifier bridge using fast recovery diodes. The PWM shaped current at the bridge output again is used to feed a d-c link inductor. The inductor further filters the current into half sinusoids. The final stage is a conventional thyristor bridge connected directly to the utility. The PWM stage is controlled such that the shaped current has a natural zero just prior to the voltage wave zero crossing. In this manner thyristor commutation is built in (classified as line-commutated, although the current is artificially quenched). This conceptual design was tested using a computer simulation.

Because the current is shaped to a half-sinusoid at the PV array interface, a large input capacitor is needed to source the 10 to 20 KHz current pulses. The array current is again pulsating at 120 Hz.

2.7 The Multistage Concept

Most recently a further refinement to this concept has been proposed and built [24]. In this paper, the authors describe a photovoltaic dc-ac inversion process using the multiple converter topology. Their approach is to use a double forward converter (parallel buck/boost) realized using power MOSFET transistors. This stage has its duty ratio modulated in response to a half-sinusoid current or voltage reference signal. By phase locking to either the utility or an internal clock, either interconnected (current reference) or stand-alone (voltage reference) operation is possible. The system operation is similar to the previous references when current programmed. When voltage programmed it has many aspects presented in this thesis.

As the above sequence of papers illustrates, the conversion of power from renewable energy sources requires the multi-stage converter concept. The research results presented here commenced at the time (1981) reference [22] was being presented. During the intervening time research of this multistage concept using wind turbine output as its power source has not been published.

For the case of wind energy, the source is not as predictable as from a PV array. Thus, the strategy to shape current would be considerably different because, with wind energy, the generator current is a random process. By taking into account other constraints of highly variable power throughput, the need to manage reactive power flow,

and to minimize pulse loading of the energy resource, a different topology was needed. The topology chosen is that of an input switching regulator (boost converter) with continuous input current and constant output voltage. Therefore, a dc voltage link is used in place of the aforementioned current link. It is now the line-interfaced stage that is switched at a high frequency rate (PWM) to achieve inversion to ac. Filtering is then used for current waveshaping at the utility interface. By controlling the inverter phase lead angle, power throughput can be varied. Then by a judicious setting of the regulated voltage, a minimum var flow can be realized. This topology meets the three requirements on power, vars, and waveform set forth previously.

What remains is the control of this cascade configuration. In [25] a description of two different means of generating PWM switching functions are presented using a microprocessor. One technique is to continuously solve an algorithm for each switching angle given a voltage magnitude of the fundamental desired. The second technique is to precompute all the necessary angles and store them (only those for a quarter wave due to symmetry) in a look up table. This second technique is the programmed waveform technique and operates in real time. Either technique is capable of nearly eliminating harmonics up to any desired order [31,32,33,34].

The boost converter topology operates as a regulator of the random source input. Its function permits the input d-c voltage to vary through a wide range while stablizing the output voltage at a set level. When a load is connected at this regulator output which has large excursions in its current demand, i.e., the PWM inverter, it is found that conventional output feedback fails to stabilize the regulator. Others [26,27,28] have investigated similar behavior in switching converters of the buck-boost type. In the technique of current-injected control, the output current is sensed and fed back. This technique has a serious disadvantage in that the converter becomes unstable for duty ratio D greater than 50%.

After experimental investigation of various control laws, a unique control strategy emerged which is very robust as a stabilizer. Chapter 5 describes its analysis in detail. Essentially the method consists of sensing the regulator input current and processing out all high frequency components due to switching. This function is then summed with the converter high frequency ramp function and compared with a processed sample of the output voltage. The duty ratio obtained is a function of both input current and regulated voltage. High dc gains are now possible so that deviations in the regulated voltage can be kept low. Furthermore, the range of duty ratio is limited only by fundamental loss mechanisms--not by the controller.

CHAPTER III

STATIC CONVERTER THEORY

3.1 Generalized Converter Theory

In Chapter 2 switching converter schemes were classified. This chapter establishes the fundamental principles upon which all bridge-type converters operate. In general an arbitrary number of sources and loads can be interconnected via a generalized switching matrix. This is a two dimensional schematic giving all possible ways of connecting M-sources to N-loads. By proper connections at the nodes through switches, the M-sources can generate at the N-loads wave-waveforms of a predetermined character. In his book [37] Wood denotes the input and output port variables as "defined" and "dependent" quantities. This terminology will be used here because it is descriptive of actual converter behavior.

Consider the switching matrix shown in Fig. 3-1. In this figure any of the M-input voltage sources V_s can be connected through an appropriate switch to any of the N-output lines. The M-independent voltage sources are the defined quantities supplying dependent currents $I_{d1},\ldots,I_{dM}$. At the output port the N-defined current sources must be supplied by the M-dependent source currents. Naturally, the

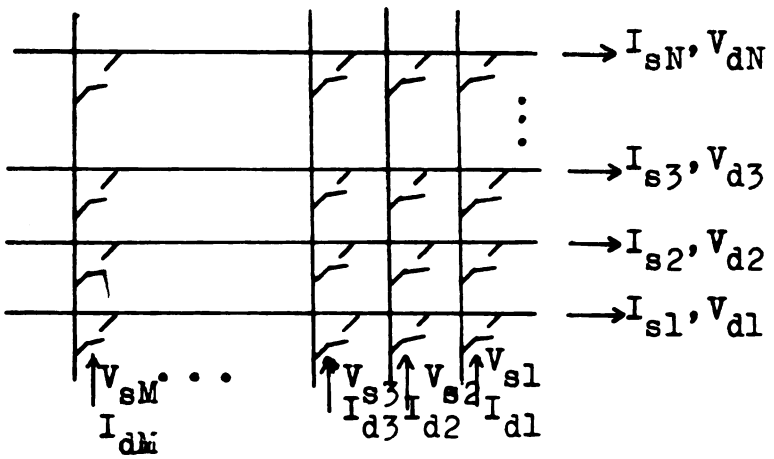


Fig. 3-1. Generalized switching matrix for a defined input voltage set.

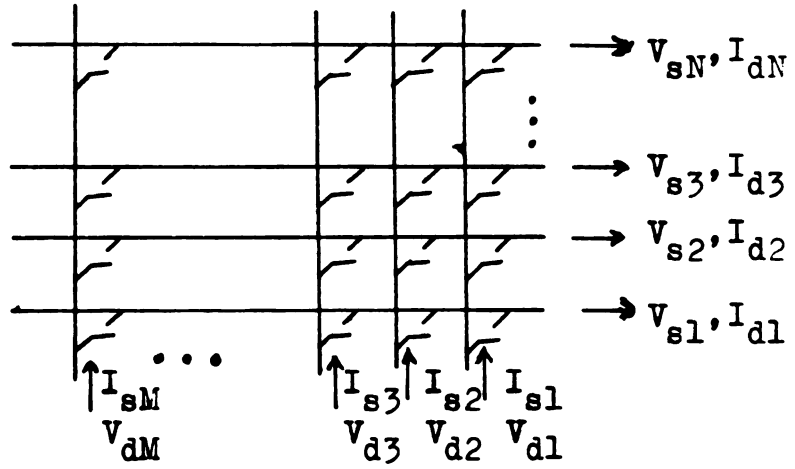


Fig. 3-2. Generalized switching matrix for a defined input current set.

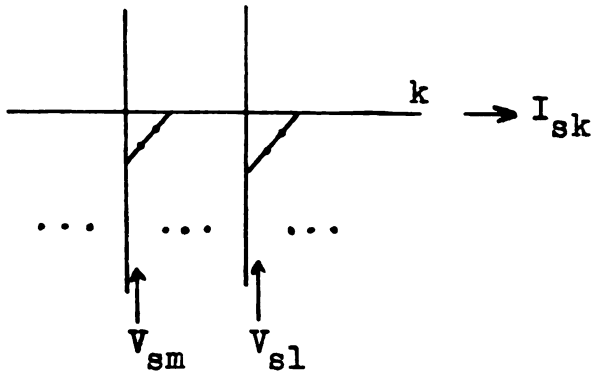


Fig. 3-3. Possibility of circulating current.

V-I characteristics of the load will dictate the dependent voltages $V_{d1},\ldots,V_{dN}$ response to these N-defined currents I_{s1} to I_{sN}. It can be shown that if all quantities are replaced by their exact electrical dual--voltages with currents, parallel with series, single polarity voltage with unidirectional current--a dual network will be constructed. Note that since the fundamental quantities are voltages and currents, there can be no third dimension to the generalized switching matrix. When duality is applied to the network in Fig. 3-1, Fig. 3-2 results. In Fig. 3-2 the M-defined current sources drive the N-defined voltages. In Chapter 4 the necessary switch realizations are given.

From circuit theory it is known that in any electrical network, the voltages and currents must conform with Kirchhoff's voltage and current laws, KVL and KCL. Application of Kirchhoff's voltage law KVL, and current law KCL to Figure 3.1 results in the following two constraints:

- Along any input (output) line one or more switches must be ON. If this condition is not satisfied, KCL will not be valid at the output (input) port because a defined current source requires a return path.
- Along any output (input) line at most one switch can be ON. Disregarding this condition results in violation of KVL at the input (output) port.

Here terms in brackets apply to the dual circuit Figure 3.2. For example, suppose all the switches are open or OFF. Define an ON switch as a logical 1 and an OFF switch as a

logical 0. With this definition the KVL description of Figure 3.1 becomes:

$$\begin{bmatrix} V_{d1} \\ V_{d2} \\ \vdots \\ V_{dN} \end{bmatrix} = \begin{bmatrix} & H & \end{bmatrix} \begin{bmatrix} V_{s1} \\ V_{s2} \\ \vdots \\ V_{sM} \end{bmatrix} \quad ; \quad \underline{V}_d = \underline{H}\,\underline{V}_s \qquad (3.1)$$

where $\underline{H}$ is an NXM matrix, $\underline{V}_d$ the Nxl dependent voltage column vector, and $\underline{V}_s$ the Mxl defined source voltage vector. Similarly the KCL description of Figure 3.1 is:

$$\begin{bmatrix} I_{d1} \\ I_{d2} \\ \vdots \\ I_{dM} \end{bmatrix} = \begin{bmatrix} & P & \end{bmatrix} \begin{bmatrix} I_{s1} \\ I_{s2} \\ \vdots \\ I_{sN} \end{bmatrix} \quad ; \quad \underline{I}_d = \underline{P}\,\underline{I}_s \qquad (3.2)$$

where $\underline{P}$ is an MXN matrix, and $\underline{I}_d$, $\underline{I}_s$ are column vectors. In order to satisfy the above constraints, $\underline{P} = \underline{H}^T$. Clearly if $\underline{H} = [0]$ and if the defined current sources are non-zero, then KCL is violated because all of the dependent currents $\underline{I}_d$ must also be non-zero. Hence $\underline{H}$ must have at least one 1 in each column. The second condition is similar. Suppose along output line k the switches to both input lines ℓ and m are closed, Figure 3.3. Because the attributes (magnitude, phase) of these defined voltage sources $V_{s\ell}$ and V_{sm} are not identical, a circulating current I_{cr} can flow. KVL is indeed violated at the input port in this case. Thus, there

can be, at most, one 1 in each row of matrix H in Figure 3.1.

The notation of [37] will be used in which $\underline{H}$ represents the matrix of existence functions for the node switches in the generalized switching matrix. Define the switch existence function as a unit amplitude pulse with period 2π and duty ratio D, ($D \leq 1$). Each existence function in H can be expanded in a Fourier series as

$$h_{ij} = D_{ij} + \frac{2}{\pi} \sum_{n=1}^{\infty} \left(\frac{\sin n\pi D_{ij}}{n} \right) \cos[n(\omega t - \psi_{ij})] \qquad (3.3)$$

when the time axis is symmetrically located on the existence function with $\psi = 0$.

The existence function for different values of duty ratio D can be approximated using a complete set of discrete Walsh functions. In this case equation 3.3 would consist of the summation of weighted Walsh functions orthogonal over the fundamental period $2\pi/\omega$. The Fourier representation has been chosen instead because of its utility in developing expressions for harmonic content. Section 3.3 outlines other valid techniques.

In a completely generalized converter, it is possible to generate at the output port defined quantities of arbitrary waveshape and frequency--strictly dependent on the switching pattern defined by $\underline{H}$. Thus $\underline{H}$ can define switching patterns that represent constant frequency of the

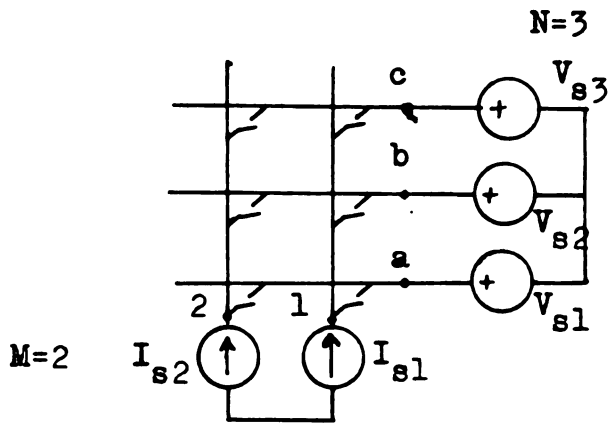
output quantities or variable frequency as desired. This property is exploited as described in Chapter 2 where either constant frequency operation, necessary in a utility interconnected mode, or variable frequency, as for instance in variable speed motor drives, are required of the inverter. We can see that $\underline{H}$ is unique during any switching interval and, for operation from periodic sources with period T_s, an integer number of switching intervals are concatenated into period T_s. Since the switching function matrix $\underline{H}$ defines the circuit topology during any subinterval of T_s, then the resulting currents exhibit the character of each such topology, drive, and loading conditions. When these currents persist from one subinterval on to the next, the circuit is in the continuous conduction mode. Conduction here refers to the presence of a non-zero switch current. On the other hand, when external conditions and circuit dynamics are such that if any of these currents go to zero within a subinterval of T_s, the circuit enters a discontinuous conduction mode.

Example 3.1: To the switching matrix of Figure 3.2, connect a pair of defined dc current sources I_{s1} and I_{s2} with $I_{s2} = -I_{s1}$. This gives M=2. For inversion into an ac defined voltage source N=2,3,... where N=2 defines a single phase configuration, and N=3 a three phase configuration and so on. Notice that where N=2, the pair of ac defined voltage sources have the same phase and frequency. In this case both may be combined into a single voltage source. The

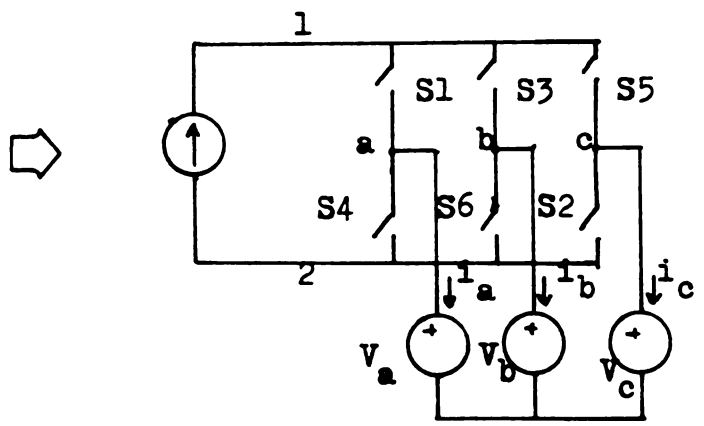
result is then a single phase bridge configuration. Should a neutral connection exist in Figures 3.1 or 3.2, a class of converters termed midpoint converters results.

Let N=3 in this example and refer to Figure 3.4. Using the relations given, Figure 3.4a can be redrawn as shown in Figure 3.4b. With the switches numbered as in Figure 3.4b, we first verify the switching matrix constraints. The requirement that along any input line at most one switch can be on, means that only one of switches s_1, s_3, s_5 and one of s_2, s_4, s_6 can be on. If two switches are on in either of these triples, it is easy to verify that the corresponding defined voltage sources are shorted resulting in excessive circulating current.

The remaining constraint requires that of switch pairs (s_1,s_4), (s_3,s_6), (s_5,s_2) one switch must be on in two of these pairs. To have none on clearly violates KCL at the input port. Furthermore, the case where both switches in a pair are allowed to be on without violating circuit theory will be inadmissable based on the desire to achieve power transfer from the dc to the ac sources. Thus, to simultaneously satisfy the two network constraints and the one constraint on power transport <u>through</u> the switching matrix reduces the choice of admissable switch pairs to s_1 and s_2 or s_6, s_3 and s_2 or s_4, s_5 and s_4 or s_6. A useful mnemonic aid for switching sequence labeling is to repeat output lines a and b as shown in Figure 3.4b and label the switch



a) $I_{s1} = -I_{s2} = I_s$



b)

Let $V_{s1} = V_a$, $V_{s2} = V_6$, $V_{s3} = V_c$

Figure 3.4. DC to AC Current Source Inverter (CSI)

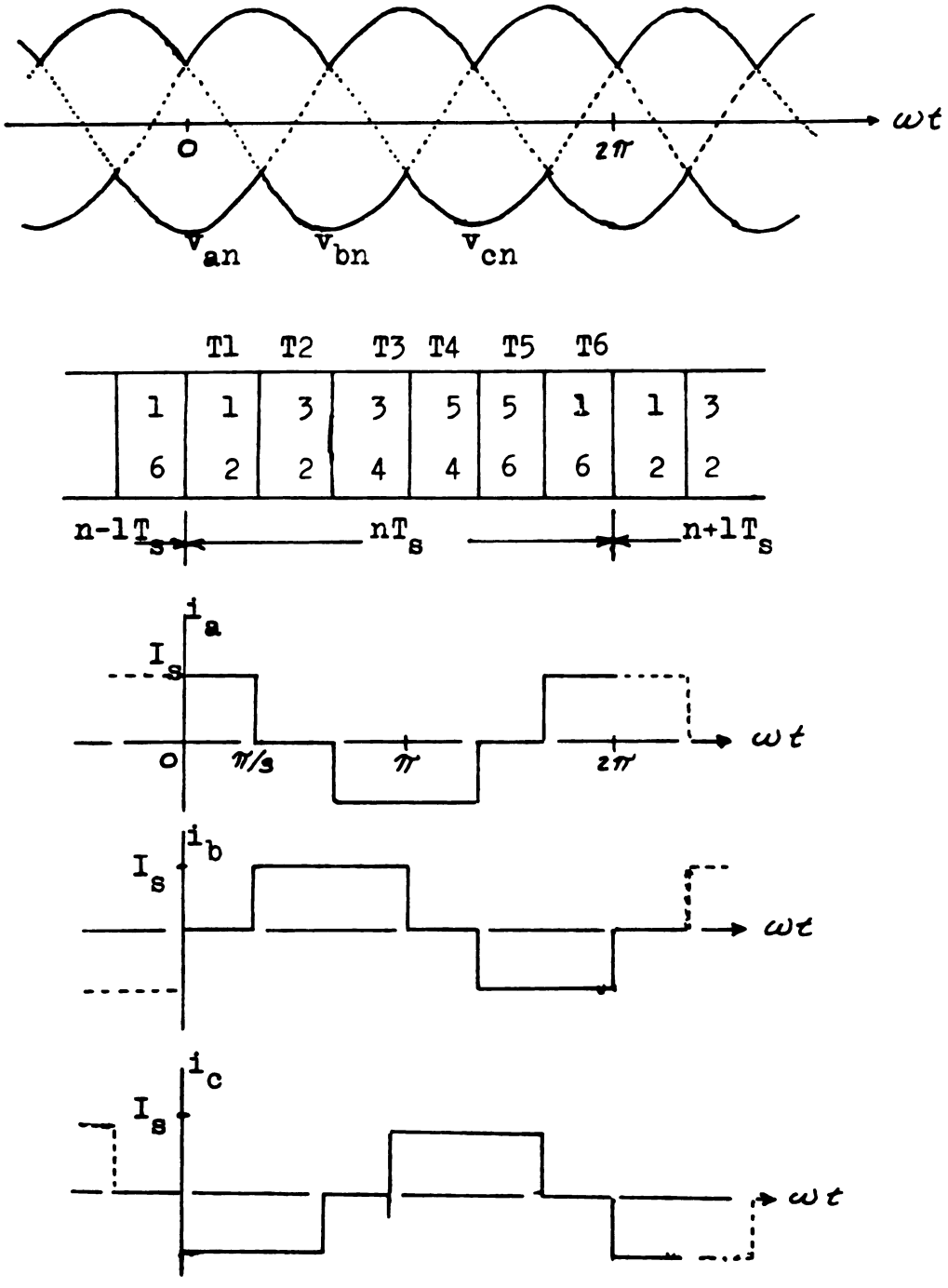


Figure 3.5. CSI converter defined voltages and dependent currents.

operations in sequence along the diagonals a-c, b-a, c-b, in an upper left to lower right fashion.

Referring to Figure 3.5 the circuit operation is as follows. Let the switch closings occur when the corresponding pole voltage phase is π radians. In figure 3.4b a pole is defined as the switch pair across the input port 1-2, e.g., (s_1, s_4), (s_3, s_6), and (s_5, s_2). By delaying the switch closings π radians the converter will operate at full inversion so that power is transferred from I_s to each of the three defined voltage sources V_{abc}. The negative of these pole voltages are shown dotted in Figure 3.5a. The solid curves define the dependent voltage V_{1-2} at the input port (note that the lower envelope is folded onto the top envelope to yield 6 pulse ripple at the dc port). In Figure 3.5b the switch pairs are given during each of the six subintervals of switching period nTs. By assigning a logic 1 to each location where a given switch is on yields the existence function matrix for each subinterval. Application of equation 3.2 yields:

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 \\ -1 \end{bmatrix} I_s \quad ; \quad I_d = H^T I_s \; ; \; t \epsilon T1 \qquad (3.4)$$

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 \\ -1 \end{bmatrix} I_s \; ; \quad t \epsilon T2$$

$$\vdots \qquad\qquad\qquad\qquad \vdots$$

$$t \epsilon T_N$$

where matrix $\underline{H}^T$ is different from one subinterval to the next in that two rows are exchanged. Figure 3.5c shows the resulting phase currents for the a and b phase. In this example current flows in 120 degree blocks so that the duty ratio D = $1/3$. Substituting this value into equation 3.3, then writing the expression for phase current i_a of Figure 3.5c results in

$$i_a(t) = \left(\frac{1}{6}+\frac{1}{\pi}\sin\frac{\pi}{6}\cos[\omega t-\frac{\pi}{6}]\right)I_s-\left(\frac{1}{3}+\frac{2}{\pi}\sin\frac{\pi}{3}\cos[\omega t-\pi]\right)\times \tag{3.5}$$

$$I_s+\left(\frac{1}{6}+\frac{1}{\pi}\sin\frac{\pi}{6}\cos[\omega t-\frac{11\pi}{6}]\right)I_s+\sum_{n=3}^{\infty}I_n\cos n\omega t$$

where the summation indexed by n defines the current harmonics. No even harmonics are present due to waveform odd symmetry. Combining terms in equation 3.5

$$i_a(t) = \frac{3\sqrt{3}}{2\pi}I_s\cos\omega t+\sum_{n=3}^{\infty}I_n\cos n\omega t \tag{3.6}$$

similarily for the phase b and c currents.

$$i_b(t) = \frac{3\sqrt{3}}{2\pi}I_s\cos\left(\omega t-\frac{2\pi}{3}\right)+\sum_{n=3}^{\infty}I_n\cos[n(\omega t-\frac{2\pi}{3})] \tag{3.7}$$

$$i_c(t) = \frac{3\sqrt{3}}{2\pi}I_s\cos\left(\omega t+\frac{2\pi}{3}\right)+\sum_{n=3}^{\infty}I_n\cos[n(\omega t+\frac{2\pi}{3})]$$

The defined voltage sources are assumed to have no harmonic components, i.e.,

$$\upsilon_{an}(t) = V_m \cos \omega t$$
$$\upsilon_{bn}(t) = V_m \cos (\omega t - 2\pi/3) \qquad (3.8)$$
$$\upsilon_{cn}(t) = V_m \cos (\omega t + 2\pi/3)$$

The power delivered to these defined sources can be computed as the product of equations 3.6 and 3.7 with 3.8. To emphasize the delivery of real power, the higher order current terms are neglected. Since switch s1 is closed when $\upsilon_{an}(t)$ is at π radians the power delivered to this source is:

$$p_a(t) = \upsilon_{an}(t) i_a(t) = V_m I_s \frac{3\sqrt{3}}{2\pi} \cos \omega t \cos(\omega t - \pi) \qquad (3.9)$$

$$= -V_m I_s \frac{3\sqrt{3}}{4\pi} - V_m I_s \frac{3\sqrt{3}}{4\pi} \cos 2\omega t$$

and for the b and c phases the result is the same as equation 3.9 with the addition of the respective phase angle. The total three phase fundamental power is then $3p_a(t)$. The double frequency terms vanish in the total power expression so that power is constant.

$$p(t) = -V_m I_s \frac{9\sqrt{3}}{4\pi} \qquad (3.10)$$

Equation 3.9 shows that the instantaneous power delivered by the defined source $\upsilon_a(t)$ is negative. Therefore, $\upsilon_a(t)$ absorbs power. This same result applies to the complete voltage source set. If the current harmonic terms had been retained, the expression 3.10 would contain a summation term of voltage and current cross products. These higher order

terms will contain no real power and represent distortion voltamperes. This example is for the specific case of the switch closings delayed by $\alpha = \pi$ radians from the corresponding voltage wave zero crossing. Figure 3.6 illustrates the ac line current and voltage. The following defining relations are used:

$$v_{ab}(t) = v_{an}(t) - v_{bn}(t)$$

$$i_{ab}(t) = i_a(t) - i_b(t) \qquad (3.11)$$

This example serves to demonstrate how sequential switching achieves inversion from a defined dc source into a defined ac source. The dependent current at the ac port approximates a sinusoid (fundamental component of the stepped wave line current). The extent to which the step approximation deviates from a sinusoid determines the harmonic content. From Figure 3.5a the presence of ripple components on the dc port dependent voltage means that the input power contains harmonics. No energy storage occurs within the switching matrix. Therefore harmonics must be present in the ac port power.

Minimizing harmonic content of converters is necessary. A notable technique is vector summation in which the step size of the current waveform shown in Figure 3.6 is reduced. In general 1-converters of the type described in example 3.1 may be combined. If the switching patterns applied to each converter are delayed by $2\pi/\ell.p$, the number of such current steps will be increased to $\ell.p$ where p is the base converter

pulse number. For example, if $\ell = 2$ a twelve pulse converter results in which the second converter switching functions are identical with the first but delayed by $\pi/6$.

This technique requires replication of converters and many switches are needed. Twelve pulse converters represent the economical and practical limit at very high power [44,45]. This is due to the limitations of realizable switch elements. Chapter 4 will introduce devices currently available for this application.

The effect of switching function timing in relation to the defined ac quantity is needed. In the specific example treated here, the phase delay angle α was π radians. Referring once more to Figure 3.5a, if α is less than π, the solid envelope will shift left along the dotted curves and discontinuties will appear in the envelope wave. As α is delayed to $\pi/2$, these discontinuties will have maximum amplitude and, further, will be symmetrical with the ωt-axis. Consequently, since dc source power is the product of I_s (constant) and this voltage envelope, the result averages to zero. The dc side and ac side harmonics are maximum. As α is delayed into the range $\pi/2$ to 0 the effect is the mirror of that just described.

3.2. Assessment of Present Single Phase Conversion Methods

The conversion of dc to ac can be achieved using either of the switching matrices of Figures 3.1 or 3.2. The converter of Figure 3.1 is a voltage source inverter VSI and

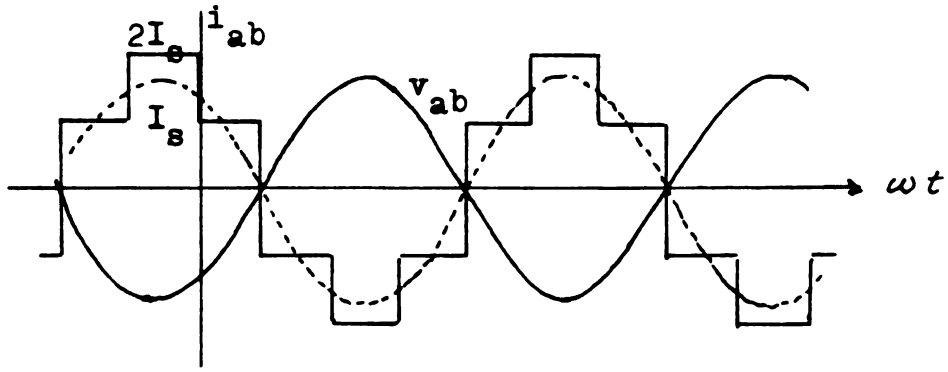
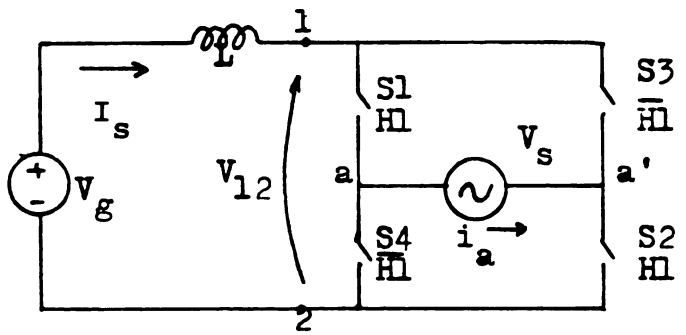
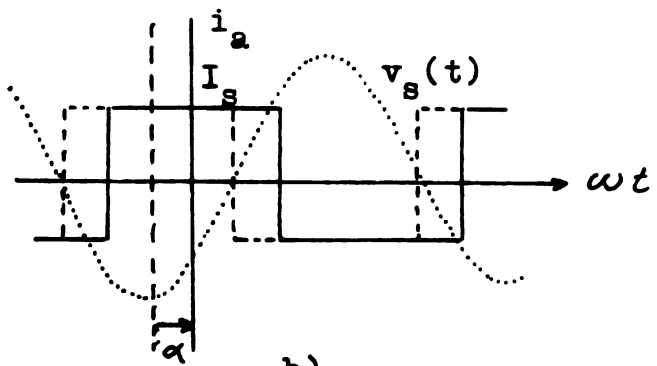


Figure 3.6. Converter line to line voltage and current.



a)



b)

Figure 3.7. Single phase CSI a) topology and b) waveforms

that shown in Figure 3.2 is a current source inverter CSI. When used in the conversion of electricity produced by wind driven generators each scheme has its advantages. In this section both the CSI and VSI converter are analyzed in the ideal case. Appendix A extends this ideal analysis by considering some practical limitations. Measurement results are presented there.

The single phase CSI converter is obtained by removing one pole from the circuit of Figure 3.4b. Because generators are voltage sources, an interface element gives the appearance of a current source to the converter. If the value of L is sufficiently large, the current I_s will be continuous. As the value of L approaches infinity the current I_s is smooth dc. Figure 3.7 outlines this circuit. If the assumption is made that L is infinite, then over any complete period of the ac voltage, the average volt-seconds accumulated by L must be zero. The utility is represented as an ideal voltage source $v_s(t)$. Its impedance is negligible relative to that of inductance L.

The switches labeled s_1, s_2, s_3 and s_4 are unidirectional current carrying and bidirectional voltage blocking. They are realized in practice using conventional silicon controlled rectifiers (SCR's). With regard to the constraints imposed in example 3.1, the dependent current $i_a(t)$ is:

$$i_a(t) = M_1 I_s - \bar{M}_1 I_s \quad ; \; \bar{n}-1 \; T_s \leq t < nT_s \tag{3.12}$$

where H_1 is the existence function of switches s_1 and s_2. The function $\bar{H}_1 = 1-H_1$ is the complement of H_1. By substituting equation 3.3 for H_1 with $D_{ij}=D_1=1/2$ and $\Psi=0$ yields:

$$i_a(t) = I_s\left[0+\frac{4}{\pi}\sum_{n=1}^{\infty}\left(\frac{\sin\frac{n\pi}{2}}{n}\right)\cos n\omega t\right]$$
$$= \frac{4I_s}{\pi}\sum_{n=1}^{\infty}\frac{1}{n}\cos n\omega t \quad ; \quad n=1,3,5,\ldots \tag{3.13}$$

Equation 3.13 shows that, in addition to the fundamental component of current with magnitude $4\ I_s/\pi$, are all odd harmonics with amplitude decreasing at 6dB/octave. The significance of this is that low order <u>current</u> harmonics are injected into the utility.

In cases where the inverter rating is a significant fraction of the utility short circuit capacity, these harmonic currents can cause voltage-wave distortion. If so, there is the potential for damage to sensitive line connected loads such as relays, circuit breakers, motors [13] etc. One finding has been that total harmonic distortion of the voltage wave (THDV) in excess of 5% does affect the operating temperature of induction motors. Others have found that THDV exceeding 8.7% causes fuse blowing in harmonic cancellation filter banks in shunt with the utility network.

Suppose the switching sequence is delayed an angle less than π in Figure 3.7. Then the expression for instantaneous power can be obtained.

$$i_a(t) = \frac{4I_s}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} \cos[n(\omega t-\alpha)]$$

$$v_s(t) = v_{aa'}(t) = V_m \cos \omega t$$

$$p(t) = i_a(t)v_s(t) = \frac{4V_m I_s}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} \cos[n(\omega t-\alpha)]\cos \omega t \qquad (3.14)$$

The fundamental (n=1) average power defined as the definite integral of p(t) over one period is:

$$P = \frac{2V_m I_s}{\pi} \cos \alpha \quad ; \quad \frac{\pi}{2} \leq \alpha < \pi \qquad (3.15)$$

By convention the quadrature power or reactive volt-amperes present due to displacement angle α is given as:

$$Q \triangleq \frac{2V_m I_s}{\pi} \sin \alpha \quad ; \quad \frac{\pi}{2} \leq \alpha < \pi \qquad (3.16)$$

Examination of both equations 3.15 and 3.16 reveals that over the given range of α the real power P is negative (into the utility) and Q is always positive. The remaining cross product terms present in p(t) of equation 3.12 for n=3,5,... represent the distortion voltamperes.

A discussion of the VSI converter is outlined in Appendix B for the single phase case. A review of the VSI performance confirms the duality of these two techniques. The CSI circuit delivers a square wave of current into the

ac source under ideal conditions and hence is a source of current harmonics. The VSI circuit generates a square wave of voltage in the ideal case and therefore represents a source of voltage harmonics. With practical sources these converters suffer a further reduction in performance. The defined source waveshapes become truncated versions of the ideal situation and system dynamics limit rise and fall times so that infinite dI/dt in the CSI and infinite dV/dt in the VSI are not possible. However, because the defined source waveshape takes on the characteristics of a pulse the harmonic content increases significantly. Other researchers have studied the consequences of this discontinuous behavior.

In [3] the effects of discontinuous current loading of fuel cells and photovoltaic arrays are described. Such current pulses also cause torque pulsations in a wind turbine generator. The secondary effects of current pulsations are harmonic interference in nearby electronic equipment, telephone, and power line carrier control.

Different applications have resulted in the development of other topologies. The area of induction heating [40] describes several.

3.3. Analytical Techniques

At present the methods used for converter analysis are application dependent. Section 3.1 introduces a basic generalized theory. This approach relies on the assumption

of ideal switches and sources. It does have capability, as demonstrated in Section 3.2, to define the various components of the instantaneous power. This makes it very useful to develop expressions for the harmonic content of a given variable. It is due to the nonlinear nature of switching circuits that no one analytical method serves in all applications.

Some of the more useful techniques are presented in [30] and include both time and frequency domain methods. A brief survey of these methods will be presented here. The Laplace transform of converter differential equations during each subinterval of operation gives the exact nature of the dependent waveforms. As the converter complexity increases this method becomes impractical. The Fourier series representation of defined quantities is another such method. As presented above, this technique uses superposition to derive the response of any selected dependent quantity. State space methods can be applied. This technique is used along with the Fourier method in this thesis. Under appropriate conditions the state space behavior during each of several subintervals can be weighted together to obtain an averaged response. This technique of state space averaging [3%] assumes transition of state between subintervals can be approximated as straight line. As such, it is very useful in predicting the low frequency behavior of switching converters.

The methods of complex variables have proved especially useful in the analysis of rotary converter. The direct, quadrature, and stationary d-q transformation used to simplify the analysis of induction and synchronous machines is one example. The use of an orthogonal set of discontinuous functions, e.g., step, ramp, have been used to develop expressions for the current waveform in an inductor-converter. The inductor is the superconducting magnetic energy store (SMES) reservoir. The discrete nature of converters makes analysis by sampling techniques feasible. In particular, the Z-transform. In [28] this method is explored and applied to a current programmed converter. The theory is extended into that of discrete modeling. It is shown that since fewer approximations are required than for state-space averaging, results are valid on dynamics up to the switching frequency.

The category of computer simulation includes analog, digital and hybrid. Analog simulation is useful because the circuit does not have to be constructed. Also, parameter variation is easily accommodated. Digital simulation using SPICE, and CSMP is fast but the algorithms are expensive. A program such as CSMP solves the converter differential equations during each switching subinterval. In converters switching at high frequency it will take considerable simulation time to assess any low frequency behavior. The conclusion of this survey of analysis methods is that no universal technique exists.

CHAPTER IV

POWER ELECTRONIC TECHNIQUES

4.1. The Pulse Width Modulation (PWM) Method

The previous chapters have shown how a switching circuit can generate a stepped or staircase approximation to a sinusoidal current waveform. The approximation is good and with add-on tuned filters, the remaining harmonic levels will satisfy the specification in [29]. The connection of several identical phase-displaced converters requires a large number of switching devices--all operating at the frequency of the a-c system to which the converter is connected. The next step is to generate this same frequency with fewer switching elements. This is possible with high speed devices operating at higher speeds.

Recall from Chapter 3 that a converter produced a square wave of some dependent quantity. The low order harmonics present in this square wave can be reduced by selectively notching portions of this waveform. This technique is called conduction-angle modulation (CAM) and is an accepted method of harmonic neutralization. By incorporating enough notches, any desired number of low-order harmonics can be eliminated. This approach is attractive because low pass filtering becomes more efficient at higher

frequencies. The continued extension of the CAM concept yields a PWM waveform. PWM is based on modulation theory and the natural sampling method of encoding the d-c source voltage into a sinusoidal 60 Hz line voltage wave. In [39] natural sampling is defined as the modulation of the width of a periodic pulse train in proportion to some modulating message wave. In natural sampling, both the pulse leading and trailing edges are so modulated. Here the message wave is the desired 60 Hz line frequency of sinusoidal waveshape. By generating a high frequency triangular carrier wave (which has been phase locked to the utility line), and then sampling the message waveform, a PWM signal results. In practice both the sinusoidal message wave and the high frequency triangular wave are input to an electronic comparator. The comparator switches states when the isosceles triangle carrier intersects the message wave. In this manner the pulse width of individual pulses is made to vary. Figures 4.1 and 4.2 depict the natural sampling result obtained using the circuit constructed from Figure 4.3. In Figure 4.2 the PWM pulse is at a logic high level for a time interval equal to the time the modulating wave exceeds the triangular carrier wave. Refer to Appendix C for a definition of the functional blocks shown in Figure 4.3. Modulation depth K is defined as the ratio of modulating wave to carrier wave.

$$K \triangleq \frac{\nu_m(t)}{\nu_c(t)} \quad ; \quad 0 < K \leq 1 \tag{4.1}$$

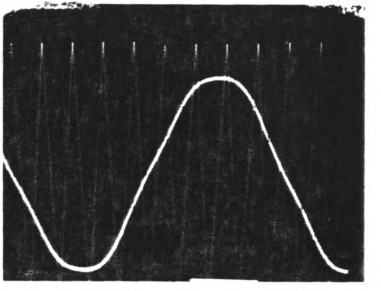


Figure 4.1. Natural sampling of sinewave with P=9.

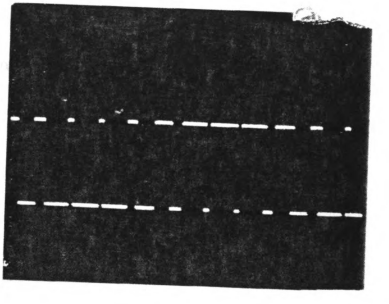


Figure 4.2. Resulting PWM wave with P=9 and K=.75.

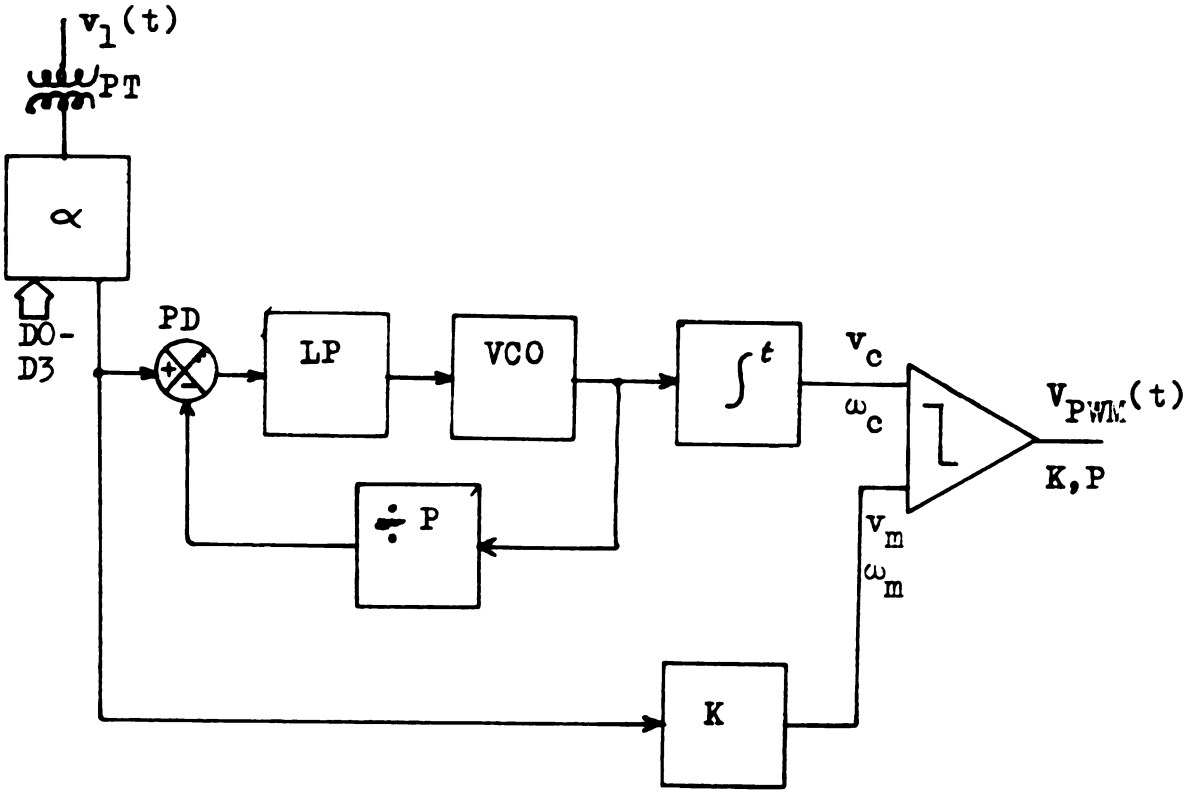


Figure 4.3. Functional diagram for natural sampling.

For $0 < K < 1$, the modulating signal can be recovered from the modulation process. For the case $K > 1$, the PWM wave tends toward a square wave. Some research has centered on this range of K. In the area of variable speed a-c drives, the harmonic degradation for K slightly greater than one is acceptable. This is not the case when current is supplied to the line.

The second characteristic of PWM determined by the circuit of Figure 4.3 is the switching to line frequency ratio P.

$$P \triangleq \omega_c/\omega_m \qquad P > 1 \tag{4.2}$$

In this work P is constrained to integer values greater than 1. A suitable choice for P depends upon the particular choice of switching devices. A high ratio (P) yields minimum weight filters, but efficiency will fall because of the large number of commutations per cycle required of the devices. A low value for P gives improved switching efficiency but larger investment in the low pass filter. This research investigated P from 5 to 30. One significant finding is that for odd integer ratios, the phase locked loop (PLL) would lock to the line frequency with an odd number of cycles in one half cycle and an even number in the other half cycle. It will be shown later in this chapter that transformer design is very critical for a PWM waveform, especially the tendency to asymmetrical magnetizing current. This is due to the ampere-turn imbalance applied to the

transformer caused by both PWM pulse width and pulse number variation between half cycles.

The PWM method is also suited to voltage control as equation 4.1 implies. A later development will give an exact relation useful for voltage level control. The effective range is limited where, for low values of K, more of the energy appears at the carrier (switching) frequency ω_c. Finally at K equal zero, all the energy is at ω_c (and multiples thereof). At intermediate K, energy appears at ω_m, ω_c and as sidebands of ω_c. It is significant that no low order harmonics appear until K exceeds 1 in which case 3rd, 5th, and higher odd harmonics appear. For these reasons and because filter requirements are minimal, the modulation depth is restricted to values less than unity.

The PWM bridge circuit was tested using both bipolar and thyristor devices. It is a fact that thyristors dominate the power electronic field where high current and voltage devices are required. However, as switching speeds are increased, the time required to commutate the thyristor consumes a larger fraction of each switching period. Present state-of-the-art thyristor devices, for example the gate-turn-off (GTO) thyristor, are efficient up to a few kHz. Overlapping this range and extending up to approximately 20 kHz, bipolar junction transistors (BJT) meet most requirements. Where converter weight is of primary concern, the minimization of magnetics requires switching speeds in the hundreds of kilohertz. Above 20 kHz the power MOSFET

has emerged as a strong contender with the BJT and at the higher frequencies clearly excels.

A frequency ratio of 30 (1.8 kHz) was chosen in this research because GTO devices could be studied at the higher end of their application range. Because of the large differences in control terminal drive requirements of these three devices, the driver circuits become more complex. The bipolar, a minority carrier device, relies on the continuous injection of base charge of magnitude dictated by the collector peak current and saturation current gain h_{FE}. The GTO is a latching device which exhibits BJT behavior for anode currents less than its latching current level I_h and remains in its high conduction state for anode current I_T greater than I_h. The thyristor enters the regenerative or latching state at the onset of double injection, i.e., injection of holes by the p-anode and electrons by the n-cathode. The advantage of the GTO is the ability of the gate to turn the device off. Where a BJT will always return to its off state upon the removal of base current, a thyristor will remain latched on. Appendix B contains an analysis of the effects a latched thyristor can have in a bridge circuit. During this research, one GTO was destroyed by excessive I^2t because of a failure in its gate driving stage. In a VSI circuit, a commutation failure is a particularly catastrophic event. The GTO thyristor is a four layer device in a p-n-p-n structure. A useful circuit model is that of a pnp transistor at the anode interconnected with

an npn transistor at the cathode. The outer p^+ and n^+ are generally heavily doped (10^{20}) and the internal p-base region is more heavily doped (10^{18}) than the adjoining n-region (10^{14}) which is also the widest for voltage blocking capability. The cathode-gate junction is of the shorted emitter structure to improve its reapplied dV/dt withstand ability. Essentially this can be modeled as a low value base to emitter shunt resistance on the npn transistor. As the device turns off, the fast-rising anode voltage induces a displacement current via the junction depletion capacitance. This current appears at the npn base as turn-on current. The shorted emitter lowers the emitter efficiency sufficiently so that the device can regain its forward blocking ability.

In inverter applications and especially in PWM circuits it is necessary to have fast turn off. Therefore, GTO devices need low minority carrier lifetime in the base regions. The highly doped end regions have low lifetime carriers already. Usual methods of base minority carrier lifetime control are the introduction of recombination centers by impurity (gold) diffusion or by high energy particle irradiation (electron and gamma). Present devices rely on the creation of lattice defects by high energy particle radiation which does not produce the high leakage currents that gold doping does. As a result, the pnp current gain h_{FE1} is low (as a result of the wide n-base) whereas the npn current gain h_{FE2} is current dependent.

Many device parameter tradeoffs are required in thyristor design. The major compromise is between forward voltage drop in the ON state V_T and turn off time t_q. These parameters are reciprocally related and contemporary devices in the 1kV GTO class exhibit turn on gains of a few hundred and turn off gain of less than ten, typically five or six. These values were confirmed experimentally.

The remaining circuitry of the PWM controller and switch driver circuits are explored in Appendix C. Figure 4.4 is a functional diagram of the complete PWM inverter stage. To minimize switching losses, a collector-to-emitter voltage snubber circuit composed of elements R, C, and D in Figure 4.4 is connected in parallel with the main switch. Figure 4.5 is a plot of measured turn off characteristics for a Motorola 2N5633, 150W switching transistor operating within its safe operating area (SOA). Since lead inductance is invariably present, the switch operation remains within the reverse bias safe operating area (RBSOA) by relying on the snubber circuit to act as a collector clamp. The driver connecting switching functions H1 and H2 to the switch elements supplies both forward and reverse drive. Current I_{B1} in Figure 4.4 is defined as the base turn on current and I_{B2} as the base reverse current drive to speed up base stored charge removal. The use of turn off drive current I_{B2} reduces the turn off time, t_{0T}, in Figure 4.5. That is the time interval from removal of forward drive until collector current has fallen to 10% of peak.

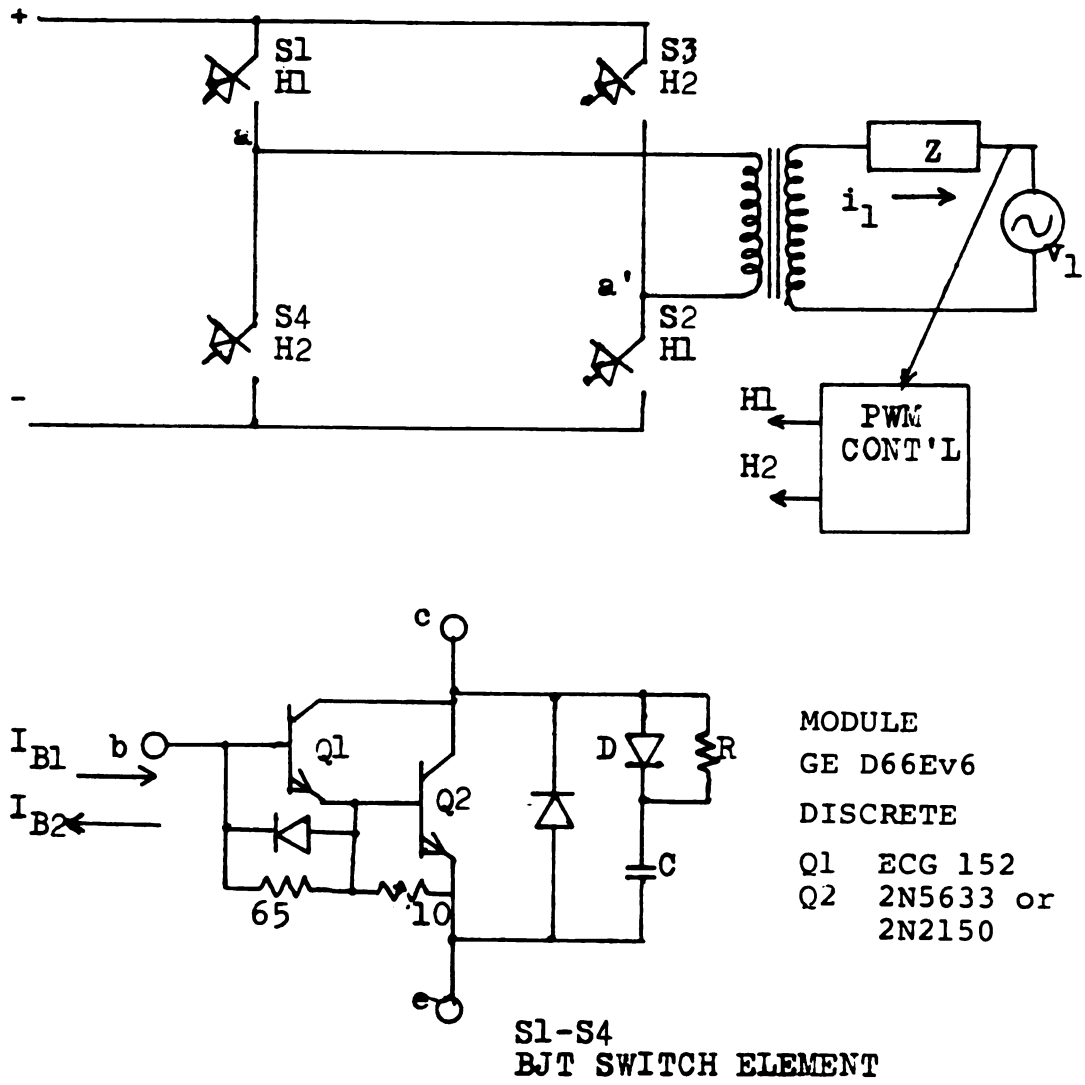


Figure 4.4. PWM inverter functional diagram.

2N5633 BJT

1) C = 0, I_{B2} = 0, t_{oT} = 35μs
2) C = 0, I_{B2} = .15A, t_{0r} = 35μs
3) C = .05μf, I_{B2} = .15A, t_{oT} = 3.5μs

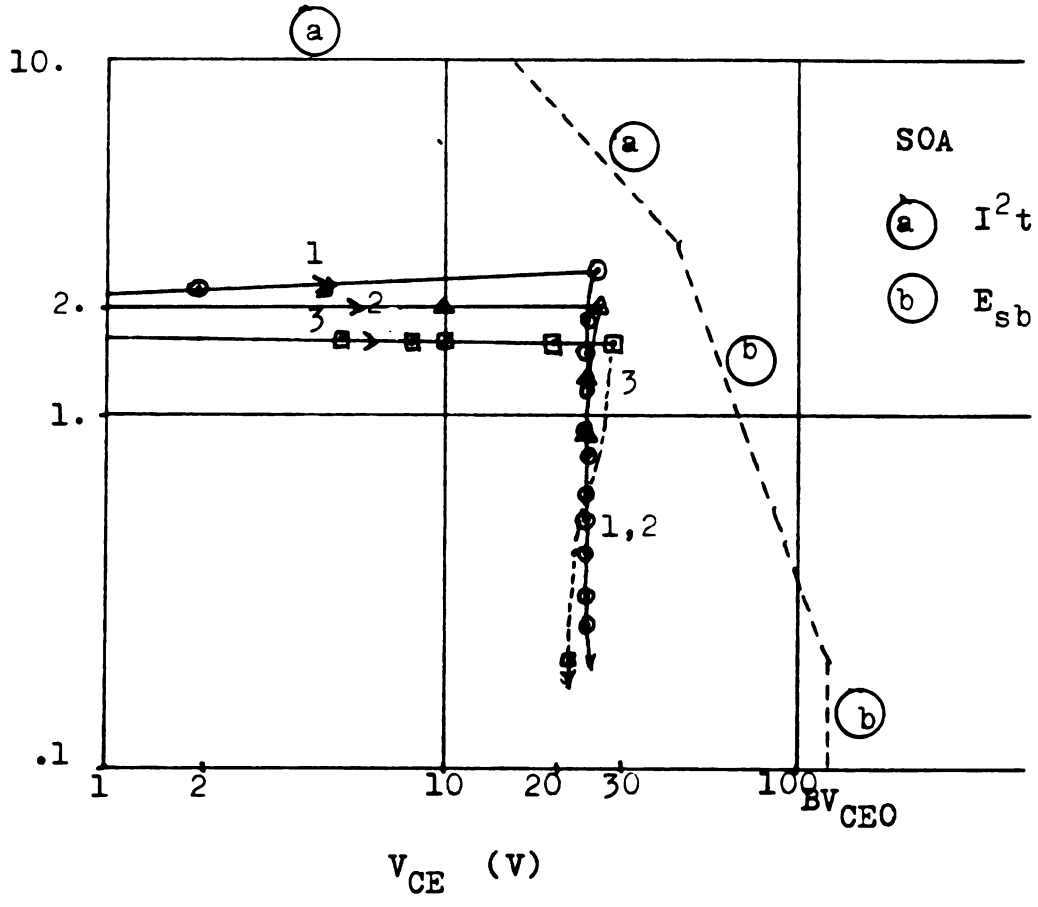


Figure 4.5. Turn off trajectories of a BJt power transistor

The respective values of I_C peak are 2.5, 2.0, and 1.6 ampere and the final V_{CE} sustaining voltage is 25 volts. The density of points reflects the relative amount of the total trajectory time spent at different current levels. Operating curve 1 has the longest turn-off time since the only means of base charge removal is recombination whereas in 2 and 3 reverse drive is applied which aids in charge removal. Operating curves 2 and 3 have an order of magnitude lower turn- off time than 1 for approximately the same level of collector current. The significant difference is that a higher density of measurement points occur on 3 for low values of V_{CE}. This means that $^{dV}/_{dt}$ limiting of $V_{CE}(t)$ during turn off by a snubber network further improves switching performance because the time on trajectory near the SOA limit b is low. Thus the transistor dissipation is lowest for curve 3 in Figure 4.5.

A further reduction of transistor dissipation is possible by the incorporation of anti saturation clamping from collector to base of the npn switch. This technique is termed a Baker clamp. Ref. [47] gives further results for turn on and turn off characteristics for various cases of reverse bias and collector clamping. A key result is that transistor energy absorption E_{sb} increases with increased gate reverse bias provided the collector voltage is clamped. The conclusion at this point is that switching applications using bipolar devices use RC networks to minimize the time at high dissipation levels and preferably have some means of

keeping the device at saturation while inhibiting operation in deep saturation.

The action of the R,C,D network is similar to that of an external current commutation circuit. When the transistor collector to emitter voltage begins to rise, the capacitor C limits its rate of increase according to the relation $I_P/C = S.R.(V_{CE})$. For case 3 of Figure 4.5, this voltage slew rate is limited to 32V/μS until C charges to V_{CE} off. In order that a large dI/dt resulting from a fully charged capacitor discharging into the collector of the npn at turn on not damage the npn, a diode D is added. This reverse biased diode forces C to discharge through resistor R with a time constant of 3.4μs (R=68 ohm) with a maximum dI/dt of $Vcap/R^2C$ or 0.1 A/μs.

The circuit shown in Figure 4.4 was constructed using bipolar switching devices and in this instance the frequency ratio P of the controller was set to 29. The switch existence functions H1 and H2 were programmed to produce 3-level PWM with a modulation depth setting K≈.9. The results of this experimentation are given in Appendix C.

The next topic involves the study of thyristors in this application. It has already been noted that thyristors are much more rugged than the BJT but what are the switching characteristics like? Unlike the BJT, a GTO thyristor requires a current source turn-on driver and a voltage source turn-off driver. Although a current pulse I_{GF} will turn a GTO on, provided its duration is sufficient to insure

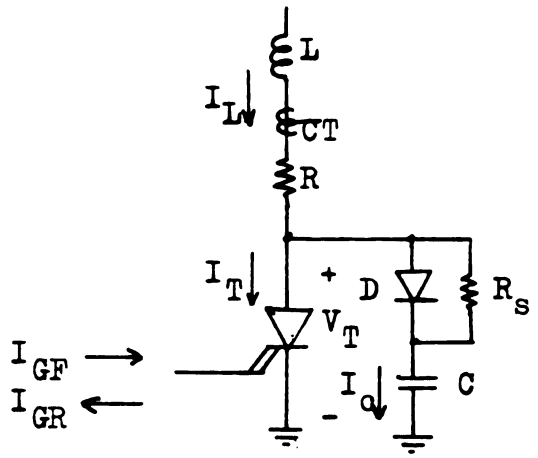
the formation of a plasma beneath the cathode contact and hence entry into the regenerative mode, it is good practice to sustain I_{GF}. Then if anode current I_T falls below I_h the device will remain conducting. The requirement for voltage sourced turn-off results from the GTO's physical construction. In a conventional thyristor (SCR), application of reverse potential (V_{AK}) creates an electric field within the thyristor that confines the conducting plasma into a high density current filament at the most remote point from the gate structure. The turn off concept is akin to extinguishing an arc by blowing it out. If the path followed by the high density current filament can be lengthened, the filament will extinguish itself. This is accomplished by placing the gate structure at the thyristor pellet center and then diffusing the p^+ anode such that the cathode, which surrounds the gate, overlaps the anode. Now when reverse gate potential is applied, the plasma retreats to the outer perimeter of the cathode where the current filament is swept off the anode. A second device fabrication step is the diffusion of a high resistivity p- into the p-type gate region between the cathode and gate to inhibit gate to cathode avalanche. The p-type gate region remains with higher conductivity to minimize its lateral resistance. The reverse gate current I_{GR} will resemble a diode reverse recovery current. When this current decays away, the reverse bias V_{AK} due to the voltage source turns

the device off. This voltage source magnitude must be less than the gate-cathode breakdown potential.

To accomplish this, the BJT driver circuits described in Appendix C were modified to provide I_{GF} current sourcing and I_{GR} voltage turn-off. If in Figure C.8, the collector resistor on Q3 is set to zero and its base resistor reduced to insure peak I_{GR} can be switched, then correct voltage sourced turn-off is achieved. A higher level I_{GF} is provided by reducing the collector load resistor of Q2 to about one-fourth.

The turn on and turn off performance of a GTO was measured using the circuit shown in Figure 4.6 and the results plotted in Figure 4.7. The value for L has been calculated from the turn-off response of Figure 4.7 since the connecting lead inductance was unknown. When I_{GR} in Figure 4.7 was increased to .52A, the anode current I_T storage and fall times remained nearly the same but the pulse width of I_{GR} was reduced 86% to 0.74μs.

Analysis of the thyristor switching waveforms can be done by considering the phenomena occurring during each time interval. During the turn on delay interval t_d, the pulse of gate current I_{GF} causes single injection by the n^+ cathode emitter to commence. At approximately one microsecond, these cathode-emitted electrons are swept across the gate region depletion layer and injection of holes by the p^+ anode has resulted in the onset of double injection. The next interval t_r defines the rise time of anode current I_T.



Th1	BTV58-1000R
V_s	26V
R	7.8 ohm
L	7.5μH
C	.047μF
R_s	68 ohm

Figure 4.6. GTO evaluation circuit

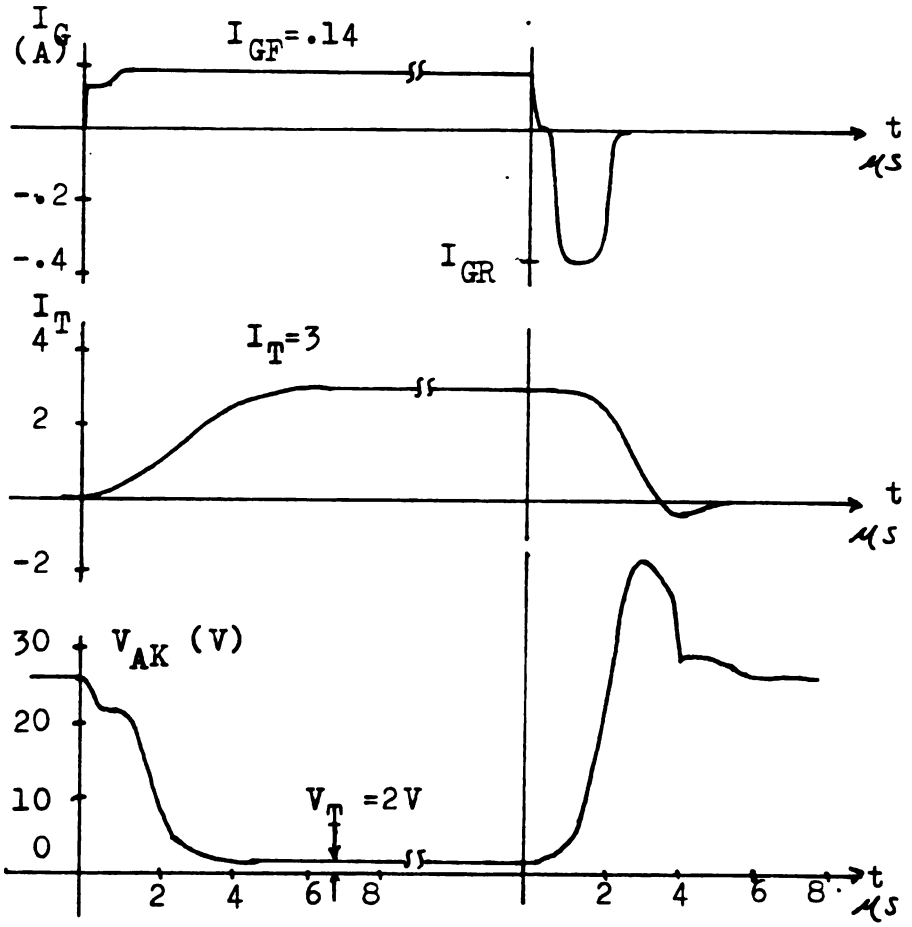
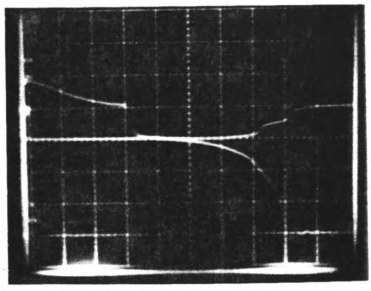
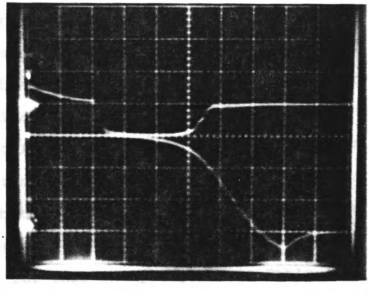


Figure 4.7. GTO switching waveforms.

During this interval the npn current gain, being a current dependent parameter, has reached the critical point at which regeneration occurs. A conducting plasma of electrons and holes exists beneath the cathode nearest the gate contact and begins to spread with finite velocity across the cathode. The anode to cathode conductivity increases rapidly and anode to cathode voltage V_{AK} drops rapidly to its ON state value V_T. By the end of the current rise time the plasma has become more uniform. In Figure 4.7 the 450 ns delay at gate current zero crossing is due to the switching speed limitation of the gate driver. The storage time t_s begins when I_G starts negative and extends to the point where I_T has dropped by 10%. During this storge time, the large pulse of gate current I_{GF} depletes excess p-base charge so that turn off of anode current can begin. During anode current fall time, the internal electric field due to $-V_{AK}$ forces the conducting plasma into a high density current filament. The anode to cathode conductivity decreases and the thyristor begins to support forward voltage. The overshoot of V_{AK} is due to lead inductance and the dI/dt of anode current. It is during this fall time t_f, that the large dV/dt of V_{AK} is capable of re-gating the thyristor on. The final dynamics in I_T and V_{AK} are due to the action of the snubber circuit. Figure 4.8a and b show the turn off transients with and without this RC damping. The data in Figure 4.8 was obtained using pulse techniques with a duty ratio of less than 4%. In a) the reverse gate current pulse



a) Without RC damping IGF .4A, IGR .5A, I_T 6A
0.5μS/cm



b) With RC damping 0.5μS/cm

Figure 4.8. GTO gate and anode current during turn off.

width is 2.5μs at the 50% points and the storage time is 1.6 μs. In b) the pulse width of I_{GR} is reduced to 1.7μs and the GTO storage time to 1.4μs. As the detail in Figure 4.8b shows, the undershoot of load current is due to capacitor current I_C acting as an external current commutation path.

Example 4.1: Investigation of the R-C snubber circuit effect on thyristor turn-off. Figure 4.8a shows that the GTO will turn off the anode current I_T quickly, and for the parameters given, yields a 275% peak overshoot in anode voltage V_{AK}. Therefore, in order to best utilize the forward blocking capability of this device near its design limit, V_{DRM}, it is essential that any inductive overvoltage be limited. The most direct method of reducing this voltage overstress is with a shunt capacitor. With this capacitance in parallel with the device, the lead inductance and capacitance form an RLC series resonant circuit. A first approximation to its behavior is to assume that when load current I_L has dropped to 90% of its ON state value, the thyristor current I_T drops to zero, i.e., the capacitor has commutated the current. The fall time t_f of I_T will be assumed a step change in this analysis. With the parameter values for this example given in Table 4.1, the initial conditions and response $i_L(t)$ can be calculated.

Using the circuit drawn in Figure 4.6 with initial conditions based on the above approximation of $i_L(0^+)=.9I_T$

$$\left.\frac{di_L(t)}{dt}\right|_{0+} = \left[Vs - Ri_L(0+) - V_{AK}(0+)\right]/L \qquad (4.3)$$

$$= -1.36\ A/\mu S.$$

The Laplace transform $I_L(s)$

$$I_L(S) = \frac{S\left[V_s(s) - [v_c(0+)](s)\right]/L + S^2[i_L(0+)](s)}{S^2 + R/L\ S + 1/LC} \qquad (4.4)$$

Substituting the Laplace transforms of the voltages and currents in equation 4.4 results in

$$I_L(s) = \frac{\left(V_S - V_T\right)/L + S\left(.9\ I_T\right)}{S^2 + R/L\ S + 1/LC} \qquad (4.5)$$

The inverse Laplace transform of equation 4.5, with damping constant $R/2L$ less than the undamped natural frequency $(LC)^{-1/2}$, e.g., the damping coefficient zeta is 0.265, yields

$$i_L(t) = \frac{\left[V_S - V_T - 0.9\ I_T\ R/2\right]}{\sqrt{\frac{L}{C} - R^2/4}} \exp\left[-\frac{Rt}{2L}\right] \sin\sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2}\ t \qquad (4.6)$$

$$+ 0.9\ I_T \exp\left[-\frac{Rt}{2L}\right] \cos\sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2}\ t\ ;\ 0 \leq t < t_1$$

Where t_1 is defined as the time at which diode D becomes forward biased. For time t greater than t_1 the resistor R_s is switched into the circuit raising the damping coefficient

Table 4.1

Parameter Values for Example 4.1

V_S = 40V

V_T = 2V

I_T = 6A

R = 6.7 ohm

C = .047 F

L = 7.5 H

V_{AK} = 14V measured

_____ R, C, and D

---- C only

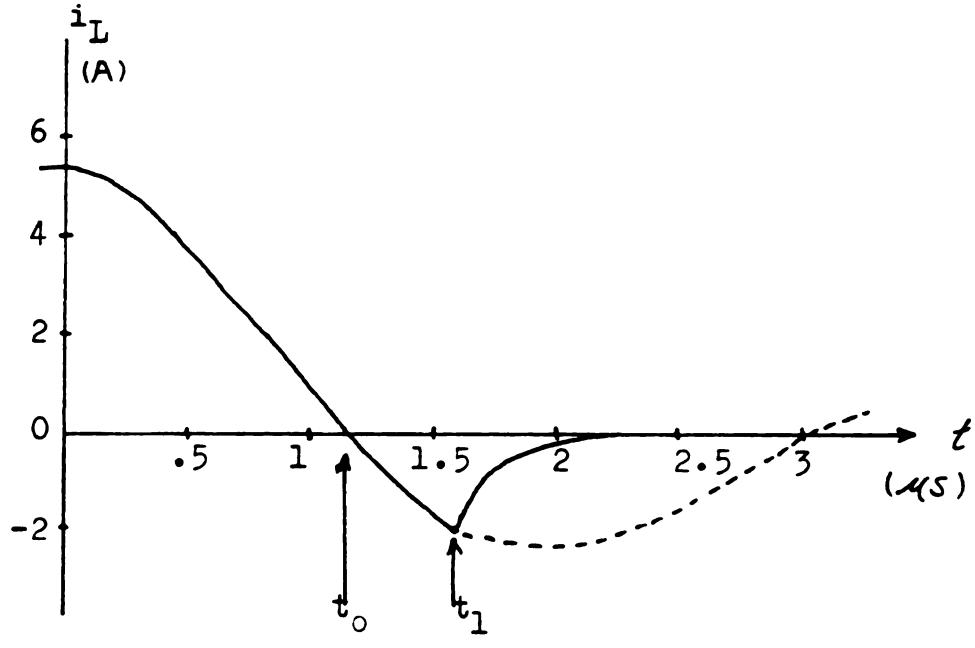


Figure 4.9. GTO turn off example.

to 2.96. This results in a hyperbolic tail to the current as shown in Figure 4.9 and verified by the actual response in Figure 4.8b lower trace. The diode D switches after its stored charge Q_{RR} is removed. Suppose this charge is removed by $i_L(t)$ given in equation 4.6 flowing through diode D over the interval t_o to t_1 in Figure 4.9. Then,

$$Q_{RR} = \tfrac{1}{2} I_R t_{rr} = \int_{t_0}^{t_1} i_L(t)dt \qquad (4.7)$$

where I_R is the peak value of this reverse current and t_{rr} is the diode reverse recovery time. For this diode Q_{RR}=.35μC and t_{rr}=.4μs so that I_R=1.8A. From equation 4.6 the corresponding value of t_1 is 1.6μs. For $t>t_1$ diode D is reverse biased so that the current response becomes

$$i_L(t) = \frac{[V_s - v_c(t_1) + I_R(R+R_s)/2]}{\sqrt{\left(\frac{R+R_s}{2}\right)^2 - \frac{L}{C}}} \exp\left[-\frac{(R+R_s)}{2L}(t-t_1)\right] X \qquad (4.8)$$

$$\sinh\sqrt{\left(\frac{R+R_s}{2L}\right)^2 - \frac{1}{LC}}\ (t-t_1)$$

$$- I_R \exp\left[-\frac{(R+R_s)}{2L}(t-t_1)\right] \cosh\sqrt{\left(\frac{R+R_s}{2L}\right)^2 - \frac{1}{LC}}\ (t-t_1)$$

where the new initial condition on capacitor voltage is computed from

$$v_c(t_1) = \frac{1}{C}\int_0^{t_1} i_L(t)dt \qquad (4.9)$$

$$= 69.17 \text{ V.}$$

The result of equation 4.9 is substituted into equation 4.8 and the result is plotted in Figure 4.9 for time greater than t_1.

This example serves to illustrate the fact that lead inductance in the connecting leads inhibits fast turn-off of circuit current. When a snubber of the type discussed is implemented the current fall time can be very rapid during the underdamped phase and highly damped after the diode D in Figure 4.6 recovers its reverse blocking capability. Thus to minimize anode current oscillation in a switching circuit the lead inductances must be minimum. The inverse diode across the switch element shown in Figure 4.4 has no effect on this phenomena in the case of resistive load. When the bridge supplies current to a reactive load, these antiparallel diodes conduct for portions of each cycle during which reactive current flows. The case of driving a transformer for isolation will be explored in the next section.

4.2. Analysis and Testing of the 2-Level PWM Converter

A PWM converter is classified as 2-level if the waveform switches between two states. The output of the converter in Figure 4.4 will be 2-level when switch pairs

(s_1,s_2) and (s_3,s_4) operate with complementary switching functions H1 and H2, where H2=1-H1. In this manner the resulting transformer voltage switches between $+V_s$ and $-V_s$. The case of 3-level PWM is obtained when either pair of switches (s_1,s_3) or (s_2,s_4) have 50% duty ratio and the remaining 2 switches each have switching functions H1 and H2. In this case the transformer voltage switches between $+V_s$ and ground at the PWM rate and then between $-V_s$ and ground. The process is periodic with period given by the 50% duty ratio switches. The experimental results for 3-level PWM are given in Appendix B.

The converter configuration of Figure 4.4 is capable of both voltage control and harmonic elimination. The frequency ratio P defines the number of pulses per cycle of the fundamental provided the system operates with modulation depth K≤1. Recent researchers [31,32] have shown that, using PWM, it is possible to eliminate P-harmonics, and achieve voltage control over the fundamental. However, the method requires the apriori calculation of the individual PWM notch width for each desired voltage level. The method is essentially one of conduction angle modulation (CAM) and differs from the natural sampling PWM considered here in that the latter achieves harmonic elimination with continuously variable voltage control. A prominent application of voltage controlled inverters is in the variable speed a-c drive field where constant flux motor operation necessitates fixed voltage per hertz ratios. This programmed waveform

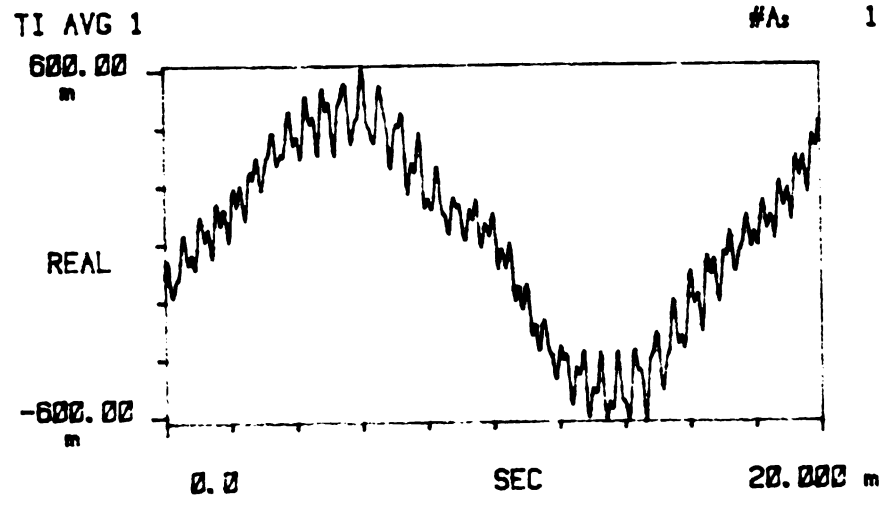
concept has been further studied in [33] wherein eight structurally related PWM wavetypes are compared using dis

tortion factor

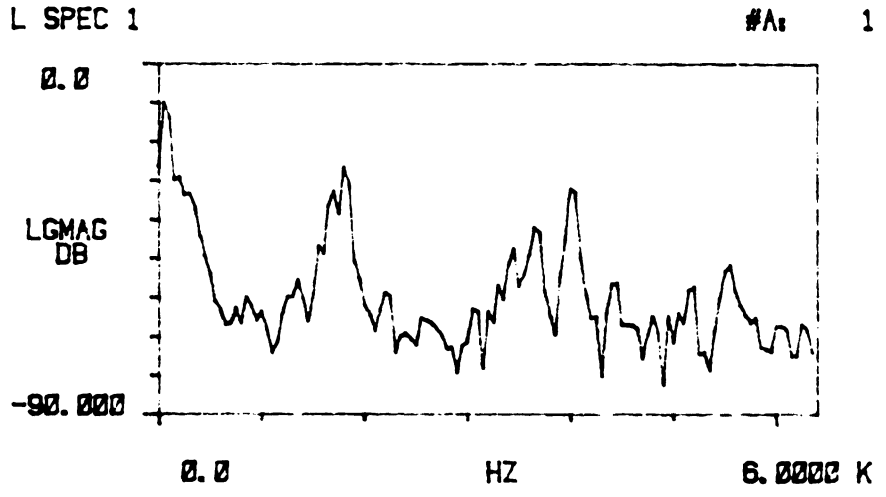
(see Appendix A) as an objective function to assess harmonic distortion for a given fundamental magnitude. Others [34] have addressed the problem of spectral error due to finite commutation time of switching devices. These finite pulse slopes introduce fine structure to the PWM spectra at harmonics of the output frequency, albeit of insignificant amplitude.

With this 2-level PWM inverter operating into a fixed load, the measured performance is shown in Figure 4.10. Here the PWM bridge switches current through the primary of an isolation transformer into a filter network consisting of a series inductor and shunt capacitor. This filter is resistively loaded. The measured load current and spectrum are shown in Figure 4.10a and b. This configuration led to several experimental findings.

First the transformer magnetizing current introdued asymmetry into the current waveform due to distortion of its output voltage. Transformer VA rating was found to have significant impact on the spectra, chiefly in the introduction of low order even and odd harmonics (Figure 4.10b). Next the filter inductor core, besides having the required high frequency properties, attained using ferrite, must be gapped. The presence of an ungapped core caused



a) Load Current P=30, K=.75, L_F=45mH, C_F=5μF.



b) Current spectrum recorded and processed on hp5423A.

Figure 4.10. 2-Level PWM with passive load a) filtered load current, b) load current spectrum.

noticeable audio noise levels due to magnetostriction as well as reduced range of load current. This happens because peak load current beyond the saturation ampere-turns negates filtering. A gapped core alleviates both these phenomena. Figure 4.10b illustrates the strong fundamental component of current at 60 Hz, the presence of several low order harmonics, and harmonic clusters about multiples of the switching frequency, f_c=60P=1800 Hz. The result so far shows that sinusoidal current is attainable in a stand-alone mode. In addition the harmonics present are amenable to filtering. Next the source of the low order harmonics can be explored.

Restricting magnetizing current harmonics imposes strict limits on transformer VA rating. In addition to core thermal limits set by hysteresis, eddy current, and Joule heating, the peak core flux levels for a given material must not be exceeded. The higher efficiency core materials available include ferrite and amorphous metal. However, because of lower permeability of these materials, core volume must be increased. The relation given in equation 4.10 shows the dependence of flux density B on construction and operating conditions.

$$\Delta B = \frac{V\tau}{NA} \times 10^{4} \qquad \text{(Tesla)} \tag{4.10}$$

In this expression ΔB represents the change in flux density to application of pulse with magnitude V volts and duration τ seconds. This pulse is applied across a winding of N turns

with an effective area A. For the case of a PWM waveform, the voltseconds ($V\tau$) applied to the transformer core increase in proportion to the amplitude of the sinusoidal modulating function. Define the saturation flux density of this core material as $\hat{B}$. Then for a given number of primary turns (N) and effective core area (A), the change in core flux density (ΔB) must remain within the operating flux limits of $\pm \hat{B}$. An increase in $V\tau$ such that ΔB exceeds either $+\hat{B}$ or $-\hat{B}$ will be accompanied by a large increase in primary current $i_p(t)$. This results due to core saturation, the attendent drop in magnetizing inductance, and a dramatic increase in core magnetizing force (H).

Consider the case where the average voltseconds ($V\tau$) impressed upon the core during alternate half cycles are not equal. This is the case illustrated in Figure 4.11 in which primary turns (N) and core area (A) are constants. The flux ϕ, Webers, and flux linkages λ, Weber turns, are used as the ordinate axis labels. The core magnetizing characteristic is drawn in C, showing the locus of core hysteresis curve apices versus increasing magnetic field H. As shown in a and b, the voltage $V_{pri}(t)=\dot{\lambda}(t)$ with an unbalanced volt-second product is supported by an offset of the core magnetizing characteristic. The nonlinearity of the core flux versus current results in an asymmetrical magnetizing current. Here the d-c bias current $I_o=^1/_N H_o$ results in the presence of even harmonics in the current superimposed on the odd harmonics produced by the odd symmetry of ϕ versus i.

With a PWM waveform, the asymmetry in voltseconds is a result of a distorted line voltage signal and any signal processing asymmetry of the control circuits. Recall also the comments on phase locked loop behavior when P is odd. The following experimental results were obtained with P=29 for which $V\tau^{+}>V\tau^{-}$ as shown in Figure 4.11a. Carry the above analysis further and assume a sinusoidal voltage wave with positive offset V_o. Since flux linkage is the integral of voltage across the N-turn primary, then flux linkages can be expressed as

$$\lambda(t) = \lambda_0 - \lambda_1 \cos \omega t$$
$$i_{pri}(t) = g^{-1}[\lambda(t)] = g^{-1}[N \phi(t)] \qquad (4.11)$$

where the function g represents the Rayleigh arc in Figure 4.11c. In [15] an empirical equation is found which gives a close approximation to actual magnetizing current. If

$$i_p(t) = A \text{ Sinh } [B\lambda(t)] \qquad (4.12)$$

equation 4.11 is substituted into equation 4.12 and expanded using the trigonometric identity Sinh (A-B)=Sinh A Cosh B-Cosh A Sinh B, an expression for $i_p(t)$ is obtained.

$$i_p(t) = A\text{Sinh}B\lambda_0\text{Cosh}B\lambda_1\cos\omega t - A\text{Cosh}B\lambda_0\text{Sinh}B\lambda_1\cos\omega t \qquad (4.13)$$

In Figure 4.12 the measured results are shown for a transformer with ungapped core and asymmetrical primary voltage. The constants in equation 4.13 were empirically determined for this case as A=.00046, $B\lambda_0$=.35, and $B\lambda_1$=9.0.

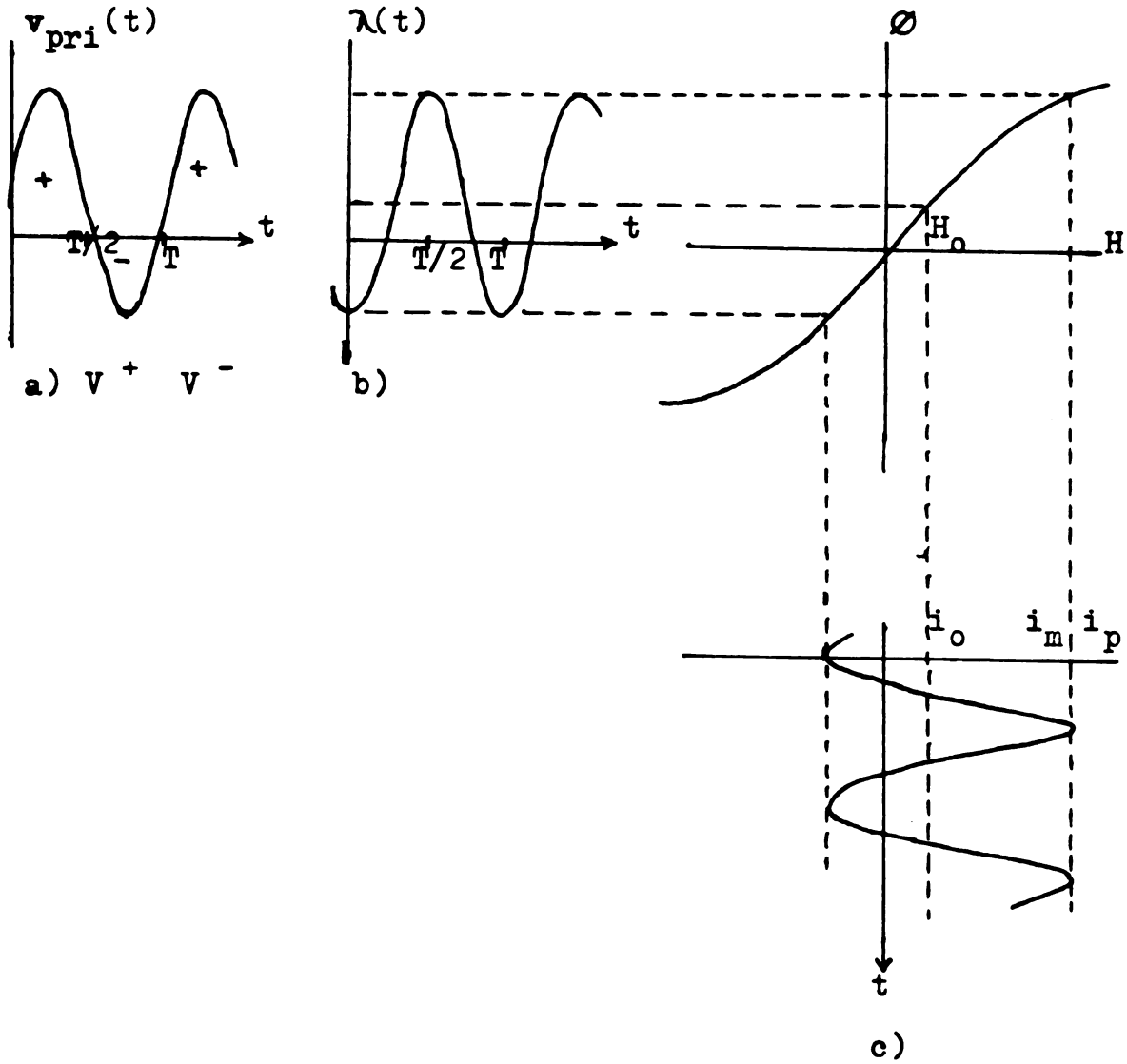


Figure 4.11. Transformer asymmetry due to core bias.

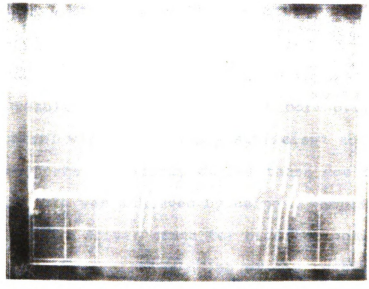


Figure 4.12. Measured magnetizing current with PWM drive, asymmetrical case. Current i_d is the bridge dc input current.

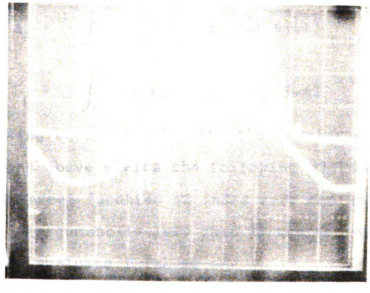


Figure 4.13. Measured magnetizing current with PWM drive, symmetrical case.

To remedy this asymmetrical condition, either the PWM drive signal can have any voltsecond unbalance sources removed (accomplished later in this research with the phase lead circuit shown in Appendix C) or neutralized. Figure 4.13 shows the results of neutralizing the core offset effects by using a control winding to apply sufficient ampere-turns of magnetizing force to exactly cancel those due to the V-s imbalance. This was achieved by using a complementary-symmetry current driver stage for bidirectional current sourcing into the control winding of the test transformer.

The harmonic content of the magnetizing current <u>envelope</u> can be obtained by computing the Fourier series for $i_p(t)$ given by equation 4.13 as

$$i_p(t) = \sum_{n=1}^{\infty} [a_n \cos n\omega t + b_n \sin n\omega t]$$

$$\text{where} \quad a_n = \frac{1}{\pi} \int_{-\pi}^{\pi} i_p(\omega t) \cos n\omega t \, d(\omega t) \qquad (4.14)$$

$$b_n = \frac{1}{\pi} \int_{-\pi}^{\pi} i_p(\omega t) \sin n\omega t \, d(\omega t)$$

Substituting equation 4.13 into the Fourier coefficient expressions above yields the following where $I_0(\cdot)$ is the modified Bessel function of index zero and argument $B\lambda_1$. Since this argument is less than 12 the series formula may be used to evaluate $I_\nu(x)$ as

$$I_\nu(x) = \sum_{s=0}^{\infty} \frac{1}{s!(S+\nu)!} \left(\frac{X}{2}\right)^{2S+\nu} \qquad (4.15)$$

where $\nu = 0$. Then the coefficient a_o in equation 4.14 becomes

$$a_0 = AI_0(B\lambda_1) \text{ Sinh } B\lambda_0. \qquad (4.16)$$

With this coefficient the offset current i_o of Figure 4.11c can be calculated as $i_o = a_o/2 \approx 90\text{mA}$. This bias in magnetizing force $H_o = Ni_o$ is neutralized as shown in Figure 4.13 by $-N_c I_{dc}$ ampere-turns. Here, N_c is the number of turns in the control winding.

A test of this neutralized transformer (Table 4.2) shows that the magnitude of control current had to be increased as the primary peak-to-peak PWM voltage was raised. Also note the column labeled K (the PWM modulation depth) giving the values such that equation 4.10 is satisfied. This is because the peak magnetizing current i_M in Figure 4.11c is held fixed at 2.2A. Table 4.2 lists the empirical results.

This data shows that peak-to-peak primary voltage (PWM) had to be increased by approximately the same percentage as modulation depth was reduced. This is consistent with maintaining constant the primary <u>fundamental</u> volts per turn. The core is an ungapped 3C8 ferrite. When a gapped core was used in this same experiment, the same volts per turn was realized for two different values of gap length. The magnetizing current peak value again held constant. The gapped core did require a greater amplitude magnetizing current (due to its increased reluctance) at lower V_{pri}.

The data of Table 4.2 serves to clarify a significant point: transformer rating for PWM application is critical. For voltage control using modulation depth control and a fixed d-c source V_s, where $V_{pp}=2V_s$, it is necessary that transformer maximum volts/turn not be exceeded at the largest value of K. Therefore, in addition to its volt-ampere rating for power through-put, the operating volts/turn must have sufficient margin below its rated value if voltage control is used. Furthermore, a gapped core is much more tolerant of voltsecond imbalance but requires larger magnetizing current.

In [11] it is shown that at 1.6 p.u. of rated voltage, the magnetizing current requirement equals the transformer rated current of distribution transformers. At more modest values of overvoltage the transformer current harmonics increase substantially. For 15 to 20 percent voltage overdrive the low order current harmonics--third, fifth, and seventh--exhibit near concurrent peaks. Most notably, the third harmonic can reach 75% of the fundamental. This is an "interconnection effect" which should be monitored by utilities where overvoltages due to distributed sources are likely.

The remaining magnetizing current harmonics for the envelope wave of $i_p(t)$ can be computed. The result will consist of both even and odd harmonics where the coefficients computed using equations 4.14 will be hyperbolic Bessel functions of corresponding order and argument $B\lambda_1$.

Table 4.2

Transformer Bias versus PWM Modulation Depth

K	V_{pri}	I_{dc}
Modulation Depth	Primary Volts (V_{p-p})	Bias Current (mA)
.91	24	80
.86	26	75
.77	28	100
.68	34	100
.59	38	100
.50	44	100
.36	58	130

The above analysis explains the presence of low order harmonic load current due to PWM. These harmonics will consist of both even and odd order. The current switching at a PWM rate within this envelope will generate current harmonics about multiples of the switching frequency.

Two techniques of evaluating the harmonic content of a PWM waveform are as follows. The first method is to compute the spectrum of individual notch waves for each of M such notches defining the PWM waveform and to use superposition [33]. This technique requires knowledge of exact pulse and notch widths. Voltage control can be realized in a microprocessor controlled PWM inverter by having the switch element firing angles stored in a look up table in memory. This is the programmed waveform method. As such the discrete and well-defined time steps inherent in this method yields exact values of the PWM pulse and notch widths. The degree of resolution in output pulse width will depend upon memory capacity and word length. A second method which analyzes the harmonic content of a PWM waveform for continuous variation (as opposed to discrete step) of pulse and notch width is based on the technique first proposed by Bennett [37,39] in an unpublished report. This technique applies to the cases of uniform and natural sampling.

Refer to Figure 4.14. The line with slope $^{1}/_{P}$ (P is the frequency ratio) intersects the modulating function (cosine curves) at the switching points of the resulting PWM waveform. The range of P is from zero to infinity. Notice

what happens as P traverses this range. For $P=\infty$ the line becomes the abscissa ($\omega_m=0$) and the output is a pulse pattern with frequency ω_c and amplitude 1. As P is increased from zero, P assumes values that are rational, irrational, and integer. At p=0 the line is vertical so that the switching function has degenerated to an impulse. It can be seen that this method accommodates all frequency ratios.

The modulating function plotted vertically in Figure 4.14 is $\pm 2k\pi \pm \pi/2\ (1-K\cos\omega_m t)$ where k=0,1,2,... and K is the modulation depth $0<K\leq 1$. For each K, a family of curves result such that the intersection of the curve with the line defines the modulated switching function $F(\omega_c t,\omega_m t)$. This can be best visualized if a third axis is drawn. Orthogonal to both $\omega_m t$ and $\omega_c t$ in Figure 4.14. The sloping line now becomes a plane orthogonal to the $\omega_m t$ and $\omega_c t$ plane. Let the shaded areas represent unity along this third axis and the unshaded areas represent zero. Then the projections of the intersection of the plane with the sides of the 3-dimensional construction unto a plane along the $\omega_c t$ axis and orthogonal to the $\omega_m t$ axis when viewed edge on is $F(\omega_c t, \omega_m t)$. The unity values of $F(\omega_c t,\omega_m t)$ represent the pulse intervals and zero values of $F(\omega_c t,\omega_m t)$ represent notch intervals. This function can be expressed as a double Fourier series in which the Fourier coefficients are themselves Fourier series. Given integers p and q, the terms of this double expansion have oscillatory components $\cos\omega_m t$,

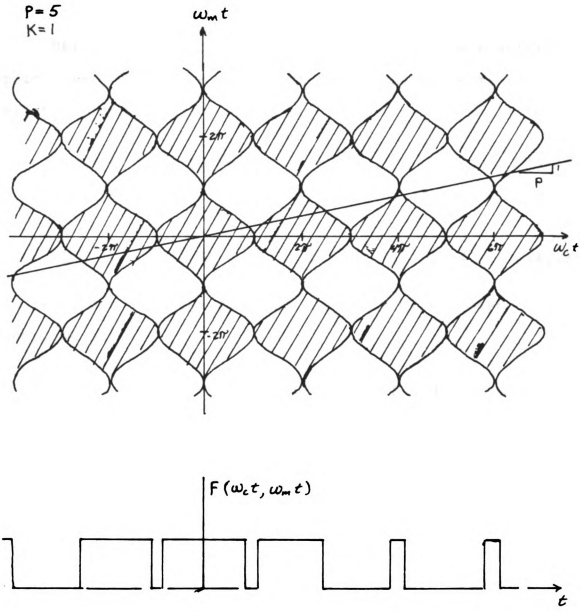


Figure 4.14. Construction for determination of PWM switching instants.

$\cos[(2p-1)\omega_c t]$, $\cos[(2p-1)\omega_c t \pm 2q\omega_m t]$, and $\cos[2p\omega_c t \pm (2q-1)\omega_m t]$. The coefficients in the expansion are products of trigonometric and Bessel functions.

Using the technique of Chapter 3, the voltage across points a-a′ in Figure 4.4 can be expressed in terms of existence functions H1 and H2 as

$$v_{a-a'}(t) = H1\ V_s - H2\ V_s \tag{4.17}$$

where $H2 = 1-H1$

$$v_{a-a'}(t) = 2V_s\ H1 - V_s \tag{4.18}$$

In reference [36] the existence function H1 has been computed as

$$\begin{aligned} H1 = {} & \tfrac{1}{2}+\tfrac{1}{2}K\cos\omega_m t + \frac{2}{\pi}\sum_{p=1}^{\infty}\left(\frac{1}{2p-1}\right)J_0\left(\frac{2p-1}{2}K\pi\right)\cos\left(\frac{2p-1}{}\omega_c t\right) \\ & - \frac{2}{\pi}\sum_{p=1}^{\infty}\sum_{q=1}^{\infty}\left(\frac{1}{2p-1}\right)\cos\left(\frac{p+q}{}\pi\right)J_{2q}\left(\frac{2p-1}{2}K\pi\right)\cos\left(\frac{2p-1}{}\omega t \pm 2q\omega_m t\right) \\ & + \frac{2}{\pi}\sum_{p=1}^{\infty}\sum_{q=1}^{\infty}\frac{1}{2p}\cos\left(\frac{p+q}{}\pi\right)J_{2q-1}\left(2pK\frac{\pi}{2}\right)\cos\left(2p\omega t \pm \frac{2q-1}{}\omega_m t\right) \end{aligned} \tag{4.19}$$

where $H1 = F(\omega_c t, \omega_m t)$, $K<1$.

Recall from Figure 4.3 that, for K=0, the base PWM wave V_{PWM} will be a square wave of frequency ratio P resulting from a comparison of a triangular wave $\omega_c(t)$ with zero. As $K \to 1$ the existence function H1 begins to exhibit an increasing fundamental component. Thus, a variable K implies voltage control over the fundamental component.

When equation 4.19 is substituted into equation 4.18 the terminal voltage is given as

$$v_{a-a'}(t) = KV_s\cos\omega_m t + \frac{4V_s}{\pi}\sum_{p=1}^{\infty}\frac{1}{2p-1}J_0\left(\frac{2p-1}{2}K\pi\right)\cos\left(\frac{2p-1}{2}\omega_c t\right) \qquad (4.20)$$

$$- \frac{4V_s}{\pi}\sum_{p=1}^{\infty}\sum_{q=1}^{\infty}\left(\frac{1}{2p-1}\right)\cos\left(\frac{p+q}{2}\pi\right)J_{2q}\left(\frac{2p-1}{2}K\pi\right)\cos\left(\frac{2p-1}{2}\omega_c t \pm 2q\omega_m t\right)$$

$$+ \frac{4V_s}{\pi}\sum_{p=1}^{\infty}\sum_{q=1}^{\infty}\frac{1}{2p}\cos\left(\frac{p+q}{2}\pi\right)J_{2q-1}\left(2pK\frac{\pi}{2}\right)\cos\left(2p\omega_c t \pm \frac{2q-1}{2}\omega_m t\right); 0\leq K\leq 1$$

where the ω terms of equation 4.19 is written as ω_c in equation 4.20. This is done because the switching frequency in this thesis is phase locked to an integer multiple P of the reference frequency ω_m, i.e., $\omega = \omega_c = P\omega_m$.

Equation 4.20 predicts the presence of a fundamental component at frequency ω_m with peak amplitude KV_s and a series of carrier frequency terms ω_c and its odd multiples. The last two oscillatory terms for synchronized operation suggest that if $[(2p-1)P\pm 2q]\omega_m$ and $[2pP\pm(2q-1)]\omega_m$ are to contain only odd harmonics, then P should be odd. Based on the earlier findings of phase-locked loop behavior and transformer magnetizing current, an even integer P will be used in the remainder of this work. Consequently the higher harmonics in the spectrum (Figure 4.10) for load current will be even.

The apparent power delivered to the defined line voltage source $v_\ell(t)$, due to PWM switching of the

transformer connected between terminals a-a' of Figure 4.4, can be evaluated.

Case I: Assume that only the fundamental component appears at the output of the transformer. Since the turns ratio is n, this voltage wil be nKV_s in peak value and have rms value $V_1=nKV_s/\sqrt{2}$. With a linear impedance Z interconnecting these sources, the conventional techniques of calculating complex power may be applied. This requires that $v_\ell(t)$ also is of fundamental content $V_{\ell_1} = V_m/\sqrt{2}$, and is assumed co-sinusoidal to be in phase agreement with equation 4.20. Then the apparent voltamperes (complex power) transferred into this impedance and defined source combination is given as

$$\begin{aligned}\bar{S}_s &= \left\{\left[\frac{(V_1)^2\cos\theta}{|Z|} - \frac{V_1V_{\ell_1}\cos\theta}{|Z|}\cos\alpha\right] + \frac{V_1V_{\ell_1}\sin\theta}{|Z|}\sin\alpha\right\} \\ &+ j\left\{\left[\frac{(V_1)^2\sin\theta}{|Z|} - \frac{V_1V_{\ell_1}\cos\theta}{|Z|}\sin\alpha\right] - \frac{V_1V_{\ell_1}\sin\theta}{|Z|}\cos\alpha\right\} \\ &= P + jQ\end{aligned} \qquad (4.21)$$

where $\theta = \tan^{-1} X/R$ is the impedance angle and α is the PWM waveform lead angle. When $Z \to jX$, $\theta = \pi/2$ the expression 4.21 reduces to the classical two source power transfer problem.

The decomposition of complex power S into average power P and reactive voltamperes Q shows the conventional dependence of P on angle α and of Q on voltage magnitudes. The average power contains that fraction of the apparent voltamperes

dissipated by the real part of Z, P_r. Likewise, the reactive voltamperes contains that fraction due to the imaginary part of Z, Q_X. No analytical relationship can be inferred for P_R or Q_X from equation 4.21. This is true in general [35]. This is also apparent by comparison of equation 4.22 with the first bracketed term of equation 4.21. Note that we cannot subtract the apparent voltamperes delivered to $v_\ell(t)$ from the total of expression 4.21. This results from the fact that apparent voltamperes do not obey the principle of conservation of energy. That average power can be arithmetically summed is a consequence of the energy principle.

$$P_R = \frac{\left(V_1^2 + V_{\ell_1}^2 - 2V_1V_{\ell_1}\cos\alpha\right)}{R^2 + X^2} R \qquad \text{Watts} \tag{4.22}$$

The average power dissipated in the impedance Z, P_R, can be calculated using circuit analysis. A more direct method for this sinusoidal case is to use a phasor diagram, Figure 4.15, of the system voltages and the connecting impedance. The impedance volt drop V_Z is obtained directly from the figure by application of the law of cosines. From this and the fact that $P_R = \frac{V_s^2 \cos\theta}{|Z|}$ yields equation 4.22.

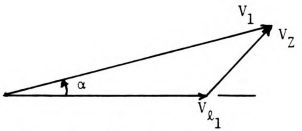
Examination of Figure 4.15 for the case of a practical inductive impedance reveals that the converter transformer output voltage must exceed the system line voltage. Thus, the transformer turns ratio n, d-c source voltage V_s, filter impedance Z, maximum or rated power P, and reactive

voltamperes Q must be chosen such that the following constraints are met. Transformer construction and core material establishes an upper limit on the volts/turn, turns ratio n affects copper loss and hence efficiency, the power dissipated in the filter P_R must be minimized, power through part P maximized, and reactive voltamperes Q minimum or zero to avoid a power factor penalty. For the case of fixed power levels, the phasors in Figure 4.15 are stationary and the above constraints are capable of being satisfied. In the case of highly variable power, as produced by a variable speed wind turbine, the operating policy will involve a compromise among these constraints. Equation 4.22 will be minimum for a minimum series resistance R. The reactive power Q of equation 4.21 can be made zero for $V_{1}/V_{\ell_1} = \cos\alpha + \sin\alpha/\tan\theta = \cos\alpha + R/X \sin\alpha$. That is, V_{1}/V_{ℓ_1} is relatively immune to lead angle variation.

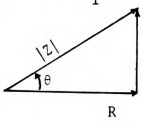
<u>Case II</u>: Assume that $v_\ell(t)$ is still of fundamental content only but let the inverter terminal voltage be given by equation 4.20. The non-linear impedance of the switching devices produces the non-sinusoidal waveform given by equation 4.20 at the transformer primary. The transformer rms output voltage is obtained as the vector sum

$$V^2 = \left(nKV_s/\sqrt{2}\right)^2 + \sum_{p=1}^{\infty} V_{cp}^2 + \sum_{p=1}^{\infty}\sum_{q=1}^{\infty} V_{opq}^2 + \sum_{p=1}^{\infty}\sum_{q=1}^{\infty} V_{epq}^2 \quad .$$

where $$V \triangleq \sqrt{\frac{1}{2\pi}\int_0^{2\pi} \left(nV_{a\text{-}a'}\right)^2 d(\omega t)} = V_s \text{ for 2-level PWM.} \qquad (4.23)$$



$$V_Z^2 = V_1^2 + V_{\ell_1}^2 - 2V_1V_{\ell_1} \cos \alpha$$



$$\cos \theta = \frac{R}{\sqrt{R^2+X^2}}$$

Figure 4.15. Phasor diagram for sinusoidal case.

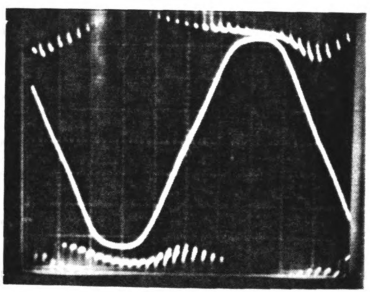


Figure 4.16. Inverter unfiltered output voltage $V_{PWM}(t)$ and line voltage $V_{\ell}(t)$.

The terms in expression 4.23 have been chosen to agree with those in equation 4.20. The first term is the fundamental component rms value. The second term is the rms value of carrier odd harmonics (V_{cp}). The remaining two terms give the rms values of harmonics about odd (V_{opq}) and even V_{epq}) multiples of the carrier frequency. Now the apparent voltamperes (S_s) supplied by the inverter must account for these non-basal frequency components. As shown in Appendix A, S_s must be expressed in terms of average power P, reactive voltamperes Q and distortion voltamperes D_s. In this decomposition Q accounts for the displacement voltamperes and D_s those due to wave distortion. In this case $S_s^2=P^2+Q^2+D_s^2$.

One technique of quantifying the distortion present in a waveform is to compute the distortion index (Γ). This measures the deviation of a given waveform from a sinewave at fundamental frequency. For a 2-level PWM waveform the distortion index is

$$\Gamma_{PWM} = \sqrt{\left(\frac{V_s}{KV_s/\sqrt{2}}\right)^2 - 1} \qquad (4.24)$$

$$= \sqrt{\frac{2}{K^2} - 1}$$

For a symmetrical square wave the distortion index is

$$\Gamma_s = \sqrt{\left(\frac{V_s}{4V_s/\sqrt{2\pi}}\right)^2 - 1} = .483 \qquad (4.25)$$

In equation 4.24 the distortion index is 1 if K=1 and for K<1 the distortion index increases rapidly. Of course, at K=0, the PWM waveform has a base frequency ω_c which is altogether different from ω_m.

When real power is subtracted from apparent voltamperes the result will be those voltamperes due to displacement and distortion, i.e., $S_s^2-P^2 = Q^2+D_s^2$. The term $\sqrt{Q^2+D_s^2}$ is defined as the non-active voltamps. The remaining questions for this case are: If distortion increases so markedly as K is reduced, then should K be used at all for voltage control? Since the non-active voltamperes also depend heavily on K, what is the optimal power factor in terms of minimum line current? Recall that when distortion currents are present, it is no longer appropriate to speak of improving power factor by simply compensating for a displacement angle. Finally, what portion of the non-active voltamperes can be compensated by power factor correction capacitors? In response to the first question, no. If the system were an adjustable ac drive, then using K for voltage control would be the most direct technique as the rotor inertia would not respond to the high frequency torque pulsations. However, in the utility interconnected application, harmonic content must be minimal [29] for the reasons stated earlier. Equation 4.20 shows that the only remaining variable to achieve voltage control, for the purpose of utility line tracking and reactive voltamperes, is V_s. Up to now this parameter has been assumed constant.

This would be the case if the source were a large battery. In this research the power source is random and so the inverter input voltage will be highly variable. Chapter 5 will address the variable input case. The following analysis is in response to the last two questions where the apparent voltamperes S_s delivered to the impedance-voltage source $v_\ell(t)$ combination must be computed. Due to the presence of the line source $v_\ell(t)$, the first terms of S_s will resemble equation 4.22. For this case

$$\begin{aligned} v_\ell(t) &= V_m \cos(\omega_m t - \alpha) \\ &= V_{\ell_1} \cos(\omega_m t - \alpha) \qquad \text{(rms)} \end{aligned} \tag{4.26}$$

where $v_{\ell_1} = V_m/\sqrt{2}$

Writing equation 4.20 at the transformer secondary and accounting for its nonideal frequency response by the incorporation of frequency-dependent phase shift components yields

$$\begin{aligned} V_{PWM}(t) = V_{s1} \cos \omega_m t &+ \sum_p V_{cp} \cos[(2p-1)\omega_c t - \psi_p] \\ &- \sum_p \sum_q V_{opq} \cos[(2p-1)\omega_c t \pm 2q\omega_m t - \psi_{opq}] \\ &+ \sum_p \sum_q V_{epq} \cos[2p\omega_c t \pm (2q-1)\omega_m t - \psi_{epq}] \end{aligned} \tag{4.27}$$

where $V_{PWM}(t) = n\, V_{a-a'}(t)$ and the coefficients have rms values of (Photo of spectrum is given in Figure C.3b.)

$$V_{s1} = {}^{nV_s}/_{\sqrt{2}} \quad \text{when } K=1$$

$$V_{cp} = {}^{4nV_s}/_{(\sqrt{2}\pi(2p-1))}\ J_0[(2p-1)\pi/2]$$

$$V_{opq} = (4nV_s \cos[(p+q)\pi])/(\sqrt{2}\pi(2p-1))\ J_{2q}[(2p-1)\pi/2]$$

$$V_{epq} = (4nV_s \cos[(p+q)\pi])/(2\sqrt{2}\pi p)\ J_{2q-1}(p\pi)$$

With the voltage on either side of the connecting impedance known, the current injected into the utility can be computed. The voltage $V_{PWM}(t)$ and $v_\ell(t)$ are shown in Figure 4.16. The current $i_\ell(t)$ is given as

$$\begin{aligned} i_\ell(t) = {} & [V_{s1}\cos\omega_m t - V_{\ell_1}\cos(\omega_m t-\alpha-\theta 1)]/|Z1| \\ & + \sum_p \frac{V_{cp}}{|Z_{cp}|}\cos[(2p-1)\omega_c t - \psi_p - \theta_{cp}] \\ & - \sum_p\sum_q \frac{V_{opq}}{|Z_{opq}|}\cos[(2p-1)\omega_c t + 2q\omega_m t - \psi_{opq} - \theta_{opq}] \\ & + \sum_p\sum_q \frac{V_{epq}}{|Z_{epq}|}\cos[2p\omega_c t \pm (2q-1)\omega_m t - \psi_{epq} - \theta_{epq}] \end{aligned} \qquad \textbf{(4.28)}$$

Where the subscript 1 refers to fundamental components

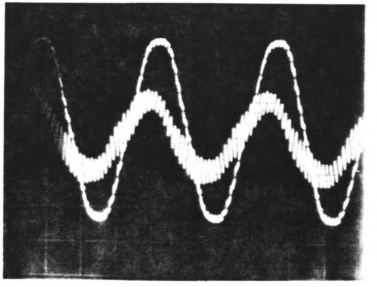
Z1=R+jX

$$Z_{cp} = R+j(2p-1)PX,\ p=1,2,\ldots$$

$$Z_{opq} = R+jh_oX,\ h_o\varepsilon\{[(2p-1)P\pm 2q];\ p,q=1,2,\ldots\}$$

$$Z_{epq} = R+jh_eX,\ h_e\varepsilon\{[(2pP\pm(2q-1)];\ p,q=1,2,\ldots\}$$

The current i (t) is shown in Figure 4.17 for a filter Q of 5.8 at the fundamental frequency. The apparent



$$P = 30,\ K = .95,\ Q = \frac{\omega_m L}{R} = 5.8$$

Figure 4.17. Line voltage $V_\ell(t)$ and injected current $i_\ell(t)$.

voltamperes S_s supplied to the impedance and line voltage combination is given by

$$S_s^2 = \left[V_1^2 + \sum_p V_{cp}^2 + \sum_p \sum_q V_{opq}^2 + \sum_p \sum_q V_{epq}^2\right] \quad (4.29)$$

$$X\left[I_1^2 + \sum_p I_{cp}^2 + \sum_p \sum_q I_{opq}^2 + \sum_p \sum_q I_{epq}^2\right]$$

Therefore, S_s will contain a group of identical frequency terms corresponding to real power transfer and reactive voltamperes plus all cross product terms. Equation 4.28 is intractable in its general form. It does illustrate that, unlike the sinusoidal case, the presence of a non-sinusoidal source produces a complicated mix of all the frequency terms present in both the voltage and current. Notice from Figure 4.17 that the line voltage $v_{\ell}(t)$ is also not a pure sinusoid but is corrupted by approximately 4% fifth harmonic. Should these terms be incorporated, the expression for apparent voltamperes becomes even more cumbersome.

In summary, this chapter has introduced the PWM method of dc to ac inversion. The technique of PWM generation based on natural sampling was investigated and results of a practical implementation were presented. Different devices used as switching elements in a bridge topology were examined and their characteristic features described. It was found that circuit inductance has a pronounced affect on switching time and R-C damping circuit behavior. An example was worked to illustrate this effect.

Next the analysis of a PWM inverter was done and results presented for a stand-alone configuration and, finally, in an interconnected mode. It was noted that stand-alone operation is the most amenable to harmonic filtering, whereas interconnection to a low impedance utility imposes the most stringent demands upon filtering. The case of only a series reactor was presented. A more refined approach would include series and shunt tuned harmonic traps.

Finally the voltampere capability was analyzed and it was found that high frequency distortion terms are dominant in the injected power. However, unlike the inverters examined in Chapter 3, these distortion components are at a much higher frequency and thus capable of minimization and elimination.

Chapter 5 will examine the cascade converter, its operation and control. An example and experimental results will demonstrate its ability to control vars and thus power factor--two features the single phase converters analyzed in Chapter 3 were unable to influence.

CHAPTER V

THE CASCADE CONVERTER FOR A VARIABLE SOURCE

5.1. Characteristics of a Variable Source

A voltage-sourced PWM converter tied to the utility line designed for maximum fundamental content, requires modulation depth K near one. The operating policy for this topology converter is to use modulation depth K as the controlled variable in a fast line-voltage tracking controller. In this manner line sags and surges can be followed provided the voltage excursions remain within the allowed 5% tolerance band. Studies [35] on power line disturbances show that these disturbances can be statistically modeled using a Polya density function. Of all total disturbances, sags (line voltage drops below 96 Vrms for 16 ms or longer) comprise 87%. If power failures are included, this fraction rises to 93%. Therefore, utility-conected VSI converters must have line disconnect capability in event of power outage in addition to fast line voltage tracking. As explained in Appendix B, the converter-utility source differential defines the reactive voltampere flow. The ratio of V.S.I. converter dc voltage to the ac line voltage is a measure of reactive power flow.

The second aspect of the operating policy follows from the random input power. Operating modes are then based on a set of desirable objectives. If constant export power is desired then, neglecting conversion losses, the output power must be at the minimum of the power available. For wind machines the available power is that contained in the natural flow of the wind and depends on the air mass density, speed, and blade aerodynamics.

In gusting winds, the minimum power may be quite low while peak values orders of magnitude higher are possible. One possible solution to such source variability is the use of batteries at the interface between the second energy conversion stage, the DC electric generator, and power conditioning equipment. With this approach, a nearly constant power could be supplied to the utility at almost the mean value of the electric power available. This is certainly an improvement as far as constant power export is concerned. The drawback is that electro-chemical energy storage is currently expensive and inefficient. Typical charge discharge efficiencies of lead acid and newer battery technologies range from 60 to 75% [1]. Another strategy is to extract the maximum power from the wind, since the "fuel cost" is zero, and convert this raw power into utility-compatible nearly constant voltage but with highly-variable current. This constitutes the best utilization of an energy source with no fuel cost. As such, overall efficiency would be of secondary importance to power utilization. At present

the utility network represents the most viable means of distributing random power because loads are always present.

The cascade converter is proposed as a topology which can extract maximum power from such variable sources and simultaneously satisfy the utility-side voltage level and power factor constraints. The voltage and current output of a wind driven generator (d-c system) are shown in Figure 5.1. This is typical of present asynchronous wind turbines in which the converter current slope is set based on the selected operating voltage range. In the test system, the voltage range is $100<V<225$. The low limit represents the converter turn on threshold and the upper value the generator limit. The probability of occurance is based on sampling a 35 minute recording every 5 seconds.

The voltage distribution has a linear slope due to the converter input loading whereas the randomness of the wind is apparent in the power distribution. The power, direct current volt amperes at the converter input, is roughly gaussian. The signal mean values have been computed separately and, with small error, $\mu_V \mu_I = \mu_P$. Note that while the output voltage range is less than an octave, the power span is over a decade. This data confirms that wind power is highly variable. For example, on this record the power ramped from 0.75 kW to over 3.1 kW, a change of 2.4 kW, in a 10 second interval! It is interesting to note that for this power distribution, the power is unlikely to remain at any particular value more than 5% of the time.

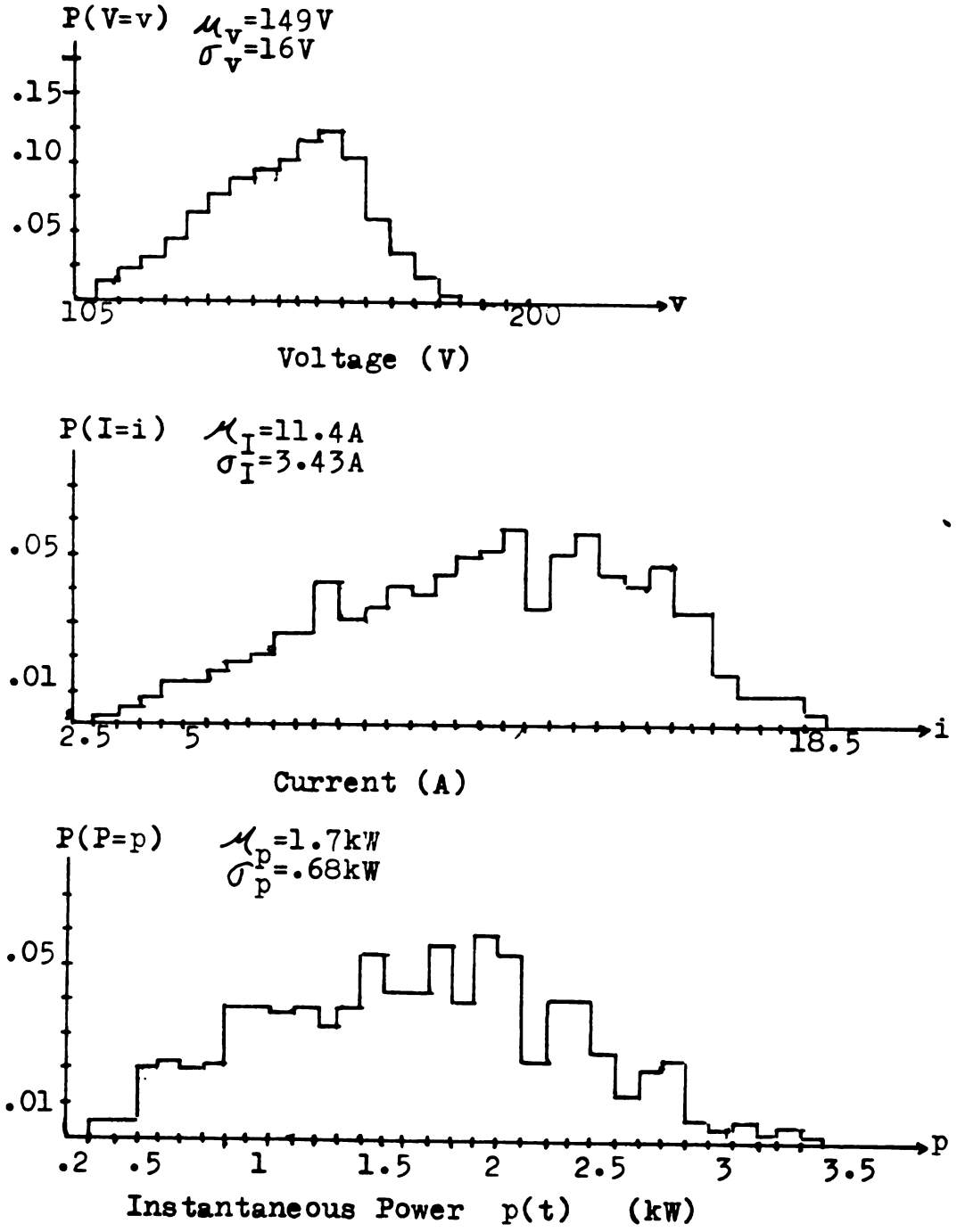


Figure 5.1. Converter input voltage, current, and power density from Dakota 4 kW DC wind generator.

Figure 5.2 is a functional diagram of this cascade converter in which the switch symbols are consistent with those used in Chapter 4. The input is represented as a current source to achieve smooth, low ripple input current. The reasons for this choice are to keep electro magnetic interference (EMI) at a minimum and also to reduce the pulsating torque load on the generator. Minimizing conducted and radiated emissions due to pulsing currents is necessary to control interference with nearby electronic equipment and to provide a low interference environment for the low-level converter circuitry. The input converter has the topology of a "boost" regulator. This is necessary to obtain smooth input current and regulated output voltage greater than the input. The reason for selecting an output voltage above the input is to operate the PWM bridge switches in their most efficient range and to optimize transformer efficiency. As noted in Chapter 4, transformer efficiency is best when losses are about 50% core and 50% copper. This means low transformation (boost) ratios. The PWM bridge controller monitors the line voltage v_1 and generates switching patterns $S_1,\cdots,S_4$ with modulation depth K and frequency ratio P. The major circuits to accomplish this are shown in Appendix C. The input converter monitors the bridge input voltage and adjusts the duty ratio D of the main switch accordingly.

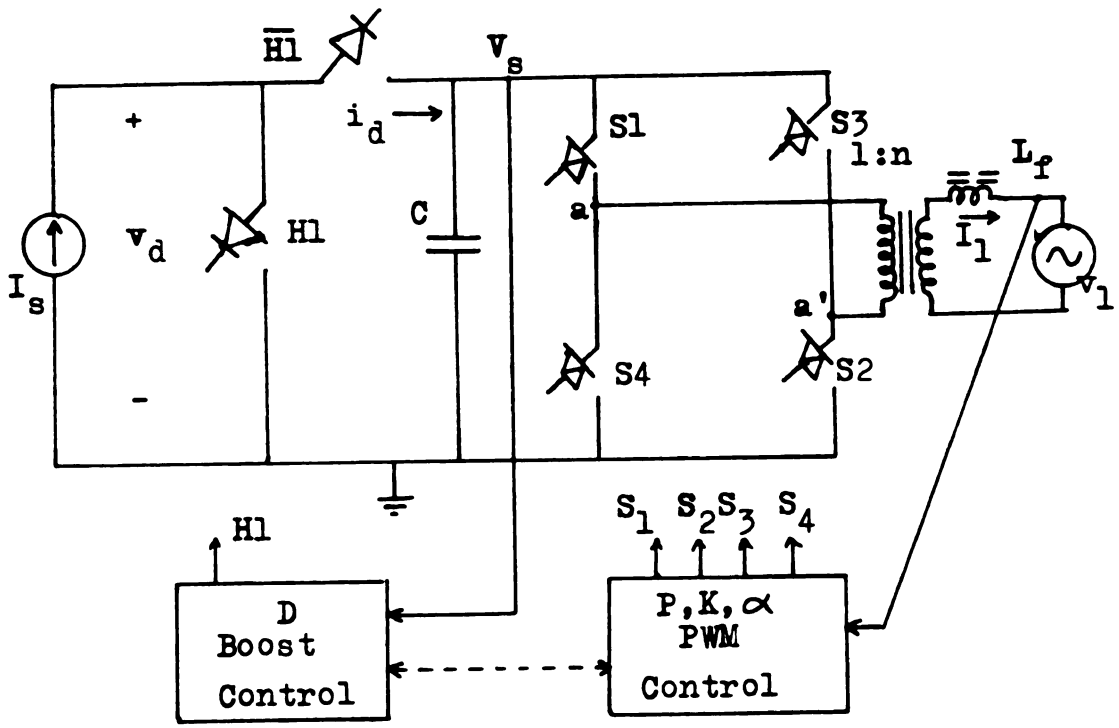
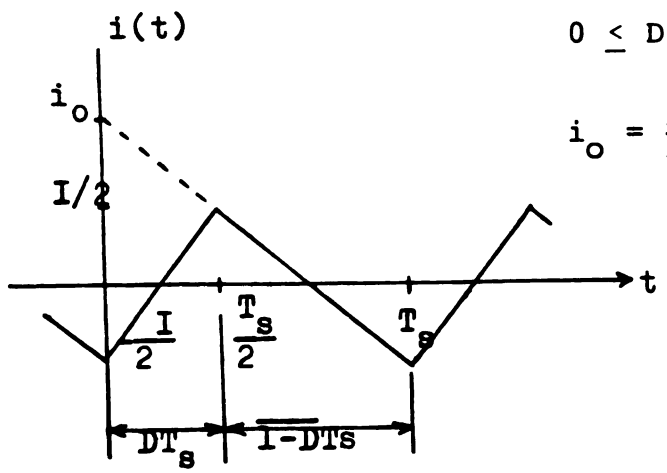


Figure 5.2. Cascade converter topology



$$0 \leq D < 1$$

$$i_o = \frac{\Delta I}{1-D} - \frac{\Delta I}{2} = \frac{\Delta I}{2}\left(\frac{1+D}{1-D}\right)$$

Figure 5.3. Converter inductor current

5.2. Input Voltage Regulation

The general converter theory presented in Chapter 3 can be applied to this converter to derive the relationship between the defined I_s,V_s and dependent i_d, v_d quantities (see Figure 5.2). In this case the existence function for the bipolar junction transistor (BJT) switch is:

$$H1 = D + \frac{2}{\pi} \sum_{n=1} 1/n \sin n\pi D \cos (n\omega_s t) \tag{5.1}$$

where $0<D<1$.

Application of equation 5.1 and $\overline{H1} = 1-H1$ to Figure 5.1 results in the following:

$$v_d = \overline{H1}\, V_s$$

$$v_d = (1-D)V_s - \frac{2V_s}{\pi} \sum_n \left(\frac{\sin n\pi D}{n}\right)\cos n\omega_s t \tag{5.2}$$

$$i_d = \overline{H1}\, I_s$$

$$i_d = (1-D)I_s - \frac{2I_s}{\pi} \sum_n \frac{\sin (n\pi D)}{n} \cos n\omega_s t \tag{5.3}$$

Examination of equation 5.2 shows that the input-dependent quantity v_d includes a ripple voltage containing all harmonics of the switching frequency. The d-c term $(1-D)V_s$ indicates the reason for the title of boost converter or regulator. Since $V_s = v_d/(1-D)$, where $0<D<1$, then V_s is greater than or equal to v_d. Assuming lossless operation, the ratio of dependent to defined quantities are equal, $i_d/I_s = v_d/V_s$.

In a practical converter, the ideal current source I_s is approximated using a voltage source and an inductor L. This practical voltage source V then supplies a nearly constant current I_s through this inductance. In the steady state, the average volt seconds accumulated by L equals zero. This from the net change in magnetic energy ΔW_m being zero. In equation 5.2, the average voltage term will equal the source $(1-D)V_s = V$. The summation term represents voltage harmonics supported by L. In order to support the voltage harmonics across L, its current must change in accordance with Faraday's law. Integrating the harmonic term of eq. 5.2 results in an expression for this current

$$i_L(t) = \frac{2V_s}{L\pi} \sum_n \frac{\sin n\pi D}{n} \int^t \cos n\omega_s t \, dt \qquad (5.4)$$

$$\frac{V_s T_s}{L\pi^2} \sum_n \frac{1}{n^2} (\sin n\pi D) \sin (n\omega_s t)$$

where $\omega_s = 2\pi/T_s$ is the switching frequency.

Equation 5.4 can be recognized as the Fourier expansion of a triangular wave. Consider the waveform shown in Figure 5.3 of a current i(t) with a peak to peak variation of I. From Figure 5.3 this current is found to be

$$i(t) = \begin{cases} \frac{\Delta I}{2_s} t - \frac{\Delta I}{2} & , \ 0 \leq t < DT_s \\ \frac{-\Delta I}{(1-D)T_s} t + \frac{\Delta I}{2}\left(\frac{1+D}{1-D}\right), & DT_s \leq t < T_s \end{cases} \qquad (5.5)$$

where the d-c component of i(t) has been omitted. The Fourier series representation of i(t) in Figure 5.3 will have as coefficients $\Delta I/(D\pi^2(1-D))$ and harmonics which decay as $1/n^2$. Therefore, for the peak to peak variation of $i_L(t)$ to equal that of i(t), the following holds:

$$\frac{V_s T_s}{L\pi^2} = \frac{\Delta I}{D(1-D)\pi^2}$$

$$\text{or} \qquad \Delta I = \frac{(1-D)V_s DT_s}{L} = \frac{VDT_s}{L} = \frac{VSI}{L} \tag{5.6}$$

Here V.S.I. is defined as the volt second integral of the input voltage supplied to the inductance L.

In the same way, the expression for dependent current i_d supplied to the output contains an average term $I_d = (1-D)I_s$. This is the load current demand in terms of the input source current. By duality with the above analysis, the harmonic current components can be shunted from the load by the incorporation of a shunt capacitor C at V_s in Figure 5.2. This done, the capacitor voltage will assume an average value of V_s and its ripple voltage will be complementary to the expression for i(t) in eq. 5.5. That is, replace ΔI with ΔV and interchange the time intervals. Integrating the harmonic term of equation 5.3 allows the dual to eq. 5.6 to be derived for ΔV as

$$\Delta V = \frac{(1-D)I_s DT_s}{C} = \frac{I_d DT_s}{C} \tag{5.7}$$

The two equations, 5.6 and 5.7, can be used to size the input series inductance and output shunt capacitance. So for a given input ripple current, i.e., the harmonic current due to semiconductor switching that is low enough to minimize input generated interference, requires that L be sufficiently large. The critical value of L,L_c, is that value for which $i_L(t=T_s) = 0$. Any further reduction in the value of L below L_c results in discontinuous input current. This situation is to be avoided in the cascade connected converter.

$$L_c = \frac{V_{MAX} D_{MAX} T_s}{\Delta I} \quad \text{Henry} \tag{5.8}$$

Similarly from eq. 5.7 the output voltage ripple in the steady state is a function of load current I_d and shunt capacitance C. Since $I_d = V_s/R_L$ then the capacitance is given as the reciprocal of load resistance and fractional output ripple $\Delta V/V_s$.

$$C_{min} = \frac{D_{MAX} T_s}{R_L\left(\frac{\Delta V}{V_s}\right)} \quad \text{Farad} \tag{5.9}$$

As an application of the above derivations, a lab converter was designed to operate under the following conditions. The switching frequency f_s of 15 kHz is a compromise between switching efficiency and audio interference. The triangular current in L causes corresponding changes in magnetizing force which generates sound in the audio band due to the magnetostriction of the ferrite core. Let $D_{MAX} =$

and assume a maximum regulated voltage V_s of 40V. If ΔI is 3% of I_s, eq. 5.8 gives L_c as 4.3 mH for V_{MAX} input of 20 volts. A loaded ripple in V_s of 0.25% requires a capacitor of several thousand μF. The resulting circuit is shown in Figure 5.4 and details are presented in Appendix C.

The circuit in Figure 5.4 can be analyzed on an energy basis during each switching period T_s under steady state operation. In steady state, the current $i_s(t)$ is as shown in Figure 5.3 with a d-c component I_s added. The capacitor voltage $v_c(t)$, as noted, is the dual of equation 5.5. During transients the magnetic and electric energy storage become unbalanced until steady state at which point $W_e \doteq \pm 1/2 C V_s \Delta V$ and $W_m \doteq \pm 1/2 L I_s \Delta I$ such that $\Delta W_e = \Delta W_m = 0$ over each interval T_s.

The energy dissipation can be accounted for by considering the dissipative elements r_p, Q_1, and D1. Diode D1 is a fast recovery rectifier (FRD) in series connection for current $i_d = (1-D)I_s$. Assume a diode forward voltage of V_f for D1. The energy dissipated due to this diode forward voltage is

$$W_D = V_f I_s (1-D) T_s \tag{5.10}$$

The series resistance r_p accounts for the finite source resistance plus the winding resistance of the inductor L. The current through r_p is continuous so that its energy loss is

$$Wr_p = \left(I_s^2 r_p + \frac{(\Delta I)^2}{12} r_p \right) T_s \tag{5.11}$$

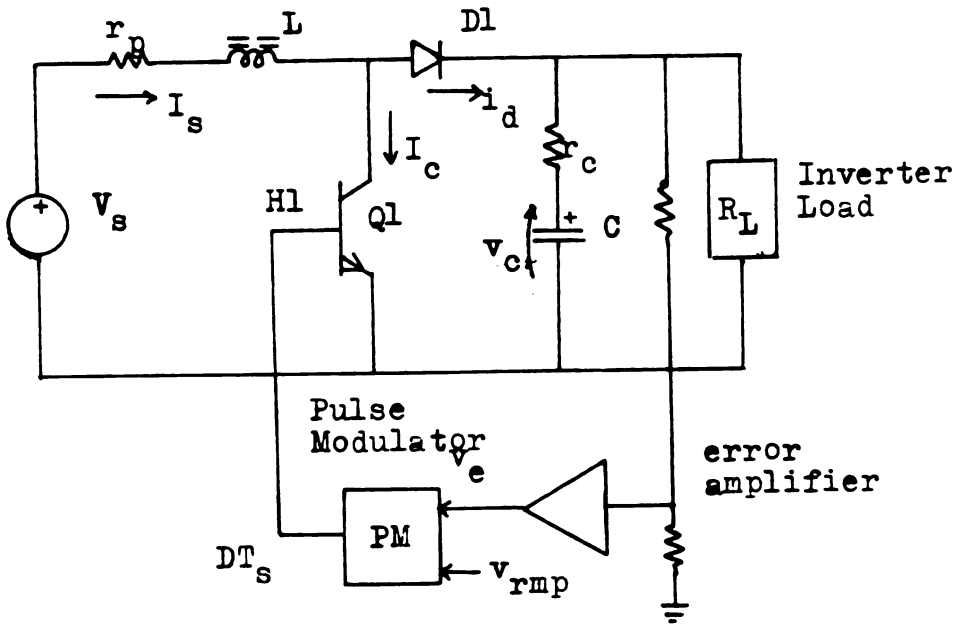
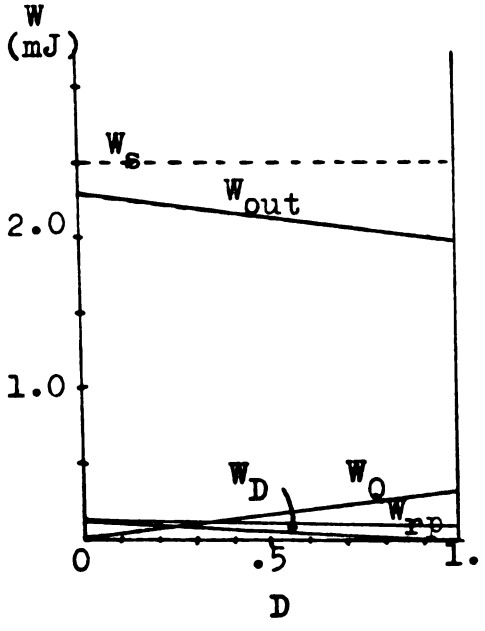


Figure 5.4. Input regulating converter



T_s	67μs
V_s	15V
I_s	2.5A
L	4.35mH
C	4700μF
r_p	.3 ohm
V_f	.8V
$V_{CE(SAT)}$	1.2V

Figure 5.5. Converter energy loss components

where $\Delta I = VDT_s/L$ from eq. 5.6, and so

$$Wr_p = \left[I_s^2 r_p + \frac{1}{12}\left(\frac{VT_s}{L}\right)^2 r_p D^2\right] T_s \qquad (5.12)$$

The input energy supplied by the source V during each switching interval T_s is

$$W_s = VI_sT_s \qquad (5.13)$$

The transistor loss components are due to its on-state loss plus the switching loss. If the switching loss is taken as 5% of the energy being switched and the transistor has saturation voltage $V_{ce(sat)}$,

$$W_Q = \int_0^{DT_s} V_{ce(sat)} \cdot i_c(t)dt + .05DW_s \qquad (5.14)$$

$$= \left[I_s V_{ce(sat)} + .05VI_s\right]DT_s$$

The total energy dissipated is the superposition of the individual energy loss terms. Using eqs. 5.10, 5.12, and 5.14, $W_{LOSS} = W_D + W_r + W_Q$. The interesting features of the energy loss function versus duty ratio D, $W_{LOSS}(D)$, is that the diode loss drops linearly for increasing D while the transistor loss increases linearly. The series resistor r_p loss is constant neglecting current ripple ΔI. These equations are plotted versus D in Figure 5.5. along with the input energy W_s for the given operating conditions. With transistor Q1 reverse base drive and collector RC damping, the measured energy loss during turn-off was 4.8% of the input energy per period.

The observed switching waveforms for Q1 and D1 are shown in Figures 5.6 and 5.7 respectively. In Figure 5.6 the transistor collector current I_c and collector to emitter voltage V_{ce} are shown. The energy dissipated each switching cycle is the result of the overlap and finite slopes of these two waveforms. For the inductor value given, the current ripple is very small and $i(t) \doteq I_s$ such that input current is nearly constant. The ringing in the voltage waveform is due to lead inductance. The total switching interval from the start (10% V_s) of collector voltage rise to finish of collector current decay (10% I_s) is 1μs. In comparison, the collector current turn on occurs in about 400 ns as shown in the lower trace of Figure 5.7. The top trace of Figure 5.7 illustrates the recovery characteristics of the fast recovery diode (FRD, a 1N3893). Reverse recovery time t_{rr} is defined as the elapsed time from the forward current passing through zero in the negative direction until it recovers to 10% of its maximum negative excursion I_{RM}. Refer to Figure 5.8 for a definition of these terms. The recovery time is a function of forward current I_F and is circuit dependent [19]. FRD's with less than 400V rating use gold or platinum diffusion to reduce carrier lifetime and hence recovery time. A fast recovery is necessary if diode switching losses are to be minimized. As Figure 5.8 shows, the reverse charge Q_R is returned back to the transistor switching side of the converter. A further improvement in switching is realized with an

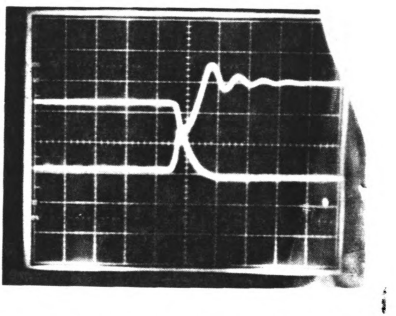
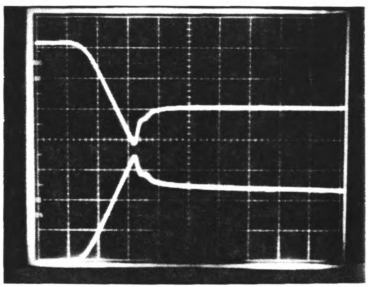


Figure 5.6. BJT switching waveforms.



time .2 μs/cm

I_F 2.2A IRM 1 A t_A .12 μs S .67

dI/dt 10 A/μs t_{rr} .24 μs t_B .08 μs

Figure 5.7. Fast recovery diode switching waveforms.

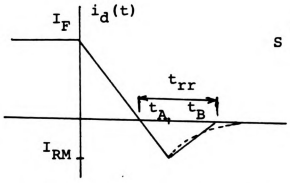


Figure 5.8. FRD characteristics defined.

epitaxial version of the FRD and still better performance with a Schottky rectifier [19]. However, current Schottky diode voltage ratings less than 100V so that its applications are limited.

It was reported above that the theoretical gain of the boost converter is given as $(1-D)^{-1}$. In the practical implementation this is not realized, especially as D approaches unity. In fact at D=1 this gain is zero. This is apparent from Figure 5.4 because, in this case, Q1 is continuously on. The practical gain can be assessed by modeling the converter as a d-c transformer with losses. Modeling the converter as an ideal transformer using the techniques of circuit averaging results in the sketch shown in Figure 5.9. The dissipative circuit elements are modeled to account for internal loss mechanisms. Because this circuit is non-linear, classical circuit analysis techniques cannot be applied. Linear circuit theory will yield an expression for the voltage transfer function V_s/V which has the characteristic form of the actual response. The deviation from true response will increase as D approaches unity. In the limit, the llinear circuit theory model will be totally in error.

The response $V_s(D)$ of the circuit model given in Figure 5.9 can be arrived at by using energy balance. The output energy per switching interval must equal the source energy minus internal losses.

$$W_0 = I_d V_s T_s = (V_s^2/RL)T_s \tag{5.15}$$

$$W_s = VI_s T_s$$

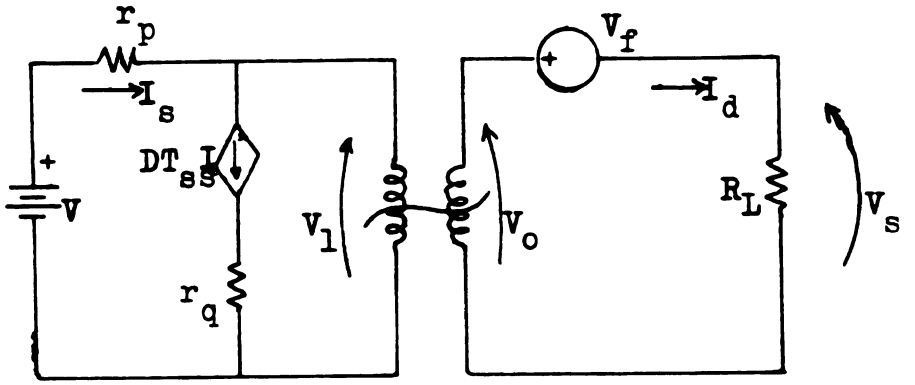
$$W_{DISSIP} = \left[I_s^2 r_p + (DI_s)^2 r_q + (1-D)I_s V_f\right]T_s \tag{5.16}$$

$$W_0 = W_s - W_{DISSIP}$$

This last equation can be solved for V_s in terms of the circuit parameters given an operating current I_s as

$$V_s^2 = \left[VI_s - I_s^2 r_p - (DI_s)^2 r_q - (1-D)I_s V_F\right]R_L \tag{5.17}$$

The lossless converter (η=1) gain is $V(1-D)^{-1}$ so that for a given D, a source current $I_s = V_s^2/VR_L$ or $I_s = V/R_L\,(1-D)^{-2}$ is required. If for each value of D, the current drawn by the ideal converter is calculated, then the voltage gain of the realizable converter may be found. Substituting this current into eq. 5.17 gives the actual V_s as a function of load R_L. This technique is applied using the element values given in Figure 5.10 to arrive at the plots for $V_s(D)$ with parameter R_L. For a converter with higher efficiency, the plots will all move closer to $V(1-D)^{-1}$. At the high end of the scale the input current I_s becomes very large, so that internal converter voltage drops affect the ideal transformer reducing V_o. At a limiting value of D, D_c>.7 in Figure 5.10, the right hand side of eq. 5.17 becomes negative. When $D>D_c$, the converter in its open loop mode collapses.



$$V_o = V_s + V_f$$
$$V_l = (1-D)V_o$$

Figure 5.9. Converter circuit averaged model

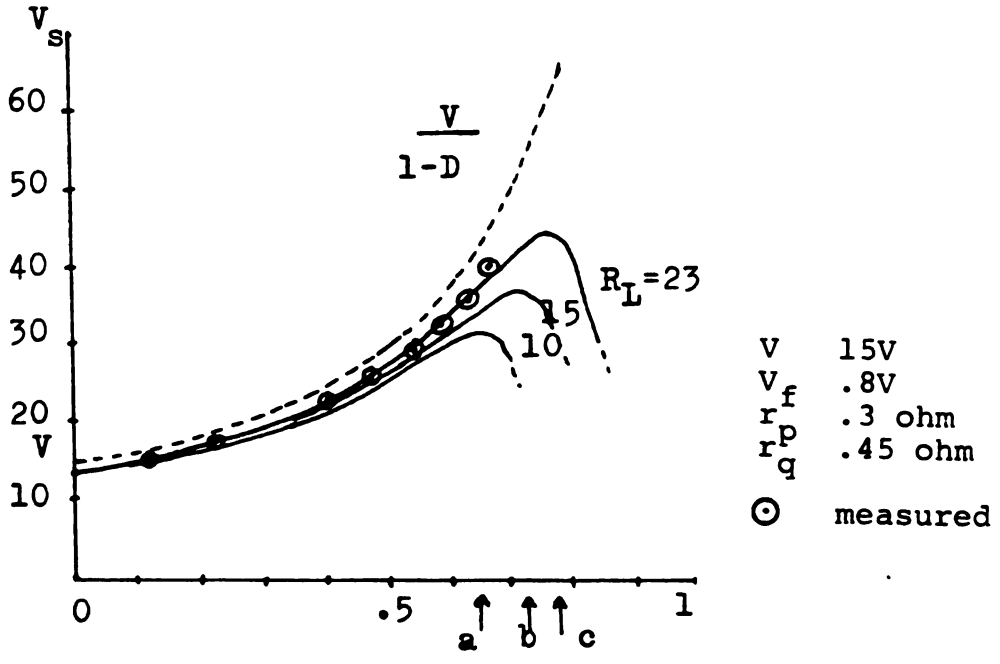
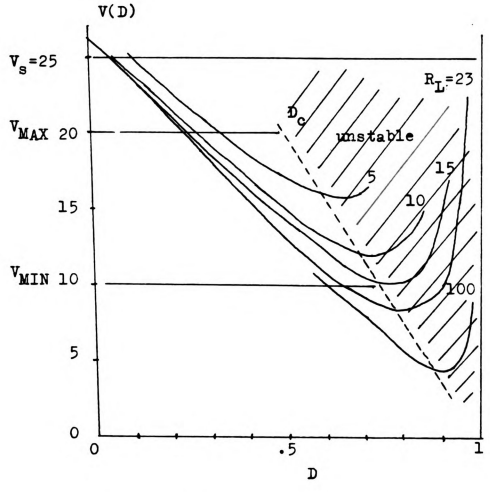


Figure 5.10. Converter response as a function of duty ratio

The points along the D-axis labeled a,b, and c represent the critical values of D,D_c at which the slope of the voltage transfer characteristic $V_s(D)$ is zero. That is, for a given load R_L, operating points on the right of D_c are unstable. In a closed loop feedback controller, this represents the point of zero phase margin. Of course any additional lag introduced by the feedback will cause instability at duty ratios less than D_c. It is well known in converter theory [28] that the analysis technique, state space averaging, is not capable of identifying these critical values of D. It is here shown that the application of energy balance to the non-linear converter circuit model does predict this very critical performance limitation.

Laboratory measurements agree with the plots shown in Figure 5.10. The goal of this converter is to translate the variable voltage of a stochastic source as shown in Figure 5.1 to a regulated level. In order to achieve a closed loop stable output for a given regulated level V_s, it is necessary that the input voltage $V+\hat{v}$ not exceed an octave in variation. Then the maximum input voltage V_{MAX} would coincide with the point D=0 and V_{MIN} would be such that $D<D_c$. As shown in Figure 5.11, the usable portion of $V_s(D)$ is that for which $V_s/V<3$. This is so because when v(t) goes to V_{MIN}, the source power is reduced by nearly an order of magnitude as shown in Figure 5.1. Thus by reducing the converter load, a higher transformation ratio may be maintained with the converter always in its stable region.



r_p .3 ohm
r_q .45 ohm
V_f .8V
V_s 25V regulated

Figure 5.11. Regulating range of the converter.

The variable which controls loading is α, the phase lead relative to the utility line of the PWM converter. Let this loading be represented as $R_L(\ )$. The regulated voltage given by eq. 5.17 can now be expressed as

$$V_s^2 = \left(\frac{V}{1-D}\right)^2 - \frac{VV_f}{(1-D)} - \frac{V^2}{R_L(\alpha)(1-D)^4}(r_p + r_q D^2) \qquad (5.18)$$

The critical value of duty ratio D_c can be obtained by setting the derivative of $V_s^2(D)$ equal to zero. The result is a cubic equation in D_c:

$$0 = 2V(1-D_c)^2 - V_f(1-D_c)^3 - \frac{4Vr_p}{R_L(\alpha)} - \frac{2D_c(D_c+1)Vr_q}{R_L(\alpha)} \qquad (5.19)$$

This can be reduced to a quadratic in D_c by recognizing that $V_f << V$. With this simplification, the expression for D_c is

$$0 = V(1-D_c)^2 - \frac{2Vr_p}{R_L(\alpha)} - \frac{D_c(D_c+1)Vr_q}{R_L(\alpha)} \qquad (5.20)$$

The solution of eq. 5.20 can only be the root for which $0<D_c<1$, thus

$$D_C = \left(\frac{1+\frac{r_q}{2R_L(\alpha)}}{1-\frac{r_q}{R_L(\alpha)}}\right) \pm \sqrt{\left(\frac{1+\frac{r_q}{2R_L(\alpha)}}{1-\frac{r_q}{R_L(\alpha)}}\right)^2 - \left(\frac{1-\frac{2r_p}{R_L(\alpha)}}{1-\frac{r_q}{R_L(\alpha)}}\right)} \qquad (5.21)$$

Using the parameter values given in Figure 5.10, this equation predicts the critical duty ratio values

$$D_{ca} = .67 \qquad D_{cb} = .72 \qquad D_{cc} = .77$$

which are slightly high due to neglecting the effect of V_f.

Equation 5.21 shows the importance of designing the regulating converter for maximum efficiency. This is because D_c approaches unity only when the switching transistor loss, represented by r_q, is very small relative to the connected load. The equivalent source resistance and inductor winding resistance r_p must also be very small relative to R_L. The techniques used in this research to minimize r_q and r_p were to use a fast driver with reverse base drive I_{B2} on Q1 in addition to collector snubbing and to wind L using Litz wire. This multiple strand insulated winding for L is needed to reduce the winding dynamic resistance due to "skin effect" at these high switching frequencies. A good treatment of this effect is to be found in Chapter 8 of [45]. As already mentioned, the diode forward voltage V_f is chosen in a trade off with switching speed, i.e., minority carrier lifetime.

5.3. State Space Analysis of the Regulator

The remaining consideration is to find the duty ratio d(t) time response. Examination of Figure 5.4 shows that this converter resembles a low pass filter. As will be shown below, the response d(t) exhibits this same low pass characteristic although with non-minimum phase. Based on the theory presented in Chapter 3, the converter of Figure 5.4 can be redrawn to highlight the changes for each subinterval of T_s. Since this converter is constrained to operate in its continuous conduction mode, two discrete

operating intervals are manifested. During subinterval DT_s, transistor Q1 conducts charging L. Simultaneously its auto-complementary switch D1 is reverse blocking with C discharging into R_L. In the subinterval $(1-D)T_s$, exactly the reverse is true. These two modes of Figure 5.4 are drawn as Figure 5.12 a, and b.

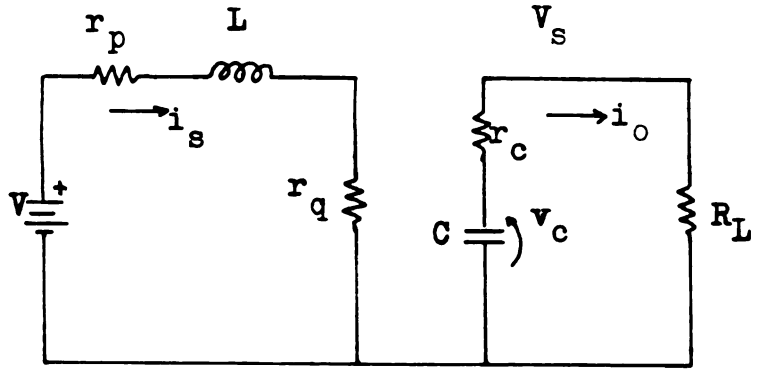
The following analysis is that of state space averaging [38] to obtain the averaged frequency response of the networks in Figure 5.12. The diode D_1 forward voltage is omitted since its only effect here is that of an independent source in series with R_L. The capacitor series resistance is included. Laboratory measurements for this equivalent series resistance were performed by charging C to its operating voltage and monitoring its voltage and current during discharge through a thyristor in place of R_L. This capacitor is actually the parallel combination of two individual electrolytics for which $r_c = 0.12$ ohms. The lead inductance calculated during this test was about 3 H. This inductance is not present in the model shown in Figure 5.12 to avoid complication due to second-order effects.

Using the inductor current i_s and the capacitor voltage v_c as state variables, the state and output equations for Figure 5.12 can be put in the form

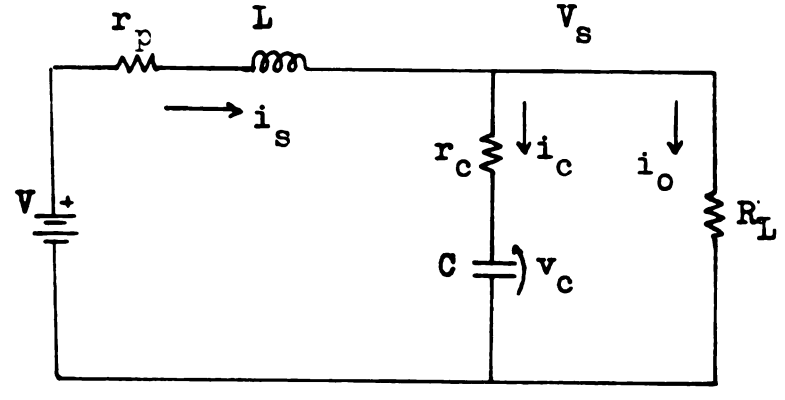
$$\dot{\underline{X}} = A\underline{X} + bu \qquad \text{State Eq.}$$

$$y = C^T\underline{X} \qquad \text{Output Eq.} \qquad (5.22)$$

where $\underline{x} = \begin{bmatrix} i_s \\ v_c \end{bmatrix}$, $u = v$, and $y = V_s$.



a) During interval DTs



b) During interval (1-D) T_s

Figure 5.12. Converter operating modes during continuous conduction

For the network in Figure 5.12a, Kirchhoff's voltage law results in

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} -\frac{r_p+r_q}{L} & 0 \\ 0 & \frac{-1}{C(R_L+r_c)} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 1/L \\ 0 \end{bmatrix} V \qquad (5.23)$$

$$V_s = \begin{bmatrix} 0 & \frac{R_L}{R_L+r_c} \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \end{bmatrix}$$

which has the form

$$\dot{X}_1 = A_1X_1 + b_1u$$
$$y = C_1^TX_1$$

where $nT_s<t<(n+D)T_s$.

In this form the vector subscript is not to be confused with the state variable subscript but only to identify the state equation for a particular time interval. Similarly, Kirchhoff's voltage and current law applied to Figure 5.12b result in the state and output expressions during that interval as

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} -\left(r_p/L + \frac{R_Lr_c}{(R_L+r_c)L}\right) & -\frac{R_L}{(R_L+r_c)}\frac{1}{L} \\ \frac{R_L}{C(R_L+r_c)} & -\frac{1}{C(R_L+r_c)} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 1/L \\ 0 \end{bmatrix} V \qquad (5.24)$$

$$V_s = \begin{bmatrix} R_L\left(1 - \frac{R_L}{R_L+r_c}\right) & \frac{R_L}{R_L+r_c} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}$$

and is of the form

$$\dot{X}_2 = A_2X_2 + b_2u$$

$$Y = C_2{}^TX_2$$

where $(n+D)T_s<t<(n+1)T_s$.

A check of the eigenvalue location for matrices A_1 and A_2 indicate that the eigenvalues are real and distinct. In both cases the eigenvalue due to the series resistor-inductor is large indicating a small time constant, and hence a rapid response. The second, the output circuit eigenvalue, is small in agreement with its long time constant. Inspection of equations 5.23 and 5.24 show that during interval DT_s, the output is strictly a function of v_c, whereas during interval $(1-D)T_s$ the source current i_s adds a contribution dependent upon r_c.

The state space averaging procedure is essentially that of making a straight line approximation of the transition matrices $\exp(A_{1,2}t)$ and is valid only for frequencies less than $1/2f_s$. Assume that during the n^{th} switching period $d_n(t)$ is constant. In this case the resulting expression will be linear:

$$\dot{\underline{X}} = [d_n(t)A_1 + (1-d_n(t))A_2]\underline{X} + [d_n(t)b_1 + (1-d_n(t))b_2]u$$

$$y = [d_n(t)C_1{}^T + (1-d_n(t))C_2{}^T]\underline{X} \qquad (5.25)$$

Substituting eqs. 5.23 and 5.24 into 5.25 gives the state space averaged model

$$\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\end{bmatrix} = \begin{bmatrix} -\left(\frac{r_p}{L} + d_n(t)\,\frac{r_q}{L} + d_n'(t)\,\frac{R_L r_c}{(R_L+r_c)L}\right) & -\frac{d_n'(t)R_L}{(R_L+r_c)L} \\ \frac{d_n'(t)R_L}{(R_L+r_c)C} & -\frac{1}{C(R_L+r_c)}\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix} + \begin{bmatrix}1/L\\ 0\end{bmatrix}V \tag{5.26}$$

$$V_s = \left[d_n'(t)R_L\left(1 - \frac{R_L}{R_L+r_c}\right) \quad \frac{R_L}{R_L+r_c}\right]\begin{bmatrix}x_1\\ x_2\end{bmatrix}, \quad d_n'(t) = (1-d_n(t))$$

which is of the form given in equation 5.22. In reality, the duty ratio d in any given switching period nT_s is not constant. In fact $d_n(t)$ may be a function of both the state $\underline{X}$ and input U. If so, equation 5.26 will be nonlinear. Assume a perturbation in both $d_n(t)$ and the input V(t) as $d_n(t) = D+\hat{d}_n(t)$ and $V(t) = V+\hat{v}(t)$. The state will then experience a perturbation $\underline{x}(t) = \underline{X}+\hat{\underline{x}}(t)$ so that the output equation becomes $V_s(t) = V_s+\hat{V}_s(t)$. Substituting these expressions into equation 5.25 results in a perturbed state which may be thought of as a steady state portion $A\underline{X}+bV$. A component due to input variation $A\hat{x}+b\hat{v}$ and one due to duty ratio variation $[A_1-A_2]\underline{X}+(b_1-b_2)V]\hat{d}(t)$. The remaining component is a nonlinear, second-order expression $[(A_1-A_2)\hat{d}\hat{\underline{x}} + (b_1-b_2)\hat{d}\hat{V}]$. This second-order component can be neglected for small perturbations. The output equation also contains these same component terms. These are: steady state $C^T\underline{X}$, state variation $C^T\hat{\underline{x}}(t)$, a duty ratio variation term $(C_1^T-C_2^T)\underline{X}\hat{d}(t)$, and a second-order term $(C_1^T-C_2^T)\hat{x}\hat{d}(t)$.

The above assumption of small perturbations and neglecting the second-order terms, results in a linearization of the nonlinear, state space averaged, perturbed system. As shown in [28], the duty ratio d(t) perturbation during interval nT_s, $\hat{d}_n(t)$, can be expressed as a series of narrow pulses which exist at intervals $(n+D)T_s$, i.e., at the switching instants. With this representation as impulse functions $\hat{d}(t) \doteq \sum_{-\infty}^{\infty} \hat{d}_n(t)T_s\,\delta(t-\overline{n+D}T_s)$, the duty ratio perturbations can be thought of as the result of sampling a continuous time function $\hat{u}(t)$ that matches $\hat{d}_n(t)$ at the sampling instants. How one proceeds from this point on determines whether the end result will be a state space averaged, discrete model, or a sampled data model of Figure 5.4.

Rewriting equation 5.22 in terms of these perturbations results in the state perturbation and output equation:

$$(\underline{X}+\hat{\underline{x}})(t) = (A\underline{X}(t)+bV) + (A\hat{\underline{x}}(t)+b\hat{v}(t)) + [(A_1-A_2)\underline{X}\hat{d}(t) + (b_1-b_2)V\hat{d}(t)] + (A_1-A_2)\hat{\underline{x}}(t)\hat{d}(t) + (b_1-b_2)\hat{v}(t)\hat{d}(t) \tag{5.27}$$

= steady state + input variation + duty ratio variation + nonlinear second-order terms.

$$y(t) = C^T\underline{X}(t) + C^T\hat{\underline{x}}(t) + (C_1^T-C_2^T)\underline{X}(t)\hat{d}(t) + (C_1^T-C_2^T)\hat{\underline{x}}(t)d(t) = V_s + \hat{v}_s(t)$$

= steady state + state variation + duty ratio variation + nonlinear second-order terms.

The state space averaged model approximates equation 5.27 as a linear time invariant system. As shown above, eq. 5.27 is neither linear nor time invariant. To remove time dependence from eq. 5.27 it is necessary that $\hat{V}(t)$ be a slowly varying function of time relative to the switching period T_s. Second, that the duty ratio driving term in the form of delta pulses is assumed constant during T_s. The linearization step has neglected the second-order term. These approximations introduce error into the model such that a determination of stability as frequencies approach the switching frequency f_s cannot be made. The utility of the method is that Laplace transform techniques can be applied.

The discrete model starts with equation 5.27 but does not make the assumption that the duty ratio perturbation d(t) u(t) is a continuous time function. Instead, it describes the small signal converter behavior during a single instant of any switching interval T_s. The main objective of discrete modeling is to predict stability and is not concerned with variation of the input. Hence, the assumption $\hat{v}(t) = 0$ is made in equation 5.27. The resulting expression is then integrated over a complete interval T_s with $\hat{d}(t)$ given as an impulse function. Care must be taken during this integration so that the impulse is confined to the proper subinterval, else causality will be lost. The resulting difference equation is both linear and shift invariant so that the Z-transform may be applied. In this

manner the behavior of duty ratio in response to a perturbation in state can be determined.

Finally, the sampled data model results from essentially neglecting the time varying aspects of equation 5.27 and using average values in their place while retaining the representation of $\hat{d}(t)$ as a string of delta pulses. The use of average values for duty ratio is consistent with the straight line approximation made in the state space averaged model (i.e., using only the constant and linear terms of a Taylor series representation of the transition matrix). The retention of duty ratio perturbation as a delta function then places this model midway between state space averaging and discrete modeling. This model, however, relies on the sampled Laplace transform in contrast to the continuous Laplace transform used in the first model.

This thesis is concerned with how the input regulator responds to inputs from a variable source with voltage and current distributions similar to those shown in Figure 5.1. The stability of this regulator was assessed in Section 5.2 using energy balance technique which related converter loss mechanisms to a critical duty ratio D_c of equation 5.21. In the following analysis the method described above as state space averaging is used to develop the output to input and output to duty ratio variation transfer functions. These, in turn, are used to obtain a complete closed loop model of this converter.

Removing the steady state contribution (equation 5.23) from equation 5.27 gives an expression for the dynamics due to perturbations of both state and input, i.e. the a-c model.

$$\dot{\hat{\underline{x}}}(t) = A\hat{\underline{x}}(t)+b\hat{v}(t)+[(A_1-A_2)\underline{X}+(b_1-b_2)V]\hat{d}(t)$$

$$\hat{v}_s(t) = C^T\hat{\underline{x}}(t)+[(C_1{}^T-C_2{}^T)\underline{X}]\hat{d}(t) \qquad (5.28)$$

Taking the Laplace transform of equation 5.28, combining and factoring results in expressions for the two desired transfer functions:

$$\hat{V}_s/\hat{V}(s) = C^T[SI-A]^{-1}b \qquad (5.29)$$

$$\hat{V}_s/\hat{d}(s) = C^T[SI-A]^{-1}\{(A_1-A_2)\underline{X}(s)+(b_1-b_2)V(s)\}+[C_1{}^T - C_2{}^T]\underline{X}(s)$$

Substituting the appropriate matrices from equations 5.23, 5.24, and 5.26 into 5.29 results in the scalar transfer functions

$$\hat{V}_{s/\hat{V}}(s) = \frac{\frac{D'R_L}{L}\left(1 - \frac{R_L}{R_L+r_c}\right)\left[S + \frac{1}{r_cC}\right]}{\left\{s^2+\left(\frac{r_p}{L} + D\frac{r_q}{L} + \frac{D'R_Lr_c}{(R_L+r_c)L} + \frac{1}{C(R_L+r_c)}\right)S + \frac{1}{C(R_L+r_c)}\left[\frac{r_p}{L}+D\frac{r_q}{L}+\frac{D'R_Lr_c}{(R_L+r_c)L}\right] + \left(\frac{D'R_L}{R_L+r_c}\right)^2\frac{1}{LC}\right\}} \qquad (5.30)$$

and,

$$\hat{V}_{s/\hat{d}}(s) = \frac{-\left(\frac{R_L}{R_L+r_c}\right)^2\left\{\frac{X_1}{SC} + \left(r_p+Dr_q+\frac{D'R_Lr_c}{R_L+r_c}\right)\frac{X_1}{LC} - \frac{D'R_L}{R_L+r_c}\cdot\frac{X_2}{LC}\right\}}{\det[SI-A]} \qquad (5.31)$$

Examination of eq. 5.30 reveals that the output to input voltage transfer function is essentially low pass. It is interesting to note the presence of a left half plane zero due to the capacitor series resistance. This expression can be put into a form which provides more insight into the converter behavior. Define an effective inductance $L_e = L/D'^2$, which is inversely proportional to the complementary duty ratio and assume $R_L >> r_c, r_p, r_q$. This yields

$$\hat{V}_s/\hat{V}(s) = \frac{\omega_n^2/D'}{S^2 + 2\zeta\omega_n S + \omega_n^2} = G_V(S) \qquad (5.32)$$

Here the following derivations have been used.

$$\lim_{r_c \to 0} \left[\frac{D'R_L}{L} \left(1 - \frac{R_L}{R_L + r_c}\right)\left(S + \frac{1}{r_c C}\right) \right] \Bigg|_{S=0} \rightarrow \lim_{r_c \to 0} \left(\frac{D'R_L^2}{LC(R_L + r_c)^2} \right) \rightarrow \frac{D'}{LC} \rightarrow \omega_n^2/D'$$

$$\omega_n^2 \triangleq 1/L_e C \quad \text{and} \quad \zeta = \frac{1}{2R_L}\sqrt{L_e/C}.$$

If equation 5.18 is solved for $1/1-D = 1/D'$ and this, in turn, substituted into the numerator of equation 5.32, it can be seen that at higher boost levels the complementary duty ratio decreases. The corresponding effect on the low pass filter performance is a reduction of the bandwidth and increased damping. Hence, higher frequencies present in the input voltage experience increased attenuation along with enhanced damping--both desirable attributes of a regulator.

Using the definitions given in eq. 5.32 in eq. 5.31 results in it being reduced to

$$\hat{V}_{s/\hat{d}}(s) = \frac{-\left[S - \frac{\omega_n^2 C}{D'}\frac{X_2}{X_1}\right]\frac{X_1}{C}}{S^2 + 2\zeta\omega_n S + \omega_n^2} = G_d(s) \qquad (5.33)$$

The response of output voltage to a perturbation in duty ratio is again second order. The numerator shows the presence of a right hand plane (RHP) zero, $S_z = \omega_n^2 C/D'(X_2/X_1)$ which is dependent on the state. At zero frequency, the variation in output voltage is related to the duty ratio perturbation by the gain factor V_s/D'. This is consistent with intuition in that low values of D' (high levels of V_s) are accompanied by greater ripple in the defined quantity. Also apparent is the non-minimum phase behavior of output voltage to perturbations in duty ratio. Furthermore, this RHP zero moves in response to the converter input impedance

$$S_z = \frac{\omega_n^2 C}{D'}\left(\frac{X_2}{X_1}\right) = \frac{V}{LI_s} = \frac{R_{IN}}{L} \qquad (5.34)$$

As equation 5.34 shows, the converter input time constant determines the zero location. Since, in the ideal converter $R_{IN} = D'^2 R_L$, the RHP zero is load dependent. In the unloaded converter this zero is at infinity and moves toward zero as loading is increased. With the PWM inverter described in Chapter 4 as the load on this input regulator, a step change in lead angle α causes this RHP zero to jump. Response tests of duty ratio to a step change

in load are given in Appendix C along with various feedback schemes.

The closed loop transfer function model for the regulator is given in Figure 5.13. In this figure only small signal behavior about the operating state is shown. Using the development given in Appendix C for the effective feedback gain $H_e(s)$ using a gain only or single pole roll-off error amplifier, the closed loop performance of Figure 5.13 is

$$\hat{v}_s/\hat{v}(s) = \frac{G_V(s)}{1+G_d H_e(s)} \tag{5.35}$$

where $H_e(s) = -aK_mK_a$.
In this expression a is that fraction of the regulated voltage compared with the reference voltage. Variation of a sets the regulated voltage V_s to a defined level. Parameter K_m is the transfer function of the pulse modulator and K_a is the error amplifier low frequency gain. The regulator low pass nature results in a loop bandwidth of eq. 5.35 that is quite small.

The above description of regulator instability can also be developed using the describing function technique. In the above analysis the pulse modulator hysteresis was neglected. Although itself an approximation, validity of the describing function technique is ensured by the low pass response of the regulator. Using this technique, the pulse modulator phase lag due to hysteresis can be modeled. From this the nonlinear element describing function is developed

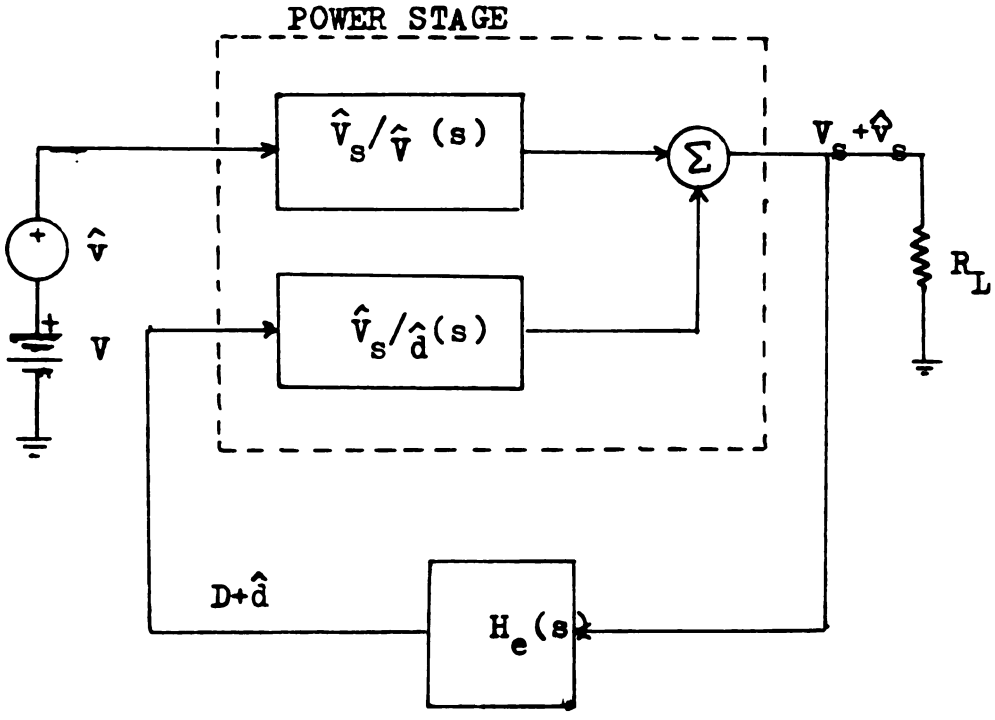


Figure 5.13. Converter closed loop configuration

using the fundamental terms only of its Fourier representation. This done, any critical frequency (limit cycle period and amplitude) can be identified as the intersection with the plant Nyquist plot by the critical loci (negative reciprocal of the nonlinear element describing function). The end result, however, will be the same as above. The gain must be low.

When the control law shown functionally in Figure 5.13 is used as the boost controller in Figure 5.2 the large deviations of inverter input current $i_d(t)$ cause this regulator to become unstable. The results of experimental variation of gain K_a of equation 5.35 showed that to decrease the sensitivity of the regulator to this large ripple current i_d, K_a had to be very low. Low gain will effectively offset the advantages of incorporating a regulator stage. For now if the input voltage V is random, then similar variations appear in the "regulated" output V_s. This has been shown in equation 5.32. If the input to output transfer function $G_V(s)$ of equation 5.32 is defined as the audio susceptability, i.e., the tendency to become an amplifier, then what is needed is for $G_V(s)$ to exhibit high attenuation.

Figure 5.14 gives the closed loop audio susceptability for this regulator with output feedback. As gain is increased, audio susceptability improves but the phase slope increases rapidly due to magnitude peaking. If the regulator output time constant is reduced, the audio susceptabil-

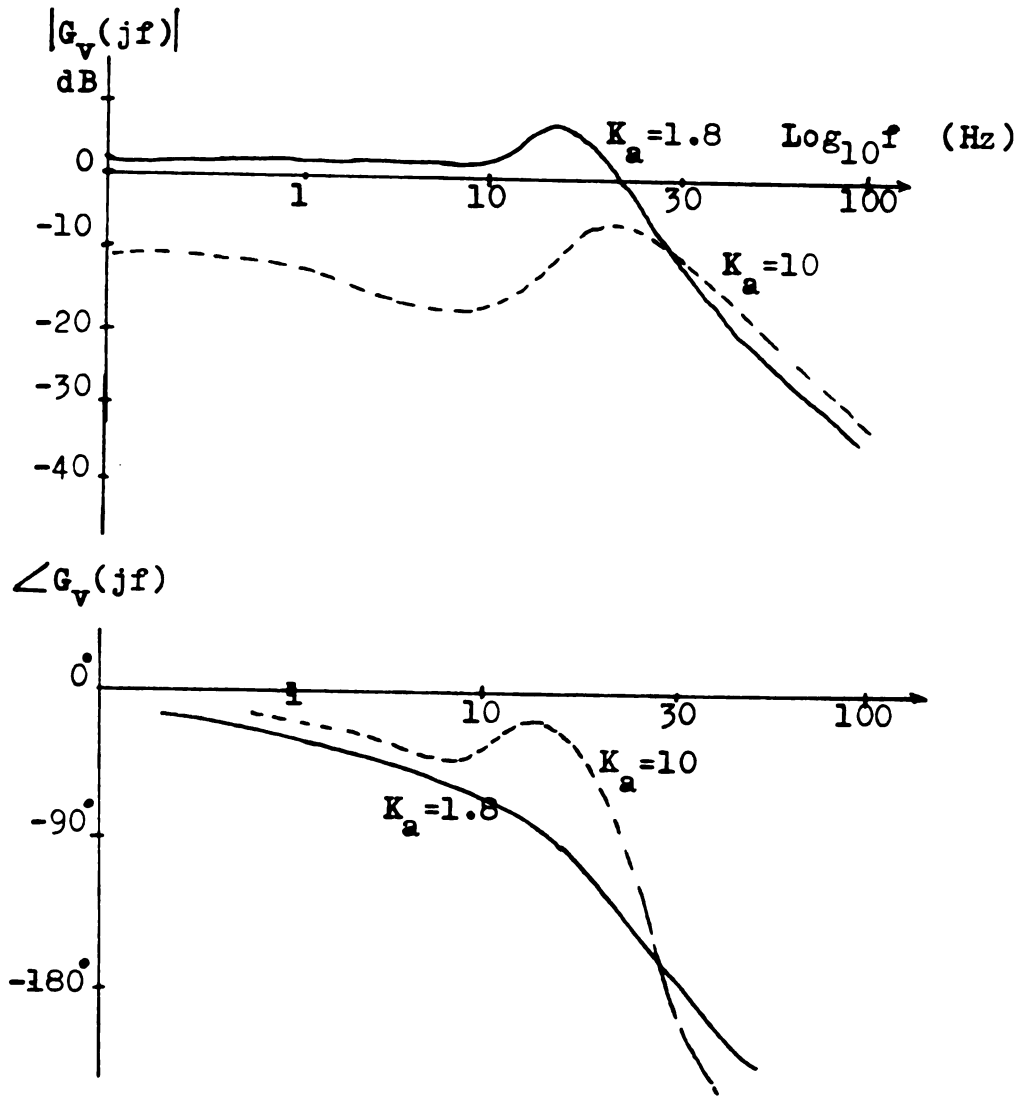


Figure 5.14. Regulator audio susceptability with output feedback.

ity becomes worse for a given gain. The data for Figure 5.14 was obtained by modulating a laboratory power supply with a variable sinusoidal source. This supply fed the boost regulator and load combination.

An experimental control circuit was discovered which is capable of stabilizing this boost regulator with a connected PWM inverter and driven by a random source. Figure 5.15 contains the modifications to Figure 5.4 needed to implement this multiple feedback controller. The auxiliary generator v_g is a sinusoidal source for audio susceptability tests and a low frequency noise generator for random input measurements. The controller acts as an analog voltage programmer converting the dc supply V_i into a voltage controlled voltage source (VCVS) of 200 VA capability. The basic boost regulator remains unchanged except that the connected load is now the PWM inverter. The output voltage is sensed via an attenuating network R10 and R11 in conjunction with error amplifier AR1. A current transformer (CT) senses the input current I_s. This signal is processed by amplifier AR2 and summed to the ramp and pedestal signal at summer AR3. These feedback signals are compared at comparator AR4. The comparator contains hysteresis so that the switching instants of D in $d(t) = D+\hat{d}(t)$ are clean. This duty ratio command d(t) controls the on time of switch element Q1 to maintain V_s constant with highly pulsating load current and randomly varying input V .

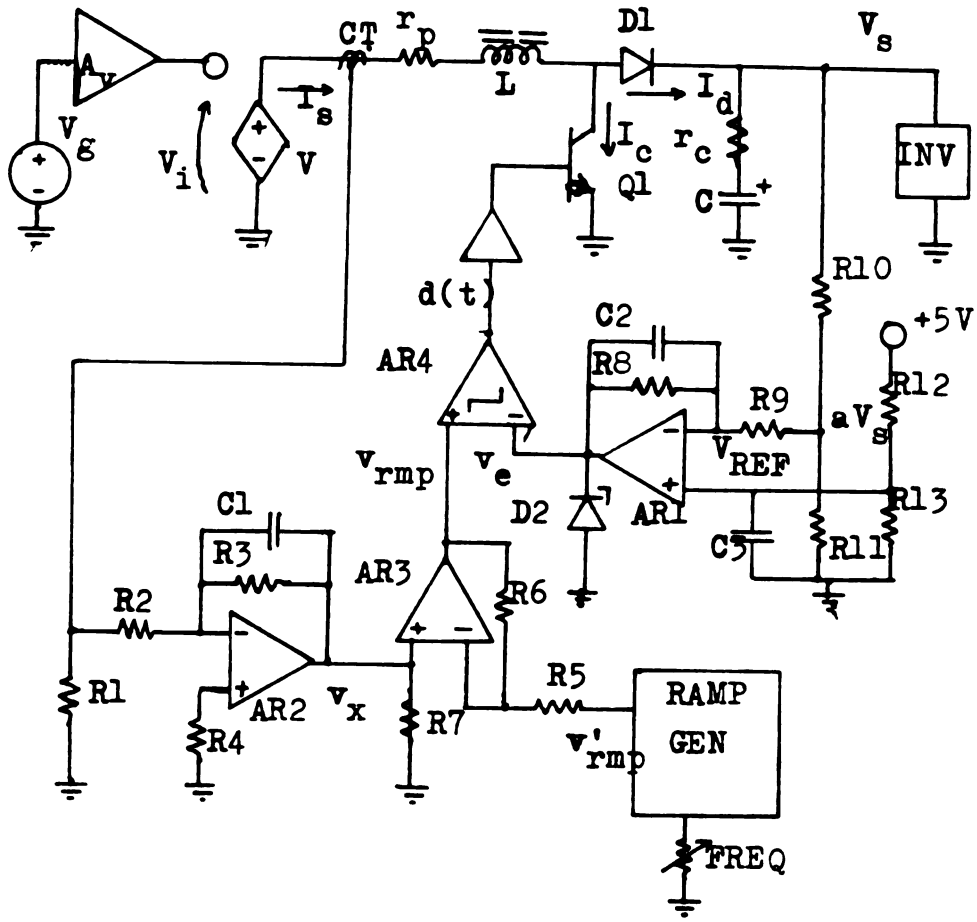


Figure 5.15. Multiple feedback regulator controller.

The analysis of this multiple feedback (MFB) controller follows. With MFB the scalar feedback gain $H_e(s)$ of equation 5.35 becomes a vector feedback gain. Because of multiple control paths to the comparator function (AP4 of Figure 5.15) its transfer function G(s) will appear by itself, as shown in Figure 5.16. The output feedback gain $H_2(s) = V_e/V_s(s)$ is found as follows:

$$V_e(s) = \frac{-K_{dc}}{1+s\tau_2} V_s(s) + \left(\frac{K_{OV}+\tau_2 S}{1+\tau_2 S}\right) V_{REF} \qquad (5.36)$$

where $K_{dc} = a\ R_8/R_9$

$a = V_{REF}/V_{so}$

V_{so} is the nominal value of V_s.

$K_{ov} = 1 + R_8/R_9$

$\tau_2 = C_2 R_8$

and the tilde symbol $\sim$ will be used to distinguish MFB analysis from the output feedback case. Since V_{REF} is fixed, a perturbation in the output results in a change in error voltage of

$$H_2(s) = \tilde{V}_e/\tilde{V}_s(s) = \frac{-K_{dc}}{1+S\tau_2} \qquad (5.37)$$

By circuit design the error voltage $V_e(t)$ is constrained to $-0.7 \leq V_e(t) \leq 4.7$ volts.

The feedback gain $H_1(s)$ can be found from Figure 5.15. The current transformer (CT) loaded 50 ohms resistive has a transfer gain of K_a of 0.1 V/A. Its phase shift is negligible over the bandwidth of the signal processing

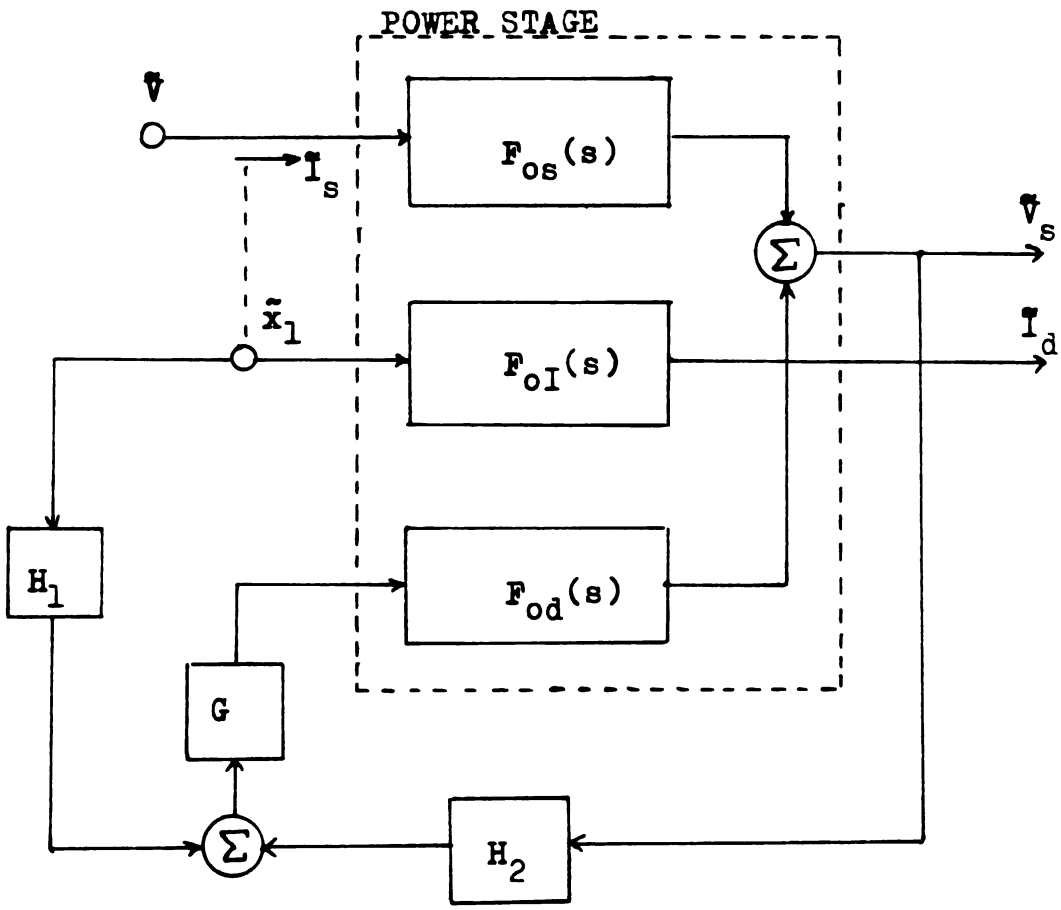


Figure 5.16. Multiple feedback model.

circuitry. The effective feedback gain $H_1(s) = \tilde{V}_{rmp}/\tilde{I}_s(s)$ is determined from

$$\tilde{V}_x(s) = \frac{R3/R2 K_a}{1+S\tau_1} \tilde{I}_s \qquad (5.38)$$

$$\tilde{V}_{rmp}(s) = (1+K_{OI})\, \tilde{V}_x(s) - K_{OI}\, V'_{rmp}(s)$$

where $K_{OI} = R6/R5$

$\tau_1 = C1R3$

yields,

$$\tilde{V}_{rmp}(s) = \frac{K_{ac}}{1+S\tau_1} \tilde{I}_s(s) - K_{OI}\, V'_{rmp}(s) \qquad (5.39)$$

where $K_{ac} = (1+K_{OI})K_a\, R3/R_2$.

Equation 5.39 can be put into the form of a transfer function $H_1(s)$ by recognizing that the periodic time function $V'_{rmp}(t) = V'_{rmp}(t+T_s)$ is very fast with respect to $\tilde{I}_s(t)$. That is, the average value of time function $V_{rmp}(t)$ is modulated by the slowly varying function of time $\tilde{V}_x(t)$.

$$H_1(s) = \tilde{V}_{rmp}/\tilde{I}_s\ (s) = \frac{K_{ac}}{1+S\tau_1} \qquad (5.40)$$

The duty ratio control signal $d(t) = D+\tilde{d}(t)$ at the comparator output is

$$d(t) = \frac{K'_m}{T_s} [\nu_e(t) - V_{rmp}(t)] \qquad (5.41)$$

where K'_m/T_s is the comparator gain obtained, as described in Appendix C, and T_s is the switching period of Q1 in Figure 5.15. The steady state portion of d(t),D is given by the steady state portions of equations 5.36, V_{so} and V_{REF}, and that of equation 5.39, V'_{rmp}. The perturbation in duty ratio d(t) results from the functions given in equations 5.37 and 5.40. In Figure 5.16 the comparator transfer function G(s) neglecting hysteresis is $K'_m/T_s = K_M$. Figure 5.17a and b illustrate the signals given in equation 5.41 for the duration of a single switching period T_s. The function $G(s) = K'_m/T_s = .373\ V^{-1}$ is obtained from Figure 5.17.

The block diagram of Figure 5.16 can be analyzed to obtain the input to output transfer function valid within the low frequency approximations made for the power stage.

$$\tilde{V}_s(s) = F_{os}(s)\,\tilde{V}(s) - F_{od}(s)\,\tilde{d}(s) \qquad (5.42)$$

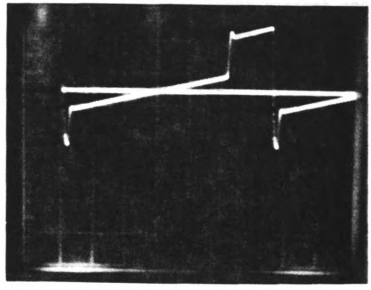
$$\tilde{d}(s) = G(s)\,[\tilde{V}_e(s) - \tilde{V}_{rmp}(s)] \qquad (5.43)$$

With r_c in Figure 5.15 neglected $\tilde{V}_s(s) = \tilde{X}_2(s)$, and since $\tilde{I}_s(s) = \tilde{X}_1(s)$ then using equations 5.37 and 5.40, equation 5.43 becomes

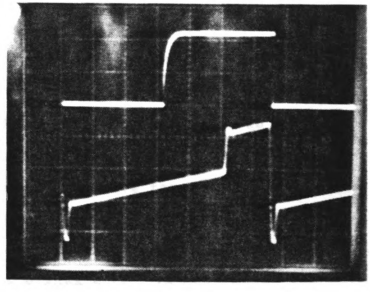
$$\tilde{d}(s) = \underline{H}_e(s)\,\underline{\tilde{X}}(s) \qquad (5.44)$$

where $\underline{H}_e(s) = [-GH_1(s) \quad GH_2(s)]$

and $\underline{\tilde{X}}^T = [\tilde{X}_1(s) \quad \tilde{X}_2(s)]$



a) Comparator input signals $V_{rmp}(t)$ and $V_e(t)$.



b) Comparator output d(t) (top) and $V_{rmp}(t)$ (bottom).

Figure 5.17. Duty ratio controller signals.

Equation 5.44 shows that the control signal d(t) for the MFB case is a function of the regulator input current and output voltage. Substitution into equation 5.42 results in

$$\tilde{V}_s(s) = F_{OV}(s)\,\tilde{V}(s) + F_{OA}(s)\,\tilde{I}_s(s) \qquad (5.45)$$

where

$$F_{OV}(s) = \frac{F_{OS}(s)}{1+F_{od}GH_2(s)}$$

$$F_{OA}(s) = \frac{F_{od}GH_1(s)}{1+F_{od}GH_2(s)}$$

The audio susceptability for the regulator is given as the $F_{OV}(s)$ component. At zero frequency this value is

$$F_{OV}(s)\Big|_{s\to 0} = \frac{1}{D'+G(0)K_{dc}V_{so}} \sim \frac{1}{K_{dc}} \qquad (5.46)$$

where $F_{os}(s)$ is the $G_r(s)$ of equation 5.32 and $F_{od}(s)$ is the $G_d(s)$ of equation 5.33 with steady state values $X_2 = V_{so}$ and $X_1 = I_{so}$.

Using the MFB method the regulator is stable for high values of d-c gain. This is very important when the input voltage varies over an octave range or more. Figure 5.18 shows the results of an audio susceptability test for this regulator for two values of duty ratio D'. This figure can be compared with Figure 5.14. In that case, low gains were needed to insure stability with the inverter load. Consequently its audio susceptability was marginal to non-existent. The most pronounced difference between these two control methods is the substantial phase lead provided with

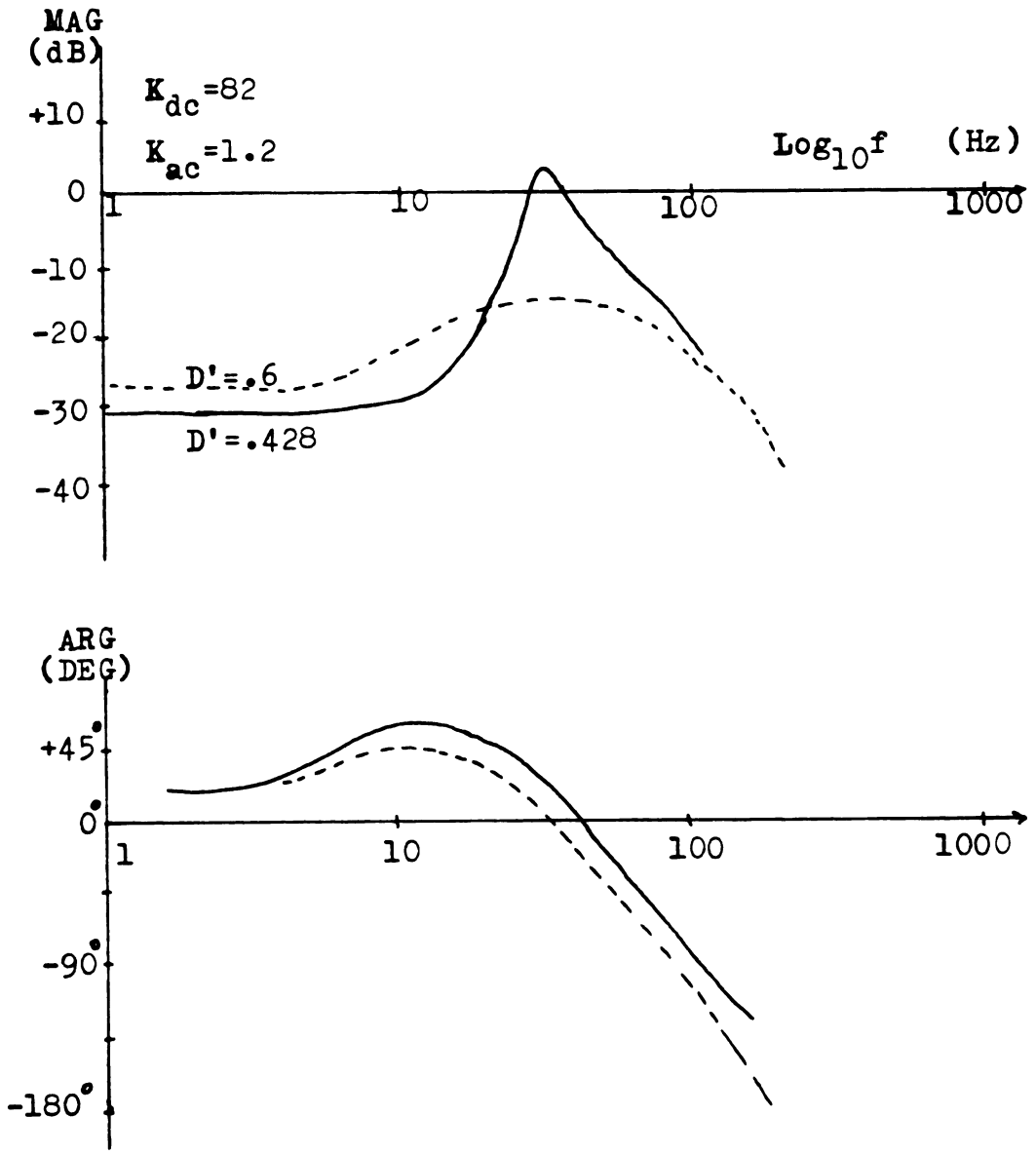


Figure 5.18. Audio susceptability of MFB regulator.

MFB. With input from a wind generator having significant spectral content below 3 Hz, the regulator functions in its region of maximum rejection. The results obtained in Chapter 4 on the PWM inverter confirm the stability provided by the MFB controller.

The extension of the ideas presented in the chapter to the multiphase case can be accomplished by proper phasing of the bridge switching functions. Referring to Figure 5.2, a three-phase inverter is realized by incorporating an additional power pole into the bridge. The only modification is to displace the pole switching patterns by $360^{o}/N$ where N is the number of phases. These changes require no modification to the PWM controller.

5.4. Source Power Tracking Using the Cascade Converter

For this inverter to function with variable power input its phase lead α relative to the utility voltage $v_{\ell}(t)$ must be controllable. The bridge controller of Figure 5.2 provides this function by applying a filtered replica of this line voltage having digitally controlled phase lead to a phase locked loop. The amount of phase lead will depend upon the filter inductance. Since this reactor must have a gapped core to accommodate the wide range in injected current anticipated, relatively low values of Q will result. Filter Q is defined here as the ratio of reactance to resistance at the fundamental, typical values obtained in the laboratory range from 3 to 6.

The operating policy of a cascade converter in the maximum power tracking mode with a wind generator source is to sample the input voltage and use this information to vary the inverter phase lead. With the lead circuit described in Appendix C, a four bit control word provides 15 discrete steps in power. A microprocessor controller is best suited to perform this control function. By comparing the input voltage sample with a look up value the processor can output a suitable control word to either raise, lower, or leave unchanged the lead angle .

An example will serve to illustrate the means of power transfer that can be achieved using the circuit of Figure 5.2. First consider the simplest case in which the inverter output voltage is assumed sinusoidal. Then case I of Chapter 4 applies so that equation 4.21 can be used to plot real power and reactive voltamperes versus angle using the regulated voltage V_s as a parameter. In order to show the influence of various circuit parameters, the defining relations will be used for V_1 and V . The current I shown in Figure 5.2 can be found:

$$I_\ell(\alpha,t) = R_e\left\{\frac{nKV_s/\sqrt{2}\; e^{j(\omega_m t+\alpha)} - V_m/\sqrt{2}\; e^{j\omega_m t}}{|Z|e^{j\theta}}\right\} \qquad (5.47)$$

$$= I_1 \cos\left[\omega_m t + \delta(\alpha) - \theta\right] \; A_{rms}$$

where

$$I_1 = \sqrt{\frac{\left(nKV_s/\sqrt{2}\right)^2 + V_m^2/2 - \; . \; nKV_s V_m \cos \alpha}{R^2 + \omega_m^2 L^2}}$$

$$\delta(\alpha) = \tan^{-1}\left[\frac{nKV_s \sin \alpha}{nKV_s \cos \alpha - V_m}\right]$$

This relation for line current is plotted in Figure 5.19 for the system parameters given. In this example the conditions are such that up to 10 kW of power can be transferred. Operation into a 240 V_{rms} utility by the wind driven source having a voltage distribution similar to that in Figure 5.1 requires that V_s be set at 200 V_{DC}. This means the regulator duty ratio need not exceed point a in Figure 5.10. Regulator stability is insured and further, since the power available from the wind turbine is low when the output voltage is low, then power throughput at high duty ratio will also be low. Conversely, when wind turbine output reaches rated power, its voltage rises so that regulator duty ratio decreases and efficiency improves as illustrated in the plot for W_{out} of Figure 5.5. Moreover, operation of bipolar transistors at this level of V_s allows the devices to be 50% derated on sustaining voltage and maintain low switching dissipation. This requires reverse bias drive since the circuits are inductive. Therefore reliable operation can be insured. As noted previously, the transformer turns ratio can be kept less than 2 so that transformer losses can be minimized. In this case n=1.7

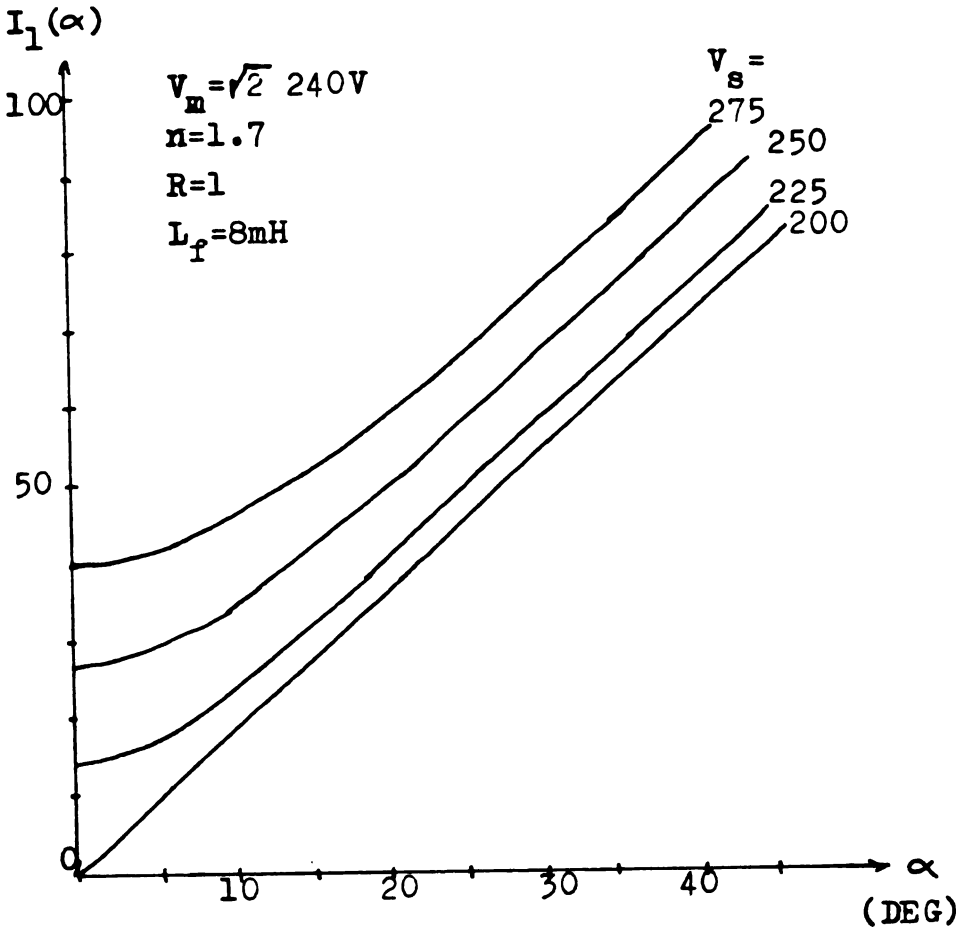


Figure 5.19. Line current I_ℓ as a function of α with parameter V_s

matches the PWM fundamental component to the utility when operating at modulation depth K near unity. Note from Figure 5.19 that line current for alpha zero is a strong function of V_s (hence the ratio of converter d-c port voltage to a-c port voltage). An interesting result is that when V_s drops below its rated value of 200V the resulting plots nearly overlay those for V_s greater than 200V by the same difference. What happens is that the angle $(\delta(\alpha)-\theta)$ of this current varies from a lagging to a leading value relative to the utility (taken as a reference phasor in this case). For a given filter Q, the angle θ is a constant. However, $\delta(\alpha)$, the angle of the filter voltage V_z with respect to V_ℓ, is a function of lead angle α given V_s. Figure 5.20 illustrates this dependence. Note in particular how rapidly $\delta(\alpha)$ approaches 90^o as α is increased for the case V_s=200. When V_s is reduced below its nominal value the angle of V_z is always greater than 90^o.

The behavior described in both Figures 5.19 and 5.20 can be used to augment Figure 4.15 for additional insight into this type of converter topology behavior. The phasor diagrams of Figure 5.21 describe the sequence for V_s less than, equal, and greater than nominal for a given lead angle. As can be seen from these sketches, it is possible to select a value of V_s given a value of utility voltage V_ℓ such that the angle of I_1 remains near zero. The control angle α can then be advanced in proportion to the power available from the source. It is important to add at this

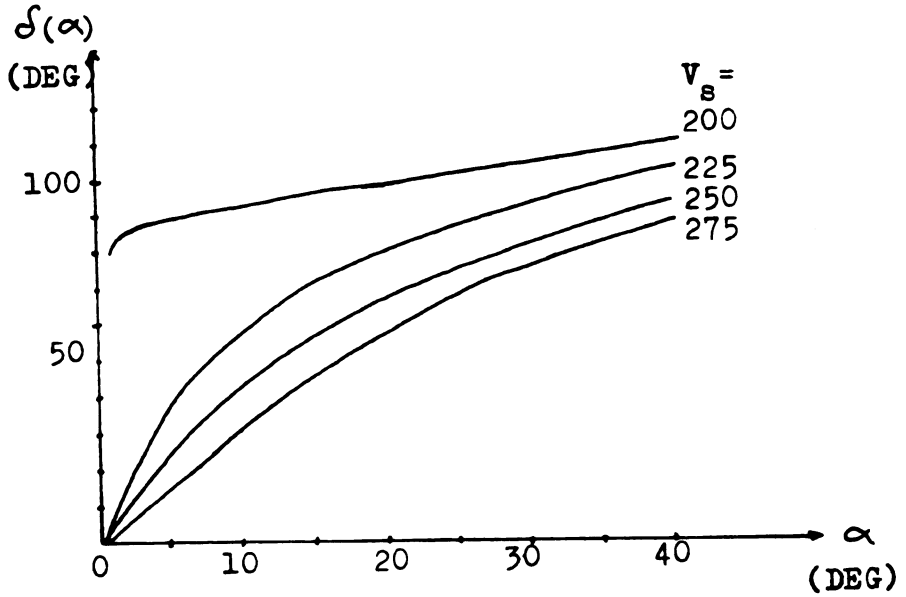


Figure 5.20. Filter voltage V_z angle as a function of α with parameter V_s

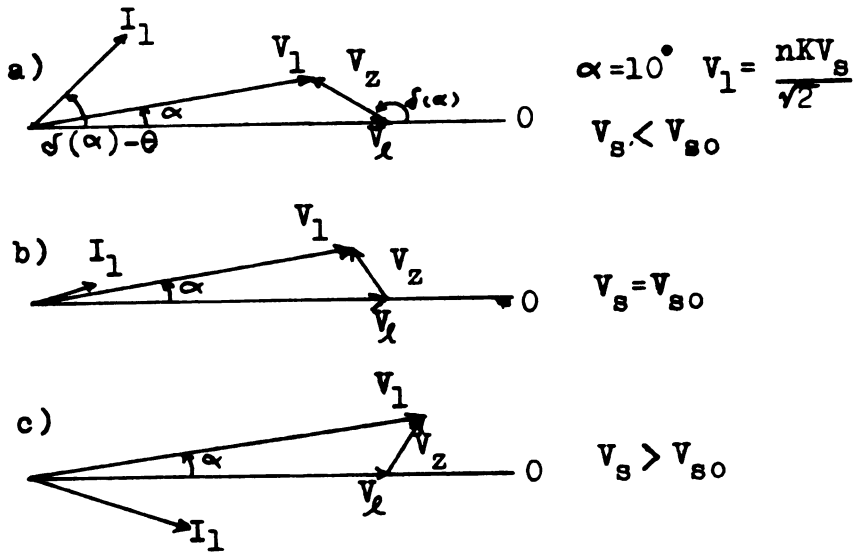


Figure 5.21. Phasor diagram for converter voltages and current

point that it would not be prudent to allow α to become a delay angle. If it did, the reactive voltamperes will increase markedly along with a reversal of power flow through the inverter. The regulator is unidirectional in power flow so that the wind turbine would not be allowed to absorb the power reversal. Consequently the regulated voltage V_s would rise, control of the regulator will be lost, and the wind turbine would run unloaded. The control used for α in this research inhibits this condition from occuring.

Rewriting equation 4.21 as 5.48 allows real power flow as well as reactive voltamperes to be assessed. The real and imaginary parts of equation 5.48 are plotted in Figure 5.22 as a function of α.

$$S(\alpha) = \left[\frac{(nK\,V_s)^2}{2|Z|}\cos\theta - \frac{nKV_sV_m}{2|Z|}\cos(\alpha+\theta)\right] + j\left[\frac{(nKV_s)^2}{2|Z|}\sin\theta - \frac{nKV_sV_m}{2|Z|}\sin(\alpha+\theta)\right] \tag{5.48}$$

With the same parameters given in the above example, raising the filter quality Q to 5 has the following effect. The real power levels P attainable are reduced for a given lead angle α. The corresponding level of reactive voltamperes Q are increased. Therefore a proportionally higher value of link voltage V_s is required. As this dc voltage is increased the behavior is again as depicted in Figure 5.22.

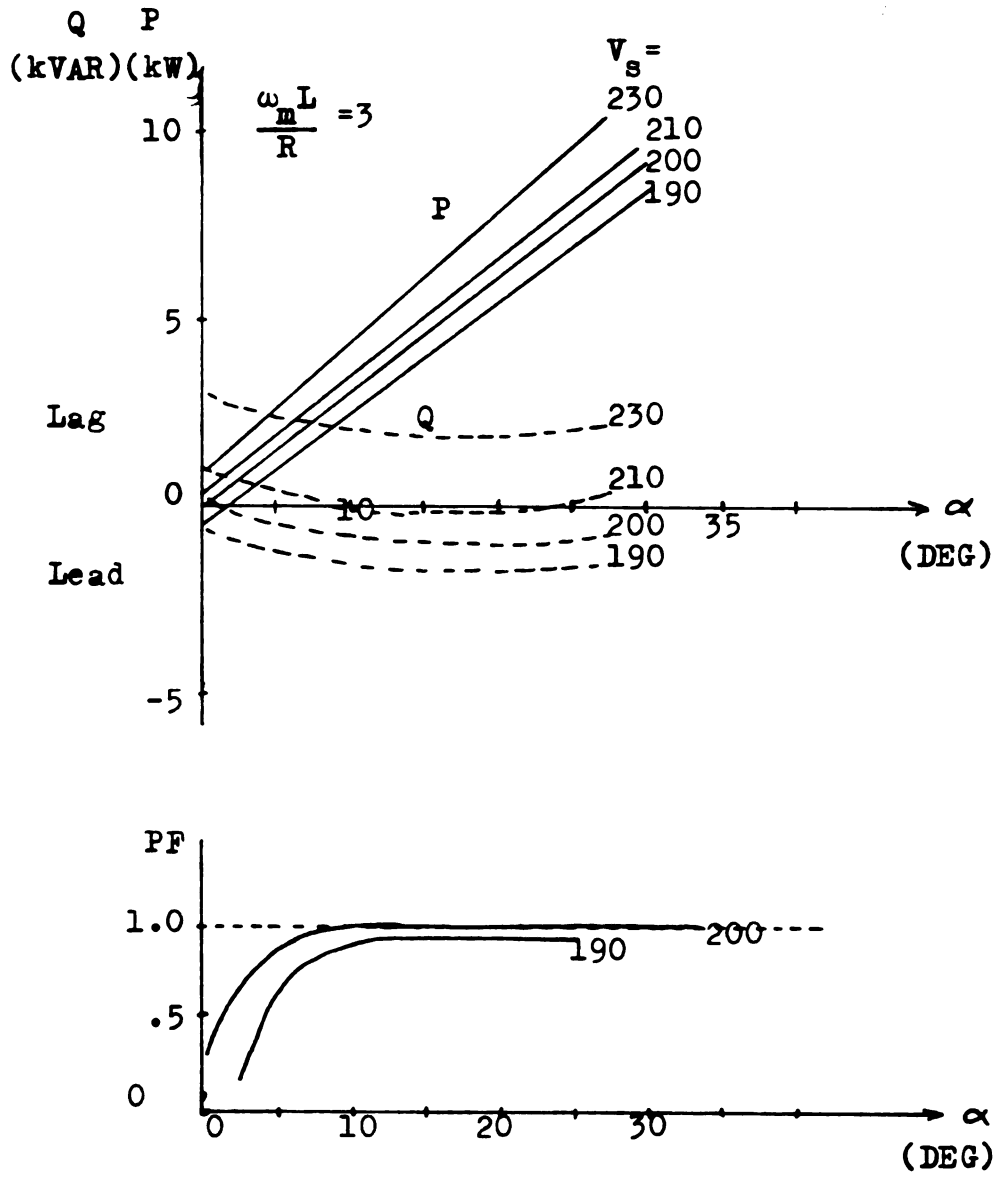


Figure 5.22. Real power P and reactive voltamperes Q versus α and typical power factor.

Figure 5.22 shows that power factor can be optimized by the correct choice of dc link voltage V_g to ac line voltage V_ℓ. This means that for a very extensive range of power level, the reactive power will remain nearly constant. Thus operation at unity power factor or any desired power factor is possible.

In conclusion, this chapter has presented data of an operational DC wind generator showing its highly variable power output over several minutes. The PWM inverter described in Chapter 4 was then cascaded with a boost type d-c converter to regulate the highly variable source voltage such that a-c line reactive voltamperes can be managed. In actual experiments it was found that because of the pulsating load presented to the regulator by this inverter output feedback was insufficient to stabilize it. It was shown that due to internal loss mechanisms the boost converter step-up ratio experiences a load dependent peak beyond which control is not possible. Consequently the control circuitry was modified to include duty ratio range limiting. However, since constraining duty ratio within this range was also insufficient to insure stability a new control scheme was devised which did. Laboratory measurements on this multiple feedback converter show a pronounced phase lead in its audio susceptability relative to the output feedback case. The resulting stability with high loop gain provides a nearly constant regulated output under highly variable input. This chapter concludes with an

example to illustrate the capability of the cascade converter to provide power tracking while maintaining a selectable level of reactive voltamperes.

CHAPTER VI

CONCLUSION

A. Present Practice

This research has explored the conversion of d-c from a highly variable source into utility compatible a-c. The survey presented in Chapter 2 categorized the various conversion schemes. It was found that the availability of high speed power devices has opened the way for high frequency power conditioning methods. The most recent of these being the pulse width modulation (PWM) and high frequency link techniques. Both methods are aimed at active waveshaping of the current. With PWM, a base band filter blocks out the high frequency components. The line injected sinusoidal envelope current appears at this inverter dc port as double frequency sinusoidal current pulses. The merit of this technique is that this current (envelope) is continuous. Field measurements of both the current source (CSI) and voltage source (VSI) converters show that injected current is a high amplitude and short duration (typically one quarter cycle) pulse. Appendices A and B present data showing the high levels of low-order harmonics present in these waveforms. It was found that the CSI outperformed the VSI at higher power because the input current sourcing

inductor of the CSI converter enables current to flow over a greater portion of the a-c cycle.

The high frequency link is essentially the mirror operation. The source current is first shaped into double frequency sinusoidal pulses and then inverted "unfolded" into the ac utility. Two methods for this waveshaping rely on high frequency switching. The key finding is that power must be processed two to three times. By processed is meant some switching operation involving semiconductor devices. However, a source with the variability of a wind generator has not been considered. Most power conditioning research at present involves dc power from photovoltaics. This means the source voltage is a function of solar insolation, array temperature, and type of cloud cover.

The high frequency link concept and its variants, current band control, and current controlled modulator (MC^2) operate at unity power factor to optimize switching efficiency in two of three conversion stages. Being a high frequency process, it requires switching devices capable of handling large amounts of power at frequencies above 10 kHz. This necessitates bipolar technology and fast recovery diodes. The high frequency (current) link is also capable of sinusoidal a-c current injection and continuous input current envelope (is similar in operation to the field modulated generator concept).

This research has also investigated different types of semiconductor switching devices. The push to higher fre-

quency operation in power conversion demands devices with the ruggedness of a thyristor and the ease of control of a FET. The power transistor and power MOSFET are best suited to high frequency operation. The gate turn off thyristors investigated in the report had problems with reliable turn off when operating at 1800 Hz. The bipolar devices did not.

B. Hypothesis

The central thesis in this research has been sinusoidal current injection with controllable reactive voltamperes and continuous source current demand. In Chapter 5 the cascade converter was investigated as a candidate for inversion from a variable source. The cascade was composed of a boost dc converter and a PWM inverter. It was found that although a boost converter can regulate its output voltage with an input range from 2 to 3:1 into a passive load, it cannot remain stable under large-signal load current. This is exactly the condition presented by a PWM inverter large current pulsations. To overcome this inherent deficiency in voltage feedback, an input current (a-c feedforward) loop was incorporated. This multiple feedback technique resulted in a very stable regulator. High values of dc gain under large signal load is possible yielding a regulator with minimum output voltage variation for large changes in its input voltage. This new multiple feedback (MFB) technique is well suited for regulation of a random source with a pulsating load current.

C. Operation

During this research, several interconnected features of the cascade converter were discovered. These involve start up and utility connection. Proper sequencing during start up is essential. With all logic control circuits powered, the dc-side contactor may be closed. If the regulator step up ratio is high at this time, a large dc source surge current will result. If this proves excessive for either the source or regulator devices, the control signal d(t) can be restricted in range to allow a soft d-c connection. Next the inverter must be energized in phase with the utility. The logic signal control provided by the PWM commutation margin circuit realizes on-off control and the phase locked loop provides synchronous operation. With the regulated voltage set for desired reactive voltampere performance, the a-c contactor is then energized. From this point on a power tracking function controls the inverter.

The disconnect procedure is essentially the reverse of the above description. If utility voltage sags or surges out of its acceptable range, a check of the level of $v_m(t)$ derived from the utility voltage $v_\ell(t)$ would be used to produce a disconnect command. All these features would be most economically done using the microprocessor controller. That is because thresholds and limits could be easily changed.

Improper sequencing can be distructive. since the bridge incorporates inverse diodes and the switch existence

functions are complementary, then enabling the ac connection prior to starting PWM operation results in each ON switch and its opposite inverse diode short circuiting the ac supply. This was found to be a problem when using the upper driver memory latch circuit described in Appendix C. It was also verified that because of the unidirectional power flow capability of the regulator, disconnect or failure of the d-c source is isolated from the a-c utility. The regulator inverter voltage link assumes the potential that the full bridge inverse diodes deliver. Therefore no real power interchange occurs. Similarly for an ac fault, the line voltage sense is capable of very rapid disconnect.

D. Future Research

Several areas for future research are opened up. Evaluation of the audio susceptability on this regulator-inverter scheme show that MFB introduces considerable phase lead in its output to input response. This should be investigated for different dc to ac feedback gain ratios. Similarly for the control d(t) to output V_s response. This is now more difficult because of multiple paths into d(t). In order to assess the injected power variability in relation to that of the input power, a spectral study of both is required. An output-input power spectra would define the degree of power smoothing provided by the low pass response of this cascade.

Measurements of conversion efficiency were not performed during this study. The most meaningful efficiency measurements on this cascade converter would require a unit of several KW rating to be constructed and connected to an operating dc SWECS. Because of high speed switching, the real power component at the input, output of the regulator, and utility injection would require use of an electronic wattmeter. This type of metering is versatile and capable of obtaining the reactive volt-ampere component at the utility connection point.

APPENDIX A

APPENDIX A

ON CONVERTER TERMINOLOGY AND MEASUREMENT RESULTS ON THE CSI INVERTER

This appendix provides definitions of the concepts used in the development of the line commutated CSI inverter.

Consider the basic synchronous rectifier circuit of Figure A.1. Assume sinusoidal input voltage $v_\lambda(t)$ and a constant load current I_s. Rectification occurs when the thyristor gating signal occurs between the line voltage $v_\lambda(t)$ zero crossing and its first peak, i.e., $0 \leq \alpha < \pi/2$. The point where $\alpha = 0$ is defined as the rectification end stop. At this value of α the thyristors conduct for π radians. If this mode of operation is chosen, there is no need for controlled switches; diodes will suffice. However, if control over v_d is desired, then the angle α must be variable. When $\alpha = \pi/2$ is reached the dependent voltage v_d is zero. This is illustrated in Figure A.2a, b, and c. Note that as α exceeds $\pi/2$, the polarity of v_d reverses and operation is now in the second quadrant. The range of α from $\pi/2$ to π is termed the inversion quadrant. Here the load current may be replaced with a defined current source (I_s in Figure A.1) so that the flow of real power will

reverse. Reactive voltamperes will continue to be absorbed tive voltamperes in any switching converter is a consequence of the displacement angle α. Displacement factor, defined current I_s lagging (positive) or leading (negative) the voltage, is determined by the product of: sign (polarity) of voltage v_d times the wavetype. Wavetype is defined positive when the ripple component of v_d makes a positive transition at the firing angle α. It is negative when the transition in v_d at angle α is to a more negative value. As Figure A.2 shows, the wavetype in quadrant I is positive (rectification) and voltage v_d is also positive. Hence, reactive voltampere requirement is positive (absorbed from source $v_s(t)$. A positive reactive voltampere requirement by definition is lagging power factor (PF). Similarly, in quadrant II operation the wavetype is positive and the polarity of v_d is now negative; therefore the displacement factor is leading, but power factor is still lagging.

The average power contained in the waveforms of Figure A.2 can be found using the definite integral expression A.1 over any number of complete periods of the fundamental. Although reactive voltamperes (VARS) can be measured using the quadrature voltage component, no definition equivalent to equation A.1 exists for VARS, [see 36, Chapter 4]. In other words, reactive voltamperes do not describe energy storage in nonlinear converter circuits. In the special case of a sinusoidal source connected to linear passive loads the apparent voltamperes result from the real power

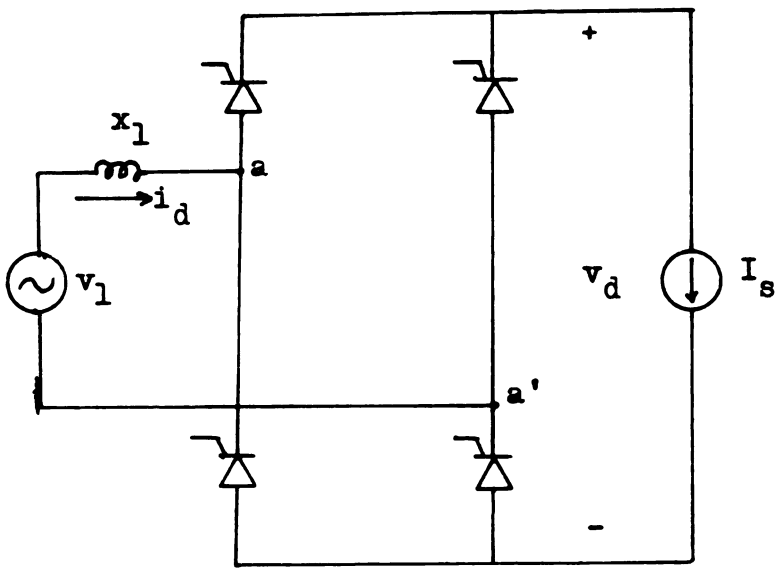


Figure A.1. Single phase synchronous rectification.

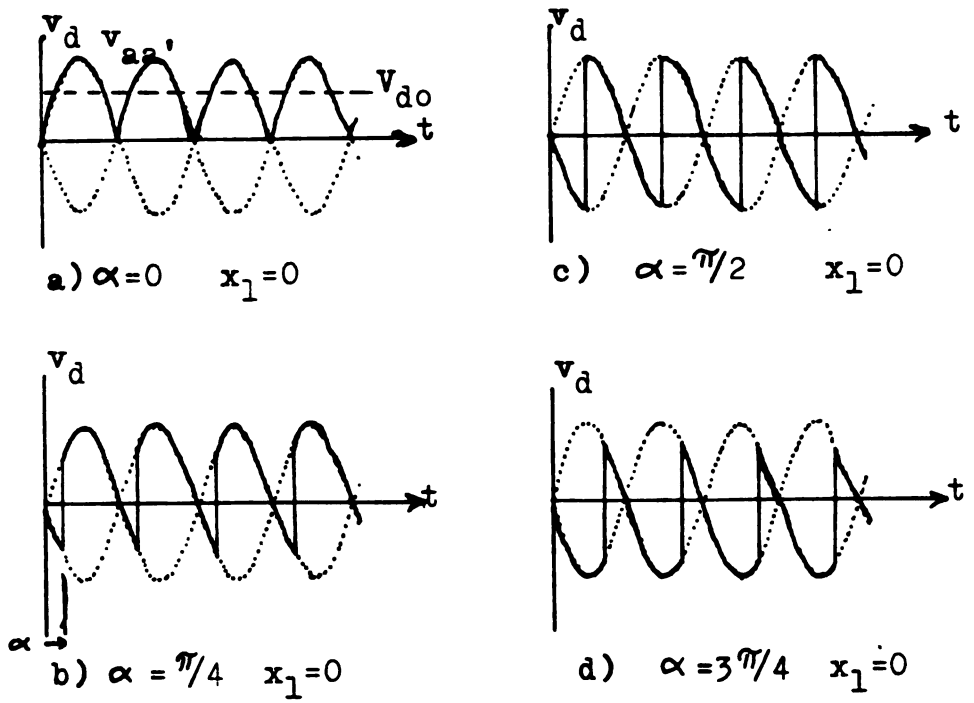


Figure A.2. Description of converter wavetype.

transfer and the energy exchange due to energy-storage characteristics of these loads. Reactive voltamperes resulting from magnetic energy storage are defined to produce a lagging power factor, while those due to electric field energy storage produce a leading power factor. In effect, apparent voltamperes constitute a maximum energy transfer capability of the system.

$$P \triangleq \frac{1}{2\pi} \int_0^{2\pi} v_\ell(t)\, i_d(t)\, d(\omega t) \qquad \text{(A.1)}$$

In this present case of a sinusoidal source, $v_\ell(t) = V_m \sin \omega t$, connected to a power electronic converter, the circuit to the right of terminals aa' of Figure A.1, contain no energy storage elements. Yet, as mentioned above, for non-zero α the circuit produces lagging reactive voltamperes. The fact that no energy storage components are present leads one to distinguish these reactive voltamperes from those produced by energy storage components. Call these non-active voltamperes. The reason for this distinction is to identify the analytical components of the apparent voltamperes supplied by the source $v_\ell(t)$ and arising from the switching action of the thyristors. By doing so, the use of power factor compensation elements and their value may be readily computed. In keeping with the definition of real power as apparent voltamperes times displacement power factor, the term reactive voltamperes, or Q, will be defined as apparent voltamperes times the sine of

the displacement angle. This function, Q, only has physical interpretation in sinusoidal supply voltage circuits

$$Q \triangleq V I \sin \alpha \qquad \text{(A.2)}$$

where upper case letters refer to the rms value of the given quantity. Here, $V = V_m/\sqrt{2}$ and $i_{drms} = I_{d_1}$. As Figure A.3 indicates, the nonlinear impedance of the thyristors introduce frequency components into $i_d(t)$ not present in $v_\ell(t)$. The effect of this non-sinusoidal dependent current is to cause the source to supply additional voltamperes. These

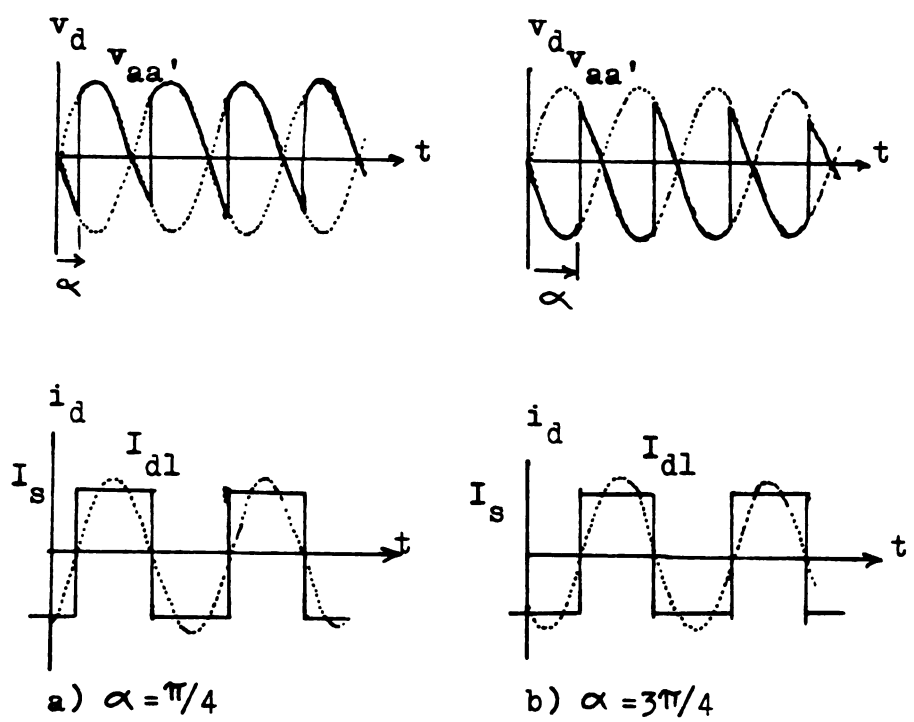


Figure A.3. CSI converter voltage and current time phase relations.

distortion voltamperes will be labeled D_s, such that the maximum energy transfer capability of the source S_s will be given as $S_s^2 = P^2+Q^2+D_s^2$. One may now state that source side power factor compensation may only be introduced with magnitude Q to remove the contribution of reactive voltamperes to the apparent voltamperes by acting as a local source or sink. No such compensation exists for distortion voltamperes D_s. From this discussion it is apparent that the distortion component sets an upper limit on the maximum attainable power factor that can be realized.

The average power P for each delay angle α in Figure A.2 can be computed using the expression A.1. Recall from circuit theory that the principle of superposition applied to harmonics of voltage and current but not to their product. Because real power enters the circuit only due to like frequency products of $v_l i_d$, and apparent voltamperes contains the contributions due to all cross product terms, the reactive voltampere term loses physical significance. By the first law of thermodynamics, all real or average powers absorbed by the load must sum arithmetically to the power delivered by the source. Not so for apparent voltamperes. These facts can be summarized in equation A.3 where the summation is over the K different load elements. As the last expression here shows, the principle of superposition does not apply. For linear passive loads containing K elements

$$P = \sum_{k=1}^{K} P_k$$

$$Q = \sum_{k=1}^{K} Q_k \qquad \text{(A.3)}$$

$$S_s^2 = \left(\sum_{k=1}^{K} P_k\right)^2 + \left(\sum_{k=1}^{K} Q_k\right)^2 \neq \left(\sum_{k=1}^{K} S_k\right)^2$$

In the case of Figure A.2 where the voltage $v_\ell(t)$ is sinusoidal and of fundamental component only, the RMS values may be computed using the expressions of equation A.4.

$$V \triangleq \sqrt{\frac{1}{2\pi}\int_0^{2\pi} v_\ell^2 \, d(\omega t)}$$

$$I \triangleq \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_d^2 \, d(\omega t)} \qquad \text{(A.4)}$$

$$I^2 = \sum_{k=1}^{N} I_k^2$$

Using the results of equation A.4 and the definitions of eq. A.3 it is found that $S_s^2 = V^2 I^2 = V^2 \sum_k I_k^2$. By definition the power factor is the ratio of average power to apparent voltamperes.

$$PF \triangleq \frac{P}{S_s} = \frac{P}{V\sqrt{\sum_{k=1}^{N} I_k^2}} \qquad \text{(A.5)}$$

where the significant harmonics are N in number. Since we have assumed only fundamental frequency source voltage, the average power P contains only a fundamental term VI_{d_1}. In

general, the supply voltage may also be assumed to consist of some finite number of significant harmonic components such that $P = \sum_{k=1}^{\infty} V_k I_k \cos \psi_k$ where the displacement angle ψ_k refers to the difference in angle between the k^{th} voltage and current components.

$$P = \frac{2V_m I_d}{\pi} \cos \alpha = \frac{2\sqrt{2}}{\pi} V I_{d\ell} \cos \alpha, \text{ Watts} \qquad (A.6)$$

$0 \leq \alpha < \pi/2$ rectification or quadrant I operation

$\pi/2 \leq \alpha < \pi$ inversion or quadrant II operation

$$Q = \frac{2V_m I_{d\ell}}{\pi} \sin \alpha, \text{ VAR (by definition)}$$

where $\alpha \equiv \psi_1$ in the sinusoidal case.

Equation A.6 illustrates that delay angle α results in reactive voltamperes due to displacement that can be cancelled with electric field storage voltamperes $Q = \omega C_o V^2$. Here C_0 is the optimum capacitance for a given voltage V to achieve exact cancellation. Note further that as α is retarded past $\pi/2$ radians, the sign of P reverses while that of Q remains unchanged. This is consistent with quadrant II operation yielding a transfer of power into the defined source v_ℓ. By Kirchhoff's current law, this same square wave of current i_d flows in the defined source. The current harmonics so injected into the souce v_ℓ will contribute distortion voltamperes which further reduce the power factor.

The vector sum of real power and reactive voltamperes given by equation A.6 can thus be equated to apparent voltamperes minus distortion voltamperes, equation A.7. The

resulting locus is plotted in Figure A.4. As this figure demonstrates, increasing the delay angle α moves the operating point out of quadrant I and into quadrant II. At $\alpha = \pi/2$ no real power transfer occurs, but the reactive voltamperes Q are maximum. This figure also illustrates the fact that a line commutated converter can only absorb (+Q)

$$S_s^2 - D_s^2 = P^2 + Q^2 \qquad (A.7)$$

reactive voltamperes whereas it is capable of bidirectional power transfer. Figure A.3 shows the displacement angle of the fundamental component of current I_{d_1} versus line voltage $v_{aa'}$. When this converter operates in quadrant II it is appropriate to refer to the current as lagging the voltage by an angle that is between $\pi/2$ and π radians.

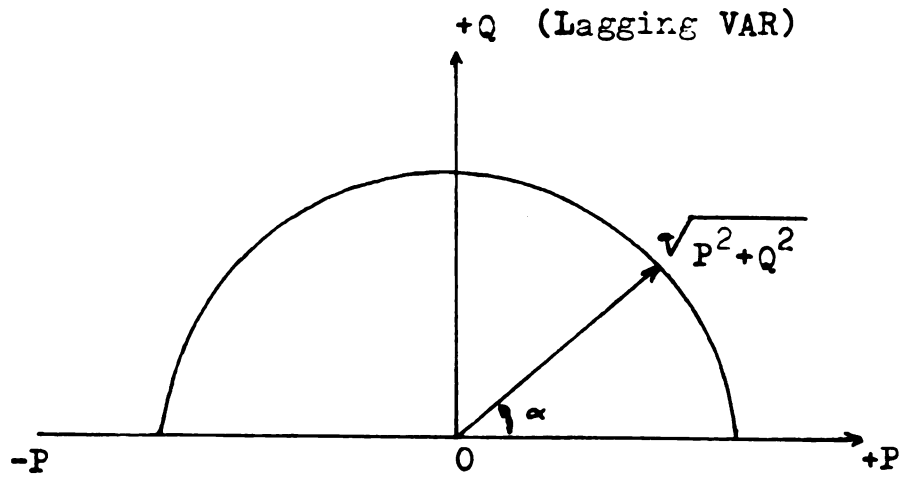


Figure A.4. Voltampere operating locus for phase angle controlled converter.

Since $\sin^2 + \cos^2 = 1$, the locus of $P^2 + Q^2$ defines a semicircle. We see that for operation at other than rectification or inversion end stop, the reactive voltampere support for line commutated converters is very significant. Later, it will be shown that in practical CSI converters with non-ideal sources, this demand for reactive voltamperes from the utility is increased even higher.

Example A.1: The ideal single phase line commutated CSI converter. The distortion voltamperes D_s for the converter topology of Figure A.1 exhibiting the waveforms of Figure A.3 can be computed as follows. Since current $i_d(t)$ is an ideal square wave of current,

$$i_d(t) = \sum_{k=1}^{\infty} \frac{4I_d}{k\pi} \cos k\omega t;\ k = 1,3,5,... \qquad \text{(A.8)}$$

$$i_{d1\ rms} \triangleq I_1 = \frac{4I_d}{\sqrt{2}\,\pi}$$

Equation A.6 can be rewritten in rms quantities so that the distortion voltamperes may be computed, here

$$P = V_1 I_1 \cos \alpha \qquad \text{Watts}$$

$$Q = V_1 I_1 \sin \alpha \qquad \text{VAR} \qquad \text{(A.9)}$$

$$\text{where } V_1 I_1 = \frac{Vm}{\sqrt{2}} \cdot \frac{4I_d}{\sqrt{2}\,\pi} = \frac{2}{\pi} V_m I_d.$$

To account for the current harmonics the expression A.4 for I must be used. Then equation A.7 for distortion voltamperes becomes

$$D_s^2 = S_s^2 - (P^2+Q^2)$$

$$= V^2 \sum_{k=1}^{\infty} I_k^2 - V^2 I_1^2 \left[\cos^2 \alpha + \sin^2 \alpha\right] \qquad \text{(A.10)}$$

$$= V^2 \sum_{k=3}^{\infty} I_k^2 \qquad k = 3,5,7,\ldots$$

$$= V^2 I_1^2 \sum_{n} 1/(2n-1)^2 \qquad n = 2,3,4,\ldots$$

$$= V^2 I_1^2 \left[Z_{(2)}\left(1 - \frac{1}{2^2}\right) - 1\right]$$

$$D_s = 0.483\, V I_1$$

where Z(z) is the Zeta function.

Equation A.10 shows that for the current waveform of Figure A.3 the distortion voltamperes are 48.3% of the fundamental voltamperes. Even with power factor correction to cancel the +Q reactive voltamperes, the line current exceeds the value needed for real power due to these distortion components.

The substitution of average power P from equation A.9 into the power factor expression A.5 reveals that the composite power factor or total power factor [29] is given by

total power factor	=	displacement power factor	x	distortion power factor

$$PF_T = (\cos \psi_1) \left(\frac{1}{\sqrt{1+\frac{1}{I_1^2}\sum_{n=2}^{\infty} I_n^2}}\right) \qquad \text{(A.11)}$$

Where total power factor is defined as the ratio of average power, the product of like frequency components, to the apparent voltamperes, which contains all frequency products. Equation A.11 shows the relative contribution to total power factor by both the displacement and distortion terms. Of course, if the current waveform in this instance were a sinusoid of fundamental component only, the distortion voltamperes vanish.

Define the distortion factor DF as the ratio of the root sum square of the harmonics to the fundamental. Then total power factor PF_T can be expressed as

$$DF_x \triangleq \frac{1}{X_1}\sqrt{\sum_{n=2}^{\infty} X_n^2}$$

$$PF_T = \frac{\cos \psi_1}{\sqrt{1+(DF_I)^2}} \qquad \text{(A.12)}$$

In these derivations it is important to note that the average power and reactive voltamperes apply only to the fundamental component. When the a-c source is not ideal, but consists of a voltage behind an impedance, it is possible for the harmonic currents injected into the line to distort the line voltage. This is possible for a weak a-c source and a converter or collection of converters interconnected to this source with a low short circuit ratio (the ratio of the system short circuit MVA to the converter MW rating). It is also apparent from Figure A.3 that a square wave of current injected into the a-c network will be

a strong source of current harmonics. If the network is infinitely stiff, these harmonic currents will not supply any real power. It is only when the source contains similar harmonics that real power transfer at harmonic frequencies takes place.

At this point, some general comments will summarize the discussion. It is shown that reactive voltamperes Q cannot be defined by an integral expression as for real power. This is because reactive voltamperes have no physical meaning. The quantity Q is an analytical tool defined to be complementary with the expression for real power P. Moreover, apparent voltamperes are not dependent on frequency and contain all frequency product terms. Distortion voltamperes arise only from the combination of unlike frequencies.

The degree any periodic waveform deviates from a sinusoid is referred to as distortion. The most common figure of merit is total harmonic distortion (THD), or distortion factor DF if given in percent. Another accepted measure is distortion index Γ given as the fractional total harmonic distortion.

$$\text{THD} \triangleq \frac{\text{rms value of harmonics}}{\text{rms value of the fundamental}}$$

$$\Gamma \triangleq \left\{\left(\frac{\text{waveform rms value}}{\text{fundamental rms value}}\right)^2 - 1\right\}^{\frac{1}{2}} \qquad \text{(A.13)}$$

Application of Γ defined in equation A.13 to example A.1 where the current has rms value I_s and fundamental component given by equation A.8 yields the .483 factor.

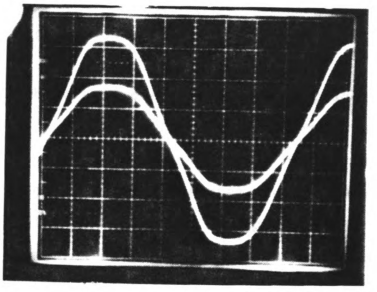
When the voltage waveform is distorted, equation A.11 must be rewritten as [36]

$$PF_T = \frac{\sum_{k=1}^{\infty} V_k I_k \cos \psi_k}{\left\{ \sum_{k=1}^{\infty} V_k^2 \cdot \sum_{k=1}^{\infty} I_k^2 \right\}^{1/2}} \qquad \text{(A.14)}$$

In this definition, the displacement factor can no longer be identified independently of the distortion term since displacement angles of all harmonics are involved in the summation. Thus, only when the harmonic content in both the voltage wave and current wave go to zero, will total power factor equal displacement power factor. This is important since utility watthour and varhour meters see only the fundamental power factor [29].

A measurement of the voltage wave harmonics are given in Figure A.5a and b. These measurements were made using a precision potential transformer to sample the utility line voltage in the Engineering building. This signal was analyzed for harmonics using a hP5423SDA. Figure A.5b shows that at this particular location the fifth harmonic dominates. An example will show the effect of voltage distortion on apparent voltamperes. Since the fifth harmonic dominates the voltage spectrum (phase is radians), only the fundamental and this component will be used.

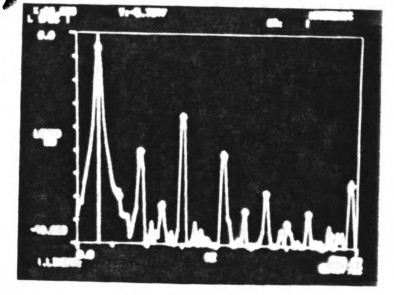
Example A.2. Illustration of equation A.14 for the conditions given in example A.1 and Figure A.5b.



a) Time Signal

$v_{\ell\ rms} = 120.6$ V

$x_1 - x_2 = 6.01$ V



b) Spectrum

0 - 800 Hz

n	%
1	100
3	0.6
5	3.75
7	0.58
9	0.076

THDV = 3.84%

Figure A.5. Measurement of voltage distortion.

$$PF_T = \frac{V_1 I_1 \cos 0 + \left(V_{1/26.7}\right)\left(I_{1/5}\right) \cos \pi}{\left\{V_1^2\ (1.0014)\ I_1^2\ (1.233)\right\}^{\frac{1}{2}}} \qquad \text{(A.15)}$$

$$= 0.893$$

Therefore, even though the displacement power factor $\cos \Psi_1 = 1$ is unity for the fundamental component, the presence of voltage and current harmonics yields a substantial reduction in the system power factor. Note that according to Figure A.4 this power factor cannot be improved by using VAR compensation techniques since it is due to distortion voltamperes.

The preceeding discussion outlined the behavior of the circuit in Figure A.1 under ideal circumstances. This can never be achieved in practice. The first step in the direction of reality calls for a finite line reactance X_ℓ. The series reactance X_ℓ models real world transmission/distribution line reactance plus any service-drop cable reactance and transformer leakage reactance. The effect of finite reactance X_ℓ is to modify the square wave of current such that transitions can no longer have infinite dI/dt. This means that when the second pair of thyristors in Figure A.1 are gated ON, the supply v_ℓ is short circuited by reactance X_ℓ until sufficient volt-seconds accumulate on X_ℓ to commutate off the first pair of thyristors. This time interval is known as the commutation overlap angle μ and its effect is to produce voltage notching of the source phase

voltage. As Figure A.7 indicates, the presence of line side inductance imposes a volt-second requirement on the source of magnitude exactly equal to that required for i_d to change from $-I_s$ to $+I_s$. If the value of $v_\ell(t)$ is e at the instant $\omega t = \alpha$, then Faraday's law gives the required commutation notch width t_N. Note that for narrow notch width, the volt-second-integral (VSI) can be approximated as:

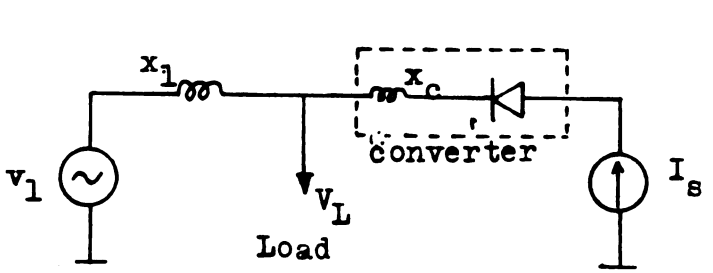
$$V.S.I. = \int_0^{t_N} (v_\ell - v_{aa}) \, dt \cong \int_0^{t_N} e \, dt = et_N$$

$$2I_d = \frac{\omega}{X_\ell} V.S.I. \qquad \text{(A.16)}$$

$$t_N = \frac{2X_\ell}{\omega e} I_d$$

An example will illustrate the application of equation A.16 to an actual CSI converter.

Example A.3: A 4kW line commutated CSI converter is operating into a 240 V_{rms} utility as depicted in the one-line diagram of Figure A.6. The line inductance consists of transformer reactance and cable reactance. On a 240V base these values are found to be 0.126 and 0.113 ohms,



$x_s = .126 + .123$
$x_c = .075$
$\omega = 377$
$V_\ell = 240 \sin \omega t$
$I_s = 12$

Figure A.6. System configuration for example A.3.

respectively. Reactance X_c is the converter internal notch suppression inductance.

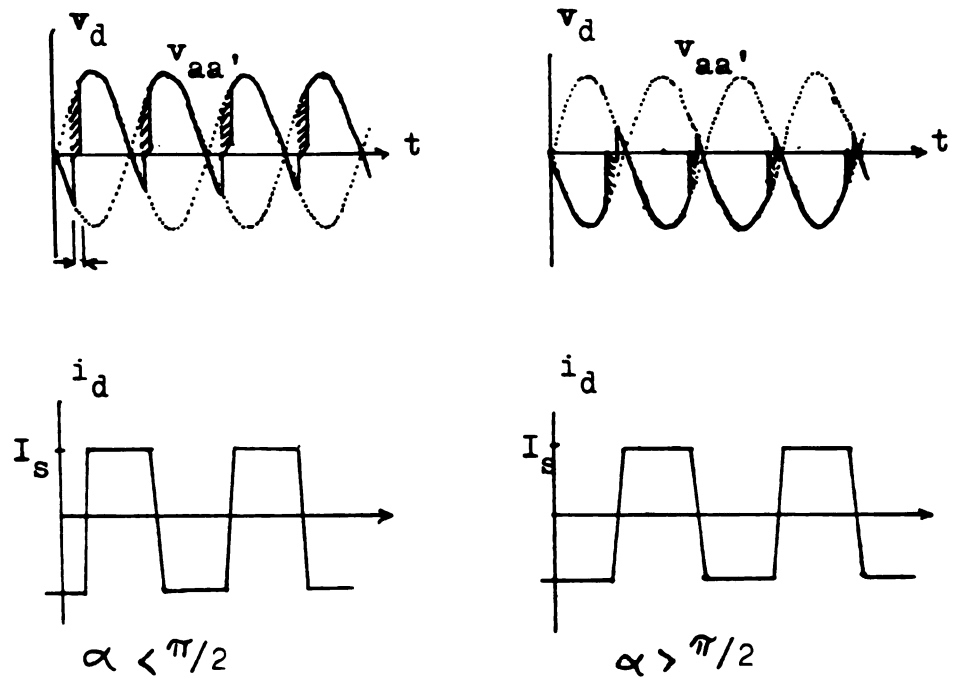


Figure A.7. Effect of finite X_ℓ on CSI operation.

Suppose the converter firing angle is set to fire 6 ms into the 60 Hz utility waveform such that $\alpha = 130^o$ at which point the value of $v_\ell(t)$ is e = 185 V. Then equation A.16 gives a value of 108 microseconds for the commutation notch width.

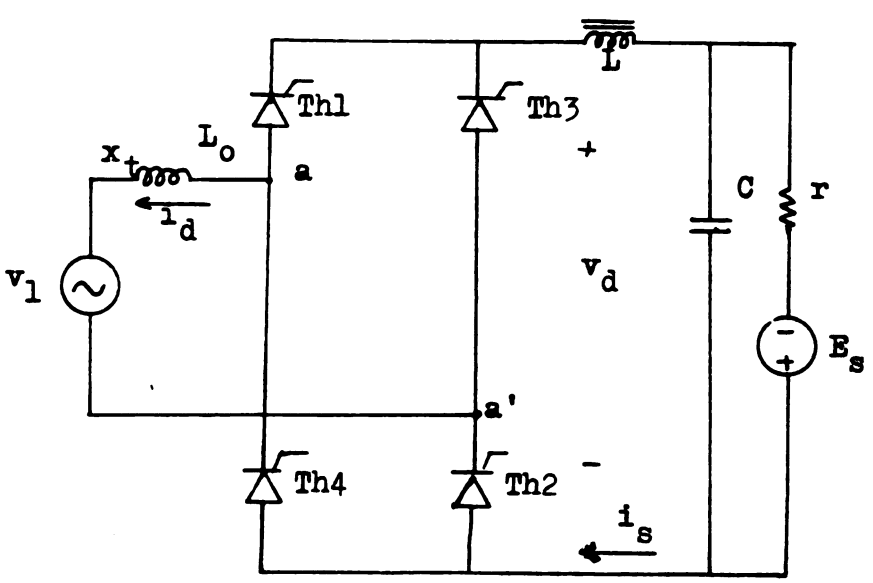
$$t_N = \frac{2(X_s+X_c)I_d}{\omega e} = \frac{2(.314)12}{377(185)} = 108\ \mu s$$

At the external load bus which represents all other loads connected to the system at this point, the observed line notching will depend on the ratio of the system and converter impedance. This means that for a very stiff system, the generation of line notch-induced voltage harmonics will

be the least severe. With the line reactance values given in Figure A.6 the voltage notch depth on the load bus is

$$V_n = \frac{X_s}{X_s+X_c} e = .76e$$
$$= 141 \text{ V}$$

The shaded area in Figure A.7 represents the voltseconds required to commutate between alternate pairs of thyristors for a finite source impedance. The analysis to this point has concentrated on the continuous conduction case. That is, a constant current source was assumed. The final modification to Figure A.1 is to replace the ideal current source with a real voltage source and a filter inductor. This inductor (L) can be either air core or of ferrous metal construction. The component values given in Figure A.8 are representative of the system considered in example A.3.



r = .7 ohm
L_o = 500μH
L_ℓ = 8μH
V_ℓ = 345 sin ωt
E_s = 160V
C = 1700μF

Figure A.8. Non-Ideal CSI converter.

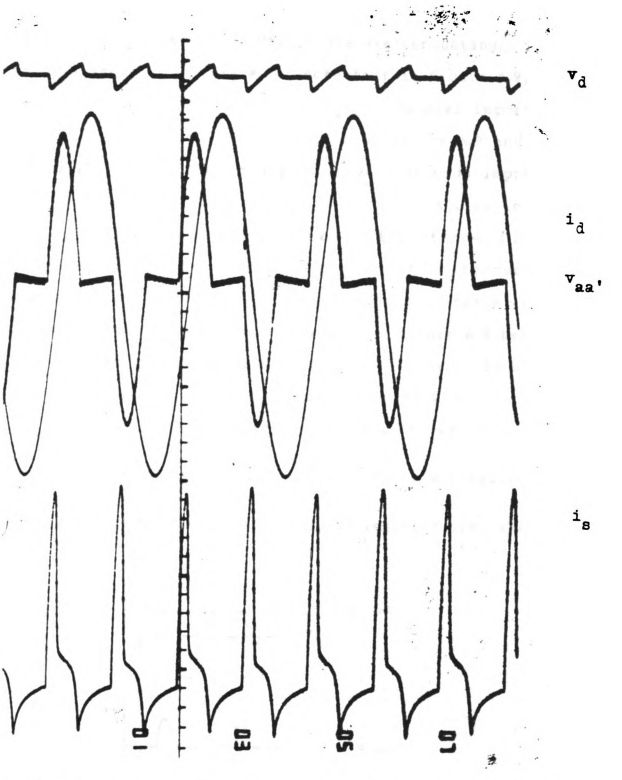
The voltages given in Figure A.9 have been chosen to correspond with values obtained during tests of this inverter. Figure A.9 is the actual oscillograph recording of signals $V_{aa'}$, V_d, i_d, and i_s. As shown in Figure A.9, the CSI converter firing angle is 152.4^o and the current pulse duration is 92^o. It should be noted that due to the potential transformer connection the recorded line voltage is $V_{a'a}$ not $V_{aa'}$. Also, the noise present on both current waveforms is due to the sampling performed by the oscillograph input modules on those particular channels. Table A.1 lists the signal levels during this test.

Table A.1

Conditions for Recorded Data in Figure A.9

Signal	Amplitude
V_{do}	-160 V_{dc}
V_d	50 V_{p-p}
I_d	13.1 A_{peak}
$V_{aa'}$	345 V_{peak}
delay angle	152.4^o (2.66 radians)
conduction angle	92^o (1.6 radian)

The analysis of Figure A.8 proceeds as follows. The input current is discontinuous (see i_s in Figure A.9). Thus thyristor commutation is a source commutation occuring when the current through a thyristor pair attempts to reverse. The capacitor C in Figure A.8 provides filtering of the dependent voltage V_d. The effect is that V_d is effectively



V_d = 82 V/cm, $V_{aa'}$ = 72.6 V/cm, i_d = 3.42 A/cm, i_s = 2.24 A/cm
Honeywell 1858 Visicorder at 80 in/sec.

Figure A.9. Oscillograph of CSI performance.

clamped to V_{do}, the potential across capacitor C during the time intervals in which no thyristors are conducting. This effect is shown in Figure A.10 (note that in Figure A.9, V_d is also inverted to coincide with $V_{a'a}$). Several important features are apparent from inspection of Figure A.9 and Figure A.10. First, the steady state volt seconds impressed upon L average to zero. Notice the strong flux bias in L due to i_s, which causes the incremental inductance of L to vary as the average d-c amp-turns produced by i_s forces the operating point to move along the magnetization curve as the d-c generation E_s varies (not apparent in Figure A.9 because E_s and V_{do} are slowly varying functions of time). Second, the peak of $i_d(t)$ occurs exactly at the point when $V_{aa'}(t) = V_{do}$. This gives the value of ωt at which $\frac{di_d(t)}{dt} = 0$. Using Figure A.10, an analytical expression can be derived for dependent current $i_d(t)$ injected into the utility.

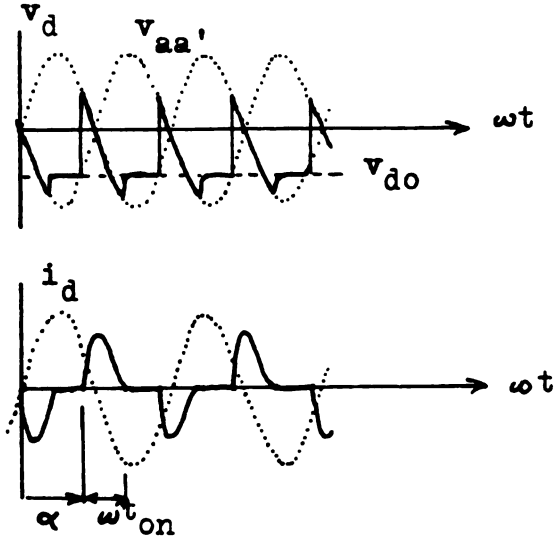


Figure A.10. Waveforms illustrating non-ideal CSI performance.

$$V.S.I. = \int_{\alpha/\omega}^{t} (v_{aa'} - V_{do})dt; \quad \alpha/\omega \leq t < \alpha/\omega + t_{ON}$$

$$= \int_{\alpha/\omega}^{t} (V_m \sin \omega t - V_{do})dt$$

$$= -V_{do}(t-\alpha/\omega) + {}^{V_m}/_{\omega}(\cos \alpha - \cos \omega t) \qquad (A.17)$$

$$i_d(t) = \frac{1}{L} V.S.I.$$

$$i_d(t) = -\frac{V_{do}}{L} (t-\alpha/\omega) + \frac{V_m}{\omega L} (\cos \alpha - \cos \omega t)$$

$$i_d(t) = 2.0 \times 10^4 \ (t-\alpha/\omega) + 114.39 \ (\cos \alpha - \cos \omega t)$$

where $\alpha/\omega \leq t < \alpha/\omega + t_{ON}$, t in ms.

Equation A.17 is plotted in Figure A.11 for two values of inductor L. The d-c component in equation A.17 vanishes

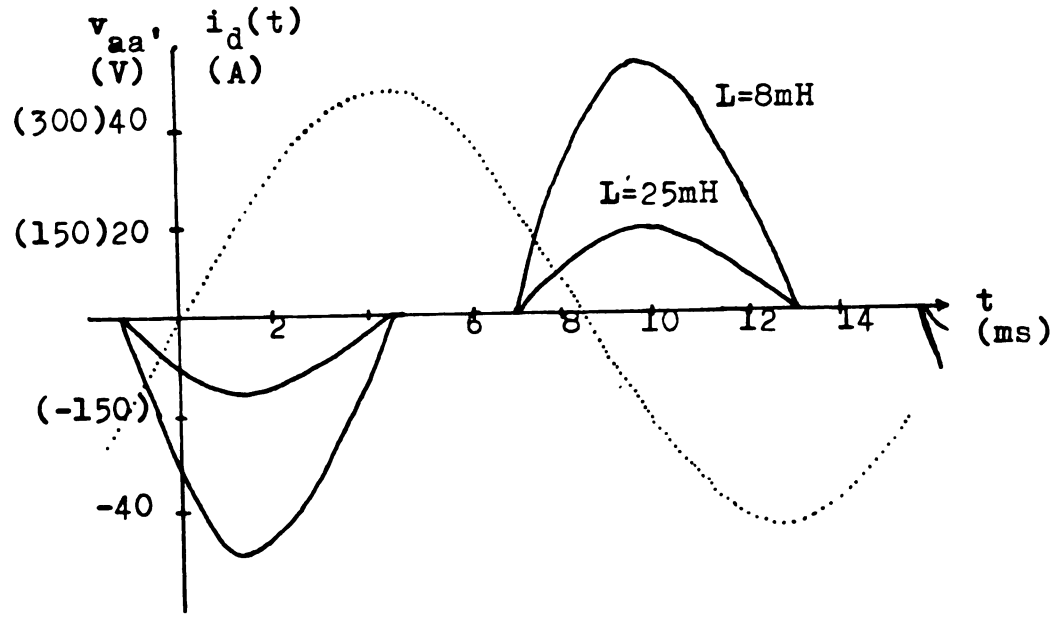
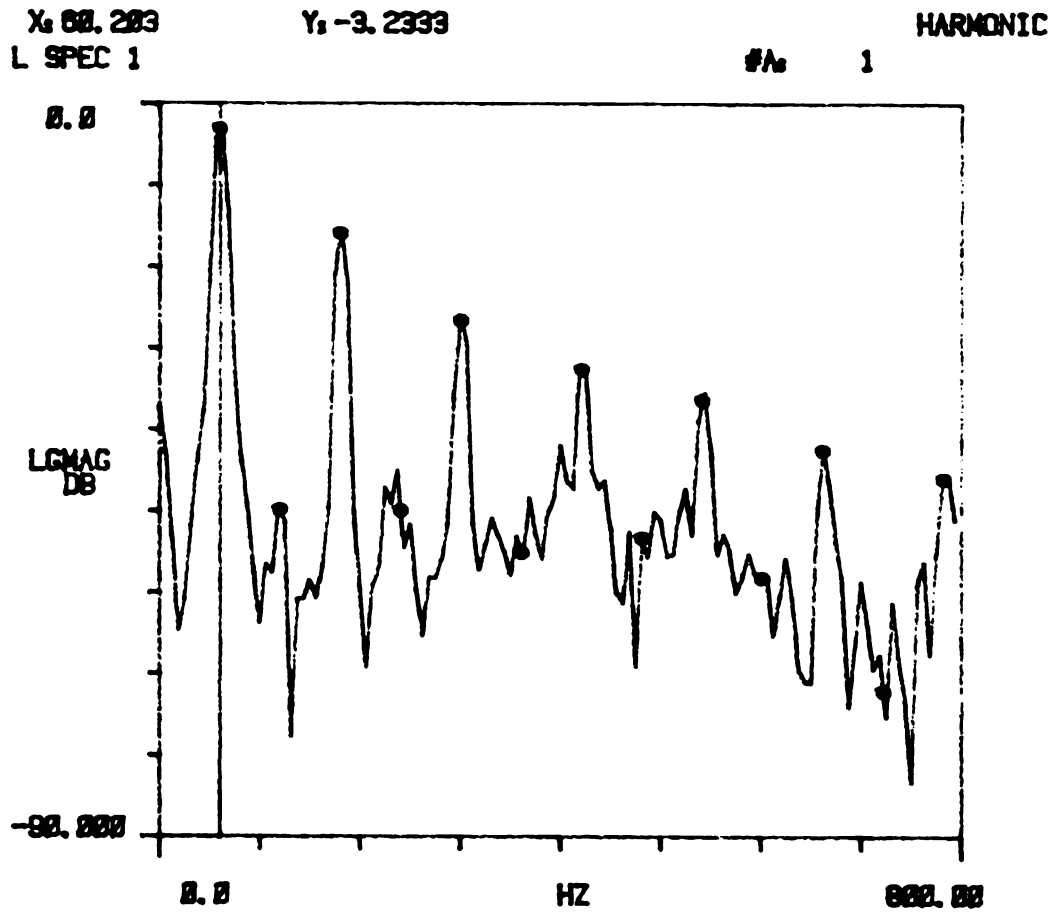


Figure A.11. Plot of equation A.17.



≈ 3 KW output from 4 KW rated dc generator

Figure A.12. Spectrum of $i_d(t)$ recorded in Figure A.9.

due to odd symmetry. The conduction angle t_{ON} is a function of thyristor firing angle α and the ratio of V_{do} to V_m. So, if α approaches π radians for a given input source voltage V_{do}, the peak amplitude of $i_d(t)$ is reduced. This is a consequence of the non-ideal current source nature of the E_s and L network.

The spectral content of $i_d(t)$ is displayed in Figure A.12. This spectrum was obtained by recording the signal $i_d(t)$ on a magnetic tape recorder during normal operation of the CSI inverter and then playing the tape back into a lab spectrum analyzer. The results of this spectral analysis show that the total harmonic distortion for current $i_d(t)$ using harmonics 3 through 9 is:

$$THDI = \sqrt{(.304)^2 + (.089)^2 + (.040)^2 + (.032)^2}$$

$$THDI = 0.32.$$

This is lower than for a square wave .483 and illustrates the current waveshaping provided by inductor L in this application.

APPENDIX B

APPENDIX B

VSI CONVERTER THEORY AND MEASUREMENT RESULTS

This appendix reviews the theory and experimental results obtained from an operational 10 kW VSI line-commutated inverter. It will be shown that this configuration generates significant harmonics even as power approaches rated value. The reason can be seen from Figure B.1 where the wind driven generator (alternator in this case) feeds an uncontrolled bridge rectifier (a three-phase Graetz circuit). The three-phase rectified voltage is filtered by

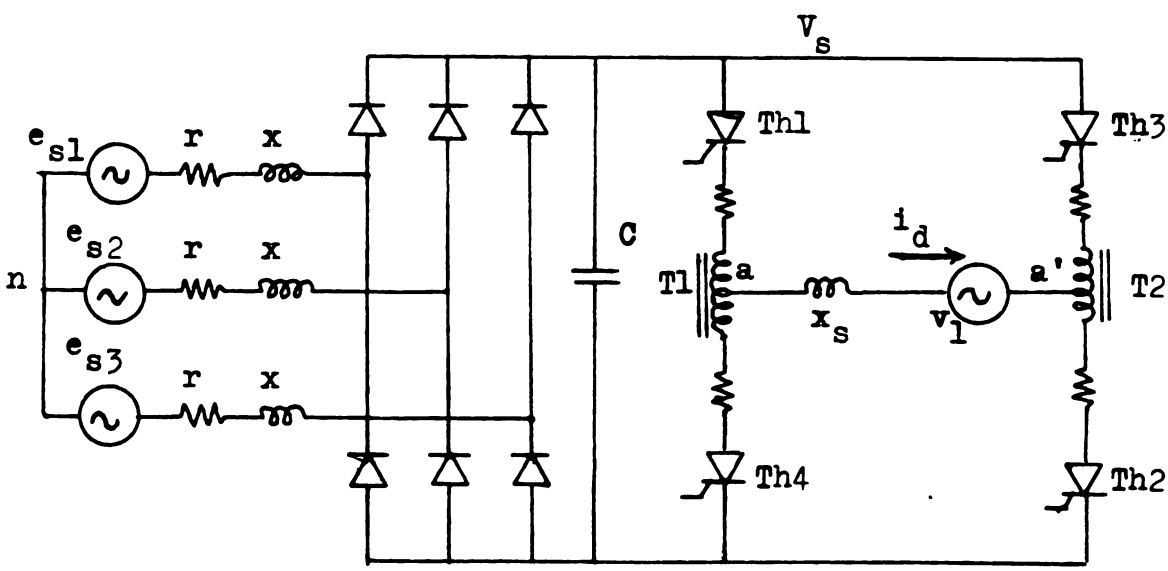


Figure B.1. Alternator driven VSI converter.

capacitor C and this filtered voltage V_s, a slowly varying function of time relative to the line voltage period, supplies through a thyristor bridge dependent current $i_d(t)$ to the utility source $V_\ell(t)$. The situation is that of a voltage source driving another voltage source; so when source potentials do not match, large currents can flow. The $^{dI}/_{dt}$ reactors shown in Figure B.1 limit the rate of current rise of the bridge thyristors and have a moderate effect on current waveshaping. It is also necessary that lead and reactor winding resistances be equal since any unbalance will introduce asymmetry between the two bridge poles and consequently generate even harmonics. Since all such converter installations are interfaced to the utility distribution network through transformers, the d-c component of the injected current will bias the transformer core. Should the ampere turns due to this bias be sufficient to cause the normal peak operating flux to exceed the knee of the transformer magnetization curve, substantial current peaking will occur along with an increase in the third harmonic of the line voltage. Reference [14] gives examples of unbalanced ampere-turns on interphase transformers and inverter transformers.

The analysis of Figure B.1 is done using the operating conditions and parameter values given in Table B.1. The base quantities are 240 V_{rms} and 37.5 KVA. The transformer has 3.66% impedance so that

$$Z_b = \frac{(.24)^2 \times 10^3}{37.5} = 1.536 \text{ ohms}$$

$$X_s = 3.66 \times 1.536 \times .01 = .056 \text{ ohms} \qquad \text{(B.1)}$$

$$L_s = X_s/\omega = 148.5\ \mu H$$

Using an inductance bridge the parameters of the tapped reactors were obtained. The remaining values in Table B.1 are nameplate or calculated.

Table B.1

VSI Converter Circuit Parameter Values

Operating values	V_s	198 V_{dc}	
	ΔV_{sp-p}	14 V_{p-p}	
	i_d	42 A_{peak}	
	V_ℓ	232 V_{rms}	
	P	5 kW	approx.
Component parameters	L_s	148.5 μH	
	$L_{reactor}$	.9 mH	
	$R_{reactor}$	.8 ohm	
	C	3900 μF	
	I_T	125 A_{rms}	Thyristor rated current

If the assumption is made that for operation at less than rated power the reactors remain linear, then $L_{reactor}$ can be set constant at its measured value. It should be

noted that the inductance measurement was made at 1 kHz so that the value given may be somewhat higher at 60 Hz.

The analysis using linear theory will give an expression for the line injected current $i_d(t)$. Given an equation for $i_d(t)$, valid over a complete cycle, it will then be feasible to make theoretical calculations of the injected current harmonic levels. It is necessary to note that for this converter both input current (to the thyristor bridge) and the line injected current will remain discontinuous. This is an essential departure from the CSI converter in which continuous current operation is a function of the d-c source parameters and the ratio of d-c to a-c line voltages as demonstrated in Appendix A. A further simplification to the circuit of Figure B.1 is to replace the generator, rectifier and filter capacitor with its Thevenin equivalent source. Using the operating values of Table B.1 the effective output resistance of this network can be determined as

$$R_{TH} = \frac{\Delta V_{s\ p\text{-}p}}{\Delta i_d} = .37 \text{ ohm}$$

$$E_{TH} \doteq V_{s\ min} + R_{TH} i_{d\ peak} = 205 \text{ V} \qquad \text{(B.2)}$$

Using the values calculated in equation B.2 the overlap conduction (i_{cc}) that will occur during a commutation failure can be found as the response of a series R-L circuit. In this instance the driving function will be a step in voltage of magnitude E_{TH}.

$$i_{cc}(t) = {}^{E_{TH}}/_{R_T}\,[1 - \exp(-R_T\,{}^{t}/_{L})] \qquad \text{(B.3)}$$

where $R_T = R_{TH} + 2(R_{ON} + R_{reactor})$. After four time constants, current $i_{cc}(t)$ will have reached 102.5 A. For different operating conditions higher or lower values will occur. The important point is that current magnitudes capable of exceeding the maximum thermal energy rating (I^2t) of the semiconductor devices can be reached rapidly in a fault. An additional feature of VSI converters would be the inclusion of series fuses with each main thyristor. The constraint being that $I^2t_{fuse} < I^2t_{Thyristor}$.

Measurements on the performance of this converter show that the thyristors are gated on an angle β ahead of the voltage wave zero crossing. This angle was found to remain very close to 3^o (.15 ms). Consider the interval from $-\beta$ to ωt_{ON} during which thyristors Th1 and Th2 are ON. Time t_{ON} is the conduction time of these devices. Application of Kirchhoff's voltage law to the circuit of Figure B.2 during

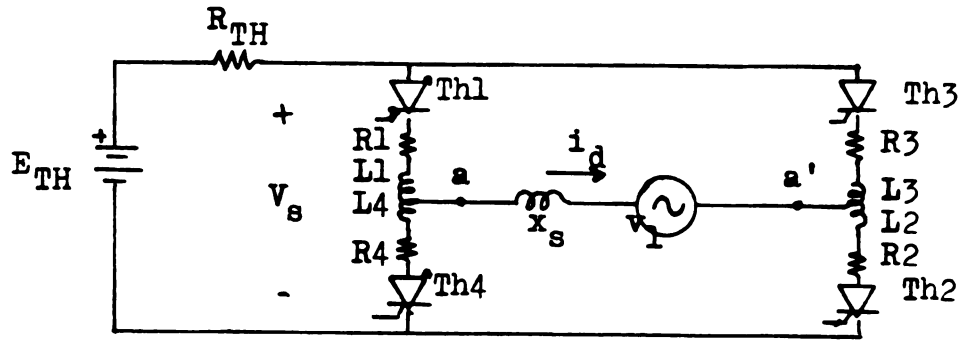


Figure B.2. Simplified VSI converter.

this time interval yields

$$E_{TH} - \nu_{\ell}(t) = (R_{TH}+R1+R2)i_d(t) + (L1+L2+L_s)\,di_d(t)/dt + V_T\,(Th1) + V_T\,(Th2) \qquad \text{(B.4)}$$

where V_T is the thyristor ON state voltage. Let $R_r = R1 + R2 = 2\,R_{reactor}$, $L_r = L1 + L2$, and $E_{TH} = E_{TH} - 2\,V_T$ then

$$E'_{TH} - V_m \sin(\omega t-\beta) = (R_{TH}+R_r)i_d(t) + (L_s+L_r)\,di_d(t)/dt \qquad \text{(B.5)}$$

Shifting the time axis in equation B.5 by β/ω and taking the Laplace transform yields

$$\frac{E'_{TH}}{S} - \frac{V_m(\omega\cos\beta - S\sin\beta)}{S^2+\omega^2} = (R_{TH}+R_r)I_d(s) + S(L_s+L_r)I_d(s)$$

$$I_d(s) = \frac{E'_{TH}}{S(L_s+L_r)(S+1/\tau)} + \frac{V_m[S\sin\beta - \omega\cos\beta]}{(L_s+L_r)(S+1/\tau)(S^2+\omega^2)} \qquad \text{(B.6)}$$

Where discontinuous conduction yields $i_d(0+) = 0$ and

$\tau = \dfrac{L_s+L_r}{R_{TH}+R_r} = \dfrac{L_T}{R_T}$, a partial fraction expansion of equation B.6 is

$$I_d(s) = \frac{E'_{TH}}{R_T S} - \frac{E'_{TH}}{R_T(S+1/\tau)} - \frac{V_m}{R_T}\left[\frac{\sin\beta + \omega\tau\cos\beta}{(1+\omega^2\tau^2)(S+1/\tau)}\right] + \frac{SV_m(\sin\beta + \omega\tau\cos\beta)}{R_T(1+\omega^2\tau^2)(S^2+\omega^2)} + \frac{\omega V_m(\omega\tau\sin\beta - \cos\beta)}{R_T(1+\omega^2\tau^2)(S^2+\omega^2)} \qquad \text{(B.7)}$$

The inverse Laplace transform of equation B.7 can be obtained to yield the time response $i_d(t)$ for $0 \le t \le t_{ON}$.

The current ceases at $t = t_{ON}$ because the line voltage source commutates the ON thyristors. This result is plotted in Figure B.3. Comparison with measured data in Figure B.4 verifies this analysis.

$$i_d(t) = \frac{E'_{TH}}{R_T}\left[1 - \exp\left(-t/\tau\right)\right] - \frac{V_m}{R_T}\left[\frac{\sin\beta + \omega\tau\cos\beta}{1+\omega^2\tau^2}\right]\exp\left(-t/\tau\right)$$
$$+ \frac{V_m}{R_T}\left[\frac{\sin\beta + \omega\tau\cos\beta}{1+\omega^2\tau^2}\right]\cos\omega t + \frac{V_m}{R_T}\left[\frac{\omega\tau\sin\beta - \cos\beta}{1+\omega^2\tau^2}\right]\sin\omega t \qquad \text{(B.8)}$$

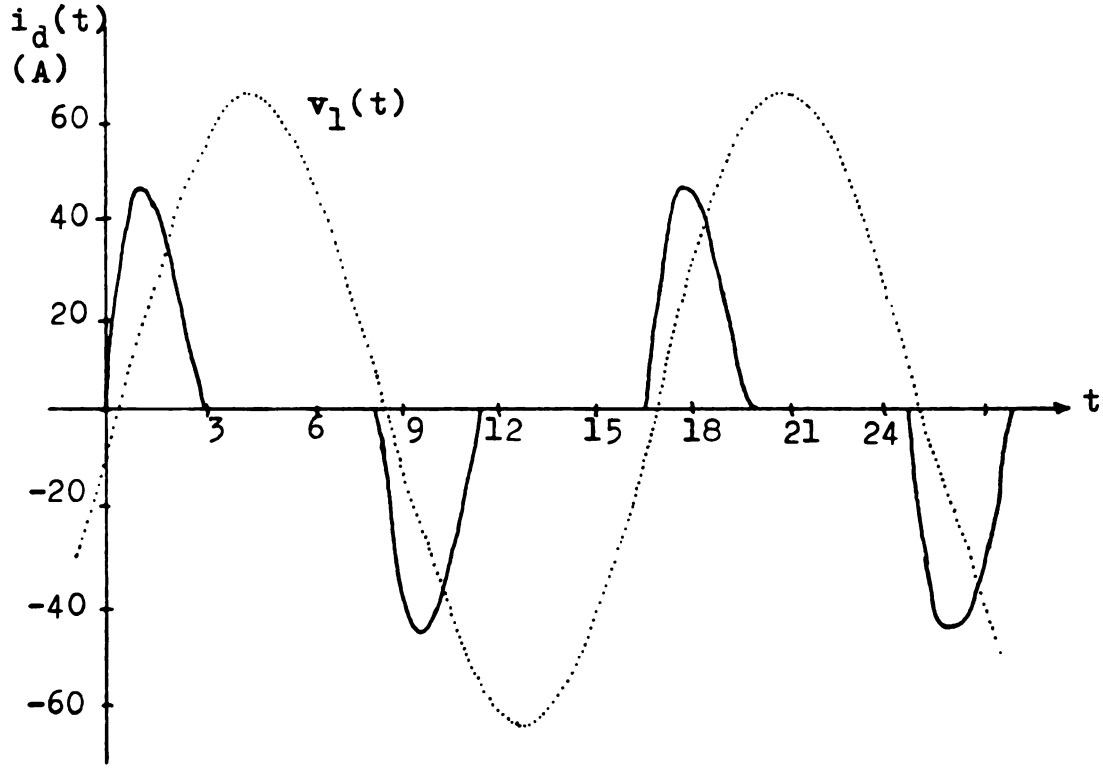
where $0 \leq t \leq t_{ON}$.

The noise present on the two current measurement channels of the oscillograph was due to signal sampling in those particular modules. All other signals were obtained using high gain differential input modules.

As Figures B.3 and B.4 show, the initial current slope $di_d(t)/dt$ is much more severe than for the CSI topology investigated in Appendix A. For the operating values shown, the initial current slope can be determined by taking the derivative of equation B.8 and evaluating the resultant expression at $t = 0+$.

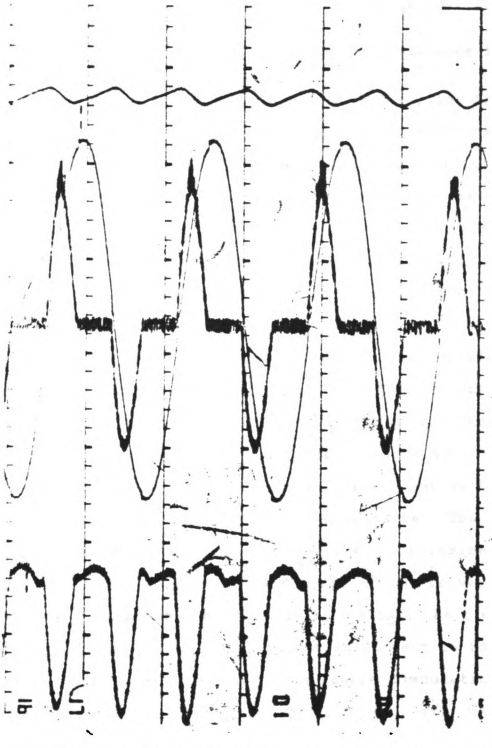
$$\left.\frac{di_d(t)}{dt}\right|_{t=0^+} = \frac{E'_{TH} + V_m}{L_T} + \frac{\omega V_m}{R_T}\left(\frac{\omega\tau\sin\beta - \cos\beta}{1+\omega^2\tau^2}\right) \qquad \text{(B.9)}$$

As equation B.9 demonstrates, the dI/dt stress on incoming thyristors is inversely proportional to the inductance pre-



$\beta = 3^{\circ}$ $E_{TH} = 205V$ $V_m = 328V$ $\tau = .975$ ms $t_{ON} = 2.75$ ms

Figure B.3. Plot of calculated line current for VSI converter.



Vs 32.7 V/cm; i_d 10.8 A/cm; $V_{aa'}$ 24.7 V/cm, i_s 10 A/cm
Honeywell 1858 Visicorder at 80 in/sec.

Figure B.4. VSI waveforms at 5 kW output.

sent between the d-c voltage source and the utility line. In the limit as $L_T \rightarrow 0$, the rate of change of thyristor anode current $\lim_{L_T \rightarrow 0} {}^{dI_T}/_{dt} \rightarrow \infty$. Since some inductance is present at all utility interconnection points, the thyristor ${}^{dI_T}/_{dt}$ limit may or may not be exceeded. Thus the main purpose of the ${}^{dI}/_{dt}$ reactors is to limit turn on current slope. As Figures B.3 and B.4 also show, a secondary feature is the introduction of some waveshaping into the current pulse trailing edge. This waveshaping will contribute to a reduction in current harmonics and help to increase the total power factor.

Examination of Figure B.4 reveals fine structure at the peaks of the voltage waveform $V_{aa'}(t)$. This detail consists of a step change in voltage $V_{aa'}$ that is a function of thyristor turn off ${}^{dI_T}/_{dt}$ and the a-c side inductance. The ringing is due to line and transformer leakage inductance resonating with distributed capacitance. The ringing frequency as determined from Figure B.4 is approximately 4 KHz. Figure B.5 is a one line diagram of the converter in Figure B.2 during one half cycle at $t = t_{ON}$. At $t = t_{ON}$, the flux change in L_r and L_s is not sufficient to force current $i_d(t)$ into source V_x and a source commutation by V_x and E_{TH} forces the conducting thyristor pair off. As soon as thyristor recovery occurs the voltage $V_{aa'}(t)$

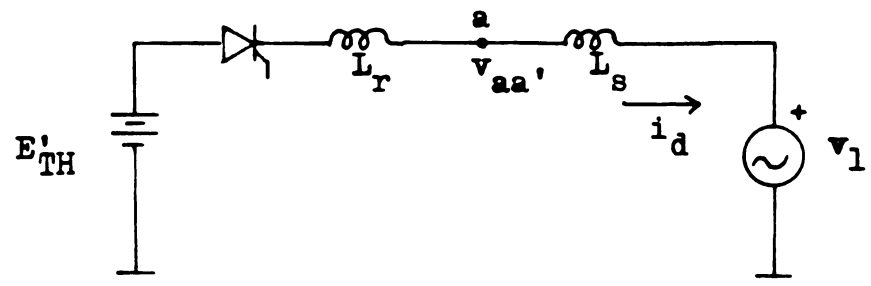


Figure B.5. VSI one line diagram during source commutation.

executes a step change in magnitude of $V_{aa'}$ given in equation B.10.

$$\Delta v_{aa'}(t) = L_s \left.\frac{di_d(t)}{dt}\right|_{t=t_{ON}} \qquad \text{(B.10)}$$

Using equation B.9 and t_{ON} from Figure B.3, the value of $V_{aa'}$ in equation B.10 is approximately 3.7 volts. This agrees quite well with the 1.5 mm step at the peak of $V_{aa'}(t)$ in Figure B.4 at each thyristor pair commutation point. One final comment on equation B.8, as the source generation increases, the defined d-c voltage E_{TH} increases proportionally resulting in the first term of equation B.8 (which defines the target current during each half cycle) increasing in magnitude. The current slope at turn on increases likewise (equation B.9) with the final result that

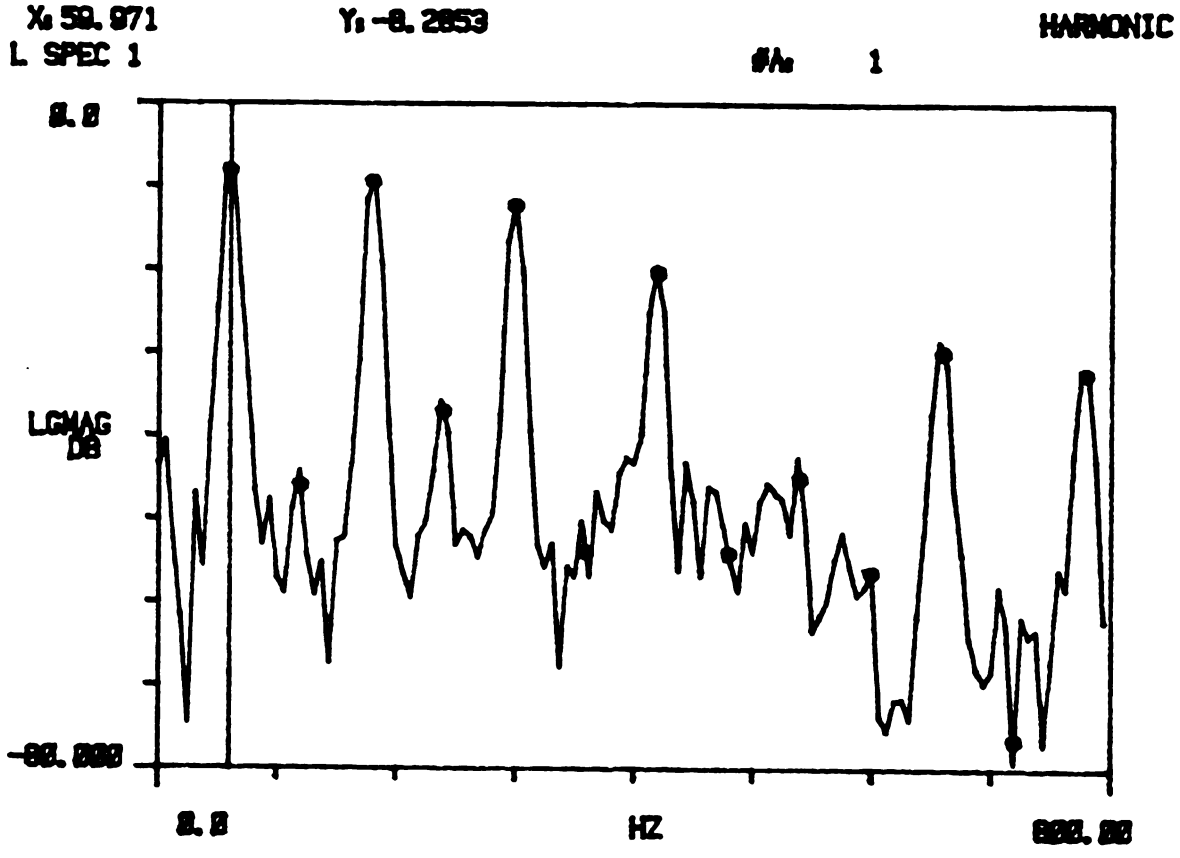


Figure B.6. Spectrum of VSI converter line current.

the current conduction interval t_{ON} remains relatively fixed. From this development, one would not expect to observe any marked reduction in harmonic content of $i_d(t)$ as rated power is approached. Such is indeed the case. Figure B.6 is the log spectrum of the time waveform $i_d(t)$ in Figure B.4. Of particular interest in Figure B.6 is the fact that third and fifth harmonics are comparable in magnitude. This spectral data was obtained from laboratory analysis of a magnetic tape recording of the VSI converter using an FM recorder having flat response from DC to the tenth harmonic. Harmonic data beyond the ninth will not be accurate. Thus the magnitudes of the eleventh and thirteenth harmonic are uncertain.

APPENDIX C

APPENDIX C

CONTROL CIRCUITS FOR PWM CONVERTER

This appendix contains the circuit schematics and analysis of the functional blocks contained in Chapters 4 and 5. Figure 4.3 is repeated here as Figure C.1 in which the main elements are the phase locked loop (PLL), the dual slope integrator and a comparator. Discussion of the phase lead ( ) circuit will be deferred until the PWM control circuitry has been completed. The PLL circuit is drawn in

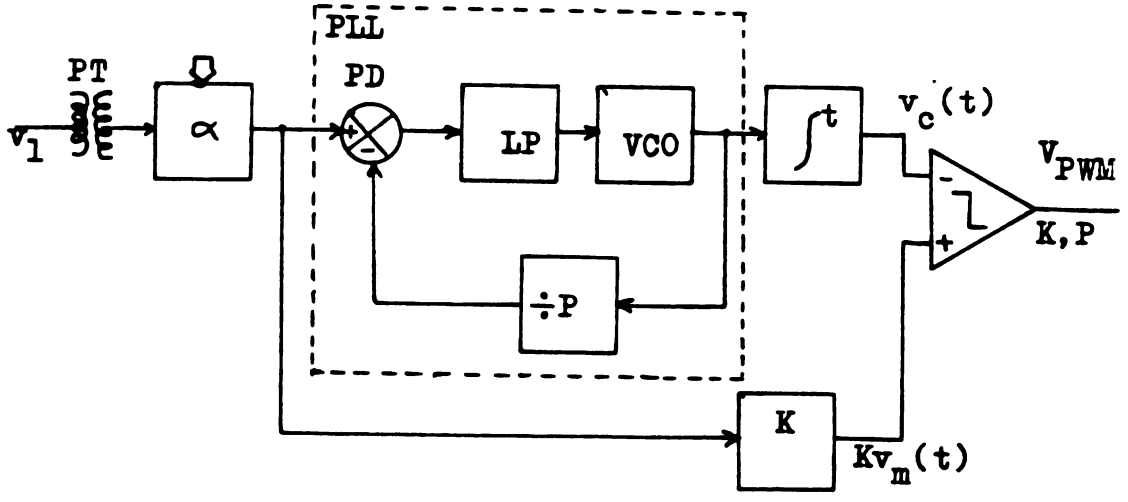
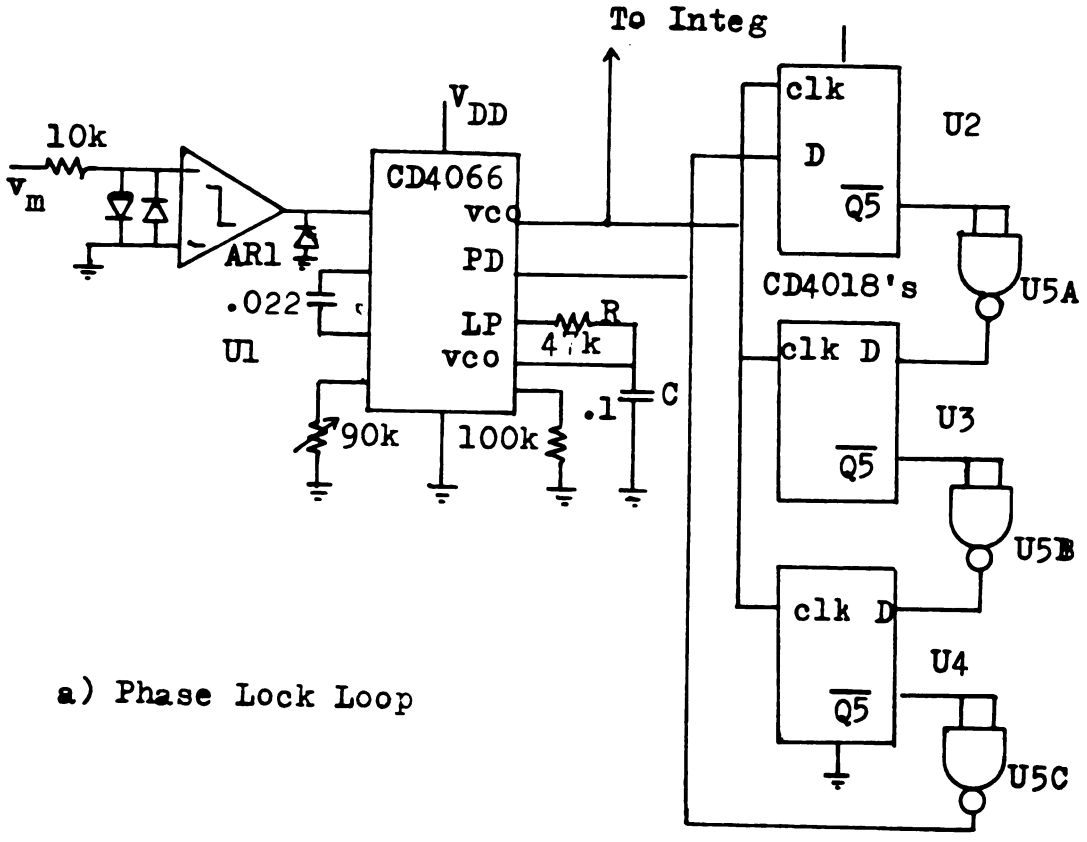


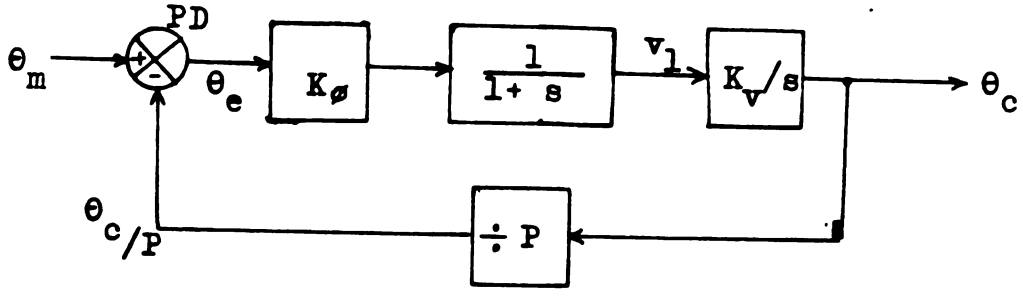
Figure C.1. Functional diagram for natural sampling.

Figure C.2. CMOS devices are used because of their wide supply voltage tolerance and low power consumption. The 60 Hz line reference signal is squared by saturating amplifier AR1. Negative excursion at the output is clamped to protect the PLL input (U1). For a frequency ratio P=30, the voltage controlled oscillator (VCO) must lock at Pf_m = 1800 Hz. Therefore, with the VCO center frequency chosen at this value the PLL will lock to a 60 Hz reference square wave so long as the frequency error remains within the acquisition bandwidth ω_n. This acquisition or lock bandwidth must be sufficient to allow for normal VCO drift and 60 Hz line frequency variation (typically less than ±1 Hz). The low pass filter (LP) has a cutoff frequency of approximately 34 Hz for loop noise rejection. The divide by P function is realized with a 15-stage twisted ring counter U2, U3, and U4 with coupling via inverters U5 A, B, and C. Only essential components and connections are shown.

The PLL circuit analysis is no more involved than a type I second order control loop. The phase detector (PD) has transfer gain K_ϕ volts/radian, the loop filter, G(s) and the VCO transfer gain, K_V radian/volt sec. In Figure C.2b the complete PLL transfer function T(s) can be determined. The VCO transfer function can be obtained as $\omega_c(s) = K_V V_1(s) = s\theta_c(s)$ so that $\theta_c(s) = (K_v/s)\, V_1(s)$. The digital phase detector has a phase at lock of $\pi/2$ radians and $V_1 = V_{DD}/2$ where V_{DD} is the supply voltage. If the output phase increases, the error voltage V_1 is reduced and vice-versa.



a) Phase Lock Loop



b) Functional Diagram

Figure C.2. Detail of PLL circuit and functional diagram.

In this case $K_\phi = {}^1/_\pi (V_{DD} - V_{SS}) = 4.7$ rad/sec., and $K_V = 818.4$ rad/volt sec. Then T(s) is

$$T(s) \triangleq \frac{\theta_c}{\theta_m}(s) = \frac{K_\phi K_V/\tau}{S^2 + 1/\tau\, S + \frac{K_\phi K_V}{P\tau}} \qquad (C.1)$$

$$T(s) = \frac{P\omega_n^2}{S^2 + 2\zeta\omega_n S + \omega_n^2}$$

where τ = RC of the LP function and

$$\omega_n = \sqrt{\frac{K_\phi K_V}{P\tau}} \text{ and } \zeta = \tfrac{1}{2}\sqrt{\frac{P}{K_\phi K_V \tau}}$$

Equation C.1 shows the low pass nature of this PLL. The closed loop 3 dB bandwidth ω_n determines the time to lock. Therefore the response to a step change in phase θ_m of $v_m(t)$ will have a damping coefficient ζ. For this circuit to respond rapidly and yet have low overshoot, it is necessary for ζ to be chosen accordingly. A $\zeta = .7$ is a common and suitable choice. Using this value and the defining relations of equation C.1 yields an expression for the loop filter capacitance C.

$$C = \frac{P}{4RK_\phi K_V \zeta^2} = .08\ \mu F \qquad (C.2)$$

Therefore a value of C = .1 μF is selected for which $\zeta = .64$ and the loop lock bandwidth is $\omega_n = 165$ rad/sec so that this circuit will settle to a step in phase in approximately 24 ms. This means that for operation in the utility phase-locked mode, the system can respond to a change in phase in

less than 2 cycles. In order to achieve such a low lock bandwidth (f_n = 26 Hz, 1.4% of f_c) it is necessary that the VCO center frequency remain within +756 Hz of f_c. The center frequency in Figure C.2a is set by the .022μf capacitor and a 90 KΩ resistor which is trimmed for f_c = 1.8 KHz with P = 30.

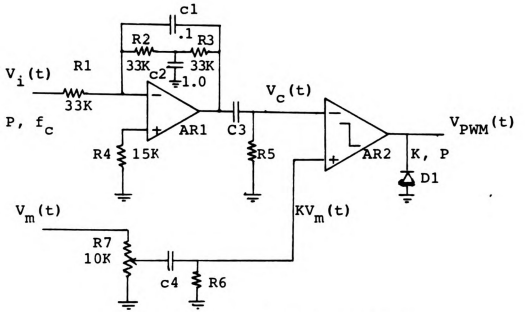
Figure C.3a is the schematic of the integrator and PWM comparator with parameters P and K. The dual-slope integrator consists of amplifier AR1 with transfer function A(s), resistors R1, R2, and R3 and capacitors C1 and C2. Resistor R4 is used to minimize input offset voltage by providing a ground path for input bias current from the non-inverting terminal of AR1 which equals that on the inverting terminal to ground. R4 = R1 $\|$ (R2 + R3) where R1 >> R_0 of the previous stage. The RC feedback network on AR1 has transfer function $T_{fb}(s) = {}^{I_{fb}}/_{V_c}(s)$

$$T_{fb}(s) = \frac{S[C1(R2+R3) + SC1R3C2R2]}{R2+R3(1+S\ R2C2)} \qquad (C.3)$$

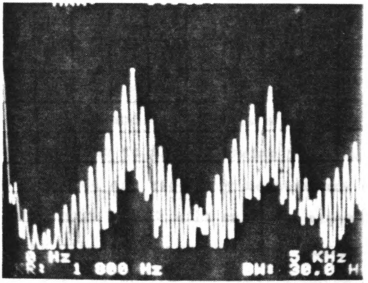
$$\frac{V_{AR1}}{V_i}(s) = \frac{-1}{R1\ T_{fb}(s)} = \frac{R2+R3(1+S\ C2R2)}{S[R1C1(R2+R3) + SC1C2R1R2R3]}$$

where R3C2 = 33 ms >> R1C1 = 3.3 ms > ${}^{2}/_{f_c}$ = 1.11 ms (C.4)

Equation C.4 will result in an ideal integration of K_I/s in the limit as C2$\rightarrow\infty$ with $K_I = -{}^{1}/_{R1C1}$. That is assuming AR1 is an ideal amplifier without dynamics A(s) : $A_0\rightarrow\infty$. In the practical circuit it is sufficient to



a) Integrator and PWM comparator.



b) Spectrum of $V_{PWM}(t)$ for K = .95 and P = 30; 60 Hz line at left is 1.5 dB above marker dot on f_c.

Figure C.3. PWM circuit and spectrum of $V_{PWM}(t)$.

select C2>>C1 such that the inequality given in equation C.4 is satisfied. For the values given in Figure C.3a operating at P=30, results in the given condition being satisfied. The effect of a non-ideal amplifier AR1 transfer function A(s) is to modify the denominator term in equation C.4 to

$$\frac{V_{AR1}}{V_i}(s) \simeq \frac{K_I}{S[1+{}^{1}/_{A(s)}]} \qquad (C.5)$$

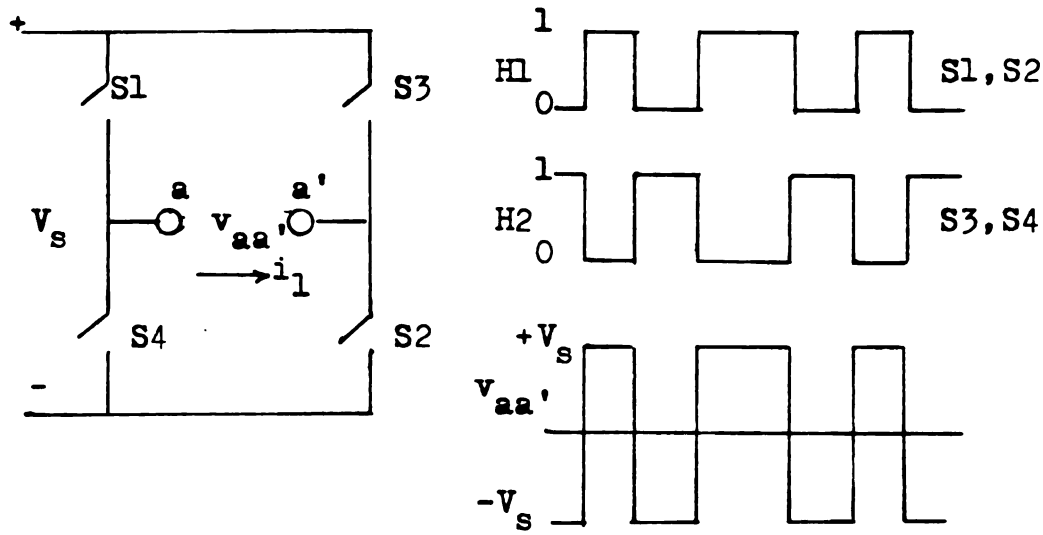
where $A(s) = \frac{GB}{S+\omega_a}$.

Hence, for operation at low frequencies ($\sim 10^3$ Hz) and with a general purpose AR1 having gain bandwidth ($GB \sim 10^6$), the error associated with the non-ideal characteristics can be neglected.

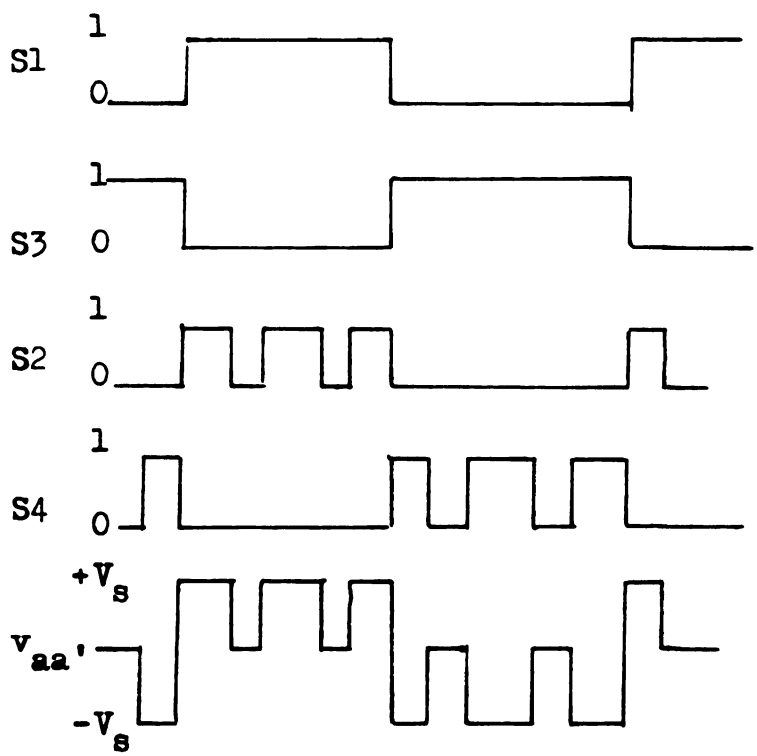
The comparator AR2 is a high gain amplifier operating open loop to achieve fast switching at the intersections of $V_c(t)$ and $KV_m(t)$. Resistors R5 and R6 are bias current return paths for AR2 and diode D1 is a negative voltage clamp for interfacing to the following T^2L logic circuits. Capacitors C3 and C4 are necessary because any d-c offsets present at the input to AR2 will cause an asymmetrical PWM wave. This, as noted in Chapter 4, will result in the generation of even harmonics and their adverse effect on transformer operation. One result of this comparator function is the introduction of pulse jitter in the PWM pulse train. Experimental results show that this PWM jitter is about 5μs. Figure C.3b shows the PWM spectrum of $V_{PWM}(t)$.

This spectrum verifies the analysis given in Chapter 4; only even spectral lines about the odd carrier multiples and odd spectral lines about even carrier multiples (the $2f_c$ line is at -35 dB relative to the 60 Hz line).

Before this PWM pattern can be applied to the bridge driver circuits, a complementary PWM pattern must be generated. In this way the top switch in a bridge pole functions during complementary intervals to the lower switch in the same pole. Figure C.4a describes these PWM patterns for the 2-level case and Figure C.4b for the 3-level case. As Figure C.4a indicates, the switching function H1 causes switching devices S1 and S2 to turn on at its logic 1 level and off at its logic 0 level. The bridge output waveform $V_{aa'}(t)$ will be either $+V_s$ as defined by switching, or existence, function H1 and at $-V_s$ as defined by existence function H2. This circuit operates between either of two states $\pm V_s$ and hence generates 2-level PWM. A second variation of the switching pattern is to operate the top switches S1 and S3 at 50% duty ratio and the lower switches S2 and S4 in the PWM pattern. Except for this case, the lower switch existence functions must be "windowed" by the top existence function of the opposite pole. Figure C.4b illustrates this case of 3-level PWM in which an additional state at 0 Volts is allowed. If the lower switch functions were not selectively blanked, either pole or both would form a low impedance path across V_s and results exactly the same as for a commutation failure described in Appendix B would follow.



a) 2-Level PWM



b) 3-Level PWM

Figure C.4. PWM switching functions.

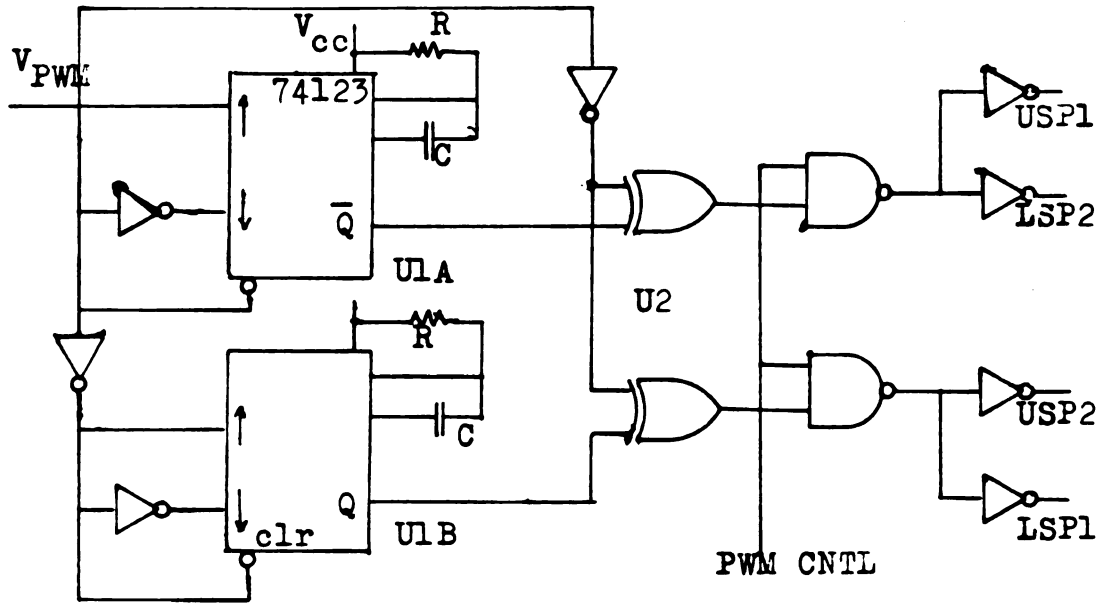
The major advantage of 3-level PWM is that switching losses on half the switches can be reduced because only two commutations per half cycle are needed.

These definitions of bridge switching functions assume ideal devices. Any practical device requires a finite time to reach its ON state and similarly some finite time to regain the OFF state. Should the existence functions shown in either Figure C.4a or b be applied to a bridge circuit with bipolar or thyristor devices, very large pole currents would occur during the turn on of one device and turn off of the remaining device in each pole. These short circuit currents would be especially destructive of bipolar devices since their base drive may be insufficient to hold the transistor in saturation. The attendant large power dissipation would quickly result in transistor failure. The second concern is that circuit inductance is invariably present and the large $^{dI}/dt$ induced voltage transients can easily exceed the bipolar collector to emitter breakdown voltage. If these transients contain sufficient energy, the transistor E_{sb} rating may be exceeded also. The second breakdown that results would then permanently damage the device. The thyristor is much more tolerant of high current surges due to its regenerative characteristics so that power dissipation will not be increased as dramatically.

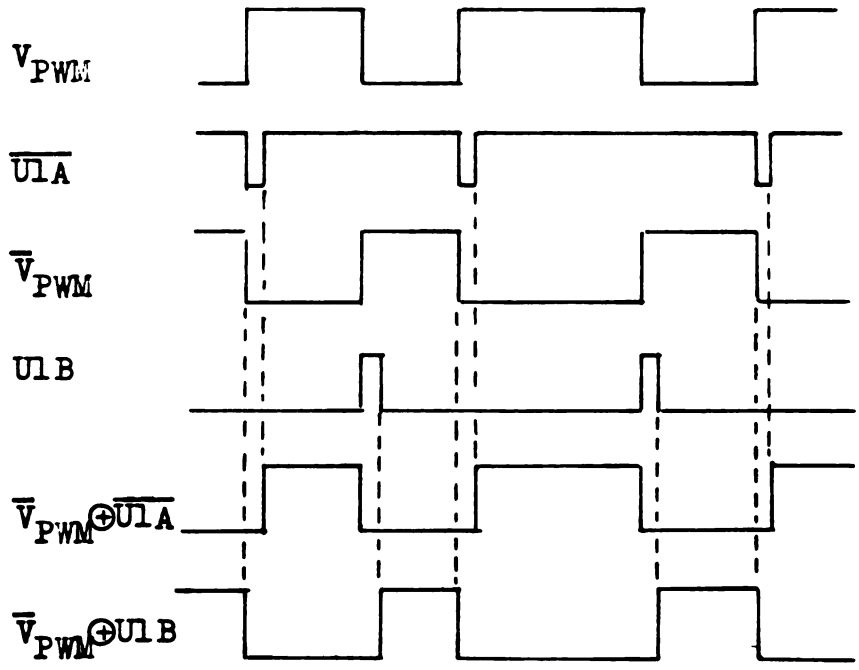
During research on the bridge operation utilizing bipolar devices, the two transistors in one pole were lost due to second breakdown in which the collector became fused to

the emitter as a result of excessive current transients. This resulted because insufficient margin had been allowed for device storage time. Storage time varies with current density and without antisaturation (Baker clamp) circuitry on the transistors, the allowed margin was exceeded. The circuit needed to introduce this switching margin is drawn in Figure C.5a for the case of 2-level PWM. In the 3-level PWM, additional gating is necessary to realize the blanking of alternate half cycles.

The circuit of Figure C.5 operates on the output signal $V_{PWM}(t)$ of Figure C.3a after some logic level translation. The objective is to generate the pair of switching functions H1 and H2 shown in Figure C.4. These existence functions are labeled according to which switch they enable, i.e., USP1 for upper switch pole one, etc. In this circuit, the base PWM wave edges are notched by an amount determined by the RC time constants of U1 A and B. The complementary pair of edge-notched PWM patterns are produced at the output of exclusive OR gates U2. Gate U3 introduces inhibit control over the PWM pattern so that the entire bridge may be shut down by external control. The logic inverter gates of U4 are needed for current drive capability into the intervening device driver stages. The timing diagram of Figure C.5b demonstrates several unique features of this circuit. First, a time lag equal to the RC time constant is introduced into the PWM existence functions. This means that the fundamental component will lag the line waveform $V_{\ell}(t)$

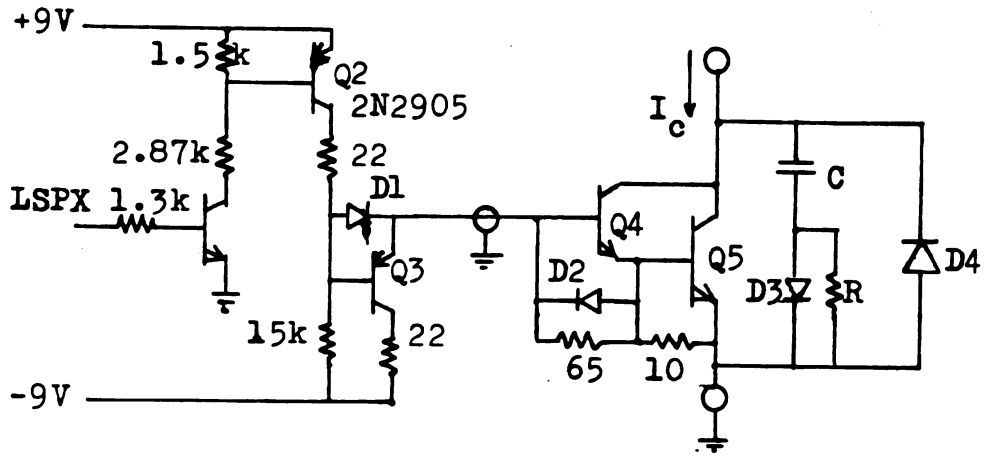


a) PWM programmable commutation margin circuit.

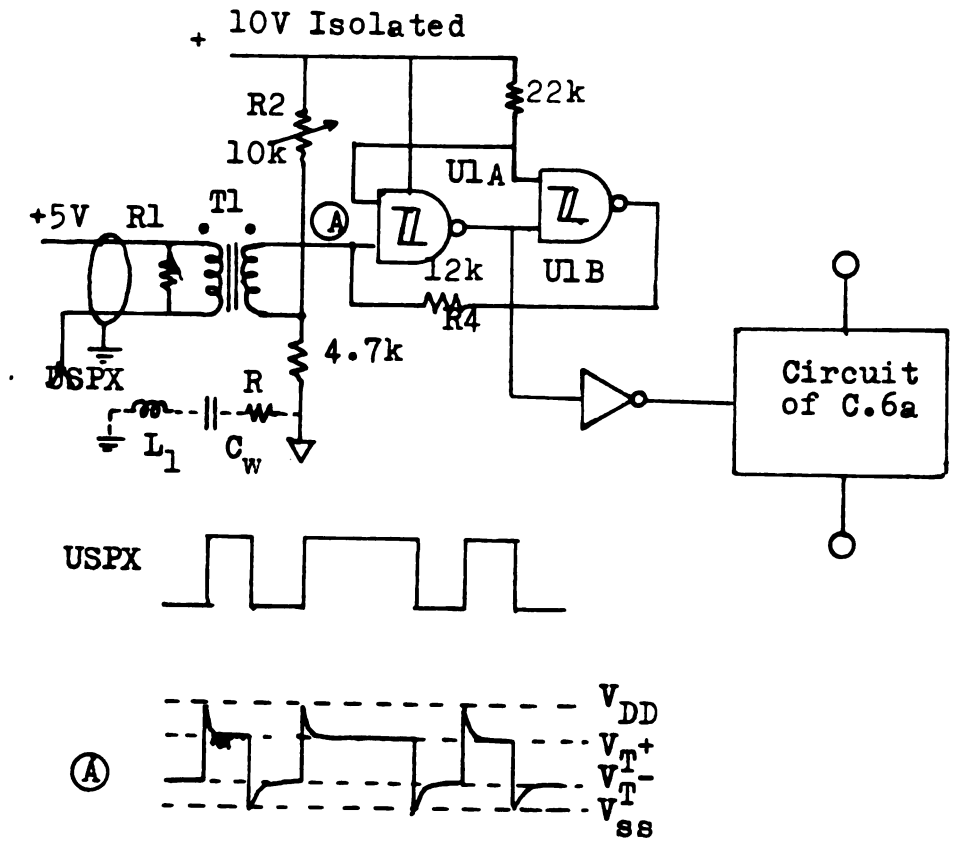


b) PWM complementary existence functions with commutation margin.

Figure C.5. Commutation margin circuit and waveforms.



a) Driver circuit with connected BJT switch.



b) Pulse reconstruction.

Figure C.6. PWM driver circuit.

by RC seconds. Second, the existence functions H1 and H2 mesh with programmable margin on both leading and trailing edges. Therefore, with turn on of sufficient margin, switching rise times and fall times and storage delay can be accommodated. Third, due to unequal propagation times through these devices, the occurrence of 10 ns delay differences are observed in both H1 and H2 at the beginning of the notch. This unavoidable effect can be compensated by increased capacitive loading in the subsequent driver (Figure C.6).

The driver stage was designed so that, with minor changes, either bipolar or thyristor devices could be switched. The input is compatible to T^2L logic or paralleled CMOS. Since the inverter bridge can have one side grounded in the transformer coupled case the driver stage couples the logic signal from Figure C.5 directly to the main switches (low side of all poles). That leaves the upper switch driver referenced to a common which switches rapidly between ground and $+V_s$. This requires to individual isolated supplies.

Figure C.6 shows the driver connected to a BJT main switch element. In this case the collector load resistors of both Q2 and Q3 are chosen for equal IB1 and IB2 drive to the Darlington connected switch. When the gate turn off (GTO) thyristor was used the necessary current source turn on drive was realized by adjusting the collector load of Q2. To provide a voltage source turn off drive the collector

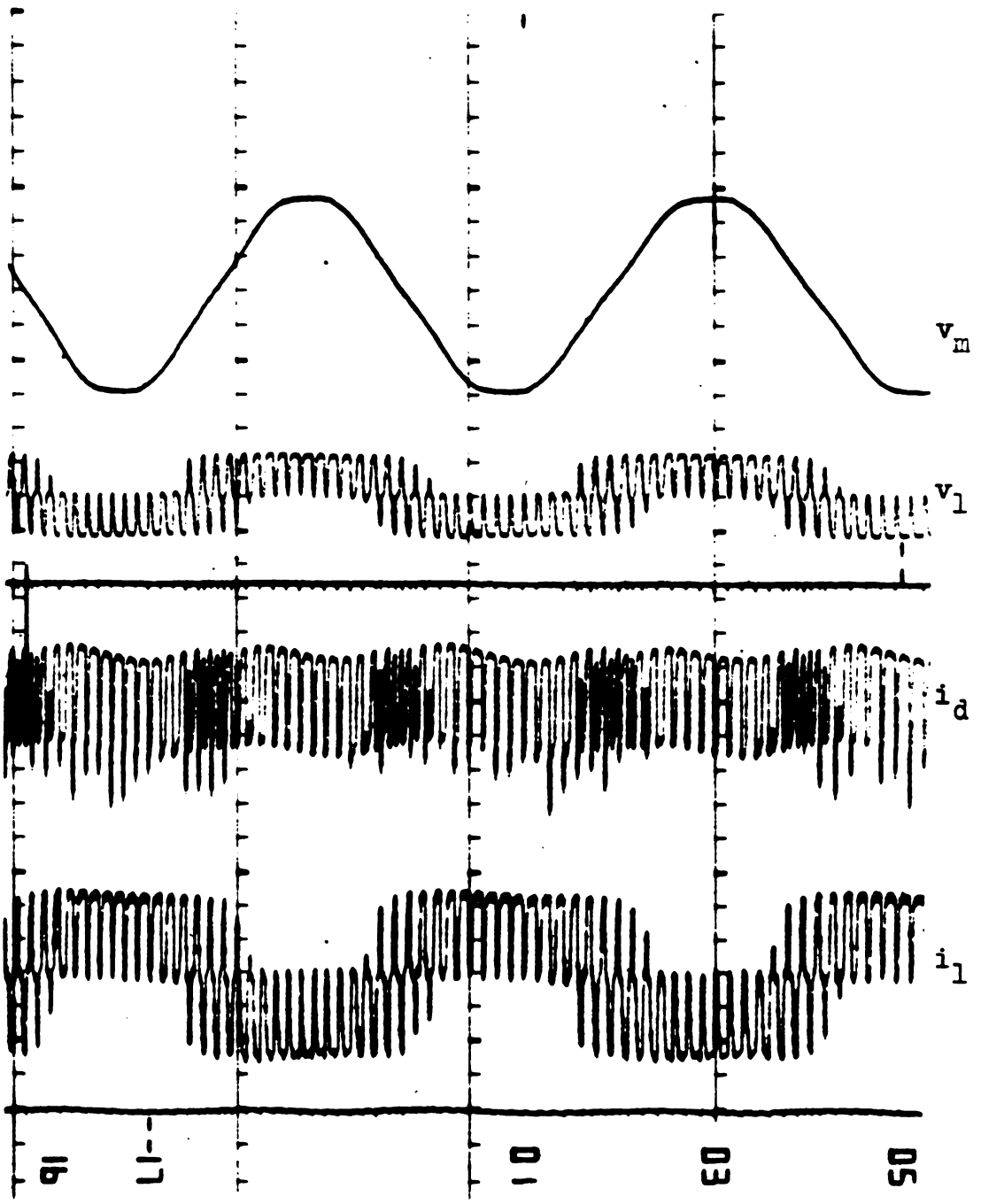
load on Q3 was reduced to zero. The supply voltage is below the avalanche potential of the GTO so that gate-cathode breakdown is prevented. A quick analysis of this circuit shows that it has two stable states which are dependent on the logic drive signal.

The circuit to the upper switch drivers is complicated by the need for operation isolated from ground. Several methods for sending the PWM switching functions to the isolated drivers are feasible. Three different methods were investigated. The use of both opto-isolators and transformers were tried. When using an opto-isolator with PWM it was found that the photo-transistor response was slew limited so that narrow PWM pulses were distorted. The lamp diode voltage signal retained the input PWM shape. In lieu of this shortcoming a pulse transformer was used. Because it takes a substantial transformer to pass logic level signals undistorted (low droop) the pulse differentiation approach was taken. In this method the PWM logic signal drives the pulse transformer so that a differentiated pulse pattern appears at its secondary. The PWM pattern is then reconstructed at the isolated ground by the Schmitt trigger latch (Figure C.6b). The small core transformer T1 has a 50×10^{-6} volt-second product, so it cannot pass the widest (500μs) PWM pulses. The load R1 on transformer T1 damps ringing when the core resets after each pulse. By empirical adjustment the best noise immunity was found to occur when the memory hysteresis adjustment R2 was increased to the

This is potentially damaging when U1A is such that its corresponding switch must be held OFF. Gating an OFF device back ON causes bridge overlap conduction to occur.

This phenomena was verified by replacing the small pulse transformers with audio quality transformers capable of passing the PWM pattern undistorted. In this case both L_ℓ and C_W were higher ($C_W \sim .003\mu F$) so that the overlap conduction problem was easily induced (a limiting resistor was added between $+V_s$ and the bridge to prevent device damage). By plotting the susceptability to failure (level of V_s) versus the ratio of notch margin to oscillation period ($T_O \sim 15\mu s$) it was found that the circuit was relatively immune for odd integer multiples of notch margin to oscillation period. This confirms that the second peak in successive odd periods of the oscillation falls within the notch margin (no bridge conduction). It also means that in this application pulse transformer design is very critical.

Performance of the circuit in Figure C.4 was next assessed using the existence functions of Figure C.4b. The upper driver circuit was modified to handle the required 50% duty ratio or 8.3 ms ON pulses for 3-level PWM. This change resulted in the circuit of Figure C.6 being replaced with a HF carrier source and an envelope detecting circuit in place of the Schmitt trigger latch. The idea was to blank a 350 KHz square wave oscillator, a propagation delay type using coupled monostable multivibrators, at intervals of 8.3 ms



Honeywell 1858 Visocorder at 160 in/sec.

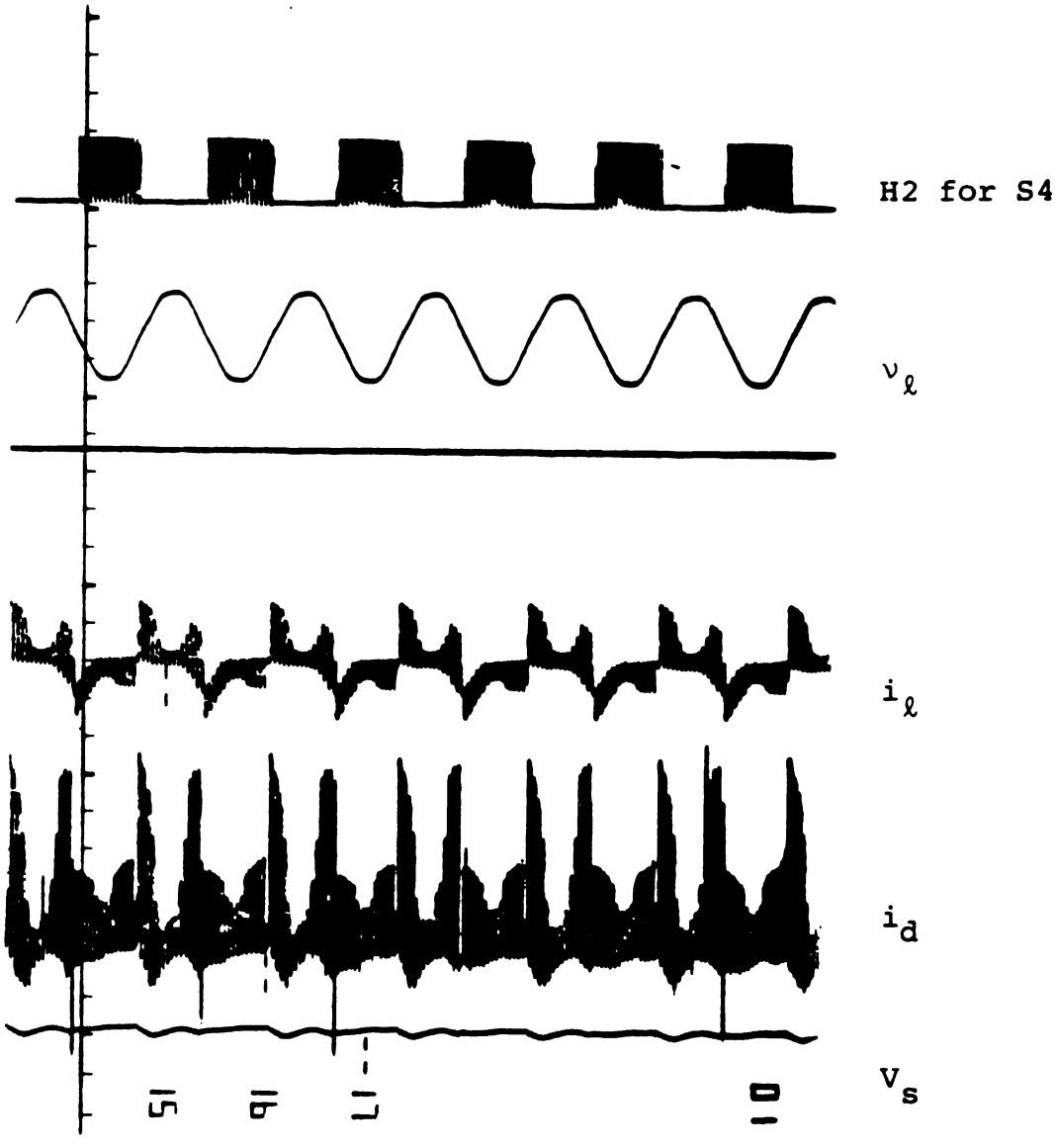
Figure c.7. 3-level PWM into a resistive load.

and send alternate pulses to switches S1 and S3 by way of the same pulse transformers. The driver was next converted into an envelope detector (circuit of Figure C.6a) by adding 384 pF of capacitance from the collector of Q1 to the anode of D1. With a transformer coupling the bridge to a resistive load on its secondary, the oscillograph recording of Figure C.7 was obtained. In this recording waveform $V_m(t)$ is the modulating signal (60 Hz reference) and $V_\ell(t)$ is the output voltage across the load resistor (no filtering). Current $i_d(t)$ is the d-c source current and $i_\ell(t)$ is the resistor current. The trace for $i_d(t)$ clearly shows that the transformer magnetizing current occurs at the zero crossings of $V_m(t)$. The current is positive but makes negative excursions (energy returns to V_s) when a reactive load, either lagging or leading, is connected.

Both currents $i_d(t)$ and $i_\ell(t)$ reveal a source of trouble which befell this experiment. The current pulses $i_d(t)$ are several amperes in magnitude, have large rates of rise and fall, and so are a source of significant levels of interference. With such a source of both conducted and radiated emissions, shielding of the PWM controller became a necessity. Before the results in Figure C.7 could be obtained, the entire driver circuit had to be enclosed in a magnetic shield and all low-level signal leads to the driver had to be replaced with shielded twisted pair. It was found experimentally that radiated magnetic fields, even though attenuating at r^{-3}, were the single most significant cause

of induced voltage transients. Hence, ferrous metal shielding and the minimization of signal lead loop areas proved to be the most reliable cure.

With this knowledge of how a 3-level PWM converter performs, the transformer secondary (rated for 120 V_{rms} 60 Hz) was connected to the utility 120 V line. This resulted in some interesting findings, as shown in Figure C.8. For the fundamental component of the PWM waveform to be coincident with the line voltages, phase lead had to be introduced ahead of the phase locked loop. This lead circuit is shown in the functional diagram in Figure C.1 with inputs from a potential transformer (PT) for the line reference signal and a vector input consisting of the four lines D0,...,D3. The first candidate circuit investigated for this application was straightforward--use a phase-lead circuit. This proved to be an unwise choice. Although it was known that phase lead is very noise and high-frequency susceptible, perhaps an introduction of a lag pole just beyond the lead pole would suppress these undesired effects and still retain an overall phase advance. This idea did work and, in fact, the results shown in Figure C.14 were obtained using it. However, the line THD levels of some 4% were very effectively magnified at the output of this lead circuit--especially the third and fifth harmonic. The resulting output began to look like a stepped wave approximation to a sinusoid. The following low-pass filter did remove a great deal of this distortion with a consequential



Honeywell 1858 Visicorder at 40 in/sec.

Figure C.8. 3-level PWM line connected.

reduction in the phase advance. This difficulty was overcome by replacing this design by a two- stage lag plus inversion of the line 60 Hz reference signal. This amounts to a tradeoff between distortion and time. By introducing in excess of 90^{o} of phase lag to the line reference signal, nearly one half of a 60 Hz cycle has gone by (no time is lost because of the 180^{o} inversion). The resulting phase lead circuit is drawn in Figure C.9.

The signal labeled H2 is the blanked PWM existence function for switch S4 and is representative of this technique. The line reference is $V_{\ell}(t)$ at the output of the potential transformer and the lower trace $V_s(t)$ shows the ripple produced on the defined source V_s. The traces for currents $i_d(t)$ and $i_{\ell}(t)$ were obtained using wideband torodial current transformers (CT) in the appropriate leads of Figure C.4. Notice the resemblance between current $i_{\ell}(t)$ and that for the VSI line commutated converter in Appendix B. The operation is similar. For d-c supply voltage V_s greater than the a-c peak, V_m current flows over the full half cycle. The bathtub shape of this current is due to the large potential across the transformer leakage inductance at the line voltage $V_{\ell}(t)$ zero crossings. This illustrates a disadvantage of the 3-level PWM inverter in a utility connected application. The method can be expected to produce similar waveshapes in a motor drive application due to the counter emf of the motor. By operating the PWM inverter at higher frequencies the integrating action of

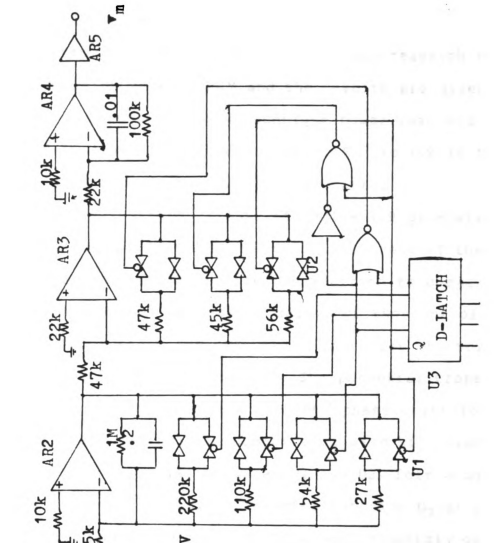


Figure C.9. Phase lead circuit

transformer magnetics would greatly enhance filtering out the 60 Hz component.

The remaining experimentation in this research was performed using 2-level PWM and the results are given in Chapter 4. When using this technique phase lead was provided in digitally encoded steps. Figure C.9 is the circuit used for 15 step (2.9°/Bit) control.

The phase advance circuit of Figure C.9 generates the phase angle by which the fundamental component of the PWM waveform leads the line voltage in addition to compensating for internal signal processing delays of the controller. Amplifer AR1 buffers the output and increases the voltage level of the RC 90° lag network. The potential transformer polarity is chosen to give a net 180° phase shift to V (t). Amplifiers AR2 and AR3, in conjunction with high speed bidirectional transmission gates U1 and U2, form a binary stepped phase lag circuit. Transfer function $G_2(s)$ consists of a 2^4 step phase lag followed by a complementary gain equalization stage. In applications requiring variable modulation depth the gain of amplifier AR4 can be made adjustable. Amplifier AR5 is a unity gain current driver. The regulator U4 biases the substrate of gates U1 and U2 below the maximum negative signal swing to be encountered. The

$$G_1(s) = \frac{K}{1+S\tau_1} \doteq \frac{K_1}{S} \; ; \text{ where } K_1 = {}^{K}/_{\tau_1} \text{ and } \omega\tau_1 >> 1$$

$$G_2(s) = \left(\frac{-K_N}{1+S\tau_N}\right)\left(\frac{-K_2}{K_N}\right) = \frac{K_2}{1+S\tau_N} \; ; \; N = 1,2,\ldots,2^4$$

$$G_3(s) = K_3 \qquad \text{(C.6)}$$

$$G(s) = G_1G_2G_3(s) = \frac{K_1K_2K_3}{S(1+S\tau_N)}$$

$$\angle G(j\omega) = -\pi/2 - \tan^{-1}\omega\tau_N$$

$$\angle G(j\omega) = -3\pi/2 - \tan^{-1}\omega\tau_N \quad \text{including PT polarity}$$

argument of G(jω) shows that the argument of the overall transfer function lies between $-3\pi/2$ and -2π radians in N-steps. In this way the necessary phase advance for VSI converter operation has been achieved. Furthermore, this advance angle is now under digital control.

The cascade converter described in Chapter 5 can be described as a R-I-W technique where the basic power conditioning techniques [3] are R - regulate, I - inversion, and W - waveshape. The R-I-W topology is chosen so that regulation of the random source is followed by the inversion and waveshape function. The circuits used to reallize this regulation function comprise a closed loop system in which feedback controls the duty ratio D of a pulse modulator. Various feedback schemes have been evaluated in order to assess the converter response. Both oscillograph and chart recorder plots of the time response of duty ratio D have been obtained in the laboratory using electronic encoding of duty ratio. This encoding was performed digitally so that the lag present, had analog techniques been applied, could be avoided. These circuits are shown in the figures below.

Figure C.10 is a detailed version of Figure 5.4 for the input regulator. In this Figure R5 is used to set the steady state duty ratio D which, in turn, controls V_s.

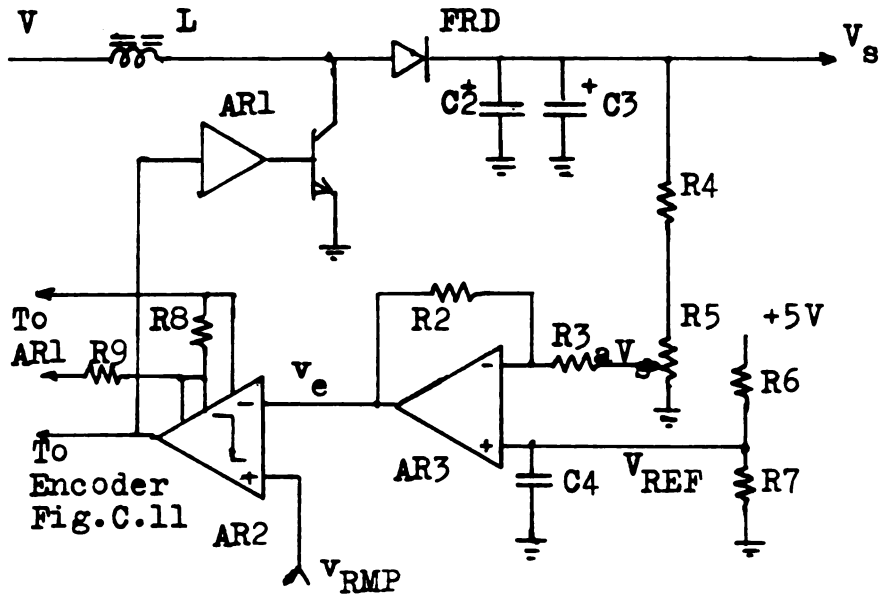


Figure C.10. Regulator control circuit.

Automatic voltage control of V_s for reactive voltampere adjustment would constitute another control loop in which R5 is replaced with an element controlled by the a-c line voltage. This can also be accomplished digitally. Amplifier AR1 is the main switch driver which is similar to the circuit of Figure C.6a. Amplifier AR3 is the feedback error amplifier and AR2 the pulse modulator. Resistors R8 and R9 are connected to the emitters of the Wilson active load on the input circuit of comparator AR2. By sampling the driver switching signal, about 200 mV of hysteresis can be obtained. In this manner, the pulse modulator performs

clean switching at the intersections of the error signal V_e (t) and the internally generated ramp function $V_{rmp}(t)$. The effective feedback gain can be found by analysis of Figure C.10. A fraction of the defined output voltage V_s is available at the error amplifier AR2 inverting input as aV_s. At the noninverting terminal, a preset reference voltage level is present for comparison with aV_s. Thus, the error amplifier transfer function $G_a(s)$ can be determined.

$$V_e = -K_a(aV_s) + (1+K_a)V_{REF} \qquad \text{(C.7)}$$

where $a \geq 0$ and $K_a = R2/R3$

$$V_e + \hat{V}_e = -aK_aV_s - ak_a\hat{V}_s + (1+K_a)\,V_{REF} \qquad \text{(C.8)}$$

Taking the small signal component of equation C.8

$$G_a(s) = \hat{V}_e/\hat{V}_s(s) = -aK_a$$

The effective feedback gain can now be derived as

$$H_e(s) = K_mG_a(s) = -aK_aK_m \qquad \text{(C.9)}$$

The circuit used to digitally encode the duty ratio D is shown in Figure C.11. In this circuit, a high frequency clock signal is gated into an eight stage counter U3. The gating signal is a buffered and inverted replica of d(t) shown in figure C.10. During the low portion of this signal DT_s, the gate IC U2 is enabled. This permits clock pulses buffered by U1B to enter the clock input of counter U3. The clock itself is a CMOS inverter biased into its linear

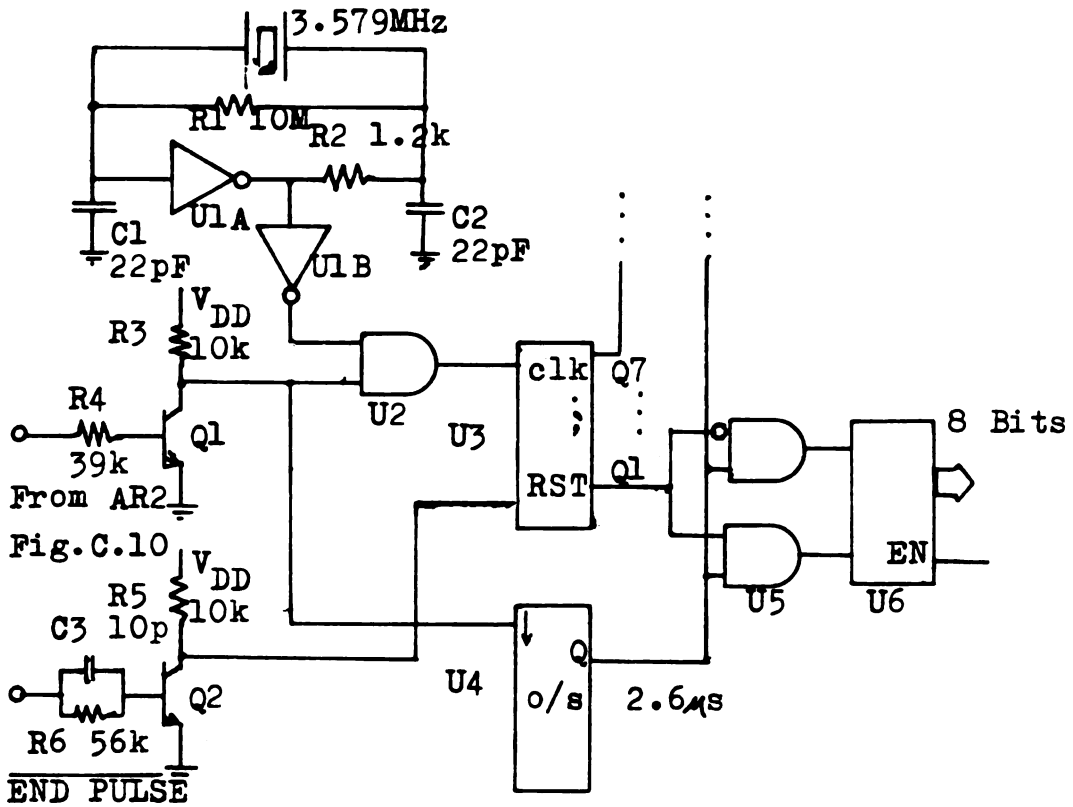


Figure C.11. Duty ratio encoder, resolution 263 ns.

region by resistor R1 (to $V_{DD}/2$). Resistor R2 limits overdrive of U1A and in this circuit must be less than 22 K so that the Barkhausen condition can be met. At the end of the interval DT_s the negative slope of the pulse on Q1's collector triggers a monostable multivibrator U4. The Q output of this IC gates the output of the counter U3 through a series of AND gates U5 into an R-S tristate latch UG. At the completion of the prescribed switching interval T_s, the pedestal on $V_{rmp}(t)$ Figure C.10 is routed through level shift transistor Q2 into the reset pin of U3. In this way,

the counter is always cleared prior to the start of the following interval. The previous count remains latched into U6 where it is available on the 8 bit bus for asynchronous decoding using a digital to analog converter (DAC) and buffered for input to a recorder. At the clock frequency given, the resolution of 263 ns is sufficient for 8 bit encoding of the complete interval T_s.

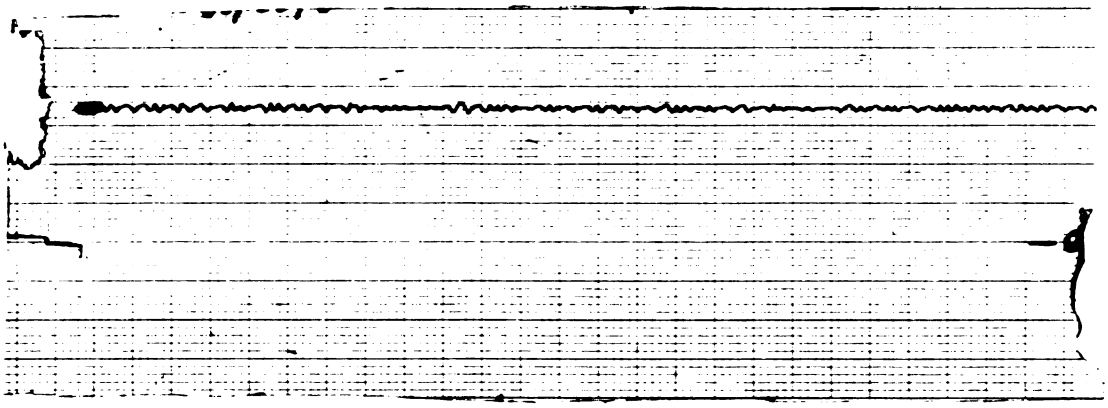
$$T_s = 2^8 \times 263 \times 10^{-9} = 67\mu s.$$

Using this circuit in conjunction with the closed loop regulator allows an assessment of the dynamics present in duty ratio to changes in load. Figure C.12a shows the encoded duty ratio of Figure C.10. In Figure C.12b and c the response to a step change in load is shown. Here, the change in damping is apparent as D is increased. For stable closed loop operation, the zeros of the return difference $1 + G_d H_e(s)$ must have negative real parts.

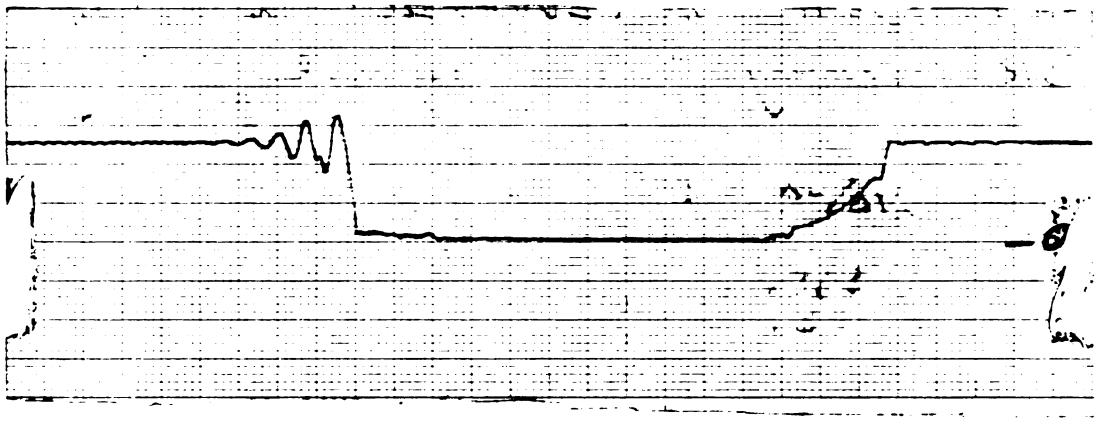
$$1+G_dH_e(s) = S^2+\left(2\zeta\omega_n+aK_aK_m\ {}^{X1}/_{C}\right)S + \left(\omega_n{}^2-aK_aK_m\ \frac{\omega_n^2}{D}\ X_2\right) = 0 \qquad \text{(C.10)}$$

In equation C.10 zeta and omega n are parameters of the power stage. Parameter a is the fraction of the output voltage such that $aV_s = 2.5$ volts. K_m is the pulse modulator gain in units of per volt. By the Hurwitz criteria,

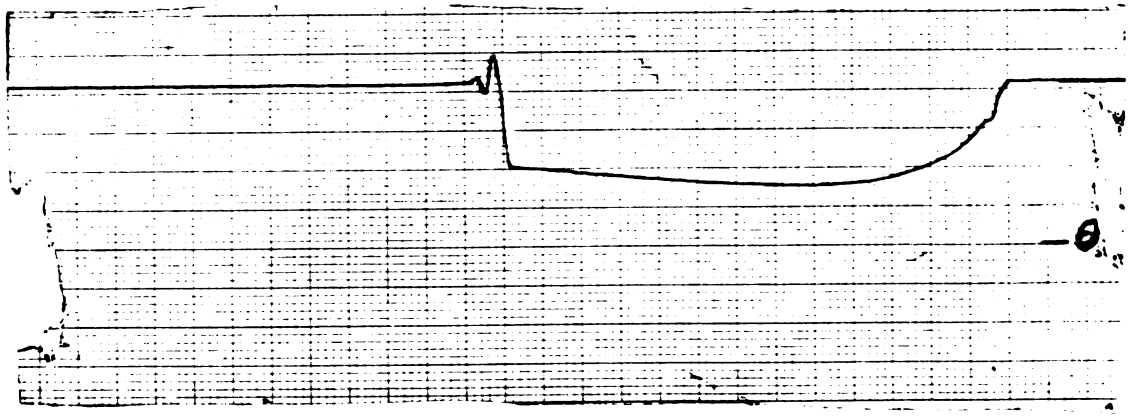
$$2\zeta\omega_n + aK_aK_m\ {}^{X1}/_{C} > 0 \qquad \text{(C.11a)}$$



a) Trace of D + d(t) for gain only case.
D = .4 V_s = 25V, K_a = 25, a = .1



b) D = .4 V_s = 25V R_L = 23,∞,23.



c) D = .6 V_s = 37.5V R_L = 23,∞,23 100 mm/sec

← t

Figure C.12. Duty ratio d(t) step response.

$$\omega_n^2 - aK_aK_m\omega_n^2/D'X_2 > 0 \qquad \text{(C.11b)}$$

Equation C.11a is always satisfied. However equation C.11b implies that the error amplifier gain K_a is constrained to

$$K_a < \frac{D'}{aK_mX_2}$$

This means that error amplifier gain must be lowered as larger boost ratios are attempted. Figure C.13 illustrates

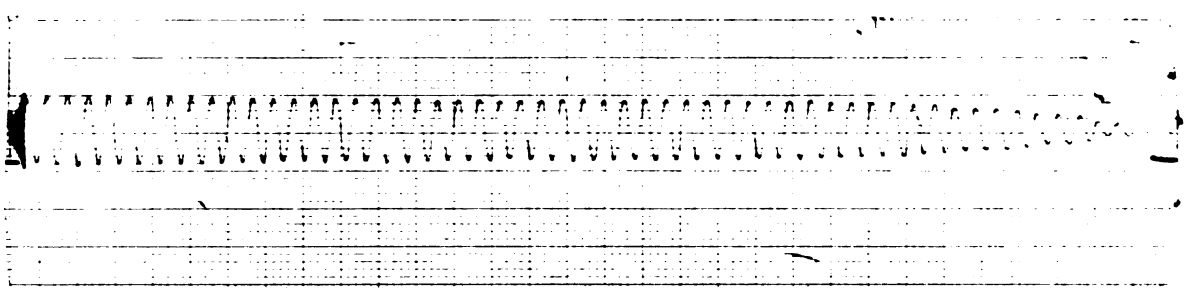
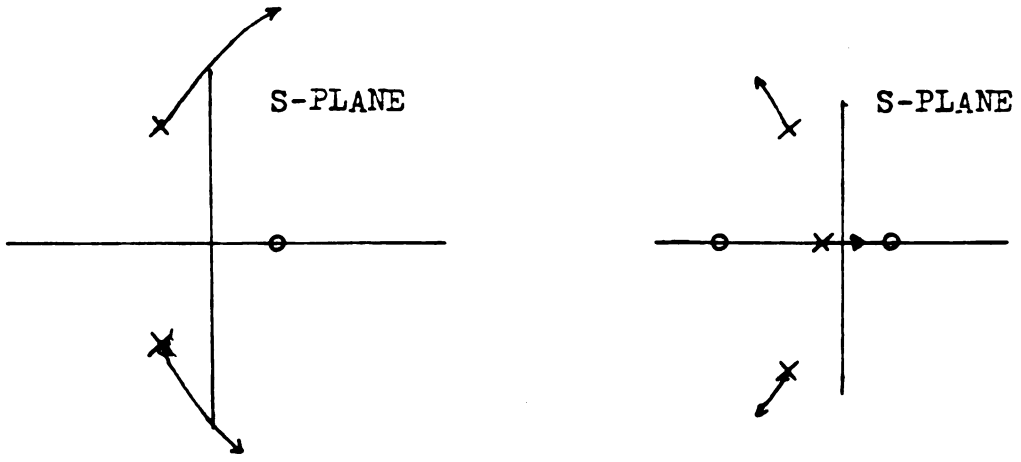


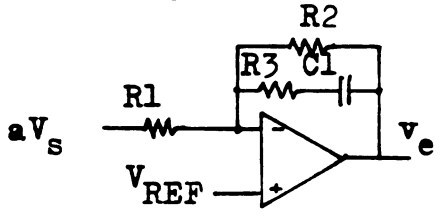
Figure C.13. Limit cycle in d(t) for excessive gain.

the limit cycle behavior of d(t) when equation C.11b is not satisfied. A look at the pole migration for the regulator is shown in Figure C.14a and b. The non-minimum phase nature of $G_d(s)$ causes instability problems. The proximity of the open loop poles to the imaginary axis requires K_a to be small. As shown in Figure C.14b, an error amplifier with lag-lead compensation maintains the conjugate poles in the



a) Gain only

b) Lag-Lead compensation



c) Circuit

Figure C.14. Error amplifier with compensation.

LHP. The lag pole, however, is now free to cross into the RHP. A circuit to realize this lag-lead function is shown in Figure C.14c. Its transfer function is:

$$\frac{\hat{V}_e}{\hat{V}_s}(s) = -a\,\frac{R_2R_3}{R1(R2+R3)}\cdot\frac{S + {}^{1}/_{\tau_Z}}{S + 1/\tau_p} \qquad \text{(C.12)}$$

where $\tau_z = C1R2 < \tau_p = C1\ (R2+R3)$.

Investigation of the return difference for this feedback scheme shows that the characteristic polynomial is cubic. The necessary stability conditions are:

$$2\zeta\omega_n + \frac{1}{\tau_p} + aK_mK_a' {}^{X1}/_{C} > 0$$

$$\omega_n^2 + 2\zeta \frac{\omega_n}{\tau_p} + a\frac{K_m K_a' X_1}{C\tau_z} - \frac{aK_m K_a' \omega_n^2 X_2}{D'} > 0$$

$$\frac{\omega_n^2}{\tau_p} - \frac{\omega_n^2 X_2}{D'\tau_z} aK_m K_a' > 0 \qquad K_a' = \frac{R2R3}{R1(R2+R3)} .$$

This last inequality requires that the error amplifier gain satisfy

$$K_a' < \frac{\tau_Z}{\tau_p}\left(\frac{D'}{aK_m X_2}\right) = \frac{\tau_Z}{\tau_p} K_a \qquad \text{(C.13)}$$

Tests using this feedback scheme again produced limit cycle behavior. This behavior is intuitive since the regulator is essentially a gain element with gain always greater than one. Therefore, additional loop gain in the form of error amplifier gain will only aggravate the situation. The conclusion is that low gains are needed. With a random input to the regulator its output will also exhibit fluctuations. The lack of regulator performance using these methods forced a complete revision of the control structure.

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