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ELECTRICAL AND THERMAL INTERFACES FOR ON-CHIP ELECTROCHEMICAL BIOSENSOR ARRAYS

presented by

Nicholas P. Trombly

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ELECTRICAL AND THERMAL INTERFACES FOR ON-CHIP ELECTROCHEMICAL BIOSENSOR ARRAYS

By

Nicholas P. Trombly

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ABSTRACT

ELECTRICAL AND THERMAL INTERFACES FOR ON-CHIP ELECTROCHEMICAL BIOSENSOR ARRAYS

By

Nicholas P. Trombly

Recent advances in bioelectronic and biomimetic interfaces composed of proteins tethered to planar electrodes offer a unique opportunity to monitor biological activity at the most basic level. Integrating these biointerfaces with microelectrode structures and microelectronics permit the development of miniaturized electrochemical biosensor array platforms that inherit many of the advantages of microfabrication, namely repeatability, scalability, low cost, rapid response, and high sensitivity. Further, the fabrication technologies associated with Micro-Electro-Mechanical Systems (MEMS) can be utilized to permit thermal control of individual electrode sites, enabling programmable control of assay temperatures, which is highly desirable in protein studies. This thesis describes the fabrication and characterization of thermally controlled electrode arrays formed on the surface of 3mm x 3mm CMOS chips. Careful development of post-CMOS compatible process sequence for on-chip electrochemistry is described, which will assist in the development of biosensor microsystems that could yield dramatic breakthroughs in medicine and the life sciences.

To my parents,

Kirk and Christy Trombly,

who make everything possible

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* Note, images in this thesis are presented in color

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Chapter 1. Introduction

Cell membranes efficiently perform a diversity of essential physical, chemical and electrical functions at the molecular scale, including catalysis, molecular transport, recognition, signal transduction, energy generation, and maintenance of transmembrane potential gradients. These processes involve complex, poorly understood interactions between multiple components, including one or more membrane protein(s) and a bilayer lipid membrane (BLM). The recent development of biomimetic interfaces consisting of membrane proteins incorporated into synthetic lipid bilayers on a microelectrode offers a unique opportunity to monitor cell-membrane processes at the most basic level. Such studies could yield dramatic breakthroughs in medicine and the life sciences, but are virtually impossible with existing tools. In addition, electrochemical biosensors based on biomimetic interfaces boast outstanding potential for development of high-density sensor arrays able to continuously monitor multiple analyte concentrations with high sensitivity and specificity. The nanoscale dimensions of proteins and lipid bilayers offer unprecedented opportunities for miniaturization, portability and rapid response. These biosensor arrays would have broad relevance, including measuring the concentrations of multiple metabolites in biological fluids for biomedical applications, monitoring pollutant levels for environmental applications, and detecting chemical and biological threat agents for homeland-security applications.

Micro-Electro-Mechanical Systems (MEMS), the integration of mechanical elements with electronic circuitry on a common substrate, offer a perfect platform upon which to base these biosensors. MEMS devices, typically fabricated on existing silicon

already containing electronic circuits through microfabrication processes commonly employed during the integrated circuit fabrication process, offer some of the same advantages inherent in IC fabrication, namely repeatability, scalability, low cost, small size, and high density capability. These microfabrication processes provide a conveniently ideal opportunity to simultaneously miniaturize electrode arrays and interface them with CMOS control, readout, and support circuitry, resulting in low cost, high density, high precision, robust, multi-element detecting biosensors with enhanced analyte sensitivity. This thesis proposes techniques to utilize post-CMOS microfabrication techniques to create the thermal and electrochemical interface for these sensors.

1.1 Motivation and Previous Research

Recently, the demand for miniaturized, integrated biosensors that can simultaneously measure multiple analytes has skyrocketed for a wide range of molecular analysis applications. These types of biosensors can best be realized using technologies associated with integrated microsystems [1, 2]. The potential impact of low-cost, portable, biochemical instruments on data collection has been compared to the impact of microprocessors on data processing [3]. This thesis seeks to address these needs by developing a new sensor array interface that allows internal CMOS data collection systems access to a scalable array of sensor elements.

The use of silicon as a substrate for solid-supported membrane arrays has been widely reported [4-6]. The fabrication of metal electrodes on the surface of integrated circuits is a well know process. Complete 3-electrode electrochemical cells, including thin film Ag/AgCl reference electrodes, have been integrated on silicon chip surfaces [7], and

Nafion cation-exchange membranes and polyurethane coatings have been utilized to improve reference electrode stability and extend operation lifetime [8-10]. However, to date, there have been limited efforts to fully integrate electrochemical sensors, including on-chip reference electrodes, monolithically with interface electronics, and those that have been reported [11, 12] incorporate for ISFET chemical sensors with very different characteristics than bioeletrochemical sensors and neither address key issues associated with integrating high density sensor arrays.

Additionally, it has been shown that different sensing proteins benefit from increased lifetime and/or reactivity when held at an optimal temperature. To date, thermal control of sensors has been widely reported [13]. The fabrication, characterization, and isolation of polysilicon micro-hotplates are well established processes. However, the literature has primarily been limited to gas sensors incorporating a thermopile sensing element on the substrate surface. These systems are vastly different from the biosensors this work is targeting. This thesis proposes a post-CMOS process enabling the formation of thermally controlled and isolated microelectrode array sites suitable for biomimetic and bioelectronic protein attachment on existing CMOS circuitry, ultimately leading to a fully integrated biochemical sensor array system, shown in Figure 1.1.

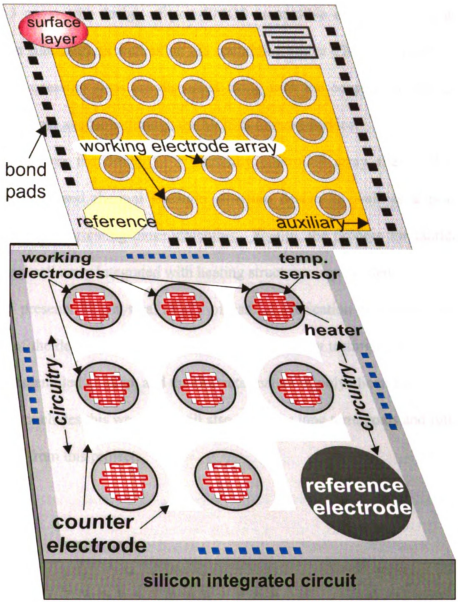


Figure 1-1: *Fully integrated biochemical sensor array system containing electrochemical array sites (top layer), temperature sensing and control (middle layer, shown at bottom) with readout circuitry contained in silicon integrated circuit*

1.2 Summary

Chapter 2 covers the background information on biochemical sensors, on-chip electrochemistry, post-CMOS MEMS processing techniques, and the development of on-chip thermal control utilizing post-CMOS thermally isolated structures.

Chapter 3 covers the design of post-CMOS compatible electrochemical arrays on passive silicon substrates as well as on die containing active CMOS circuitry. Specific masking and processing steps are discussed along with the constraints inherent in the AMI C5F/N process available through the MOSIS foundry service.

Chapter 4 covers the design of a thermally controlled array sites. The heating structures, sensors, and thermal isolation structure design as well as a post-CMOS process capable of fabricating those structures. Finally, the process for fabricating an electrochemical cell array integrated with heating structures is presented.

Chapter 5 presents the physical results of various fabrication processes, evidence of functionality of the designed electrochemical arrays, stability testing, C-V measurements with proteins assembled on-chip, and the characterization of polysilicon heaters/sensors.

Chapter 6 concludes this work and will also show the long term goals and future work to be generated from this project.

Chapter 2. Background

Bioelectrochemical Microsystems have the potential to revolutionize the study of proteins and have widespread ramifications in the medical field, specifically on point of care diagnosis. This potential has gone largely unrealized due to the interdisciplinary challenges involved in designing and creating biomaterials that interface to electrodes, while simultaneously fabricating those electrodes as array structures on active circuitry. Consequently, the array fabrication sequence, which is the primary focus of this work, must be compatible with post-processing of, in this case, CMOS chips as well as self-assembly of bio-interfaces. This process integration is further complicated by the attempt to thermally control the array sites. Following is a background discussion of each of the three major components being incorporated into the electrode array. Additionally, it should be stated that this work is directly built upon the thesis work of Nathan Dotson and that much of the background information for this work has been discussed in detail in his thesis [14].

2.1 Biochemical Sensors

Many types of sensors have been developed utilizing a biological recognition element that converts biochemical activities into signals measured, in turn, via a secondary transducer that is typically either electrical, optical, or mass-based. A plethora of biosensor technologies has been explored and reviewed in the literature, including cell-based biosensors [15-17], DNA hybridization arrays [18], and protein bioreceptors including enzymes [19] and antibodies [20, 21]. The most common secondary transducer mechanisms are optical [22], mass-based [23], and electrical [3, 24] (often referred to as

electrochemical). Each of these technologies has strengths, but most are not well suited for inexpensive miniaturization into high density arrays (on the order of ten thousand elements per millimeter) or are incapable of measuring extremely low analyte concentrations. For example, optical readout equipment is typically quite large, occupying several cubic meters of room space, and very expensive. Other techniques are limited because they can only detect the presence of specific analytes (antibodies, DNA), are not reusable, cannot measure concentrations, or require a specific electrolytic solution to catalyze reactions. Most of the existing protein-based sensors (including many mass-based approaches) rely on soluble proteins that can be easily immobilized. Although these devices can measure some biochemical analytes, they are immobilized in (relatively) thick films that limit sensitivity and signal gain and are not well suited to measure some of the most important cellular processes. Sensors based on biomimetic interfaces, discussed in further detail below, capitalize on the advantages of nanoscale interfaces (~5nm) and are uniquely capable of observing many essential physical, chemical and electrical functions in cell membranes. However, to date they remain a largely untapped resource. Furthermore, of the secondary transducer mechanisms that have been employed, electrical measurements have a clear advantage for miniaturization, mass production, and integration as microsystems [25, 26].

Based on this analysis, protein bioreceptors coupled via biomimetic interfaces to electrical transducers (electrodes) and electronic measurement techniques form the biosensor platform most compatible with the aims discussed here. There are several distinct advantages to this platform. It employs biodetection mechanisms that do not destroy or "use up" the bioreceptors, enabling enabling continuous monitoring of analyte

concentration over time. It employs semiconductor fabrication techniques that enable mass production of devices rapidly, cheaply, and with high reproducibility [1], and it does not require extensive post-processing, micromachining, or highly complex packaging that compromise the cost of some biosensor approaches. It is compatible with microelectronics, allowing a highly integrated system of biological recognition and instrumentation to be constructed. This feature minimizes signal noise and allows high density sensor arrays to be fabricated on a miniaturized chip substrate and further supports fast and simultaneous measurements. High density microelectrode arrays accommodated by this approach improve signal characteristics (increased current, signal-to-noise ratio, etc.) [27], allow multiple studies of individual or linked events in a single device, support replicating the same measurement to increase accuracy, enable measurement of micro-scale spatial concentration gradients, and offer the potential for miniaturization to single protein/cell devices. Furthermore, exploiting new biomimetic interface technologies described below, this sensor platform can uniquely access the sensory capabilities of membrane proteins, including gated-ion channels, as well as certain redox enzymes in a pseudo-natural, nanoscale environment. Thus, this class of biosensor is very flexible and can react with a wide range of chemicals, biomolecules, and even whole cells.

2.1.1 Biomimetic Interfaces

Cell membranes carry out many essential functions at the molecular scale, including regulation of ion transport, maintenance of transmembrane potential gradients and signal transduction [28]. Many of these functions can be reproduced *in vitro* by reconstituting the appropriate membrane proteins in lipid bilayers [28]. The resulting

biomimetic interfaces can be produced at very small size [4, 5] on microelectronics-compatible electrodes [6, 29] and have been shown to be highly functional biosensors [30] that can be composed of diverse set of membrane proteins [31]. Voltage-gated ion channels have been reconstituted in bilayers on microfabricated silicon substrates [32], and simultaneous optical and electrical recording of single gramicidin channels has been reported [33]. A typical biomimetic membrane system is shown in Figure 2.1(a). In this example, the expressed membrane activity is ion transport through the protein channel. A hydrophilic (aqueous) layer established by polymeric spacer molecules facilitates activity by stabilizing the lipid bilayer, elevating it above the electrode to prevent direct contact between the protein channel and electrode, and providing a reservoir for ions. The electrode provides the reporting mechanism.

2.1.2 Bioelectronic Interfaces

This technology can be extended to the immobilization of soluble proteins, particularly redox enzymes that have many useful sensor characteristics. Because the oxidation and reduction reactions catalyzed by dehydrogenase enzymes directly produce or consume electrons, dehydrogenase activity can be directly measured by current passing through an electrode. Prototype macro-biosensors based on dehydrogenase systems have been developed by the Dr. R. Mark Worden et. al [34] and elsewhere [35]. However, despite the commercial biosensor market exceeding $500 million/year, there are virtually no dehydrogenase-based commercial biosensors, due to technical challenges with *in-situ* regeneration of the enzyme's cofactor [36]. To address this issue, our colleagues have recently developed a novel molecular approach that uses cysteine as a trifunctional linker molecule (Figure 2.1(b)) [37]. In this work, dehydrogenase enzymes were bound to their

cofactors (e.g., NADP) by affinity interactions and the cofactors were bound to an electron mediator (toluidine blue O) and a gold electrode using the trifunctional linking molecule. This approach can potentially be extended to fabricate nanoscale interfaces for other soluble proteins and support the signaling needs of other membrane proteins.

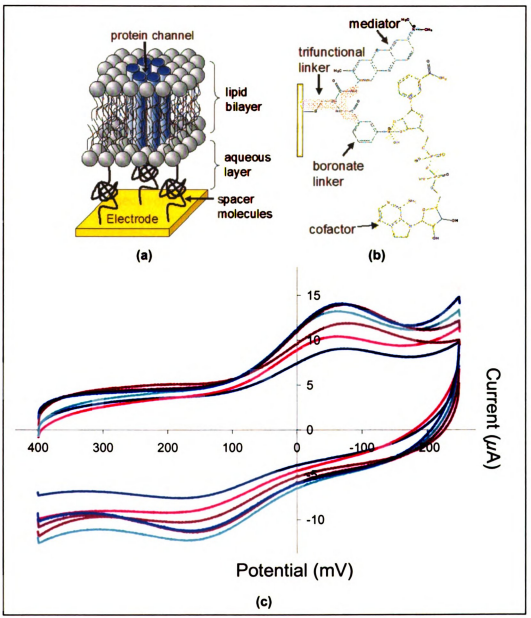


Figure 2-1: *(a) multilayered biomimetic interface with embedded protein channel, (b) a bioelectronic interface for dehydrogenase enzymes, (c) cyclic voltammetry response curves of a sorbitol dehydrogenase biosensor at various sorbitolol concentrations*

Prototype biosensors have been constructed (on CMOS-compatible gold electrodes) based on these two interfaces and characterized them using cyclic voltammetry. Selective ion transport through an ion channel was demonstrated by redox waves in the presence of monovalent cations but not anions [37]. Such experiments can be used to confirm that gated ion channels and associated transporters are embedded in the biomimetic interface in an active conformation [38]. Additionaliy, multiple cycles of dehydrogenase-catalyzed reaction and cofactor regeneration were demonstrated (Figure 2.1(c)). Biosensors constructed with both yeast alcohol dehydrogenase and a thermostable SADH gave linear calibration curves for ethanol (up to 50 mM) and isopropyl alcohol, respectively.

2.1.3 On-Chip Electrochemistry

Cyclic voltammetry (CV) is a sensitive electrical method to measure biomimetic interface activity. It provides insight into phenomena such as the integrity of the BLM. For example, we used CV to confirm assembly multilayered biomimetic interface shown in Figure 2.1(a). As sequential layers are added, the current due to ferricyanide oxidation and reduction drops. The extremely low current level following BLM deposition is consistent with literature observations that BLM have extremely high resistivity (greater than $10^8\ \Omega$ cm), thus allowing high signal-to-noise ratios in biosensors.

2.2 Post CMOS Processing

Post CMOS processing is any process conducted on a wafer or die after it leaves the original fabrication house. These processes, which usually fall into one of three categories: photolithography, film deposition, and etching, must be carefully planned and implemented so as to be non-destructive to the embedded CMOS circuitry. In order to

ensure that the circuitry is not damaged, the wafer/die must be well protected to prevent breakage or contamination and the processes must be compatible with the material already contained in and on the substrate. This means that any films deposited on the substrate should naturally adhere to an exposed substrate surface, such as oxide or metal, and be deposited at low temperatures so as not to melt the existing CMOS metals [14]. In this work, all three processes have been implemented on passive substrates as well as on fabricated CMOS die. An analysis of these steps follows [39].

2.2.1 Photolithography

Photolithography, or the transferring of shapes on a mask to the surface of a silicon wafer, is typically the most critical process in microelectronic fabrication. This process typically consists of seven steps: wafer cleaning, photoresist application, soft baking, mask alignment, exposure, development, and hard baking. Due to the precision required in generating masks for CMOS processes, with feature sizes down to about 65nm, and the careful alignment of subsequent masks, photolithography is also the most expensive fabrication process, with mask sets costing upwards of one million dollars per mask.

In the first step in the photolithographic process, wafer cleaning, wafers are chemically cleaned to remove any particulates that may be present on the surface of the wafer as well as any chemical residues, which may have been left behind from the wafer formation process, or native oxides that may have grown on the wafer surface. This ensures proper adhesion of the photoresist, a polymer with properties alterable by the exposure to ultraviolet light.

Next, photoresist, which is commonly referred to as PR, is applied to the wafer in liquid form using a spin coater. This spin coater utilizes a vacuum to secure the substrate and then spins the wafer at a few thousand RPMs after the PR has been deposited or as it is being deposited, depending on the type of spin coater. A photoresist layer of uniform thickness ranging from about half of a micron to ten microns thick is produced, depending on the speed and the amount of time that the coater is spinning. This process is also known as "spin coating" and can be used to deposit other liquid polymers, such as spin-on-glass, which will be discussed later in this paper.

Third, the wafer and photoresist coating are soft baked at around 150°C for around fifteen minutes. This removes almost all of the solvents from the PR and makes the photoresist become photosensitive, or imageable. Overbaking will degrade the photosensitivity of the PR, while underbaking will cause the development of all PR areas, regardless of exposure.

Following the soft bake, the mask, which is typically a glass substrate patterned with ink (for prototype purposes) or a very thin layer of metal, usually chromium or nickel, that completely blocks ultraviolet light, is aligned relative to the wafer to get the orientation correct. These masks, illustrated in Figure 2-1, are typically classified as clear field or dark field, which means that the ultraviolet light either passes through the field surrounding the pattern or through the pattern itself, respectively. The alignment is done using alignment marks, also shown in Figure 2-1, and a mask aligner, which is the tool used to transfer the image on the mask to the photoresist on the substrate. While there are several types of mask aligners, such as dual sided, cassette, and large area proximity aligners, the type used in this work is a Karl Suss MJB3 submicron single-sided contact

mask aligner. This is the most basic and inexpensive form of aligner, where the mask, held image side down in a frame, is aligned to the wafer using the microscope incorporated into the system and adjustment knobs that alter the substrate position relative to the mask. Once the alignment marks match up, the mask is pressed against the resist-covered substrate, making "hard contact", which means that the distance between the mask and wafer are ideally zero, which minimizes undesirable diffractive effects and ideally enables a perfect transfer of the mask image to the wafer.

Figure 2-2: *Dark field mask (left) and alignment marks (top left). Clear field mask (right) and alignment marks (top right).*

However, due to the facts that the distance between the mask and photoresist layers is never actually zero and the photoresist itself has a thickness, minimal diffractive errors do occur. Another major disadvantage of contact photolithography is the transfer of defects from mask to substrate and substrate to mask during each alignment. These defects include dust particles trapped between the mask and substrate and the transfer of errant ink dots, etcetera, from the mask to the photoresist and then, in turn, the substrate after etching.

Once the mask is aligned to the wafer, hard contact is made, the microscope is retracted, and the mask/PR/wafer is exposed to the high intensity ultraviolet light source.

The amount of time the system is exposed to the light is critical, as overexposure will result in removal of extra photoresist during development and underexposure will result in an incomplete image transfer, both of which are highly undesirable. This is one reason that process characterization was an important feature of this research.

Following exposure, the photoresist is placed in a developer, which removes certain areas of the resist, depending on the type. If a negative resist is used, the areas of PR not exposed to the UV light are removed. Unfortunately, negative photoresist requires a different type of developer and slightly more complex patterning process. For this reason, this research utilizes positive photoresist, which is etched away if exposed to UV light, leaving the opaque portions of the mask on the substrate. Following the development, the substrate is hard baked at an elevated temperature to harden the PR, making it a suitable masking layer for certain etchants.

2.2.2 Film Deposition

Film deposition is the process by which layers of material, typically metal and dielectric, are deposited onto the surface of a substrate, typically a silicon wafer in the case of CMOS and post-CMOS fabrication. The three major types of deposition are chemical vapor deposition (CVD), physical vapor deposition (PVD), and to a lesser extent, spin coating.

Chemical vapor deposition is a chemical process used to deposit thin films, typically insulators and semiconductors, onto a substrate from a gas phase. This process typically heats the substrate above 300°C, much higher than both PVD and spin coating, allowing it to react with gaseous precursors in the chamber to produce the desired film. There are several variations of CVD techniques: low pressure CVD, plasma-enhanced

CVD, metal-organic CVD, rapid thermal CVD, among others. Due to the fact that most of these techniques raise the substrate temperature above 300°C (which can easily damage semiconductor circuitry) as well as contamination issues involved, this process was undesirable for this research and will not be discussed in further detail.

Physical vapor deposition also deposits thin films, in this case typically metals as well as some insulators and semiconductors, onto the surface of a substrate, in this case silicon and silicon dioxide. In this process, the substrate as well as the material to be deposited, or target, is placed in a vacuum pumped chamber and the target is then transformed into a gas phase through various methods, typically thermal evaporation, sputtering, or electron-beam deposition, of which the latter two techniques are available in the semiconductor fabrication laboratory at Michigan State. Once in gas form, the molecules cool and adhere to the substrate surface.

The most basic technique for transforming the source material into the gas phase is thermal evaporation. In this process, the crucible containing the target is heated, typically by utilizing resistive and inductive heating techniques, so that the target melts and then evaporates. Unfortunately, this technique is limited to the deposition of high vapor pressure metals, such as Au and Al, due to process heating limitations. Additionally, there is a contamination risk associated with the heating of the crucible itself.

The first of the two PVD process available at MSU, and the one exclusively utilized in this research, is electron-beam evaporation. A high-energy electron beam is used to melt the target in e-beam evaporation. Source material temperatures significantly higher than standard evaporation techniques can be achieved using this method enabling

a wider range of materials to be deposited, such as insulators and low vapor pressure metals. An added benefit to e-beam evaporation is that, because the crucible containing the target is not directly heated as much as with thermal evaporation, the possibility of contamination is lowered.

The second PVD method available is sputtering, which entails bombarding the source material with an ion beam, knocking off target atoms to land on the substrate. Generation of the ion beam impinging on the source is achieved through an arc discharge in a pressure range of 1-100μTorr, at 500-1000V, which is then focused into a narrow column and accelerated [14]. Sputtering is the most optimal PVD method due to the superior deposition control, wide range of compatible source materials, and the ability to simultaneously deposit and etch materials by using multiple ion beam.

The most important factor in choosing PVD over CVD in this research is the fact that while the temperature of the target is raised significantly in PVD, the substrate is not. Conversely, CVD raises the substrate temperature substantially, which may damage CMOS circuitry by melting the aluminum used in most processes during post-fabrication processing.

The third method of thin film deposition is spin coating, which is typically limited to various types of polymers such as photoresist and spin-on glass (SOG). This process entails placing the substrate in a spin coater, coating the substrate with a liquid source material, and then spinning the substrate at a set speed and time in order to create a uniform layer thickness across the surface. There are two deposition methods available. The first is simply pipetting the liquid onto the surface before spinning while the second

entails automated spraying while spinning. Unfortunately, there are very few useful materials that can be deposited in this manner.

2.2.3 Etching Techniques

Etching in regards to MEMS is the process of removing selected surface materials by bringing the surface of the substrate into contact with a liquid or gas etchant that selectively attacks a target material. There are several different types of etching to consider when developing an etch process: isotropic, anisotropic, wet, and dry. Important factors when choosing the type of etch and etchant are etch rate and selectivity. Etch rate is the material thickness removed over time, typically listed in terms of angstroms per minute. Higher etch rates have the advantage of speed, but may unfortunately make the process difficult to control and reproduce. Low etch rates take more time, but processes involving them are much more easily controlled and reproducible. An etchant's selectivity is the ratio of etch rates for various materials. For example, if an etchant had a 40:1 selectivity of Si to SiO_2, that would mean it etches silicon 40 times faster than silicon dioxide. The selectivity is critical when designing an overall etch process to ensure that masking materials are available and that other surface materials are not inadvertently etched away. Often, an etchant will very slowly attack a mask, which may slightly alter final results for long etches, which is shown in figure 2.3.

The two major classifications of etchants, isotropic and anisotropic, must be carefully considered in order to determine the structures formed by a process as well as the individual process steps. The former etches target materials at the same rate in all directions and is commonly used in wafer thinning and thin film etches. When used with thick films or bulk silicon, these etchants always undercut the masking material. The

latter etches the target material much more quickly in one direction in regards to a material's crystal structure than others, lending anisotropic etches the ability to calculate and produce exact pattern dimensions in the etched material. These types of etchants typically have etch rates and selectivities associated with each crystal plane in the material. One thing to keep in mind is that, due to the plane selectivity, these etchants may undercut the mask. Anisotropic etching is commonly used when producing bulk silicon structures, typically etching the (100) and (110) directions much, much faster than the (111) [40-46]. When developing an etch process, it is important to consider what types of shapes and structures you are trying to produce and select the appropriate type of etchant at each process step in order to successfully produce the intended structures.

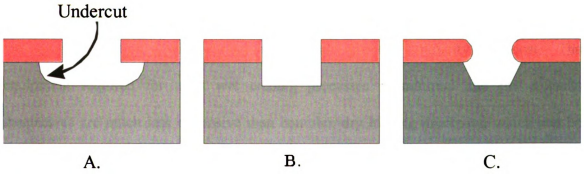


Figure 2-3: *A. Isotropic etch, note that the etch rate is the same for all directions. B. Anisotropic etch, note, the etch is direction dependant which adds some control to the etching process. C. Mask erosion and undercut which can result from very long etches [14].*

A second way to classify etch processes is wet etching versus dry etching. Wet etching is a chemical process in which the material to be etched away is not typically directly soluble in the etchant solution. Rather, the reactive species is usually present in the etching solution, which causes most wet etching processes to take place in three steps: etchant species movement to the surface of the substrate, chemical reaction with exposed

material producing soluble byproducts (usually a liquid or gas), and finally, byproduct movement away from the substrate surface. In order to control the etch rate, the solution is typically agitated, which aids in delivery of the etchant species to the substrate surface and byproduct removal. Additionally, agitation aids in the reduction of gas bubbles that may form as reaction byproducts as well as preventing these bubbles from adhering to the substrate surface, preventing the delivery of fresh etchant to that portion of the pattern [47]. Another issue commonly effecting wet etching is resist scumming, which occurs when patterned photoresist is incompletely developed. The small amount of photoresist left behind can substantially slow the etch process. A more extensive treatment on wet etching is available [48].

While wet etching can have serious drawbacks such as poor process control and excessive contamination, there are several advantages such as potentially high selectivity, the ability to pattern a wide variety of materials, process simplicity, and cost. The equipment required for most wet etching processes is minimal and the etchants themselves are much less expensive than complex dry etching processes, which can be cost prohibitive. For these reasons, wet etching is still used in a variety of IC processes and exclusively in this research. A selection of wet etchants used in this research, the materials they etch, and the masking material is found in Table 1, with a more complete treatment in Appendix B [49, 50].

Table 1: *Wet etchants and basic properties*

Material	Wet Etchant	Masking Material	Etch Rate (A/min) unless noted
Ag	KI	Photoresist	1.8-6 μm
Al	Aluminum Etchant Type A: Phosphoric + Acetic + Nitric Acid + Water 16:1:1:2 @50^0C	Photoresist	6600
Au	Potassium Iodine (KI)	Photoresist	.5-1 μm
Cr	Hydrochloric Acid (HCl)	Photoresist	1500
Si (Anisotropic)	TMAH: 0.5% $(NH_4)_2S_2O_8$ (Ammonium Persulfate): 1% Si	Silicon Dioxide or Silicon Nitride	10k (100) 40-100 100/111 etch ratio
SiO_2	Buffered Hydrofluoric Acid (BHF) 5:1 ammonium fluoride NH_4F : hydrofluoric acid HF	Photoresist	1000

The alternative to wet etching is dry etching. There are several different dry etching techniques commonly utilized in microfabrication, such as plasma etching, reactive ion etching, and ion milling. Dry etching processes have several advantages over wet process, such as the fact that they are typically more easily repeated than wet etching processes due to their substrate temperature immunity and the ease with which the processes can be initiated and ended. Additionally, most dry etching techniques, like RIE, are highly anisotropic enabling the fabrication of precise structures. Finally, there is typically less chemical waste in these procedures and there is much less chance of substrate contamination in plasma environments. Unfortunately, these systems are incredibly complex and very expensive, which can render them inaccessible.

2.3 On-Chip Thermal Control

The On-Chip Thermal Control of this chip is based on two of the three fundamental laws of heat transfer: conduction, and convection [51]. In addition, there are several material properties central to the design of the heater and sensor structures.

2.3.1 Conduction

A temperature gradient within a homogeneous substance results in an energy transfer rate within a medium that can be calculated by *Fourier's Law*

$$q = -kA\frac{\partial T}{\partial n} \qquad \textbf{Eq. 2-1 [14]}$$

here $\frac{\partial T}{\partial n}$ is the temperature gradient in the direction normal to the area A. The thermal conductivity k is an experimental constant for the medium involved, and this constant may depend on other properties, such as temperature and pressure which will be discussed in further detail later. The units for k are $W/m^{\circ}K$.

The minus sign in *Fourier's Law* is required by the second law of thermodynamics, which states: thermal energy results from a thermal gradient which must be from a warmer to a colder region.

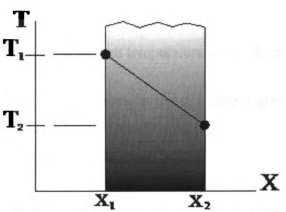


Figure 2-4: *Graphical representation of Fourier's Law [14]*

If the temperature profile within the medium is linear as shown in Figure 2-6 above, it is allowable to replace the temperature gradient with

$$\frac{\Delta T}{\Delta x} = \frac{T_2 - T_1}{x_2 - x_1} \qquad \textbf{Eq. 2-2 [14]}$$

This type of linearity is always seen in a homogeneous medium of fixed *k* during steady state heat transfer.

Steady state heat transfer occurs whenever the temperature at every point within the body, including the surfaces, is independent of time. If the temperature changes with time, energy is either being stored in or removed from the body. The storage rate is

$$q_{stored} = mc_p \frac{\partial T}{\partial t} \qquad \textbf{Eq. 2-3 [14]}$$

where the mass *m* is the product of volume V and density ρ [14, 51].

2.3.2 Convection

Whenever a solid body is exposed to a moving fluid having a temperature gradient from that of the body, energy is carried or convected from or to the body by the fluid.

If the temperature of the upstream temperature of the fluid is T_∞ and the surface temperature of the solid is T_s, the heat transfer per unit time is given by

$$q = hA(T_s - T_\infty) \qquad \textbf{Eq. 2-4 [14]}$$

which is known as Newton's law of cooling. This equation defines the convective heat transfer coefficient h as the constant proportionality relating the heat transfer per unit time and unit area to the overall temperature difference. The units of h are $W/m^2 \cdot {}^oK^1$.

. The fundamental energy exchange at a solid-fluid boundary is by conduction, and this energy is then convected away by the fluid flow. From earlier equations we obtain

$$hA(T_s - T_\infty) = -kA\left(\frac{\partial T}{\partial y}\right)_S \qquad \textbf{Eq. 2-5 [14]}$$

where the subscript on the temperature gradient indicates evaluation in the fluid at the surface [51]. Convection can be via two modes forced convection and natural convection [14]. Natural convection will be the mode of convective heat transfer in this work and the analysis will be discussed further in later sections.

2.3.3 Material Properties Affecting Heat Transfer

Thermal Conductivity of Solids

Thermal conductivities of numerous pure metals and alloys are well known and widely available. The thermal conductivity of the solid phase of a metal of known composition is primarily dependent only upon temperature. In general, k for a pure metal decreases with temperature; alloying elements tends to reverse this trend.

The thermal conductivity of a metal can usually be represented over a wide range of temperature by

$$k = k_0(1 + b\theta + c\theta^2) \qquad \textbf{Eq. 2-6 [14]}$$

where $\theta = T - T_{ref}$ and k_0 is the conductivity at the reference temperature T_{ref}. For many engineering applications the range of temperature is relatively small and $k = k_0(1 + b\theta)$.

The thermal conductivity of a nonhomogeneous material is usually very dependent upon the apparent bulk density, which is the mass of the substance divided by the total volume occupied. This total volume includes the void volume, such as air pockets within the overall boundaries of the piece of the material. The conductivity also varies with temperature. As a general rule, *k* for a nonhomogeneous material increases both with increasing temperature and increasing apparent bulk density [14].

Thermal Conductivity of Liquids

For most liquids, *k* is usually temperature dependent on temperature but insensitive to pressure. Thermal conductivities of most liquids decrease with increasing temperature. The exception to this is water, which exhibits increasing *k* up to 150 °C and decreasing *k* after this point. Water has the highest thermal conductivity of all common liquids except the liquid metals.

Thermal Conductivity of Gases

The thermal conductivity of a gas increases with increasing temperature, but is essentially independent of pressure for those close to atmospheric. At high pressures, the effect can be very significant.

Density

Density can be defined as the mass per unit volume. Density data for most solids and liquids are only slightly temperature dependent and are negligibly influenced by pressure up to 100 atm. The density of a gas, however, is strongly dependent upon the

pressure as well as upon the temperature. In the absence of specific gas data, the density can be represented by

$$\rho = \rho_1 \left(\frac{p}{p_1} \right) \qquad \textbf{Eq. 2-7 [14]}$$

The specific volume is the reciprocal of the density,

$$v = \frac{1}{\rho} \qquad \textbf{Eq. 2-8 [14]}$$

and the specific gravity is the ratio of the density to that of pure water at a temperature of 4°C and a pressure of one atmosphere. Thus

$$S = \frac{\rho}{\rho_w} \qquad \textbf{Eq. 2-9 [14]}$$

where S is the specific gravity.

Specific Heat

The *specific heat* of a substance is a measure of the variation of its stored energy with temperature. From thermodynamics the two specific heats are:

$$\text{specific heat at constant volume: } c_v \equiv \left. \frac{\partial u}{\partial T} \right|_v$$

$$\text{specific heat at constant pressure: } c_p \equiv \left. \frac{\partial h}{\partial T} \right|_p$$

Here u is the energy per unit mass and h is the enthalpy per unit mass. In general, u and h are functions of two variables: temperature and specific volume, and temperature and pressure, respectively. For substances which are incompressible, solids and liquids,

c_p and c_v are numerically equal. For gases, however, the two specific heats are considerably different. The units of c_p and c_v are $J/kg \bullet {}^oK$..

For solids, specific heat data are only weakly dependent upon temperature and are even less affected by pressure. It is usually acceptable to use to use the limited specific heat values at constant pressure, over a fairly wide range of temperatures and pressures. Specific heats of liquids are even less pressure dependent than those of solids, but they are somewhat temperature influenced.

Gas specific heat data exhibit a strong temperature dependence. The pressure effect is slight except near the critical state, and the pressure dependence diminishes with increasing temperature. For most engineering calculations specific heats for gases found in common tables are suitable for pressures up to 1.4×10^6 Pa.

Thermal Diffusivity

A useful combination of terms already considered is the *thermal diffusivity* α, defined by

$$\alpha \equiv \frac{k}{\rho c_p} \qquad \textbf{Eq. 2-10 [14]}$$

It is seen that α is the ratio of the thermal conductivity to the thermal capacity of the material. Its units are m^2/s. Thermal energy diffuses rapidly through substances with high α and slowly through those with a low α [51].

Thermal Resistance

It is useful at this point to introduce the notation of thermal resistance of a material, R_T, defined the temperature drop across the material per unit heat current, or

$$R_T = \frac{\Delta T}{I_Q} = \frac{X}{kW^2} = \frac{1}{hW^2}$$ **Eq. 2-11 [14]**

where X is the thickness of the material. This expression combined with ideas laid out in the section dealing with heat transfer through a plane wall above, made for this structure, suggest that a series of adjacent thermal resistances will add linearly so that the total equivalent thermal resistance is just the sum of individual thermal resistances for this structure.

$$R_T = \sum_i \frac{X_i}{k_i W^2}$$ **Eq. 2-12 [14]**

Heat Capacity of a Polysilicon Resistor

The heat capacity of a material can be expressed as

$$C_T = \rho_m t W L \overline{C}_m$$ **Eq. 2-13 [14]**

where ρ_m is the mass density of the material (2330 kg/m^3 for polysilicon), t, W, and L are the thickness, width, and length, respectively, of the material, and $\overline{C}_m$ is the specific heat per unit mass (753 J/(kg-Kelvin) for polysilicon). Heat capacity is sometimes given as a per volume constant, such that

$$C_T / V = \rho_m \overline{C}_m$$ **Eq. 2-14 [14]**

Temperature Coefficient of Resistance

Resistance of a material is a function of temperature (unless specifically designed otherwise). The temperature coefficient of resistance (TCR), αR, is itself generally a

function of temperature, but can often be assumed constant over a small temperature range. The TCR is defined as

$$\alpha_p = \frac{R_T - R_{T_0}}{R_{T_0}(T - T_0)} \qquad \text{Eq. 2-15 [14]}$$

where, R_T is the resistance at temperature T and R_{To} is the resistance at temperature T_o. The resistance of the polysilicon is also a function of stress in the material. However the change in resistance due to stress is negligible compared to the change due to temperature and can be neglected for basic analysis.

Extraction of αR is very important for the characterization and performance of the polysilicon resistor that will be acting as a temperature sensor. This parameter must be found through experimental analysis of the resistor in a highly controlled temperature environment over a wide temperature range to ensure accuracy in temperature readings.

2.4 One-Dimensional Steady-State Conduction

The conductive heat transfer rate at a point within a medium is related to a local temperature gradient by Fourier's Law **Eq. 2-1**. In many one-dimensional problems we can write the temperature gradient simply by inspection of the physical situation. The situation we are dealing with can be modeled from this basic heat transfer situation by taking the physical geometry of the situation into consideration.

2.4.1 Plane Wall Fixed Surface Temperatures

The simplest heat transfer problem is that of one-dimensional, steady-state conduction in a plane wall of homogeneous material having constant thermal conductivity and with each face held at a constant uniform temperature as shown below.

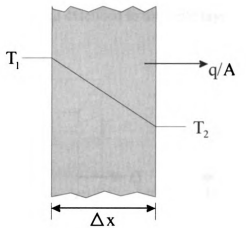


Figure 2-5: *Heat transfer by conduction in a plane wall [14]*

Separation of variables and integration of Eq. 1 where the gradient direction is x results in

$$q\int_{x_1}^{x_2} dx = -kA\int_{T_1}^{T_2} dT \qquad \textbf{Eq. 2-16 [14]}$$

or

$$q = -kA\frac{T_2 - T_1}{x_2 - x_1} = -kA\frac{T_2 - T_1}{\Delta x}$$

This equation can be rearranged as

$$q = \frac{T_1 - T_2}{\Delta x / kA} = \frac{\text{thermal potential difference}}{\text{thermal resistance}} \qquad \textbf{Eq. 2-17 [14]}$$

Notice that the resistance to the heat flow is directly proportional to the material thickness, inversely proportional to the material thermal conductivity, and inversely proportional to the area normal to the direction of heat transfer.

These principles are readily extended to the case of a composite plane and can be directly applied to the various layers in the CMOS design flow. The case for the

composite plane which will later be extended to multiple layers is shown in Figure 2-6 (a) below:

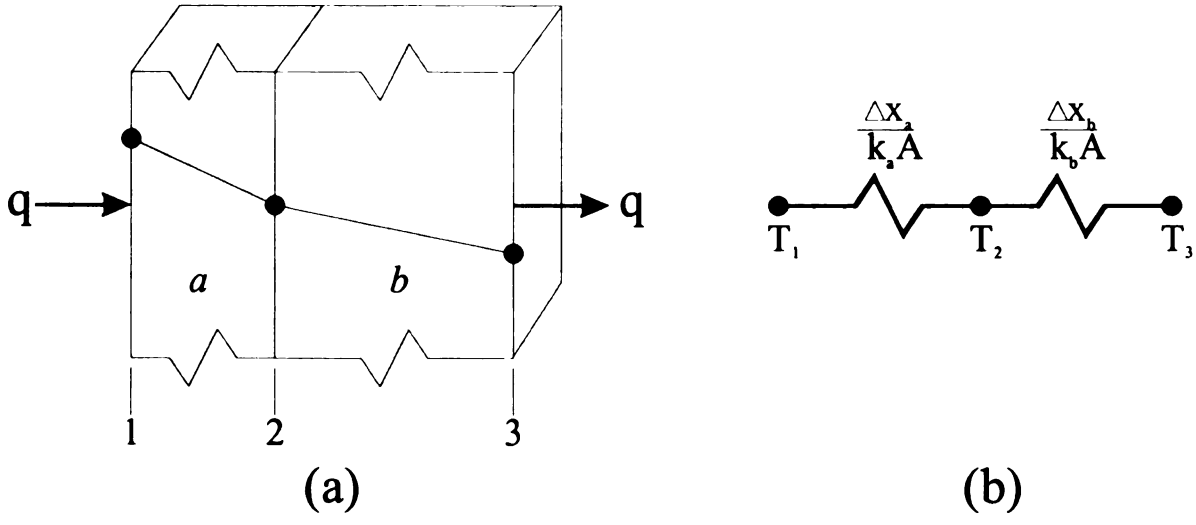


Figure 2-6: *(a) Heat transfer through a composite wall. (b) Equivalent thermal resistance of composite wall [14]*

In the steady-state the heat transfer rate entering the left face is the same as that leaving the right face. Thus,

$$q = \frac{T_1 - T_2}{\Delta x_a / k_a A} \quad \text{and} \quad q = \frac{T_2 - T_3}{\Delta x_b / k_b A}$$

Together these give:

$$q = \frac{T_1 - T_3}{(\Delta x_a / k_a A) + (\Delta x_b / k_b A)} \qquad \textbf{Eq. 2-18 [14]}$$

Equations 12 and 13 illustrate the analogy between conductive heat transfer and electrical current flow, an analogy that is rooted in the similarity between Fourier's and Ohm's laws. It is convenient to express Fourier's law as

$$\text{conductive heat flow} = \frac{\text{overall temperature difference}}{\text{summation of thermal resistances}} \qquad \textbf{Eq. 2-19 [14]}$$

In the case of Figure 2-8 (a) above the total thermal resistance is simply the sum of the two resistances in series as shown in Figure 2-8 (b) above. The extension to three or more layers is obvious.

2.5 One Dimensional Systems: Transient Analysis Fixed Surface Temperature

Another key component in analyzing various structures for thermal isolation is the transient characteristics of heat transfer. For some proposed structures there is no thermal boundary layer of high resistance providing thermal isolation between array sites. In these cases there is silicon substrate, an oxide layer, or a combination of the two separating the biosensor array sites. In these cases, the temperature at a distance x away from our heater layer into the silicon substrate, oxide, or other material can be approximated by this particular analysis. In this manner we will see if sufficient thermal isolation coinciding with proper operation of an array site is feasible.

In considering this transient conduction problem, it can be treated approximately by considering the body to be initially at some uniform temperature and suddenly having the temperature of part of the surface changed to and held at a known constant value different from the initial temperature.

The solution to this conductive problem is approximated by using the transient analysis for a semi-infinite body. The solution to a temperature at some distance x below the surface is

$$\frac{T(x,t)-T_s}{T_i-T_s} = erf\left(\frac{x}{\sqrt{4\alpha t}}\right) \qquad \textbf{Eq. 2-20 [14]}$$

Values for the Gaussian error function can be obtained from various mathematical tables.

From such analysis MEMS structures can be designed and their behavior modeled down into the body of the MEMS chip [14].

Chapter 3. Post-CMOS Electrochemical Arrays

The design of Post-CMOS compatible biosensor arrays is a key component in this thesis. Due to the largely unstudied nature of the protein structures involved in the research, the design constraints of the sensor system were initially centered around the MOSIS, a low-cost, low-volume VLSI circuit fabrication service geared toward prototyping for research and educational institutions [52], service's AMI C5N process itself. The AMI C5N process is AMI Semiconductor's C5F/N 0.5 micron process, which is a non-silicided CMOS process supporting stacked contacts with 3 metal layers and 2 polysilicon layers, one of which is a high resistance layer, intended for supply voltages of three to five volts. One of the most challenging aspects of this process to deal with in regards to post processing is that it is a planarized process, but this plays more of a factor in the design of the thermal aspects, discussed later. Any process steps used to generate the electrode arrays must be compatible with the process in that all steps must be relatively low temperature so as not to melt any of the existing CMOS metals, any materials deposited on the chip surface must adhere to it, and any process steps must be implemented on a single die. These are not trivial obstacles, especially considering the AMI C5N process layers are proprietary information that is not easily obtained. Constructed from the limited information available [52, 53], Figure 3.1 illustrates the AMI C5N process layers as we believe them to be. All of the metal layers are TiN/AlCu/TiN, where the AlCu alloy is approximately 0.4% copper. The intermetal dielectrics are unknown, but assumed to be Silicon Dioxide (SO_2).

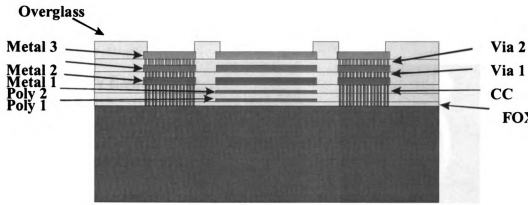


Figure 3-1: *AMI C5N Process Layers*

Building upon AMSaC's (Dr. Mason's research group, Advanced Microsystems and Circuits) success in the fabrication and design of a single three-electrode electrochemical cell [9], various 2x2 electrode arrays on a passive silicon substrate were initially designed utilizing post-CMOS compatible steps in order to allow for experimentation in multiple protein deposition. Following that, a 3x3 electrode array and the corresponding post-CMOS processes were designed and fabricated, allowing readout by an on-chip integrated potentiostat [54].

3.1 Electrode Arrays on Passive Silicon Substrates

The first step in creating on-chip electrode arrays was to create a 2x2 array of electrodes on a passive silicon substrate to perfect the process steps needed to be undertaken on the single active die as well as to allow our multidisciplinary team the opportunity to deposit multiple proteins on a single chip, which to our knowledge had never been done. In order to do this, we started with the knowledge gained in fabricating the single electrochemical cell, shown in figure 3.2.

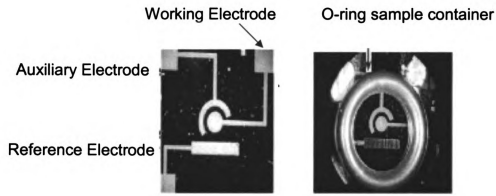


Figure 3-2: *(Left) Single electrochemical cell (Right) Electrochemical cell with O-ring reservoir*

Originally, the passive substrate used was a <100> P-type silicon wafer doped with Boron (the same type of wafer and dopant as AMI C5N) from Silicon Valley Microelectronics [55]. Next, 20nm of titanium was to be deposited via E-beam evaporation (which, as previously discussed, was chosen for its consistency and low substrate temperature) to act as an adhesion layer between the silicon and the 100nm of gold that was then deposited. Titanium is also a suitable adhesion layer between titanium nitride and gold, which is the surface of metal 3 in the C5N process. Finally, 100nm of silver was evaporated on to the wafer.

Additionally, when designing for the 2x2 array, we needed to somehow isolate the traces routing the working electrodes to pads on the edge of the chip from each other, similar to the way the metal layers run underneath the overglass in standard IC processes. In order to mimic the C5N process, a method to deposit a dielectric over the surface of the wafer surface was needed. Unfortunately, dielectrics are typically deposited using CVD processes, which we had no access to and which typically elevate substrate temperatures near or past the melting point of gold. As an alternative, we chose a spin on

dielectric, or more appropriately, a spin-on-glass (SOG), specifically Accuglass, which is manufactured by Honeywell [56].

Finally, a mask set was designed, laying out four circular working electrodes, a small u-shaped auxiliary electrode, and a large u-shaped reference electrode as the outer border, with the auxiliary and reference electrode being equidistant from all four working electrodes. The masks were then generated using a high resolution positive film print from Advanced Imaging Services [57]. These types of masks are good for feature sizes down to 15μm, which was more than adequate for this first prototype. Using this mask set, the wafer was then patterned and etched with the mask set shown in figure 3.3(a), producing the structure illustrated in Figure 3.3(b). A table of etchants used for each material is presented in Appendix B. Initially, this structure allowed for the self-assembly of proteins in their own o-ring reservoirs, Figure 3.3(c). Once the proteins were assembled, the chip was intended for immersion in the test solution, shown in Figure 3.3(d). This structure was also eventually used for a new microfluidic method of protein deposition.

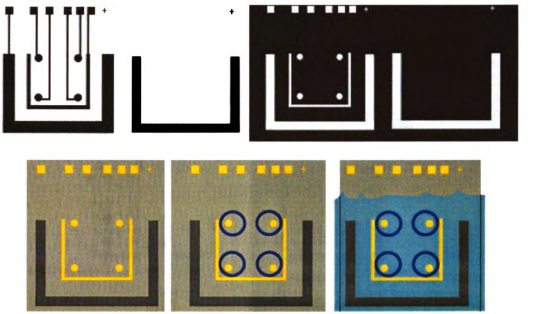


Figure 3-3: *2x2working electrode electrochemical cell array mask set (top), 2x2 electrochemical array structure with separate O-ring assembly sites enabling array immersion in solution (bottom)*

As another consequence of working with previously unstudied structures, the step coverage of the proteins was not known, nor was the impact of working electrode size on overall current flow. To investigate these issues, additional mask sets, shown in Figure 3.4, were generated with different size working electrodes, SOG openings, and a final, smaller, easily scalable 2x2 array microstructure.

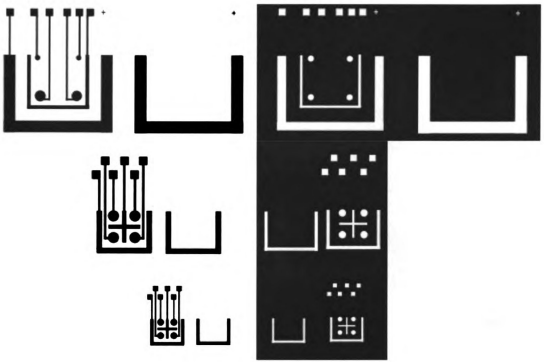


Figure 3-4: *(Top) Mask set with smaller and larger working electrodes (Bottom) Final scalable array mask*

3.2 On-chip Electrochemical Arrays

The design for the on-chip electrochemical arrays is essentially dictated by the original chip design, shown in Figure 3.5. While the metal films deposited post-CMOS and the etchants used to remove them are the same as the process developed for the passive substrate, there are a couple extra issues involved in successfully fabricating three electrode systems on 3.4mm x 3.4mm CMOS chips. The first issue is the size and manipulation of the die itself, while the second deals with overglass openings and step coverages.

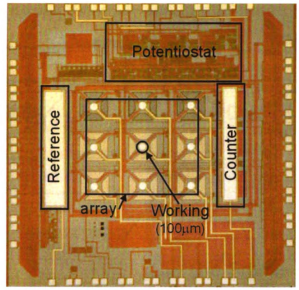


Figure 3-5: *CMOS electrochemical readout and thermal interface chip highlighting basic electrochemical components [54]*

First, the tiny size of the die itself presents manipulation problems, as it is easily dropped when the edges are held by tweezers and any grasping on the top and bottom of the die presents opportunities to scratch the surface or crack the die. An easily implemented solution to this problem was to superglue the die to a glass microscope slide. Additionally, when the photoresist was deposited using the spin coater using the settings of 3000RPM for 30 seconds, the resist built up on the edges and in the corners of the die due to the surface tension and viscosity of the resist in conjunction with the height of the die (shown in Figure 3.6(a)), which was highly undesirable. In order to nullify this phenomenon, a rectangle was stamped out of brass sheet metal in order to form a chip frame, which was attached to the glass microscope slide, allowing for a planar surface surrounding the chip, shown in Figure 3.6(b). Additionally, the spin coater was reset to 4500 RPMs for 40 seconds in order to optimize the photoresist layer uniformity [58].

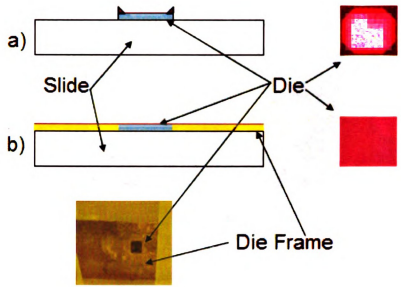


Figure 3-6: *(a) Photoresist buildup at corners of die without frame (b) Photoresist uniformity with addition of frame*

In the passive substrate electrochemical arrays, the SOG was used to simulate the overglass that the metal 3 lines ran underneath, isolating the lines from the conductive solution. Obviously the SOG is not needed for this purpose on the CMOS chip, as it has its own overglass. However, due to the unknown step coverage of the different proteins deposited on the gold electrodes, the SOG can be used in a way to ensure that the proteins need only attach to a planar surface. Measurements taken with a surface profilometer indicate that the overglass openings down to the electrodes are approximately 2μm deep. Assuming, worst case, that the titanium and gold coat the sides of the pit, we need to ensure that a) the protein need only cover the floor of the pit and b) the entire metal 3 surface at the floor of the pit is covered by TiAu. This can be achieved using appropriate masking steps, specifically, by making the TiAu working electrode larger than the metal 3 electrode/opening, depositing SOG, and then etching a hole in the SOG slightly smaller

than the metal 3 electrode/opening. The undesirable possibilities are illustrated in Figure 3.7(a), while the ideal structures are shown in Figure 3.7(b).

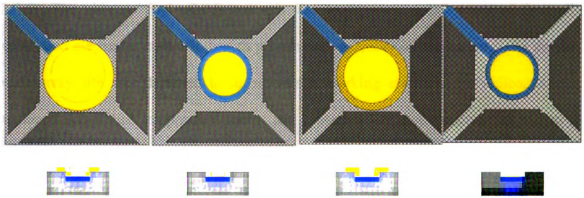


Figure 3-7: *Undesireable overflow of Gold on Al and incomplete electrode coverage (left) and ideal structures (right)*

The mask set designed to achieve these results as well as align to the MOSIS chip was generated by *MicroGraphics Plus, Inc.* [59] using microfiche technology [60, 61]. Using a 25X reduction ratio when generating the film, feature sizes down to 1μm can be achieved. The final mask set is illustrated in Figure 3.8. Once the electrodes were fabricated on-chip, a copper board was etched using the mask in figure 3.8b and the chips were wiredbonded to the board and the traces wirebonds were covered in epoxy, leaving the electrodes exposed to enable testing in an aqueous environment.

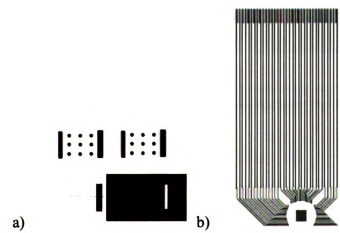


Figure 3-8: *a) On-Chip Electrochemical mask set b) Copper test board mask*

Chapter 4: Thermally Controlled Electrodes

The ultimate goal of this research was to fabricate a 3x3 array of thermally controlled electrodes compatible with protein self-assembly on the surface. To do this, each array site was designed to incorporate a working electrode, polysilicon heater, undoped polysilicon temperature sensor and a thermal isolation structure, as shown in Figure 4.1. Four different resistor values were used for the heaters, while the sensor value and layout remained constant. Each site's heater and sensor elements are selectable by external address pins in order to individually control and readout individual sites. The select ability also allows for infrequent heating for short periods of time, which reduces any degrading effects on the protein or readout circuitry that heating may have.

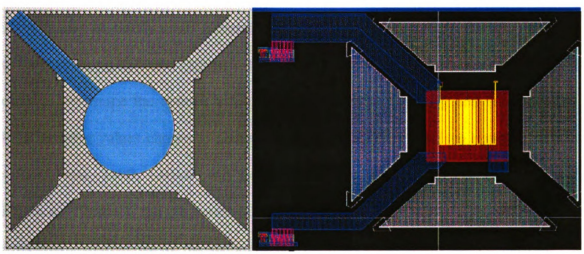


Figure 4-1: *Sensor array site showing the metal 3 electrode opening (left blue), the temperature sensor (right, yellow), heater (right, red), and openings for thermal isolation structures (left in grey, right in blue gray)*

4.1 Heater Array

One of the most critical aspects of this research is the ability to incorporate heating into each array site. This heating will enable longer lifetimes for protein sensor elements, a more robust sensor, and can be utilized to maximize sensor activity. The heaters are serpentine polysilicon resistors that will experience joule heating due to the power dissipated through the resistor. This is a common technique used for heating in MEMS and circuit designs [62-66]. The power dissipated by each heating element is basically limited by the maximum allowed Vdd for the AMI process. This voltage was originally thought to be 5 volts with the capability to use 10 volts with wide supply lines. Larger voltages may cause the metal lines to degrade over time, which was the cause of some concern until AMI updated its process documentation to reflect that voltages up to 20 volts may be safetly used. Several heaters have been designed for the array sites, all of them covering the same chip area, 100μm x 100μm, yet differing in resistive values in order to determine the optimal value to achieve sufficient heating and controllability. Four resistive values chosen to coincide with those used in previous research. These values: 195Ω, 300Ω, 1.05kΩ, and 2.6kΩ, have been implemented into the 3x3 array. Figure 4.2 illustrates the placement of the various heaters and Table 2 shows the results from circuit simulations for the maximum power through each heater for 5V and 10V.

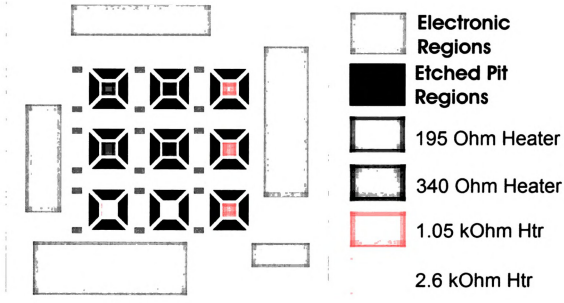


Figure 4-2: *Block diagram of biosensor array sites. Indicated colors represent various heater resistor values.*

Table 2: *Power dissipation through heater resistors from Spice circuit simulation*

Resistive Value	Power at 5V Supply	Power at 10V Supply
195 Ω	96.1 mW	192.3 mW
340 Ω	63.45 mW	126.9 mW
1.05 kΩ	22.8 mW	45.6 mW
2.6 kΩ	9.45 mW	18.9 mW

These power levels should be more than sufficient to provide well over 180°C for systems incorporating sufficient thermal isolation. Conversely, a system with inadequate isolation will most likely fall well short of the required protein heating.

4.2 Temperature Sensing Network

The second half of the incorporation of thermal control involves the ability to accurately measure both the ambient and array site. The original design provides a

resistive bridge circuit for temperature sensing at the array sites and a simple resistor acting as a basic ambient sensor.

4.2.1 Resistive Bridge Network

It was intended that a Wheatstone bridge be used for detecting the small variations in the resistive value for the temperature sensor resistor. The Wheatstone bridge, shown in Figure 4.3, consists of two voltage dividers with matched resistors.

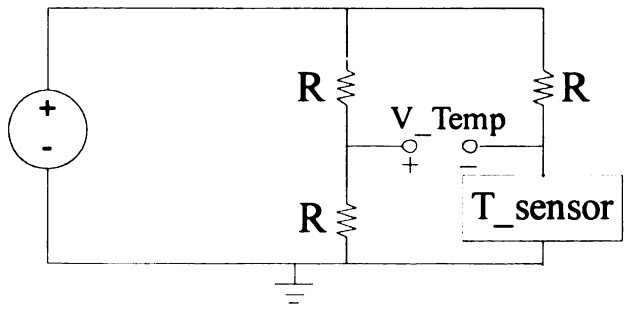


Figure 4-3: *Bridge configuration for temperature sensing network of MEMS system [14]*

When a control voltage is applied, the circuit will establish a voltage differential, V_Temp, which is defined by the two voltage dividers. All the resistors except the sensor resistors are matched on the layout and are very close on chip to ensure device matching. The resistive value of the temperature sensing element will be $R + \Delta R_T$, where ΔR_T is given by the following equation:

$$\Delta R = \alpha_p R \Delta T$$

where α_p is the Temperature Coefficient of Resistance of the polysilicon temperature sensor. If there is no difference in temperature between the sensor and the bridge elements, all resistors will simply have a resistance of R so the output voltage across the bridge will ideally equal zero. However, if there is any temperature difference, the output

voltage, V_temp, will correspond to that temperature difference according to Equation 4-1

$$V\_temp = \left(\frac{-\Delta R_T}{2(2R + \Delta R_T)} \right) \qquad \textbf{Eq. 4-1 [14]}$$

If the TCR of the polysilicon is known, this equation can be translated to Equation 4-2, which gives us the temperature difference.

$$\Delta T = \frac{4V\_temp}{-\alpha_p (V_{IN} + 2V\_temp)} \qquad \textbf{Eq. 4-2 [14]}$$

Where ΔT is the difference in temperature between the reference temperature at which the chip is held and the temperature at the selected array site. The TCR can be found by characterizing the change in resistance of the temperature sensor resistors over a wide temperature range in a highly controlled temperature environment.

4.2.2 Temperature Array Sites

Each array site has a polysilicon resistive temperature sensing element which enables the measurement of the array site temperature relative to the background temperature. This design employs a technique common to commercial temperature sensing devices in which the temperature sensing operation is based on the TCR of the sensing material. However, in commercial sensors a material such as platinum is usually used for the temperature sensing resistor. Undoped polysilicon is used in this research due to the availability of the material in the chosen fabrication process, the extremely close proximity to the heating layer, and the fact that undoped polysilicon has a much higher resistance than doped poly. This is advantageous in all but eliminating any heating of the sensing resistors due to the current through the resistors generated by

voltage source placed across them, which would corrupt the array temperature data. These sensing resistors were all designed with nominal resistance values of 200 kΩ.

4.3 Thermal Isolation Structure

It is imperative that a MEMS structure for the heated biosensor array provide sufficient thermal isolation for each array site from its nearest neighbor and the bulk substrate in order to generate sufficient heating at low power. Sacrificial and bulk micromachining can be used to generate a structure capable of providing such isolation, shown in Figure 4.4. There are a variety of issues associated with this structure and the chosen fabrication process that must be considered during design.

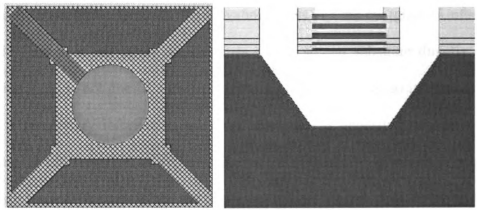


Figure 4-4: *Desired suspended array site formed by sacrificial etching and bulk micromachining*

In order to frontside process the die, AMI C5N process layers must be utilized as masking and sacrificial layers to realize a thermally isolated structure. Ideally we would like to leave an opening to the silicon surface through the overglass and passivation layers, shown in Figure 4.5, after fabrication steps.

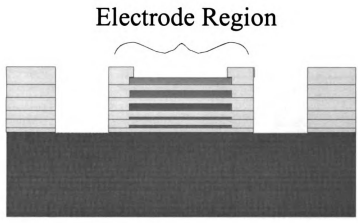


Figure 4-5: *Ideal, and ultimately desired, structure providing for openings to the silicon substrate for bulk micromachining. This structure is, unfortunately, not available straight from the fabrication house.*

Ideally, this would consist of drawing layers of Active, Contact, Via, and Overglass to generate the appropriate openings in passivation layers and the overglass. Unfortunately, the AMI C5N does not allow for openings to the silicon substrate directly from the fabrication facility, not does it allow for oversize contacts or vias, so intermetal dielectic (which is proprietary information and thus unknown) is deposited into these regions. This material can be etched away, but if it contains silicon nitride, which is suspected, it is difficult to mask the rest of the die to protect against the hot phosphoric acid etchant. Hence, it is necessary to use sacrificial etching techniques employing the existing layers in the AMI C5N process to expose the silicon surface. Due to the possibility of a silicon nitride dielectric, there is really only one way to provide openings down to the silicon substrate. This entails using metal and via layers as sacrificial layers to be etched away to access the silicon substrate, as shown in Figure 4.6.

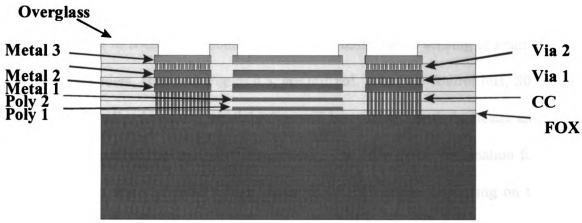


Figure 4-6: *Sacrificial etch design using metal and via layers as sacrificial layers. A subsequent metal and anisotropic bulk etch step is then performed to generate suspended MEMs structures.*

This design incorporates a PR masking layer that is not attacked by the aluminum or oxide etchant. In order to reach the silicon surface, 2 etches must be performed. First, an aluminum etch is performed, which clears out metals 1-3 as well as the contact material, exposing hundreds of holes down to the substrate oxide from the surface. Second, an oxide etch will clear away any surface oxide to provide access to the substrate. After the silicon is exposed, an extended anisotropic etch will finally release the proposed MEMS suspended structure, providing thermal isolation for the biosensor array sites. The process is illustrated in Figure 4.7.

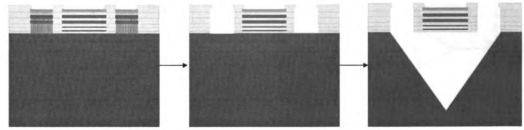


Figure 4-7: *Sacrificial etch design etches sacrificial metal and via layers to expose the silicon substrate, which is then anisotropically etched to form suspended microstructures.*

4.4 Array Site Selection

In order to access a particular array site for temperature sensing or heating, NOR and AND decoders, shown in Figure 4.8, are utilized. The two control bits, S0 and S1, supplied externally, determine which bit line will be enabled. Both the heater and sensor arrays have identical row and column decoders. The only input combination for any of the NOR gates that will yield a high output is 00. Therefore depending on the input signals, only one bit line can be logic high at any time. Additionally, each bit line is enabled utilizing a transmission gate and discharged through transistor. The entire array is enabled when the En' pin is grounded and disabled when the bit is pulled high.

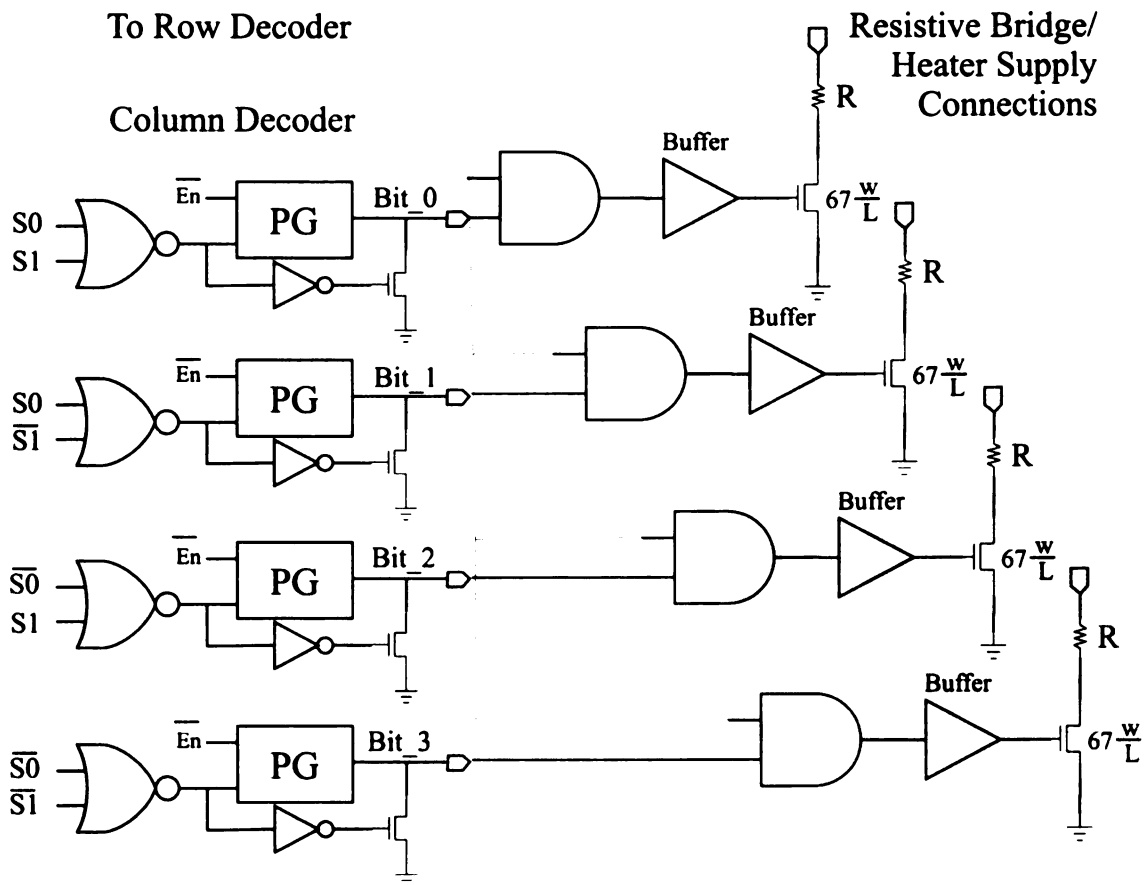


Figure 4-8: *Example schematic of array selection circuit*

The bitlines select the individual sites using the illustrated AND decoder, which is then buffered to provide the necessary drive to the large transistor, which, when enabled, connects a chosen temperature sensor or heating element to ground, thereby completing either the bridge or heater circuit. The buffer is required to drive the parasitic capacitance inherent in all the array sites, which are essentially in parallel with each other. A large selection MOSFET minimizes the transistor Ron, which both enables close matching of the resistances in the bridge circuit and minimizes power loss in the heating supply lines.

Figure 4.9 presents the select bits necessary to access individual array sites. Note that while there are four row and column bit lines, chip real estate limited our array to 3x3, thereby making it necessary to leave row bit_0 and column bit_3 disconnected from all circuitry.

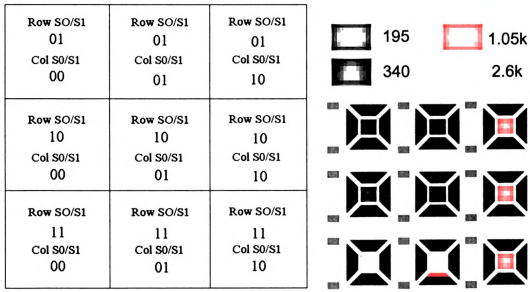


Figure 4-9: *Select bits and corresponding array sites*

Chapter 5: Results and Characterization

The goal of creating integrated an integrated biosensor array interface capable of heating, heat sensing, and interfacing with electrochemical analysis systems has been achieved. Several versions of electrode arrays based on passive substrates were fabricated and secondary alcohol dehydrogenase and sorbitol dehydrogenase proteins were deposited on the electrode surfaces. Further, Two electrode arrays were fabricated on active circuitry and two more were fabricated on active circuitry with heating and sensing capabilities. The details are laid out in the following.

5.1 Electrode Array Fabrication

Several different versions of a 2x2 electrode array were fabricated on P-type silicon wafers using the process outlined in Appendix A. Some of these are pictured in Figure 5.1. In order to expedite the fabrication process to quickly supply our colleagues with base material for protein deposition experiments, the reference electrodes were fabricated separately, also shown in Figure 5.1, or a standard reference electrode was utilized in the test procedures.

Figure 5-1: *Three electrode electrochemical arrays (left) and separate reference electrodes (right)*

As there was no literature found listing a wet etchant for the spin-on-glass and spin-on-glass is similar in chemical makeup to Silicon Dioxide, BHF was used. Initial

fluorescence microscopy results seemed to indicate that the protein was attaching to the SOG and not the gold, illustrated in Figure 5.2, and that perhaps the SOG mask was inverted. In order to verify that the SOG was patterned in the manner intended, an SEM micrograph was taken, a surface profile was done, and a standard micrograph was taken (Figure 5.2), all of which correlate and indicate the patterning was correct. It was suspected that gold may absorb illuminescence generated very close to the surface.

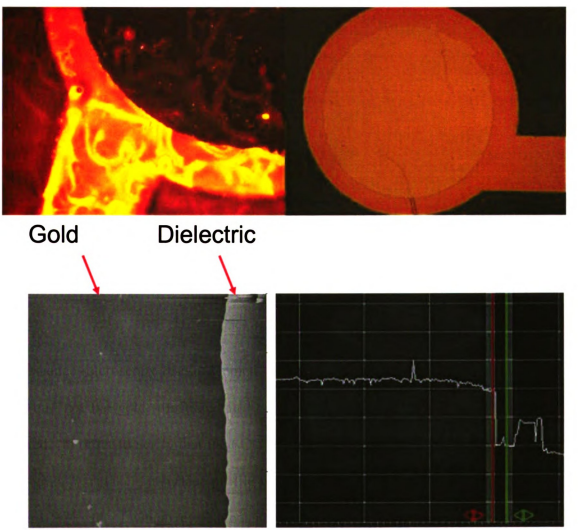


Figure 5-2: *Working electrode fluorescence microscopy (top left), micrograph (top right), AFM (bottom left), and profile (bottom right) showing a SOG step of ~ 400nm*

The chips were immersed in Potassium Ferric Cyanide solution and a CV curve was generated in order to illustrate proper functionality. The resulting curve has the characteristic shape of a three electrode electrochemical cell and is shown in Figure 5.3. Following verification of functionality, sorbitol dehydrogenase was assembled on the electrode surface and immersed in varying concentrations of sorbitol solution, generating the CV curves shown in Figure 5.3

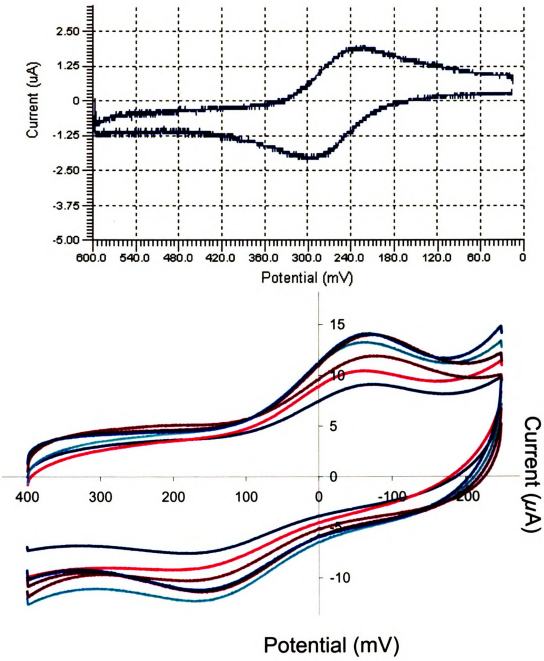


Figure 5-3: *CV curve of electrode array in Potassium Ferric Cyanide solution indicating proper functionality (top), CV concentration curves for sorbitol dehydrogenase in sorbitol solution(bottom). Courtesy of Dr. R. M. Worden*

Once the electrodes on passive substrates were fabricated and functioning as expected, the fabrication process was applied to the active MOSIS die, outlined in

Appendix A as well. Once the electrodes were formed, illustrated in Figure 5.4, the chip was wirebonded to a copper etched board, with all of the working electrodes bonded together for readout convenience. Wires were then soldered to the board and the traces and wirebonds were covered with epoxy. The resulting CV verification curve, also shown in Figure 5.4, was taken using a bench-top potentiostat.

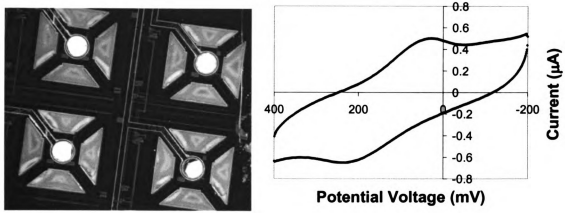


Figure 5-4: *On-chip working electrodes (left) and CV curve verifying functionality (right)*

5.2 Thermal Isolation Structures

The thermal isolation structure fabrication process did not work as designed. Originally, the AMI process metals were believed to be Aluminum, which can be etched with Phosphoric + Acetic + Nitric Acid. However, it was later discovered that the metal layers are TiN/AlCu/TiN. TiN can be etched with BHF, as can Aluminum, so the process needed to be modified to initially etch the pits with BHF. In fact, assuming the intermetal dielectric was silicon dioxide, the pits could simply be etched using BHF and then TMAH. Unfortunately, this etch did not work as intended either. It is now believed that the intermetal dielectric is silicon dioxide and silicon nitride. In addition, TMAH also etches the AMI metals, so an extended TMAH etch undercut the masking layer and

etched away the electrodes, shown in Figure 5.5. In an effort to avoid this, KOH was utilized due to a specific source indicating it did not etch Al. The results of this etch were contradictory to that source, as it did indeed etch away the metal layers as well as the oxide, overetching the island, also shown in Figure 5.5

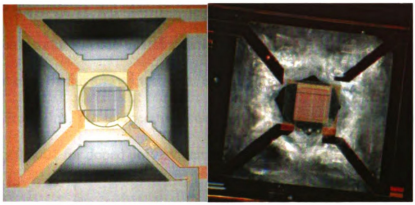


Figure 5-5: *TMAH etching of CMOS metal layers (left) KOH over etch of thermal isolation structure (right)*

Ultimately, alternating BHF and the Aluminum etchant provided access to the silicon substrate, which was then etched with a TMAH/Ammonium Persulfate/Silicon solution that protects the metal layers. This process is outlined in Appendix A. The results of successful etching are presented in Figure 5.6.

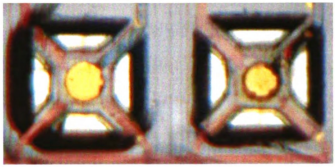


Figure 5-6: *TMAH etching generating thermal isolation structures*

5.3 Heater Characterization

The heaters and polysilicon temperature sensors were characterized using a regulated temperature chamber. Due to unforeseen complications with temperature sensing resistors being damaged, shown in Figure 5.7, the Wheatstone bridge could not be utilized to characterize and readout the heaters. Instead, in order to characterize the system, the temperature in the chamber was adjusted and the change in resistance was monitored for each of the array sites. The temperature vs. resistance plots are shown in Figure 5.8. From this, the temperature coefficient of resistance was determined to be approximately 0.0001 for doped poly, which is consistant with the literature.

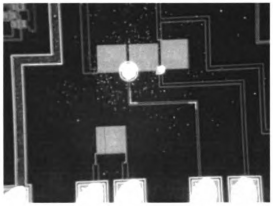
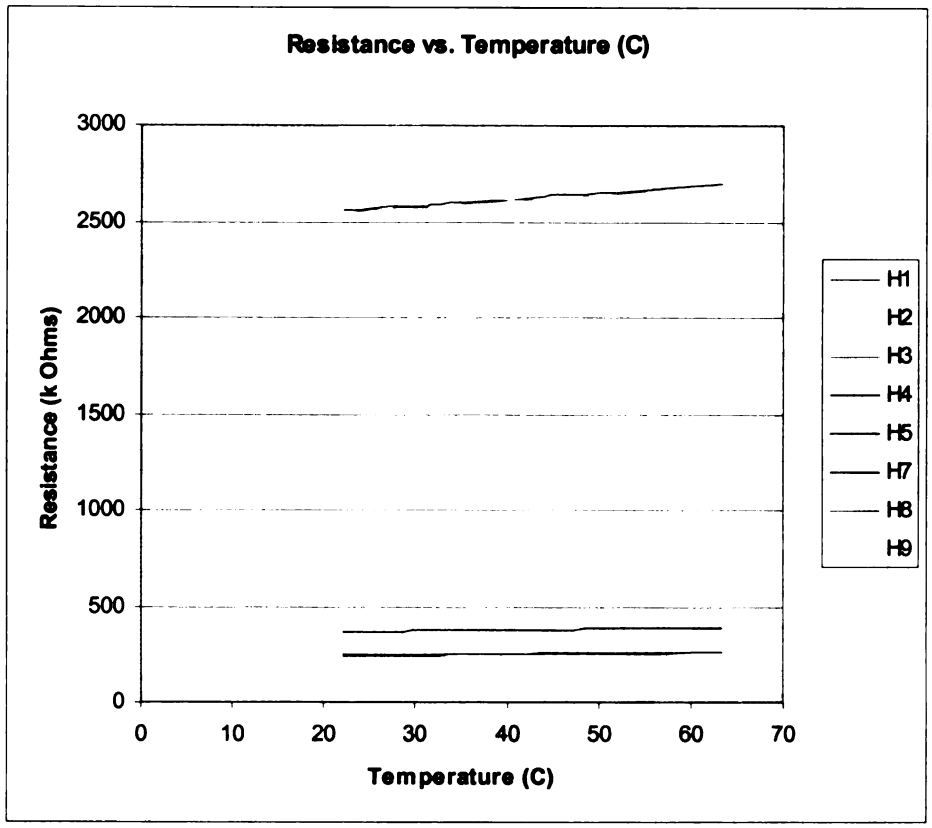


Figure 5-7: *Temperature sensing bridge resistor damage*



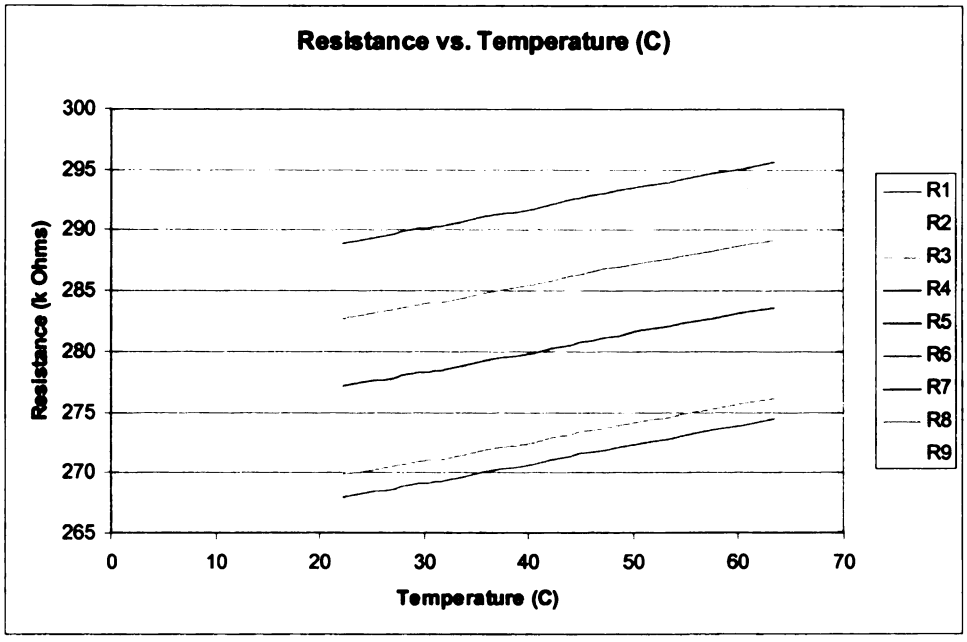


Figure 5-8: *Temperature vs resistance for polysilicon heaters(top) and sensors (bottom)*

After the temperature coefficient of resistance was determined, the heaters were characterized for a chip without isolation structures and for a chip with etched pits. To do this, a voltage was applied across the heating resistors, which were chosen via the integrated array selection circuitry. The temperature generated was determined by first measuring the resistance of the heater, applying the voltage for several minutes, and subsequently measuring the resistance value, from which the temperature can be determined. The temperatures generated in these chips are presented in Figure 5.9.

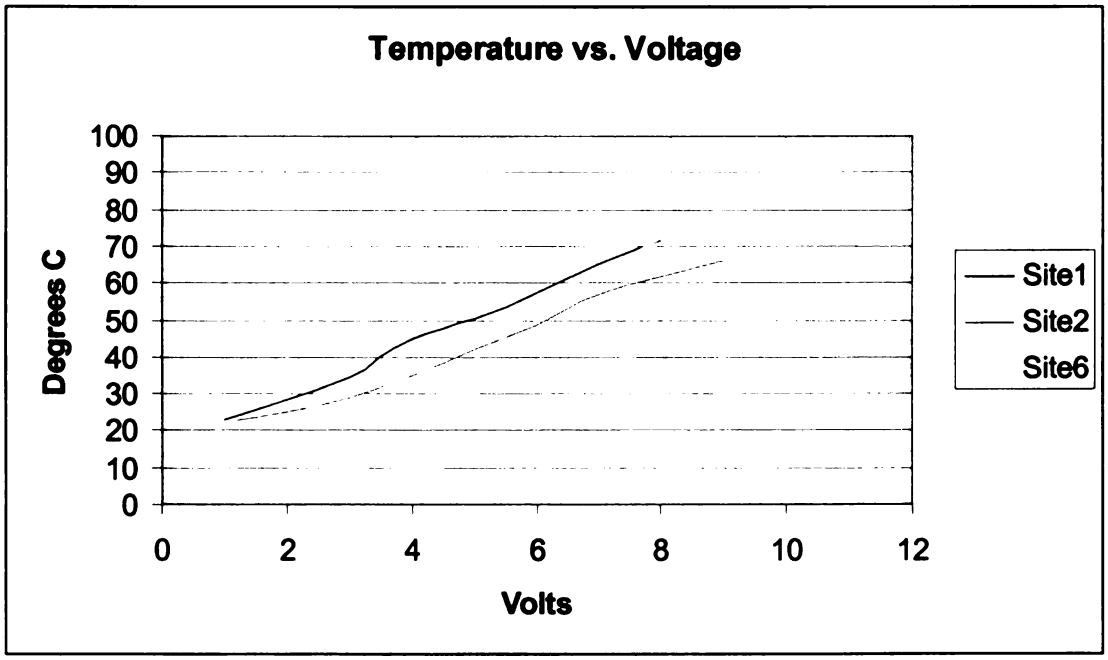
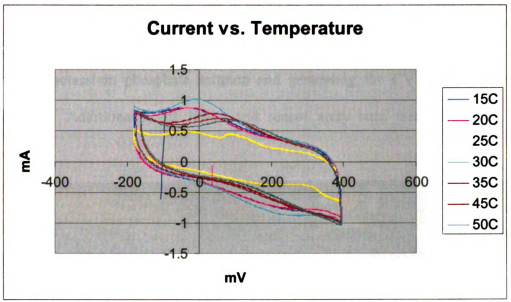


Figure 5-9: *Temperature generated by poly heaters vs, input voltage*

Once heating capabilities were established, Secondary Alcohol Dehydrogenase was assembled on the surface of a 2x2 array in order to be thermally tested for reactivity. The electrode system was immersed in a solution 0.3ml 2-propanol (IPA) in 80ml Phosphate Buffer (PBS-PH7.4) and heated up to 50C while CV testing was taking place,

which generated the CV curves in Figure 5.10 and the plot of maximum current, which is directly proportional to reactivity, vs. temperature. This plot is consistent with the literature, showing that the protein has an optimal operation temperature.



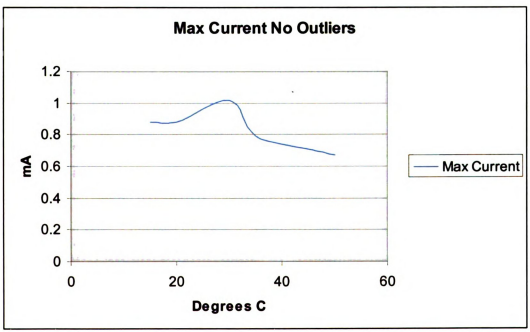


Figure 5-10: *CV curves for SADH at various temperatures (top) Reactivity of SADH vs temperature (bottom)*

5.4 Integrated Biosensor Interface

Once all the steps were perfected individually, they simply needed to be integrated to generate the integrated biosensor interface, shown in Figure 5.11. The fabrication process for this is discussed in detail in Appendix A. The resulting interface was verified to be functional and readable by the on-chip potentiostat by immersing the interface in potassium phosphate solution and generating the CV curve(s) shown in Figure 5.11. Additionally, the heater and sensor array sites were cycled to verify accessibility.

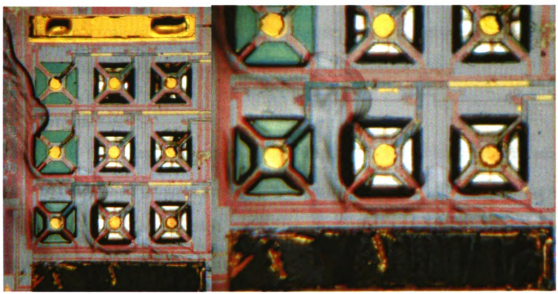


Figure 5-11: *Integrated biosensor interface*

Chapter 6: Conclusions and Future Work

In this work, an integrated biosensor interface was designed, fabricated, and tested enabling on-chip readout of three electrode electrochemical arrays and thermal control of individual array sites. A post-CMOS compatible fabrication process allowing the integration of active circuitry, thermal control, electrochemical cells, and bio-interfaces was realized, despite limited process information and the lack of dry etching facilities. This in itself proves that mass fabrication of these sensors could be easily and inexpensively realized. This sensor could one day lead the way toward revolutionary advances in the study of proteins and point of care diagnosis of disease.

6.1 Contributions

This thesis describes several major contributions to this body of work and the work of the AMSaC group in general. Specifically, the main contributions of this work are the definition of a fabrication process for post-CMOS formation of electrode arrays suitable for biosensors, the identification of a procedure for thermal isolation of electrode arrays on the surface of a CMOS chip, and the integration of post-CMOS electrode arrays suitable for biosensors and thermal isolation structures benefiting them. All of these procedures are available in Appendix A as step by step procedures.

The fabrication process for post-CMOS formation of electrode arrays suitable for biosensors is broken down into three major parts: metal film deposition, photolithography, and etching. First, biologically friendly metals titanium, gold and silver are deposited on a substrate, both passive and fabricated IC die, using PVD e-beam evaporation. Photolithography is then performed and the metal layers are etched to form

three electrode structures suitable for protein attachment. Finally, spin-on-glass was deposited and patterned in a similar manner both for array site isolation as well as to enable proper protein coverage of the electrode.

The procedure for thermally isolating the electrode structures is limited to photolithography and etching. First, a photoresist layer is applied and patterned. Then, an etch is performed to remove the three metal layers and intermetal dielectrics in order to gain access to the silicon substrate. Finally, and extended silicon etch is performed to undercut the heating and sensing circuitry as well as the electrode site, thereby thermally isolating the electrode and allowing for its thermal control. This was especially challenging due to the unknown nature of the process layers used in the AMI C5N process. Specifically, it was unknown the process metals contained TiN and it is suspected one of the intermetal dielectrics is silicon nitride.

The integration of the two processes was a natural progression. The two processes were simply altered in order to enable the formation of both the post-CMOS electrode array structures and the thermal isolation structures. In fact, many of the layers deposited for the array site formation, like gold, further protect underlying layers from the possibility of being etched away during the release of thermal isolation structures.

6.2 Future Work

Future work will consist of development of a fabrication utilizing DRIE instead of wet etching and the design of high density arrays and new thermal sensing capabilities. DRIE is much more easily duplicated and controlled than wet etching, as is demonstrated in the literature, and also possesses the capability to etch silicon nitride, which is suspected to be one of the intermetal dielectrics. Additionally, the thermal sensing

capabilities could benefit greatly from a true voltage reference. This would make temperature readout infinitely more accurate and convenient. Finally, if undoped, high resistance poly resistors are used again, multiple contacts should be placed between the poly and metal 3 to insure structural integrity.

APPENDIX A
Fabrication Processes

Fabrication Process for Three Electrode Arrays

1) Superglue chip to glass slide
2) Deposit 20nm Ti and 100nm Au using PVD
3) Cover chip with "chip holder" using tape (reduces photoresist buildup at edges of chip)
4) Spin on photoresist (microposit 1813) for 40 seconds at 4500 RPM
5) Remove chip holder
6) Soft bake for 1 minute at 115 C
7) Expose (on our aligner) for 90s
8) Develop for 30s in developer
9) Hard bake for 20 minutes at 135 C
10) Etch Gold Using Gold Etchant Type A (KI) for 30s
11) Etch Ti in BHF (1:5) for 1s
12) Remove photoresist (using acetone)
13) Deposit 100nm Ag using PVD
14) Repeat steps 3-9
15) Etch Ag using the same gold etchant (type A) for 1 second
16) Remove photoresist
17) Repeat steps 3-9
18) Immerse chip in 1M FeCl3 solution for 120 minutes at 30 C
19) Dry chip, place in dessicator for 24 hours
20) Coat with Nafion
21) Let dry
22) Remove PR
23) Place in dessicator for 24 hours
24) Wirebond
25) Cover wirebonds with epoxy

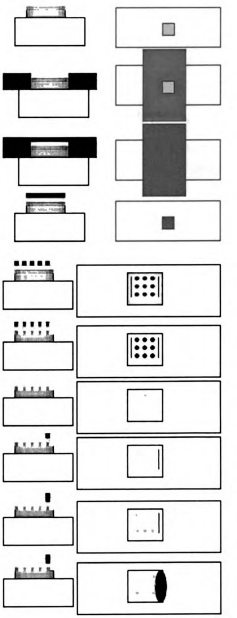


Figure A-1: *(Right) Electrode formation process*

Thermal Isolation Etch Process

1) Superglue chip to glass slide
2) Cover chip with "chip holder" using tape (reduces photoresist buildup at edges of chip)
3) Spin on photoresist (microposit 1813) for 40 seconds at 4500 RPM
4) Remove chip holder
5) Soft bake for 1 minute at 115 C
6) Expose (on our aligner) for 90s
7) Develop for 30s in developer
8) Hard bake for 20 minutes at 135 C
9) Etch with BHF for 30s
10) Etch with Aluminum Type I etch @ 50^0C with agitation for 5 minutes
11) Etch with BHF for 5 minutes
12) Alternate Al Type I and BHF etches 1 minute each until silicon is exposed
13) Etch with TMAH/Ammonium Persulfate/Silicon solution @ 80^0C with agitation for 90 minutes
14) Remove photoresist (using acetone)

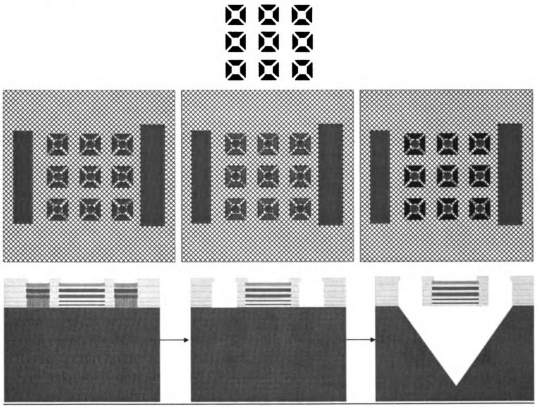


Figure A-2: *(Top) Mask for thermal release structures. (Middle)Top view of chip during etch process. (Bottom) Cross sectional view of chip during etch process.*

System Etch Process

1) Superglue chip to glass slide
2) Deposit 20nm Ti and 100nm Au using PVD
3) Cover chip with "chip holder" using tape (reduces photoresist buildup at edges of chip)
4) Spin on photoresist (microposit 1813) for 40 seconds at 4500 RPM
5) Remove chip holder
6) Soft bake for 1 minute at 115 C
7) Expose (on our aligner) for 90s
8) Develop for 30s in developer
9) Hard bake for 20 minutes at 135 C
10) Etch Gold Using Gold Etchant Type A (KI) for 30s
11) Etch Ti in BHF (1:5) for 1s
12) Remove photoresist (using acetone)

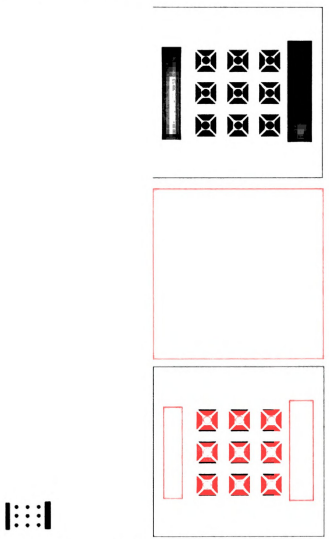


Figure A-3: *(Left) Mask for first 12 steps of process. (Right) Top view of chip during etch process.*

System Etch Process

13) Deposit 100nm Ag using PVD
14) Repeat steps 3-9
15) Etch Ag using the same gold etchant (type A) for 1 second
16) Remove photoresist

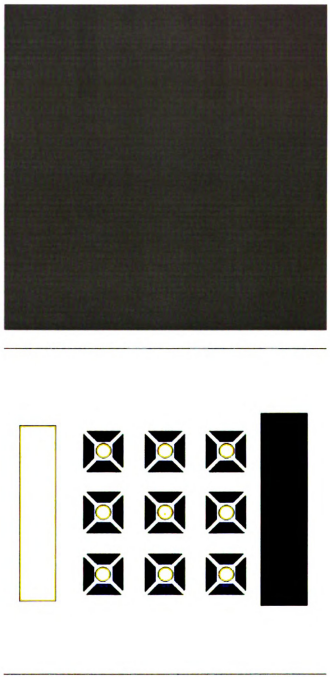


Figure A-4: *(Left) Mask for steps 13-16 of process. (Right) Top view of chip during etch process.*

System Etch Process

17) Pipette on Accuglass, let sit for 60s
18) Spin for 45s at 300RPM
19) Bake at 80^0C for 1 minute
20) Bake at 150^0C for 1 minute
21) Bake at 250^0C for 4 minutes
22) Repeat steps 3-9
23) Etch SOG with BHF for 30s
24) Remove photoresist

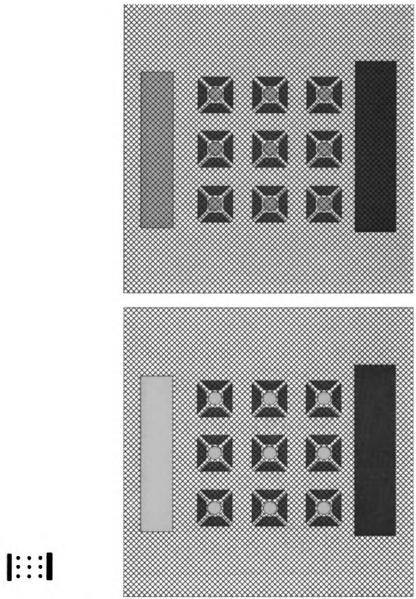


Figure A-5: *(Left) Mask for steps 17-24 of process. (Right) Top view of chip during etch process.*

System Etch Process

25) Repeat steps 3-9
26) Etch with BHF for 30s
27) Etch with Aluminum Type I etch @ 50^0C with agitation for 5 minutes
28) Etch with BHF for 5 minutes
29) Alternate Al Type I and BHF etches 1 minute each until silicon is exposed
30) Etch with TMAH/Ammonium Persulfate/Silicon solution @ 80^0C with agitation for 90 minutes
31) Remove photoresist

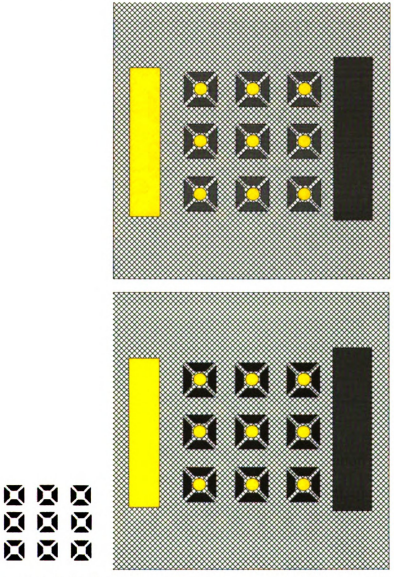


Figure A-6: *(Left) Mask for steps 25-31 of process. (Right) Top view of chip during etch process.*

System Etch Process

32) Repeat steps 3-9
33) Immerse chip in 1M FeCl3 solution for 120 minutes at 30 C
34) Dry chip, place in dessicator for 24 hours
35) Coat with Nafion
36) Let dry
37) Remove photoresist
38) Place in dessicator for 24 hours
39) Wirebond
40) Cover wirebonds with epoxy

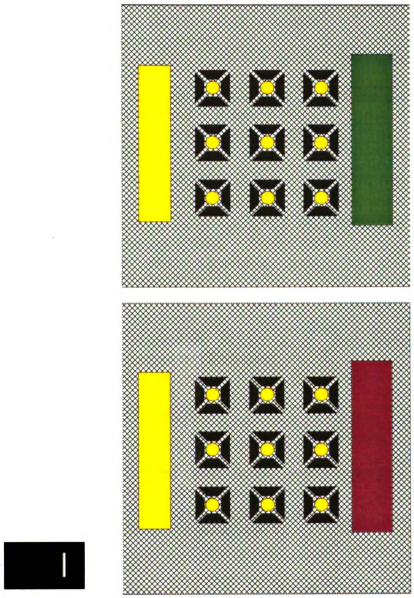


Figure A-7: *(Left) Mask for steps 32-40 of process. (Right) Top view of chip during etch process.*

APPENDIX B

Etchants for AMI C5N Compatible Post-CMOS Processing

Table 3: *Etchants for AMI C5N Compatible Post-CMOS Processing*

Material	Wet Etchant	Masking Material	Etch Rate (Å/min)
Ag	KI	Photoresist	1.8-6 μm
Ag	CR-7 : 9% $(NH_4)_2Ce(NO_3)_6$ + 6% $HClO_4$ + H_2O (Available from Cyantek)	Photoresist	450
Ag	5-9 HNO_3 : 1-5 H_20 @ 39-49°C	Photoresist	12-25μm
Al	Aluminum Etchant Type A: Phosphoric + Acetic + Nitric Acid + Water 16:1:1:2 @50°C	Photoresist	6600
Al	BHF	Photoresist	1400
Au	Potassium Iodine (KI)	Photoresist	.5-1 μm
Cr	Hydrochloric Acid (HCl)	Photoresist	1500
Cr	Chromium Etchant CR-7: 9% $(NH_4)_2Ce(NO_3)_6$ + 6% $HClO_4$ + H_2O (Available from Cyantek)	Photoresist	170
Si (Isotropic)	HF + HNO_3 + Acetic (1:3:8)	SiO_2, Si_3N_4	50 μm
Si (Anisotropic)	TMAH: 0.5% $(NH_4)_2S_2O_8$ (Ammonium Persulfate): 1% Si	SiO_2, Si_3N_4	10k (100) 40-100 100/111 etch ratio
Si (Anisotropic)	KOH@80°C	Silicon Nitride	14k (100) 400 100/111 etch ratio
SiO_2	Buffered Hydrofluoric Acid (BHF) 5:1 ammonium fluoride NH_4F : hydrofluoric acid HF	Photoresist	1000
Si_3N_4	Phosphoric Acid@160°C	Silicon Dioxide	19-28
Ti	BHF	Photoresist	>10k
Ti	Titanium Etchant $20H_20$:$1H_20_2$:1HF	Photoresist	8800
TiN	BHF	Photoresist	2.5

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