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thesis entitled

A COMPACT FULLY ON-CHIP IMPEDANCE SPECTROSCOPY SYSTEM

presented by

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has been accepted towards fulfillment
of the requirements for the

M.S. degree in Electrical Engineering

Major Professor's Signature

May 10, 2007

Date

A COMPACT FULLY ON-CHIP IMPEDANCE SPECTROSCOPY SYSTEM

By

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A THESIS

Submitted to
Michigan State University
in partial fulfillment of the requirements
for the degree of

MASTER OF SCIENCE

Department of Electrical Engineering

2007

ABSTRACT

A COMPACT FULLY ON-CHIP IMPEDANCE SPECTROSCOPY SYSTEM

By

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Impedance Spectroscopy (IS) is a powerful technique for characterizing materials and interrogating many sensors, particularly within evolving nanotechnologies. Applications for this technique range from DNA identification to trace vapor detection. The instrumentation to support these emerging applications has, however, lagged far behind the materials and sensor research. To enable next-generation micro-scale systems based on nanotechnologies, on-chip IS instrumentation are needed. This thesis presents a new mixed-signal integrated circuit suitable for chip-scale implementation of IS instrumentation to support high density sensor arrays within a microsystem platform. The circuit is based on the frequency response analyzer approach for IS, which is best suited to the slow changing parameters measured by many sensors, including a model chemiresistor gas sensor array. In 0.5μm CMOS, the IS circuit occupies 205μm x 108μm and can operate from 33.3Hz to 1.66kHz. The results of this thesis demonstrate that high density sensor arrays and their readout circuitry can all be integrated on one low power low cost integrated chip, meeting the needs of many current and upcoming IS applications.

Dedicated to my parents who have been my first and best teachers, not only of knowledge, but of a passion for learning, and the discipline crucial to both.

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Chapter 1: Impedance Spectroscopy

I. Introduction

Impedance Spectroscopy (IS) is emerging as a powerful technique in the field of micro-scale sensing. IS is commonly used in many macro-scale applications such as monitoring electrochemical reactions, testing coatings [1], testing batteries [2] and many other applications [3],[4]. Recently, it has begun to be applied to micro-scale sensors across a wide variety of applications. These micro-scale applications hold great promise for biological research and medical applications. The explosive growth of potential applications for IS has jumped far ahead of the instrumentation necessary to enable these applications. The goal of this research is to begin work in developing the underlying circuitry that will be necessary to enable the potential applications to be realized.

II. Overview of IS

Some general categories of micro-scale IS applications will be presented along with some representative literature. The goal is to introduce the scope of IS and consider the instrumentation requirements. After giving an overview of the applications, the fundamentals of IS will be presented.

A. Applications

IS has been used for quite some time to investigate human tissue. For example, Peura, Ristic, Kun, et. al. have written a series of papers on detecting tissue ischemia (lack of oxygen and nutrients to tissue eventually resulting in the death of the tissue) [5], [6], [7], [8], [9]. Although, their work is not on the micro-scale, the ability to implement on-chip IS might greatly expand the applications of this work. For instance, [10] shows that IS can detect ischemia leading to organ failure in the intestine. For this to be brought to practical

application, an embedded sensor would be necessary. Additionally, IS has been applied for the detection of skin cancer [11] and skin irritation [12].

More recently, IS has been coupled with on-chip fluidics for particle detection. This research allows for differentiating various particle types [13], monitoring position of particles [14], and measuring the size of the particle [15]. One unique application is the testing of neural probes. It is necessary that the "cultured probes" be well covered and sealed by neural cells. IS was applied to inspect the probes and determine the state of their coating [16]. The use of IS in on-chip fluidics again naturally leads to the need for on-chip IS instrumentation circuitry.

Not only can particles be detect, but if the analyte is a cell, it has been shown that a great deal of information about cells can be extracted using IS. Work has been published showing that it is possible to detect and sort blood cells [17] based on abnormalities in the cells, this is applicable for use in cancer screening [18], [19]. Other authors have been able to inspecting cell's membranes and cytoplasm [20] and detecting bacterial viability [21]. Although, there are still some limitations of size, range, and sensitivity. [22] states that IS will become an important technique in impedance based single cell measurements. The goal of this research is to help address some of those issues, specifically size and sensitivity.

Biological sensors are a key area of application for IS. It has been used for "immunosensors, DNA sensors and biocatalytic enzyme-based biosensors" [23]. The DNA sensors have been used to classify unknown DNA strands [24] and for other applications [25]. Another key biosensor application is the use of proteins bonded to electrodes. As the proteins react to specific chemicals, the reaction can be measured using IS [26], [27], [28], [29]. The protein-based sensors offer a wide variety of possibilities because proteins are

very selective and proteins can be found that will react with many different chemicals. Many of these sensors present the possibility of creating high density sensor arrays. Such arrays could use many different proteins to provide a wide range of analyte detection.

The protein-based sensors usually only operate in solutions; however there are other sensors capable of detecting chemicals in gas [30], [31]. These sensors are usually treated as simple resistive sensors, referred to as chemiresistors (CR), but research is being done to determine what extra information IS may yield. While an on-chip IS system is applicable to all of the above applications, this project specifically targets detecting the impedance information in gas sensors.

B. Impedance Spectroscopy Basics

IS is the process of measuring a sensor's impedance (complex resistance) response over a wide range of frequencies. A great deal of information can be gathered from the impedance spectrum, and this has opened up many of the above exciting applications.

The reason IS provides so much information is that the response of the system changes with frequency. Thus, a broad range of information can be collected in a single measurement. The physical reasons for this vary between each system. To simplify the physical details a sensor is generally modeled using an equivalent circuit. (Two common equivalent circuit are shown in Figure 1.) The equivalent circuit is a model that gives the same impedance response as the system being measured. Typically the component values of the equivalent circuit can be mapped to the physical properties of the sensor.

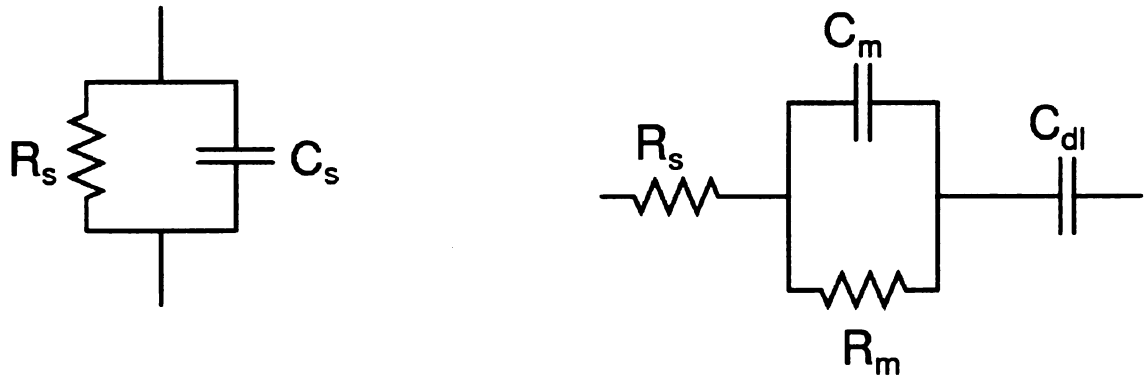

Figure 1: Two typical equivalent circuits are shown. (a) is a possible equivalent circuit for gas sensors. (b) is a common equivalent for sensors in solution.

Generally, the sensor's equivalent circuit remains constant, but as it responds to its environment one or more component values change. For sensors this becomes a valuable tool, because once the equivalent circuit of a sensor is known, the interface circuitry need only identify the change in component values to detect a change in the system.

The response of a sensor is often visualized using a Bode (Figure 2) or Nyquist plot (Figure 3). Because the impedance values are complex numbers they can be represented in two different ways. A Bode plot shows the amplitude and phase values across the range of frequencies. The Nyquist plot shows the data as real vs. imaginary. The equivalent circuit values, ie. the sensor response, can be found from either plot.

As an example, a Tethered Bilayer Lipid Membrane (tBLM) sensor has an equivalent circuit like the one shown in Figure 1 (b) [26]. When the proteins in the tBLM react, this is reflected by a the change in the value of R_m. The plots below show the response of the sensor for three values of R_m. In the case of a tBLM sensor, the interface circuitry would need to be able to accurately detect the shift in response in the sub-Hertz range.

A good overview of IS from a chemists' perspective is given in [23].

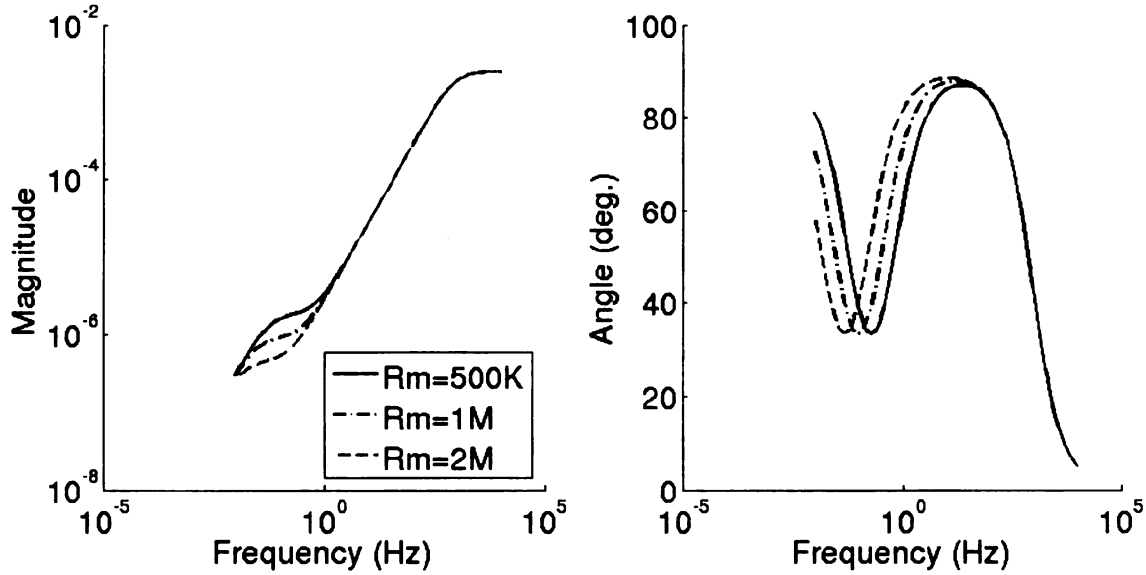

Figure 2: Bode Plot of tBLM sensor response, shows the change in R_m in both phase and magnitude.

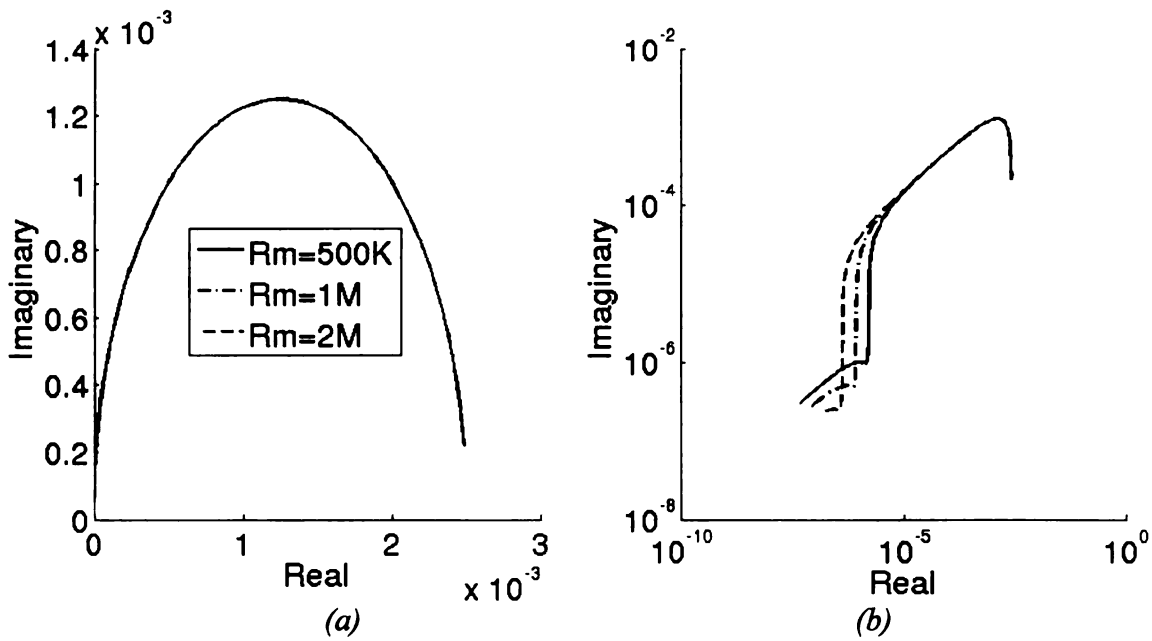

Figure 3: Nyquist plot of tBLM sensor response. (a) is on linear axes as is typical. (b) is on log-log axes to make the change in response clear.

III. Motivation for On-Chip IS

Clearly many applications exist for IS, and much work has been done in testing and expanding these applications. Nearly all of the applications above attach on-chip probes to bench-top instruments (either some form of network analyzer or a PC with a DAQ) to do

the actual impedance measurement. While bench-top instruments are useful for initial research they present some serious limitations as well. Bench-top equipment can be very expensive, which severely limits any sort of large scale deployment or production of the IS systems. Some of the applications listed above present exciting possibilities for portable or even in vivo applications, however the size and power requirements of bench-top equipment make this impossible.

Some of the sensor applications (especially the DNA, protein, and chemiresistors sensors) offer the possibilities of a high density array of sensors. It is not possible to bring hundreds of sensor leads all out to a bench-top instrument. Multiplexing the raw signals is also not possible because of transistor leakage. In a typical CMOS process, the transistor leakage is around 10pA [32]. If one hundred channels are multiplexed, then the total leakage through the multiplexer will begin to approach the same magnitude as that of the signal [33]. Finally, long leads required for bench-top equipment increase the amount of noise coupled onto the system. The goal of this research is to begin to address these needs by providing a fully on-chip IS system capable of supporting high density arrays of sensors.

A. Literature Review

There are a number of IS systems which have been developed which rely on computers for most of their computation. [34] uses discrete components on a PCB to perform measurements. In this case, a sinusoidal stimulus is applied and the output is amplified and read by a computer. It appears that only the amplitude is measured and the full sensor response is then inferred from the amplitude and a known equivalent circuit. In a similar manner, [5] uses discrete components to stimulate and read the sensor. The raw data from the sensor is then digitized and passed to a computer which computes the amplitude and

phase data from this. Instead of using a sinusoidal stimulus, [18] stimulated the sensor with an impulse. The response of the sensor to the impulse was once again passed to a computer which converted the data to the frequency domain using the Fast Fourier Transform. Computer based solutions, while useful for testing suffer from all of the bench-top limitations listed above.

Some more compact solutions have been presented. [1], replaces the computer with a commercial digital signal processor. However, a number of external amplifiers and other components are still required for this system. [35] discusses fully on-chip system but gives very few details as to the implementation. From the details that are given, it appears that only the impedance magnitude is measured and not the phase. While amplitude alone may be useful for some systems, in general, information is lost without the full complex response of the sensor. Thus no fully on-chip system that measures the full complex response of the sensor has been found.

None of the preceding systems are suitable for high density senor arrays. Too much bandwidth would be required to transmit all the raw information for processing by a computer. The more compact systems, once multiplied by many sensors would become too large for economical use. [36] is an on-chip sensor array system, however it only has programmable amplifiers, and no IS is actually done.

On-Chip IS is a very new field. No published research could be found which presented a fully on-chip system capable of computing complete impedance data.

B. Goals of This Research

No known fully on-chip IS system currently exists, despite the many applications which need this technology. Thus, the primary goal of this research is to begin meeting the needs of the many new IS applications being proposed, by providing a fully on-chip IS system.

The goal is to develop an IS system that is not only fully integrated on an IC, but sufficiently compact to allow the system to support high density sensor arrays on a single IC.

Due to the lack of published research in this area, very little is known about the issues or requirements of on-chip IS. Some of the requirements of an on-chip IS system can be derived from the application research, but much is unknown about how best to build these systems. Also, there are a number of methods for implementing IS measurements (some are discussed in chapter 2). Beyond developing an IS system, this research also attempts to explore the possible solution space and identify which parameters are important and which solutions are practically realizable.

C. Requirements of On-Chip Applications

Even when building a general baseline test system, some specifications are needed. A specific target application must be selected and requirements drawn from this. This project targets measuring the IS of chemiresistors (CR). The exact equivalent circuit for the system is not yet known, but a parallel RC circuit, like that shown in Figure 1(a) is assumed, with component values around 1MΩ and 40pF.

Drawing from this target, some specifications can be established. Depending on the exact component values, the sensor's break frequency is around 4kHz. To allow for a good interrogation range then, the system should be able to cover 100Hz – 10kHz, or a similar 2 decade range. It is typical that these systems exhibit large base resistances around 100kΩ to 10MΩ and can not be interrogated with voltages above 1V. This translates into small total currents on the order of 100nA. The actual sensor response may represent only a fraction of the base value. This system will target currents in the nano-amp range.

As noted earlier, many of the applications of IS require the use of high density sensor

arrays. This also raises some unique requirements. The first requirement, which has already been discussed, is that off-chip bandwidth is limited, so all of the sensor's responses must be processed to a sufficient extent that they can be easily transmitted off of the chip. Secondly, if hundreds of sensors are all multiplexed down to one interface circuit, leakage current becomes a serious issue, as each channel of the multiplexer will leak into the output. Thus, with the small sensor signals expected in this project it is not possible to multiplex hundreds of sensors down to one interface. Instead, the IS interface, or at least the front end, needs to be small enough so that it can be instantiated many times on the die.

Chapter 2: Design Methodology

I. Possible Solutions

A. Frequency Response Analyzer

The Frequency Response Analyzer (FRA) is a common method for making IS measurements [37]. For instance, it is used for cell sorting in [17]. In this system, the sensor is stimulated with a single sine wave (See Figure 5 below). The output of the sensor is then multiplied by the same sine wave as well as a cosine wave of the same magnitude. The DC value of the multiplier output caries the sensor response, so it is then passed into a low pass filter. (Typically an integrator is used because it has a cutoff frequency at 0 Hz.) After filtering, the two outputs are proportional to the Real and Imaginary portions of the sensor's response. After the measurement is completed, a new measurement can be taken at the next frequency. The advantage of this system is that it is simple, which offers many hardware optimizations, such as implementing it in the analog domain.

The disadvantage of this system is that it is slow. It can only measure one frequency at a time and for each measurement the integrator must be given enough time to reach an accurate value. Because the integration time is a function of the signal period (1/f) the loss in speed is significant at the lower frequencies.

B. Fast Fourier Transform

A second method commonly used is based on the Fast Fourier Transform (FFT) [38], [39]. It has been used for instance in cell [18] and tissue [12] testing. This addresses the speed restrictions of the FRA method. Instead of measuring a range of discrete frequencies the sensor is stimulated with a wide-band signal, such as an impulse. The response of the sensor is digitized and transformed to the frequency domain using the FFT algorithm. This

provides a speed boost because there is no integrator and all frequencies are measured at once. The process is illustrated in Figure 4.

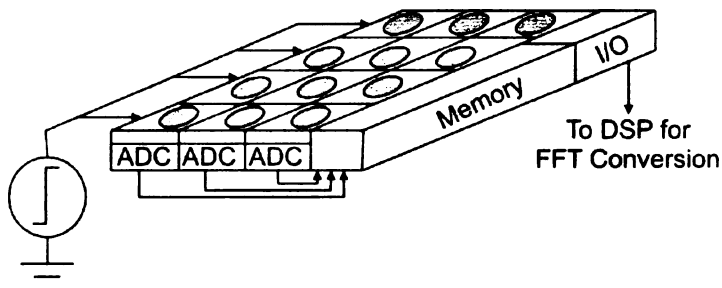

Figure 4: System illustration of the FFT approach to IS for arrays. Each cell requires its own ADC if the sensors are to be monitored simultaneously.

The disadvantage of this system is that it makes many size and power trade offs in order to accomplish its speed goals. All components in this system are digital, which requires more area and power. This system requires a much faster ADC than the FRA because it must capture high frequency data. After the data is digitized, it needs to be processed using the FFT. If it is to be processed on-chip, a DSP unit will need to be included which would consume a lot of space. If the data is to be processed off chip, a very large amount of data would need to be transferred off chip. In either case with a high density array of sensors, a large amount of memory would be required to store the data until it could be processed or transmitted.

As an example of the hardware requirements, [40] presents the design of an 128 cell sensor array, where each cell has an ADC and shift register. However, the ADC on this chip is too slow for a FFT system. This design already requires a large chip (6.4mm x 4.5mm), adding a faster ADC and larger shift registers would make the chip area even larger yet.

C. Other Methods

The two solutions mentioned above are the most commonly used IS systems. Sometimes

variations on these ideas are employed. For instance, there has been some work done to eliminate the integrator in the FRA solution by changing the algorithm [41].

Also, in some cases, when only the magnitude information is needed, very simple resistance or current readout circuits can be used [35]. This is acceptable for some applications, however the phase information is lost in this approach. Thus this approach is not acceptable for general IS.

D. The Best Solution

Chemiresistor systems do not usually change rapidly, as applying vapors and removing them takes some time. This means that speed is not a crucial restriction, instead area and power are the critical restrictions. So, the FFT solution becomes a poor option because it is very expensive in terms of area. The simplicity of the FRA solution now becomes very important.

The FRA solution has excellent potential for miniaturization. The two key components in this system are the multiplier and integrator. Both of these can be implemented in the analog domain, reducing the space and power requirements of the system. Also, because the integrator removes all harmonics from the DC signal, the multiplier used does not need to be very accurate, again allowing for further miniaturization.

For this project then, the FRA solution seemed the best choice. The multiplier and integrator can be bundled in a tight cell that can be instantiated many times. After integration, the output of the system is sufficiently large that it can be multiplexed. Also the output is a DC value which is then easily digitized and processed.

A more detailed comparison of the FRA, FFT, and some other approaches is presented in [33].

II. Approach

A. System Level Design

The system level design is shown in Figure 5. This system works using a dual phase variable frequency signal generator. The sine wave (as a voltage) is used to stimulate the sensor. The sensor's response (as a current) is then multiplied by the original sine and the cosine. The result of the multiplication is as follows:

$$[A\sin(\omega t+\phi)+C]\times B\sin(\omega t)=\frac{AB}{2}[\cos(\phi)-\cos(2\omega t+\phi)]+BC\sin(\omega t) \quad (1)$$

$$[A\sin(\omega t+\phi)+C]\times B\cos(\omega t)=\frac{AB}{2}[\sin(\phi)+\sin(2\omega t+\phi)]+BC\cos(\omega t) \quad (2)$$

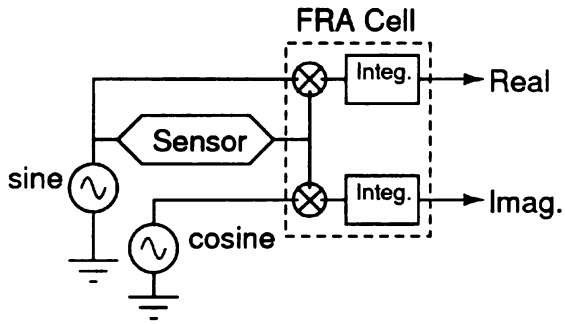

Figure 5: System level schematic.

Where A is the amplitude of the sensor response, ω is the frequency of the signal generator, ϕ is the sensor phase shift, C is the DC offset of the sensor (this is introduced by the system, see "Current Mirror" below), and B is the magnitude of the stimulus signal. The DC portion of the resulting equations represents the Real and Imaginary response of the sensors. The AC portion of this system must be eliminated. To accomplish this, a low pass filter could be used, however for a low frequency stimulus, the filter must have a sharp cutoff, or a portion of the AC response will be included. In this case an integrator, which has a cutoff at 0Hz, provides a better filter.

B. Matlab Simulations

After the system level design was complete, Matlab simulations were made to test the proposed system. For this system, the equivalent network shown in Figure 1(b) was used. The Matlab code calculated the response of the sensor to stimulus, multiplied that response by the correct sine waves and then applied a low pass filter to the result. Finally, it provided plots of key intermediate and final results.

i. Matlab Code

The source code for each of these scripts is shown in the appendix. They are explained briefly here.

- eis3.m – This is the main application, it allows the initial values to be set such as frequency range and sensor parameters.
- lbm_sensor.m – This generates the transfer function for the sensor network.
- gen_step.m – The calculations are done in steps, this sets up the necessary frequency, time, and signal arrays for the current step.
- eis_system.m – This does the actual multiplication and filtering of the signal.
- makePlots.m – This adds the current calculation step results to the final plot.

ii. Lessons Learned

A number of conclusions and lessons were drawn from the Matlab simulations. The first was that a simple chirp would not work for stimulating the system. It had originally been suggested that a signal that had a linearly increasing frequency would provide a good stimulus for the system. However, simulation results showed that because of the capacitance in the sensor, each frequency needed to be held for a short time to allow transient responses to settle out of the system. The simulations also showed that the necessary model parameters, representing the sensor response, could be computed from the

Nyquist plot. This can be seen in Figure 3.

The Matlab design used 1st and 2nd order low pass filters (LPF) instead of integrators to test the cut-off requirements on the system. It was found that the cut-off frequency of the filter needed to be at least a decade less than the minimum frequency being measured. It should be smaller yet for accurate measurements. The capacitance required to make a filter with a cut off less than 10 Hz was too large for the size restrictions of this system. Given a 1MΩ resistance, a first order filter would require 16nF capacitor, which would be much too large. An active filter is a possibility, but would still be difficult to design at such a low frequency. Also, the LPFs were also not significantly faster than the integrator.

C. Circuit Design

After the Matlab simulations were complete, each component had to be designed and tested. Then each component was laid out and integrated together. These steps will be discussed in the next chapter.

III. Challenges

Keeping the size small was the foremost challenge of this design. Most decisions were made with this as the primary consideration. Because this design was implemented entirely in the analog domain, accuracy was also a challenge. As will be discussed later, the accuracy of the system pivots on the integrator. After size and accuracy, it was also important to keep the power consumption low. Many applications would benefit from systems that could be battery powered. Since this system would be instantiated many times (once for every sensor) on a single chip, each IS cell needed to consume very little power in order to keep the whole system power low.

Chapter 3: Circuit Implementation

I. Analog Components

This project uses analog signal processing to achieve a compact low power design. In fact each IS cell is fully analog. The components that make up each cell will be discussed here. The digital control circuitry will be discussed in the next section.

A. Multiplier

i. Design

The multiplier has only a few requirements. It must accept one voltage input and one current input. The current will be single ended, but the voltage may be differential. The output must be a single ended current. Linearity requirements will be discussed later.

There are a number of analog multiplier circuits to choose from. The standard Gilbert multiplier uses at least six transistors [42]. A standard reference on analog multipliers, [43], recommends an eight transistor design. However, there are a couple of opportunities to optimize this design, so that much less area is needed.

The input currents are expected to be very small - small enough to allow operations in the sub-threshold (or weak inversion) region, this is the first opportunity for optimization. Two advantages are gained by making use of the sub-threshold region. The first advantage is of course that this allows operation at very low power levels. Second, in this region, the drain current is related exponentially to the gate voltage. In sub-threshold saturation, the drain current equation is

$$I_{sd} = I_S \frac{W}{L} \exp\left[\frac{V_S - \kappa V_G}{U_T}\right] \approx I_S \frac{W}{L} \exp\left[\frac{\kappa V_{SG}}{U_T}\right] \quad (3)$$

for a pMOS device. Thus the transconductance becomes

$$g_m = \frac{\partial i_D}{\partial v_{SG}} = I_S \frac{W}{L} \frac{\kappa}{U_T} \exp\left[\frac{\kappa V_{SG}}{U_T}\right] = \frac{\kappa}{U_T} I_d \quad (4)$$

Thus g_m is proportional to I_{ds}. This makes voltage-current multiplication very easy.

The second opportunity to be exploited is that only the DC output of this multiplier is important. This means that any harmonics that the multiplier may add to the signal can be easily ignored. Thus, the design does not require a high linearity multiplier. The final opportunity to be used here is that only a two quadrant multiplier is needed. To start with, both input signals are sine waves with no DC offset, which would require a four quadrant multiplier, but by adding a DC offset to the input current this restriction can be lifted. This same DC offset will come in handy for the current mirror later on.

Given the above requirements and opportunities a very compact multiplier was designed. This multiplier uses only 5 transistors. It is shown in Figure 6 below.

ii. Circuit

In the multiplier (Figure 6), M2 and M3 are biased in the sub-threshold region by current from M1 and I_{in}. Because of this, the g_m of both is proportional to the bias current. Thus I_{d2} and I_{d3} (the drain currents from M2 and M3) are proportional to I_{in} times $V_{in+/-}$, making multiplication inherent to the structure. The bias current provided by M1 is not strictly necessary, because I_{in} has its own DC offset that can act as a bias current; however, M1 insures that a small bias current is always present. M4 and M5 convert the differential currents coming out of M2 and M3 into the single ended current, I_{out}.

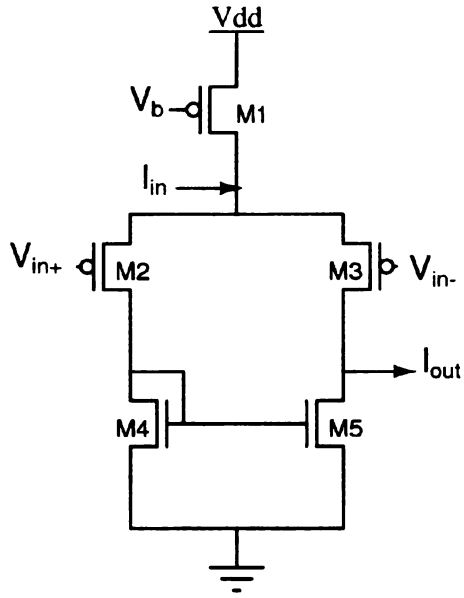

Figure 6: Multiplier schematic

The mathematical derivation for this multiplier is as follows: The sub-threshold drain current relationship:

$$I_{sd} = I_S \left(\frac{W}{L}\right) e^{\frac{V_s - \kappa V_g}{kT}} = I_S \left(\frac{W}{L}\right) e^{\frac{V_s - \kappa V_g}{U_T}} \quad (5)$$

Assuming that M2 and M3 are identical, the ratio of their currents becomes:

$$\frac{I_{sd2}}{I_{sd3}} = e^{\frac{-\kappa V_{id}}{U_T}} \quad (6)$$

Where V_{id} is the difference of V_{in+} and V_{in-}. The bias current is

$$I_{tail} = I_{sd2} + I_{sd3} \quad (7)$$

Dividing this by both I_{sd2} and I_{sd3} then applying equation 6 gives:

$$\frac{I_{tail}}{I_{sd2}} = 1 + e^{\frac{\kappa V_{id}}{U_T}} \qquad \frac{I_{tail}}{I_{sd3}} = e^{\frac{-\kappa V_{id}}{U_T}} + 1 \quad (8)$$

Solving equations 8 for the drain current and taking the difference (which is I_{out}) gives:

$$I_{sd2} - I_{sd3} = \frac{I_{tail}}{1 + e^{\frac{\kappa V_{id}}{U_T}}} - \frac{I_{tail}}{1 + e^{\frac{-\kappa V_{id}}{U_T}}} = I_{tail} \tanh\left(\frac{-\kappa V_{id}}{2U_T}\right) = I_{out} \quad (9)$$

For small values of x, tanh(x) is approximately equal to x. Thus,

$$I_{out} \approx \frac{-\kappa}{2U_T} V_{id} \times I_{tail} \quad (10)$$

iii. Layout

The final multiplier layout was extremely compact. It is shown in Figure 7. M2 and M3 are placed close together and exactly symmetrical in an attempt to achieve good matching.

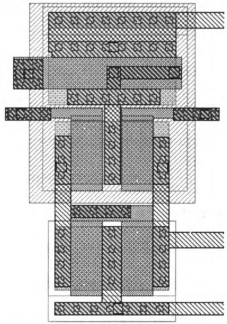

Figure 7: Multiplier Layout. The multiplier dimensions are 16μm x 30μm.

iv. Testing and Performance

Simulations show approximately 30dB linearity in general. When the DC current exceeds AC current magnitude by more than 95%, linearities of 45 to 50dB could be achieved in simulation.

B. Integrator

i. Design

The integrator is the critical component in this design for two reasons. First, it is by far

the largest component present, and size is important in this design. Second, the accuracy of the entire system hinges on the integrator. Accuracy is critical not only because the integrator must remove any harmonics from the multiplier, but also because the integrator is taking in a very small current and building it into a larger current. Size and accuracy become competing restrictions as larger integrators are more accurate.

The generic integrator solution uses a capacitor in the feedback of an op-amp. The op-amp would have to be small due to the overall size restrictions of the entire SI system, and thus would exhibit many non-idealites. The capacitor also would have to be small. This would lead to large voltages on the capacitor. The voltage problem is aggravated by the fact that it may be necessary to integrate over multiple cycles. This long integration time could make the charge on the capacitor even larger.

This system needed a compact integrator with a very large range. The chosen solution was to use a switched current integrator [44], built from two current mode sample and hold (S/H) cells. Switched current circuits enable a very wide range of operation; however they suffer from charge injection errors. These errors are particularly challenging at low current levels. However, [45] proposes a switched current S/H cell that is very accurate even at low currents. This paper claims accuracy better than 0.1% for currents above the 10pA range. The currents in this application are in the nano-amp range so this circuit should be well suited to this application. Beginning with the S/H cell from [45] a full integrator was designed.

ii. Circuit

The schematic for the integrator is show in Figure 8. The operation when I_{in} averages positive is as follows:

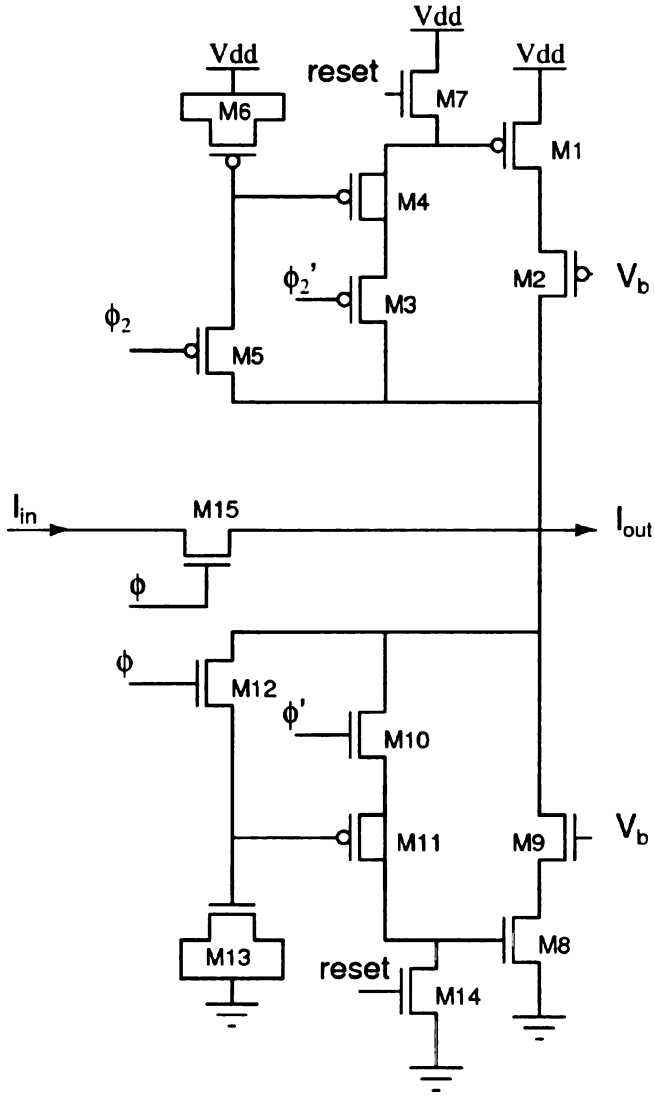

Figure 8: Switched current integrator schematic

1. ϕ and ϕ' are high, ϕ_2 and ϕ_2' are also high
   - M8 is now diode connected and sinks the sum of the current from I_{in} and M1.
   - The capacitance on the gate of M8 is charged to the voltage necessary to hold this current constant.
2. ϕ' goes low then ϕ goes low

- These steps are discussed in [45]. Their purpose is to cancel charge injection from M10 and M12 by dividing it between M11, M13, and the gate of M8.
- With both M10 and M12 are off, M8 continues to sink a constant current, because of the voltage stored on its gate.
- Essentially M8 has stored the sum of I_{in} and the previous sample.

3. ϕ_2 and ϕ_2' go low
   - Now M1 is diode connected and it copies the current stored on M8.
   - Note also that M15 is off, so only the current from M8 is sampled.
4. ϕ_2' goes high, then ϕ_2 goes high
   - The current sum from M8 is now held on M1.
   - This cumulative sum will be added to the next sample from I_{in}.

If the average of I_{in} is negative, the roles of the upper and lower memory cells must be reversed. This is accomplished by clocking M15 with ϕ_2 instead of ϕ.

The cycle above is continued over the integration time, with the sum stored in M1 as the integral of the input. When integration is complete, I_{out} must be read. The process for reading I_{out} is as follows:

1. M15 is turned off to block I_{in}.
2. ϕ_2 and ϕ_2' are held high so M1 continues to store the integral.
3. M14 is turned on, ϕ and ϕ' go low, so that M8 will not pull any current.
4. I_{out} is now equal to the integral and can then be read.
5. After a readout is made, the system can be reset to zero using M7 and M14.

iii. Layout

The layout is shown with the multiplier attached in Figure 9. The design of this

integrator makes heavy use of MOS capacitances, that is why many of the transistors are very large. The optimal size for these transistors is difficult to gage. Sizing information given in [45] does not correlate with simulation data. It may be that the Cadence simulations do not model charge injection well. This disagreement made sizing difficult, but the final sizes chosen were a compromise between information in [45] and simulation results.

The spacing between the S/H cells and between the integrator and multiplier are set to allow exactly enough room for signal routing and for the current mirror.

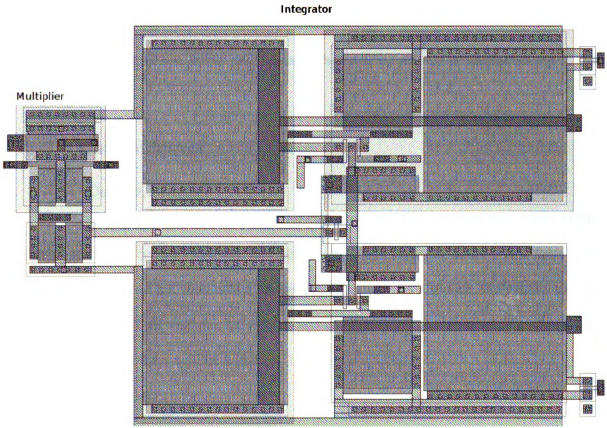

Figure 9: Integrator with multiplier attached. The integrator dimensions are 81μm x 70μm.

iv. Design Challenges

As mentioned above there were some challenges with the simulation. The accuracy of

the simulation with regard to charge injection was unknown. Also, initially the simulation results were very wrong. Eventually it was identified that the simulation parameter gmin was too large and needed to be set to 1e-18.

Addressing error was also a challenge. After charge injection, the second source of error was charge leakage. M1 and M8 need to store a constant charge on their gates. The exponential and square relation (depending on region of operation) of gate voltage to drain current exaggerates this problem because a small drift in gate voltage translates into a large change in stored current levels. To address this M1 and M8 were given very large gates. Beyond that the only other solution is to keep the clocking cycles fast enough to limit the change due to leakage.

If the charge injection errors are constant, they will be able to be calibrated out in the final system.

C. Current Mirror

i. Design

The final component of the system is the current mirror which makes two copies of the sensor response current (Shown in Figure 10). The current mirror has three key requirements: it can not load down the sensor or change its response, it must be able to handle an AC current with no DC offset, and the two output currents need to be nearly identical. Each of these will be addressed below.

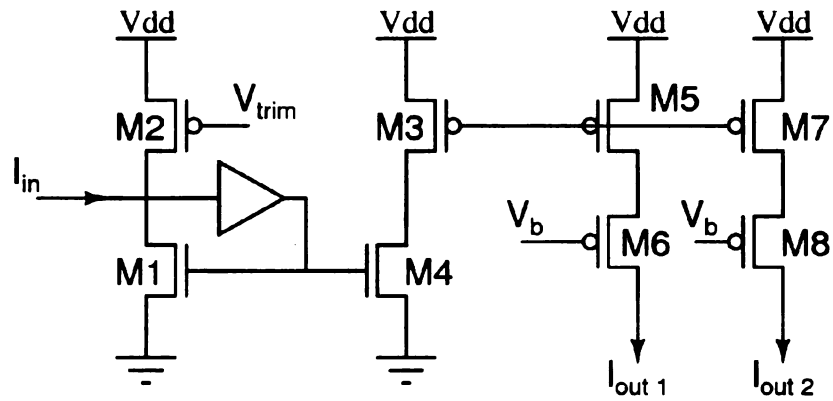

Figure 10: Current mirror. Outputs 2 identical currents with an added DC offset from M2.

The first challenge was caused by the g_m of M1. The sensor providing I_{in}, sees a resistance of $1/g_m$. When the current is small, this value is very large and significantly changes the response of the sensor. Two methods were used to address this. M2 adds a DC current, thus increasing the total current through M1 and increasing g_m. The second and most important step was the addition of the buffer. This increases the value of g_m by the gain of the buffer. Together these reduce $1/g_m$ to a value that is insignificant compared to the sensor resistance.

If the sensor to be interrogated has a series capacitance, as many solution based sensors due, then the sensor output will be a pure AC signal, this leads to the second requirement. M1 is only able to mirror positive currents. The multiplier that comes after the mirror also only accepts positive currents. The solution is to add a DC offset that will prevent the drain current in M1 from ever going negative. This is the primary purpose of M2. V_{trim}, is set elsewhere in the chip to a value that will provide a sufficiently large DC current. This value must be tuned for the sensor that will be measured.

The final challenge is common to most current mirrors. The output currents must match. To accomplish this M6 and M8 were added to guard the drain voltages of M5 and M7. Also, this portion of the mirror was laid out in an attempt to reduce error due to

process variations.

ii. Circuit

The schematic is shown in Figure 10. The operation of this circuit is straightforward. All peculiarities are discussed above.

iii. Layout

The layout is shown in Figure 11. The mirror is laid out long and narrow to allow it to fit tightly between the multipliers of two cells. The gap between M1 and M3 (near I_{in}) is to allow for routing. As noted above M5 and M7 are placed close to each other and are nearly symmetrical to reduce errors due to process variation.

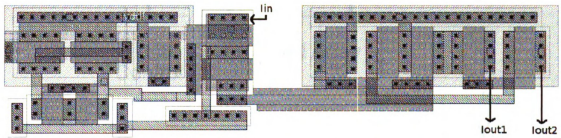

Figure 11: Current mirror layout. The buffer is on the far left, and the two output branches are on the right.

II. Digital Logic

While the heart of the system is all analog, it does need some peripheral digital logic. That logic will be discussed briefly here.

A. Cell Digital Logic

Every cell has three digital control signals: *reset*, *negative*, and *read*. The *reset* signal returns the integrator to its zero state. The *negative* signal controls how input for the integrator is clocked. In other words, it controls whether the integrator can sum positive or negative currents. The *read* signal indicates that the integrator should be placed in read out mode so that the final sum can be read. These three signals are handled by some simple digital logic which enables and disables the appropriate transistors in the integrator based

on these inputs.

B. Chip Control Logic

The chip is designed to have many instances of the IS cell. All of the cells need to be managed and accessible. This is done with a few digital inputs: *Address*, *Negative*, *Read*, and *Set*. The address lines allow each cell to be selected individually. When *Set* goes high the value of *Negative* is latched in for the cell given by *Address*. Also, if *Read* is high that cell will be latched into read mode. (Only one cell can be in read mode at a time.) Finally, to reset the cells a special address must be selected and *Negative* driven high. This will send the reset signal to all the cells.

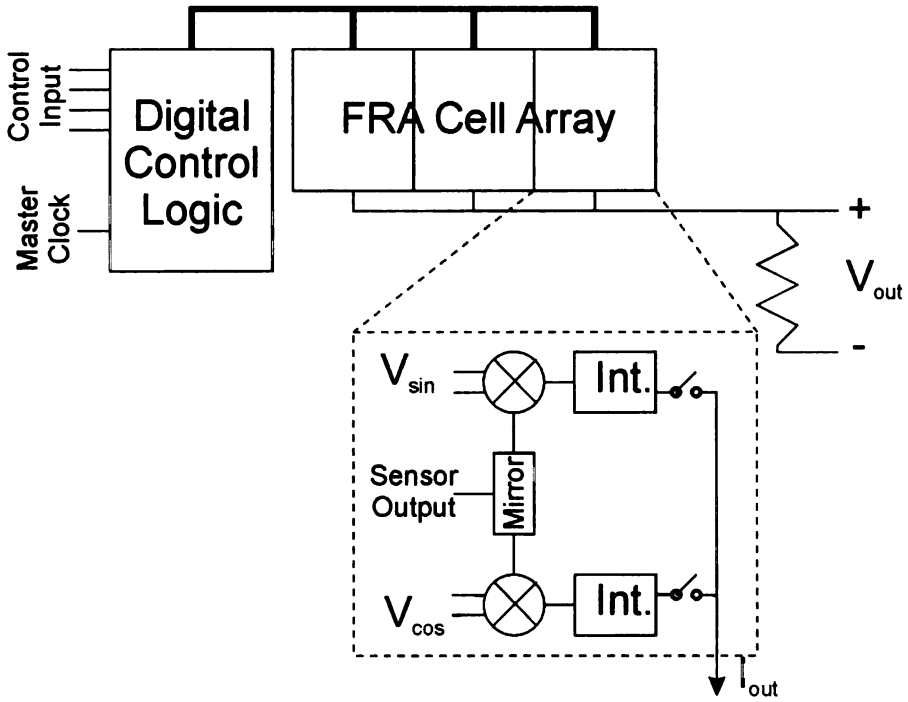

Figure 12: Complete IS array system.

The integrator uses four clocks. All of these are driven from one master clock. The master clock is first divided into two non-overlapping clocks using an inverter ring; these supply the ϕ and ϕ_2 branches. After the inverter ring, the two clocks are fed into unbalanced Schmidt triggers. The Schmidt triggers fire on a high almost immediately, but

have a long delay before coming down, this allows for the small difference in ϕ and ϕ'.

Chapter 4: Test Results

I. Test Setup

After the design and layout was complete, the chip was fabricated and tested. The chip contained a multiplier and integrator configured to allow test points at each critical point. The majority of the testing was performed on these. In addition the chip also included 6 multiplier and integrator pairs setup with all necessary digital logic to enable testing 3 loads simultaneously. The general testing configuration is shown in Figure 13. The external instrumentation will be discussed here, afterward the test of the multiplier, integrator and full system will be discussed.

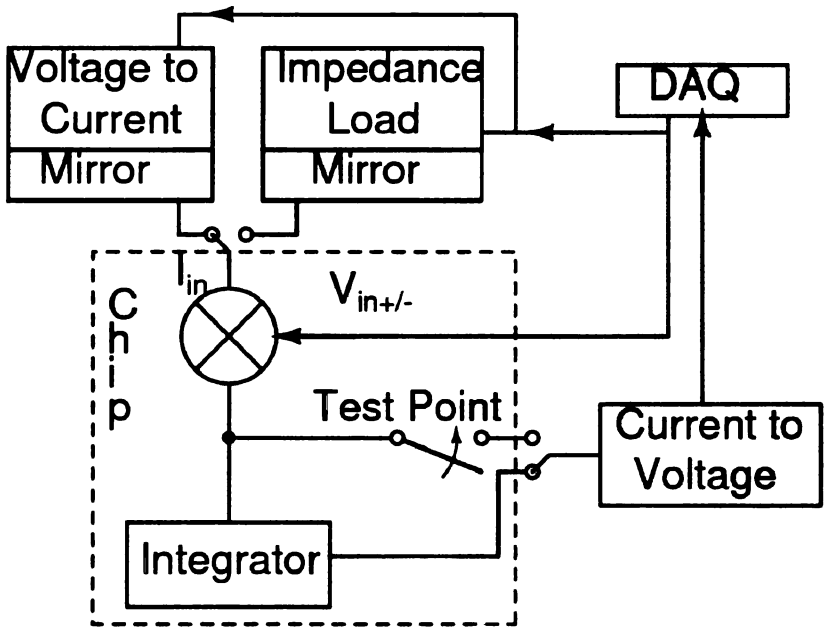

Figure 13: Overview of test setup used.

A. Data Acquisition Card

The Data Acquisition Card (DAQ) was used for all digital and analog signal control. This card only generated and read voltages, so some signals had to be converted to and from currents for testing purposes.

B. Voltage-to-Current Converter

For initial testing of the system, a current generator was needed capable of generating very small currents with low noise. The circuit shown in Figure 14 was developed for this purpose. A very large resistor could have been used by itself, but thermal noise on a resistor is proportional to its resistance. The goal of this circuit was to generate very small currents without the need for large noisy resistors. Also, this circuit provides a low output impedance, which makes interfacing with the multiplier easier.

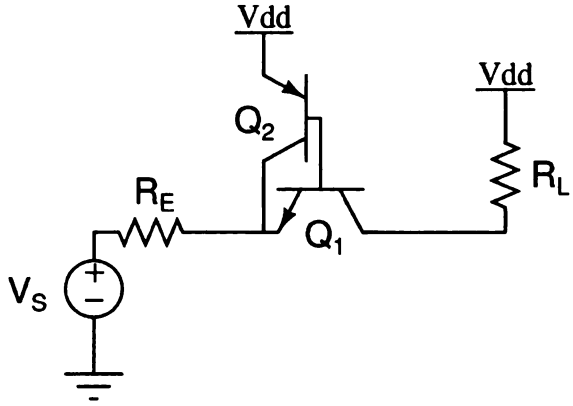

Figure 14: Voltage-to-current converter used to generate very small currents.

This circuit is essentially a common base amplifier, with an additional transistor added. A standard common base amplifier has no current gain. Transistor Q_2, drops the current gain further by providing a portion of the current that R_E requires, thus reducing the output current. The second function of Q_2, is to shift the base voltage of Q_1 down from V_{dd} by about 0.6V. This allows the output voltage an extra 0.6V of swing. The total output current of this generator is then:

$$I_{out} = \frac{\beta_f}{1+2\beta_f}\left[\frac{V_{DD}-(V_{EB}+V_{BE})}{R_E} - \frac{V_S}{R_E}\right] \quad (11)$$

The combination of the scale factor and the offset term allows large voltage inputs to generate small current outputs. Also, the output current is not effected by the output voltage (provided $V_{out} > V_{dd}-1$). An even wider output voltage swing was provided by following this stage with a BJT mirror. The tested output characteristics of this converter are given in Figure 15.

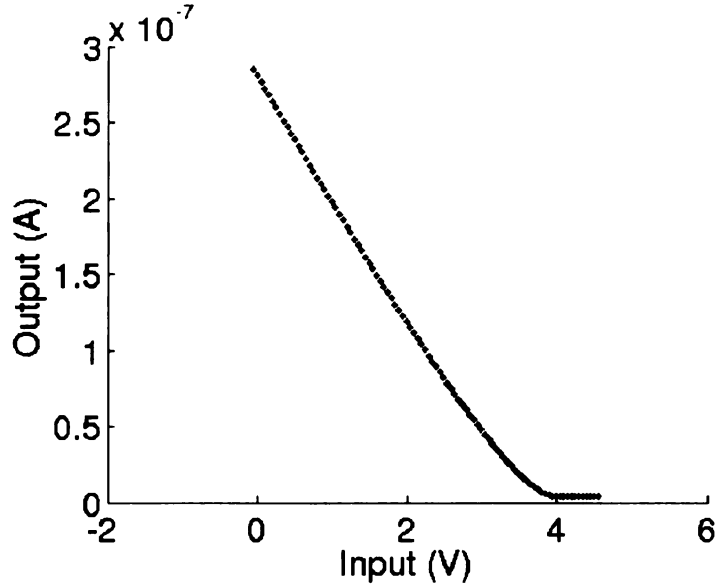

Figure 15: Calibration curve for voltage-to-current converter. Shows that current can be generated between 7nA – 280nA, when R_E is 2MΩ.

C. Impedance Load

Once the system operation was verified, the voltage-to-current converter was replaced with an impedance load. A parallel resistor and capacitor were used for the impedance load. The circuit is shown in Figure 16. In this load, R_S was set to 1MΩ and both 220pF and 100pF were used for C_S. The ideal current response for the 220pF system is shown in Figure 17. For all tests in this system, a voltage is applied to the impedance load and a current is read, so the transfer function for the load is

$$\frac{I_{out}}{V_{in}} = \frac{1+j\omega CR}{R} = \frac{1}{R} + j\omega C \quad (12)$$

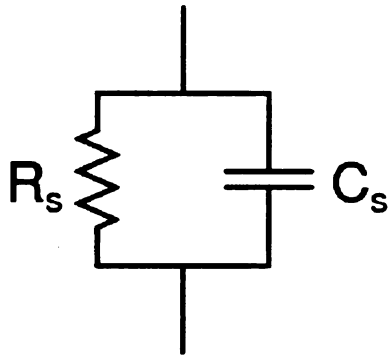

Figure 16: Impedance load used for testing system.

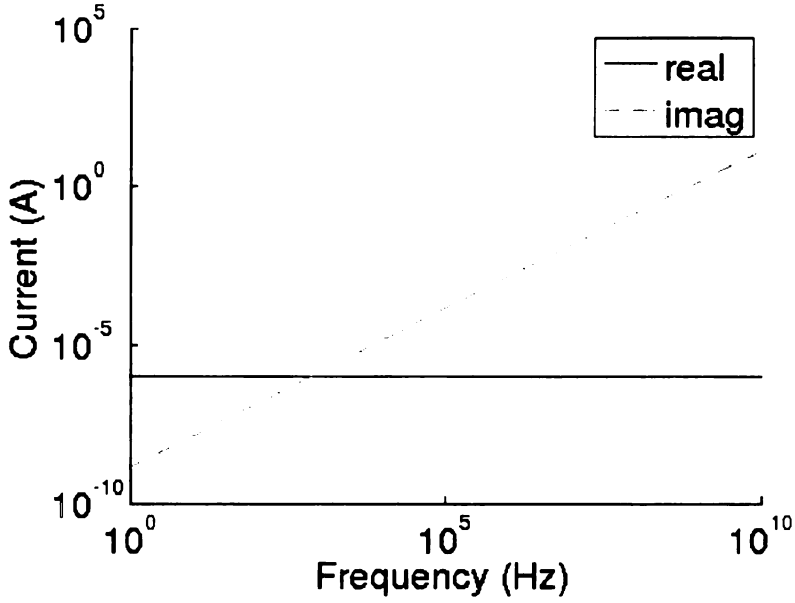

Figure 17: The imaginary and real response of the impedance load is shown, given a 1 volt stimulus. For this simulation R_S = 1MΩ and C_S = 220pF.

This load gives numerous benefits for testing purposes. The real and imaginary responses are very distinct, and can be identified in any small frequency range. Also, the real and imaginary responses are each only dependent on one component so changing component values are clearly seen and identified.

D. Current-To-Voltage Converter

The output of the multiplier and integrator is a current, this must be converted to a voltage so that it can be read with a standard DAQ. For the final system, a resistor was

used to make this conversion, however for initial tests this was not sufficient. A converter was needed with low input impedance (so that the output voltage of the integrator could be kept fixed), high gain and low noise.

To achieve this, a common emitter amplifier was used. The circuit is shown in Figure 18. The output of this is given by

$$V_{out} = V_{DD} - \beta_f R I_{input} \quad (13)$$

This provided two key benefits. First the resistance was effectively multiplied by β_f without significantly increasing the thermal noise. Second, the input voltage is held constant at 0.6V

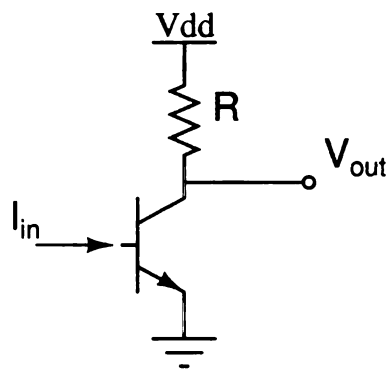

Figure 18: Common emitter amplifier used for high gain current-to-voltage conversion.

E. Other

To further reduce noise in the system, the power supply voltage also had to be filtered. A very simple first order filter was sufficient to achieve this, the circuit is given in Figure 19. Also, a current mirror was needed for the voltage-to-current converter as well as to interface the impedance load to the multiplier input. A very simple BJT mirror was used for this, and is shown in Figure 20.

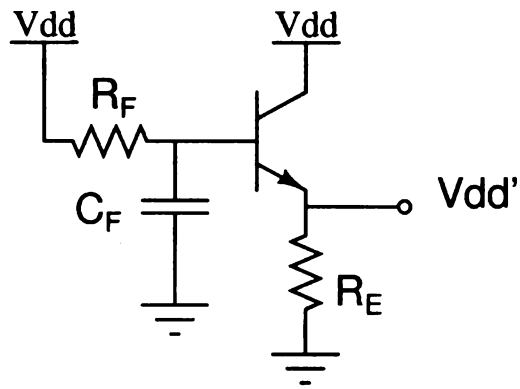

Figure 19: Power supply noise filter.

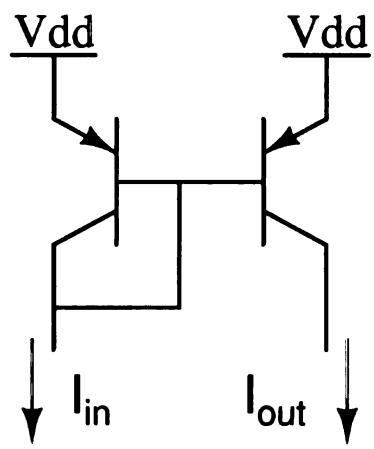

Figure 20: BJT Mirror used throughout the external instrumentation.

II. Multiplier Testing

To test the multiplier alone, an the voltage-to-current converter was used to provide I_{in}. This was driven from the positive portion of the $V_{in+/-}$ input to reduce phase distortion as little as possible. The output of the multiplier was applied to the current-to-voltage converter so that the values could be read by the DAQ. These initial tests showed that the multiplier was indeed outputting a wave form consistent with multiplied signals.

The output of the multiplier was consistent with expectations. An example output is given in Figure 21, when a 100Hz stimulus signal was used. As expected from Equation 1

in Chapter 2, the key frequency components are at DC, 100Hz, and 200Hz. The 200Hz component should have had an equal magnitude to that of the DC component, so clearly the multiplier is not ideal. However, because only the DC value is of interest and there are no significant non-idealities near DC this output is entirely satisfactory.

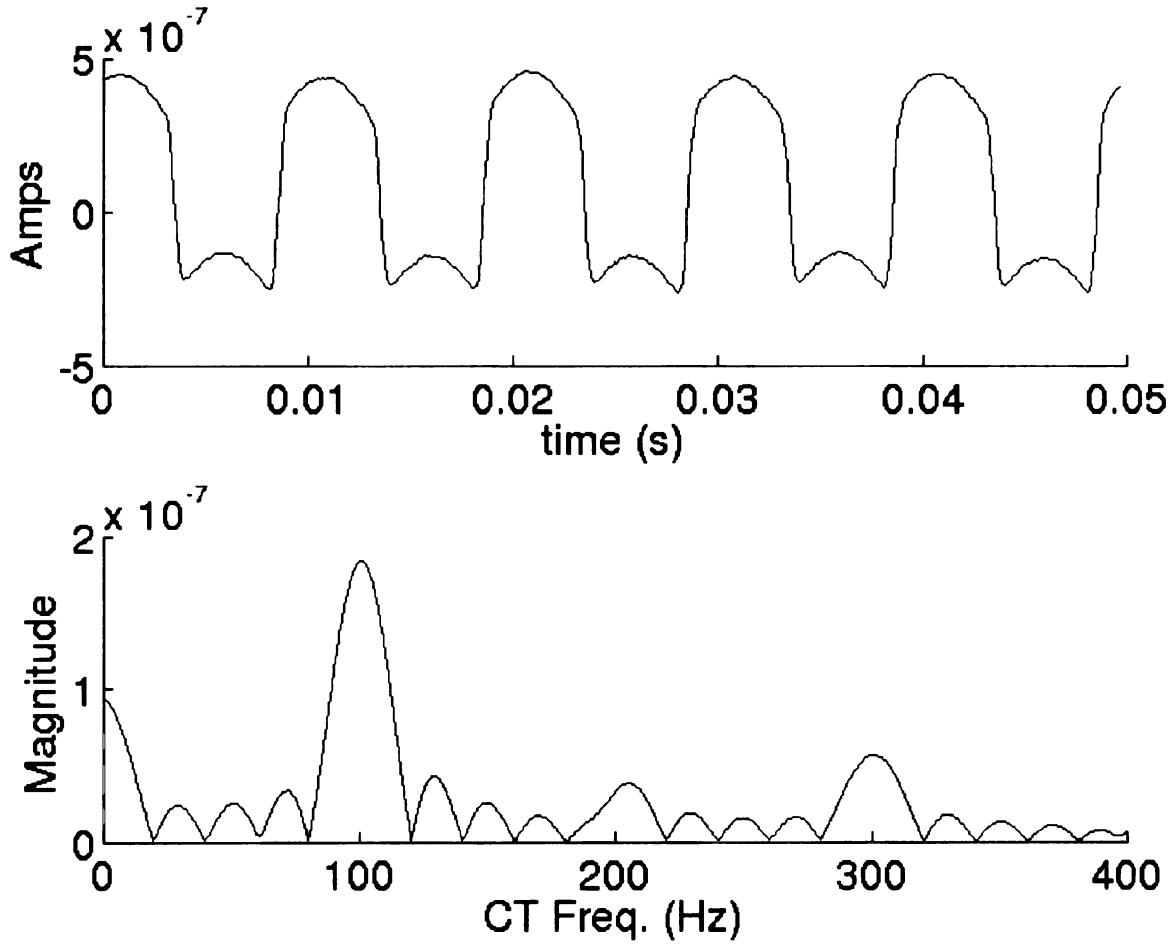

Figure 21: Output of multiplier given two 100Hz sine waves. The time and frequency domain values are shown here.

Once the gross behavior of the multiplier was verified, the voltage-to-current converter was replaced with the impedance load. However, the initial test showed that the voltage at the I_{in} node varies widely, as the current varies. Thus, the impedance load can not be connected directly to the I_{in} node. Also, the internal mirrors described above were not available for use with testing just the multiplier, thus an external BJT mirror was introduced to allow the voltage at I_{in} to vary while the voltage across the load was

controlled only by the stimulus. This does however, validate the need for a well designed input mirror.

The final multiplier test was to sweep the frequency range and record the multiplier response at each frequency point. The multiplier response was then integrated digitally and the DC value computed. This test shows what the response of the system would be given an ideal integrator. The real component response is given in Figure 22. These results are for a single test run. Linear regression shows that the slopes were 52.0pA/Hz and 59.7pA/Hz for the 220pF and 100pF loads respectively. The imaginary component of the response is given in Figure 23. Here the slopes were 187pA/Hz and 104pA/Hz for the 220pF and 100pF loads. In all cases, only data above 300Hz was used for the regression.

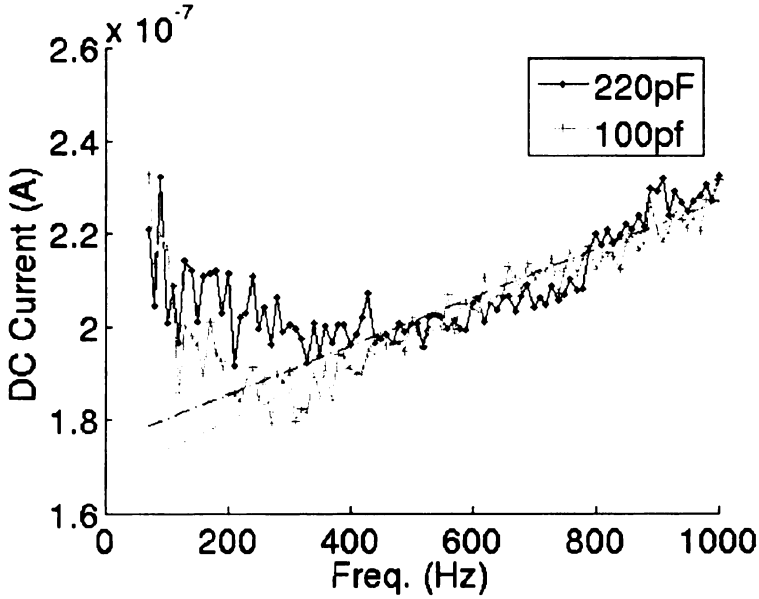

Figure 22: DC value of multiplier output for product of two sine waves across a frequency range. The line slopes are 52.0pA/Hz (220pF) and 59.7pA/Hz (100pF). (The resistive component of the load was held constant at 1MΩ)

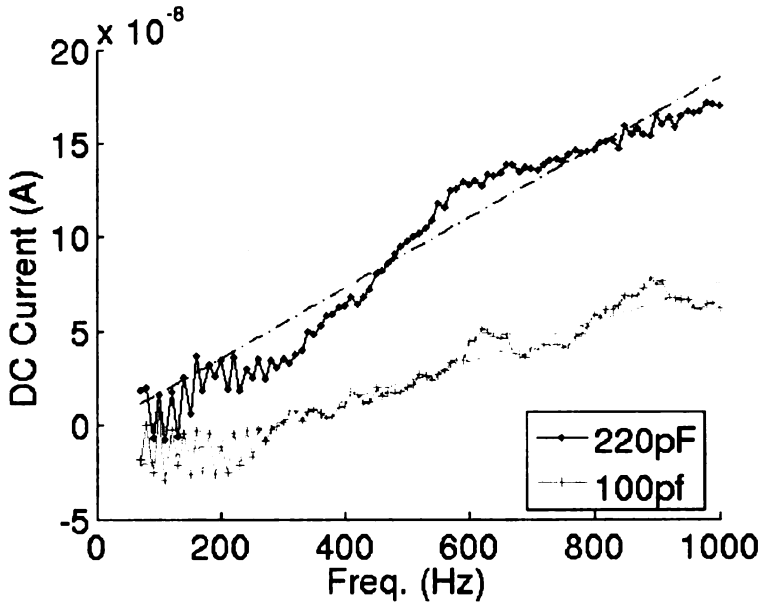

Figure 23: DC value of multiplier output for product of a sine and cosine wave across a frequency range. The line slopes are 187pA/Hz (220pF) and 104pA/Hz (100pF).

These tests show that the system is reading true real and imaginary responses. The imaginary slope reduces by approximately the same factor as the capacitive load, this is as expected from equation 12. The real response did not change with the change in capacitive load, this is also correct. However, the real response was not flat as expected. The small amount of slope that is seen is likely due to parasitic capacitances in the bread board used to assemble the load and in the BJT mirror.

Below 300Hz, there appears to be significant noise. This noise is due in part to 60Hz power line noise. The rest is likely due to flicker noise. The multiplier design was not optimized for noise, so it is reasonable to expect significant noise contributions.

In summary, the operation of the multiplier has been verified. Also, the overall system of multiply and integrate has been shown to produce correct values.

III. Integrator Testing

Integrator testing began with investigating the integrator reset states. It was discovered that the pMOS sample and hold (S/H) was not fully reseting. This is due to the use of an

nMOS reset switch which is unable to pull the node voltage all the way up to V_{dd}. During design, this issue was known, but it was assumed that the pMOS stage did not need a complete reset. Testing showed this assumption was not correct. So, an alternative reset method was developed. Initially both pMOS and nMOS networks are set to reset mode and the integrator input gate is turned off. Then the pMOS network is taken out of reset and cycled through a single sample cycle. Because the input gate is off and the nMOS network is in reset the pMOS network samples and stores approximately 3.8nA, which is sufficiently close to 0A. This method was shown to be effective.

Next the integrator was tested storing a single sample and outputting that sample. This showed that each network needed at least 60μsec to sample a value, and the time to correct errors between ϕ and ϕ' falling should be about half that.

To provide a safety factor, the integrator was set to sample for 100μsec and then have a 50μsec correction time. For every integration cycle, both networks must sample data, so this gave a total sampling time of 300μsec and a sampling rate of 3.33kHz. This means that the integrator can not process signals above 1.66 kHz. The lower frequency limit is set by the number of integration cycles used. All tests shown here used 100 integration cycles. Using 100 cycles, only a single period would be integrated for a 33.3 Hz signal. This then is the lowest frequency which can be integrated.

It was also found that in hold mode, the value stored in the pMOS network would grow at a rate of 269nA/s. This represents the charge leakage from the gate capacitance of the hold transistor. This and charge injection at switching, compose the key components of error in the integrator. Provided these errors are constant, they can be removed by calibration, however further tests showed a significant random variation in these errors.

The final test was to integrate sine waves of varying DC offset. For each DC offset sine waves of 5 or more different amplitudes were integrated. The averaged output in Figure 24, shows that the DC level was detected and the integration slope is nearly a linearly related to the DC offset. It was necessary to use two ranges of the voltage-to-current converter to cover the complete test range. The difference in current converters, is likely the key cause for the right shift of the 'High Range curve.' However, the right shift is also due in-part to the random error introduced by the integrator.

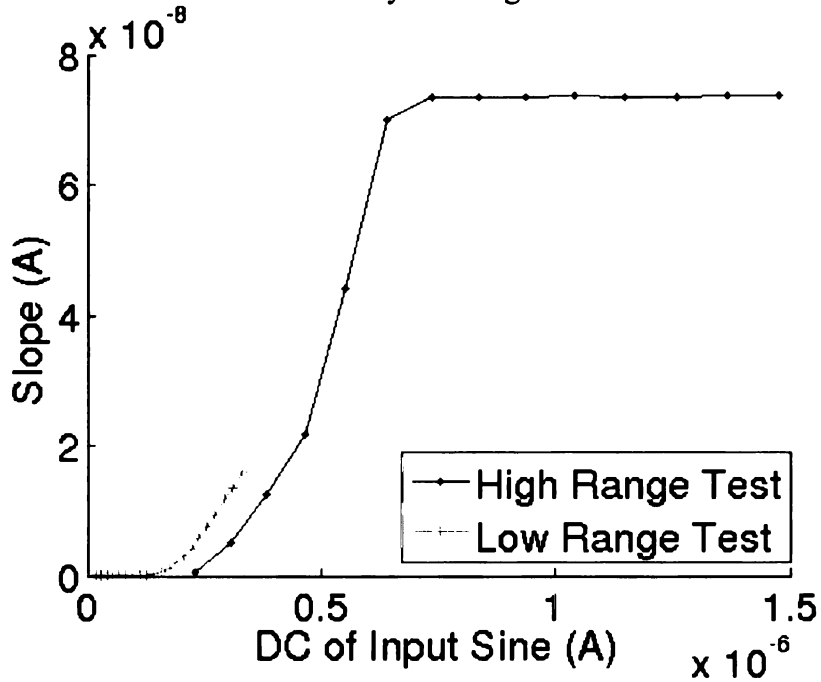

Figure 24: Results for integrating sine waves of varying DC offsets. This shows that the DC offset detection is nearly linear. The right shift of the 'High Range' curve is due in part to the use of a different current generator.

The lower saturation level in Figure 24 is due to charge injection errors. For input currents less than 170nA, the charge injection errors swamp out the signal and only internal errors are integrated. The upper limit is not inherently due to the integrator, but is due instead to the current-to-voltage conversion. When the voltage at the output node comes within 0.4V of V_{dd}, the pMOS network switches off. For the high range a 500kΩ resistor was used for current-to-voltage conversion, thus when the currents became large the

voltage approached V_{dd} and shut the integrator off. This causes a trade-off in current-to-voltage conversion, as a large resistance is required to accurately read small currents, but a large resistance lowers the total possible output current.

Within, each DC level, the standard deviation of the measurement set was computed, with respect to total output current. Within the linear portion of the high range, the standard deviation averages about 270nA. In the low range, standard deviation steadily decreases down to 21nA. However, the output current does not exceed 3 standard deviations, until the output slope is greater than 2nA, which is an input current of 200nA. Thus, below this point noise significantly dominates the signal.

In summary, it was shown that the integrator did function correctly. It has a frequency input range of 33.3 Hz to 1.66kHz. Within that range it can integrate signals with DC levels above 170nA, but the output error requires inputs to be above 200nA. The upper limit on currents is determined by the current-to-voltage conversion used. Either a dual range conversion is needed or some low input impedance converter needs to be used.

IV. Full Impedance Measurement

The final test was to connect the multiplier and integrator together and attempt to interrogate an impedance load. The results for the real component computation are shown in Figure 25. The noise below 300Hz that was seen in the multiplier is amplified here. For this reason, all regressions were computed only from data above 300Hz. The slopes are 29.0pA/Hz for the 220pF load and 11.8pA/Hz for the 100pF load. The slopes are about equal, as expected, because the load capacitance has no effect on the real component. They are both slightly above zero, because of parasitic capacitances as described above.

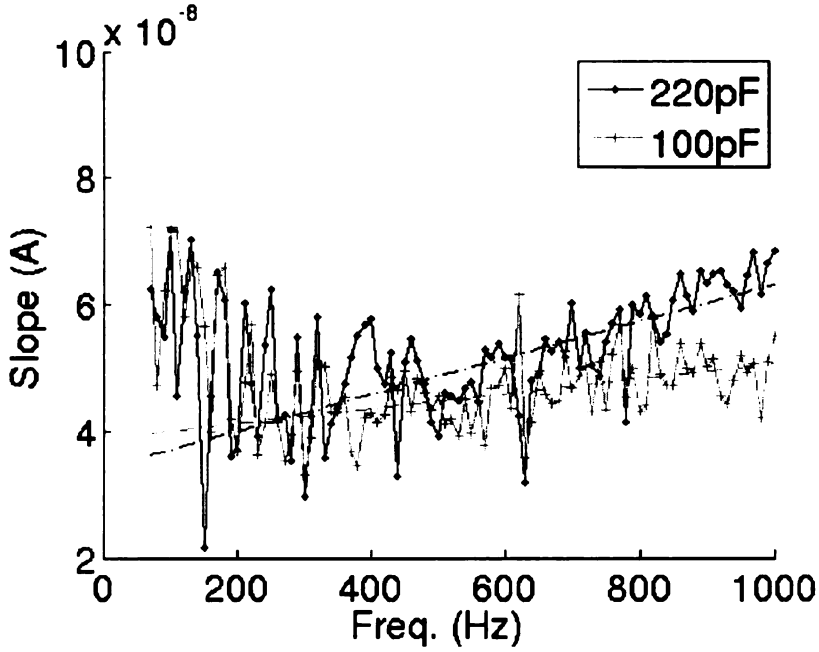

Figure 25: Full system integration showing the real component of the impedance load. As expected, there is little change in real component as capacitance changes. (The resistive component of the load was held constant at 1MΩ)

The output for the imaginary response is shown in Figure 26. The slopes are 45.5pA/Hz for the 220pF and -1.49pA/Hz for the 100pF load. The 220pF load should have a greater slope than the 100pF load, so this is correct. However, the 100pF load should have had a slope closer to 20pA/Hz. The negative slope is caused by the large noise in the system.

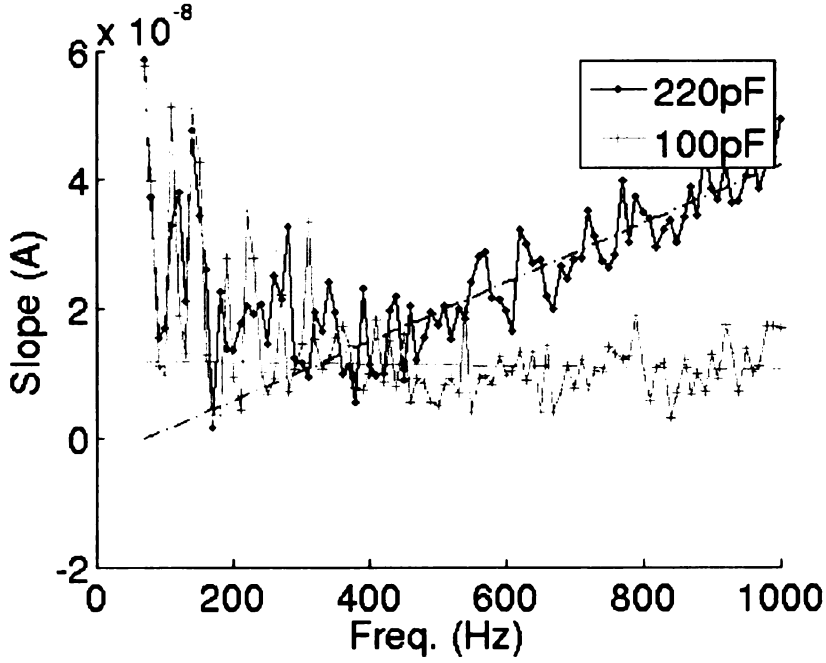

Figure 26: Full system integration showing the imaginary component of the impedance load. As expected the slope decreases as capacitance decreases.

There is significantly more noise in this output than was seen in the digitally integrated multiplier output. Thus the charge injection and leakage of the integrator is adding significant noise. There appears to be more noise here than was seen in the DC integration test in Figure 24 above for two reasons. First, the input amplitudes here are larger than those that could be used for the DC integration test. The second reason is that the sine wave test used large data sets to average out the error.

In the data presented here, 5 measurements were taken and averaged at each point. This reduced the noise to a level that allowed these trends to be seen. More measurements and averaging should reduce the noise more, but would require significant time to perform, and thus would not be practical in an a usable system.

In summary, the system is functioning, but the excessive noise in the integrator makes it poorly suited to application other than detection (where it could detect a change in impedance, but likely not be able quantify the change.) An integrator with less noise is

required to make this system into a reliable IS measurement platform. Alternative integrators are discussed in Chapter 5.

V. Other Components

The multiplier tests above demonstrated the need for a current mirror to isolate the impedance load from the multiplier. However, the mirror was only fabricated in the full array system and due to the change in integrator reset methodology, the full array system could not be tested.

Likewise, the digital logic, was not well tested because it was only included in the full system. Some basic tests were run to show that the digital logic was operational, but a full test was not possible.

Chapter 5: Conclusions and Future Work

I. Final Specifications

The fully integrated mirco-IS system was developed with these specifications:

- Size: 205 μm x 108 μm (For 2 integrators, 2 multipliers, a mirror, and signal routing capable of computing real and imaginary sensor response in parallel.)
- Frequency range: 33.3 Hz – 1.66 kHz (although noise limited measurements to 300Hz – 1.66 kHz)
- Detection level: Very low in this generation. Was capable of detecting a 120pF change in impedance load.

II. Contributions

This thesis provides significant contributions to the field of micro-impedance spectroscopy. Specifically, it presents the following:

(1) The first known fully on-chip IS system was demonstrated. This work provides an IS measurement system which is not only fully integrated on an IC, but sufficiently compact to support high density sensor arrays. This will provide a basis for enabling the many IS applications to deployed in mobile and eventually in vivo systems.

(2) An extremely compact multiplier which is very well suited to this application was also presented. This multiplier design is able to fully exploit the reduced linearity requirements in favor of reduced space requirements. Further, it was experimentally shown that the multiplier did perform correctly and produce good results.

(3) A possible compact integrator was also designed and tested. Testing showed that this type of integrator was not well suited to this application, because of its lack of precision. The key requirements for an integrator were identified as precision, range, and size.

(4) Peripheral components necessary to implement a complete system were also identified. It was shown that an input mirror with very low input impedance is needed for interfacing with the sensor. After the sensor response is computed, a wide ranging current readout is needed for final sensor response output.

III. Future Work

A. Multiplier

The multiplier functioned well, above 300Hz. The current layout was not optimized for noise. Once it is resized for noise performance the lower frequency limitation should be reduced. Also, a better integrator should provide further noise reduction as it would average the multiplier output.

B. Alternative Integrators

The switched current integrator did not provide satisfactory results. While it is very compact and capable of performing integration, its random error is much too large. A different integrator is needed. Two possible options are present here.

i. Log Domain

A log domain integrator is a possible option. A CMOS implementation is shown in Figure 27 [46]. The output of this system is

$$I_{out}=\frac{1}{\tau}\int I_{+in}-I_{-in}dt \qquad \tau=\frac{C}{I_O}\frac{U_T}{I_S\kappa} \quad (14)$$

Because of the sub-threshold logarithmic compression, the internal currents are quite small, and thus power consumption is reduced. This also prevents the capacitor from saturating.

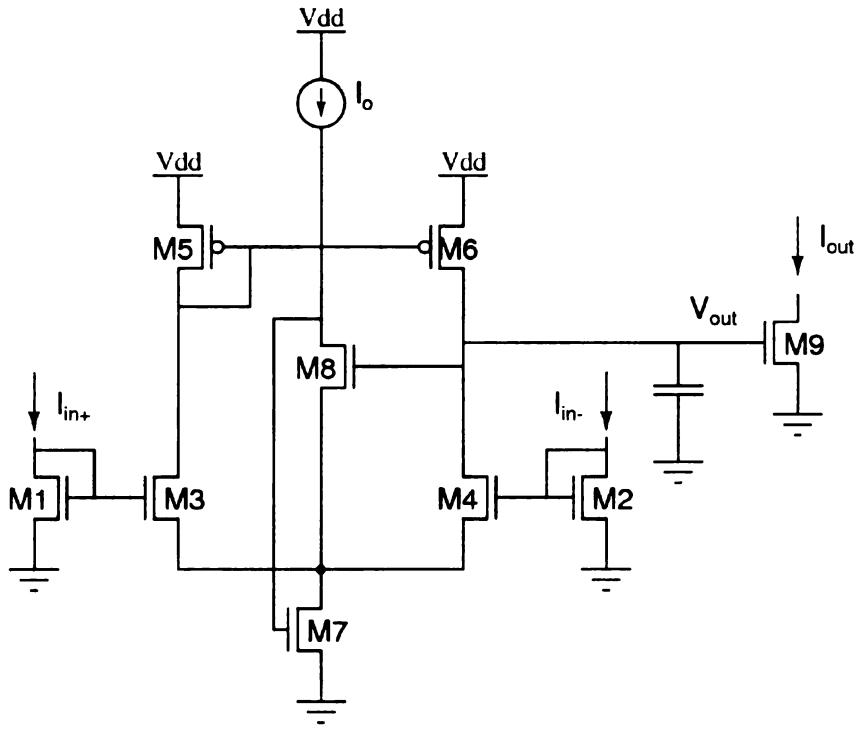

Figure 27: Standard log domain integrator.

The disadvantage of this system is that logarithmic conversions inherently lose precision. Also, this system is very sensitive to component mismatch. Because of the need for good matching, the transistors will all need to be large. With the addition of the capacitor, this integrator will likely be somewhat larger than the current switched current integrator.

ii. Relaxation Oscillator

In the gas sensor domain, it is very common to make a resistance-to-time converter from a relaxation oscillator. A simple resistance-to-time converter is shown in Figure 28. This works by generating a current through the resistive sensor, R_s, and integrating that current in the capacitor. When the capacitor reaches a specific value, the current is reversed and the capacitor is discharged. The value of the resistance is then encoded as the period of the digital output D_{out}. Because a current is being integrated in a capacitor, it should be possible to modify this structure to compute integrals of a sine wave as well. This

approach was first suggested by Chao Yang, a fellow researcher in the IS field.

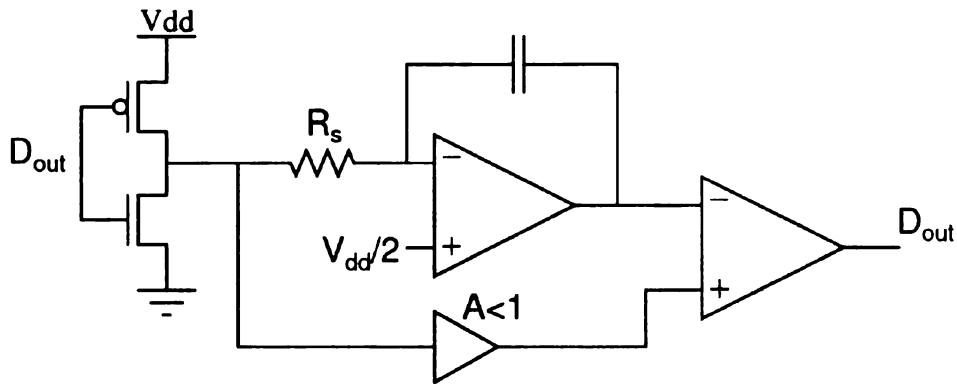

Figure 28: Simple oscillator for resistance to time conversion.

The advantage of this system would be that it would directly provide a digital output. Also, the resolution of the system is simply determined by the speed of a digital counter. The disadvantage of this system is that it would be quite large, as it requires a high gain op-amp and a comparator.

C. On-Chip Current-to-Voltage converter.

The current chip uses a single resistor to convert the output of the integrator to a voltage. If the new integrator outputs a current, then a better current-to-voltage conversion mechanism is needed. For small currents, a large resistance (such as 1MΩ) is needed to generate a sufficiently large voltage for detection. However, when the integrator output becomes large, then a smaller resistance is needed to prevent the total voltage from approaching V_{dd}.

This could be achieved by fabricating two resistors on chip and using a comparator to switch automatically between them. In which case the output would be a voltage and a digital bit indicating the range used. Alternatively a current mode ADC could be placed on the chip as well, but it would have to have a large dynamic range.

Appendix

I. Code Listings

A. eis3.m

This is the main application, it allows initial values to be set such as frequency range and sensor model parameters.

```
%Simple AM demodulation system for EIS
%
%                  Mult          Amp
% /---------------(X)--->[LP filter]->DC value of Sensor
Amplitude response
%(~)-->[Sensor]---/
%Vin      Sen    SOut


%--------------
%General Setup
%--------------

clear
decStart = -2;
decEnd = 10; %6
Rs = 400;
Rm = 1e6;
Cm = 0.5e-6;
Cdl = 5e-6;

%---------------
%Initial Calcs
%---------------

% midDec = (decEnd + decStart) / 2;
% fs = [10^decStart:(10^decStart)/2:10^midDec
10^midDec:(10^midDec)/2:10^decEnd];
fs = logspace(decStart, decEnd, 200);

[Sen, Sens] = lbm_sensor(Rs, Rm, Cm, Cdl, fs);

figure(1);
subplot(2,1,1); loglog(fs, abs(Sens)); title('Sensor Bode
Plot');
subplot(2,1,2); semilogx(fs,angle(Sens).*(180/pi));
```

```
title('Sensor Bode Plot - Phase');

time_t = [0];
freq_t = [0];
SenOut_t = [0];
Mult_t = [0];
Sig_t = [0];
SigCos_t = [0];

%-----------------
%Computation loop
%-----------------
for dec=[decStart:decEnd]
    fprintf('\nComputing 1e%i Hz ...', dec);
    [Vin VinCos f t] = gen_step(10^dec);
    %t = t + max(time_t);

    fprintf('Computing...');
    [SenOut Mult Sig SigCos] = eis_system(t, f, Vin,
VinCos, Sen);

    fprintf('Concating ...');
    time_t = horzcat(time_t, t + max(time_t));
    freq_t = horzcat(freq_t, f);
    iend = size(time_t,2);
    SenOut_t = horzcat(SenOut_t, SenOut);
    Mult_t = horzcat(Mult_t,Mult);
    Sig_t = horzcat(Sig_t,Sig);
    SigCos_t = horzcat(SigCos_t,SigCos);

    figure(2);
    makePlots(time_t, freq_t, SenOut_t, Mult_t, Sig_t,
SigCos_t);

    figure(3);
    plot(Sig, SigCos);
    title('Nyquist Plot');xlabel('Real');ylabel('Imag.');
end

fprintf('\nDone\n');
```

B. lbm_sensor.m

This generates the transfer function for the sensor network.

```
%Simple AM demodulation system for EIS
%
%                    Mult            Amp
```

```
% /---------------(X)--->[LP filter]->DC value of Sensor
Amplitude response
%(~)-->[Sensor]---/
%Vin      Sen    SOut


%--------------
%General Setup
%--------------

clear
decStart = -2;
decEnd = 10; %6
Rs = 400;
Rm = 1e6;
Cm = 0.5e-6;
Cdl = 5e-6;

%---------------
%Initial Calcs
%---------------

% midDec = (decEnd + decStart) / 2;
% fs = [10^decStart:(10^decStart)/2:10^midDec
10^midDec:(10^midDec)/2:10^decEnd];
fs = logspace(decStart, decEnd, 200);

[Sen, Sens] = lbm_sensor(Rs, Rm, Cm, Cdl, fs);

figure(1);
subplot(2,1,1); loglog(fs, abs(Sens)); title('Sensor Bode
Plot');
subplot(2,1,2); semilogx(fs,angle(Sens).*(180/pi));
title('Sensor Bode Plot - Phase');

time_t = [0];
freq_t = [0];
SenOut_t = [0];
Mult_t = [0];
Sig_t = [0];
SigCos_t = [0];

%-----------------
%Computation loop
%-----------------
for dec=[decStart:decEnd]
    fprintf('\nComputing 1e%i Hz ...', dec);
```

```
    [Vin VinCos f t] = gen_step(10^dec);
    %t = t + max(time_t);

    fprintf('Computing...');
    [SenOut Mult Sig SigCos] = eis_system(t, f, Vin,
VinCos, Sen);

    fprintf('Concating ...');
    time_t = horzcat(time_t, t + max(time_t));
    freq_t = horzcat(freq_t, f);
    iend = size(time_t,2);
    SenOut_t = horzcat(SenOut_t, SenOut);
    Mult_t = horzcat(Mult_t,Mult);
    Sig_t = horzcat(Sig_t,Sig);
    SigCos_t = horzcat(SigCos_t,SigCos);

    figure(2);
    makePlots(time_t, freq_t, SenOut_t, Mult_t, Sig_t,
SigCos_t);

    figure(3);
    plot(Sig, SigCos);
    title('Nyquist Plot');xlabel('Real');ylabel('Imag.');
end

fprintf('\nDone\n');
```

C. gen_step.m

The calculations are done in steps, this sets up the necessary frequency, time, and signal arrays for the current step.

```
function [Sig SigCos freq time] = gen_step(fmin);

fmax = fmin * 10;
dt = 1/(10*fmax);
df=(fmax - fmin + fmin)/100;

% The final LPF in the system, has a very long time constant
% because I do this calculation in steps, it needs a warmup
period for each
% step.  That is what this is.
time = [0:dt:200*(1e-2/fmin)];
tmp_time = time;
freq = [fmin.*ones(1,size(time,2))];

for f=[fmin:df:fmax]
```

```
    t_hold = 2/(f);
    len = size([0:dt:t_hold-dt], 2); %1+fix((t_hold-dt)/dt);
    tmp_time = horzcat(tmp_time, [0:dt:t_hold-dt]);
    time = horzcat(time, max(time)+[dt:dt:t_hold]);
    freq = horzcat(freq, f.*ones(1,len)); %size(tmp_time,2)
end

Sig = sin((2*pi).*freq.*tmp_time);
SigCos = cos((2*pi).*freq.*tmp_time);
end
```

D. eis_system.m

This does the actual multiplication and filtering of the signal.

```
%
%                    Mult            Amp
% /---------------(X)--->[LP filter]->DC value of Sensor
Amplitude response
%(~)-->[Sensor]---/
%Vin     Sen   SOut

% time - array of time to analyze over
% freq - Frequency to use at each time point
% delay - initial "warm-up" time for sensor
% sensor - tf() of sensor system
function [SOut Mult Amp AmpCos] = eis_system(time, freq,
Vin, VinCos, sensor)

%(~) - Signal generator
% supplied as arguments: Vin VinCos

%[Sensor] - Model Senor as an RC network
% supplied as argument: sensor

%Find the signal out of the sensor
[SOut,t] = lsim(sensor, Vin, time);
SOut = SOut'; %convert to row matrix


%(X) - Multiply Vin by SOut in time domain
Mult = Vin.*SOut;
MultCos = VinCos.*SOut;

%[LP Filter] - Filter out just the DC
%low pass filter, 2nd order:
% H(s) = wp^2 / s^2 + (wp/Qc)s + wp^2
fo = 1e-3;
```

```
wp = 2*pi*fo;
Qc = 1;
%LPFilt = tf([wp^2], [1 (wp/Qc) wp^2]);
LPFilt = tf([1], [1/(2*pi*fo) 1]);

[Amp,t] = lsim(LPFilt, Mult, time);
Amp = Amp'; %convert to row matrix

[AmpCos,t] = lsim(LPFilt, MultCos, time);
AmpCos = AmpCos'; %convert to row matrix


end
```

E. makePlots.m

This adds the current calculation step results to the final plot.

```
function [] = makePlots(time, freq, Sen, Mult, SigSin,
SigCos)

subplot(2,3,1);
plot(time, Sen);
title('Sensor Output');
xlabel('Time');

subplot(2,3,4);
plot(time,Mult);
title('Multiplier Out');
xlabel('Time');

comp = SigSin + j.*SigCos;

subplot(2,3,2:3);
plot(freq,SigSin,'-b', freq, SigCos, '--r', ...
     freq,abs(comp), '--g');
% plot(time,SigSin,'-b', time, SigCos, '--r', ...
%      time,abs(comp), '--g');
legend('Sin','Cos','Mag','Location','Best');
title('Final DC Out');
ylabel('Value');
xlabel('Frequency');

subplot(2,3,5:6); plot(freq, (180/pi).*angle(comp), '-r');
title('Final Phase');
ylabel('Deg.');
xlabel('Frequency');
end
```

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