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IMPEDANCE EXTRACTION MICROSYSTEM FOR NANOSTRUCTURED ELECTROCHEMICAL SENSOR ARRAYS

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IMPEDANCE EXTRACTION MICROSYSTEM FOR NANOSTRUCTURED ELECTROCHEMICAL SENSOR ARRAYS

By

Chao Yang

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ABSTRACT

IMPEDANCE EXTRACTION MICROSYSTEM FOR NANOSTRUCTURED ELECTROCHEMICAL SENSOR ARRAYS

BY

CHAO YANG

Electrochemical biosensors transform biochemical reactions into electrical information through various electrode transducers. With their high sensitivity and specificity, electrochemical biosensors are ideal agents to detect many inorganic and organic substances. Recently, the microfabrication of biosensors has matured to the point where high density arrays can be generated. A microsystem comprised of such arrays and an integrated circuit (IC) suitable for sensor interrogation and information extraction enables the capabilities of electrochemical sensors to be employed in applications that require miniaturization, including point of care medical diagnostics and distributed safety and security monitoring. In such a microsystem, the interrogation IC must provide extremely high sensitivity, to read the weak response from the miniaturized sensors, and be capable of multi-channel simultaneous readout, to support high density (~100 elements) arrays. This dissertation focuses on overcoming the challenges and limitations in electronics that impede the development of electrochemical microsystems. Specifically, this research targets electrochemical impedance spectroscopy, an essential assay technique for many sensor interfaces. Several possible architectures for multichannel impedance spectroscopy were explored in this dissertation. The key functional blocks, identified as an impedance extractor and digitizer and a wide frequency range quadrature signal generator, were designed, tested, and implemented within a prototype biosensor

array system to validate the design. The results of this research pave the way for further development of ICs for electrochemical sensors and lay a solid foundation for future implementations of fully integrated electrochemical impedance microsystems.

ACKNOWLEDGEMENTS

Though only my name appears on the cover of this dissertation, a great many people have contributed to its production. I owe my gratitude to all those people who have made this dissertation possible and because of whom my graduate experience has been one that I will cherish forever.

First of all, I would like to thank my advisor, Professor Andrew Mason, for his support and mentor in my dissertation work. I am grateful for his encouraging to explore my own during this research. He also gave me tremendous support and understanding for my family. It was a great experience with Prof. Andrew Mason.

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1 Introduction

1.1 Motivation

Electrochemical biosensors [1] are composed of biological element and a sensing element (transducer). They transfer biochemical reaction information into electrical information through the coupling of their two elements. Electrochemical biosensors could be glucose, deoxyribonucleic acid (DNA), proteins, hormones, or even micro-organisms. With their high sensitivity and sensing target specificity, electrochemical biosensors are ideal agents to detect many varieties of inorganic or organic substances [2]. A wide range of applications can be found based on the assay of inorganic or organic substances.

A personal blood glucose monitoring device is a very successful and practical application of biosensors. Blood glucose biosensors benefit 20 million diabetes patients [3] in the US. Biosensors can also be used to diagnose diseases. For example, Wang [4] has developed electrochemical biosensors that quantify the degree of HIV infection. It was estimated that medical biosensor-related products would reach 7 billion US dollars in 2004, and grow at a rate of 9.7% until 2008 [5]. Biosensor arrays provide a very efficient way to perform drug screening in pharmacology research[6, 7]. In security, biosensors are useful to sense bio-toxins and biological warfare agents[8]. In environmental related areas, biosensors can be used for on-site monitoring of water, air, waste processing and soil[9, 10]. Furthermore, biosensors can speed up food testing and greatly promote public food safety in the food industry.

To date, the microfabrication of biosensors is maturing to the point where high density arrays are being, or will soon be, generated. These arrays provide tremendous

advantages. 1) The miniaturized elements increase the detection sensitivity and require smaller amounts of reagents for the analysis, which leads to lower costs. 2) By having large numbers of detection sites and integrating various functionalities, biosensors arrays provide massively parallel sensing capability. 3) The miniaturized biosensor array provides more flexibility in real application due to its small physical size. Traditional expensive and bulky bench-top instruments limit the capability and performance of sensor arrays because long electrical cabling introduces a significant amount noise and interference on the small signals generated from miniaturized biosensors.

To maximize the benefit of the miniaturized biosensor arrays, a microsystem built with these arrays and their interrogation integrated circuit is necessary. Following Moore's Law [11] for more than 30 years, integrated circuit technology can provide powerful information acquisition and signal processing capability within a tiny silicon die. Its low cost and small size leverage the advantages of a biosensor array. With the rapid progress in CMOS circuit compatible biosensor fabrication techniques [12-14], these arrays can be put directly on top of a silicon integrated circuit to form a fully integrated biosensor microsystem. A conceptual structure for such a system is shown in Figure 1.1. This microsystem can be applied in many areas, such as medical diagnostics [5], pharmacology research [6], security enhancement [8], environmental protection [10], and others.

In order to exploit these advantages, some technical challenges must be overcome. These challenges span over a broad range of disciplines, including the microfabrication of the biosensor, electrode construction and electronics design. For the electrical system, it is not just the miniaturized copies of the bench-top instruments. In conventional

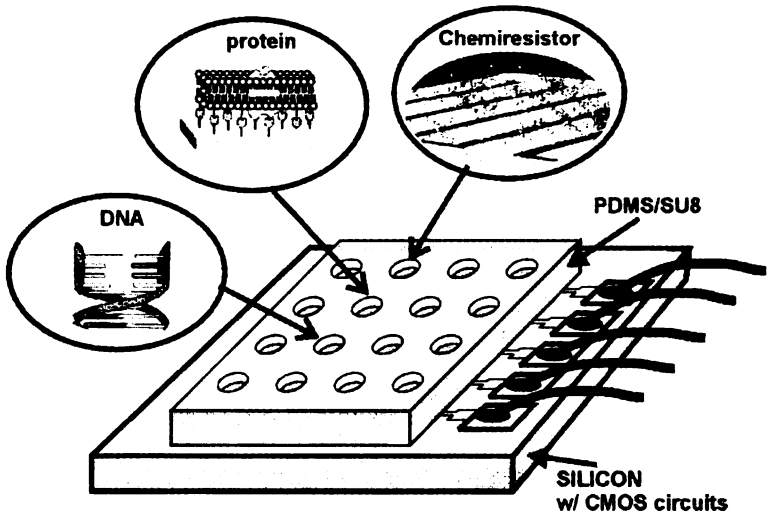


Figure 1.1. Concept diagram of the biosensor array microsystem, the miniaturized biosensor array is built on top of the integrated circuit die.

biological analysis platform, the highest performance instruments are always used, ensuring that the measurement is not limited by the detection system. The performance of the integrated electronics in the biosensor microsystem is limited by the available hardware resource on the silicon die. Moreover, the lower response level of the nano/micro-scale biosensors requires the interface electronics to be more sensitive than bench-top instruments. The electrical system level innovation is also necessary to support the in-parallel interrogation of the large biosensor array. Overcoming the challenges and limitations on the electronics for the microsystem will make a powerful propellant for the adventures leading to the fully integrated electrochemical biosensor microsystem.

This dissertation presents the realization of the integrated electrical system for the biosensor microsystem based on the understanding of the features of biosensor arrays and their electrical interface needs. The focus is the impedance spectroscopy (IS)

interrogation based electrical systems for biosensor array readout. To overcome all above mentioned challenges, creation is needed at both circuit and system level.

1.2 Background

1.2.1 Integrated biosensor microsystems

To date, the microfabrication of biosensors is maturing to the point where high density arrays are, or will soon be, available. Research on miniaturization of biosensors started in the 1990's with a microarray on a glass chip for DNA sequencing [15]. During the same time period, on-silicon chip microelectrode design also made progress[12, 14]. In recent years, some label-free and reusable biomimetic biosensors have been built for electrochemical applications [16-18]. As stated in the motivation section, these miniaturized biosensor arrays provide tremendous advantages. To fully realize these advantages, a microsystem that combines the biosensor microarray and miniaturized interrogation instruments is desired. The conceptual block diagram of such a system is shown in Figure 1.4. Biological recognition element inside the microsystem gathers the

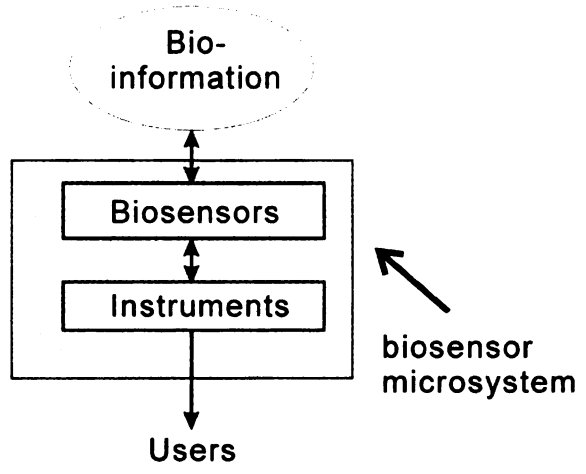


Figure 1.2. Integrated biosensor microsystem.

bio-related information through various reactions with testing environment, and the instrument (transducer) translates inside bio-information into a meaningful forms for end users. Optical analysis based biosensor integration systems are currently in widespread use[19, 20], but they require extensive external equipment. Electrochemical biosensors are considered to be one of the most promising technologies for the next generation of high-performance biosensors because of their inherent scalability and their cost-efficiency in terms of fabrication and detection reagents.

Practically, an integrated electrochemical biosensor microsystem consists of biosensor arrays, interface electrodes, and electrical circuits for interfacing and post signal processing. To increase the reliability of the system and minimize the interference from outside and among different elements, biosensor arrays and electrodes should be built on the top of the silicon chips where the electrical circuit system is built. Figure 1.3 shows a conceptual structure for the microsystem. Some CMOS fabrication compatible processes have been developed for this purpose[12]. Electrodes are always built with

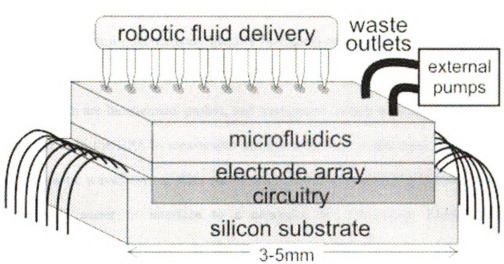


Figure 1.3. Integrated biosensor microsystem.

solid metal, like aluminum or gold. They provide the bases for the formation of the biosensors and bridge between the electrochemical biosensor and electrical circuitry. Electrode size determines the biosensor size. Accordingly, smaller electrode arrays are required to match the miniaturized biosensor array elements. The dimension of a miniaturized electrode could reach 50μm[13]. In some situations, multi-analytes and samples need to appear at different sensor elements, so microfluidic channels are needed to conduct analytes to individual biosensors[12]. The electrical circuit in the integrated biosensor microsystem plays several roles. First, it supports the potentiostat system for each biosensor elements. Second, it generates and applies the proper stimulus signal for different interrogation methods. Third, it processes the potentiostat results. Normally the potentiostat response is conditioned first [21].

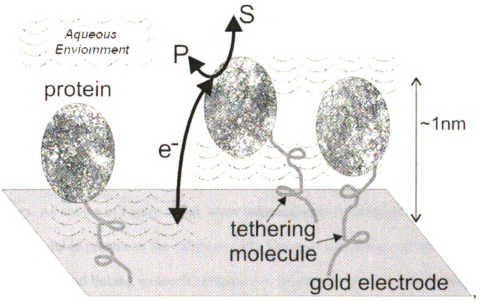
1.2.2 Label-free and reversible electrochemical biosensors

To provide background information for this dissertation research, some potential biosensor elements that are compatible with goals of this research are discussed. Biosensors [1] are devices utilizing biological reactions or binding events to quantitatively or semi-quantitatively identify biological-relevant analytes. There are two fundamental elements in biosensor devices: biological recognition elements (abbreviated as BRE), which are biochemical probes, and transducers, which transfer the biochemical information from the BRE to measurable information, such as electrical signals, optical signals, acoustic waveforms or other forms. Electrical information is preferable to others because it is easier to interface to a computer for processing. Electrochemical procedures[22-25] are involved in the conversion of the biological information to electrical information.

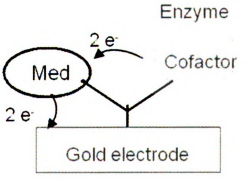
Some biosensors need preprocessing to label the analytic species before sensing. Those labels turn out to be the real detecting target after binding happens. The sensing procedure for some biosensors is non-reversible, which means the sensors need to be replaced frequently. For a biosensor array, these labels and non-reversibility will result in the waste of the unused and reusable sensor elements. These limitations even make the sensing impossible in some situations, such as implanted sensing devices, battle field sensing devices and portable field biosensor devices.

DNA-based biosensors are popular biosensors available for a real application. DNA biosensors use affinity mechanisms to bind the targeted molecules. This kind of biosensor needs preparation of the analytes to attach the florescent or electrochemical labels for the optical[26] or electrochemical[27-29] readout. Also, the sensing procedure is irreversible because once the DNA couples are formed between sensing elements and target molecules this binding can not be broken without destroying the DNA sequence. Antibodies[30-33] can serve as the immunoassay based BRE too. They also rely on the affinity mechanism between antibodies and antigens. Each antibody recognizes a unique antigen [34]. In the human body, this precise binding (affinity) mechanism allows an antibody to label a microbe or an infected cell to initiate an attack by the other parts of the immune system, or to directly neutralize its target (i.e. by blocking a part of a microbe that is essential for its invasion and survival). However, during this attachment process, the binding between the antibody and antigen is so tight that antibody can not come off in a time frame that allows reuse. Therefore, antibody biosensors are also irreversible sensors.

Some protein BREs provide very efficient, specific and selective recognition with good stability and reversibility and without pre-tagging of target species, i.e., label-free. Based on the natural state of these proteins in living organisms, they are categorized as soluble protein and membrane protein. Soluble proteins are dissolved in the liquid cytoplasm of cells. Membrane proteins are attached to, or associated with, the membrane



(a)



(b)

Figure 1.4. Biosensor platform with soluble protein immobilized.

of a cell or an organelle.

1.2.2.1 Soluble protein based biosensors

Many enzymes flow within the liquid environment inside cells. They catalyze (i.e. accelerate) chemical reactions. Like as other catalysts, enzymes are not consumed by the reactions they catalyze. Enzymes are much more specific than other catalysts, making well suited as biosensors. Enzymes can detect the existence and concentration of specific molecules by using a transducer to monitor the reaction rate. Because enzymes are not consumed during the reaction, enzyme-based biosensors are re-usable and can provide reproducible results. As a result, enzymes[35-38] are the most commonly used BREs in protein based biosensors.

Soluble proteins are commonly made immobilized on the electrochemical biosensors. As shown in Figure 1.4(a), some tethering/linking molecules are employed to anchor the soluble protein to the electrode [39]. Enzymes are always involved in charge transformation, and linking molecules (Figure 1.4. (b)) can be used to transfer this charge onto an electrode. Thus, enzyme activities can be monitored by reading the electrical current on the electrode.

1.2.2.2 Membrane proteins

In contrast to the soluble proteins, membrane proteins are attached to, or embedded in, the cell membrane or attached to the surface of it. Cell membranes are composed primarily of a bilayer lipid membrane (BLM), which provides several nanometer-thick insulating barrier between cellular compartments. A diverse set of membrane proteins

impart specific functionalities to precisely control molecular-level transport and signaling. Figure 1.5 shows a conceptual diagram of the cell membrane and a diverse set of proteins.

Because many membrane processes either have an electrochemical basis or can be coupled to electrochemical processes, an electrochemical platform is ideally suited to both measure and control membrane phenomena. It is possible to build electrochemical biosensors with membrane proteins[40]. Some techniques only manipulate single cells and test the electrochemical features of the cell membrane[41]. However, the complicated cell manipulation process makes it hard to use, and availability of the cell membrane protein limits the variety of the protein types. Alternatively, membrane proteins can be embedded into artificial membranes to form a bio-mimetic interface[42]. The membrane protein based biosensor could be built by attaching the artificial membrane to the biosensor platform, as shown in Figure 1.6.

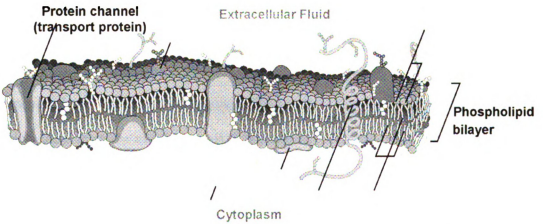


Figure 1.5. Diagram of varieties of proteins that is embedded into or attached with the cell membrane, source: Wikipedia (without copyright control).

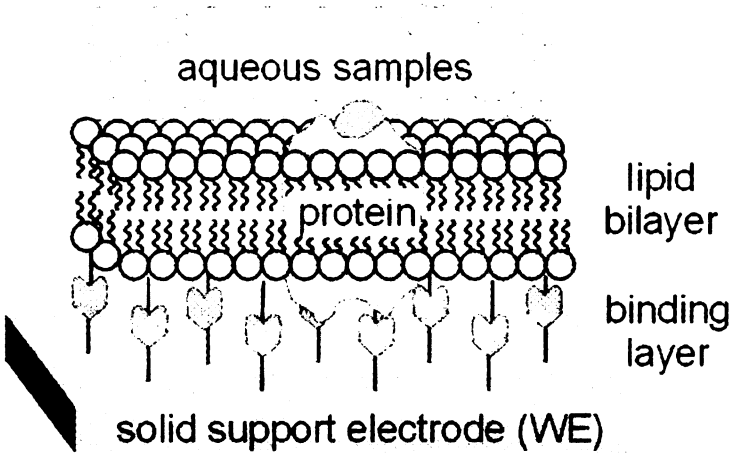


Figure 1.6. Manmade membrane tethered to the solid surface, protein is embedded.

1.2.2.3 Nanostructured bio-interface

The nanostructured biomimetic interfaces can be thought to be an artificial cell membrane. Living cells carry out many vital processes using cell membranes that consist mainly of lipid bilayer and membrane proteins. These functions can be reproduced in the laboratory using biomimetic interfaces, whose structure mimics that of a cell membrane. Since the thickness of lipid bilayers and proteins is about 5nm, research on biomimetic interfaces represents an integration of Biotechnology and Nanotechnology. The nanostructured biomimetic interfaces provide pseudo-natural environments for the membrane proteins. Comparing with the real cell membrane, the synthetic interface can be embedded with more types of protein. With is thickness in the same dimension as proteins, these interface make is possible to study the properties of single protein. This interface features fast response and high sensitivity and therefore are good biosensor candidature. Furthermore, they are feasible to be integrated for multiparameter biosensor array valuable for healthcare, biomedical research, environmental monitoring, etc. They are the prototype biosensors for this dissertation works. Chapter 3 will detail their

characterization. The nanostructured biomimetic interfaces have high sensitivity but their response signal is very weak. The interrogation electronics muust provide very high sensitivity level in order to extract the biomimetic interface information from a weak signal.

1.2.3 Electronic interrogation systems

Traditional bench-top instruments limit the capability of biosensor arrays. They support only one biosensor elements at a time and can not provide a low cost solution for array based multi-channel measurement. Further more, complicated setup of these instruments limits their application for biosensor arrays outside laboratories. Thus, with the miniaturization of biosensors and electrodes, compact interrogation electronics have to be developed. Early efforts in this area have yielded an ion-sensitive field effect transistor (ISFET) arrays in CMOS compatible processes [43, 44], where the biochemical activities of biosensor controls the gate potential of FET transistor and convert the bio-information to electric channel current change. A hybrid microsystems that combine the traditional optical based method and electrical systems [45] was developed by bridging the optical information and electric one with CCD sensors. Potentiostat, which bridges the electrochemical sensors with electric interrogation system, is a necessity for a real electrochemical biosensor interrogation system, and on-chip potentiostats have been developed [46, 47] for compact electrochemical instruments to interface with biosensor array [13, 48], record neural signal [49]. Miniaturized front end electrodes and circuits that digitize results have been integrated with a potentiostat [50] to promote the integration level of the microsystem. However, all of the above only constructed a basic interface for the biosensors; the responses of the sensors were analyzed outside of the

microsystem. They have limitations for the interrogation of a large array of biosensors, especially for an impedance spectroscopy system, where a significant amount of raw data is generated from every sensor element. Thus, a high throughput data path and lot of hardware resources are required to send out this raw information. These solutions are nearly impossible for interrogation on an entire array in parallel. Some impedance spectroscopy systems were also built for biomedical and biochemical measurements [51-53] but do not include integrated circuits. Therefore, they are not suitable for an array based application. At the time of writing, no publications on stand-alone impedance spectroscopy microsystems supporting sensor array can be found.

1.2.4 Challenges of the biosensor microsystems

As a hybrid system, there are many challenges in different aspects, like the microfabrication of biosensors, electrode building and electrical system design. The focus of this thesis is the electrical system of the integrated biosensor array microsystem. In conventional biological analysis platforms, the highest performance instruments are always used, ensuring that the measurement is not limited by the detection system. Unlike these conventional systems, in miniaturized platforms the performance could be limited by the integrated instruments – namely, an on chip electrical circuit system.

As the biosensor elements in the array scale down, their sensitivity will increase, but their response signal level also becomes smaller. The on-chip electronics in the microsystem should be able be capture these weak response signals from a biosensor. The most important feature of the integrated biosensor array is the large amount of sensing elements. Parallel interrogation is expected in order to exploit this advantage. These parallel operations for the large sensor array require a large amount of signal processing

tasks, especially for an electrochemical impedance spectroscopy (EIS) system where complicated signal processing is needed to extract the impedance information. In the traditional method, the potentiostat result is processed by some device with powerful computation capability, such as a digital signal processor (DSP) or computer. It is impossible to instantiate computational devices for each channel due to its physical size. It is also hard to process the sensor array result by a centralized computational device; even a high performance digital signal process can not handle this heavy work load for the large sensor array. The throughput capability of the data channel transferring the original data out could also be a problem for the large sensor array. The solution to this problem is distributing the computation into an individual channel with a compact size analog circuit. How to design such a compact size analog circuit to realize the required computation with the expected performance is a challenge for the electrical system. To enhance the flexibility and lower the measurement cost, the stimulus generator is expected to be integrated to provide a standalone system. Different interrogation techniques need different types of stimulus. Thus, a compact size stimulus generating circuit with flexible waveform is another challenge.

1.3 Research objective and approaches

In this research, an electrical system for a miniaturized, tagless and reusable biosensor array microsystem was developed. The focused interrogation method is impedance spectroscopy. The proposed electrical system includes a sinusoid stimulus generator, impedance spectroscopy circuit and a digitization circuit to provide digital output to facilitate data transmission for parallel interrogation. Conceptually, the electrical system for an EIS microsystem is shown in Figure 1.7. Currently, there are no

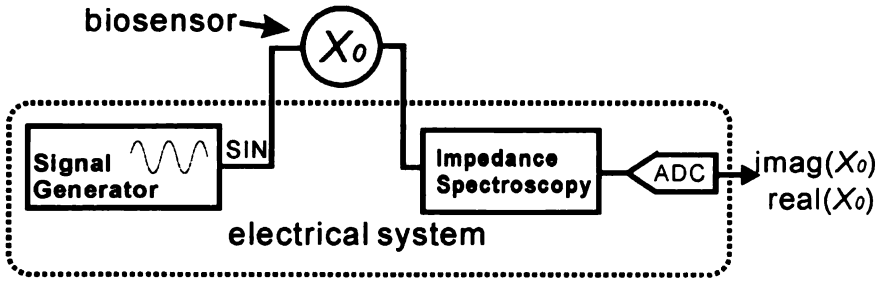


Figure 1.7. Electronic system of the impedance spectroscopy.

publications regarding the realization of channel level signal processing for multi-channel EIS systems. For an EIS application, the sinusoid stimulus signal is needed over a wide frequency range (1mHz to 10kHz). Again, there are no publications reporting a sinusoid signal generator for such a wide frequency range.

This research will first develop a feasible electrical system solution for the biosensor microsystem. Based on this system-level solution, the signal generator and impedance spectroscopy blocks will be designed and fabricated with individual integrated circuits to verify the feasibility of the VLSI realization of this electric system. For the prototype design, a tethered bilayer lipid membrane protein biosensor [42] was selected to define the specifications for the electrical system. All the individual functional circuit blocks will be tested with a fabricated chip. Furthermore, the impedance spectroscopy circuit will also be tested with the real biosensor or biomaterial.

Biosensor microsystem design is complicated and multi-disciplinary work, involving research on integrated electrical systems, microfabrication of electrodes and the development of miniaturized biosensors. Thus, the fully integrated biosensor array microsystem is outside the scope of this thesis. The research in this dissertation will

provide a solid knowledge and technology basis for the future development of a fully integrated microsystem.

1.4 Thesis outline

Chapter 2 describes popular electrochemical interrogation methods and prototype microsystem realization. Chapter 3 discusses the requirements for the biosensor array impedance spectroscopy (IS) microsystem and some feasible system level approaches for the electrical portion. Based on the conclusion of the system approach in Chapter 3, Chapter 4 describes the development and VLSI realization of a channel level compact impedance spectroscopy circuit (an impedance digitizer). In Chapter 5, a wide frequency range quadrature sinusoid signal generator, which covers frequencies from 1 mHz to 10kHz, is developed and implemented in VLSI. The testing results for the many VLSI realizations required for a multi-channel EIS system are provided and discussed in Chapter 6. In the final chapter, both the summary of this dissertation work and suggestions for future research in this area are provided.

2 Electrochemical Interrogation Methods

In the biosensor, while BREs actually capture biological information, transducers are required to convert the biological information into measurable form so that further processing on the information can be performed. This measurable information can include electrical signals, optical signals, acoustic waveforms and other forms. Electrical information is preferable to others because it is easier to interface with and be processed by the computer. Electrochemical procedures[22-25] are ideal to produce the electrical result. Basically, all sensing procedures in electrical biosensors have the following generalized steps. 1) The analytic species appears in the reaction chamber (normally a specific buffer solution) and collides with the BREs. 2) The targeted analyte and the probe form bio-chemical bonds, which change certain electrochemical properties of the biosensor. 3) The transducer translates this electrochemical property change and translates this to observable quantities electrochemically. To sense the electrochemical feature change, an electronic signal is required to stimulate the biosensor. The electrical response from the biosensor carries electrochemical property information. A potentiostat works as the bridge between the electronic system and the biological system during this procedure. Some electrochemical measurement techniques are developed on top of the potentiostat to extract different information with a specific stimulus. The potentiostat system and popular electrochemical interrogation methods will be studied in this chapter. In addition, a prototype voltammetry microsystem built to study the electronics systems for the microsystem will be discussed.

2.1 Potentiostat

While there are many electrochemical interrogation methods, they are all based on the potentiostat. In amperometric operation, the potentiostat applies a voltage with a predefined shape to a biosensor and monitors the current response. A typical potentiostat in the electrochemical domain is illustrated in Figure 2.1. Electrodes are solid contacts built with metal or semiconductor. They provide the interface between chemical reaction and electrical system. According to the function of the electrodes, they are classified as working electrode (WE), reference electrode (RE) and counter electrode (CE). The potentiostat measures the voltage-to-current (VI) response. We can apply the voltage between two electrodes (i.e. WE and RE in Figure 1.3) and monitor the current flow between them. Normally, three electrode potentiostats are widely used with the RE put as close as possible to the WE. With the feedback system built with an amplifier connecting RE and CE, the potential of RE is fixed to the reference (analog ground) potential. RE

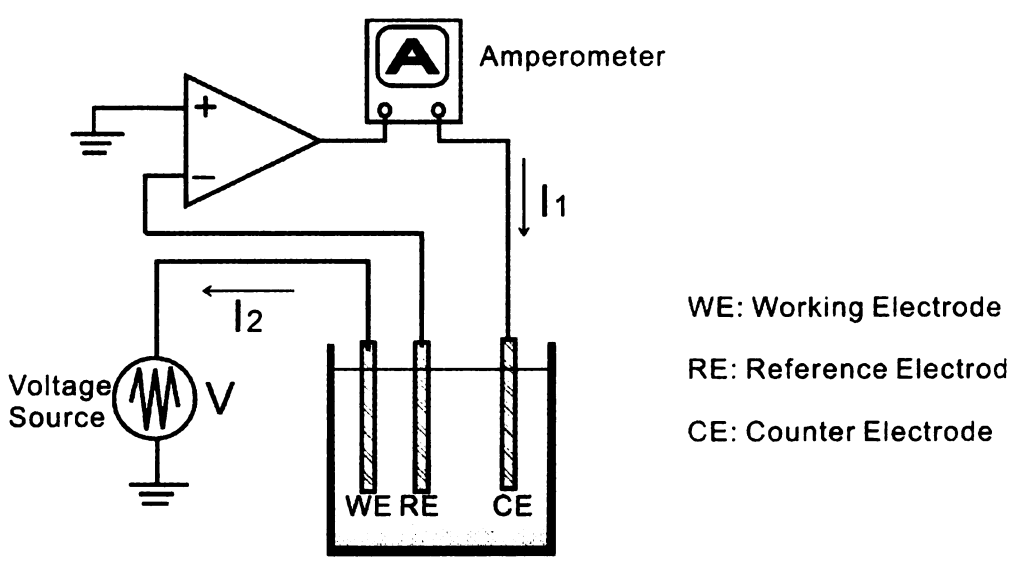


Figure 2.1. Simplified schematic of a typical electrochemical potentiostat system. Normally three electrodes are employed: a working electrode, a reference electrode and a counter electrode.

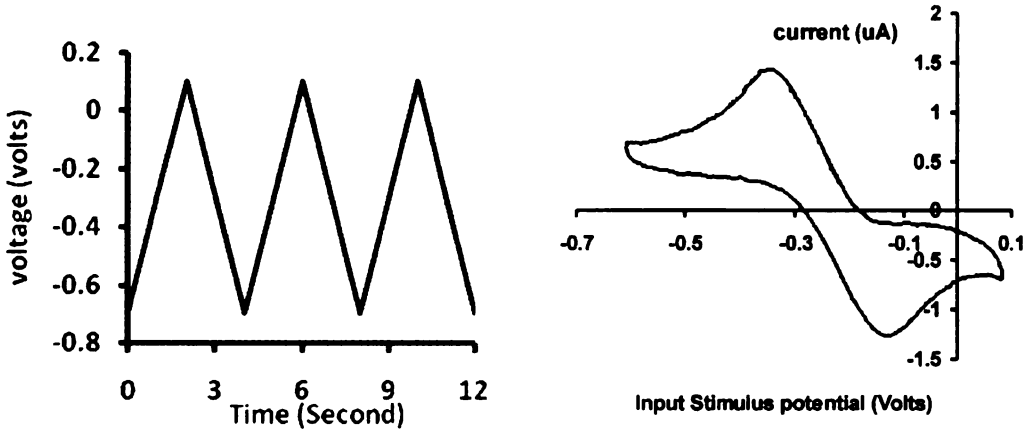
does not draw current because of the very high input impedance of the amplifier. Therefore, the potential in the solution around the CE is the same as the RE and fixed to the reference potential. A three electrode potentiostat system has several advantages over its two electrode counterpart. First, it provides very accurate potential control between the WE and the surrounding solution where electrochemical reactions occur on the interface in response to the potential difference. Secondly, in-series solution resistance can be minimized to the point of becoming negligible through placing the RE very close to the WE. In real applications, some systems have more than three electrodes. Their principles are the same as that for the three electrode system.

With the potentiostat system, a wide range of techniques have been developed to qualitatively and quantitatively determine the kinetics and thermodynamics of electrochemical reactions. Several techniques that are often used for biosensors are introduced in this chapter.

2.2 Voltammetric techniques

Voltammetric techniques study the response of a biosensor over time by applying a time-varying stimulus. They study the relationship among stimulus potential (E), responding current (I), and time (t).There are several variations on these techniques[54]. Cyclic voltametry is the most widely used votametric method.

Cyclic voltammetry (CV) has become an important and widely used electroanalytical technique in many areas of biochemistry. It is widely used to study reduction-oxidation (redox) processes, reaction intermediates, and the stability of reaction products. This technique is based on varying the applied potential at WE in both the forward and reverse directions (at some scan rate) and monitoring the current. A typical



(a) (b)

Figure 2.2. (a) typical stimulus potential for cyclic voltammetry, (b)cyclic voltammogram.

stimulus potential waveform is shown in Figure 2.2(a). It is a triangle wave with a certain slope and amplitude. The timing information of this sweep is contained within the slope of the triangle waves. The result of the cyclic voltammetry can be shown visibly by plotting the instant responding current against the instant stimulus potential (Figure 2.2(b)). This plot is called a cyclic voltammogram.

2.3 Impedance spectroscopy

Instead of studying the relationship between the stimulus potential, response current and time, impedance spectroscopy (IS) studies the relationship between the stimulus potential, response current and frequency of stimulus. IS monitors the transfer function of the biochemical system to a sinusoid stimulus at individual frequency points and plots the ratio against the frequency. In some situations, several interrogation techniques can have comparable effectiveness. However, when complex heterogeneous reactions interact with mass transport, a frequency analysis is more efficient [55].

2.3.1 Bode plot

If a sinusoid signal is fed in as the stimulus, assuming that the electrochemical

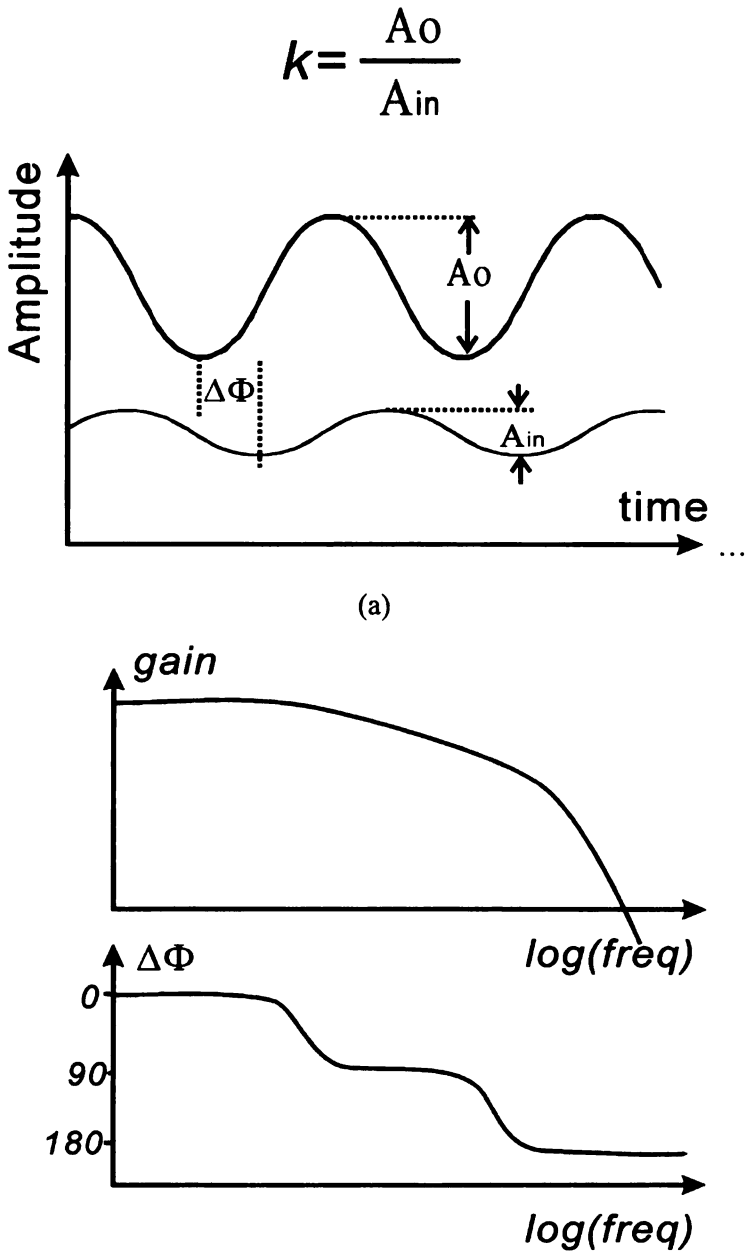


Figure 2.3. (a) the input sinusoid waveform and the electrochemical response of a potentiostat system. The output waveform is still a sinusoid, but multiplied by K with a phase delay of $\Delta\Phi$, (b) bode plot of the system response.

system is linear (which is true for small signals), the response of the electrochemical system is also a sinusoid of the same frequency but with differences in phase and amplitude (Figure 2.3). If a phase shift is involved, we can not use a single resister or conductor to represent the transfer function. Instead, impedance (or admittance) are needed to represent both the amplitude and phase changes. To characterize the transfer function of the system, we can extract the amplitude gain (K) and phase shift ($\Delta\varphi$) by comparing the response and the stimulus of the biosensor. Then (K, $\Delta\varphi$) pairs for the frequency range of interest is acquired and plotted as in Figure 2.3(b). This kind of plot is called a Bode plot.

2.3.2 Nyquist plot

Alternatively, we can rewrite the sinusoid signal of a certain known frequency as an in-phase component and quadrature phase component, as given by

$$a\sin(\omega t + \phi) = a\sin(\phi)\cos(\omega t) + a\cos(\phi)\sin(\omega t) \tag{2.1}$$

At a known frequency, we can just use the coefficients of these two components to represent this signal. With the help of complex notation, the amplitude of the in-phase component and the quadrature phase component are represented as the real and imaginary parts of a complex number ($A+jB$). Thus the transfer function of the system can be easily represented mathematically by

$$Z = \frac{A_0 + jB_0}{A_{in} + jB_{in}} \tag{2.2}$$

By mathematical derivation in the complex domain, we can derive Z, which is also a complex number. By plotting the real portion versus the imaginary portion of Z over the frequency range of interest, a plot shown in Figure 2.4 is achieved. This kind of imaginary part versus real part plot is called a Nyquist plot. A Nyquist plot does not present the frequency information directly, but the shape of the curve in it already gives enough information.

2.3.3 Linearity of electrochemical systems

In the above discussion, a fundamental assumption is that the system under study is linear. For a biosensor based electrochemical system, this is not always true [56]. In order to apply the IS method introduced above, a small signal analysis for non linear systems concept is used to linearize the system. This concept states that, for a nonlinear system, if a stimulus signal is small enough, it can be viewed as a linear system at that point with very good accuracy. In the potentiostat for an electrochemical biosensor system, a large DC voltage is applied to set the proper state of the system, and a small AC stimulus is applied. Finally, the output AC signal is monitored and compared with the input AC

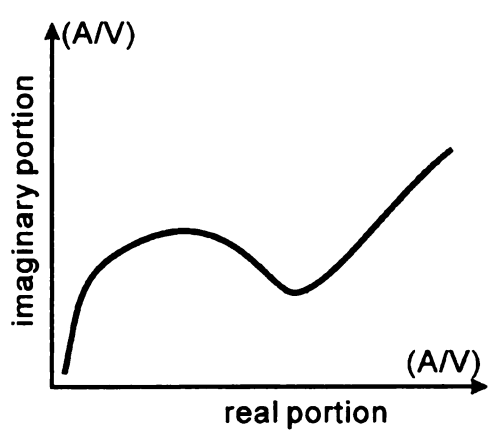


Figure 2.4. Example of the Nyquist plot of the admittance for a biochemical potentiostat.

signal to extract the impedance information.

2.3.4 Electrical circuit models for electrochemical systems

For IS, the electrochemical systems on the surface of a solid electrode are always modeled as electrical circuit networks. The components used in the circuit model and their values embody certain electrochemical processes and phenomena involved in electrochemical reactions. By analyzing the IS result, either with a Bode plot or a Nyquist plot, we can figure out the component parameters of interest in the equivalent circuit model. Eventually, the electrochemical reactions can be studied quantitatively from the component values of the circuit model. There are many different circuit models for different types of electrochemical processes [56].

2.4 Prototype potentiostat microsystem

To better understand electrochemical microsystems and explore the practical issues of real VLSI realization of such microsystems, an amperometric microsystem that support the electrochemical biosensor array has been developed based on the previous works of our group [46, 57]. This microsystem can perform the voltammetry interrogation techniques for a biosensor microarray.

2.4.1 Architecture of the microsystem

The system view of the amperometric microsystem is shown in Figure 2.5. A miniaturized electrode array was formed on top of the silicon chip, in which the interface circuits are built. A variety of biosensors will be deposited onto the corresponding electrodes with a CMOS compatible process. A reference electrode (RE), a counter

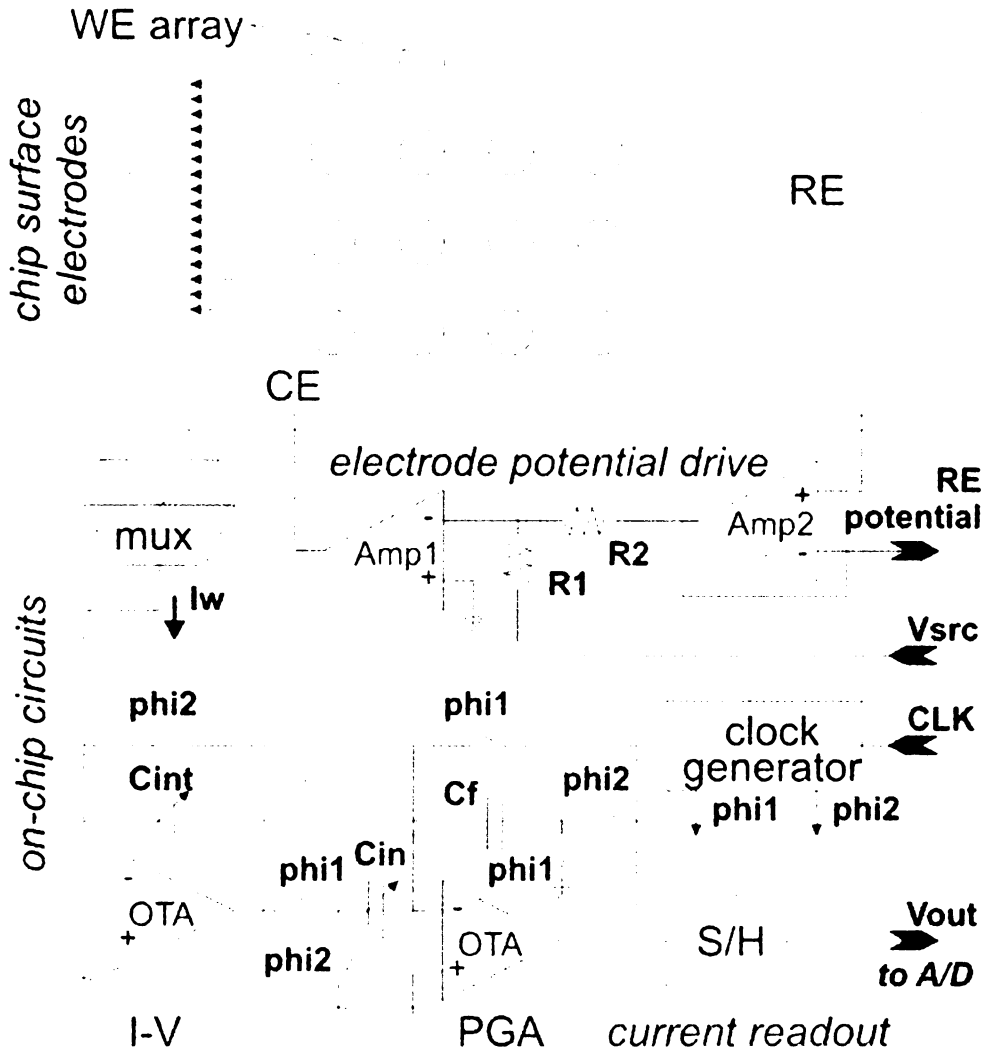


Figure 2.5. An amperometric microsystem comprised of a switched capaitor amperometric readout block, an electrode potential drive block, and a current switching matrix (mux).

electrode (CE), and a multi-parameter array of working electrodes (WE) were patterned on the surface of an electrochemical interface circuit using post-CMOS fabrication. The interface circuit drives a three-electrode system of an on-chip biochemical sensor array. It also provides amperometric readout for the biosensor array's current response. To cater to the diversity and explore the high sensitivity of biochemical sensors, this interface circuit must deal with a wide range of input current with a low noise feature.

In the electrode potential drive block of Figure 2.5, control signal *Vsrc* sets the potential applied across the electrochemical cell, and either a constant voltage or a sweeping signal (for CV measurements) can be applied. *Amp2* is configured as a unity gain buffer to sense the RE potential without loading RE. *Amp1* and *Amp2* form a feedback circuit to control the RE potential through the CE to establish a potential difference between the RE and the chosen WE. Notice that the RE can not sink/source electrical current, so all current measured at the WE comes from the CE, which helps maintain the stability of the RE electrochemical potential.

In the current readout block [58], a switched capacitor (SC) charge integrator converts the sensor output current into a voltage, which then goes through a programmable gain amplifier (PGA) that has auto-zero compensation. The output voltage is then sampled, held, and fed to an A/D converter. The entire readout chain utilizes correlated double sampling (CDS) [59] to reduce the *kT/C* noise as well as amplifier offset. The output of the current readout block, *Vout*, is given by [58]:

$$V_{out} = \frac{I_W}{C_{int} f_S} \cdot \frac{C_{in}}{C_f} \qquad (2.3)$$

where, *fs* is the frequency of phi1, *Iw* is the sensor current from the working electrode, *Cint* is the integrator capacitor, *Cin* is the binary weighted programmable capacitor at the PGA input, and *Cf* is the feedback capacitor of the PGA.

The response sensitivity of bio-interfaces applied to the WE array can vary widely, resulting in a broad range of currents to be measured by the readout circuit. The current generated by the transducer is also directly proportional to the area of the WE. To support these variable current levels, which are not set until after the electrochemical interface circuit is fabricated, it is vital that the current readout block operate over a wide range of input currents. As shown by (2.3), the overall readout circuit gain (*Vout/Iw*) is determined by the clock frequency, the PGA gain (*Cin/Cf*), and the value of the integrator capacitor. Thus, by using on-chip programmable capacitors for *Cint* and *Cin* and adjusting the clock frequency, the readout circuit can be adapted to a large input current span. The capacitor values and operational frequency were designed to support input currents ranging from 10 pA to 10 μA.

2.4.2 VLSI realization

Two kinds of amplifiers are employed for the electronic interface, depending on their loading characteristics. The amplifiers used in the potentiostat drive block in Figure 2.5 drive the biosensors, which could have complicated impedance characteristics over a wide value range. In order to minimize the effects of varying loading on the stability of the system, a two-stage amplifier is designed because its dominant pole is located inside the amplifier and is independent of the loading characters. For the amplifiers in the current readout block, their loadings are purely capacitive with known value. Thus, cascode single stage amplifiers are employed here to save hardware area by eliminating

the Miller compensation components. With the dominant pole located at the output node, the purely capacitive loading will only improve the phase margin.

The schematic of the two-stage amplifier used in the electrode potential drive stage is plotted in Figure 2.6. With Miller compensation, the internal pole at the node "a" and the output pole are split away from each other, while the internal pole becomes the dominant pole. Simulation shows this amplifier has 110dB DC gain and at least 3.5MHz unit gain bandwidth with varying loading conditions. For a bioelectrochemical application, the frequency of the stimulus is always in a very low frequency range, i.e. less than 100Hz. The DC gain and the bandwidth are high enough to make sure the electrode potential driving stage can transfer the stimulus to the sensors accurately.

An operational transconductance amplifier (OTA) configuration has been chosen for the switched capacitor (SC) current readout block. The two main design

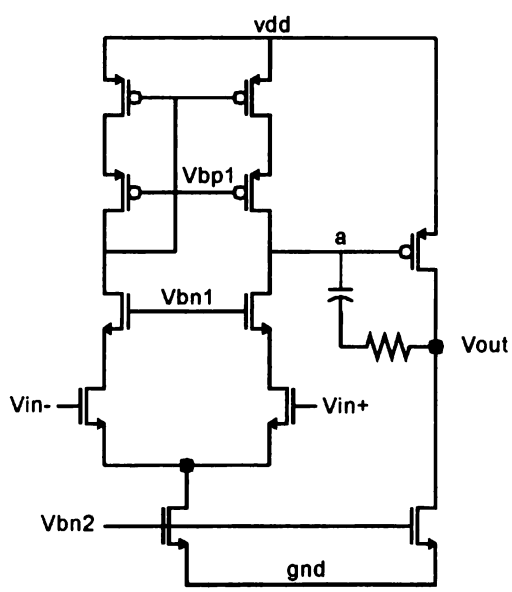


Figure 2.6. Schematic of the two stage amplifier.

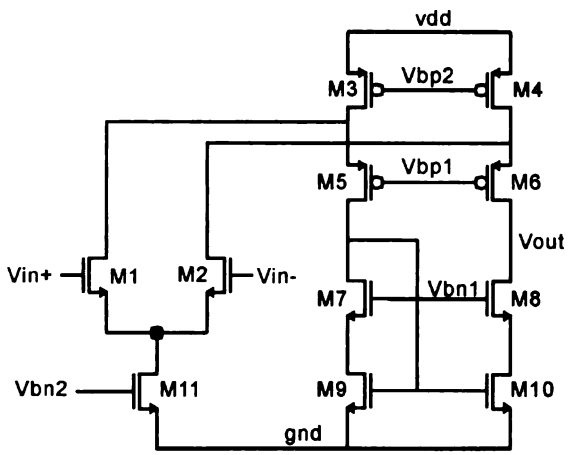


Figure 2.7. Schematic of the folded cascode OTA.

considerations for this OTA are high gain, to ensure precision operation, and rapid settling time, to ensure that the output settles within half of the clock period. Figure 2.7 shows the schematic of an OTA. MN1 and MN2 form the input differential pair, MN11 acts as the tail current source pair, MP5 and MP6 are cascode transistors to the input differential pair, MP3 and MP4 form the PMOS current source and MN7, MN8, MN9, MN10 form a wide swing cascoded NMOS current source. Because the load is purely capacitive in SC circuits, an op amp with a single high impedance output node is suitable. A cascode gain stage is selected for the high gain and immunity to the Miller effect at high frequencies. The amplifier output is shorted to the input during the first phase of SC operation. Therefore, a folded topology, which allows the input and output voltages to be at the DC same level, is necessary. Due to the higher mobility of NMOS devices, NMOS transistors are chosen for the differential input stage to provide a higher transconductance, gain, and bandwidth than their PMOS counterparts. The simulated performance of this circuit shows a DC gain of 79dB, unity gain bandwidth of 24MHz with a 60 degree phase margin, 49 V-sec^{-1} slew rate and 33 nsec settling time, an input/output range of 0.8 V to 3

V, CMRR of 107 dB (DC) and PSRR of 80 dB. In 0.5μm CMOS with a 3.3V supply and 3pF load, the circuit, including the bias stage, dissipates 1.1mW.

2.4.3 Electrochemical experiment

The circuit was fabricated with a 0.5 μm CMOS process. Figure 2.8 shows the 3×3mm die with circuit blocks labeled and surface electrodes illustrated. This version of the chip implements a 4×4 array of 100 μm2 working electrodes, but the circuit and post-CMOS process can be scaled to a much higher density, covering the entire surface of the chip. Array density is ultimately limited by fluid handling constraints to approximately 100 electrodes per chip with our existing equipment.

To perform initial electrochemical testing with the system, a prototype electrode array built on a glass chip is employed. As both silicon chip and glass are made of silicon,

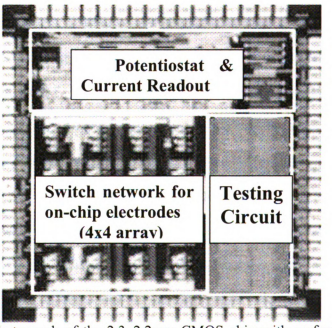


Figure 2.8. Die photograph of the 2.3x2.2mm CMOS chip with surface electrodes and circuit blocks labeled.

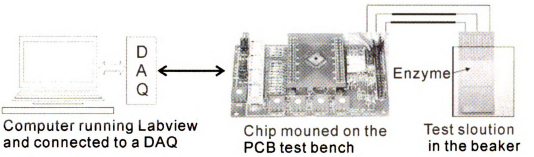


Figure 2.9. The testing setup for the biosensor microarray based on-chip platform.

they have very similar physical features. Thus, a glass chip can mimic a CMOS chip very well. The same micro-fabrication procedures of electrode formation and biosensor deposition, are performed for the prototype electrode array. The whole testing setup for the biosensor array platform, including the prototype biosensor array, is shown in Figure 2.9.

To verify the on-chip electrochemical interface circuit properly performs cyclic voltammetry measurements, a cyclic voltammogram of secondary alcohol dehydrogenase modified electrodes (working electrodes) is performed. They are in the 0.1M PBS with 2-propanol of concentration 5, 15 and 25mM. The temperature is at 25 ° C and the scan rate is set to 100 mV s^{-1}. The reference electrode is a Ag/AgCl electrode. A 530 mV peak-to-peak triangle wave was generated and applied between CE and WE, sweeping from -100 mV to 430 mV (with respect to the RE potential) at 2 Volts. The on-chip amperometric readout circuit was clocked at 100 kHz, and the cyclic voltammogram shown in Figure 2.10 was captured. The typical shape of this curve verifies the on-chip potentiostat operates as expected and can perform cyclic voltammetry. The oxidization peak values, which are the bottom peaks in Figure 2.10, are also plotted against the

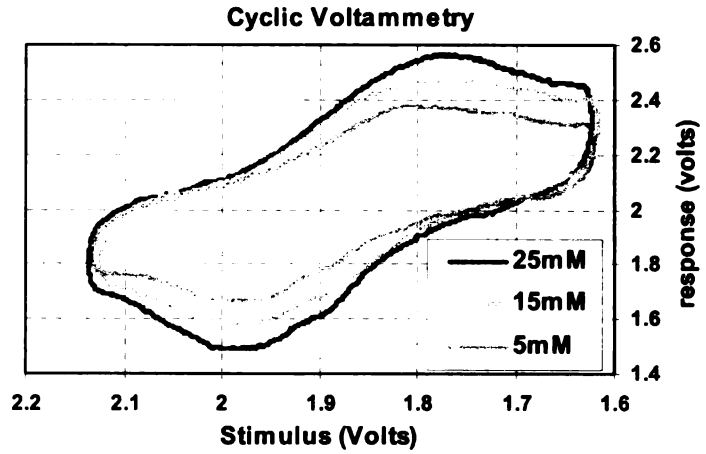


Figure 2.10. Cyclic voltammogram of secondary alcohol dehydrogenase modified electrodes in 5, 15 and 25 mM 2-propanol in 0.1M PBS, at 25 ° C and 100mVs^{-1} scan rate, vs. Ag/AgCl reference electrode.

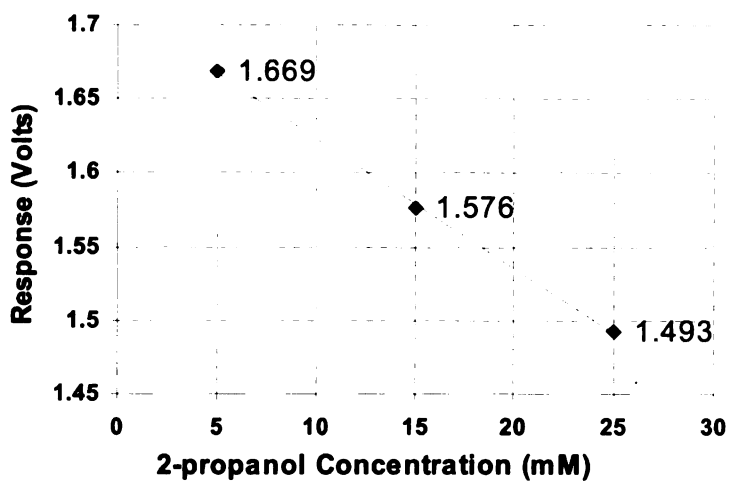


Figure 2.11. Oxidation peak values VS. 2-propanol concentration levels.

concentration levels of the 2-propanol in Figure 2.11. The high linearity of their relationship is convincing of good performance of this on-chip potentiostat platform.

2.4.4 Conclusion

A single-chip amperometric readout circuit and electrode array system suitable for bioelectrochemical measurements has been designed and implemented. The on-chip

circuitry features an electrode potential control block and a current readout block that serves as an electrochemical potentiostat capable of performing chronoamperometery and cyclic voltammetry.

3 System Approaches for a Impedance Spectroscopy Microsystem

In this chapter we will propose an impedance spectroscopy system targeted for on-chip biosensor arrays, specifically the miniaturized on-chip protein embedded tethered bilayer lipid membrane (tBLM) [42] biosensor array. The electrical features and circuit models of the tBLM biosensor array will be discussed first. The system level approach for impedance spectroscopy will also be discussed. Feasible approaches are given at the end of this chapter.

3.1 Electrical features of a miniaturized tBLM biosensor

The structure of a tBLM biosensor is illustrated in Figure 3.1. Protein is embedded into the artificial lipid bilayers to mimic the function of ion channels in the cell

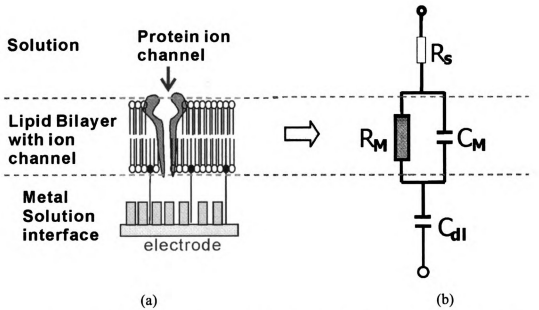


Figure 3.1. (a) structure of the tBLM biosensors and (b) their equivalent circuit mdoel.

membrane. Some ion channels are very specific and selective to certain types of ions in the bulk solution. Once the corresponding ions are present in the bulk solution, these ion channels will open and conduct current when the proper potential drop across the lipid bilayers is applied. The tBLM's conductivity (real portion of the admittance) carries the information of existence and concentration of certain ion in the solution. This conductivity information is modeled in the equivalent circuit as a resister (R_M in Figure 3.1(b)), which is the sensing parameter of interest.

In this structure (Figure 3.1(a)), other phenomena couple electrochemically with the ion channel activities and prevent direct resistance measurement of R_M. At the surface of the electrode, the accumulation of ions near the electrode form a metal-solution double layer capacitance, which is modeled as C_{dl} in Figure 3.1(b). This capacitor prevents DC resistance measurement techniques to be applied for R_M. Two surfaces of the artificial lipid bilayers also form a capacitor, which is called the membrane capacitor and is in parallel with R_M. The bulk solution surrounding the tBLM shows resistance to ions and thus affects the electrochemical system as a resistor (modeled as R_S in Figure 3.1(b)). Its effect is normally ignored because its value, which is in the hundreds of ohms range, is much smaller than the impedance of the other components in the circuit models. Typical values for other components in the equivalent circuit in Figure 3.1f(b) are C_m = 0.59 $\mu F/cm^2$, C_{dl} = 3.9 $\mu F/cm^2$, and R_m = 46 $K\Omega cm^2$(would vary according to target analyte concentration)[60].

In order to measure the R_M with the coexistence of the other components in Figure 3.1(b), electrochemical impedance spectroscopy (EIS) is employed. Through analyzing

the response of the system over frequency, R_M can be deduced. Figure 3.2 shows the EIS response of a tBLM biosensor with area of $0.1cm^2$ corresponding to two different analyte concentration levels. Both a Bode plot and a Nyquist plot are shown.

In Figure 3.2 , impedance value in the flat region of the impedance plots can be approximated as the ion opening resistance (R_M in Figure 3.1(b)). The frequency range corresponding to the flat region of impedance plot could range from several mHz to tens of KHz [61]. This frequency range is not related to the size of the tBLM biosensor because the featuring frequency is determined by the ratio of those components in the circuit model and the scaling is proportional for all components. We can also figure out the range of the response current. It is obvious that the current response is directly proportional to the area of the tBLM biosensors. Also the current is proportional to the stimulus signal strength. As discussed in Chapter 1, in order to linearize a tBLM biosensor electreochemical system, only small excitation is allowed. Assuming it is 5mV, the strength of the current response between the 10 mHz to 10 KHz is about $1nA/cm^2$ ~ $10uA/cm^2$. The size of the miniaturized tBLM sensor can be changed from sub-mm range to sub-cm range. In order to design an EIS system with compatibility for more general purpose applications, we summarize the electrical interface as in Table.3.1

TABLE 3.1. RANGE OF FREQUENCY AND CURRENT RESPONSE

Interested frequency Range	1mHz ~ 10KHz
Sinusoid current response strength	0.001nA ~ 100nA

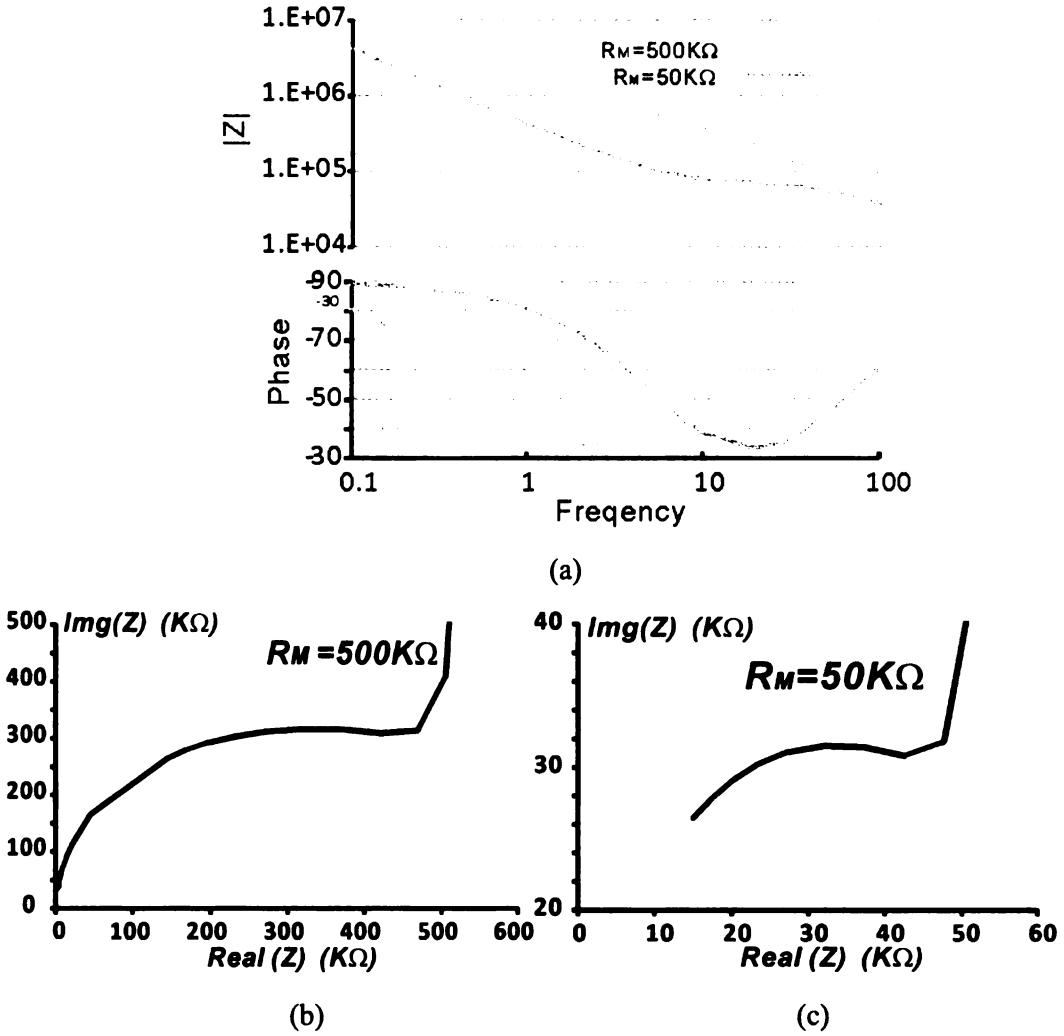


Figure 3.2. The EIS output of tBLM biosensor with an area of $0.1cm^2$, with two sets of R_M's mimicking sensing the analyte with different concentration. (a) shows the output on a Bode plot, (b) shows the EIS output on a Nyquist plot with R_M=500KΩ, (c) shows the EIS output on a Nyquist plot with R_M=50KΩ. The Bode plot shows that the frequency range of interest is at low frequencies.

3.2 Techniques to realize on-chip EIS

Several techniques are used to perform impedance spectroscopy. They can be sorted into two categories: the fast Fourier transform (FFT)-based IS and the frequency response analyzer (FRA) based IS.

3.2.1 FFT based methods

A Fourier transform is a mathematical method used to transfer a time domain signal ($x(t)$) into the frequency domain ($F(\omega)$), shown in (3.1). $F(\omega)$ shows the frequency content of $x(t)$. $F(\omega)$ is a complex number and can be expressed as amplitude and phase, or real part and imaginary part.

$$F(\omega) = \frac{1}{2\pi} \int_{-\infty}^{\infty} x(t) e^{-i\omega t} dt \tag{3.1}$$

The FFT is an efficient algorithm to compute the discrete Fourier transform (DFT), and is very suitable to digital signal processing. A general block diagram of FFT based impedance spectroscopy system is shown in Figure 3.3. A white noise source produces the perturbation excitations to the biosensors. An A/D converter converts the biosensor response to a digital signal, and the discrete-time Fourier transform (FFT) is performed in the digital domain with the help of the digital signal processor (DSP).

The most important advantage of the FFT is that the FFT method can work out the frequency response at all interested frequencies at the same time. To gain this benefit, the small stimulus excitation source needs to produce all the interested frequency components simultaneously. There are multiple ways to generate a pseudo white bandwidth source that contains as many frequency components as possible[51]. White noise contains many frequency components, which means that it can serve as the source

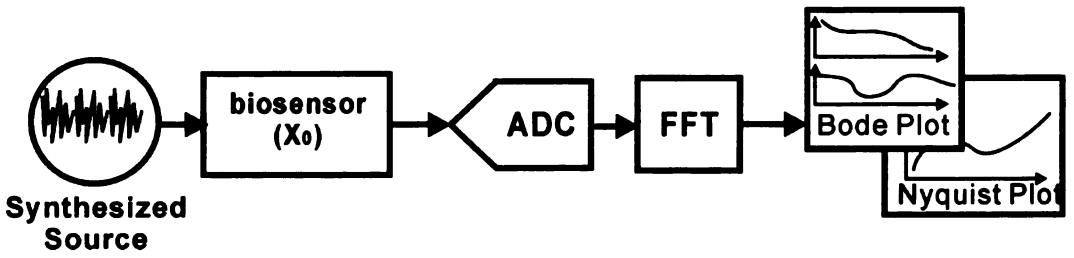


Figure 3.3. The principle block diagram of FFT based EIS system.

here. Computers can be used to generate a pseudo random digital sequence as the white noise source. The edges of the square pulse have many frequency components, so we can also use periodic square pulses or random square pulses as stimuli. All above mentioned methods have the random spectrum and thus result in more or less variation due to the uneven strength of frequency components in the spectrum. Instead, a synthesized source with a limited number of frequency points with the same strength can be generated with the help of the computer.

The FFT block plays a key role in the FFT based solution. Complicated computation is needed to perform the discrete Fourier transform even if the efficient fast Fourier transform or some other techniques [62] are employed. Large memory is also needed to store the intermediate results and the input/output digital sequence. These factors prevent the analog realization. DSP or a computer is always involved in the FFT.

The composite signal source and the computation intensive Fourier transform force the FFT based solution to require systems with powerful digital computation and control capability, such as a personal computer or a DSP system. Although some practice was done to realize the FFT with an analog circuit [63], it is far from practical due to the poor accuracy and preprocessing/pre-storing of the input data set. The size and power of the intensive digital circuit of the FFT method prohibits it from being implemented for low-power compact integrated biosensor interrogation systems.

3.2.2 FRA based method

Unlike the FFT based method, which works out the response at all interested frequencies at the same time, frequency response analyzer (FRA) based methods process

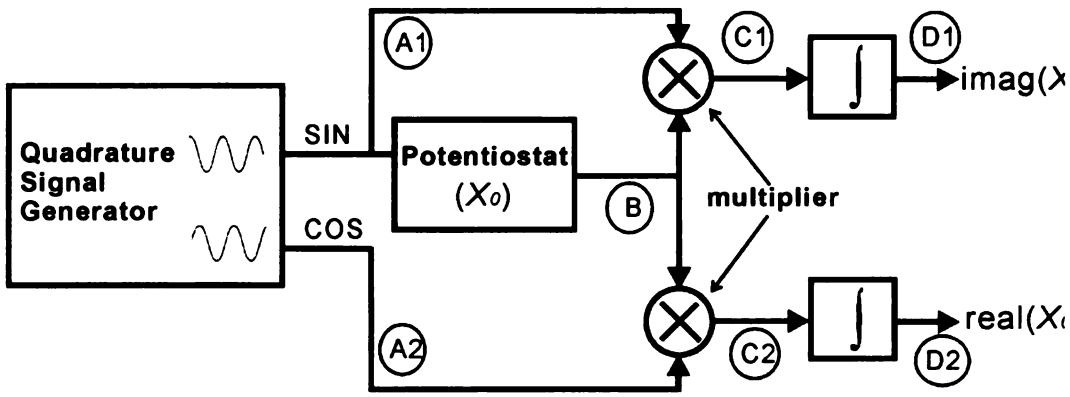


Figure 3.4. Block diagram of frequency response analyzer based impedance. Spectroscopy.

the response at single frequency points one at a time. Its principle block diagram is shown in Figure 3.4. It consists of a quadrature signal generator, multipliers and integrators.

A quadrature signal generator produces a pair of sinusoid signals with the same amplitude and frequency, but with a 90° phase shift. It produces signals at a single frequency one at a time and is capable of sweeping over the entire frequency range of interest. A couple of multipliers are employed to perform the needed signal processing. As its input and output are all analog signals, the multipliers are realized with an analog circuit. In the end, integrators remove the interference and produce the constant DC signals which represent the real and imaginary parts of the admittance of the biosensors.

Assume that the signal generator produces the sine and cosine signal with zero initial phase at a frequency of ω. The response of the biosensor (at node B) can be expressed as $A\sin(\omega t+\varphi)$. The pair (A, φ) represents the impedance information of the biosensors. The signal at node B can also be expressed as:

$$A\sin(\omega t+\varphi) = A\cos(\varphi)\sin(\omega t) + A\sin(\varphi)\cos(\omega t) \qquad (3.2)$$

The coefficients in (3.2), i.e., Acos(φ) and Asin(φ), represent the real part and imaginary part of the admittance of the biosensors. The system in Figure 3.4 calculates Acos(φ) and Asin(φ), at each frequency point of interest. The outputs of the multipliers are

$$S_{C1} = A\sin(\omega t + \varphi)\sin(\omega t) = \frac{A}{2}[\cos(\varphi) - \cos(2\omega t + \varphi)] \tag{3.3}$$

$$S_{C2} = A\sin(\omega t + \varphi)\cos(\omega t) = \frac{A}{2}[\sin(\varphi) + \sin(2\omega t + \varphi)] \tag{3.4}$$

Both (3.3) and (3.4) have the DC components and AC components located at twice the stimulus frequency. The DC components are the real part and imaginary part of the admittance with a scaling factor of 0.5. With the help of the integrator, the components at twice the stimulus frequency are suppressed, and the DC components are amplified.

$$\begin{aligned} S_{D1} &= \frac{1}{T}\int_0^T \frac{A}{2}[\cos(\varphi) - \cos(2\omega t + \varphi)]dt \\ &= \frac{A}{2}\cos(\varphi) - \frac{A}{4T\omega}[\sin(2\omega t + \varphi) - \sin(\varphi)] \end{aligned} \tag{3.5}$$

$$\begin{aligned} S_{D2} &= \frac{1}{T}\int_0^T \frac{A}{2}[\sin(\varphi) + \sin(2\omega t + \varphi)]dt \\ &= \frac{A}{2}\sin(\varphi) + \frac{A}{4T\omega}[\cos(2\omega t + \varphi) - \cos(\varphi)] \end{aligned} \tag{3.6}$$

To suppress the components at double the stimulus frequency (interference components), we either integrate over a long enough time or make the duration of the time to be exactly the half period of the stimulus signal. At high frequencies, the former method is always used because it is hard to control the duration of integration to be

exactly half of the period. As the relative error is small to set the duration of integration to be half cycle at low frequencies, latter method is chosen for low frequency interrogation and minimizes interrogation time.

In addition to a high feasibility of realization as an integrated circuit, this architecture is immune to the DC offset of the multiplier. If there are input referred DC offsets at the inputs of the multiplier, its transfer function is

$$z = (x + a)(y + b) = xy + ax + ay + ab \tag{3.7}$$

where *a* and *b* are the DC offsets, and *x* and *y* are sinusoid signals of the same frequency. The first term in (3.7) will generate the desired DC output. The last term is another DC term that can be cancelled through calibration. It will not ruin the DC output. The first term will also generate AC interference at the double frequency point. This, along with the 2^{nd} and 3^{rd} terms in (3.7), will be suppressed by the integrators in Figure 3.4. As a result, only the desired DC signal is presented at the output.

This architecture is also immune to the multiplier's odd order nonlinearities. These nonlinearities only introduce the harmonics at multiples of the stimulus frequency and the integrators in Figure 3.4 can suppressed them. However, the even order nonlinearities of the multipliers will generate interference DC signals and affect the resolution of this FRA based system. 3^{rd} order and 4^{th} order nonlinearities are the most significant non-ideal effects in an analog multiplier. Their effects on the accuracy of the FRA based system are discussed below.

Assuming the multiplier in Figure 3.4 has 3^{rd} order and 4^{th} order nonlinearities, its transfer function can be expressed as,

$$
\begin{aligned}
& z = xy \\
& +k_{31}x^2y + k_{32}xy^2 + k_{33}x^3 + k_{34}y^3 \\
& +k_{41}xy^3 + k_{42}x^2y^2 + k_{43}x^3y + k_{44}x^4 + k_{45}y^4
\end{aligned} \tag{3.8}
$$

where x and y are sine signals with the same frequency. The first line shows the wanted multiplication function, and the 2nd and 3rd lines represent the unwanted nonlinear transfer function. All of the 3rd order nonlinearities (terms in the 2nd line of (3.8)) only generate non-DC harmonics, which can be suppressed by the integrators. Thus, the system is robust against 3rd order nonlinearities. This conclusion is also true for all other odd order nonlinearities. In (3.8), only xy and x^2y^2 terms generate DC components at the output. By substituting x and y with $Asin(\omega t+\varphi)$ and $sin(\omega t)$ and only including xy and x^2y^2 terms, we get,

$$
\begin{aligned}
z &= xy + k_{42}x^2y^2 = A\sin(\omega t+\phi) + k_{42}\sin^2(\omega t+\phi)\sin^2(\omega t) \\
&= \frac{A}{2}\cos(\phi) + k_{42}A^2\frac{\cos^2(\varphi)+1}{2} + F
\end{aligned} \tag{3.9}
$$

where F represents the non-DC terms, and will be suppressed by the integrators. The first DC term in (3.9)'s result is the real part information of input signal (see (3.2)). The second DC term is a product of the 4th order nonlinearity (x^2y^2). We can see that the output is accurate as long as k_{42} is much smaller than the first DC term. Higher even order nonlinearities also produce a DC term in (3.9), but their effect should be much smaller than 4th order one. To keep these nonlinear terms at DC in (3.9) small enough, the even order harmonics of multiplier should be controlled.

For the analog multiplier circuit, it is hard to achieve very high linearity. However, with some balanced structures, it is easy to suppress the even order nonlinearities to the

point where they can be ignored. Normally, for a balanced analog multiplier structure, odd order harmonics dominate the linearity performance. That kind of non-linearity does not affect the accuracy of the result because the integrators employed in an FRA based system illuminate their effects.

3.3 Proposed biosensor array based EIS microsystem

Considering the above discussion on FFT-based and FRA-based IS systems, we have obvious reasons to choose the FRA-based IS system as the architecture for our EIS system. As shown in Figure 3.4, a quadrature sinusoid signal generator is necessary for a stand-alone EIS system based on the FRA structure. For the tBLM biosensor, the frequency range of interest is from 1mHz to 10kHz (TABLE 3.1). Thus an on-chip quadrature sinusoid signal generator is developed to cover this range. Two possible interrogation systems will be proposed based on the FRA architecture in Figure 3.4. One system targets the rapid interrogation for low frequencies measurement. Normal FRA methods require a long interrogation time at low stimulus frequencies (sub Hz or lower) because the integrator in Figure 3.4 requires at least half of a stimulus cycle to eliminate the AC interference. The proposed method tries to avoid the use of this integrator in AC interference elimination. A second system is based on a compact IS circuit to support the multichannel, high accuracy EIS system. The performance and feasibilities of these two systems will be studied, but in the end, only one of them was chosen as the prototype electrical system for the biosensor array microsystem.

3.3.1 Rapid response IS systems

3.3.1.1 Delay in EIS systems

In an FRA based EIS system, the total response time of the system is decided by two factors. One is the delay of the biosensor; the other is the delay from the interrogation system. These will both be analyzed to determine where the bottleneck occurs.

Potentiostat systems interface with biosensors and translate their electrochemical response into electrical information. For a frequency range of less than 10kHz, the electronics introduce only a negligible delay. The potentiostat delay is mainly due to the biosensor delay. For an EIS system, we need to vary stimulus frequencies to sweep across all of the interested frequency points. The biosensor delay determines the settling time of the frequency transition. We will take the tBLM biosensor as an example to study these delays. Its circuit model is redrawn with a sinusoid voltage source in Figure 3.5. Assuming that the sinusoid voltage source frequency changes from ω_0 to ω_1 at t=0, then we can get the current response as

$$I(t) = \frac{A_5}{(C_1+C_2)} e^{-\frac{1}{R_M(C_1+C_2)}t} + A\cdot\sin(\omega_1 t+\varphi) \qquad (3.10)$$

where A_5 is a constant determined by ω_0 and ω_1, and A, φ are the amplitude and phase of the response current. For the detailed derivation of (3.10) please see Appendix. (3.10) shows that in addition to a stable response signal at frequency ω_1 (second term), there is also a term(first term) embodying the transition effects. The first term will die out eventually with a time constant of $R_M(C_1+C_2)$. The settling time of a frequency change is proportional to this time constant. For typical values of the tBLM biosensor [60], this

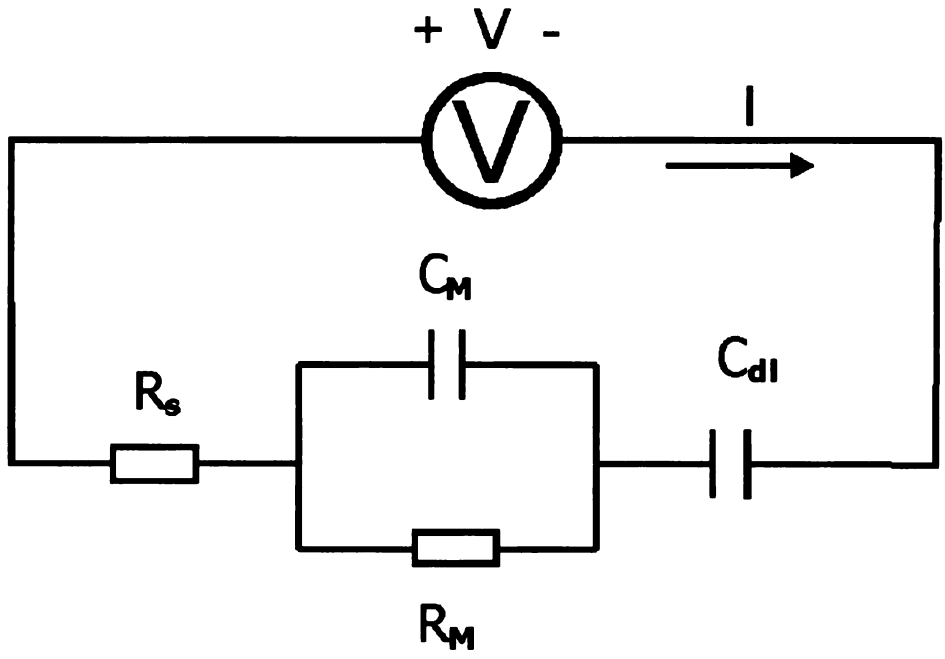


Figure 3.5. Equivalent circuit model for tBLM biosensor.

time constant is about 0.25 sec. So, there is up to a several seconds waiting time for the EIS system to read a stable output after a frequency change.

For the FRA based IS system (Figure 3.4), the integrator takes times to suppress the double frequency AC interference. As shown in Figure 3.6, the averaged DC components remain constant regardless of the integration time. However, the AC interference dies out exponentially as integration duration increases. Because the AC component crosses over the zero point at multiples of half a period of the stimulus frequency, we can minimize the interrogation response time by tightly controlling the integration duration to be half of a period of the stimulus. However, the delay is still large for very low frequency measurement. For example, if 1mHz is the frequency of interest, the minimum integration duration is 500 seconds (about 11min). Compared with the several second delay of a typical tBLM biosensor in frequency transition, the delay of the EIS

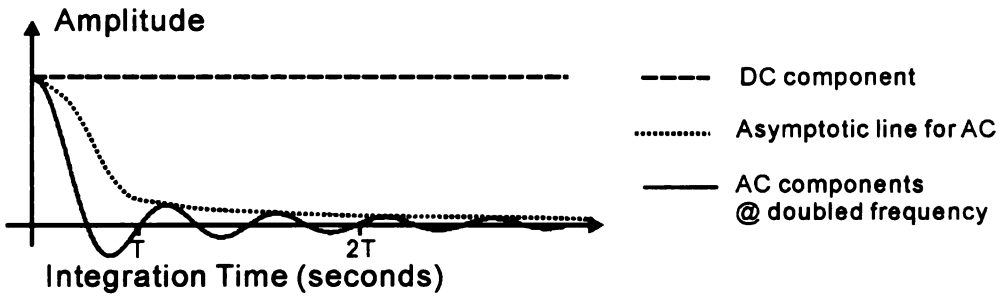


Figure 3.6. The DC and double frequency AC interference in the integrator output.

interrogation system is dominant. It becomes worse if multiple low frequencies are selected and the large scale biosensor array is interrogated. To overcome this problem, a fast EIS architecture is proposed.

3.3.1.2 Rapid EIS systems

As discussed in the previous section, the integrator is the bottleneck causing the long delay for low frequency EIS interrogation with a conventional FRA based system. Thus, to improve the interrogation speed, a new architecture eliminating the integrator for AC interference suppression is proposed. The principle block diagram of this system is shown in Figure 3.7. Instead of interrogating single elements, as in a conventional FRA based EIS system, this new method interrogates two identical biosensor elements simultaneously with in-phase and quadrature phase sinusoid stimuli of the same frequency. Then, complex domain (dealing with signals having real and imaginary parts) signal processing is done to extract the real and imaginary part of the biosensors' admittance. No integrator is required in this new system.

To explain this system mathematically, assume that we have two identical biosensor elements. For the configuration in Figure 3.7(a), the summation operation at the output is expressed as

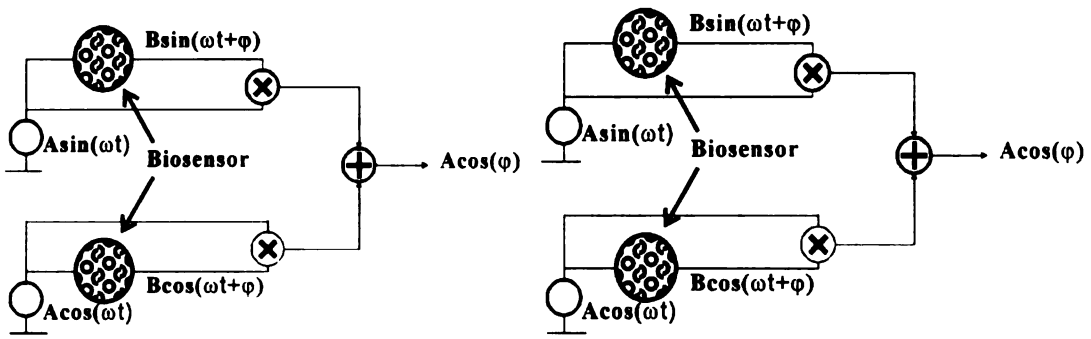


Figure 3.7. The principle block diagram of the fast interrogation EIS system: (a) the configuration to produce the real portion of the admittance, (b) the configuration to produce the imaginary portion of the admittance.

$$A\sin(\varphi)B\sin(\omega t+\varphi)+A\cos(\omega t)B\cos(\omega t+\varphi)=AB\cos(\varphi) \qquad (3.11)$$

This result is the real part of the admittance. Similarly, for the configuration in Figure 3.7(b), the subtraction at the output is expressed as

$$A\cos(\varphi)B\sin(\omega t+\varphi)-A\sin(\varphi)B\cos(\omega t+\varphi)=AB\sin(\varphi) \qquad (3.12)$$

which is exactly the imaginary part of the admittance.

(3.11) and (3.12) show that the stable outputs are presented at the output of the EIS system as long as the biosensors' responses are stable. Thus, only the biosensors' delays appear in the frequency transition. The elimination of the integrators greatly improves the interrogation speed for low frequencies. Due to this dramatic improvement in the interrogation speed, this system can scan the whole biosensor array sequentially in a reasonable time. We can use just one this system and use multiplexer to access all the array elements. The system level block diagram for the rapid EIS based biosensor array microsystem is shown in Figure 3.8. The signal generator provides the sinusoid stimulus for the biosensors and the reference signal for the IS circuit. A multiplexer is employed to

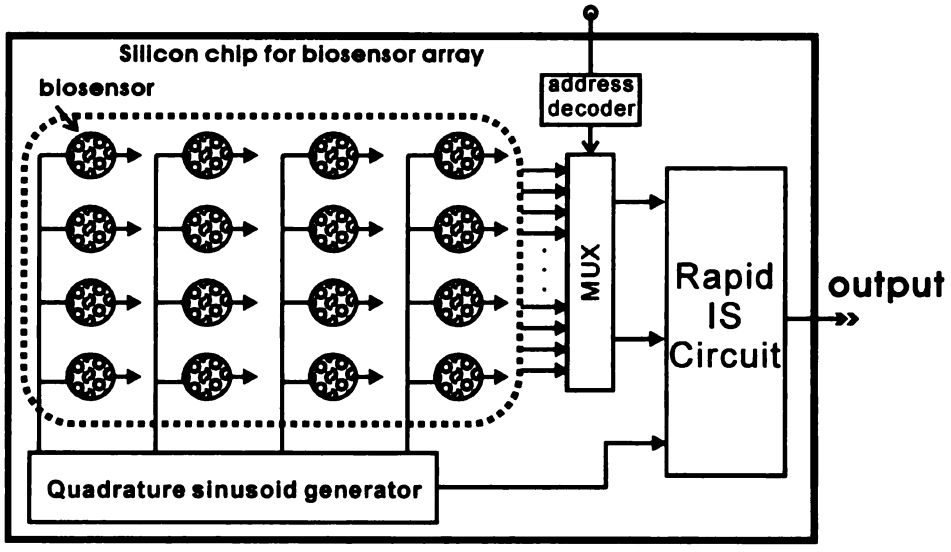


Figure 3.8. The principle block diagram of the fast EIS microsystem.

pick up the desired sensor element pairs for the EIS circuit. All electrical components can be integrated on a single silicon die.

3.3.1.3 Accuracy limitation due to non-ideal effects

(3.11) and (3.12) show that the AC interference can be completely canceled. However, this is based on the assumption that all components are ideal. The mismatches between the biosensor and the readout circuit (analog multiplier) will result in the leakage of AC interference at the output and affect the accuracy.

Error due to biosensor mismatch

This rapid EIS system requires two identical sensor elements. In reality, mismatch between sensor elements is unavoidable, and it will limit the accuracy. For a sensor pair with a certain admittance mismatch, the effect of sensor mismatch can be studied by comparing the mismatch and the value of the biosensor admittance. Relative error is defined as the ratio,

$$Relative\ error = \frac{\left|Y_1 - Y_2\right|}{\left|Y_1\right|} \tag{3.13}$$

where Y_1 and Y_2 are the admittance of two biosensors. The admittance can be expressed with a magnitude and phase pair (A,φ).The relationship between relative error and mismatch is plotted in Figure 3.9. Output signals are always digitized before further processing. In order to relate the relative error to the resolution of the digital signal, the vertical axis on the right reveals how many bits of resolution we can achieve. Specifically, it shows that the mismatching error could be 15% of the base impedance values with a 5° phase mismatch and 20% magnitude mismatch in admittance.

By relating the mismatch of the components in the circuit model of an electrochemical biosensor to that of the magnitude and phase of the biosensor, we can

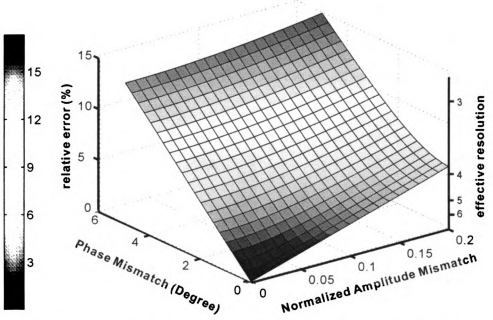


Figure 3.9. Output relative error versus the different levels of mismatch in amplitude and phase of two identical biosensors, and the equivalent resolution in terms of digital presentation.

have more of a sense of the degree of mismatch for the real biosensors. Again, we take the tBLM biosensor as an example. The phase and magnitude changes due to changes in the individual circuit model components are studied by changing every component's value up to 20%. The admittances at a frequency of interest (1Hz, where *Rm* shows up in the model) are taken. The result is plotted in Figure 3.10. Several conclusions are drawn:

- *Cdl* and *Cm* have limited effects on the magnitude change. There is a less than 5% change with a 20% change in *Cdl* or *Cm*.

- *Rm* has a dominant effect on the magnitude change. A 20% change in *Rm* results in nearly a 14% change in magnitude.

With tBLM biosensors, a good match between the *Cdl* components (electrode and solution double layer capacitor) of different biosensors can be easily achieved. This is because *Cdl* depends on the area of the solid electrode, which can be accurately controlled during manufacturing. In addition, *Cm* contributes less than a 1% effect with a 20% mismatch. As a result, a mismatch of *Cdl* and *Cm* results in a relatively low error for

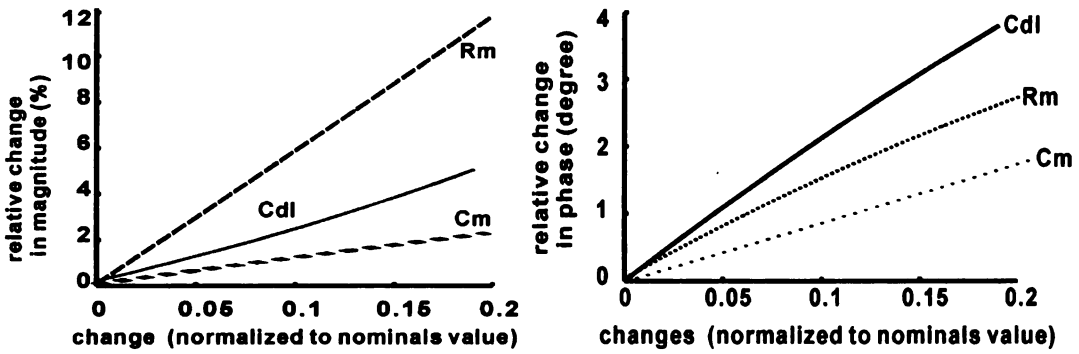


Figure 3.10. Magnitude and phase changes due to a change of up to 20% in component values found in the tBLM biosensor circuit model. The base values for the components are Rm=50KOhms, Cm=0.5uF and Cdl=5uF.

tBLM biosensors at a frequency of interest. The mismatch of the *Rm* component dominants the admittance mismatch. However, a 20% base value mismatch is tolerable during measurement because amplitude always changes several decades at a frequency of interest[61].

Due to this mismatch effect, the fast interrogation method can not achieve a high resolution. However, with the above analysis, moderate accuracy (around six bits) is feasible. For some qualitative interrogation situation, for example, detecting whether or not certain elements is present, three bits of resolution can give enough information. Thus, this method can also be applied for a badly matched sensor pair in these situations.

Error due to circuit mismatch

The gain mismatch and the input referred offset of the multipliers will affect how effectively AC interference can be eliminated. To study the effects of both the gain mismatch and the input referred offset,, we will rewrite equation (3.11) for the system diagram in Figure 3.7, including the offset and gain mismatch of the multiplier. It is,

$$\begin{aligned}&\left[A\sin(\omega t)+V_{OS1}\right]\left[B\sin(\omega t+\phi)+V_{OS12}\right]+(1+\alpha)\left[A\cos(\omega t)+V_{OS21}\right]\left[B\cos(\omega t+\phi)+V_{OS22}\right] \\ &=AB\cos(\phi)+kAB\end{aligned} \tag{3.14}$$

where *Vosij* represents the input referred offset of the ith input of the jth multiplier, and α represents the gain mismatch of the multipliers. On the right side of (3.14), the first term is the wanted result. The second term is the error due to mismatch and the offset of the multipliers. *k* is a parameter determined by the multiplier's mismatch and is expressed as

$$k = \alpha\cos(\omega t)\cos(\omega t+\phi) + \frac{V_{OS11}}{A}\sin(\omega t+\phi) + \frac{V_{OS11}V_{OS12} + (1+\alpha)V_{OS21}V_{OS22}}{AB} + \frac{V_{OS12}}{B}\sin(\omega t) + (1+\alpha)\left(\frac{V_{OS22}}{B}\cos(\omega t) + \frac{V_{OS21}}{A}\cos(\omega t+\phi)\right) \quad (3.15)$$

k shows the relative error due to the multipliers' mismatch compared with the wanted output, or the first term in (3.14). The expression for *k* in (3.15) illustrates that *k* is determined by the multiplier gain mismatch and the relative input referred offset compared with the amplitude of the input signal. Because there are so many terms in (3.15), even a very small gain mismatch and offset results in a significant error. More than 30% relative error (k) is observed when only a 5% gain mismatch and a 5% relative input offset is applied on (3.15). We should observe the same error level if we rewrite (3.12) with the gain mismatch and offset of the multiplier.

This observation almost excludes the analog solutions for the multipliers. The large gain mismatching (more than 5%) of two analog multipliers [64-71] is expected. Furthermore, an input referred offset of more than 10mV is very common for analog multipliers. In order to provide enough dynamic range of the input signal, we can not keep the input signal very large. Thus, the relative input referred offset can not be small. The solution is to perform the multiplication in the digital domain, where the multiplier gain mismatch and offset can be minimized to zero. At the system level, the sensor's response should be digitized with an ADC, and all other signal processing performed in the digital domain with the help of a DSP.

3.3.1.4 Summary of the rapid response EIS system

A new EIS system was developed to significantly improve the interrogation speed at low frequencies (sub-Hertz or lower). It eliminates the AC interference suppression integrators used in a conventional FRA based IS system to improve the speed. The new system suppresses the AC interference by coupling two biosensors' responses. The measurement accuracy of the new system is strongly affected by the matching of the biosensor and readout channels. Digital domain signal processing is recommended to achieve the readout channel matching. As a biological system, biosensors always have poor matching. However, the biosensor mismatch for some type of sensors, e.g. tBLM protein biosensor, is tolerable. We can extract the desired impedance information with a moderate level of accuracy from these biosensors. If the matching of biosensors can be improved significantly in related research, this method can work for wider range of biosensors. In this dissertation, we would not realize this system due to its limited accuracy.

3.3.2 Multi-channel compact high accuracy EIS systems

Although integrators in FRA-based IS systems (Figure 3.4) introduced large delays for low frequency interrogation, the system provides the high accuracy result with the circuit non-idealities. Section 3.2.2 has discussed the non-ideality tolerance in detail. Analog and mixed-signal ICs can realize the FRA-based IS system with a very compact size. Just as any analog circuit system, this realization will have many circuit level non-idealities. The integrators in this system will suppress these effects significantly and help to guarantee high accuracy. Based on this understanding, an EIS system featuring multi-channel parallel interrogation was developed. For biosensor array screening, the long

interrogation delay for low frequencies can be alleviated by simultaneous in-parallel interrogation.

3.3.2.1 Electrical system of the multi-channel high accuracy EIS

Figure 3.11 shows the electrical system of the multi-channel EIS, in which the compact IS circuit is built and instantiated for every biosensor element in the array. A quadrature sinusoid signal generator is also employed in this system to provide the sinusoid stimulus for the biosensor and the reference signal for the IS circuit. With advances in the development and microfabrication of the biosensors, the scale of the biosensor microarray can reach hundreds or even thousands of elements. Due to the limited number of PADs on the silicon die, it is not feasible to reserve dedicated pads for every unit readout channel to send out the interrogation result. Thus, the unit IS circuit needs not only to extract the impedance information from the biosensor, but also to digitize the extracted impedance information. The digitized results can be put into a global shifter bank so that the impedance information of all the active channels can be read out through the same serial data interface PADs.

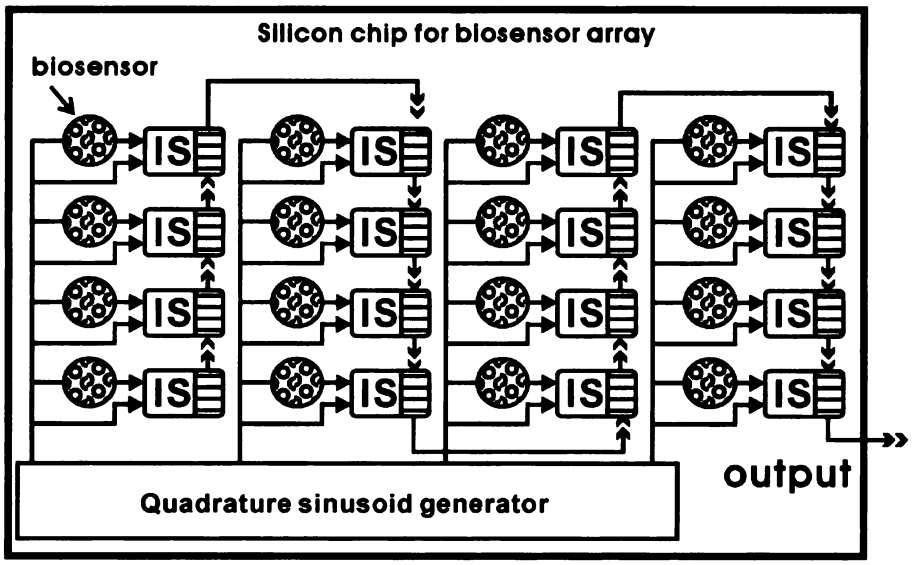


Figure 3.11.The principle block diagram of the multi-channel EIS microsystem.

3.3.2.2 Rapid interrogation of tBLM biosensors

For tBLM biosensors, shown in Figure 3.1, the impedance value is dominated by Rm (the sensing parameter) at low frequencies. Thus, low frequency IS is conducted to extract the value of Rm. The FRA structure based compact EIS system will have a long interrogation time at low frequencies. A new method that extracts the value of Rm of tBLM biosensors with high frequency IS is developed so that the rapid interrogation can also be achieved with this compact EIS system for tBLM biosensors.

For the circuit model in Figure 2.1(b), the admittance of the tBLM biosensors is

$$Y(\omega)=\frac{1}{\frac{1}{g_M+j\omega C_M}+\frac{1}{j\omega C_{dl}}}=\frac{\frac{g_M}{g_M^2+\omega^2C_M^2}+j\left(\frac{\omega C_M}{g_M^2+\omega^2C_M^2}+\frac{1}{\omega C_{dl}}\right)}{\left(\frac{g_M}{g_M^2+\omega^2C_M^2}\right)^2+\left(\frac{\omega C_M}{g_M^2+\omega^2C_M^2}+\frac{1}{\omega C_{dl}}\right)^2} \quad (3.16)$$

At frequencies where $g_M<<\omega C_M$, (3.16) this becomes,

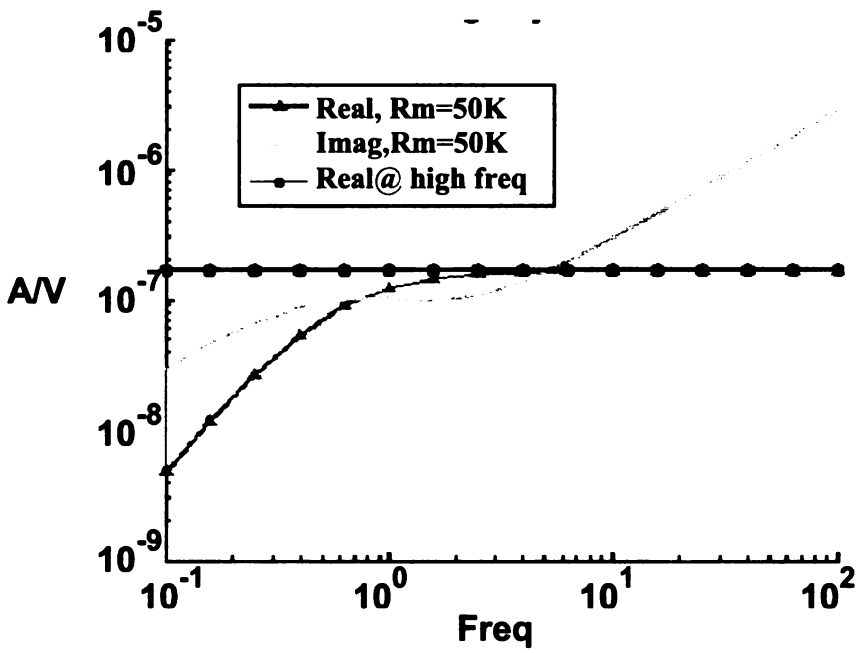


Figure 3.12. A plot of the real and imaginary admittance of a tBLM biosensor model.

$$Y(\omega) = \frac{g_M}{\left(1+\frac{C_M}{C_{dl}}\right)^2} + \frac{j\omega C_M}{1+\frac{C_M}{C_{dl}}} \tag{3.17}$$

For a given tBLM sensor, C_M and C_{dl} are constant. Thus, the real portion of admittance, which is proportional to g_M, is independent of frequency. A plot is shown in Figure 3.12 for a 1mm x 1mm tBLM biosensor (the typical parameters are R_M=50~500KOhms/CM^2, C_M=500nF.CM^2 and C_{dl}=5uF.CM^2).

In Figure 3.12, the dotted black line represents . The real portion of the admittance approaches this dotted line after about 10Hz. Thus we can measure the real portion of admittance above 10Hz, and deduce the g_M. Although higher frequencies may also be picked, the accuracy will be less at those frequencies because both the imaginary portion

and the admittance increase with frequency. Extracting the small real portion from the much larger admittance reduces accuracy.

3.3.2.3 Summary of multi-channel high accuracy EIS systems

The compact, high accuracy EIS systems provide a multi-channel IS solution for biosensor array microsystems. Its structure is based on the FRA. The analog/ mixed-signal IC realization of this system can provide the compact size. The internal integrator makes the system robust against the real analog circuit non-idealities and guarantees accurate results. Further, this system does not impose any matching constraints on biosensors as rapid EIS system does. It works for all kinds of miniaturized biosensors. Although it still has a long interrogation time for low frequencies, simultaneous in-parallel multi-channel interrogation alleviates the issue significantly for whole array impedance scanning.

3.4 VLSI implementation for the multi-channel EIS system

Two possible system solutions for the biosensor microarray interrogation EIS system have been discussed in this chapter. Our conclusion is that a compact, multi-channel, high accuracy EIS system is a better choice for an EIS biosensor array microsystem because it can support a wider range of biosensor types and provide accurate results in spite of circuit non-ideality. For an on-chip electronic system, this is a very important feature because we lose the freedom in choosing the best performance electronics that exists with bench-top instruments. Limited choices for on-chip electronics always meant more circuit non-ideality. Thus, robustness to circuit non-ideality becomes very critical for an on-chip electronic system.

In the rest of this dissertation, the feasibility of a VLSI realization of a multi-channel EIS system will be explored. The main challenge in a VLSI realization is to provide all the required functions and performance within a limited physical size budget. Two key functional blocks will be studied: a channel-wise impedance extraction and the digitization circuit cell, and a wide frequency range quadrature sinusoid signal generator.

3.4.1 Compact impedance extracting and digitizing circuit

In the multi-channel EIS system, the impedance extraction and digitization circuit cell is instantiated for every sensor element in the array to provide massively parallel interrogation capability. With most of the chip area on top of the die populated by biosensor elements, the circuit cell must be compact enough to be fit into the space budget underneath every sensor element. With the increasing scale of the array, this physical area budget could be very tight. As discussed earlier in this chapter, this circuit cell not only provides the impedance extraction function, but also needs to digitize the extracted impedance information. Further, it needs to provide a shift register bank to stream out the interrogation result of the entire array with limited I/O pad resources. Chapter 4 will study this readout channel in detail and present a compact solution meeting the requirements that was developed and fabricated.

3.4.2 Quadrature sinusoid signal generator

For a stand alone FRA-based IS microsystem, a quadrature sinusoid signal generator is necessary. It needs to produce a pair of sinusoid outputs with the same frequency and amplitude, but with a 90° phase shift (in-phase & qudrature-phase signal or I&Q signals) over 7 orders of frequency range (1mHz -10KHz) with good frequency accuracy. Furthermore, good matching between the I & Q signals is also very important

for accurate results. So far, there have not been any publications that achieved sinusoid generation with accurate frequency control over such a wide frequency range. Although its physical size budget is not as tight as that of the channel-wise unit impedance readout circuit cell, the limited available chip real estate excludes some realization options and puts forth more challenges for implementatoin. A hybrid structure and VLSI realization of a prototype quadrature sinusoid signal generator is described in Chapter 5. It inherently guarantees good I&Q matching. Moreover, it is completely controlled by digital signals to achieve high frequency resolution and permit easy interface with a computer.

4 Compact On-chip Impedance Spectroscopy

In this chapter, a very compact impedance spectroscopy (IS) system and circuit will be developed and built. Its working frequency range is from 1mHz to 10kHz. It provides digitized information of a sensor's impedance response. A new analog-to-digital (ADC) circuit structure is proposed to build this compact IS circuit. In contrast to a traditional ADC, which converts an instantaneous analog value into a digital value, this ADC converts the phase and amplitude information of a sinusoid input into the digital domain. We will refer to this circuit as a "lock-in ADC" because it needs a reference clock to extract impedance information in a manner that is similar to a lock-in amplifier [72]. The principle operation of the lock-in ADC is shown in Figure 4.1. Its input (*Ix*) is a sinusoid current, which is the current response of a biosensor to a sinusoid voltage stimulus

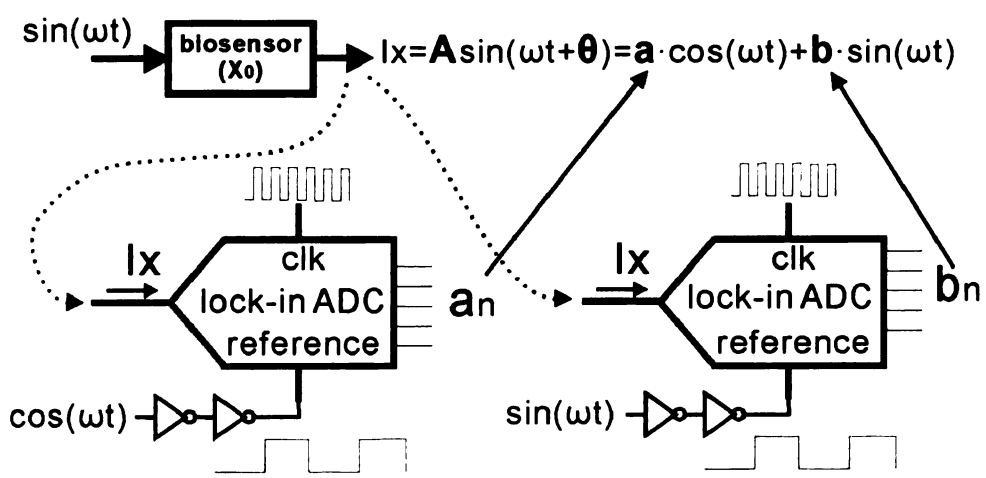


Figure 4.1. The lock-in ADCs extract and digitize the impedance information of a biosensor.

($sin(\omega t)$). The amplitude (A) and phase (θ) of Ix carry the sensor's impedance information. Ix can also be represented as the sum of cosine and sine components.

$$Asin(\omega t+\theta)=a\cdot cos(\omega t)+b\cdot sin(\omega t) \tag{4.1}$$

The coefficients in (4.1) represent the imaginary and real parts of the biosensor's admittance (the reciprocal of impedance), respectively. The relationship between these coefficients and the amplitude (A) and phase (θ) information is

$$\begin{cases} a=Asin(\theta) \\ b=Acos(\theta) \end{cases} \tag{4.2}$$

As shown in Figure 4.1, the lock-in ADC digitizes the sensors' admittance information, i.e. a or b in (4.1). It needs a square wave reference signal that is either in phase with the sine component or in phase with the cosine component. If the reference signal is in phase with the sine component, the digital output is the coefficient of the input current's sine component. In the other case, the digital output is the coefficient of its cosine component. Digital counters are employed inside the lock-in ADC. These counters can be reconfigured to work as a shifter to perform the serial readout.

This compact IS circuit is set to be instantiated for each miniaturized element of the biosensor array microsystem. A principle block diagram for the electrical part of the micosystem is illustrated in Figure 4.2. Every biosensor has its own IS readout circuit cell. Due to limited pad resources in the integrated circuit package, it is impossible for every readout channel of a large scale biosensor array (around 100elements or more) to have a dedicated pad to output the extracted impedance information. Thus, a shift register is built within each IS circuit. The shift registers within each cell are connected together to

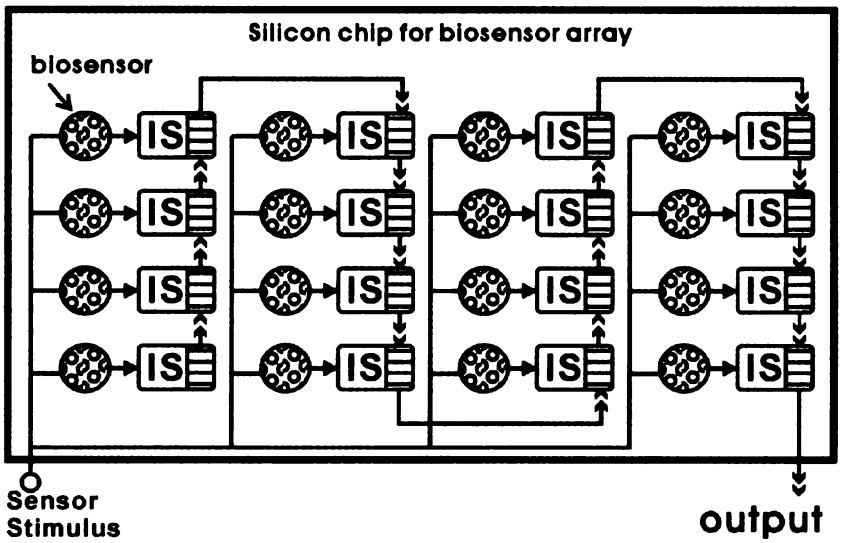


Figure 4.2. Block diagram of the biosensor array based microsystem.

form one large shifter such that the result of each IS circuit cell can then be accessed through a single set of serial data pads.

To fit the IS circuit cell with the area of each miniaturized biosensor element, a compact EIS system was developed. As shown in Figure 4.3, this EIS system incorporates an analog signal processing function, performing the FRA analysis, and the result quantization function, converting the output into digital domain and storing it. A new circuit architecture is proposed that permits the required functions to share hardware resources such that the layout size is minimized to fit to the individual sensor's size. Also, this new architecture eliminates non-ideal circuit effects, such as leakage, offset, and nonlinearity, to achieve high accuracy for low frequency interrogation.

The proposed compact architecture was built with a switched capacitor circuit. All other functions (digitization, integration, multiplication) are realized around it. Starting

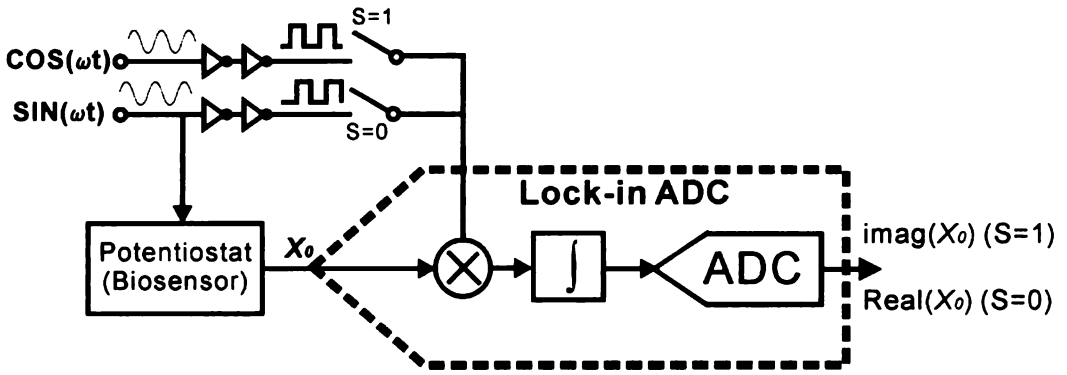


Figure 4.3. Functional block diagram of the proposed EIS system.

with the realization of the integrator, we will show the architecture step by step as it moves toward a fully integrated IS structure.

4.1 Integrator design

As discussed in Chapter 3, the integrator in an FRA removes the AC harmonics from the output of the multiplier. The inputs of the multiplier are two sinusoids of the same frequency. The frequencies of the harmonics at the multiplier's output occur at multiples of the input sinusoid frequency. By integrating the multiplier's output over one or more periods of the sinusoid signal, these harmonics can be suppressed completely.

An typical integrator for an FRA circuit would be composed of an op-amp and a capacitor in a feedback loop as shown in Figure 4.4. However, this structure is not suitable for an IS application because the range of signals that can be integrated is limited by the supply voltage. For a long integration time required for low frequency EIS interrogation (sub-Hertz or lower) or a large input current, the voltage on the capacitor could reach 1KV if the supply voltage were not limited. This is unrealistic for microelectronic components. In order to provide a wide output range with the analog integrator, current mode operation has been adopted in some literature [73, 74]. With a

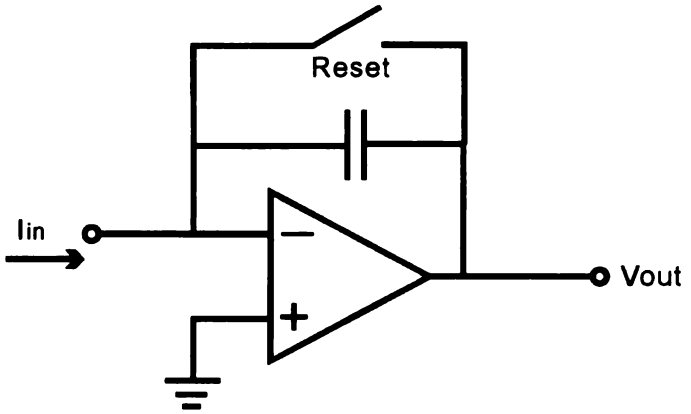


Figure 4.4. Simple integrator circuit.

current mode integrator, the integration result is actually stored on a capacitor as a voltage, which drives the gate of a MOSFET and converts the stored voltage information into the transistor's drain current. Although these current mode integrators provide a much wider output range compared to the one in Figure 4.4, they become problematic with a long integration time because 1) the charge on the storing capacitor will slowly leak, and this leakage becomes very significant for a long integration duration; 2) the output signal range could still be limited by the physical size of the output MOSFET; and 3) the power consumption budget also limits the current output range.

In this dissertation, a mixed-signal method is proposed to remove the limitations on the output range. The principle diagram of the new method is illustrated in Figure 4.5. It is based on the integrator in Figure 4.4. However, instead of storing the integration result solely on the capacitor as in Figure 4.4, this new method stores the result in both the digital and analog domains. It can provide a large output range because the digital representation (binary number) is very flexible with regard to range expansion.

In Figure 4.5, the capacitor and two counters are initially reset. During the integration, the input current is continuously fed into the integrator and charges

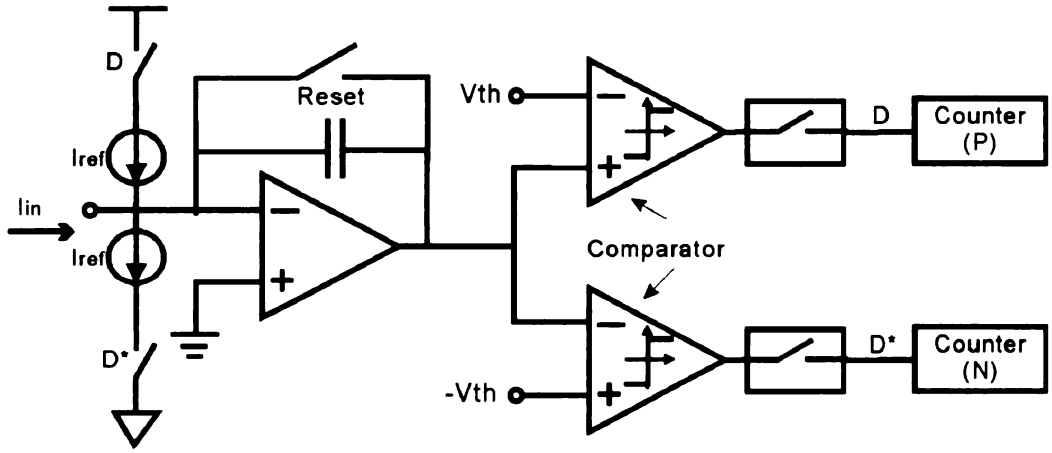


Figure 4.5. The mixed mode integrator diagram.

(discharges) the integrating capacitor. There are two comparators to set the lower boundary (*-Vth*) and upper boundary (*Vth*) of the integrator's output. Once the output is above this range the comparator outputs "1". The clock signal samples the 1's and feeds the proper reference current in at the input in order to subtract the absolute value of the voltage drop on the capacitor by a fixed amount in one clock cycle. The voltage change (ΔV) due to the reference compensation current is:

$$\Delta V = \frac{I_{ref} \cdot T_{clk}}{C} \tag{4.3}$$

where T_{clk} is the period of the clock. Meanwhile, two synchronized counters count the clocked output of the comparators. For example, if D becomes "1" at a clock edge, the counter (P) counts 1 and a ΔV is subtracted from the simple integrator's result. Alternatively, if $D^*=1$, the counter (N) counts 1 and a ΔV is added to the simple integrator's result. At the end of the integration, we have three values stored in the system: the simple integrator's analog output, and the two counters' outputs in the digital domain. Counter (P) and counter (N) store the number of D=1's and D*=1's respectively.

Applying the charge conservation theory for the integration process, we can recover the integration result expressed by

$$\frac{1}{C}\int_0^T I_{in}dt = V_{res} + \Delta V\sum D_i - \Delta V\sum D_i^* = V_{res} + \Delta V\left(\sum D_i - \sum D_i^*\right) \quad (4.4)$$

where V_{res} is the simple integrator's analog output at the end of integration, and $\sum D_i$ and $\sum D_i^*$ are the value of counter (P) and counter (N).

As this integrator is targeted for the long integration duration, the counter could overflow. In order to decrease the count for D and D*, Vth is set large and ΔV is chosen very close to Vth such that consecutive 1's at D and D* are minimized. Thus, this integrator can work with a very long integration duration (tens of seconds and greater) with a reasonably sized counter. Leakage could be a problem with the long integration time. However, in this proposed EIS solution, leakage is cancelled automatically and does not deteriorate the result. This will be detailed later in this chapter.

4.2 Analog-to-digital convertor

The proposed integrator already partially digitizes the result. If ΔV is taken as the reference unit, the digital output results of the new integrator represent the integer part of the digital output, which is the difference of the counter (P) and the counter (N) as shown in (4.4). The residue value at the simple integrator output represents the decimal part of the result if $\Delta V > V_{th}$. With an increase in integration time, i.e. more than one stimulus cycle, V_{res} becomes insignificant in (4.4). Thus, the counter (N) and the counter (P) already provide enough resolution, and we can ignore the residue analog output (V_{res}). The output of the ADC is just the difference of counter (P) and counter (N). In an EIS

application, a long integration time is always required due to the low frequency interrogations. For a high stimulus frequency, the integration can be performed for several consecutive stimulus cycles in order to extend the integration time. Thus, the analog to digital conversion is realized without any additional hardware other than the new proposed integrator itself.

4.3 Analog multiplication for EIS applications

The multiplier is employed in EIS system to extract the real part or imaginary part of the response. Its function is summarized in equations (3.3) and (3.4). The integrators that follow the multiplier pick out the DC components and suppress the AC interference (Figure 3.4). As long as the multiplier is a balanced structure, its linearity and offset are not critical in an FRA-based IS system because the integrator will suppress all AC interference that they introduce. For an unbalanced structure, the odd order harmonics will introduce error in the DC information (see the discussion in section 3.2.2). The consumption of both power and silicon area is very important because this IS circuit will be instantiated for every miniaturized biosensor element in an array. There are several options for an integrated CMOS analog multiplier. These options will be studied in this section, and a solution for the proposed EIS system will be proposed.

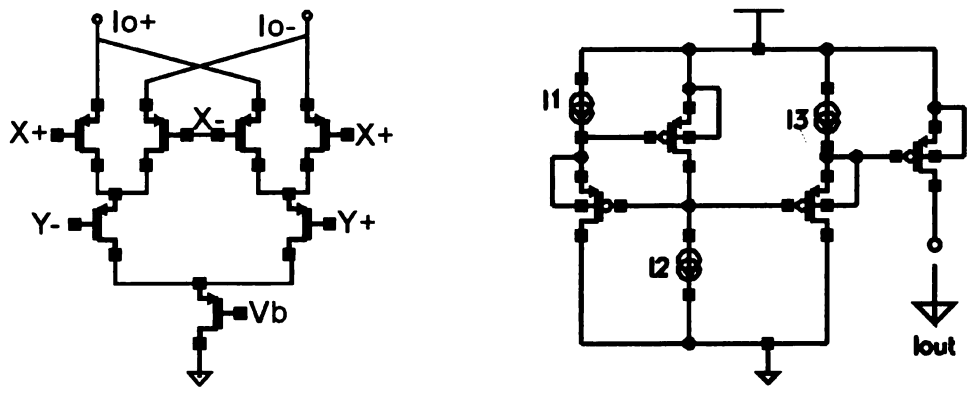
The most commonly used analog multipliers are ones built with CMOS transistors working within a strong inversion region [67-70]. These multipliers, based on the large signal models of CMOS transistors in a linear or saturation region, provide good linearity for large signals. Their offset is also small because transistors operating above threshold possess better matching performance. They achieve good performance with high power, which limits their application in a multichannel EIS system.

Because multiplier linearity and offset are not critical for an FRA-based EIS solution, analog multipliers working in the sub-threshold region, which have large nonlinearity and offset but consume small area and power, are better options. Figure 4.6(a) shows a Gilbert analog multiplier realized with CMOS in the sub-threshold region [75]. It is a balanced structure and works with a small bias current. Rairigh [76] proposed an EIS system with a similar sub-threshold CMOS analog multiplier. Another kind of sub-threshold CMOS analog multiplier is the CMOS translinear principle based multiplier [65]. One example of this multiplier is shown in Figure 4.6 (b). Its output can be expressed as,

$$I_{out} = \frac{I_1 I_2}{I_3} \tag{4.5}$$

where I1, I2, and I3 are the current sources shown in Figure 4.6(b). The problem with this structure is that it is not balanced and therefore it is not suitable for EIS applications.

Modulation based analog multipliers provide very good linearity and accuracy[66].



(a) (b)

Figure 4.6. The subthrehold multiplier: (a) Gilbert subthreshold CMOS analog multiplier, (b) CMOS translinear principle based multiplier.

They convert one input of the multiplier into time domain information (sequence of pulses) and modulate this with the other input. The penalty is the complicated hardware. Thus, they are not good solutions for an EIS system.

All of the above multiplier solutions provide multiplication between two analog inputs. As discussed in Chapter 3, for the FRA-based solution, the non-ideal effects of the analog multiplier are not a problem as long as the multiplier has a balanced topology. Thus, the chopping circuit in Figure 4.7, which has a balanced structure, could be a good choice. One of its inputs is a digital signal (X) that controls the two switches in Figure 4.7. At the differential output, the analog input signal (Y) is modulated by X. There are many frequency components at the differential output, but the component representing to the product of the two signals (X and Y) is located at DC. All of the other components are located at other frequencies and would be suppressed by the integrator in the overall EIS system. The principle is explained below.

Assume an integrator is used to integrate the differential output current in Figure 4.7. Let Y be the response of the biosensor in a EIS interrogation,

$$Y = B\sin(\omega t + \varphi) \tag{4.6}$$

Let X be a square wave with a 50% duty cycle. Its frequency is also ω and it is in phase with sin(ωt) such that

$$X = \mathrm{sgn}(sin(\omega t)) = \begin{cases} 1, & nT \le t < nT + T/2 \\ -1, & nT + T/2 \le t < (n+1)T \end{cases} \tag{4.7}$$

where T is the period of the stimulus signal. If the integration time is set to the period of the stimulus, the result of the integration is:

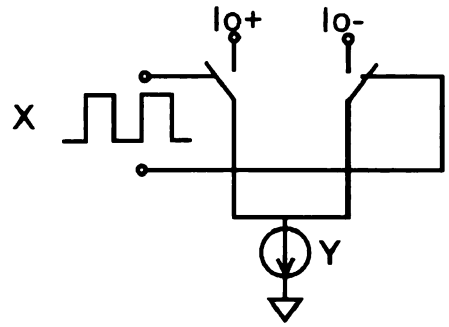


Figure 4.7. A simplified chopping circuit, Y is a current input, X is large square-wave signal.

$$I_{out} = \frac{1}{T}\int_0^T YX dt = \frac{1}{T}\int_0^{\frac{T}{2}} b\sin(\omega t + \varphi)dt - \frac{1}{T}\int_{\frac{T}{2}}^{T} b\sin(\omega t + \varphi)dt \tag{4.8}$$

Solving this integral, we get

$$I_{out} = \frac{b}{\omega T}\left[\cos(\omega T + \varphi) - 2\cos\left(\frac{\omega T}{2} + \varphi\right) + \cos(\varphi)\right] \tag{4.9}$$

Substituting ωT with 2π in (4.8), I_{out} becomes

$$I_{out} = \frac{b}{\pi}\cos(\varphi) \tag{4.10}$$

which is the scaled real part of the response current. Similarly, if the square-wave signal is in phase with cos(ωt), X is given by

$$X = \mathrm{sgn}(cos(\omega t)) = \begin{cases} 1, & nT \le t < nT + T/4 \\ -1, & nT + T/4 \le t < (nT + 4T/3) \\ 1, & nT + 4T/3 \le t < (n+1)T \end{cases} \tag{4.11}$$

Thus, the integration result is

$$I_{out} = \frac{1}{T}\int_0^T YX dt = \frac{2}{\pi} b\sin(\varphi) \tag{4.12}$$

which is proportional to the imaginary part of the response.

(4.6)-(4.12) show that the desired impedance information can be extracted through multiplying the analog response signal with a digital reference signal using a chopping amplifier. However, the chopping technique changes the direction of the signals (Y in Figure 4.7). For a compact IS system, the input signal is a sensor's current response to a sinusoid stimulus, and thus the direction of the sensor's response current can not be reversed directly. Although this current could be mirrored to generate a copy in the reverse-direction, resolution would be lost due to mirroring mismatch. Instead of building a dedicated chopping circuit for the multiplication function, the chopping multiplication function is incorporated into the analog integrator in this dissertation. The new integrator is shown in Figure 4.8. Instead of reversing the input current direction at the clock edge, the polarity of the integrator itself is reversed by flipping the integrating capacitor. During an integration cycle, the capacitor connects in one direction for the first half cycle and its direction is changed for the second half cycle. In terms of the charge on the capacitor, this flipping operation changes the direction of the input current. In short, this system (shown in Figure 4.8) changes the sign of the integrator instead of the direction of the input signal.

$\varphi 1$ in Figure 4.8 represents the reference square wave. At time 0, the integrator is reset. The multiplication integrator works from time 0 to time T, which is the period of the reference signal. Assuming $\varphi 1$ is in phase with $sin(\omega t)$, as shown in waveform (a) in Figure 4.8, and *Iin* is $Asin(\omega t+\theta)$, then *Vout* at time T+ (+ sign means after the rising edge of $\varphi 1$) is

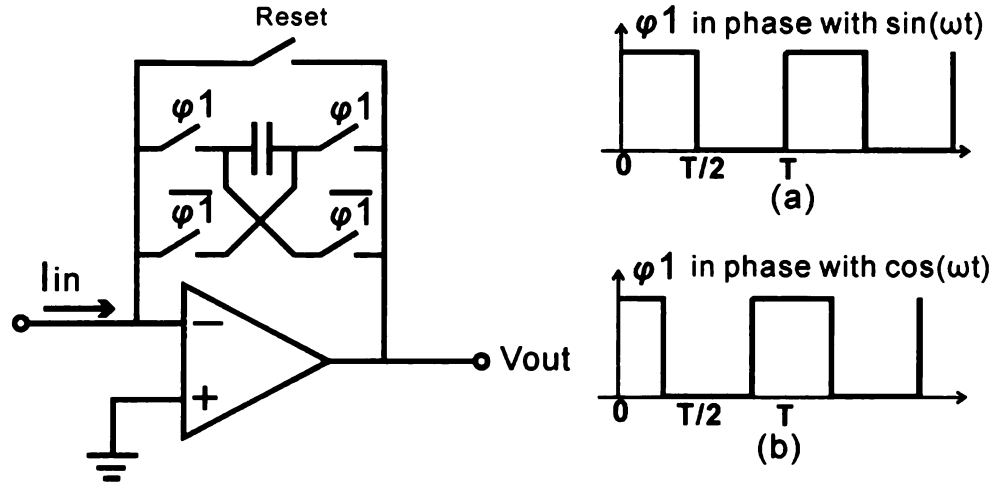


Figure 4.8. Multiplication integrator.

$$\text{Vout} = \frac{1}{C}\int_{0}^{T/2} \text{Iindt} - \frac{1}{C}\int_{T/2}^{T} \text{Iindt} = \frac{2T}{\pi C} Acos(\theta) \tag{4.13}$$

The result is proportional to real part of the input current signal. Similarly, if φ1 is in phase with $cos(\omega t)$, shown in waveform (b) in Figure 4.8, then *Vout* at time T+ is

$$\text{Vout} = \frac{1}{C}\left(\int_{0}^{T/4} \text{Iindt} - \int_{T/4}^{3T/4} \text{Iindt} + \int_{3T/4}^{T} \text{Iindt}\right) = \frac{2T}{\pi C} Asin(\theta) \tag{4.14}$$

The result is proportional to the imaginary part of the input current signal.

Saving chip area, this multipling integrator realized the multiplication function without any dedicated hardware for an analog multiplier. Another advantage of this circuit is that it is immune to the integrator's leakage. For a general analog integrator, the leakage current at the op-amp's negative input node will steal charge from the integrating capacitor, which results in a loss of information for periods of long integration. In the multipling integrator, the capacitor is flipped back and forth according to the square wave, and the leakage current steals charge from both plates of the integrator. Because the

voltage at the op-amp's negative input is fixed by the feedback loop, the leakage current is constant. With the 50% duty cycle square wave, this constant leakage current will steal the same amount of charge from both plates of capacitor, and its affect is canceled at the end of the integration.

4.4 Lock-in ADC

The realization of chopping techniques on a simple capacitor integrator (Figure 4.8) could also migrate to the proposed mixed-mode integrator to expand its output range and digitize its result, as shown in Figure 4.9. This block diagram shows the detailed system of the lock-in ADC shown in Figure 4.3. It is the core of the compact IS system.

φ1 in Figure 4.9 represents the reference square wave. The left portion of the circuit is the multipling integrator. The rest of the circuit is the digitizer. Similar to the mixed-mode integrator presented in Figure 4.5, two comparators and two reference currents (*Iref1* or *Iref2*) are used to digitize the integrator's output and keep it within the pre-

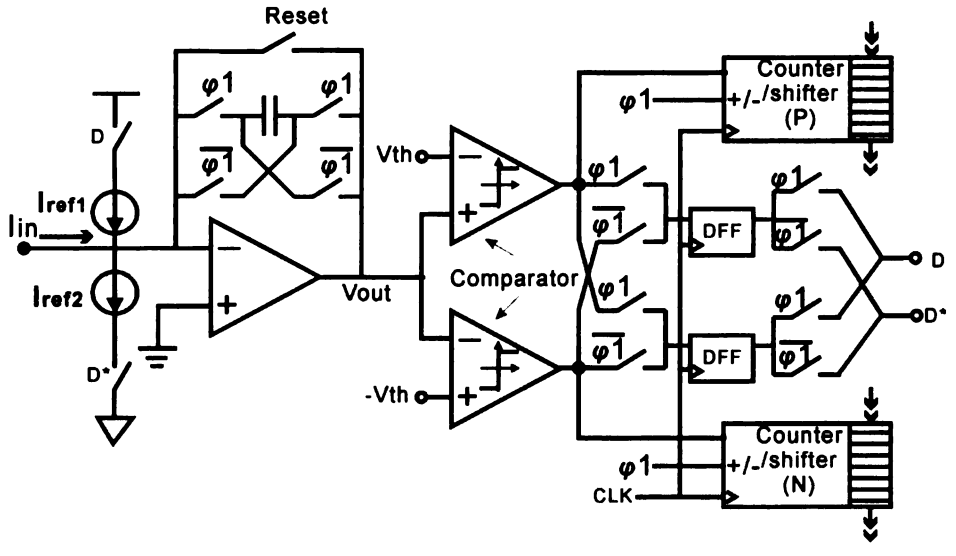


Figure 4.9. Block diagram of the lock-in ADC based IS system.

defined range. The system in Figure 4.9 requires two bidirectional counters to count the events on two comparator's outputs. Their counting mode (up/down counting) is controlled by $\varphi 1$. If $\varphi 1$ is high, the counter is configured as an up counter; if $\varphi 1$ is low, it is in down counting mode. At the end of a measurement, the contents of these two counters show the digitization result. The procedure will be detailed below.

There are two clock domains in this system, i.e, the updating clock (*clk* in Figure 4.9) and the chopping clock (φ in Figure 4.9). The former is a fixed frequency clock. The latter's frequency is equal to the stimulus frequency, which is variable. In some situations, this could result in error, and a method to deal with it will be discussed later.

To simplify the explanation of the operation of the lock-in ADC system, let's assume that at any $\varphi 1$'s transition edge, both D and D^* are low. The general case will be considered later. Suppose $\varphi 1$ is in phase with $sin(\omega t)$, as the waveform (a) in Figure 4.8. After resetting the counters and integrating capacitor at time 0, the integrator starts its work. $\varphi 1$ is 1 from time *0* to *T/2*. At time *T/2* (before the φ1's edge), based on the charge conservation theory for the input node, we have

$$\int_0^{T/2} \text{Iin}\,dt = \text{C}\square\text{Vres1} - \text{Iref1}\square\text{T0}\sum_1^N \text{Di} + \text{Iref2}\square\text{T0}\sum_1^N \text{D}_\text{i}^* \qquad (4.15)$$

where V_{res1} is the residue value at the integrator output, T_0 is the updating clock period, and N is the number of clock cycles from time 0 to *T/2*. During this period, counters are set to up counting mode because $\varphi 1$ is high. The counters are reset at time 0. At time *T/2*, the counter (P)'s content is the summation of the D_i's and that of counter (N) is the summation of the D_i^*'s. Both of the summations are included in (4.15).

At time *T/2*, the integrator capacitor is flipped. Immediately following, the integrator's output becomes ($-V_{res1}$). From time *T/2* to T^- (before the $\varphi 1$'s rising edge), the following equation holds

$$\int_{T/2}^{T} \text{Iindt} = C(\text{Vres1} + \text{Vres2}) - \text{Iref1T0}\sum_{N+1}^{2N} \text{Di} + \text{Iref2T0}\sum_{N+1}^{2N} D_i^* \qquad (4.16)$$

where V_{res2} represents the integrator's output voltage at time *T* (before the $\varphi 1$'s rising edge). ($V_{res1}+V_{res2}$) represents the voltage change from time *T/2* to *T*. After $\varphi 1$'s rising edge at time *T*, the integrator capacitor is flipped back, and integrator's output becomes ($-V_{res2}$). During this half cycle, the counters initial values are $\sum_{1}^{N} \text{Di}$ and $\sum_{1}^{N} D_i^*$, respectively; and both counters are set to down counting mode because φ1 is low. At the end (time *T*), counter (P)'s content is $\left(\sum_{1}^{N} \text{Di} - \sum_{N+1}^{2N} \text{Di}\right)$ and that of counter (N) is $\left(\sum_{1}^{N} D_i^* - \sum_{N+1}^{2N} D_i^*\right)$. To show the result over the entire cycle, we must subtract (4.16) from (4.15), which gives ,

$$\begin{aligned} &\int_{0}^{T/2} \text{Iindt} - \int_{0}^{T/2} \text{Iindt} \\ &= -C\text{Vres1} - \text{Iref1T0}\left(\sum_{1}^{N} \text{Di} - \sum_{2N+1}^{2N} \text{Di}\right) + \text{Iref2T0}\left(\sum_{1}^{N} D_i^* - \sum_{2N+1}^{2N} D_i^*\right) \qquad (4.17) \\ &\approx -\text{Iref1T0}\left(\sum_{1}^{N} \text{Di} - \sum_{2N+1}^{2N} \text{Di}\right) + \text{Iref2T0}\left(\sum_{1}^{N} D_i^* - \sum_{2N+1}^{2N} D_i^*\right) \end{aligned}$$

From (4.13) we know that the left side of (4.17) is proportional to the coefficient of the real portion of the input signal. The right hand side of (4.17) shows that the result is composed of the residue value on integrator and the contents in the two counters. Because we chose the parameters such that $|CV_{res1}| < \frac{1}{2}\max(I_{ref1}T_0, I_{ref2}T_0)$, we can ignore the analog residue portion and treat it as noise. Thus, the real portion information is presented digitally by two counters. The digitalized real portion coefficient can be recovered by

$$A=\text{Counter (N)}-k1*\text{Counter(P)} \tag{4.18}$$

,where *k1* counts for the mismatching of two reference currents (*Iref1* and *Iref2*). Calibration is needed to find *k1* for an accurate readout. The calibration method will be discussed later in the dissertation.

Similarly, if $\varphi 1$ is in phase with $cos(\omega t)$, the counter's results carry the digitized imaginary coefficient information of the input signal.

We assumed that both *D* and *D** were low at the transition edge of $\varphi 1$. Now we will

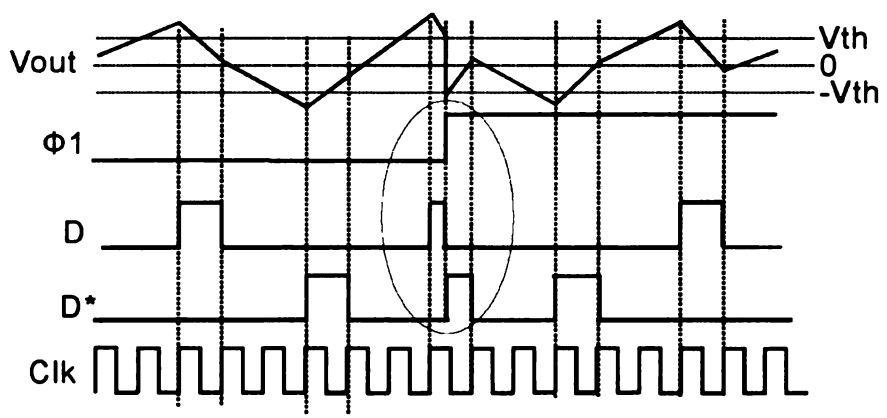


Figure 4.10. Waveform of the compensation current control signal (D and D* in Figure 4.9), for D and D* are low on the flipping of the capacitor.

discuss the case where D or D^* is high at the transition edge of $\varphi 1$. When either of them is high, they require a fixed amount of compensating charge to draw the integrator's voltage output back into the range during a clock cycle by controlling the reference currents. If the integrator capacitor's polarity is changed due to $\varphi 1$'s edge during the process, the polarity of this charge should have also been reversed accordingly. Otherwise, it would result in an error up to one digitized step. To take care of this issue, multiplexing switches at the inputs and outputs of the D-flip flops are inserted as shown in Figure 4.9. If D is high when $\varphi 1$'s rising edge comes, these switches will provide the waveforms shown in Figure 4.10. When φ1's edge arrives, D is high. It charges the integrator with I_{ref1}. After $\varphi 1$'s edge, D goes low and D^* becomes high, which will charge the integrator with I_{ref2}. I_{ref1} and I_{ref2} are set to be equal. This switching between I_{ref1} and I_{ref2} changes the polarity of the charge to match that of the integrator capacitor because the two currents have the same values but different polarities. The waveform of the integrator's output is also plotted in Figure 4.10. Practically, there is still a mismatch between these two currents, but it can be easily controlled to within 1%. As a result, this feature suppresses the error to be much smaller than one digitized step.

$k1$ in (4.15) represents the mismatch between I_{ref1} and I_{ref2}. We need to extract $k1$ for the real circuit to accurately recover the impedance information based on (4.15). If only a DC current is injected into the system in Figure 4.9, it will charge two plates of the integrating capacitor equally because every plate is connected to the input for 50% of the conversion process. As a result, its effect is canceled completely for any frequency of $\varphi 1$. Thus, the counters result should give a zero with (4.18) and $k1$ is found by

$$k1=\text{Counter(N)/Counter(P)} \tag{4.19}$$

4.5 Synchronization of signals from two clock domains

As mentioned earlier in this chapter, the chopping signal and the updating clock are independent, but it is possible for both signals to transition at the same time. This edge coincidence should be avoided for proper operation of the system. The control signal generator block generates all the control and clocks needed for the IS system, and eliminates the edge coincidence. The principle block diagram of the control generator is shown in Figure 4.11.

Although the chopping signal and the updating clock are in different clock domains, we can synchronize them with a clock that is much higher frequency than either signal. The error introduced due to this synchronization is negligible if the synchronizing clock frequency is high enough. In Figure 4.11, the input sinusoid is converted to a square wave by two digital inverters. DFF1~DFF3 are used to synchronize this square wave and produce three copies of it, each with a slightly different delay. The output of DFF2 is used as the internal chopping control signal. The outputs of DFF1 and DFF3 form a pulse through an XOR gate, and the edges of the chopping signal occur within the center of the pulse. The updating clock is derived from the main clock of 10MHz by dividing by 100. DFF4 is used to resynchronize the updating clock. The clock input of DFF4 is gate-controlled by the pulse, which blocks the events of the updating clock within the pulse duration. Because the pulse spans the chopping clock edge, it protects the chopping clock against any potential change from the updating clock.

The synchronization of the two signals from different clock domains to avoid any edge coincidence introduces some error. In the derivation of the chopping techniques for real/imaginary part extraction, it is assumed that the chopping signal and the sinusoid

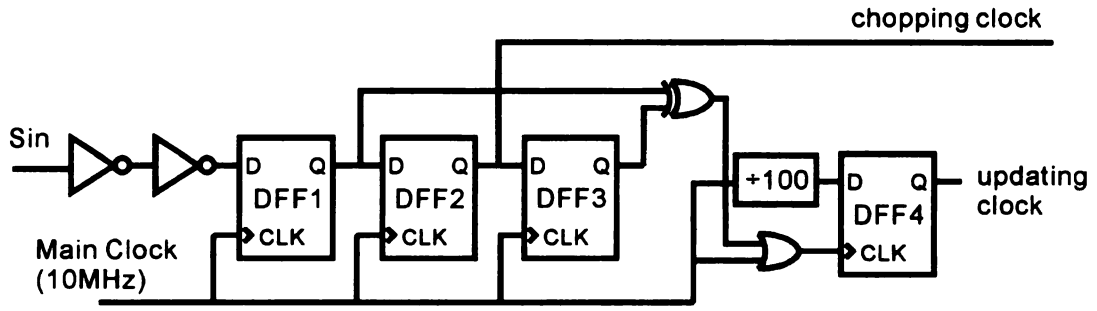


Figure 4.11. Block diagram of the control block, which generates the updating clock and the chopping control signal. An XOR gate is used to generate a pulse covering the edge of the chopping clock. This pulse will block the change on the updating clock through gating the clock of DFF4 and therefore avoiding conflict between the chopping signal and the updating clock.

should be in phase. For the chopping signals in Figure 4.11, the synchronization method described above introduces a delay of up to two 10MHz clock cycles compared to the sinusoid. However, since the frequency of the sinusoid is much lower than 10MHz (10kHz maximum), these delays only introduce negligible error. At the same time, when the pulse suppresses changes from the updating clock, it changes the period of frequency update by two consecutive 10MHz clock cycles surrounding the pulse. However, this error can also be neglected due to the relative high frequency of the main clock.

4.6 Circuit realization

Three major circuits are employed by the lock-in ADC in Figure 4.9. They are an op-amp, a comparator and a bidirectional counter/shifter. These blocks are realized with the AMI 0.5μm CMOS process.

4.6.1 Op-amp

Figure 4.12 shows the op-amp circuit. A folded cascode structure is implemented because it provides sufficient DC gain within a single stage. Because there is only one dominant pole in this structure and its load is only a capacitor, no extra hardware is

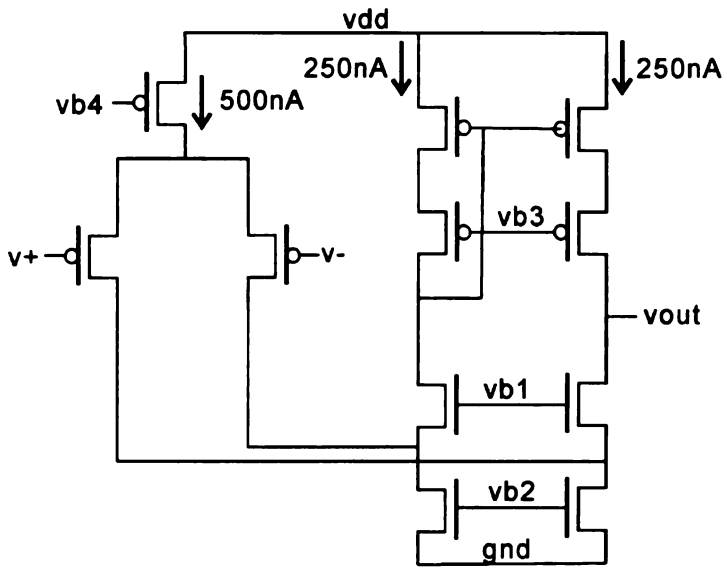


Figure 4.12. Folded cascade op-amp circuit designed for the lock-in ADC system.

required for stability compensation. With a total current consumption of 1μA, this circuit works in the sub-threshold region. The simulation results in Figure 4.13 show that it can provide 76dB DC gain with a unit gain bandwidth of 870kHz. A 1pF capacitor is used as a load in the simulation because the designed integrator capacitor in Figure 4.9 is 1pF. For a targeted 10-bit resolution and 100kHz clock, this amplifier provides enough DC gain and bandwidth.

4.6.2 Comparator

Two comparators are employed in Figure 4.9. In order to save silicon area, a circuit that combines these functions into one dual level comparator was designed and is shown in Figure 4.14. This is an amplifier-based comparator, and its output logic is defined in Figure 4.14. A DC sweep simulation was performed on the input voltage to check its functionality, and the result is plotted in Figure 4.15.

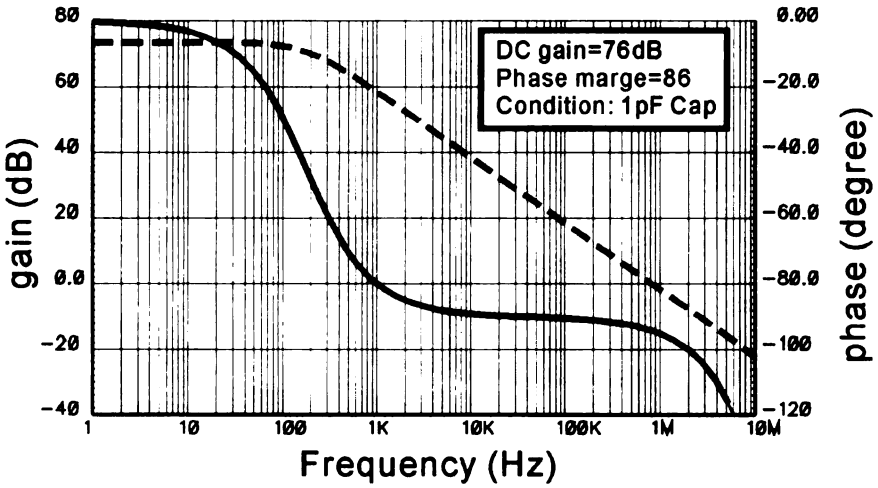


Figure 4.13. AC simulation of the amplifier in Figure 4.12.

4.6.3 Bidirectional counter/shifter

Two bidirectional counters are employed to count D's and D*'s during the conversion process. Due to the limited number of chip I/O pads and the potential need for a large number of counters (up to 100) within a multi-channel microsystem, it would be a significant advantage if the outputs of multiple EIS cells could to be read out through a serial data link. Thus, a shift register based counter structure was selected[77, 78]. As speed is not critical in this microsystem with up to a 100kHz clock, an asynchronous counter was chosen to avoid unnecessary dynamic power for unchanging bits. In [29], a very compact size counter/shifting register is designed. It achieves hardware efficiency through sharing most of the hardware between the asynchronous counter and shift register. The counter in [29] was configured as a up counter, and it is also feasible to configure it to function as a down counter. However, to build a bidirectional counter, more complicated control logic is normally required to enable dynamic switching between the two working modes. The scale of such control logic increases exponentially as the number of bits increases. In this biosensor microsystem application, the counter's

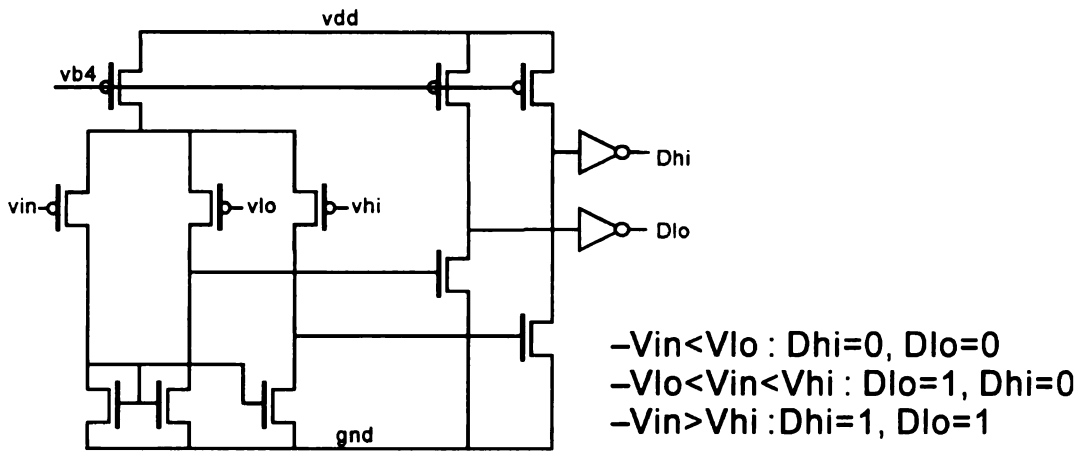


Figure 4.14. Circuit schematic of a dual-level comparator.

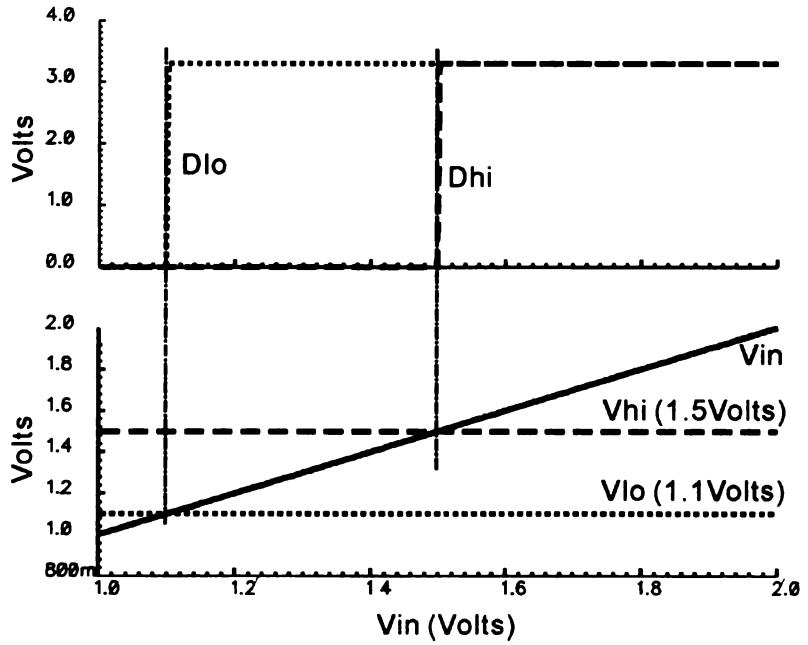


Figure 4.15. The input voltage DC sweep of the dual level comparator.

number of bits is set to twenty to support a wide range of sensor responses. Thus, the size (and power) of conventional up/down counter structures and their control circuitry present a limitation that must be addressed by designing a new ultra compact bidirectional counter/shifter circuit. The new counter is based on the up counter proposed

in [49], but an algorithm-based, down counting method was developed so that it can reuse the up counting circuits with some minor modifications.

The counters in the Figure 4.9 count down (minus 1) many times when φ1 is low. With a 4-bit counter taken as an example, if a countdown by *n* were to happen during a period where φ1 was low,, the counter result could be expressed as

$$a_3a_2a_1a_0 - n \tag{4.20}$$

where $a_3a_2a_1a_0$ is the initial value of the counter. It can also be rewritten as

$$a_3a_2a_1a_0 - n = -(-a_3a_2a_1a_0 + n) \tag{4.21}$$

In two's complement representation, the negative operation can be performed by a bit inversion plus '1'

$$-a_3a_2a_1a_0 = \overline{a_3a_2a_1a_0} + 1 \tag{4.22}$$

Thus, (4.20) can be rewritten as

$$\begin{aligned} & a_3a_2a_1a_0 - n \\ & = -(-a_3a_2a_1a_0 + n) \\ & = -((\overline{a_3a_2a_1a_0} + 1) + n) \quad * \\ & = -(\overline{a_3a_2a_1a_0} + n) - 1 \\ & = \left(\overline{(\overline{a_3a_2a_1a_0} + n)} + 1\right) - 1 \quad * \\ & = \overline{(\overline{a_3a_2a_1a_0} + n)} \end{aligned} \tag{4.23}$$

Steps with a (*) mean that the two's compliment representation for the negative sign operation was performed. The beginning of (4.23) represents the counting down by *n*, and

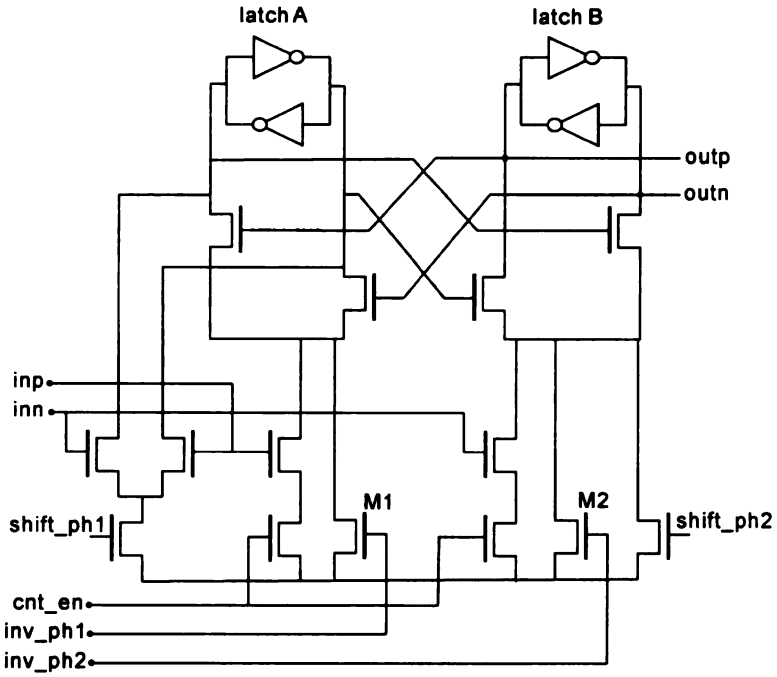


Figure 4.16. Schematic of the new up/down counter with shift register capability.

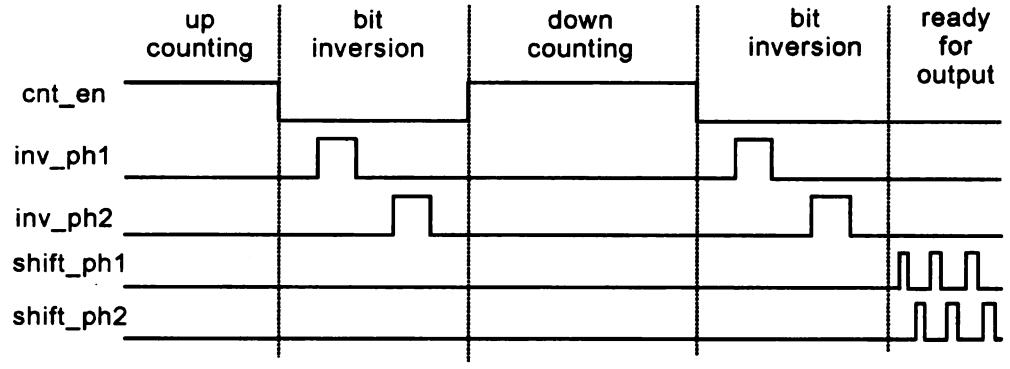


Figure 4.17. Waveform of the control signals for the proposed bidirectional counter/shifter.

the end of (4.23) shows that only bit inversion and up counting by n is performed. Thus, we see that the counting down can be achieved by simply counting up with a bit-inversions at the start and end of counting down operation. This concept can be applied to generate an up/down counter using an up counting circuit and minimal additional hardware.

To realize this idea, an up counter/shifter circuit cell with the bit inversion capability was designed and is shown in Figure 4.16. It is based on the up counter/shifting register in [49]. Two NMOS transistors (M1 and M2) and related control signals are inserted to provide the bit inversion capability. This circuit has two latches built with two back to back connected inverters. Both its input and output are in differential form. In counting mode, both *shift-ph1* and *shift_ph2* are set to be low and *cnt_en* is set to be high. In shifting mode, *cnt_en* is low, and the non-overlapping signals *shift_ph1* and *shift_ph2* shift the input to the output. In bit inversion mode, both *cnt_en* and shifting control signals (*shift_ph1* and *shift_ph2*) are kept low. The non-overlapping square pulses on *inv_ph1* and *inv_ph2* force the flip-flop to invert its state. The pulse of *inv_ph1* comes first and inverts latch A. Then the pulse of *inv_ph2* causes latch B to invert too. According to (4.23), for proper operation it is important to make sure that the bit inversions are performed both before and after any consecutive down counting cycle. The waveforms of the control signals for proper operation are summarized in Figure 4.17. This bidirectional counter/shifter contains only 24 transistors, which is less than the D flip-flop standard cell (28 transistors) developed by Tanner[79]. Because most of the transistors in Figure 4.17 are NMOS, it is easier to achieve higher hardware efficiency than a D flip-flop, which has the same number of both NMOS and PMOS transistors. With this compact cell circuit in Figure 4.16, a multi-bit bidirectional counter can be built as shown in Figure 4.18. Two 20-bit bidirectional counters/shifters are employed for the lock-in ADC in Figure 4.9.

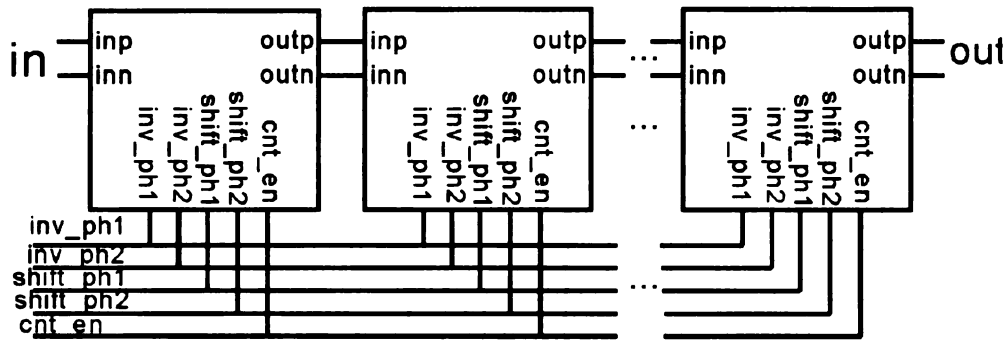


Figure 4.18. Block diagram of the scalable up/down counter.

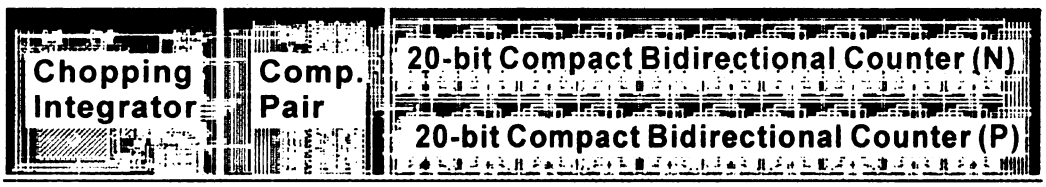


Figure 4.19. The layout of the lock-in ADC (600μm X 100μm).

4.6.4 System integration

Using the compact VLSI realization of functional blocks described above, the integrated lock-in ADC in Figure 4.9 was constructed, and the layout of this cell is shown in Figure 4.19. The whole circuit occupies an area of only 0.06mm^2. With this size, a 3mm by 3mm die can integrate more than 100cells, which is enough for current and anticipated microsystem needs. A system level transient simulation was performed to verify its functionality. For this function verification simulation, a 1kHz sinusoid input was chosen and simulation was continued for just one cycle to cut down simulation time. In real operation, with a 100kHz clock, there are only 10 clock cycles within one cycle of the 10kHz stimulus. In order to obtain high resolution, it needs to run for at least 100 stimulus cycles for a 10kHz frequency point.. The simulated waveforms of several critical signals are plotted in Figure 4.20. Comparing the simulation result in Figure 4.20 with the waveform in Figure 4.10, we can conclude that it functions as expected.

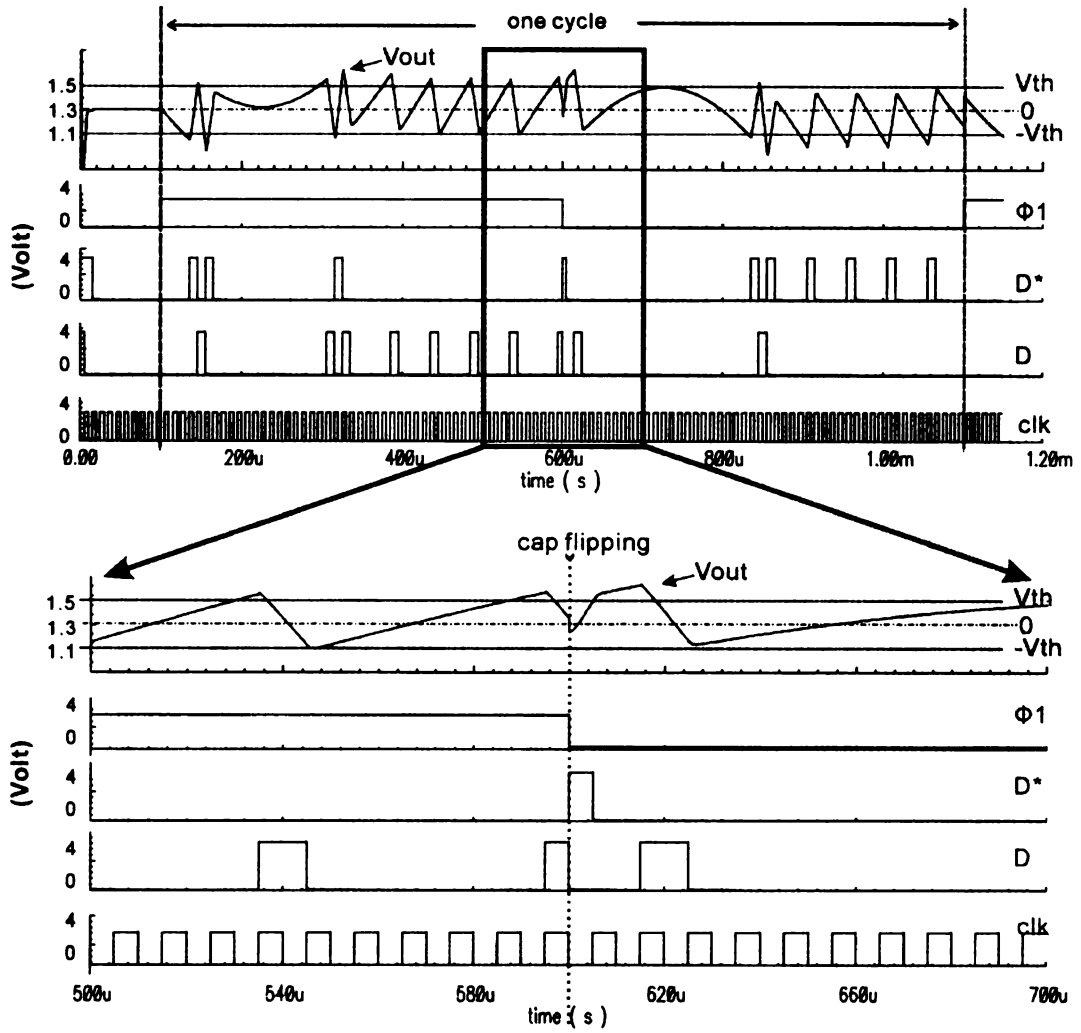


Figure 4.20. The simulation waveforms of some signals in the lock-in ADC system. The input sinusoid stimulus frequency is 1kHz.

4.7 Conclusion

A new structure is developed for a compact readout channel for an on-chip electrochemical impedance spectroscopy system in this chapter. It performs not only the impedance information extraction, but also impedance information digitization. With the help of this structure, the signal processing load of a biosensor array based EIS system can be distributed to each channel. The result of this chapter proves the feasibility of the multi-channel on-chip IS microsystem proposed in Chapter 3. Utilizing the AMI 0.5μm CMOS technology, a compact VLSI circuit realization is also achieved. A new super

compact bidirectional counter/shifter circuit is designed to significantly improve hardware efficiency. The test results of this circuit will be described in Chapter 6.

5 Integrated Quadrature Sinusoid Signal Generator

A qudrature sinusoid signal generator is a signal generator that can produce a sine wave (in-phase) and a cosine wave (qudrature phase) at the same frequency simultaneously. This function is necessary for the proposed on-chip EIS system. As discussed in Chapter 3, the frequency range of the output signal is expected to be 1mHz to 10kHz. The matching between the in-phase output and qudrature phase output is very critical. The target spurious free dynamic range (SFDR) of the sinusoid output is above 48dB. In this chapter, an on-chip qudrature sinusoid signal generator is developed to meet the requirements of the on-chip EIS system. A new hybrid structure is developed to achieve the required frequency range while keeping good in-phase qudrature-phase matching (IQ matching).

5.1 Approaches for the sinusoid signal generator

In commercial products and research papers, many solutions for a sinusoid signal generator are implemented. Generally speaking, they can be categorized in to three groups: digital signal processing (DSP) based solutions, oscillator based solutions and non linear circuit based solutions.

5.1.1 Digital signal processing based sinusoid generator

DSP based solutions generate the sinusoid signal through digital means [80, 81]. They consist of a digital memory bank, digital signal processor, digital to analog converter, and analog output circuits. As these methods operate in the digital domain and employs mature technologies, they provide very reliable performance and are therefore widely used in industry. There are two main architectures used to generate the sinusoid

with the DSP. One is a variable-clock-based method, while the other is a direct digital synthesis (DDS) based method.

Figure 5.1 shows the block diagram of the variable-clock-based method. A memory block is used to store all of the digitized samples of a periodic waveform over an entire period. A clocked address decoder enumerates all memory contents sequentially. The output of the memory reconstructs the periodic waveform in the digital domain. The frequency of the waveform is determined by the frequency of the updating clock. Finally, the digital to analog convertor translates the waveform to the analog domain. At the output of the generator, an analog filter smoothes the output and produces a clear image.

Similarly, a DDS based solution also employs a waveform memory block, which is enumerated by a clock. However, the frequency of the clock is fixed, as shown in Figure 5.2. The phase increment (delta phase) is tunable to control the frequency of the output waveform. Instead of sweeping across the entire waveform memory contents one by one, in DDS based systems the address decoder bypasses a certain number of memory addresses between two fixed-clock readings. The number of memory elements bypassed is controlled by the delta phase. The higher the delta phase, the more memory cells are bypassed, and therefore the higher the frequency of the output signal.

The digital signal processing based method is very flexible and can produce nearly

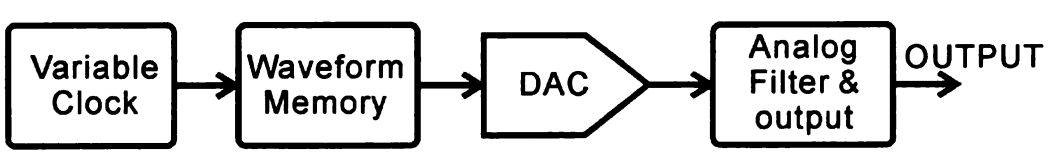


Figure 5.1.The block diagram of the variable clock based digital domain signal generator.

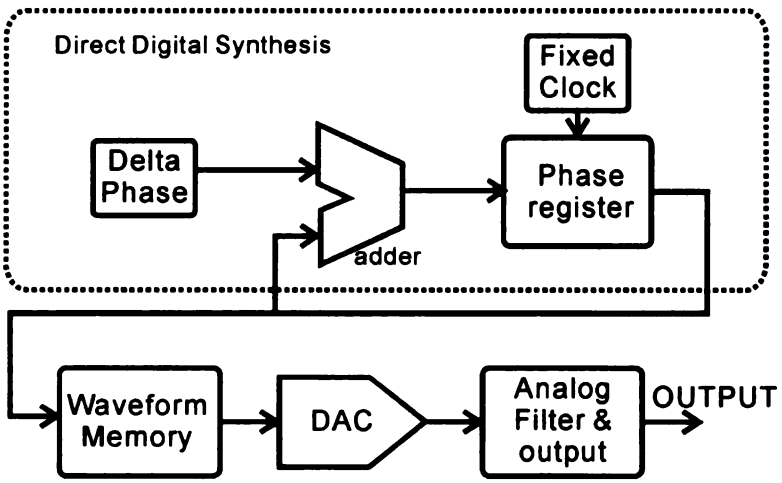


Figure 5.2. The block diagram of the direct digital synthesis based signal generator.

all shapes of waveforms. It can generate any periodic pattern as long as it has been saved in the waveform memory. For qudrature sinusoid outputs, it can also maintain good IQ matching with a preloaded waveform memory. The main drawback of this system is that it requires a very large memory, and thus large chip area, to generate low frequency signals. In order to relax the design requirements of the analog filter, the replicas in the DAC output should be distanced from the signal. Thus, the update clock frequency can not be very low. With a relatively high update clock frequency, a large oversampling ratio is expected for low frequency signals. As a result, a large memory space is needed due to the large number of samples. The physical size of large memory limits its application in an on-chip EIS system, where a lot of area is dedicated to on-chip biosensors. For only a high frequency sinusoid generator, a DSP based method is overqualified because it can generate any kind of periodic signal. The required flexibility in waveforms is achieved through generalizing the generator's structures. This results in complicated hardware that can then be optimized for only sinusoid generation.

5.1.2 The oscillator based sinusoid signal generator

An oscillator is the most widely used circuit to generate pure sine waves. There are many ways to build an oscillator, such as LC tank oscillators[82], RC oscillators[83] and transconductance (g_m)-C oscillators[84]. Qudrature oscillators are designed to generate qudrature signals[85-88]. In all oscillator based sinusoid signal generators, the frequency is controlled by the circuit components through factors such as the inductance, resistance, capacitance and transconductance. Frequency tuning is realized with the control of these parameters. In order to maintain a good accuracy in frequency, a feedback loop (which is always a phase locked loop) is used to track the output frequency with respect to a reference. The problem with these oscillator based signal generators is that it is hard to cover a wide frequency range because the component values, which control the frequency, can not change over a very wide range (7~8 orders of magnitude are desired). ,A subthreshold, widely tunable, CMOS transconductance providing a frequency tuning range over 7 decades has been presented [89], but accurate frequency control is difficult because it is impractical to exactly tune the transconductance over that range.

5.1.3 Nonlinear transfer function based signal generator.

In nonlinear transfer function based methods, a triangle wave is generated first. Then a nonlinear transformation is performed on the triangle wave to approximate the sine waveform, as shown in Figure 5.3 (a). The *tanh* function is a good transformation for a sine wave output. Bipolar transistors can be used to realize the *tanh* function, which is explicit in Figure 5.3 (b) [90]. A diode and a MOS transistor can also be used to realize a nonlinear function that is suitable for synthesizing a sine wave[91, 92].

Although this nonlinear transfer function based method makes the realization of the sinusoid signal generator easy due to the ease of generating a triangle wave; its main drawback is its linearity. It depends on the *tanh* function to approximate half a sine wave. It is important to pick the right range of the nonlinear transfer function to make a good approximation. A nonlinearity of 0.2% is reported in[92] Thus, the peak value and the common mode bias voltage of the triangle wave are very critical. For a board-level design, it is feasible to tune the triangle wave generator to match the nonlinear transfer function circuit. However, for on-chip applications, the nonlinear transfer function is largely affected by the process and temperature variation of the device. This makes it hard to control its quality in terms of linearity. Furthermore, if this type of generator is employed for quadrature output, two identical nonlinear transfer functions are required. The mismatching between them will directly contribute the IQ mismatch.

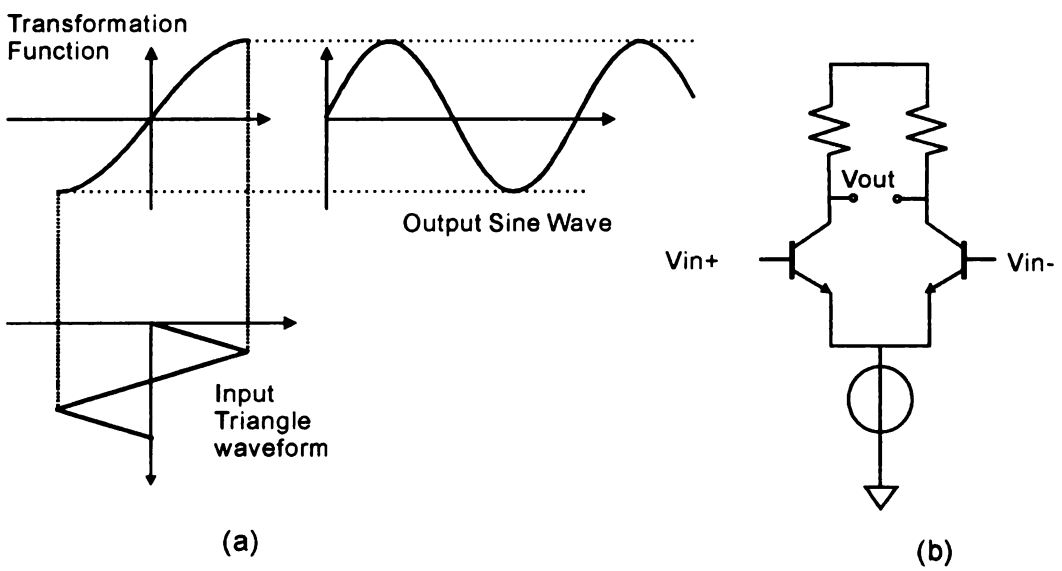


Figure 5.3. The principles of a triangle-to-sine signal generator: (a) transformation from triangle waveform to sine waveform, (b) a typical circuit to perform the transformation.

5.2 Hybrid quadrature sinusoid signal generator

All above mentioned solutions have some limitations for realizing an on-chip quadrature sinusoid generator with good linearity and IQ matching in addition to accurate frequency control over wide range (1mHz to 10kHz). A new architecture was developed to meet these requirements. It is built with a hybrid structure, where different principles are applied for the low frequency output and the high frequency output such that a wide range of the frequencies are covered. For high frequencies (above 100Hz), an unevenly tapped resistor chain with a tunable updating clock is employed. In the low frequency range, a subsampling concept is utilized through a sample and hold circuit. It also inherently keeps a good matching between in-phase and quadrature phase outputs because two outputs are generated from the same resistor chain. The principle block diagram illustrating the structure is shown in Figure 5.4. The proposed signal generator is purely controlled by digital signals and its output frequency is set with respect to the main input digital clock. Therefore high frequency accuracy is easily achieved. The detailed design for each block will be addressed in the following.

5.2.1 Principles of an R-chain based quadrature sinusoid signal generator

With a DSP based signal generator, the waveform is stored in the memory block. A tunable clock reads this memory block and then sends the results to a digital-to-analog convertor (DAC) to produce the corresponding analog output. This system can generate many varieties of periodic waveforms because the memory contents can be changed according to the desired output waveform. If the output is only a sinusoid, the contents of the memory are fixed. In order to save hardware, the memory block can be eliminated and the waveform information can be stored as analog signals in a resistor chain DAC.

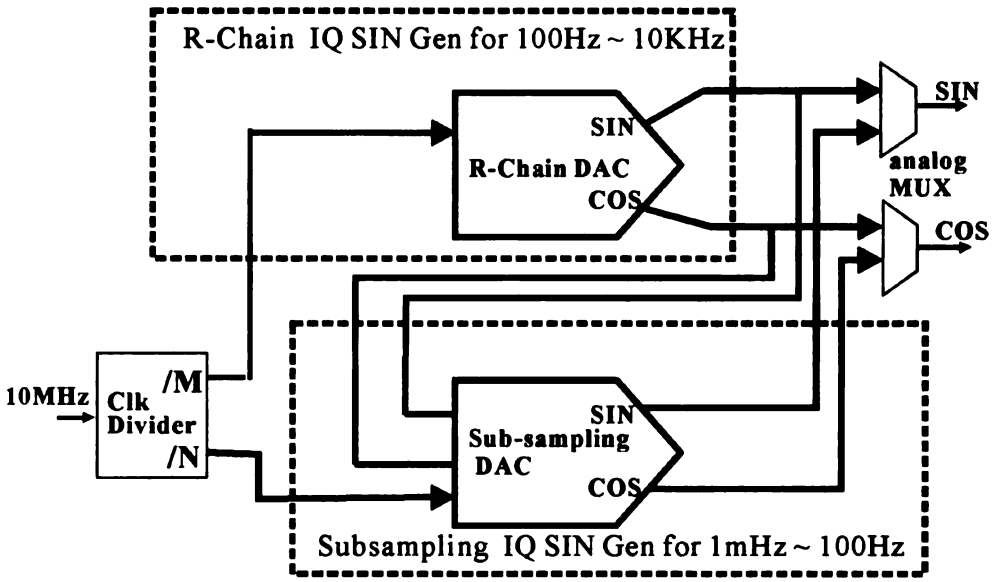


Figure 5.4. The principle structure for the proposed quadrature signal generator.

This principle is shown in Figure 5.5, where the data points of the sine wave are stored in analog form with an oversampling ratio of fourteen. The top and bottom voltages of the resistor chain in Figure 5.5 (b) are set to the peak and valley of the sine wave. The resistor values are chosen such that each tapped point has a voltage equal to the corresponding point in the sinusoid waveform (Figure 5.5 (a)).At any given time, only one switch is tuned on. The main clock controls these switches to pick the correct tap in the chain. The sequence of turning on the switches is 1-2-3-4-5-6-7-8-7-6-5-4-3-2. By repeating this sequence a sinusoid waveform is generated. In order to have a continuous output, a filter is used to smooth the output waveform and filter out any replicas present in the output.

5.2.2 The architecture of an R-chain based signal generator

As shown in Figure 5.6, in this design the same resistor chain is used for both the sine wave output and cosine wave output. At each tapping point of the resistor chain,

there are two switches, one for the sine wave and the other for the cosine. A token ring controls the two sets of switches. Two identical filters are used to smooth the each output.

5.2.3 R-Chain DAC design

An R-chain DAC is used to generate a quadrature sinusoid signal of 100Hz and above. The most important parameter of the DAC is the number of taps along the resistor

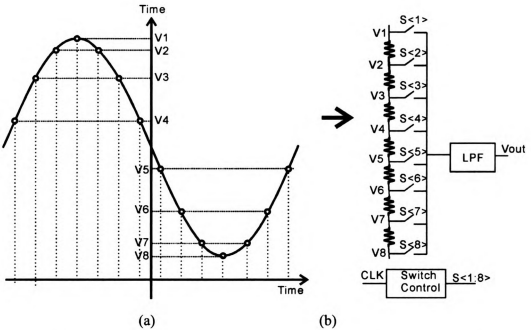


Figure 5.5. Example of a resistor chain based DAC working as sinusoid signal generator (oversampling ratio is 14), (a) the sampling points in a sinusoid waveform; (b) the structure of a DAC with an unevenly tapped resistor chain.

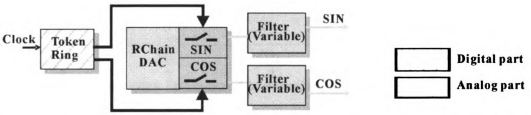


Figure 5.6. Architecture of a resistor chain DAC based qudrature sinusoid signal generator.

chain. This is decided by the oversampling ratio of the output sinusoid. Although more taps correspond to better linearity, they also require more silicon area for the switches and routing metal. Also, more taps complicate the switching control logic circuit because more switches need to be controlled. In this section, the effect of the oversampling ratio on the linearity of the DAC's output is studied, and an optimized oversampling ratio is selected.

The typical spectrum of the DAC's output for a sinusoid waveform is shown in Figure 5.7. The strengths of the fundamental signal and its replicas are enveloped by a rectified *sinc* function, which results from the sample and hold feature of the output waveform. The points of intersection between the rectified *sinc* function and the horizontal axis are located at multiples of the sampling frequency. The linearity is

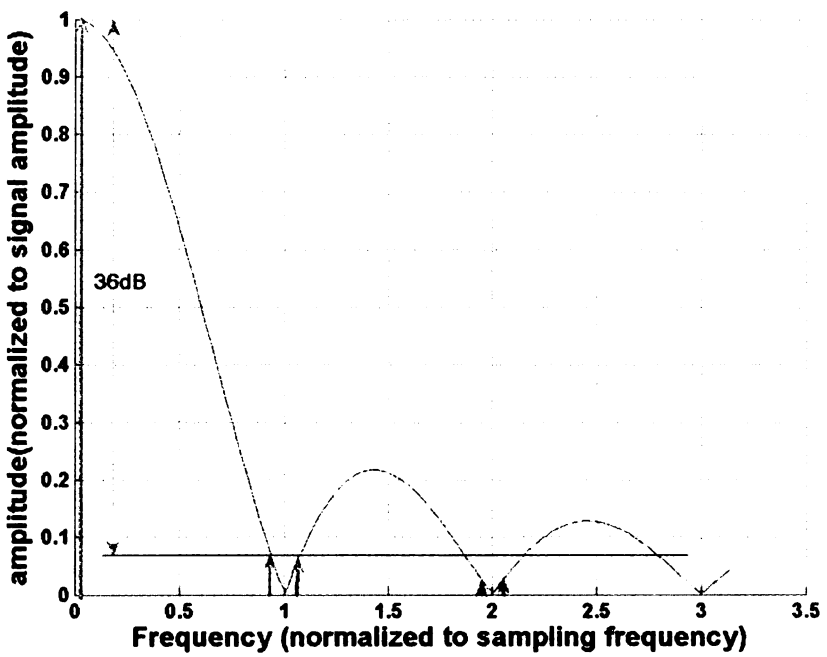


Figure 5.7. The spectrum of an R-chain DAC. The envelop is a rectified sinc function, the frequency is normalized to the sampling frequency, and the output amplitude is normalized to the signal strength.

analyzed by studying the spurious free dynamic range (SFDR), which is defined as,

$$SFDR = \frac{Strengh\ of fundamental\ signal}{Strengh\ of\ the\ total\ replicas}$$

Due to the asymptotic decrease in the amplitude of the *sinc* function, only the first replica has significant effect. So, the relationship between the oversampling ratio and the first replica's dominant SFDR is studied.

The strength of the fundamental frequency component in Figure 5.7 is,

$$A_0 = \left| \frac{\sin\left(2\pi \frac{f_0}{2f_s}\right)}{2\pi \frac{f_0}{2f_s}} \right| \tag{5.1}$$

where f_0 is the output sinusoid frequency, f_s is the updating frequency and

$$\frac{f_0}{f_s} = over\ sampling\ ratio \tag{5.2}$$

Similarly, the strength of the first replica is

$$A_1 = \sqrt{\left(\frac{\sin\left(2\pi \frac{f_s - f_0}{2f_s}\right)}{2\pi \frac{f_s - f_0}{2f_s}} \right)^2 + \left(\frac{\sin\left(2\pi \frac{f_s + f_0}{2f_s}\right)}{2\pi \frac{f_s + f_0}{2f_s}} \right)^2} \tag{5.3}$$

and the first replica's dominant SFDR is

$$SFDR = 20\log\left(\frac{A_0}{A_1}\right) \tag{5.4}$$

Combining (5.1) - (5.4), the relationship between linearity and oversampling ratio is developed, which is then plotted in Figure 5.8. It indicates that if the oversampling ratio is greater than 512, a linearity of 50dB can be achieved directly. However, that oversampling ratio is unrealistic in practice. The number of taps is roughly half of the oversampling ratio. An oversampling ratio of 512 would correspond to 256 taps, which will result in a very large amount of routing metal and taps, in addition to very complicated digital control logic for switch control. Thus, it is preferable to lower the oversampling ratio and employ a low pass filter (LPF) to further suppress any replicas. Also, the oversampling ratio can not be too low. The oversampling ratio determines the distance between the fundamental signal and its replicas. A very low oversampling ratio tightens the performance requirements for the LPF. Thus, a tradeoff is made between the

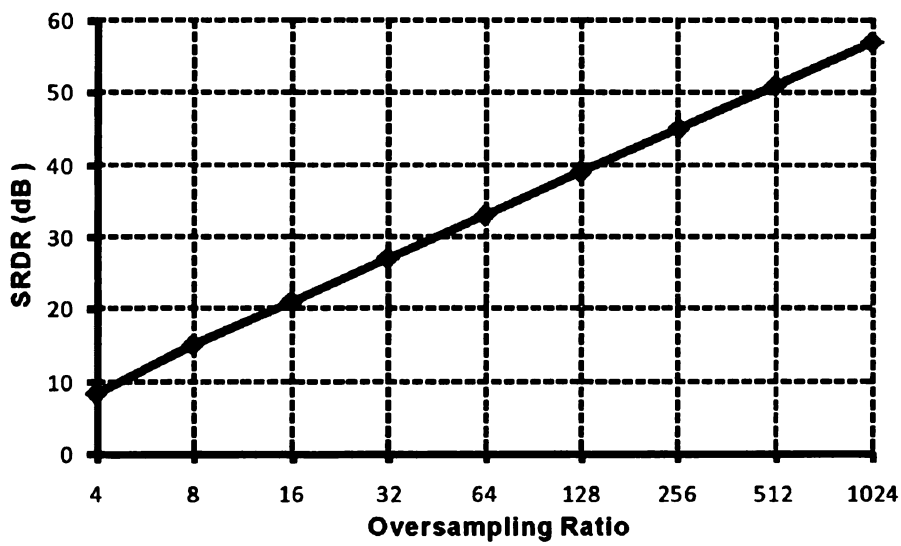


Figure 5.8. Linearity versus oversampling ratio for the DAC's output.

complexity of the LPF and that of the R-chain DAC. Therfore, an oversampling ratio of 64 was chosen. Only 33 taps are needed for this ratio, which is reasonable and feasible for both hardware area and switch control logic complexity. With a 64x oversampling ratio, the SFDR of the DAC's sinusoid output is 33dB. The proceeding LPF should provide at least 17dB suppression of replicas at a frequency of roughly 64x the signal frequency.

In Figure 5.4, the main clock of 10MHz is divided to generate an updating clock for the R-chain DAC. The highest output frequency of 156kHz is achieved by directly employing the main clock as the updating clock. The low frequency of the R-chain based signal generator is set to 100Hz to loosen the requirement on the filter.

5.2.4 Filter design for an R-chain based sinusoid signal generator

It is not difficult to design a filter that suppresses the replicas 64x away from signals by 17dB for a fixed sampling frequency. However, in the R-chain based signal generator, the sampling frequency is changing from MHz range to kHz range to cover a wide output frequency range. In order to overcome this challenge, a reconfigurable LPF was developed. The filter is a 2^{nd} order Butterworth filter with three optional cutoff frequencies. The configurations of the filter according to the output frequency is shown in

TABLE 5.1, CONFIGURATION OF THE FILTER FOR DIFFERENT OUTPUT FREQUENCY RANGES

Output Frequency Range	Cut off frequency of the 2nd order Butterworth LPF	Worst case first replicas suppression
100Hz – 1KHz	2K	-21dB @ 100Hz
1KHz – 10KHz	20K	-21dB @ 1KHz
Above 10KHz	200K	-21dB @ 10KHz

5.2.5 Sub-sampling based quadrature sinusoid signal generator.

The R-chain DAC based signal generator is not suitable for low frequency sinusoid output because the updating clock will scale down proportionally with the output frequency and make it hard for the filter to suppress the replicas close to the desired signals. Thus, for frequencies of 100Hz and lower, a sub-sampling based sinusoid signal generator is proposed. It can provide good linearity for a sinusoid signal of very low frequency with a high oversampling ratio, which loosens the requirements for the low pass filter design.

Sub-sampling is also referred to as down-sampling. It is a signal sampling technique. In contrast to Nyquist sampling techniques, the sub-sampling technique uses a sampling frequency much lower than twice the signal frequency. The first replicas of the sampling output will be located near DC. As the replicas carry the same information as the sampled fundamental signal, the first replicas are used to store the information in a sub-sampling technique. This is often used in communication systems to down convert the information from an RF band to a low intermediate frequency band to facilitate further signal processing [82, 93].

In this research, this technique is employed to produce a low frequency sinusoid waveform through sampling a high frequency sinusoid signal. The sequence of the sampling result of a sinusoid input is given by

$$f(n) = \sin\left(2\pi n \frac{f_0}{f_s}\right) \tag{5.5}$$

where f_0 is the signal frequency and f_s is the sampling frequency. Assuming that f_0 is very close to f_s then $\Delta f = f_0 - f_s$, and (5.5) can be expressed as

$$f(n) = \sin\left(2\pi n \frac{f_s + \Delta f}{f_s}\right) = \sin\left(2\pi n + 2\pi n \frac{\Delta f}{f_s}\right) = \sin\left(2\pi n \frac{\Delta f}{f_s}\right) \tag{5.6}$$

which shows that the sampled output is also a sinusoid but has frequency of Δf. This sub-sampling technique is graphically shown in Figure 5.9. A sinusoid input (solid line) is sampled by a frequency very close to it and another sinusoid at output (dotted line) is formed. The principle block diagram of this kind of signal generator is shown in Figure 5.10.

To have a constant sinusoid output from sub-sampling it is very critical to keep a constant relationship between sampling frequency and input signal frequency. This is easily achieved with the proposed structure. The sub-sampling signal generator is realized by sampling the R-chain signal generator's output with a clock derived from the same main clock. For the R-chain based signal generator, the output frequency is exactly controlled by and related to the main clock. The sampling frequency for the sub-sampling signal generator is also generated from the main clock, and thus the frequency difference between the sampling frequency and the output frequency of the R-chain signal generator will be constant and can be tightly controlled. The output frequency range of the sub-sampling signal generator and the corresponding frequency of the R-chain based signal generator output are listed in

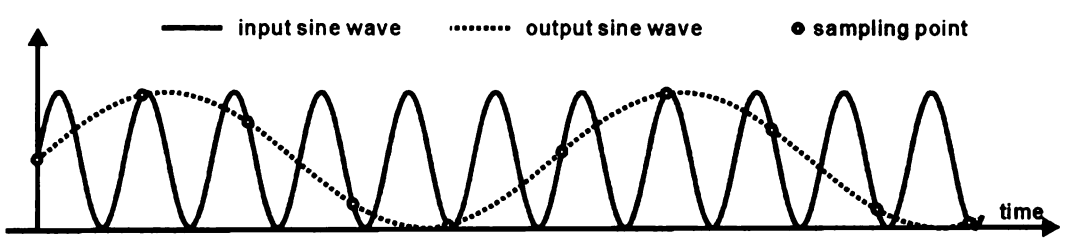


Figure 5.9. Concept of sub-sampling techniques.

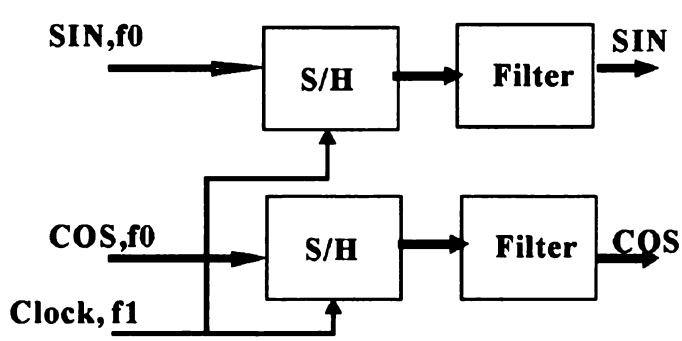


Figure 5.10. The block diagram of a sub-sampling system.

5.2.6 Filter design for a sub-sampling signal generator

The over sampling ratio (OSR) for the S/H in a sub-sampling circuit is roughly equal to the frequency ratio of the input signal and the output signal.

shows that the smallest OSR is about 100. Furthermore, the sampling frequency does not change too much because it only varies by a small amount around the input signal frequency. Therefore, it is not difficult to design a filter to smooth the output.

A 2^{nd} order Butterworth filter with a 250Hz cutoff frequency is employed to smooth the output. With the minimum OSR of 100, the SFDR is about 37dB based on the plots in Figure 5.8. This filter will provide replica suppression of at least 24dB for 0.1Hz to 10Hz and at least 64dB for 10 Hz to 100Hz, which is enough to achieve a total SFDR of at least 50dB. For the output frequency of 1 mHz -0.1Hz, replicas exist within the pass band of the filter. Thus, the filter does not provide any suppression for these replicas. However, in this range the S/H itself already provides good SFDR of more than 50dB because the OSR is over 1000.

TABLE 5.2. INPUT SINGAL FREQUENCY SETTINGS FOR DIFFERENT RANGES OF OUTPUT FREQUENCIES

Output frequency range	Input signal frequency (M is the divider ratio for an R-chain DAC updating clock)
1mHz – 0.1Hz	99.968 Hz (M=1563)
0.1Hz – 10Hz	1001.6Hz (M=156)
10Hz – 100Hz	9765.5Hz (M=16)

5.3 Circuit realization

5.3.1 The R-Chain DAC

The R-chain DAC is built with many resistors in series. 33 taps, including two ends of the chain, are needed for an OSR of 64. As the chain is unevenly tapped, the values of the resistors between any two consecutive taps could be different. For good linearity of the DAC, proportional matching of these resistors is very important. As matching between different sized resistors is worse than that between resistors of the same size, the resistor chain is composed of 1000 resistors of the same size. The 33 tapping points are mapped into points between 0 and 1000. Theoretically, the method can provide a linearity of 10 bits (60dB), which meets the requirement of 50dB linearity. The circuit of the resistor chain is shown in Figure 5.11.

At each tap, two switches are added for the sine and cosine signals. Instead of a CMOS switch, only an NMOS transistor is used for the switch. This saves silicon area and simplifies the control logic design.

5.3.2 Low pass filter design

Both the RCDAC signal generator's output and the sub-sampling signal generator's output need a filter to suppress the replicas and switching noise. These filter's

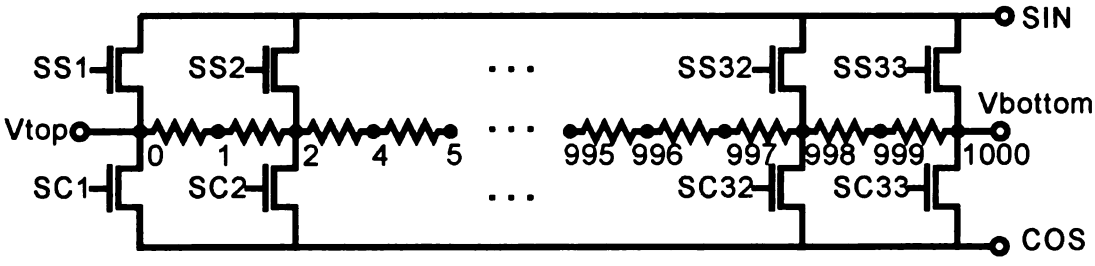


Figure 5.11. A circuit for an R-chain DAC for a signal generator.

characteristics and requirements have been discussed earlier in this chapter. In this section, their circuit realization will be discussed.

5.3.2.1 Structure of the filter

A g_m-C structure was adopted to design the filters. For a 2nd order Butterworth LPF, its g_m-C realization is shown in Figure 5.12. It is a g_m-C structure that can be used to synthesize different biquadratic LPFs [94]. By setting the g_m and capacitors values, we can realize the 2^{nd} order Butterworth filter. The ratio of C1 to C2 is set to 2, so that the Q is fixed at 0.707, which provides maximum pass-band flatness for the pass band. All the parameters are summarized in TABLE 5.3 for the two kinds of filters used in the system.

Instead of using a metal-insulator-metal (MIM) capacitor, the NMOS gate capacitance is used. Because the g_m is also built with the NMOS transistors, the NMOS gate capacitance will track the process variation of *gm*. Although this tracking can not cancel out the process variation of the cut-off frequency very well, it narrows down the process variation range.

For configurable filters, the g_m values and the capacitance values have two level settings. Combining them, filters with three different cutoff frequencies are provided. Two sets of capacitor values are achieved by putting two individual capacitors in parallel and using one of them to tune the capacitance value. For the transconductance, a circuit structure is developed to provide two g_m values.

With the fixed filter, the g_m and capacitance values are fixed. Because the cutoff frequency is very low, with a reasonable capacitor value (feasible within the silicon area), the g_m is inevitably small, as shown in TABLE 5.3. A new structure that provides a very small g_m was designed to meet this need.

5.3.2.2 OTA with two transconductance levels

The filter capacitor can not be too large such that it will not fit within the on-chip system. This indicates that the g_m values need to be small. There are several ways to design an OTA with a small g_m. They are 1) OTA with current division [95] and source degeneration [96], 2) floating gate OTA [97, 98] and 3) bulk driven OTA [99, 100]. The

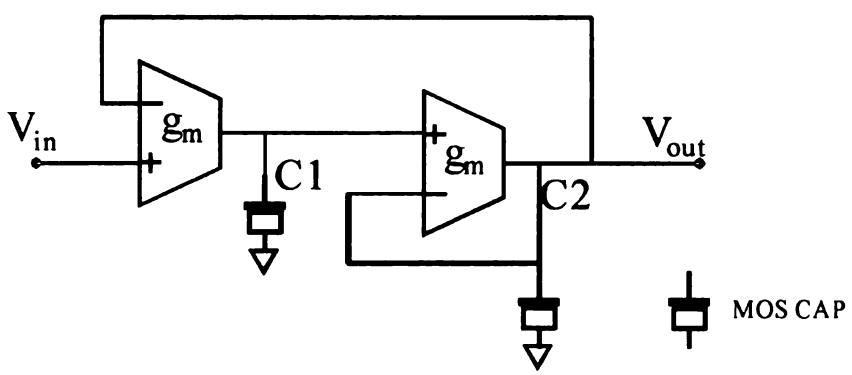


Figure 5.12. Schematic of the g_m-C biquadratic filter.

TABLE 5.3. THE PARAMETERS FOR THE FILTER DESIGN.

Configurable Filter					Fixed Filter				
Gm	C1	C2	Fc	Q	gm	C1	C2	Fc	Q
60n	5p	2.5p	2k	0.707	9n	7.5p	3.7p	250	0.707
600n	5p	2.5p	20k	0.707					
600n	0.5p	0.25p	200k	0.707					

OTA with current division and source degeneration was adopted because it consumes less power, is easier to control, and provides relatively good performance [101].

The schematic of the designed OTA is shown in Figure 5.13. It combines the current division and source degeneration techniques. [101] also built an OTA by combining these two techniques. In Figure 5.13, the combination is realized in a different way. The current division is realized with the mirror structure (Mn1&Mn2, Mn3&Mn4). The internal feedback loops involving the input pair will control the gate of the current mirrors including Mn1 and Mn3, respectively. Because the current of the input pairs is fixed, this structure will give better linearity performance. PMOS transistors in the triode region working as MOS-resistors are used as the source degeneration resistor. The g_m of the OTA is

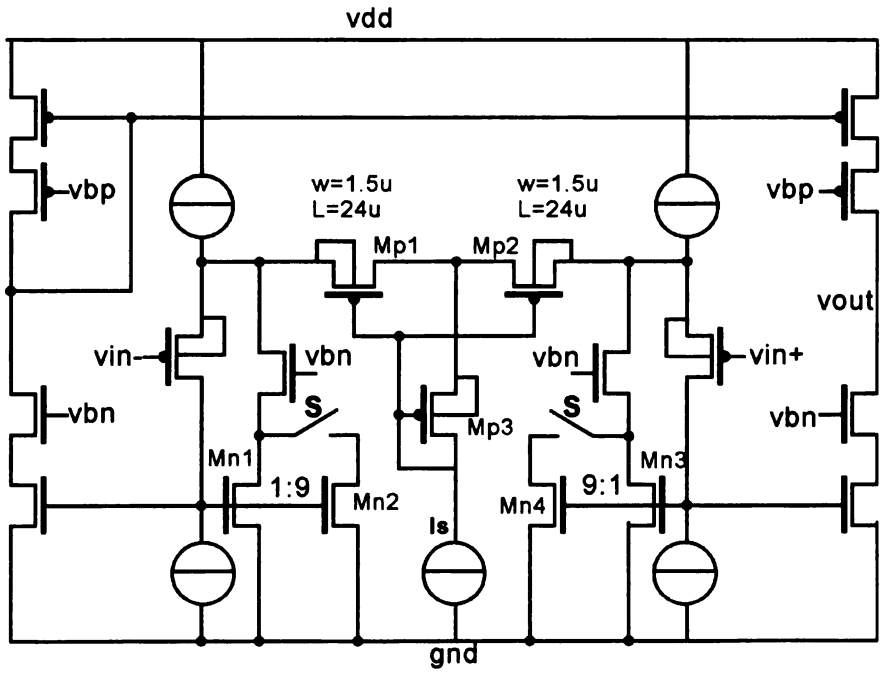


Figure 5.13. OTA with a small g_m (two level tunable). The signal S selects the g_m level.

$$g_m = K\frac{g_{O1,2}}{2} \tag{5.7}$$

$$g_{O1,2} = 2\sqrt{\mu C_{OX}\frac{I_S}{2}\left(\frac{W}{L}\right)_{Mp1,2}} \tag{5.8}$$

where K is the ratio of the current division (controlled by S in the Figure 5.13 circuit) and I_S, as shown in Figure 5.13, is the bias current for the source degeneration MOS-resistor. Thus we can tune the transconductance (g_m) with the size of the MOS-R and its bias currents. In order to keep the circuit working properly, the overall current direction within the MOS-R can not be changed. Thus the minimum of I_S should be larger than the maximum AC current within a margin of tolerance, which improves the linearity of this circuit.

5.3.2.3 OTA with small transconductance levels

For the filters used at the output of the sub-sampling signal generator, TABLE 5.3 shows the transconductance is only 9nS. The same circuit topology in Figure 5.13 is used for a small g_m OTA too. The circuit for the OTA with a small transconductance is shown in Figure 5.14. The current division switch is removed, and the division ratio is fixed at 10. A smaller drain current and longer length of MOS-R in (5.8) are used to generate a small g_o.

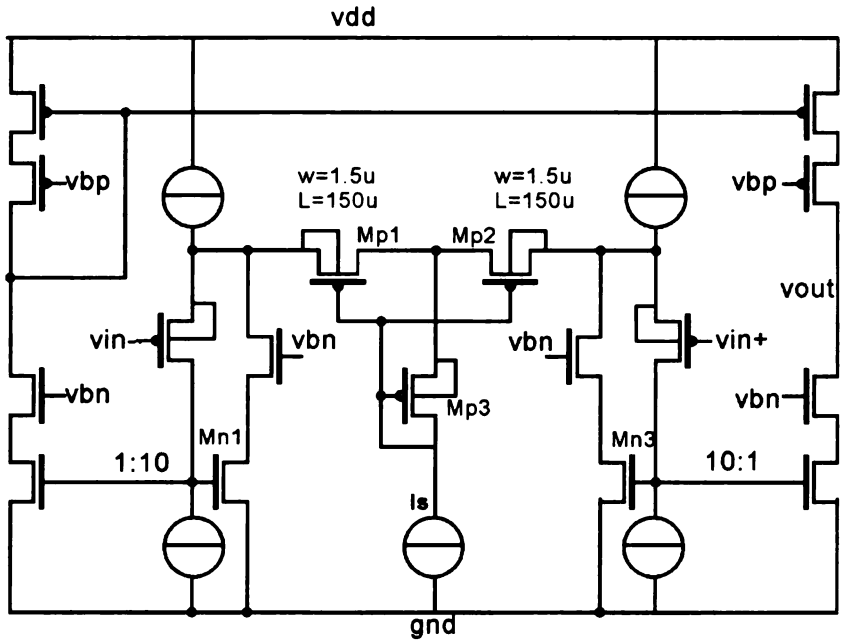
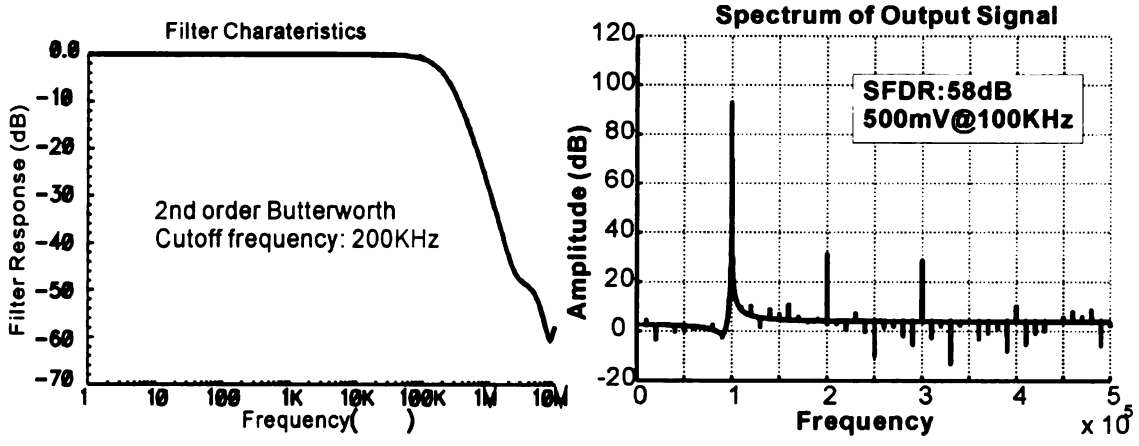


Figure 5.14. OTA with a small g_m.

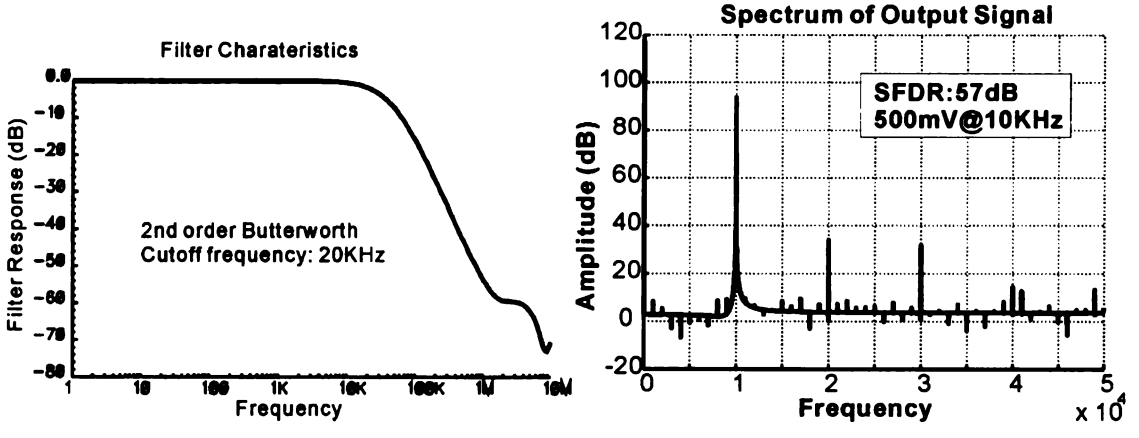
5.3.2.4 Filter characteristics

The transfer functions and the linearity of the filters were verified with simulation. The transfer function and linearity performance of the variable frequency filter with a cutoff frequency of 200kHz, 20kHz and 2kHz are shown in Figure 5.15, Figure 5.16, .and Figure 5.17, respectively. The transfer function and linearity performance of the fixed cutoff frequency (250Hz) filter are shown in Figure 5.18. These results show that the filter meets the design requirements and can provide a dynamic range of more than 57dB.



(a) (b)

Figure 5.15. (a) transfer function and (b) the linearity of the variable filter with cut-off frequency of 200KHz.



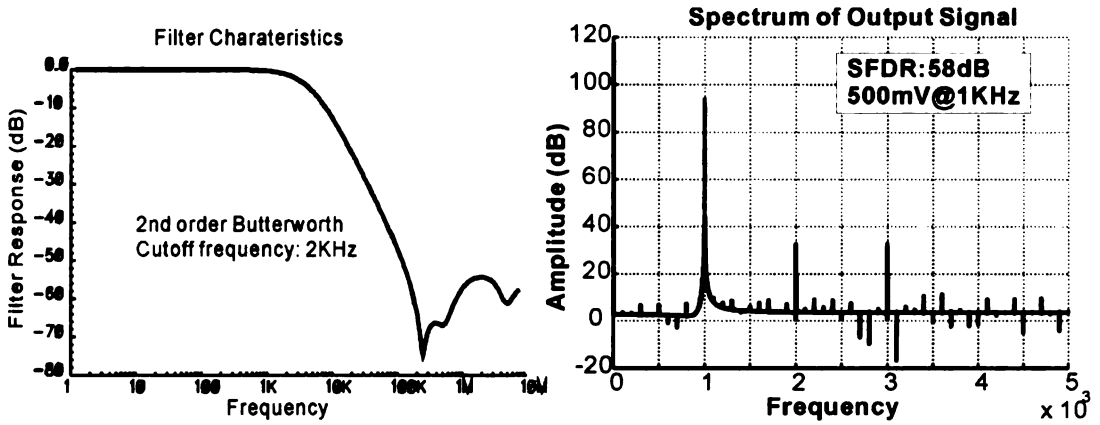
(a) (b)

Figure 5.16. (a) Transfer function and (b) linearity of the variable filter with a cut-off frequency of 20KHz.

5.3.3 Sub-sampling quadrature sinusoid signal generators

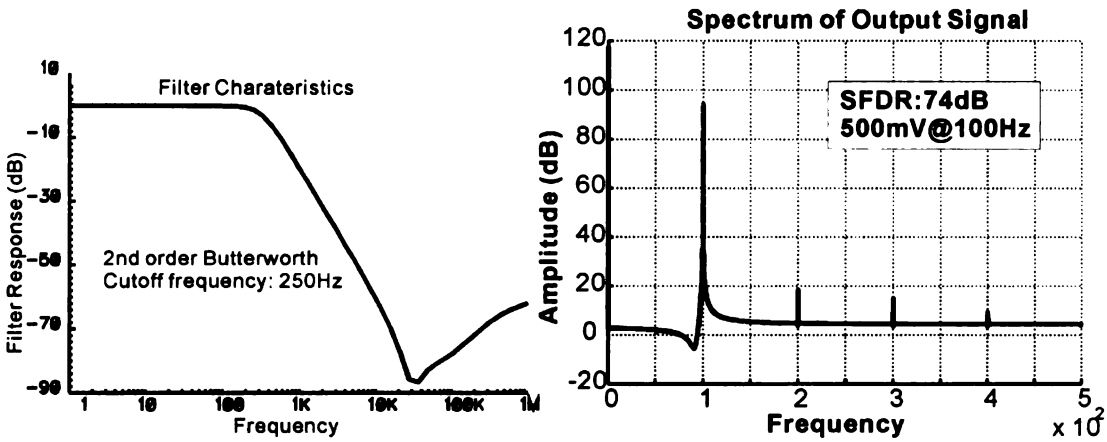
The circuit of a sub-sampling signal generator is shown in Figure 5.19. A simple capacitor track and hold (T/H) circuit is followed by a 2nd order Butterworth filter with a cutoff frequency of 250 Hz.

CMOS transmission gates are used as the sampling switch. For the I and Q channels, the middle switch is the real switch, and the two switches on each end are half size



(a) (b)

Figure 5.17. (a) Transfer function and (b) the linearity of the variable filter with a cut-off frequency of 2KHz.



(a) (b)

Figure 5.18. (a) Transfer function and (b) the linearity of the variable filter with a cut-off frequency of 250Hz.

dummy switches to compensate for the charge injection of the switch operation. This cancellation is beneficial for a moderate linearity level (50dB).

During the system analysis, the relationship between OSR and SFDR was based on an ideal S/H circuit. This assumption is important for a sub-sampling signal generator. If a normal 50% duty cycle T/H circuit is used for a sub-sampling signal generator instead

of an S/H circuit, a lot of the energy of the original signal will leak through to the output in the tracking windows and deteriorate the low frequency output, as shown in Figure 5.21. Thus, a 50% duty cycle clock, providing a wide sampling window, results in leakage energy around the updating frequency. This leakage will badly deteriorate the SFDR. To overcome this problem with a simple T/H circuit, the duty cycle of the T/H clock was changed so that it only tracks the input within a very narrow window, which not only limits the original signal leakage power but also moves the leaked energy to higher frequencies where a simple filter can effectively screen this leakage out. The digital control block will generate the narrow width square pulse (low duty cycle square wave) with a width of 0.1μsec.

The leakage of the sampling capacitor could be a serious problem with a very low frequency output because the sampling frequency is only about 100Hz. In order to suppress it, minimum sized NMOS transistors were used and the capacitor was set to 1pF. Because the stored value only changes a small amount for two consecutive samplings, the

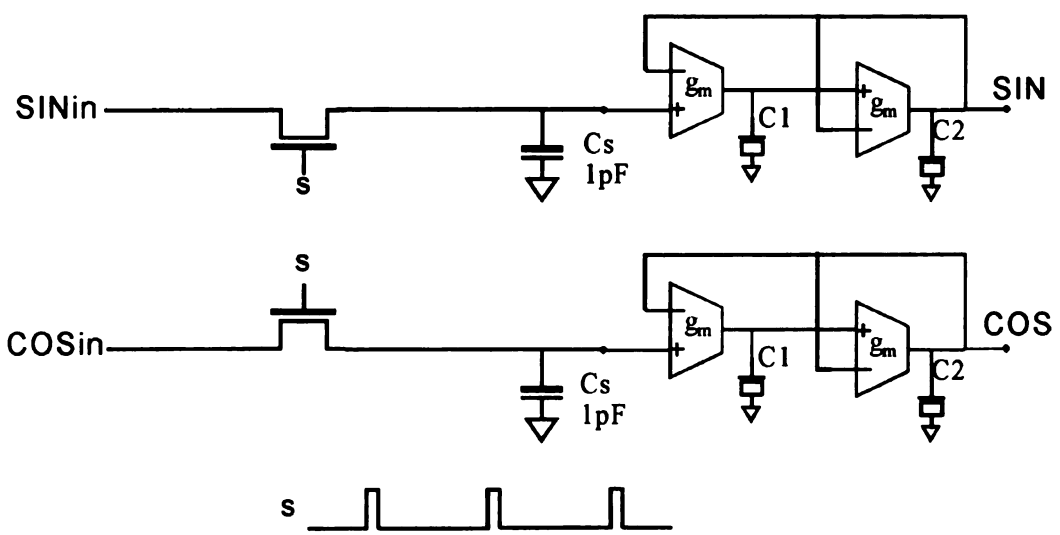


Figure 5.19. Circuit of the sub-sampling quadrature sinusoid signal generator.

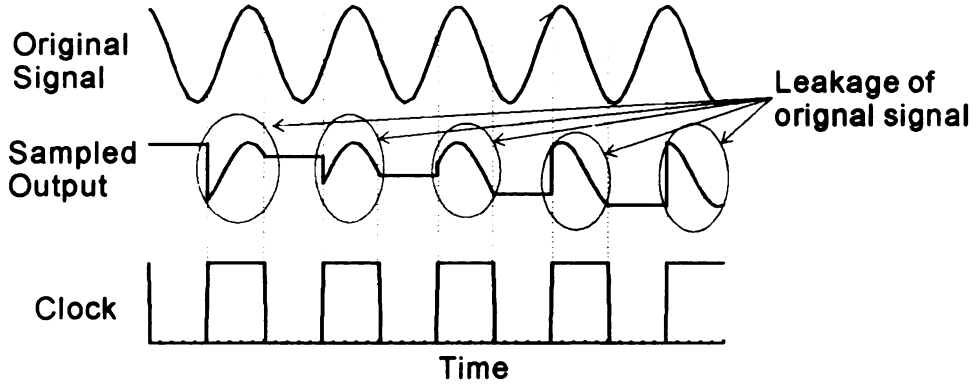


Figure 5.21. The original signal leaks out to the output through the tracking window.

minimum size NMOS transistors do not affect the sampling speed at all.

5.3.4 Digital control circuit

5.3.4.1 Clock divider

Two clock dividers are used in the circuit to provide a clock for the R-chain DAC and sub-sampling circuit. The divider circuit is shown in Figure 5.20. An asynchronous counter is used to reduce power consumption. The divider ratio is set by a memory register value. To generate the clock for the R-chain DAC, the counter and register have 11 bits. For the sub-sampling clock, the counter and register have 17 bits. The values of registers and their corresponding output frequencies are summarized in TABLE 5.4.

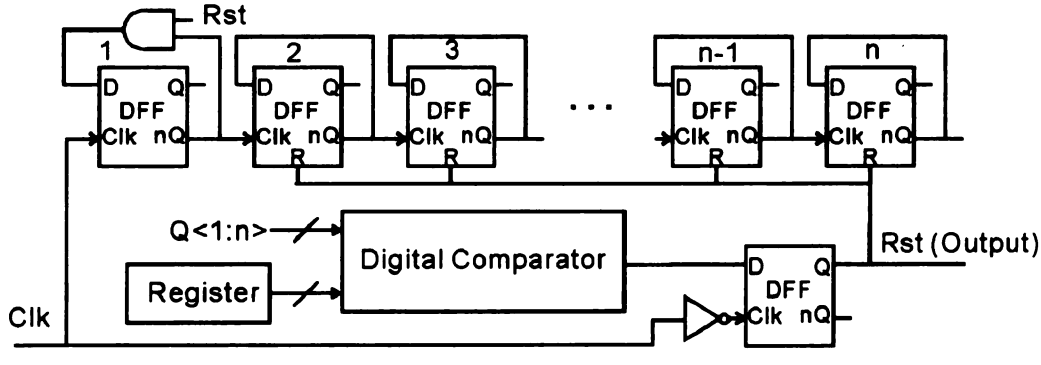


Figure 5.20. The clock divider circuit.

TABLE 5.4. THE CLOCK DIVIDER SETTINGS FOR DIFFERENT FREQUENCY OUTPUTS.

Frequency Range	Register M (11 Bits)	Frequency output of DAC	Register N (17 bits)
100-78K Hz	71B'h~002'h	100-78K Hz	N/A
10-100 Hz	10'B	9765.6 Hz	401'h - 40B'h
0.1-10 Hz	9C'h	1001.6Hz	2701'h – 2765'h
1m-0.1 Hz	61B'h	99.968Hz	186C1'h-1971A'h

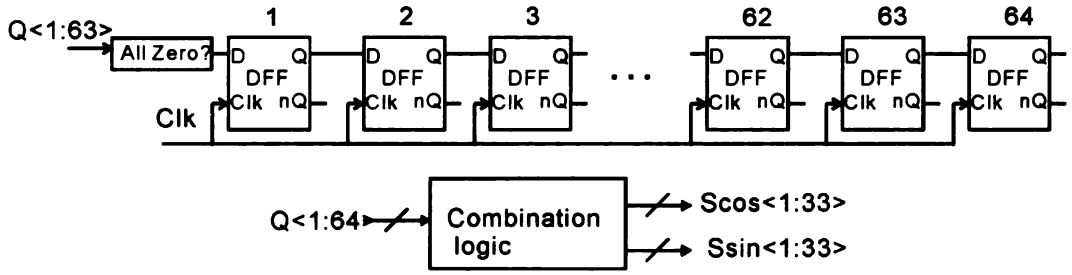


Figure 5.22. The token ring based switch network's control signal generator.

5.3.4.2 Switch control for the R-chain DAC signal generator

A token ring is used to generate the correct switch controls for the tap switch network of the sine and cosine outputs. As shown in Figure 5.22, there are 64 elements in the ring corresponding to an OSR of 64. At any time, only one "1" is in the ring. An all zero detector verifies this single "1" rule and pulls the ring back from any other incorrect states. Each switch in the R-chain DAC corresponds to two elements in the ring. A combination logic block generates the switch control signals by providing a mapping describing this relationship. As both the sine and cosine control signals are generated from the same token ring, their phase relationship can be well-maintained.

5.3.5 System integration

Using the above designed fundamental building blocks, the overall integrated quadrature sinusoid signal generator was implemented with the AMI 0.5μm CMOS

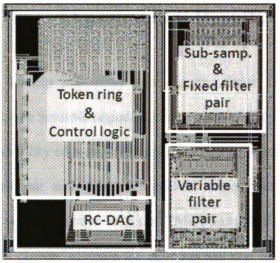


Figure 5.23. The layout of the quadrature sinusoid signal generator. Its size is $1mm^2$.

process. The layout of this signal generator is plotted in Figure 5.23. Its silicon area is $1mm^2$. This circuit is very large compared with the size ($0.06mm^2$) of the channel-wise compact IS readout circuit developed in Chapter 4. However, we only need one signal generator for the entire microsystem. Thus, this size is acceptable for an integrated impedance spectroscopy microsystem.

5.4 Conclusion

A wide frequency range quadrature sinusoid signal generator was presented in this chapter. With its hybrid structure, it can provide good phase and amplitude matching for the quadrature sinusoid signal from 1mHz and 10kHz. It inherently guarantees frequency tuning accuracy because it is purely digitally controlled. The prototype of this design has been fabricated with a 0.5μm CMOS process. With a size of $1mm^2$, it can serve as the stimulus generator for an integrated IS microsystem. Testing results will be given in Chapter 6.

6 Experimental Results

The a compact on-chip impedance spectroscopy circuit (Chapter 4) and wide frequency range quadrature sinusoid signal generator circuit (Chapter 5) were developed to demonstrate the feasibility of a multi-channel impedance spectroscopy microsystem and to explore the relevant analog/mixed signal IC design methodology for such a system., Both circuits were fabricated with the AMI 0.5μm CMOS technology using a 3V power supply. This chapter presents the experimental test results of the fabricated chips. In addition, test results for a prototype electrochemical biosensor system using the designed circuits are presented to verify the application potential of this thesis research.

6.1 Measurement of the compact IS circuit

The die photo of the prototype IS lock-in ADC is shown in Figure 6.1 with the main functional blocks labeled. The size of each lock-in ADC cell is 100μm by 600μm, and two of these cells are on the prototype chip. Due to the compact size of this circuit, which

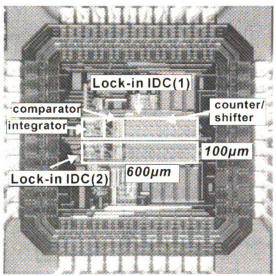


Figure 6.1. Die of two lock-in ADCs.

was a rigorously maintained design goal, more than 100 copies of this circuit can be instantiated on a typical 3mm by 3mm silicon chip. This is sufficient for both existing and near future IS based biosensor array microsystems. The lock-in ADC cell consumes 2μA of current in the working mode. To measure the circuit's performance and verify its functionality, two sets of experiments are performed to characterize the lock-in ADC, and demonstrate its practical impedance information extraction capability.

6.1.1 Experiment setup

A data acquisition card (DAQ E2530A) from Agilent Technologies (Santa Clara, CA, USA) was used to interface the lock-in ADC with a PC running software to configure and control the chip. The setup is shown in Figure 6.2. The DAQ E2530A can generate both analog and digital patterns and read analog or digital signals. It generates the sinusoid voltage signals for a sensor model that mimics the function of the biosensors. The current response of the sensor model due to the sinusoid stimulus is sent to the lock-in ADC. The DAQ E2530A also generates all of the digital control signals for the lock-in ADC. The digitized results from the chip are also read out serially by the DAQ E2530A so they can be displaced and stored on the PC.

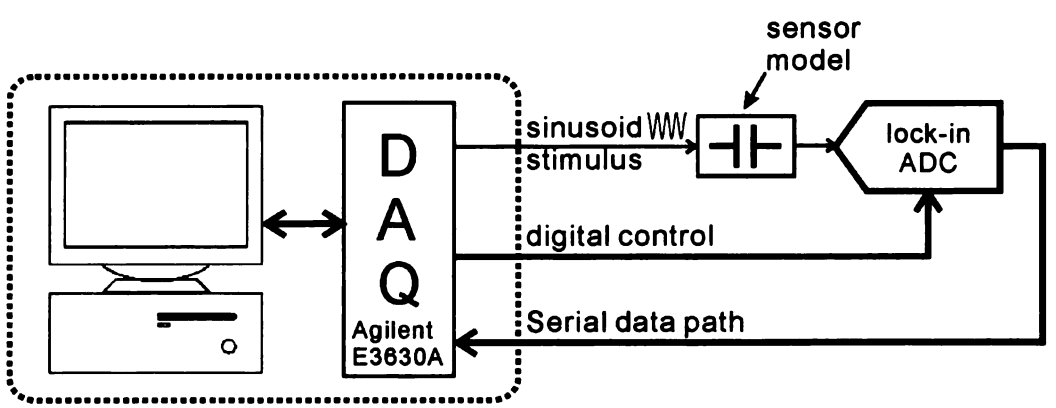


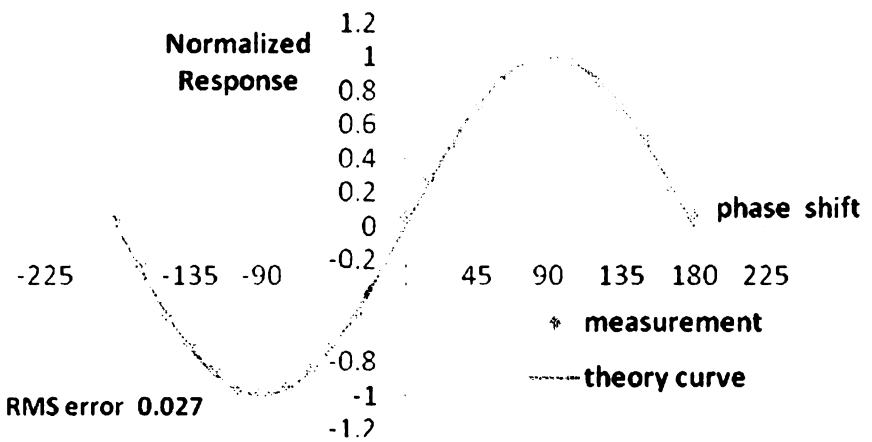
Figure 6.2. Experiment setup for the lock-in ADC.

Two sensor model circuits were designed to characterize the performance of the lock-in ADC. To characterize the amplitude and phase transfer function of the lock-in ADC, a pure capacitor is used for the sensor model. For a voltage sinusoid stimulus strength of several hundreds of mV, which is large enough to surpass the noise effects of the DAQ card, an off-the-shelf capacitor can generate a current response range from several hundreds of nA to sub-pA. By setting the capacitor to different values and sweeping the amplitude of the sinusoid voltage stimulus, the lock-in ADC can be tested over a wide input current amplitude range. The phase relationship between the capacitor response current and the voltage stimulus is fixed at 90°. Thus we can sweep the phase delay of the sinusoid voltage stimulus to sweep the phase of the response current. The second sensor model circuit is the model for the tBLM biosensor [42], described in 6.1.3. This circuit model is used to verify the impedance extraction capability and accuracy.

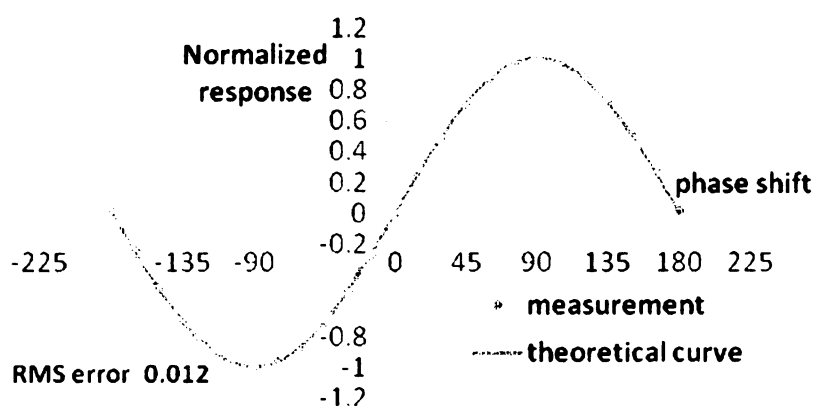
6.1.2 Characteristics of conversion

The lock-in ADC extracts the phase and amplitude information of an input sinusoid current. The phase and amplitude transfer characteristics were studied individually in the experiments.

Sinusoid current signals with constant amplitude were fed into the lock-in ADC. Their phase with respect to the reference clock was then changed. The observed phase vs. the normalized output is plotted in Figure 6.3. The results are normalized to the peak value. Two sets of sinusoid signals were tested: one is 10Hz with an amplitude of 30nA and the other is 1kHz with an amplitude of 1.4nA. The lock-in ADC was configured to measure the imaginary coefficient only. The real coefficient can be found through shifting the curve in Figure 6.3 by 90 degrees. Theoretically, as shown in (4.2), with a



(a)

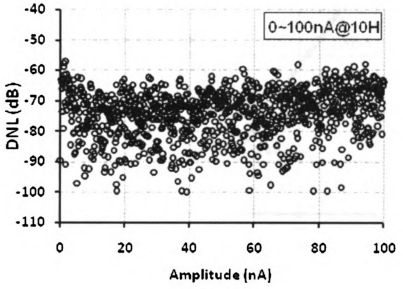


(b)

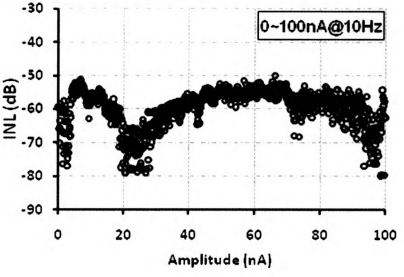
Figure 6.3. Phase vs. output with an input sinusoid of (a) 30nA amplitude @1KHz and (b) 1.4nA@10Hz.

constant amplitude and frequency, the relationship between the phase shift and the imaginary coefficient is a sine wave. Figure 6.3 also plots the theoretical prediction. We can see that the measured results match the theoretical curve very well. The RMS error for 30nA 1KHz sine input is 0.027 and that for 1.4nA 10Hz sine input is 0.012.

To examine the amplitude transfer function, a 100 Hz sinusoid signal with 0 initial phase was supplied and its real portion coefficient was extracted by the lock-in ADC. The amplitude of the sinusoid signal was swept and the lock-in ADC output was observed. The relationship between the input signal's amplitude and the digital output (digitized real portion) is linear for a constant phase and frequency. Thus, the ADC's benchmarks, integrated non-linearity (INL) and differential non-linearity (DNL) plots, are used to show the lock-in ADC's amplitude conversion accuracy. With the input amplitude changing from 0 to 100nA, the 1024 points of INL and DNL are plotted in Figure 6.4. The results show that the circuit can provide more than 50dB dynamic range for an input range of 100nA.



(a)



(b)

Figure 6.4. The lock-in ADC's amplitude transfer performance with respect to 8-bit digitization: (a) DNL, (b) INL.

The lock-in ADC can be configured to accommodate a wide range of input signal strengths by changing the magnitude of the two reference currents and the updating clock. Figure 6.5 plots the amplitude conversion characteristics of the lock-in ADC for the

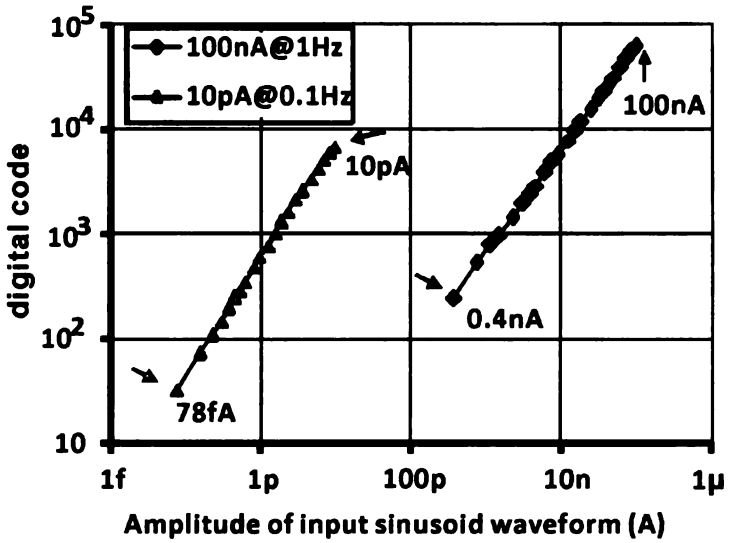


Figure 6.5. Amplitude conversion characterization for the zero phase sinewave input. The lock-in ADC is configured to accommodate a wide range of input signals.

largest signal range and the smallest signal range. Figure 6.5 shows that the achievable sensitivity is better than 100fA.

6.1.3 Impedance information extraction

The experiment setup in Figure 6.6 was used to verify the function of the lock-in ADC as an IS system. A sensor model circuit and component values were chosen to mimic a real IS-based biosensor[102]. A sinusoid voltage stimulus was applied and the current response was analyzed by the lock-in ADC. The real and imaginary current response was recovered from the digital output of the chip. The results are plotted in Figure 6.7. The calculated impedance for a given set of component values in the sensor circuit model in Figure 6.6 are also plotted for comparison. Plots in Figure 6.7 show that the chip's measured results follow the theoretical prediction very well. The maximum absolute error observed is 0.6nA, and the RMS absolute error is 0.1nA. Compared with

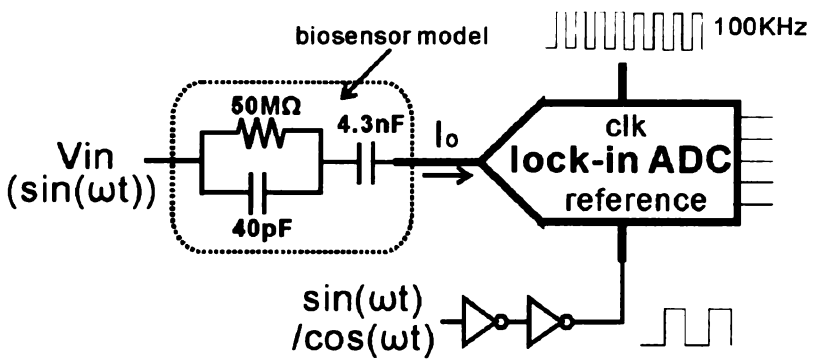


Figure 6.6. Experiment setup for verifying impedance extraction.

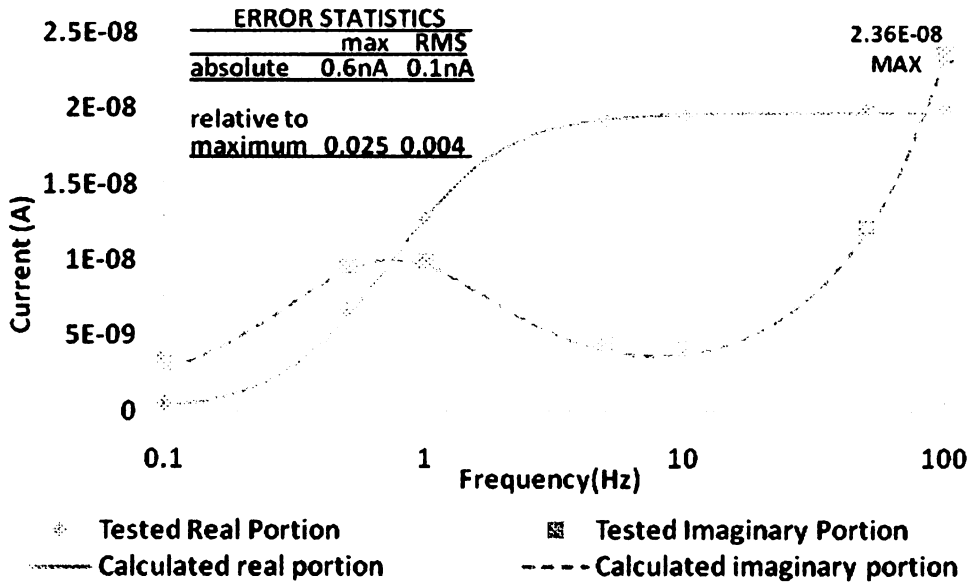


Figure 6.7. The real and imagineary coefficients of current response from the setup in Figure 6.6. The test result and theoritical expectitations are given for comparision.

the maximum result of 23.5nA, the relative maximum error is 0.025 and the RMS error is 0.004.

6.1.4 Discussion

The above experiments prove that the lock-in ADC can extract and digitize the impedance information with good accuracy. Its low power and compact size meet the

requirements of an IS-based biosensor array microsystem. The performance is summarized in TABLE 6.1.

TABLE 6.1. PERFORMANCE SUMMARY OF THE LOCK-IN ADC

	Parameters
Technology	0.5μm CMOS
Area	0.06mm^2
Power	6uW
Amplitude conversion Resolution	50dB
Phase conversion RMS error	<2.7%
Frequency range	1mHz ~ 10KHz
Maximum current range	100nA

6.2 Measurements of the quadrature sinusoid signal generator

A die photo of the prototype quadrature sinusoid signal generator is shown in Figure 6.8. The circuit occupies 1mm by 1mm. With a 3V supply, the entire circuit draws

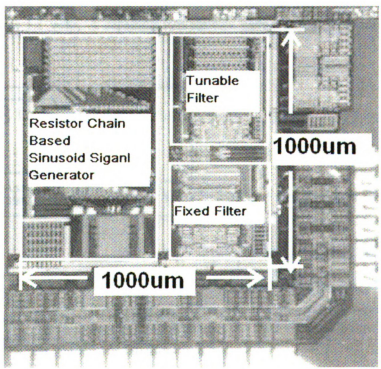


Figure 6.8. Die photo of the quadrature sinusoid signal generator.

only 60μA of current during operation. Several experiments were performed to test the quality of the output sinusoid in terms of the dynamic range and matching between the in-phase and quadrature-phase outputs. As the filter's performance is critical for the signal quality, the filters used in the system were also characterized through experiments.

6.2.1 Experiment setup

Two sets of experiments were conducted to test the transfer function of the filters and the output signal of the signal generator individually. A spectrum analyzer (E4395A) from Agilent Technologies (Santa Clara, CA, USA) and a power supply were employed to test the filters. This setup is shown in Figure 6.9. The spectrum analyzer was set to the A/B response testing mode. A small signal was generated at the RF out port and was then fed back to the spectrum analyzer at port B as the input reference signal. It was also fed to the input of the filters. The DC value of the RF output is always zero, and the filter input's DC bias is 1.1 volts. A capacitor and resistor were used, as in Figure 6.9, to set

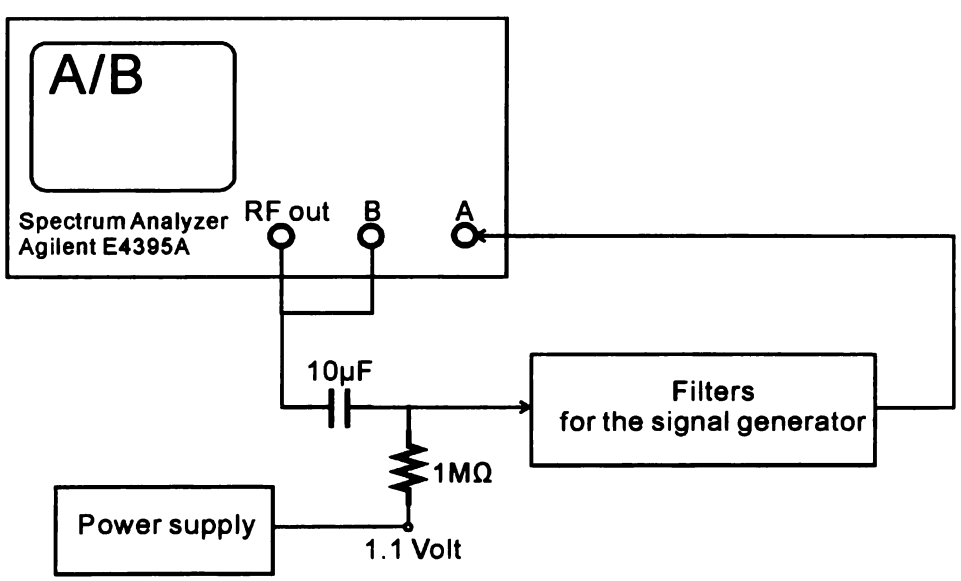


Figure 6.9. Experiment setup for the filter testing.

the proper working point for RF out signal being input to the filter. The filter's response output was connected to the *A* port of the spectrum analyzer. The frequency sweep range and the signal power were set through the spectrum analyzer.

To test the overall signal generator, a data acquisition card (DAQ E3630A) from Agilent Technologies (Santa Clara, CA, USA) was employed, as shown in Figure 6.10. The DAQ generates the digital control signals for the signal generator and receives the sine and cosine output from the test chip at two of its analog input channels. The spectrum analysis of these input signals was performed with a computer.

6.2.2 Analog filter characterization

Two kinds of filters are employed by this design. Both of them are 2nd order Butterworth filters, and the same g_m-C structure (Figure 5.12) was selected for both of them. One has three optional cutoff frequencies; the other has a fixed cutoff frequency. Experiments were performed to check their AC transfer characteristics and large signal linearity, both of which are important for good quality sinusoid output.

Figure 6.11 shows the measured transfer function of the filters. All curves are put into one plot for easier comparison. Due to process variations, the cutoff frequencies are

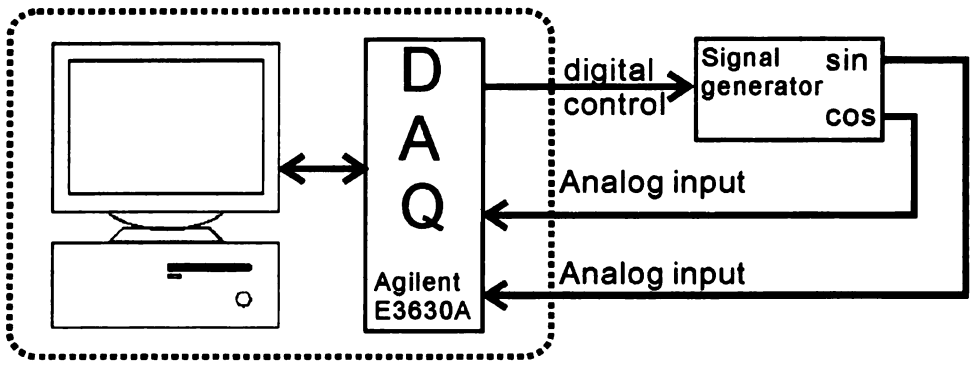


Figure 6.10. Experiment setup for the signal generator testing.

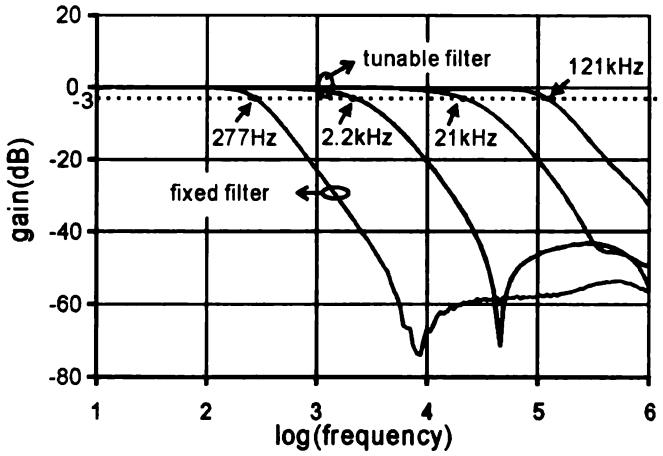
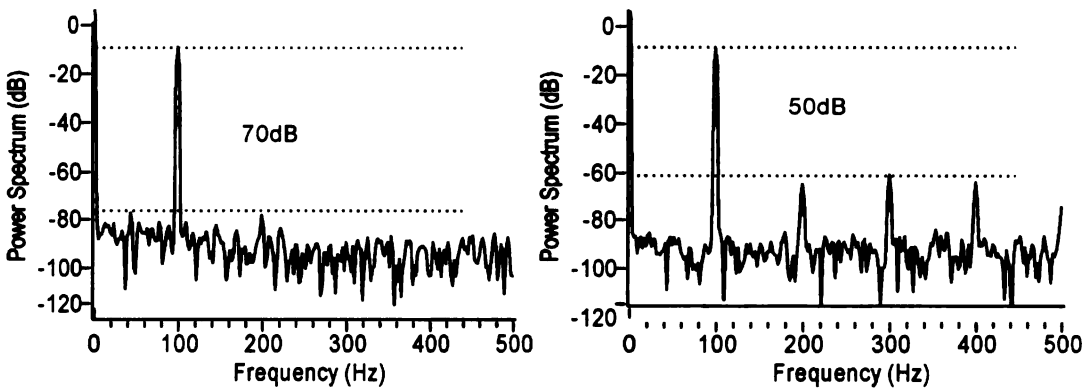


Figure 6.11. Measured frequency response of the filters on the signal generator chip.



(a) (b)

Figure 6.12. Output spectrum for a 100Hz sine input with a 450mV amplitude for (a) a tunable filter and (b) a fixed filter.

shifted for some of the curves, compared with the simulation results in Chapter 5. However, since the designed 2nd Butterworth filter can provide more than enough suppression of the harmonics, this process variation does not interfere with performance..

Figure 6.12 shows the linearity plot for each filter. Only one plot is given for the tunable filter because the main nonlinearity contributors, Mp1 and Mp2 in Figure 5.13, are the same for all three cutoff frequencies. Both filters can provide more than 50dB of linearity with an input strength of 450mV, which is enough for the 48dB output linearity of the signal generator.

6.2.3 Quadrature sinusoid output

Several output frequency points were generated ranging from 1mHz to 10kHz. The waveforms of two extreme output frequencies are plotted in Figure 6.13. Figure 6.14 shows the observed phase mismatch, which is the variation from the expected 90 degree phase between the sine and cosine outputs. Figure 6.15 shows the amplitude mismatch between sine and cosine output. The spurious free dynamic range (SFDR) of the output (450mV amplitude) is plotted in Figure 6.16. The linearity in Figure 6.16 represents the

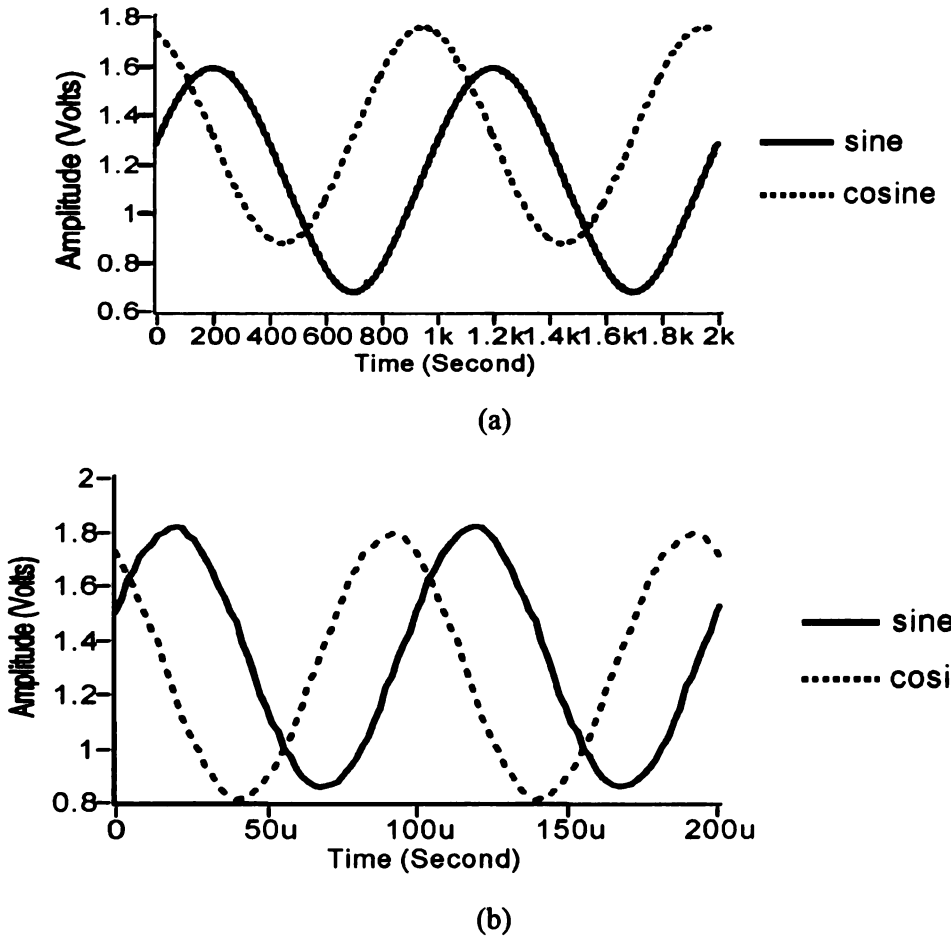


Figure 6.13. Waveform of quadrature sinusoid output at two extreme frequencies, (a) 1mHz and (b) 10KHz.

signal strength difference between the desired frequency and the largest secondary spike in the output signal spectrum.

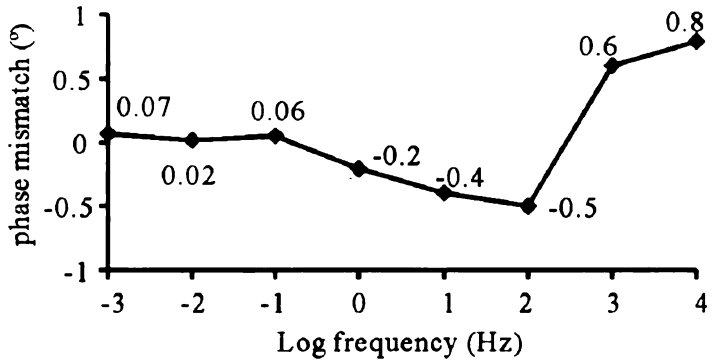


Figure 6.14. The phase mismatch between the output quadature signals.

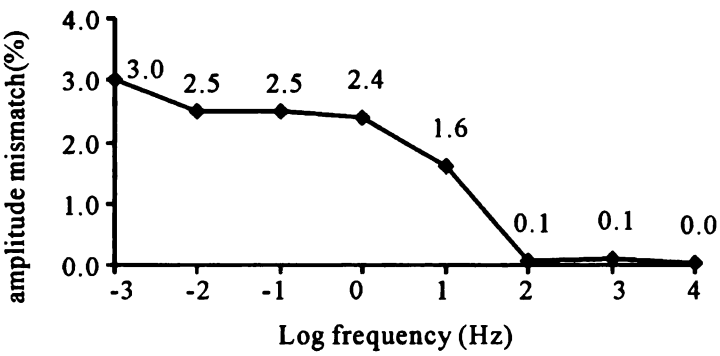


Figure 6.15. The amplitude mismatch between the output quadature signals.

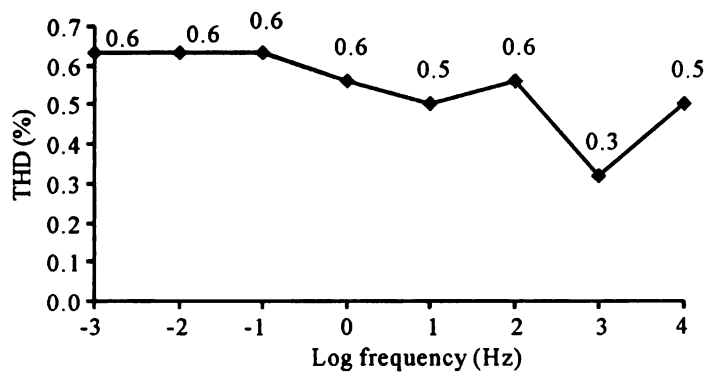


Figure 6.16. Spurious free dynamic range (SFDR) of the output (450mV amplitude).

6.2.4 Discussion

The results show that the signal generator developed for this dissertation can provide a quadrature sinusoid output over the expected frequency range with good phase (< 1°) and amplitude matching (< 3%) between sine and cosine output. Figure 6.13(a) shows a DC offset difference between sine and cosine outputs for a 1mHz output. This is due to the offset of the filters. It is constant for all the frequency points generated with the sub-sampling circuit (1mHz ~ 100Hz), so it is easy to be corrected through calibration. The frequency accuracy is guaranteed inherently due to the digital clock control. The measured linearity is above 44dB. Overall, its performance is summarized in TABLE 6.2.

6.3 Biosensor measurement

6.3.1 Experimental setup

To test the designed IS circuit under real conditions, a prototype electrochemical biosensor system was developed utilizing a miniaturized biosensor fabricated on a glass chip. The test setup for this prototype system is shown in Figure 6.17. The DAQ was employed to generate the stimulus and control signal and to read the lock-in ADC's output. Eight miniaturized gold electrodes were patterned on the glass chip, and then biosensor interfaces (described below) were self assembled onto the electrode. The bulk metal around the round electrode serves as the counter electrode, where the 5mV sinusoid

TABLE 6.2. THE PERFORMANCE SUMMARY OF THE QSSG

Technology	0.5um CMOS, 3volts
Die area	1mm^2
Power Consumption	60uA
Frequency range	1m Hz ~ 10K Hz
Phase mismatching	<0.8°
Amplitude mismatching	<3%
Linearity	>44dB

stimulus signal is applied. The lock-in ADC extracts the response from one electrode on the array at a time.

With the assistance of collaborators from Chemical Engineering, tBLM sensor interfaces were fabricated onto the gold electrodes. Briefly, a self assembled monolayer (SAM) of 1,2-dipalmitoyl-sn-glycero-phosphothioethanol (DPPTE) tether lipid was formed on a clean gold electrode by placing the array in a 1mM ethanolic solution of DPPTE for 24 hrs. A tethering lipid DPPTE has a terminal thiol group that forms a covalent bond with a gold surface and creates an organized SAM. The SAM modified gold was washed in ethanol to remove unabsorbed lipid molecules and dried under nitrogen. The upper leaflet of the bilayer was deposited by fusion of vesicles made of 1,2-dioleoyl-sn-glycero-phosphocholine (DOPC) mobile lipids. Excess liposomes were replaced with fresh electrolyte solution after the tethered bilayer lipid membrane (tBLM)

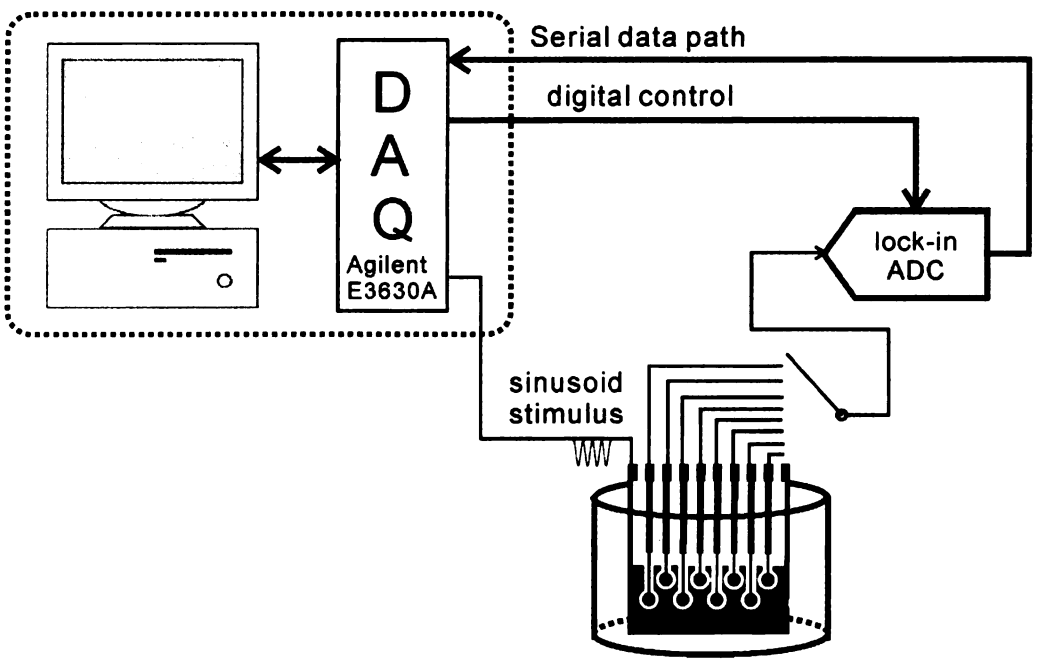


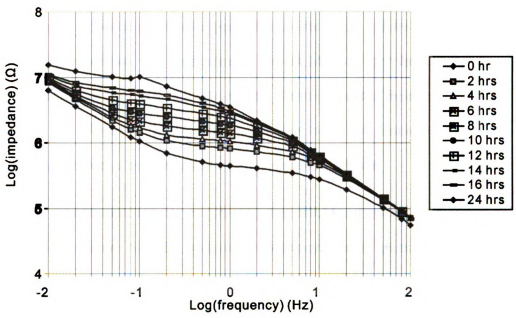
Figure 6.17. The experiment setup for the real biosensor impedance extraction.

formation. Impedance measurements were conducted in a 100mM sodium chloride solution over the frequency range of 10 mHz to 100 Hz.

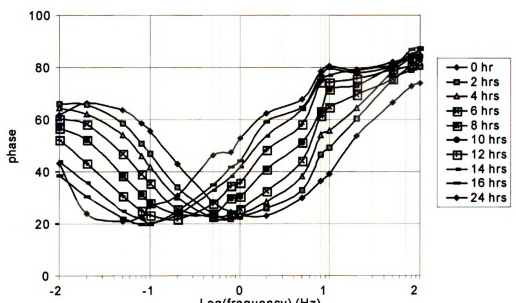
6.3.2 Experimental results

Prior experiments have shown that it is useful to monitor the quality of the biosensor interface during its formation on the electrode. Thus, this procedure was chosen as the subject of experiments to characterize the lock-in ADC. Figure 6.18 shows the impedance changes of the tBLM after the upper leaflet of the bilayer was deposited by the fusion of vesicles (DOPC). 0 hours result means the base impedance of the SAM. These plots show that the impedance increases over time as the upper layer forms, as expected. The impedance data were fitted to the modified Randles's equivalent circuit shown in Figure 3.1(b) using Z-view software (Scribner Associates, Inc., Southern Pines, NC). The equivalent circuit is a combination of a resistor and capacitors that can be related to the physical characteristics of the biointerface. The membrane capacitance (C_m) and the membrane resistance (R_m) are modeled in a parallel arrangement as they represent the properties of the bilayer membrane. For a DPPTE monolayer, the C_m and R_m values were found to be 0.635 $\mu F/cm^2$ and 20 $K\Omega cm^2$, respectively. For the tBLM, C_m and R_m values of 0.505 $\mu F/cm^2$ and 425 $K\Omega cm^2$ were observed. The capacitance value for the tBLM is in good agreement with the reported values for high quality BLMs on an interface[60]. However, a slightly lower value was obtained for membrane resistance suggesting there may have been some pinhole defects in tBLM. One possible reason is that the defects were mainly at the edges of the electrode where SAM formation was not perfect. The molecules at the edges have a smaller number of molecules surrounding them, resulting in less hydrophobic interactions and disordered arrangement of lipids.

Even so, we were able to obtain the electrochemical parameters of a tBLM in the frequency range under study.



(a)

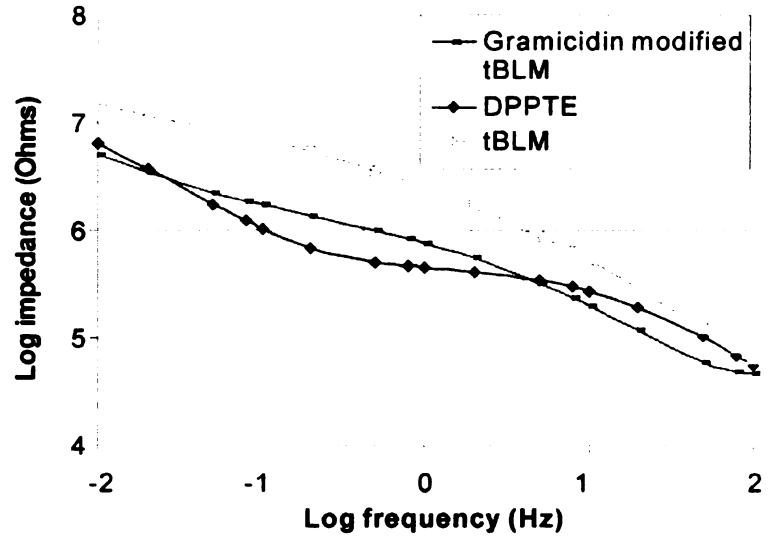


(b)

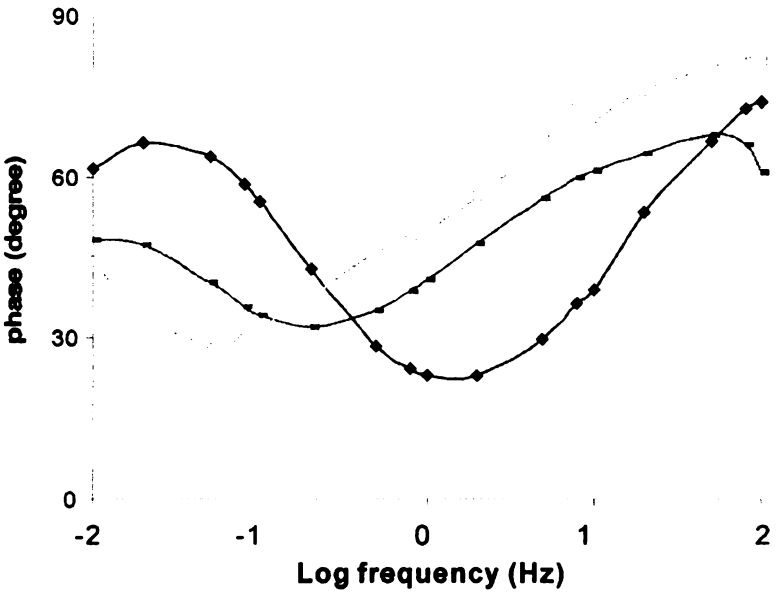
Figure 6.18. Impedance of monolayer and tBLM: (a) magnitude, (b) phase.

After the tBLM measurements, a 1 μM concentration of gramicidin ion channel protein was introduced to the electrolyte solution. Gramicidin exists as a dimer that is known to incorporate itself almost spontaneously in a pre-formed tBLM. The monomers get partitioned in lower as well as upper leaflets of the tBLM and are able to move freely within each monolayer. The fluid nature of the tBLM allows for the free movement of these gramicidin monomers within the sensor. The alignment of these monomers creates a channel that allows the passage of ions through the tBLM. Gramicidin ion channels selectively transport alkali metal ions through the cell membrane.

The impedance of monolayer (DPPTE), pure tBLM and gramicidin modified tBLM are plotted in Figure 6.19 for comparison. Incorporation of gramicidin in the tBLM decreased the membrane resistance from 425 to 59 $k\Omega cm^2$ due to the passage of sodium ions through tBLM. These results show that the gramicidin ion channels respond to alkali metal ions in the solution through a significant change of membrane impedance.



(a)



(b)

Figure 6.19. Impedance of monolayer, tBLM and gramicidin modified tBLM, (a) magnitude, (b) phase.

6.3.3 Discussion

The measurement of gramicidin activity demonstrates that the circuit developed in this dissertation can be similarly used to measure the activity of different proteins based

biomimetic interfaces using a platform that is small enough to support a large array of such sensors with (or on top of) a single microelectronic chip. Using an array of compact lock-in ADC cells, multiple measurements can be done at the same time, allowing for simultaneous address and monitoring of molecular events by each electrode on the chip.

6.4 Conclusion

The feasibility of the VLSI realization of the compact quadrature sinusoid signal generator and compact impedance extractor and digitizer is critical for the success of multi-channel EIS biosensor array microsystem. In this chapter, the silicon realization of these two critical blocks was characterized and verified with a series of experiments. The quadrature signal generator can produce quadrature sinusoid waveforms with good IQ matching over seven orders of frequency range (1mHz to 10kHz). The lock-in ADC can extract the impedance information with a sensitivity of up to 0.1pA of amplitude and has successfully extracted and digitized the impedance information for the gramicidin modified tBLM biosensor. These results show that the designed signal generator and impedance extracting/digitizing circuit function as they were designed to and can support impedance extraction in the biosensor microsystems. The circuits developed in this thesis research enable a chip-scale realization of an EIS sensor array microsystem.

7 Summary and Future Work

7.1 Summary of the contributions

Microsystems that integrate a miniaturized biosensor array atop a silicon chip and interrogate each sensor element electrochemically using integrated electronics within the chip have a tremendous advantage over existing alternatives. This dissertation developed the electrical systems and circuits for an impedance spectroscopy-based biosensor array microsystem to address the special issues related to a large scale miniaturized biosensor array. Two system level approaches for the electronics of the microsystem were developed. For one of these systems, prototype functional blocks were developed and fabricated, and verified. The results of this research provide a solid basis for future research on all aspects of biosensor microsystems.

7.1.1 Proposed two architectures for the IS biosensor microsystem

Two new options for the interface electronics of a biosensor array based impedance spectroscopy microsystem have been designed. Both of them are based on a frequency response analyzer (FRA), which enables the compact IC realization of a full IS system. One significantly decreases the interrogation time at low frequencies (sub-hertz or lower) through eliminating the integrators used in a conventional FRA based structure and performing its function with complex signal processing in the analog domain. The other one features high accuracy and compact size so that it can provide multi-channel in-parallel interrogation for every sensor element. The VLSI realization of the key functional blocks for the second one was also developed in this dissertation because it provides higher accuracy and can support a wider range of sensor types.

7.1.2 The smallest known impedance extractor and digitizer circuit

In this dissertation, a novel compact IS readout circuit was developed and fabricated with the AMI 0.5μm CMOS technology. Its physical size is only 0.06mm^2. A 3mm by 3mm silicon die it can integrate more than 100 of these IS circuits, which is enough for anticipated microsystem needs. This lock-in ADC circuit not only extracts the impedance information of the biosensors but also digitizes this information locally so that the results for the whole array can be read with a serial interface to conserve pad resources. Incorporating several innovative circuit blocks and methodologies, the new lock-in ADC provides all of the features of a traditional IS measurement system within an ultra compact integrated circuit that is many orders of magnitude smaller than all reported alternatives.

7.1.3 The widest frequency range quadrature sinusoid signal generator

An on-chip stimulus sinusoid generator is a necessary component for a stand-alone IS microsystem. Many biosensors are measured with low frequency stimulus, i.e. from 1mHz to 10kHz. At the integrated circuit level, there are no known options to cover this wide frequency range of seven orders of magnitude. Thus, a novel hybrid signal generator structure was developed and silicon-verified with the AMI 0.5μm CMOS technology. It generates a quadrature sinusoid signal (both sine and cosine signals) covering the above mentioned frequency range with inherently guaranteed matching between the signals. The performance of the new signal generator is outstanding for many sensor applications and the very small size (~1mm^2) makes it ideally suited for use in integrated microsystems.

7.2 Future work

Based on the results of this dissertation, the following suggestions for future research are made.

7.2.1 Fully integrated IS microsystem

The channel-wise compact IS circuit and the compact wide frequency range quadrature sinusoid signal generator represent two hardware hurdles for the fully integrated multi-channel IS microsystem. These hurdles have been overcome during this dissertation, in which those two blocks have been designed and their performances have been verified with real chip experiments. The results validate the concept of the integrated IS microsystem proposed in Chapter 3. Thus, the next step is to develop the fully integrated electronic system for this IS microsystem.

A conceptual system diagram for a fully integrated IS microsystem is proposed in Figure 7.1. This system employs one quadrature sinusoid signal generator that generates the stimulus for all of the biosensor elements in the array. For each biosensor element, one dedicated compact IS readout circuit is used to extract and digitize the impedance information. To provide a more generic interface, a three electrode system is adopted for each biosensor. A half-amplifier is used to support the three electrode system for each biosensor. All the half-amplifiers within the same column share a common second half amplifier. This half-amplifier concept was developed for an infrared imaging system[103, 104] and a potentiostat circuit[105]. This half-amplifier can save hardware area. Different elements in the array may have different DC bias settings. This can be achieved by setting the WE potential individually through configuring the DC point of the lock-in ADC's input. A block that sets every element's WE potential according to the input

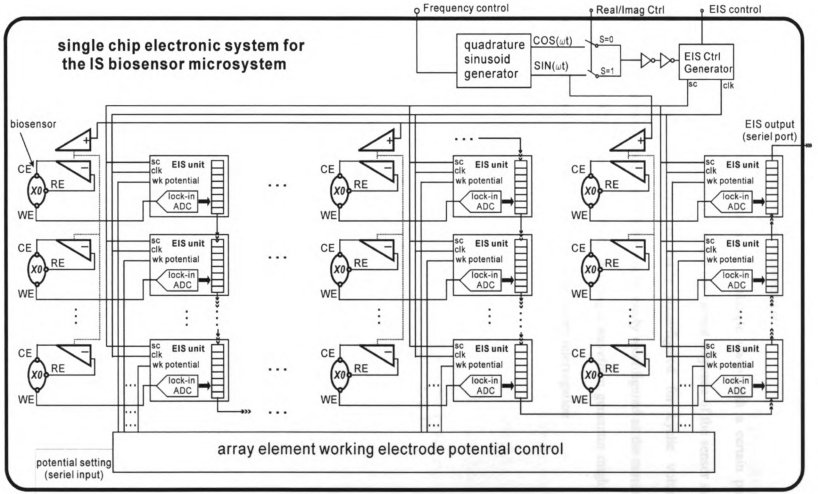


Figure 7.1. Proposed electronic system for the impedance spectroscopy biosensor array based microsystem.

7.2.2 Extension to cyclic voltammetry measurement

In cyclic voltammeter measurement, a triangle wave with a certain pattern is applied as the stimulus to a potentiostat and the current response of the sensor system is measured. The proposed system is easily reconfigured for cyclic voltammetry applications, and the proposed integrator can be easily reconfigured as the current mode continuous time (CT) Sigma-Delta ADC. A triangle waveform generator might also be required to generate the stimulus for cyclic voltammetry interrogation

Appendix. Response of the tBLM biosensor to frequency change

Let the frequency change happens at t=0+. We can express the source as:

$$V(t) = \sin(\omega_0 t) - \sin(\omega_0 t) \cdot u(t) + \sin(\omega_1 t) \cdot u(t) \tag{A.1}$$

where $u(t)$ is the step function. The first term in (4.1) is ignored because it represents a stable periodic signal and is easy to be added back in a linear system, like the tBLM circuit model. We will add its response later in the result directly. To facilitate this derivation, the analysis is performed in S domain, where only the signals after time 0+ are studied. By ignoring the first term, (A.1) become (A.2),

$$V_1(t) = -\sin(\omega_0 t) \cdot u(t) + \sin(\omega_1 t) \cdot u(t) \tag{A. 2}$$

Its Laplace transformation is

$$V_1(s) = -\frac{\omega_0}{s^2 + \omega_0^2} + \frac{\omega_1}{s^2 + \omega_1^2} \tag{A.3}$$

The transfer function of equivalent circuit in Figure.3.1 is

$$Z(s) = \frac{1}{g_m + s \cdot C_1} + \frac{1}{s \cdot C_2} \tag{A.4}$$

So the current response of the circuit is

$$I(s)=\frac{V}{Z}=\frac{V_1(s)}{Z(s)}=\frac{-\frac{\omega_0}{s^2+\omega_0{}^2}+\frac{\omega_1}{s^2+\omega_1{}^2}}{\frac{1}{g_m+s\cdot C_1}+\frac{1}{s\cdot C_2}}$$

$$=\frac{\omega_1}{s^2+\omega_1{}^2}\cdot\frac{(g_m+s\cdot C_1)\cdot s\cdot C_2}{g_m+s\cdot(C_1+C_2)}-\frac{\omega_0}{s^2+\omega_0{}^2}\frac{(g_m+s\cdot C_1)\cdot s\cdot C_2}{g_m+s\cdot(C_1+C_2)} \qquad (A.5)$$

$$=\frac{A_1}{s+j\omega_1}+\frac{A_2}{s-j\omega_1}+\frac{A_3}{s+j\omega_0}+\frac{A_4}{s-j\omega_0}+\frac{A_5}{g_m+s\cdot(C_1+C_2)}$$

where, $A_1=(s-j\omega_1)\cdot I(s)\big|_{s=j\omega_1}$, $\quad A_2=(s+j\omega_1)\cdot I(s)\big|_{s=-j\omega_1}$

$A_3=(s-j\omega_0)\cdot I(s)\big|_{s=j\omega_0}$, $\quad A_4=(s+j\omega_0)\cdot I(s)\big|_{s=-j\omega_0}$

$$A_5=(g_m+s\cdot(C_1+C_2))\cdot I(s)\big|_{s=-\frac{g_m}{C_1+C_2}}$$

$$=\left(\frac{\omega_0}{\left(\frac{g_m}{C_1+C_2}\right)^2+\omega_0{}^2}-\frac{\omega_1}{\left(\frac{g_m}{C_1+C_2}\right)^2+\omega_1{}^2}\right)\left(\frac{g_m\cdot C2}{C_1+C_2}\right)^2$$

(5) can also be expressed as:

$$I(s)=\frac{(A_1+A_2)+(A_2-A_1)j\omega_1}{s^2+\omega_1^2}+\frac{(A_3+A_4)+(A_4-A_3)j\omega_0}{s^2+\omega_0^2}+\frac{A_5}{g_m+s\cdot(C_1+C_2)} \qquad (A.6)$$

Transforming (6) into time domain, we get,

$$I(t)=\frac{A_5}{(C_1+C_2)}e^{-\frac{g_m}{C_1+C_2}t}$$
$$+(A_3+A_4)\cos(\omega_0 t)+(A_4-A_3)\sin(\omega_0 t) \qquad (A.7)$$
$$+(A_1+A_2)\cos(\omega_1 t)+(A_2-A_1)\sin(\omega_1 t)$$

In (7), first term present the transition effect; the terms in second line present the stable response for $-\sin(\omega_0 t)$; and 3rd line terms present the stable response for $\sin(\omega_1 t)$.

(7) shows the time domain response for (2), now we can easily derive the time domain response for (1). As the first term in (1) present a stable stimulus, the response to it should also be stable. Also the stable response to the second term in (1) should cancel that of the first term in (1), as the first two term will cancel each other after t=0+. At stable response of (1), we should not see any response to $\sin(\omega_0 t)$. Assuming that a frequency change happens at t=0, the response of the (1) is

$$\begin{aligned} I(t) &= \frac{A_5}{(C_1+C_2)} e^{-\frac{g_m}{C_1+C_2}t} + (A_1+A_2)\cos(\omega_1 t) + (A_2-A_1)\sin(\omega_1 t) \\ &= \frac{A_5}{(C_1+C_2)} e^{-\frac{1}{Rm(C_1+C_2)}t} + (A_1+A_2)\cos(\omega_1 t) + (A_2-A_1)\sin(\omega_1 t) \end{aligned} \tag{A.8}$$

(A.8) can be represented as

$$I(t) = \frac{A_5}{(C_1+C_2)} e^{-\frac{1}{Rm(C_1+C_2)}t} + A\cdot\sin(\omega_1 t+\varphi) \tag{A.9}$$

where second term represents the sensor's stable response, and first term will die out eventually.

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