TRANSISTOR LARGE SIGNAL ANALYSIS

Thesis for the Degree of Ph. D
MICHIGAN STATE UNIVERSITY
HELMY HASSAN ELSHERIF
1964


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TRANSISTOR LARGE SIGNAL ANALYSIS

By

Helmy Hassan ElSherif

AN ABSTRACT

Submitted to
Michigan State University
in partial fulfillment of the requirements
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Department of Electrical Engineering

1964

Approved by 

Abstract

by

Helmy H. ElSherif

A problem of major concern in recent years is a description of the transistor from the point of interest of the circuit designer. This thesis devises an equivalent circuit that is a modification of the charge control model of the transistor.

The equation describing the base emitter junction is modified to include the effects of the base resistance and the variation of the saturation current with the collector to emitter voltage. Also a partially saturated region of operation is introduced to more accurately predict the base control charge.

The relative importance of the different charge control model capacitances in predicting the circuit operation is investigated and curves are presented showing the significance of each.

A computer program is developed which reduces the transistor model to a form which can be treated independent of the circuit in which it is connected. This reduced representation is in the linear graph form.

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A THESIS

Submitted to
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TO MY MOTHER

AND

TO A FRIEND

ACKNOWLEDGMENTS

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LIST OF SYMBOLS

BASCUR	Current through base lead
C	Capacitance
CBE	Base emitter junction capacitance
CBEX	Stray capacitance between base and emitter leads
CBC	Base collector junction capacitance
CBCX	Stray capacitance between base and collector leads
CCEX	Stray capacitance between emitter and collector leads
COLCUR	Current through collector lead
D_n	Electrons diffusion length
D	The derivative w.r.t. time, d/dt
I	Current through a P-N junction
I_o	Saturation current of a P-N junction
I_{BE} = XIBE	The current through base emitter diode
I_B	Base current
I_C	Collector current
I_{BC} = XIBC	Current that would flow through base collector diode
K = XK	Boltzmann's constant
L_n	Diffusion length of electrons
L_p	Diffusion length of holes
N_a	Concentration of acceptors
N_d	Concentration of donors

Q_B	Base control charge
q = Q	Electronic charge
QS	Storage charge in the base region
RBB	Resistance of base semiconductor material
RCC	Resistance of collector semiconductor material
T = TEMP	Temperature of junction
T_E = TE	Emitter time constant
T_B = TB	Base time constant
T_C = TC	Collector time constant
V_o = VO	Contact potential of a P-N junction
V_t	Effective voltage across junction
V_{ap}	Applied voltage across junction
VBE	Voltage between base and emitter leads
VBEIN	Voltage across base emitter junction
VBB	Base emitter bias voltage
VCC	Collector emitter bias voltage
VIN	Input signal between base and emitter leads
VCE	Collector emitter voltage
XIBX	Component of base emitter current that contributes to the build up of the storage charge in the base QS
XIB	Component of base emitter current that contributes to the build up of the base charge QB
XICIN	Internal collector current
XIBIN	Internal base current
W	Width of the base region
α_N	Normal common base current gain
β	Common emitter current gain

CHAPTER I

INTRODUCTION

The transistor is one of the most important components of today. It is being used extensively in all areas of electronics. There are a number of equivalent circuits that describe the transistor,[1] however, they are limited to small signal conditions.

The dc current equation for a p-n junction is given by;

$$I = I_o(e^{\frac{qV}{kT}} - 1) \tag{1.1}$$

The small signal equivalent circuits make the assumption that the voltage applied to the junction V is much less than $\frac{kT}{q}$ and hence equation (1.1) can be approximated by

$$I = I_o(1 + \frac{qV}{kT} - 1) = \frac{I_o qV}{kT} \tag{1.2}$$

The advancement of the computer industry, the development of micro electronic circuitry and the fact that the transistor is very often driven beyond the small signal region of operation, make equation (1.2) a poor approximation of the actual operation. This has brought about the necessity to develop an equivalent circuit for the transistor that can describe the large signal behavior as well as the small signal behavior.

In 1957, Beauffoy and Sparkes[2] developed a charge control model for the transistor. They represented the device in saturation

saturation the same way as Ebers and Moll[3], as two transistors in parallel, one operating normally and the other in reverse (collector operating as emitter and emitter as collector). Though satisfactory for devices of symmetric geometric construction, it is not adequate for asymmetric ones of more complicated geometry.

The existence of system analysis programs, [4] that made use of linear graph techniques makes it desirable to have the transistor model in a reducable representation as in Fig. (1.1).

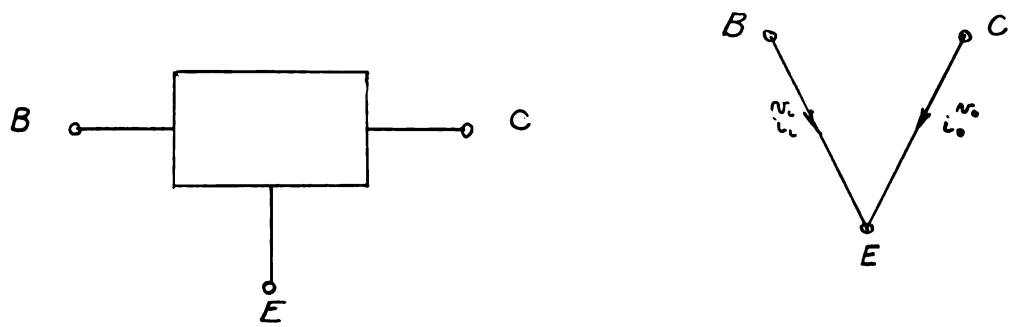


Fig. (1.1) Linear Graph Representation of the Transistor

One variable associated with each group element will be specified and the other must be obtained. The material that follows fulfills this requirement and can be divided into three major sections.

Chapter 2 discusses the modification and description of the charge control equivalent circuit devised by Beauffoy and Sparkes[2] and discusses the different nonlinear elements and their mode of variation.

Chapter 3 presents the details of a digital computer program that performs the required analysis based on the results of Chapter 2. It also gives the state model of the transistor in the four different modes of operation.

Chapter 4 shows a comparison between the experimental and calculated results.

CHAPTER II

TRANSISTOR LARGE SIGNAL EQUIVALENT CIRCUIT

2.1 Transistor Large Signal Performance

The transistor is a three terminal device. It is either a PNP or an NPN with the N region or the P region respectively being the base. Anyone of the two P regions or the two N regions can act as an emitter and the other as a collector. When the terminal designated by the manufacturer to be the emitter is used as an emitter, the transistor is said to be operating under normal conditions. When the terminal designated as collector is used as an emitter, the transistor is said to be operating under inverse conditions. In either case, the performance of a transistor under large signal conditions can be divided into four separate regions:

a. Cut-Off Region

   In this region both junctions are reverse biased.

b. Normal Active Region

   Here, the emitter-base junction is forward biased, while the base-collector junction is reverse biased.

c. Partial Saturation Region

   In this case of operation, both junctions are forward biased, yet the voltage across the base-collector junction will permit a current flow in the forward direction that is much less that the base current, in magnitude.

d. Complete Saturation Region

Both junctions are forward biased, and the voltage across the base-collector junction will permit a current flow in the forward direction, of the same order of magnitude as the base current.

The discussion from now on will be restricted to NPN transistors, but the analysis will be equally valid for PNP transistors provided suitable substitutions of sign are made.

Fig. (2.1) shows the charge distributions of both holes and electrons in the base region for the four cases of operation. The gradients are approximately linear and are proportional to the net current flowing from the emitter to the collector.

L. J. Giacoletto,[12] showed that the base region is not an equipotential. The total charge in the base region (which changes parabolically with distance) can be approximated as shown in Fig. (2.1) which holds during both turn on time and turn off time for the greatest majority of cases.

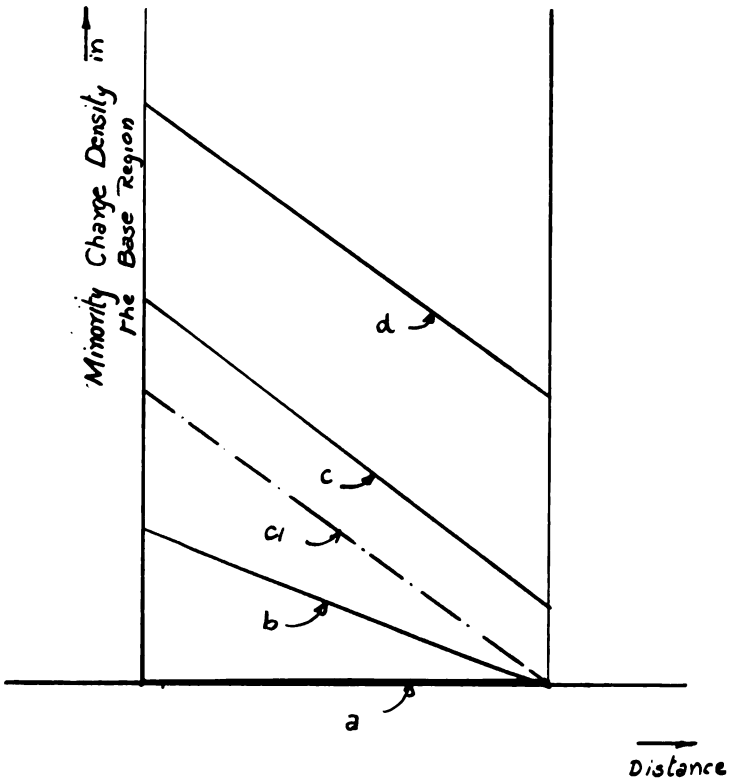
2.2 Cut-Off Region

In the cut-off region only, an equilibrium concentration of electrons and holes exists and the base charge can, for all practical purposes be taken as equal to zero.

2.3 Normal Active Region

It has been shown[2] that the base charge Q_b, of electrons (and of holes in excess of the number of impurity atoms) is given by:

$$Q_B = \frac{W^2 I_E}{2D_n} \qquad (2.1)$$



Case a: $V_{be} < 0$; $V_{bc} < 0$

Case b: $V_{be} > 0$; $V_{bc} < 0$

Case c: $V_{be} > 0$; $V_{bc} > 0$, the difference between C1 and c show the storage charge in this case.

Case d: $V_{be} > 0$; $V_{bc} >> 0$, the difference between C1 and d is saturation charge.

Fig. (2.1) Charge Distribution in the Base of an NPN Transistor

(The dimension of $\frac{W^2}{2D_n}$ is $\frac{cm^2}{cm^2/sec}$ = sec)

Defining now, three time constants

a. T_E, the emitter time constant = $\frac{Q_B}{I_E}$

b. T_B, the base time constant = $\frac{Q_B}{I_B}$

c. T_C, the collector time constant = $\frac{Q_B}{I_C}$

Equation 2.1 can be rewritten in the form:

$$Q_B = T_E \cdot I_E = \frac{W^2 I_E}{2D_n} \tag{2.2}$$

The base current is given by

$$I_B = (1 - \alpha_N) \cdot I_E$$

$$= (1 - \alpha_N) \cdot Q_B/T_E = Q_B/T_B \tag{2.3}$$

$$T_B = T_E/(1 - \alpha_N) \tag{2.4}$$

and α_N is the normal common base current gain.

$$I_C = \alpha_N I_E = \alpha_N Q_B/T_E = Q_B/T_C \tag{2.5}$$

$$T_C = T_E/\alpha_N \tag{2.6}$$

Also, since the common emitter current gain β is given by

$$\beta = \alpha_N/(1 - \alpha_N) \tag{2.7}$$

and

$$T_E = (1 - \alpha_N)T_B$$

$$T_C = T_E/\alpha_N = (1 - \alpha_N)T_B/\alpha_N$$

it follows that

$$T_B = \beta T_C \tag{2.8}$$

The Equivalent Circuit:

Fig. (2.2) shows the equivalent circuit of a transistor operating in the normal active region.

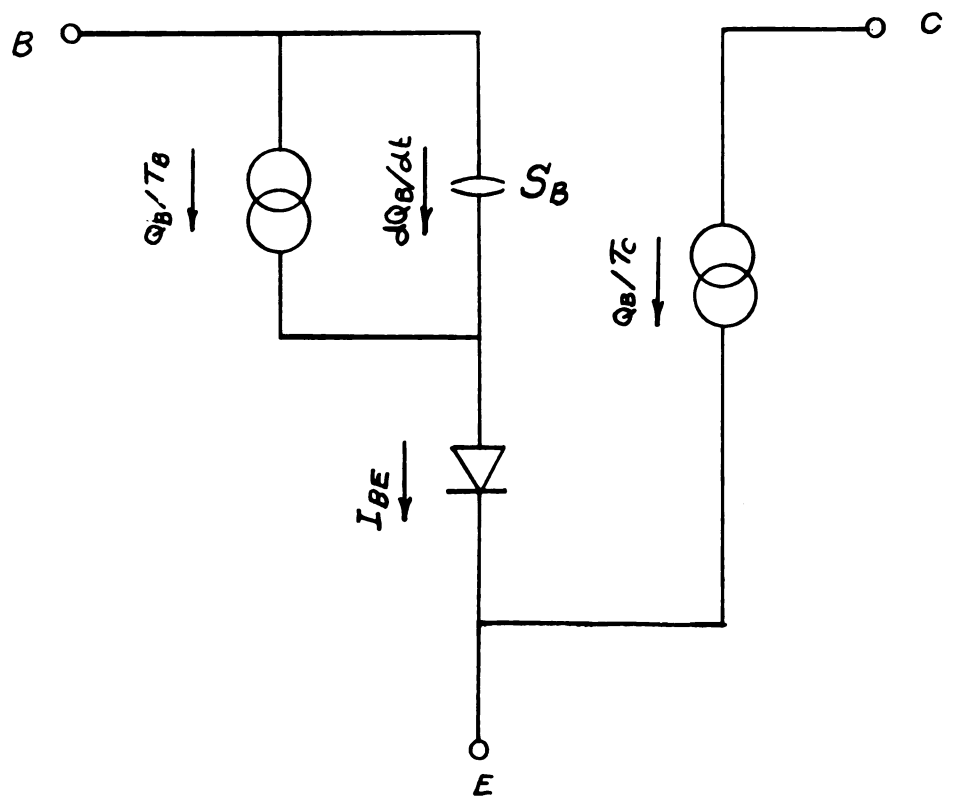


Fig. (2.2) Ideal Large Signal Equivalent Circuit for the Normal Active Region

The base current, via the effect of the base emitter junction will cause the total base control charge, Q_B, to build up in the base storage capacitance, S_B, which is an infinite capacitance in the sense that it accumulates the charge entering the base region without generating a potential difference between the base and emitter junction connections to it. Thus, in the absence of the base resistance any potential difference between the emitter and base terminals appears across the base emitter diode.

The diode represents the actual base emitter junction behavior. Due to the charge recombination in the base, a base current flows which is represented by Q_B/T_B in Fig. (2.2). The other current generator is a charge dependent one and gives the collector current I_C as

$$I_C = Q_B/T_C \tag{2.9}$$

There are some imperfections other than the recombination in the base and these are listed as:

1. The collector cut-off current I_{CO}, consists of a steady current of electrons from the base into the collector. I_{CO} is usually in the microampere range and can be neglected for all practical reasons.

2. The base resistance R_{BB}', arises from the resistivity of the semiconductor forming the base region. Its presence means that neither lossless nor instantaneous charge injection can be achieved.

3. Junction Capacitances Whenever the collector voltage or the emitter voltage changes, the corresponding transition region (the region in which the electrostatic potential is changing) width also changes, resulting in a variation of the base width. The sign of the changes in each case is such that when the emitter collector current is increased, both transition regions decrease in width.

It has been shown[5] that both capacitances can be given by:

$$C = k(V_o - V_{ap})^n \qquad (2.10)$$

where

k and n are constants

V_o is the contact potential, a positive quantity

and V_{ap} is the internal voltage across the junction

4. Collector Resistance R_C, arises from the resisitivity of the semi-conductor forming the collector region.

Figure (2.3)[2] shows the equivalent circuit for the actual nonsaturated transistor.

The characteristics of the emitter junction, base resistance, and the collector resistance will be discussed later.

The charge in the base is governed by:

$$I_B = Q_B/T_B + dQ_B/dt \qquad (2.11)$$

where, I_B is the base current flowing through the base emitter junction diode.

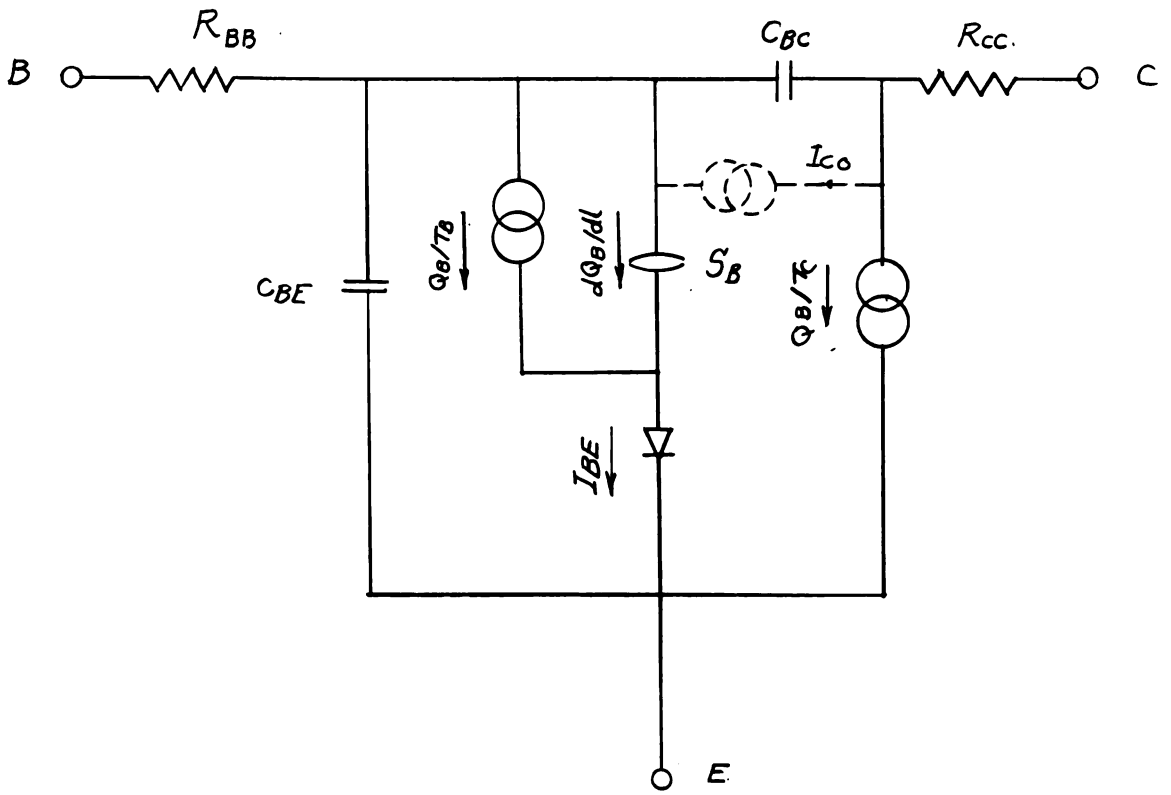


Fig. (2.3) Large Signal Equivalent Circuit for the Normal Active Region

2.4 Partially Saturated Region

Previously, the single definition of saturation has been that the base collector junction is forward biased.

It has been noticed that silicon devices saturate at collector to emitter voltages of about 0.2 - 0.3 volts, while the base voltage in this saturated condition is about 0.7 - 0.8 volts, or higher. According to the previous definition of saturation, the collector to emitter saturation voltage would be greater than 0.7 volts, which is not true.

The partially saturated region is defined as the region in which the base collector junction is forward biased, and in which the base control charge Q_B, and the storage charge Q_S are building up.

Referring to Fig. (2.1), the difference between curve C1 and C represent the storage charge Q_S, which in contrast to the control charge Q_B does not contribute to any increase in the collector current. Q_S can be considered as being supplied by two equal components of current, one through the base emitter diode and the other through the base collector diode.

In this partially saturated region, I_{BE} less the recombination current Q_B/T_B is greater than twice I_{BC}. Thus, a fraction of I_{BE} equal to I_{BC} will build up Q_S and the remainder of I_{BE}, namely $I_{BE} - I_{BC}$ will build up more base control charge, Q_B, in turn causing the collector current to increase. As shown in Fig. (2.4), S_s is an infinite capacitance in which Q_S is stored.

Hence Q_B and Q_S are controlled by the following equations:

$$I_B = Q_B/T_B + dQ_B/dt = I_{BE} - I_{BC} \qquad (2.12)$$

and

$$I_{BX} = Q_S/T_S + dQ_S/dt = I_{BC}$$

where

I_{BE} is the current through the base emitter diode

I_{BC} is the current that would be supplied by the collector-base diode

Q_B is the base control charge

Q_S is the base stored charge

Referring again to Fig. (2.1), the criterion for the partially saturated case is that the current I_{BE} less the recombination current in the base be twice the current that would flow through the base-collector junction I_{BC}. Thus,

$$(I_{BE} - Q_B/T_B)/2 > I_{BC} > 0 \qquad (2.13)$$

is the criterion for partial saturation.

Fig. (2.4) shows the equivalent circuit for the partially saturated transistor, which is also the same for the totally saturated case.

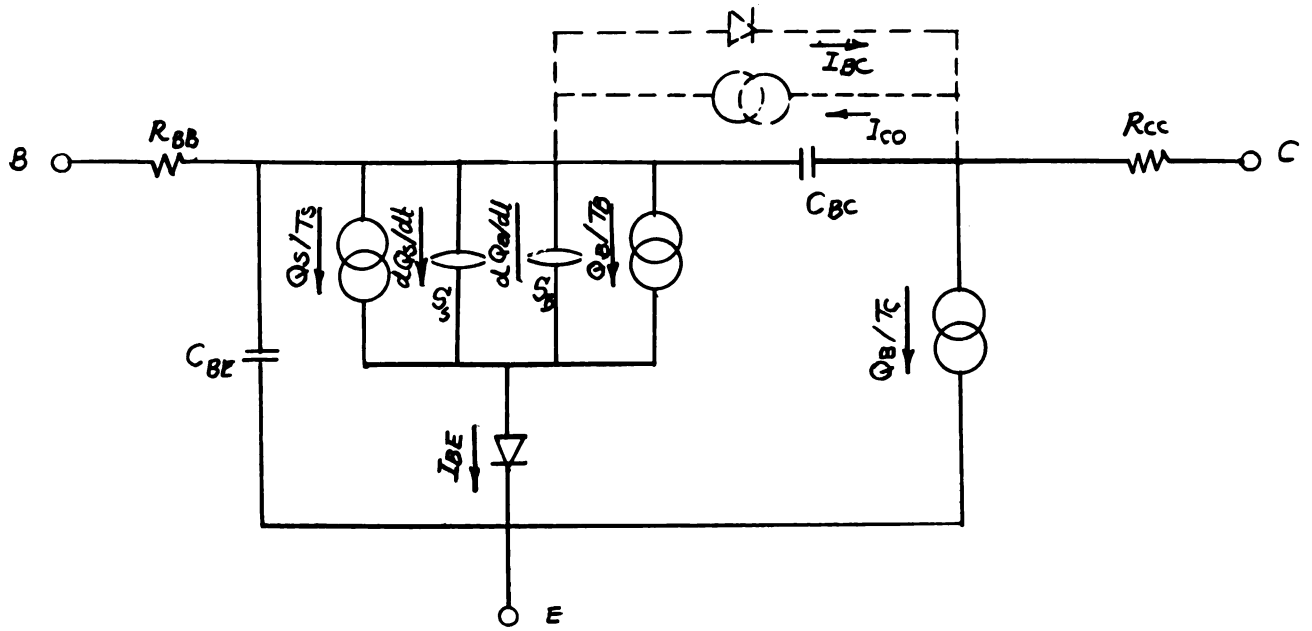


Fig. (2.4) Equivalent Circuit of a Transistor in Saturation

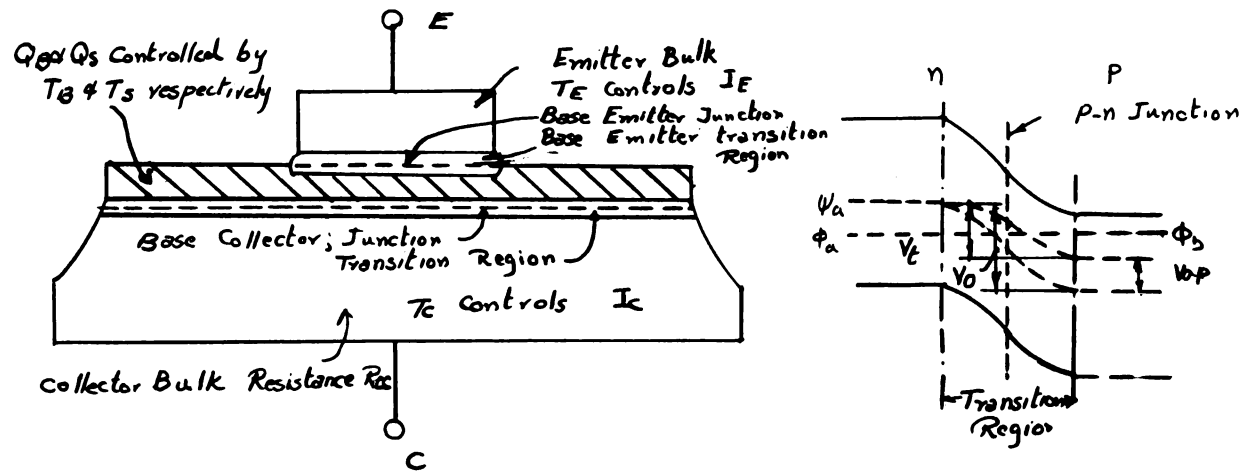


Fig. (2.5) Schematic Diagram Showing the Different Regions in a Transistor

The voltage level diagram, shown in Fig. (2.5) shows how the total voltage, V_t, across the junction, is related to the built in contact potential, V_o, and the applied voltage V_{ap}.

2.5 Totally Saturated Case

In this case, both junctions are forward biased and the bias on the collector base junction is such that:

$$I_{BC} > (I_{BE} - Q_B/T_B)/2 > 0 \qquad (2.14)$$

This excess current $(I_{BE} - Q_B/T_B)$, will not contribute to an increase of the base control charge Q_B, but will only contribute to the build up of the storage charge Q_S, and the presence of this storage charge will introduce delays that will be discussed in a later portion.

Fig. (2.4) gives the equivalent circuit of the totally saturated transistor and Equation (2.14) is the criterion for total saturation.

The diode shown between the base and collector represents the base collector junction.

2.6 Inverse Active Region

In this case, the discussion and equivalent circuit are the same as those of the normal active region with the exception that the collector is now acting as an emitter and the emitter is acting as a collector.

Fig. (2.5) shows a schematic diagram for the transistor showing how the different components are distributed.

2.7 Characteristics of the Base Emitter Diode Junction in a Transistor

Chih Tang Sah[6] showed that the current flowing through a semiconductor junction may be divided into four components according to the location of the recombination and generation of electrons and holes. These are:

1. Bulk recombination generation current.
2. Bulk recombination and generation current in the transition region.
3. Surface recombination and generation current.
4. Surface channel current.

The current through a p-n junction is thus the combination of these four components and is given by the following equation:

$$I = I_o \left(e^{(qV/mkT)} - 1\right) \qquad (2.15)$$

where,

V is the voltage directly across the junction.

Due to the presence of the base lead resistance and the resistance of the base semiconductor material, V is related to V_{BE}, the voltage applied between the base and emitter leads, by the following equation:

$$V = V_{BE} - I_{BE} \cdot R_{BB} \qquad (2.16)$$

Figure (2.6) shows the variation of the base emitter current, I_{BE} as a function of V_{BE}, with the collector emitter voltage as a parameter, for a Texas Instruments, 2N744 NPN epitaxial double diffused high speed mesa selicon transistor.

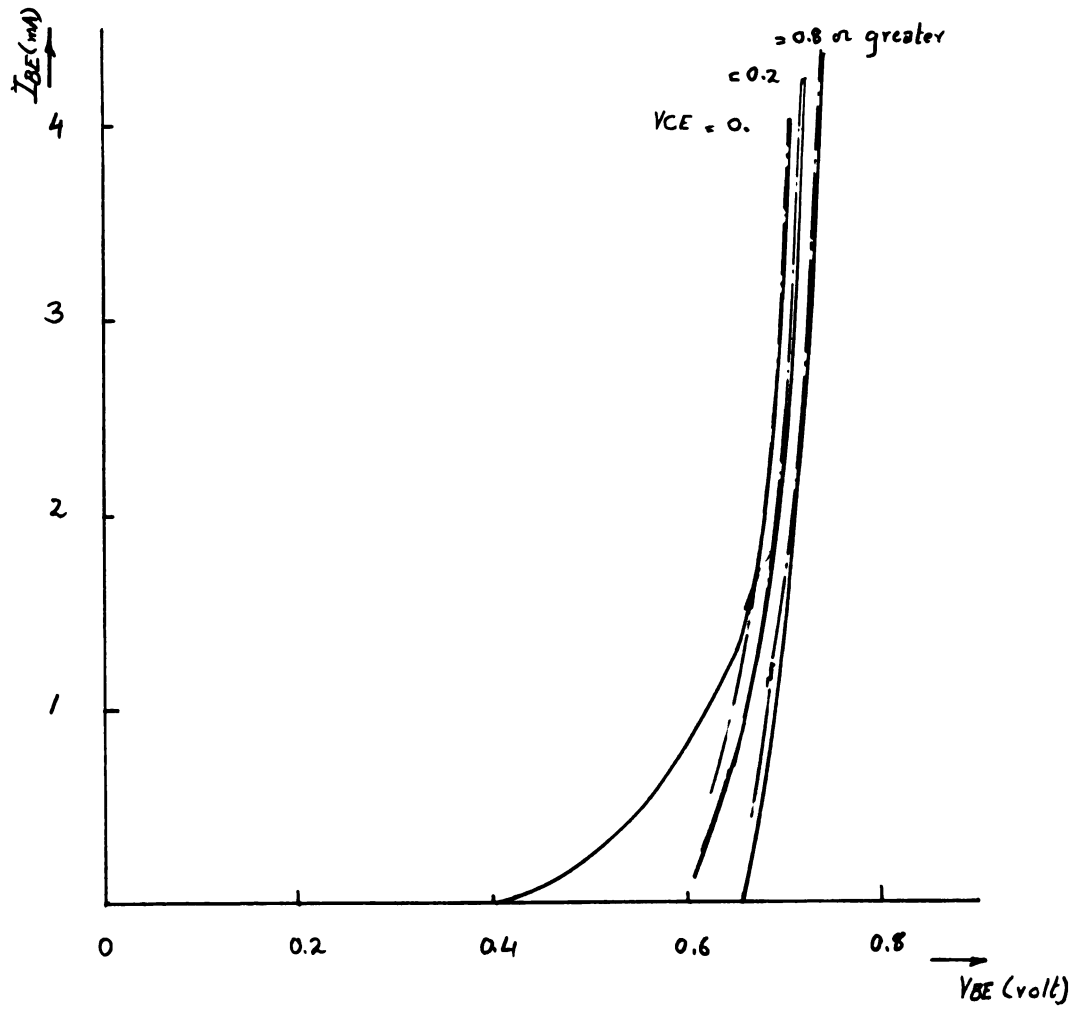


Fig. (2.6) Variation of I_{BE} with V_{BE}

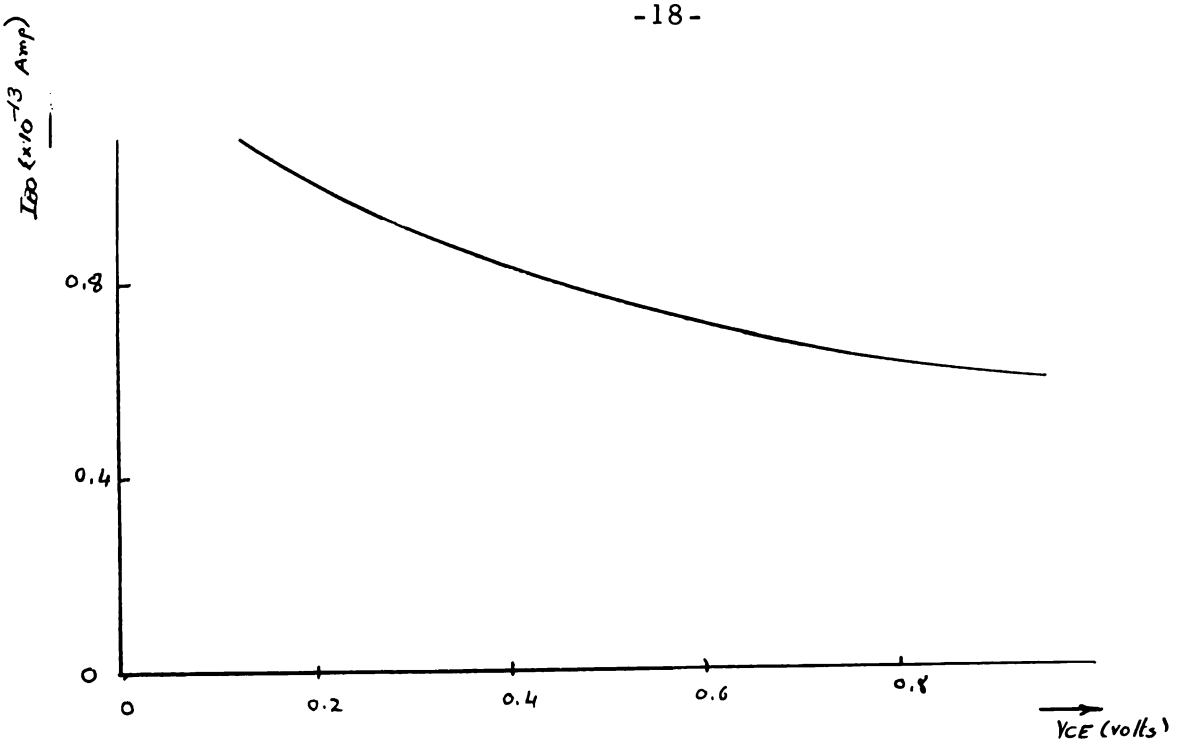


Fig. (2.7) Variation of I_{BEO} With V_{CE}

It was found*, that Equation (2.15) describes the curves in Fig. (2.6) to a very close approximation, with I_o being a function of V_{CE}, the collector emitter voltage. This relation is shown in Fig. (2.7). For the previous transistor the equation governing the base emitter current is

$$I_{BE} = I_{BEO} \cdot (e^{(35.3V_{BE} - 282.4 I_{BE})} - 1) \text{ Amp.} \qquad (2.17)$$

where,

I_{BEO}, is the saturation component of I_{BE}, and is shown in Fig. (2.7) as a function of V_{CE}.

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* A study done by the author at International Business Machines

The dashed curves in Fig. (2.6) show I_{BE} as calculated from Equation (2.17) and Fig. (2.7).

2.8 Summary

In this chapter, the transistor model was introduced, the partial saturation region has been defined, and an equation describing the current through the base emitter junction as a function of the collector emitter junction voltage was introduced.

In the following chapter, the state model of the transistor will be obtained and adapted to a computer analysis program.

CHAPTER III

TRANSISTOR STATE MODEL AND ITS ADAPTATION IN A COMPUTER ANALYSIS PROGRAM

A major contribution of this thesis is a computer program MISTAP (MIchigan State Transistor Analysis Program). MISTAP gives a linear graph representation of the transistor through the use of the transistor state model. Presuming that the characteristics of the device have already been stored in the computer, the user has to supply one set of input parameters and one set of output parameters, and MISTAP will supply the remaining two parameters. The results obtained through the use of MISTAP are sometimes within $\pm$ 3% and generally within 10% deviation.

To the knowledge of the author, MISTAP is the first program of its kind and handles the transistor from a completely general point of view.

3.1 Capabilities of MISTAP

1 - MISTAP can handle up to 50 different transistors.

2 - MISTAP can handle up to 20 different types of transistors.

(The capabilities supplied in 1 and 2 can be increased by increasing the size of the dimension statements.)

3 - MISTAP supplies to the user, a set of differential equations (derivatives of four different variables for each transistor), and gives the user the freedom to use any method he likes for their solution.

4 - The solution is accomplished in the shortest possible time, because at times when a fast transistor is operating in a slow circuit, most of the differential equations are replaced by linear and nonlinear algebraic equations, which are generally much faster to solve than the differential equations, (the algebraic solution is usually for time increments much longer than that required for integrating the differential equation).

5 - If under any conditions, some of the devices are operating under inverse conditions, (the collector acting as an emitter and the emitter acting as a collector), MISTAP will handle them in the same way, provided that their inverse characteristics are supplied.

3.2 Mode of Operation

First, the subroutine starts by comparing the circuit time constant to the transistor time constant (RBB.CBE), if the circuit time increment is greater than three times the device time constant, the solution is totally or partially by the use of nonlinear algebraic equations, otherwise it is accomplished through the use of differential equations.

Secondly, MISTAP will find the mode of operation of each device, transfers the inputs to those applicable to NPN devices and after the solution is completed it is transformed back to the correct conditions.

In solving for the necessary variables, MISTAP makes use of another four subroutines, MSTAP1, MSTAP2, MSTAP3, and MSTAP4. Before returning to the calling program, it compares its results with those obtained in a previous iteration, if the difference is less than a predetermined error, it will return to the calling program, otherwise it will call another subroutine, VAL, which has to be written by the circuit analyst and which will use the results of MISTAP to determine a more accurate set of inputs. Fig. (3.1) gives the block diagram of MISTAP.

When the voltage is specified and the current is the variable to be solved for algebraically the solution is by the use of the Newton Raphson Method[11], (Appendix I). When the current is the specified variable and the voltage is to be solved for algebraically this is done by the direct solution of the nonlinear algebraic equation (Appendix II).

In the following section, the different subroutines used in conjunction with MISTAP are discussed.

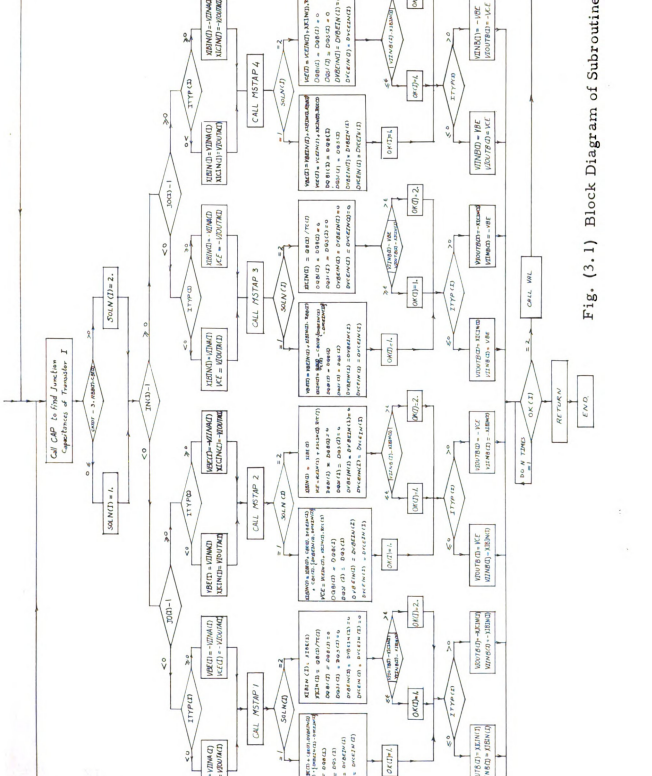

Fig. (3.1) Block Diagram of Subroutine MISTAP

3.3 Subroutine MSTAP 1

This subroutine expects to be supplied VBE and VCE and supplies back to MISTAP enough information to determine XIBIN and XICIN.

Evaluation of Differential Equations

With reference to the transistor equivalent circuit shown in Fig. (3.2),

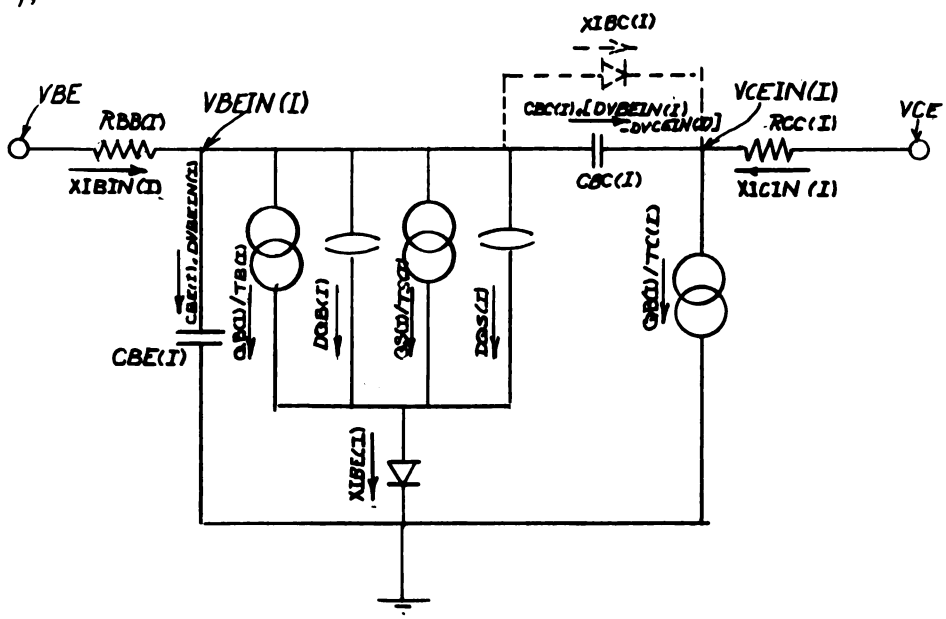

Fig. (3.2) Equivalent Circuit of Transistor I

$$VBE = VBEIN(I) + XIBIN(I) \cdot RBB(I) \qquad (3.1)$$

$$VCE = VCEIN(I) + XICIN(I) \cdot RCC(I) \qquad (3.2)$$

$$XIBIN(I) = XIBE(I) + (CBE(I)+CBC(I)) \cdot DVBEIN(I) - CBC(I) \cdot DVCEIN(I) \qquad (3.3)$$

$$XICIN(I) = QB(I)/TC(I) - CBC(I) \cdot (DVBEIN(I) - DVCEIN(I)) \qquad (3.4)$$

Substituting Equations (3.3 and 3.4) in Equations (3.1 and 3.2) and simplifying we get

$$DVBEIN(I) = \left[VBE-VBEIN(I)-XIBE(I).RBB(I) + (RBB(I)/RCC(I)).(VCE-VCEIN(I) - (QB(I).RCC(I))/TC(I)\right] / CBE(I).RBB(I) \quad (3.5)$$

$$DVCEIN(I) = \left[VCE-VCEIN(I) - (QB(I).RCC(I)/TC(I)) + (RCC(I).CBC(I)\cdot(VBE-VBEIN(I)-XIBE(I).RBB(I))/RBB(I).(CBE(I)+CBC(I))\right] / \left[CBC(I).CBE(I).RCC(I)/(CBE(I)+CBC(I))\right] \quad (3.6)$$

$$DQB(I) = XIB - QB(I)/TB(I) \quad (3.7)$$

$$DQS(I) = XIBX - QS(I)/TS(I) \quad (3.8)$$

Derivatives Supplied to MISTAP

$$DVBE1N(I) = DVBEIN(I) \quad (3.9)$$

$$DVCE1N(I) = DVCEIN(I) \quad (3.10)$$

$$DQB1(I) = DQB(I) \quad (3.11)$$

$$DQS1(I) = DQS(I) \quad (3.12)$$

(the terms on the left hand side of the equations 3.9, 10, 11, 12 are the terms that are integrated. Their solutions are: VBE1N(I), VCE1N(I), QB1(I), and QS1(I)).

Solution is by the use of Nonlinear Algebraic Equations

Here, the set of nonlinear algebraic equations to be solved are:

$$QS(I) = XIBX . TS(I) \quad (3.13)$$

$$QB(I) = XIB.\,TB(I) \tag{3.14}$$

$$XIBIN(I) = XIBE(I) \tag{3.15}$$

$$XICIN(I) = QB(I)/TC(I) \tag{3.16}$$

XIBE(I) is obtained through the solution of:

$$XIBE(I) = XIBEO(I).\ EXP(VBE-XIBE(I).RBB(I)).Q/XMBE.XK.TEMP(I)) - 1 \tag{3.17}$$

The solution of Equation (3.17) is performed by Newton Raphson method, for numerical solution of nonlinear algebraic equations, as shown in the block diagram Fig. (3.3). Also, the integrating program will have these values of derivatives available;

DQS1(I) = 0.0

DQB1(I) = 0.00

DVBEIN(I) = 0.00

DVCEIN(I) = 0.00

The state model in this case is:

$$\begin{bmatrix} DV_{BEIN} \\ DV_{CEIN} \\ DQ_B \\ DQ_S \end{bmatrix} = \begin{bmatrix} \dfrac{V_{BE}-V_{BEIN}-I_{BE}\cdot R_{BB}+\dfrac{R_{BB}}{R_{CC}}\left(V_{CE}-V_{CEIN}-\dfrac{Q_B}{T_C}R_{CC}\right)}{R_{BB}\cdot C_{BE}} \\ \dfrac{V_{CE}-V_{CEIN}-\dfrac{Q_B}{T_C}\cdot R_{CC}+\dfrac{R_{CC}\cdot C_{BC}}{R_{BB}(C_{BE}+C_{BC})}\left(V_{BE}-V_{BEIN}-I_{BE}\cdot R_{BB}\right)}{\dfrac{C_{BC}\cdot C_{BE}}{C_{BE}+C_{BC}}\cdot R_{CC}} \\ I_B-\dfrac{Q_B}{T_B} \\ I_{BX}-\dfrac{Q_S}{T_S} \end{bmatrix}$$

Fig. (3.3) gives the block diagram of subroutine MSTAP 1.

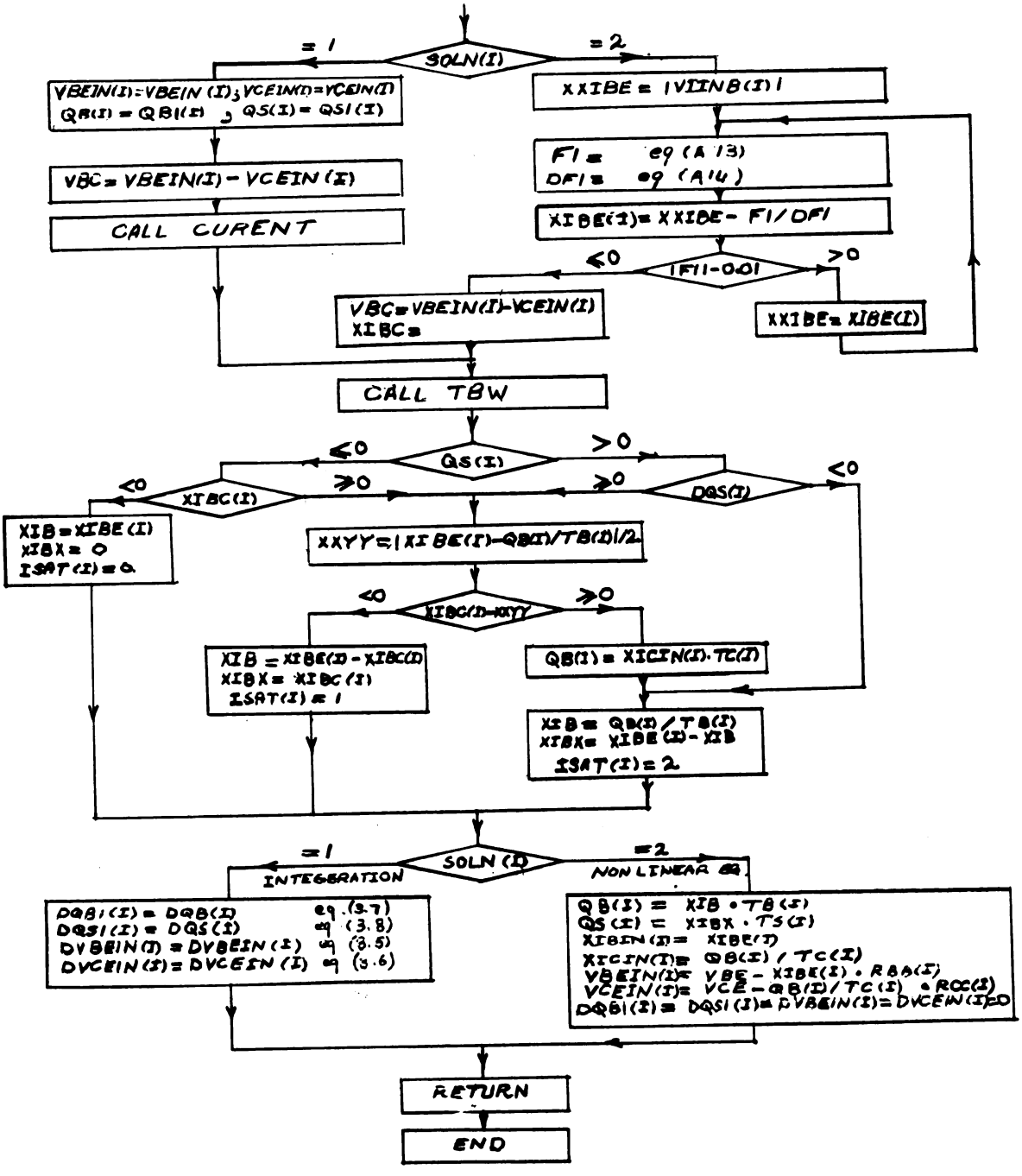

Fig. (3.3) Block Diagram of Subroutine MSTAP 1

3.4 Subroutine MSTAP 2

This subroutine expects to be supplied with VBE and XICIN(I) and it returns to MISTAP enough information to determine VCE and XIBIN(I).

Evaluation of Differential Equations

Referring to Fig. (3.2), and substituting Equation (3.3) in Equation (3.1), we get

$$VBE = VBEIN(I) + \left[XIBE(I)+(CBE(I)+CBC(I)) \cdot DBVEIN(I)-CBC(I) \cdot DVCEIN(I)\right] \cdot RBB(I) \qquad (3.18)$$

Solving Equation (3.4) and Equation (3.18) for DVBEIN(I) and DVCEIN(I), we get

$$DVBEIN(I) = \left[VBE-VBEIN(I)-XIBE(I) \cdot RBB(I)+XICIN(I) \cdot RBB(I)-(QB(I) \cdot RBB(I))/TC(I)\right] \; / \; RBB(I) \cdot CBE(I) \qquad (3.19)$$

$$DVCEIN(I) = XICIN(I)-(QB(I))/TC(I)+ [CBC(I) \cdot (VBE-VBEIN(I)-XIBE(I) \cdot RBB(I)]/[RBB(I) \cdot (CBE(I)+CBC(I))] \; / \; \left[CBC(I) \cdot CBE(I)/(CBC(I)+CBE(I))\right] \qquad (3.20)$$

together with

$$DQB(I) = XIB - QB(I)/TB(I) \qquad (3.21)$$

$$DQS(I) = XIBX - QS(I)/TS(I) \qquad (3.22)$$

Derivatives supplied to MISTAP

DQB1(I) = DQB(I)

DQS1(I) = DQS(I)

DVBE1N(I) = DVBEIN(I)

DVCE1N(I) = DVCEIN(I)

Solution is by the use of Nonlinear Algebraic Equations

In this case, we cannot solve for VCEIN algebraically, since its variation does not vary with any of the known quantities only and it is a function of the junction capacitances as well. Thus, in this case, VCEIN(I) has to be solved for by the use of the integration while the rest of the variables can be solved for algebraically.

The following are the set of algebraic and differential equations supplied back to MISTAP

QS(I) = XIBX . TS(I) (3.23)

QB(I) = XIB . TB(I) (3.24)

XIBIN(I) = XIBE(I)

This is obtained by the same way as in MSTAP1, together with

DQB1(I) = 0.00

DQS1(I) = 0.00

DVBE1N(I) = 0.00

DVCE1N(I) = DVCEIN(I)

State model in this case is :

$$\begin{bmatrix} DV_{BEIN} \\ DV_{CEIN} \\ DQ_B \\ DQ_S \end{bmatrix} \begin{bmatrix} \dfrac{V_{BE}-V_{BEIN}-I_{BE}\cdot R_{BB}+I_{CIN}\cdot R_{BB}-\dfrac{Q_B}{T_C}R_{BB}}{R_{BB}\cdot C_{BE}} \\ \dfrac{I_{CIN}-\dfrac{Q_B}{T_C}+\dfrac{C_{BC}}{R_{BB}(C_{BE}+C_{BC})}\left[V_{BE}-V_{BEIN}-I_{BE}\cdot R_{BB}\right]}{\dfrac{C_{BC}\cdot C_{BE}}{C_{BC}+C_{BE}}} \\ I_B-\dfrac{Q_B}{T_B} \\ I_{BX}-\dfrac{Q_S}{T_S} \end{bmatrix}$$

Fig. 3.4 gives the block diagram of subroutine MSTAP 2

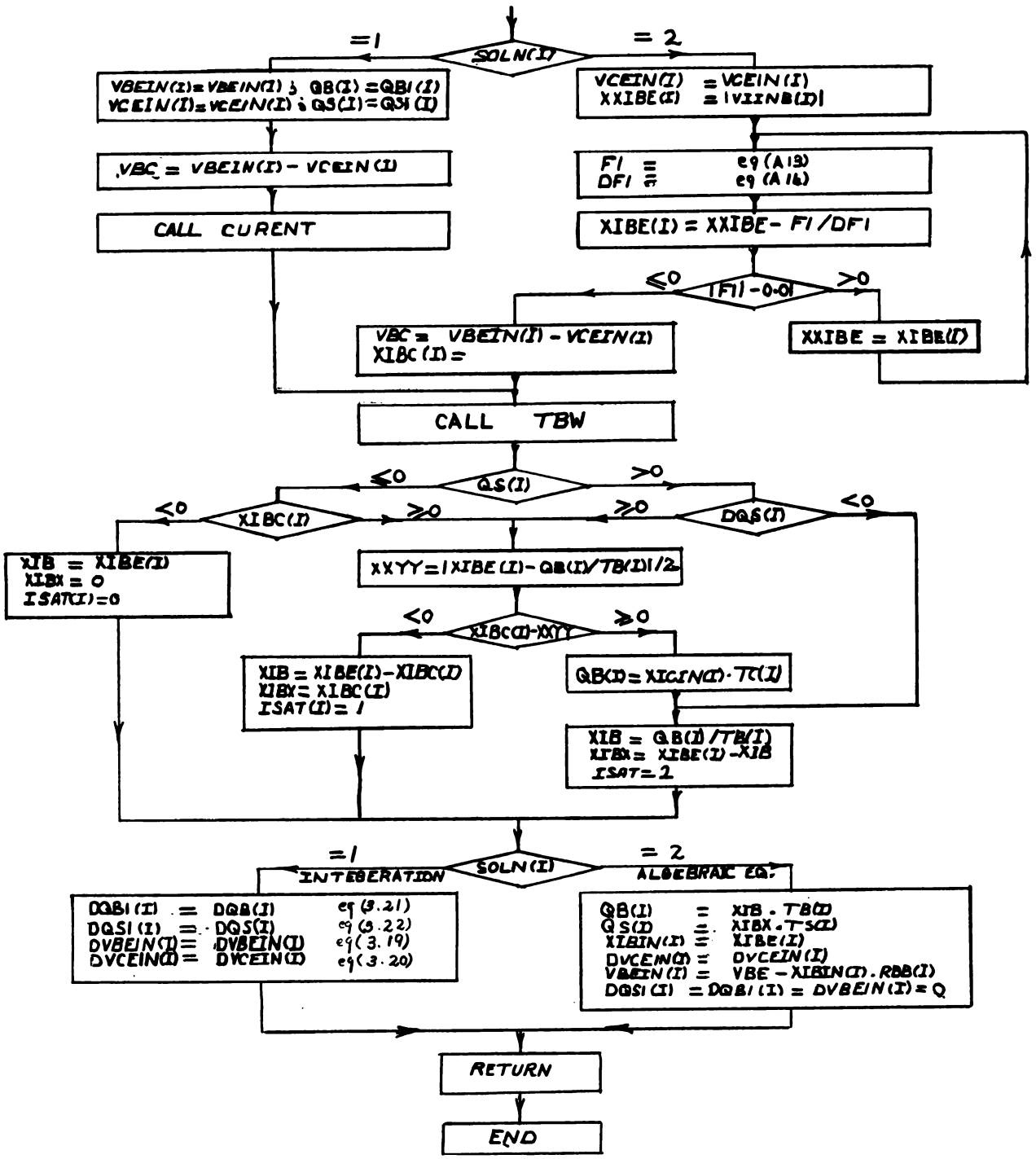

Fig. (3.4) Block Diagram of Subroutine MSTAP 2

3.5 Subroutine MSTAP 3

This subroutine expects to be given XIBIN(I) and VCE and supplies back enough information to determine VBE and XICIN(I).

Evaluation of Differential Equations

Referring to Fig. (3.2) and substituting Equation (3.4) in Equation (3.2), we get

$$VCE = VCEIN(I)+(QB(I)/TC(I)-CBC(I).DVBEIN(I)+CBC(I).DVCEIN(I)) .RCC(I) \quad (3.26)$$

Solving Equation (3.26) and Equation (3.3) for DVBEIN(I) and DVCEIN(I), we get

$$DVBEIN(I) = \frac{XIBIN(I)-XIBE(I)+\left[VCE-VCEIN(I)-\frac{QB(I).RCC(I)}{TC(I)}\right]/RCC(I)}{CBE(I)} \quad (3.27)$$

$$DVCEIN(I) = \left[VCE-VCEIN(I)-\frac{QB(I).RCC(I)}{TC(I)}+\frac{CBC(I).RCC(I)}{CBE(I)+CBC(I)}(XIBIN(I)-XIBE(I)\right] /CBC(I).CBE(I).RCC(I)/(CBE(I)+CBC(I)) \quad (3.28)$$

together with equations (3.21 and 3.22).

Derivatives Supplied to MISTAP

DQB1(I) = DQB(I)

DQS1(I) = DQS(I)

DVBE1N(I) = DVBEIN(I)

DVCE1N(I) = DVCEIN(I)

Solution is by the use of Nonlinear Algebraic Equations

Here the set of equations yielding a solution are:

$$QB(I) = XIB \;.\; TB(I)$$

$$QS(I) = XIBX \;.\; TS(I)$$

$$VBE = \frac{XMBE(I) \,.\, XK \,.\, TEMP(I)}{Q} \;.\; \ln \frac{XIBIN(I)+XIBEO(I)}{XIBEO(I)} + XIBIN(I) \,.\, RBB(I) \qquad (3.29)$$

and

$$XICIN(I) = QB(I)/TC(I)$$

The following differential equations are also supplied to the integrating subroutine

$$DQB1(I) = 0.0$$

$$DQS1(I) = 0.0$$

$$DVBE1N(I) = 0.0$$

$$DVCE1N(I) = 0.0$$

In this case the state model is:

$$\begin{bmatrix} DV_{BEIN} \\ DV_{CEIN} \\ DQ_B \\ DQ_S \end{bmatrix} \quad \begin{bmatrix} \dfrac{I_{BIN}-I_{BE}-\left[V_{CE}-V_{CEIN}-\dfrac{Q_B \cdot R_{CC}}{T_C}\right] \dfrac{1}{R_{CC}}}{C_{BE}} \\ \dfrac{V_{CE}-V_{CEIN}-\dfrac{Q_B \cdot R_{CC}}{T_C}+\dfrac{C_{BC} \cdot R_{CC}}{C_{BE}+C_{BC}}\left[I_{BIN}-I_{BE}\right]}{\dfrac{R_{CC} \cdot C_{BC} \cdot C_{BE}}{C_{BE}+C_{BC}}} \\ I_B - \dfrac{Q_B}{T_B} \\ I_{BX} - \dfrac{Q_S}{T_S} \end{bmatrix}$$

Fig. (3.5) gives the block diagram of subroutine MSTAP 3

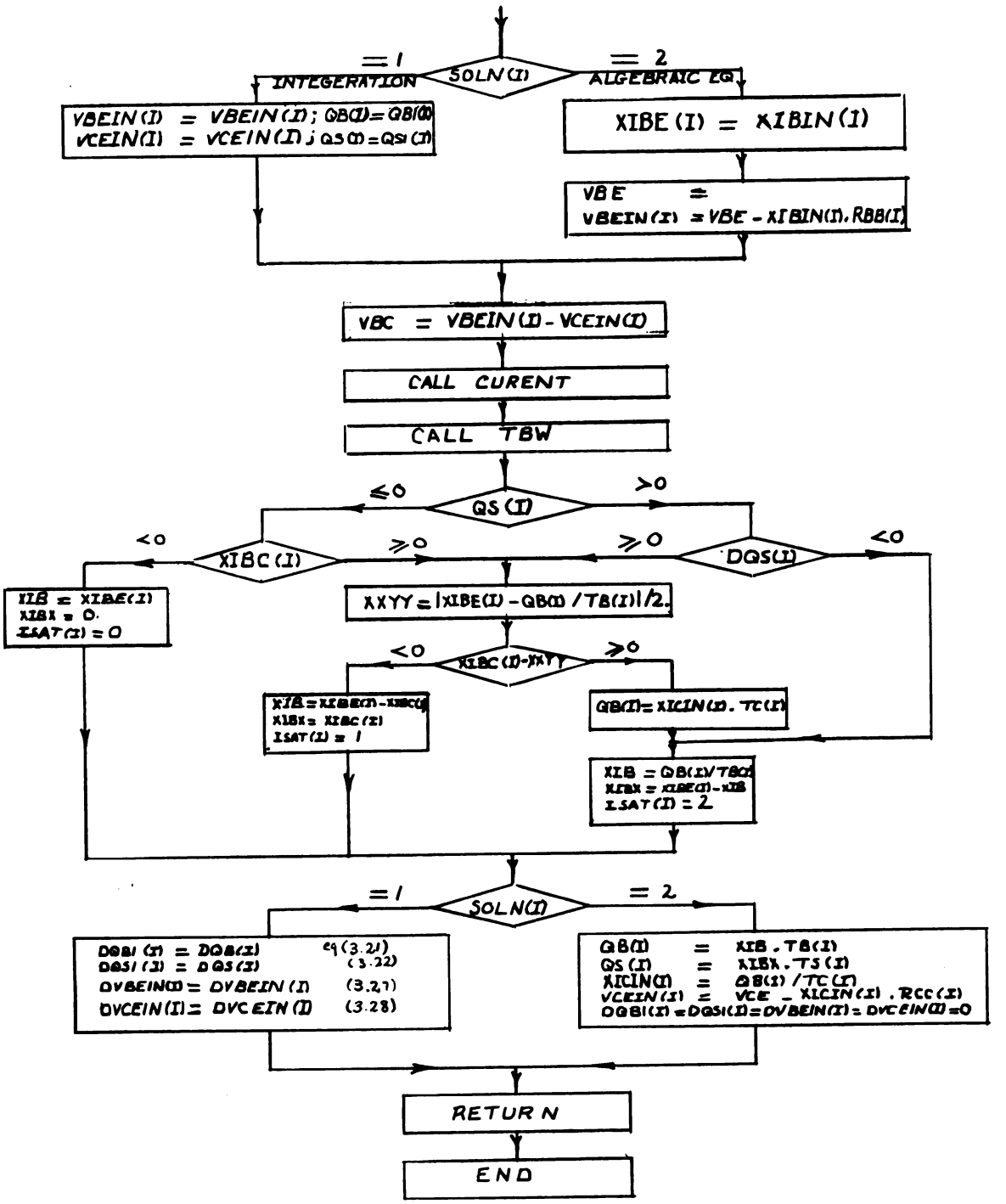

Fig. (3.5) Block Diagram of Subroutine MSTAP 3

3.6 Subroutine MSTAP 4

This subroutine expects to be supplied with XIBIN(I) and XICIN(I) and returns back enough information to determine VBE and VCE.

Evaluation of Differential Equations

Solving Equations (3.3 and 3.4) for DVBEIN(I) and DVCEIN(I), we get:

$$DVBEIN(I) = (XIBIN(I)-XIBE(I)+XICIN(I)-QB(I)/TC(I))/CBE(I) \qquad (3.30)$$

$$DVCEIN(I) = \Big[XICIN(I) - QB(I)/TC(I)+(CBC(I).(XIBIN(I)-XIBE(I))/[CBE(I)+CBC(I)]\Big] \Big/ \Big[CBC(I).CBE(I)/(CBC(I)+CBE(I))\Big] \qquad (3.31)$$

Together with Equations (3.21 and 3.22)

Derivatives Supplied to MISTAP

DQB1(I) = DQB(I)

DQS1(I) = DQS(I)

DVBE1N(I) = DVBEIN(I)

DVCE1N = DVCEIN(I)

Solution is Partially by the use of Algebraic Equations

Again, here as in MSTAP 2, VCE has to be obtained through the solution of the differential equation describing VCEIN(I). The set of equations yielding the solution are

QB(I) = XIB . TB(I)

QS(I) = XIBX . TS(I)

VBE is given by Equation (3.29)

together with the following set of differential equations:

DQB1(I) = 0.00

DQS1(I) = 0.00

DVBE1N(I) = 0.00

DVCE1N(I) = DVCEIN(I)

In this case the state model is:

$$\begin{bmatrix} DV_{BEIN} \\ DV_{CEIN} \\ DQ_B \\ DQ_S \end{bmatrix} \quad \begin{bmatrix} \dfrac{I_{BIN} - I_{BE} + I_{CIN} - \dfrac{Q_B}{T_C}}{C_{BE}} \\ \dfrac{I_{CIN} - \dfrac{Q_B}{T_C} + \dfrac{C_{BC}}{C_{BE}+C_{BC}} \left[I_{BIN} - I_{BE}\right]}{\dfrac{C_{BE} \cdot C_{BC}}{C_{BE} + C_{BC}}} \\ I_B - Q_B/T_B \\ I_{BX} - Q_S/T_S \end{bmatrix}$$

Fig. (3.6) gives the block diagram of subroutine MSTAP 4

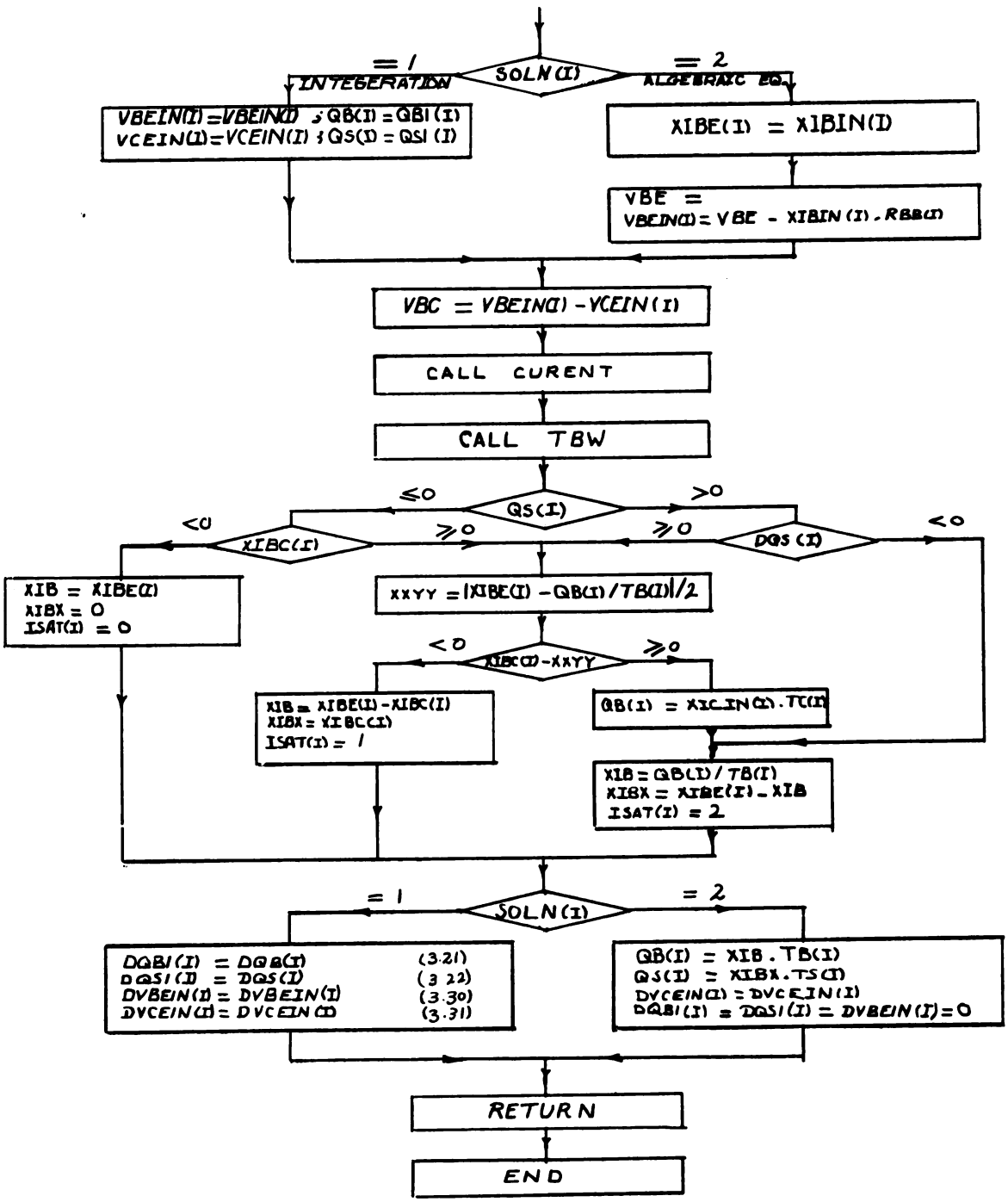

Fig. (3.6) Block Diagram of Subroutine MSTAP 4

3.7 SUBROUTINE CAP

This subroutine calculates the value of the junction capacitances of transistor I, first by finding the type of transistor I, i.e.,

L = ITYP(I)

$$CBC(I) = XKBC(L) \cdot (VO(L) - VBC)^{XBC(L)} \quad (3.32)$$

$$CBE(I) = XKBE(L) \cdot (VO(L) - VBEIN(I))^{XBE(L)} \quad (3.33)$$

3.8 SUBROUTINE CURRENT

This subroutine calculates the value of the current through the junction by first knowing the type of the transistor.

L = ITYP(I)

$$XIBE(I) = XIBEO(L) \cdot (EXP(Q \cdot VBEIN(I)/MBE(L) \cdot K \cdot TEMP(I))-1) \quad (3.34)$$

$$XIBC(L) = XIBCO(L) \cdot (EXP(Q \cdot VBC/MBC(L) \cdot K \cdot TEMP(I))-1) \quad (3.35)$$

3.9 SUBROUTINE TBW

As has been mentioned before, TC varies with the collector to emitter voltage VCE, and Beta, the common emitter current gain varies with XICIN, the collector current, and finally TS, the saturation time constant varies with the collector current saturation level. Each of the previous variations is represented by one curve as shown in Fig. (3.7, 3.8 and 3.9). These curves are stored as curves with ten points representing each. Subroutine TBW performs the necessary interpolation to find TC(I), TS(I) and TB(I). Fig. (3.10) shows the block diagram of subroutine TBW.

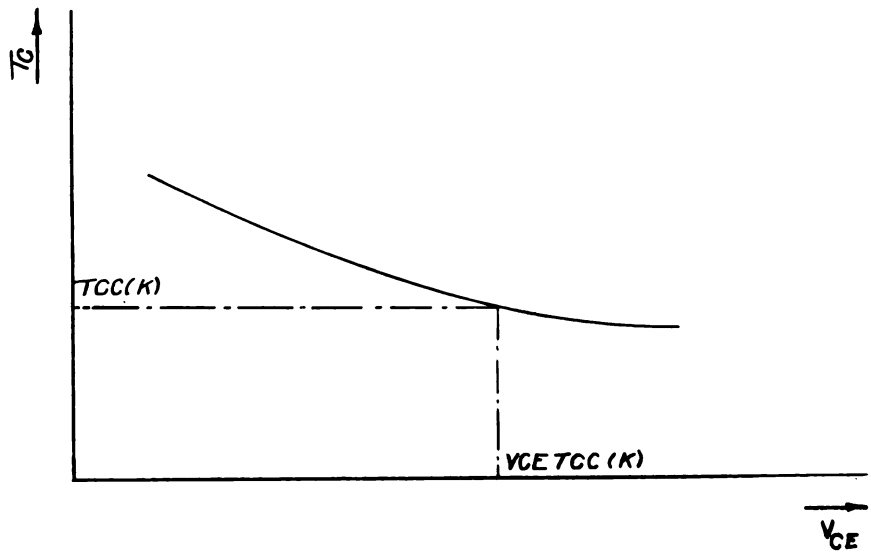

Fig. (3.7) Variation of T_C with V_{CE}

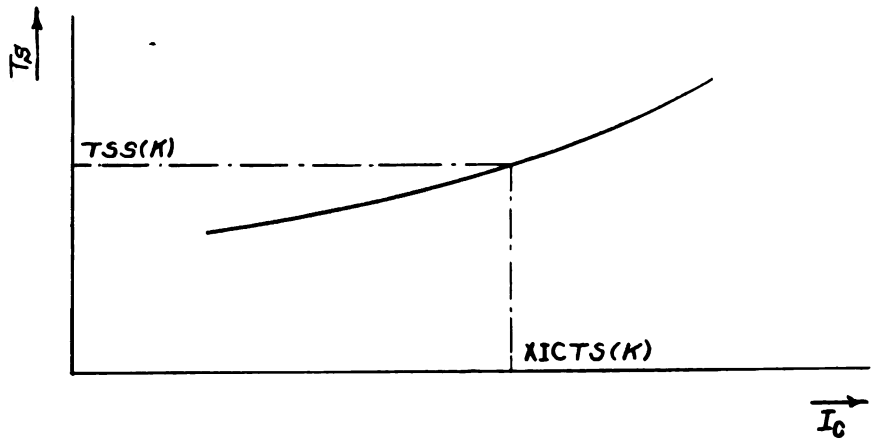

Fig. (3.8) Variation of T_S with Collector Current

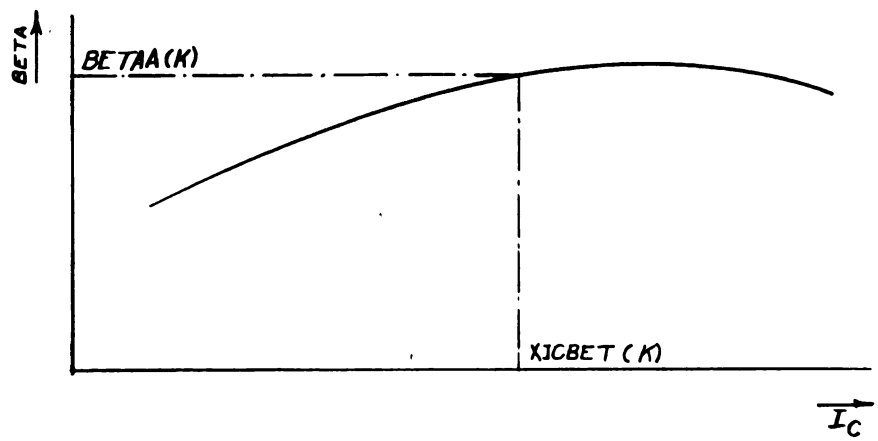

Fig. (3.9) Variation of Beta with the Collector Current

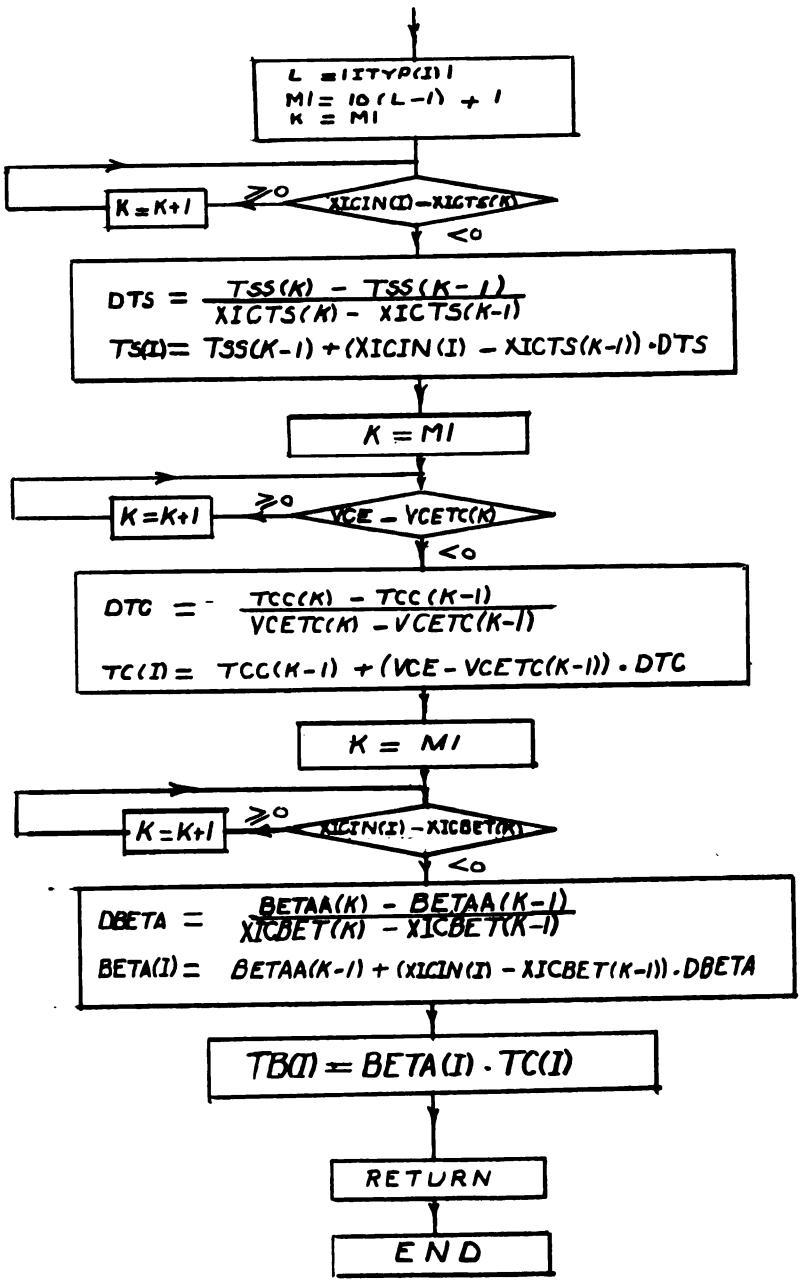

Fig. (3.10) Block Diagram of Subroutine TBW

CHAPTER IV

EXPERIMENTAL CORRELATIONS

In this part, discussion is limited to relating the suggested model to the actual device by comparing the predicted results obtained by the aid of this model and the digital computer, to those measured in the laboratory.

There are five capacitances in the combined test circuit and equivalent circuit of the transistor, Fig. (4.1). These are]

a - Base emitter junction capacitance, CBE

b - Base collector junction capacitance, CBC

c - Base emitter stray capacitance, (capacitance between base emitter leads and base emitter socket terminals), CBEX.

d - Collector emitter stray capacitance, (capacitance between collector emitter leads and corresponding socket terminals), CBCX.

e - Collector emitter stray capacitance, (capacitance between collector emitter leads and corresponding socket terminals), CBEX.

The mathematical prediction starts with the base emitter junction and stray capacitances, CBE and CBEX, being the only ones existing. The other three are included individually afterwards and the effect of each is then discussed.

The necessary differential and algebraic equations are first developed. The solution of the differential equations is by the Runga-Kutta method of numerical integration. The symbols used are in the same form of those used in the FORTRAN program so as to make it easy for anyone who wants to go through the steps in detail.

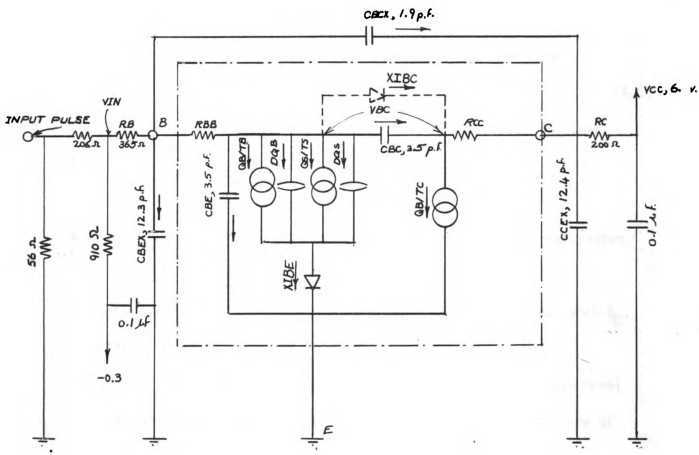

Fig. (4.1) Complete Test Circuit and Transistor Equivalent Circuit (inside dashed lines)

The following tests are performed with the test circuit shown in Fig. (4.1). The transistor used is a Texas Instrument, 2N744 Epitaxial Diffused High Speed Mesa Selicon Transistor. The charge measurements were performed by the device characterization group of International Business Machines Corporation, according to the method suggested by Cornell Hegedus[9]. The characteristics of the transistor are as follows:

1 - Base emitter diode junction characteristic, as given by Equation (2.17) and Fig. (2.7).

2 - Base collector diode junction characteristic is given by:

$$I_{BC} = 0.22 \times 10^{-10} . (e^{29 V_{BC}} - 1) \qquad (4.1)$$

where, V_{BC} is the voltage across the base collector junction.

3 - Variation of T_C, the collector time constant, with V_{CE}, the collector emitter voltage, is shown in Fig. (4.2).

4 - The variation of T_S with the collector current during saturation is shown in Fig. (4.3).

5 - The variation of beta, the common emitter current gain with I_C, the collector current is shown in Fig. (4.4).

The values of T_C and T_S for the particular voltage level or current level are obtained by interpolation through the use of Fig. (4.2) and Fig. (4.3) respectively.

The value of beta is obtained by interpolation through the use of Fig. (5.4). T_B is hence obtained from:

$$T_B = \beta . T_C \qquad (4.2)$$

6 - R_{CC} = 5 ohms, R_{BB} = 8 ohms, $C_{BC} = C_{BE}$ = 3.5 p.f.

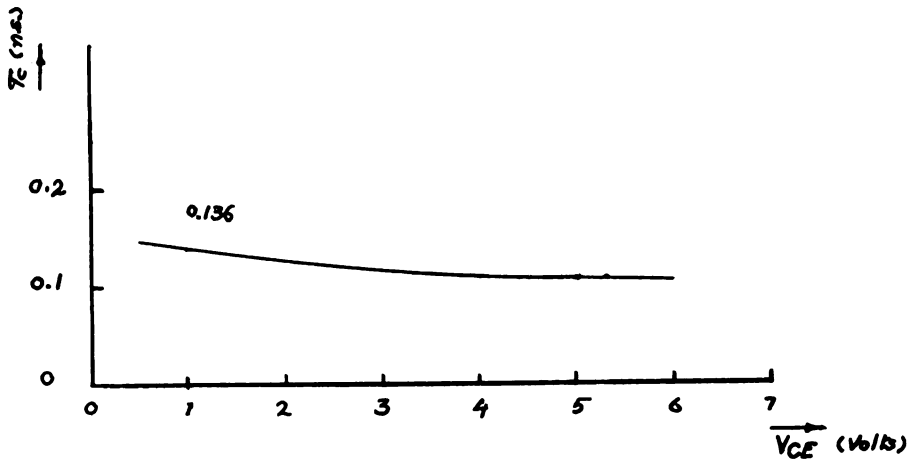

Fig. (4.2) Variation of T_C with V_{CE}, for 2N744

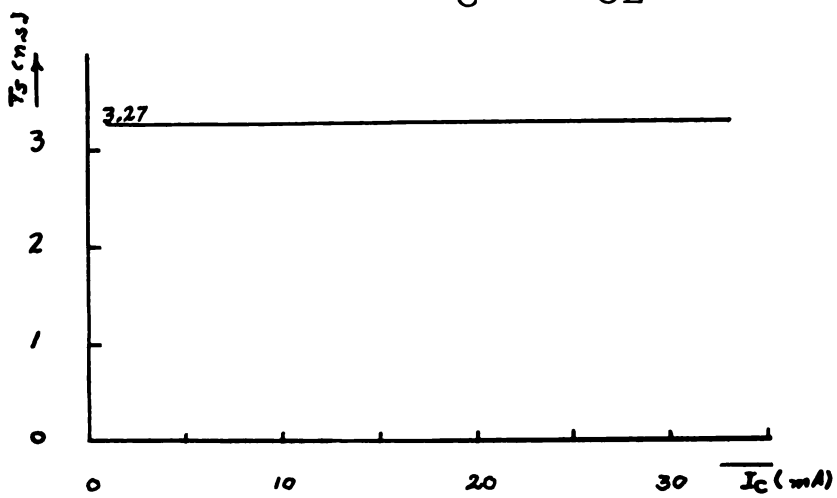

Fig. (4.3) Variation of T_S with I_C, for 2N744

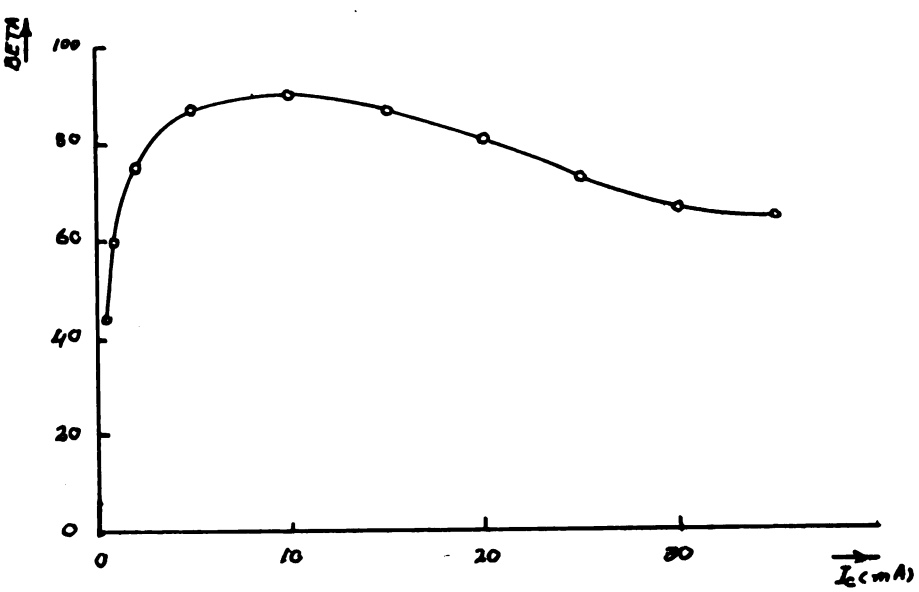

Fig. (4.4) Variation of Beta with I_C, for 2N744

4.1 Base Emitter Junction and Stray Capacitances are the only Capacitances

Fig. (4.5) shows the essential equivalent and test circuits with the elements under the dashed box representing the elements of the transistor equivalent circuit under consideration. In the development that follows, the letter D before any quantity will have the following meaning:

$$DXY = d(XY)/dt$$

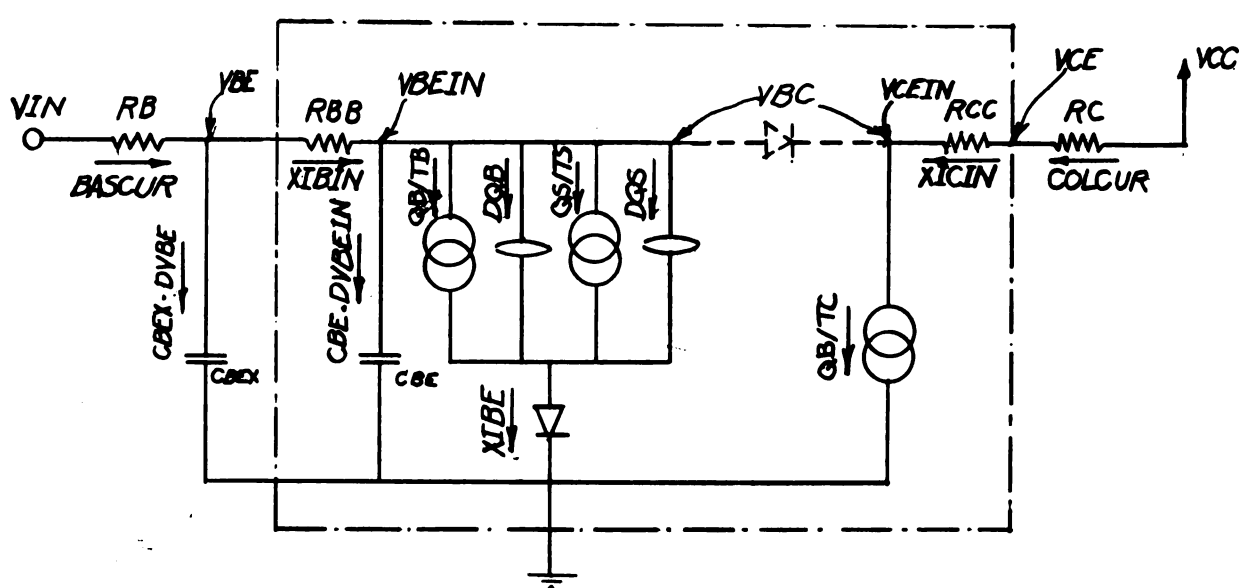

Fig. (4.5) Essential Test and Equivalent Circuit with Base Emitter Capacitances Being the Only Ones Included.

Evaluation of Differential Equations

From Fig. (4.5)

$$COLCUR = XICIN \tag{4.3}$$

$$BASCUR = XIBIN + CBEX \cdot DVBE \tag{4.4}$$

$$XIBIN = XIBE + CBE \cdot DVBEIN \tag{4.5}$$

$$VIN = VBE + BASCUR \cdot RB$$

$$= VBE + (XIBIN + CBEX \cdot DVBE) \cdot RB$$

$$\therefore DVBE = (VIN - VBE - XIBIN \cdot RB)/RB \cdot CBEX \tag{4.6}$$

$$VBE = VBEIN + XIBIN \cdot RBB \tag{4.7}$$

$$= VBEIN + (XIBE + CBE \cdot DVBEIN) \cdot RB$$

i.e.

$$DVBEIN = (VBE - VBEIN - XIBE \cdot RBB)/RBB \cdot CBE \tag{4.8}$$

$$DQB = XIB - QB/TB \tag{4.9}$$

$$DQS = XIBX - QS/TS \tag{4.10}$$

where

XIB = component of XIBE, current through base emitter junction, contributing to the build up of the base charge QB.

XIBX = component of XIBE contributing to the build up of the storage charge QS.

$$XICIN = QB/TC \tag{4.11}$$

$$VCE = VCC - COLCUR \cdot RC \tag{4.12}$$

$$VCEIN = VCE - XICIN \cdot RCC \tag{4.13}$$

$$XIBE = XIBEO \cdot [EXP(Q \cdot VBEIN/MBE \cdot XK \cdot TEMP) - 1] \tag{4.14}$$

Two different tests have been taken, one with a larger base drive than the other. Table I gives a summary of these results while Figs. (4.6 and 4.7) show a comparison between the collector emitter voltage obtained mathematically and experimentally, for these two cases. The following results require the introduction of some definitions which are introduced below:

Turn on Delay

This is the time that elapses between the time the input signal is applied and the time the output signal reaches 10% of its final steady state value.

Rise Time

This is the time that it takes the output signal to rise from 10% to 90% of its final steady state maximum value.

Fall Time

This is the time required by the output signal to drop from 90% to 10% of its maximum steady state value.

Saturation Time, or Storage Time

This is the time that elapses between the instant the input signal drops to 90% of its final steady state maximum value and the instant that the output signal drops to 90% of its own maximum steady state value.

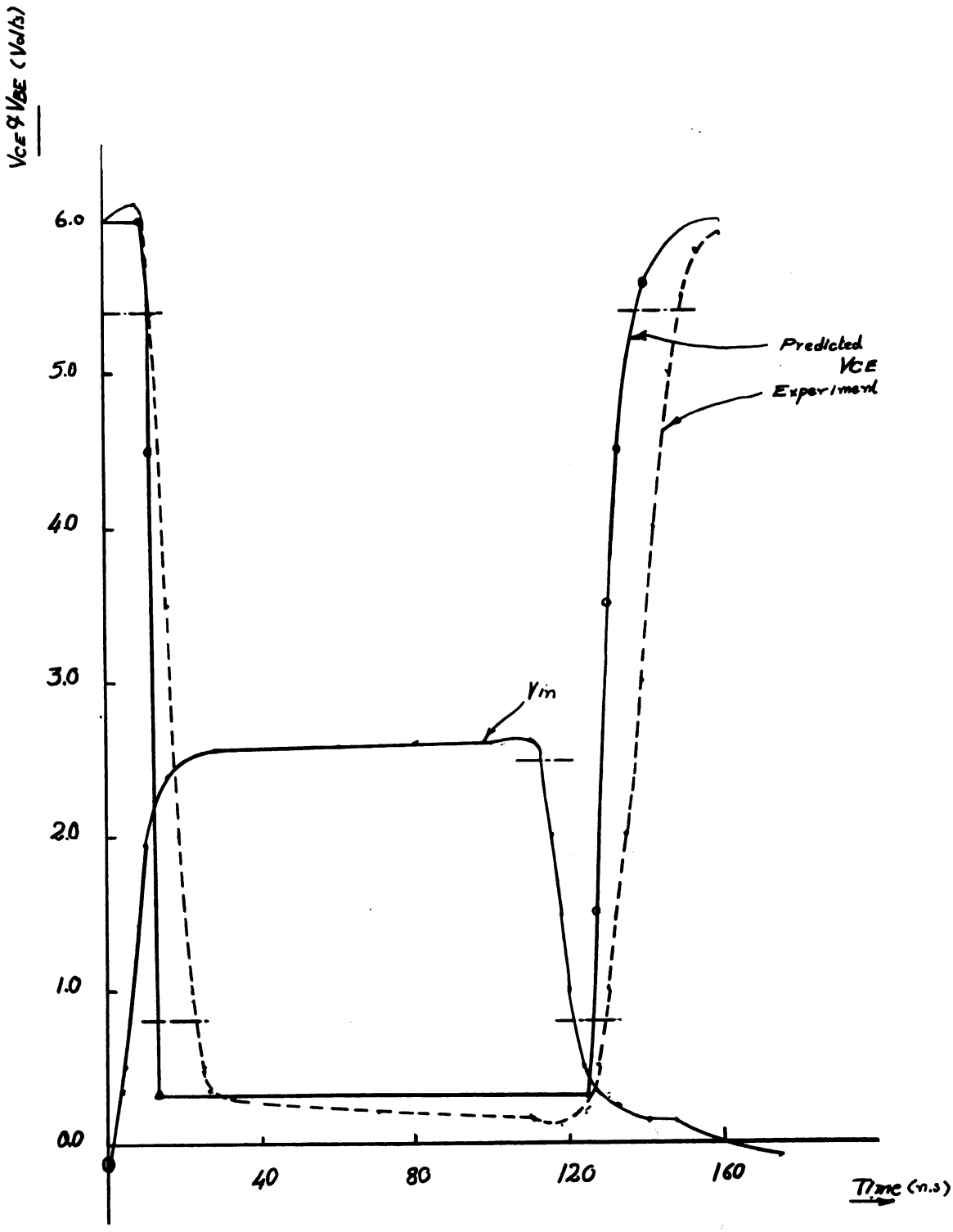

Fig. (4.6) Base Emitter Junction and Stray Capacitances
(Heavy Saturation)

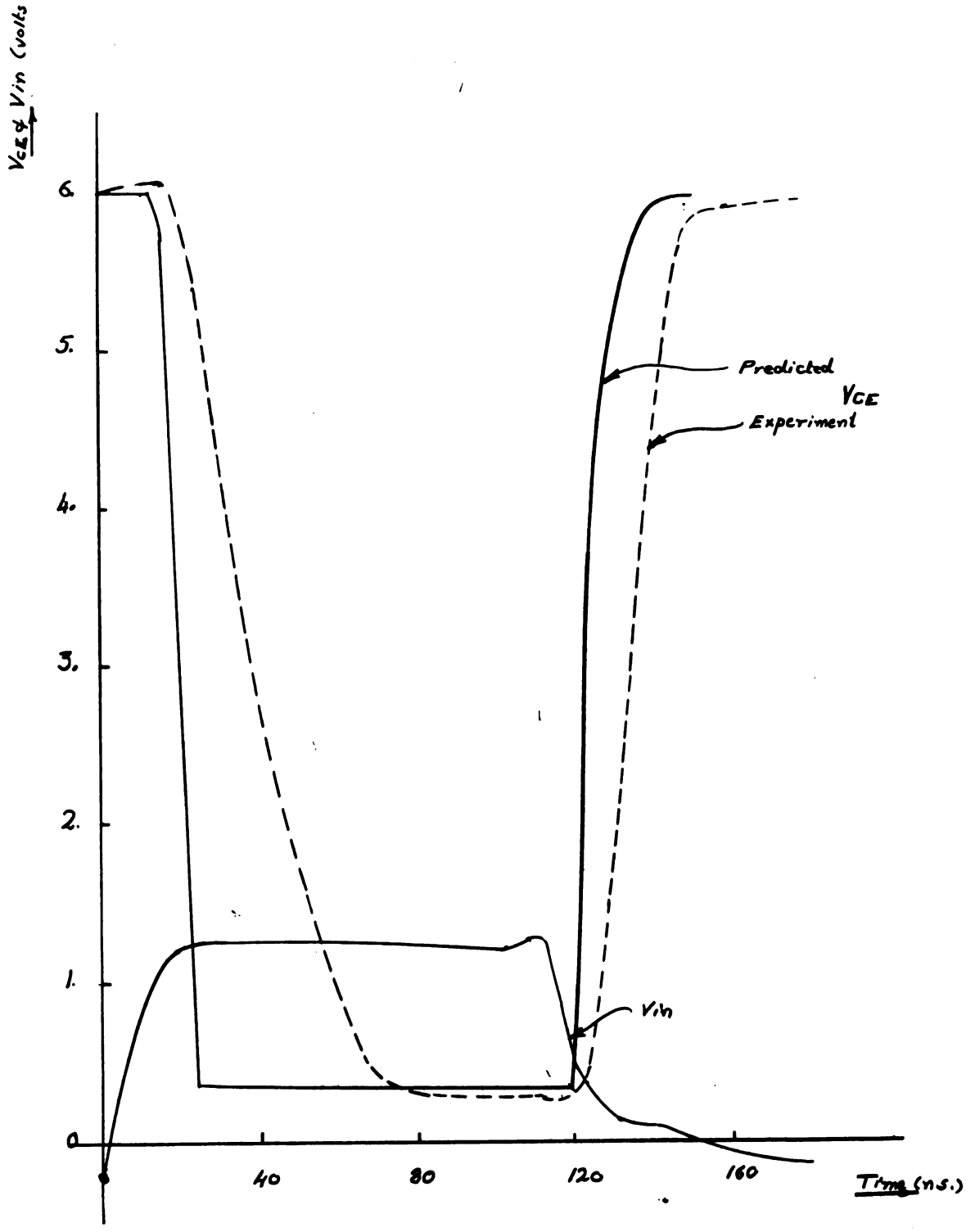

Fig. (4.7) Base Emitter Junction and Stray Capacitance

(Light Saturation)

TABLE I

Comparison Between Predicted and Experimental Results When Base Emitter Capacitances are the Only Ones Included

	Heavy Drive	Light Drive
Turn on delay, n. s.		
predicted t_{dp}	10	16
experiment t_{de}	12	23
difference	-2	-7
% error	-16. 7%	-30. 3%
Rise Time, n. s.		
predicted t_{rp}	2. 5	5
experiment t_{re}	11	36
difference	-8. 5	-30
% error	-77%	-83. 5%
Fall Time, n. s.		
predicted, t_{fp}	12	12
experiment, t_{fe}	21	22
difference	-9	-10
% error	-43%	-45. 5%
Saturation Time, n. s.		
predicted, t_{sp}	12	5
experiment, t_{se}	16	11
difference	-4	-6
% error	-25%	-54. 5%

To sum up the results given in Table I, although the percentage differences are rather large, the two curves (experimental and predicted) have the same form.

The addition of the collector emitter capacitance should increase the delay and reduce the errors. The predicted base current will be mentioned and discussed later.

4.2 Base Emitter Junction Capacitance, Base Emitter Stray Capacitance and Collector Emitter Stray Capacitance are the Ones being Considered

Fig. (4.8) shows the test circuit and the transistor equivalent circuit with the capacitances mentioned above are the only one included.

Evaluation of Differential Equations

Referring to Fig. (4.8), with symbols adjacent to nodes being names of voltages and symbols next to arrows being names of currents

$$\text{BASCUR} = \text{XIBIN} + \text{CBEX} \cdot \text{DVBE} \tag{4.15}$$

$$\text{COLCUR} = \text{XICIN} + \text{CCEX} \cdot \text{DVCE} \tag{4.16}$$

$$\text{XIBIN} = \text{XIBE} + \text{CBE} \cdot \text{DVBEIN} \tag{4.17}$$

$$\text{XICIN} = \text{QB}/\text{TC} \tag{4.18}$$

$$\text{VIN} = \text{VBE} + \text{BASCUR} \cdot \text{RB}$$

$$= \text{VBE} + (\text{XIBIN} + \text{CBEX} \cdot \text{DVBE}) \cdot \text{RB}$$

Thus,

$$\underline{DVBE = (VIN - VBE - XIBIN \cdot RB)/RB \cdot CBEX} \qquad (4.19)$$

$$VCC = VCE + COLCUR \cdot RC$$

$$= VCE \cdot (XICIN + CCEX \cdot DVCE) \cdot RC$$

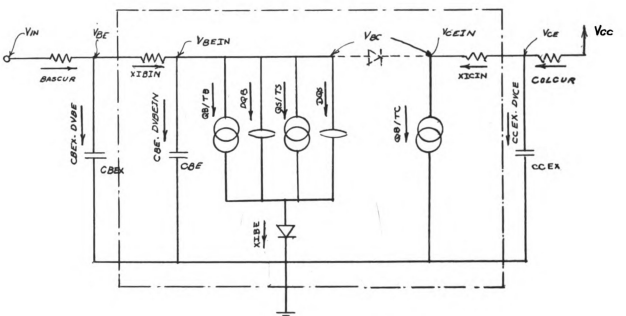

Fig. (4.8) Essential elements of the test circuit and transistor equivalent circuit. Collector emitter stray capacitance and the two base emitter capacitances are the only ones.

or,

$$\underline{DVBEIN = (VBE - VBEIN - XIBE \cdot RBB)/RBB \cdot CBE} \qquad (4.20)$$

$$\underline{DQB = XIB - QB/TB} \qquad (4.21)$$

$$\underline{DQS = XIBX - QS/TS} \qquad (4.22)$$

XIB and XIBX are as defined in part 5.1

$$XICIN = QB/TC \tag{4.23}$$

$$VCEIN = VCE - XICIN \cdot RCC \tag{4.24}$$

and $$XIBE = XIBEO \cdot (EXP(Q \cdot VBEIN/MBE.XK.TEMP) - 1) \tag{4.25}$$

With the same set of input signals used in part 5.1 the predicted outputs as compared to the experimental ones are shown in Figs. (5.9 and 5.10). Table II summarizes these results.

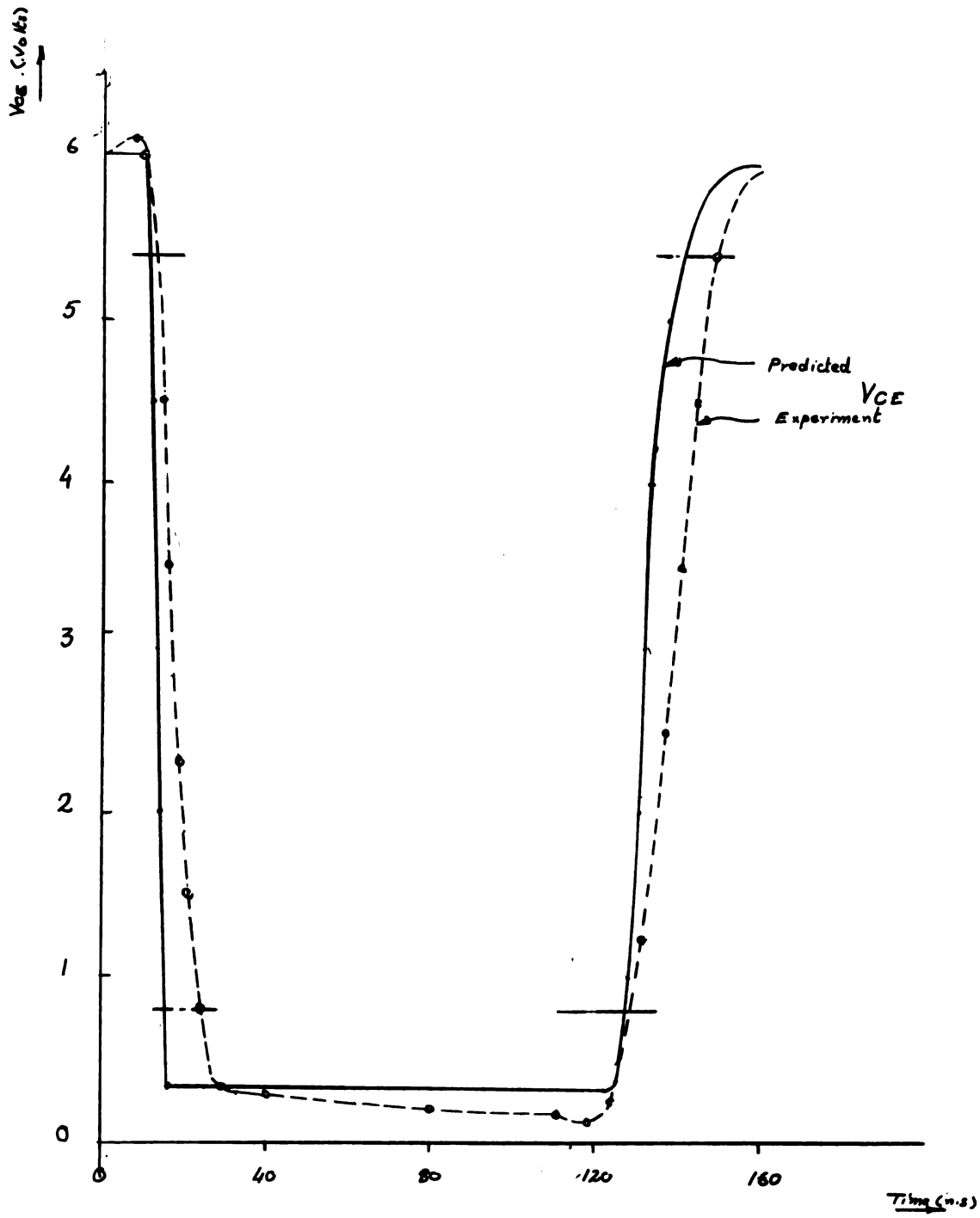

Fig. (4.9) Base Emitter Junction and Stray Capacitances and Collector Emitter Stray Capacitance are the ones considered under Heavy Drive Conditions

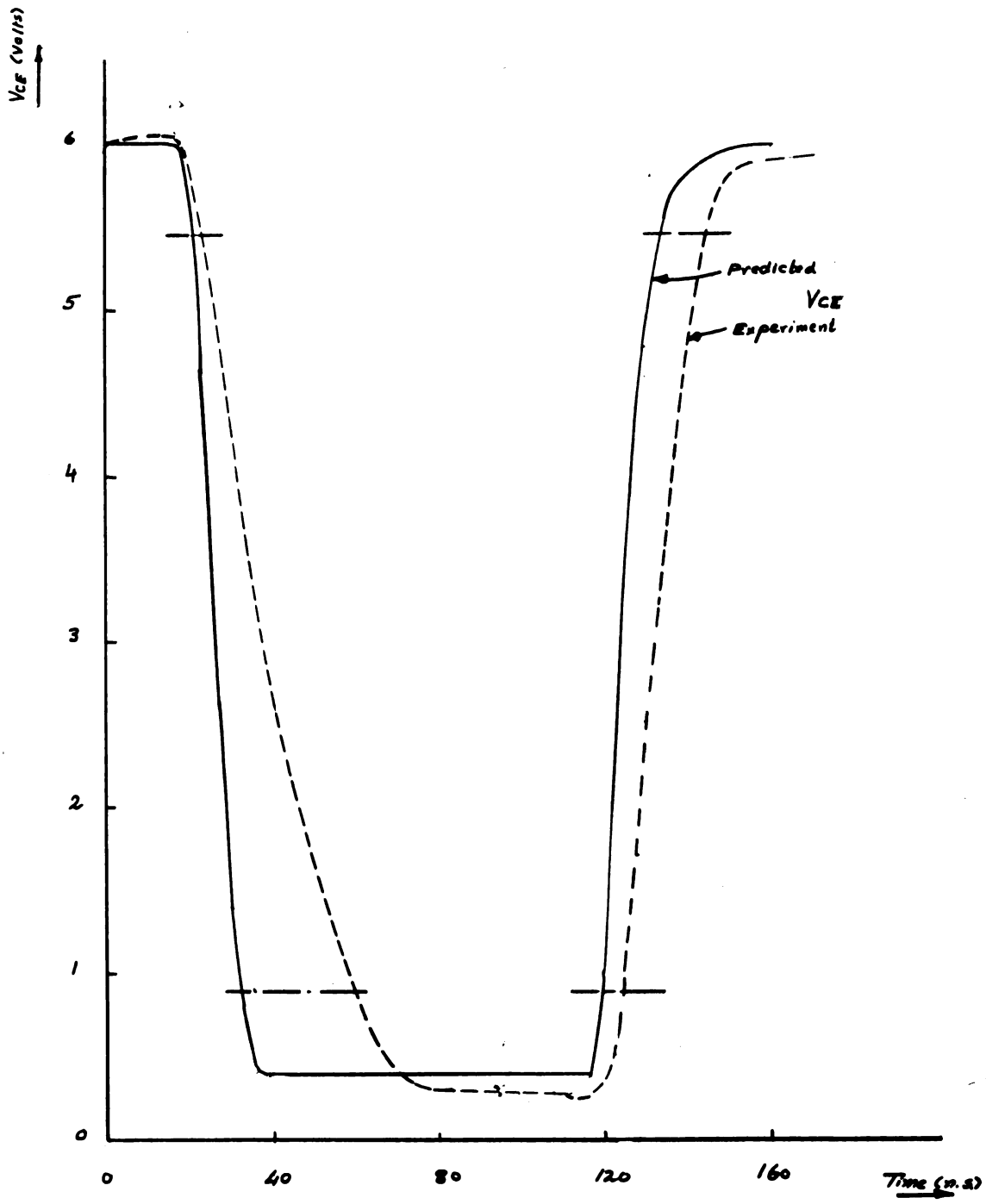

Fig. (4.10) Base Emitter Junction and Stray Capacitances and Collector Emitter Capacitance are the ones included under Light Drive Conditions

TABLE II

Comparison Between Predicted and Experimental Results for the Case When Base Emitter Junction and Stray Capacitance, in Addition to the Collector Capacitance are the only one Included

	Heavy Drive	Light Drive
Turn on Delay, n.s.		
Predicted, t_{dp}	12	20
Experiment, t_{de}	12	23
Difference	0	-3
% error	0	-13%
Rise Time, n.s.		
Predicted, t_{rp}	2.6	11.5
Experiment, t_{re}	11	36
Difference	-8.4	-24.5
% error	-76%	-66%
Fall Time, n.s.		
Predicted, t_{fp}	14	15
Experiment, t_{fe}	21	22
Difference	-7	-7
% error	-33.3%	-31.8%
Saturation Time, n.s.		
Predicted, t_{sp}	12.5	5.5
Experiment, t_{se}	16	11
Difference	-3.5	-5.5
% error	-21.8%	-50%

Thus, we see that the collector emitter stray capacitance, as expected introduced more delay in the output signal. As can be seen from Table II, the differences between the experimental and predicted results have decreased.

4.3 Base Emitter Junction Capacitance, Base Emitter Stray Capacitance Stray Capacitance, Collector Emitter Stray Capacitance and Base Collector Junction Capacitance.

Fig. (4.11) shows the transistor equivalent circuit and the components of the test circuit with the capacitances named above being the ones considered.

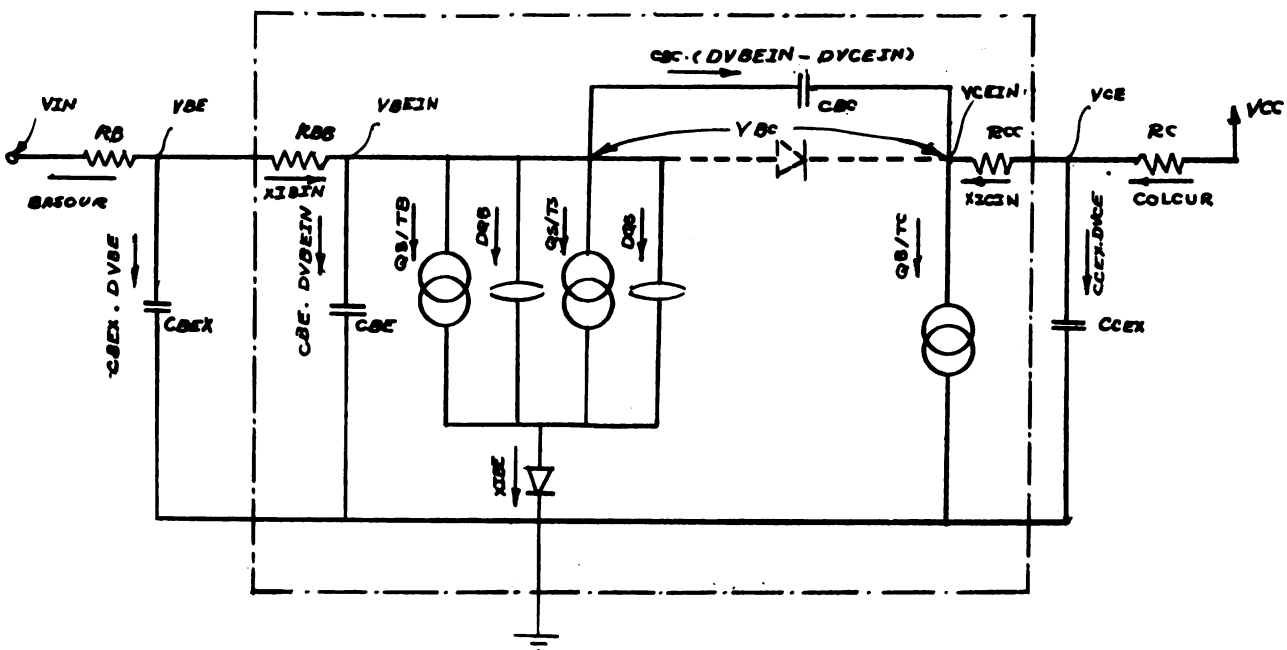

Fig. (4.11) Equivalent Circuit of Transistor and Test Circuit with Base Collector Stray Capacitance being the only one Missing.

Evaluation of Necessary Differential Equations

$$COLCUR = XICIN + CCEX \cdot DVCE \tag{4.26}$$

$$BASCUR = XIBIN + CBEX \cdot DVBE \tag{4.27}$$

$$XICIN = QB/TC - CBC \cdot (DVBEIN - DVCEIN) \tag{4.28}$$

$$XIBIN = XIBE + CBE \cdot DVBEIN + CBC \cdot (DVBEIN-DVCEIN)$$

$$= XIBE + (CBE + CBC) \cdot DVBEIN-CBC \cdot DVCEIN \tag{4.29}$$

$$VIN = VBE + BASCUR \cdot RB$$

$$= VBE + (XIBIN + CBEX \cdot DVBE) \cdot RB$$

or $$\underline{DVBE = (VIN - VBE - XIBIN \cdot RB)/RB \cdot CBEX} \tag{4.30}$$

$$VCC = VCE + COLCUR \cdot RC$$

$$= VCE + (XICIN + CCEX \cdot DVCE) \cdot RC$$

or, $$\underline{DVCE = (VCC - VCE - XICIN \cdot RC)/RC \cdot CCEX} \tag{4.31}$$

$$VBE = VBEIN + XIBIN \cdot RBB$$

$$= VBEIN + (XIBE + (CBE + CBC) \cdot DVBEIN-CBC \cdot DVCEIN) \cdot RCC$$

$$= VBEIN+XIBE \cdot RBB + (CBE + CBC) \cdot RBB \cdot DVBEIN-RBB \cdot CBC \cdot DVCEIN \tag{4.32}$$

$$VCE = VCEIN + XICIN \cdot RCC$$

$$= VCEIN + (QB/TC-CBC \cdot DVBEIN+CBC \cdot DVCEIN) \cdot RCC$$

$$= VCEIN + (QB/TC) \cdot RCC-RCC \cdot CBC \cdot DVBEIN+RCC \cdot CBC \cdot DVCEIN \tag{4.33}$$

From Equation (4.33)

$$DVCEIN = (VCE-VCEIN-(QB/TC) \cdot RCC+RCC \cdot CBC \cdot DVBEIN)/RCC \cdot CBC \tag{4.34}$$

Substituting (4.34) in (4.32) and simplifying, we get:

$$DVBEIN = \frac{(VBE-VBEIN-XIBE.RBB+(RBB/RCC).(VCC-VCEIN-(QB/TC).RCC)}{RBB.CBE} \quad (4.35)$$

From Equation (4.32), we get:

$$DVBEIN = (VBE-VBEIN-XIBE.RBB+RBB.CBC.DVCEIN)/RBB.(CBE+CBC) \quad (4.36)$$

Substituting (4.36) in (4.33) and simplifying, we get:

$$DVCEIN = (VCE-VCEIN-(QB/TC).RCC-(RCC.CBC/RBB(CBE+CBC)).(VBE-VBEIN-XIBE.RBB))/RCC.CBC.CBE/(CBE+CBC) \quad (4.37)$$

$$DQB = XIB - QB/TB \quad (4.38)$$

$$DQS = XIBX - QS/TS \quad (4.39)$$

and

$$XIBE = XIBEO.(EXP(Q.VBEIN/MBE.XK.TEMP)-1) \quad (4.40)$$

where XIB and XIBX are as defined previously.

Comparing Equation (4.30) to Equation (4.17), we notice that they are the same. However, when comparing Equation (4.35) to Equation (4.20) we notice that DVBEIN is increased by:

$$(VCC - VCEIN - (QB/TC) . RCC)/RCC . CBE$$

This quantity is negative during turn on and positive during turn off, i.e., DVBEIN is reduced during turn on and is increased during turn off. This means more delay for VBEIN, referring to Equation (4.40), this means more delay to XIBE, the current that builds up the charge QB in the base.

Equation (4.37) now replaces Equation (4.24) which implies that VCEIN does not change instantaneously any longer, but is delayed.

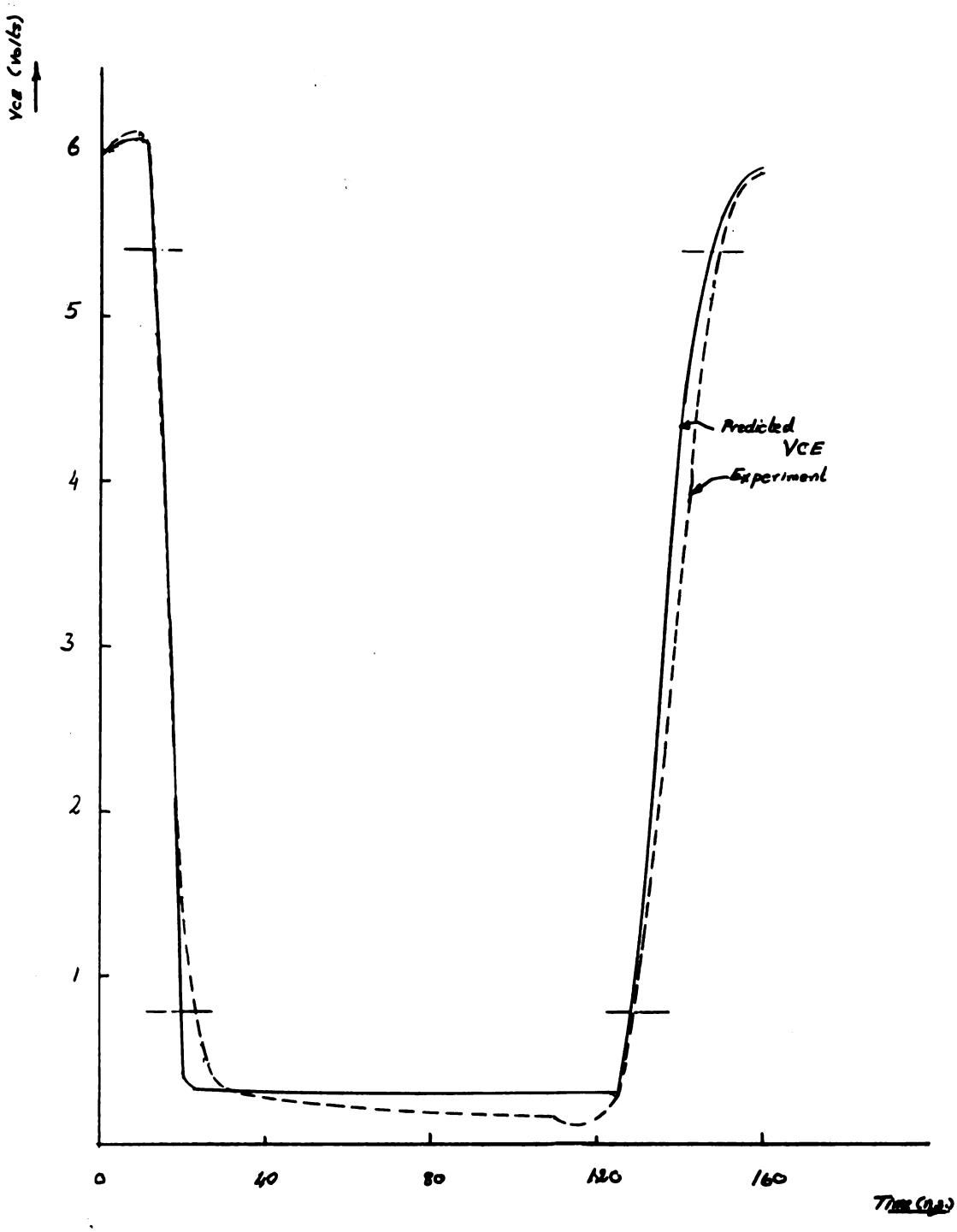

Fig. (4.12) Base Emitter, Collector Emitter and Base Collector Junction Capacitances with Heavy Base Drive

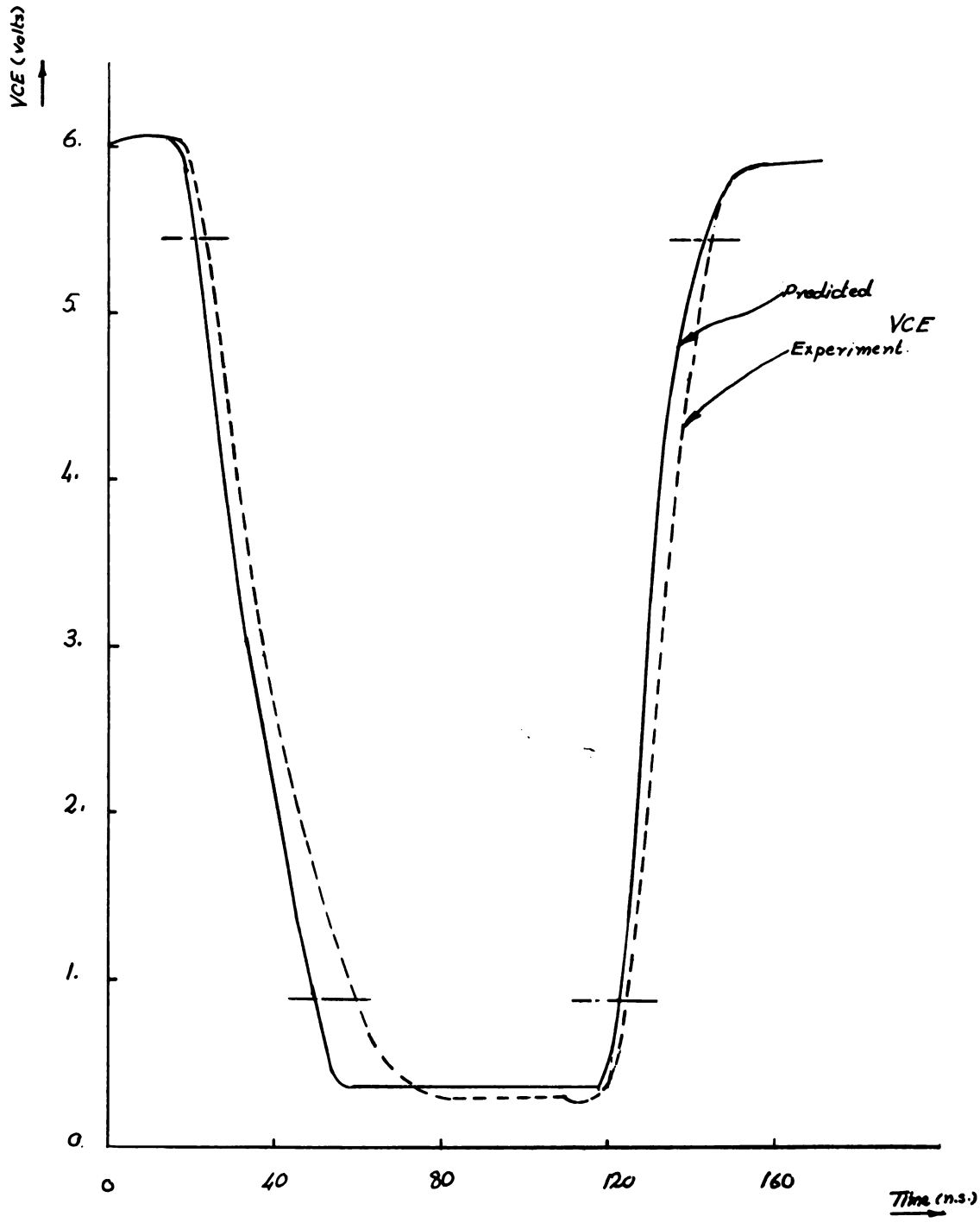

Fig. (4.13) Base Emitter, Collector Emitter and Base Collector Junction Capacitances with Light Base Drive

From Table III, it is seen that the consideration of the Base Collector Junction Capacitance brought the errors close to 10% margin. The delays were increased as was expected from the differential equations.

TABLE III

Comparison between Predicted and Experimental Results when Base Collector Stray Capacitance is the only one Omitted.

	Heavy Drive	Light Drive
Turn on Delay, n.s.		
Predicted, t_{dp}	12.5	20.5
Experiment, t_{de}	12	23
Difference	+0.5	-2.5
% error	4.15%	-10.9%
Rise Time, n.s.		
Predicted, t_{rp}	8	29
Experiment, t_{re}	11	36
Difference	-3	-7
% error	-27.3%	-19.5%
Fall Time, n.s.		
Predicted, t_{fp}	18.5	20
Experiment t_{fe}	21	22
Difference	-2.5	-2
% error	-11.5	-9.1%
Saturation Time, n.s.		
Predicted, t_{sp}	14.5	6.5
Experiment, t_{se}	15.5	10
Difference	-1	-3.5
% error	-6.65%	-35%

4.4 All Capacitances are Included

Fig. (4.14) shows the total equivalent circuit with all the capacitances (junction and stray) being included.

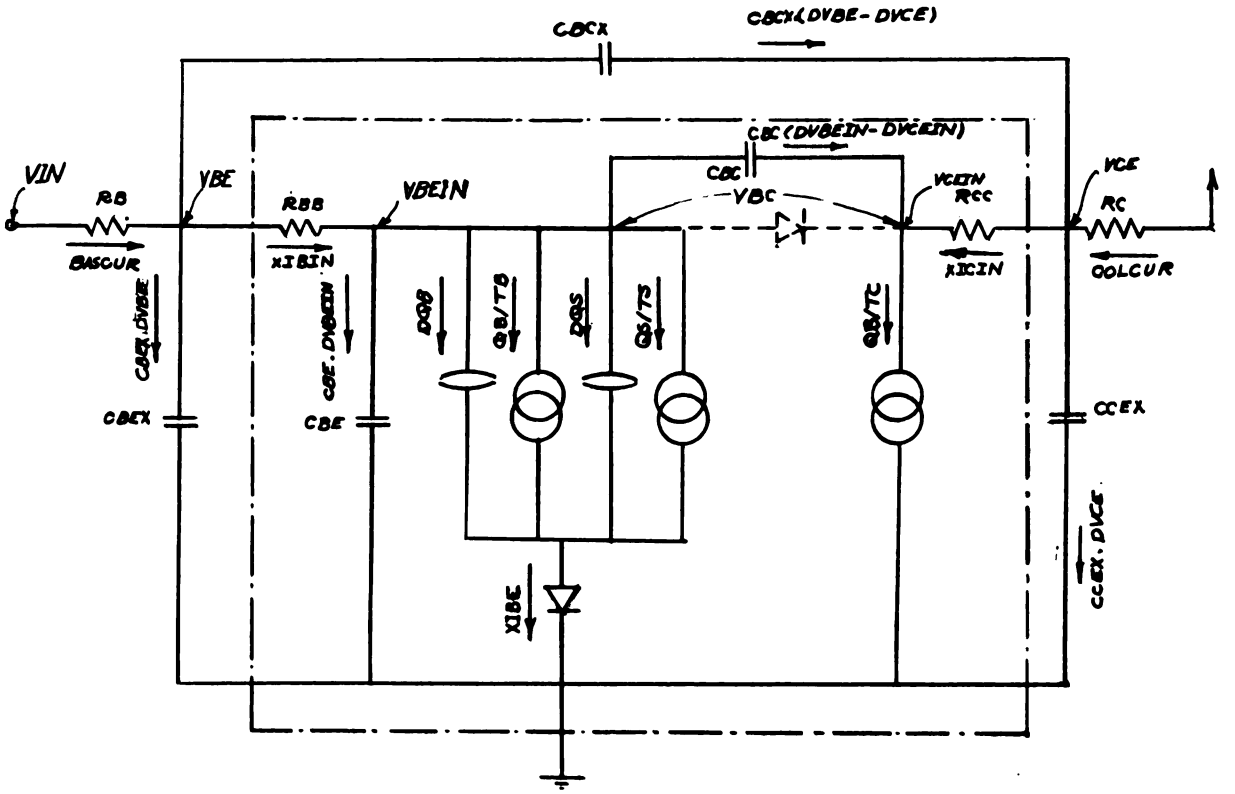

Fig. (4.14) Essential Elements of Test Circuit and Transistor Equivalent Circuit Including all Capacitances

Evaluation of Necessary Differential Equations

Referring to Fig. (4.14), we can write:

$$\begin{aligned} COLCUR &= XICIN + CCEX \cdot DVCE - CBCX \cdot (DVBE - DVCE) \\ &= XICIN + (CCEX + CBCX) \cdot DVCE - CBCX \cdot DVBE \end{aligned} \qquad (4.41)$$

$$BASCUR = XIBIN + CBEX \cdot DVBE + CBCX \cdot (DVBE - DVCE)$$

$$= XIBIN + (CBEX + CBCX) \cdot DVBE - CBCX \cdot DVCE \quad (4.42)$$

$$XICIN = QB/TC - CBC \cdot (DVBEIN - DVCEIN) \quad (4.43)$$

$$XIBIN = XIBE + CBE \cdot DVBEIN + CBC \cdot (DVBEIN - DVCEIN)$$

$$= XIBE + (CBE + CBC) \cdot DVBEIN - CBC \cdot DVCEIN \quad (4.44)$$

$$VIN = VBE + (XIBIN+(CBEX+CBCX).DVBE-CBCX.DVCE).RB$$

$$= VBE+XIBIN.RB+(CBEX+CBCX).RB.DVBE-RB.CBCX.DVCE \quad (4.45)$$

$$VCC = VCE + COLCUR \cdot RC$$

$$= VCE + (XICIN+(CCEX+CBCX).DVCE-CBCX.DVBE).RC$$

$$= VCE+XICIN.RC+(CCEX+CBCX).RC.DVCE-CBCX.RC.DVBE \quad (4.46)$$

From Equation (4.46)

$$DVCE = (VCC-VCE-XICIN.RC+CBCX.RC.DVBE)/RC(CCEX+CBCX) \quad (4.47)$$

Substituting Equation (4.47) in Equation (4.45) and simplifying, we get:

$$DVCE = \left[VIN-VBE-XIBIN.RB+\frac{RB.CBCX.(VCC-VCE-XICIN.RC)}{RC.(CBCX+CCEX)}\right] \Big/ \left[RB.(CBEX + \frac{CBCX.CCEX)}{CBCX+CCEX}\right] \quad (4.48)$$

From Equation (4.45), we get

$$DVBE = (VIN-VBE-XIBIN.RB+RB.CBCX.DVCE)/RB.(CBEX+CBCX) \quad (4.49)$$

Substituting Equation (4.49) in Equation (4.46) and simplifying, we get:

$$DVCE = \frac{VCC-VCE-XICIN.RC + \dfrac{RC.CBCX.(VIN-VBE-XIBIN.RB)}{RB.(CBEX+CBCX)}}{RC.\left[CCEX + \dfrac{CBEX.CBCX}{CBEX+CBCX}\right]} \qquad (4.50)$$

$$VBE = VBEIN + XIBIN \,.\, RBB$$

$$= VBEIN + (XIBE + (CBE + CBC) + DVBEIN - CBC.DVCEIN).RBB$$

$$= VBEIN + XIBE.RBB + RBB.(CBE + CBC).DVBEIN - RBB.CBC.DVCEIN$$

(4.51)

$$VCE = VCEIN + XICIN \,.\, RCC$$

$$= VCEIN + (QB/TC - CBC.DVBEIN + CBC.DVCEIN).RCC$$

$$= VCEIN + (QB/TC).RCC + CBC.RCC.DVCEIN - CBC.RCC.DVBEIN$$

(4.52)

Solving Equation (4.51) and Equation (4.52) for DVBEIN and DVCEIN, we get:

$$DVBEIN = \frac{(VBE-VBEIN-XIBE.RBB+RBB.(VCC-VCEIN-(QB/TC).RCC)/RCC)}{RBB \,.\, CBE} \qquad (4.53)$$

and,

$$DVCEIN = \frac{VCC-VCEIN-(QB/TC).RCC + \dfrac{RCC.CBC.(VBE-VBEIN-XIBE.RBB)}{RBB.(CBE+CBC)}}{RCC \,.\, CBC.CBE/(CBE+CBC)} \qquad (4.54)$$

In addition, we have:

$$DQB = XIB - QB/TB \qquad (4.55)$$

$$DQS = XIBX - QS/TS \qquad (4.56)$$

$$XIBE = XIBEO.(EXP(Q.VBEIN/MBE.XK.TEMP) - 1) \qquad (4.57)$$

Equations (4.53 and 4.54) are the same as Equations (4.35 and 4.37) while Equation (4.30) is now replaced by Equation (4.48) and Equation (4.37) is replaced by Equation (4.50). This shows that the effect of the base collector stray capacitance is to increase the delay of the output signal by increasing the delay of VBE and VCE, while the junction capacitance CBC increases the delay of the output signal by increasing the delay of VBEIN and VCEIN.

Figures (4.15 and 4.16) show the experimental and predicted curves for this case and Table IV summarizes the results.

From Table IV, we see that the differences are within 10% which are reasonable considering the errors made in reading and plotting the results and also in measuring the parameters.

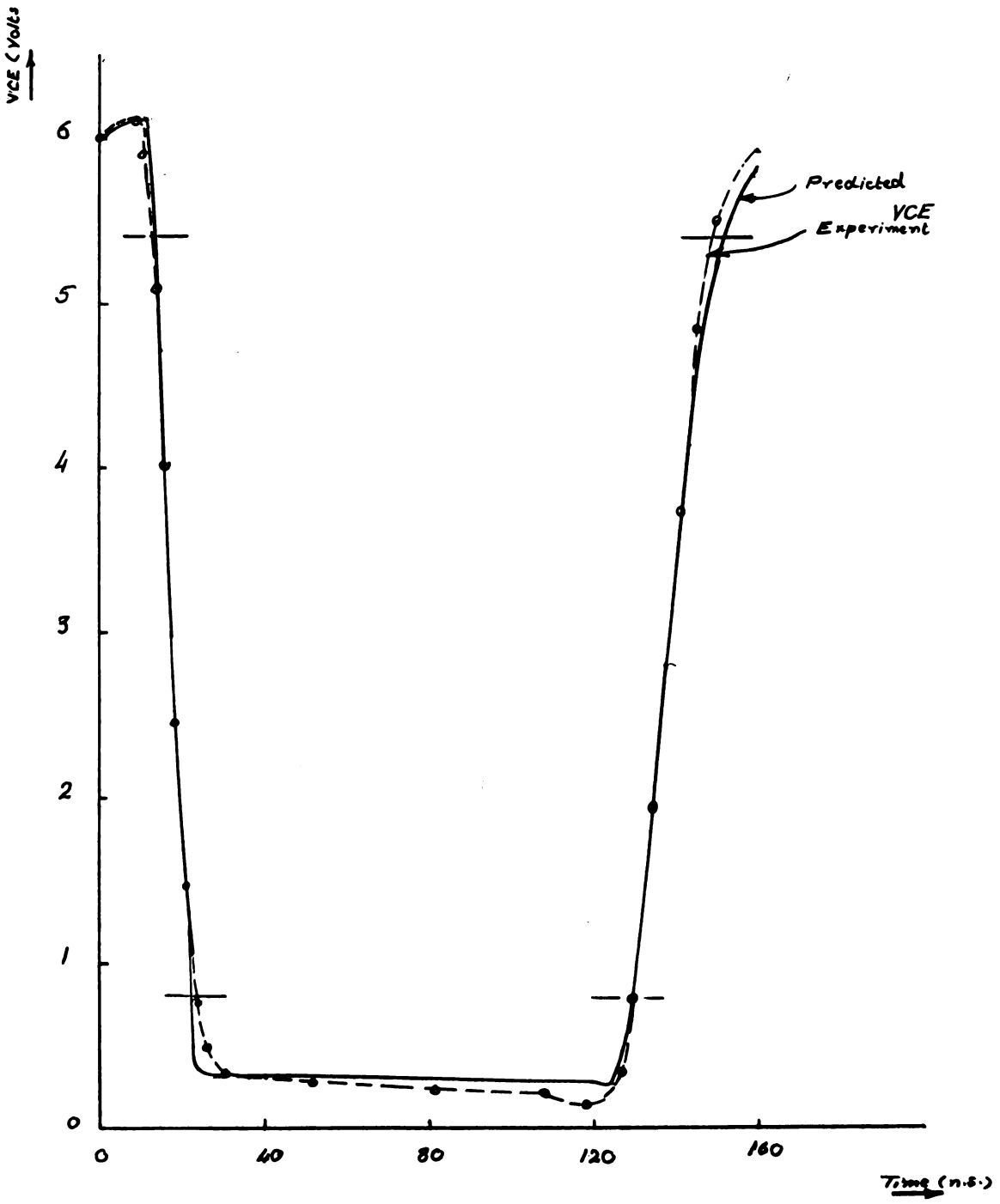

Fig. (4.15) Base Emitter, Collector Emitter and Base Collector Junction Capacitances under Heavy Drive Conditions

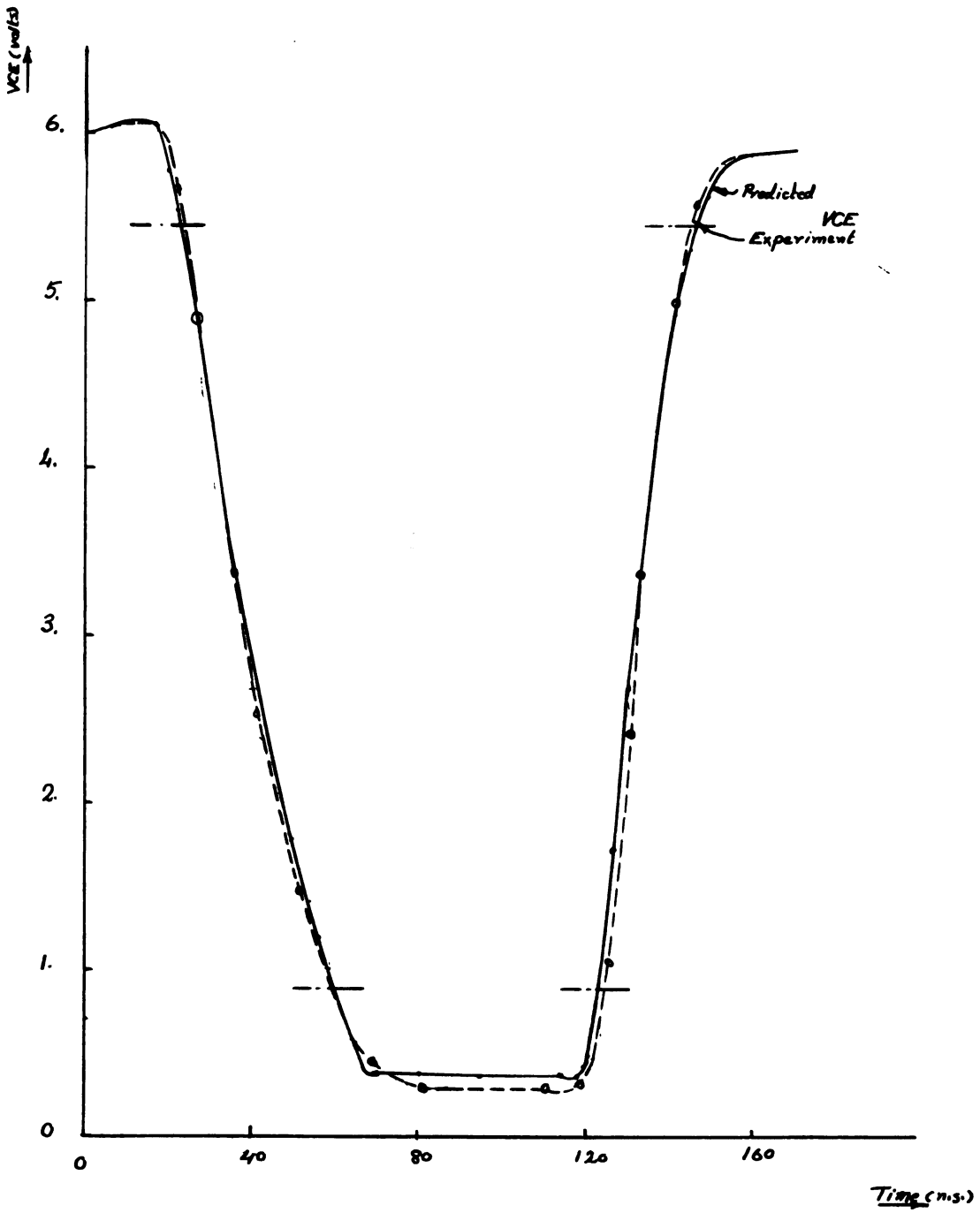

Fig. (4.16) Base Emitter, Collector Emitter and Base Collector Junction Capacitances under Light Drive Conditions

TABLE IV

Comparison Between Experimental and Predictable Results with all Capacitance Included

Turn on Delay, n.s.		
Predicted, t_{dp}	12.25	22.5
Experiment, t_{de}	12	23
Difference	0.25	0.5
% Error	2.08	-2.18%
Rise Time, n.s.		
Predicted, t_{rp}	10	37.5
Experiment, t_{re}	11	36
Difference	-1	1.5
% Error	-9.1%	4.15%
Fall Time, n.s.		
Predicted, t_{fp}	22.5	23
Experiment, t_{fe}	21	22
Difference	1.5	1
% Error	4.15%	4.55%
Saturation Time, n.s.		
Predicted, t_{sp}	16	9
Experiment, t_{se}	15.5	10
Difference	0.5	-1
% Error	3.22%	-10%

Summing up, Fig. (4.17) shows the outputs of cases 5.1, 2, 3, and 4, as compared to the experimental output; under light drive conditions.

Defining the TURN OFF DELAY as the time elapsed between the moment when the input signal falls to 90% of its final steady state value, and the moment when the output signal falls to 50% of its maximum steady state value. Table V gives a comparison of the turn off delay time for each of the four previous cases.

TABLE V

Effect of Difference Junction and Stray Capacitance on the Turn Off Delay Time

	Experiment	Predicted	Difference	%error
Heavy Driving Conditions				
Case a	25	15	-10	-40%
Case b	25	16	-9	-36%
Case c	25	22	-3	-12%
Case d	25	24	-1	- 4%
Light Driving Conditions				
Case a	16.5	8	- 8.5	-51.5%
Case b	16.5	10	- 6.5	-39.4%
Case c	16.5	13	- 3.5	-21.2%
Case d	16.5	15.5	- 1	- 6.1%

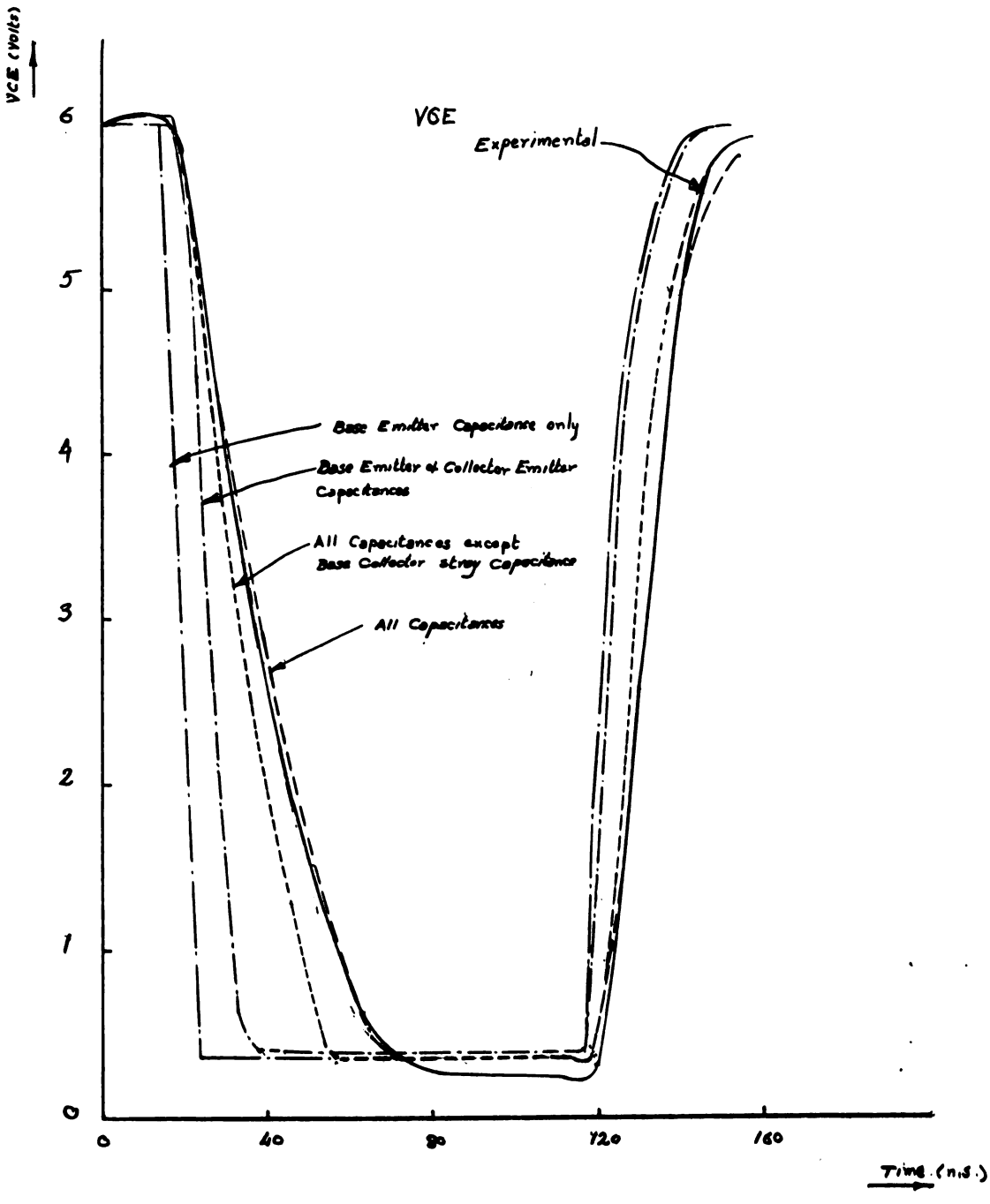

Fig. (4.17) Effect on Adding Different Capacitances on the Predicted Output as Compared to the Experimental Results

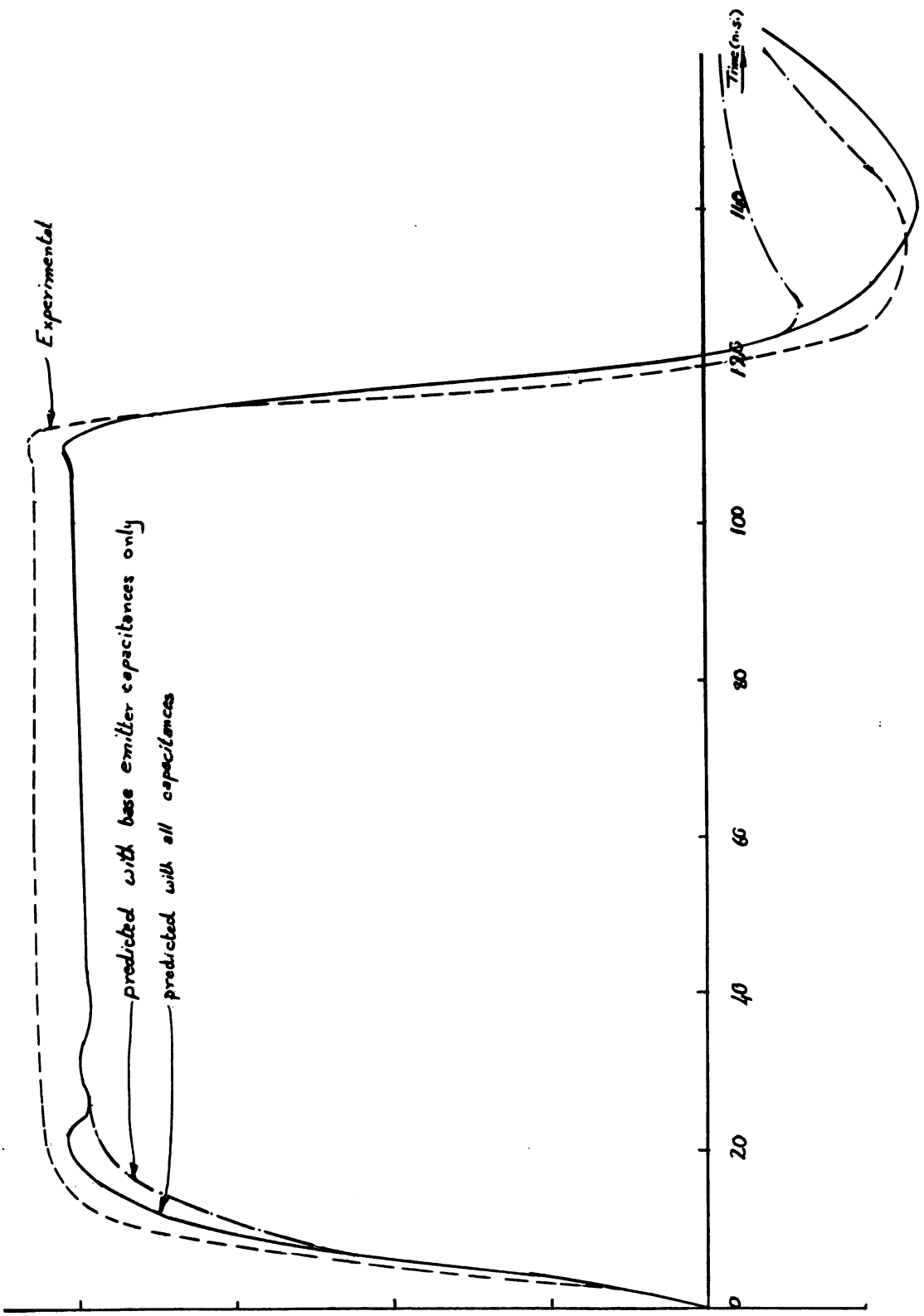

Fig. (4.19) Predicted Base Currents and Experimental Ones Under Heavy Drive Conditions

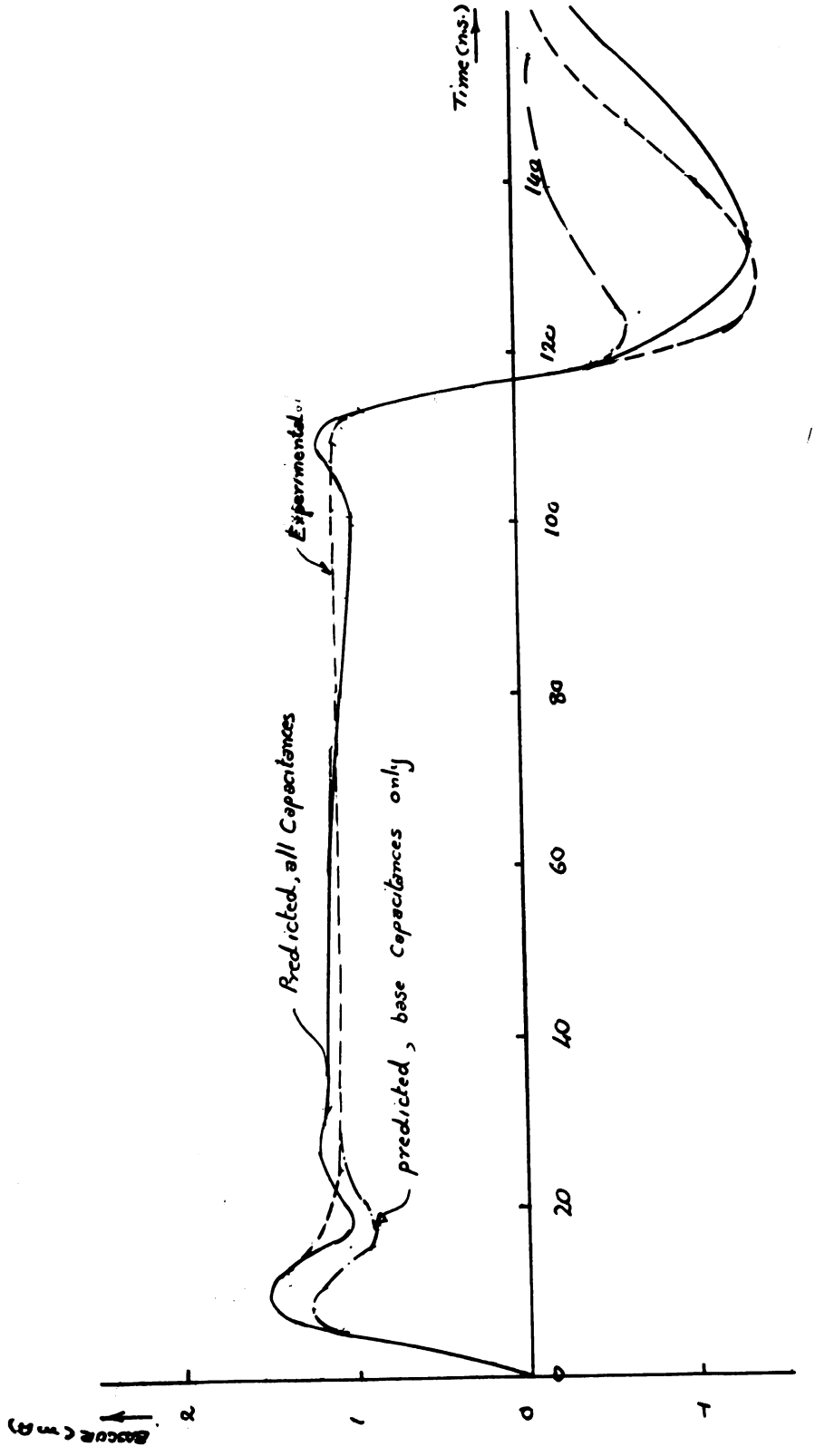

Fig. (4.18) Predicted Base Currents and Experimental Ones Under Line Drive Conditions

Figures (4.18) and 4.19) show the predicted base currents for the case when the base emitter capacitances are the only ones included, and the case when all capacitances are included, together with the experimental result.

In the case of heavy drive condition, the error in the maximum steady state magnitudes is 0.25/4. = 6.25%, and in the case of light drive it is 7%. This error could be due to an error in reading the bias voltage, as a very small error in reading this quantity will result in a relatively large error in the base current, which depends greatly on VBEIN, and this voltage is the exponent of the exponential term in Equation (4.57).

4.5 Additional Test Circuits

The test circuit shown in Figure (4.20) was used in testing the transistor model with a sine wave input and a triangular wave input with a resistive load and an inductive load.

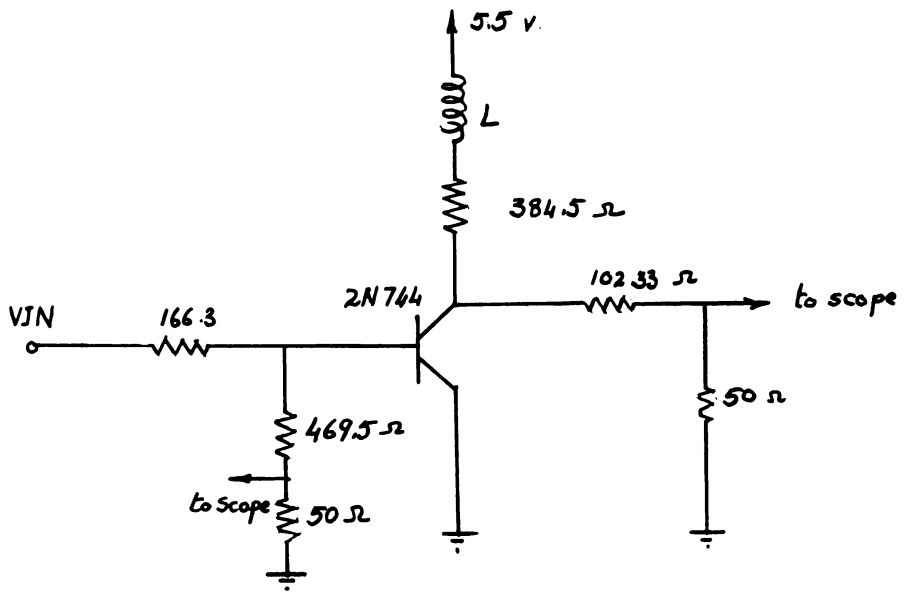

Fig. (4.20) Test circuit used with sine and triangular wave inputs.

In the following discussion, Cases a, b and c will refer to the following:

Case a, repetitive triangular wave form input, 100 n.s. cycle duration time, with resistive load, L = 0

Case b, repetitive triangular wave form input, 100 n.s. cycle duration time, with inductive load, L = 2μH

Case c, repetitive sine wave input, 100 n.s. cycle duration time, with resistive load, L = 0.

Figures (4.21, 4.22, and 4.23) show the predicted and experimental input and output wave forms in these three cases.

4.6 Discussion

In this chapter the suggested equivalent circuit of the transistor was tested. Three different circuits were used, capacitive, resistive and inductive.

The correlations between the experimental and predicted results were very good with resistive and capacitive circuits. However, with inductive circuits the correlations were not quite as good. Although the difference in case of the inductive load was comparatively high, the predicted wave forms have almost the same shape. The main error in case of inductive loading is in the rise and fall times, however, the turn on delay and storage time are fairly accurate.

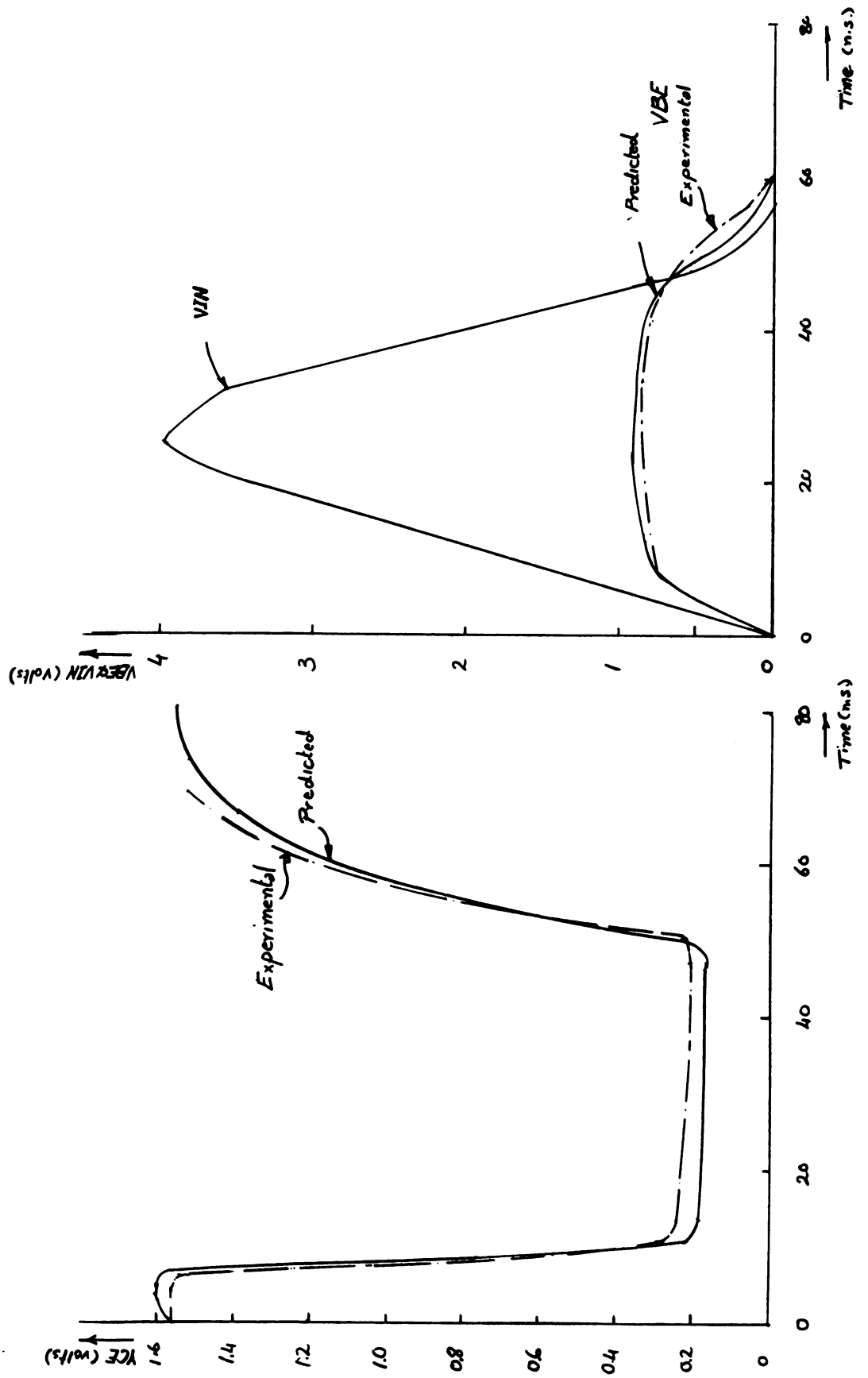

Fig. (4.21) Correlations between Experimental and Predicted Results in Case a.

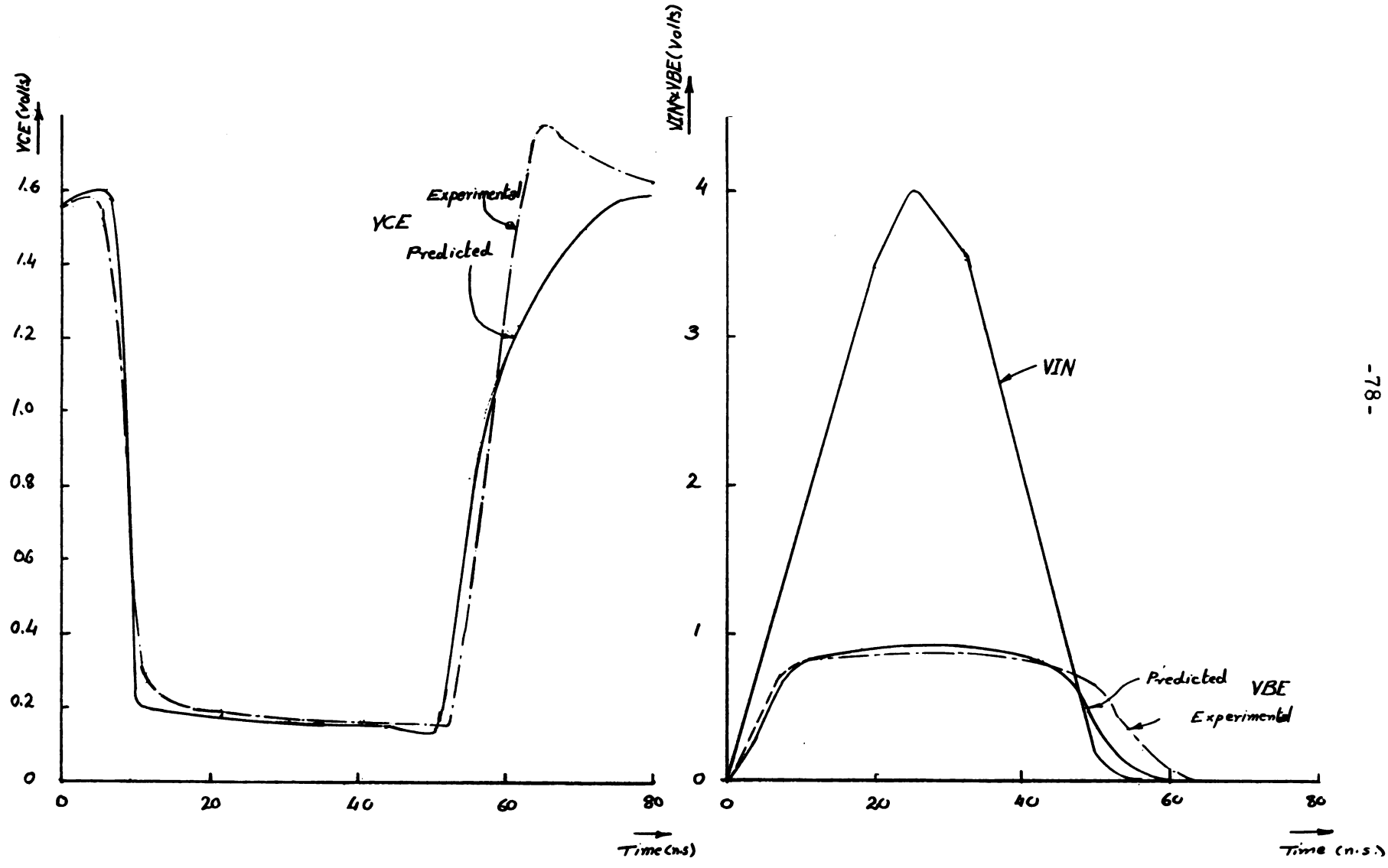

Fig. (4.22) Correlations between Experimental and Predicted Results in Case b.

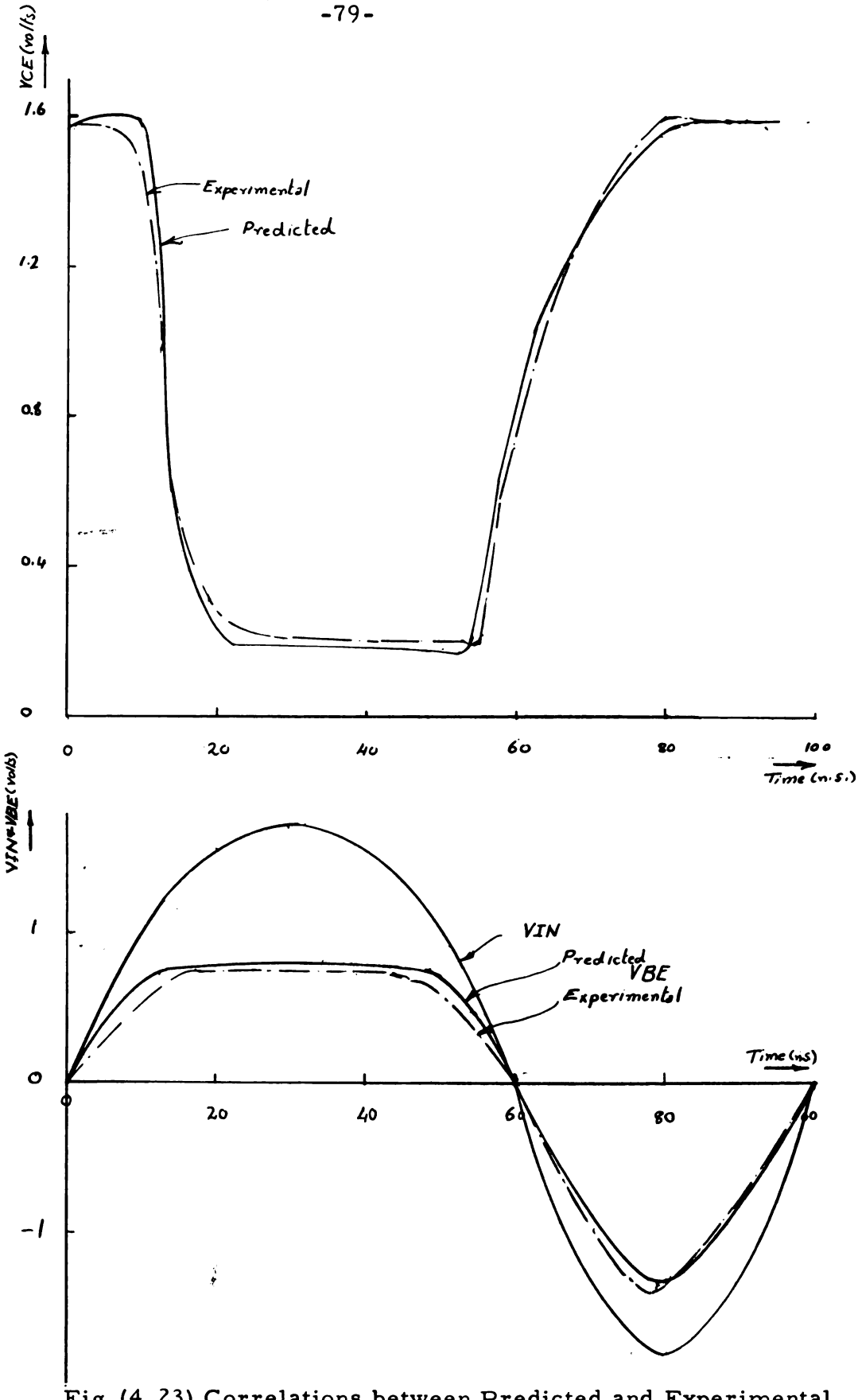

Fig. (4.23) Correlations between Predicted and Experimental Results in Case c.

CHAPTER V

CONCLUSION

The previous study has shown that the suggested transistor model is capable of giving a good approximation to the actual device performance, at least in most of the cases tested.

The incorporation of the defined partial saturation region was significant in predicting collector saturation voltage levels close to the actual ones.

The computer analysis program allows the use of the transistor in all possible modes of interconnection. When the circuit time constant is large compared to the time increment required to solve the state model, MISTAP has the advantage of reducing the solution time to a minimum through the use of numerical techniques to solve nonlinear algebraic equations. In cases when the collector emitter is selected as a branch, the solution must be achieved through the use of differential equations, independent of the time constant of the external network, since there is no direct relation between the base control charge Q_B, and the collector emitter voltage.

Future work should include investigation of the validity of the suggested model in describing different transistors and in its use in different types of circuits. The effects of inductive loading on rise and fall times should be investigated. Also, work should be done in order to make possible the use of algebraic equations alone to solve cases when the collector emitter is selected as a branch, and the time constant of the external network is much greater than that of the transistor.

APPENDIX I

SOLUTION FOR THE CURRENT THROUGH A P-N JUNCTION WHEN THE VOLTAGE IS SPECIFIED BY NEWTON RAPHSON METHOD

Consider Fig. (A-1) and assume that the current through the p-n junction is given by

$$I_D = I_0(e^{KV_D} - 1) \tag{A1}$$

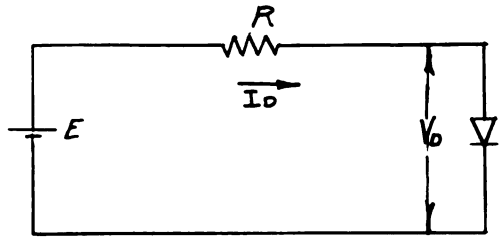

Fig. (A-1) P-N Junction in Series with a Resistance

$$\text{Let } F = I_D - I_0(e^{KV_D} - 1) \tag{A2}$$

$$dF = dI_D - KI_0 e^{KV_D} dV_D \tag{A3}$$

we want F so that

$$F + dF = 0$$

$$\text{or } dI_D - KI_0 e^{KV_D} dV_D = -I_D + I_0(e^{KV_D} - 1) \tag{A4}$$

$$\text{now } I_D = \frac{E - V_D}{R} \tag{A5}$$

$$\text{or } dI_D = -\frac{dV_D}{R} \tag{A6}$$

Substituting (A6) in (A4), we get

$$-\left[\frac{1}{R}\,dV_D + KI_0\,e^{KV_D}dV_D\right] = -I_D + I_0(e^{KV_D} - 1)$$

$$\therefore\ dV_D = \left[1/[\frac{1}{R} + KI_0e^{KV_D}]\right][+I_D - I_0(e^{KV_D} - 1)] \qquad \text{(A7)}$$

In order that the effect of the external circuit on dV_D be neglected

$$\frac{1}{R} << KI_0e^{KV_D} \approx KI_D$$

$$K \approx 40$$

for $I_D = 1$ mA

$$\frac{1}{R} << 40 \times 10^{-3}$$

or $R >> 25$ ohms

If $I_D = 10$ mA $\quad \frac{1}{R} << 40 \times 10^{-2}$

or $R >> 2.5$ ohms

So, in general, the change in dV should be considered. However, the following discussion will show that the effect of including the variation in dV is only to slow the convergence and will not affect the final answer.

Referring to Fig. (A2), for any voltage V_D, there will always exist a current I_D, hence during solution, the voltage and currents will oscillate between two finite limits.

At these limiting points

$$dV = -x\,dI \qquad \text{(A8)}$$

where: $x > 0$

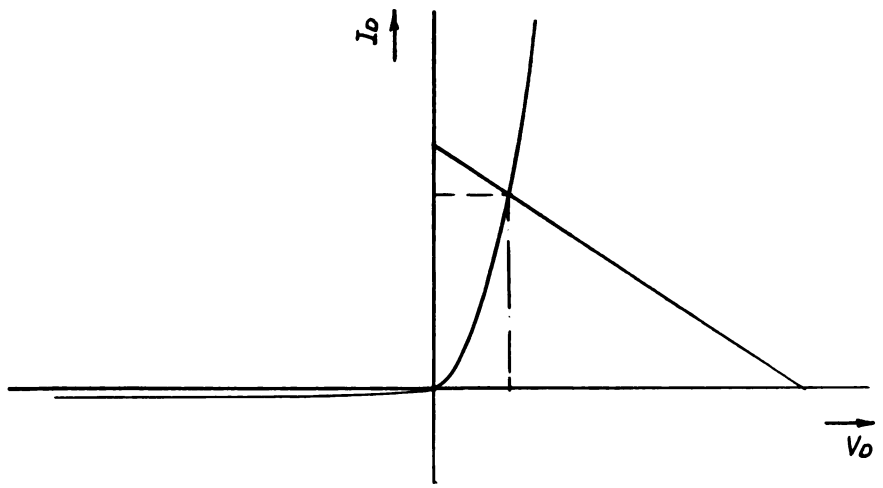

Fig. (A2) Diode Characteristics

Substituting (A8) in (A3), we get

$$dF = (dI_D + KX\, I_0\, e^{KV_D}\, dI_D)$$
$$\approx (1 + KX\, I_D)\, .\, dI_D \qquad \text{(A9)}$$
$$\frac{dF}{dID} = 1 + KXI_D$$

and hence the iteration formula is

$$I_{D1} = I_{D0} - \frac{F(I_{D0},\ V_{D0})}{1 + KXI_{D0}} \qquad \text{(A10)}$$

if the variation in dV is not included

$$I_D = I_{D0} - F(I_{D0}) \qquad \text{(A11)}$$

From Equations (A10) and (A11), it is obvious that the effect of including the variation in dV is simply to prolong the iteration time.

If X in Equation (A10) is such that

$$KXI_{DO} = -1$$

a solution cannot be obtained although it exists. Thus, in order to avoid problems and to get faster iteration, the effect of dV is neglected.

In MISTAP, the base current was described by

$$I_B = I_{BO}.(EXPF(K(VBE - IB.RBB)) - 1) \qquad (A12)$$

$$F = I_{BO}.(EXPF(K(VBE - IB.RBB)) - 1) - I_B \qquad (A13)$$

$$DF = - K.RBB.I_{BO}EXPF(K(VBE - IB.RBB)) - 1) \qquad (A14)$$

and the iteration formula is

$$IB = IBO - \frac{F(IBO)}{DF(IBO)} \qquad (A15)$$

APPENDIX II

SOLUTION FOR THE VOLTAGE ACROSS A P-N JUNCTION WHEN THE CURRENT IS THE SPECIFIED VARIABLE

Referring to Equation (A1) for any current $I_D \geq -I_{D0}$ there will always be a unique voltage V_D.

Rewritting Equation (A1)

$$I_D = I_{D0}(e^{KV_D} - 1)$$

or $$\frac{I_D + I_{D0}}{I_{D0}} = e^{KV_D}$$

$$V_D = \frac{1}{K} \ln \left[\frac{I_D + I_{D0}}{I_{D0}} \right]$$

$$F = \frac{1}{K} \ln \left[\frac{I_D + I_{D0}}{I_{D0}} \right] - V_D \qquad \text{(A16)}$$

$$dF = \frac{1}{K} \cdot \frac{I_{D0}}{I_D + I_{D0}} \cdot dI_D - dV_D \qquad \text{(A17)}$$

it is again required to have dF such that

$$F + dF = 0$$

$$\frac{1}{K} \frac{I_{D0}}{I_D + I_{D0}} dI_D - dV_D = -\frac{1}{K} \ln \frac{I_D + I_{D0}}{I_{D0}} + V_D$$

Referring to Fig. (A1) and substituting Equation (A6) in Equation (A17), we get

$$\left[\frac{1}{K} \cdot \frac{I_{D0}}{I_D + I_{D0}} + R \right] dI_D = -\frac{1}{K} \ln \left[\frac{I_D + I_{D0}}{I_{D0}} \right] + V_D \qquad \text{(A18)}$$

in order that the effect of the external circuit be neglected.

$$R << \frac{1}{K} \quad \frac{I_{D0}}{I_D + I_{D0}} \approx \frac{I_{D0}}{KI_D}$$

Since $I_{D0} \approx 10^{-15}$ and $K \approx 40$

for $I_D = 1mA$

$$R << \frac{10^{-15}}{40 \times 10^{-3}} = .025 \times 10^{-12} \text{ ohms}$$

Again the effect of the external circuit on dI_D cannot be ignored. However, the following argument will show that taking it into consideration will mainly reduce the speed of convergence and might cause indeterminate solutions. Substituting Equation (A8) in Equation (A17) and we get

$$dF = \left(- \frac{1}{KX} \cdot \frac{I_{D0}}{I_D + I_{D0}} - 1 \right) dV_D$$

and the iteration formula is

$$V_D = V_{D0} + \frac{F(V_{D0}, I_{D0})}{1 + \frac{1}{KX} (I_{D0}/I_D + I_{D0})} \tag{A19}$$

If the variation in I_{D0} is not included

$$\therefore V_D = V_{D0} + F(V_{D0}) \tag{A20}$$

In MISTAP, the base current was given by

$$IB = IB0(EXP(K(VBE-IB.RBB))-1)$$

or $$\frac{IB + IB0}{I_{B0}} = EXP(K(VBE - IB \cdot RBB))$$

or $$V_{BE} = \frac{1}{K} \ln\left(\frac{IB + IB0}{IB0}\right) + IB \cdot RBB \qquad (A21)$$

Equation (A21) is used to determine the voltage across the junction given the current through it.

APPENDIX III

INPUT-OUTPUT Information for MISTAP

The following information adds to what has been previously mentioned in Chapter VII about MISTAP. It is information about input quantities which have to be supplied before MISTAP is called and output quantities supplied by MISTAP.

Temp (I)	Temperature of transistor I
Q	Magnitude of electronic charge
XK	Magnitude of Boltzmann's Constant
XMBE(I)=MBE(I) in (7.34)	A constant giving the value of effective voltage across base emitter junction
XMBC(I)=MBC(I) in (7.35)	A constant giving the value of of effective voltage across base collector junction
MTYP	Number of transistor types (different characteristics)
ITYP(I)	$1 < I < N$ give the type of I^{th} transistor $1 < \lvert ITYP(I) \rvert < MTYP$ is negative, for NPN transistor, is positive for PNP transistor
N	Number of transistors for which a solution is required
IN(I)	+1 if graph element representing base emitter is a branch -1 if graph element representing base emitter is a chord

JO(I)	+1 if the graph element representing collector emitter is a branch -1 if the graph element representing collector emitter is a chord for the I^{th} transistor
VIINA(I)	for IN(I) = +1 input current for transistor I for IN(I) = -1 input voltage for transistor I
VIOUTA(I)	for JO(I) = +1 output current for transistor I for JO(I) = -1 output voltage for transistor I
VIINB(I)	for IN(I) = +1 input voltage for transistor I for IN(I) = -1 input current for transistor I
VIOVTB(I)	for JO(I) = +1 output voltage for transistor I for JO(I) = -1 output current for transistor I
EPSILO	A constant regulating accuracy to be obtained

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