## DESIGN AND IMPLEMENTATION OF EFFICIENT ENERGY HARVESTING CIRCUITS FOR ULTRA LOW POWER AND IMPACT ENERGY APPLICATIONS

By

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#### ABSTRACT

## DESIGN AND IMPLEMENTATION OF EFFICIENT ENERGY HARVESTING CIRCUITS FOR ULTRA LOW POWER AND IMPACT ENERGY APPLICATIONS

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The battery-powered electronic systems, such as wearable and mobile device, wireless sensors, implantable bio-medical devices, etc., have widely appeared in our daily life to improve the life quality and work efficiency. However, the dependence on batteries has brought great challenges to current electronic devices in many aspects, such as system miniaturization, massive deployment, device lifetime and environmental pollution, etc. To address these issues, the idea of harvesting the energy from the ambient environment instead of the battery has been proposed. Various energy harvesting technologies have been implemented as the alternative solutions for the battery-powered electronic devices. However, low PCE (power conversion efficiency) prevents these energy harvesting technologies is the power threshold which is the minimum energy that can be harvested by the energy harvesting systems. Actually the power threshold sets the lower limit of the capability for energy harvesting systems, therefore, overcoming the threshold effect could significantly improve the efficiency of the energy harvesting systems. The objective of this dissertation is to investigate the power conversion efficiency and the power threshold of energy harvesting technologies, and then propose several solutions to overcome these issues.

Firstly, the RF energy harvesting front-end which consists of an antenna, matching network and rectifier is examined due to pervasive wireless power in the environment. The conventional matching network in the near field RF energy harvesting front-end needs to trade-off between the coupling coefficient and Q-factor. In chapter 2, a high-Q series resonant matching network is proposed so that both of high coupling coefficient and high-Q matching network can be obtained at the same time, therefore the power conversion efficiency of the near filed RF energy harvesting can be significantly improved. Besides the matching network, the rectifier also plays a key role in RF energy harvesting systems. The major bottleneck of the RF rectifier is nearly zero power transfer efficiency when the input power is below the power threshold. Such operating region is called "dead zone" for the RF rectifier. To free the dead zone, a hybrid rectification technique which utilizes both of RF power and vibration power to efficiently harvest the energy below the threshold level is proposed in chapter 3. This technique utilizes low-frequency and low-power piezoelectric signal as the biasing circuit of the RF rectifier so that the threshold voltage of the RF rectifier can be optimized and thus effective power threshold is significantly reduced.

In addition to the RF energy harvesting, vibration energy harvesting is also crucial, especially for the sensors embedded inside the structural and/or underneath the ground. Compared to continuous RF energy, the vibration energy is impulsive so that it is difficult for the harvester to capture the whole energy during a short pulse period. However, if the impulsive energy can be stretched in the time domain while keeping the total energy constant, the harvesting duration will become longer so that it is possible for the harvester to harvest the whole energy. Based on this idea, a non-linear compressive circuit, named "time-dilation circuit", is proposed in chapter 4. This technique can quickly respond to the impulsive energy so that the dynamic harvesting range is extended.

Comparing to electromagnetic propagation, acoustic propagation has less attenuation in the conductive media. Thus, the ultrasonic energy harvesting attracts more interest for the sensors embedded inside composite materials or human body. Furthermore, the use of ultrasound also allows miniaturization of the embedded telemetry system by relaxing the transducer size. In chapter 5, a CMOS system-on-chip (SOC) ultrasonic receiver tag is implemented to investigate the ultrasonic energy harvesting and telemetry. This system can not only harvest its operational energy directly from the acoustic interrogation signal, but also achieve bi-directional communication using acoustic back-scattering, thus it is successfully shown that the ultrasonic energy harvesting and telemetry is a proper solution for such applications.

Finally, the contributions of this dissertation and open problems for future work are summarized in chapter 6. This dissertation is dedicated to my family: my dear mother Ying Liu, my passed father Yucai Feng, my wife Ling Sun and my lovely son Kevin Jinyuan Feng as well as my parents-in-law Yuanbi Sun and Yurong Ma.

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#### **CHAPTER 1**

### **INTRODUCTION**

# 1.1 Introduction of Energy Harvesting

Energy harvesting, also known as power harvesting or energy scavenging, is generally defined as the process of scavenging various energies from ambient environment. The harvested energies are then accumulated and stored for either immediate or later use [10]. The concept of energy harvesting is not brand new and its history can date back to B.C. when the windmills and watermills were invented. Such kinds of energy harvesting methods can be classified as macro-scale energy harvesting since the energy sources are renewable energy so that the available power level is usually above kilowatt. In recent years, as the rapid development of semiconductor devices and integrated circuits, various energy harvesting technologies have been invented and implemented, such as electromagnetic, thermoelectric and vibration energy harvesting, etc. These technologies have driven energy harvesting into a micro-scale level to meet the growing energy demand of the world.

Different from its macro-scale counterpart of which the common goal is to feed the utility grid, the micro-scale energy harvesting technologies aim to provide the perpetual device without feeding the grid. It is known that battery-powered solution is also able to free the electronic systems from power cord. But the lifetime of battery-powered solution is limited (usually several years), so the maintenance effort could exponentially increase as the sensor network expands. Energy harvesting is a very practical and useful supplementary method for lifetime extension of the battery-powered systems. It even can replace the batteries so that the lifetime of the system only depends on the device itself. In addition, environmental pollution is an increasing concern in our society. By getting rid of the battery, energy harvesting is a very promising solution to the environment protection. Last but not least, the electronic system can be further miniaturized without the battery, so more and more applications and markets could be explored, such as wearable and implantable devices, etc.

	Macro-scale	Micro-scale	
Energy Sources Renewable energy (e.g., so-		Environmental energy (e.g.,	
	lar, wind, etc.)	vibration, electromagnetic ra-	
		diation, etc.)	
Energy Level above kilowatt		below milliwatt	
Purpose Reduce the dependence to		Prolong system's lifetime and	
natural resources (such a		ultimately provide perpetual	
gas, coal, etc.)		devices	

Table 1.1 Macro-scale v.s. micro-scale energy harvesting comparison.

Ubiquitous environmental energy sources, such as solar, thermal, vibration and electromagnetic energy, have been explored and developed in many research studies during the last decades. Compared to macro-scale energy transducers which are characterized by the energy density, the micro-scale energy transducers use the power density as the main figure-of-merit. Table. 1.2 shows the power density of four popular energy sources. It is obvious that the solar energy has the highest power density and is quite suitable for outdoor applications, but the disadvantage is also quite conspicuous due to the need of light. Thermal energy has medium power density and is suitable for the industry applications, especially for the machines with huge temperature difference, but it is not applicable for the constant temperature environment such as office building. Vibration energy and electromagnetic energy are usually ubiquitous in the environment, but it is a great challenge for the energy harvesters to capture them due to the small power density. Thus the use of the energy

Energy Sources	Power Density
Solar	Outdoors $10 \text{mW}/cm^2$ ; Indoors $10 \mu \text{W}/cm^2$

Table 1.2 Power density of four popular energy sources [1].

	, , , , , , , , , , , , , , , , , , ,
Thermal	Human $25\mu$ W/cm <sup>2</sup> ; Industrial 1-10mW/cm <sup>2</sup>
Vibration	Human $4\mu$ W/ <i>cm</i> <sup>2</sup> ; Industrial $100\mu$ W/ <i>cm</i> <sup>2</sup>
Electromagnetic	Ambient Source (GSM): $0.01 \mu W/cm^2(100m)$ -
	$0.3\mu$ W/cm <sup>2</sup> (25m); Dedicated Source (EIRP)
	4W): $1.27 \mu W/cm^2$ (5m)



Figure 1.1 General energy harvesting system model.

harvesting technologies depend on the practical applications and available energy sources.

## **1.2 Energy Harvesting System Model**

Any energy harvesting system can be modeled as a transducer connecting with the load impedance which represents the power consumption of the load system, as shown in Fig. 1.1. The transducer converts the ambient energy to electrical energy which is represented by voltage source  $V_{OC}$ . The transducer itself has an equivalent electrical output impedance  $Z_S$  which varies with source voltage  $V_{OC}$  and its operating frequency  $f_S$ . As it can be seen in Table. 1.3, each source has a wide range of open circuit voltage and its operating frequency could also vary, so the source impedance is not fixed. It is known that  $Z_L$  and  $Z_S$  should be a conjugated match for maximum power transfer. However,  $Z_L$  is also variable because the power consumption of the load system is not always constant. In addition,  $Z_L$  is also affected by the source voltage. Therefore, how to efficiently harvest the energy is the major task for every energy harvesting system.

Conventional energy processing circuits consist of AC-DC conversion and DC-DC conversion as shown in Fig. 1.2. The AC power sources such as vibrational and electromagnetic energy should firstly feed the AC-DC converter and then perform DC-DC conversion, while the DC power sources such as thermal and solar energy can be directly DC-DC converted. For AC-DC conver-

Energy Sources	Typical Open Cir-	Operating Fre-	Typical Source Impedance $Z_S$
	cuit Voltage V <sub>OC</sub>	quency $f_S$	
Solar	$0.5 \mathrm{V} \sim 5 \mathrm{V}$	DC	Variable impedance: $1k\Omega$ ~
			100kΩ
Thermal	$10 \text{mV} \sim 10 \text{V}$	DC	Constant resistive impedance:
			$1\Omega \sim 100\Omega$
Vibration	$10V \sim 50V$	$0.1 \text{Hz} \sim 1 \text{KHz}$	Constant capacitive impedance:
			$10 \mathrm{k}\Omega \sim 100 \mathrm{k}\Omega$
Electromagnetic	$100 \text{mV} \sim 5 \text{V}$	$100 \text{KHz} \sim 5 \text{GHz}$	Constant inductive impedance:
			$1 \mathrm{k} \Omega \sim 10 \mathrm{k} \Omega$

Table 1.3 Electrical Characteristics of four popular energy sources [2].



Figure 1.2 Conventional Energy Processing Circuits.

sion, although there exist many different circuit typologies, the basic part actually can be thought as a simple half-wave rectifier, which consists of a diode and a storage capacitor. Once the input voltage is above the diode's threshold voltage, the current can charge the storage capacitor. However, below the threshold, the reverse current is comparable to the forward current, leading to a very low power transfer efficiency, thus this area is also called dead-zone for the AD-DC conversion, as shown in Fig. 1.3. The second issue is related to the DC-DC conversion whose function is to efficiently convert the variable DC power. Since the input DC power is variable, to obtain the maximum power transfer, a special technique called maximum power point tracking (MPPT) is usually used.



Figure 1.3 Illustration of dead zone for AC-DC conversion.

MPPT is implemented by the sophisticated control algorithm and can be illustrated by using the solar cell circuit model as shown in Fig. 1.4. The equivalent circuit model of a solar cell mainly consists of a current source and a forward biased diode. The current source  $I_{PH,SC}$  represents the generated photo current,  $R_S$  is the parasitic series resistance,  $R_P$  is the equivalent shunt resistance.  $I_{PH}$  and  $V_{PH}$  are output current and terminal voltage of the solar cell. Therefore the I-V equation for this circuit model can be expressed as

$$I_{PH} = I_{PH,SC} - I_{SAT} \left( e^{\frac{qV_{PH,SC}}{AKT}} - 1 \right) - V_{PH,SC} / R_P$$
(1.1)

where  $V_{PH,SC} = V_{PH} + I_{PH}R_S$ . Fig. 1.4 (b) plots the output current verse the output voltage for the solar cell using this equation for different light intensities. Fig. 1.4 (c) presents the output power of the solar cell as a function of its terminal voltage. It can be seen that for a given light intensity, there exists an optimal output voltage for the solar cell at which the maximum power can be obtained. This point is called maximum power point (MPP). It is noted that the MPP changes significantly as the light intensity changes. Therefore various sophisticated control algorithms have been proposed to track the MPP to ensure the solar cell can always output the maximum power. However, such kind of sophisticated control algorithms require not only more power consumption,





Figure 1.4 Illustration of MPPT by using solar cell application: (a) Typical circuit model for solar cell; (b) Output current v.s. output voltage; (c) Output power v.s. output voltage [3].

but also additional setup time, thus it is difficult to capture impulsive energy whose magnitude could be very high but duration is short.

## **1.3 Research Motivation**

As mentioned in previous section, the available energy that can be harvested in the environment could be quite low and intermittent, thus the efficiency transferred from the harvested energy into the effective electrical energy is a key factor for the successful deployment of the energy harvesting systems. Sophisticated control algorithms and circuits could help to improve the efficiency, but their power consumption could not be affordable for self-powered devices. Based on this analysis, two research questions are proposed: (1) Can the energy be harvested more efficiently for ultra low power applications, eg., when the energy source is in dead-zone? (2) Can the energy be harvested



Figure 1.5 (a) A structural health sensor embedded under the ground; (b) Proposed hybrid energy harvesting method.

more efficiently for impact energy applications, eg., when the energy source is impulsive?

To answer the first question, a hybrid energy harvesting technique is proposed to reduce the threshold effect as shown in Fig. 1.5. Assuming there exist multiple energy sources in the environment, for example, RF power is usually the main power source for structural health sensor, however, if the structural health sensor is embedded under ground, the strain power can be used as an auxiliary power source to improve the efficiency. Specifically, the major source  $V_{OC1}$ , which is RF power in this case, delivers the most of the energy that is consumed by the load, while the auxiliary source  $V_{OC2}$ , is used to decrease the threshold effect, so the power transfer efficiency of the main path is able to be improved.

One proposed solution for the second question is to use a time-dilation technique as shown in Fig. 1.6. Considering two football players come into a head-on collision, the transient energy could be very large but the duration is very short, so conventional energy harvesting system is unable to perform MPPT during such short period. However, if the charging duration can be stretched while the total energy is kept constant, the following DC-DC converter may have more time to perform MPPT algorithm. Actually this idea is to make the energy storage capacity adaptive through a simple sensing circuit, specifically, small storage capacity can achieve the fast response while the



Figure 1.6 (a) Illustration of stretching impulsive energy in time domain ; (b) Proposed time-dilation method.

large storage capacity is able to fully capture the energy.

# 1.4 Thesis Contributions and Organization

This dissertation will focus on the design and implementation of the efficient energy harvesting circuits for ultra low power and impact energy applications. The major contributions in this dissertation includes:

1. A high-Q series impedance matching technique is proposed in chapter 2 to improve the power transfer efficiency for near-field RF energy harvesting applications. The conventional parallel matching technique is widely used in current RF energy harvesting applications. However, one major limitation is the trade-off between the Q-factor of the impedance matching network and the coupling coefficient of the energy transfer link. Based on the series matching network, the proposed impedance matching technique can not only achieve high Q-factor and low loss, but also release the constrain between the Q-factor and the coupling coefficient, so that the energy harvesting efficiency is significantly improved.

2. A hybrid rectification technique is proposed in chapter 3 to improve the power transfer efficiency of the voltage rectifier for ultra low power applications. In the hybrid rectification technique, the main energy harvesting source is RF energy while the auxiliary source is low-frequency and low-power vibration energy. In ultra low power applications, the conventional voltage rectifier faces the threshold issue, that is to say, the power transfer efficiency of the voltage rectifier is near to zero when the input power is below the power threshold. To overcome this issue, the proposed hybrid rectification technique utilizes the low frequency vibration signal as the DC bias of the high frequency RF signal, thus the effective threshold is reduced and the power transfer efficiency is improved.

3. A non-linear compressive circuit is proposed in chapter 4 to improve the power transfer efficiency of the harvesters for impact energy applications. This compressive circuit consists of a full wave rectifier and a time-dilation circuit. When the impulsive signal exceeds the preset threshold, the time-dilation circuit is triggered to provide an additional way to store the impulsive energy, thus the energy can be harvested as much as possible.

In addition, this dissertation also presents one system-level design for ultrasonic energy harvesting and back-telemetry in chapter 5. This system implementation is to prove that the near-field passive ultrasonic telemetry system could be used for embedded monitoring inside the conductive structures and ionic media where the RF attenuation is significant.

Finally, chapter 6 summarizes the contributions of this research and also points out the open problems that could be future directions for this work.

9

#### **CHAPTER 2**

### **HIGH-Q SERIES RESONANT Z-MATCHING NETWORK**

## 2.1 Introduction

As the rapid development of the wearable, implantable and embedded devices, wireless energy scavenging techniques have become increasingly important over the past few years [3], especially in the applications of body area networks [11], [12], implantable bio-medical devices [13], [14], and structural health monitoring [15], [16], etc. Fig. 2.1 shows a typical RF energy harvesting system which is widely used in the near field applications. The power is wireless transferred from the reader to the transponder through inductively coupling of the two coils and then an AC-DC rectifier (or voltage multiplier) converts the coupled AC power to DC power for proper operation of the processing circuit. Thus high efficiency energy conversion is desired in such energy-constrained system. In this chapter, a high-Q series resonant impedance matching network is proposed to improve the power transfer efficiency of the wireless energy harvesting link.

### 2.2 Parallel Resonant Method

Inductive coupling is widely used in wireless power transfer system, particularly in the near field region. The system consists of a reader and a transponder and utilizes two weekly coupled coils to form an inductive link, as shown in Fig. 2.2. The inductive link can be modeled as a transformer with two resonant circuits. The voltage can thus be induced in the transponder coil and then rectified to a DC voltage for proper operating the following processing circuit. Between the processing circuit and the coil, a matching network is needed to resonate the system. Among various matching strategies on the transponder side, parallel matching is the most popular method due to its ease in tuning. However, one major limitation is that the total quality factor  $Q_T$  of the transponder is dependent on its coil inductance  $L_t$ . This implies that if  $L_t$  is constrained by the size of the coil,  $Q_T$ 



Figure 2.1 Block diagram of a typical inductively coupled wireless energy scavenging system.



Figure 2.2 Parallel model of inductive coupling.

and hence the power transfer efficiency and voltage gain are constrained. In this section, we will first revisit the key parameters which affect the performance in parallel matching and then propose a new matching technique to increase its Q-factor to optimize the efficiency.

We first examine the mathematical model in Fig. 2.2. The transformer is formed by the mutual inductances of two coils  $M=k\sqrt{L_rL_t}$ , where k is coupling coefficient which strongly depends on geometry of the two coils and their relative spacing and alignment. Therefore, once the size and the distance between the two coils are fixed, the maximum value of k is usually constrained. The induced voltage in these two coils can be modeled as two dependent voltage sources  $sMi_t$  and  $sMi_r$ . For the sake of simplicity, the RF reader is modeled as a series LC-circuit, where  $L_r$  represents the reader coil inductance,  $R_r$  represents the reader coil resistance and  $V_S$  is the reader source voltage. Similarly,  $L_t$  and  $R_t$  represent the inductance and the resistance of the transponder coil. A matching network is usually required at the transponder to maximize the power transfer to the transponder

load and in effect boost the small induced voltage sMir.

Due to easy tuning, parallel matching is widely used in inductive power link. To resonate the capacitive input impedance of the sensor, the maximum inductance of the transponder coil is constrained. However, in most applications, the coil size is relatively small and hence  $L_t$  is also small, so another parallel capacitor  $C_P$  is still needed to tune the resonant circuit, as shown in Fig. 2.2. For the sake of convenient calculations, we use  $C_{Lp}=C_L+C_P$  and then transform the parallel  $R_LC_{Lp}$  to their series representation, where  $C_{Ls}\approx C_{Lp}$  and  $R_{Ls}=R_L/Q_L^2$ , under the reasonable assumption of  $Q_L\gg 1$ . At the resonant frequency, series  $L_t$  and  $C_{Ls}$  cancel each other, thus the induced voltage  $sMi_r$  is firstly divided between  $R_t$  and  $R_{Ls}$  and then boosted approximately  $Q_L$  times because of the capacitor  $C_{Ls}$ .

Assuming  $R_{Ls} = \alpha R_t$ , the voltage gain  $A_{V_t}$  and the power transfer efficiency  $\eta_{P_t}$  at the transponder side are given by

$$A_{V_t} = \left| \frac{V_L}{sMi_r} \right| = \left| \frac{\frac{1}{j\omega C_{Ls}} + R_{Ls}}{R_t + R_{Ls}} \right| \approx \frac{\alpha}{1 + \alpha} Q_L$$
(2.1)

$$\eta_{P_t} = \frac{P_L}{P_{|sMi_r|}} = \frac{R_{Ls}}{R_t + R_{Ls}} = \frac{\alpha}{1 + \alpha}$$
(2.2)

To relate the transponder side with the reader side, the dependent voltage source  $sMi_t$  is modeled as the transformed transponder impedance  $Z_{tr}=\beta/(1+\alpha)R_r$ , where  $\beta=k^2Q_tQ_r$ . With the help of derivation of  $Z_{tr}$ , it is more intuitive to estimate the voltage gain  $A_{V_r}$  and power transfer efficiency  $\eta_{P_r}$  at the reader side,

$$A_{V_r} = \left|\frac{sMi_r}{V_S}\right| = \frac{\omega M}{R_r + Z_{tr}} = \frac{\omega M}{R_r} \cdot \frac{1 + \alpha}{1 + \beta + \alpha}$$
(2.3)

$$\eta_{P_r} = \frac{P_{Z_{tr}}}{P_S} = \frac{Z_{tr}}{Z_{tr} + R_r} = \frac{\beta}{1 + \beta + \alpha}$$
(2.4)

Assuming the loss through the transmission medium can be ignored at the resonant frequency  $(P_{Z_{tr}} \approx P_{|sMi_r|})$  and hence the total voltage gain  $A_V$  and power transfer efficiency  $\eta_P$  can be obtained by combining (2.1) and (2.3), (2.2) and (2.4) as

$$A_V = A_{V_t} A_{V_r} = \frac{\omega M}{R_r} \cdot \frac{\alpha}{1 + \beta + \alpha} \cdot Q_L$$
(2.5)

$$\eta_P = \eta_{P_t} \eta_{P_r} = \frac{\alpha}{1+\alpha} \cdot \frac{\beta}{1+\beta+\alpha}$$
(2.6)

Substituting  $\alpha = Q_t/Q_L$  and  $\beta = k^2 Q_t Q_r$  into (2.5) and (2.6),  $A_V$  and  $\eta_P$  can be rearranged in terms of Q-factors as,

$$A_V = \frac{kQ_rQ_T}{1+k^2Q_rQ_T} \cdot \sqrt{\frac{L_t}{L_r}}$$
(2.7)

$$\eta_P = \frac{k^2 Q_r Q_T}{k^2 Q_r Q_T + 1} \cdot \frac{Q_t}{Q_t + Q_L} \tag{2.8}$$

where  $Q_T = Q_t Q_L/(Q_t + Q_L)$  is total Q-factor of the transponder side. It is shown that both  $A_V$ and  $\eta_P$  improve as the increase of  $Q_T$ . Since generally  $Q_L \ll Q_t$  (suppose  $Q_t > 100$  and  $Q_L$  is  $5\sim10$ ),  $Q_T$  is mainly determined by  $Q_L$  and thus increasing  $Q_L$  is more practical to improve  $A_V$ and  $\eta_P$ . However, for parallel matching in which  $Q_L = R_L/(\omega L_t)$ , once  $R_L$  (or power consumption of the load) is fixed, increasing  $Q_L$  can only be achieved by decreasing  $L_t$ , which is equivalent to shrink the coil size or reduce the number of turns, but either way would degenerate the coupling coefficient k, which actually is the most important factor affecting the efficiency of the inductive link. Therefore, it is indicated that the trade-off between  $Q_L$  and k is one major limitation for parallel matching strategy to achieve high efficiency.

### 2.3 **Proposed Series Resonant Strategy**

To overcome the limitation imposed by the transponder coil  $L_t$  in the parallel matching strategy, a series matching strategy is proposed [17], as shown in Fig. 2.3 (a). In this series matching network,  $C_1$  is set to be *m* times of  $C_{Lp}$  while keeping  $R_L$  constant, thus  $Q'_L$  increases to  $mQ_L$  and the series form of the load resistor  $R'_{Ls}$  decreases to  $R_{Ls}/m^2$ , resulting in  $\alpha$  shrinking to  $1/m^2$  times.  $C_2$  is chosen to be  $m/(m-1)C_{Lp}$  for resonance. To tune the circuit more easily, a high-Q inductor  $L_1$  is series inserted between  $C_2$  and  $C_1$  in the practical circuit, as shown in Fig. 2.3 (c).

Firstly we let  $C_2=C_{Lp}$  to resonate with  $L_t$ , this resonance is easily obtained when the impedance of the left series  $L_tC_2$  can only show pure resistance  $R_t$  in Smith Chart; then the same procedure can be applied to the right  $L_1C_1$  matching. Finally, both of the left and right parts are permitted to



Figure 2.3 Mathematical model of the transponder circuit using series matching strategy: (a) Parallel form of the load and (b) their equivalent series form; (c) shows an more convenient method to tune the circuit by replacing single  $C_2$  with a series  $L_1C_2$ .

be connected together only when it is sure that each part resonates very well. After transforming the parallel  $C_1R_L$  to a series  $C_1R_{Ls}$ , the same analysis procedure for the parallel matching strategy is still applicable to the series matching strategy, in which  $\alpha$  and  $Q_L$  are substituted with  $\alpha/m^2$ and  $mQ_L$ , respectively. Another modification is that the parasitic loss imposed by  $L_1$  should be considered. Assuming  $L_1$ 's parasitic loss  $R_1=\gamma R_t$ , then the modified voltage gain  $A'_V$  and power transfer efficiency  $\eta'_P$  are given by

$$A'_V = \frac{\omega M}{R_r} \cdot \frac{\alpha}{(1 + \gamma + \beta)m + \alpha/m} \cdot Q_L$$
(2.9)

$$\eta_P' = \frac{\alpha\beta}{(1+\gamma)(1+\gamma+\beta)m^2 + \alpha^2/m^2 + (2+2\gamma+\beta)\alpha}$$
(2.10)

To compare the performance of two matching strategies, we define two figure-of-merits (FOMs)



Figure 2.4 Improving factors of (a) voltage gain  $f_V$  and (b) power transfer efficiency  $f_P$  v.s. the multiplication of  $Q_L$ .

 $f_V$  and  $f_P$  as

$$f_V = \frac{A'_V}{A_V} = \frac{1 + \beta + \alpha}{(1 + \gamma + \beta)m + \alpha/m}$$
(2.11)

$$f_P = \frac{\eta'_P}{\eta_P} = \frac{(1+\alpha)(1+\beta+\alpha)}{(1+\gamma)(1+\gamma+\beta)m^2 + \alpha^2/m^2 + (2+2\gamma+\beta)\alpha}$$
(2.12)

It is easily shown that when  $m_V = \sqrt{\frac{\alpha}{1+\gamma+\beta}}$ ,

$$f_{V,max} = \frac{1+\beta+\alpha}{2\sqrt{\alpha(1+\gamma+\beta)}} \approx \frac{1}{2}\sqrt{\frac{\alpha}{1+\gamma+\beta}} = \frac{1}{2}m_V$$
(2.13)

and when  $m_P = \sqrt[4]{\frac{\alpha^2}{(1+\gamma)(1+\gamma+\beta)}},$  $f_{P,max} = \frac{1+\alpha}{\alpha} \cdot \frac{1+\beta+\alpha}{(\sqrt{1+\gamma}+\sqrt{1+\gamma+\beta})^2} \approx \frac{\alpha}{(\sqrt{1+\gamma}+\sqrt{1+\gamma+\beta})^2}$ (2.14)

To estimate  $f_V$  and  $f_P$  as a function of m, the coupling coefficient k is set to be 0.01 and  $Q_t=Q_r=150$ ,  $Q_L=5$ , which are the same parameters used in the measurements. However, the value of  $\gamma$  is difficult to obtain, so we have to estimate it according to:  $\gamma=Q_t/(mQ_{L_1})$ , if  $10 \ge m \ge 1$  and  $Q_t=150$ , then  $150/\gamma \ge Q_{L_1} \ge 15/\gamma$ . Thus we can use different  $\gamma$  to model  $Q_{L_1}$ : ultra high-Q ( $\gamma=0.1$ ,



Figure 2.5 Experimental setup used for powering distance evaluation.

 $1500 \ge Q_{L_1} \ge 150$ ), moderate high-Q ( $\gamma$ =1,  $150 \ge Q_{L_1} \ge 15$ ) and low-Q ( $\gamma$ =10,  $15 \ge Q_{L_1} \ge 1.5$ ). The Q-factor of small value SMD inductor around 13.56MHz is about 25~50, thus the assumption of  $\gamma$ =1 is more reasonable. From the results shown in Fig. 2.4, it is noted that both of  $f_V$  and  $f_P$  first increase with m and reach a maximum. Then, both  $f_V$  and  $f_P$  decrease because larger m results in smaller equivalent  $R_{Ls}$  and hence most of the induced voltage and power are consumed by the parasitic loss  $R_t$  and  $R_1$ . It can also be seen that it is difficult to improve the efficiency if low-Q inductor is used. Fig. 2.3 (c) shows the benefits of the proposed matching strategy, which uses a large coil  $L_t$  to improve the coupling coefficient k and small  $L_1$  instead of  $L_t$  to increase the load qualify factor  $Q_L = R_L/(\omega L_1)$ . Consequently, the constraint imposed by  $L_t$  in parallel matching is able to be released in this proposed matching strategy and thus the efficiency of the inductive link is significantly improved.

### 2.4 Measurement Results

The performance of the proposed matching strategy has been verified using the experimental setup shown in Fig. 2.5, in which the 13.56 MHz reader and the sensor are separated by an adjustable distance. The reader and the sensor coils have been fabricated on a planar PCB and the specifica-



Figure 2.6 Comparison of the voltage generated across a constant load using parallel and proposed matching.

tions of the respective coils are summarized in Table. 5.2. The reader coil is driven by TI TRF7960 chipset [18], whose maximum output power is set to 200mW. For this work we use a conventional Schottky-based Dickson voltage multiplier as the front-end circuit. To compare the performance of the proposed matching network, a conventional parallel matching network is used as a benchmark. At 13.56MHz, the input impedance of the sensor is measured to be  $C_L$ =56pF in parallel with  $R_L$ =350 $\Omega$ . The inductance  $L_t$  of the transponder coil is 0.84 $\mu$ H and the theoretical  $C_{Lp}$ =164pF. For parallel matching,  $C_P$  is set to 110pF; for proposed matching, from Fig. 2.4, it is seen that both of  $f_V$  and  $f_P$  have a distinct improvement within the range of  $m\approx 3\sim 5$ , thus  $L_1$  is chosen to be 0.18 $\mu$ H ( $m=L_t/L_1\approx 4.7$ ) while  $C_2$ =166pF and  $C_1$ =783pF, respectively.

In the first set of experiments, a resistor  $R_L=350\Omega$  and capacitor  $C_L=56\text{pF}$  (equal to the input impedance of the sensor) were chosen as the static load for the parallel and the proposed matching network. The measured results are shown in Fig. 2.6, which plots the voltage across the load with respect to the distance  $D_{rs}$  between the reader and the sensor. The results show that given a fixed  $D_{rs}$  the boosted voltage in the proposed approach is double that of the parallel matching approach. Also note that the threshold of the Schottky multiplier ( $V_L=V_{ON} \approx 300\text{mV}$ ) is reached at respective



Figure 2.7 Comparison of the voltage generated by Schottky-multiplier using the parallel and the proposed matching: (a) 18-stage multiplier used for analog VDD; (b) 12-stage multiplier used for digital VDD.

Parameters	Reader	Transponder
Turns N	4	3
Outer length <i>a</i> (cm)	12.6	10.7
Outer width <i>b</i> (cm)	7.8	1.4
Trace width <i>w</i> (mm)	1.27	1.27
Trace space <i>s</i> (mm)	0.5	0.25
Trace thickness $t$ ( $\mu$ m)	35	35
Self-inductance $L(\mu H)$	5.6	0.84
Unloaded Q	150	150

Table 2.1 Coil specifications.

distances of 13cm for the parallel matching and 17cm for the proposed approach.

For the second set of experiments, the fixed impedance was replaced by the Schottky voltage multipliers. The results of an 18-stage multiplier in this experiment are shown in Fig. 2.7 (a) where the inset shows the same response in logarithmic scale. These results again show that the proposed approach can significantly boost the voltage compared to the conventional parallel matching. Note that the maximum output voltage of the Schottky multiplier is limited by the over-voltage protection diodes integrated on the sensor IC. Fig. 2.7 (b) compares the measured

response obtained from a 12-stage multiplier, and shows that the improvement in voltage-boosting and hence the powering distance can still be achieved for the proposed matching. Therefore, it is concluded that the proposed matching strategy can significantly improve the link performance.

### 2.5 Summary

The power matching network between the transponder coil and the voltage rectifier is necessary for wireless power transfer (WPT) system. It is shown [19] that the WPT system's PCE is heavily determined by: (1) the coupling coefficient k between the reader coil and the transponder coil; (2) the quality-factors of their corresponding matching networks. In most actual applications, the dimension of the transponder coil is usually constrained; furthermore, misalignment between these two coils always happens. Thus the coupling coefficient could be so weak that the power propagation range is very limited.

To compensate such weakly coupled link and the degeneration of the Q-factor, a high-Q matching network is desirable and the communication bandwidth can be traded-off if the throughput is not high. It is well known that the coupling coefficient is proportional to the coil inductance. However, in traditional parallel matching network, the coil inductance is inversely proportional to the Q-factor, thus small coil inductance results in high Q-factor but week coupling coefficient which is unwanted in WPT system. To release the constrain between the Q-factor and k, this chapter proposes a novel series matching network which uses large coil to improve k and small series inductor to boost Q-factor. The boosted AC voltage has another benefit that can overcome the dead-zone of the rectifier to improve the power conversion efficiency (PCE).

#### **CHAPTER 3**

### HYBRID RECTIFICATION TECHNIQUE FOR RF ENERGY HARVESTING

## 3.1 Introduction

The previous chapter illustrates the importance of the impedance matching network in the wireless energy harvesting system. Besides the impedance matching network, the RF rectifier or voltage multiplier also plays an important role in efficiency improvement. The key parameter that affects the performance of any rectifier is the threshold-voltage of the rectifying device that sets the lower-limit on the amplitude of the input RF signal at which the rectifier can start harvesting energy. That is to say, if the input RF signal is below the threshold voltage, the power conversion efficiency of the rectifier is nearly zero. Thus the minimum energy that is able to be harvested depends on the rectifier's threshold voltage. To push the limit of the start up energy, this chapter proposes a hybrid rectification technique which utilizes both of RF power and vibration power to efficiently harvest the energy below the threshold level. Firstly, the voltage conversion efficiency (VCE) and power conversion efficiency (PCE) of the conventional rectifier are analyzed and discussed. Then several state-of-art rectifiers are presented to prove that the limitation is not completed solved. Finally the hybrid PZT assisted RF rectifier is proposed to address this limitation.

# 3.2 VCE and PCE of The Conventional Voltage Rectifier

Voltage rectifier is also named AC-DC converter. A typical conventional half-wave voltage rectifier is shown in Fig. 3.1 (a) with the load capacitor  $C_L$  and load current  $I_L$ . The pass transistor  $M_P$  is implemented in PMOS to avoid the body-bias issue in the standard single well CMOS process when cascading multiple stages.

As shown in Fig. 3.2, when the input RF voltage  $V_{RF}$  is above the output DC voltage  $V_{OUT}$ , the transistor is forward biased. Depending on the relationship between  $V_{RF}$  and  $V_{OUT}$ , the transistor



Figure 3.1 Typical half-wave rectifier: (a) conventional; (b) with ideal compensated voltage.

can be either in the saturation region or subthreshold region. If  $V_{sg} < |V_{TH}|$ , the transistor works in subthreshold region where the current is

$$I_{Sub} \approx I_{S}exp(\frac{V_{SG} - |V_{TH}|}{nV_T})(1 - exp(-\frac{V_{SD}}{V_T}))$$
(3.1)

where  $I_S$  and *n* are empirical parameters with  $n \ge 1$ ;  $V_{SG} = V_{SD} = V_{RF} \cos\theta - V_{OUT}$ ,  $V_{TH}$  and  $V_T$  are the threshold voltage and thermal voltage, respectively. To simplify the analysis, the subthreshold current (region 2) can be linearized as

$$I_{Sub} = I_S \frac{\phi_2 - \theta}{\phi_2 - \phi_1} \tag{3.2}$$

where  $\phi_1 = cos^{-1}(\frac{V_{OUT} + |V_{TH}|}{V_{RF}})$  and  $\phi_2 = cos^{-1}(\frac{V_{OUT}}{V_{RF}})$ , are conducting angles for the saturation region and forward biased region, respectively. Similar, the saturation current (region 1) can be linearized as

$$I_{Sat} = I_F - (I_F - I_S)\frac{\theta}{\phi_1}$$
(3.3)

where  $I_F = \frac{1}{2}\mu_P C_{ox}(\frac{W}{L})(V_{RF} - V_{OUT} - |V_{TH}|)^2$  is the maximum saturation current.

When the input RF voltage  $V_{RF}$  is below the output DC voltage  $V_{OUT}$ , the transistor is reverse biased with  $V_{sg} = 0$ , which indicates the reverse leakage current is in the subthreshold region but with zero source to gate voltage,

$$I_{Rev} \approx I_S exp(-\frac{|V_{TH}|}{nV_T})(1 - exp(-\frac{V_{SD}}{V_T}))$$
(3.4)



Figure 3.2 Voltage and current waveform of the pass transistor  $M_P$ .

The linearization method is still applicable to the reverse leakage current (region 3) as

$$I_{Rev} = I_R \frac{\theta - \phi_2}{\pi - \phi_2} \tag{3.5}$$

where  $I_R = I_S exp(-\frac{|V_{TH}|}{nV_T})$  is the maximum leakage current at which  $V_{SD} = V_{OUT} + V_{RF} \ge 3V_T$  so that the effect of  $V_{SD}$  can be ignored. After linearizing the currents, the charges in different regions can be easily calculated, thus in one period

$$Q_{Sat} = (I_F + I_S)\phi_1 \tag{3.6}$$

$$Q_{Sub} = I_S(\phi_2 - \phi_1)$$
 (3.7)

$$Q_{Rev} = I_R(\pi - \phi_2) \tag{3.8}$$

In steady state, according to the charge conservation  $Q_{Sat} + Q_{Sub} = Q_{Rev} + Q_L$ , which can be

extended by

$$(I_F + I_S)\phi_1 + I_S(\phi_2 - \phi_1) = I_R(\pi - \phi_2) + 2\pi I_L$$
(3.9)

Using Taylor series expansion  $cos^{-1}\theta \approx \pi/2 - \theta$  for  $\phi_1$  and  $\phi_2$ , the voltage conversion efficiency (VCE) can be estimated by

$$\frac{V_{OUT}}{V_{RF}} = \frac{\pi}{2} - \frac{I_F}{I_F + I_S + I_R} \cdot \frac{|V_{TH}|}{V_{RF}} - \pi \frac{I_R + 2I_L}{I_F + I_S + I_R}$$
(3.10)

The power conversion efficiency is defined as

$$PCE = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}}$$
(3.11)

where  $P_{OUT} = V_{OUT}I_L$ , is output power of the rectifier.  $P_{LOSS}$  is power consumption of the pass transistor and can be estimated by

$$P_{LOSS} \approx P_{forward} + P_{reverse}$$

$$\approx \frac{1}{\pi} \left( \int_{0}^{\phi_{1}} I_{Sat} V_{SD} d\theta + \int_{\phi_{1}}^{\phi_{2}} I_{Sub} V_{SD} d\theta + \int_{\phi_{2}}^{\phi_{2}} I_{Rev} V_{SD} d\theta \right)$$

$$(3.12)$$

with

$$\int_{0}^{\phi_{1}} I_{Sat} V_{SD} d\theta 
= \int_{0}^{\phi_{1}} (I_{F} - (I_{F} - I_{S}) \frac{\theta}{\phi_{1}}) \cdot V_{RF}(\cos\theta - \cos\phi_{2}) d\theta$$
(3.13)  

$$= V_{RF} I_{F} \phi_{1} \sin^{2} \frac{\phi_{2}}{2} + V_{RF} I_{S}(\sin\phi_{1} - \phi_{1} \cos^{2} \frac{\phi_{2}}{2}) 
\int_{\phi_{1}}^{\phi_{2}} I_{Sub} V_{SD} d\theta 
= \int_{\phi_{1}}^{\phi_{2}} I_{S} \frac{\phi_{2} - \theta}{\phi_{2} - \phi_{1}} \cdot V_{RF}(\cos\theta - \cos\phi_{2}) d\theta$$
(3.14)  

$$= V_{RF} I_{S} (\frac{\phi_{1} + \phi_{2}}{2} - \sin\phi_{1} - \frac{\phi_{2} - \phi_{1}}{2} \cos\phi_{2}) 
\int_{\phi_{2}}^{\pi} I_{Rev} V_{SD} d\theta 
= \int_{\phi_{2}}^{\pi} I_{R} \frac{\theta - \phi_{2}}{\pi - \phi_{2}} \cdot V_{RF}(\cos\phi_{2} - \cos\theta) d\theta$$
(3.15)  

$$= V_{RF} I_{R} (1 + \frac{2 + \pi - \phi_{2}}{2} \cos\phi_{2})$$
### 3.3 State-of-Art Rectifiers

In order to overcome the limitations due to the  $V_{th}$  and to improve the PCE, several passive and active rectifier topologies have been reported in literature [14,15,20–23]. In this part some of these state-of-art techniques are examined.

#### 3.3.1 Passive Rectifiers

Many techniques have been proposed to generate the compensation voltage for passive rectifiers. The most popular one is the differential-driven cross-coupled rectifier, which actively biases the gate of the transistor with positive and negative RF signal, as shown in Fig. 3.3 (a). Due to simple and robust structure, this technique is widely used in UHF energy harvesting applications, however it also needs the start-up voltage above the threshold voltage to turn on NMOS or PMOS at the initial stage.

Another method shown in Fig. 3.3 (b) is to use pseudo floating gate device which actually connects the gate of the diode-tied transistor and the gate of the MOS capacitor to form a high-impedance node to trap charge on the floating gate. The charge on the floating gate is therefore fixed which results in a fixed voltage bias across the MOS capacitor. The charges that are trapped inside the floating gate device act as a gate-source bias to passively reduce the effective threshold voltage of the transistor. Although the circuit structure using pseudo floating gate is not complex, it requires initial programming on each floating gate before working, and the amount of charge is hard to control, and additional circuitry is needed to inject or remove charge from the floating gate.

The method shown in Fig. 3.3 (c) is called internal threshold cancellation, in which the capacitor  $C_{BP}$  holds the thresholds voltage of the MOS diode  $M_{P1}$  by replicating its threshold voltage with  $M_{PB}$ . Another equivalent circuit is applied to the MOS diode  $M_{N2}$ . This equivalent circuit can accurately track the process and temperature variation in these diodes by matching  $M_{PB}$  to  $M_{P1}$ and  $M_{NB}$  to  $M_{N2}$ . In addition, the leakage currents of all diodes are minimized by the large bias resistor Rb. Actually the internal threshold cancellation technique needs sufficiently large input to



Figure 3.3 Three popular passive rectifiers: (a) Differential cross-coupled rectifier [4]; (b) Pseudo floating gate rectifier [5]; (c) Internal  $V_{TH}$  cancellation rectifier [6].

start up the circuit and the bias resistor  $R_B$  that is around the M $\Omega$  range is a large value.

Due to the simple circuit architecture, the passive rectifiers can work in ultra high frequency with low start-up power, so it is suitable for long distance application. However, the power transfer efficiency is low and sometimes special process is needed to improve the efficiency.

### 3.3.2 Active Rectifiers

The other kind of rectifier is active rectifier which replaces diode with actively controlled switch to improve the efficiency. The switch usually implemented in MOSFET which has very low resistance when conducting. As shown in Fig. 3.4 (a), the control circuit for active rectification usually uses comparator to sense the AC input and open the transistor at the correct time to allow the



Figure 3.4 (a) Comparator based active diode [7]; (b) Offset control high efficiency active rectifier [8]; (c) Illustration of leakage current issue in active rectifier [8].

current to flow in the correct direction. So it can obtain high power conversion efficiency with high conducting current. However, the comparator has a trade off between the speed and power, so it is very difficult to achieve fast response with little power. In addition, the switch is usually implemented in large size for low on-resistance so that its gate capacitance could be very large and the comparator needs strong driving capability which is also very difficult to achieve under low power condition. So the active rectifier is difficult to operate in at ultra high frequencies where the available power is very limited. Another issue that cannot be neglected for an active rectifier is the timing. Due to the offset and propagation delay of the comparator, the switch cannot be completed turned off when the input AC signal is lower than the output DC voltage (shown in Fig. 3.4 (b) and (c)), causing the reverse leakage current to conduct so that the efficiency is decreased.



Figure 3.5 Conceptual hybrid rectifer [9].

# 3.4 Proposed PZT Assisted RF Rectifier

Based the analysis above, it can be seen that all of the existing methods without special processes still require the input amplitude to be at least equal to the  $V_{TH}$  of the MOSFET, although they can achieve excellent power conversion efficiency. To overcome the threshold-voltage input amplitude limitation, we propose a solution by using hybrid rectification technique. The technique relies on the fact that most energy-scavenging sensors operate in an environment where multiple sources of power could be available. Typically, the energy from each signal source could be harvested using a separate rectifier operating independently, as shown in Fig. 3.5(a). Their outputs could then be combined in series to boost the output voltage. This approach, however, requires that each energy source has similar electrical driving capability which is determined by the frequency f,



Figure 3.6 The concept of a hybrid voltage-multiplier and its potential application to a structural health monitoring sensor that scavenges RF and vibration energy.

the amplitude V and the output impedance Z of the source, which might not be possible when the physics and efficiency of energy transduction for different energy sources are dissimilar.

An example of a sensor with multiple power sources is an RF identification (RFID) sensor that is attached to a mechanical structure [15] where one of the sources of energy could be ambient vibration in addition to the RF signal used for powering and interrogation of the sensor as shown in Fig.3.6. The energy that could be harvested from the ambient vibration might be much lower than the energy that could be harvested from the RF source. Also, a piezoelectric transducer used for vibration energy scavenging is purely capacitive with very limited current-driving capability, whereas a near-field electromagnetic transducer (for scavenging RF signals) is purely inductive with a limited voltage-driving capability. In such cases, a hybrid rectifier design (as shown in Fig. 3.5(b)) offers a solution that can exploit the electrical properties (f,V,Z) of the sources in conjunction with each other and not independent of each other. For example, due to their capacitive nature piezoelectric transducers can generate large open-load voltages and therefore could be used for biasing the gates of the MOSFETs in the rectifier. This in turn could reduce the minimum amplitude requirements on the incident RF signal. This would then imply that a smaller size inductor coil could be used for bio-telemetry applications or in the case of a far-field RFID sensor, the powering-distance of the sensor could be significantly increased.



Figure 3.7 Complementary cross-coupled rectifier.

Therefore I will present a novel rectifier structure which uses a purely capacitive, high amplitude and low frequency piezo signal to boost the DC component of the AC controlled gate voltage of rectifying transistors.

## 3.4.1 Threshold Compensation Investigation

At a low input RF signal level, complimentary cross-coupled rectifier(CCCR) cell as shown in Fig. 3.7 is preferred because it can achieve highest power conversion efficiency thanks to differentially dynamic bias scheme [21]. The gate-to-source voltage of PMOS(NMOS) device  $V_{GP}(V_{GN})$  is determined as

$$V_{GP} = V_{RF} \frac{C_C}{C_C + C_{par}} \tag{3.16}$$

where  $C_{par}$  is the total parasitics capacitance of PMOS and proportional to the size of the transistor(Width× Length).  $V_{GP}$  needs to be larger than  $V_{th}$  to turn on the devices in the rectifier. Several stages can be cascaded to generate a sufficiently high DC output voltage ( $V_{DC}$ ). The number of stages (N) is determine as

$$N = \frac{V_{DC}}{V_{out}} \tag{3.17}$$



Figure 3.8 DC boosting effect simulation setup ( $V_{RF}$ =0.3  $V_{pk-pk}$ ,  $f_{RF}$ =13.56 MHz,  $R_L$ =20 K $\Omega$ ,  $C_L$ =1 nF).



Figure 3.9 Optimal bias voltages versus input RF signal.

To overcome the threshold limit of the CMOS devices at low RF input amplitude range, the DC components of their gate voltages need to be compensated i.e biasing a positive DC level for the NMOSs and a negative DC level for the PMOSs. An investigation of DC biasing effect is performed with a CCCR is shown in Fig. 3.8(a).

Fig. 3.8(b) shows an example of the DC output voltage versus DC bias levels when  $V_{RF}$ =300 m $V_{pk-pk}$  and  $f_{RF}$ =13.56 MHz. It reveals an optimal DC biasing voltage pair for NMOSs and

PMOSs ( $V_{BN}$ =500 mV,  $V_{BP}$ =-500 mV) for a peak DC output voltage of 180 mV. When the DC biasing levels go beyond the optimal values, the DC output voltage decreases gradually. This is because when the biasing level increases, the reverse drain current increases faster than the forward drain current since the transistors enters triode region in the conduction period at large DC bias levels. This effect worsens the rectifying behavior of the rectifier. This behavior is well-known and analyzed in previous reports [4, 22]. A set of simulation runs are performed for a wide range of  $V_{RF}$  to find the optimal biasing levels and the result is shown in Fig. 3.9. It is clear to see that DC bias voltages decreases with the increase of RF amplitude.

#### 3.4.2 Circuit Implementation

To generate the DC bias, the piezoelectric signal can be taken into consideration since its available frequency response usually falls below 10 kHz, which thus can be considered as a DC signal with respect to RF signal. Another consideration to use PZT signal is low power consumption since it only requires very little power to drive the gate of rectifier device. Therefore, based on the different physical properties of the PZT signal and RF signal, we propose a HR in which the gates of the rectifier device are not biased by the RF signal but by the clamped piezoelectric signals. The CCCR structure has been extended here by adding an appropriate DC bias to enable it to work at extremely low input RF signal levels.

A pair of biasing voltage generators (Fig. 3.10 (b) and (c)) generate the gate biasing voltages for the NMOS and PMOS devices respectively. The NMOS biasing voltage generator (Fig. 3.10 (b)) consists of two symmetrical branches that generate the two 180<sup>o</sup> phase shifted biasing voltages  $V_{GN+}$  and  $V_{GN-}$  for the cross coupled NMOS transistors in Fig. 3.10 (b). For simplicity, only upper branch is considered. The RF input  $V_{RF+}$  provides the AC component analogous to the main rectifier circuit (Fig. 3.10 (a)). The PZT signal  $V_{PZ+}$  is first bounded in its amplitude to the gate to source voltage  $V_{GS}$  of the vertical diode connected PMOS and the PN junction between bulk and the lower S/D terminal that forms a bipolar diode in parallel pointing the other way  $P_{1N}$  (a PMOS configuration known as Tobi-element [24]). Then the resultant voltages  $V_{PZN+}$  is



Figure 3.10 Proposed HR: (a) main rectifier; (b) DC bias generator for NMOS gate terminals and (c) for PMOS gate terminals.

rectified by the horizontal diode-connected PMOS  $P_{2N}$  to provide the DC bias level to  $V_{GN+}$ . In other words, the low frequency clipped PZT signals  $V_{PZN+}$  is superimposed with the RF signal. This DC boosted RF signal is then used to synchronously drive the gates of the CCCR, instead of directly using the incident RF signals, i.e. the RF amplitude no longer need to be larger than  $V_{th}$ as in the CCCR. The lower symmetrical branch and the branches in Fig. 3.10 (d) generating the biasing voltages  $V_{GP+}$  and  $V_{GP-}$  for the rectifying PMOSs operate analogously.

Fig.3.11 shows some of the relevant simulated waveforms from the biasing generators. As intended, the extremes of  $V_{PZN+}$  and  $V_{PZP+}$  are bounded due to Tobi-elements( $P_{1N,1P}$ ) in the first stage of bias generators. The  $V_{GS}$  of the  $P_{1N,1P}$  and the  $V_{th}$  of of bulk-S/D P-N diode determines



Figure 3.11 Simulated waveform of critical nodes in bias voltage generators.  $F_{piezo}$ =10 KHz,  $V_{piezo}$ =1 V,  $F_{RF}$ =13.56 MHz,  $V_{RF}$ =0.3  $V_{pk-pk}$ .

the positive and negative bounding limits, respectively. This  $V_{GS}$  is depended on the size of the  $P_{1N,1P}$  and can be adjusted to the optimal value, making the rectifier able to harvest RF energy efficiently at ultra low RF amplitudes.

#### **3.4.3** Device Size Analysis and Optimization

The width(W) and length(L) of MOS devices are the design constrains of loading condition and PCE while the chip area is mainly determined by the coupling capacitor  $C_C$  value. The number of stage N in the rectifier needs to be minimal to achieve higher peak PCE since the body effect in multistage topology increases  $V_{TH}$  of NMOSs in the last stages [25]. Therefore, the output voltage is maximized throughout following optimized sizing analysis. For drain current matching between NMOS and PMOS, the aspect ratio  $(W/L)_{PMOS}=2(W/L)_{NMOS}$  are chosen. Assume that 1 V DC output voltage and 10  $\mu$ A output current at 300 m $V_{pk-pk}$  RF voltage and a 10 KHz PZT are the design target.

For  $C_C=10$  pF, the DC output voltage of one stage rectifier as a function of device sizes is shown in Fig.3.12. When the transistor size increases, the conductive strength of the transistor increases in accordance with the increase of  $C_{par}$  which reduces the effective  $V_{GP}$  and  $V_{GN}$  as



Figure 3.12  $V_{OUT}$  versus device size of the main rectifier ( $V_{RF}$ =0.3  $V_{pk-pk}$ , L= 0.1  $\mu$ m,  $C_C$ =10 pF and  $I_{OUT}$  = 10 $\mu$  A).



Figure 3.13 Equivalent circuit of the upper branch of NMOS bias generator.

stated in Eq.3.16. Therefore, there exists an maximal  $V_{out} = 200 \text{ mV}$  at an optimal W/L=100.

In addition, the size of the devices in the bias generator should also be optimized. Consider the upper branch of a NMOS bias generator as shown in Fig.3.13.  $C_{Par}$  is the total parasitics capacitor to ground at note  $V_{GN+}$  which is the total parasitics capacitance of  $P_{2N}$  and NMOS in the main rectifier. In the initial state, a part of current from PZT signal ( $I_{P2N}$ ) is rectified through  $P_{2N}$  to charge to the parasitics capacitor  $C_{Par2}$  to increase the DC component of  $V_{GN+}$ . At the steady state, where the DC component of  $V_{GN+}$  reaches to approximately positive clipped PZT voltage

 $V_{PZN+}$ , most current from PZT signal  $I_{PZT}$  flows into diode-connected  $P_{P1N}$  i.e  $I_{PZT} \simeq I_{P1N}$ . The current  $I_{P1N}$  is model as [26]

$$I_{P1N} = \begin{cases} I_{so} \cdot \frac{W}{L} \cdot e^{\frac{V_{gs}}{nV_T}} (1 - e^{\frac{-V_{ds}}{V_T}}) & V_{gs} < V_{th} \\ \beta \cdot \frac{W}{L} (V_{gs} - V_{th})^2 & V_{gs} \ge V_{th} \end{cases}$$
(3.18)

where  $I_{so}$  is the subthreshold unit current, n is the subthreshold region swing parameter,  $V_T$  is the thermal voltage(typically is 26 mV at 27<sup>o</sup>C) and  $\beta$  is process constant. Because  $P_{1N}$  is connected as a diode,  $V_{ds} = V_{gs} = V_{PZN+}$  of which amplitude is in a range of 300-800 mV, much larger than  $V_T$ . Therefore, Eq. 3.18 is rewritten as

$$I_{P1N} = \begin{cases} I_{so} \cdot \frac{W}{L} \cdot e^{\frac{V_{PZN+}}{nV_T}} & V_{PZN+} < V_{th} \\ \beta \cdot \frac{W}{L} (V_{PZN+} - V_{th})^2 & V_{PZN+} \ge V_{th} \end{cases}$$
(3.19)

Since PZT current  $I_{PZT}$  is calculated as

$$I_{PZT} = C_P \cdot V_{PZT} \cdot 2 \cdot \pi \cdot f_{PZT} \tag{3.20}$$

where  $V_{PZT}$  and  $f_{PZT}$  are voltage amplitude and frequency of PZT signal. From (3.19) and (3.20),  $I_{PZT} \simeq I_{P1N}$ , the amplitude of  $V_{PZN+}$  can be solved

$$V_{PZN+} = \begin{cases} n.V_T.ln(\frac{C_P.V_{PZT}.2.\pi.f_{PZT}}{I_{so}.\frac{W}{L}}) & V_{PZN+} < V_{th} \\ \sqrt{\frac{C_P.V_{PZT}.2.\pi.f_{PZT}}{\beta.\frac{W}{L}}} + V_{th} & V_{PZN+} \ge V_{th} \end{cases}$$
(3.21)

It can be seen from (3.21) that the amplitude of  $V_{PZN+}$  is depended on both PZT electrical properties (voltage amplitude and frequency), PZT coupling capacitor  $C_P$  and the size of transistor  $P_{1N}(W/L)$ . This voltage amplitude determines the DC bias level of NMOS gate voltage  $V_{GN+}$ , thereby affecting to the output voltage generated by the main rectifier as analyzed part II. Since the current  $I_{P2N}$  is very small, the voltage dropping on diode  $P_{2N}$  can be negligible. With  $V_{BN,opt}$  is the optimal DC bias voltage for NMOSs, the optimal amplitude of  $V_{PZN+} \simeq V_{BN,opt}$ .

Therefore from Eq.(3.21), we can find the optimal value pair (W/L and  $C_P$ ) for each bias generator branch at a given PZT source. For example, at 0.3 V RF voltage,  $V_{BN+,opt}$ =0.5 V as



Figure 3.14 Six stage HR.

investigated in part II, and with a PZT source ( $V_{PZT}=2$  V and  $f_{PZT}=10$  kHz), the optimal value pairs can be found as (1.25  $\mu$ m/1  $\mu$ m;0.1 pF), (5  $\mu$ m/1  $\mu$ m;0.4 pF) or (10  $\mu$ m/1  $\mu$ m;1p pF). The diode connected  $P_{2N,2P}$  serves as a rectifier to the clipped PZT signals  $V_{PZN,PZP}$  and can be chosen with a small size. The RF coupling capacitor  $C_{RF}$  needs to be sufficiently large compared with the parasitics capacitance of  $P_{2N,2P}$  to maximize the amplitude of  $V_{GN,GP}$  due to the capacitive voltage divisions as shown in Eq. 3.16. The device size W/L=5  $\mu$ m/0.2  $\mu$ m for  $P_{2N,2P}$  and  $C_{RF}=0.4$  pF are selected.

#### 3.4.4 Measurement Results

With a design target of  $V_{DC}=1$  V and  $I_{OUT}=10 \ \mu$ A, a six stage HR as shown in Fig.3.14 along with a six stage CCCR for comparison are implemented on the same die in a 90 nm CMOS process. Fig.3.15 shows the chip micrograph of both rectifiers. The active silicon area of the two rectifiers have the same size of approximately 0.137  $mm^2(550 \ \mu\text{m} \times 250 \ \mu\text{m})$ . This is because the coupling capacitors  $C_C$  are implemented by metal-in-metal(MIM) caps and span mostly the area of the rectifiers, the bias generators in HR contribute ignorably additional silicon area. The test chip was implemented with an ESD protection circuit. This would degrade the performance of the rectifiers, however the two rectifiers are put under the same condition and the performance comparison is still rational. A impedance matching network can be designed to improve the total performance of both two rectifiers, but designing a matching network is out of the scope of this paper.



Figure 3.15 Micrograph of voltage multiplier chip.

The measurement setup for the chip test is shown in Fig. 3.16. A single-ended RF signal from a signal generator is converted into differential signal by using a transformer balun CX2147 with insertion loss of 0.3 dB. To emulate the differential piezoelectric signal, signals from two channels of TGA1421 are synchronized with a phase shift of  $180^{\circ}$ . These output signals are connected in series with big resisters of 1 M $\Omega$  to limit the output current flowing into the circuit. To measure the input current of the RF signals, two small resistors of  $100\Omega$  are connected in series with the balun and the input current is calculated by measuring differential voltage at two points X and Y [27]. Since the measuring probe has a loading capacitor  $C_{probe}$  of 15 pF, the intrinsic current flowing into the chip is calculated as

$$I_{INintr} = I_{IN} - I_{probe}$$
  
=  $\frac{V_{XY}}{R_{sens}} - V_{rms,XX'} \times (2.\pi.f_{RF}.C_{probe})$  (3.22)

where  $I_{intr}$  is the intrinsic input current flowing into the chip and  $f_{RF}$  is the RF frequency. The input power is calculated through the intrinsic input current and input voltage. The input RF power



Figure 3.16 Measurement setup of the test chip.

and PZT power are calculated as

$$P_{RF,IN} = \int_0^T I_{IN,intr} \times V_{rms,XX'} dx$$
(3.23)

$$P_{PZT} = N.2.V_{PZT}^2 .2.\pi.f_{PZT}.C_P$$
(3.24)

with N is the number of stages of the rectifier. The output power is calculated through DC output voltage and loading resistor  $R_L$ . The PCE is calculated as

$$PCE = \frac{P_{OUT}}{P_{IN}} = \frac{V_{DC}^2 \times R_L}{P_{RF,IN} + P_{PZT}}$$
(3.25)

Fig. 3.17 shows the function of DC output voltage versus input RF voltage at different loading conditions. It is worth noting that the parasitic inductor and capacitor of the package and bonding wire do cause a distortion for the input RF voltage and the DC output voltage. Therefore, a better intrinsic performance can be predicted. In this measurement setup, the pseudo PZT signals are kept at amplitude of 2 V and a frequency of 10 kHz. The intrinsic input power of the pseudo PZT signal is calculated at 1.2  $\mu$ W(-29.2 dBm).

It is clear to see that the HR has deadzone free and is able to harvest power at ultra low input voltage from 100 mV. On the other hand, the deadzone exists in the CCCR and limits its ability



Figure 3.17 DC output voltage vesus input RF voltage.

to harvest power at a RF input voltage amplitude higher than  $V_{TH}$  (around 0.5 V) of the CMOS devices. For example, at 300 mV input voltage with the loading resister of 330 K $\Omega$ , the HBR can generate an DC voltage of 1V while the CCCR is almost silent and can only generate the same DC voltage level at the input voltage of 650 mV. This output power level(3  $\mu$ W) can be sufficient for some subthreshold mixed signal blocks which are widely used in sensor applications.

When CCCR turns on, its DC output voltage increases at a faster rate and overcomes the HR at large input voltage levels. The reason is that DC bias levels in bias generator are constant with the RF amplitude while the higher the RF input voltage level, the lower the optimal DC bias levels for maximal output voltage. However this performance degeneration at high input RF levels is less significant because a sensor system needs only a supply voltage of 1.2 V for normal operations (in 90 nm CMOS technology). In addition, providing too large DC supply voltage at large RF input signal will decrease the power efficiency of the telemetry sensor system.

Fig. 3.18 shows the PCE of the two rectifiers at different loading resistors when the RF frequency and pseudo PZT signal are kept constant. We can see that the HR outperforms the CCCR in low input power range. At 100 k $\Omega$  loading resistor and -12.9 dBm input power, the PCE of the CCR is only 9.7 % while it is for HR four times larger with 40.3 %. The PCE of the HR achieves



Figure 3.18 Comparison of measured PCE versus input power  $P_{IN}$  ( $f_{RF} = 13.56$  MHz,  $F_{PZT} = 10$  kHz and  $V_{PZT} = 2$  V).

a peak value before it decreases at higher input power levels.

The peak value of PCEs increases with the decrease of loading resistor value. It means that the HR works more effectively at larger loading current condition. It is because the rectifying transistors are sized at high aspect ratio (W/L), hence, they are more effective in generating larger currents. However, compared with the CCCR, the peak PCE of the HR becomes higher than the peak PCE of CCR when  $R_L$  gets larger. With  $R_L$  is 680 K $\Omega$ , for instance, the peak PCE of the HR is 14.36 % at -14.6 dBm input power while the peak PCE of the CCR is 13.67 % at -6.5 dBm input power. It is also noted that when loading resistor increases, the PCE curve of the HBR moves toward to the small input power region and the HR can start harvesting power at smaller input power level.

Another set of experiments with a fixed RF signal and varying amplitude and frequency of the



Figure 3.19 DC output voltage of the HR verse PZT input amplitude at different PZT frequency ( $V_{RF,pk-pk}$ =300 mV,  $F_{RF}$  13.56 MHz and  $R_L$ =330 K $\Omega$ ).

PZT signal are conducted. Fig. 3.19 shows the dependency of the DC output voltage on  $V_{PZT}$  and  $f_{PZT}$ . The DC bias of the hybrid VM may not be properly generated if the PZT amplitude is too small. It is clear to see that the DC output voltage increases with increasing amplitude of  $V_{PZT}$  up to an optimal value. This optimal  $V_{PZT}$  value decreases with the increase of  $f_{PZT}$ . Thereafter, it decreases gradually with the increase of the PZT's amplitude. This phenomenon because the DC boosting level of the gate control signals increases with the PZT amplitude. This, in turn, increases the reverse current and lowers the DC output voltage.

Another behavior of the HR is that the maximal DC output voltage of the HR decreases with frequency of PZT. This is because the lower PZT frequency, the larger the drift of the DC level of the gate controlling voltages due to charge leakage into the substrate, thus the lower the maximal DC output voltage.

# 3.5 Summary

This chapter presents a novel CMOS hybrid rectifier that can efficiently scavenge energy from a combination of a radio-frequency (RF) signal and a low-frequency, low-energy signal from a piezoelectric (PZT) transducer. The piezoelectric signal is used for biasing a complimentary crosscoupled rectifier (CCCR) chain to an operating point where the RF signal energy can be efficiently harvested even if its amplitude is well below the threshold voltage ( $V_{th}$ ) of the rectified device. The optimal device sizes have been thoroughly investigated to achieve the maximal DC output voltage. The measurement result shows that the 6-stage hybrid rectifier(HR) can generate a 1 V DC output voltage and a 3  $\mu$ A output current from a combination of a 300 mV peak-to-peak, 13.56 MHz RF signal and a 10 KHz-2 V PZT signal. The proposed HR can effectively eliminate the deadzone and yields a significant improvement in power conversion efficiency (PCE) for low input power as compared to a conventional (CCCR) on the same die in a 90 nm CMOS technology.

#### **CHAPTER 4**

### TIME DILATION TECHNIQUE FOR IMPULSIVE ENERGY HARVESTING

# 4.1 Introduction

In addition to the wireless energy harvesting, the vibration energy is also ubiquitous in the environment. Thus it is a natural source for the energy harvesting devices, especially for the sensors that are attached to or embedded inside the structure. However, different with the wireless energy that is almost constant and continuous, the vibration energy is characterized to be variable and intermittent. In some particular conditions, the vibration caused by the impact could be impulsive so that it is difficult for the harvester to capture the whole energy during short pulse period. In this chapter, a non-linear compressive technique is proposed and the corresponding time-dilation circuit is presented for extending the energy harvesting duration.

Self-powered sensors operate by harvesting energy directly from the signal being sensed [15]. For example, a piezoelectric transducer could be used for sensing vibrations or variations in mechanical strain and the energy in the strain variations could also be used for the computation, data storage and data transmission. One of the challenges in designing self-powered sensors is the threshold effect which limits the sensing, powering and hence the operating range [28]. This operating range (in sensing and powering) is determined by two energy thresholds: (a) minimum energy required to activate the sensor; and (b) maximum energy above which the sensor could incur electrical damage. For example, in head-impact monitoring, presence of these energy thresholds limits the measurement range of impact energy and hence the acceleration levels that could easily exceed 100g [29]. If a piezoelectric transducer (for example, PZT ceramic) is used as a transducer, such high-levels of acceleration could easily produce open-load voltage levels in hundreds of volts. To prevent damage to the sensor, a typical architecture will dissipate most of the impulse energy through the over-voltage protection circuits; and hence the sensor would be unable to accurately measure the magnitude of energy [15]. Another approach is to use a compressive



Figure 4.1 (a) Powering and sensing mechanism of the PFG head-impact monitoring sensor; (b) time-dilation approach where the impact energy is spread in time; and (c) compressive response of a time-dilated impact monitoring sensor.

"shunt" regulator type architecture [28] which dissipates a major fraction of the energy through a resistor and is thus able to compress the input range (as shown in Fig. 4.1(c)) within the minimum and maximum threshold levels. This method ensures that the sensor can be quickly activated by small magnitude impacts, whereas compressive response beyond an energy threshold  $E_{min}$  ensures sensor operation within electronic safety compliance levels. However, the dissipative nature of this approach makes it unsuitable for head-impact monitoring because the duration of the impact is too short (in the order of a few milliseconds) for accurate energy measurement. Therefore, the time-dilation approach is proposed to achieve a compressive response similar to Fig. 4.1(c) and at the same time enable accurate energy measurement. The principle exploits the impulsive nature of head-impacts which occur infrequently, as illustrated in Fig. 4.1(b). The sparsity with respect to time is exploited by the time-dilation approach where the impulsive signal is stretched out in time (as shown in Fig. 4.1(b)) while retaining as much of the energy (area under the curve) as the original impulse. Before the time-dilation circuit is discussed, it's worth to discuss the equivalent circuit model of a piezoelectric transducer which has been used for our simulation studies.



Figure 4.2 (a) Equivalent circuit of the piezoelectric transducer; (b) Simulated pulse response of the piezoelectric transducer with  $1M\Omega$  load.

# 4.2 Modeling of the Piezoelectric Transducer

For this work, a piezoelectric transducer has been used for harvesting impact energy; therefore, any simulation or analysis of the time-dilation based energy measurement has to incorporate an equivalent circuit of the piezoelectric transducer. The most commonly used equivalent circuit model that captures the transient response of a piezoelectric transducer is shown in Fig. 4.2(a). The voltage source  $V_S(\propto F \propto a)$  models the force F applied to the transducer due to the head

Table 4.1 Equivalent circuit parameters used in simulation.

$C_M$	R <sub>M</sub>	$L_M$	N	$C_P$	$R_L$
227.4nF	57.87Ω	1H	0.05417	80.08nF	1MΩ

impact and is proportional to the acceleration *a*. The capacitor  $C_M$  models the mechanical stiffness of the transducer, the resistor  $R_M$  models the mechanical damping, and the inductor  $L_M$  models the mechanical mass. The mechanical domain is coupled to the electrical domain (according the function of the transducer) through a transformer with a turn ratio of *N*. In the electrical domain,  $C_P$ is the equivalent intrinsic capacitance of the transducer and  $R_L$  represents a resistive load connected at the transducer's output terminals. Table. 4.1 [30] list the values of these circuit parameters chosen for the simulation study. The mechanical impact has been modeled as a short-duration pulse whose amplitude is proportional to the applied force. The magnitude of the pulse is also proportional to the acceleration levels and the impact energy. The response of the equivalent circuit of the piezoelectric transducer is simulated as shown in Fig. 4.2(b) for a 75V input pulse with a duration of 1ms. The resonant response of the output is determined by the resonant frequency (product of the equivalent inductance and capacitance) and the decay is determined by the total equivalent resistance. The transducer response and hence the parameters of the equivalent circuit parameters have been verified using measured results as shown in the inset of Fig. 4.2(b) for a load of 1M $\Omega$ .

### 4.3 **Proposed Time-dilation Circuit**

The equivalent circuit of the piezoelectric transducer can be used to study the response of a timedilation circuit shown in Fig. 4.3. For comparison, Fig. 4.3 also shows an equivalent circuit without the time-dilation circuit. In both of the circuits,  $I_L$  models the load current of the sensor,  $C_L$  is the load capacitance, and  $D_L$  represents a zener diode which models the functionality of an overvoltage protection circuit. In practice, the current  $I_L$  is triggered only when the voltage  $V_{OUT}$ 



Figure 4.3 Equivalent circuit of a self-powered sensor: (a) without, and (b) with the time-dilation circuit.

exceeds a minimum threshold level  $V_{MIN}$ . The full-wave rectification is achieved using the diodes  $D_{R1} - D_{R4}$  formed using a bulk-driven cross-coupled pMOS circuit which was reported in [31].

For the circuit without the time-dilation (shown in Fig. 4.3(a)), the rectified current of  $I_P$  increases the voltage  $V_{OUT}$  past the minimum threshold  $V_{MIN}$  which then activates the sensor and hence the current  $I_L$ . If the current  $I_P$  exceeds the sensor current  $I_L$ , the voltage  $V_{OUT}$  will increase until the zener,  $D_L$ , starts drawing the extra current. Thus, for large impulse currents most of the impact energy is dissipated through the zener. The time-dilation circuit shown in Fig. 4.3(b) mitigates this problem in the following manner. Initially, the sensor voltage  $V_{OUT} = 0$  implies that the nMOS transistor  $N_T$  is OFF and hence the storage capacitor  $C_T$  is disconnected. Therefore, during start-up the behavior of circuit in Fig. 4.3(b) is identical to the start-up for the circuit in Fig. 4.3(a). But when the voltage  $V_{OUT}$  exceeds  $KV_{TH}$ , with K being the number of diodes in the chain  $D_1-D_K$  and  $V_{TH}$  being the threshold voltage of the transistor  $N_T$ , the storage capacitor  $C_T$  is connected in parallel with the sensor. Thus, the additional piezoelectric current now charges up the storage capacitor without dissipating energy through the zener. When the impulse subsides (after the impact), the charge stored on the capacitor  $C_T$  drives the sensor current until  $V_{OUT}$  falls below the activation voltage  $V_{MIN}$ . Thus, by using time-dilation circuit, the sensor can more accurately measure the level of impact energy.

Fig. 4.4 compares the simulation results of the output voltage of the full wave rectifier with and without time-dilation circuit for input pulse of magnitudes 100V and 300V, respectively. It is



Figure 4.4 Comparison between the output voltages of the full wave rectifier with (red line) and without (blue line) time-dilation circuits with respect to the input pulse of (a) 100V and (b) 300V.

clearly shown that without time-dilation circuit, the full wave rectifier just follows the input but the maximum voltage is limited by the protection circuit, thus it is unavoidable to waste the energy through the protection circuit. In contrast, by using the time-dilation circuit, the output voltage can be built up progressively once  $N_T$  is turned ON and can be held by the storage capacitor  $C_T$  even after the input subsides. The over-voltage protection is determined by the break-down voltage of the reverse p-n junction which for a  $0.5\mu$ m CMOS process is approximately 10V. The minimum voltage  $V_{MIN}$  is determined by the voltage required to activate hot-electron injection on the floating-gate injectors. This voltage has been experimentally determined to be around 6V, based on our previous work [31]. The threshold voltage of the diodes (proposed and measured in [31]) is approximately 1V, which leads to the number of diodes in Fig. 4.3(b) as K=6.

Thus, there is sufficient time for the sensor to measure the level of the impact energy. In addition, the time that the energy is stored on the capacitor also increases as the input pulse level increases. It is also shown in the simulation that the start-up responses are identical for both circuits. Fig. 4.5 compares the energy that can be measured for the sensor with and without time-dilation circuit. As the input pulse level increases, the energy that can be measured monotonically increases for both configurations. However, it is clearly shown that: by using the time-dilation circuit the sensor can harvest more energy from the input impulse and hence should be able to



Figure 4.5 Comparison between the stored energy with (red line) and without (blue line) time-dilation circuit as the input pulse level increases.

activate more sensor functions.

# 4.4 Differential Configuration and Rotational Impact

As described in the previous section, a single piezoelectric transducer based time-dilation circuit could be used to measure the energy of an impact that is spatially localized around the position of the transducer. This is shown in Fig. 4.6(a) which corresponds to the case when a specific region of the helmet experiences linear acceleration. However, for concussion studies the statistics of rotational acceleration is also important. The helmet experiences a rotational acceleration (about some reference axis - typically the neckline of the player) when it experiences a lateral impact as shown in Fig. 4.6(a). In this case, regions of the helmet that are symmetric about the reference axis will experience different levels of impact energies and will result in the rotational motion (or snap) of the head. The case for linear acceleration and rotational acceleration can be discriminated using piezoelectric transducers placed at different spatial locations.

In Fig. 4.6(b) we show measured responses from piezoelectric transducers placed at three locations on the helmet. For a direct head-on impact, the front piezoelectric transducer generates a large output pulse signal, and the piezoelectric transducers located at the sides of the helmet show



Figure 4.6 (a) Illustration of the linear and rotational accelerations; (b) Measured pulse responses of the sensors in three positions with respect to the direct and lateral impacts, respectively.

similar but weak responses. For the lateral impact, the piezoelectric transducers on the two sides generate strong and complementary responses as expected, and the front piezoelectric transducer show a very weak response because the impact is parallel to the front transducer.

Based on these observations, energy due to a linear acceleration impact can be measured using a single transducer and has already been verified in the simulation shown in Fig. 4.4. The impact energy causing the rotational acceleration can be measured using a pair of transducers in a differential configuration as shown in Fig. 4.7(a). The positive terminals of the transducers are used as two inputs of the rectifier while the negative terminals of the transducers are connected together. Thus, the direct and lateral impacts shown in Fig. 4.6(b) can be seen as the common-mode and differential-mode inputs for the full wave rectifier, respectively.

Similar to the previous simulation study, the equivalent circuit in Fig. 4.7(a) is used to understand the time-dilated response for measuring rotational impact energy. Fig. 4.7(b) presents the



Figure 4.7 (a) A pair of piezoelectric transducers are connected in differential configuration to test the rotational acceleration; (b) The simulated output voltage of the rectifier for the common-mode and differential-mode input signal when using differential connected piezoelectric transducers with time-dilation circuit.

simulated output voltage of the rectifier for the common-mode and differential-mode input signal when using differential connected piezoelectric transducers with the time-dilation circuit. It can be seen that the configuration of piezoelectric transducers in Fig. 4.7(a) only responds to the differ-

ential signal (due to rotational impact) but not to the common-mode signal (that caused by linear acceleration).

# 4.5 PFG based Self-powered Energy Measurement and Data-logging

The piezo-floating-gate (PFG) based self-powered sensing was reported in [15] and is briefly described here. PFG based sensors exploits an interesting property of the ceramic and polymer based piezoelectric materials (e.g. PZT and PVDF), which is able to generate large open-source voltage (>10V/ $\mu\epsilon$ ), with pico-to-nano amperes of current driving capability (due to large capacitive coupling). This property, however, is ideal for triggering impact-ionized hot-electron injection (IHEI) in silicon transistors requiring high-voltages while operating with ultra-low currents. If the gate of the silicon transistor is isolated by the high quality insulating oxide, such as floating gate transistor the injected electrons remain there for long intervals of time (>8 years for 8 bits precision). As the piezoelectric element is periodically excited, more electrons are injected onto the floating gate and the total amount of charge on the floating gate indicates the duration and extent of the mechanical disturbance. We have shown that the PFG self-powering device is capable of operating at pico-watt  $(10^{-12}-10^{-9} \text{ W})$  power dissipation levels, with its response remaining invariant for mechanical strain-levels down to a few micro-strains ( $\mu\epsilon$ ). This enables the PFG device to potentially sense, compute and store at the fundamental limits of the harvestable impact-energy.

In this work, the PFG principle is used to measure the magnitude of impact energy which determines the amount of charge that is deposited on the time-dilation capacitor in Fig. 4.3(b). The amount of charge can be estimated by the time it takes to discharge the time-dilation capacitor. However, for self-powered operation the measured data also needs to be stored on a non-volatile memory for subsequent retrieval. Self-powered and non-volatile time-measurement can be readily implemented using our previously reported linear floating-gate injector topology [32]. The circuit level schematic of the linear floating-gate injector is shown in Fig. 4.8. The circuit consists of a floating-gate pMOS transistor  $M_{\rm fg}$  whose source is driven by a constant current source  $I_{\rm ref}$  which is



Figure 4.8 Schematic of the data-logging circuit with a floating-gate based linear injector and a spiking analog-to-time converter

powered by either a piezoelectric transducer (during battery-less operation) or by an energy source  $V_{\text{ext}}$  (when the data is being retrieved by a reader). Note that the energy sources are isolated by a diode which allows  $V_{\text{ext}}$  to supersede the signal generated by the piezoelectric transducer. The opamp *A* (connected to  $V_{\text{ref}}$ ), the constant current source  $I_{\text{ref}}$ , and the floating-gate transistor  $M_{\text{fg}}$  form a negative feedback configuration when the switch  $S_{\text{P}}$  is open, thus ensuring that the source  $V_{\text{s}}$  and gate  $V_{\text{g}}$  voltages remain constant. Since the drain voltage of  $M_{\text{fg}}$  is tied to ground, if the reference voltage  $V_{\text{ref}}$  exceeds 4.2V, the negative feedback will cause the source-to-drain voltage of  $M_{\text{fg}}$  to also exceed 4.2V, which causes electrons to inject onto the floating-gate. Because all terminal parameters of the floating-gate transistor are held constant during the injection process, the injection current  $I_{\text{inj}}$  remains constant. Thus, the amount of charge injected onto the floating-gate, or the decrease in floating-gate voltage  $V_{\text{fg}}$ , is proportional to the duration for which the source current  $I_{\text{ref}}$  is activated and  $S_{\text{P}}$  is open. This can be expressed as:

$$\Delta V_{\rm fg} = \frac{1}{C_T} \int_0^T I_{\rm inj} dt = \frac{I_{\rm inj}}{C_T} \tau(T), \qquad (4.1)$$

where  $\tau$  is the duration of injection and  $C_{\rm T}$  is the total floating-gate capacitance which includes  $C_{\rm fg}$ , tunneling capacitance, and other parasitic capacitances associated with the floating node.

The change in floating-gate voltage  $\Delta V_{fg}$  is measured by closing the switch  $S_P$  which breaks the feedback loop by shorting the other terminal of  $C_{fg}$  to ground. Because the source current  $I_{ref}$  is constant,  $\Delta V_{out} = \Delta V_{fg}$  which is read-out using a analog-to-time converter as shown in Fig. 4.8. The

analog-to-time converter uses a multiplexer to switch the voltage reference of a comparator to one of three voltages  $V_{out}$ ,  $V_{cal1}$  and  $V_{cal2}$ . The calibration voltages  $V_{cal1}$  and  $V_{cal2}$  are the outputs of two linear injectors whose values remain fixed and are programmed only during the sensor initiation. The purpose of these calibration voltages is to compensate for any gain and offset errors in the analog-to-time converter. The output  $D_{out}$  of the comparator periodically toggles the pMOS and the nMOS switches, one at a time. Thus the current  $I_P$  charges the capacitor  $C_{ADC}$  to the voltage  $V_s$  after which the current  $I_L$  is turned ON which discharges  $C_{ADC}$  and generates a spike, as shown in the inset of Fig. 4.8. The time-difference  $T_{out}$  between two spikes is proportional to the voltage input which in turn is proportional to the floating-gate voltage  $V_{fg}$ . For calibration, the MUX then selects the first calibration voltage  $V_{cal1}$  and measures the corresponding time-difference  $T_{cal1}$  after which it selects the next calibration voltage  $V_{cal2}$  and measures the corresponding time-difference  $T_{cal2}$ . The output voltage  $V_{out}$  can be determined in terms of  $T_{out}$  and the calibration parameters as:

$$V_{\text{out}} = \frac{V_{\text{cal1}} - V_{\text{cal2}}}{T_{\text{cal1}} - T_{\text{cal2}}} (T_{\text{out}} - T_{\text{cal1}}) + V_{\text{cal1}}.$$
(4.2)

### 4.6 Measurement Results

The system architecture of the PFG sensor IC is shown in Fig. 4.9(a). It consists of 21 linear floating-gate injector channels where 14 of the channels are programmed to trigger at different levels of impacts. The 7 remaining channels are used for storing: (a) an identification code for the sensor; (b) placement location on the helmet; and (c) calibration voltages for the analog-to-time converter. The system architecture is divided into two main modules: (a) the self-powering module; and (b) the programming module. During the programming mode, an external supply  $V_{ddD}(\sim 2V)$  activates the high-voltage charge-pumps which generate the supply voltage  $V_{dda}$  to drive the sensor and the read-out buffers. The high-voltage charge-pumps are also used for generating the tunneling voltage  $V_{Tun}(\sim 16V)$  which is used for erasing the charge on the floating-gates of the linear injectors. A Power on Reset (PoR) generates the reset (RST) signal which is used to



Figure 4.9 (a) System architecture for the PFG sensor. (b) Micrograph of the sensor IC integrating different modules: 1. Floating Gate Array; 2. Digital Decoder; 3. Tunneling Voltage Charge-pump; 4. Level Shifter; 5. Injection Control; 6. Diode Protection & Rectifier; 7. Voltage References; 8. Tunneling Charge-pump; 9. Injection Charge-pump; 10. Ring Oscillator; 11. Analog-to-time Converter; 12. Supporting circuitry, power-on reset, buffers, etc.

Table 4.2 Command Description

RESET	Clear all registers and select the first channel	
NEXT	Select the next channel	
INJECT	Reduce the value of current channel	
TUNNEL	Increment the value of all channels	

initialize the contents and state of all the digital registers and state-machines. A digital processor controls the hot-electron injection, tunneling and read-out through digital control lines (RESET, NEXT, INJECT and TUNNEL). The functionalities of each of these control signals are summarized in Table 4.2. The circuit level implementation for many of the read-out and charge-pump modules have been previously reported [15] and is omitted here for the sake of brevity. A prototype PFG sensor IC was fabricated in a  $0.5\mu$ m CMOS process and its micrograph is shown in Fig. 4.9(b) along with its measured specifications summarized in Table 4.3.

The sensor IC was then integrated on an external printed circuit board as shown in Fig. 4.10(b) which hosts the sensor IC, the time-dilation capacitor, the piezoelectric interface and the programming interface. The size of the sensor is  $2 \text{ cm} \times 1.5 \text{ cm}$  and easily fits in between the helmet's cushion pads. For our validation studies, the prototypes of the sensor boards were attached to a



Figure 4.10 Experimental setup used in the drop-tests: a COTS football helmet with embedded Integrated PFG sensor prototypes (inset).

Process	$0.5\mu m$ CMOS process	
Size	2.5mm × 2.5mm	
Energy Requirement for Self-powered Mode	100nJ	
Power Dissipation for Read-out Mode	75µW	
Power Dissipation for Programming Mode	150µW	
Supply Voltage	1.5V – 2.5V	
Read-out Resolution	< 8 bits @ 10Ksps	

Table 4.3 Interface Specifications of the Self-powered IC

Table 4.4 Technical details of the helmet

Brand Name	Riddell
Item Weight	4.8 pounds
Item Size	13''L × 9.5''W × 10''H
Material Type	Polycarbon Lexan Shell-Steel and Polyvinyl Coated Mask

football helmet (technical specifications summarized in Table 4.4) as shown in Fig. 4.10(a).

Fig. 4.11 shows measured results from a fabricated prototype comparing the voltage  $V_{OUT}$  under three different conditions: (a) without any time-dilation, based on the schematic shown in Fig. 4.3(a); (b) time-dilation using  $C_T = 50$ nF; and (c) time-dilation using  $C_T = 1\mu$ F. As shown in Fig. 4.11(a), the zener clips the output voltage at  $V_{MAX} = 10$ V and the sensor shuts down after the impulse decays. For the time-dilation circuit in Fig. 4.11(b), the storage capacitor  $C_T$  holds the



Figure 4.11 Measured results showing  $V_{\text{out}}$  for the sensor with: (a) no time-dilation circuit; (b) time-dilation circuit with  $C_{\text{S}} = 50$  nF; and (c) time-dilation circuit with  $C_{\text{S}} = 1 \,\mu\text{F}$ .

extra charge. Note that in Fig. 4.11(b), the start-up response remains unaffected which is important for logging different levels of impact. The result in Fig. 4.11(c) shows that choosing the right range of values for  $C_T$  is important as a large storage capacitor (even though it can store more charge) will take a longer time (hence duration of impulse event) to push the voltage  $V_{OUT}$  beyond  $V_{MIN}$  and activate the sensor.

The measurement setup emulated a smaller scale drop-test procedure reported in [33]. The helmet with the integrated sensor was dropped from two height levels: Height A (1 foot) and Height B (2 feet). For linear impact test, the helmet was dropped head first along a vertical axis passing through the top of the helmet. Fig. 4.12 shows the output of the piezoelectric transducer (without the sensor attached) when the helmet is dropped from heights A and B. The response clearly shows the impulsive nature of the piezoelectric signal generation and the voltage level clearly shows the need for the time-dilation approach.

Fig. 4.13 (a) shows the data recorded from the sensor when the helmet is dropped repeatedly from 1 foot. Note that even at this height the first three channels record the level of impact indi-



Figure 4.12 Signal recorded at the output of a PZT-5H piezoelectric transducer (10M $\Omega$  load) when the helmet is dropped from 1 foot (height A) and 2 feet (height B), respectively.



Figure 4.13 Measured output from three of the sensor channels when the helmet is repeatedly dropped from (a) 1 foot; (b) different heights.

cated by the change in their output voltage. The linearity of the response shows that the voltage measurements could be calibrated to different impact energy levels with corresponding acceleration levels. Fig. 4.13 (b) shows data recorded from the sensor when the helmet was dropped from 3 different heights. The Control signifies that the helmet was just tapped while at rest. The result shows that the sensor's gain increases as the height increases and hence the concussion energy,



Figure 4.14 (a) Measured impact distribution using three sensors: sensor 1 is in the front, sensor 3 is in the side and sensor 2 is in between; (b) Rotational impact test using a differential PFG sensor.

validating the sensor's ability to log diverse levels of impact.

Fig. 4.14 (a) presents the distribution of the data measured using three sensors where: sensor 1 was located in the front of the helmet, sensor 3 was located on the side and sensor 2 was located in between. During the drop test, the front position of the helmet directly impacts the ground, thus the change of the sensor 1 output is the largest of all three. The sensor 3 was mounted in the side of the helmet and its transducer is aligned parallel to the direction of the impact force, thus, its output remains relatively unchanged. Mounted between sensor 1 and 3, the sensor 2 also records the occurrence of the impact but shows a lower gain than sensor 1.

The rotational impact test was also performed in which a pair of PZT transducers were mounted on two sides of the helmet and their outputs were differentially connected as shown in Fig.4.7(a). For this test, the helmet was dropped along an axis passing through the side of the helmet. As described before, the direct and lateral impacts can be seen as the common-mode and differentialmode inputs for the sensor, respectively. The result in Fig. 4.14 (b) clearly shows that the sensor can record the instances of rotational impact (acceleration) and remains unaffected by the instances of direct impact (or linear acceleration).
# 4.7 Summary

This chapter presents a miniature sensor system that can be used to monitor the level and frequency of head impacts in helmeted sports. A time-dilation circuit enables the sensor to measure high energy impulses and a linear floating-gate injector enables the sensor to record data on non-volatile memory. The sensor is self-powered and operates by harvesting the energy from the head-impact with no need for batteries. It is demonstrated that different configurations and placements of the sensor inside a helmet can be used to sense, measure and record spatial and temporal statistics of linear and rotational head impacts. It is envisioned that due to its small form-factor and its low-cost, a large array of these self-powered sensors could be embedded at different locations inside the helmet. The historical information of the impacts and the type and nature of the impacts recorded by the sensors could be important mapping data for traumatic brain injury (TBI) researchers to prognosticate concussions during the course of normal play. Note that the activation threshold of the sensor (minimum impact energy) can be adjusted by changing the size of the time-dilation capacitor. In this manner, the sensor could be customized for different spatial locations and for different players.

### **CHAPTER 5**

# A CMOS SYSTEM-ON-CHIP FOR PASSIVE, NEAR-FIELD ULTRASONIC ENERGY HARVESTING AND BACK-TELEMETRY

# 5.1 Introduction

While passive radio-frequency (RF) based tagging and back-telemetry systems are attractive for embedded and implanted monitoring of environmental and biological processes [15, 34–38], the technology cannot be used inside conductive or ionic media where RF attenuation could be significant. An alternative solution to RF based telemetry is acoustic or ultrasonic based telemetry which has been demonstrated to exhibit low attenuation inside conductive media [39–46]. The use of ultrasound also allows miniaturization of the embedded telemetry system by relaxing the size requirements on the piezoelectric transducer. Also, unlike RF transmission which is regulated according to FCC requirements, ultrasonic power requirement is only limited by structure's mechanical compliance. In the literature, several ultrasonic telemetry systems have been reported for use in metallic structures [47–49] and for in-vivo applications [50]. In [41–46] passive ultrasonic telemetry systems have also been reported which eliminate the need for batteries on the sensors. However, these systems are either bulky or power hungry and thus are not suitable for massive deployment in practical applications.

This chapter presents the system-on-chip implementation of a near-field passive ultrasonic telemetry system that could be used for embedded monitoring inside the conductive structures and ionic media. Near-field operation allows optimization of the back-telemetry link via resonance tuning at the reader so that the complexity of the tag can be relaxed. In addition, once the resonant power and telemetry link has been established, near-field operation makes the interrogation and communication immune to the multi-path reflections from the material boundaries and discontinuities. An illustration of an ultrasonic tagging system is shown in Fig. 5.1 where an ultrasonic reader scans the surface of a conductive structure surrounding an array of embedded sensors/tags.



Figure 5.1 Illustration of an ultrasonic based telemetry system using acoustic coupling through the metal barrier.

The role of these sensors/tags is to convey measurements of some physical property of interest for example, temperature, pH, corrosion or humidity back to the reader. Under near-field operating conditions, the acoustic impedance of the piezoelectric transducer at the sensor/tag is reflected as an equivalent electrical impedance on the reader's telemetry circuits. To establish two-way communications, the sensor/tag firstly harvests energy from the reader signal and then electrically modulates the acoustic impedance of its piezoelectric transducer. A change in the sensor's acoustic impedance is reflected as a change in the driving current through the ultrasonic reader and then the current change is demodulated to recover the sensor data.

# 5.2 System Overview

#### 5.2.1 Ultrasonic power transfer and telemetry model

The most common ultrasonic transducers are the piezoelectric type materials like lead zirconimum titanate (PZT) and can convert acoustic energy into electrical energy or vice versa. Fig. 5.2(a) shows an interface comprising of a transmit PZT transducer and a receive PZT transducer which are separated by a metallic barrier. The transmit PZT is excited by an AC voltage source  $V_{IN}$  driven through a source resistance  $R_S$ . The generated ultrasonic wave propagates through the metal barrier and impinges on the receive PZT where the acoustic stress wave is converted into



(a)



Figure 5.2 Ultrasonic powering and communication system based on Mason model: (a) system diagram; (b) equivalent circuit model.

an electrical signal which then drives a load resistor  $R_L$ . For the sake of simplicity, in Fig. 5.2(a) an air backing has been used as a replacement for the front and tail mass [51]. For a disk-shaped transducer with diameter D the ultrasonic near-field depth L is given by [52]

$$L = \frac{D^2 f}{4v} \tag{5.1}$$

where f is the ultrasonic frequency and v is the velocity of the ultrasonic wave in the barrier material. Thus, for a fixed diameter of the transducer and the velocity of the ultrasound, a larger

near-field depth can be achieved at higher frequency. In this paper we have chosen the operating frequency f=13.56MHz which for a transducer with D=22mm and v=6400m/s (for Aluminum), leads to a near-field depth of L=256mm, sufficient for telemetry across millimeter sized barriers. Another advantage of using a higher operating frequency is that it allows the use of on-chip capacitors in the energy harvesting circuits as will be described in section III. Specifically, a 13.56MHz operating frequency is also compatible with the ISM band RFID standard which enables reuse of commercial off-the-shelf RFID readers for the proposed ultrasonic back-telemetry.

The efficiency of this near-field ultrasonic link can be analyzed using acoustic wave equations as described in [41]. However, the analytical solutions to the wave equations in piezoelectric materials are very complex, thus for one-dimensional analysis the acoustic link can be simplified using the Mason's equivalent lumped circuit model [53] as shown in Fig. 5.2 (b). The transformers  $N_1$  and  $N_2$  connect the acoustical and the electrical domains where all the mechanical parameters of the piezoelectric layer and the backing layer can be transformed to an equivalent T-network as shown in Fig. 5.2(b). The electrical impedances  $Z_{Tk}$  and  $Z_{Sk}$  correspond to the  $k^{th}$  element and can be estimated for a specific frequency f as

$$Z_{Tk} = j \cdot Z_{0k} \cdot tan(2\pi f \cdot \frac{t_k}{2\nu_k})$$

$$Z_{Sk} = -j \cdot Z_{0k} \cdot sin^{-1}(2\pi f \cdot \frac{t_k}{\nu_k})$$
(5.2)

where  $Z_{0k}$  and  $t_k$  are the characteristic impedance and the thickness of the  $k^{th}$  layer and  $v_k$  is the velocity of the ultrasound in the  $k^{th}$  layer. The characteristic impedance  $Z_{0k}$  can be estimated as

$$Z_{0k} = \rho_k \cdot v_k \tag{5.3}$$

with  $\rho_k$  being the density of the  $k^{th}$  layer.

The power transfer efficiency (PTE) for the ultrasonic model can be estimated by inserting the material properties of the PZT transducer and the acoustic properties of the metallic barrier (summarized in Table 5.1) into the model. Note that the PTE is given by

$$PTE = \frac{P_{OUT}}{P_{IN}} = \frac{Re(V_L \cdot I_L)}{Re(V_{IN} \cdot I_{IN})}$$
(5.4)

R		
Parameters	PZT	Aluminum
Density $\rho$ (kg/m <sup>3</sup> )	7800	2700
Velocity v (m/s)	2820	6400
Thickness t (mm)	0.25	0.1~4
Area $A (\mathrm{mm}^2)$	380	380
Permittivity $\varepsilon_{33}^S$ (F/m)	$4.78 \times 10^{-8}$	
N <sub>1</sub> N <sub>2</sub>	33.93	

Table 5.1 Material parameters used for link simulations.



Figure 5.3 The simulation of power transfer efficiency based on Mason model as a function of metal thickness.

where the load current  $I_L$  and load voltage  $V_L$  are determined using circuit simulations.

Fig. 5.3 shows the simulation result where the PTE of the model in Fig. 5.2(b) has been computed for metal thickness ranging from 0.1mm to 4mm. The transmit PZT and the receive PZT were chosen to have same dimensions and exhibited similar acoustical properties as a PZT-5H material. The frequency of the input source was set to 13.56MHz and the load resistor  $R_L$  was chosen to be 100 $\Omega$ . It can be seen from the result that the power transfer efficiency drops rapidly as the distance increases so that the energy harvesting distance is very limited, or the power transfer efficiency is too small.



Figure 5.4 Proposed ultrasonic communication system.



Figure 5.5 Power management modules which include a voltage multiplier, a voltage limiter and a regulator.

## 5.2.2 System Architecture

The system architecture of a ultrasonic back-telemetry system is shown in Fig. 5.4. The reader comprises of the digital controller, the analog front-end and the impedance matching circuit. The digital controller implements a state machine that sends and receives commands to and from the tag. The analog front-end modulates the digital signal with ultrasonic carrier and demodulates the backscatter signal. The impedance matching circuit is used to create a resonant network comprising of the the transmit PZT, the transmission medium and the receive tag. The receiver tag consists of a receive PZT and a matching circuit which forms a part of the ultrasonic resonant network.



Figure 5.6 The measurement results for different types of voltage multipliers (12-stage, 18-stage and 24-stage) under the load resistor of  $10M\Omega$  and  $1M\Omega$ .

Through this network, the tag receives electrical power and a power management module comprising of voltage multipliers and voltage regulators generate stable supply voltages for other on-chip modules. A demodulator extracts the raw data received over the resonant network and a digital state-machine performs error-correction and decodes the commands received from the reader. The state-machine also controls an analog-to-digital (ADC) converter which samples and digitizes the sensor signal for transmission back to the reader. Reverse transmission is achieved through backscattering by turning ON and OFF a switch connected to the receive PZT. Other modules in the system-on-chip design includes a power-on-reset (POR) circuit which is used for initializing all the states of the digital modules. An integrated ring-oscillator provides stable clock for digital baseband and the ADC.

# 5.3 Circuit Design of the Ultrasonic Tag

#### 5.3.1 Power Management Circuits

Due to the attenuation of the ultrasonic signal inside the solid medium and the transducer's limited energy conversion efficiency as well as the impedance mismatch at various interface, the magni-



Figure 5.7 Measurements of LDO: (a) dropout voltage for digital block; (b) dropout voltage for analog block; (c) line regulation for analog block when  $V_{IN} = 0$ V to 10V; (d) line transient response for analog block with  $I_L = 0.4\mu$ A,  $V_{IN} = 0$ V to 6V; (e) line transient response for analog block with  $I_L = 0.4\mu$ A,  $V_{IN} = 6$ V to 0V; (f) ripple rejection for analog block with  $I_L = 0.4\mu$ A; (g) line transient response for analog block with  $I_L = 400\mu$ A,  $V_{IN} = 0$ V to 6V; (h) line transient response for analog block with  $I_L = 400\mu$ A,  $V_{IN} = 6$ V to 0V; (i) ripple rejection for analog block with  $I_L = 400\mu$ A,  $V_{IN} = 6$ V to 0V; (i) ripple rejection for analog block with  $I_L = 400\mu$ A.

tude of the signal induced at the receive PZT is typically below 1V. Therefore a voltage multiplier is required to transfer charge and boost voltage on a storage capacitor [54,55]. For this implementation we have used a standard Dickson type multiplier [56] as shown in Fig. 5.5. The multiplier is comprised of Schottky junction diodes (with approximate threshold voltage of  $V_{th} \approx 300mV$ ) and produces an output voltage  $V_{OUT} \approx N \cdot (V_{IN} - V_{th})$ , with N being the number of multiplier stages.



Figure 5.8 (a) Block diagram and (b) detailed circuit design of data recovery circuit.

The measurement results in Fig. 5.6(a) and (b) shows the output of the multiplier with different number of stages and measured under different loading conditions. The power transfer efficiency of the voltage multiplier highly depends on the input power level and the loading condition. For input power level around -10dBm, the voltage multiplier' efficiency is around 10% with 100k $\Omega$  of load resistor. In addition, to limit the maximum voltage (in this case 11V) generated by the multiplier, the output voltage is clamped using a diode chain as shown in Fig. 5.5. If the multiplier output  $V_{DC}$  is below 11V, the voltage limiter only consumes nA level current so that the limiter's efficiency can be thought nearly 100%.

Considering that the multiplier output will fluctuate with the magnitude of the received power and is susceptible to high-frequency ripples, a regulator has been used to obtain a stable DC output

voltage. In this work, we have implemented a hybrid topology combining the efficiency of a switching regulator with the simplicity of ripple-rejection ability of a linear regulator. The circuit is shown in Fig. 5.5 and consists of a current reference circuit formed by transistors  $M_1 \sim M_{10}$ and a regulator circuit formed by transistors  $M_{11} \sim M_{13}$  and  $M_{D1} \sim M_{DN}$ . Transistors  $M_1$ ,  $M_2$ and  $C_1$  form the start-up circuit in Fig. 5.5 and transistors  $M_3 \sim M_{10}$ ,  $C_2$  and R generate a supplyinsensitive current which is given by  $I_{ref} \approx U_T / R \log(M)$  with M being the ratio of the aspect ratios for transistors  $M_9$  and  $M_{10}$ . Once the current reference is set up,  $M_2$  is turned on and  $M_1$  is turned off to minimize the power consumption. Note that a minimum voltage is required for the current reference to be enabled. Below the minimum voltage level the current reference is OFF. This leads to a switching response similar to a switching-type regulator where if the load voltage goes below a certain threshold, the load is disconnected and the storage capacitor is recharged till the voltage level exceeds the threshold. Once the input voltage level is greater than the minimum startup voltage, the circuit formed by the transistors  $M_{11} \sim M_{13}$  and  $M_{D1} \sim M_{DN}$  act as a linear regulator. Because the current flowing through the diode chain  $M_{D1} \sim M_{DN}$  is held constant by the current reference, the voltage  $V_{DD}$  is held constant by the feedback transistor  $M_{12}$  and the output transistor  $M_{13}$ . Note the load current flows through the output transistor  $M_{13}$ , therefore the driving capability of  $M_{13}$  has to be adjusted by increasing its aspect ratio. The efficiency of this linear regulator is determined by the power dissipation due to  $M_{13}$  which is a function of the load current and the voltage drop  $V_{DC} - V_{DD}$ .  $C_3$  is used to stabilize the output voltage when the load current  $I_L \neq 0$ , and disable the current through  $M_{13}$  when  $I_L = 0$ . For this design, the regulator was designed for a maximum load current of 1mA, so the size of  $M_{13}$  was chosen to be  $300\mu$ m/0.6 $\mu$ m and the size of  $C_3$  was chosen to be 1pF.

Some experimental results corresponding to the proposed regulator are shown in Fig. 5.7 where two regulators were designed one for driving the analog modules and the other for driving the digital modules. The preset output voltages for digital and analog regulators were chosen to be 2V and 4V, respectively. The input to the regulator was a triangle wave as shown in Fig. 5.7 (a) and (b) and dropout voltages were around 0.8V and 1.2V for digital block and analog block, respectively.



Figure 5.9 Communication protocol: (a) PIE; (b) Manchester.

It is noted that the results of regulator for analog block are shown in Fig. 5.7 because regulator for digital block exhibit the similar behavior. The line regulation measured for the analog regulator was 120mV when  $V_{IN} = 5V$  to 10V, which corresponds to 2.4% of deviation as shown in Fig. 5.7 (c). For the digital regulator the deviation was measured to be 2.2% under the condition  $V_{OUT} = 1.88V$  to 2.04V when  $V_{IN} = 2.7V$  to 10V. Fig. 5.7 (d), (e) and (g), (h) show the line transient responses for loading current of 0.4 $\mu$ A and 400 $\mu$ A, respectively. It is noted that the start-up response time are similar for both cases (148 $\mu$ s for  $I_L = 0.4 \mu$ A and 146 $\mu$ s for  $I_L = 400 \mu$ A, which corresponds to 6.7KHz bandwidth), but the shut-down time is determined by the loading current (1000 $\mu$ s for  $I_L = 0.4 \mu$ A and 1.46 $\mu$ s for  $I_L = 400 \mu$ A) because the discharging time  $t \propto C_3 V_{DD}/I_L$ . Fig. 5.7 (f) and (i) show the ripple rejection performance of the analog regulator when driving a small load current (0.4 $\mu$ A) and when driving a large load current (400 $\mu$ A), respectively. The input is 6V DC voltage with 1V ripple at 13.56MHz, and the analog regulator can suppress the voltage ripple to 192mV for  $I_L = 0.4 \mu$ A and 416mV for  $I_L = 400 \mu$ A.

The efficiency of the regulator can be estimated as

$$\eta = \frac{I_{OUT}V_{OUT}}{(I_{OUT} + I_q)V_{IN}}$$
(5.5)

where  $I_q$  is the quiescent current (also called ground current). In this design,  $I_q$  is nA level so that it can be neglected when comparing to  $I_{OUT}$  which is around  $\mu$ A level. Thus, the regulator's



Figure 5.10 (a) current reference; (b) ring oscillator with pulse shaping; (c) power-on reset circuit; (d) 8-bit single-slope ADC.

efficiency is just the ratio of output voltage to input voltage. For the regulator that drives the digital modules, the input voltage is 2.7V and the output voltage is 1.9V, thus its efficiency can be estimated to be 70.4%. For the regulator that drives the analog modules, the input voltage is 5V and the output voltage is 3.8V, thus its efficiency can be estimated to be 76%.

## 5.3.2 Data Recovery Circuit

The data recovery circuit is shown in Fig. 5.8(a) and demodulates a pulse-interval encoded (PIE) modulation signal. In a PIE code a longer duration between two digital pulses represents logic '1' and a short duration between two pulses represents logic '0'. The envelope of the modulated piezo-

electric signal is first extracted by a voltage doubler followed by a low-pass filter. A comparator then compares the filtered signal with  $V_2$  which is the mid-point of the supply voltage. Since the DC component of the  $V_1$  equals  $V_2$ , the comparator extracts the PIE signal. Note that a hysteretic comparator has been used in this design to reduce the effect of noise and interference. Fig. 5.8(b) shows the schematic of the comparator where transistors  $M_3 \sim M_6$  form a positive feedback which determines the upper and lower hysteresis transition points. The output of the comparator controls the gate of  $M_{11}$  which in turn controls the charging or discharging the capacitor *C*. For long duration between two binary pulses (logic '1' in PIE code),  $M_{11}$  is turned off sufficiently long so that the the capacitor is charged to a voltage exceeding the inverter threshold voltage - thus producing a logic "high" output. For short duration between the binary pulses (logic '0'), the output of the inverter remains low. Thus, the circuit in Fig. 5.8(a) effectively recovers the transmitted digital data.

### 5.3.3 Digital Baseband and Manchester Encoder

The digital baseband module includes the preamble circuit, the ADC controller and the Manchester encoder. The PIE data transmitted from the reader to the tag is encapsulated in a frame consisting of 4-bit preamble bits, 3-bit command bits and 1-bit CRC code, as shown in Fig. 5.9 (a). The 4-bit preamble is chosen to be '1100', 3-bit command encodes eight possible instructions that can operate the tag and the sensor, and 1-bit CRC is odd parity error checking. The preamble module firstly verifies the 4-bit preamble and then outputs the corresponding command if the 1-bit CRC code is correct. Based on the received command, the baseband circuit can have different responses, such as read the ADC data or just send a series of verification codes. The reverse transmission from the tag to the reader utilizes the Manchester encoding scheme where the data symbol '1' is encoded as '10' and the data symbol '0' is encoded as '01', as shown in Fig. 5.9 (b). Similar to the forward link, the protocol for the reverse link also consists of 4-bit preamble, 8-bit data and 3-bit CRC code. The 4-bit preamble is again set to be '1100', and the 8-bit data represents the ADC output or a series of '0' if just verification command is received. The modulator is a simple NMOS switch

which is turned ON/OFF by the Manchester data stream, thus transmitting ultrasonic wave can be back-scattered to the reader, as shown in Fig. 5.4.

#### 5.3.4 Sensor Data Acquisition Circuitry

A power-on reset (POR) shown in Fig. 5.10(c) detects the change in the supply voltage and generates a delayed digital pulse which is used to initialize all the digital logic and internal registers. The delay time  $t_d$  is determined by the charging current  $I_{ch}$  and capacitor size  $C_c$ ,

$$t_d = \frac{C_c V_{th}}{I_{ch}} \tag{5.6}$$

where  $V_{th}$  is the threshold of the inverter. In addition, the current-starved inverters have been used to minimize the power dissipation. An internal ring-oscillator is used for generating the system clock for the digital baseband and the clock is also used in the single slope ADC. A 3-stage current starved ring oscillator is proposed with pulse shaping circuit, as shown in Fig. 5.10 (b). The starved current is controlled by the current reference in which the resistor *R* can be used to tune the clock frequency. The schematic of a single slope ADC used in this design is shown in Fig. 5.10 (d). In the sampling phase,  $S_1$  is closed and  $S_2$  is open so that the input voltage  $V_{IN}$  is sampled on the capacitor. In the counting phase,  $S_1$  is open and  $S_2$  is closed, the capacitor begins to discharge through constant current source  $I_{REF}$ . Meanwhile, an 8-bit counter is trigger for counting the discharging time until the sampled voltage reaches  $V_{REF}$ . Once the sampled voltage is below  $V_{REF}$ , the comparator generates a pulse to stop the counter. Therefore the digital output can be assumed as

$$N = \frac{C \cdot (V_{IN} - V_{REF})}{I_{REF}} \cdot f \tag{5.7}$$

where *f* is the frequency of the counting clock. It is noted that *f* and  $I_{REF}$  should be tuned to meet the 8-bit resolution requirement for the full range. As shown in Fig. 5.11, the ADC's input range is 0.9V~3.2V and the resolution is about 12.8mV per bit. The SNR was measured to be approximately 47dB which results in an effective number of bits to be 7.5bits. The maximum sampling rate of the ADC is 250KS/s. Also, note that the reference current  $I_{REF}$  is generated using a



Figure 5.11 Measured result of the 8-bit ADC.



Figure 5.12 Measurement setup of the ultrasonic communication system: (a) the ultrasonic reader consists of Xilinx FPGA and TI Analog Front End (AFE); (b) Tx PZT and Tx PZT are separated by 2mm thick Al metal barrier; (c) micro-graph of the fabricated ultrasonic tag IC.

PTAT and hence varies linearly with temperature. The counter clock frequency f is generated using a ring-oscillator shown in Fig. 5.10(b) whose frequency also varies linearly with temperature. Thus, according to equation 5.7, the ADC output should theoretically be temperature compensated. However, transistor mismatch in the PTAT circuit and the offset mismatch between the amplifiers in Fig. 5.10(d) will lead a weak dependency on temperature. Note that the response of the piezoelectric transducer will also vary with temperature, so any temperature or mismatch compensation has to be achieved at a system level using calibration tables.



Figure 5.13 (a) Measured transmit power from the Tx PZT and (b) receive power from Tx PZT.



Figure 5.14 Measured results showing protocol synchronization between the reader and the tag IC.

# 5.4 Measurement Results

The ultrasonic tag IC has been implemented and fabricated in a  $0.5-\mu$ m standard CMOS process with a die area of  $3mm \times 3mm$ , as shown in Fig. 5.12 (c). The main specifications of this SOC is listed in Table 5.2. The total power consumption of the system-on-chip was measured to be

Fabrication process	$0.5-\mu m$ standard CMOS	
Die size	3mm×3mm	
Total power consumption	22.3µW	
ADC	14.9µW	
Digital baseband	3.4µW	
POR Oscillator and Demodulator	3.3µW	
Voltage regulator	0.7µW	
Ultrasonic modulation scheme	100%ASK	
Carrier frequency	13.56MHz	
Interrogation distance	2mm	
Sensor input voltage	0.9V - 3.2V	

Table 5.2 Main Specifications for Proposed Ultrasonic Receiver IC.

22.3 $\mu$ W out of which the ADC consumes 14.9 $\mu$ W, digital baseband consumes 3.4 $\mu$ W, the regulator consumes 0.7 $\mu$ W, and the remaining 3.3 $\mu$ W is consumed by the demodulator, the POR and the oscillator. The custom-made ultrasonic reader comprises of an FPGA board (Xilinx Spartan-3) and a COTS Texas Instruments chipset (TRF7960). Since the communication protocol in this design has been customized, the built-in communication protocol of the TRF7960 was bypassed and only the analog front (AFE) was used. The FPGA board is used for command and control of the TRF7960 chipset. The system setup is shown in Fig. 5.12 where the output power of TRF7960 is set to 200mW and the carrier frequency is 13.56MHz with 100% ASK. The benefits of using ASK as opposed to other modulation schemes like FSK or PSK is that the demodulation circuits are relatively simple to implement which is important for a power constrained energy harvesting application.

An impedance matching network is inserted between the PZT and the communication circuits to maximize power transmission. The input impedances for the Tx PZT and Rx PZT measured at 13.56 MHz are found to be  $3.2+8.7j\Omega$  and  $2.7+13.6j\Omega$ . Thus T-type matching network is used so that the Q-factor of the matching network can be adjusted and the input impedance is appropriately transformed to  $50\Omega$ . The communication and power transfer channel is formed by the metal plate between two PZTs. The path loss of the channel should is first characterized to determine the optimal placement of receiver tag relative to the reader. When the PZTs are respectively impedance matched, the power received by the Rx PZT at a distance of 2mm is found to be -10.2dBm when the transmit power from the Tx PZT is measured to be 17.3dBm, as shown in Fig. 5.13. Thus the channel attenuation is estimated to be 27.5dB which corresponds to 0.18% of power transfer efficiency. It should be mentioned that the measured power transfer efficiency is very close to the theoretical calculation based on Mason model which shows 0.21% for 2mm thickness Al in Fig. 5.3.

A snapshot of the successful communication sequence between the reader and the tag is shown in Fig. 5.14. First, the transmitter issues a PIE encoded 'Query' command (top waveform) '11000010' (the first pulse is ignored). The first four bits '1100' correspond to the preamble and the trailing three bits '001' indicates the command, and the last bit '0' is CRC. Then, the receiver correctly demodulates and recovers the command (second and third waveform), and sends back an 'Acknowledgement' (bottom waveform), which is then received and recovered by the transmitter. The 'Acknowledgement' signal is Manchester encoded as '110000000000000'. Similar to PIE code, the first four bits '1100' is also preamble, and the remaining eight bits '00000000' is 'Acknowledgement' signal, the last three bits '000' is the CRC. Once the protocol synchronization has been established between the reader and tag, the reader can issue additional commands to control and monitor the tag.

# 5.5 Summary

This chapter presents the design of a completed near-field ultrasonic receiver tag SoC. The tag harvests its operational energy directly from the acoustic interrogation signal generated by a reader which is implemented using a 13.56MHz COTS device. Due to the near-field operation, the tag can achieve bi-directional communication using an acoustic back-scattering, where the properties of the communication link can be optimized by the reader. The operation of the system has been verified using prototypes fabricated in a  $0.5\mu$ m CMOS process. While the use of near-field op-

	This work	[42]	[43]	[57]
Carrier frequency (MHz)	13.56	1	power channel: 1	1
			communication: 4	
PZT size (mm <sup>2</sup> )	380	506	power PZT: 3492	28
			communication: 506	20
System size (mm <sup>2</sup> )	10	31.75	_	96.8
Modulation Scheme	ASK	ASK	OFDM	ASK, PSK, FSK
Barrier	Al	Steel	Steel	Skin
Interrogation distance (mm)	2	304.8	63.5	
Power consumption (mW)	0.022	$\leq 100$	-	1.8
Bidirectional communication	Yes	Yes	Yes	Yes
Energy harvesting	Yes	Yes	Yes	Yes
Sensing external signal	Yes	Yes	Yes	Yes
SOC	Yes	No	No	No

Table 5.3 Performance Comparison.

eration limits the interrogation distance of the proposed system, the complexity of the tag can be significantly reduced. The near-field depth, however, can be adjusted by choosing a higher operating frequency which also allows the use of on-chip capacitors for harvesting acoustic energy. Table 5.3 compares the proposed design with other ultrasonic energy harvesting and tagging systems. The comparison shows that the power dissipation of the proposed system is an order of magnitude lower than other systems. If a figure-of-merit (FOM) is defined as

$$FOM = \frac{D_{Com}}{S_{PZT} \times S_{Sys} \times P_{Sys}}$$
(5.8)

where  $D_{Com}$  is the communication distance,  $S_{PZT}$  and  $S_{Sys}$  are sizes of PZT and system, respectively, and  $P_{Sys}$  is power consumption of the system, the proposed design is two orders of magnitude superior than that of [42]. Note that the FOM could not be computed for other references in Table 5.3 because some of the experimental parameters were not reported.

#### **CHAPTER 6**

## CONCLUSION

# 6.1 Summary of Contributions

Energy harvesting technology is playing a more and more important role in the advanced electronic systems that require smaller form-factor, lower cost and longer life-time. However, efficiently converting the harvested energy from the environment into effective electrical energy is a key factor for the successful deployment of the energy harvesting systems. This dissertation thus focuses on the improvement of the power conversion efficiency of the energy harvesting circuits. Specifically, this dissertation presents several solutions to answer the research problems that are proposed in section 1.3: how to efficiently harvest the power for (1) ultra low power applications and (2) impact energy applications. The major contributions of this dissertation are summarized as below.

1. To harvest as much power as possible for the ultra low power applications, a high-Q series matching network is proposed and verified. Compared to the conventional parallel matching network which needs to trade-off between the Q-factor and the coupling coefficient, the series matching network uses an extra small inductor to boost the Q-factor so that the coil inductance can be released from the matching network, and then the size of the coil can be enlarged to achieve larger coupling coefficient. Therefore, the constrain between the Q-factor and coupling coefficient can be released. With high-Q matching network, the coupled AC voltage can be boosted to overcome the dead zone of the voltage rectifier, leading to the efficiency improvement of the overall RF power harvesting systems. The measurement results show that given a fixed distance the boosted voltage in the series matching network is nearly double of that in the parallel matching network.

2. To minimize the threshold effect of the rectifying device, a hybrid rectification technique is proposed and verified. The hybrid rectification technique can efficiently harvest the RF signal lower than the threshold with the help of the PZT energy which is used as DC boost voltage for the RF signal. Compared to the conventional cross-coupled rectifier, the peak power conversion

efficiency of the proposed hybrid rectifier is able to be increased by 30%. In addition, the hybrid rectifier works more efficiently at larger loading condition because of large size of the rectifying transistor.

3. To extend the harvesting duration for the impact energy applications, a time-dilation circuit is proposed and verified. In time-dilation, impact energy is spread and conserved in time such that the self-powered sensor can accurately measure the energy level while operating within the electronic safety compliance levels. A nonlinear compressive circuit enables the sensor to quickly respond to the impact while enhancing the dynamic range (range of impact levels that can be measured) of the PFG sensor.

4. To investigate the energy harvesting applications in the conductive structures or ionic media, an ultrasonic receiver system is designed and implemented in standard CMOS process. The system is self-powered by harvesting the ultrasonic energy from a remote vibration source. In addition, this system operates in the acoustic near-field so that the bi-directional communication can be achieved by using acoustic back-scattering. Due to the near-field operation, the interrogation distance is relative short, but the power consumption of the system is significantly low when comparing to other ultrasonic energy harvesting systems.

# 6.2 **Open Problems**

Although this research has proposed several effective solutions to improve the efficiency for energy harvesting systems, there are still many open problems that can lead to further improvement in this area. Some of these open problems are discussed below.

One of these problems that can be explored is the possibility of auto-tuning impedance matching network for the RF energy harvesting. Auto-tuning impedance matching network could help to maintain the efficiency considering the available RF power is variable in the frequency and amplitude. One of the main problems with auto-tuning impedance matching network is the need of the control circuits that will increase the power consumption of the system. An alternative method is to use wideband impedance matching network, however the high Q-factor is difficult to obtain for wideband network, thus this is still an interesting problem for future research.

Another open problem associated with the RF energy harvesting is to explore more hybrid rectification techniques to overcome the dead-zone issue. This research proposes to use vibration energy as the auxiliary bias for the voltage rectifier to reduce the threshold effect, however, other ambient energy sources can also be considered, such as thermal or solar energy, depending on the practical applications. As mentioned in section 1.1, the benefit of the thermal and solar energy is the higher power density compared to vibration source. Integrating solar energy harvesting function into the wireless sensors could be quite useful for outdoor wireless sensor network, such as the environmental monitoring sensors that can use the DC power harvested from the solar cell as the bias for the RF rectifier.

This dissertation presents a near-field ultrasonic energy harvesting system with back telemetry. Operation in the acoustic near-field limits the communication distance between the tag and the reader. To extend the telemetry capability, it is thus worth to investigate the far-field ultrasonic energy harvesting system. In addition, the ultrasonic system miniaturization and power reduction are also attractive for future work, especially for the implantable medical applications where the use of the ultrasonic is considered to be safe. BIBLIOGRAPHY

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