A WWV SYNCHRONIZED DIGITAL CLOCK

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ABSTRACT

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This work contains the details of the design of a WWV synchronized digital clock. The microprocessor-based digital clock automatically sets itself to the correct time using the encoded time information in the 10 MHz WWV transmissions. (WWV is a station operated by the National Bureau of Standards dedicated to the continuous transmission of time information and radio wave propagation conditions.) Once the digital clock has set itself it will frequently update the displayed time in order that it never varies from the correct time. The WWV synchronized digital clock described in this work differs from previous ones in that it is a consumer-oriented and inexpensive device.

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CHAPTER I

INTRODUCTION

1.1 Background

Devising an accurate timepiece is a problem man has been endeavoring to solve for thousands of years. In the past, sundials, hourglasses, and mechanical timepieces were used to keep time. These devices are very inaccurate, by today's standards, because of the inherent inaccuracy of their timing sources (sun, sand, pendulum, spring, etc.). Today, most timepieces derive their timing signals from either a quartz crystal oscillator or the 60 Hz power line frequency. A fine quartz timepiece has very good short term accuracy (about 1 part in 10^8) but because of frequency drift by the oscillator it will gain or lose about 30 seconds a year. On the other hand, a clock with a 60 Hz line frequency time base has poor short term accuracy (about 1 part in 10^4) but for the long term it will normally vary less than 2 seconds from the correct time. Of course, the time on any clock dependent solely on the power from an electric utility company can greatly vary from the true time if a power outage should occur.

The National Bureau of Standards (NBS) in Boulder, Colorado, operate a cesium beam clock which is used as the world time standard. The frequency of the cesium beam controlled oscillator in the clock is one of the stablest frequencies in existence (stable to 1 part in 10^{12}).[(1)] The standard time maintained by NBS is called Coordinated

Universal Time (UTC). NBS broadcasts coded UTC on the shortwave frequencies of 2.5, 5, 10, 15, and 20 MHz from their station WWV located in Fort Collins, Colorado.

The objective of this thesis is the design of a clock that will interpret the coded UTC transmissions from WWV and display that information. Ideally, this clock will have the short term accuracy of a quartz crystal oscillator and a long term accuracy better than the 60 Hz line frequency. If the power to the clock is interrupted for any period of time, when it resumes the clock will automatically set itself.

While clocks that derive their time from NBS already exist commercially, they differ from the one described in this thesis in two important aspects.(2) First, the commercial models are made to be used in a scientific research establishment and therefore are relatively expensive instruments (greater than $2500). The clock described in this thesis is aimed at the consumer and will be much less expensive. Secondly, most of the commercial models use the 60 KHz WWVB transmission which requires the use of a bulky antenna that must be mounted externally of any structure. The 10 MHz WWV broadcast, the clock described herein uses, can be received on a telescoping whip antenna thus enabling the clock to be made into a self-contained unit.

Because of the daily periodic changes in the ionosphere, only the shortwave frequencies above approximately 10 MHz will propagate over long distances during the day and only the frequencies below about 11 MHz will propagate over long distances at night. Based on the above fact the 10 MHz WWV frequency was chosen for the clock because it is the only WWV frequency that can be received during both the day and night.

1.2 WWV Time Code

The coded UTC information is transmitted continuously by WWV. NBS has employed a method of encoding the time of the day and day of the year that requires an entire minute to transmit.[1] Figure 1 shows the envelope used to modulate a 100 Hz subcarrier of WWV. A pulse occurs once each second except the zeroth second of the minute. The leading edge of every pulse coincides with the start of the second and the pulse width determines whether it is a coded zero, one or marker. The pulse width of a coded zero, one and marker is 0.2, 0.5 and 0.8 seconds respectively.

Each minute is divided into six ten-second segments called frames. A marker occurs every tenth second marking the end of the frame. The fifth second of each frame is always a coded zero. Thus only eight seconds of a frame remain to carry coded time information. The eight bits of data contained in these eight seconds will henceforth be referred to as a record. The first record of the minute always consists entirely of zeros. The second record contains the minute information in binary coded decimal (BCD). Note that the first four bits of the record are the units and the last four are the tens of the coded number in binary. The third record contains the hour information encoded the same as the minutes. The remaining three records contain day of the year and time correction data not used by this device. Figure 2 exemplifies the WWV time code, showing the relevant part of the code that would be transmitted beginning at 21:39:00.

WWV broadcasts contain additional information along with the encoded time. Of major interest is a 1 KHz tone burst that occurs at the start of each minute and has a duration of 0.8 seconds.

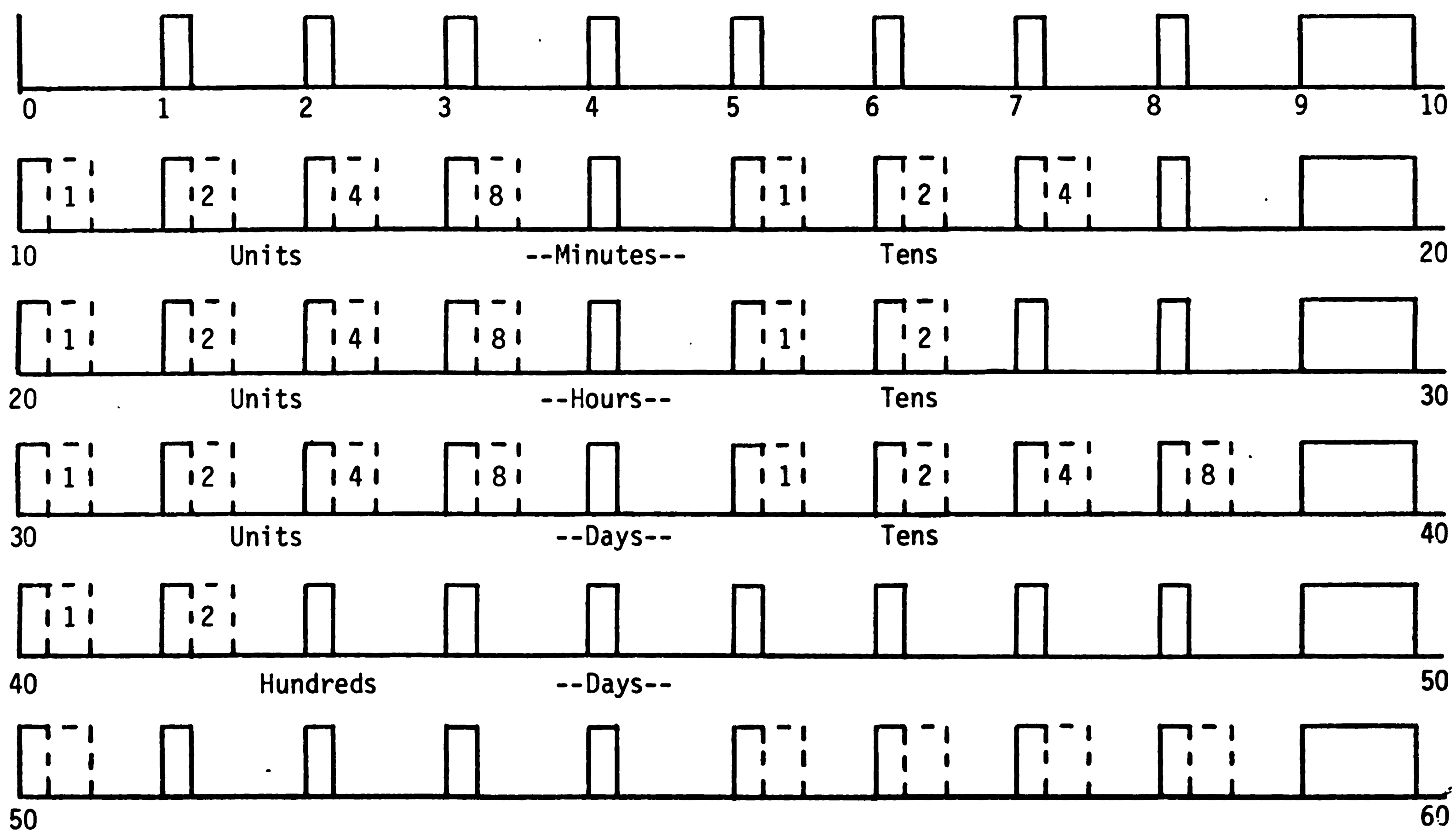


Figure 1 -- WWV Time Code

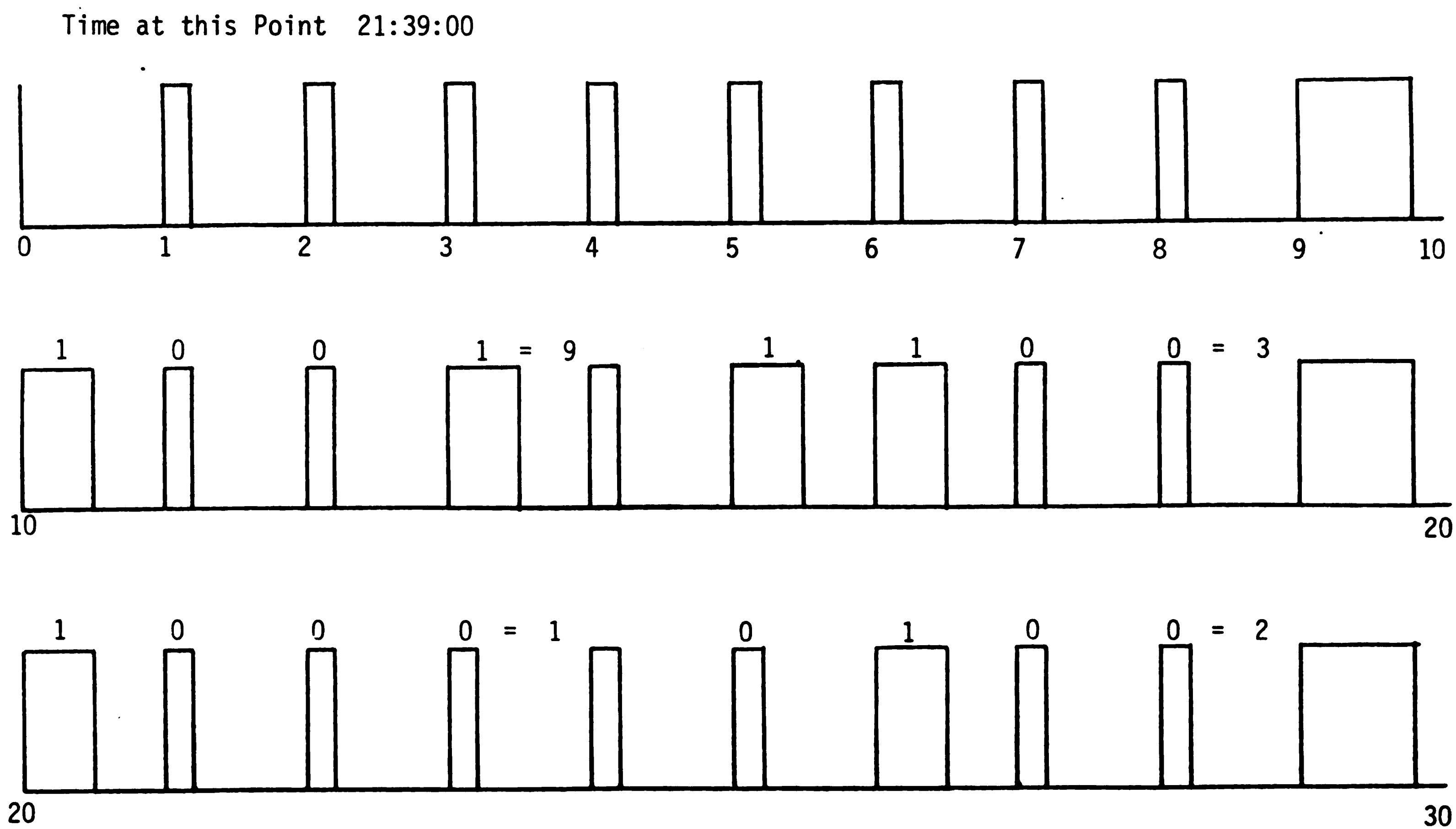


Figure 2 -- Example of WWV Coded Time

CHAPTER II

SYSTEM ORGANIZATION

2.1 Introduction

A block diagram of the self-setting clock is illustrated in Figure 3. The system is divided into three main parts: the clock, the microprocessor (μP), and the receiver and signal conditioning section.

2.2 Clock Subsystem

The clock consists of a divider, six counters, a multiplexer, and a display. The counters are connected to count in the typical hours-minutes-seconds fashion. The outputs from the counters are time multiplexed using timing control signals from the divider. The display decodes the multiplexed counter outputs and displays the time information on six multiplexed LED digits.

Time is kept by the clock essentially independent of the rest of the system. A 1 Hz pulse train needed to drive the seconds counters of the clock is obtained by dividing down the signal from a high frequency crystal oscillator. The short term accuracy of this 1 Hz signal is sufficient to keep the clock reasonably precise during intervals when the transmission from WWV is not received.

There are three inputs to the clock that are under μP control: the seconds set, the minutes and hours reset, and the minutes clock. The seconds set allows the μP to set the seconds to one. With the minutes and hours reset input the μP can zero the minutes and hours counters.

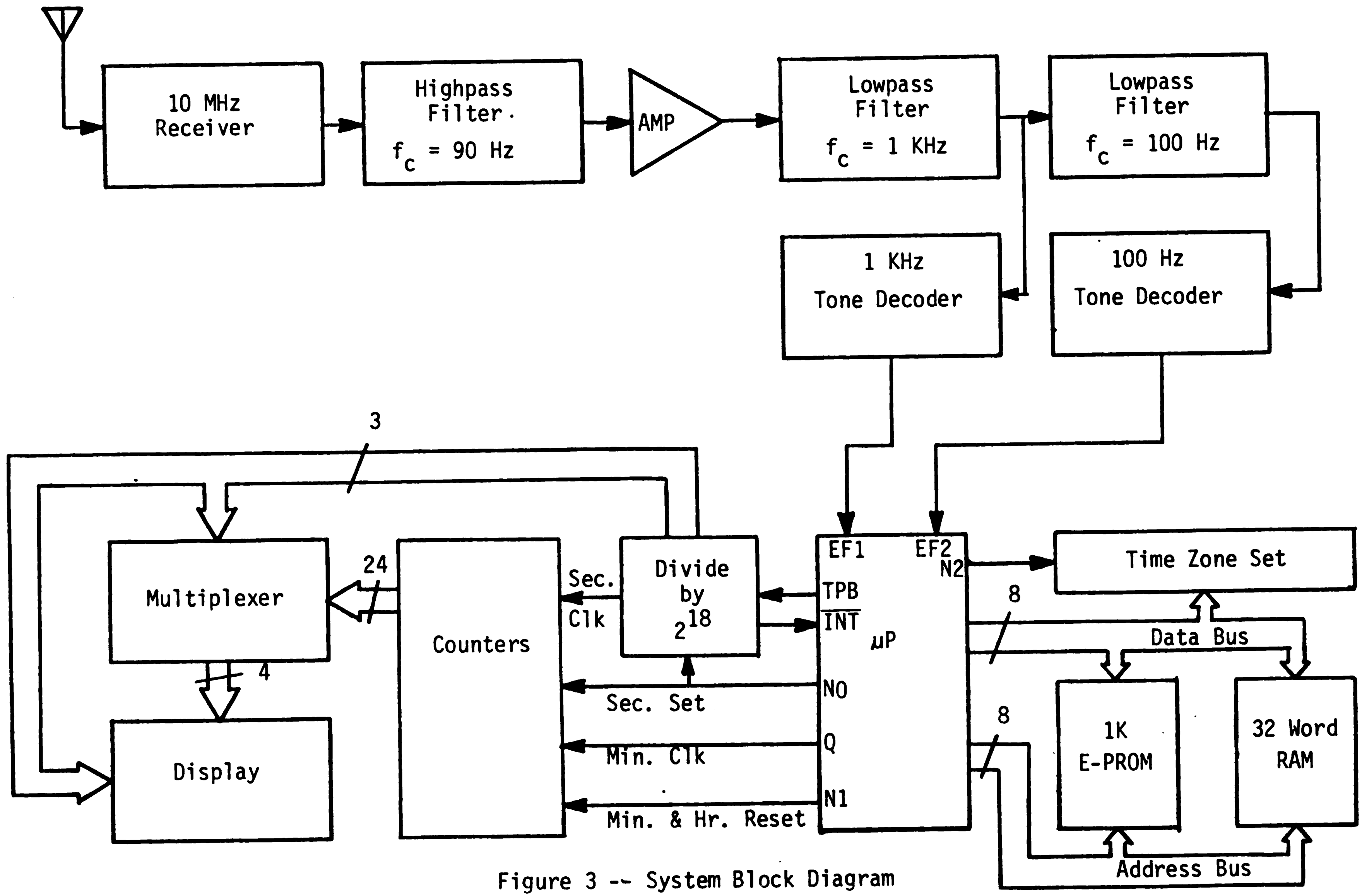


Figure 3 -- System Block Diagram

For each pulse on the minutes clock input the minutes counters are incremented by one. Sixty pulses on this line will return the minutes counters to zero and increment the hours counters by one. Thus the μP sets the time by serially outputing the time data onto this line.

2.3 Receiver and Signal Conditioning Subsystem

The receiver converts the 10 MHz WWV signal down to baseband. The audio output from the receiver is first passed through a highpass filter with a low frequency cutoff of 90 Hz that blocks the large DC component which would overload the next stage. The signal is then amplified to a level acceptable to drive the tone decoders.

Tone decoders employ phase locked loops (PLL) which are known to have the undesirable tendency to lock on to harmonics of the center frequency of the voltage controlled oscillator (VCO).[(3)] Thus the signal is passed through lowpass filters designed to sufficiently attenuate the harmonics before it reaches to the tone decoders.

A tone decoder is a device which will output a logic signal which state depends on whether a tone within its bandwidth is present at its input. The bandwidth of the tone decoder is made to be very small so essentially it will detect only one frequency. Two tone decoders are needed in this system, one to detect the 100 Hz tone carrying the encoded time and the other to detect the 1 KHz tone that signifies the start of each minute.

2.4 Microprocessor Subsystem

The tone decoder outputs are fed into the μP's flag inputs. Through the software program, contained in the eraseable programmable read only memory (E-PROM), the μP determines the length of the pulses on the flags, decodes the time information, and outputs this data to the clock. The μP uses a random access memory (RAM) to temporarily store data.

The time encoded on WWV is referenced to the prime meridian, therefore a set of switches are interfaced with the μP through which the time zone correction (in BCD) can be made. Table 1 shows how the switches should be set for various time zones in the continental United States.

Table 1 -- Time Zone Setting

TIME ZONE	SWITCHES							
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
Eastern Daylight	on	on	off	on	on	on	on	on
Eastern Standard Central Daylight	off	on	off	on	on	on	on	on
Central Standard Mountain Daylight	on	off	off	on	on	on	on	on
Mountain Standard Pacific Daylight	off	off	off	on	on	on	on	on
Pacific Standard	on	on	on	off	on	on	on	on

CHAPTER III

HARDWARE ORGANIZATION

3.1 Analog Hardware Implementation

The analog portion of the system is divided into three major sections: the receiver, filter, and tone decoder. Each section contains a detailed circuit description followed by a schematic diagram of the final circuit.

3.1.1 Receiver

After doing extensive research on the design of RF receivers it was decided that the actual receiver design was beyond the scope of this thesis. The system requirements of the receiver are simply that it must receive the 10 MHz WWV signal from a relatively small telescoping antenna and produce a usable baseband signal. Another restriction put on the receiver, and the most difficult to achieve, is that it must use relatively modern and readily available components. A design suggested by the staff of *73 Magazine* in their December 1977 edition was the only one found that came close to meeting the design constraints.[4]

A block diagram of the single conversion, superheterodyne receiver is illustrated in Figure 4. The RF amplifier buffers the antenna and provides some signal gain into the tuned circuit. A high Q tuned circuit preceding the mixer passes the 10 MHz WWV signal and attenuates the image frequency which in this case is 9.090 MHz. The 10 MHz signal

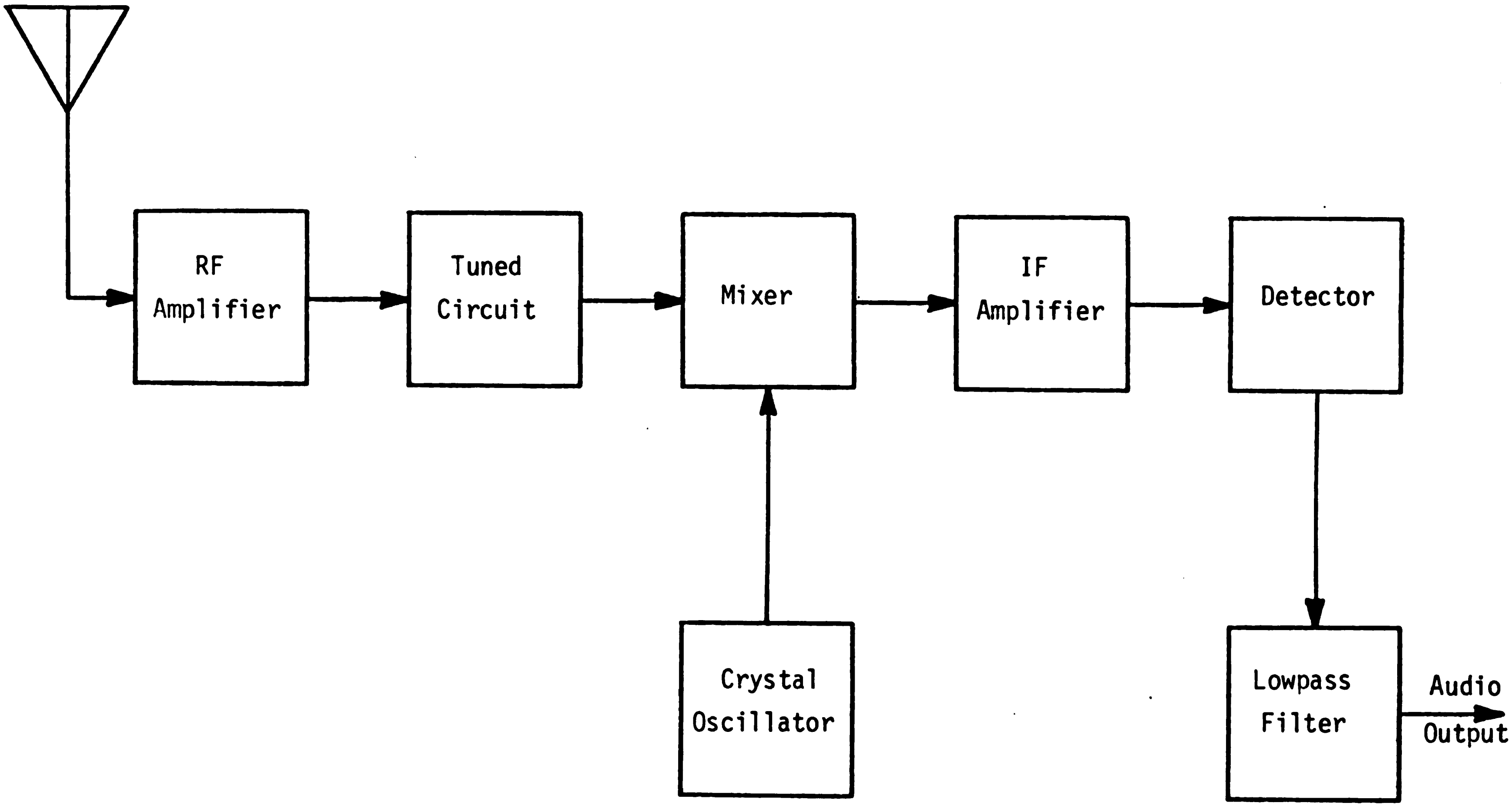


Figure 4 -- Receiver Block Diagram

and the 9.545 MHz signal from the crystal oscillator are mixed to produce the sum and difference frequencies of 19.454 MHz and 455 KHz respectively. The IF amplifier amplifies and bandpass filters the 455 KHz signal. It provides the signal with approximately 60 db of gain within the 3 KHz passband. The 455 KHz signal is finally envelope detected, lowpass filtered and presented at the audio output.

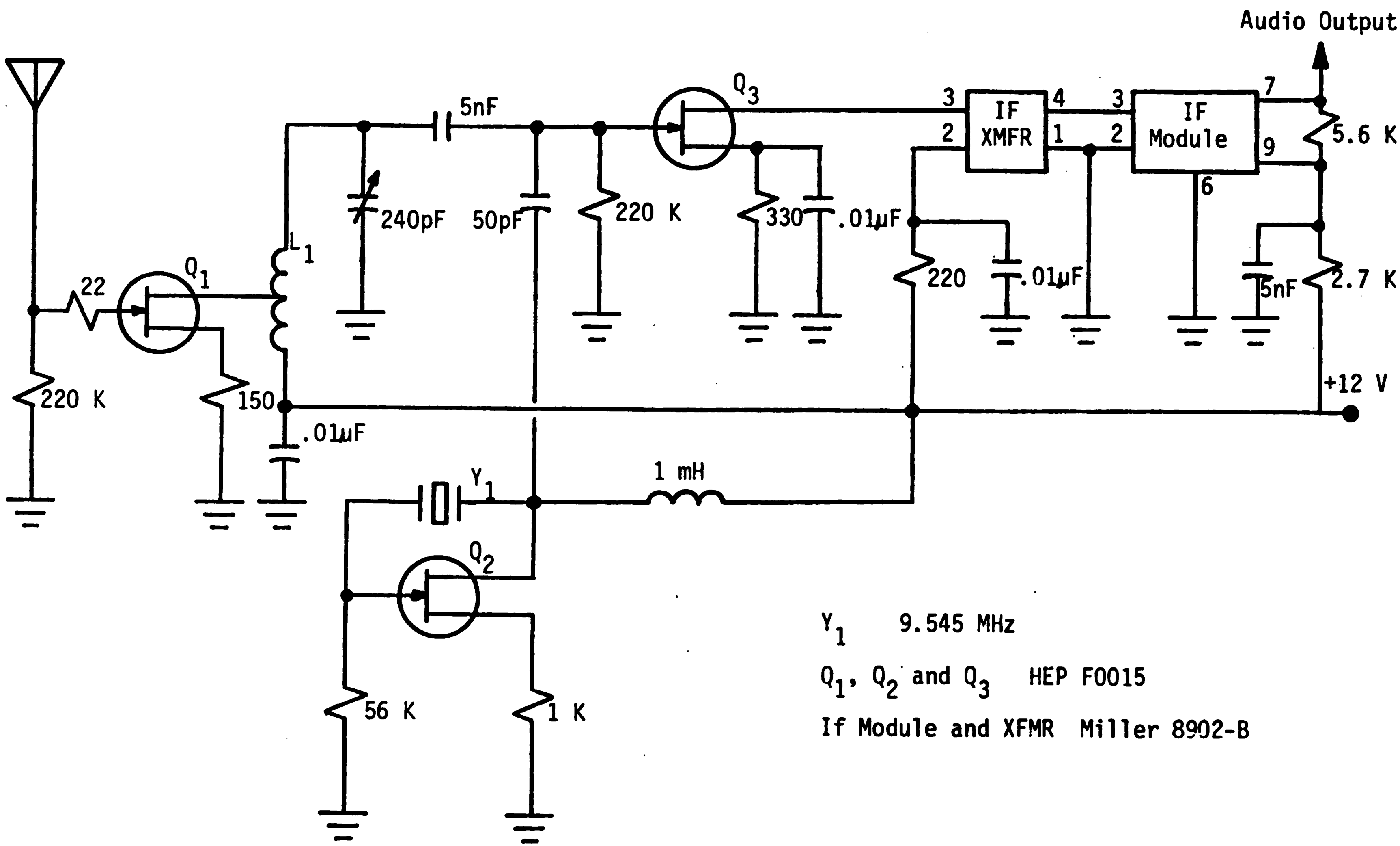
The receiver schematic is shown in Figure 5. The three transistors are idential n-channel JFET's. Q1 is the RF amplifier. Q2 and Y1 form the crystal oscillator. Q3 performs as the mixer. The heart of the receiver is the commercially available, prepackaged IF strip which provides most of the gain and filtering to the signal. A diode detector and lowpass filter are contained on the IF strip. The inductor L1 is 30 turns of #26 wire on a ¼ inch form tapped at 15 turns. The antenna is a 51 inch telescoping whip type. The IF transformer and IF module together form J. W. Miller part 8902-B.

3.1.2 Filters

The requirements of the lowpass filters are that they must pass the desired tone frequency (f_0) and sufficiently attenuate its harmonics ($2f_0$, $3f_0$, etc.). Consider the lowpass transfer function

$$T_{LP}(s) = \frac{K}{s^2 + \frac{\omega c}{Q} s + \omega_c^2}$$

where $\omega_c = 2\pi f_0$. The normalized log magnitude of this transfer function is given by:



Y_1 9.545 MHz

Q_1, Q_2 and Q_3 HEP F0015

If Module and XFMR Miller 8902-B

Figure 5 -- Receiver Schematic

$$LM\left[\frac{T_{LP}(j\omega)}{K}\right] = 20\log\left(\left(1-\frac{\omega^2}{\omega_c^2}\right)^2+\left(\frac{2Q}{\omega_c}\right)^2\right)^{\frac{1}{2}}$$

Q is choosen to be one so that the filter will not ring and cause spurious outputs from the tone decoder. With Q equal to one the log magnitude can be evaluated at $\omega = \omega_c$ and $\omega = 2\omega_c$. When this is done it is found that the log magnitude of the transfer function at $2\omega_c$ is approximately 8 db down from ω_c which was experimentally found to be a sufficient attenuation.

The Sallen and Key lowpass filter in Figure 6 has the transfer function

$$T_V(s) = \frac{\dfrac{k}{R_1R_2C_1C_2}}{s^2 + s\left(\dfrac{1}{R_1C_1}+\dfrac{1}{R_2C_1}+\dfrac{1-k}{R_2C_2}\right)+\dfrac{1}{R_1R_2C_1C_2}}$$

where $k = 1 - \frac{r_2}{r_1}$.(5) Comparing T_V to T_{LP} the design equations are found to be

$$\omega_c = \left(\frac{1}{R_1R_2C_1C_2}\right)^{\frac{1}{2}} \qquad Q = \frac{\omega_c}{\dfrac{1}{R_1C_1}+\dfrac{1}{R_2C_1}+\dfrac{1-k}{R_2C_2}} \qquad K = \frac{k}{R_1R_2C_1C_2}$$

Choosing $C_1 = C_2 = 1$ and $R_1 = R_2$ and substituting into the design equations yields

$$R_1 = R_2 = \frac{1}{\omega_c} \qquad k = 3 - \frac{1}{Q} \qquad r_2 = r_1\left(2 - \frac{1}{Q}\right)$$

The highpass filter was devised by first designing a Sallen and Key lowpass filter with the desired cutoff frequency (f_c = 90 Hz) and then making a lowpass to highpass transformation. This transformation

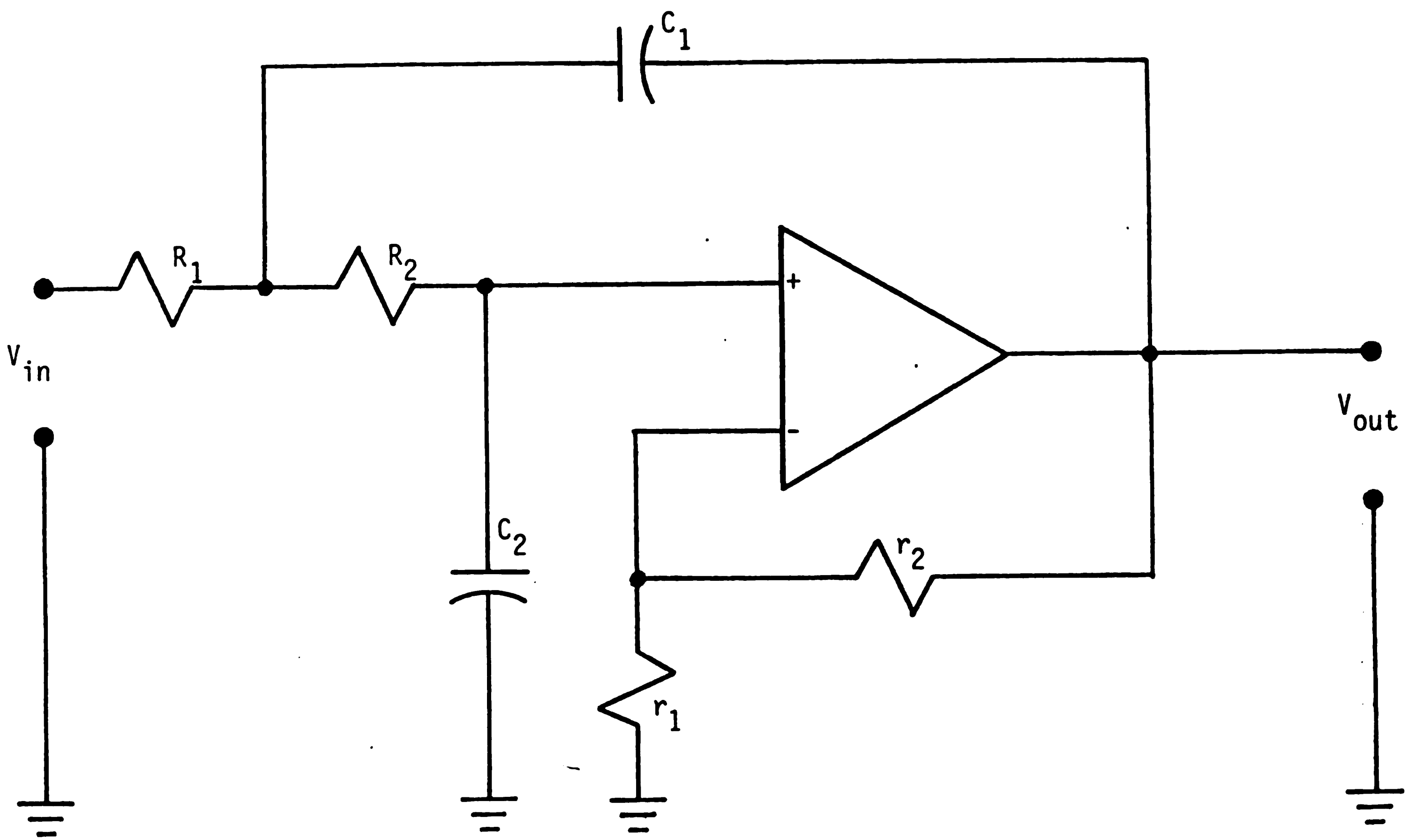


Figure 6 -- Sallen and Key Lowpass Filter

is made by replacing the resistors in the lowpass circuit by capacitors of value $1/R\omega_c$ and replacing the capacitors in the lowpass circuit by resistors of value $1/C\omega_c$ where $\omega_c = 2\pi f_c$. The highpass filter obtained by this transformation has the same cutoff frequency and rolloff characteristics as its lowpass counterpart.

After determining the nominal element values from the design equations, impedance scaling is used to obtain practical element values. Using this method, an impedance scaling factor is choosen; all of the nominal resistor values are multiplied by this factor and all of the nominal capacitor values are divided by this factor to get the final element values.

The circuit for the filter section is illustrated in Figure 7. The overall gain of the section is adjusted by varying R_4 to obtain the optimum signal level to drive the tone decoders. The cutoff frequency of the first lowpass filter is 1 KHz and f_c = 100 Hz for the second one. The large resistor values, which would be unacceptable for use with 741 op amps, can be used with the CA3140 op amps because of their extremely high input impedance (1.5 teraohms).

3.1.3 Tone Decoders

A block diagram of a 567 IC tone decoder is illustrated in Figure 8. The 567 consists of a current controlled oscillator (CCO), a phase detector, and a quadrature phase detector (QPD). The CCO and phase detector are connected in a typical phase locked loop (PLL) configuration. When a tone within the PLL's bandwidth (capture range) is present at the input the PLL will go into lock and output a 90 degree phase shifted version of the tone to the QPD. The QPD multiplies the input signal with the output of the PLL and produces a DC voltage which drives the

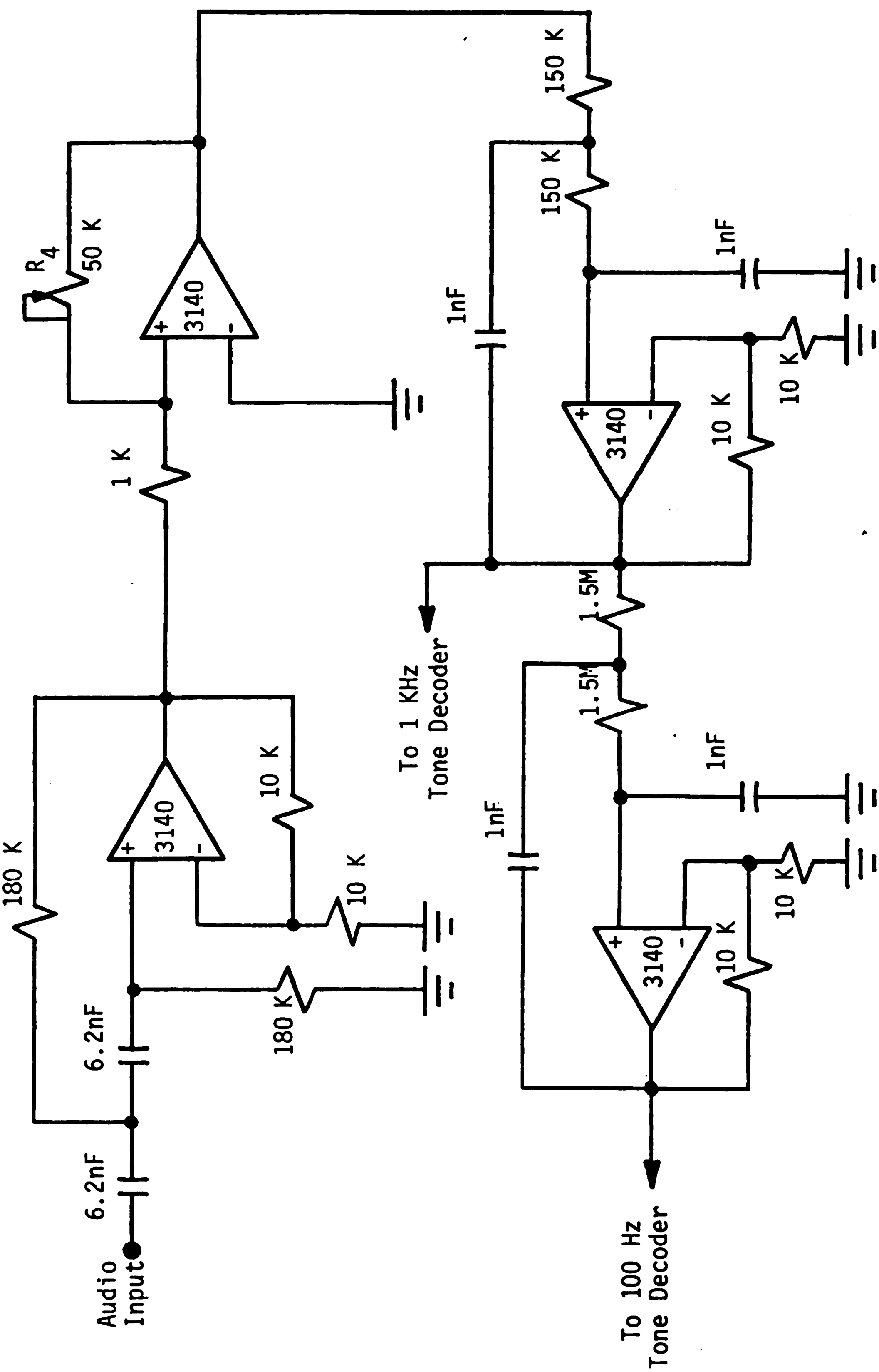


Figure 7 -- Filter Circuit Diagram

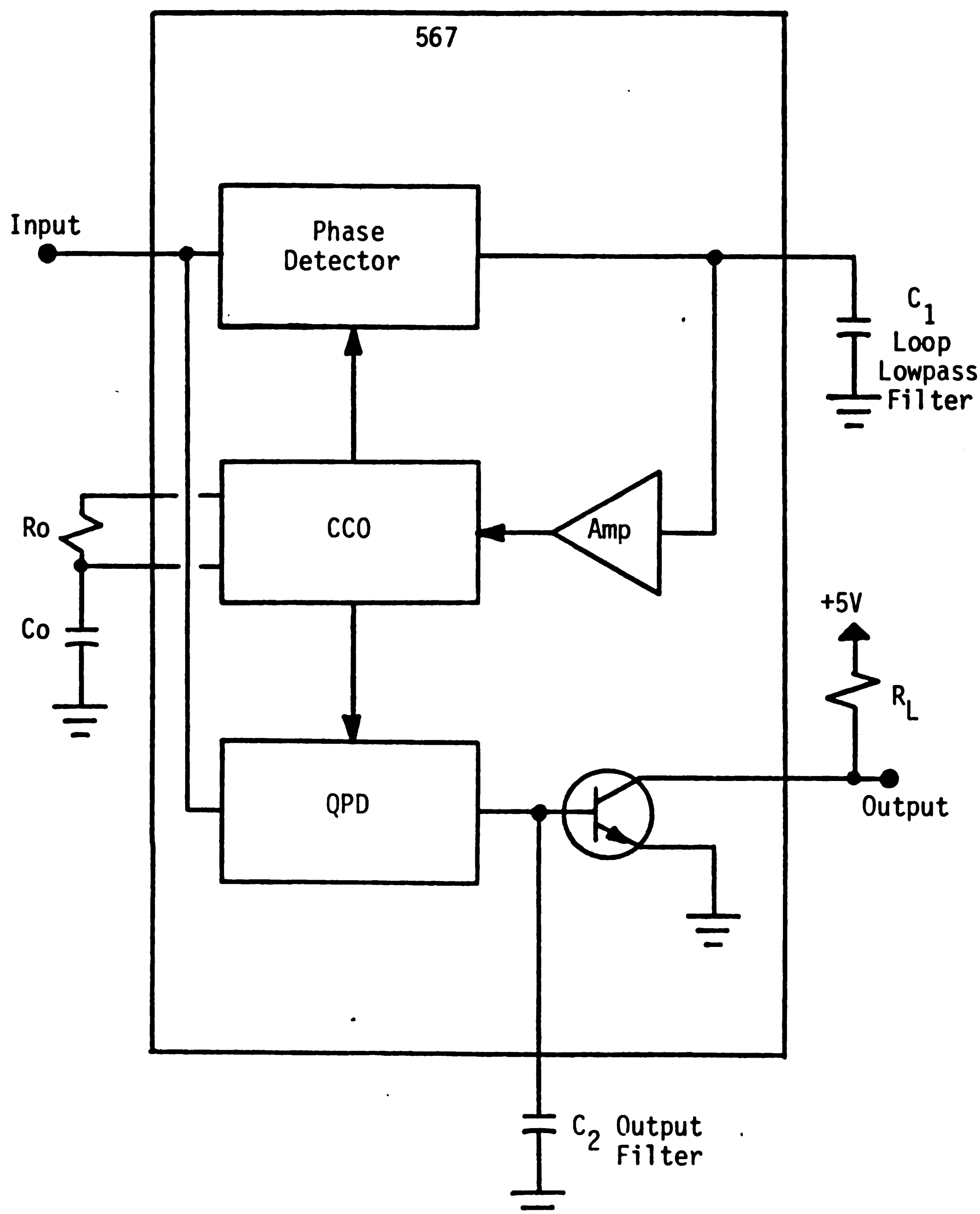


Figure 8 -- 567 Tone Decoder

output transistor into saturation. If the tone at that input is outside the PLL's bandwidth the QPD will multiply the input with the CCO's center frequency and produce an AC voltage which is effectively shorted to ground by the output filter capacitor and keeps the output transistor in the off state. When the transistor is off no current flows through R_L and the output is at a logical high voltage. A saturated transistor has approximately a 0.2 volt drop across it bringing the output down to a logical low voltage.

The CCO's center frequency is set by choosing appropriate values for R_0 and C_0. The value of C_1, the loop lowpass filter capacitor, determines the bandwidth of the PLL. An important design trade-off exists in choosing the value of C_1. Increasing the value of C_1 decreases the bandwidth of the PLL which is highly desirable but it also increases the amount of time required to lock on to the signal. Since the leading edge of each of the tone bursts signify the start of a second, the lock-up time should be as short as possible to enable the μP to accurately set the seconds. Another design trade-off appears in determining the value of C_2 the output filter capacitor. Increasing the value of C_2 increases the ability of the tone decoder to reject noise and close out-of-band signals but also increases the turn-off time. The turn-off time is critical when measuring the length of the tone bursts and therefore should be made as short as possible.

A method of obtaining a fast response, narrow band tone decoder is shown in Figure 9.[3] This method utilizes two 567 tone decoders each of which has a wide bandwidth and therefore a fast response. One 567 has a center frequency a little above and the other a little below the desired tone to be detected. The two outputs are OR'ed (logically

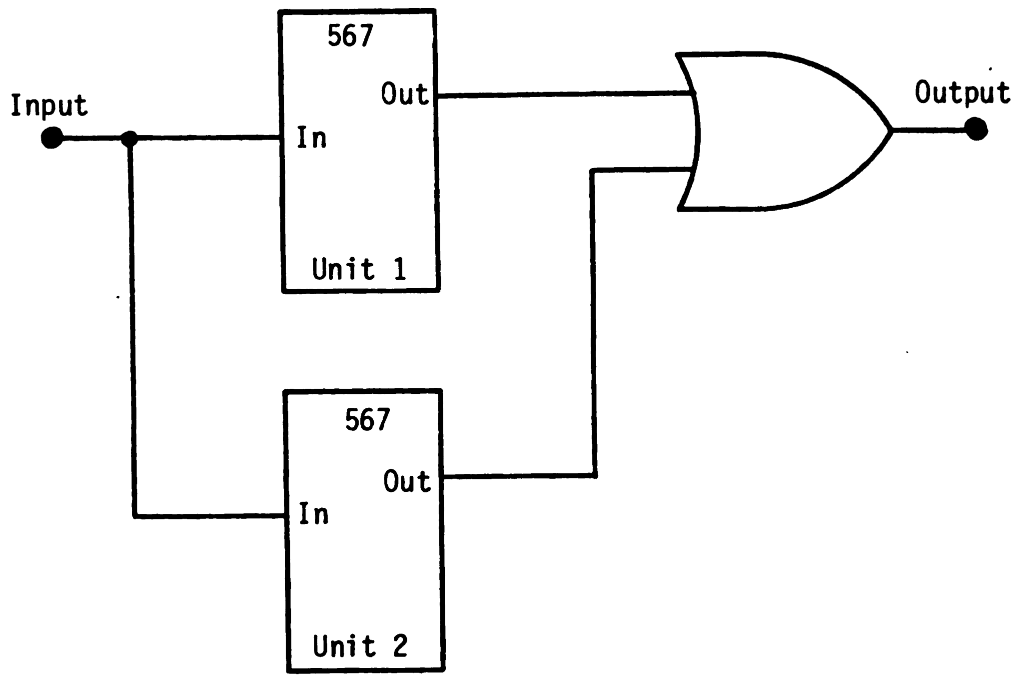


Figure 9 -- Fast Response, Narrow Band Tone Decoder

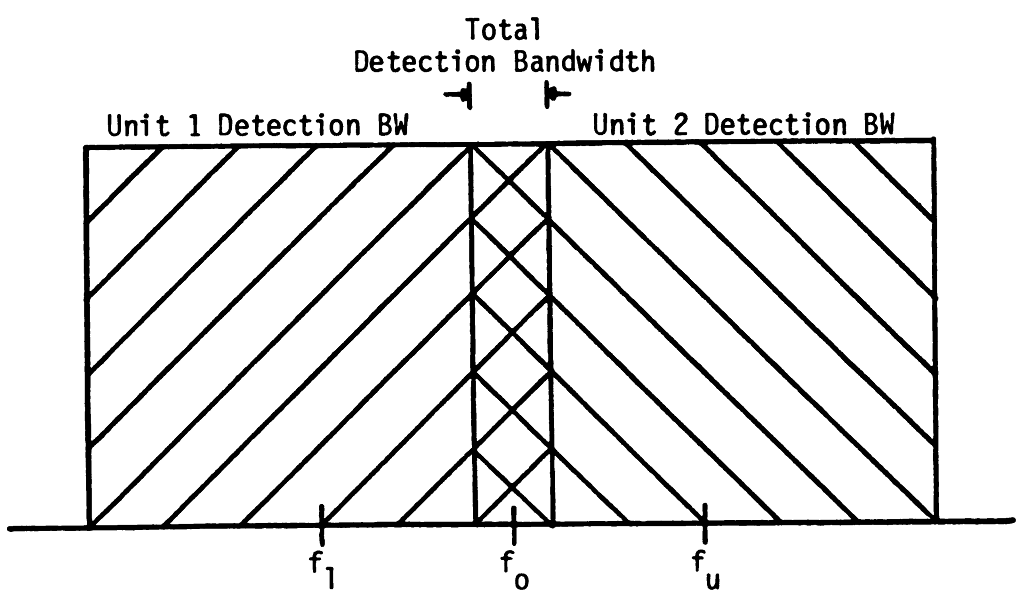


Figure 10 -- Dual Tone Decoder Detection Bandwidth

AND'ed) to produce a tone decoder with a bandwidth equal to the overlap of the individual 567's bandwidths (Figure 10). Note that the OR function is used because of the negative logic outputs of the 567's (i.e. a tone present equals a logic zero).

One small problem with this design is that the bandwidth of the 567's decrease as the signal level decrease below 200 mV. If this should occur there may be no overlap of the two bandwidths causing the desired tone to be rejected. So effort must be made to keep the signal level above this threshold.

Two of these fast response, narrow band tone decoders are used in this system: one to decode the 100 Hz tone and the other for the 1 KHz tone. Each decoder uses an XR 2567 IC which contains two independent 567's. The schematic of the tone decoding section of the system with appropriate component values is illustrated in Figure 11.

3.2 Digital Hardware Implementation

CMOS digital logic is utilized throughout the digital portion of the system because of its low power consumption and wider variety of logic functions available on IC's in comparison with other logic families. Although most CMOS logic can operate anywhere in the range from 3 to 18 volts, one IC, namely the E-PROM, requires 5 volts; therefore, to conserve on the number of power supplies, all the logic operates off of 5 volts.

3.2.1 Microprocessor

The μP used in this system is the RCA CDP1802 COSMAC microprocessor.[6] The CDP1802 was selected for the following reasons: CMOS

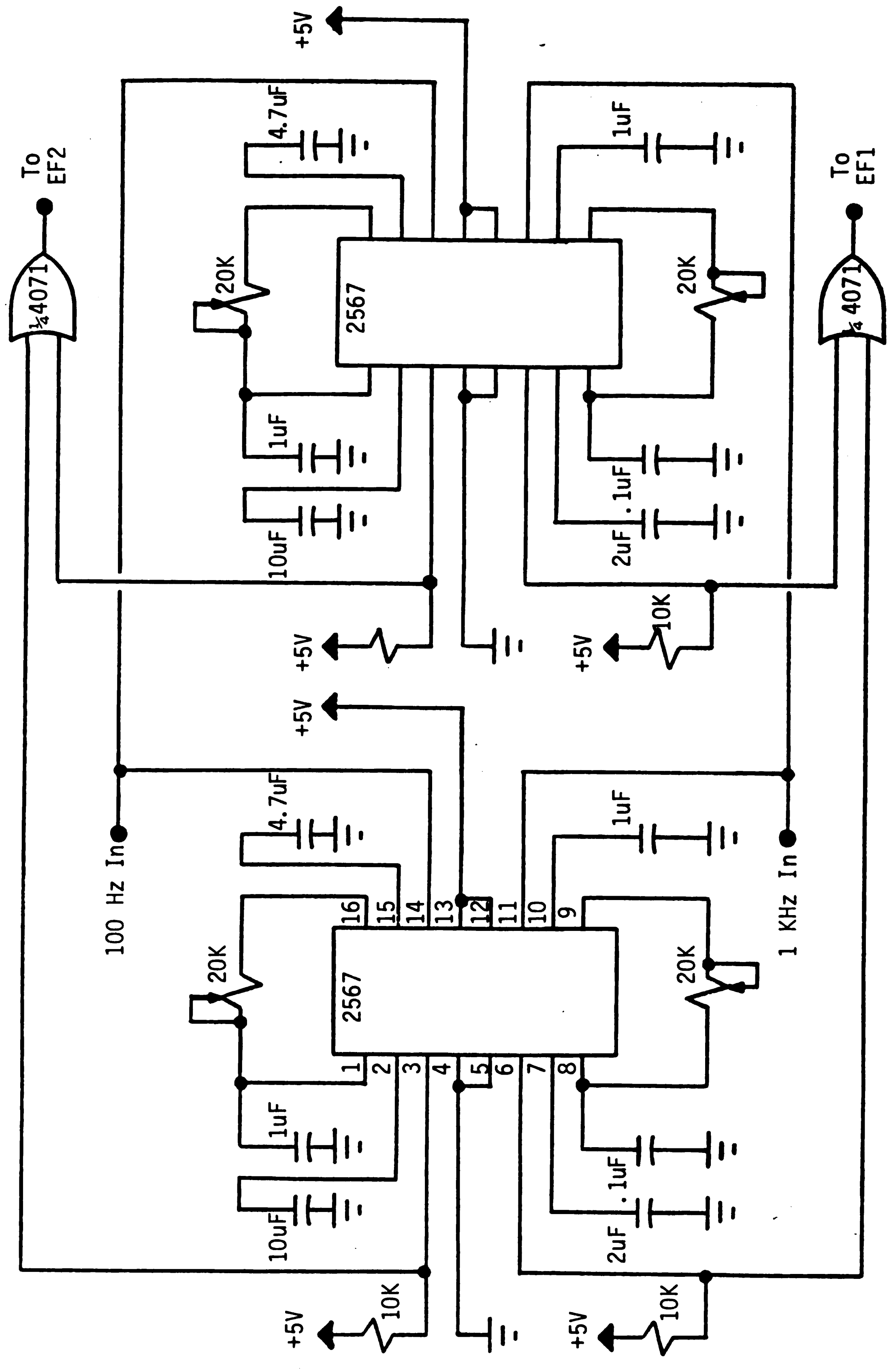


Figure 11 -- Tone Decoder Circuit Diagram

logic, powerful instruction set, and single power supply. A pin-out of the CDP1802 is provided in Figure 12. The speed of the uP is determined by the frequency of the crystal connected between the CLOCK and $\overline{\text{XTAL}}$ inputs. This frequency was choosen to be 2.097152 MHz (2^{21} Hz) because it is easily divided down to provide a 1 Hz signal for the clock.

Figure 13 shows the circuit for the microprocessor section of the system. Connected to the bi-directional data bus are: a 1024 by 8 bit E-PROM, a 32 by 8 bit RAM, and an interfaced set of switches. Addresses 0000_{16} to $03FF_{16}$ access the E-PROM and 0400_{16} to $041F_{16}$ access the RAM. When addressing memory the μP puts the upper 8 bits of the address on the address lines first. The 4042 4 bit latch is used to decode the upper part of the address. The three upper address bits needed for this memory structure are latched in the 4042 by the trailing edge of TPA (a timing signal from the μP).

The state of the switches is read when the μP executes an INP 4 instruction. The execution of this instruction causes the N2 line to go high which disables the memory and turns on the 4066 bilateral switches. With the bilateral switches on, the switches S1 to S8 are connected to the data bus. Because of the pull-up resistors on the data bus, when a switch is "off" the data line will be a logical high level. A switch being "on" shorts the data line to ground and puts it at a logical zero level.

The connection of C_1 and R_1 to the $\overline{\text{CLEAR}}$ control line causes the μP to reset when power is applied to the system.

Figure 12

CDP1802 Pin-Out

CDP1802

	CLOCK	1	40	Vdd	
CONTROL	$\overline{\text{WAIT}}$	2	39	$\overline{\text{XTAL}}$	
CONTROL	$\overline{\text{CLEAR}}$	3	38	$\overline{\text{DMA IN}}$	
	Q	4	37	$\overline{\text{DMA OUT}}$	
STATE CODES	SC1	5	36	$\overline{\text{INTERRUPT}}$	
STATE CODES	SC0	6	35	$\overline{\text{MWR}}$	
	$\overline{\text{MRD}}$	7	34	TPA	TIMING PULSES
DATA BUS	BUS 7	8	33	TPB	TIMING PULSES
DATA BUS	BUS 6	9	32	MA7	MEMORY ADDRESS
DATA BUS	BUS 5	10	31	MA6	MEMORY ADDRESS
DATA BUS	BUS 4	11	30	MA5	MEMORY ADDRESS
DATA BUS	BUS 3	12	29	MA4	MEMORY ADDRESS
DATA BUS	BUS 2	13	28	MA3	MEMORY ADDRESS
DATA BUS	BUS 1	14	27	MA2	MEMORY ADDRESS
DATA BUS	BUS 0	15	26	MA1	MEMORY ADDRESS
	Vcc	16	25	MA0	MEMORY ADDRESS
I/O COMMANDS	N2	17	24	$\overline{\text{EF1}}$	I/O FLAGS
I/O COMMANDS	N1	18	23	$\overline{\text{EF2}}$	I/O FLAGS
I/O COMMANDS	N0	19	22	$\overline{\text{EF3}}$	I/O FLAGS
	Vss	20	21	$\overline{\text{EF4}}$	I/O FLAGS

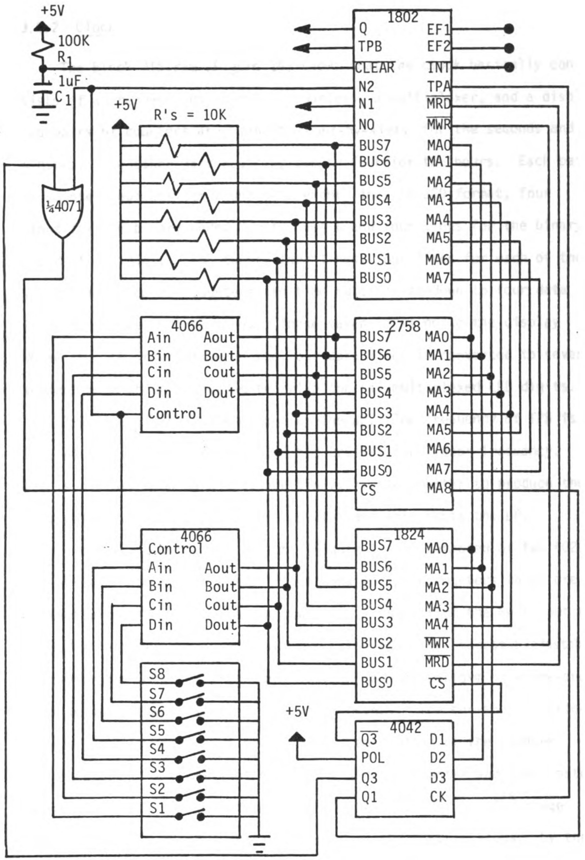


Figure 13 -- Microprocessor Circuit Diagram

3.2.2 Clock

The block diagram (Figure 14) shows that the clock basically consists of a frequency divider, six counters, a multiplexer, and a display. Two pairs of counters are used to count-by-sixty for the seconds and minutes. The other pair count-by-twenty-four for the hours. Each pair of counters outputs its count onto eight lines in BCD format, four lines for the binary coded "units" digit and four lines for the binary coded "tens" digit. The twenty-four lines, four lines for each of the six digits, from the counters are time multiplexed down to four data lines and three control lines. These seven lines go to the display where the BCD information on the four data lines is converted to seven-segment code which is needed to drive the six multiplexed LED digits.

TPB is a timing pulse output by the µP. The frequency of TPB is 262.144 KHz (2^{18} Hz) which is 1/8 the crystal oscillator frequency. TPB is divided down by a 18 stage binary ripple counter to produce the 1 Hz pulse train that clocks the counter and interrupts the µP.

The frequency divider circuit (Figure 15) is composed of two 4020's and a 4047. The 4020's are 14 stage binary ripple counters which are connected to produce a 18 stage counter. A pulse from the NO output of the µP will reset the counter to zero. The 4047 is a monostable/astable multivibrator which is programmed (hard wired) to perform as a one-shot with an output pulse width of 250 microseconds. The one-shot is triggered by the trailing edge of the 18^{th} stage output of the counter. The Q output of the one-shot clocks the seconds counter and the $\overline{Q}$ output goes to the $\overline{\text{INTERRUPT}}$ input on the µP. The 4^{th}, 5^{th}, and 6^{th} stage outputs from the ripple counter are used as the control signals by the multiplexer.

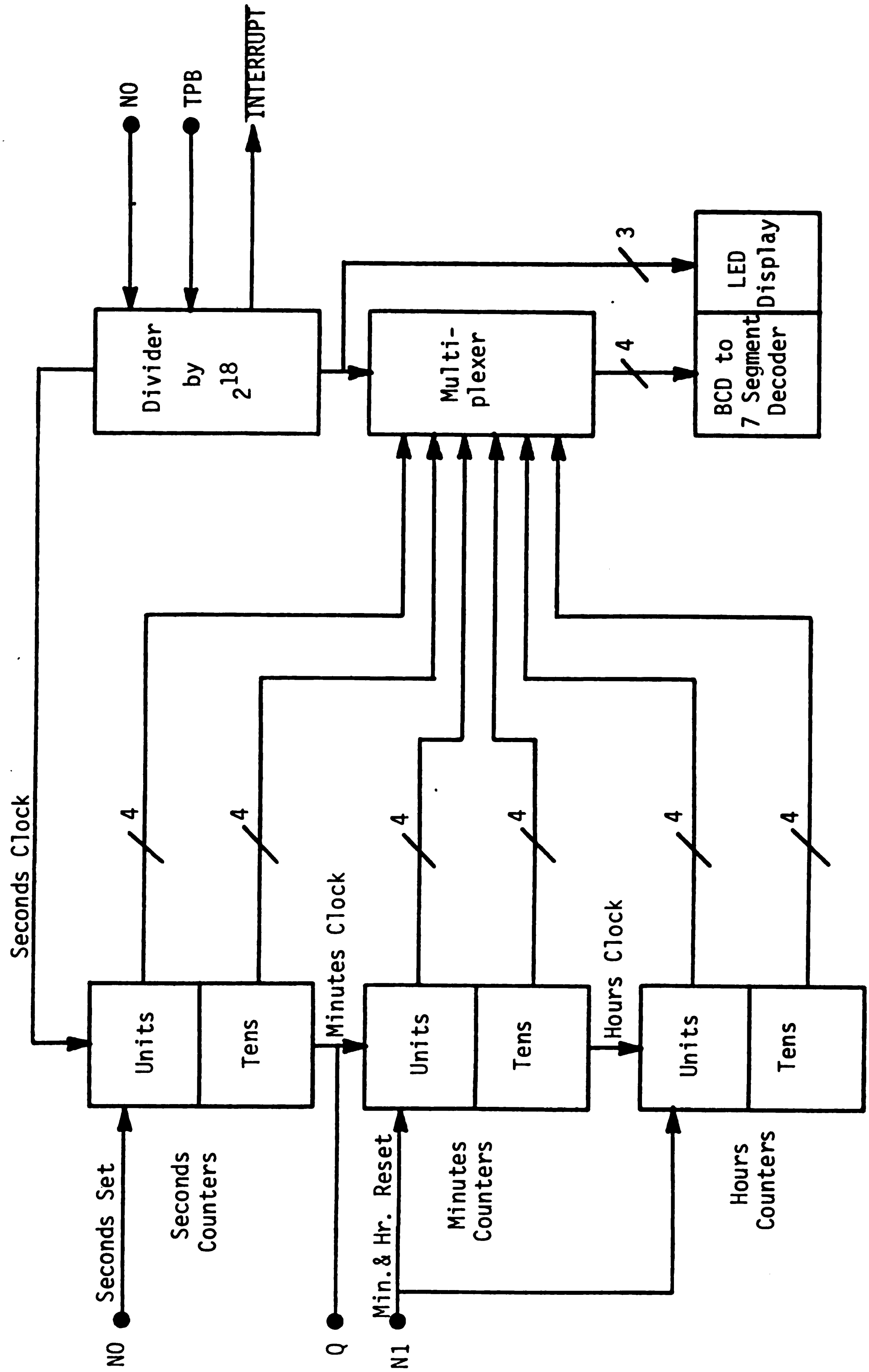


Figure 14 -- Clock Block Diagram

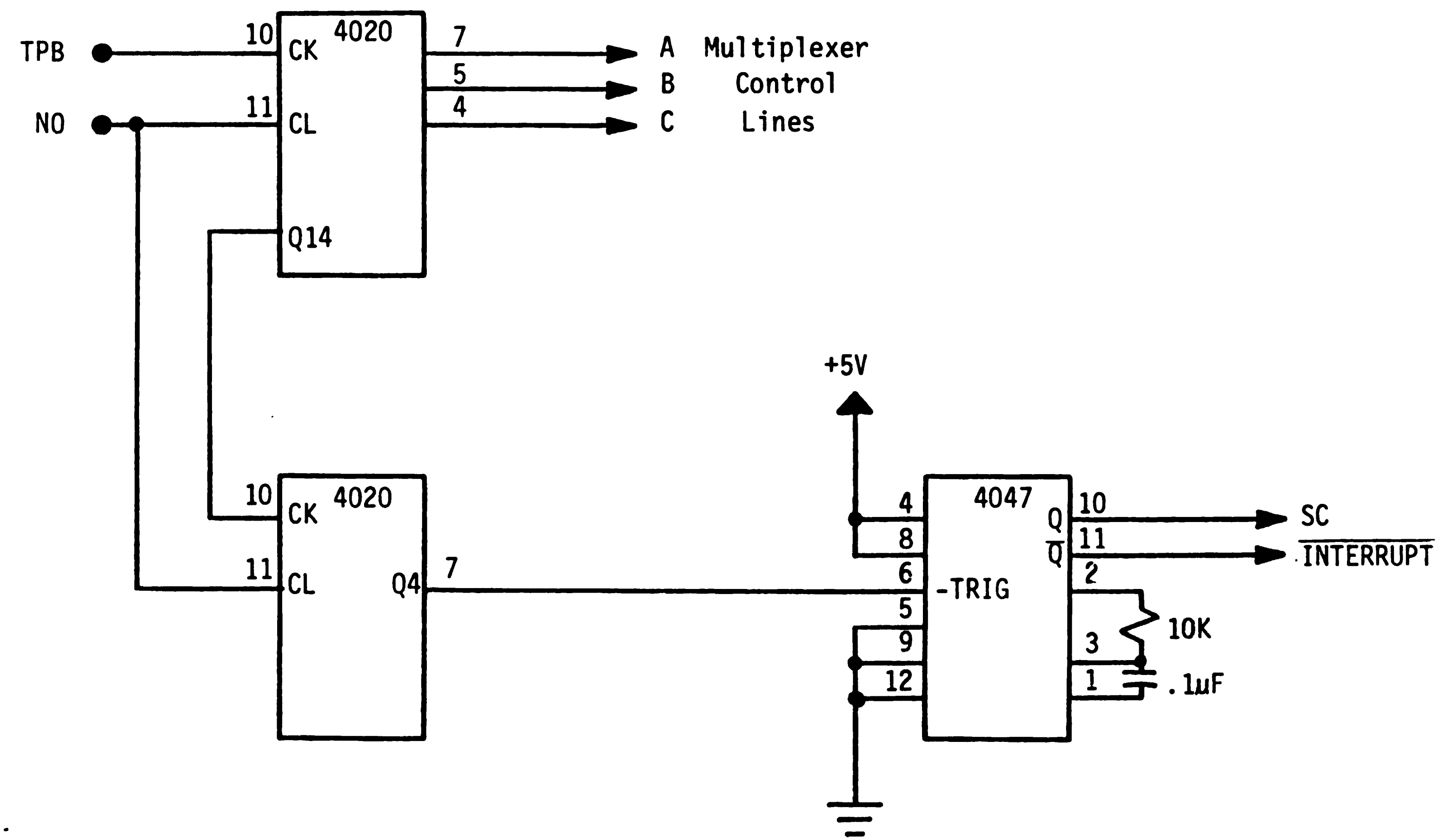


Figure 15 -- Frequency Divider Circuit Diagram

The three 4518's in the clock circuit (Figure 16) are dual decade counters. Q4A is connected to Enable B for each of the 4518's so the B counter will increment every time the A counter cycles from 9 to 0. The ANDing of Q2B and Q3B resets both the A and B counters of the seconds and minutes 4518's and clocks the following 4518 to produce the count by sixty function. The ANDing of Q3B and Q2B resets both the A and B counters of the hours 4518 to produce the count by twenty-four function. A pulse on the NO line from the μP will first reset the seconds counters then on the trailing edge increments the seconds A counter to one. The NO line and S3B are ANDed to clock the minutes A counter when the seconds set pulse occurs between the 40th and 59th second. Pulses on the Q line from the μP will also clock the minutes. A pulse on the μP's N1 line will reset both the hours and the minutes.

Four 4051 8 to 1 multiplexers compose the multiplexer circuit (Figure 17). Only six of the eight lines are used on each of the 4051's. The three control lines come from the frequency divider circuit.

The BCD information on the four lines from the multiplexers is converted to seven segment code by the 4511 in the display circuit (Figure 18). The outputs of the 4511 go through current limiting resistors then on to segment inputs of the multiplexed common-cathode LED display. The 4028 BCD to decimal decoder is used to decode the three control lines. The outputs of the 4028 sequentially turn the transistors on and off and hence the LED digits.

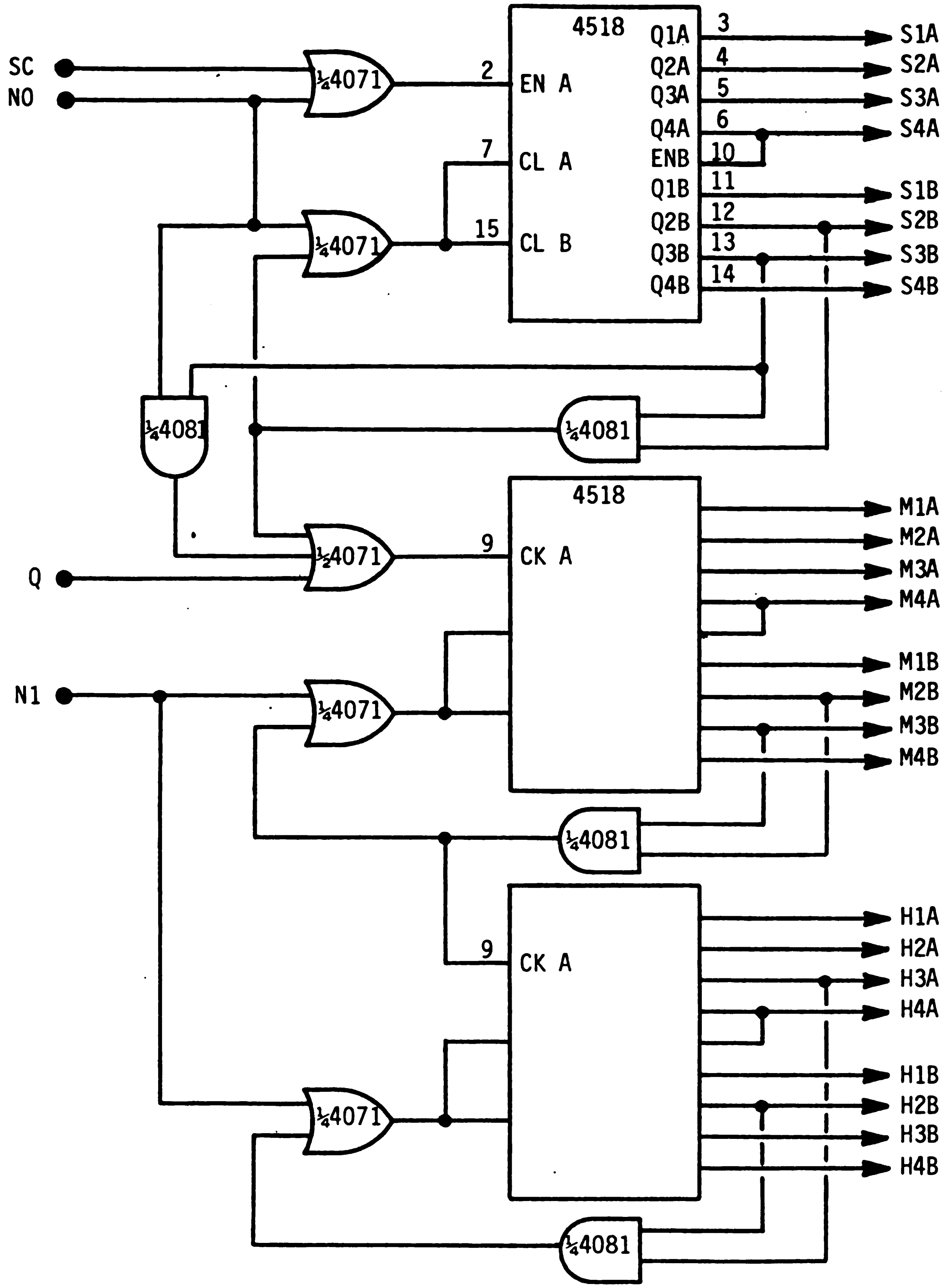


Figure 16 -- Clock Circuit Diagram

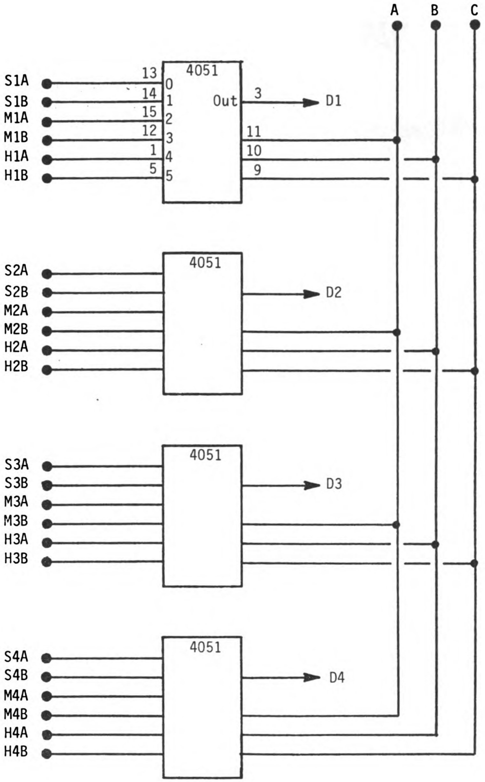


Figure 17 -- Multiplexer Circuit Diagram

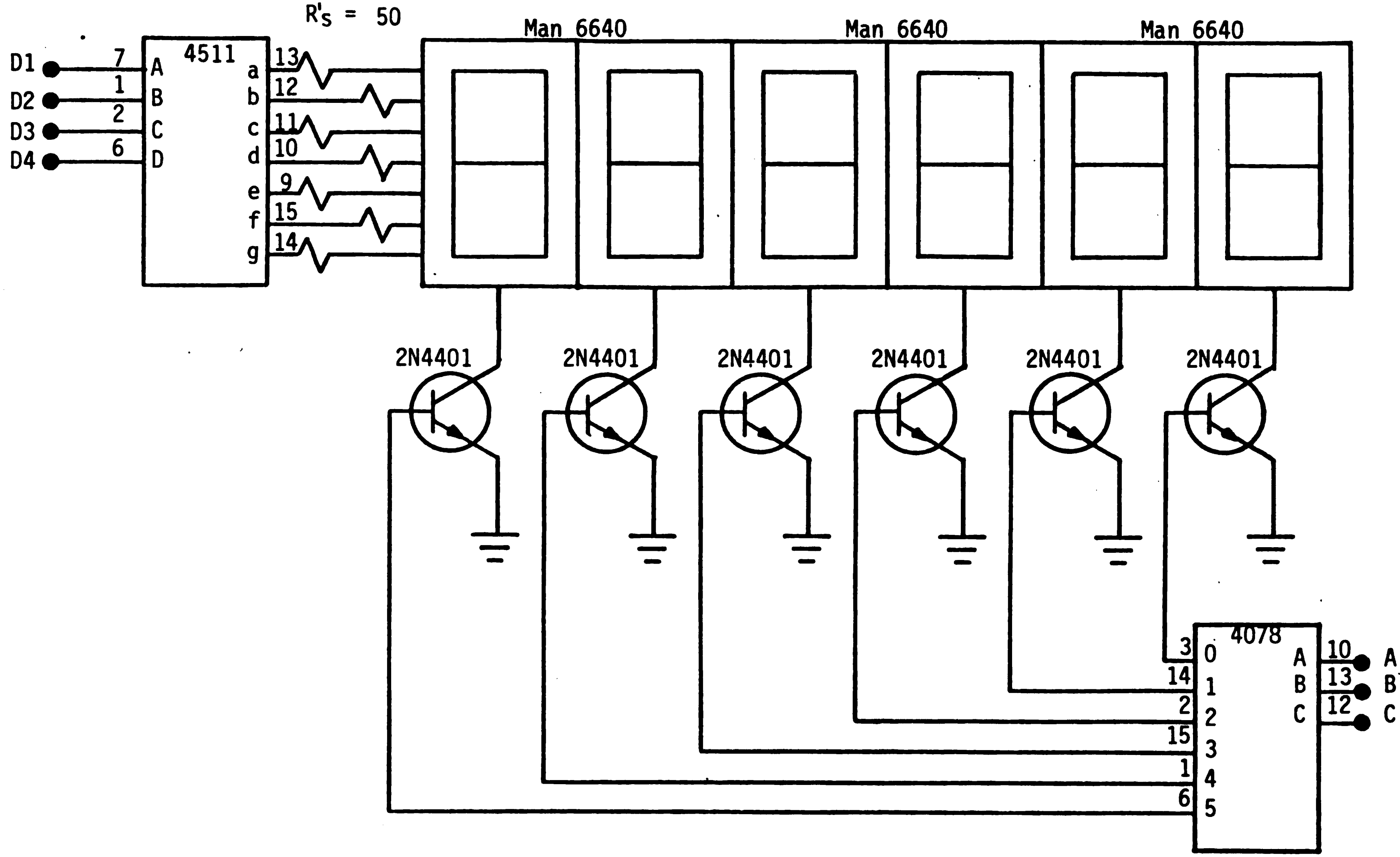


Figure 18 -- Display Circuit Diagram

CHAPTER IV

SOFTWARE ORGANIZATION

4.1 Introduction

The μP operation is controlled by a sequence of instructions (program) stored in the E-PROM. The program was written in COSMAC assembly language and assembled and simulated with the COSMAC Software Development Package on the MSU CDC6500 computer.[7] The object code generated by the cross-assembler was loaded into the E-PROM via a ROM programmer. The Appendix contains the assembly language listing of the uP program.

The μP program contains a number of timing loops where a counter is incremented each time through the loop. The number in the counter is related to a second by the following equation:

$$1 \text{ second} = \frac{\text{clock frequency}}{(16)(\text{No. of instructions in loop})} = \frac{131072}{\text{No. of instructions in loop}}$$

4.2 Seconds Set Routine

Figure 19 shows the logic flow of the initial portion of the program. On power-up the μP resets the clock's counters to 00:00:01 and enters the seconds set routine. First the μP waits for the 1 KHz tone and then upon reception enters a timing loop. The timing loop determines whether the 1 KHz tone is the WWV signal or noise triggering the tone decoder. If the 1 KHz tone is present for at least 0.7 seconds and the 100 Hz tone is present for no more than 25 ms during the 0.8

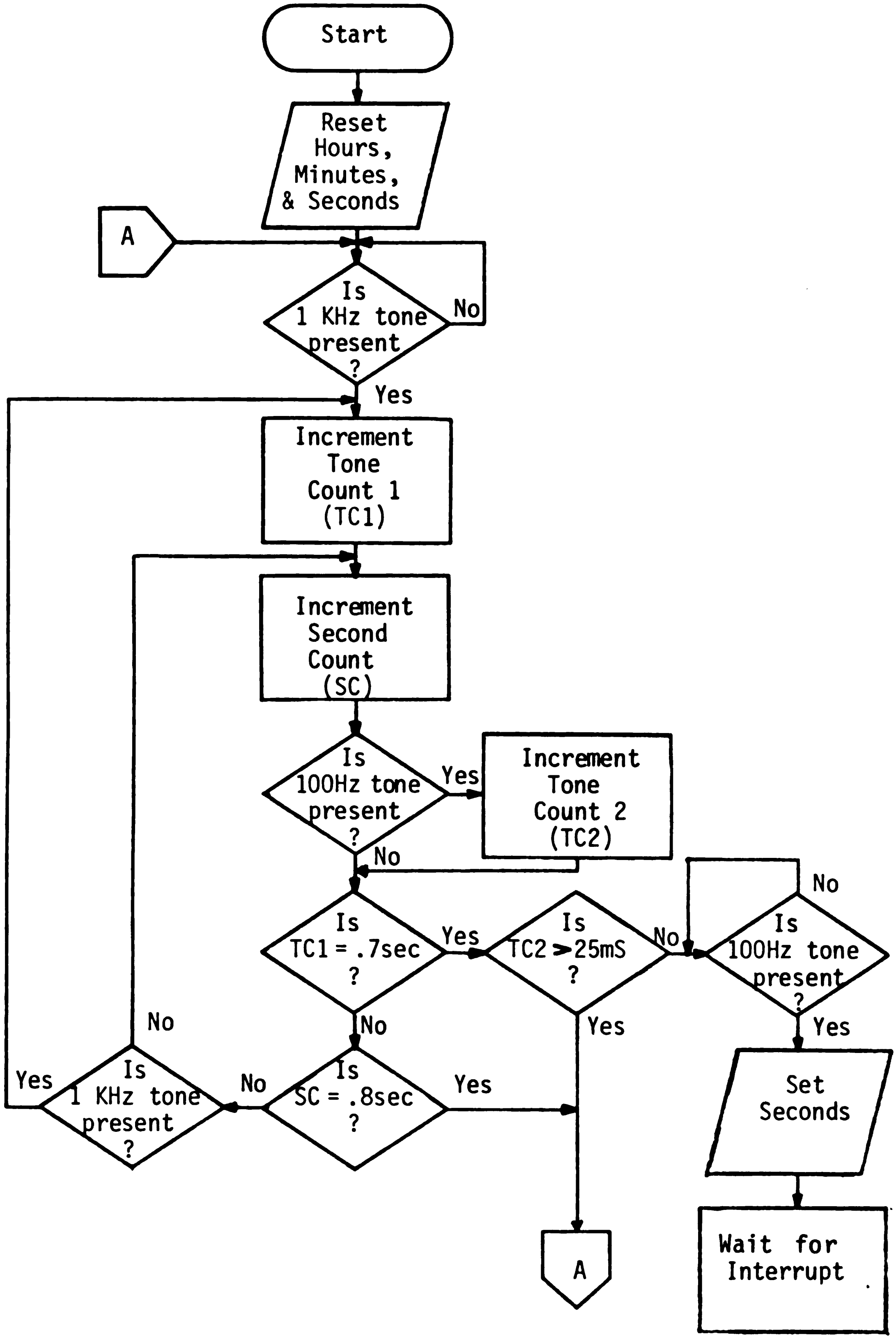


Figure 19 -- Seconds Set Routine

seconds after entering the loop the µP will set the seconds of the clock to one immediately after the next 100 Hz tone is detected. If the above conditions are not met the µP goes back and waits for the next 1 KHz tone to occur. After setting the seconds the µP idles, waiting for an interrupt.

4.3 Interrupt Routine

The interrupt routine measures the length of the 100 Hz tone bursts, thus determining if they are coded zeros, ones or markers and stores this information in RAM for future use by the coder routine. The interrupt pulses from the divider circuit, which was synchronized to WWV in the seconds set routine, occurs at the start of each second. Every time an interrupt pulse occurs when the µP is waiting for an interrupt the interrupt routine is executed.

The logic flow of the interrupt routine is illustrated in Figures 21 through 23. The three pieces of information used to ascertain the pulse type are determined by the three timing loops. These three pieces of information are: how long the 100 Hz tone was present during the intervals 0.0 to 0.2 seconds (ZC), 0.2 to 0.5 seconds (OC), and 0.5 to 0.8 seconds (MC). Table 2 illustrates how the pulse type is determined by the three variables.

Once the pulse type is ascertained the remainder of the routine is devoted to decoding the time information. The data contained in the first three frames of the time code are stored in the three words record1, record2, and record3 as shown in Figure 20. The fifth pulse of the frame, which is always transmitted as a coded zero, is used as an error checking, control element. If the fifth pulse is not a coded

Table 2 -- Pulse Type Decoding Method

0.0 s < ZC ≤ 75 ms	0.0 s < OC ≤ 0.3 s	0.0 s < MC ≤ 0.3 s	error
75 ms < ZC ≤ 0.2 s	0.0 s < OC ≤ 0.1 s	0.0 s < MC ≤ 0.1 s	ZERO
75 ms < ZC ≤ 0.2 s	0.1 s < OC ≤ 0.3 s	0.0 s < MC ≤ 0.1 s	ONE
75 ms < ZC ≤ 0.2 s	0.1 s < OC ≤ 0.3 s	0.1 s < MC ≤ 0.3 s	MARKER
75 ms < ZC ≤ 0.2 s	0.0 s < OC ≤ 0.1 s	0.1 s < MC ≤ 0.3 s	error

Figure 20

Bit-Packing of Record

RECORD	9	8	7	6	4	3	2	1	No. of pulse in frame
	8	7	6	5	4	3	2	1	No. of bit in word

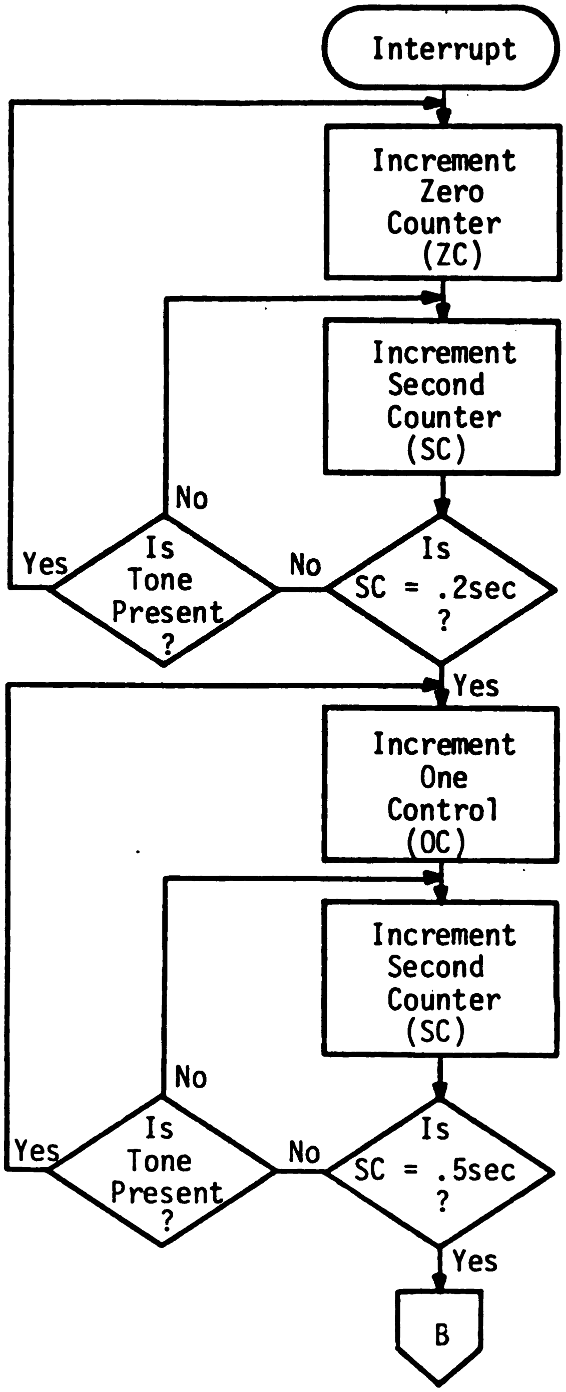


Figure 21 -- Interrupt Routine

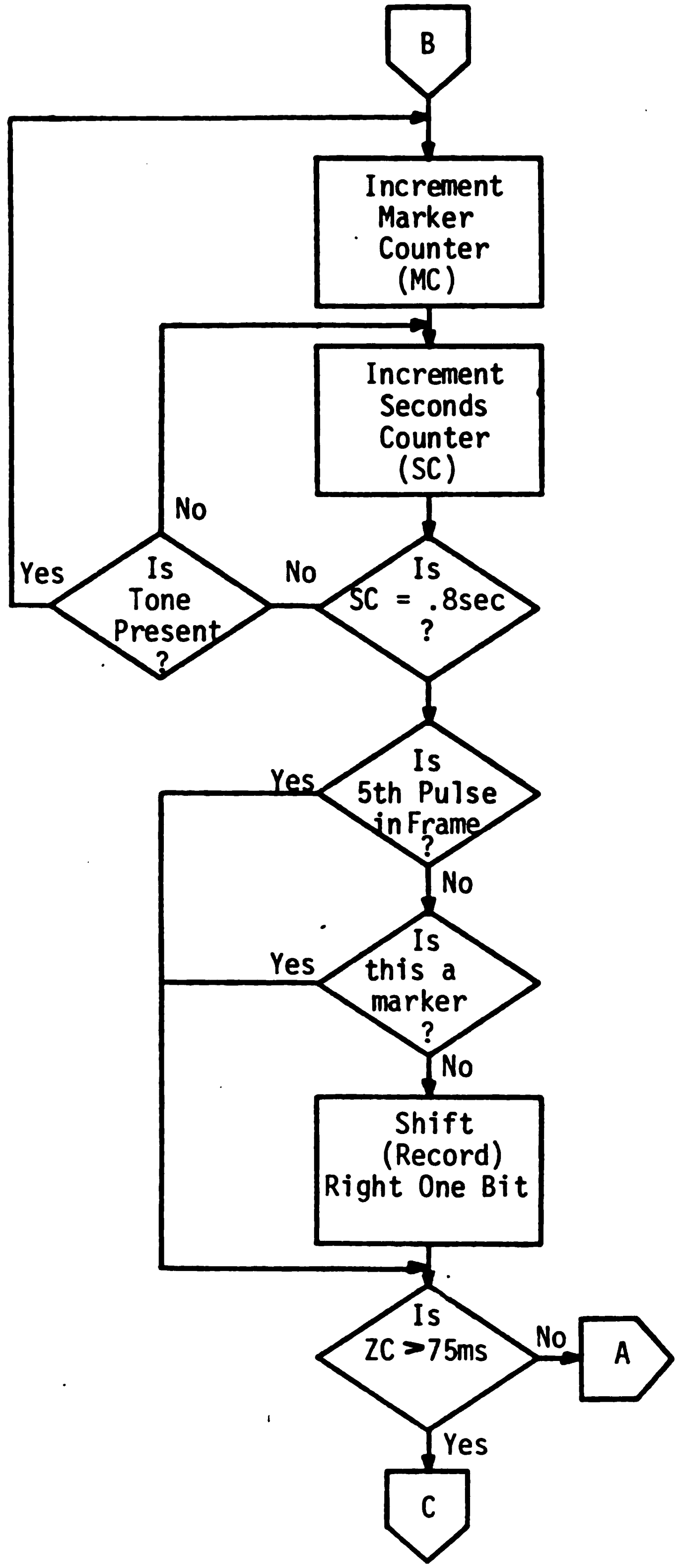


Figure 22 -- Interrupt Routine (Continued)

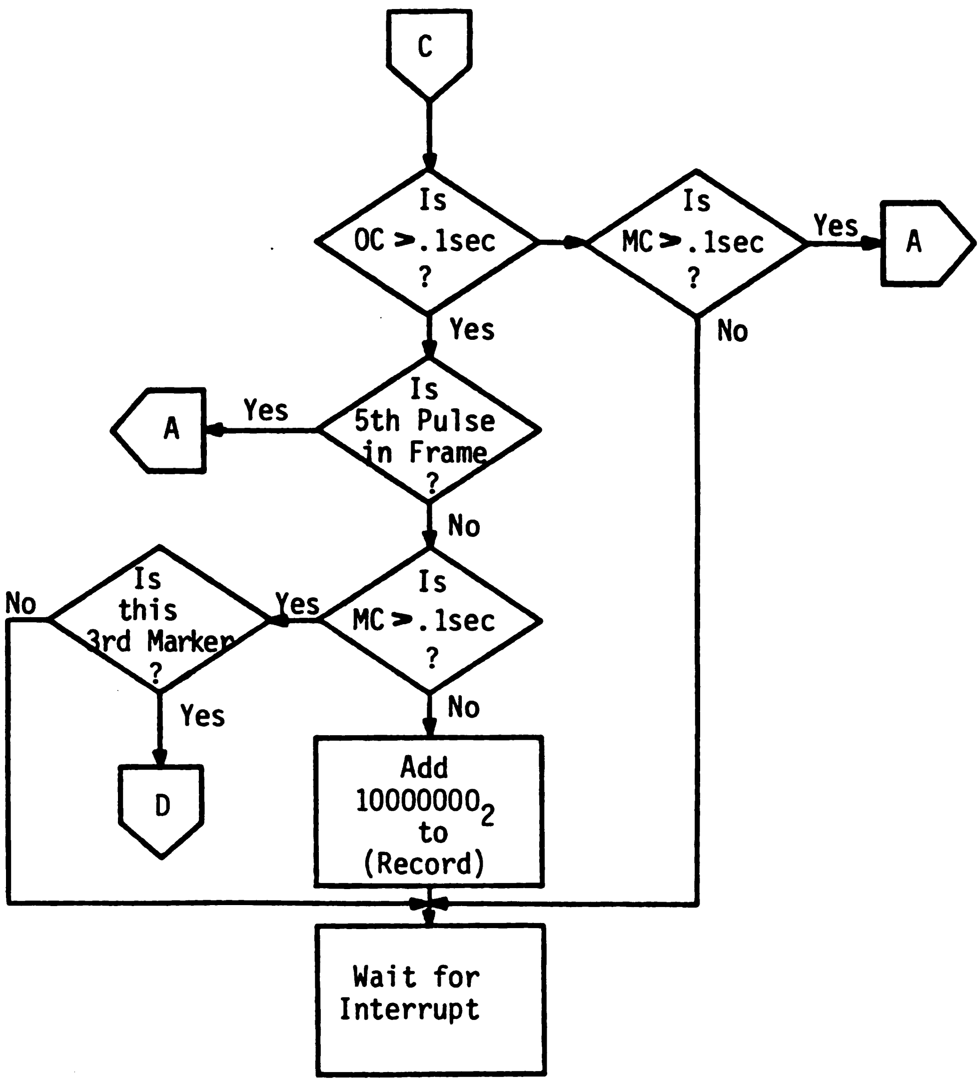


Figure 23 -- Interrupt Routine (Continued)

zero the μP goes back to the seconds set routine and waits for the start of the next minute. Because all the pertinent information is obtained in the first thirty seconds of the minute when the third marker is encountered the μP ignores the rest of the time code and executes the coder routine.

4.4 Coder Routine

The coder routine sets the hours and minutes with the time information obtained by the interrupt routine. Figure 24 illustrates the logic flow of the coder routine. The BCD time information in record2 and record3 is converted to straight binary and checked to see if it makes sense. The time is corrected for the difference in time zone and finally the clock is set with this information.

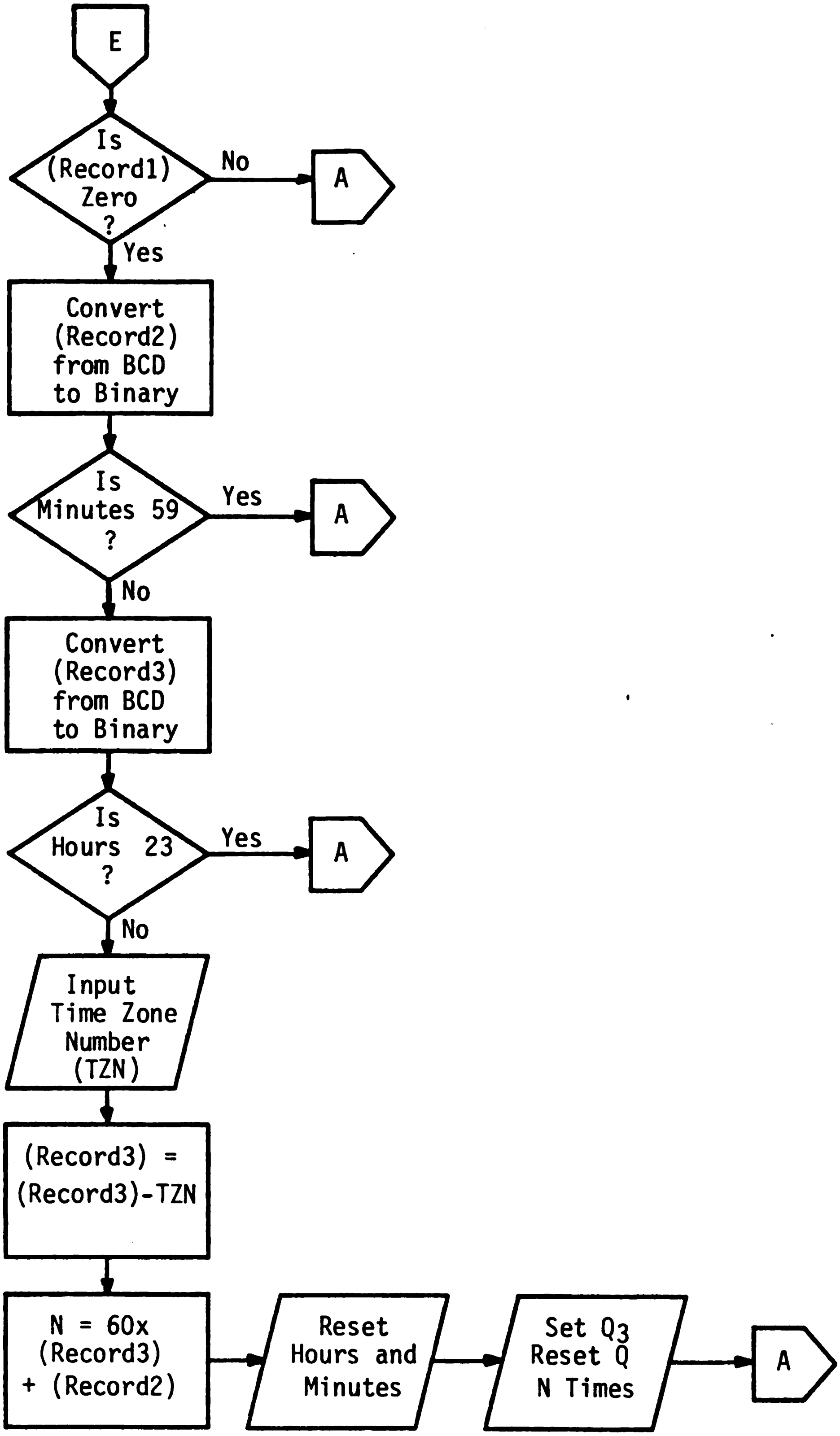


Figure 24 -- Coder Routine

CHAPTER V

CONCLUSIONS

The purpose of this thesis was the design and construction of an inexpensive, self-contained digital clock that would automatically set itself to the correct time using the WWV transmissions. This objective was attained.

The clock was constructed and tested by the author. The clock has one major problem, it will set the hours and minutes only in the hours between sunset and sunrise. There are two reasons for this problem. Firstly, and most importantly, the receiver is not very sensitive. During the testing of the receiver it was found that one of the transistors in the prepackaged IF module was bad and had to be replaced. There was no cross-reference for the original transistor, so the replacement transistor may not be a very close match and could reduce the gain and selectivity of the IF module. An improvement in the receiver performance may result if the IF module is replaced by a new one. Secondly, the MUF (maximum usable frequency) may not be as high as 10 MHz during the day when this unit was tested (April 1979).

Another section of the clock that could use improvement is the tone decoders. They are too sensitive to variations in the input signal voltage. A receiver with a good AGC (automatic gain control) circuit could remedy this problem. Perhaps a better solution to this problem would be to replace the filters and tone decoders by an analog microprocessor. The analog microprocessor could digitize the analog signal from the receiver, perform some digital bandpass filtering, and output digital signals indicating if either the 1 KHz or 100 Hz tones are present.

At night, while the clock would reset the seconds almost every minute, the hours and minutes would only set on the average of once every 15 to 20 minutes. This average was improved to once every 5 to 10 minutes when a Hewlett Packard amplifier with a gain of 26 db was inserted between the antenna and the receiver. About once every 20 times the clock set the hours and minutes it would set them to the wrong time. During the day (if the clock had set the previous night) the crystal oscillator kept the clock accurate to the second.

While the prototype of the clock cost about $150 in parts, a number of design changes could easily put the cost below $100. The whole clock section could be replaced by a single clock integrated circuit. The E-PROM, which is the most expensive IC in the device, could be replaced by a much less expensive mask-programmed ROM. It is the author's belief that a unit similar to this one could be manufactured and sold at the price of a moderately price clock radio.

APPENDIX

ASSEMBLY LANGUAGE PROGRAM LISTING

```
FL LOC  COSMAC CODE   SOURCE LINE
   0000 7100          START: DIS, X'00'    ..DISABLE INTERRUPTS.
F  0002 F800                 LDI  A.1(INT) ..LOAD ADDRESS OF
   0004 B1                   PHI  R1       ..INTERRUPT ROUTINE.
F  0005 F800                 LDI  A.0(INT)
   0007 A1                   PLO  R1
   0008 63                   OUT  3        ..RESET HR,MIN,AND SEC.
   0009 C4                   NOP
F  000A F800          ONEK:  LDI  A.1(REC) ..LOAD ADDRESS OF
   000C B2                   PHI  R2       ..DATA RECORD INTO
F  000D F800                 LDI  A.0(REC) ..THE X REGISTER.
   000F A2                   PLO  R2
   0010 F800                 LDI  X'00'
   0012 52                   STR  R2
   0013 B3                   PHI  R3       ..CLEAR SECOND COUNT.
   0014 A3                   PLO  R3
   0015 B4                   PHI  R4       ..CLEAR TONE RECEIVED
   0016 A4                   PLO  R4       ..COUNT.
   0017 B5                   PHI  R5       ..CLEAR 100 HZ RECEIVED
   0018 A5                   PLO  R5       ..COUNT.
   0019 F805                 LDI  X'05'
   001B A7                   PLO  R7       ..LOAD BIT COUNTER.
   001C F803                 LDI  X'03'
   001E A8                   PLO  R8       ..LOAD MARKER COUNTER.
   001F 3C1F          LOOP1: BN1  LOOP1    ..WAIT FOR 1 KHZ TONE.
   0021 14            OK1:   INC  R4
   0022 13            OK2:   INC  R3
F  0023 3D00                 BN2  OK3
   0025 15                   INC  R5
F  0026 3000                 BR   OK4
   0028 94            OK3:   GHI  R4
   0029 94                   GHI  R4
   002A 94            OK4:   GHI  R4       ..CHECK FOR MINIMUM
   002B FD1E                 SDI  X'1E'    ..TONE RECEIVED COUNT.
F  002D 3200                 BZ   RESET
   002F 93                   GHI  R3       ..CHECK TO SEE IF A
   0030 FD22                 SDI  X'22'    ..SECOND HAS GONE BY.
   0032 320A                 BZ   ONEK
   0034 3421                 B1   OK1
   0036 3022                 BR   OK2      ..NO TONE RECEIVED.
   0038 95            RESET: GHI  R5
   0039 FD02                 SDI  X'02'
   003B 3B0A                 BL   ONEK
   003D 3D3D          LOOP2: BN2  LOOP2    ..WAIT FOR 100HZ TONE.
   003F E0                   SEX  R0
   0040 61                   OUT  1        ..RESET SECONDS.
   0041 C4                   NOP
   0042 7000                 RET, X'00'    ..ENABLE INTERRUPTS.
   0044 00                   IDL           ..WAIT FOR INTERRUPT.
F  0045 F800          CODER: LDI  A.0(REC)
   0047 A2                   PLO  R2
   0048 72                   LDXA
   0049 3A0A                 BNZ  ONEK     ..CHECK FOR ZERO FIRST
   004B 8A            CDR1:  GLO  RA       ..RECORD.
   004C AB                   PLO  RB
   004D F80F                 LDI  X'0F'
   004F F2                   AND           ..GET LOWER 4 BITS OF
   0050 AA                   PLO  RA       ..RECORD.
   0051 F8F0                 LDI  X'F0'
   0053 F2                   AND           ..GET UPPER 4 BITS OF
   0054 F6                   SHR           ..RECORD.
   0055 52                   STR  R2
   0056 8A                   GLO  RA
```

```
  0057 F4                ADD
  0058 AA                PLO  RA
  0059 F0                LDX
  005A F6                SHR
  005B F6                SHR
  005C F6                SHR
  005D 52                STR  R2
  005E 8A                GLO  RA
  005F F4                ADD
  0060 F4                ADD
  0061 AA                PLO  RA
  0062 FD3B              SDI  59
  0064 3B0A              BL   ONEK         ..IF MINUTES > 59 TRY
  0066 60                IRX               ..AGAIN.
  0067 82                GLO  R2
F 0068 FD02              SDI  A.0(REC)+2
  006A 324B              BZ   CDR1
  006C 8A                GLO  RA
  006D FD17              SDI  23
  006F 3B0A              BL   ONEK         ..IF HOURS > 23 GO BACK.
  0071 62                OUT  2            ..RESET HRS AND MINS.
  0072 6C                INP  4            ..GET TIME ZONE.
  0073 8A                GLO  RA
  0074 F7                SM
F 0075 3300              BGE  CDR2
  0077 FC18              ADI  24
  0079 AA          CDR2: PLO  RA
F 007A 3200              BZ   CDR4
  007C F83C              LDI  60
  007E AC                PLO  RC
  007F 2C          CDR3: DEC  RC
  0080 7B                SEQ
  0081 7A                REQ
  0082 8C                GLO  RC
  0083 3A7F              BNZ  CDR3
  0085 2A                DEC  RA
  0086 8A                GLO  RA
  0087 3079              BR   CDR2
  0089 8B          CDR4: GLO  RB
  008A 320A              BZ   ONEK
  008C 2B                DEC  RB
  008D 7B                SEQ
  008E 7A                REQ
  008F 3089              BR   CDR4
F 0091 F800        INT:  LDI  A.0(INT0)
  0093 A0                PLO  R0
F 0094 F800              LDI  A.1(INT0)
  0096 B0                PHI  R0
  0097 D0                SEP  R0
  0098 F891        INT0: LDI  A.0(INT)
  009A A1                PLO  R1
  009B F800              LDI  X'00'
  009D B3                PHI  R3           ..CLEAR SECOND COUNT.
  009E A3                PLO  R3
  009F B4                PHI  R4           ..CLEAR ZERO COUNT.
  00A0 A4                PLO  R4
  00A1 B5                PHI  R5           ..CLEAR ONE COUNT.
  00A2 A5                PLO  R5
  00A3 B6                PHI  R6           ..CLEAR MARKER COUNT.
  00A4 A6                PLO  R6
  00A5 27                DEC  R7           ..DECREMENT BIT COUNTER.
```

```
    00A6 14          INT1:  INC   R4         ..INCREMENT ZERO COUNT.
    00A7 13          INT2:  INC   R3         ..INCREMENT SECOND COUNT
    00A8 83                 GLO   R3
    00A9 FDCC               SDI   X'CC'
    00AB 93                 GHI   R3
    00AC 7D0C               SDBI  X'0C'
F   00AE 3200               BZ    INT3       ..BRANCH IF SC = .2 SEC.
    00B0 35A6               B2    INT1       ..BRANCH IF 100 HZ.
    00B2 30A7               BR    INT2       ..SIGNAL NOT PRESENT.
    00B4 15          INT3:  INC   R5         ..INCREMENT ONE COUNT.
    00B5 13          INT4:  INC   R3         ..INCREMENT SECOND COUNT
    00B6 83                 GLO   R3
    00B7 FD00               SDI   X'00'
    00B9 93                 GHI   R3
    00BA 7D20               SDBI  X'20'
F   00BC 3200               BZ    INT5       ..BRANCH IF SC = .5 SEC.
    00BE 35B4               B2    INT3       ..BRANCH IF 100 HZ.
    00C0 30B5               BR    INT4       ..SIGNAL NOT PRESENT.
    00C2 16          INT5:  INC   R6         ..INCREMENT MARKER COUNT
    00C3 13          INT6:  INC   R3         ..INCREMENT SECOND COUNT
    00C4 83                 GLO   R3
    00C5 FD33               SDI   X'33'
    00C7 93                 GHI   R3
    00C8 7D33               SDBI  X'33'
F   00CA 3200               BZ    INT7       ..BRANCH IF SC = .8 SEC.
    00CC 35C2               B2    INT5       ..BRANCH IF 100 HZ.
    00CE 30C3               BR    INT6       ..SIGNAL NOT PRESENT.
    00D0 87          INT7:  GLO   R7
F   00D1 3200               BZ    INT8       ..DO NOT SHIFT IF BIT 5.
    00D3 96                 GHI   R6
    00D4 FD07               SDI   X'07'
F   00D6 3800               BL    INT8
    00D8 F0                 LDX
    00D9 F6                 SHR              ..SHIFT RECORD RIGHT
    00DA 52                 STR   R2         ..ONE BIT.
    00DB 94          INT8:  GHI   R4
    00DC FD05               SDI   X'05'      ..CHECK FOR MINIMUM ZERO
    00DE 330A               BGE   ONEK       ..COUNT.
    00E0 95                 GHI   R5
    00E1 FD07               SDI   X'07'      ..CHECK FOR MINIMUM ONE
F   00E3 3800               BL    INT9       ..COUNT.
    00E5 96                 GHI   R6
    00E6 FD07               SDI   X'07'      ..CHECK FOR MINIMUM
    00E8 330A               BL    ONEK       ..MARKER COUNT.
F   00EA C00000             LBR   END
    00ED 87          INT9:  GLO   R7
    00EE 320A               BZ    ONEK       ..START OVER IF BIT 5
    00F0 96                 GHI   R6         ..IS NOT ZERO.
    00F1 FD07               SDI   X'07'      ..CHECK FOR MINIMUM
F   00F3 3800               BL    INTA       ..MARKER COUNT.
    00F5 F880               LDI   B'10000000'
    00F7 F4                 ADD              ..ADD ONE TO RECORD.
    00F8 52                 STR   R2
F   00F9 C00000             LBR   END
    00FC 28          INTA:  DEC   R8
    00FD 88                 GLO   R8
    00FE 3245               BZ    CODER      ..BRANCH IF LAST MARKER
    0100 60                 IRX              ..START A NEW RECORD.
    0101 F805               LDI   X'05'
    0103 A7                 PLO   R7         ..LOAD BIT COUNTER.
    0104 E0          END:   SEX   R0
```

```
0105 7000            185         RET, X'00'        ..ENABLE INTERRUPTS.
0107 00              186         IDL               ..WAIT FOR INTERRUPT.
0400                 187         ORG   X'0400'
0400 00              188 REC:    DC    X'00'
0401                 189         END

02:44:39 05/08/79   SL86101     190 LINES PRINT.     6 PAGES PRINT.  COST AT RG3 I
```

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