DC CAPACITOR MINIMIZATION OF SINGLE PHASE POWER CONVERSION AND APPLICATIONS

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ABSTRACT

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Single-phase power conversion system such as PWM rectifier, grid connected PV inverter system, static synchronous compensator (STATCOM) can be implemented by an H-bridge inverter with a large electrolytic DC capacitor to absorb the ripple power pulsating at twice the line frequency (2ω ripple power). In order to reduce the capacitor size and to achieve high power density, a single phase DC-capacitor-less inverter with SVPWM control is proposed.

The DC-capacitor-less inverter consists of an H-bridge and an additional phase leg connected to an AC capacitor to absorb the 2ω ripple power. The H-bridge and the additional phase leg can be analyzed together as an unbalanced three phase system. By adopting SVPWM control and choosing the optimal AC capacitance and the voltage reference, the voltage and current stress of the switches can be minimized to the same as H-bridge circuit. Among the existing methods, the proposed method has the minimal energy storage capacitor and total device power rating (*TDPR*), resulting in small capacitor size and low cost, for unity power factor inverter, PWM rectifier and STATCOM applications. The size of capacitor can be reduced by 10 times with only 1.5 times *TDPR* of H-bridge circuit.

One important application of the single phase DC-capacitor-less inverter with SVPWM control is solid state variable capacitor (SSVC) for flexible AC transmission systems (FACTS) devices. SSVC based on the DC-capacitor-less inverter shows special benefit of *TDPR*, which is minimal among all applications. In order to reduce the DC capacitor to minimal value, a novel

control system directly based on ripple power is proposed for fast dynamic response and good steady state performance. In addition, the proposed control system can be extended for other single phase applications and can compensate not only 2ω ripple power, but also other even order frequency ripple power caused by the harmonics of grid voltage. As a result, the capacitor size is reduced by 13 times with only 1.125 times *TDPR* of H-bridge circuit.

Another important application is high power density and high efficiency inverter system. An interleaved DC-capacitor-less inverter with SiC devices is proposed for inverter application with different power factors. In order to improve THD performance for output voltage, an enhanced phase-shift interleaved PWM scheme is extended to unbalanced three phase system with different power factors. In order to further reduce the filter size, a new structure of integrated coupled inductors is proposed to suppress circulating current between the two parallel inverters and to filter output current at the same time. As a result, the total capacitor size is reduced by 16 times and power density of 45 W/in^3 is achieved.

In conclusion, the proposed DC-capacitor-less inverter with SVPWM is a competitive candidate for high power density, high efficiency and low cost single phase power conversion applications.

Dedicate to my Family:
Honglai Chen and Wei Chen
Fan Xu
Kevin Fan Chen

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1.1 H-Bridge circuit for single phase power conversion applications

H-bridge circuit has been widely used for single phase power conversion applications such as inverter, PWM rectifier and reactive power compensation. The power rating of the system ranges from several hundred watts to several tens of kilowatts.

With energy use and greenhouse gas emissions rising every year, renewable energy has drawn more and more attention from both the industries and governments worldwide due to its environmental friendliness, sustainability nature, economic benefits, and energy security [1].

The renewable energy landscape has changed significantly over the last decade. The U.S. Energy Information Administration (EIA) estimates that about 13% of world electricity generation was from renewable energy in 2013, with a projection for nearly 18% in 2040 [2]. One of the important applications of H-bridge circuit is the single phase DC-AC power conversion stage in renewable energy system such as photovoltaic and full cells.

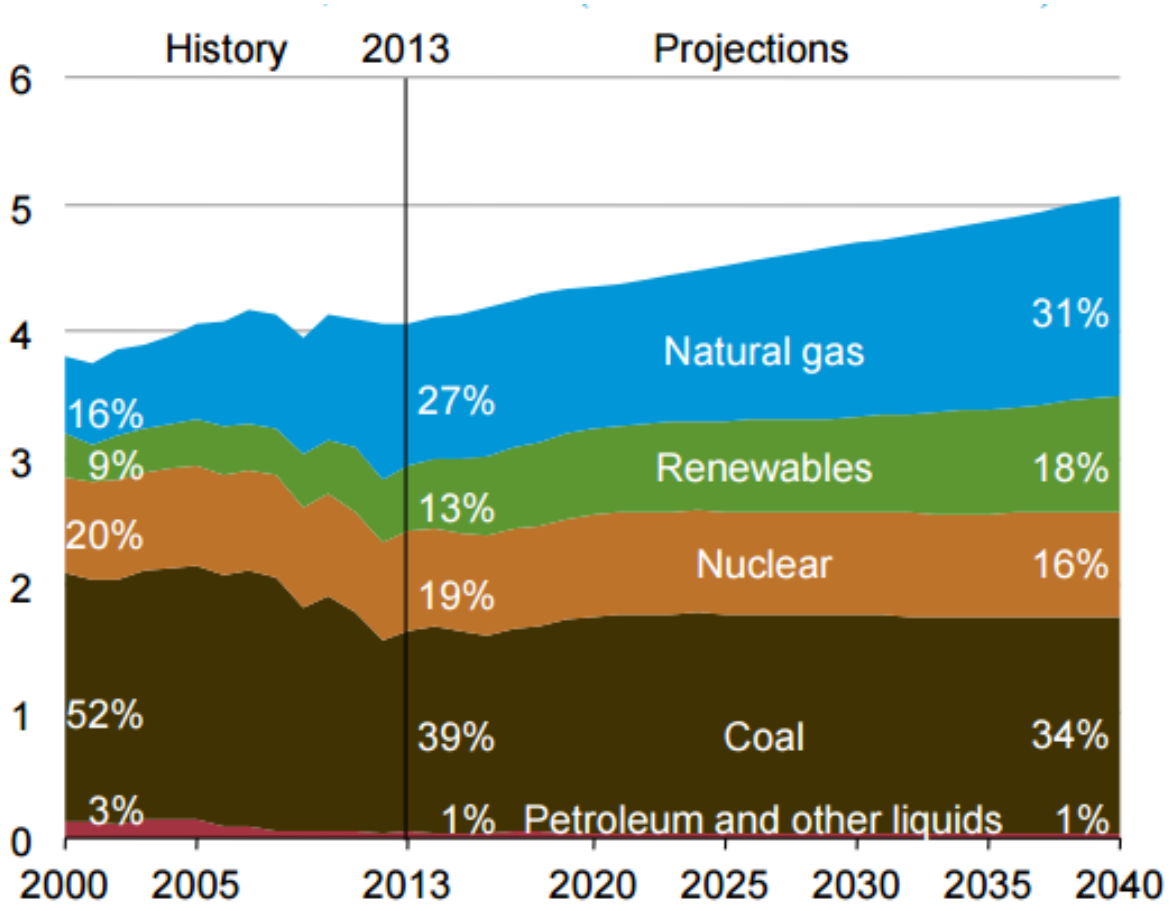

Figure 1: Electricity generation by fuel, 2000-2040 (trillion kilowatt-hours) [2].

For grid-connected solar power system, DC-AC power conversion stage interfaces PV module(s) with the grid to inject sinusoidal current into the grid. Grid-connected PV systems are categorized into three categories: centralized inverter, string inverter, and AC-Module "micro-inverter" as it shown in Figure 2 [3, 4]. Micro-inverter with power rating from 150 W to 500 W, has become the trend for grid-connected PV systems due to its advantages including: improved energy harvest, improved system efficiency, lower installation costs, "Plug-N-Play" operation, and enhanced modularity and flexibility [1, 5]. H-bridge circuit is one of the most popular topologies for micro-inverter.

However many challenges remain in the way of achieving low manufacturing cost, high

efficiency, and long operational lifetime. Since micro-inverter is typically connected to PV panel module directly, it is desirable for inverter to match the lifetime of the PV module. Most PV module manufacturers offer a warranty of 25 years on 80% of initial efficiency, and a material and workmanship warranty of five years [6].

It is well known that the bulky electrolytic DC-link capacitors in single phase inverter are the limiting components that determine the lifetime of the micro-inverter [7]. The life time of electrolytic capacitors is typically 1000~10000 hours at their rated voltage and temperature rating [8]. In order to achieve high reliability (long operational lifetime), a great deal of research has been done to reduce the required capacitance for DC-link capacitor, in order to replace electrolytic capacitor with film capacitor, which has lower energy density, however much higher reliability.

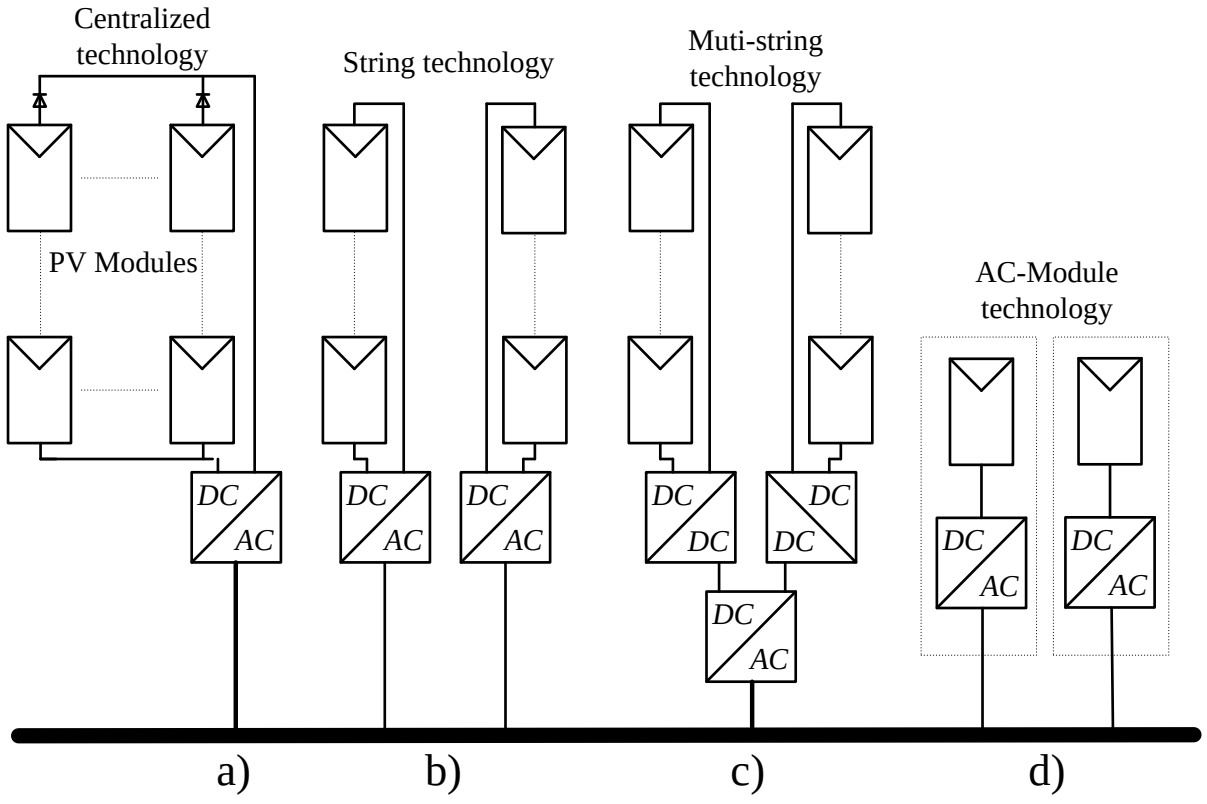

Figure 2: Photovoltaic (PV) system configurations.

Renewable energy is also widely used in distributed power generation, which could involve standby power for commercial customers, regional systems supplying neighborhoods or individual units that may or may not be grid inter-tied [9]. In a stand-alone system, the user is isolated from the utility grid either by choice or by circumstance. Figure 1.3 shows a typical fuel cell stand-alone system configuration. The H-bridge inverter in stand-alone system often operates as a voltage source inverter to deliver power to load. However, the problem of bulky electrolytic DC-link capacitors still exists in this kind of single phase DC-AC system.

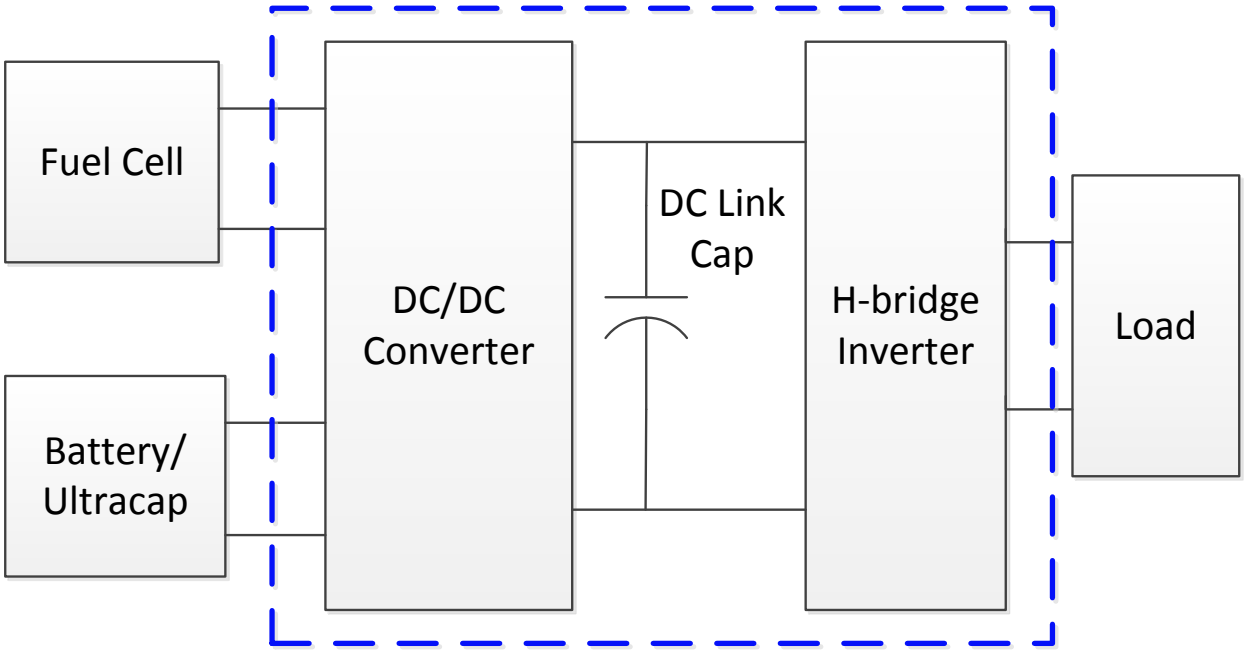

Figure 3: A typical fuel cell stand-alone system configuration.

For single phase rectifier application, PWM AC-DC converter has numerous advantages over classical passive rectifier topologies including: unity power factor, low THD, bidirectional power flow, and low components count [10, 11], and is well suited for applications with power ranging from data center servers to LED lighting.

Conventional boost PWM PFC converter consists of a full-wave diode bridge rectifier and a

boost circuit. In the power stage, there are two diode voltage drops at the rectifier bridge and one at the boost circuit, which set a hard limit on system efficiency [12]. Compared to conventional boost PWM PFC, H-bridge PWM rectifier don't need extra diode rectifier, thus greatly reducing the conduction loss. In addition, the H-bridge PWM rectifier can achieve much better power factor and THD performance for grid side current. Recently, due the development and maturation of wide band gap devices (GaN and SiC MOSFETs), totem pole PFC has already drawn a lot of attention from industries [12-16]. In the future, H-bridge PWM rectifier will be a good candidate for AC-DC converter with the cost reduction of wide band gap devices.

The concept of flexible AC transmission systems (FACTS) has been widely accepted as a breakthrough for modernizing today's power grids because FACTS devices can enhance the network stability, reliability and controllability, which in turn, improve grid transmission capability and power quality [17-27].

H-bridge circuit has been widely adopted for FACTs devices such as series compensator, shunt compensator and unified power flow controller (UPFC). As it shown in Figure 4, H-bridge circuit is adopted as multilevel converter module in star-configured cascade PWM static synchronous compensator (STATCOM) for industrial and utility power distribution systems. This enables to eliminate a bulky, heavy, and costly line-frequency transformer from the STATCOM system [22]. However, for each H-bridge circuit module, bulky electrolytic DC capacitors are needed to maintain smooth DC voltage for the normal operation of H-bridge circuit, which increase the size and cost of the total system.

Figure 5 shows the circuit configuration of distributed power-flow controller (DPFC). The DPFC adopts multiple small-size single-phase H-bridge converters instead of the one large-size three-phase series converter in the UPFC. The large number of series converters provides

redundancy, thereby increasing the system reliability [17]. Since the DPFC units are clamped on transmission lines, the size and the weight is very critical to the system. Therefore, the bulky electrolytic DC capacitors will be a big limitation of the system.

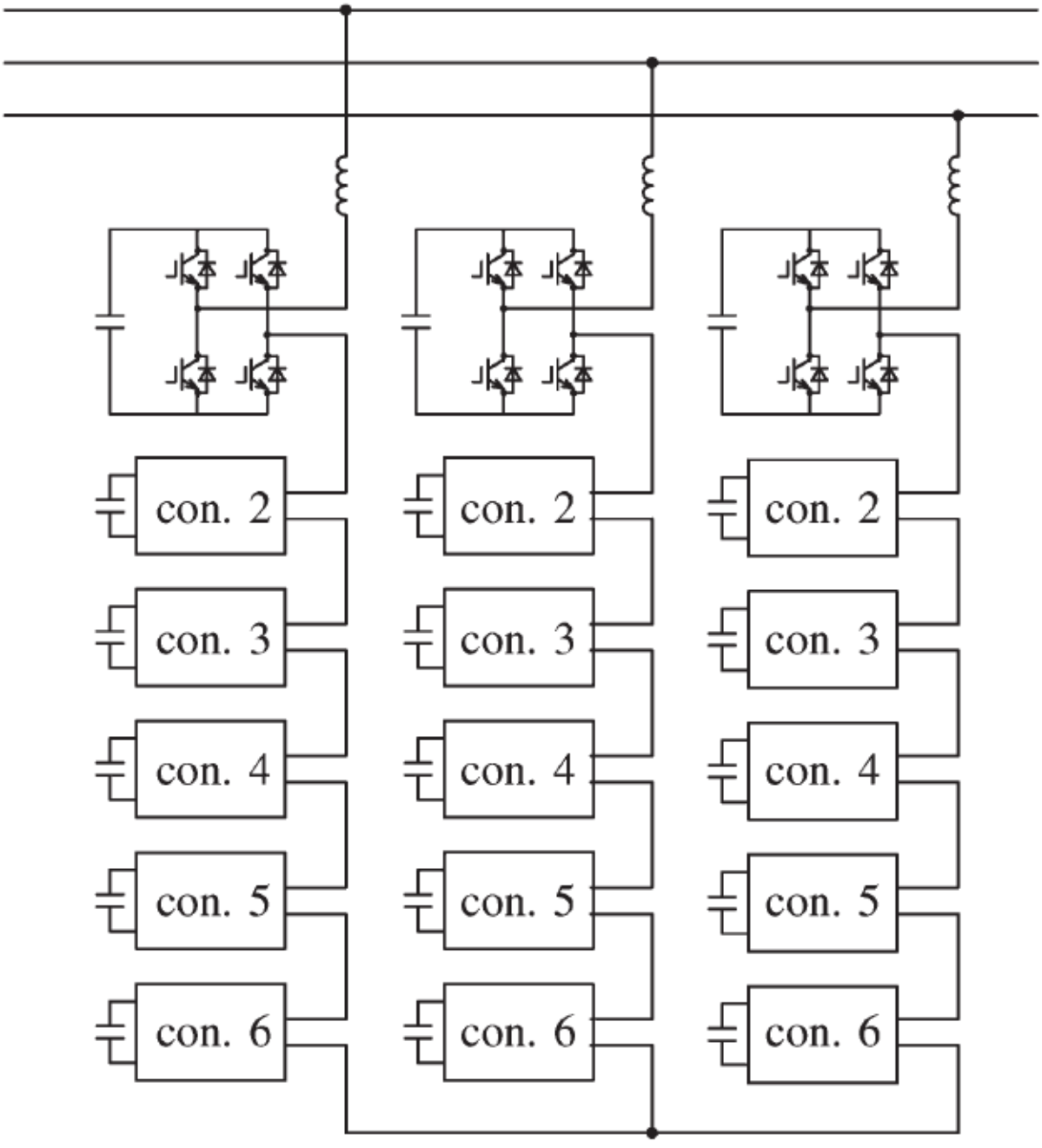

Figure 4: Circuit configuration of star-configured cascade PWM STATCOM

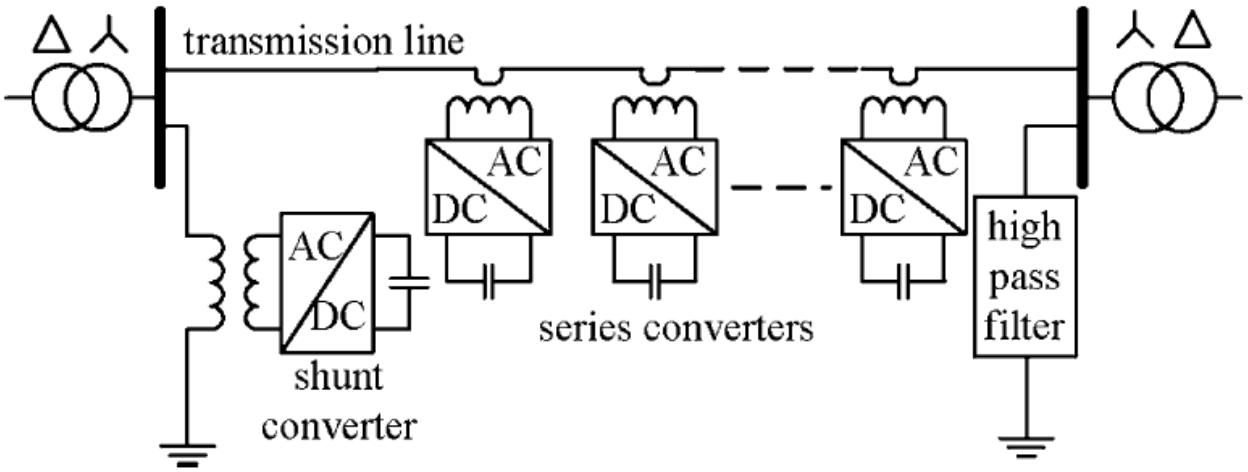

Figure 5: Circuit configuration of distributed power-flow controller (DPFC).

1.2 Problem of H-Bridge inverter

For all single phase power conversion systems, the power of the AC side is time varying, while the power of DC side is constant. As it shown in Figure 6, the rated AC voltage, v_s and the rated AC current, i_s are defined as:

$$v_s = \sqrt{2}V_s \sin(\omega t), \tag{0.1}$$

$$i_s = \sqrt{2}I_s \sin(\omega t + \varphi). \tag{0.2}$$

The rated AC power, p_s and the rated DC power, p_{dc} will be:

$$p_s = V_s I_s \cos(\varphi) + V_s I_s \sin(2\omega t + \varphi - \frac{\pi}{2}), \tag{0.3}$$

$$p_{dc} = V_s I_s \cos(\varphi). \tag{0.4}$$

And the rated apparent power of the system, S will be

$$S = V_s I_s. \tag{0.5}$$

The mismatching power between AC power and DC power is expressed as

$$p_{2\omega} = S\sin(2\omega t + \varphi - \frac{\pi}{2}), \tag{0.6}$$

which is fluctuated at twice the line frequency. The mismatch is defined as 2ω ripple power, $p_{2\omega}$. In order to balance the power mismatch, an energy storage element is required to balance the 2ω ripple power, $p_{2\omega}$.

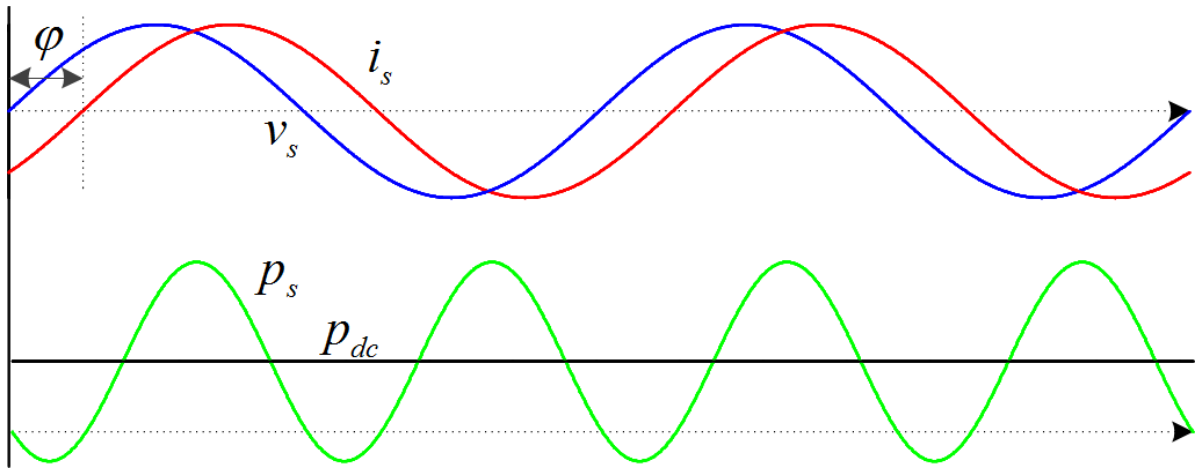

Figure 6: AC voltage/current and power waveforms.

H-bridge converter shown in Figure 7 has been widely used for single conversion systems such as PV inverter systems, PWM rectifiers, and STATCOM.

Conventional H-bridge circuit requires a DC capacitor decoupling the unbalance AC and DC power, in order to maintain a smooth DC link voltage. The required DC capacitance, C_{dc_H} can be expressed as [28]:

$$C_{dc\_H} = \frac{S}{\omega V_{dc} \Delta V_{dc}}, \tag{0.7}$$

where V_{dc} is the average voltage across the DC capacitor, ΔV_{dc} is the allowed peak-to-peak DC

voltage ripple.

From (1.7), we can find that the DC capacitance is directly proportional to the apparent power of the system and is reversely proportional to the allowed DC voltage ripple. For normal operation of H-bridge inverter, the peak-to-peak DC voltage ripple is within 2.5%, which results in very large DC capacitance value. Therefore, a bulky electrolytic capacitor is commonly used for H-bridge circuit.

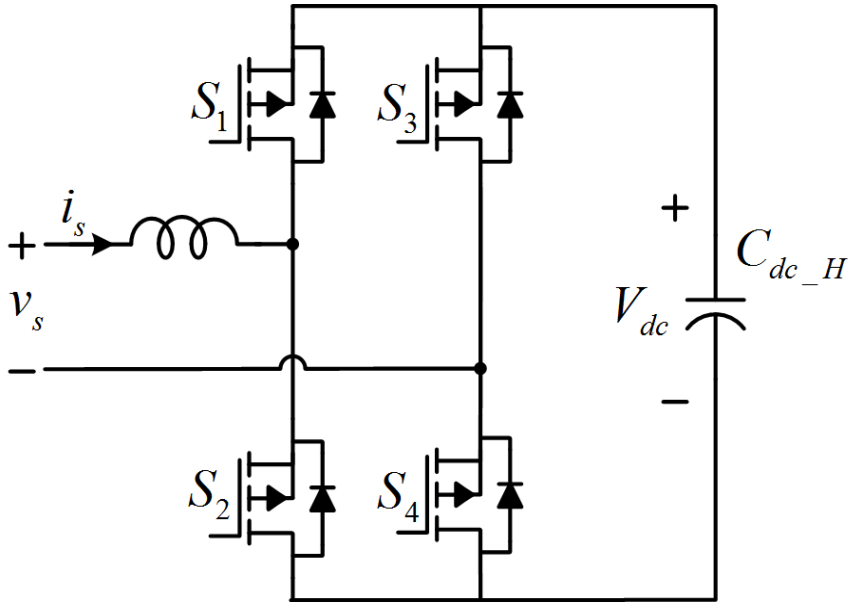

Figure 7: H-bridge for single phase power conversion.

For many single phase power conversion applications, the system requires long lifetime and high reliability. For example, the grid connected PV inverter module must be highly reliable (long operational lifetime) since most PV module manufacturers offer a warranty of 25 years on 80% of initial efficiency, and a material and workmanship warranty of five years [29].

The main limiting components inside the inverters are the DC electrolytic capacitors used for power decoupling [30, 31]. The operational lifetime for electrolytic capacitors can be

estimated by the operation voltage and temperature of the capacitor [32-34].

In order to increase the lifetime of the single phase power conversion system and to improve the reliability of the system, one possible way is to replace the electrolytic capacitors with film capacitors.

Compared to electrolytic capacitor, film capacitor has the advantages of high current ripple capability, high operating temperature, very small equivalent series resistance and inductance. However, the energy density of film capacitor is much lower than electrolytic capacitor and the cost is higher [35]. A summary of the comparison between electrolytic capacitor and film capacitor is shown in Table 1.

However, directly using film capacitor for the DC capacitor in single phase power conversion system will result in extremely large size of capacitor, low power density and high cost.

Table 1: DC capacitor comparison between film and electrolytic.

Parameter	Film	Aluminum Electrolytic
Capacitance	Low	High
ESR	Low	High
Max operating temp	105 ℃	85 ℃
Max DC voltage	Larger than 1000 V	600 V
Ripple current	High	Low
Life	Long	Short
Energy density	Low	High
Failure mode	Fail open	rupture
Construction	Dry	Liquid electrolyte
Polarity	Non polar	Have polarity
Cost	high	low

Therefore, a lot of work has been done to reduce the DC capacitor of H-bridge single phase system [28, 36-54]. By reducing the total capacitor requirement of the single phase system, film capacitor can be used to achieve systems with high power density, high reliability and high efficiency.

1.3 Scope of the dissertation

The goal of the research is to investigate the low cost method to reduce the DC capacitor of H-bridge in order to develop a single phase system with high efficiency, high power density and

high reliability for inverter, PWM rectifier and STATCOM applications.

In this dissertation, the existing single phase topologies are evaluated based on the energy requirement of capacitor (size of capacitor) and total device power rating, *TDPR* (cost of semiconductor devices) in chapter 2. A DC-capacitor-less inverter with SVPWM control for single phase power conversion is proposed to achieve minimum voltage and current stress in Chapter 3. By adding another phase leg to control an AC capacitor, the 2ω ripple power can be absorbed by the capacitor and theoretically 2ω ripples to the DC capacitor can be eliminated completely. By adopting SVPWM control method for DC-capacitor-less inverter and choosing the optimal AC capacitance and the voltage reference, the *TDPR* is greatly reduced compared to SPWM control method, and is only 1.5 times of conventional H-bridge for unity power factor inverter, PWM rectifier and STATCOM applications. As a result, the proposed method for DC capacitor minimization has the minimal energy storage capacitor and total device power rating among the exiting methods to reduce DC capacitor of H-bridge, in order words, smaller capacitor size and lower semiconductor device cost.

Two important applications of the proposed DC-capacitor-less inverter with SVPWM control: solid state variable capacitor and high power density inverter are investigated in Chapter 4 ~ 7.

One important application of the single phase DC-capacitor-less inverter with SVPWM control is solid state variable capacitor (SSVC) for flexible AC transmission system (FACTS) devices. The special benefits of SSVC based on the DC-capacitor-less inverter in terms of current stress of the shared leg and efficiency are analyzed in Chapter 4. The *TDPR* of SSVC is minimal among all single phase applications, which is only 1.125 times of conventional H-bridge circuit.

For SSVC application, any ripple power which has not been compensated by AC capacitor

will go into DC capacitor, since the DC capacitor is connected to neither DC source (inverter case) nor load (PWM rectifier case). Therefore, compared to other applications, the control system for SSVC is more challenging. The existing control method [46] still requires a large DC capacitor with same capacitance value of AC capacitor in order to maintain the stability of the system during dynamic transient. In order to reduce the DC capacitor to minimal value just for filtering switching ripple (less than 1/3 of AC capacitor), a novel control system directly based on ripple power is proposed to achieve stable DC voltage and fast dynamic response in Chapter 5. The proposed control system can be easily extended for other single phase applications. In addition, the control system can be modified to compensate not only 2ω ripple power, but also other even order frequency ripple power caused by the harmonics of grid voltage.

Another important application is high power density and high efficiency inverter system. An interleaved DC-capacitor-less inverter with SVPWM is proposed for inverter application with different power factors (1 ~ 0.7 leading and lagging) in Chapter 6. By adopting SVPWM control, the voltage and current stress is minimized. Considering the worst case of 0.7 leading power factor, the *TDPR* is only 1.78 times of H-bridge circuit. In order to improve THD performance for inverter output voltage, an enhanced phase-shift interleaved PWM scheme is adopted. The interleaved PWM scheme is extended from balanced three phase system to unbalanced three phase system with different power factors for single phase application. In order to further reduce the filtering components' size, a new structure of integrated coupled inductors is proposed to suppress circulating current between the two parallel inverters and to filter output current at the same time. Compared to existing coupled inductor design, the volume of inductors can be reduced by 35%. As a result, the total capacitor size is reduced by 16 times and power density of 45 W/in^3 is achieved.

In order to achieve single phase inverter system with high power density, high efficiency and high reliability, SiC MOSFETs are adopted for the interleaved DC capacitor-less inverter to achieve 216-kHz switching frequency. The size of filtering components including DC filtering capacitor and AC output LC filter are significantly reduced. The design and optimization of gate driver and PCB layout is investigated for the interleaved DC-capacitor-less inverter system to fully utilize the advantages of SiC MOSFETs. An effective and efficient DSP digital control program is designed to meet the control requirement for the proposed system.

In conclusion, the proposed DC-capacitor-less inverter with SVPWM is a competitive candidate to replace H-bridge for various single phase power conversion applications such as PWM rectifier, inverter and STATCOM, with high power density, high efficiency and low cost. The content of each chapter is summarized as following:

Chapter 2: Criteria to evaluate single phase topologies to reduce DC capacitor of H-bridge are explained in details based on capacitive energy storage requirement (size of capacitor) and total device power rating (cost of semiconductor devices). Review and comparison of existing single phase topologies with capacitive energy storage component for ripple power compensation are provided.

Chapter 3: A DC-capacitor-less inverter with SVPWM control for single phase power conversion with minimum voltage and current stress is proposed. The H-bridge and the additional phase leg can be analyzed together as an unbalanced three phase system. By adopting SVPWM control and choosing the optimal AC capacitance and the voltage reference, the voltage and current stress of the switches can be minimized to the same as the conventional H-bridge. Among the existing DC capacitor reduction methods for H-bridge, the single phase system with SVPWM has the minimal energy storage capacitor and TDPR. As a result, the size of capacitor is

reduced by more than 10 times with only 1.5 times TDPR of H-bridge circuit.

Chapter 4: A solid state variable capacitor (SSVC) based on the DC-capacitor-less inverter with SVPWM is developed for reactive power compensation. The solid state variable capacitor shows special advantages in terms of the switches' current stress and efficiency compared to other applications. The SSVC system based on DC-capacitor-less inverter reduces capacitor size by 13 times with 1.125 times TDPR of conventional H-bridge circuit, which is minimal among all single phase applications.

Chapter 5: In order to reduce the DC capacitor to minimal value just for filtering switching ripple (less than 1/3 of AC capacitor), a novel control system directly based on ripple power is proposed to achieve stable DC voltage and fast dynamic response. The proposed control system can be easily extended for other single phase applications. In addition, the control system can be modified to compensate not only 2ω ripple power, but also other even order frequency ripple power caused by the harmonics of grid voltage.

Chapter 6: An interleaved DC-capacitor-less inverter with SVPWM is proposed for inverter application with different power factor (1 ~ 0.7 leading and lagging). By adopting SVPWM control, the voltage and current stress of the system is minimized. Considering the worst case of 0.7 leading power factor, the TDPR is only 1.78 times of H-bridge circuit. In order to improve THD performance for inverter output voltage, an enhanced phase-shift interleaved PWM scheme is adopted. The interleaved PWM scheme is extended from balanced three phase system to unbalanced three phase system with different power factor for single phase application. In order to further reduce the filtering components' size, a new structure of integrated coupled inductors is proposed to suppress circulating current between the two parallel inverters and to filter output current at the same time. Compared to existing coupled inductor design, the volume of inductors

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Chapter 7: In order to achieve a high power density, high efficiency and high reliability inverter system, SiC MOSFETs are adopted to achieve 216-kHz switching frequency. The size of filtering components including DC filtering capacitor and AC output LC filter is significantly reduced. The design and optimization of gate driver and PCB layout for the interleaved DC-capacitor-less inverter system is investigated to fully utilize the advantages of SiC MOSFETs. An effective and efficient DSP digital control program is designed to implement SVPWM control, ripple power compensation and interleaved PWM scheme. As a result, the system can achieve 96% efficiency at full load and good dynamics response to meet the control requirement for the interleaved DC-capacitor-less inverter system.

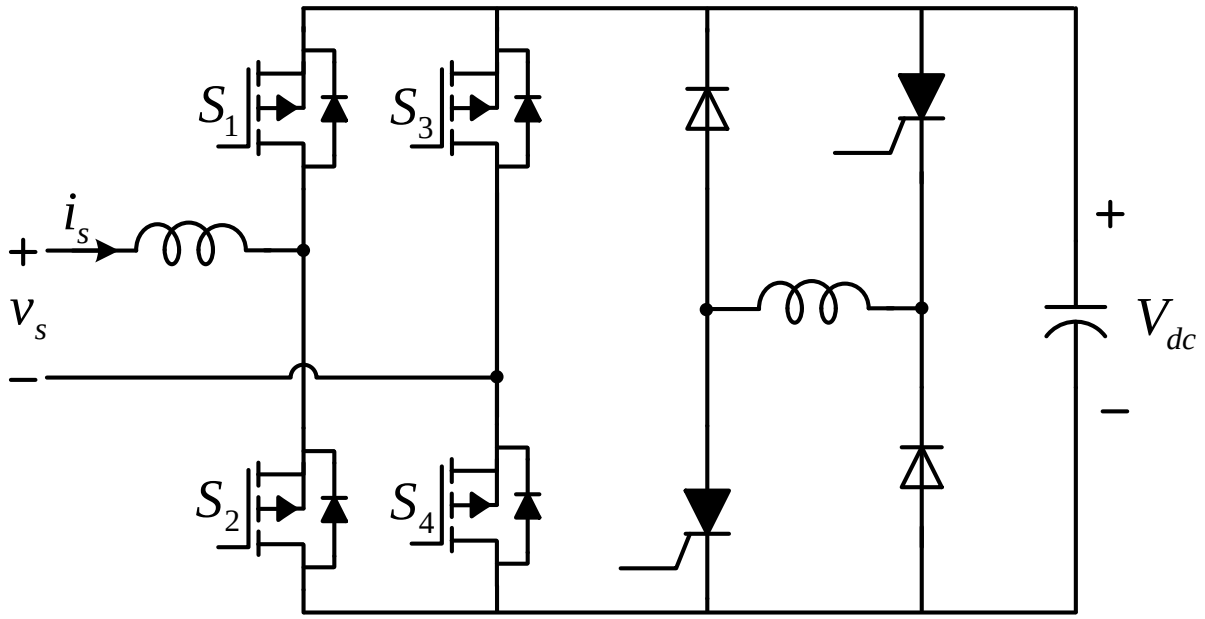
Chapter 8: Conclusion of the dissertation contributions is summarized; suggestions for future work are provided.

CHAPTER 2 SINGLE PHASE INVERTER TOPOLOGIES WITH CAPACITIVE ENERGY STORAGE FOR RIPPLE POWER COMPENSATION

In order to reduce the DC capacitor bank of H-bridge for single phase power conversion, a great deal of research has been done on active power decoupling methods. The basic idea is to use extra energy-storage components such as capacitor or inductor, which permits much larger fluctuation of voltage or current, to balance the 2ω ripple power.

A lot of topologies using inductor as energy storage components for 2ω ripple power compensation are investigated in [47, 55-57]. Some of the existing topologies are shown in Figure 8.

However, compared to capacitor, the inductor has much lower energy density and higher power losses under high switching frequency operation. Therefore, more detailed analysis and comparison of topologies based on capacitive energy storage for voltage source H-bridge circuit are investigated.



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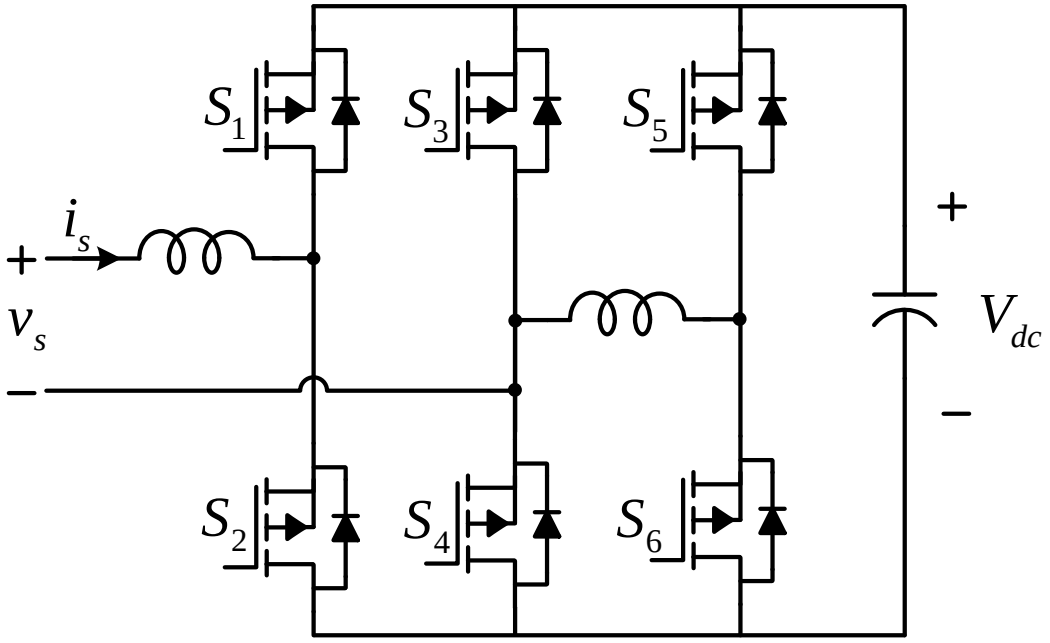


(b)

Figure 8: Topologies using inductor as energy storage components for 2ω ripple power compensation.

2.1 Criteria to evaluate single phase topologies with capacitive energy storage for ripple power compensation

For single phase power conversion system, the key point is to minimize the energy-storage capacitor, number of extra switches, and voltage/current stress of both switches and passive components. One effective way to evaluate the circuits and power decoupling methods is to compare the energy requirement of energy-storage capacitor, *Ec* and the total device power rating, *TDPR* [58].

Ec is an indicator of the capacitor size; *TDPR* is an indicator of how much total silicon area is needed for the semiconductor devices.

For conventional voltage source H-bridge converter, the bulky DC electrolytic capacitor is used for energy-storage capacitor and E_C can be calculated by

$$E_C = \frac{1}{2} C_{dc\_H} V_{dc\_\max}^2 = \frac{1}{2} C_{dc\_H} (V_{dc} + \frac{1}{2}\Delta V_{dc})^2 \tag{1.1}$$

Substitution of (1.7) into (2.1) yields:

$$E_C = \frac{S}{2\omega V_{dc}\Delta V_{dc}} (V_{dc} + \frac{1}{2}\Delta V_{dc})^2, \tag{1.2}$$

In order to maintain a smooth DC link voltage, the ripple DC voltage is design to be $\Delta V_{dc} << V_{dc}$, and E_C can be simplified to

$$E_C \approx \frac{S}{\omega} \frac{V_{dc}}{2\Delta V_{dc}}. \tag{1.3}$$

In the following analysis, it assumes that the modulation index of inverter is 1, and that minimum DC voltage is adopted. Therefore, minimum DC voltage, V_{dc} will be

$$V_{dc} = \sqrt{2} V_s. \tag{1.4}$$

The *TDPR* for conventional H-bridge will be:

$$TDPR_{H-bridge} = 4 \cdot V_{dc} \cdot \sqrt{2} I_s = 4\sqrt{2} V_s \cdot \sqrt{2} I_s = 8S . \tag{1.5}$$

Instead, if using an extra capacitor to absorb the 2ω ripple power, the minimal capacitor energy storage requirement, $E_{C\_\min}$ can be calculated by integrating half cycle of the 2ω ripple power, $p_{2\omega}$:

$$E_{C\_\min} = \left| \int_{-\varphi/2\omega}^{T/2-\varphi/2\omega} p_{2\omega} dt \right| = \frac{S}{\omega} . \tag{1.6}$$

As we can see, for conventional H-bridge system, if allowed peak-to-peak DC ripple voltage ΔV_{dc} is 2.5% of the DC voltage, the stored energy in DC capacitor is more than 20 times of the minimum energy storage requirement, which results in lower power density [28].

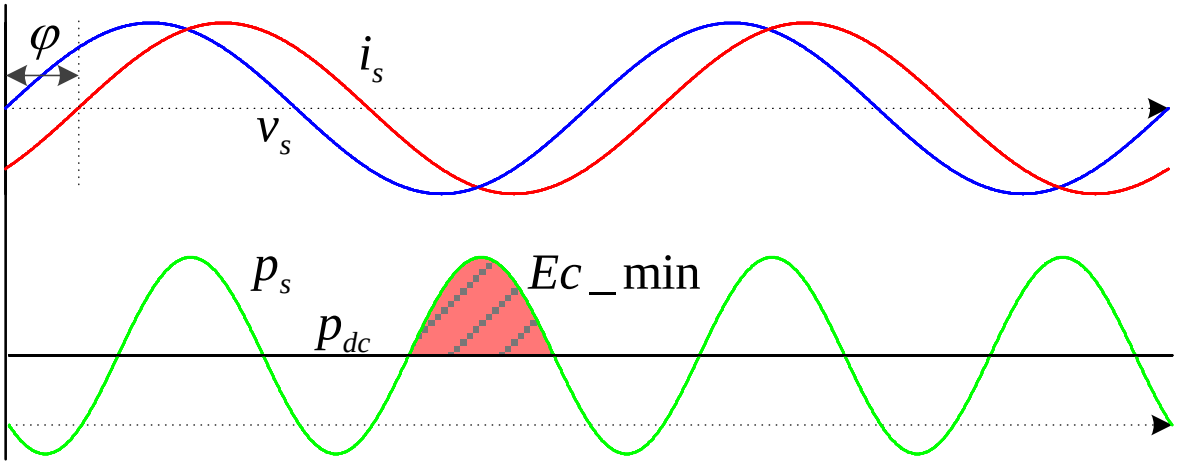


Figure 9: Minimal capacitor energy storage requirement.

2.2 Review and comparison of existing single phase topologies with capacitive energy storage component for ripple power compensation

Based on the criteria of energy requirement of energy-storage capacitor, E_C and the total

device power rating, *TDPR*, the existing topologies and power decoupling methods can be evaluated.

In Figure 10, the energy-storage capacitor, C_d is connected to DC link by a buck converter, and the capacitor voltage is unipolar [39, 40]. If the capacitor voltage reference is a full-wave rectified sinusoidal waveform, the 2ω ripple power can be transferred to the capacitor as it shown in Figure 11.

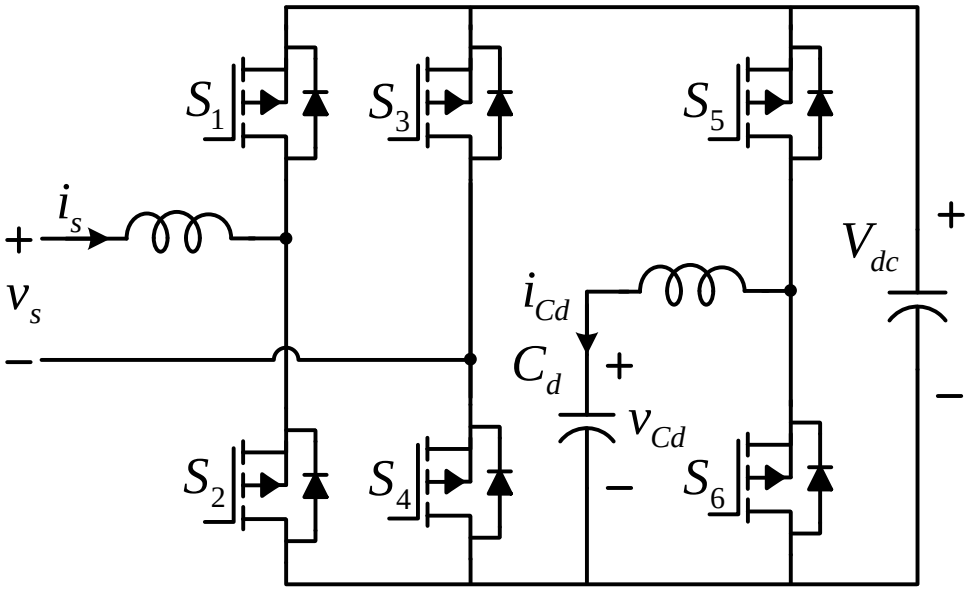


Figure 10: Single phase converter with unipolar energy-storage capacitor.

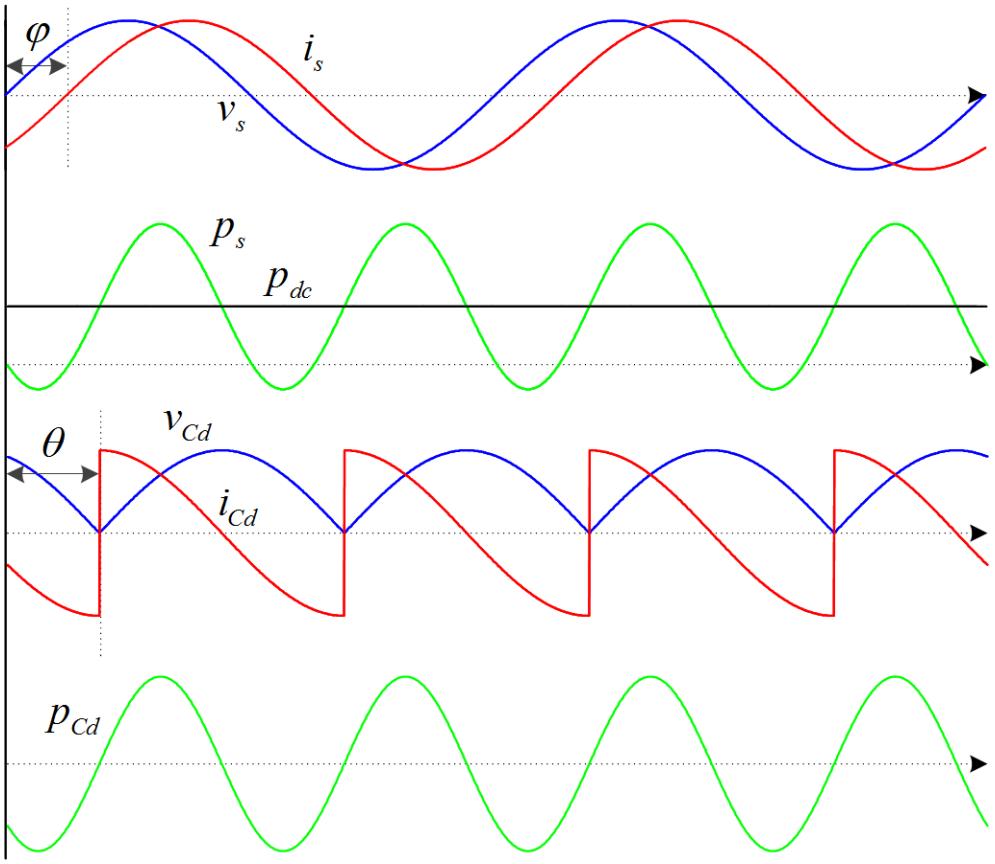


Figure 11: Single phase converter with unipolar energy-storage capacitor key waveforms.

The energy-storage capacitor's voltage and current are expressed as

$$v_{Cd} = \sqrt{2}V_{Cd}\left|\sin(\omega t + \theta)\right|, \tag{1.7}$$

$$\begin{aligned} i_{Cd} &= \sqrt{2}I_{Cd}\cos(\omega t + \theta)\cdot \mathrm{sgn}(\sin(\omega t + \theta)) \\ &= \sqrt{2}\omega C_d V_{Cd}\cos(\omega t + \theta)\cdot \mathrm{sgn}(\sin(\omega t + \theta)) \end{aligned}. \tag{1.8}$$

Then the power stored in the energy-storage capacitor will be

$$p_{Cd} = V_{Cd}I_{Cd}\sin(2\omega t + 2\theta) = \omega C_d V_{Cd}^2 \sin(2\omega t + 2\theta). \tag{1.9}$$

As it shown in Figure 11 (b), the power of C_d is controlled equal to the grid 2ω ripple power:

$$p_{Cd} = p_{2\omega}. \tag{1.10}$$

Then, the 2ω power to DC side can be fully eliminated.

By designing C_d to be:

$$C_d = \frac{I_s}{\omega V_s}, \tag{1.11}$$

the DC voltage can be fully utilized, and energy-storage capacitor's voltage and current magnitude will be:

$$V_{Cd} = V_s, \tag{1.12}$$

$$I_{Cd} = I_s. \tag{1.13}$$

In ideal case, the DC link voltage will be:

$$V_{dc} = \sqrt{2} V_s. \tag{1.14}$$

and the energy storage requirement is equal to the minimal value:

$$E_C = \frac{1}{2} C_d V_{dc}^2 = \frac{S}{\omega} = E_{C\_\min}, \tag{1.15}$$

and *TDPR* for all applications including unit power factor inverter, PWM rectifier and reactive power compensation will be:

$$\begin{aligned} TDPR &= 4 \cdot V_{dc} \cdot \sqrt{2} I_s + 2 \cdot V_{dc} \cdot \sqrt{2} I_s \\ &= 12S = 1.5 TDPR_{H-bridge} \end{aligned}. \tag{1.16}$$

However, the full-wave rectified sinusoidal reference, which contains rich harmonics, is difficult for the control system to track. Although it is possible to decrease the harmonics in the reference by increasing the energy-storage margin (therefore the capacitor voltage does not go down to zero), this will compromise full utilization of the energy-storage capacitor. Therefore, in real application, E_C will be larger than the ideal case, E_{Cmin}. The minimal reported E_C is 1.5 $E_{C\_\min}$ [39, 40].

Some circuits also adopt a boost converter to connect energy storage capacitor to DC link [59]. The circuit analysis is similar; however the energy storage capacitor will have high DC bias voltage (larger than DC link voltage). Therefore, E_C will be larger than E_{Cmin}. Compared to buck converter, the controller design for boost converter will be more difficult, since boost converter has a right half plane zero in control loop.

In Figure 12, the PWM rectifier system consists of an H-bridge and a half-bridge circuit for ripple power compensation [38]. The voltage/current waveforms and power are shown in Figure 13. The sum of the power of C_1 and C_2 is controlled to be equal to the 2ω ripple power on grid side.

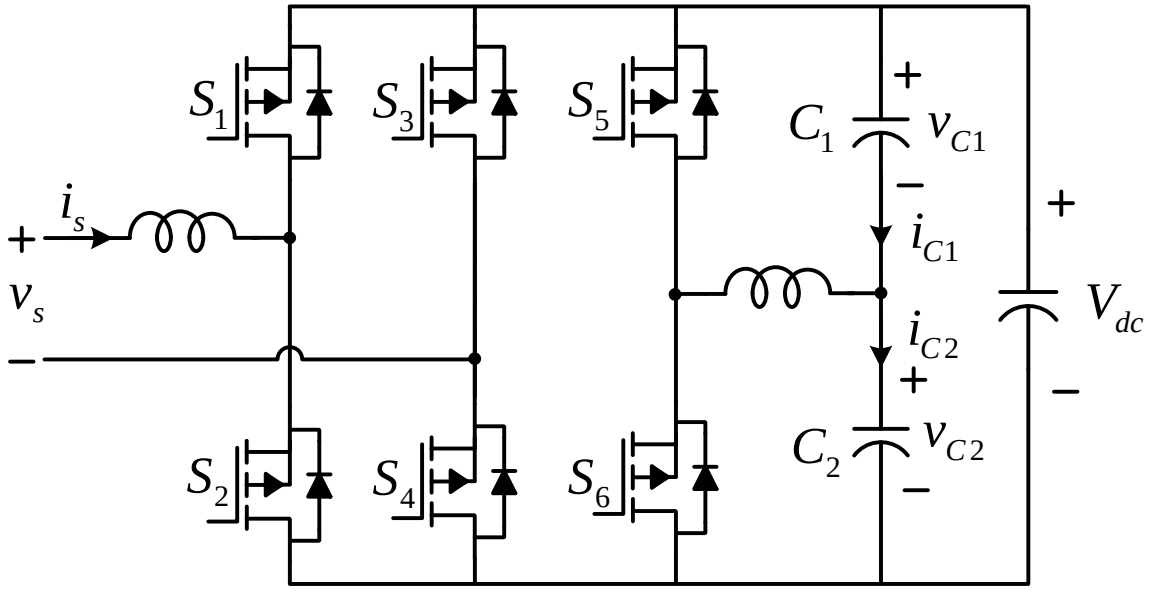


Figure 12: Single phase inverter with half bridge for ripple compensation.

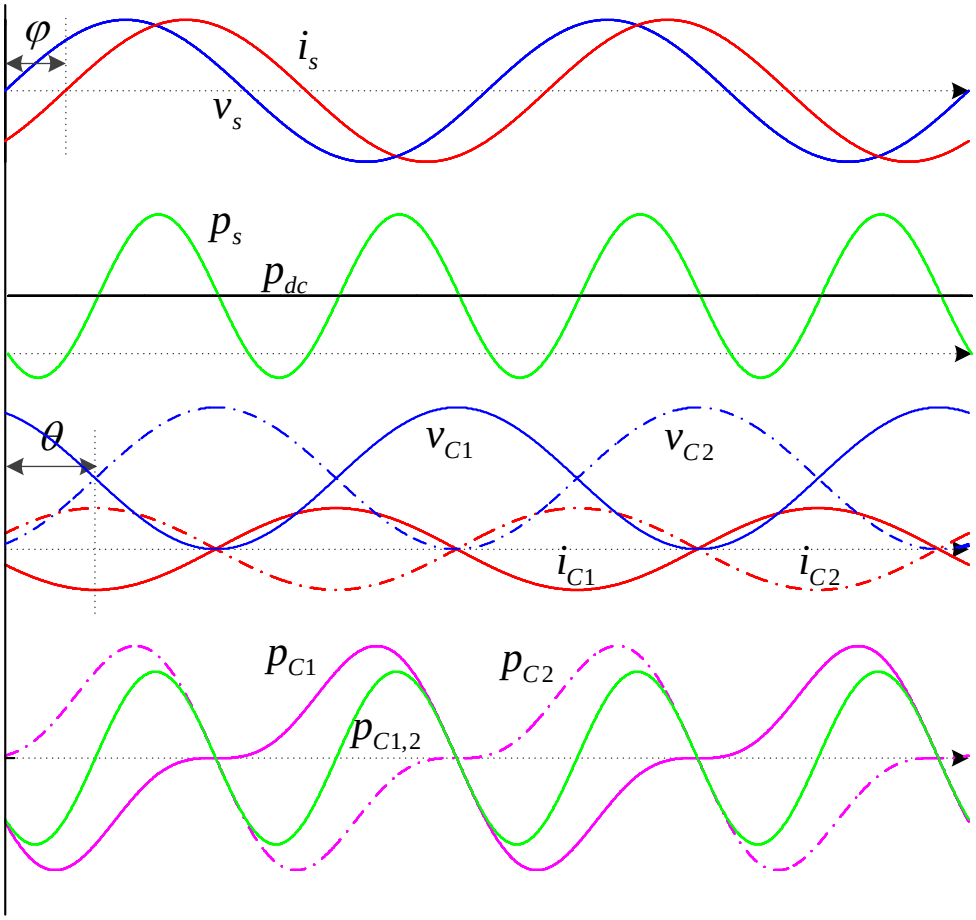


Figure 13: Single phase inverter with half bridge for ripple compensation key waveforms.

The two DC capacitors' voltage and current are express as:

$$v_{C1} = \frac{V_{dc}}{2} - \sqrt{2}V_C \sin(\omega t + \theta), \tag{1.17}$$

$$v_{C2} = \frac{V_{dc}}{2} + \sqrt{2}V_C \sin(\omega t + \theta), \tag{1.18}$$

$$\begin{aligned} i_{C1} &= -i_{C2} = -\sqrt{2}I_C \cos(\omega t + \theta) \\ &= -\sqrt{2}\omega C_f V_C \cos(\omega t + \theta) \end{aligned}. \tag{1.19}$$

Then, the sum of power of C_1 and C_2 will be

$$p_{C1,2} = v_{c1}i_{c1} + v_{c2}i_{c2} = 2\omega C_f V_C^2 \sin(2\omega t + 2\theta). \tag{1.20}$$

By designing C_f to be:

$$C_1 = C_2 = C_f = \frac{I_s}{2\omega V_s}. \tag{1.21}$$

The DC capacitors' voltage and current magnitude will be:

$$V_C = V_s, \tag{1.22}$$

$$I_C = I_s / 2. \tag{1.23}$$

Since the peak voltages of C_1 and C_2 are V_{dc}, the DC voltage will be

$$V_{dc} = 2\sqrt{2}V_s, \tag{1.24}$$

which is double of the DC voltage requirement of conventional H-bridge system. The peak currents of C_1 and C_2 is equal to $\sqrt{2}I_s / 2$. The currents of S_5 and S_6 are the subtraction of the currents of C_1 and C_2; and the peak currents of S_5 and S_6 are equal to AC output peak current.

The energy storage requirement will be:

$$E_C = 2 \times \frac{1}{2} C_f V_{dc}^2 = \frac{4S}{\omega} = 4E_{C\_\min}, \tag{1.25}$$

and *TDPR* will be:

$$TDPR = 6 \cdot V_{dc} \cdot \sqrt{2}I_s = 6 \cdot 2\sqrt{2}V_s \cdot \sqrt{2}I_s = 24S = 3TDPR_{H-bridge}. \tag{1.26}$$

The advantage of this circuit is that C_1 and C_2 are also utilized as the DC filter capacitor. However, in order to keep the switches' current stress same as the H-bridge, the required DC voltage of the circuit is double of H-bridge's DC voltage. Therefore, *TDPR* is 3 times of $TDPR_{H\text{-}bridge}$. In addition, the voltages of C_1 and C_2 have a DC component of half DC link voltage to maintain a constants DC voltage, which is the sum of the voltage of C_1 and C_2. The individual power of C_1 and C_2 has another component with the line frequency, beside 2ω ripple power as it

shown in Figure 13. Although the line frequency components of the power of C_1 and C_2 are cancelled out, the energy of C_1 and C_2 are not fully used for 2ω ripple power compensation and the energy storage requirement E_C is significantly increased, which is 4 times of E_{Cmin}.

In Figure 14, the circuit combines the half-bridge circuit for ripple power compensation with one leg of the H-bridge inverter in Figure 12. Therefore, the circuit has the minimum components among the existing topologies. The circuit basic operation is similar to circuit in Figure 12. And the energy storage requirement E_C remains the same, which is 4 times of E_{Cmin}.

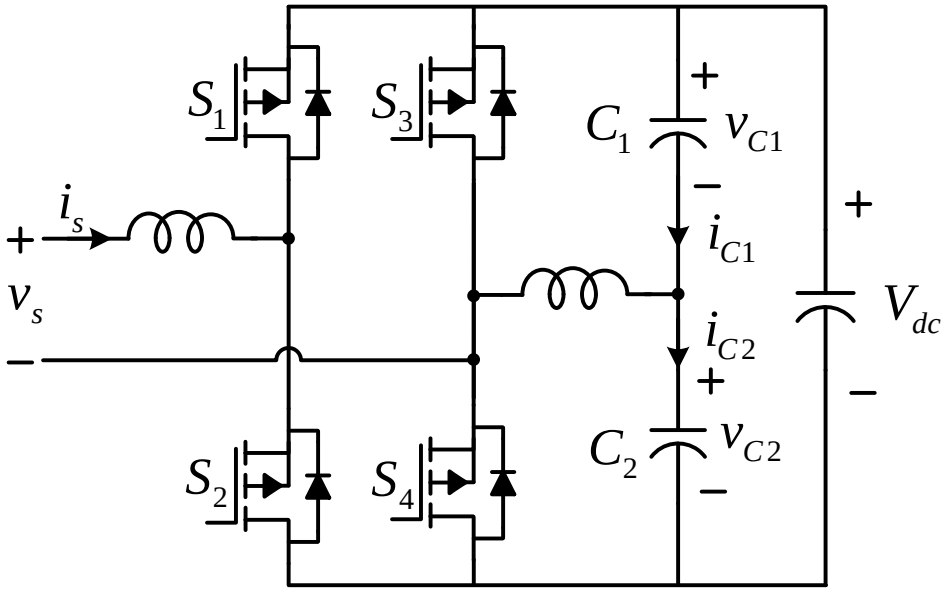


Figure 14: Single phase inverter with minimum components for ripple compensation.

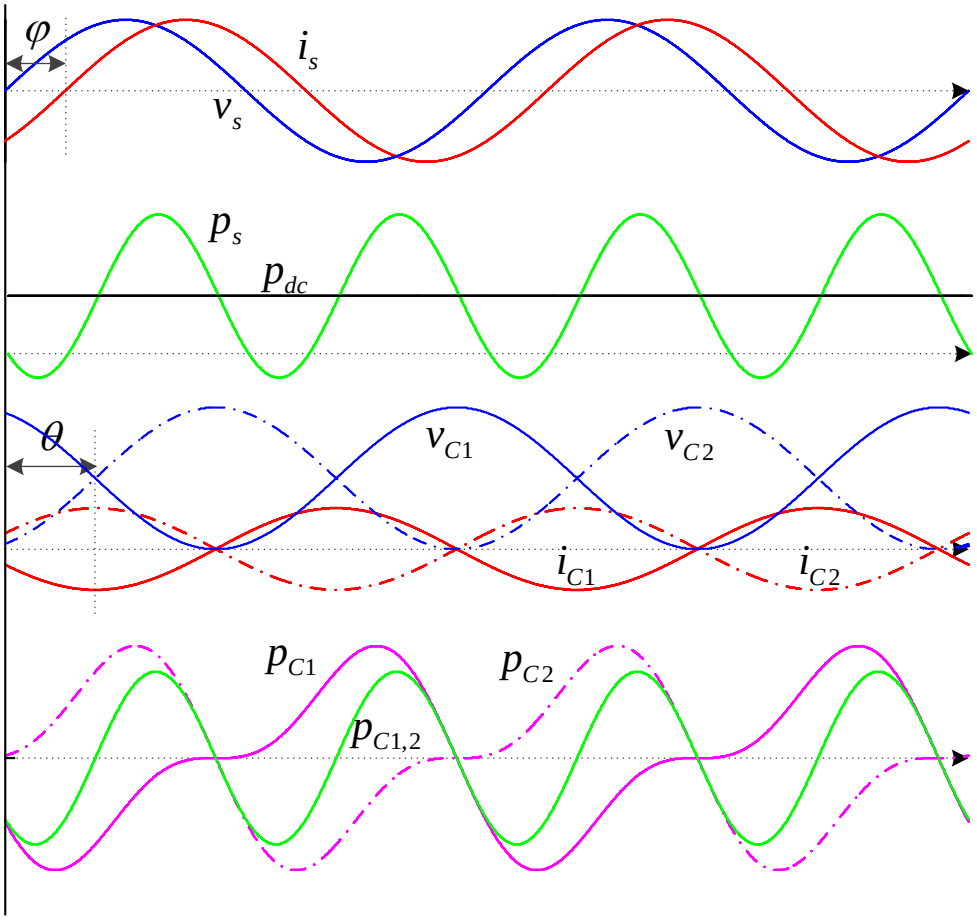


Figure 15: Single phase inverter with minimum components for ripple compensation key waveforms.

Another advantage is that the current stress of the shared leg will not increase for applications of inverter, PWM rectifier with unity power factor and reactive power compensation with leading current. Therefore, the *TDPR* is reduced to 2 times of $TDPR_{H\text{-}bridge}$ for these applications.

A single-phase PWM rectifier with the power decoupling ripple-port shown in Figure 16 is proposed in [28, 41]. By adding any extra H-bridge to interface the energy-storage capacitor, the capacitor works in AC mode and the voltage/current waveforms are sinusoidal as it shown in Figure 17.

The capacitor's voltage and current are expressed as

$$v_{Cac} = \sqrt{2}V_{Cac}\sin(\omega t + \theta), \tag{1.27}$$

$$i_{Cac} = \sqrt{2}I_{Cac}\cos(\omega t + \theta) = \sqrt{2}\omega C_{ac}V_{Cac}\cos(\omega t + \theta). \tag{1.28}$$

Then the power of the AC capacitor will be

$$p_{Cac} = V_{Cac}I_{Cac}\sin(2\omega t + 2\theta) = \omega C_{ac}V_{Cac}^2\sin(2\omega t + 2\theta). \tag{1.29}$$

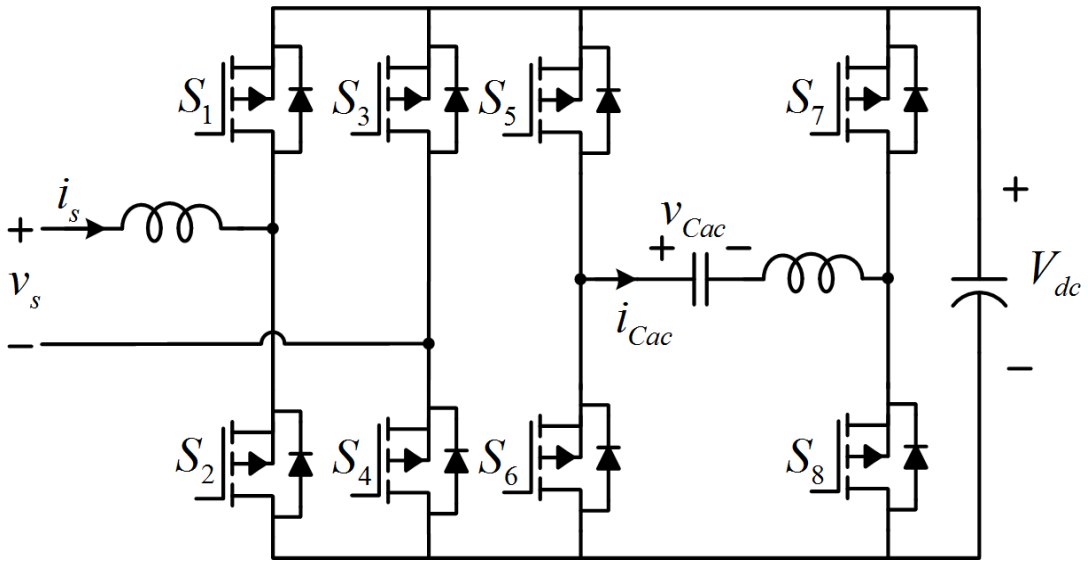


Figure 16: Single phase inverter with H-bridge for ripple compensation.

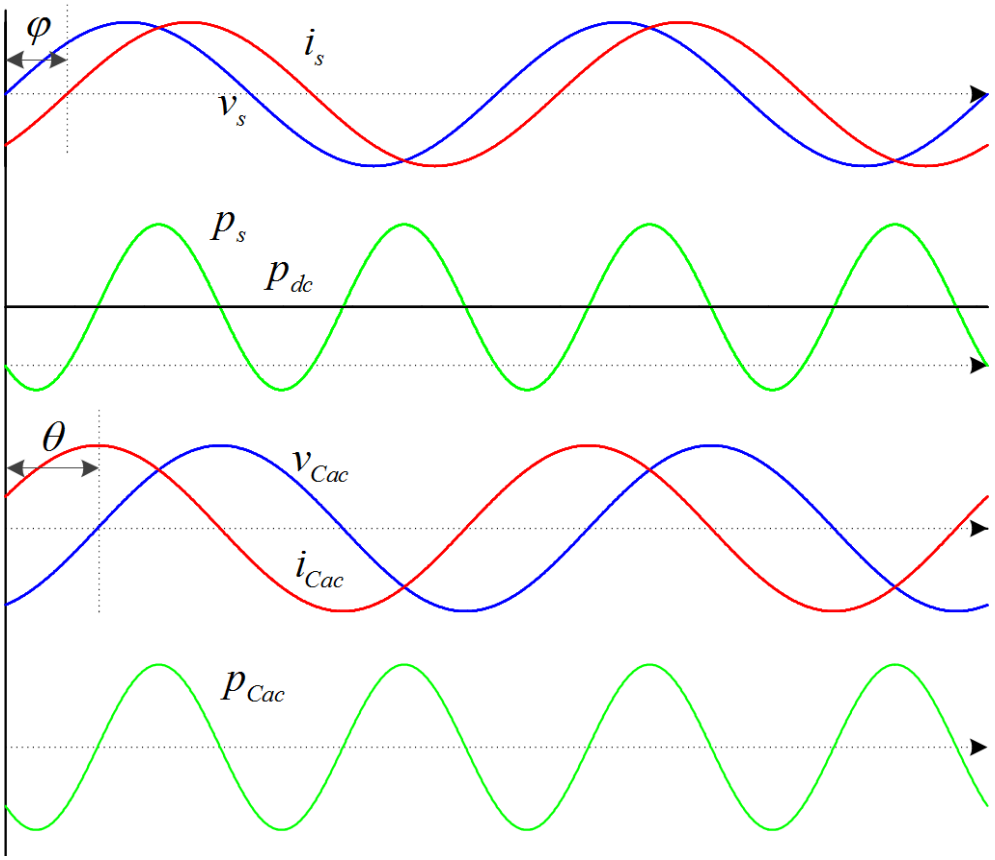


Figure 17: Single phase inverter with H-bridge for ripple compensation key waveforms.

By designing C_{ac} to be:

$$C_{ac} = \frac{I_s}{\omega V_s}, \tag{1.30}$$

the DC voltage can be fully utilized, and AC capacitor voltage/current magnitude will be:

$$V_{Cac} = V_s, \tag{1.31}$$

$$I_{Cac} = I_s. \tag{1.32}$$

In ideal case, the DC voltage will be:

$$V_{dc} = \sqrt{2} V_s, \tag{1.33}$$

and the energy storage requirement is:

$$E_C = \frac{1}{2} C_{ac} (\sqrt{2} V_{Cac})^2 = C_{ac} V_{ac}^2 = \frac{S}{\omega} = E_{C\_\min}, \tag{1.34}$$

and *TDPR* will be:

$$\begin{aligned} TDPR &= 4 \cdot V_{dc} \cdot \sqrt{2} I_s + 4 \cdot V_{dc} \cdot \sqrt{2} I_s \\ &= 16S = 2TDPR_{H-bridge} \end{aligned}. \tag{1.35}$$

Since the energy-storage capacitor is fully utilized, the capacitance is minimized. However, the system needs too many auxiliary switches, which increase the system's complexity and total device power rating.

In [45, 46], the PWM rectifier system shown in Figure 18 consists of an H-bridge and an additional phase leg connected to an AC capacitor, C_{ac}. Compared to the topology in Figure 16, the number of extra switches is reduced. And the energy storage requirement E_C remains the same, which is equal to the minimal value.

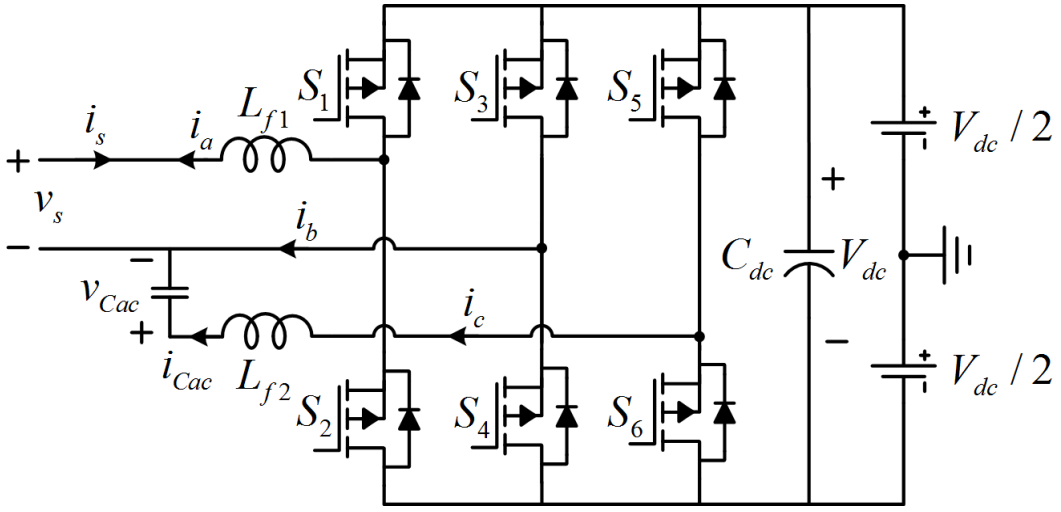


Figure 18: Single phase inverter with extra phase leg and AC capacitor for ripple compensation.

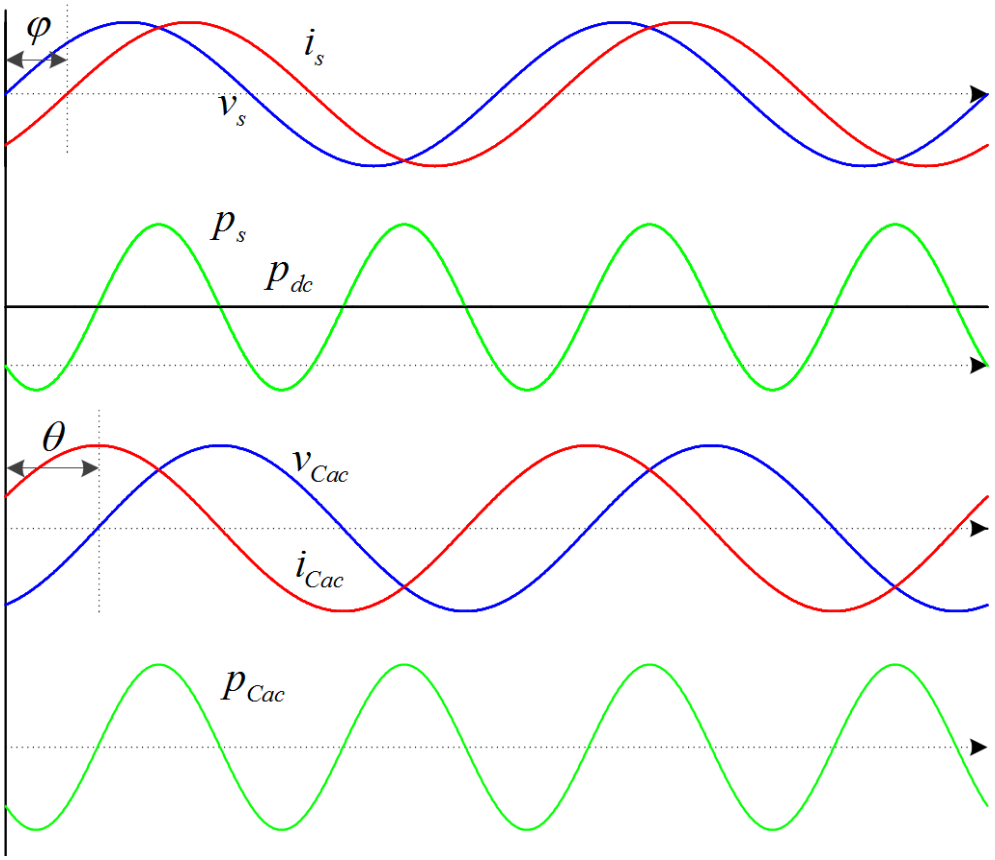


Figure 19: Single phase inverter with extra phase leg and AC capacitor for ripple compensation key waveforms.

However, because of the adoption of SPWM control, the magnitude of the sinusoidal voltage generated by phase B is higher than original H-bridge's phase A and C. Therefore, the required DC voltage is greatly increased and the voltage stress of switches is higher. A detailed analysis of the required DC voltage and *TDPR* for all single phase power conversion cases is provided in Chapter II.

In this dissertation, a DC-capacitor-less inverter for single-phase power conversion with minimum voltage and current stress is proposed. The circuit has the same topology in Figure 18. However the system is analyzed as an unbalance three-phase system. By adopting SVPWM

control and choosing the optimal AC capacitance and the voltage reference, the DC-capacitor-less inverter can be used for PWM rectifier, inverter with unity power factor and STATCOM (current leading voltage) without increasing both current and voltage stress. Since only two more switches are needed and voltage/current stress is the same as the original H-bridge, *TDPR* is only increased by 50%. The total size of capacitor (including the AC capacitor and the DC capacitor) of DC-capacitor-less inverter is reduced by more than 10 times compared to conventional H-bridge system.

Two important applications, that is, solid state variable capacitor (SSVC) and high power density single phase inverter will be investigated. A solid state variable capacitor based on the DC-capacitor-less inverter is competitive candidate to replace the conventional H-bridge in flexible AC transmission systems (FACTS) devices. Interleaved single phase inverter with SiC devices based on DC-capacitor-less inverter is proposed and developed to achieve high power density and high efficiency.

2.3 Conclusions

Two importance concepts: the energy requirement of energy-storage capacitor, E_C and the total device power rating, *TDPR* are introduced to evaluate the existing topologies using capacitive energy storage elements. The advantage and the limitation of the topologies are compared and summarized.

Based on the analysis, the topology using an H-bridge with an extra leg has the potential to have the lowest energy requirement of energy-storage capacitor and the total device power rating among the existing topologies. However, in order to minimize the voltage and current stress of

the switches, the system needs to be controlled as an unbalanced three phase system and by adopting SVPWM instead of SPWM. A detailed analysis and comparison of SVPWM and SPWM control is provided in next chapter.

CHAPTER 3 DC-CAPACITOR-LESS INVERTER FOR SINGLE PHASE POWER CONVERSION

The DC-capacitor-less inverter for single-phase power conversion with minimum voltage and current stress has the same topology shown in Figure 18. However, the two legs of the original H-bridge and the extra leg will be considered together as an unbalanced three-phase system. By adopting SVPWM control and choosing the optimal AC capacitance and the voltage reference, the voltage and current stress of the switches can be minimized to the same as H-bridge circuit. DC-capacitor-less inverter with SVPWM has the minimal AC capacitor for energy storage capacitor and very small DC capacitor only for filtering switching ripple. As a result, the size of capacitor is reduced by more than 10 times with only 1.5 times *TDPR* of H-bridge circuit for unity power factor inverter, PWM rectifier and STATCOM applications. Among the existing methods to reduce H-bridge DC capacitor, the proposed method has the minimal energy storage capacitor and total device power rating (TDPR), resulting in small capacitor size and low semiconductor device cost.

In this chapter, the operation of the proposed system and cases analysis for unity power factor inverter, PWM rectifier and reactive power compensation are provided. A comparison of DC voltage requirement, switches current stress and TDPR between SPWM and SVPWM is provided to show the benefits of the DC-capacitor-less inverter in terms of voltage and current stress. A 1.5-kVA single phase power conversion system is designed and tested to verify DC-capacitor-less inverter for different applications.

3.1 Operation of DC-capacitor-less inverter

Taking the output voltages of the three phase-legs as controlled voltage sources v_a, v_b, v_c, the equivalent circuit for the DC-capacitor-less inverter is shown in Figure 20

Suppose the grid voltage and the rated grid-side current to be:

$$v_s = \sqrt{2}V_s \sin(\omega t), \tag{2.1}$$

$$i_s = \sqrt{2}I_s \sin(\omega t + \varphi). \tag{2.2}$$

and the voltage and current of the storage AC capacitor to be:

$$v_{Cac} = \sqrt{2}V_{Cac} \sin(\omega t + \theta), \tag{2.3}$$

$$i_{Cac} = \sqrt{2}I_{Cac} \cos(\omega t + \theta) = \sqrt{2}\omega C_{ac} V_{Cac} \cos(\omega t + \theta). \tag{2.4}$$

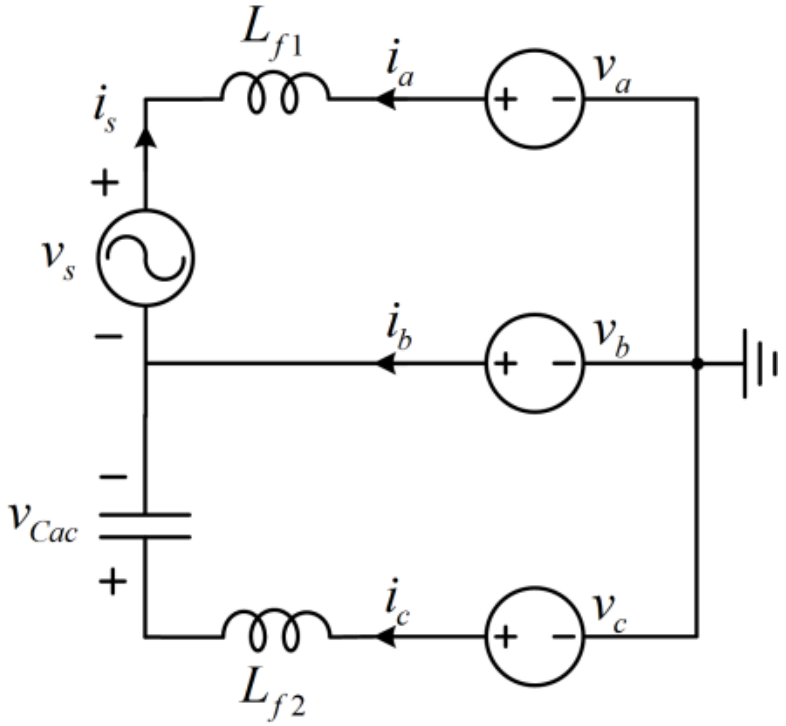


Figure 20: Equivalent circuit of the DC-capacitor-less inverter.

Then, we can get the expression of grid power:

$$\begin{aligned} p_g &= v_s i_s = V_s I_s[\cos(\varphi) - \cos(2\omega t + \varphi)] \\ &= V_s I_s[\cos(\varphi) + \sin(2\omega t + \varphi - \frac{\pi}{2})] \end{aligned}, \tag{2.5}$$

which contains DC power component and the 2ω ripple power component

$$p_{2\omega} = V_s I_s \sin(2\omega t + \varphi - \frac{\pi}{2}). \tag{2.6}$$

The instantaneous power generated by C_{ac} can also be obtained:

$$p_{Cac} = v_{Cac} i_{Cac} = \omega C_{ac} V_{Cac}^2 \sin(2\omega t + 2\theta). \tag{2.7}$$

To simplify the analysis, the power on filter inductors L_{f1} and L_{f2} (which are normally less than 5% pu) is neglected [60, 61]. Then, the power of C_{ac} should be controlled equal to the grid 2ω ripple power:

$$p_{Cac} = p_{2\omega}. \tag{2.8}$$

Therefore, the magnitude and phase of v_{Cac} should satisfy the following equations:

$$\omega C_{ac} V_{Cac}^2 = V_s I_s. \tag{2.9}$$

$$\theta = \frac{1}{2}(\varphi - \frac{\pi}{2}), \text{ or } \frac{1}{2}(\varphi - \frac{\pi}{2}) + \pi. \tag{2.10}$$

If the decoupling capacitance is designed to be

$$C_{ac} = \frac{I_s}{\omega V_s}, \tag{2.11}$$

the magnitude of the voltage and current of C_{ac} will be:

$$V_{Cac} = V_s, \tag{2.12}$$

$$I_{Cac} = I_s, \tag{2.13}$$

and the current and voltage stress of the system can be minimized.

3.2 Cases analysis

According to the previous analysis, for any φ, there are two possible solutions of θ. Since the system can be treated as an unbalanced three phase system, SVPWM can be adopted. For SVPWM, the minimum DC voltage is determined by the maximum line-to-line voltage. For the rated power, we have:

$$\left|\dot{V}_{ab}\right| = \left|\dot{V}_{cb}\right| = \left|\dot{V}_{s}\right| = \left|\dot{V}_{Cac}\right|, \tag{2.14}$$

$$\left|\dot{I}_{a}\right| = \left|\dot{I}_{c}\right| = \left|\dot{I}_{s}\right| = \left|\dot{I}_{Cac}\right|. \tag{2.15}$$

For PWM rectifier with unity power factor, inverter with unity power factor and STATCOM, there will be two possible solutions for θ. Only by choosing θ to be $-\frac{\pi}{4}$, $\frac{\pi}{4}$ and 0 for PWM rectifier, inverter and STATCOM respectively, the magnitude of $\dot{V}_{ac}$ is smaller than V_s, and the magnitude of $\dot{I}_b$ is smaller than I_s. Then, the voltage stress is $\sqrt{2}V_s$, and the current stress is $\sqrt{2}I_s$. Therefore, the voltage and current stress of switches are equal to the original H-bridge system.

If θ is not chosen properly, the current and voltage stress will be greatly increased. For example, θ can also be π for STATCOM case. However, the magnitude of $\dot{V}_{ac}$ will be $2V_s$, and the magnitude of $\dot{I}_b$ will be $2I_s$. and the voltage and current stress will be doubled. Figure 21, Figure 22, and Figure 23 show the phasor diagrams of three specific cases with the minimum voltage and current stress.

Because the voltage and current stress of the proposed system and the H-bridge system are the same, the two systems can use the same rating switches, and the power loss on switches can be

directly compared based on the each phase's current. For full rated power, phase A and phase C's leg currents of the DC-capacitor-less inverter are the same as the two legs' current of conventional H-bridge system, and phase B's current of DC-capacitor-less inverter is always smaller than H-bridge's phase current. Then, the power loss on phase A and C together are almost equal to the H-bridge system; and the power loss on phase B is always smaller than half of the H-bridge system. Therefore the total switch power loss of the DC-capacitor-less inverter is less than 150% of the H-bridge system.

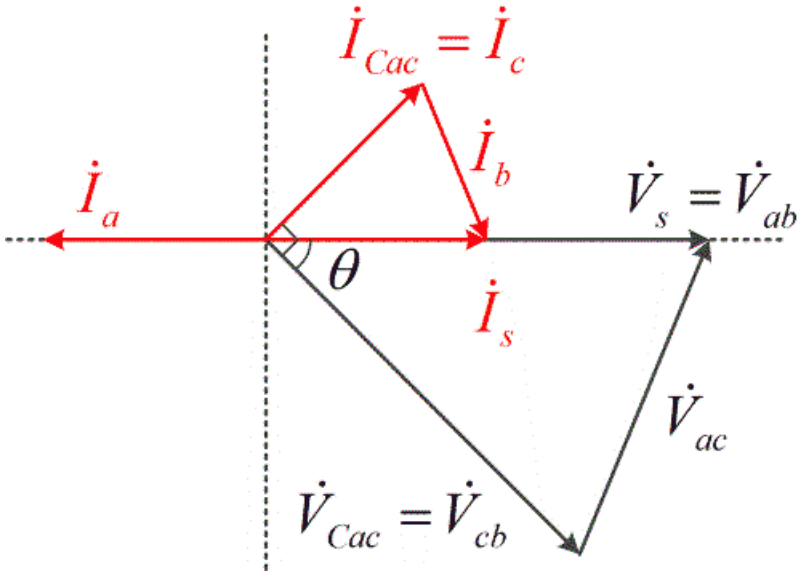


Figure 21: Phasor diagrams of PWM rectifier with unity power factor, $\varphi = 0, \theta = -\frac{\pi}{4}$.

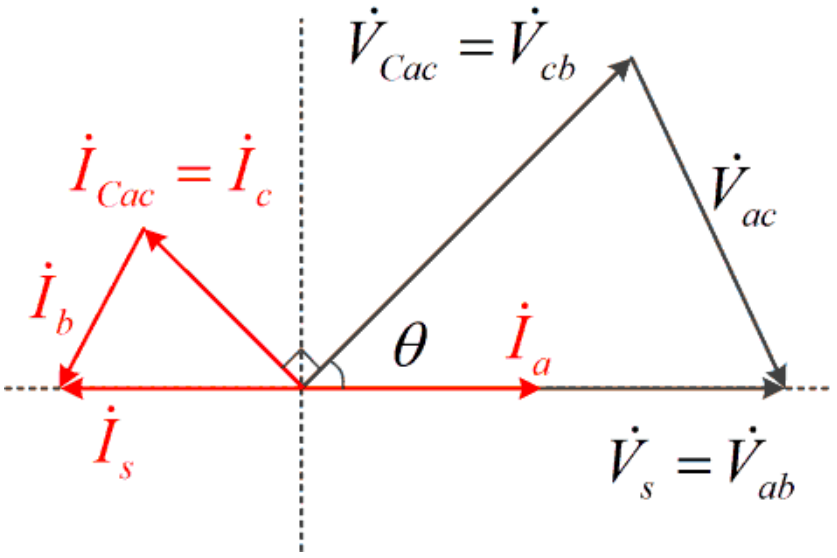


Figure 22: Phasor diagrams of inverter with unity power factor, $\varphi = \pi$, $\theta = \frac{\pi}{4}$.

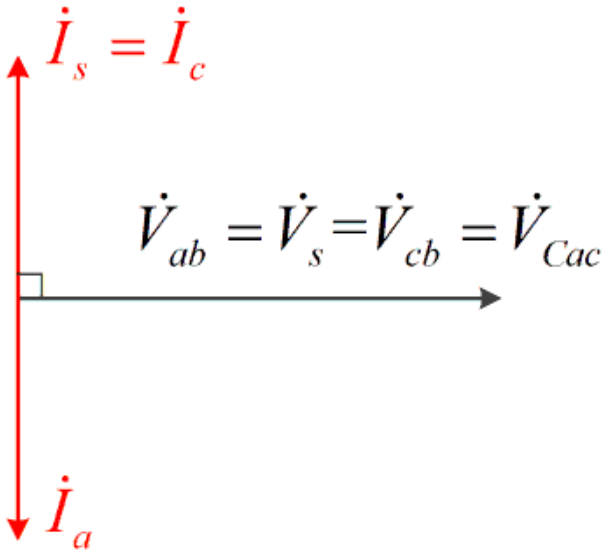


Figure 23: Phasor diagrams of STATCOM with current leading, $\varphi = \frac{\pi}{2}$, $\theta = 0$.

3.3 General case analysis

Figure 24 shows the phasor diagram of general case. The angle between $\dot{V}_{ab}$ and $\dot{V}_{cb}$ is $|\theta|$:

$$\angle(\dot{V}_{ab},\dot{V}_{cb}) = |\theta|, \tag{2.16}$$

and the angle between $\dot{I}_s$ and $\dot{I}_c$ is:

$$\angle(\dot{I}_{ac},\dot{I}_c) = \left|\theta-\varphi+\frac{\pi}{2}\right|. \tag{2.17}$$

According to triangle relationship, V_{ac} and I_b are expressed as

$$V_{ac} = \sqrt{V_s^2+V_s^2-2V_s^2\cos(\theta)}, \tag{2.18}$$

$$I_b = \sqrt{I_s^2+I_s^2-2I_s^2\cos(\theta-\varphi+\frac{\pi}{2})}. \tag{2.19}$$

When φ is from –π/2 to π, V_{ac} and I_b are minimized when θ is chosen as:

$$\theta = \frac{1}{2}(\varphi-\frac{\pi}{2}). \tag{2.20}$$

When φ is from –π to –π/2, V_{ac} and I_b are minimized when θ is chosen as:

$$\theta = \frac{1}{2}(\varphi-\frac{\pi}{2})+\pi. \tag{2.21}$$

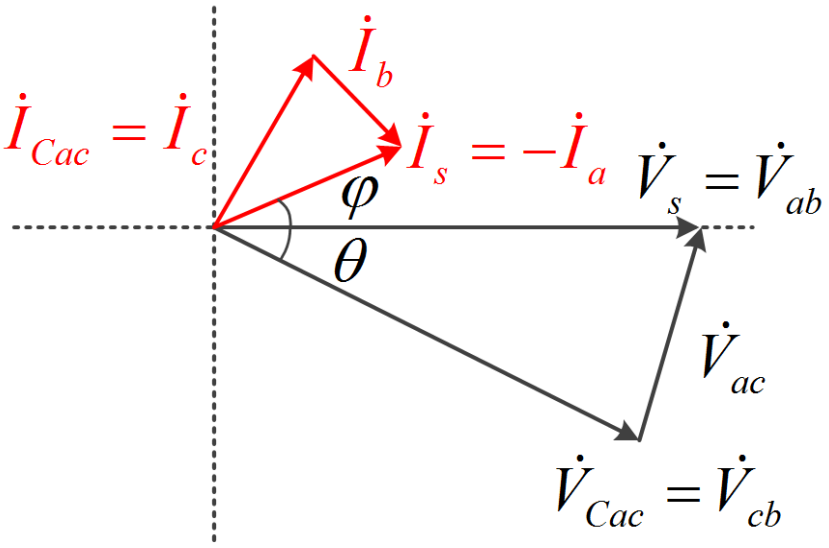


Figure 24: Phasor diagram of general case.

3.4 Comparison of DC voltage requirement, switches current stress and TDPR between SPWM and SVPWM

In order to show the benefit of SVPWM, the minimum DC voltage requirement and switches current stress, and *TDPR* are compared between SPWM and SVPWM control [62, 63].

For SVPWM, the minimum DC voltage is determined by the maximum line-to-line voltage. Based on previous analysis, the minimum DC voltage is express as:

$$\begin{aligned} V_{dc\_\min} &= \max(\sqrt{2}V_s, \sqrt{2}V_{ac}) \\ &= \max(\sqrt{2}V_s, \sqrt{2}\sqrt{V_s^2 + V_s^2 - 2V_s^2\cos(\theta)}) \\ &= \begin{cases} \max(\sqrt{2}V_s, \sqrt{4V_s^2 - 4V_s^2\cos(\frac{1}{2}(\varphi - \frac{\pi}{2}))}), when -\frac{\pi}{2} < \varphi \le \pi \\ \max(\sqrt{2}V_s, \sqrt{4V_s^2 + 4V_s^2\cos(\frac{1}{2}(\varphi - \frac{\pi}{2}))}), when -\pi \le \varphi \le -\frac{\pi}{2} \end{cases} \end{aligned} \quad . \qquad (2.22)$$

The DC voltage requirement for different φ is shown in Figure 25. By choosing V_s as the base

voltage value, the DC voltage requirement reaches maximum value 2 pu, when φ = π/2.

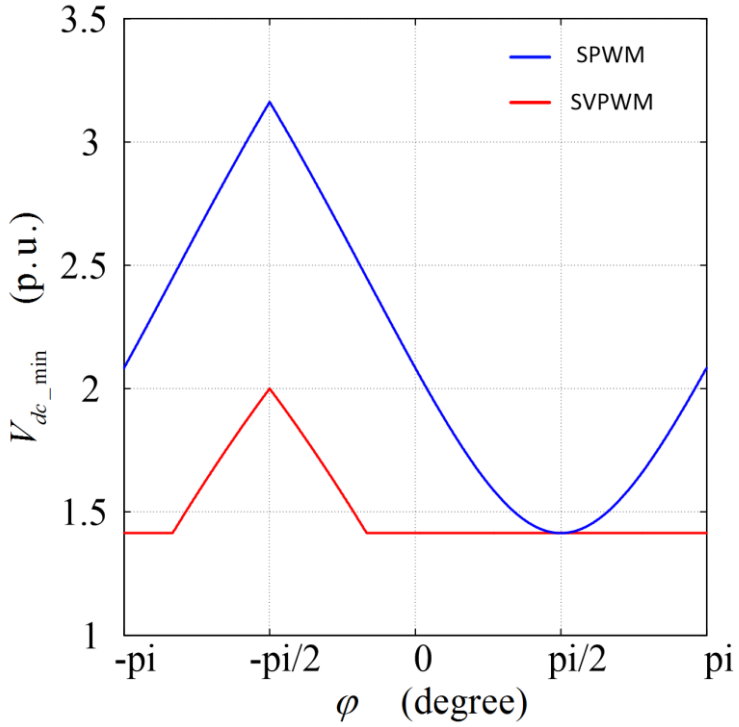


Figure 25: DC voltage requirement for different φ.

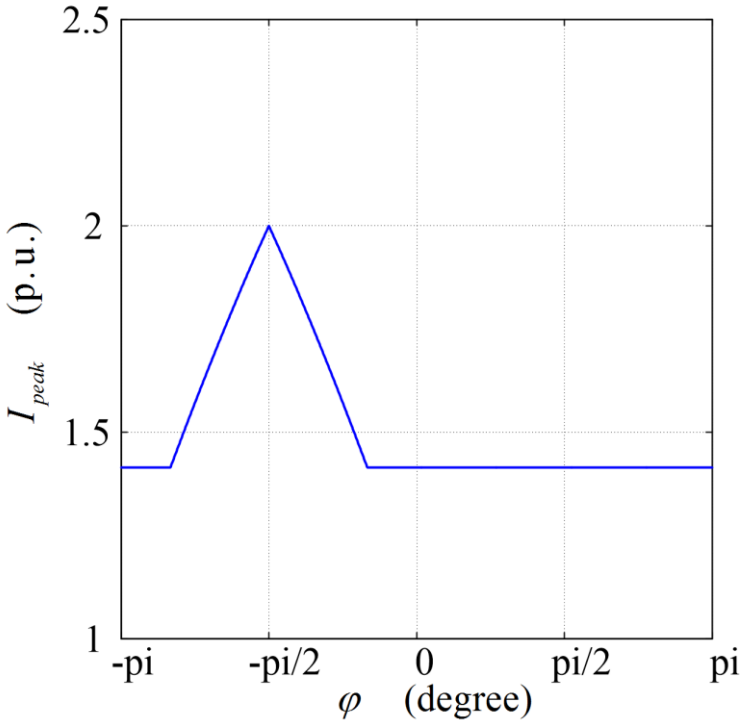


Figure 26: Switches' current stress for different φ.

In order to simplify the current stress analysis, the current stress of all switches is determined by the maximum peak current of three phases. Based on previous analysis, the switches' current stress is express as:

$$\begin{aligned} I_{peak} &= \max(\sqrt{2}I_s, \sqrt{2}I_b) \\ &= \max(\sqrt{2}I_s, \sqrt{2}\sqrt{I_s^2 + I_s^2 - 2I_s^2\cos(\theta - \varphi + \frac{\pi}{2})}) \\ &= \begin{cases} \max(\sqrt{2}I_s, \sqrt{4I_s^2 - 4I_s^2\cos(\frac{1}{2}(\varphi - \frac{\pi}{2}))}), when -\frac{\pi}{2} < \varphi \le \pi \\ \max(\sqrt{2}I_s, \sqrt{4I_s^2 + 4I_s^2\cos(\frac{1}{2}(\varphi - \frac{\pi}{2}))}), when -\pi \le \varphi \le -\frac{\pi}{2} \end{cases} \end{aligned} \quad . \quad (2.23)$$

The switches' current stress for different φ is shown in Figure 26. By choosing I_s as the base current value, the switches' current stress reaches maximum value 2 pu, when φ = π/2.

Based on minimum DC voltage requirement and switches' current stress, the *TDPR* for different φ is shown in Figure 27. By choosing $S = V_s I_s$ as the base power, the *TDPR* reaches maximum value 19.3 pu, when φ = π/2.

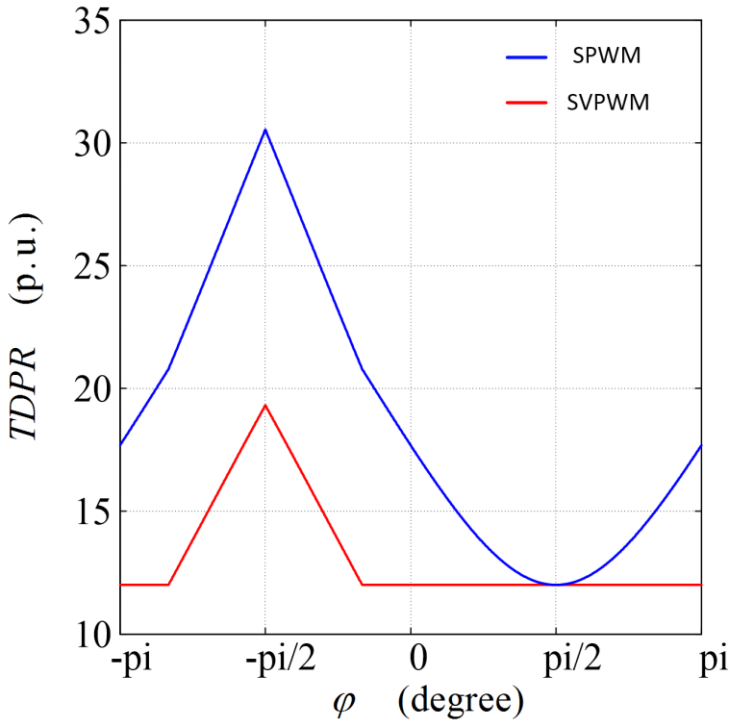


Figure 27: *TDPR* for different φ.

For SPWM, since phase A, B, C output voltages, v_a, v_b, v_c are sinusoidal, the DC voltage requirement is determined by the maximum peak value of v_a, v_b, v_c.

One possible solution [45, 46] is:

$$\dot{V}_a = \dot{V}_s / 2\,, \tag{2.24}$$

$$\dot{V}_b = -\dot{V}_s / 2\,, \tag{2.25}$$

$$\dot{V}_c = \dot{V}_{cb} + \dot{V}_b = \dot{V}_{Cac} + \dot{V}_b\,. \tag{2.26}$$

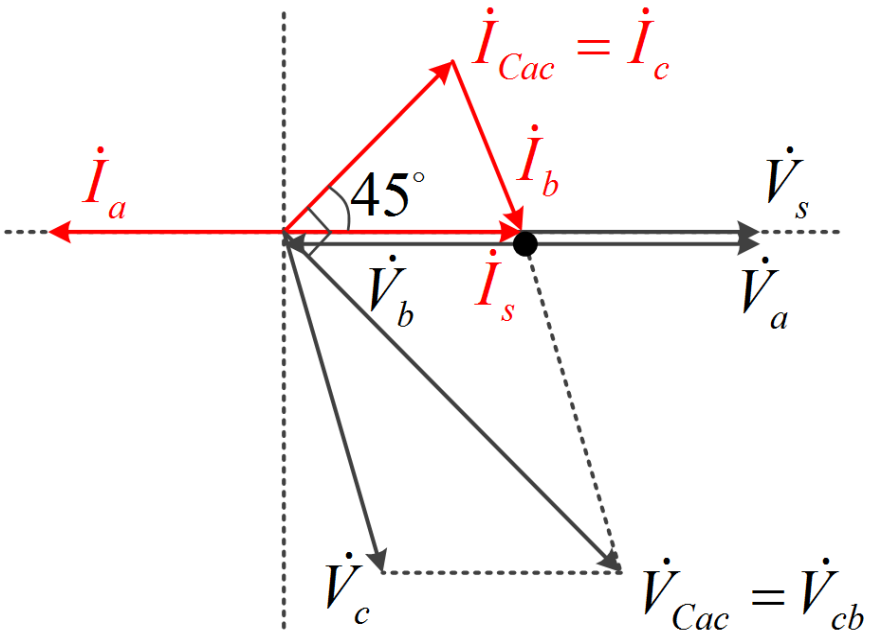


Figure 28: Phase diagram of PWM rectifier for SPWM.

Take PWM rectifier case as an example. For SVPWM, the minimum DC voltage is $\sqrt{2}V_s$. For SPWM, according to the triangle relationship, we have:

$$V_a = V_s / 2, \tag{2.27}$$

$$V_b = V_s / 2, \tag{2.28}$$

$$V_c = \sqrt{(V_s / 2)^2 + V_s^2 - \cos 45^\circ V_s^2} = 0.737 V_s. \tag{2.29}$$

The minimum DC voltage determined by the peak value of v_a, v_b, v_c. As it shown in Figure 28, v_c has the maximum peak voltage, the minimum DC voltage is $2\sqrt{2}V_c$, which is 47% larger than the DC voltage of SVPWM.

The DC voltage requirement for SPWM can be calculated by:

$$
\begin{aligned}
V_{dc\_\min} &= \max(\sqrt{2}V_s, 2\sqrt{2}V_c) \\
&= \max(\sqrt{2}V_s, 2\sqrt{2}\sqrt{(V_s/2)^2 + V_s^2 - V_s^2\cos(\theta)}) \\
&= \begin{cases} \max(\sqrt{2}V_s, \sqrt{10V_s^2 - 8V_s^2\cos(\frac{1}{2}(\varphi - \frac{\pi}{2}))}), when -\frac{\pi}{2} < \varphi \le \pi \\ \max(\sqrt{2}V_s, \sqrt{10V_s^2 + 8V_s^2\cos(\frac{1}{2}(\varphi - \frac{\pi}{2}))}), when -\pi \le \varphi \le -\frac{\pi}{2} \end{cases}
\end{aligned}
\quad . \qquad (2.30)
$$

Accordingly, the DC voltage requirement for different φ is shown in Figure 25. The switches' current stress of SPWM is the same as SVPWM in Figure 26. Similarly, *TDPR* for SPWM is calculated and is shown in Figure 27.

As we can see, compared to SPWM, SVPWM can greatly reduce the DC voltage requirement, thus reducing the *TDPR*. When $-\frac{\pi}{6} \le \varphi \le \pi$ or $-\pi \le \varphi \le -\frac{5\pi}{6}$, the DC voltage requirement and phase C switches current stress can be the same as the original H-bridge system, and the *TDPR* will be

$$TDPR = 12S = 1.5TDPR_{H-bridge}. \qquad (2.31)$$

Therefore, the TDPR for applications such as inverter, PWM rectifier and STATCOM (current leading) will be minimal.

3.5 SVPWM control

For SVPWM, the αβ transformation is defined as

$$
\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 \\ 0 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_s \\ v_{Cac} \end{bmatrix}. \qquad (2.32)
$$

According to (3.32), the trace of the space vector projected on αβ reference frame can be

obtained based on v_s and v_{Cac}. Since the line-to-line voltage of the system is unbalanced, the space vector projection on αβ reference frame is no longer a circle. Instead, the projection becomes be an ellipse or a line.

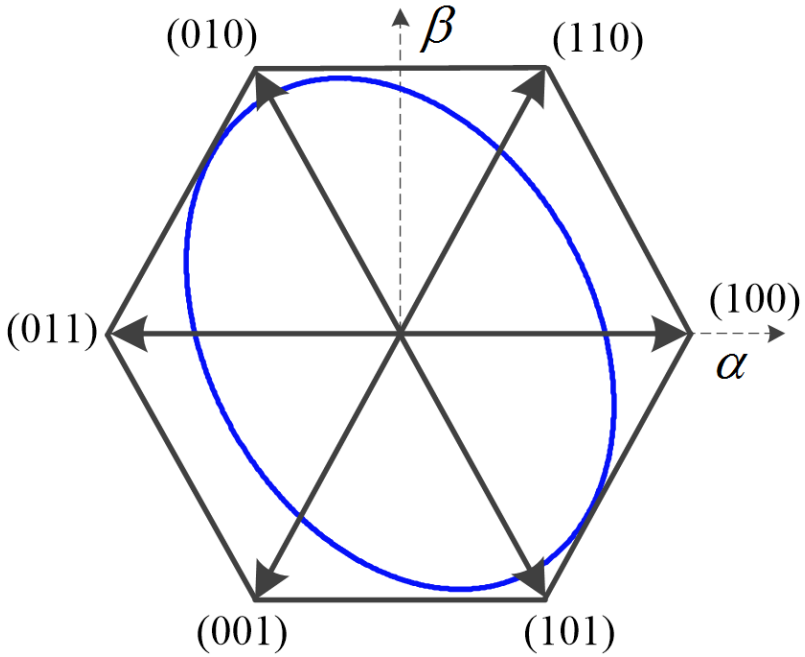


Figure 29: Space vector projections of PWM rectifier.

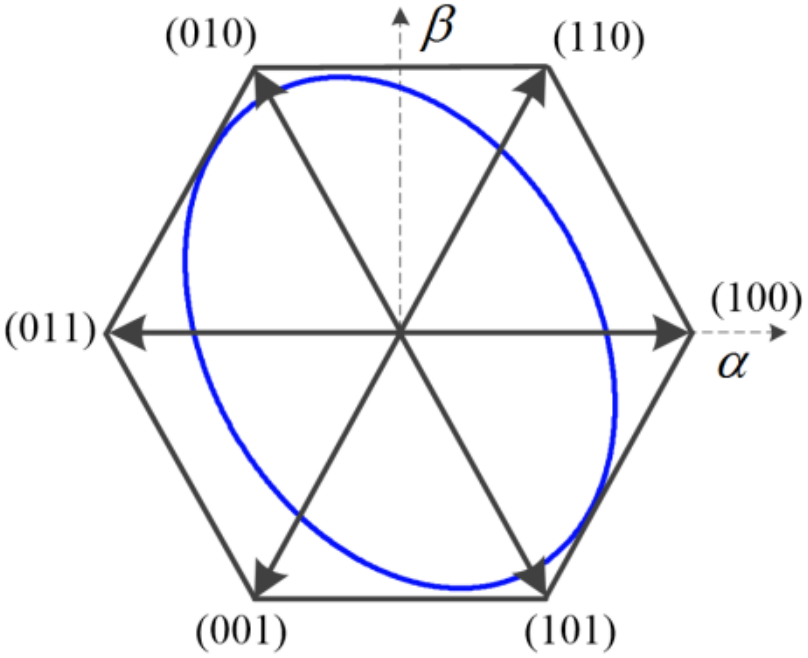


Figure 30: Space vector projections of inverter.

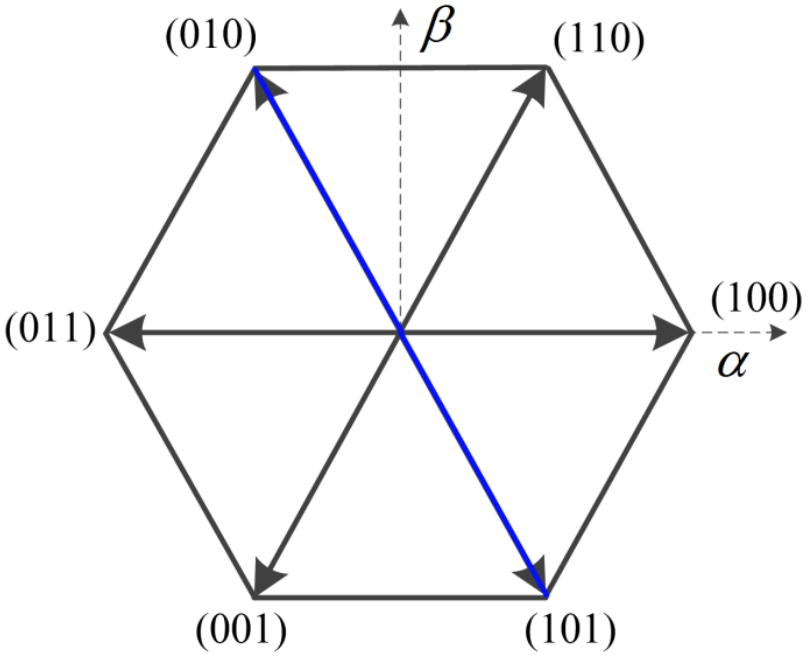


Figure 31: Space vector projections of STATCOM.

Figure 29, Figure 30, and Figure 31 show the space vector projections of PWM rectifier, inverter and STATCOM cases on αβ reference frame. The projections of PWM rectifier and inverter become an ellipse; the only difference is the moving direction of the vector: PWM rectifier is clockwise, and inverter is counterclockwise. The projection of STATCOM is a line, the vector moves back and forth along the line.

3.6 Control Strategy

In the previous analysis, the filter inductors, L_{f1} and L_{f2} are neglected for simplification. In the following analysis, in order to fully absorb the 2ω ripple power, the filter inductors are taken into consideration to calculate the voltage and current reference of C_{ac}.

Taking the reactive powers of L_{f1} and L_{f2} into account, the instantaneous power of DC capacitor from the grid side becomes:

$$\begin{aligned} p_{ab} &= v_s i_s - L_{f1}\frac{di_s}{dt} i_s = \frac{1}{2}V_s I_s \cos(\varphi) + \\ &\frac{1}{2}V_s I_s \sin(2\omega t + \varphi - \frac{\pi}{2}) - \frac{1}{2}\omega L_{f1} I_s^2 \sin(2\omega t + 2\varphi) \end{aligned}, \tag{2.33}$$

and the 2ω ripple power component is:

$$\begin{aligned} p_{ab\_2\omega} &= \frac{1}{2}V_s I_s \sin(2\omega t + \varphi - \frac{\pi}{2}) - \\ &\frac{1}{2}\omega L_{f1} I_s^2 \sin(2\omega t + 2\varphi) = \frac{1}{2}P_{ab\_2\omega} \sin(2\omega t + \varphi_{ab}) \end{aligned}. \tag{2.34}$$

where

$$P_{ab\_2\omega} = \sqrt{(V_s I_s)^2 + (\omega L_{f1} I_s^2)^2 + 2\omega L_{f1} V_s I_s^3 \sin\varphi}\,, \tag{2.35}$$

$$\tan\varphi_{ab} = -\frac{V_s I_s \cos\varphi + \omega L_{f1} I_s^2 \sin(2\varphi)}{V_s I_s \sin\varphi - \omega L_{f1} I_s^2 \cos(2\varphi)}\,. \tag{2.36}$$

Similarly, the instantaneous power of DC capacitor from C_{ac} side becomes

$$p_{cb} = v_{Cac} i_{Cac} - L_{f2} \frac{di_{Cac}}{dt} i_{Cac}$$
$$= \frac{1}{2} \frac{V_{Cac}^2}{\frac{1}{\omega C_{ac}} - \omega L_{f2}} \sin(2\omega t + 2\theta) . \quad (2.37)$$

The power from C_{ac} side should be controlled equal to the 2ω ripple power from the grid side:

$$p_{cb} = p_{ab\_2\omega} . \quad (2.38)$$

Therefore, the magnitude and phase of v_{Cac} should be:

$$V_{Cac} = \sqrt{P_{ab\_2\omega} (\frac{1}{\omega C_{ac}} - \omega L_{f2})} , \quad (2.39)$$

$$\theta = \frac{1}{2} \varphi_{ab} . \quad (2.40)$$

and the magnitude of i_{Cac} should be:

$$I_{Cac} = \frac{V_{Cac}}{\frac{1}{\omega C_{ac}} - \omega L_{f2}} . \quad (2.41)$$

Figure 32 shows the control system, which consists of two control loops. The first one is to control the grid current and the second one is to control the voltage and current of the ac capacitor. The sampling frequency is 20 kHz; L_{fs1} and L_{fs2} are designed to be 4.5% and 1.5% respectively.

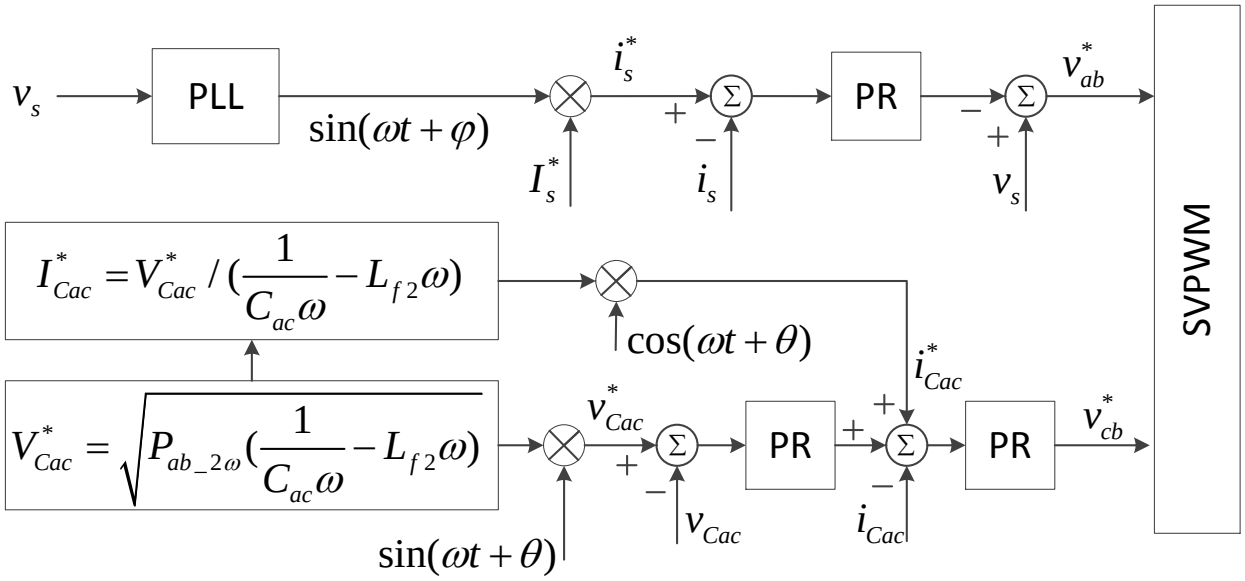


Figure 32: Control System for DC-capacitor-less single phase system.

A proportional-resonant (PR) controller is adopted for the grid current control [64-68]. The transfer function of PR controller is:

$$G_{PR}(\mathrm{s}) = k_p + \frac{2k_r\omega_c s}{s^2 + 2\omega_c s + \omega_o^2}. \tag{2.42}$$

And the bode plot of PR controller is shown in Figure 33.

The transfer function from V_{ab} to grid current, i_s is

$$G_{is\_vab}(\mathrm{s}) = \frac{1}{L_{fs1}s}. \tag{2.43}$$

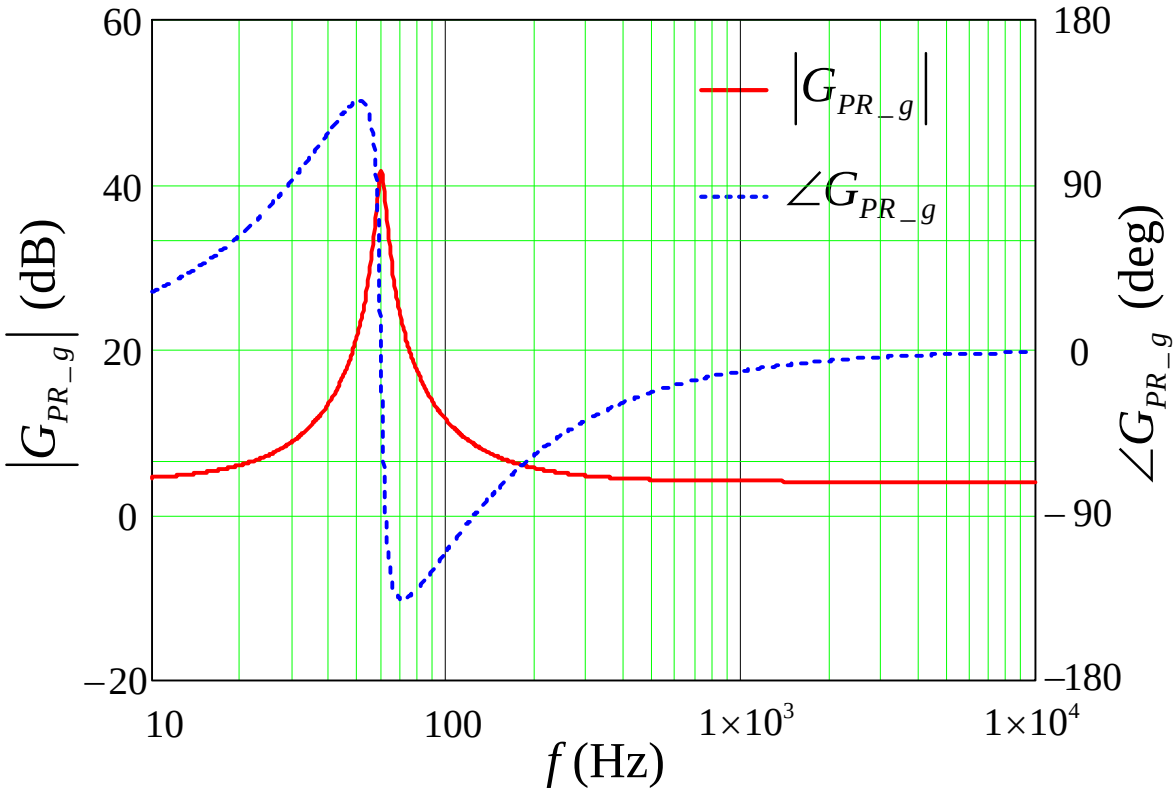


Figure 33: Grid current PR controller.

Taking the delay caused by sampling time, T_s, the grid current loop transfer function is:

$$G_{g\_loop}(s)=G_{PR\_g}(s)\cdot G_{is\_vab}(s)\cdot\frac{1-e^{-sT_s}}{sT_s}. \tag{2.44}$$

PR controller parameters are as follows: k_p=24, k_r=90, ω_c=25; and the bode plot of grid current loop transfer function is shown in Figure 34

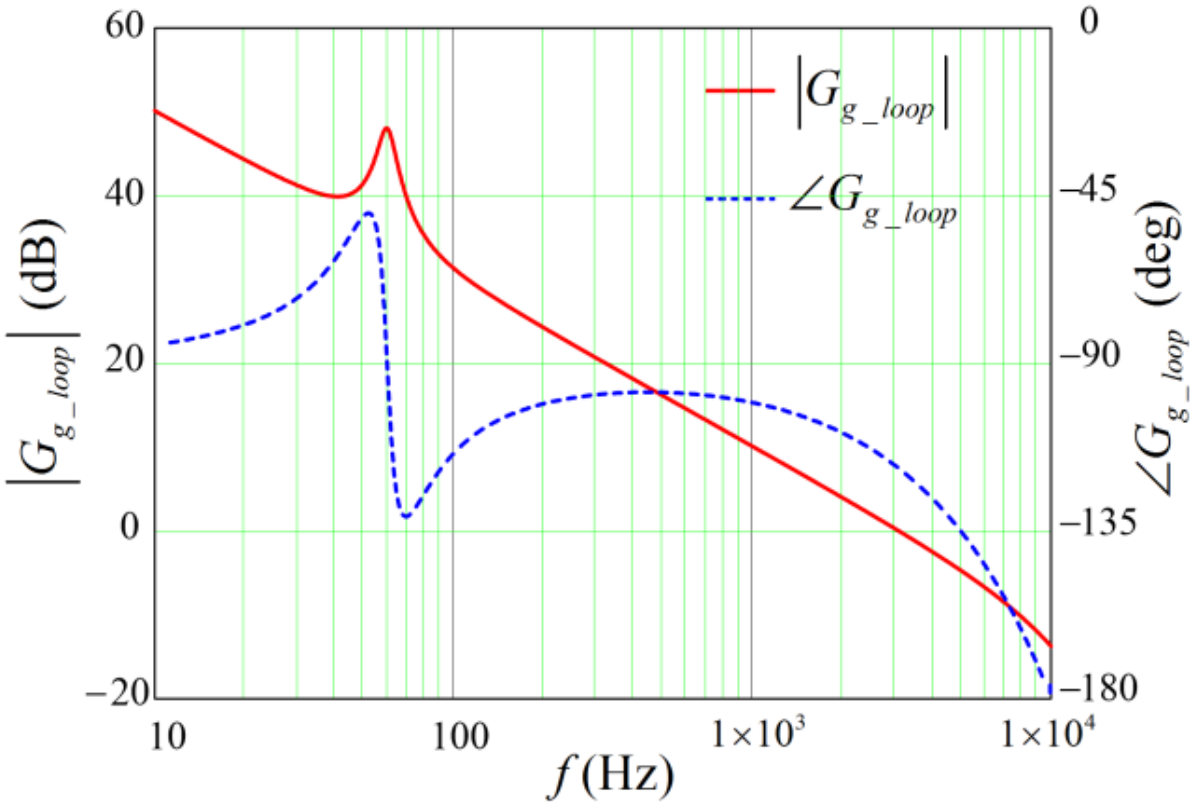


Figure 34: Grid current loop.

For the control of AC capacitor, dual loop structure is used: the outer voltage loop and inner current loop. For current inner loop, the transfer function from V_{cb} to AC capacitor current, i_{Cac} is:

$$G_{ic\_vcb}(\mathrm{s}) = \frac{1}{L_{fs2}s + \dfrac{1}{C_{ac}s}}. \tag{2.45}$$

The AC capacitor current loop transfer function is:

$$G_{i\_loop}(\mathrm{s}) = G_{PR\_i}(\mathrm{s}) \cdot G_{ic\_vcb}(\mathrm{s}) \cdot \frac{1 - e^{-sT_s}}{sT_s}. \tag{2.46}$$

PR controller parameters are as follows: k_p=8, k_r=11, ω_c=50; and the bode plot of AC capacitor current loop transfer function is shown in Figure 35

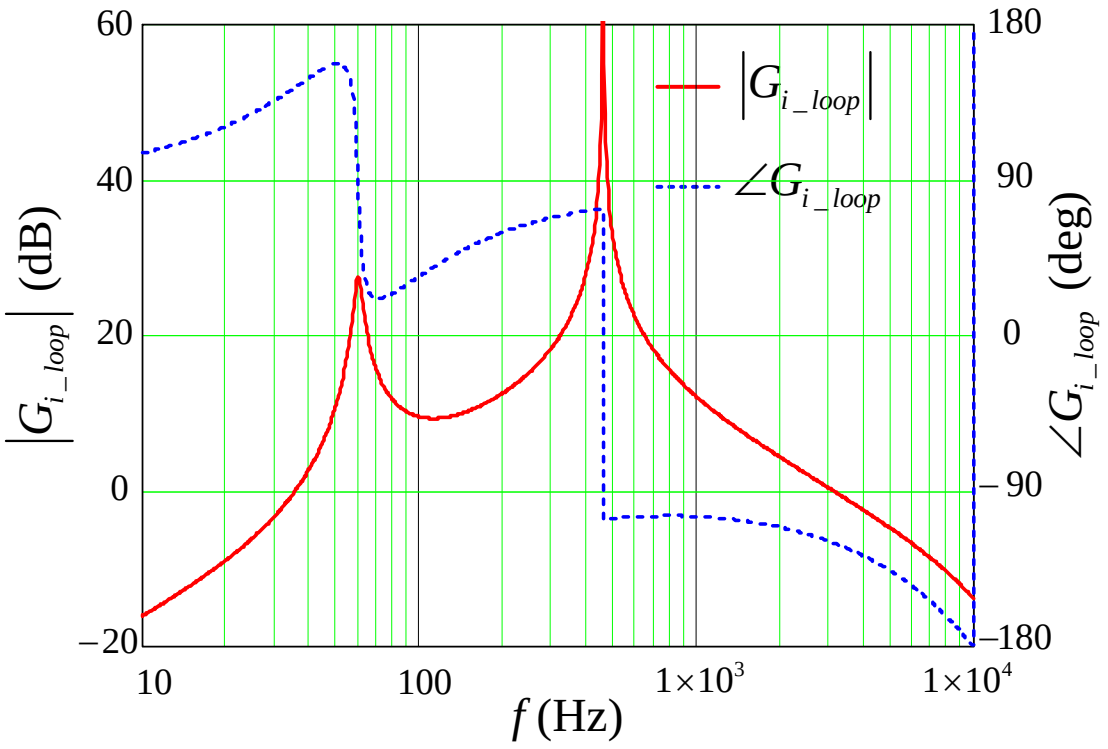


Figure 35: AC capacitor current loop.

Accordingly, the transfer function from AC capacitor current reference to AC capacitor current is:

$$G_i(\mathrm{s}) = \frac{G_{i\_loop}(\mathrm{s})}{G_{i\_loop}(\mathrm{s}) + 1}. \tag{2.47}$$

The bode plot of the transfer function from AC capacitor current reference to AC capacitor current is shown in Figure 36

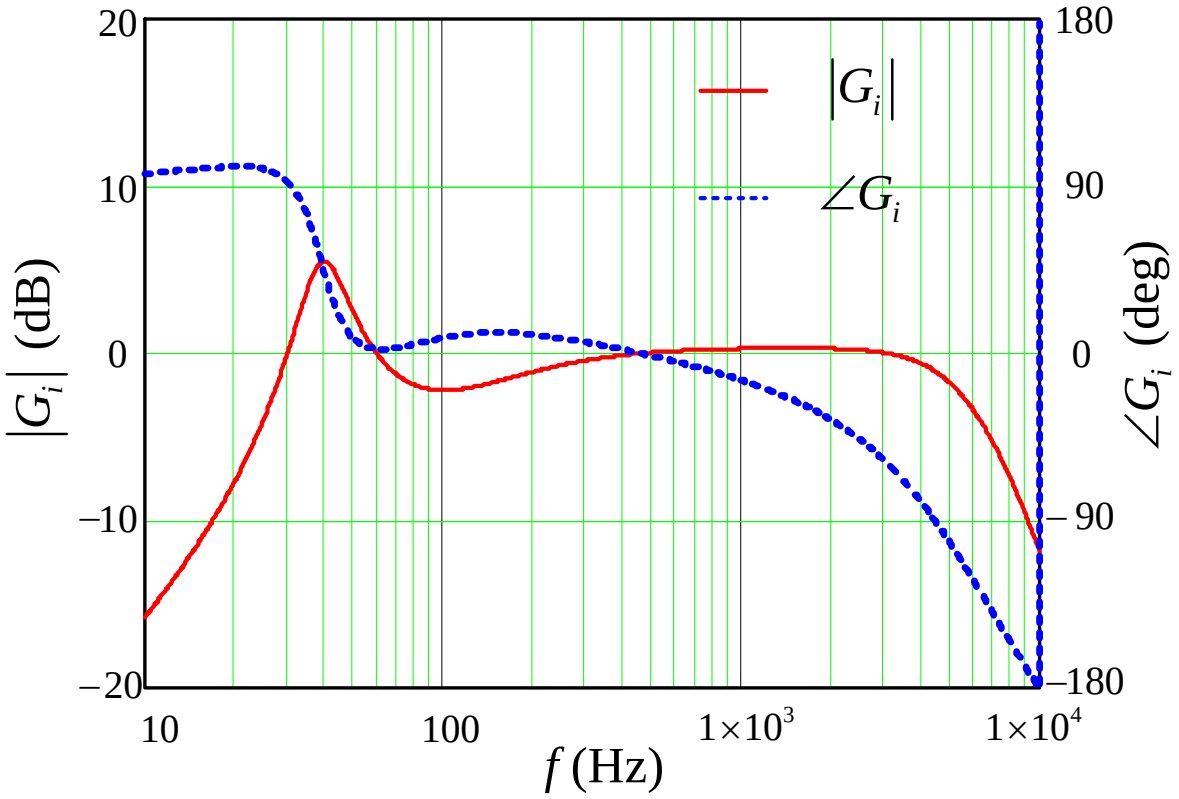


Figure 36: Transfer function from AC capacitor current reference to AC capacitor current.

For the voltage outer loop, the transfer function from AC capacitor current to AC capacitor voltage is:

$$G_{vc\_ic}(\mathrm{s}) = \frac{1}{C_{ac}s}. \tag{2.48}$$

The AC capacitor voltage loop transfer function is:

$$G_{v\_loop}(\mathrm{s}) = G_{vc\_ic}(\mathrm{s}) \cdot G_i(\mathrm{s}) \cdot G_{PR\_v}(\mathrm{s}) \cdot \frac{1-e^{-sT_s}}{sT_s}. \tag{2.49}$$

PR controller parameters are as follows: k_p=1.8, k_r=5, ω_c=25; and the bode plot of AC capacitor voltage loop transfer function is shown in Figure 37.

As it shown in Figure 35 and Figure 37, by using dual loop control, the AC capacitor control

loop can achieve an acceptable bandwidth to track the voltage and current reference.

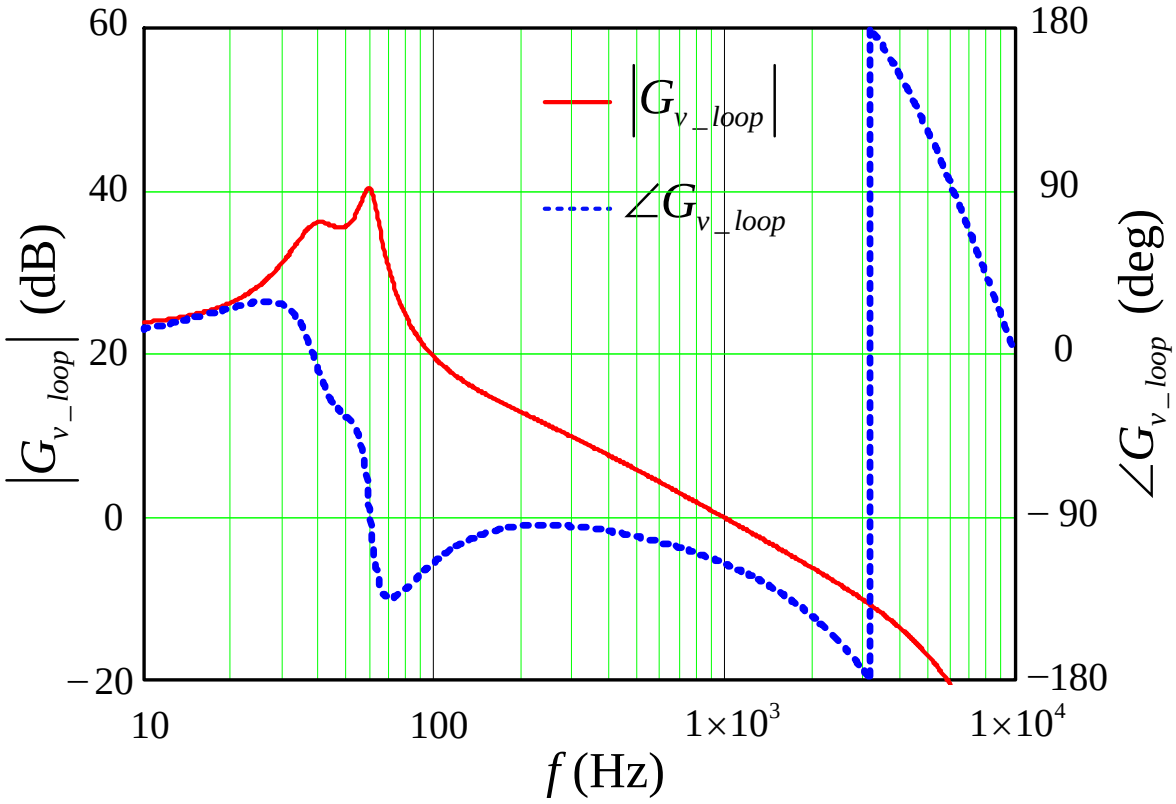


Figure 37: AC capacitor voltage loop.

3.7 Experimental results

To verify the effectiveness of the proposed DC capacitor-lees inverter and the active power decoupling method, a 1.5-kVA single phase power conversion system for PWM rectifier, inverter and STATCOM is designed. The key parameters are listed below in Table 2.

Table 2: Key Parameters for DC capacitor-less inverter system

DC voltage, V_{dc}	185 V
switching frequency, f_{sw}	10 kHz
DC capacitance, C_{dc}	170 μF (0.55 pu)
grid voltage, V_s	120 VAC (60 Hz)
AC capacitance, C_{ac}	300 μF (1 pu)
filter inductance, L_{f1}	1.2 mH (0.045 pu)
filter inductance, L_{f2}	0.4 mH (0.015 pu)

For conventional H-bridge system, if the allowed DC voltage ripple is 2.5% of DC average voltage, the DC capacitance is 4.6 mF (15.5 pu). For the proposed single phase power conversion system, since the 2ω ripple power can be absorbed by AC capacitor, theoretically DC capacitor only needs to absorb switching current ripple, of which the capacitance is 100 μF (0.33 pu) [69, 70].

However, in practice, considering the other frequency ripple power which has not been compensated by AC capacitor, the DC capacitance is designed to be 170 μF (0.55 pu). The calculated AC energy storage capacitor is 300 μF (1 pu). Compared to conventional H-bridge system, the proposed DC capacitor-less inverter reduces the total size of the capacitor (including DC capacitor and AC capacitor) by 10 times.

The filter inductance L_{f1} is larger than L_{f2} because the system is connected to grid through an isolated transformer; and the transformer leakage inductance is also taken into account.

For the filter inductance L_{f2}, trade-off design is necessary. With smaller L_{f2}, the size of passive component can be reduced. One the other hand, with smaller L_{f2}, the current switching

ripple of i_{Cac} is larger, which may cause higher power losses. Here, L_{f2} is designed to be 0.4 mH (0.015 pu), to make the current ripple within 20%.

Figure 38, Figure 39, and Figure 40 show the simulation results of PWM rectifier, inverter, and STATCOM cases. v_a^*, v_b^*, v_c^* are the reference signals for controlled voltage sources v_a, v_b, v_c. Since SVPWM is adopted, the reference signals are not sinusoidal, and the DC voltage can be fully utilized. The average value of v_{dc} is 185 V and the ripple voltage is within 3 V (1.5%). The relationship between v_s, v_{Cac}, i_s, and i_{Cac} is consistent with the theoretical analysis.

A 1.5-kVA prototype of proposed DC-capacitor-less inverter for single phase power conversion has been built.

Figure 41, Figure 42, and Figure 43 show the experimental key waveforms of PWM rectifier, inverter and STATCAOM cases. The average DC voltage is 185 V. For all cases, the voltage ripple is within 5 V (2.5%).

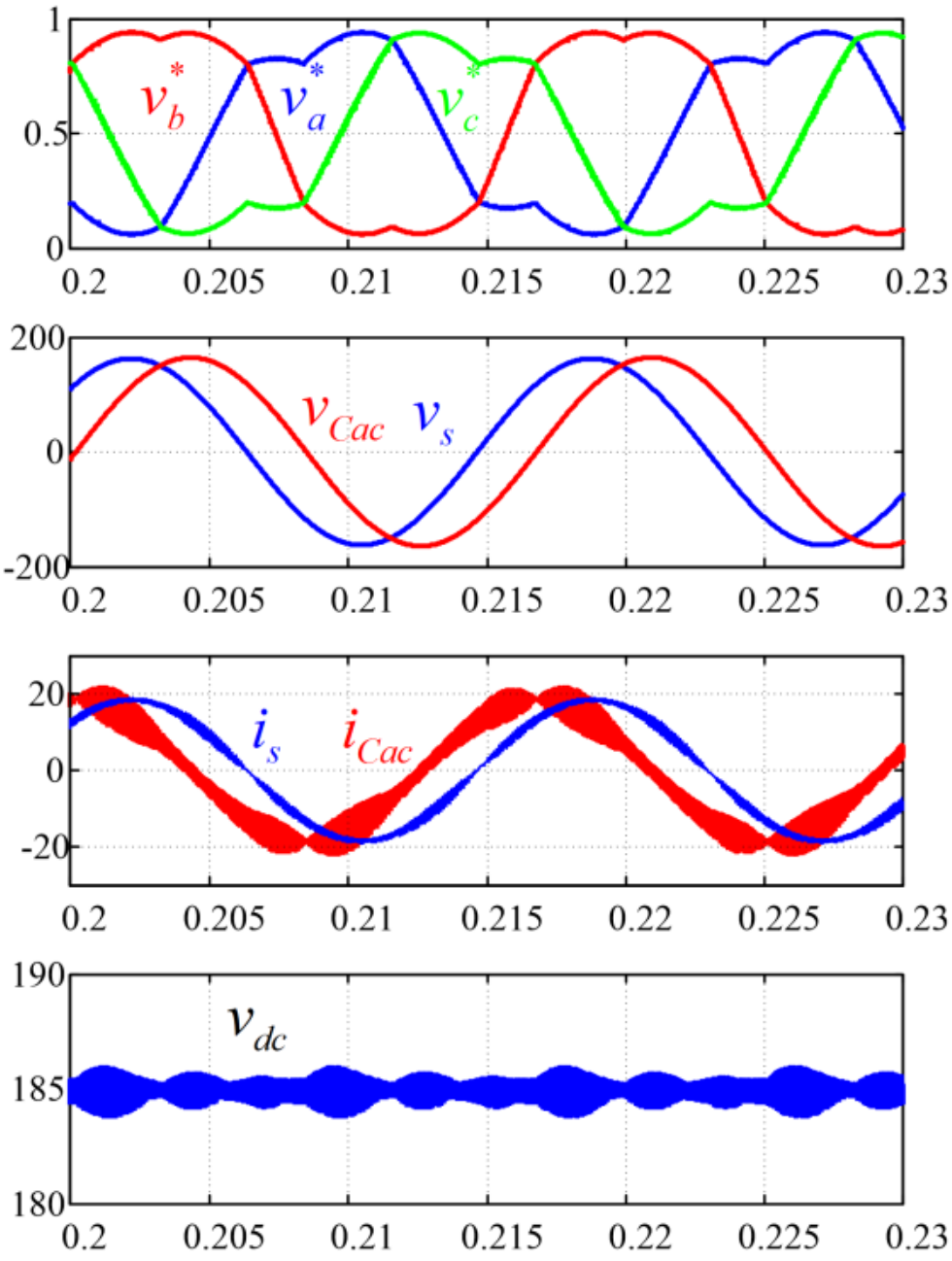


Figure 38: Simulation results PWM rectifier (PF = 1).

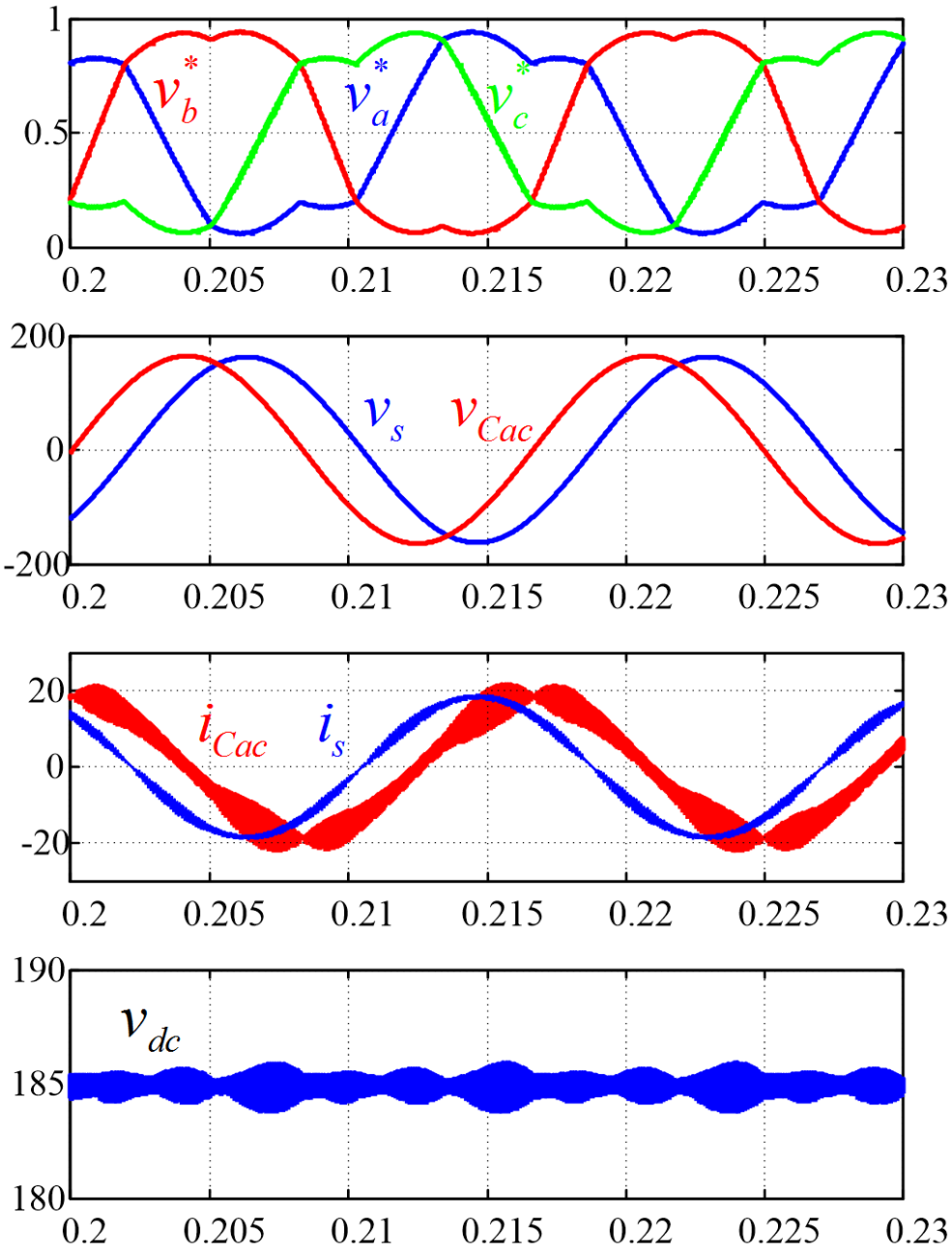


Figure 39: Simulation results inverter (PF = -1).

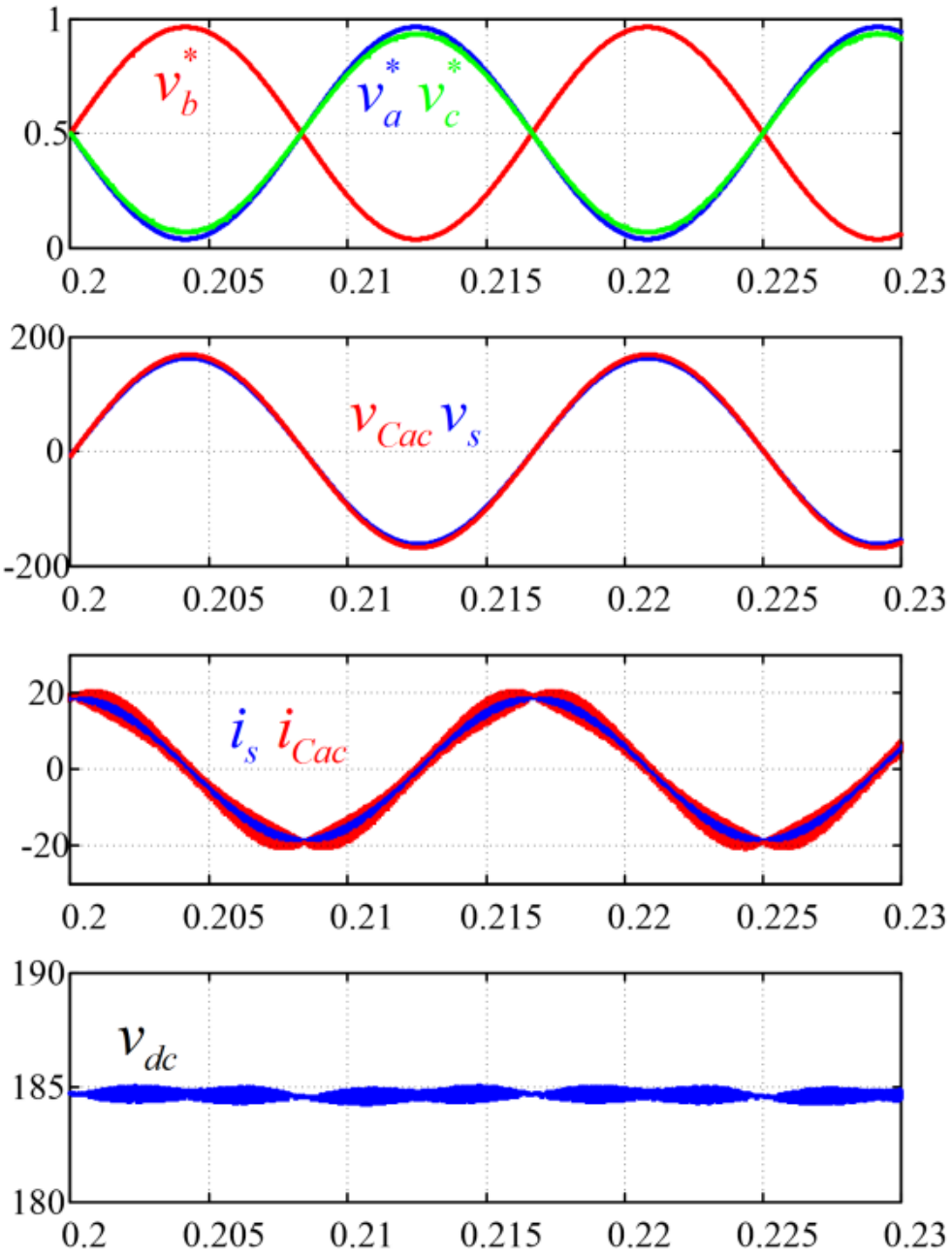


Figure 40: Simulation results STATCOM (PF = 0, current leading voltage).

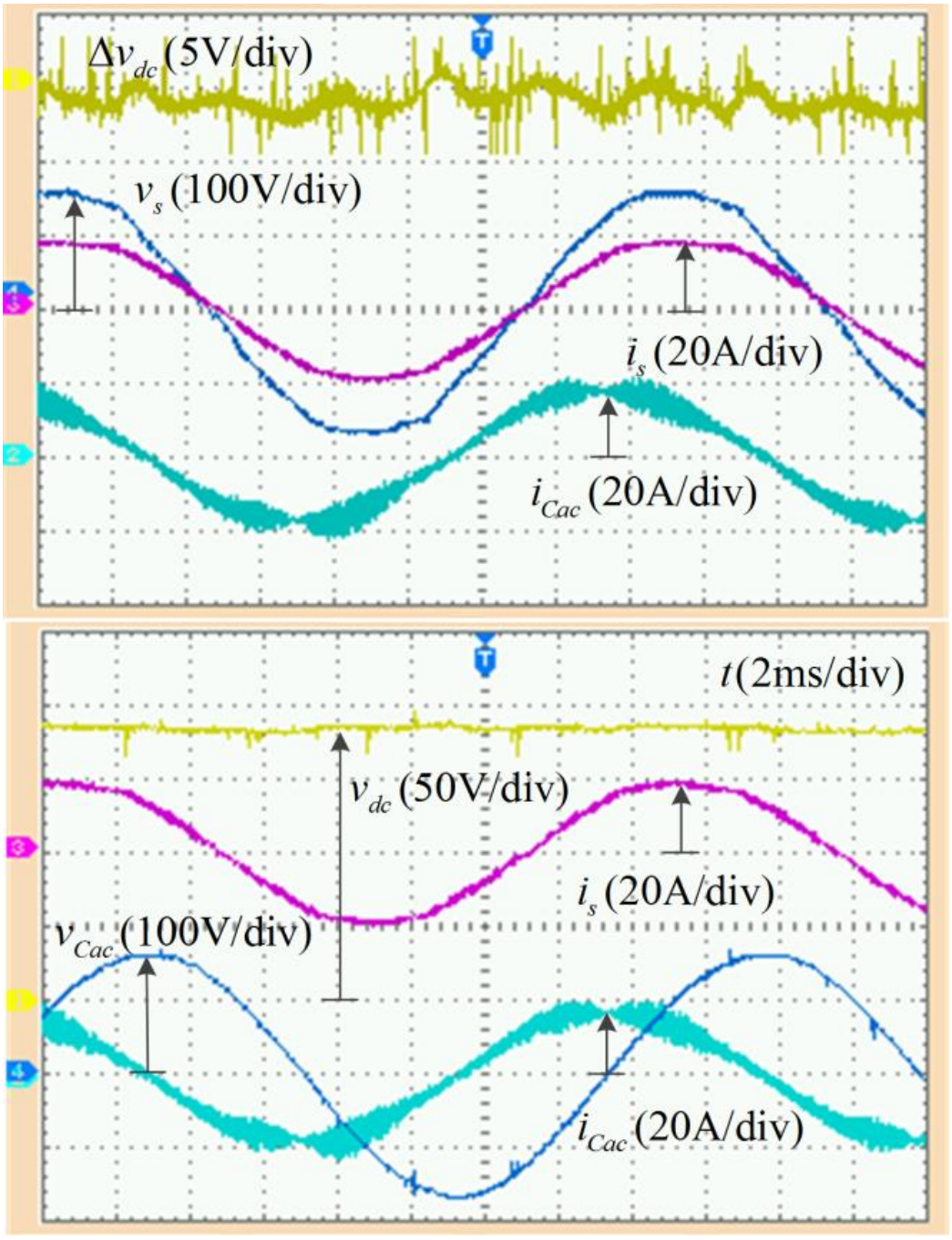


Figure 41: Experimental key waveforms for PWM rectifier.

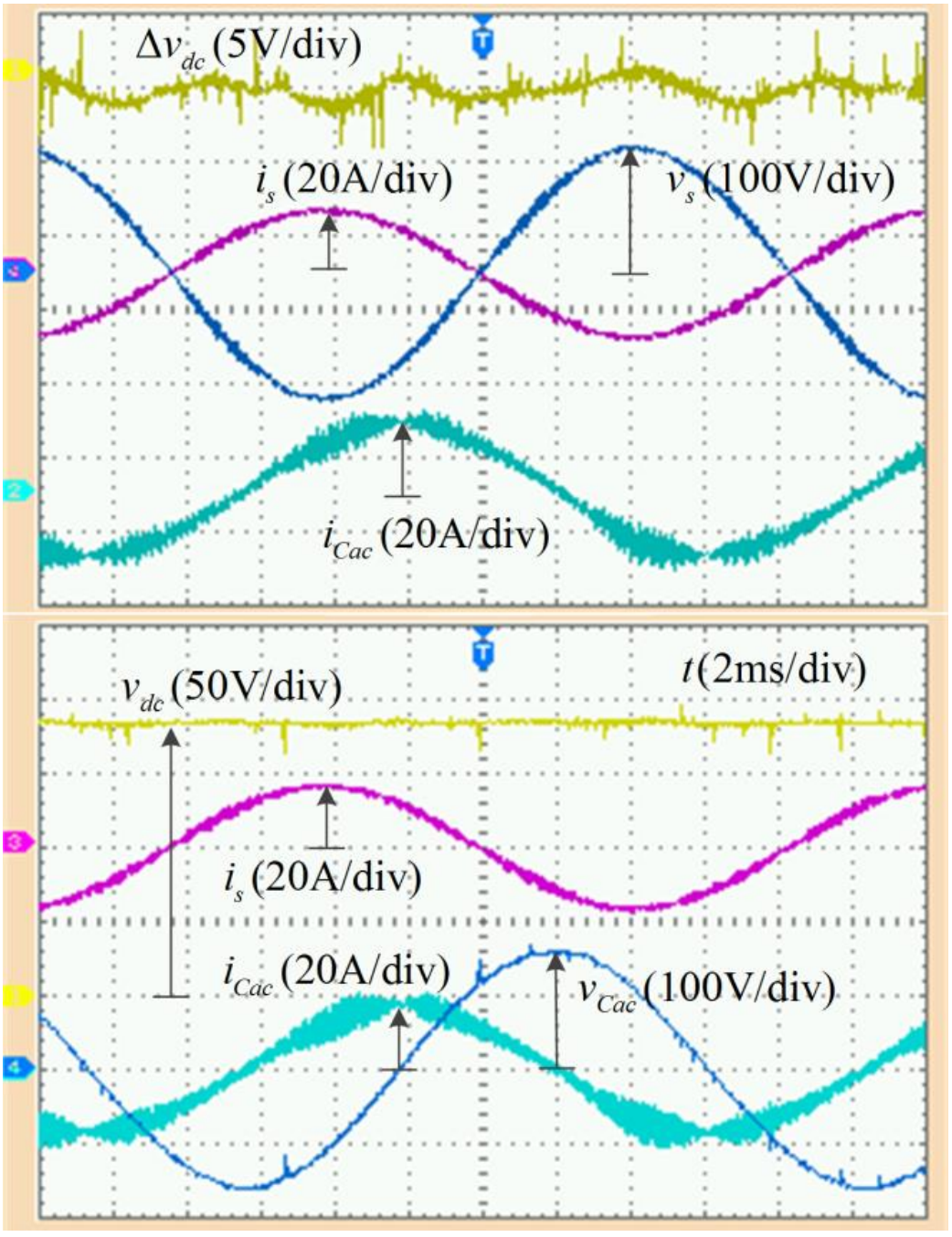


Figure 42: Experimental key waveforms for inverter.

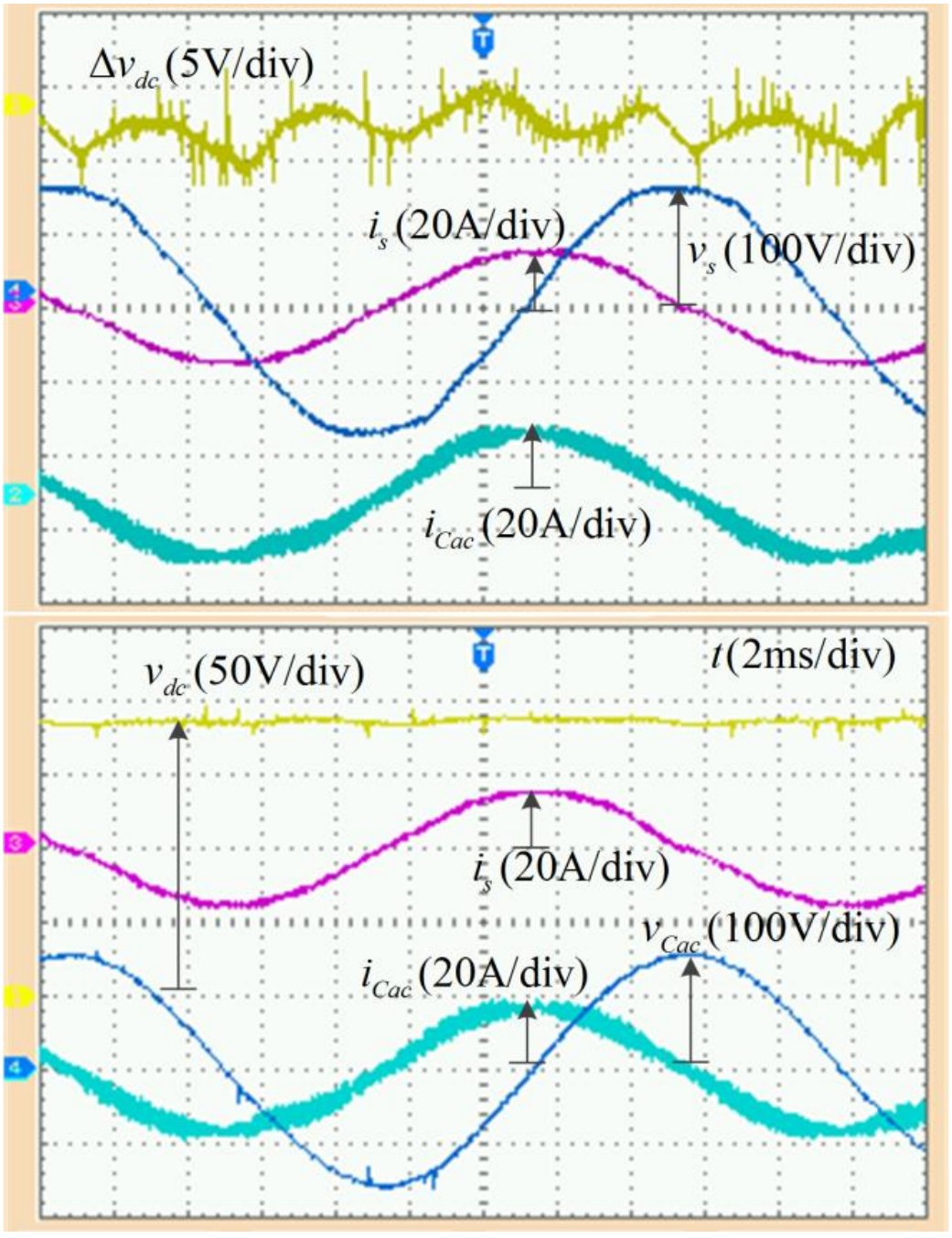


Figure 43: Experimental key waveforms for STATCOM.

Figure 44 shows the DC ripple FFT analysis of PWM rectifier, inverter and STATCAOM cases. The 2ω (120 Hz) voltage is within 0.5V, indicating that the DC capacitor-less inverter and power decoupling method have effectively absorbed the 2ω ripple power.

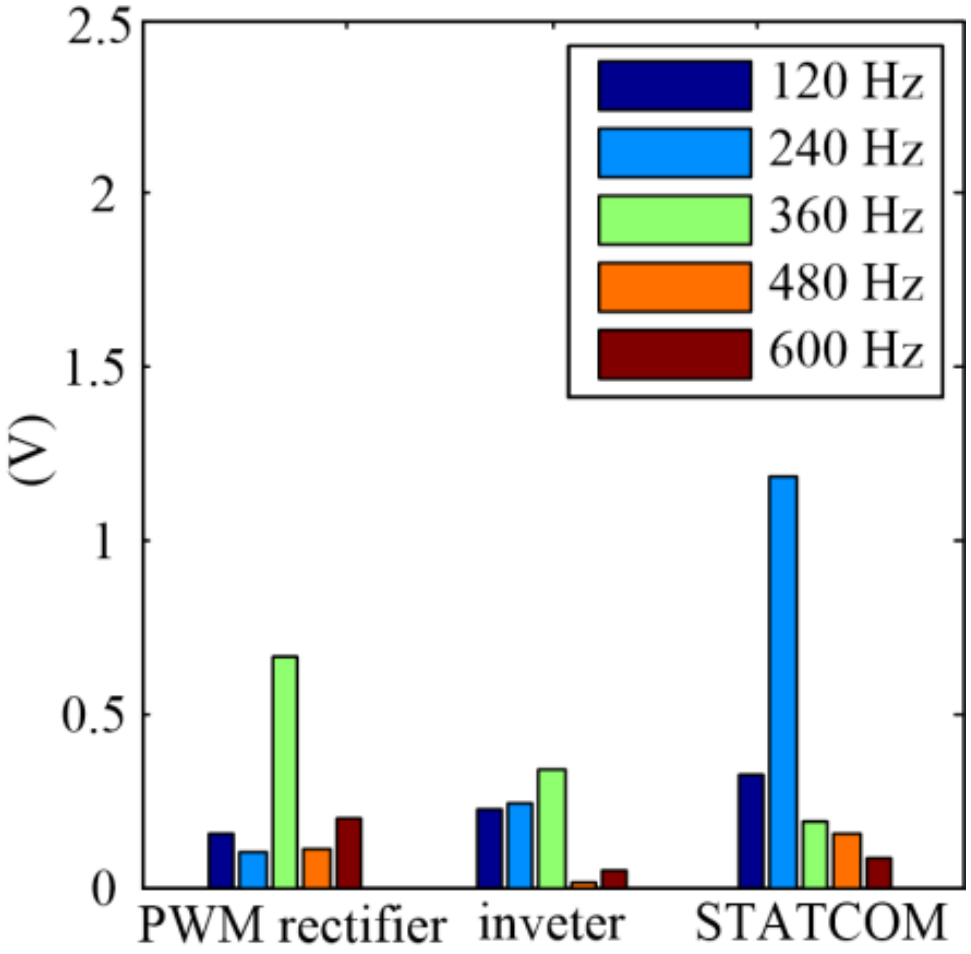


Figure 44: DC ripple FFT analysis.

3.8 Conclusions

A DC-capacitor-less inverter with SVPWM control for single-phase power conversion with minimum voltage and current stress is proposed. Only an AC capacitor to absorb 2ω ripple power and a minimum DC capacitor to absorb the switching ripple power are needed. By adopting SVPWM control and choosing the optimum AC capacitance and the voltage reference,

the voltage and current stress of the switches can be minimized. The size of the capacitor is reduced by 10 times.

A detailed analysis and comparison between SVPWM and SPWM control show that the SVPWM can significantly reduce the voltage stress and that the DC voltage requirement remains the same as conventional H-bridge inverter for PWM rectifier, inverter and STATCOM cases.

A dual loop with outer voltage loop and inner current loop is designed for AC capacitor control. The detailed controller design analysis shows that the control system has enough bandwidth track the AC capacitor voltage and current reference.

Theoretical analysis and experimental results have been presented. The simulation and experimental waveforms are consistent with the theoretical analysis.

CHAPTER 4 SOLID STATE VARIABLE CAPACITOR

In this chapter, an important application of DC-capacitor-less inverter with SVPWM: solid state variable capacitor (SSVC) is investigated. A variable AC capacitor (with capacitance variable from 0 to C_{ac}) is traditionally implemented by an H-bridge inverter and a bulky electrolytic DC capacitor with capacitance of 20 times the AC capacitance value, C_{ac} to absorb the ripple power pulsating at twice the line frequency (2ω ripple power).

The SSVC based on DC-capacitor-less inverter with SVPWM shows special advantage in terms of the switches' current and voltage stress compared to other applications such as unity power factor inverter and PWM rectifier. The *TDPR* of SSVC based on based on DC-capacitor-less inverter is only 1.125 times of H-bridge circuit.

The SSVC system can reduce the DC capacitance to the minimal value just for absorbing switching ripples. The fixed AC capacitor controlled by the additional phase leg absorbs the 2ω component and theoretically can eliminate 2ω ripples to the DC capacitor completely. The total capacitor size is reduced by 13 times with only 12.5% increase on *TDPR* compared to H-bridge circuit.

Compared to other existing methods to reduce DC capacitor of H-bridge, the SSVC based on DC-capacitor-less inverter shows strong benefits in terms of cost of semiconductor devices and size of energy storage capacitor. Theoretical analysis of the SSVC is provided. Simulation and experimental results are shown to prove the effectiveness of the SSVC system.

4.1 Introduction

The concept of flexible AC transmission systems (FACTS) has been widely accepted as a

breakthrough for modernizing today's power grids because FACTS devices can enhance the network stability, reliability and controllability, which in turn, improve grid transmission capability and power quality [17-27]. Essentially, all FACTS devices, such as series compensator, shunt compensator and unified power flow controller (UPFC) could be theoretically represented by "ideal" variable capacitors.

Figure 45 shows an ideal variable AC capacitor, of which the capacitance can vary continuously from zero to a fixed value, C_{ac}. However, variable capacitors are not available for power grid applications, where kilo- to mega-volt-amps are needed.

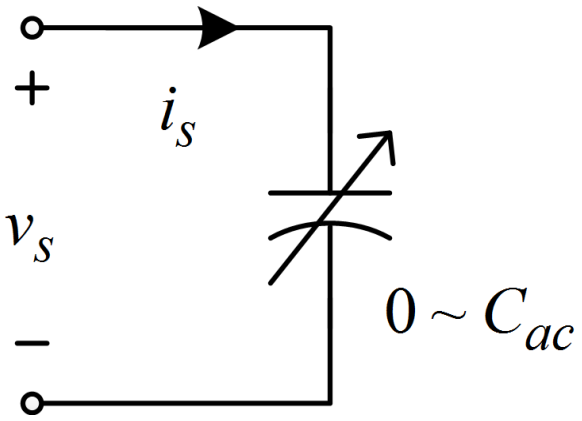


Figure 45: An ideal variable capacitor.

The DC-capacitor-less single phase power conversion system is a competitive candidate to implement a variable capacitor. The solid state variable capacitor (SSVC) shown in Figure 46 consists of an H-bridge and an additional phase leg connected to an AC capacitor with fixed capacitance, C_{ac} and can reduce the DC capacitance to the minimal value just for absorbing switching ripples.

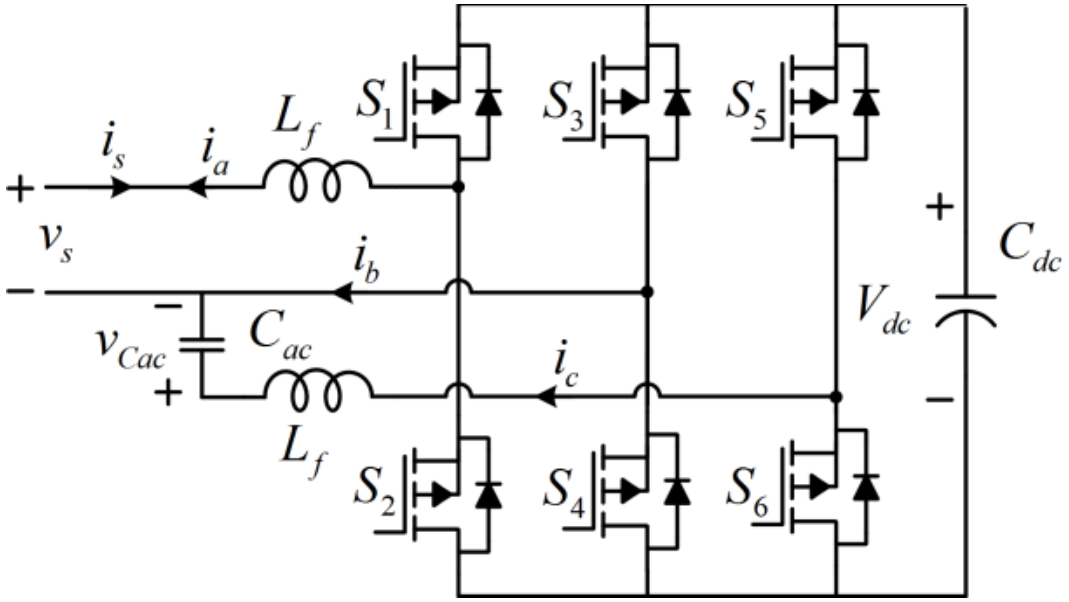


Figure 46: Proposed SSVC system configuration.

4.2 Operation of SSVC

For SSVC cases, the ideal grid voltage and the grid-side current reference will be:

$$v_s = \sqrt{2}V_s \sin(\omega t), \tag{3.1}$$

$$i_{s\_ref} = \sqrt{2}I_{s\_ref} \sin(\omega t + \frac{\pi}{2}). \tag{3.2}$$

Then the expression of grid power reference is:

$$p_s = v_s i_{s\_ref} = V_s I_{s\_ref} \sin(2\omega t). \tag{3.3}$$

Based on previous analysis, the AC energy storage capacitor, C_{ac} is designed to be

$$C_{ac} = \frac{I_s}{\omega V_s}, \tag{3.4}$$

where, I_s is the rated grid side current.

By choosing the optimal phase angle for AC capacitor reference

$$\theta = 0\,, \tag{3.5}$$

the voltage and current of C_{ac} will be:

$$v_{Cac} = \sqrt{2}V_{Cac}\sin(\omega t) = \sqrt{2}\sqrt{\frac{I_{s\_ref}}{I_s}}V_s\sin(\omega t)\,, \tag{3.6}$$

$$i_{Cac} = \sqrt{2}I_{Cac}\cos(\omega t) = \sqrt{2}\sqrt{\frac{I_{s\_ref}}{I_s}}I_s\cos(\omega t)\,. \tag{3.7}$$

Based on the grid side current and AC capacitor voltage and current, the phasor diagram of the SSVC can be obtained and shown in Figure 47.

If the phase angle of AC capacitor reference is not chosen properly as it shown in Figure 48:

$$\theta = \pi\,, \tag{3.8}$$

the voltage and current stress will be significantly increased.

According to phasor diagram relationship, V_{ac} and I_b are expressed as

$$V_{ac} = V_{ab} - V_{bc}\,, \tag{3.9}$$

$$I_b = -I_a - I_c\,. \tag{3.10}$$

For rated power, the line to line voltage of V_{ac} in Figure 47 will be 0 and the line to line voltage is determined by grid side voltage with SVPWM control. However, the V_{ac} in Figure 48 will be two times of gird side voltage, in other words, the DC voltage requirement will be two times of H-bridge circuit.

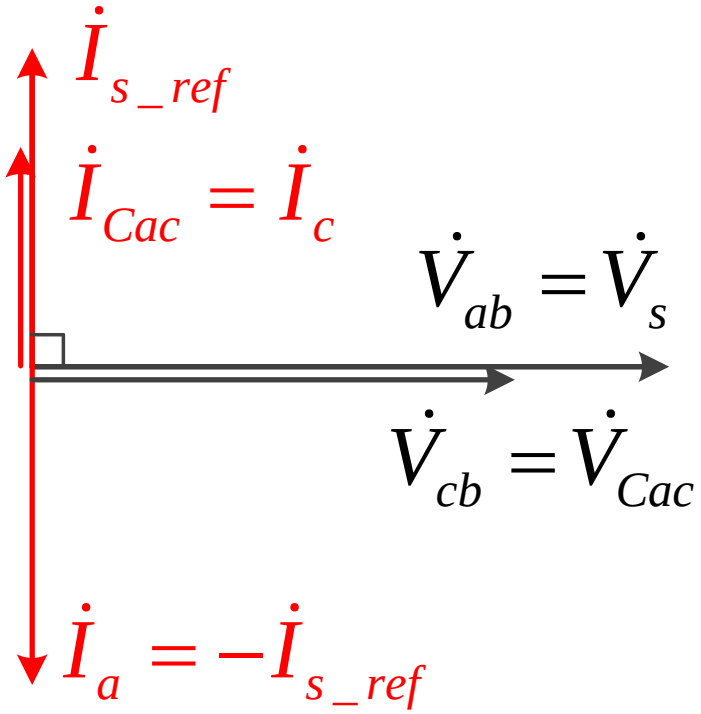


Figure 47: Phasor diagram of SSVC with optimal reference.

For rated power, the current of shred leg I_b in Figure 47 will be 0. However, the V_{ac} in Figure 48 will be two times of gird side current, in other words, the current stress of shared leg will be two times of H-bridge circuit.

If the phase angle of AC capacitor is not chosen properly, the TDPR of SSVC system will be:

$$\begin{aligned} TDPR &= 4 \cdot V_{dc} \cdot \sqrt{2} I_s + 2 \cdot V_{dc} \cdot 2\sqrt{2} I_s \\ &= 32S = 4TDPR_{H-bridge} \end{aligned}. \tag{3.11}$$

The *TDPR* is significantly increased with non-optimal phase angel for AC capacitor reference, which is 4 times of H-bridge.

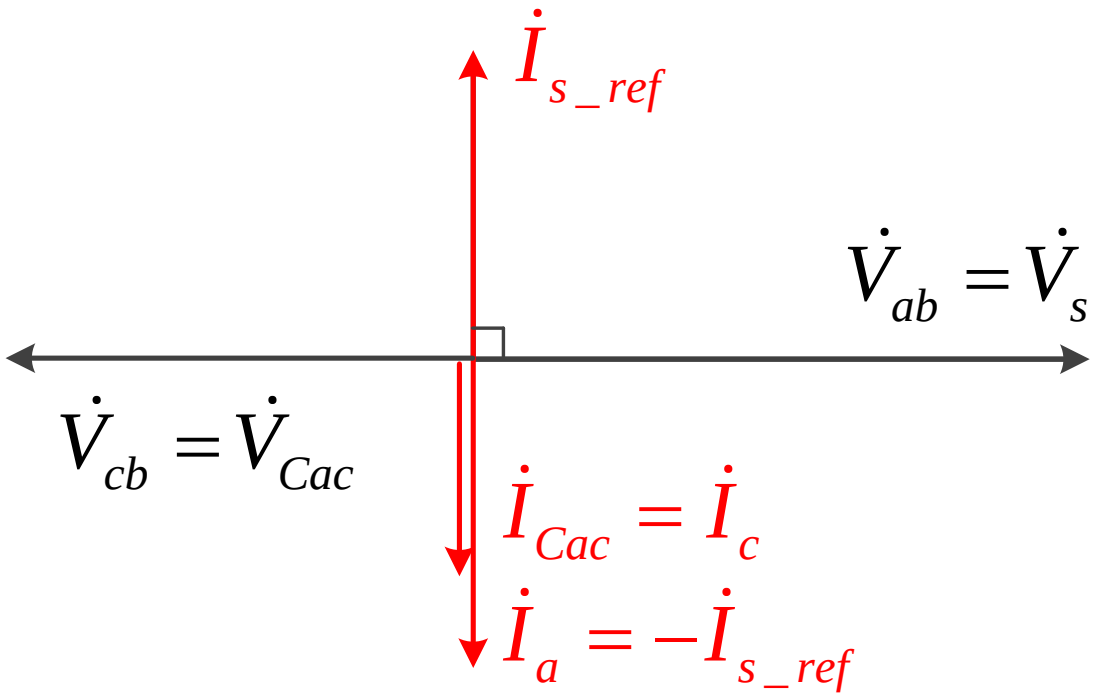


Figure 48: Phasor diagram of SSVC with non-optimal reference

By choosing the optimal phase angle for AC capacitor reference, the voltage stress can be reduced to the same as H-bridge circuit, and the shared leg current stress will be much lower, a detailed analysis to show the benefit is provided in the following section.

By adopting the SVPWM control method, the trace of the space vector projected on αβ reference frame can be obtained based on v_s and v_{Cac}. Since the line-to-line voltage of the system is unbalanced, the space vector projection on αβ reference frame is no longer a circle. Instead, the projection becomes be a line.

Figure 49 shows the space vector projections of SSVC on αβ reference frame. The projection of STATCOM is a line, the vector moves back and forth along the line. SVPWM control for SSVC will be a special case; the generated reference for phase A, B and C leg by SVPWM control will be:

$$v_a^* = -v_b^* = \frac{1}{2} v_{ab}^*, \tag{3.12}$$

$$v_c^* = v_b^* + v_{cb}^*. \tag{3.13}$$

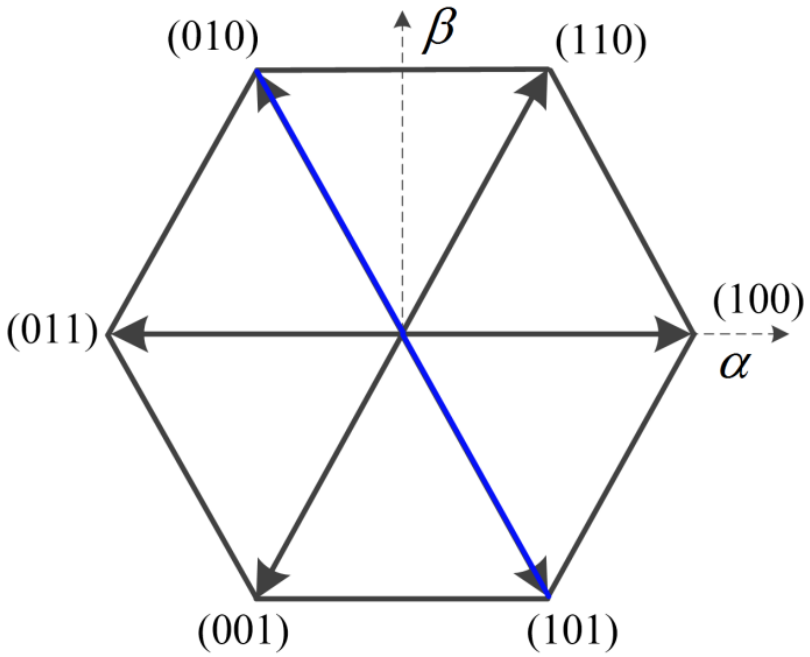


Figure 49: Space vector projections of SSVC.

4.3 Benefit of SSVC in terms of current stress on shared leg and *TDPR*

The phase A and phase C's current stress are determined by i_{s_ref} and i_{cac} respectively. Since the AC capacitor's current, i_{cac} reaches maximum when grid-side current reference equal to rated grid side current, the current stress of phase A and phase C's switches are $\sqrt{2} I_s$.

According to the three phases' current relationship, we can get

$$\dot{I}_b = -(\dot{I}_a + \dot{I}_c) = \dot{I}_s - \dot{I}_{Cac}. \tag{3.14}$$

Based on the expression of grid side current and AC capacitor current, the phase B's current, i_b can be expressed as:

$$i_b = i_{s\_ref} - i_{Cac} = \sqrt{2}(I_{s\_ref} - \sqrt{I_s \cdot I_{s\_ref}})\cos(\omega t). \tag{3.15}$$

Figure 50 shows the current magnitude of the I_b with different grid current, I_s.

As it shown in Figure 51, with rated power, i_{s_ref} and i_{Cac} are equal, then phase B's current, i_b is zero. In real system, since the grid current and AC capacitor current all have switching ripple, phase B's current will be the switching ripple current difference between i_{s_ref} and i_{cac}.

When the grid current is smaller than rated current, the maximum magnitude of i_b happens when:

$$I_{s\_ref} = I_s / 4. \tag{3.16}$$

And phase B's current will be

$$i_b = i_{s\_ref} - i_{Cac} = -\frac{\sqrt{2}}{4} I_s \cos(\omega t). \tag{3.17}$$

Therefore, the current stress of phase B is $\sqrt{2}I_s / 4$, which is only one fourth of the original H-bridge system's current stress.

According the phase to phase voltage relationship, the voltage phasor of the three phases satisfy:

$$\dot{V}_a = \dot{V}_s / 2, \tag{3.18}$$

$$\dot{V}_b = -\dot{V}_s / 2, \tag{3.19}$$

$$\dot{V}_c = \dot{V}_b + \dot{V}_{cb} = \dot{V}_{Cac} - \dot{V}_s / 2. \tag{3.20}$$

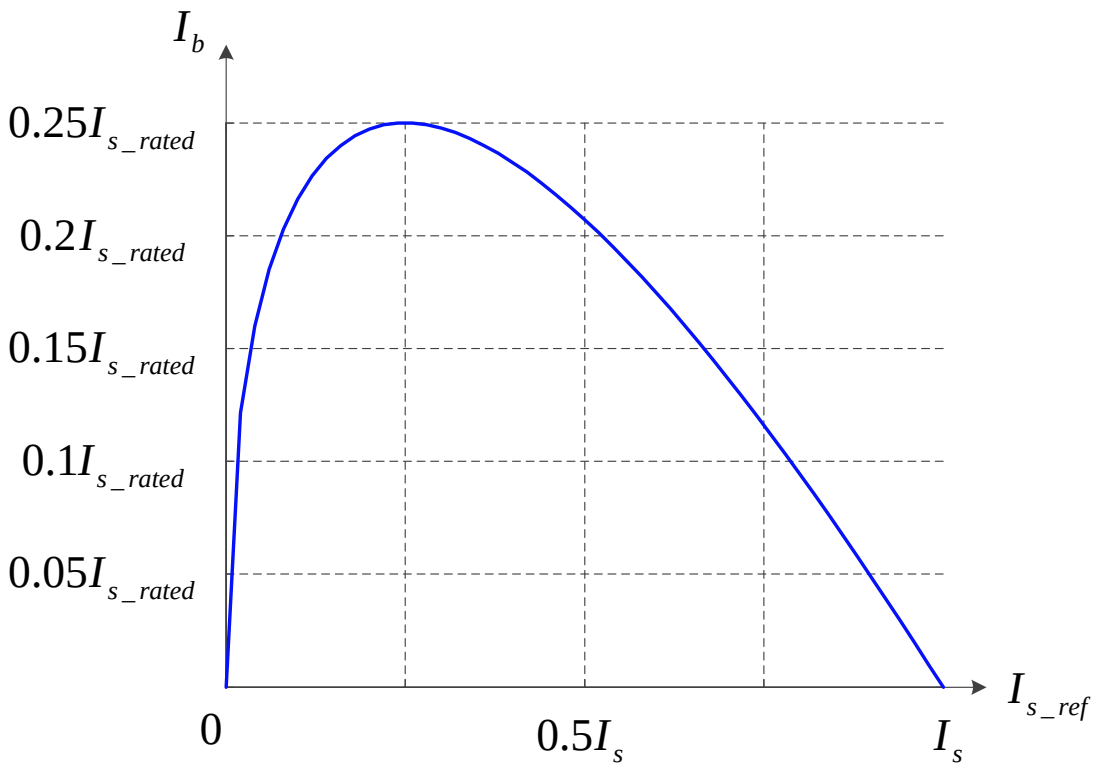


Figure 50: The magnitude of the shared leg's current, i_b with different grid current.

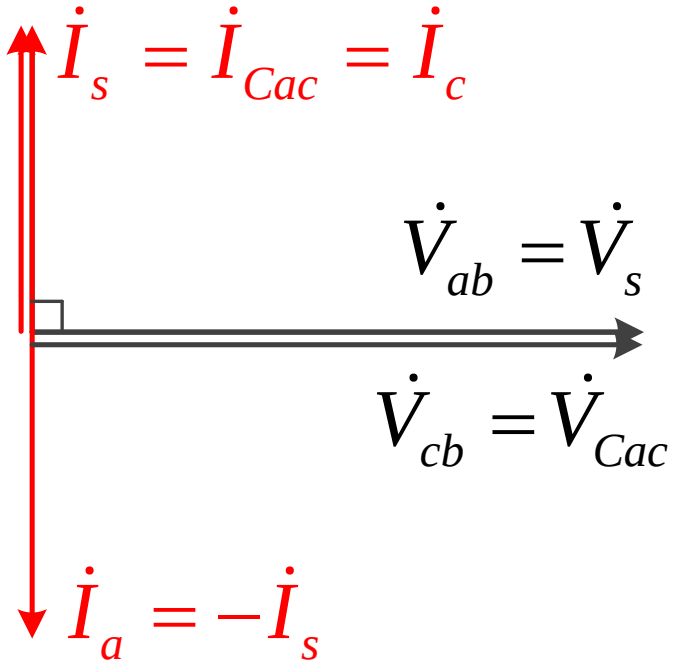


Figure 51: Phasor diagram of SSVC with rated current.

With rated power, $\dot{V}_s$ and $\dot{V}_{Cac}$ are equal, the magnitude of $\dot{V}_a, \dot{V}_b, \dot{V}_c$ are all equal to $\sqrt{2}V_s/2$. When the grid current is smaller than rated current, the magnitude of $\dot{V}_{Cac}$ are smaller than $\dot{V}_s$. None of the magnitude three phase voltage phasor is larger than $\sqrt{2}V_s/2$. Therefore, the DC link voltage of the proposed SSVC is expressed as:

$$V_{dc\_SSVC} = 2 \cdot \sqrt{2}V_s / 2 = \sqrt{2}V_s, \tag{3.21}$$

which is the same as the conventional H-bridge.

Based on the previous analysis, the switches' current and voltage stress of the SSVC system can be minimized by designing the AC capacitor and voltage and current reference properly. As a result, the *TDPR* of SSVC system is only 1.125 times of H-bridge circuit:

$$\begin{aligned} TDPR &= 4 \cdot V_{dc} \cdot \sqrt{2}I_s + 2 \cdot V_{dc} \cdot \sqrt{2}I_s / 4 \\ &= 9S = 1.125 TDPR_{H-bridge} \end{aligned}. \tag{3.22}$$

For the SSVC based on DC-capacitor-less inverter with SVPWM, a very small DC filtering capacitor is needed for switching ripple. The DC capacitor is 0.27 times of AC capacitor size. In the next chapter, a control method based on ripple power for AC capacitor reference is proposed and explained to achieve good steady state and dynamic performance with the small DC capacitor size.

In order to show the benefit of proposed method in SSVC application, the voltage and current stress of other existing methods are analyzed.

In Figure 10, the energy-storage capacitor, C_d is connected to DC link by a buck converter, and the capacitor voltage is unipolar. If the capacitor voltage reference is a full-wave rectified sinusoidal waveform as it shown in Figure 52, the 2ω ripple power can be transferred to the

capacitor.

For SSVC application, the energy-storage capacitor's voltage and current are expressed as

$$v_{Cd} = \sqrt{2}V_{Cd}\left|\sin(\omega t)\right|, \tag{3.23}$$

$$\begin{aligned} i_{Cd} &= \sqrt{2}I_{Cd}\cos(\omega t)\cdot \mathrm{sgn}(\sin(\omega t)) \\ &= \sqrt{2}\omega C_d V_{Cd}\cos(\omega t)\cdot \mathrm{sgn}(\sin(\omega t)) \end{aligned}. \tag{3.24}$$

Then the power stored in the energy-storage capacitor will be

$$p_{Cd} = V_{Cd} I_{Cd}\sin(2\omega t) = \omega C_d V_{Cd}^2 \sin(2\omega t). \tag{3.25}$$

As it shown in Figure 52, the power of C_d is controlled equal to the grid 2ω ripple power:

$$p_{Cd} = p_{2\omega}. \tag{3.26}$$

Then, the 2ω power to DC side can be fully eliminated.

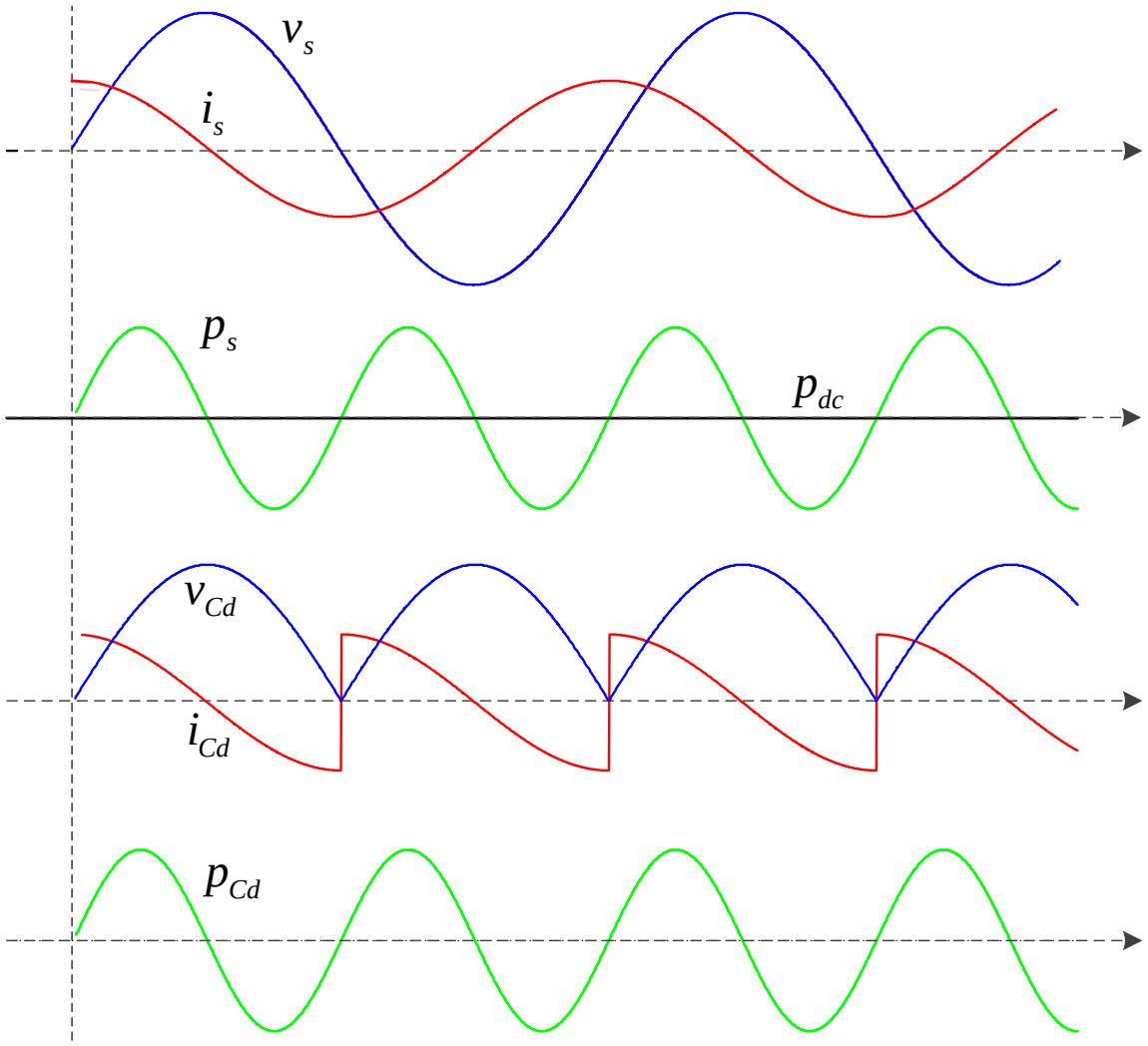


Figure 52: Single phase converter with unipolar energy-storage capacitor key waveforms for SSVC cases

By designing C_d to be:

$$C_d = \frac{I_s}{\omega V_s}, \tag{3.27}$$

the DC voltage can be fully utilized, and energy-storage capacitor's voltage and current magnitude will be:

$$V_{Cd} = V_s, \tag{3.28}$$

$$I_{Cd} = I_s . \tag{3.29}$$

In ideal case, the DC link voltage will be:

$$V_{dc} = \sqrt{2}V_s . \tag{3.30}$$

and the energy storage requirement is equal to the minimal value:

$$E_C = \frac{1}{2}C_d V_{dc}^2 = \frac{S}{\omega} = E_{C\_\min}, \tag{3.31}$$

and *TDPR* for SSVC application will be:

$$\begin{aligned} TDPR &= 4 \cdot V_{dc} \cdot \sqrt{2} I_s + 2 \cdot V_{dc} \cdot \sqrt{2} I_s \\ &= 12S = 1.5 TDPR_{H-bridge} \end{aligned} . \tag{3.32}$$

However, the full-wave rectified sinusoidal reference, which contains rich harmonics, is difficult for the control system to track. Although it is possible to decrease the harmonics in the reference by increasing the energy-storage margin (therefore the capacitor voltage does not go down to zero), this will compromise full utilization of the energy-storage capacitor. Therefore, in real application, E_C will be larger than the ideal case, E_{Cmin}. The minimal reported E_C is 1.5 $E_{C\_\min}$. In additional, the system requires DC capacitor with the same size of energy-storage capacitor, C_d.

In Figure 12, the system consists of an H-bridge and a half-bridge circuit for ripple power compensation. The sum of the power of C_1 and C_2 is controlled to be equal to the 2ω ripple power on grid side.

The two DC capacitors' voltage and current are express as:

$$v_{C1} = \frac{V_{dc}}{2} - \sqrt{2}V_C \sin(\omega t), \tag{3.33}$$

$$v_{C2} = \frac{V_{dc}}{2} + \sqrt{2}V_C \sin(\omega t), \tag{3.34}$$

$$\begin{aligned} i_{C1} &= -i_{C2} = -\sqrt{2} I_C \cos(\omega t) \\ &= -\sqrt{2}\omega C_f V_C \cos(\omega t) \end{aligned} . \tag{3.35}$$

Then, the sum of power of C_1 and C_2 will be

$$p_{C1,2} = v_{c1} i_{c1} + v_{c2} i_{c2} = 2\omega C_f V_C^2 \sin(2\omega t) . \tag{3.36}$$

By designing C_f to be:

$$C_1 = C_2 = C_f = \frac{I_s}{2\omega V_s} . \tag{3.37}$$

The DC capacitors' voltage and current magnitude will be:

$$V_C = V_s , \tag{3.38}$$

$$I_C = I_s / 2 . \tag{3.39}$$

Since the peak voltages of C_1 and C_2 are V_{dc}, the DC voltage will be

$$V_{dc} = 2\sqrt{2} V_s , \tag{3.40}$$

which is double of the DC voltage requirement of conventional H-bridge system. The peak currents of C_1 and C_2 is equal to $\sqrt{2} I_s / 2$. The currents of S_5 and S_6 are the subtraction of the currents of C_1 and C_2; and the peak currents of S_5 and S_6 are equal to AC output peak current.

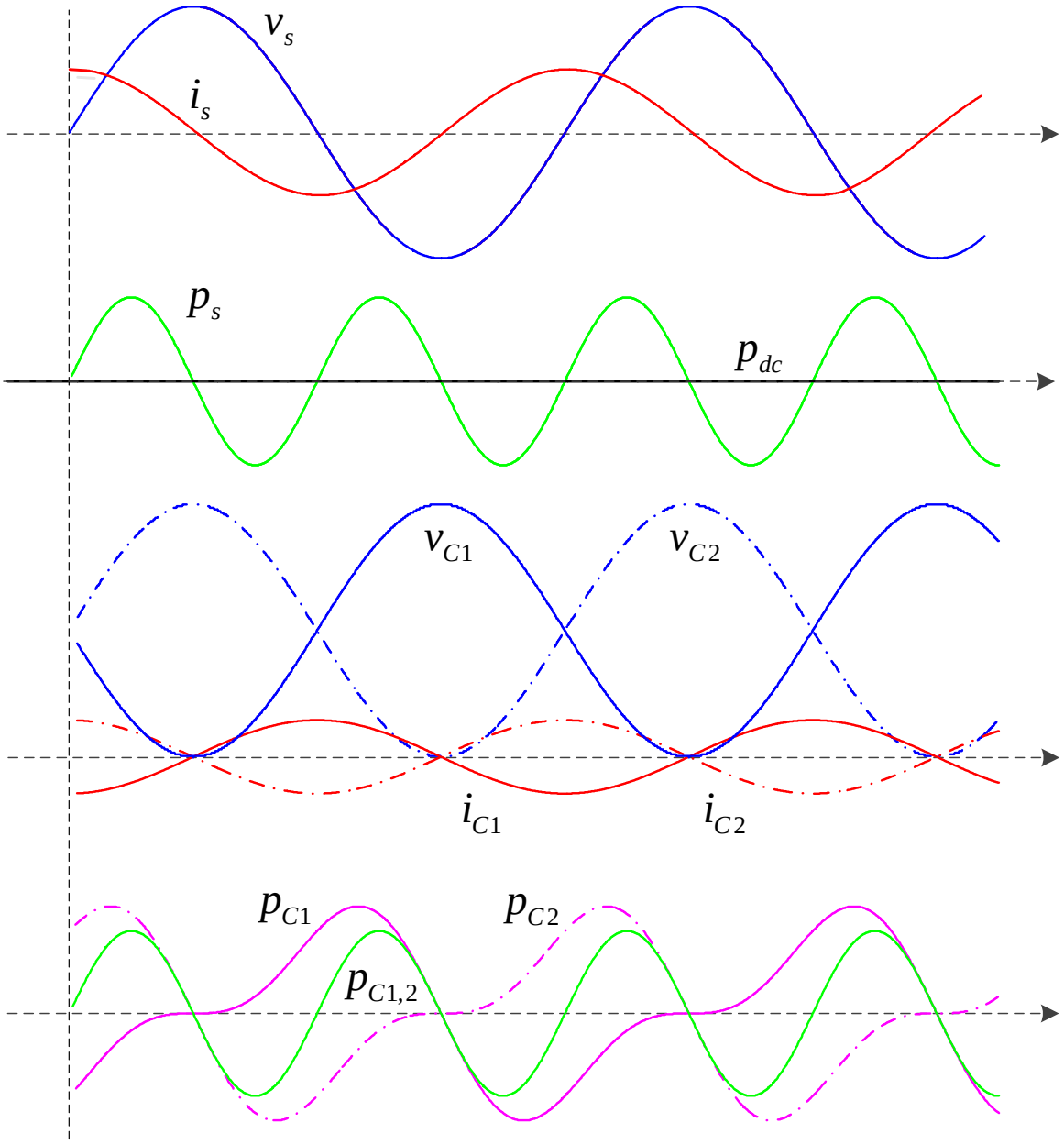


Figure 53: Single phase converter with half bridge for ripple compensation key waveforms for SSVC case

The energy storage requirement will be:

$$E_C = 2 \times \frac{1}{2} C_f V_{dc}^2 = \frac{4S}{\omega} = 4E_{C\_\min}, \tag{3.41}$$

and *TDPR* for SSVC application will be:

$$TDPR = 6 \cdot V_{dc} \cdot \sqrt{2} I_s = 6 \cdot 2\sqrt{2} V_s \cdot \sqrt{2} I_s = 24S = 3TDPR_{H-bridge}. \quad (3.42)$$

The advantage of this circuit is that C_1 and C_2 are also utilized as the DC filter capacitor. However, in order to keep the switches' current stress same as the H-bridge, the required DC voltage of the circuit is double of H-bridge's DC voltage. Therefore, *TDPR* is 3 times of $TDPR_{H\text{-}bridge}$. In addition, the voltages of C_1 and C_2 have a DC component of half DC link voltage to maintain a constants DC voltage, which is the sum of the voltage of C_1 and C_2. The individual power of C_1 and C_2 has another component with the line frequency, beside 2ω ripple power. Although the line frequency components of the power of C_1 and C_2 are cancelled out, the energy of C_1 and C_2 are not fully used for 2ω ripple power compensation and the energy storage requirement E_C is significantly increased, which is 4 times of E_{Cmin}.

In Figure 14, the circuit combines the half-bridge circuit for ripple power compensation with one leg of the H-bridge inverter in Figure 12. Therefore, the circuit has the minimum components among the existing topologies. And the energy storage requirement E_C remains the same, which is 4 times of E_{Cmin}.

Another advantage is that the current stress of the shared leg is only 1/4 of AC output current. Therefore, the *TDPR* is significantly reduced:

$$TDPR = 4 \cdot V_{dc} \cdot \sqrt{2} I_s + 4 \cdot V_{dc} \cdot \sqrt{2} I_s / 4 = 10S = 1.25TDPR_{H-bridge}. \quad (3.43)$$

A SSVC system can also be implemented by the circuit with the power decoupling ripple-port shown in Figure 16. By adding any extra H-bridge to interface the energy-storage capacitor, the capacitor works in AC mode and the voltage/current waveforms are sinusoidal.

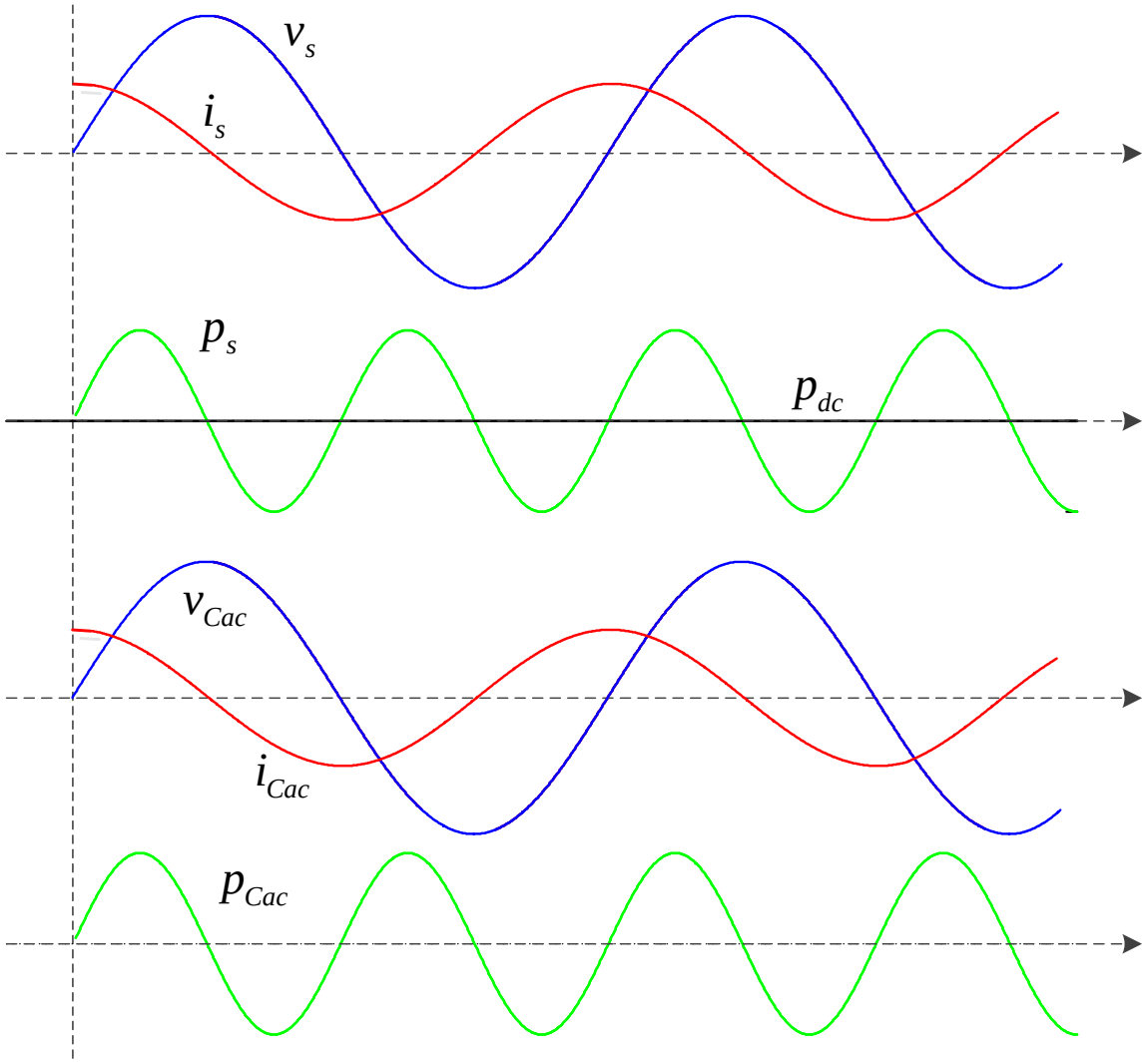


Figure 54: Single phase converter with minimal component for ripple compensation key waveforms for SSVC cases.

The capacitor's voltage and current are expressed as

$$v_{Cac} = \sqrt{2}V_{Cac}\sin(\omega t), \tag{3.44}$$

$$i_{Cac} = \sqrt{2}I_{Cac}\cos(\omega t) = \sqrt{2}\omega C_{ac}V_{Cac}\cos(\omega t). \tag{3.45}$$

Then the power of the AC capacitor will be

$$p_{Cac} = V_{Cac} I_{Cac} \sin(2\omega t) = \omega C_{ac} V_{Cac}^2 \sin(2\omega t). \tag{3.46}$$

By designing C_{ac} to be:

$$C_{ac} = \frac{I_s}{\omega V_s}, \tag{3.47}$$

the DC voltage can be fully utilized, and AC capacitor voltage/current magnitude will be:

$$V_{Cac} = V_s, \tag{3.48}$$

$$I_{Cac} = I_s. \tag{3.49}$$

In ideal case, the DC voltage will be:

$$V_{dc} = \sqrt{2} V_s, \tag{3.50}$$

and the energy storage requirement is:

$$E_C = \frac{1}{2} C_{ac} (\sqrt{2} V_{Cac})^2 = C_{ac} V_{ac}^2 = \frac{S}{\omega} = E_{C\_\min}, \tag{3.51}$$

and *TDPR* for SSVC application will be:

$$\begin{aligned} TDPR &= 4 \cdot V_{dc} \cdot \sqrt{2} I_s + 4 \cdot V_{dc} \cdot \sqrt{2} I_s \\ &= 16S = 2TDPR_{H-bridge} \end{aligned}. \tag{3.52}$$

The SSVC system based on circuit in Figure 16 also needs a DC filtering capacitor with 0.6 times of AC capacitor. However, [41] has not demonstrated the performance of the control system with dynamic response to sudden load change.

The E_C and *TDPR* of each method for SSVC application are summarized in Table 3.

Table 3: Comparison of E_C and *TDPR* of different topologies for SSVC applications.

Methods to reduce DC capacitor of H-bridge for SSVC application	***Ec***	***DC capacitor***	***TDPR***
circuit in Figure 10	1.5 Ec_{min}	Same size as energy storage capacitor	1.5 $TDPR_{H\text{-}bridge}$
circuit in Figure 12	4 Ec_{min}	Not required	3 $TDPR_{H\text{-}bridge}$
circuit in Figure 14	4 Ec_{min}	Not required	1.25 $TDPR_{H\text{-}bridge}$
circuit in Figure 16	Ec_{min}	0.6 times of energy storage capacitor (no dynamic test)	2 $TDPR_{H\text{-}bridge}$
DC-capacitor-less inverter with SVPWM	Ec_{min}	0.27 times of energy storage capacitor	1.125 $TDPR_{H\text{-}bridge}$

Among the five methods, the SSVC based on DC-capacitor-less inverter has the minimal E_C and *TDPR*, in other words, minimal size of energy storage capacitor and cost of semiconductor devices. Compared to the topologies in Figure 16 with the same minimal E_C, the *TDPR* of SSVC with DC-capacitor-less is 44% smaller. Compared to the topologies in Figure 14 with 1.25 times *TDPR* of H-bridge circuit (the second smallest), the E_C of SSVC based on DC-capacitor-less inverter is 75% smaller.

4.4 DC capacitor optimization

Figure 55 shows the PWM switching details during one switching cycle. S_a, S_b, S_c are the switching functions of three phases determined by SVPWM strategy; i_{Cdc} is the ideal inverter DC capacitor current.

Based on three phases' reference, and the SVPWM operation of SSVC, the duty cycle for each phase leg, D_a, D_b, D_c can be calculated:

$$D_a = \frac{1}{2} + \frac{\sqrt{2}V_s}{2V_{dc}}\sin(\omega t), \tag{3.53}$$

$$D_b = \frac{1}{2} - \frac{\sqrt{2}V_s}{2V_{dc}}\sin(\omega t), \tag{3.54}$$

$$D_c = \frac{1}{2} + (2\sqrt{\frac{I_{s\_ref}}{I_s}} - 1)\frac{\sqrt{2}V_s}{2V_{dc}}\sin(\omega t). \tag{3.55}$$

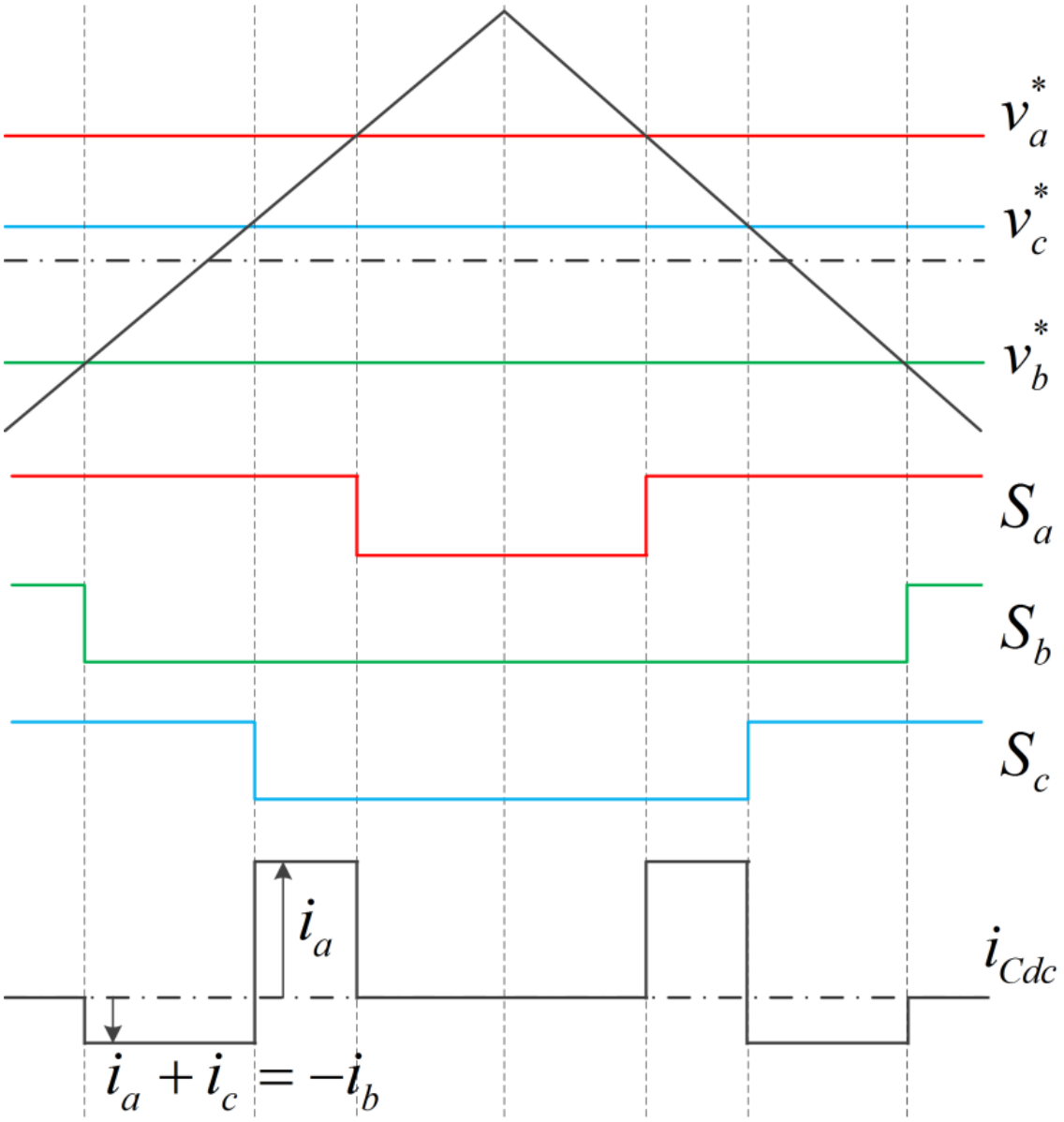


Figure 55: PWM switching details during one switching cycle.

By integrating the current of DC capacitor $i_{Cdc,}$ the voltage ripple on DC capacitor can be calculated:

$$\Delta V_{dc} = \frac{\int i_a \cdot (S_a - S_c)}{C_{dc}} = \frac{i_a (D_a - D_c) T_{sw}}{C_{dc}} = \frac{1}{C_{dc}} \sqrt{2} I_s^* \cos(\omega t) \cdot (2 - 2\sqrt{\frac{I_{s\_ref}}{I_s}}) \frac{\sqrt{2} V_s}{2 V_{dc}} \sin(\omega t) T_{sw} \quad (3.56)$$

When $\omega t = \pm \frac{\pi}{4} + k\pi$, the voltage ripple will reach maximum:

$$\Delta V_{dc\_\max} = \frac{I_{s\_ref}}{I_s} \cdot (1 - \sqrt{\frac{I_{s\_ref}}{I_s}}) \frac{V_s I_s}{C_{dc} V_{dc}} T_{sw}. \quad (3.57)$$

Based on (4.19), for rated grid current, the grid current and the AC capacitor current will be fully canceled theoretically without considering the effect of filtering inductor. Therefore, the current to DC capacitor is zero, and the voltage ripple is zero.

When $\sqrt{\frac{I_{s\_ref}}{I_s}} = 0.44$, the voltage ripple reaches maximum, the minimum DC capacitor to filter switching ripple can be designed by:

$$C_{dc\_\min} = \frac{0.15 V_s I_s}{\Delta V_{dc\_\max} V_{dc}} T_{sw}. \quad (3.58)$$

4.5 Experimental results

To verify the effectiveness of the developed SSVC, a 1.5-kVA SSVC is designed. The key parameters are listed below in Table 4.

For conventional H-bridge system, if the allowed DC voltage ripple is within 2.5%, the DC capacitance is 4.6 mF (15.5 pu). For the SSVC system, since the 2ω ripple power can be absorbed by the AC capacitor, theoretically the DC capacitor only needs to absorb switching current ripple,

of which the capacitance is 50 μF [69-72]. In real system design, a film capacitor with 85-μF capacitance (0.27 pu) is used for DC filtering capacitor. The AC capacitor is designed to be 300 μF (1 pu). Since the capacitor voltage rating of developed SSVC and conventional H-bridge system is the same, the total capacitor size is directly proportional to the capacitance value of the required capacitor if the same type of capacitors is used. Compared to conventional H-bridge system, the SSVC system reduces the total size of the capacitor including DC capacitor and AC capacitor by 13 times.

Table 4: Key parameters for SSVC.

DC-link voltage, V_{dc}	200 V
switching frequency, f_{sw}	10.8 kHz
DC capacitance, C_{dc}	85 μF (0.27 pu)
grid voltage, V_s	120 VAC (60 Hz)
AC capacitance, C_{ac}	300 μF (1 pu)
filter inductance, L_f	0.4 mH (0.015 pu)

For the filter inductance L_f, trade-off design is necessary. With a smaller L_f, the size of passive component can be reduced. On the other hand, with a smaller L_f, the current switching ripple is larger, which may cause higher power losses. Here, L_f is designed to be 0.4 mH (0.015 pu), to make the current ripple within 20%.

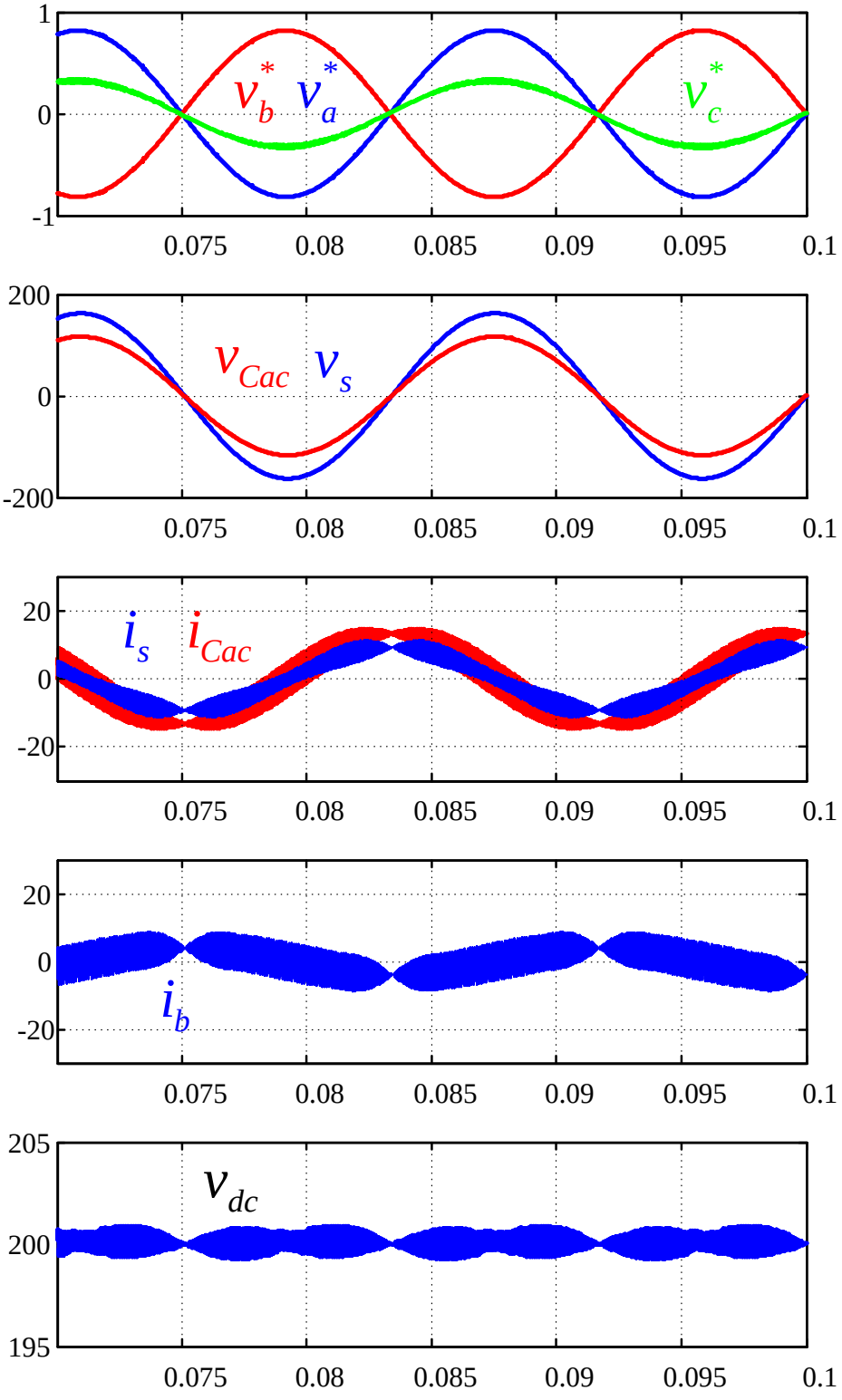


Figure 56: Simulation results half rated grid current.

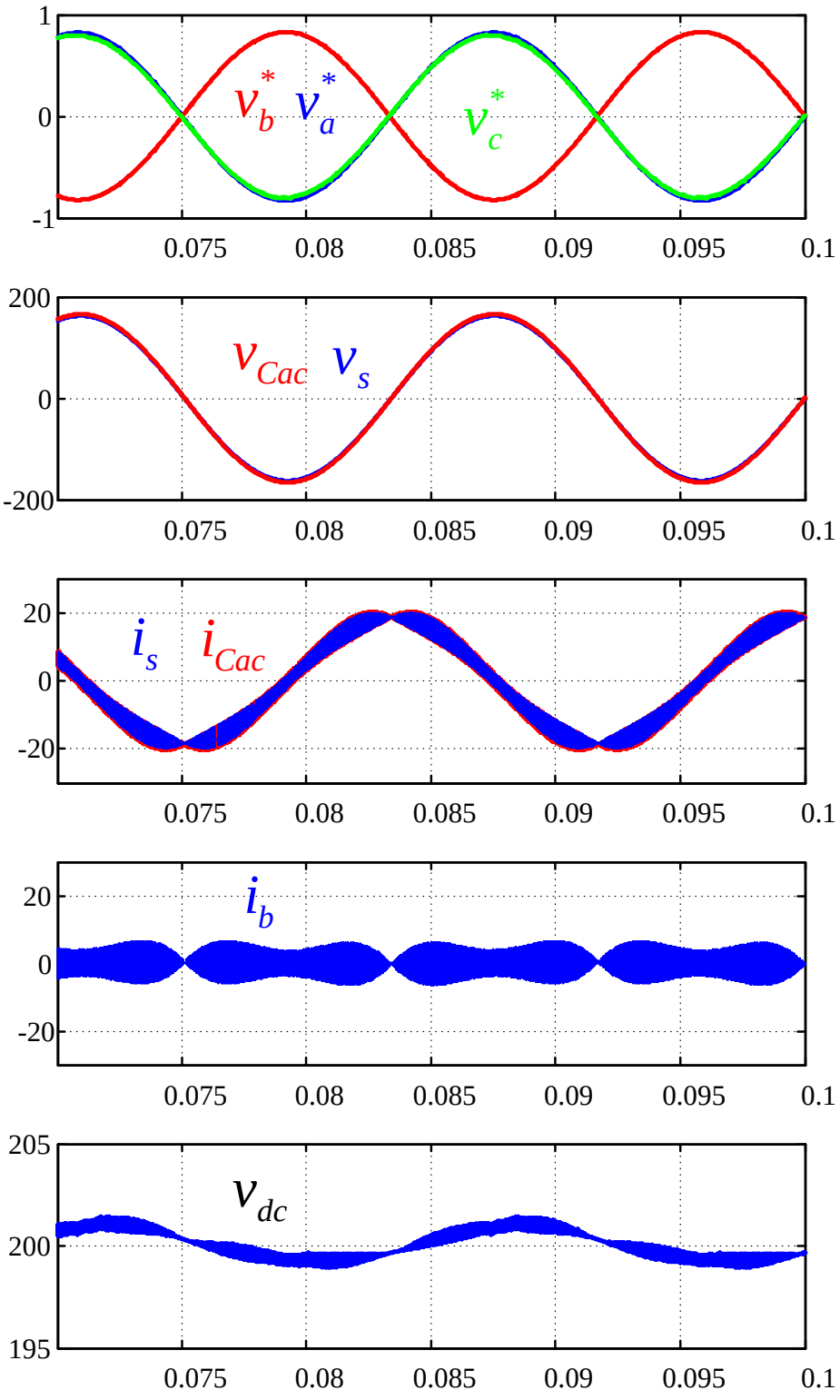


Figure 57: Simulation results full rated grid current.

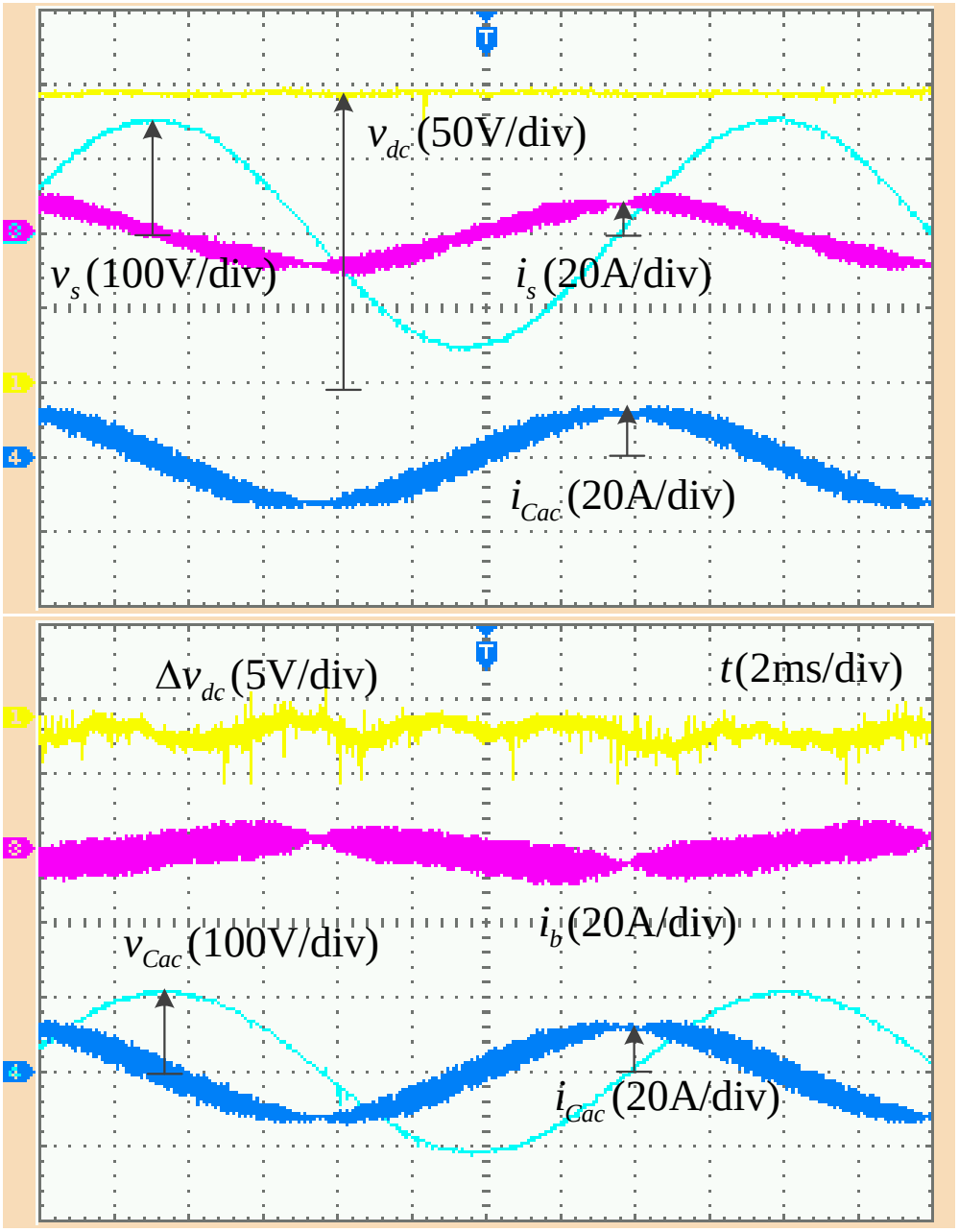


Figure 58: Steady state experimental waveforms half rated grid current.

Figure 56 and Figure 57 show the simulation results of the SSVC with full rated power and half rated power. m_a, m_b, and m_c are modulation signals for controlled voltage sources v_a, v_b, and v_c. The ripple power to the DC capacitor is completely eliminated, thus the DC capacitor voltage only has switching ripple. The average value of v_{dc} is 200 V and the ripple voltage is within 5 V (2.5%).

The relationship between v_s, v_{Cac}, i_s, and i_{Cac} is consistent with the theoretical analysis.

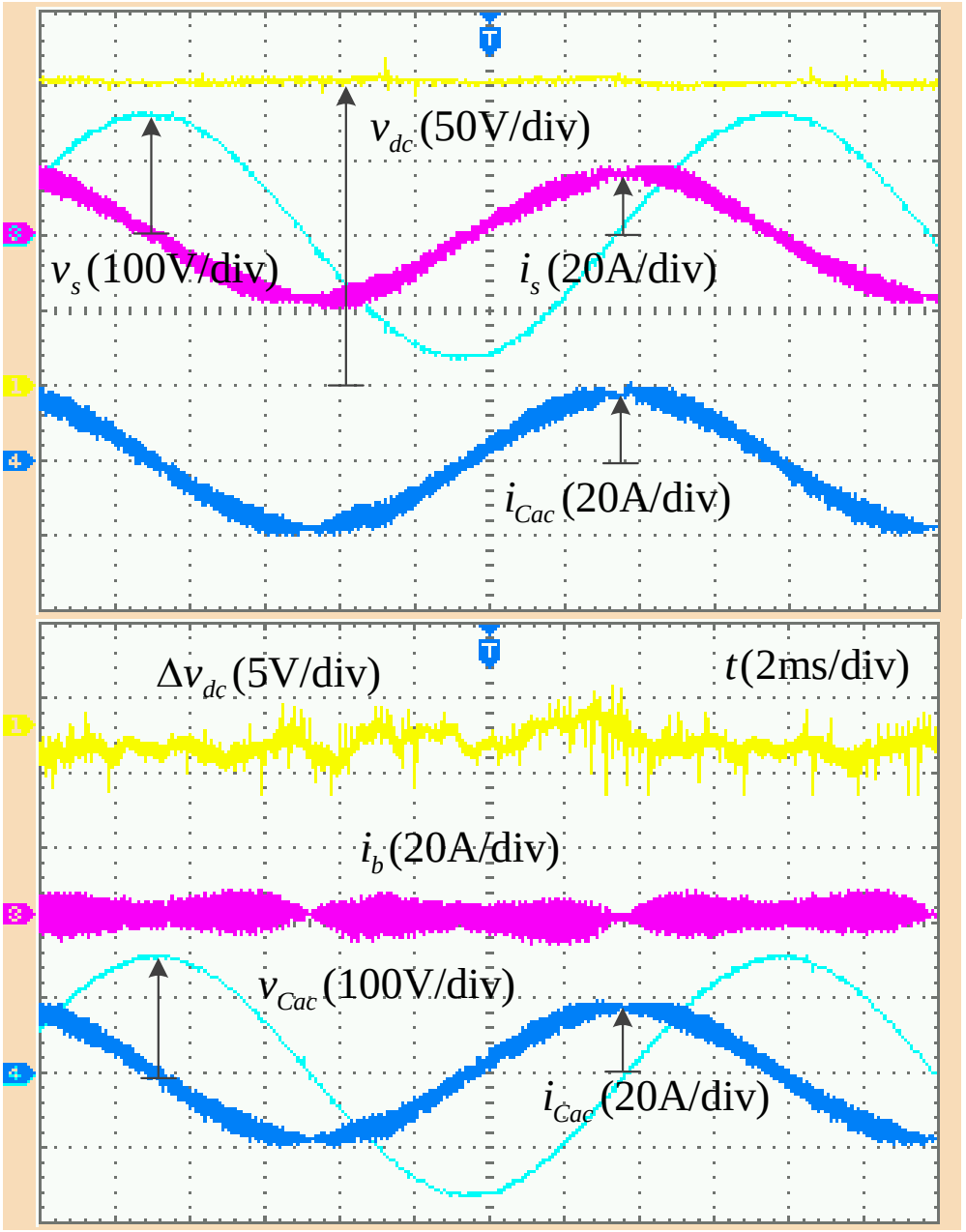


Figure 59: Steady state experimental waveforms full rated grid current.

A 1.5-kVA SSVC prototype has been built. Figure 58 and Figure 59 show the experimental key waveforms of the SSVC with half and full rated power. The average DC voltage is 200 V and

the DC voltage ripple is within 5 V (2.5%).

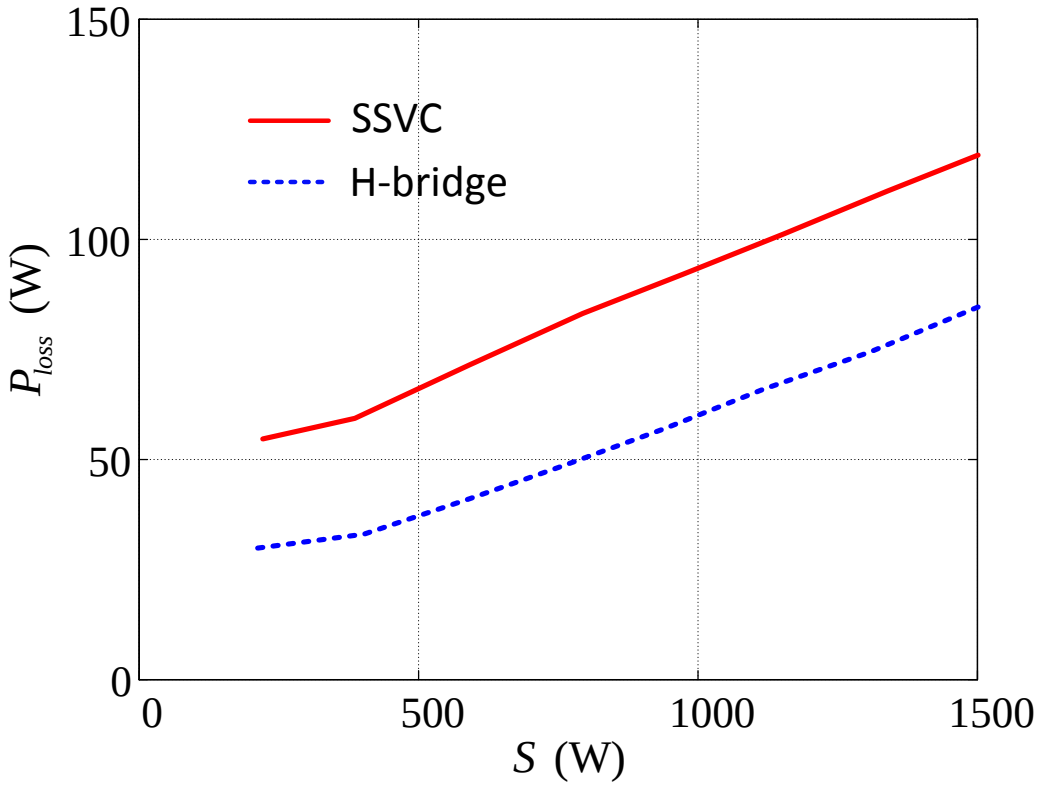


Figure 60: Power loss comparison between SSVC and conventional H-bridge.

Figure 60 and Figure 61 show the loss and efficiency comparison of SSVC and conventional H-bridge. Since the system is designed for reactive power compensation, the efficiency of the system is defined as:

$$\eta = 1 - \frac{P_{loss}}{S}, \tag{3.59}$$

where, P_{loss} is the active power consumed by the system and S is the apparent power of the system.

As it shown in Figure 60, compared to H-bridge, the additional power loss of the SSVC is

not significantly increased with higher grid power. Since the shared leg's current magnitude is decreasing with higher grid power, p_s, when p_s is large than 1/4 of the rated power as it shown in Figure 50, the power loss on shared leg is also decreased. Therefore, the total power loss caused by the added phase leg and AC capacitor is relatively low with higher grid power.

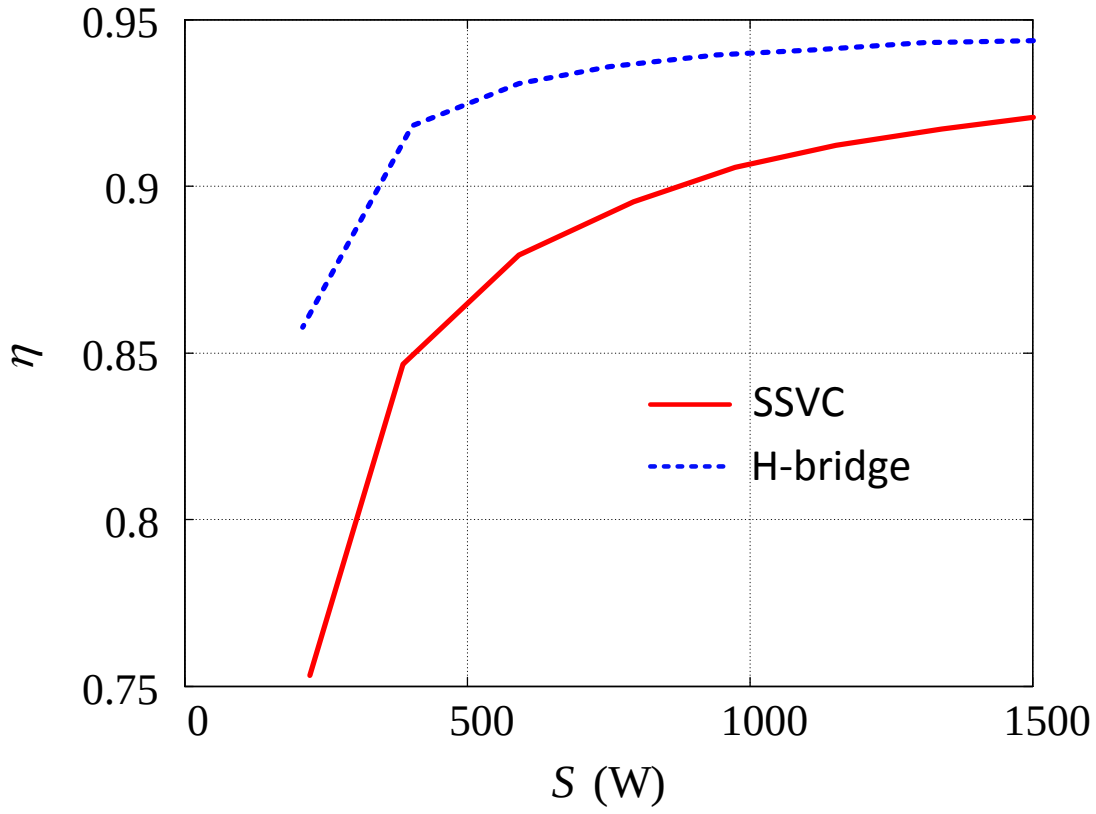


Figure 61: Efficiency comparison between SSVC and conventional H-bridge.

4.6 Conclusions

A solid state variable capacitor with minimum capacitor is developed. By adding an additional phase leg connected to an AC capacitor, the 2ω ripple power to the DC-link is completely

eliminated and the total capacitor size has been reduced by is 13 times compared to the conventional H-bridge system with 2.5% DC voltage ripple.

The SSVC system shows special benefits in terms of switches' current and voltage stress and efficiency compared to other applications. The current stress on the shared the leg is only one fourth of the conventional H-bridge inverter. In addition, the analysis of DC capacitor current shows that the current ripple of grid current and AC capacitor can be partially cancelled, which can reduce the DC filtering capacitor size.

The simulation and experiment have verified the theoretical analysis the effectiveness of the SSVC with minimum capacitor.

CHAPTER 5 IMPROVED CONTROL SYSTEM FOR SSVC

Since the solid state variable capacitor system only has a very small DC capacitor to maintain the DC voltage, the uncompensated ripple to DC side will cause very large voltage ripple on DC capacitor and may cause instability of the system.

Figure 62 shows the DC connections for different single phase power conversion applications. For SSVC application, any ripple power which has not been compensated by AC capacitor will go into DC capacitor, since the DC capacitor is connected to neither DC source (inverter case) nor load (rectifier case). Therefore, compared to other applications, the control system for SSVC is the more challenging.

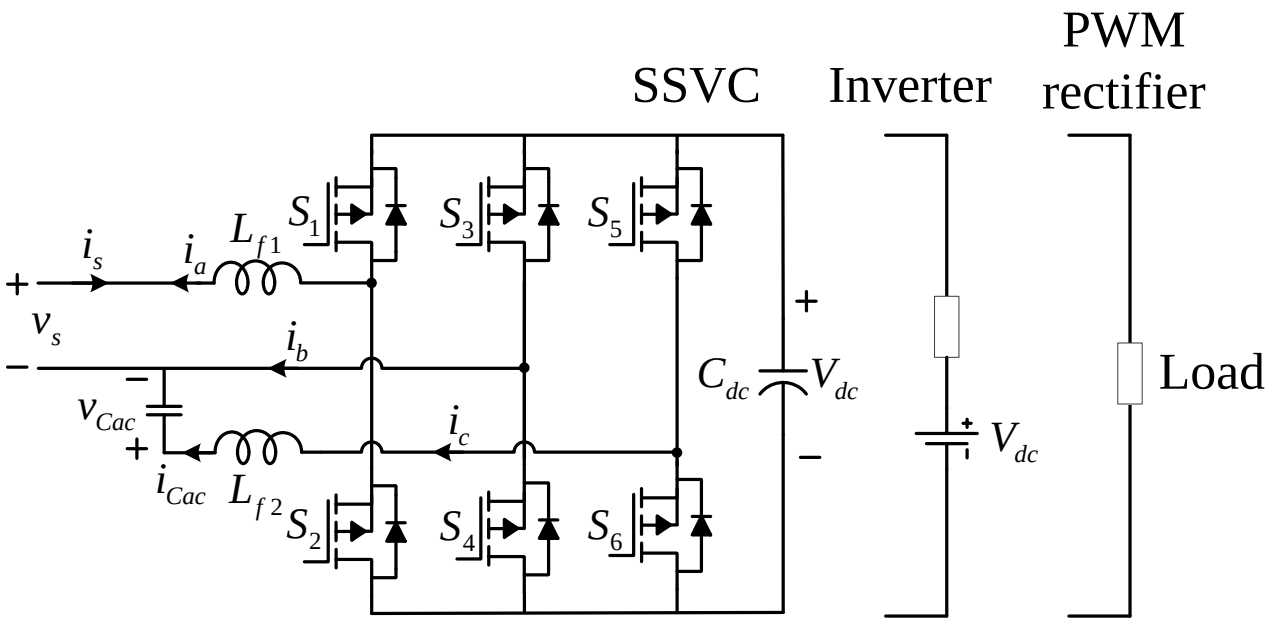


Figure 62: DC side connections for different applications

The existing control method [46] requires a large DC capacitor with same value of AC

capacitor in order to maintain the stability of the system. In Chapter 3, the control system calculates AC capacitor's voltage and current reference based on grid voltage and current phasors' magnitude and phase angle, can greatly reduce DC capacitor size, and achieve good steady state performance. However, the control system requires complicated mathematic calculation, which puts a lot burden on DSP controller with higher sampling frequency application (20-kHz) and is hard to achieve good dynamic response during transient of step load change.

In order to reduce the DC capacitor to minimal value just for filtering switching ripple (less than 1/3 of AC capacitor), a novel control system directly based on ripple power is proposed to maintain stable DC voltage and to achieve fast dynamic response.

The proposed control system calculates AC capacitor voltage and current reference directly based on grid side ripple power and DC capacitor ripple power, without complicated calculation. The feedforward part of the AC capacitor power is calculated by grid ripple power, which is updated with the sampling frequency (20-kHz) to achieve fast dynamic response and maintain table DC voltage during sudden load change transition. The feedback part of the AC capacitor power is calculated based on DC capacitor ripple power. By using discrete Fourier transform (DFT), the DC capacitor ripple power can be calculated based on the DC voltage ripple. Since the feedforward updated with very fast sampling frequency can compensate most the ripple power during transient of step load change. The feedback part don't need wide bandwidth and only need to be updated with twice line frequency (120-Hz), just for achieving better steady-state ripple power compensation performance.

By adopting the proposed the control method, the DC capacitor of SSVC is reduced to minimal value only for filtering high frequency switching ripple current (0.27 pu). The proposed control system can also be easily extended for other single phase applications. In addition, the

control system can be modified to compensate not only 2ω ripple power, but also other even order frequency ripple power caused by the harmonics of grid voltage.

5.1 C_{ac} voltage and current reference based on AC capacitor power

First, the AC capacitor reference based on AC capacitor power reference is analyzed. In order to compensate the ripple power for grid side, the power reference of C_{ac}, p_{Cac} should be controlled equal to the ripple power, p_{ripple}. And the energy of C_{ac}, E_{Cac} should be

$$E_{cac} = \frac{1}{2} C_{ac} v_{Cac}^2 = \int p_{Cac} = \int p_{ripple} = \int v_s i_s \,. \tag{4.1}$$

Ideally, the ripple power is equal to grid side power, p_s and can be directly calculated based on v_s and i_s.

The voltage of C_{ac} should satisfy:

$$| v_{Cac} | = \sqrt{\frac{2}{C_{ac}} \int p_{Cac}} \,. \tag{4.2}$$

By changing the polarity of the voltage reference properly, C_{ac} can work in AC mode.

The current reference of C_{ac} is

$$i_{Cac} = C_{ac} \frac{dv_{Cac}}{dt} \,. \tag{4.3}$$

The AC capacitor voltage and current reference is accurate and simple to calculate directly based on power reference. Figure 63 shows the relationship of grid voltage/current, AC capacitor power, energy, and voltage reference.

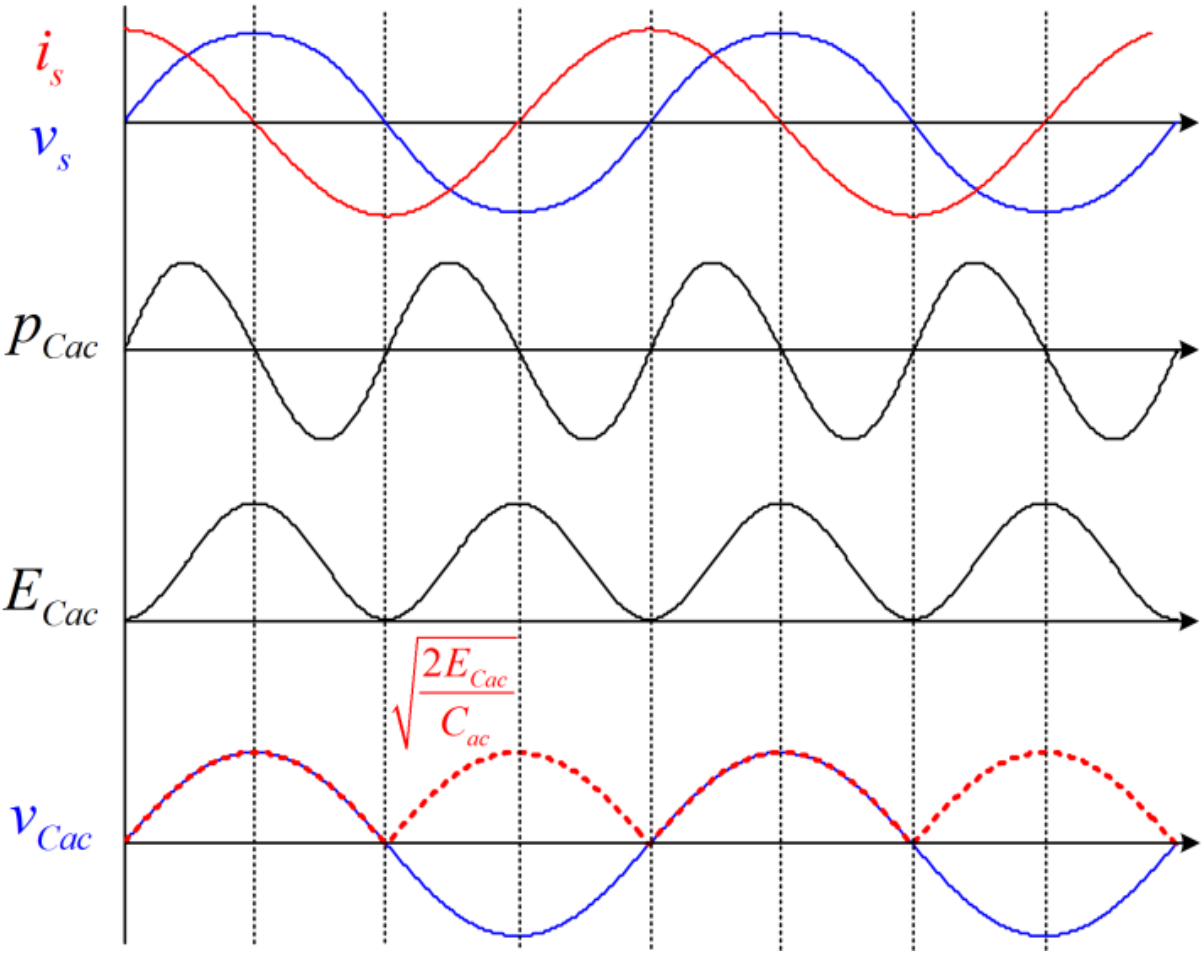


Figure 63: Relationship between C_{ac} voltage and ripple power.

5.2 Control Strategy

Figure 64 shows the control system, which consists of grid side current control, DC voltage control, AC capacitor voltage and current control, and feedforward and feedback compensation for the AC capacitor power reference.

The DC voltage controller is to maintain the DC-link voltage V_{dc} by controlling the phase angle of grid current, φ. The grid side current controller is to regulate the reactive power by controlling the magnitude of grid current, I_{s_ref}. A proportional-resonant (PR) controller is used for

the capacitor voltage/current control.

The reference voltages for phase A, B and C generated by SVPWM control can be expressed as:

$$v_a^* = -v_b^* = \frac{1}{2} v_{ab}^*, \tag{4.4}$$

$$v_c^* = v_b^* + v_{cb}^*. \tag{4.5}$$

where v_{cb}^* is the reference to control grid side current; and v_{cb}^* is the reference to control the AC capacitor. Then the reference for phase C is derived in (25).

The feed-forward part of the AC capacitor power reference is directly calculated based on grid voltage and current reference. The grid power reference, p_{grid} is express as:

$$p_{grid} = v_{ab}^* \cdot i_s^*. \tag{4.6}$$

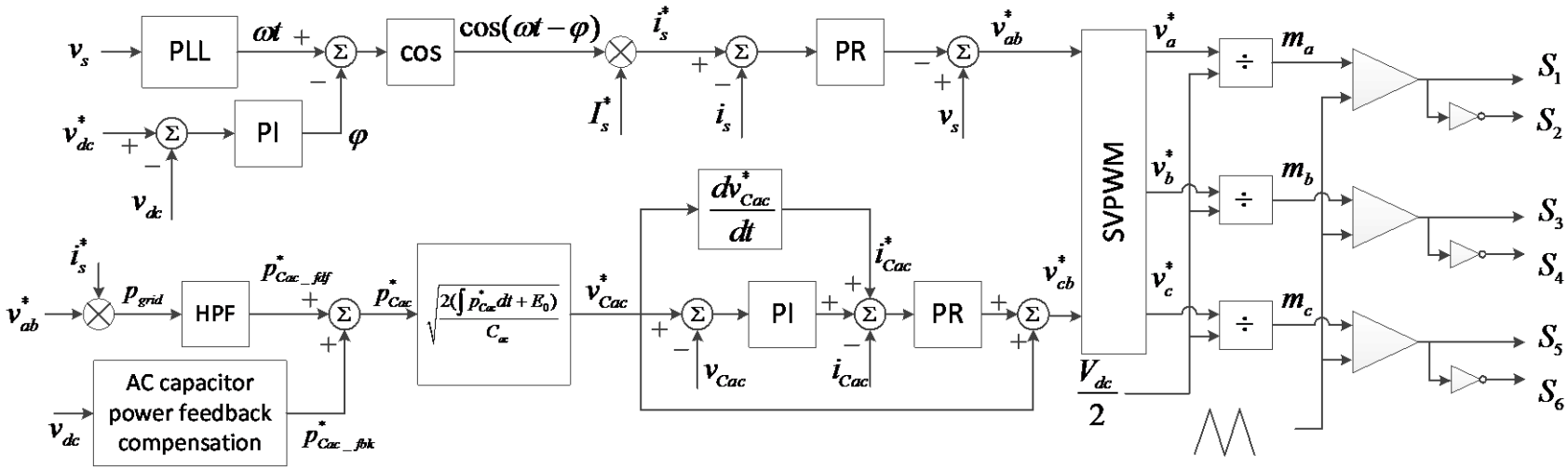


Figure 64: Control system for SSVC.

The grid power reference, p_{grid} has DC component, which is the power loss of the system, and 2ω ripple AC component, which is the ripple power needed to be compensated by AC capacitor. By using a high pass filter (HPF), the 2ω ripple power for AC capacitor power reference, $p^*_{Cac\_fdf}$ can be obtained based on p_{grid}.

The feedback part of AC capacitor power reference, $p^*_{Cac\_fdk}$ is calculated based on DC ripple power and is described in details in the following section.

5.3 Closed-loop compensation for ripple power

Considering parameter deviation in practical applications and steady-state error in the capacitor voltage and current control, it is difficult to eliminate ripple power to the DC capacitor only by feed-forward control. Therefore, the relationship between power mismatch and DC-link ripple voltage needs to be investigated in order to design the closed-loop ripple power compensation.

Assuming that the DC-link voltage is:

$$v_{dc} = V_{dc} + \Delta V_{\sin}\sin(2\omega t) + \Delta V_{\cos}\cos(2\omega t), \tag{4.7}$$

the ripple power to the DC capacitor is expressed as:

$$\begin{aligned} p_{dc\_r} &= p_{dc\_r\_\cos}\cos(2\omega t) + p_{dc\_r\_\sin}\sin(2\omega t) = C_{dc}\frac{dv_{dc}}{dt}v_{dc} \\ &= C_{dc}V_{dc}\left(\frac{d\Delta V_{\sin}}{dt}\sin(2\omega t) + \frac{d\Delta V_{\cos}}{dt}\cos(2\omega t) + 2\omega\Delta V_{\sin}\cos(2\omega t) - 2\omega\Delta V_{\cos}\sin(2\omega t)\right) \end{aligned}. \tag{4.8}$$

The relationship between magnitude of ripple power and magnitude of ripple voltage on DC capacitor satisfies:

$$p_{dc\_r\_\sin} = C_{dc}V_{dc} \cdot (-2\omega \cdot \Delta V_{\cos} + \frac{d\Delta V_{\sin}}{dt}), \tag{4.9}$$

$$p_{dc\_r\_\cos} = C_{dc}V_{dc} \cdot (2\omega \cdot \Delta V_{\sin} + \frac{d\Delta V_{\cos}}{dt}). \tag{4.10}$$

The ripple power to the DC capacitor is the mismatched power between grid side ripple power and AC capacitor power. Based on the mismatched power, the AC capacitor's voltage reference can be compensated to fully absorb ripple power.

Figure 65 shows the closed-loop ripple power compensation for AC capacitor voltage reference. Discrete Fourier transform (DFT) is used to calculate $\Delta V_{\sin}$, $\Delta V_{\cos}$ from the DC ripple voltage. PI controllers then regulate ripple voltage components toward zero by changing the power compensation terms $p^*_{\cos}, p^*_{\sin}$. According to the relationship between power mismatch and DC voltage ripple, the compensated AC capacitor power should be

$$p^*_{Cac\_fdk} = -p^*_{\sin}\sin(2\omega t) + p^*_{\cos}\cos(2\omega t), \tag{4.11}$$

Since the AC capacitor voltage reference is obtained based on sinusoidal reference, the capacitor current reference can be directly calculated by derivation of the capacitor voltage reference without introducing noise.

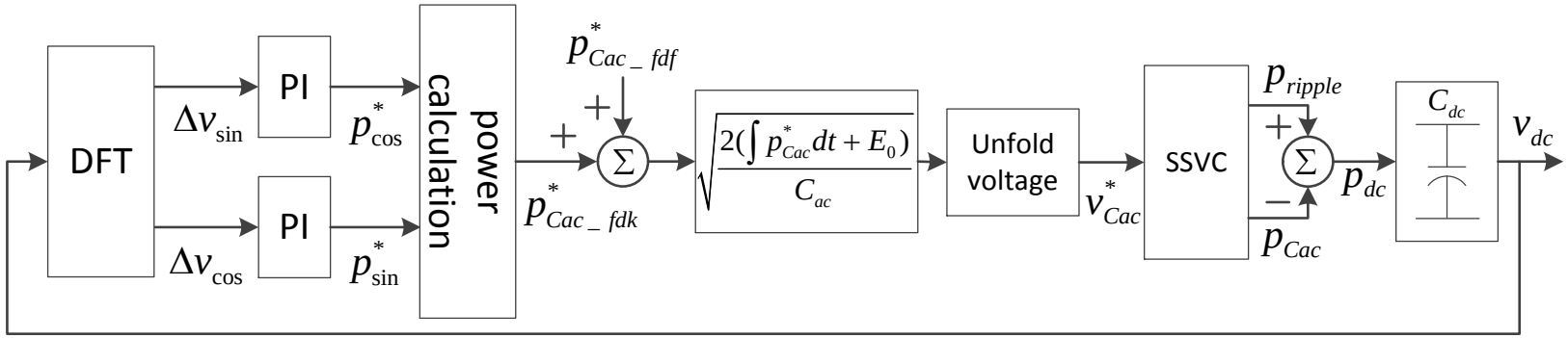


Figure 65: Closed-loop compensation for AC capacitor voltage reference.

In order to design the PI controller for ripple power feedback, the transfer functions from magnitude of ripple power to magnitude of ripple voltage on DC capacitor is derived:

$$\begin{pmatrix} \Delta V_{\sin}(s) \\ \Delta V_{\cos}(s) \end{pmatrix} = -\begin{bmatrix} A_{11}(s) & A_{12}(s) \\ A_{21}(s) & A_{22}(s) \end{bmatrix} \begin{pmatrix} p_{\sin\_Cac}(s) \\ p_{\cos\_Cac}(s) \end{pmatrix}$$
$$= -\begin{bmatrix} \frac{s}{C_{dc}V_{dc}s^2 + (2\omega)^2 C_{dc}V_{dc}} & \frac{2\omega}{C_{dc}V_{dc}s^2 + (2\omega)^2 C_{dc}V_{dc}} \\ \frac{-2\omega}{C_{dc}V_{dc}s^2 + (2\omega)^2 C_{dc}V_{dc}} & \frac{s}{C_{dc}V_{dc}s^2 + (2\omega)^2 C_{dc}V_{dc}} \end{bmatrix} \begin{pmatrix} p_{\sin\_Cac}(s) \\ p_{\cos\_Cac}(s) \end{pmatrix}, \quad (4.12)$$

Based on the expression of transfer functions, we can get:

$$A_{11}(s) = A_{22}(s), \quad (4.13)$$

$$A_{12}(s) = -A_{21}(s), \quad (4.14)$$

and the bode plot of $A_{11}(s)$ and $A_{12}(s)$ are shown in Figure 66 and Figure 67 respectively.

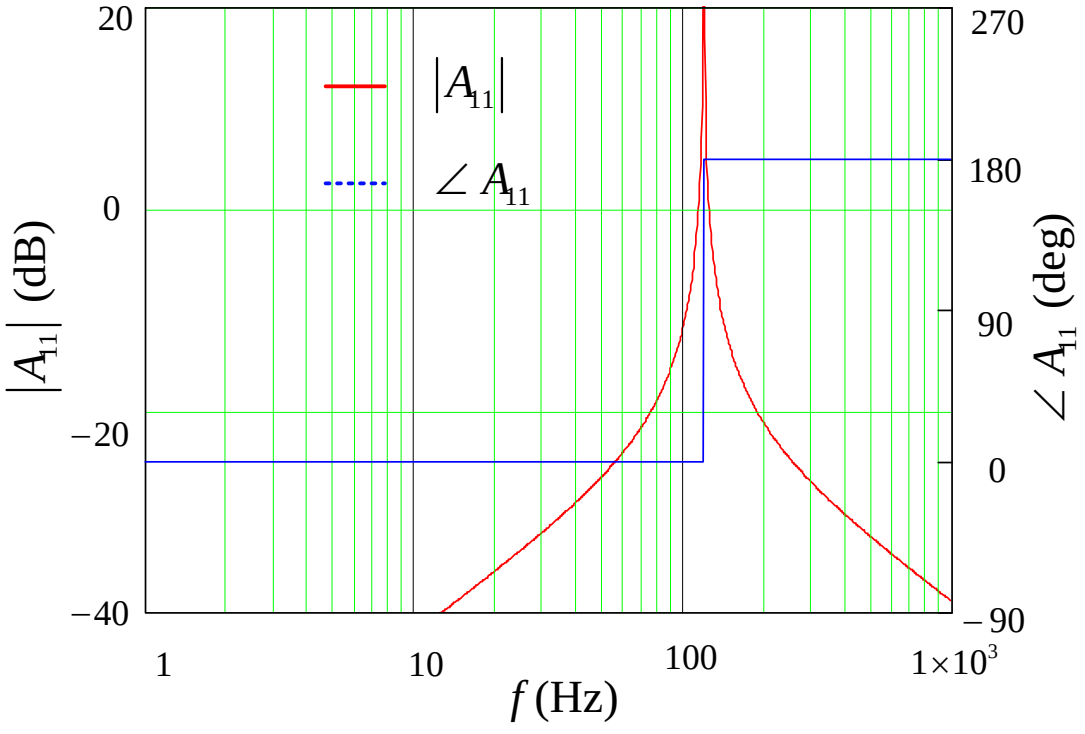


Figure 66: Bode plot of $A_{11}(s)$.

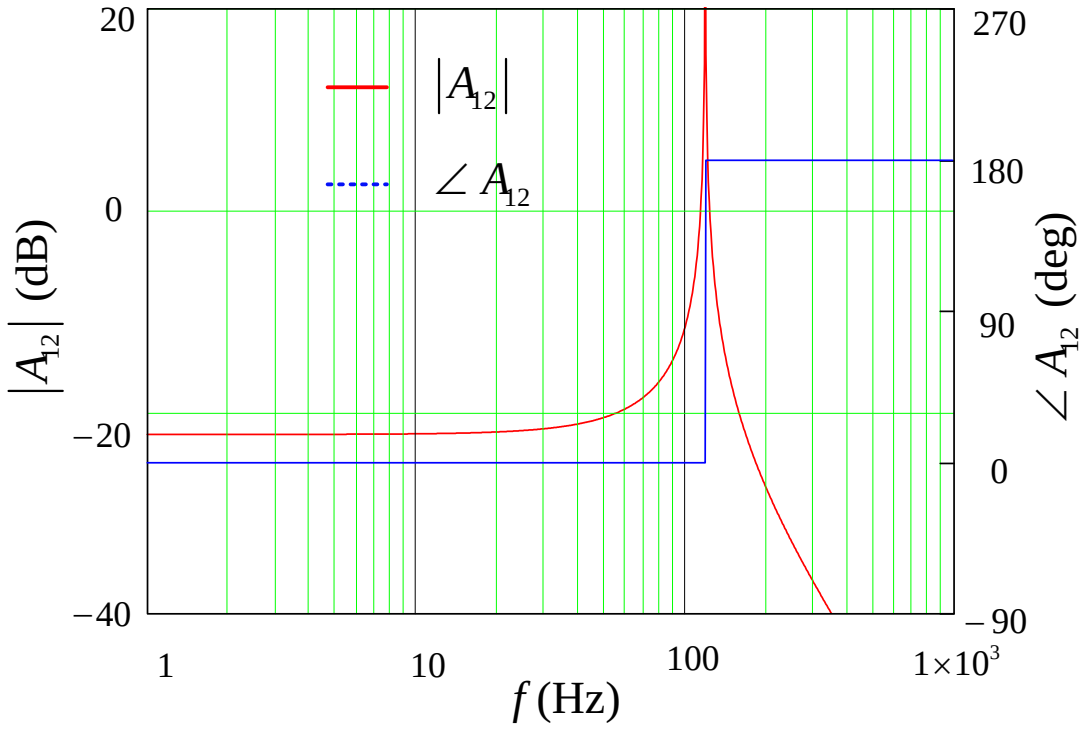


Figure 67: Bode plot of $A_{12}(s)$.

Since feedback part only need 10-Hz bandwidth for steady state compensation, the magnitude of $A_{11}(s)$ is much lower than $A_{12}(s)$ within 10 Hz frequency, and the resonant peak is far away from 10 Hz. Therefore, the system can be simplified to a decoupled system with constant gain within 10-Hz bandwidth:

$$\begin{pmatrix} \Delta V_{\sin}(s) \\ \Delta V_{\cos}(s) \end{pmatrix} \approx \begin{bmatrix} 0 & -\dfrac{1}{2\omega C_{dc} V_{dc}} \\ \dfrac{1}{2\omega C_{dc} V_{dc}} & 0 \end{bmatrix} \begin{pmatrix} p_{\sin\_Cac}(s) \\ p_{\cos\_Cac}(s) \end{pmatrix}. \tag{4.15}$$

In other words, $\dfrac{d\Delta V_{\cos}}{dt}$ and $\dfrac{d\Delta V_{\sin}}{dt}$ part in (5.9) and (5.10) can be neglected; and the PI controller just need to compensate enough magnitude gain for the closed-loop system.

The proposed control system can also be easily extended for other applications including inverter and PWM rectifier. Since the DC side connections are different for other applications, the feedback part design need to be slightly modified. Taking PWM rectifier case as an example, the DC side is connected to DC capacitor and DC resistance load, R_{dc}. The power to the DC side is expressed as:

$$\begin{aligned} p_{dc} &= C_{dc}\frac{dv_{dc}}{dt}v_{dc} + \frac{v_{dc}^2}{R_{dc}} \\ &= C_{dc}V_{dc}\left(\frac{d\Delta V_{\sin}}{dt}\sin(2\omega t) + \frac{d\Delta V_{\cos}}{dt}\cos(2\omega t)\right) \\ &+ C_{dc}V_{dc}\left(2\omega\cdot\Delta V_{\sin}\cos(2\omega t) - 2\omega\cdot\Delta V_{\cos}\sin(2\omega t)\right) \\ &+ \frac{V_{dc}^2 + 2V_{dc}\left(\Delta V_{\sin}\sin(2\omega t) + \Delta V_{\cos}\cos(2\omega t)\right)}{R_{dc}} \end{aligned}, \tag{4.16}$$

and the ripple power to DC side will be:

$$\begin{aligned} p_{dc\_r} &= p_{dc\_r\_\cos}\cos(2\omega t) + p_{dc\_r\_\sin}\sin(2\omega t) \\ &\approx C_{dc}V_{dc}\left(2\omega\cdot\Delta V_{\sin}\cos(2\omega t) - 2\omega\cdot\Delta V_{\cos}\sin(2\omega t)\right). \\ &+ \frac{2V_{dc}\left(\Delta V_{\sin}\sin(2\omega t) + \Delta V_{\cos}\cos(2\omega t)\right)}{R_{dc}} \end{aligned} \tag{4.17}$$

By neglecting $\frac{d\Delta V_{\cos}}{dt}$ and $\frac{d\Delta V_{\sin}}{dt}$ terms, the relationship between the magnitude of ripple power and the magnitude of ripple voltage on DC capacitor satisfies:

$$p_{dc\_r\_\sin} = -C_{dc}V_{dc}\cdot 2\omega\cdot\Delta V_{\cos} + \frac{2V_{dc}\Delta V_{\sin}}{R_{dc}}, \tag{4.18}$$

$$p_{dc\_r\_\cos} = C_{dc}V_{dc}\cdot 2\omega\cdot\Delta V_{\sin} + \frac{2V_{dc}\Delta V_{\cos}}{R_{dc}}. \tag{4.19}$$

Different from SSVC cases, the magnitude of ripple power, $p_{dc\_r\_\sin}$, $p_{dc\_r\_\sin}$ and the magnitude of ripple voltage $\Delta V_{\sin}$, $\Delta V_{\cos}$ are coupled together. By adding a simple decoupling network as it shown in Figure 68, the two compensation terms p_1^*, p_2^* can be designed and

controlled separately. The coefficient of decoupling network can be calculated by:

$$\begin{bmatrix} k_{11} & k_{12} \\ k_{21} & k_{22} \end{bmatrix} = \begin{bmatrix} \frac{2V_{dc}}{R_{dc}} & -C_{dc}V_{dc} \cdot 2\omega \\ C_{dc}V_{dc} \cdot 2\omega & \frac{2V_{dc}}{R_{dc}} \end{bmatrix}^{-1}. \tag{4.20}$$

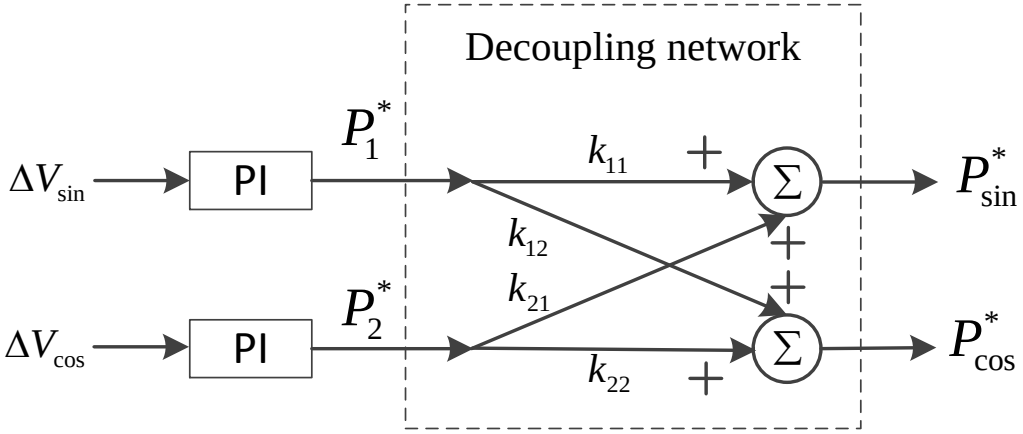


Figure 68: Decoupling network for feedback compensation.

5.4 Improved control system for ripple power with other frequency

In real system, the grid voltage may contain other odd order harmonics. Suppose the grid voltage and the rated grid-side current to be:

$$v_s = V_s \sin(\omega t) + \sum_{n=3,5...} V_n \sin(n\omega t), \tag{4.21}$$

$$i_s = I_s \sin(\omega t + 90^\circ). \tag{4.22}$$

Then, we can get the expression of ripple power, p_{ripple}:

$$p_{ripple} = v_s i_s = \sum_{n=1,2,3...} p_{\sin\_n} \sin(2n\omega t) + p_{\cos\_n} \cos(2n\omega t). \tag{4.23}$$

Since the grid voltage contains odd harmonics, the ripple power contains not only 2ω ripple power, but also other even frequency ripple power.

One advantage of the proposed feedback control system is that it can be easily modified to compensate other even frequency ripple power.

Assume the DC-link voltage to be expressed as

$$v_{dc} = V_{dc} + \sum_{n=1,2,3...} \Delta V_{\sin\_n} \sin(2n\omega t) + \Delta V_{\cos\_n} \cos(2n\omega t) \cdot \tag{4.24}$$

and the ripple power to the DC capacitor is expressed as

$$\begin{aligned} p_{dc\_r} &= C_{dc} \frac{dv_{dc}}{dt} v_{dc} \\ &\approx 2\omega C_{dc} V_{dc} \sum_{n=1,2,3...} \Delta V_{\sin\_n} \cos(2n\omega t) - \Delta V_{\cos\_n} \sin(2n\omega t) \end{aligned} . \tag{4.25}$$

The ripple power to the DC capacitor is the mismatched power between grid side ripple power and AC capacitor power. Based on the mismatched power, the AC capacitor's reference can be compensated to fully absorb ripple power.

Since the proposed control system calculates the AC capacitor voltage reference directly based on the power reference. The compensated capacitor power should be the sum of even frequency ripple power

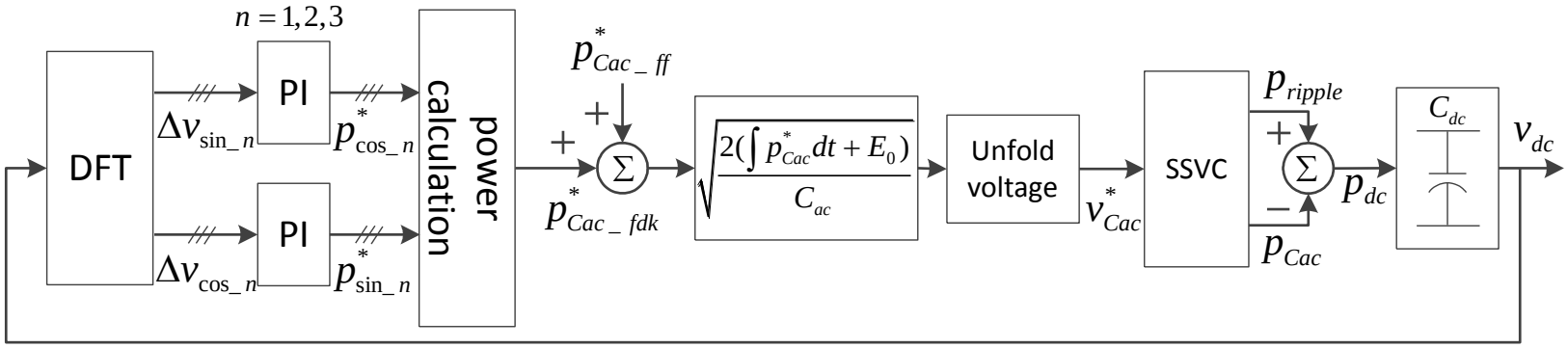


Figure 69: Modified closed-loop compensation for AC capacitor voltage reference.

As it shown in

Figure 69, discrete Fourier transform (DFT) is used to calculate $\Delta V_{\sin\_n}$, $\Delta V_{\cos\_n}, n = 1,2,3...$ from the DC ripple voltage. PI controllers then regulate ripple voltage components toward zero by changing the power compensation terms $p^*_{\cos\_n}, p^*_{\sin\_n}, n = 1,2,3....$. According to the relationship between power mismatch and DC voltage ripple, the compensated capacitor power should be

$$p^*_{Cac\_fdk} = \sum_{n=1,2,3...} -p^*_{\sin\_n}\sin(2n\omega t) + p^*_{\cos\_n}\cos(2n\omega t)\cdot \tag{4.26}$$

5.5 Experimental results

Figure 70 shows the DC voltage FFT analysis of SSVC with half rated and full rated power. The 2ω (120 Hz) voltage is within 0.5 V. According to (5.12), the 2ω ripple power to DC capacitor can be calculated based on the 2ω voltage on DC capacitor. Therefore, the 2ω ripple power is smaller than 1 W, which is 0.067% of the rated power (1.5 kW), indicating that the proposed active power decoupling method have effectively absorbed the 2ω ripple power.

By adopting the improve control system for compensation of grid ripple power with other frequency, the ripple power with other frequencies (240 Hz, 360 Hz, 480 Hz) have also been compensated.

Figure 71 shows the dynamic response to sudden load changes. The control system can track the current and voltage reference quickly. During sudden load change, there is no excessive DC voltage overshoots. After the load changes, the AC capacitor voltage and current will automatically change to compensate the ripple power by the feed-forward control; and the feedback compensation for voltage reference will work instantaneously to further reduce ripple

voltage on DC capacitor.

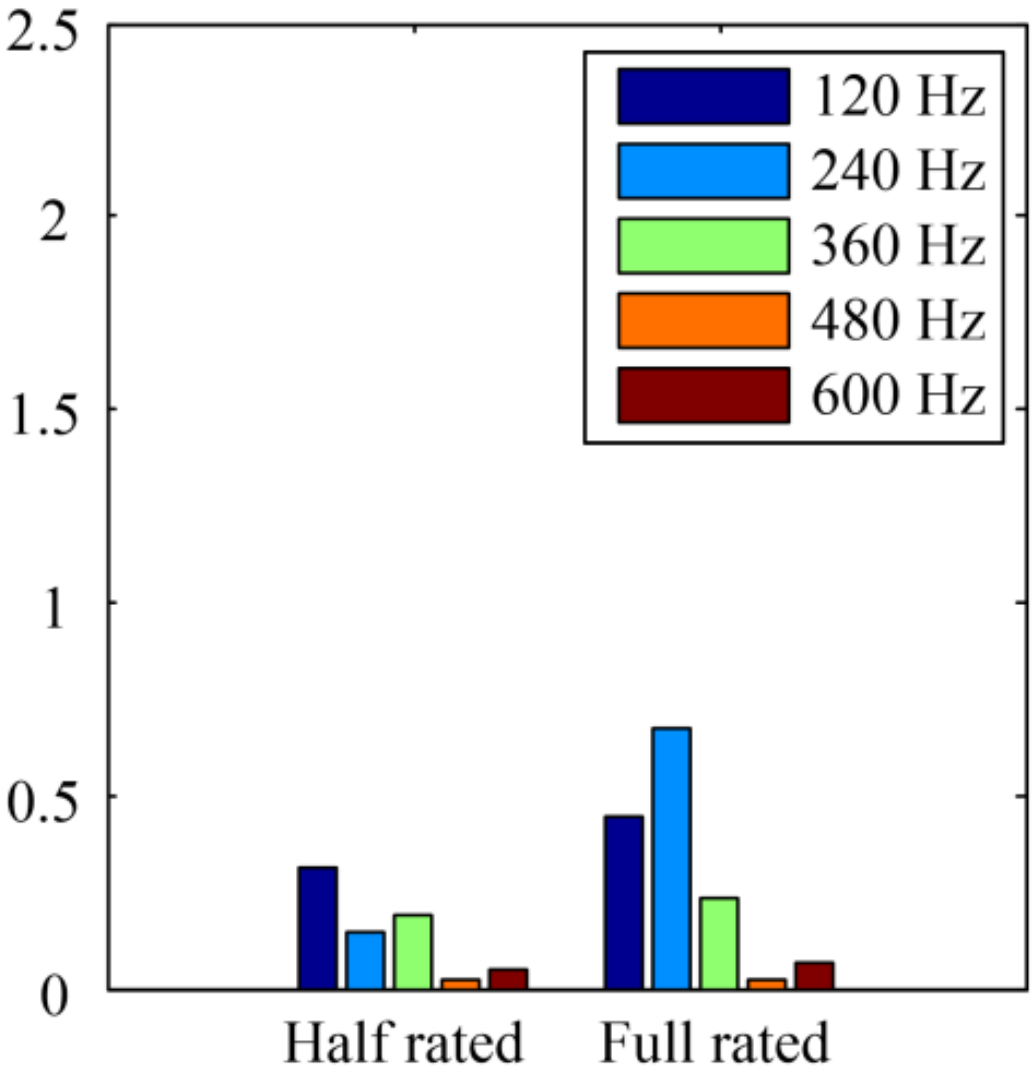


Figure 70: DC voltage FFT analysis.

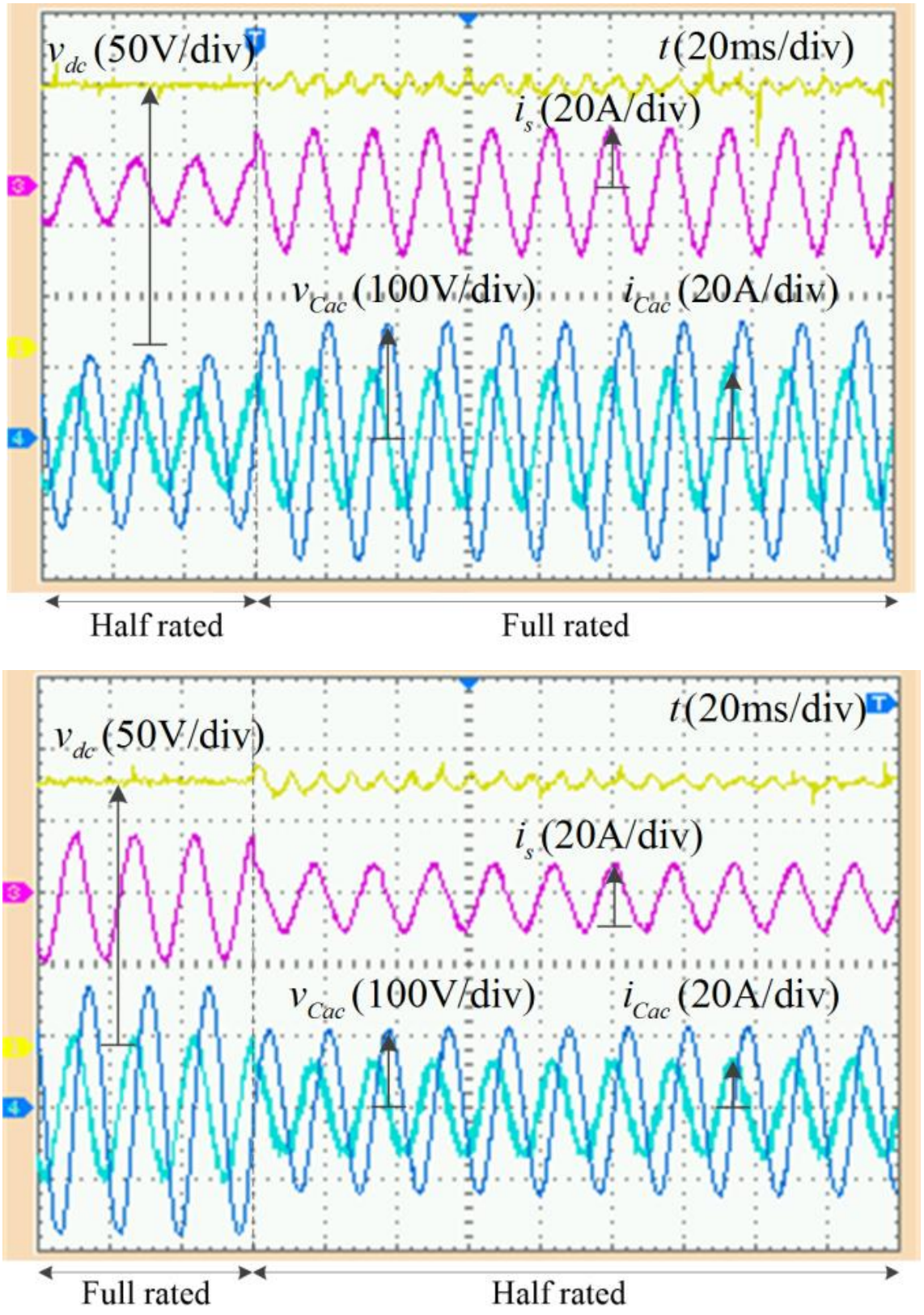


Figure 71: Transient response to sudden load changes.

5.6 Conclusions

A novel control system for solid state variable capacitor (SSVC) is proposed to reduce DC capacitor to minimal value. A closed-loop compensation for capacitor voltage reference is adopted to fully eliminate the ripple power to DC capacitor. The proposed control system calculates AC capacitor voltage and current reference directly based on grid side ripple power and DC capacitor ripple power, without complicated mathematic calculation.

The feedforward part of the AC capacitor power is calculated by grid ripple power, which is updated with the sampling frequency (20-kHz) to achieve fast dynamic response and maintain table DC voltage during sudden load change transition. The feedback part of the AC capacitor power is calculated based on discrete Fourier transform of DC capacitor ripple power with twice line frequency (120-Hz), to achieve better steady-state ripple power compensation performance.

Another advantage of the proposed control scheme is that it can be easily extended to other single phase power applications. In addition, the control scheme can be modified to compensate other even frequency ripple power, since in many cases the grid voltage may contain other frequency harmonics.

The experimental results are shown to verify the steady state and the dynamic performance of the proposed control system.

CHAPTER 6 INTERLEAVED DC-CAPACITOR-LESS SINGLE PHASE INVERTER

Singe phase inverters has been widely used for PV systems. However, conventional H-bridge inverter with bulky electrolytic capacitor has large size, lower power density and relatively low reliability. Making single phase inverter system smaller and more reliable will enable more solar-powered homes, more efficient distributed electrical grids.

In order to achieve a high power density inverter system, an interleaved DC-capacitor-less inverter with SVPWM control is proposed as it shown in Figure 72. The proposed inverter system can work under different power factors from 1 ~ 0.7 both leading and lagging to minimize total device power rating. For worst case of 0.7 leading power factor, the total device power rating of proposed system is only 1.78 times *TDPR* of H-bridge.

By using the two-channel interleaved structure, the conduction loss and passive components' size (both DC input filtering capacitors and AC output filtering inductors) can be significantly reduced [73-80]. Since the inverter is controlled as an unbalanced three phase system, conventional single inverter interleaved PWM scheme cannot achieve the best performance. In order to improve THD for inverter output AC voltage, an enhanced phase-shift interleaved PWM scheme for balanced three phase system is extended to unbalanced there phase system for single phase applications with different power factors.

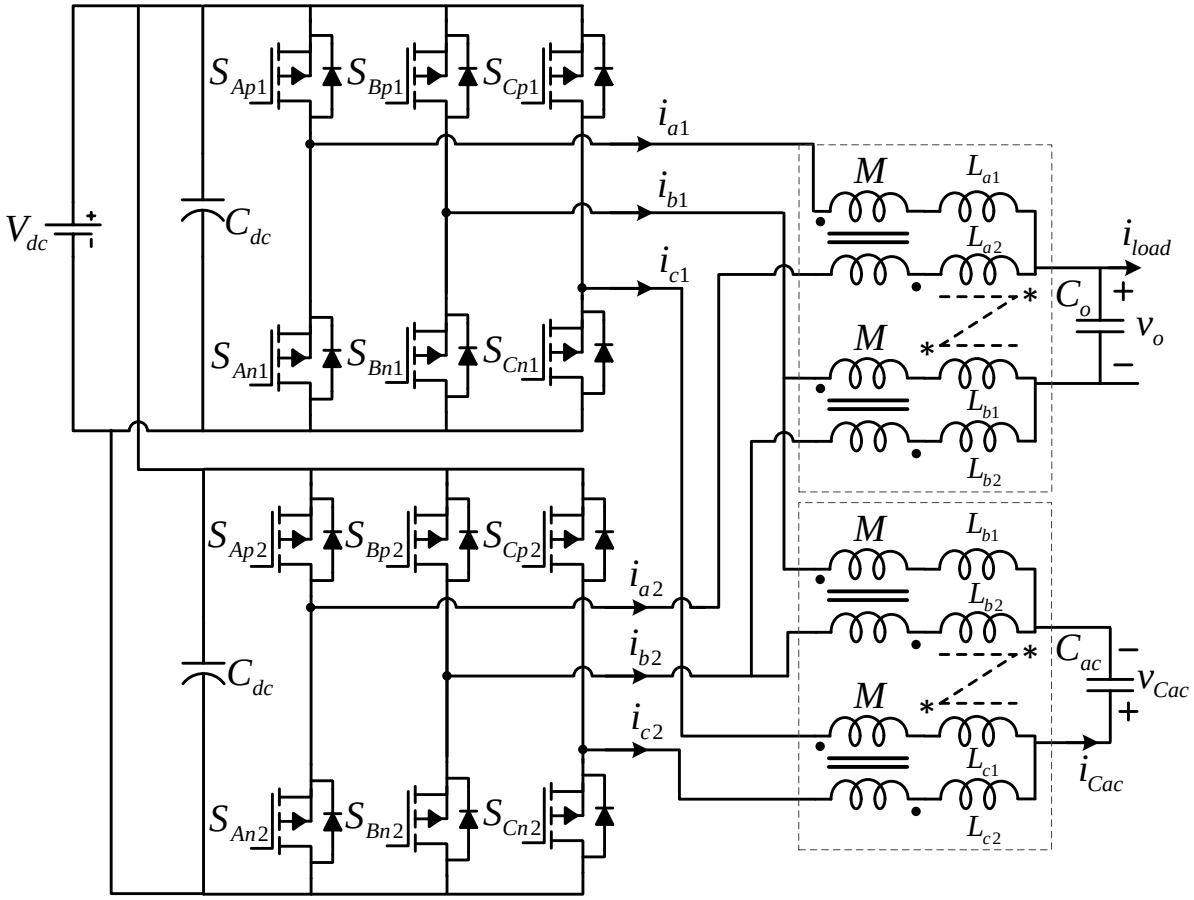


Figure 72: Proposed interleaved DC-capacitor-less inverter system.

For the interleaved structure, a new structure of integrated coupled inductors is proposed to suppress circulating current between the two parallel inverters and to filter output current at the same time. As a result, the total volume of filtering magnetics is reduced by 35% compared to existing design of two separated coupled inductors. In addition, designing the parallel subsystems symmetric will also help to optimize thermal design, since the power loss can be more evenly distributed and more surface area can be utilized for heat dissipation.

As a result, the capacitor size is reduced by more than 16 times with only 1.78 times TDPR of H-bridge circuit. The developed 2-kVA single phase inverter system specification is shown in Table 5.

Table 5: Specification of single phase inverter system.

Maximum load, P_o	2 kW
Power density	> 45 W/in^3
Voltage input	V_{dc_source} = 450 V, R_{dc} = 10 Ω
Voltage output, V_o	240 ± 12 V AC
Voltage frequency, f_o	60 ± 0.2 Hz
Power factor, *pf*	0.7 ~ 1 (leading and lagging)
Output voltage THD	< 5%
Input ripple current (120Hz)	< 20%

6.1 DC voltage requirement and *TDPR* for different power factor

Since the DC source for the single phase inverter is modeled as a constant DC voltage source in series with a DC resistor as it shown in Figure 73, the voltage across DC capacitor, V_{dc}, will vary with the load and power factor, *pf*, while the minimum DC voltage requirement to generate the output AC voltage will also change with load and power factor.

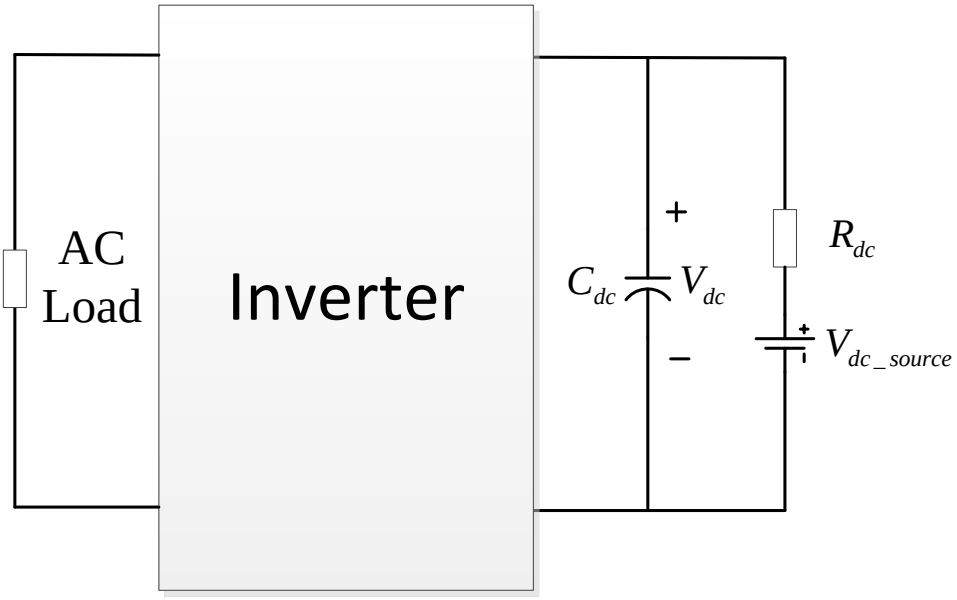


Figure 73: DC source for single phase inverter system.

Based on the previous analysis, the minimum DC voltage requirement will be the same as the conventional H-bridge inverter with SVPWM control if the output current, i_{load}, is lagging the output voltage, v_o. And without considering the power loss, minimum DC voltage requirement will be 340 V with modulation index of 1.

For DC source output voltage, V_{dc}, the minimal voltage happens when the load is maximum with unity power factor (pf = 1), and the minimal DC source output voltage will be 400 V. Therefore, the DC voltage has enough margins (60 V) for the inverter normal operation with output current, i_{load}, lagging the output voltage, v_o.

In order to analysis the current stress and *TDPR* of inverter case with unity power factor and 0.7 lagging power factor, the optimal reference for AC capacitor is analyzed.

For unity power factor case, we can get the expression of grid power:

$$\begin{aligned} p_g &= v_s i_s = V_s I_s[-1-\cos(2\omega t+\pi)] \\ &= V_s I_s[-1+\sin(2\omega t+\frac{\pi}{2})] \end{aligned}, \tag{5.1}$$

which contains DC power component and the 2ω ripple power component

$$p_{2\omega} = V_s I_s \sin(2\omega t + \frac{\pi}{2}). \tag{5.2}$$

The instantaneous power generated by C_{ac} can also be obtained:

$$p_{Cac} = v_{Cac} i_{Cac} = \omega C_{ac} V_{Cac}^2 \sin(2\omega t + 2\theta). \tag{5.3}$$

To simplify the analysis, the power on filter inductors L_{f1} and L_{f2} is neglected. Then, the power of C_{ac} should be controlled equal to the grid 2ω ripple power:

$$p_{Cac} = p_{2\omega}. \tag{5.4}$$

Therefore, the magnitude of v_{Cac} should satisfy the following equations:

$$\omega C_{ac} V_{Cac}^2 = V_s I_s, \tag{5.5}$$

If the decoupling capacitance is designed to be

$$C_{ac} = \frac{I_s}{\omega V_s}, \tag{5.6}$$

the magnitude of the voltage and current of C_{ac} will be:

$$V_{Cac} = V_s, \tag{5.7}$$

$$I_{Cac} = I_s. \tag{5.8}$$

By choosing the optimal phase angle:

$$\theta = \frac{\pi}{4}, \tag{5.9}$$

the current and voltage stress of the system can be minimized.

The phase diagram of unity power factor is shown in Figure 74. And the current stress of shared leg is:

$$I_{peak\_shared} = \sqrt{4I_s^2 - 4I_s^2 \cos(\frac{\pi}{4})} = 0.765 \cdot \sqrt{2} I_s, \tag{5.10}$$

which is 76% of H-bridge current stress.

As a result, the *TDPR* of DC-capacitor-less inverter with SVPWM for inverter application with unity power factor is 1.38 times of H-bridge circuit:

$$\begin{aligned} TDPR &= 4 \cdot V_{dc} \cdot \sqrt{2} I_s + 2 \cdot V_{dc} \cdot 0.765 \sqrt{2} I_s \\ &= 11.06S = 1.38 TDPR_{H-bridge} \end{aligned}, \tag{5.11}$$

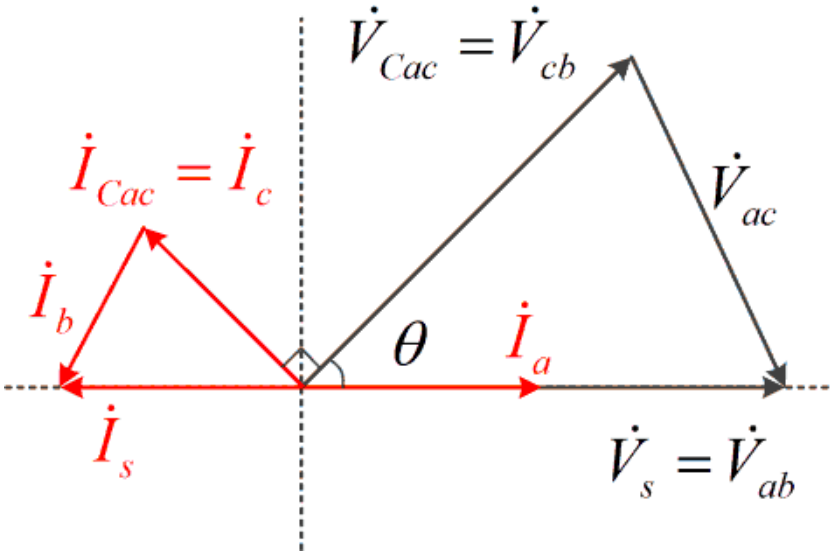


Figure 74: Phasor diagrams of inverter case with unity power factor.

Similarly, for 0.7 lagging power factor case, we can get the expression of grid power:

$$\begin{aligned} p_g &= v_s i_s = V_s I_s [-1 - \cos(2\omega t + \frac{3}{4}\pi)] \\ &= V_s I_s [-1 + \sin(2\omega t + \frac{\pi}{4})] \end{aligned}, \tag{5.12}$$

which contains DC power component and the 2ω ripple power component

$$p_{2\omega} = V_s I_s \sin(2\omega t + \frac{\pi}{4}). \tag{5.13}$$

The instantaneous power generated by C_{ac} can also be obtained:

$$p_{Cac} = v_{Cac} i_{Cac} = \omega C_{ac} V_{Cac}^2 \sin(2\omega t + 2\theta) . \tag{5.14}$$

By choosing the optimal phase angle:

$$\theta = \frac{\pi}{8} \ , \tag{5.15}$$

the current and voltage stress of the system can be minimized.

The phase diagram of 0.7 lagging power factor is shown in Figure 75. And the current stress of shared leg is:

$$I_{peak\_shared} = \sqrt{4I_s^2 - 4I_s^2 \cos(\frac{\pi}{8})} = 0.39 \cdot \sqrt{2} I_s , \tag{5.16}$$

which is 39% of H-bridge current stress.

As a result, the *TDPR* of DC-capacitor-less inverter with SVPWM control for inverter application with 0.7 lagging power factor is 1.2 times of H-bridge circuit:

$$\begin{aligned} TDPR &= 4 \cdot V_{dc} \cdot \sqrt{2} I_s + 2 \cdot V_{dc} \cdot 0.39 \sqrt{2} I_s \\ &= 9.56S = 1.2 TDPR_{H-bridge} \end{aligned} , \tag{5.17}$$

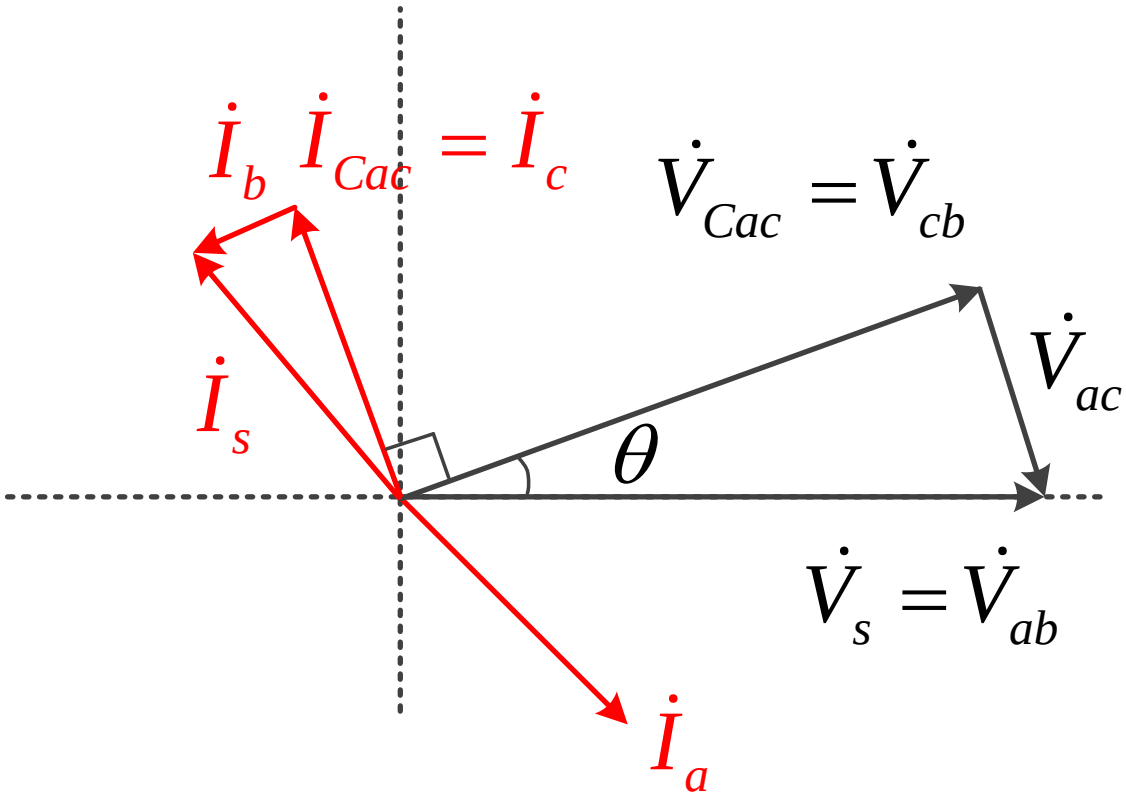


Figure 75: Phase diagram of inverter case with 0.7 lagging power factor.

When the output current, i_o, is leading the output voltage, v_o, the minimum DC voltage requirement and the DC source output voltage, V_{dc} will both vary with power factor.

Based on previous analysis in Chapter 3, the minimum DC voltage requirement can be calculated by the phase angle between output current, i_{load}, and output voltage, v_o. The DC source output voltage, V_{dc} should satisfy the following equation:

$$V_{dc\_source} = V_{dc} + P_o \cdot pf \cdot R_{dc} / V_{dc}, \tag{5.18}$$

and can be calculated by:

$$V_{dc} = \frac{V_{dc\_source} + \sqrt{V_{dc\_source}^{\ 2} - 4P_o \cdot pf \cdot R_{dc}}}{2}. \tag{5.19}$$

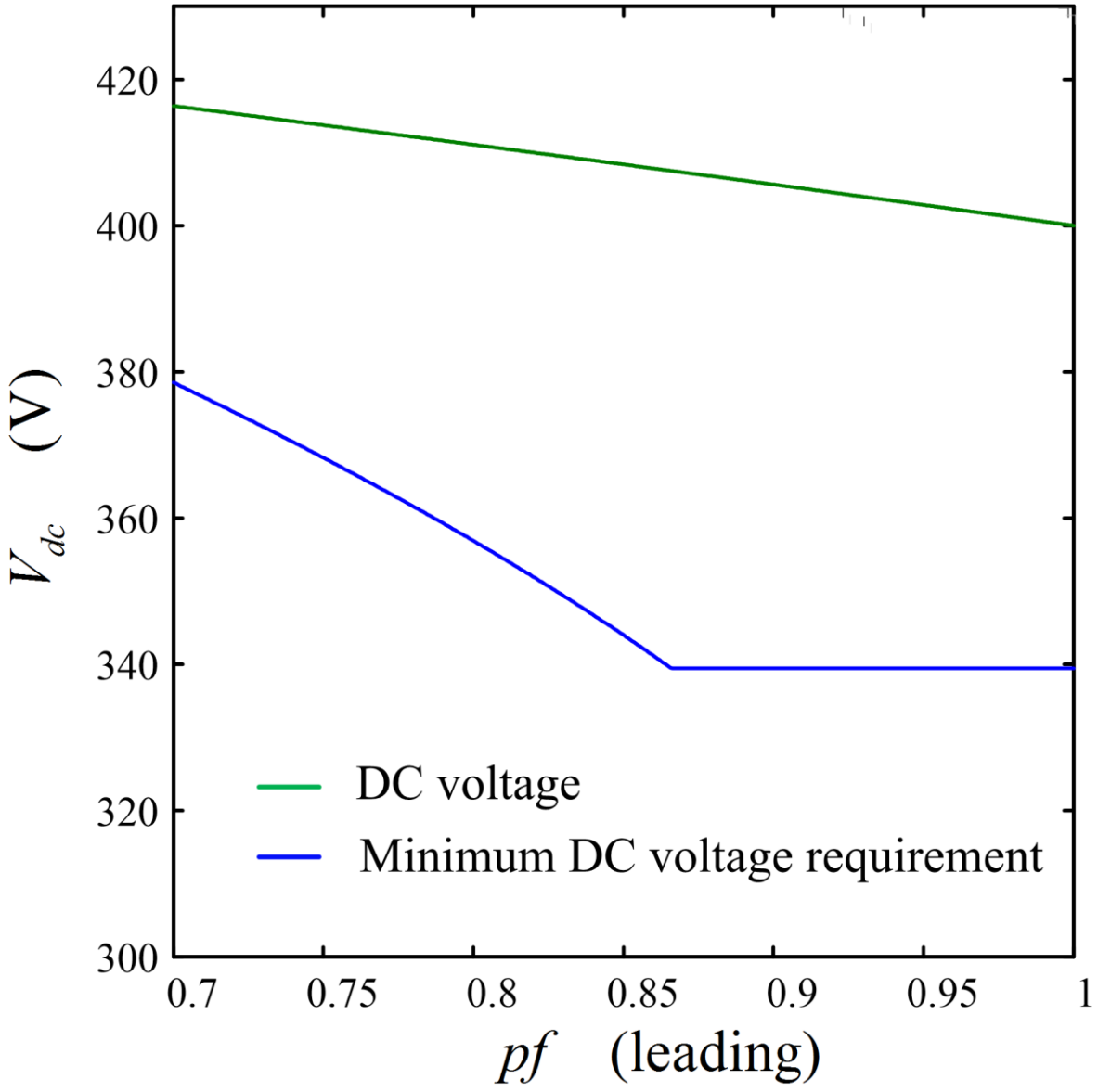


Figure 76: Minimum DC voltage requirement and DC voltage with full load for different *pf* (leading).

The minimum DC voltage requirement and the inverter DC capacitor voltage, V_{dc} with full load for different *pf* (leading) are shown in Figure 76. As we can see, the DC voltage margin is enough when *pf* is from 0.7 to 1.

With the decease of power factor, the minimum DC voltage requirement with SVPWM will

slightly increase. For worst case of 0.7 leading power factor, the minimum DC voltage requirement is determined by the maximum line to line voltage with SVPWM control, and the phase A and phase C has the maximum voltage:

$$\begin{aligned} V_{dc\_\min} &= \sqrt{2}V_{ac} \\ &= \sqrt{4V_s^2 - 4V_s^2\cos(\frac{3\pi}{8})} = 1.11\cdot\sqrt{2}V_s \end{aligned}, \tag{5.20}$$

which is only 1.11 times of H-bridge minimal DC voltage requirement.

Based on analysis in Chapter 3, the current stress of shared leg also reaches maximum when power factor is 0.7 leading. The phase diagram of the worst case is shown in Figure 77. And the current stress of shared leg is:

$$I_{peak\_shared} = \sqrt{4I_s^2 - 4I_s^2\cos(\frac{3\pi}{8})} = 1.11\cdot\sqrt{2}I_s, \tag{5.21}$$

which is only 1.11 times of H-bridge current stress.

As a result, the *TDPR* of DC-capacitor-less inverter with SVPWM for inverter application with 0.7 leading power factor is 1.78 times of H-bridge circuit:

$$\begin{aligned} TDPR &= 4\cdot 1.11V_{dc}\cdot\sqrt{2}I_s + 2\cdot 1.11V_{dc}\cdot 1.11\sqrt{2}I_s \\ &= 14.3S = 1.78TDPR_{H-bridge} \end{aligned}. \tag{5.22}$$

For the single phase inverter system based on DC-capacitor-less inverter with SVPWM, a very small DC filtering capacitor is needed for switching ripple. The DC capacitor is 0.2 times of AC capacitor size with 200-kHz switching frequency. In the next chapter, the hardware and software optimization of the proposed system and control method are explained in details to achieve good steady state and dynamic performance with the small DC capacitor size.

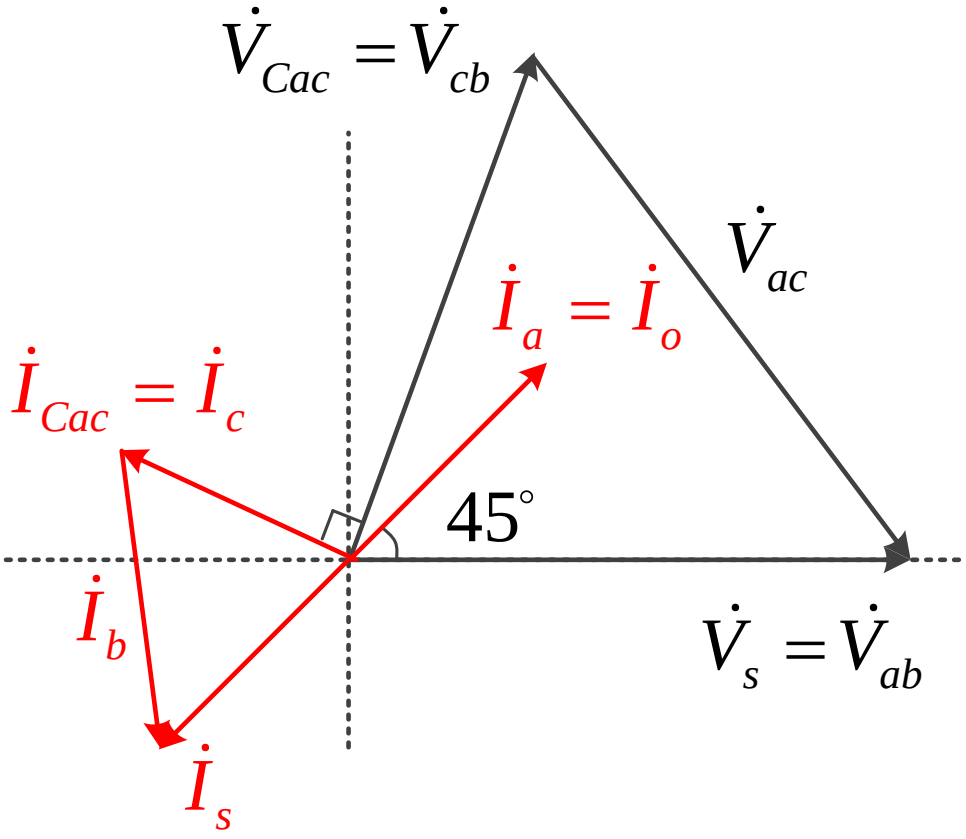


Figure 77: Phase diagram of inverter case with 0.7 leading power factor.

In order to show the benefit of proposed method in single phase inverter application, the voltage and current stress of other existing methods are analyzed. The following analysis will take unity power factor inverter case as an example and the other power factor cases can be analyzed accordingly.

In Figure 10, the energy-storage capacitor, C_d is connected to DC link by a buck converter, and the capacitor voltage is unipolar. If the capacitor voltage reference is a full-wave rectified sinusoidal waveform, the 2ω ripple power can be transferred to the capacitor. The key waveforms for unity power factor inverter are shown in Figure 78.

The energy-storage capacitor's voltage and current are expressed as

$$v_{Cd} = \sqrt{2}V_{Cd}\left|\sin(\omega t + \frac{\pi}{4})\right|, \tag{5.23}$$

$$\begin{aligned} i_{Cd} &= \sqrt{2}I_{Cd}\cos(\omega t + \frac{\pi}{4})\cdot \mathrm{sgn}(\sin(\omega t + \frac{\pi}{4})) \\ &= \sqrt{2}\omega C_d V_{Cd}\cos(\omega t + \frac{\pi}{4})\cdot \mathrm{sgn}(\sin(\omega t + \frac{\pi}{4})) \end{aligned}. \tag{5.24}$$

Then the power stored in the energy-storage capacitor will be

$$p_{Cd} = V_{Cd}I_{Cd}\sin(2\omega t + \frac{\pi}{2}) = \omega C_d V_{Cd}^2 \sin(2\omega t + \frac{\pi}{2}). \tag{5.25}$$

As it shown in Figure 78, the power of C_d is controlled equal to the grid 2ω ripple power:

$$p_{Cd} = p_{2\omega}. \tag{5.26}$$

Then, the 2ω power to DC side can be fully eliminated.

By designing C_d to be:

$$C_d = \frac{I_s}{\omega V_s}, \tag{5.27}$$

the DC voltage can be fully utilized, and energy-storage capacitor's voltage and current magnitude will be:

$$V_{Cd} = V_s, \tag{5.28}$$

$$I_{Cd} = I_s. \tag{5.29}$$

In ideal case, the DC link voltage will be:

$$V_{dc} = \sqrt{2}V_s. \tag{5.30}$$

and the energy storage requirement is equal to the minimal value:

$$E_C = \frac{1}{2}C_d V_{dc}^2 = \frac{S}{\omega} = E_{C\_\min}, \tag{5.31}$$

and *TDPR* for all applications for unit power factor inverter application will be:

$$TDPR = 4 \cdot V_{dc} \cdot \sqrt{2} I_s + 2 \cdot V_{dc} \cdot \sqrt{2} I_s = 12S = 1.5 TDPR_{H-bridge} \quad (5.32)$$

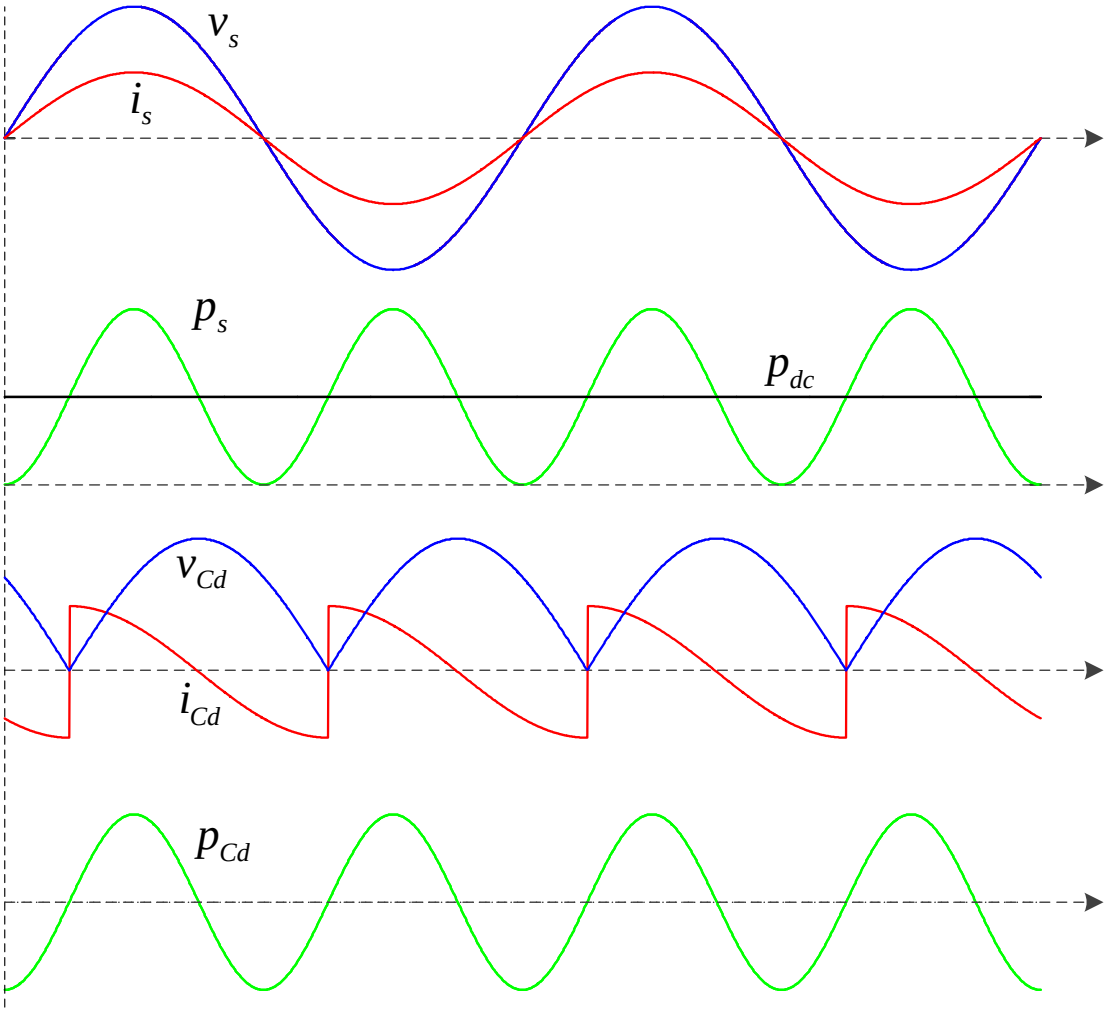


Figure 78: Single phase converter with unipolar energy-storage capacitor key waveforms for unity power factor inverter cases

However, the full-wave rectified sinusoidal reference, which contains rich harmonics, is difficult for the control system to track. Although it is possible to decrease the harmonics in the reference by increasing the energy-storage margin (therefore the capacitor voltage does not go down to zero), this will compromise full utilization of the energy-storage capacitor. Therefore, in

real application, E_C will be larger than the ideal case, E_{Cmin}. The minimal reported E_C is 1.5 $E_{C\_\min}$. In additional, the system requires DC capacitor with the same size of energy-storage capacitor, C_d.

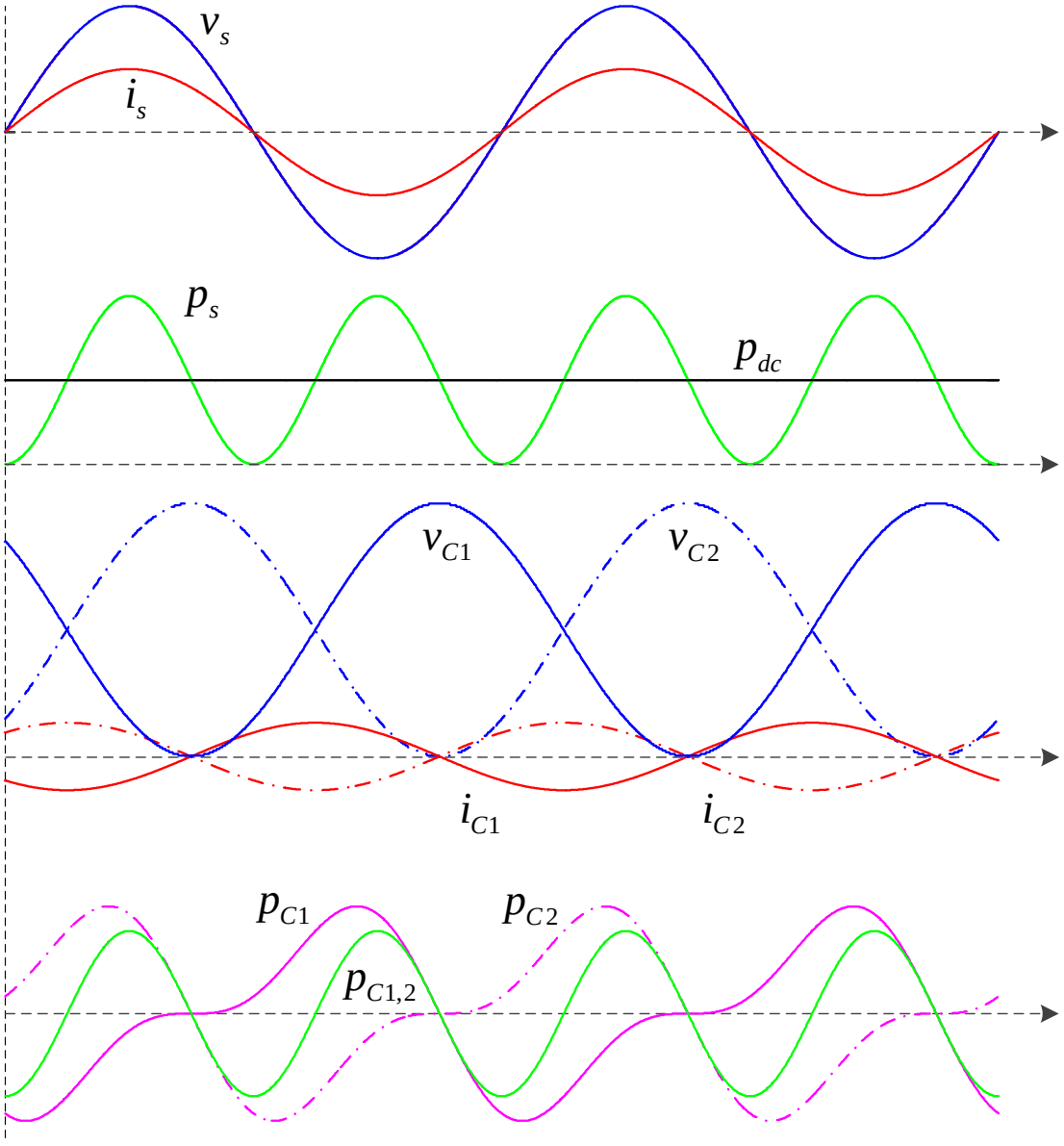


Figure 79: Single phase converter with half bridge for ripple compensation key waveforms for unity power factor inverter case

In Figure 12, the inverter system consists of an H-bridge and a half-bridge circuit for ripple power compensation [38]. The voltage/current waveforms and power are shown in Figure 79. The sum of the power of C_1 and C_2 is controlled to be equal to the 2ω ripple power on grid side.

The two DC capacitors' voltage and current are express as:

$$v_{C1} = \frac{V_{dc}}{2} - \sqrt{2}V_C \sin(\omega t + \frac{\pi}{4}), \tag{5.33}$$

$$v_{C2} = \frac{V_{dc}}{2} + \sqrt{2}V_C \sin(\omega t + \frac{\pi}{4}), \tag{5.34}$$

$$\begin{aligned} i_{C1} &= -i_{C2} = -\sqrt{2}I_C \cos(\omega t + \frac{\pi}{4}) \\ &= -\sqrt{2}\omega C_f V_C \cos(\omega t + \frac{\pi}{4}) \end{aligned}. \tag{5.35}$$

Then, the sum of power of C_1 and C_2 will be

$$p_{C1,2} = v_{c1}i_{c1} + v_{c2}i_{c2} = 2\omega C_f V_C^2 \sin(2\omega t + \frac{\pi}{2}). \tag{5.36}$$

By designing C_f to be:

$$C_1 = C_2 = C_f = \frac{I_s}{2\omega V_s}. \tag{5.37}$$

The DC capacitors' voltage and current magnitude will be:

$$V_C = V_s, \tag{5.38}$$

$$I_C = I_s / 2. \tag{5.39}$$

Since the peak voltages of C_1 and C_2 are V_{dc}, the DC voltage will be

$$V_{dc} = 2\sqrt{2}V_s, \tag{5.40}$$

which is double of the DC voltage requirement of conventional H-bridge system. The peak currents of C_1 and C_2 is equal to $\sqrt{2}I_s / 2$. The peak currents of S_5 and S_6 are equal to AC output

peak current.

The energy storage requirement will be:

$$E_C = 2 \times \frac{1}{2} C_f V_{dc}^2 = \frac{4S}{\omega} = 4E_{C\_\min}, \tag{5.41}$$

and *TDPR* for unity power factor inverter application will be:

$$TDPR = 6 \cdot V_{dc} \cdot \sqrt{2} I_s = 3TDPR_{H-bridge}. \tag{5.42}$$

The advantage of this circuit is that C_1 and C_2 are also utilized as the DC filter capacitor. However, in order to keep the switches' current stress same as the H-bridge, the required DC voltage of the circuit is double of H-bridge's DC voltage. Therefore, *TDPR* is 3 times of $TDPR_{H\text{-}bridge}$. In addition, the voltages of C_1 and C_2 have a DC component of half DC link voltage to maintain a constants DC voltage, which is the sum of the voltage of C_1 and C_2. The individual power of C_1 and C_2 has another component with the line frequency, beside 2ω ripple power. Although the line frequency components of the power of C_1 and C_2 are cancelled out, the energy of C_1 and C_2 are not fully used for 2ω ripple power compensation and the energy storage requirement E_C is significantly increased, which is 4 times of E_{Cmin}.

In Figure 14, the circuit combines the half-bridge circuit for ripple power compensation with one leg of the H-bridge inverter in Figure 12. Therefore, the circuit has the minimum components among the existing topologies. And the energy storage requirement E_C remains the same, which is 4 times of E_{Cmin}.

The current stress of the shared leg can be calculated by:

$$I_{peak\_shared} = \sqrt{4I_s^2 - 4I_s^2 \cos(\frac{\pi}{4})} = 0.76 \cdot \sqrt{2} I_s. \tag{5.43}$$

Therefore, the *TDPR* is reduced:

$$TDPR = 4 \cdot V_{dc} \cdot \sqrt{2} I_s + 4 \cdot V_{dc} \cdot I_{peak\_shared} = 14.08S = 1.76 TDPR_{H-bridge} . \quad (5.44)$$

An inverter system can also be implemented by the circuit with the power decoupling ripple-port shown in Figure 16. By adding any extra H-bridge to interface the energy-storage capacitor, the capacitor works in AC mode and the voltage/current waveforms are sinusoidal as it shown in Figure 80.

The capacitor's voltage and current are expressed as

$$v_{Cac} = \sqrt{2} V_{Cac} \sin(\omega t + \frac{\pi}{4}) , \quad (5.45)$$

$$i_{Cac} = \sqrt{2} I_{Cac} \cos(\omega t + \theta) = \sqrt{2} \omega C_{ac} V_{Cac} \cos(\omega t + \frac{\pi}{4}) . \quad (5.46)$$

Then the power of the AC capacitor will be

$$p_{Cac} = V_{Cac} I_{Cac} \sin(2\omega t + \frac{\pi}{2}) = \omega C_{ac} V_{Cac}^2 \sin(2\omega t + \frac{\pi}{2}) . \quad (5.47)$$

By designing C_{ac} to be:

$$C_{ac} = \frac{I_s}{\omega V_s} , \quad (5.48)$$

the DC voltage can be fully utilized, and AC capacitor voltage/current magnitude will be:

$$V_{Cac} = V_s , \quad (5.49)$$

$$I_{Cac} = I_s . \quad (5.50)$$

In ideal case, the DC voltage will be:

$$V_{dc} = \sqrt{2} V_s , \quad (5.51)$$

and the energy storage requirement is:

$$E_C = \frac{1}{2} C_{ac} (\sqrt{2} V_{Cac})^2 = C_{ac} V_{ac}^2 = \frac{S}{\omega} = E_{C\_\min} , \quad (5.52)$$

and *TDPR* for unity power factor inverter will be:

$$\begin{aligned} TDPR &= 4 \cdot V_{dc} \cdot \sqrt{2} I_s + 4 \cdot V_{dc} \cdot \sqrt{2} I_s \\ &= 16S = 2TDPR_{H-bridge} \end{aligned} . \tag{5.53}$$

The SSVC system based on circuit in Figure 16 also needs a DC filtering capacitor with 0.6 times of AC capacitor. However, [41] has not demonstrated the performance of the control system with dynamic response to sudden load change.

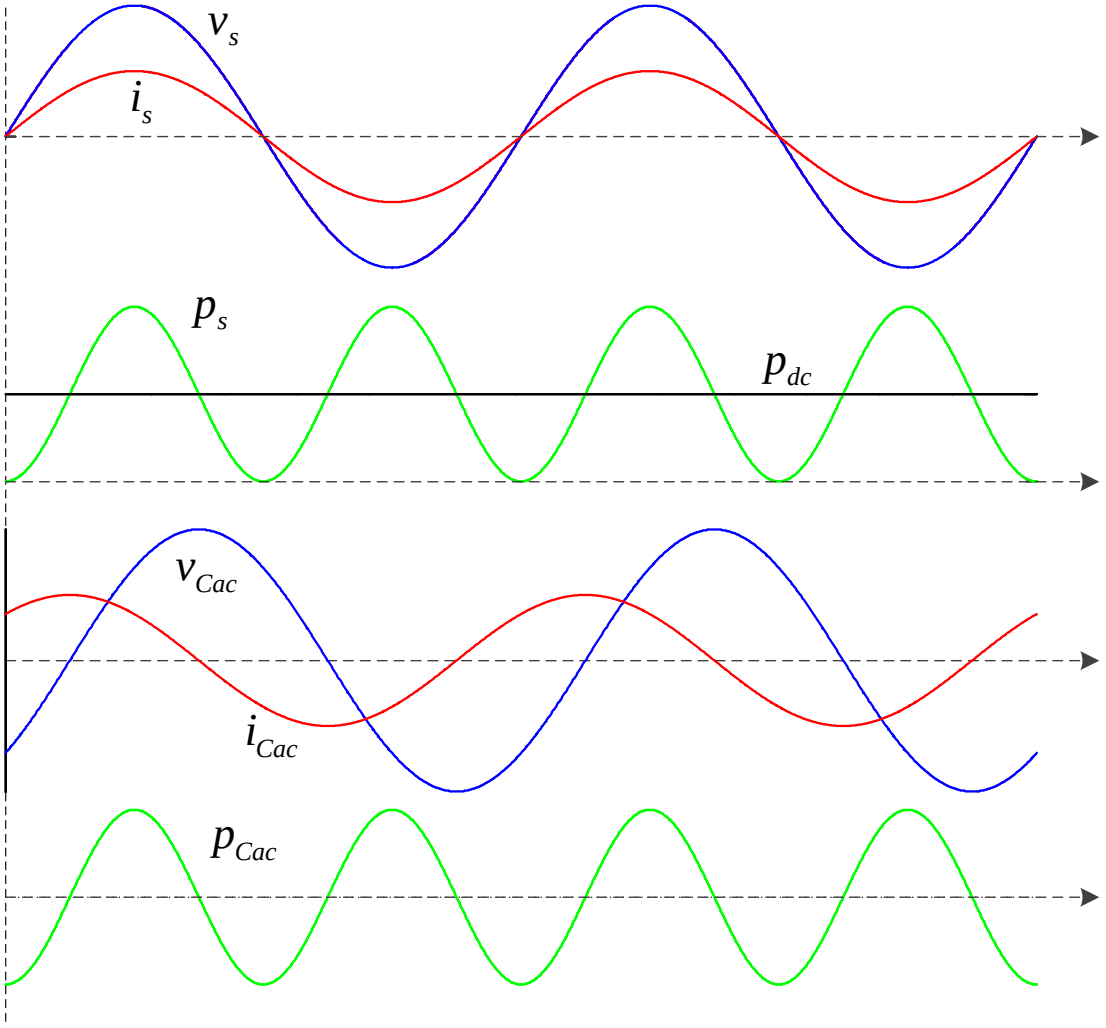


Figure 80: Single phase converter with minimal component for ripple compensation key waveforms for unity power factor inverter cases.

Table 6: Comparison of E_C and *TDPR* of different methods for inverter applications with different power factors.

Methods to reduce DC capacitor of H-bridge for inverter application	***Ec***	***DC capacitor***	***TDPR (pf =1)***	***TDPR (pf = 0.7 leading)***	***TDPR (pf = 0.7 lagging)***
circuit in Figure 10	$1.5Ec_{min}$	Same size as energy storage capacitor	1.5 $TDPR_{H\text{-}bridge}$	1.5 $TDPR_{H\text{-}bridge}$	1.5 $TDPR_{H\text{-}bridge}$
circuit in Figure 12	$4Ec_{min}$	Not required	3 $TDPR_{H\text{-}bridge}$	3 $TDPR_{H\text{-}bridge}$	3 $TDPR_{H\text{-}bridge}$
circuit in Figure 14	$4Ec_{min}$	Not required	1.8 $TDPR_{H\text{-}bridge}$	2.34 $TDPR_{H\text{-}bridge}$	1.4 $TDPR_{H\text{-}bridge}$
circuit in Figure 16	Ec_{min}	0.6 times of energy storage capacitor	2 $TDPR_{H\text{-}bridge}$	2 $TDPR_{H\text{-}bridge}$	2 $TDPR_{H\text{-}bridge}$
DC-capacitor-less inverter with SVPWM	Ec_{min}	0.2 times of energy storage capacitor	1.39 $TDPR_{H\text{-}bridge}$	1.78 $TDPR_{H\text{-}bridge}$	1.2 $TDPR_{H\text{-}bridge}$

The E_C and *TDPR* of each method for inverter application with power factors of 1, 0.7 leading and 0.7 lagging are summarized in Table 6.

Among the five methods, the DC-capacitor-less inverter with SVPWM has shown best performance in terms of E_C and *TDPR*, in other words, smaller size of capacitor and lower cost of

semiconductor devices.

For circuit in Figure 10, Figure 12 and Figure 16, the extra circuit for ripple power compensation is controlled independently with H-bridge inverter, and the total device rating remains the same for different power factors. Circuit in Figure 10 has low *TDPR* (1.5 times of H-bridge) for all power factors (1 ~ 0.7 leading and lagging), however the E_C has to be designed larger than minimal value, and best reported value is 1.5 times of E_{Cmin} [39].

For circuit in Figure 14 and proposed DC-capacitor-less inverter with SVPWM, H-bridge inverter shares leg with extra circuit for ripple power compensation. The current stress of the shared leg and minimal DC voltage requirement may change with power factor. For both methods, the worst case happens when power factor is 0.7 leading.

Compared to the topologies in Figure 16 with the same minimal E_C, the *TDPR* of proposed system is 11% smaller for worst case of 0.7 leading power factor. Compared to the topologies in Figure 10 with 1.5 times *TDPR* of H-bridge circuit, the E_C of proposed system is 33% smaller.

6.2 Interleaved phase shift PWM scheme

As it shown in Figure 81, the single phase inverter system adopts interleaving technique to achieve higher equivalent switching frequency and reduce the filter size [74, 76-80]. The Thevenin-equivalent output voltage between phase A and phase B becomes:

$$v_{ab\_eq} = \frac{v_{a1} + v_{a2} - v_{b1} - v_{b2}}{2} . \tag{5.54}$$

For conventional interleaved single phase inverter system, phase-shifted PWM scheme adopts the two carriers (v_{carr1}, and v_{carr2}) with phase angles of 0 °, 90 °respectively; and the output voltage can achieve best THD. As it shown in Figure 82, the equivalent voltage switching only happens

between adjacent levels.

However for the proposed interleaved inverter system, where SVPWM is adopted, although the interleaving technique yields the best attainable phase output voltage in terms of THD with 180 ° phase shift of the PWM carriers, it is not the case for line-to-line output voltages.

Figure 82 and Figure 83 illustrate the cases with 90 °and 180 °phase shift of PWM carriers for the proposed system using SVPWM respectively. The reference signals (v_a^* , v_b^*, and v_c^*) are compared to their respective carrier signal to set the ON–OFF state of the switches.

In Figure 82, the phase angles for the two carriers (v_{carr1}, and v_{carr2}) are 0 °, 90 °; and in Figure 83, the phase angles for the two carriers (v_{carr1}, and v_{carr2}) are 0 °, 180 °. For both cases, during certain intervals, the equivalent line-to-line voltage, v_{ab_eq} is switching among three adjacent levels.

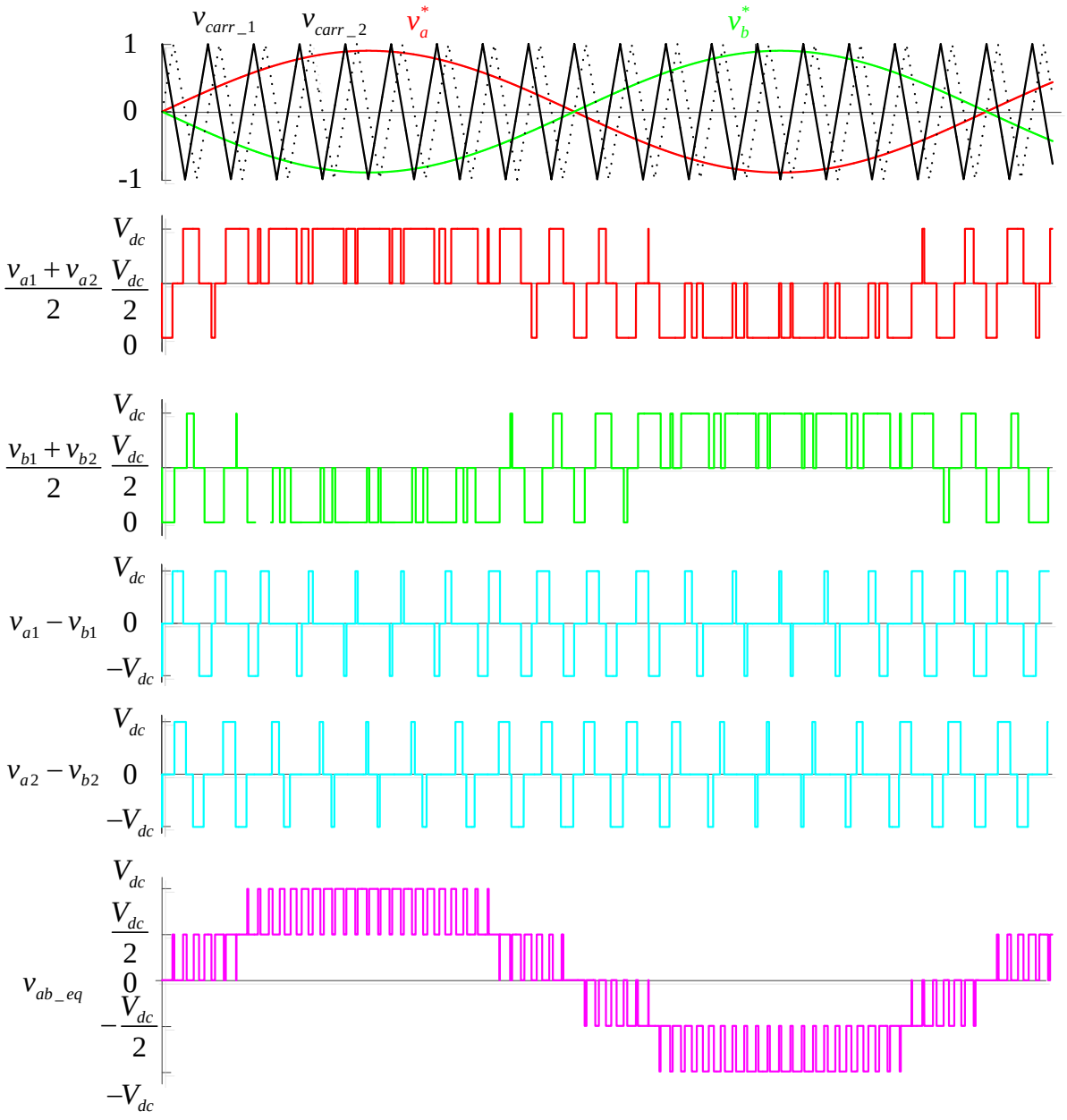


Figure 81: Key waveforms for SPWM single phase inverter using carriers with 90 °phase shift.

However, an interesting phenomenon can be found: if carriers with phase angles of 0 °, 90 °are used, v_{ab_eq} only switches between adjacent levels, when two phase reference signals have different polarities; if carriers with phase angles of 0 °, 180 ° are used, v_{ab_eq} is only switching between adjacent levels when two phase's reference signals have the same polarity. Based on this

characteristic, an enhanced phase-shift PWM carrier scheme [81-83] can be developed.

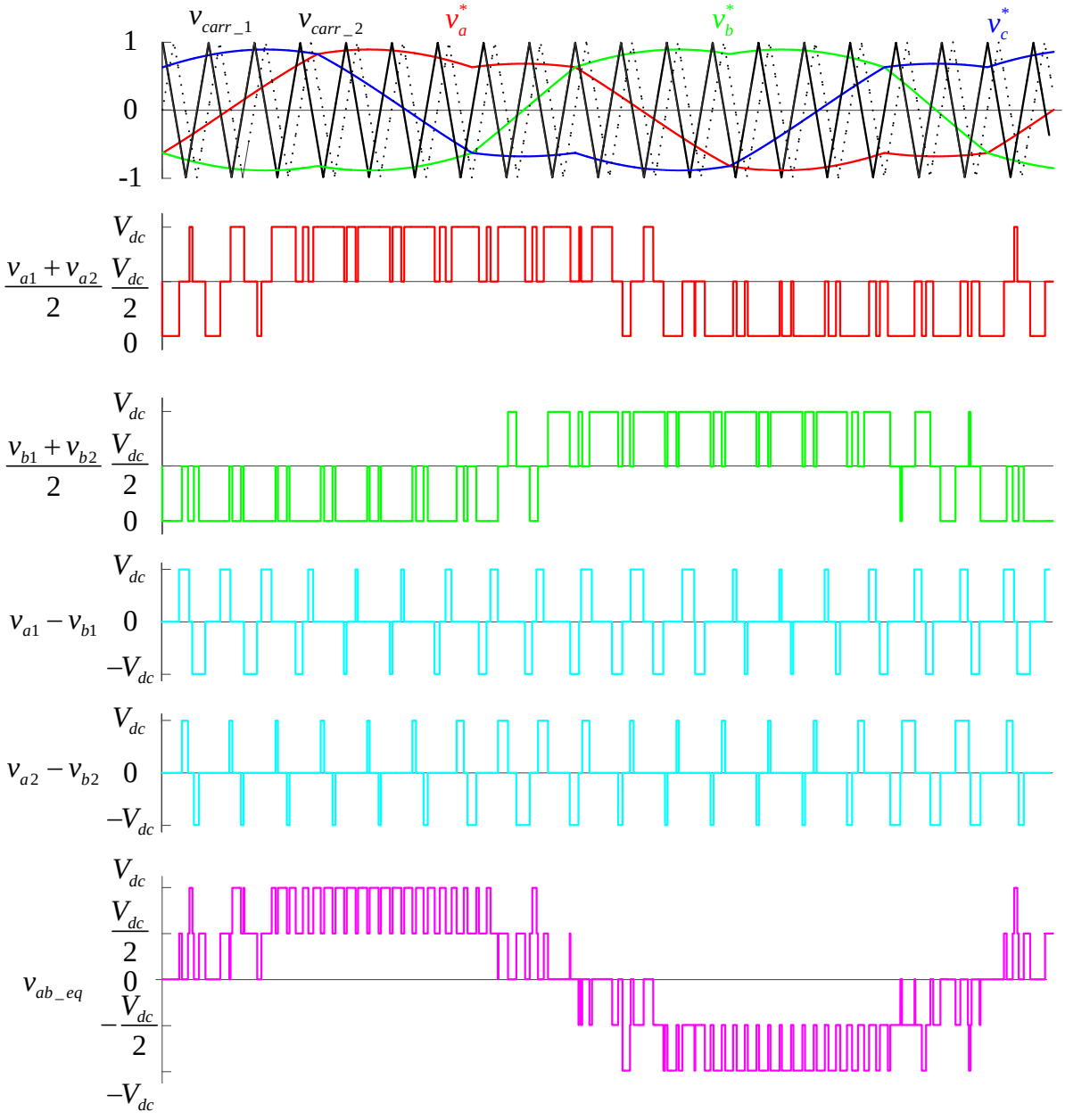


Figure 82: Key waveforms for proposed SVPWM single phase inverter using carriers with 90 ° phase shift.

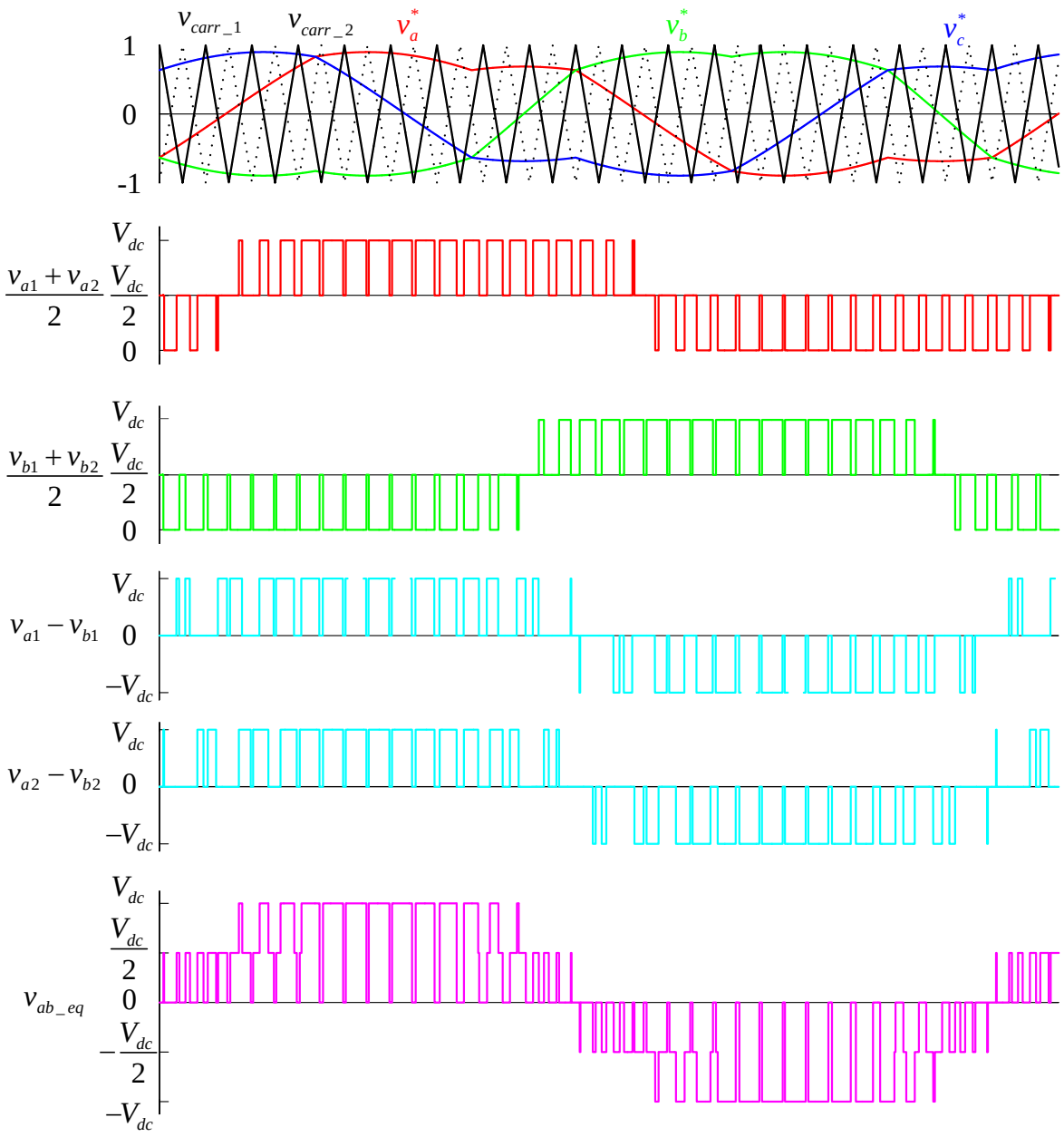


Figure 83: Key waveforms for proposed SVPWM single phase inverter using carriers with 180 ° phase shift.

As shown in Figure 84, two sets of carriers are used. The phase angles for the two carriers in set 1 (v_{carr11}, and v_{carr12}) are 0 °, 180 °; the phase angles for the two carriers in set 2 (v_{carr21}, and v_{carr22}) are 90 °, 270 °. When the reference signals are larger than 0, set 1 carries are used; when the

reference signals are smaller than 0, set 2 carries are used. As a result, V_{ab_eq} only switches between adjacent levels.

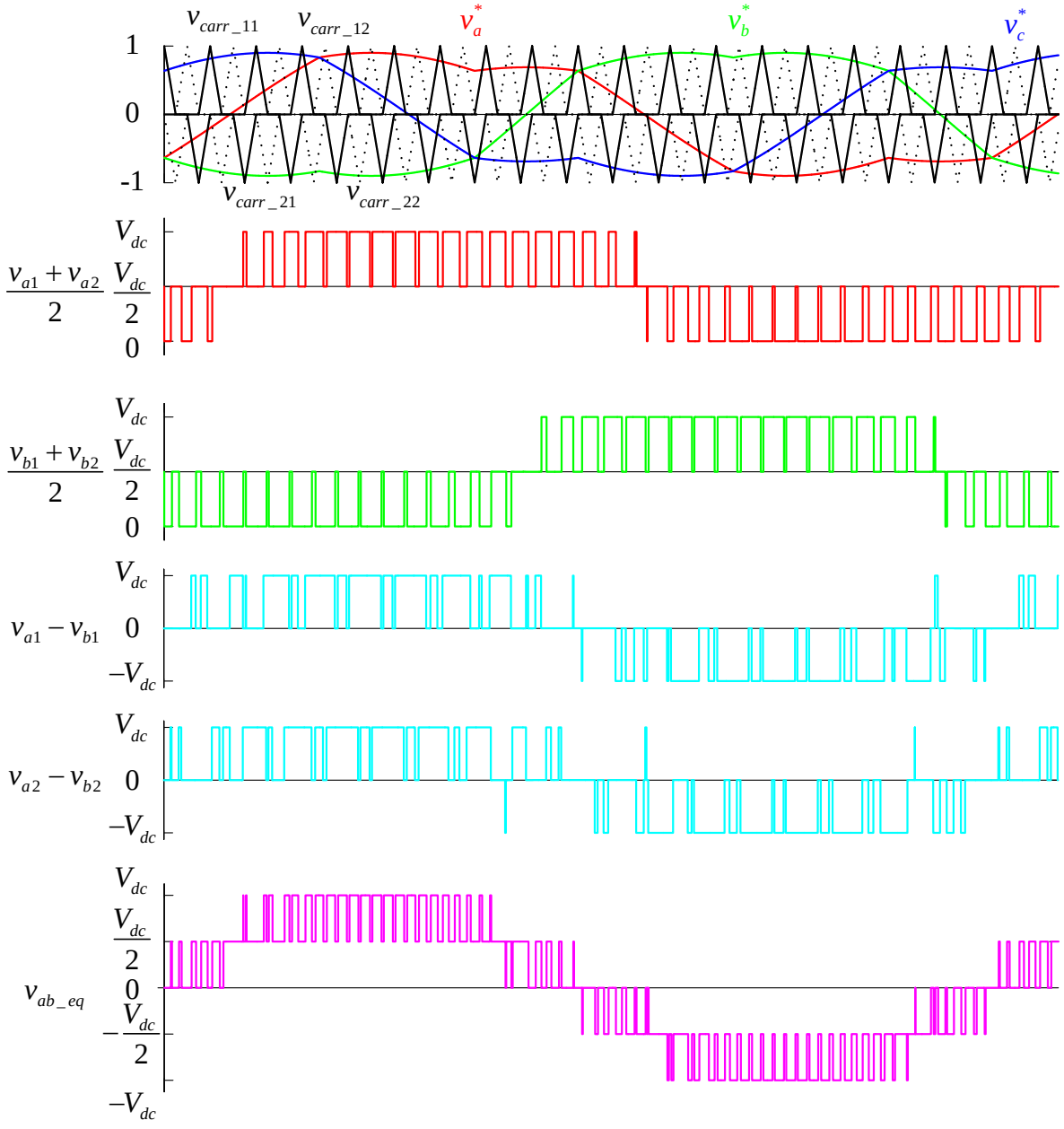


Figure 84: Key waveforms for proposed SVPWM single phase inverter using two sets of carriers.

In [83], the line-to-line THD versus modulation index for balanced three phase system is analyzed in detailed. In this application, the AC output voltage is fixed and the change of DC

capacitor voltage is small; however, the AC capacitor voltage will be controlled to compensate the grid 2ω ripple power. Since the system is controlled as unbalanced three phase system, the reference signals will change with different AC output power; and the output AC voltage THD will change simultaneously.

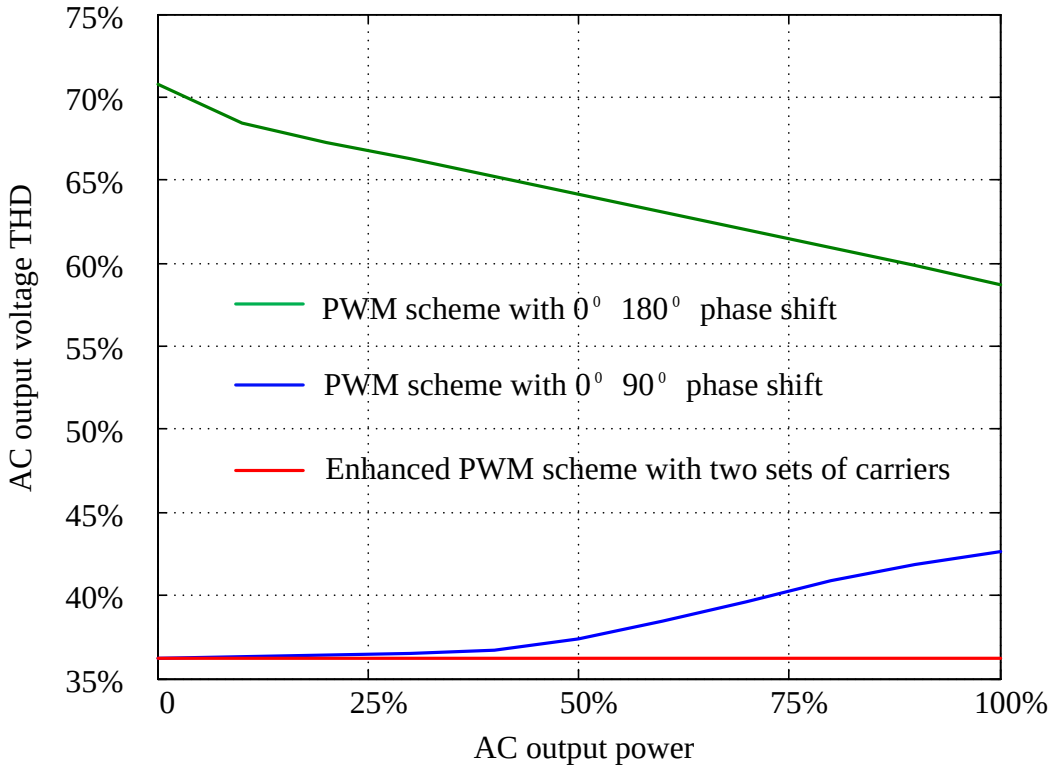


Figure 85: AC output voltage THD versus AC power with different interleaved PWM scheme: unity power factor resistance load.

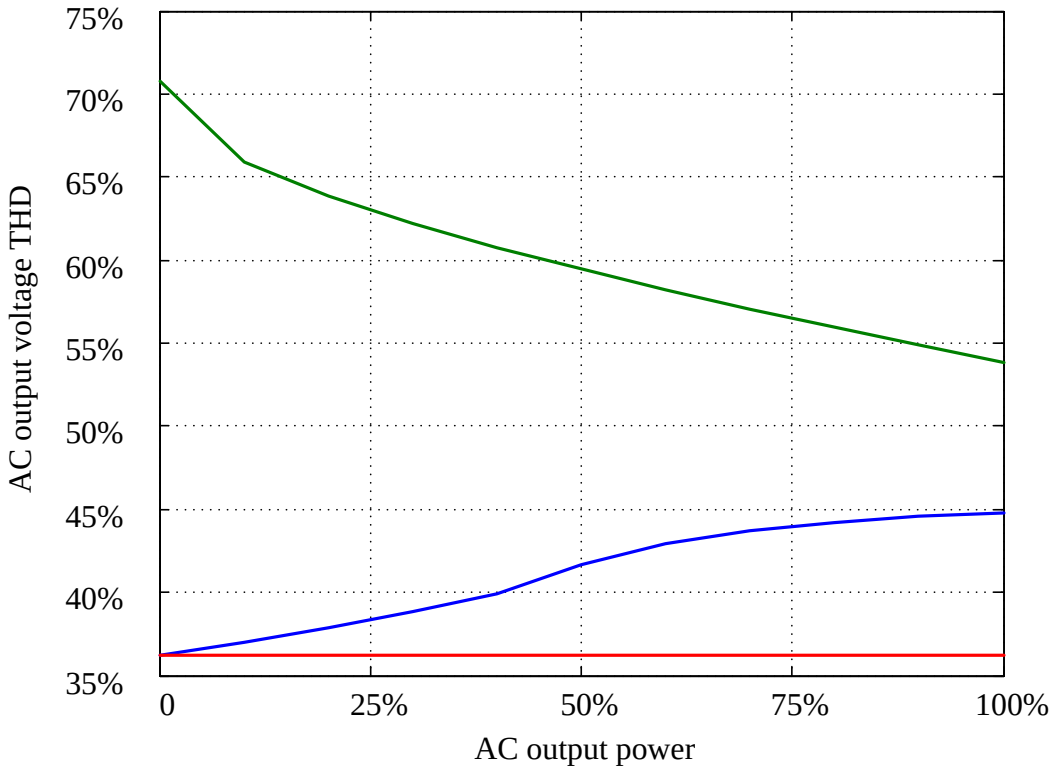


Figure 86: AC output voltage THD versus AC power with different interleaved PWM scheme: 0.7 power factor capacitive load.

Figure 85, Figure 86 and Figure 87 show the AC output voltage THD versus AC power with different PWM scheme. It can be seen that the THD performance has been effectively improved by adopting the enhanced phase-shift PWM carrier scheme.

With the increase of AC output power, the THD with PWM scheme using carriers with 180 ° phase shift decreases; and the THD with PWM scheme using carriers with 90 ° phase shift increases; THD with PWM scheme using two sets of carriers remains the same and can achieve the best THD performance.

For different types of load, the THD performances with different PWM schemes are also different. THD with PWM scheme using carriers with 180 ° phase shift has best performance

when inverter is connected capacitive load; and the THD with PWM scheme using carriers with 90 °phase shift has best performance when inverter is connected inductive load; THD with PWM scheme using two sets of carriers remains the same for different load and can achieve the best performance.

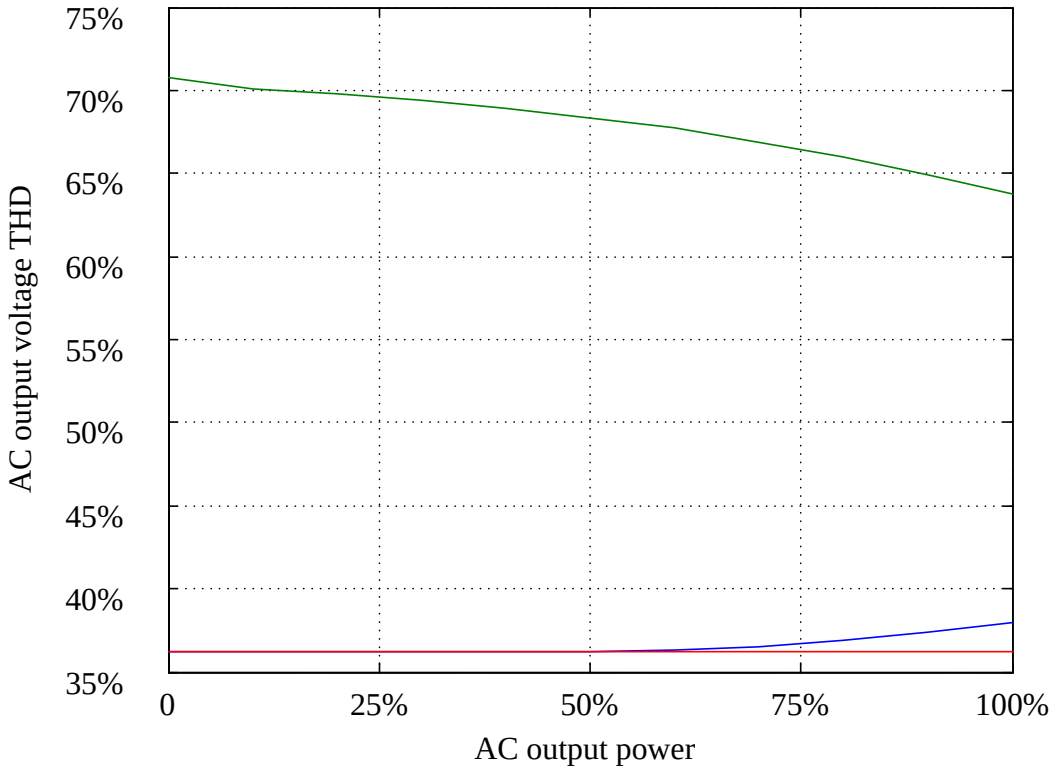


Figure 87: AC output voltage THD versus AC power with different interleaved PWM scheme: 0.7 power factor inductive load.

Figure 88, Figure 89, Figure 90, Figure 91, Figure 92, and Figure 93 show the FFT analysis of AC output voltage with different PWM scheme. The switching frequency is 216 kHz. It can be seen that the enhanced phase-shift PWM carrier scheme significantly reduced the magnitude of low frequency components of AC output voltage, which will reduce the EMI filter size

significantly.

FFT analysis of PWM scheme using carriers with 180 ° phase shift shows that the worst case happens with inductive load and the line-to-line voltage has a 120-V component of double switching frequency (432 kHz); FFT analysis of PWM scheme using carriers with 90 ° phase shift shows that the worst case happens with capacitive load and the line-to-line voltage has a 50-V component of switching frequency (216 kHz); FFT analysis of PWM scheme using two sets of carriers shows that the worst case happens with resistance load and the line-to-line voltage has a 60-V component of four times of switching frequency (864 kHz).

The peak component of output AC voltage of PWM scheme using two sets of carriers happens at much higher switching frequency than the PWM schemes with 90 ° phase shift and has much lower magnitude than the PWM schemes with 180 ° phase shift. Therefore, the EMI filter size can be significantly reduced.

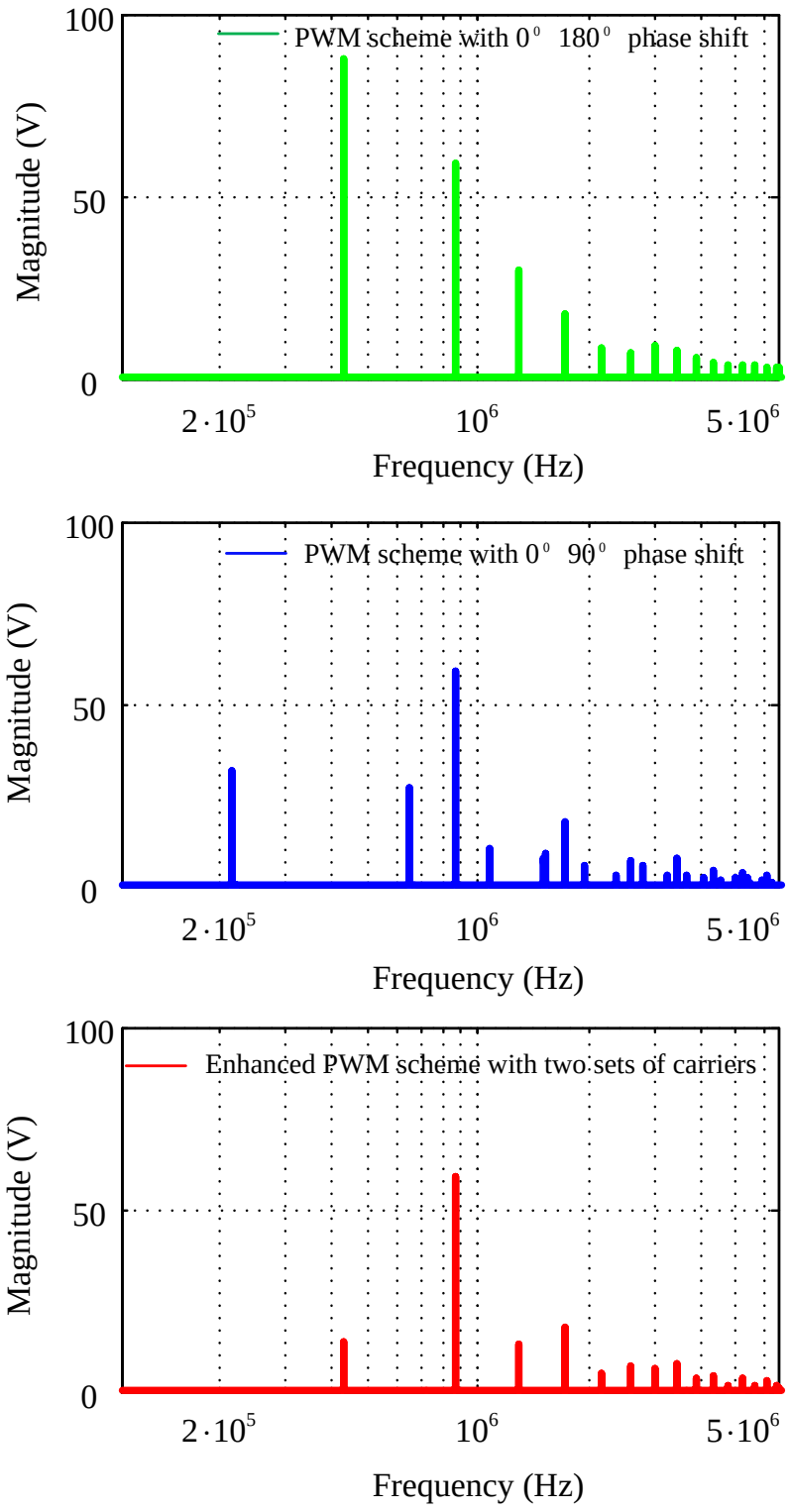


Figure 88: FFT analysis of AC output voltage with different interleaved PWM scheme: unity power factor resistance full load.

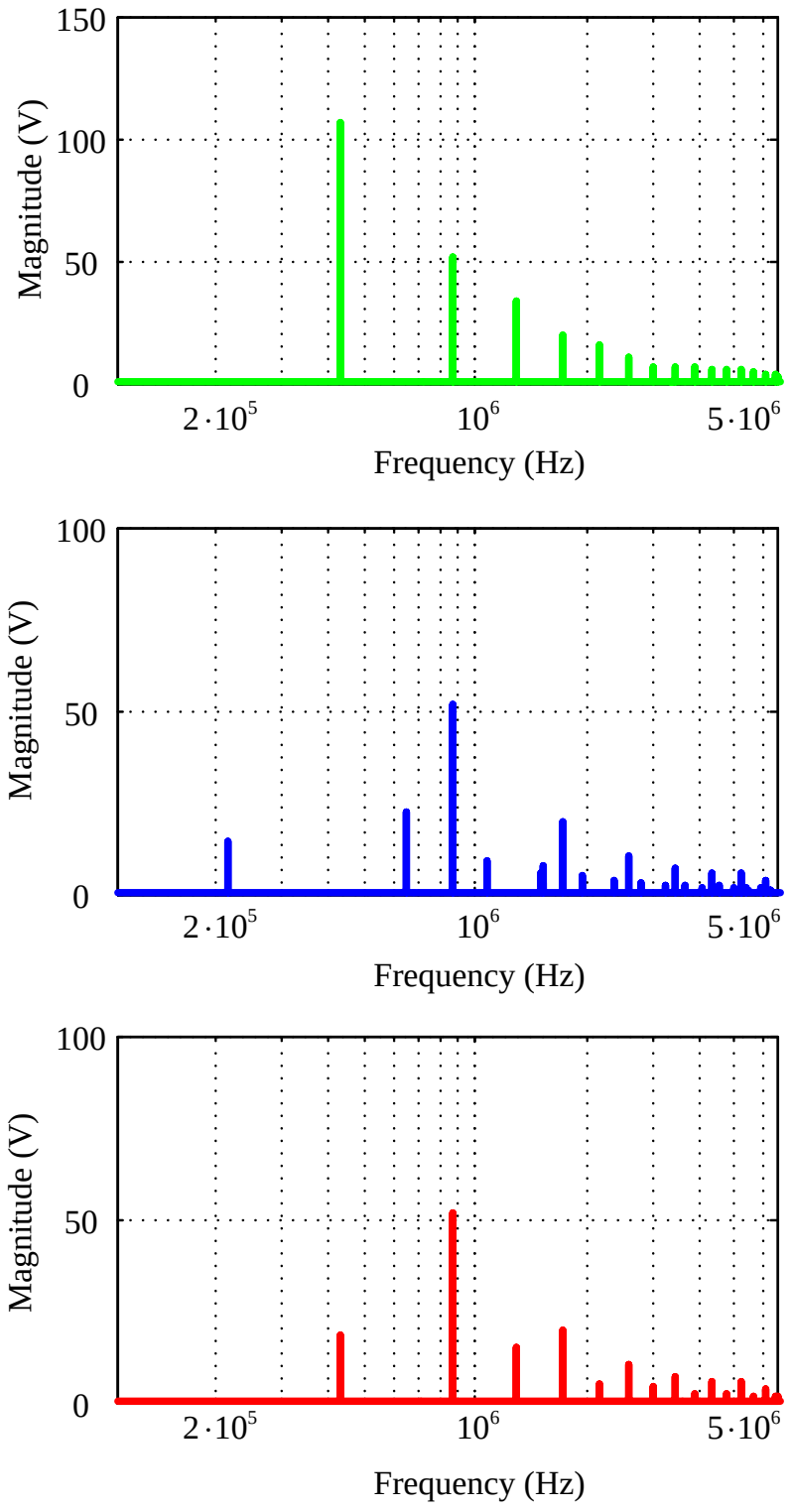


Figure 89: FFT analysis of AC output voltage with different interleaved PWM scheme: unity power factor resistance half load.

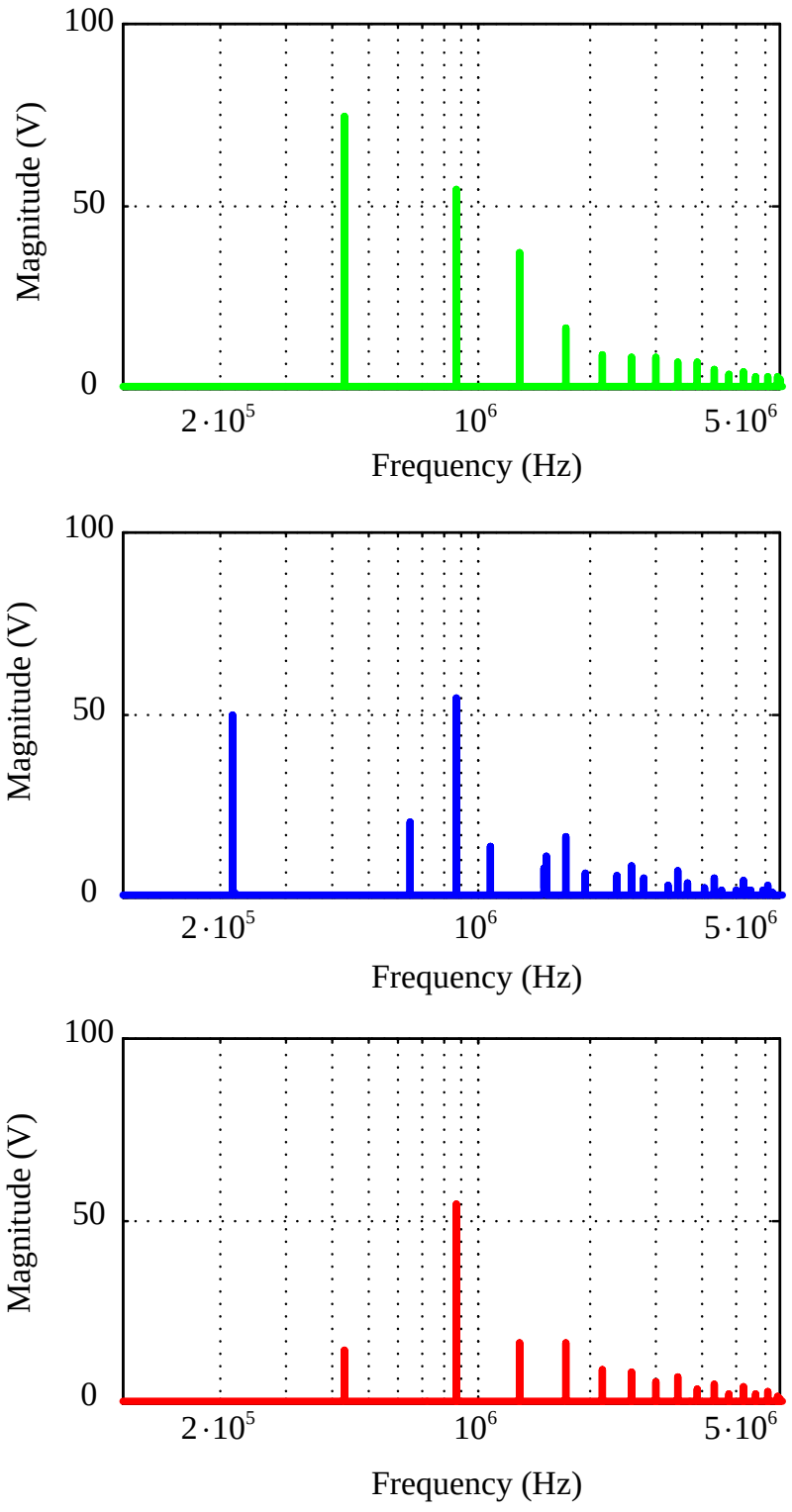


Figure 90: FFT analysis of AC output voltage with different interleaved PWM scheme: 0.7 power factor capacitive full load.

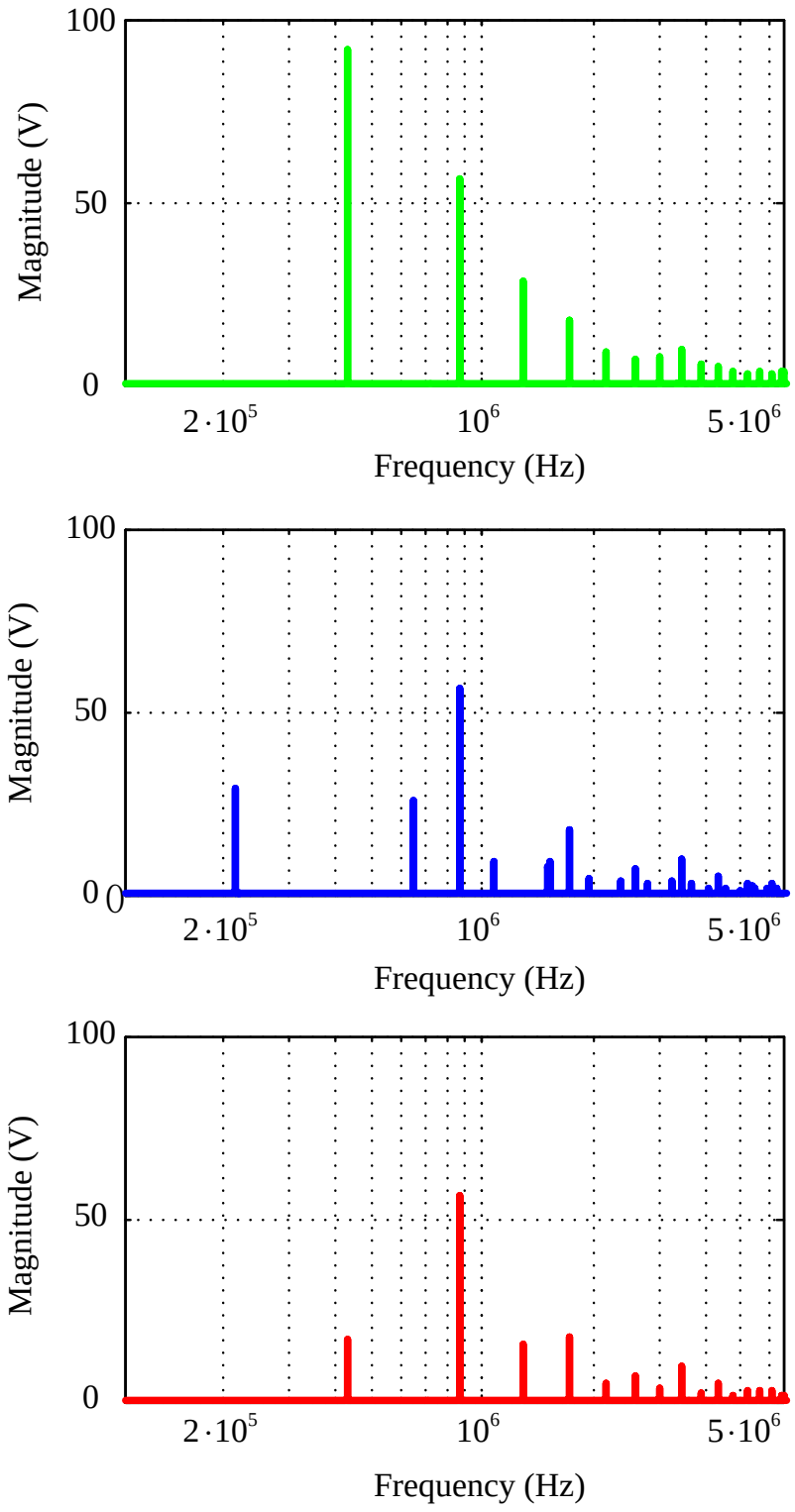


Figure 91: FFT analysis of AC output voltage with different interleaved PWM scheme: 0.7 power factor capacitive half load.

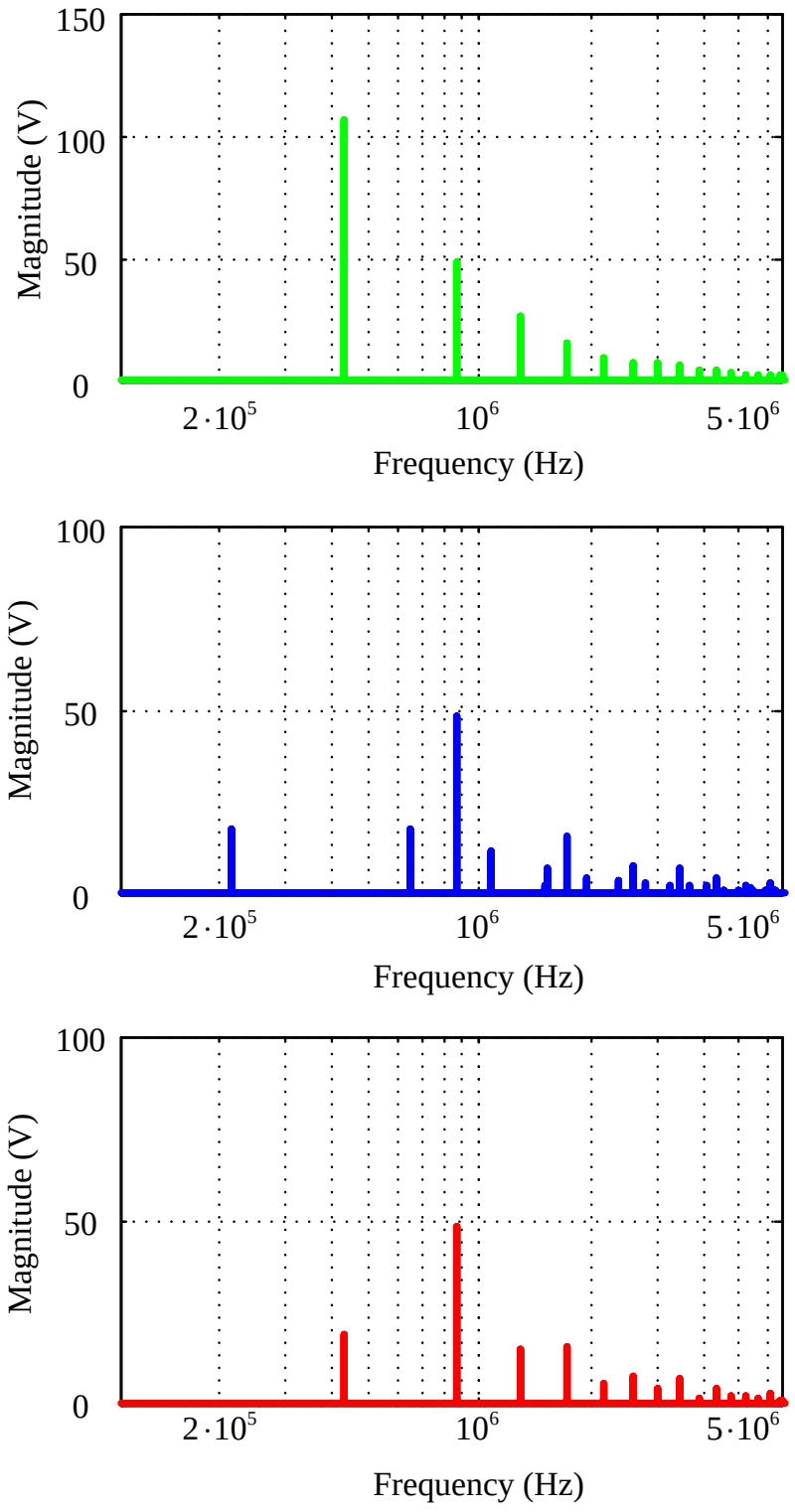


Figure 92: FFT analysis of AC output voltage with different interleaved PWM scheme: 0.7 power factor inductive full load.

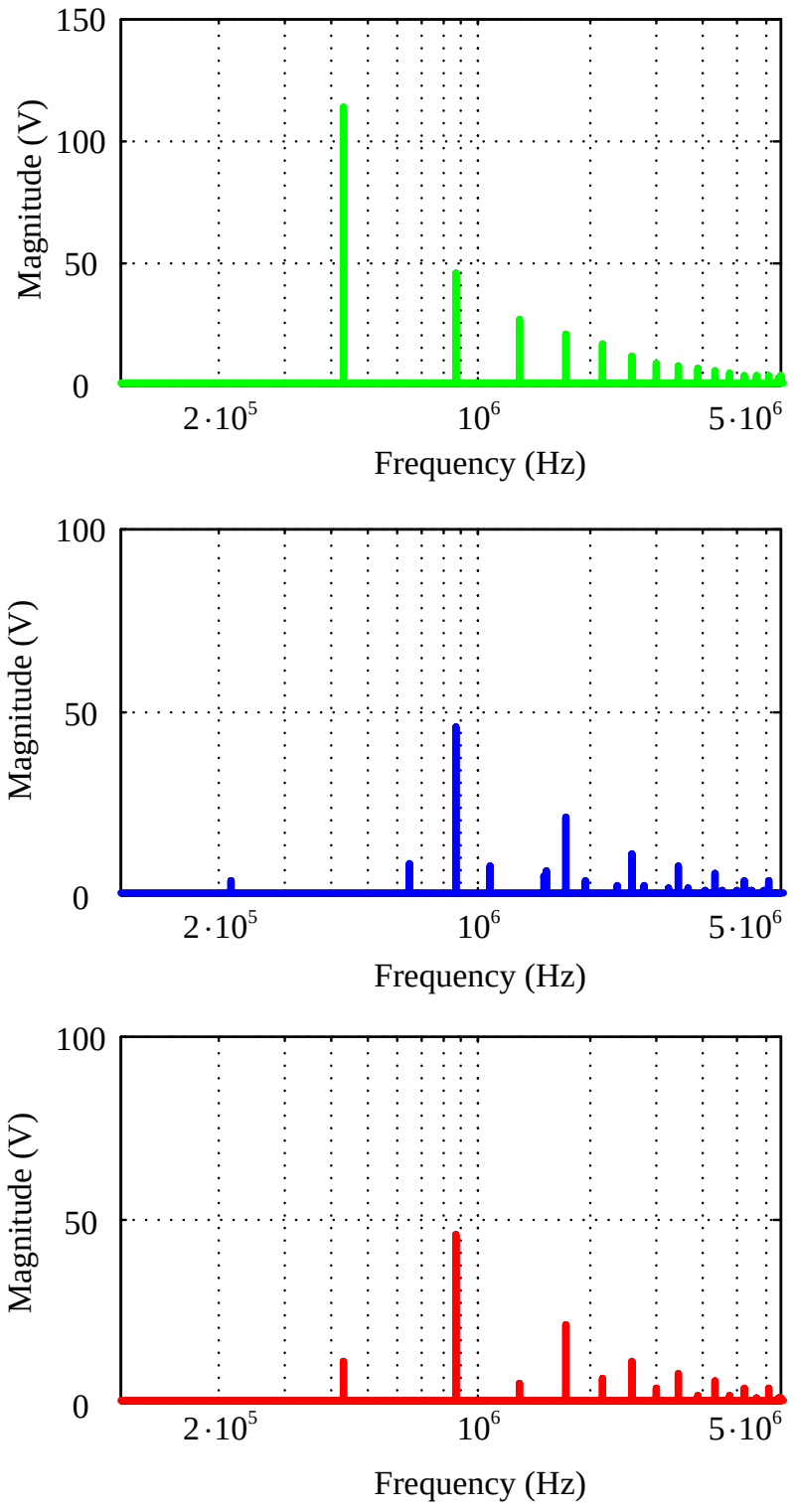


Figure 93: FFT analysis of AC output voltage with different interleaved PWM scheme: 0.7 power factor inductive half load.

6.3 Coupled inductor optimization

For paralleled inverter system, interleaving operation can reduce the overall input or output current ripple. However, interleaving operation will create significant circulating currents between the paralleled two phases [73, 74, 78, 80]. The inversely coupled inductors can substantially reduce the circulating current between the interleaved two phases.

A coupled inductor can be built to achieve the purpose of suppressing circulating current and filtering output current at the same time for each phase. The coupled inductor is equivalent to an inversely coupled transformer and two separated inductors shown in Figure 94.

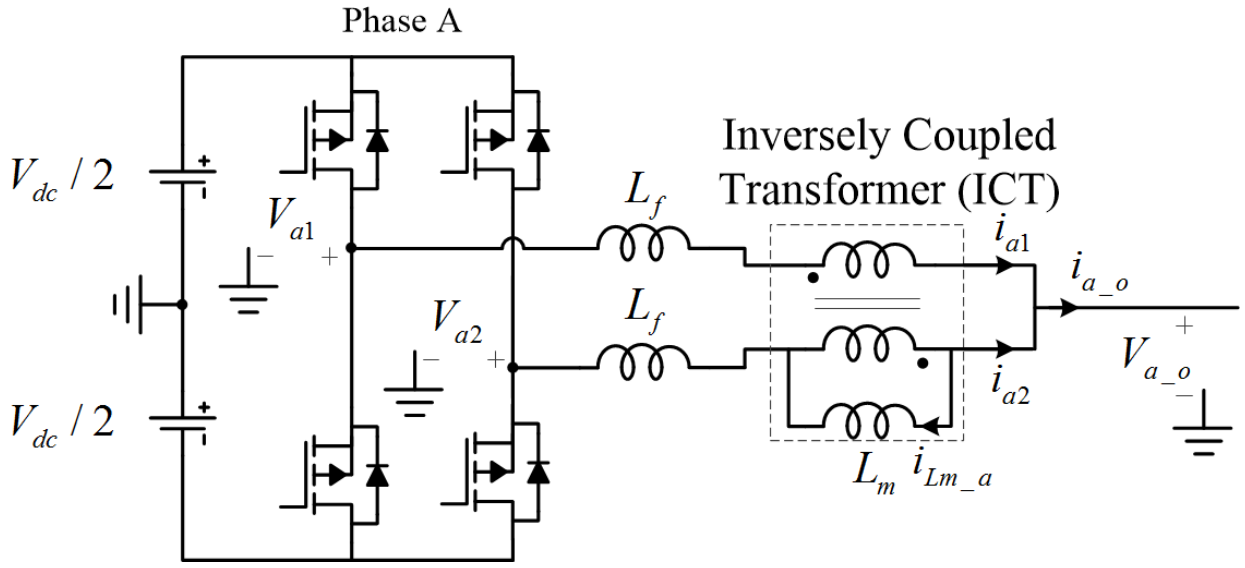


Figure 94: One phase leg with integrated coupled inductor.

The coupled inductor can be implemented by 4 U cores shown in Figure 95 [84]. The two inner U cores work together as inversely coupled transformer; while the two outer U cores work as two separated filtering inductors. By changing the airgap between the inner U cores and outer

U cores, the filtering inductance value can be adjusted.

For the proposed interleaved DC-capacitor-less inverter, each phase leg needs at least one coupled inductor. Since phase B both connected to AC output and AC capacitor, two separated coupled inductors for AC output and AC capacitor are needed in order to have symmetric output impedance of phase A and phase B, for better EMI design.

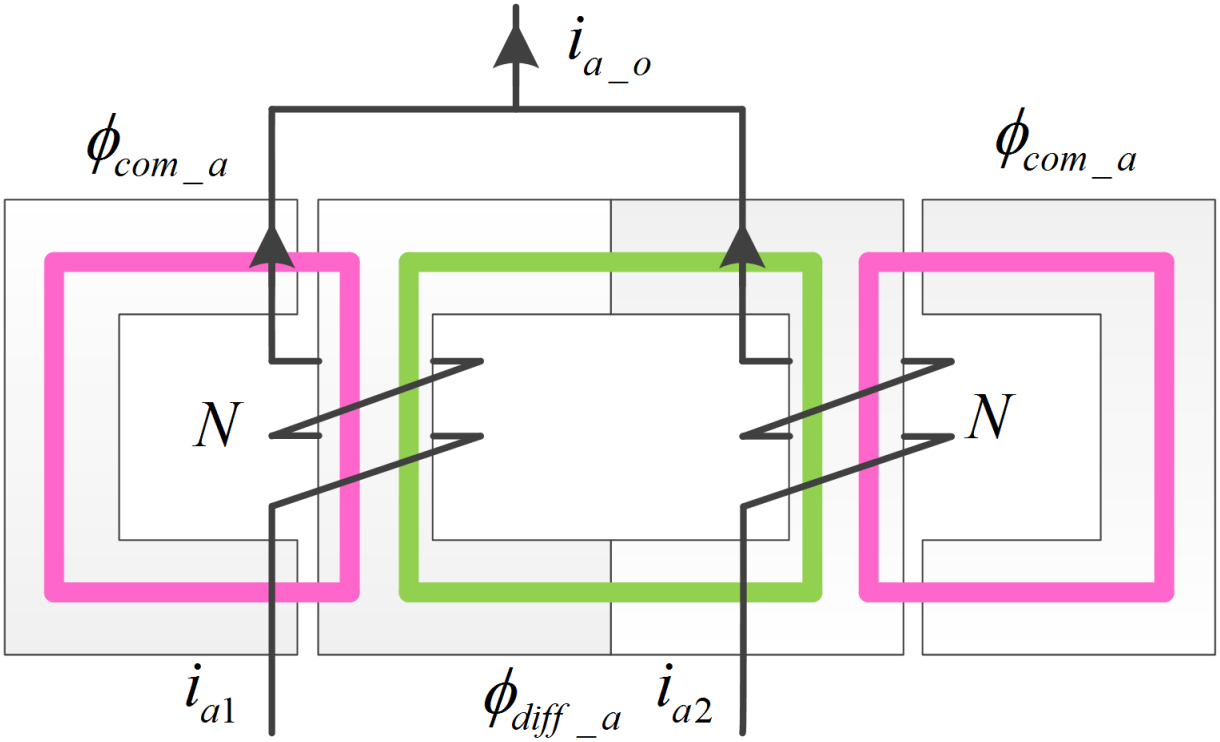


Figure 95: Coupled inductor implemented by 4 U cores.

Considering that the two coupled inductors of each pair for AC output and AC capacitor have the same current with reverse direction, the two coupled inductors of each pair can be further optimized to reduce the size and loss on magnetic components. The two coupled inductors can be combined together as one integrated coupled inductor as indicated by the dashed

box in Figure 72.

The currents through the inductors are split into common mode (CM) and differential mode (DM) components. The equivalent circuit of the integrated coupled inductor is shown in Figure 96.

Take phase A as an example, the current of each leg will be expressed by common mode current, i_{a_CM} and differential mode current, i_{a_DM}:

$$i_{a1}=0.5(i_{a\_CM}+i_{a\_DM}), \tag{5.55}$$

$$i_{a2}=0.5(i_{a\_CM}-i_{a\_DM}). \tag{5.56}$$

And the common mode current and differential mode current satisfy:

$$\frac{di_{a\_CM}}{dt}=\frac{L_{a1}+L_{a2}}{L_{a1}\cdot L_{a2}}\left(\frac{V_{a1}+V_{a2}}{2}-V_{a\_o}\right), \tag{5.57}$$

$$\frac{di_{a\_DM}}{dt}=\frac{1}{2M+L_{a1}+L_{a2}}(V_{a1}-V_{a2}). \tag{5.58}$$

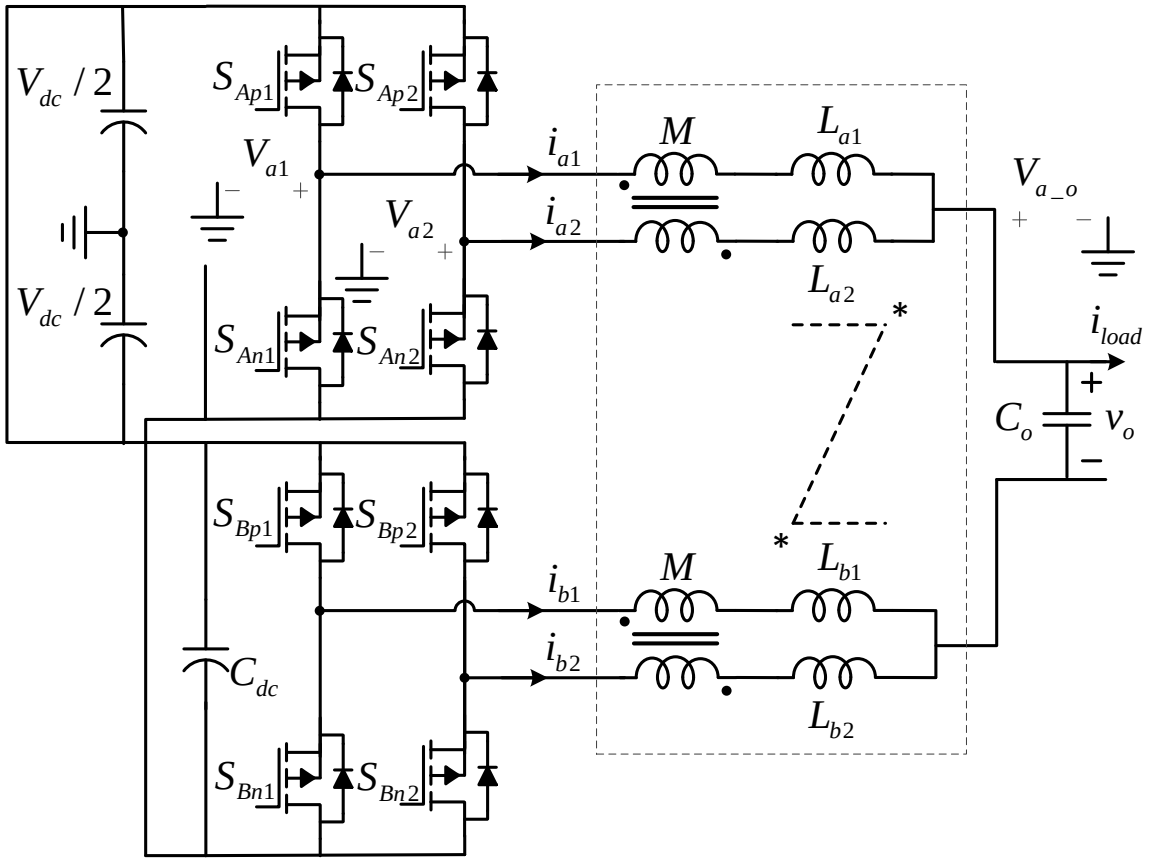


Figure 96: The equivalent circuit of coupled inductor.

The common mode current sees high impedance produced by the mutual inductor, *M*. The differential mode voltages, v_{x1}-v_{x2} (x=a, b) in phase A and B are shown Figure 84. When differential mode voltage is given, the larger differential mode inductance, *M*, the smaller differential mode current will be. The maximum differential mode peak current, i_{DM_max} can be calculated by:

$$i_{DM\_\max} = \frac{V_{dc}}{4 f_{sw}(2M + L_{x1} + L_{x2})} \ (x = a,b,c)\,. \tag{5.59}$$

The common mode current only sees impedance produced by L_{x1}, L_{x2}, (x=a, b, c). Take AC output voltage as example, the equivalent common mode filtering inductance is:

$$L_{f\_ab} = \frac{L_{a1} \cdot L_{a2}}{L_{a1} + L_{a2}} + \frac{L_{b1} \cdot L_{b2}}{L_{b1} + L_{b2}}. \tag{5.60}$$

The maximum common mode current is determined by the load current and output ripple current. Considering the dynamic response, the allowed maximum common mode current, i_{CM_max} is designed to be 125% of the maximum load current.

In order to reduce the size of coupled inductor, a new structure of integrated coupled inductor is proposed. The 3D structure of the integrated coupled inductor and the differential mode and common mode flux paths are shown in Figure 97 and Figure 98 respectively.

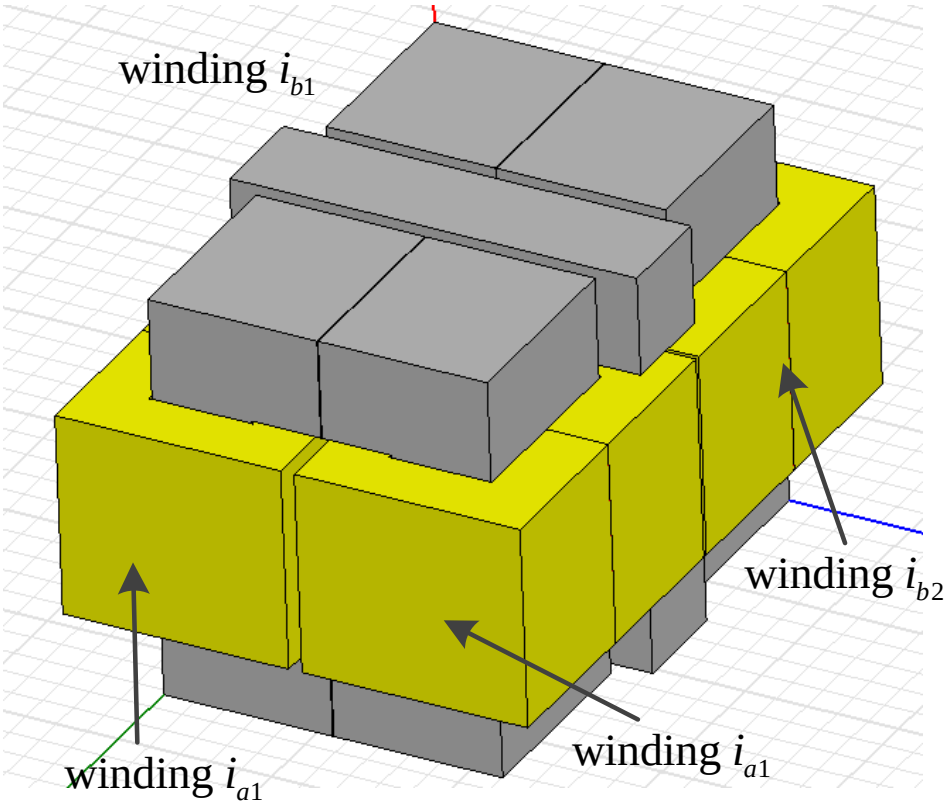


Figure 97: 3D structure of the integrated coupled inductor.

The proposed integrated coupled inductor has 4 U cores and 2 I cores. As it shown in Figure

98, two pairs of U cores without air-gap generate the high impedance of differential mode mutual inductor, *M*. I cores and U cores generated the common mode inductance for output current filtering. The air-gaps between I core and U core can be adjusted to change the output filtering inductance.

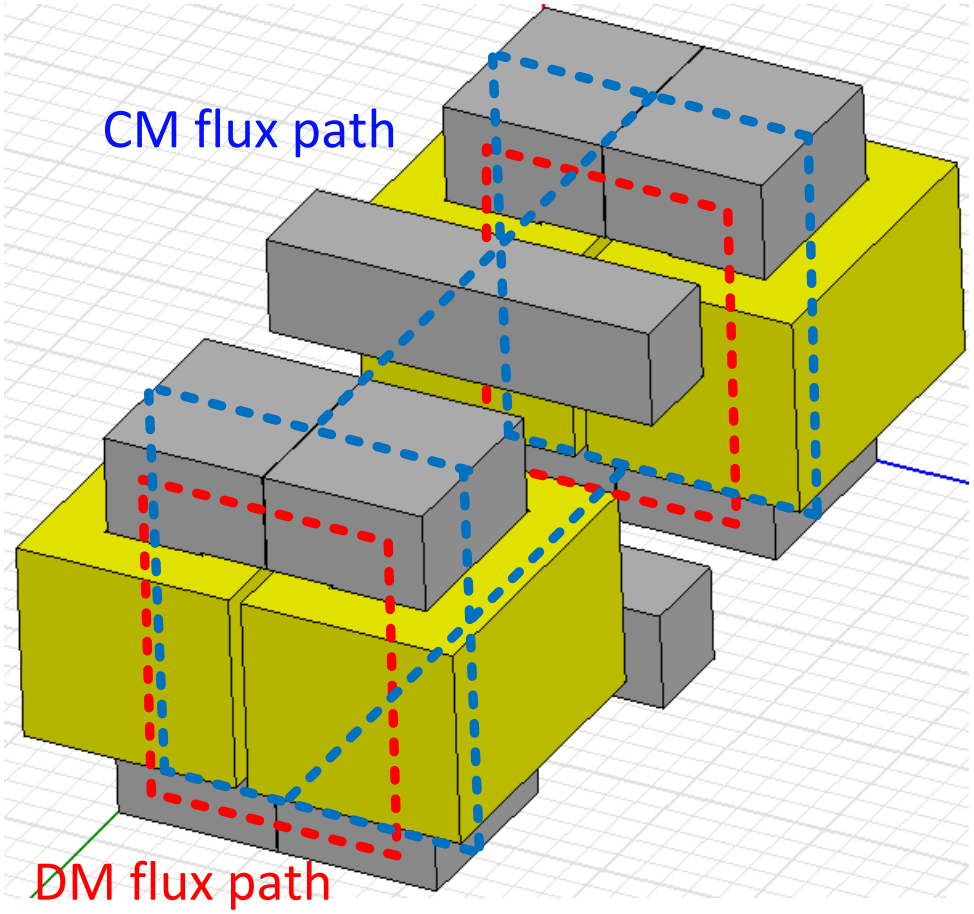


Figure 98: Differential mode (DM) and common mode (CM) flux path of integrated coupled inductor.

The comparison between two separated coupled inductors [84] and proposed integrated coupled inductor is shown in Figure 99. The dimension of proposed integrated coupled inductor

is 43mm × 30mm × 26.5mm (x, y, z), while the dimension of the two separated coupled inductors is 43mm × 46mm × 26.5mm (x, y, z). Since the proposed integrated coupled inductor adopts I cores to generate the output filtering inductor instead of the outer U cores for output filtering inductor in separated coupled inductor. As a result, the total volume of proposed integrated coupled inductor is only 65% of the volume of two separated coupled inductors.

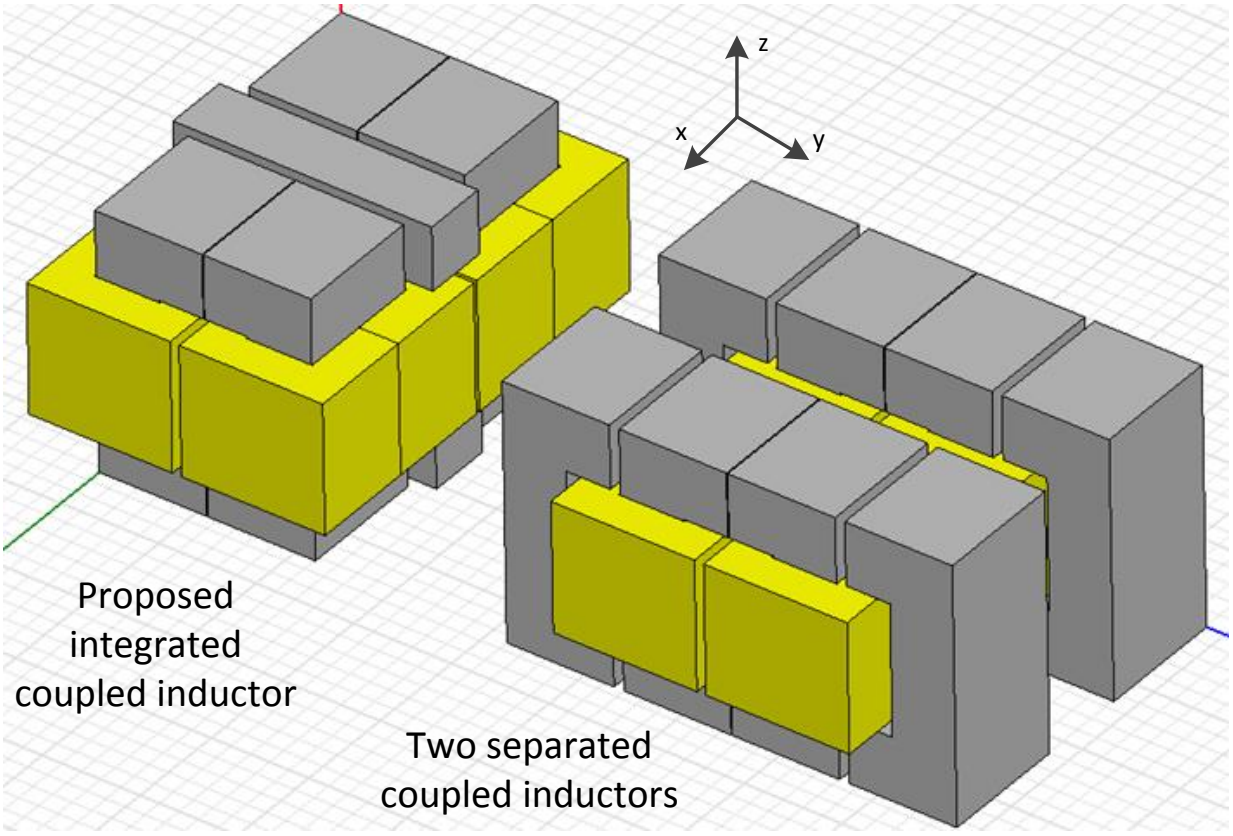


Figure 99: Comparison between two separated coupled inductor [84] and proposed integrated coupled inductor

For integrated coupled inductor design, the number of turns is designed to be 23; the differential mode inductance and common mode inductance are designed to be:

$$M = 500\ \mu H,$$
$$L_{a1} = L_{a2} = L_{b1} = L_{b2} = 50\ \mu H. \tag{5.61}$$

The maximum flux density happens when the differential mode current and the common mode current both reach the maximum value. Figure 100 shows the simulation results of integrated coupled inductor and Figure 101 shows the simulation results of separated coupled inductors.

For the proposed integrated coupled inductor, when i_{DM_max} = 0.4 A and i_{CM_max} = 10 A, the maximum flux density reaches 0.4 T for ferrite core, indicating that the integrated coupled inductor design is proper. Since the differential mode and common mode fluxes superimpose on C shape core legs, the flux density for each leg is different. For the leg where differential mode and common mode fluxes have the same direction, the flux density reaches the maximum value, while for the leg where differential mode and common mode fluxes have different directions, the fluxes are partially cancelled and the flux density is smaller.

For two separated coupled inductor design, the same number of turns is used. Based on the simulation results, the inner U cores' flux distribution is very similar to integrated coupled inductor. The flux density of outer U cores is also similar to I cores in the integrated coupled inductor, however with much larger size. In other words, the core loss of I core in integrated coupled inductor is smaller. In conclusion, the proposed structure of coupled inductor greatly reduces the magnetic components' size with lower core loss.

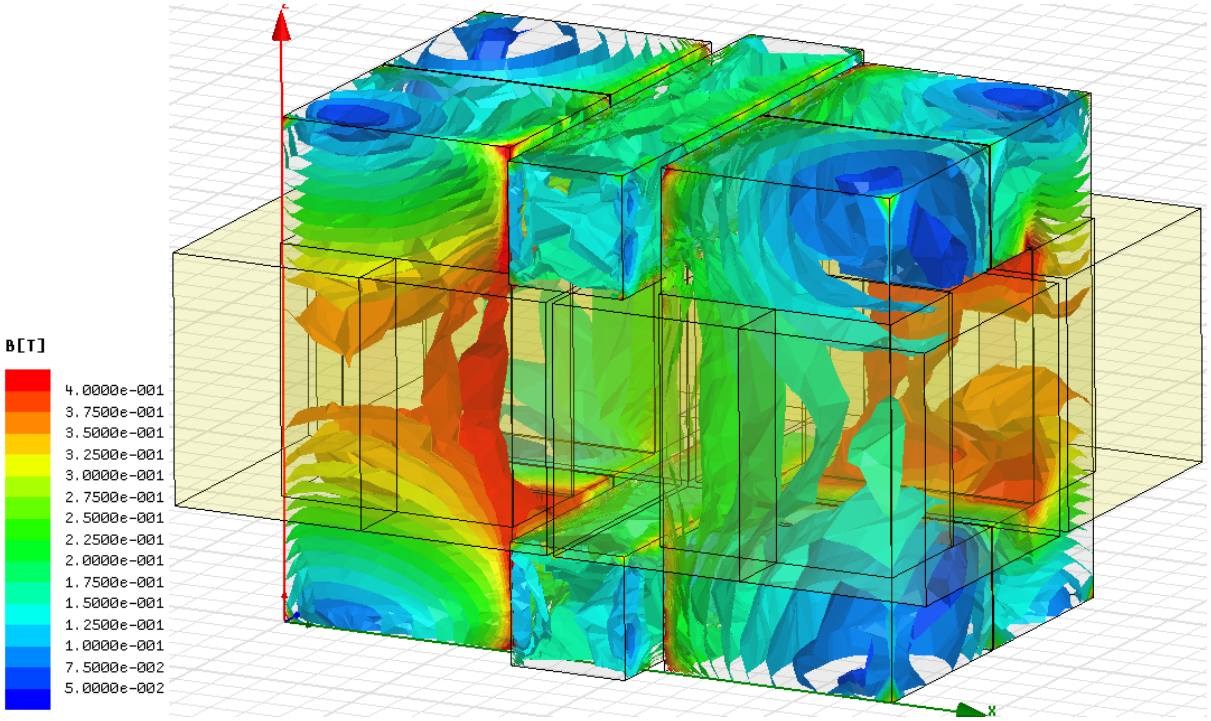


Figure 100: Simulation result of the integrated coupled inductor.

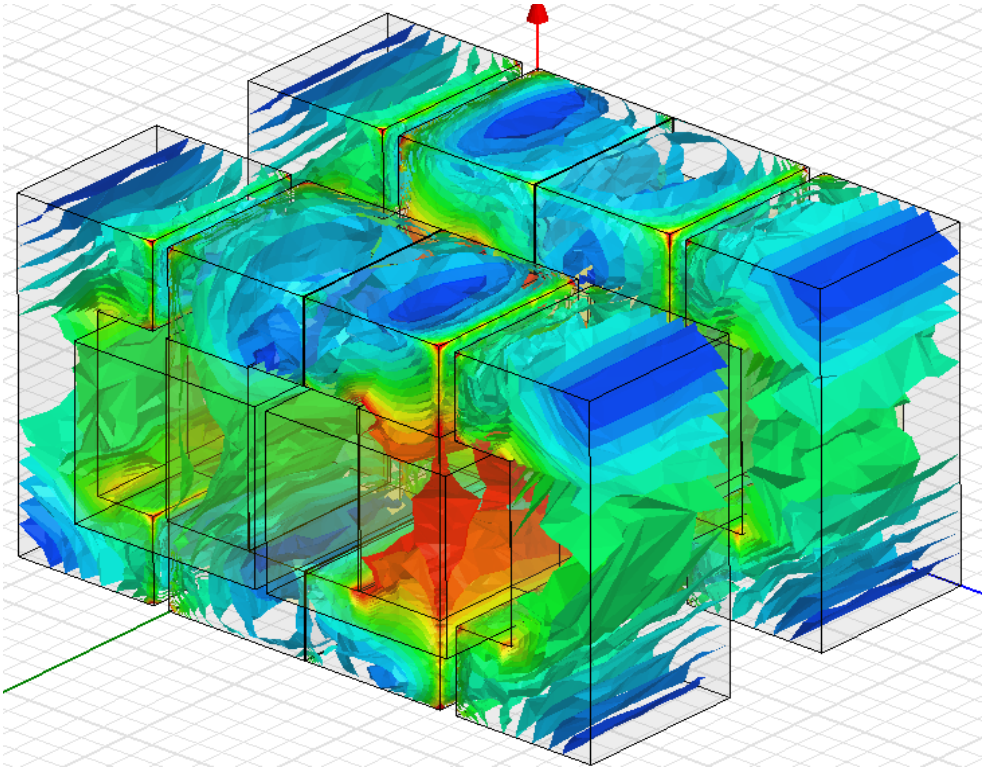


Figure 101: Simulation result of two separated coupled inductors.

6.4 Experimental results

The key parameters for the 2-kW inverter system are listed below in Table II. The SiC MOSFETs from Cree (C2M0160120D) are used for the inverter.

For conventional H-bridge system, if the allowed DC voltage ripple is 2.5%, the DC capacitance is 2 mF (20 pu). By using the proposed inverter system, the DC capacitor is 20 μF (0.2 pu), and the AC capacitor is 100 μF (1 pu). Compared to conventional H-bridge system, the total size of the capacitor (including DC capacitor and AC capacitor) is reduced by 16 times.

Table 7: Key parameters for 2-kW single phase inverter.

DC capacitance, C_{dc}	20 μF (0.2 pu)
switching frequency, f_s	216 kHz
AC capacitance, C_{ac}	100 μF (1 pu)
Resistance load	28.8 Ω resistor
Capacitive load	20 Ω resistor in series with 65 μF capacitor
Inductive load	20 Ω resistor in series with 50 mH inductor

Figure 102 shows the equivalent line to line voltages, which switches only between adjacent levels. The voltage waveforms are consistent with the theoretical analysis.

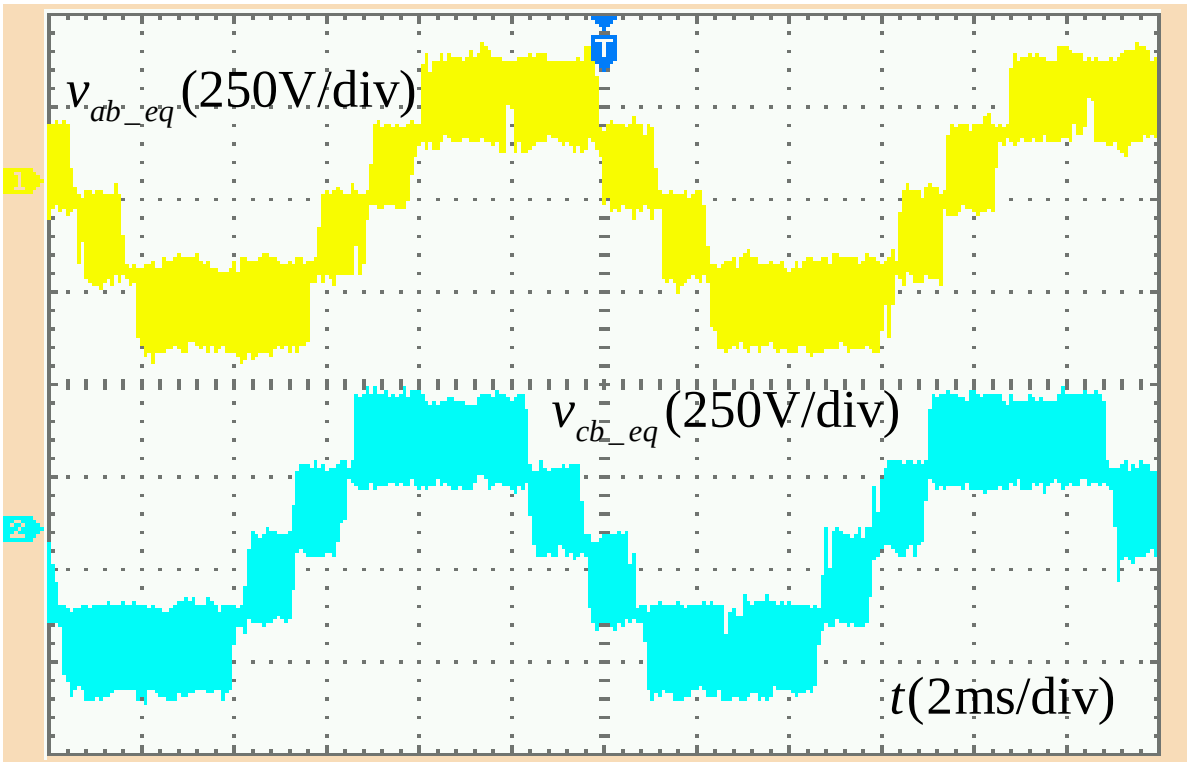


Figure 102: Equivalent line to line voltage of proposed inverter.

Figure 103 shows the current sharing experimental waveforms of phase A. The current difference between two channels is within 1A (less than 5% of peak-to-peak full rated current), indicating that the integrated coupled inductor has effectively suppressed the circulation current.

Figure 104, Figure 105, and Figure 106 show experimental waveforms at full load with different power factors. For unity power factor load, 28.8-Ω resistance load is used. 20-Ω resistor in series with 65-μF capacitor is used for 0.7 leading power factor load, and 20-Ω resistor in series with 50-mH inductor is used for 0.7 lagging power factor load. The experimental waveforms of AC output voltage and AC capacitor voltage/current are consistent with the theoretical analysis.

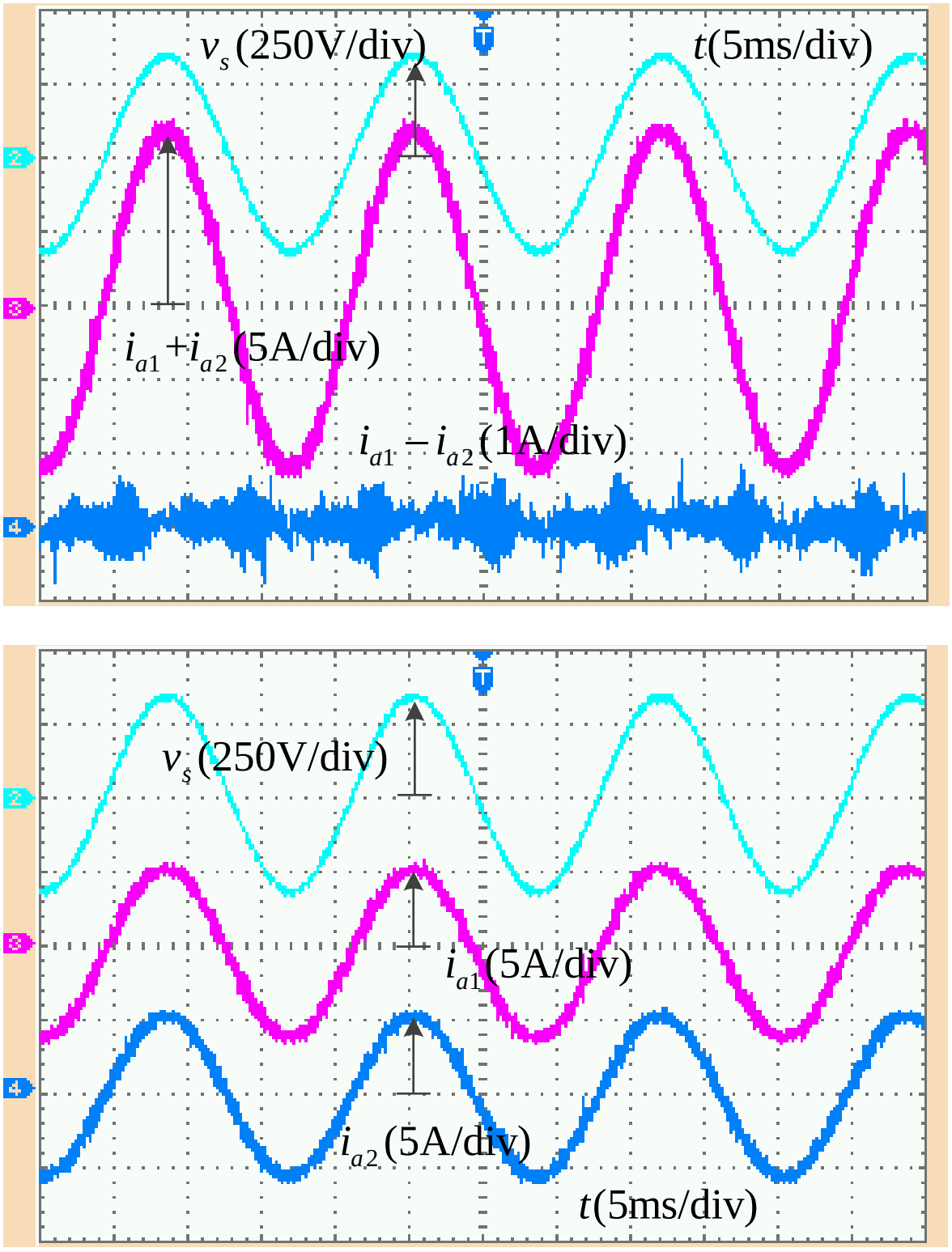


Figure 103: Current sharing waveforms of phase A.

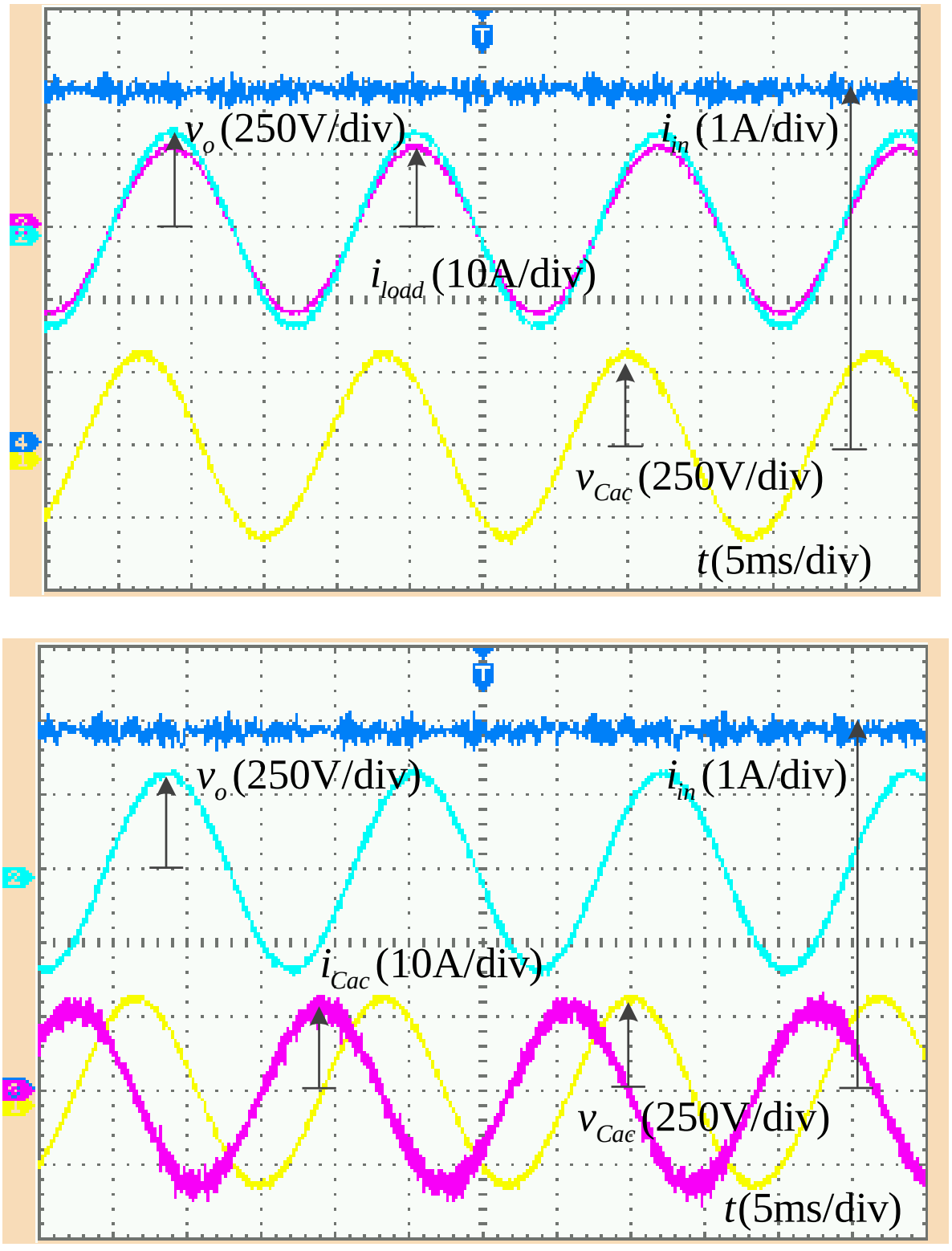


Figure 104: Full load experimental waveforms of proposed inverter system with unity power factor resistance load.

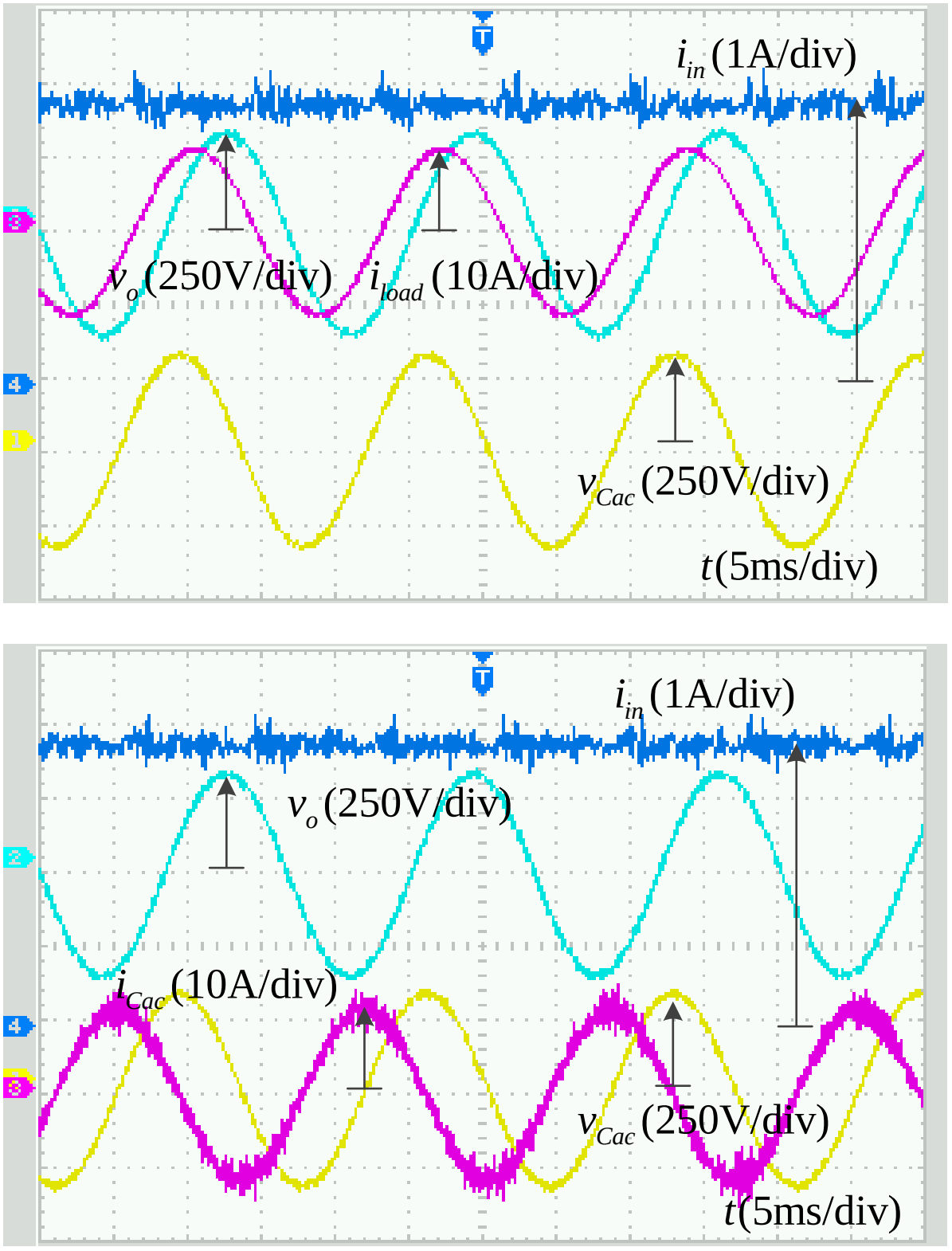


Figure 105: Full load experimental waveforms of proposed inverter system with 0.7 power factor capacitive load.

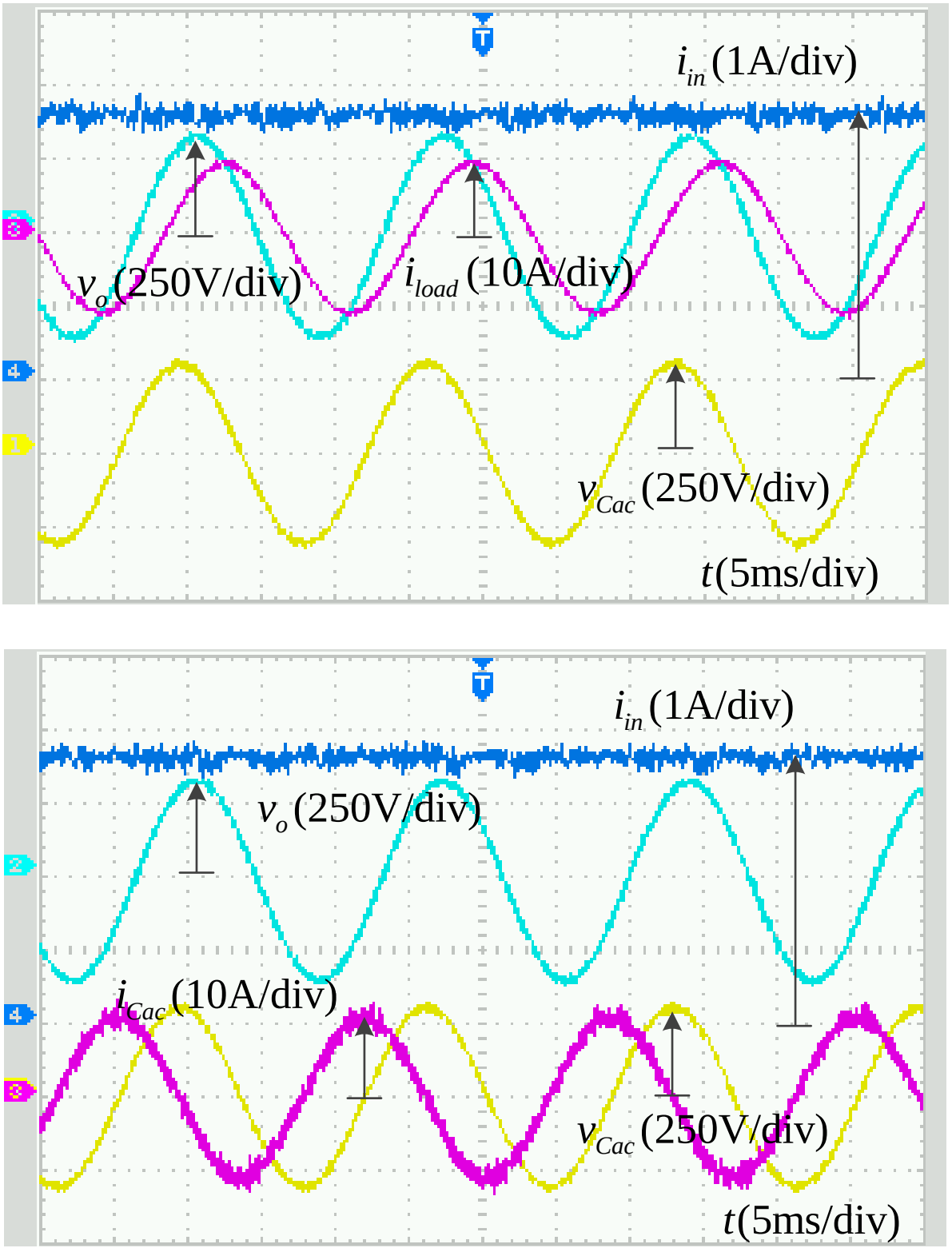


Figure 106: Full load experimental waveforms of proposed inverter system with 0.7 power factor inductive load.

In the experiment, an ideal DC voltages source in series with a 10-Ω resistor is used as the input of the inverter. As is shown in Figure 104, Figure 105, and Figure 106, The DC input current ripple for different load cases is within 0.5 A. In other words, the DC ripple voltage is within 5 V (1.25% of rated input DC voltage), indicating that the AC capacitor has effectively absorbed the 2ω ripple power.

6.5 Conclusions

An interleaved DC-capacitor-less inverter with SVPWM is proposed for inverter application with different power factor. The proposed interleaved DC-capacitor-less single-phase inverter significantly reduces the total capacitor size by 16 times to achieve high power density with switching frequency of 216 kHz.

The DC voltage requirement for different load is analyzed to show that the proposed interleaved DC-capacitor-less inverter with SVPWM can operate with the input DC voltage source. The proposed system shows best performance among existing methods in energy requirement of capacitor and total device power rating. The adoption of the enhanced phase-shift interleaved PWM scheme effectively improves the THD of inverter output voltage. A detailed analysis is provided to compare the performance of enhanced phase-shift interleaved PWM scheme for different power factors. For the interleaved structure, a new structure of integrated couple inductors is proposed to suppress circulating current between the two parallel inverters and to filter output current at the same time. The volume of integrated coupled inductor is reduced by 35% compared with the design of two separated coupled inductors. The 3D structure and flux path are analyzed to verify the integrated coupled inductor design.

The simulation and experiment have verified the theoretical analysis and the effectiveness of the proposed interleaved DC-capacitor-less inverter.

CHAPTER 7 DEVELOPMENT OF HIGH SWITCHING FREQUENCY INTERLEAVED DC-CAPACITOR-LESS INVERTER WITH SIC MOSFETS

In order to achieve inverter system with high power density, high efficiency and high reliability, SiC MOSFETs are adopted to achieve 216-kHz switching frequency. The size of filtering components including DC input filtering capacitors and AC output LC filter can be significantly reduced.

However, the high switching frequency operation of SiC MOSFETs requires careful design of gate driver and PCB layout to fully utilize the advantages of SiC MOSFETs. In addition, since the digital controller's computation capability is limited, it is very critical to optimize DSP control programming to implement SVPWM control, ripple power compensation and interleaved PWM scheme. As a result, the system can achieve 96% efficiency at full load and good dynamics response to meet the control requirement for the proposed interleaved DC-capacitor-less inverter system.

7.1 Silicon Carbide power devices

Wide band gap (WBG) semiconductors such as SiC and GaN, with high breakdown electric field, low carrier concentration and high thermal conductivity, have drawn significant research interests in recent years. Compared to silicon semiconductors, WBG semiconductor's high breakdown field enables thinner high-voltage devices and lower conducting loss. The low carrier

concentration facilitates faster tum-on capability and lower switching losses. The high thermal conductivity enables improved reliability and higher temperature operation capability. [85-93]

Table 8 shows the comparison of the properties of Si and SiC.

Table 8: Comparison of the properties of Si and SiC.

Parameter	Si	4H-SiC
Bandgap energy (eV)	1.1	3.3
Relative permittivity (MV/cm)	11.8	10
Critical electric field	0.3	2.0
Electron saturated drift velocity ($\times 10^7$cm/s)	1.0	2.0
Thermal conductivity (W/cm·K)	1.5	4.9

For high voltage and high power applications, SiC Schottky diodes (SBDs) and MOSFETs are competitive candidates to replace Si diodes and IGBTs respectively. SiC SBDs are now commercially available up to 1700 V. The main advantage of a high-voltage SiC SBD lies in its extremely low reverse-recovery charge (Q_{rr}). Currently, Cree's latest C2M1000170J (1700V, 3.6A) can achieve 1-Ω $R_{ds(on)}$ with 24-nC Q_{rr}. The superior dynamic performance of SiC DBDs can significantly reduce switching losses in a typical hard-switched IGBT/MOSFET based application such as motor-drive inverters and uninterruptible power supplies (UPS) [94-97].

Compared to Si IGBTs/MOSFETs, SiC MOSFETs have much lower conducting losses, and higher ruggedness. SiC MOSFETs can operate reliably up to junction temperatures of 200 ^{0}C. SiC MOSFETs can achieve much faster turn-on/off speed, which allows very high switching frequency operation. The switching frequency of 1200-V SiC MOSFETs can be boosted up to

50-200 kHz. The combination of SiC SBDs and MOSFETs will save approximately 60-80% of switching losses resulting in an efficiency improvement of 4-6% points in a typical power electronic system. In addition, cooling requirements will be substantially reduced in direct proportion to the reduction in losses [98]. Now, 1200-V/300-A SiC MOSFETs module with SiC SBD is available in market.

By upgrading the system with SiC devices, the interleaved DC-capacitor-less inverter system can achieve much higher power density, efficiency and reliability. First, SiC devices enable a much higher switching frequency of the system to minimize the filtering inductors and capacitors, further improving the power density. Second, as the SiC devices have lower conducting and switching losses, and higher temperature operation capability, the SiC-based single phase inverter system will be more efficient and reliable than Si-based system.

For the 2-kW inverter system, 1200-V SiC MOSFETs from Cree (C2M0160120D) with 160-mΩ R_{dson} are adopted [99].

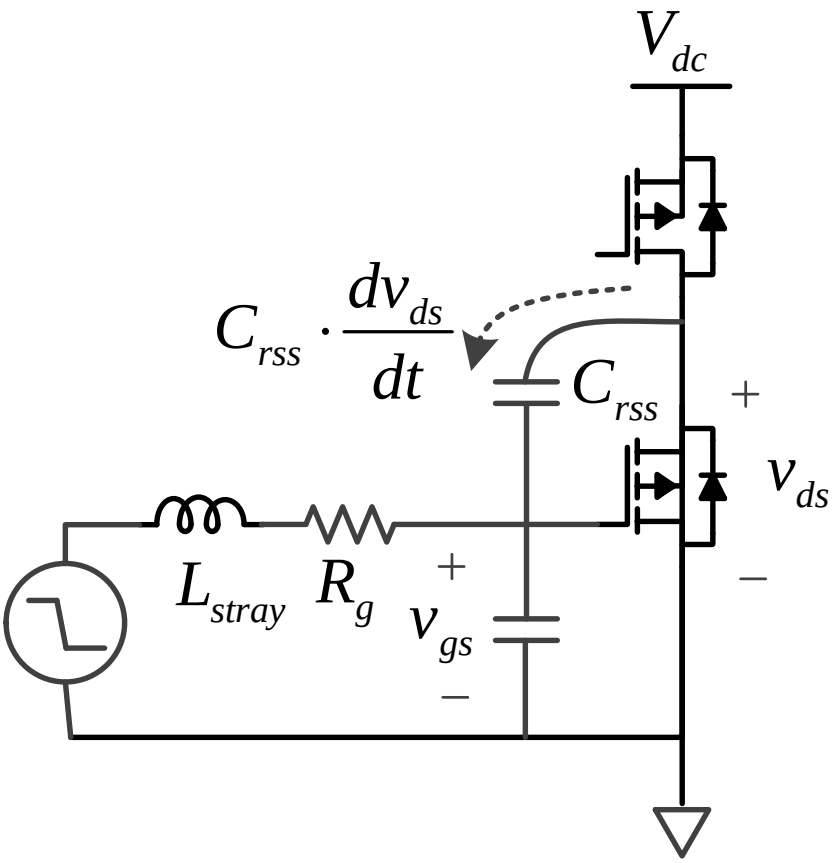
7.2 PCB layout design and optimization

Since the SiC MOSFETs are switching at very high frequency (216 kHz) and has very fast turn-on/off speed, which results in very high dv/dt and di/dt. It is very important to carefully design the inverter's PCB layout including gate driver, power supply and DC voltage bus bar.

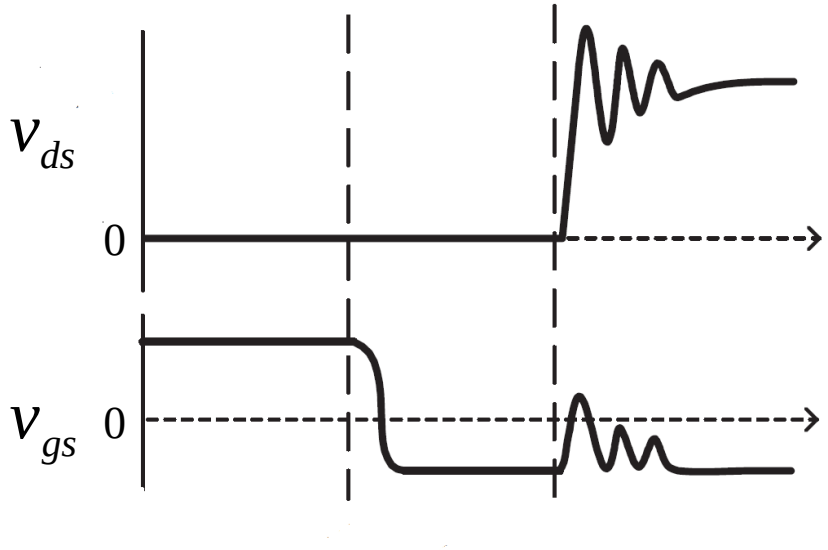
In order to reduce the switching loss of SiC MOSFETs, the typical turn-on and turn-off time of the SiC MOSFETs is around 10~15 ns. For DC-capacitor-less inverter, the fast turn-on/off speed will cause very high dv/dt, when the MOSFETs are working under hard switching.

Figure 107 shows the v_{gs} voltage spike caused by miller effect during turn-off transition. In

scenario of top MOSFET hard switching, after bottom MOSFET turn-off, the current will freewheel through body diode of bottom MOSFET. During a very short dead time period, both top and bottom MOSFETs are off. After that, the top MOSFET turns on; and a non-negligible amount of displacement current flows through the reverse miller capacitance C_{rss} due to the quick voltage change, *dv/dt* across the drain to-source terminals. The displacement current, that is, $C_{rss} \cdot dv_{ds} / dt$, flows into the bottom MOSFET input capacitance C_{iss}. Since the parasitic inductor, L_{stray} is in series to the gate terminal, a voltage fluctuation is induced in the bottom MOSFET gate-to-source voltage v_{gs}. The voltage fluctuation caused by L_{stray} may falsely turn on the bottom MOSFET again irrespective of the gate control signal if the voltage fluctuation reaches the MOSFET threshold voltage [100-102].



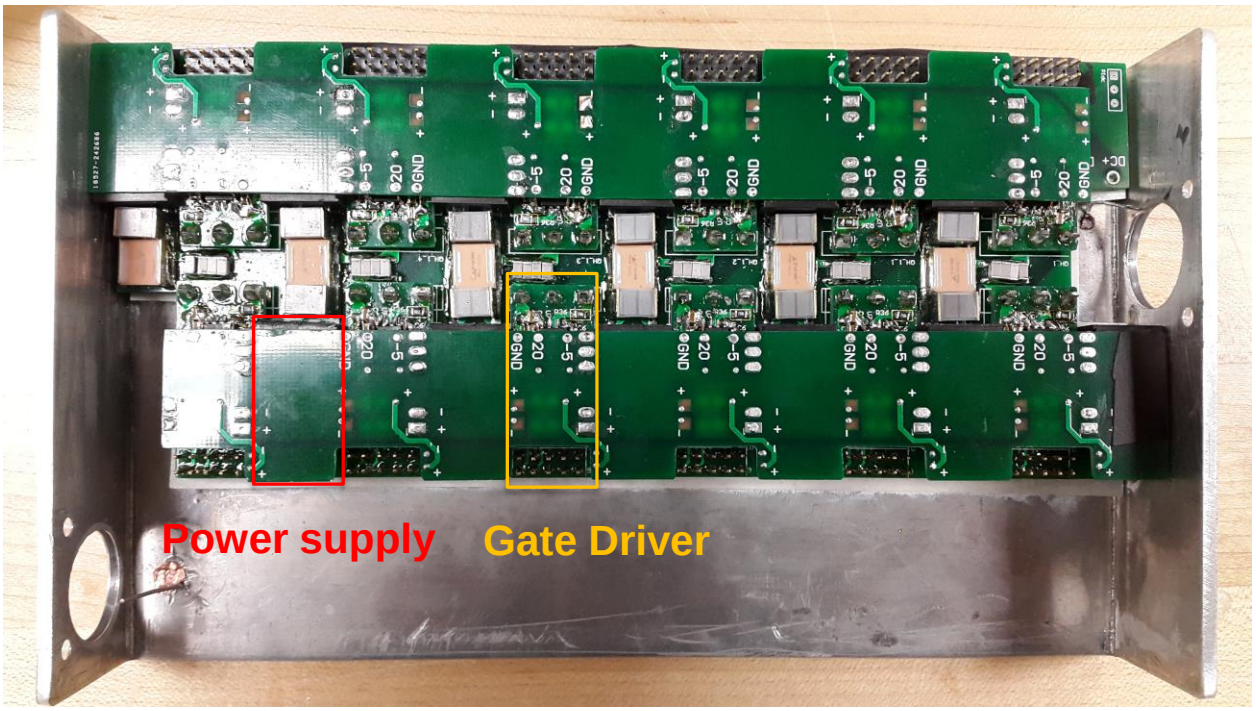
(a)



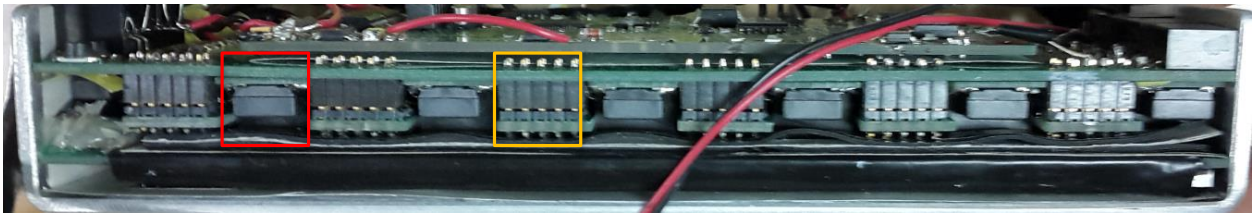
(b)

Figure 107: V_{gs} voltage spike caused by miller effect during turn-off transition.

Therefore, it is very critical to reduce the stray inductance in gate driver loop. The 3D layout of gate driver and power supply is optimized to minimize the gate driver loop and to achieve a compact system. Figure 108 shows the gate driver and power supply layout. In this design, the gate driver board for each MOSFET is directly mounted to the MOSFET pins to minimize the stray inductance in gate driver loop



(a) Top view



(b) Side view

Figure 108: Gate driver and power supply layout with top view and side view.

To further reduce the risk of false turn-on of MOSFET, negative 5 V is adopted for turn-off gate driver voltage. Since the gate driver loop is minimized, external turn-on gate resistor is designed to be 2 Ω and external turn-off gate resistor is designed to be 0 Ω to achieve fast turn-on/off and low switching loss.

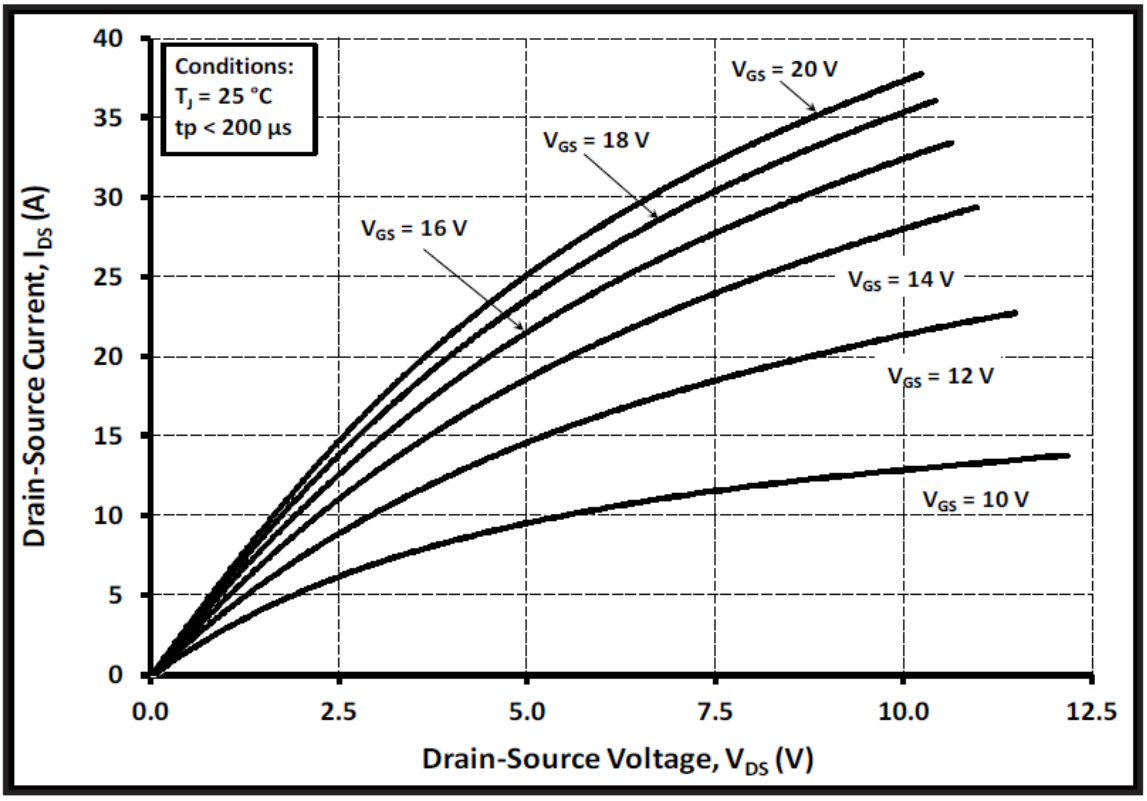


Figure 109: SiC MOSFET output charateristic [99].

Since the drain-source on-state resistance of SiC MOSFET (R_{dson}) shows a stronger correlation with gate drive turn-on voltage. Figure 109 shows the SiC MOSFET (C2M0160120D) output characteristics under 25^0C junction temperature [99]. The R_{dson} at 12-V turn-on voltage can be larger than two times of the R_{dson} at 20-V turn-on voltage. In order to obtain the best R_{dson} performance and lowest conduction loss, positive 20 V is adopted for turn-on gate driver voltage.

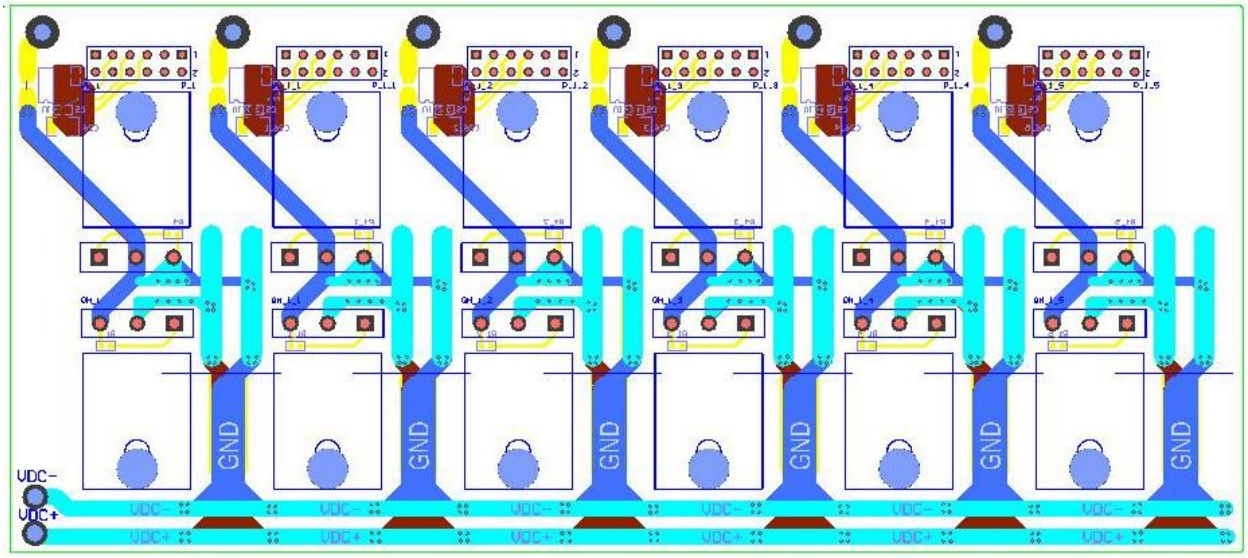
Finally, the gate drivers for SiC MOSFETs adopt positive 20 V and negative 5 V in order to achieve reliable fast switching, low conduction loss and reliable operation.

For conventional inverter system's gate driver design (with 10~20-kHz switching frequency), a shared power supply is used for all low side gate drivers. However, for 200-kHz system, the cross talk between each phase is significant. The high *di*/*dt* noise can be easily picked up through the shared power supply for low side gate drivers. In order to suppress the cross talk between phase legs, separated power supplies are adopted for low side MOSFET gate drivers.

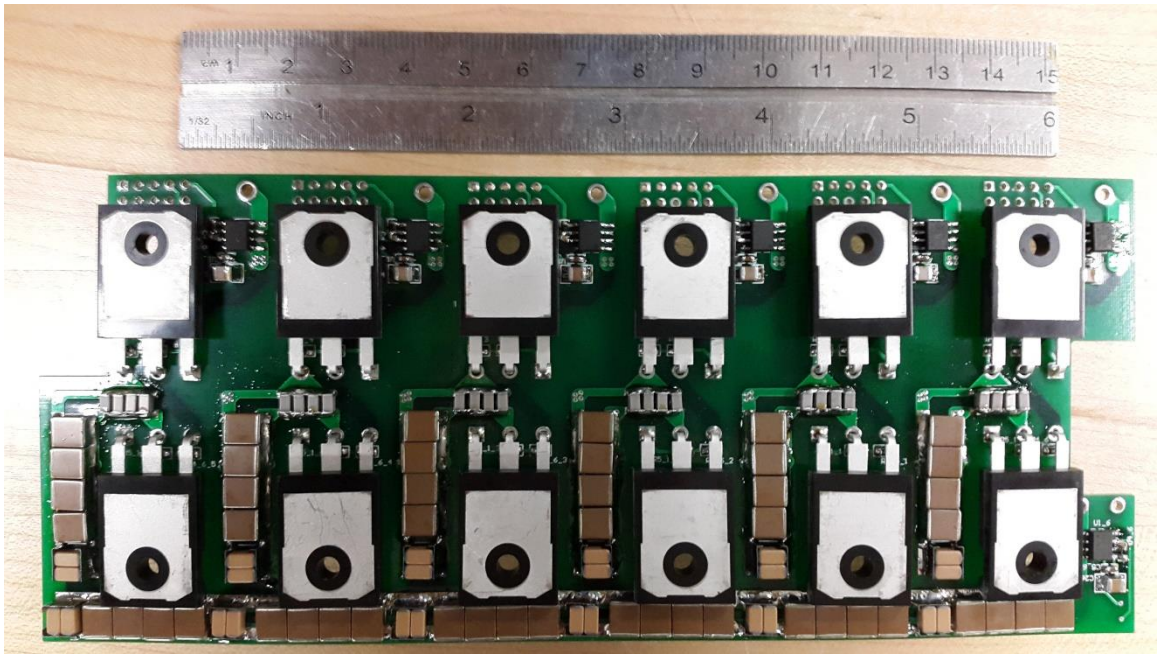
Large stray inductances of the DC voltage bus bar can cause voltage and current overshoots and ringing on MOSFETs and increase the voltage stress on MOSFETs. The bus bar PCB layout is optimized as it shown in Figure 110.

For each phase leg, separated trace is used and surface mounted film and ceramic capacitors are used to absorb high frequency current. In this way, parasitic inductance on bus bar is minimized; and the high frequency noise and the cross talk between different phase legs are effectively suppressed.

By optimizing the gate driver, power supply and bus bar PCB layout, the high performance and reliable operation of SiC MOSFETs are achieved.



(a) PCB bus bar layout



(b) Main power board bottom view

Figure 110: PCB layout of inverter bus bar.

7.3 Control system and optimization

The DSP control program needs to be carefully designed to meet the control requirement for the DC-capacitor-less inverter system. To achieve better dynamic response, DSP ADC sampling and the digital control program will be optimized for higher programming efficiency.

Figure 111 shows the control block of the digital system including interleaved carrier control, current sharing control, SVPWM control, AC output voltage control, 2ω ripple power compensation control (AC capacitor power control), and DC voltage control.

However, since the switching frequency (216 kHz) is very high, if the same fixed ADC sampling frequency is adopted, the DSP (F28035 with 60-MHz clock frequency) will not be able to finish all the calculation within one ADC sampling period [103]. Optimization of the DSP control program is required to achieve fast response with limited DSP calculation capability.

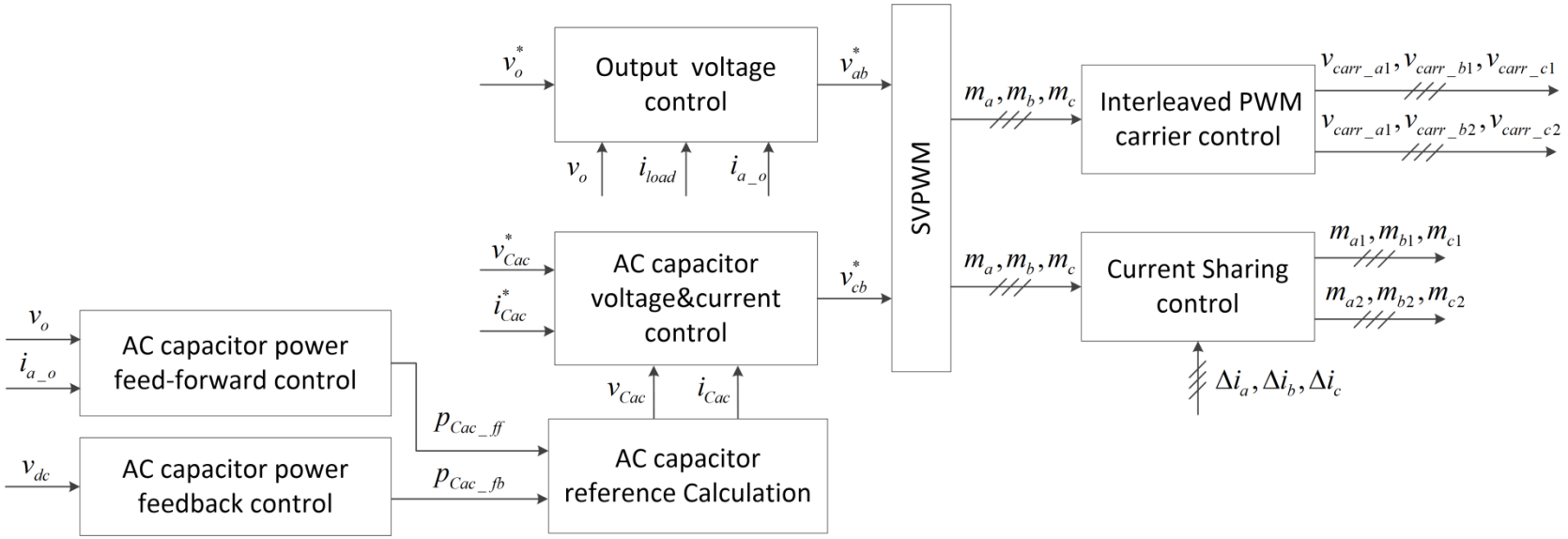


Figure 111: Proposed interleaved DC-capacitor-less inverter control system.

In order to fully utilize the DSP calculation capability, the control scheme is divided into two categories based on the control blocks' control bandwidth requirement: 1. fast updated functions including SVPWM control, current sharing control and interleaved PWM carrier control, and 2. slow updated functions including DC voltage control, AC output voltage control, AC capacitor voltage/current control, and 2w ripple power control.

Figure 112 shows the proposed digital control scheme. The fast updated functions will be executed every ADC sampling period, while the slow updated functions will be executed in a proper sequence and all slow updated functions' calculation will be finished in every four sampling period.

In this way, the control blocks, such as SVPWM control, current sharing control and interleaved PWM carrier control, can be updated every ADC sampling period to meet high frequency bandwidth requirement. At the same time, the control blocks, such as DC voltage control, AC output voltage control, AC capacitor voltage/current control, and 2ω ripple power control, which don't need very high frequency bandwidth, can use the rest of time in very sampling period to fully utilized the calculation capability of DSP without sacrifice of the fast updated functions' bandwidth.

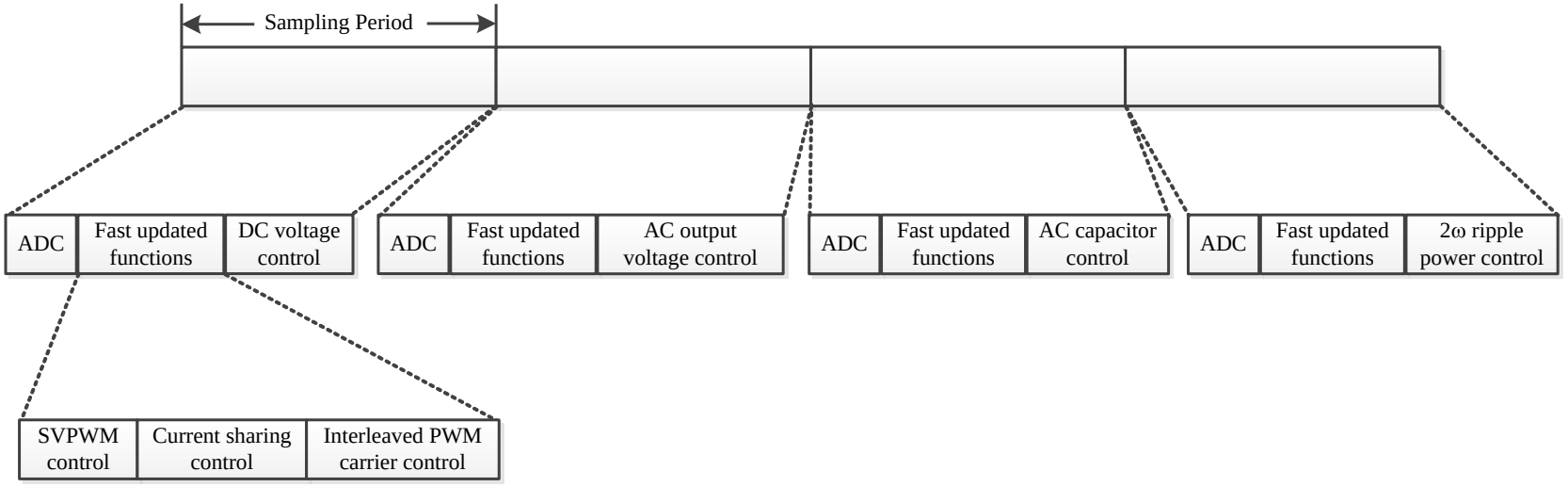


Figure 112: Proposed digital control scheme.

7.4 Experimental results

Figure 113 shows the prototype of 2-kW interleaved DC-capacitor-less inverter with SiC MOSFETs. The prototype is designed and tested by five members' team. As the team leader, I have designed main power board, integrated coupled inductors and digital control system. My labmates have contributed a lot work on 3D structure design and test of hardware including gate driver, power supply, DSP controller board and integrated coupled inductors. I would like to appreciate their help for design, test and assembling of the prototype.

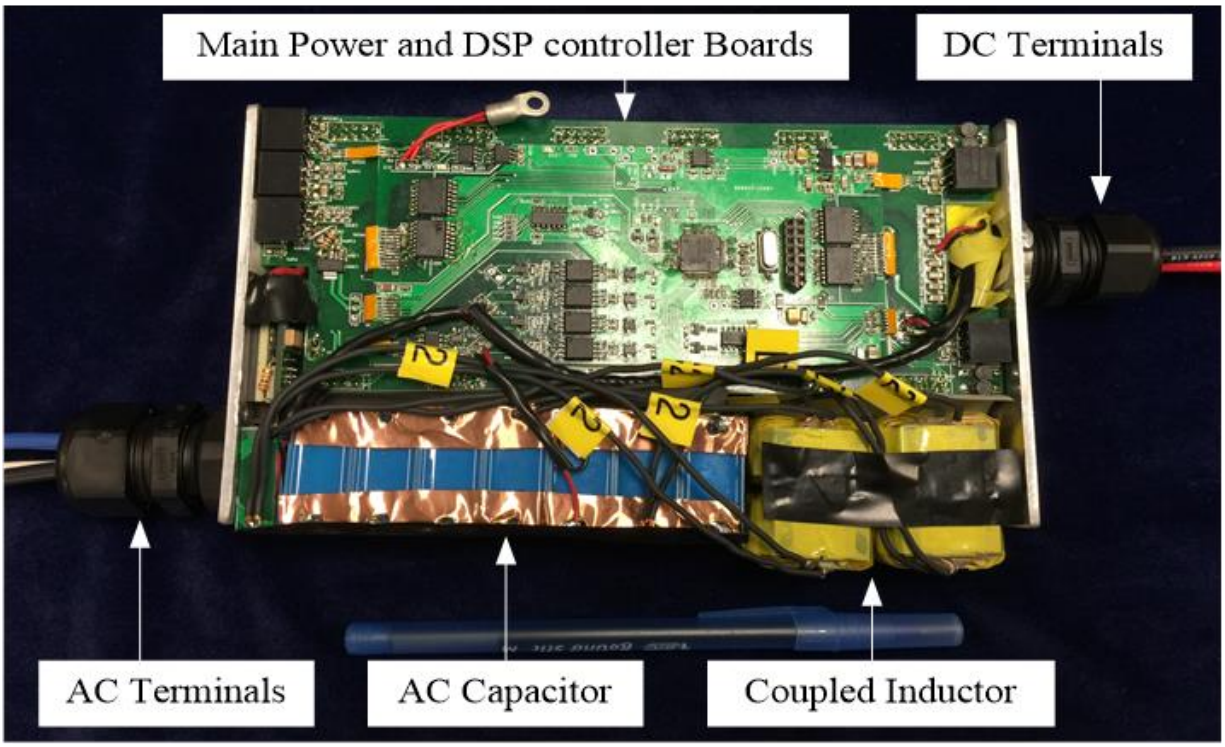


Figure 113: Prototype of 2-kW interleaved DC-capacitor-less inverter with SiC MOSFETs

The DSP controller board and interface board is on the top of main power board. The SiC MOSFET on the main power board is connected to the bottom case, and the bottom case also

works as heat sink. The AC film capacitor for AC ripple power compensation and the integrated coupled inductors connected to AC output and AC capacitor are also shown in Figure 113. The inverter has very compact structure and the dimension of the system is 7.30 inches x 4.75 inches x 1.26 inches.

Figure 114 shows the gate driver signal of high side MOSFET on two different phase legs. The voltage spike on negative voltage caused by miller effect is effectively suppressed by minimizing the loop of MOSFET gate driver.

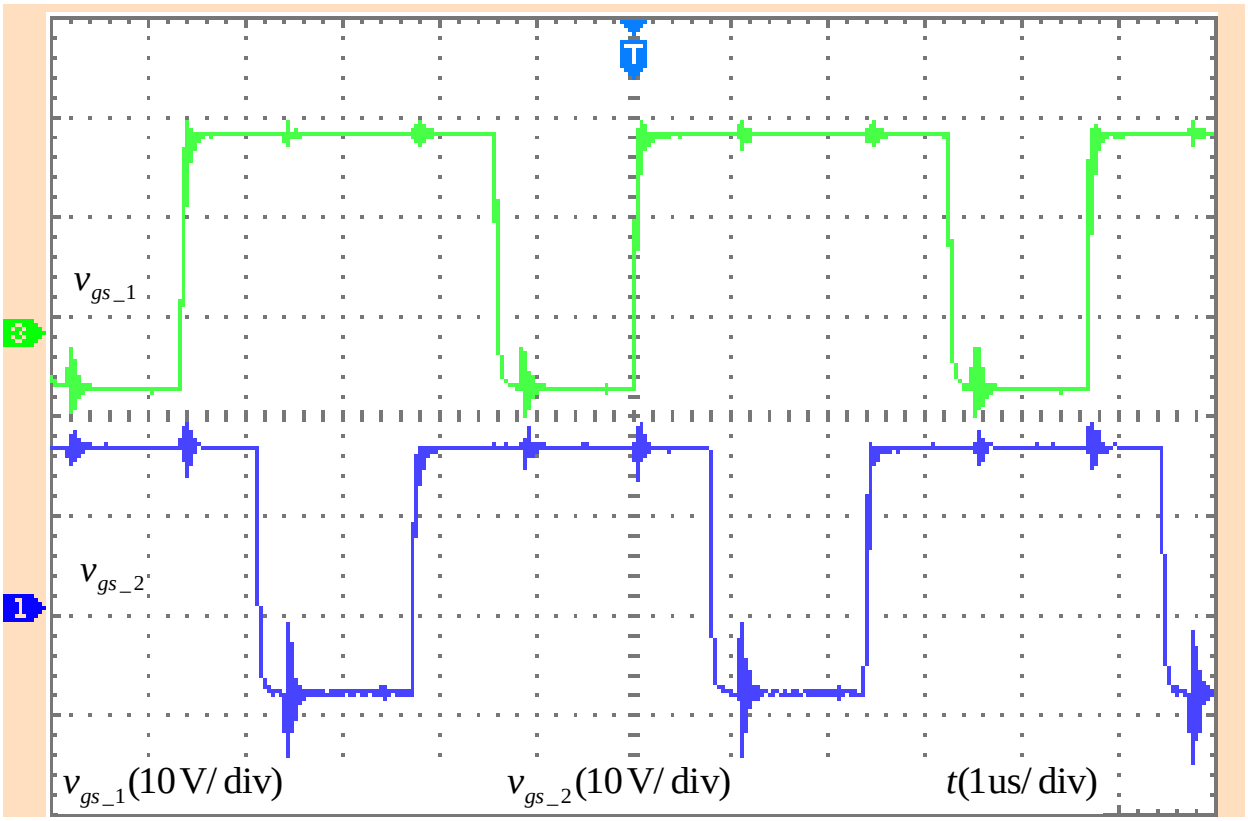


Figure 114: Gate driver signal of proposed system

The other voltage spike caused by cross talk between different phase legs on gate signal is effectively suppressed by using separated power supplies for each gate drivers and adopting

optimized bus bar PCB layout.

Figure 115 shows the dynamic response to sudden load change between 1 kW and 1.5 kW; and Figure 116 shows the dynamic response to sudden load change between 1.5 kW and 2 kW. As it shown in Figure 115 and Figure 116, the AC capacitor voltage, v_{cac} can follow the sudden change of output current, i_o to compensate the 2ω ripple power effectively.

In the first switching cycle, the AC capacitor power feed-forward control block immediately tracks the output current and change the feed-forward AC capacitor power reference. And the AC capacitor and current reference will be updated within one switching cycle.

In the following several switching cycles, the AC capacitor power feedback control block updates the feedback AC capacitor power reference based on DC input current and voltage to further accurately compensate 2ω ripple power and achieve good steady state performance.

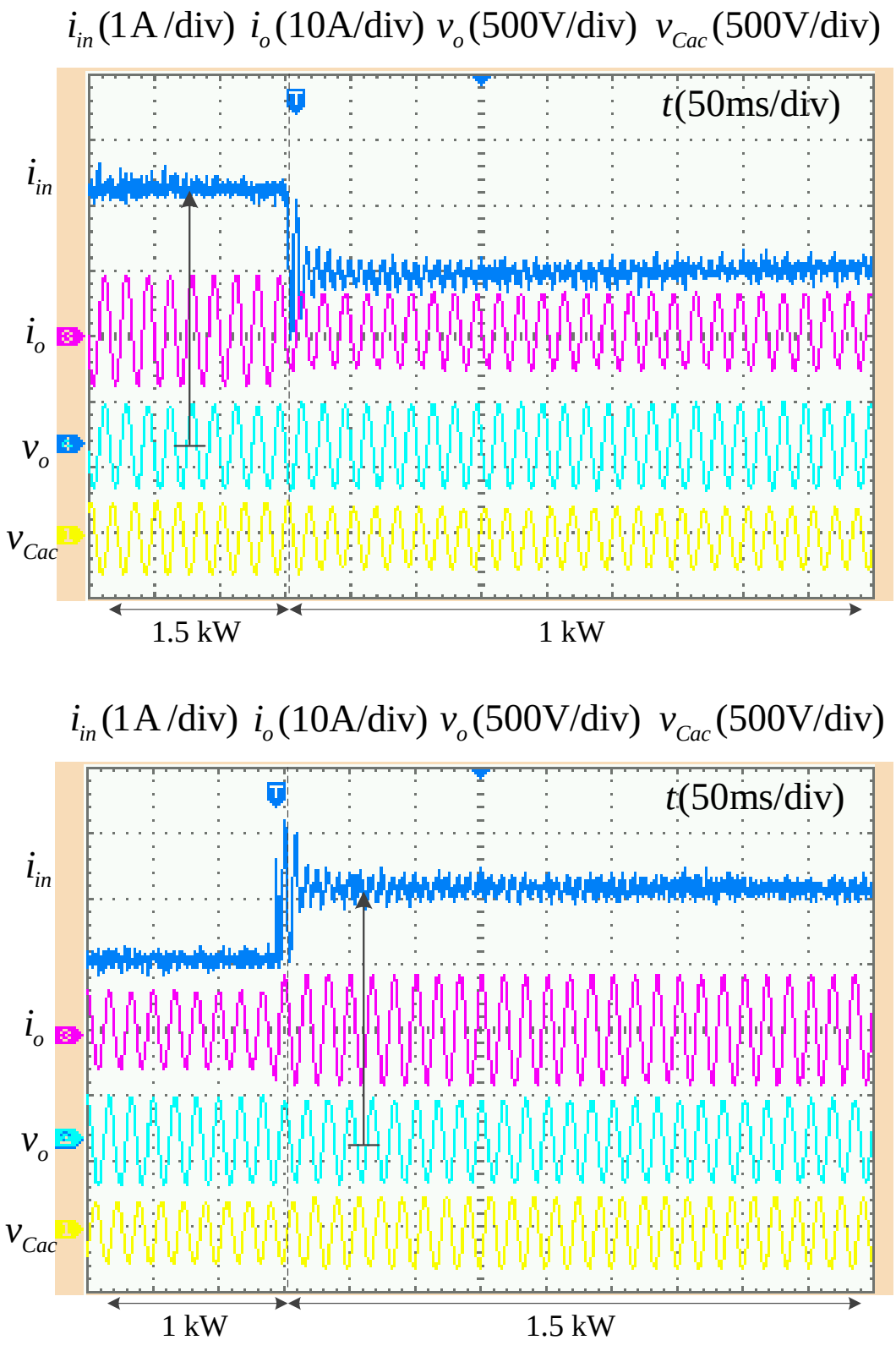


Figure 115: Dynamic response to sudden load change between 1 kW and 1.5 kW.

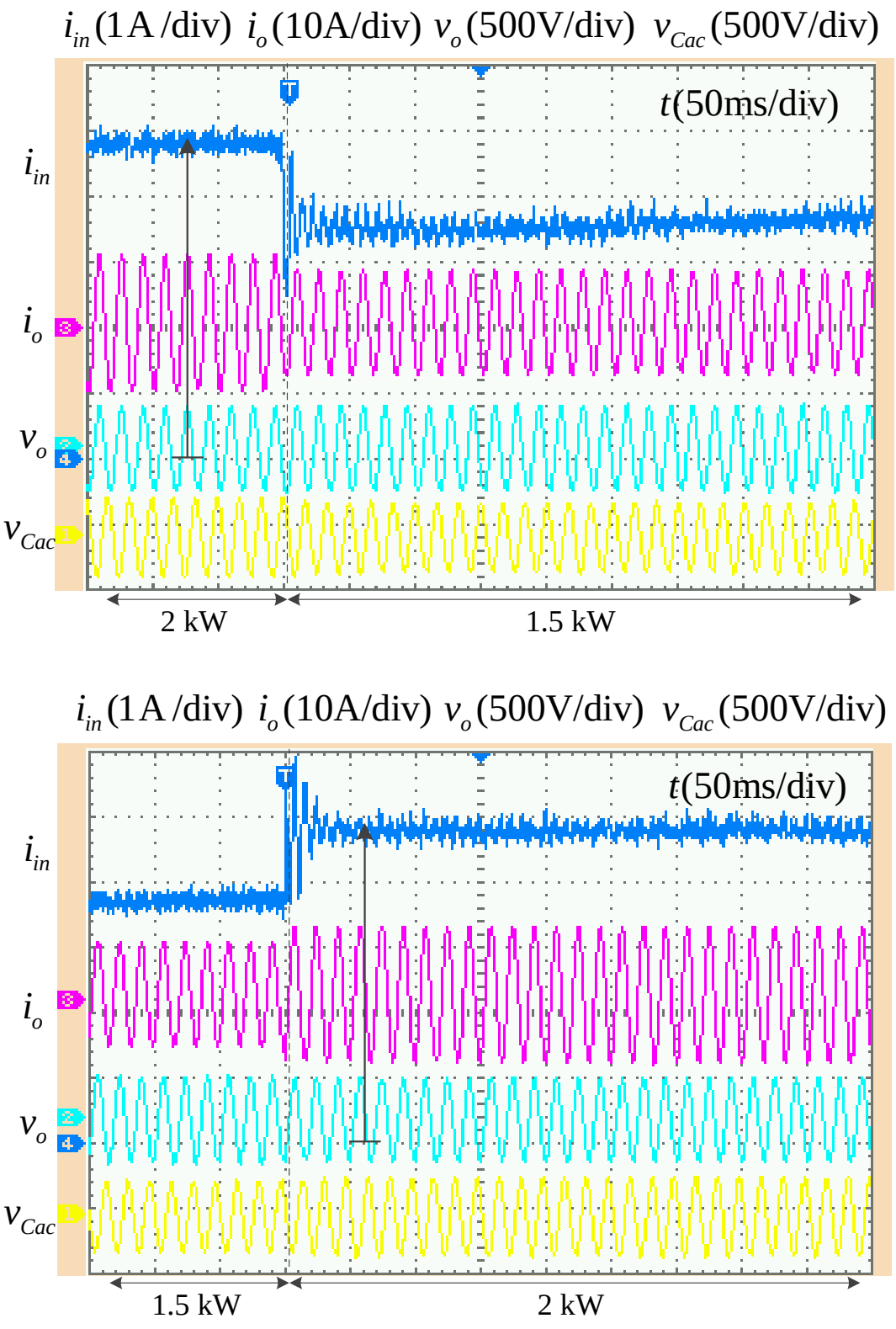


Figure 116: Dynamic response to sudden load change between 1.5 kW and 2 kW.

Figure 117 shows the efficiency vs output power for the proposed system. For rated power (2 kW), the system can achieve the efficiency of 96.2%.

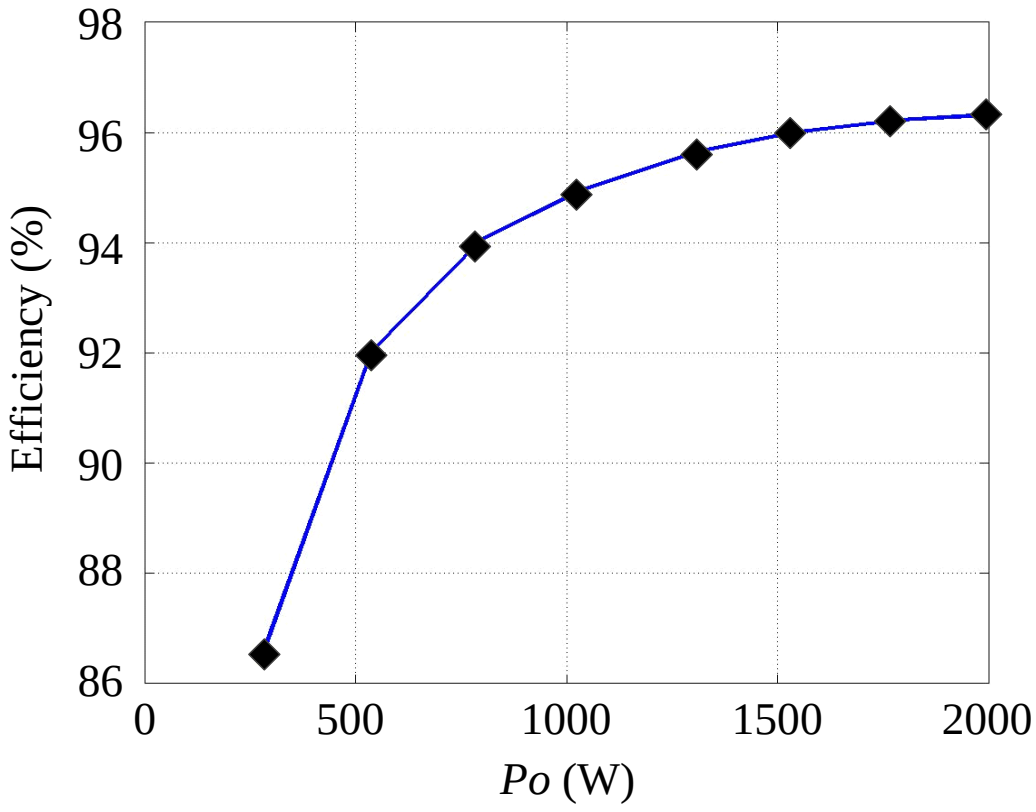


Figure 117: Efficiency vs output power for the proposed system.

7.5 Conclusions

In order to achieve a high power density, high efficiency and high reliability inverter system, SiC MOSFETs are adopted to achieve 216-kHz switching frequency. The design of gate driver, power supply and DC voltage bus bar PCB layout is provided in details to fully utilize the benefit of SiC MOSFETs.

Since the digital controller's computation capability is limited and the switching frequency of SiC MOSFETs is very high, it is very critical to optimize DSP control program to meet the control requirement for the DC-capacitor-less inverter system.

The experimental results have verified the effectiveness of the optimization of hardware and software design.

CHAPTER 8 CONCLUSION AND FUTURE WORK

8.1 Contributions

The contributions of this dissertation are listed as following:

- The problem of conventional single phase conversion system based on H-Bridge inverter is investigated; and the existing topologies with capacitive energy storage component for ripple power compensation are reviewed and evaluated based on the size of total capacitor size and total device power rating
- A DC-capacitor-less inverter for single phase power conversion with minimum voltage and current stress has been proposed. By adding another phase leg to control an AC capacitor, the 2ω ripple power can be absorbed by the capacitor and theoretically 2ω ripples to the DC capacitor can be eliminated completely. The H-bridge and the additional phase leg can be analyzed together as an unbalanced three phase system. By adopting SVPWM control and choosing the optimal AC capacitance and the voltage reference, the voltage and current stress of the switches can be minimized to the same as the conventional H-bridge. The size of capacitor is reduced by 10 times compared to the conventional H-bridge system.
- A solid state variable capacitor (SSVC) based on the proposed circuit shows benefits in terms of current stress of the share leg and efficiency, which is a competitive candidate for reactive power compensation applications with high power density and high reliability requirement. The shared leg's current stress is only one fourth of the stress of conventional H-bridge inverter. As a result, the capacitor size is reduced by 13 times with only 1.125 times TDPR of H-bridge circuit.

- In order to reduce the DC capacitor to minimal value, a novel control system directly based on ripple power for SSVC is proposed to achieve stable DC voltage and fast dynamic response. The feedforward part of the AC capacitor power is calculated by grid ripple power with the sampling frequency (20-kHz) to achieve fast dynamic response and maintain table DC voltage during sudden load change transition. The feedback part of the AC capacitor power is calculated based on discrete Fourier transform of DC capacitor ripple power with twice line frequency (120-Hz) to achieve better steady-state ripple power compensation performance. The steady state and dynamic performance of the proposed control scheme is verified by experimental results.
- An interleaved DC-capacitor-less inverter with SiC devices is proposed for high power density and high efficiency inverter applications. By using the two-channel interleaved structure, the conduction loss and passive component size can be significantly reduced. In order to improve THD performance for inverter output voltage, an enhanced phase-shift interleaved PWM scheme is adopted. A new structure of integrated couple inductors is proposed to suppress circulating current between the two parallel inverters and to filter output current at the same time. As a result, the total capacitor size is reduced by 16 times and power density of 45 W/in^3 is achieved.
- In order to achieve inverter system with high power density, high efficiency and high reliability, SiC MOSFETs are adopted to achieve 216-kHz switching frequency. The size of filtering components including DC filtering capacitor and AC output LC filter is significantly reduced. The design and optimization of gate driver and PCB layout is investigated to fully utilize the advantages of SiC MOSFETs. The DSP controller

programming is also optimized to meet the control requirement for the DC-capacitor-less inverter system.

8.2 Recommendations for future work

- The solid state variable capacitor is possible to replace the H-bridge inverter module in cascaded multilevel converter topologies such as transformer-less unified power flow controller (UPFC) and static synchronous compensator (STATCOM) to deal with the system fluctuating power problem. However, the power to each H-bridge inverter in cascaded STATCOM may not be the same and may contain other frequency components beside 2ω ripple power. It is very interesting and challenge topic to reduce the DC capacitor of H-bridge inverter and to keep a low total device power rating at the same time.
- The PCB layout, gate driver and power supply design of interleaved DC-capacitor-less inverter with SiC MOSFET can be further optimized for high switching frequency operation. Since the SiC MOSFET gate driver need 20V/-5V, a better power supply for gate driver circuit with high efficiency is needed. Better isolated gate driver with high current capability can also be adopted to improve the current design to have a better layout and more compact structure.
- For interleaved DC-capacitor-less inverter system, it is possible to adopt an asymmetrical structure for AC output and AC capacitor to achieve overall better performance. The improved interleaved DC-capacitor-less inverter can achieve very low THD of output voltage and have a much smaller size of filtering inductors as the same time. Moreover, the light load efficiency of system can be also improved.

8.3 Solid state variable capacitor in cascaded STATCOM

The proposed DC capacitor-less inverter can be treated as a converter cell and it can be used to replace the H-bridge inverter module in cascaded multilevel converter topologies such as transformer-less unified power flow controller (UPFC) and static synchronous compensator (STATCOM) to deal with the system fluctuating power problem.

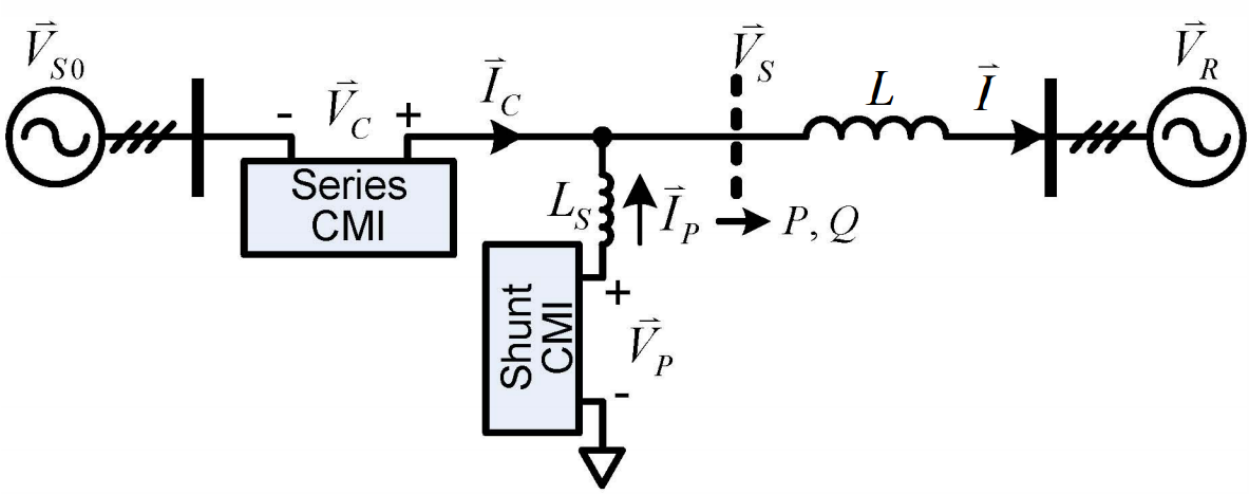


Figure 118: Transformer-less UPFC using cascaded multilevel inverter.

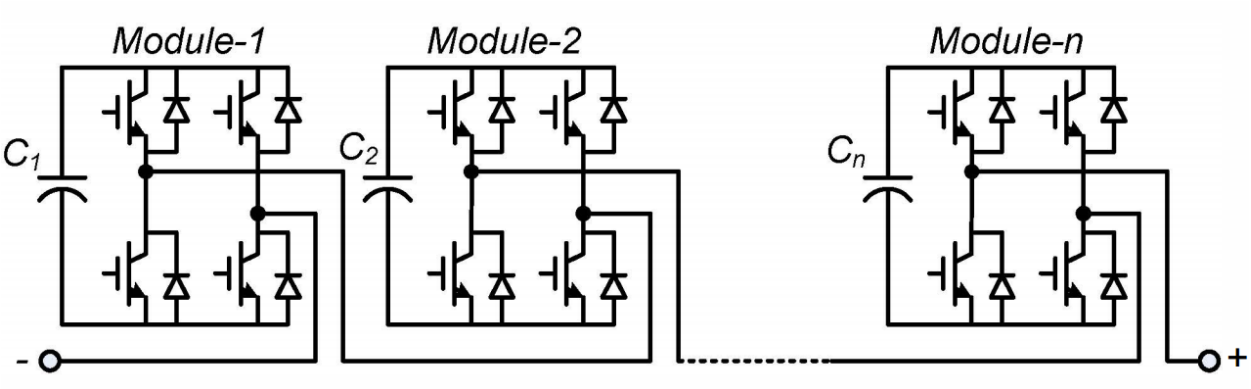


Figure 119: Cascaded multilevel inverter based on H-bridge.

The transformer-less UPFC shown in Figure 118 adopted two cascaded multilevel inverters (CMIs) and the control of the two cascaded multilevel inverters as a power flow controller make it possible to independently control active and reactive power flows. The transformer-less UPFC has the advantages of light weight, high efficiency, high reliability, low cost and fast dynamic response [23, 24].

Figure 119 shows the cascaded multilevel inverters based on conventional H-bridge inverter. However, a known problem of transformer-less UPFC is that each H-bridge module may need a large and bulky capacitor to hold the DC voltage. As the number of H-bridge module increases, the whole system may become very huge in size. The proposed DC-capacitor-less inverter cell could be a potential candidate to solve this problem. With much smaller capacitance, the voltage of each module can be controlled to maintain a constant DC voltage. Nevertheless, the capacitance reduction can only be achieved at the expense of increased number of active components.

Another design challenge is that the power of each inverter module may not be the same and may contain other frequency components beside 2ω ripple power. In chapter 5, an improved feedback control scheme for AC capacitor makes it possible to compensate other even frequency components power as well. However, the total device power rating may increase significantly when the system need to compensate all ripple power. A trade-off between the compensated ripple power by AC capacitor and the capacitance of DC capacitor is very important to keep the balance between DC capacitor size and total power device rating. The feasibility of this method and optimization of the system will be studied in future research work.

8.4 Improved interleaved DC-capacitor-less inverter

In Chapter 6, the proposed DC-capacitor-less inverter has a symmetrical integrated inductor structure for AC output and AC capacitor. Since AC capacitor is adopting film capacitor, which has much larger capacitance value than AC output filtering capacitor, the inductor current for AC capacitor allows much larger current ripple with same voltage ripple design. In addition, unlike the AC output voltage, the AC capacitor voltage don't have requirement on THD and EMI. It is possible to adopt an asymmetrical structure for AC output and AC capacitor to achieve overall better performance.

Figure 120 shows the proposed improved interleaved DC-capacitor-less inverter. The improved interleaved DC-capacitor-less inverter has two separated AC capacitors, C_{ac1} and C_{ac2}. And the two AC capacitors are connected to phase B and phase C of the two parallel inverters respectively. For each AC capacitor, separated filtering inductors, L_{c1} and L_{c2}, are used.

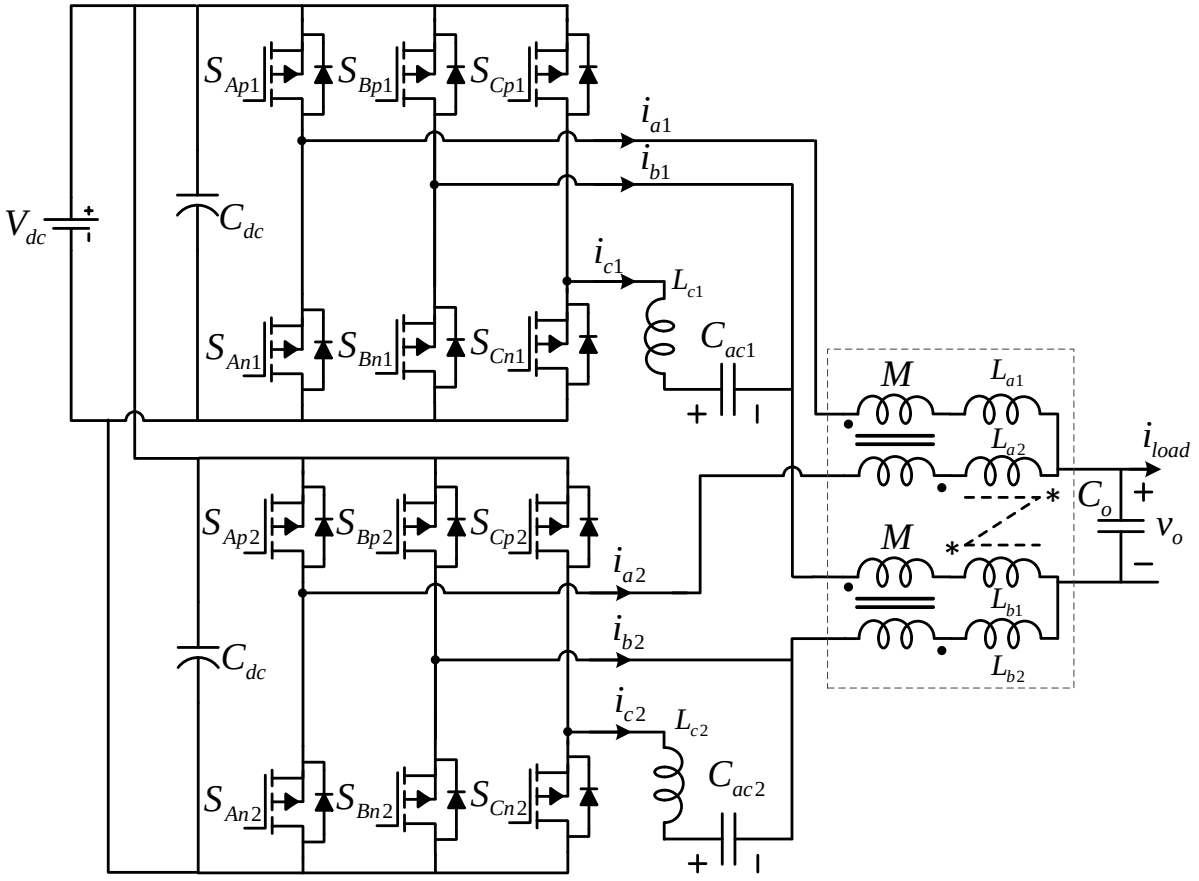


Figure 120: Proposed improved interleaved DC-capacitor-less inverter.

Since the improved interleaved DC-capacitor-less inverter still adopts the same integrated coupled inductor structure for AC output voltage, the output voltage can still have very low THD. At the same time, the proposed interleaved DC-capacitor-less inverter will have the following advantages.

The design of filtering inductor L_{c1} and L_{c2} can be optimized to achieve much smaller size. Since the AC capacitors are film capacitor and have large capacitance value, the AC capacitor will allow much larger switching ripple current than AC output capacitor without significantly increasing the power losses. The current ripple on L_{c1} can be designed to be 2 ~3 times larger than integrated coupled inductor. In addition, since two separated AC capacitors are used, the

inversely coupled transformer is no longer needed. Therefore, the size of the two separated filtering inductors can be much smaller than one coupled inductor.

Moreover, the improved interleaved DC-capacitor-less inverter will have a much better light load efficiency. When the system is working under light load, the system only need one AC capacitor to compensate the ripple power, and phase leg connected the other AC capacitor can stop switching in order to reduce power loss.

For proposed interleaved DC-capacitor-less inverter, since two separated AC capacitor is adopted, one additional voltage sensor is needed for AC capacitors and the two control loop is needed to compensate the two AC capacitors separately.

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