DEVELOPMENT OF EPOXY CHIP-IN-CARRIER INTEGRATION FOR LAB-ON-CMOS ELECTROCHEMICAL MICROSYSTEM

By

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ABSTRACT

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Miniaturized biosensor arrays are attractive for parallel analysis of multiple parameters and targets. Overcoming the need for bulky bench-top instruments, miniaturized electrochemical sensor arrays enable many applications such as DNA testing, drug screening, antibody and protein analysis and biosensing. With advances in CMOS technology and microfabrication, it has become possible to integrate and miniaturize the sensors and CMOS instrumentation electronics on a single chip. Further integration with microfluidics leads to a more powerful lab-on-CMOS microsystem. However, such integration involves multidisciplinary knowledge of CMOS design, sensor technology, microfluidics and post-CMOS microfabrication and packaging. This dissertation seeks to overcome the challenges in post-CMOS fabrication and packaging and the size disparity between CMOS IC chip and microfluidics to enable lab-on-CMOS electrochemical sensing. A new, low-cost, CMOS compatible epoxy chip-in-carrier integration process was designed to package CMOS IC chip and expand the CMOS chip surface area. A new reliable surface polymer silver interconnect process was developed utilizing modified screen printing methods. The silver ink metal interconnects enable inexpensive electrical connections for CMOS ICs with improved yield due to their high thickness. An improved polymer silver interconnect process tailored to high density contacts was also invented by embedding interconnects in SU8 microchannels. For the first time, direct on-CMOS electrochemical measurements were achieved using an on-CMOS microelectrode array within on-CMOS microfluidic channels. This work defines a new lab-on-CMOS platform that enables on-CMOS electrochemical sensing within

liquid-handling microfluidics.

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1 Introduction

1.1 Motivation

Identifying and quantitatively measuring analyte concentrations is one of the key objectives in chemical, biological and medical applications such as environmental monitoring, biohazard detection, clinical diagnosis, bio-product manufacturing, and drug discovery [1-4]. In particular, biosensors provide great diversity, sensitivity and specificity through hybridization, binding, transfer and interaction with target analytes by using antibody, antigen, peptide, aptamer, DNA, etc. interfaces. Biosensors are powerful tools not only for understanding the fundamental behaviors of biointerfaces but also for development of medical devices. For example, using electrochemical techniques, glucose sensors have both broadened our understanding of the glucose oxidase biointerface and been developed into the most commercially successful household biosensors in recent years [5].

To measure signals from biosensors, including analyte concentration in solutions, many techniques have been developed, such as electrochemical methods, optical imaging, thermal detection, and spectrometry [6]. Electrochemical sensors are often desirable because they offer label-free detection, low power consumption, low cost, and potential for miniaturization. The electrochemical methods are widely used in the detection of hybridized DNA [7-13], neuron tissue [14, 15], bacteria [16-19] and enzymes reaction [20-24]. Unfortunately, existing electrochemical instruments are bulky, expensive and inefficient with low throughput. The recently developed advanced semiconductor CMOS microelectronics enables low power and low cost integrated circuits (IC) on much smaller chips that can replace the existing bulky instruments. These tiny CMOS IC chips also bring benefits like high sensitivity, high density I/O

suitable for array signal handling, and high performance.

As instrumentation shrinks to chip scale, nowadays the biosensors can be dramatically miniaturized down to micrometer size with enhanced performance due to advancements of MEMS and microfabrication technology. Together with CMOS instrumentation IC, the miniaturized biosensors can offer better sensitivity, lower power consumption and low cost at a smaller device compared to traditional instruments. Meanwhile, CMOS IC fabrication process is a very mature manufacturing process which is compatible with a lot of biosensor fabrication process. This allows biosensors to be monolithically integrated with CMOS IC chips during or after CMOS manufacture. Often, microfluidic technology is adopted in biosensor array to take advantage of microfluidics' fluid handling capability. Microfluidics is a recently emerging technology that manipulates fluids in small volume, using components like micromixers, microvalves and micropumps. Microfluidics can automatically handle fluids of biosensors in microfluidic channels and essentially reduce the usage of expensive bio-reagents.

With the addition of powerful CMOS IC, integrating three components of CMOS IC, biosensors and microfluidics altogether into a miniaturized microsystem could become very rewarding. Through integration, the microsystem could allow highly sensitive, high throughput biosensing with CMOS IC and automatic microfluidics. The large variety of biological targets available to biosensors also drives a demand for high throughput biosensing where the high density CMOS I/O could ease sensor signal wiring issues. Many solutions have been reported to integrate CMOS IC, biosensor and microfluidics. They either integrate CMOS IC and biosensor, or fabricate biosensor and microfluidics together. However, the breakthrough solution of monolithic integration of microfluidics and biosensors directly on top of CMOS IC still remains

as an open challenge.

1.2 My approach

To enable monolithic integration of CMOS IC, biosensor and microfluidics, my approach for integrating a CMOS microfluidic biosensor microsystem is presented as shown in Figure 1.1, which is adapted from prior work developed in our lab. A CMOS instrumentation IC chip acts as the substrate of the microsystem. A biosensor fabricated post-CMOS on the surface of the chip is connected through contact openings in the top CMOS dielectric layer to the underlying CMOS electronics. Microfluidics is integrated right on top of the CMOS IC and biosensor array. With proper packaging and encapsulation, the integrated CMOS microfluidic biosensor array microsystem can interface with external supporting instruments and carry out on-chip biosensor measurement.

This approach could have many advantages. Biosensor miniaturization and CMOS implementation could allow reduced use of reagents and cost, enhanced sensitivity and

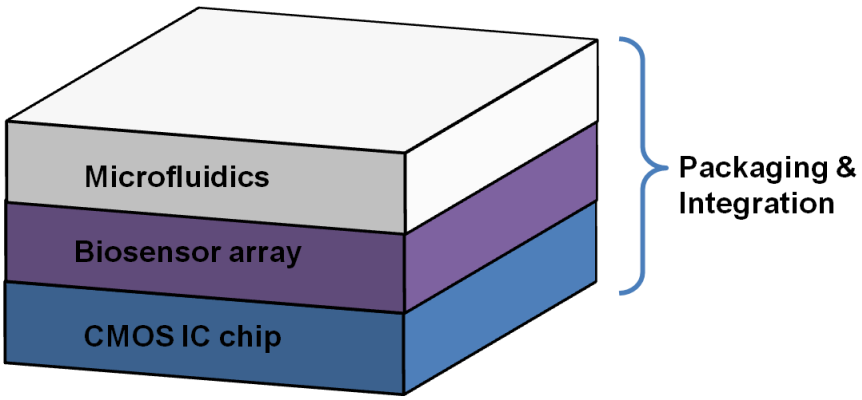


Figure 1.1. Conceptual illustration of an integrated CMOS microfluidic biosensor microsystem. Biosensor is on top of CMOS chip and then integration is finished by microfluidics, packaging and encapsulation.

portability. The direct, on-chip, electrical connection of electrodes to the instrumentation circuit could eliminate external wiring and provides immunity from environmental noise. The minimization of noise could permit highly sensitive circuits to measure the responses from miniaturized biosensors. Integration of microfluidics could provide localized and automatic fluidic handling necessary for the biosensors on CMOS chip with reduced reagent usage. The integrated microsystem could further eliminate the need for bulky bench top equipment, and can be utilized toward handheld portable lab-on-chip applications.

1.3 Challenges

To realize the microsystem concept defined by Figure 1.1, the design, fabrication and integration introduce many challenges. The microsystem structurally consists of three individual components: electrochemical CMOS electronics, biosensors and microfluidics. The technology for implementing each component is generally mature and well studied within its own field. However, each component have evolved individually and is generally not well suited to be integrated with others. Little study has been done to solve the unique issues involved in combining CMOS, biosensors and microfliudics. To integrate them together, efforts are needed to synergistically understand constraints imposed by each part. Based on prior work in our lab and preliminary studies within this thesis project, the main challenges to achieving the integration of CMOS microfluidic biosensor array microsystem are defined by the following questions.

- How can the integration of microfluidics be performed on top of a CMOS IC and biosensor array?
- How can packaging and encapsulation processes be developed to enable both biosensors and CMOS chips fully operational with integrated microfluidics?
- How can we insure the fabrication process is compatible for CMOS IC, biosensor and microfluidics?

1.4 Thesis goals

The main goal of the thesis is to overcome the challenges described above and develop an integrated CMOS microfluidic biosensor array microsystem. Based on individual understandings of CMOS electronics, biosensors and microfluidics, efforts will focus on finding ways how to integrate them together with proper fabrication and packaging technologies. Scientific contributions are expected in areas of microsystem integration methods and microfabrication methods.

1.5 Thesis organization

In this thesis, Chapter 2 covers the background and literature review of biosensor, CMOS electrochemical circuits, electrodes, packaging and microfluidics. Chapter 3 presents the development of a unique integration approach of epoxy chip-in-carrier integration. Several chip-in-carrier process methods are designed and carried out to demonstrate the developmental efforts. Chapter 4 covers planarization, metal interconnects and microfluidic integration in chip-in-carrier integration using a passive silicon die. Three types of planarization, thin film metal and silver ink metal interconnects are presented to enable electrical connections for the chip. Chapter

5 covers implementation of chip-in-carrier method for an active CMOS IC chip. A revised metal interconnects are presented to count for the active CMOS IC chip. Chapter 6 covers the contributions and future work.

2 Background and Literature Review

2.1 Protein based biosensors

In the healthcare and medical area, the development of drugs and treatments is based on the multiple science disciplines including biology, physiology, toxicology, genetics and proteomics, etc. The study of these disciplines is accelerated by the help of sensors and transducers developed by advanced fabrication technology. Biosensor, named as the sensors and transducers related to biology, becomes more familiar nowadays and is used in the literature in many ways. In broad perspective, biosensor can be defined as a device used to measure biologically-derived signals or that senses using biomimetic strategies or that detects the presence of biomolecules. Generally, it consists of molecular recognizing unit or biointerface that interacts with biological substances and generates one form of energy, and signal transducer that generates electrical signals. The generated electrical signals are then transferred to and interpreted by readout circuits. The applications of biosensors also include many areas closely related to human life such as quality assurance in agriculture, food and pharmaceutical industries, monitoring environmental pollutants and biological warfare agents, medical diagnostics, biological assays and more. Being a sensor, the general requirements include continuous operation, appropriate sensitivity, fast and predicable response, high reliability and selectivity, easy to calibrate, and etc.. Biosensors are required to be biocompatible and do not deteriorate in the presence of biological substances.

Among many biosensors developed, antibody based, DNA and protein biosensors emerge gain more attention due to the importance of the applications. DNA biosensors have been matured over the past decades since the emergence of polymerase chain reaction (PCR) technique. The DNA detection and replication can identify and reproduce the biotarget and

genomic database analyses can assign putative functions to the proteins. Protein biosensors are one of the highly needed biosensors for preclinical, toxicological and clinical studies in order to identify the candidates for drug screening, monitor efficacy and toxicity, etc.. Their functional properties can only be verified and characterized through extensive electrobiochemical studies with the proteins residing in their operating media. For example, membrane proteins are only active and functional when embedded in the cell membrane. Antibody based biosensor is usually used in immnunoassay to measure the presence or concentration of a macromolecule or a small molecule in a solution. Through the immunoassay of biological liquids such as serum or urine, analyte concentration is analyzed in medical and research practice. Due to the huge varieties of the proteins, antibody, DNA etc., together with a number of experimental parameters to control to fully characterize the biotargets, the number of experiments needed is exceptionally large. However, lack of good, low cost biosensors usually makes the experimental study a tedious, linear effort in time.

Ongoing research progress in biosensors suggests possible solutions for high throughput biosensing study. Integrated microsystems including CMOS circuits and sensors for DNA, antibody or gas analysis have been developed with advanced microfabrication and sensing technology. These works can be used as good example solutions to refer to, that take advantage of benefits of each individual technology, for the microsystem development for high throughput biosensor study.

2.2 CMOS electrochemical techniques and circuits

Traditionally, high-cost bulky instrumentation is used to characterize the proteins in biology research and study. In the case of microsystem, a low-power, low-cost CMOS IC solution is

required to replace the bulky instrumentation. A number of electrochemical instrumentation CMOS ICs have been developed in the past decades for various applications [25-27]. Depending on implementation methods, electrochemical instrumentation circuits can be categorized into two types, amperometric technique and electrochemical impedance spectroscopy (EIS) technique. In this section, the existing electrochemical instrumentation circuits implemented in CMOS IC are briefly reviewed.

2.2.1 Benefits of CMOS technology for high throughput biosensing

The proteins, antibodies, and DNAs can be immobilized on electrodes and their interaction with analytes is electrochemically detectable. This combination allows the use of electrochemical instruments to study the analytes, however, the work calls for intensive time and labor investment under current technologies. New and better tools are required in order to overcome the challenges such as the isolation of single protein species, observation of individual molecule activities, parallel studies under different conditions and even high throughput operation. The high throughput operation requires large number of sample measurements being made in parallel. The highly integrated CMOS IC is competitively capable of handling thousands of signals at the same time with high speed and low power, which is a superior feature to carry out large number of simultaneous readouts from biosensors. While many biosensing mechanisms are electrochemical in nature, CMOS electronics can perform electrochemical measurements and also provide benefits like high resolution, low power and miniaturization. Therefore, CMOS is a promising instrumentation tool to be employed in the high throughput automated biosensors.

2.2.2 Amperometric technique

Amperometric technique is to detect the current flowing through by applying potential between WE and RE. The simplified structure of amperometric technique is as shown in Figure 2.1. Controlled by the potentiostat, the working electrode potential is usually constant or ramped linearly in cycles versus time, e.g., chronoamperometry or e.g., cyclic voltammetry. In the ramping case, when the potential reaches a set potential, the working electrode potential is ramped down backward. This inverting process can happen multiple times during an experiment. The resulting current is plotted versus applied voltage to give the cyclic voltammetry trace. Cyclic voltammetry can be used to study the electrochemical properties of an analyte in solution by monitoring the oxidation/reduction current peaks, current levels etc. This technique is used in the development of biosensors where many bio-analytes are subject to redox reaction, especially

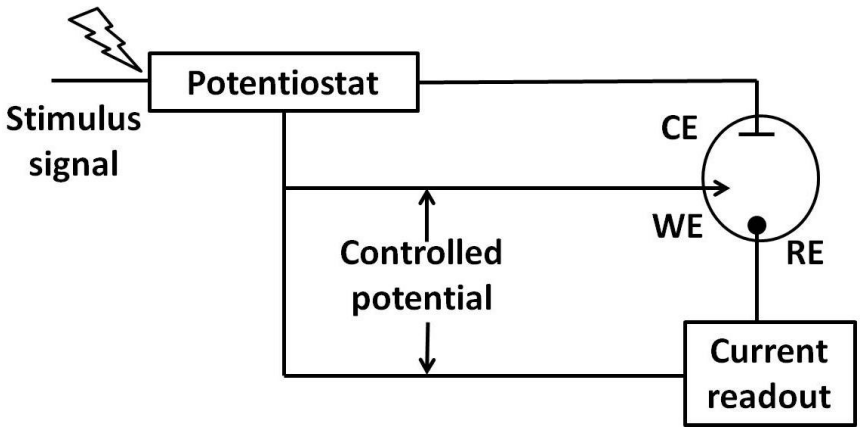


Figure 2.1. Simplified block diagram of circuits for amperometric measurement

in enzymes, DNA and protein detections.

Cyclic voltammetry can be designed as a two-electrode (working/counter) or a three-electrode (working/counter/reference) system. If three-electrode system is employed, it can be

arranged to control the potential of working electrode with respect to the reference electrode while measuring the current between working and counter electrodes.

One of the most important electrolyte redox couples used in cyclic voltammetry is potassium ferrocyanide/potassium ferricyanide ($K_4[Fe(CN)_6]/K_3[Fe(CN)_6]$). The reaction is

$$Fe(CN_6)^{-4} \leftrightarrow Fe(CN_6)^{-3} + e$$

When V_{WEvsRE} is scanned positively, $Fe(CN_6)^{-4}$ is oxidized to $Fe(CN_6)^{-3}$ and the current keeps increasing until $Fe(CN_6)^{-4}$ ions are depleted at vicinity of WE. During the reverse scan, $Fe(CN_6)^{-3}$ is reduced to $Fe(CN_6)^{-4}$ and the current keeps increasing until $Fe(CN_6)^{-3}$ ions are depleted at vicinity of WE as well. The peak potentials are noted as E_{pa} and E_{pc} for anodic peak potential and cathodic peak potential, respectively. The difference of peak potentials is given by

$$E_{pa} - E_{pc} = \frac{59mV}{n}$$

where n is the number of electrons involved in the redox reaction.

The peak current for the forward scan, i_{pc} is given by

$$i_{pc} = 2.69 \times 10^8 n^{3/2} A D^{1/2} v^{1/2} C$$

where, i_{pc} is peak current, A; n is number of electrons involved; A is electrode area, m^2; D is diffusion coefficient, m^2/s; C is concentration, mol/L and v is scan rate, V/s. From the equation, we can see the peak current i_{pc} is proportional to concentration and square root of scan rate. This is under the assumption of fast electron transfer and that the reaction is only diffusion limited. If the electron transfer is not reversible or the scan rate is so fast that the reaction is no longer

diffusion limited, the peak current is not proportional to square root of scan rate.

Numerous CMOS circuits have been introduced over the past decades with various functionality and performance to meet different application demands [28-32]. In the amperometric circuits design, it is key to improve the minimum detection current. Noise is a fundamental performance limitation for the amperometric circuits. One type of noise that needs to consider is 1/f noise because it is the dominating noise source for DC current detection circuit. Chopping and correlated double sampling (CDS) can be used to eliminate the 1/f noise. Thermal noise is another type of noise that limits the resolution of measurement. Longer integration time can reduce the thermal noise [33].

2.2.3 EIS technique

Electrochemical impedance spectroscopy (EIS) is a technique to measure the impedance of a target in AC steady state with constant DC bias conditions with electrochemical activity involved. By applying a small sinusoidal voltage over a range of frequencies the resulting current is measured and the impedance information is obtained over frequencies. When applying a reagent to the biosensor, the respective impedance changes. The response contains phase and amplitude information, algebraically related to real and imaginary components, which are extracted using an analog circuit or Fast Fourier Transform (FFT) algorithm. The FFT algorithm, however, is not a practical approach in the microsystem implementation due to poor multiplier linearity and accuracy and demands for preprocessing/pre-storing of the input data set and intensive computation needs. Alternatively, the frequency response analyzer (FRA) based method can be implemented in a compact analog circuits. The FRA method deals with one frequency response at a time. In biosensors using impedance spectroscopy, the applied small

signal (usually 10mV or less) will not damage the delicate biomolecule probe layer. Impedance spectroscopy techniques are widely used to develop membrane protein biosensors [34], gas sensors [35], humidity sensors [36] and DNA sensors [37].

In the EIS measurement, the frequency generally ranges from 10mHz to 100kHz. State-of-the-art commercial impedance analyzers also have data evaluation software and fitting programs which can generate the transfer function of the measured interface according to an equivalent circuit. Many EIS circuits have been realized at CMOS chip-level recently based on FRA method [25-27, 38].

2.2.4 Why on-chip?

Current fabrication technology is capable of post-CMOS process that can put microelectrodes on the CMOS chip. Sensor electrodes can stay off the CMOS chip and the measurement still could be taken. When sensing takes place on chip, no physical wires are included in the setup and this leads to lower noise and increased resolution which is very critical, for example, in possible detection of single molecule event. Again, CMOS chip is superior in interconnections thanks to its integrated signal routing which solves the routing problems associated with high density array of electrodes. To study a number of different proteins with statistical behaviors under various conditions, high density array is very desirable to increase the efficiency and reduce time cost. The sensors on CMOS could be able to form and test numerous biointerfaces simultaneously with much improved sensitivity.

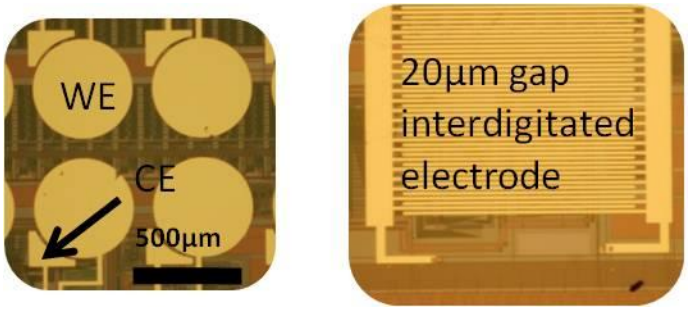
2.3 Electrodes for electrochemistry in microsystems

The electrochemical system consists of three electrodes, WE, CE and RE. The roles of WE,

CE and RE are different so as to their materials. WE is the location where bio-probe is immobilized or reaction takes place. Gold or carbon paste is usually used to attach bio-probes through covalent bonding of function chemical groups of bio-linkers. Platinum is often chosen thanks to its catalytic role in hydrogen peroxide detection. In recent research, nanomaterials have been conjugated with bio-probes either covalently or non-covalently to amplify the bio-signal. CE provides current path and is expected to be inert during reaction and much larger than WE so that half reaction at CE occurs fast enough, so as not to limit the process at WE. CE is usually made of noble metals like gold, platinum or carbon. For RE, whose potential should be stable, independent of the composition of other ions in the analyte, and reproducible even after a small electric current flow, Ag/AgCl, Cl^- reference electrode is preferably used. Generally, Ag rod is coated by hardly soluble AgCl and surrounded by electrolyte reservoir containing the Cl^- anion which is made of liquid-tight coating with diaphragm or porous membrane. Pseudo reference electrode is sometimes used which is only the metal rod without the salt or oxide coating and electrolyte reservoir. The use of pseudo-reference electrode asks for the defined and specific operation condition to calculate its potential.

In the development of miniaturized electrochemical system, electrodes need to be integrated with the CMOS chip to interface with bio targets to make electrochemical measurements. The fabrication of on-CMOS electrodes should be compatible with the CMOS. The existing semiconductor fabrication techniques for metallization include physical vapor deposition, sputtering deposition, and electroplating, all of which deposit thin metal films atomically. To utilize these existing semiconductor fabrication techniques compatible with CMOS and driven by semiconductor manufacturing, the three electrodes should be in planar embodiment determined by the fabrication methods.

The geometry of planar electrodes has to be carefully designed before moving to fabrication stage with consideration of multiple factors. The geometries on microelectrode size, shape, gap and positioning were studied by Bard [39], Wightman et. al. [40]. Two representative planar



(a) (b)

Figure 2.2. Two representative electrode designs. Disk electrode design (a); interdigitated electrode design (b).

electrode designs are shown in Figure 2.2. One is disc working electrode with closely placed counter electrode which is suitable for amperometric measurement. The other one is a high density interdigitated electrode which is good for impedance measurement with enhanced sensitivity and detection limits because of increased overlapping electrode area. The microelectrode could lead to many improvements including increased temporal resolution, decreased sensitivity to the effects of solution resistance, and the ability to make spatially resolved chemical measurements. Because of their small area, the double layer capacitance is reduced which allows the electrode potential to change rapidly. Voltammetry at microelectrodes is often a time-independent process and this characteristic is useful in sensor applications. The current at a disk electrode is complicated because non-uniform current density occurs at this structure. Nevertheless, the current at the disk electrode is similar to the currents at spherical electrodes whose current distribution has precise solution. Because the currents generated at

microelectrodes are small, accompanied by the small gaps between electrodes, the effects of ohmic iR drop are considerably less than at electrodes of conventional size. For microelectrodes, the instrumentation can be much simpler than that used with electrodes of conventional size. The three-electrode potentiostat used in conventional voltammetry is not necessary with microelectrodes because of the immunity to ohmic drop found with microelectrodes.

2.4 Encapsulation of CMOS microsystem for tests in liquid environment

To enable CMOS on-chip measurement, encapsulation is required that will maintain the on-chip electrode biosensor while ensures the stable operation of the CMOS electronics. In this article, packaging chip means putting CMOS chip in a physical fixture and electronically connecting the CMOS chip with wires. Encapsulation means after the chip is packaged, the chip, wires and package are properly insulated for testing in liquid environment. Related packaging or encapsulation methods that meet these demands have not been well studied due to its unique nature of testing environment. Testing environments of CMOS and biosensing are not conventionally established to match each other but sometimes even contradict. Proper integration is so critical that without proper packaging and encapsulation all the efforts in the previous development stages would result in failure. A satisfactory integration solution needs to take care of multiple aspects including microfabrication, bio-compatibility, building material, and packaging technologies, etc.

2.4.1 Review of prior works

One of the prerequisites to CMOS testing is that most of the CMOS ICs are commonly packaged in a ceramic package and wire-bonded to the body, regardless of the package mount format to external board. Many works have been reported using ceramic package for CMOS [25,

41-46]. The requirements for the encapsulation are to provide electrical insulation of the chip and electrical connections (e.g., wire bonds), and to be resistant to processing chemicals while biologically compatible. In this section, a review of different encapsulation methods with ceramic package and wire bonds will be presented. In the end, an alternative packaging approach that eliminated the wire bonds will be presented.

CMOS microelectrode array for electrochemical lab-on-a-chip applications: Using conventional microfabrication techniques an 8×8 6µm circular microelectrodes with center to center 37µm spacing were fabricated on silicon [42, 45]. Another chip with built-in very-large-scale integration potentiostat for electrochemical analysis was designed with individually addressable 32×32 array of 7µm square microelectrodes with 37µm center to center spacing on a CMOS chip [42, 45]. The CMOS microelectrode was post processed at the die level to coat the exposed aluminum layers with gold and electroless nickel immersion gold (ENIG) deposition was employed to create on chip electrode. Cyclic voltammetry was performed using a potassium ferricyanide electrolyte solution. Epoxy was applied by hand to encapsulate bonding wires. The ENIG deposition was reliable and reproducible. However, the epoxy application was not robust and resulted in several lost chips. The application of the epoxy required fine control to cover the bonding wires without coating the microelectrode array.

CMOS capacitive sensor lab-on-chip packaged by direct-write fabrication process: Sawan et. al. developed a high precision CMOS capacitive sensor [43]. The passivation on CMOS was removed by pad-etching process. The electrical wires and other components were encapsulated using low-temperature bonding techniques called direct-write fabrication process (DWFP). DWFP is a robotic deposition technique used to make layer-by-layer microscale

structures composed of paste filaments with different cross-sections. The filaments were formed by a micronozzle and deposited on a substrate when the extrusion of a paste-like material for building of planar or three-dimensional structures. The molding of an uncured epoxy resin followed the deposition of the filament deposition. The method could be a good candidate for chemical, biological microfluidics because it was not necessary to deal with expensive microfabrication in the cleanroom. The DWFP realized microfluidic structure on top of the integrated capacitive sensor.

CMOS microelectrode array for bidirectional interaction with neuronal networks: A 6.5mm×6.5mm chip was comprised of 128 stimulation and recoding-capable electrodes in an 8×16 array and an integrated reference electrode [44]. The chip was manufactured from foundry using an industrial 0.6um CMOS process. A 2-mask post-CMOS processing procedure was used to cover the Al electrodes with biocompatible platinum and to protect the Al using three stack of silicon nitride and silicon oxide. Reactive ion etching was applied to etch the dielectric stacks to define the electrode shape and locations. The processed chip was mounted on custom designed PCB and wire-bonded. Those wires and bonding pads were protected by water resistant medical epoxy. A glass ring was used to form a large reservoir to contain cell medium. In this case, epoxy was again used as the encapsulation material.

High-density CMOS switch matrix electrode array: A high-density CMOS switch matrix chip was mounted and wire-bonded on a custom-designed printed-circuit board (PCB) and connected with an electroplated nickel/gold edge-connector [41, 44]. A glass ring was then glued on the PCB, and a water-resistant medical epoxy (EPOTEK 302-3M) is used to encapsulate the bond wires and the pads. The packaging yield was currently limited by the poor adhesion of the

epoxy to the chip substrate. If the epoxy lifts off from the substrate, culture media can flow to the bond wires leading to electrolysis and corrosion, which renders the chips unusable. For short term cultivation or acute preparation an estimated yield of about 90% was achieved. For long term culturing over several weeks, the yield dropped to an estimated 70%.

A CMOS electrochemical impedance spectroscopy biosensor array: A fully integrated biosensor 10×10 array in a standard CMOS process was presented which implemented electrochemical impedance spectroscopy [25]. This system was able to detect various biological analytes, such as DNA and proteins, in real time and without the need for molecular labels. ENIG process was used to deposit on-chip gold electrodes. To do EIS measurement without interfering with the electronic data acquisition they isolated the conductive solution from the bond-wires, I/O pads, and the IC package by using an electrically insulating epoxy (EPOTEK H70S). The ENIG process suffered from rough gold surface and requires circuit design techniques to achieve consistent gold deposition over the whole chip area.

Biocompatible encapsulation of CMOS based chemical sensors: CMOS-based chemical sensors was encapsulate bonded on a cartridge and encapsulated with Parylene, while the sensing area was exposed by laser ablation and sonication [46]. They used a pulsed UV laser to ablate the frames on the perimeter of the ISFET sensing membrane. After ablation of the Parylene, the membrane Parylene was stripped in a standard ultrasonic bath. The success of this approach depended highly on the perfect focusing of the laser to remove Parylene uniformly. Otherwise, a non-uniform ablation could cause problems including areas where Parylene was not removed or there were damages to the underlying sensing membrane. Parylene was ablated the Parylene on the perimeter of the sensing area with the laser and the remaining membrane was lifted off with

sonication to expose the sensing region. Measured results demonstrated better electrical isolation than previous reported techniques.

Lab-on-CMOS integration of microfluidics and electrochemical sensors: Dr. Mason's lab introduced a CMOS-microfluidics integration scheme for electrochemical microsystems [47]. The author developed an alternative approach to package the CMOS chip. Instead of the traditional ceramic package, a micromachined extended carrier is fabricated to package the CMOS chip and the electrical connection is made by surface film metal routing. The leveled carrier and chip established a flat and smooth surface for integrating microfluidic structures. A model device with SU8 microfluidic mixers and detection channels over microelectrodes on a CMOS integrated circuit was constructed. Functional integrity of microfluidic structures and on-CMOS electrodes was verified by a simultaneous sample dilution and electrochemical detection experiment within multi-channel microfluidics.

2.4.2 Discussions

Several prior works of microsystem packaging for liquid environment have been reviewed and the packaging with ceramic package and wire bonds can be summarized into two parts, epoxy encapsulation and Parylene coating. Major goal of these types of packaging is to insulate the wire bonds for liquid environment. Epoxy encapsulation is an obvious and quick solution that can seal the wire bonds with relative low cost. Due to the small size of the chip and wire bonds, epoxy encapsulation is highly dependent on the person's hand-on skill to avoid epoxy to flood over the chip surface. The mismatch in thermal expansion coefficients between silicon and epoxy may lead to crack of the epoxy in a varied temperature environment and the fact that epoxy absorbs moisture also contributes to potential epoxy cracking and leakage. Parylene coating is

superior in protection of electronics from liquid environment. Parylene deposition is a low temperature process and Parylene covers every exposed surface of the sample. To open the sensing area on the CMOS chip, Parylene etching is needed. Parylene etching is usually done by oxygen plasma etching which requires physical mask to define the etching pattern which is not easy in the structure where the CMOS chip is wire bonded to package or PCB board. The laser cutting of Parylene used in the work is able to exclude the need for physical mask. The dose of the laser needs to be accurate enough that the laser does not penetrate the Parylene and drill the CMOS.

The last work which uses an extended silicon carrier eliminates the use of the wire bonds and it demonstrates the functional integrity of the lab-on-CMOS concept. This approach provides a surface platform that can be used for wide selection of microfluidic integration. The fabrication process requires a micromachined silicon carrier that went through multiple fabrication steps and the surface leveling of the carrier and the chip was critical to make thin film metal interconnect routings.

The traditional packages of IC chip prevent options for encapsulation and thus the yield is also affected by the unreliable encapsulation process. Even though the on chip measurements in liquid environments were achieved, most of them were limited to measurements in reservoir or only single channel microfluidics. The lab-on-CMOS carrier concept is more suitable for integration of multichannel microfluidics because of the extended CMOS chip surface. The types and applications of microfluidics have rapidly developed in recent years, covering huge amount of information. Microfluidics will be generally reviewed in the following section with basic background and several technical applications.

2.5 Microfluidics

Miniaturization is the key topic in analytical chemistry and life sciences. In the past two decades, miniaturization of fluid handling and fluid analysis has been developed in the interdisciplinary research field of microfluidics. Microfluidics is the science and technology involved in fluid transfer, separation, mixing and analysis for "micro-volumes" of fluidics. "Micro" means at least one of the following features, the volumes handled ranging from fL to μL; the device sizes smaller than mm; scaling effects of the micro-domain. Microfluidic applications cover micro arrays, DNA sequencing, sample preparation and analysis, cell separation and detection, as well as environmental monitoring. The use of microfluidics has many advantages such as, small amounts of sample and reagent, less time consumption, lower cost and high throughput. The research publications on microfluidics has been growing exponentially and a few books on microfluidics have been written recently [48-50].

2.5.1 Behavior of fluids in microscale

Different from macroscale, the behavior of the fluids in microscale is dominated by the fluidic resistance. At microscale, the Reynolds number becomes very low. Reynolds number represents the effect of momentum of a fluid over the effect of viscosity. A major result from this is that fluids, when placed side by side, do not necessarily mix in traditional fashion with eddies or swirls while the mixing is primarily achieved through the diffusion. The Reynolds number is calculated by the equation (1.1) below.

$$Re = \rho V \frac{L}{\eta} \tag{1.1}$$

where Re is the Reynolds number, ρ density of the fluid, V the velocity, L characteristic length,

and η viscosity. When Re<2100, it is in laminar flow regime where the fluid flows slowly with no inertial effects. In this case, it is considered to be in microfluidics regime so that the fluids mix predominantly by diffusion. When Re>4000, it is in unstable laminar flow regime where the turbulent flow occurs. In this case, it is no longer considered as microfluidics regime so that the behavior of the fluids follows the same as normal fluids in macro scale. As seen in the equation, the Reynolds number is related to channel geometry. A characteristic length D is introduced to replace the L depending on the channel geometry. For example, in channel with circular cross section, the diameter of the circle is the D. For rectangular cross section, $D=\frac{2ab}{a+b}$, where a, b are the sides. For an equilateral triangle, $D=\frac{\sqrt{3}}{3}a$, where a is the side.

2.5.2 Materials and fabrication process in microfluidics

A variety of fabrication techniques are used to make the microfluidic devices and the different techniques can be categorized as silicon micromachining and polymeric micromachining.

In the early days, most of the microfluidic devices were made of silicon largely because pre-established fabrication tools for silicon industry were available. The channels were either etched with KOH or dry etched using deep reactive ion etching or XeF_2 isotropic etching [51]. A glass cover is bonded on top of the silicon to seal the microfluidic channels and provide translucent view. In certain cases, device can be made of glass only. Active devices are fabricated in silicon also because of established technologies of metal deposition and piezoelectric material deposition. In some applications, silicon can not be used to make the device because of its conductivity when electrokinetic manipulation is involved. Despite of the established technology, the silicon microfluidics are relatively expensive because of the large surface needed for

channels and the use of expensive facilities. In addition, silicon is not always chemically and biochemically compatible.

Polymeric micromachining offers an alternative low cost option to fabricate the microfluidic devices. Thick film negative photoresist SU8 is patterned on a silicon wafer using optical photolithography. The SU8 serves as a mold for an elastomer such as polydimethylsiloxane (PDMS) [52-55]. The PDMS structure with microchannels can be bonded to a glass slide with surface treatment of oxygen plasma to form a complete device which is optically transparent. Multiple PDMS layer can be stacked together to form three-dimensional complex structure.

The thick-film SU8 can be directly used to make the devices. SU8 microchannels are formed on a silicon or glass substrate. SU8 has the advantage of simple micromachining. Channels can also be made by hot embossing with a hard template. The template can be made from silicon, glass or metals. This method is especially promising for mass production.

2.5.3 Microfluidics in biosensor applications

Microfluidics has been referred to as a technology that deals with the fluids in microscale while its implementation has been carried out under the context called micro total analysis systems (μTAS) in academia. μTAS or lab on a chip (LOC) originally means to realize the all the steps for chemical analysis of a sample including, sampling, sample transport, filtration, dilution, chemical reactions, separation and detection, on chip scale to reproduce a shrunk lab. Over the years, μTAS has brought in diverse spectrum of scientific and engineering disciplines and become a complicated multidisciplinary research fields. Microfluidics is the core technology that enables μTAS where the manipulation of fluids is the fundamental element. A vast number of technologies contribute to the μTAS such as the microfabrication, assembly and interfacing,

optical integration, flow control and instrumentation. The discussion of these technologies is beyond the scope of the thesis goal but can be found in the thorough reviews in [56-58].

Considering its application, μTAS covers various areas in biology to realize chip scale systems. First, cell handling and analysis has been implemented including cytometry [59], cell separation [60], cell lysis and whole cell analysis [61, 62], cell traps [63], and cell culture [64] etc.. Second, biomimetic systems inspired by the behavior of animals and bio processes have been studied [65]. Biopowered systems which attempted to utilize the molecular motors or biological systems have been demonstrated for various examples [66, 67]. Third, μTAS finds its application in clinical diagnosis such as blood cell separation and blood analysis, detection of pathogens. Fourth, the tools for immunoassays and DNA analysis including sequencing, separation and polymerase chain reaction have been developed on chip. Fifth, μTAS also found itself contributing to environmental concerns and gas analysis where the toxic substances in the air or water were detected and gas preconcetration, mixing and separation were studied. Lastly, related to the topic of this thesis, protein has been studied with μTAS in various approaches [68-71].

2.5.4 Discussions

The rapid advancements in microfluidics in past decades have provided a rich references of fabrication techniques and application specific examples. However, it has not been presented that how to successfully incorporate microfluidics with CMOS ICs for advanced integrated sensing platform. Motivated by the recent carrier based chip packaging reviewed in Section 2.4, the integration between microfluidics and CMOS IC becomes possible. The carrier based IC packaging used either silicon based or polymer based carrier of which both had its shortcomings

of high cost or low yield. In the next chapter, the chip-in-carrier IC packaging will be further analyzed and developed and the efforts will be mainly made under the goal of how to integrate with generic multichannel microfluidics. The chip-in-carrier IC packaging will be a solid foundation for the full lab-on-CMOS implementation in Chapter 5.

3 Chip-in-Carrier Platform for Integration of Microfluidics and CMOS Biosensor

3.1 Microfluidics and CMOS electrochemical biosensor array

Microfluidics could enable high-throughput automated biosensing with reduced use of reagents and parallel operations. With reduced volume and scale, the sensitivity of the sensors is also improved. Actually, numerous works in microfluidic device have demonstrated these attractive features of microfluidics. Meanwhile, the high density CMOS electronics is also capable of wiring a large number of sensor arrays for high-throughput analysis, an absolutely desirable feature matching microfluidics. Therefore, microfluidics is a very important part that could fully expand the capability of the CMOS electrochemical biosensor toward high-throughput analysis and characterization. To integrate microfluidics with the CMOS electronics, it is necessary to take a comprehensive overview of the technology of CMOS electronics packaging which is the required part to enable the CMOS ICs and affects the strategy to integrate the microfluidics. After the review, the requirements for of packaging will be discussed for the integration of microfluidics and CMOS. Then, chip-in-carrier integration will be generally discussed, followed by progressive development of polymer chip-in-carrier process. The chapter will end with discussion of the polymer chip-in-carrier process and its impact on the following planarization and metallization process.

3.2 Electronic packaging technologies for integration of microfluidics and CMOS biosensor array

In addition to traditional wire bonded ceramic package, many other technologies have emerged to handle and package the CMOS die and modules in recent years. These technologies enable die level processing and high density system integration that greatly enhance the

performance of the chips and decrease the form factors. Electronic packaging has two main concepts, namely system on chip (SOC), where the complete system is integrated into a single chip and system in a package (SIP) or system on a package (SOP) where the integration is done using the IC package. In SOC technology, a single integrated circuit chip contains all the necessary electronic components for a system. It could be the most compact version of the integrated system which only consists of electronic components. However, the challenge is obvious because it needs long design times due to integration complexities, several mask steps and intellectual property issues. In my project, the integration involves biosensors and microfluidics thus SOC is not the exact type of integration of interest. Meanwhile, SIP contains several chips integrated on a separate substrate to form a complete system. An SIP is a multichip module (MCM) that includes all the components of a complete system. SIPs can be divided into two main categories: MCM and 3-D packaging. MCMs are chip packages that contain several dies mounted together on a substrate. The MCM was invented for the purpose of regrouping of good ICs on a ceramic substrate. The MCMs are horizontal or 2-D and the interconnects are realized by wirings. The short interconnects among the chips improve the performance of the chips and reduce the noise. MCMs are classified by substrate: MCM-C (with ceramic), MCM-D (deposited), MCM-S (with silicon) and MCM-L (with laminated circuit board). 3-D packaging includes stacked packages, stacked similar or dissimilar die. The interconnects are wire bonds, flip chip or through silicon vias (TSV). SOP is a similar concept to SIP which offers the system solution in a package. However, SOP took one step further in overcoming the integration shortcomings of SOC and SIP. In SOP, the substrate has embedded functional components of the system which can be wirings, capacitors, inductors, filters and antennas.

3.2.1 Interconnects

The major types of interconnect techniques available are wire bond, flip chip and tape automated bonding (TAB). Wire bonding is the most general way where a fine metal (gold or aluminum typically) is bonded between I/O pads on the chip and the pins on the package. The process is done by pressure, ultrasonic and heat. The main advantages of wire bonding are high yield, high interconnect density of 30 to 35μm, and high flexibility of interconnect. The disadvantages of the wire bonding are high dynamic power dissipation, high I/O inductance, and additional signal delay. The shortcomings of the wire bonding in my project have also been analyzed in Chapter 3. Mainly, the wire bonding prohibits post-CMOS fabrication and integration. In flip-chip technology, the IC chip is placed on a substrate with its active surface facing the substrate. Interconnects between I/O pads on the chip and the pins on the package are done by solder bumps or Sn-Au balls through thermal heating, eutectic or thermosonic bondings. Flip-chip interconnects provide the shortest possible chip-to-package interconnection distance. However, it needs pre-determined design and various extra material and process including underfill epoxy, substrate metallization, substrate solder mask and chip passivation. Also, in flip-chip technology, solder migration, heat dissipation, die inspection and stress related reliability remain challenges. TAB is a high-density interconnection technology based on placing bare die onto a polyimide film with copper leads. The die is bonded to the metal lead through bumps using thermocompression bonding. One of the advantages of TAB is to test the chip prior to assembly.

3.2.2 Chip packaging for microfluidics

Microfluidics usually needs a large substrate in centimeter range compared to the relatively

small CMOS die area which is only a few millimeters in dimension. The utilization of substrate to facility microfluidic integration is especially attractive for the millimeter sized CMOS die. Flexible polyimide film has been used as the substrate to package the CMOS die and microfluidics [72]. The die was bonded to the substrate with flip-chip method and substrate area at the chip surface was etched away so that the chip surface was accessible by microfluidics that is bonded on the substrate. The channel height was limited by the solder bump height and the substrate thickness and only one channel of fluids can pass across the chip surface.

Instead of flip chip, people also have used surface film metal for interconnects. In this method, the chip is embedded in the substrate, such as high-density interconnect (HDI) [73, 74], chip-level integrated interconnect (CL-I^2) technology [75, 76], bumpless build-up layer (BBUL) packaging by Intel [77] and self-aligned wafer-level integration technology (SAWLIT) [78]. All these techniques generally share similar steps for the integration of chips. Chips are embedded in etched silicon cavities in carrier substrate followed by coating of a passivation layer on top of the chips and the substrate. The chip is embedded in the substrate so that both top surfaces of the chip and substrate are leveled on the same plane and surface film metal interconnects are fabricated with photolithography. Therefore, when the microfluidics is designed or integrated, the chip and the substrate can be simply considered as a single flat substrate with active sensing region located at the chip area.

In fact, the similar concept has been developed in the die handling and testing area, named reconstructed wafer, wafer level embedding technology or molded reconfigured wafer [79-82]. These technologies mold polymer around the die, usually known good die, to form a wafer with embedded die for reduced package and test cost and other integration and packaging needs. This

technique also can serve as a possible solution to integrate CMOS and microfluidics because it extends the CMOS chip surface although they were developed for die handling and testing purposes.

3.3 Requirements of packaging for the integration of microfluidics and CMOS for high throughput biosensor analysis

To realize high throughput biosensor analysis, the integration of microfluidics and CMOS is needed to take advantages of both technologies. Microfluidic imposes a restraint because its structures occupy a large surface area of a few cm^2s compared to the millimeter sized CMOS die. The dimension of CMOS die can not be increased up to centimeters because the cost of the CMOS die increases exponentially as the size increases. Thus, in order to incorporate microfluidics into the microsystem, the area of the platform should be increased. Also, it is desired to allow multi channel microfluidics on the chip surface to enable high-throughput analysis. To both operate the CMOS circuit and detect the sensing signal from biointerface on the CMOS chip, the CMOS die should be electrically connected to external electronic instruments and on-chip sensing electrodes.

3.4 Chip-in-carrier integration

By analyzing the electronic packaging technology and requirements of packaging for the integration of microfluidics and CMOS, embedded chip with extended substrate and interconnects is the best candidate for the chip packaging. The extended substrate and interconnects have been described in Sec. 3.2.2 and they can allow microfluidics integration. By incorporating microfluidics, CMOS electrochemical circuits, and packaging technology, a new chip-in-carrier CMOS microfluidic electrochemical biosensor (CMEB) microsystem is designed

for high throughput analysis. As shown in Figure 3.1, the CMOS chip is extended with a carrier platform to obtain more surface area beyond the CMOS die, allowing room for multiple microfluidic inlets/outlets. The carrier also provides planar routing of electrical signals to connect CMOS I/O pads to electrical contacts on the periphery of the carrier platform. This method is called chip-in-carrier integration.

The general structure of chip-in-carrier is to embed the chip in an extended carrier and provide a flat platform for further integration or stacking of other components. The chip-in-carrier structure is not only limited to pBLM formation and characterization but can be applied to other microfluidic chemical or bio sensors with CMOS instrumentation electronics. It is also possible to integrate sensors of other modalities such as temperature and humidity. As long as the existing sensor technology has a large footprint compared to the size of the CMOS electronics, the chip-in-carrier structure can be used to facilitate the integration.

3.4.1 Requirements and challenges of the chip-in-carrier integration

The first and the most important part of the microsystem integration is the chip-in-carrier fabrication. The carrier provides two major functions for the microsystem. The carrier contains the CMOS chip that should be capable of full functions through reliable interconnects and the carrier allows microfluidic structure to be placed on it. The interconnects are realized by the surface metal routing, thus, top surfaces of the carrier and the CMOS chip should be on the same plane so that the surface metal routing could continuously run from the contacts of CMOS chip to the peripheral I/O pads. The flatness of carrier and CMOS chip surfaces is also important for the following microfluidic structure fabrication. Other factors to consider are the feasibility of the process and the cost effectiveness.

Up to date, there are mainly two ways to construct the carrier for the embedded chip. One is silicon carrier as described in Section 3.2.2 and the other is polymer carrier that molds around the chip. The pros and cons of both approaches will be discussed in the following section.

3.4.2 Comparison of silicon carrier and epoxy carrier

To implement chip-in-carrier structure, silicon wafer or polymer wafer has been reconstructed with chips embedded in them as discussed in section 3.2.2. Both silicon and polymer wafer techniques could be used to make the carrier in our project.

Silicon carrier fabrication relies on the established semiconductor processing tools. Several groups also have reported silicon carrier based chip packaging for sensor integration [47, 83, 84]. One of the key procedures is the deep reactive ion etching (DRIE) of silicon wafer to create the holes. The chip is embedded in the holes with polymer or spin-on-glass sealing the gap. The hole

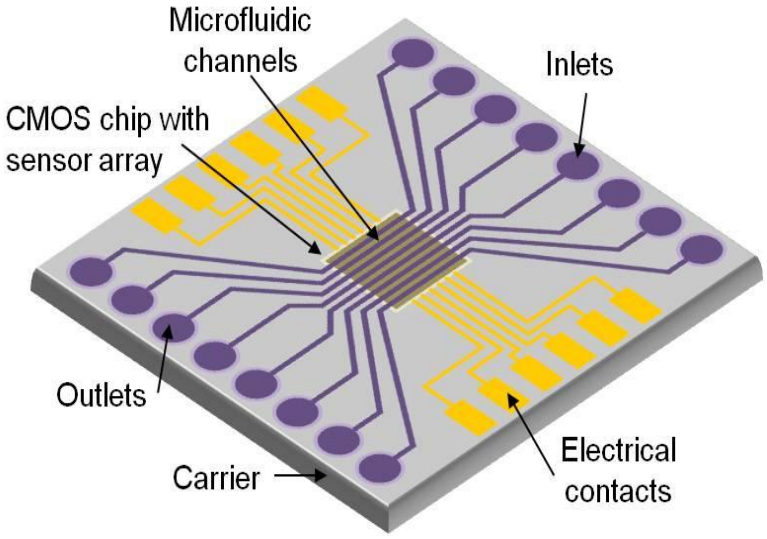


Figure 3.1. Conceptual view of an integrated CMOS-microfluidic instrumentation array.

should match the chip as exactly as possible in order to minimize the use of sealant. The chips are manufactured by dicing a large wafer and the sizes among chips can easily vary by tens of micrometers. Therefore, it is not practical to make a universal photomask for DRIE silicon etching and each chip should be individually considered for masking. The DRIE process is also expensive and often only available in the cleanroom environment. However, in a wafer level carrier, the silicon carrier does not produce much stress because of minimal use of polymer filler.

On the other hand, polymer carrier is simply made by molding polymer around the chip so that the carrier will automatically align to the chip. This process does not require lengthy photolithography and silicon etching process. The polymer composite can be adjusted according to different applications. The cost is also low and only needs hot plate or oven to cure the polymer. If the carrier is made into a wafer scale, the mismatch in the thermal expansion coefficients (CTE) between silicon and polymer could cause deformation of the carrier and the composition of the polymer should be carefully adjusted to match the CTE.

In our project, our goal is to integrate the electrochemical biosensor microsystem and it does not necessarily have to be done in wafer level process. Therefore, the mismatch of CTE and deformation of the polymer carrier are not significant problems while the complexity and cost of the silicon carrier do not make it the better choice. Thus, we will use the polymer carrier as the scheme to package the chip. Recently, a group reported polymer based carrier packaging for single die [85]. The process relied on unreliable manual handling of chip to make the carrier and was not suitable for mass production.

3.5 Process of polymer chip-in-carrier integration

3.5.1 Overview of fabrication procedure

The carrier and chip surfaces should maintain at the same flat plane. Therefore, both polymer and chip should be aligned against a guiding flat substrate when being molded. Meanwhile, after the polymer is molded and cured both the carrier and the chip should be removed from the guiding substrate. Another handling substrate could be used to help hold the fluidic polymer before curing and handling.

The general fabrication procedure of the polymer chip-in-carrier could be summarized as shown in Figure 3.2. First, the chip is bonded to the glass holder with its top surface facing the holder. The bonding should be temporary in order to release the chip and the polymer carrier later. The bonding material needs to be immiscible with molding polymer. Second, another glass holder is placed and pressed on top the chip and polymer is filled into the gap between the two glass holders. In this step, the bonding of the chip should be good enough so that the polymer does not smear under the chip. Third, the liquid phase polymer is then cured and the temporary bonding layer is dissolved. The top glass holder, polymer carrier and the chip are then released from the bottom glass holder. The top surfaces of polymer carrier and chip are supposed to be flat and seamless. All the process should be compatible with CMOS.

This general procedure has been reported in the past [79, 86]. However, the key information of the process, such as the temporary bonding tape, polymer composition and die handling tool, are not reported and the work can not be exactly repeated. Therefore, the development of the process is needed to identify the materials and details of the work. The development starts with the polymer selection for the carrier.

3.5.2 Polymer for the carrier: SU8 and epoxy

The main purpose of the polymer in this work is molding around the chip to make the carrier. As the mostly used polymer structural material in MEMS microfabrication, SU-8, a negative photoresist, is considered. SU-8 is available in a wide range of viscosities and is suitable to form thick layers and high aspect ratio structures [87]. Typically, SU8 is soft baked to evaporate solvent away before going through UV exposure and cross link of the SU8. In our process, with the presence of the handling glass, the SU8 is sandwiched between two glass holders and the solvent could hardly evaporate during soft bake. Thus, the baking time is greatly increased and the SU8 is almost impossible to get ready for the upcoming UV exposure. Due to this drawback of SU8, SU8 is not suitable for the carrier material.

On the other hand, epoxy is investigated as the carrier material. The most favorable fact of the epoxy is its simple curing method. The epoxy can be cured without baking at room temperature or faster at higher temperature. Also, some epoxies are bio-compatible and available in various viscosities and glass transition temperatures to work in different conditions. A biocompatible epoxy EPO-TEK 302-3M (Epoxy Technology, Inc.) is selected initially because of its low viscosity that is desirable to fill the narrow gaps between two glass holders.

3.6 Temporary bonding material

As shown in the Figure 3.2, a temporary bonding material is used to bond the chip to the glass holder. A few requirements for the material are obvious. The temporary bonding material should be immiscible with epoxy and can be dissolved after the epoxy is cured while not deteriorate the epoxy. The bonding should be good enough preventing epoxy smear under the chip. Intuitively, the fluidic temporary bonding material should be as thin as possible so that

carrier and chip surfaces remain as flat as possible. Other subtle requirements of the material are going to be revealed as experimental studies are carried out.

3.6.1 Photoresist

Photoresist is usually used as a sacrificial material for lift-off process in microfabrication. Photoresist is also used as an adhesive layer and can be dissolved by acetone or photoresist stripper. Unfortunately in my experiment it is found that baked photoresist mixes with epoxy during the molding step. Therefore, photoresist is disqualified as the temporary bonding material to be used, at least, alone. However, photoresist is still useful if there is an intermediate layer between photoresist and the epoxy. Parylene, as a good insulation thin film material, can be

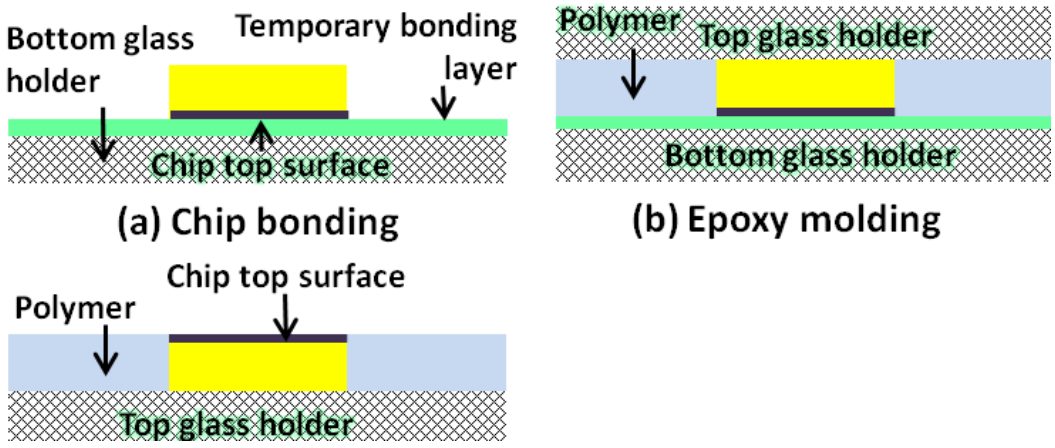


Figure 3.2. Process flow of polymer chip-in-carrier. (a) The chip is temporarily bonded to a glass holder with top surface facing the holder. (b) Top glass holder covers and presses on the top the chip and the polymer is filled into the gap and cured. (c) The temporary bonding layer is etched or dissolved and the top glass holder, chip and the polymer carrier are released from the bottom glass holder. The polymer carrier and chip surfaces are in flush.

coated after the chip is bonded, serving as the intermediate layer.

The process flow is as shown in Figure 3.3. First, photoresist is spin coated on the glass

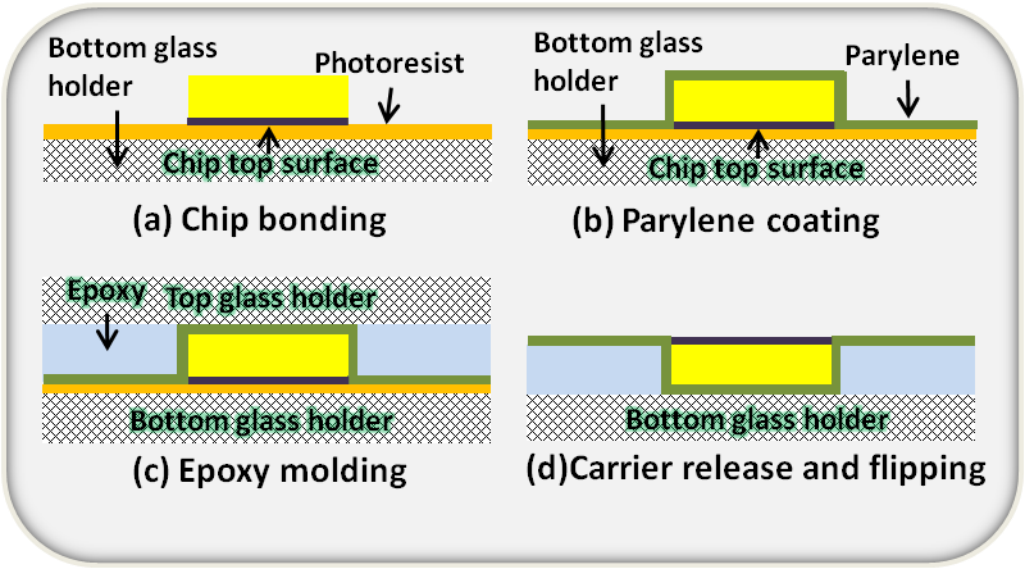


Figure 3.3. Process flow of epoxy chip-in-carrier with Parylene coating. (a) The chip is temporarily bonded to a glass holder with top surface facing the holder using photoresist. (b) 5μm Parylene is deposited over the chip and photoresist using vapor deposition. (c) A top glass holder is pressed against the chip and epoxy is filled in the gap between the two glass holders. (d) The photoresist is dissolved in acetone to release the top chip-in-carrier and the bottom glass holder is detached. The chip is now embedded in the epoxy carrier and surface of the carrier is covered with Parylene.

holder and the chip is bonded to the glass holder with its top surface facing toward the glass holder, as shown in Figure 3.3 (a). The photoresist is baked on hotplate at 110℃ to bond the chip and the chip should be pressed uniformly to avoid weak bonding point. Second, a thin 5μm Parylene film is deposited on the chip using room temperature vapor deposition as shown in

Figure 3.3 (b). The Parylene film works as an intermediate insulation layer which separates the photoresist film with the epoxy. Without the Parylene film, the epoxy will blend with photoresist and the photoresist loses function as the temporary bonding layer. Then, another glass holder is placed on top of the chip, perpendicular with respect to the bottom glass holder. Epoxy is then dispensed into the gap between the two glass holders to form the carrier. The epoxy is supplied at one end of the gap and the epoxy will travel forward through the gap to the opposite end by capillary effect, which is as shown in Figure 3.4. In this case, the glass holder is a 1”×3” glass slide and the two crossed glass holders define a 1”×1” area for the epoxy carrier. Because the epoxy fills the gap as the meniscus travels from one side to the opposite side, it can minimize trapped bubbles inside the epoxy carrier. After the epoxy is cured, at room temperature or faster at higher temperature on hotplate, the epoxy carrier is ready for release. To release the epoxy carrier and dissolve the photoresist temporary bonding layer, the whole structure is immersed in acetone bath and cleaned by DI water.

Initially, Shipley 1813 is selected as the photoreisist to be used. Shipley 1813 is a thin positive photoresist generally used in the photolithography which can be spin coated as thin as 1~2μm. Shipley 1813 also works well as the bonding material when handling die or other small device for spin coating. The Shipley 1813 is spin coated as thin as 1.3μm at spin speed of 3000rpm. However, after the epoxy is molded and cured, the area to release is relatively large at 1”×1” in this case and the thin photoresist layer can not be effectively dissolved by the acetone throughout the area. It is found that even after 24 hours of soaking, the photoresist still can not be fully dissolved. Consequently, a thicker photoresist layer is needed to fully release the 1”×1” carrier area.

AZ4620 is a type of thick photoresist that measures ~7-8µm thick when spin coated at 3000rpm. Therefore, instead of the Shipley 1813, AZ4620 is spin coated on the glass holder to have a thicker release layer. The rest of the process follows exactly the same as the ones shown in Figure 3.3 (b-d). In this method, the epoxy carrier is able to be successfully released in the acetone bath. The chip-in-carrier structure is inspected carefully, especially at the chip-to-carrier boundary region. A discontinued surface profile is observed along the chip-to-carrier boundary and the surface transition is often very abrupt as shown in Figure 3.5. The gap is measured using

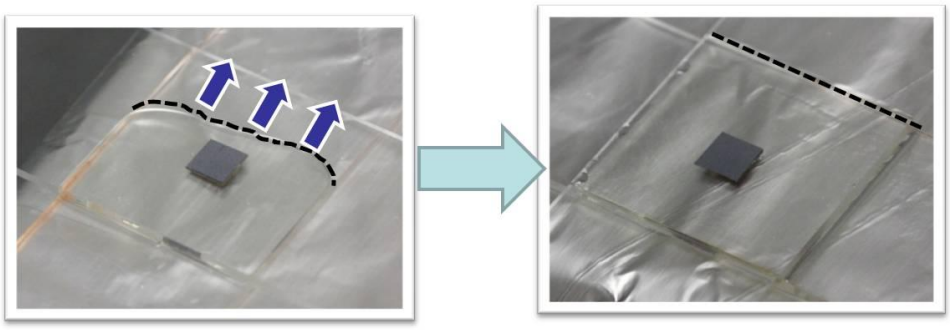


Figure 3.4. Top view of the silicon chip sandwiched by the two glass holders while the epoxy is filled between the two 1”×3” glass slides from one side and the epoxy meniscus (dotted line) travels through the gap by capillary force (left figure) until completely filling the overlapping area (right figure).

surface profilometer and the gap is as deep as 6µm. This deep gap is highly undesired should be minimized because this causes difficulty for surface metal routing to continuously cross the boundary.

This problem is caused by the push-out effect of the adhesives at the bonding interface as shown in Figure 3.6. The push-out photoresist occupies the space, stopping the epoxy from

molding seamlessly around the chip and creating valley between the chip and the carrier. The thicker and more fluidic the photoresist layer is, the more photoresist is pushed out. Therefore, for the thick AZ4620, predictably more push-out effect occurs. To verify the push-out effect of AZ4620, the bonded chip is inspected under scanning electron microscope (SEM). The AZ4620 photoresist is spin coated on the glass holder at 3000rpm and the chip is directly bonded to the chip with pressure while being baked on hotplate for 3 minutes at 110℃. The pressure is necessary to ensure reliable bonding to avoid the penetration of Parylene or epoxy into the chip

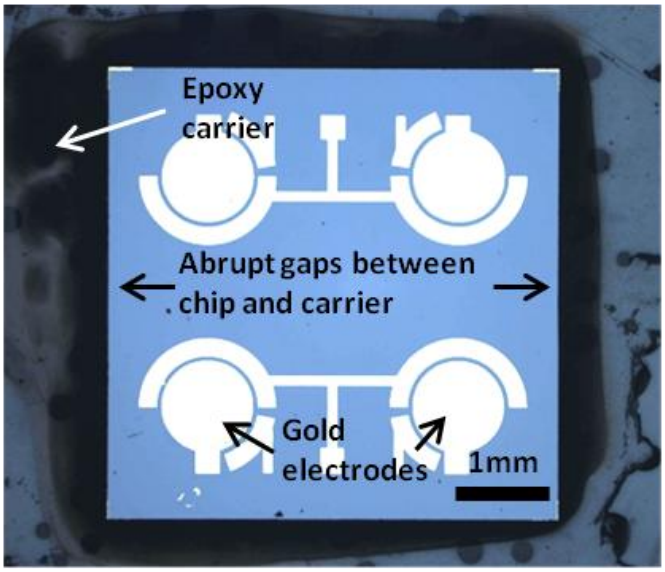


Figure 3.5. Chip embedded in the epoxy carrier using AZ4620. Abrupt gaps between the chip and carrier are observed.

surface. In the SEM image as shown in Figure 3.7, the AZ4620 is pushed out around the chip edges and accumulates on the sidewall of the chip. These photoresist later will be removed, leaving gaps and valleys between the chip and the carrier. Knowing that a sub-micron metal thin film interconnects would run between carrier and chip, these gaps are too large to overcome. An

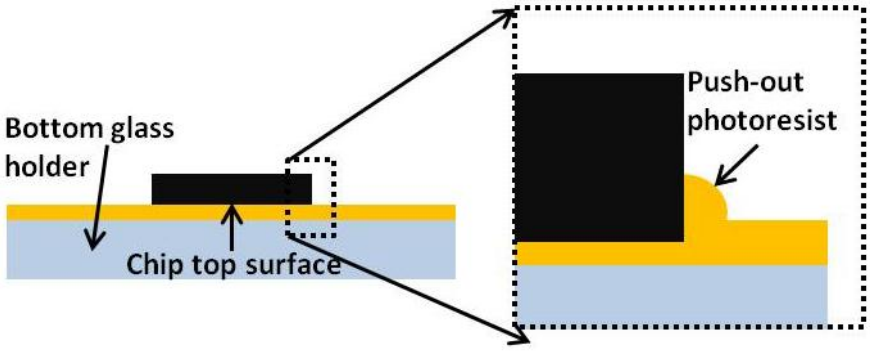


Figure 3.6. The push-out effect of photoresist. The photoresist is pushed out when the chip is bonded the chip.

additional planarization layer could reduce or eliminate the gaps for smoother transition.

Until now, two methods using two types of different photoresists have been designed and tested. In the first method, the thin Shipley 1813 photoresist makes the carrier release impossible.

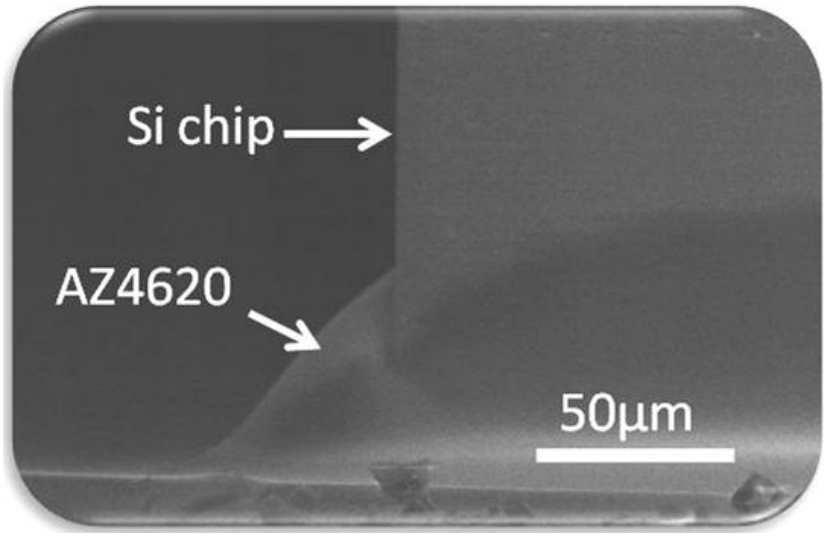


Figure 3.7. SEM image of the push-out effect of AZ4620 photoresist. The Si chip is bonded on the glass slide with AZ4620 photoresist.

In the second method, the thick AZ4620 photoresist causes push-out effect mainly because of its thickness. Thereby, a method that compromises both approaches is developed, which is as shown in Figure 3.8. This method uses thin photoresist to minimize the push-out effect while limited the area coated by photoresist to the extent of the chip. The process is similar to the previous

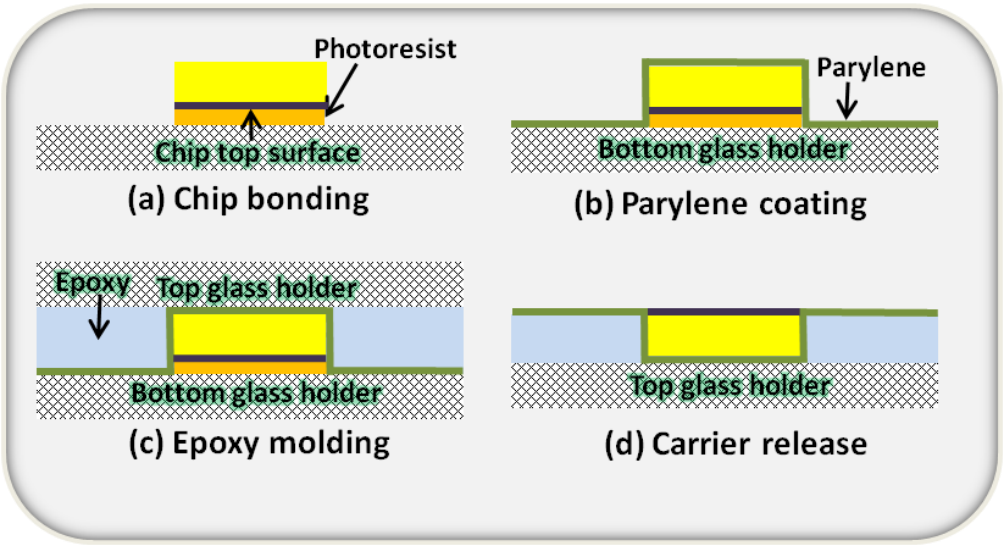


Figure 3.8. Process flow: AZ 5214 photoresist was spin coated on glass holder and the chip was bonded to the surface (a); 5μm Parylene was deposited (b); another glass holder covered on the top and the epoxy was filled into the gap and cured for 3 hours at 65℃ (c); The packaging was released and AZ 5214 was rinsed off (d).

ones except a few differences. Each chip is then bonded face down to a 1”×3” glass holder using a spin coated layer of AZ 5214 photoresist. The photoresist beyond the chip is then developed, leaving photoresist only under the chip, as shown in Figure 3.8(a). This is achieved by the self masking of the chip for the UV exposure. This approach ensures that each chip is bonded with exact same area of photoresist layer. A layer of 5μm Parylene is then coated over the chip and glass holder, as shown in Figure 3.8(b). Then, a second glass holder is then placed orthogonally

on the top, and biocompatible epoxy EPO-TEK 302-3M (Epoxy Technology, Inc.) is injected into the gap between the holders and cured at 65℃ for 3 hours, as shown in Figure 3.8(c). The adhesion between Parylene and glass is weak without any surface treatment, so the Parylene can be easily peeled off even in water. Notice that the silicon chip is entirely encapsulated by Parylene and photoresist during this release process to protect CMOS circuitry. Once the bottom glass holder is removed, the structure is then immersed in acetone to dissolve the photoresist on the chip's surface, as shown in Figure 3.8(d). With this process a gap is still possibly present between chip and the carrier but is small enough within ~1μm range. This gap can be overcome by adding another planarization layer. However, there are some rough edges by torn Parylene along certain side of the chip because the photoresist bonded chip is pulled with force and some Parylene is already bonded to the thin photoresist film during Parylene deposition. This issue is especially critical because this occurs at the chip-to-carrier transition region. Therefore, if high quality is required, steps to clean the torn and rough Parylene film edges are needed using plasma etching.

3.6.2 Parylene

In the process above, the weak adhesion between the Parylene film and glass surface is utilized for the release process. It implies that it is possible to completely only use the Parylene as the temporary bonding and release layer without the use of photoresist.

A Parylene-only process is then designed as shown in Figure 3.9. The chip is placed on a glass holder with its top surface facing downward and thick ~10μm Parylene is deposited on the chip. The Parylene deposition is isotropic and the Parylene can diffuse into the gap between the chip and glass holder. Then, similar process is followed to mold epoxy around the chip and the

chip-in-carrier structure is released in water. The chip surface is covered with Parylene layer and this layer is etched away by plasma to expose the on-chip sensors. This process eliminates the photoresist and because the chip is homogeneously coated by Parylene and the Parylene can be readily patterned and etched by photolithography and oxygen plasma, there are no rough or torn Parylene edges.

However, overall, the plasma etching of Parylene is time dependent and the heat generated by the high power plasma could affect the carrier structure because of the CTE mismatch

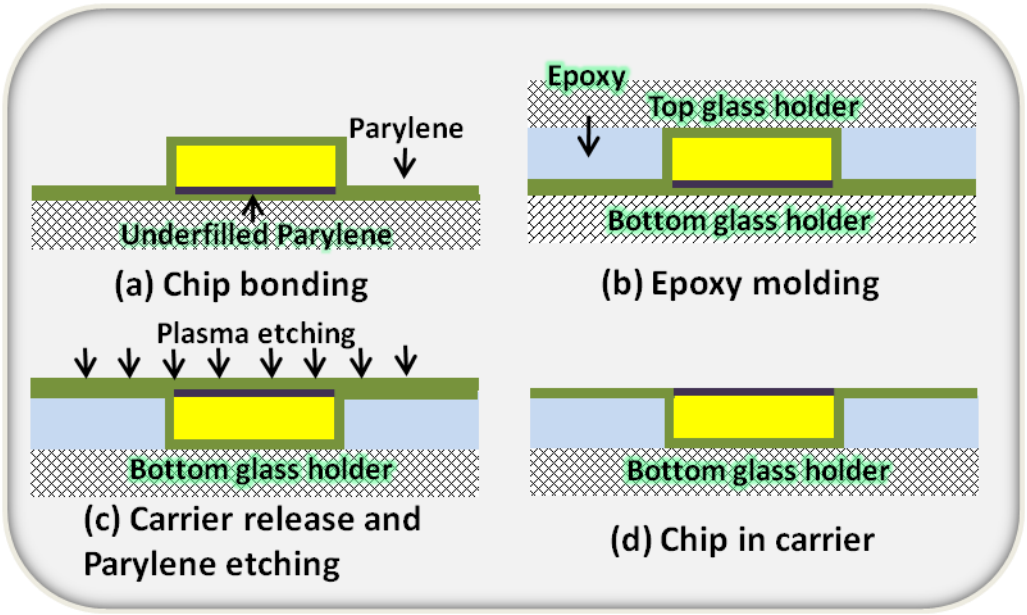


Figure 3.9. (a) Chip is placed on a glass holder with its top surface facing downward and 10µm Parylene is deposited; (b) A second glass holder is placed on top of the chip and epoxy is filled and molded around the chip; (c) The chip-in-carrier structure is released in water and Parylene is etched by plasma to expose the chip surface; (d) The final device has the chip in the carrier and the carrier surface is Parylene.

between epoxy and Si and low glass transition temperature of epoxy. Also, an important fact is that the deposition of Parylene can take a long time if thick film is needed, e.g. 10µm, and it requires dedicated equipment for deposition which is not always easily accessible.

Through the experiments above, it becomes clear that the temporary bonding material is an important factor to have a smooth surface transition. In the processes using photoresist, Parylene is used as the intermediate layer because the epoxy blends with photoresist. Parylene provides other benefits including an excellent insulation protection material for the chip and easy to pattern but long time oxygen plasma etching in vacuum chamber could cause heat up the device and cause thermal issues to the device. Therefore, an alternative approach that can avoid the use of Parylene is beneficial in terms of simplifying the process and cost reduction. In the following section, a temporary bonding material, Waferbond, will be introduced to replace the photoresist and Parylene.

3.6.3 Waferbond

Waferbond is a specially designed temporary bonding material from Brewers Science that is for die and thin wafer handling and enables back-end-of-line (BEOL) processing with standard semiconductor equipment. Waferbond is a low-viscosity solution in solvent to provide planarization during spinning and forms coatings 10 to 27µm thick. Waferbond is resistant to acids, bases, and most solvents. Most importantly, Waferbond does not mix with epoxy, thus, an intermediate layer, like Parylene, is not necessary when molding epoxy. The epoxy can be directly applied on the Waferbond layer without interaction between epoxy and Waferbond.

To verify the quality of the Waferbond coating and push-out effect, a chip is bonded to a substrate using spin-coated Waferbond. The Waferbond is spin coated on a silicon substrate at

2500rpm and the thickness is about 8μm. The Waferbond is first soft baked on a hotplate at 120℃ and 180℃ each for 2 minutes. The chip is then bonded on the substrate without pressure by baking the Waferbond on hotplate at 180℃ for 2 minutes. To see the push-out effect of Waferbond, the bonded chip is inspected using SEM as shown in Figure 3.10. The push-out

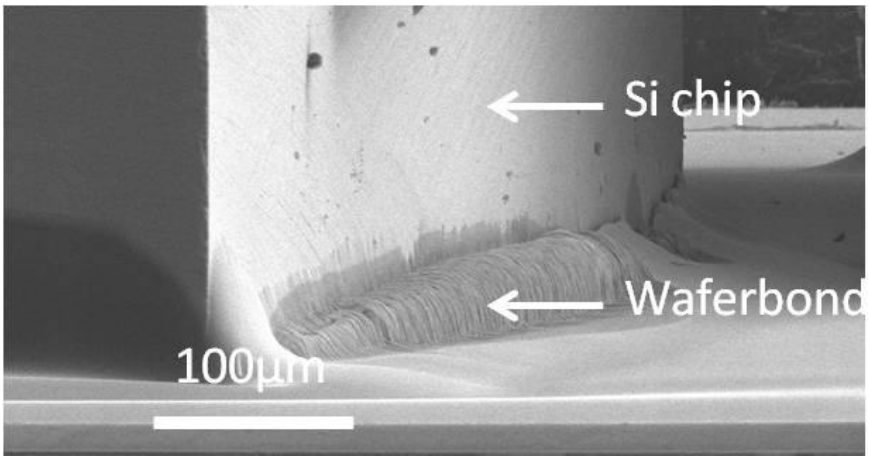


Figure 3.10. SEM image of the push-out effect of Waferbond. The Si chip is bonded on the glass slide with Waferbond.

effect is observed similar to AZ4620. Even though the chip is not pressed to bond, a pile of Waferbond climbs up against the sidewall of the silicon chip thanks to the surface tension. By applying additional planarization layer, the gap created by this push-out effect can be filled.

A process similar to the Figure 3.2 is designed with Waferbond as the temporary bonding material except a few details as shown in Figure 3.11. First, in the step of chip bonding, the chip is gently placed on the Waferbond coating without pressure. That is because the chip would easily slip on the Waferbond coating when pressed with unbalanced force and makes streak marks on the Waferbond coating as shown in Figure 3.12. These streak marks will be transferred to the epoxy carrier, creating unpredictable deep gaps between the chip and the carrier. To release

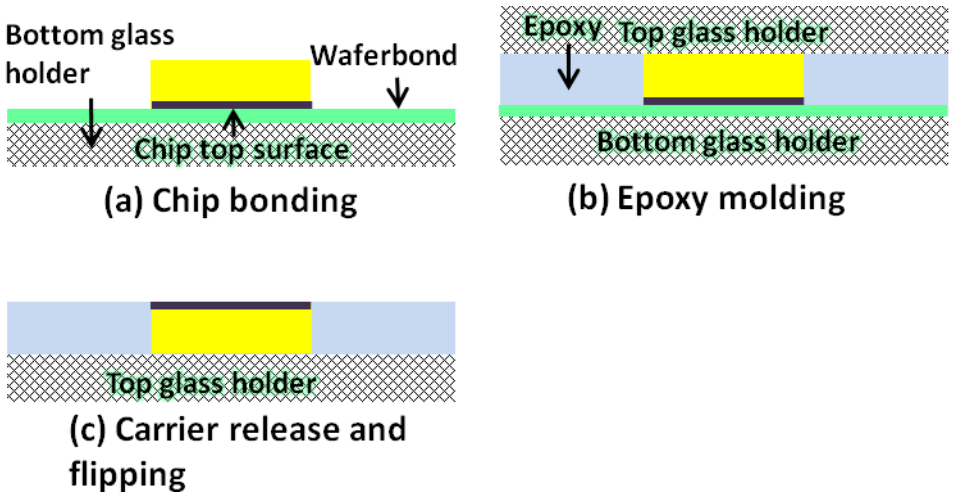


Figure 3.11. Waferbond process. (a) Chip is placed on a glass holder with its top surface facing downward and bonded with spin coated Waferbond; (b) A second glass holder is placed on top of the chip and epoxy is filled and molded around the chip; (c) The chip-in-carrier structure is released in Waferbond remover bath.

the carrier, the Waferbond is dissolved in Waferbond remover bath at 110℃ for 2 hours and then rinsed off at 70℃ for 15 minutes. In the end, the surface of the carrier is epoxy.

One variation of the process which can be very interesting is that the bottom glass holder in the final device can be excluded, making the carrier standing alone with reduced thickness. In particular, the reduced thickness could be desirable in the 3D integration of multiple functional stacks with smaller form factor, which is nowadays the driving motivation in the electronic packaging in order to enclose as many components as possible into small space. To remove the bottom glass holder, the only thing to do is applying Waferbond coating on the bottom glass holder before putting it on the chip and molding epoxy around the chip. The process is shown in Figure 3.13.

3.7 Discussions

The polymer chip-in-carrier designs have been developed and the details of the process have been studied with emphasis on the temporary bonding materials and the polymer. Epoxy was identified as the molding polymer and temporary bonding materials are considered to release the cured epoxy carrier. Photoresist was discovered to temporarily bond the chip and Parylene was found in the process as intermediate layer to separate photoresist from epoxy because photoresist blends with epoxy solution. To better release the large epoxy carrier area, thick

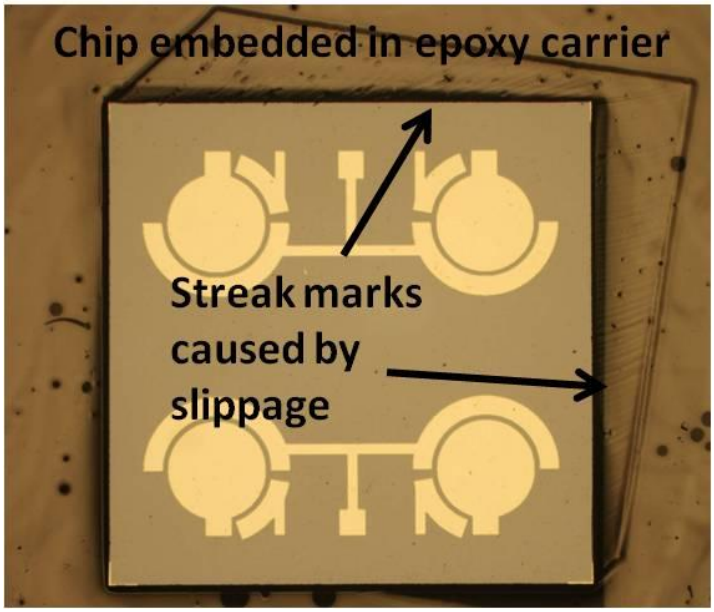


Figure 3.12. Streak marks printed on the epoxy caused by slippage of the chip when the chip is bonded on the Waferbond coating with non-uniform pressure.

photoresist AZ4620 was found to be better material. To reduce the push-out effect, alternative approach using thin photoresist Shipley 1813 was found to limit the photoresist coating only under the chip area and the release relies on the weak bonding between Parylene and glass. Furthermore, a process that used only Parylene was found where the process needs thick

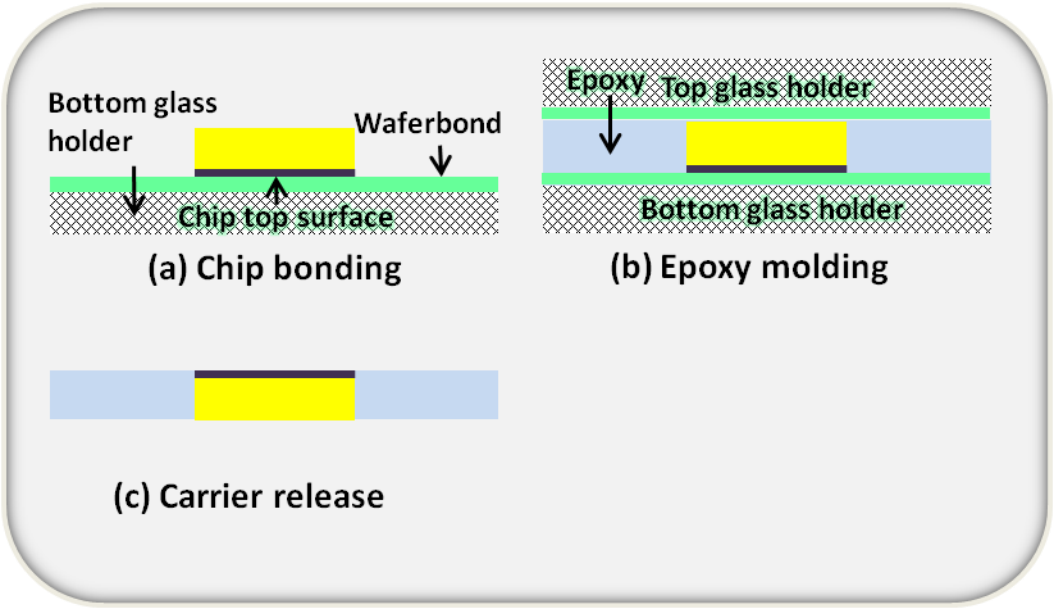


Figure 3.13. Waferbond process for carrier without bottom glass holder. The process is the same as in Figure 3.11 except that the top glass holder is coated with Waferbond and both glass holders are released in the end.

Parylene deposition and long time of Parylene etching. In the end, Waferbond is introduced and found to be the best temporary bonding material because of its reliable bonding and release property.

The continuity of the surface transition between chip and the carrier was found to be very critical in order to make film metal interconnects which is usually only a few nanometers in thickness. Thick electroplating metallization techniques also require thin metal seeding layer which needs to be continuous. In the meantime, the push-out effect of the bonding materials was discovered to cause valleys between the carrier and the chip. Also, the almost vertical chip side wall topology makes the smooth transition even challenging. It is found that the depth of valleys as small as 1µm is possible but it is very difficult to control it within the range of nanometer

metal thickness with consistency at four sides of the chip. Therefore, an additional planarization layer is required to make smooth surface transition from the carrier to the chip. However, the reduction and control of the push-out effect are still important because it determines the planarization process and the subsequent metal interconnect fabrication. The planarization process and the metal interconnects will be discussed in Chapter 4.

4 Chip-in-Carrier Integration: Planarization and Metal Interconnects

To enable on-chip microfluidic electrochemical sensing, the chip-in-carrier integration was developed in Chapter 3 as the first step. The chip is embedded in the epoxy carrier so that it established a flat surface platform for integration. In order to take measurement on chip, the chip should be electrically connected through metal interconnects. The continuity of the surface transition between chip and the carrier is very critical in order to make film metal interconnects which are usually only a few nanometers in thickness. The surface flatness is also preferable for the integration of the microfluidics. However, a few micrometers of roughness on the surface can be overcome by conformal materials (e.g., PDMS or SU8) used in microfluidics structures.

4.1 Challenges of chip-in-carrier integration

To make metal interconnects from the pads on chip to the edge of the carrier, the primary concern of roughness is at the boundary at the edge of chip and carrier which is not perfectly smooth due to the push-out effect described in Chapter 3. The general depiction around the area

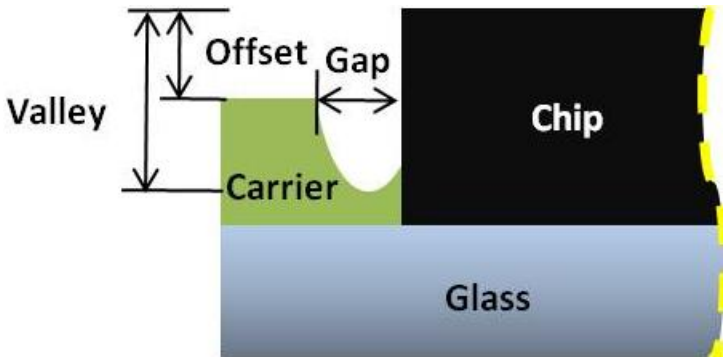


Figure 4.1. Boundary between the chip and the epoxy carrier. The gaps and valleys are caused by the push-out effect.

is represented as shown in Figure 4.1. The offset is the height difference between the carrier and the chip, caused by the thickness of the temporary bonding layer. The gap and valley are the result of the push-out effect. Valley depths ranging from 0 to 10s of microns have been observed. As a result, a carrier surface planarization process is required to alleviate the gaps and valleys between the carrier and the chip and thus allows subsequent integration of thin film metal interconnects and microfluidic structures. In this chapter, two process steps, planarization and metal interconnects, that overcome surface roughness will be presented as shown in Figure 4.2. Microfluidic integration on the chip-in-carrier will be presented with electrochemical measurements within the microfluidic channels.

4.2 Surface planarization

4.2.1 Requirements

From the carrier process using the Waferbond in Section 3.6.3, the thickness of the Waferbond is about 8µm. As a result, offsets, as defined in Figure 4.1, could be as large as 8µm around the chip. The distribution of shapes and topology of the valleys around the chip edges caused by Waferbond push-out effect is largely non-uniform in micro scale because the placement of or pressure on the chip is carried out manually. Even if a special die pick and place tool is used to bond the chip with controlled maneuver and pressure, the gaps and valleys could not be universally the same at four sides of the chip. Meanwhile, the actual CMOS chip often requires interconnects at four sides of the chip. Therefore, to guarantee the chip to be functional, it is required to have smooth surface transitions at all four sides of the chip. The planarization process needs to eliminate the gaps and valleys with smooth transition to allow metal interconnects to run through and reduce offset for subsequent microfluidic integration.

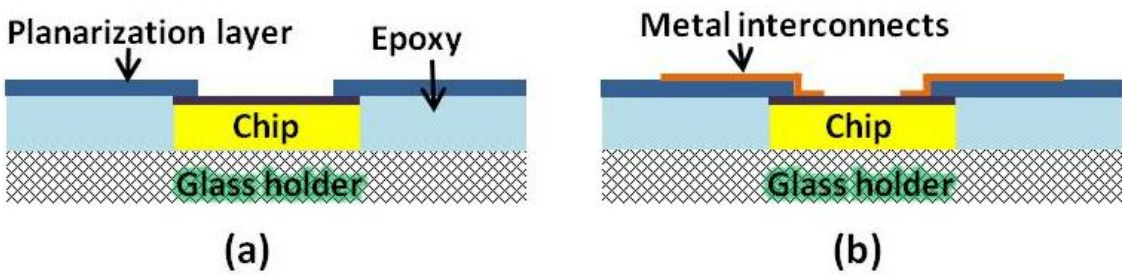


Figure 4.2. Two process steps of the chip-in-carrier integration. The planarization process (a); the metal deposition and interconnects fabrication (b).

Depending on the planarization material, two planarization mechanisms are available.

4.2.2 Planarization materials

The materials used for the planarization need to fill in the gaps and valleys and reduce the offset. The planarization materials are the surface on which metal will be deposited later, so the materials should allow good adhesion to metals. As shown in the Figure 4.3, eventually, the metal interconnects will run from the planarization layer surface to the chip surface to make electrical connections. On this path, the metal interconnects go down a step where the planarization layer stops. This step has to be short in height and smooth enough for the metal interconnects to be continuous. From experimental test, the step height should be less than 10μm to have a reliable continuous metal coverage on the substrate and the step should have positive slope for a sub-micron metal film.

With all these conditions considered, two materials, Parylene and polyimide, were selected to create the planarization layer. They are both film dielectric material which are also bio compatible and resistive to chemicals. Both materials were used to fabricate the planarization layer, and pros and cons of each material are discussed in the end.

4.2.3 Parylene planarization

Parylene, or poly (p-xylylene), is a thin film polymer that is good for insulating electronics. Parylene is chemically inert, permitting conformal coating, and has excellent barrier properties. Parylene C (poly(monochloro-p-xylylene)) has the highest possible biocompatibility rating

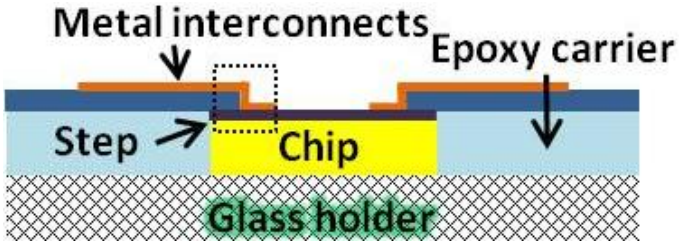


Figure 4.3. Metal interconnects on planarization layer. The metal interconnects cross the step of the planarization layer at the edge of the chip.

among polymers for long term implants and has an extensive history of use in the medical industry. Because of its biocompatibility, biostability, low cytotoxicity and resistance against hydrolytic degradation, Parylene C has been widely used in micro/nano-fabricated devices and microfluidics. Parylene C utilizes a simple chemical vapor deposition method with low process temperature and is compatible with standard microfabrication processes.

The fabrication process of Parylene as a thin film polymer material is uniquely different than usual liquid based polymers. Parylene is a thin film polymer material whose monomer is heated into vapor and condensed on sample surface as it forms polymer. The deposition is omni-directional and the thickness is uniform at all surfaces. The Parylene can be patterned by normal oxygen plasma through a photomask.

Thus, Parylene was used in the planarization process because of its chemical property and

easy fabrication method. 10 µm of Parylene was deposited on the chip-in-carrier device using PVD (PDS 2035CR, Specialty Coating Systems), and Parylene layer was patterned through photolithography and the oxygen plasma etching. Thick 12µm photoresist AZ4620 was used as the masking layer because the etch rates of Parylene and photoresist in oxygen plasma are similar. After patterning, the Parylene layer at the chip area was etched away as shown in Figure 4.2(a). The step created by the oxygen plasma with photoresist as the mask was a positive slope. The patterned Parylene planarization layer on chip-in-carrier device is as shown in Figure 4.4.

4.2.4 Polyimide planarization

Polyimide is a polymer of imide monomers. Polyimide parts are not affected by commonly used solvents and oils, including hydrocarbons, esters, ethers, alcohols and freons. They also resist weak acids but are not recommended for use in environments that contain alkalis or inorganic acids. Polyimide resin is used as an insulating and passivation layer in the manufacture of digital semiconductor and MEMS chips. The polyimide layers have good mechanical elongation and tensile strength, which helps the adhesion between the polyimide layers or

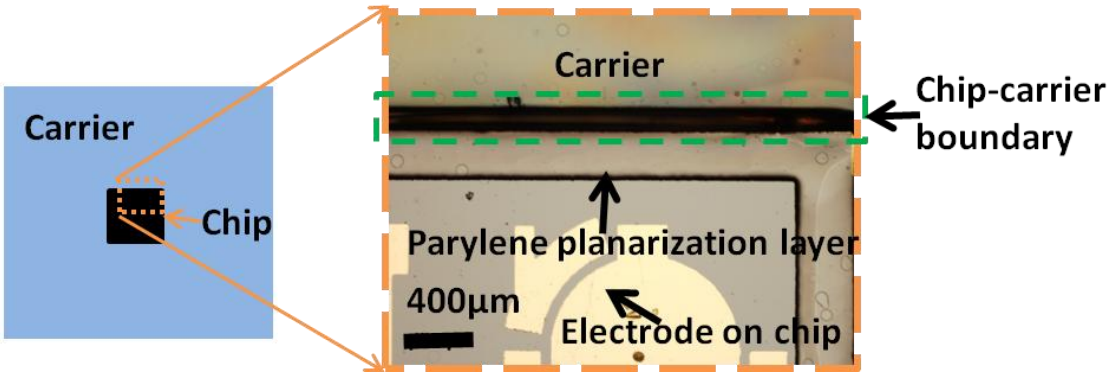


Figure 4.4. Parylene planarization layer on chip-in-carrier device.

between polyimide layer and deposited metal layer.

Polyimide process includes curing steps at temperatures as low as 200℃ and up to 300℃. To allow the process to be compatible with the epoxy carrier, a high temperature epoxy EPO-TEK® U300-2 was selected as the carrier material. The continuous operating temperature of EPO-TEK® U300-2 is -55℃ to 225℃, which is in the range of minimum curing temperature of polyimide.

Polyimide was used to create a planarization layer on the EPO-TEK® U300-2 carrier. Polyimide was spin coated on the device at thickness of 10µm in order to overcome offset. To achieve this thickness, the PI2555 polyimide was spin coated at 1000rpm for three times. Each layer of the PI2555 polyimide was about 4µm. Multiple layers of polyimide blended with each other and resulted in reduced thickness. Polyimide was cured at its minimum curing temperature of 200℃. The polyimide planarization layer is as shown in Figure 4.5.

4.2.5 SU8 planarization

SU8 was also considered as the planarization material which can be used to form thick film that can be used as planarization layer. SU8 is widely used in MEMS fabrication; it is available in a wide range of viscosities and is suitable to form thick layers and high aspect ratio structures [87]. The SU8 is a negative photoresist whose sidewall profile is negative under normal conditions. The sidewall profile could be adjusted by varying the UV exposure time and developing time. SU8 polymer is hard to remove once the pattern is developed because the UV exposure makes the SU8 cross linked and hardened. This is different from polyimide, whose curing occurs at baking process after pattern development.

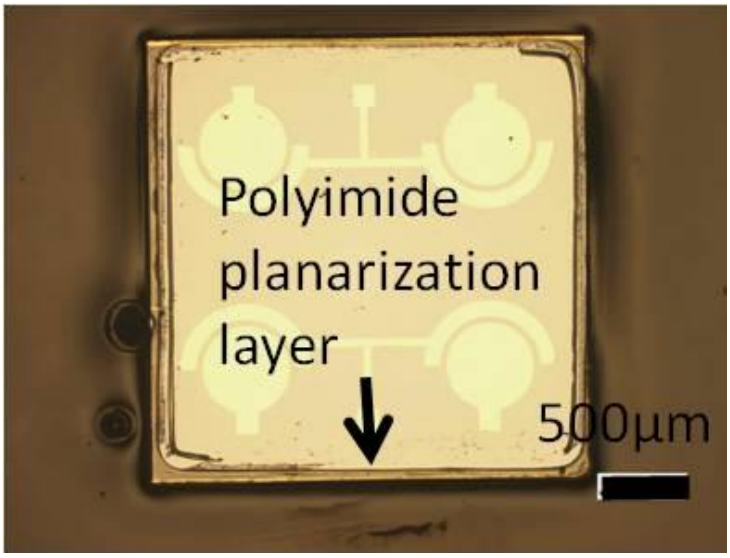


Figure 4.5. Polyimide planarization layer on chip-in-carrier device.

SU8 was spin coated on the chip-in-carrier to create a 10µm layer and soft baked at 95℃ on a hotplate. Extra UV light exposure, more than recommended dose in manual, was done to the SU8 film followed by post bake at 95℃. The SU8 film was then flood exposed to UV light to completely cross link the SU8 photoresist. The quality of the SU8 film was later verified by the successful subsequent metal interconnects.

4.2.6 Discussions

Parylene process requires special deposition equipment and the deposition time for 10µm thickness is hours long because the thickness is determined by the amount of monomers loaded in the deposition equipment. The etching of the parylene was done by oxygen plasma and high etching rate of 0.1µm/min needs high RF power of 300W in our RIE machine. This high power increased the temperature in the process vacuum chamber. In vacuum, the epoxy was observed to get softened easily and deformed at lower temperature than that in ambient atmosphere. The

deformed epoxy carrier destroyed the flatness of the carrier surface. To avoid this problem, a cooling system is required to reduce the heating caused by high power in the vacuum chamber which was not available in our RIE machine.

Polyimide process only includes simple standard fabrication steps of spin coating, baking and wet etching. The thickness of the polyimide is easily adjusted by multiple coatings to the desired thickness, 10μm in my case, which is a quick process. The wet etching of polyimide is also a quick process taking only a few minutes. Polyimide film tends to shrink and become non-uniform over the large surface through the baking process. To reduce the non-uniformity and shrinkage of polyimide film, a clean and uniformly heating hotplate is desired within controlled ambient environment.

SU8 is less prone to non-uniformity due to its relatively higher viscosity which also makes it easier to coat a thicker layer. The process parameters of SU8 need to be carefully characterized for the transparent epoxy carrier and opaque silicon substrate. The processing time of SU8 is also longer than polyimide and SU8 is hard to rework.

As a conclusion, all three materials can be used as the planarization materials depending on the equipment availability, processing time and the requirements of planarization. In this work, both Parylene and SU8 were used depending on the requirements of planarization set by the following metal interconnects process. Polyimide planarization was not adopted later because of low process yield caused by our baking hotplate with limited temperature control.

4.3 Metal interconnects

4.3.1 Requirements

The metal interconnects are needed to make electrical connections for the chip to external instruments. Obviously, the metal interconnects have to be low in resistance and the fabrication process has to be CMOS compatible. Also, the interconnects need to be thick to get reliable connections while reducing the cost of the metal and fabrication process.

4.3.2 Thin film metal interconnects

For sensing electrodes, noble metals like gold and platinum have to be used. However, for metal interconnects, due to the required larger thickness for better conductance and yield, expensive noble metals are not recommended.

Except noble metals, the best metals available for the interconnects are copper and aluminum because of the low cost and its high conductivity. In our chip-in-carrier design, the electrode pad is gold on silicon oxide and both copper and aluminum could be used as the interconnect conductor as long as it can be deposited large thickness at sub micron with low cost. Copper is a better conductor than aluminum though copper cannot be etched with gaseous plasma. A barrier material is usually required for copper interconnects because diffusion of copper into surrounding materials would degrade their properties, for example, silicon forms deep-level traps when doped with copper. The barrier metal must limit copper diffusivity sufficiently to chemically isolate the copper conductor, yet have high electrical conductivity in order to maintain a good electronic contact. Aluminum only requires a thin barrier metal to promote low ohmic resistance when making contact directly to silicon or aluminum layers. Resistance to electromigration, the process by which a metal conductor changes shape under the

influence of an electric current flowing through it and which eventually leads to the breaking of the conductor, is significantly better with copper than with aluminum. The better electromigration resistance allows higher currents to flow through a given size copper conductor than aluminum. The slight increase in conductivity along with this improvement in electromigration resistance makes the copper a better option to drive a full-scale investment in copper-based technologies and fabrication methods for high performance semiconductor devices.

To validate the use of thin films for chip-in-carrier metallization, a device was fabricated using copper interconnects. The starting chip-in-carrier was fabricated using Waferbond process in Figure 3.11 and planarized using 10µm Parylene layer.

Copper interconnects on Parylene planarization: The metal interconnects were deposited by thermal physical vapor deposition. 50Å titanium was deposited as the adhesion layer and 8000Å copper was deposited as the main interconnects using physical vapor deposition (PVD) process. Ten interconnects were patterned to connect the electrodes on the chip. Copper and the titanium were patterned by wet etching respectively. The final device is as shown in Figure 4.6.

Copper interconnects on polyimide planarization: A second device with polyimide planarization layer was also used to deposit copper metal interconnects. 50Å titanium was deposited as the adhesion layer and 8000Å copper was deposited as the main interconnects using physical vapor deposition (PVD) process. The close up view of the fabricated interconnects are as shown in Figure 4.7. The polyimide planarization was not clearly defined at the edge of the planarization due to poor process control. As a result, the resistance of metal interconnects was not consistent for all of 10 interconnects.

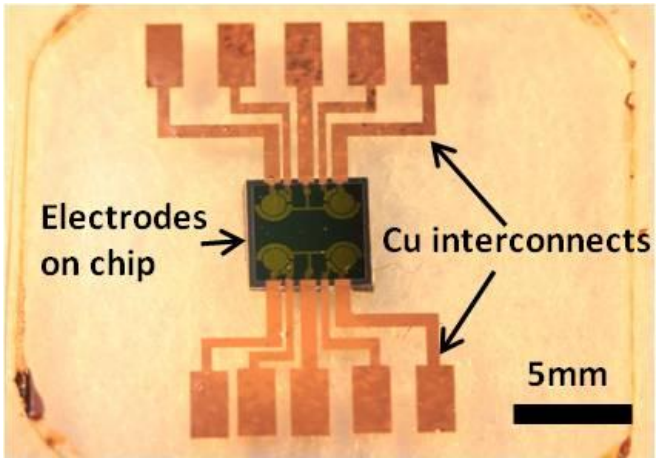


Figure 4.6. Chip in carrier with interconnects. The surface of the carrier is planarized by Parylene.

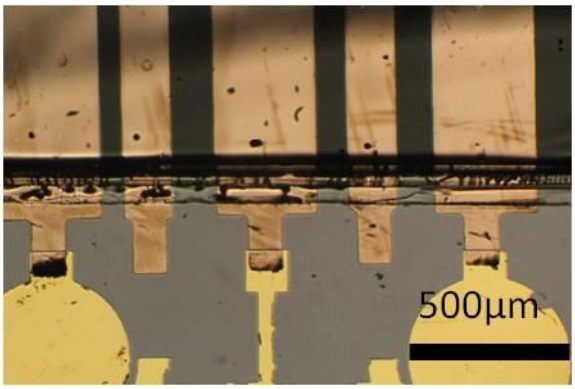


Figure 4.7. Close up view of the copper interconnects on the epoxy carrier. Epoxy chip-in-carrier was made of high temperature epoxy and polyimide planarization layer.

Copper interconnects on SU8 planarization: Another iteration of thin film metal interconnects were fabricated on another chip-in-carrier. The chip-in-carrier was made by the process of Figure 3.8 where Parylene layer was left during the process as the surface of the carrier. The planarization layer was realized by SU8. The device and the close up view of the

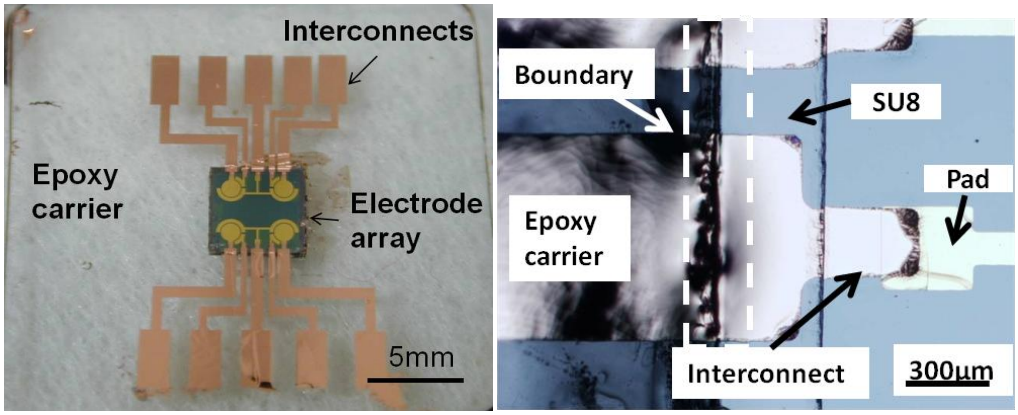


Figure 4.8. Final chip-in-carrier device made by carrier process of Figure 3.8 with 2×2 electrode array, copper thin film interconnects and SU8 planarization (left); Close-up view of the boundary area between carrier and the chip (right).

interconnects near the chip and carrier boundary is as shown in Figure 4.8. The resistance of the interconnects was measured to evaluate the process and verify the functionality of the packaging and smooth transition between carrier and chip. The resistance was measured between two ends of the interconnects on the carrier and the chip. From individual measurements shown in Figure 4.9, the average resistance was calculated to be 3.31Ω, which was similar to the 1.5Ω resistance of a planar copper trace running only on the carrier surface. These results confirmed that the transition between carrier and chip was smooth enough and did not produce significant resistance for interconnects.

Some of the copper interconnects were not continuous at the step of planarization layer. The discontinuous metal interconnects could be the result of the directional nature of the deposition of the physical vapor deposition method. The coverage of the metal deposition can be improved by constant rotation of sample together with angle variation. The improvements are still limited

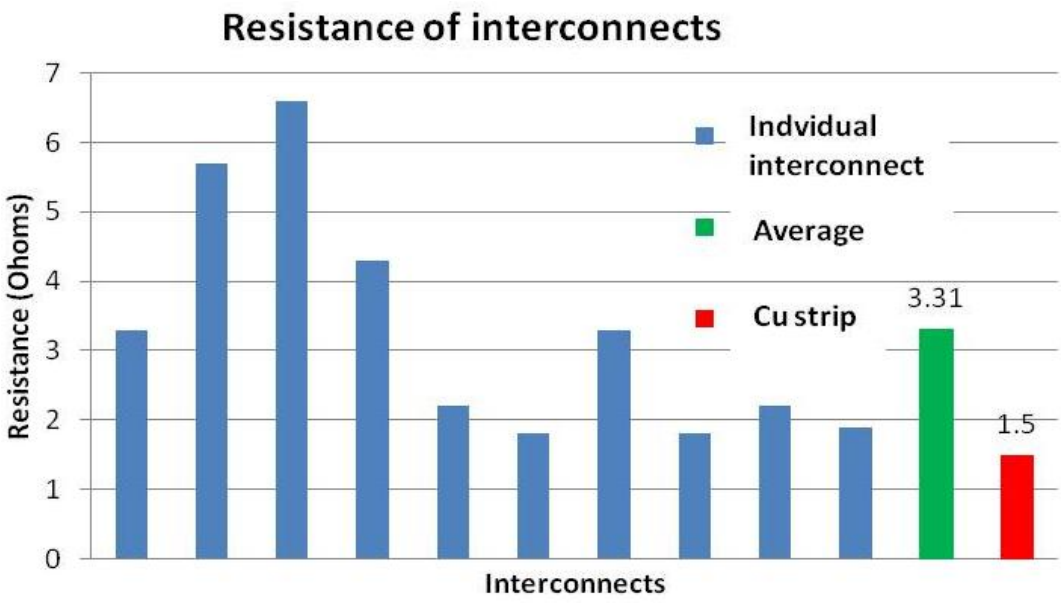


Figure 4.9. Resistances of individual interconnects and their average of 3.31Ω with comparison to a copper strip at 1.5Ω. The resistance is measured directly across the boundary between the carrier and the silicon die.

because the goal is to have all interconnects functional at four sides of the chip. The metal deposited by sputtering system could have better step coverage which could improve the quality of the interconnects. However, the thickness of the metal film is still limited to 1~2μm due to the expensive cost of deposition equipment usage. An alternative way to form thicker interconnects with lower cost is highly desired to improve yield of interconnects.

4.3.3 Screen printed silver ink interconnects

The screen-printing method of metallization is a well-developed technology in which print ink or resin is deposited over a substrate through a predefined mask or screen. Screen-printed planar metallization can deposit layers thick enough to overcome uneven surface profile steps. Additionally, compared to thin film deposition, screen-printing offers a wide material selection

and low process cost. The screen-printing method is similar to the existing lift-off photolithography method. Lift-off process uses photoresist as a sacrificial layer to deposit thin material on the substrate. Motivated by the lift-off process, for chip-in-carrier screen printing method could be modified using sacrificial photoresist as the screen. This modification could eliminate the use of metal mesh screen in conventional screen printing method. The chemical property of the metallic print ink is also important that the solvent of the ink should be immiscible with photoresist and the excessive ink should be removable after the ink is fully cured.

Therefore, a CMOS compatible modified screen printing method was developed to form metal interconnects on a planarized chip-in-carrier as shown in Figure 4.10. The starting chip-in-carrier was fabricated using Waferbond process in Figure 3.11. A first Parylene planarization layer ($Parylene_1$ in Figure 4.10(a)) was deposited to the entire chip-in-carrier assembly and patterned by O_2 RIE process to cover the chip-carrier boundary and the carrier, leaving everything inside the chip bond pads exposed. To start the metallization process, AZ4620 photoresist was spin-coated over the assembly to form a layer thick enough to continuously cover the steps at the boundary and then it was exposed and developed to form a screen-printing mask for planar interconnects that route signals from the chip to the outer edge of the carrier. Silver (Ag) ink, PG-007 (Paru Co), was then screen printed through the AZ4620 mask and a squeegee was used to flatten the film, and then the whole device was baked at 90℃ for 1 hour using a hotplate to cure the silver ink. This process provides an approximately 10μm planar metallization layer, which is thick enough to overcome the height difference between the CMOS die and the carrier. After silver ink was cured, acetone was used to remove the AZ4620 screen mask and reveal the interconnect patterns. In order to insulate the interconnects from the aqueous environment, a second Parylene layer ($Parylene_2$ in Figure 4.10(c)) was then deposited and patterned by O_2 RIE process to form a

protection and insulation layer, leaving only the on-chip biosensing electrodes exposed.

Optical images of the fabricated device after screen-printed planar metallization are shown in Figure 4.11. For further inspection, SEM inspection was also performed to reveal the details. As shown in Figure 4.12, the step height of the chip-in-carrier process was completely filled by the screen-printed metallization layer, with no observable breaks in interconnect traces. To verify electrical interconnection between the on-chip Au electrodes and the connection pads on the carrier, resistance of all Ag ink interconnects was tested using a probe station and digital voltage

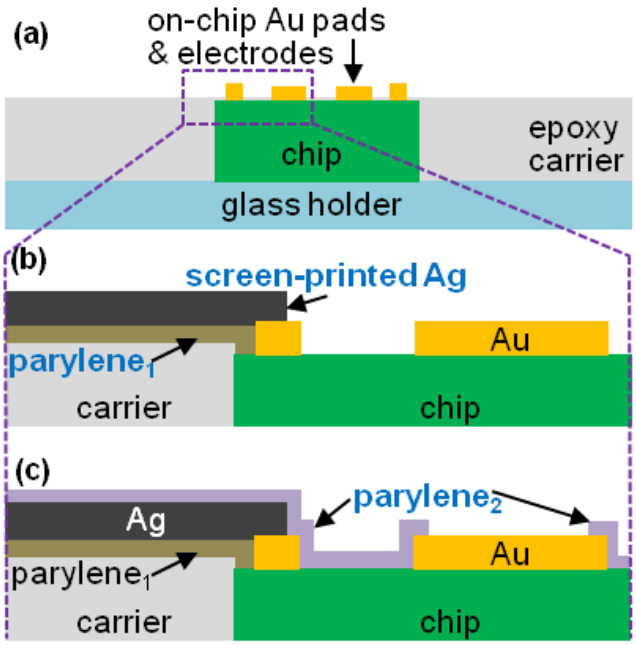


Figure 4.10. Post-CMOS process flow for chip-in-carrier approach with screen printed planar interconnects: (a) device after epoxy chip-in-carrier process [88] using a dummy dielectric-coated Si die to mimic a CMOS chip; (b) first Parylene coating to cover die edge followed by Ag planar electrical interconnects screen-printed on surface of the chip-in-carrier assembly; (c) second Parylene layer to insulation all but sensor electrodes from the aqueous chemical environment. Following these steps, a microfluidics layer can be attached to the surface.

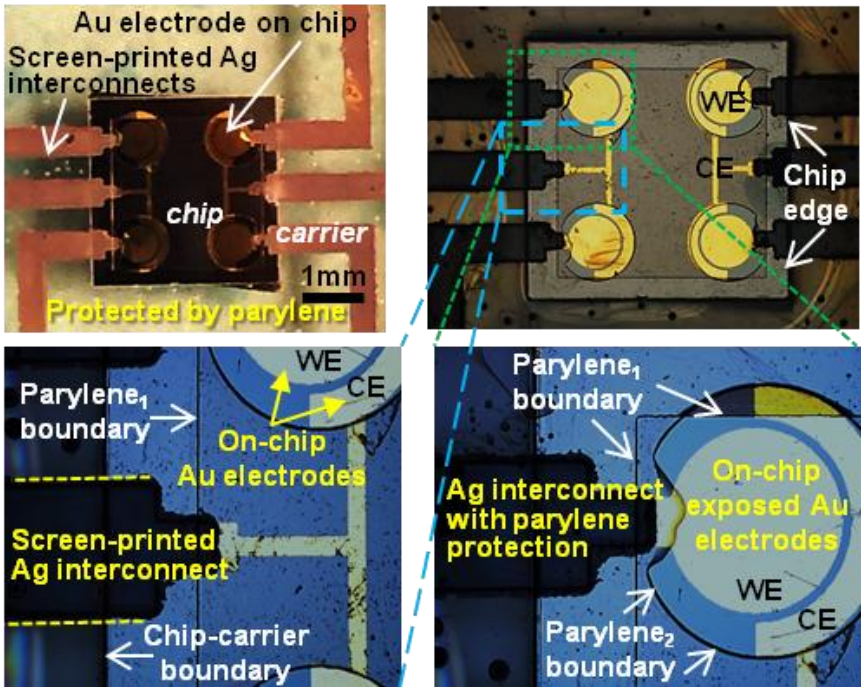


Figure 4.11. Optical inspection of the screen-printed planar metallization layer. Screen-printed Ag interconnects were observed to be continuous even when crossing the chip-carrier boundary.

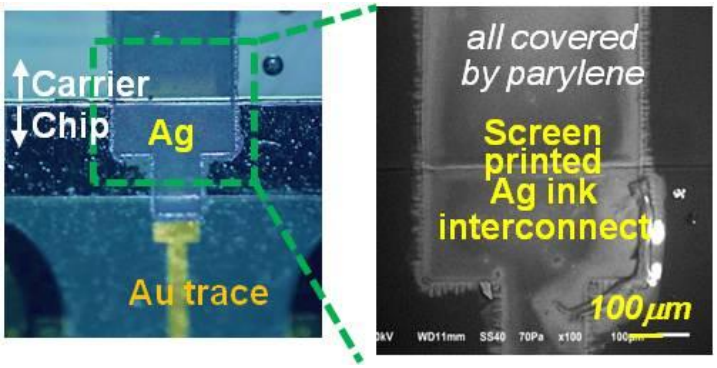


Figure 4.12. SEM inspection of the planar Ag ink interconnect protected by a parylene insulation layer.

meter. Most of the traces showed electrical resistance of around 10Ω, which demonstrated that the screen printing planar metallization process is a reliable method to form electric interconnects for

lab-on-CMOS platforms.

4.3.4 Electrochemical measurements

The chip-in-carrier with planarization and thin film metal interconnects was evaluated for electrochemical sensing. A Parylene passivation layer was deposited and patterned to insulate the Cu wires and leave only the gold electrodes exposed. A commercial instrument (CHI760C, CH Instruments Inc.) was used to perform cyclic voltammetry (CV) measurements using a typical electrolyte solution with 0.1M potassium chloride and 1mM potassium ferricyanide ($K_3[Fe(CN)_6]$). On-chip WE and off-chip commercial liquid junction Ag/AgCl RE and a platinum CE were used as shown in Figure 4.13. 10 cycles of the resulting redox cycling plot is

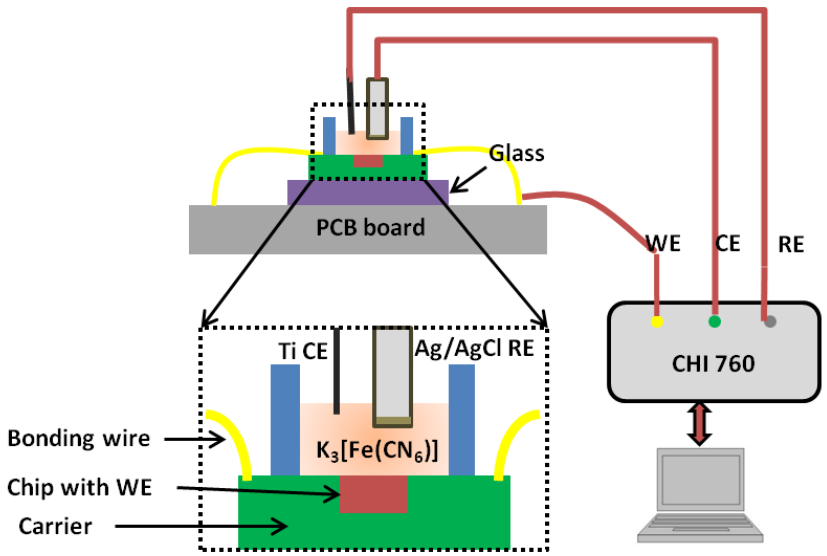


Figure 4.13. Testing setup of cyclic voltammetry measurement of potassium ferricyanide solution with the gold working electrodes on the chip.

shown in Figure 4.14 with clear redox current peaks. The result confirmed that the gold WE remained clean and unaffected after going through the chip-in-carrier fabrication process. The

Parylene insulation was also intact to protect the interconnects.

The chip-in-carrier with silver ink metal interconnects was evaluated for electrochemical sensing as well. A Parylene passivation layer was deposited and patterned to insulate the silver ink wires and leave only the gold electrodes exposed. A commercial instrument (CHI760, CH Instruments Inc.) was used to perform cyclic voltammetry (CV) measurements using a typical electrolyte solution with 1M potassium chloride and 20mM and 25mM potassium ferrocyanide ($K_4[Fe(CN)_6]$). On-chip WE and off-chip commercial liquid junction Ag/AgCl RE and a platinum CE were used. The redox reaction was described in Section 2.2.2. As the concentration of $K_4[Fe(CN)_6]$ changed from 20mM to 25mM, increase of reduction and oxidation peak currents was observed as shown in Figure 4.15. The V_{WEvsRE} was scanned from 0V to 0.5V. The result

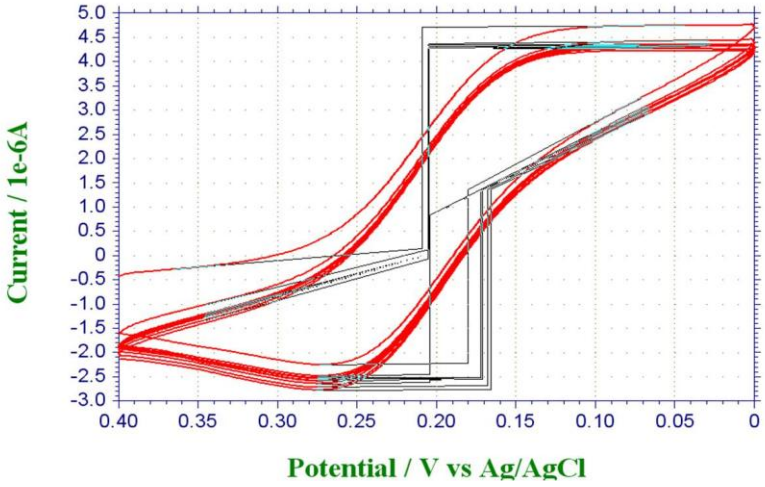


Figure 4.14. Cyclic voltammetry measurement of 1mM potassium ferricyanide solution with the gold working electrodes on the chip with thin film metal interconnects. Off chip RE and CE were used.

confirmed that the gold WE remained clean and unaffected after going through the chip-in-carrier fabrication process.

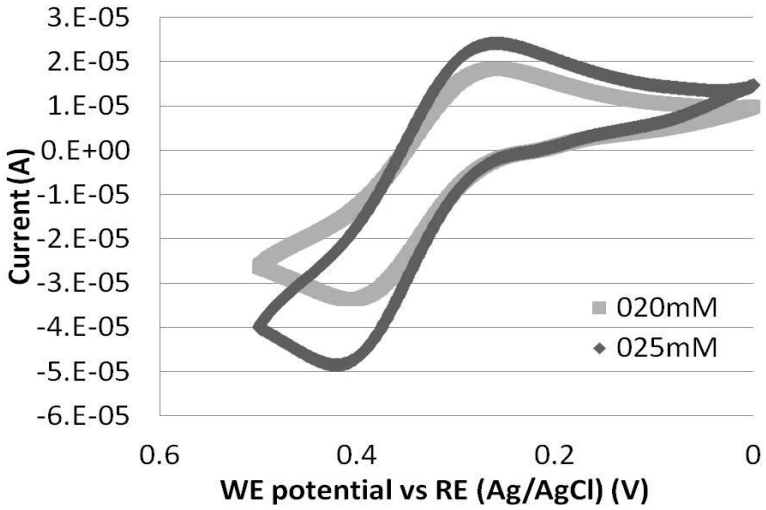


Figure 4.15. Cyclic voltammetry measurements of 20mM and 25mM potassium ferrocyanide solutions with the gold working electrodes on the chip-in-carrier with silver ink interconnects.

4.3.5 Microfluidic leakage test

To demonstrate that chip-in-carrier with metal interconnects are compatible with subsequent microfluidic layer attachment, a microfluidic leakage test was designed. Screen printed interconnects, which are thicker than thin film metal interconnects, could lead to greater surface profile variation on chip-in-carrier. The greater the surface profile varies, the more difficult the microfluidic layer attachment is without leakage.

Thus, to demonstrate the microfluidic capability of epoxy chip-in-carrier for lab-on-CMOS applications, a PDMS multichannel microfluidic structure was prepared. SU8 mold was fabricated

on a silicon wafer and 1:10 ratio mixed polymer of Sylgard 184 PDMS and curing agent was poured over the SU8 mold and cured overnight at room temperature. The cured PDMS structure was precisely aligned with assistance of mask aligner and bonded onto the chip-in-carrier assembly with uncured PDMS as adhesive. The setup for the leakage test is as shown in Figure 4.16. The chip-in-carrier with silver ink interconnects was used for the microfluidic integration as shown in Figure 4.17. Fluid with blue dye was flowed through the microchannel to test if the thick metallization layer created leakage path in the fluidics. Figure 4.17(a) shows that the device allows fluid to flow across a series of screen-printed metal traces on the carrier, and Figure 4.17(b) shows that the device allows fluid to flow from carrier, onto chip, and back

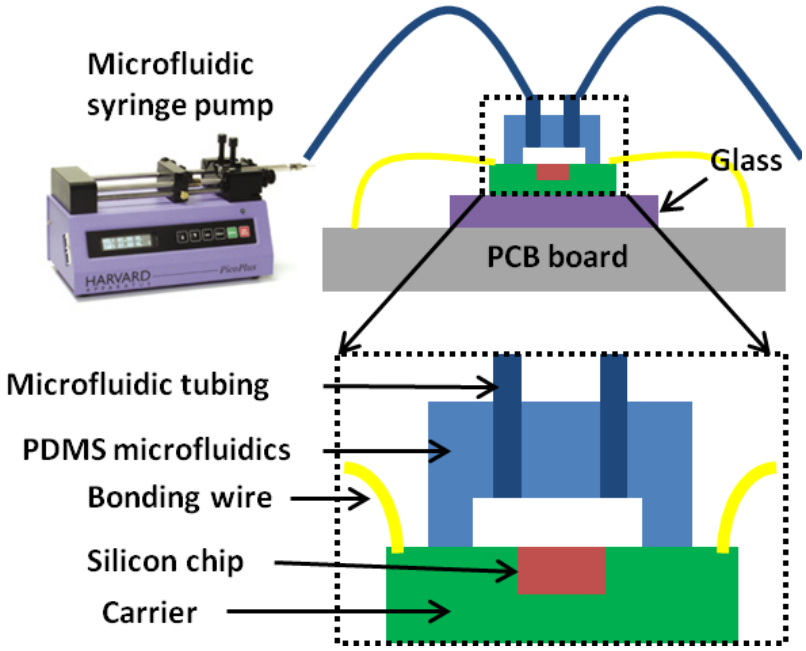


Figure 4.16. Experimental setup of microfluidic leakage test.

onto carrier. No leakage was observed during any of these experiments and the epoxy chip-in-carrier is suitable for lab-on-CMOS applications and flexible in choosing microfluidic designs given the much expanded surface area.

It is very important to mention this chip-in-carrier approach is not only limited to lab-on-CMOS applications but also can be used in any integration situations where extended surface of the chip is needed to interface with other device components. The chip-in-carrier packaging scheme provides a universal platform for foreseeable highly integrated multi-component, multi-functionality smart microsystems that possess the CMOS IC as the core electronic brain.

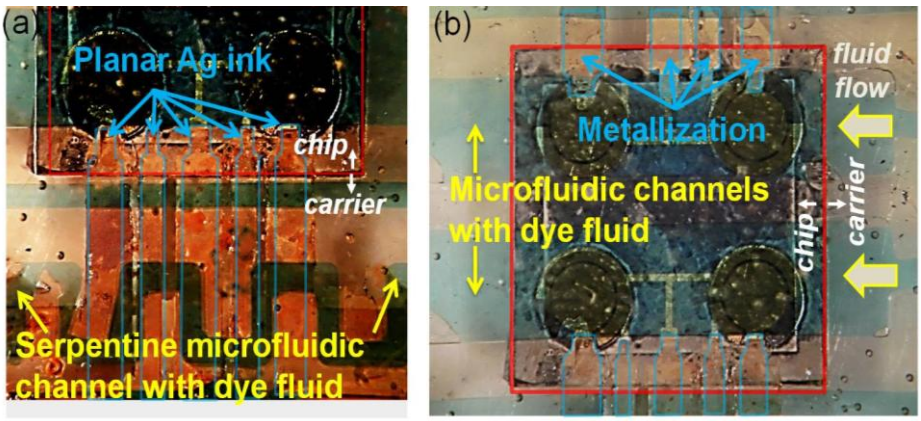


Figure 4.17. No-leakage test: After the integration with PDMS microchannel, the system was tested with dyed DI water driven by syringe pump. (a) The fluid passes over multiple planar metallization traces; (b) the fluid flows across the chip-carrier boundary and over Au electrodes on the silicon chip.

4.4 Discussions

The continuity of the surface transition between chip and the carrier was found to be very critical in order to make film metal interconnects. The scale is usually only a few nanometers in thickness. In the meantime, the push-out effect of the bonding materials was discovered to cause valleys between the carrier and the chip. Surface planarization across carrier and chip boundary

was achieved using thin Parylene film deposited in vapor. On the other hand, liquid-based polyimide and SU8 were used for planarization as an alternative approach with less fabrication steps. Two methods have been developedwere presented to fabricate electrical interconnects for the chip. Thin film copper was deposited using the conventional PVD process and patterned to make the interconnects. The limitation of deposition thickness of PVD process set higher requirement for the step height and surface profile variation for the prior planarization process. Subsequently, a screen printing process of a conductive silver ink was developed to have thicker interconnects which ease the requirements and complexity of the planarization layer.

All of the developments and results in this chapter were achieved using a passive silicon die rather than an active CMOS instrumentation chip. The CMOS IC chip contains active semiconductor components and much larger number of contact pads, leading to higher requirement of fabrication process yield. In Chapter 5, an electrochemical CMOS IC chip will be used to make the integrated CMOS electrochemical biosensor array microsystem and new challenges and solutions related uniquely to CMOS IC chip will be discussed.

5 Lab-on-CMOS Electrochemical Microsystem Using an Epoxy Chip-in-Carrier and Polymer Silver Interconnects

In Chapter 4, an epoxy chip-in-carrier integration process was presented with a passive silicon die. The ultimate goal of this thesis work is to implement the epoxy chip-in-carrier integration process with an active CMOS IC chip in order to realize a lab-on-CMOS electrochemical microsystem that can perform microfluidic operation and electrochemical measurement directly on the surface of a CMOS chip. In contrast to the passive silicon die, an active CMOS IC chip contains functional circuits and a much larger number of contact pads, leading to a requirement for higher yield from the chip-in-carrier integration process. Furthermore, the chip-in-carrier integration process must be tailored to unique physical and electrical characteristics of an active CMOS IC.

Building on the epoxy chip-in-carrier approach in Chapter 4, this chapter presents a lab-on-CMOS integrated microsystem with epoxy chip-in-carrier and polymer silver interconnects. The building blocks of the lab-on-CMOS microsystem, including the CMOS electrochemical IC chip, on-CMOS electrode array, and chip-in-carrier package, will be described first. Then, polymer silver interconnects will be presented followed by microfluidic integration to demonstrate functionality and CMOS compatibility of the lab-on-CMOS integrated microsystem.

5.1 Microsystem Overview

In general, the lab-on-CMOS concept refers to an integrated microsystem which can perform typical biological lab experiments on top of a CMOS instrumentation chip. In practice, the lab-on-CMOS microsystems that have been developed focus on realizing microfluidic operation directly on CMOS IC chips, often accompanied by sensing activity using the CMOS

IC chip. Utilizing the epoxy chip-in-carrier integration process developed in prior chapters, the next goal is to design a lab-on-CMOS microsystem that integrates microfluidics, on-CMOS electrode sensor array and a CMOS electrochemical instrumentation IC chip. Functionally, the target lab-on-CMOS microsystem is expected to perform direct on-CMOS electrochemical sensing using the CMOS electrochemical instrumentation IC chip, within the integrated microfluidics.

To build this lab-on-CMOS microsystem, we will start with a CMOS amperometric instrumentation chip developed in our lab, and then we will apply our post-CMOS process to fabricate an on-CMOS microelectrode array and our epoxy chip-in-carrier integration process (Ch. 3) to package the CMOS chip. The next step in integration is formation of metal interconnects for the lab-on-CMOS assembly, which requires development of a new polymer silver screen printing method that will be presented in Section 5.3. Finally, a microfluidic layer must be integrated with the CMOS array assembly to complete the lab-on-CMOS microsystem, as presented in Section 5.4.

5.2 CMOS amperometric instrumentation chip, on-CMOS microelectrode array and epoxy chip-in-carrier

5.2.1 CMOS amperometric instrumentation chip

A CMOS amperometric instrumentation circuit consisting of potentiostat and amperometric readout circuit was developed by our group for sensing applications [89]. As shown in Figure 5.1, a typical potentiostat topology was adopted with only one operational amplifier to reduce power consumption. Input V_{ref1} was applied to the positive end of the opamp and the feedback network can hold the V_{RE} to be equal to V_{ref1}. The power supply was set to 5V, and the RE and CE can be

driven in the range of 0.1V to 4.9V with a rail-to-rail opamp (r2rop) design [90]. A low-noise amperometric readout circuit topology was adopted from our previous work [91]. An integrator was used to convert the current to voltage, since capacitive feedback readout achieves lower noise compared to resistive feedback and current conveyor [92]. The output voltage of the integrator was connected to a programmable gain amplifier (PGA) with a gain of C_{C1}/C_{C2}. A sample and hold (S/H) circuit was used to output a stable voltage. The non-overlapping clock signals were generated by an on-chip clock generator block. The output of amperometric readout is given by

$$V_o = \frac{I_{WE}}{f_s \cdot C_{int}} \cdot \frac{C_{C1}}{C_{C2}}$$

where I_{WE} is the current collected at WE, f_s is the frequency of the switch clocks, C_{int} is the capacitor value of the integrator, C_{C1} and C_{C2} are the capacitors in PGA circuit.

The chip had four individual readout channels that can support four sets of three-electrode electrochemical sensors as shown in Figure 5.1. The chip was 2.2mm×2.2mm in size and had surface contact openings to make electrical connections for working electrode (WE), reference electrode (RE) and counter electrode (CE). The power supply was set to 5V, and the RE and CE can be driven in the range of 0.1V to 4.9V. The current readout range was tested within 100pA-10μA. The performance of the CMOS circuit is summarized in Table 5.1.

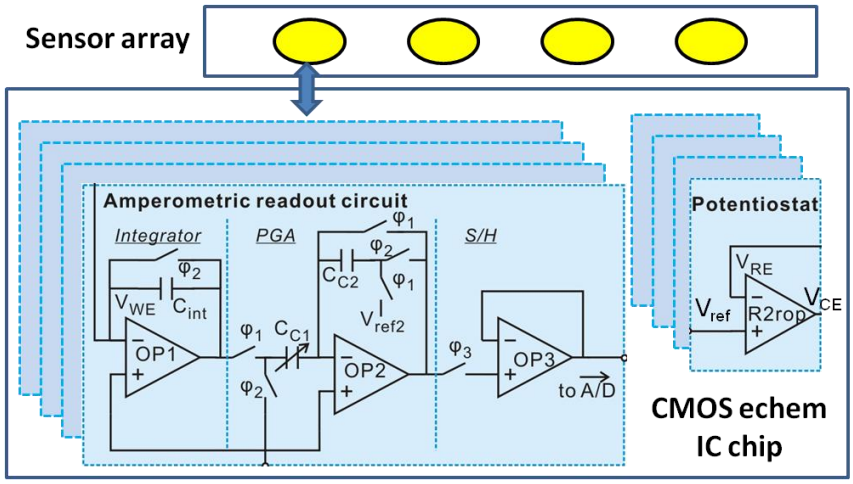


Figure 5.1. Schematic of the microsystem, consisting of the amperometric instrumentation circuit and the electrochemical sensor.

Table 5.1.

Performance summary of the CMOS amperometric instrumentation circuit

Power supply	5V
Chip size	2.2mm×2.2mm
Input/output range of potentiostat	0.03-4.90V
Current readout range	100pA-10μA
Number of pads	40
Gap between adjacent pads	20μm

5.2.2 Microelectrode array on CMOS

To make electrochemical measurements on CMOS chip, microelectrodes need to be fabricated on CMOS. 2×2 microelectrode array can be implemented to utilize the four individual readout channels in CMOS chip. To enable electrical connection between CMOS electronics and electrodes fabricated on the surface of the CMOS chip, open contacts in overglass are designed

in layout. Also, to allow better reliability of electrode pattern and surface routing, top metal layer is avoided in circuit routing to have a smooth chip surface.

The CMOS chip is manufactured in ON 0.5µm CMOS process and the die are received as 2.2mm × 2.2mm in size. 2×2 gold microelectrode array is fabricated on chip using the process developed in our group [93]. The CMOS chip was handled by bonding it to a wafer to allow standard PVD and photolithography process with improved minimum feature resolution. The microelectrode array consists of WE, CE, and RE and each of them is routed to the respective

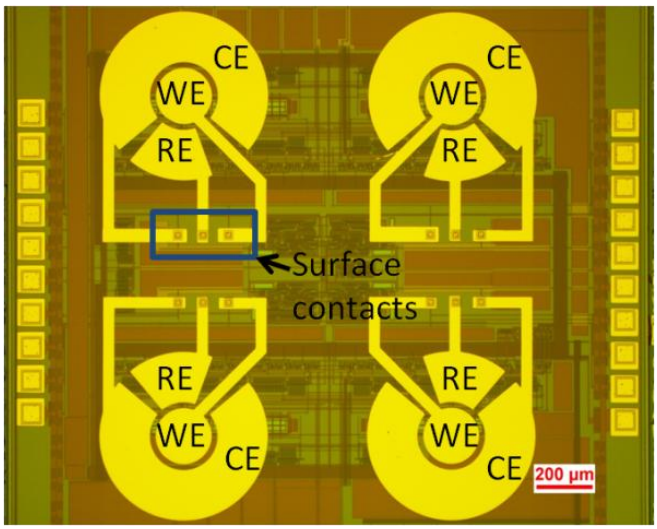


Figure 5.2. 2×2 electrochemical microelectrodes fabricated on the CMOS amperometric instrumentation chip. Each electrode is routed to its respective surface contact.

contact opening on chip surface as shown in Figure 5.2. The CMOS chip with electrodes is then ready for epoxy chip-in-carrier integration.

5.2.3 Epoxy chip-in-carrier

The chip-in-carrier integration process developed in our group was used to package the

CMOS chip. Waferbond, a commercial temporary bonding material, was spin-coated on a 1”×3” glass slide at 3000rpm, followed by contact baking at 120℃ and 180℃, each for 2min. The CMOS chip is then bonded on the glass slide with CMOS top surface facing down. A second glass slide was then placed on top of the CMOS chip and a biocompatible epoxy EPO-TEK 302-3M (Epoxy Technology, Inc.) was infused between the two glass slides. The meniscus of the epoxy travelled from one side all the way through the other side. The epoxy was then cured at room temperature for 24 hours. Waferbond was then dissolved in Waferbond remover bath at 110℃ for 1-4 hours and the chip-in-carrier structure was released. The fabricated chip-in-carrier device of CMOS chip with on chip electrode array is as shown in Figure 5.3.

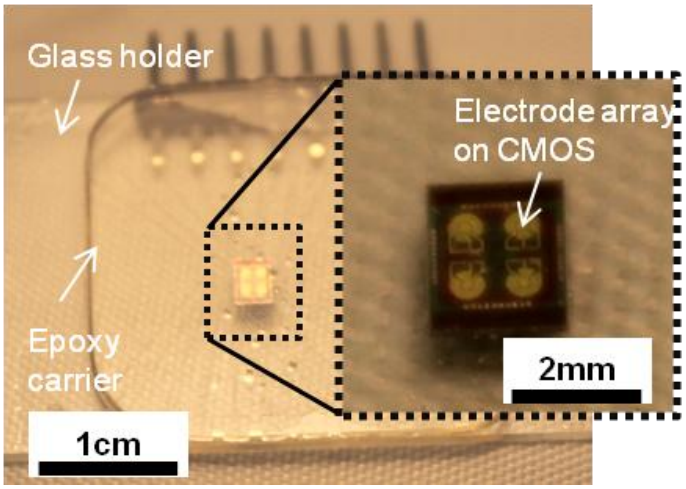


Figure 5.3. Fabricated chip-in-carrier device of CMOS chip with on chip electrode array.

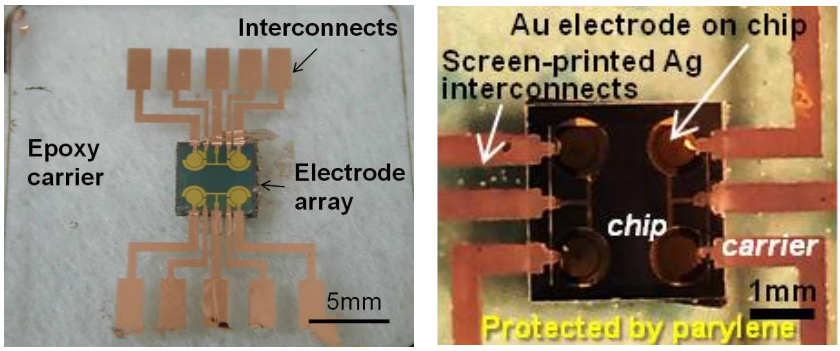
5.3 Polymer silver interconnects

5.3.1 Analysis of challenges

After the epoxy chip-in-carrier integration was finished as described above, the next step in

our lab-on-CMOS process is the fabrication of electrical interconnects routing CMOS signals to the chip-carrier edge. In prior designs (Chapter 4), the interconnects were realized by thin film metal and polymer silver ink, as shown in Figure 5.4(a) and (b). In design in Figure 5.4(a), thin film Ti/Cu was deposited and patterned [94]. A weakness of this approach is that the thin film metal needs PVD equipment to deposit and the thickness of the metal is not recommended to exceed 1µm due to cost and equipment limitation, which limited the yield of device fabrication. In the design in Figure 5.4(b), the polymer silver paste was screen printed over a photoresist "screen" mask. The polymer silver paste could print thick metal interconnects with simple fabrication tools. However, after the removal of photoresist screen, the screen printed interconnects where observed to have expanded up to 20µm from the designed width. This is assumed to be due to the thickness (~10µm) of the photoresist screen. Also, removal of the photoresist screen by acetone and water was found to etch the polymer silver interconnects, which could potentially dissolve smaller line width interconnects and cause open circuits. For the CMOS IC chip used in this work, 40 I/O pad contacts were located around the chip, and the spacing between contacts and size of the contacts were only 20µm and 100µm, respectively. Overall, achieving functional metal interconnects with small spacing and contact size was found to be challenging with the polymer silver paste screen printing method.

To enhance the yield of high density interconnects at the CMOS I/O pad contacts, a new method is needed to fabricate the lab-on-CMOS planar interconnects. Photolithography has to be utilized to achieve precise interconnect patterns. Polymer silver paste can make thick interconnects and improve the yield. Thus, photolithography and polymer silver paste still have advantages that we would like to retain while eliminating the disadvantages associated with removing the photoresist screen.



(a) (b)

Figure 5.4. Chip-in-carrier with thin film metal interconnects (a) and screen printed silver interconnects (b).

Because the removal of the photoresist screen was found to cause most of the problems with forming interconnects, a modified approach wherein the screen layer was left on the device surface was explored. The key element in this modification is to replace the soluble photoresist screen with a structural material that does not need to be removed from the interconnect layer.

5.3.2 Process development

To replace soluble photoresist screen with structural material in screen printing method, SU8, a negative photosensitive polymer, was selected. SU8 is a material used to build high aspect ratio microstructures. A conceptual illustration of the chip-in-carrier with SU8 being part of the device is shown in Figure 5.5. The polymer silver interconnects are embedded in the fabricated SU8 microchannels, creating electrical connections from the CMOS I/O pads. The SU8 microchannels have to be directly patterned on the CMOS chip-in-carrier. Some challenges were identified after preliminary experiments of SU8.

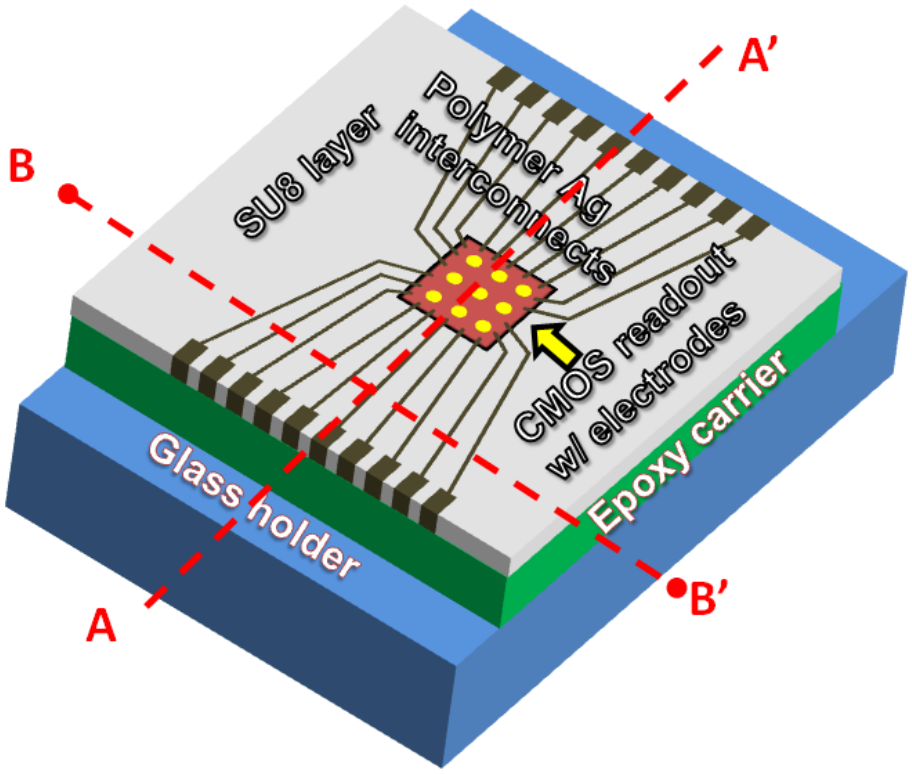


Figure 5.5. Illustration of CMOS chip-in-carrier with polymer silver interconnects embedded in SU8 layer. The cross sectional view of AA' will be shown in Figure 5.7 and the screen printing process of the polymer silver paste using squeegee shown along the BB' line in Figure 5.8.

First, in the metallization process, the SU8 layers are on top of two layers of glass and epoxy which are at least 2mm. SU8 is commonly coated on a thin single substrate of silicon or glass, and coating on a thick substrate is not covered in manuals or the literature. During soft bake, the underlying thick layers reduce the effective heating of SU8, and the SU8 layer could not be baked thoroughly with the standard baking hotplate temperature and time. The incomplete baking could lead to failure of SU8 patterning. To fully bake the SU8, the temperature was set at 105℃, higher than 95℃ recommended in the manual.

Second, the minimum feature size of interconnects needs to be carefully designed. One

challenge is that the non-flat profile near the border between chip and carrier hinders tight contact between the substrate and the photomask. The loose contact could lead to UV light diffraction during UV exposure and cause errors in patterns. This error may enlarge or reduce the pattern depending on the polarity of the photoresist. For negative photoresist SU8, this error means that the remaining SU8 structure after development is wider than expected dimension.

Third, the exposure background of SU8 is transparent in the carrier region and opaque or reflective in the chip region. The overglass of the CMOS IC chip is clear and reveals all of the semiconductor and metal layers inside the CMOS IC chip, which have various reflection properties for UV light. Thus, the ideal UV exposure dose for SU8 varies at different points of the device.

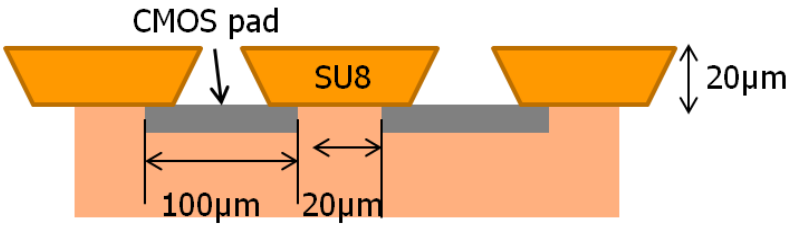


Figure 5.6. Cross sectional view of SU8 microchannel on CMOS chip across CMOS I/O pads.

All three of these design issues are amplified and become more significant as the minimum feature size becomes comparable with the thickness of SU8. Considering these factors the interconnect line width in the photomask design was carefully designed. As shown in Figure 5.6, the thickness and the width of the SU8 structure are comparable. If the interconnect line width is too wide, the width of SU8 walls between interconnects are reduced and prone to detachment by over development. On the other hand, if the interconnect line width is too narrow, the SU8

cannot be completely developed through the SU8 thickness. Similarly for UV exposure dose for SU8 is critical. Overexposure could lead to closure of microchannel and loss of feature. Underexposure could undercut the SU8 wall structure and cause peeling of SU8. Also, unlike common photoresists, SU8 is difficult to remove and reapply, and thus all of the effort to construct the chip-in-carrier structure is lost if the SU8 patterning fails.

5.3.3 Final process

The detailed process steps and parameters were identified after several rounds of experimental effort. SU8-3025 was spin coated at 3000rpm to make a 20µm layer, thick enough to overcome step differences between carrier and chip as shown in Figure 5.7(II). Following the product manual, SU8-3025 was soft baked, exposed, hard baked and developed in sequence. This first $SU8_1$ layer was the planarization layer and also protected CMOS chip side walls from electrically shorting with interconnects. The $SU8_1$ was treated with oxygen plasma at 60W for 60 seconds. This helped the second SU8-3025 layer coat uniformly. Then, a second $SU8_2$ was also spin-coated and patterned to create microchannels for interconnects as shown in Figure 5.7(III). A polymer silver conductor ESL 1901-S (ESL ElectroScience) was then filled into the microchannel using a rubber squeegee as shown in Figure 5.7(IV) and Figure 5.8. ESL 1901-S is a silver-filled, flexible resin material designed for use as a conductor on low temperature substrates. ESL 1901-S was then cured at 50℃ for 30mins. The viscosity of ESL 1901-S could be adjusted by adding thinner. More viscous silver paste makes it harder to fill the narrow SU8 microchannel. A 5µm conformal coating of Parylene was deposited and patterned using oxygen plasma (Nordson March RIE-1701) to insulate the interconnects with the electrodes exposed.

5.4 Microfluidics integration

To demonstrate high throughput microfluidic capability, a multichannel microfluidic structure was designed and bonded to the chip-in-carrier assembly. SU8 microfluidics could have

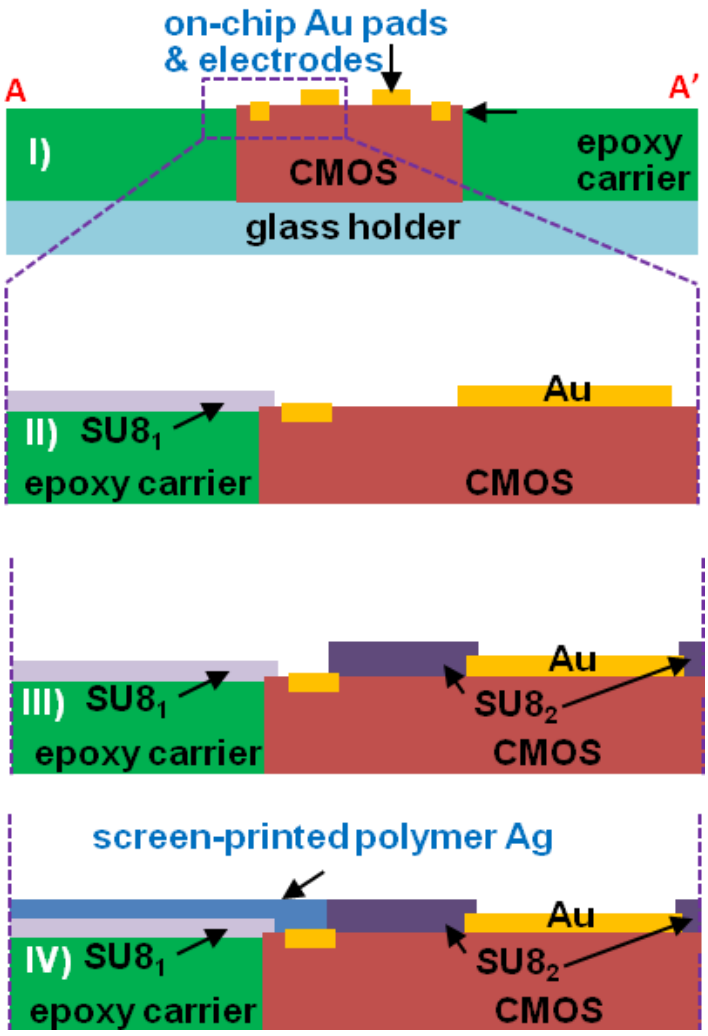


Figure 5.7. Fabrication steps of the chip-in-carrier with screen-printed Ag interconnects and detailed view of the border area between carrier and the CMOS chip. $SU8_1$ is spin coated as planarization layer (II) and $SU8_2$ is spin coated as screen layer for screen-printing process (III). Polymer silver is then deposited using squeegee as illustrated in Figure 5.8.

been constructed directly on top of the chip-in-carrier. However, the processing parameters for SU8 are difficult to characterize because of the unique structure of the chip-in-carrier as a substrate. Alternatively, PDMS microfluidics uses flexible material that could overcome rough surface profile and can be fabricated separately from the chip-in-carrier assembly. In our work, PDMS was selected to implement the microfluidics because of the existing PDMS fabrication parameters and the functionally sufficient capability of PDMS microfluidics in the validation

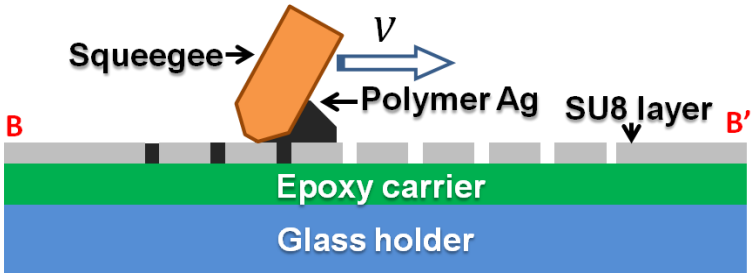


Figure 5.8. Illustration of screen printing process of Polymer silver. The squeegee was used to spread the polymer silver through the channels defined by the SU8 layer.

of lab-on-CMOS microsystem.

The PDMS mold was fabricated using SU8 on a section of oxidized silicon wafer using photolithography with the mask shown in Figure 5.9. Two serpentine microfluidic mixing networks were included with 6 microchannels passing across the CMOS chip surface in parallel. The width of the microchannels was uniformly set at 175µm.

Once the SU8 mold was formed, PDMS (10:1 ratio of precursor to curing agent) was poured over SU8 mold and bubbles in the PDMS were removed in a vacuum chamber before quickly curing at an elevated temperature. Once cured, the microfluidic structure was peeled from the SU8 mold and bonded to the top Parylene layer on the chip-in-carrier assembly. The

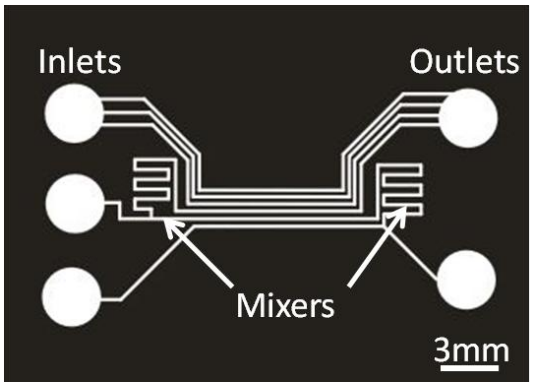


Figure 5.9. The design of microfluidics. 3mm inlets and outlets are placed on each side of the microfluidics and mixers were located before and after the main channels.

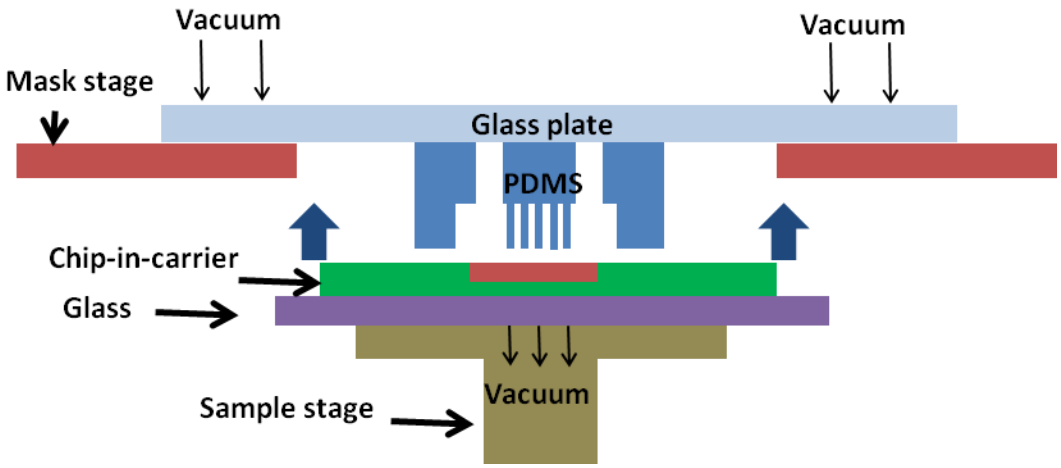


Figure 5.10. Schematic of the alignment method to bond PDMS microfluidics on chip-in-carrier.

bonding between PDMS and Parylene was achieved by applying thin layer of uncured PDMS polymer as adhesion agent to the bottom of microfluidic structure. The alignment and bonding was realized with the assistance of the aligner as shown in Figure 5.10. The aligner has microscrew that can achieve fine alignment in x, y and theta axis. The top side of the PDMS block was weakly attached to a big glass plate which is held on the mask stage, while the electrode glass

slide was fixed on the sample stage. After precise alignment using the microscope, the sample stage was raised up to bond the PDMS block and the chip-in-carrier. The assembly was then cured at 100℃ for 15 min. This PDMS-Parylene bonding was found to be strong enough to allow low pressure microfluidic operation.

5.5 Results

The CMOS amperometric instrumentation chip with microelectrode array described in section 3.2 was used for the chip-in-carrier integration, and polymer silver interconnects were screen printed on the device as shown in Figure 5.11. Pads were selectively connected for a

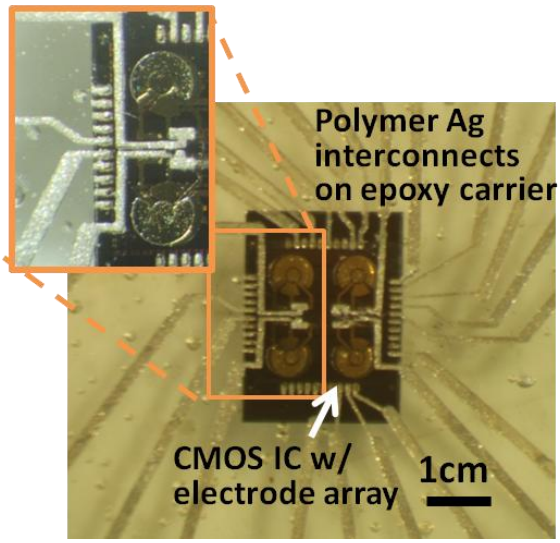


Figure 5.11. CMOS chip-in-carrier with polymer Ag interconnects embedded in SU8 microchannels.

single CMOS readout channel to validate the interconnect process. Resistance of the interconnects was measured and the values were all less than 10Ω from carrier edge to the pad on CMOS chip. The low resistance is expected from the low sheet resistance of the polymer ink (20mΩ/sq) and the wide cross sectional area of the interconnects (50µm width×20µm height).

The highly conductive interconnects should guarantee operation of the CMOS chip, which was further verified by making electrochemical measurement using the CMOS chip as discussed below.

5.5.1 CMOS chip-in-carrier testing

To evaluate the performance of the CMOS chip and the chip-in-carrier packaging, a custom evaluation board was designed to interface the chip with a data acquisition (DAQ) card (National Instruments, DAQ USB-6259). The DAQ generates digital signals to configure and control the

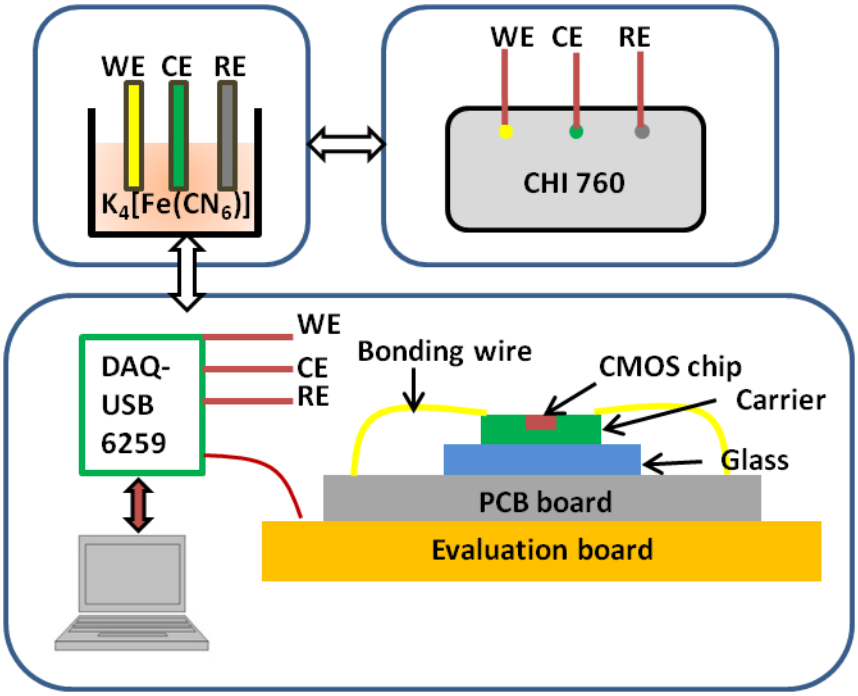


Figure 5.12. Testing setup for electrochemical measurements using chip-in-carrier and commercial CHI760 instrument.

chip, provides input voltage, acquires and digitizes analog outputs from the chip, and displays and stores data on a PC running LabVIEW. The polymer silver interconnects on the chip-in-carrier assembly were first wire bonded to a custom designed PCB board which was then

connected to the custom evaluation board as shown in Figure 5.12.

To verify the functionality of the CMOS chip and the quality of the polymer silver interconnects, cyclic voltammetry measurements were performed for redox recycling electrolyte, potassium ferrocyanide. The redox reaction was described in Section 2.2.2. The measurements have been widely used as a pretest for many redox enzymatic biosensors to evaluate the functionality and quality of the electrodes and the instrumentation system. Solutions of

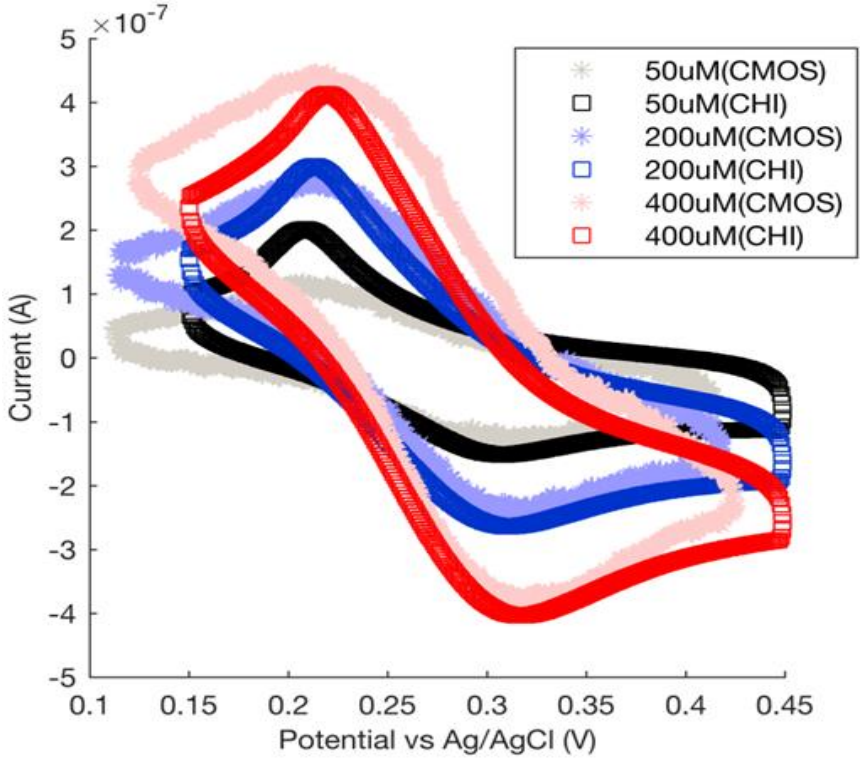


Figure 5.13. Cyclic voltammetry of three concentrations of potassium ferrocyanide ($K_4[Fe(CN_6)]$) by CHI760 commercial instrument and CMOS chip. CMOS measurement data were processed to align with CHI measurement data.

potassium ferrocyanide ($K_4[Fe(CN_6)]$) with three different concentrations (50µM, 200µM, 400µM) were prepared, having 100mM potassium chloride (KCl) as buffer electrolyte. Three

off-chip standard commercial electrodes of 1mm diameter working electrode (gold), counter electrode (platinum wire) and reference electrode (silver/silver chloride) were put in the solutions

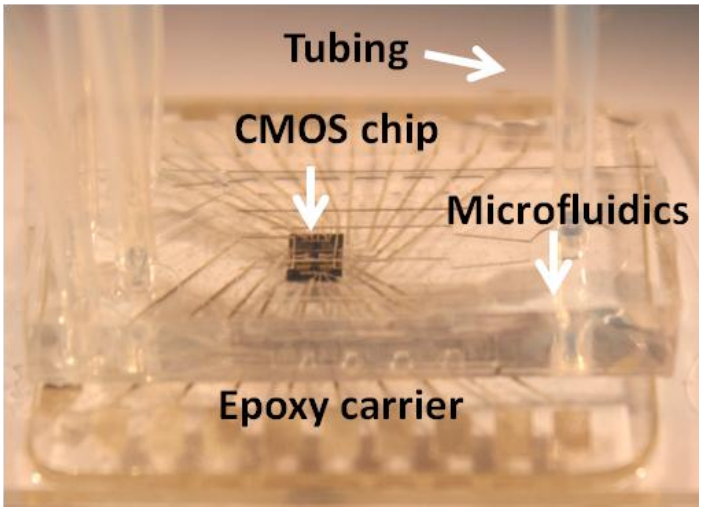


Figure 5.14. Integrated lab-on-CMOS microsystem with microfluidics bonded on chip-in-carrier assembly.

and kept in fixed positions with respect to each other to minimize errors originated from spatial displacement. To benchmark performance of the experimental assembly against commercial equipment, the electrodes were connected, in turn, to a commercial electrochemical instrument (CHI760, CH instruments) and then to the CMOS chip. To perform cyclic voltammetry (CV) experiments, a triangle wave input was applied to sweep V_{WEvsRE} from 0.15V to 0.45V at scan rate of 0.03V/s. The CHI760 instrument generates the input signal internally, but for the CMOS chip the input signal was generated by the DAQ card. Before data was recorded, 5 CV cycles were executed to stabilize current readings.

The same measurements with the same potential range and scan rate were taken by both CMOS chip and CHI760, and the results were as shown in Figure 5.13 at three $K_4[Fe(CN_6)]$ concentrations. The CMOS measurement data were processed to align redox peak potentials with

CHI760 measurement data. Qualitatively, the response current was observed to be responsive to both potential and concentration variations. A key parameter in CV measurements is the redox

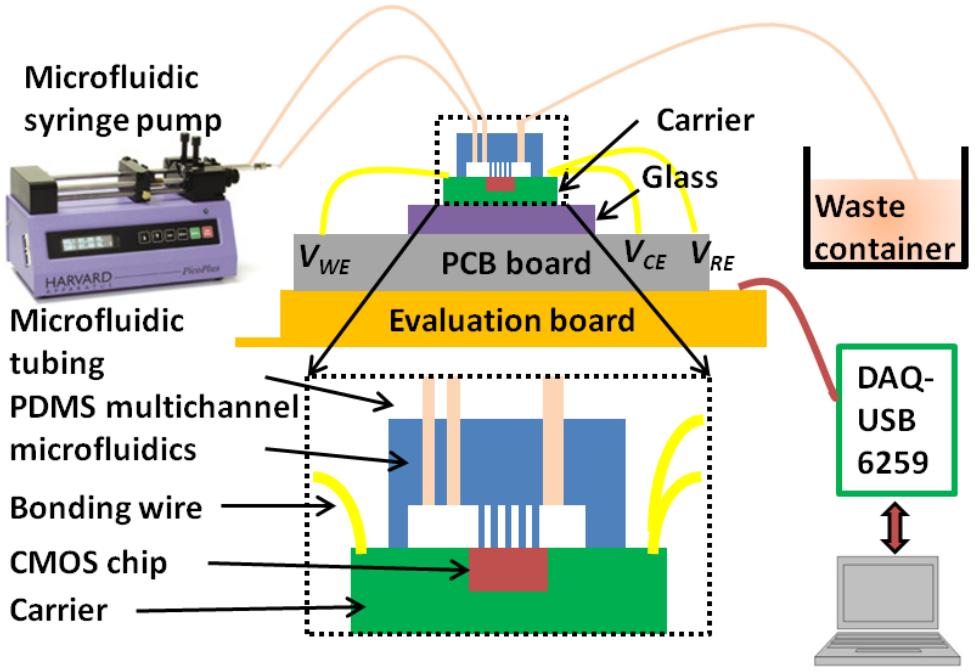


Figure 5.15. Testing setup for CMOS chip-in-carrier with integrated microfluidic channels.

current peak potential. Figure 5.13 shows that the CMOS chip responds to concentration changes very similarly to the commercial CHI760 instrument, maintaining a constant redox peak separation across measurements. The test proved that the CMOS chip was fully functional in the chip-in-carrier packaging and all the I/O pads were electrically connected by polymer silver interconnects in SU8 microchannel.

5.5.2 Lab-on-CMOS testing

Following verification of CMOS chip performance, the final goal is to demonstrate multichannel microfluidic operation using the chip-in-carrier integration process. Using the process described in section 5.6, a multichannel microfluidic device was attached to the top of

the CMOS chip-in-carrier assembly. The final integrated lab-on-CMOS microsystem shown in Figure 5.14 contains an on-CMOS electrochemical sensor array with six on-CMOS

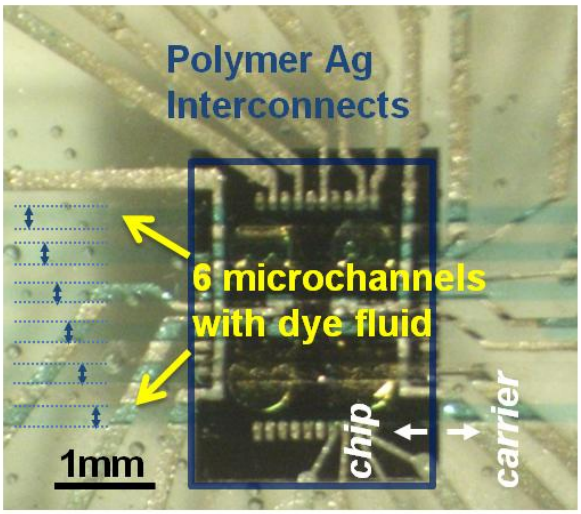


Figure 5.16. Microfluidic channels on CMOS chip-in-carrier. Blue dye DI water flowed through microchannels across carrier and CMOS chip without leakage.

microfluidics channels enabled by the chip-in-carrier assembly. With the abundant surface area available on the chip-in-carrier, five 3mm inlet/outlet ports were placed along two sides of the microfluidic structure without difficulty.

PTFE tubing was connected to the ports and dyed blue DI water was infused through the microfluidic channels by microfluidic syringe pumps (Harvard Apparatus). The testing setup is described in Figure 5.15. All microchannels were inspected under a microscope and found to be sealed well enough to enable continuous flow without leakage as shown in Figure 5.16. High pressure testing was not carried out because our target applications do not require high pressures.

Following microfluidic integration, an electrochemical measurement was made using on-CMOS electrodes to demonstrate on-chip sensing capability. An electrolyte solution of 400µM

$K_4[Fe(CN_6)]$ and 100mM KCl buffer was pumped through the microchannels to reach the electrode area. Both on-chip gold WE and CE were used for the experiment.

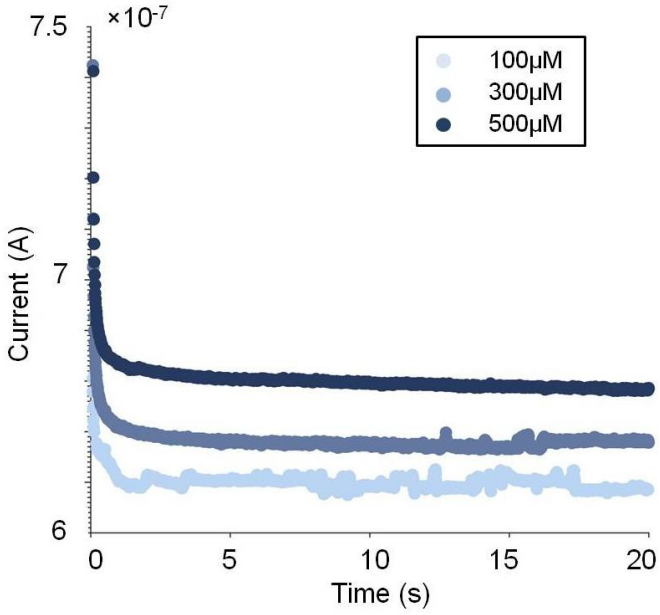


Figure 5.17. On-CMOS chronoamerometry of potassium ferrocyanide ($K_4[Fe(CN_6)]$) with three concentrations of 100µM, 300µM and 500µM.

Chronoamperometry was then performed using the CMOS chip within the lab-on-CMOS device using $K_4[Fe(CN_6)]$ solutions of three different concentrations (100µM, 300µM, 500µM). The solutions were delivered through the integrated microfluidic channels. With CE and RE electrically shorted together, a step potential V_{WEvsCE} was applied for 20s at 0.4V. The result of three measurements is as shown in Figure 5.17. The response values at t=20s were plotted against concentrations to produce the calibration curve showing good linearity with an R^2 fit error of 0.985, which is shown in Figure 5.18. These results demonstrate that the quality of the gold electrodes and performance of the CMOS circuits were not affected by the chip-in-carrier process. They further show that the lab-on-CMOS device was able to deliver test samples to the

electrodes via microfluidics while the interconnects and CMOS chip were well protected from the electrolyte solution by Parylene passivation. Moreover, to the best of our knowledge, these

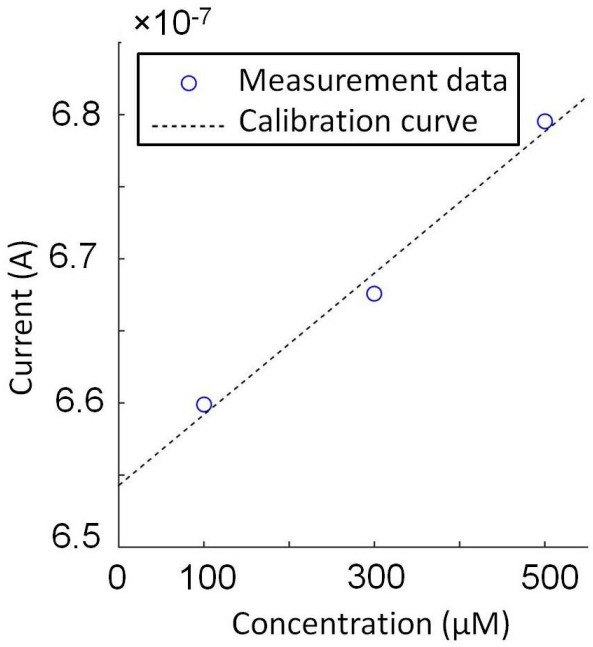


Figure 5.18. Calibration curve of on-CMOS chronoamerometry of potassium ferrocyanide ($K_4[Fe(CN_6)]$) with three concentrations of 100μM, 300μM and 500μM.

results demonstrate the first ever on-CMOS electrochemical sensor measurements using multichannel on-CMOS microfluidics.

Furthermore, a cyclic voltammetry measurement was made with on-CMOS electrode. An electrolyte solution of 400μM $K_4[Fe(CN_6)]$ and 100mM KCl buffer was pumped through the microchannels to reach the electrode area. Both on-chip gold WE and CE were used for the experiment. To eliminate experimental variation, an off-chip Ag/AgCl RE was placed in a waste container at the outlet of the microfluidics and connected through the conductive electrolyte solution. Cyclic voltammetry was then performed using the CMOS chip within the lab-on-CMOS device using $K_4[Fe(CN_6)]$ solution delivered through the integrated microfluidic channels.

The V_{WEvsRE} was scanned between 0.25V and 0.55V with scan rate of 0.03V/s. The results in Figure 5.19 show that the whole CV cycle was successfully measured with clear redox peaks.

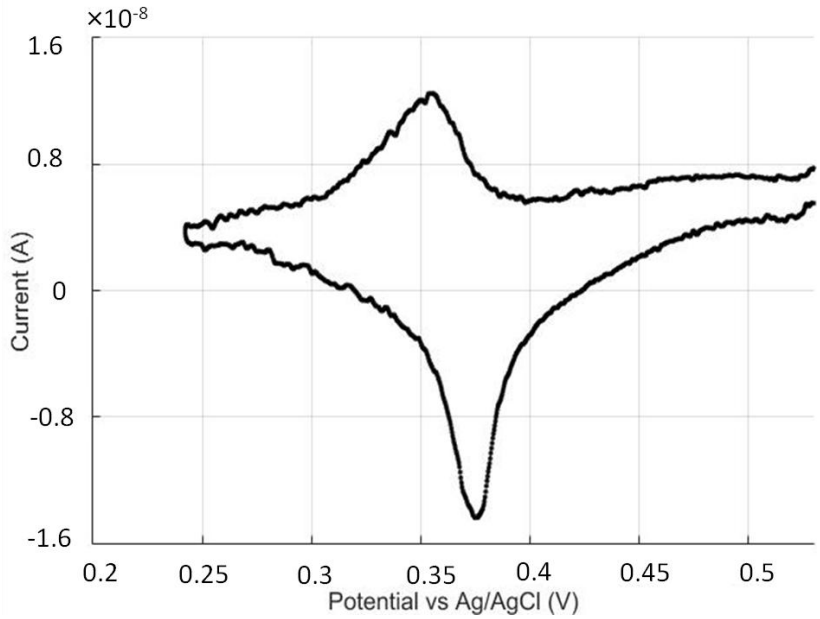


Figure 5.19. On-CMOS CV measurement of 400μM potassium ferrocyanide ($K_4[Fe(CN_6)]$) in microfluidic channels using CMOS chip.

The response current measured from the on-CMOS electrodes was in the nA range, which was in good agreement with measurements made by the commercial CHI760 using the same size off chip working electrode. Compared to the results in Figure 5.13 with on-CMOS instrumentation and off chip electrodes, the lab-on-CMOS results show a much smaller current due to the smaller on-CMOS working electrode, and shifted redox peaks, which is likely due to RE potential drop across the resistive path to the off-chip standard RE. Peak separation was also reduced because of the smaller distance between WE and CE and iR drop.

To select a process for interconnect fabrication, a guideline of thin film metal process and screen printed silver polymer process is summarized in Table 5.2. Thin film metal process is

preferred for smaller feature size with less number of I/Os. Screen printed silver polymer process is preferred for bigger feature size with more number of I/Os because of better yield of the process.

5.6 Conclusion

A new process for implementing a lab-on-CMOS electrochemical microsystem was introduced using polymer silver interconnects and epoxy chip-in-carrier integration. This lab-on-CMOS approach solves the dimensional conflict between CMOS readout circuitry and microfluidics and allows integration of CMOS instrumentation with a variety of microfluidic structures. Successful use of microfluidic structures and on-CMOS electrochemical measurements were demonstrated using the designed lab-on-CMOS device.

The chip-in-carrier packaging scheme with polymer silver interconnects was developed as a solution to lab-on-CMOS electrochemical sensing. However, it is very important to note that this chip-in-carrier approach is not only limited to only lab-on-CMOS applications but can also be

Table 5.2.

Comparison of two interconnects processes

	Thin film metal process	Screen printed silver polymer process
Gap between metal, linewidth	~10µm	>50µm
I/O number for 2.2mm×2.2mm	<20	>20, limited by size of CMOS chip
CMOS contact size	>20µm	>40µm
Tools and materials	PVD, sputtering, element metal (Cu, Al)	Squeegee, polymer silver
Yield	Low	High

used in any integration situations where extended surface of the chip is needed to interface discrete functional components. The chip-in-carrier packaging scheme provides a universal platform for chips, sensors, resistors, capacitors or PCBs to be highly integrated to reduce device form factor. In an era of portable and wearable devices, the chip-in-carrier packaging scheme can be an enabling technique to develop highly integrated smart devices.

6 Summary, Contributions and Future Work

6.1 Summary

This dissertation presents new chip-in-carrier integration and lab-on-CMOS electrochemical microsystem to address the existing challenges of microsystem integration of CMOS instrumentation ICs, biosensors and microfluidics. Fundamentals of protein biosensors, CMOS electrochemical circuits, electrodes, encapsulation methods for on-chip measurements in liquid and microfluidics were introduced. A comprehensive literature study was completed to identify existing challenges in the integration of CMOS microfluidic biosensor microsystems. A unique low-cost epoxy chip-in-carrier integration process was developed to package the CMOS IC chip while enabling microfluidic integration on the CMOS chip. The integration process was divided into three steps of epoxy chip-in-carrier process, planarization and metal interconnects processes. Each step was comprehensively analyzed and experimentally developed with different materials and process designs. The epoxy chip-in-carrier integration greatly expands chip surface area to centimeter scale while electrically connecting the chip using microfabricated surface metal interconnects. For the first time, a lab-on-CMOS electrochemical microsystem with polymer silver interconnects was developed. Electrochemical measurements were successfully made using an on-CMOS microelectrode array within on-CMOS integrated microfluidic channels. This work enables direct on-CMOS electrochemical sensing within a complete microsystem that includes CMOS IC, electrochemical sensor and microfluidics. This work establishes a physical platform for the integration of CMOS ICs and electrochemical sensor arrays. Moreover, this work bridges the gap between CMOS ICs and microfluidics and provides new integration and miniaturization techniques that can be utilized by a wide range of microsystems.

6.2 Contributions

This dissertation addresses multidisciplinary challenges in the integration of microelectronics, microfabrication, electrochemical sensors and packaging technology by inventing new chip-in-carrier integration methods for lab-on-CMOS electrochemical microsystems. These achievements were made by comprehensive knowledge learned from courses, scientific literature and, most importantly, my extensive experience gained from numerous experimental work done in microfabrication facility. The significant contributions of this work include:

- *Designed a new, low-cost, CMOS compatible packaging process to expand the CMOS IC chip surface area for microfluidic sensor integration.*

The epoxy chip-in-carrier integration process was designed using low-cost epoxy material and fabrication processes. Key steps and materials in the epoxy chip-in-carrier process were identified and experimentally developed with different materials and fabrication tools. The materials and processes used are all CMOS compatible and readily available with low cost.

- *Developed a new screen printing process for fabrication of high-yield chip-in-carrier surface interconnects to enable lab-on-CMOS integration.*

The silver ink metal interconnects enable the electrical connections for CMOS ICs with improved yield due to its high thickness. The method is low in cost compared with traditional thin film metal interconnects which require expensive physical vapor deposition tools. A second polymer silver interconnects tailored to high density contacts were also invented by embedding interconnects in SU8 microchannels.

- *Developed a fully integrated lab-on-CMOS electrochemical microsystem that achieved, for the first time, direct electrochemical measurements using a CMOS instrumentation chip, on-CMOS microelectrode arrays, and on-CMOS microfluidic channels.*

Potassium ferrocyanide was electrochemically detected in the lab-on-CMOS electrochemical microsystem using integrated microfluidics, on-CMOS microelectrode and CMOS IC. This work enables the capability of on-CMOS electrochemical sensing in liquid handled by microfluidics.

6.3 Future work

This research establishes a platform for microsystem integration in lab-on-CMOS applications. The following suggestions are made for future work.

- *Implement the epoxy chip-in-carrier integration process at the wafer level*

The epoxy chip-in-carrier process is suitable for wafer level process for mass production. A number of CMOS chips can be embedded in an epoxy wafer and the epoxy wafer can be diced into individual carriers after planarization and metallization. Further study of chemical and physical properties of the epoxy may be required as the wafer size increases.

- *Implement an electrochemical biosensor using the presented lab-on-CMOS microsystem platform*

The presented lab-on-CMOS microsystem platform is very flexible in on-CMOS microelectrode array design and microfluidics design. There are many biosensors that can employ this lab-on-CMOS microsystem to improve the sensitivity and throughputs by designing appropriate CMOS ICs, microelectrode arrays and microfluidics.

- *Integrate multiple CMOS IC chips in a single epoxy carrier to realize multifunctional microsystem*

The cost of designing and manufacturing multi-functional CMOS IC chips is much higher and designing single function CMOS IC chips. It could be very cost effective to integrate several individual CMOS IC chips into one chip-in-carrier platform to realize more complicated function.

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