NUMERICAL ANALYSIS OF MAXIMUM MICROWAVE POWER FROM A TUNNEL-DIODE OSCILLATOR

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CHANDRAKANT BHAILALBHAI PATEL
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This is to certify that the

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NUMERICAL ANALYSIS OF MAXIMUM MICROWAVE POWER FROM A TUNNEL-DIODE OSCILLATOR

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Chandrakant B. Patel

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R. J. Giacoletto
Major professor

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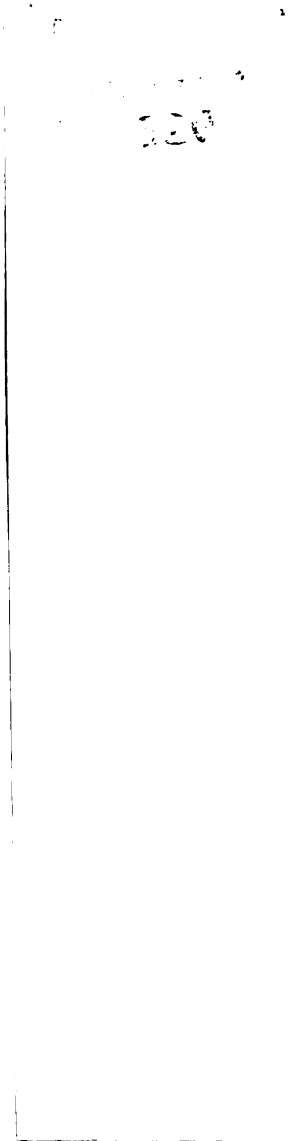

ABSTRACT

NUMERICAL ANALYSIS OF MAXIMUM MICROWAVE POWER FROM A TUNNEL-DIODE OSCILLATOR

By

Chandrakant B. Patel

The available literature on negative-resistance oscillators contains abundant information on small-signal analysis of tunnel-diode oscillators. Little consideration, however, has been given to large-signal analysis. Those analyses which are available are based on

1. low-frequency circuit operation; and
2. assumption of a single-frequency sinusoidal voltage at the tunnel diode terminals.

In this thesis, the large-signal operation of a tunnel-diode oscillator circuit is examined with the object of delivering maximum fundamental power to the load. The exact analysis of the circuit operation results in a highly nonlinear, third-order and second-degree differential equation. The circuit can also be described by means of a set of first-order, nonlinear differential equations--its mathematical model. Using a digital computer, this set of equations is numerically integrated in the time-domain using a fourth-order Runge-Kutta scheme. The

time-domain solution retains all significant harmonics, and frequency-domain analysis can then be used to evaluate the harmonic content. This method of solution can be easily extended to study the effects of voltage-dependent elements such as the tunnel-diode junction capacitance.

The set of equations describing the tunnel-diode oscillator operation, with the circuit designed for the d c operating point in the negative-conductance region, is numerically integrated until the digital computer cyclic solution corresponds to the steady-state operation of the circuit as determined when the harmonic components of two consecutive periods of the diode voltage are identical within specified limits. The fundamental power delivered to the load is next evaluated. This procedure, as outlined, is repeated for a number of different bias values and a number of different load resistances. These results indicate an optimum bias and an optimum load resistance for maximum fundamental power. The optimum bias is closer to the diode valley point than to the peak point; the flatter the diode valley characteristic, the closer will be the optimum bias to the valley point. The ratios, $(V_V - V_{opt})/(V_V - V_P)$, for the two diodes analyzed here are 0.382 and 0.345. The actual fundamental frequency of operation obtained from the time-domain analysis of the circuit is slightly lower than the frequency calculated from small-signal analysis.

Circuit operation corresponding to optimum load resistance cannot be obtained by small-signal build-up from the bias point. Rather, this limit-cycle must be obtained by a large-signal perturbation, as for instance by external triggering. The power delivered to the load is reduced when the operating frequency is increased. Analysis of circuit operation with a voltage-dependent junction capacitance indicates somewhat higher maximum power delivered to the load and slightly lower operating frequency than with the same circuit and a constant junction capacitance.

Two specific configurations of load circuit were used for most of the computer analysis work. Of greater interest would be the synthesis of an optimum circuit configuration for obtaining maximum fundamental power from a specific diode. A few simple computations were made in connection with this synthesis problem. The results of these simple calculations are consistent with the analytic results, but are not of sufficient generality to produce a fully-synthesized circuit.

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Chandrakant Bhailalbhai Patel

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CHAPTER 1

INTRODUCTION

1.1 Background

A negative-resistance device is of considerable interest as a signal-generating device. The tunnel diode, a two-terminal negative-resistance semiconductor device, opened up entirely new fields for circuit and solid-state device engineers. The significant properties of the tunnel diode were first observed by Leo Esaki while experimenting on degenerately doped p-n junction. Esaki's results were first published in an historic paper [1] in early 1958.

The tunnel diode differs in the basic physical mechanism of its operation from the common rectifying diode. Quantum-mechanical tunneling, from which the name "tunnel diode" is derived, is uniquely exploited in this active device to produce a negative resistance when it is properly biased. The immediate applications of the device were seen as amplification and generation of signals, possibly at millimeter-wave frequencies; as detector, mixer, fast computer memory, and logic element. As research continued and related technology advanced, the

device was better understood and now has a fairly well established place in modern semiconductor technology. This device may find even greater usage as an element in integrated electronic circuits.

An important use of the tunnel diode is as a negative-resistance element in an oscillator circuit to generate high-frequency power.

1.2 Survey of the Literature and the Problem Area

The basic problem of this thesis is part of the problem of an exact analysis of a tunnel-diode oscillator circuit. This thesis will concentrate on

1. high-frequency operation,
2. design of a circuit to maximize the fundamental power delivered to the load, and
3. synthesis of a circuit for high-frequency operation.

The highly nonlinear characteristic of the tunnel diode requires extensive use of a digital computer for a detailed analysis of circuit operation.

It is fitting at this stage to review briefly the literature in the area of negative-resistance oscillators. Van der Pol [22,28] first studied the nonlinear theory of electrical oscillations. Subsequently, two-terminal negative-resistance "black boxes" were devised using tetrodes, transistors, diodes and resistors [35,36,37]; various negative-resistance oscillators and amplifiers were designed [29,30,31,32].

The tunnel diode as a two-terminal negative-resistance element was analyzed by Kim and Brandli [4], Chow [5], G. Dermit [20] and others [2,7,14]. Their analysis considered

1. small-signal operation of the device, and
2. a simplified third-degree polynomial approximating the current-voltage (I-V) characteristic for the tunnel diode.

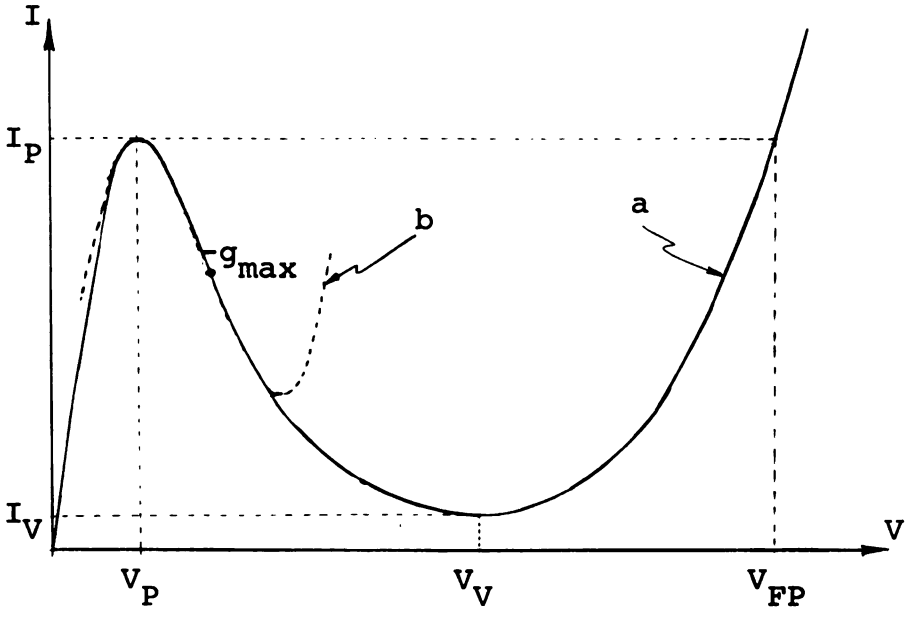


Figure 1.1. Tunnel diode I-V characteristics

(a) Actual
(b) Third-degree polynomial approximation

The circuit operating point was generally chosen as the point of maximum negative-conductance on the curve.

K. Tarnay [6,7] and Coerver [8] considered better approximations (see Section 2.5) to the I-V characteristic.

They analyzed low-frequency operation (below self-resonant frequency, see Chapter 3) by assuming a pure sinusoidal signal. Gartner-Schuller's [17] computer results are likewise for low-frequency operation. Sterzer [9] in his computer calculations used a highly exact approximation for I-V characteristic (tenth-degree polynomial) but he assumed a single-frequency operation. It should be noted that in all these publications the voltage dependency of the junction capacitance is neglected, and the capacitance is assumed to be constant.

The above survey of the literature reveals that large-signal analyses of the tunnel-diode oscillator circuits for high-frequency operation have not been very exact. Better solutions of the problem continue to be of great importance. The improved solutions should consider higher harmonic content of the signals and should include junction capacitance as a voltage-dependent element.

It was through the realization of the overall significance of the problem that the author was motivated to carry out further research in the area of high-frequency power in tunnel-diode oscillators.

1.3 Thesis Summary

The phenomenon of quantum-mechanical tunneling and the qualitative explanation of the tunnel diode action are covered in Chapter 2. There follows a development of

the tunnel-diode equivalent circuit. This equivalent circuit is applicable for analysis from dc through gigahertz frequencies. Also described are the various analytical methods for approximating the I-V characteristic of a tunnel diode.

The small-signal oscillator circuit, its design and its small-signal stability are considered in Chapter 3. Large-signal operation of the tunnel-diode oscillator circuit is analyzed in Chapter 4. Applicable equations are formulated, and their numerical solutions by a digital computer are studied in detail. Examples of maximum power delivered to a useful load are given for two types of tunnel diodes. Effects of voltage dependency of the junction capacitance are examined and illustrated.

A hybrid approach for optimizing the fundamental power generated by the intrinsic tunnel diode is given in Chapter 5. Circuit synthesis is considered to implement the hybrid-approach solutions. A summary of the overall work and conclusions is given in the final Chapter 6.

CHAPTER 2

THE TUNNEL DIODE AND ITS EQUIVALENT CIRCUIT

This chapter first describes the tunneling phenomenon to which the specific property of the device is attributed. Then the equivalent circuit of the device, depending on the tunneling property and other physical characteristics, is developed.

2.1 Tunneling

Classical physics predicts that a particle of total energy, E, cannot penetrate a potential barrier greater than its own energy. The phenomenon known as quantum-mechanical tunneling predicts that a particle of total energy, E, can penetrate the potential barrier of a height greater than E and be found beyond the barrier. The probability of finding the particle on the other side of the barrier decreases with the height and the width of the barrier. These results can be demonstrated by solving Schroedinger's wave equation in a simple, one-dimensional problem.

2.2 Schroedinger's Wave Equation

The time-dependent, one-dimensional Schroedinger wave equation [10] for a particle is

$$-\frac{\hbar^2}{2m}\frac{\partial^2\Psi(x,t)}{\partial x^2} + V(x,t)\Psi(x,t) = j\hbar\frac{\partial\Psi(x,t)}{\partial t} \qquad (2.1)$$

where $\Psi(x,t)$ = wave function defining motion of the particle, $V(x,t)$ = potential energy function, $\hbar = \frac{h}{2\pi}$ where h = Planck's constant = 6.6252×10^{-34} joule-sec., m = mass of the particle, and $j = \sqrt{-1}$.

The time-independent Schroedinger wave equation can be obtained by separating time and position variables as $\Psi(x,t) = \psi(x)\,\phi(t)$ provided $V(x,t) = V(x)$ only.

Substituting these in (2.1) and separating variables we get:

$$\frac{1}{\psi(x)}\left\{-\frac{\hbar^2}{2m}\frac{d^2\psi(x)}{dx^2} + V(x)\psi(x)\right\} = \frac{j\hbar}{\phi(t)}\frac{d\phi(t)}{dt} \; . \qquad (2.2)$$

Since the left-hand side is a function of x only and the right-hand side is a function of t only, and since x and t are independent variables, we must have

$$\frac{1}{\psi(x)}\left\{-\frac{\hbar^2}{2m}\frac{d^2\psi(x)}{dx^2} + V(x)\psi(x)\right\} = C \; , \qquad (2.3)$$

and

$$j\hbar\frac{1}{\phi(t)}\frac{d\phi(t)}{dt} = C \; . \qquad (2.4)$$

Solving (2.4),

$$\phi(t) = e^{-jCt/\hbar} = e^{j\omega t} \qquad (2.5)$$

where ω = angular frequency = $2\pi f = C/\hbar$. Hence, $C = 2\pi f\hbar$ = fh = E, total energy of the particle; hence

$$-\frac{\hbar^2}{2m}\frac{d^2\psi(x)}{dx^2} + [V(x)-E]\psi(x) = 0 \quad . \tag{2.6}$$

This is the time-independent Schroedinger's wave equation.

Figure 2.1 shows the particle with total energy, E, encountering a potential barrier, V, of width d.

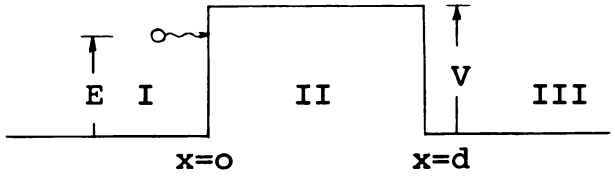


Figure 2.1. Particle of total energy, E, encountering a potential barrier, V, of width, d.

In regions I and III the arbitrary choice is made that $V(x) = 0$, so Schroedinger's wave equation for these regions is

$$\frac{d^2\psi(x)}{d^2x} + \frac{2m}{\hbar^2}E\psi(x) = 0 \quad . \tag{2.7}$$

Let the solution in region I be $\psi_1(x) = A\cos\alpha x + B\sin\alpha x$. Then substituting this, we get

$$(-\alpha^2 + \frac{2m}{\hbar^2}E)(A\cos\alpha x + B\sin\alpha x) = 0 \quad . \tag{2.8}$$

Since $\psi(x) \neq 0$, $\alpha^2 = \frac{2m}{\hbar^2}E$.

Similarly the solution in region III is

$$\psi_3(x) = D\cos\alpha x + F\sin\alpha x \quad .$$

In region II, $V(x) = V$, so the Schroedinger wave equation in region II is

$$\frac{d^2\psi_2(x)}{dx^2} + \frac{2m}{\hbar^2}(E-V)\psi_2(x) = 0 \quad . \tag{2.9}$$

The most general solution of (2.9) is

$$\psi_2(x) = C_1 e^{-\beta x} + C_2 e^{\beta x} \quad . \tag{2.10a}$$

Now $\int_{x_1}^{x_2} \psi(x)\psi^*(x)dx$ is the probability of finding the particle in an interval, $x_2 - x_1$. From the physical consideration $\int_{x_1}^{x_2} \psi(x)\psi^*(x)dx$ is finite. If $C_2 \neq 0$ in (2.10a), $\int_{x_1}^{x_2} \psi(x)\ \psi^*(x)dx \to \infty$ as $d \to \infty$. So $C_2 = 0$. Hence

$$\psi_2(x) = Ce^{-\beta x} \quad . \tag{2.10b}$$

Substituting (2.10b) in (2.9) we get

$$\left\{\beta^2 + \frac{2m}{\hbar^2}(E-V)\right\} Ce^{-\beta x} = 0 \quad .$$

Since $\psi_2(x) \neq 0$,

$$\beta^2 = \frac{2m}{\hbar^2}(V-E) \quad . \tag{2.11}$$

At $x = 0$ and $x = d$, the boundary conditions to be satisfied are:

1. $\psi(x)$ be continuous and finite, and
2. $\frac{d\psi(x)}{dx}$ be continuous and finite.

Matching the boundary conditions:

a) between regions I and II, at $x = 0$,

$$A = C \quad \text{(continuity of } \psi(x)\text{)},$$

$$\alpha\beta = -\beta C \quad \text{(continuity of } \frac{d\psi(x)}{dx}\text{)};$$

b) between regions II and III, at $x = d$,

$$Ce^{-\beta d} = D \cos\alpha d + F \sin\alpha d ,$$

$$-\beta Ce^{-\beta d} = \alpha[-D \sin\alpha d + F \cos\alpha d] .$$

Writing constants A, B, D and F in terms of C the solutions are

for region I $$\psi_1(x) = C[\cos\alpha x - \frac{\beta}{\alpha} \sin\alpha x] , \qquad (2.12a)$$

for region II $$\psi_2(x) = C \exp(-\beta x) , \qquad (2.12b)$$

and for region III
$$\psi_3(x) = Ce^{-\beta d}[(\cos\alpha d + \frac{\beta}{\alpha} \sin\alpha d) \cos\alpha x + (\sin\alpha d - \frac{\beta}{\alpha} \cos\alpha d) \sin\alpha x]$$
$$= Ce^{-\beta d}[\cos\alpha(x-d) - \frac{\beta}{\alpha} \sin\alpha(x-d)] . \qquad (2.12c)$$

For any of the regions $\int_{x_1}^{x_2} \psi(x)\psi^*(x)dx \neq 0$. So the particle can be found in region III beyond the barrier with

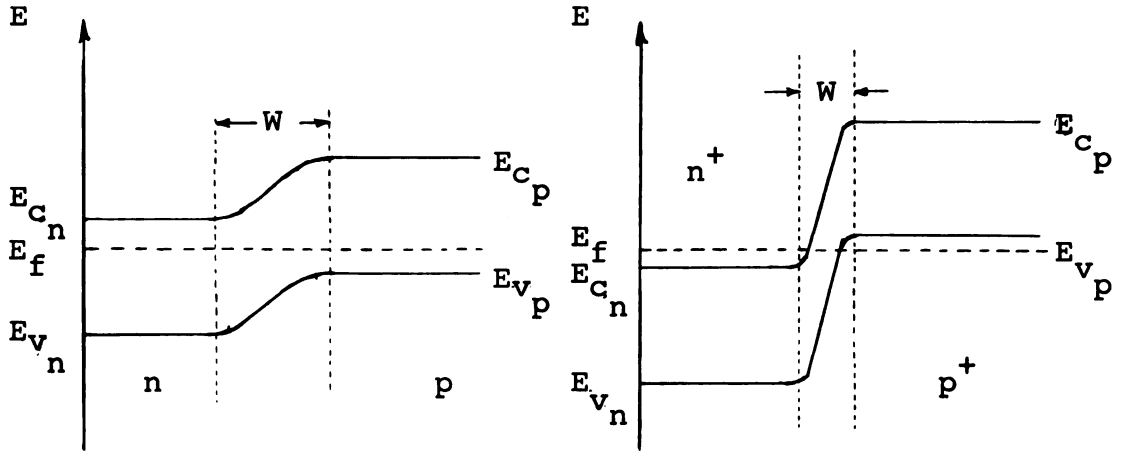
finite probability. It can be seen that $|\psi(x)|$ in region III is reduced by a factor of $e^{-\beta d}$ as compared to $|\psi(x)|$ in region I. This clearly indicates that the thinner the barrier the higher the probability of penetration. Also the smaller the barrier height the higher the probability of penetration.

2.3 Qualitative Explanation of the Tunnel-Diode Action

A tunnel diode is a p-n junction with both p and n semiconductors heavily doped to degeneracy. There are two main effects of heavy doping. Firstly, the depletion layer width, W, is small, that is, it constitutes a thin energy barrier. Secondly, some empty energy states in the valence band of p-type semiconductor and some occupied energy states in the conduction band of the n-type semiconductor are at the same energy and vice versa. This energy-level situation allows tunneling from the occupied states in the conductance band to the empty states in the valence band and vice versa. Because the barrier is thin the probability of tunneling is enhanced. (See Figure 2.2)

With no voltage applied, ($V_B = 0$), the tunnel-diode junction is in equilibrium, and the same number of electrons tunnel each way to yield zero net current.

When a small forward-bias voltage ($V_B > 0$) is applied, more electrons tunnel from the n-side into the empty states in the p-type material than in the reverse direction. This



(a) Lightly doped (b) Heavily doped

Figure 2.2. Band structure of a p-n semiconductor junction
E_c: conduction-band edge energy
E_v: valence-band edge energy
E_f: Fermi energy

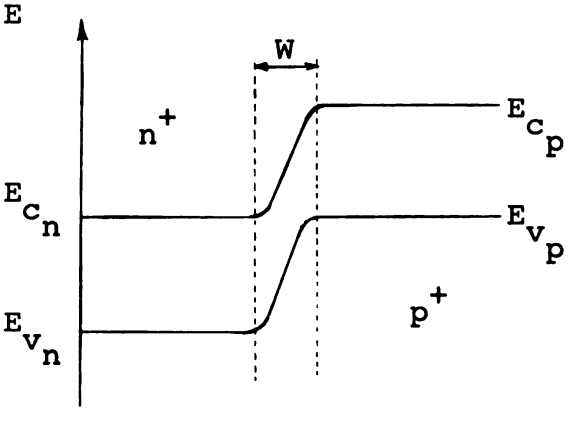


Figure 2.3. Band structure of a p-n junction when tunneling is almost zero.

asymmetry results in a steep rise in the forward current. This rise in forward current with forward bias continues until the empty states in the p-type semiconductor, at the same level as the filled states in the n-type semiconductor, begin to decrease. An increase in forward bias ($V_B > V_P$, see Figure 2.4) at this stage results in a decrease in forward current. This decrease in forward current continues until finally there are no empty states in the p-type material opposite the filled states in the n-type material at the same level. The tunneling current is zero, ($V_B > V_V$). At this point the conduction-band edge is at the same level as the valence-band edge (Figure 2.3). Simultaneously the ordinary p-n junction injection current--mainly diffusion current--is flowing, so the net current does not quite go to zero. The behavior of the tunnel diode for higher forward-bias voltages ($V_B > V_V$) is similar to that of an ordinary p-n junction.

When a small reverse-bias voltage, ($V_B < 0$), is applied, the number of empty states in the n-type semiconductor at the same energy level as the filled states in the p-type semiconductor is greatly increased. Also the reverse bias enhances the electron flow from the p-side to the n-side. As a result, the reverse current increases sharply with reverse bias. As deduced from the above explanation the current-voltage plot of a tunnel diode will be as shown in Figure 2.4.

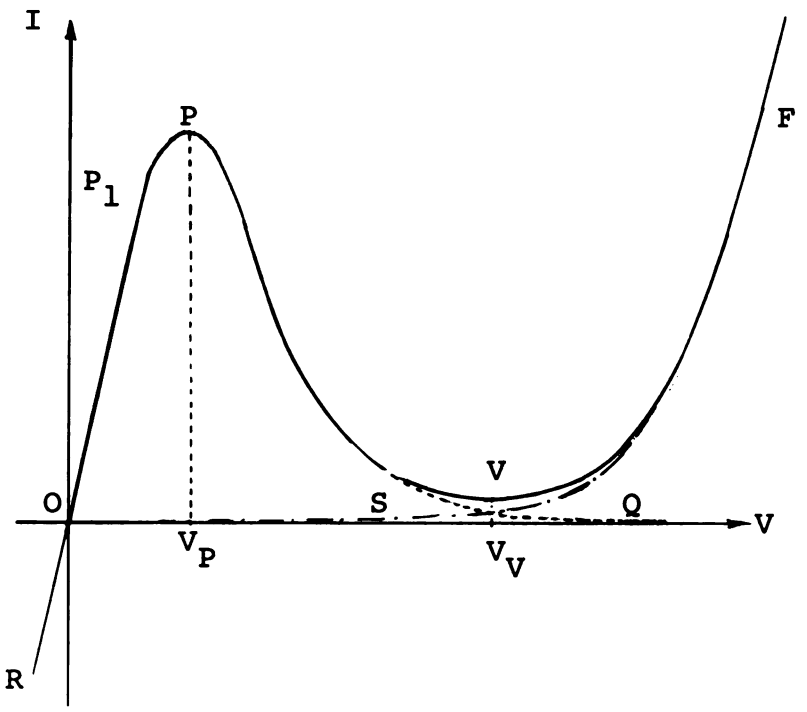


Figure 2.4. I-V plot of a tunnel diode

OP_1: Increasing tunneling current due to small forward bias.

P_1P: Tunneling decreases but resultant tunneling current still increases.

P: Peak point

PQ: Tunneling and tunneling-current component decreases to almost zero.

VF: Total current starts increasing due to ordinary diode injection current, OSF.

OR: Tunneling current due to reverse bias.

2.4 Direct and Indirect Tunneling

The laws of conservation of energy and momentum apply throughout the process of tunneling. The change in momentum before and after tunneling involves some exchange of momentum with the crystal lattice. The case where electron momentum is equal before and after tunneling is called direct tunneling. The processes described in Sections 2.2 and 2.3 are of direct tunneling. If the electron momentum is different before and after tunneling, the process is called indirect tunneling. The probability of indirect tunneling is much lower than that of direct tunneling, owing to the added requirement of the conservation of momentum.

Observing the energy-band-momentum diagram of germanium and silicon (Figure 2.5) we can see that direct tunneling is possible in the case of germanium only. For the silicon junction the peak tunneling current will be very small, since here a momentum of $\hbar k'_c$ in addition to energy is required for tunneling.

Another semiconductor suitable for direct tunneling is gallium arsenide. Therefore most of the tunnel diodes are of germanium or of gallium arsenide.

2.5 Approximating the I-V Characteristic

The static current-voltage characteristic of a tunnel diode was indicated in Sections 2.3 and 2.4 to be as shown in Figure 2.6. An expression approximating

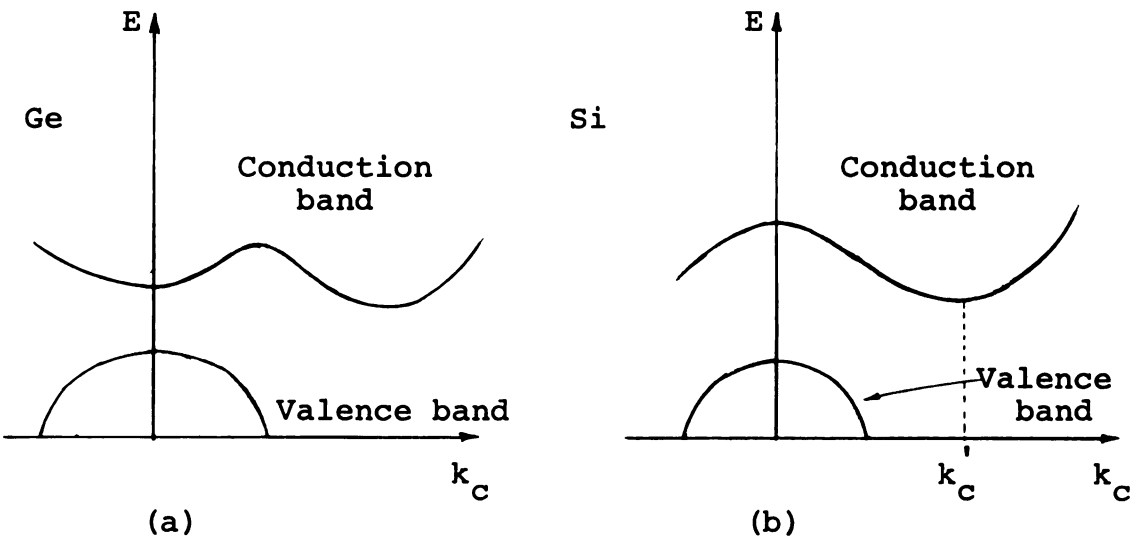


Figure 2.5. Energy band-momentum diagram (a) Germanium, (b) Silicon.

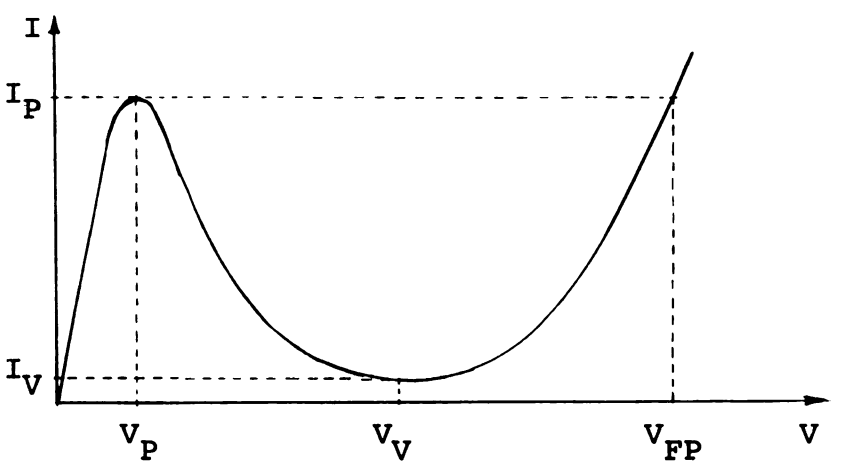


Figure 2.6. Static current-voltage characteristic of a tunnel diode.

I_P: Peak current

I_V: Valley current

V_P: Peak voltage

V_V: Valley voltage

V_{FP}: Forward peak voltage

this current-voltage characteristic is required for any analysis or computing purposes. The I-V characteristic can be approximately through various methods:

(a) Polynomial approximation

$$I(V) = a_0 + a_1 V + a_2 V^2 + \text{---} + a_N V^N = \sum_{j=0}^{N} a_j V^j \quad (2.13)$$

The coefficients a_j, j = 0,1,2,---,N are evaluated in accordance with the desired polynomial fit. The least-square fit is most commonly used. The degree of polynomial, N, depends on the desired accuracy of the fit. For a more accurate fit in a given region the data associated with the region can be given additional weight [38].

(b) Considering $g(V) = dI(V)/dV$, and noticing the flat valley region, Narud and Meyer [13] suggested the following approximation:

$$g(V) = K(V-V_P)(V-V_V)^3 \quad (2.14)$$

Equation (2.15) is obtained by integrating (2.14) by parts and using peak-point and valley-point voltage and current values.

$$I(V) = \int g(V)\,dV$$

$$= \frac{I_V - I_P}{(V_P - V_V)^5} \left[5(V-V_P)(V-V_V)^4 - (V-V_V)^5\right] + C \quad (2.15)$$

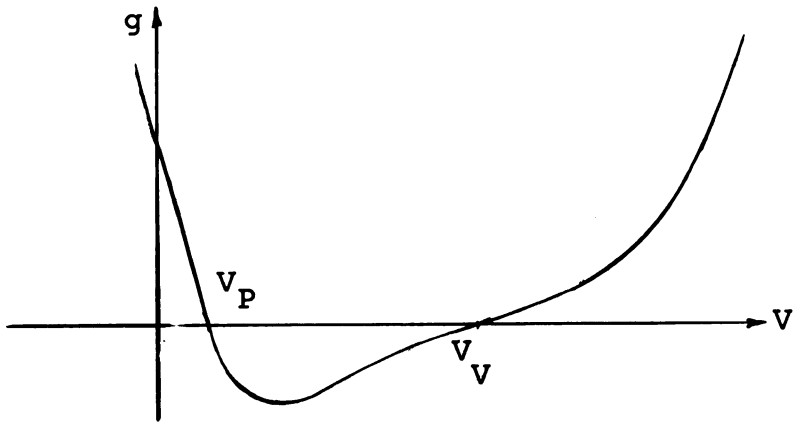


Figure 2.7. Tunnel-diode conductance vs. voltage

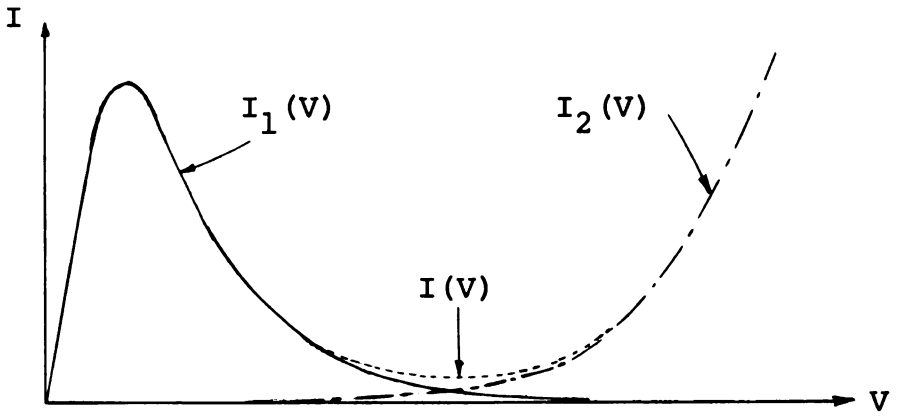


Figure 2.8. Tunnel-diode static characteristic: Ferendici and Ko's approximation.

From valley point (I_V, V_V), the constant of integration, $C = I_V$, is obtained. $I(V) = 0$ for $V = 0$ is obtained only for certain ratios of I_P/I_V and V_V/V_P [13].

(c) Using the equation (2.15) for $g(V)$ Scanlan [14] suggested evaluation using g_{max}.

At g_{max}, $\frac{dg(V)}{dV} = 0$, and

$$\frac{dg(V)}{dV} = (V-V_V)^3 + 3(V-V_V)^2(V-V_P) = 0$$

gives

$$V = \frac{V_V + 3V_P}{4} \quad .$$

Hence substituting for V into (2.14):

$$- g_{max} = - \frac{27}{64} \frac{(V_V-V_P)}{4} (V_V-V_P)^3 K \quad .$$

Hence

$$g(V) = g_{max} \frac{256}{27} \frac{(V-V_P)(V-V_V)^3}{(V_V-V_P)^4} \quad , \qquad (2.16)$$

and

$$I(V) = \int g(V)\,dV$$

$$= \frac{256}{540} \frac{g_{max}}{(V_V-V_P)^4} V \left\{ \begin{array}{l} 4V^4 - 5(3V_V+V_P)V^3 + 20V_V(V_P+V_V)V^2 \\ -10V_V^2(3V_P+V_V)V + 20V_V^3V_P \end{array} \right\} + K' \quad . \qquad (2.17)$$

The constant of integration, K', can be evaluated from the choice of axes.

(d) K. Tarnay[12] suggested still another approximation considering: (a) the field-emission current due to electrons passing from valence band to conduction band and (b) the current due to electrons tunneling from conduction band to valence band. His expression is as follows:

$$I(V) = a(V_V - V)^2 \tanh(qV/2kT) + g_V V \ , \qquad (2.18)$$

where

$$a = \frac{I_V - g_V V_V}{(V_V - V_P)^2 \tanh(qV_P/2kT)} \ , \text{ and } \ g_V = \frac{I_V}{V_V} \ .$$

This expression gives a poor approximation to experimental curves, especially in the negative-conductance region.

(e) Two-term exponential approximation:

Observation of tunneling current and direct-injection diode current components, led A. Ferendici and W. H. Ko [11] to suggest a simple two-term approximation of the static current-voltage characteristic of a tunnel diode.

$I_1(V)$ = Tunneling-current component (Figure 2.8).

$I_2(V)$ = Ordinary diode injection current component.

$$I(V) = I_1(V) + I_2(V) = AVe^{-aV} + B(e^{bV} - 1) \ . \qquad (2.19)$$

This two-term fit generally gives ±5% accuracy over the entire curve. The accuracy can be increased over

any desired region by selecting the pilot points from that region for evaluation of constants A, a, B and b. (see Appendix A.)

2.6 Equivalent Circuit

The current-voltage characteristic of a tunnel diode junction is explained in Section 2.3. This current flows through a p-n junction which is essentially depleted of mobile carriers. Owing to the existing voltage across this depletion layer, there are flux lines and a related capacitance associated with the junction. Therefore the tunneling junction is represented by a varying conductance shunted by a varying capacitance. The junction capacitance, $C_d(V_D)$, is a function of junction voltage, V_D [15,16]. For a step junction, which is the case for the tunnel junction, the junction capacitance, C_d, is proportional to $(V_D-V_c)^{-1/2}$.

$$C_d \propto (V_c-V_D)^{-1/2} \text{ for } V_D < V_V \tag{2.20}$$

where V_D = junction voltage

and V_c = contact potential, (n with respect to p)

$\approx$ + 0.6 volts for Ge, and

$\approx$ + 1.1 volts for GaAs.

The electrons traversing the tunnel junction travel through the semiconductor bulk material. The electron collisions with the crystal lattice give rise to a resistance r_s termed 'spreading' or 'series resistance.' The value of

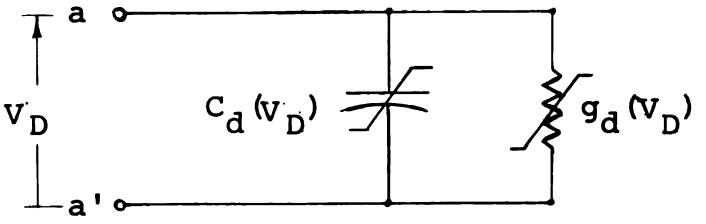


Figure 2.9. Equivalent circuit for a tunneling junction.

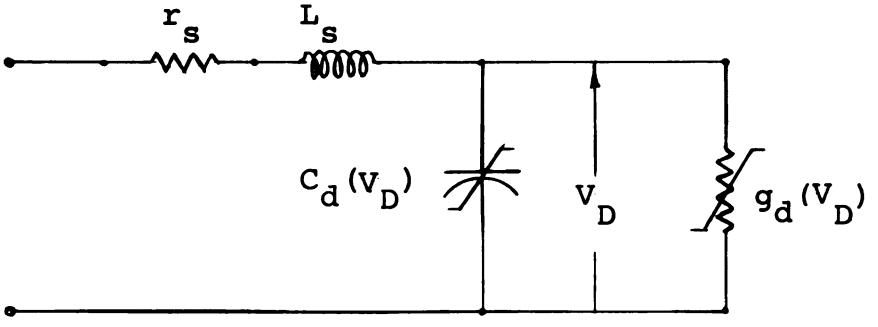


Figure 2.10. Equivalent circuit of a tunnel diode.

this series resistance depends upon the doping level and the geometry of the diode. The physical length of the lead from the semiconductor to external terminals gives rise to a series inductance, L_s, of the order of a few nanohenries. The series resistance, r_s, and the series inductance, L_s, are represented in series with the tunnel-junction. The resulting equivalent circuit of the tunnel diode is as shown in Figure 2.10. The validity of this equivalent circuit was verified by Gartner and Schuller's [17] experiments.

Computer calculations herein will use this equivalent circuit with $C_d(V_D) = C_D$. The effect of considering C_d as a function of V_D will also be examined.

CHAPTER 3

THE TUNNEL-DIODE OSCILLATOR

3.1 Introduction

A tunnel diode can be used in negative-resistance amplifiers [18,19] and in negative-resistance oscillators [5,14]. It can also be used as a detector or as a mixer, in which case the variation of negative resistance with the signal level is essential. In all these cases the diode must be biased in the negative-resistance region. A tunnel diode can be biased to produce three different potential conditions: (1) bistable, (2) monostable, and (3) astable. These are shown in Figure 3.1.

In its negative-resistance region, a tunnel diode can be biased two ways, viz., bistable and astable. In bistable biasing the two stable points are a anc c. This type of biasing is used in switching type circuits [5]. The astable biasing is used in amplifiers, oscillators, etc. The tunnel diode used as an oscillator circuit element is considered here.

3.2 Stability Criterion for the Tunnel-Diode Circuits

In a tunnel-diode oscillator circuit, the tunnel diode is biased in the negative conductance region. The

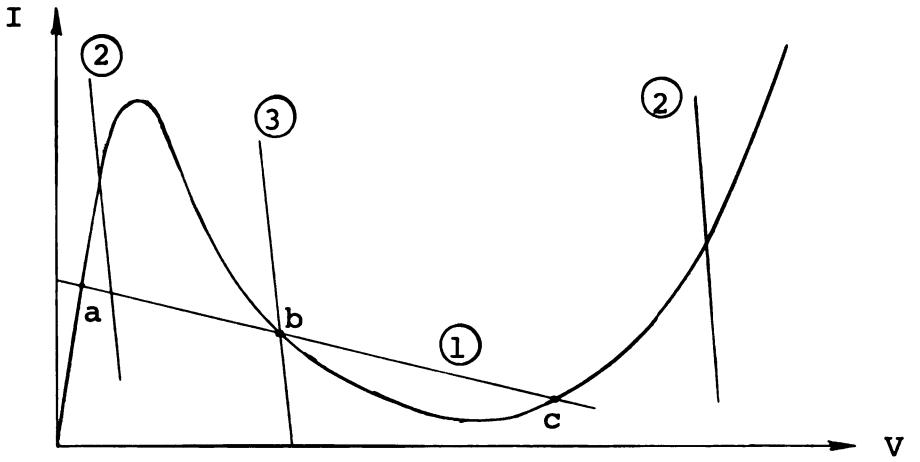


Figure 3.1 Biasing a tunnel diode: (1) bistable, (2) monostable and (3) astable.

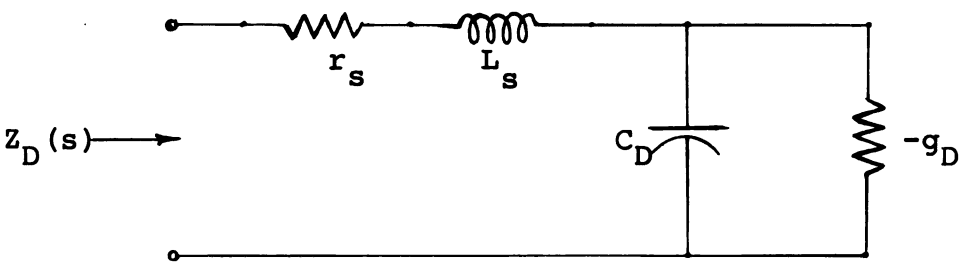


Figure 3.2 Small-signal equivalent circuit of a tunnel diode.

circuit is designed to be unstable so small-signal oscillations will start due to circuit noise or transient effect and grow. The circuit stability is in part determined by small-signal analysis.

The small-signal equivalent circuit for the tunnel diode is shown in Figure 3.2. Here $-g_D$ is the value of negative conductance at the dc bias point, V_D.

The loop impedance of the circuit of Figure 3.3 is $Z_c(s) + Z_D(s)$, where $Z_D(s)$ is the impedance of a two-terminal active device and $Z_c(s)$ is the passive network impedance. As shown in Appendix B, the circuit is stable if $Z_c(s) + Z_D(s) = 0$ has no solution in the closed right-half s-plane, viz., $Re(s) > 0$ [2].

The above definition of stability is derived from the small-signal, that is, linear analysis of the device. The following example of a small-signal analysis of tunnel-diode oscillator circuit, Figure 3.4, gives a procedure to obtain (G, C) parameter values so that $Z_c(s) + Z_D(s) = 0$ has a root in the right-half s-plane.

Consider the tunnel-diode equivalent circuit shunted with a parallel G-C circuit as shown in Figure 3.4.

For this circuit

$$Z_c(s) = \frac{1}{G + Cs} \quad , \tag{3.1a}$$

$$Z_D(s) = r_s + L_s s + \frac{1}{-g + C_D s} \quad , \tag{3.1b}$$

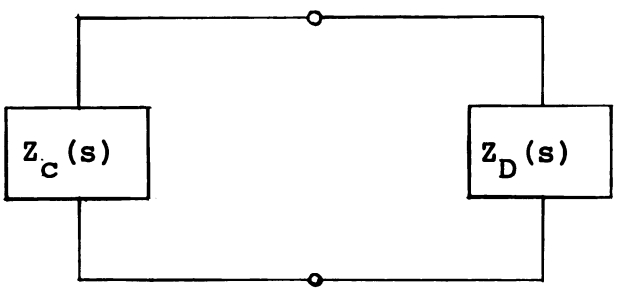


Figure 3.3 Circuit showing connection of circuit with impedance, $Z_C(s)$ to the diode with impedance, $Z_D(s)$.

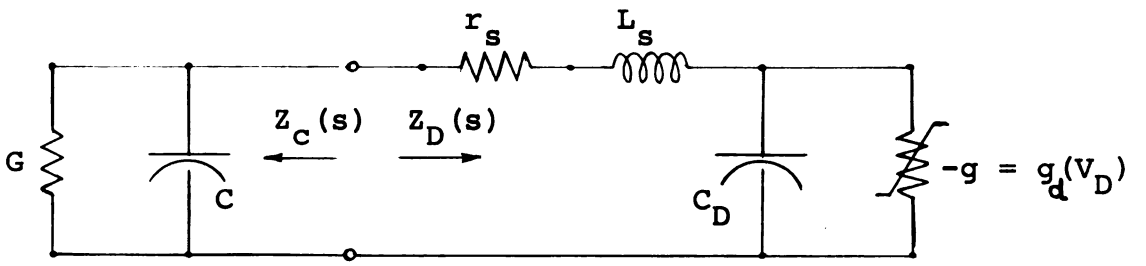


Figure 3.4 Small-signal equivalent circuit of the tunnel diode with a parallel G-C network.

where -g is the negative conductance of the intrinsic tunnel diode at the dc bias point, V_D. The loop impedance is

$$Z_c(s) + Z_D(s) = \frac{(-g+C_Ds) + (r_s+L_ss)(G+Cs)(-g+C_Ds) + (G+Cs)}{(G+Cs)(-g+C_Ds)} . \tag{3.2}$$

For stability [3], examine the characteristic equation,

$$Z_c(s) + Z_D(s) = 0 = as^3 + bs^2 + cs + d, \tag{3.3}$$

where

$$a = C_DCL > 0 ,$$

$$b = -gCL_s + C_D(r_sC + GL_s) ,$$

$$c = -g(r_sC + GL_s) + r_sGC_D + C_D + C \quad \text{and}$$

$$d = G - g - r_sGg ,$$

to determine whether all roots are in the left-half plane, (LHP).

If all the coefficients of the characteristic equation are positive then all the roots will be in LHP. Therefore, for d > 0 implies

$$\left(G + \frac{1}{r_s}\right) > g . \tag{3.4}$$

This result constitutes the condition for dc stability.

Since Equation (3.3) has real coefficients, the complex roots must be a conjugate pair. The necessary condition, according to Routh's algorithm, for the complex roots of (3.3) to be in LHP is (bc-da) < 0. Introducing the

values of the coefficients,

$$bc - da = A_1G^2 + A_2G + A_3 = F(G,C) \ , \tag{3.5}$$

where

$$A_1 = r_sL_sC_D^2 - gC_DL_s^2 \ ,$$

$$A_2 = -gC_Dr_sCL_s + r_s^2 C_D^2 C + L_sC_D^2 + g^2CL_s^2 \ ,$$

$$A_3 = r_sC^2C_D(1-gr_s) + r_sCC_D^2 + gC^2L_s(gr_s-1) \ .$$

Consider first a pair (G_o, C_o) of circuit values such that the complex roots are on the imaginary axis. Thus $s = \pm j\omega_o$ with ω_o as the desired operating frequency. Substituting $s = j\omega_o$ into (3.3) and using

$$\mathrm{Re}[Z_c(j\omega_o) + Z_D(j\omega_o)] = 0 \ , \tag{3.6}$$

and $\quad \mathrm{Im}[Z_c(j\omega_o) + Z_D(j\omega_o)] = 0 \ ,$

the following equations are obtained:

$$\begin{aligned} G_o(r_sC_D - gL_s) + C_o(1 - gr_s - C_DL_s\omega_o^2) &= 0 \ , \\ G_o(1 - gr_s - C_DL_s\omega_o^2) + C_o(gL_s - r_sC_D) &= 0 \ . \end{aligned} \tag{3.7}$$

Next, the value of G_o (and/or C_o) are altered such that (3.3) has a complex conjugate root, $s_o = \sigma_o \pm j\omega_o$ with $\sigma_o > 0$. The correct direction of change to G_o is determined by evaluating $\left.\frac{\partial F(G,C)}{\partial G}\right]_{(G_o,C_o)}$. If the derivative

is positive, G_o is increased, otherwise G_o is decreased to get $\sigma_o > 0$.

$$\frac{dF(G,C)}{dG} = 2GL_sC_D(r_sC_D - gL_s) + L_sC_D^2 + C(r_s^2C_D^2 + g^2L_s^2) - 2r_sgL_sC_DC \quad . \tag{3.8}$$

Thus in the small-signal analysis of the tunnel-diode oscillator (Figure 3.4), there must be a root, $s_o = \sigma_o + j\omega_o$, of the loop impedance, with $\sigma_o > 0$. If so, then over a period of a small-signal oscillation, the energy generated by the negative conductance of the tunnel diode is more than the energy dissipated by the lossy elements. Once the oscillations start and grow in amplitude, the small-signal conductance, -g, no longer applies because it it constant only over a very small region around the bias point. For large-signal oscillations the voltage-dependent diode conductance, $g_d = d\, i(v_D)/d\, v_D$, must be used. In the large-signal operation, the diode will operate part of the time in the region where the diode small-signal conductance is positive. Additional losses are produced. These additional losses together with the nonlinear characteristic of the diode establish a steady-state operation. For steady-state operation, the average power generated by the diode is equal to the average power dissipated by the lossy elements of the circuit.

3.3 Operating Frequency and Circuit

The type of circuit used depends in part on the operating frequency, f_o. The terminal impedance of the tunnel diode shown in Figure 3.2 is

$$Z_D(j\omega) = \left[r_s - \frac{g_D}{g_D^2 + (\omega C_D)^2} \right] + j\omega \left[L_s - \frac{C_D}{g_D^2 + (\omega C_D)^2} \right] \tag{3.9}$$

$$= \mathrm{Re}(Z_D) + j\ \mathrm{Im}(Z_D).$$

(a) Resistive cut-off frequency, f_R.

The resistive cut-off frequency, $f_R = \omega_R/2\pi$ is the value of ω for which $\mathrm{Re}(Z_D) = 0$. Equating $\mathrm{Re}(Z_D) = 0$ gives

$$r_s - \frac{g_D}{g_D^2 + (\omega_R C_D)^2} = 0 . \tag{3.10a}$$

Solving for ω_R,

$$\omega_R = \frac{1}{C_D} \sqrt{\frac{g_D}{r_s} - g_D^2} . \tag{3.10b}$$

For $\omega_o < \omega_R$,

$$\mathrm{Re}[Z_D(\omega_o)] < 0 . \tag{3.10c}$$

For $\omega_o > \omega_R$, the terminal resistance is no longer negative, and the tunnel diode cannot be used as an oscillator for frequencies greater than the resistive cut-off frequency.

(b) Self-resonant frequency, f_S.

The self-resonant angular frequency, $\omega_S = 2\pi f_S$, is the value of ω for which $\mathrm{Im}(Z_D) = 0$.

$$\mathrm{Im}(Z_D) = \omega_S L_s - \frac{\omega_S C_D}{g_D^2 + (\omega_S C_D)^2} = 0 \ . \qquad (3.11a)$$

Solving for ω_S,

$$\omega_S = \frac{1}{C_D}\sqrt{\frac{C_D}{L_s} - g_D^2} \ . \qquad (3.11b)$$

If $\omega_o < \omega_S$,

$$\mathrm{Im}[Z_D(\omega_o)] < 0 \ , \qquad (3.11c)$$

and if $\omega_o > \omega_S$,

$$\mathrm{Im}[Z_D(\omega_o)] > 0 \ . \qquad (3.11d)$$

With present technology, tunnel diodes with resistive cut-off frequencies up to 30 GHz can be produced. Generally the resistive cut-off frequency is found to be greater than the self-resonant frequency, f_S.

The tunnel-diode small-signal equivalent circuit with a load circuit of terminal impedance, $Z_L(\omega)$, forming an oscillator, is shown in Figure 3.5. Here $-g_D$ is the incremental conductance of the tunnel diode at the bias point; r_s, L_s and C_D are diode parameters explained in Section 2.6.

With the small-signal operating frequency, f_o, the following conditions must be satisfied for a steady-state solution:

$$[Z_L(\omega_o) + Z_D(\omega_o)]I = 0 , \tag{3.12a}$$

or

$$Re[Z_L(\omega_o) + Z_D(\omega_o)] = 0 , \tag{3.12b}$$

and

$$Im[Z_L(\omega_o) + Z_D(\omega_o)] = 0 . \tag{3.12c}$$

From Equations (3.10c) and (3.11d) for $f_o < f_s$, $Im(Z_D(\omega_o)) < 0$, a capacitive reactance, and for $f_o > f_s$, $Im(Z_D(\omega_o)) > 0$, an inductive reactance. For the circuit operating as an oscillator and for $f_o < f_s$, $Im(Z_L(\omega_o)) > 0$, an inductive load, and for $f_o > f_s$, $Im(Z_L(\omega_o)) < 0$, a capacitive load. Thus, selection of an operating frequency dictates the nature of the load-circuit necessary for oscillation.

Here the aim is to concentrate on high-frequency operation, $f_o > f_s$; only capacitive-load circuits of the type shown in Figures 3.6b and 3.6c will be used. The oscillator circuit with the operating frequency $f_o < f_s$, load circuit inductive, was analyzed on a small-signal basis by Chow [5]. The large-signal analysis with certain assumptions was carried out by Kim and Brandli [4], Coerver [8], and others [7,9,14,17].

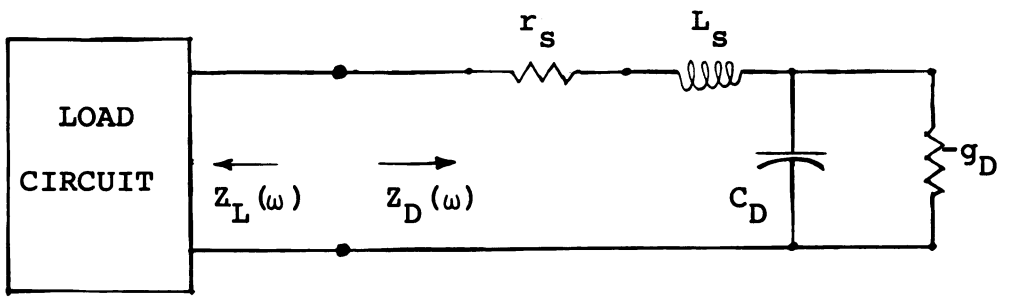


Figure 3.5 Tunnel-diode oscillator circuit.

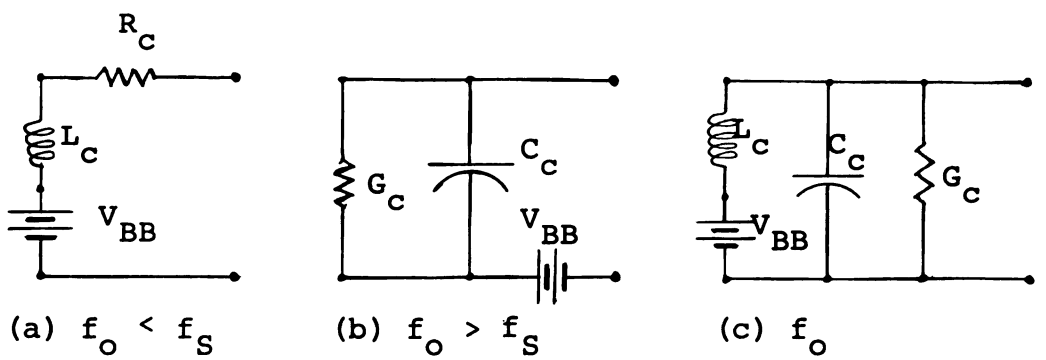


Figure 3.6 Load circuits for the tunnel-diode oscillator (a) inductive, (b) capacitive, (c) inductive or capacitive load depending on f_o.

V_{BB} is the dc bias voltage.

3.4 Oscillator Circuit

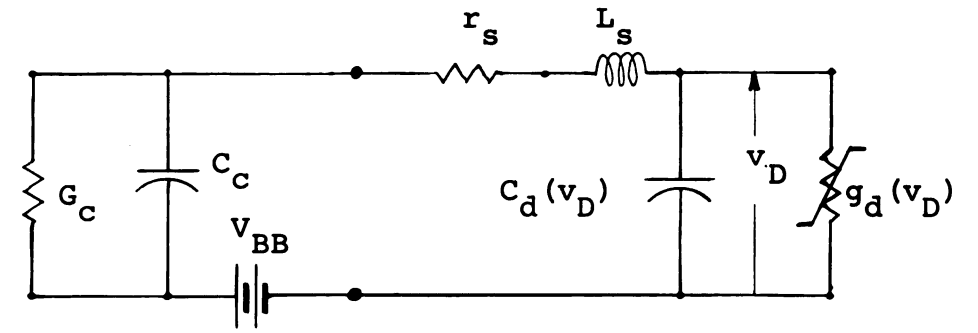
The tunnel-diode oscillator circuit with an operating frequency, f_o, which is greater than the self-resonant frequency, f_s, but less than the resistive cut-off frequency, f_R, $f_s < f_o < f_R$ is shown in Figure 3.7.

In the circuit of Figure 3.7b, the load circuit must be capacitive, viz., $2\pi f_o C_c' - (1/2\pi f_o L_c') > 0$. Parameters L_c' and C_c' can be calculated from the values of C_c and f_o considering $C_c' = kC_c$, $k > 1$.

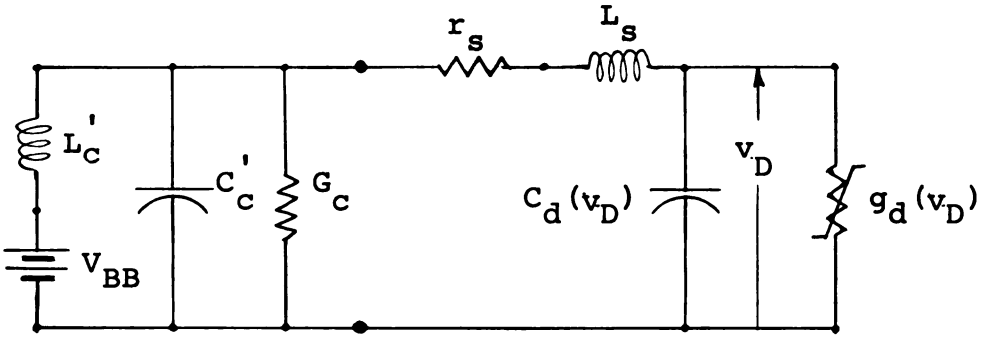
(a) Selection of an Operating Bias-point, V_D.

The tunnel diode as an oscillator circuit element must be biased in the negative-conductance region. The bias point, V_D, must lie between peak point, V_P, and valley point, V_V, i.e., $V_P < V_D < V_V$. It should be noticed from the V-I characteristic of the tunnel diodes that the valley region is flat compared to the peak region. This phenomenon is more pronounced in gallium-arsenide tunnel diodes than in germanium tunnel diodes (Figure 3.8). This indicates that the region with the higher negative resistance is flatter near the valley region than near the peak region.

The power generated by the diode depends on the voltage swing about the bias point and the incremental negative resistance of the tunnel diode. Since the higher negative-resistance region is flatter near the valley point, the bias point for maximum fundamental power should



(a)



(b)

Figure 3.7 Tunnel-diode oscillator circuits with an operating frequency $f_o > f_s$.

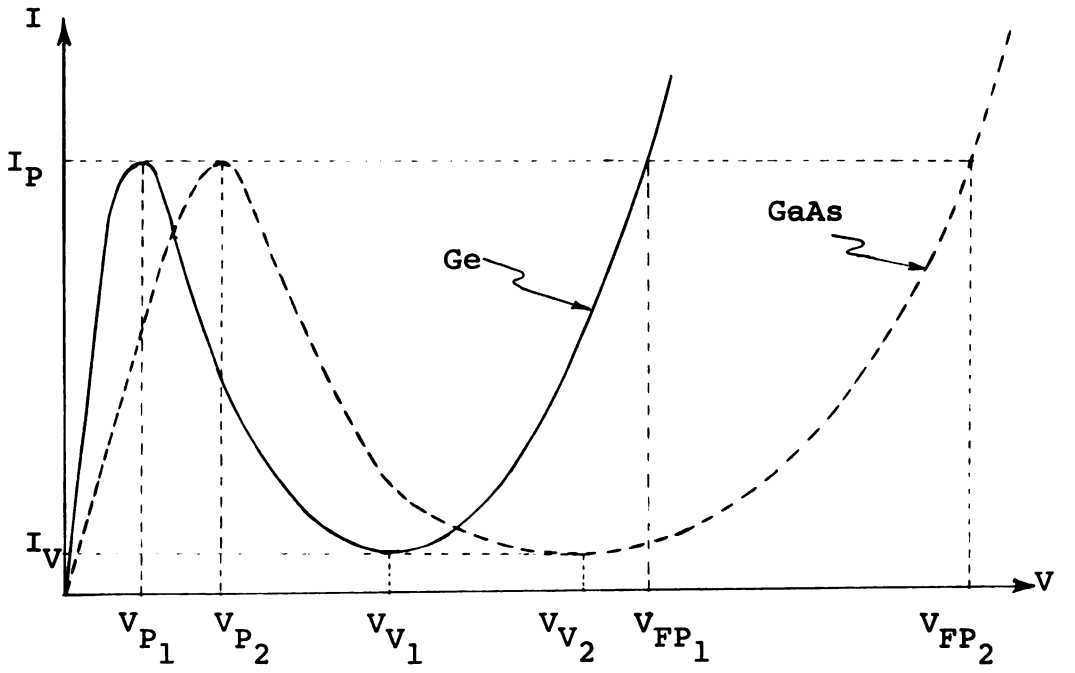


Figure 3.8 Current-voltage characteristics of
(1) Germanium tunnel diode, and
(2) Gallium-Arsenide tunnel diode.

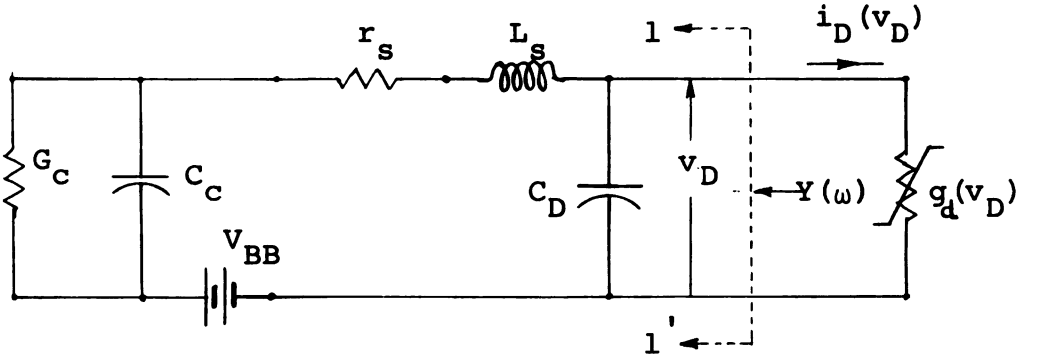


Figure 3.9 Tunnel-diode oscillator circuit.

be closer to the valley point, i.e., $(V_V - V_D) < (V_D - V_P)$. Sterzer [9] has shown in his computer calculations using $v_D(t) = V_D + V_o \sin(2\pi t/T)$ that the optimum bias voltage, V_D, for the maximum power generation is very close to the valley point. His results also show that the flatter the valley region, the closer will be the operating bias point, V_D, to the valley point, V_V. Similar results will be derived in Chapter 5.

(b) Load Parameters: G_c, C_c and V_{BB}.

The discussion of the stability of the tunnel-diode circuits in Section 3.2 pointed out that small-signal instability is essential for an oscillator circuit. The circuit parameters, G_c and C_c, are designed accordingly. The bias supply, V_{BB}, can be determined from the operating bias point, V_D, and from r_s and G_c,

$$V_{BB} = V_D + (r_s + \frac{1}{G_c})\ I_D(V_D) \ .$$

A tunnel-diode oscillator circuit is shown in Figure 3.9. Here $g(V_D)$ and C_D are the negative conductance and the junction capacitance respectively, at the quiescent point, V_D. Initially C_D is assumed constant. To the left of terminals 1-1', the admittance is $Y(\omega)$, a function of frequency. Node admittance for the circuit is

$$Y_{Node}(\omega) = Y(\omega) + g(V_D) \ .$$

The conditions for an oscillator with an operating frequency, f_o, are (see Appendix B, equations (B.11a) and (B.11b)):

(a) for the operating frequency of the oscillator to be f_o,

$$\mathrm{Im}[Y_{Node}(\omega_o)] = \mathrm{Im}[Y(\omega_o)] = 0 \ , \tag{3.13a}$$

and (b) for the oscillation to start (due to the circuit noise) and grow,

$$\mathrm{Re}[Y(\omega_o)] < |g_d(V_D)| \ . \tag{3.13b}$$

Let

$$R = r_s + \frac{G_c}{G_c^2 + (\omega_o C_c)^2} \ , \tag{3.14a}$$

and

$$\omega_o X = {}_oL_s - \frac{\omega_o C_c}{G_c^2 + (\omega_o C_c)^2} \ , \tag{3.14b}$$

then,

$$Y(\omega_o) = \frac{R}{R^2 + (\omega_o X)^2} + j\left(\omega_o C_D - \frac{\omega_o X}{R^2 + (\omega_o X)^2}\right). \tag{3.15}$$

$\mathrm{Im}[Y(\omega_o)] = 0$, implies

$$\omega_o C_D - \frac{\omega_o X}{R^2 + (\omega_o X)^2} = 0 \ . \tag{3.16}$$

Solving,

$$R^2 = \frac{\omega_o X}{\omega_o C_D} - \omega_o^2 X^2 \quad . \tag{3.17a}$$

This implies $\omega_o X$ must be positive. From (3.14b), $(\omega_o X)_{max} = \omega_o L_s$ when $C_c = 0$. Let $\omega_o X = k\omega_o L_s$, $k < 1$, then

$$R = \sqrt{\frac{k\omega_o L_s}{\omega_o C_D} - k^2 \omega_o^2 L_s^2} \quad . \tag{3.17b}$$

For R to be real,

$$\frac{kL_s}{C_D} - k^2 \omega_o^2 L_s^2 > 0. \quad \text{This implies } k < \frac{1}{\omega_o^2 L_s C_D} \quad .$$

Hence,

$$k \leq \min \left(1, \frac{1}{\omega_o^2 L_s C_D}\right) = k_{max} \quad . \tag{3.18}$$

Rewriting Equations (3.14a) and (3.14b) as:

$$R - r_s = R = \frac{G_c}{G_c^2 + (\omega_o C_c)^2} \quad , \tag{3.19b}$$

and

$$L_s - X = \chi = \frac{C_c}{G_c^2 + (\omega_o C_c)^2} \quad , \tag{3.19b}$$

and solving them simultaneously for G_c and C_c:

$$G_c = \frac{R}{R^2 + (\omega_o \chi)^2} \quad , \tag{3.20a}$$

and

$$C_c = \frac{X}{R^2 + (\omega_o X)^2} \ . \qquad (3.20b)$$

Thus for a different value of k a different set of values (G_c, C_c) for a given operating frequency, $f_o > f_s$ is obtained.

The condition (3.13b) for growing oscillations can be used to give a lower limit for the parameter, k. Using

$$\mathrm{Re}[Y(\omega_o)] = \frac{R}{R^2 + (\omega_o X)^2} < -g_d(V_D) \equiv g_D \ , \qquad (3.21)$$

substituting for R, from (3.17a), writing $X = kL_s$, and simplifying, gives:

$$\frac{C_D}{kL_s} < (g_D^2 + \omega_o^2 C_D^2) \ , \qquad (3.22a)$$

or

$$k > \frac{C_D/L_s}{g_D^2 + \omega_o^2 L_s^2} = k_{min} \ . \qquad (3.22b)$$

Thus, the bounds for parameter k are:

$$k_{min} = \frac{C_D/L_s}{g_D^2 + \omega_o^2 L_s^2} < k < \min\left(1, \frac{1}{\omega_o^2 L_s C_D}\right) = k_{max} \ . \qquad (3.23)$$

The set of values (G_{c_m}, C_{c_m}) evaluated for $k = k_{min}$ means that $\mathrm{Re}[Y(\omega_o)]\big|_{G_{c_m}, C_{c_m}} = g_D$. According to small-signal

analysis, this circuit is on the verge of instability and the oscillations may not grow or will grow very slowly. In computer calculations (see Chapter 4) exactly the same result is obtained. However, it should be kept in mind that the small-signal analysis is only a means to obtain suitable load parameters, G_c, C_c and V_{BB}, for an oscillator circuit. The circuit with G_c, C_c values evaluated for $k < k_{min}$ means it is a small-signal stable circuit. Large-signal analysis of the same circuit may nevertheless show instability as corresponding to oscillations as will be shown in Chapter 4.

As mentioned in Section 3.2, the circuit must be dc stable. That is, the diode biased in the negative-resistance region should have a unique dc operating point on its I-V characteristic, as indicated by Equation (3.24) and shown in Figure 3.10.

$$(G_c + \frac{1}{r_s}) > |-g_D| \ . \tag{3.24}$$

Thus the algorithm for designing a tunnel-diode small-signal oscillator circuit is as follows:

(a) Obtain tunnel-diode parameters C_D, r_s and L_s from the specification sheet of the diode.

(b) Obtain a static I-V characteristic for the tunnel diode.

(c) Calculate the static I-V characteristic for the intrinsic tunnel-diode junction from step (b). Next evaluate parameters A, a, B,

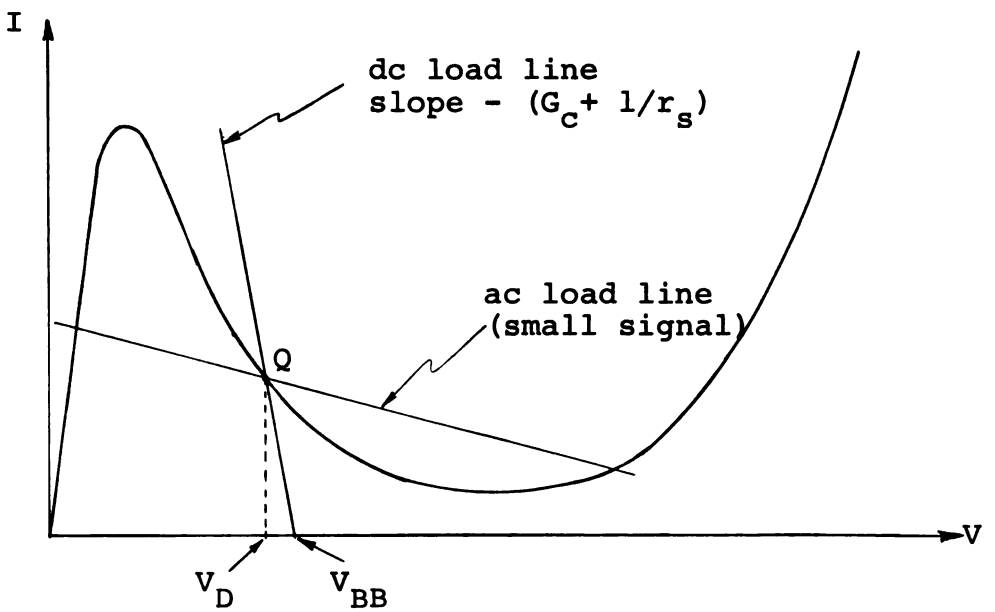


Figure 3.10. I-V characteristic of the intrinsic tunnel diode with dc and (small signal) ac load line for an oscillator circuit of Figure 3.9.

and b approximating this curve as outlined in Appendix A.

(d) Select an operating dc bias point, V_D, ($V_P < V_D < V_V$) and calculate $g_d(V_D)$. Equation (2.19) and $g(V) = dI/dV$ gives:

$$g_d(V_D) = Ae^{-aV_D}(1 - aV_D) + Bbe^{bV_D}. \qquad (3.25)$$

(e) Calculate two cutoff frequencies, f_R and f_S, and select an operating frequency, f_o, such that $f_S < f_o < f_R$. Calculate k_{max} and k_{min}.

(f) Evaluate the load conductance, G_c, and the load capacitance, C_c, for a value of k such that $k_{min} < k < k_{max}$.

(g) Check for dc stability according to (3.24). Finally, calculate

$$V_{BB} = V_D + (r_s + \frac{1}{G_c}) I_D(V_D).$$

This completes the design of a small-signal oscillator with an operating frequence, f_o.

CHAPTER 4

THE TUNNEL-DIODE OSCILLATOR CIRCUIT: ITS ANALYSIS AND SOLUTION

4.1 Introduction

The small-signal equivalent circuit of the tunnel diode developed in Chapter 2 gives very satisfactory results for the gain, bandwidth, etc., of a tunnel-diode amplifier or the cut-off frequencies of a small-signal oscillator [5,20]. However, this model fails to give satisfactory answers to the typical large-signal nonlinear problems such as the determination of the output waveform, harmonic content, etc., in a tunnel-diode circuit.

To perform large-signal analysis of the tunnel-diode oscillator circuit by analytical methods, the characteristic of the negative-resistance element, the intrinsic tunnel diode, must be simplified considerably. Kim and Brandli [4] approximated the I-V characteristic of the intrinsic tunnel diode by a third-degree polynomial about the operating bias point [4,5,22], as

$$i(v) = -g_D v + hv^3 \ , \tag{4.1a}$$

where

$$-g_D = -\frac{3\Delta I}{2\Delta V} = \text{conductance at the dc bias point,} \tag{4.1b}$$

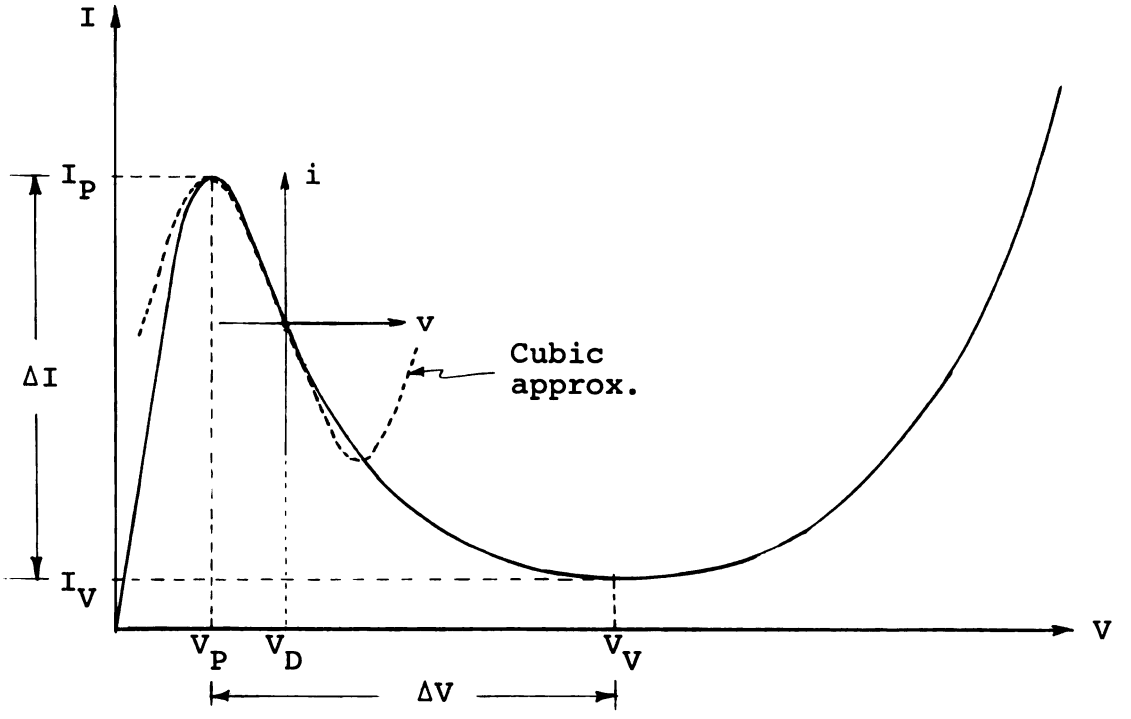


Figure 4.1. I-V characteristic of the tunnel diode and the cubic approximation (i-v) used by Kim and Brandli.

$$h = \frac{2\Delta I}{(\Delta V)^3} , \qquad (4.1c)$$

$$\Delta V = V_V - V_P , \text{ and } \Delta I = I_P - I_V . \qquad (4.1d)$$

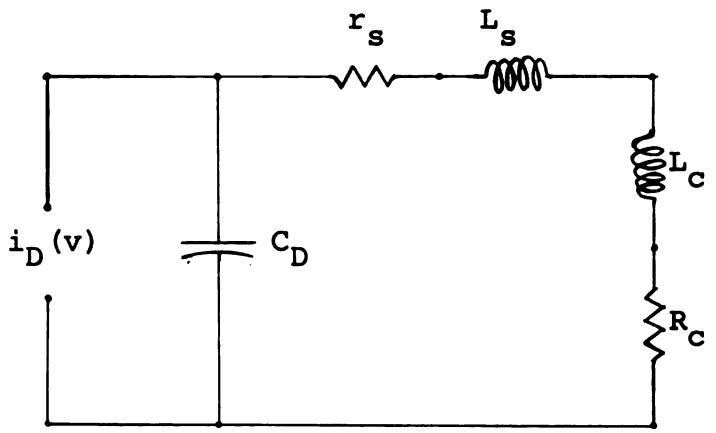
The analysis by Kim and Brandli assumes $v = V \cos(\omega t)$, a perfect sinusoidal voltage about the dc bias point, V_D, at the intrinsic tunnel-diode terminals. Despite the poor approximation to the I-V characteristic (Figure 4.1) and the pure sinusoidal voltage assumption, meaningful qualitative results were obtained.

4.2 Solution by Coerver and Sterzer

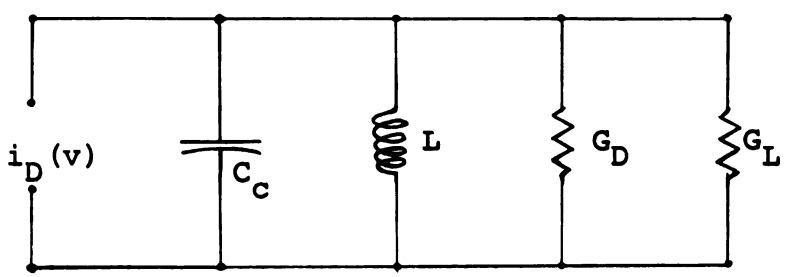
Coerver [8] carried out an analysis of a tunnel-diode oscillator using a fifth degree polynomial similar to Equation (2.17)[14], to approximate the intrinsic tunnel-diode static I-V characteristic. He simplified the oscillator circuit by neglecting harmonics, i.e., assuming single-frequency operation (Figure 4.2). Also he assumed a circuit operating frequency, $f_o < f_S$. Coerver's calculations show that the dc bias point, V_D, for the maximum fundamental power should be such that

$$(V_V - V_D)/(V_V - V_P) = 0.4 .$$

Sterzer [9] used a tenth degree polynomial to approximate the static I-V characteristic of the intrinsic tunnel diode. His computer calculations show that the dc bias point for generating the maximum rf power should be



(a)



(b)

Figure 4.2. (a) Coerver's tunnel-diode oscillator circuit

(b) Equivalent circuit of (a) at a frequency $f_o = \omega_o/2\pi < f_s$ where G_L is load conductance and G_D is to account for diode and cavity losses and L is the equivalent shunt inductance.

closer to the valley region. Another important result is that the maximum power generated by diodes with flat valleys is greater than the power from diodes with narrow valleys.

For an accurate solution a good approximation to the nonlinear I-V characteristic is needed, but additionally, the effect of higher harmonics must be considered. A better approach is to formulate the solution of the oscillator circuit in the time domain. If a steady-state time-domain solution is available, harmonic analysis can be employed to determine harmonic content. Because of the nonlinearity of the device, numerical methods of analysis must be used.

The time-domain solution of the large-signal oscillator circuit is given in the remainder of this chapter. A Fourier analysis of $v_D(t)$ as constituting a frequency-domain signal of the form,

$$v_D(t) = V_D + \sum_{k=1}^{K} \left[V_{s_k} \sin\omega_o t + V_{c_k} \cos\omega_o t \right], \quad K \geq 2$$

is carried out in Chapter 5.

4.3 Large-Signal Tunnel-Diode Oscillator Circuit

The complete large-signal oscillator circuit with operating frequency $f_o > f_s$, i.e., capacitive load circuit, is shown in Figure 4.3.

The following set of equations describes the tunnel-diode section of the circuit.

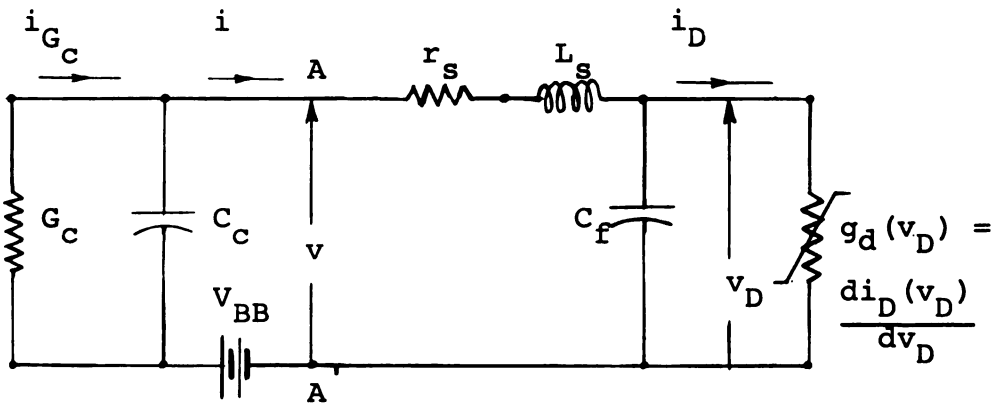


Figure 4.3. Complete large-signal tunnel-diode oscillator circuit with parallel G_c - C_c load, for operating frequency $f_o > f_s$.

Let $i = i(t)$, $v = v(t)$ and $v_D = v_D(t)$. Next, applying Kirchoff's law at terminal A-A':

$$i_D(v_D) + C_d \frac{dv_D}{dt} = i \ . \tag{4.2}$$

The voltage drop across the extrinsic elements, r_s and L_s is:

$$L_s \frac{di}{dt} + r_s i = v - v_D \ . \tag{4.3}$$

The solution of (4.3) with $i(t = 0) = i(0)$ is:

$$i(t) - i(0) = \frac{e^{-\frac{r_s}{L_s}t}}{L_s} \int_0^t [v(t') - v_D(t')]e^{\frac{r_s}{L_s}t'} dt' \ . \tag{4.4}$$

Substituting for $i(t)$ from (4.2) and using the notations,

$$\dot{v}_D = \frac{dv_D}{dt} \quad \text{and} \quad \ddot{v}_D = \frac{d^2 v_D}{dt^2} \ ,$$

results in

$$C_d \dot{v}_D + i_D(v_D) = i(0) + \frac{e^{-\frac{r_s}{L_s}t}}{L_s} \int_0^t [v(t') - v_D(t')]e^{\frac{r_s}{L_s}t'} dt' \ . \tag{4.5}$$

Differentiating equation (4.5) with respect to time:

$$c_d\ddot{v}_D + i_D'(v_D)\dot{v}_D = -\frac{r_s}{L_s^2} e^{-\frac{r_s}{L_s}t} \int_0^t [v(t')-v_D(t')]e^{\frac{r_s}{L_s}t'} dt' + \frac{v-v_D}{L_s} , \quad (4.6a)$$

$$= -\frac{r_s}{L_s} [i(t) - i(0)] + \frac{v-v_D}{L_s} , \quad (4.6b)$$

$$= -\frac{r_s}{L_s} [i_D(v_D) + c_d\dot{v}_D - i(0)] + \frac{v-v_D}{L_s} , \quad (4.6c)$$

where

$$i_D'(v_D) = \frac{d}{dv_D} (i_D(v_D)) = g_d(v_D) .$$

Rearranging Equation (4.6c):

$$c_D\ddot{v}_D + \left[g_d(v_D)+\frac{r_s C_d}{L_s}\right]\dot{v}_D + \frac{r_s i_D(v_D)}{L_s} + \frac{v_D}{L_s} = \frac{v+i(0)r_s}{L_s} . \quad (4.7)$$

Equation (4.7) completely describes the operation of the tunnel diode in the circuit of Figure 4.2.

The load circuit to the left of terminals A-A' in Figure 4.3 is described by the following set of equations:

$$i_{G_c}(t) = i(t) + C_c\dot{v} , \quad (4.8a)$$

$$v(t) = V_{BB} - \frac{1}{G_c} [i(t) + C_c\dot{v}] , \quad (4.8b)$$

$$= V_{BB} - \frac{1}{G_c} [i_D(v_D) + C_d\dot{v}_D + C_c\dot{v}]. \quad (4.8c)$$

From Equation (4.3), $\dot{v} = \frac{d}{dt}(v(t))$ is

$$\dot{v} = L_s \frac{d^2 i(t)}{dt^2} + r_s \frac{di(t)}{dt} + \dot{v}_D$$

$$= L_s \left[i_D''(v_D)\dot{v}_D^2 + i_D'(v_D)\ddot{v}_D + C_d \dddot{v}_D \right] \qquad (4.9)$$

$$+ r_s \, i_D'(v_D)\dot{v}_D + C_d \ddot{v}_D + \dddot{v}_D$$

where $\frac{di(t)}{dt}$ and $\frac{d^2 i(t)}{dt^2}$ are derived from Equation (4.2).

Substituting Equation (4.9) into (4.8c) and the resulting expression for v into Equation (4.7), produces a single nonlinear differential equation in v_D. The expression for $i_D(v_D)$ can be selected as any one of the following expressions, (repeated from Section 2.5):

$$i_D(v_D) = a_o + a_1 v_D + a_2 v_D^2 + \text{---} + a_N v_D^N \ , \ N \geq 1 \ ,$$

or

$$i_D(v_D) = \frac{I_P - I_V}{(V_V - V_P)^5} \left[5(v_D - V_P)(v_D - V_V)^4 - (v_D - V_V)^5 \right] + I_V \ ,$$

or

$$i_D(v_D) = a(V_V - v_D)^2 \tanh \frac{q v_D}{2kT} + g_V v_D \ ,$$

or

$$i_D(v_D) = A v_D e^{-a v_D} + B\left(e^{b v_D} - 1 \right) \ .$$

The complete equation describing the oscillator circuit shown in Figure 4.3 is obtained by substituting for v, $i_D(v_D)$ and $i_D'(v_D)$ (from Equation (4.10)) into (4.7). The resulting equation is a third-order, second-degree nonlinear differential equation in v_D. Analytical solutions

are not known, and straightforward analytical approximations quickly become complex and require numerical approximations. A feasible method of solving specific numerical cases is to use a digital computer to form time-domain solutions on an incremental time basis.

4.4 System Model of the Oscillator Circuit

The primary purpose of the system approach is to develop a set of first-order differential equations describing the oscillator circuit of Figures 3.7a and 3.7b. Also, this approach permits the study of the effects of voltage dependency of junction capacitance, $C_d(v_D)$, without any difficulty.

The large-signal oscillator circuit shown in Figure 3.7a is redrawn as Figure 4.4a for convenience.

The system graph of Figure 4.4 is shown in Figure 4.4b. The notations, lettering, and the direction of the arrows are the same as described in reference [21]. The circuit tree is shown in heavy lines.

The system model for the oscillator circuit is derived as follows:

(1) The set of equations describing the circuit elements, capacitors C_c, C_d and inductor L_s, is

$$\frac{d}{dt}\begin{bmatrix} v_1 \\ v_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} \frac{1}{C_c} & o & o \\ 0 & \frac{1}{C_d} & 0 \\ 0 & 0 & \frac{1}{L_s} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ v_3 \end{bmatrix} . \qquad (4.11)$$

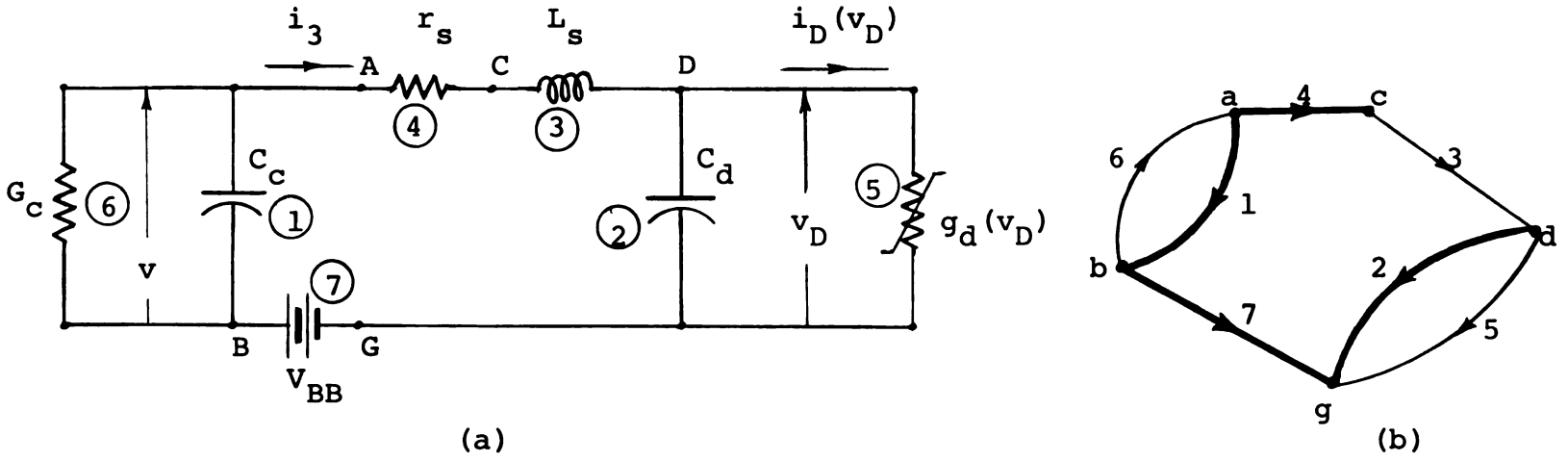


Figure 4.4. Large-signal tunnel-diode oscillator circuit (a) Schematic, (b) System-graph.

(2) Writing the circuit and the cut-set equations [21] from the system-graph of Figure 4.4b:

$$i_1 = i_6 - i_3 = v_6 G_c - i_3 = -v_1 G_c - i_3 \ . \tag{4.12a}$$

$$i_2 = i_3 - i_5 = i_3 - i_D(v_D) = i_3 - i_D(v_2) \ . \tag{4.12b}$$

$$v_3 = -v_4 + v_1 + v_7 - v_2 = - i_3 r_s + v_1 + V_{BB} - v_2 \ . \tag{4.12c}$$

Writing (4.12) in matrix notation,

$$\begin{bmatrix} i_1 \\ i_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} -G_c & 0 & -1 \\ 0 & -i_D(\ ) & 1 \\ 1 & -1 & -r_s \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ i_3 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ V_{BB} \end{bmatrix} . \tag{4.13}$$

(3) Substituting Equation (4.13) into (4.11)

$$\frac{d}{dt}\begin{bmatrix} v_1 \\ v_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} \frac{1}{C_c} & 0 & 0 \\ 0 & \frac{1}{C_d} & 0 \\ 0 & 0 & \frac{1}{L_s} \end{bmatrix} \left\{ \begin{bmatrix} -G_c & 0 & -1 \\ 0 & -i_D(\ ) & 1 \\ 1 & -1 & r_s \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ i_3 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ V_{BB} \end{bmatrix} \right\}$$

$$= \begin{bmatrix} -G_c/C_c & 0 & -1/C_c \\ 0 & -i_D(\ )/C_d & 1/C_d \\ 1/L_s & -1/L_s & -r_s/L_s \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ i_3 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ V_{BB}/L_s \end{bmatrix} . \tag{4.14}$$

In this set of differential equations, v can be substituted for v_1 and v_D for v_2. This substitution results in the following set of equations:

$$\frac{d}{dt}\begin{bmatrix} v \\ v_D \\ i_3 \end{bmatrix} = \begin{bmatrix} -\frac{G_c}{C_c} & 0 & -\frac{1}{C_c} \\ 0 & -\frac{i_D(\ )}{C_d} & \frac{1}{C_d} \\ \frac{1}{L_s} & -\frac{1}{L_s} & -\frac{r_s}{L_s} \end{bmatrix} \begin{bmatrix} v_1 \\ v_D \\ i_3 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \frac{V_{BB}}{L_s} \end{bmatrix} . \qquad (4.15)$$

This describes the large-signal oscillator of Figure 4.4. Solving this set of equations on a digital computer is relatively easy compared to solving the higher-order differential equation, Equation (4.7).

For initial conditions, the values of $v(t)$, $v_D(t)$ and $i_3(t)$ for $t = 0$, must be specified. The bias voltage, V_{BB} is obtained from $V_{BB} = V_D + I_D(v_D)\left[r_s + 1/G_c\right]$ where V_D is the intrinsic diode dc bias point. If $v_D(t = 0) = V_D$, then a trivial solution of Equation (4.15) is obtained because $\dot{v}_D = \dot{v} = \dot{i}_3 \equiv 0$. In an actual oscillator, the electrical noise in the circuit may start the oscillations, which in turn begin to grow in amplitude due to small-signal instability. In computer simulation the initial perturbation is provided by selecting $v_D(t = 0)$ not equal to the dc bis point, V_D. A satisfactory choice of initial conditions is:

$$
\begin{aligned}
&\text{at} \quad t = 0 \qquad v_D(0) = V_B (\neq V_D) \ , \\
&\text{then} \qquad\quad i_3(0) = i_D(V_B) \ , \\
&\text{and} \qquad\quad v(0) = V_B + i_D(V_B) r_s \ , \\
&\qquad\qquad\quad = V_{BB} - i_D(V_B)/G_c \ .
\end{aligned}
\tag{4.16}
$$

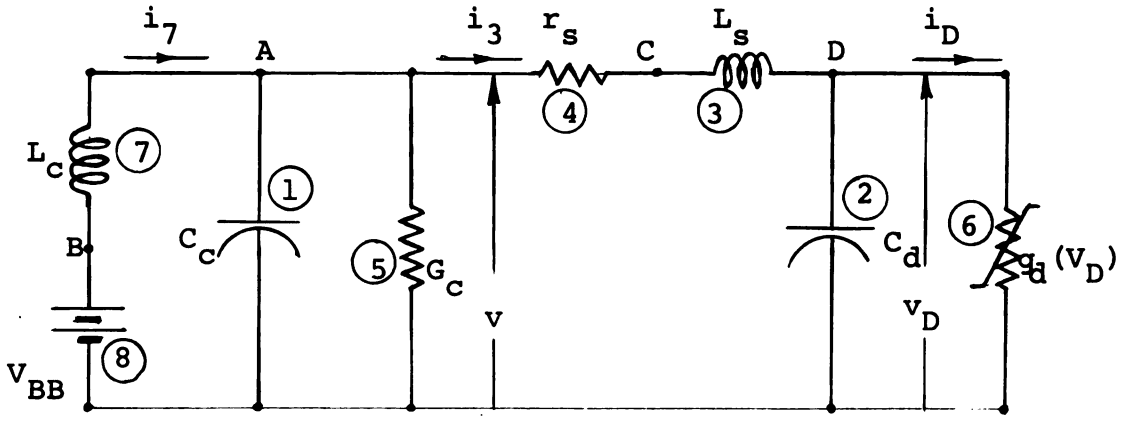
These initial conditions will give non-zero values to $\dot{v}_D$, $\dot{v}$ and $\dot{i}_3$. The ratio, $V_B/V_D \neq 1$, is equivalent to noise excitation in an actual oscillator circuit.

A similar set of first-order differential equations, describing the second form of the oscillator circuit shown in Figure 3.7b, will be derived next.

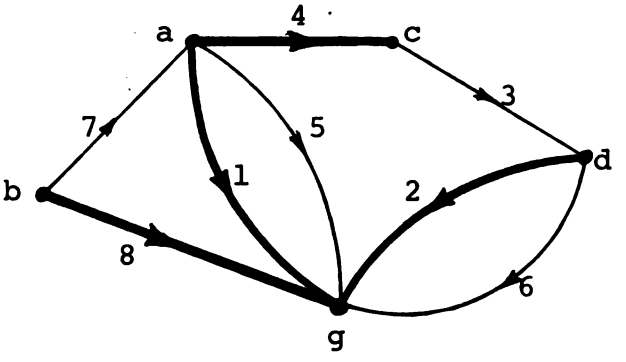
The large-signal oscillator circuit shown in Figure 3.7b is redrawn as Figure 4.5a for convenience. It is an equivalent to the circuit considered in the preceding section. Its system graph is shown in Figure 4.5b.

Now to derive the state model of the oscillator circuit, write the set of equations describing the C_c, C_d, L_s and L_c circuit elements as follows:

$$
\frac{d}{dt}\begin{bmatrix} v_1 \\ v_D \\ i_3 \\ i_7 \end{bmatrix} = \begin{bmatrix} \frac{1}{C_c} & & 0 & 0 \\ 0 & \frac{1}{C_d} & 0 & 0 \\ 0 & 0 & \frac{1}{L_s} & 0 \\ 0 & 0 & 0 & \frac{1}{L_c} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ v_3 \\ v_7 \end{bmatrix} \ . \tag{4.17}
$$



(a)



(b)

Figure 4.5. Complete large-signal tunnel-diode oscillator (a) Equivalent circuit, and (b) its System-graph.

Writing the circuit and the cut-set equations, similar to (4.12) and putting them in the matrix form:

$$\begin{bmatrix} i_1 \\ i_2 \\ v_3 \\ v_7 \end{bmatrix} = \begin{bmatrix} -G_c & 0 & -1 & 1 \\ 0 & -i_D(\,) & 1 & 1 \\ 1 & -1 & -r_s & 0 \\ -1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v \\ v_D \\ i_3 \\ i_7 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ v_8 \end{bmatrix} . \qquad (4.18)$$

Substituting Equation (4.18) into (4.17), multiplying the matrices, and substituting v for v_1 and V_{BB} for v_8, the resulting set of equations is:

$$\frac{d}{dt}\begin{bmatrix} v \\ v_D \\ i_3 \\ i_7 \end{bmatrix} = \begin{bmatrix} -\frac{G_c}{C_c} & 0 & \frac{1}{C_c} & \frac{1}{C_c} \\ 0 & -\frac{i_D(\,)}{C_d} & \frac{1}{C_d} & 0 \\ \frac{1}{L_s} & -\frac{1}{L_s} & -\frac{r_s}{L_s} & 0 \\ -\frac{1}{L_c} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v \\ v_D \\ i_3 \\ i_7 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ \frac{V_{BB}}{L_c} \end{bmatrix} . \qquad (4.19)$$

This is the system model for the oscillator shown in Figure 4.5a. Once again a suitable initial condition for $v_D(t)$ must be specified.

If the dc bias point for the intrinsic tunnel diode is V_D, $(V_P < V_D < V_V)$, then $V_{BB} = V_D + I_D(V_D)r_s$. For $v_D(t = 0) = V_D$ the solution of (4.16) will be trivial since

then $\dot{v}(0) = \dot{v}_D(0) = \dot{i}_3(0)$ and $\dot{i}_7(0) \equiv 0$. Accordingly suitable initial conditions are:

$$\text{at} \qquad t = 0 \ , \quad v_D(0) = V_B (\neq V_D) \ .$$

$$\text{Then,} \qquad i_3(0) = i_D(V_B) \ , \tag{4.20}$$

$$v(0) = V_B + i_D(V_B) r_s \ ,$$

$$i_7(0) = i_D(V_B) + [V_B + i_D(V_B) r_s] G_c \ .$$

In both sets of equations the expression for $i_D(v_D)$ can be any one of those given in (4.10). For any reasonably accurate expression for $i_D(v_D)$, the set of equations given in (4.15) or (4.19) cannot easily be solved by analytical methods. They were solved on a digital computer. At the same time solving them numerically on a digital computer allows freedom to:

(a) choose any form for $i_D(v_D)$ without making the solution any more complicated;

(b) study the effect of the junction capacitance, C_d, as a voltage dependent element, $C_d = C_d(v_D)$.

4.5 Numerical Solution of the System-Model

The system models developed in (4.15) and (4.19) for the large-signal tunnel-diode oscillator circuits of Figures 4.4 and 4.5 respectively, were solved on a CDC 3600 digital computer using Fortran IV language.

The load-circuit parameters are G_c and C_c. For studying large-signal analysis, the starting point,

$v_D(t = 0)$, is chosen to be the peak point voltage, V_P. This choice permits steady-state solutions which cannot be obtained by small perturbation of a circuit which is ac small-signal stable. $V_d(t = 0) = V_P$ is equivalent to the shock excitation of the circuit.

The set of first-order differential equations can be solved by either the Runge-Kutta method or by the Adam-Moulton method with the Runge-Kutta starter [23,33]. The computer program used for this is an expansion of the method suggested by Hildebrand [23] for a system of two first-order differential equations. The Adam-Moulton method is referred to as one of the closed types of predictor-corrector formulas. A Fortran subroutine, RKAMSUB [24], based on this was used to solve Equations (4.15) and (4.19). This subroutine integrates the set of equations for the specified time-step, ΔT, using fourth-order Runge-Kutta method.

The time-step size, ΔT, with which RKAMSUB integrates the system of differential equations, should be small enough to yield a reasonably accurate solution and at the same time large enough to yield the solution in a reasonably short time. With the expected operating frequency, f_o, the expected time period will be $T = 1/f_o$. So $\Delta T \approx T/100$ should be sufficient, considering the nonlinearity involved.

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The system model of the circuit of Figure 4.4 (or Figure 4.5) is solved starting at time t = 0 with the initial conditions on $v_D(t)$, $v(t)$ and $i_3(t)$ given by (4.16), (or (4.20)). As mentioned before

$$v_D(t = 0) = V_P \ .$$

The set of equations (4.15), (or (4.19)) is integrated numerically until $v_D(t)$ corresponds to the steady-state operation of the circuit. To ascertain when steady-state is reached, $v_D(t)$ is Fourier-analyzed [34] and its fundamental, second and third harmonic components are obtained as:

$$v_D(t) = V_{D_O} + \sum_{p=1}^{P=3} \left[V_{d_{sp}} \sin\left(\frac{2\pi p}{T'} t\right) + V_{d_{cp}} \cos\left(\frac{2\pi p}{T'} t\right) \right],$$

$$= V_{D_O} + \sum_{p=1}^{P=3} V_{D_p} e^{j\left(\frac{2\pi p}{T'} t - \phi_p\right)}, \qquad (4.21)$$

where,

T' = the new time-period of oscillation

$V_{d_{sp}}$ = p th harmonic sine component

$V_{d_{cp}}$ = p th harmonic cosine component

$V_{D_p} = \frac{1}{2}\sqrt{V_{d_{sp}}^2 + V_{d_{cp}}^2}$ = p th harmonic component

and $\phi_p = \arctan\left(-V_{d_{cp}}/V_{d_{sp}}\right)$. If the harmonic

components V_{D1}, V_{D2} and V_{D3} of two consecutive periods of $v_D(t)$ differ by less than 1, 2 and 4 per cent respectively, it is assumed that the solution corresponds to the steady-state operation.

The resultant period of oscillation, T', not being equal to the assumed period of oscillation, $T = 1/f_o$, is not a surprising result. The period, T, is based on small-signal analysis, while the actual period of oscillation, T', is the result of a large-signal analysis of the non-linear problem. It should be noticed that T' is always greater than T. In other words, the resultant fundamental frequency of oscillation, $f_o' = 1/T'$, is less than the assumed operating frequency, f_o.

Using the solution corresponding to the steady-state operation of the circuit, $i_D(t) = i_D(v_D(t))$ is evaluated point by point for one period of $v_D(t)$. Then $v(t)$ and $i_D(t)$ are Fourier analyzed in the form:

$$i_D(t) = I_{d_o} + \sum_{p=1}^{P=3} \left[I_{d_{sp}} \sin\left(\frac{2\pi p}{T} t\right) + I_{d_{cp}} \cos\left(\frac{2\pi p}{T} t\right) \right], \quad (4.22)$$

and

$$v(t) = V_o + \sum_{p=1}^{P=3} \left[V_{sp} \sin\left(\frac{2\pi p}{T} t\right) + V_{cp} \cos\left(\frac{2\pi p}{T} t\right) \right]. \quad (4.23)$$

The average power generated by the intrinsic tunnel diode at the $p^{\underline{th}}$ harmonic is:

$$P_{D_p} = 0.5\left(V_{d_{sp}} I_{d_{sp}} + V_{d_{cp}} I_{d_{cp}}\right) . \quad (4.24)$$

The average power delivered to the load conductance, G_c, at the fundamental frequency, f_o, will be

$$P_{G_{c1}} = 0.5 \left(V_{s1}^2 + V_{c1}^2 \right) G_c \ , \tag{4.25a}$$

and at the $p^{\underline{th}}$ harmonic

$$P_{G_{cp}} = 0.5 \left(V_{sp}^2 + V_{cp}^2 \right) G_c \ . \tag{4.25b}$$

The logic diagram of a typical computer program based on the aforesaid procedure is given in Figure 4.6.

4.6 Examples

For a given tunnel diode, the procedure stated in Section 4.5 is repeated for different dc operating points between $(V_P + V_V)/2$ and V_V. For each operating point, sets of load circuit elements (G_c, C_c), are obtained for values of $k = k_{max}$, (Δk), $0.8k_{min}$ where $\Delta k = \frac{k_{max} - k_{min}}{10}$ (see Section 3.4). The circuit elements (G_c, C_c) evaluated for the parameter $k < k_{min}$ indicate small-signal stable circuits. As shown in the output curves to follow, the maximum power is actually obtained when circuit elements correspond to $k < k_{min}$. For each set of (G_c, C_c), the oscillator circuit of Figure 4.3 is solved as described in Section 4.5. From the results, a plot is obtained for the power, $P_{G_{c1}}$ delivered to the load vs. the load conductance, G_c.

This procedure is followed for two tunnel diodes--one a narrow valley germanium tunnel diode and the other

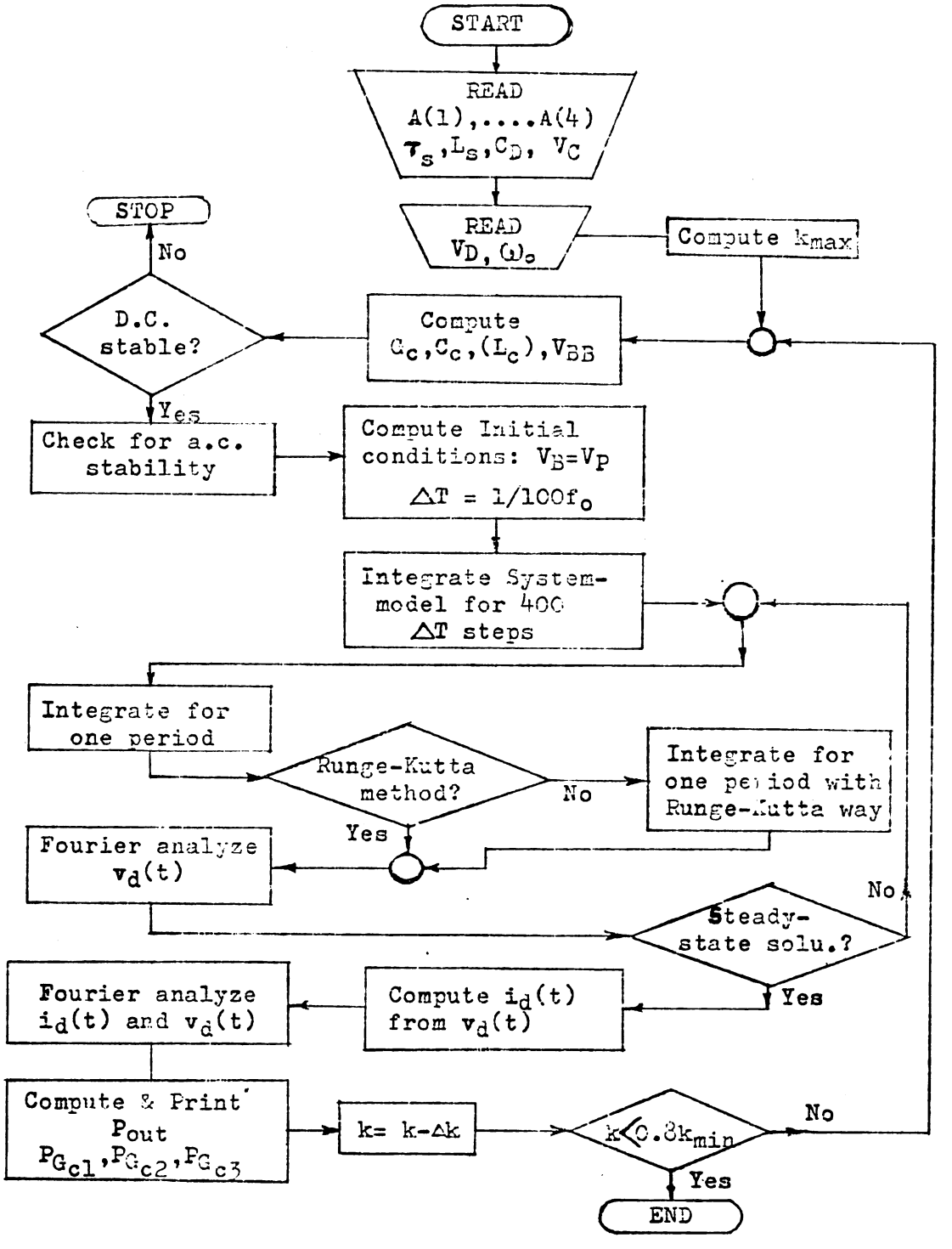


Fig. 4.6. Logic Diagram of the Computer Program for Analyzing Tunnel Diode Oscillator Circuit

a flat valley gallium-arsenide tunnel diode. The pertinent specifications for these two diodes are listed in Table 4.1.

The parameters A, a, B and b in the specifications are the same as described in Appendix A for approximating the static current-voltage characteristic of the intrinsic tunnel diode. The current-voltage plots for both diodes are shown in Figure 4.7.

1. GaAs Tunnel Diode ZJ61-22, Calculations

From the specifications:

valley point voltage, V_V = 670 mV

peak point voltage, V_P = 120 mV.

The dc operating points attempted were

V_D = 0.44, 0.46, 0.4β, 0.50, and 0.52 volts.

For $V_D = 0.44$, $\omega_S = 2.27 \times 10^9$, $\omega_R = 4.80 \times 10^9$.

For $V_D = 0.52$, $\omega_S = 2.49 \times 10^9$, $\omega_R = 3.65 \times 10^9$.

So select $\omega_o = 2.77 \times 10^9$ radians/sec.

The load-circuit elements, G_c,C_c, calculated for the bias point, V_D = 0.48 volts, and for several values of $k < k_{max}$ are plotted in Figure 4.8. The set (G_{c_m},C_{c_m}) corresponding to $k = k_{min}$ is marked by a star (*).

The complete oscillator circuit of Figure 4.3 is solved as described in Section 4.5 for V_D = 0.43, (0.02), 0.53 and for different circuit parameters, G_c,C_c. In this

TABLE 4.1

Tunnel-Diode Specifications

Parameter		ZJ61-22 GaAs	1N2941 Ge
r_s	ohms	2	1
L_s	nh	6	5
C_d	pf	25	20
A		0.51554	0.44
a		8.6207	16.8
B		1.6114×10^{-5}	5.4×10^{-7}
b		6.4694	15.4
V_P	mV	120	60
I_P	mA	22.01	9.64
V_V	mV	670	400
I_V	mA	2.01	0.47
g_{max}	mhos	-0.0693	-0.0595
at V_d	volt	0.23	0.12

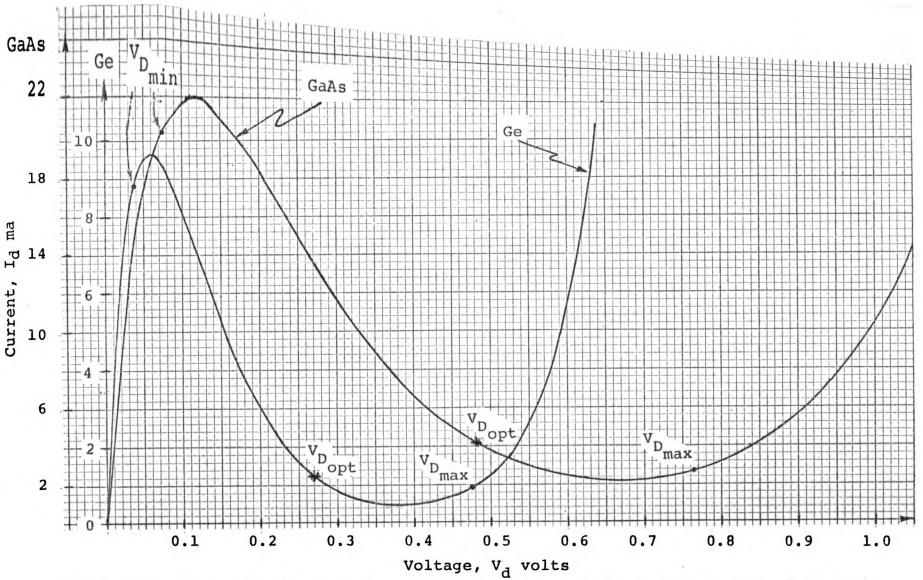


Figure 4.7 Current-voltage characteristics of GaAs and Ge intrinsic tunnel diodes.

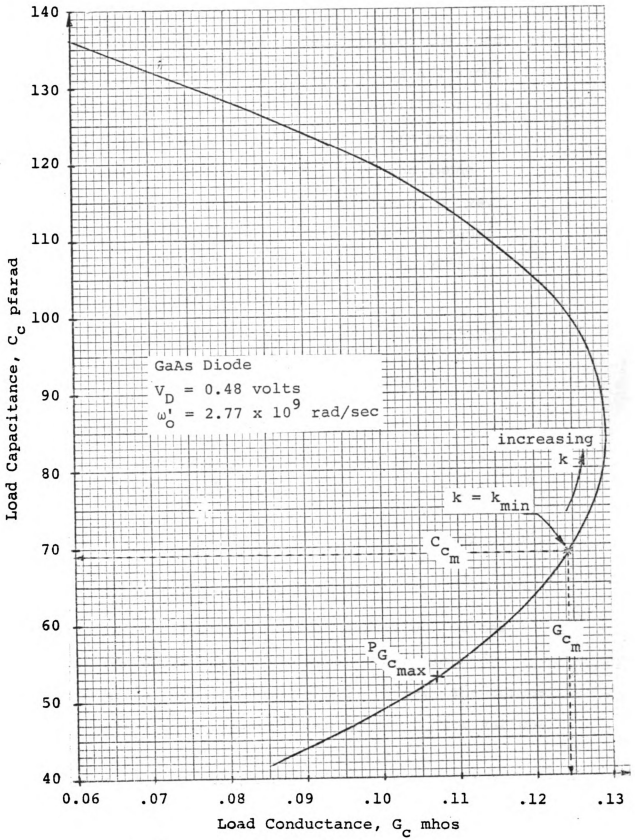


Figure 4.8 Variation of load capacitance and conductance for constant operating frequency.

case maximum fundamental power is delivered to the load conductance, G_c, when V_D = 0.48 volts. Table 4.2 shows the complete set of calculations for the oscillator circuit when V_D = 0.48 volts. Similar tables are prepared for each dc operating point. The plots of the fundamental power delivered to the load conductance, G_c vs. G_c for various dc operating points are shown in Figure 4.9. Figure 4.10 shows a similar plot for the second and third harmonic power delivered to G_c.

2. Germanium Tunnel Diode, 1N2941, Calculations

From the specifications:

V_P = 0.06 volts, V_V = 0.40 volts.

The dc operating points attempted were

V_D = 0.25, 0.26, 0.27, 0.28 and 0.29 volts.

For V_D = 0.25, $\omega_S = 2.99 \times 10^9$, and $\omega_R = 7.12 \times 10^9$.

For V_D = 0.29, $\omega_S = 3.10 \times 10^9$, and $\omega_R = 5.52 \times 10^9$.

So select $\omega_o = 3.25 \times 10^9$ radians/sec.

Calculations similar to those described for the gallium-arsenide diode were performed. The optimum dc operating point is found to be V_D = 0.27 volts. The curves of the fundamental power delivered to G_c vs. G_c for various dc operating points are shown in Figure 4.11.

The results of the maximum power delivered to load conductance, G_c, for the two diodes are summarized in Table 4.3.

TABLE 4.2

Large-Signal Computer Results of Oscillator Circuits of Figure 4.4
(GaAs Diode)
V_D = 0.48 volts, $\omega_o = 2.77 \times 10^9$ rad/sec, $C_D = C_D(V_V)$ pf

V_{BB} Volts	G_c mhos	C_c pfarad	Resultant ω_o' rad/sec	Power Generated (at ω_o') by Diode mW	Power to G_c			Small-Signal Re(Y) / $\lvert -g_D \rvert$	
					Fundamental mW	Second Harmonic μW	Third Harmonic μW		
0.55	0.06972	132.4	2.67×10^9	1.33	0.276	0.276	0.027	0.527	
0.53	0.10268	118.2	2.70 "	1.50	0.469	0.055	0.022	0.612	
0.525	0.11248	111.7	" "	1.57	0.546	0.008	36.0	0.651	
0.5246	0.11926	105.8	" "	1.62	0.614	0.1	0.05	0.687	
0.5224^-	0.127	95.3	" "	1.71	0.73	0.133	0.079	0.727	
0.522^{--}	0.12935	86.8	" "	1.77	0.824	0.155	0.103	0.822	
0.522^-	0.129	80.0	" "	1.82	0.901	0.167	0.121	0.884	
0.522^+	0.1272	74	" "	1.83	0.972	0.05	0.07	0.943	
0.523	0.1245	69	2.73×10^9	1.854	1.026	0.043	0.066	1.00	ac small-signal unstable
0.524	0.1213	65	" "	1.88	1.067	0.203	0.018	1.055	
0.525^+	0.118	61.4	" "	1.884	1.099	0.25	0.0165	1.108	
0.526^-	0.1145	58.3	" "	1.878	1.122	0.30	0.014	1.16	
0.527^+	0.1111	55.7	" "	1.86	1.137	0.366	0.01	1.211	
0.528^+	0.1078	53.4	2.70×10^9	1.83	1.1375	0.268	0.10	1.261	
0.530^-	0.1045	51.3	" "	1.793	1.1318	0.312	0.08	1.311	ac small-signal stable
0.531	0.1014	49.5	" "	1.73	1.11	0.338	0.055	1.36	
0.532	0.0984	47.8	" "	1.624	1.063	0.36	0.018	1.408	
0.5335	0.0955	46.3	" "	1.35	0.906	0.485	0.007	1.456	
0.5348	0.0928	45	No steady-state solution.						

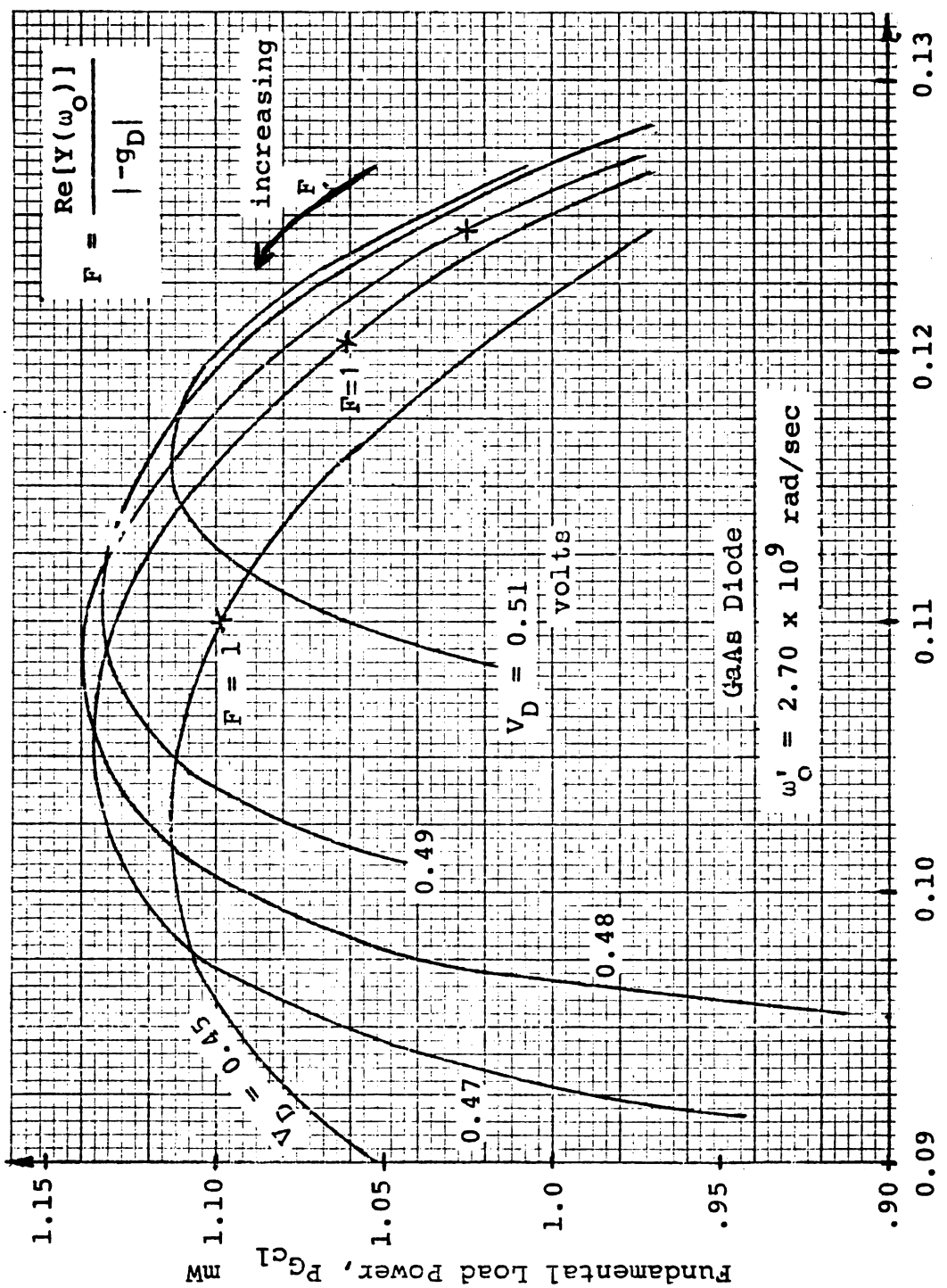


Figure 4.9 Fundamental load power vs. load conductance for different diode biases.

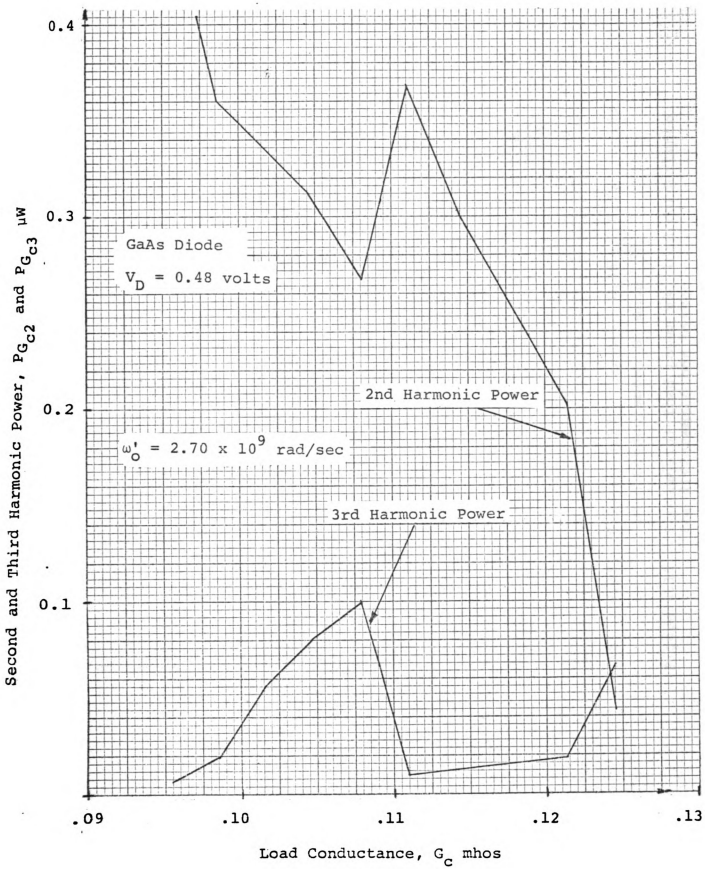


Figure 4.10 Second and third harmonic load power vs. load conductance.

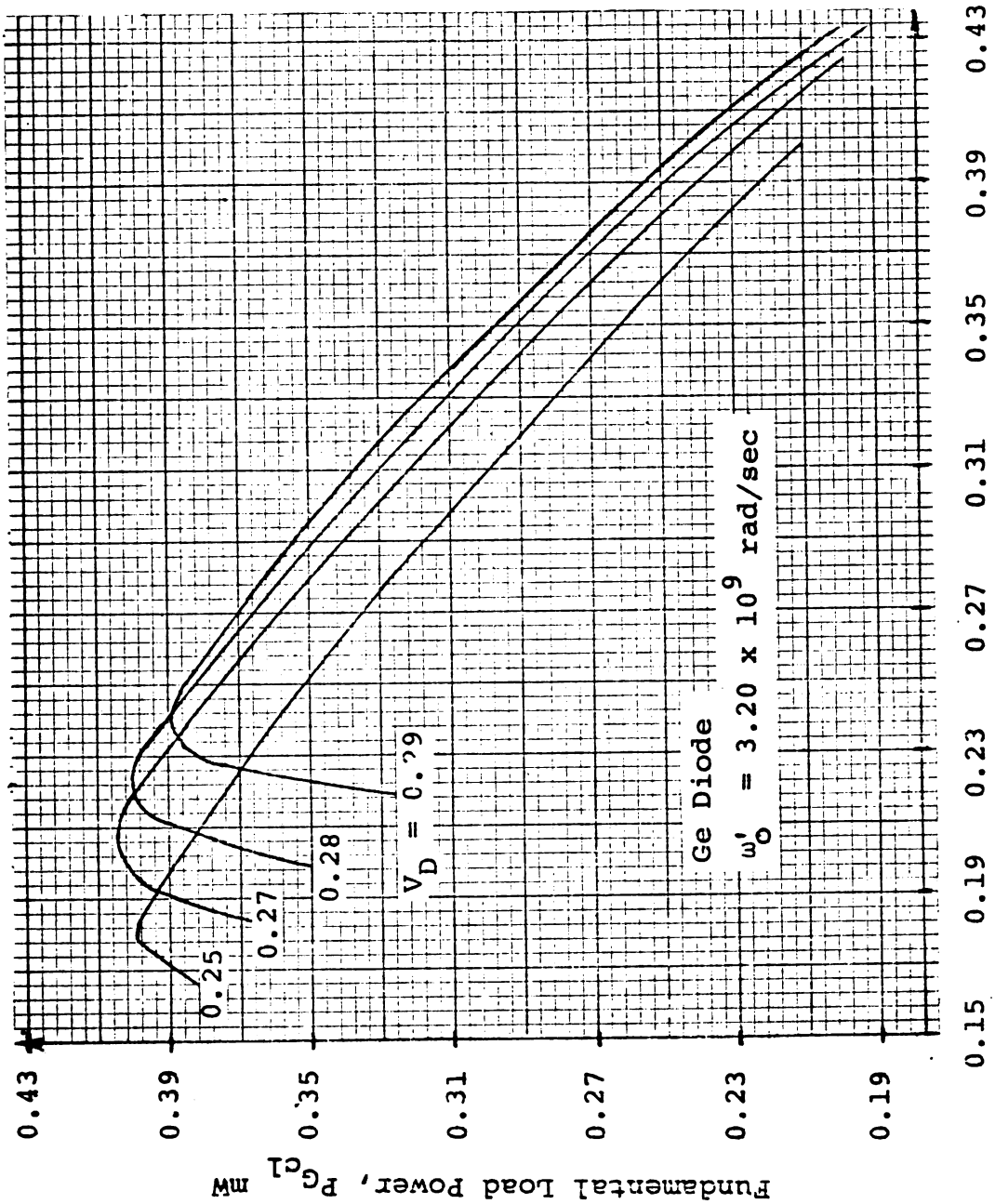


Figure 4.11 Fundamental load power vs. load conductance for different diode biases.

TABLE 4.3

Values for an Optimum Circuit and Related Performance Data

Parameter	Tunnel Diode		Units
	GaAs	Ge	
G_c	0.1078	0.20	mhos
C_c	53.35	40.9	pfarad
V_{BB}	0.5284	0.2778	volts
ω_o designed	2.77×10^9	3.25×10^9	rad/sec
ω_o' resultant	2.70×10^9	3.2057×10^9	rad/sec
P_{out} by diode	1.8328	0.518	mW
P_{Gc1} Fundamental	1.1375	0.402	mW
P_{Gc2} 2nd Harm.	0.27	0.354	μW
P_{Gc3} 3rd Harm.	0.10	0.001	μW
$\frac{Re[Y(\omega_o)]}{\lvert -g_D \rvert}$	1.261	1.284	
$\frac{V_V - V_{opt}}{V_V - V_P}$	0.345	0.382	
$V_{D_{max}}$	0.7680	0.479	volts
$V_{D_{min}}$	0.0726	0.037	volts

As mentioned earlier it should be noted that the operating angular frequency, ω_o', is slightly less than designed ω_o for both diodes. According to (3.13b),

$$F = \frac{\text{Re } [Y(\omega_o)]}{|-g_D|} < 1 ,$$

is required for the oscillations to grow. For both diodes this ratio is much greater than 1. So for these cases, $v_D(t = 0)$ value close to V_D will result in decaying oscillations such that $v_D(t \to \infty) = V_D$. By choosing $v_D(t = 0) = V_P$ = the peak voltage, the diodes are perturbed sufficiently that sustained large-signal oscillations are obtained.

4.7 Effects of Varying Circuit Parameters

(a) Oscillator Circuit with G-L-C Load Circuit

The equivalent $G_c - L_{c_{equ.}} - C_{c_{equ.}}$ circuit of the $G_c - C_c$ load circuit considered in the preceding section is shown in Figure 4.5. The circuit elements $C_{c_{equ.}} = nC_c$ and $L_{c_{equ.}} = 1/[(n-1)\omega_o^2 C_c]$, $n > 2$ are computed to keep the operating frequency constant. The above calculations were repeated for n = 3. In general it is observed that the average fundamental power delivered to the load conductance, G_c, is increased by about 10 per cent. But at the same time, the operating angular frequency of oscillation, ω_o', decreases significantly. Table 4.4 summarizes the calculations which are similar to those for Table 4.2 but for the

TABLE 4.4

Large-Signal Computer Results of Oscillator Circuits of Figure 4.5
(GaAs Diode)

V_D = 0.42 volts, $\omega_o = 2.77 \times 10^9$ rad/sec, $C_D = C_d(V_V)$ pfarad, V_{BB} = 0.49 volts

Load Circuit			Resultant	P_{out} From	Power to Load G_c		
G_c mho	C_c pfarad	L_c nh	ω_o' rad/sec	Diode mW	Fundamental mW	2nd Harmonic µW	3rd Harmonic µW
0.06972	396.3	0.492	2.043×10^9	1.46	0.717	0.076	0.003
0.11248	335.1	0.583	2.043 "	1.76	1.08	0.038	0.002
0.12684	285.9	0.684	2.043 "	1.84	1.209	0.494	0.009
0.12946	249.2	0.784	2.027 "	1.87	1.257	0.911	0.006
0.12293	200.6	0.974	1.979 "	1.88	1.297	2.42	0.012
0.1162	179.3	1.09	1.963 "	1.87	1.30	2.70	0.013
0.10856	161.6	1.2	1.93 "	1.86	1.29	3.63	0.078
0.09802	142.8	1.37	1.904 "	1.83	1.26	4.49	0.065
0.08474	124.4	1.57	1.86 "	1.78	1.24	5.61	0.175

equivalent circuit of Figure 4.4. The tunnel diode under consideration is ZJ61-22 and the operating point is V_D = 0.48 volts. The conclusions with regard to an increase in fundamental power and a decrease in the resultant operating frequency, are evident when the data of Tables 4.2 and 4.4 are compared.

(b) Oscillator Circuit with Junction Capacitance as a Junction-Voltage Dependent Element.

The oscillator circuit considered in Section 4.6 is solved again, but this time the junction capacitance, C_D, it considered to be a junction-voltage dependent element:

$$C_d \propto (V_c - v_D)^{-1/2} \quad \text{for} \quad v_D < V_V ,$$

and $$C_d = C_d(V_V) \quad \text{for} \quad v_D \geq V_V ,$$

where V_c = contact potential.

The specified value of C_d is used for $v_D = V_V$:

$$C_d(v_D) = \frac{C_d(V_V)\sqrt{V_c - V_V}}{\sqrt{V_c - v_D}} . \qquad (4.26)$$

The calculations show that the average fundamental power delivered to G_c when the junction capacitance is considered a voltage-dependent element, $C_d = C_d(v_D)$, is always higher than the same power delivered to G_c when the junction

capacitance is considered voltage-independent, viz., $C_d = C_d(V_D)$. Figure 4.12 shows the graphs of the power output for the two cases for the GaAs tunnel diode and the dc operating point equal to 0.48 volts.

(c) Effect of Varying Operating Frequency

As the operating frequency approaches the resistive cut-off frequency, ω_R, the G_c element value decreases sharply. Soon the value of G_c decreases enough to violate dc stability condition (3.24) and we get

$$(G_c + \frac{1}{r_s}) < |-g_D| \cdot$$

When a circuit with component values causing dc instability was simulated on the computer, oscillation could not be sustained.

For the circuits satisfying dc stability (3.24) the power delivered to load G_c decreased rapidly as the operating frequency was increased.

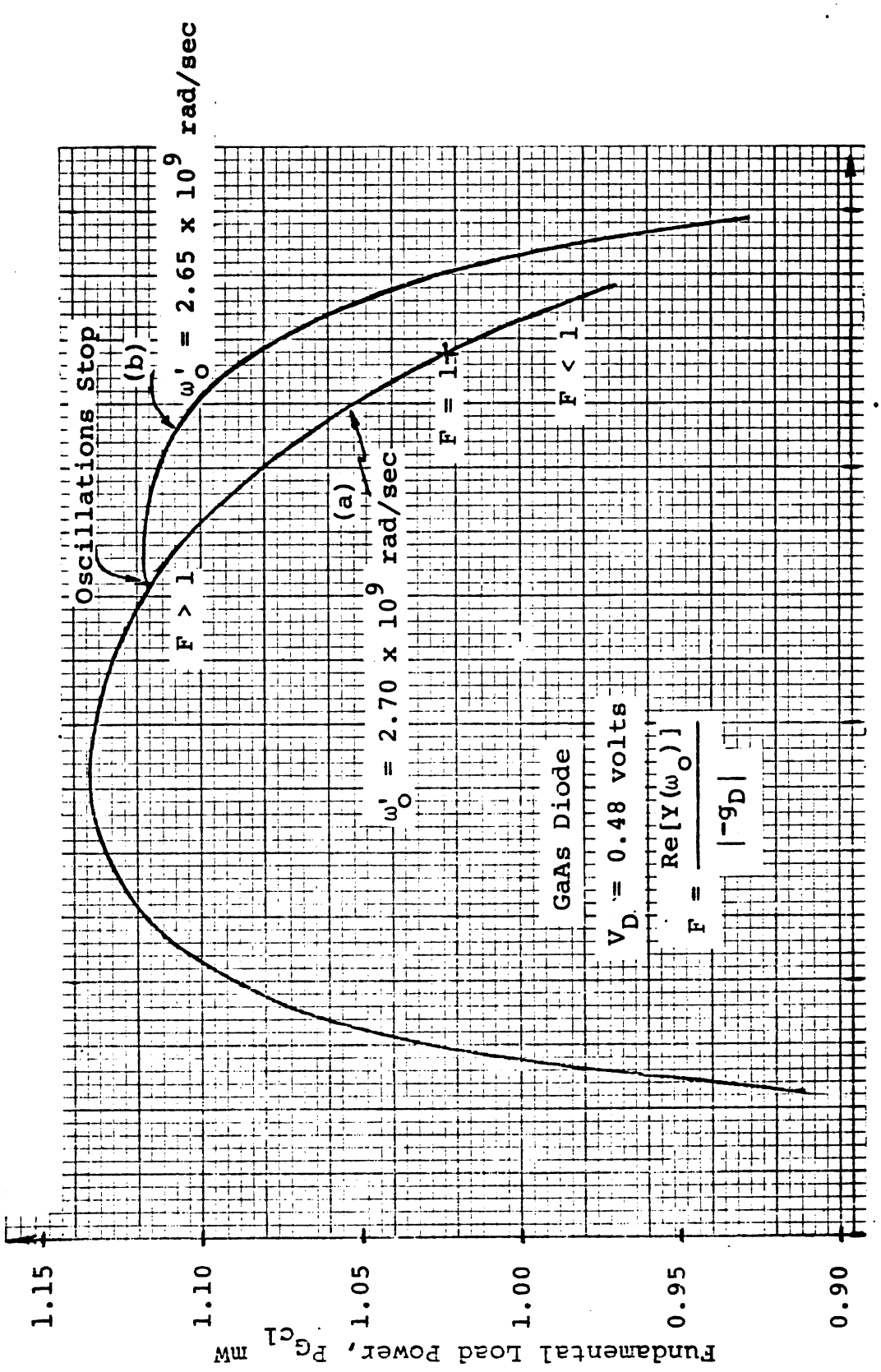


Figure 4.12 Fundamental load power vs. load conductance (a) junction capacitance constant, (b) junction capacitance voltage dependent.

CHAPTER 5

HYBRID APPROACH FOR MAXIMIZING LOAD POWER

5.1 Introduction

The intrinsic tunnel diode is the device element which due to its dynamic ~~negative~~-resistance property converts dc power into signal ac power. Hence, an attractive approach to maximize the load power is to determine the optimum voltage $v_D(t)$ at the intrinsic-diode terminals that will produce maximum fundamental power, P_1, where

$$P_1 = \frac{1}{T}\int_0^T v_{D1}(t)\,i_{D1}(t)\,dt \ , \qquad (5.1)$$

and $v_{D1}(t)$ and $i_{D1}(t)$ are the fundamental frequency components of $v_D(t)$ and $i_D(t)$, respectively. Next a circuit, with the diode elements r_s, L_s and C_D included, that will sustain $v_D(t)$ at the intrinsic-diode terminals must be synthesized. The determination of the optimum voltage $v_D(t)$ cannot be carried out analytically by conventional variational calculus techniques due to the highly nonlinear nature of the intrinsic diode. Rather, extensive computer calculations were used. With the optimum $v_D(t)$ determined a suitable circuit can be designed following

usual circuit synthesis procedure. This approach is called a hybrid approach.

5.2 Criterion for the Maximum Fundamental Power from the Intrinsic Diode

The circuit designed must be such that current-voltage matching exists at the intrinsic-diode terminals, A_1-B (Figure 5.1). The A_1-B terminal admittance of the circuit is determined by the harmonic components of $v_D(t)$ and the resulting $i_D(t)$.

To determine optimum components of $v_D(t)$, consider the Fourier analysis of $v_D(t)$:

$$v_D(t) = V_{do} + \sum_{k=1}^{N_V} \left[V_{d_{sk}} \sin\left(\frac{2\pi}{T} t\right) + V_{d_{ck}} \cos\left(\frac{2\pi}{T} t\right) \right], \tag{5.2}$$

where $V_{d_{sk}}$ and $V_{d_{dk}}$ are $k^{\underline{th}}$ harmonic sine and cosine components, respectively. Consider 360 equally spaced values per period of $v_D(t)$. Performing point-by-point calculations 360 equally spaced values per period of $i_D(t) = i_D(v_D(t))$ can be obtained using one of the expressions from those given in (4.10). The Fourier analysis of $i_D(t)$ is:

$$i_D(t) = I_{do} + \sum_{k=1}^{N_I} \left[I_{d_{sk}} \sin\left(\frac{2\pi}{T} t\right) + I_{d_{ck}} \cos\left(\frac{2\pi}{T} t\right) \right]. \tag{5.3}$$

From this, the $k^{\underline{th}}$ harmonic component of the power produced at the intrinsic tunnel diode is:

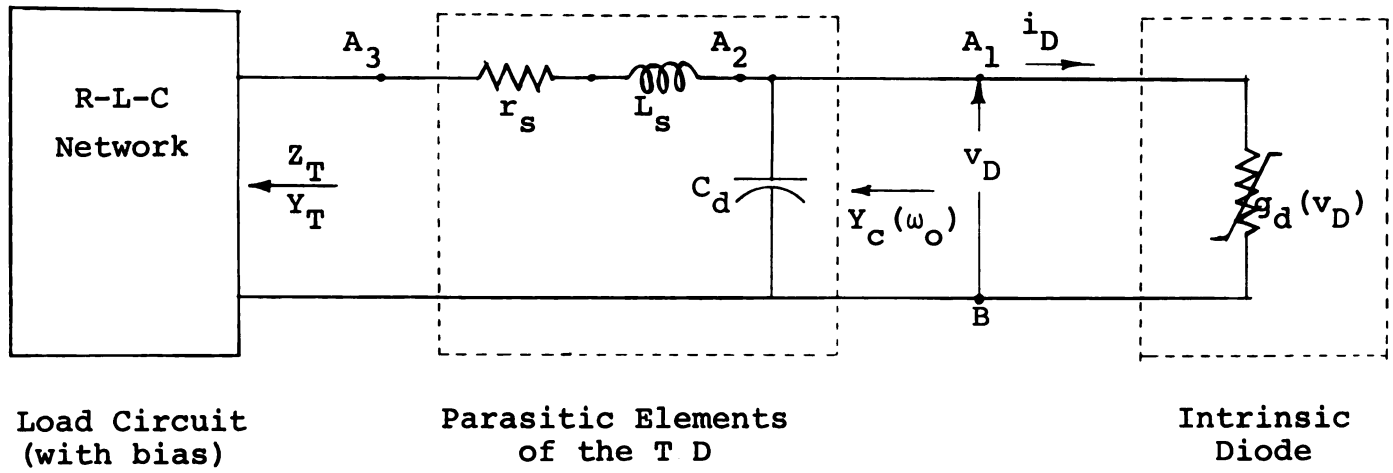


Figure 5.1. Intrinsic tunnel diode and the circuit for the maximum power.

$$P_{dk} = 0.5\left(V_{d_{sk}} I_{d_{sk}} + V_{d_{ck}} I_{d_{ck}}\right) \quad . \tag{5.4}$$

P_{dl} is to be maximized with respect to the (2k + 1) harmonic components of $v_D(t)$, V_{do}, $V_{d_{sk}}$, $V_{d_{ck}}$; k = 1,2,...N_V. It should be noted that P_{dl} will be a negative quantity as corresponding to positive power being delivered to the load.

5.3 Circuit Design for the Maximum Power from the Intrinsic Diode

For the passive-circuit to the left of terminals, A_1-B, (Figure 5.1), the voltage and the current are $v_D(t)$ and $-i_D(t)$, respectively. For current-voltage matching at the common terminals, A_1-B, the circuit admittance at the fundamental frequency, ω_o, should be

$$Y_c(\omega_o) = \frac{V_{d_{sl}} + jV_{d_{cl}}}{-I_{d_{sl}} - jI_{d_{cl}}} = Y_R(\omega_o) + jY_I(\omega_o) \quad . \tag{5.5}$$

Similarly at the $k^{\underline{th}}$ harmonic, the circuit admittance should be:

$$Y_c(k\omega_o) = \frac{V_{d_{sk}} + jV_{d_{ck}}}{-I_{d_{sk}} - jI_{d_{ck}}} \quad . \tag{5.6}$$

These equations provide admittance requirements for the circuit design after the operating frequency, ω_o, is selected.

Consider the case where only fundamental frequency components are assumed. Following the analysis as indicated above, the required admittance at the A_1-B terminals is

$$Y_C(\omega_o) = Y_R(\omega_o) + jY_I(\omega_o) \ . \tag{5.7}$$

At the A_2-B terminals the admittance required is

$$Y_R(\omega_o) + j(Y_I(\omega_o) - \omega_o C_D) \ . \tag{5.8}$$

Then,

$$Z(\omega_o) = \frac{Y_R(\omega_o) - j\left(Y_I(\omega_o) - \omega_o C_D\right)}{\left(Y_R(\omega_o)\right)^2 + \left(Y_I(\omega_o) - \omega_o C_D\right)^2} \ ,$$

$$= Re[Z(\omega_o)] + jIm[Z(\omega_o)] \ , \tag{5.9}$$

is the impedance required at the A_2-B terminals. Similarly at terminals, A_3-B

$$Z_T(\omega_o) = [Re[Z(\omega_o)] - r_s] + j[Im[Z(\omega_o)] - \omega_o L_s]$$

$$= Re[Z_T(\omega_o)] + jIm[Z_T(\omega_o)] \tag{5.10}$$

is required. When $\omega_o = \omega_{max}$, then $Re[Z_T(\omega_o)] = 0$ as then all the power produced by the intrinsic tunnel diode is dissipated in the series resistance, r_s. When the operating angular frequency ω_o, is equal to ω_S, the reactive component of $Z_T(\omega_o)$, is equal to zero as corresponding to the definition of ω_S. For $\omega_o > \omega_S$, $Im[Z_T(\omega_o)]$ is negative

corresponding to a capacitive load circuit. For $\omega_o < \omega_s$, $\mathrm{Im}[Z_T(\omega_o)]$ is positive corresponding to an inductive load-circuit requirement.

To determine $\omega_{max} = \omega_m$,

$$\mathrm{Re}[Z_T(\omega_m)] = \frac{Y_R(\omega_m)}{[Y_R(\omega_m)]^2 + [Y_I(\omega_m) - \omega_m C_D]^2} - r_s = 0 \ .$$

Then

$$\frac{Y_R(\omega_m)}{r_s} - Y_R^2(\omega_m) = Y_I^2(\omega_m) - 2\omega_m C_D Y_I(\omega_m) + \omega_m^2 C_D^2 \ , \tag{5.11}$$

or

$$\omega_m^2 C_D^2 - 2\omega_m Y_I(\omega_m) C_D + \left(Y_I^2(\omega_m) + Y_R^2(\omega_m) - \frac{Y_R(\omega_m)}{r_s} \right) = 0 \ . \tag{5.12}$$

Hence

$$\omega_m = \frac{Y_I(\omega_m)}{C_D} \pm \left(\sqrt{\frac{Y_R(\omega_m)}{r_s} - Y_R^2(\omega_m)} \right) \frac{1}{C_D} \ . \tag{5.13}$$

This expression for ω_{max} is identical to the expression in (3.10b) for the resistive cut-off frequency when

$$Y_I(\omega_m) = 0 \quad \text{and} \quad Y_R(\omega_m) = g_D \ .$$

Similarly, the solution of $\mathrm{Im}[Z_T(\omega_m)] = 0$ (for obtaining an expression for ω_s) results in the following cubic equation:

$$- \frac{Y_I(\omega_s)}{L_s} + \frac{\omega_s C_D}{L_s} = \omega_s Y_R^2(\omega_s) + \omega_s Y_I^2(\omega_s) - 2\omega^2 Y_I(\omega_s) C_D + \omega_s^3 C_D^2 \ . \tag{5.14}$$

When, as is usually the case $Y_I(\omega_S) << Y_R(\omega_S)$, the equation yields

$$\omega_S = \sqrt{\frac{1}{L_s C_D} - \frac{Y_R^2(\omega_S)}{C_D^2}} \quad . \tag{5.15}$$

This is identical to the equation (3.11b) for the self-resonant frequency if $Y_R(\omega_S) = g_D$.

Thus, when $\omega_o < \omega_{max}$, the load circuit of Figure 5.1 should be designed such that the admittance to the left of terminals A_1-B is $Y_c(\omega_o)$. Upon completion of the design the dc stability requirements, according to (3.13), must also be met for proper functioning of the oscillator circuit.

In Appendix C it is shown that any two frequency admittance specifications, such as:

$$Y_T(\omega_o) = Y_{R1}(\omega_o) + jY_{I1}(\omega_o) \tag{5.16a}$$

$$Y_T(2\omega_o) = Y_{R2}(2\omega_o) + jY_{I2}(2\omega_o) \tag{5.16b}$$

can always be realized if $Y_{R1}(\omega_o)$ and $Y_{R2}(\omega_o)$ are positive.

5.4 Examples

The procedure mentioned in Sections 5.2 and 5.3 was carried out for the two diodes analyzed in Section 4.6.

The most difficult part of the hybrid approach is that of obtaining the optimum harmonic components of $v_D(t)$, viz., V_{do}, V_{s1}, V_{c1}, V_{s2}, V_{c2} (as for $N_v = 2$). Several attempts were made to find these analytically. Finally a

computer program, namely, GREAT--Generalized Random Extremum Analysis Technique--, (Appendix D) was used for numerical evaluation. This program finds the minimum value of a function of several variables. The initial value of each variable is selected at random from within the specified limits. Evaluating the direction cosines with respect to each variable, the variables are increased or decreased to minimize the functional value.

For a gallium-arsenide tunnel diode, considering the fundamental sine-cosine components only, the optimum bias point is found to be about 0.465 ± 0.004 volts and the corresponding maximum fundamental power, P_{max}, generated is about 1.947 mW. When second harmonic components are also introduced, the optimum bias point shifts to 0.405 ± 0.004 volts and the maximum fundamental power output increases to about 2.264 mW, a 16.3 per cent increase.

Similarly for a germanium tunnel diode, considering the fundamental sine-cosine components only, the optimum bias point of about 0.27 ± 0.004 volts is obtained, and maximum fundamental power output is about 0.530 mW. When second harmonic components are also considered, the optimum bias point of about 0.23 ± 0.004 volts and P_{max} about 0.633 mW results. Introducing third harmonic components gives optimum bias point between 0.24 and 0.28 volts and P_{max} about 0.67 mW. Inclusion of higher harmonic components results in larger output power, but computer time required

to find the optimum voltage components increases considerably. As might be expected higher harmonics produce progressively smaller changes in P_{max}. Table 5.1 gives typical starting and final values of harmonic components of diode voltage,

$$v_D(t) = V_{do} + V_{s1} \sin\omega_o t + V_{c1} \cos\omega_o t + V_{s2} \sin 2\omega_o t + V_{c2} \cos 2\omega_o t \ , \qquad (5.17)$$

and the power output from a gallium-arsenide tunnel diode, ZJ61-22.

As mentioned in Section 5.3, the diode current

$$i_D(t) = I_{do} + I_{d_{s1}} \sin\omega_o t + I_{d_{c1}} \cos\omega_o t + I_{d_{s2}} \sin 2\omega_o t + I_{d_{c2}} \cos 2\omega_o t \ , \qquad (5.18)$$

is calculated from $v_D(t)$. The harmonic components of $i_D(t)$ for the two cases listed in Table 5.1 are given in Table 5.2.

When only fundamental components are considered, the circuit admittance required for the gallium-arsenide diode is according to Equation (5.5):

$$Y_c(\omega_o) = 2.4387 \times 10^{-2} - j\ 5.6915 \times 10^{-10} \ .$$

Then, $\omega_{max} = 4.3079 \times 10^{9}$, and $\omega_S \approx 2.3 \times 10^{-9}$ radians/sec.

With $g_d(V_{do}) = -2.65 \times 10^{-2}$ mhos, $r_s = 2$ ohms and $\omega_o > \omega_S$,

TABLE 5.1

$v_D(t)$ Harmonic Components when Fundamental Power is Maximum (GaAs Diode)

Component		Initial Value (Monte-Carlo Method)	Final Value
1st case: Fundamental Component only			
V_{do}	Volts	0.41695	0.46425
V_{s1}	"	0.06931	0.31349
V_{c1}	"	-0.23125	-0.24794
P_{out}	mW	-1.2624	-1.9480
2nd case: Fundamental and Second Harmonic Components			
V_{do}	Volts	0.46802	0.41067
V_{s1}	"	0.12911	0.43022
V_{c1}	"	-0.04920	-0.04584
V_{s2}	"	0.123	-0.02570
V_{c2}	"	-0.06229	-0.11747
P_{out}	mW	-1.3033	-2.26293

TABLE 5.2

$i_D(t)$ Harmonic Components when Fundamental Power is Maximum (GaAs Diode)

Component		1st Case	2nd Case
I_{do}	ma	9.7076	12.953
$I_{d_{s1}}$	ma	-7.6451	-10.401
$I_{d_{c1}}$	ma	6.0465	1.108
$I_{d_{s2}}$	ma	-3.7962	- 0.229
$I_{d_{c2}}$	ma	-0.8987	- 1.052

the dc stability condition requires the load conductance G_c to be greater than 0.025 mhos.

The circuit elements--G_c,C_c--for $\omega_o = 2.4 \times 10^9$, ($10^8$), 4.2×10^9 radians/sec are calculated according to Equations (5.7) through (5.10). These are plotted in Figure 5.2. The results from the exact analysis (discussed in Chapter 4) for different ω_o's are tabulated in Table 5.3. The fundamental power generated by the gallium-arsenide diode is 1.948 mW in each case. In the table ω_o, G_c and C_c are from Figure 5.2. ω_o' is the resultant (fundamental) frequency of oscillation; P_{out} is the power generated by the diode; and P_{G_c} is the power delivered to the load, G_c.

It is evident that the power output from the diode, P_{out}, and the power delivered to the load, G_c, at the fundamental frequency reduces rapidly when the higher fundamental frequencies are considered.

The optimum circuit performance obtained in Chapter 4 is also listed in Table 5.3. V_D for this case was 0.48 volts. A comparison of this with the data of set no. 2, Table 5.3 shows that the fundamental $P_{G_{c1}}$ and P_{out} obtained in Chapter 4 are higher: $P_{G_{c1}}$ by 7 per cent and the power transfer efficiency, $P_{G_{c1}}/P_{out}$ by 5 percent.

However, the small-signal analysis for the circuit elements (obtained by hybrid approach) listed in Table 5.3

TABLE 5.3

Circuit Values and Related Performance Data
for Hybrid Synthesis
(GaAs Diode)

Set No.	ω_o rad/sec	Load Circuit G_c m-mhos	Load Circuit C_c pfarad	ω_o' Resultant rad/sec	$-P_{out}$ from Diode mW	$P_{G_{cl}}$ mW
1	2.50×10^9	262.5	36.88	2.44×10^9	1.892	1.207
2	2.75 "	130.0	65.8	2.708 "	1.844	1.056
3	2.90 "	70.53	57.4	2.85 "	1.670	0.88
4	3.10 "	32.98	43.85	Non-oscillatory circuits		
5	3.20 "	23.15	38.44			
Optimum Circuit of Chapter 4, $V_D = 0.48$ volts						
	2.77×10^9	107.8	53.4	2.702×10^9	1.83	1.1375

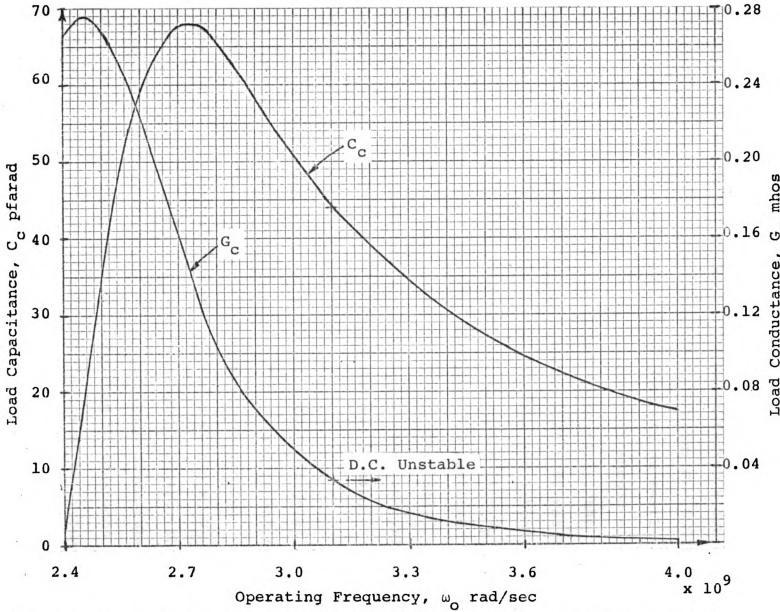


Figure 5.2. Load capacitance and load conductance vs. operating frequency for maximum fundamental power from GaAs intrinsic tunnel diode.

indicates that the factor $F = Re[Y_c(\omega_o]/|-g_D|$ is equal to 0.926--less than 1, unlike the value of factor F for the optimum case obtained in Chapter 4. Factor F = 0.926 indicates that the circuits are very close to ac small-signal stability. Consequently, the circuits should always be shock excited. When analyzed numerically, the oscillations could not be generated when $v_D(t = 0)$ was selected close to $V_{do} = 0.46$ volts. The results listed in Table 5.3 are obtained by considering $v_D(t = 0) = V_P = 0.12$ volts. The last two sets in Table 5.3 resulted in non-oscillatory circuits when analyzed numerically. This is due to dc instability. But small-signal analysis indicates dc instability for data of set no. 5 only, while set no. 4 is very close to it.

In the second case of Table 5.1, the voltage at the intrinsic-diode terminals, $v_D(t)$, up to and including second harmonic components, is considered. Table 5.1 lists one set of several optimum voltage components, V_{do}, V_{s1}, V_{c1}, V_{s2}, V_{c2} producing same fundamental power. The circuit admittance, matching at the intrinsic-diode terminals, is calculated for this set according to Equations (5.5) and (5.6). The resulting admittances at the fundamental and the second harmonics are:

$$Y_c(\omega_o) = 2.418 \times 10^{-2} + j\ 1.135 \times 10^{-6}$$

and

$$Y_c(2\omega_o) = -8.955 \times 10^{-3} - j\ 7.353 \times 10^{-6}\ .$$

Note that $Re[Y_c(2\omega_o)]$ is negative. Several different optimized sets were attempted. But for each case $Re[Y_c(2\omega_o)]$ was found to be negative. Similar results were obtained for the germanium tunnel diode. Consequently, in the case of these two tunnel diodes a circuit could not be designed that could provide the required current-voltage matching for the second harmonic. This need not be true for tunnel diodes in general. Designing a circuit with $Y_c(\omega_o)$ only, and neglecting the mismatch at the second harmonic, resulted in greatly reduced power output when analyzed numerically as outlined in Chapter 4.

CHAPTER 6

CONCLUSIONS

In this thesis a computer algorithm has been developed for evaluating the fundamental power delivered to the load of a tunnel-diode oscillator circuit. This algorithm has been successfully used to determine changes in fundamental power with changes in circuit parameters. Specifically it was found that simple operating circuits could be optimized to produce maximum fundamental power. When the optimized circuit is used, tunnel-diode voltage and current are rich in harmonic content. Large-signal analyses that assume perfect sinusoidal signals are not adequate to evaluate optimum performance.

From an in-depth computer evaluation of a germanium and a gallium-arsenide tunnel-diode oscillator circuit it was found that

(1) Optimum tunnel-diode bias voltage is closer to the valley voltage than to the peak voltage.

(2) The optimum tunnel-diode bias voltage approaches closer to the valley voltage as the valley region of the diode flattens out.

(3) Fundamental power delivered to the load decreases as the operating frequency increases.

(4) The operating frequency was somewhat lower than the frequency indicated by small-signal analysis.

(5) Maximum power output was found to occur with a circuit which was small-signal stable. This mode of operation would be feasible only if provisions were made for shock exciting the circuit.

(6) Somewhat greater fundamental power can be obtained by the use of a voltage-dependent junction capacitance in comparison with circuit operation in which the junction capacitance is constant.

(7) For maximum power output the conversion efficiency was about 23.7 per cent.

(8) Contrary to some reports in the literature, at no time was it found that the circuit would oscillate at a frequency greater than the resistive cut-off frequency.

Although the findings listed above were verified for only the two diodes examined, they are believed to be generally valid. From the work completed, it is considered feasible to use the algorithm developed to design simple circuits for optimum operating conditions. At ultra-high frequencies the circuits become more complex and it is not certain whether the algorithm can be modified to include the added complexities. This area, particularly as it relates to transmission-line analysis, could be the subject of further investigation.

APPENDICES

APPENDIX A

APPROXIMATION TO TUNNEL-DIODE STATIC CURRENT-VOLTAGE CHARACTERISTIC EQUATION

A useful two-term approximation of the tunnel-diode I-V characteristic was first suggested by Ferendici and Ko [11] as

$$I_T(V_T) = A' V_T e^{-a' V_T} + B' (e^{b' V_T} - 1) \qquad (A.1)$$

where $I_T(V_T)$ is the terminal current and V_T is the terminal voltage. The I_d-V_d characteristic of the intrinsic tunnel diode at terminals a-a' (see Figure A.1), is obtained as discussed below.

The equivalent circuit of the tunnel diode is as shown in Figure A.1. For static characteristic as obtained at low frequency, the effects of series inductance, L_s, and junction capacitance, $C_d(V_d)$, can be neglected. Then

$$I_d(V_d) = I_T(V_T - V_{r_s}) \text{ where } V_{r_s} = I_T(V_T) r_s . \qquad (A.2)$$

Thus point-by-point calculations will give the characteristic of the intrinsic tunnel diode. This characteristic can similarly be approximated by

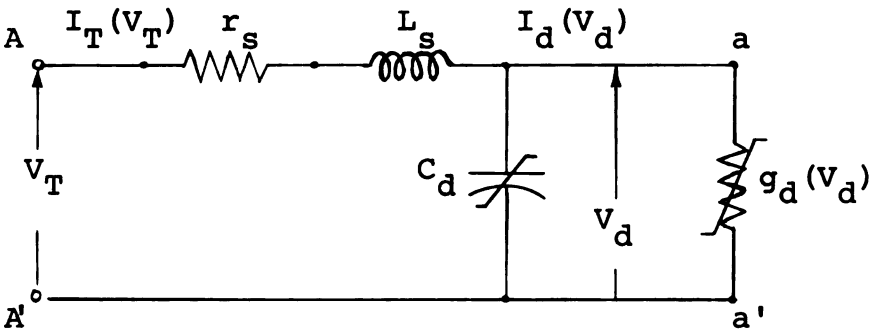


Figure A.1. Equivalent circuit of a tunnel diode

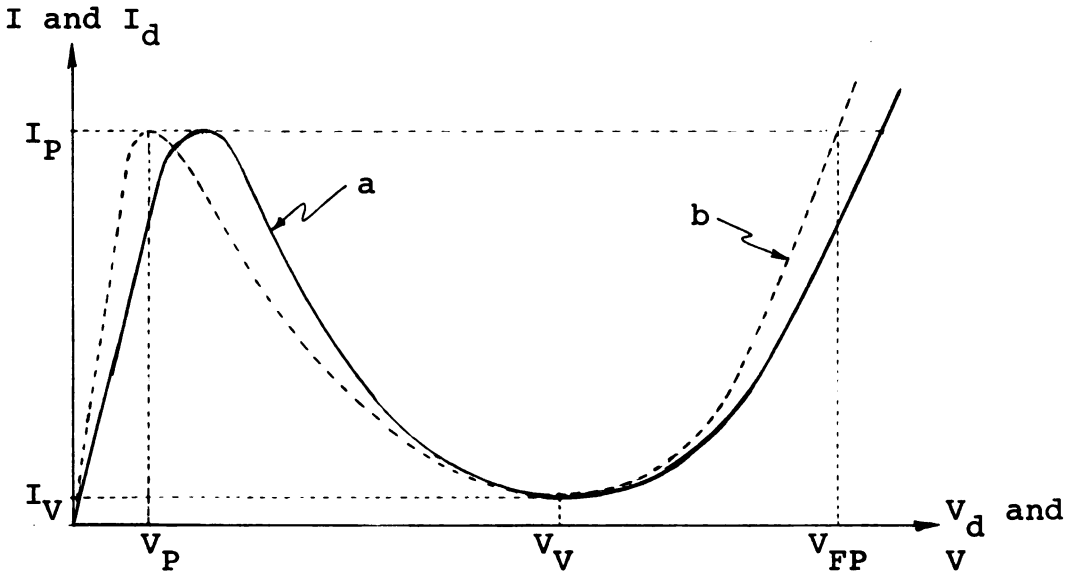


Figure A.2. Static current-voltage characteristics at
(a) Tunnel diode, terminals A-A^1
(b) Intrinsic tunnel diode, terminals a-a^1

$$I_d(V_d) = AV_d e^{-aV_d} + B(e^{bV_d} - 1) \qquad (A.3)$$

The parameters A, a, B, and b can be evaluated as follows:

Suitable pilot points are chosen according to the fit desired. Herein, a closer fit is desired in the negative-conductance region and near the valley and peak points. Suitable pilot points are:

(a) peak point, (V_P, I_P)

(b) valley point, (V_V, I_V)

(c) point of maximum negative conductance, or a point (V_C, I_C) near it, and

(d) a point between (V_V, I_V) and (V_{FP}, I_P) or (V_{FP}, I_P). The contribution of the diode-injection current (2nd term of Equation A.3) is considered negligible for $V_d < V_c$. Consider

$$g_d(V_d) = \frac{dI_d(V_d)}{dV_d} = A(1 - aV_d)e^{-aV_d} \text{ for } V_d < V_c . \qquad (A.4)$$

Using $g_d(V_P) = 0$ in (A.4) gives $a = 1/V_P$. For the point (V_C, I_C), $I_C = AV_C e^{-aV_C}$.

Knowing the coefficient a, the coefficient

$$A = \frac{I_C \exp(V_C/V_P)}{V_C} , \qquad (A.5)$$

can be determined.

At the valley point the tunneling current component (1st term of Equation A.3) is

$$I_t(V_V) = AV_V e^{-aV_V} , \tag{A.6}$$

and the diode injection current component, $I_D(V_d)$, at valley point will be

$$I_D(V_V) = I_d(V_V) - I_t(V_V) \tag{A.7}$$

Near $V = V_{FP}$, $I_t(V_{FP}) \simeq 0$, so $I_D(V_{FP}) = B(e^{bV_{FP}} - 1)$.

Consider the ratio

$$\frac{I_D(V_{FP})}{I_D(V_V)} = r = \frac{e^{bV_{FP}} - 1}{e^{bV_V} - 1} . \tag{A.8}$$

In (A.9) the only unknown is b, but due to the involved exponentials it must be solved numerically, as follows:

First guess, $b_0 = \ln(r)/(V_{FP} - V_V)$.

Since $V_V < V_{FP}$, $b < b_0$.

Consider $b_1 = 0.98b_0$, and evaluate $r_1 = \frac{e^{b_1 V_{FP}} - 1}{e^{b_1 V_V} - 1}$.

If $r_1 < r$, consider $b_2 = 0.99b_0$ and evaluate r_2; if $r_2 < r$, consider $b_3 = 0.995b_0$ and evaluate r_3. Continue the process until $r_n < r$. Then $b_{n-1} < b < b_n$. Then, try $b_{n+1} = (b_{n-1} + b_n)/2$ and calculate r_{n+1}.

Continuing this procedure find b_k giving r_k, as close to the ratio, r, as desired. Finally, knowing b, evaluate

$$B = \frac{I_D(V_{FP})}{e^{bV_{FP}} - 1} \tag{A.9}$$

Thus, parameters A, a, B and b are determined for the intrinsic tunnel-diode junction characteristic.

APPENDIX B

STABILITY OF A LINEAR ACTIVE SYSTEM

B.1 In this appendix the stability of an active linear network, N_d, connected to a passive linear network, N, as shown in Figure B.1 is considered.

Since the networks, N and N_d, are linear and their parameters are constant, the pertinent differential equations relating v(t) with i(t) and $v_D(t)$ with $i_D(t)$ will be linear with constant coefficients [25] as

$$P\left(\frac{d}{dt}\right) i(t) = Q\left(\frac{d}{dt}\right) v(t) \ , \tag{B.1}$$

$$P_d\left(\frac{d}{dt}\right) i_D(t) = Q_d\left(\frac{d}{dt}\right) v_D(t) \ , \tag{B.2}$$

where P, Q, P_d and Q_d are polynomial operators of the form:

$$a_m \frac{d^m}{dt^m} + a_{m-1} \frac{d^{m-1}}{dt^{m-1}} + \ldots + a_1 \frac{d}{dt} + a_0 \ . \tag{B.3}$$

Here m, the degree of the polynomial operator, is a fixed integer and the coefficients $a_0, a_1, \ldots, a_m$ are functions of the network elements alone. The degrees of the polynomials are not necessarily the same. When N and N_d are connected as shown in Figure B.1, $v_D(t) = v(t)$, and $i_D(t) = - i(t)$. Accordingly, (B.1) and (B.2) become:

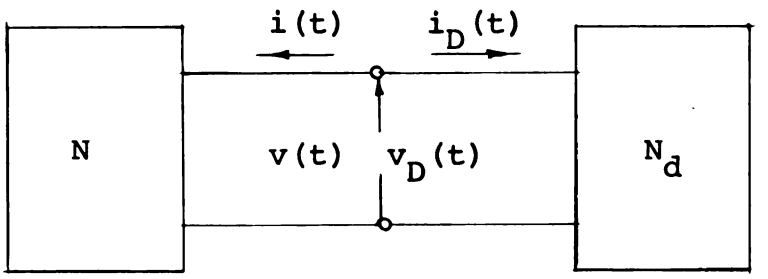


Figure B.1. A linear active network, N_d, connected to a passive linear network, N, showing terminal voltages and currents.

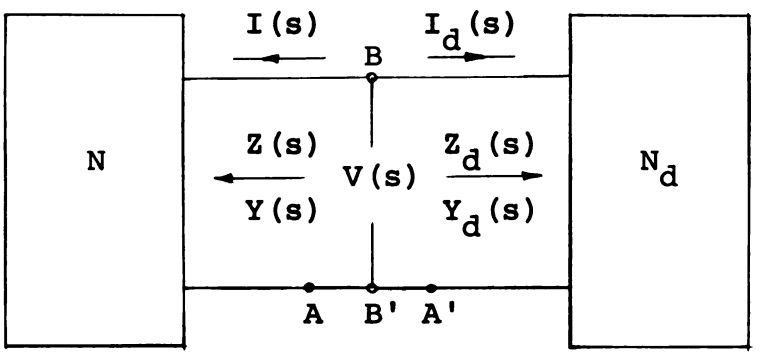


Figure B.2. System of Figure B.1 with their terminal impedances and admittances.

$$\begin{bmatrix} P\frac{d}{dt} & -Q\frac{d}{dt} \\ P_d\frac{d}{dt} & Q_d\frac{d}{dt} \end{bmatrix} \begin{bmatrix} i(t) \\ v(t) \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} . \tag{B.4}$$

Solutions of (B.4) will contain terms of the form Ae^{st} where $s = \sigma + j\omega$, a complex number [25].

$$\begin{aligned} i(t) &= I(s)e^{st} , \\ v(t) &= V(s)e^{st} , \end{aligned} \tag{B.5}$$

is a solution. However, the general solution [25] will be:

$$\begin{aligned} i(t) &= \sum_{k=1}^{m} A_k(s)\, e^{s_k t} , \\ v(t) &= \sum_{k=1}^{m} B_k(s) e^{s_k t} . \end{aligned} \tag{B.6}$$

For studying the stability of the system shown in Figure B.1 it is sufficient to substitute (B.5) into (B.4) and check whether the resulting characteristic polynomial is a Hurwitz polynomial, viz., a polynomial having all its roots with a negative real part. Substituting (B.5) into (B.4) and canceling e^{st}, the set of equations obtained is:

$$\begin{bmatrix} P(s) & -Q(s) \\ P_d(s) & Q_d(s) \end{bmatrix} \begin{bmatrix} I(s) \\ V(s) \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} . \tag{B.7}$$

The characteristic polynomial, Δs, of the set of equations (B.7) is:

$$\Delta s = P(s)\, Q_d(s) + P_d(s) Q(s) \ . \tag{B.8}$$

For system stability, $\Delta s = 0$ should not have any root with a positive real part. The natural frequencies of the system are the roots of the characteristic equation. Consider

$$\begin{aligned} \frac{\Delta(s)}{Q(s)Q_d(s)} &= \frac{P(s)}{Q(s)} + \frac{P_d(s)}{Q_d(s)} \\ &= \frac{V(s)}{I(s)} + \frac{V_d(s)}{I_d(s)} \\ &= Z(s) + Z_d(s) \\ &= Z_{Loop}(s) \ . \end{aligned} \tag{B.9}$$

Similarly,

$$\frac{\Delta(s)}{P(s)P_d(s)} = Y(s) + Y_d(s) = Y_{Node}(s) \ . \tag{B.10}$$

$Z_{Loop}(s)$ and $Y_{Node}(s)$ are the loop impedance and the node admittance respectively, for the system shown in Figure B.2. $Z(s) + Z_d(s)$ is the input impedance for terminals, A-A'; $Y(s) + Y_d(s)$ is the input admittance for terminals, B-B'.

The natural frequencies of a network can also be obtained from $Z_{Loop}(s) = 0$ and $Y_{Node}(s) = 0$. In general, the natural frequencies obtained from these will be different. If no independent voltage or current source is

connected in the network, or if $Z_{Loop}(s)$ and $Y_{Node}(s)$ are obtained by considering all the voltage sources shorted and current sources open, then the natural frequencies obtained on either the impedance basis or the admittance basis will be unique [26]. The tunnel-diode oscillator circuit analyzed in Chapters 3 and 4 can be analyzed on either basis.

The input impedance (admittance) of a stable network is positive real. A positive real function, G(s), must satisfy [27]:

$$\mathrm{Re}[G(s)] \geq 0 \text{ for } \mathrm{Re}(s) = \mathrm{Re}(\sigma + j\omega) = \sigma \geq 0 \ . \quad \text{(B.11)}$$

If the input impedance, $Z_{Loop}(s)$, (admittance, $Y_{Node}(s)$), is such that:

$$\mathrm{Re}\left[Z_{Loop}(s)\right] < 0$$

$$\mathrm{Re}\left[Y_{Node}(s)\right] < 0 \text{ for } \mathrm{Re}(s) = 0, \text{ viz., } s = j\omega \ . \quad \text{(B.12a)}$$

Then the corresponding network will be unstable and any oscillation initiated will grow in amplitude. Since the oscillations are of angular frequency, ω_0, as given by either

$$\mathrm{Im}[Z_{Loop}(s)] = 0$$

or

$$\mathrm{Im}[Y_{Node}(s)] = 0 \text{ with } s = j\omega \ . \quad \text{(B.12b)}$$

APPENDIX C

CIRCUIT SYNTHESIS BASED ON TWO-FREQUENCY ADMITTANCE SPECIFICATION

In this Appendix it will be shown that a suitable circuit can be synthesized to have a given admittance at two frequencies provided the conductances of the two admittances are positive.

Let the admittances at the two frequencies be:

$$Y(\omega_1) = Y_R(\omega_1) + jY_I(\omega_1) \ ,$$

and

$$Y(\omega_2) = Y_R(\omega_2) + jY_I(\omega_2) \ . \qquad \text{(C-1)}$$

The imaginary parts of an admittance specified at two frequencies can always be realized by a three-element Foster network. In a degenerate case, a two-element Foster network will be sufficient. This will be obvious from the following sketches:

Figure C.1: for situations where $\text{Im}[Y(\omega_1)] > 0$ and $\text{Im}[Y(\omega_2)] < 0$,

Figure C.2: for situations where $\text{Im}[Y(\omega_1)] < 0$ and $\text{Im}[Y(\omega_2)] < 0$, and $\text{Im}[Y(\omega_1)] > 0$ and $\text{Im}[Y(\omega_2)] < 0$.

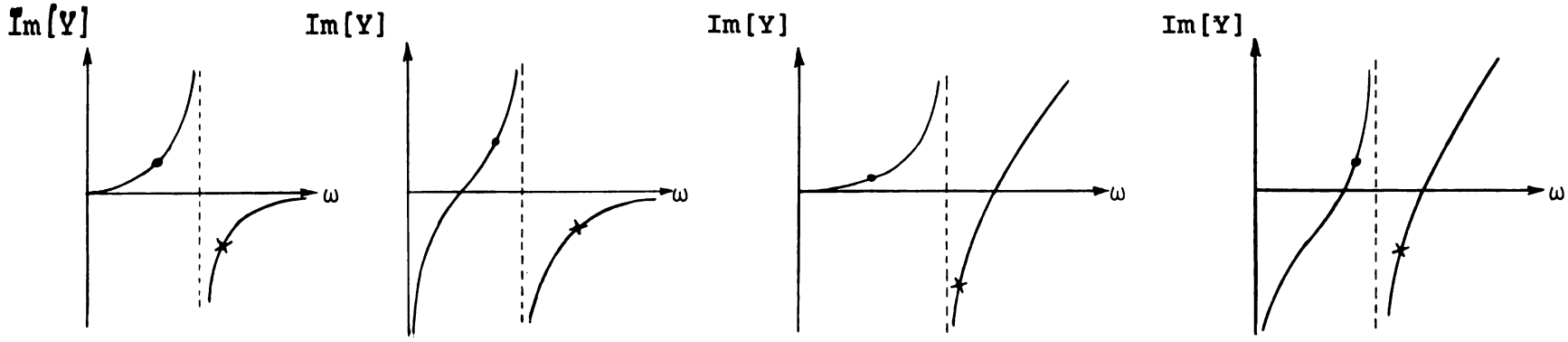


Figure C.1. Frequency characteristics for the Foster networks providing $\mathrm{Im}[Y(\omega_1)] > 0$ (•) and $\mathrm{Im}[Y(\omega_2)] < 0$ (×) , $\omega_1 < \omega_2$.

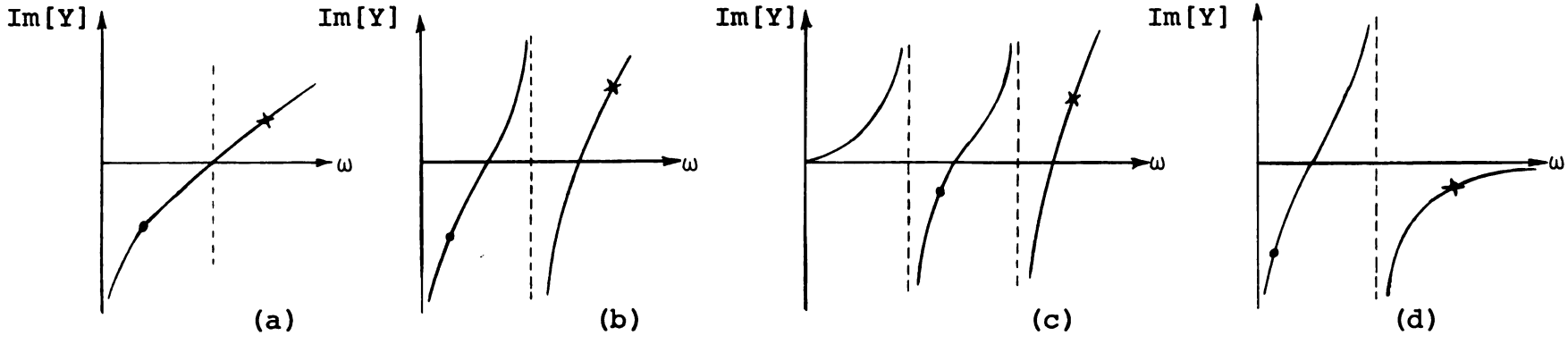


Figure C.2. Frequency characteristics of Foster networks providing
(a),(b),(c): $\mathrm{Im}[Y(\omega_1)] < 0$, $\mathrm{Im}[Y(\omega_2)] > 0$, $\omega_1 < \omega_2$
(d): $\mathrm{Im}[Y(\omega_1^1)] < 0$, $\mathrm{Im}[Y(\omega_2^2)] < 0$, $\omega_1^1 < \omega_2^2$.

Thus the form of the Foster network realizing the imaginary parts of two admittances will be:

$$\frac{ks\left(s^2 + \omega_2^2\right)}{s^2 + \omega_1^2} \quad \text{or} \quad \frac{k\left(s^2 + \omega_1^2\right)}{s\left(s^2 + \omega_2^2\right)} , \tag{C.2}$$

or in a degenerate case, like Figure C.1(a) and C.2(a):

$$\frac{ks}{s^2 + \omega_1^2} \quad \text{or} \quad \frac{k\left(s^2 + \omega_1^2\right)}{s} . \tag{C.3}$$

The real parts of the admittances must be realized first. In doing so, the imaginary parts will be altered, but they can always be realized as shown in Figures C.1 and C.2.

For realizing the real parts of the admittance either of the two general forms of networks shown in Figure C.3 should be adequate. Consider the network of Figure C.3a.

Let $G_1 = \frac{1}{R_1}$ and $R_2 = \frac{1}{G_2}$. Then

$$Y(s) = \frac{CG_1 s}{G_1 + Cs} + \frac{1}{R_2 + Ls} ,$$

$$= \frac{LCG_1 s^2 + (R_2 CG_1 + C)s + G_1}{(G_1 + Cs)(R_2 + Ls)} ,$$

$$- G_1 \left[\frac{(s^2 + 1/LC) + (R_2/L + R_1/L)s}{\left(s^2 + \frac{G_1 R_2}{LC}\right) + \left(\frac{G_1}{C} + \frac{R_2}{L}\right)s} \right] . \tag{C.4}$$

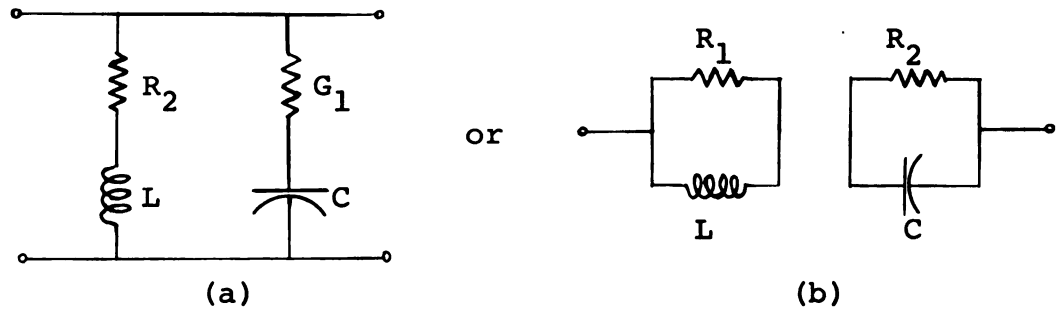


Figure C.3. Networks to realize the real parts of an admittance specified at two frequencies.

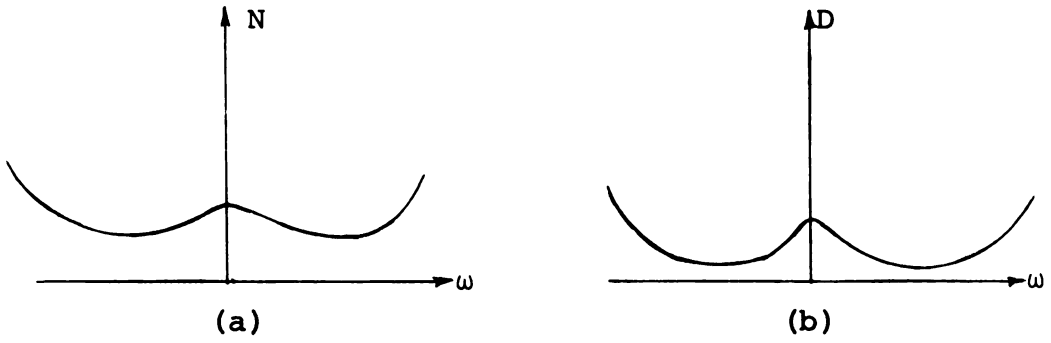


Figure C.4. Numerator and denominator of Equation (C.7).

The function defined in equation (C.4) cannot be negative on the jω axis because it is a positive real function.

Consider the quantity,

$$G_1 \left[\frac{\left(s^2 + \frac{1}{LC}\right) + \left(\frac{R_2}{L} + \frac{R_1}{L}\right)s}{\left(s^2 + \frac{G_1R_2}{LC}\right) + \left(\frac{G_1}{C} + \frac{R_2}{L}\right)s}\right]\left[\frac{\left(s^2 + \frac{1}{LC}\right) - \left(\frac{R_2}{L} + \frac{R_1}{L}\right)s}{\left(s^2 + \frac{G_1R_2}{LC}\right) - \left(\frac{G_1}{C} + \frac{R_2}{L}\right)s}\right] . \tag{C.5}$$

With the substitution of S = jω, only even-power terms in s will effect the real part of the admittance. Odd-power terms in s will effect only imaginary parts of the admittance. With odd-power terms dropped (C.5) becomes

$$G_1 \frac{\left(s^2 + \frac{1}{LC}\right)\left(s^2 + \frac{R_2G_1}{LC}\right) - \frac{1}{L}(R_1 + R_2)\left(\frac{G_1}{C} + \frac{R_2}{L}\right)s^2}{\left(s^2 + \frac{R_2G_1}{LC}\right)^2 - \left(\frac{G_1}{C} + \frac{R_2}{L}\right)^2}$$

Substituting jω for s in (C.6) and simplifying gives:

$$G_1\left[\frac{\omega^4 + \omega^2\left(R_2^2 + R_1R_2\right)/L^2 + R_2G_1/L^2C^2}{\left(-\omega^2 + R_2G_1/LC\right)^2 + \left(G_1/C + R_2/L\right)\omega^2}\right] \equiv \frac{N}{D} . \tag{C.7}$$

This real part of the desired network, (C.7), must be positive real. Also any real zeros in ω^2 must be double; there are no real zeros on the jω-axis. Thus the numerator, N, will be of the form shown in Figure C.4(a) and the

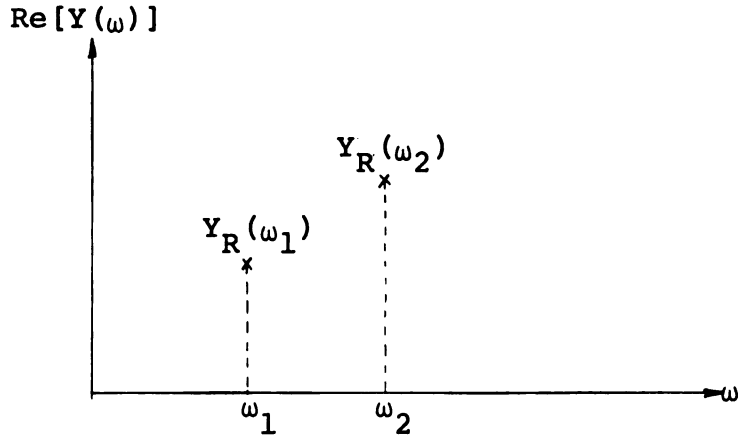


Figure C.5a. Real parts of the admittance function at the frequencies ω_1 and ω_2.

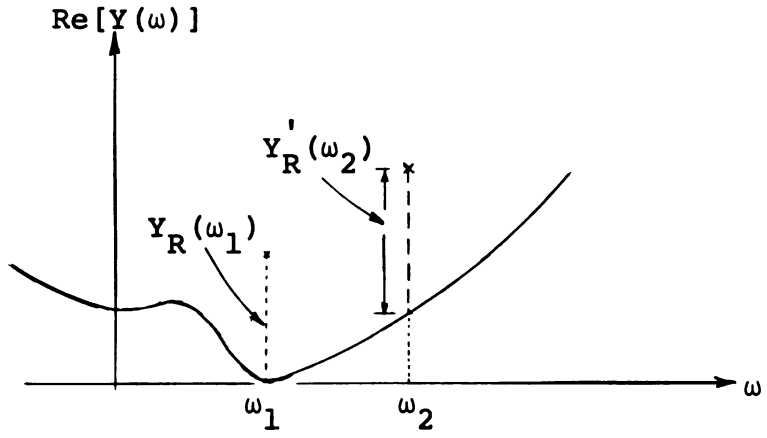


Figure C.5b. Real part of admittance function $Y_1(\omega)$.

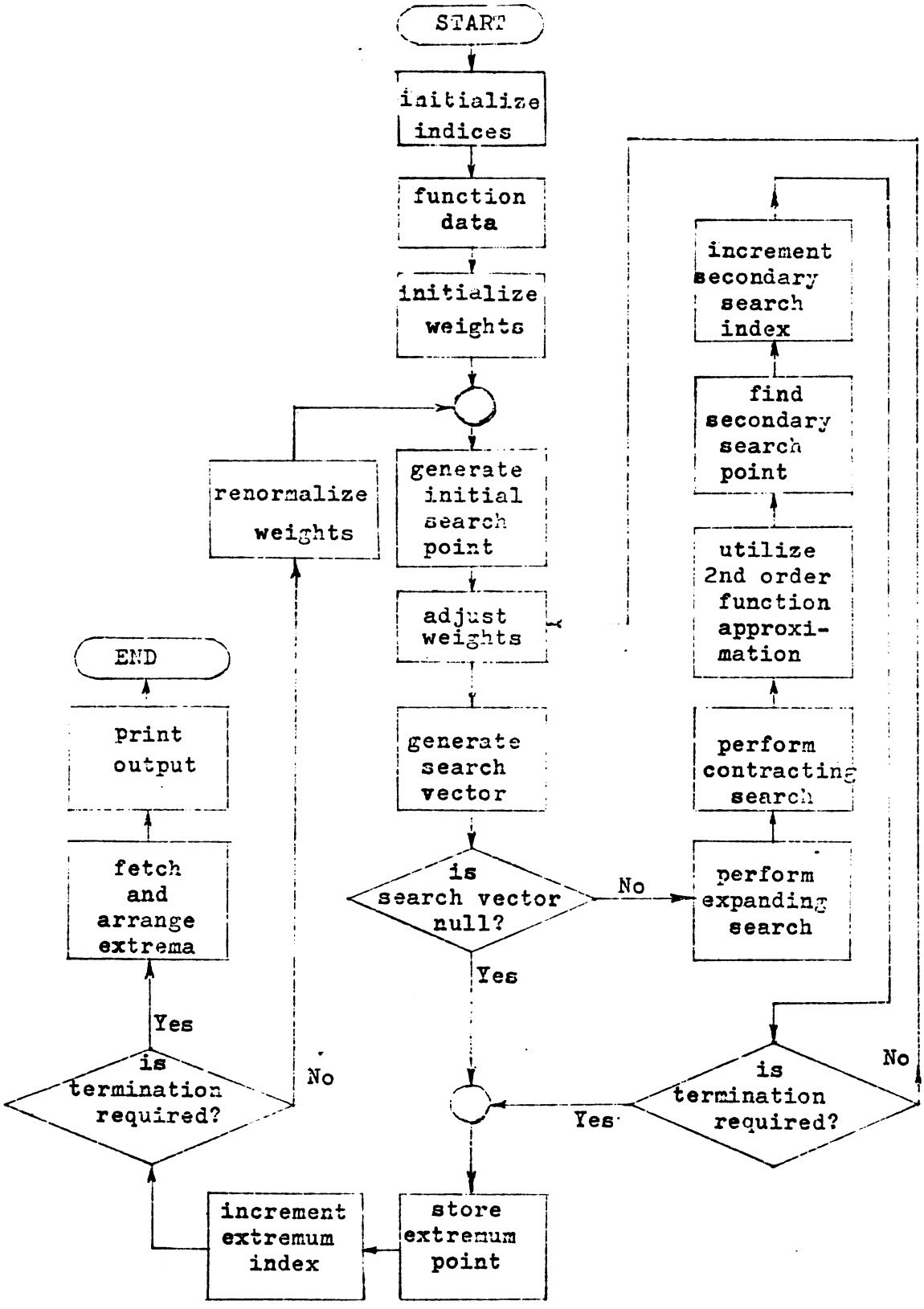
denominator, D, will be of the form shown in Figure C.4(b).

The ratio, N/D, can be almost any positive number.

Example: Let $Y_R(\omega_1) < Y_R(\omega_2)$.

Design a four element G-C, R-L network (like Figure C.3a) of terminal admittance function $Y_1(\omega)$ such that $\mathrm{Re}[Y_1(\omega_1)] = Y_R(\omega_1)$. This network will partially realize $Y_R(\omega_2)$ since $\mathrm{Re}[Y_1(\omega_2)] \neq Y_R(\omega_2)$ in general. Let $\mathrm{Re}[Y_1(\omega_2)] = Y_R'(\omega_2)$. This is shown in Figure C.5b. Now by scaling the element values, a zero is created at ω_2 by reducing $Y_R(\omega_2)$ by the amount $Y_R(\omega_2)-Y_R'(\omega_2)$. Scaling the element values will not affect the zero designed at ω_1. When this is completed, $Y_R(\omega_1)$ and $Y_R(\omega_2)$ are realized. With this result, the modified imaginary parts to be realized can be calculated and the design is completed with a properly designed Foster network.

APPENDIX D



Logic Diagram of the Computer Program
"Generalized Random Extremum Analysis Technique"
(Courtesy of Instrument Division, Lear Siegler, Inc.,
Grand Rapids, Michigan)

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