DESIGN OF HIGH SENSITIVITY ENERGY HARVESTERS FOR BODY IMPLANTABLE DEVICES AND IoT APPLICATIONS

By

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ABSTRACT

DESIGN OF HIGH SENSITIVITY ENERGY HARVESTERS FOR BODY IMPLANTABLE DEVICES AND IoT APPLICATIONS

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The advances in Internet of Things (IoT) enabled more and more devices to be connected to the clouds for effective remote control over multiple devices. Expansion in the application areas of IoT also raises the question of sustainability of massive sensor usage and their power management in terms of economic and environmental aspects. Radio frequency (RF)-powered devices attract great attention for the development of wireless sensor networks since they do not need any battery replacement or maintenance over the long run. These features of RF-powered devices eliminate the environmental and economic concerns at the same time since they make use of propagating wave energy instead of internal power sources. The primary function of RF energy harvesters is to convert the received wireless energy into direct current (DC) voltage and store it across a capacitor for further use.

This work is based on 915 MHz RF energy source where the maximum allowed effective isotropic radiated power (EIRP) is 4 W. The maximum distance at which a radio frequency identification (RFID) tag can operate is strongly dependent on the sensitivity value, which is the smallest power necessary for the desired DC output voltage of the RF energy harvester. Therefore, the focus of this work is to improve the sensitivity. Typically, multi-stage rectifiers are incorporated in modern RF energy harvesters where the threshold voltage of the rectifying elements determine the sensitivity value of the harvester.

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KEY TO ABBREVIATIONS AND SYMBOLS

AC	Alternating Current
AM	Amplitude Modulation
Balun	Balanced to Unbalanced
C	Capacitance
CC	Coupled Capacitance
CMOS	Complementary Metal Oxide Semiconductor
d	Distance [m]
DC	Direct Current
DUT	Device Under Test
EIRP	Effective Isotropic Radiated Power
EM	Electromagnetic
FM	Frequency Modulation
G_A	Antenna Directional Gain [dBi]
G_{boost}	Passive Voltage Boosting
GSG	Ground-Signal-Ground
GSSG	Ground-Signal-Signal-Ground
IC	Integrated Circuit
IoT	Internet of Things
ISM	Industrial, scientific and medical
L	Length [m]
LTE	Long Term Evolution

MIM	Metal Insulator Metal
MOS	Metal Oxide Semiconductor
N	Number of Stages
NMOS	N-Channel Metal Oxide Semiconductor Field Effect Transistor
NFET	N-Channel Field Effect Transistor
PMOS	P-Channel Metal Oxide Semiconductor Field Effect Transistor
PFET	P-Channel Field Effect Transistor
P	Power [W]
PMU	Power Management Unit
Q-factor	Quality Factor
R	Resistance [Ω]
RF	Radio Frequency
RFID	Radio Frequency Identification
t	Time [s]
UHF	Ultra-High Frequency
V	Voltage [V]
W	Width [m]
X	Reactance [Ω]
Z	Impedance [Ω]
λ	Wavelength [m]

Subscripts

ant	Antenna
av	Available
EIRP	Effective Isotropic Radiated Power
in	Input
load	Load
out	Output
rec	Rectifier
th	Threshold
th,high	Upper Threshold
th,low	Lower Threshold

1 INTRODUCTION

1.1 Background and Motivation

The advances in Internet of Things (IoT) enabled more and more devices to be connected to the clouds for effective remote control over multiple devices. Expansion in the application areas of IoT also raises the question of sustainability of massive sensor usage and their power management in terms of economic and environmental aspects. Radio frequency (RF)-powered devices attract great attention for the development of wireless sensor networks since they do not need any battery replacement or maintenance over the long run. These features of RF-powered devices eliminate the environmental and economic concerns at the same time since they make use of propagating wave energy instead of internal power sources. The primary function of RF energy harvesters is to convert the received wireless energy into direct current (DC) voltage and store it across a capacitor for further use.

In general, wireless powering is possible through two different approaches: wireless energy harvesting and wireless power transfer. The former one makes use of available ambient RF signals that are there for other purposes. On the other hand, the latter assumes the presence of dedicated sources which are only for transmitting power. One challenge that inspired wireless powering is the continuously increasing number of sensors which require solutions to limit the overall power consumption. The scaling of complementary metal oxide semiconductor (CMOS) technology enables ultra-low voltage and ultra-low power designs. Especially for IoT nodes, the integrated circuit (IC) solutions include on-chip power management and digital signal processing units. Having a digital signal processing block enables the reduction in the overall data through some techniques such as classification, compression etc. which effectively reduces the total power

consumption. The sensor nodes need to operate at very low power levels and an additional block must be designed to manage the overall power scheme of the sensor. It is essential that each block is optimized for the least possible power consumption. Also, IC solutions need to be well analyzed to utilize the energy harvesting by considering the performance parameters such as sensitivity, the smallest power necessary for the desired output voltage, and efficiency, the ratio of delivered power to the available.

Today, RF energy harvesters are used in wide range of application areas such as radio frequency identification (RFID) systems, inventory management, smart buildings, and biomedical health monitoring. Most commonly, the industrial, scientific and medical (ISM) band at 902-928 MHz is used for RF energy harvesting although there are numerous studies in literature that exploit different frequency bands such as 2.45 GHz or 5.8 GHz [1]. Besides the ISM bands, some studies [2] have used 500-700 MHz band since the radiation level is significant due to wireless digital-TV broadcast. The selection of the operating frequency is highly related with the power density of the available ambient signals. In 902 – 928 MHz band, a 4 W effective isotropic radiated power (EIRP) is allowed by regulation.

This work is based on 915 MHz RF energy harvester where the maximum allowed EIRP is 4 W. The maximum distance at which an RFID tag can operate is strongly dependent on the sensitivity value, which is the smallest power necessary for the desired output DC voltage of the RF energy harvester. Therefore, the focus of this work is to improve the sensitivity. Typically, multi-stage rectifiers are incorporated in modern RF energy harvesters, where the threshold voltage of the rectifying elements determine the sensitivity value of the harvester. Such design and trade-off studies are performed as part of this work.

1.2 Overview of RF Energy Harvesters

State of the art energy harvesters are generally composed of a receiving antenna, a full wave rectifier, a power management unit (PMU) and a load. The co-design of antenna, rectifier and power management unit allows further optimization of each block to achieve a high sensitivity. Figure 1-1 illustrates the main building blocks of an RF energy harvester.

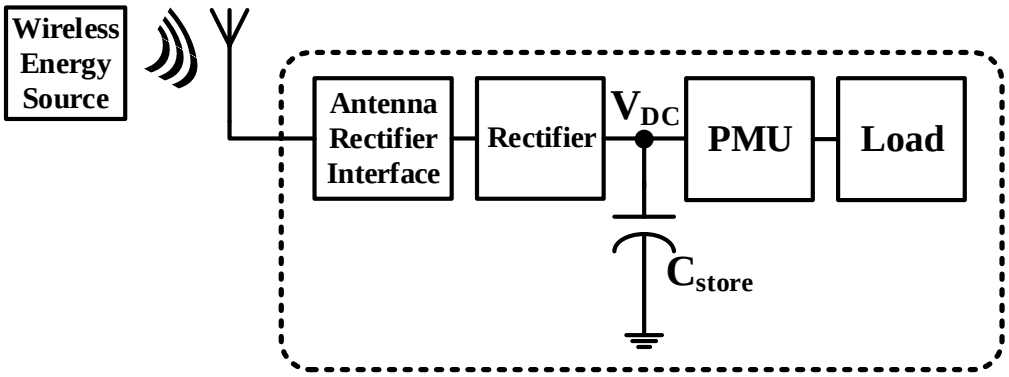

Figure 1-1. Energy Harvester Building Blocks

The available power for the impedance matched antenna in the far field is given in [3] as follows.

$$P_{av} = P_{EIRP} G_A \left(\frac{\lambda}{4\pi d}\right)^2 \quad 1\text{-}1$$

P_{EIRP} is the effective isotropic radiated power, G_A is the receiving antenna directional gain, λ is the wavelength and d is the distance to the radiating source. According to above equation, the available power decreases with the square of the distance from the radiating source, whereas the covered area by the RF source increases at the same proportion.

The energy harvester receiving antenna captures the propagating RF energy and provides the rectifier with a certain amount of alternating current (AC) signal. The amplitude of the AC voltage that is developed across the input terminals of the rectifier is heavily dependent on the

antenna-rectifier interface. The rectifier, then, converts the AC signal into the DC voltage and stores it across the storage capacitor whose size is mostly determined based on the specification for the charging and discharging times. According to the output of the rectifier, the power management unit decides whether the current will be supplied to the load or not. The load of the energy harvester can be a transmitter that can be turned on and off through the output of the power management unit. There are also studies that report a resistor load for demonstration purposes. Design of RF energy harvesters requires the co-optimization of building blocks.

1.3 Design Tasks

The primary aim of this study is to design high-performance energy harvester tags that have excellent sensitivity and high efficiency values. Additionally, it is also targeted that the energy harvesters are tolerant to changes in environment. That is especially important for biomedical applications. For instance, RF powered body implanted devices are located in the human body, which is inhomogeneous and has significantly different electrical characteristics than air. The medium for the waves to propagate now differs from the conventional medium of air as the human body has different layers such as bones, muscles or fat. Therefore, the design must account for the changes in the environment so that a robust operation can be maintained under all conditions.

1.3.1 Sensitivity

Sensitivity is defined as the minimum amount of power required for a desired amount of DC output voltage and a load current of the energy harvester. Due to effects like refraction, deflection, absorption etc. the propagating waves experience some attenuation. This attenuation is called the path loss which varies with respect to the frequency of waves, the distance between the transmitter and receiver, and the properties of the medium. Specifically, for the sensor networks, where a large distance operation may be desired, it is crucial that the energy harvester has a high sensitivity

value, implying that lower power levels are enough for proper harvesting process, so that it can operate at larger distances.

1.3.2 Efficiency

There are multiple definitions of efficiency found in the literature. This work defines the RF-DC power conversion efficiency as the ratio of the delivered power to the load (P_{load}) to the power available at the receiving antenna (P_{av}). This relation is given in [3] as follows.

$$PCE = \frac{P_{load}}{P_{incident} - P_{reflected}} = \frac{P_{load}}{P_{av}} = \frac{V_{out}^2}{P_{av}R_{load}} \quad 1\text{-}2$$

There are occasions that the design can be optimized towards a better sensitivity or towards a better efficiency. The decision depends on the application that directly defines the amount of power that the energy harvester is required to deliver to the subsequent stage, determining the efficiency or sensitivity. Similarly, based on the available power, distance between the energy harvester and the power source, or the properties of the medium in which the waves propagate set the sensitivity requirement of the application. The design parameters that play roles on compromises between sensitivity and efficiency will be analyzed in section 3.2.

1.3.3 Tolerance to Environment Changes

A receiving antenna and a rectifier are the two important building blocks of a conventional energy harvester. The receiving antenna and the rectifier are usually designed and optimized at a single targeted frequency. This means that the antenna-rectifier interface and the matching network mostly consider a narrow band operation. However, the received power can be significantly attenuated if the energy harvester is placed in a physical environment with different characteristics. The energy harvester performance experiences a peak when the impedance of the antenna and the impedance of the rectifier are conjugately matched. There are numerous studies in the literature

that explore dual-band or wide-band approaches for more robust operation. Despite the increased complexity of the design, it could be especially beneficial to have a wide-band energy harvester if the intention is to place harvester tags into different structures (i.e. bone, tissue, muscle, air etc.).

Still, even though a narrow band operation is intended, the input impedance of the rectifier can be arranged in a way that the reduction in the sensitivity due to impedance mismatch between antenna and rectifier can be minimized at the expense of peak sensitivity. Briefly, a design with higher immunity to impedance mismatches, hence, to environmental changes, is possible. A more detailed explanation and some simulation results will be given in section 3.2.1 to prove the above statement.

1.4 Technology

The ICs are designed using the TSMC 65nm CMOS technology. The adopted process features nine metal layers, metal-insulator-metal (MIM) capacitor and transistor models. Apart from the conventional transistors, the technology also includes thick oxide n-channel field effect transistors (NFETs) and thick oxide p-channel field effect transistor (PFETs), high- and low-threshold transistors and deep n-well layer. Among them, low threshold voltage (V_{th}) transistors and the deep n-well layer are especially beneficial as the sensitivity value is under direct influence of the threshold value of the rectifier transistors. Therefore, all the n-channel metal oxide semiconductor field effect transistors (NMOS) and p-channel metal oxide semiconductor field effect transistors (PMOS) have their own body-source connection in order to avoid the body effect. From the perspective of technology node, energy harvester design favors the newer processes as the threshold voltage of transistors decrease as the technology scales. The IC designs are performed using the foundry provided models in Cadence.

2 LITERATURE REVIEW

2.1 Available Energy Sources

As stated previously, energy harvesting is a process that the energy harvester accumulates the small amount of power from ambient energy sources over time and provides the subsequent circuit with the required DC power. This process is possible through the existence of ambient energy sources such as wind energy, vibration, solar energy, heat energy and RF energy. These energy sources have different requirements to be exploited. For example, the solar energy needs solar cells to be available for use which would bring a concern of area. Similarly, the vibration energy requires a piezoelectric material that occupies large area for small sensor applications. The power densities of the mentioned energy sources also differ. Table 2-1 includes a summary of respective power densities and requirements of each energy sources [4].

Table 2-1. Available Ambient Energy Sources

	Solar Energy		**Thermal Energy**	**RF Energy**		**Piezoelectric Energy - Vibration**	
	Outdoor	**Indoor**	**Industry**	**GSM**	**Wi-Fi**	**Human Motion**	**Machine Motion**
Power Density ($\mu W/cm^2$)	100 mW/cm^3	100 $\mu W/cm^3$	10000	300	150	40	80
Availability	Day Time		Always	Always		Activity Time	
Area Requirement	Large		Large	Small		Large	

As can be seen from the above table, although the solar energy can supply a huge power density, it fails in terms of area constraints and its non-continuous operation. These criteria prove decisive considering the small area and continuous operation requirement of IoT sensors in almost

all application areas. Thermal energy, similarly, fails due to area constraints although it provides continuous operation. The piezoelectric energy is generated from mechanical activities such as vibration. That means that the energy is sustained as long as there is a mechanical motion. However, the output is highly varied as it faces some irregular motions. In comparison with the rest of the energy sources, RF energy sources do not depend on environmental changes, therefore, the RF energy source is widely accepted and used to harvest energy especially for IoT sensor applications. A study [5] explored available RF energy sources in London area. The respective power density of each RF source is given in Table 2-2.

RF band is a wide frequency band starting from kHz and covers until GHz range. RF energy harvesters exploits different energy sources at different frequencies. Apart from the source listed in Table 2-1, RF energy sources also include amplitude modulation (AM) radio broadcasting signals covering the frequency range of 525 – 1705 kHz, frequency modulation (FM) radio signals covering 87.5 – 108 MHz, TV broadcasting signals covering 54 - 88 MHz, 174 - 216 MHz, 470 - 806 MHz, ISM bands 902 - 928 MHz or 2.4 - 2.5 GHz.

Table 2-2. Available RF Energy Sources in London Area

Band	Frequency (MHz)	Average Power Density (nW/cm^2)	Maximum Power Density (nW/cm^2)
GSM900 (MTx)	880 - 915	0.45	39
GSM900 (BTx)	925 - 960	36	1930
GSM1800 (MTx)	1710 - 1785	0.5	20
GSM1800 (BTx)	1805 - 1880	84	6390
3G (MTx)	1920 - 1980	0.46	66
3G (BTx)	2110 - 2170	0.12	240
Wi-Fi	2400 - 2500	0.18	6

Besides RF energy harvesting, wireless energy transfer is also possible through near field transfer techniques such as resonant inductive coupling and magnetic resonance coupling [6]. For these techniques, however, the drawback is the rapidly decreasing power strength with distance, at the rate of 60 dB per decade. This does not allow power transfer over larger ranges. On the other hand, far-field RF transmission has the power strength attenuation of 20 dB per decade which does not limit the power transfer as much. For wireless sensor networks, far-field RF energy harvesting proves to be more advantageous as the sensor networks are expected to be widely spread over an area.

An interesting study can be found in [7] where the aim is to exploit multiple energy sources simultaneously. The authors explore the design of a dual (solar + electromagnetic) energy harvesting powered communication system at 2.4 GHz ISM band and -15.6 dBm sensitivity is accomplished for 2.8 V output voltage by exploiting both electromagnetic (EM) and light sources.

2.2 Application Areas of Energy Harvesters

There has been an extensive research concentrated on the energy harvesters recently. Although it is a relatively newer concept, researchers are trying to utilize energy harvesting in a most efficient way. Even though recently emerging IoT applications draw the most attention, there are also different application areas where energy harvesters can be very useful. This section investigates the various application areas of energy harvesters found in the literature.

Today, the demand and advancements in smart systems are growing exponentially. Smart agriculture is one of the systems that requires massive amount of sensor networks in order to utilize the usage of resources such as moisture or nutrition for the plants. This is possible by building up different sensor networks to monitor the moisture and nutrition level of sets of plants allowing the

farmers to take action immediately if any abnormality observed [8]. Similarly, livestock can also be monitored through similar sensors. The body temperature or the body movement of each livestock can be tracked to detect any kind of disease or abnormality.

The second area where the RF powered sensor networks could be useful is the smart buildings and homes [9]. This concept relies on the constant communication of multiple devices over a cloud network where the user can remotely and effectively control the devices. For example, temperature of the living room in a house can be arranged or a set of devices can be programmed to start operating remotely. To get rid of long run maintenance and replacement costs, the power can be supplied to these sensors by RF energy harvesting.

Recently, some companies [10], [11] have also released RF energy harvesters that can be used in several areas. Among them, there are office products such as keyboards, mouses, headphones, smart watches etc. without any need of battery. Additionally, there are also commercially available tags that can be used in inventory management and product tracking.

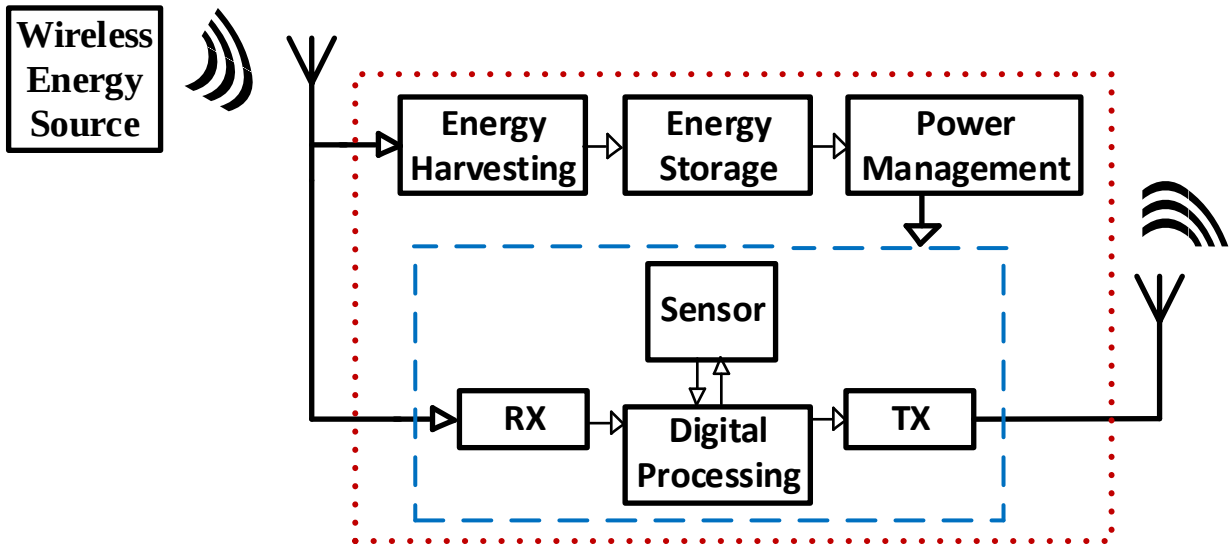

Figure 2-1. Energy Harvester with Sensor Nodes

Figure 2-1 shows a complete chip scheme that includes an energy harvester unit to power a sensor node. All the on-chip blocks can be powered up through energy harvesting while a power management unit governs the overall power delivery.

Advancements in RF energy harvesting facilitated the use of wirelessly powered devices in biomedical applications as well. Among them, implantable energy harvester tags are studied in [12] where the investigation was on the feasibility of direct and forward links for ultra-high frequency (UHF)-RFID tags implanted into human limbs. Implantable energy harvester tags are useful for health monitoring purposes. They can monitor several body reactions over time, or they can track level of certain substances in the body.

[13] is another study that investigates the implantable biomedical devices that support wireless powering and communication. A typical active implantable device architecture and building blocks are presented while the discussion is made on improving power link by utilizing focused powering through transmitter optimization. A quasi-isotropic RF energy harvester is introduced in [14] for autonomous long distance IoT operations. The authors demonstrate an energy harvester composed of four series connected rectennas which can achieve an activation distance over 26 meters in the best-case condition.

2.3 Existing Approaches to Energy Harvester Design

2.3.1 Rectifier Topologies

Multi-stage rectifiers are incorporated in modern RF energy harvesters where the threshold voltage of the rectifying elements determine the sensitivity of the harvester. To overcome the high threshold problem, there are several techniques proposed in the literature. The main idea lying behind most of today's energy harvesters was firstly discussed by J.F. Dickson in 1976. In that

work [15], charges are being pumped along the multiplier chain causing a progressive voltage built after each multiplier stage. Figure 2-2 illustrates the conventional Dickson voltage multiplier.

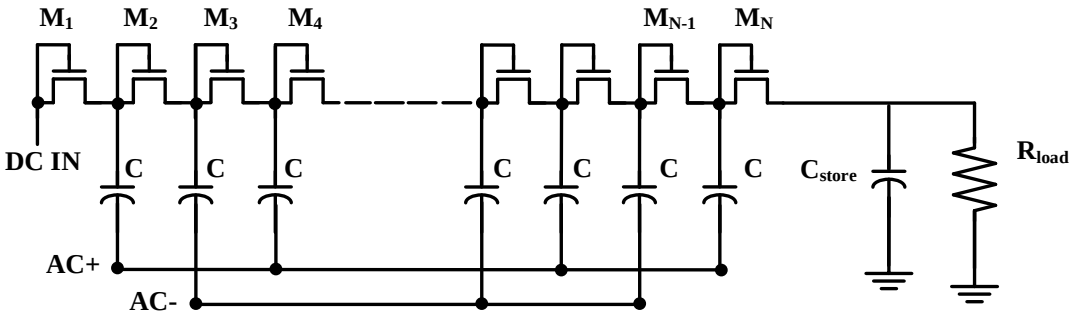

Figure 2-2. Conventional Multi-Stage Dickson Rectifier

In this topology, there is a differential AC voltage applied as the rectifier input, where the storage capacitor accumulates the DC voltage across its terminals and supplies the resistive load with a current. Originally, Dickson voltage multiplier was designed for DC multiplying purposes, thus, requiring an input DC voltage. The RF equivalent of this topology is realized by simply grounding the $DC\ IN$ node and using available RF energy as an input instead of dedicated clock signals.

The working mechanism of the above topology is as follows. For the sake of simplicity, disregard the reverse leakage of the transistors and assume that the rectifier operates at the steady state. Let a sinusoidal signal with an amplitude of V_{AMP} and period of T to be applied at the $AC+$ node while $AC-$ node is grounded. Further assume that the first half of each cycle is the duration that the sinusoid input level is below 0 and the second half of each cycle is the duration that the sinusoid input level rises above 0 for $AC+$ node. Referring to Figure 2-2 and under above assumptions, the leftmost capacitor is charged to voltage level of $-V_{AMP}$ during the first half cycle. During the second half cycle of the first period, $AC+$ reaches the value of V_{AMP}, pushing the voltage level of the first node to $2V_{AMP}$. The capacitors cannot discharge back since the preceding

transistor is reverse biased and the charges are constantly transferred to subsequent node through the following transistor. The above described flow only gives a brief concept and omits the presence of threshold voltage, V_{th}, of transistors. In fact, the voltage rise diminishes by V_{th} after passing through each transistor. Therefore, a minimum amount of input signal level is required to overcome the threshold voltage, implying that V_{AMP} must be greater that V_{th} for proper operation. However, as far as the RF energy harvesting is concerned, the signal level drops significantly with the distance to the source according to Equation 1-1. Because of the diminished power, the input signal level may not be able to overcome the threshold voltage of the transistors in a standard CMOS process. Consequently, researchers seek for more advanced solutions to overcome the threshold voltage of rectifier transistors.

Among them, [16] offered technology-based solution by using zero-V_{th} transistors. However, using non-standard CMOS process increase production cost and still does not prove to be quite effective due to increased reverse leakage.

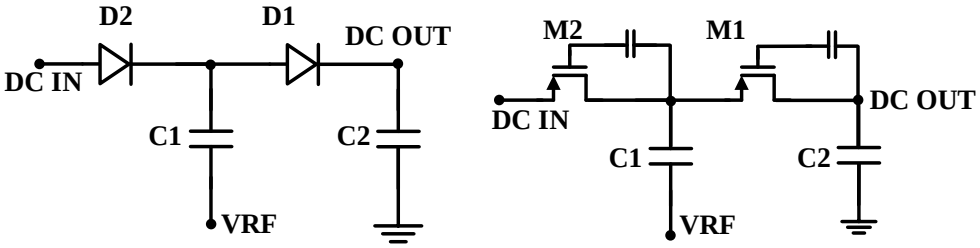

Figure 2-3. A Conventional Voltage Doubler Rectifier (left) and a PMOS Floating-Gate Rectifier (right)

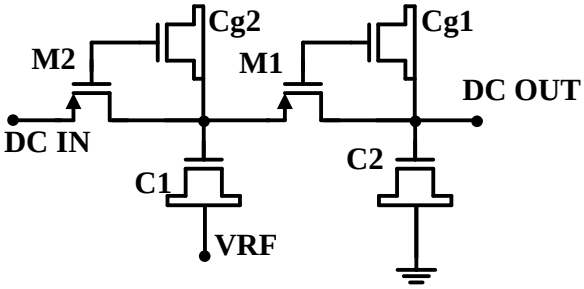

Figure 2-4. Transistor Level Schematic of PMOS Floating-Gate Rectifier

Another study [17] uses floating-gate devices where pre-biasing is required on floating gates. In this topology, a charge is injected into the floating gate of the transistor and it remains in the gate oxide due to high impedance of the oxide layer in order to reduce the threshold voltage of the rectifier. Figure 2-3 shows the schematics of a conventional voltage doubler and a PMOS floating-gate rectifier while the transistor level schematic of the floating-gate rectifier is seen in Figure 2-4.

The floating-gate device can be designed by connecting a metal oxide semiconductor (MOS) capacitor between the gate and drain of the transistor as displayed in Figure 2-4. Since the gates of both MOS transistors are connected together, a high impedance node has been created to trap the charges at the floating gate. These trapped charges behave as a voltage bias at the gate of the rectifier transistor, creating an effective gate to source potential difference, which effectively helps to overcome the threshold voltage of the transistor. It is utterly critical that a high impedance is sustained at the floating node so that the charges are retained for a long time to provide a useful lifetime of the device. Nevertheless, this topology demands pre-charging of the floating gates, which may be problematic in some applications where pre-charging is not an option.

On the contrary to above proposals, the optimum solution must be free of pre-charging and must avoid the use of additional circuits in conventional process options. For this purpose, researchers explored smart circuit solutions where a self-threshold compensation is achieved. The self-compensation method was first claimed in [18], where the gate of each transistor is connected to the source of the proceeding transistor as illustrated on the left side of Figure 2-5. This compensation technique provides a bias voltage offset equal to the voltage increment at each stage, approximately $Vout/N$ where N stands for the number of stages and $Vout$ stands for the output voltage. However, for designs that employ large number of stages, this improvement is almost negligible and does not bring a substantial performance improvement. Depending on the threshold

voltage of the process and required output voltage, the order of compensation may be increased. For instance, instead of shorting the gate of each transistor to the source of the following transistor, one can short it to the source of the following third transistor or so. Connecting it to the source of second following or any even number following transistor would fail due to the inconsideration of alternating phase at each stage. The order of compensation can be further increased to improve the gate biasing as shown on the right side of Figure 2-5.

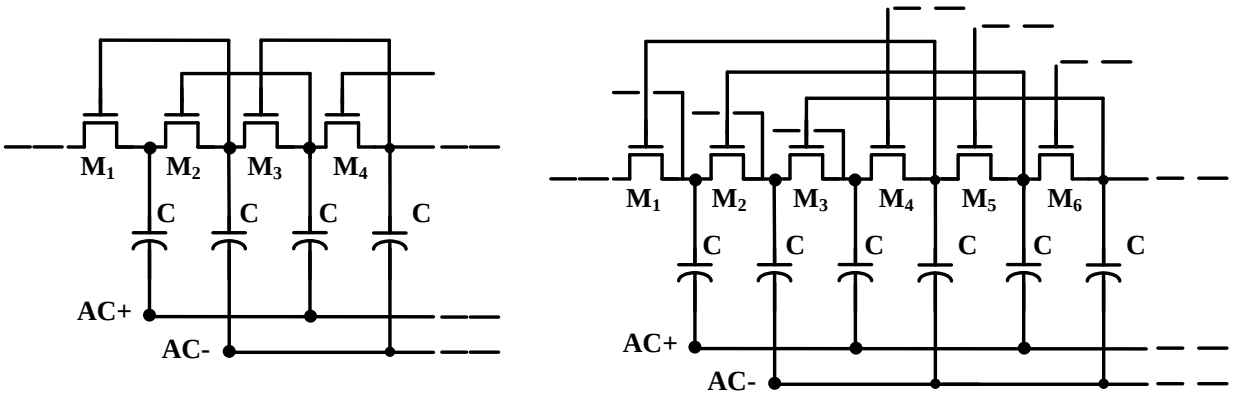

Figure 2-5. Single Order Self Compensation Method (left) and Higher Order Self Compensation Method (right)

A more sophisticated symmetrical differential drive topology is given in [19]. The circuit in Figure 2-6 illustrates a single state cross coupled differential configuration. Referring to Figure 2-6, the circuit operation in this topology can be described as follows. The gate of each transistors is actively biased with differential mode signal. When $AC+$ is negative and $AC-$ is positive, transistors M_1 and M_4 are turned off while M_2 and M_3 are turned on. Therefore, the charges accumulated at node X can only flow through M_2 as M_1 transistor is already turned off. Similarly, the accumulated charge at the preceeding node (source of M_3) can now flow through M_3 increasing the amount of charge at node Y. This operation continues and the charge flow between the stages increase the voltage after each stage progressively. Note that M_2 and M_4 are PMOS transistors

whereas M_1 and M_3 are NMOS transistors. Hence, W/L ratios of NMOS and PMOS pairs must be scaled based mobility difference between them which is a process dependent parameter.

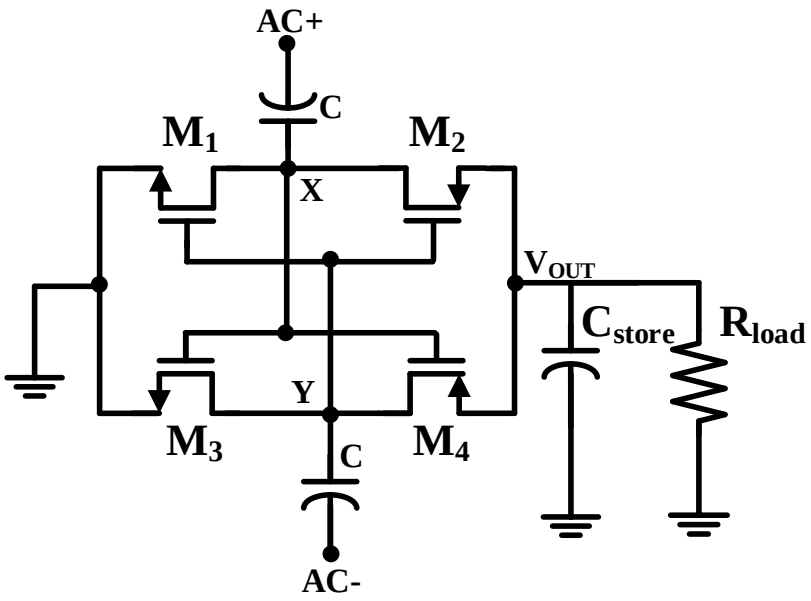

Figure 2-6. A Differential Drive Rectifier Circuit

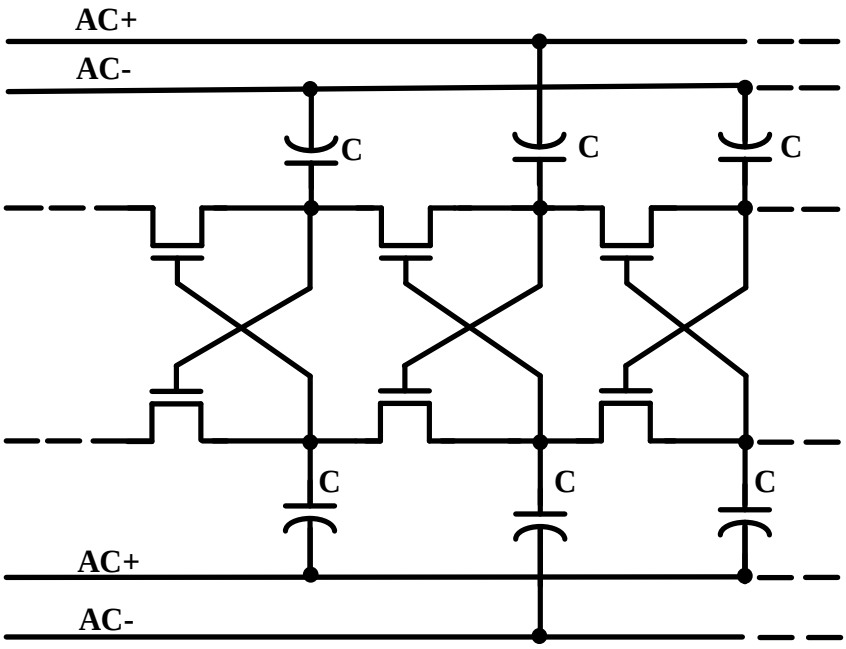

Figure 2-7. Threshold Self Compensation in Differential Drive Topologies

Similar compensation as described previously can also be applied to the circuit in Figure 2-6 by connecting the gate of each transistor to the common node of the transistor pair at the opposite side as illustrated in Figure 2-7. The order of compensation can be further increased. However, the phase of the signal at each node must be considered while determining the order of compensation.

2.3.2 Exploration of Different Frequency Bands

In addition to investigation of several rectifier topologies, researcher have also explored energy harvesters operating at different frequencies. As explained in section 2.1 thoroughly, there are various RF signals at different frequencies roaming around with considerable power densities. Multiple studies have exploited different frequency bands and even examined multi-band or wide-band approaches.

Among them, [20] examined a rectenna functioning at three different LTE bands: 0.79 - 0.96 GHz, 1.71 - 2.17 GHz and 2.5 - 2.69 GHz. In this design, different rectifiers and antennas are designed for different frequencies and their outputs are summed at the end through a DC combining technique. Although having different rectennas for different frequencies reduces the complication, the total occupied area is increased which requires additional compactness for applications like implantable energy harvester tags. This effort achieves a sensitivity of -20 dBm.

Unlike the above study, [21] demonstrates a dual-band RF energy harvester that operates at 915 MHz and 2.44 GHz by using a single dual-band rectenna. This study achieves a -19.5 dBm of sensitivity for 1 V output voltage at 915 MHz while the sensitivity value improves to -25 dBm at 2.44 GHz for the same output voltage level.

Most commonly, the frequency of operation for energy harvesters in [3], [22], [1], [23], [19], [24], [25], [26] is the ISM band of 902 – 928 MHz in North America and 868 MHz in Europe. A

triple band energy harvester is given in [1] where ISM bands of 900 MHz, 2.45 GHz and 5.8 GHz are used altogether.

[27] is based on 2.4 GHz operation and the effort achieves -34.5 dBm sensitivity for an output voltage of 1.6 V with a resistive load of 1.8 MΩ. A more detailed table on state-of-the-art energy harvesters with employed techniques will be given in section 2.4.

2.4 State of the Art Energy Harvesters

As mentioned throughout section 2, there are several approaches to energy harvester design. Besides the exploration of different frequency bands, researchers also explore different topologies and techniques to improve the overall harvester performance. Table 2-3 gives a broad list of state-of-the-art energy harvesters in the literature with their respective performance parameters.

Table 2-3. State-of-the-Art Energy Harvesters

	[1]			[3]	[19]	[22]	[23]	[24]	[25]	[26]
Technology	180 nm CMOS			90 nm CMOS	180 nm CMOS	130 nm CMOS	90 nm CMOS	65 nm CMOS	130 nm CMOS	65 nm CMOS
Frequency (MHz)	915	2450	5800	868	953	915	915	900	902 - 928	2400
Sensitivity (dBm) @Vout, Rload = ∞	N.A	N.A	N.A	-27, 1V	N.A	-31.8	-24	-17.7	N.A	-30.7
Sensitivity (dBm) @Vout, @Rload	-19.4	-16.2	-14.2	-23, 1 V, 1 MΩ	-13, 1 V, 100 kΩ,	N.A	-18.3, 1.2 V, 1MΩ	-16, 1 V, 147 kΩ	-20.5, 1 V, 1 MΩ	-25, 1 V, 1 MΩ
	1.8 V, 5.45 MΩ									
Max PCE @RF Input Power, @Rload, @Vout	N.A			40%, -17 dBm	82.6%, -24.5 dBm, 100 kΩ	N.A	16.1%, -15.83 dBm	36.5%, 147 kΩ	32%, -15 dBm, 3.2 V	38%
Efficiency @Minimum RF Input Power	N.A			7%, -23 dBm	N.A	N.A	11%	N.A	N.A	36%
Requirement	-			Control Loop	-	-	Deep n-well	Deep n-well	-	Deep n-well

3 ENERGY HARVESTER DESIGN METHODOLOGY

3.1 Overview

Design of energy harvesters includes a receiving antenna, a high-sensitivity and efficient rectifier, an additional unit that governs the power scheme of the harvester, namely the power management unit and a load that draws current from the built-up DC voltage and stored charge.

RF energy harvesting deals with small amount of powers. The operation is based on the accumulation of small-scale input RF signals and their rectification. Therefore, every building block must be carefully analyzed and must be designed for smallest possible internal power consumption. For instance, rectifier must be efficient in rectifying RF signals. Similarly, power management unit must consume small power in order not to disrupt the overall harvester operation. The load of energy harvester is also quite important while selecting design parameters. For a load that is expected to draw large amount of current at a fixed voltage level, the energy harvester design becomes more challenging as the delivered power to the load simply increases. Nevertheless, co-design of every building block is advantageous for the designer as it provides an additional degree of freedom.

In this study, design methodologies of rectifier and power management unit will be given in detail. A thorough discussion will be made upon the design parameters of each block. As stated in section 1.2, the antenna-rectifier co-design is also crucial for the overall harvester performance. Although this work does not focus on antenna design, requirements of antenna–rectifier co-design will be provided as well.

This work exploits two different rectifier topologies. First one is a multi-stage approach similar to the one shown in Figure 2-6. The second one, on the other side, employs a threshold

compensation method as illustrated in Figure 2-7. Both approaches are based on the differential drive principle realizing full wave rectification.

3.2 Rectifier Design

3.2.1 Antenna–Rectifier Co-Design

The principle behind the energy harvesters relies on an antenna capturing the roaming RF signals and providing the rectifier terminals with a certain amount of voltage. The amount of voltage that is developed across the rectifier input terminals depends on the received power by the antenna, input impedance of the rectifier and the output impedance of the antenna. In order to prevent the reflections between antenna and rectifier, an excellent impedance matching between antenna and rectifier impedances is of quite importance. In order to visualize this interface, an illustration is provided in Figure 3-1.

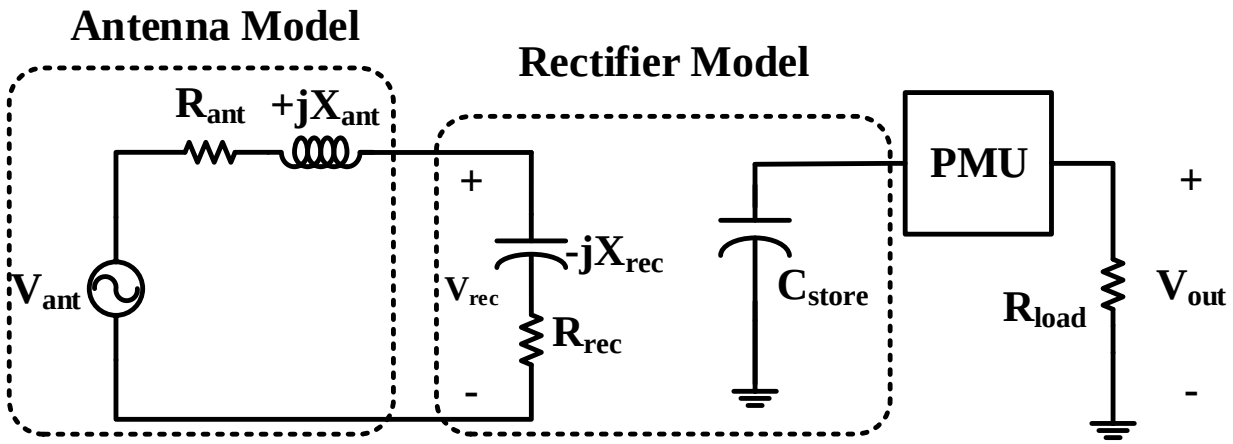

Figure 3-1. Antenna–Rectifier Interface

In the above figure, the capacitive and resistive input impedance of the rectifier can be modelled with a resistor and a capacitor in series. Because a conjugate matching is required between rectifier and antenna impedances, the desired antenna must have an inductive impedance. The antenna impedance is modelled with a resistor and an inductor in series. Furthermore, for the

sake of clarity, the received power by the antenna is represented by a voltage source. Based on the Thevenin equivalent circuit principle, V_{ant} value can be given as follows.

$$V_{ant} = \sqrt{8R_{ant}P_{av}} \tag{3-1}$$

P_{av} represents the available power that is received by the antenna. Note that the above equation omits the existence of radiation loss of the antenna. Based on the radiation efficiency, an additional loss resistance must be added in series with R_{ant}. The predominant purpose is now to provide the rectifier with largest possible voltage. Antenna-rectifier conjugate matching is the first step to prevent reflections. Afterwards, the aim is to maximize V_{rec} which is possible through passive voltage boosting, G_{boost}. The equation that relates V_{ant}, V_{rec} and the impedances is given as follows.

$$G_{boost} = \frac{V_{rec}}{V_{ant}} = \frac{X_{rec} + R_{rec}}{X_{rec} + R_{rec} + X_{ant} + R_{ant}} \tag{3-2}$$

Considering the above equation, the way to maximize V_{rec} is to maximize V_{ant} and G_{boost} simultaneously. By arranging the impedance parameters on the right-hand side of the equation, G_{boost} can be maximized. Ideally, when a conjugate match exists, $X_{rec} = -X_{ant}$, and assuming that $X_{rec} \gg R_{rec}$, Equation 3-2 reduces into Equation 3-3.

Therefore, passive voltage boosting is maximized when X_{rec} is maximized and the resistive terms are minimized. Combining the above equations, P_{av} reduces into Equation 3-4.

$$G_{boost} = \frac{V_{rec}}{V_{ant}} \approx \frac{X_{rec}}{R_{rec} + R_{ant}} \quad 3\text{-}3$$

$$P_{av} = \frac{(R_{ant} + R_{rec})^2}{{X_{rec}}^2} \frac{{V_{rec}}^2}{8R_{ant}} \quad 3\text{-}4$$

$$P_{av} = \frac{(R_{ant} + R_{rec} + X_{rec} + X_{ant})^2}{(R_{rec} + X_{rec})^2} \frac{{V_{rec}}^2}{8R_{ant}} \quad 3\text{-}5$$

Equation 3-4 is useful in determining the rectifier design parameters. Ideally, as voltage boosting, G_{boost}, goes to infinity, the energy harvester performance must increase. However, there are additional challenges when the quality factor (Q-factor) of the rectifier impedance, which is the ratio of X_{rec}/R_{rec}, grows larger. The biggest challenge of a high Q-factor impedance is the reduced tolerance to impedance mismatches. Having a lower Q-factor impedance and lower G_{boost} results in an energy harvester that is more immune to impedance mismatches. This points out to smaller degradations in sensitivity due to impedance mismatches for lower Q-factor impedances.

There is already a design trade-off between improved peak sensitivity and immunity to impedance mismatches. Equation 3-5 gives the complete expression for P_{av} where the conjugate matching does not exist. If impedance mismatch exists, which is the case when X_{ant}/X_{rec} ratio is different than 1, then Figure 3-2 illustrates the sensitivity behavior with respect to the amount of mismatch based on Equation 3-5. Note that, the numbers are arbitrarily chosen, and they do not refer to any actual design. This is a mathematical derivation for demonstration purposes.

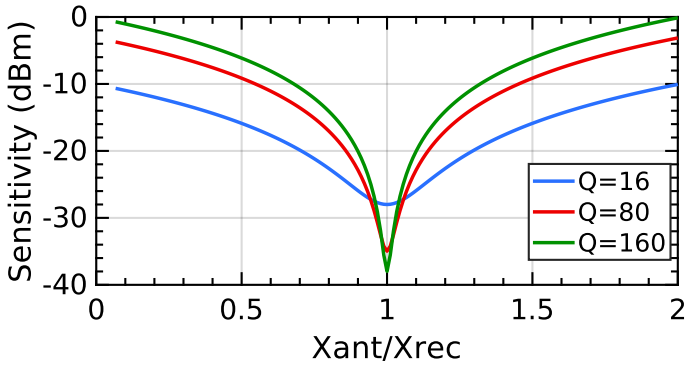

Figure 3-2. Mismatch in Imaginary Impedances vs. Sensitivity for Different Q-factor Values

As can be seen in the above figure, although a high Q-factor antenna-rectifier interface favors the peak sensitivity when a perfect match exists, the sensitivity value diminishes rapidly as the amount of mismatch increases. For instance, at the mismatch amount of 50%, $X_{ant}/X_{rec} = 0.5$, blue curve shows the greatest sensitivity even though it performs much worse at the perfectly matched case. Therefore, impedance matching becomes even more crucial if a high Q-factor impedance is chosen for the rectifier. Considering that impedance matching becomes more difficult and requires a larger inductor for high X_{rec} values, it may be more beneficial to choose a reasonable X_{rec}value resulting in a lower Q-factor to ease the matching and to save area at the expense of sacrificed peak sensitivity.

3.2.2 Transistor Types and Sizing

As revealed in the last paragraph of section 3.1, this work employs two different multi-stage differential drive full wave rectifier topologies. Despite the slight differences between those two, the main procedure remains very similar. In both topologies, the transistor characteristics must be carefully investigated as they play a significant role on the rectifier performance.

First, in order to interpret the effect of each design parameter, the circuit must be isolated from the effects of other design parameters as much as possible. Therefore, instead of digging into

multi-stage approach, a single stage topology must be carefully analyzed at first. Besides, the impedance matching concerns must also be momentarily disregarded. Towards that aim, the differential drive topology in Figure 2-6 is further analyzed by inserting a differential sinusoidal voltage source with a particular frequency and a particular amplitude as shown in Figure 3-3.

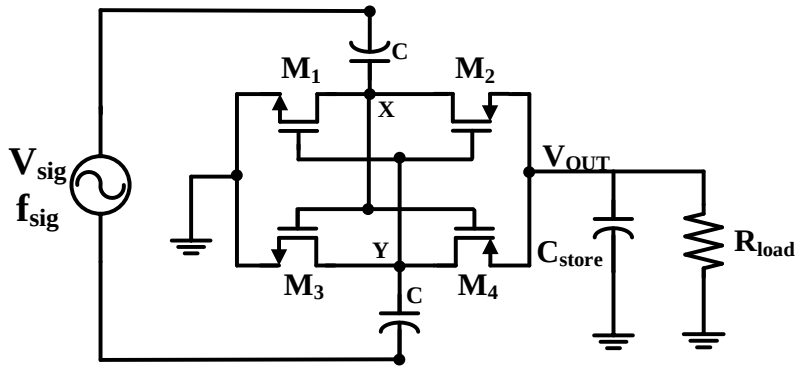

Figure 3-3. Analysis Setup for a Single Stage Topology

In this setup, the input amplitude is fixed, thus, the focus is merely on the internal parameters of transistors. In this consideration, the threshold voltage of transistors, the width to length ratio (W/L) and PMOS and NMOS design matching are of high importance. The common conception in the literature states that maximum output voltage for a given input amplitude points to higher efficiency. Even though this concept holds true most of the time, it neglects the effect of transistor sizing, hence, the secondary effects like leakage and parasitics are mostly disregarded. If the transistor size is increased continuously, it is true that conduction is improved. However, larger transistors possess larger parasitic capacitances, thus, poorer RF performance. Moreover, too large device size results in increased leakage conduction as well. Therefore, a study must be conducted to find an optimum device size that maximizes the overall performance. There are some studies [16], [17] in the literature that report optimum transistor sizing. In this work, the length of every transistor is set to minimum allowed value of 60 nm to avoid larger parasitics. Afterwards, some set of simulations have been run to find out the optimum device size for each harvester cell.

Nonetheless, it is still important to keep in mind that current approach analyzes the effect of device size alone, ignoring the interactive and complete design procedure.

Figure 3-4 gives the developed output voltage in time with respect to different device sizes where m stands for the number of transistors operating in parallel. The unit size of each transistor is $W = 1.2\,\mu m, L = 60\,nm$ for NMOS, and $W = 3.6\,\mu m, L = 60\,nm$ for PMOS transistors. Based on Figure 3-4, $m = 5$ is chosen since increasing m further would increase the parasitics without a remarkable improvement in the output voltage. Note that, these values are valid only for one design cell that exploits the available low threshold voltage transistor and originally having 8 stages overall. The same simulation also assumes the presence of 1 MΩ resistive load. Similar simulations are also run for each design cell that uses various transistor types or different number of stages. It is also verified that the mobility difference between NMOS and PMOS transistors can be accounted by setting $(W/L)_{PMOS} = 2.6\,(W/L)_{NMOS}$. Furthermore, all the fabricated designs make use of deep n-well layer in the adopted process by employing NMOS transistors with isolated bodies to avoid the body effect.

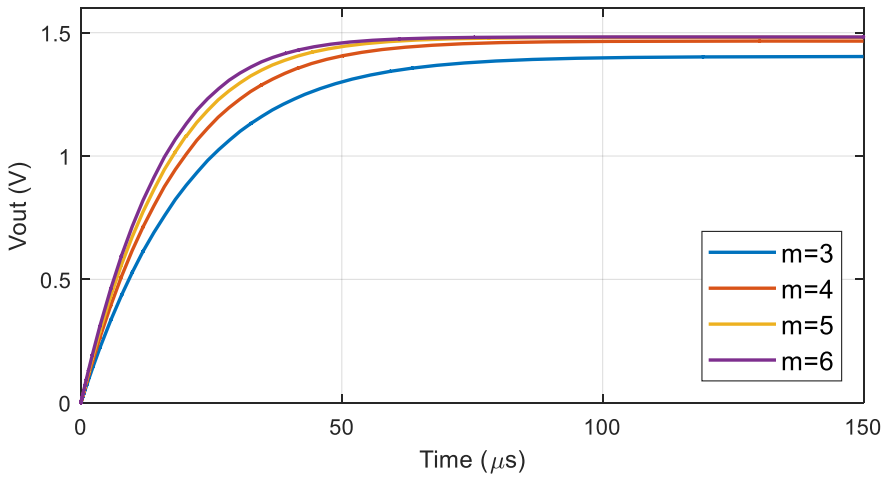

Figure 3-4. Output Voltage Transient Waveform for Different Device Sizes

Other than the tradeoff between direct conduction, reverse leakage and parasitics, there is another design variable that is under direct influence of device sizing. The rectifier input impedance heavily depends on the device size along with the number of stages. Even though a more detailed analysis on transistor size and rectifier input impedance relationship is spared for section 3.2.3, a brief description will be given for the sake of completeness.

Referring to left side of Figure 3-5, the rectifier input impedance is evaluated differentially. The role of the transistor type and size is notable as each transistor could be basically represented by resistors and capacitors. Using larger transistors would result in increased capacitor while a smaller resistor is observed. This yields smaller X_{rec} and R_{rec} values. As mentioned in section 3.2.1, the design requires a precise analysis of impedance matching between antenna and rectifier. In this sense, device sizing provides an additional design freedom to come up with a reasonable rectifier impedance along with the total number of stages.

3.2.3 Rectifier Input Impedance

The differential drive topology in Figure 2-6 can be further analyzed by inserting a 100 Ω differential port to determine the input impedance of a single rectifier as shown in the left side of Figure 3-5. In this setup, the impedance seen by the differential circuit refers to input impedance of a single stage rectifier. This impedance is highly dependent on the transistor size as mentioned in section 3.2.2. Fixing the transistor size only based on direct conduction, reverse leakage and parasitics leaves the designer a single design parameter to adjust the rectifier input impedance. Number of stages would be the only design parameter left to determine the impedance. However, this may require using large number of stages to obtain an impedance that could be matched with an antenna easily. It is another design challenge since increasing the number of stages continuously

reduces the efficiency again due to increased reverse leakage. Therefore, device sizing and determination of the number of stages are the two parameters that must be co-optimized.

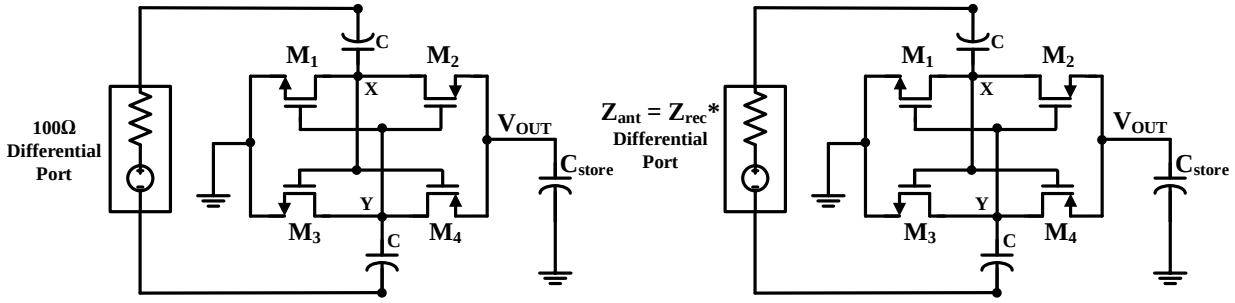

Figure 3-5. Impedance Analysis Setups for Single Stage Topology

The primary purpose here is to build the configuration shown on the right side of Figure 3-5 where $Z_{rec} = Z_{ant}$ in order to guarantee the maximum power transfer.

Table 3-1 shows the input impedance of single stage differential drive rectifiers with same transistor sizes in different technology nodes. 45 nm CMOS technology provides the lowest Q-factor impedance whereas 130 nm CMOS technology provides the highest. All designs include transistors with minimum lengths allowed in the process. Therefore, 130 nm process has lowest imaginary part of the impedance as it has the largest transistor capacitances due to longer length of the rectifier transistors.

Table 3-1. Single Stage Differential Drive Rectifier Input Impedances in Different Technology Nodes

Transistor Size (NMOS - 1 µm, PMOS - 2.8 µm)	**Single Stage Z_{in}**
45 nm CMOS	428 - j59875
65 nm CMOS	60 - j29800
130 nm CMOS	25.7 - j28410

3.2.4 Number of Stages

As revealed in the last paragraph of section 3.1, this work employs two different differential drive full wave rectifier topologies. Despite the slight differences between those two, the main procedure remains very similar. Both of those topologies are implemented in multi stage configuration for various reasons. This section will examine the reasons lying behind the multi-stage approach.

After analysis of single stage topology in previous sections, the effect of increasing the number of stages on the rectifier performance must be investigated. Referring the two-stage topology in Figure 3-6, the relationship between the required input voltage amplitude and the number of stages for a fixed output voltage value is of great importance. For instance, for a 1 V output DC voltage, two-stage topology will require smaller input amplitude in comparison with the single stage topology. In other words, for a fixed amount of input amplitude, two-stage topology would produce larger DC output voltage compared to single stage topology. At this point, the question would be the extent up to which increasing the number of stages keep benefiting the rectifier performance. Ideally, required rectifier input amplitude would decrease almost linearly with increasing number of stages. However, having higher number of stages also causes increased power consumption. The power consumption, in this context, is due to reverse leakage. A constant increase in the number of stages also gives rise to reverse leakage current and even results in a reduction in the rectifier efficiency. Also, after some point, the input amplitude cannot be reduced as it becomes too small and cannot overcome the threshold voltage of transistors.

Another aspect of number of rectifier stages would be the impedance. As mentioned in section 3.2.3, number of stages play a significant role in rectifier input impedance since it basically equals to parallel combination of each rectifier stage impedances.

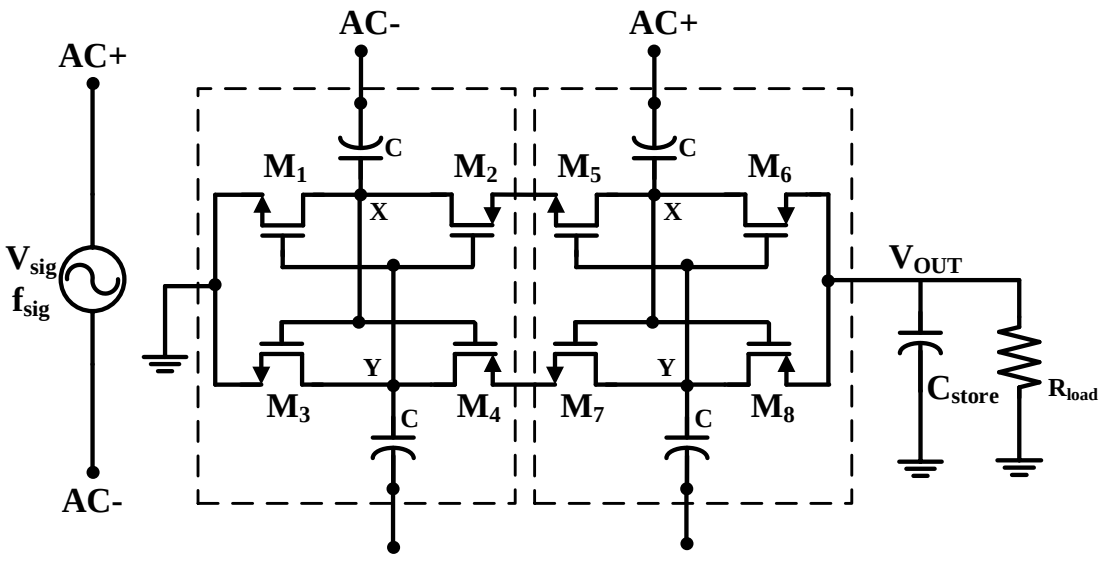

Figure 3-6. Two-Stage Topology Schematic

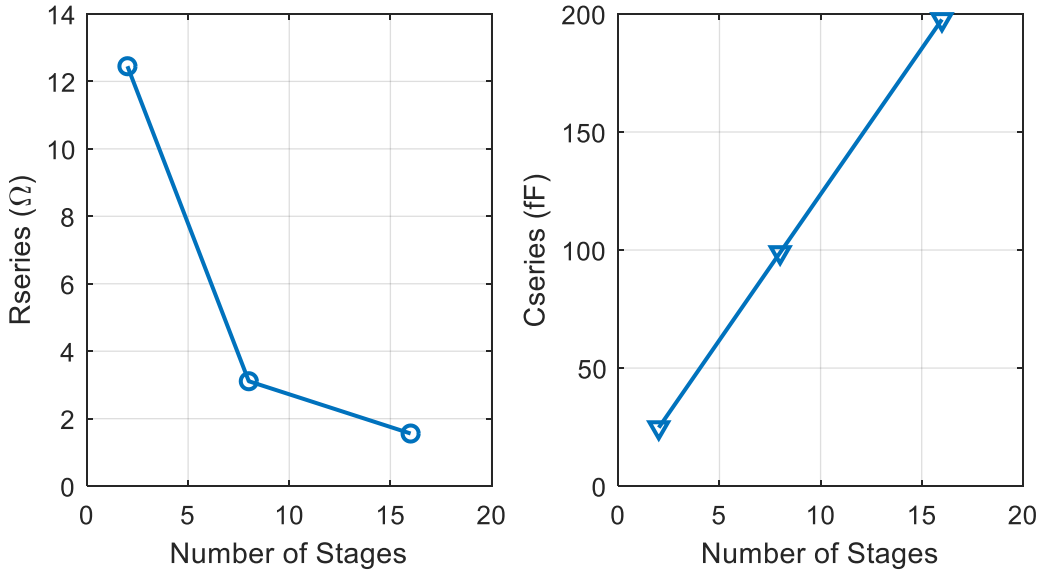

Figure 3-7. Rectifier Input Impedance for Different Number of Stages

If the impedance of the rectifier is represented with a series resistor and a series capacitor as in Figure 3-1, the equivalent series resistance diminishes with the increasing number of stages while the equivalent series capacitance increases as can be seen in Figure 3-7. Therefore, along with the transistor sizing, number of stages is also a significant design parameter to control the rectifier impedance.

After going through the effect of stage number, the assumption of having an ideal voltage source at the input, as shown in Figure 3-5, can be abandoned in order to account for the rectifier impedance effect. Assuming a fixed device size, and referring to Equation 3-4, it is now mathematically evident that V_{rec} is a function of number of stages with a linear inverse proportion. Similarly, X_{rec} also has a linear inverse proportion with number of stages. Therefore, increasing the number of stages would generate the same effect on these two parameters, leaving P_{av} unaffected. Then, based on the same equation, if $R_{ant} = R_{rec}$ is satisfied, P_{av} would be minimized, implying an excellent sensitivity. However, the assumption that increasing number of stages would decrease V_{rec} with a linear inverse rate does not hold completely true due to reverse leakage problem as mentioned earlier. Also, having smaller number of stages would decrease the overall series capacitance seen looking into the rectifier which would result in huge imaginary part of the input impedance. Then, it becomes quite challenging to match the antenna impedance to that of the rectifier. The inevitable impedance mismatch then causes reflections, effectively reducing the energy harvester sensitivity. Increasing the number of stages also increases the charging time as the signal basically has longer path to travel. This study includes several different fabricated energy harvesters with different number of stages. A complete list of fabricated designs will be given in section 4.

3.2.5 Coupling and Load Capacitances

This section gives a discussion on the methodology of choosing coupling and load capacitances. The values of these capacitors affect the transient behavior of the circuit without any influence on the sensitivity values. It is also shown in [16] that the coupling capacitor value larger than 100 fF is sufficient to sustain an unaffected harvester performance given that load current is small enough. In this study, the coupling capacitance value is chosen to be 170 fF and they are

implemented by using high density MIM capacitors. Depending on the application, the load capacitance can be chosen differently. For the applications that require rapid refresh late, a smaller load capacitance would be a better choice as the charge and discharge times are shorter. On the contrary, for the applications that do not require rapid refresh rate, a larger load capacitance would be preferable because of their larger charge storage capacity. The largest density of the MIM capacitors in the adopted process is 2 fF / μm^2. Therefore, it would be area inefficient to put an on-chip load capacitor. For demonstration purposes, this study employs load capacitors ranging from 13 pF to 20pF. For additional charging capacity, larger off-chip capacitors can be used. Figure 3-8 shows simulated output waveforms in time for different load capacitance values. As can be seen, the steady state output voltage remains the same with changing capacitor sizes. This points out to unchanged sensitivity value.

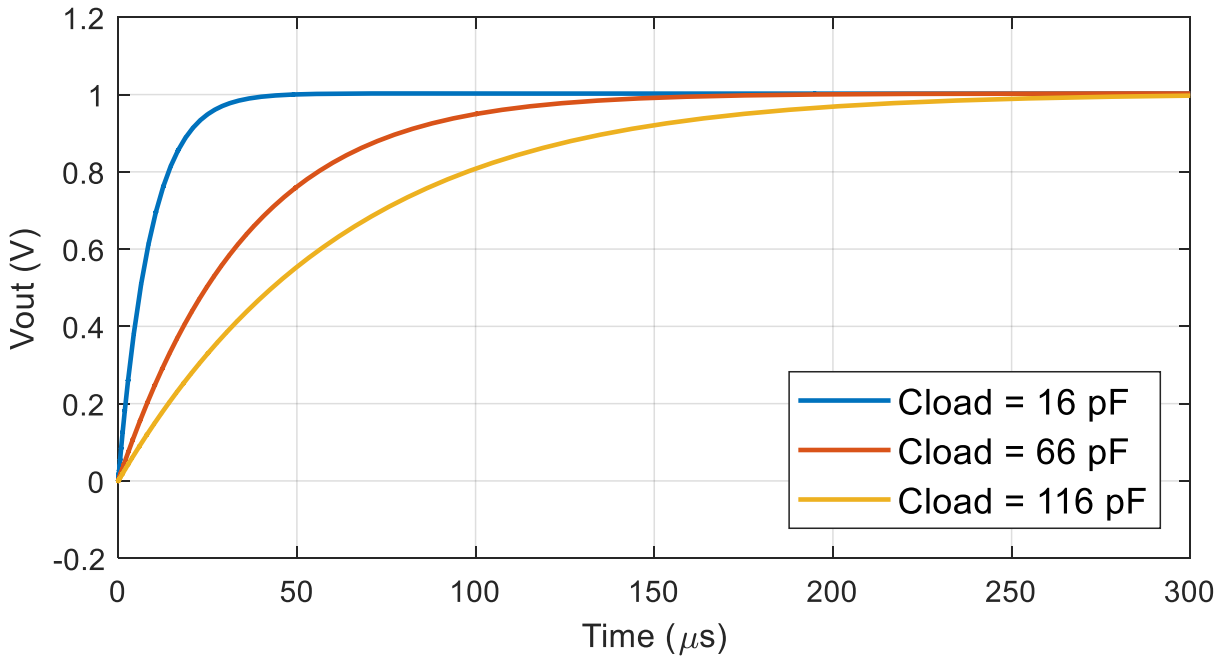

Figure 3-8. Output Voltage Transient Waveform for Different Load Capacitances

3.3 Power Management Unit Design

Unlike many other conventional RF energy harvesters, this design employs an additional unit to govern the entire power scheme. Conventionally, the stored DC output voltage is directly used to deliver power to the load of energy harvester. However, directly connecting the output of the energy harvester to the load results in power delivery to the load before a desired output level is reached. Therefore, it requires higher input power to reach the same DC output level. Also, charging time increases presenting a disadvantage for the applications that require rapid operation and faster refresh rates. The employed power management unit prevents power delivery to the load until a desired upper threshold voltage ($V_{th,high}$) is reached. Only when the output voltage reaches $V_{th,high}$ value, the power management unit allows the load to draw current. As the load is drawing current, the load capacitor starts discharging. The discharging operation continues until low threshold value ($V_{th,low}$) is reached. Once the output level is at $V_{th,low}$, the power management unit comes into play again and stops the load from drawing current to prevent the load capacitor from discharging completely. This operation continues in a similar manner and effectively improves the harvester sensitivity. Determining $V_{th,high}$ and $V_{th,low}$ values are completely up to application requirements and they can be set through the adjustments in number of stacked transistors or in the transistor sizes in voltage reference or voltage divider circuits.

A complete schematic of power management unit and the load is given in Figure 3-9. The power management unit consists of a voltage divider, a voltage reference circuit and a comparator. The power management unit is designed to consume ultra-low power in order not to harm the sensitivity value of the energy harvester. It uses the output voltage of the rectifier as VDD.

In this study, a CMOS transistor based reference voltage circuit [28] is used as the resistor based reference circuits require large resistors to keep the power consumption low. Basically, the voltage divider divides the voltage and the comparator compares the divided voltage with the reference voltage value. The switch that is inside the comparator block, referring to Figure 3-9, creates a control voltage that is fed back to the voltage divider in order to adjust the voltage division ratio. The respective W/L ratios of each transistor are given in Table 3-2.

The flow of operation in the power management unit is as follows. Referring to Figure 3-9, suppose that the load capacitor is charging and VDD is raising. The increase in VDD also gives rise to $VDIV$. At the instant that $VDIV$ exceeds $VREF$, then the comparator output becomes high. Having a high comparator output sets $VCTRL$ to low value, allowing N_1 transistor to turn on. Since N_1 and M_5 transistors also draw current now, the voltage division ratio changes and $VDIV$ increase further to keep the load drawing current. Meanwhile, since $VCTRL$ is low M_{21}transistor is turned off which means that VG is high enough to let M_{22} transistor to draw current. In this setup, M_{22} transistor is acting as a load for demonstration purposes. Eventually, the load capacitor is discharged until $V_{th_{low}}$. At this point, $VDIV$ will fall below $VREF$ due to voltage division, leading comparator output to become low, hence resulting in high $VCTRL$. Then, N_1 and M_5 transistors are off causing $VDIV$ to fall even lower. Meanwhile, since $VCTRL$ is high, M_{21} transistor turns on pulling VG to zero which effectively prevents the load transistor, M_{22}, from drawing current. VDD starts raising again.

This setup is a demonstration that energy harvester power scheme can be controlled by an additional unit in order to determine the intervals that a current is supplied to the load or not. Given the size of the transistors, Table 3-2, and the topology adopted, the current that power management unit draws is in nA scale as shown on the right side of Figure 3-10. The voltage waveforms of

some important nodes in the power management unit and the load, referring to Figure 3-9, are also given in Figure 3-10. Power management unit schematic is given Figure 3-11 and the layout of complete power management unit with load is given in Figure 3-12.

Table 3-2. Power Management Unit Transistor Types, Width and Length Values

Transistor Number	Transistor Type	W/L
M_1, M_2, M_3, M_4, M_5	Thick Oxide – NMOS with deep n-well layer	$1\mu m/20\mu m$
M_6, M_7, M_8, M_9, M_{10}, M_{11}	Thick Oxide – NMOS with deep n-well layer	$1\mu m/10\mu m$
M_{12}	Thick Oxide – NMOS with deep n-well layer	$1\mu m/10\mu m$
M_{13}, M_{14}	General Purpose – NMOS with deep n-well layer	$5\mu m/0.3\mu m$
M_{15}	General Purpose – NMOS with deep n-well layer	$1\mu m/1\mu m$
M_{16}, M_{17}, M_{18}, M_{19}, M_{20}	Thick Oxide – NMOS with deep n-well layer	$1\mu m/20\mu m$
M_{21}	Thick Oxide – NMOS with deep n-well layer	$1\mu m/1\mu m$
M_{22}	General Purpose – NMOS with deep n-well layer	$1\mu m/0.2\mu m$
N_1	Thick Oxide – PMOS	$5\mu m/1\mu m$
N_2, N_3	Thick Oxide – PMOS	$1\mu m/20\mu m$
N_4	Thick Oxide – PMOS	$9\mu m/1\mu m$
N_5, N_6	General Purpose – PMOS	$5\mu m/0.3\mu m$
N_7	General Purpose – PMOS	$1\mu m/10\mu m$
N_8	General Purpose – PMOS	$1\mu m/1\mu m$

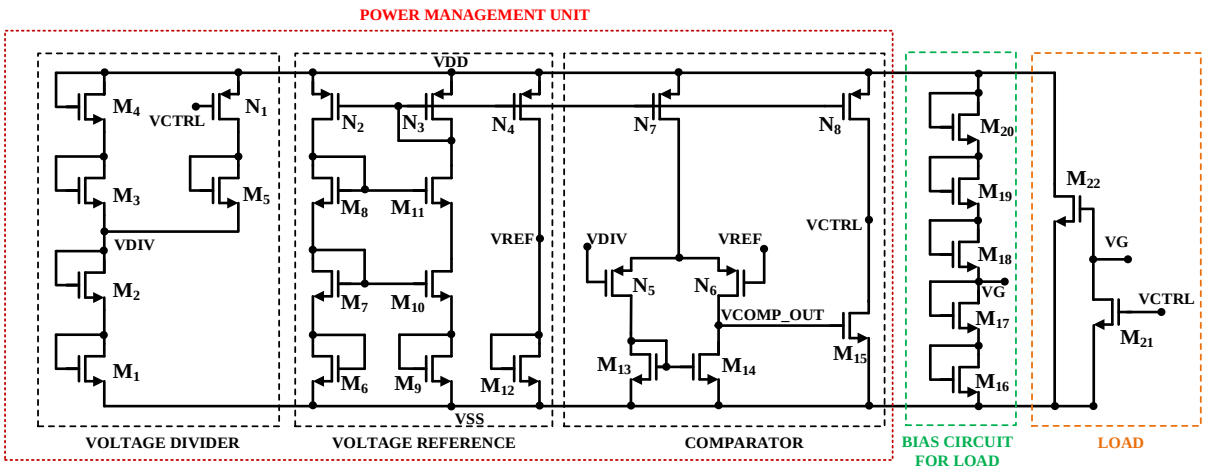

Figure 3-9. Power Management Unit with Load

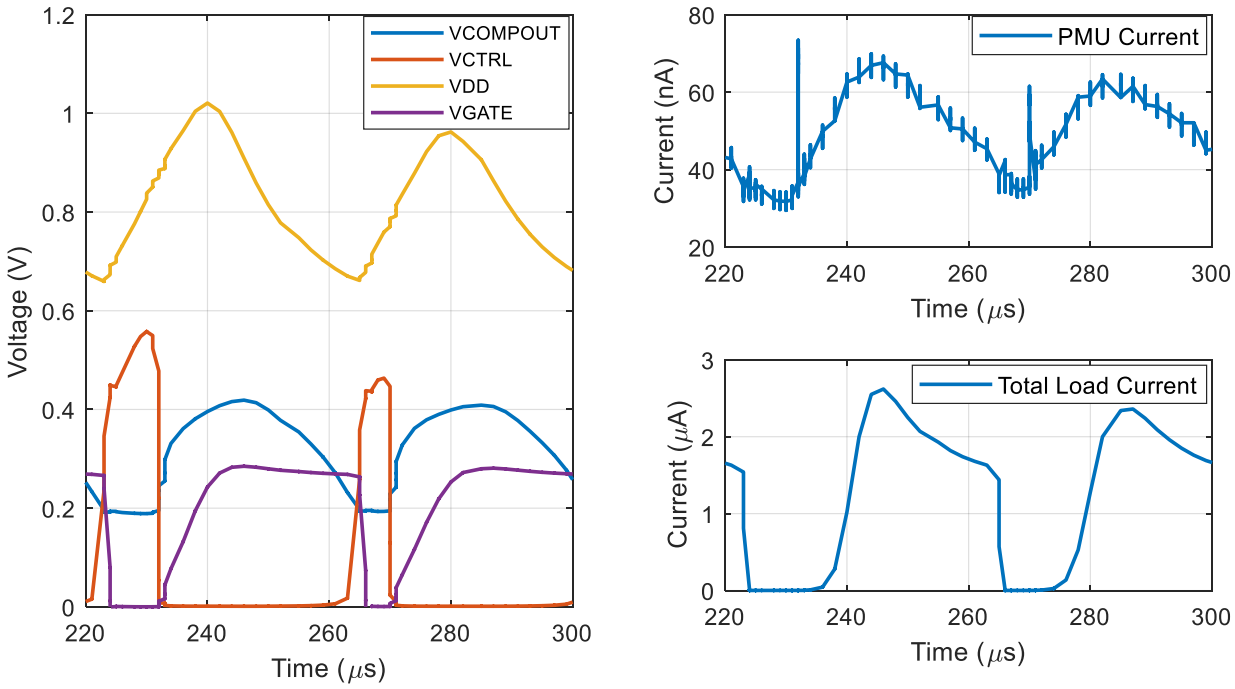

Figure 3-10. Respective Voltage and Current Levels in Power Management Unit and Load

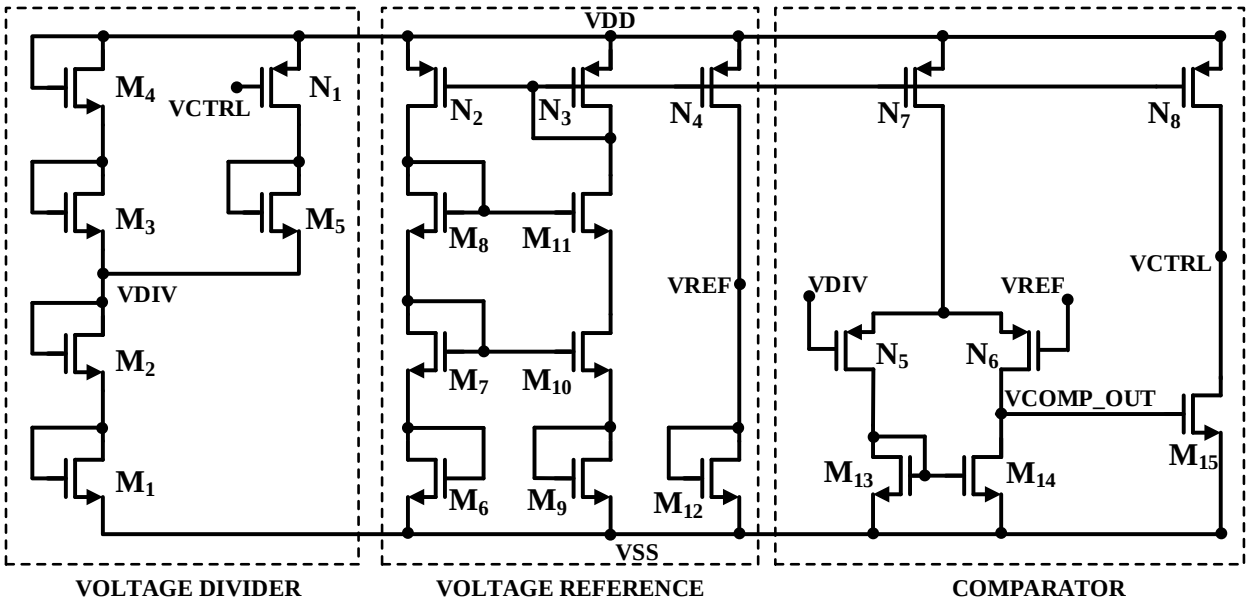

Figure 3-11. Power Management Unit

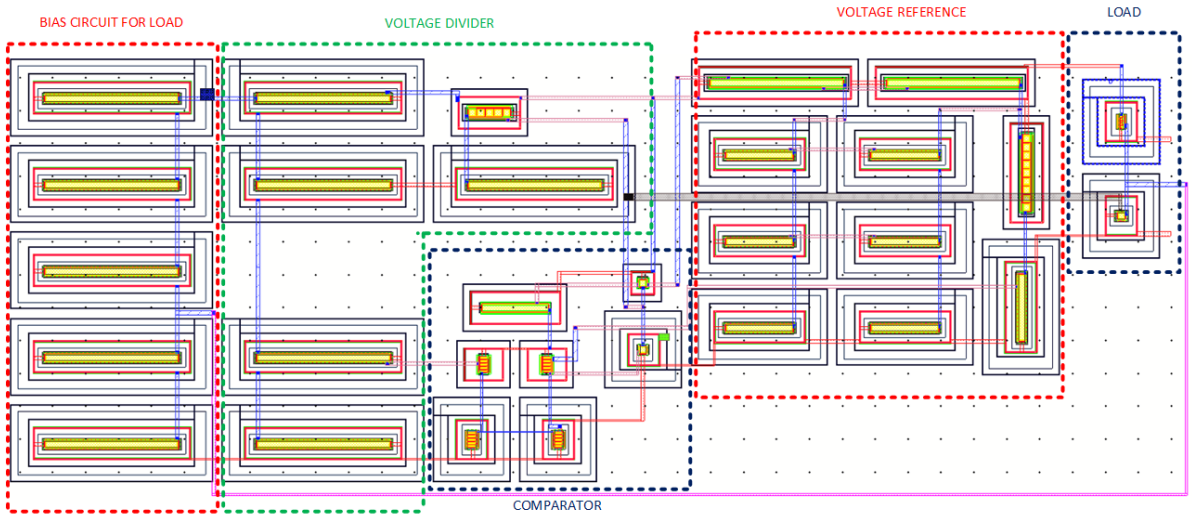

Figure 3-12. Layout of Power Management Unit with Load

4 FABRICATED DESIGNS

This study includes several different fabricated designs, their simulation and measurement results and the comparison between the designs. Namely, designs with different number of stages, different transistor types, different topologies and different frequency of operation are fabricated and measured. The performance of each design will be listed and explained in this section.

Mainly, two different topologies, as in Figure 2-6 and Figure 2-7 are employed with the concentration mainly on the one in Figure 2-6. Besides, 6 stages, 8 stages, 16 stages, 32 stages and 64 stages rectifiers are fabricated, measured and the comparisons will be given. Among them, 8 stages, 16 stages and 32 stages designs have two different versions, one employing power management unit and the other one not employing. In some designs, low threshold voltage transistors are exploited. Finally, one of the designs have 2.4 GHz operation whereas the rest is based on 915 MHz. A complete list is given in Table 4-1. For the rest of this thesis, the fabricated designs will be referred based on their design number that is placed on the first column of Table 4-1.

The fabricated designs differ in terms of their input impedance, and the required V_{rec} for a targeted output DC voltage. Therefore, they have different sensitivity and efficiency values as well. As discussed in section 3.2.4, number of stages have a direct effect on rectifier impedance. Therefore, designs with larger number of stages have impedance values with smaller real and imaginary parts (absolute value). The input impedance of D_9 also has smaller real and imaginary parts (absolute value) since the frequency of operation is 2.4 GHz. Ideally, the impedance should scale linearly with increasing number of stages. However, due to increased area in the layout, hence, increased parasitics from routings, the linear relation does not exist.

In the design process, the layouts of each design are resistance (R) + capacitance (C) + coupled capacitance (CC) extracted. In order to verify the extracted impedance, EM simulations of the routings are also done. For instance, Figure 4-1 shows the EM simulation layout of the input lines for a 16 stage design where the input is distributed parallelly in order to prevent routing parasitics to cause different degradation at the input level for each stage to make sure that the same input is applied to each stage.

Table 4-1. Fabricated Designs

Design Number	Number of Stages	Frequency (MHz)	Rectifier Transistor Type	Power Management Unit	Topology
D_1	8	915	General Purpose - RF	Yes	Figure 2-6
D_2	8	915	General Purpose - RF	No	Figure 2-6
D_3	8	915	Low Threshold	No	Figure 2-6
D_4	16	915	General Purpose - RF	Yes	Figure 2-6
D_5	16	915	General Purpose - RF	No	Figure 2-6
D_6	32	915	Low Threshold	Yes	Figure 2-7
D_7	32	915	Low Threshold	No	Figure 2-7
D_8	64	915	General Purpose - RF	No	Figure 2-6
D_9	6	2400	General Purpose - RF	Yes	Figure 2-6

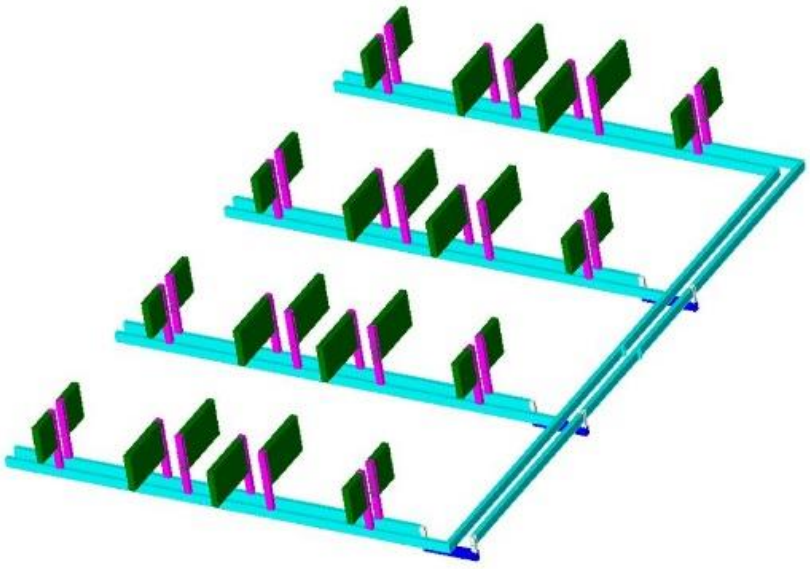

Figure 4-1. Electromagnetic Simulation Layout of the Input Lines

4.1 Simulation and Measurement Setups

The simulation setting for the designed rectifiers is as follows. At first, for each design, an ideal input voltage source is placed, as in Figure 3-3, to determine the amount of input voltage swing required for a desired output voltage. Afterwards, a 100Ω differential port is placed instead of an ideal voltage source across the input terminals of the rectifier to determine the input impedance of the rectifier differentially. After finding out V_{rec}, R_{rec} and X_{rec}, it is now easier to calculate the necessary P_{av} based on Equation 3-4 which assumes the presence of an antenna with a conjugately matched impedance. Furthermore, the calculation can be verified through another set of simulation, as shown in right side of Figure 3-5. A differential port with an impedance that is conjugate of the rectifier impedance and with a power level same as P_{av} is placed and a transient simulation, or an envelope simulation for larger durations, is run to check if the intended output can be obtained. Additionally, in order to model the measurement tool at the output side, a 1 MΩ resistor is placed in parallel with a 30 pF capacitor which are the values specified at the measurement tool datasheet.

The measurement setup, on the other hand, includes the following. The fabricated designs are probed with GSSG probes at the input side to measure the input impedance of the rectifier through Keysight Performance Network Analyzer (N5227A). After the input impedance of the rectifiers are verified, the chips are again probed at the input side with ground-signal-signal-ground (GSSG) probes and connected to a broadband isolated balanced to unbalanced (balun). After differential to single ended conversion, the single ended port of the balun is connected to a signal generator, Keysight Analog Signal Generator (E8257D), which can create sinusoidal signals with certain input power or amplitude at a desired frequency. Meanwhile, the output of the rectifier is also probed, and the output is connected to an oscilloscope, four channel digital storage oscilloscope (Tektronix TBS1064), to observe the output waveform. The output waveforms are captured and transferred to a computer for further analysis which are revealed in section 4.1. The diagrams for measurement setups are given in Figure 4-2.

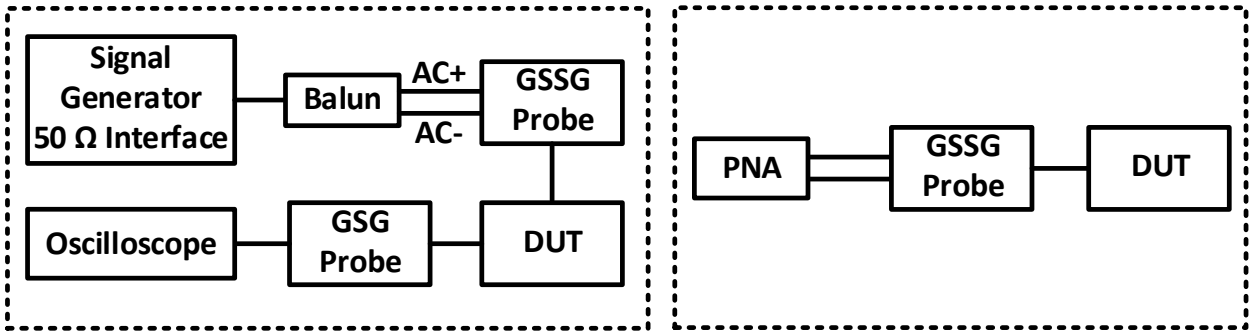

Figure 4-2. Measurement Setups for Output Voltage Waveform (left), and Input Impedance (right)

However, the initial simulation setup differs from the measurement setup for reasons like it is not possible to generate differential signal with the currently owned signal generator. Therefore, a balun had to be used and the simulation setting has also been changed to account for the differences in measurement setup and the measurement tools. Therefore, in order to compare the simulation results with the measurements, a 50 Ω input port is used in the simulations to supply a

single ended input power. Then, the s-parameter file of the broadband balun is inserted into the schematic to model the balun that is used in the measurements. The cable and adaptor losses are also measured for necessary calibrations. Then, finally, the oscilloscope input impedance is added into the schematic as a load of the rectifier.

4.2 Results and Discussion

In this section, measurement and simulation results will be given for each design. As stated in section 4.1, the simulation setup is arranged in a way that it matches with the measurement setup. Then, the interpretation will be on the measurement results with the current setup and how it would translate the expected results if an impedance matched antenna existed. The total loss due to cables, adapters and DC blocks are measured to be 2.5 dB. The measurement results show an agreement with the simulation results.

4.2.1 Design 1: 8 Stages Energy Harvester Design with PMU

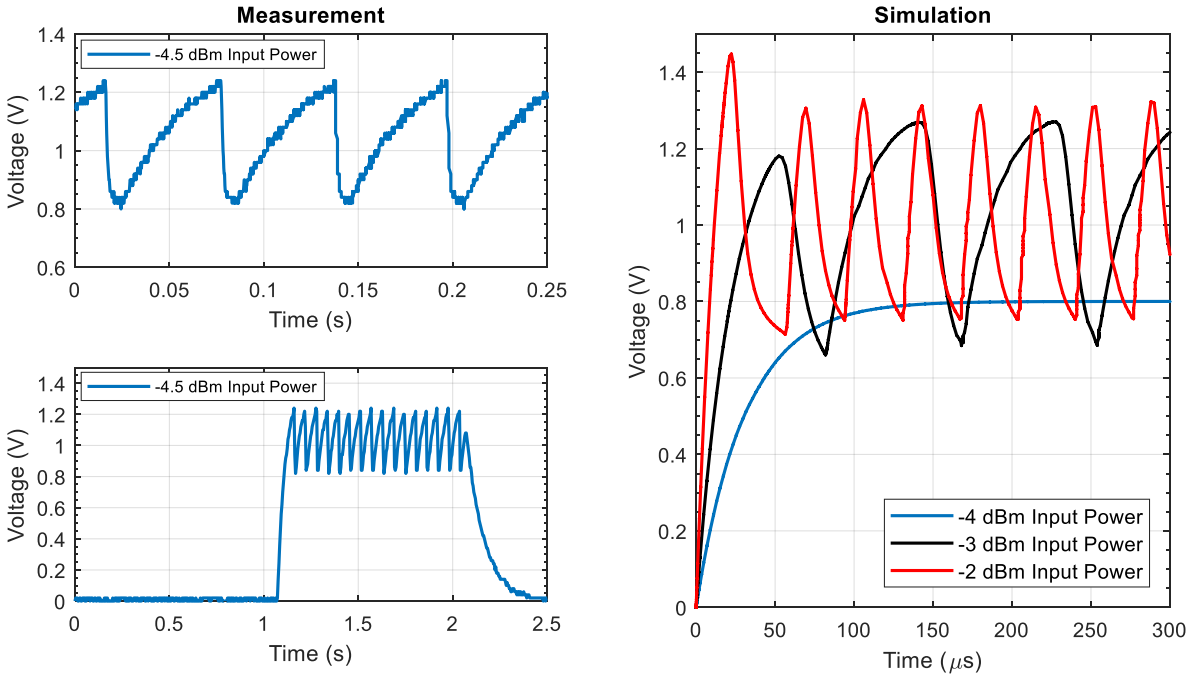

Figure 4-3. Measurement and Simulation Results of Design 1

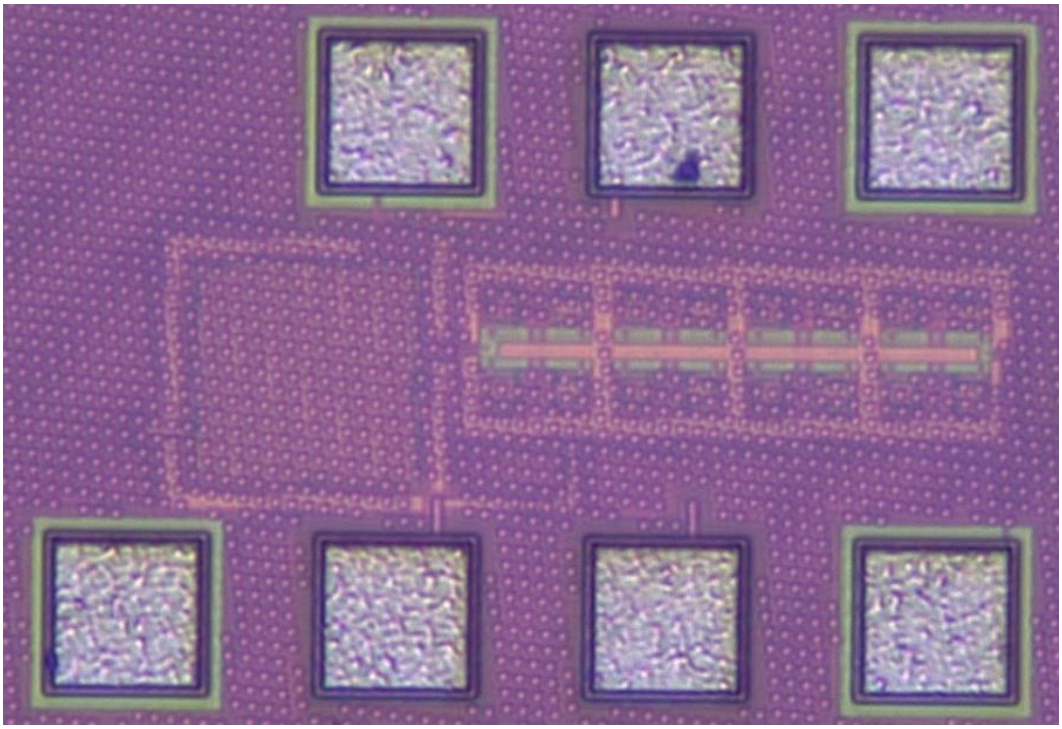

Figure 4-4. Design 1 Micrograph

4.2.2 Design 2: 8 Stages Energy Harvester Design

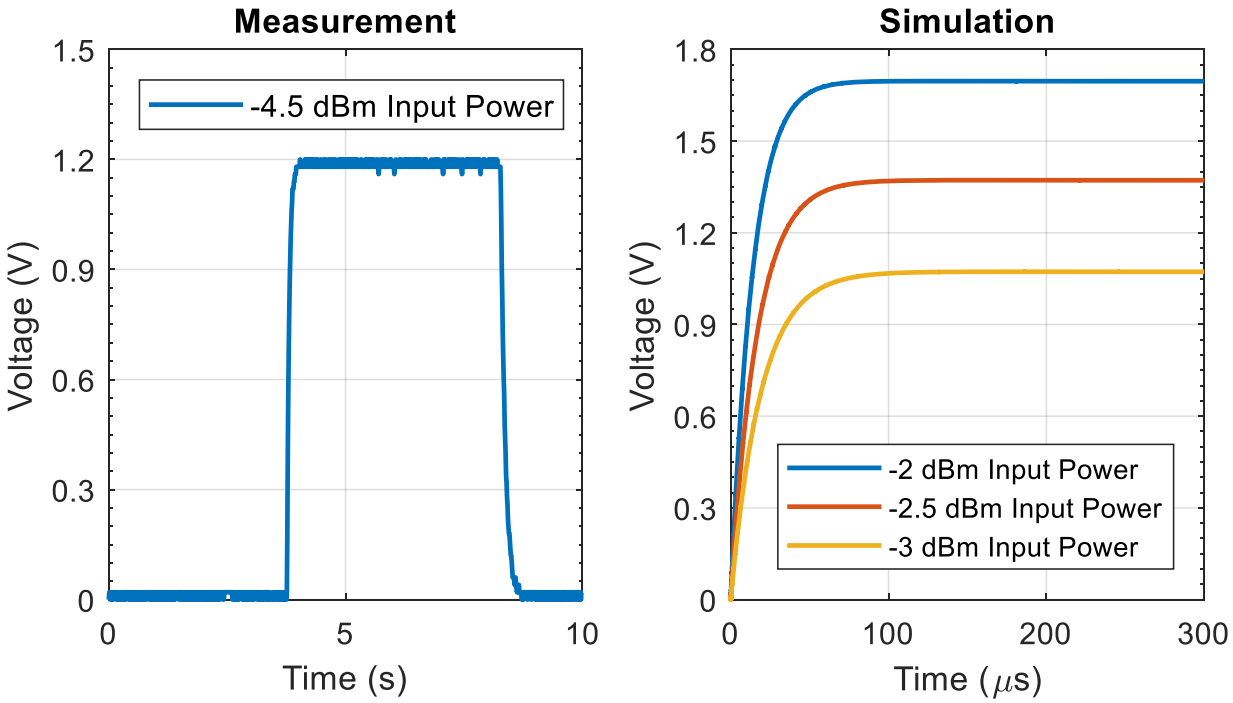

Figure 4-5. Measurement and Simulation Output Transient Voltage Waveforms of Design 2

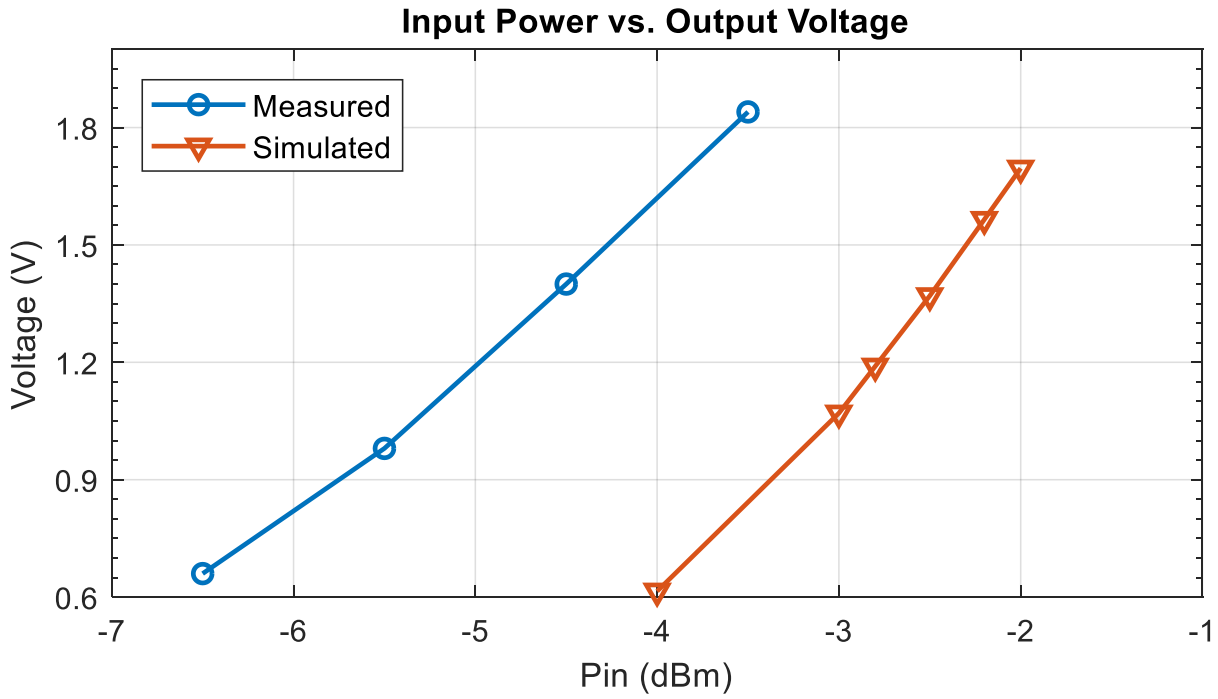

Figure 4-6. Measurement and Simulation Input power vs. Voltage Levels of Design 2

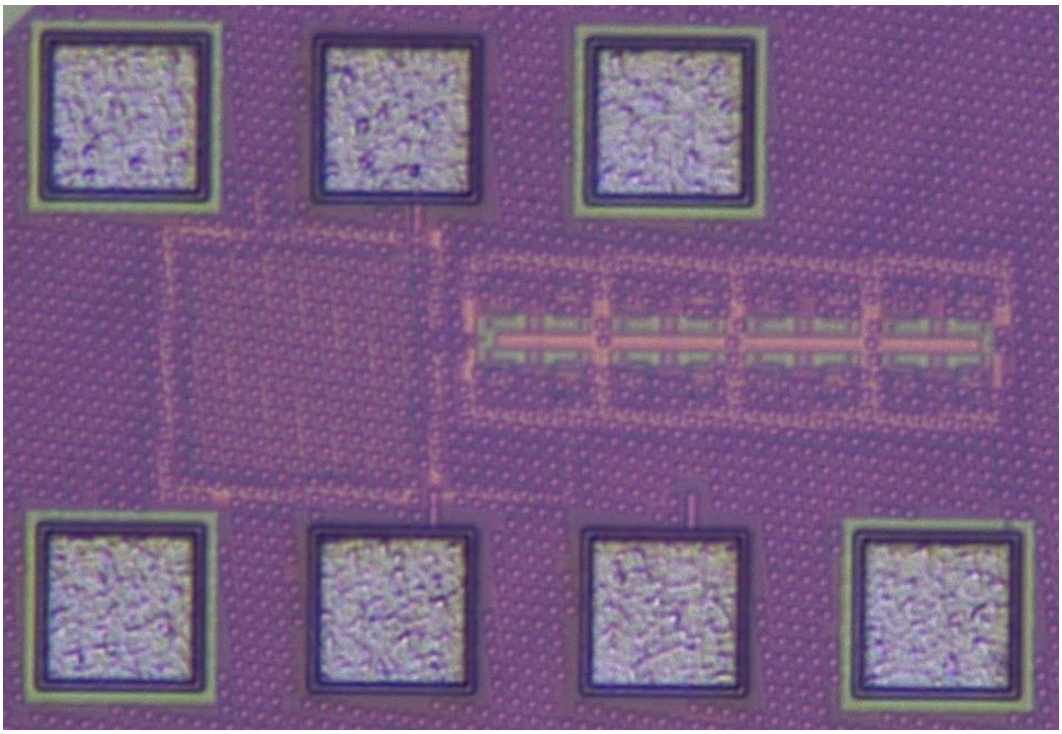

Figure 4-7. Design 2 Micrograph

4.2.3 Design 3: 8 Stages Energy Harvester Design Using Low Threshold Transistors

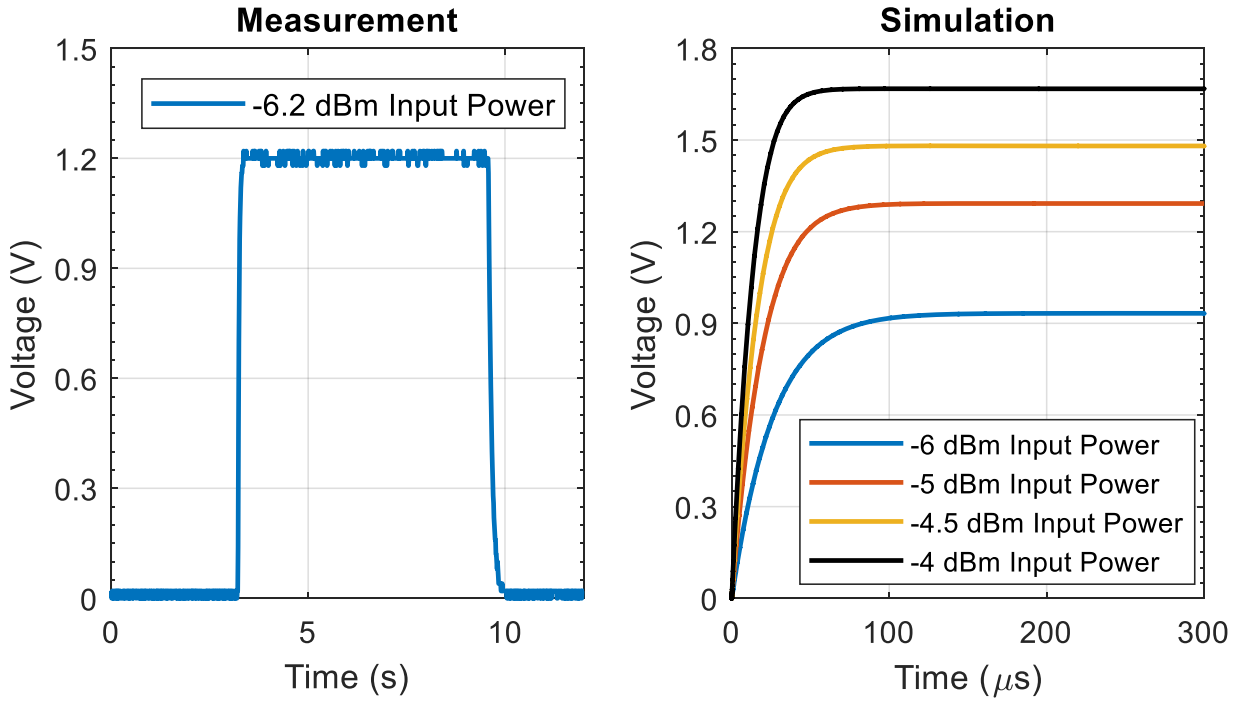

Figure 4-8. Measurement and Simulation Output Transient Voltage Waveforms of Design 3

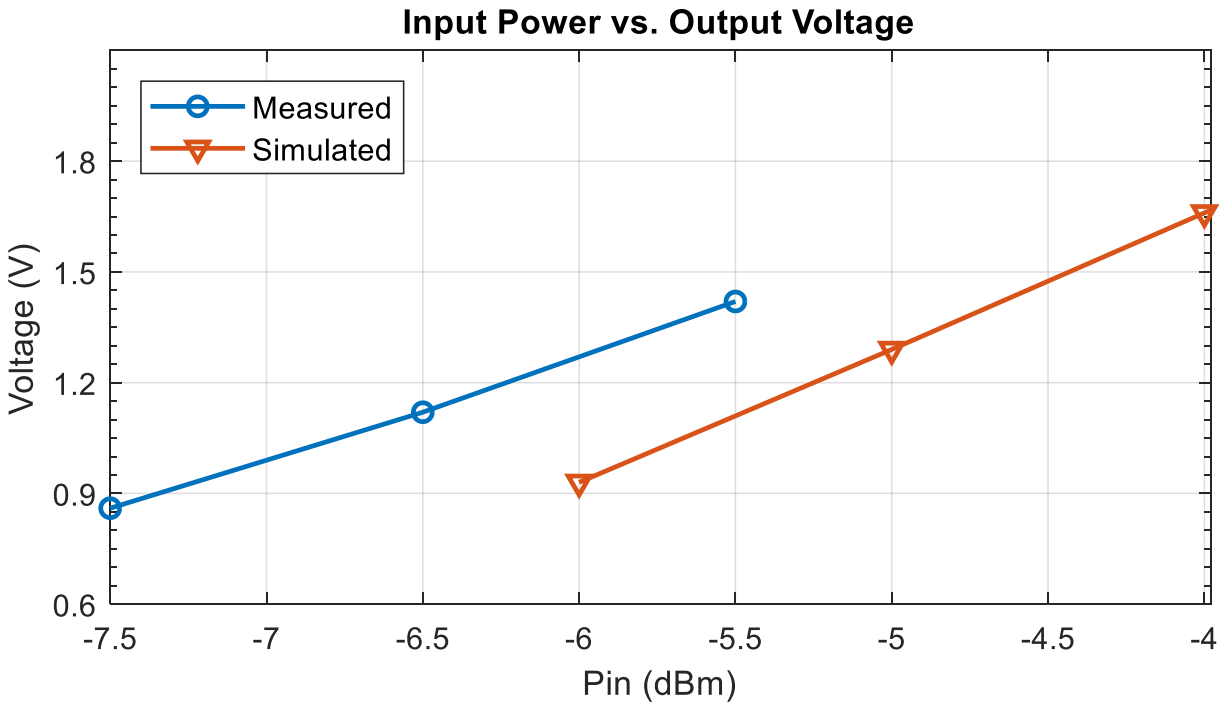

Figure 4-9. Measurement and Simulation Input Power vs. Voltage Levels of Design 3

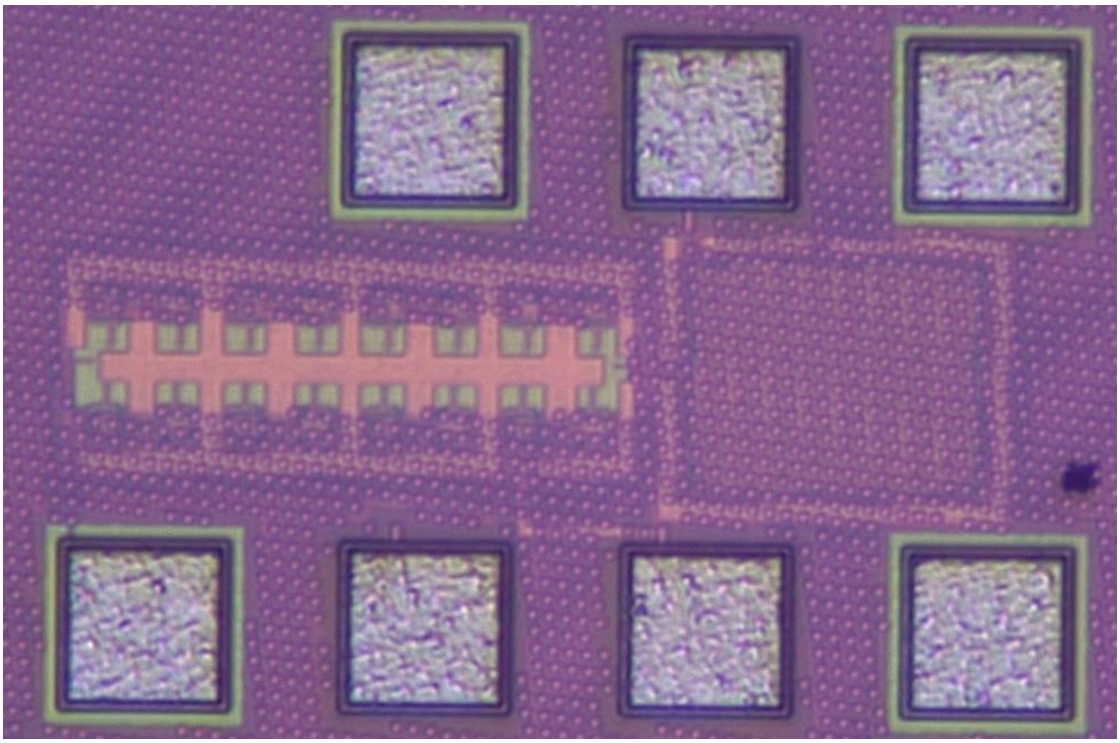

Figure 4-10. Design 3 Micrograph

4.2.4 Design 4: 16 Stages Energy Harvester Design with PMU

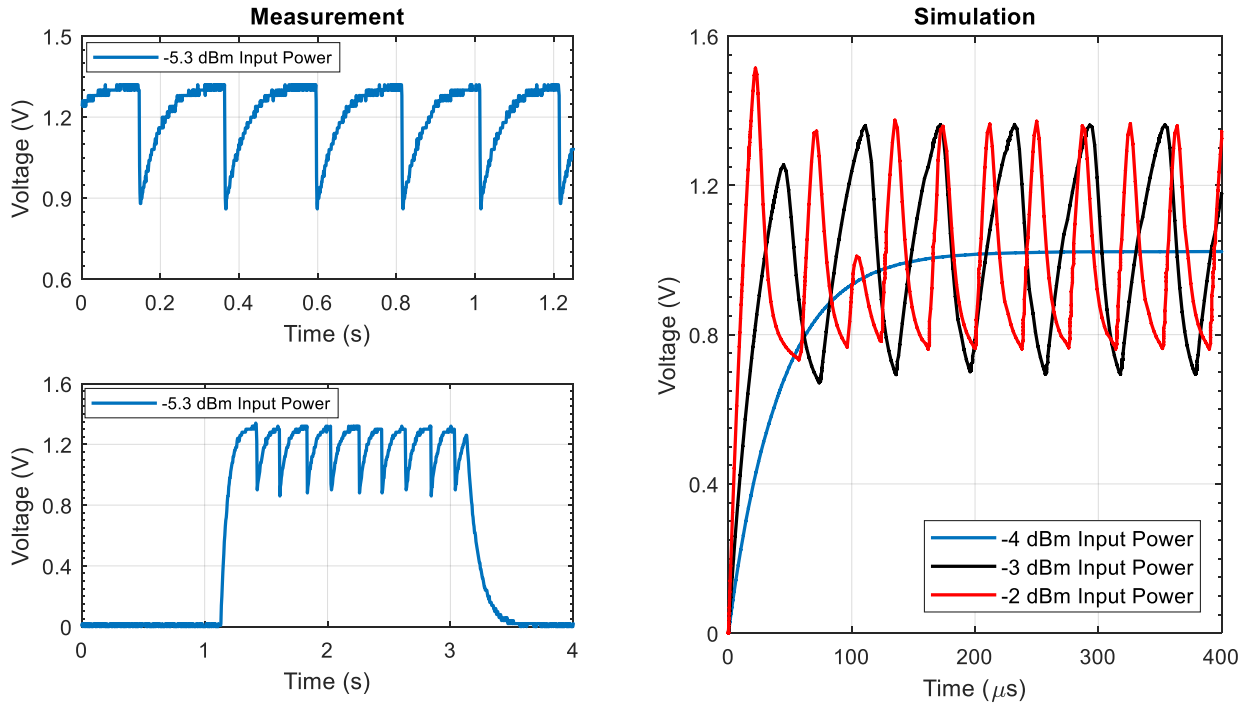

Figure 4-11. Measurement and Simulation Results of Design 4

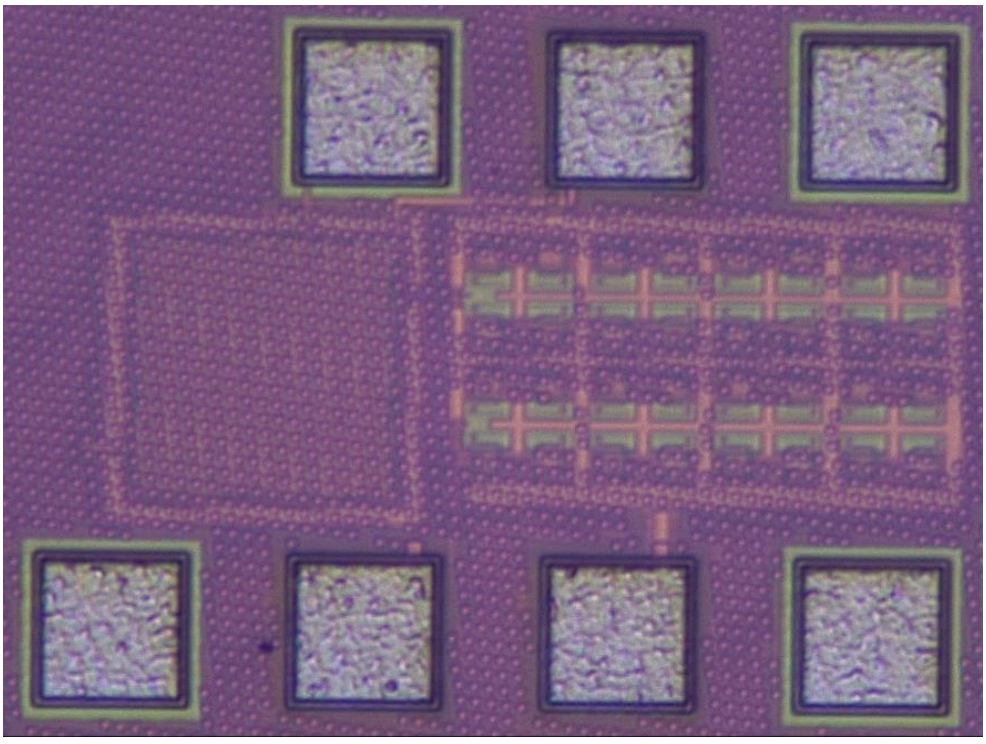

Figure 4-12. Design 4 Micrograph

4.2.5 Design 5: 16 Stages Energy Harvester Design

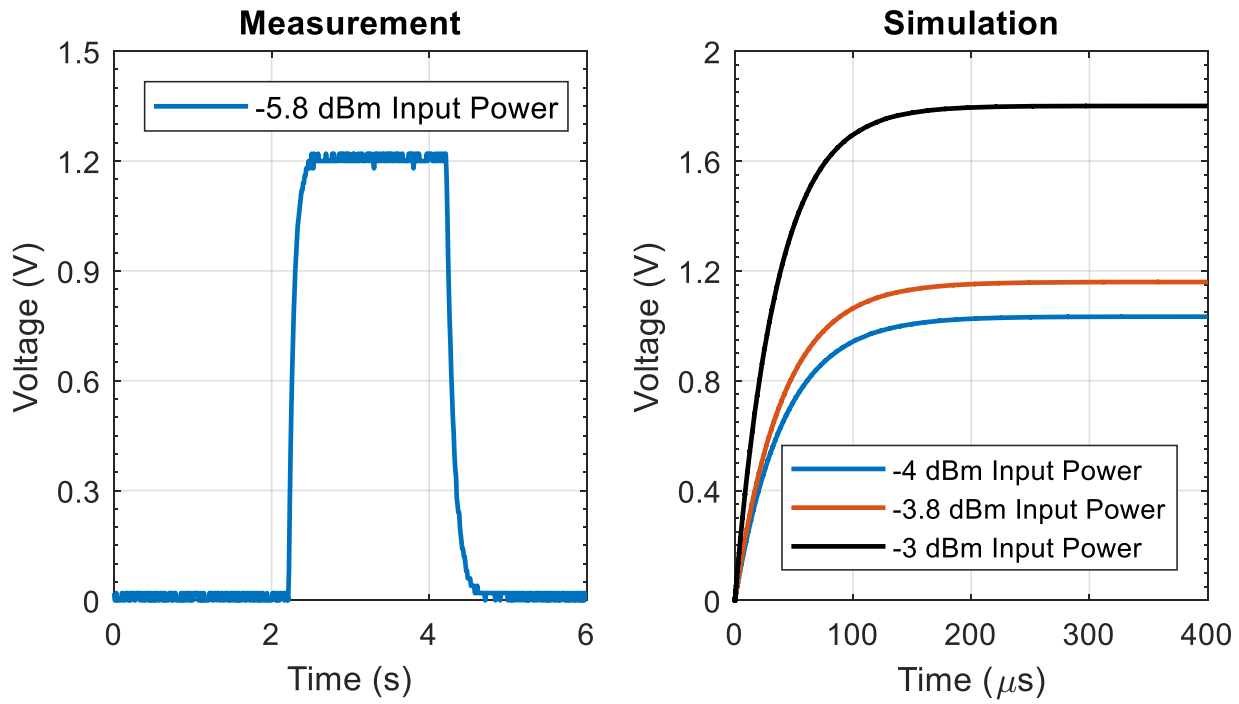

Figure 4-13. Measurement and Simulation Output Transient Voltage Waveforms of Design 5

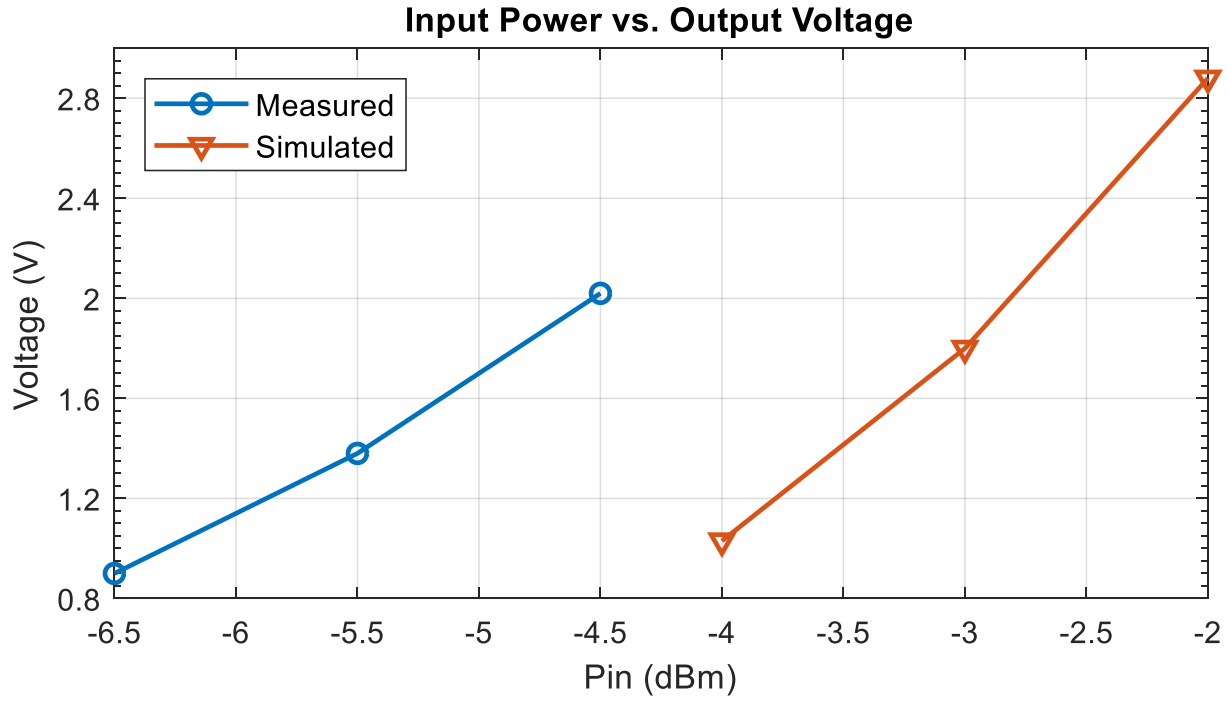

Figure 4-14. Measurement and Simulation Input Power vs. Voltage Levels of Design 5

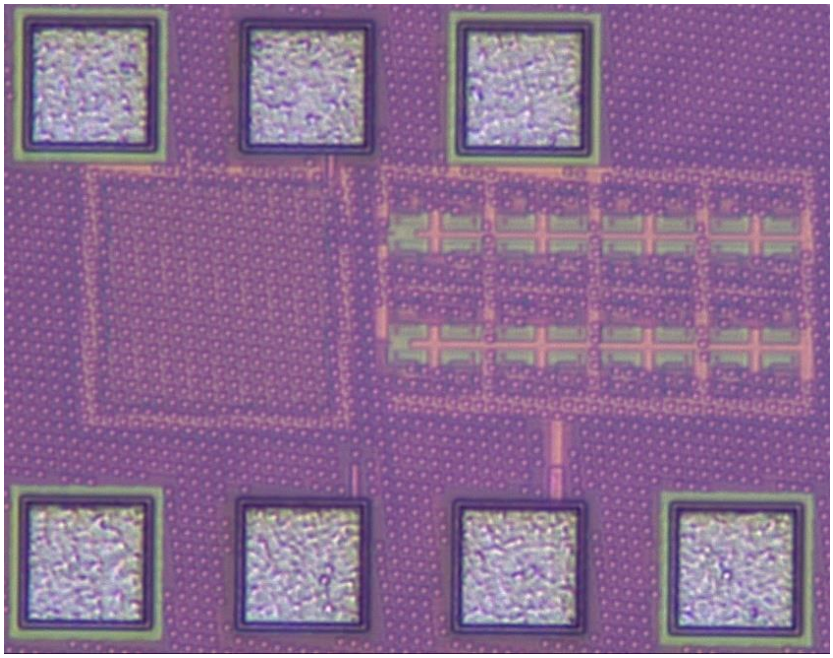

Figure 4-15. Design 5 Micrograph

4.2.6 Design 6: 32 Stages Energy Harvester Design Using Low Threshold Transistors with PMU and Threshold Compensation

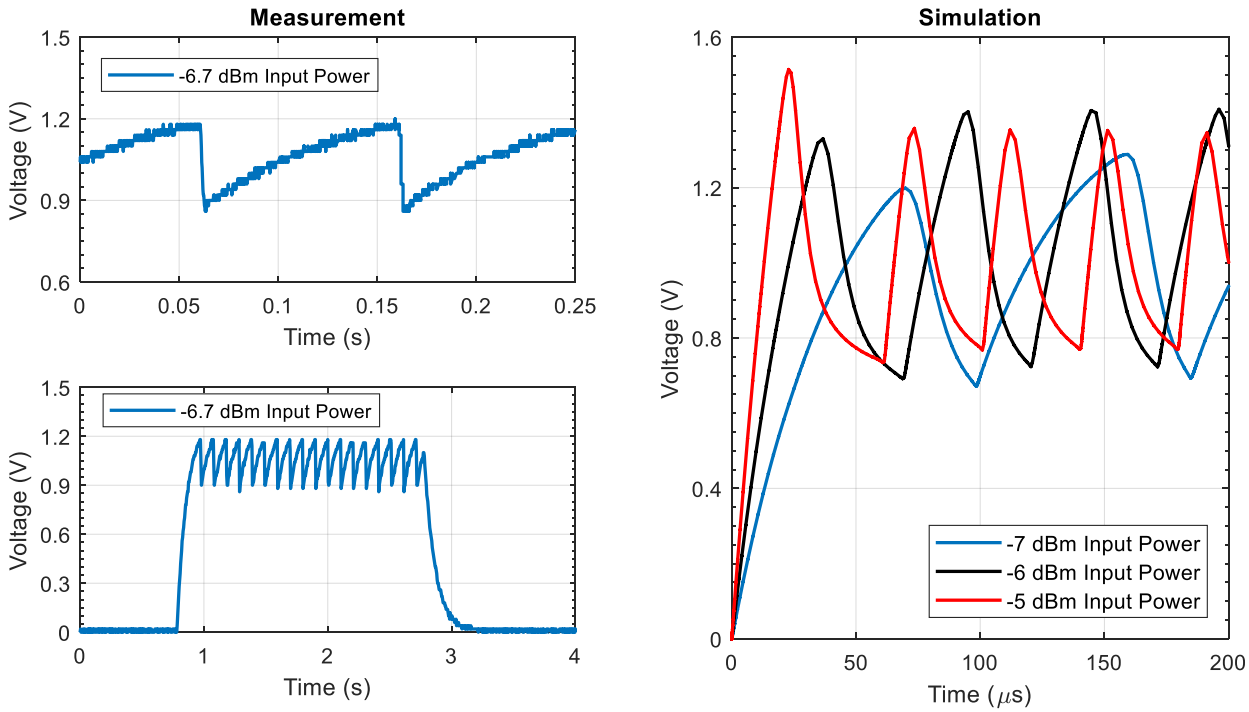

Figure 4-16. Measurement and Simulation Results of Design 6

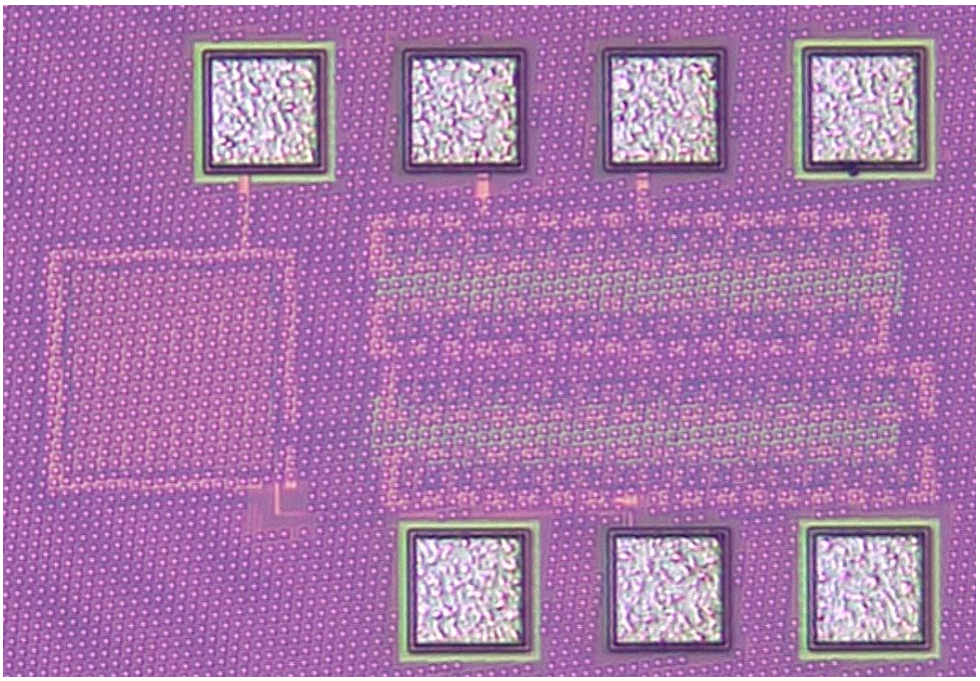

Figure 4-17. Design 6 Micrograph

4.2.7 Design 7: 32 Stages Energy Harvester Design Using Low Threshold Transistors with Threshold Compensation

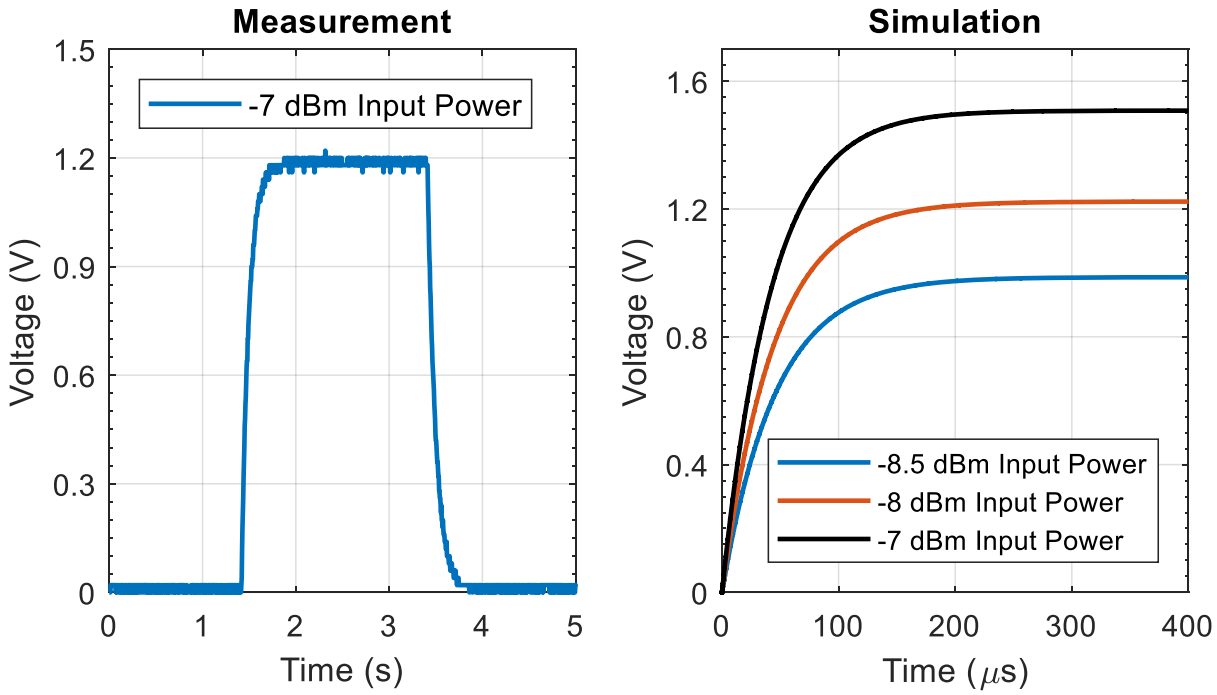

Figure 4-18. Measurement and Simulation Output Transient Voltage Waveforms of Design 7

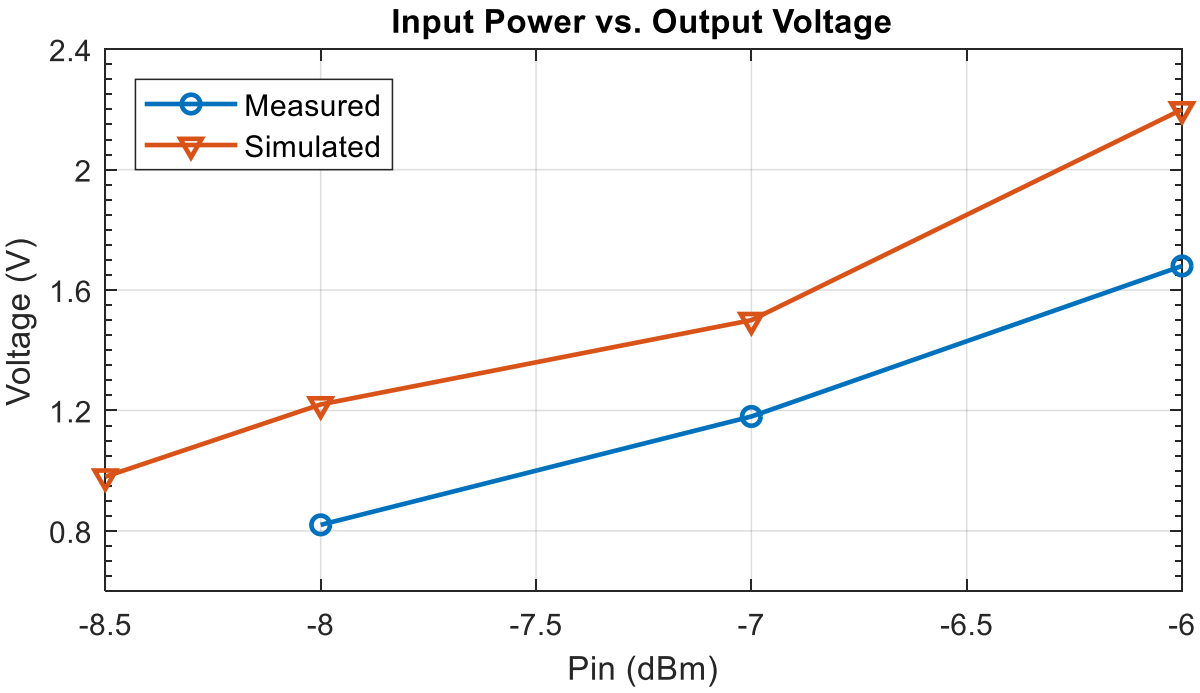

Figure 4-19. Measurement and Simulation Input Power vs. Voltage Levels of Design 7

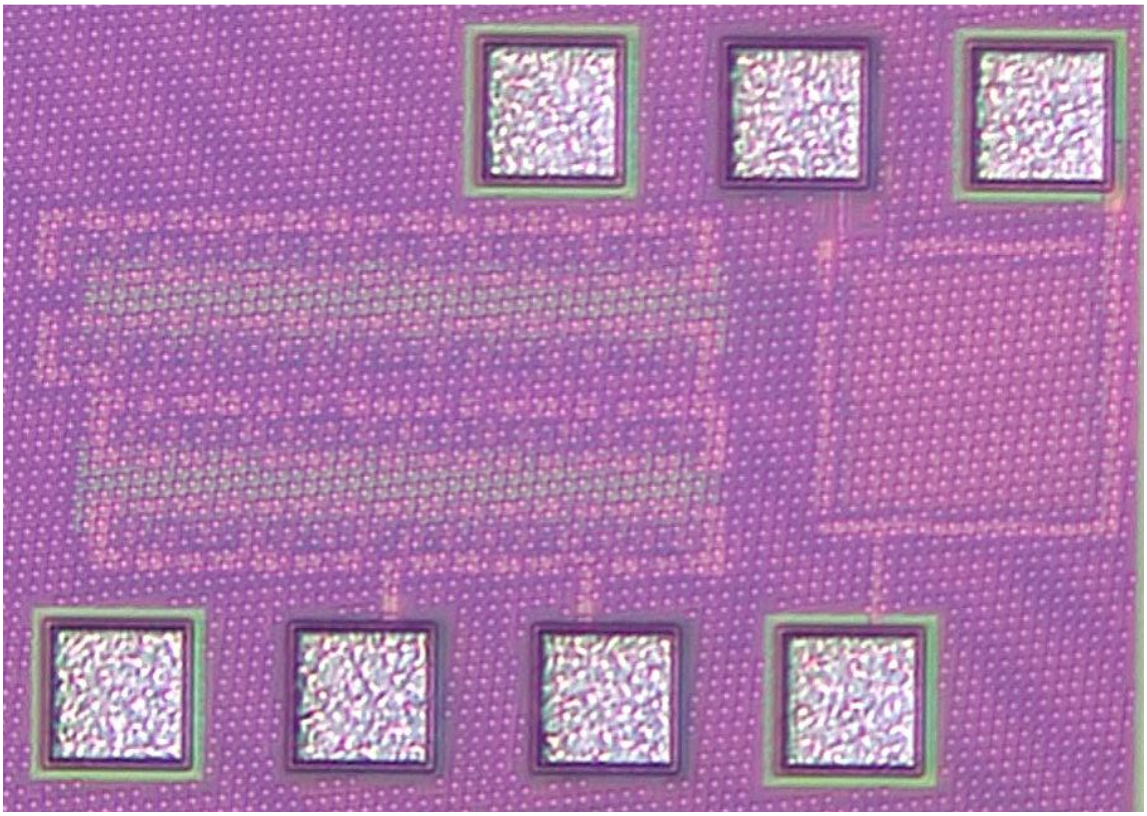

Figure 4-20. Design 7 Micrograph

4.2.8 Design 8: 64 Stages Energy Harvester Design

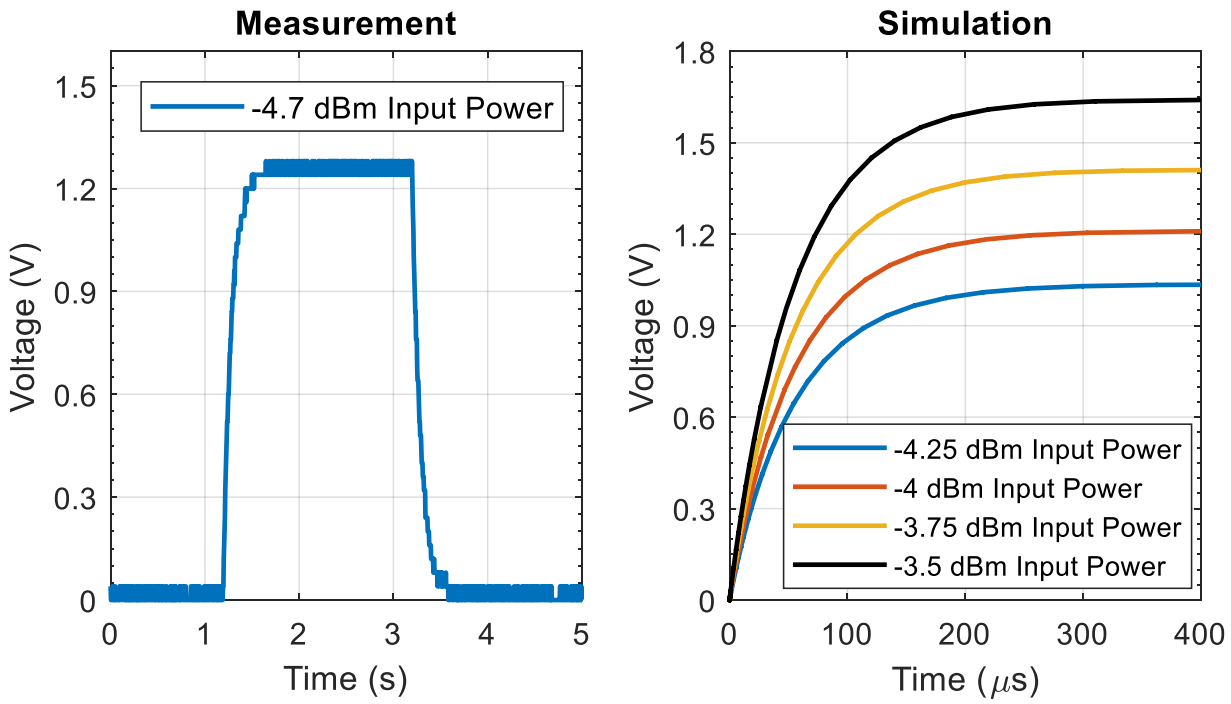

Figure 4-21. Measurement and Simulation Output Transient Voltage Waveforms of Design 8

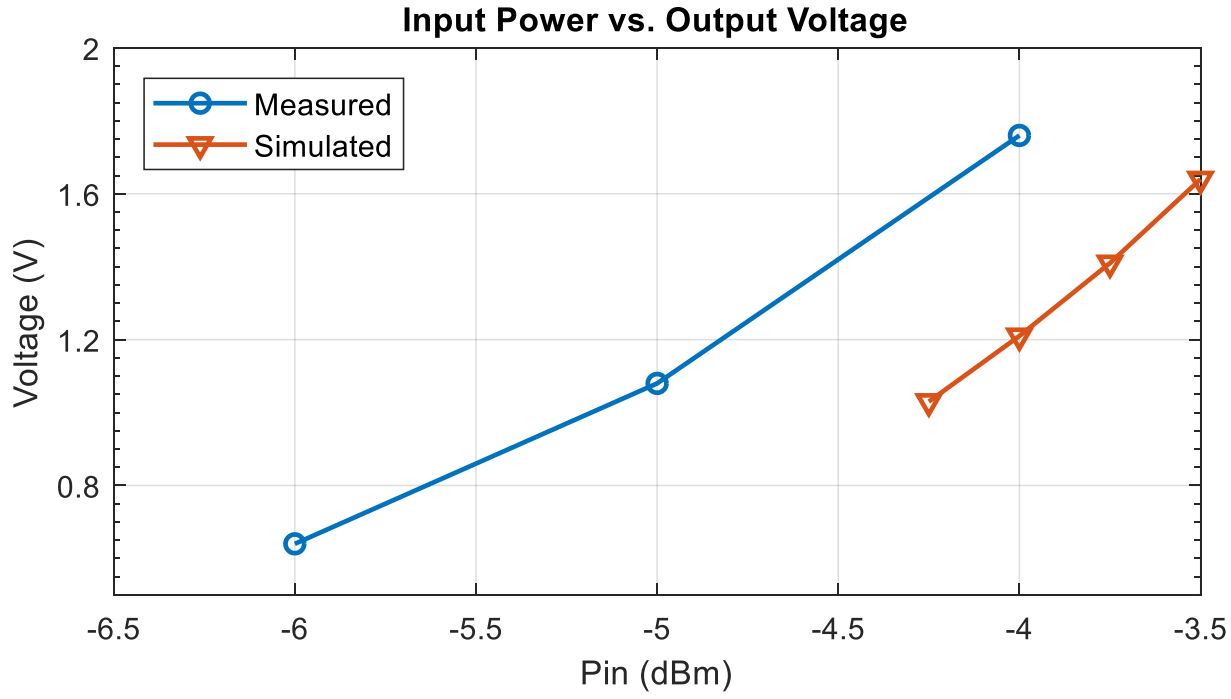

Figure 4-22. Measurement and Simulation Input Power vs. Voltage Levels of Design 8

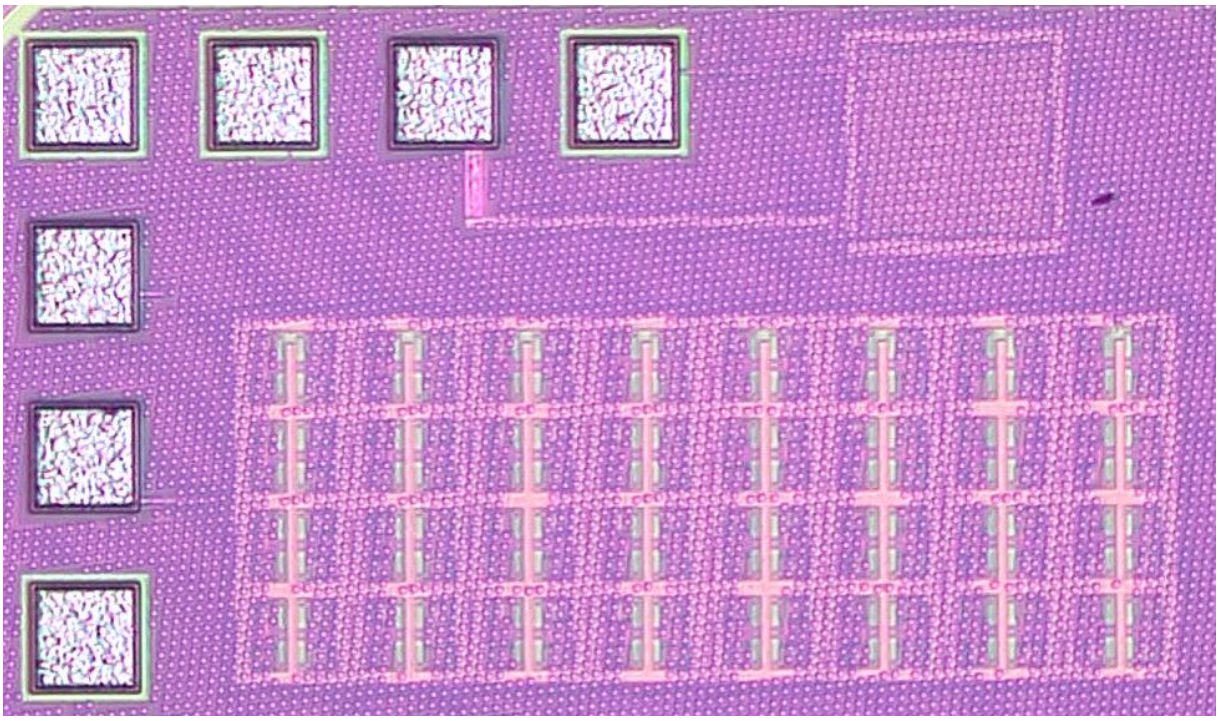

Figure 4-23. Design 8 Micrograph

4.2.9 Design 9: 6 Stages Energy Harvester Design with PMU

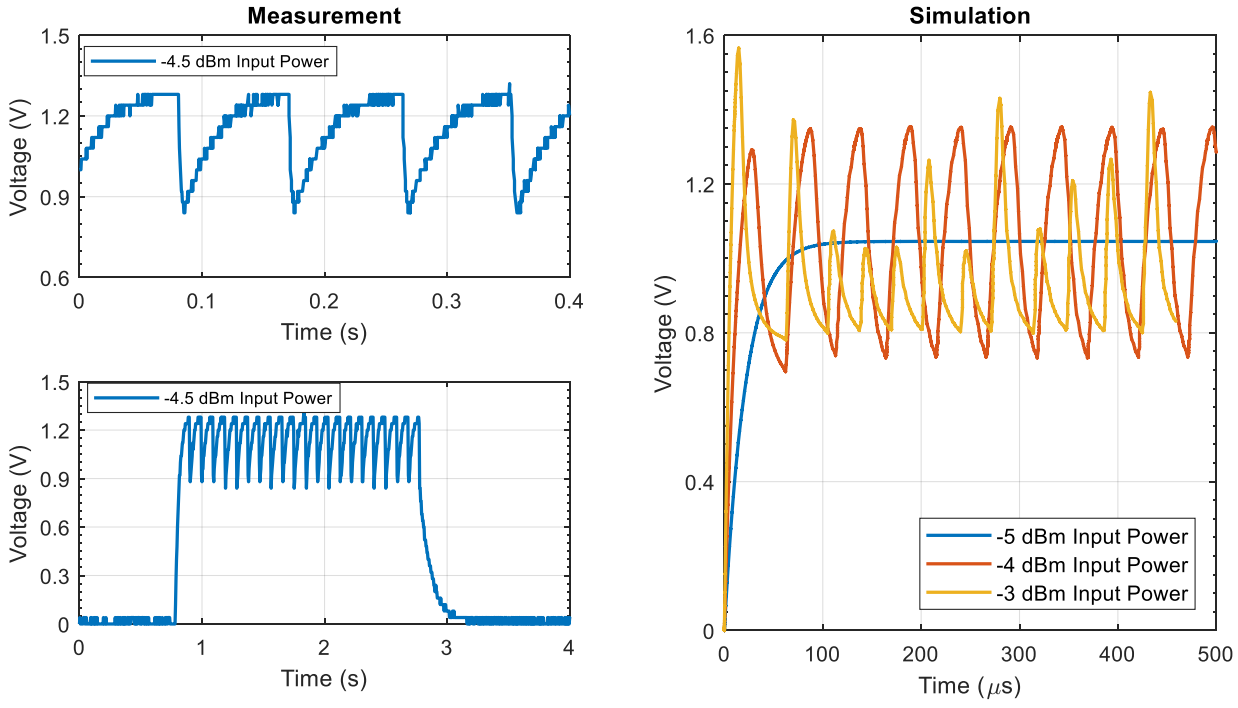

Figure 4-24. Measurement and Simulation Results of Design 9

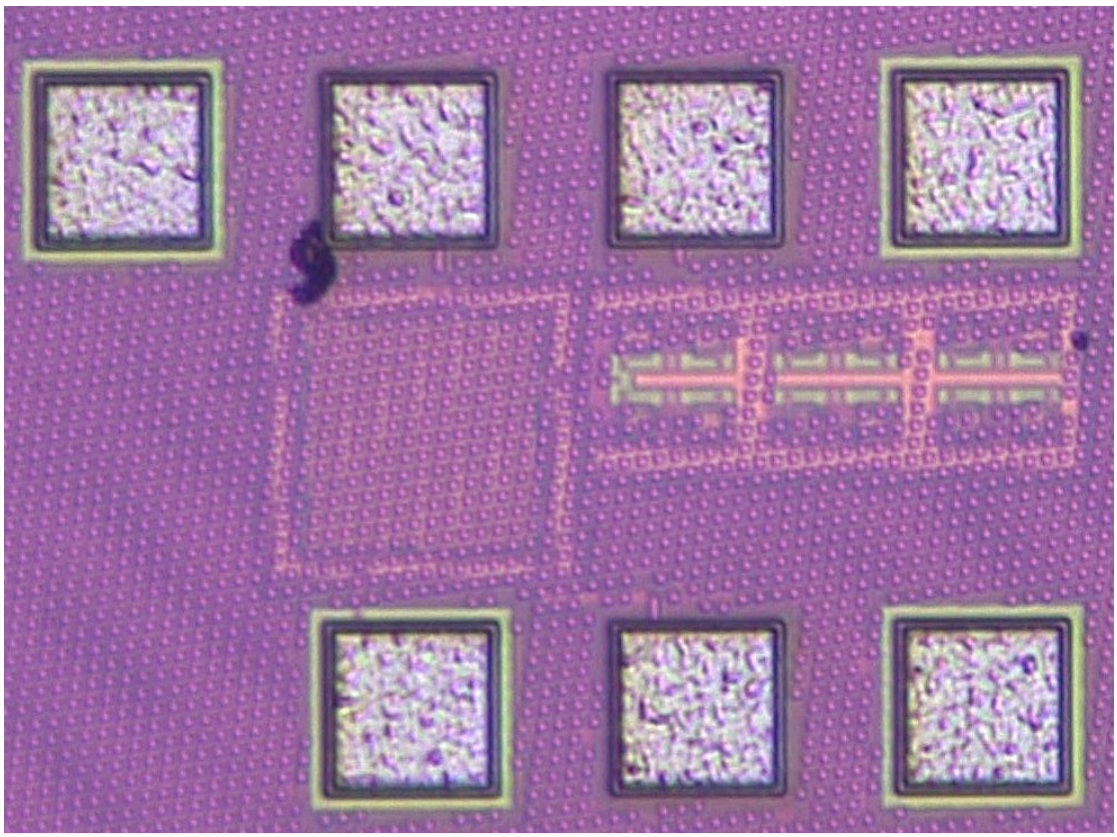

Figure 4-25. Design 9 Micrograph

4.2.10 Results Summary

This section summarizes the obtained results and gives expected results for complete energy harvester that includes a conjugately matched antenna based on the calculations and simulation results since the measured and simulated performance match well. Figure 4-27 illustrates the setup that simulations are based on while the calculations are based on Equation 3-4. Table 4-2 shows the measured and simulated input impedances for each design at their design frequencies along with the measured and simulated necessary input power from a 50 Ω signal generator to achieve 1.2 V DC output voltage. The measured values are after the loss of the adapters, cables and DC blocks are taken into account. The total loss due to them is 2.5 dB.

Table 4-2. Measured and Simulated Input Impedances at Design Frequencies and Sensitivity Values for 1.2 V Output Voltage After Loss Calibrations

Design Number	Measured Impedance	Simulated Impedance	Measured Sensitivity	Simulated Sensitivity
D_1	10 - j1120 Ω	7.65 - j1143 Ω	-4.5 dBm	-3 dBm
D_2	10 - j1150 Ω	7.66 - j1165 Ω	-5 dBm	-2.75 dBm
D_3	11 - j922 Ω	9.45 - j1019 Ω	-6.2 dBm	-5.2 dBm
D_4	12.5 - j496 Ω	11.8 - j452 Ω	-5.3 dBm	-3 dBm
D_5	11.8 - j492 Ω	10.7 - j450 Ω	-5.8 dBm	-3.8 dBm
D_6	45 - j220 Ω	37 - j396 Ω	-6.7 dBm	-6.5 dBm
D_7	46 - j220 Ω	37 - j396 Ω	-7 dBm	-7.5 dBm
D_8	25 - j152 Ω	22 - j169 Ω	-4.7 dBm	-3.7 dBm
D_9	12.5 - j496 Ω	13.9 - j562 Ω	-4.5 dBm	-4 dBm

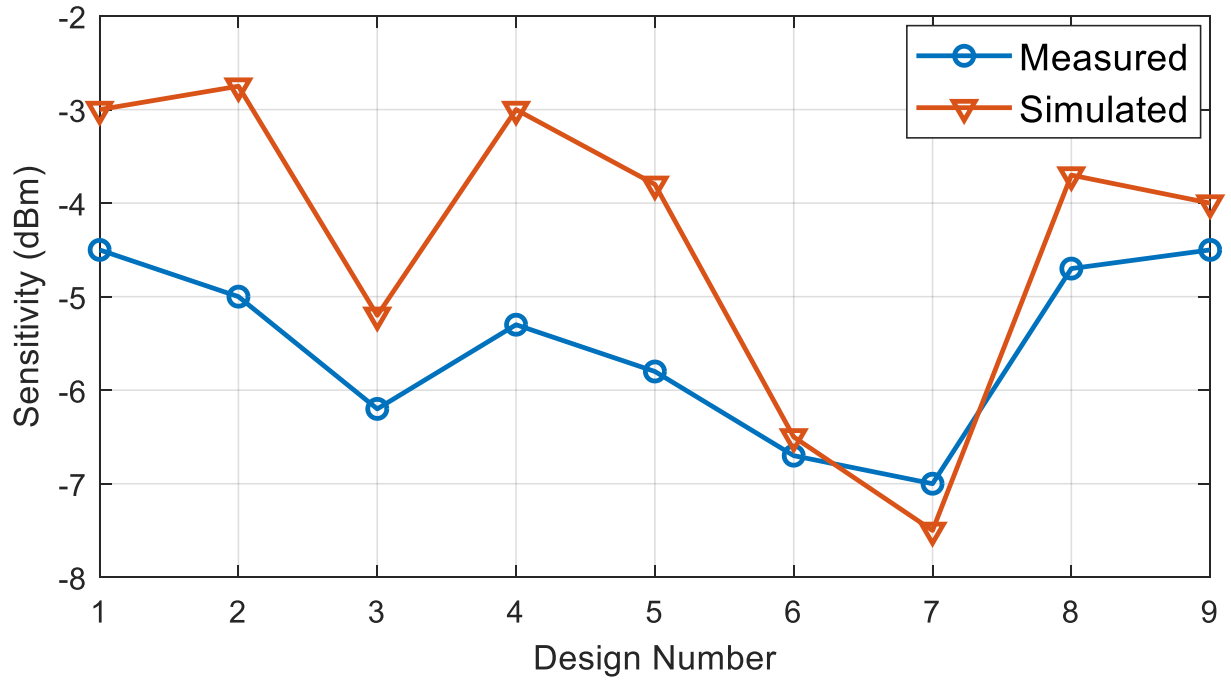

Figure 4-26. Measured and Simulated Sensitivity Values for 1.2 V Output Voltage After Loss Calibration based on 50 Ω Single Ended Input Source and Balun Setup

Table 4-3. Energy Harvester with a Conjugately Matched Antenna Simulated and Calculated Sensitivity Values for Different Load Conditions

Design Number	Simulated (Rload = ∞)	Calculated (Rload = ∞)	Simulated (Rload = 1 MΩ)
D_1^*	-34.5 dBm	-36.5 dBm	-20 dBm
D_2	-38 dBm	-38.6 dBm	-20.5 dBm
D_3	-35 dBm	-36.6 dBm	-22.5 dBm
D_4^*	-27.5 dBm	-27.8 dBm	-19 dBm
D_5	-32 dBm	-32.55 dBm	-20 dBm
D_6^*	-26 dBm	-26.5 dBm	-17 dBm
D_7	-28 dBm	-28.5 dBm	-18 dBm
D_8	-28 dBm	-28.5 dBm	-11.5 dBm
D_9^*	-27 dBm	-27 dBm	-21 dBm

In Table 4-3, those of the designs that have '*' sign include PMU that also presents a load to the rectifier while drawing current. The simulated PMU load is 1 MΩ when it is on and 130 MΩ when it is off. Therefore, the equivalent load resistance equals to parallel combination of the PMU load and the external 1 MΩ resistance.

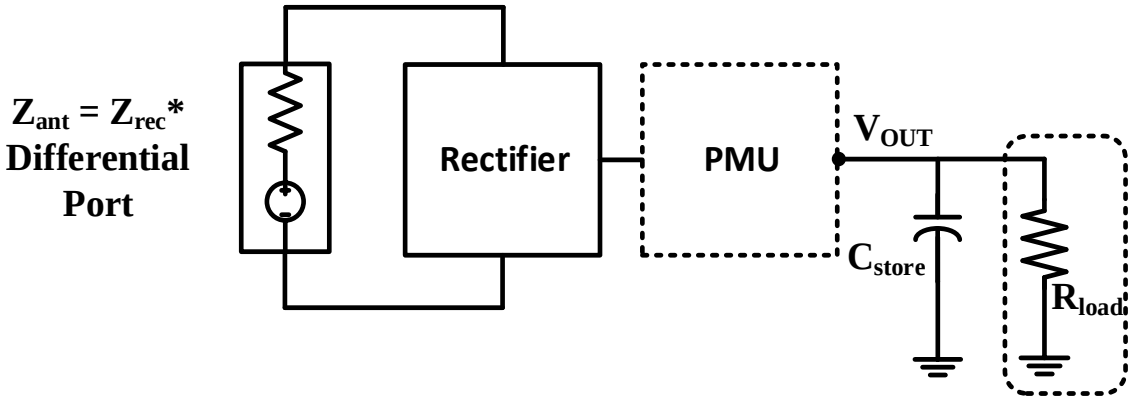

Figure 4-27. Simulation Setup for Rectifier and Antenna Conjugately Matched Energy Harvesters

5 SUMMARY AND CONCLUSIONS

In this thesis, 915 MHz and 2.4 GHz energy harvester building blocks are investigated. The design and co-optimization of the blocks are introduced. It has been stressed multiple times that the antenna and the rectifier interface is crucial. Similarly, a power management unit is co-designed with the rectifier and the load to optimize the overall performance. Several rectifier topologies in the literature are analyzed, the employed ones are further discussed. Differential drive topology is found to be superior to others while a self-compensation technique is used in two of the fabricated designs. The design parameters such as transistor sizing, number of stages and the rectifier input impedance are discussed in detail.

Simulation and measurement results are provided. The current design does not include an attached antenna. Therefore, the measurements are performed by using a 50 Ω signal generator connected to a balun to create a differential input signal. The measurement and simulation setups are given in section 4.1. Based on the current setups, the simulation and measurement results are in good agreement indicating that the complete energy harvester that includes a conjugately matched antenna should perform similar to simulations as well.

The future work includes the measurements with an attached antenna. The expected complete energy harvester results, based on the calculations and the simulation results, are given in Table 4-3.

APPENDIX

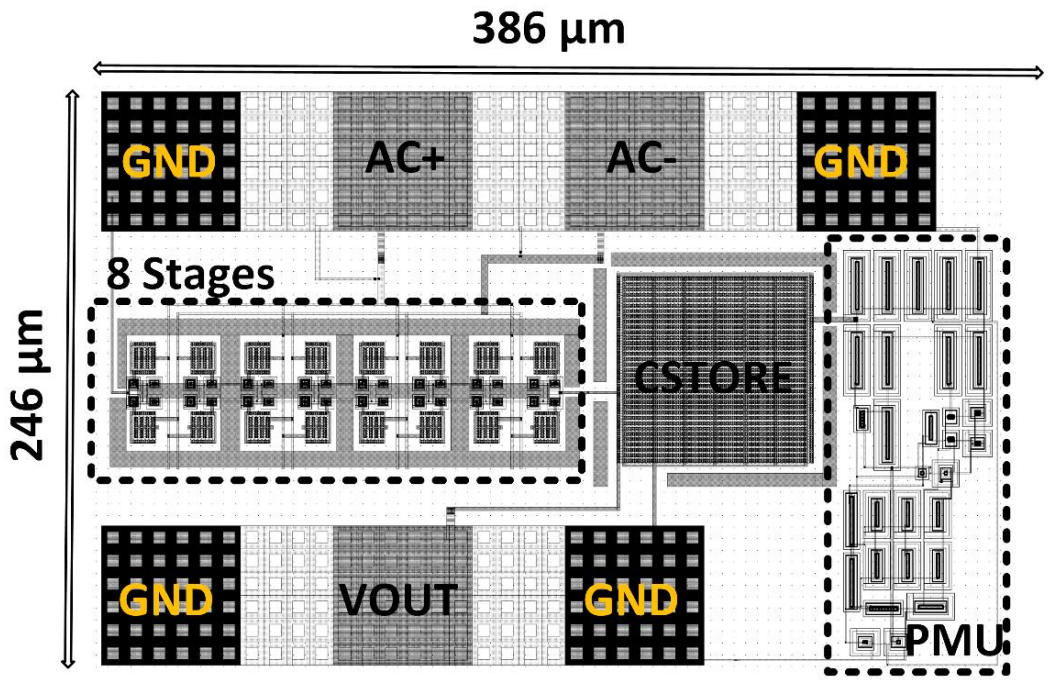

Figure A-1. Layout of Design 1

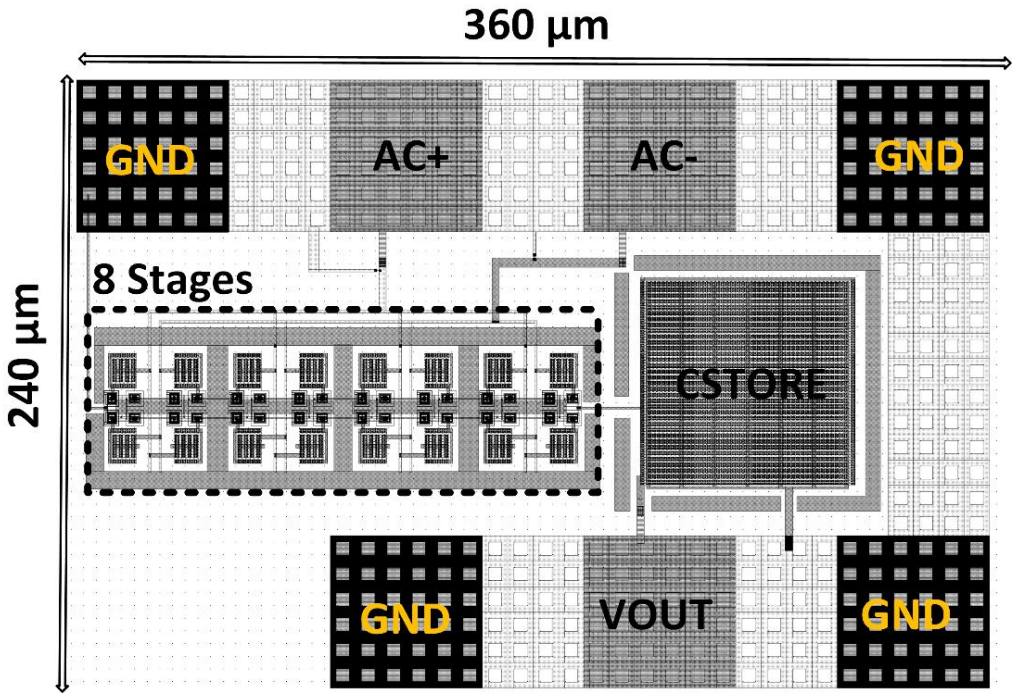

Figure A-2. Layout of Design 2

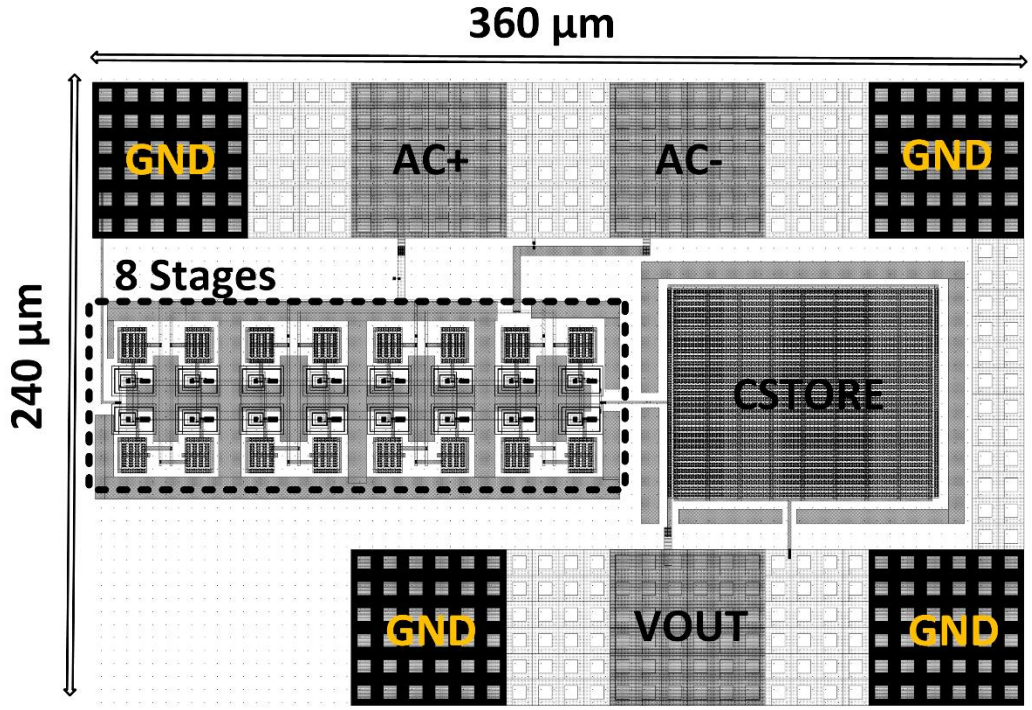

Figure A-3. Layout of Design 3

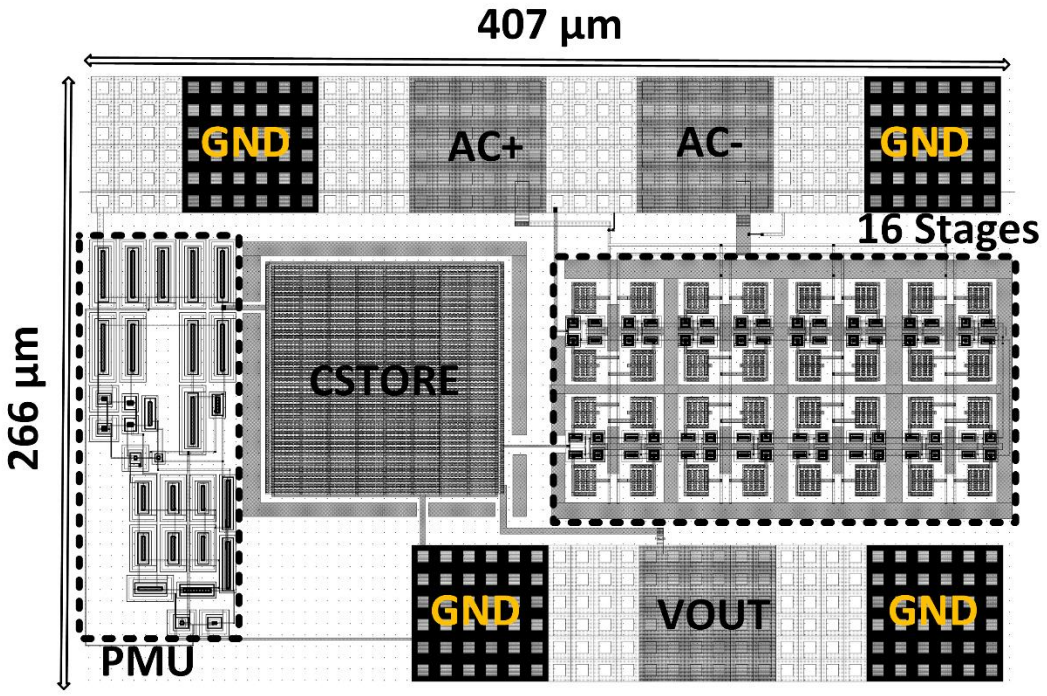

Figure A-4. Layout of Design 4

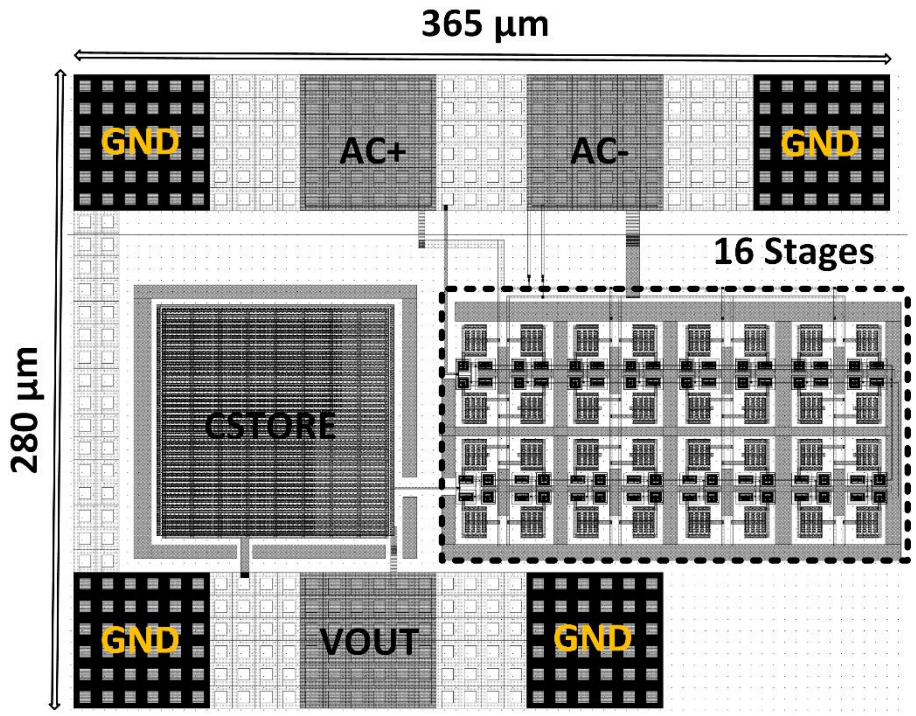

Figure A-5. Layout of Design 5

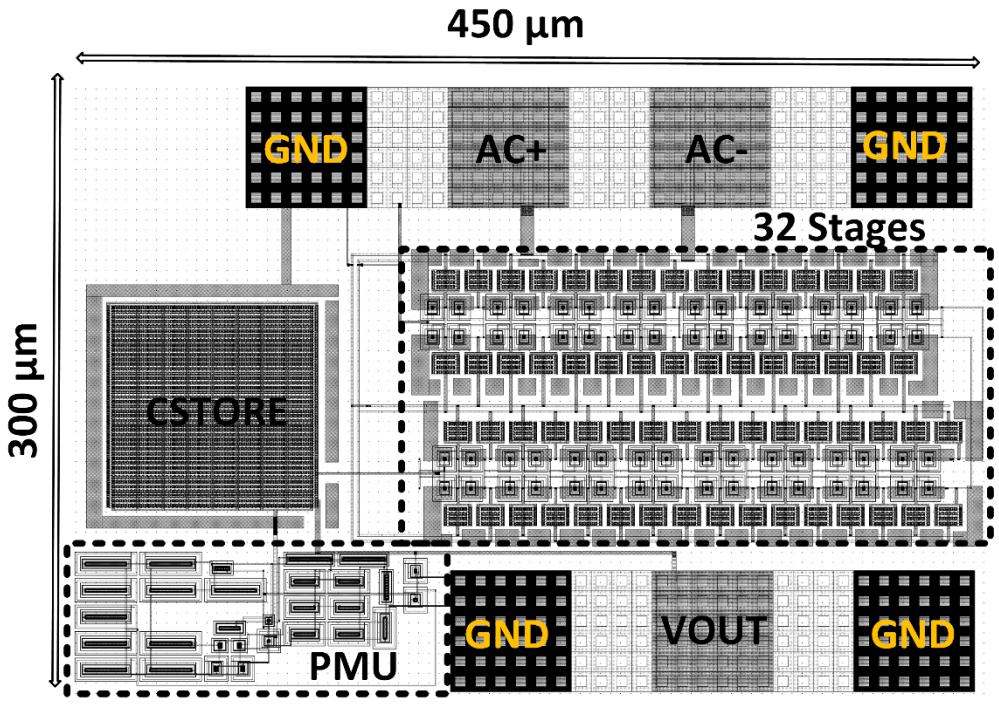

Figure A-6. Layout of Design 6

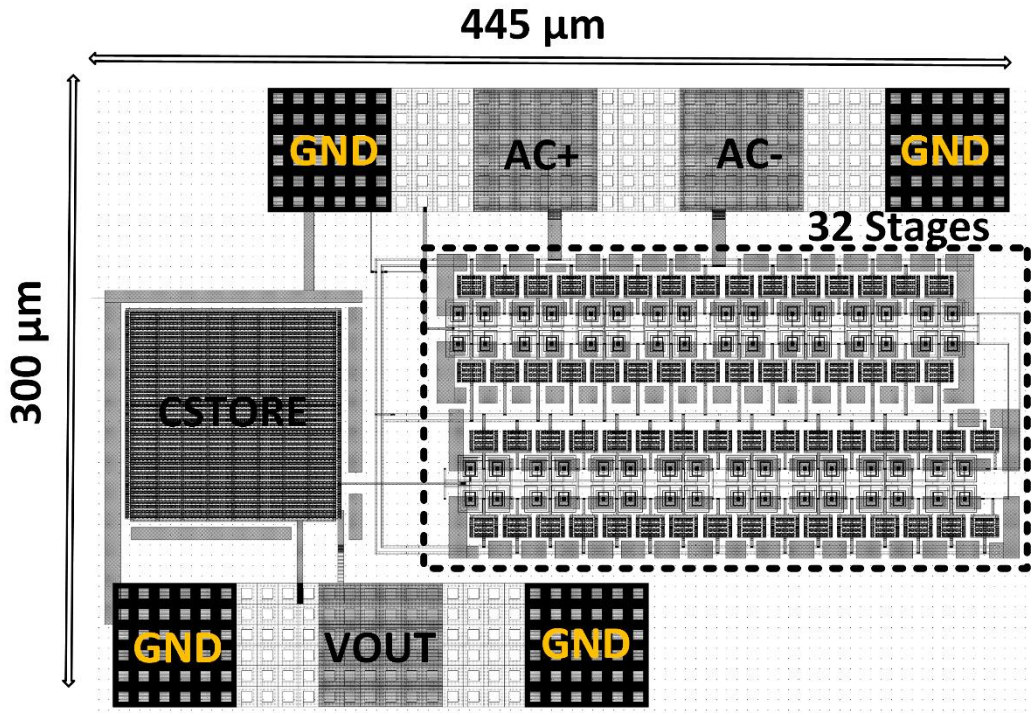

Figure A-7. Layout of Design 7

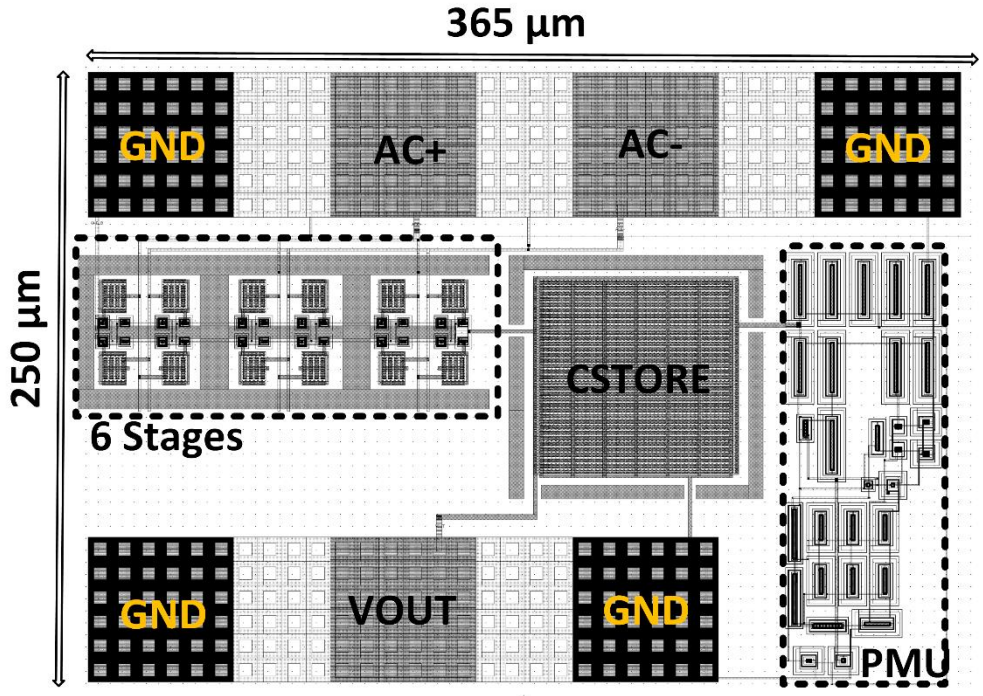

Figure A-8. Layout of Design 9

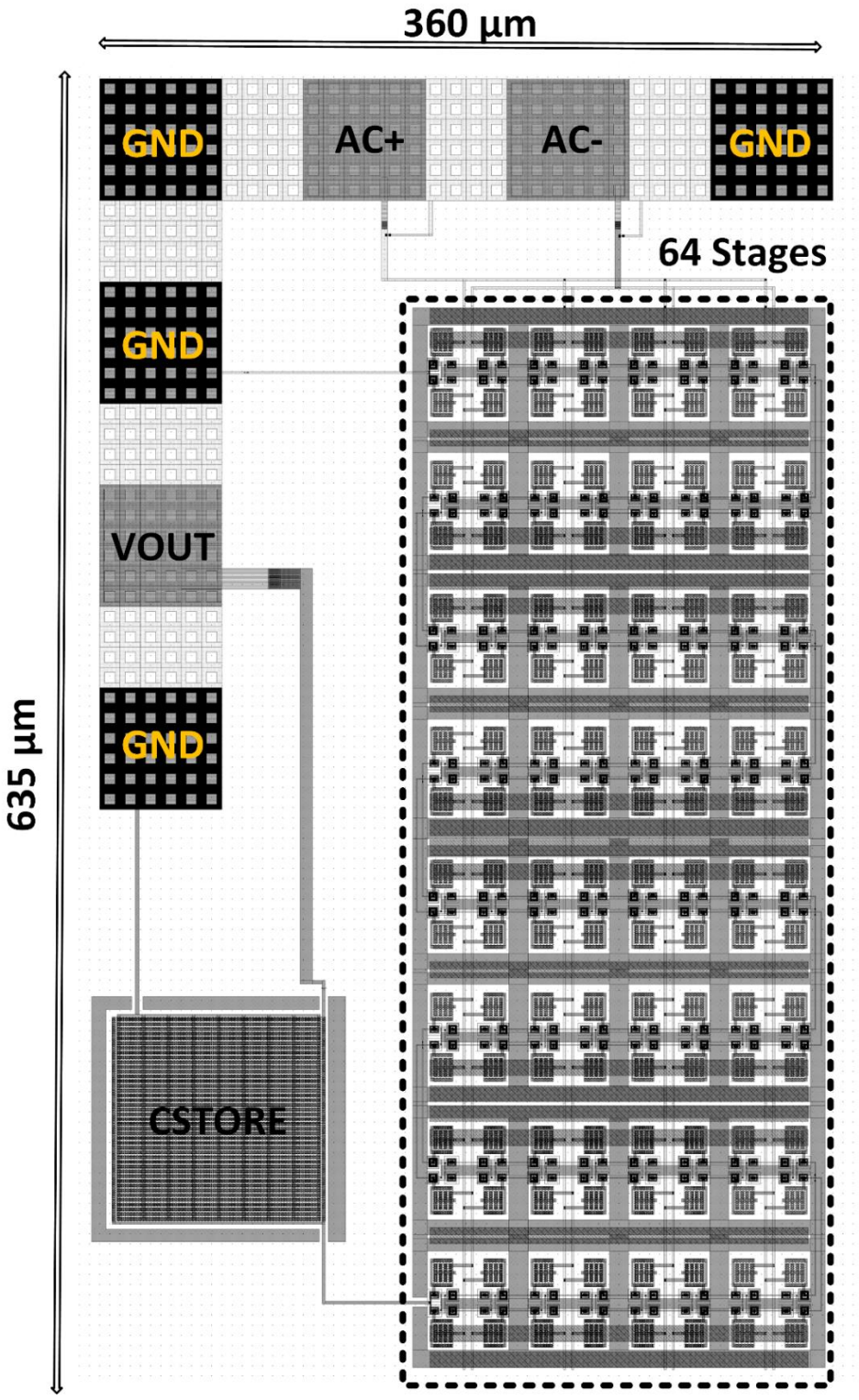

Figure A-9. Layout of Design 8

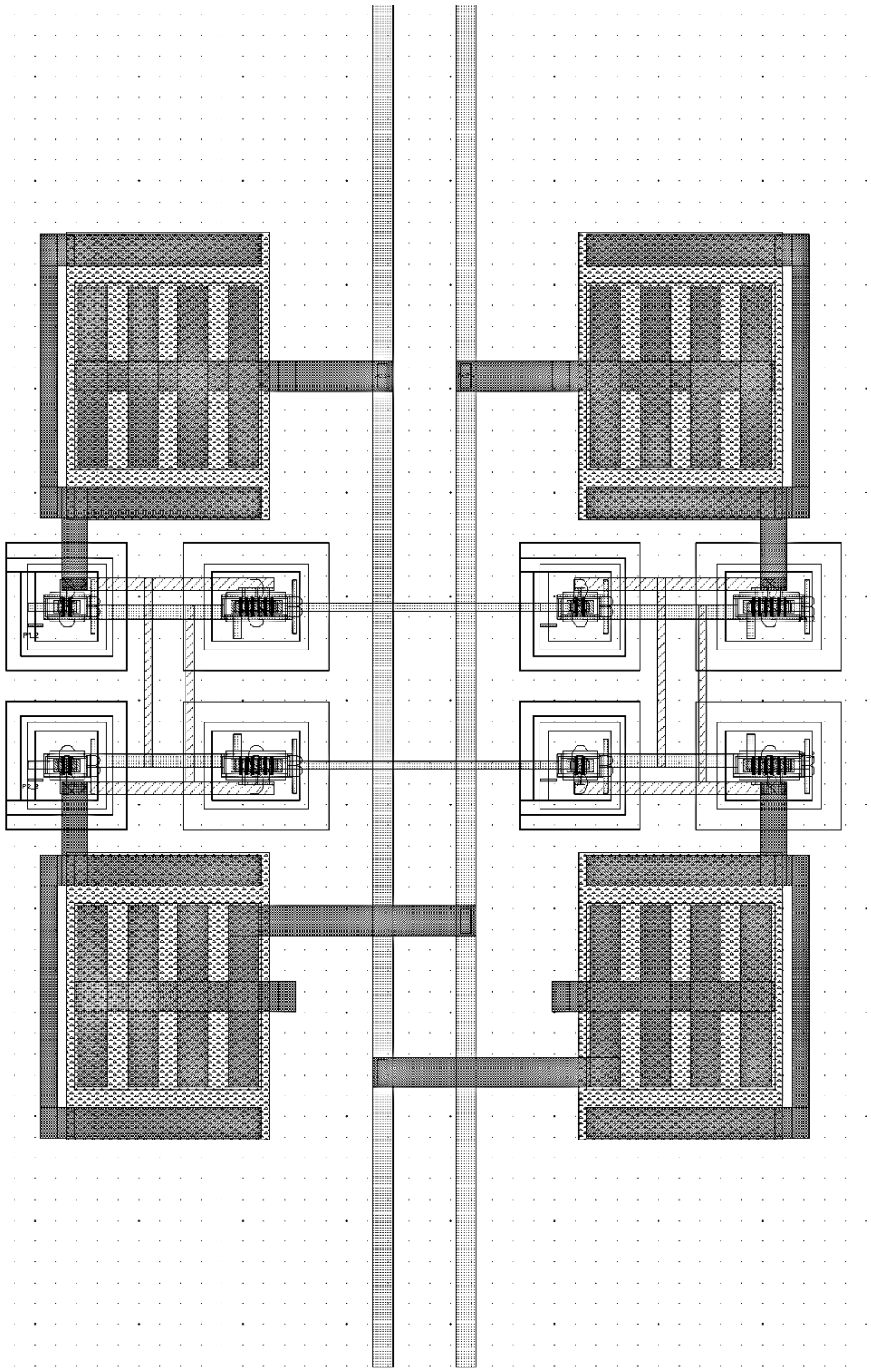

Figure A-10. Layout of a Two-Stage Rectifier

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